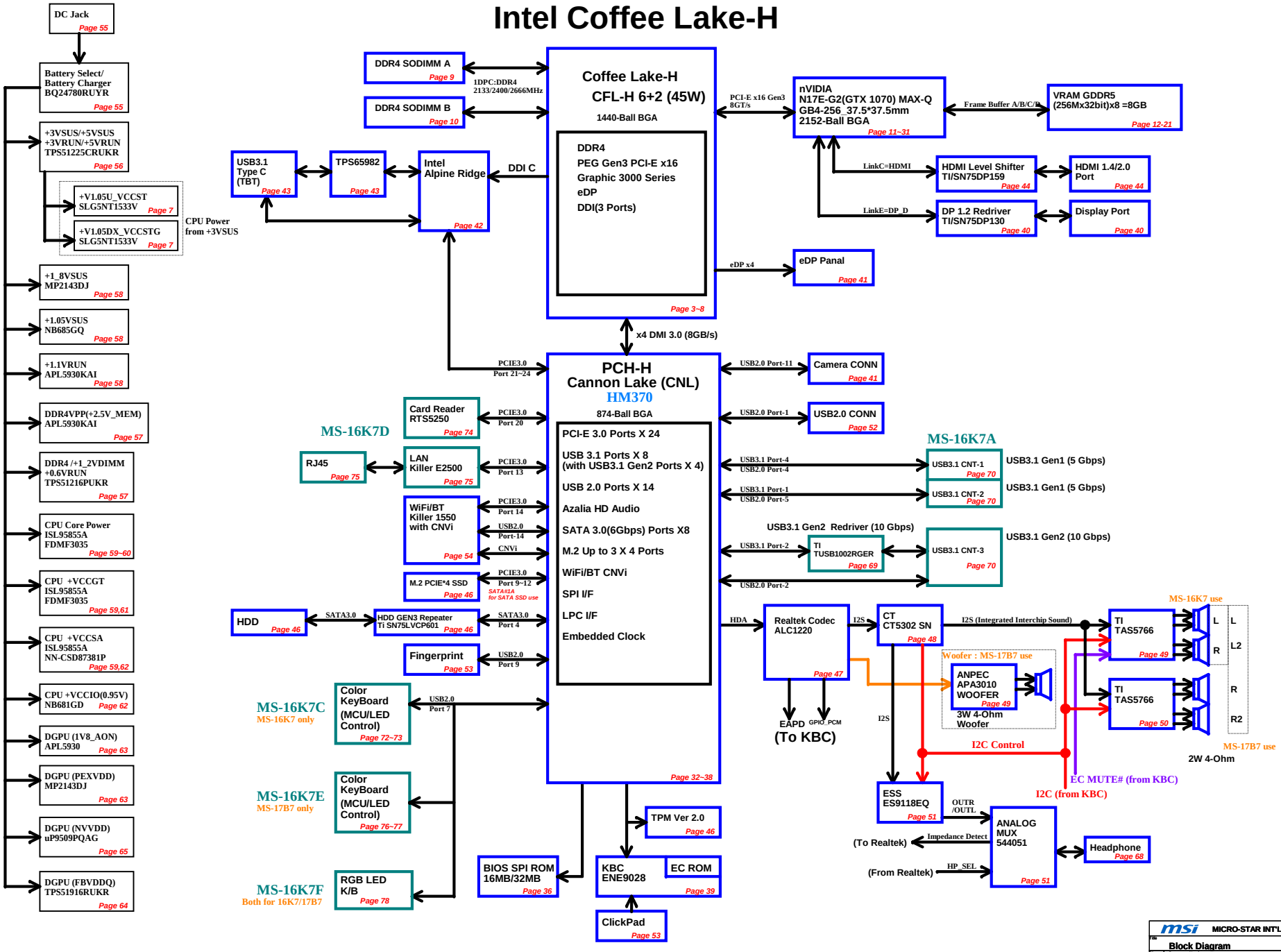
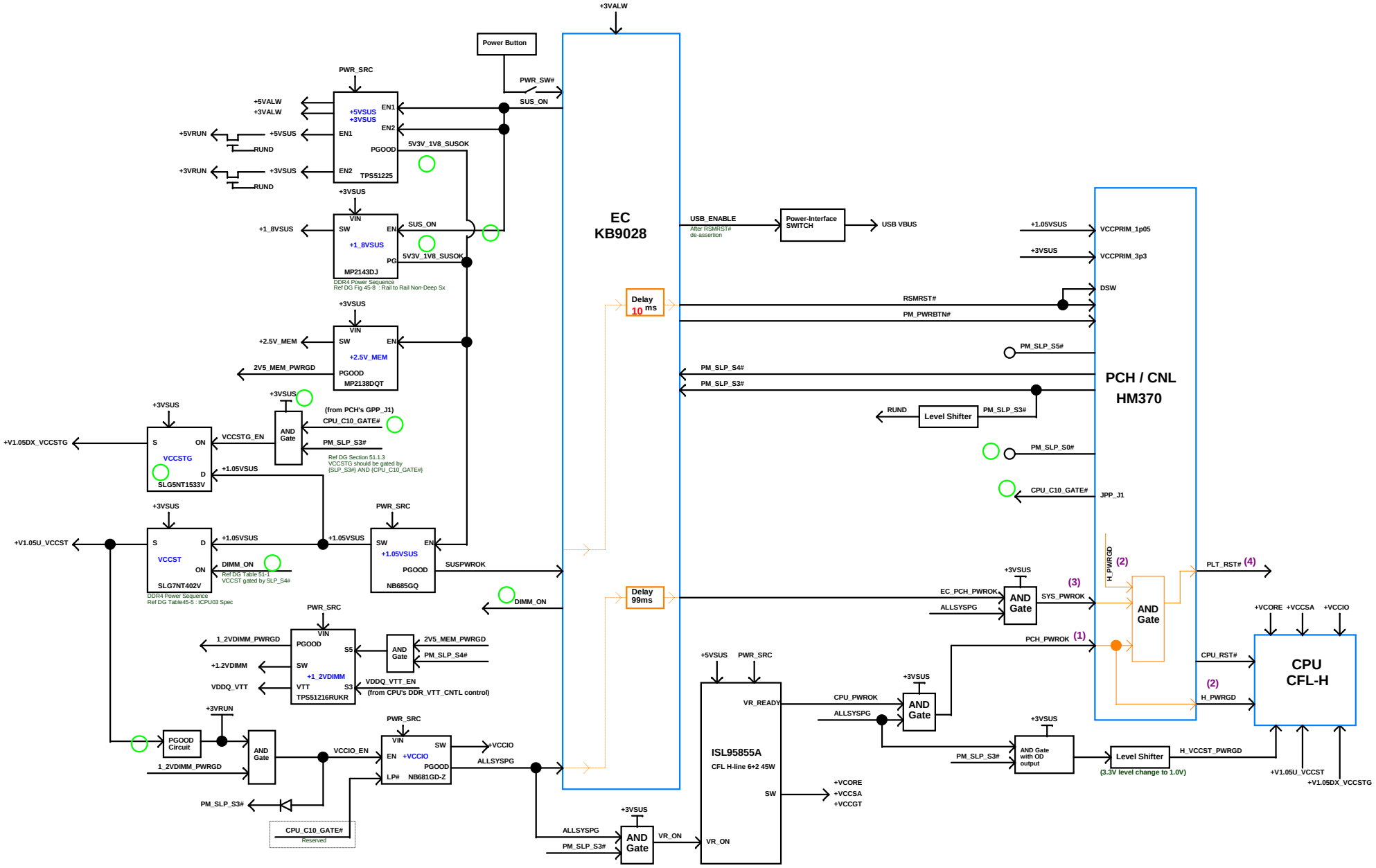
MS-16K7/17B7 Ver : 10



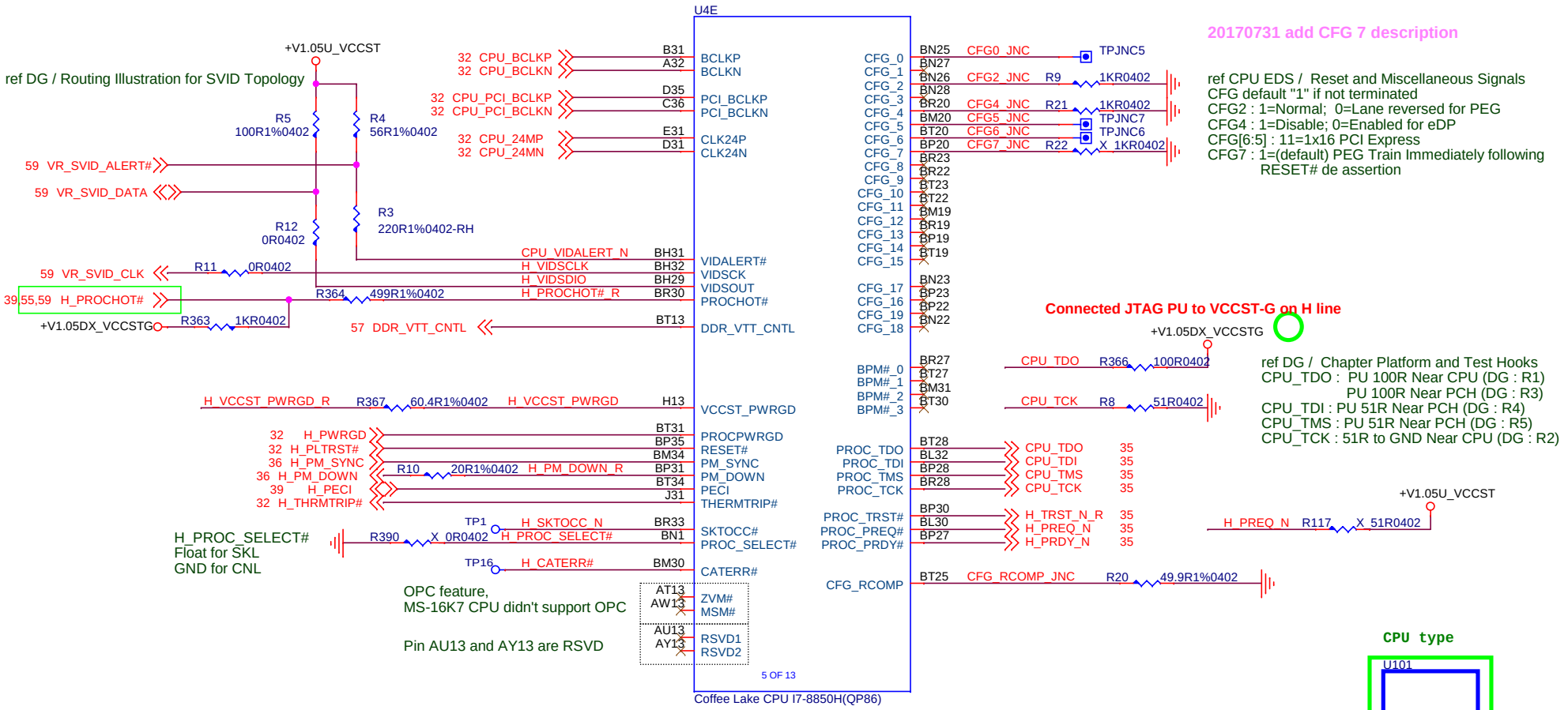
MS-16K7 : CFL-H Mobile Power on Block Diagram

ref DG Chapter45 Power Sequencing Spec

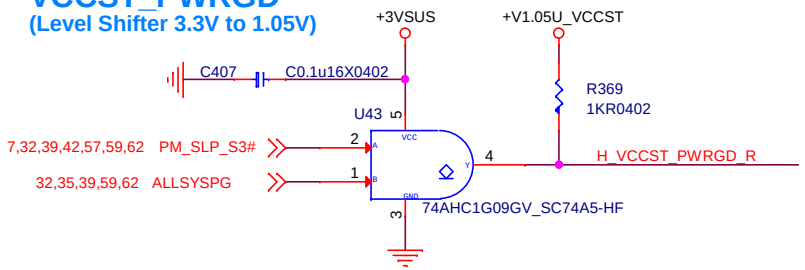


msi	MICRO-STAR INT'L CO.,LTD.		
Title	Power ON Block Diagram		
Size	Document Number		Rev
Custom	MS-16K7		10
Date:	Sheet 2 of 88		

CFL-H (HOST)



VCCST_PWRGD
(Level Shifter 3.3V to 1.05V)



74AHC1G09GV is AND Gate with open drain output

MICRO-STAR INT'L CO.,LTD.		
Title: CFL-H(HOST)		
Size: Custom	Document Number: MS-16K71	Rev: 10
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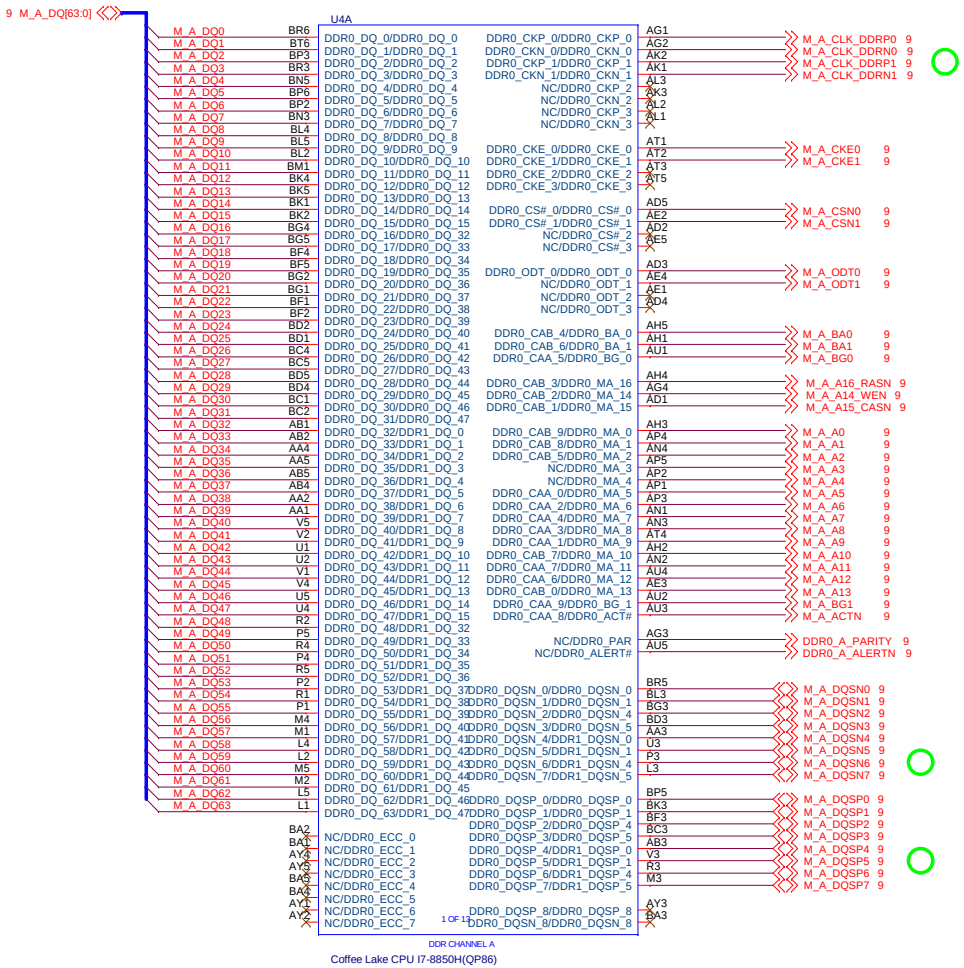
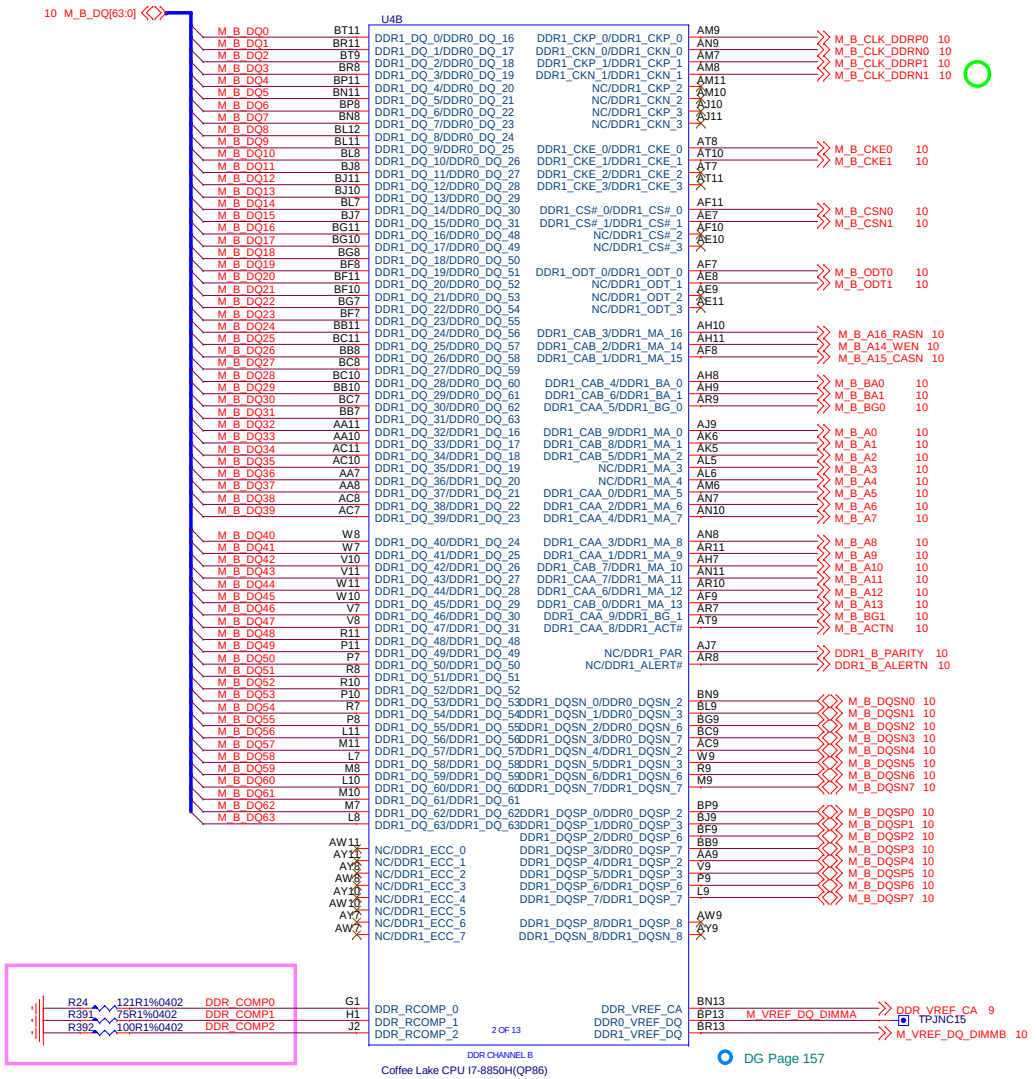
DDR Channel A



DDR Channel B



DG Page 157

20170731 the three Resistance close CPU

MICRO-STAR INT'L CO.,LTD.			
Title: CFL-H(DDR4)			
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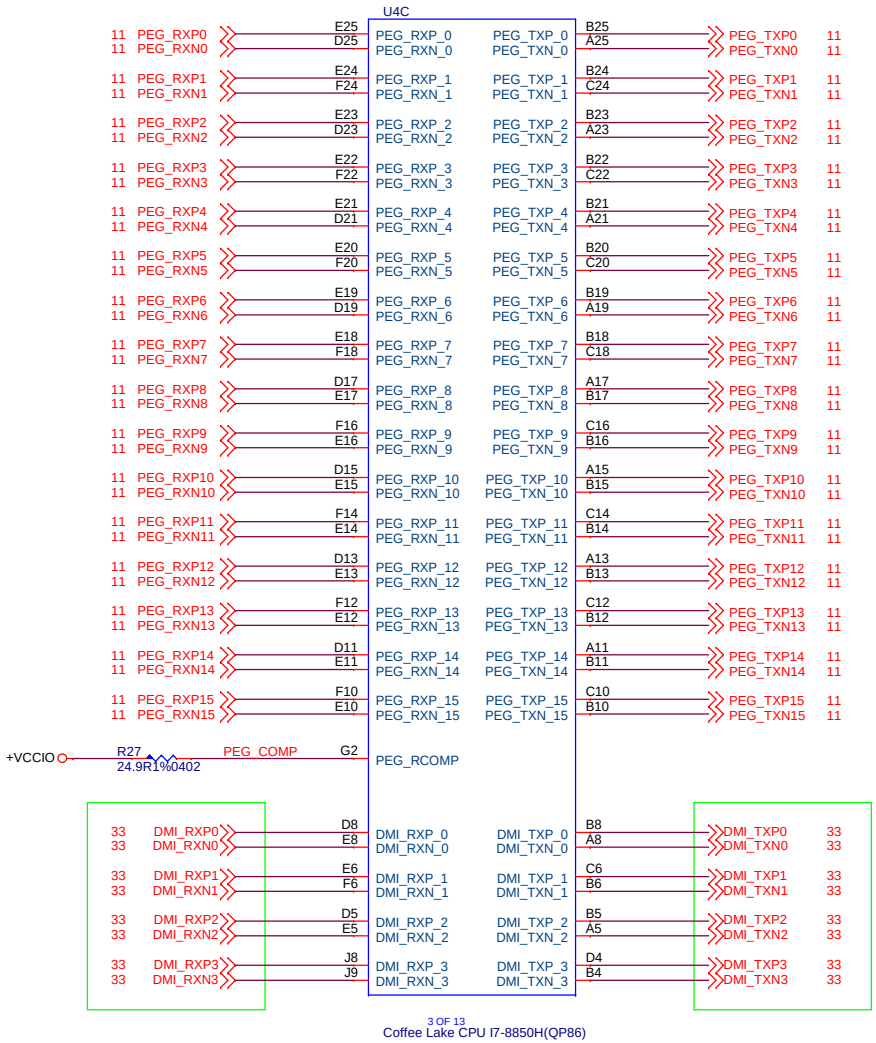
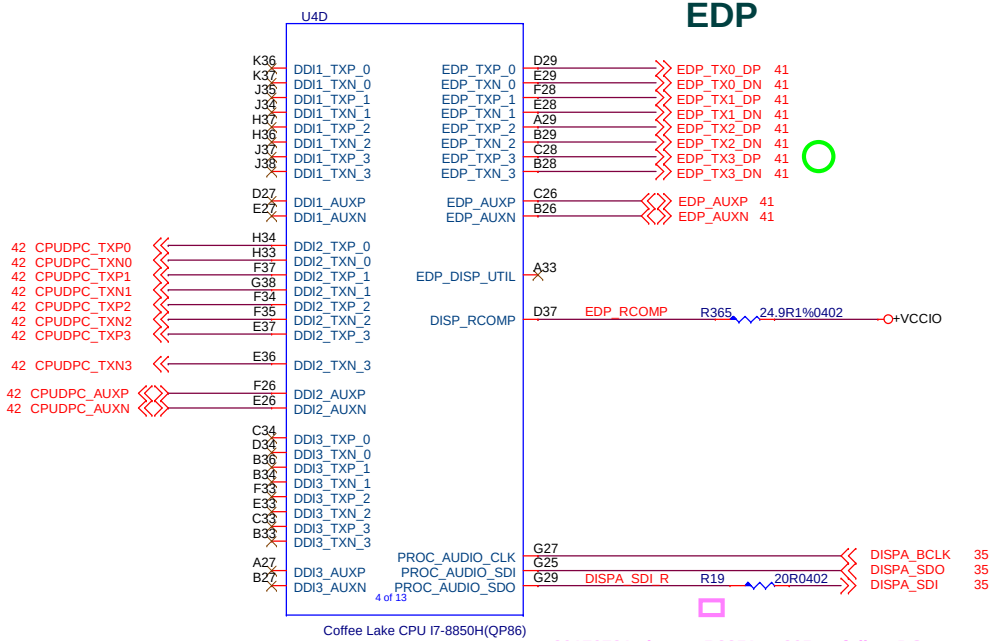


DDI C
DP to AR



EDP

20170731 change R2351 to 20R to follow DG

MICRO-STAR INT'L CO.,LTD.

Title	CFL-H(DMI/Display)	
Size: Custom	Document Number: MS-16K71	Rev: 10
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remove three 220uF Cap (Power repeat)

Follow CRB v0.7
+VCCCORE
3 x 220uF POSCAP
12 x 22uF 0603
42 x 10uF 0402
48 x 1uF 0201

+VCC_CORE

C437 C22u10X5-HF, C434 C22u10X5-HF, C425 C22u10X5-HF, C22 C22u10X5-HF, C428 C22u10X5-HF, C435 C22u10X5-HF

C423 C22u10X5-HF, C433 C22u10X5-HF, C426 C22u10X5-HF, C420 C22u10X5-HF, C421 C22u10X5-HF, C432 C22u10X5-HF

C613 C10u6.3X50402-HF, C611 C10u6.3X50402-HF, C439 C10u6.3X50402-HF, C440 C10u6.3X50402-HF, C27 C10u6.3X50402-HF, C26 C10u6.3X50402-HF, C419 C10u6.3X50402-HF, C623 C10u6.3X50402-HF, C25 C10u6.3X50402-HF, C622 C10u6.3X50402-HF

C441 C10u6.3X50402-HF, C621 C10u6.3X50402-HF, C19 C10u6.3X50402-HF, C624 C10u6.3X50402-HF, C625 C10u6.3X50402-HF, C430 C10u6.3X50402-HF, C525 C10u6.3X50402-HF, C510 C10u6.3X50402-HF, C620 C10u6.3X50402-HF, C511 C10u6.3X50402-HF

C617 C10u6.3X50402-HF, C615 C10u6.3X50402-HF, C524 C10u6.3X50402-HF, C512 C10u6.3X50402-HF, C509 C10u6.3X50402-HF, C619 C10u6.3X50402-HF, C507 C10u6.3X50402-HF, C508 C10u6.3X50402-HF, C614 C10u6.3X50402-HF, C522 C10u6.3X50402-HF

C527 C10u6.3X50402-HF, C616 C10u6.3X50402-HF, C523 C10u6.3X50402-HF, C618 C10u6.3X50402-HF, C28 C10u6.3X50402-HF, C506 C10u6.3X50402-HF, C427 C10u6.3X50402-HF, C24 C10u6.3X50402-HF, C20 C10u6.3X50402-HF, C520 C10u6.3X50402-HF

C521 C10u6.3X50402-HF, C612 C10u6.3X50402-HF

C478 C1u6.3X50201-HF, C32 C1u6.3X50201-HF, C666 C1u6.3X50201-HF, C649 C1u6.3X50201-HF, C664 C1u6.3X50201-HF, C665 C1u6.3X50201-HF, C648 C1u6.3X50201-HF, C34 C1u6.3X50201-HF, C477 C1u6.3X50201-HF, C30 C1u6.3X50201-HF

C484 C1u6.3X50201-HF, C653 C1u6.3X50201-HF, C485 C1u6.3X50201-HF, C486 C1u6.3X50201-HF, C655 C1u6.3X50201-HF, C29 C1u6.3X50201-HF, C654 C1u6.3X50201-HF, C650 C1u6.3X50201-HF, C651 C1u6.3X50201-HF, C489 C1u6.3X50201-HF

C491 C1u6.3X50201-HF, C483 C1u6.3X50201-HF, C490 C1u6.3X50201-HF, C657 C1u6.3X50201-HF, C487 C1u6.3X50201-HF, C656 C1u6.3X50201-HF, C652 C1u6.3X50201-HF, C488 C1u6.3X50201-HF, C667 C1u6.3X50201-HF, C668 C1u6.3X50201-HF

C658 C1u6.3X50201-HF, C663 C1u6.3X50201-HF, C661 C1u6.3X50201-HF, C492 C1u6.3X50201-HF, C493 C1u6.3X50201-HF, C494 C1u6.3X50201-HF, C659 C1u6.3X50201-HF, C660 C1u6.3X50201-HF, C662 C1u6.3X50201-HF, C495 C1u6.3X50201-HF

C475 C1u6.3X50201-HF, C481 C1u6.3X50201-HF, C479 C1u6.3X50201-HF, C31 C1u6.3X50201-HF, C480 C1u6.3X50201-HF, C35 C1u6.3X50201-HF, C476 C1u6.3X50201-HF, C482 C1u6.3X50201-HF

+VCC_CORE

+VCC_CORE

128A

U4I

AA13	VCC1	VCC64	AH13
AA31	VCC2	VCC65	AH14
AA32	VCC3	VCC66	AH29
AA33	VCC4	VCC67	AH30
AA34	VCC5	VCC68	AH31
AA35	VCC6	VCC69	AH32
AA36	VCC7	VCC70	AJ14
AA37	VCC8	VCC71	AJ29
AA38	VCC9	VCC72	AJ30
AB29	VCC10	VCC73	AJ31
AB30	VCC11	VCC74	AJ32
AB31	VCC12	VCC75	AJ33
AB32	VCC13	VCC76	AJ34
AB35	VCC14	VCC77	AJ35
AB36	VCC15	VCC78	AJ36
AB37	VCC16	VCC79	AK31
AB38	VCC17	VCC80	AK32
AC13	VCC18	VCC81	AK33
AC14	VCC19	VCC82	AK34
AC29	VCC20	VCC83	AK35
AC30	VCC21	VCC84	AK36
AC31	VCC22	VCC85	AK37
AC32	VCC23	VCC86	AK38
AC33	VCC24	VCC87	AL13
AC34	VCC25	VCC88	AL29
AC35	VCC26	VCC89	AL30
AC36	VCC27	VCC90	AL31
AD13	VCC28	VCC91	AL32
AD14	VCC29	VCC92	AL35
AD31	VCC30	VCC93	AL36
AD32	VCC31	VCC94	AL37
AD33	VCC32	VCC95	AL38
AD34	VCC33	VCC96	AM13
AD35	VCC34	VCC97	AM14
AD36	VCC35	VCC98	AM29
AD37	VCC36	VCC99	AM30
AD38	VCC37	VCC100	AM31
AE13	VCC38	VCC101	AM32
AE14	VCC39	VCC102	AM33
AE30	VCC40	VCC103	AM34
AE31	VCC41	VCC104	AM35
AE32	VCC42	VCC105	AM36
AE35	VCC43	VCC106	AN13
AE36	VCC44	VCC107	AN14
AE37	VCC45	VCC108	AN31
AE38	VCC46	VCC109	AN32
AF29	VCC47	VCC110	AN33
AF30	VCC48	VCC111	AN34
AF31	VCC49	VCC112	AN35
AF32	VCC50	VCC113	AN36
AF33	VCC51	VCC114	AN37
AF34	VCC52	VCC115	AN38
AF35	VCC53	VCC116	AP13
AF36	VCC54	VCC117	AP30
AF37	VCC55	VCC118	AP31
AF38	VCC56	VCC119	AP32
AG14	VCC57	VCC120	AP35
AG31	VCC58	VCC121	AP36
AG32	VCC59	VCC122	AP37
AG33	VCC60	VCC123	AP38
AG34	VCC61	VCC124	K13
AG35	VCC62		
AG36	VCC63		
	VCC_SENSE	AG37	
	VSS_SENSE	AG38	

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Coffee Lake CPU I7-8850H(QP86)

VCORE_VCC_SEN 59

R362
X_49.9R1%0402

VCORE_VSS_SEN 59

+VCC_CORE

+VCC_CORE

U4J

K14	VCC1	VCC64	W35
L13	VCC2	VCC65	W36
L14	VCC3	VCC66	W37
N13	VCC4	VCC67	W38
N14	VCC5	VCC68	Y29
N30	VCC6	VCC69	Y30
N31	VCC7	VCC70	Y31
N32	VCC8	VCC71	Y32
N35	VCC9	VCC72	Y33
N36	VCC10	VCC73	Y34
N37	VCC11	VCC74	Y35
N38	VCC12	VCC75	Y36
P13	VCC13		
P14	VCC14		
P29	VCC15		
P30	VCC16		
P31	VCC17		
P32	VCC18		
P33	VCC19		
P34	VCC20		
P35	VCC21		
P36	VCC22		
R13	VCC23		
R31	VCC24		
R32	VCC25		
R33	VCC26		
R34	VCC27		
R35	VCC28		
R36	VCC29		
R37	VCC30		
R38	VCC31		
T29	VCC32		
T30	VCC33		
T31	VCC34		
T32	VCC35		
T35	VCC36		
T36	VCC37		
T37	VCC38		
T38	VCC39		
U29	VCC40		
U30	VCC41		
U31	VCC42		
U32	VCC43		
U33	VCC44		
U34	VCC45		
U35	VCC46		
U36	VCC47		
V13	VCC48		
V14	VCC49		
V31	VCC50		
V32	VCC51		
V33	VCC52		
V34	VCC53		
V35	VCC54		
V36	VCC55		
V37	VCC56		
V38	VCC57		
W13	VCC58		
W14	VCC59		
W29	VCC60		
W30	VCC61		
W31	VCC62		
W32	VCC63		

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Coffee Lake CPU I7-8850H(QP86)

MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power1)

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Follow CRB v0.7
+VCCDU (+1_2VDIMM)
4 x 22uF 0603
12 x 10uF 0402

11.1A

+VCCSA

U4L

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8 VCCSA9 VCCSA10 VCCSA11 VCCSA12 VCCSA13 VCCSA14 VCCSA15 VCCSA16 VCCSA17 VCCSA18 VCCSA19 VCCSA20 VCCSA21 VCCSA22

3.3A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18 VDDQ19 VDDQ20 VDDQ21 VDDQ22 VDDQ23 VDDQ24 VDDQ25

+1_2VDIMM

C814 C804 C822 C815 C22u10X5-HF

C813 C805 C812 C682 C801 C809 C688 C800 C684 C685 C709 C10u6.3X50402-HF

Close CPU Y23 pin

C686 C10u6.3X50402-HF

6.4A

+VCCIO

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21

0.13A

VCCPLL_OC1 VCCPLL_OC2 VCCPLL_OC3

+VCCSFR_OC

0.06A

VCCST

+V1.05U_VCCST

0.02A

VCCSTG2 VCCSTG1

+V1.05DX_VCCSTG

0.15A

VCCPLL1 VCCPLL2

+V1.05U_VCCPLL

VCCSA_SENSE VSSSA_SENSE

VCCSA_VCC_SENSE 59
VCCSA_VSS_SENSE 59

VCCIO_SENSE VSSIO_SENSE

+VCCIO

12 OF 13

Coffee Lake CPU I7-8850H(QP86)

Remove +VCCVDDQ_CLK, it combine with VDDQ.
Pin number Y12

+VCCSFR_OC

R385 0R0402 +1_2VDIMM

+V1.05U_VCCPLL

R376 0R0402 +V1.05U_VCCST

+V1.05U_VCCPLL

C500 C1u10X50402-HF

Close CPU H28 and J28 pin

recommend external test point on CRBv0.7.

TPJNC16 TPEV_PEG_VIEW_2

35 PCH_2_CPU_TRIGGER_R
35 CPU_2_PCH_TRIGGER_R

R377 30R0402 CPU_2_PCH_TRIGGER

U4M

RSVD_TP5 IST_TRIG RSVD_TP4 RSVD_TP3 RSVD_TP1 RSVD_TP2 RSVD15 RSVD28 RSVD27 RSVD14 RSVD13 RSVD30 RSVD31 RSVD2 RSVD1 RSVD5 RSVD4 VSS_A36 VSS_A37 PROC_TRIGIN PROC_TRIGOUT RSVD24 RSVD23 RSVD7 RSVD21 RSVD26 RSVD29 RSVD19 RSVD18 RSVD9

RSVD11 RSVD10 RSVD12 RSVD3 RSVD25 RSVD22 RSVD20 RSVD17 RSVD16 RSVD8 RSVD6

13 OF 13

Coffee Lake CPU I7-8850H(QP86)

Follow CRB v0.7
+VCCSA
5 x 47uF 0805
4 x 22uF 0603
7 x 10uF 0402
1 x 1uF 0201

+VCCSA

C403 C395 C424 C16 C422 C47u6.3X5-HF

C17 C21 C431 C436 C22u10X5-HF

C411 C410 C406 C408 C409 C402 C18 C10u6.3X50402-HF

C33 C1u6.3X50201-HF

+VCCIO

C610 C670 C529 C10u6.3X50402-HF

Follow CRB v0.7
+VCCIO
3 x 22uF 0603

+V1.05DX_VCCSTG Cap side of CRB and PDG are 0201

C37 C1u10X50402-HF

+VCCSFR_OC Cap side of CRB and PDG are 0201

C683 C643 C1u10X50402-HF

+V1.05U_VCCST Cap side of CRB and PDG are 0201

C459 C1u10X50402-HF

Close CPU H30 pin

+V1.05DX_VCCSTG

+V1.05DX_VCCSTG

+3VSUS

U2

VDD S D CAP GND ON

SLG5NT1533V_STDFN8-HF

C39 C0.1u50X0402-HF

+1.05VSUS

C455 C10u6.3X50402-HF

VCCSTG_EN

R17 0R0402

C38 C470p50X0402

+3VSUS

U3

X_M74VHC1GT08DFT2G_SC705-RH

R604

100KR0402

PM_SLP_S3# 3,32,39,42,57,59,62

1.8V Level

CPU_C10_GATE# 36,62

PN : T3E-1GT0800-O05
MC74VHC1GT08
AND Gate Level Shifter

	VCC	Min	Max
VIH	3V	1.4V	
VIL	3V		0.53V

(1)Ref DG Section 51.1.3
VCCSTG should be gated by
{SLP_S3#} AND {CPU_C10_GATE#}
(2)Power Sequence spec tCPU26 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 65 us

20170913 add R604 to follow DG

+V1.05U_VCCST

20170731 change C45 to 0.1uF

+V1.05U_VCCST

+3VSUS

U44

VDD S D CAP GND ON

SLG5NT1533V_STDFN8-HF

C43 C0.1u50X0402-HF

+1.05VSUS

C41 C10u6.3X50402-HF

PM_SLP_S4# 32,39,57

C462 C220p50N0402

R372 100KR0402

Discharge R Max 300 Ohm

Ref DG Table 51-1
VCCST gated by SLP_S4#

20170731 change C45 to 0.1uF
20170804 change U39 to SLG5NT1533V to correct power sequence control by PM_SLP_S4#
C404 change from 2200pF to 220pF

MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power2)

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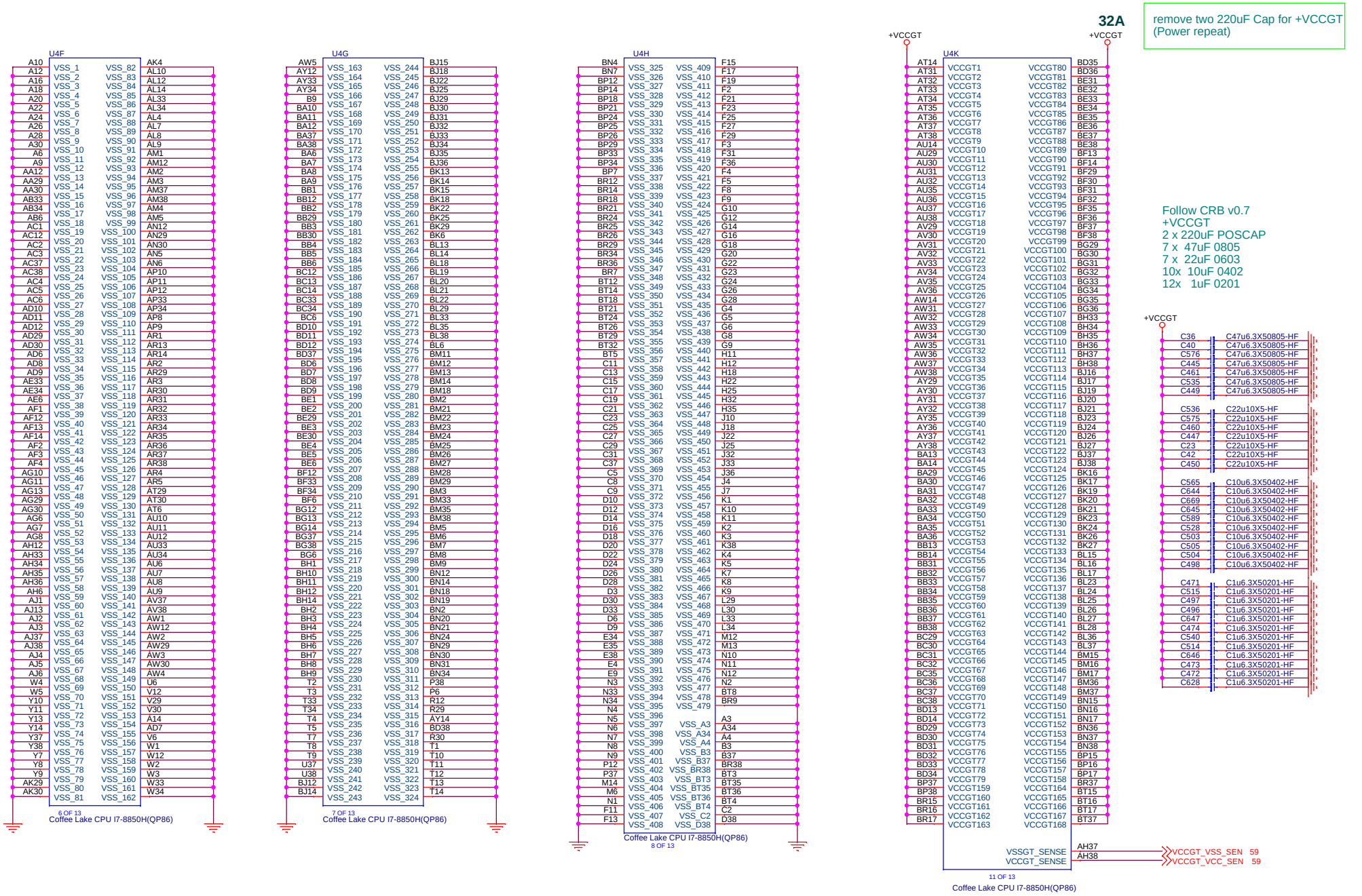

MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power3)

Size: A3 | Document Number: MS-16K71 | Rev: 10

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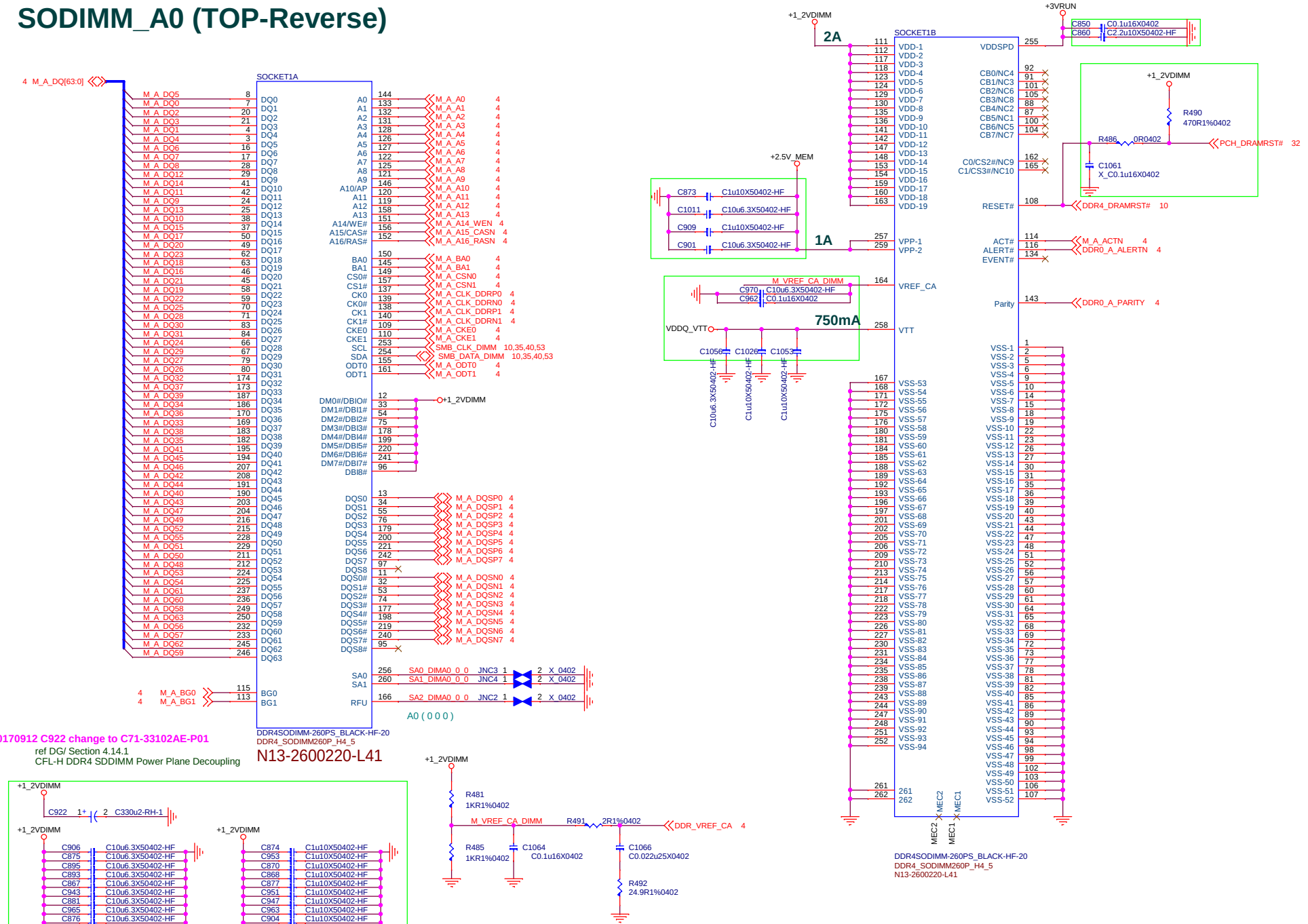
SODIMM_A0 (TOP-Reverse)



Title	DDR4_SODIMM_A0
Size / Document Number	Custom / MS-16K71
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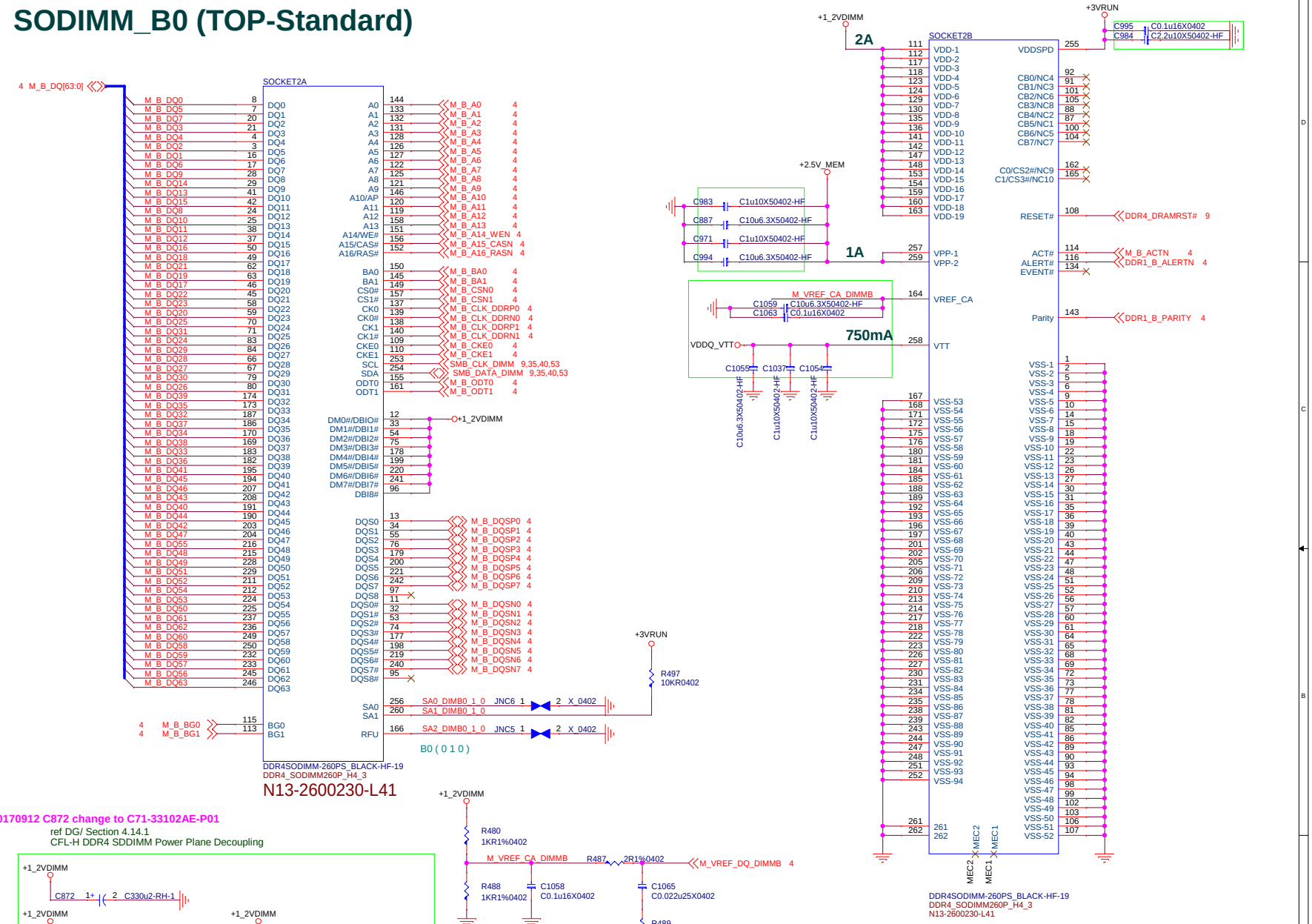
MICRO-STAR INT'L CO.,LTD.

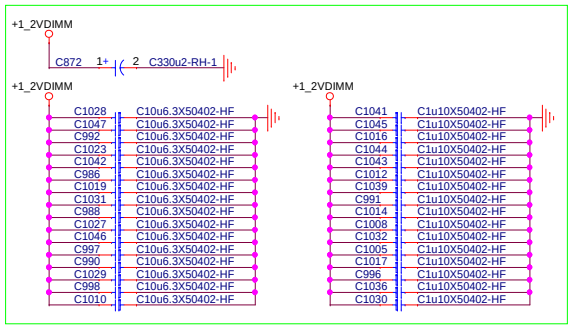
SODIMM_B0 (TOP-Standard)



20170912 C872 change to C71-33102AE-P01

ref DG/ Section 4.14.1

CFL-H DDR4 SDDIMM Power Plane Decoupling



msi MICRO-STAR INT'L CO.,LTD.			
Title: DDR4_SODIMM_B0			
Size: Custom	Document Number: MS-16K71		Rev: 10
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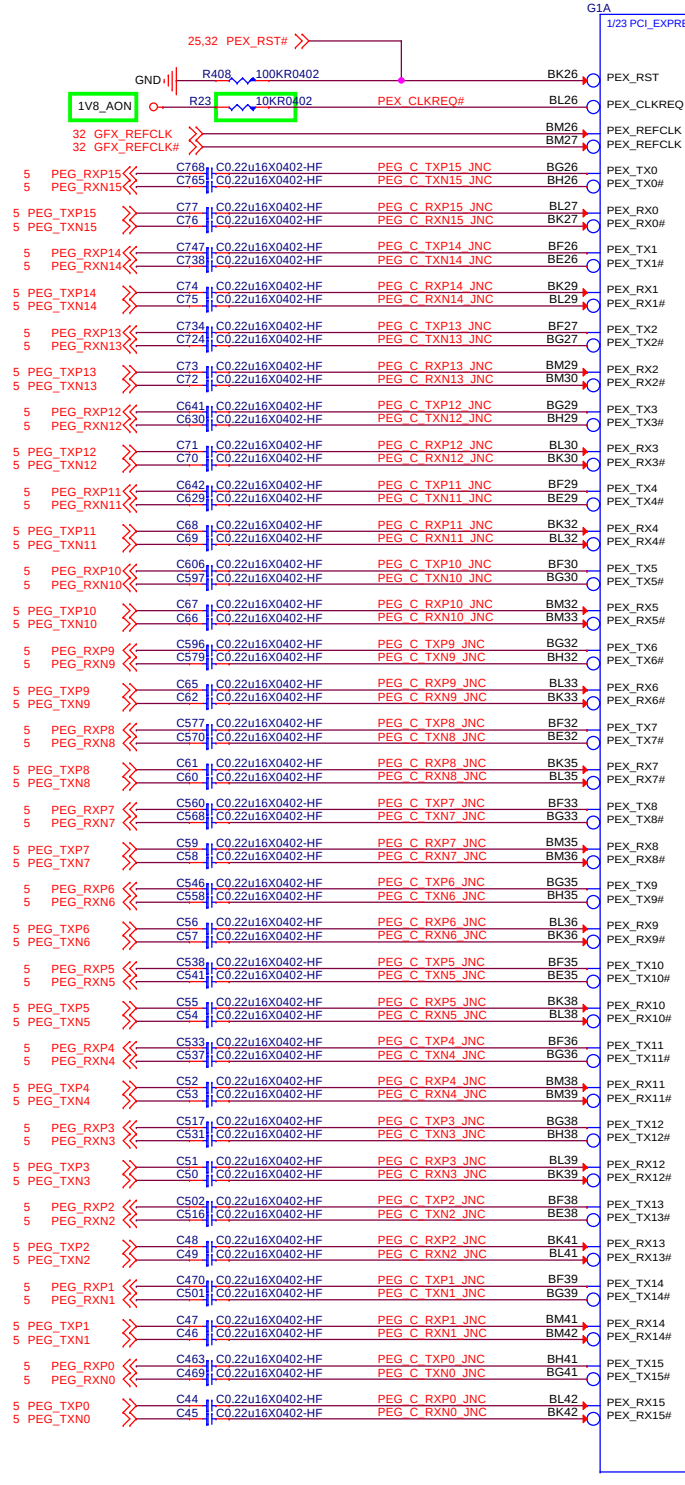
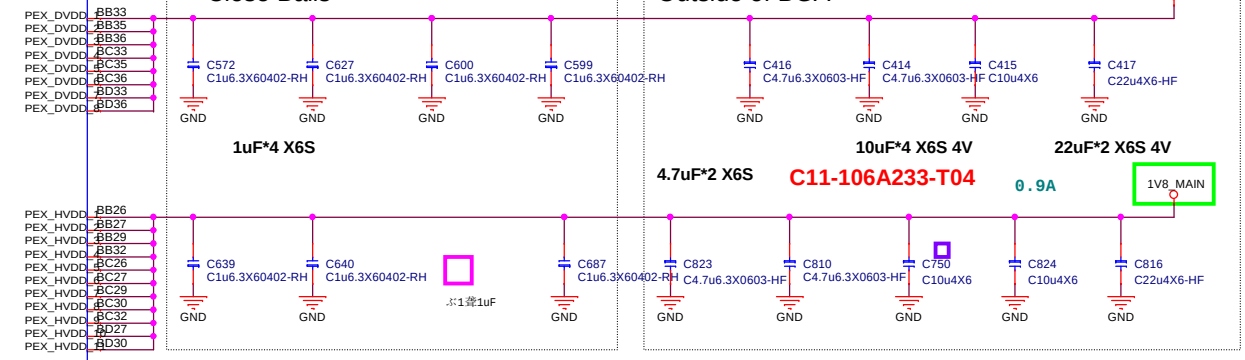
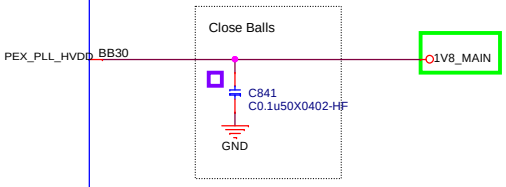
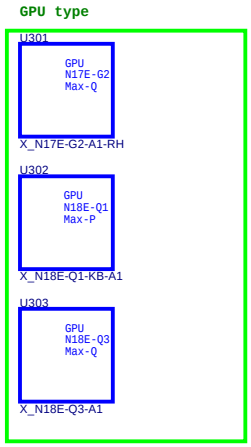
GPU PCI EXPRESS

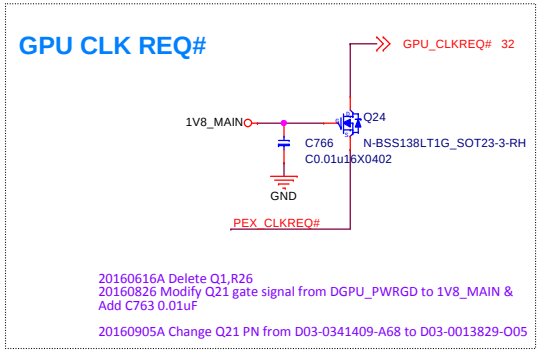






DG Page 117	Under GPU	Near GPU
PEX_HVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 1 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	1 X 0.1uF(0402)	





PEX_TERMP BL44 PEX_TERMP R18 2.49KR1%0402 GND

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_PCI-E Host

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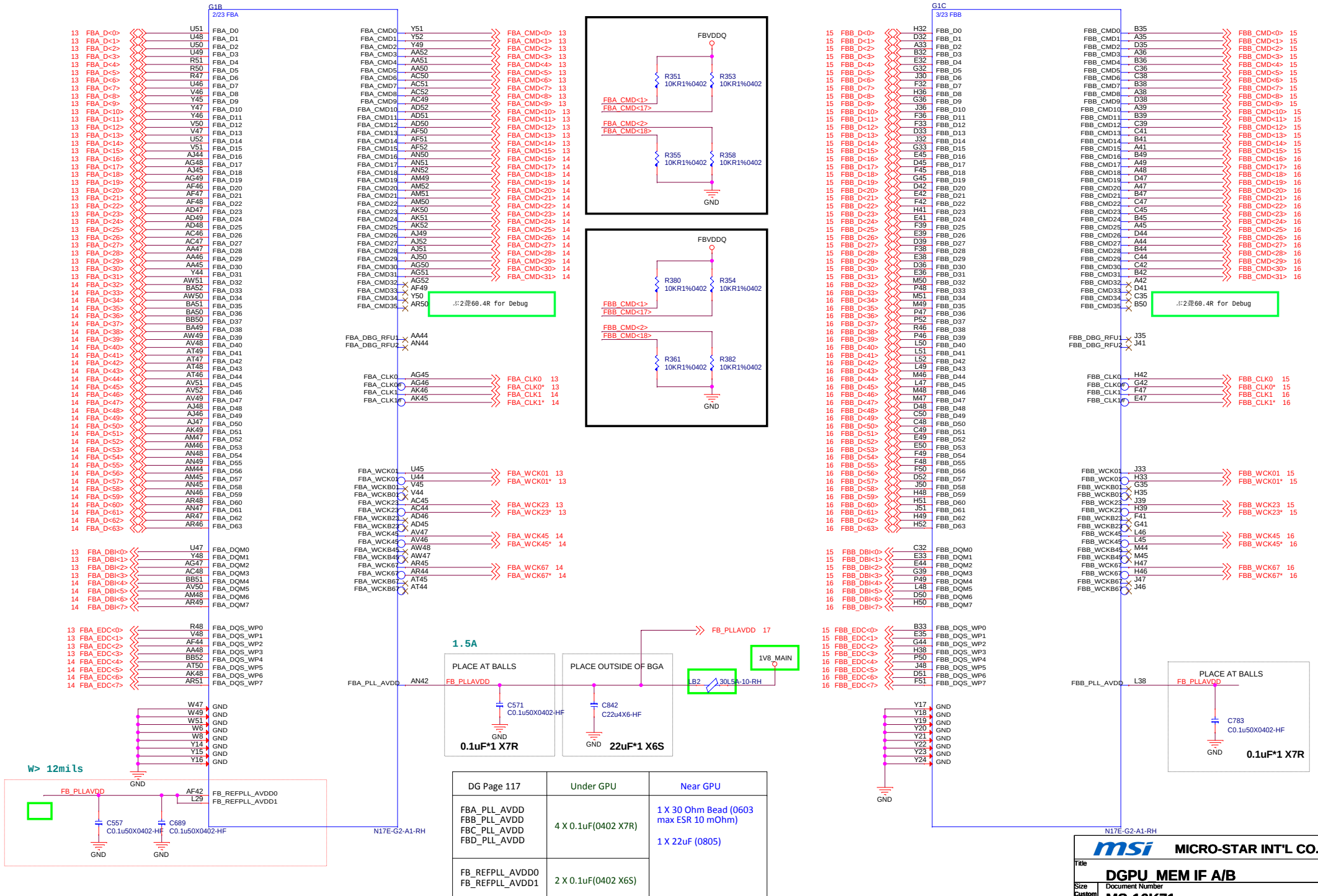
GPU Frame Buffer Partition A/B



DG Page 117	Under GPU	Near GPU
FBA_PLL_AVDD FBB_PLL_AVDD FBC_PLL_AVDD FBD_PLL_AVDD	4 X 0.1uF(0402 X7R)	1 X 30 Ohm Bead (0603 max ESR 10 mOhm) 1 X 22uF (0805)
FB_REFPLL_AVDD0 FB_REFPLL_AVDD1	2 X 0.1uF(0402 X6S)	

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Title: DGPU_MEM IF A/B

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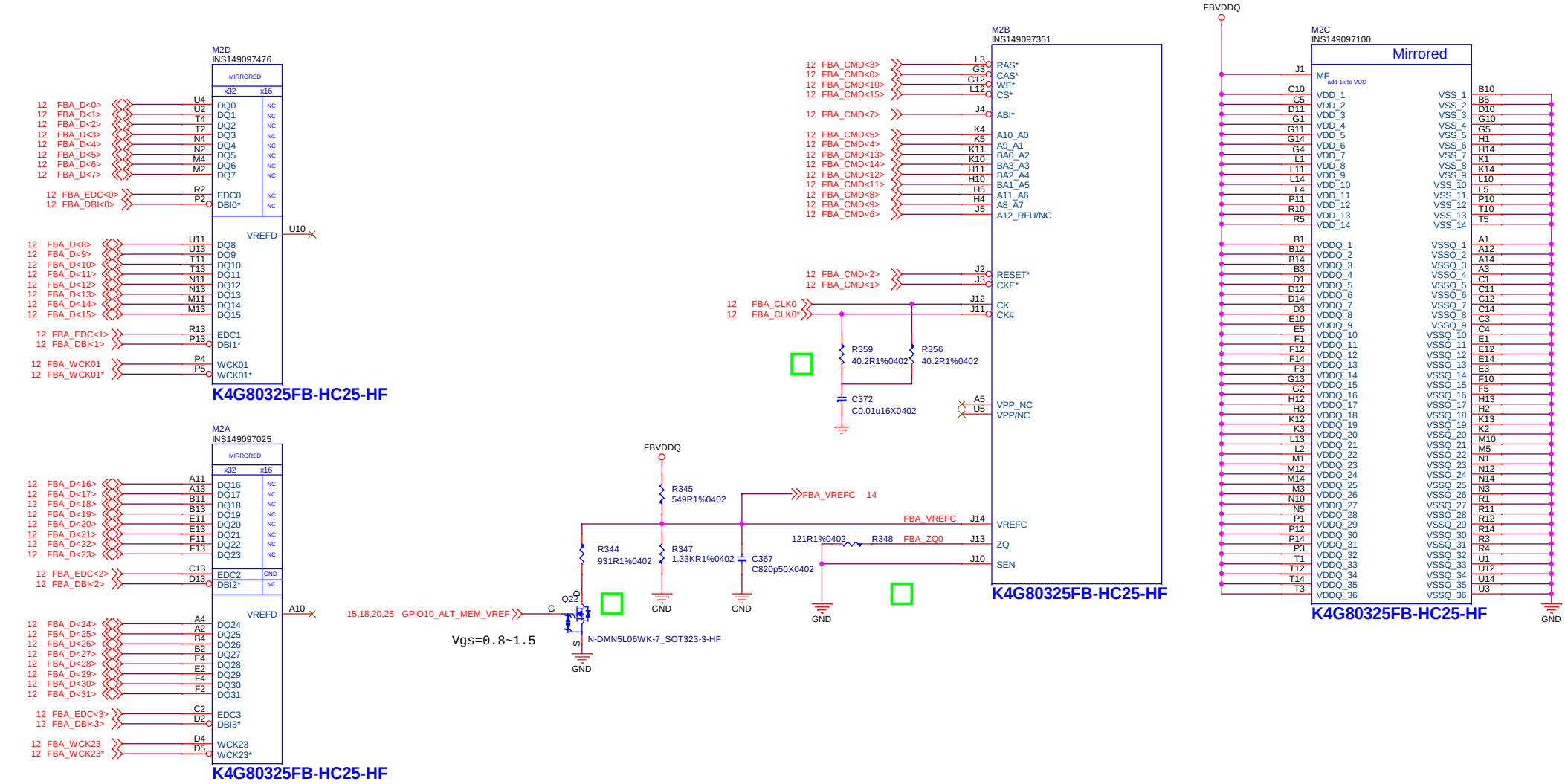
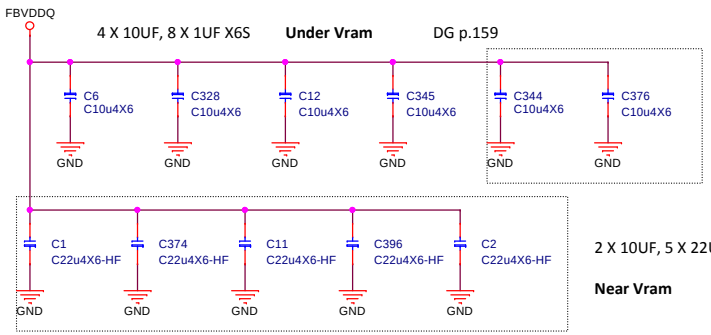
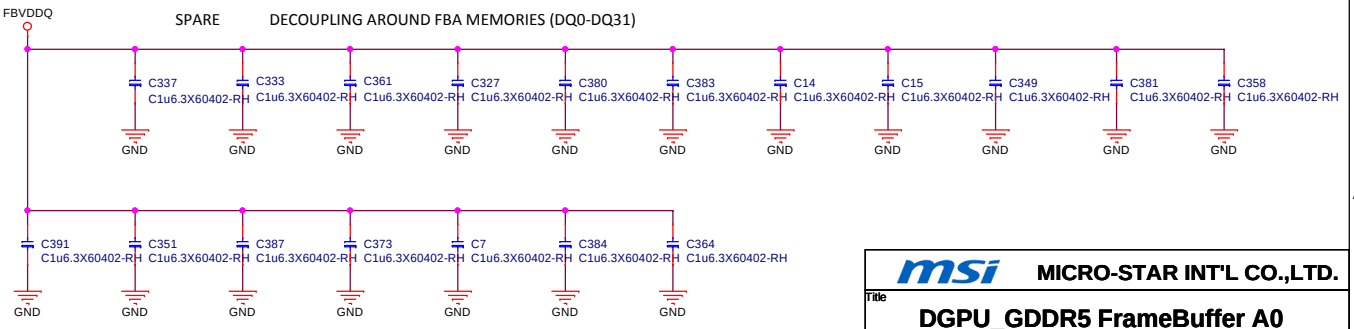
Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

DGPU_GDDR5 FrameBuffer A0







MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer A0

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Custom	MS-16K71	10

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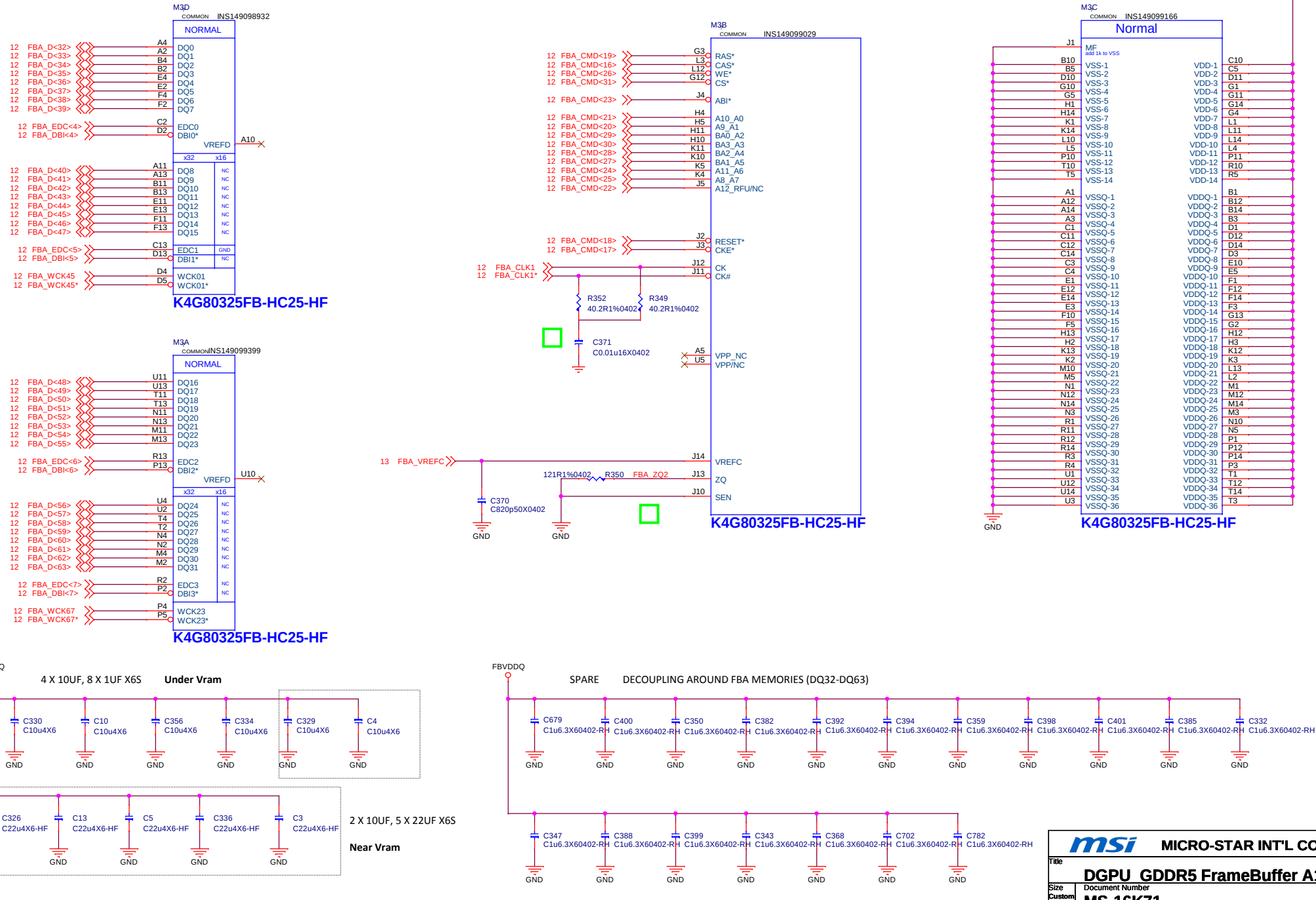
DGPU_GDDR5 FrameBuffer A1



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer A1	
Size: Custom	Document Number: MS-16K71	Rev: 10
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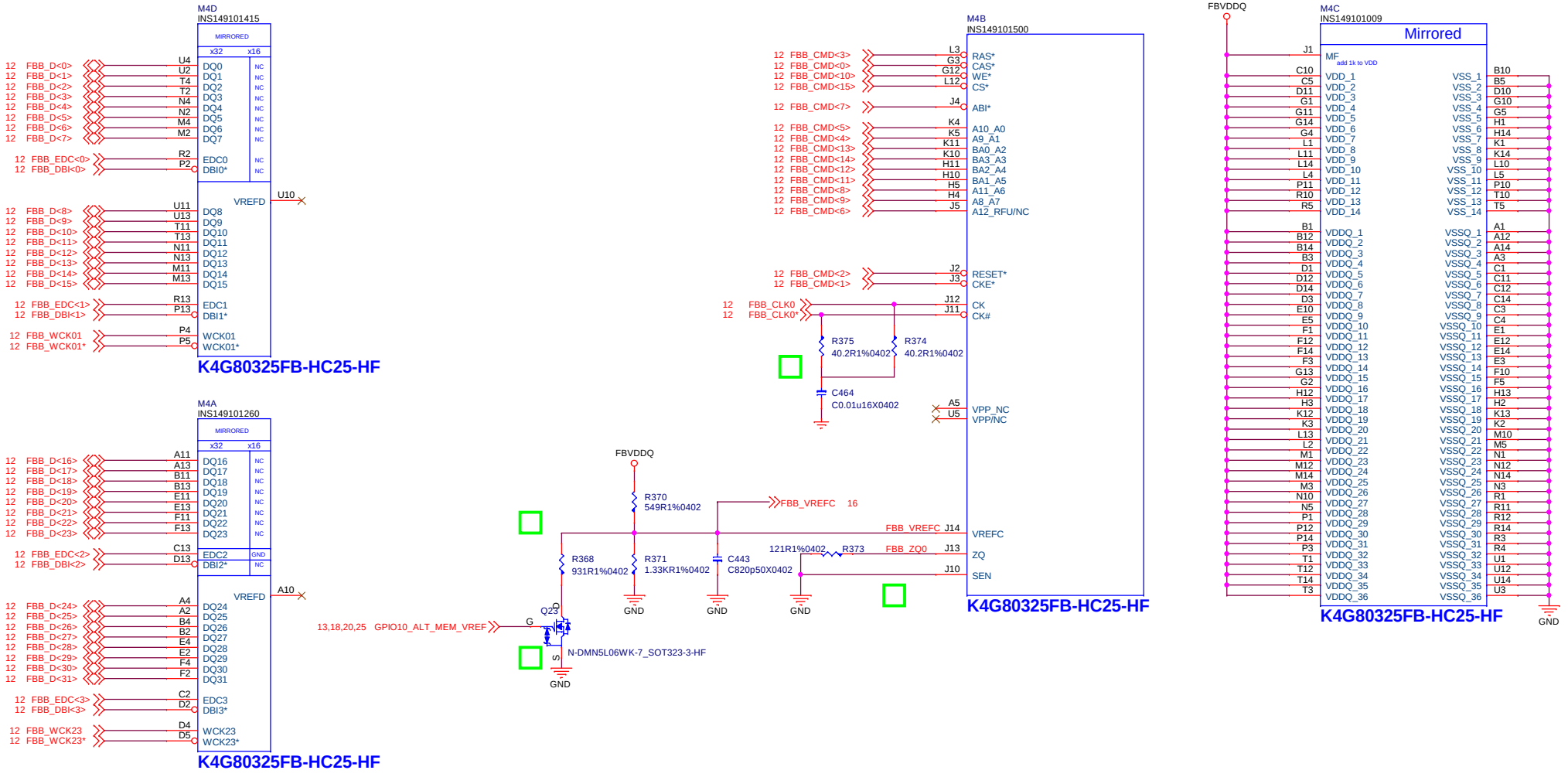
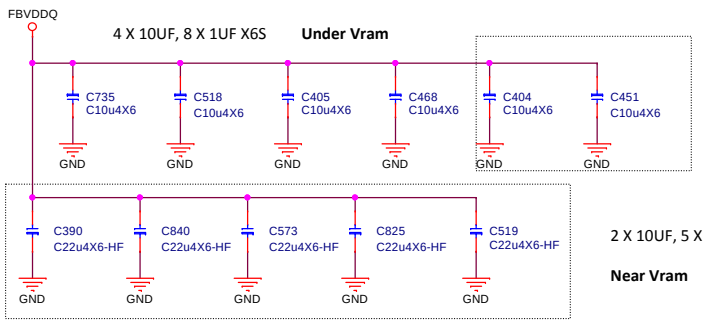
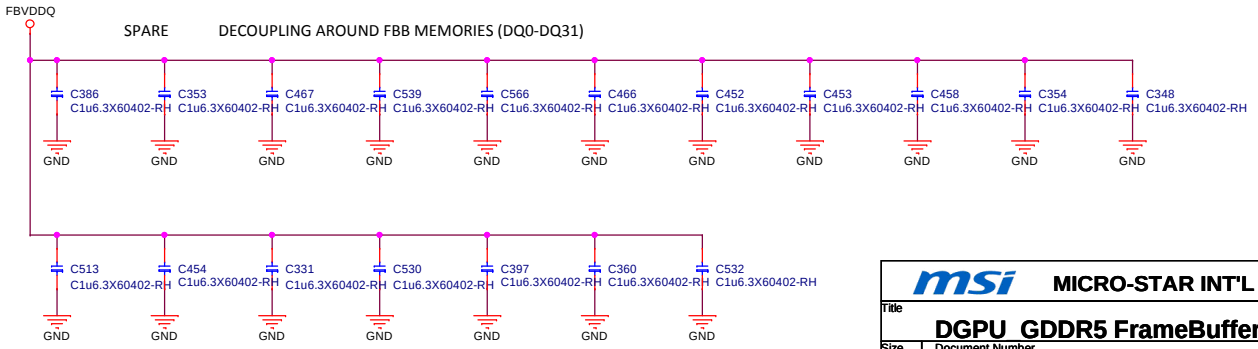
DGPU_GDDR5 FrameBuffer B0







MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B0	
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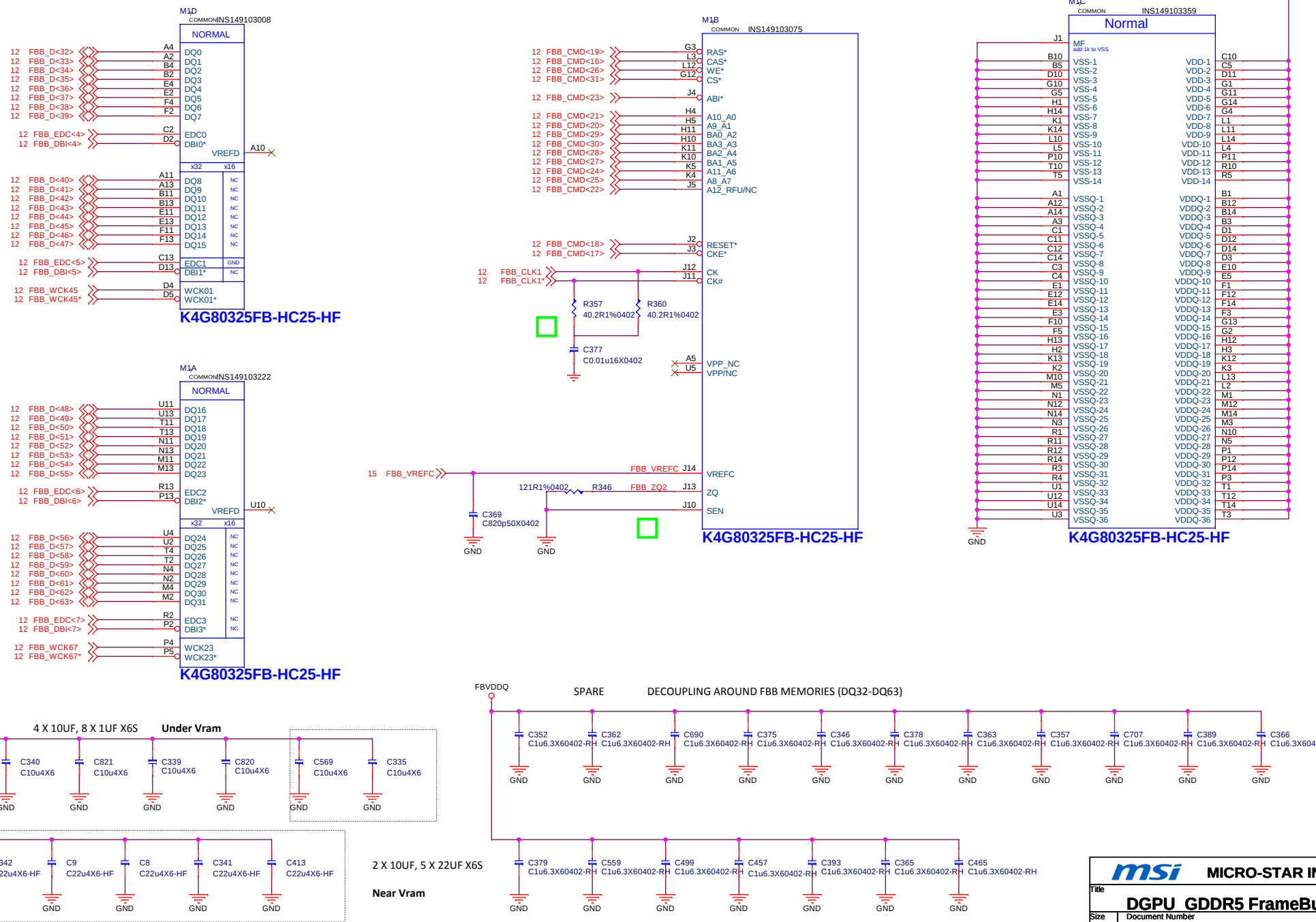
DGPU_GDDR5 FrameBuffer B1



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer B1	
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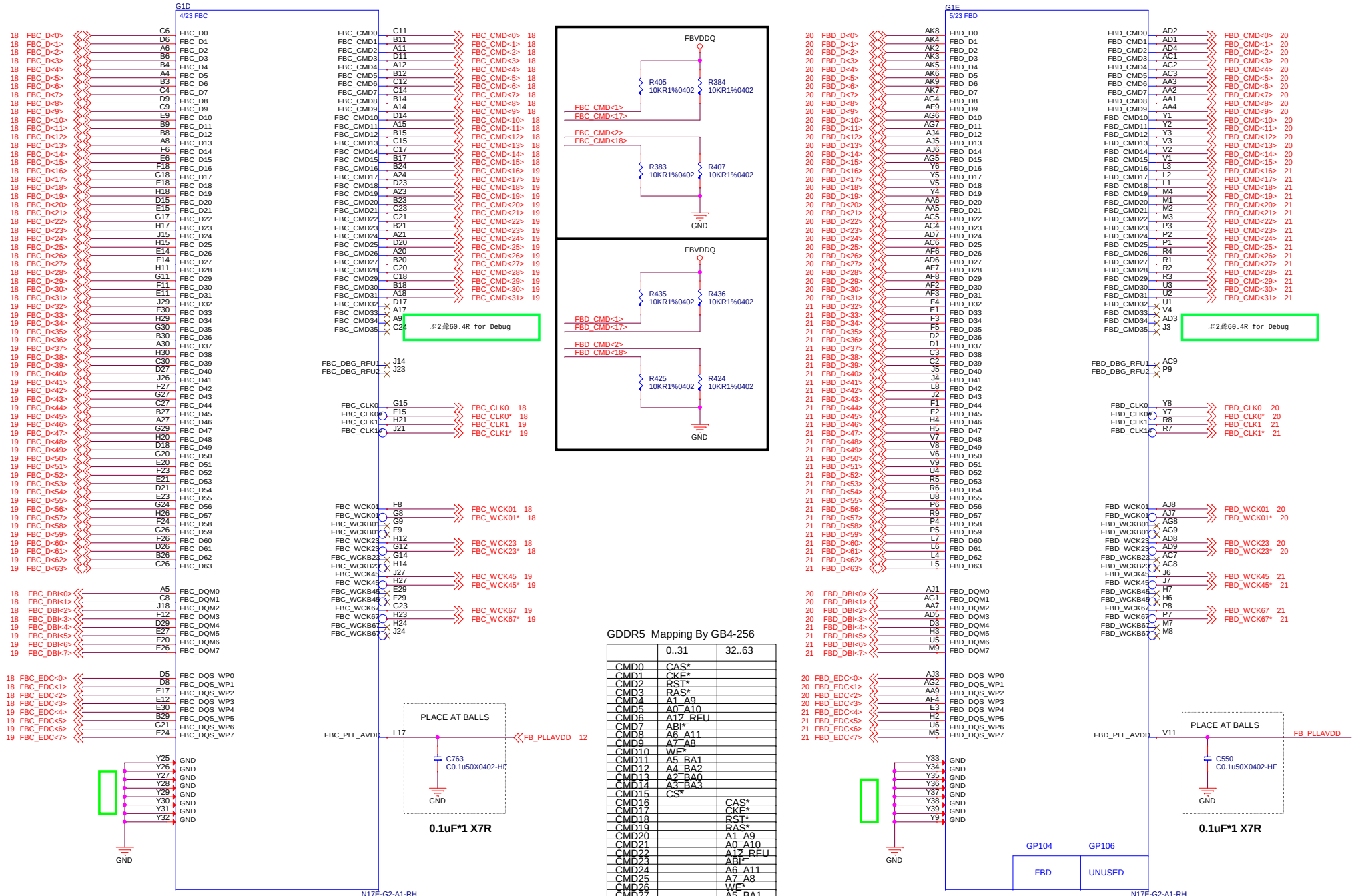
GPU Frame Buffer Partition C/D



GDDR5 Mapping By GB4-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_MEM IF C/D

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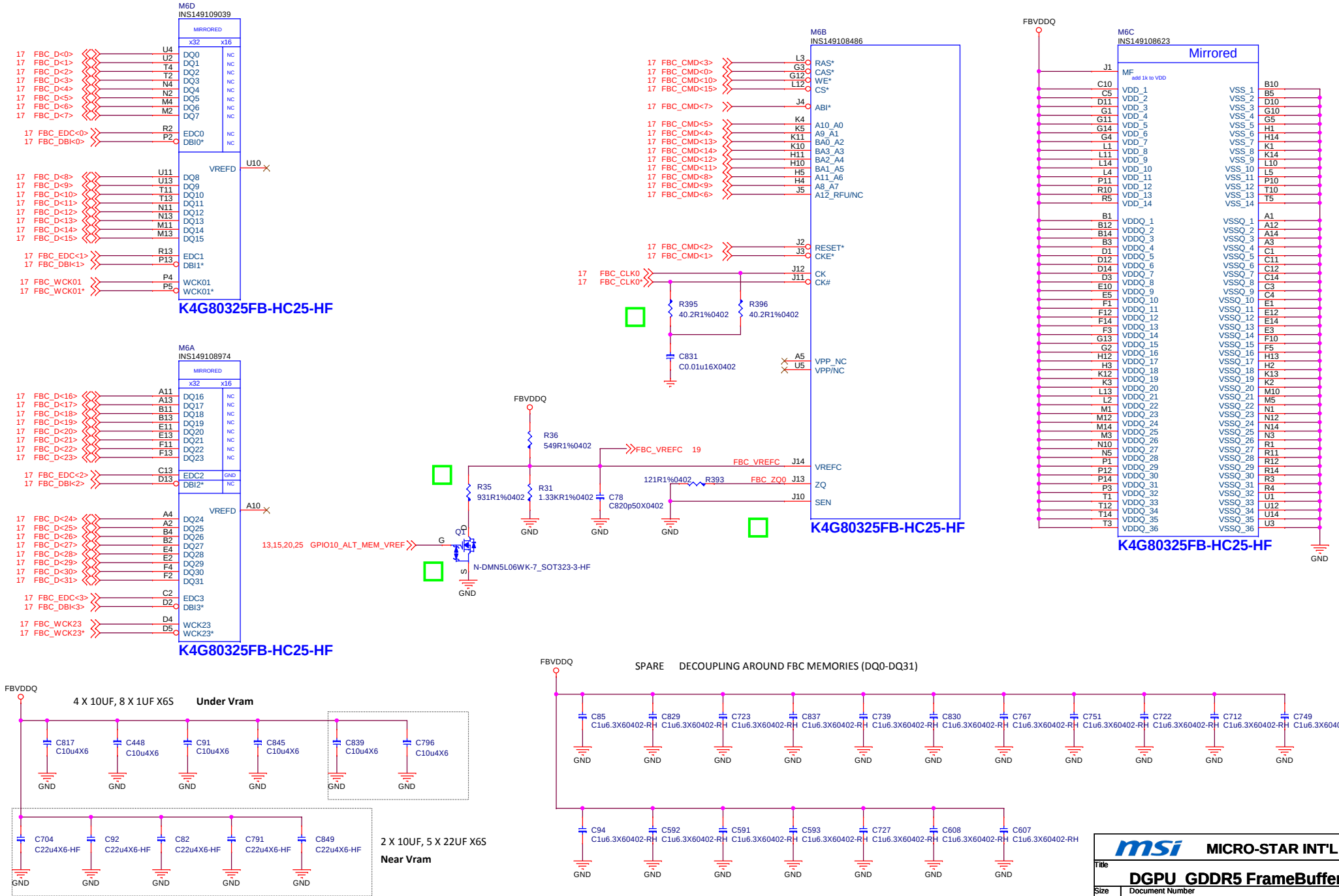
DGPU_GDDR5 FrameBuffer C0



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer C0	
Size: Custom	Document Number: MS-16K71	Rev: 10
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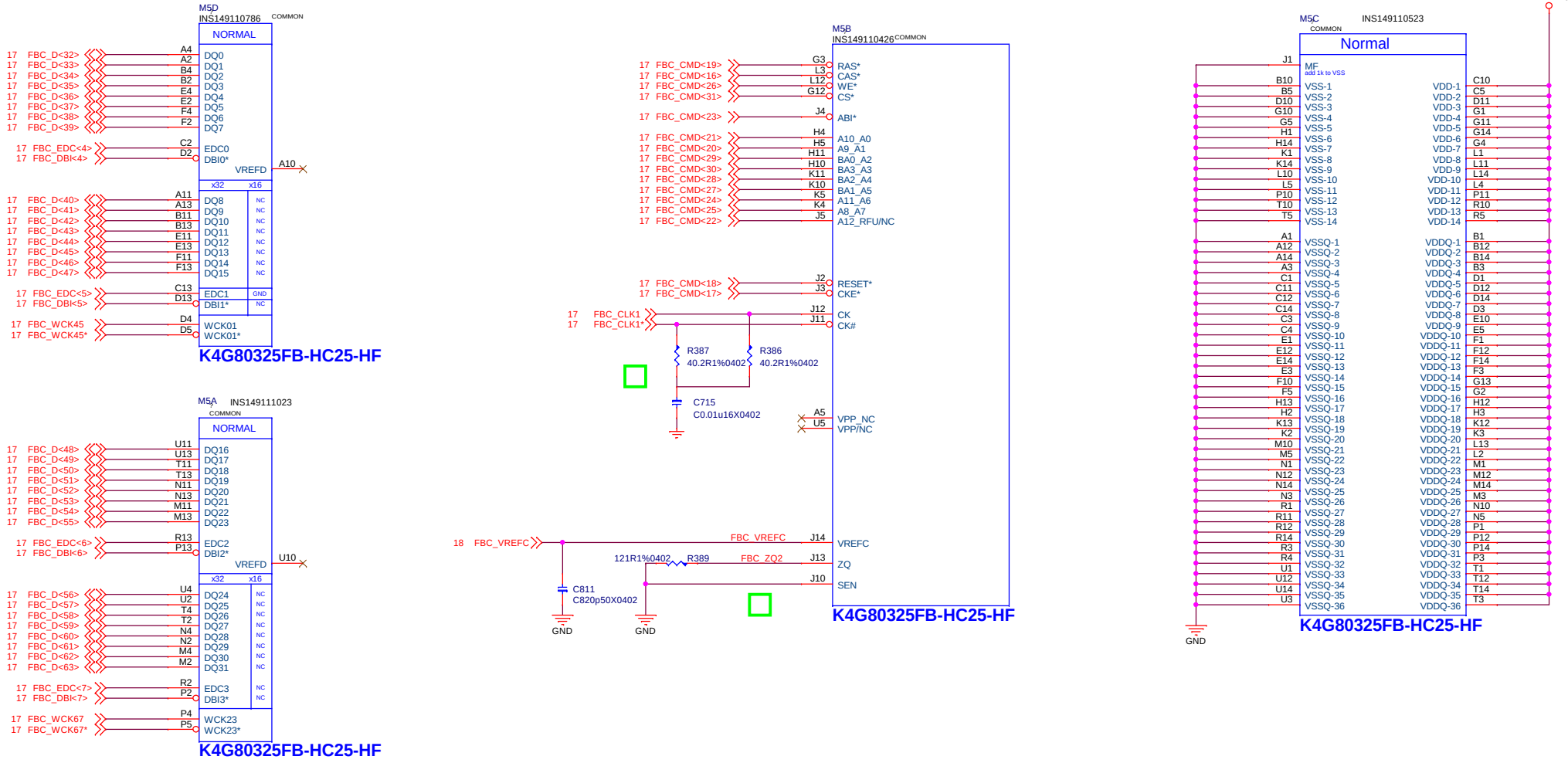
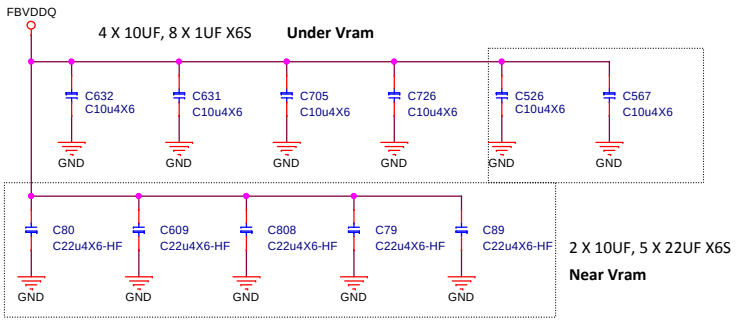
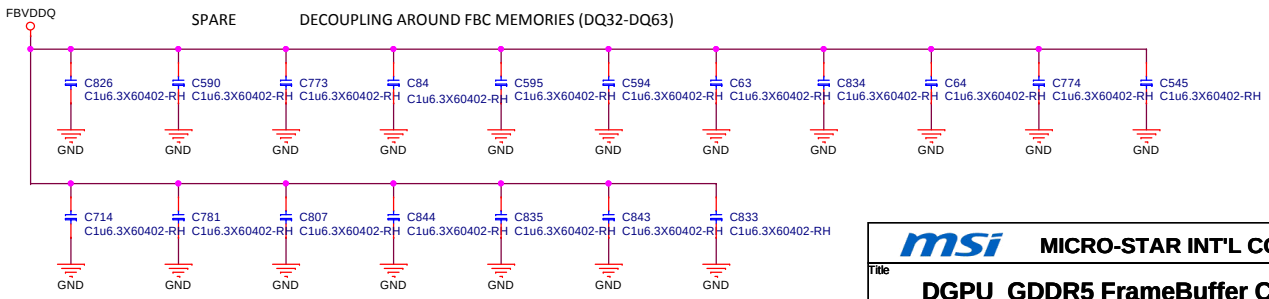
DGPU_GDDR5 FrameBuffer C1







MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer C1	
Size: Custom	Document Number: MS-16K71	Rev: 10
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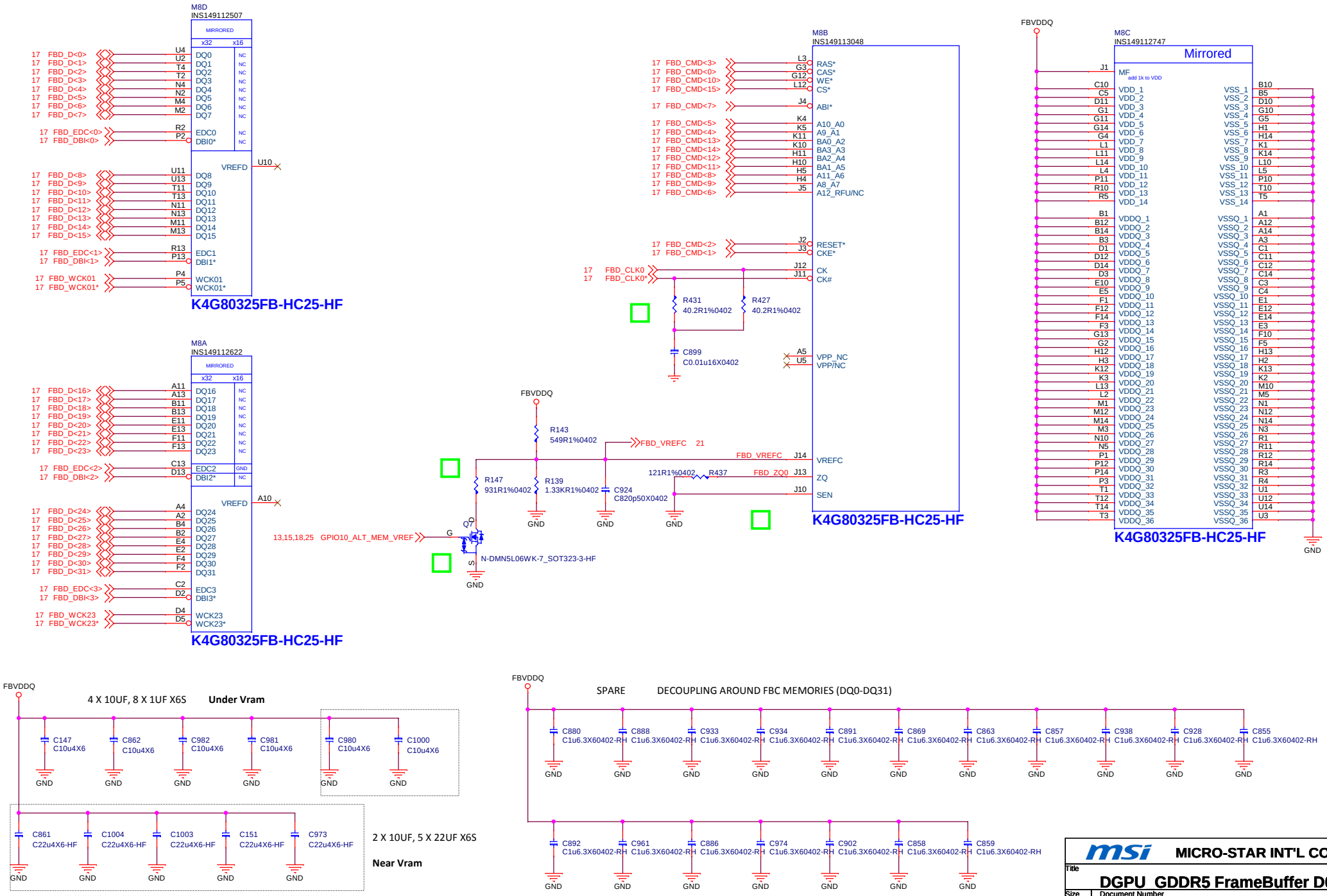
DGPU_GDDR5 FrameBuffer D0



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer D0	
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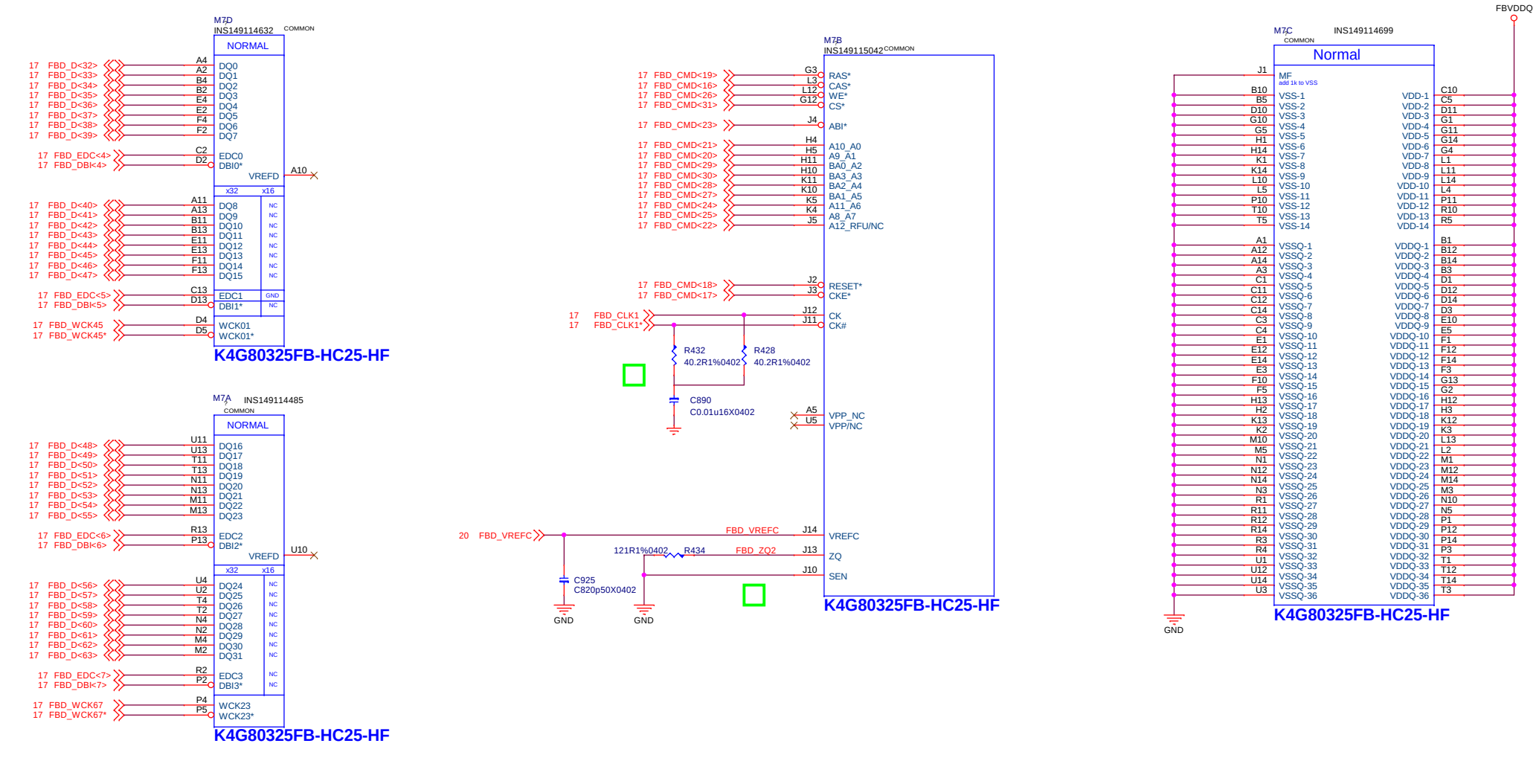
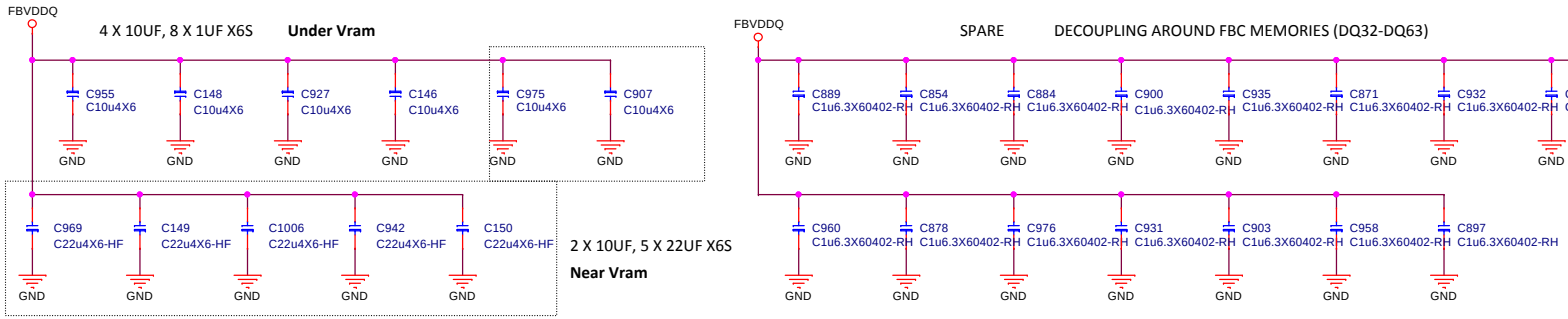
DGPU_GDDR5 FrameBuffer D1





MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GDDR5 FrameBuffer D1	
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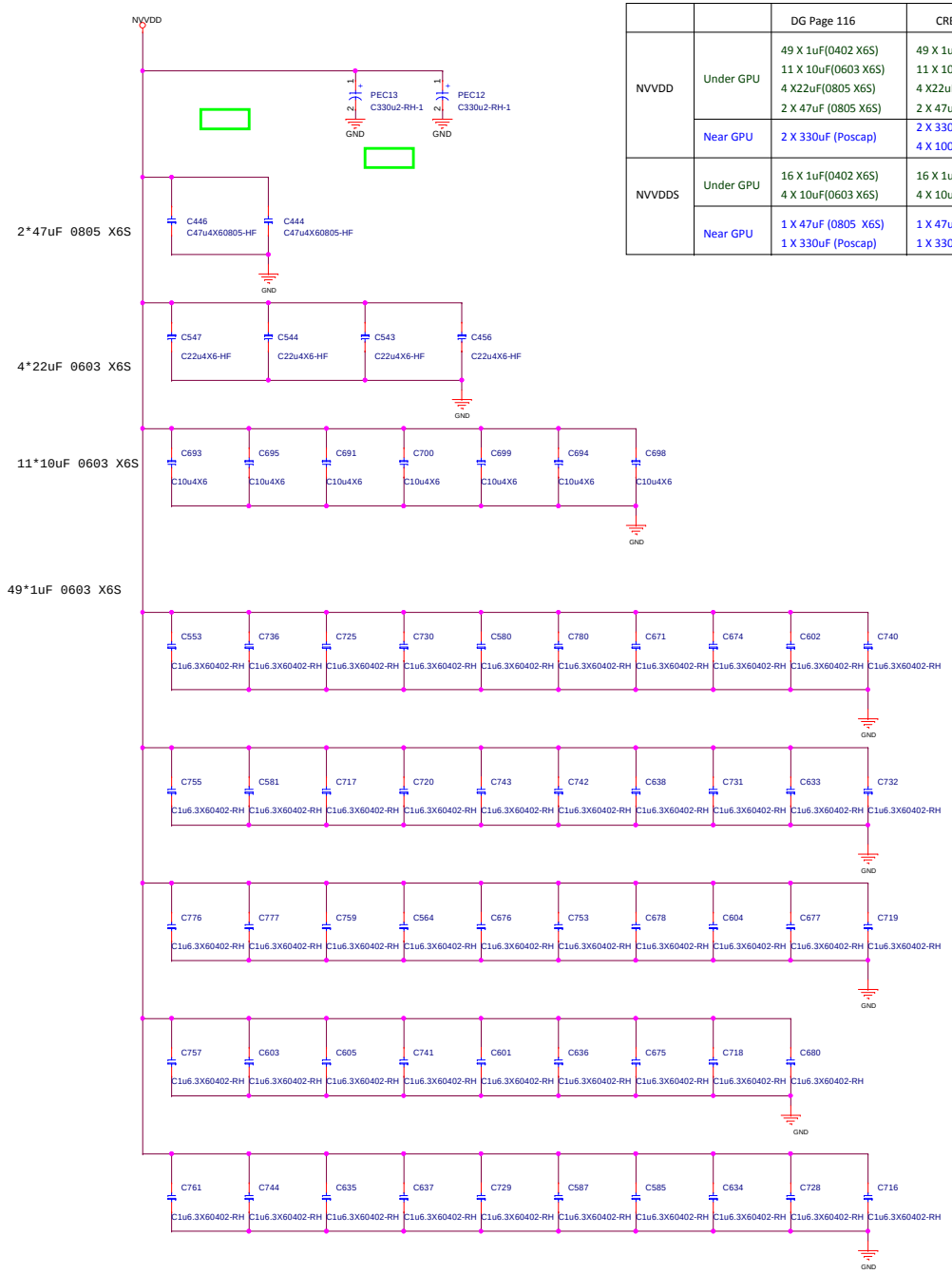
GPU DECOUPLING A

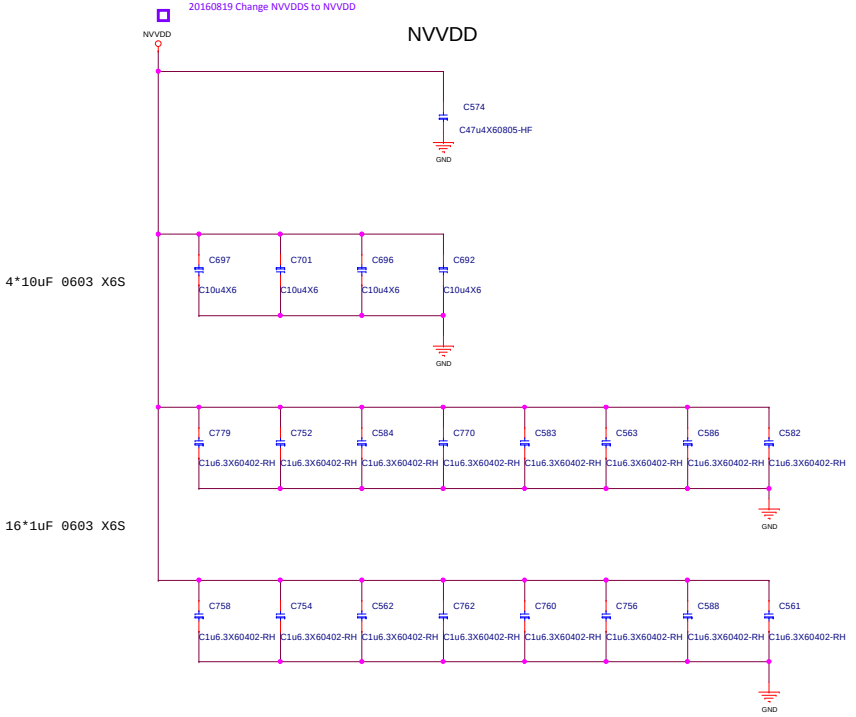
NVVDD

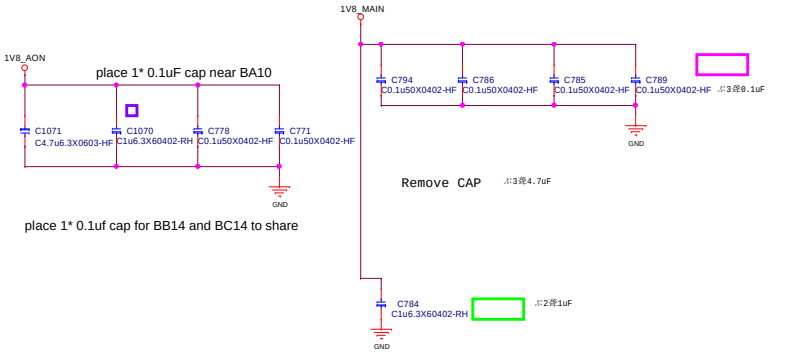


		DG Page 116	CRB
NVVDD	Under GPU	49 X 1uF(0402 X6S) 11 X 10uF(0603 X6S) 4 X22uF(0805 X6S) 2 X 47uF (0805 X6S)	49 X 1uF(X7R 6.3V) 11 X 10uF(X6S 6.3V) 4 X22uF(X6S 6.3V) 2 X 47uF (X6S 4V)
	Near GPU	2 X 330uF (Poscap)	2 X 330uF (Poscap) 4 X 100uF (X5R 4V) add
NVVDDS	Under GPU	16 X 1uF(0402 X6S) 4 X 10uF(0603 X6S)	16 X 1uF(X6S 6.3V) 4 X 10uF(0603 X6S 4V)
	Near GPU	1 X 47uF (0805 X6S) 1 X 330uF (Poscap)	1 X 47uF (0805 X5R 4V) 1 X 330uF (AL-Polymer)

20160819 Change NVVDDS to NVVDD

NVVDD





		DG Page 117	CRB
1V8_MAIN	Under GPU	7 X 0.1uF(0402)	7 X 0.1uF(0402 X7R)
	Near GPU	3 X 1uF (0402) 3 X 4.7uF (0603)	3 X 1uF (0603 X7R) 3 X 4.7uF (0603 X6S)
1V8_AON	Under GPU	2 X 0.1uF(0402)	2 X 0.1uF(0402 X7R)
	Near GPU	1 X 1uF (0402) 1 X 4.7uF (0603)	1 X 1uF (0603 X7R) 1 X 4.7uF (0603 X6S)

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Title: DGPU_GPU DECOUPLING A

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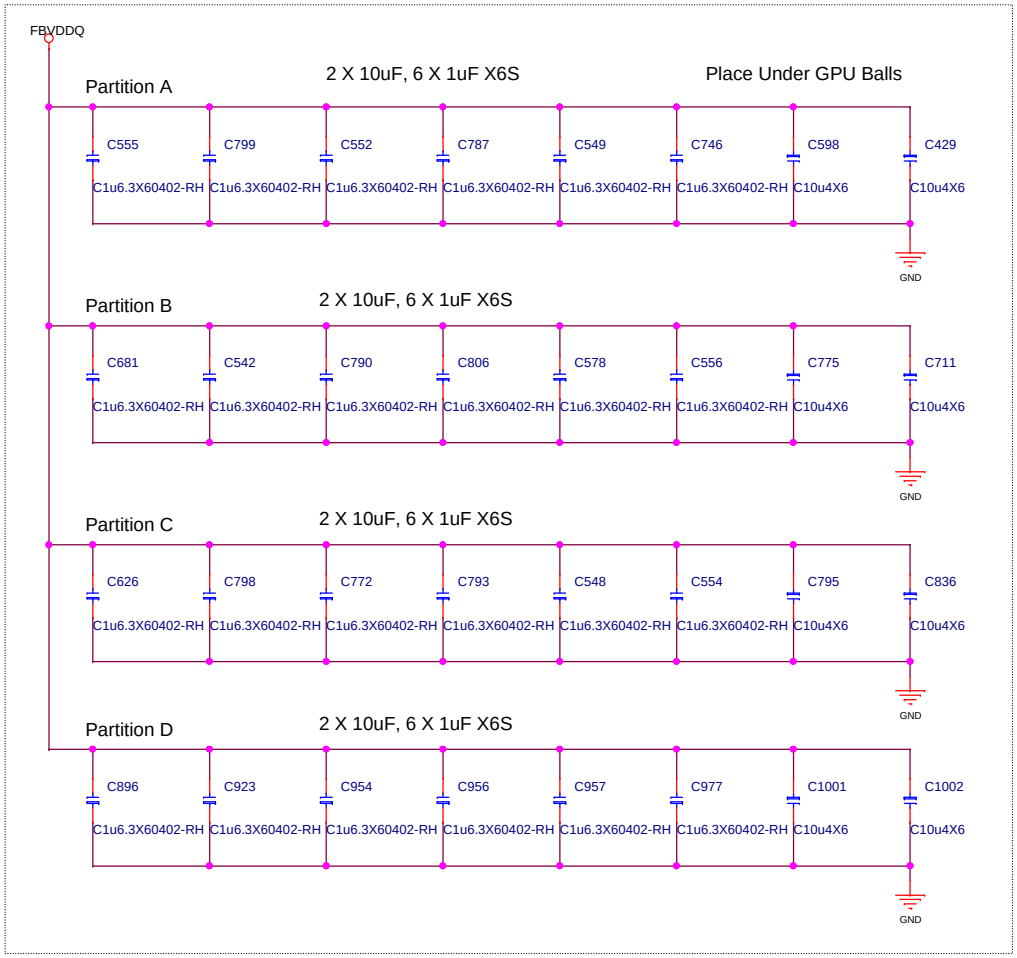
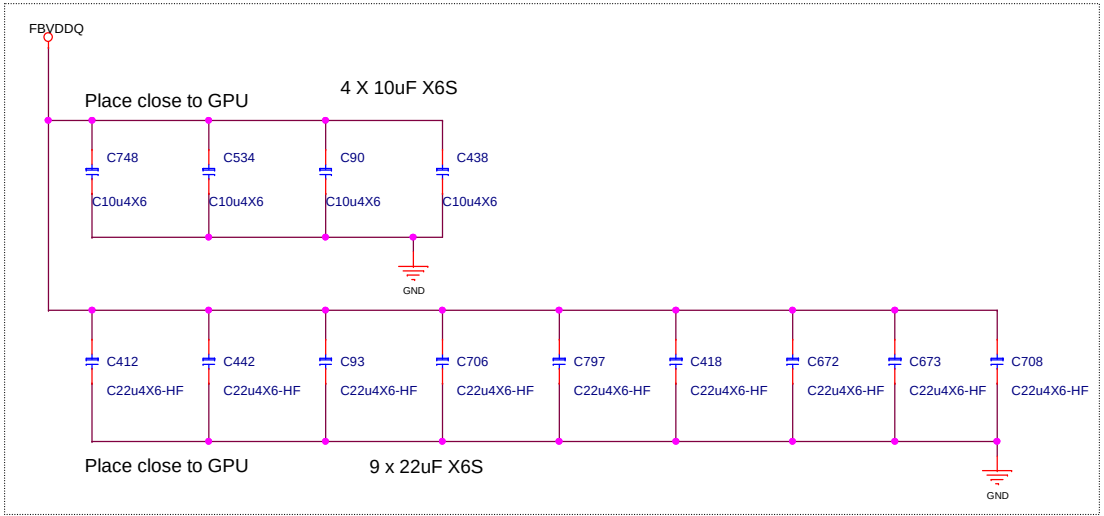
GPU DECOUPLING B

FBVDDQ



		DG Page 116	CRB
FBVDDQ (GPU side)	Under	24 X 1uF(0402 X6S) 5 X 10uF(0603 X6S)	24 X 1UF(0402 X6S 6.3V) 5 X 10uF(X6S 4V)
	Near	7 X 10uF(0603 X6S) 9 X 22uF(0603 X6S)	7 X 10uF(0603 X6S 4V) 9 X 22UF(0603 X6S 4V)



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING B

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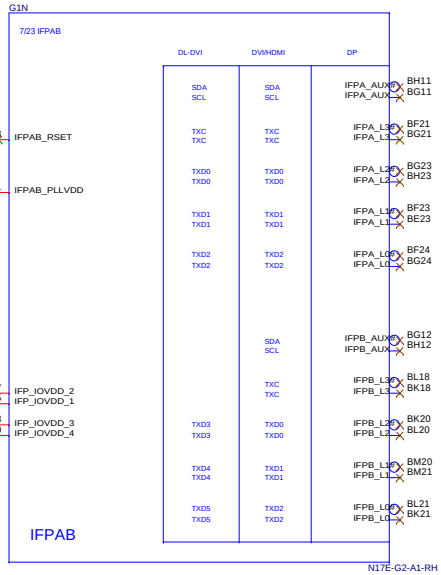
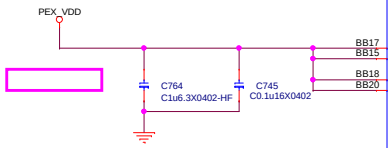
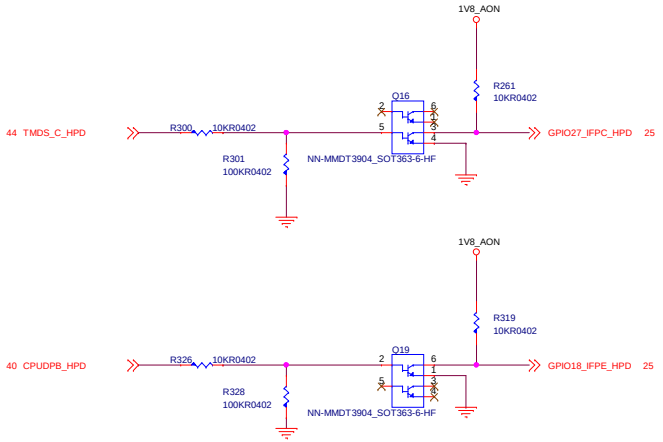
DG Page 117	Under GPU	Near GPU
IFP_IOVDD	12 X 0.1uF(0402 X6S)	3 X 4.7uF (0603) 3 X 1uF (0402)

0.305A for each IFP_IOVDD in use

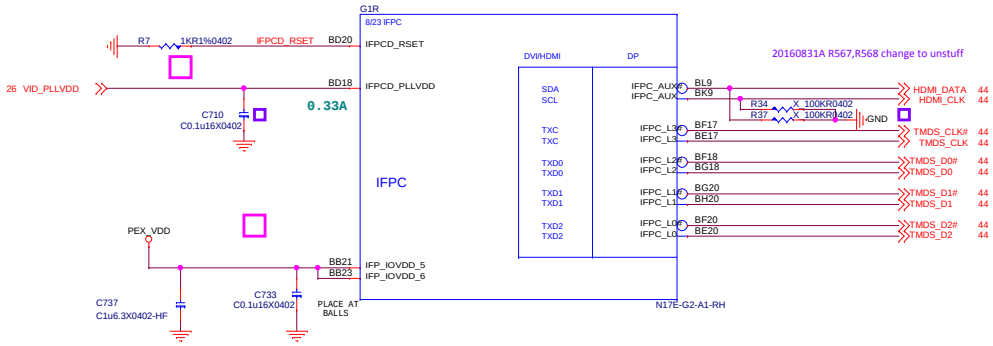
20160922 Delete R560 1KR & IFPAB_RSET



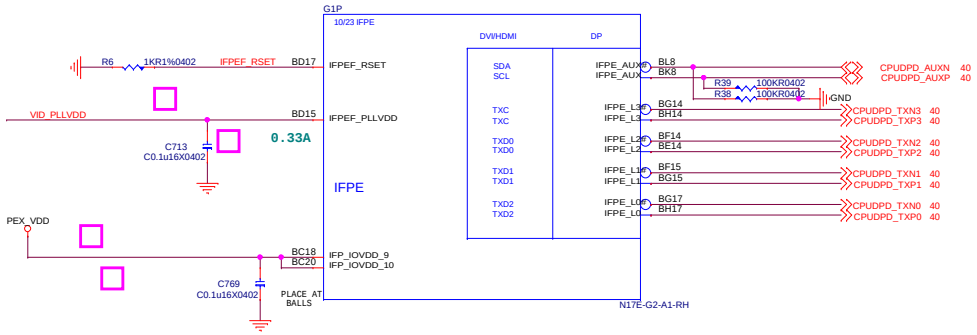


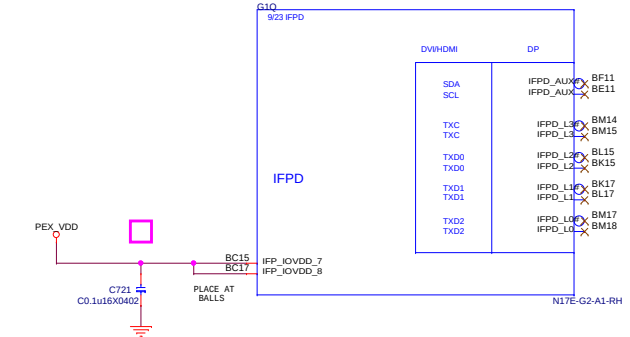


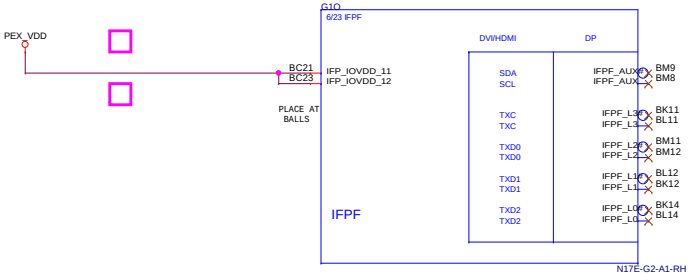
20160914 Delete R562,R564,R565,R583 & GPIO14_IFPA_HPD,GPIO15_IFPB_HPD,GPIO17_IFPD_HPD,GPIO24_IFPF_HPD



20160831A R567,R568 change to unstuff







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Title: DGPU_DACA,Display IF

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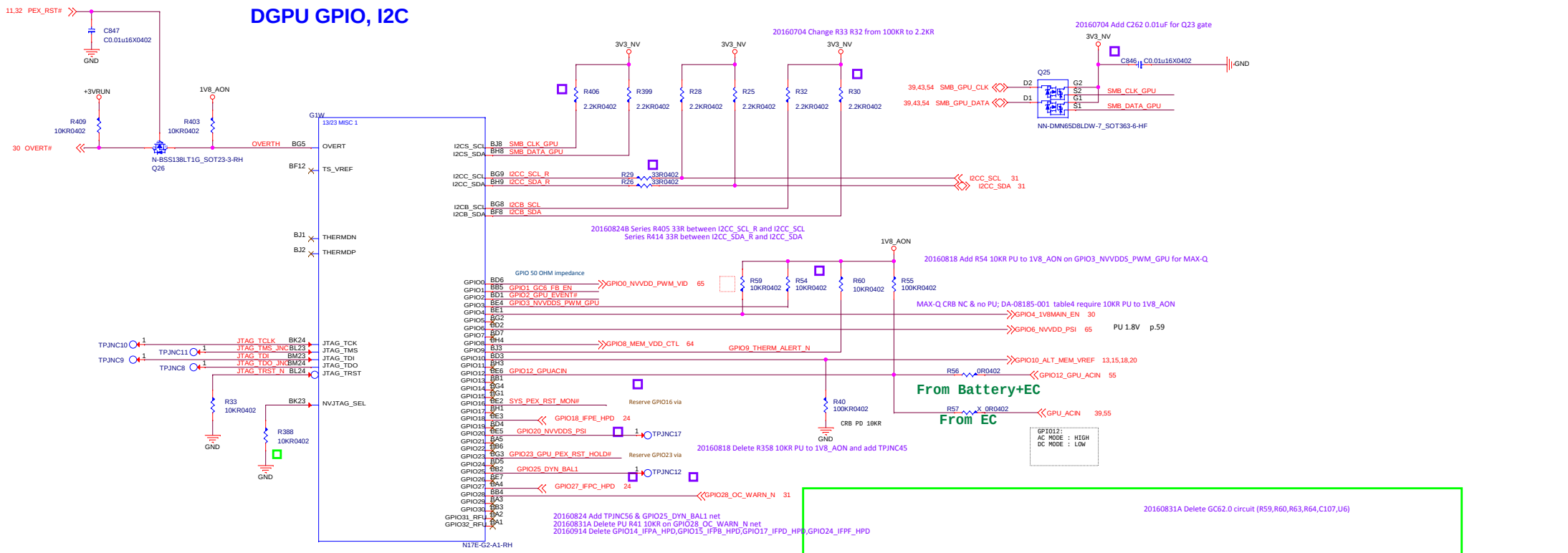
DGPU GPIO, I2C



Pin Number	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source, 10K pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDDS_PWM	O	PWM output to control the NVVDDS power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Fram Lock	OD, 10K pull-up to 1V8 _AON
GPIO6	NVVDD_PSI#/NVVDDS_PSI#	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight enable control signal to turn on a logo LED	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT#	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD; Quadro: Power_Brake#	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	
GPIO14	HPD_IFPA#	I	Hot Plug Detect for IFPA	Inverted input
GPIO15	HPD_IFPB#	I	Hot Plug Detect for IFPB	Inverted input
GPIO16	GC6M: SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_IFPD#	I	Hot Plug Detect for IFPD	Inverted input
GPIO18	HPD_IFPE#	I	Hot Plug Detect for IFPE	Inverted input
GPIO19	3DVision/STEREO	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE	I/O		
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI Swap Ready Out	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIE self-reset control	OD, 10K pull-up to gated 3V3
GPIO24	HPD_IFPF#	I	Hot Plug Detect for IFPF	Inverted input
GPIO25	Unused	I/O		
GPIO26	Unused	I/O		
GPIO27	HPD_IFPC#	I	Hot Plug Detect for IFPC	Inverted input
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10K pull-up to 1V8 _AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	Unused	I/O		

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPIO,I2C

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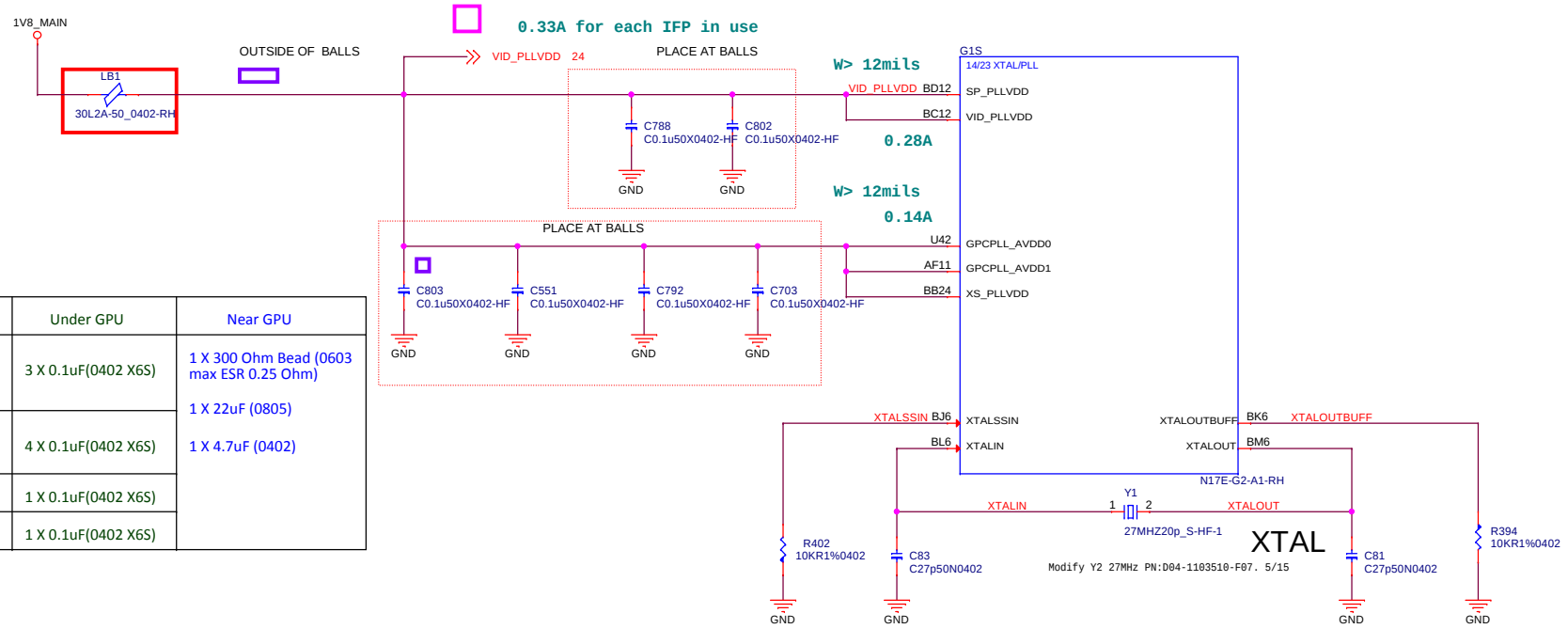
20160704 Add C1041 22uF & C1038 4.7uF & C1040 0.1uF for VID_PLLVDD

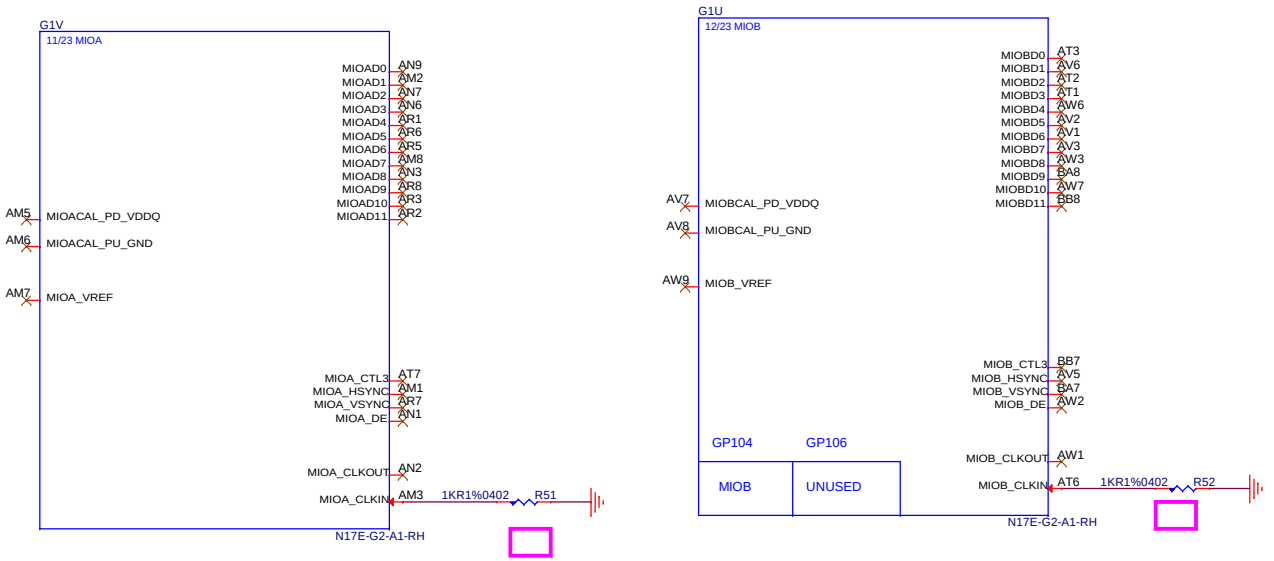
20160912A Delete C1041 & C1038

DGPU MIO & XTAL



DG Page 117	Under GPU	Near GPU
IFPAB_PLLVDD IFPCD_PLLVDD IFPEF_PLLVDD	3 X 0.1uF(0402 X6S)	1 X 300 Ohm Bead (0603 max ESR 0.25 Ohm) 1 X 22uF (0805)
GPCPLL_AVDDx XS_PLLVDD	4 X 0.1uF(0402 X6S)	1 X 4.7uF (0402)
SP_PLLVDD	1 X 0.1uF(0402 X6S)	
VID_PLLVDD	1 X 0.1uF(0402 X6S)	

Multi-use IO(MIO) Interface



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Title: DGPU MIO & XTAL

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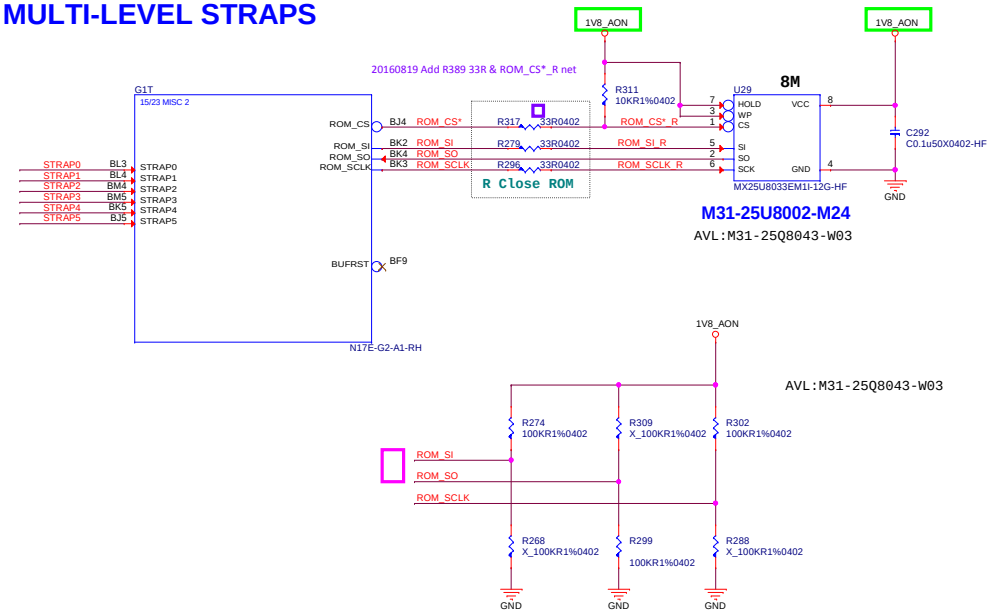
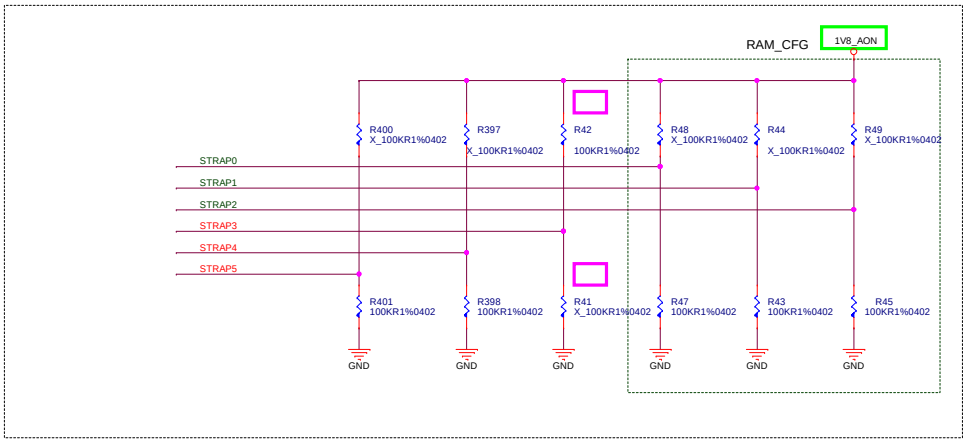
ROM, MULTI-LEVEL STRAPS





DEFAULT SETTING SAMSUNG	V_TOP1 5010 M12-8032535-S02 X_K4G80325FB-HC25-HF	256M*32
MICRON	V_TOP2 5010 M12-2563215-M30 X_MT51J256M32HF-80-A-HF	256M*32

20160817 Delete V_TOP3 M12-5GQ4H45-H23 and V_TOP4 M12-41325D5-S02

STRAP2	STRAP1	STRAP0	RAMCFG[2:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

256M*32
SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100 V	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

SOR_EXPOSED :GPU AUDIO SETTING

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT V
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE (DUAL GPU)
0:SMB_ALT_ADDR DISABLE (SINGLE GPU)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW SWING POWER
0:PCIE_CFG HIGH SWING POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

MICRO-STAR INT'L CO.,LTD.

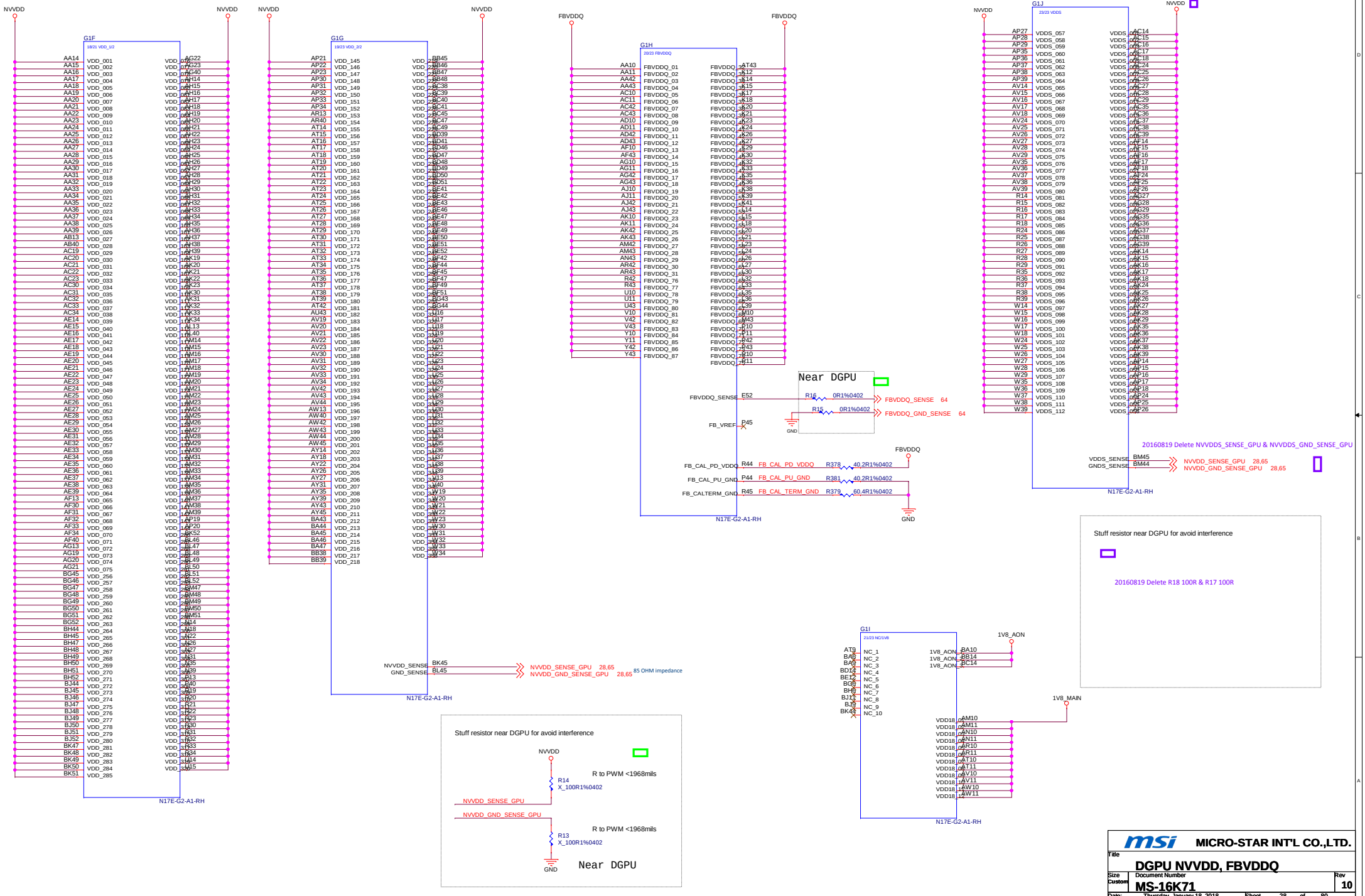
Title: DGPU_ROM,HW Straps

Size: Custom | Document Number: MS-16K71 | Rev: 10

Date: Thursday, January 18, 2018 | Sheet 27 of 80

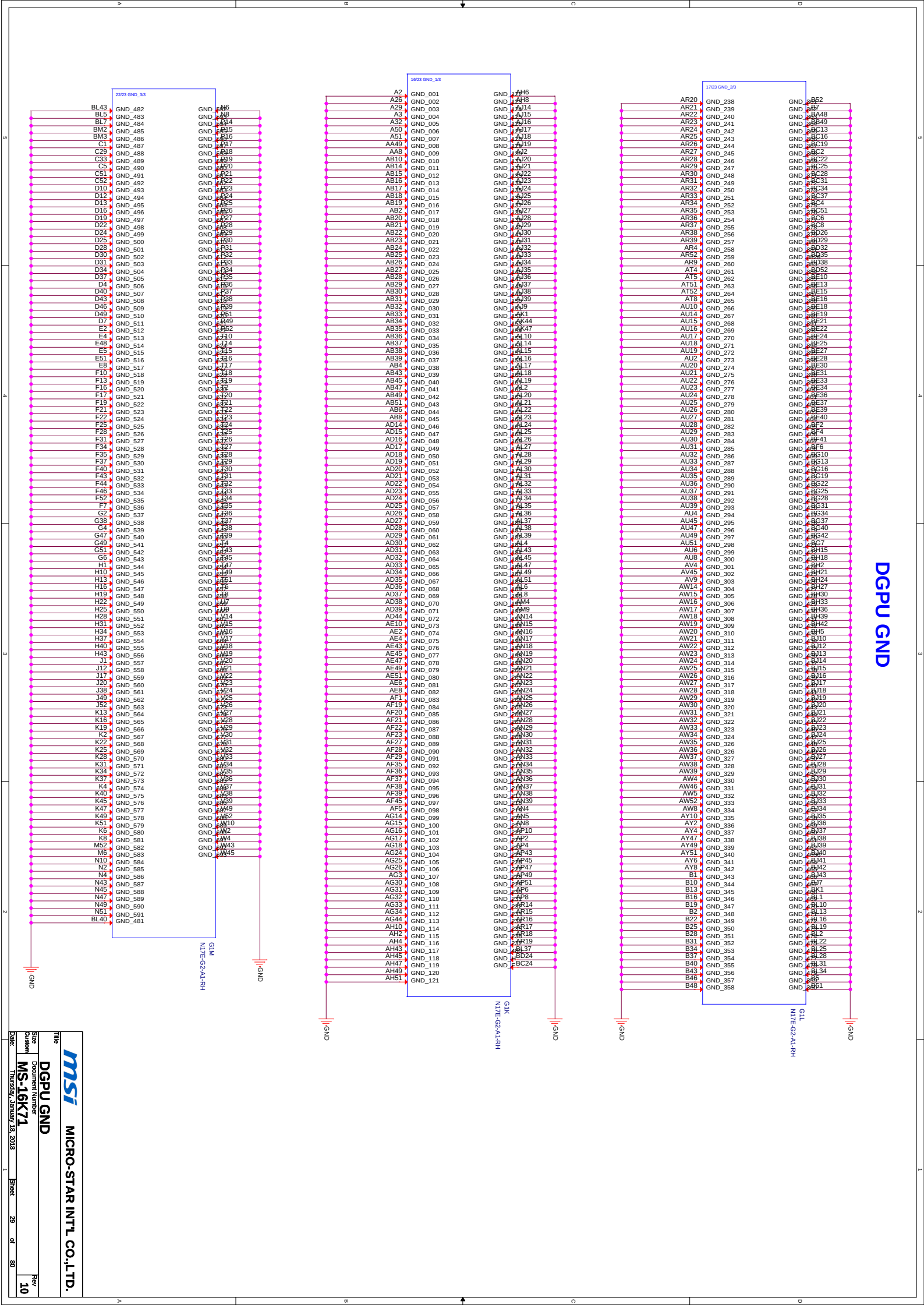
GPU NVVDD, FBVDDQ

20160819 Change VDDS connect to NVVDD



Title	DGPU NVVDD, FBVDDQ		
Size: Custom	Document Number: MS-16K71		Rev: 10
Date: Thursday, January 18, 2018	Sheet 28 of 80		

MICRO-STAR INT'L CO.,LTD.


DGPU GND
22/23 GND_3/3
16/23 GND_1/3
17/23 GND_2/3
G1M N17E-G2-A1-RH
G1K N17E-G2-A1-RH
G1L N17E-G2-A1-RH
GND
MICRO-STAR INT'L CO.,LTD.
Title
DGPU GND
Size
Custom
Document Number
MS-16K71
Rev
10
Date:
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Sheet
29
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80

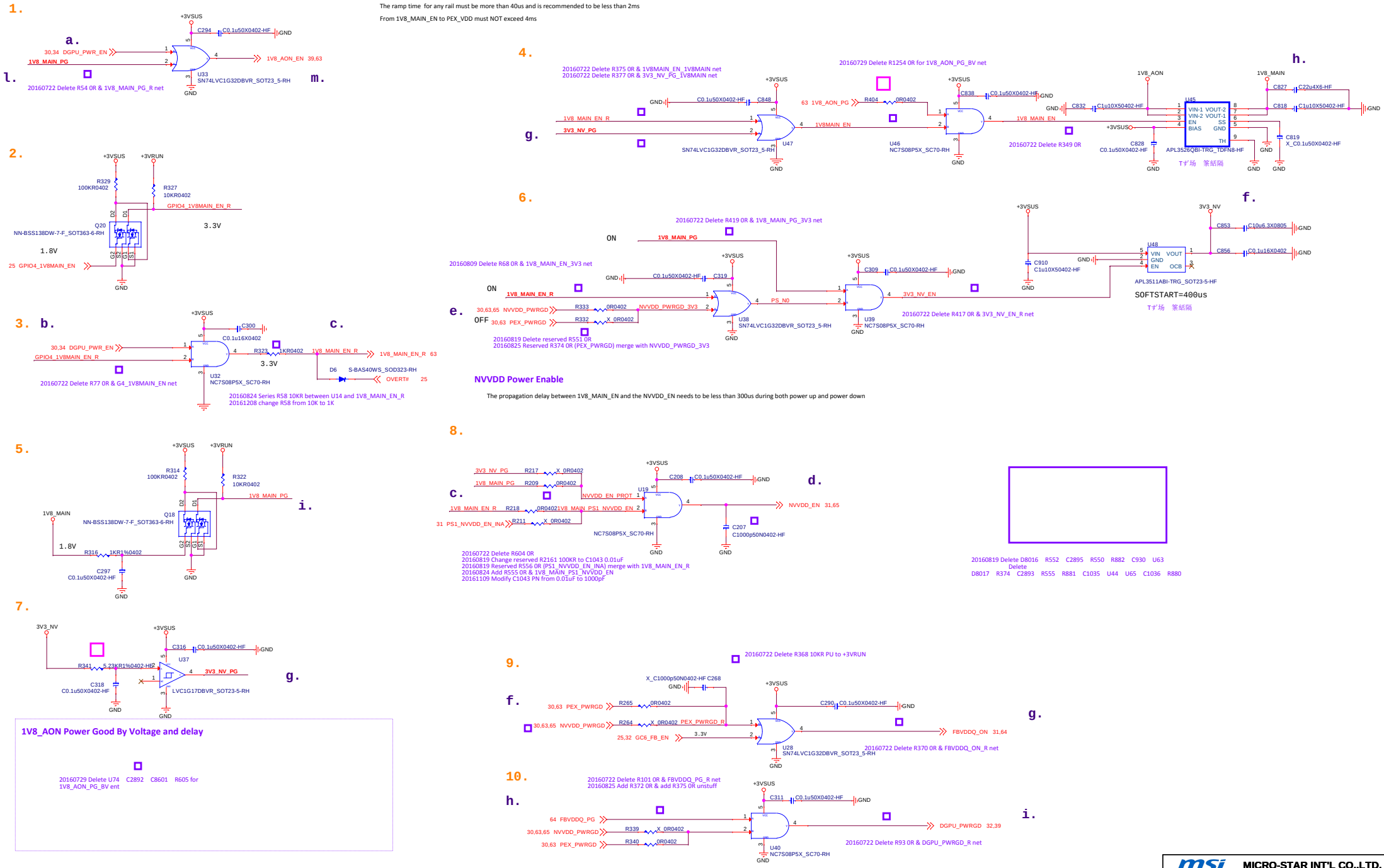
nVIDIA Power Sequence Control

Power on = 1V8_AON ->1V8_MAIN->3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power off= DGPUPWREN->(PEX_VDD->NVVDDQ->3V3_NV)->FBVDDQ->1V8_MAIN->1V8_AON

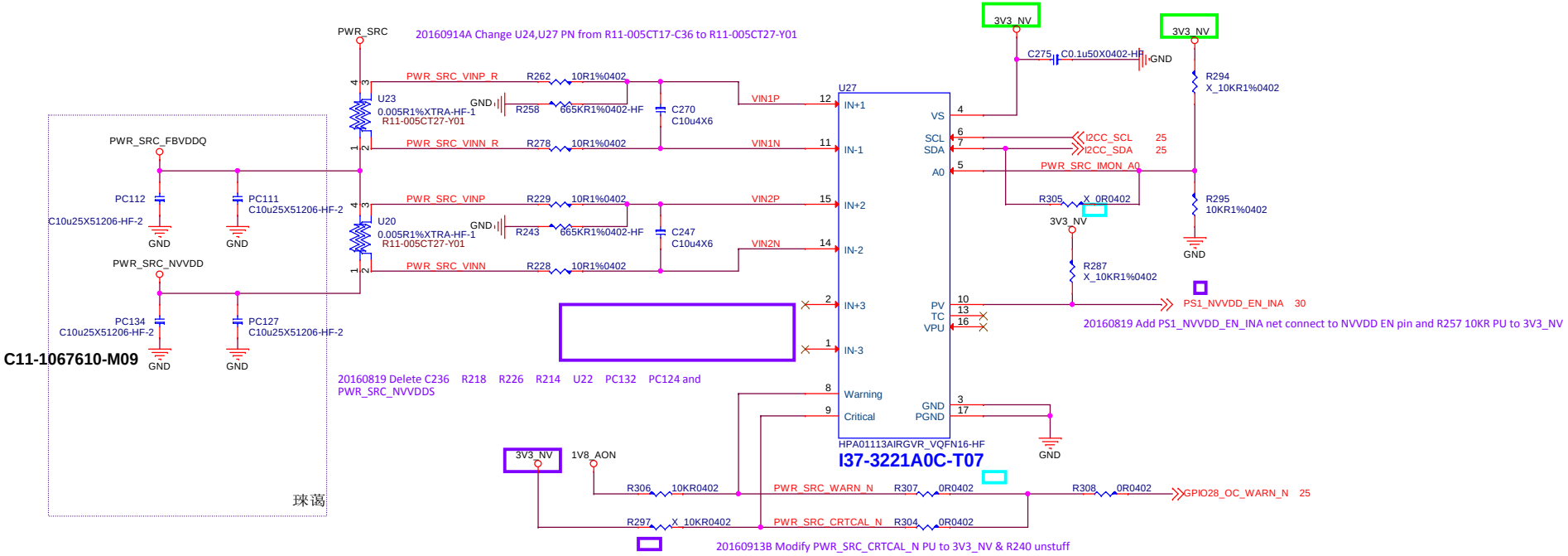
The ramp time for any rail must be more than 40us and is recommended to be less than 2ms

From 1V8_MAIN_EN to PEX_VDD must NOT exceed 4ms



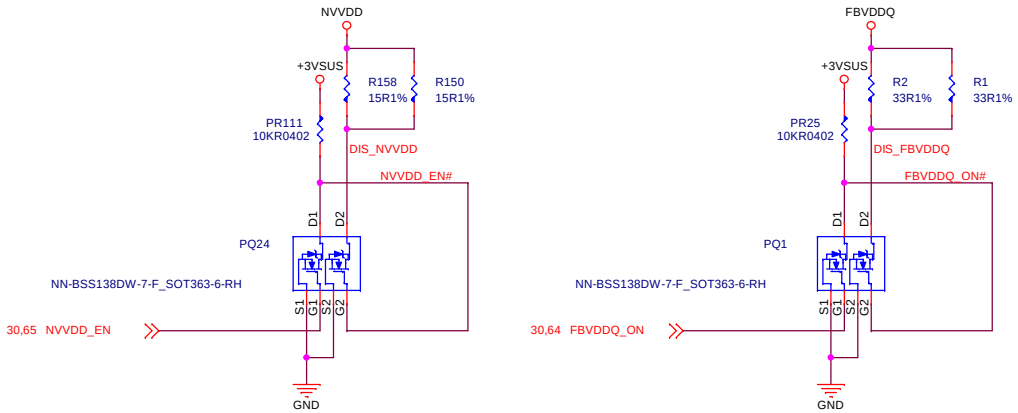
MSI	MICRO-STAR INT'L CO.,LTD.		
Title	DGPU_Power Sequence		
Size	Document Number MS-16K71		Rev 10
Date:		Sheet 30 of 80	

DGPU_Power Control



Discharge

20160819 Delete NVVDDS discharge
(PQ30 PR160 PC98 Q47)



20160722 Delete 3V3_NV discharge
circuit(Q41 R556 R557 R558 R559)

PEX_VDD ず场 篆4ms

3V3_AONず场 篆 2ms

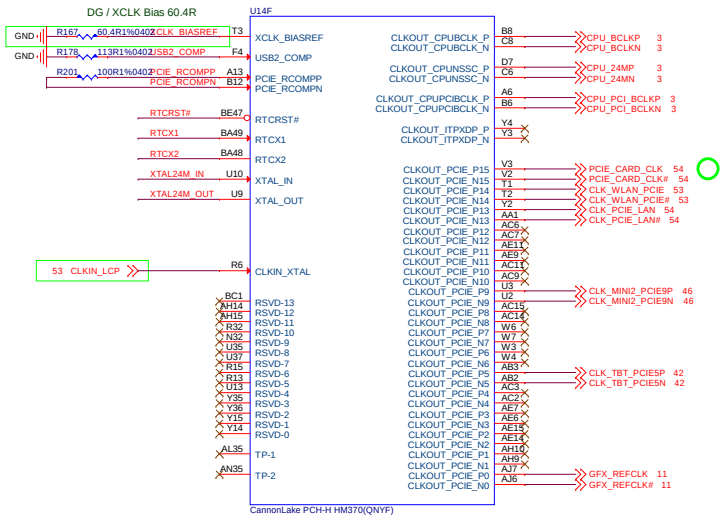
1V8AONず场 篆2ms

1V8_MAINず场 篆320us

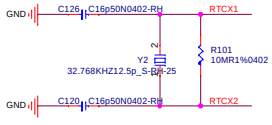
MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Discharge	
Size: Custom	Document Number: MS-16K71	Rev: 10
Date: Thursday, January 18, 2018	Sheet 31 of 80	

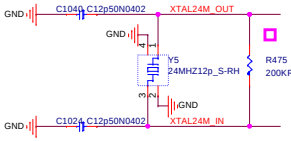
HM370 (RTC/PCIE_Clock/Clock/RSVD)



RTC Block(Close to PCH)



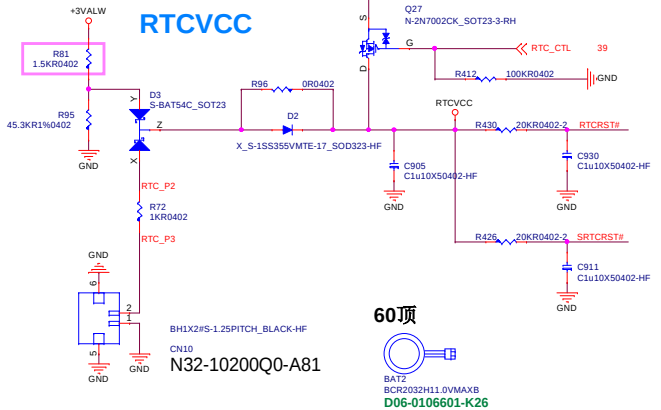
24MHz Clock



20170828 R2175 change to 200K to follow DG and CRB

20170731 change R2185 to 1.5K to follow DG

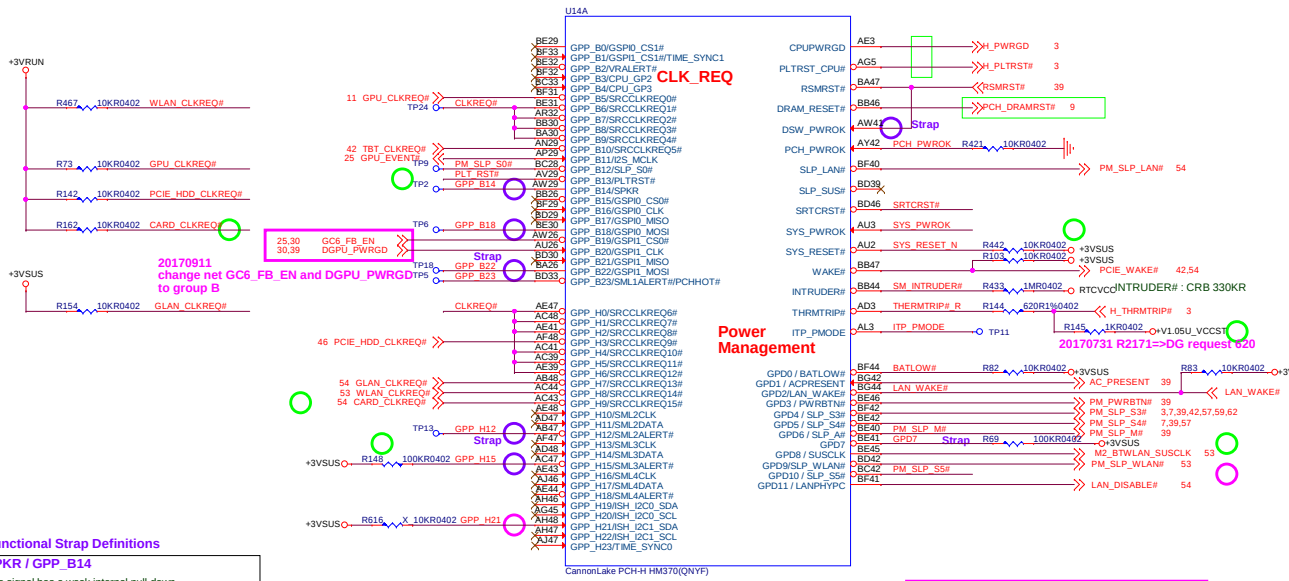
RTCVCC



60项

BAT2
BCR2032H11.0VMAXB
D06-0106601-K26

HM370 (CLKREQ/ACPI)



20170911
change net GC6_FB_EN and DGPU_PWRGD to group B

20170731 R2171=>DG request 620

Functional Strap Definitions

SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

GSPI0_MOSI / GPP_B18
The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

GSPI1_MOSI / GPP_B22
This Signal has a weak internal pull-down.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC

SML1ALERT# / PCHHOT#/ GPP_B23
This signal has an internal pull-down.

GPP_H12
This signal has a weak internal pull-down.

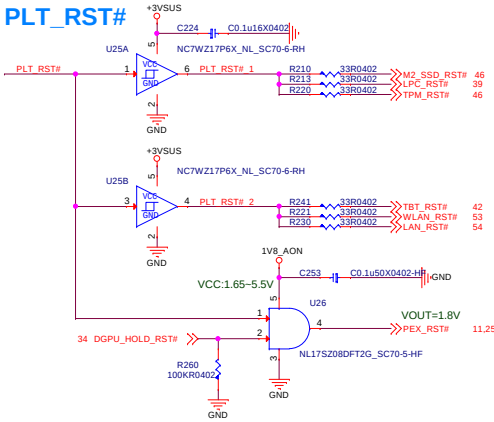
GPP_H15
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

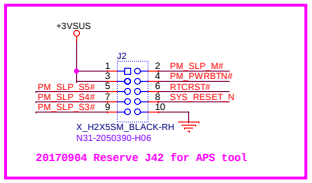
GPPD7
External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

DG/ RTC Well Input Strap
RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

Strap pin
GPP_H21 pull-up for 24 MHz XTAL operation for PCH-LP
20171005 change to unstuff for PCH-H

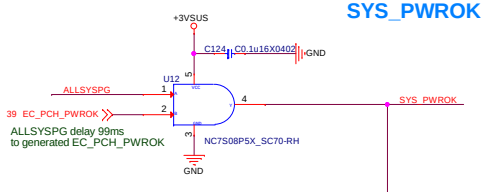
PLT_RST#



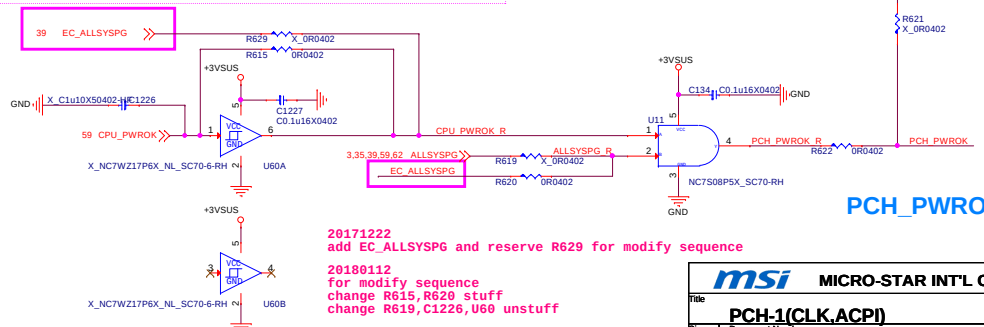


20170904 Reserve J42 for APS tool

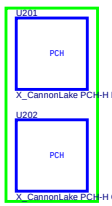
SYS_PWROK



PCH_PWROK



PCH type



20171222
add EC_ALLSYSPG and reserve R629 for modify sequence

20180112
for modify sequence
change R615,R620 stuff
change R619,C1226,U60 unstuff

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-1(CLK,ACPI)	
Size	Document Number MS-16K71	Rev 10
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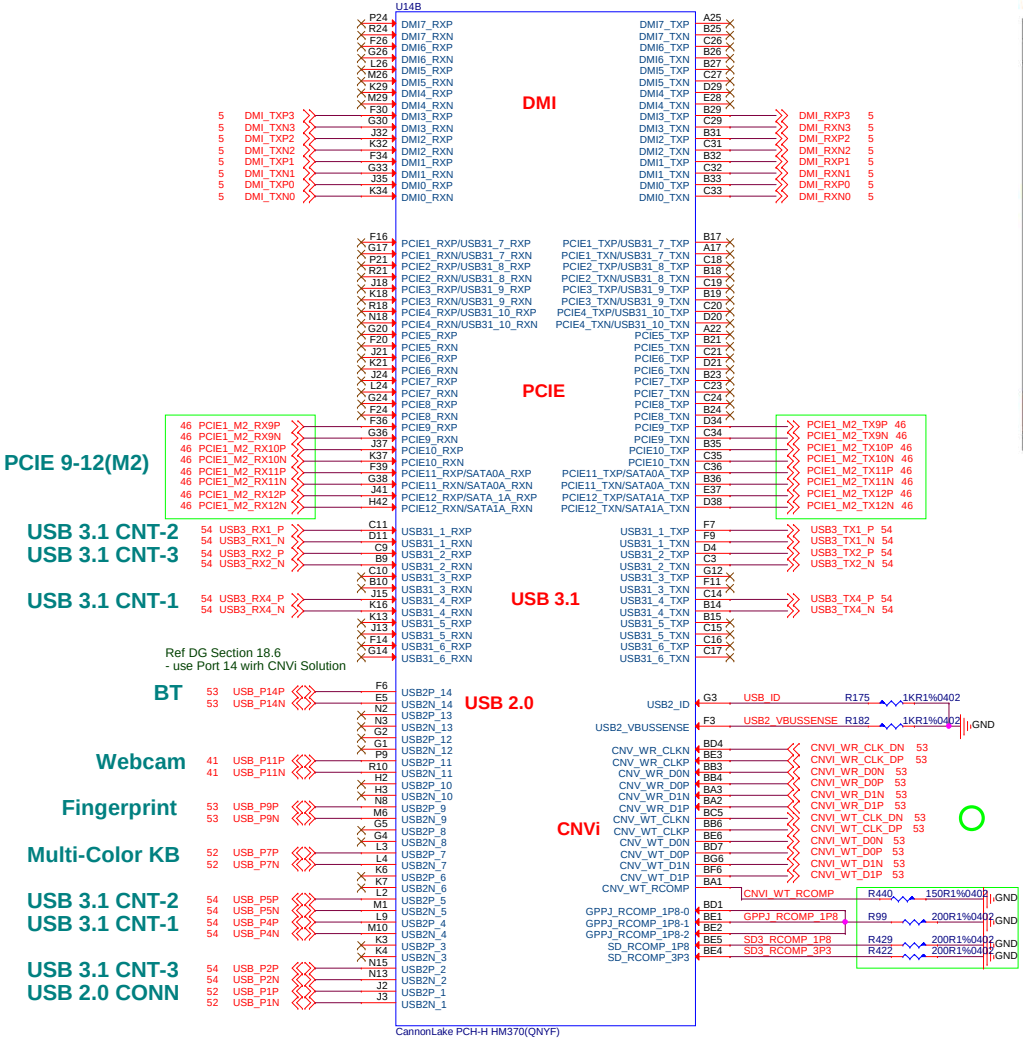
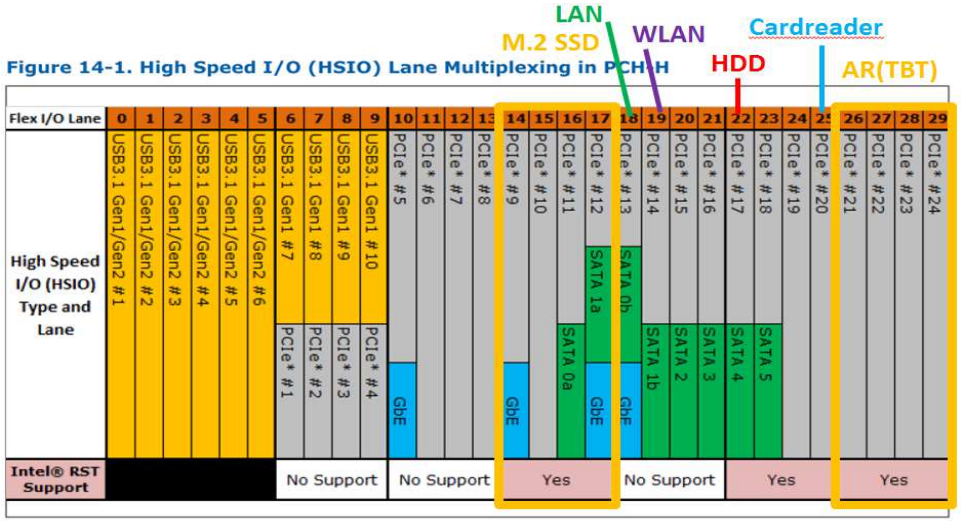
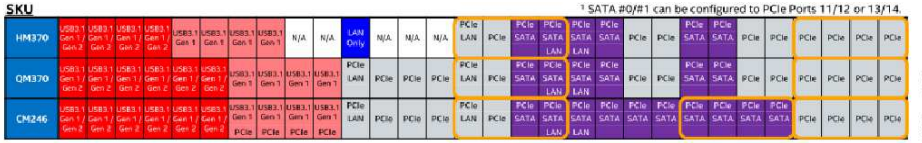
HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)







- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

msi	MICRO-STAR INT'L CO.,LTD.	
Title	PCH-2(DMI/PCIE/USB)	
Size	Document Number MS-16K71	Rev 10
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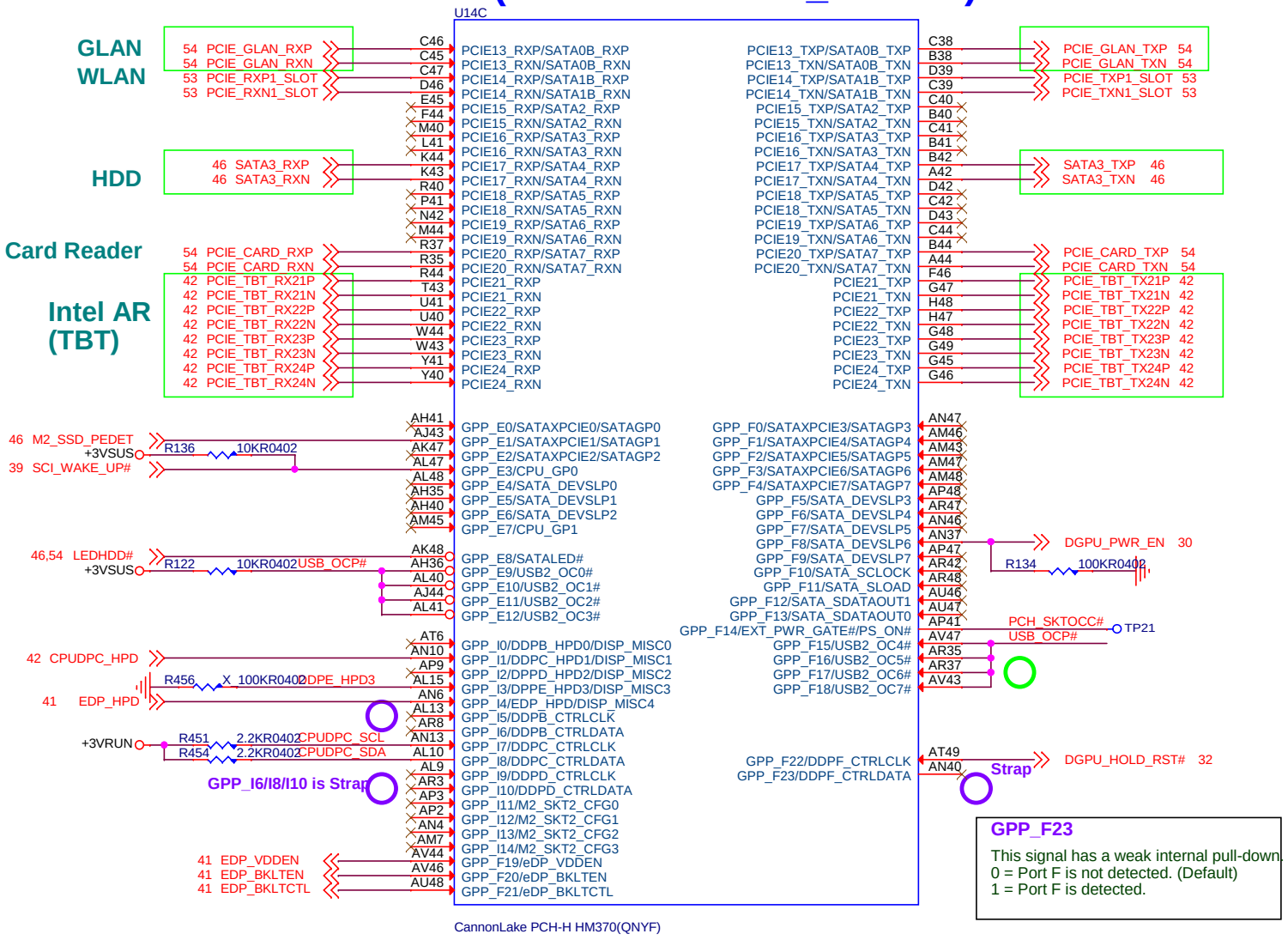
HM370(SATA/PCIE/USB_OC/DDI)



CannonLake PCH-H HM370(QNYF)

Functional Strap Definitions

DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

MICRO-STAR INT'L CO.,LTD.

Title: PCH-3(SATA/PCIE/USB_OC/DDI)

Size: Custom | Document Number: MS-16K71 | Rev: 10

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HM370 (HDA/GPIO/TJAG)

Functional Strap Definitions

SMBALERT# / GPP_C2

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

SML0ALERT# / GPP_C5

This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

HDA_SDO

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

+3VSUS
R617 X_4.7KR0402
GPP_C2
R618 X_20KR0402-2
+3VSUS
R76 2.2KR0402 SUS_SMBCLK
R77 2.2KR0402 SUS_SMBDATA
SML0_CLK_R
SML0_DATA_R
GPP_C5
TP8
Strap
+3VSUS R78 X_10KR0402
1 = eSPI Is selected for EC.

20170801
delete C8613
add C8888,C8889,C8890,C8891,C8892
to follow DG

U14D

SMBUS
GPP_C0/SMBCLK BE26
GPP_C1/SMBDATA BF26
GPP_C2/SMBALERT# BE25
GPP_C3/SML0CLK BF25
GPP_C4/SML0DATA BE24
GPP_C5/SML0ALERT# BF24
GPP_C6/SML1CLK BF27
GPP_C7/SML1DATA BE27
GPP_C8/UART0_RXD BE23
GPP_C9/UART0_TXD BB24
GPP_C10/UART0_RTS# BA24
GPP_C11/UART0_CTS# AP24
GPP_C12/UART1_RXD/ISH_UART1_RXD AU24
GPP_C13/UART1_TXD/ISH_UART1_TXD AP21
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AW24
GPP_C15/UART1_CTS#/ISH_UART1_CTS# BD21
GPP_C16/I2C0_SDA BF23
GPP_C17/I2C0_SCL BC22
GPP_C18/I2C1_SDA BF21
GPP_C19/I2C1_SCL BE21
GPP_C20/UART2_RXD BD20
GPP_C21/UART2_TXD BE20
GPP_C22/UART2_RTS# AW21
GPP_C23/UART2_CTS# AV21

GPIO
GPP_D0/SPI1_CS#/SBK0/BK0 BF19
GPP_D1/SPI1_CLK/SBK1/BK1 BE19
GPP_D2/SPI1_MISO/SBK2/BK2 BE18
GPP_D3/SPI1_MOSI/SBK3/BK3 BF18
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4 BE15
GPP_D5/I2S2_SFRM/CNV_RF_RESET# BE16
GPP_D6/I2S2_TXD/MODEM_CLKREQ BA17
GPP_D7/I2S2_RXD AW18
GPP_D8/I2S2_SCLK AV18
GPP_D9/ISH_SPI_CS#/GSPI2_CS0# BA20
GPP_D10/ISH_SPI_CLK/GSPI2_CLK BB20
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO BB16
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI AN18
GPP_D13/ISH_UART0_RXD/I2C2_SDA BE17
GPP_D14/ISH_UART0_TXD/I2C2_SCL BF17
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN AR18
GPP_D16/ISH_UART0_CTS#/CNV_WCEN BF14
GPP_D17/DMIC_CLK1/SNDW3_CLK AW15
GPP_D18/DMIC_DATA1/SNDW3_DATA AV16
GPP_D19/DMIC_CLK0/SNDW4_CLK BD16
GPP_D20/DMIC_DATA0/SNDW4_DATA BF15
GPP_D21/SPI1_IO2 BD17
GPP_D22/SPI1_IO3 BC17
GPP_D23/ISH_I2C2_SCL/I2C3_SCL BE14

CNVI_RF_RESET 53
MODEM_CLKREQ 53

20170911
change net GC6_FB_EN and DGPU_PWRGD
to group B

TP25
TP26
TP27
TP28

47 CODEC_HDA_BITCLK
R85 33R0402
C102 C2p50N0402
47 CODEC_HDA_RST#
R92 33R0402
C106 C2p50N0402
HDA_BCLK BD11
HDA_RST_N BE10
C113 C2p50N0402
47 CODEC_HDA_SDIN0
CODEC_HDA_SDIN0 BF10
C104 C2p50N0402
47 CODEC_HDA_SDOUT
39 FLASH_SECURITY
47 CODEC_HDA_SYNC
R90 33R0402
R86 1KR1%0402
R91 33R0402
C105 C2p50N0402
HDA_SDO BF12
HDA_SYNC BG13
Strap
5 DISPA_BCLK
5 DISPA_SDI
5 DISPA_SDO
R105 30R0402 DISPA_BCLK_R AM3
R109 30R0402 DISPA_SDO_R AM2
AN3
BD12
BE12

AUDIO
HDA_BCLK/I2S0_SCLK
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
HDA_SDI0/I2S0_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDACPU_SCLK
HDACPU_SDI
HDACPU_SDO
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA

20170731 change R2352 and R2353 to 30R to follow DG

53 M2_WLAN_CL_CLK AR2
53 M2_WLAN_CL_DATA AT5
53 M2_WLAN_CL_RST# AU4
CL_CLK
CL_DATA
CL_RST#

2016012 Add M2_WLAN_CL_CLK, M2_WLAN_CL_DATA, M2_WLAN_CL_RST# for WLAN

TJAG
CPU_TRST# AM4 H_TRST_N_R 3
PCH_JTAG_TCK AJ3 TP12
PCH_JTAG_TDI AH2 CPU_TDI 3
PCH_JTAG_TMS AJ4 CPU_TMS 3
PCH_JTAGX AH4 CPU_TCK 3
PCH_JTAG_TDO AH3 CPU_TDO 3
PRDY# AM5 H_PRDY_N 3
PREQ# AL2 H_PREQ_N 3
TRIGGER_IN AK2
TRIGGER_OUT AK3 TRIGGER_OUT_R121 30R0402 CPU_2_PCH_TRIGGER_R 7 PCH_2_CPU_TRIGGER_R 7

CannonLake PCH-H HM370(QNYF)

+V1.05DX_VCCSTG
CPU_TDO R133 100R0402
CPU_TDI R135 51R0402
CPU_TMS R123 51R0402
Connected JTAG PU to VCCST-G on H line

ref DG / Chapter Platform and Test Hooks
CPU_TDO : PU 100R Near CPU (DG : R1)
PU 100R Near PCH (DG : R3)
CPU_TDI : PU 51R Near PCH (DG : R4)
CPU_TMS : PU 51R Near PCH (DG : R2)
CPU_TCK : 51R to GND Near CPU (DG : R2)

SMB Isolation

+3VSUS
+3VRUN
R246 1KR1%0402
R263 1KR1%0402
Q14 NN-DMN65D8LDW-7_SOT363-6-HF
D2 D1 G2 S2 G1 S1
PWRGD PS SMBUS ISOLATE
3,32,39,59,62 ALLSYSPG
GND
+3VRUN
R247 2.2KR0402
R269 2.2KR0402
NN-DMN65D8LDW-7_SOT363-6-HF
Q13
SUS_SMBCLK
SUS_SMBDATA
D1 D2 S1 G1 S2 G2
SMB_CLK_DIMM 9,10,40,53
SMB_DATA_DIMM 9,10,40,53
C246 X_C0.1u16X0402
C271 X_C0.1u16X0402
C266 C0.1u16X0402
GND GND GND

54 SML0_CLK
54 SML0_DATA
R411 X_0R0402 SML0_CLK_R
R410 X_0R0402 SML0_DATA_R
EC28 X_C10p50N0402
EC29 X_C10p50N0402
+3VSUS
R75 499R1%0402 SML0_CLK_R
R74 499R1%0402 SML0_DATA_R

MICRO-STAR INT'L CO.,LTD.

Title: PCH-4(HDA/GPIO/TJAG)
Size: Custom
Document Number: MS-16K71
Rev: 10
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20170731 change R2226 unstuff to follow CRB

HM370 (UART/I2C/SPI)

CLK_PCI_KBC CI8 — X_C10p50N0402 — GND
CLK_PCI_TPM CI6 — X_C10p50N0402 — GND

U14E

+3VRUN

39 KBRST#
39,46 LAD0
39,46 LAD1
39,46 LAD2
39,46 LAD3
39,46 LPC_FRAME#
R68 10KR040
39,46 INT_SERIRQ — R87 — 10KR1%0402 — LPC_PIRQ_PU
+3VSUS
EC_CLKRUN# R — AV32
39 CLK_PCI_KBC — R438 — 22R0402 — CLK_PCI_KBC_R
46 CLK_PCI_TPM — R420 — 22R0402 — CLK_PCI_TPM_R
+3VSUS — R89 — 10KR0402 — PME#
39 SUSPWRDNACK
39 ECESPI_RST#
TP3 GPP_A15

+3VSUS
R71 10KR1%0402
EC_CLKRUN# R — R88 — 0R0402 — EC_CLKRUN# 39
R70 — X_10KR0402 — GND

GPP_K7
GPP_K10
42 TBT_CIO_PLUG_EVENT#
42 TBT_FORCE_PWR_R
39 KBSCI#

EDS:SCI capabillity is available on all GPIOs

BE39 GPP_A0/RCIN#/ESPI_ALERT1#
BB39 GPP_A1/LAD0/ESPI_IO0
AW37 GPP_A2/LAD1/ESPI_IO1
AV37 GPP_A3/LAD2/ESPI_IO2
BA38 GPP_A4/LAD3/ESPI_IO3
BE38 GPP_A5/LFRAME#/ESPI_CS0#
AW35 GPP_A6/SERIRQ/ESPI_CS1#
BA36 GPP_A7/PIRQA#/ESPI_ALERT0#
BB36 GPP_A8/CLKRUN#
BB34 GPP_A9/CLKOUT_LPC0/ESPI_CLK
BE36 GPP_A10/CLKOUT_LPC1
BF36 GPP_A11/PME#/SD_VDD2_PWR_EN#
BC37 GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
BF38 GPP_A13/SUSWARN#/SUSPWRDNACK
BE35 GPP_A14/SUS_STAT#/ESPI_RESET#
BE33 GPP_A15/SUSACK#
BD38 GPP_A16/CLKOUT_48
BF35 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
BD34 GPP_A18/ISH_GP0
BE34 GPP_A19/ISH_GP1
BA33 GPP_A20/ISH_GP2
AW32 GPP_A21/ISH_GP3
AV34 GPP_A22/ISH_GP4
GPP_A23/ISH_GP5

LPC

N48 GPP_K4
N47 GPP_K5
P47 GPP_K6
R46 GPP_K7
P48 GPP_K8
V47 GPP_K9
V48 GPP_K10
W47 GPP_K11
Y46 GPP_K12/GSXDOUT
Y48 GPP_K13/GSXSLOAD
W46 GPP_K14/GSXDIN
AA45 GPP_K15/GSXSRESET#
Y47 GPP_K16/GSXCLK
R47 GPP_K17/ADR_COMPLETE
T47 GPP_K18/NMI#
T48 GPP_K19/SMI#
T46 GPP_K20
T45 GPP_K21
L48 GPP_K22/IMGCLKOUT0
M45 GPP_K23/IMGCLKOUT1

CannonLake PCH-H HM370(QNYF)

AW13 GPP_G0/SD_CMD
BE9 GPP_G1/SD_D0
BF8 GPP_G2/SD_D1
BF9 GPP_G3/SD_D2
BG8 GPP_G4/SD_D3
BE8 GPP_G5/SD_CD#
BD8 GPP_G6/SD_CLK
AV13 GPP_G7/SD_WP
KBSMI# 39
EDS:GPP_G[7:0] (support SMI# only)

AV6 GPP_J0/CNV_PA_BLANKING — TP19
AY3 GPP_J1/CPU_VCCIO_PWR_GATE# — CPU_C10_GATE# 7,62
AW3 GPP_J2
AT10 GPP_J3

Strap

AV4 GPP_J4/CNV_BRI_DT/UART0_RTS# — CNVI_BRI_DT 53 — GPP_J4
AY2 GPP_J5/CNV_BRI_RSP/UART0_RXD — CNVI_BRI_RSP 53
BA4 GPP_J6/CNV_RGI_DT/UART0_TXD — CNVI_RGI_DT 53 — GPP_J6
AV3 GPP_J7/CNV_RGI_RSP/UART0_CTS# — CNVI_RGI_RSP 53
AW2 GPP_J8/CNV_MFUART2_RXD — TP10
AU9 GPP_J9/CNV_MFUART2_TXD — TP20
AV7 GPP_J10
AR13 GPP_J11/A4WP_PRESENT

L47 GPP_K0
L46 GPP_K1
U48 GPP_K2
U47 GPP_K3

DG / Single Flash Topology Table 29-3
(1) R use 50 Ohm for 3.3V
(2) SPIO_IO2/IO3 PU 1KR when using quad mode

GND — CI1 X_C10p50N0402

AW47 SPI0_CLK — PCH_SPI_CLK — R118 — 49.9R1%0402 — SPI_CLK
AY47 SPI0_CS0# — SPI_CS0#
AW48 SPI0_CS1#
AY48 SPI0_IO2 — PCH_SPI_WP# — R110 — 49.9R1%0402 — SPI_WP#
BA46 SPI0_IO3 — PCH_SPI_HOLD# — R108 — 49.9R1%0402 — SPI_HOLD#
BA45 SPI0_MISO — PCH_SPI_MISO — R443 — 49.9R1%0402 — SPI_MISO
AU41 SPI0_MOSI — PCH_SPI_MOSI — R439 — 49.9R1%0402 — SPI_MOSI
AT40 SPI0_CS2#

Strap Pin

AE2 PM_DOWN
AF3 PM_SYNC — PCH_PM_SYNC — R141 — 30R0402 — H_PM_DOWN 3 / H_PM_SYNC 3

AF2 PECI — PCH_PECI — R138 — X_10KR0402 — GND

CRB : PCH PECI 10KR NC

20170731 change R2228 to R11-0103012-W08
but no stuff following CRB

Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP_J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

SPI0_IO2

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_IO3

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

MISO isn't Strap

2 170831
add R3535 and R3536 for GCoff

40 DP_HPD — R152 — 0R0402 — GPP_K7
39,44 HDMI_HPD_DET — R157 — 0R0402 — GPP_K10

BIOS ROM type

U401 — BIOS ROM for GS (16MB) — X_MX25L12873FM2I-10G-HF
U402 — BIOS ROM for WS (32MB) — X_S25FL256SAGNFI011-RH

SPI FLASH ROM 16MB

+VCCSPI : connect to +3VSUS

+VCCSPI — R338 1KR0402 — SPI_WP#
+VCCSPI — R337 1KR0402
GND — C284 C0.1u16X0402
+VCCSPI — R291 1KR0402
+VCCSPI — R292 100KR0402

39 SPI_CS0#
39 SPI_MISO

U34
1 CS — VCC 8
2 DO(IO1) — HOLD(IO3) 7 — SPI_HOLD#
3 WP(IO2) — CLK 6 — SPI_CLK 39
4 GND — DI(IO0) 5 — SPI_MOSI 39
GND
MX25L12873FM2I-10G-HF

20170809 U79 change from socket to ROM
P/N M31-2512832-M24

M31-2512893-W03
,M-IC FLASH,128M(16Mx8bit),10ms,SOIC-8pin(208mil),WINBOND/W25Q128JVSIQ,2.7V,3.6V,SPI,,HALOGEN FREE

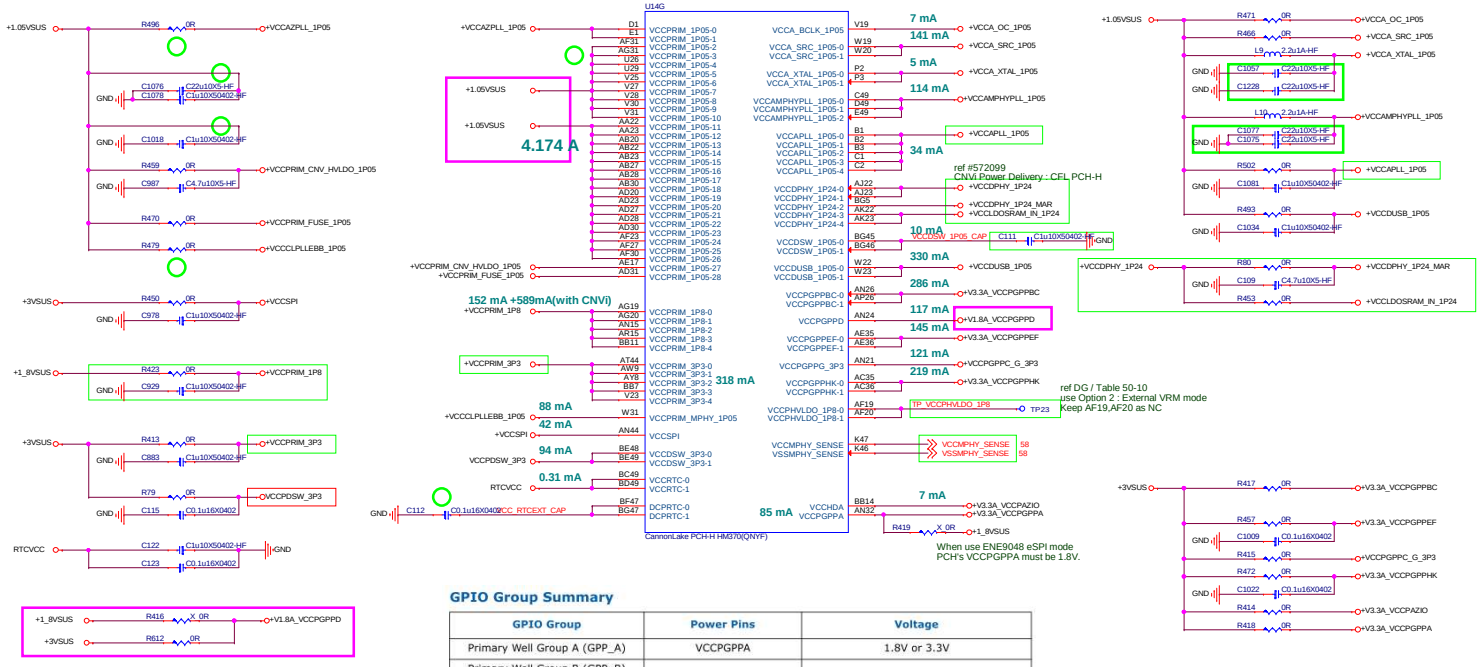
M31-2512832-M24
,M-IC FLASH,128M(16Mx8bit),40ms,SOP-8pin,MXICMX25L12873FM2I-10G(T),2.7V,3.6V,SPI,,HALOGEN FREE

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5(UART/I2C/SPI)
Size:
Document Number: MS-16K71
Rev: 10
Date: Thursday, January 18, 2018 Sheet 36 of 80

HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B) Primary Well Group C (GPP_C)	VCCPGPPBC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E) Primary Well Group F (GPP_F)	VCCPGPPEF	1.8V or 3.3V
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Power Descriptions for PCH in CNL-H

Name	Description
VCCA_BCLK_1P05	**Analog supply for BCLK circuitries**: 1.05V
VCCA_SRC_1P05	**Analog supply for PCIe clock circuitries**: 1.05V
VCCA_XTAL_1P05	**Analog supply for XTAL circuitries**: 1.05V
VCCDUSB_1P05	**Supply for USB digital logic**: 1.05V
VCCAPLL_1P05	**Analog supply for BCLK/DMI/Audio PLLs:** 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	**Primary Well**: 1.05V. For PCIe//USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVi.
VCCDSW_1P05	**Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	**Mod PHY Primary**: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers.
VCCAMPHYPLL_1P05	**Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs**: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P8	**1.8V Primary Well**.
VCCPRIM_3P3	**3.3V Primary Well**.
VCCSPI	**SPI Primary Well 3.3V or 1.8V**, for SPI interface.
VCCHDA	**HDA Audio Power 3.3V, 1.8V, or 1.5V**, for Intel® High Definition Audio.
VCCDSW_3P3	**3.3V Deep Sx Well**.
VCCRTC	**RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. ***Note:*** VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations. ***Note:*** Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCPGPPA	**1.8V or 3.3V for GPP_A group.**
VCCPGPPBC	**1.8V or 3.3V for GPP_B and GPP_C groups.**
VCCPGPPD	**1.8V or 3.3V for GPP_D group.**
VCCPGPPEF	**1.8V or 3.3V for GPP_E and GPP_F groups.**
VCCPGPPG_3P3	**3.3V for GPP_G group.**
VCCPGPPHK	**1.8V or 3.3V for GPP_H and GPP_K groups.**
VCCMPHY_SENSE	**1.05V Sense Line.**
VSSMPHY_SENSE	**0V (Ground) Sense Line.**
VSS	**Ground.**

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Title: PCH-6(Power)

Size: Custom | Document Number: MS-16K71 | Rev: 10

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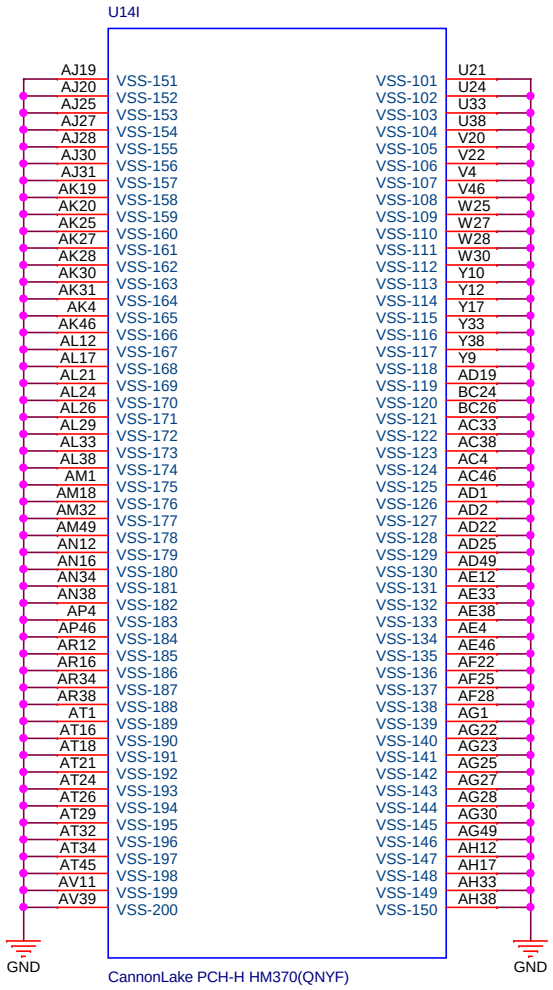
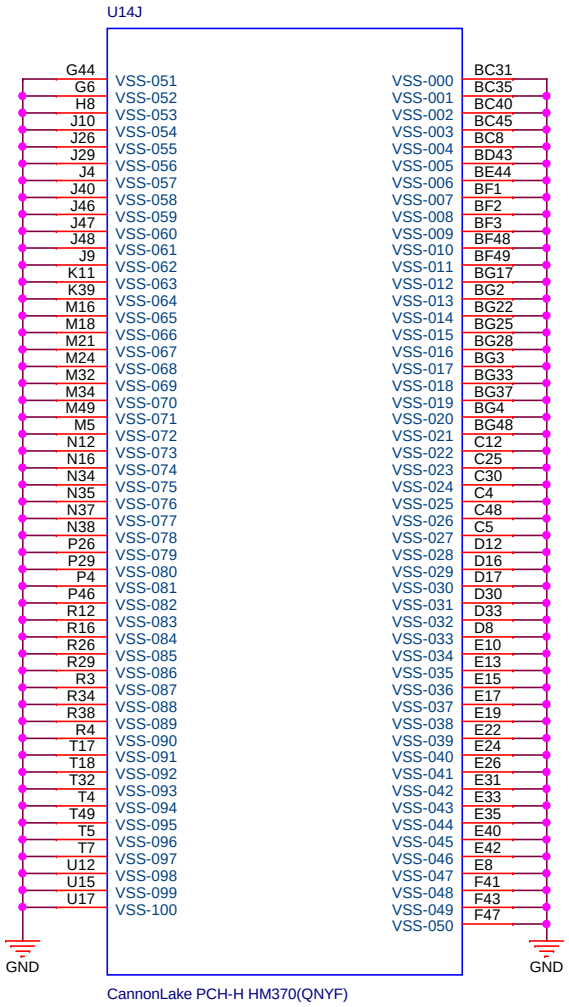
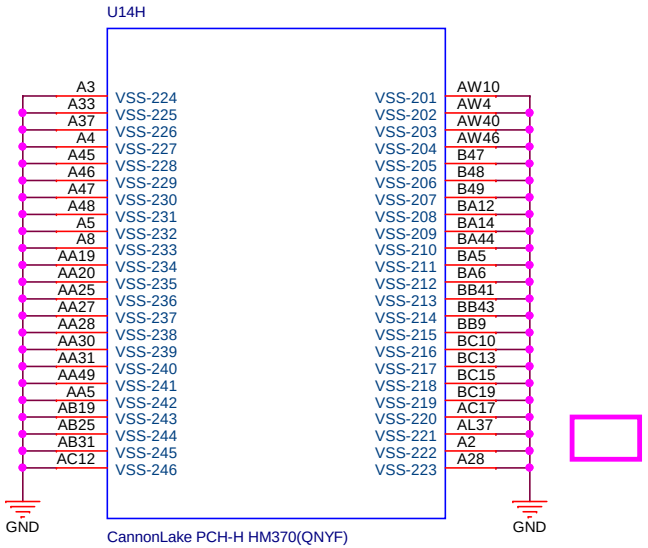
PCH-H(GND)







20170731 Add TP22 to follow CRB suggestion
20170911 Del TP22 to follow CRB 0.9

MICRO-STAR INT'L CO.,LTD.

Title	PCH-7(GND)	
Size: Custom	Document Number: MS-16K71	Rev: 10
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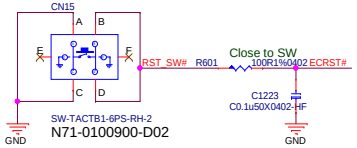
KBC/EC/uP (ENE9028)

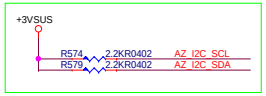
Hardware Reset

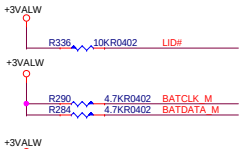


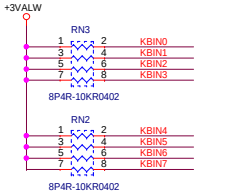
remove OVERT# (Active Low)

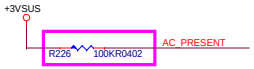
PU/PD

RSMRST# follow DG modify to 10K



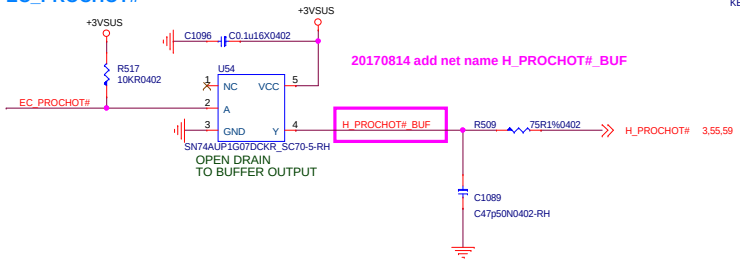






20170829 add R3528

EC_PROCHOT#



20170814 add net name H_PROCHOT#_BUF

U31

LPC I/F
SERIRQ
LFRAME#
PCICLK
CLKRUN#/GPIO1D
LAD0
LAD1
LAD2
LAD3

FAN&PWM
ECRST#
KBRST#/GPIO01
SCI#/GPIO0E
GA20/GPIO00
PCIRST#/GPIO05
PWM0/GPIO0F
PWM1/GPIO10
PWM2/GPIO11
PWM3/GPIO19
FANPWM0/GPIO12
FANPWM1/GPIO13
FANFB0/GPIO14
FANFB1/GPIO15

IKB
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25/UART_SOUT
KSO6/GPIO26
KSO7/GPIO27/SERIRQ(LPC_Bypass)/UART_RTS
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B/LAD3(LPC_Bypass)
KSO12/GPIO2C/LAD2(LPC_Bypass)/UART_DTR
KSO13/GPIO2D/LAD1(LPC_Bypass)
KSO14/GPIO2E/LAD0(LPC_Bypass)
KSO15/GPIO2F
KSO16/GPIO48/UART_SOUT2
KSO17/GPIO49
KSI0/GPIO30/E51TXD
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37/EDI_DO

ESB
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT_O

CIR
GPIO40/AD6
GPIO41/CIR_RLC_TX/AD7
GPIO0A/OWM
GPIO0D/RLC_TX2

SPI FLASH
MISO/GPIO5B
MOSI/GPIO5C
SPICLK/GPIO58
SPICS#/GPIO5A

PS2 I/F
PSCLK3/GPIO4E
PSDAT3/GPIO4F
PSCLK2/GPIO4C/SCL3
PSDAT2/GPIO4D/SDA3
PSCLK1/GPIO4A/SCL2/SMBD_CLK
PSDAT1/GPIO4B/SDA2/SMBD_DAT

UART
E51TXD/GPIO16
E51CLK/GPIO17

GPIO5D
GPIO5E

KB9028Q-C-RH

POWER/GROUND
VCC_LPC
VCC
VCC-1
VCC-2
VCC-3
VCC0
VCC_IO2
AVCC
AGND
GND
GND-1
GND-2
GND-3
GND-4

When use ENE9048 eSPI mode
PCH's VCCPGPPA must be 1.8V

R538 X_0R0402 +1_8VSUS
R537 0R0402 +3VALW
C1118 C0.1u16X0402
+3VALW
C317 C1111 C1112 C1113
C0.1u16X0402

SMBUS
SDA0/GPIO45
SCL0/GPIO44
IEDI_SDA/SDA1/GPIO47
IEDI_SCL/SCL1/GPIO46

SMB_GPU_DATA 25,43,54
SMB_GPU_CLK 25,43,54
EC_SDA 44
EC_SCL 44

AD/DA
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
AD4/GPI42
AD5/GPI43

MB_ID
CAMERA_ON 41
DGPU_PWRGD 30,32
WLAN_PWRON 53
KBIN0
KBIN1
KBIN2
KBIN3
KBIN4
KBIN5

SDI
GPXIOA00/GPIO60/SHICS#
GPXIOA01/GPIO61/SHICLK
GPXIOA02/GPIO62/SHIDO

EC_SPI_CS 52
EC_SPI_CLK 52
EC_SPI_DO 52

POWER_FAIL0/GPIO63/GPXIOA03
GPIO64/GPXIOA04
GPIO65/GPXIOA05
VCOUT1/GPIO66/GPXIOA06
VCOUT0/GPIO67/GPXIOA07
GPIO68/GPXIOA08
GPIO69/GPXIOA09
GPIO6A/GPXIOA10
GWG/GPIO6B/GPXIOA11
SDIDO/GPIO78/GPXIOD00
GPIO79/GPXIOD01
EC_EN#/GPIO7A/GPXIOD02
GPIO7B/GPXIOD03
GPIO7C/GPXIOD04
GPIO7D/GPXIOD05
GPIO7E/GPXIOD06
GPIO7F/PECI

SUS_ON 56
GPUFAN_FB2 45
ADP_ICC 55
EC_PROCHOT#

ALLSYSPG 3,32,35,59,62
LED_BLUETOOTH# 54
LED_CHARGE 54
LED_BATLOW 54
AC_PRESENT 32
EC_SPI_DI 52
AC_OK 55
GPU_ACIN 25,55
PWR_SW# 45
1V8_AON_EN 30,63
EC_ALLSYSPG 32
PECI_904BPWR
H_PECI_R

R222 43R0402 H_PECI 3
R273 X_10KR0402 +3VSUS

ALLSYSPG
20171220
add EC_ALLSYSPG for modify sequence

for ENE9048 ,GPIO7E
define PECI Power to VCCST

R532 0R0402 DGPU_LED 45

for ENE9048 ,GPIO04
KBSMI# PU 3.3V

GPIO04
i_clk_8051/GPIO07
PROCHOT#/i_clk_peri/GPIO08
POWER_FAIL1/GPIO18
GPIO50
GPIO52
WDT_LED#/GPIO54
GPIO56
XCLK32K/GPIO57
GPIO59

ECESPI_RST# R
KBSMI# 36
R605 0R0402 SUSPWRDNACK 36
R285 X_0R0402 ECESPI_RST# 36

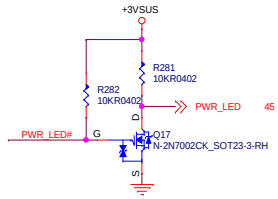
SCI_WAKE_UP# 34
EC_PCH_PWROK 32
WLAN_LED 54
USB_ENABLE 52,54
PWR_LED#

EC_PCH_PWROK
GPIO18 : ALLSYSPG delay 99ms
to generated EC_PCH_PWROK

RSMRST# 32
PM_SLP_S3# 3,7,32,42,57,59,62
PM_SLP_S4# 7,32,57

LED
GPIO1A/NUMLED#
GPIO53/CAPSLED#
GPIO55/SCROLED#

LED_NUM# 54
LED_CAP# 54
PM_SLP_M# 32



ENE9028 & 9048 Power Notes :

pin9 VCCLPC :
3.3V for ENE9028's LPC mode.
1.8V for ENE9048's eSPI mode.

pin111 VCC0 :
3.3V for ENE9028's PLC function
3.3V for ENE9048's eSPI operation with Pre-Driver.

N5A-26F0450-H06

CN14
FPC26P-B-1PITCH_NATURAL-RH-1

KBOUT17 26
KBOUT16 25
KBIN0 24
KBIN1 23
KBIN2 22
KBIN3 21
KBIN4 20
KBIN5 19
KBIN6 18
KBIN7 17
KBOUT15 16
KBOUT14 15
KBOUT13 14
KBOUT12 13
KBOUT11 12
KBOUT10 11
KBOUT9 10
KBOUT8 9
KBOUT7 8
KBOUT6 7
KBOUT5 6
KBOUT4 5
KBOUT3 4
KBOUT2 3
KBOUT1 2
KBOUT0 1

27
28

For EMI

EC45
KBOUT7 1 2
KBOUT6 3 4
KBOUT5 5 6
KBOUT4 7 8
8p4C-100p50N0402-RH

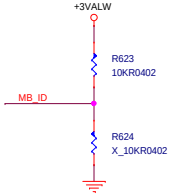
EC44
KBOUT3 1 2
KBOUT2 3 4
KBOUT1 5 6
KBOUT0 7 8
8p4C-100p50N0402-RH

EC46
KBOUT11 1 2
KBOUT10 3 4
KBOUT9 5 6
KBOUT8 7 8
8p4C-100p50N0402-RH

EC47
KBOUT15 1 2
KBOUT14 3 4
KBOUT13 5 6
KBOUT12 7 8
8p4C-100p50N0402-RH

KBOUT16 PC146 C100p16X0402
KBOUT17 PC147 C100p16X0402

Remove MB_ID

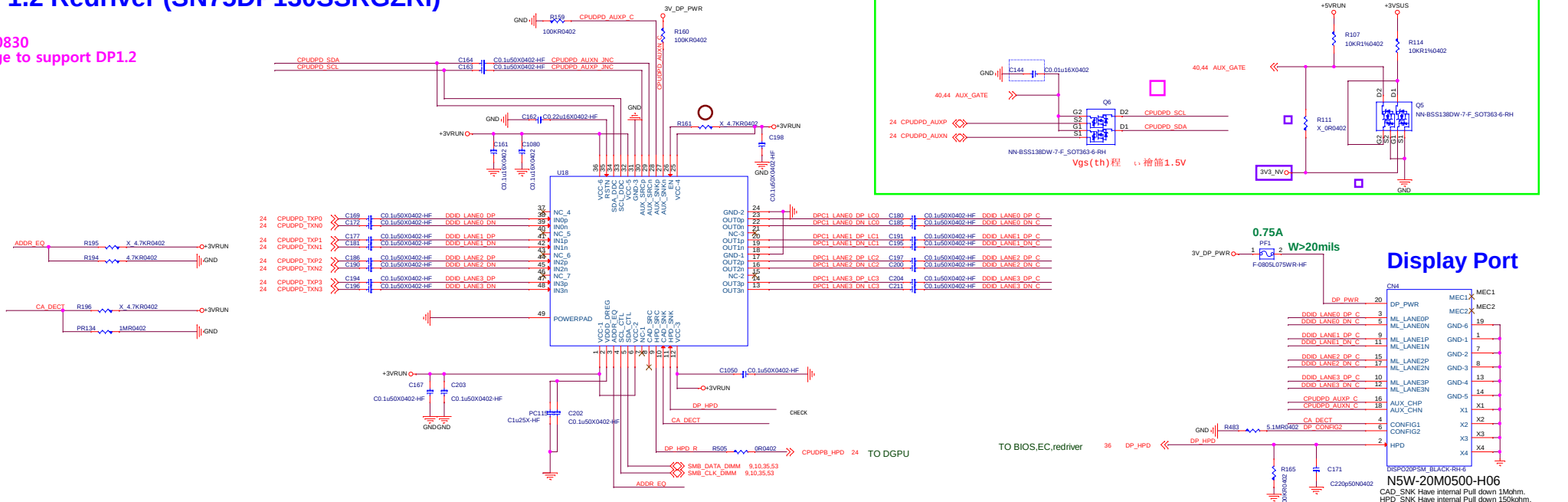


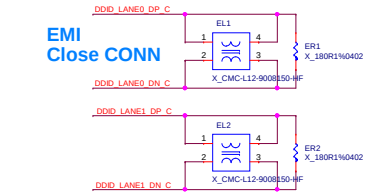
MB_ID	GS	WS
1	per key	White Color
0	3 Area	NA

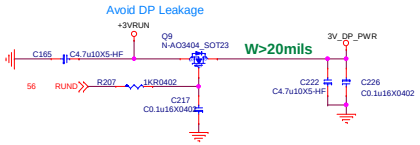
msi	MICRO-STAR INT'L CO.,LTD.	
Title	KBC/EC/uP (ENE9028)	
Size: Custom	Document Number: MS-16K71	Rev: 10
Date: Thursday, January 18, 2018	Sheet 39 of 80	

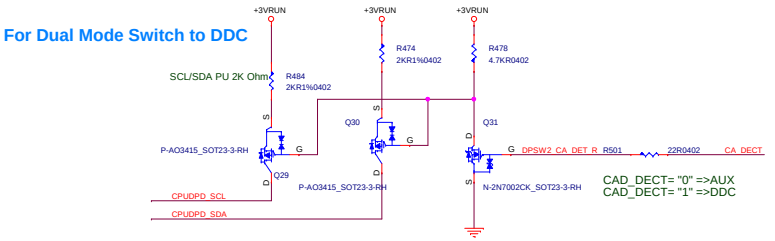
DP 1.2 Redriver (SN75DP130SSRGZRI)

20170830
change to support DP1.2







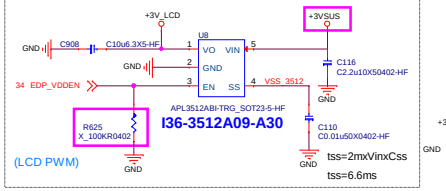


MICRO-STAR INT'L CO.,LTD.

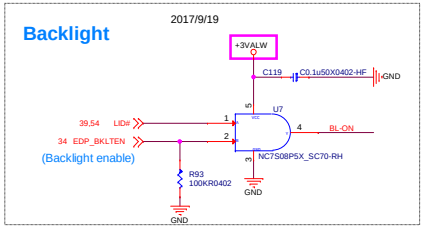
Title	DP 1.2 (SN75DP130SSRGZR)	
Size: Custom	Document Number: MS-16K71	Rev: 10
Date: Thursday, January 18, 2018	Sheet 40 of 80	

Pannel Device Logic Power

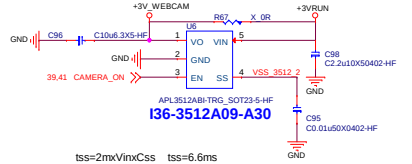
20171220
change input to +3VSUS for panel sequence
reserve R625 for Panel power off
blinking issue



Backlight



CAMERA Power

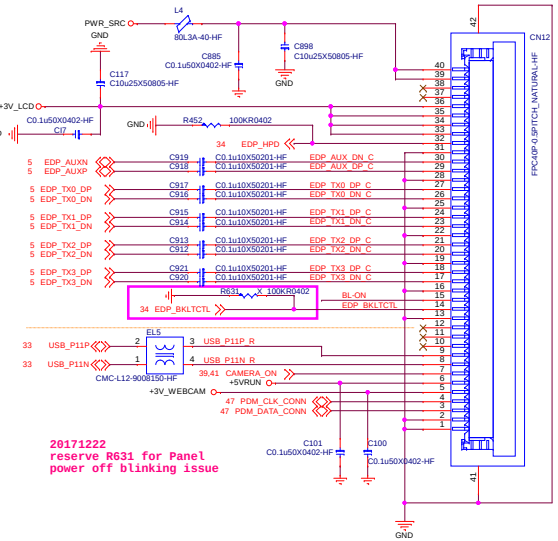


eDP Connector

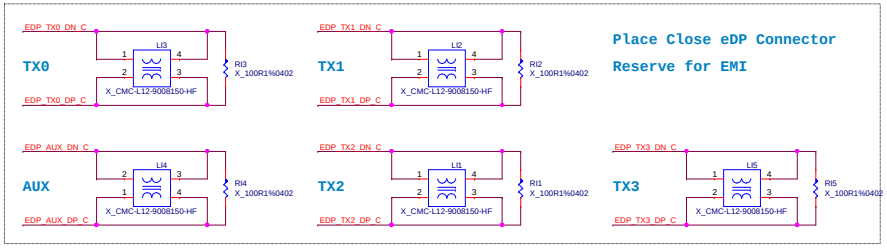
N5A-40F0180-A81

eDP CONN

20171222
reserve R631 for Panel
power off blinking issue



Place Close eDP Connector
Reserve for EMI



LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufactureer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer˜s use
35	NC	Reserved for LCD manufacturer˜s use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

LCD Module Pin Define FOR QHD+ PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer˜s use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	NC	Reserved for LCD manufacturer˜s use
19	NC	Reserved for LCD manufacturer˜s use
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	VDD	LCD logic and driver power(3.3V)
23	VDD	LCD logic and driver power(3.3V)
24	VDD	LCD logic and driver power(3.3V)
25	NC	Reserved for LCD manufacturer˜s use
26	LCD_GND	LCD logic and driver ground
27	LCD_GND	LCD logic and driver ground
28	LCD_GND	LCD logic and driver ground
29	LCD_GND	LCD logic and driver ground
30	LCD_GND	LCD logic and driver ground
31	HPD	Backlight ground
32	NC	Reserved for LCD manufacturer˜s use
33	PWM_OUT	PWM_OUT
34	PWM_IN	PWM_IN
35	NC	Reserved for LCD manufacturer˜s use
36	NC	Reserved for LCD manufacturer˜s use
37	NC	Reserved for LCD manufacturer˜s use
38	VBL	LED Anode
39	VBL	LED Anode
40	NC	Reserved for LCD manufacturer˜s use
41	LED_C1	LED Cathode 1
42	LED_C2	LED Cathode 2
43	LED_C3	LED Cathode 3
44	LED_C4	LED Cathode 4
45	LED_C5	LED Cathode 5
46	LED_C6	LED Cathode 6
47	LED_C7	LED Cathode 7
48	LED_C8	LED Cathode 8
49	NC	Reserved for LCD manufacturer˜s use
50	NC	Reserved for LCD manufacturer˜s use

MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector/Camera

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Thunderbolt

20170830
modify for AR b-step, c-step chip and wake function

DDI C
DP++

CIO1

CIO0

B07-L634015-I06

20170830
reserve U3053 and C8999

20170830
R228,R232 change to 2.2K to follow CRB

20170830
R262 change to unstuff

20170919
R461 change to connect with TBT_CLKREQ#_R

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100K PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

MICRO-STAR INT'L CO.,LTD.

Title: Alpine Ridge(TBT)

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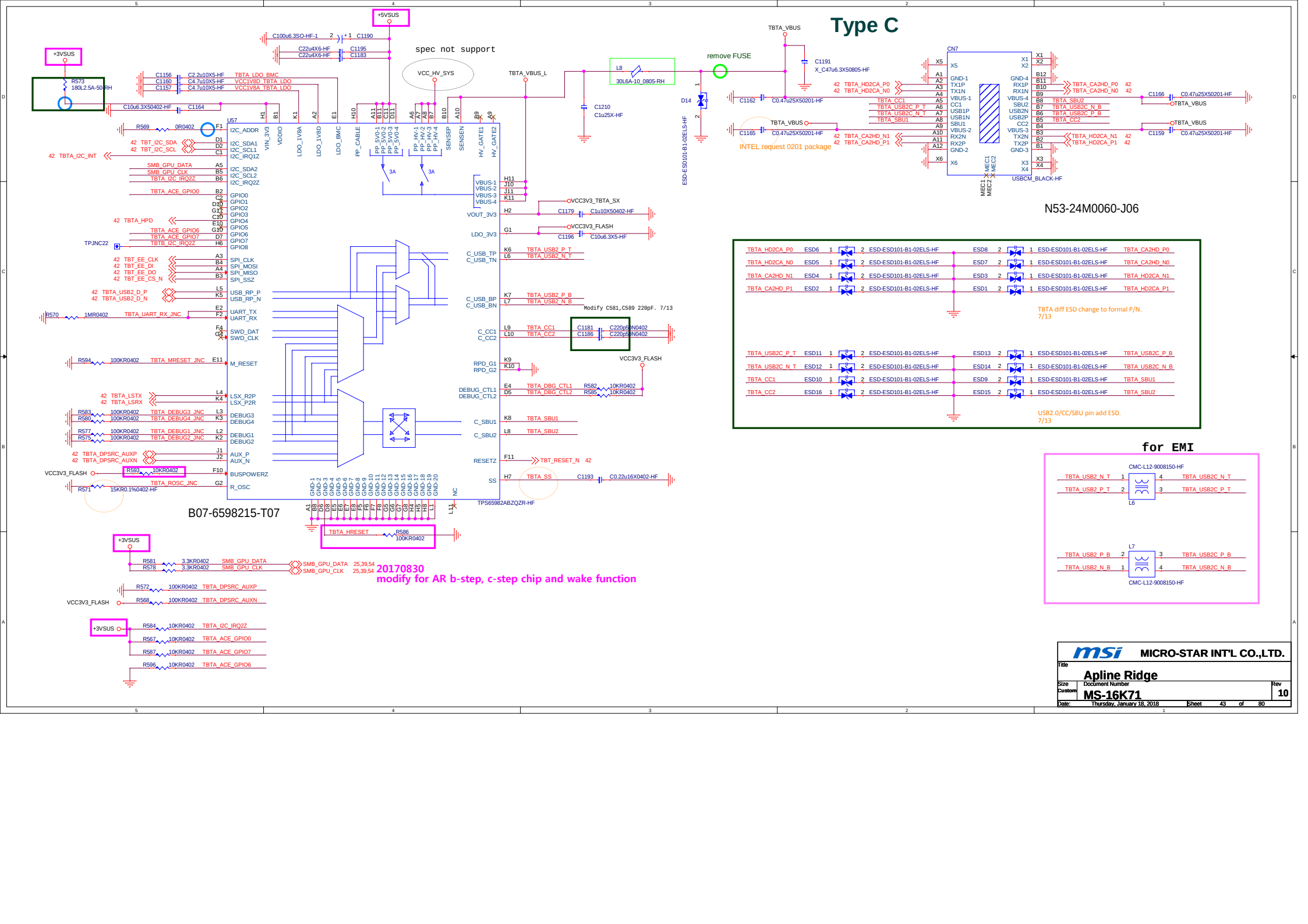
Type C
spec not support
remove FUSE
INTEL request 0201 package
N53-24M0060-J06
B07-6598215-T07
TPS65982ABZQZR-HF
USBCM_BLACK-HF
ESD-ESD101-B1-02ELS-HF
TBTA diff ESD change to formal P/N.
7/13
USB2.0/CC/SBU pin add ESD.
7/13
for EMI
CMC-L12-9008150-HF
Modify C581,C589 220pF. 7/13
20170830
modify for AR b-step, c-step chip and wake function
MICRO-STAR INT'L CO.,LTD.
Apline Ridge
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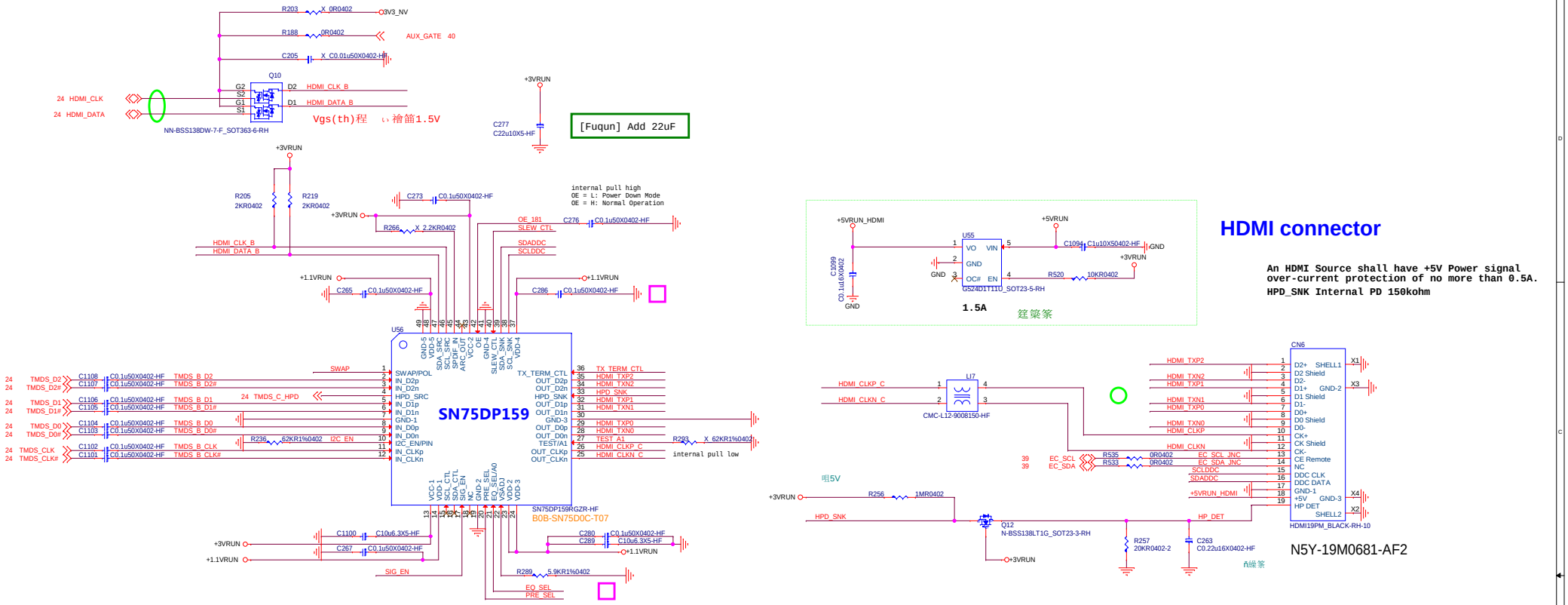

Title	HDMI
Size	C
Document Number	MS-16K71
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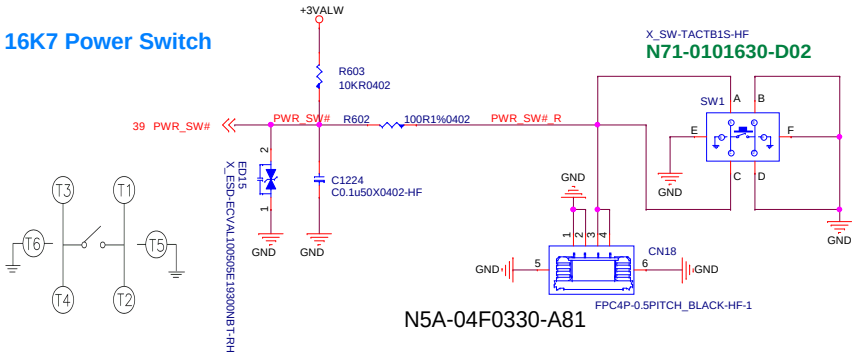
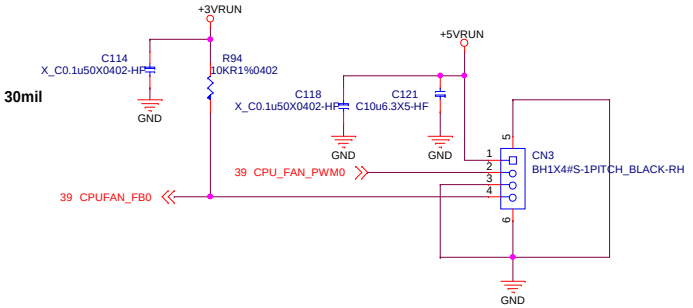
MICRO-STAR INT'L CO.,LTD.

PWR SW/CPU FAN/BTB CONN/ LED CONN

16K7 Power Switch

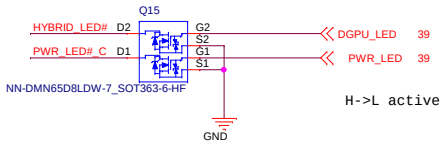


CPU FAN

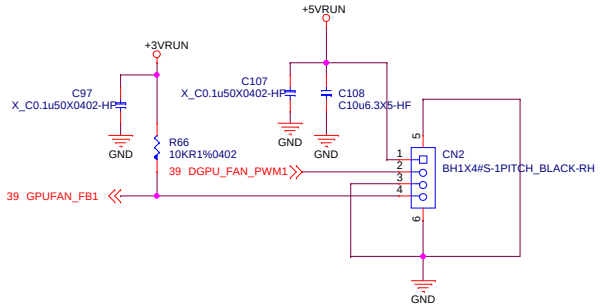


Control PWR LED

DGPU_LED	PWR_LED	LED COLOR
L	H	RED
H	H	ORANGE
H	L	GREEN
L	L	X

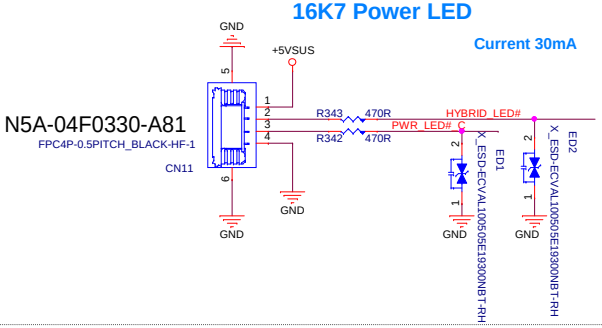


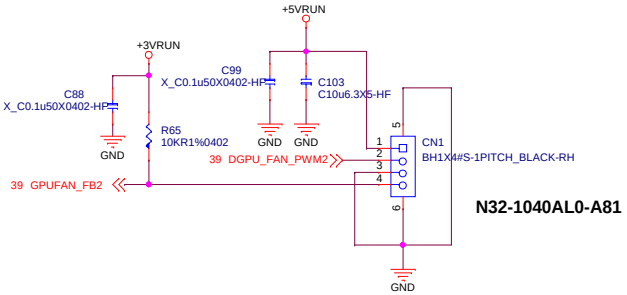
DGPU FAN



16K7 Power LED

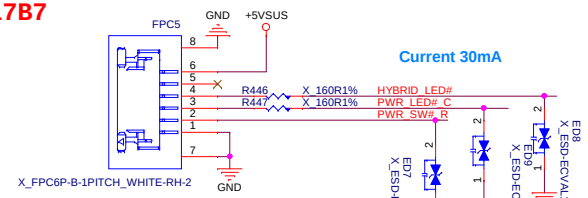
Current 30mA





Power LED+SW For 17B7

Current 30mA



remove 16K2's LED_ACPI#_BR and APCI_BR Circuit

MSI MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/BTB CONN/LED

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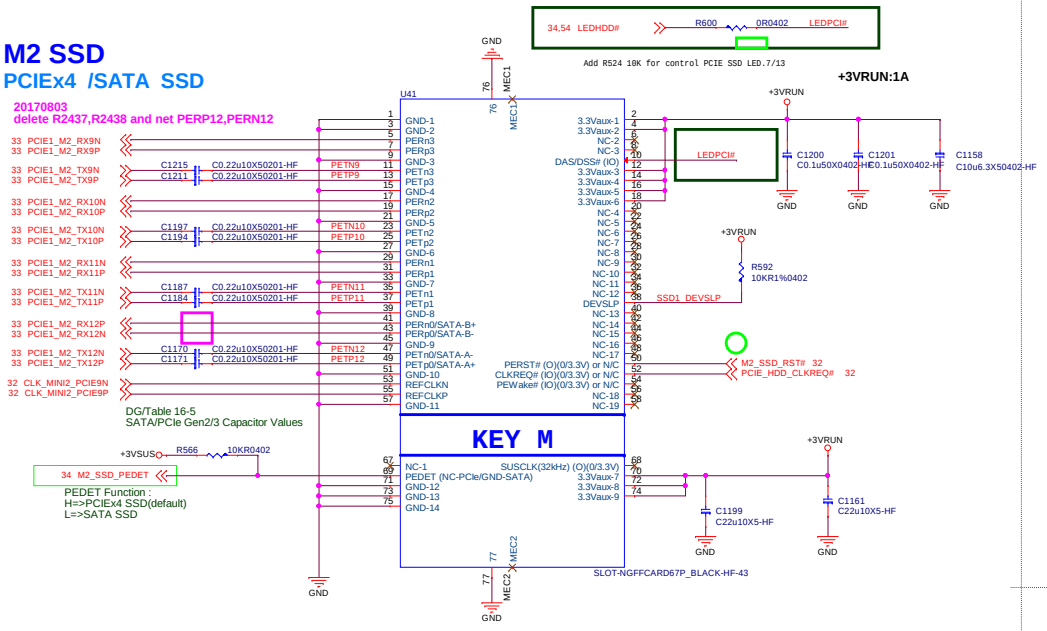
M2 SSD

PCIEx4 /SATA SSD

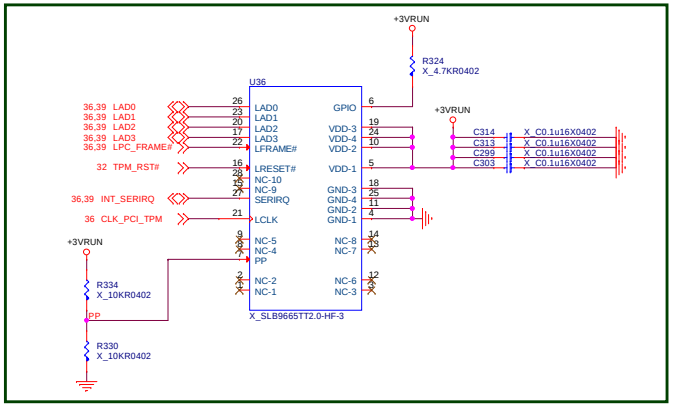


N15-0670530-L41

40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

TPM

FOR WS



Physical Presence(PP)
The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled .

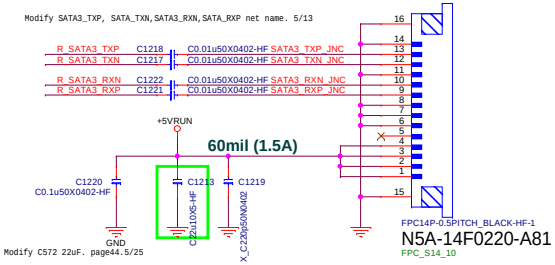
DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (***default***)	–4	NC (***default***)	0
0	0	0	7
1	–2	1	14

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (***default***)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

TI SN75LVCP601RTJR HW Setting

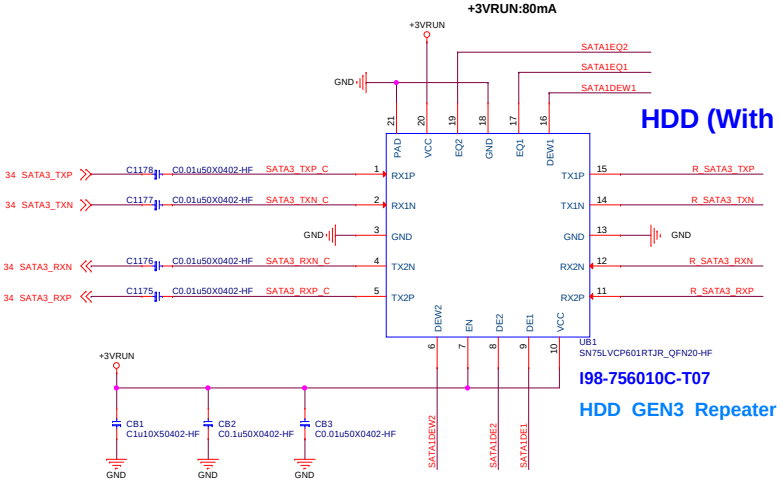
20171227
delete TPJNC24 and TPJNC25
add R632 and R633 for SA

HDD2



(Must used the gold fresh type)

+3VRUN:80mA



HDD (With Repeater)

I98-756010C-T07

HDD GEN3 Repeater

Title	M2 SSD/HDD/TPM
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MICRO-STAR INT'L CO.,LTD.

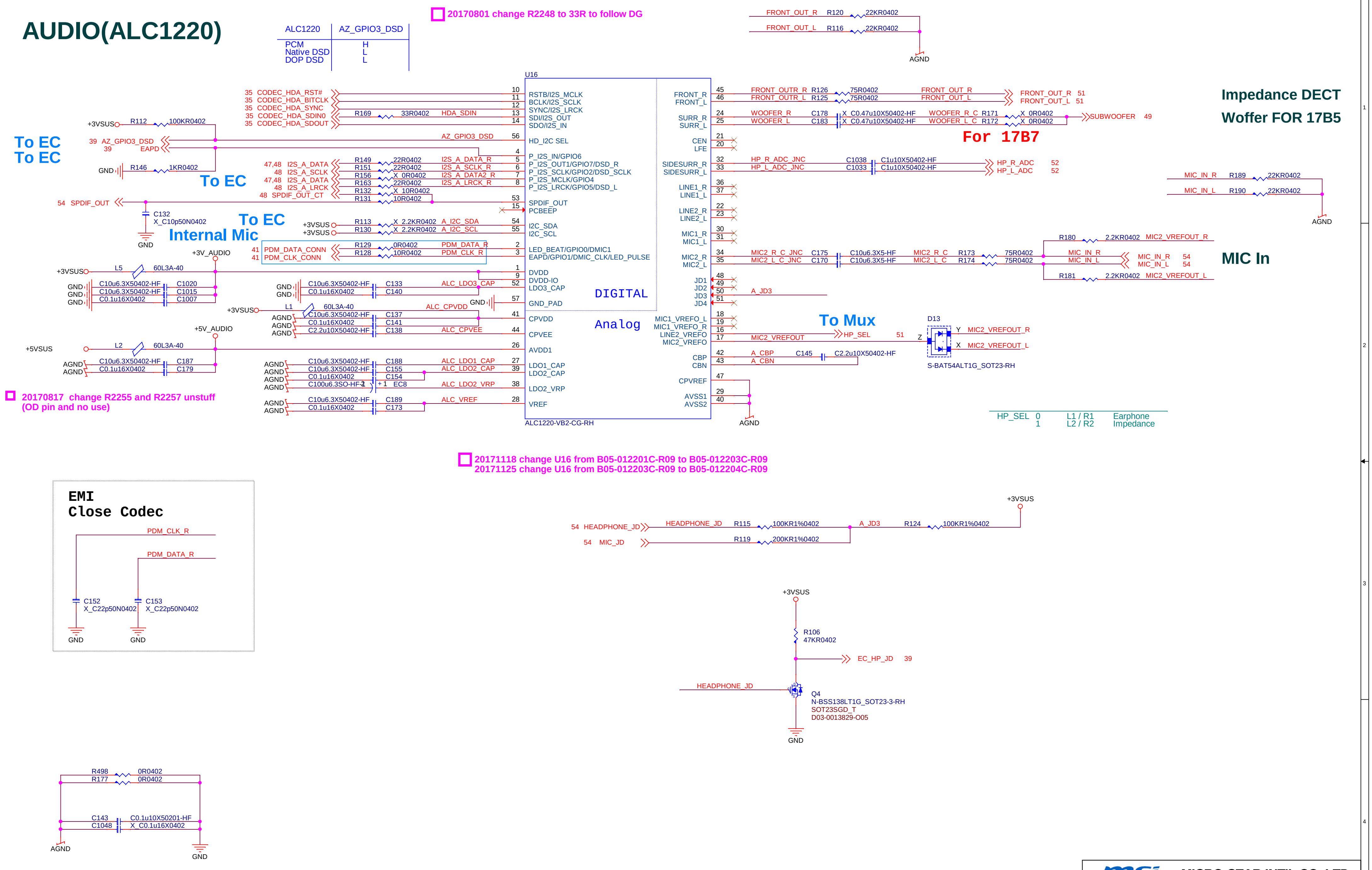
AUDIO(ALC1220)

ALC1220	AZ_GPIO3_DSD
PCM	H
Native DSD	L
DOP DSD	L

20170801 change R2248 to 33R to follow DG

20170817 change R2255 and R2257 unstuff (OD pin and no use)

20171118 change U16 from B05-012201C-R09 to B05-012203C-R09
20171125 change U16 from B05-012203C-R09 to B05-012204C-R09



U16
ALC1220-VB2-CG-RH
RSTB/I2S_MCLK
BCLK/I2S_SCLK
SYNC/I2S_LRCK
SDI/I2S_OUT
SDO/I2S_IN
HD_I2C SEL
P_I2S_IN/GPIO6
P_I2S_OUT1/GPIO7/DSD_R
P_I2S_SCLK/GPIO2/DSD_SCLK
P_I2S_MCLK/GPIO4
P_I2S_LRCK/GPIO5/DSD_L
SPDIF_OUT
PCBEEP
I2C_SDA
I2C_SCL
LED_BEAT/GPIO0/DMIC1
EAPD/GPIO1/DMIC_CLK/LED_PULSE
DVDD
DVDD-IO
LDO3_CAP
GND_PAD
CPVDD
CPVEE
AVDD1
LDO1_CAP
LDO2_CAP
LDO2_VRP
VREF
DIGITAL
Analog
FRONT_R
FRONT_L
SURR_R
SURR_L
CEN
LFE
SIDESURR_R
SIDESURR_L
LINE1_R
LINE1_L
LINE2_R
LINE2_L
MIC1_R
MIC1_L
MIC2_R
MIC2_L
JD1
JD2
JD3
JD4
MIC1_VREFO_L
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
CBP
CBN
CPVREF
AVSS1
AVSS2
To EC
To EC
To EC
To EC
Internal Mic
35 CODEC_HDA_RST#
35 CODEC_HDA_BITCLK
35 CODEC_HDA_SYNC
35 CODEC_HDA_SDIN0
35 CODEC_HDA_SDOUT
39 AZ_GPIO3_DSD
39 EAPD
47,48 I2S_A_DATA
48 I2S_A_SCLK
47,48 I2S_A_DATA
48 I2S_A_LRCK
48 SPDIF_OUT_CT
54 SPDIF_OUT
41 PDM_DATA_CONN
41 PDM_CLK_CONN
FRONT_OUT_R R120 22KR0402
FRONT_OUT_L R116 22KR0402
FRONT_OUT_R 51
FRONT_OUT_L 51
SUBWOOFER 49
HP_R_ADC 52
HP_L_ADC 52
Impedance DECT
Woffer FOR 17B5
For 17B7
MIC In
MIC_IN_R 54
MIC_IN_L 54
To Mux
HP_SEL 51
D13
S-BAT54ALT1G_SOT23-RH
MIC2_VREFOUT_R
MIC2_VREFOUT_L
HP_SEL 0 L1 / R1 Earphone
1 L2 / R2 Impedance
EMI
Close Codec
PDM_CLK_R
PDM_DATA_R
C152 X_C22p50N0402
C153 X_C22p50N0402
54 HEADPHONE_JD
54 MIC_JD
R115 100KR1%0402
R124 100KR1%0402
R119 200KR1%0402
A_JD3
R106 47KR0402
EC_HP_JD 39
Q4
N-BSS138LT1G_SOT23-3-RH
SOT23SGD_T
D03-0013829-O05
R498 0R0402
R177 0R0402
C143 C0.1u10X50201-HF
C1048 X_C0.1u16X0402
AGND
GND

msi MICRO-STAR INT'L CO.,LTD.

Title	Audio(ALC1220)
Size	Custom
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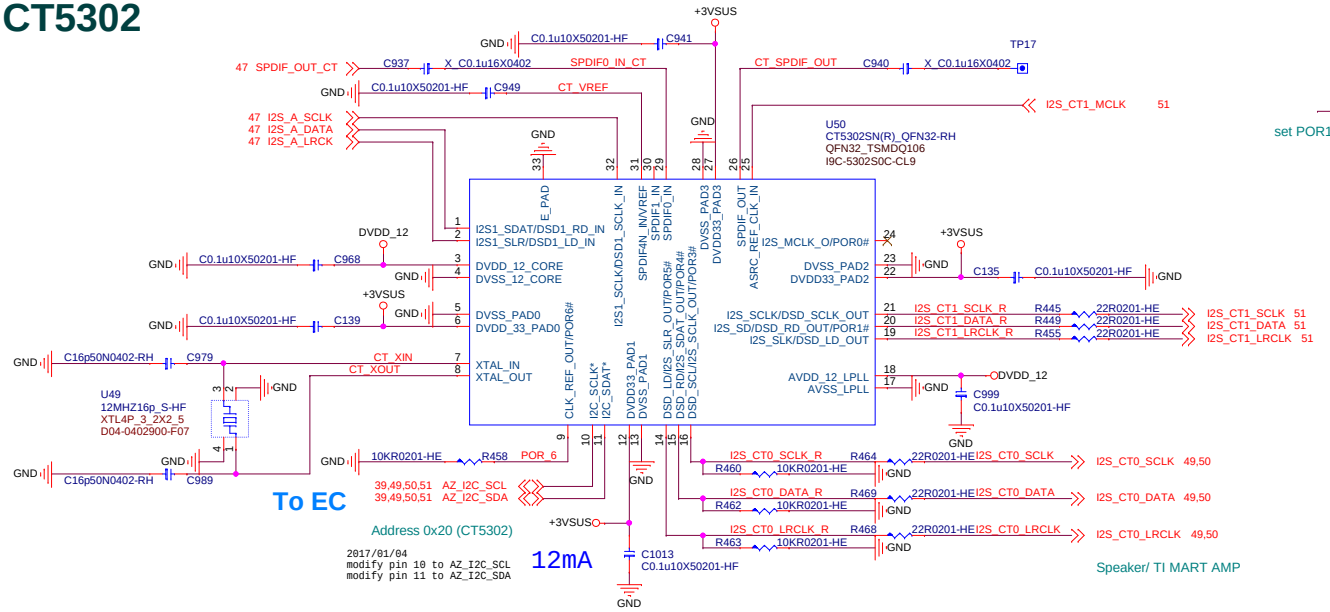
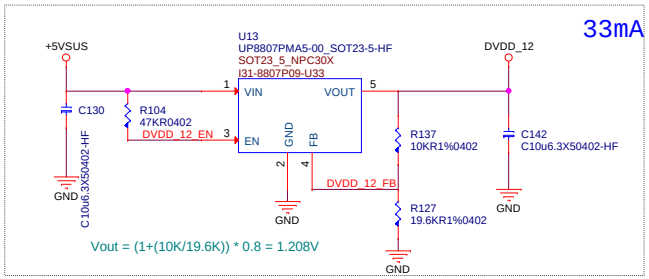
CT5302





HW SETTING

I2S output slave mode:

Select I2S1 output port

No.	POR1	Definition
0	0	I2S output master mode
1	1	I2S output slave mode

HW SETTING

Hardware Crystal:

Select current external crystal frequency

No	POR4	POR3	Definition
0	0	0	12.0000MHz
1	0	1	11.2896MHz
2	1	0	12.2880MHz
3	1	1	14.3180MHz

HW SETTING

I2C Slave ID

Define chip I2C slave address

No	POR6	POR5	Definition
0	0	0	0x20
1	0	1	0x22
2	1	0	0x24
3	1	1	0x26

Pin Name	Description	Function Table
POR_IN_1	POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE	Select I2S1 output port is master or slave mode
POR_IN_3	POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0]	Select Crystal frequency
POR_IN_4		
POR_IN_5	POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0]	I2C serial interface device ID selection
POR_IN_6		

MICRO-STAR INT'L CO.,LTD.

Title: CT5302

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20180110
change smart Amp connect with PWR_SRC

SMART AMP LEFT

WIDTH > 40 mils

1.5A

PVCC=5V Vpp=5*2=10. Vrms=10/2.828=3.53
(RL=4 ohm) Po max =(Vrms) ^2/RL=(3.53)^2/4= 3.1W
I max=0.62 A

PVCC=19V Vpp=19*2=38. Vrms=38/2.828=13.43
(RL=4 ohm) Po max =(Vrms) ^2/RL=(13.43)^2/4= 45W
I max=2.3 A

To EC

2017/01/04
modify pin 36 to AZ_I2C_SCL
modify pin 35 to AZ_I2C_SDA

Address 0x98 (SPEAKER)

14dB/353-384KHz

TAS5766MRMTR_VQFN48-HF
VQFN48_T142X220
I71-5766M0C-T07

AMP WOOFER

SPK L2 / Woffer FOR 17B7

YG Normal:3W,Max:3.5W 4ohm
10DB / 2W

20171222
reserve R630

20180110
R252 change to 61.6K for woofer gain modification(too big)

H :Shutdown >2.2V
L: Active <0.4V

X_APA3010XA-TRL_MSOP8-LF
I71-0301002-A30

F(Low-pass) = 1/ 2 RC=1/(2 *3.3n*39K)=1.237k Hz

Left SPK+Woofer Conn

BH1X6#S-1.25PITCH_BLACK-RH
N32-1060720-A81

From EC

To WOOFER AMP

To SPEAK AMP

NN-DMN65D8LDW-7_SOT363-6-HF

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Title	SMART AMP L & WOOFER
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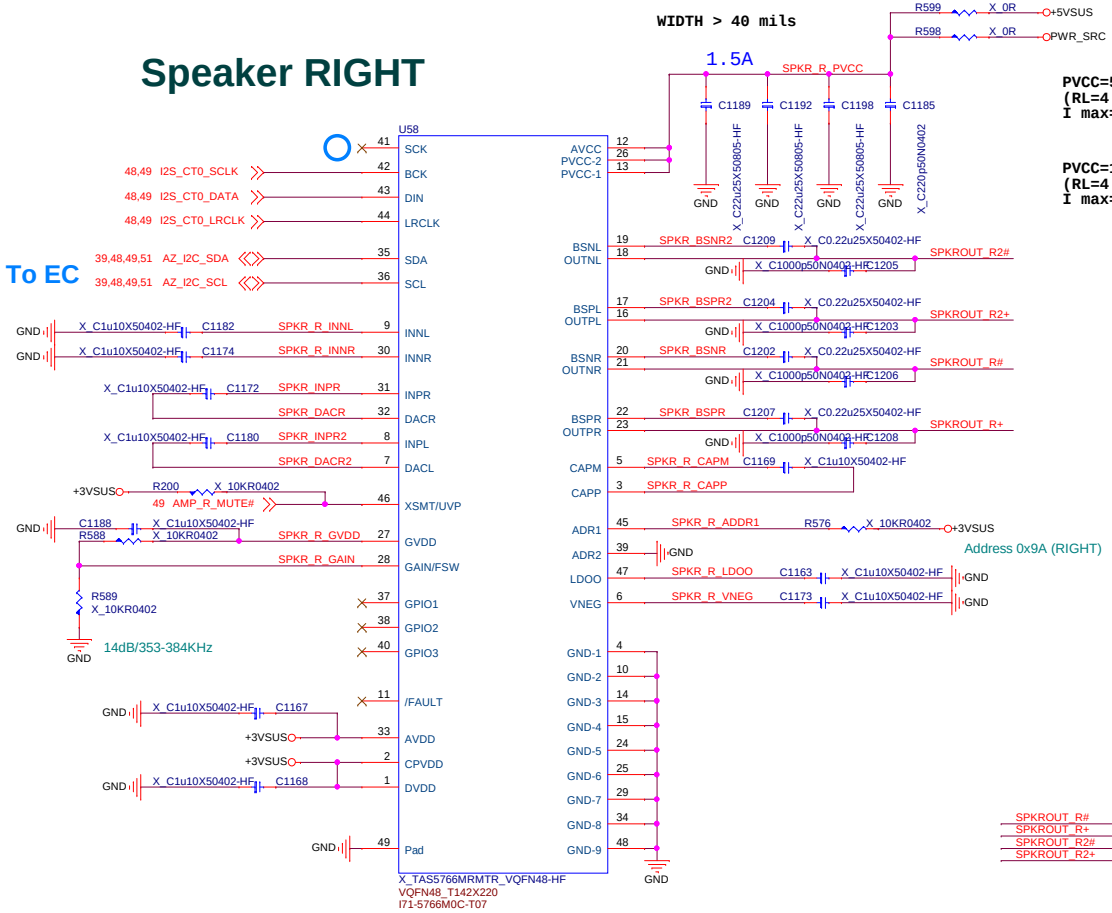
20180110
change smart Amp connect with PWR_SRC

Speaker RIGHT

WIDTH > 40 mils

1.5A



To EC

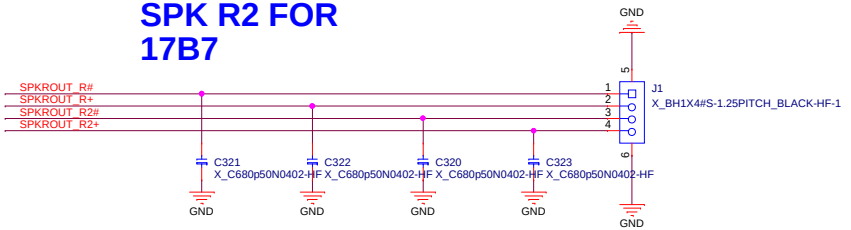
PVCC=5V Vpp=5*2=10. Vrms=10/2.828=3.53
(RL=4 ohm) Po max =(Vrms) ^2/RL=(3.53)^2/4= 3.1W
I max=0.62 A

PVCC=19V Vpp=19*2=38. Vrms=38/2.828=13.43
(RL=4 ohm) Po max =(Vrms) ^2/RL=(13.43)^2/4= 45W
I max=2.3 A

Address 0x9A (RIGHT)

Right SPK Conn

SPK R2 FOR 17B7



MICRO-STAR INT'L CO.,LTD.

Title: SMART AMP R

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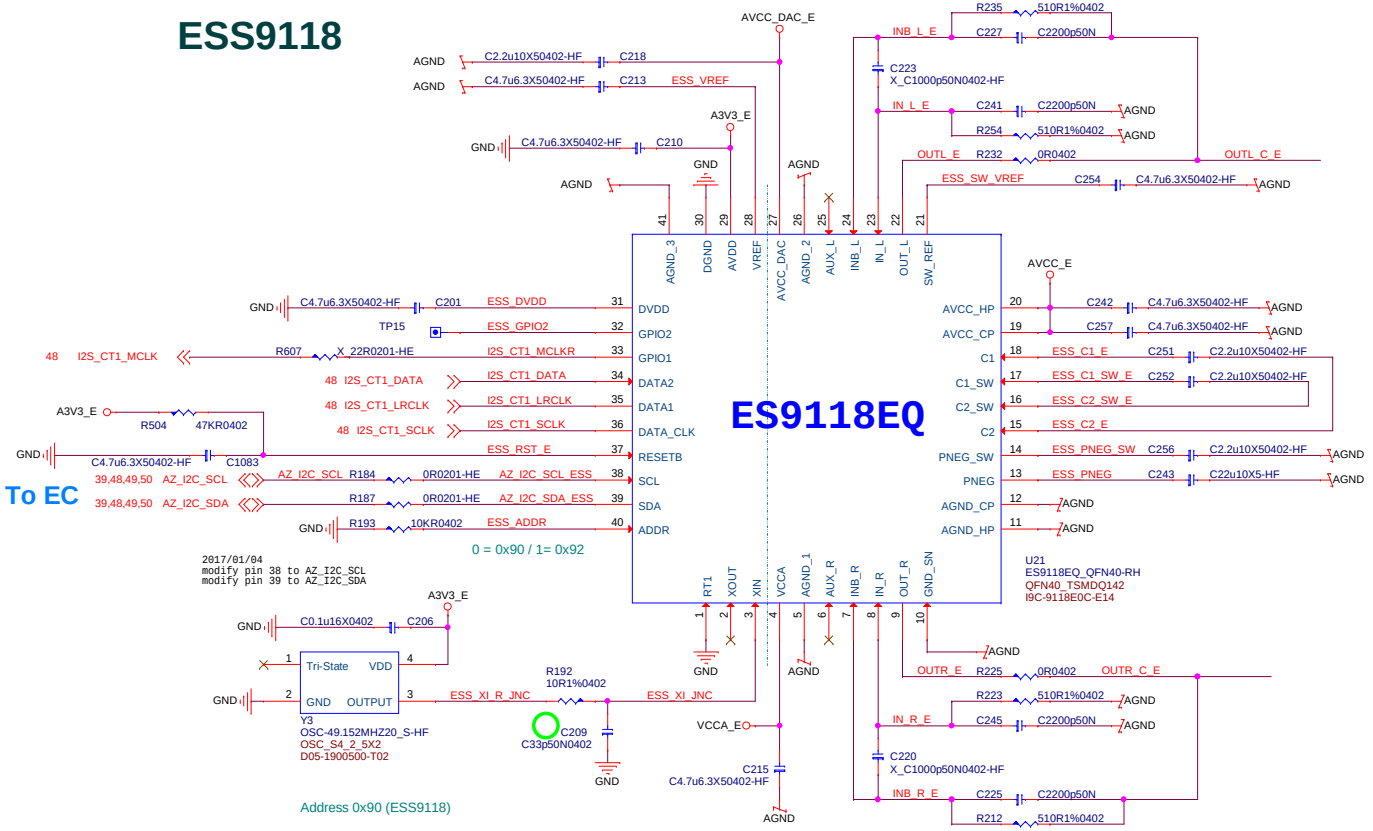
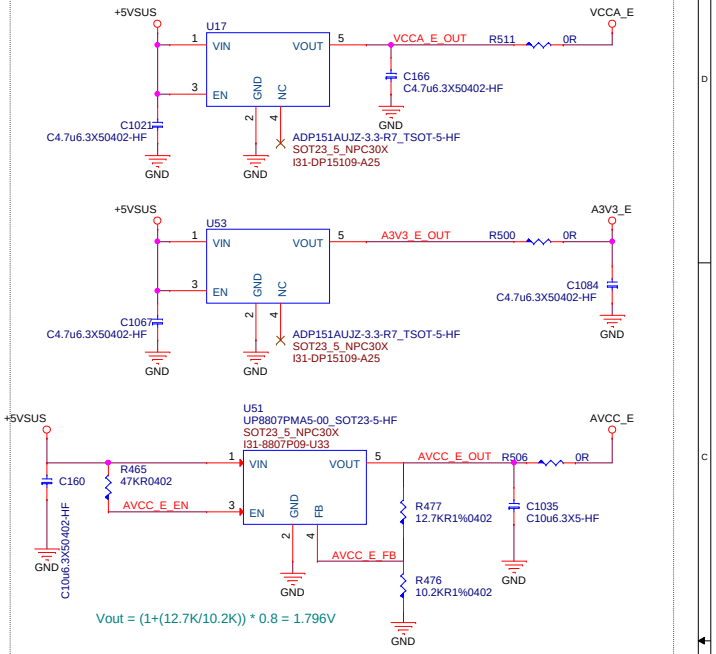
ESS9118



Power



Truth Table

INPUTS				OUTPUTS				
AC/DC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L,R) C/P Shunts	L1, R1 C/P Shunts	L2, R2 C/P Shunts
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic "0" ≤ 0.5V, Logic "1" ≥ 1.4V or Float with a 3.3V Supply or 5V supply.
SEL: Logic "0" ≤0.5V, Logic "1" ≥ 1.4V with a 3.3V Supply or 5V supply.
X = Don't Care

Audio MUX

SEL 0 L1 / R1 Earphone
1 L2 / R2 Impedance

20180110
R239 change to 10K for HP_SEL HIGH LEVEL low voltage
R626,R627 change to 20R for Headphone pop noise
when system turn off and decrease cross-talk

H: MUTE
L :ACTIVE

20171220
add R626,R627, net OUTL_R_E and OUTR_R_E
reserve R628

HP JACK

FROM REALTEK

ESS OUT

ALC1220 IN

U22
ISL54405IRUZ-T_UTQFN16-RH
TQFN16
I94-544050C-I11

Title	ESS Audio (ES9118EQ)
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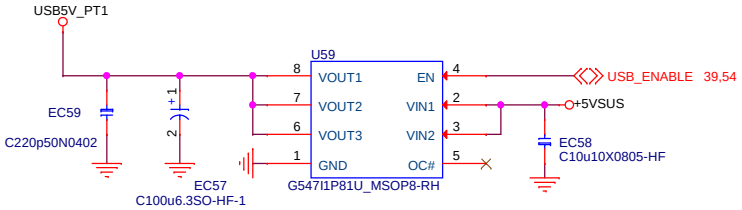
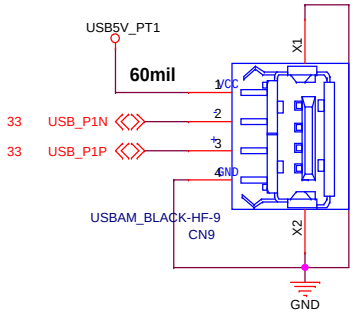
MICRO-STAR INT'L CO.,LTD.

USB2.0 CONN



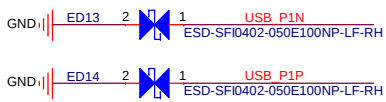
I36-5478102-G07

G5478I1 MAX :2.5A

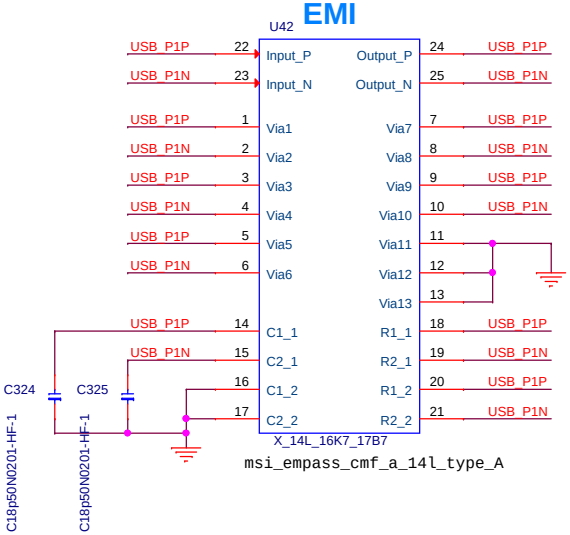


N53-04M1331-AF2

ESD



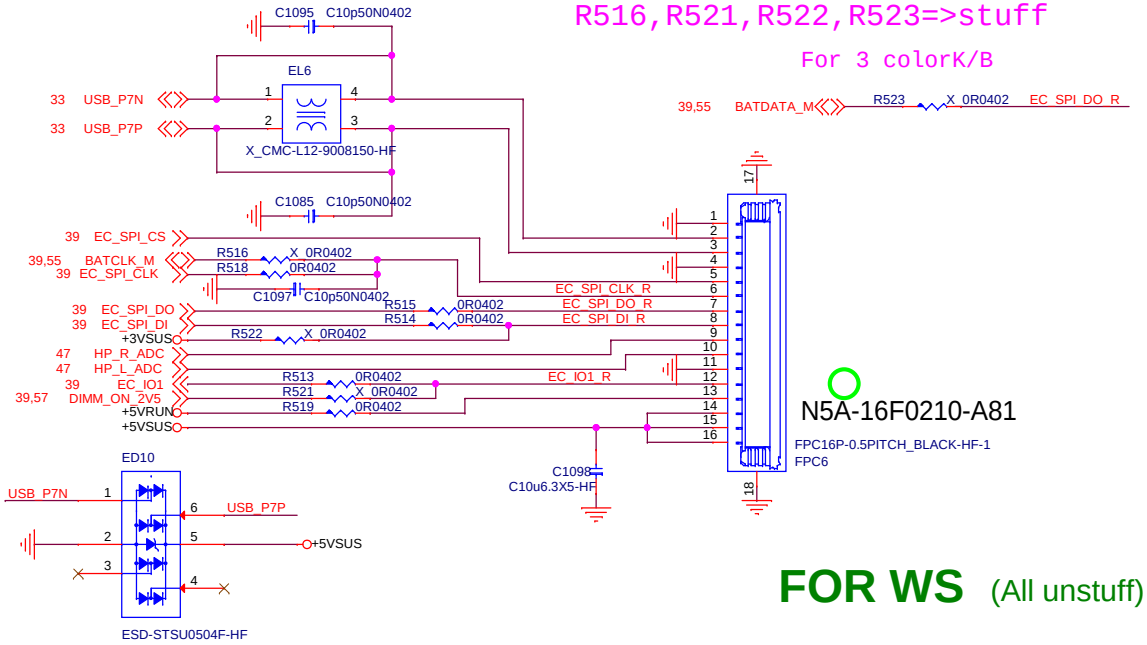
EMI



RGB Color Keyboard Control

For 3 colorK/B
R513,R514,R515,R518,R519=>unstuff
C1097=>unstuff
R516,R521,R522,R523=>stuff

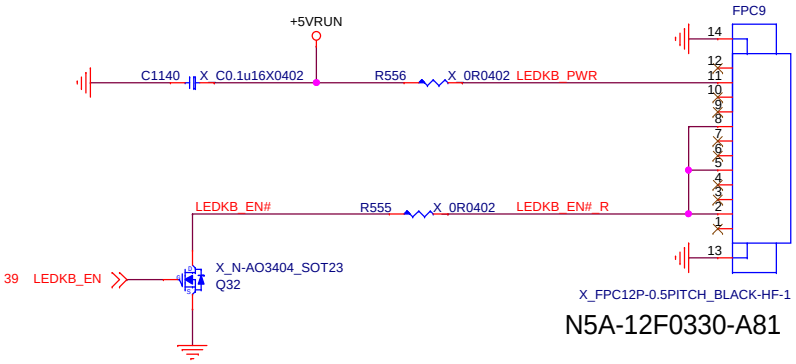
For 3 colorK/B



FOR WS (All unstuff)

White Color Keyboard Control

FOR WS (All stuff)



N5A-12F0330-A81

MICRO-STAR INT'L CO.,LTD.

Title: **USB2.0/Keyboard Control**

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WLAN /ClickPad/FP

EMI

Ref DG Section 18.6
- use USB 2.0 Port 14 wirh CNVi Solution

N15-0670520-L41
SLOT_NGFFCARD67_H2_15

PN : T70-7SZ0870-O05
AND Gate/ NL17SZ08DFT2G

	VIH Min	VIL Max
1.65 to 1.95	0.75*VCC	0.25*VCC
2.3 to 5.5	0.7*VCC	0.3*VCC

20170817 change R2394 stuff and R2397 unstuff for strap pin setting

Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

GPP_J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

FOR WS

2016012 Add U34,R88,R39,R40,R157,C208,C225 for +3VRUN_WLAN switch

FOR WS

20170902 Add Q19,R161,R705 for isolated WLAN_CLKREQ#

Finger Print

FOR WS

(All stuff)

Click Pad

Same Side

FPC6P-B-1PITCH_WHITE-RH-2
N5A-06F0310-A81

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Title	WLAN /ClickPad/FP
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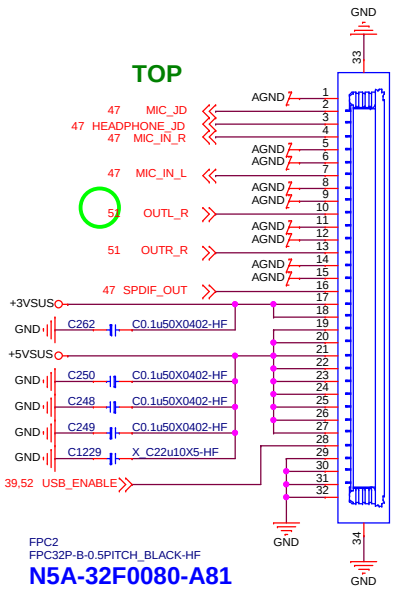
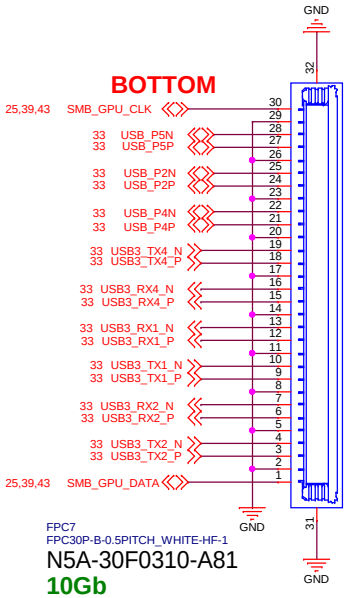
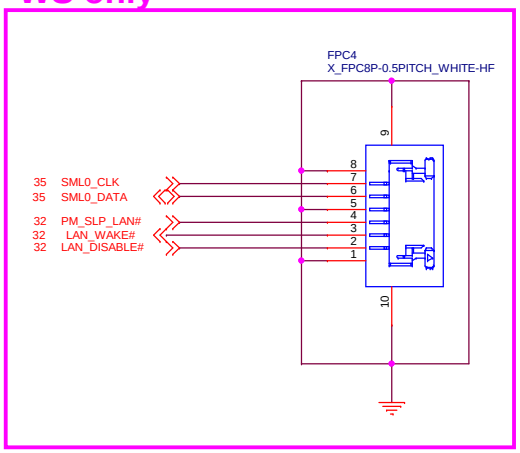
16K7/17B7 BTB CONN

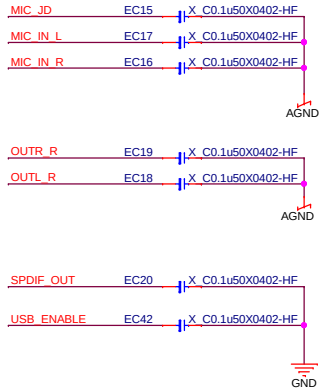
(Audio CONN/USB3.0)

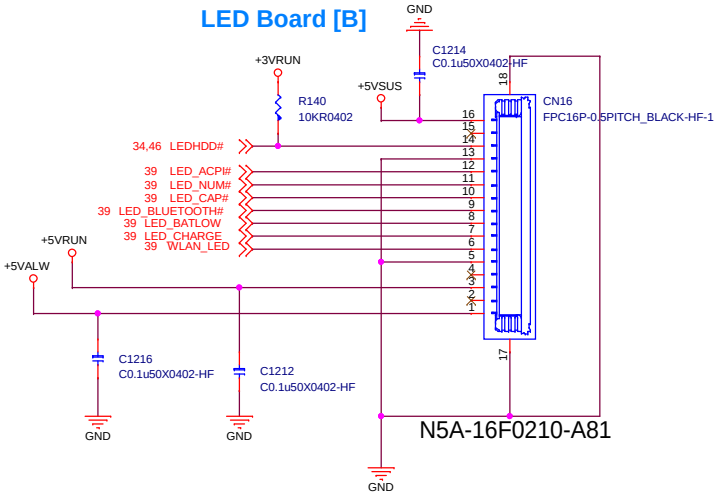
20171220
change FPC2 to 32pin and modify FPC7 pin define for new design
(Audio issue and USB3.1 solution change)

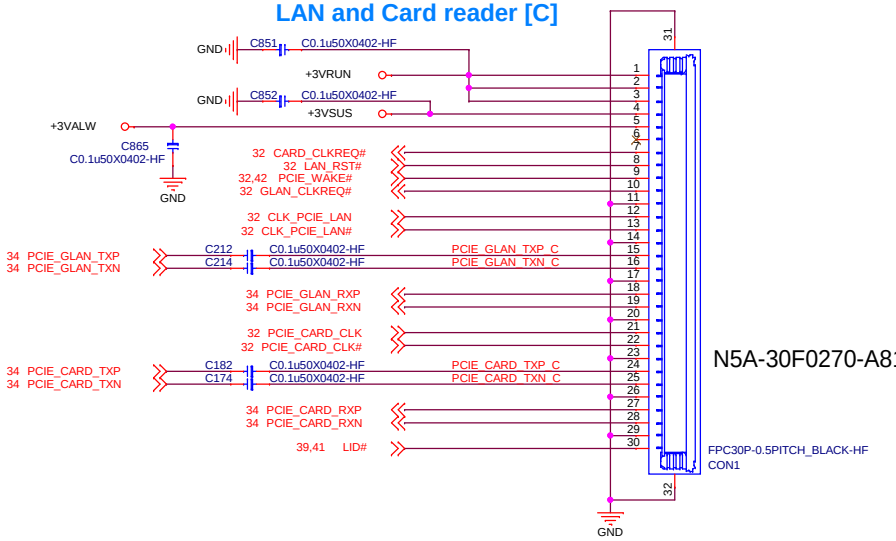












MICRO-STAR INT'L CO.,LTD.

Title: CPU FAN/BTB CONN

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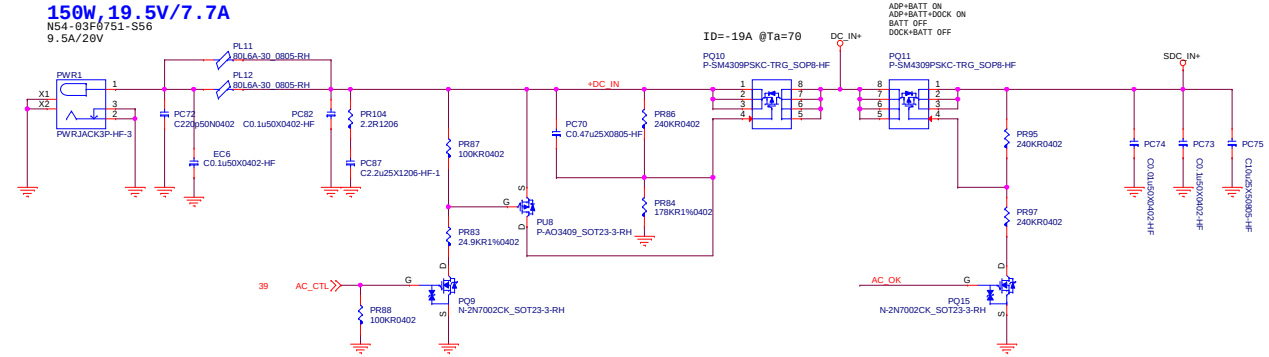
N92-03M0941-SL0

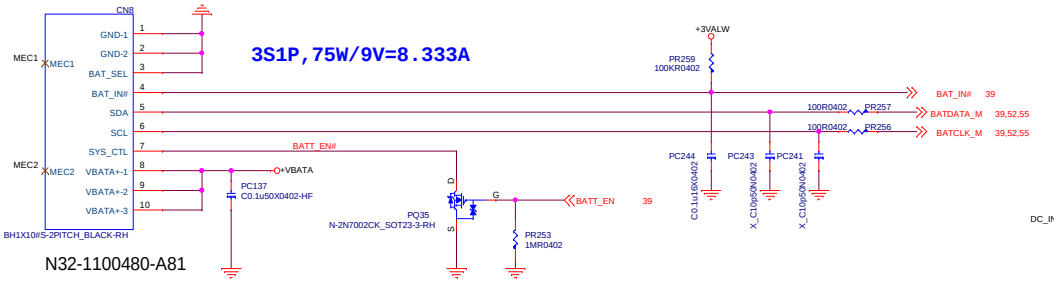
150W,19.5V/7.7A

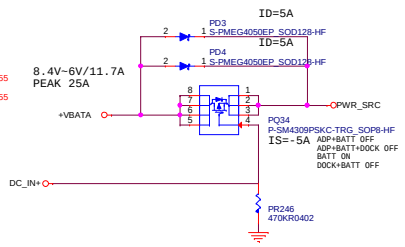
N54-03F0751-S56

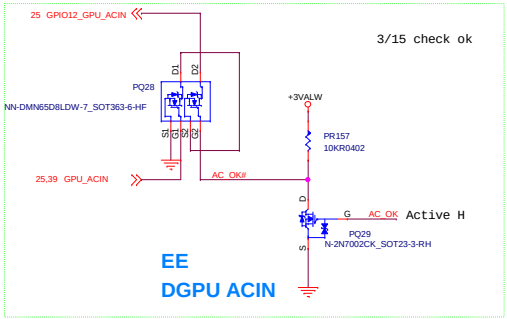
9.5A/20V



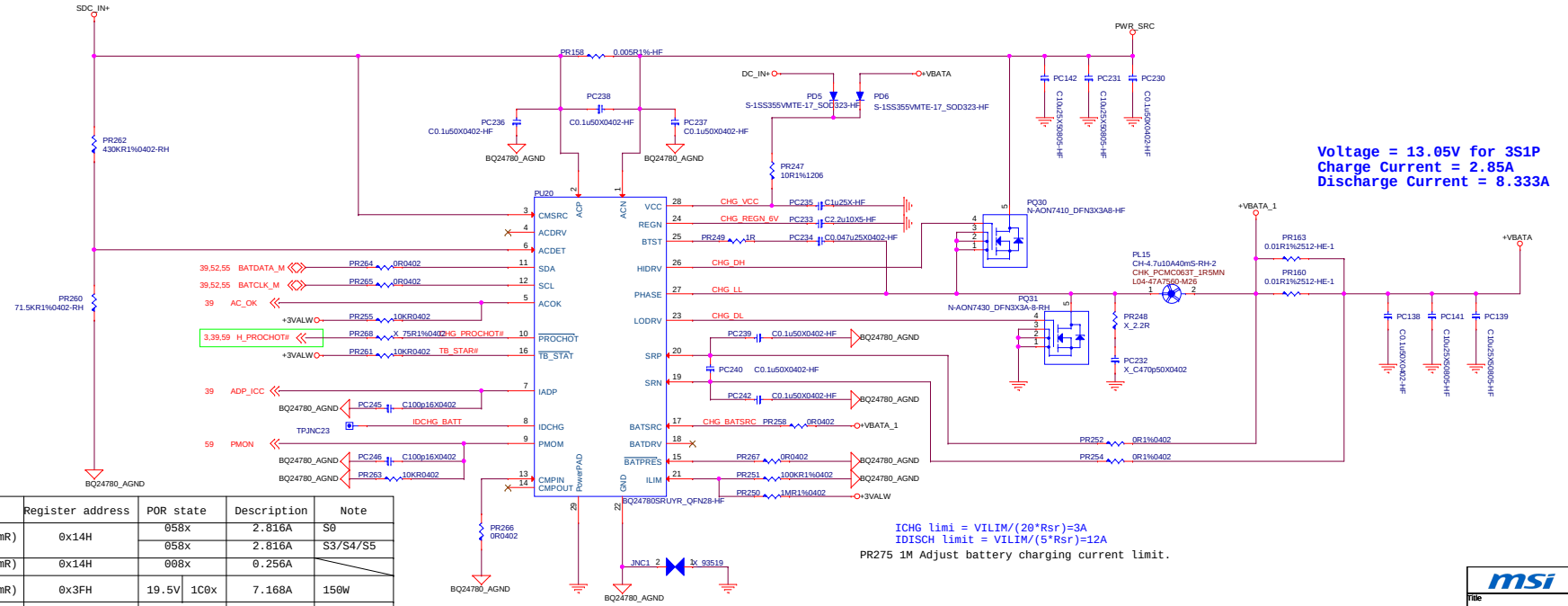
AC_OK#	GPU_ACIN (EC control)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC







N32-1100480-A81



Voltage = 13.05V for 3S1P
Charge Current = 2.85A
Discharge Current = 8.333A

Register name	Register address	POR state	Description	Note
Charge current(5mR)	0x14H	058x	2.816A	S0
		058x	2.816A	S3/S4/S5
Prepare charge(5mR)	0x14H	008x	0.256A	
Input current(10mR)	0x3FH	19.5V 1C0x	7.168A	150W
Charge voltage	0x15H	330x	13.056V	3S1P
Discharge current(5mR)	0x39H	06xx	3.072A	BOOST current

ICHG limi = VILIM/(20*Rsr)=3A
IDISCH limit = VILIM/(5*Rsr)=12A

PR275 1M Adjust battery charging current limit.

MICRO-STAR INT'L CO.,LTD.

Title: **Battery select/Charger**

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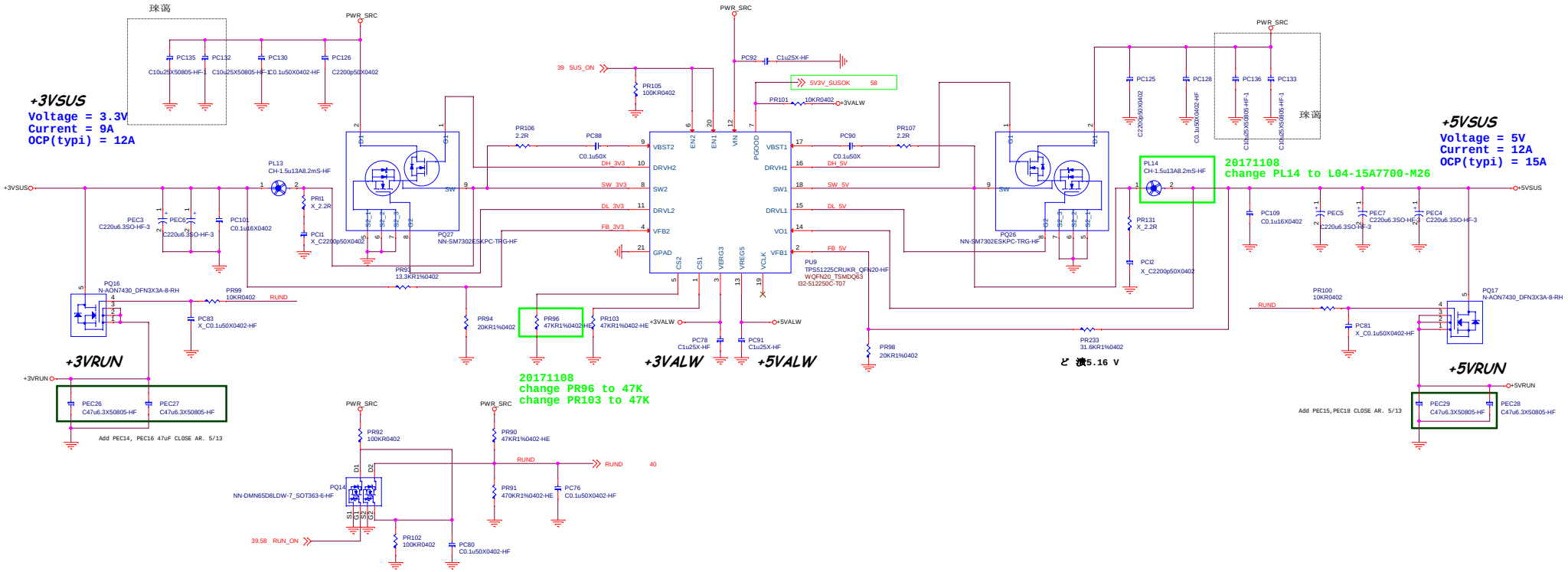
System Power



MICRO-STAR INT'L CO.,LTD.			
Title: System Power			
Size: Custom	Document Number: MS-16K71		Rev: 10
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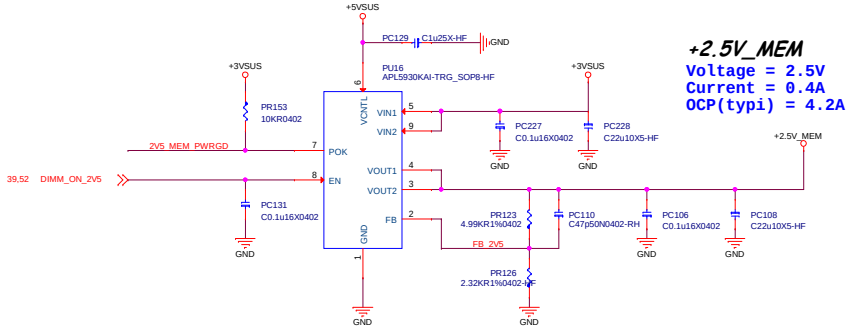
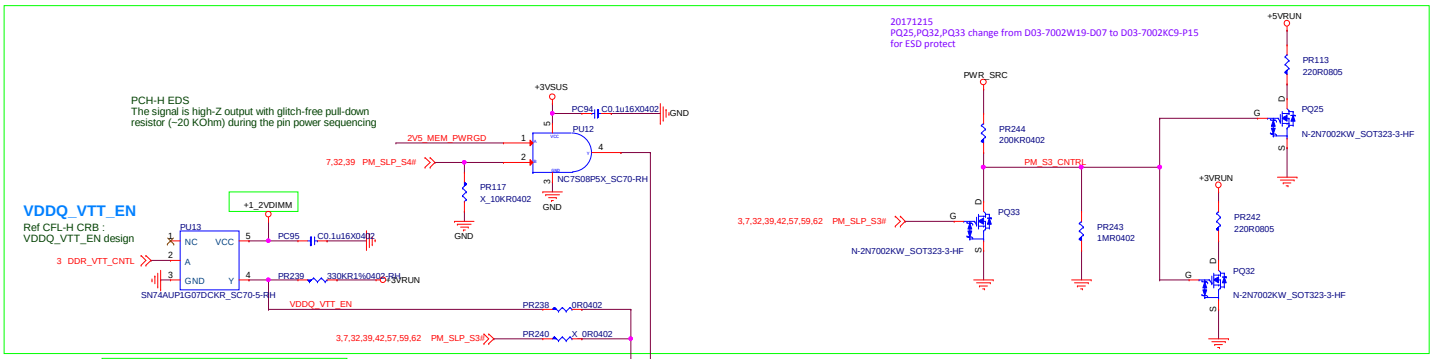
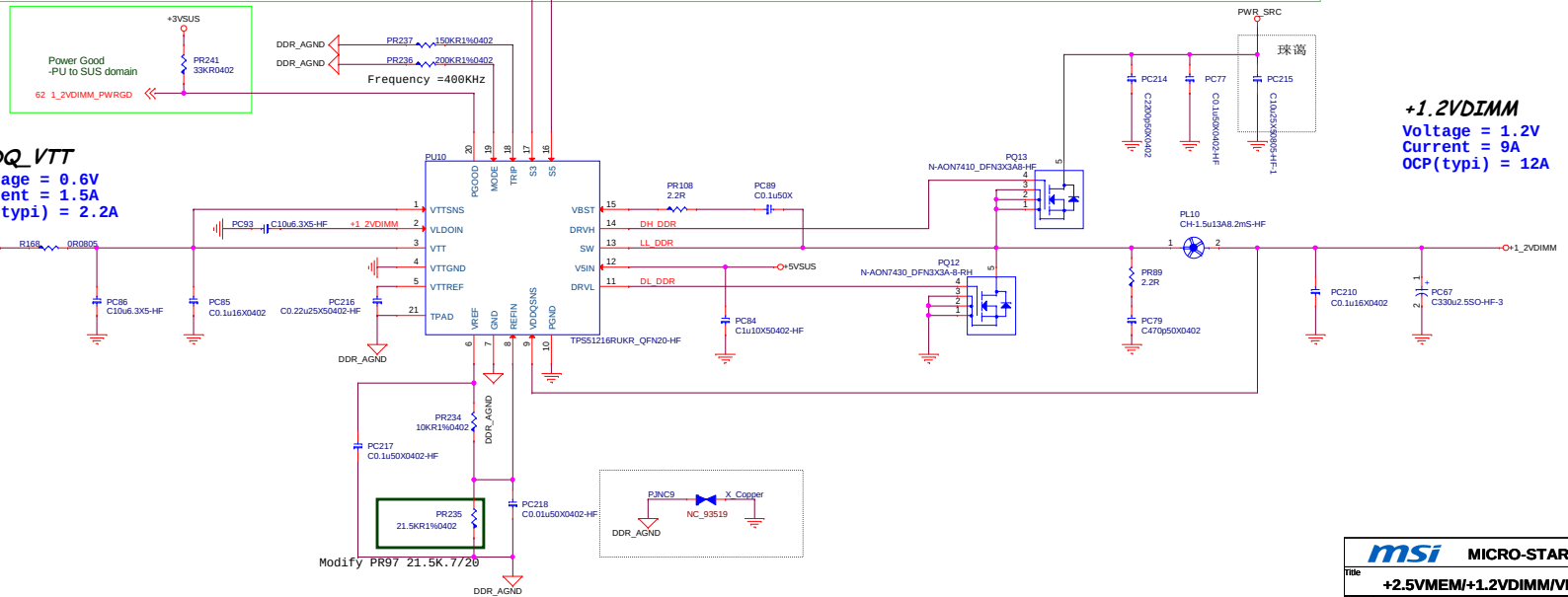
+2.5V_MEM (DDR4/Vpp)



+2.5V_MEM
Voltage = 2.5V
Current = 0.4A
OCP(typi) = 4.2A

+1.2VDIMM / VDDQ_VTT(0.6V)





VDDQ_VTT
Voltage = 0.6V
Current = 1.5A
OCP(typi) = 2.2A

+1.2VDIMM
Voltage = 1.2V
Current = 9A
OCP(typi) = 12A

MICRO-STAR INT'L CO.,LTD.		
Title: +2.5VMEM/+1.2VDIMM/VDDQ_VTT		
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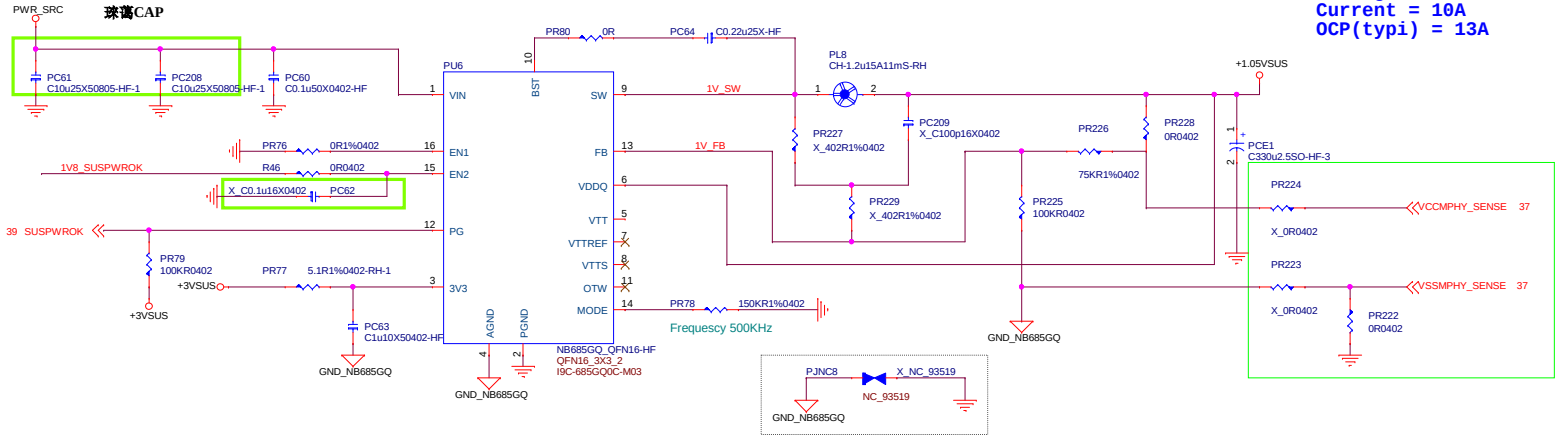
+1.05VSUS

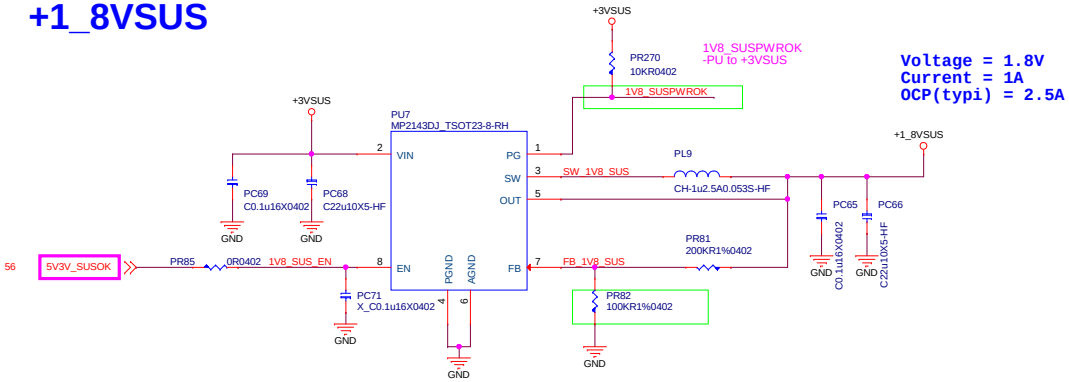
20171108
change PC62 to unstuff

Voltage = 1.05V
Current = 10A
OCP(typi) = 13A

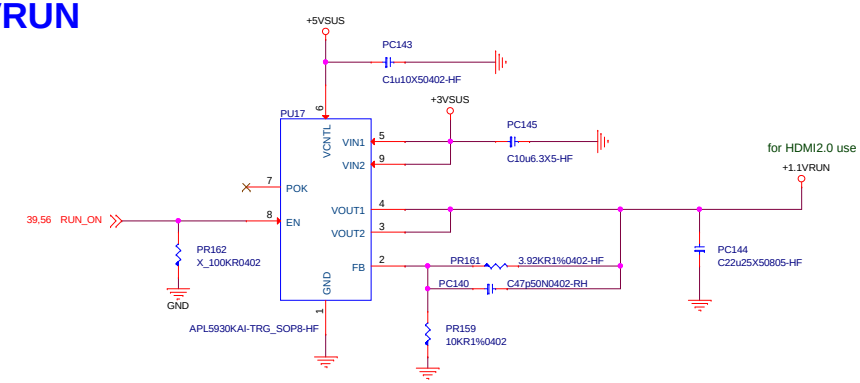


+1_8VSUS

Voltage = 1.8V
Current = 1A
OCP(typi) = 2.5A



+1.1VRUN



MICRO-STAR INT'L CO.,LTD.		
Title: +1.05VSUS/+1_8VSUS/+1.1VRUN		
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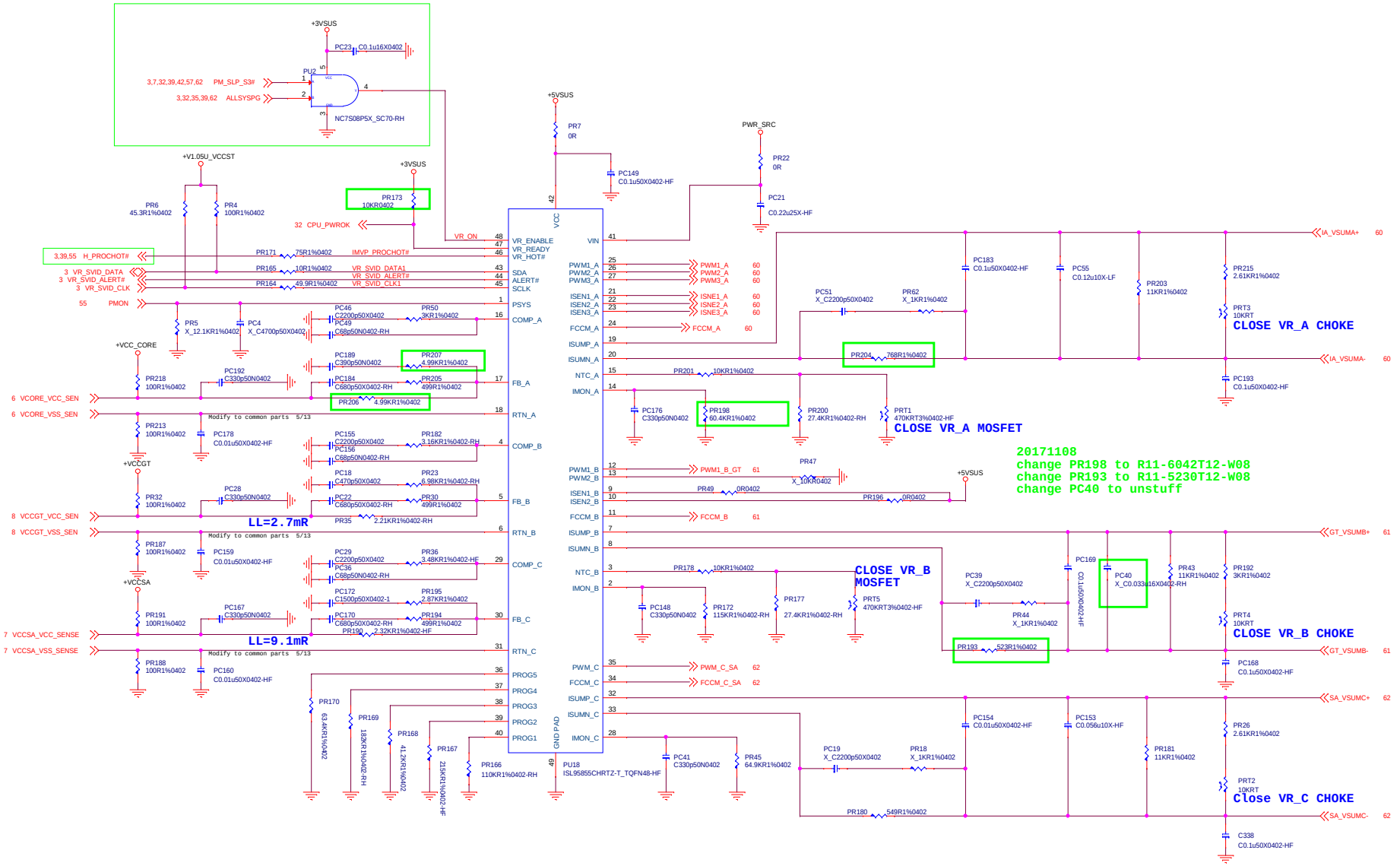
Coffee Lake H-line 6+2
45W ISL95855A



msi MICRO-STAR INT'L CO.,LTD.			
Title: CFL-H 6+2 45W ISL95855A			
Size: Custom	Document Number: MS-16K71		Rev: 10
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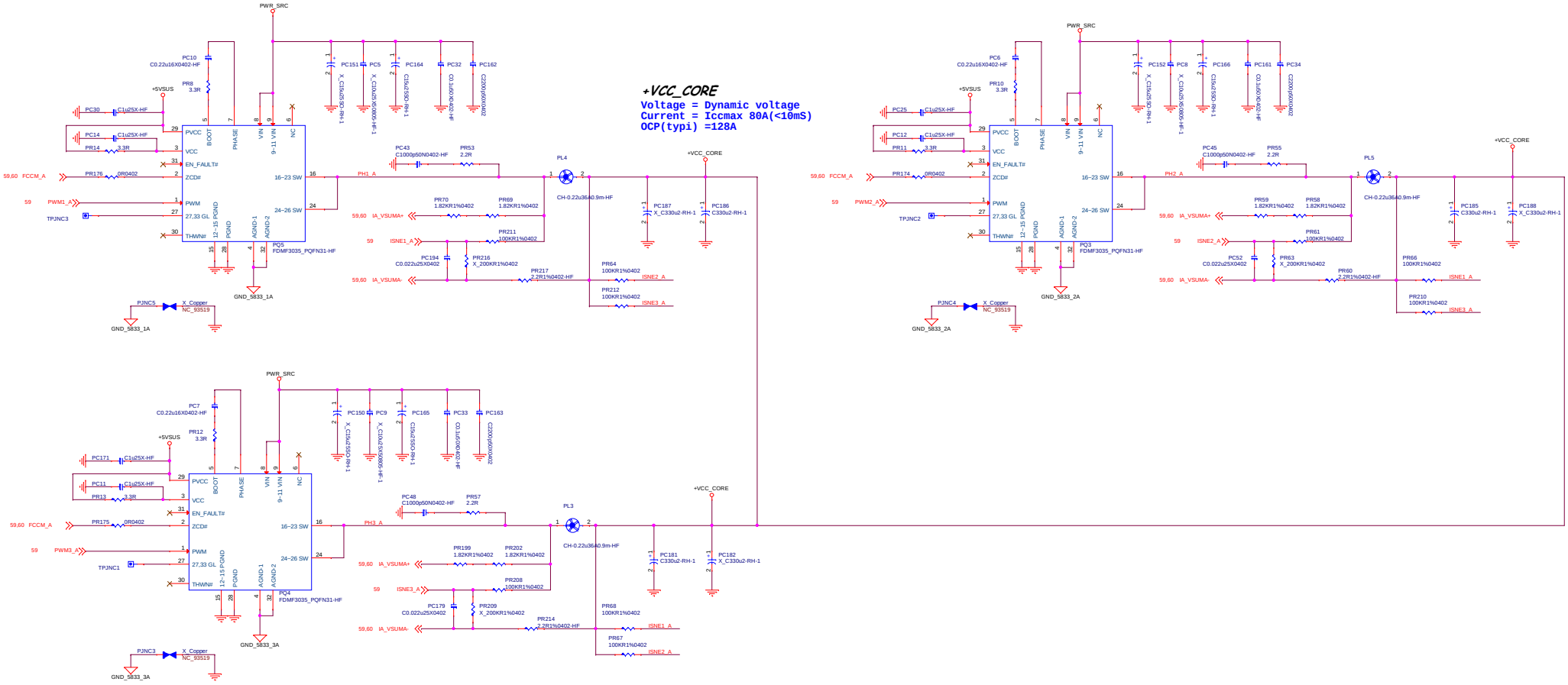

MSI	MICRO-STAR INT'L CO.,LTD.		
Title: Vcore			
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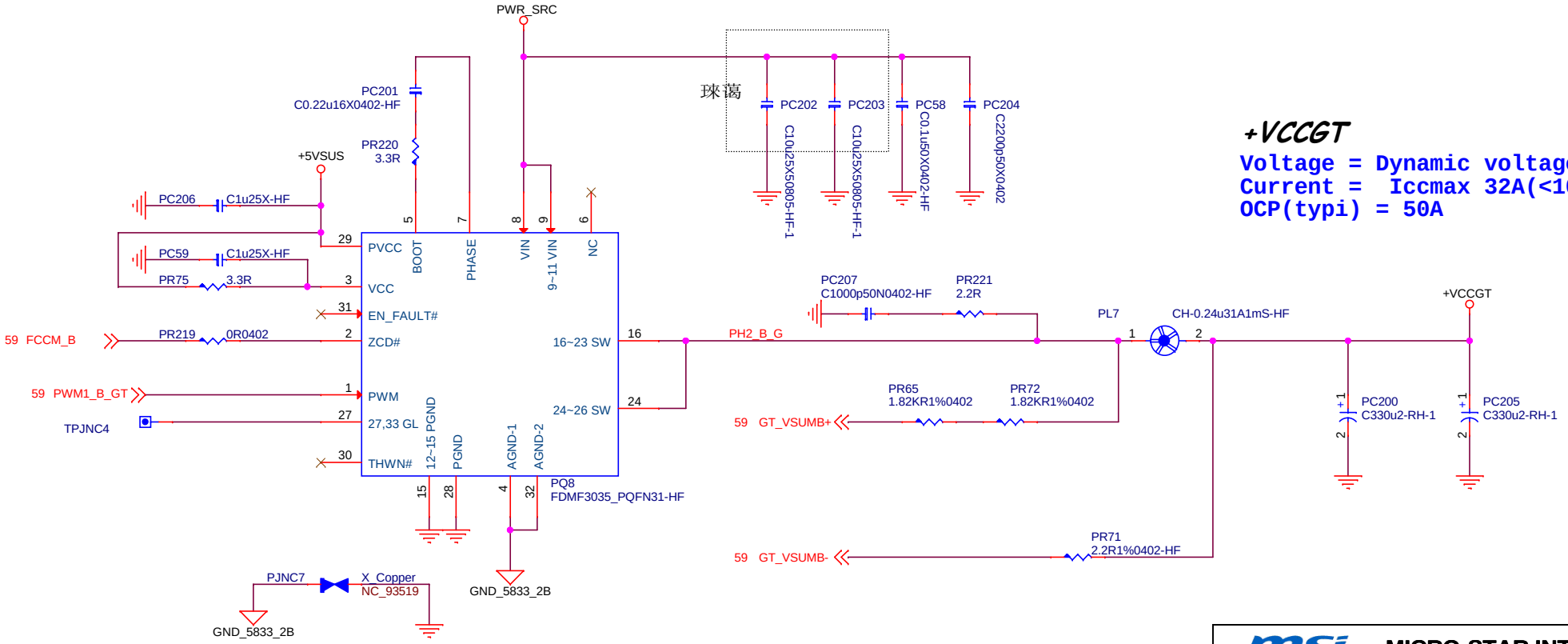
+VCCGT



+VCCGT

Voltage = Dynamic voltage
Current = Iccmax 32A(<10mS)
OCP(typi) = 50A

MICRO-STAR INT'L CO.,LTD.		
Title: VCCGT		
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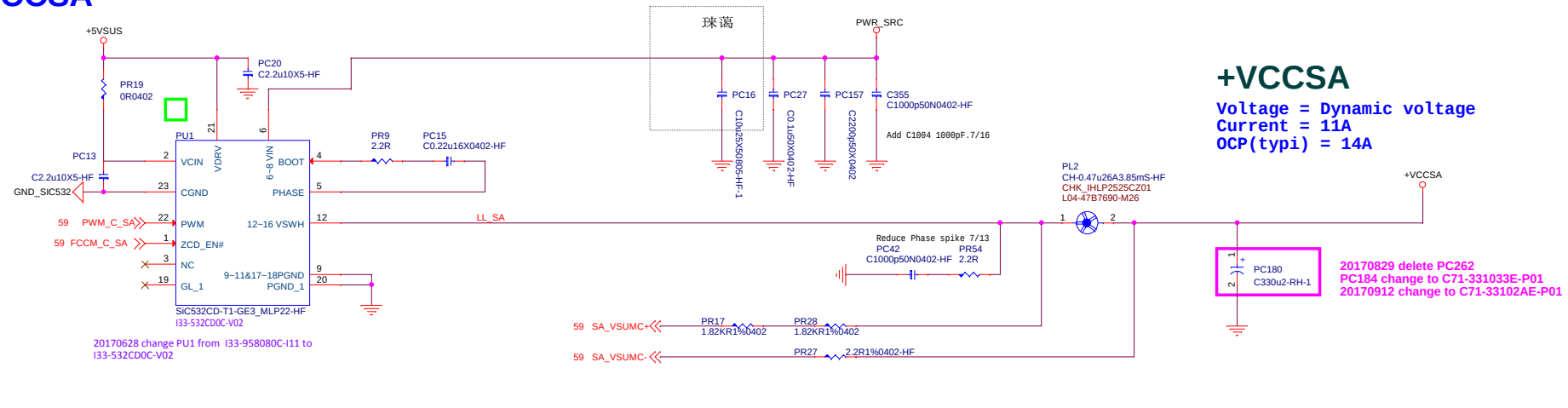
+VCCSA



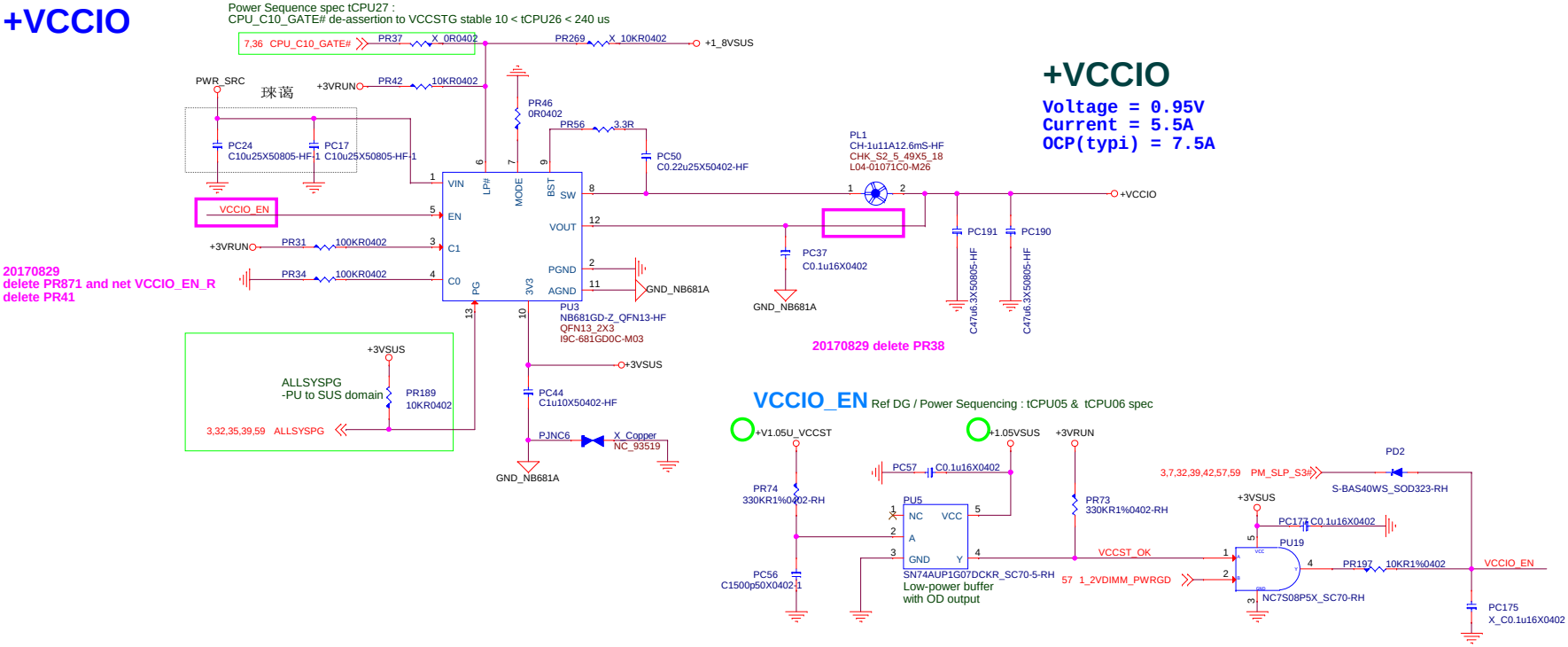
20170628 change PU1 from I33-958080C-I11 to I33-532CD0C-V02

+VCCSA

Voltage = Dynamic voltage
Current = 11A
OCP(typi) = 14A

20170829 delete PC262
PC184 change to C71-331033E-P01
20170912 change to C71-33102AE-P01

+VCCIO



20170829
delete PR871 and net VCCIO_EN_R
delete PR41

20170829 delete PR38

+VCCIO

Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A

VCCIO_EN Ref DG / Power Sequencing : tCPU05 & tCPU06 spec

MICRO-STAR INT'L CO.,LTD.			
Title: VCCSA/VCCIO			
Size: Custom	Document Number: MS-16K71		Rev: 10
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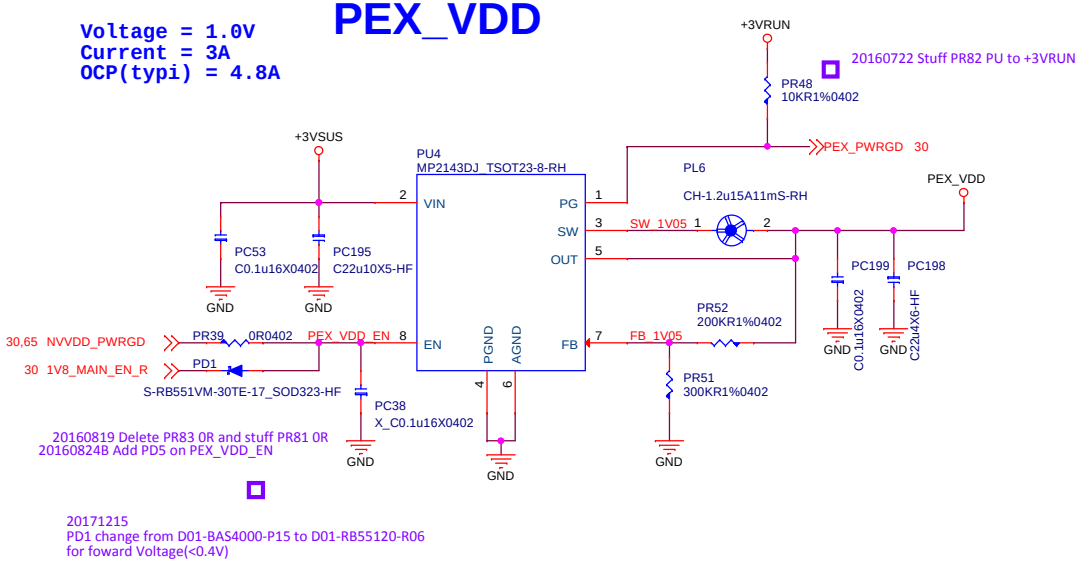
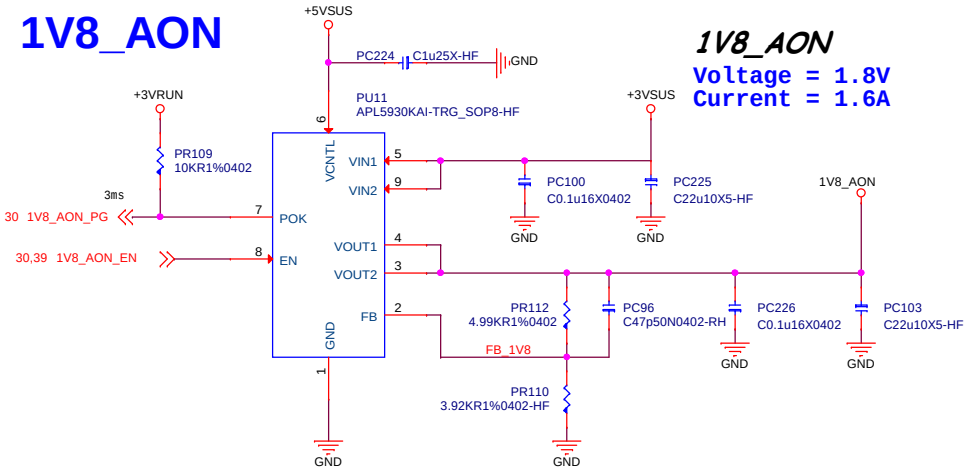
PEX_VDD

Voltage = 1.0V
Current = 3A
OCP(typi) = 4.8A



1V8_AON



MICRO-STAR INT'L CO.,LTD.		
Title: PEX_VDD/1.8V		
Size: Custom	Document Number: MS-16K71	Rev: 10
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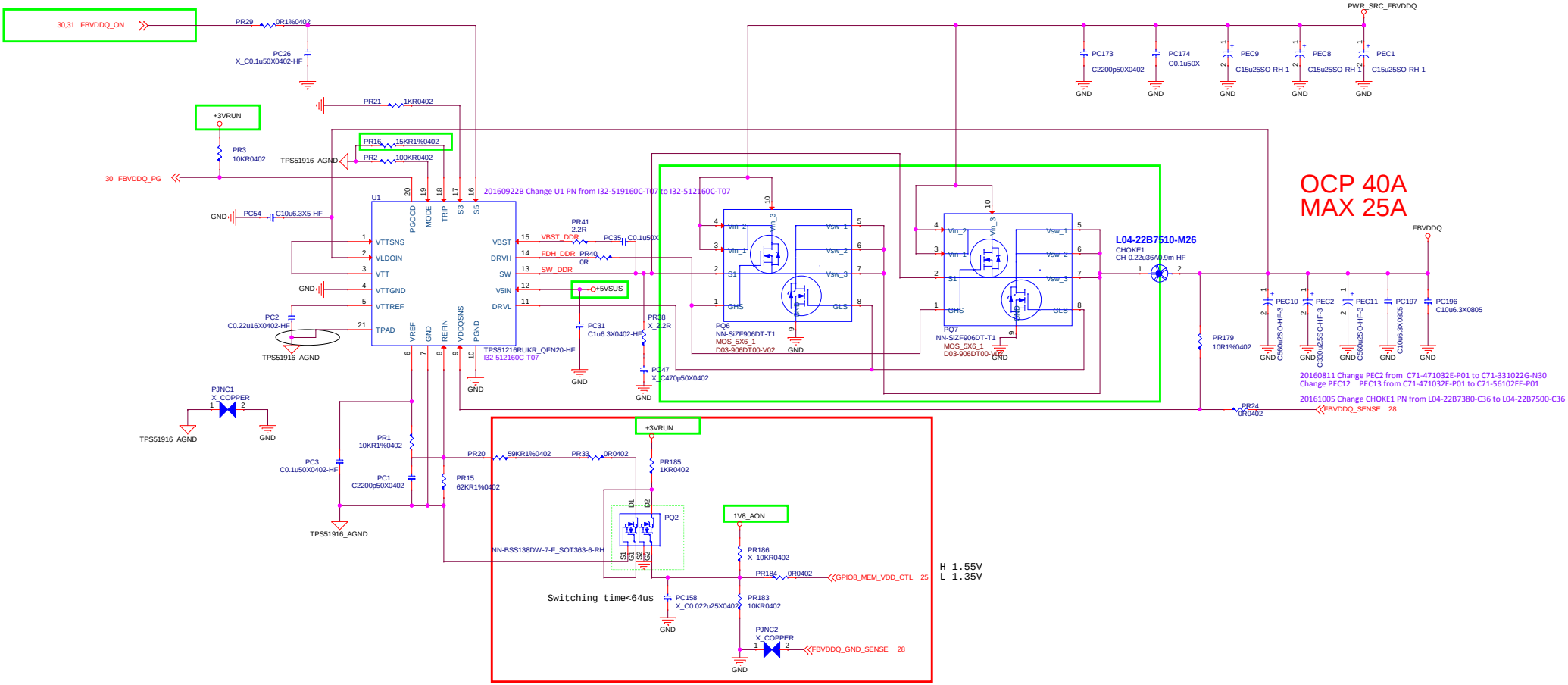
FBVDDQ

20171108
change PR16 to R11-0153T12-W08



msi MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
Size	Document Number: MS-16K71	Rev: 10
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DGPU POWER / UP9509P

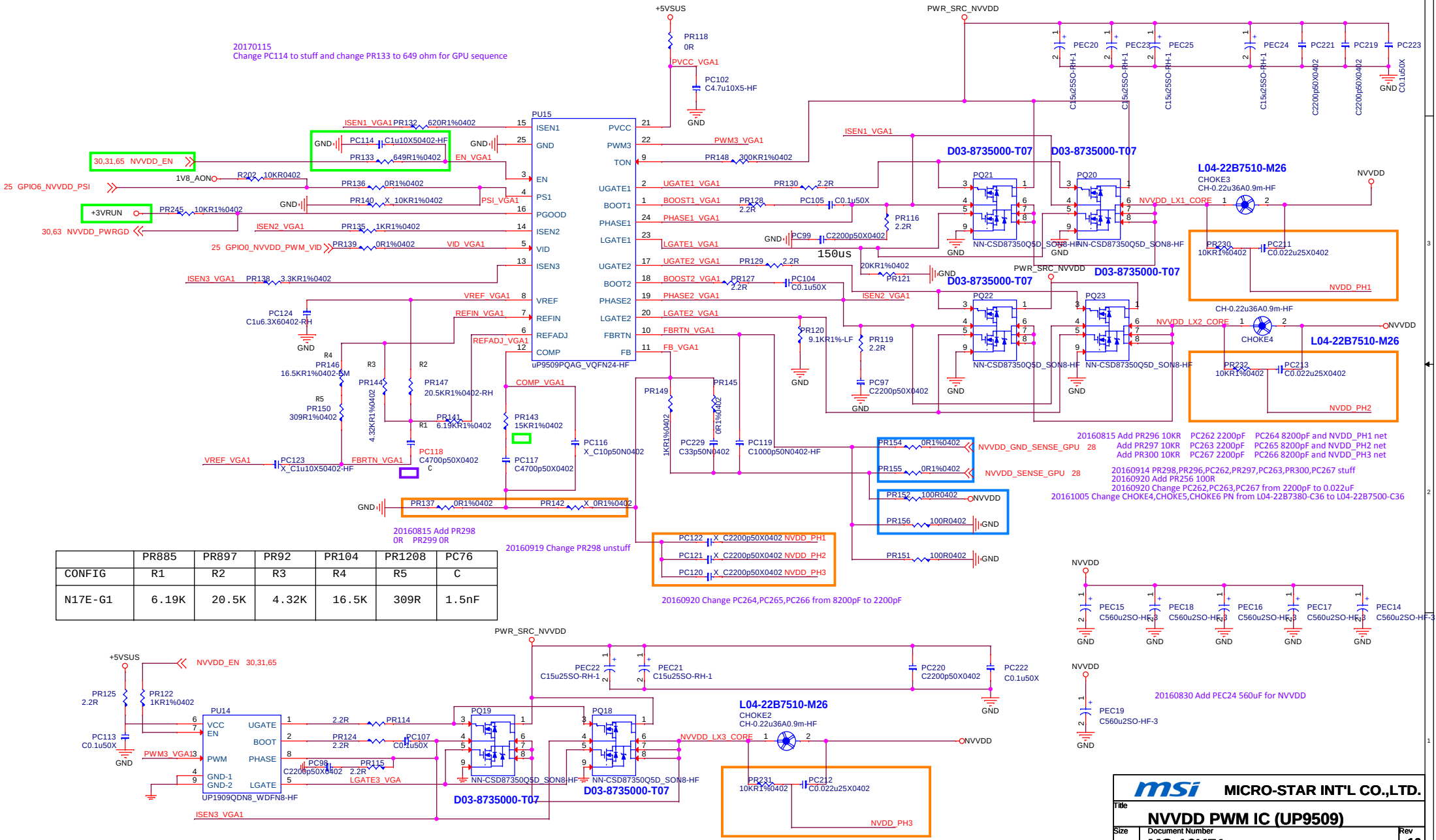
EDP-Peak 180A

EDP-Con 80A

DGPU POWER NVVDD

VBoot:0.8V

Vmin:0.3V / Vmax:1.3V

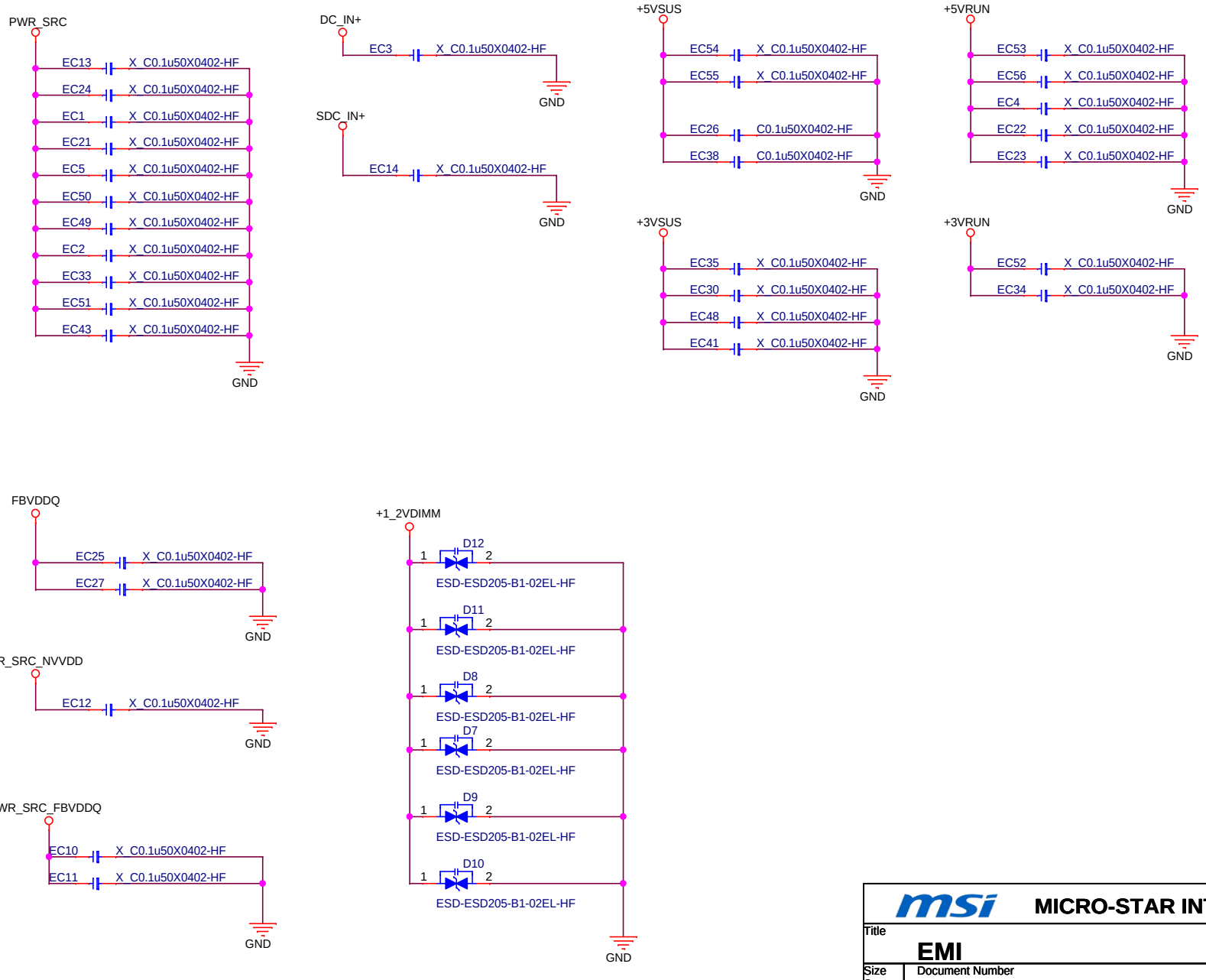


	PR885	PR897	PR92	PR104	PR1208	PC76
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

Title	NVVDD PWM IC (UP9509)
Size	Document Number: MS-16K71
Rev	10
Date:	Sheet 65 of 79

MICRO-STAR INT'L CO.,LTD.

EMI



MICRO-STAR INT'L CO.,LTD.		
Title: EMI		
Size: Custom	Document Number: MS-16K71	Rev: 10
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dGPU Holes

MGPU1
H_R185D169BR276_PB_N

MGPU2
H_R185D169BR276_PB_N

GND

CPU Holes

MCPU2 H_R276D169_PB_N
MCPU1 H_R276D169_PB_N
MCPU3 H_R276D169_PB_N

GND

UME5
CPU BKT
CPU_GPU_BRACKET
307-6K70111-HG0

PCB1
PD0-16K7110-H73
PD0-16K7110-H73

FM2 FM12 FM28 FM37
FM4 FM13 FM29 FM38
FM6 FM14 FM30 FM40
FM7 FM16 FM31 FM43
FM8 FM18 FM32
FM9 FM19 FM33
FM10 FM25 FM34
FM11 FM27 FM35

MH6 X_H_R217D91_N
MH10 X_H_R197D118_PT_N
MH13 X_H_O236X256D91X110_N
MH14 X_H_R197D91_N
MH7 X_H_R217D91_N

MH9 X_H_R315D118_1_V3_N
H_R315D118_V3_N
MH5 X_H_R217D91_N
MH11 H_R197D118_PT_N
X_ME_ SCREW HOLE

MH4 X_H_R315D118_1_N
MH3 X_H_NR47D47_1_N
MH8 X_H_NR47D47_1_N

FM21 FM5 FM1 FM26
FM17 FM39 FM23 FM41

XX1 XX16 XX2 XX15 XX17 XX18 XX19
X_H_NR118D118_N

XX20 XX21 XX22 XX23 XX24 XX25 XX26
X_H_NR118D118_N

XX27
X_H_NR118D118_N

E3 E1 E2
X_HS-MS1011-RH

UME13
Y01-REMPAS1-000
EMPASS_USB20
20171108 add

MH12
MXM Stand-off
E2B-16K1010-RH
SSD stand-off bottom

UME1
HDMI Lable
HDMI ROYALTY
Y01-RHDMI03-000

UME2
BIOS Lable
UEFI_CODE_BIOS_LABEL
G51-N1CO041-A09

For MP

20171226 add UME33~40

For 16K7

UME33 E2Y-6K21111-Y40 RUBBER
UME37 E2Y-6K21111-Y40 RUBBER
UME34 E2Y-6K21111-Y40 RUBBER
UME38 E2Y-6K21111-Y40 RUBBER
UME35 E2Y-6K21111-Y40 RUBBER
UME39 E2Y-6K21111-Y40 RUBBER
UME36 E2Y-6K21111-Y40 RUBBER
UME40 E2Y-6K21111-Y40 RUBBER

For 17B7 Memory

UME24 E2Y-7B12311-Y40 X_RUBBER
UME28 E2Y-7B12311-Y40 X_RUBBER
UME25 E2Y-7B12311-Y40 X_RUBBER
UME29 E2Y-7B12311-Y40 X_RUBBER
UME26 E2Y-7B12311-Y40 X_RUBBER
UME30 E2Y-7B12311-Y40 X_RUBBER
UME27 E2Y-7B12311-Y40 X_RUBBER
UME31 E2Y-7B12311-Y40 X_RUBBER

For 17B7

UME10 E2P-7B12211-Y42 X_EMI
UME12 E2Y-7B12411-Y40 X_RUBBER
UME41 E2P-1211311-G40 X_MYLAR
UME11 E2P-7B12611-G40 X_RUBBER

For 16K7

UME9
MB PC
MB_PC
E2P-6K11611-Y42

RU2
E2M-3570611-G40
MECH

20171226 delete UME21~UME23 for useless(ME)
20180110 add UME41 for 17B7 ME

MICRO-STAR INT'L CO.,LTD.

Title: Screw/ME
Size: Document Number: MS-16K71 Rev: 10
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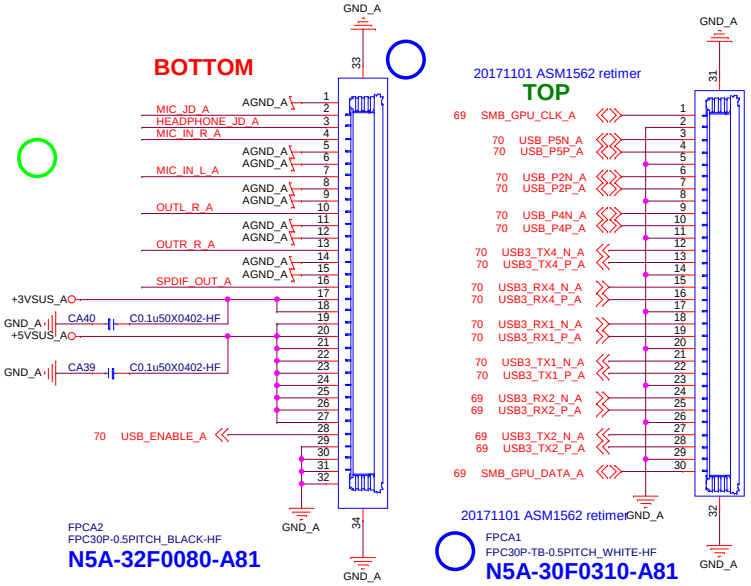
16K7-A Board (Audio CONN)

20171220
change FPCA2 to 32pin and modify FPCA1 pin define for new design
(Audio issue and USB3.1 solution change)

BTB Connector From MB

CONN Pin Current Capability : ???A/Pin

BOTTOM



N5A-32F0080-A81

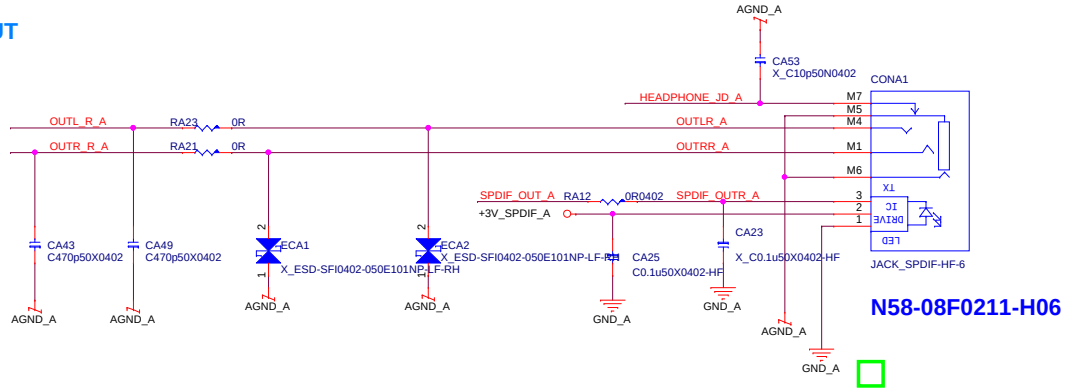
20171101 ASM1562 retimer

TOP

N5A-30F0310-A81

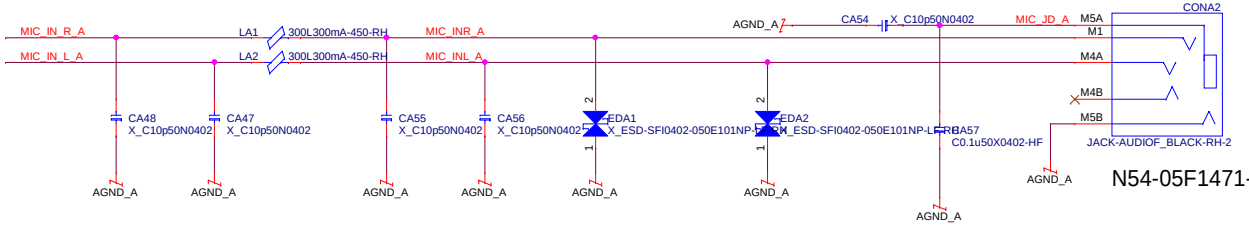
10Gb

HP OUT / SPDIF OUT



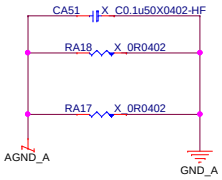
N58-08F0211-H06

MIC IN



N54-05F1471-H06

FMA7 FMA8

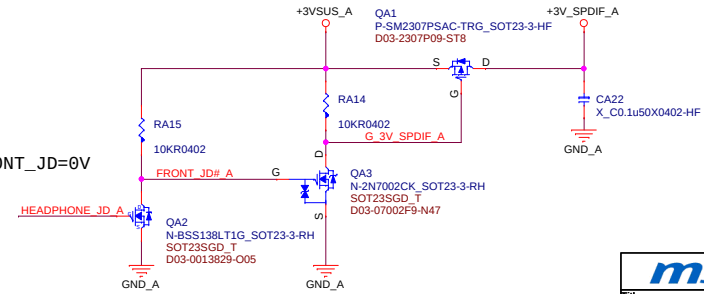


EMI

VGS_ON : -1V~-2V

SPDIF Power

ALC1220 FRONT_JD=0V



MSI	MICRO-STAR INT'L CO.,LTD.		
Title	[A] Audio		
Size: Custom	Document Number: MS-16K7A		Rev: 10
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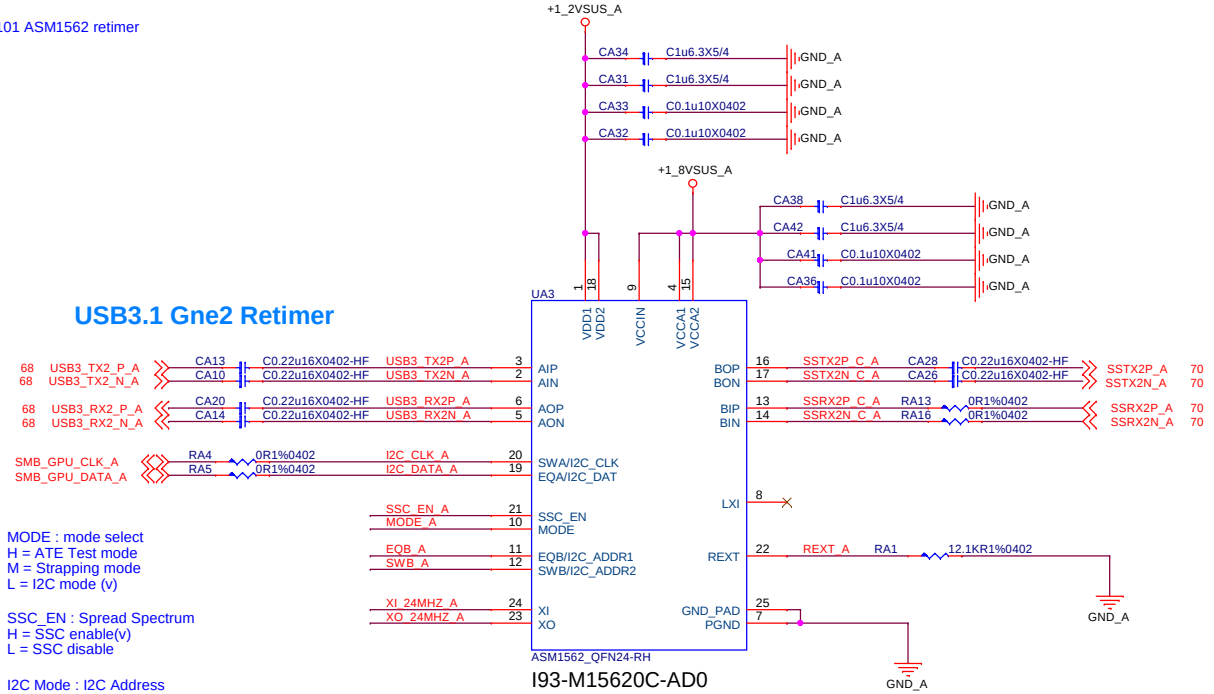
USB3.1 Gne2 Retimer ASM1562

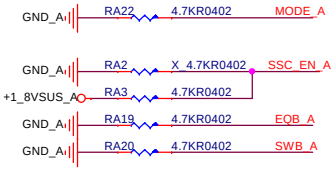
20171101 ASM1562 retimer

USB3.1 Gne2 Retimer



EC

Strap

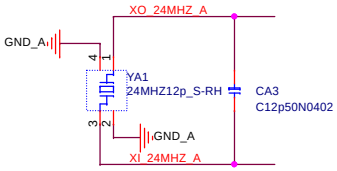


MODE : mode select
H = ATE Test mode
M = Strapping mode
L = I2C mode (v)

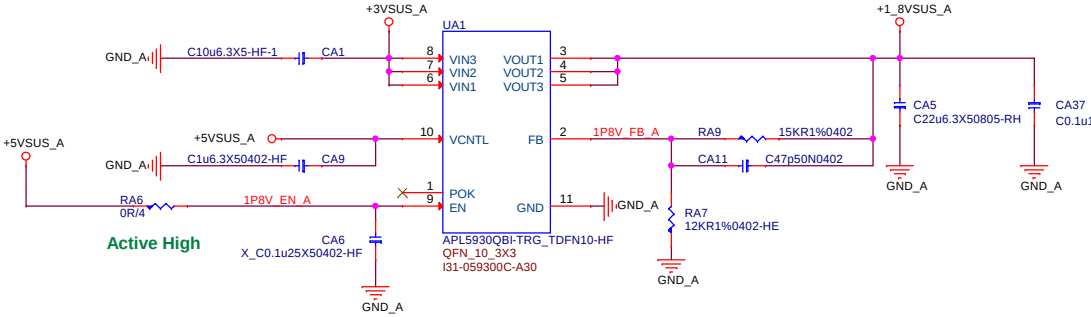
SSC_EN : Spread Spectrum
H = SSC enable(v)
L = SSC disable

I2C Mode : I2C Address
EQB = Address 1 ; SWB = Address 2
LL = 78

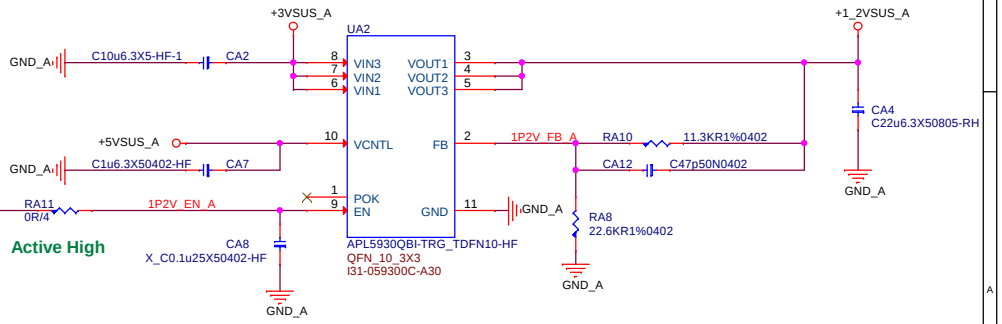
24MHz Clock



+1_8VSUS_A



+1_2VSUS_A



MICRO-STAR INT'L CO.,LTD.

Title: [A] USB3.1 GEN2 REDRIVER

Size	Document Number	Rev
A3	MS-16K7A	10

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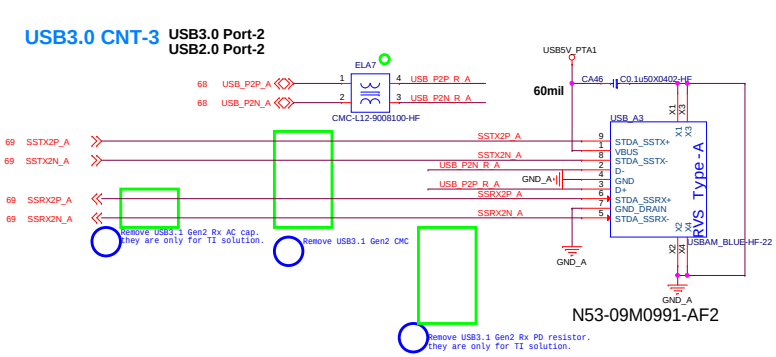
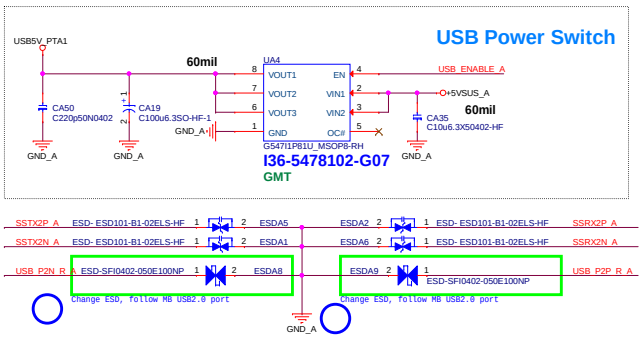
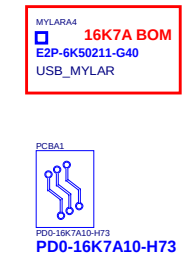
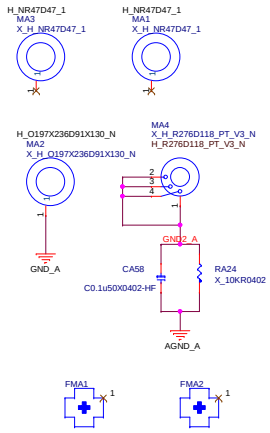
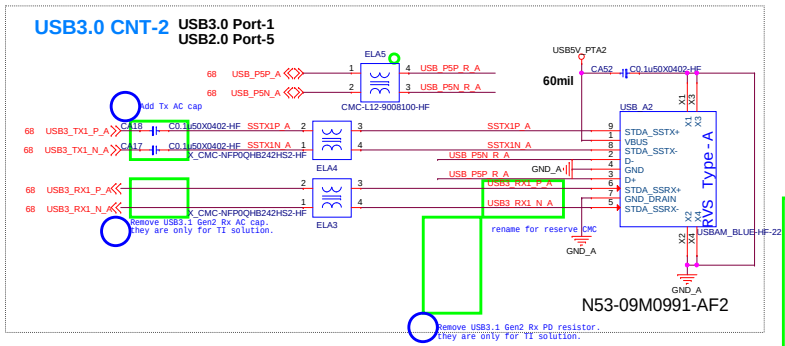
[A] USB3.0 CNT-2/-3

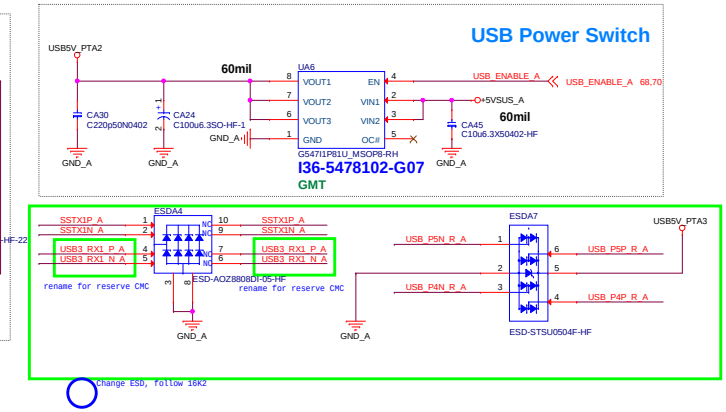


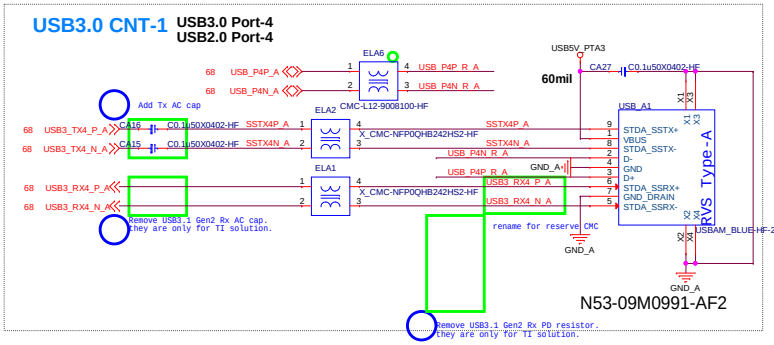


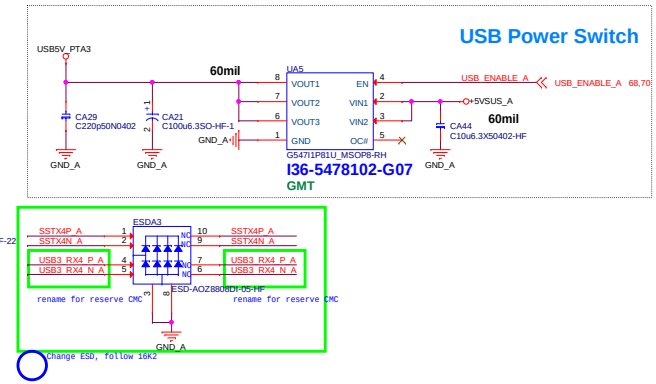












msi	MICRO-STAR INT'L CO.,LTD.		
Title	[A] USB3.0 CNT-3/-4		
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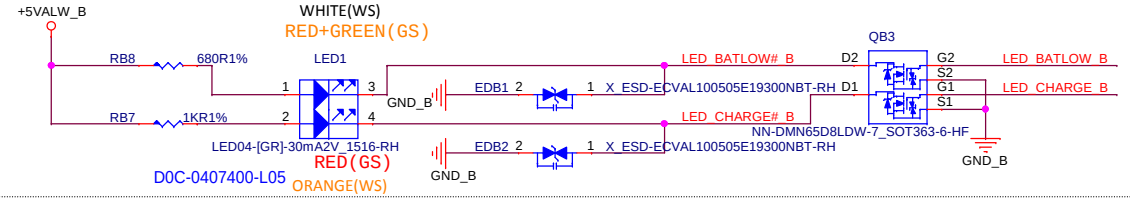
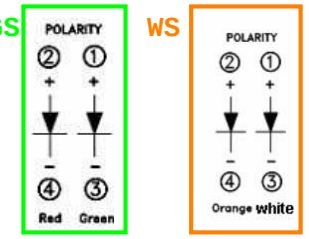
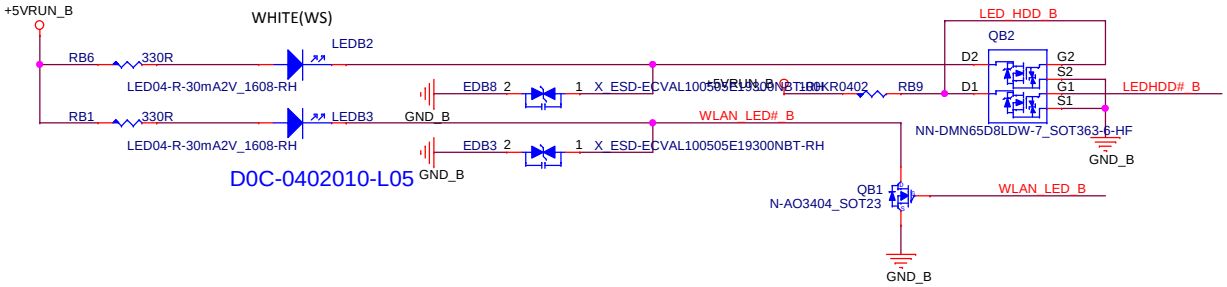
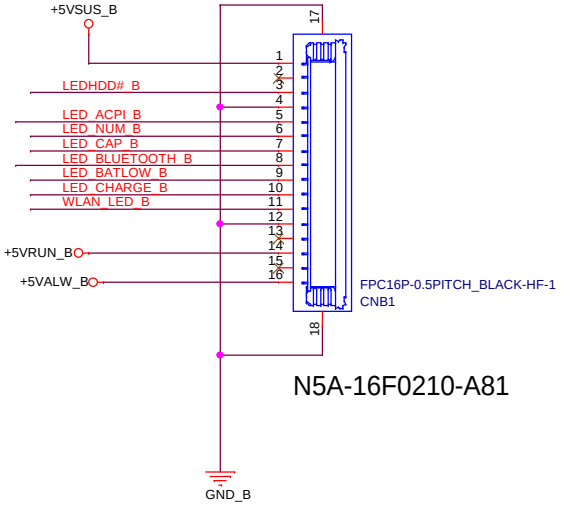
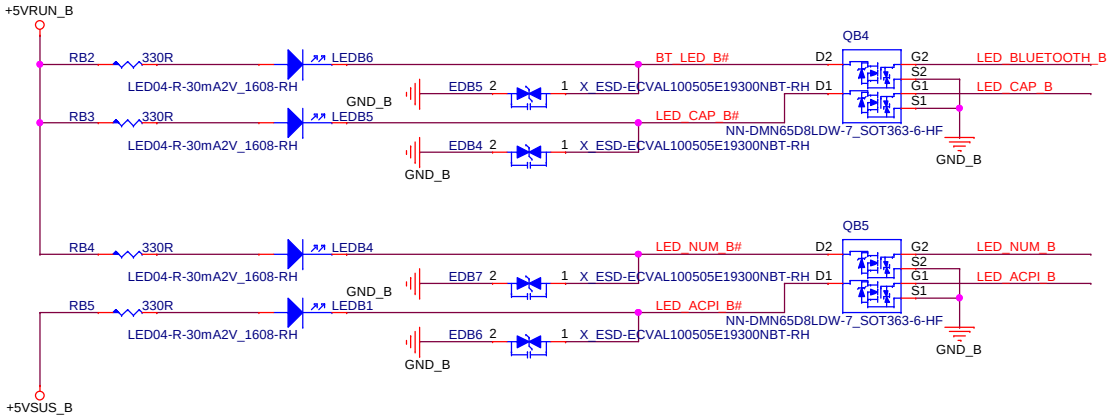
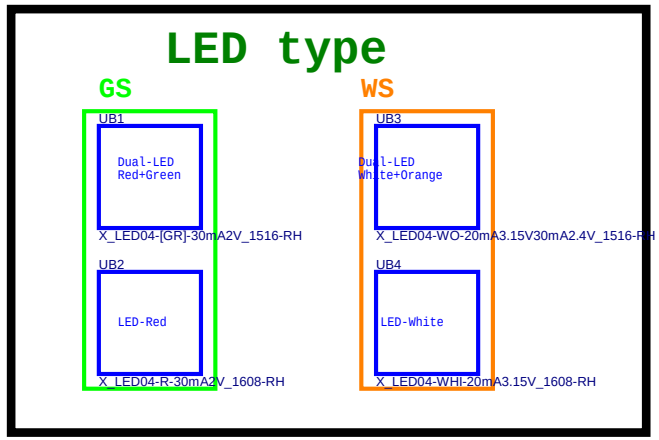




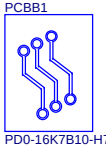




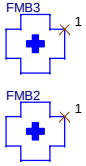


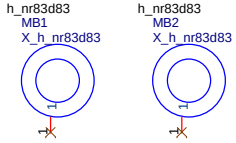


Hannstar: H73
TRIPOD: T53



PD0-16K7B10-H73





MICRO-STAR INT'L CO.,LTD.

Title	[B] LED	
Size B	Document Number MS-16K7B	Rev 10
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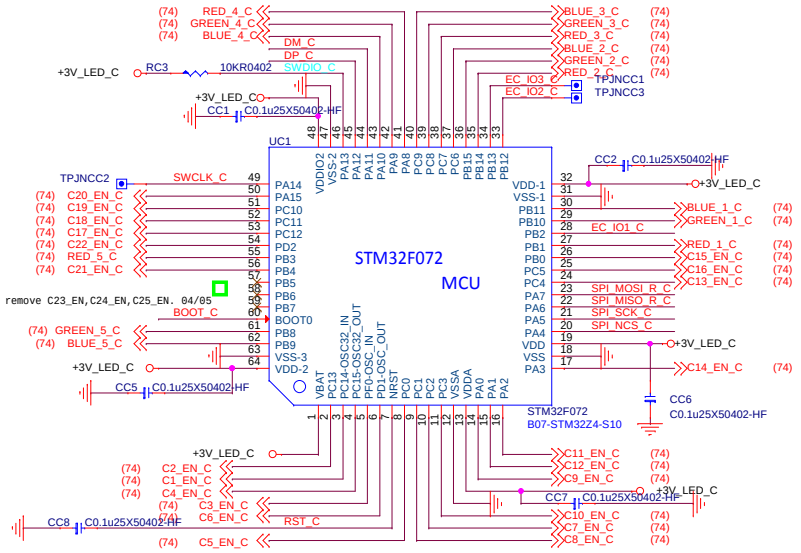
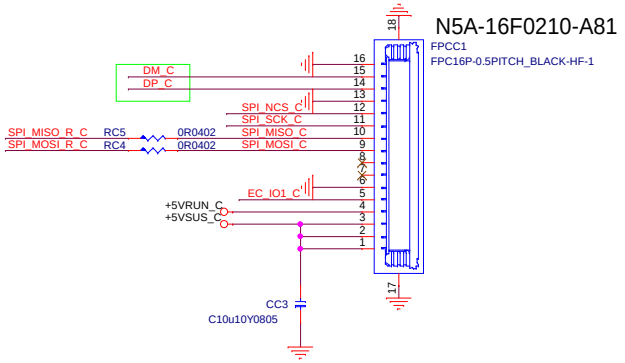
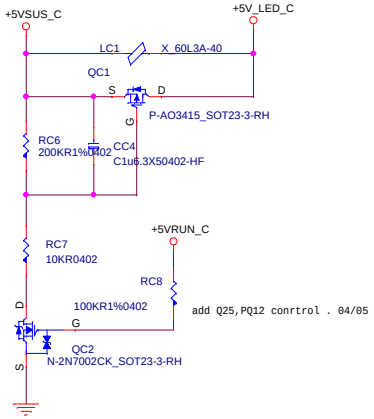
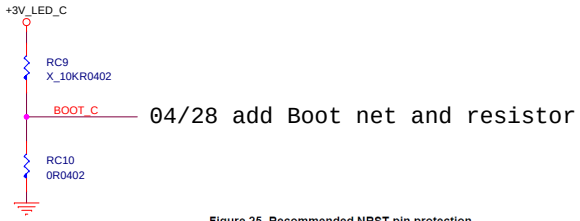




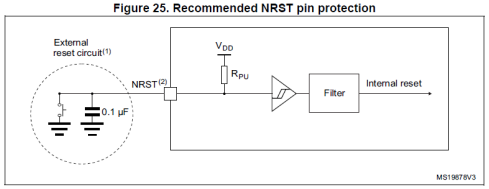


Confirm Pin 1 position

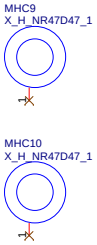


04/28 add Boot net and resistor

Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.



UMEC5 **16K7C BOM**

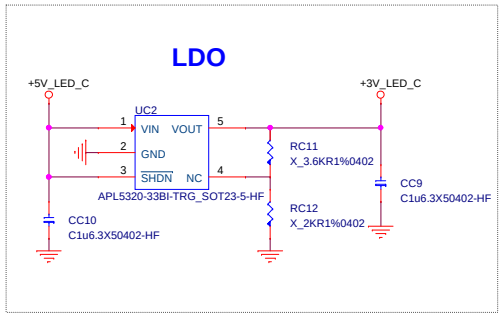
E2Y-Z001511-G40

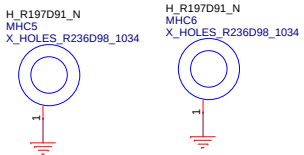
MECH WASHER

UMEC6

E2Y-Z001511-G40

MECH WASHER





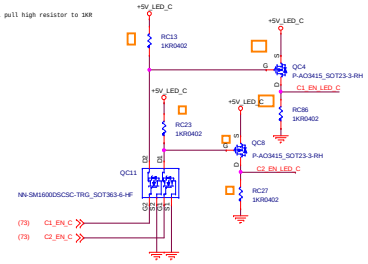
MICRO-STAR INT'L CO.,LTD.

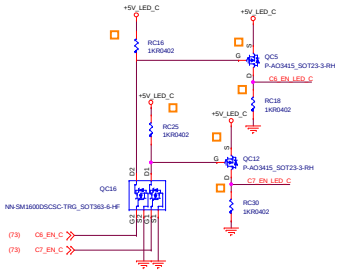
Title: [C]MCU/Matrix/Power

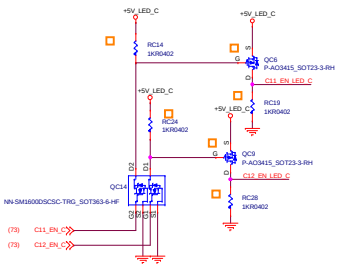
Size | Document Number: MS-16K7C | Rev: 10

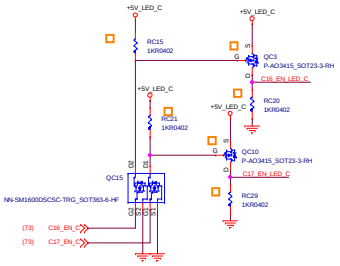
Date: | Sheet 72 of 80

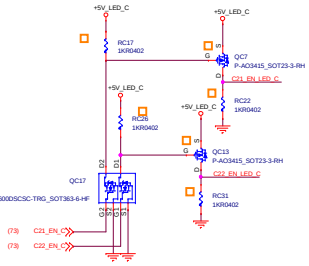
2016/12/01 modfiy all pull high resistor to 1KR

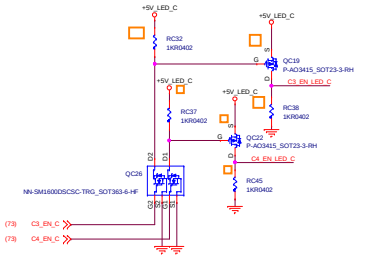


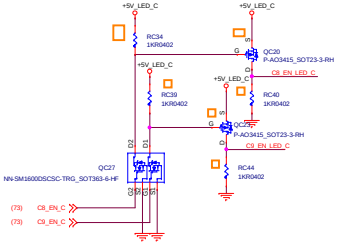


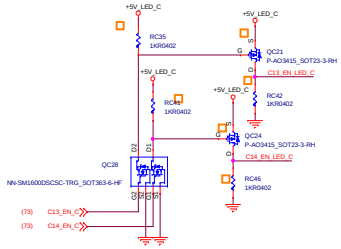


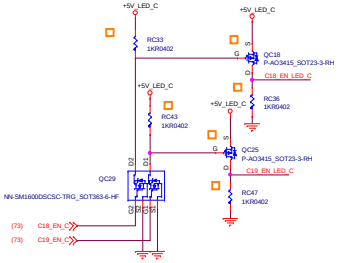










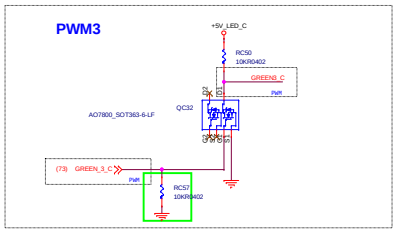


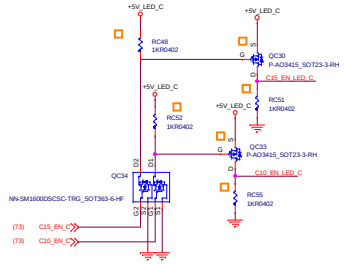
Modify R10,R11,R12,R13,R14,R19,R20,R22,R23,R24,R30,R31,R32,R33,R40,R41,R42,R43,R50,R51,R52,R56 3K to 1K

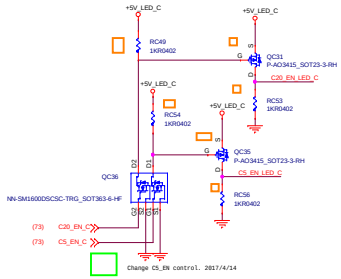
Modify R15,R16,R17,R18,R21,R25,R26,R27,R28,R29,R34,R35,R36,R37,R38,R45,R46,R47,R48,R54,R55,R57,R58 1K to 1.5K

Modify Q1,Q11,Q16,Q17,Q18,Q19,Q2,Q21,Q22,Q23,Q24,Q3,Q31,Q32,Q33,Q35,Q4,Q5,Q6,Q7,Q8,Q9 AO3407A to AO3415

2017/04/19

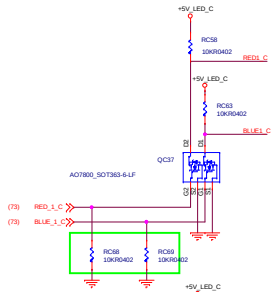


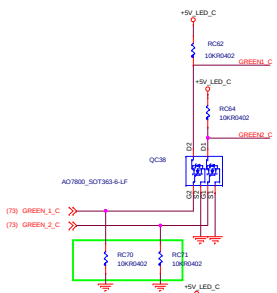


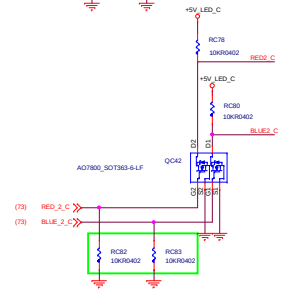


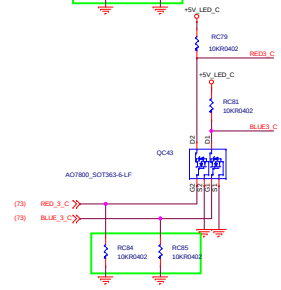
Change C5_EN control. 2017/4/14

PWM1 PWM2 PWM3

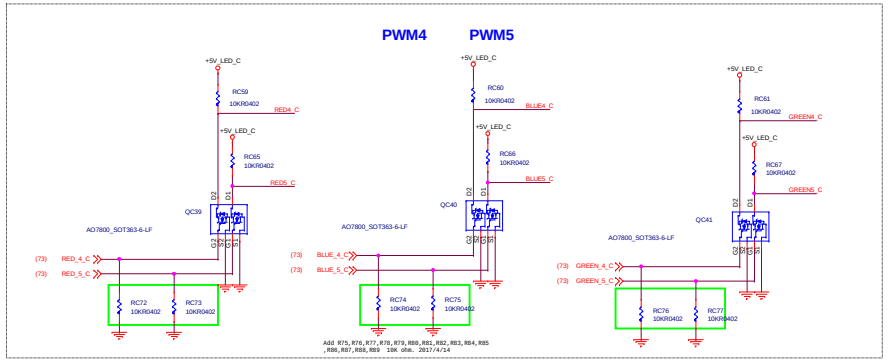




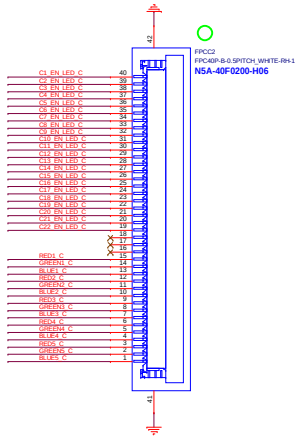




PWM4 PWM5



Add R75,R76,R77,R78,R79,R80,R81,R82,R83,R84,R85,R86,R87,R88,R89 10K ohm. 2017/4/14



PD0-16K7C10-H73

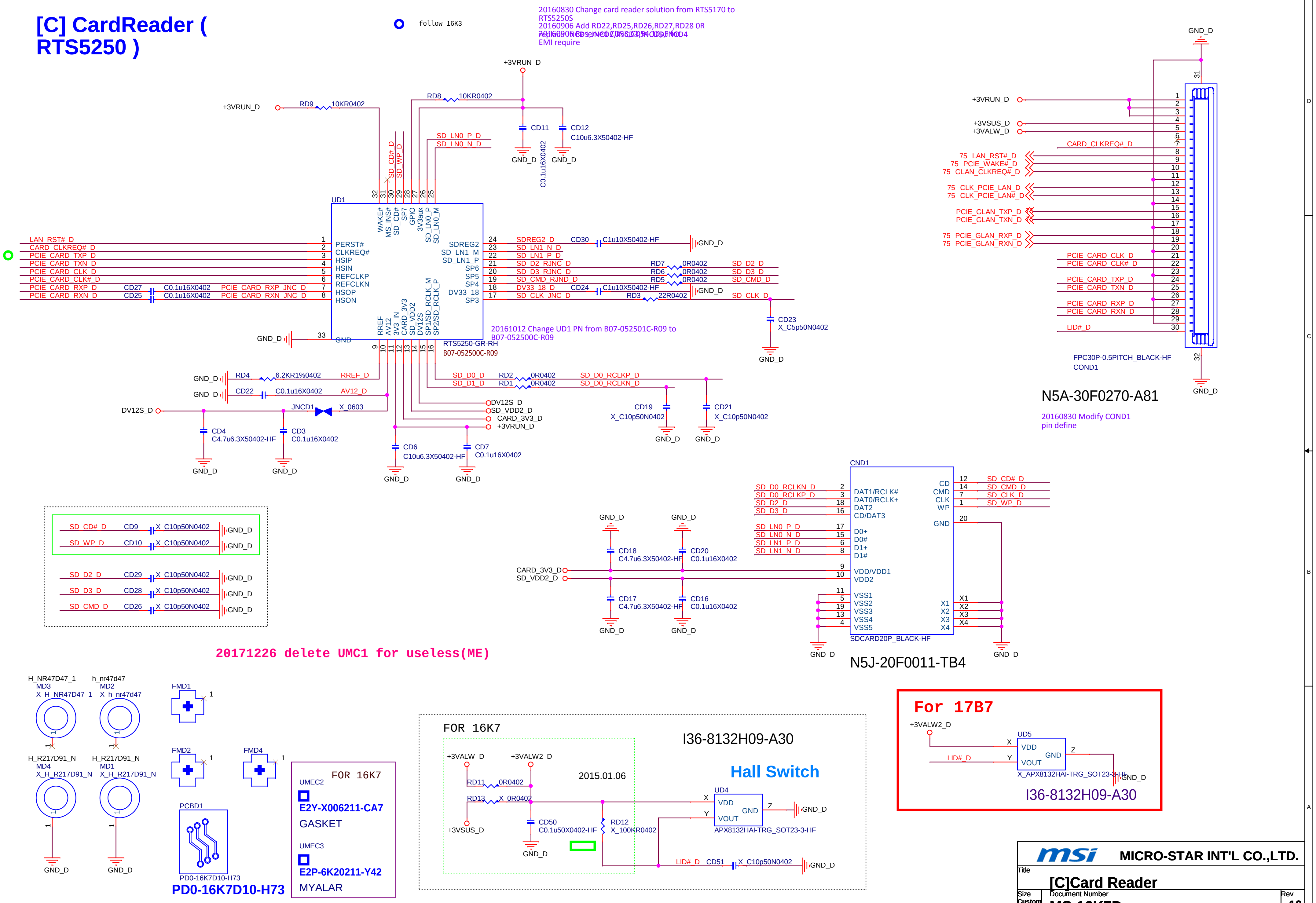
MICRO-STAR INT'L CO.,LTD.

Title: [C]LED control

Size: Document Number: MS-16K7C Rev: 1.0

Date: Sheet 73 of 80

[C] CardReader (RTS5250)

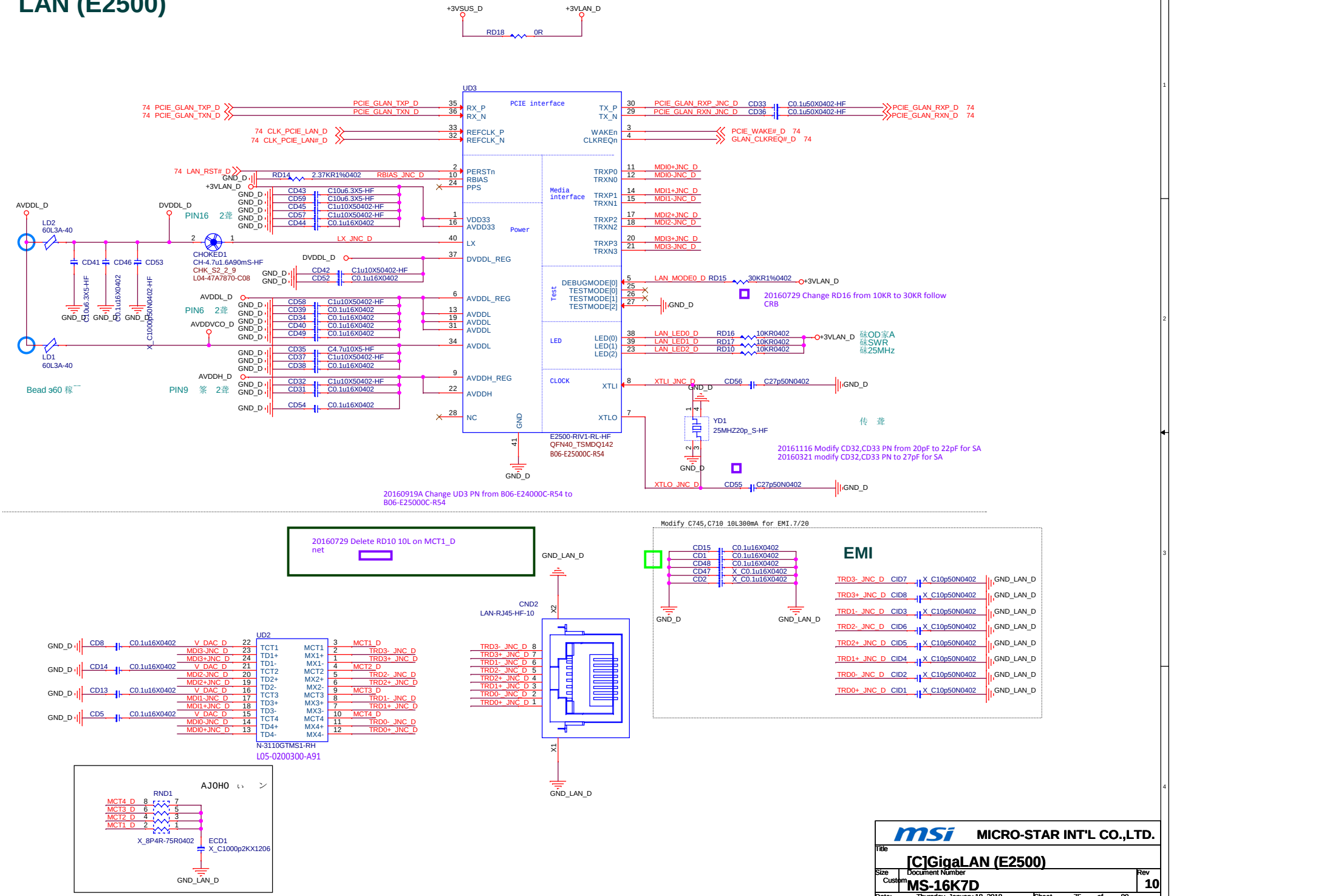


follow 16K3
20160830 Change card reader solution from RTS5170 to RTS5250S
20160906 Add RD22,RD25,RD26,RD27,RD28 0R
EMI require
+3VRUN_D
RD9 10KR0402
RD8 10KR0402
CD11
CD12 C10u6.3X50402-HF
C0.1u16X0402
GND_D
SD_LN0_P_D
SD_LN0_N_D
SD_CD#_D
SD_WP_D
UD1
PERST#
CLKREQ#
HSIP
HSIN
REFCLKP
REFCLKN
HSOP
HSON
GND
WAKE#
MS_INS#
SD_CD#
SP7
GPIO
3V3aux
SD_LN0_P
SD_LN0_M
SDREG2
SD_LN1_M
SD_LN1_P
SP6
SP5
SP4
DV33_18
SP3
REF
AV12
3V3_IN
CARD_3V3
SD_VDD2
DV12S
SP1/SD_RCLK_M
SP2/SD_RCLK_P
RTS5250-GR-RH
B07-052500C-R09
LAN_RST#_D
CARD_CLKREQ#_D
PCIE_CARD_TXP_D
PCIE_CARD_TXN_D
PCIE_CARD_CLK_D
PCIE_CARD_CLK#_D
PCIE_CARD_RXP_D
PCIE_CARD_RXN_D
CD27 C0.1u16X0402 PCIE_CARD_RXP_JNC_D
CD25 C0.1u16X0402 PCIE_CARD_RXN_JNC_D
SDREG2_D CD30 C1u10X50402-HF
SD_LN1_N_D
SD_LN1_P_D
SD_D2_RJNC_D RD7 0R0402 SD_D2_D
SD_D3_RJNC_D RD6 0R0402 SD_D3_D
SD_CMD_RJND_D RD5 0R0402 SD_CMD_D
DV33_18_D CD24 C1u10X50402-HF
SD_CLK_JNC_D RD3 22R0402 SD_CLK_D
CD23 X_C5p50N0402
20161012 Change UD1 PN from B07-052501C-R09 to B07-052500C-R09
RD4 6.2KR1%0402 RREF_D
CD22 C0.1u16X0402 AV12_D
DV12S_D
JNCD1 X_0603
CD4 C4.7u6.3X50402-HF
CD3 C0.1u16X0402
CD6 C10u6.3X50402-HF
CD7 C0.1u16X0402
SD_D0_D RD2 0R0402 SD_D0_RCLKP_D
SD_D1_D RD1 0R0402 SD_D0_RCLKN_D
DV12S_D
SD_VDD2_D
CARD_3V3_D
+3VRUN_D
CD19 X_C10p50N0402
CD21 X_C10p50N0402
+3VSUS_D
+3VALW_D
CARD_CLKREQ#_D
75 LAN_RST#_D
75 PCIE_WAKE#_D
75 GLAN_CLKREQ#_D
75 CLK_PCIE_LAN_D
75 CLK_PCIE_LAN#_D
PCIE_GLAN_TXP_D
PCIE_GLAN_TXN_D
75 PCIE_GLAN_RXP_D
75 PCIE_GLAN_RXN_D
PCIE_CARD_CLK_D
PCIE_CARD_CLK#_D
PCIE_CARD_TXP_D
PCIE_CARD_TXN_D
PCIE_CARD_RXP_D
PCIE_CARD_RXN_D
LID#_D
FPC30P-0.5PITCH_BLACK-HF
COND1
N5A-30F0270-A81
20160830 Modify COND1 pin define
CND1
SD_D0_RCLKN_D
SD_D0_RCLKP_D
SD_D2_D
SD_D3_D
SD_LN0_P_D
SD_LN0_N_D
SD_LN1_P_D
SD_LN1_N_D
DAT1/RCLK#
DAT0/RCLK+
DAT2
CD/DAT3
D0+
D0#
D1+
D1#
VDD/VDD1
VDD2
VSS1
VSS2
VSS3
VSS4
VSS5
CD
CMD
CLK
WP
GND
X1
X2
X3
X4
SD_CD#_D
SD_CMD_D
SD_CLK_D
SD_WP_D
SDCARD20P_BLACK-HF
N5J-20F0011-TB4
CARD_3V3_D
SD_VDD2_D
CD18 C4.7u6.3X50402-HF
CD20 C0.1u16X0402
CD17 C4.7u6.3X50402-HF
CD16 C0.1u16X0402
SD_CD#_D CD9 X_C10p50N0402
SD_WP_D CD10 X_C10p50N0402
SD_D2_D CD29 X_C10p50N0402
SD_D3_D CD28 X_C10p50N0402
SD_CMD_D CD26 X_C10p50N0402
20171226 delete UMC1 for useless(ME)
H_NR47D47_1 MD3 X_H_NR47D47_1
h_nr47d47 MD2 X_h_nr47d47
H_R217D91_N MD4 X_H_R217D91_N
H_R217D91_N MD1 X_H_R217D91_N
FMD1
FMD2
FMD4
PCBD1
PD0-16K7D10-H73
PD0-16K7D10-H73
FOR 16K7
UMEC2
E2Y-X006211-CA7
GASKET
UMEC3
E2P-6K20211-Y42
MYALAR
FOR 16K7
I36-8132H09-A30
Hall Switch
+3VALW_D
+3VALW2_D
2015.01.06
RD11 0R0402
RD13 X_0R0402
+3VSUS_D
CD50 C0.1u50X0402-HF
RD12 X_100KR0402
UD4
VDD
VOUT
GND
APX8132HAI-TRG_SOT23-3-HF
LID#_D CD51 X_C10p50N0402
For 17B7
+3VALW2_D
UD5
LID#_D
X_APX8132HAI-TRG_SOT23-3-HF
I36-8132H09-A30

MICRO-STAR INT'L CO.,LTD.

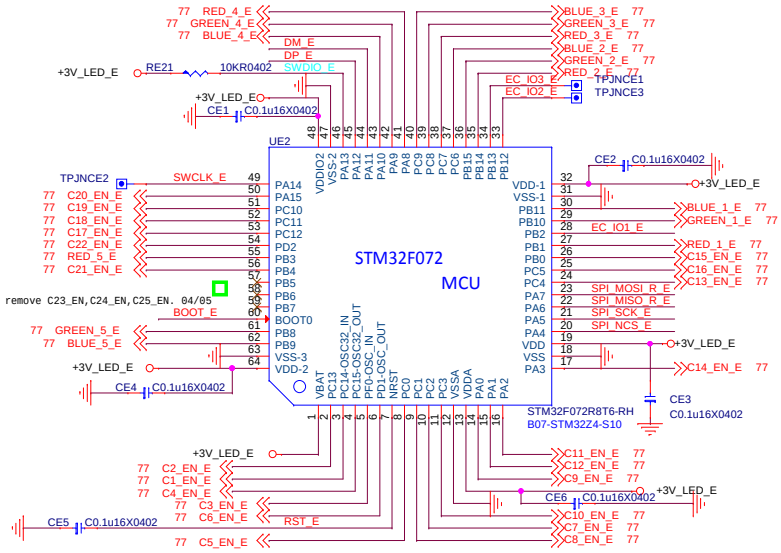
Title	[C]Card Reader	
Size: Custom	Document Number: MS-16K7D	Rev: 10
Date: Thursday, January 18, 2018	Sheet 74 of 80	

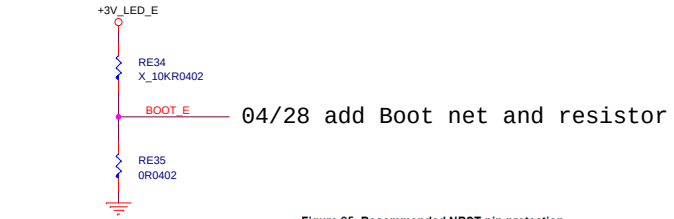
LAN (E2500)



Title	[C]GigaLAN (E2500)
Size	Custom
Document Number	MS-16K7D
Rev	10
Date:	Thursday, January 18, 2018
Sheet	75 of 80

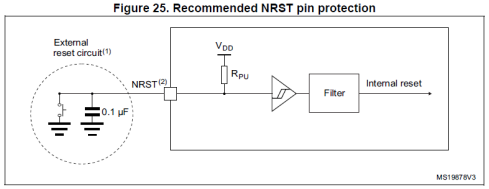
MICRO-STAR INT'L CO.,LTD.



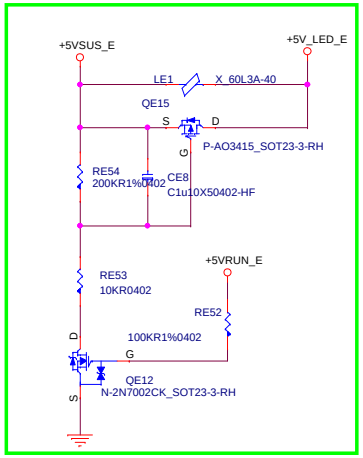


04/28 add Boot net and resistor

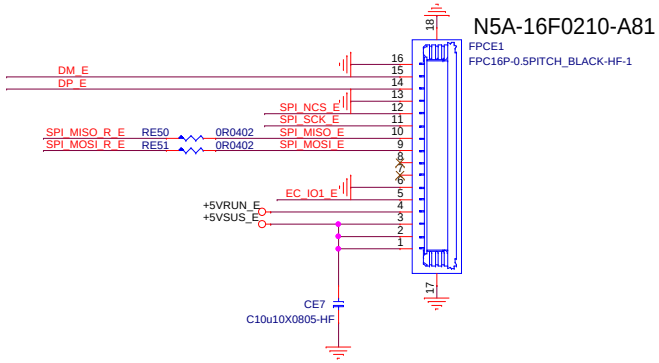
Figure 25. Recommended NRST pin protection



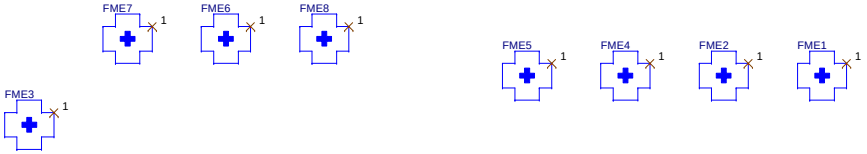
1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 56: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

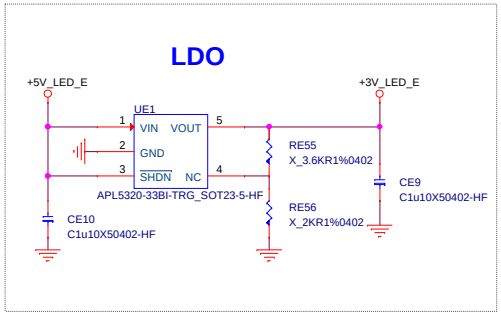


add Q25,PQ12 conrtrol . 04/05



Confirm Pin 1 position





MICRO-STAR INT'L CO.,LTD.

Title: [E]MCU/Matrix/Power

Size: | Document Number: MS-16K7E | Rev: 10

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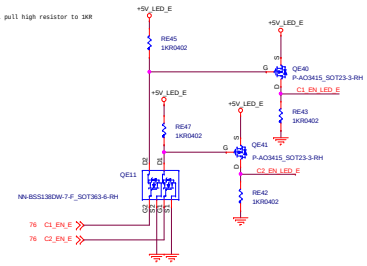
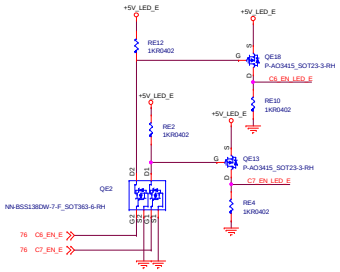
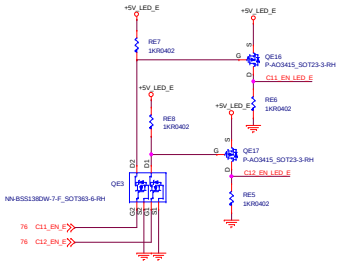
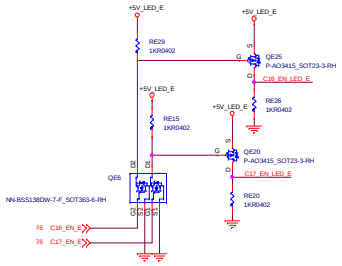
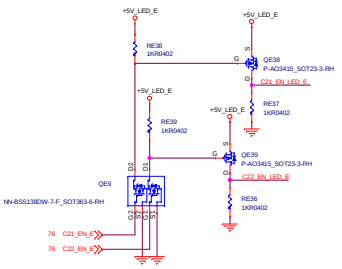
2016/12/01 modfiy all pull high resistor to 1KR

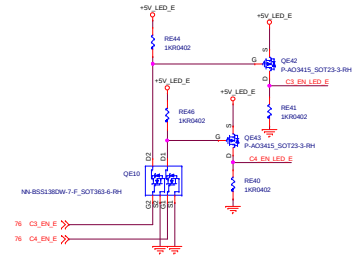


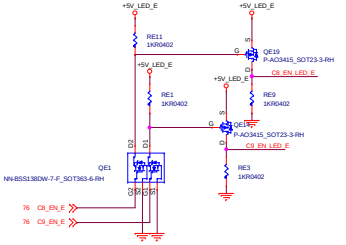


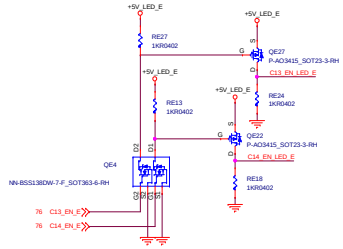


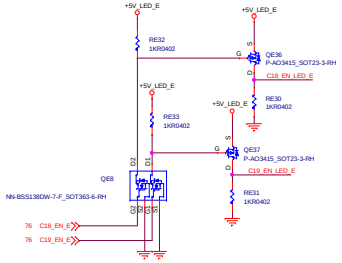


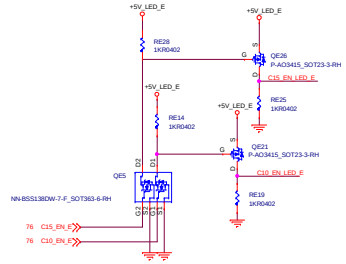


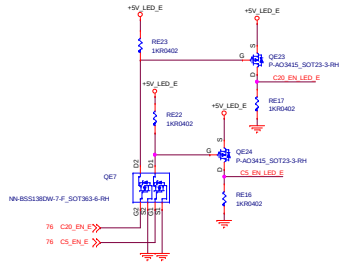






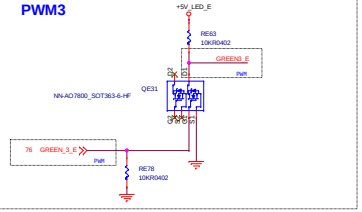




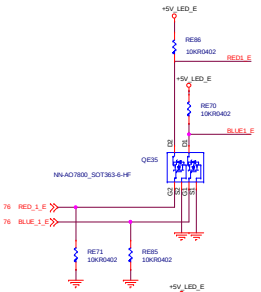


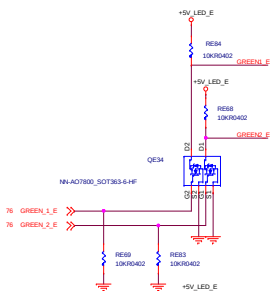
Change C5_EN control. 2017/4/14

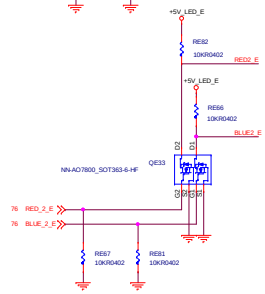
PWM3

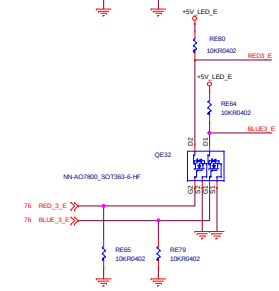


PWM1 PWM2 PWM3

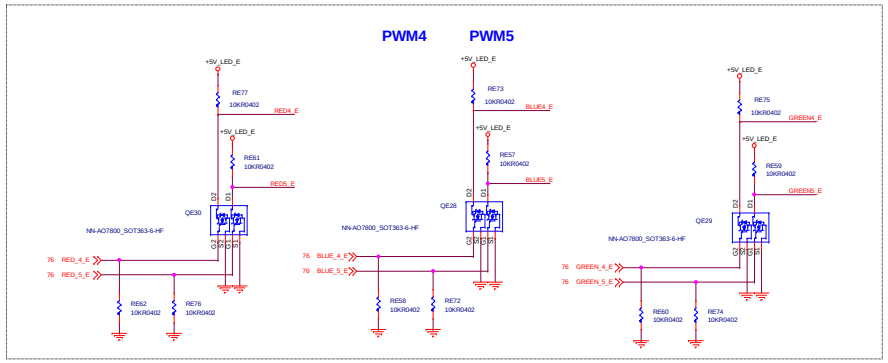








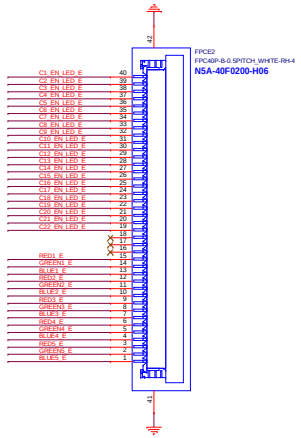
PWM4 PWM5



PCBE1

PD0-16K7E10-H73

PD0-16K7E10-H73



MICRO-STAR INT'L CO.,LTD.

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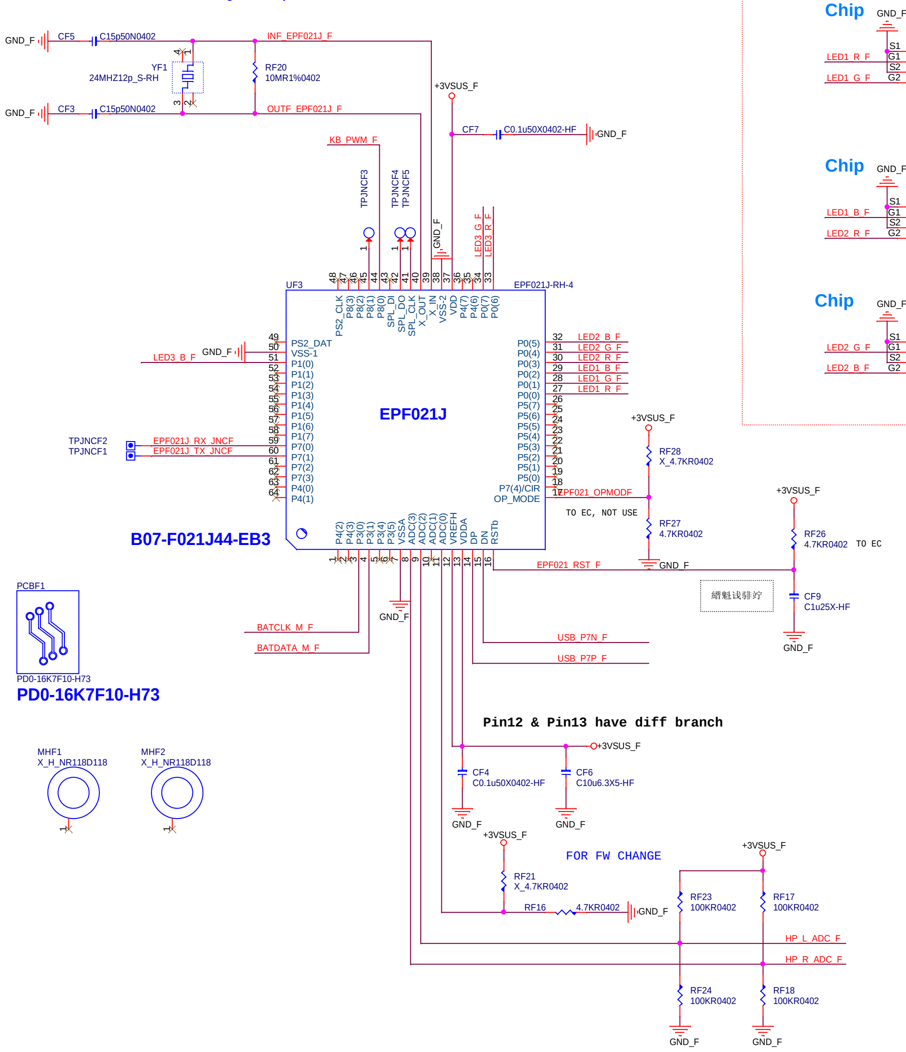
LED 8051 Controller

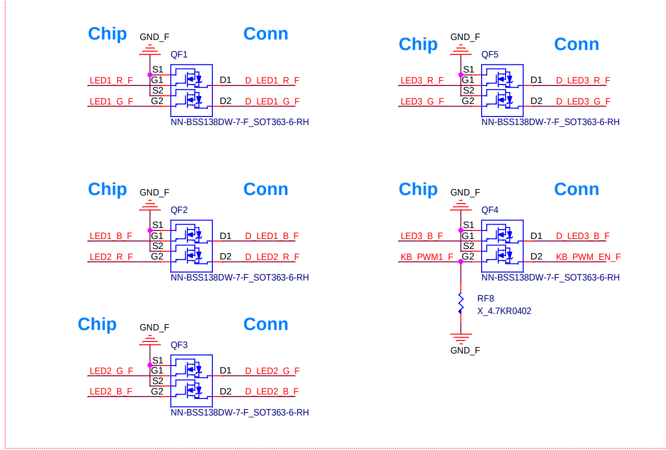
F PCB 8/21 稂糤

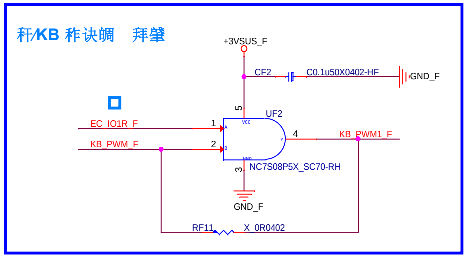
C749 and C750 change to 15pF for SA



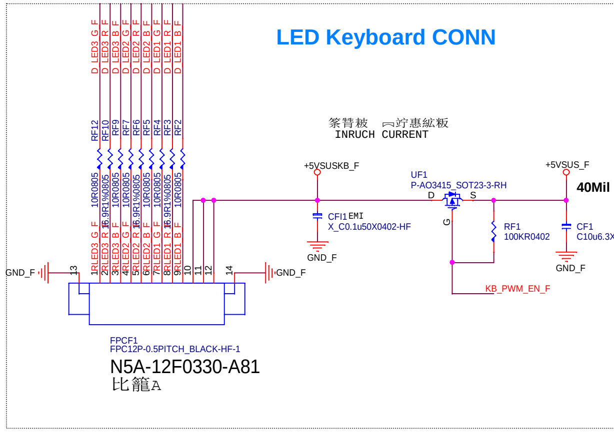
GND_F
CF5
C15p50N0402
INF_EPF021J_F
YF1
24MHZ12p_S-RH
RF20
10MR1%0402
CF3
C15p50N0402
OUTF_EPF021J_F
+3VSUS_F
CF7
C0.1u50X0402-HF
KB_PWM_F
TPJNCF3
TPJNCF4
TPJNCF5
UF3
EPF021J-RH-4
EPF021J
LED3_B_F
TPJNCF2
TPJNCF1
EPF021J_RX_JNCF
EPF021J_TX_JNCF
B07-F021J44-EB3
RF28
X_4.7KR0402
EPF021_OPMODF
TO EC, NOT USE
RF27
4.7KR0402
RF26
4.7KR0402
TO EC
EPF021_RST_F
CF9
C1u25X-HF
BATCLK_M_F
BATDATA_M_F
USB_P7N_F
USB_P7P_F
PCBF1
PD0-16K7F10-H73
PD0-16K7F10-H73
Pin12 & Pin13 have diff branch
CF4
C0.1u50X0402-HF
CF6
C10u6.3X5-HF
MHF1
X_H_NR118D118
MHF2
X_H_NR118D118
FOR FW CHANGE
RF21
X_4.7KR0402
RF16
4.7KR0402
RF23
100KR0402
RF17
100KR0402
HP_L_ADC_F
HP_R_ADC_F
RF24
100KR0402
RF18
100KR0402

EPF021J Sink current not enough, only using BSS138 (0.22A)

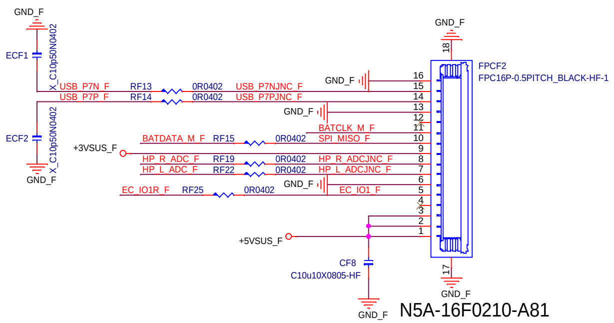




LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G



ECF1
X_C10p50N0402
USB_P7N_F
USB_P7P_F
RF13
RF14
0R0402
USB_P7NJNC_F
USB_P7PJNC_F
ECF2
BATDATA_M_F
RF15
BATCLK_M_F
SPI_MISO_F
HP_R_ADC_F
HP_L_ADC_F
RF19
RF22
HP_R_ADCJNC_F
HP_L_ADCJNC_F
EC_IO1R_F
RF25
EC_IO1_F
+5VSUS_F
CF8
C10u10X0805-HF
FPCF2
FPC16P-0.5PITCH_BLACK-HF-1
N5A-16F0210-A81

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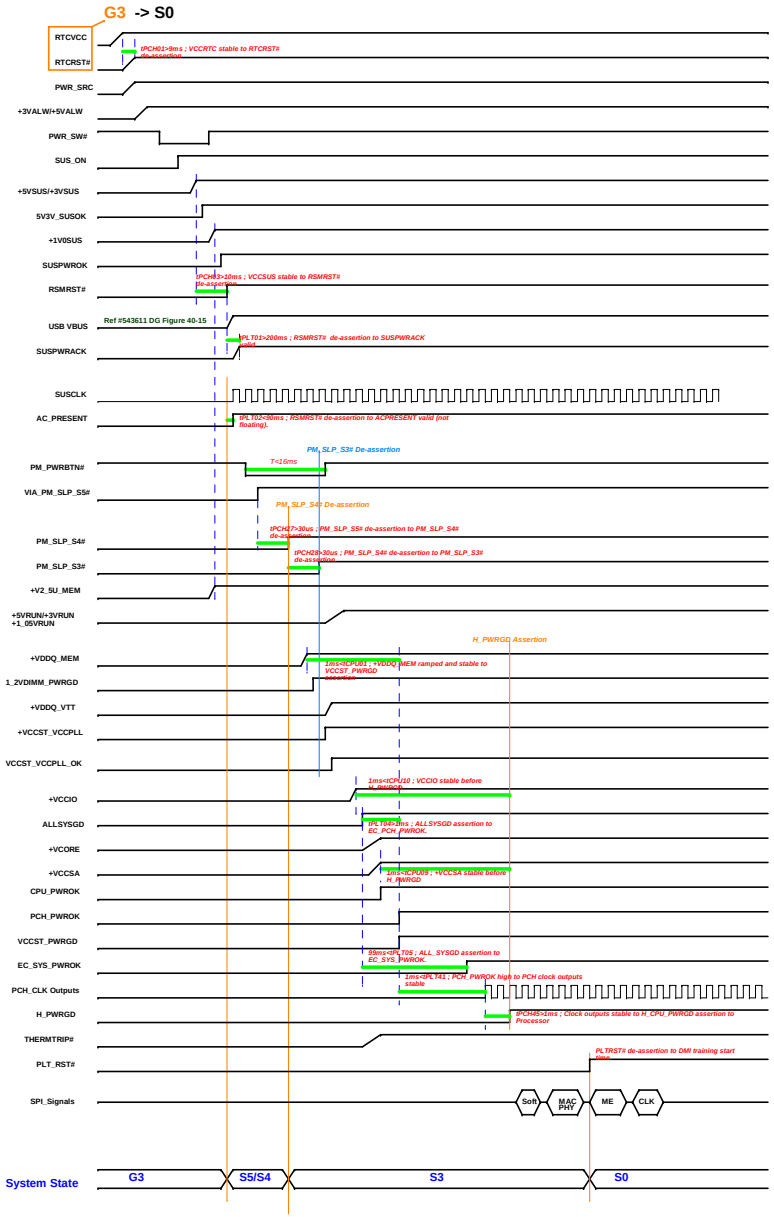
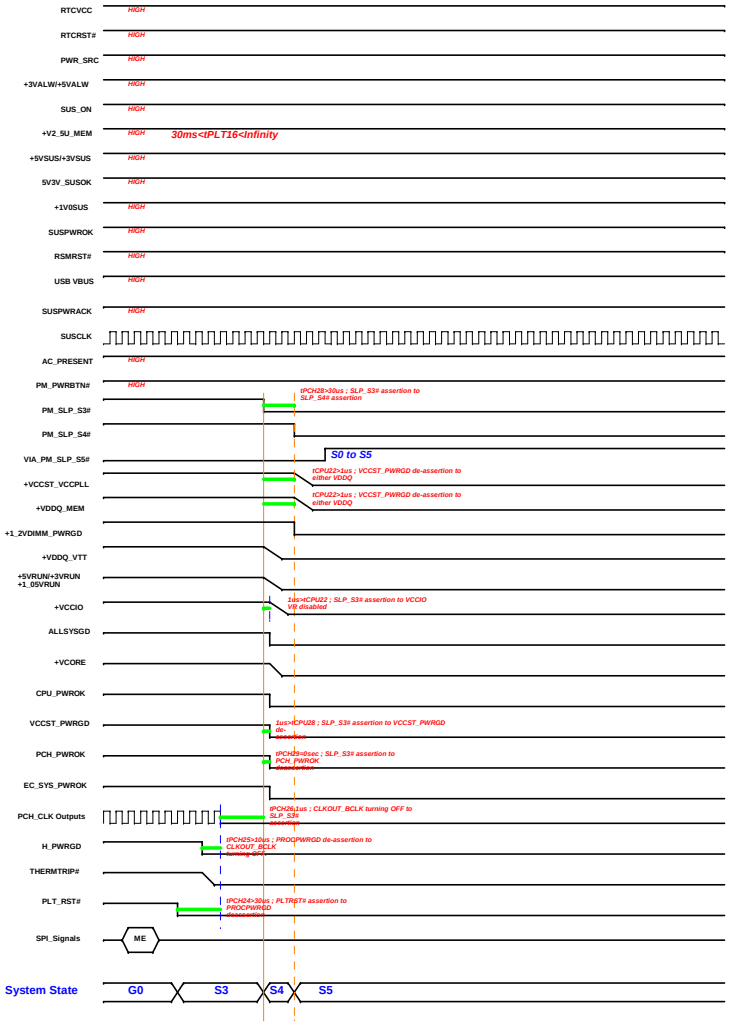
SKL-S DT Power ON Sequence G3 to S0

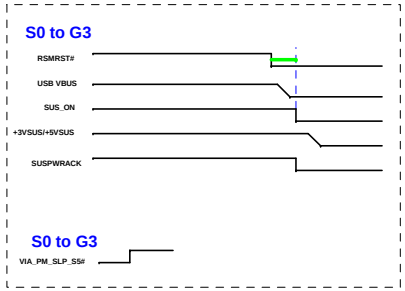
Ref #543611 Chapter40
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters



MS-1813 : SKL-S DT Power Down Sequence S0 to S5

Ref #543611 Chapter40
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters





msi MICRO-STAR INT'L CO.,LTD.

Title: Power on Sequence
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History

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DATE	PAGE	DESCRIPTION
20170714	ALL	first version from 16K5
20170731	ALL	modify all material data to follow CIS data
	3	Add CFG7 description
	37	change R2228 to R11-0103012-W08 but no stuff following CRB
	33	R2171=> DG request 620
	4	add description=> R27,R343,R344 need to close CPU
	5,36	change R2351 to 20R to follow DG change R2352 and R2353 to 30R to follow DG
	37	change R2226 unstuff to follow CRB
	7	change C45 to 0.1uF
	33	R2185=> change to 1.5K to follow DG
	57	correct PC84 and PC 89 value
	39	add test point for PCH pin AL37 to follow CRB suggestion
20170801	48	change R2248 to 33R to follow DG
	36	delete C8613 add C8988,C8989,C8990,C8991,C8992 to follow DG
	11~31	20170801A~20170801B change GPU design from 1060(16K5) to 1070(16K3)
20170803	3~8	CPU change to OAD-16P5002-I06
	47	delete R2437,R2438 and net PERP12,PERN12
20170804	7	For power sequence U39 change to I36-1533V0C-SF9 control by PM_SLP_S4# C404 change from 2200pF to 220pF
	40	add TP45
20170809	34,35	change PCIE port arrange for SATA SSD and HDD working correctlly Lan from port 13 to port 5 SATA HDD from port 14 to port 13
	55,73 74	In order to follow DG add C8993~C8996 and net PCIE_GLAN_TXP_C,PCIE_GLAN_TXN_C, PCIE_CARD_TXP_C,PCIE_CARD_TXN_C delete CD89~CD92 and net PCIE_CARD_TXP_JNC_D,PCIE_CARD_TXN_JNC_D, PCIE_GLAN_TXP_JNC_D,PCIE_GLAN_TXN_JNC_D
	36	U79 change from socket to ROM P/N M31-2512832-M24
20170814	39	add net name H_PROCHOT#_BUF
20170817	53	change R2394 stuff and R2397 unstuff for strap pin setting
	47	change R2255 and R2257 unstuff (OD pin and no use)
20170824	39,47 52	modify for 3 keyboard delete TP45 add R3518, R3519, R3520, R3521, R3522, R3523, R3524, R3525, C8997, C8998 add net EC_SPI_DO_R, EC_SPI_DO_R, EC_SPI_DI_R, HP_R_ADC, HP_L_ADC, HP_R_ADC_JNC, HP_L_ADC_JNC
	39,43	add R3526,R3527 for PD function
20170825	55~65	power modify power solution
	69	modify USB3.1 register value(refer to 16K5 SA results)
20170828	32	change R2175 to 200K to follow DG and CRB
	52	delete U98 for layout
20170829	39 62	add R3528 for AC_PRESENT PC184 change to C71-331033E-P01 delete PC262 delete PR871 and net VCCIO_EN_R delete PR38,PR41
20170830	32,39 42,43	modify for AR b-step, c-step chip and wake function change AR power from +3VRUN to +3VSUS R228,R232 change to 2.2K to follow CRB add R3529,R3530,R3531 add Q3032 to avoid leakage TBT_CLKREQ# change to pull up to +3VSUS reserve U3054,C8999,C9013
	40	change DP solution to DP1.2(B0B-751300C-T07)
20170831	36	add R3535 and R3536 for GCoff
20170902	35,32 53	add CLINK and power contrpl signals for WLAN to support vPro
20170904	32,39	reserve J42 for APS tools delete TP11,TPJNC56
20170906	53	delete C12,C125,C129,C131,C136.
20170907	32,39	change net name from RTC_CTL# to RTC_CTL
	35	add TP25~TP28 for BIOS debug
20170908	32	change Q27 from D03-65D8L09-D07 to D03-07002F9-N47
	53	R64 change to C1225C11-2212813-W08
	40	C171 change from C11-2212813-W08 to C11-2211042-W08
20170911	32,35 37,53	change net GC6_FB_EN and DGPU_PWRGD to group B change VCCPGPPD from 3.3V to 1.8V(SUS) delete U9 and U10 delete R503 and R507
	38	Delete TP22 to follow CRB 0.9
	33,34	change PCIE port for 2 PCH LAN from PCIE5 to PCIE13 HDD from PCIE13 to PCIE17 AR from PCIE17~20 to PCIE21~24 WLAN from PCIE21 to PCIE14 Cardreader from PCIE23 to PCIE20
	36,39	delete TP4 and GPP_A13 add net SUSPWRACK delete R285 and ECESPI_RST#_R and ECESPI_RST#

DATE	PAGE	DESCRIPTION
20170912	32	change R95 and R96 stuff and D2 change to unstuff
	9,10 62	change C872,C922,PC180 from C71-331033E-P01 to C71-33102AE-P01
20170913	7	add R604 to follow DG
	32,36	change TBT_CIO_PLUG_EVENT# and TBT_FORCE_PWR_R from GPIO K to H
	36,39	add R285,R605 and net ECESPI_RST#, ECESPI_RST#_R
	43	U57 pin A11,B11,C11,D11,H10 change to connect with +5VSUS
	48,51	Delete TP14 add R606,R607 and net I2S_CT1_MCLK,I2S_CT1_MCLKR
	53	add R608~R611 add net CNVI_BRI_RSP_R,CNVI_RGI_DT_R,CNVI_RGI_RSP_R,CNVI_BRI_DT_R
	62	PC175 change to unstuff reserve PR269 for CPU_C10_GATE#
	5657 58	modify SUS power sequence control
	64	power change PQ6,PQ7 to D03-906DT00-V02
20170915	67	delete MGPU3 and MGPU4 add XX17~XX26 (Hole)(footprint=>H_NR118D118) change Hole name MH1=>XX1,MH2=>XX2,MH15=>XX15,MH16=>XX16
	ALL	update CFG for pre-BOM
	59,61	power fine tune device value PC189劤390pF C11-3911812-W08 PC172劤1500pF C11-1522812-W08 PC40劤0.033uF C11-3332512-Y01 PC205 stuff 330uF PR35劤2.21K R11-2211T22-W08 PR170劤63.4K R11-6342T12-W08 PR168劤41.2K R11-4122T12-W08 PR198劤53.6K R11-5362T12-W08 PR172劤115K R11-1153T12-W08 PR193劤511R R11-5110T12-W08 PR45劤64.9K R11-6492T12-W08
20170918	40	delete R166,R197 delete net GPUDPE_HPD_Q
	70	modify USB3.1 RX R location by Ti suggestion(RA2,RA3,RA4,RA5,RA6,RA7)
	53	correct C1225 mark
20170919	40	Q29 and Q30 change to connect with CPUDPD_SCL and CPUDPD_SDA
	42	R461 change to connect with TBT_CLKREQ#_R
	41	delete Q3,R98,R84, net LID2# U7 change to connect with +3VALW
	32,36	change TBT_CIO_PLUG_EVENT# and TBT_FORCE_PWR_R to PCH group K by BIOS request
	53	R444 and Q28 unstuff,R441 stuff
	64	net SW_DDR connect with PQ6,PQ7
	36	add net GPP_K10
	44	delete D4
	52	correct Q32
20170920	39	delete Q21,R318,R320
	37	add R612 for +3VSUS
	53	add U9,U10,C127,C128,R613,R614
	32	reserve R615 for power sequence
20170921	73	ME request change CND2 to N55-08F0851-AF2
	32	delete R615 and add C1226 for power sequence
	44	add LI7 for HDMI
20170922	32	add U60, R615,C1227 for power sequence add R616 for 24MHz XTAL operation
20170925	35	delete TP7 Add R617 and R618 for vPro
	36	R292 change to stuff
	32	Add R619,R620,R621,R622
	58	Add PR270
	57	change net name DIMM_ON to DIMM_ON_2V5 to control +2.5V_MEM
20170926	37	change R482 to L9 change R494 to L10 add C1228 C1075 change C11-1057412-Y01 to C11-2267413-M09
	67,72	delete FMD3,FM20,FM22,FM42,FM44 Add XX27
20170927	37	delete FM3,FM15,FM24,FM36,FMB1
	44	add net HDMI_CLKP_C and HDMI_CLKN_C
	ALL	All footprint FILTER_S4_1_2X1 need to change to FILTER_S4_1_25X1
20170928	39,45	CH15,SW1 change footprint to SWTA_S6_5_2X6_3_T for CFM
20170929	55	delete +VBATA_1
	72~75	modify PCB name MS-16K7D KB LED control Board change to Card reader board MS-16K7C Card Reader board change to Per Key LED control board
20170929	39,53	delete BT_PWR_ON and EC9 add R623,R624 and net MB_ID
	36,39	change net name from SUSPWRACK to SUSPWRDNACK
20171005	72,76	delete ECC1,ECC2,ECE1,ECE2,RC1,RC2,RE48,RE49 for modify USB2.0 signal layout
	61	PL7 change from L04-24B7010-C36 to L04-24B7020-M26
	64,65	CHOKE1~CHOKE4 change from L04-22B7500-C36 to L04-22B7510-M26
	27	U29 change from M31-25Q8043-W03 to M31-25U8002-M24
	48	U50 change from OI9-CT53001 to I9C-5302S0C-CL9
20171013	32,59	C1226 change to C11-1057412-Y01 PR173 change to R11-1583T12-W08 R622 change to stuff,R621 change to unstuff for modify sequence
	35	R410,R411 change to unstuff R74,R75 change to 2.2K
	39	add MB_ID descrption
	45	modify con setting for 16K7/17B7
	46	make TPM partition unstuff
	47,49 50	modify config for 16K7/17B7
	52	modify KB connector config for 16K7/17B7
	59	power modify R value PR198=>R11-7872T12-W08 PR204=>R11-7680T12-W08 PR206=>R11-4991T12-W08 PR207=>R11-4991T12-W08
	67	delete UME7

DATE	PAGE	DESCRIPTION
20171016	52	correct C1097 CFG
20171018	47	U16 change from B05-012201C-R09 to B05-012203C-R09
20171025	32	C1226 change to 5010
	47,49	U16 change from B05-012203C-R09 to B05-012204C-R09
	50	change AMP and connector CFG setting for ME
20171027	73,77	QC1~QC7,QC20,QE28~QE35 change to use D03-0780009-A68 for circuit design
20171030	67	UME5 change PN from 307-6K30111-HG0 to 307-6K70111-HG0
20171108	67	add UME13 for EMPASS
	56	change PR96,PR103 to R11-0473T12-W08 change PL14 to L04-15A7700-M26
	64	change PR16 to R11-0153T12-W08
	59	change PR198 to R11-6042T12-W08 change PR193 to R11-5230T12-W08 change PC40 to unstuff
	58	change PC62 to unstuff
20171215	9,10	C970,C1059 change to stuff for SA
	63	PD1 change from D01-BAS4000-P15 to D01-RB55120-R06 for foward Voltage(<0.4V)
	57	PQ25,PQ32,PQ33 change from D03-7002W19-D07 to D03-7002KC9-P15 for ESD protect

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DATE	PAGE	DESCRIPTION
20171220	32,39	add EC_ALLSYSPG for modify sequence
	41	change U18 Vin to +3VSUS for panel sequence reserve R625 for Panel power off blinking issue
	51	add R626,R627, net OUTL_R_E and OUTR_R_E reserve R628
	54	change FPC2 to 32pin and modify FPC7 pin define for new design (Audio issue and USB3.1 solution change)
	68,69, 70	change FPC pin define and USB3.1 solution (Audio issue and USB3.1 solution change)
20171222	32	add EC_ALLSYSPG and reserve R629 for modify sequence
	49	reserve R630
	67	Add UME24~UME31 for 17B7 memory only UME21~UME23 stuff only for 16K7
	74	UMEC2,UMEC3 only stuff for 16K7
	3~8	CPU P/N update to OAD-16K5003-I06
	32~38	PCH P/N update to OB1-16K5002-I06
	42	AR P/N update to B07-L634015-I06
	41	reserve R631 for Panel power off blinking issue
20171226	74	delete UMC1 for useless(ME)
	67	delete UME21~UME23 for useless(ME) add UME33~UME40(ME) delete UME3,UME4,UME6,UME8(ME)
	72	add UMEC5,UMEC6(ME)
20171227	44	change R270 and R286 stuff for SA change R289 to 5.9K(R11-0592T12-W08) for SA
	46	delete TPJNC24 and TPJNC25 add R632 and R633 for SA
20171228	72,73	change C board Part reference to follow 16K5 for layout modify
20180104	41,49, 54,68	update 5010/5020 for C1229,R630,R631,RA18
20180104	35	change R74,R75 to R11-4990T12-R01
20180110	ALL	correct PCB P/N and description
	51	R239 change to 10K for HP_SEL HIGH LEVEL low voltage R626,R627 change to 20R for Headphone pop noise when system turn off and decrease cross-talk
	49,50	R252 change to 61.6K for woofer gain modification(too big) change smart Amp connect with PWR_SRC
	67	add UME41(17B7 ME)
20180111	ALL	create new CFG setting for BOM
20180112	32,59	for modify sequence R615,R620 change to stuff R619,C1226,U60 change to unstuff PR173 change to 10K
20180115	65	Change PC114 to stuff and change PR133 to 649 ohm for GPU sequence
	ALL	delete useless CFG setting

16K7 10 (GS combine with WS)

DATE	PAGE	DESCRIPTION
20180115	ALL	add CFG for WS
20180116	46	correct TPM P/N B0C-09665A2-I14
	ALL	add CFG without CPU
20180118	12~16	modify vram config for N18E-Q1-KB

DATE	PAGE	DESCRIPTION

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