MS-AC71 Ver: 1.1

Intel -SugarBay plamform

CPU:

INTEL-Sandy bridge LGA1155

System Chipset:

INTEL-Cougar Point

OnBoard Chipset:

HD Audio Codec:ALC887

LAN-RTL8111E

SIO:Fintek F171808A

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3+1Phase

Other:

SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

MICRO-STAR INT'L CO.,LTD

MS-AC71

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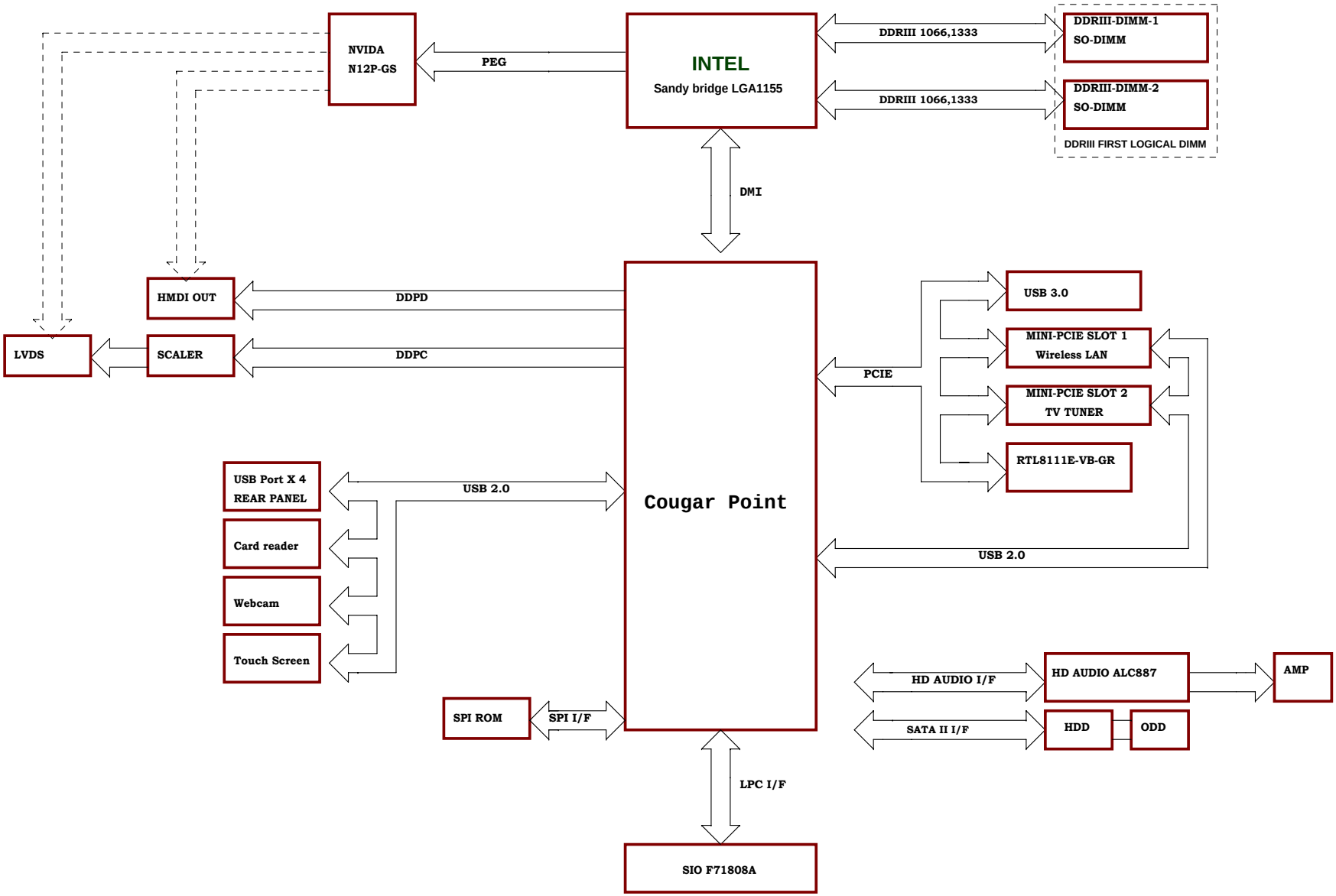
MS-AC71 (MS-AC711)



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-AC71	
Size: Custom	Document Description: Block Diagram	Rev: 1.1
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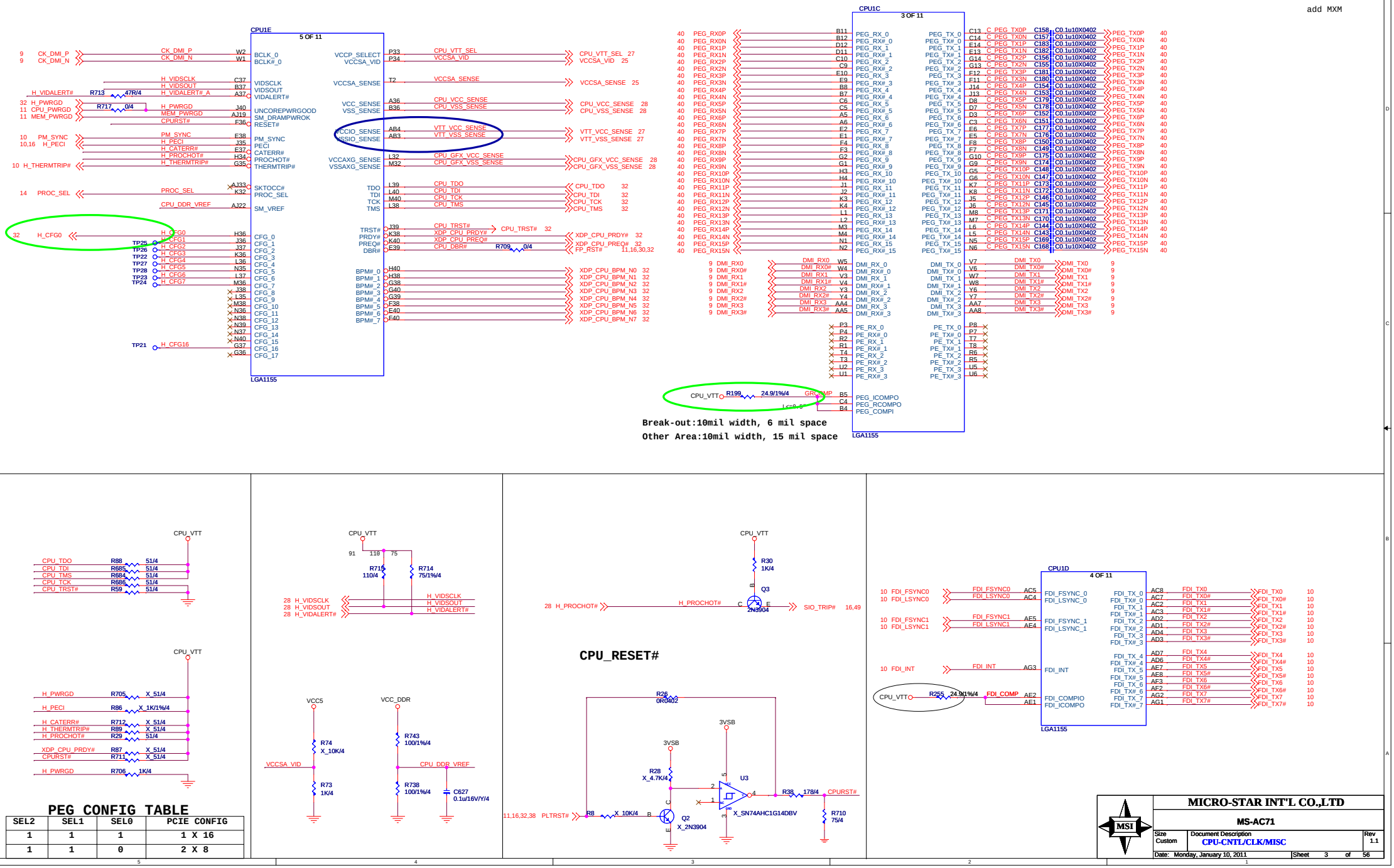
add MXM
CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
Break-out:10mil width, 6 mil space
Other Area:10mil width, 15 mil space
CPU_RESET#
CPU1D
4 OF 11
LGA1155
PEG CONFIG TABLE
SEL2 SEL1 SEL0 PCIE CONFIG
1 1 1 1 X 16
1 1 0 2 X 8
MICRO-STAR INT'L CO.,LTD
MS-AC71
CPU-CNTL/CLK/MISC
Rev 1.1
Monday, January 10, 2011
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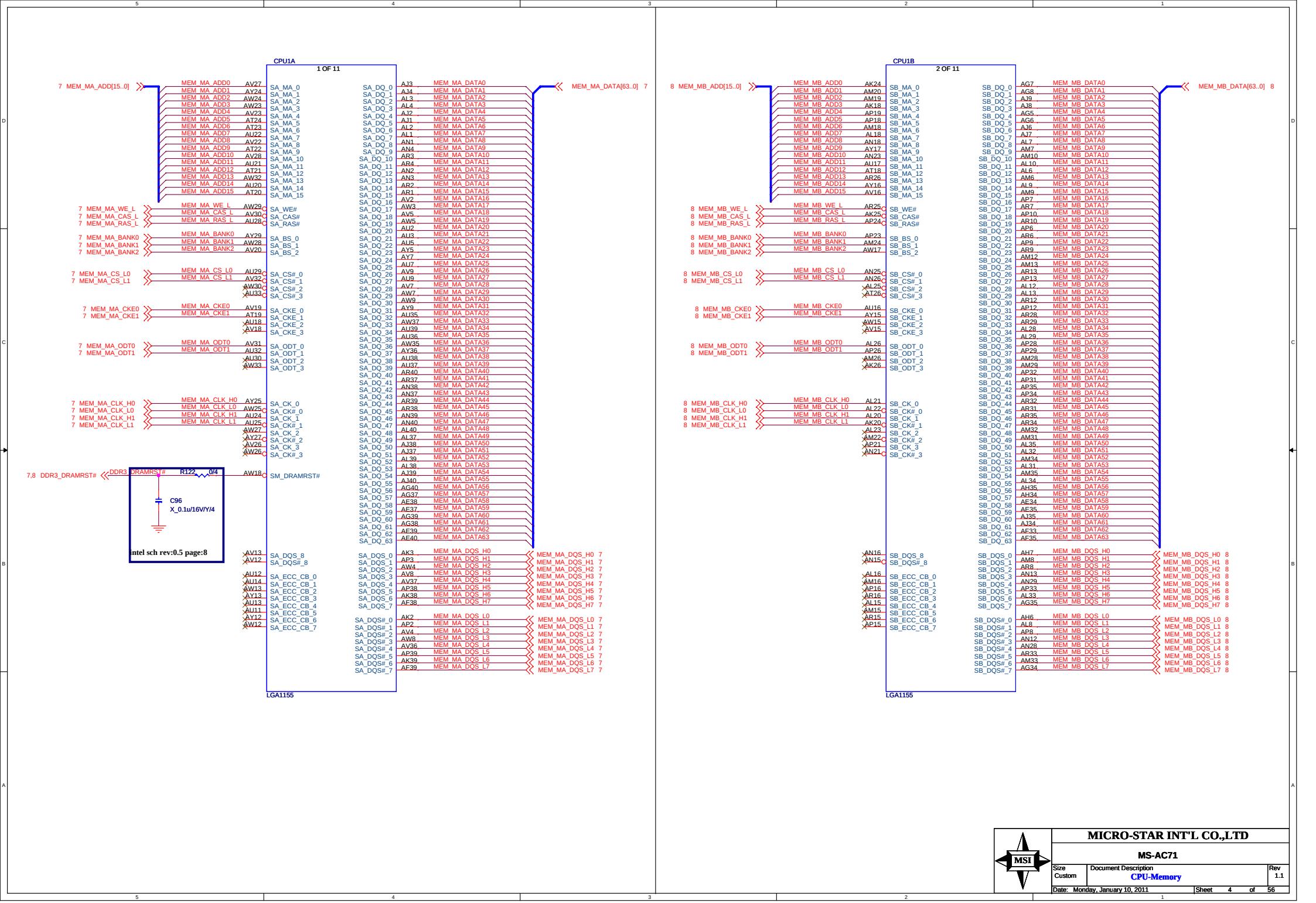

MICRO-STAR INT'L CO.,LTD

MS-AC71

Size	Document Description	Rev
Custom	CPU-Memory	1.1

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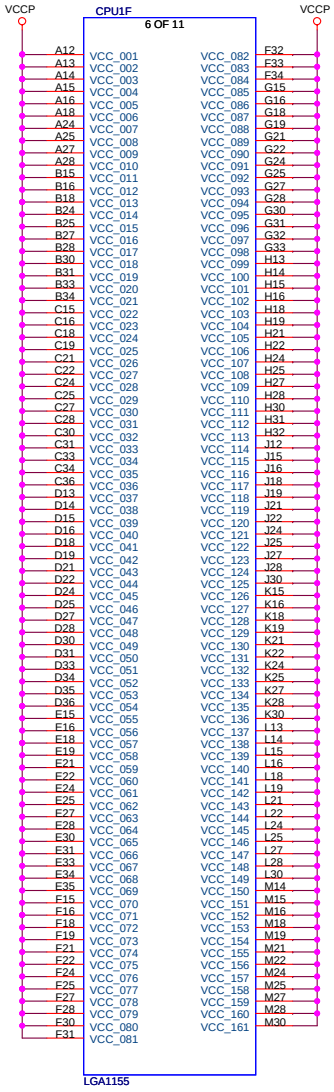
PROCESSOR VDDQ:4.75A

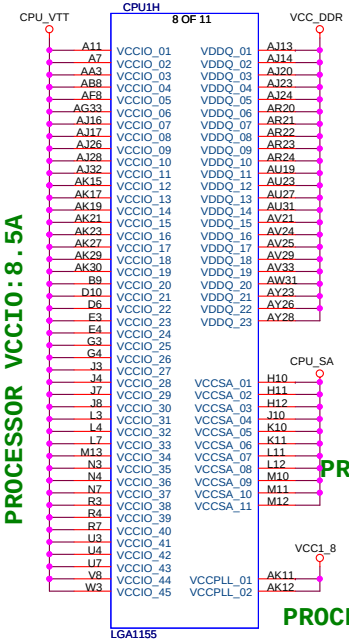
PROCESSOR VAXG:35A

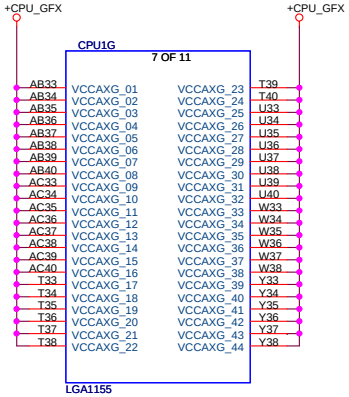
PROCESSOR VCCIO:8.5A

PROCESSOR VCCSA:8.8A

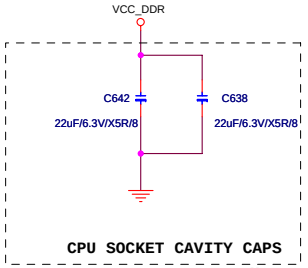
PROCESSOR VCCPLL:1.5A



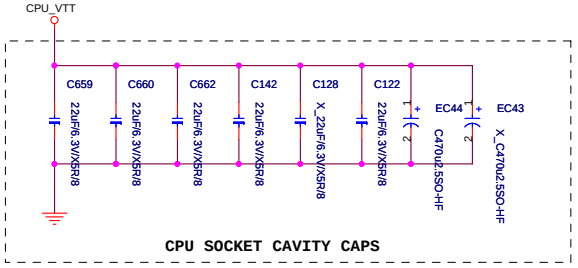


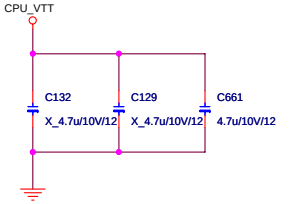


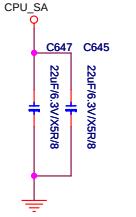
+1.5V_DDR3-Decoupling

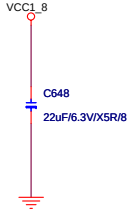


+CPU_VTT Decoupling









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MS-AC71		
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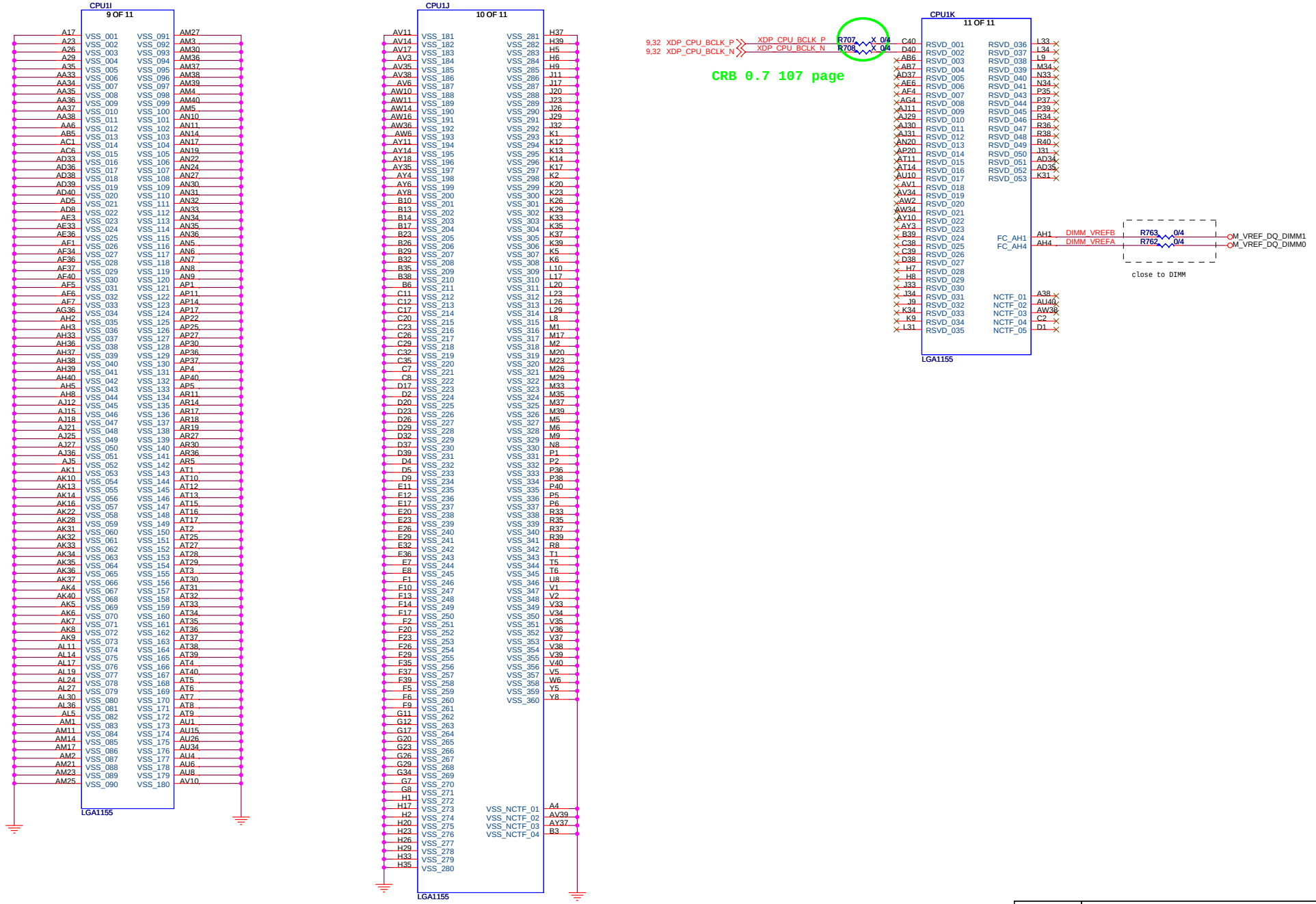

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MS-AC71	
Size: Custom	Document Description: CPU-GND
Rev: 1.1	
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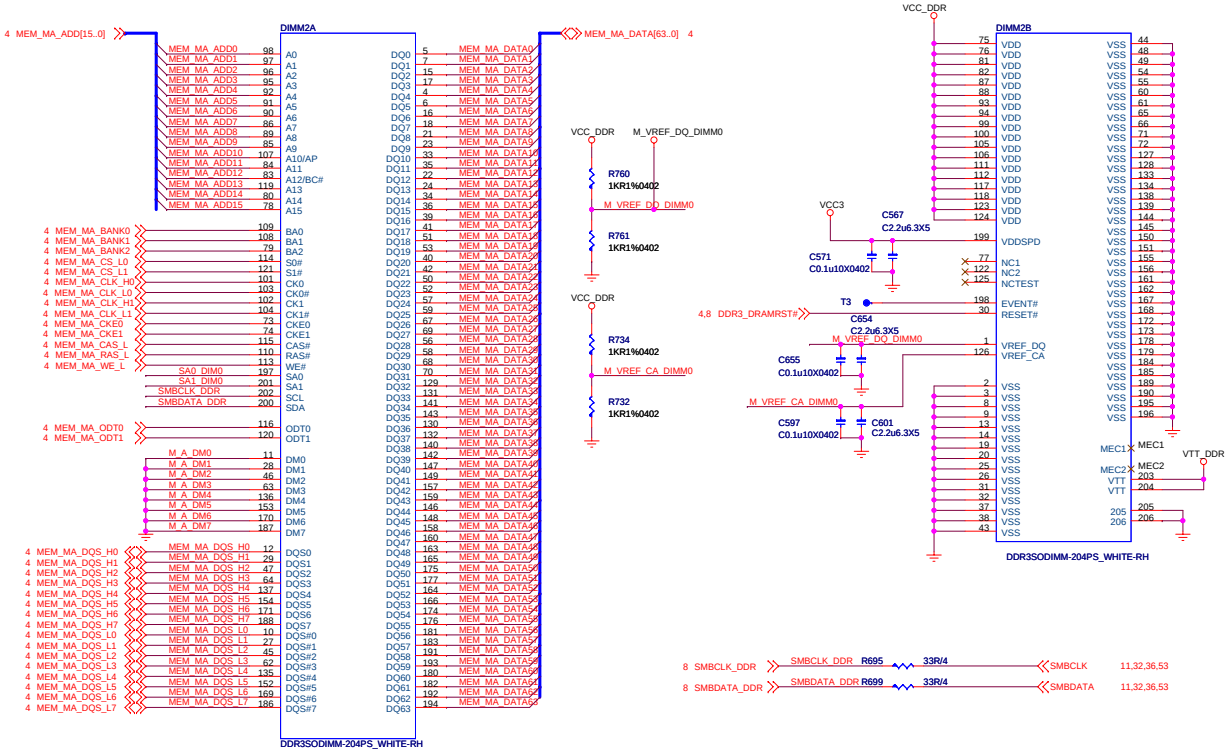
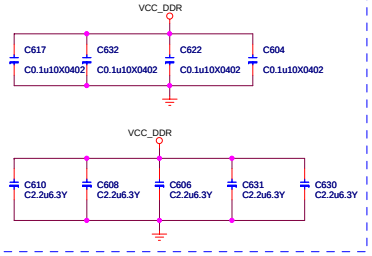
SODIMM#A



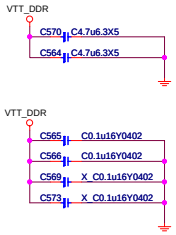
ADDRESS: 000
0xA0

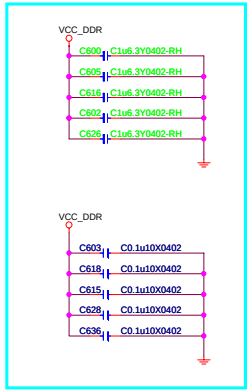
H=11mm

Layout note: Place capacitors between and near DDR connector if possible.



CHANNEL A V_SM_VTT DECOULPING CAPS





MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: C	Document Description: DDR III SODIMM 1	Rev: 1.1
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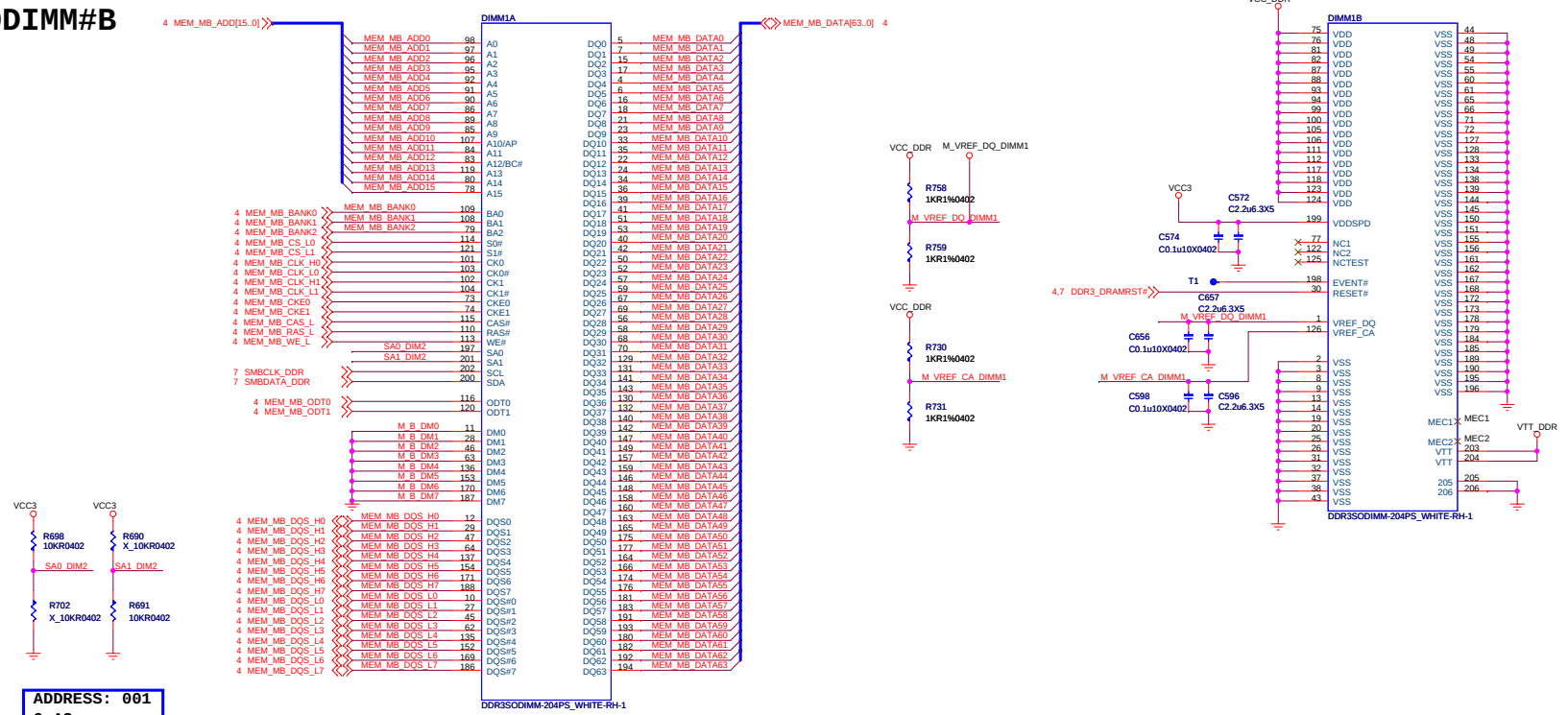
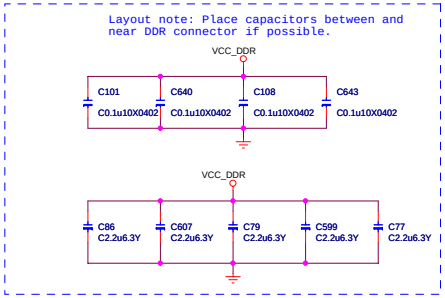
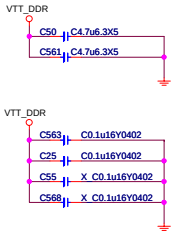
SODIMM#B

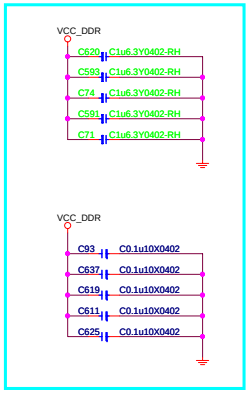


H=11mm



CHANNEL A V_SM_VTT DECOUPLING CAPS





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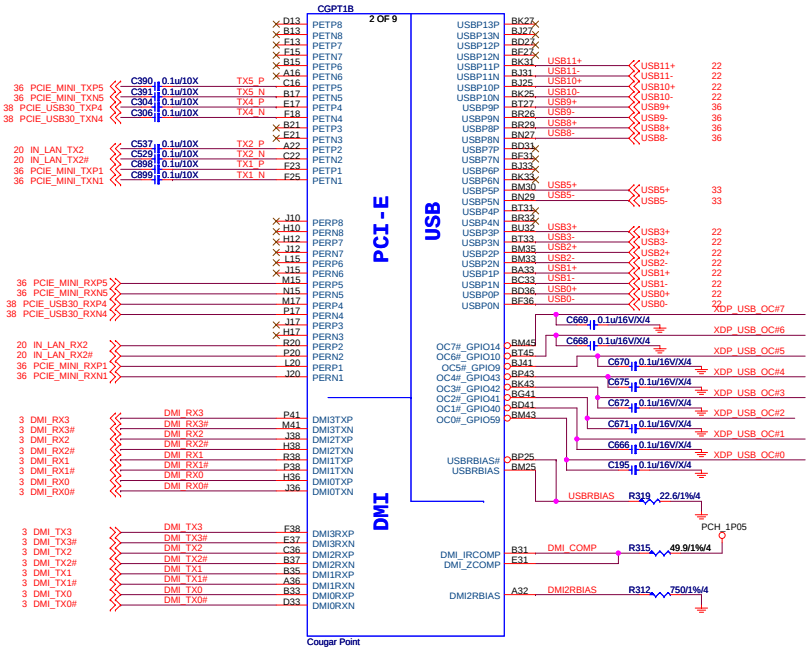
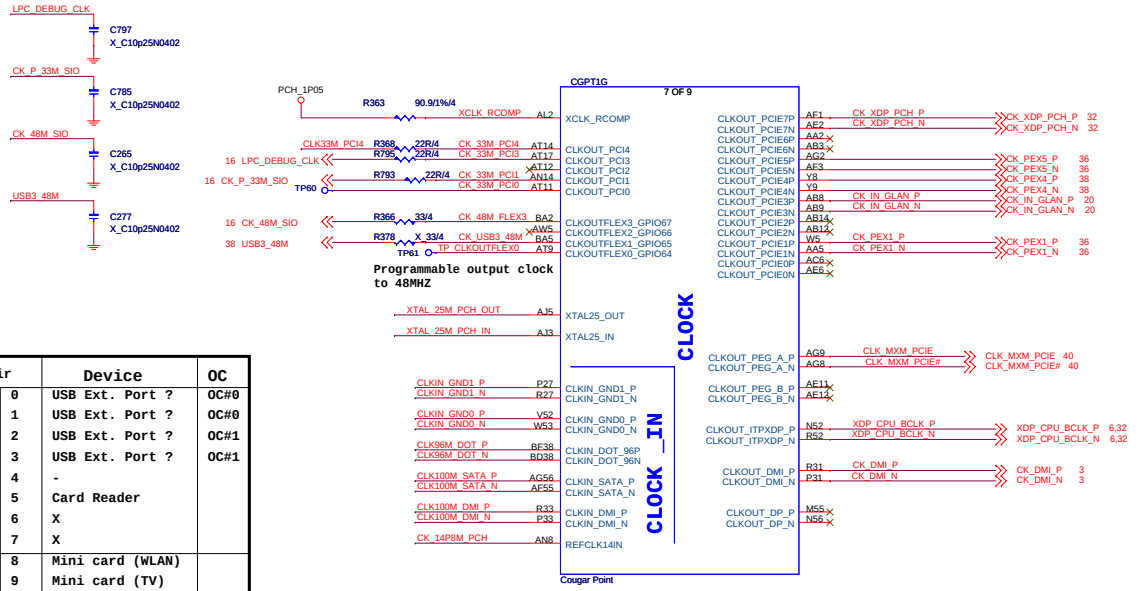
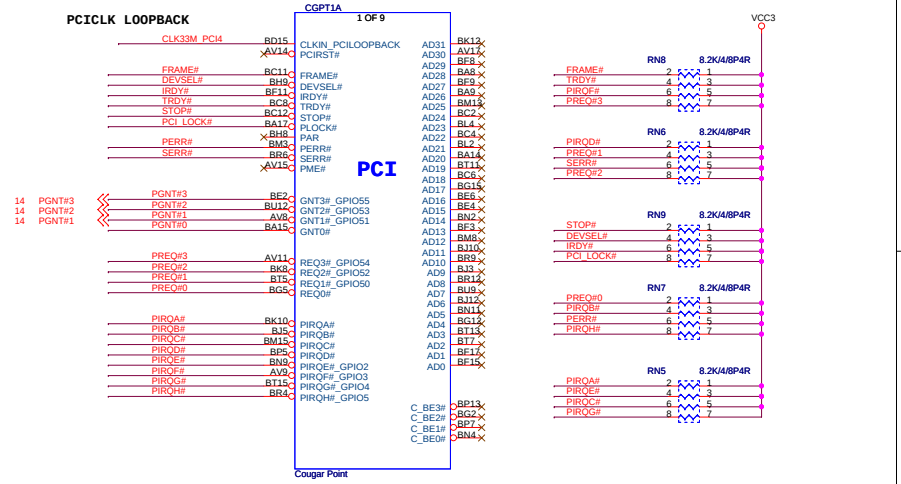
MS-AC71		
Size: C	Document Description: DDR III SODIMM 2	Rev: 1.1
Date: Monday, January 10, 2011	Sheet 8 of 56	

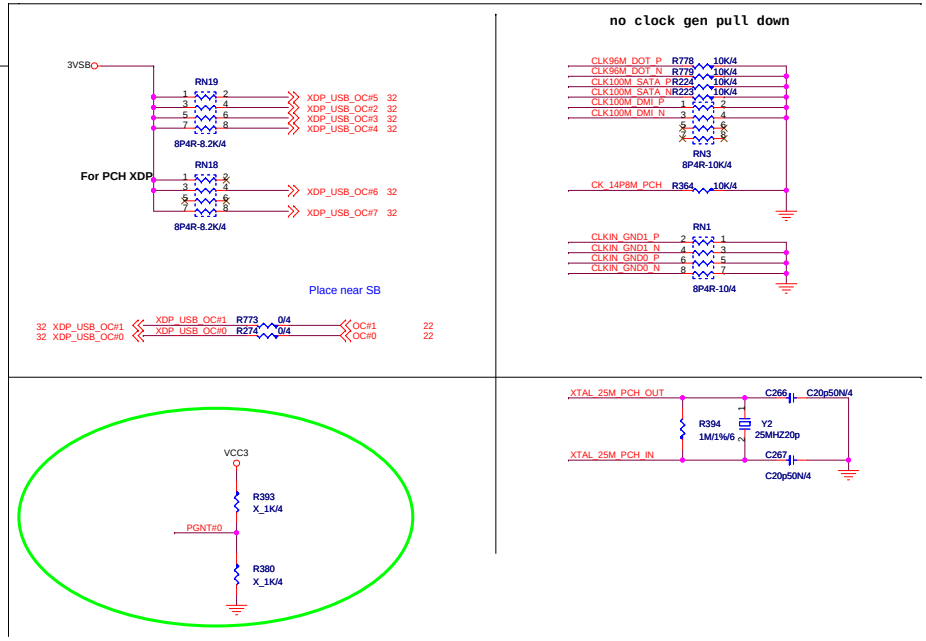
H61 SKU:PCIe ports 7 and 8 are disabled.
H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



Pair		Device	OC
EHCI#1	0	USB Ext. Port ?	OC#0
	1	USB Ext. Port ?	OC#0
	2	USB Ext. Port ?	OC#1
	3	USB Ext. Port ?	OC#1
	4	-	
	5	Card Reader	
	6	X	
	7	X	
EHCI#2	8	Mini card (WLAN)	
	9	Mini card (TV)	
	10	Webcam	
	11	Touch Screen	
	12	X	
	13	X	







MSI	MICRO-STAR INT'L CO.,LTD		
	MS-AC71		
Size: C	Document Description: CP PCI/E/DMI/USB/CLK		Rev: 1.1
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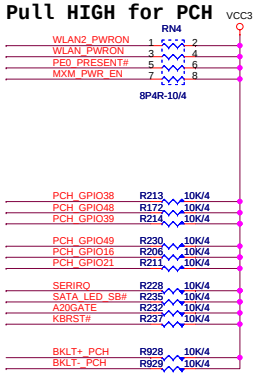
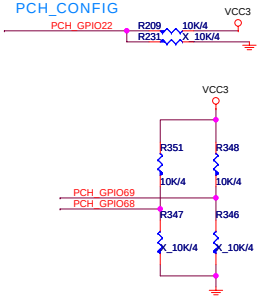
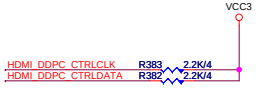
H61 SKU:SATA ports 2 and 3 are disabled.







MICRO-STAR INT'L CO.,LTD	
MS-AC71	
Size: Custom	Document Description: CP SATA/HOST/FAN/GPIO/VGA
Rev: 1.1	
Date: Monday, January 10, 2011	Sheet 10 of 56

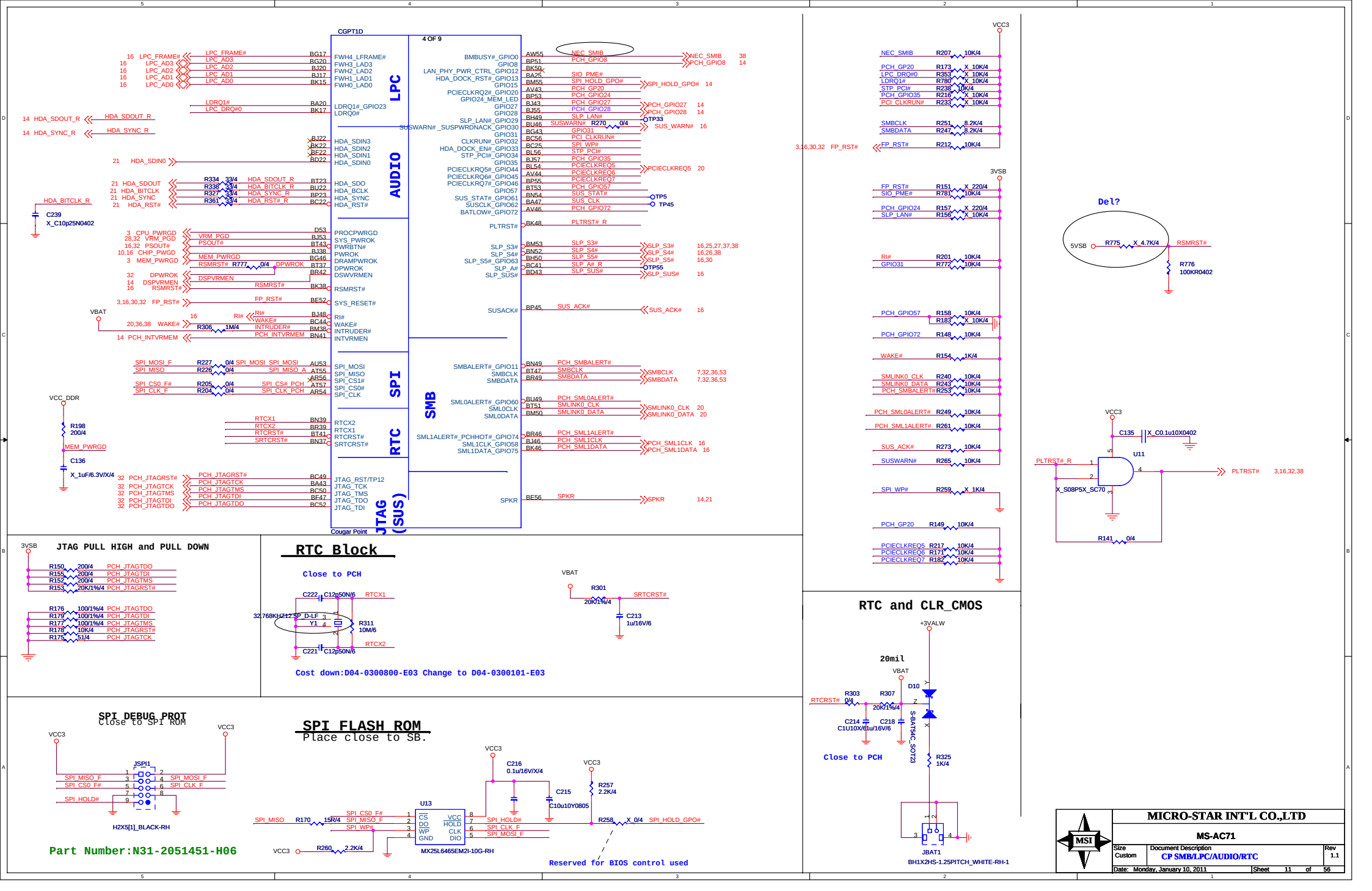

CGPT1D
4 OF 9
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
Cougar Point
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
Cost down:D04-0300800-E03 Change to D04-0300101-E03
SPI DEBUG PROT
Close to SPI ROM
SPI FLASH ROM
Place close to SB.
Part Number:N31-2051451-H06
Reserved for BIOS control used
RTC and CLR_CMOS
Close to PCH
Del?
MICRO-STAR INT'L CO.,LTD
MS-AC71
CP SMB/LPC/AUDIO/RTC
Monday, January 10, 2011
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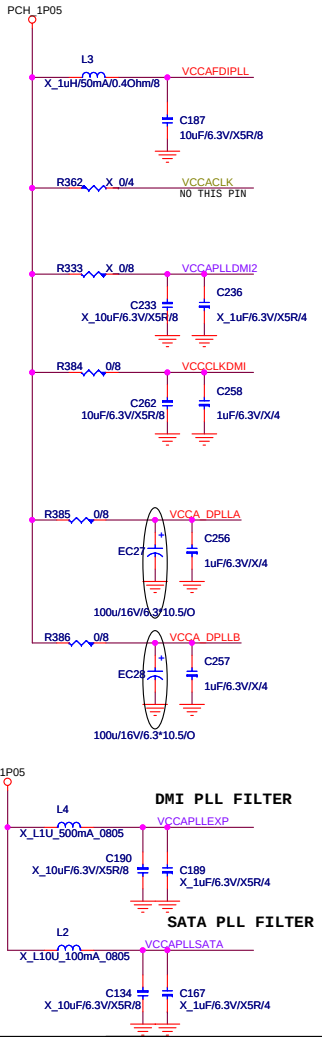
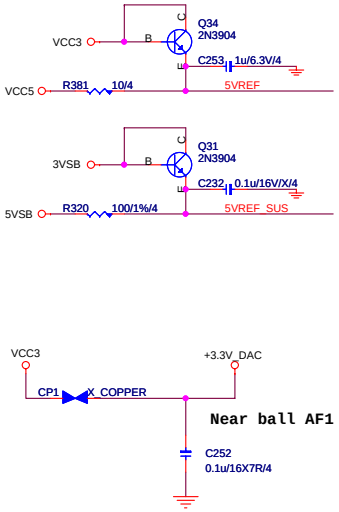
Table 3-7. VCCPLL Decoupling Requirements

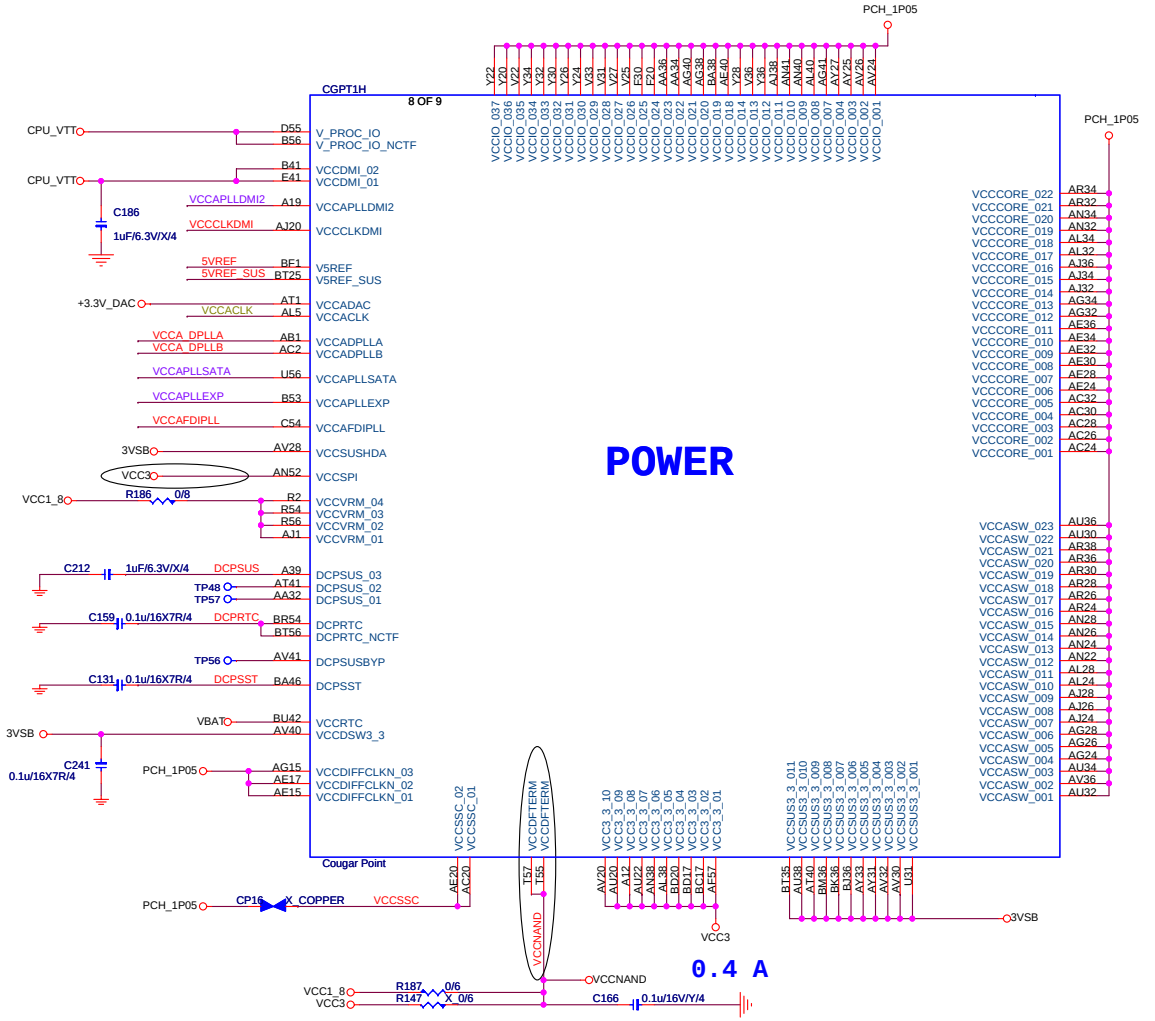
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220uF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10uF 0805 X5R	1	3mΩ	0.51nH	Output		1,2,3

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

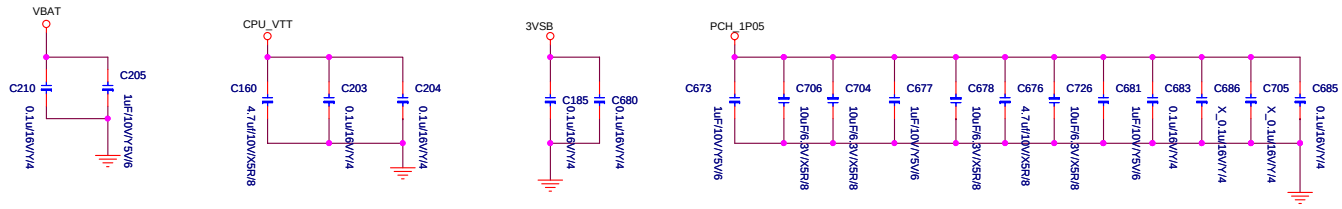


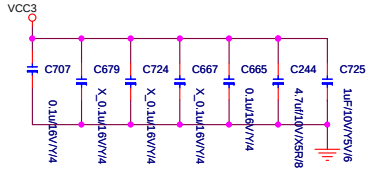
5VREF & 5VREF_SUS Sequencing Circuit



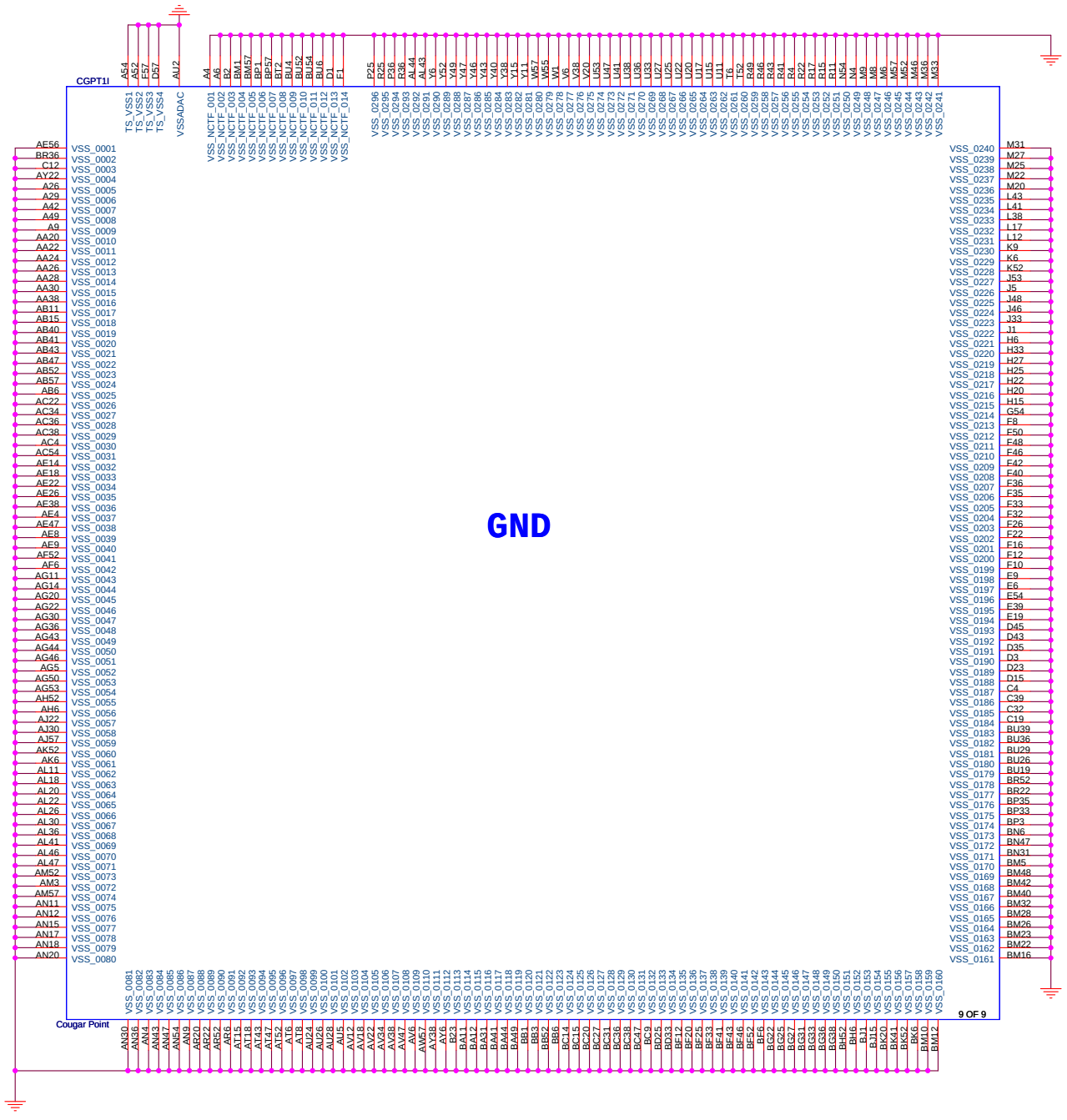


PCH decoupling cap

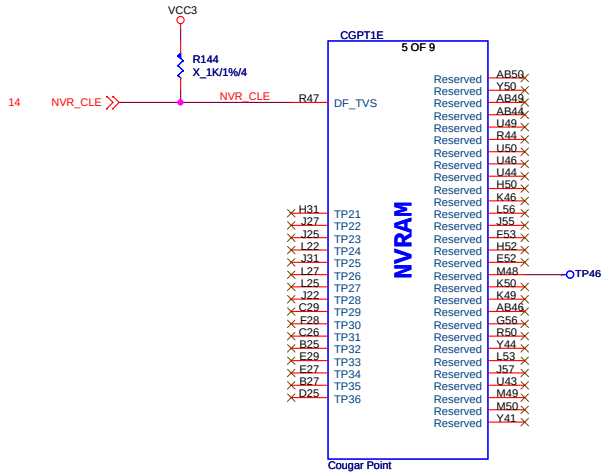




MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: CP POWER	Rev: 1.1
Date: Monday, January 10, 2011	Sheet 12 of 56	



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: CP GND/NVRAM	Rev: 1.1
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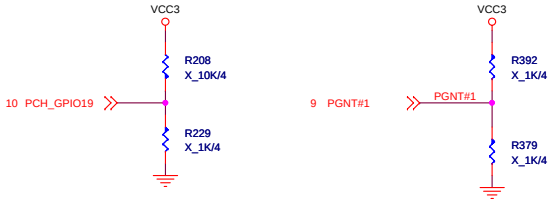
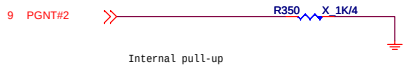
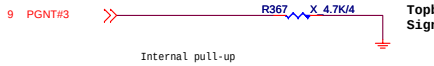
CP REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating

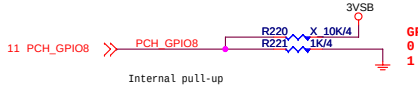




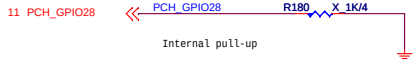
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up



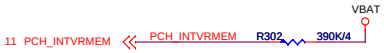
GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

INT3_3V#
0 : ????????????????
1 : ???????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



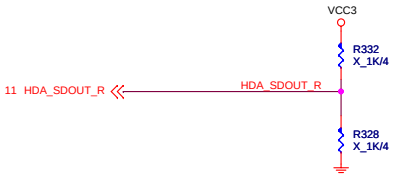
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

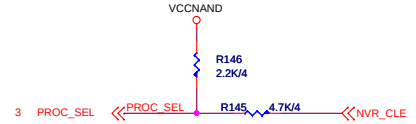
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



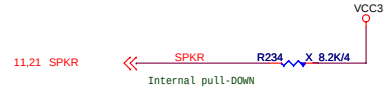
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

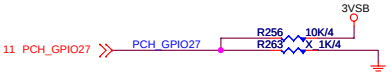
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

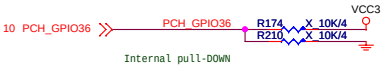


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

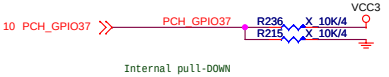


In Deep Sleep Power Well.

If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high



Cougar point EDS PAGE:93 This signal should not be pull high

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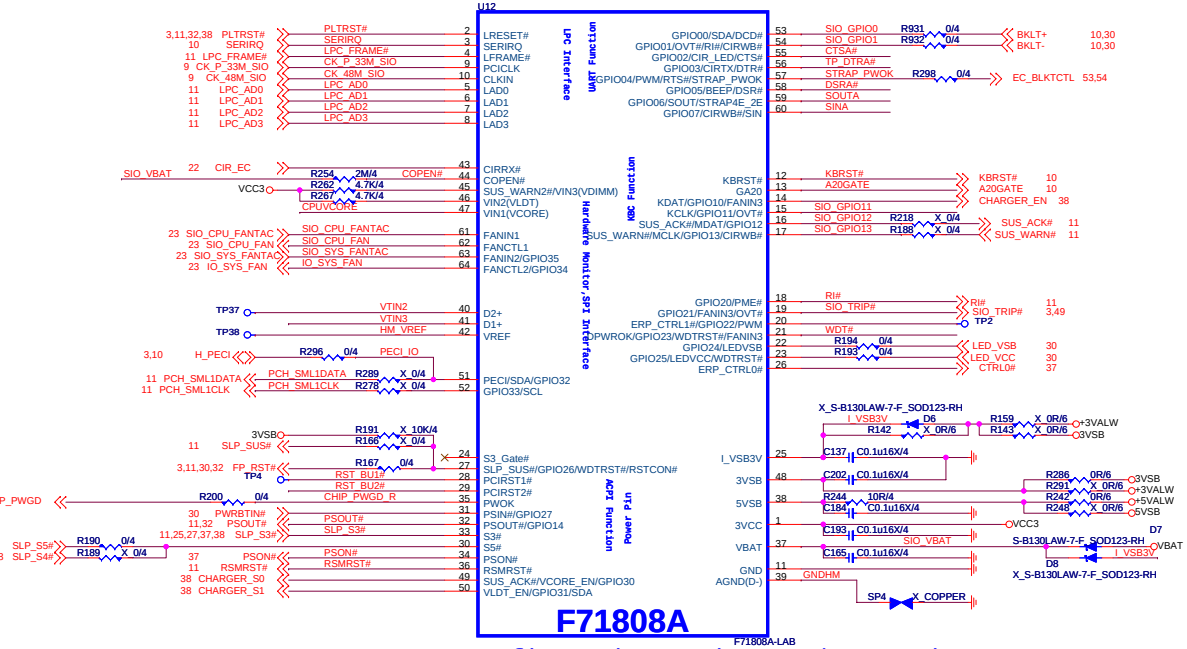

PIN	Function	NET Name	HI	LO
64	SIO_SYS1_FAN	FANCTL2	PWM FAN	LINEAR FAN
59	SOUTA	Config 4E/2E	4E	2E

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PCH

GPIO	Alt Func	Type	POWER	SMI	TOL	DEFAULT	SIGNAL NAME	Pull up or Pull down	BIOS
GPIO0	BMBUSY#	I/O	CORE	Y	3.3V	GPI	NEC_SMIB	**Pull-up 10K to VCC3**	GPI
GPIO1		I/O	CORE	Y	3.3V	GPI	WLAN2_PWRON		GPO
GPIO2	PIRQE#	I/OD	CORE	Y	5V	GPI	PIRQE#	**Pull-up 8.2K to VCC3**	No USE
GPIO3	PIRQF#	I/OD	CORE	Y	5V	GPI	PIRQF#	**Pull-up 8.2K to VCC3**	No USE
GPIO4	PIRQG#	I/OD	CORE	Y	5V	GPI	PIRQG#	**Pull-up 8.2K to VCC3**	No USE
GPIO5	PIRQH#	I/OD	CORE	Y	5V	GPI	PIRQH#	**Pull-up 8.2K to VCC3**	No USE
GPIO6		I/O	CORE	Y	3.3V	GPI	BKLT-	**Pull-up 10K to VCC3**	GPI
GPIO7		I/O	CORE	Y	3.3V	GPI	BKLT+	**Pull-up 10K to VCC3**	GPI
GPIO8	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	PCH_GPIO8	**Pull-down 1K to GND**	No USE
GPIO9	OC5#	I/O	Suspend	Y	3.3V	Native	OC5#	**Pull-up 10K to 3VSB**	Native
GPIO10	OC6#	I/O	Suspend	Y	3.3V	Native	OC6#	**Pull-up 10K to 3VSB**	Native
GPIO11	SMBALERT#	I/O	Suspend	Y	3.3V	Native	PCH_GPIO11	**Pull-up 10K to 3VSB**	No USE
GPIO12	LAN_PHY_PWR_CTRL	I/O	Suspend	Y	3.3V	Native	**(NC)**		No USE
GPIO13	HDA_DOCK_RST#	I/O	Suspend	Y	3.3V	GPI	SIO_PME#		No USE
GPIO14	OC7#	I/O	Suspend	Y	3.3V	Native	OC7#	**Pull-up 10K to 3VSB**	Native
GPIO15	Unmultiplexed	I/O	Suspend	Y	3.3V	GPO	SPI_HOLD_GPO#	**Internal pull-down**	Straps
GPIO16	SATA4GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO16	**Pull-up 10K to VCC3**	No USE
GPIO17		I/O	CORE	N	3.3V	GPI	WLAN_PWRON	**Pull-up 10K to VCC3**	GPO
GPIO19		I/O	CORE	N	3.3V	GPI	PCH_GPIO19	**Internal pull-up**	Straps
GPIO20	PCIECLKRQ2#	I/O	CORE	N	3.3V	Native	PCH_GP20	**Pull-down 10K to GND**	Native
GPIO21	SATA0GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO21	**Pull-up 10K to VCC3**	No USE
GPIO22	SCLOCK	I/O	CORE	N	3.3V	GPI	PCH_GPIO22	**Pull-up 10K to VCC3**	No USE
GPIO23	LDRQ1#	I/O	CORE	N	3.3V	Native	**(NC)**		No USE
GPIO24	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PCH_GPIO24	**Pull-up 10K to 3VSB**	No USE
GPIO25	PCIECLKRQ3#	I/O	Suspend	N	3.3V	Native	USB3_CLKRQ#	**Pull-up 10K to 3VSB**	Native
GPIO26	PCIECLKRQ4#	I/O	Suspend	N	3.3V	Native	PCIECLKRQ4#	**(pull high)**	Native
GPIO27	Unmultiplexed	I/O	Deep Sleep	N	3.3V	GPI	DSW_WAKE#	**internal pull-up**	GPI
GPIO28	Unmultiplexed	I/O	Suspend	N	3.3V	GPO	PLL_ODVR_EN	**internal pull-up**	Straps
GPIO29	SLP_LAN#	I/O	Suspend	N	3.3V	GPI	SLP_LAN#	**Pull-up 10K to 3VSB**	No USE
GPIO30	SUSPWRDNACK	I/O	Deep Sleep	N	3.3V	Native	SUSPWRACK	**Pull-up 10K to 3VSB**	Native
GPIO31	ACPRESENT	I/O	Deep Sleep	N	3.3V	GPI	AC_PRESENT	**Pull-up 10K to 3VSB**	No USE
GPIO32	**CLKRUN#**	I/O	CORE	N	3.3V	GPO	PM_CLKRUN#	**Pull-up 8.2K to VCC3**	
GPIO33	HDA_DOCK_EN#	I/O	CORE	N	3.3V	GPO	HDA_DOCK_EN#	**Test Pin**	No USE
GPIO34	STP_PCI#	I/O	CORE	N	3.3V	GPI	STP_PCI#	**Pull-up 10K to VCC3**	No USE
GPIO35	**(Mobile Only)**	I/O	CORE	N	3.3V	GPO	PCH_GPIO35	**Test Pin**	No USE
GPIO36	SATA2GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO36	**Pull-down 10K to GND**	Straps
GPIO37	SATA3GP	I/O	CORE	N	3.3V	GPI	PCH_GPIO37	**Pull-down 10K to GND**	Straps
GPIO38	SLOAD	I/O	CORE	N	3.3V	GPI	PCH_GPIO38	**Pull-up 10K to VCC3**	No USE
GPIO39	SDATAOUT0	I/O	CORE	N	3.3V	GPI	GFX_DET		GPI
GPIO40	OC1#	I/O	Suspend	N	3.3V	Native	USB_OC1#	**(pull high)**	Native

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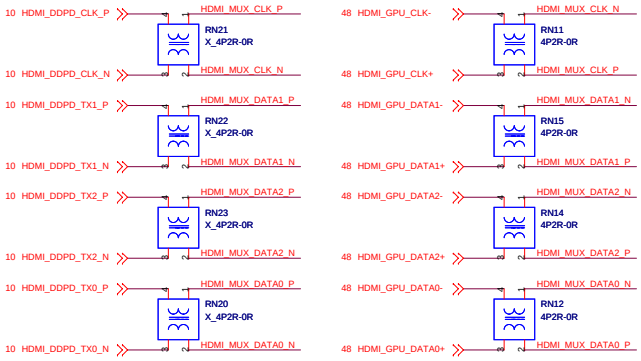

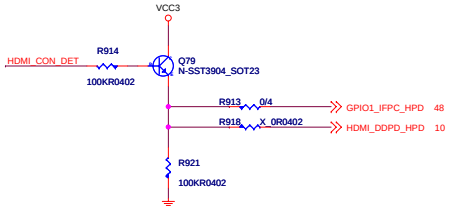

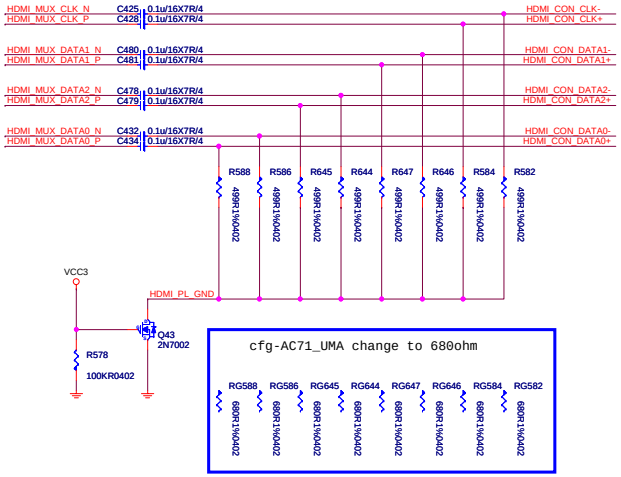

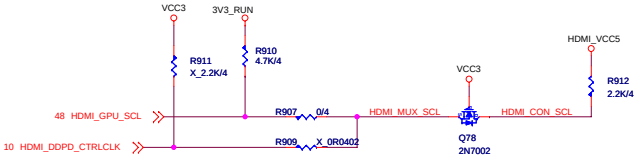

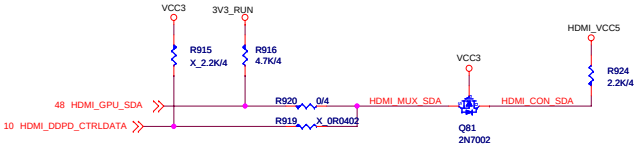

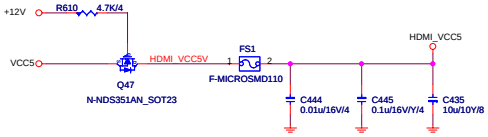

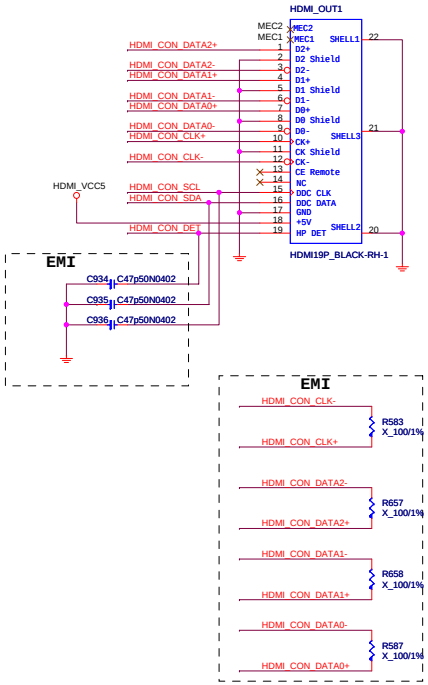

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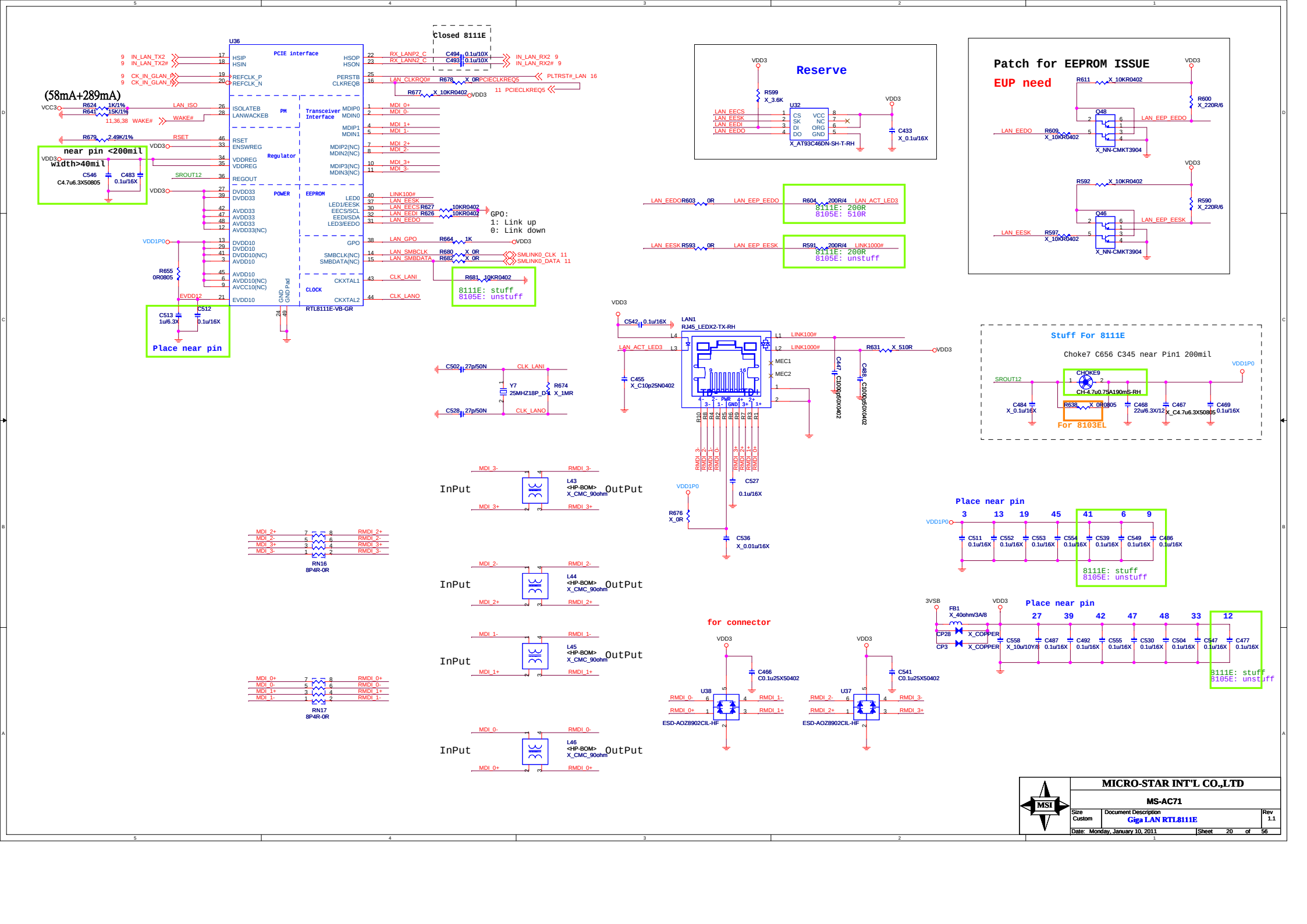
U36
PCIE interface
RTL8111E-VB-GR
Closed 8111E
(58mA+289mA)
near pin <200mil
width>40mil
Place near pin
Reserve
X_AT93C46DN-SH-T-RH
Patch for EEPROM ISSUE
EUP need
X_NN-CMKT3904
GPO:
1: Link up
0: Link down
8111E: stuff
8105E: unstuff
LAN1
RJ45_LEDX2-TX-RH
Stuff For 8111E
Choke7 C656 C345 near Pin1 200mil
CH-4.7u0.75A190mS-RH
For 8103EL
InPut
OutPut
L43
L44
L45
L46
<HP-BOM>
X_CMC_90ohm
RN16
RN17
8P4R-0R
for connector
U38
U37
ESD-AOZ8902CIL-HF
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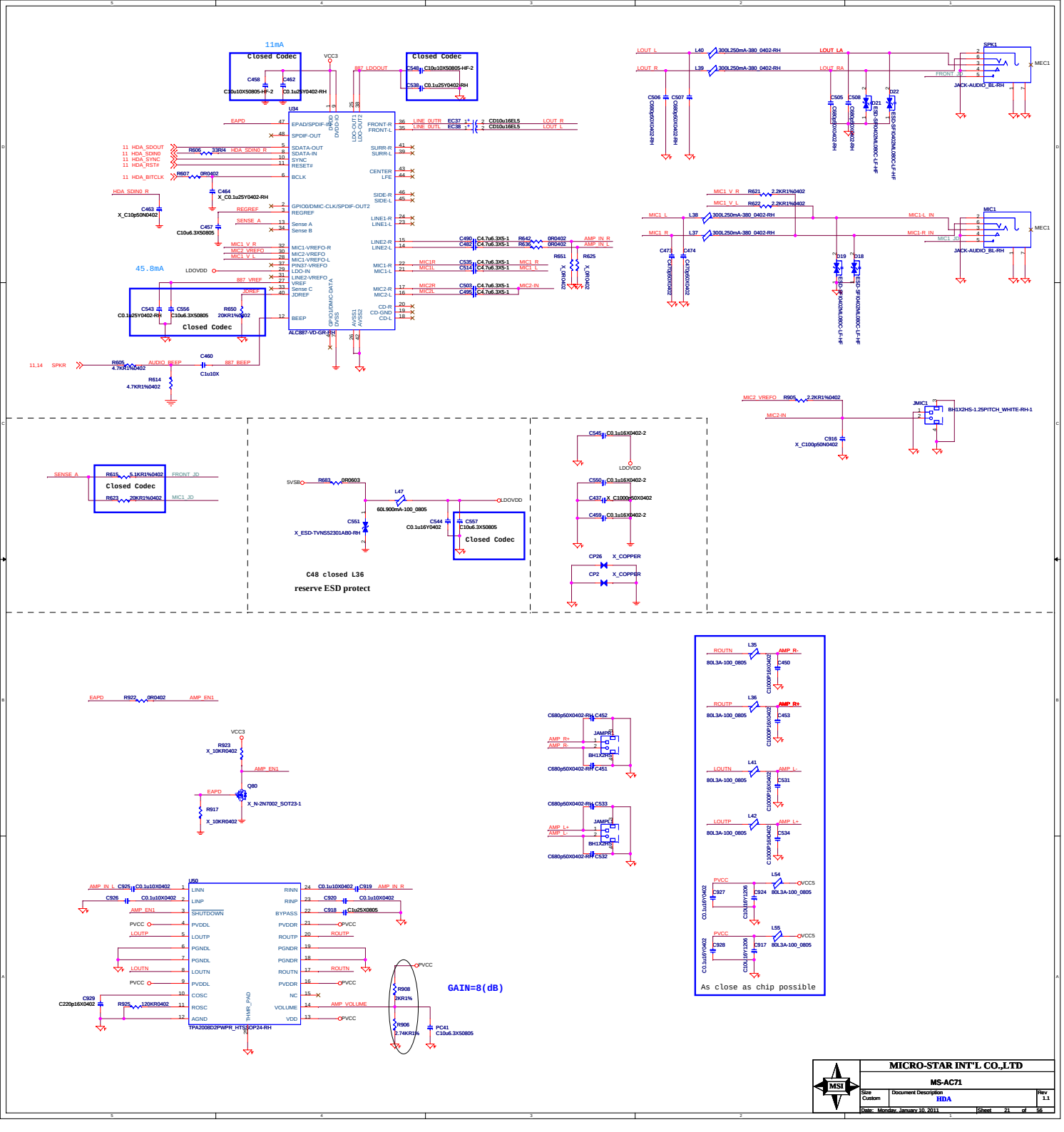

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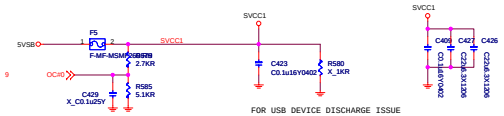
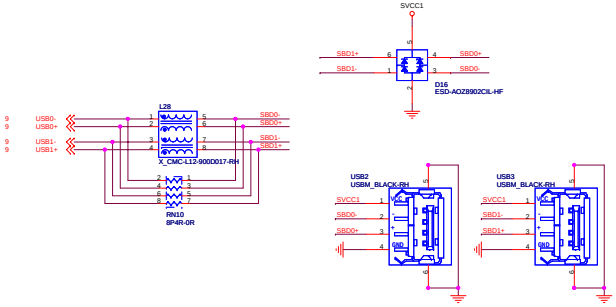
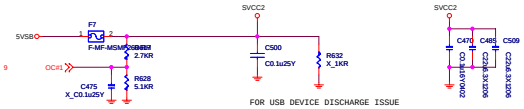
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



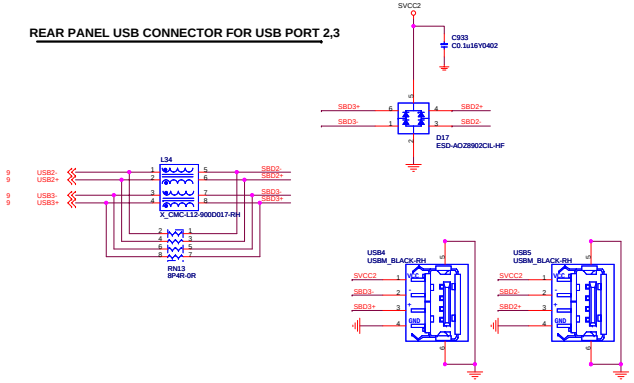
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



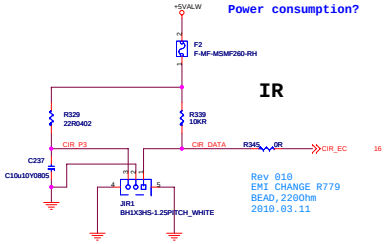
POWER CIRCUIT FOR USB PORT 2,3 (REAR)



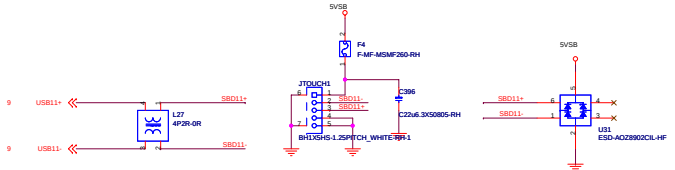
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



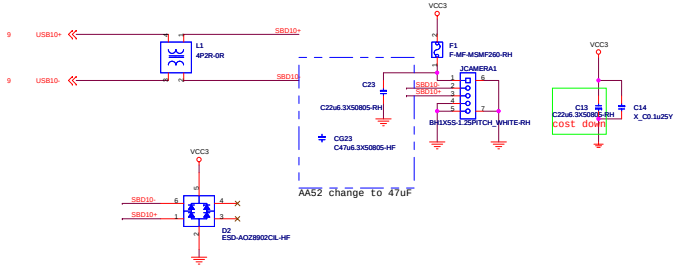
Power consumption?



Multi Touch



Webcam



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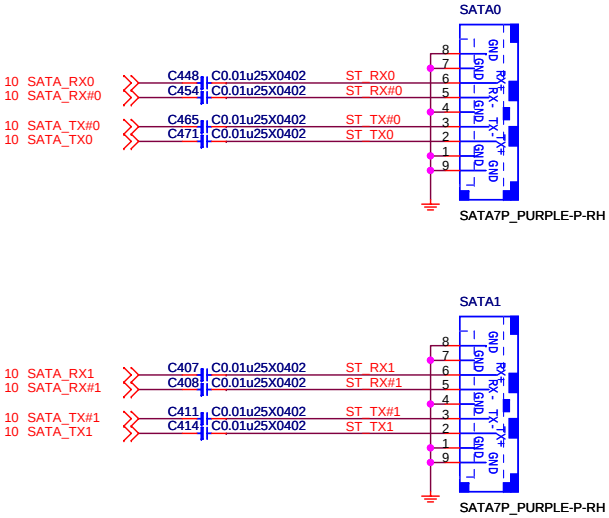
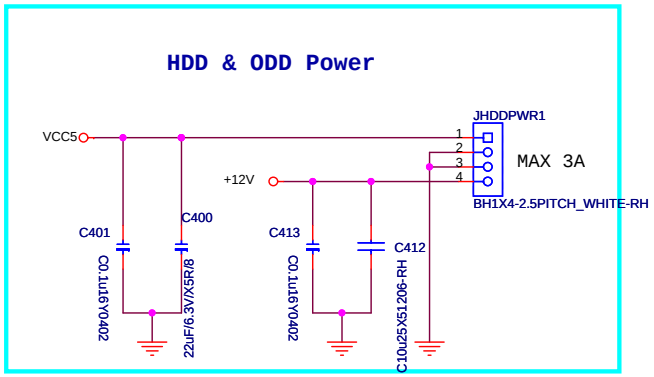
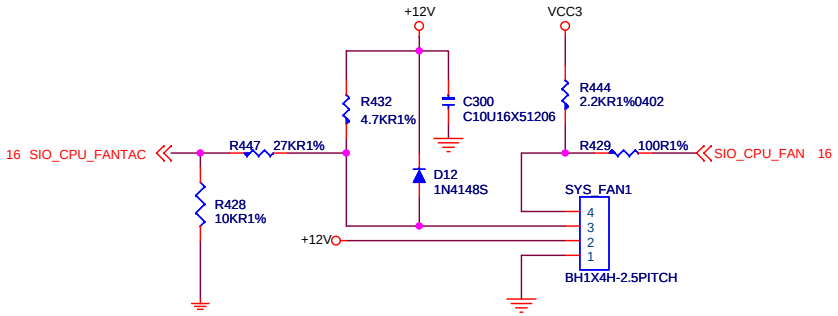
SATA HDD



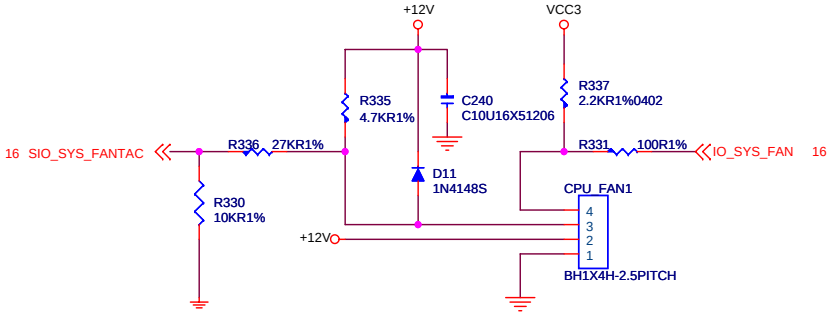
HDD & ODD Power



SYSTEM FAN



CPU FAN



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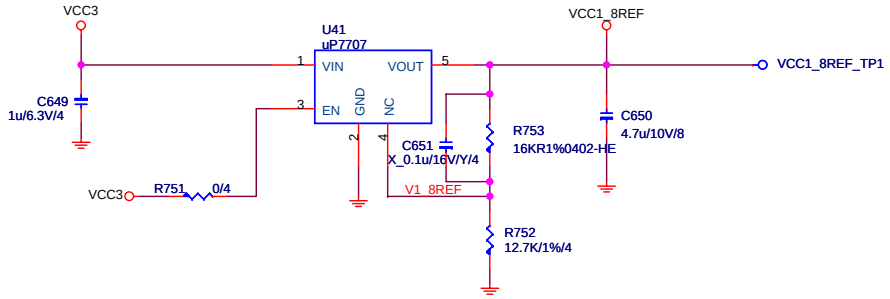
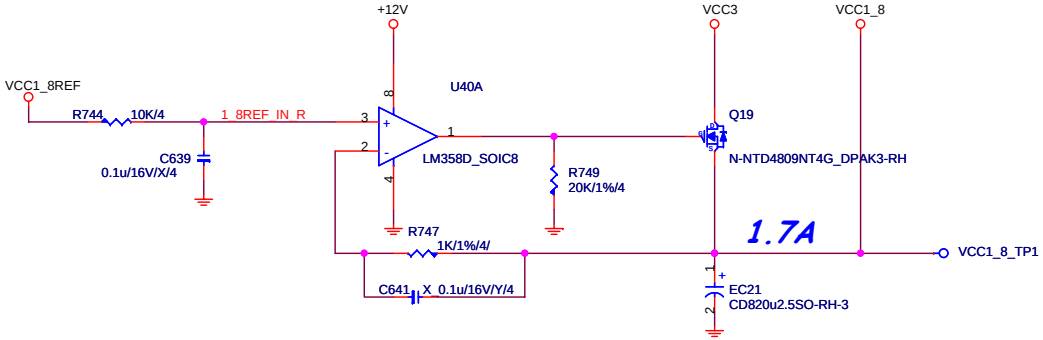
VCC1_8REF



CPU_PLL_1_8



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CPU_SA Power

VTT-->CPU_SA

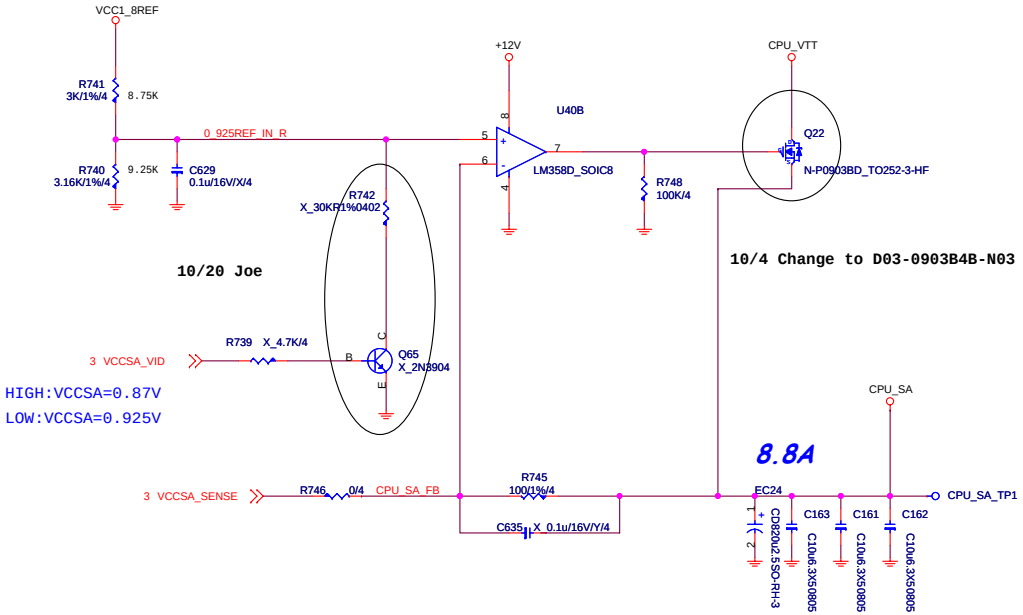
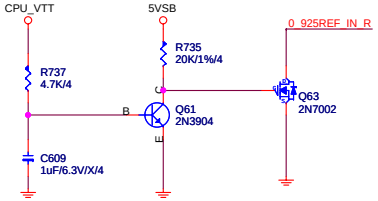


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 X5R	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1, 2, 3

Waitting CPU_VTT Ready



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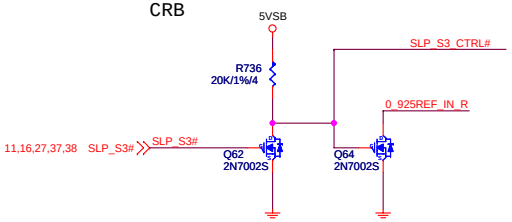


CP Power

DDR-->PCH

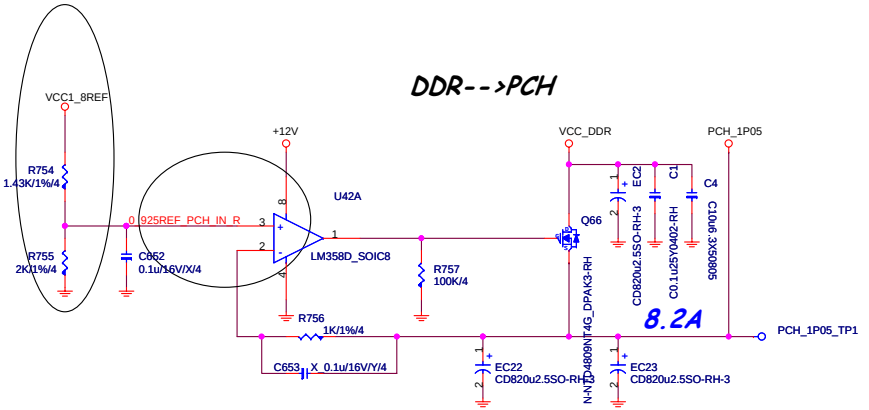
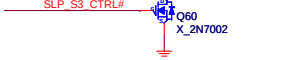


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1X560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different that those shown.

CRB



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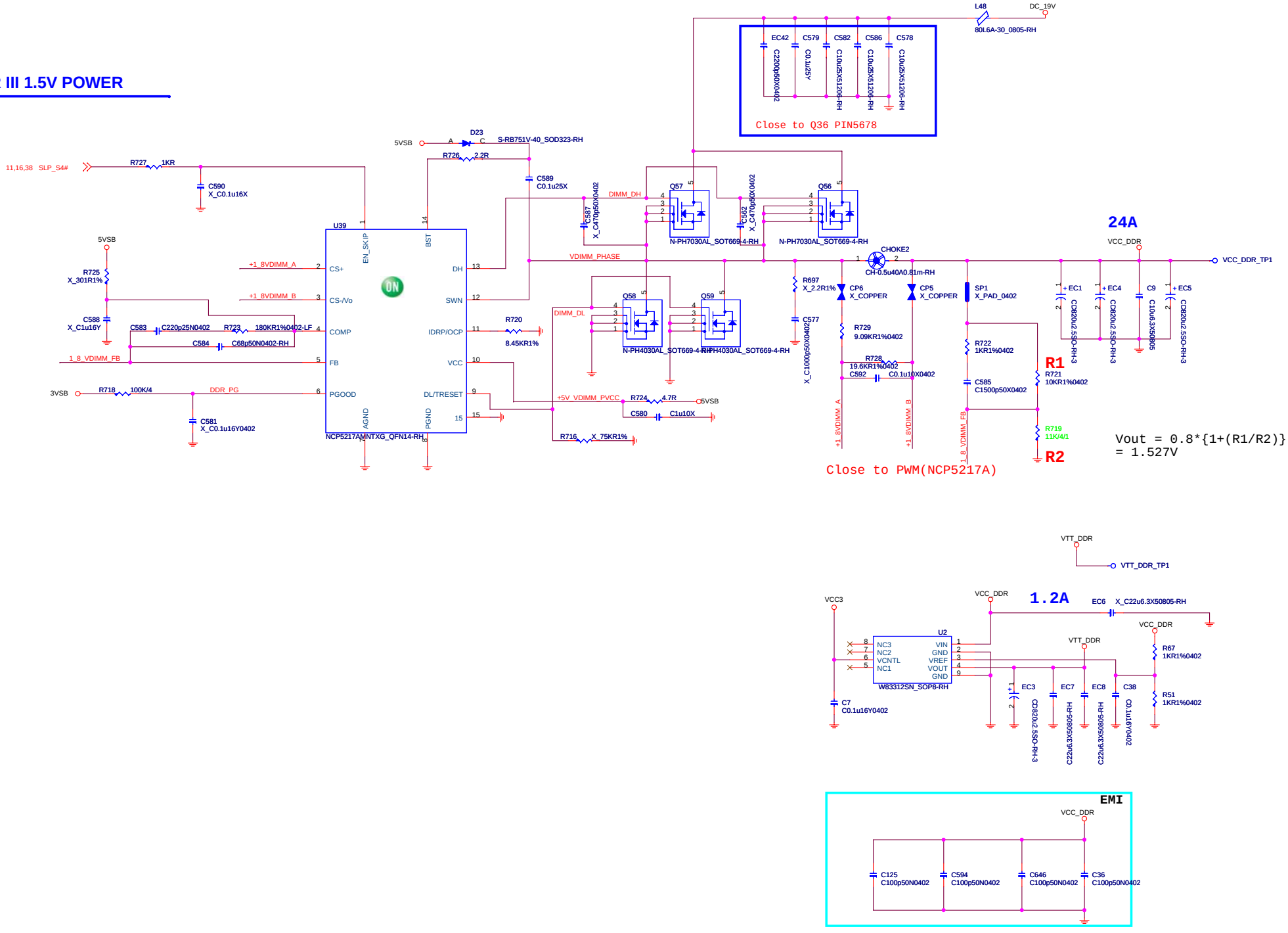
DDR III 1.5V POWER



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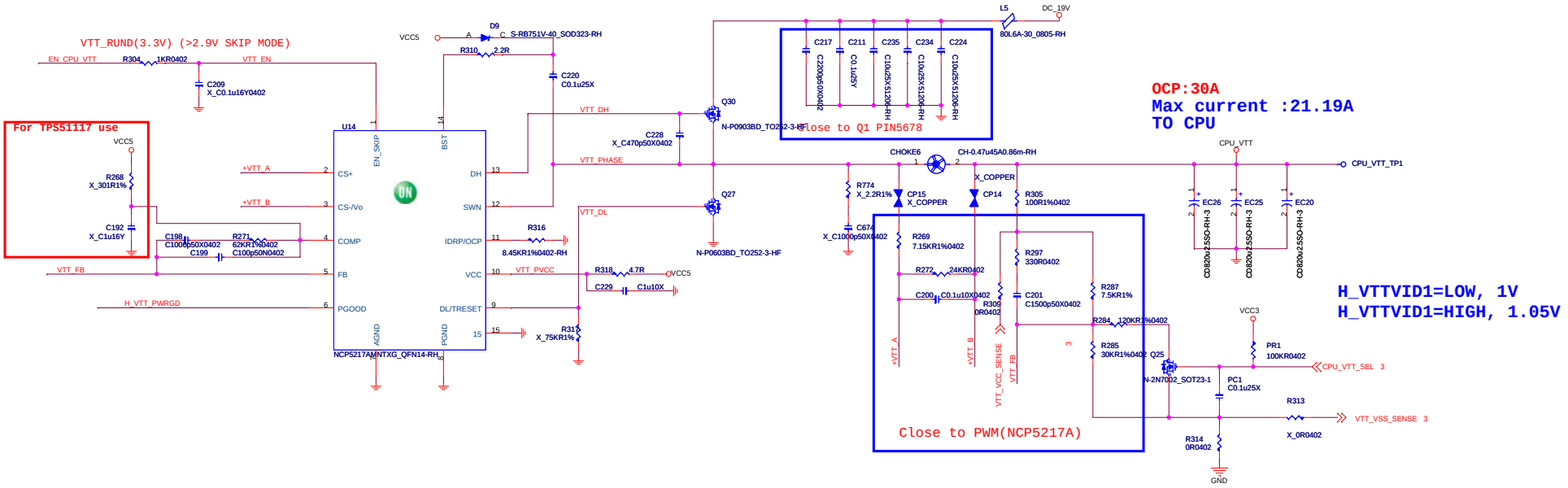

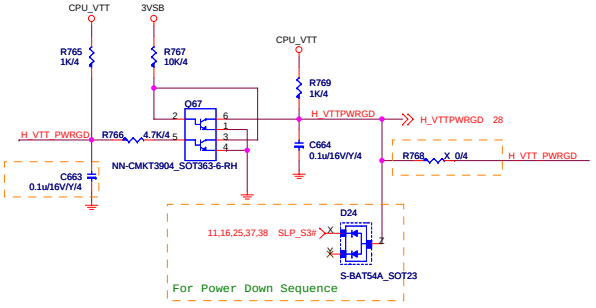

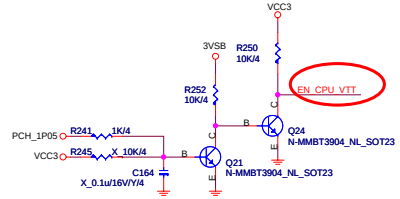

1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA

If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR

If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

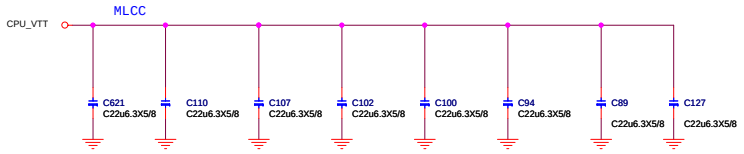

Table 3-6. VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

MSI	MICRO-STAR INT'L CO.,LTD		
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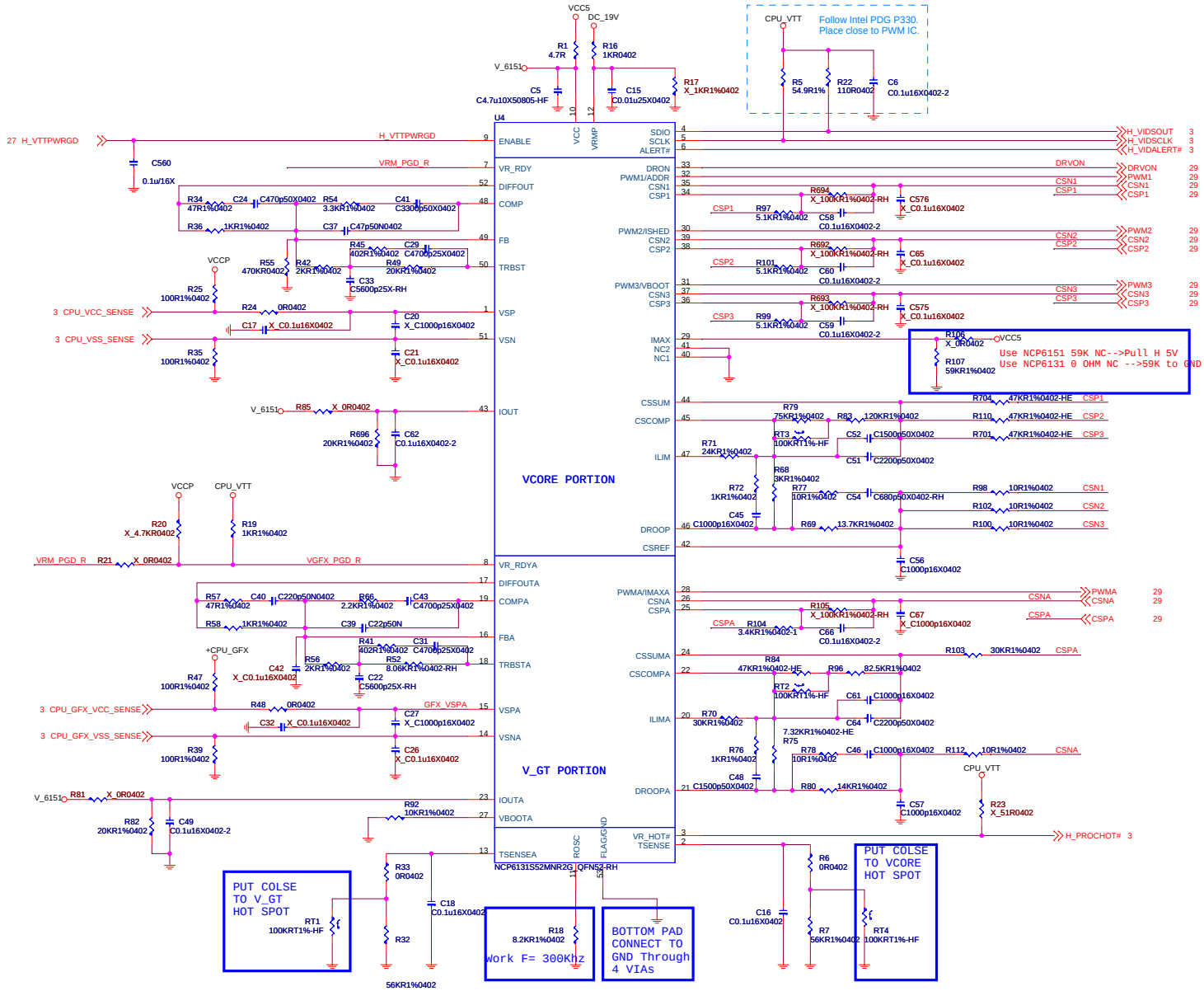
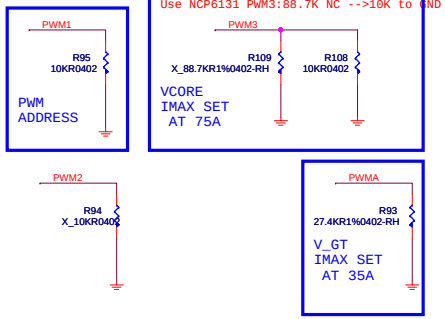
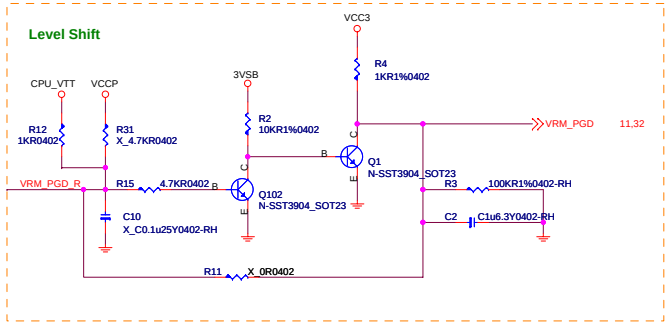
Modulize of NCP6151/NCP6131 COLAY (19V VR12)



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101





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MS-AC71		
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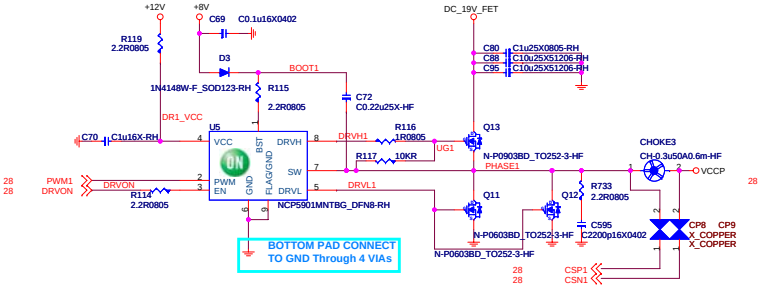
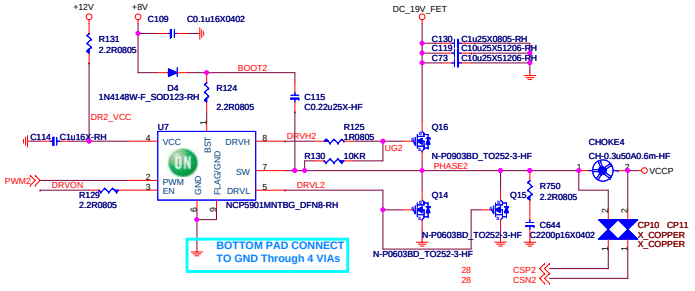
+CPU_VCCP

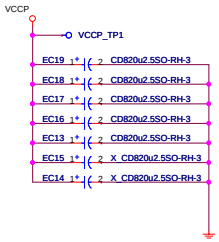
High Side D03-0480900-O05 High Side D03-0903B4B-N03
Low Side D03-0480600-O05 Low Side D03-0603B2B-N03

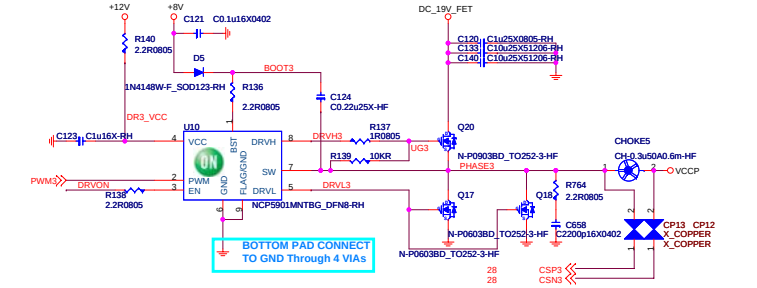
VCCP:75A



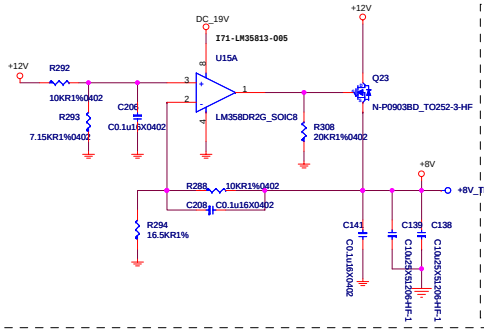


+CPU_VCCP Output Caps

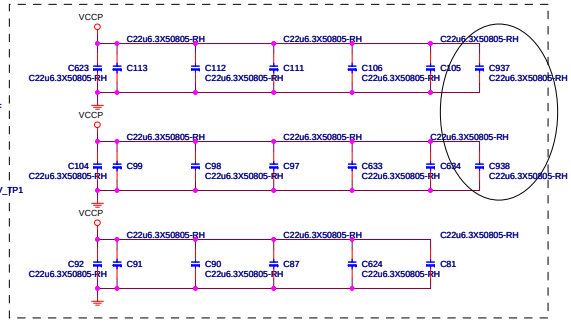




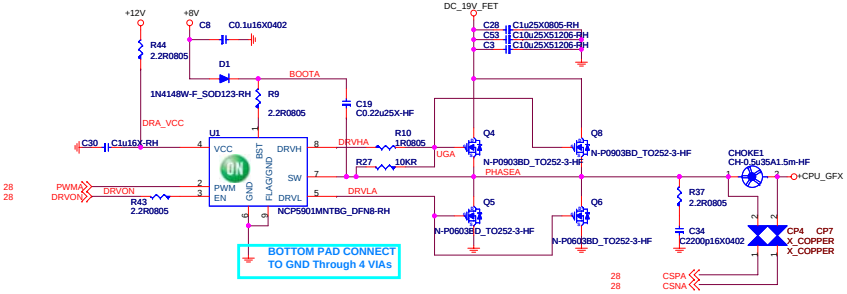
12V to 8V 0.5A



+CPU_VCCP-Decoupling

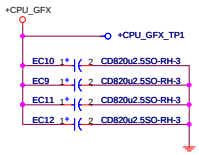


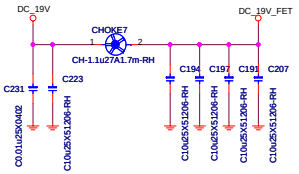
+CPU_GFX



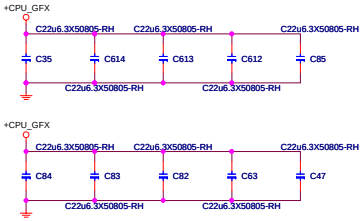
+CPU_GFX Output Caps

+CPU_GFX:35A





+CPU_GFX Decoupling



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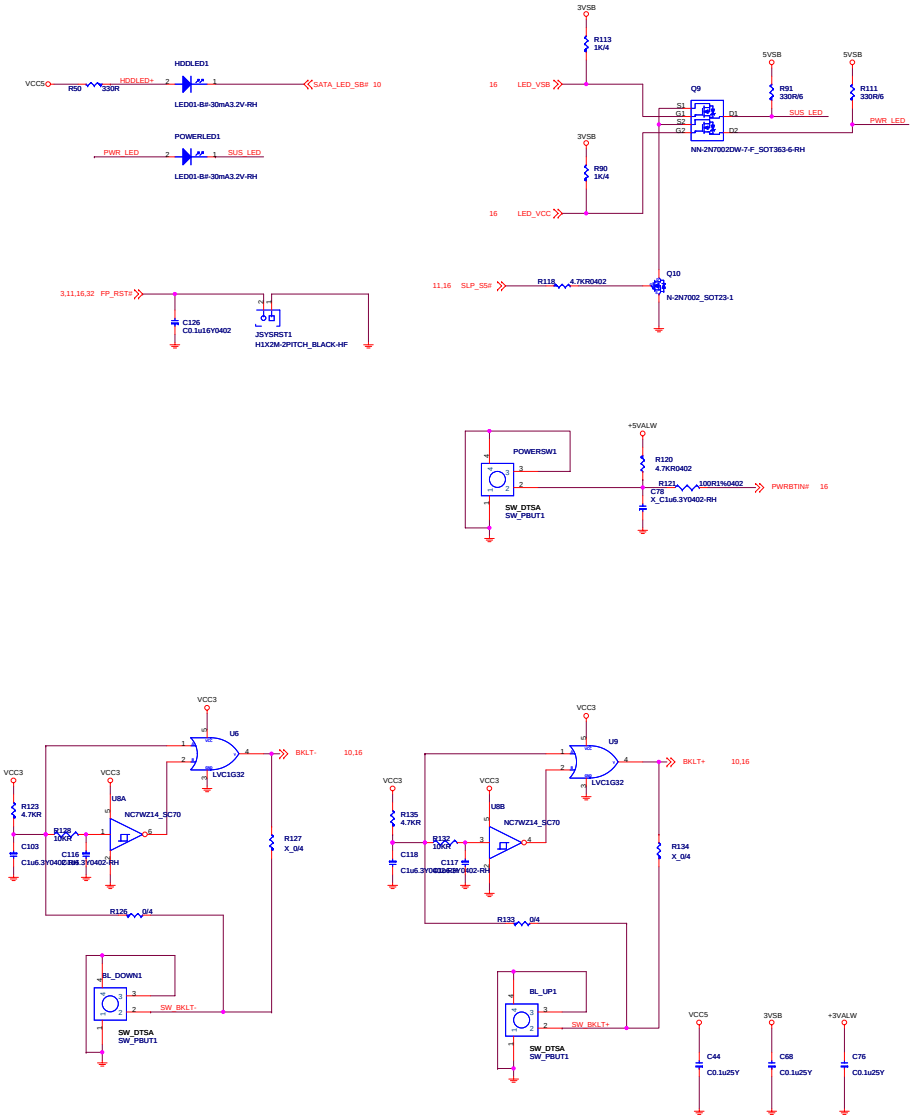
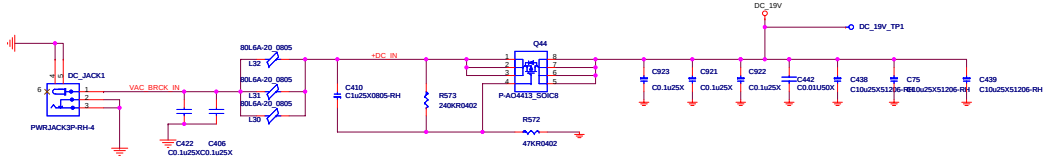
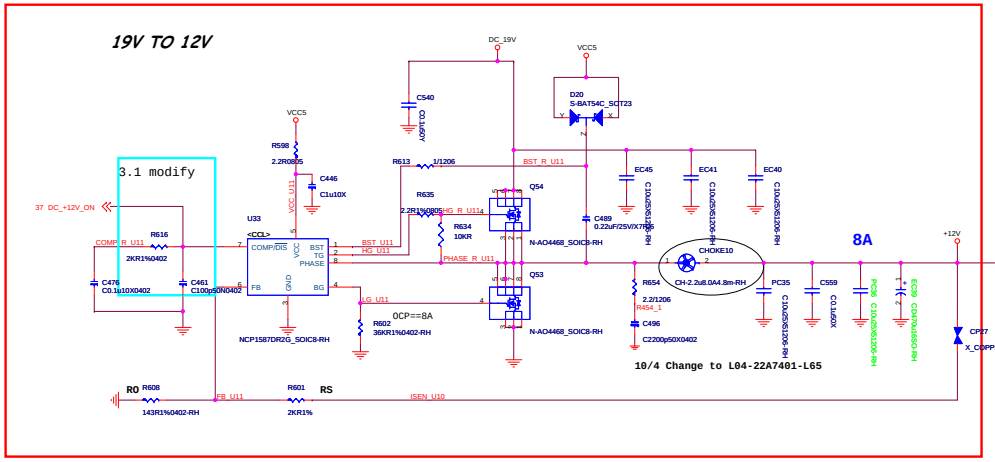
LED (for Fintek 71882)







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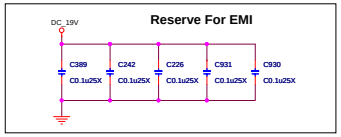
LG_U11



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SB_SINK
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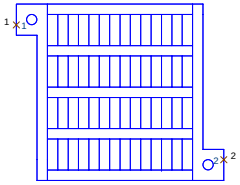
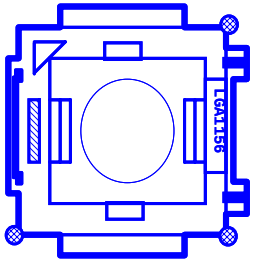
SB_SINK

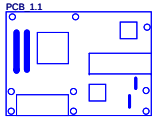


AURAS (0P103760)

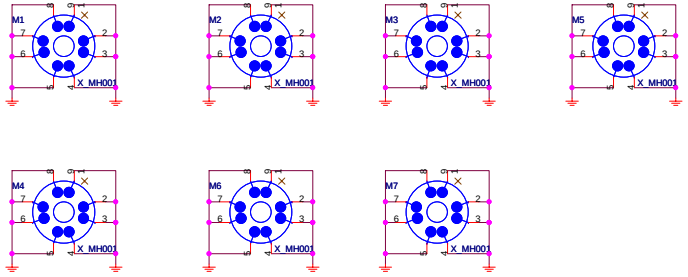
CPU1_X1
CPU SOCKET



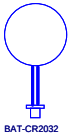
PCB1
PCB_1.1



Mounting Holes

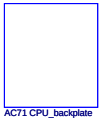


BAT1



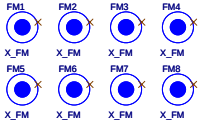
BAT-CR2032

CPU_backplate

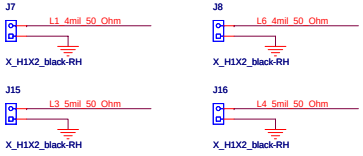


AC71 CPU_backplate

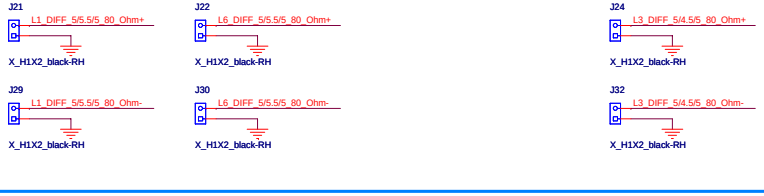
Optical Fiducial Marks-120



Single End 50ohm



Diff 80ohm



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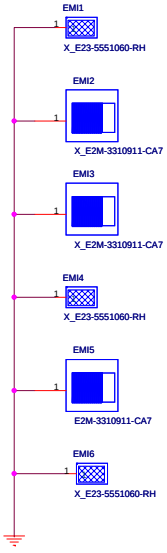
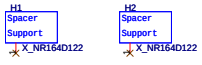
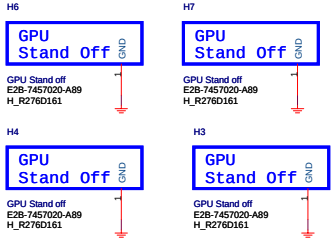


VRM SINK



GPU Stand off



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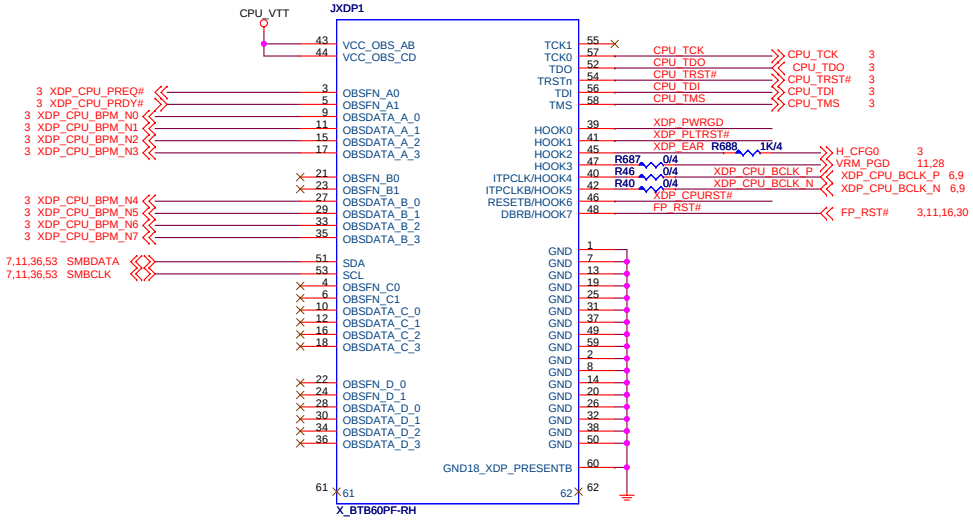
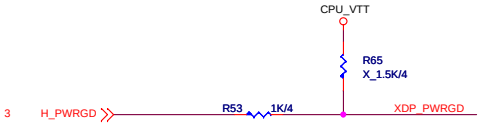
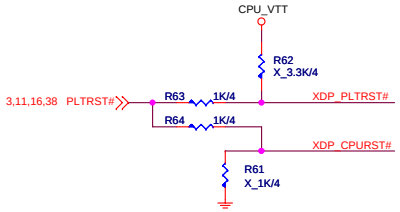
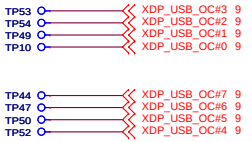
Reserve debug port 5020

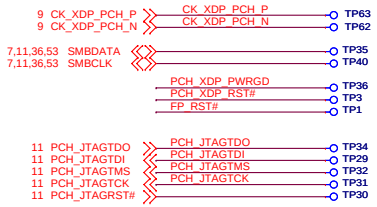




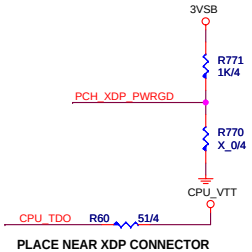


PCH XDP





PCH XDP PWRGD/RESET



PLACE NEAR XDP CONNECTOR

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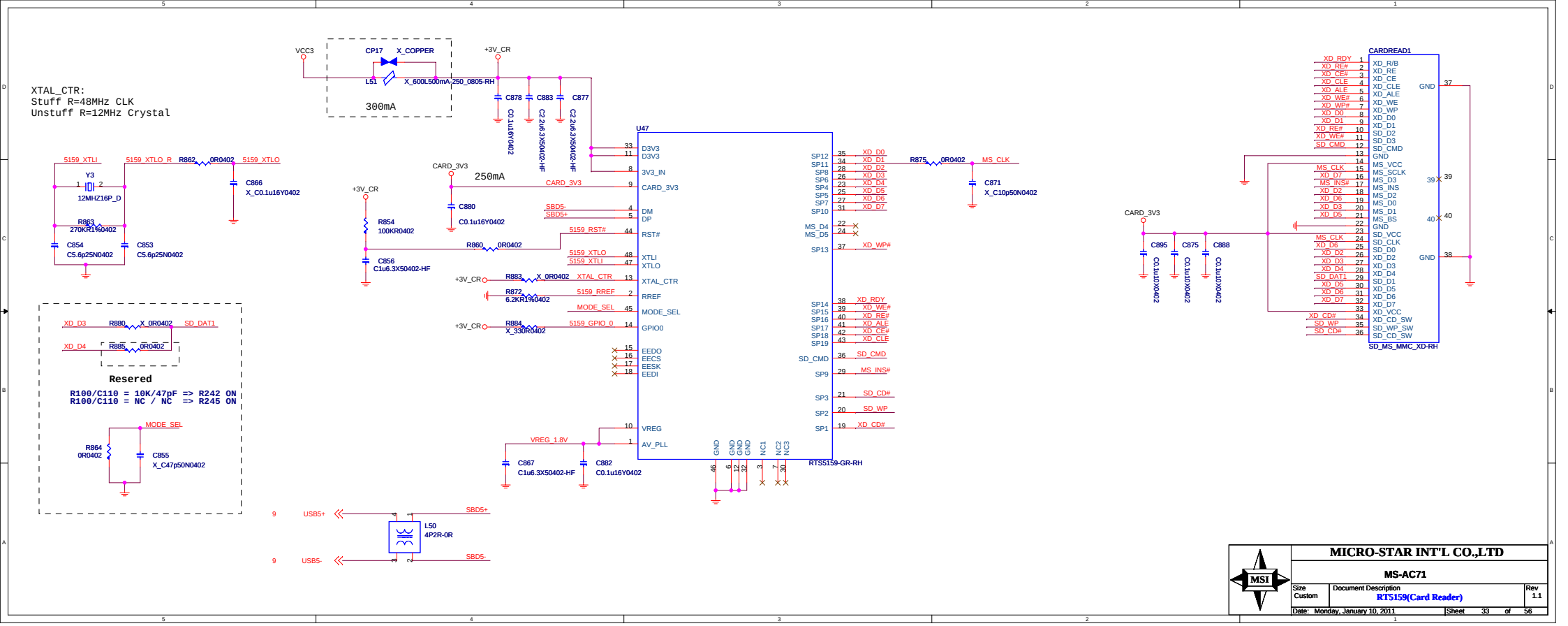

MICRO-STAR INT'L CO.,LTD	
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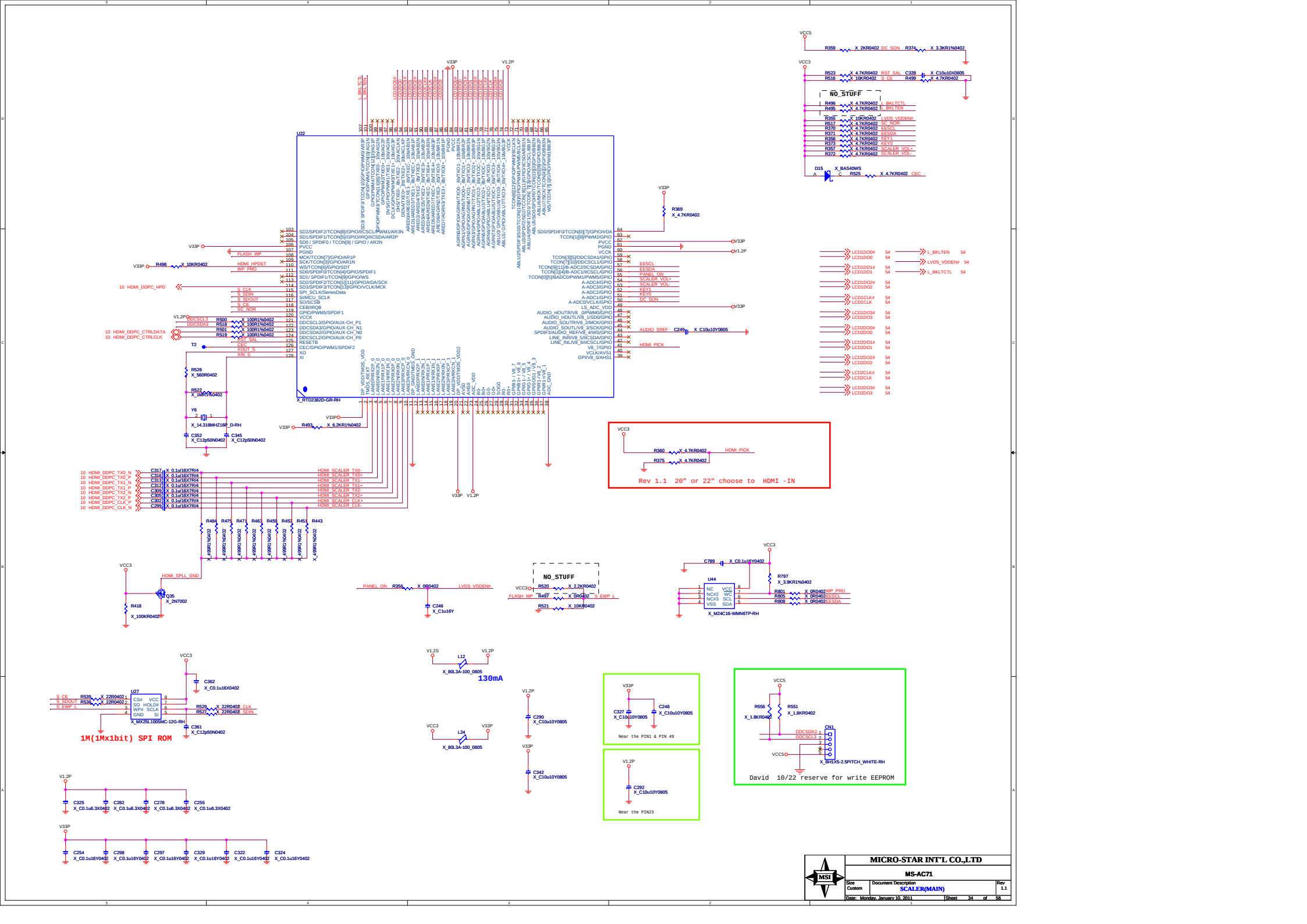
U22
X_RTD2382D-GR-RH
SD2/SPDIF2/TCON[8]/GPIO/IIICSCL/PWM1/AR3N
SD1/SPDIF1/TCON[5]/GPIO/IRQ/IICSDA/AR2P
SD0 / SPDIF0 / TCON[9] / GPIO / AR2N
PVCC
PGND
MCK/TCON[7]/GPIO/AR1P
SCK/TCON[3]/GPIO/AR1N
WS/TCON[6]/GPIO/SDT
SD0/SPDIF0/TCON[4]/GPIO/SPDIF1
SD1/ SPDIF1/TCON[9]/GPIO/WS
SD2/SPDIF2/TCON[1][11]/GPIO/IRDA/SCK
SD3/SPDIF3/TCON[13]/GPIO/VCLK/MCK
SPI_SCLK/SeriesData
SI/MCU_SCLK
SO/SCSB
CEB/IRQB
GPIO/PWM5/SPDIF1
VCCK
DDCSCL3/GPIO/AUX-CH_P1
DDCSDA3/GPIO/AUX-CH_N1
DDCSDA2/GPIO/AUX-CH_N0
DDCSCL2/GPIO/AUX-CH_P0
RESETB
CEC/GPIO/PWM1/SPDIF2
XO
XI
SD0/SPDIF0/TCON[0][7]/GPIO/IrDA
TCON[1][8]/PWM2/GPIO
PVCC
PGND
VCCK
TCON[3][5]/DDCSDA1/GPIO
TCON[7][10]/DDCSCL1/GPIO
TCON[9][11]/B-ADC2/IICSDA/GPIO
TCON[1][4]/B-ADC1/IICSCL/GPIO
TCON[0][5]/BADC0/PWM1/PWM5/GPIO
A-ADC4/GPIO
A-ADC3/GPIO
A-ADC2/GPIO
A-ADC1/GPIO
A-ADC0/VCLK/GPIO
LS_ADC_VDD
AUDIO_HOUTR/V8_0/PWM0/GPIO
AUDIO_HOUTL/V8_1/SDI/GPIO
AUDIO_SOUTR/V8_2/MCK/GPIO
AUDIO_SOUTL/V8_3/SCK/GPIO
SPDIF3/AUDIO_REF/V8_4/WS/GPIO
LINE_INR/V8_5/IICSDA/GPIO
LINE_INL/V8_6/IICSCL/GPIO
V8_7/GPIO
VCLK/AVS1
GPI/V8_0/AHS1
FLASH_WP
HDMI_HPDET
WP_PRO
S_CLK
S_SDIN
S_SDOUT
S_CE
SC_NOR
DDCSCL3
DDCSDA3
REST_SAL
CEC
XOUT_S
XIN_S
EESCL
EESDA
PANEL_ON
SCALER_VOL+
SCALER_VOL-
KEY1
KEY0
DC_SON
AUDIO_SREF
HDMI_PICK
LS_ADC_VDD
LCD1DO0#
LCD1DO0
LCD1DO1#
LCD1DO1
LCD1DO2#
LCD1DO2
LCD1CLK#
LCD1CLK
LCD1DO3#
LCD1DO3
LCD2DO0#
LCD2DO0
LCD2DO1#
LCD2DO1
LCD2DO2#
LCD2DO2
LCD2CLK#
LCD2CLK
LCD2DO3#
LCD2DO3
L_BKLTEN
LVDS_VDDEN#
L_BKLTCTL
HDMI_SCALER_TX0-
HDMI_SCALER_TX0+
HDMI_SCALER_TX1-
HDMI_SCALER_TX1+
HDMI_SCALER_TX2-
HDMI_SCALER_TX2+
HDMI_SCALER_CLK+
HDMI_SCALER_CLK-
HDMI_SPLL_GND
Rev 1.1 20" or 22" choose to HDMI -IN
NO_STUFF
1M(1Mx1bit) SPI ROM
130mA
Near the PIN1 & PIN 49
Near the PIN23
David 10/22 reserve for write EEPROM
MICRO-STAR INT'L CO.,LTD
MS-AC71
SCALER(MAIN)
Rev 1.1
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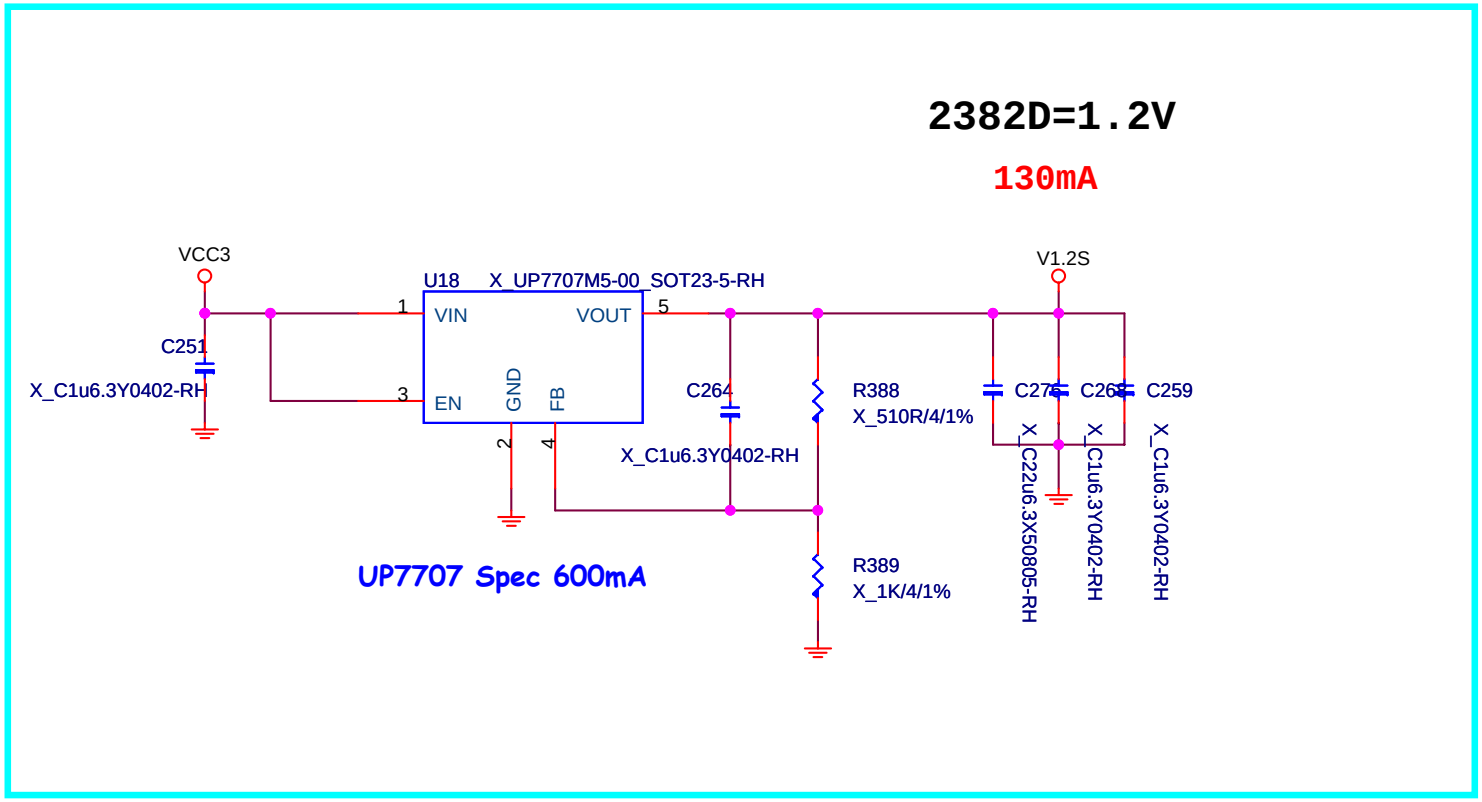

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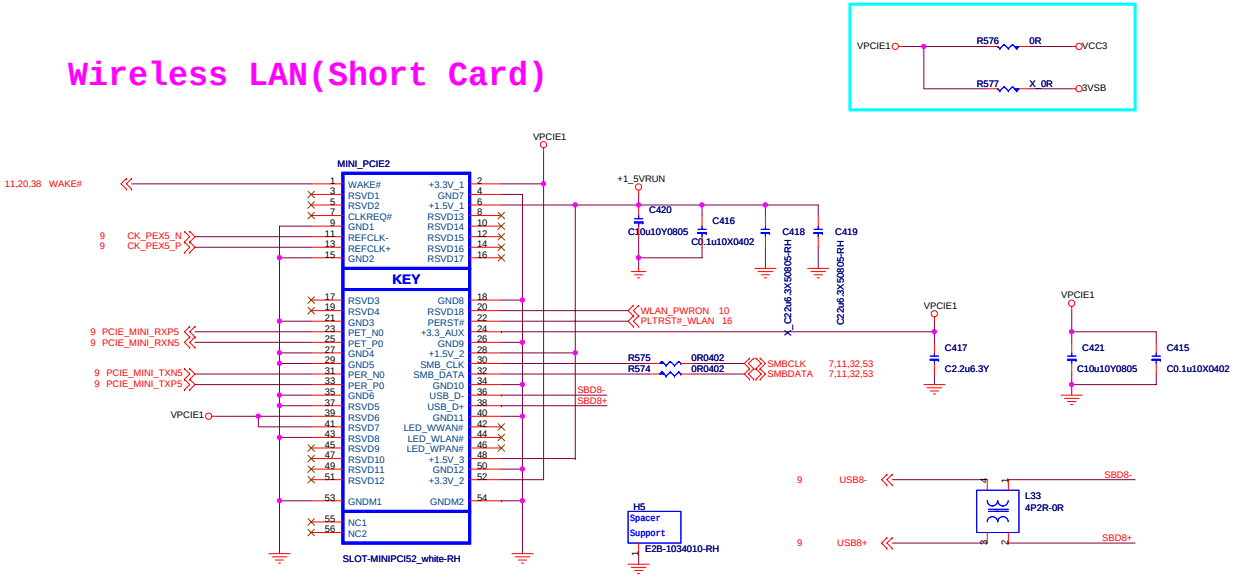
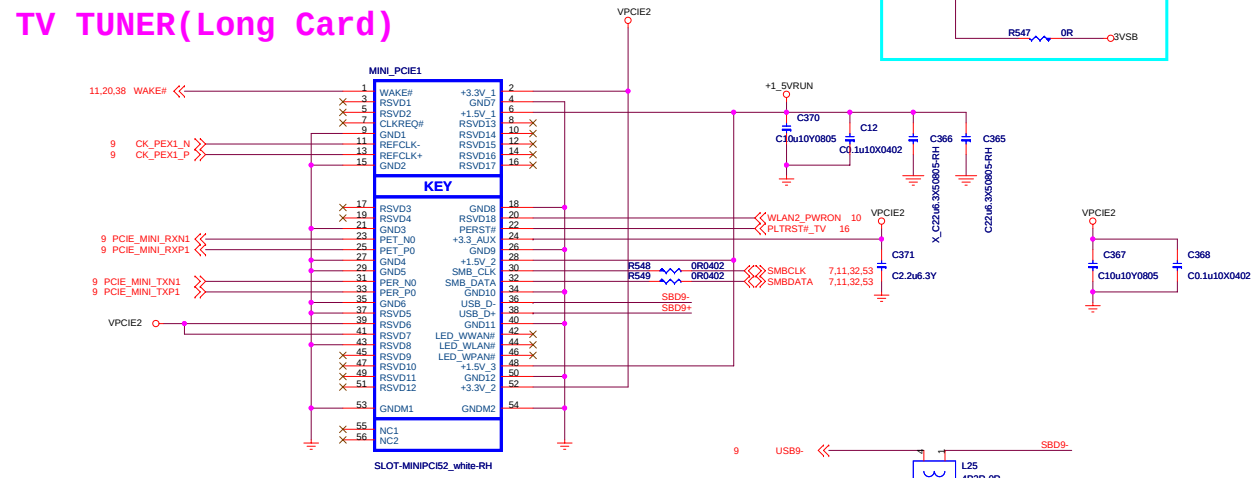
Wireless LAN(Short Card)

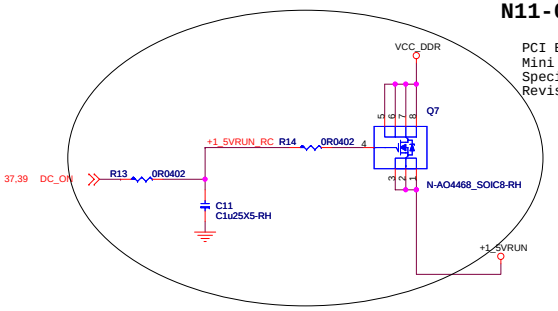


TV TUNER(Long Card)



N11-0520040-A81

PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2



H8
Spacer
Support
E2B-1034010-RH

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	MS-AC71	
Size: Custom	Document Description: MINI-PCIE Slot	Rev: 1.1
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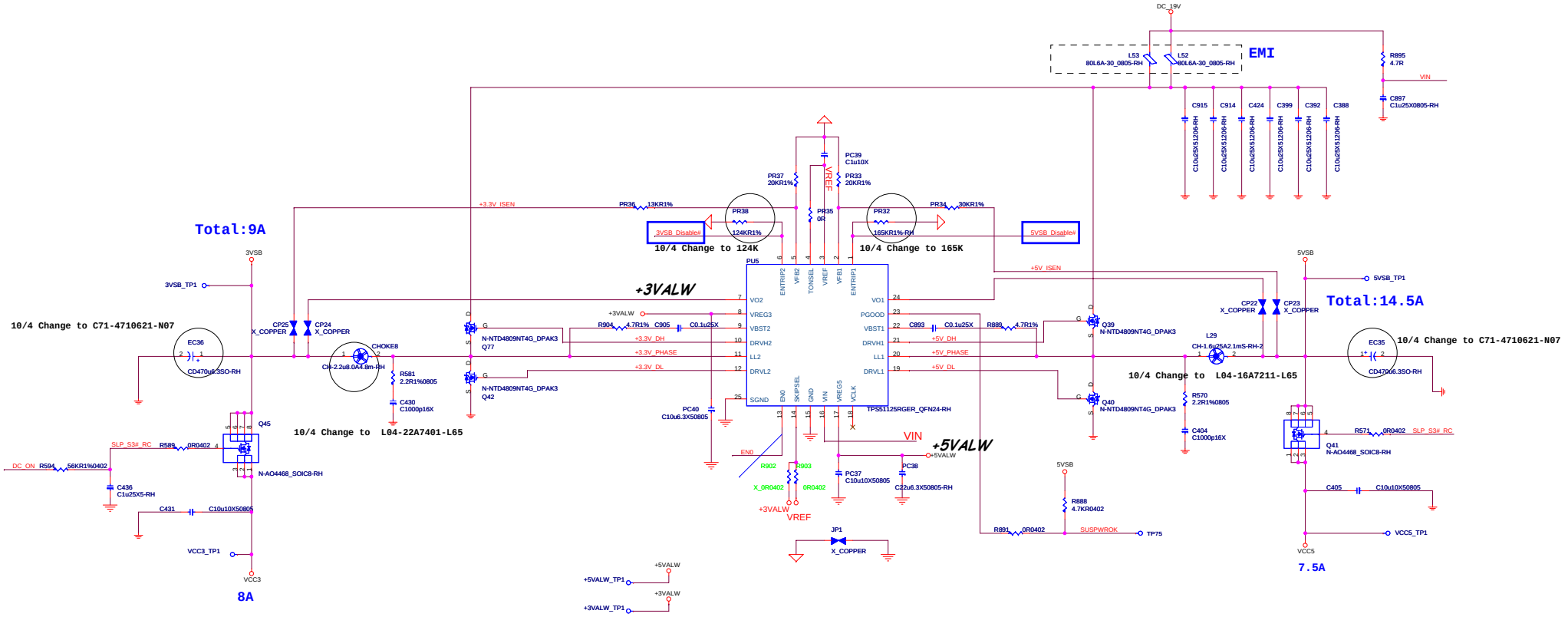
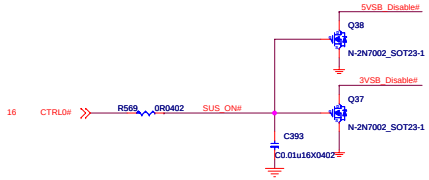
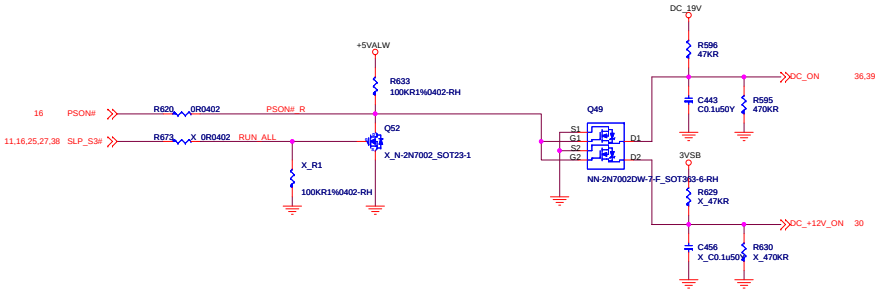
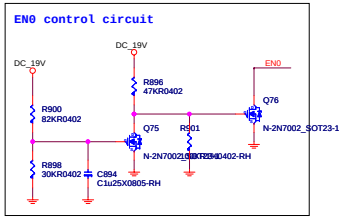


EN0 open: LDO on and turn on switcher channel

EUP Function.







MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size: Custom	Document Description: System Power VCC3 / VCC5		Rev: 1.1
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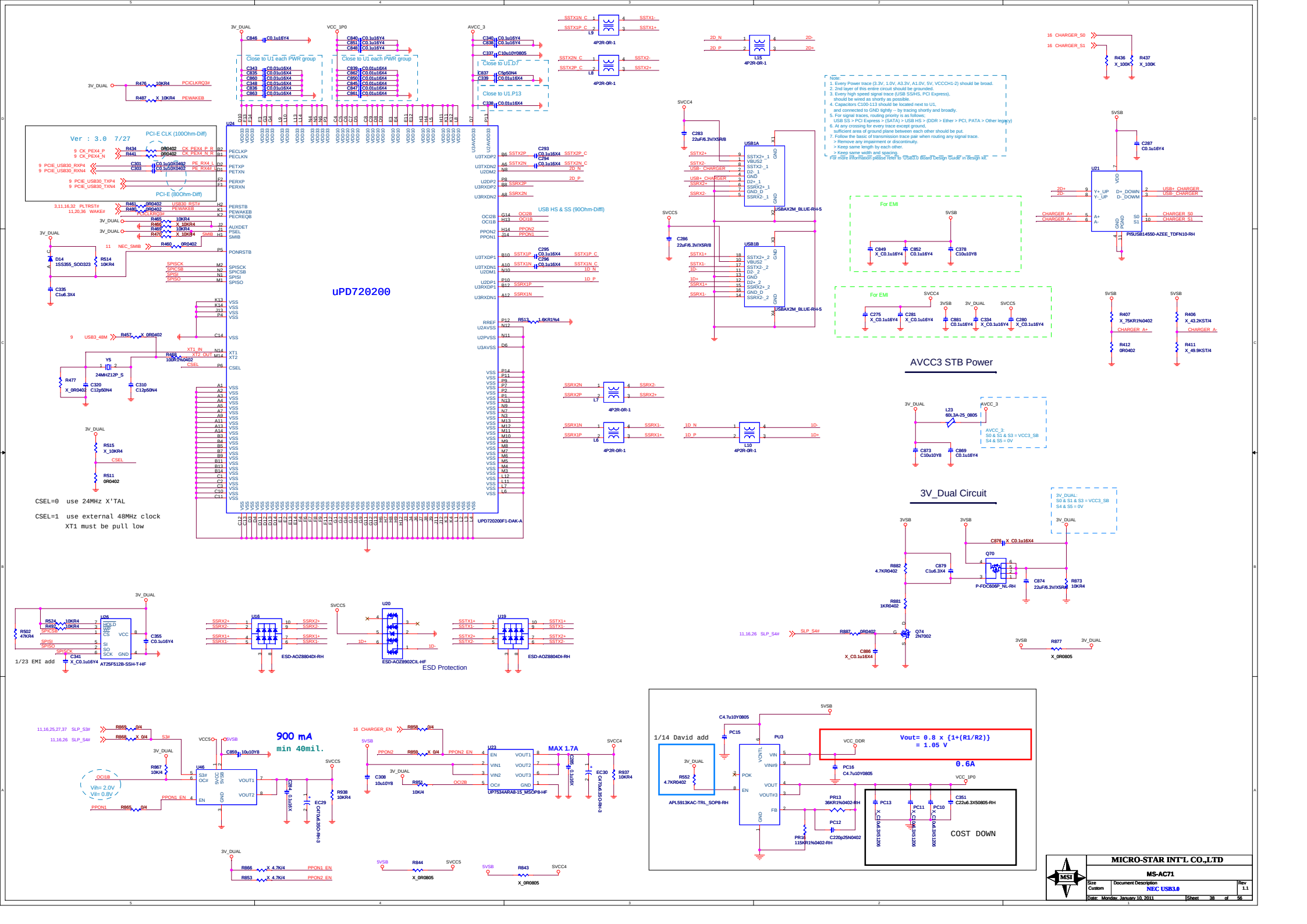
uPD720200
Ver : 3.0 7/27
PCI-E CLK (100Ohm-Diff)
PCI-E (80Ohm-Diff)
USB HS & SS (90Ohm-Diff)
CSEL=0 use 24MHz X'TAL
CSEL=1 use external 48MHz clock
XT1 must be pull low
1/23 EMI add
ESD Protection
AVCC3 STB Power
3V_Dual Circuit
1/14 David add
900 mA
min 40mil.
MAX 1.7A
Vout= 0.8 x {1+(R1/R2)}
= 1.05 V
0.6A
COST DOWN
For EMI
Close to U1 each PWR group
Close to U1.D7
Close to U1.P13
Note:
1. Every Power trace (3.3V, 1.0V, A3.3V, A1.0V, 5V, VCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows; USB SS > PCI Express > (SATA) > USB HS > (DDR > Ether > PCI, PATA > Other legacy)
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.
For more information please refer to "USB3.0 Board Design Guide" in design kit.
MICRO-STAR INT'L CO.,LTD
MS-AC71
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Document Description: NEC USB3.0
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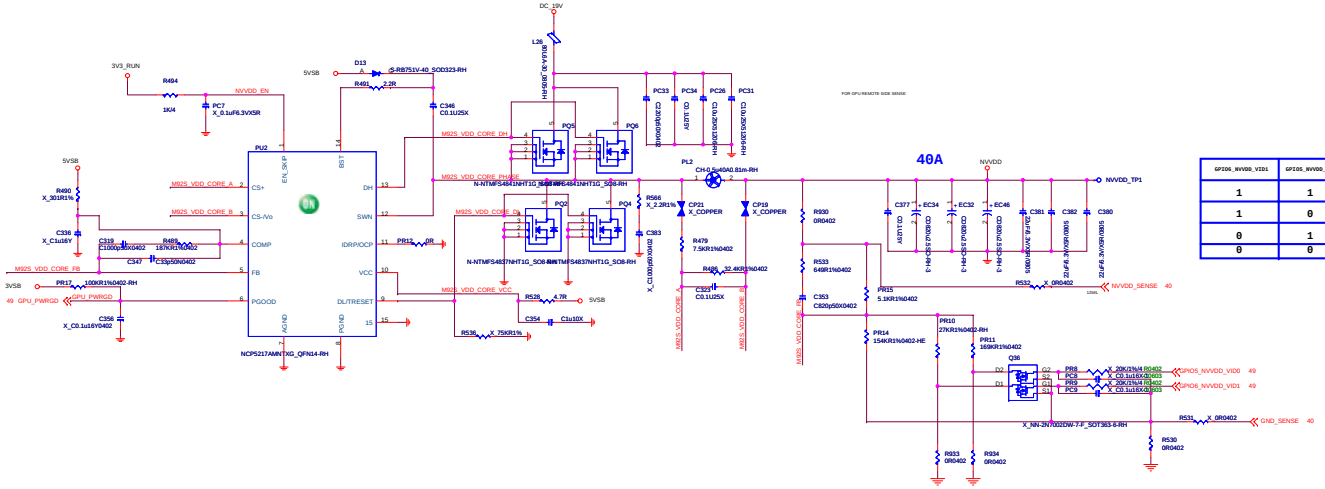
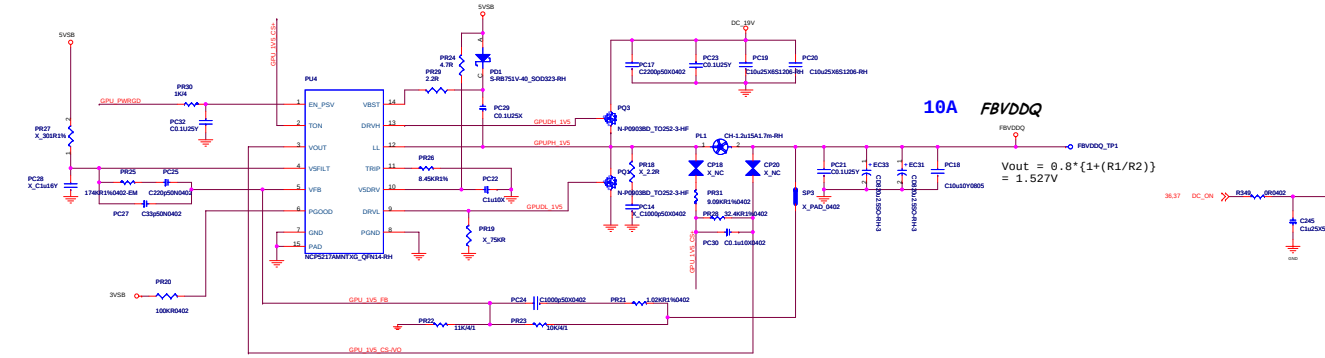
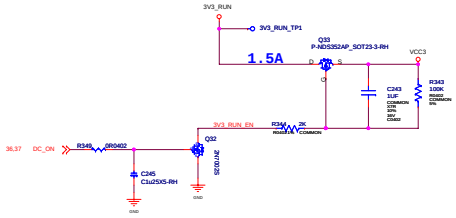
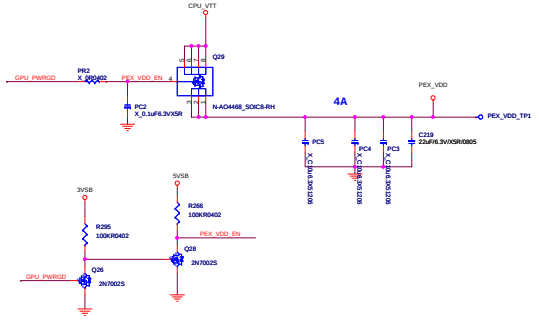
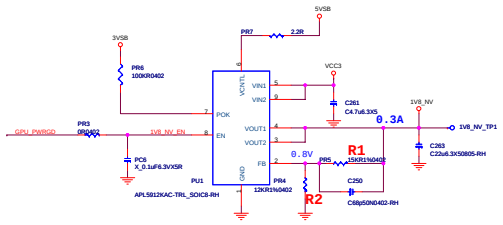


GPIO6_NVVDD_VID1	GPIO5_NVVDD_VID0	N12P-GS
1	1	1.000V
1	0	0.975V
0	1	0.850V
0	0	0.825V









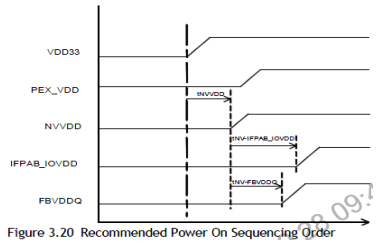


Figure 3.20 Recommended Power On Sequencing Order

MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: GPU Power - NCP5388	Rev: 1.1
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G1A

BGA973_H2_1
COMMON

1/16 PCI_EXPRESS

PEX_IOVDD AK16
PEX_IOVDD AK17
PEX_IOVDD AK21
PEX_IOVDD AK24
PEX_IOVDD AK27

PEX_IOVDDQ AG11
PEX_IOVDDQ AG12
PEX_IOVDDQ AG13
PEX_IOVDDQ AG15
PEX_IOVDDQ AG16
PEX_IOVDDQ AG17
PEX_IOVDDQ AG18
PEX_IOVDDQ AG22
PEX_IOVDDQ AG23
PEX_IOVDDQ AG24

PEX_IOVDDQ AG25
PEX_IOVDDQ AG26
PEX_IOVDDQ AJ14
PEX_IOVDDQ AJ15
PEX_IOVDDQ AJ19
PEX_IOVDDQ AJ21
PEX_IOVDDQ AJ22
PEX_IOVDDQ AJ24
PEX_IOVDDQ AJ25
PEX_IOVDDQ AJ27
PEX_IOVDDQ AK18
PEX_IOVDDQ AK20
PEX_IOVDDQ AK23
PEX_IOVDDQ AK26
PEX_IOVDDQ AL16

C238 0.1UF 6.3V 10% X7R C0402 COMMON
C757 0.1UF 6.3V 10% X7R C0402 COMMON
C742 1UF 6.3V 10% X7R C0603 COMMON
C743 1UF 6.3V 10% X7R C0603 COMMON
Place near GPU balls
C225 4.7UF 6.3V 20% X5R C0603 COMMON
C230 10UF 6.3V 20% X5R C0805_67 COMMON
Place close to GPU
PEX_VDD
C703 C22u6.3X50805-RH
NVIDIA suggestion. (20100827)

C752 0.1UF 6.3V 10% X7R C0402 COMMON
C741 0.1UF 6.3V 10% X7R C0402 COMMON
C751 1UF 6.3V 10% X7R C0603 COMMON
C758 1UF 6.3V 10% X7R C0603 COMMON
Place near GPU balls
C682 4.7UF 6.3V 20% X5R C0603 COMMON
C684 10UF 6.3V 20% X5R C0805_67 COMMON
Place close to GPU
PEX_VDD
C227 C22u6.3X50805-RH
NVIDIA suggestion. (20100827)

16 PLTRST#_GPU → AM16 PEX_RST
PEG_CLKREQ_R → AR13 PEX_CLKREQ
R323 X_0R0402 R0402 +0.05R DNI
R324 100K 5% R0402 COMMON
3V3_RUN

NV_CRITICAL_NET NV_IMPEDANCE DIFF_PAIR
R736 X_200R1%0402 R0402 DNI 90DIFF 1 PEX_TSTCLK_OUT → PEX_TSTCLK_OUT AJ17 PEX_TSTCLK_OUT
90DIFF 1 PEX_TSTCLK_OUT* → PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK_OUT

9 CLK_MXM_PCIE → AR16 PEX_REFCLK
9 CLK_MXM_PCIE# → AR17 PEX_REFCLK

3 PEG_RX0P	C0.1u10X0402	C708 C_PEG_RX0P	AL17	PEX_TX0
3 PEG_RX0N	C0.1u10X0402	C709 C_PEG_RX0N	AM17	PEX_TX0
3 PEG_TX0P			AP17	PEX_RX0
3 PEG_TX0N			AN17	PEX_RX0
3 PEG_RX1P	C0.1u10X0402	C687 C_PEG_RX1P	AM18	PEX_TX1
3 PEG_RX1N	C0.1u10X0402	C688 C_PEG_RX1N	AM19	PEX_TX1
3 PEG_TX1P			AN19	PEX_RX1
3 PEG_TX1N			AP19	PEX_RX1
3 PEG_RX2P	C0.1u10X0402	C710 C_PEG_RX2P	AL19	PEX_TX2
3 PEG_RX2N	C0.1u10X0402	C711 C_PEG_RX2N	AK19	PEX_TX2
3 PEG_TX2P			AR19	PEX_RX2
3 PEG_TX2N			AR20	PEX_RX2
3 PEG_RX3P	C0.1u10X0402	C689 C_PEG_RX3P	AL20	PEX_TX3
3 PEG_RX3N	C0.1u10X0402	C690 C_PEG_RX3N	AM20	PEX_TX3
3 PEG_TX3P			AP20	PEX_RX3
3 PEG_TX3N			AN20	PEX_RX3
3 PEG_RX4P	C0.1u10X0402	C712 C_PEG_RX4P	AM21	PEX_TX4
3 PEG_RX4N	C0.1u10X0402	C713 C_PEG_RX4N	AM22	PEX_TX4
3 PEG_TX4P			AN22	PEX_RX4
3 PEG_TX4N			AP22	PEX_RX4
3 PEG_RX5P	C0.1u10X0402	C691 C_PEG_RX5P	AL22	PEX_TX5
3 PEG_RX5N	C0.1u10X0402	C692 C_PEG_RX5N	AK22	PEX_TX5
3 PEG_TX5P			AR22	PEX_RX5
3 PEG_TX5N			AR23	PEX_RX5
3 PEG_RX6P	C0.1u10X0402	C714 C_PEG_RX6P	AL23	PEX_TX6
3 PEG_RX6N	C0.1u10X0402	C715 C_PEG_RX6N	AM23	PEX_TX6
3 PEG_TX6P			AP23	PEX_RX6
3 PEG_TX6N			AN23	PEX_RX6
3 PEG_RX7P	C0.1u10X0402	C693 C_PEG_RX7P	AM24	PEX_TX7
3 PEG_RX7N	C0.1u10X0402	C694 C_PEG_RX7N	AM25	PEX_TX7
3 PEG_TX7P			AN25	PEX_RX7
3 PEG_TX7N			AP25	PEX_RX7
3 PEG_RX8P	C0.1u10X0402	C716 C_PEG_RX8P	AL25	PEX_TX8
3 PEG_RX8N	C0.1u10X0402	C717 C_PEG_RX8N	AK25	PEX_TX8
3 PEG_TX8P			AR25	PEX_RX8
3 PEG_TX8N			AR26	PEX_RX8
3 PEG_RX9P	C0.1u10X0402	C695 C_PEG_RX9P	AL26	PEX_TX9
3 PEG_RX9N	C0.1u10X0402	C696 C_PEG_RX9N	AM26	PEX_TX9
3 PEG_TX9P			AP26	PEX_RX9
3 PEG_TX9N			AN26	PEX_RX9
3 PEG_RX10P	C0.1u10X0402	C718 C_PEG_RX10P	AM27	PEX_TX10
3 PEG_RX10N	C0.1u10X0402	C719 C_PEG_RX10N	AM28	PEX_TX10
3 PEG_TX10P			AN28	PEX_RX10
3 PEG_TX10N			AP28	PEX_RX10
3 PEG_RX11P	C0.1u10X0402	C697 C_PEG_RX11P	AL28	PEX_TX11
3 PEG_RX11N	C0.1u10X0402	C698 C_PEG_RX11N	AK28	PEX_TX11
3 PEG_TX11P			AR28	PEX_RX11
3 PEG_TX11N			AR29	PEX_RX11
3 PEG_RX12P	C0.1u10X0402	C720 C_PEG_RX12P	AK29	PEX_TX12
3 PEG_RX12N	C0.1u10X0402	C721 C_PEG_RX12N	AL29	PEX_TX12
3 PEG_TX12P			AP29	PEX_RX12
3 PEG_TX12N			AN29	PEX_RX12
3 PEG_RX13P	C0.1u10X0402	C699 C_PEG_RX13P	AM29	PEX_TX13
3 PEG_RX13N	C0.1u10X0402	C700 C_PEG_RX13N	AM30	PEX_TX13
3 PEG_TX13P			AN31	PEX_RX13
3 PEG_TX13N			AP31	PEX_RX13
3 PEG_RX14P	C0.1u10X0402	C722 C_PEG_RX14P	AM31	PEX_TX14
3 PEG_RX14N	C0.1u10X0402	C723 C_PEG_RX14N	AM32	PEX_TX14
3 PEG_TX14P			AR31	PEX_RX14
3 PEG_TX14N			AR32	PEX_RX14
3 PEG_RX15P	C0.1u10X0402	C701 C_PEG_RX15P	AN32	PEX_TX15
3 PEG_RX15N	C0.1u10X0402	C702 C_PEG_RX15N	AP32	PEX_TX15
3 PEG_TX15P			AR34	PEX_RX15
3 PEG_TX15N			AP34	PEX_RX15

PEX_SVDD_3V3 AG19
GF108 PEX_SVDD_3V3_NC F7
GT21X PEX_SVDD_3V3

C756 0.1UF 6.3V 10% X7R C0402 COMMON
C842 0.1UF 6.3V 10% X7R C0402 COMMON
C841 4.7UF 6.3V 20% X5R C0603 COMMON
Place near GPU balls
R847 X_0R0402 R0402 +0.05R COMMON
R846 0R0402 R0402 0.05R COMMON
3V3_RUN
PEX_VDD

NC A2, A7, AA4, AB4, AB7, AC5, AD6, AF6, AG6, AJ5, AK15, AL7, B7, C7, D5, D6, D7, E5, E7, E4, G5, G32, P6, U7, V6, Y4

Co-lay GB2b-128 and GB2-128.
Stuff for GB2b-128.

R541 X_20KR1%0402 R535 X_20KR1%0402 3V3_RUN STRAP4
R540 X_20KR1%0402 R534 X_20KR1%0402 3V3_RUN STRAP3
PGOOD R473 X_10K COMMON 1% R0402
MULTI_STRAP_REF2_GND R408 X_40.2K 1%R0402 COMMON
GND

VDD33 J10, J11, J12, J13, J9

C820 0.1UF 6.3V 10% X7R C0402 COMMON
C821 0.1UF 6.3V 10% X7R C0402 COMMON
C822 0.1UF 6.3V 10% X7R C0402 COMMON
Place near GPU balls
C274 1UF 6.3V 10% X5R C0402 COMMON
C270 4.7UF 6.3V 20% X5R C0603 COMMON
Place close to GPU
3V3_RUN

VDD_SENSE D35
VDD_SENSE P7
VDD_SENSE AD20
GND_SENSE AD19
GND_SENSE R7
GND_SENSE E35
NVVDD_SENSE
GND_SENSE
NVVDD_SENSE 39
GND_SENSE 39

Suggest PEX_PLVDD connect 10nH for N12M-GE

PEX_PLLVDD AG14
PEX_PLLVDD 16MIL
C731 0.1UF 6.3V 10% X7R C0402 COMMON
C732 0.1UF 6.3V 10% X7R C0402 COMMON
C733 0.1UF 6.3V 10% X7R C0402 COMMON
Place near GPU ball
C730 1UF 6.3V 10% X7R C0603 COMMON
C729 4.7UF 6.3V 20% X5R C0603 COMMON
LB2 120R@100MHz L0603 COMMON
N/A 25% FERRITE N/A 0.18R 500mA 500mA
PEX_VDD

GT21X GF108
RFU PEX_PLL_HVDD_NC AG20 SNN_PEX_RFU1 TP65
PEX_TERMP AG21 PEX_TERMP R790 2.49K R0402 1%
TESTMODE AP35 GPU_TESTMODE R321 10K R0402 5%
3V3_RUN 3.3V 16MIL 1.0A

MICRO-STAR INT'L CO.,LTD			
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Size: Custom	Document Description: GPU_PCIE		Rev: 1.1
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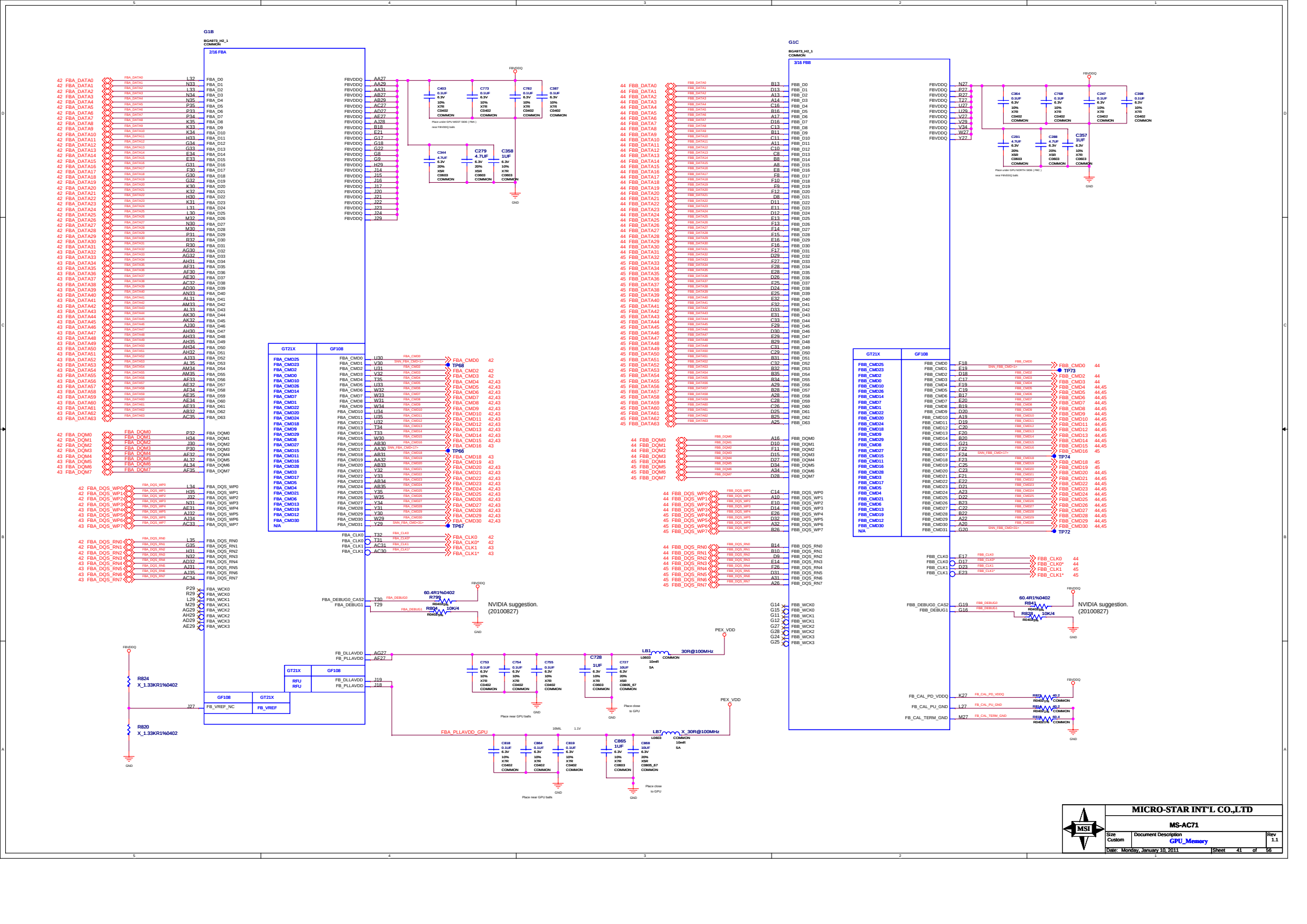
G1B
BGA973_H2_1
COMMON
2/16 FBA
G1C
BGA973_H2_1
COMMON
3/16 FBB
GT21X
GF108
NVIDIA suggestion.
(20100827)
NVIDIA suggestion.
(20100827)
MICRO-STAR INT'L CO.,LTD
MS-AC71
Size
Custom
Document Description
GPU_Memory
Rev
1.1
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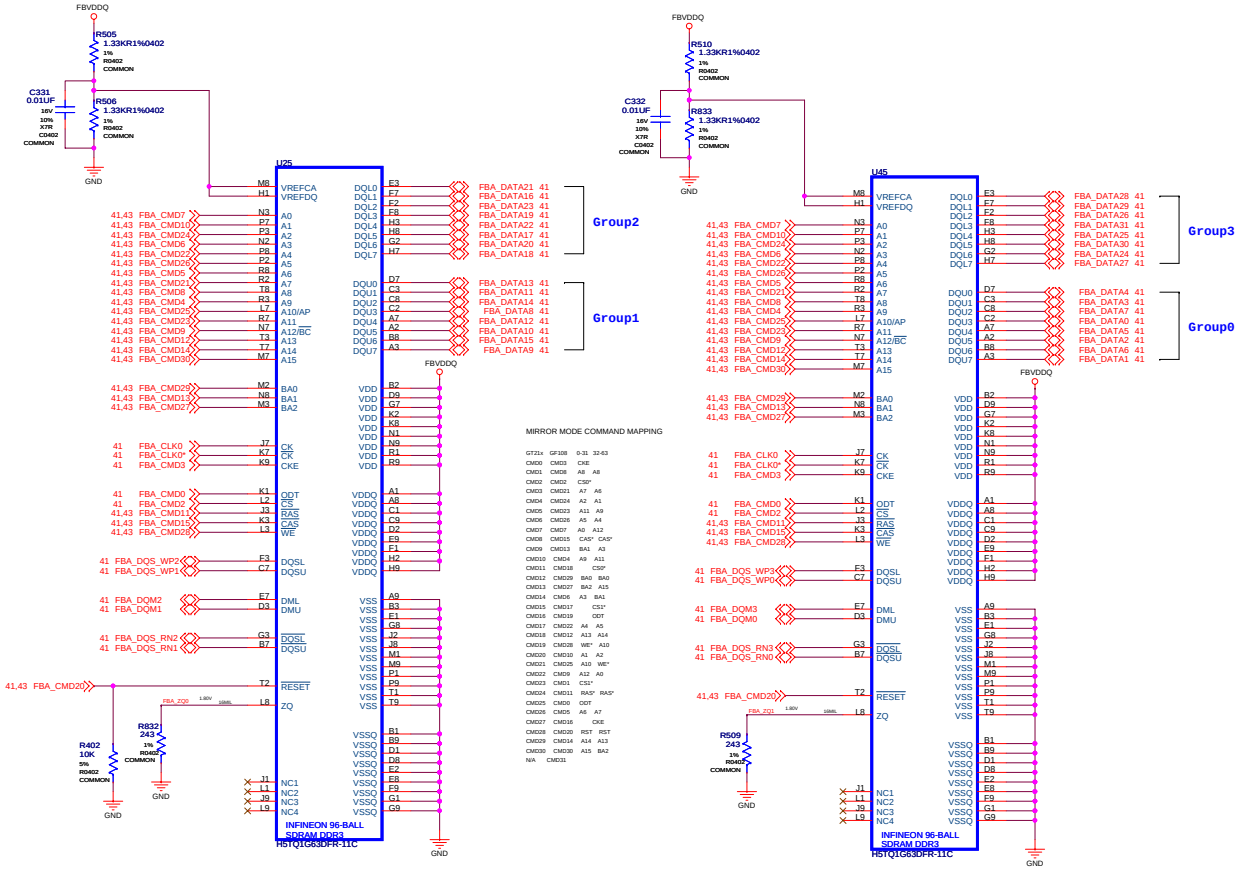
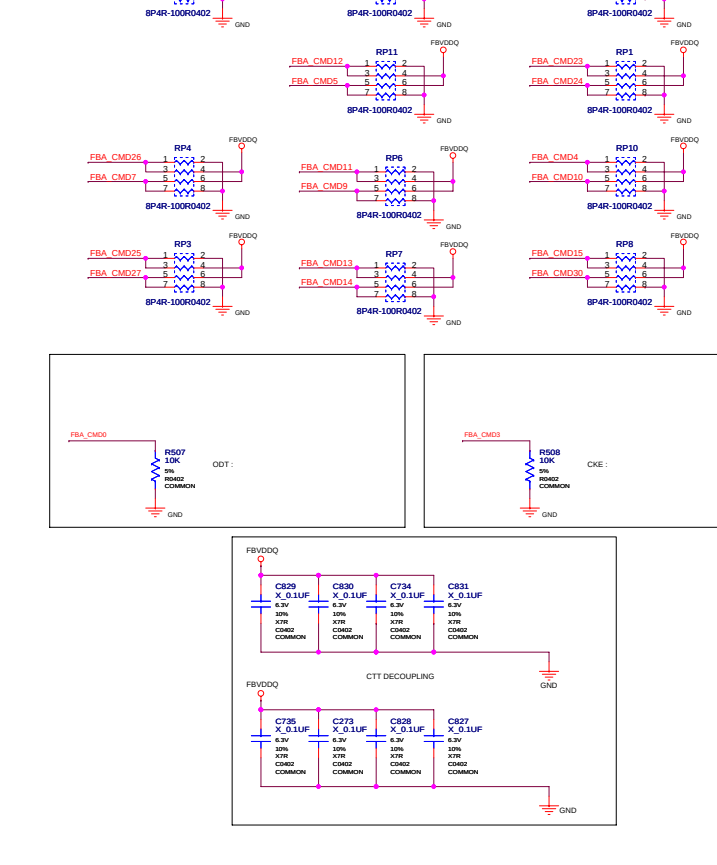
4. MEMORY PARTITION A LOWER 32 BITS





MEMORY PARTITION A SIGNAL CONSTRAINTS

FBA_CLK0	FBA_CLK0	1	80DIFF
FBA_CLK0*	FBA_CLK0	1	80DIFF
FBA_DQS_WP0	FBADQS0	1	80DIFF
FBA_DQS_RN0	FBADQS0	1	80DIFF
FBA_DQS_WP1	FBADQS1	1	80DIFF
FBA_DQS_RN1	FBADQS1	1	80DIFF
FBA_DQS_WP2	FBADQS2	1	80DIFF
FBA_DQS_RN2	FBADQS2	1	80DIFF
FBA_DQS_WP3	FBADQS3	1	80DIFF
FBA_DQS_RN3	FBADQS3	1	80DIFF

MICRO-STAR INT'L CO.,LTD

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Custom	VRAM-A_LOWER	1.1

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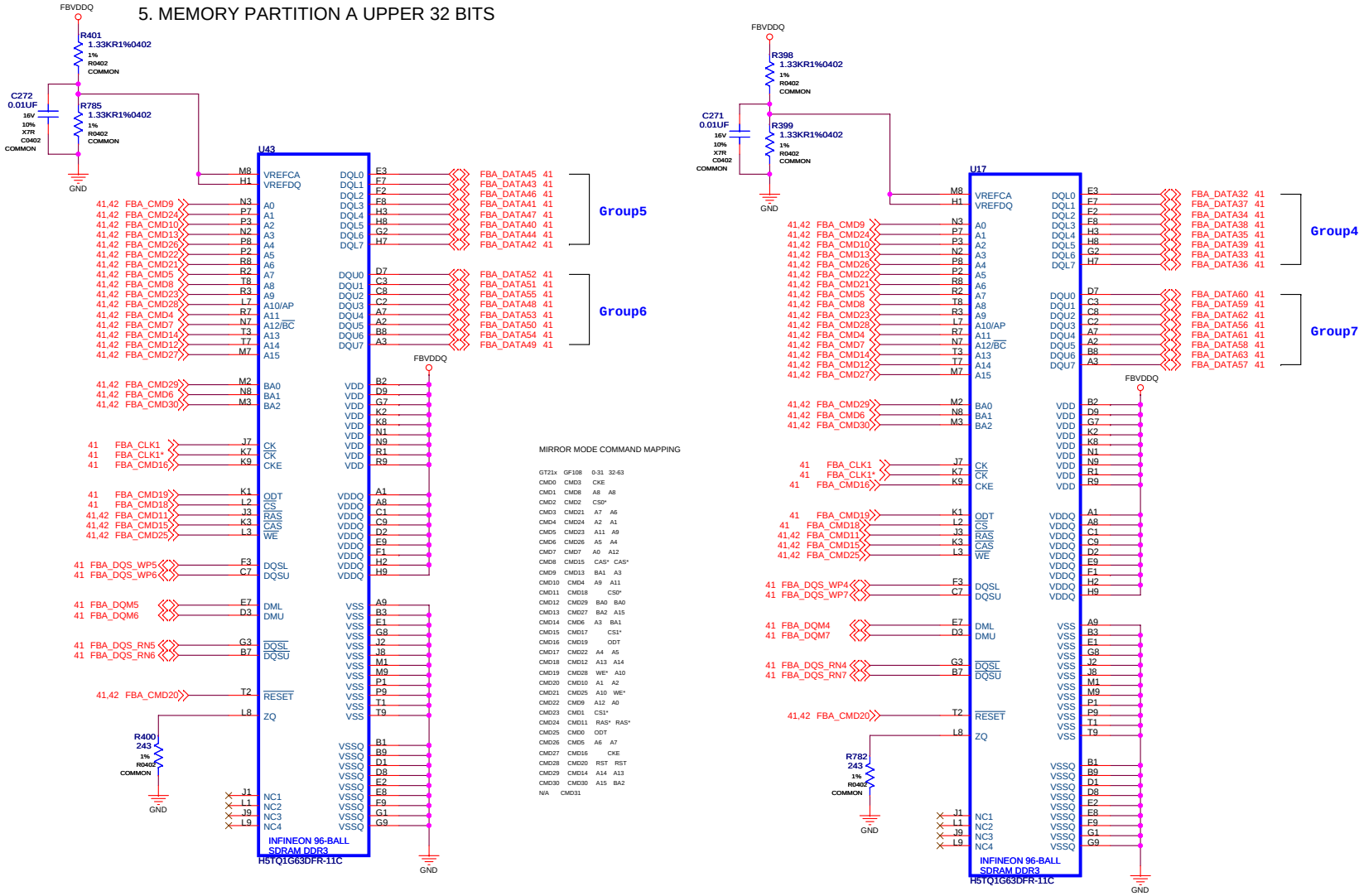
5. MEMORY PARTITION A UPPER 32 BITS



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Size: Custom	Document Description: VRAM-A_UPPER		Rev: 1.1
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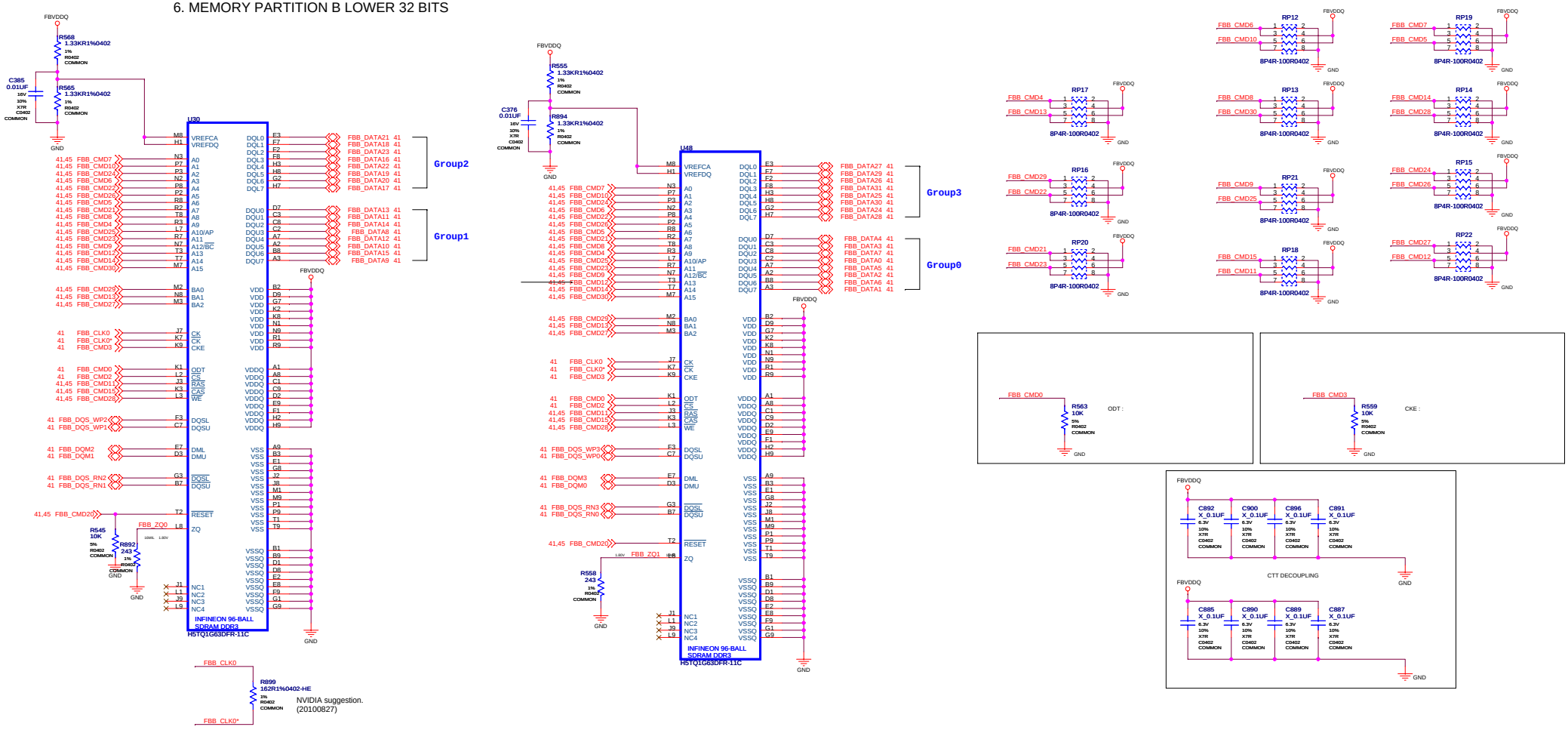
6. MEMORY PARTITION B LOWER 32 BITS



MEMORY PARTITION C SIGNAL CONSTRAINTS

NET	DIFFPAIR	CRITICAL	IMPEDANCE
FBB_CLK0	FBB_CLK0	1	80OHM
FBB_CLK0*	FBB_CLK0	1	80OHM
FBB_DQS_WP0	FBBDQS0	1	80OHM
FBB_DQS_RN0	FBBDQS0	1	80OHM
FBB_DQS_WP1	FBBDQS1	1	80OHM
FBB_DQS_RN1	FBBDQS1	1	80OHM
FBB_DQS_WP2	FBBDQS2	1	80OHM
FBB_DQS_RN2	FBBDQS2	1	80OHM
FBB_DQS_WP3	FBBDQS3	1	80OHM
FBB_DQS_RN3	FBBDQS3	1	80OHM

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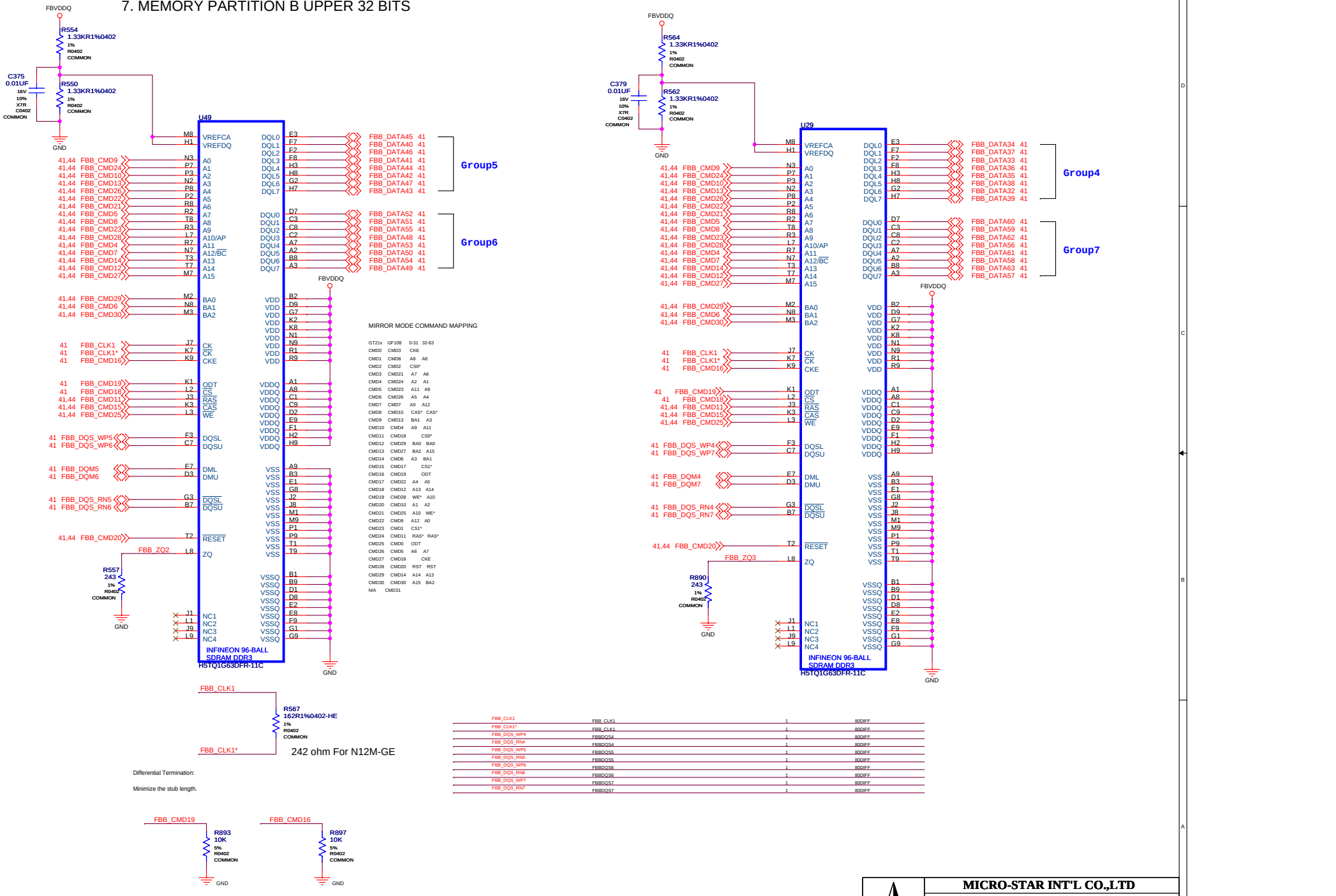
7. MEMORY PARTITION B UPPER 32 BITS



FBB_CLK1	FBB_CLK1	1	80DIFF
FBB_CLK1*	FBB_CLK1	1	80DIFF
FBB_DQS_WP4	FBBDQS4	1	80DIFF
FBB_DQS_RN4	FBBDQS4	1	80DIFF
FBB_DQS_WP5	FBBDQS5	1	80DIFF
FBB_DQS_RN5	FBBDQS5	1	80DIFF
FBB_DQS_WP6	FBBDQS6	1	80DIFF
FBB_DQS_RN6	FBBDQS6	1	80DIFF
FBB_DQS_WP7	FBBDQS7	1	80DIFF
FBB_DQS_RN7	FBBDQS7	1	80DIFF

GT21x	GF108	0-31	32-63
CMD0	CMD3	CKE	
CMD1	CMD8	A8	A8
CMD2	CMD2	CS0*	
CMD3	CMD21	A7	A6
CMD4	CMD24	A2	A1
CMD5	CMD23	A11	A9
CMD6	CMD26	A5	A4
CMD7	CMD7	A0	A12
CMD8	CMD15	CAS*	CAS*
CMD9	CMD13	BA1	A3
CMD10	CMD4	A9	A11
CMD11	CMD18		CS0*
CMD12	CMD29	BA0	BA0
CMD13	CMD27	BA2	A15
CMD14	CMD6	A3	BA1
CMD15	CMD17		CS1*
CMD16	CMD19		ODT
CMD17	CMD22	A4	A5
CMD18	CMD12	A13	A14
CMD19	CMD28	WE*	A10
CMD20	CMD10	A1	A2
CMD21	CMD25	A10	WE*
CMD22	CMD9	A12	A0
CMD23	CMD1	CS1*	
CMD24	CMD11	RAS*	RAS*
CMD25	CMD0	ODT	
CMD26	CMD5	A6	A7
CMD27	CMD16		CKE
CMD28	CMD20	RST	RST
CMD29	CMD14	A14	A13
CMD30	CMD30	A15	BA2
N/A	CMD31		

MICRO-STAR INT'L CO.,LTD			
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Size: Custom	Document Description: VRAM-A_UPPER		Rev: 1.1
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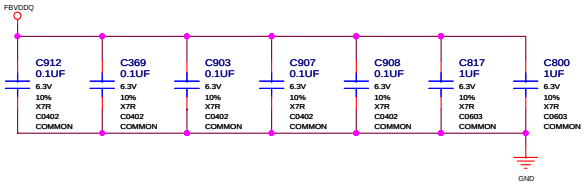
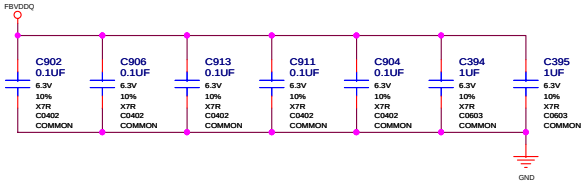
8. MEMORY DECOUPLING CAPS

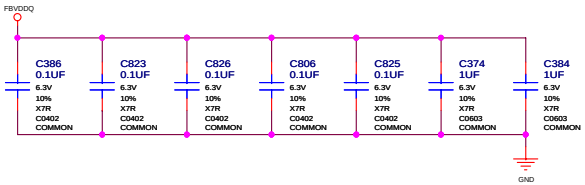
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 0-15



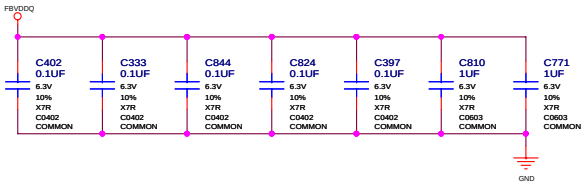
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 0-15



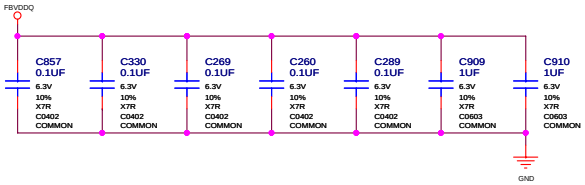
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A LOWER BITS 16-31



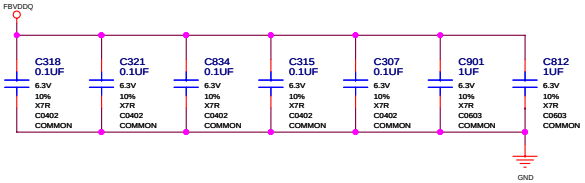
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B LOWER BITS 16-31



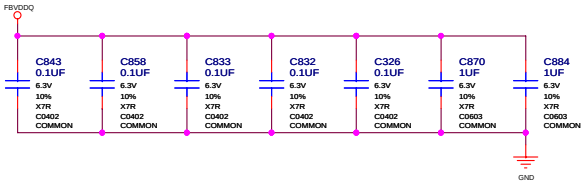
DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 32-47



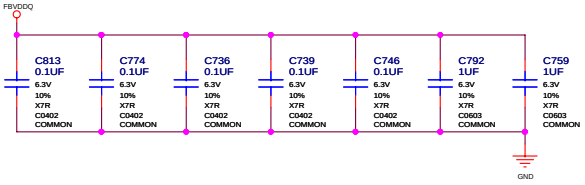
DECOUPLING CAPS FOR ONE MEMORY OF PARTION B UPPER BITS 32-47



DECOUPLING CAPS FOR ONE MEMORY OF PARTION A UPPER BITS 48-63



DECOUPLING CAPS FOR ONE MEMORY OF PARTION C UPPER BITS 48-63



MSI	MICRO-STAR INT'L CO.,LTD	
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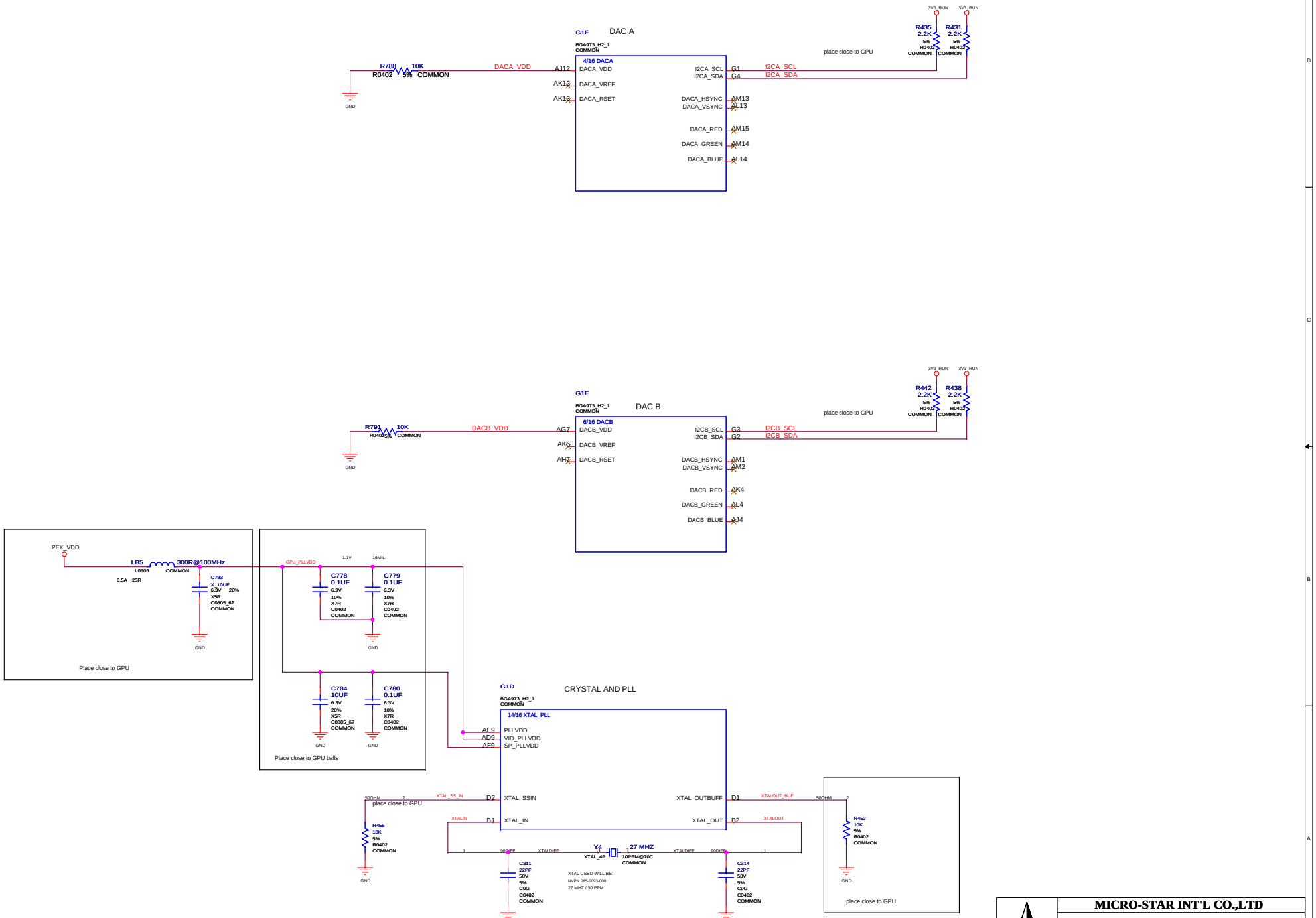

MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: GPU DAC/CRYSTAL	Rev: 1.1
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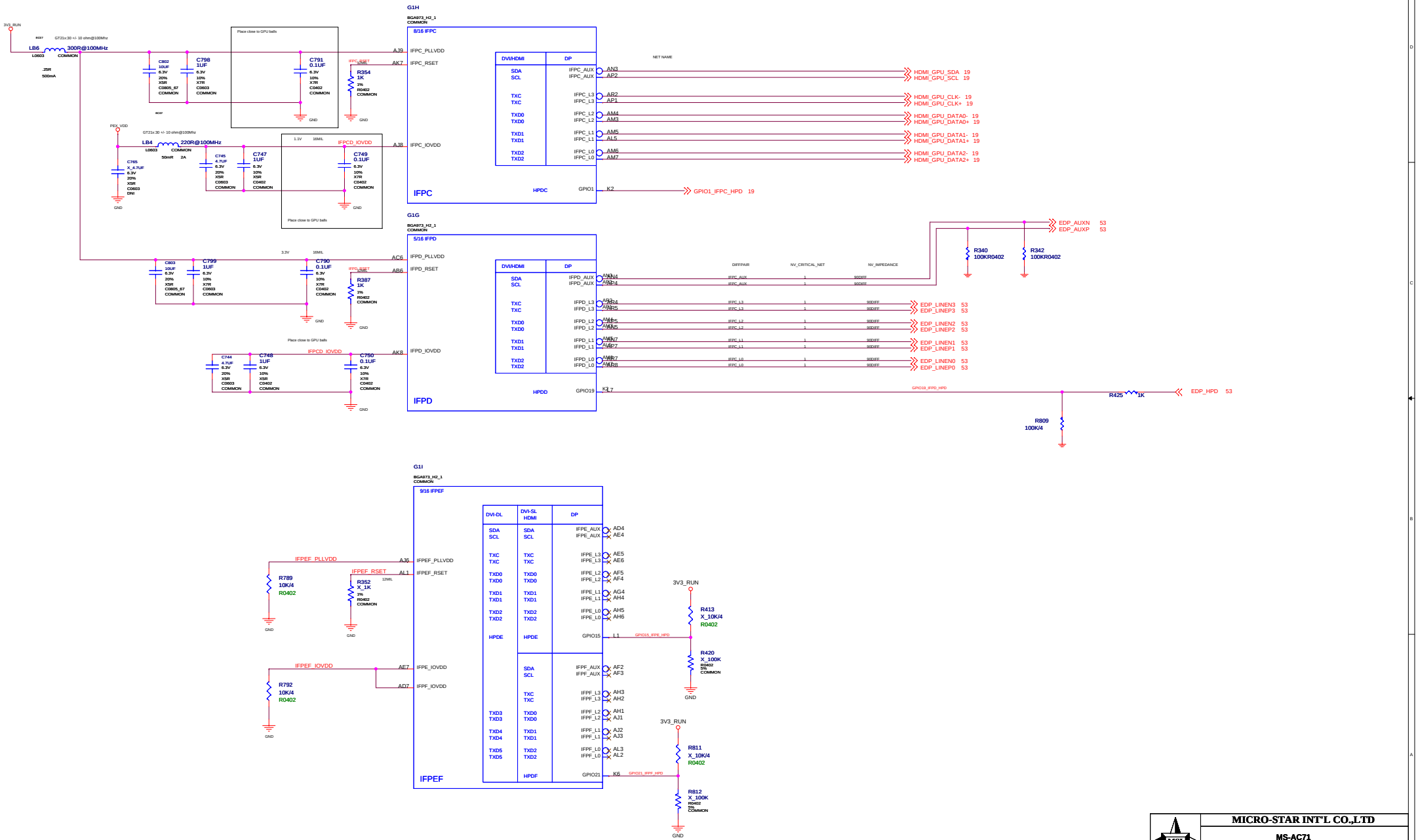
10. DP LINKS CD, LINK EF



MICRO-STAR INT'L CO.,LTD			
MS-AC71			
Size: Custom	Document Description: GPU DP_LINK		Rev: 1.1
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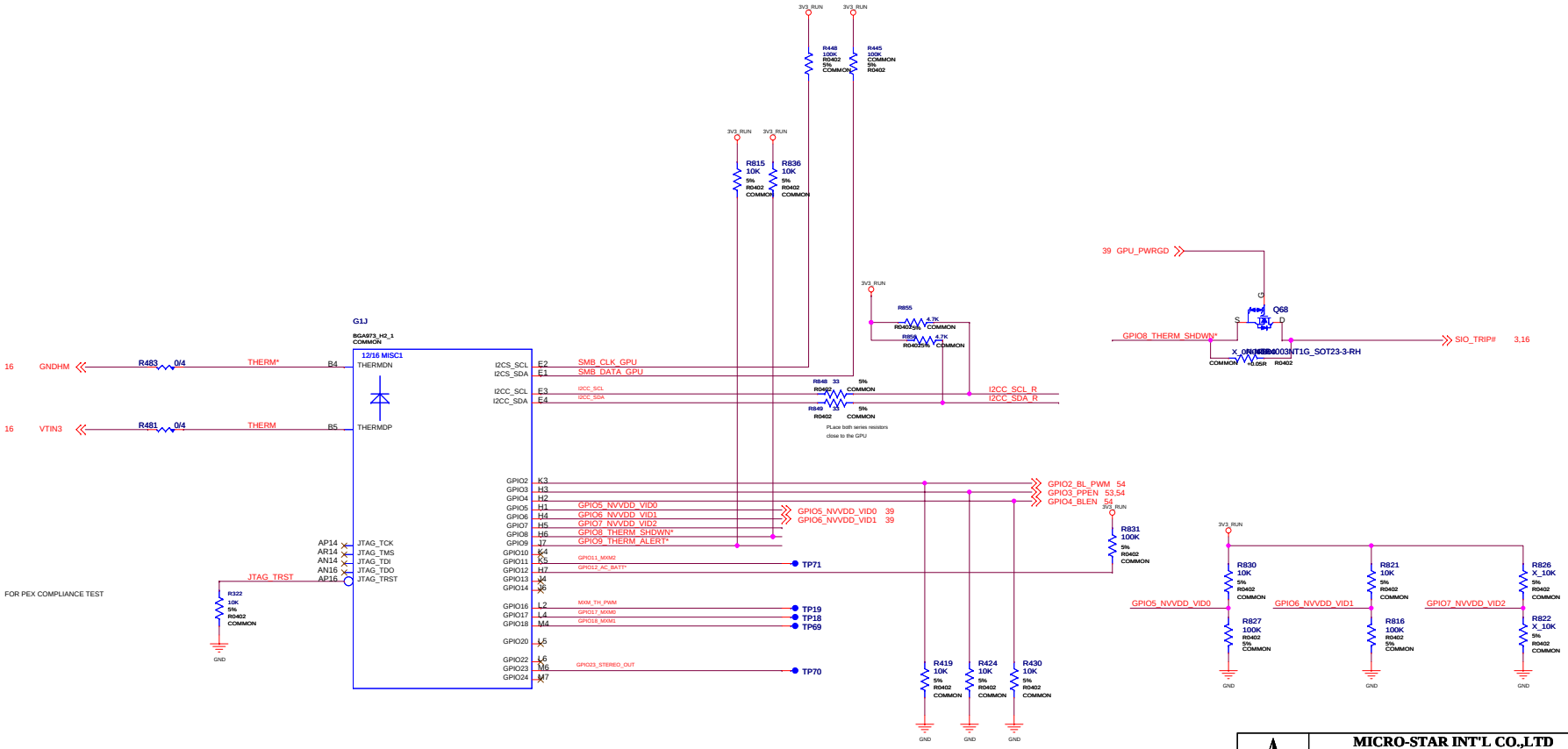
12. GPIO, JTAG, TEMP SENSOR, Info ROM



MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: GPU GPIO/JTAG/TEMP SENSOR	Rev: 1.1
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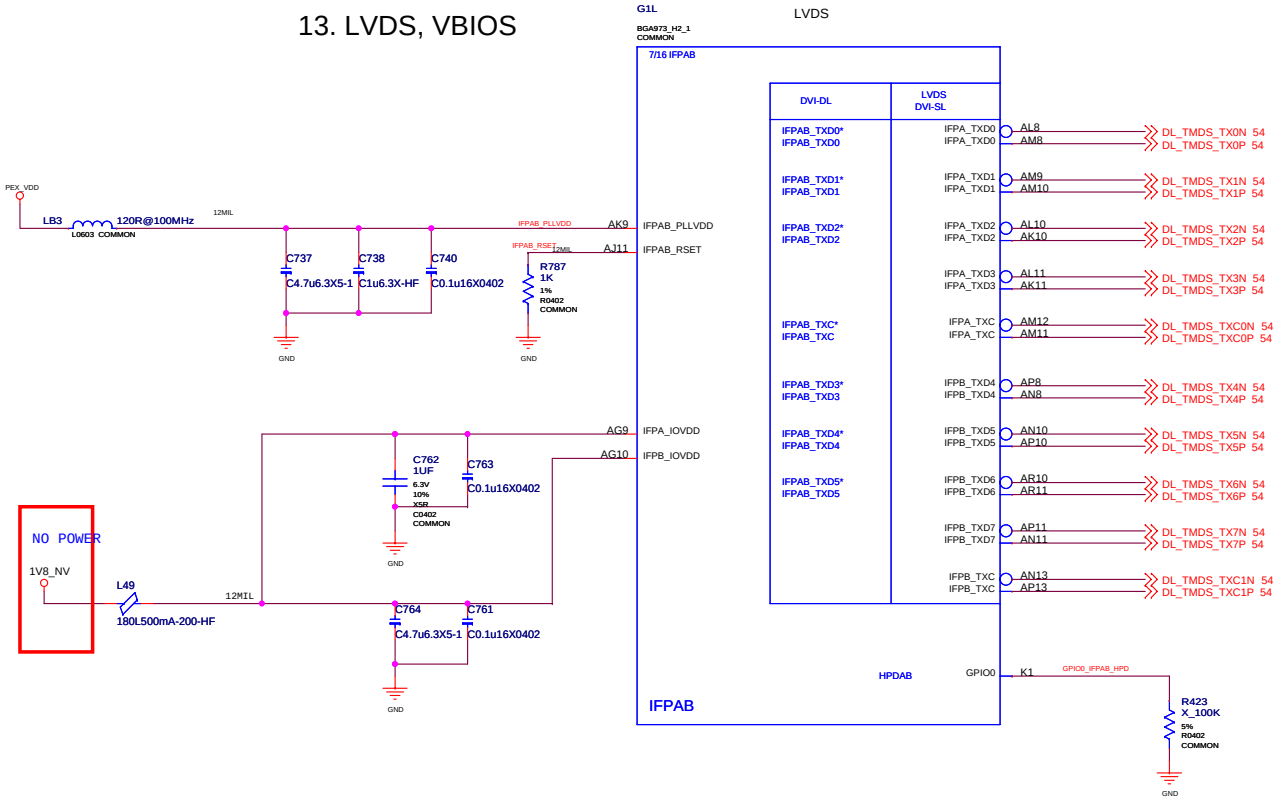
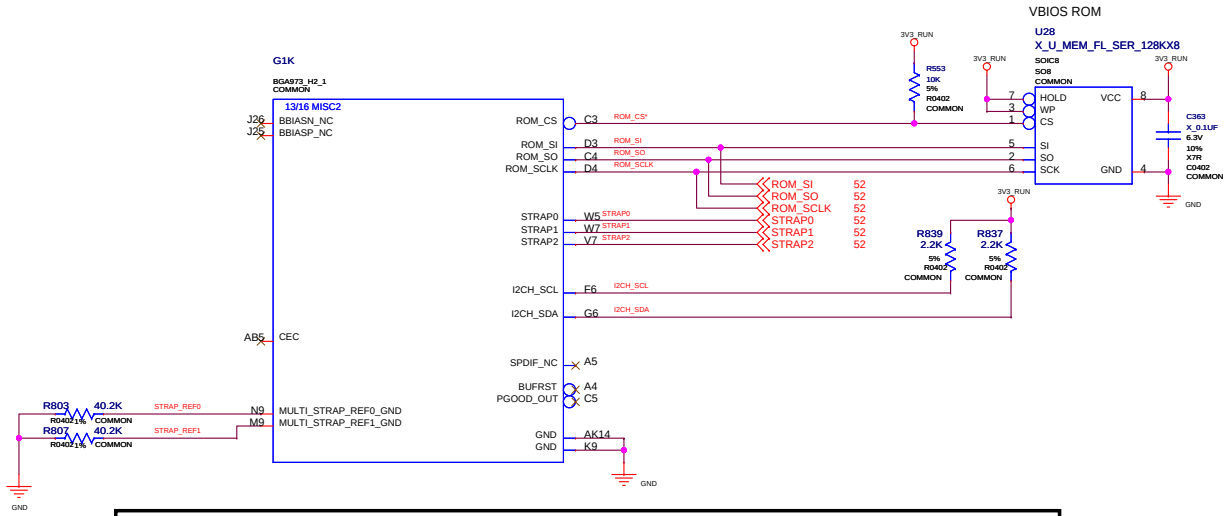
13. LVDS, VBIOS





Mode	Multi_strap_ref1_GND	Multi_strap_ref0_GND
Binary Production	40.2K 1% to GND	NC
Multi-Level	40.2K 1% to GND	40.2K 1% to GND

MICRO-STAR INT'L CO.,LTD		
MS-AC71		
Size: Custom	Document Description: GPU LVDS/VBIOS	Rev: 1.1
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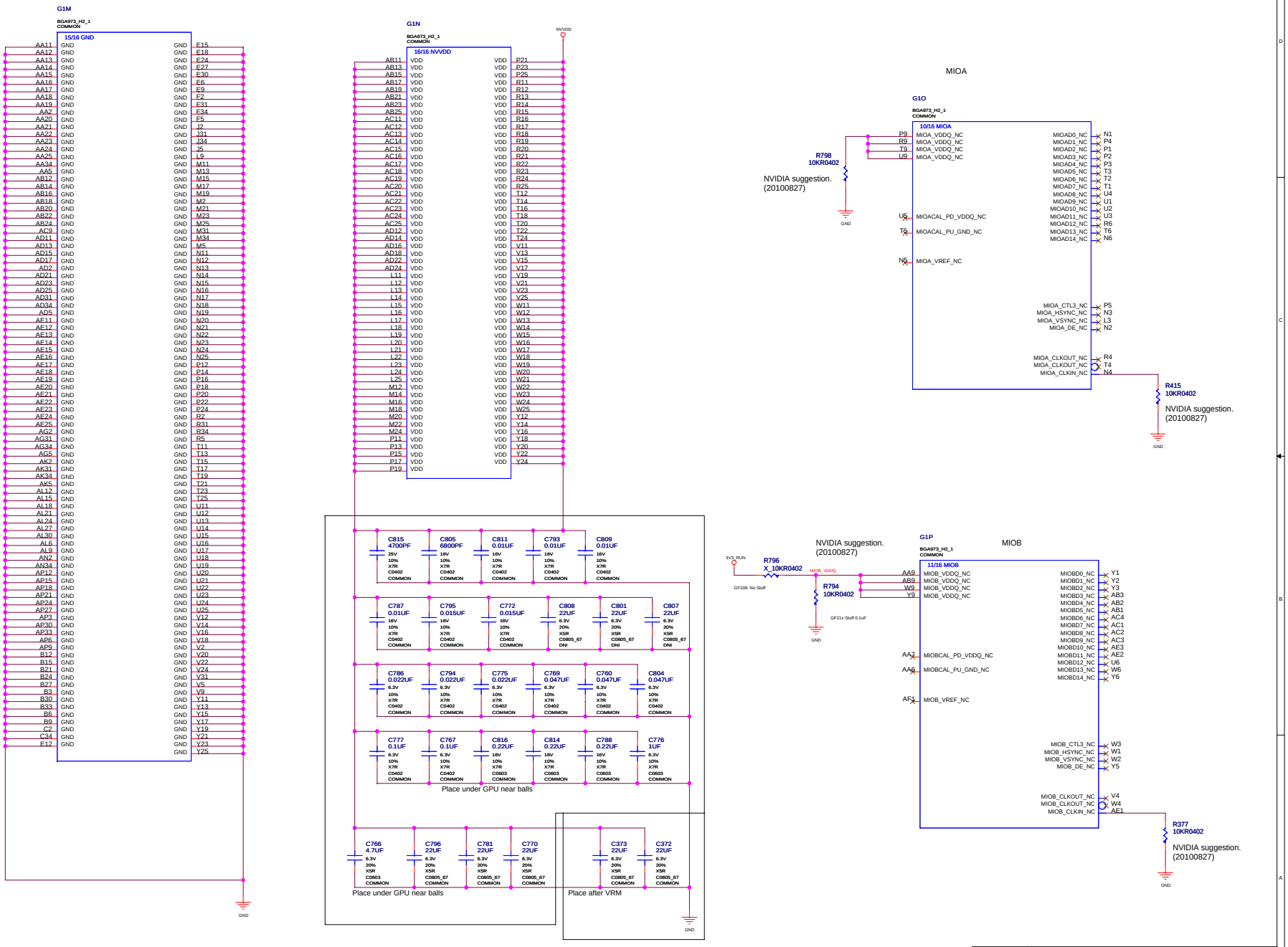
14. MIOA, MIOB, GPU VDD/DCPLNG/GND



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: GPU MIO/VDD Decoupling	Rev: 1.1
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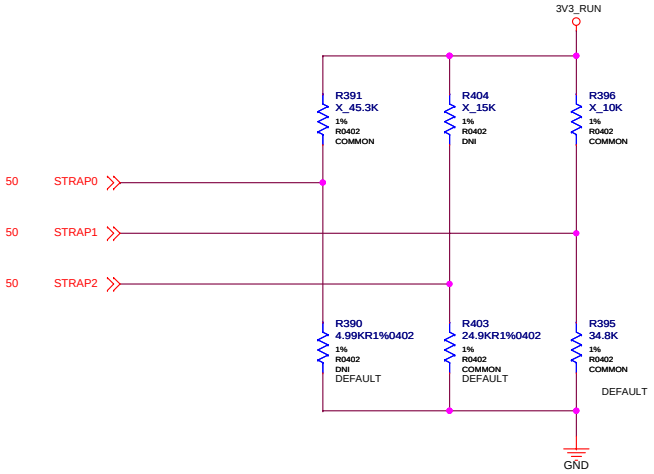
17. STRAPS, MOUNTING HOLES

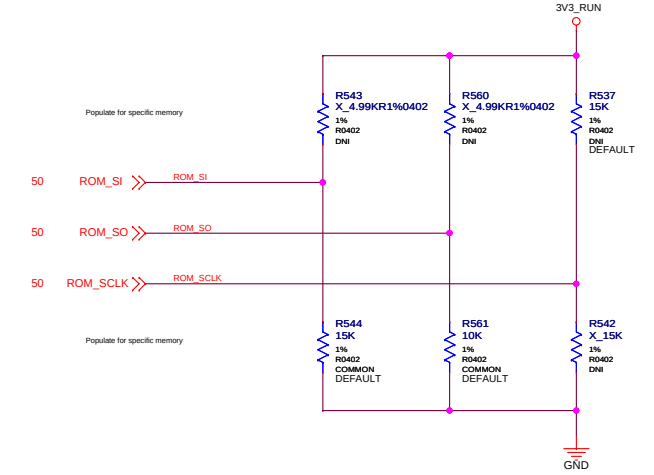
STRAP0 was defined to select LVDS panel, if EDID was saved through VBIOS,
PD 5K = 0000 (It means EDID save table 0)



STRAP0

STRAP1

STRAP2



ROM_SO

ROM_SI

ROM_SCLK

STRAP2 should 25K PD (N12P-GS: 0DF4) => 0100
15K PU (N12M-GE-B:0A7A) =>1010

USER_BIT0
USER_BIT1
USER_BIT2
USER_BIT3

Default All SKU(s):
0xF = 45K PU
LVDS Panel EDID Mode

3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3

Set at HW reset by the PEX_PADCFG Circuit
0x0: Desktop default (normal swing) - 5k PD
0x1: Mobile default (low swing) - 10k PD

PCDEVID_3:0] Definitions (Note Actual DEVID set also depends on PCI_DEVID_4)

PCI_DEVID_0
PCI_DEVID_1
PCI_DEVID_2
PCI_DEVID_3

GT218	GT216	GF108
1000 5K PU GT218-700	1000 5K PU GT216-600	0000 5K PD GF108-630
0100 25K PD GT218-730	0100 25K PD GT216-630	
	1100 25K PU GT216-640	
	1100 25K PU GT216-950	

VGA_DEVICE — 0: 3D DEVICE; 1: VGA DEVICE — Set at HW reset by the Device Detect Circuit

SMB_ALT_ADDR — 0: Thermal Sensor ADR = 0x9E

FB_0_BAR_SIZE — 0: Default

XCLK_417 — 0: Default

0x1 = 10K PD

RAM_CFG[3:0] Definitions

RAM_CFG_0
RAM_CFG_1
RAM_CFG_2
RAM_CFG_3

GF108 64Mx16
0000 5K PD Reserved
0001 10K PD Reserved
0010 15K PD HYNIX
0011 20K PD SAMSUNG

GT108 128Mx16
0100 25k PD Reserved
0101 30k PD Reserved
0110 35k PD HYNIX
0111 45k PD SAMSUNG

DEFAULT

0001 Reserved
0001 64Mx16 128-bit 10K PD Qimonda
0010 64Mx16 128-bit 15K PD Hynix
0011 64Mx16 128-bit 20K PD Samsung
0100 Reserved
0101 32Mx16 128-bit 30K PD Qimonda
0110 32Mx16 128-bit 35K PD Hynix
0111 32Mx16 128-bit 45K PD Samsung

* 32Mx16 MAY BE 64Mx16 run at 1/2 density

GT215/6

1001 Reserved
1001 64Mx16 64-bit 10K PU Qimonda
1010 64Mx16 64-bit 15K PU Hynix
1011 64Mx16 64-bit 20K PU Samsung
1100 Reserved
1101 128Mx16 64-bit 30K PU Qimonda
1110 128Mx16 64-bit 35K PU Hynix
1111 128Mx16 64-bit 45K PU Samsung

PEX_PLL_EN_TERM100 — 0: DISABLED

SLOT_CLK_CONFIG — 1: GPU and MCH COMMON REFCLK

SUB_VENDOR — 1: VBIOS ROM IS PRESENT

PCI_DEVID_EXT — 0: PCDEVID[4] = 0 or 1 (SKU Specific)

0x6 = 35K PD PCDEVID_EXT=0
0xE = 35K PU PCDEVID_EXT=1

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111

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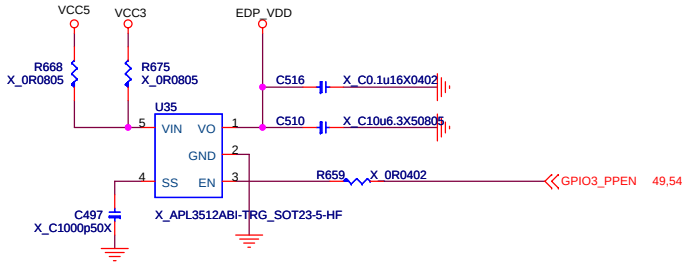
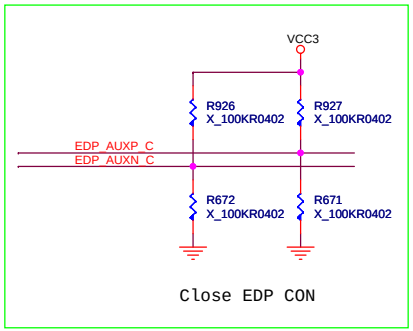
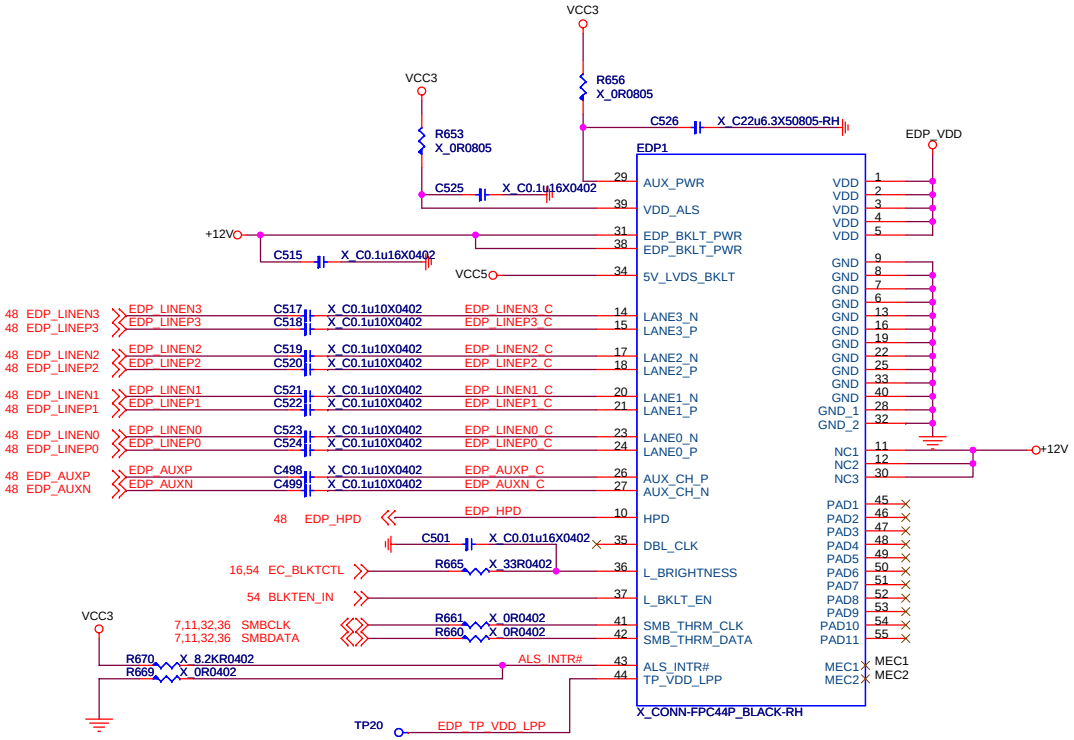
EDP POWER







MSI	MICRO-STAR INT'L CO.,LTD	
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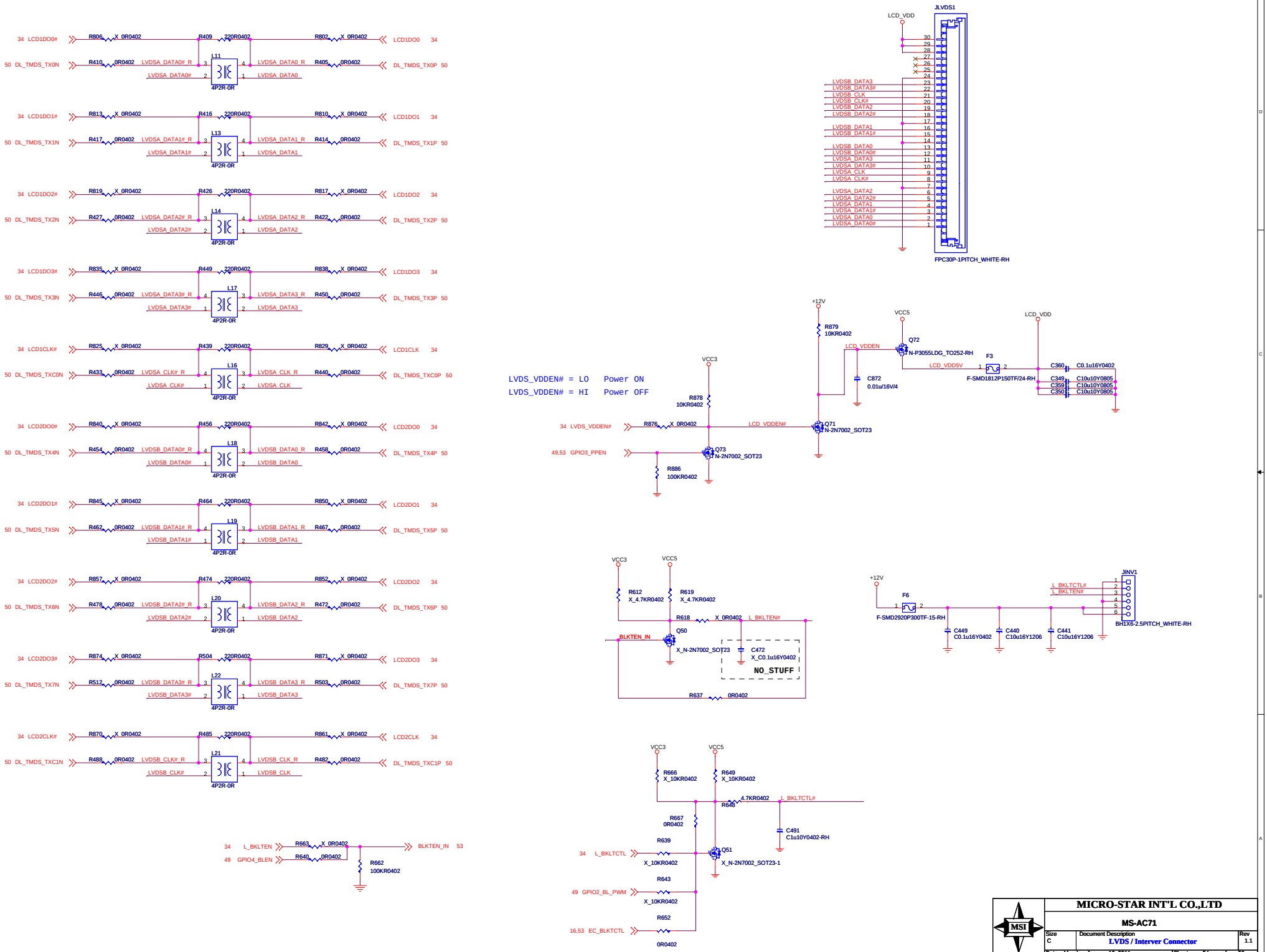
34 LCD1DO0# R806 X 0R0402 R409 220R0402 R802 X 0R0402 LCD1DO0 34
50 DL_TMDS_TX0N R410 0R0402 LVDSA_DATA0# R L11 LVDSA_DATA0# LVDSA_DATA0 LVDSA_DATA0_R R405 0R0402 DL_TMDS_TX0P 50
4P2R-0R
34 LCD1DO1# R813 X 0R0402 R416 220R0402 R810 X 0R0402 LCD1DO1 34
50 DL_TMDS_TX1N R417 0R0402 LVDSA_DATA1# R L13 LVDSA_DATA1# LVDSA_DATA1 LVDSA_DATA1_R R414 0R0402 DL_TMDS_TX1P 50
4P2R-0R
34 LCD1DO2# R819 X 0R0402 R426 220R0402 R817 X 0R0402 LCD1DO2 34
50 DL_TMDS_TX2N R427 0R0402 LVDSA_DATA2# R L14 LVDSA_DATA2# LVDSA_DATA2 LVDSA_DATA2_R R422 0R0402 DL_TMDS_TX2P 50
4P2R-0R
34 LCD1DO3# R835 X 0R0402 R449 220R0402 R838 X 0R0402 LCD1DO3 34
50 DL_TMDS_TX3N R446 0R0402 LVDSA_DATA3# R L17 LVDSA_DATA3# LVDSA_DATA3 LVDSA_DATA3_R R450 0R0402 DL_TMDS_TX3P 50
4P2R-0R
34 LCD1CLK# R825 X 0R0402 R439 220R0402 R829 X 0R0402 LCD1CLK 34
50 DL_TMDS_TXC0N R433 0R0402 LVDSA_CLK# R L16 LVDSA_CLK# LVDSA_CLK LVDSA_CLK_R R440 0R0402 DL_TMDS_TXC0P 50
4P2R-0R
34 LCD2DO0# R840 X 0R0402 R456 220R0402 R842 X 0R0402 LCD2DO0 34
50 DL_TMDS_TX4N R454 0R0402 LVDSB_DATA0# R L18 LVDSB_DATA0# LVDSB_DATA0 LVDSB_DATA0_R R458 0R0402 DL_TMDS_TX4P 50
4P2R-0R
34 LCD2DO1# R845 X 0R0402 R464 220R0402 R850 X 0R0402 LCD2DO1 34
50 DL_TMDS_TX5N R462 0R0402 LVDSB_DATA1# R L19 LVDSB_DATA1# LVDSB_DATA1 LVDSB_DATA1_R R467 0R0402 DL_TMDS_TX5P 50
4P2R-0R
34 LCD2DO2# R857 X 0R0402 R474 220R0402 R852 X 0R0402 LCD2DO2 34
50 DL_TMDS_TX6N R478 0R0402 LVDSB_DATA2# R L20 LVDSB_DATA2# LVDSB_DATA2 LVDSB_DATA2_R R472 0R0402 DL_TMDS_TX6P 50
4P2R-0R
34 LCD2DO3# R874 X 0R0402 R504 220R0402 R871 X 0R0402 LCD2DO3 34
50 DL_TMDS_TX7N R512 0R0402 LVDSB_DATA3# R L22 LVDSB_DATA3# LVDSB_DATA3 LVDSB_DATA3_R R503 0R0402 DL_TMDS_TX7P 50
4P2R-0R
34 LCD2CLK# R870 X 0R0402 R485 220R0402 R861 X 0R0402 LCD2CLK 34
50 DL_TMDS_TXC1N R488 0R0402 LVDSB_CLK# R L21 LVDSB_CLK# LVDSB_CLK LVDSB_CLK_R R482 0R0402 DL_TMDS_TXC1P 50
4P2R-0R
34 L_BKLTEN R663 X 0R0402 BLKTEN_IN 53
49 GPIO4_BLEN R640 0R0402 R662 100KR0402
JLVDS1 LCD_VDD
LVDSB_DATA3 LVDSB_DATA3# LVDSB_CLK LVDSB_CLK# LVDSB_DATA2 LVDSB_DATA2# LVDSB_DATA1 LVDSB_DATA1# LVDSB_DATA0 LVDSB_DATA0# LVDSA_DATA3 LVDSA_DATA3# LVDSA_CLK LVDSA_CLK# LVDSA_DATA2 LVDSA_DATA2# LVDSA_DATA1 LVDSA_DATA1# LVDSA_DATA0 LVDSA_DATA0#
FPC30P-1PITCH_WHITE-RH
LVDS_VDDEN# = LO Power ON
LVDS_VDDEN# = HI Power OFF
+12V R879 10KR0402 VCC5 Q72 N-P3055LDG_TO252-RH LCD_VDDEN LCD_VDD5V F3 F-SMD1812P150TF/24-RH LCD_VDD C872 0.01u/16V/4 C360 C0.1u16Y0402 C349 C10u10Y0805 C359 C10u10Y0805 C350 C10u10Y0805
VCC3 R878 10KR0402 34 LVDS_VDDEN# R876 X 0R0402 LCD_VDDEN# Q71 N-2N7002_SOT23
49,53 GPIO3_PPEN Q73 N-2N7002_SOT23 R886 100KR0402
VCC3 VCC5 R612 X_4.7KR0402 R619 X_4.7KR0402 R618 X 0R0402 L_BKLTEN# BLKTEN_IN Q50 X_N-2N7002_SOT23 C472 X_C0.1u16Y0402 NO_STUFF R637 0R0402
+12V F6 F-SMD2920P300TF-15-RH C449 C0.1u16Y0402 C440 C10u16Y1206 C441 C10u16Y1206 L_BKLTCTL# L_BKLTEN# JINV1 BH1X6-2.5PITCH_WHITE-RH
VCC3 VCC5 R666 X_10KR0402 R649 X_10KR0402 R648 4.7KR0402 L_BKLTCTL# R667 0R0402 C491 C1u10Y0402-RH
34 L_BKLTCTL R639 X_10KR0402 Q51 X_N-2N7002_SOT23-1
49 GPIO2_BL_PWM R643 X_10KR0402
16,53 EC_BLKTCTL R652 0R0402
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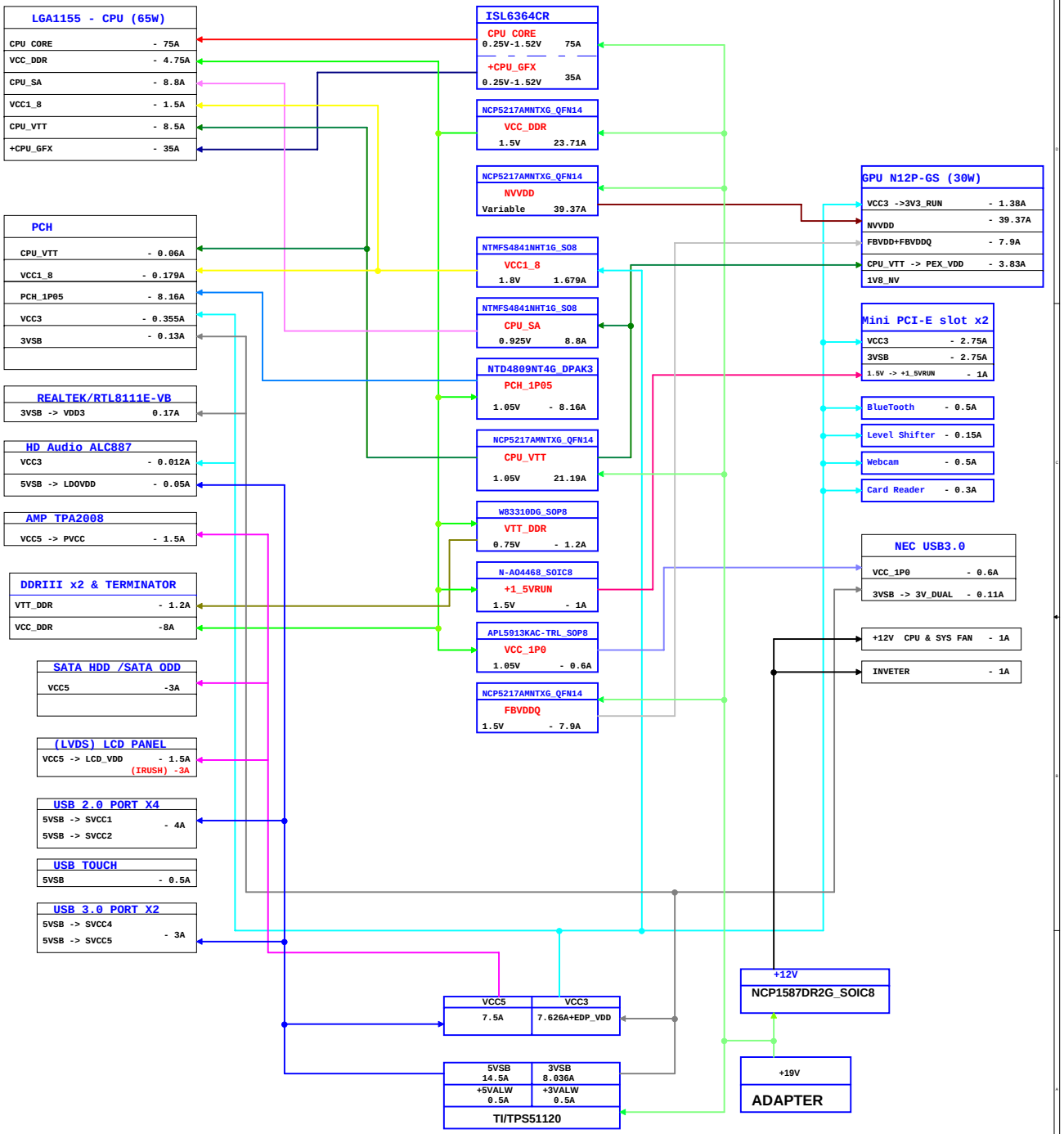
LGA1155 - CPU (65W)
CPU CORE - 75A
VCC_DDR - 4.75A
CPU_SA - 8.8A
VCC1_8 - 1.5A
CPU_VTT - 8.5A
+CPU_GFX - 35A
PCH
CPU_VTT - 0.06A
VCC1_8 - 0.179A
PCH_1P05 - 8.16A
VCC3 - 0.355A
3VSB - 0.13A
REALTEK/RTL8111E-VB
3VSB -> VDD3 0.17A
HD Audio ALC887
VCC3 - 0.012A
5VSB -> LDOVDD - 0.05A
AMP TPA2008
VCC5 -> PVCC - 1.5A
DDRIII x2 & TERMINATOR
VTT_DDR - 1.2A
VCC_DDR -8A
SATA HDD /SATA ODD
VCC5 -3A
(LVDS) LCD PANEL
VCC5 -> LCD_VDD - 1.5A
(IRUSH) -3A
USB 2.0 PORT X4
5VSB -> SVCC1
5VSB -> SVCC2
- 4A
USB TOUCH
5VSB - 0.5A
USB 3.0 PORT X2
5VSB -> SVCC4
5VSB -> SVCC5
- 3A
ISL6364CR
CPU CORE
0.25V-1.52V 75A
+CPU_GFX
0.25V-1.52V 35A
NCP5217AMNTXG_QFN14
VCC_DDR
1.5V 23.71A
NCP5217AMNTXG_QFN14
NVVDD
Variable 39.37A
NTMFS4841NHT1G_SO8
VCC1_8
1.8V 1.679A
NTMFS4841NHT1G_SO8
CPU_SA
0.925V 8.8A
NTD4809NT4G_DPAK3
PCH_1P05
1.05V - 8.16A
NCP5217AMNTXG_QFN14
CPU_VTT
1.05V 21.19A
W83310DG_SOP8
VTT_DDR
0.75V - 1.2A
N-AO4468_SOIC8
+1_5VRUN
1.5V - 1A
APL5913KAC-TRL_SOP8
VCC_1P0
1.05V - 0.6A
NCP5217AMNTXG_QFN14
FBVDDQ
1.5V - 7.9A
GPU N12P-GS (30W)
VCC3 ->3V3_RUN - 1.38A
NVVDD - 39.37A
FBVDD+FBVDDQ - 7.9A
CPU_VTT -> PEX_VDD - 3.83A
1V8_NV
Mini PCI-E slot x2
VCC3 - 2.75A
3VSB - 2.75A
1.5V -> +1_5VRUN - 1A
BlueTooth - 0.5A
Level Shifter - 0.15A
Webcam - 0.5A
Card Reader - 0.3A
NEC USB3.0
VCC_1P0 - 0.6A
3VSB -> 3V_DUAL - 0.11A
+12V CPU & SYS FAN - 1A
INVETER - 1A
VCC5
7.5A
VCC3
7.626A+EDP_VDD
5VSB
14.5A
3VSB
8.036A
+5VALW
0.5A
+3VALW
0.5A
TI/TPS51120
+12V
NCP1587DR2G_SOIC8
+19V
ADAPTER
MICRO-STAR INT'L CO.,LTD
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0A to 1.0

(2010/11/24)

Page.04 Dummy C96

Page.16 Dummy D8
Page.16 Add Q103,Q932(Dummy)

Page.20 Modify LAN1's pin L1 connect to net "LINK100#"
Page.20 Modify LAN1's pin L2 connect to net "LINK1000#"

Page.23 Change part reference "SATA2" to "SATA0"

Page.26 Change R719 from 10.2Kohm to 11Kohm

Page.27 Change C199 from 22pF to 100pF
Page.27 Change R271 from 39Kohm to 62Kohm
Page.27 Change R314 from 100ohm to 0ohm
Page.27 Dummy R313

Page.28 Change C24 from 820pF to 470pF
Page.28 Change C40 from 680pF to 220pF
Page.28 Change R66 from 4.02Kohm to 2.2Kohm
Page.28 Change C52 from 1000pF to 1500pF
Page.28 Change C48 from 820pF to 1500pF
Page.28 Change C54 from 2200pF to 680pF
Page.28 Change R84 from 35.7Kohm to 47Kohm
Page.28 Change R75 from 3Kohm to 7.32Kohm
Page.28 Change R80 from 9.1Kohm to 14Kohm

Page.29 Stuff C623,C624,C633,C634
Page.29 Change R293 from 20Kohm to 7.15Kohm
Page.29 Change R288 from 0ohm to 10Kohm
Page.29 Change R294 from 0ohm 0402 to 16.5Kohm 0603 and stuff it
Page.29 Stuff C208

Page.30 Change DC_JACK1's pcb footprint from "MINIDIN1_4" to "DCJACK_5"

Page.38 Change R406 from 75Kohm to 43.2Kohm
Page.38 Change R407 from 43.2Kohm to 75Kohm

Page.39 Change PC8,PC9 from 1uF to 0.1uF and dummy
Page.39 Change PR8,PR9 from 36Kohm to 20Kohm and dummy
Page.39 Dummy Q36,R531,R532
Page.39 Change R530 and R930 from 49.9ohm to 0ohm
Page.39 Add R933 and R934

(2010/11/26)

Page.10 Add R935,R936

(2010/11/29)

Page.39 Add EC46

(2010/11/30)

Page.22 Add C933
Page.22 D2, D16, D17, U31 change to D0G-0200529-A68

Page.31 Add EMI1,EMI2,EMI3,EMI4,MEI5
Page.38 U16, U19 change to D0G-25B050C-A68

(2010/12/01)

Page.13 Delete TP8,TP9,TP6,TP7,TP17,TP41,TP64
Page.13 CGPT1 pin A54/A52/F57/D57/A4/BM57/BP1 connect to GND

Page.19 Add C934,C935,C936

Page.26 Stuff EC3

Page.31 Add EMI6

Page.32 Change JXDP1's pcb footprint from "2X30_XDP_CONN" to "2X30_XDP_CONN_TEST"

Page.38 Add R937,R938

(2010/12/06)

Page.38 Dummy R487

(2010/12/07)

Change R936,R929,C933,C934,C935,C936 ASM-LEVEL FROM 5010 to 5020

(2010/12/11)

Change R288 from 0ohm to 10Kohm again (BOM Issue)

1.0 to 1.1

(2010/12/22)

Page.31 Add SB_SINK

Page.38 Change R412 from 49.9Kohm to 0ohm & Dummy R406,R407,R411(Auto mode)

Page.53 Modify EDP1's pin 11,12,30 connect to +12V

(2010/12/23)

Page.23 Change CPU FAN from SIO FAN1 to SIO FAN2

Page.23 Change SYS FAN from SIO FAN2 to SIO FAN1

(2010/12/27)

Change CGPT1's P/N from "OB1-7728001" to "B01-00H6105-I06"

Page.48 Delete Q69,R421

Page.48 Change R809 from 20Kohm to 100Kohm

Page.48 Change R425 from 200Kohm to 1Kohm

Page.38 Change USB1's footprint from "USB_D18_V3_0" to "USB_A2_18_1"

Page.29 add power solution c937 c938

(2011/1/7)

NEC 3.0 K/B MOUSE S3 WAKE UP SOLUTION

UNSTUFF : R378 R457 R477 R515

STUFF : Y5 C320 C310 R511

OSD Backlight control

UNSTUFF : Q51 R649

STUFF : R667

Change : R652 10K--> 0

(2011/01/10)

Page.31 Change CPU1_X1's P/N from "E21-AE12010-L06" to "E21-S016010-L06"

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