MODEL NAME : ***AAM00***

PCB NO : ***LA-C361P***

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
TPM@ : TPM function
EMC@ : Pop of EMI parts
VRAMS@ : Samsung GDDR5 for GPU
VRAMH@ : Hynix GDDR5 for GPU
VRAMM@ : Micron GDDR5 for GPU
BreakDown@ : for measure power consumption
CSMB@ : CSMB sku
BC@ : BC sku (GPU N16P-Q1)
GX@ : GPU N16P-GX
UMA@ / DIS@ : UMA/DIS

PCB
ZZZ R1@
PCB 1BG LA-C361P REV0 MB

CPU
UH1 R1@
SKL-H_BGA1440

PCH
UH2 R1@
SKY-H-PCH_BGA837

GPU
UV1 BC@
N16P-Q1-A2
UV1 GX@
N16P-GX-A2

Samsung 2G
RV312
20K_0402_1%
VRAMS@
UV5
K4G41325FC-HC03_FBGA170P~D
VRAMS@
UV6
K4G41325FC-HC03_FBGA170P~D
VRAMS@
UV9
K4G41325FC-HC03_FBGA170P~D
VRAMS@
UV10
K4G41325FC-HC03_FBGA170P~D
VRAMS@

Hynix 2G
RV312
34.8K_0402_1%
VRAMH@
UV5
H5GC4H24AJR-R0C_FBGA170P~D
VRAMH@
UV6
H5GC4H24AJR-R0C_FBGA170P~D
VRAMH@
UV9
H5GC4H24AJR-R0C_FBGA170P~D
VRAMH@
UV10
H5GC4H24AJR-R0C_FBGA170P~D
VRAMH@

Micron 2G
RV312
24.9K_0402_1%
VRAMM@
UV5
EDW4032BABG-60-F_FBGA170P~D
VRAMM@
UV6
EDW4032BABG-60-F_FBGA170P~D
VRAMM@
UV9
EDW4032BABG-60-F_FBGA170P~D
VRAMM@
UV10
EDW4032BABG-60-F_FBGA170P~D
VRAMM@

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Issued Date	2011/08/25	Deciphered Date	2011/08/25	Title: Cover Page
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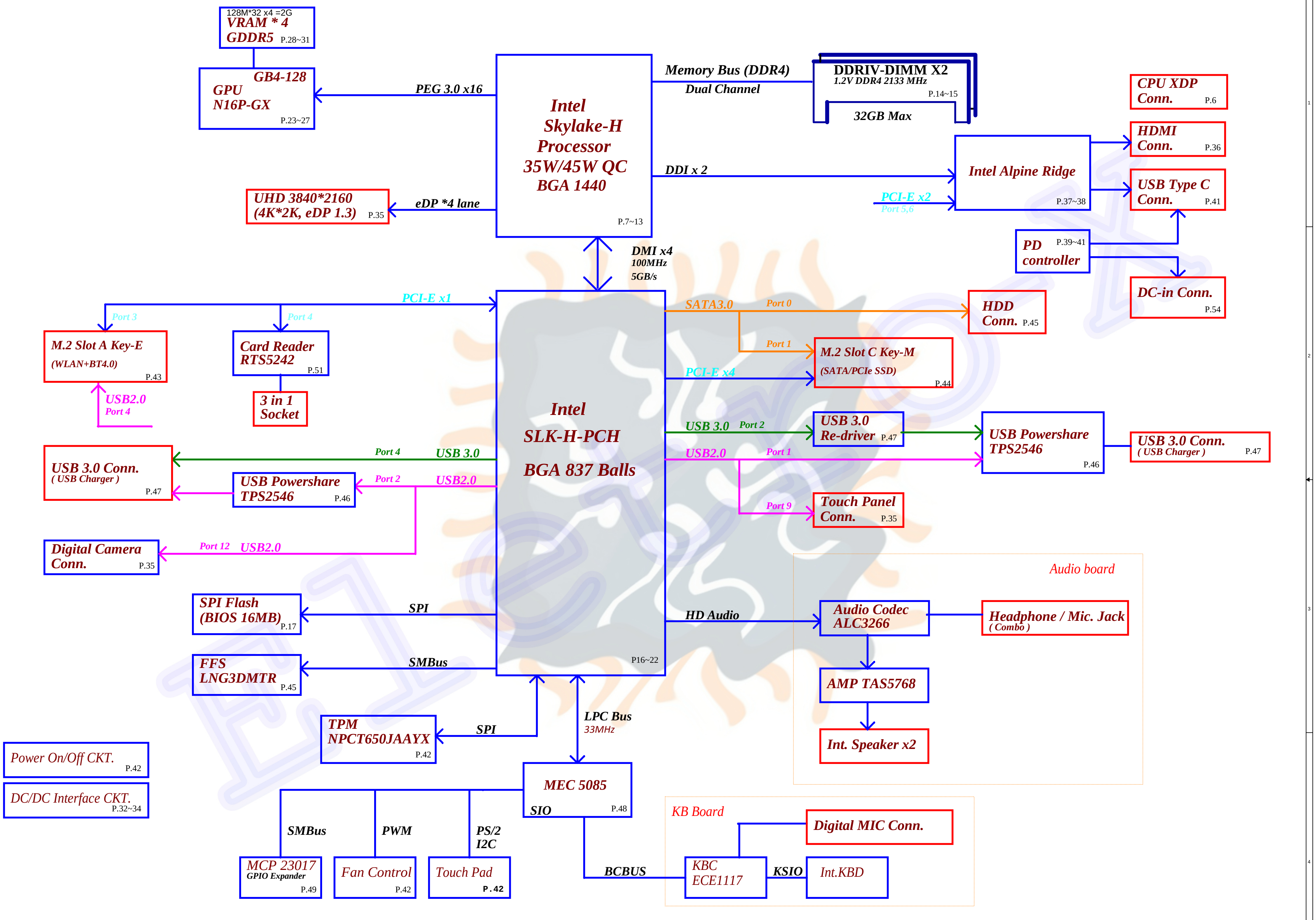
				Date: Thursday, August 06, 2015 / Sheet 1 of 71



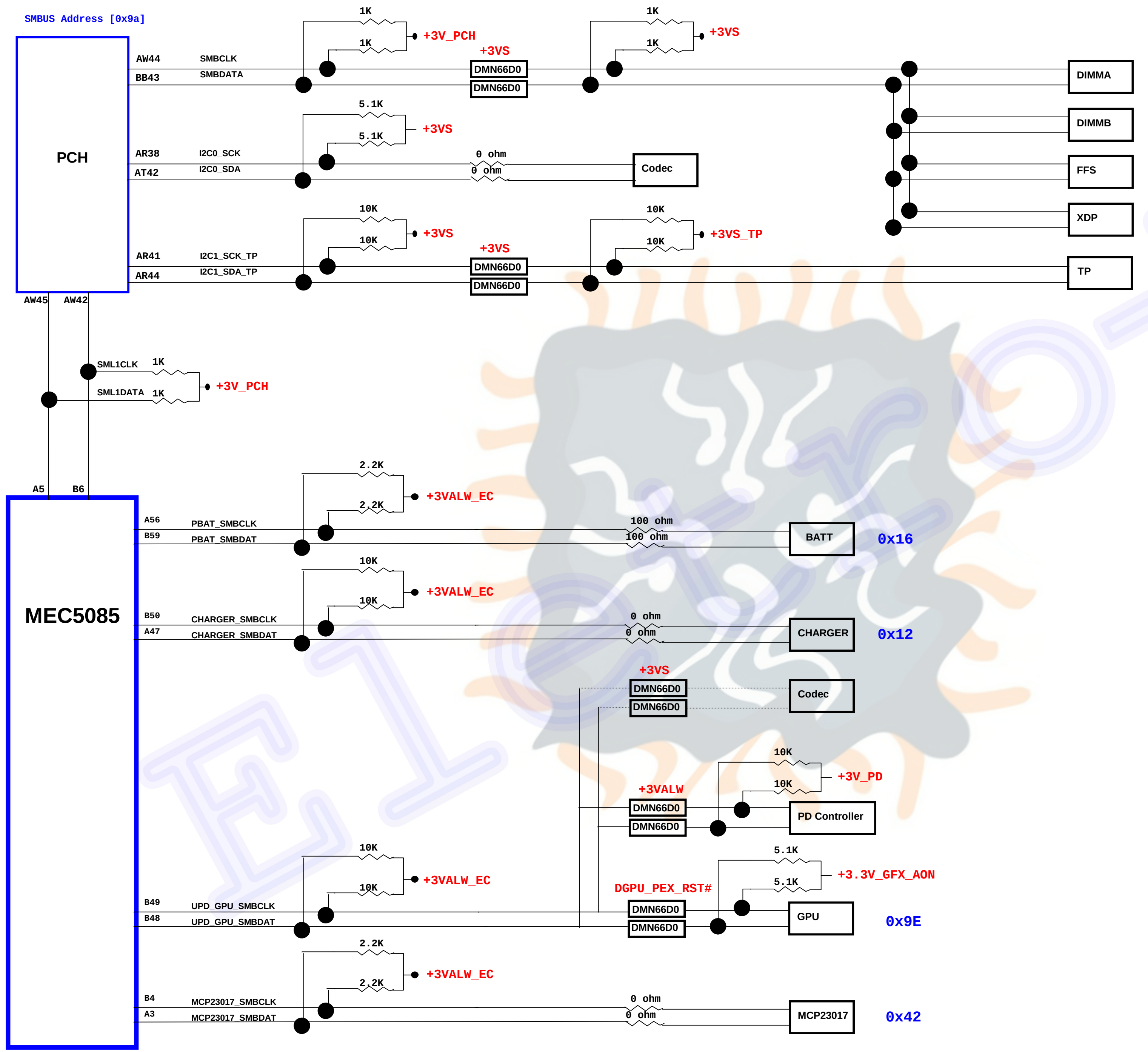
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **Block diagram**

Size | Document Number: **LA-C361P** | Rev 0.1(X00)

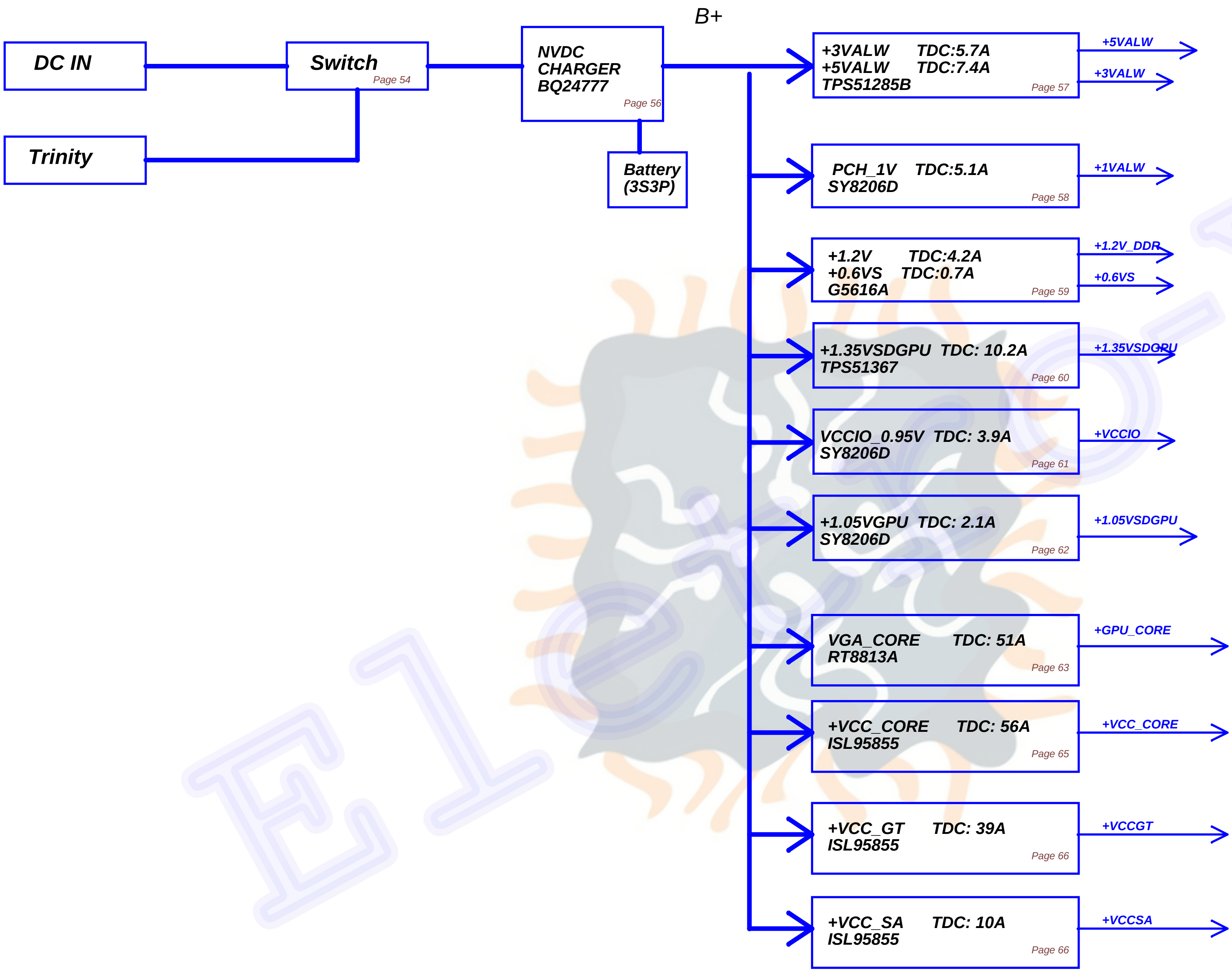
Date: Thursday, August 06, 2015 | Sheet 2 of 71



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/15	Title: SMBus Block Diagram

Size: Custom | Document Number | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 5 of 71



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: Power Sequence diagram
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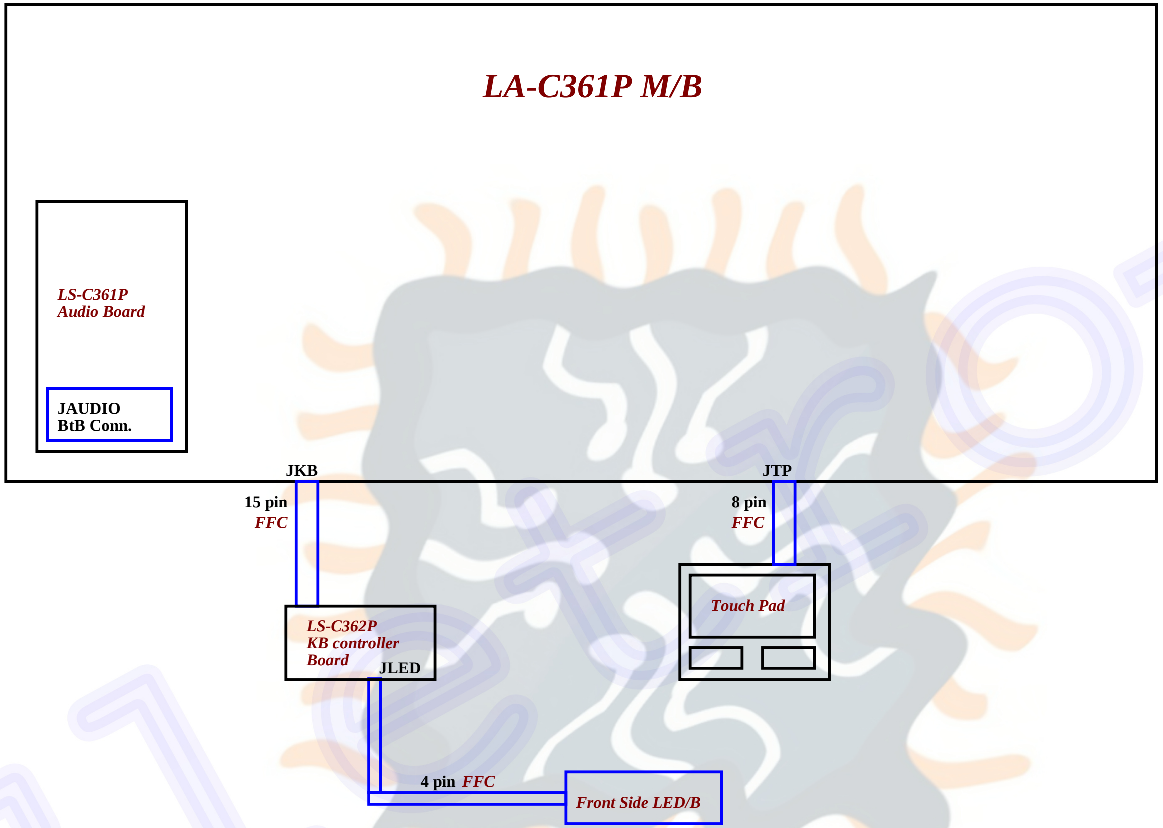
				Date: Tuesday, August 11, 2015 Sheet 53 of 71

Compal Confidential

Project Code : AAM00
File Name :



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: *DB block diagram*

Size | Document Number | Rev 0.1(X00)

Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION
Lane 1	NGFF-1 WLAN + BT
Lane 2	CARD READER
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	Alpine Ridge
Lane 16	Alpine Ridge

USB3	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	SSD
1A	N/A
N/A	N/A
N/A	N/A
0B	None
1B	HDD
2	None
3	None

CLKOUT_PCIE	DESTINATION
0	None
1	None
2	None
3	NGFF-1 WLAN
4	CARD READER
5	Thunderbolt
6	NGFF-2 SSD
7	GPU
8	None
9	None

CLKOUT_PCIE	DESTINATION
10	None
11	None
12	None
13	None
14	None
15	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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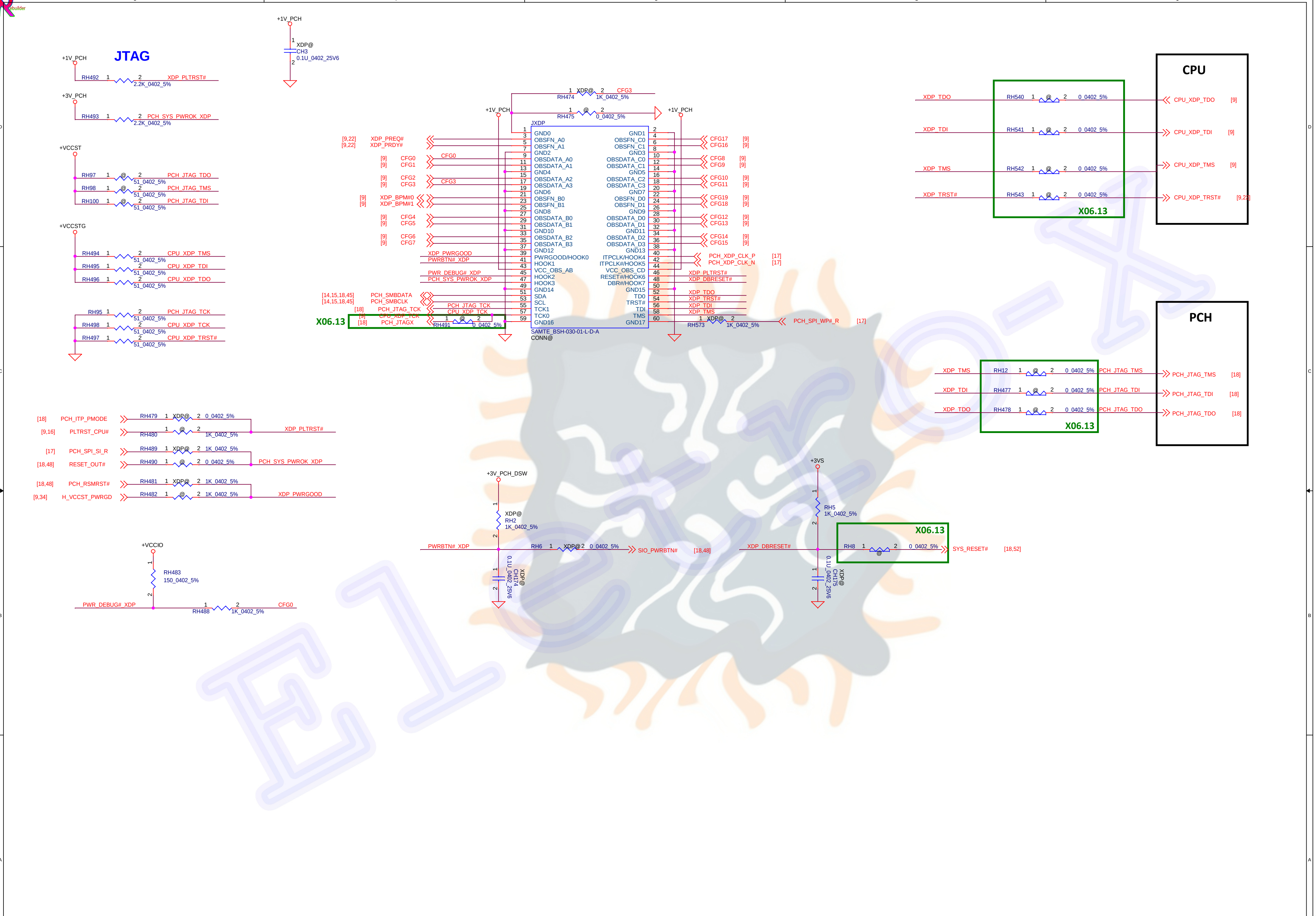
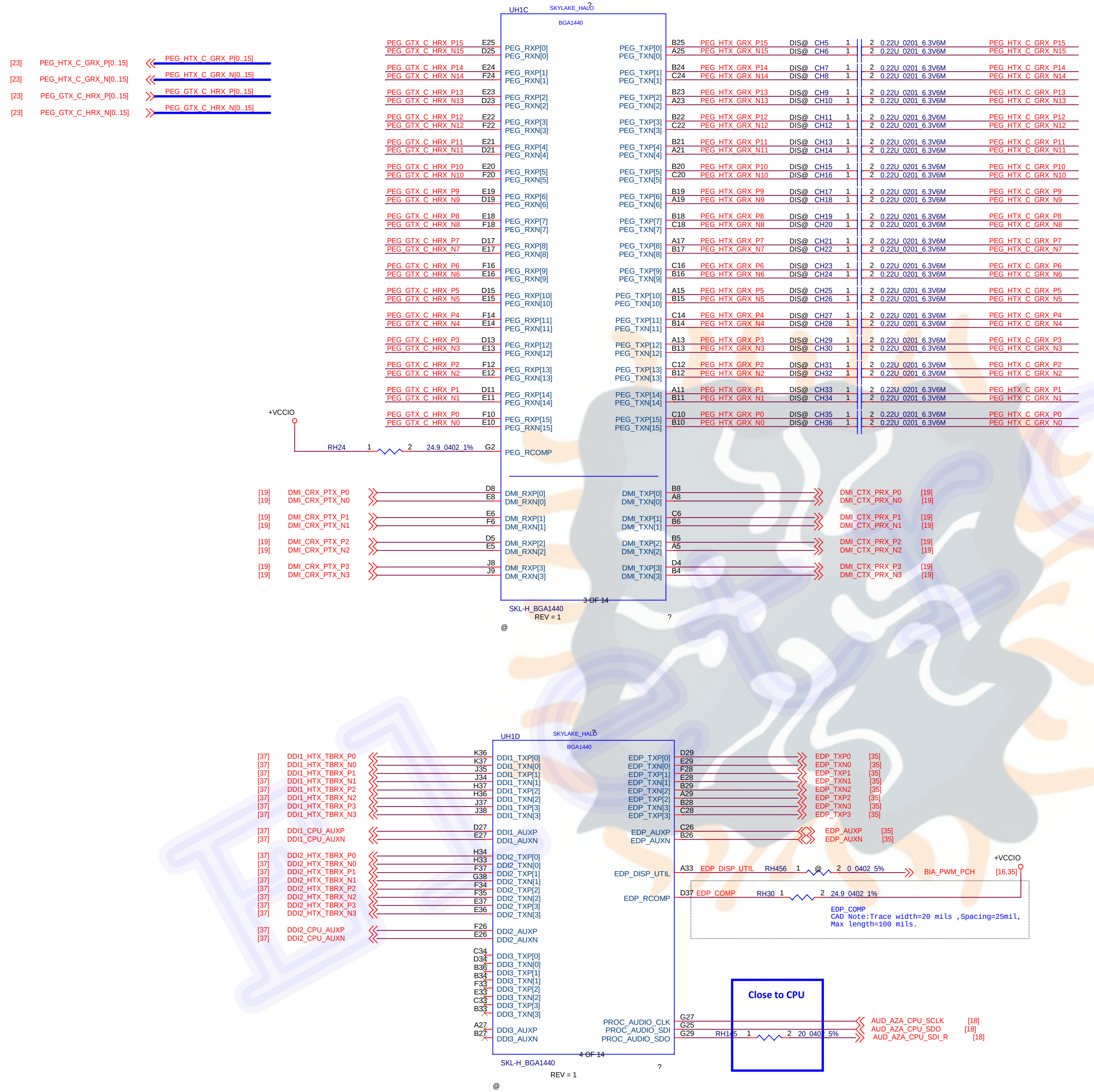
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: Notes List
				Size / Document Number: LA-C361P / Rev 0.1(X00)
				Date: Thursday, August 06, 2015 / Sheet 4 of 71



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: XDP CONN

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 6 of 71



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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: PROCESSOR(1/7) DMI,FDI,PEG
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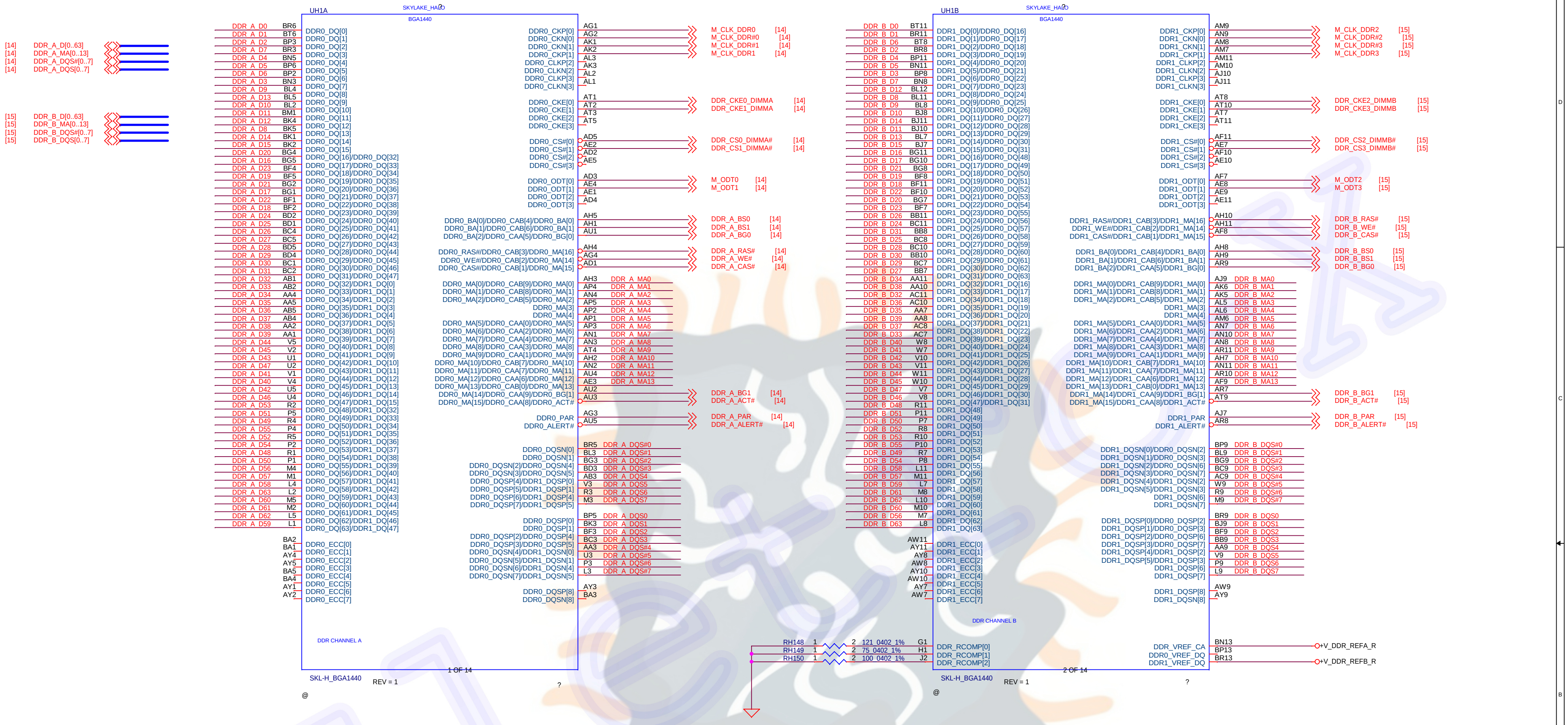
				Date: Thursday, August 06, 2015; Sheet 7 of 71

Interleave



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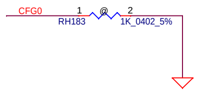
Title: PROCESSOR(3/7) DDRIII

Size: C | Document Number | Rev: 0.1(X00)

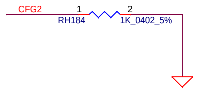
Date: Thursday, August 06, 2015 | Sheet 8 of 71

CFG Straps for Processor

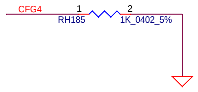
Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.



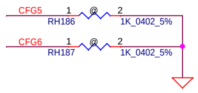
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



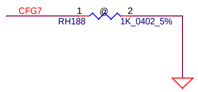
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

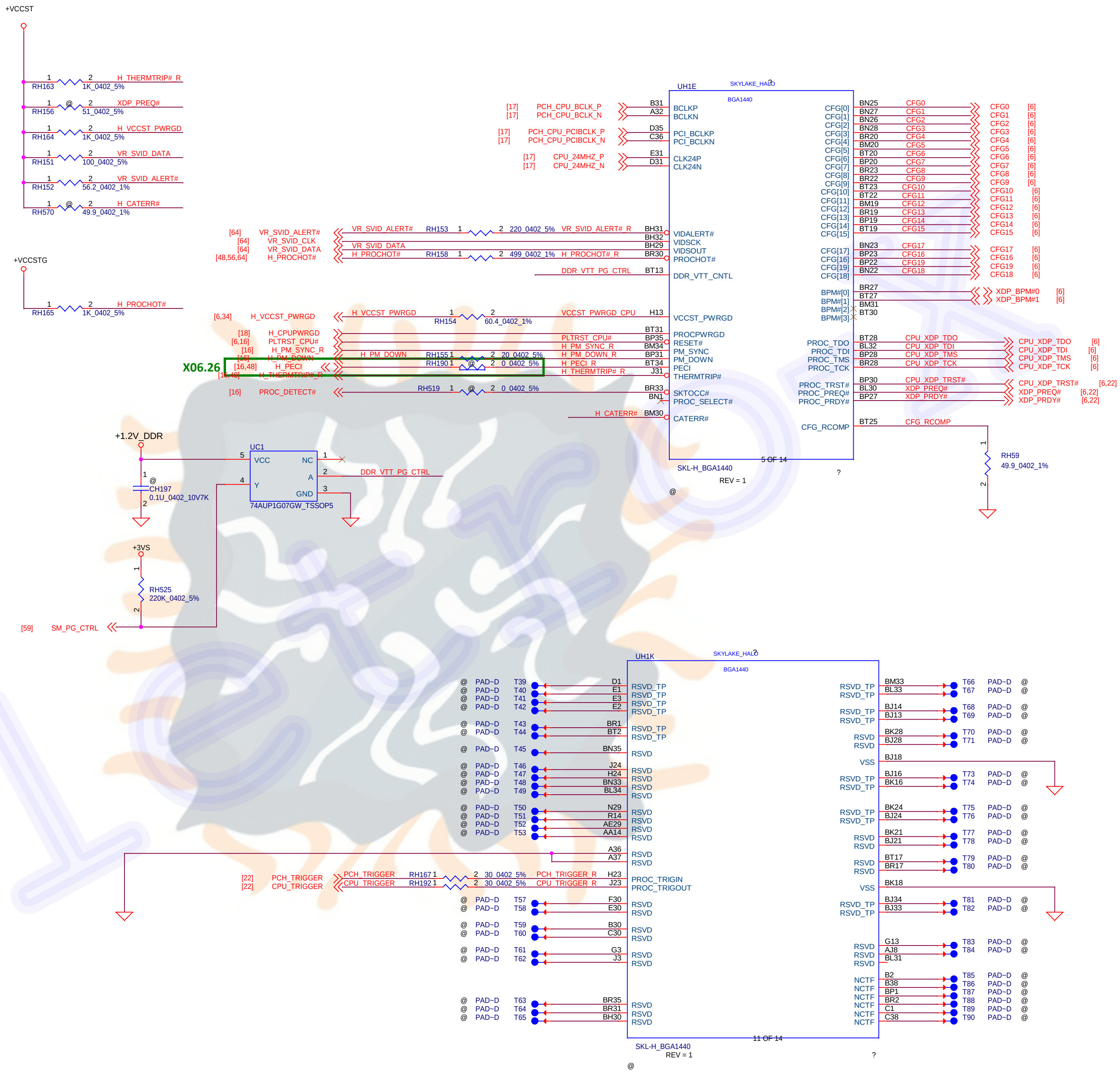


PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

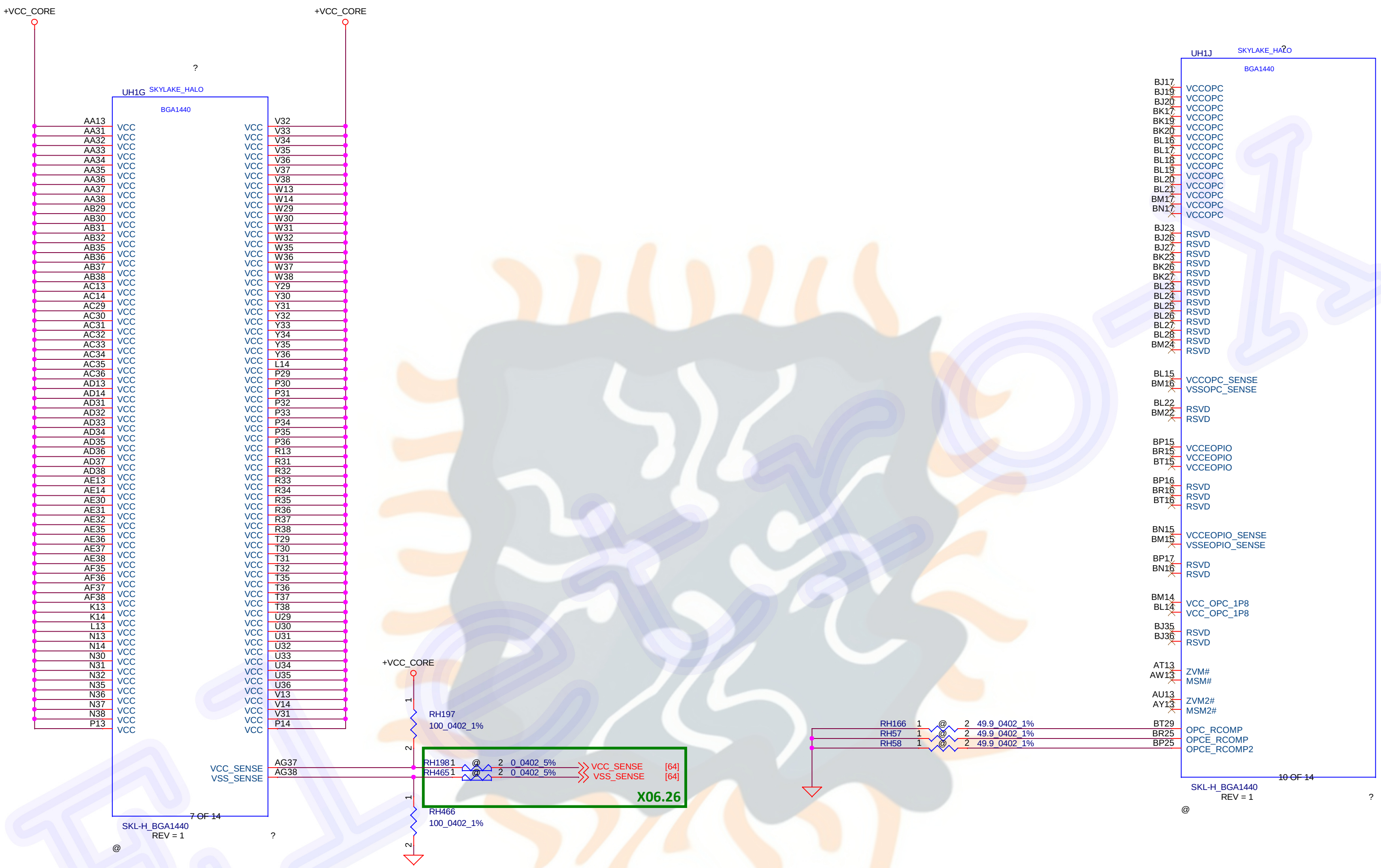




Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: PROCESSOR(4/7) RSVD,CFG

Size: C | Document Number | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 9 of 71



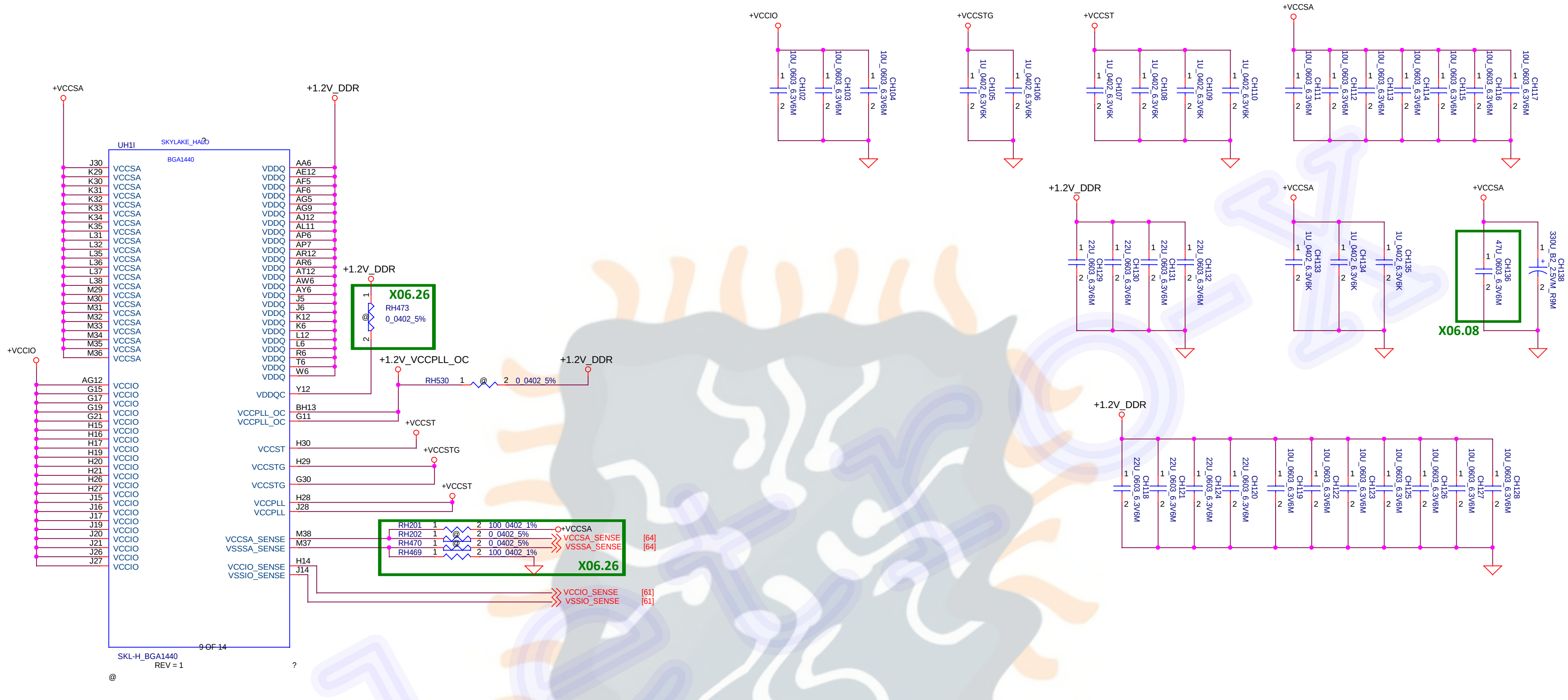
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title

PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 10 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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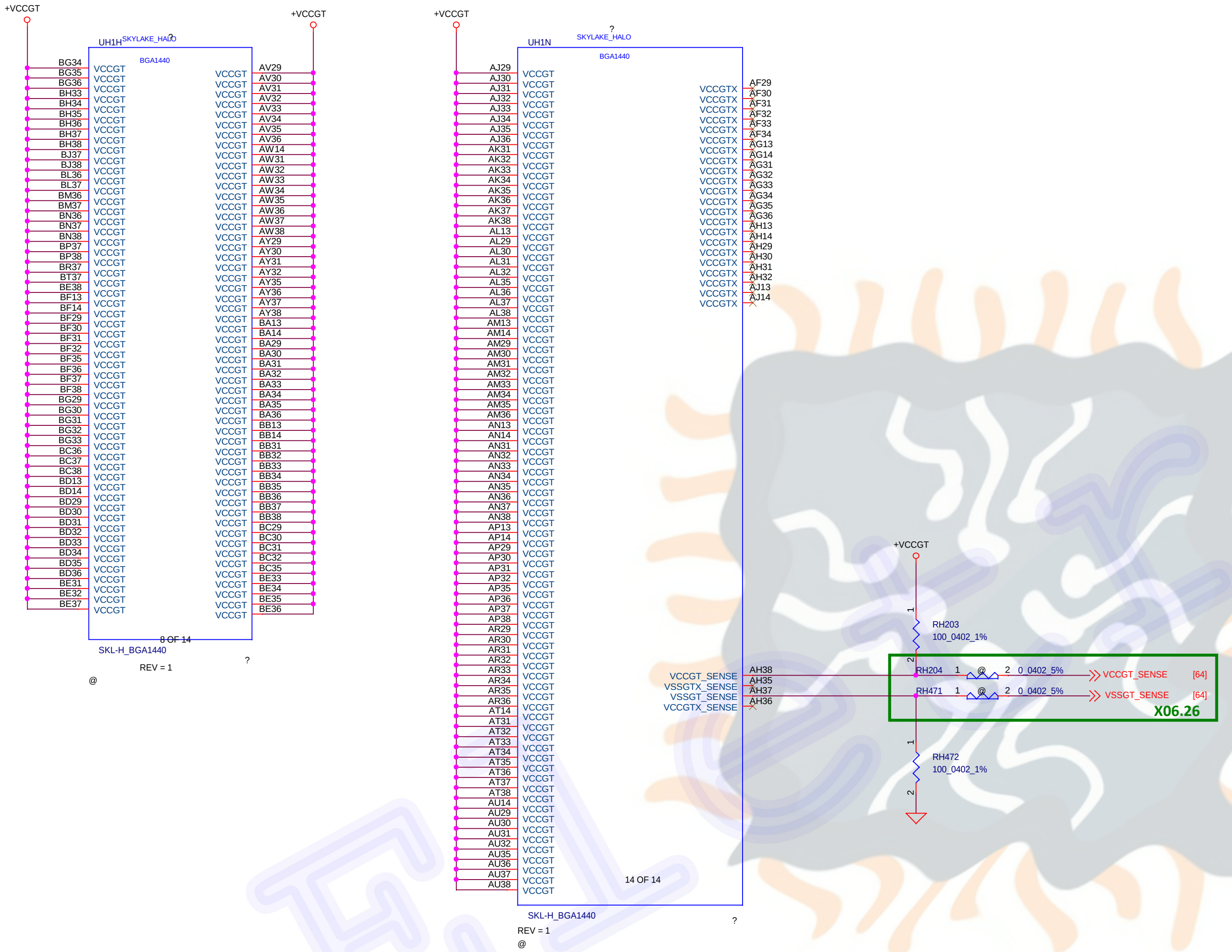
Compal Electronics, Inc.

Title: *PROCESSOR(6/7) PWR*

Size: Custom | Document Number | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 11 of 71

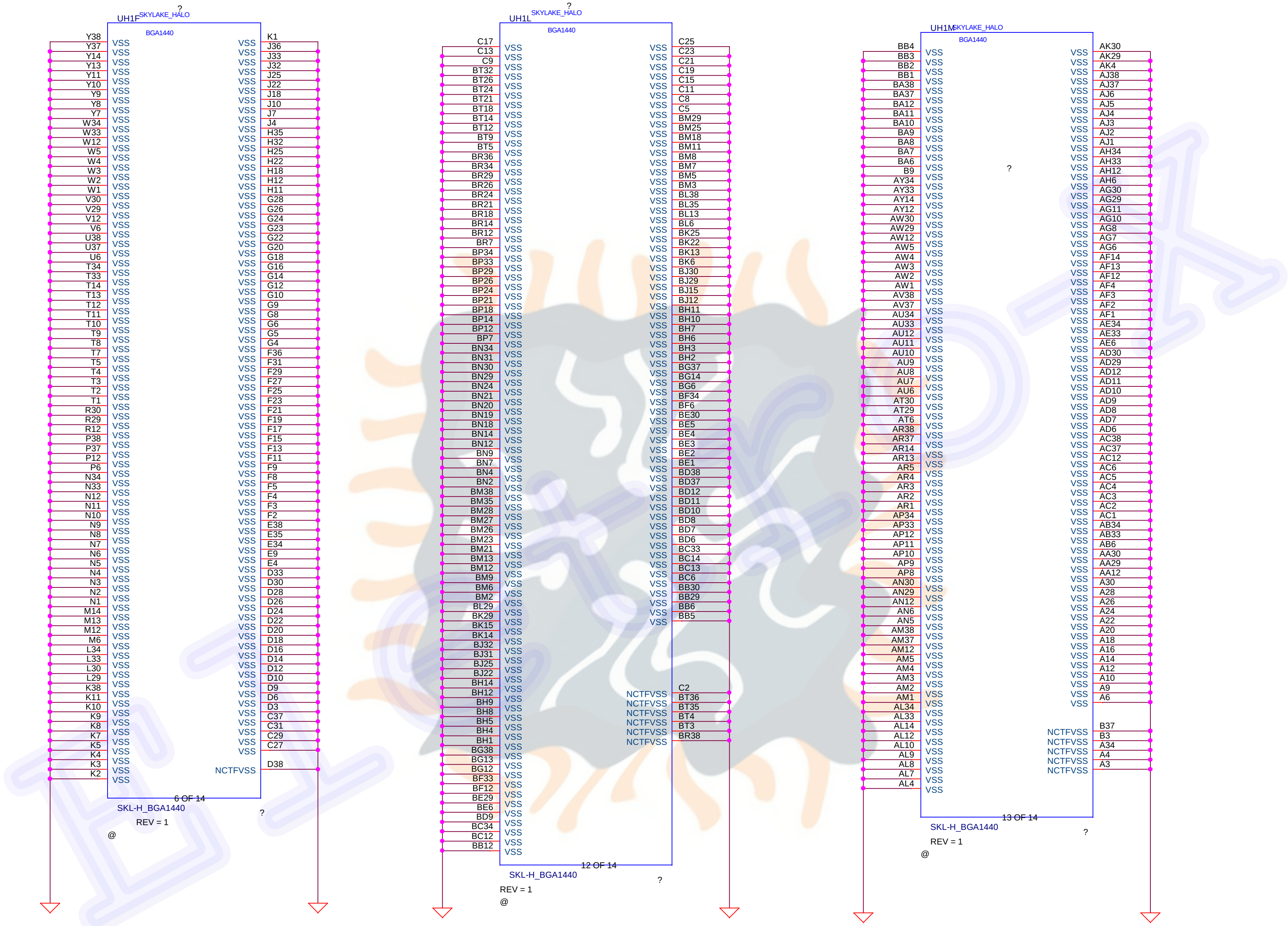


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(2/7) PM,XDP,CLK**

Size: Custom | Document Number | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 12 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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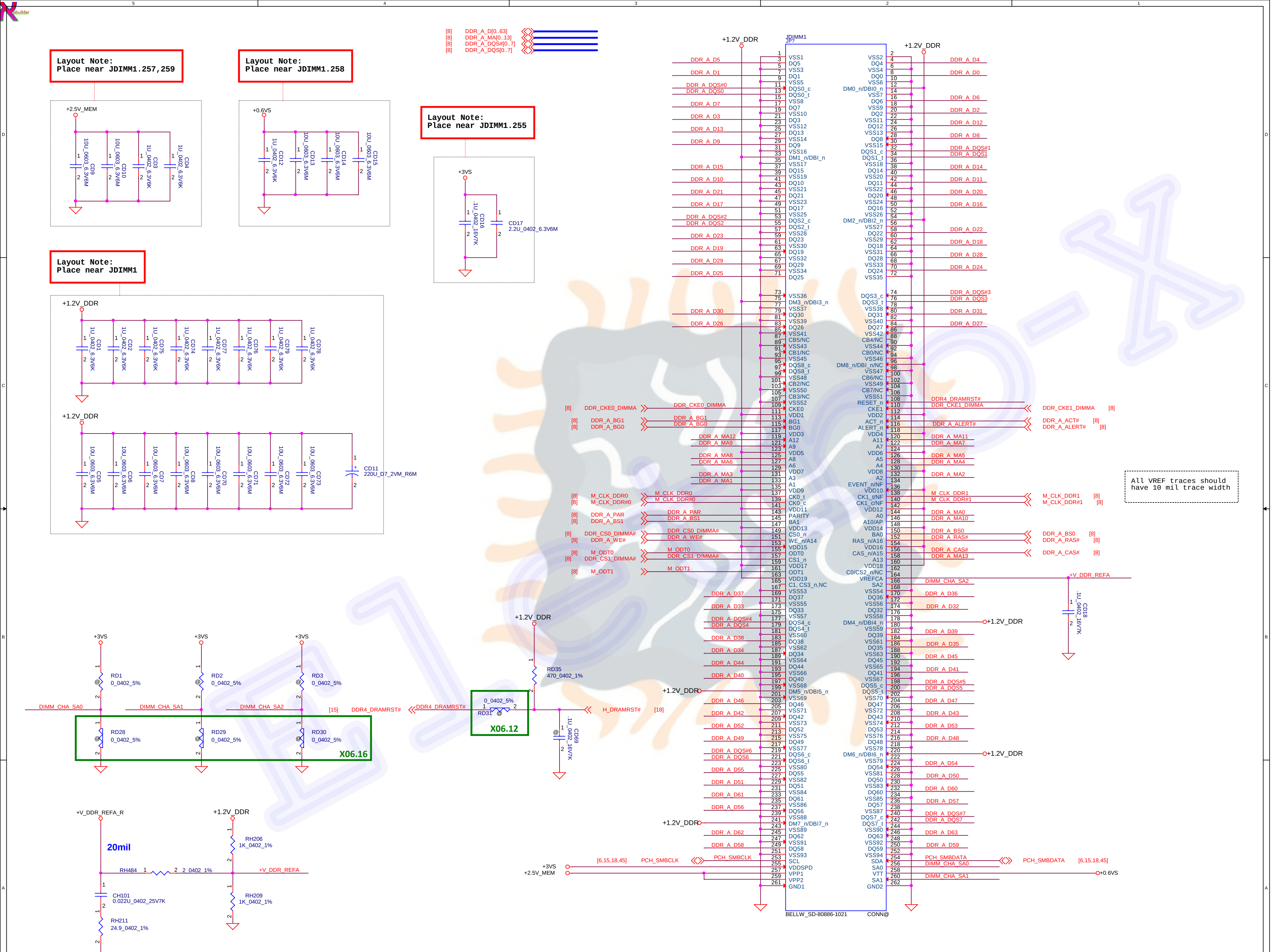
Title: **PROCESSOR(7/7) VSS**

Size: Custom | Document Number | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 13 of 71



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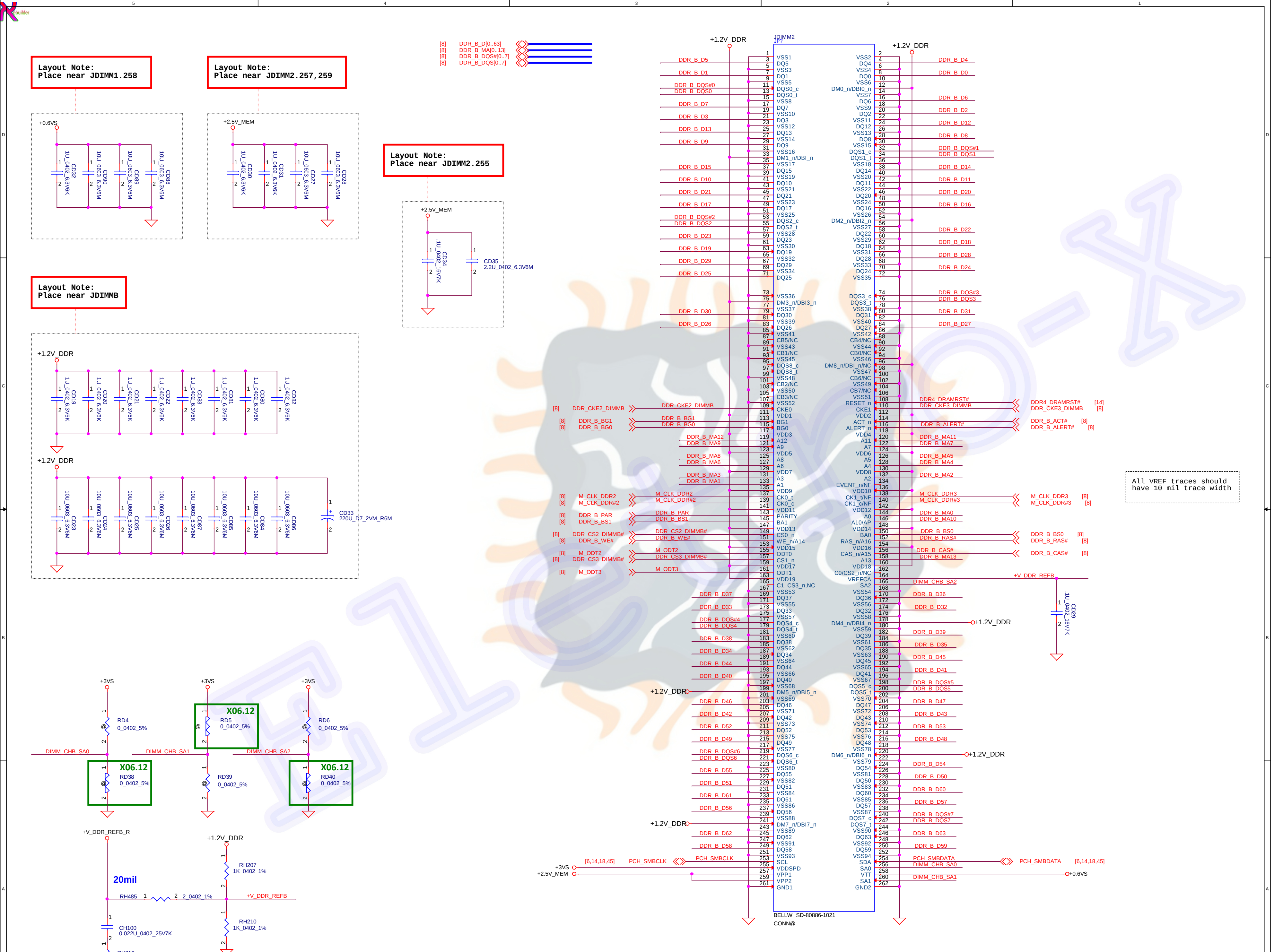
Title: DDRIII DIMMA

Document Number: LA-C361P

Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 14 of 71

Eletro-X



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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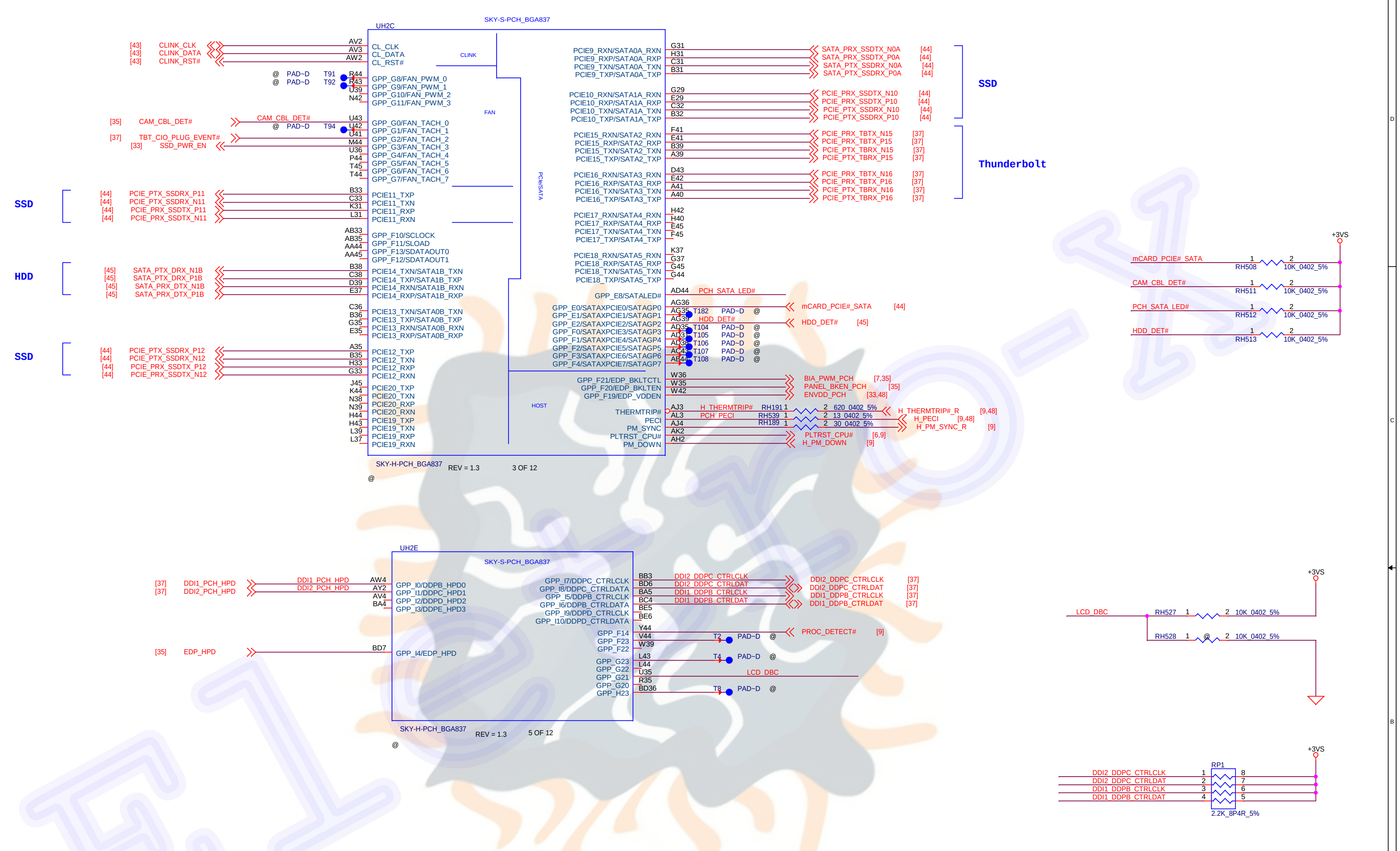
Compal Electronics, Inc.

Title: DDRIII DIMMB

Size | Document Number: LA-C361P | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 15 of 71



PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

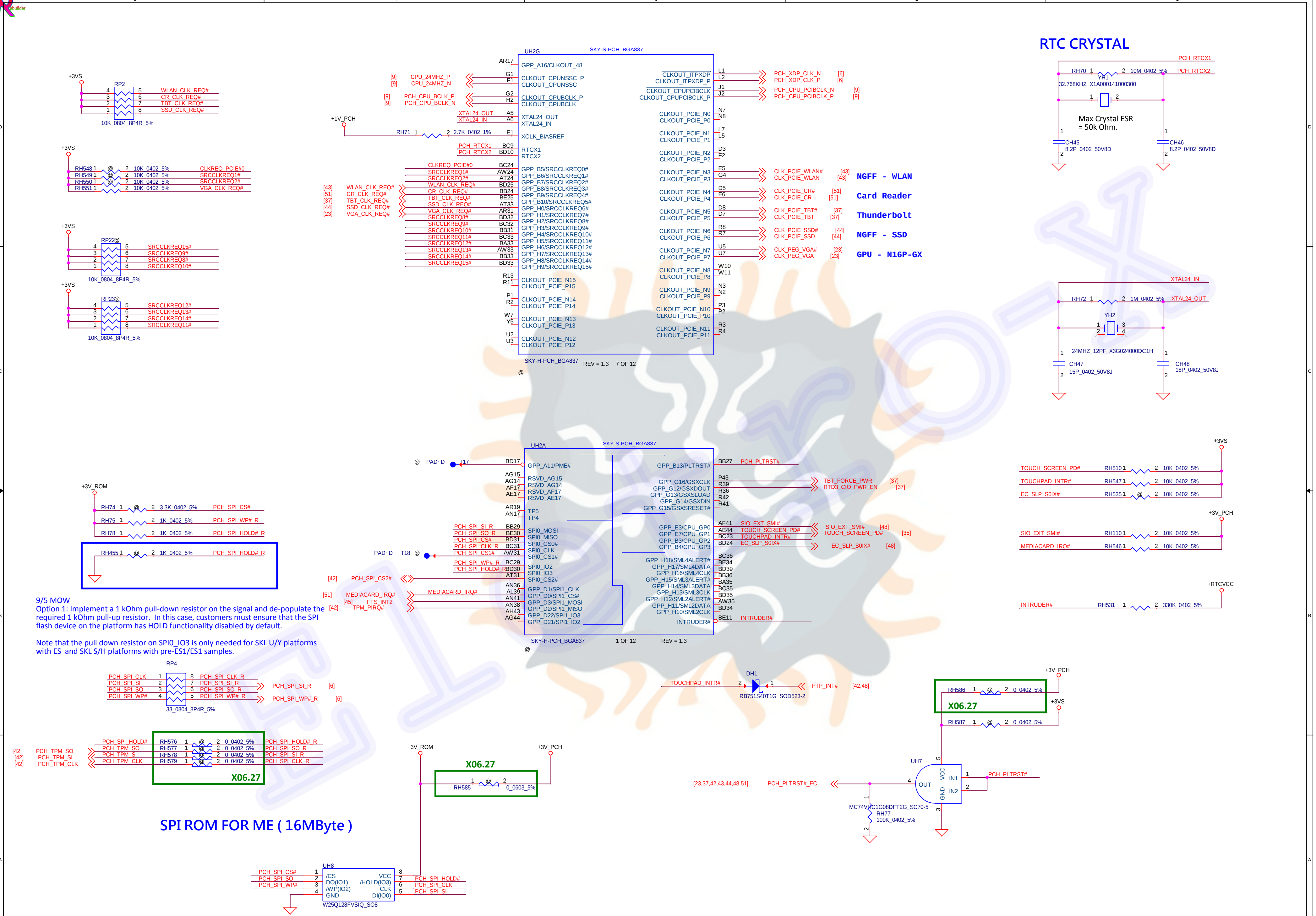
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (1/8) SATA,HDA**

Size | Document Number: **LA-C361P** | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 16 of 71

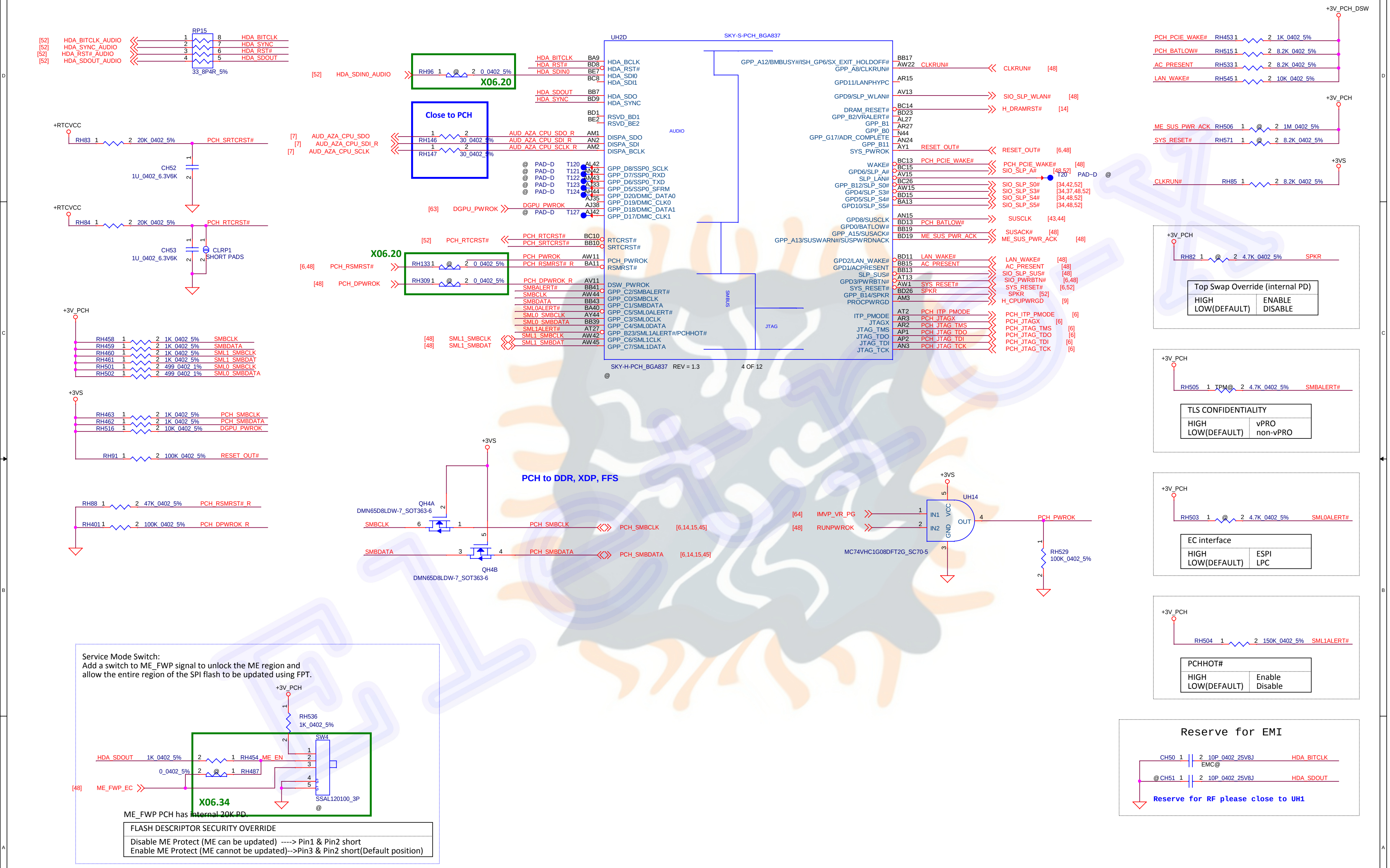


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (2/8) SMBUS, CLK, SPI, LPC**

Size | Document Number: **LA-C361P** | Rev 0.1(X00)



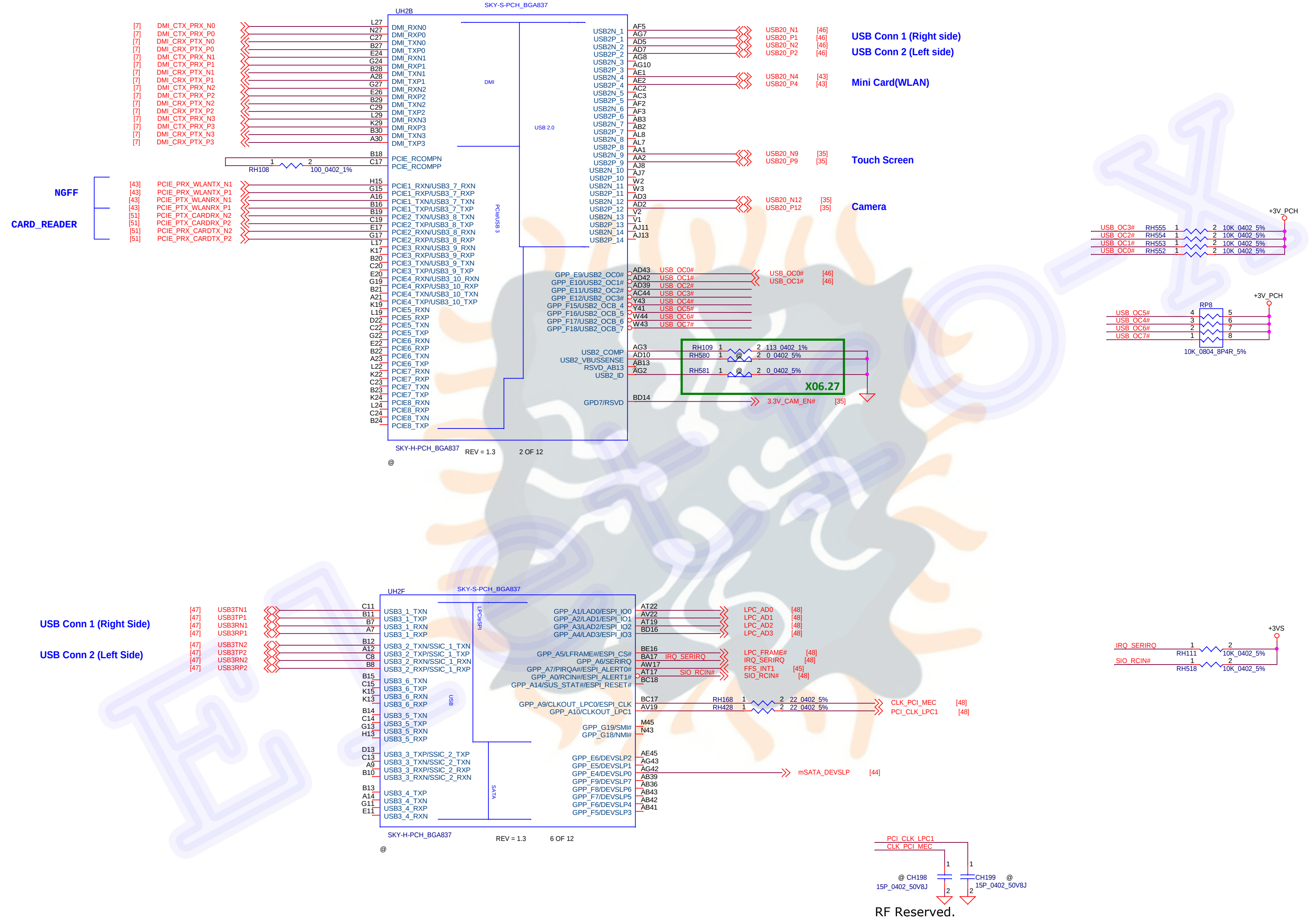
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size | Document Number: **LA-C361P** | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 18 of 71



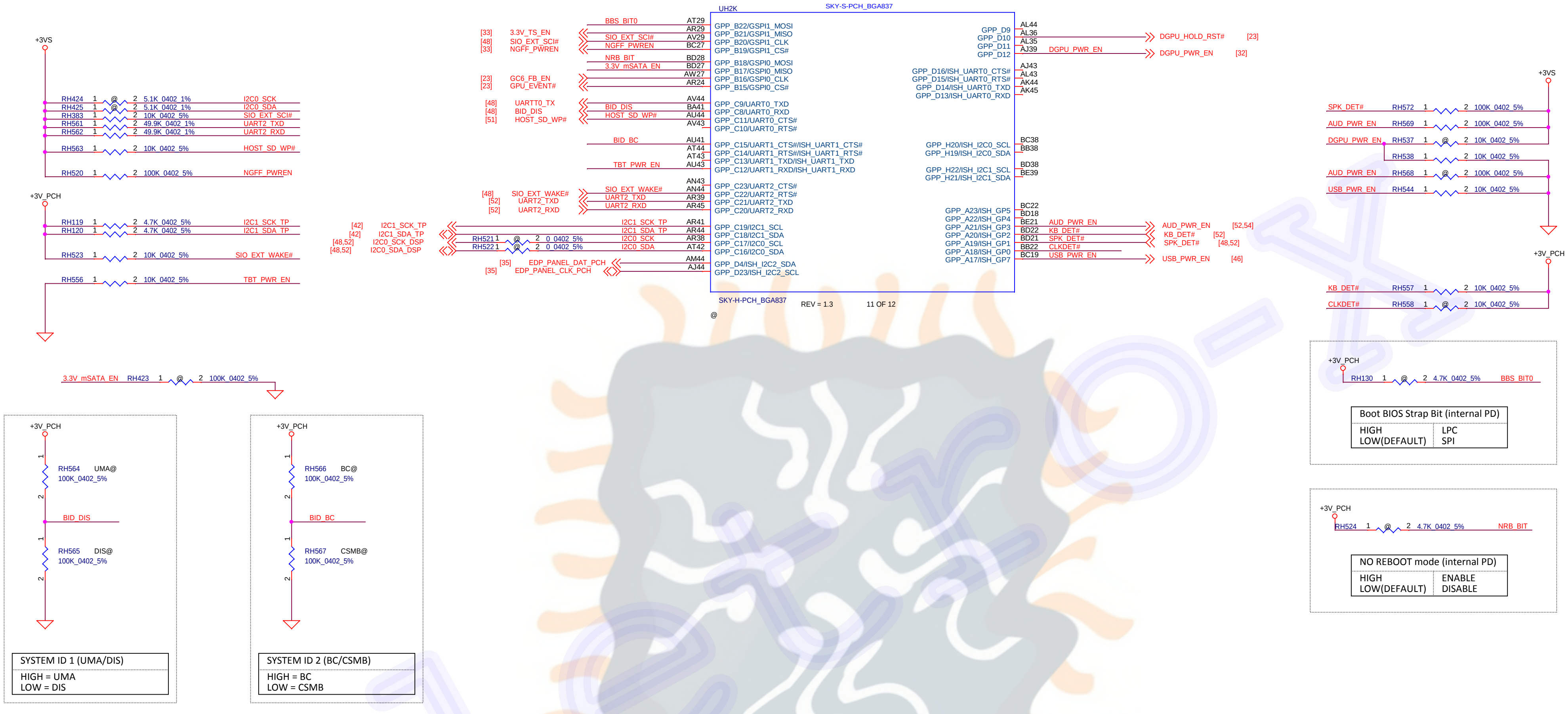
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: *PCH (4/8) PCI, USB*

Size | Document Number: *LA-C361P* | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 19 of 71



SYSTEM ID 1 (UMA/DIS)
HIGH = UMA
LOW = DIS

SYSTEM ID 2 (BC/CSMB)
HIGH = BC
LOW = CSMB

Boot BIOS Strap Bit (internal PD)	
HIGH	LPC
LOW(DEFAULT)	SPI

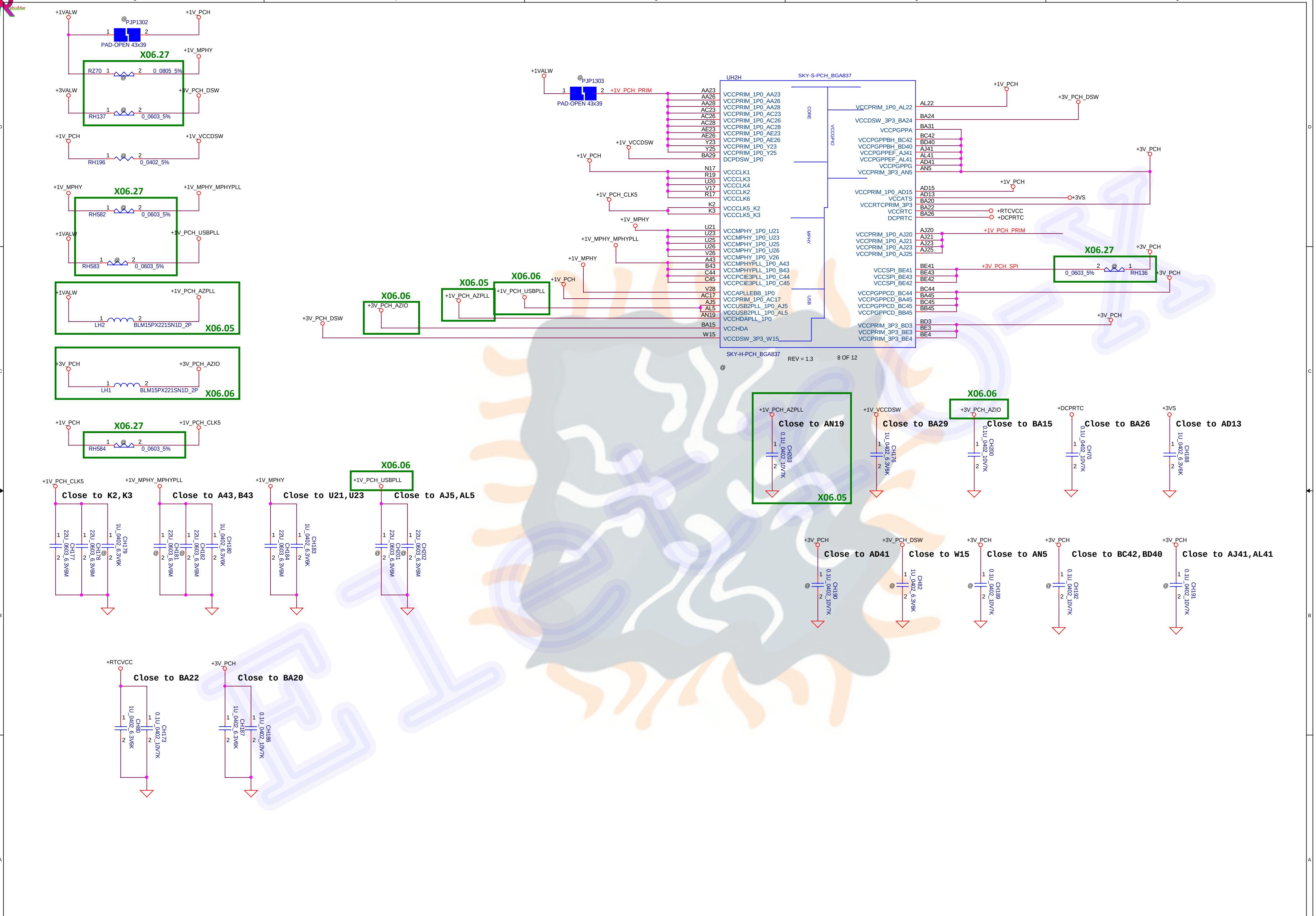
NO REBOOT mode (internal PD)	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size | Document Number: **LA-C361P** | Rev 0.1(X00)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: PCH (6/8) PWR
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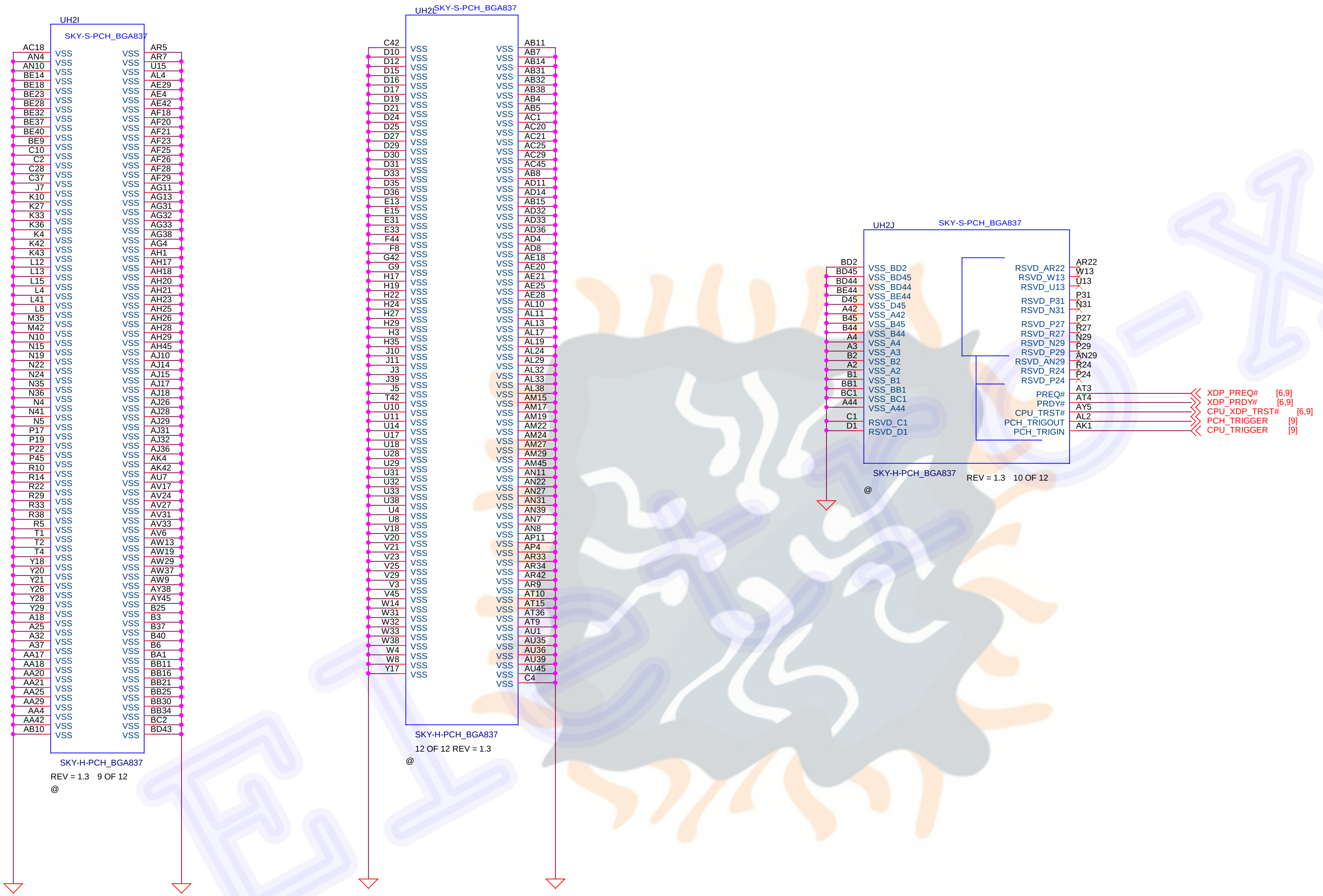
				Date: Thursday, August 06, 2015 / Sheet 21 of 71



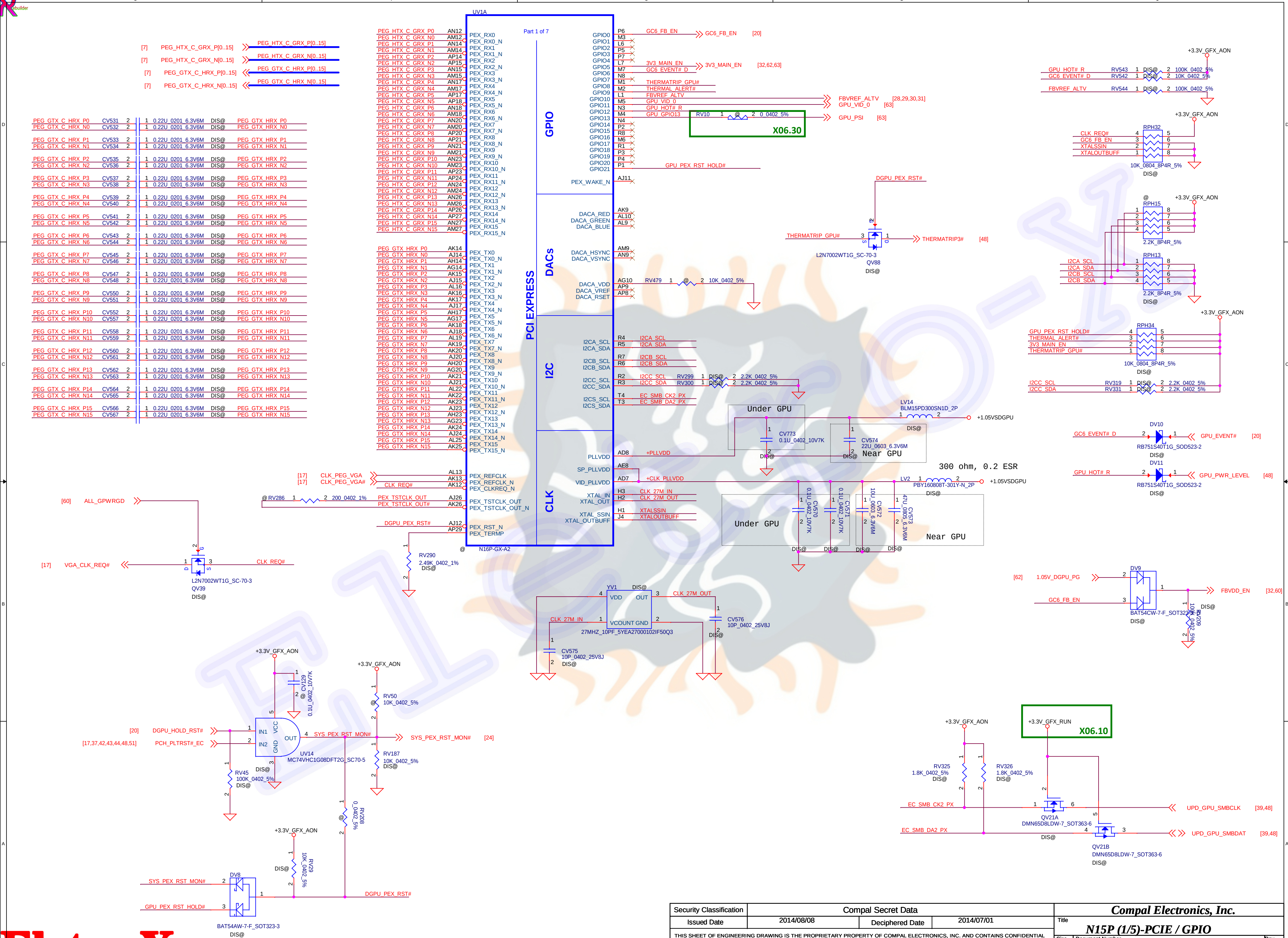
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size Document Number: **LA-C361P** Rev 0.1(A00)

Date: Thursday, August 06, 2015 Sheet 22 of 71



Security Classification	Compal Secret Data		
Issued Date	2014/08/08	Deciphered Date	2014/07/01

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Compal Electronics, Inc.

Title: **N15P (1/5)-PCIE / GPIO**

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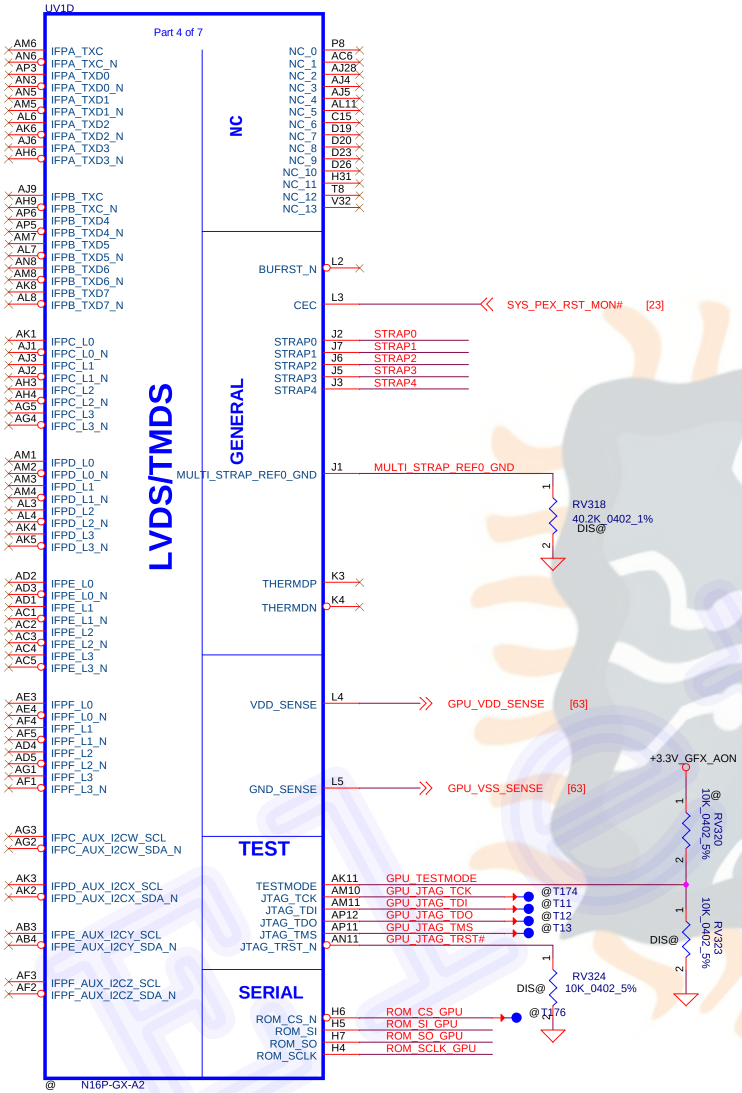
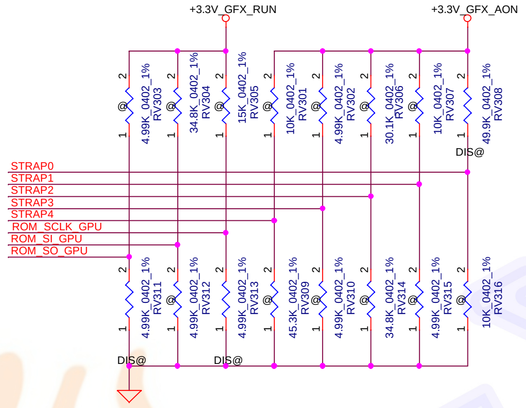


Straps



Memory	Berlinetta N16P-GX	Berlinetta-P N16P-Q1
Hynix_H5GC4H24AJR-R0C	0x6 (0110)	0x6 (0110)
Samsung_K4G41325FC-HC03	0x3 (0011)	0x3 (0011)
Micron_EDW4032BABG-60-F	0x4 (0100)	None RVL

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

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Issued Date	2014/08/08	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: ***N15P (2/5)-DP / Straps***

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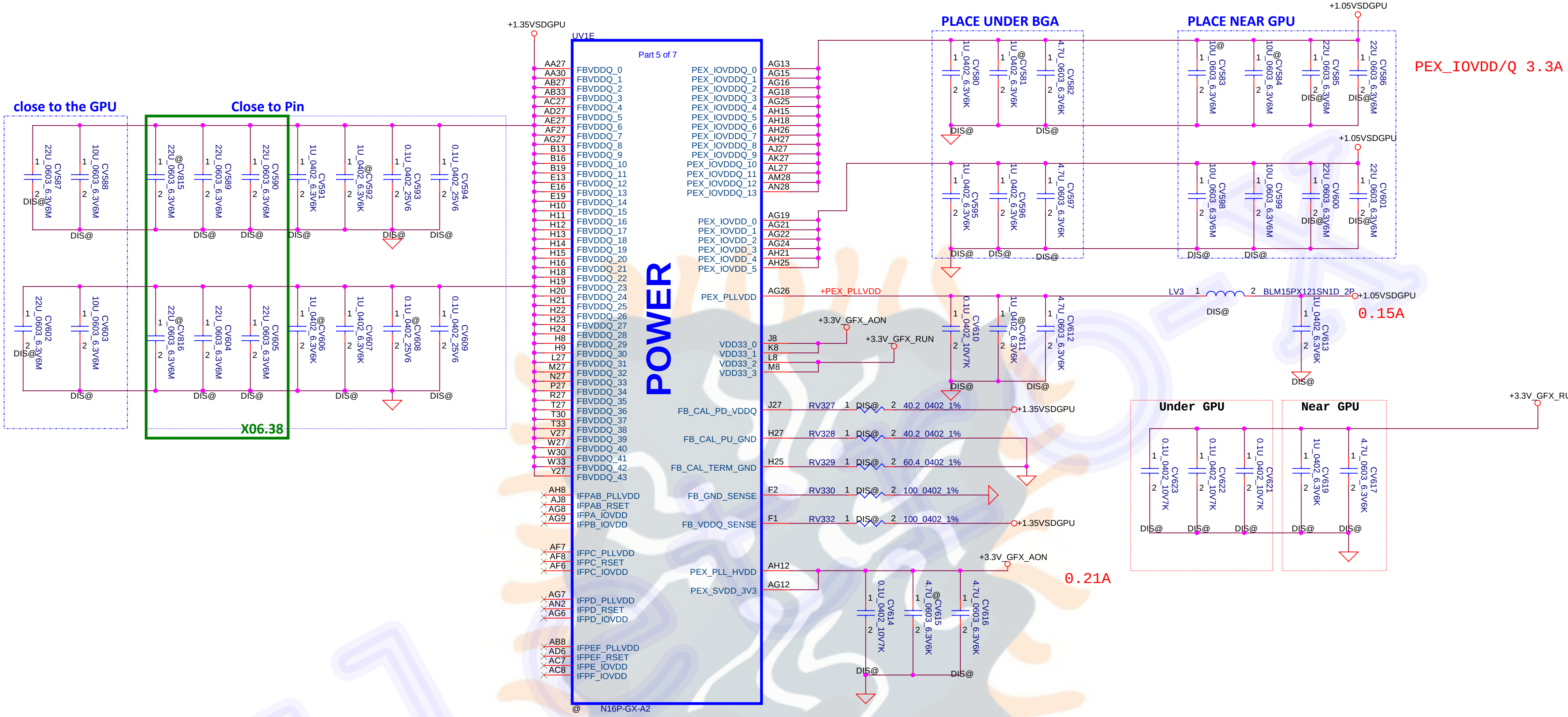
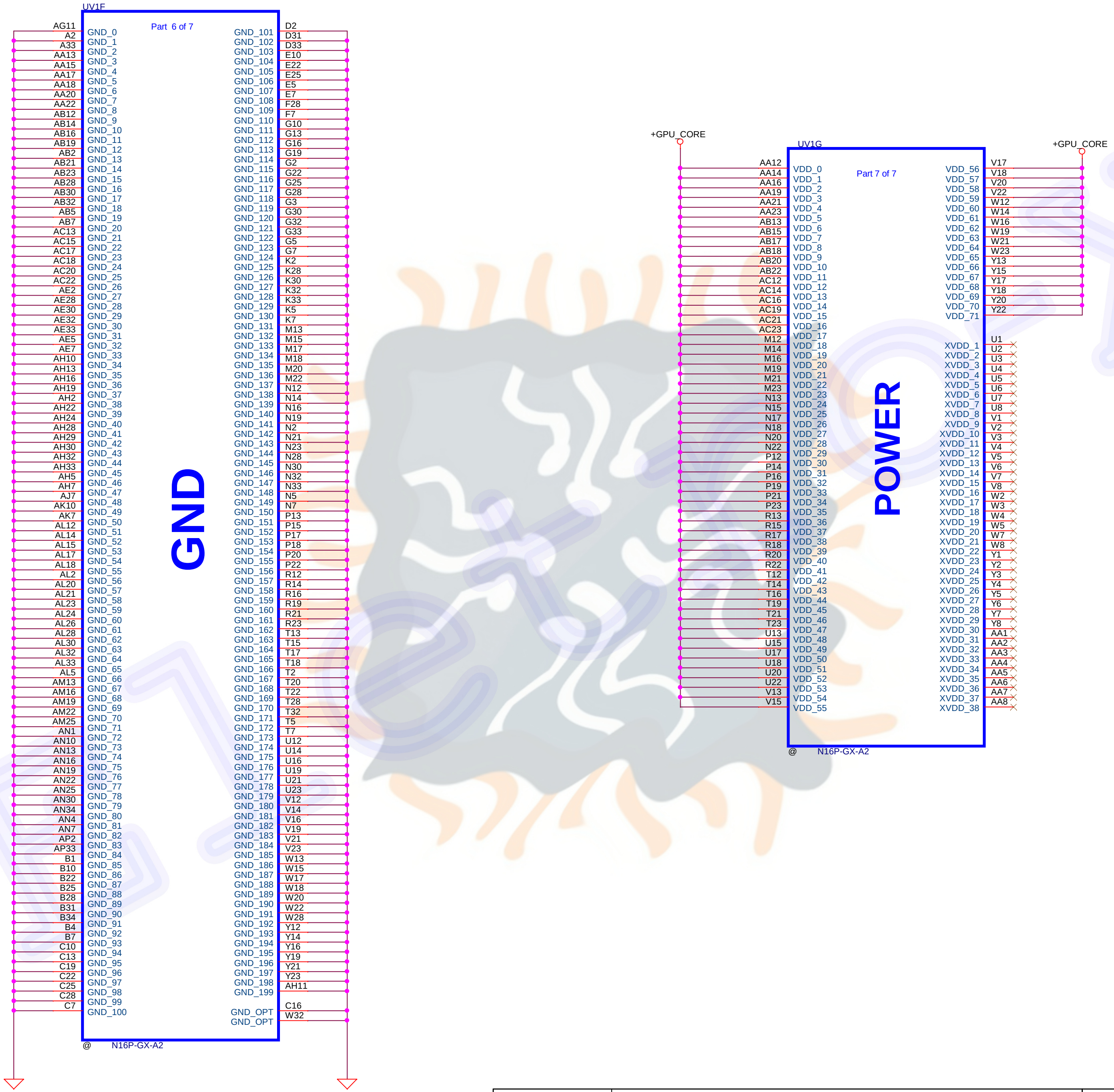


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/08/08	Deciphered Date	2014/07/01	Title: N15P (3/5)-Power
				Size / Document Number / Rev 0.1(X00)
				Date: Thursday, August 06, 2015 / Sheet 25 of 71



Security Classification	Compal Secret Data		
Issued Date	2014/08/08	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title

N15P (4/5)-Power / GND

Size Document Number Rev 0.1(X00)

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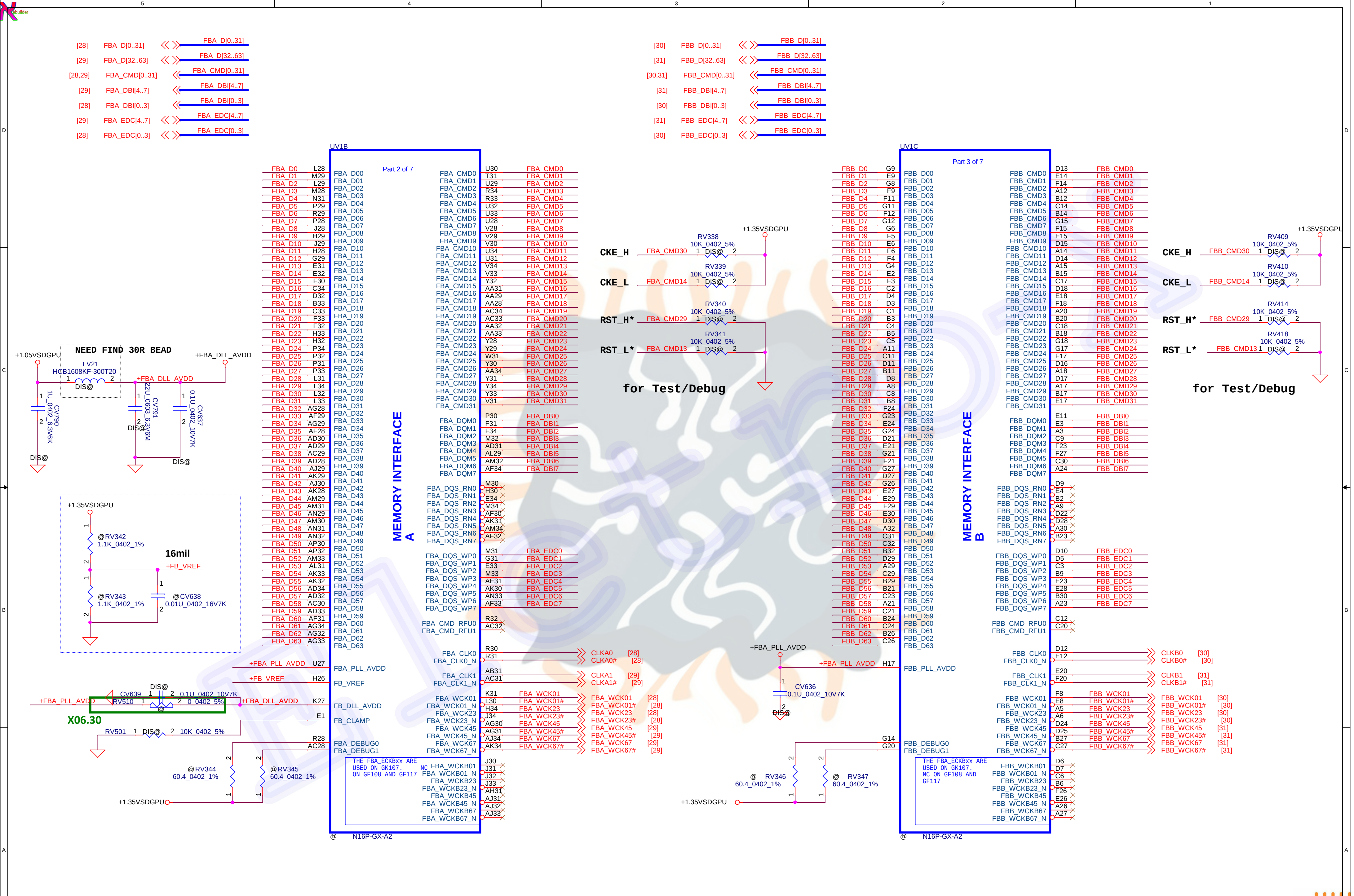

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Issued Date	2014/08/08	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: **N15P (5/5)-Memory A/B**

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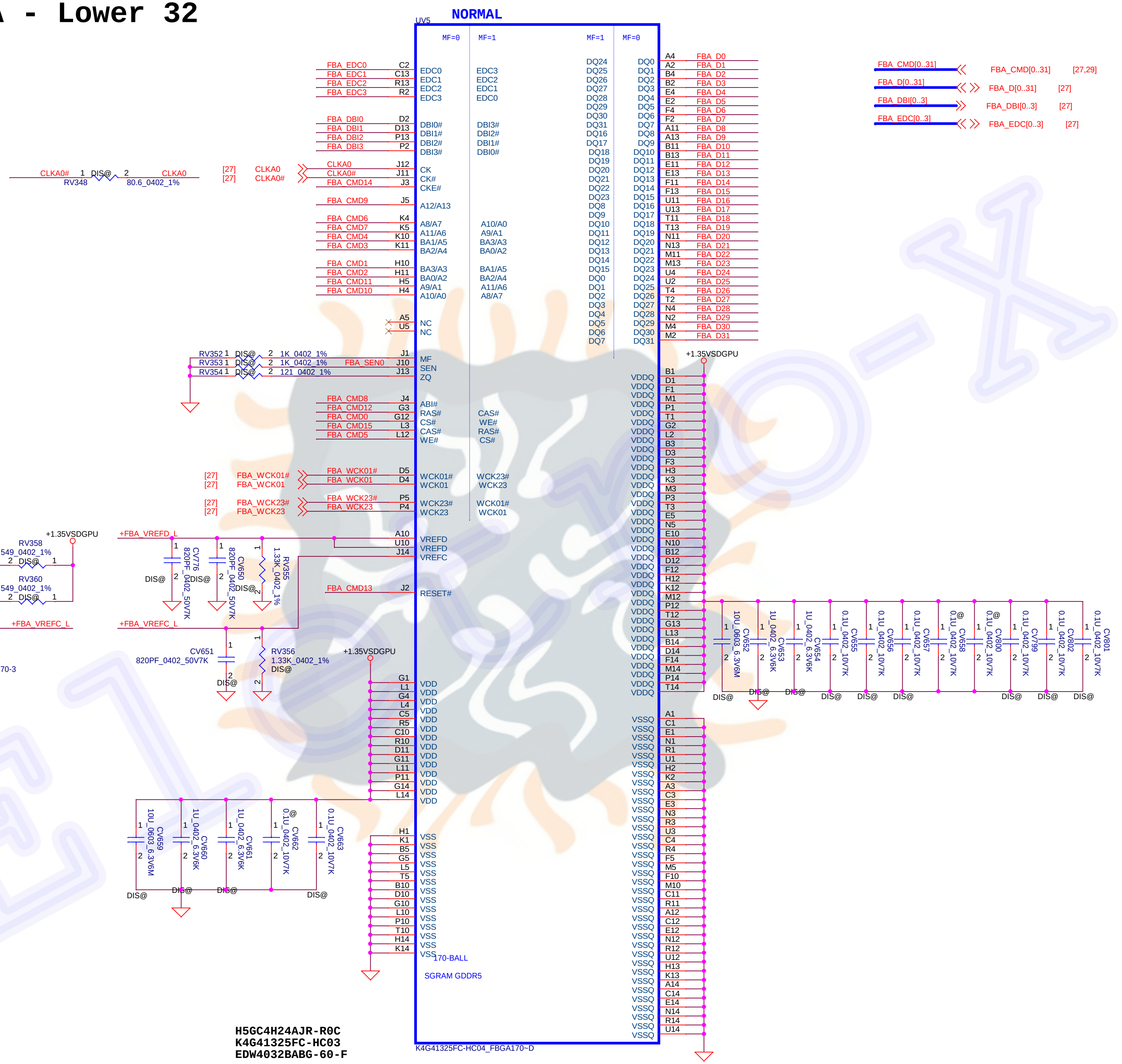
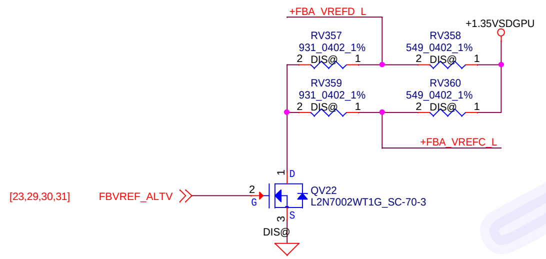
Memory Partition A - Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*





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Issued Date	2014/08/08	Deciphered Date	2014/07/01

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Compal Electronics, Inc.

Title: VRAM_GDDR5_A Lower

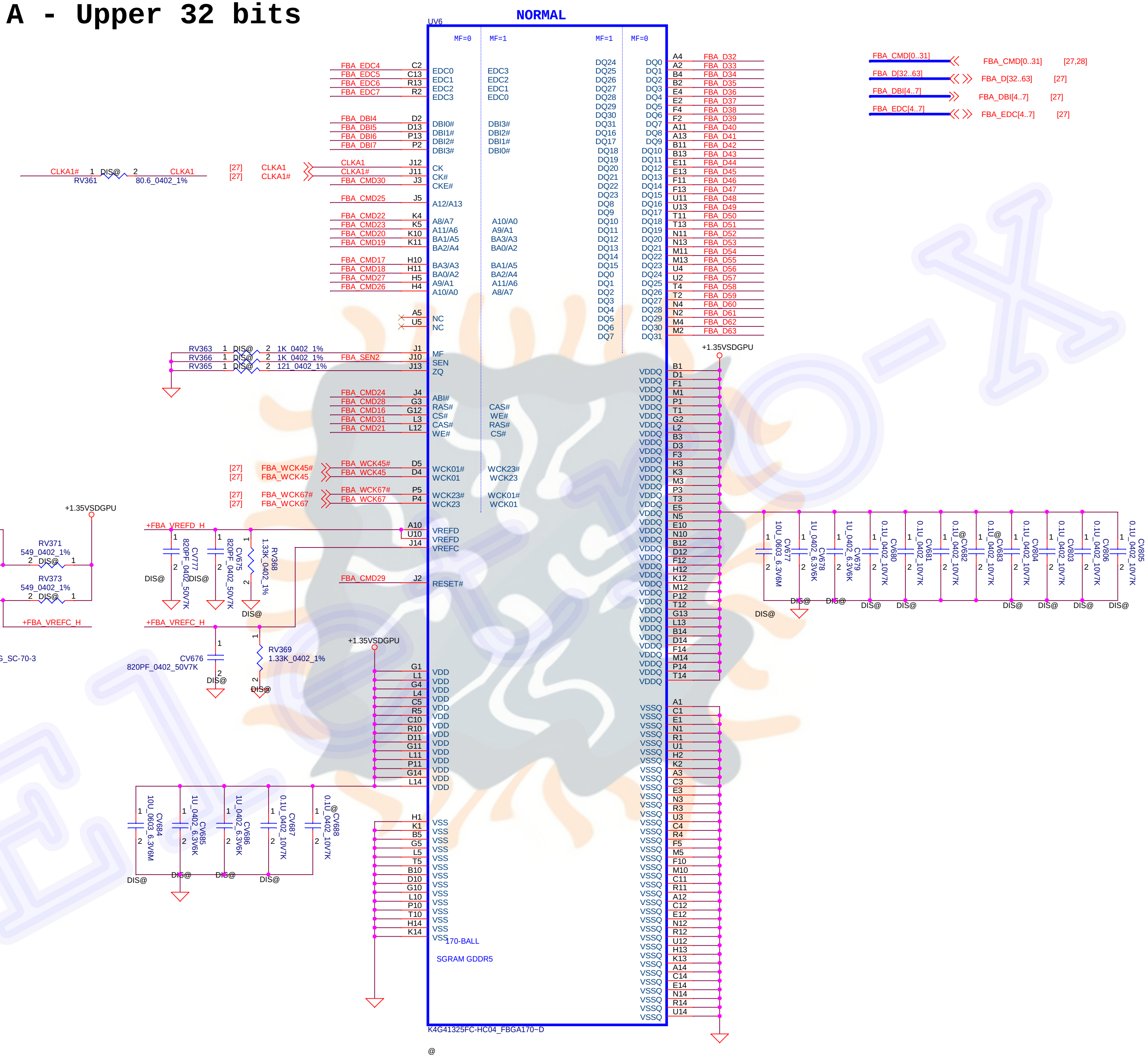
Size | Document Number | Rev 0.1(X06)

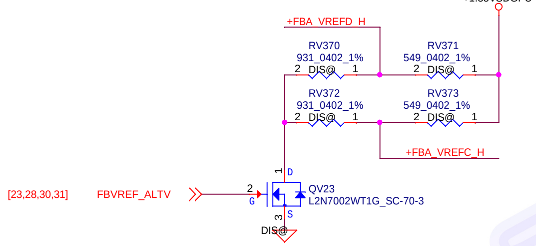
Date: Thursday, August 06, 2015 | Sheet 28 of 71

Memory Partition A - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*





Security Classification	Compal Secret Data		
Issued Date	2014/08/08	Deciphered Date	2014/07/01

Compal Electronics, Inc.

Title: VRAM_GDDR5_A Upper

Size | Document Number | Rev 0.1(X00)

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Memory Partition B - Lower 32 bits

64X32 GDDR5

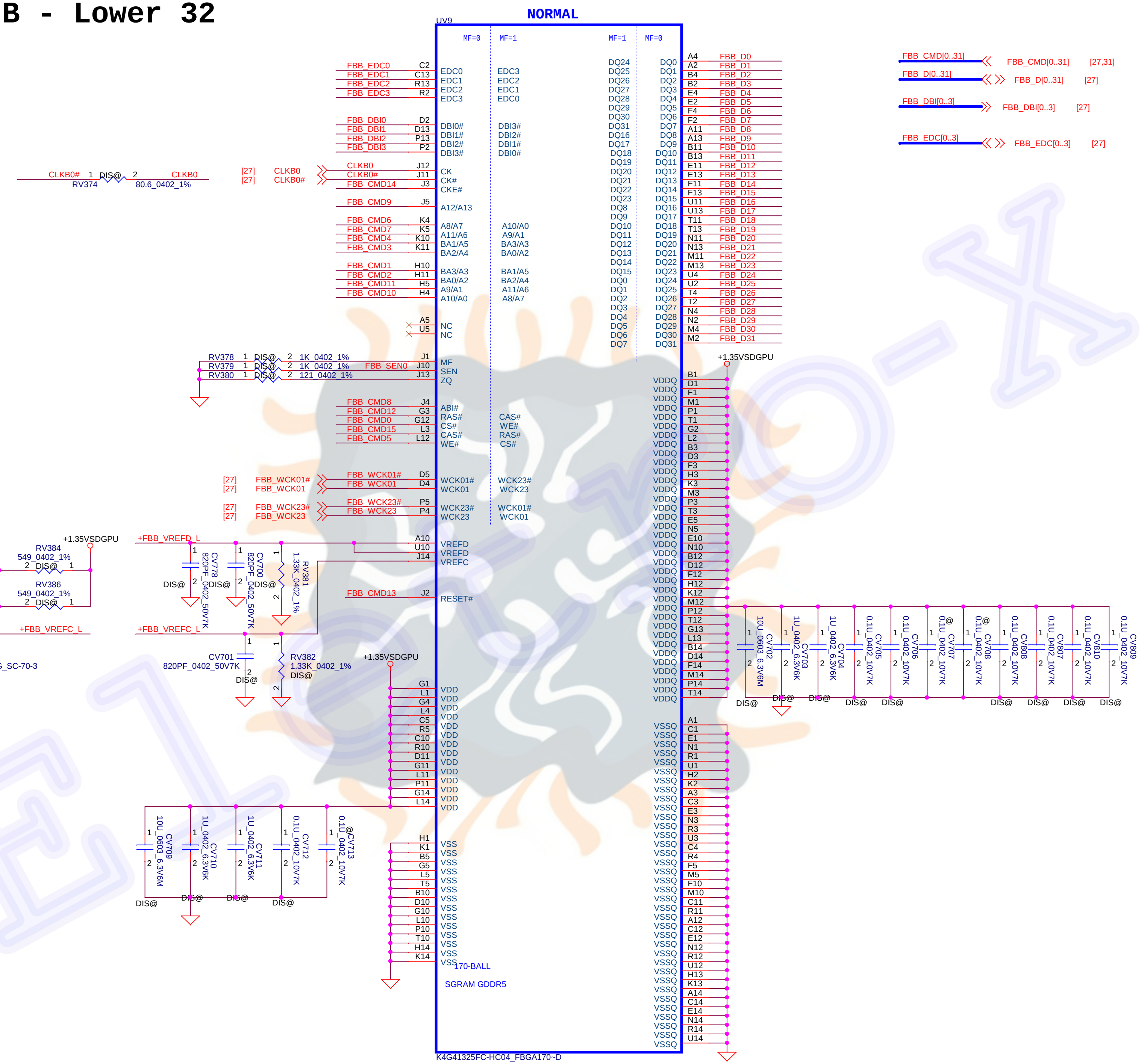
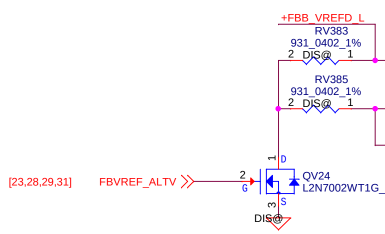


Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



Security Classification	Compal Secret Data		
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Title: *VRAM_GDDR5_B Lower*

Document Number | Rev 0.1(A00)

Date: Thursday, August 06, 2015 | Sheet 30 of 71

Memory Partition B - Upper 32 bits

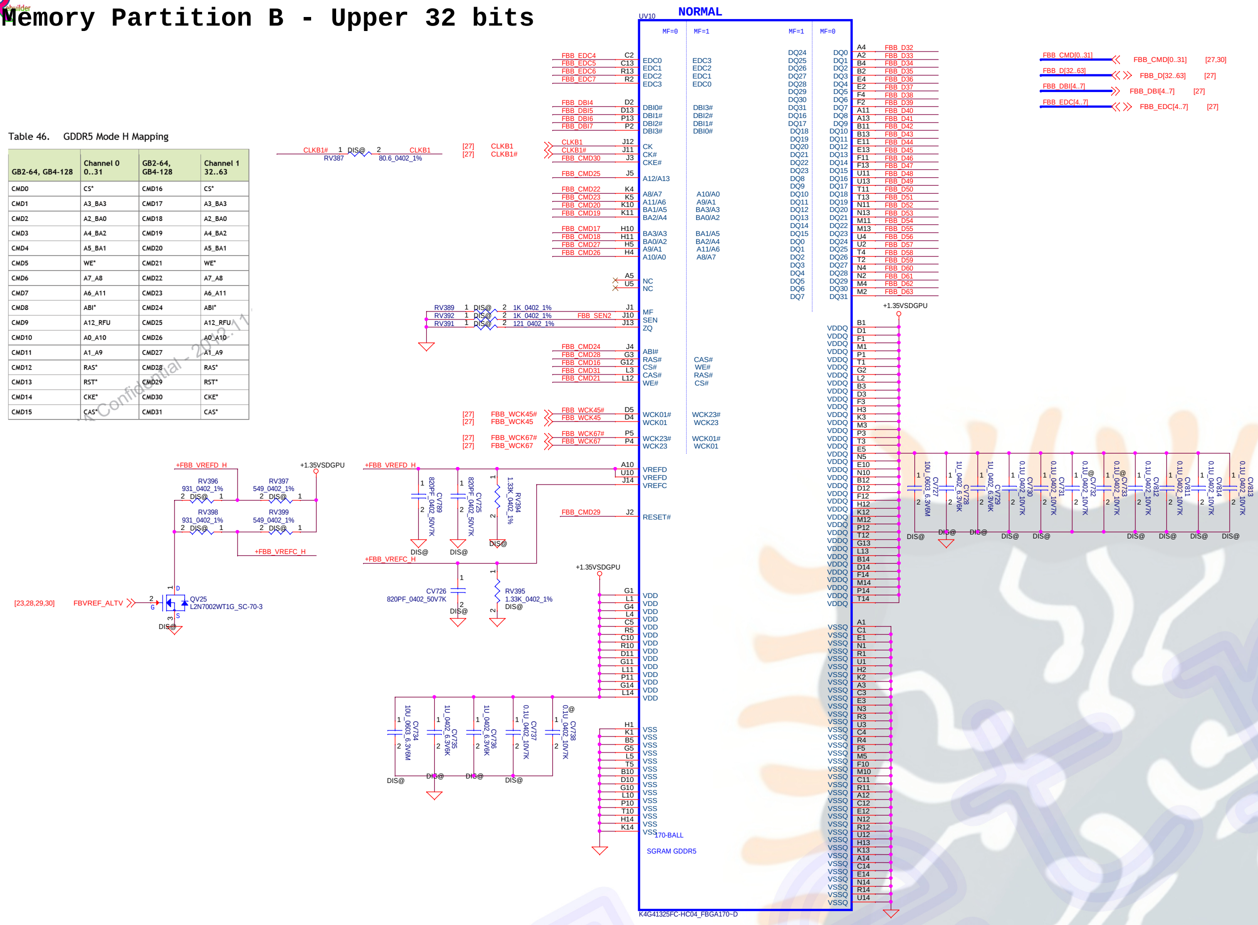


Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

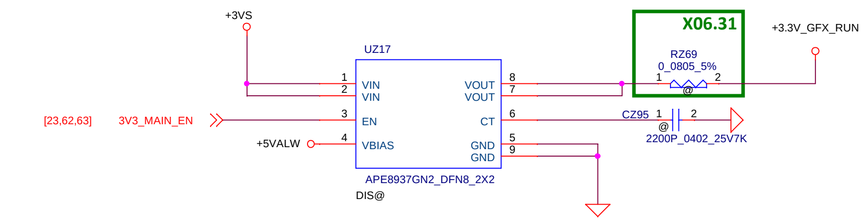
Security Classification	Compal Secret Data		
Issued Date	2014/08/08	Deciphered Date	2014/07/01

Compal Electronics, Inc.

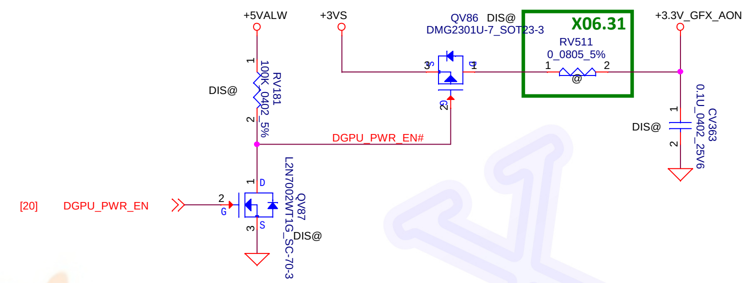
Title: *VRAM_GDDR5_B Upper*

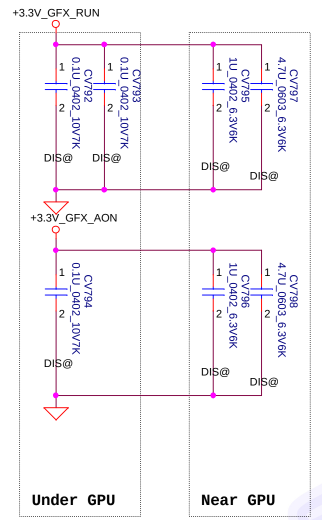
Size | Document Number | Rev 0.1(X00)

+3.3V_GFX_RUN

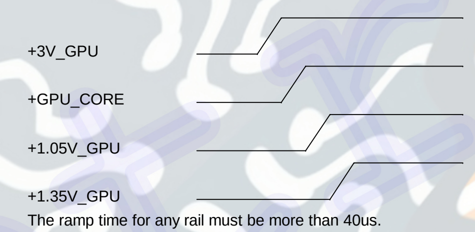


+3VALW to +3.3V_GFX_AON



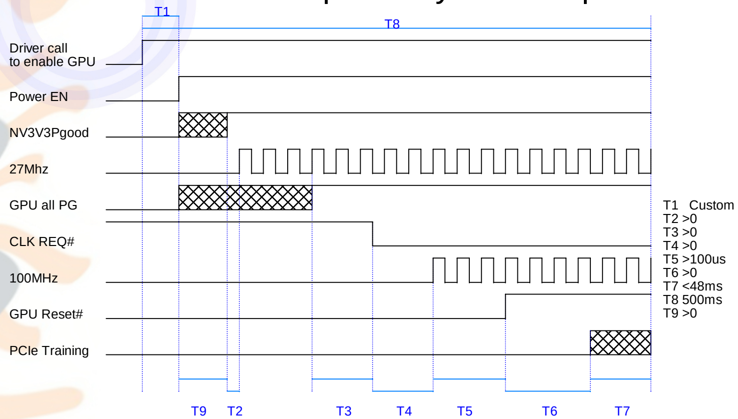


GPU Power Up Power Rail Sequence

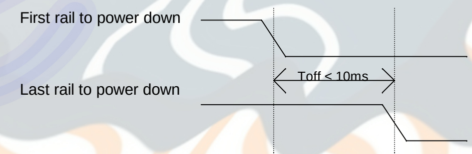


The ramp time for any rail must be more than 40us.

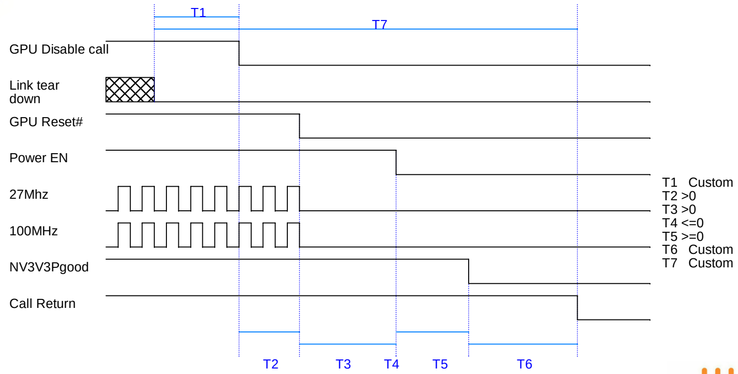
GPU Power Up Sub-system Sequence



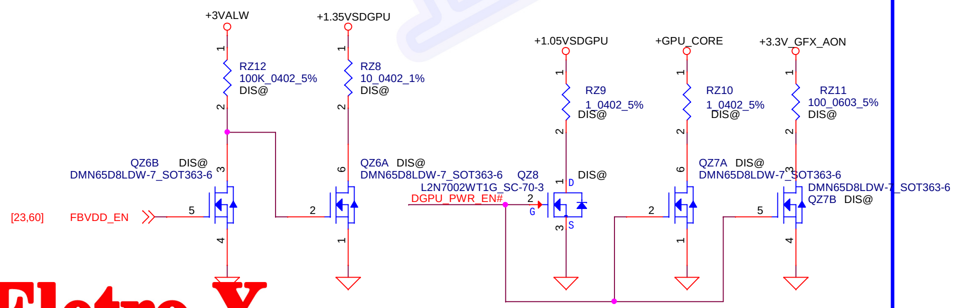
GPU Power Down Sequence



GPU Power Down Sub-system Sequence



Discharge



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: GPU DC/DC interface

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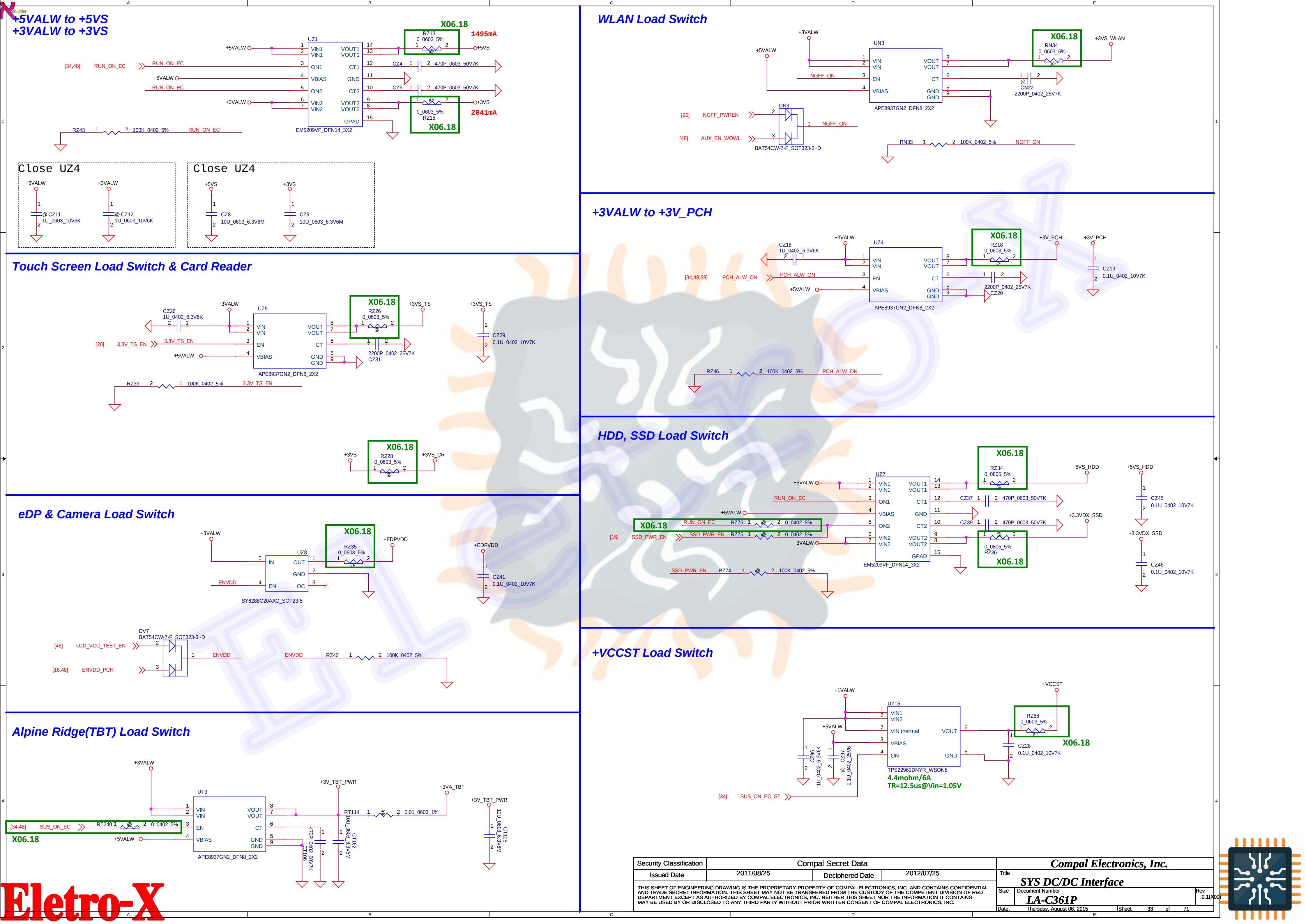
Date: Thursday, August 06, 2015 | Sheet 32 of 71



+5VALW to +5VS
+3VALW to +3VS
1495mA
2041mA
Close UZ4
Close UZ4
WLAN Load Switch
+3VALW to +3V_PCH
Touch Screen Load Switch & Card Reader
HDD, SSD Load Switch
eDP & Camera Load Switch
+VCCST Load Switch
Alpine Ridge(TBT) Load Switch
4.4mohm/6A
TR=12.5us@Vin=1.05V
Security Classification
Compal Secret Data
Issued Date
2011/08/25
Deciphered Date
2012/07/25
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Compal Electronics, Inc.
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SYS DC/DC Interface
Size
Document Number
LA-C361P
Rev
0.1(X00)
Date: Thursday, August 06, 2015
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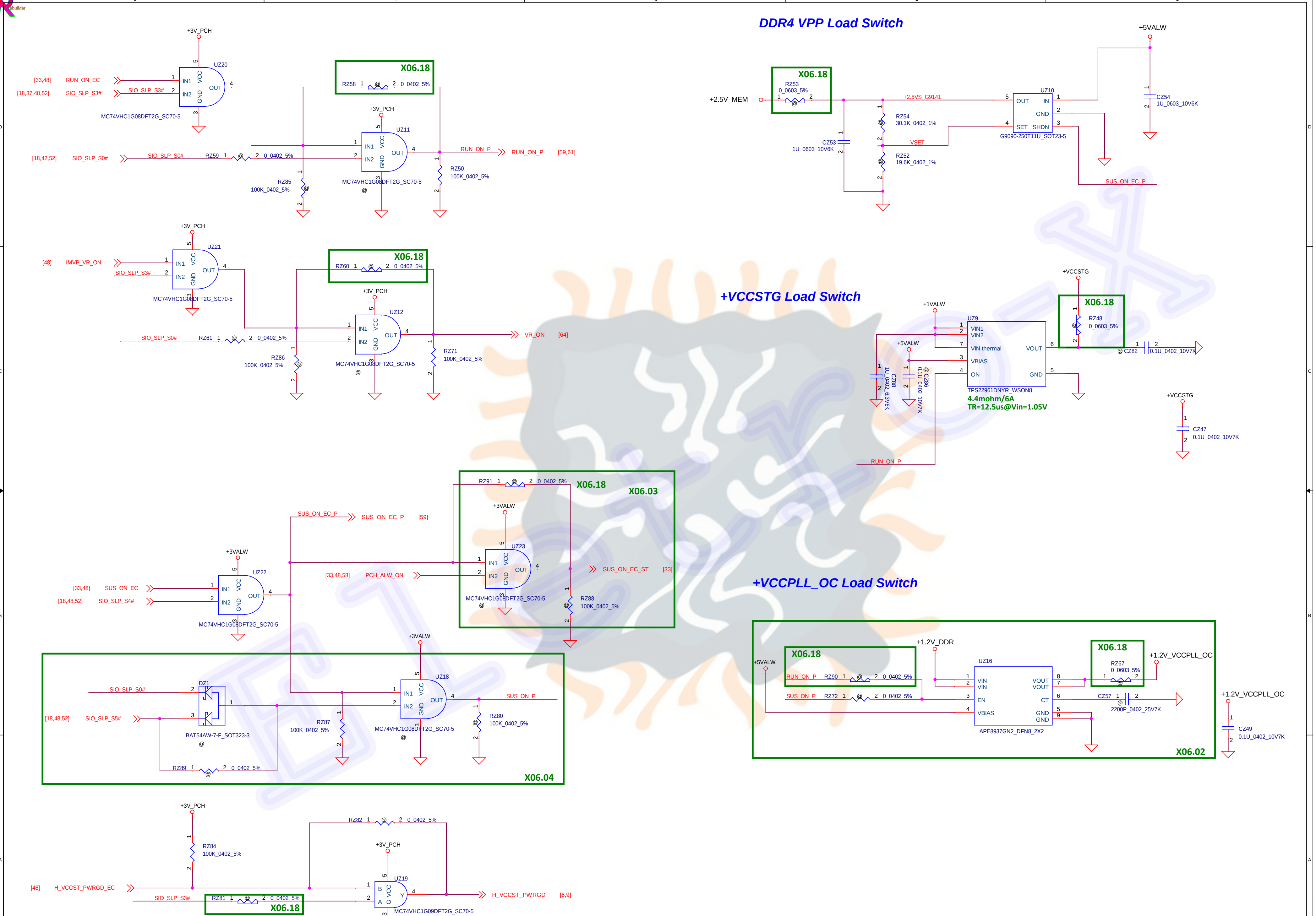
Eletro-X



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Compal Electronics, Inc.

Title: EC ENE-KB9012/ KC3810

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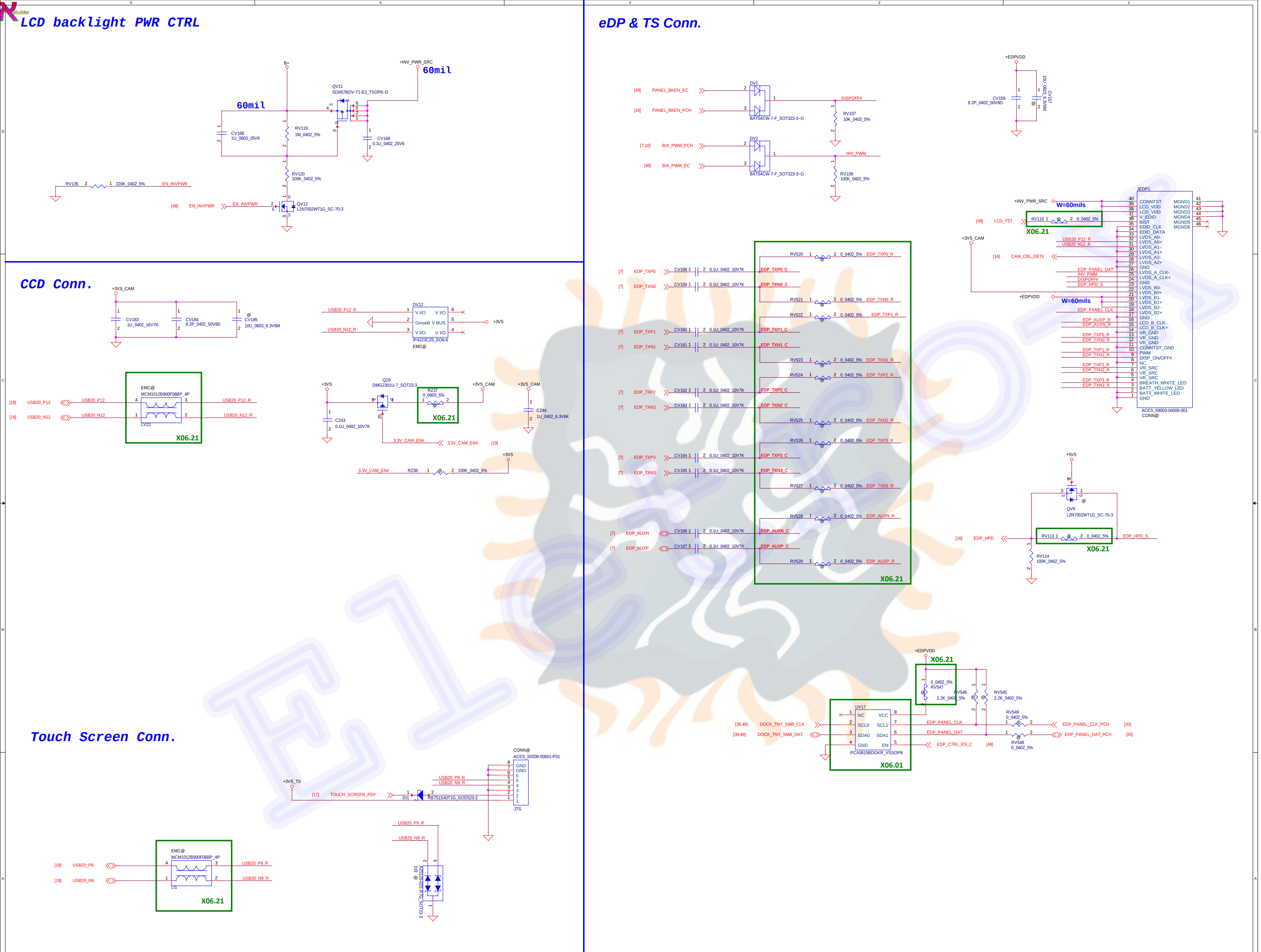
Date: Thursday, August 06, 2015 | Sheet 34 of 71



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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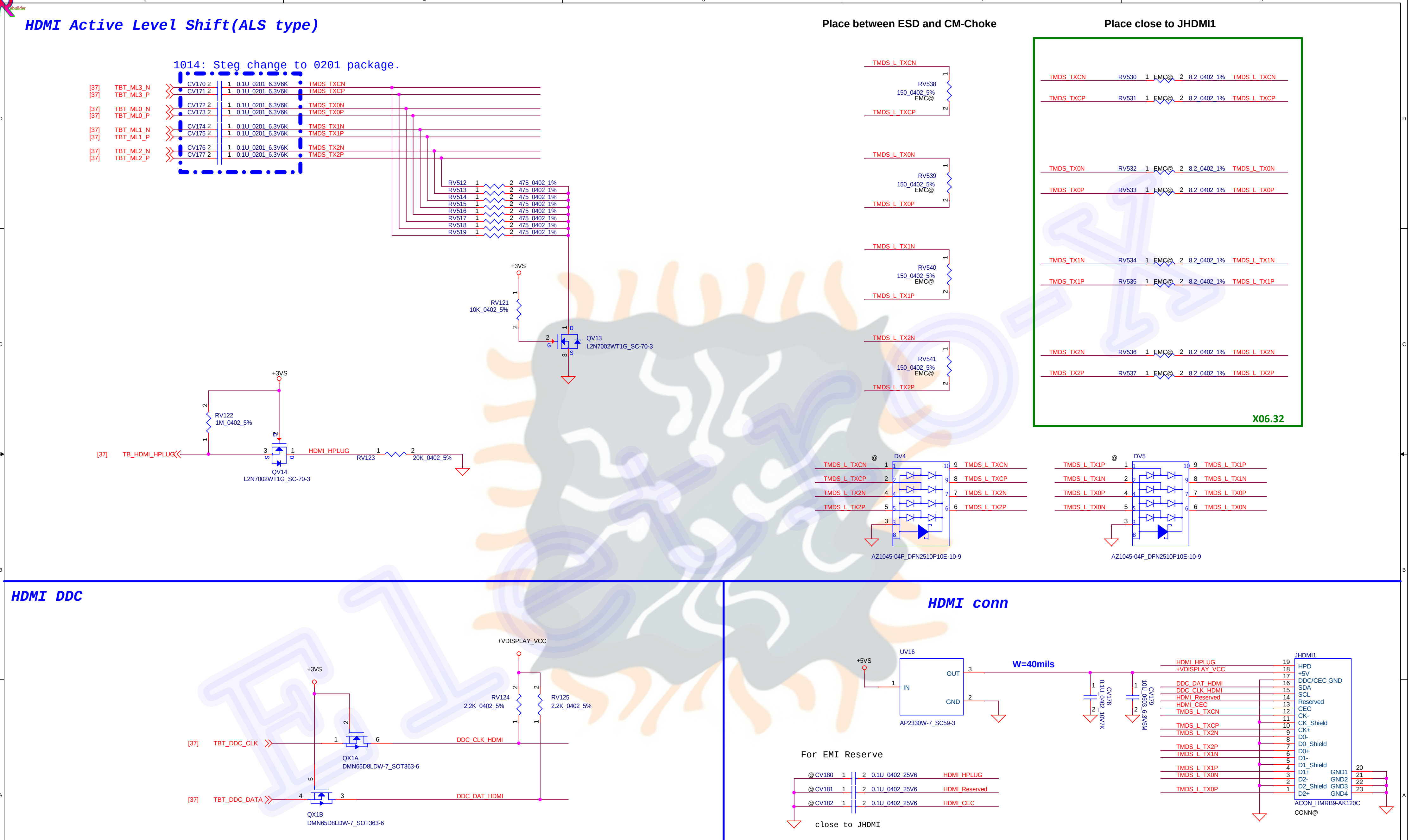
Compal Electronics, Inc.

Title: eDP /TS conn.

Size | Document Number: LA-C361P | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 35 of 71



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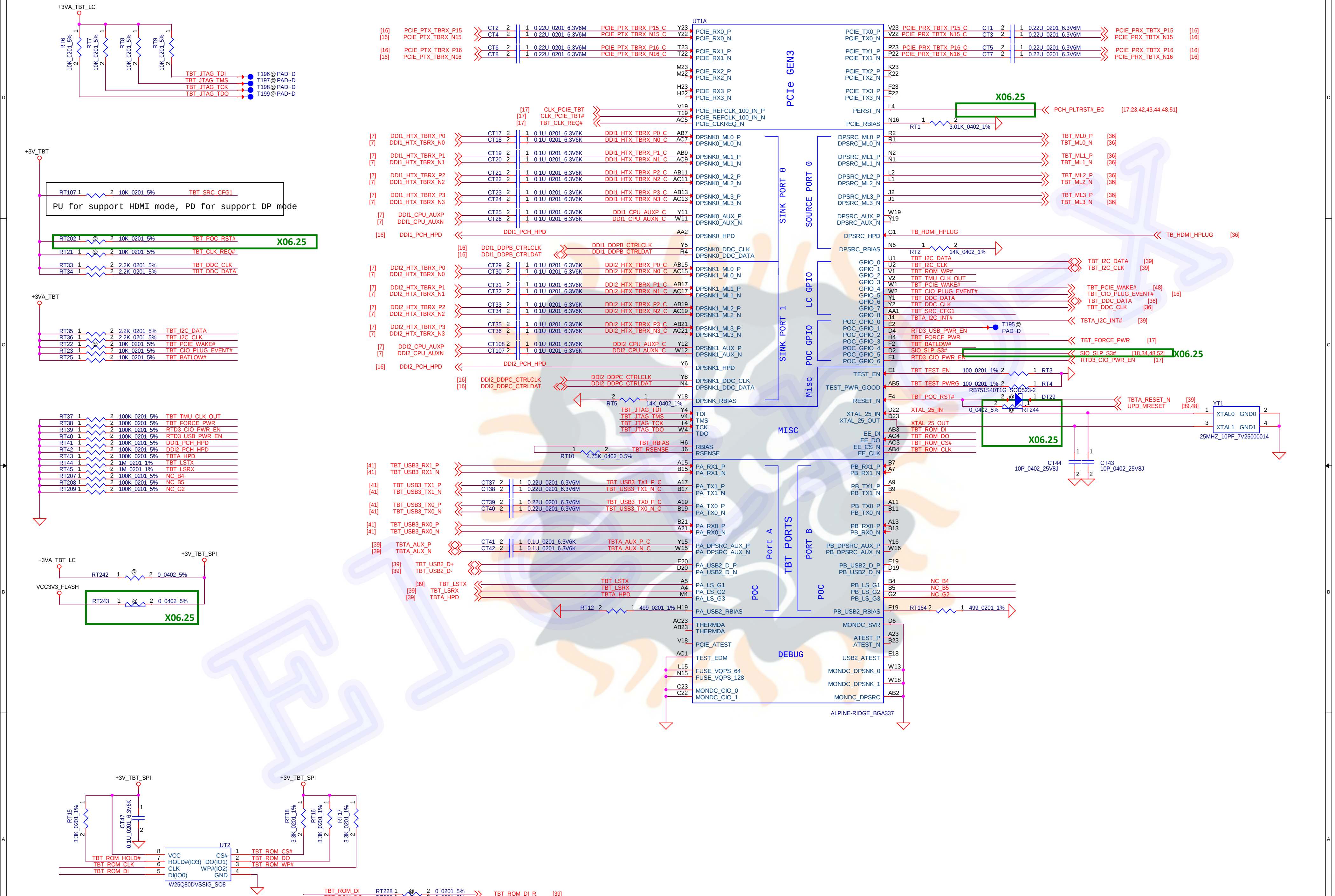
				Date: Thursday, August 06, 2015; Sheet 36 of 71

Eletro-X



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Issued Date	2014/01/20	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: AR_TBT (1/2) DP / PCIE

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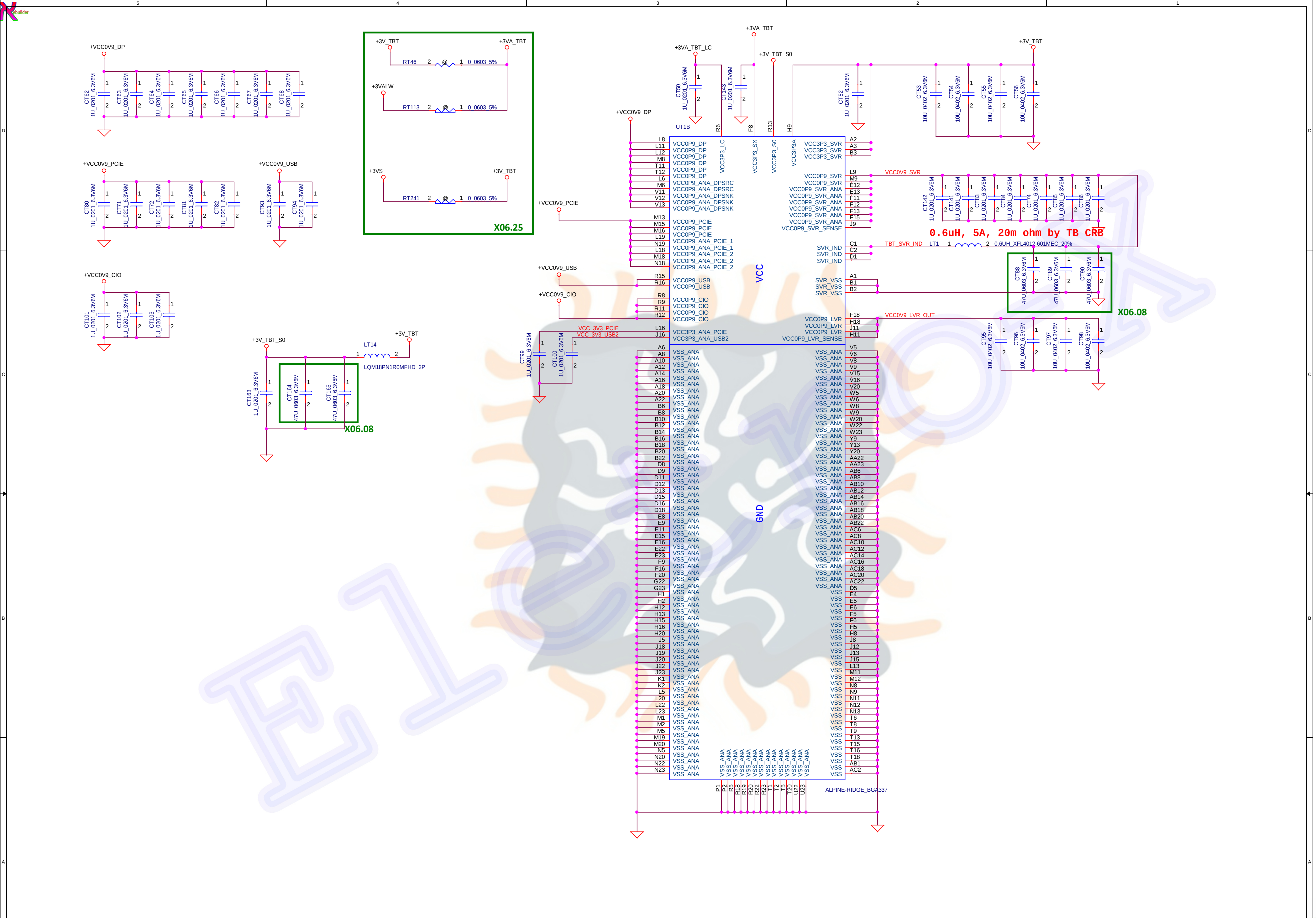
Eletro-X



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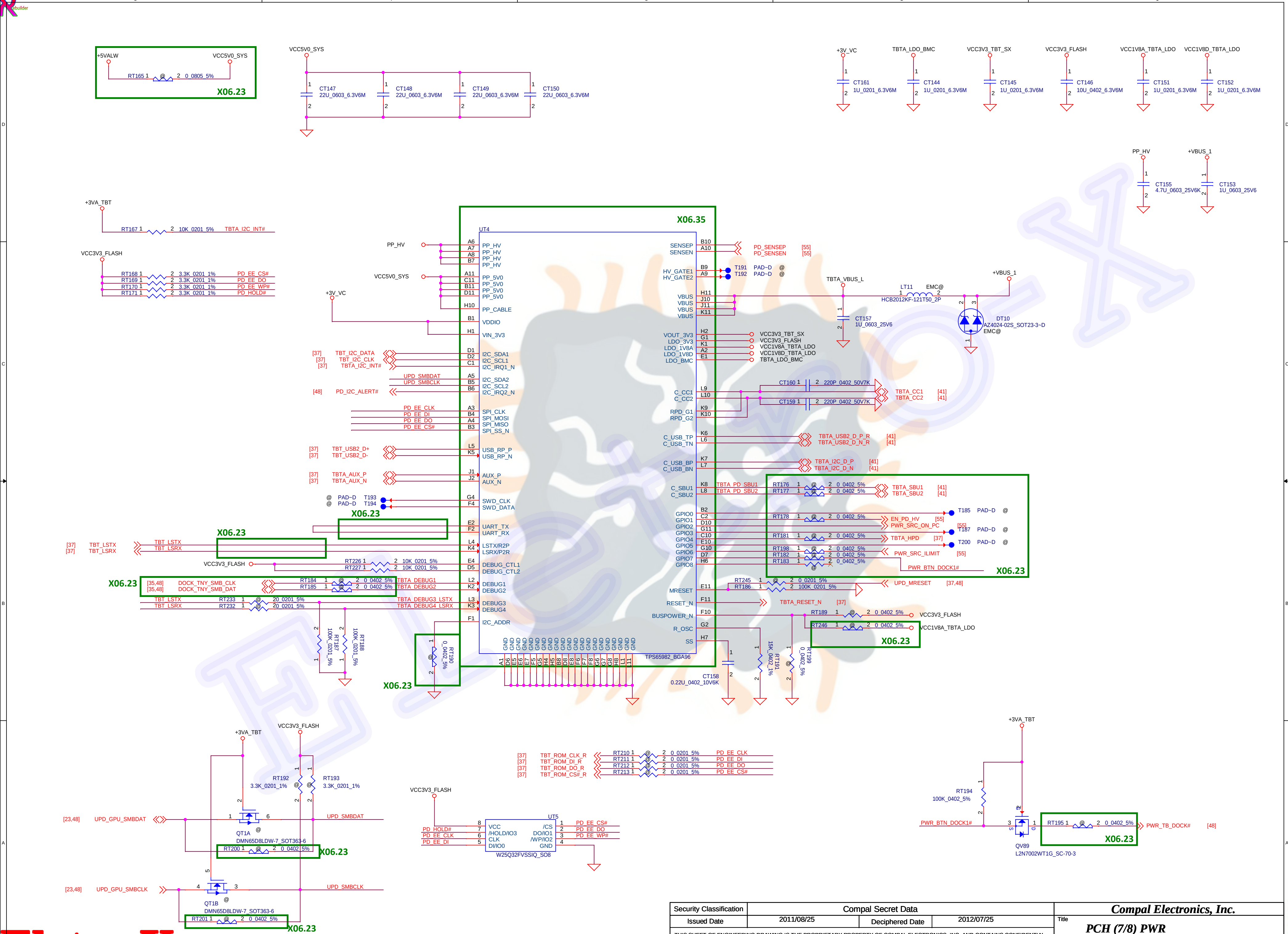
Compal Electronics, Inc.

Title: *AR_TBT (2/2) PWR / GND*

Size: C | Document Number: *LA-C361P* | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 38 of 71



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: PCH (7/8) PWR

Size | Document Number: LA-C361P | Rev: 0.1(X00)

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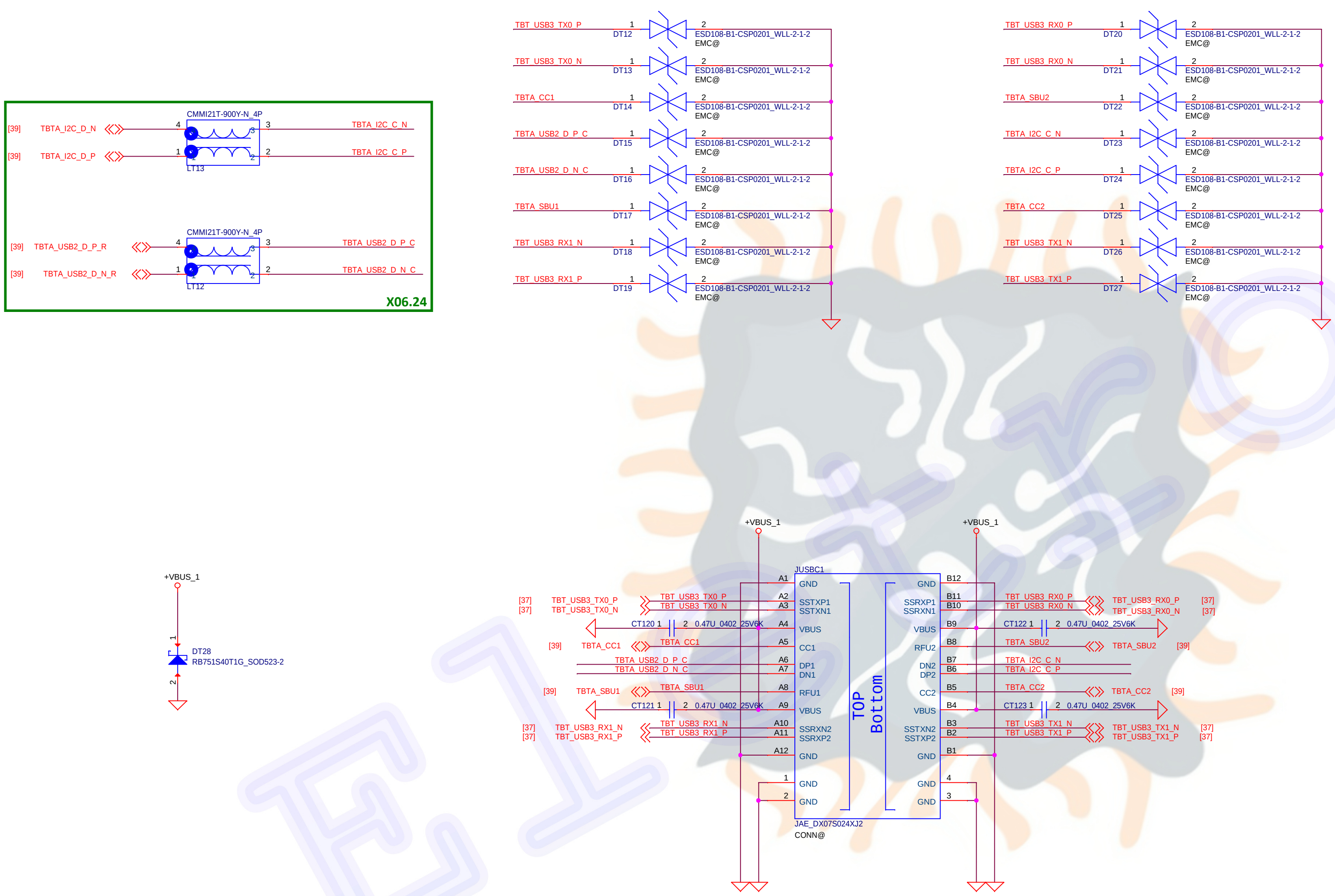

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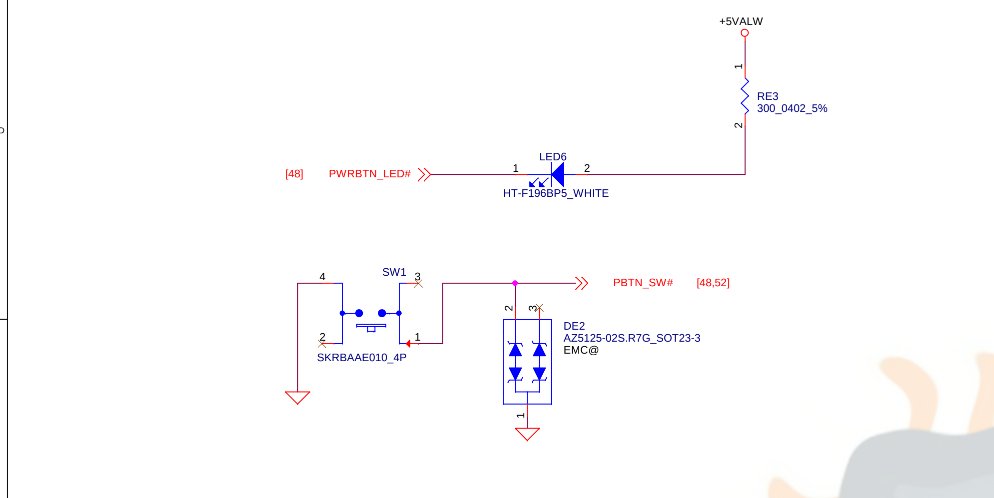
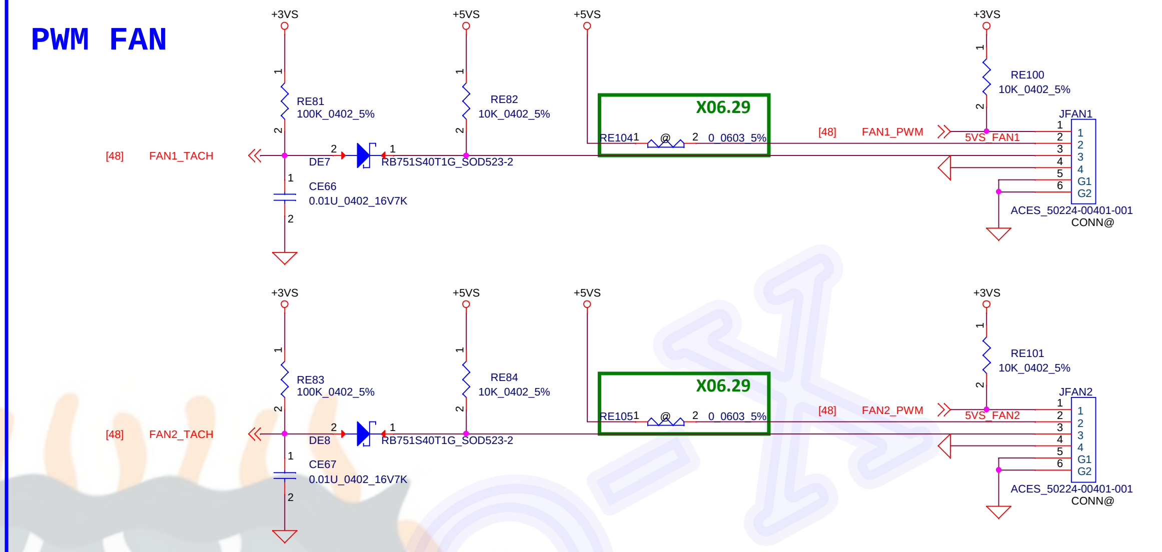
				Date: Thursday, August 06, 2015; Sheet 41 of 71

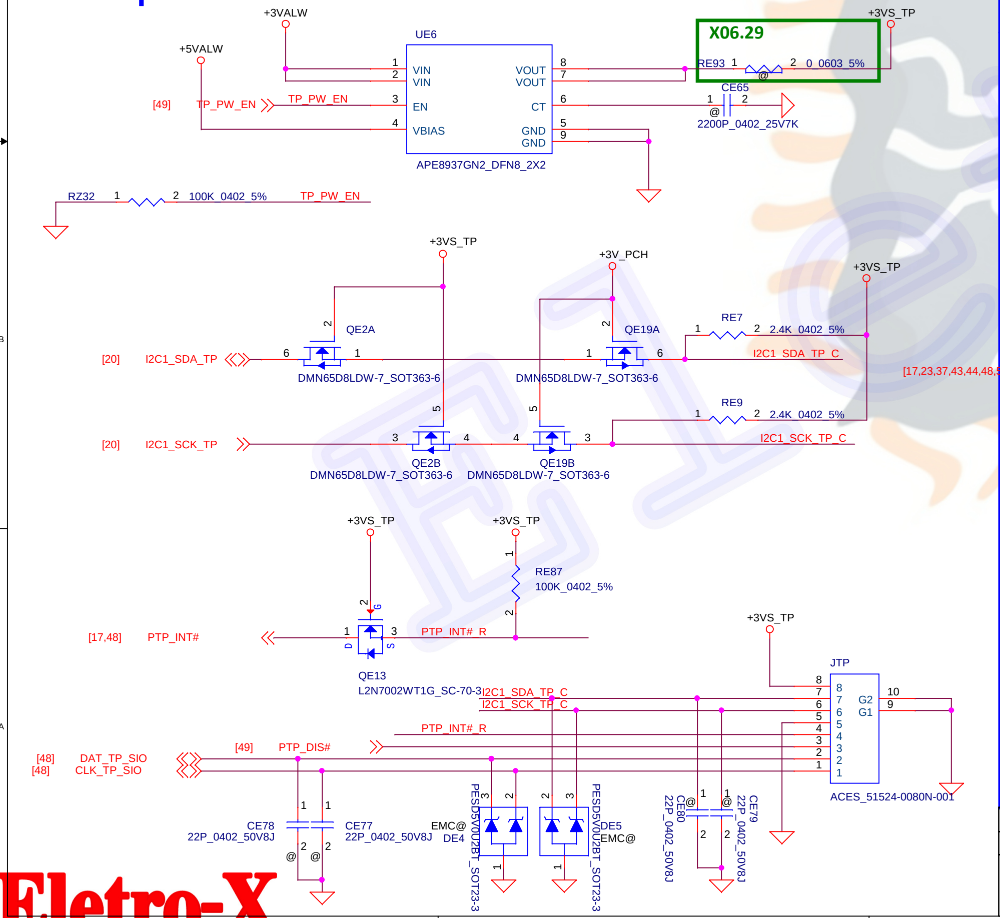
Power Button and LED



PWM FAN

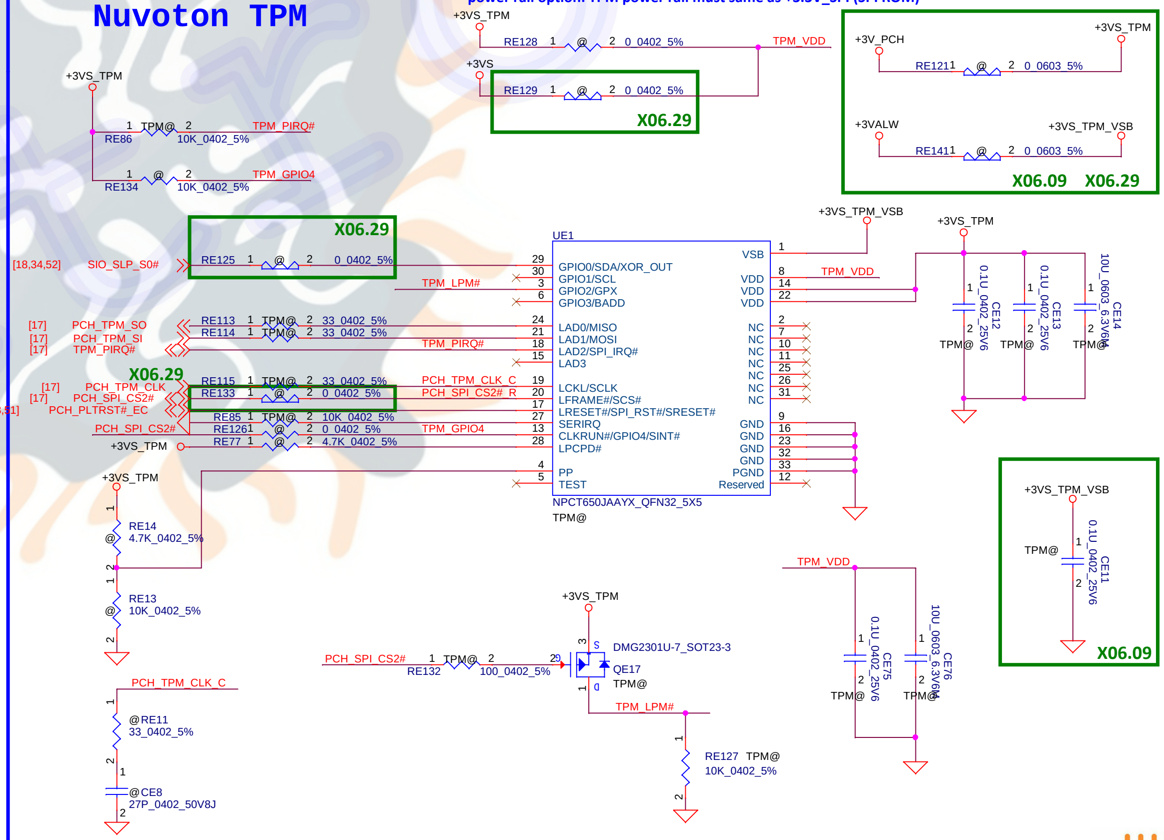


Touch pad



Nuvoton TPM

power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)



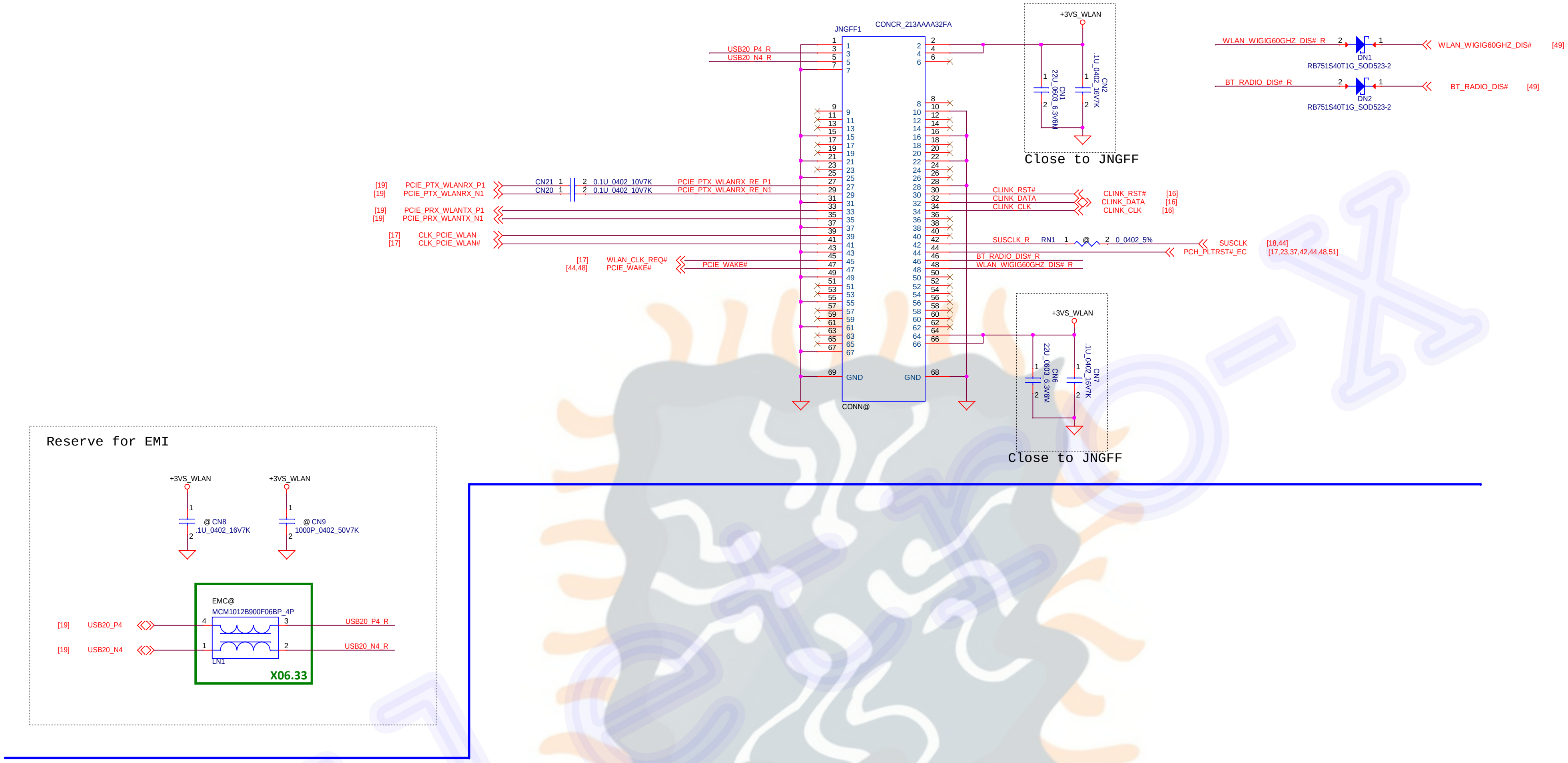
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **FAN/TP/KB/PWR SW**

Size: Custom | Document Number: LA-C361P | Rev: 1.0(0.0)

M.2 Slot-A Key-A (WLAN + BT)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: NGFF
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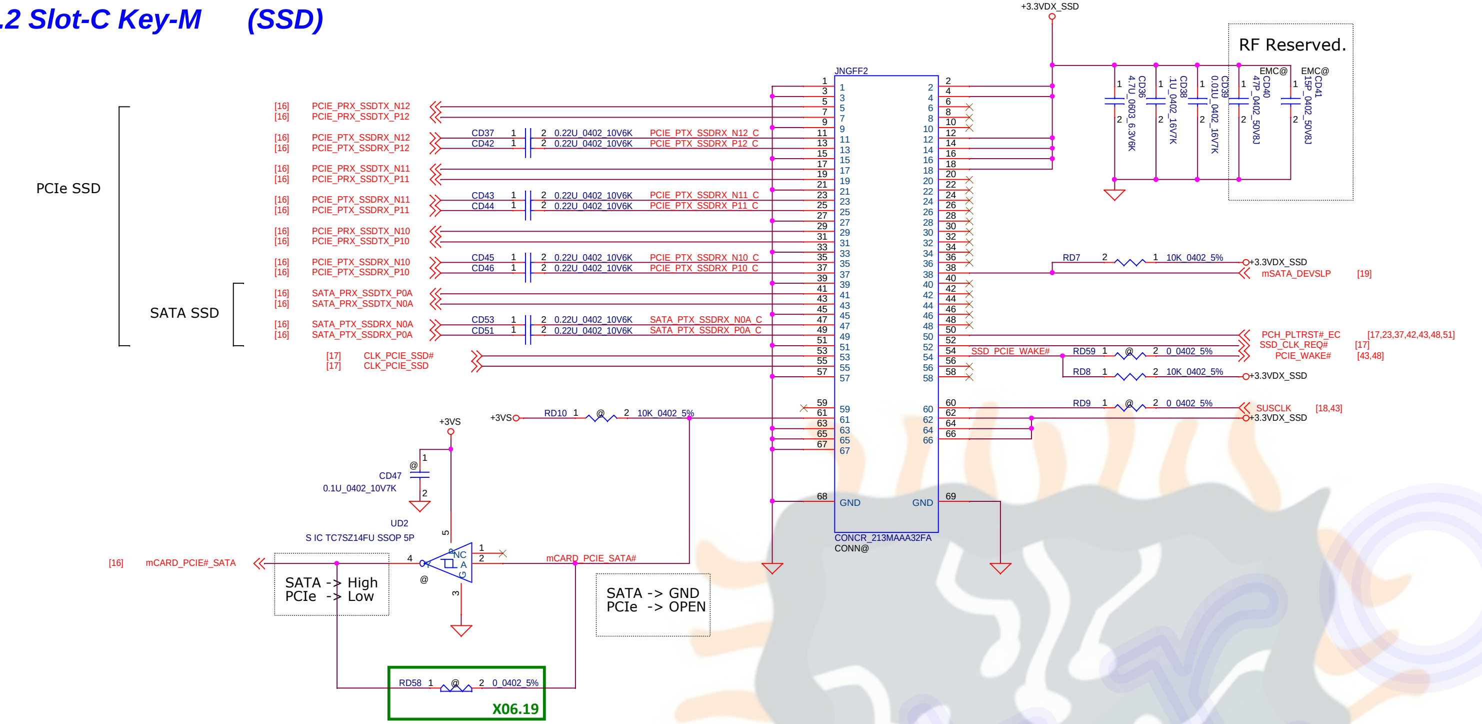
				Date: Thursday, August 06, 2015; Sheet 43 of 71

M.2 Slot-C Key-M (SSD)



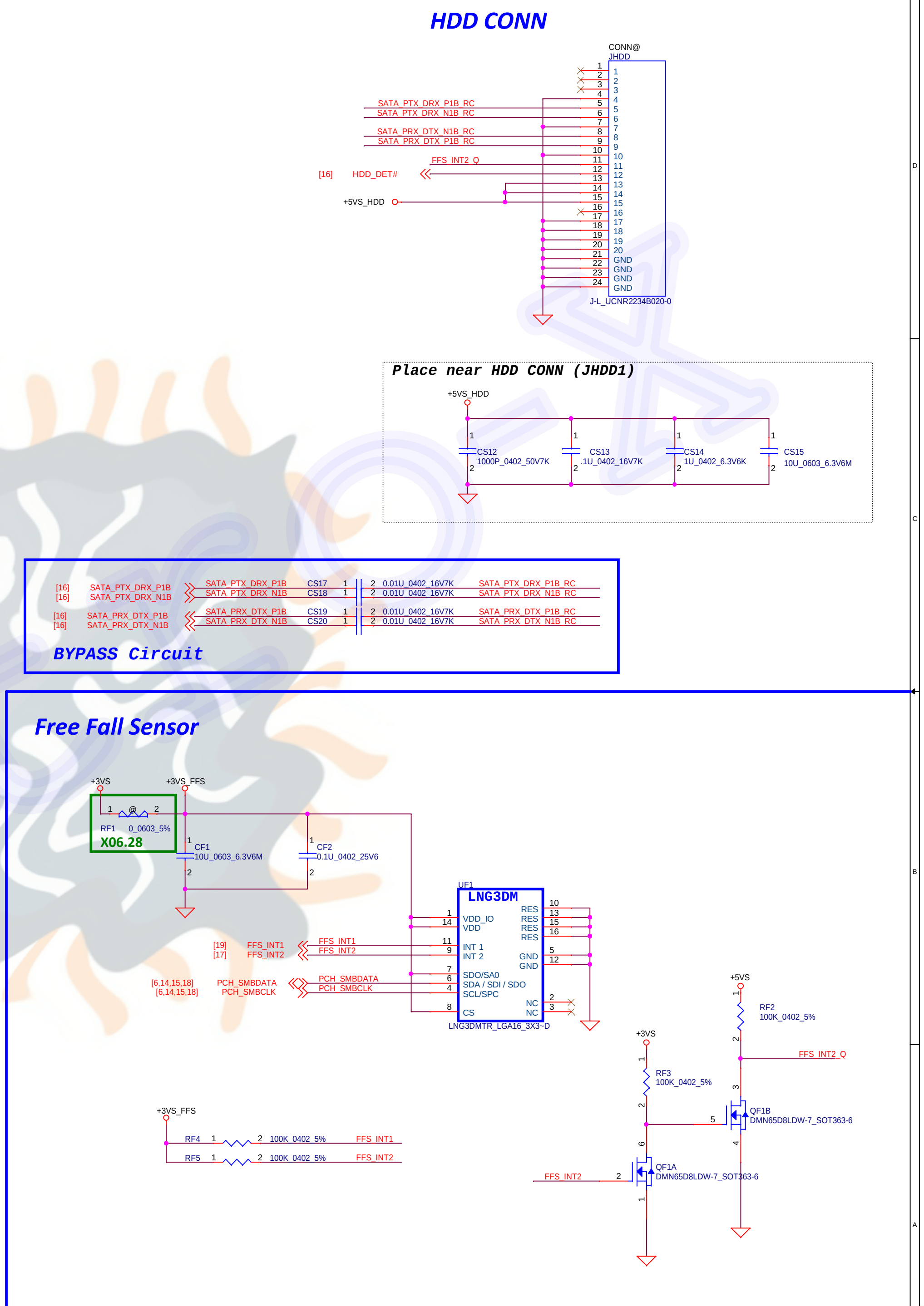
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: SSD

Size: C — Document Number: LA-C361P — Rev: 0.1(X00)

Date: Thursday, August 06, 2015 — Sheet 44 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: DC/DC INTERFACE

Size: C | Document Number: LA-C361P | Rev: 0.1(X00)

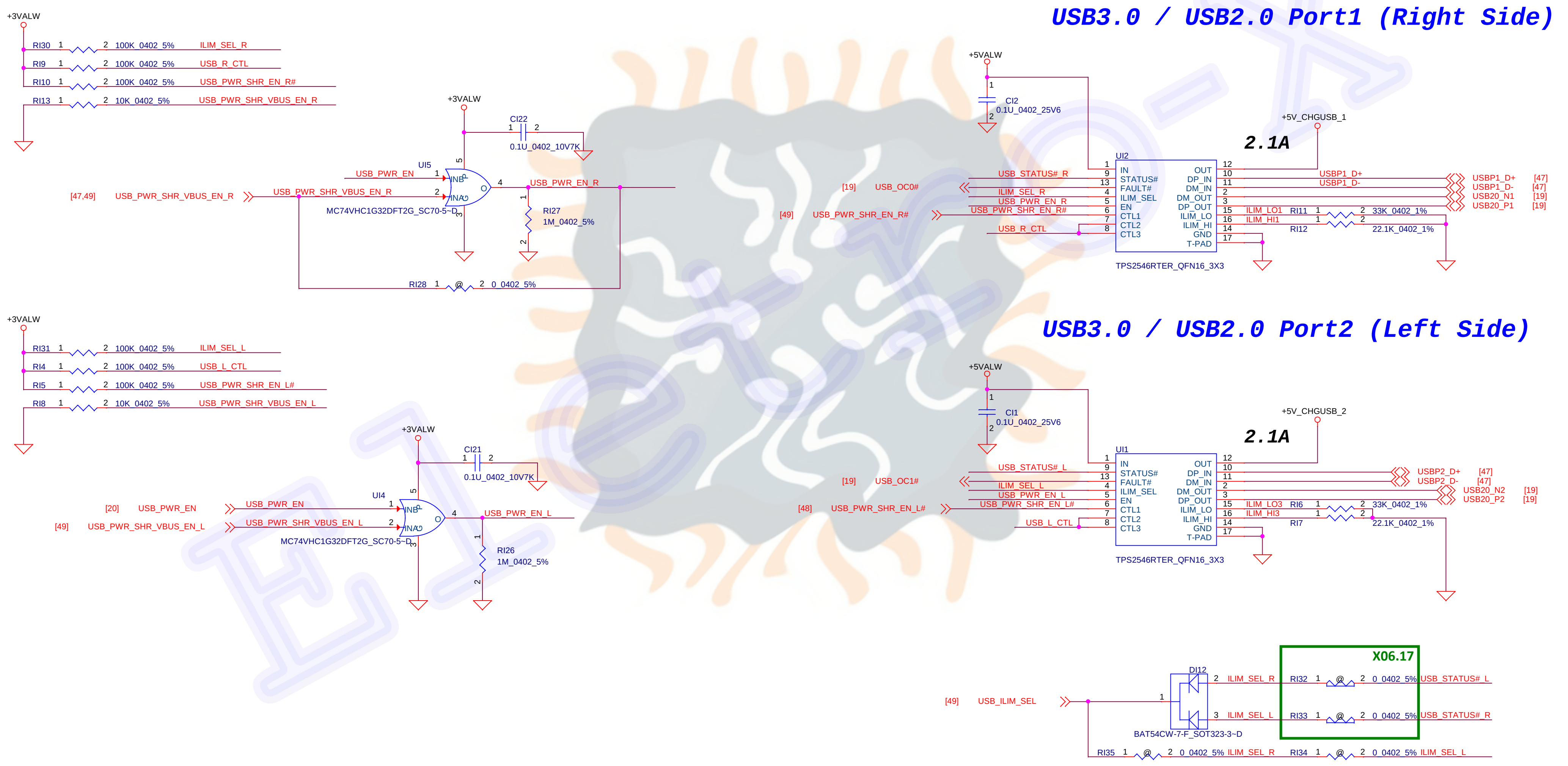
Date: Thursday, August 06, 2015 | Sheet 45 of 71

Eletro-X

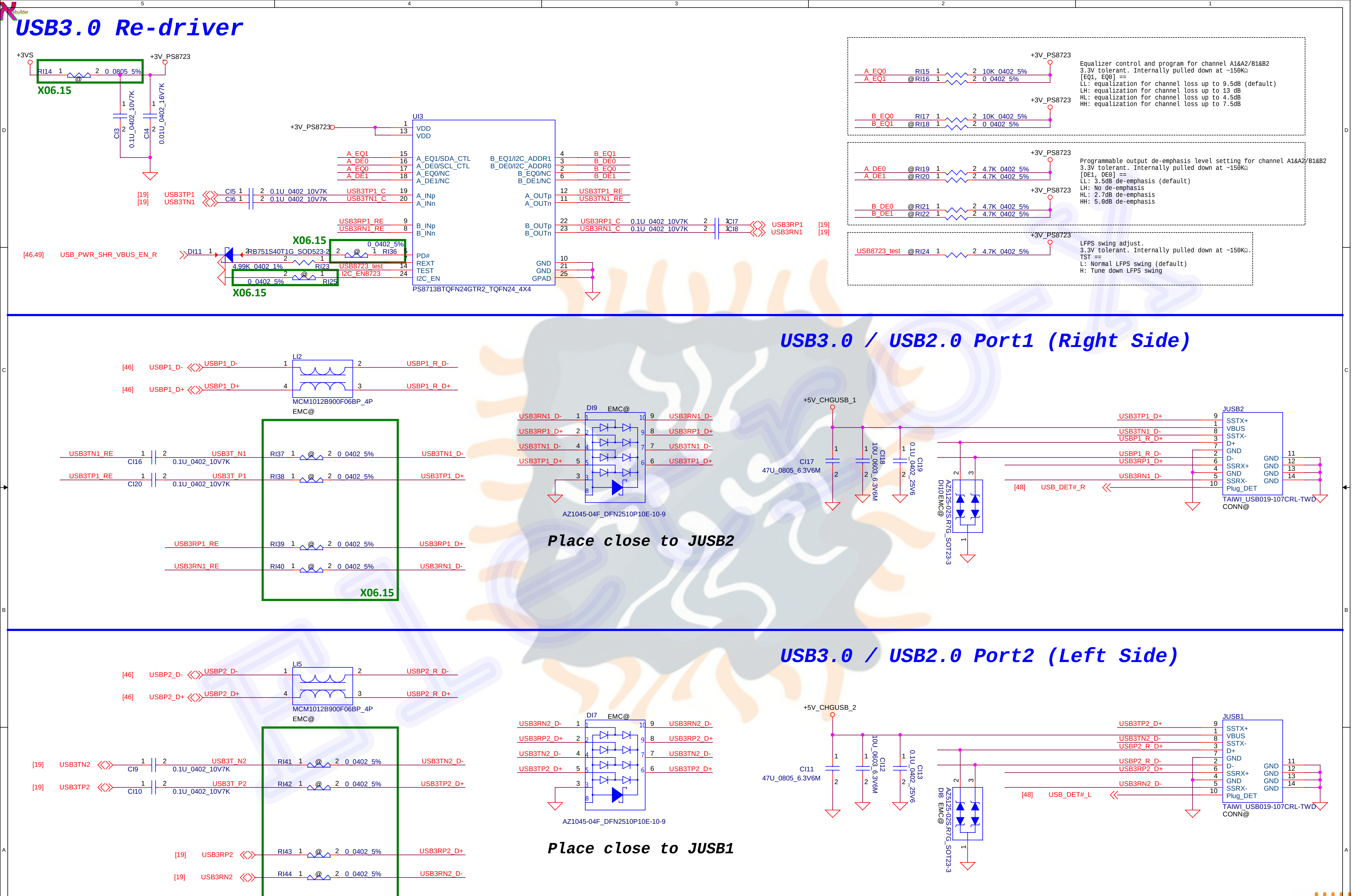
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: USB Powershare
				Size / Document Number: LA-C361P / Rev 0.1(A00)
				Date: Thursday, August 06, 2015 / Sheet 46 of 71



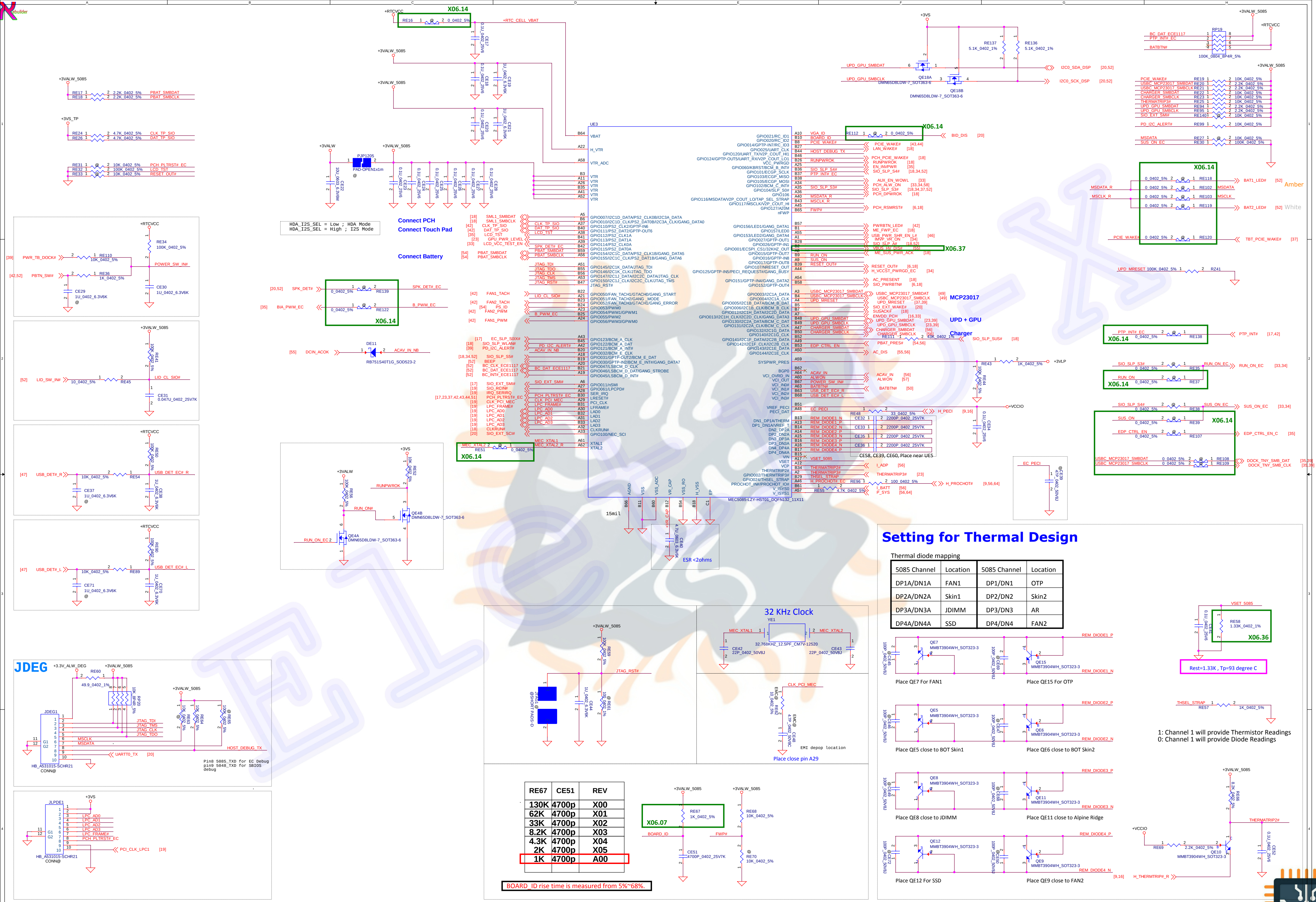
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: USB conn.

Size | Document Number: LA-C361P | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 47 of

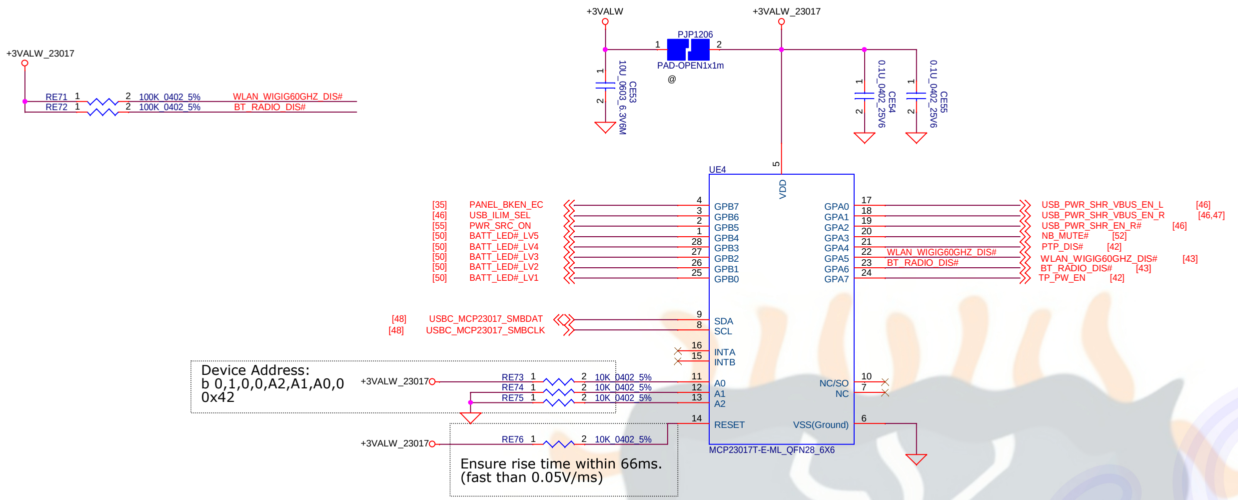


Setting for Thermal Design

Thermal diode mapping

5085 Channel	Location	5085 Channel	Location
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDIMM	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2

RE67	CE51	REV
130K	4700p	X00
62K	4700p	X01
33K	4700p	X02
8.2K	4700p	X03
4.3K	4700p	X04
2K	4700p	X05
1K	4700p	A00

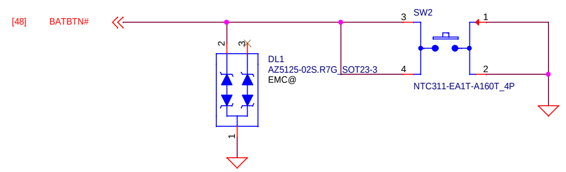


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/21

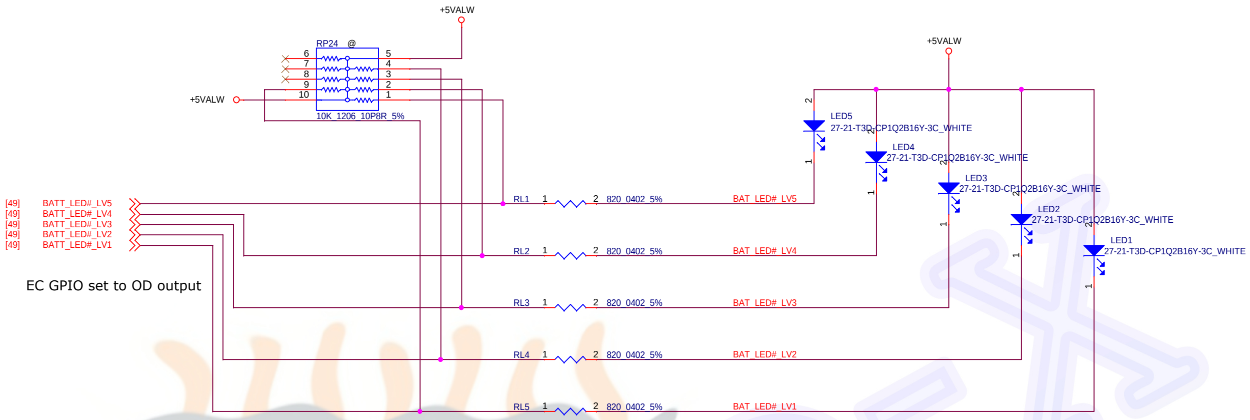
Compal Electronics, Inc.

Title	AMP TPA3113/SPK conn.	
Size C	Document Number LA-C361P	Rev 0.1(X00)
Date: Thursday, August 06, 2015	Sheet 49 of 71	

BATT LED Power Button



Battery Gauge LED



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/15	Title: LED indicator
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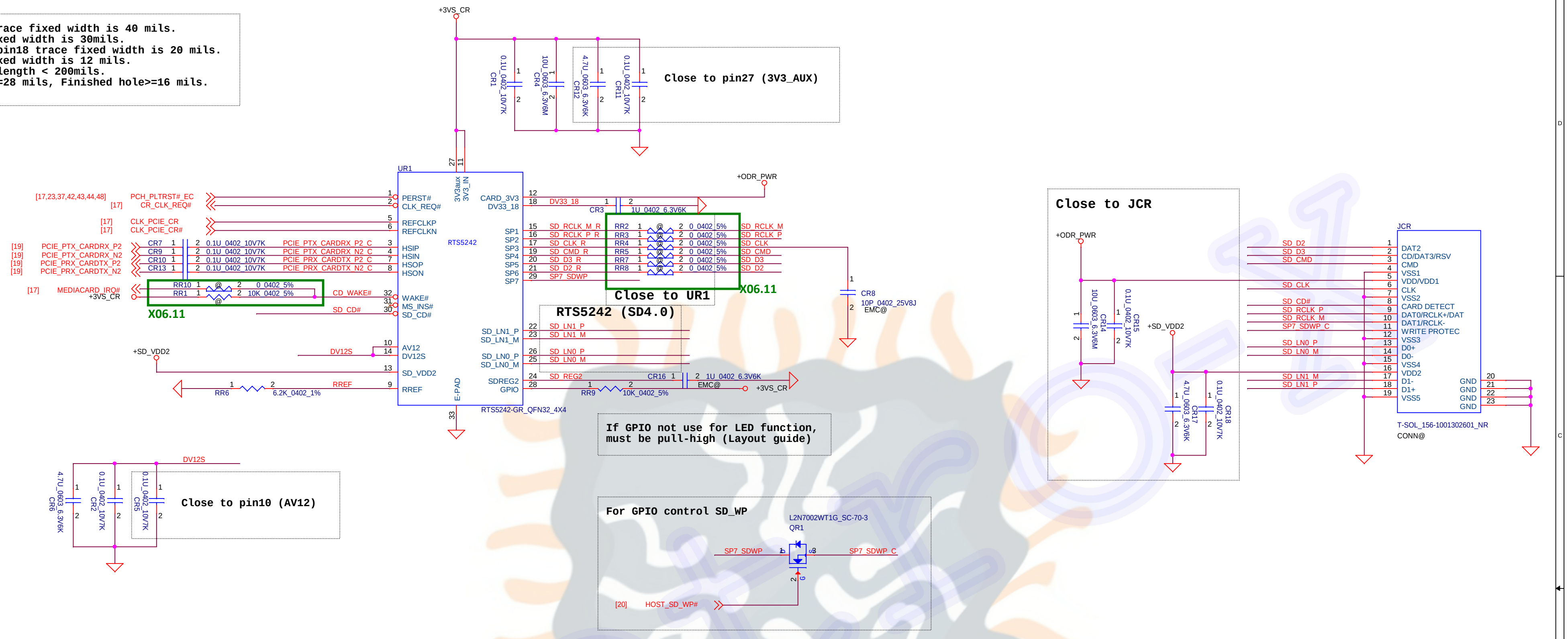
				Date: Thursday, August 06, 2015; Sheet 50 of 71

Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



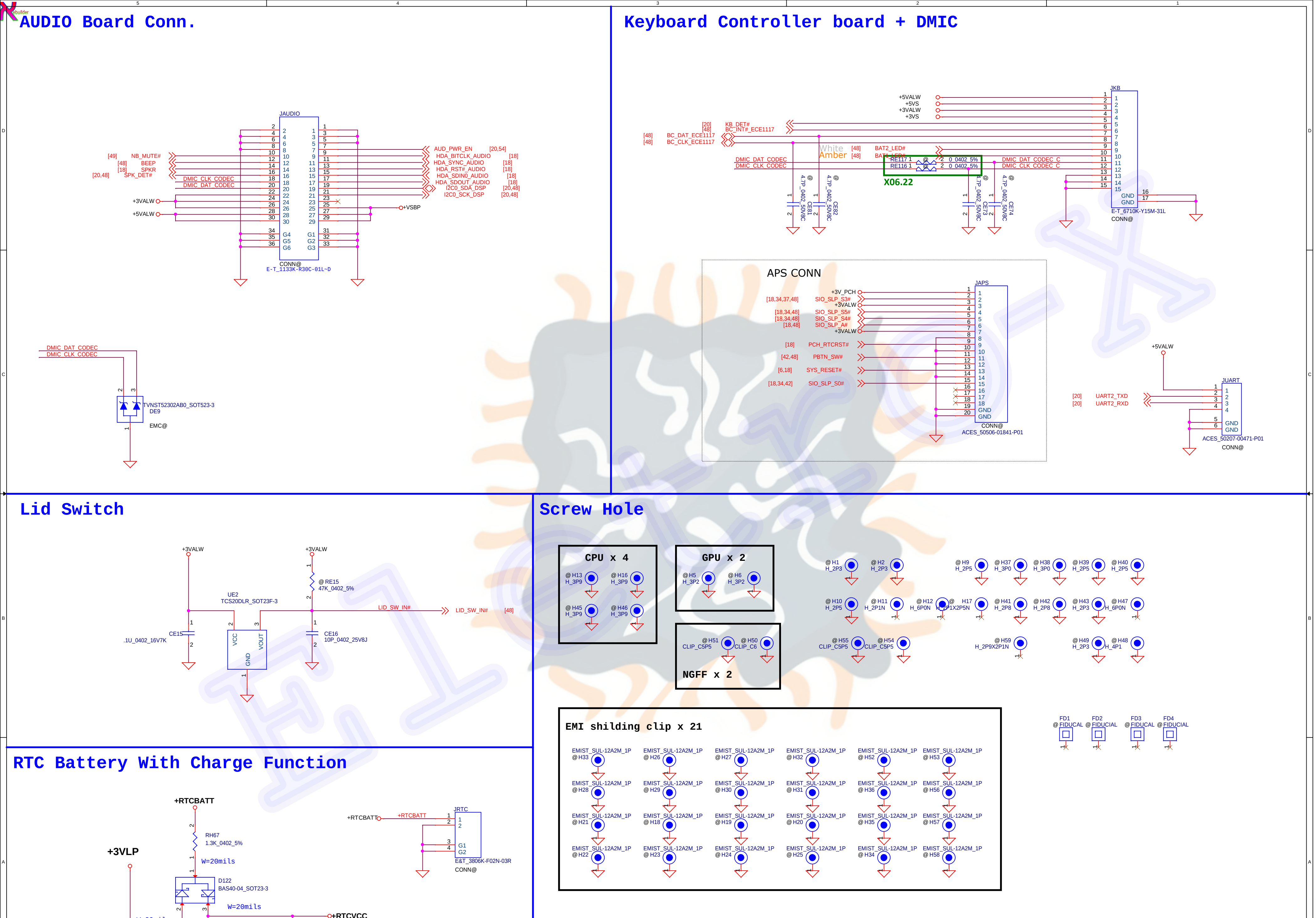
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Card Reader**

Size | Document Number | Rev 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 51 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: **TPM/BTB conn.**

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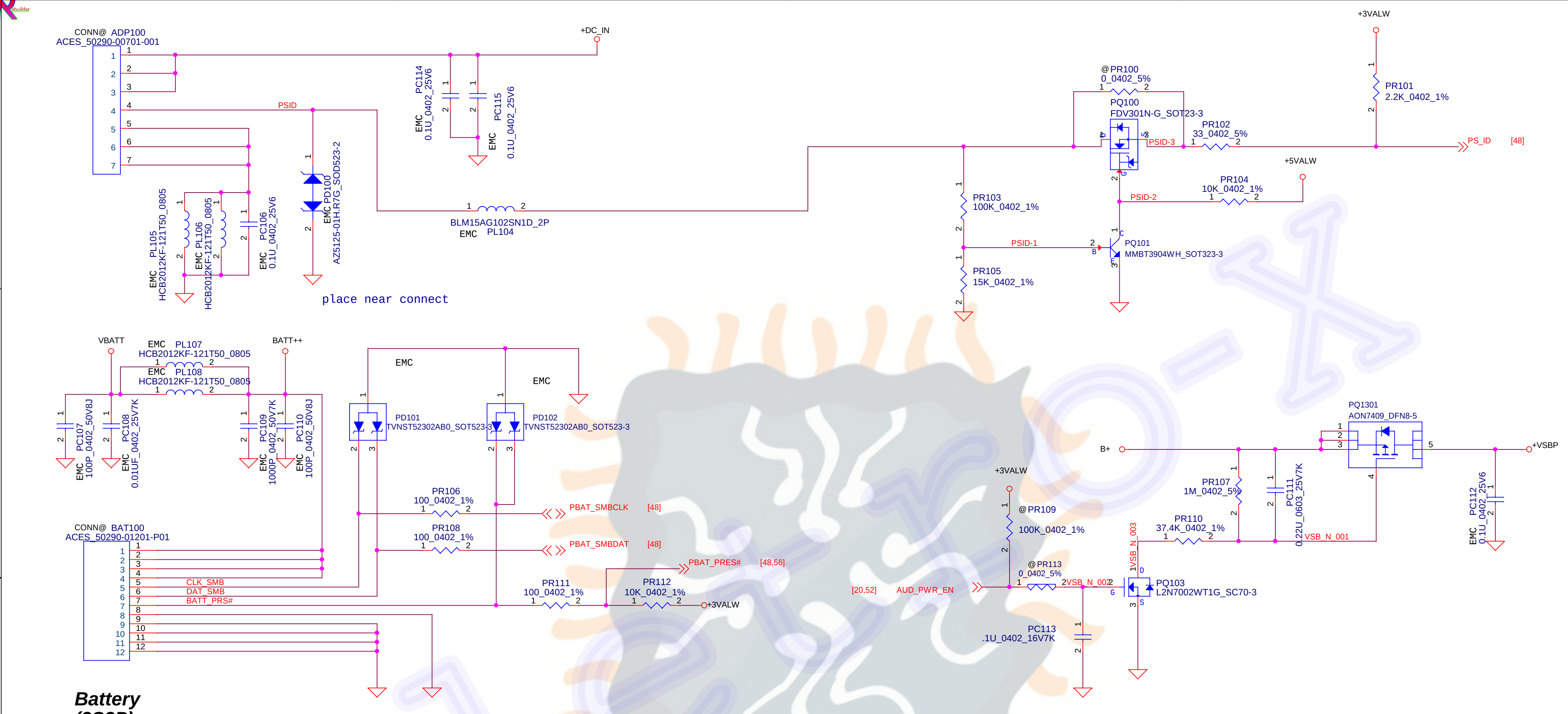
Date: Thursday, August 06, 2015 | Sheet 52 of 71

Eletro-X



Battery (3S3P)

JIMBTY battery connector

SMART Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Smart Adapter circuit (39.1)

	Compal Electronics, Inc.
Title	PWR-DCIN / BATT CONN / OTP
Size / Document Number	LA-C361P
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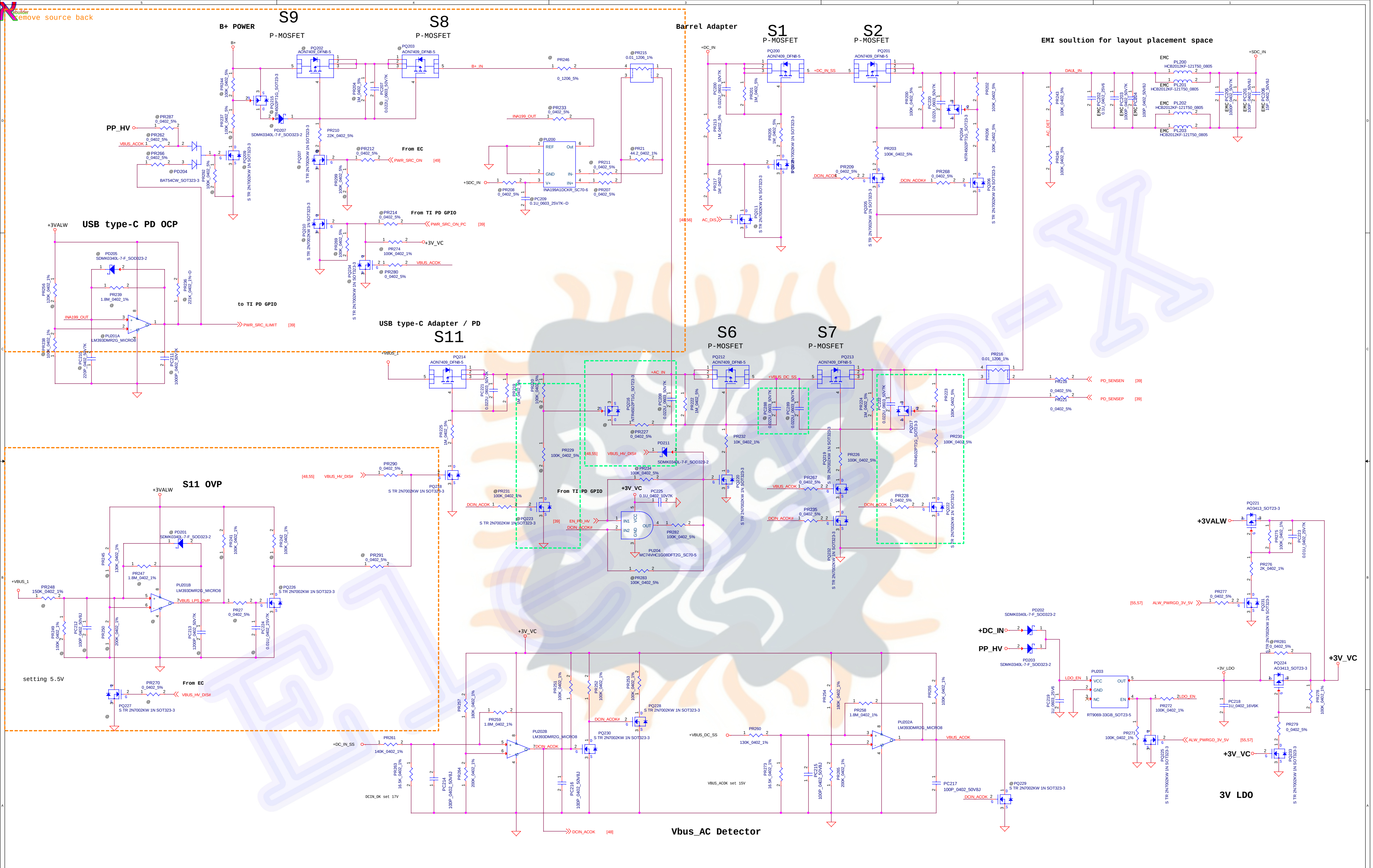


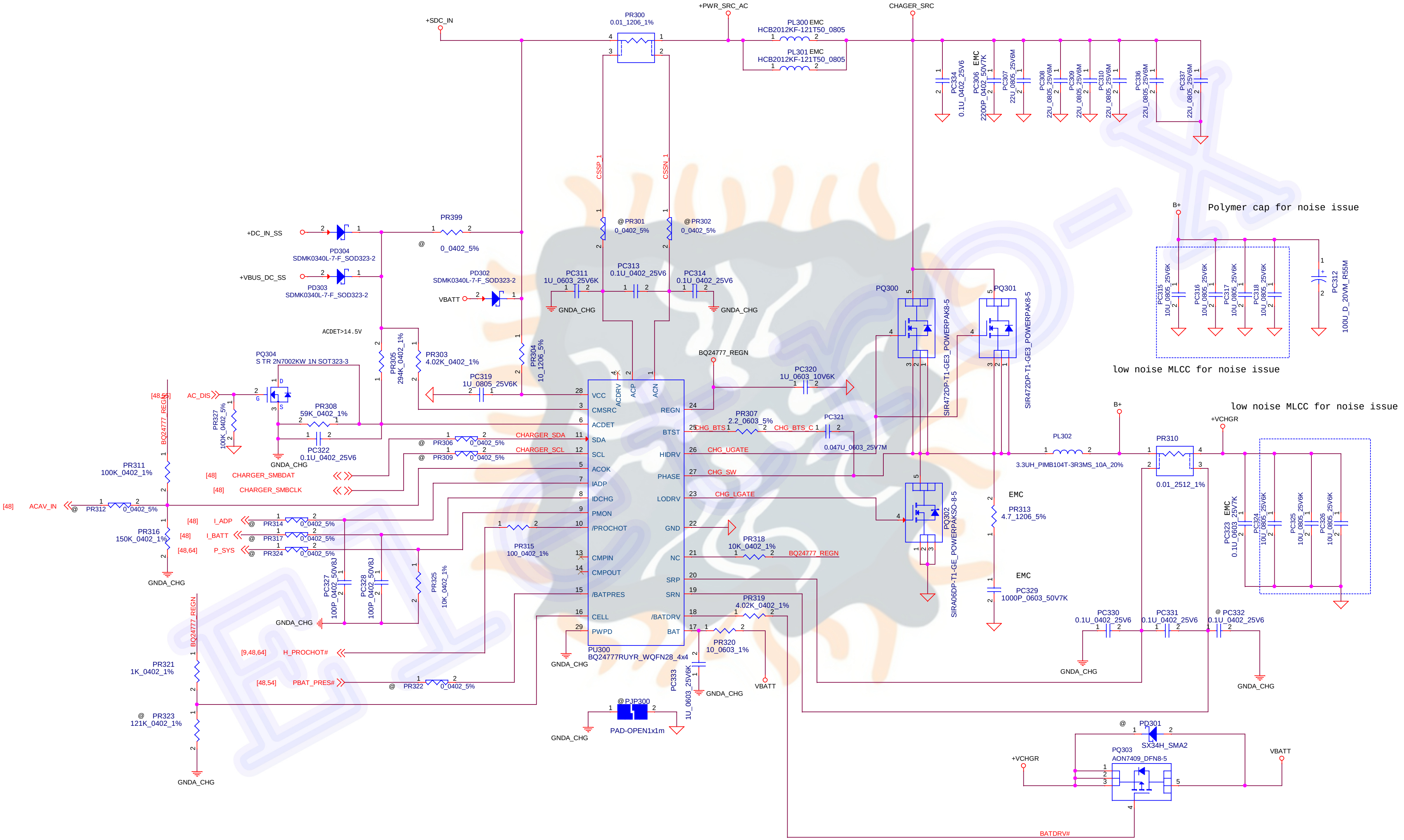
Docking Power Control(41.1), Support component(41.2)

Compal Electronics, Inc.

Title: Docking

Document Number: LA-C361P

Date: Tuesday, August 11, 2015 Sheet 55



Charger controller(40.1), Support component(40.2)

Compal Electronics, Inc.	
Title	Charger
Size / Document Number	LA-C361P
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Date:	Tuesday, August 11, 2015
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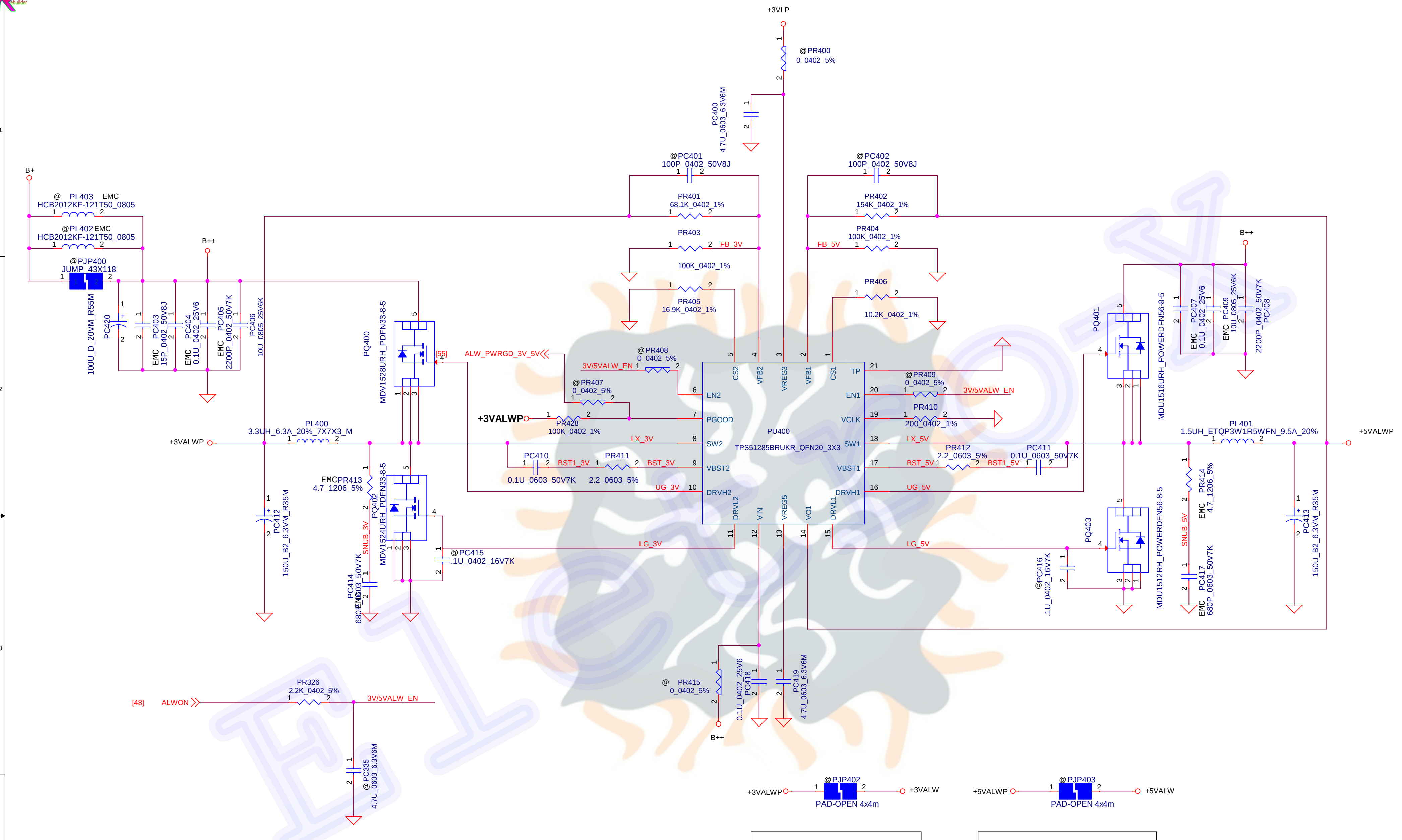


3.3VALWP
TDC 5.7A
Peak Current 8.1A
OCP current 9.7A

5VALWP
TDC 7.4A
Peak Current 10.5A
OCP current 12.6A

3V/5V controller(35.1), Support component(35.2)

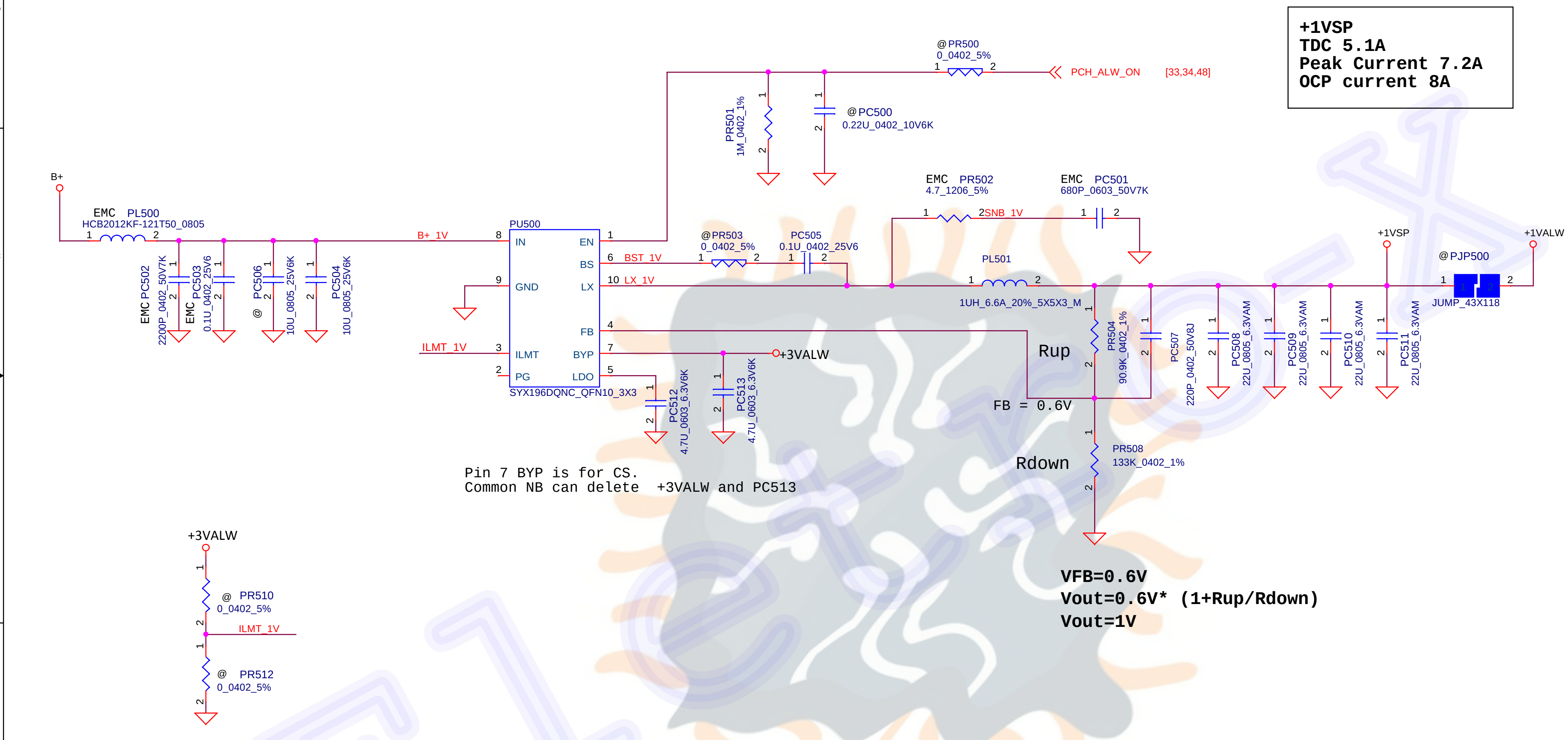
Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Document Number: LA-C361P

Rev: 1.0(A00)

Date: Tuesday, August 11, 2015 Sheet 57 of 71



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

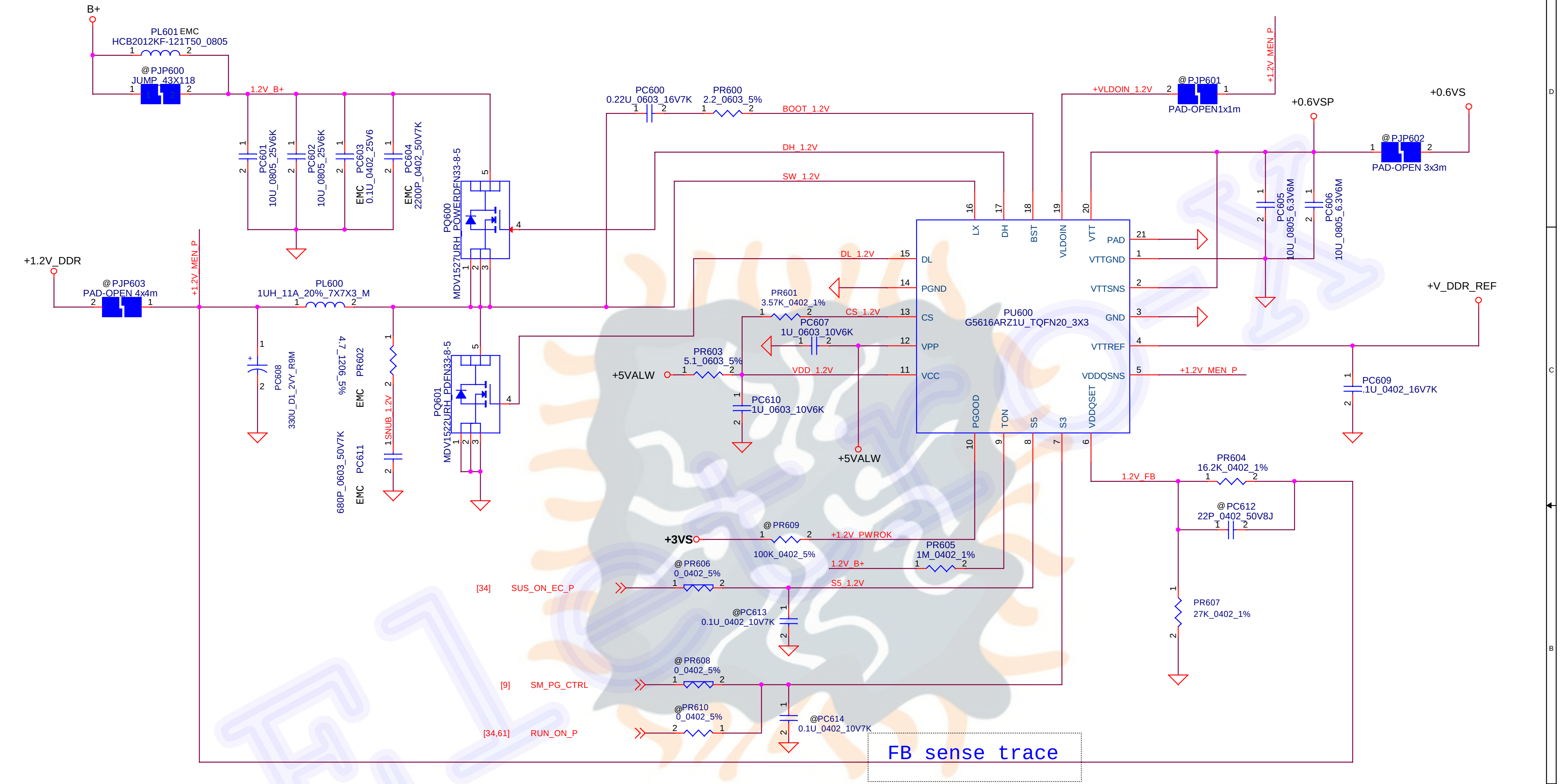
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P40-PWR_+1VA**

Size	Document Number	Rev
	LA-C361P	0.1

Date: Tuesday, August 11, 2015 | Sheet 58 of 71



1.2Volt +/- 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

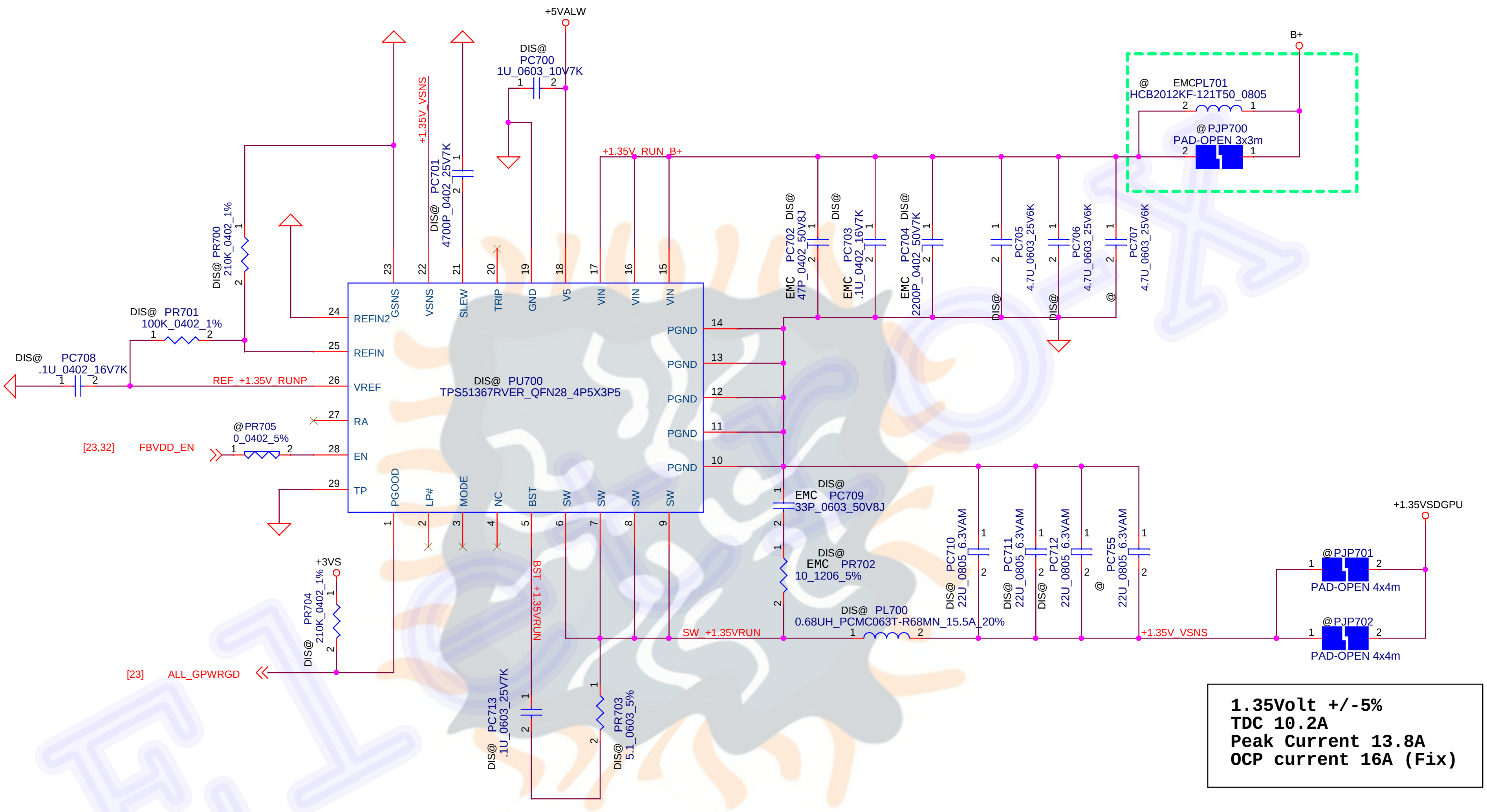
DDR controller(35.3), Support component(35.4)

Compal Electronics, Inc.

Title: +1.35V_MEN/+0.675V_DDR_VTT

Size | Document Number: LA-C361P | Rev 1.0(A00)

Date: Tuesday, August 11, 2015 | Sheet 59 of

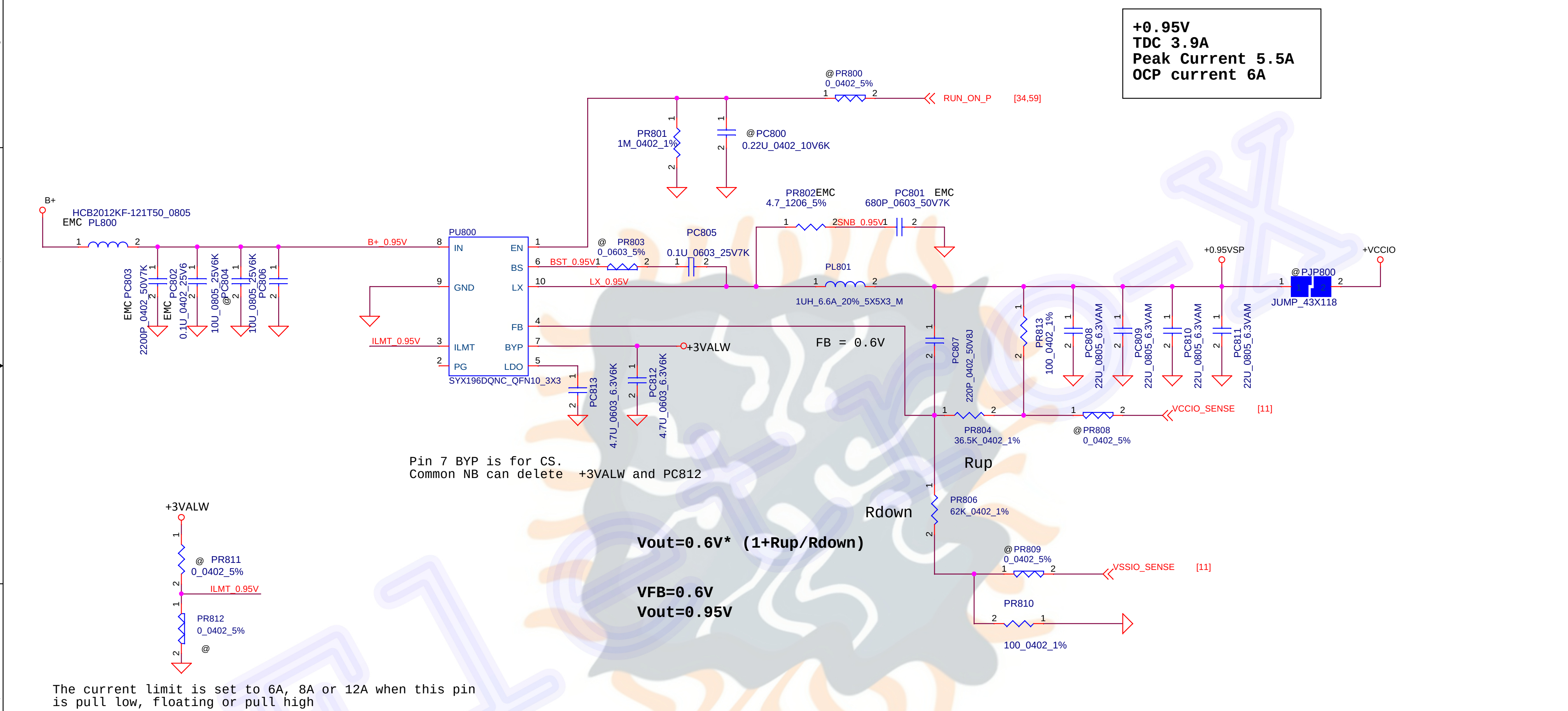


1.35Volt +/-5%
TDC 10.2A
Peak Current 13.8A
OCP current 16A (Fix)

DDR controller(35.3), Support component(35.4)

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PWR_+1.5VDGPU
Size / Document Number	LA-C361P
Rev	1.0(A00)
Date:	Tuesday, August 11, 2015
Sheet	60 of 71

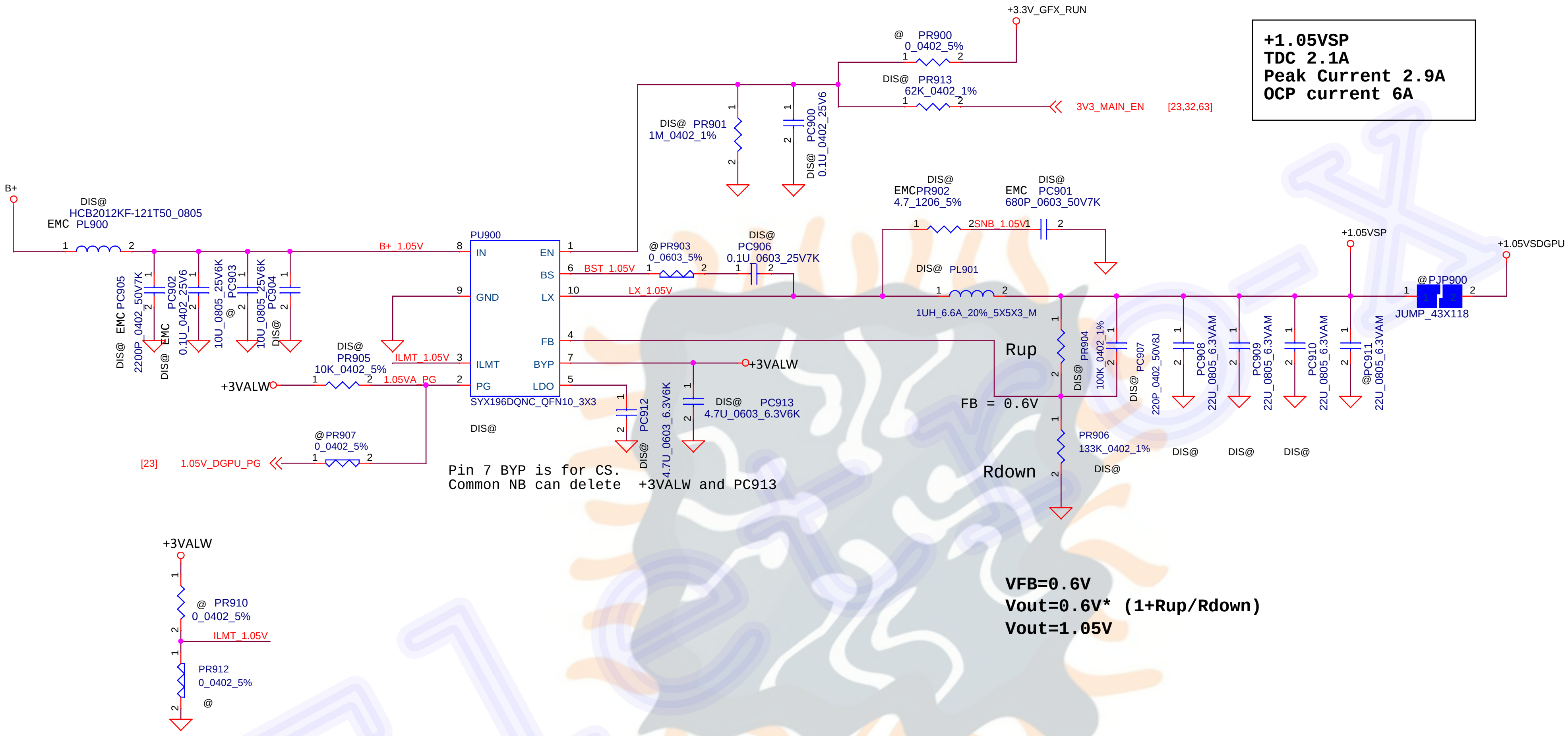


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title: P40-PWR_+0.95VA

Size | Document Number: LA-C361P | Rev 0.1

Date: Tuesday, August 11, 2015 | Sheet 61 of 71

1.05V controller(35.5), Support component(35.6)



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P40-PWR_+1.05VA*

Size	Document Number	Rev
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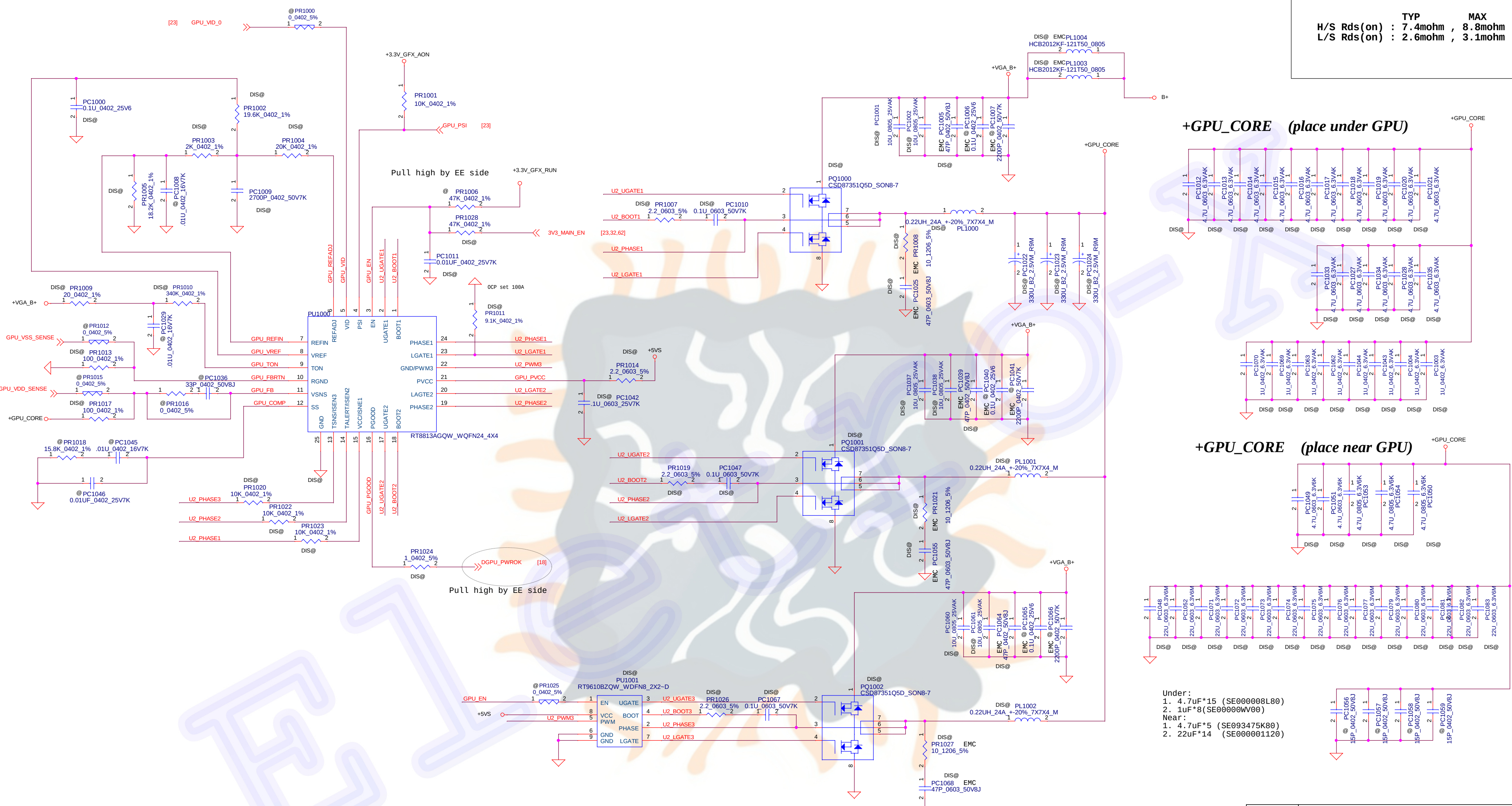
Date: Tuesday, August 11, 2015 Sheet 62 of 71

GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%

	TYP	MAX
H/S Rds(on) :	7.4mohm ,	8.8mohm
L/S Rds(on) :	2.6mohm ,	3.1mohm



Under:
1. 4.7uF*15 (SE000008L80)
2. 1uF*8(SE00000WV00)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*14 (SE000001120)

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.

Title	VGA_CORE	
Size	Document Number: LA-C361P	Rev 1.0(A00)
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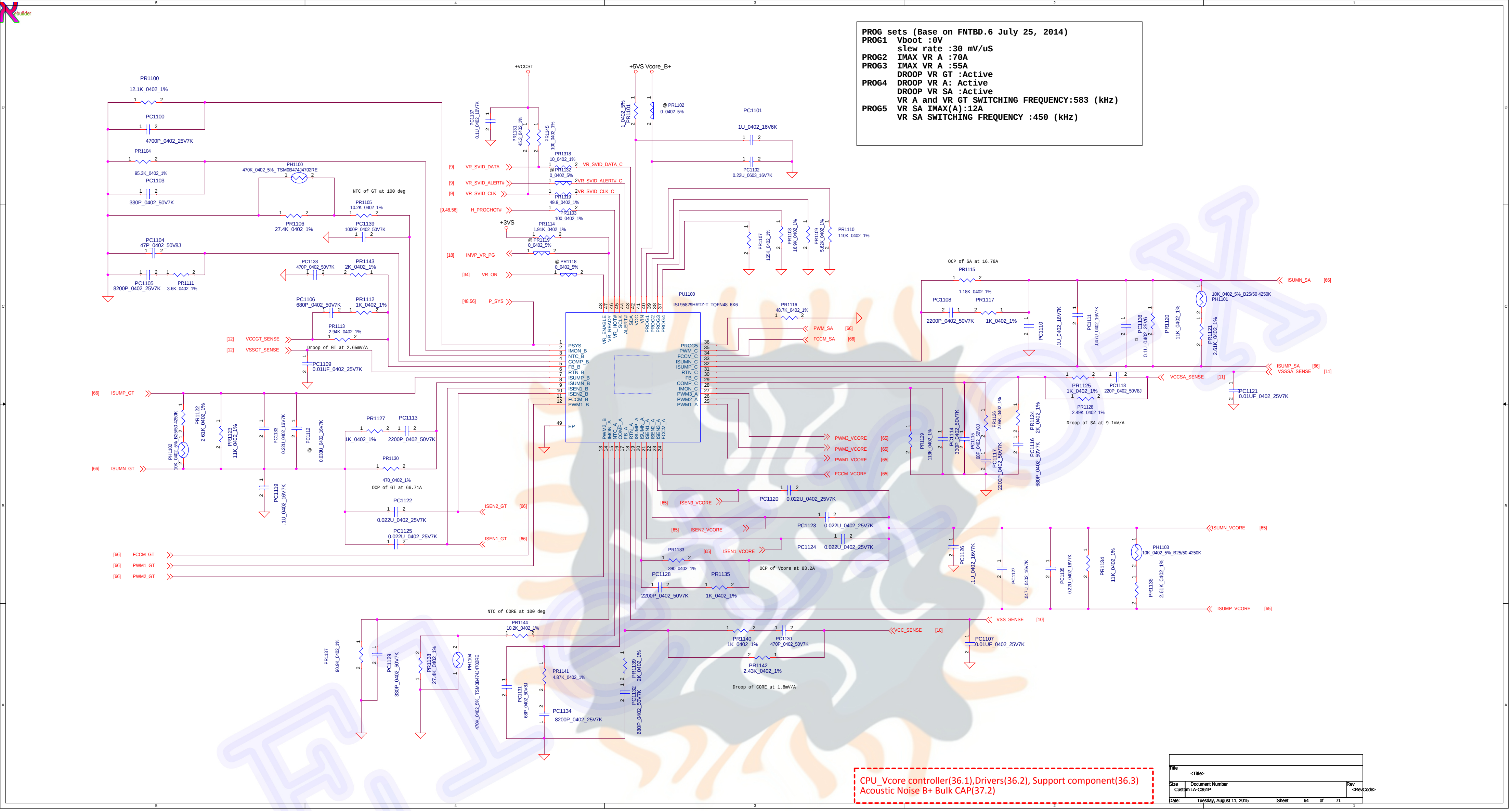

PROG sets (Base on FNTBD.6 July 25, 2014)
PROG1 Vboot :0V
slew rate :30 mV/uS
PROG2 IMAX VR A :70A
PROG3 IMAX VR A :55A
DROOP VR GT :Active
PROG4 DROOP VR A: Active
DROOP VR SA :Active
VR A and VR GT SWITCHING FREQUENCY:583 (kHz)
PROG5 VR SA IMAX(A):12A
VR SA SWITCHING FREQUENCY :450 (kHz)
PU1100
ISL95829HRTZ-T_TQFN48_6X6
NTC of GT at 100 deg
OCP of GT at 66.71A
Droop of GT at 2.65mV/A
OCP of SA at 16.78A
Droop of SA at 9.1mV/A
OCP of Vcore at 83.2A
NTC of CORE at 100 deg
Droop of CORE at 1.8mV/A
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)
<Title>
Document Number
Custom LA-C361P
<RevCode>
Tuesday, August 11, 2015
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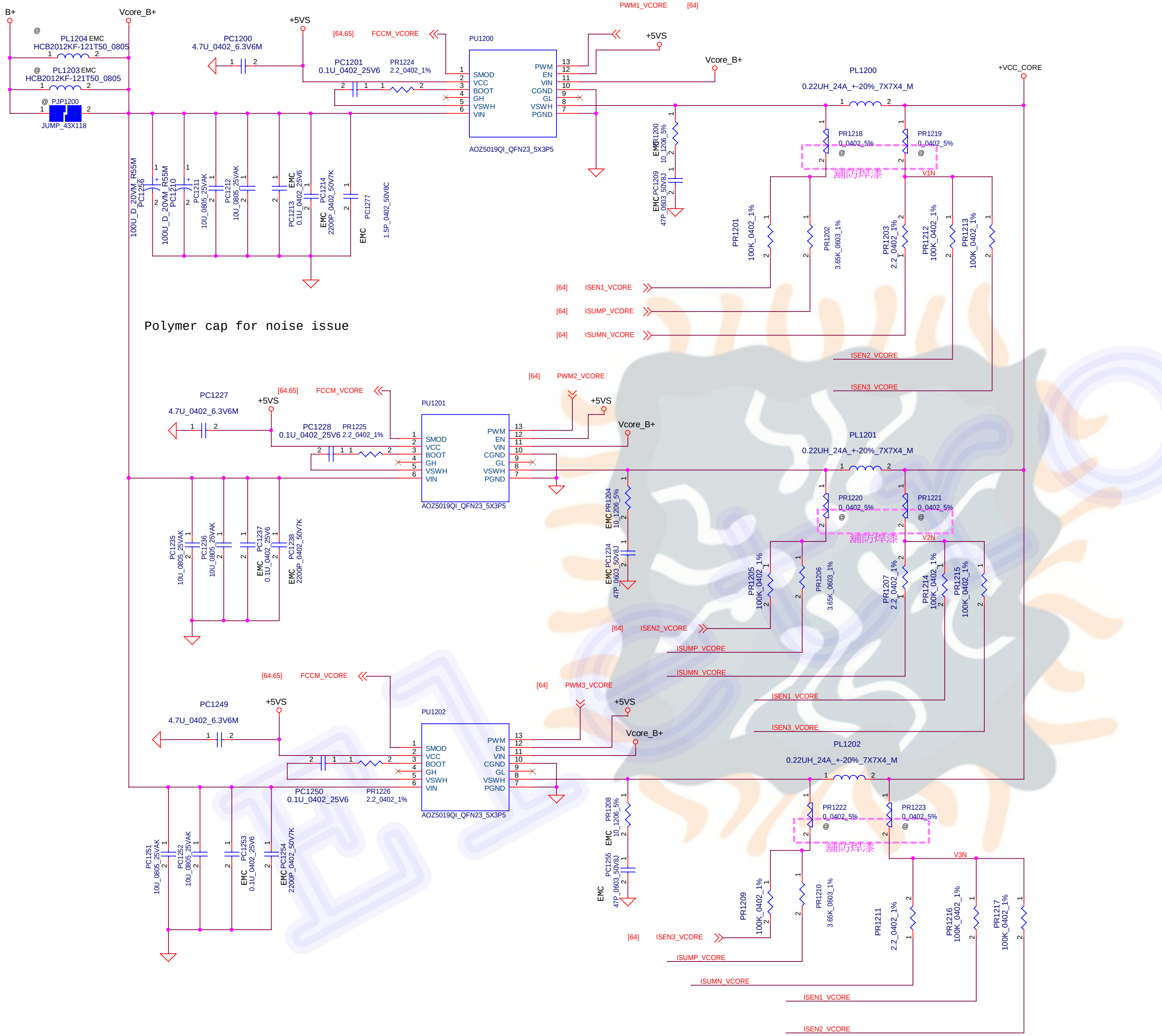
VCC_core (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):56A
Peak Current 68A
DC Load line -1.8mV/A
AC Load line -1.8mV/A
OCP Current 83.2A
DCR 0.97mohm +/-5%

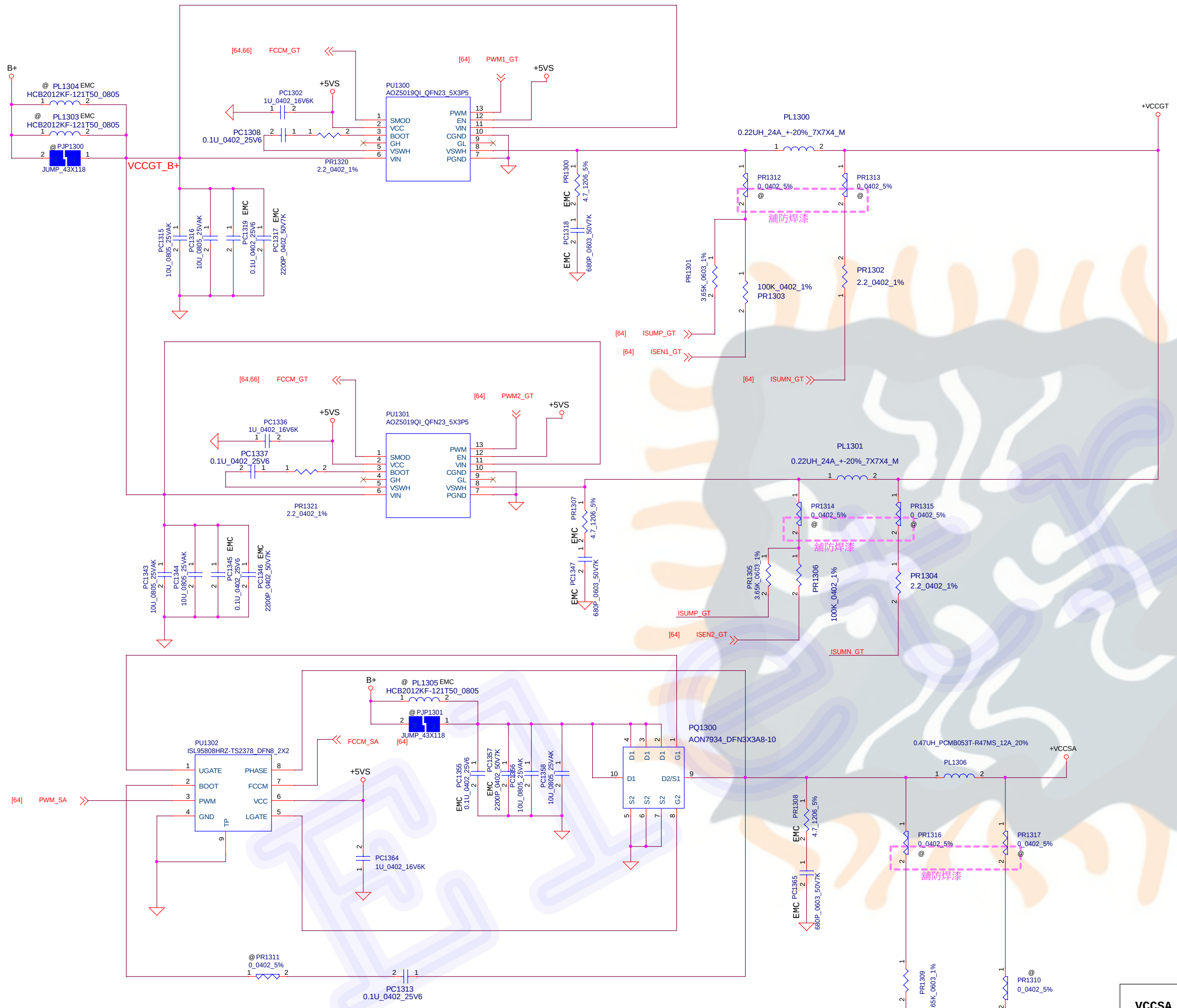


Polymer cap for noise issue

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3),
CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)

Title	<Title>	
Size C	Document Number LA-C361P	Rev <RevCode>
Date: Tuesday, August 11, 2015	Sheet 65 of 71	

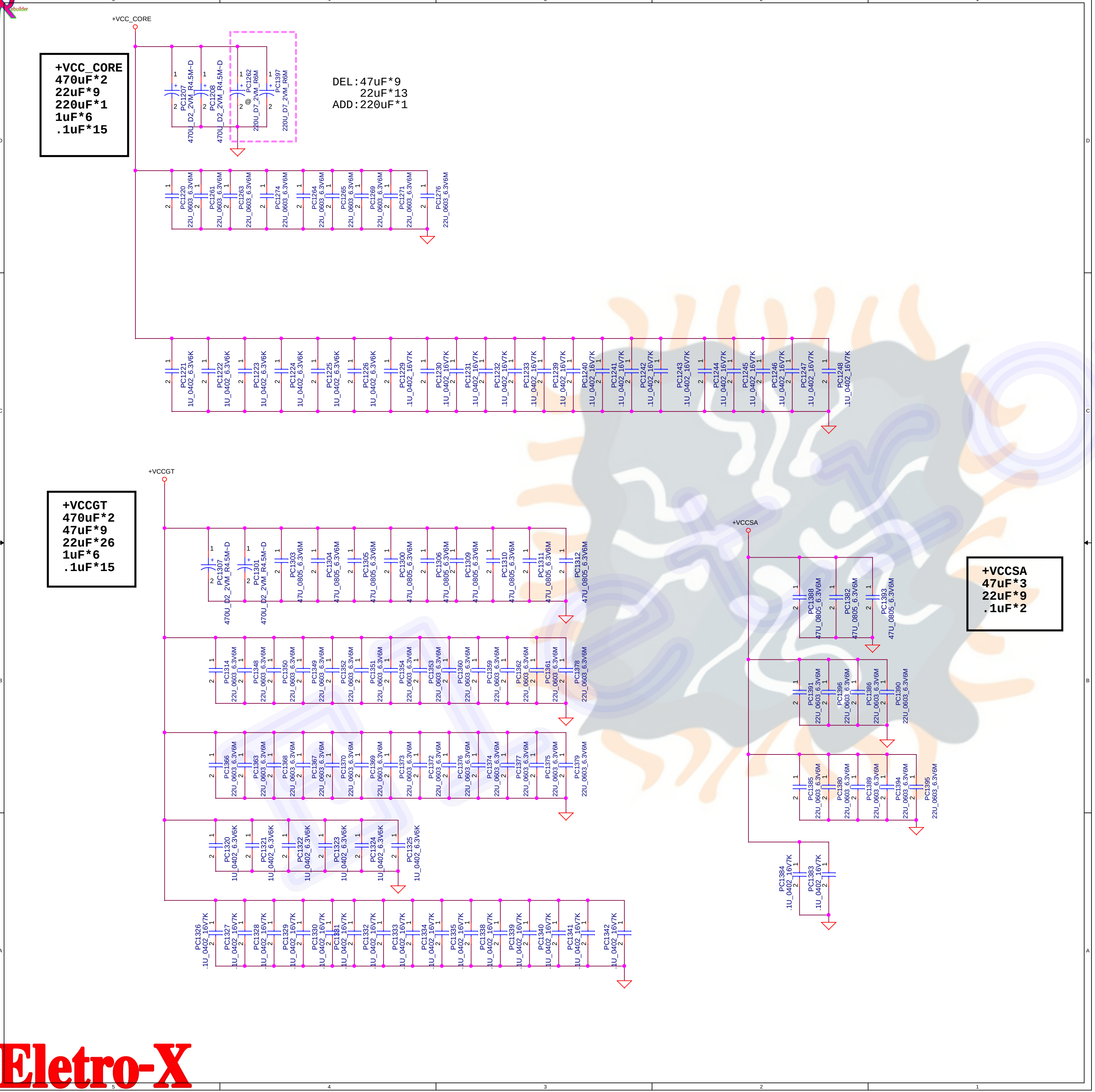
VCCGT (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):39A
Max Current 55A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 66.7A
DCR 0.97mohm +/-5%



VCCSA (Base on PDDG rev 0.7)
PL2 TDC__default):TBD
PL2 TDC_max (40Sec):10A
Max Current 11A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 7.4mohm/8.5mohm +/-5%

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

Title	<Title>	
Size Custom	Document Number LA-C361P	Rev <RevCode>
Date: Tuesday, August 11, 2015	Sheet 66 of 71	


+VCC_CORE
+VCC_CORE
470uF*2
22uF*9
220uF*1
1uF*6
.1uF*15
DEL:47uF*9
22uF*13
ADD:220uF*1
+VCCGT
+VCCGT
470uF*2
47uF*9
22uF*26
1uF*6
.1uF*15
+VCCSA
+VCCSA
47uF*3
22uF*9
.1uF*2

Version Change List (P. I. R. List)

Page 1

Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List) Page 1

Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Eletro-X

Version Change List (P. I. R. List)   Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, de-POP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the same power rail	Change RH571 power rail from +3VS to +3V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIG_SO8 to W25Q128FVSIQ_SO8	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Change RZ58 connection from UZ11.2 to UZ11.4, Change RZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit for useless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH194,CH195. Delete net MPHYP_PWR_EN, move RZ70 to page 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UT5 from W25Q80BLZPIG_WSON8 to W25Q80DVSSIG_SO8,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC3V3_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBT. Add RT198 to PWR_SRC_ILIMIT.Swap UT4.B2/C2 net. Update RT165 from 1206 to 0805, RT167,RT168, RT169.RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT192,RT192,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net UPD_SMBDAT/UPD_SMBCLK"	X01 X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	Update RE67 to 62K	X01
8	18	PM	2014/12/15	EE	modify for support deep sleep function	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	change Power rail for correct design	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	Add pull high resistor for MB side	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Change GPIO for sync common GPIO table	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Pin swap for DFB review	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add pull high resistor by vendor request	Add RPH34 replace to RV520,RV521,RV522 and add net THERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Follow CRB XDP design	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB boardfile	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Change net BID_BC to GPP_C15, Add Net UARTT0_TX from GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Modify Debug UART from closed Chassis to Open Chassis	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Change PU resistor follow Miramar	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Add 2 PAD for ME NUT	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add series resistor follow CRB	Add RE111 43K series SIO_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Change BOM to follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	Add RE112 and Connect net BID_DIS to UE3.A10, swap Net BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/ PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Update BOM for design change	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change JNGFF1 to CONCR_213AAAA32FA	
26	18	PCH	2014/12/17	EE	Change array resistor to resistor for routing	Change RP21 to RH576,RH577,RH578,RH579. Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change net name by EC request	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, USB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USB_DET_EC_R#	
28	18	TS	2014/12/18	EE	Update Touch Screen Connector by ME request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Add Pull down resistor for USB2.0	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Reserve test point for Alpine Ridge	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Delete common mode chok & ESD for vendor feedback	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete I2C signal from EC to Codec.	Delete QE14	
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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/04/10	Deciphered Date	2014/05/01	Title: NOTE
				Size / Document Number: LA-B072P / Rev 1.0
				Date: Thursday, August 06, 2015 / Sheet 70 of 71

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
20				EE			X01
21				EE			X01
22				EE			X01
23				EE			X01
24				EE			X01
25				EE			X01
26				EE			
27				EE			
28				EE			
29				EE			
30				EE			
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32				EE			
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34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/04/10	Deciphered Date	2014/05/01	Title: NOTE
				Size / Document Number: LA-B072P / Rev 1.0
				Date: Thursday, August 06, 2015 / Sheet 71 of 71

MODEL NAME : ***AAM00***

PCB NO : ***LS-C361P***

BOM P/N : ***TBD***

ZZZ R1@

PCB 1BG LS-C361P REV0 AUDIO/B 8

Dell/Compal Confidential

Schematic Document

Berlinetta (SKY-LAKE H)

Audio Board

2014-06-20

Rev: 0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title: P01-Cover Page
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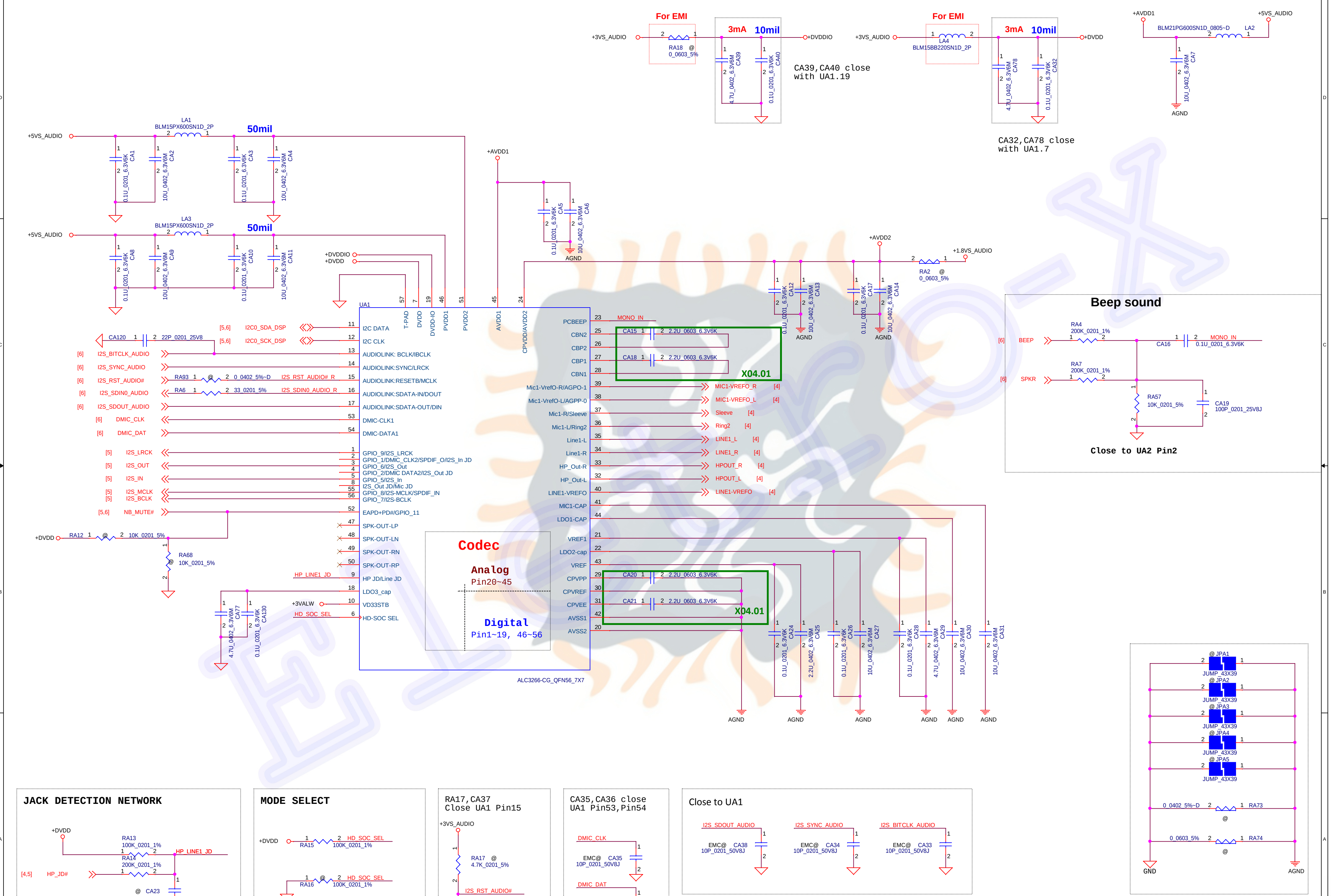
				Date: Saturday, July 18, 2015 / Sheet 1 of 7

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

Compal Electronics, Inc.

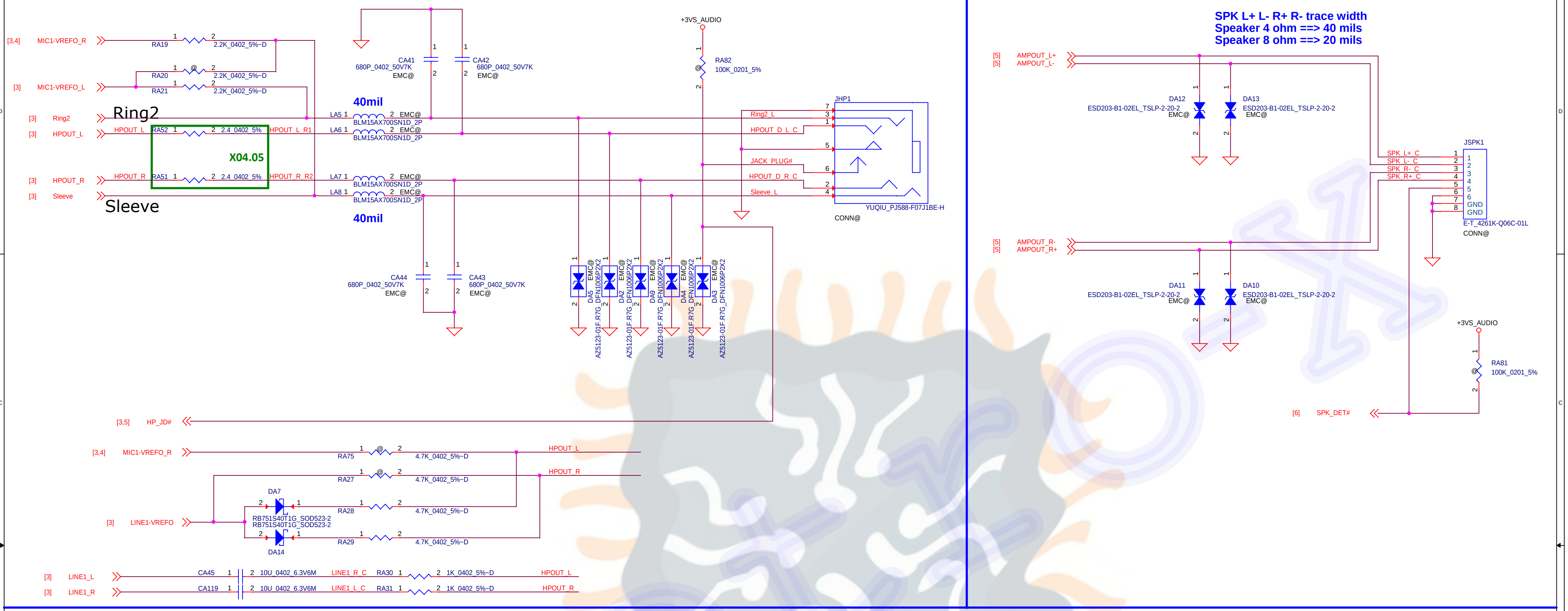
Title: P21-Audio Codec

Size | Document Number: LA-B441P | Rev 0.1

Date: Thursday, July 23, 2015 | Sheet 3 of 7

Universal Audio Jack

Int. Speaker Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/07/04	Deciphered Date	2013/10/28	Title: P22-Audio Conn
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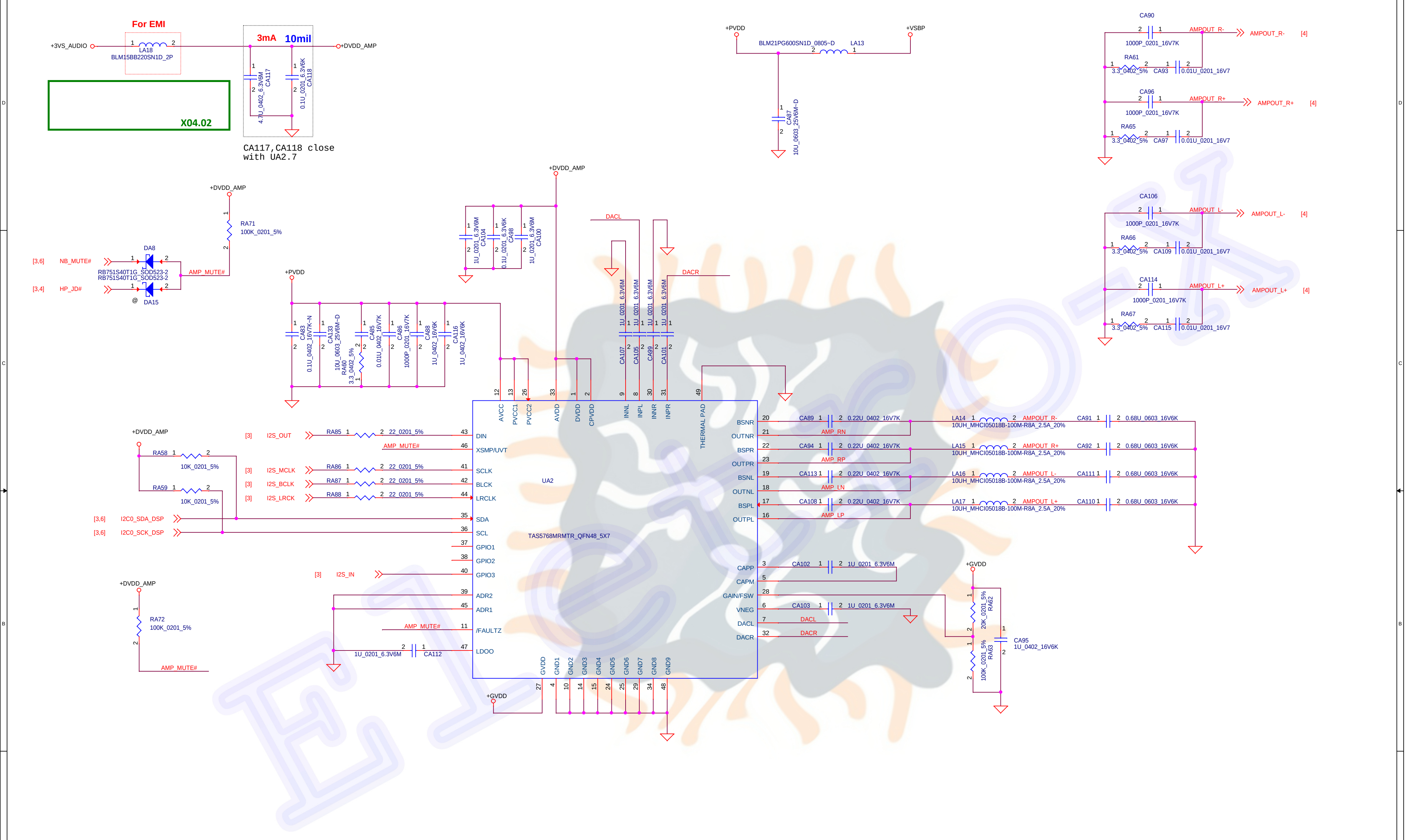
				Date: Thursday, July 23, 2015 / Sheet 4 of 7

SMART AMP



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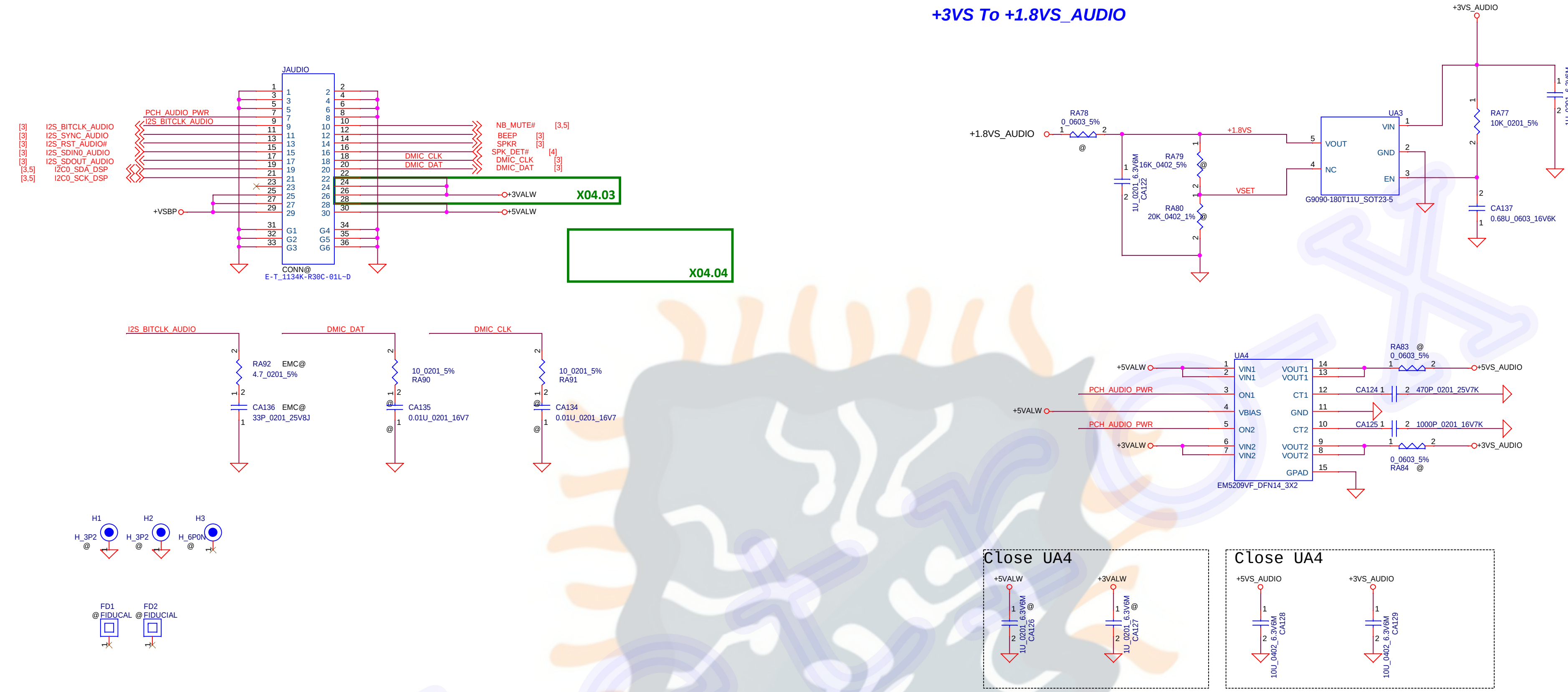
				Date: Thursday, July 23, 2015 / Sheet 5 of 7



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title: P45-PWR_PIR-2
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				Date: Thursday, July 23, 2015 Sheet 6 of 7

Version Change List (P. I. R. List) Page 1

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Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title: P45-PWR_PIR-2
				Size / Document Number: LA-9261P / Rev 0.1
				Date: Saturday, July 18, 2015 / Sheet 7 of 7

MODEL NAME : ***AAM00***

PCB NO : ***LS-C362P***

BOM P/N : ***TBD***

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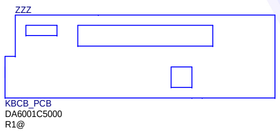
Schematic Document

Berlinetta (Keyboard Controller Board)

2014-08-05

Rev: 0.1



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title: P01-Cover Page
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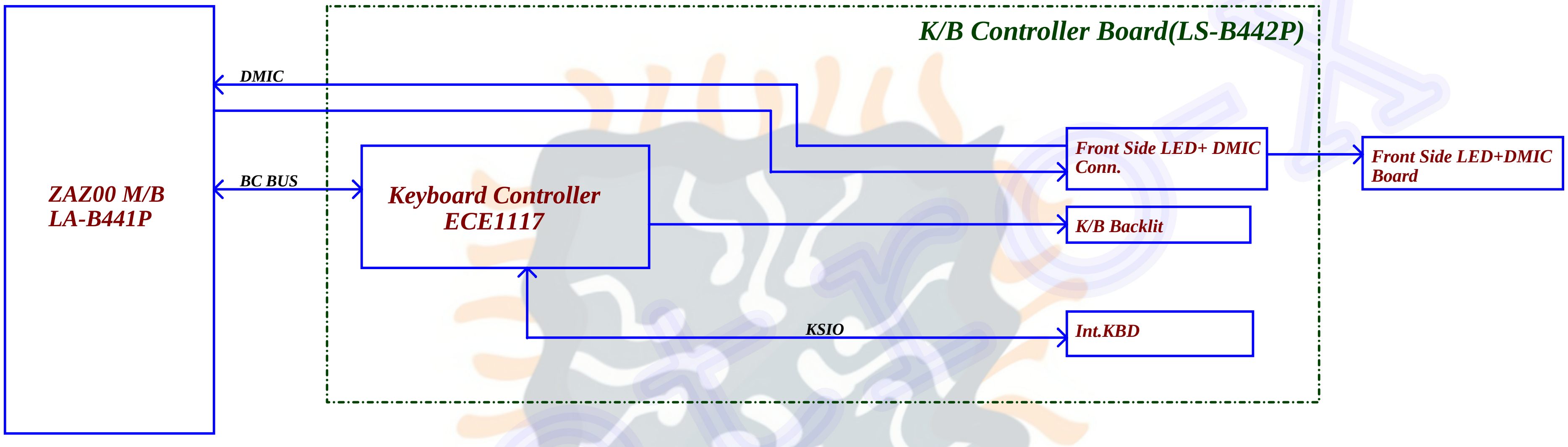
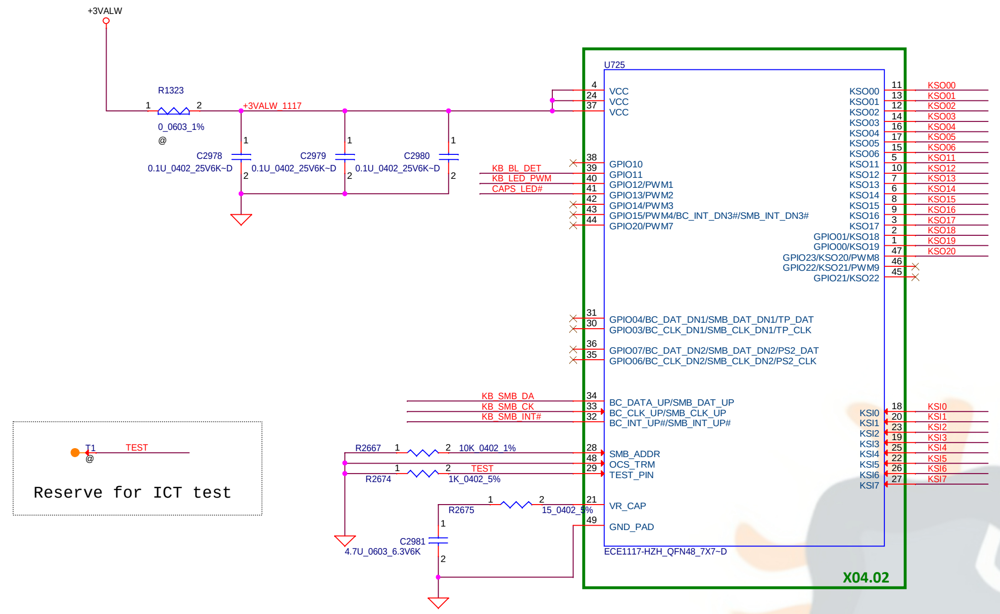
				Date: Saturday, July 18, 2015 / Sheet 1 of 4



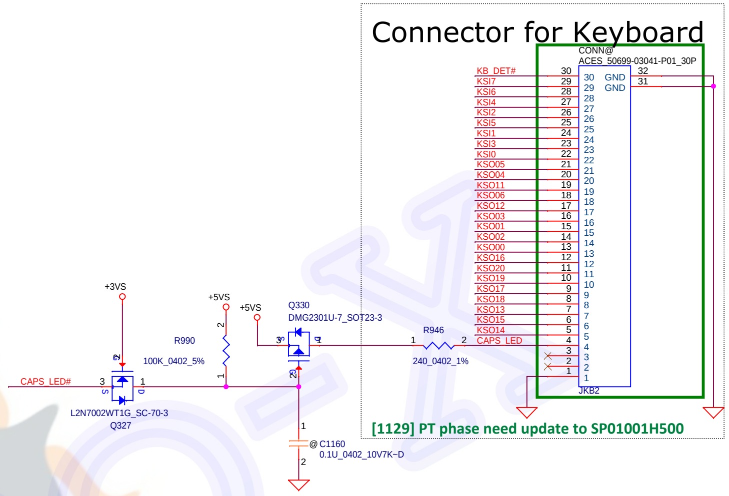
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/02/23	Deciphered Date	2013/10/28	Title: P02-Block Diagram
				Size / Document Number: LS-C362P / Rev 0.1
				Date: Saturday, July 18, 2015 / Sheet 2 of 4



Connector Pin Name	Keyboard Signal	ECE1117 Pin Name
30	Diag_Loop	
29	KSI7	KSI7
28	KSI6	KSI6
27	KSI4	KSI4
26	KSI2	KSI2
25	KSI5	KSI5
24	KSI1	KSI1
23	KSI3	KSI3
22	KSI0	KSI0
21	KSO5	KSO5
20	KSO4	KSO4
19	KSO7	KSO11
18	KSO6	KSO6
17	KSO8	KSO12
16	KSO3	KSO3
15	KSO1	KSO1
14	KSO2	KSO2
13	KSO0	KSO0
12	KSO12	KSO16
11	KSO16	KSO20
10	KSO15	KSO19
9	KSO13	KSO17
8	KSO14	KSO18
7	KSO9	KSO13
6	KSO11	KSO15
5	KSO10	KSO14
4	CAP_LOCK_LED	GPIO13
3	NC	
2	NC	
1	GND	

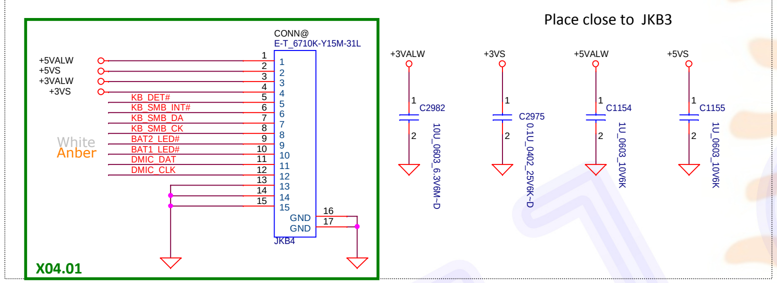
X01_0305: Change JKB2 connector to follow connector list.

Connector for Keyboard



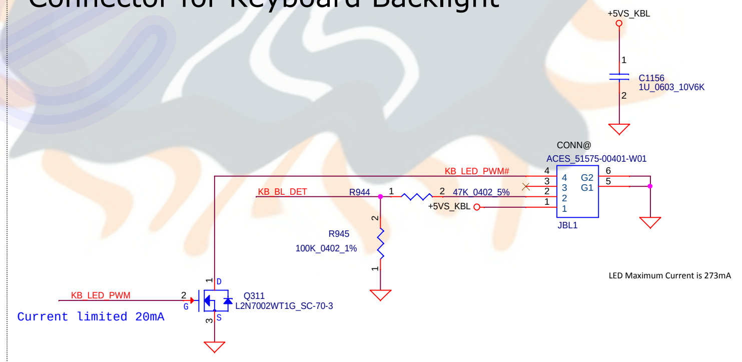
X01_0304: Change JKB3 connector to follow connector list.

Connector for M/B

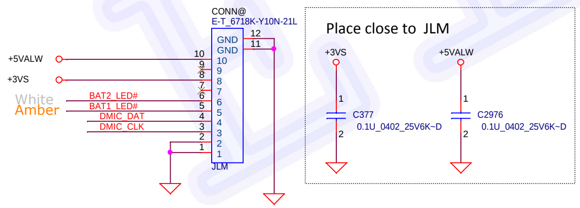


R03_0708: Remove screw hole H1, H2.

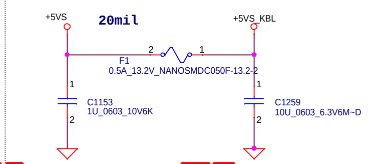
Connector for Keyboard Backlight



Connector for LED+DMIC Board



Fuse for Backlight



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P03-KB Controller*

Size | Document Number: *LS-C362P* | Rev 0.1

Date: Friday, July 24, 2015 | Sheet 3 of 4

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
AAM00	1							
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Security Classification	Compal Secret Data		
Issued Date	2013/07/04	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P04-Change List*

Size | Document Number: *LS-C362P* | Rev 0.1

Date: Saturday, July 18, 2015 | Sheet 4 of 4