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Model Name : D4PB1/D5PB1
File Name : TBD
BOM P/N:43

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D4PB1/D5PB1
M/B Schematics Document

SKL U22/KBL U22 U42 Processor + DDR4

2017-02-22

Rev:1.0

ZZZ
LA-F241P MB REV1
DAA000EV010
DA2@

ZZZ1
LS-D303P FUN/B
DA400299000
DAS@

ZZZ2
LS-D302P USB/B
DA6001HX000
DAS@

ZZZ3
LS-A133P
DA600101010
DAS@

ZZZ4
LS-D301P LID/B
DA400272000
DAS@

ZZZ5
LS-B734P
DA6001B8010
DAS@

ZZZ5
HDMI LOGO
RO0000003HM
HDMI@

ZZZ
LS-B732P
DA4001YF010
DAS@

ZZZ
DAZ PCB
DAZ1IB00100
DAZ@

X4EA99BOL01 includes EMC@, EMI@ and ESD@

ZZZ
SMT EMC EE AF241 D4PB1
X4E@EMC
X4EA99BOL01

UC1
FJ8067702739739 SR342 H0 2.5G
CPU_SR342@
SA0000A37N0

UC1
S IC FJ8067702739740 SR341 H0 2.7G ABO
CPU_SR341@
SA0000A34L0

UC1
S IC FJ8067703281813 QN5C Y0 1.8G
CPU_QN5C@
SA0000AQZ10

UC1
S IC FJ8067702739738 SR343 H0 2.4G ABO!
CPU_SR343@
SA0000A38M0

KBL-R U42

UC1
S IC FJ8067703281813 QN5C Y0 1.8G
CPU_QN5C@
SA0000AQZ10

UC1
S IC FJ8067702739738 SR2ZW H0 2.4G ABO!
CPU_3860@
SA0000A3860

UC1
S IC FJ8067702739738 QLDP H0 2.4G BGA
CPU_3820@
SA0000A3820

UC1
S IC FJ8067702739739 SR2ZU H0 2.5G ABO!
CPU_3760@
SA0000A3760

UC1
S IC FJ8067702739739 QLDM H0 2.5G BGA
CPU_3720@
SA0000A3720

UC1
S IC FJ8066201924931 SR2F0 D1 2.4G ABO!
CPU_2T80@
SA000092T80

UC1
S IC FJ8067702739741 QLDU H0 2.6G BGA
CPU_3L20@
SA0000A3L20

UC1
S IC FJ8067702739740 SR2ZV H0 2.7G ABO!
CPU_3450@
SA0000A3450

UC1
S IC FJ8067702739633 QLYG H0 2.6G BGA
CPU_DO10@
SA0000ADO10

UC1
S IC FJ8067702739628 QLYF H0 2.8G BGA
CPU_DP10@
SA0000ADP10

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Title: *Cover Page*

Size: Custom | Document Number: *LA-F241P* | Rev: 0.1

Date: Wednesday, June 14, 2017 | Sheet 1 of 54

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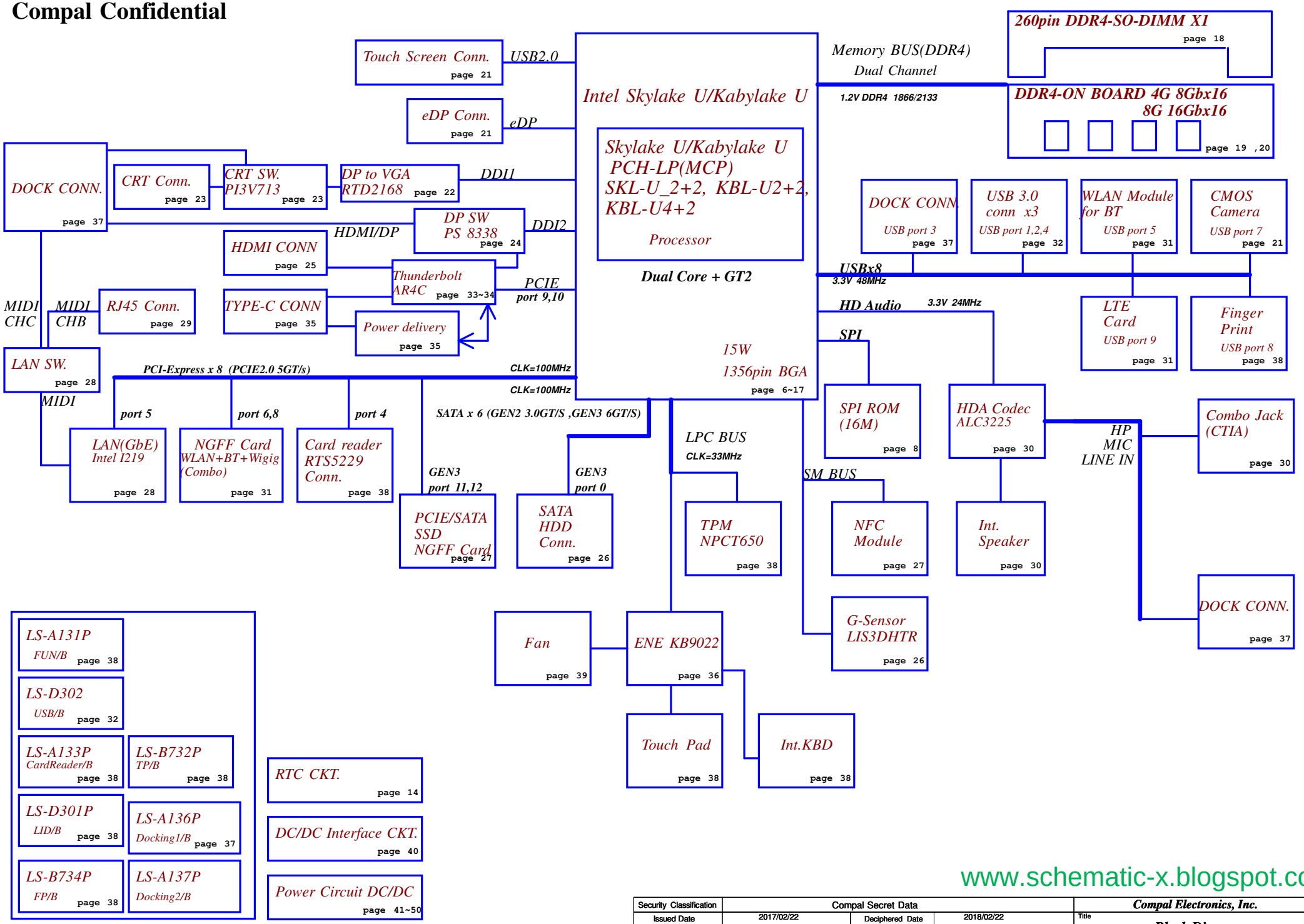

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Title: Block Diagrams			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 2 of 54		

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	Res	Vbrd	PCB version	Project	Note
EVT	0K	0v	0.1	New P6	
PVT	12k	0.345V	0.2		
PreMP	15k	0.430V	1		

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	dGPU	VGA@
Connector	CONN@	ON Board DDR4	X76OBRAM@
EMC requirement	EMC@	N16S-GT	SGT@
EMC requirement unpop	@EMC@	Without WiGi Funct i on	NOWG@
EMI requirement	@EMI@/EMI@	HDD Redriver	X76TI@/X76PAR@
Thunderbolt Funct i on	TBT@	N16V-GM	VGM@
RF requirement	@RF@/RF@	VRAM BOM Select	X76@
LTE Funct i on	3G@	Single/Dual Rank	SR@/DR@ (DR@ is not been used in this project)
UMA only	UMA@		
VPRO Funct i on	VPRO@/NOVPRO@		
VGA EMI Requirement	@VGA_EMI@/VGA_EMI@	PD Funct i on	PD@
VGA UNPOP	@VGA@	CPU Code	QH7Y@
VGA RF Requirement	@RF@_VGA@	ESD requirement	ESD@
VGA Power	22@/23E@	Touch screen reserve	TS@
GC6 Funct i on	GC6@/NOGC6@/NGC6	KBL-R U42	U42@
INTEL CMC	CMC@	KBL U22	U22@
ESPI	ESPI @		

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON	OFF	OFF
+2.5V	DDR4 +2.5V Power Rail	ON	ON	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

I2C Address Table

BUS	Device	8Bit Read/Write
SOC_SMBCLK_1 +3VS	JDIMM1	A4/A5
SOC_SMBCLK_1 +3VS	Gsensor U26	30/31
SOC_SML0CLK +3VS	JNFC1	52/53
SOC_SML0CLK +3V_LAN	LAN UL1	C8/C9
SOC_SML1CLK_1 +3VSDGPU_MAIN	UGPU1	9E/9F
SOC_SML1CLK_1 +3VS	Thermal Sensor UU24	98/99
SOC_SML1CLK_1 +3VS	PCH_LP	90/91
EC_SMB_CK1 +3VLP_EC	PD U5007	70/71
EC_SMB_CK1 +3VLP_EC	Battery PJP201	16/17
EC_SMB_CK1 +3VLP_EC	Charger PU301	12/13

43 level BOM table

43 Level	Description	BOM Structure
431A0NBOL01	SMT MB AD301 B4DBG QJFC 2.3G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL02	SMT MB AD301 B4DBG QJ8M 2.4G UMA HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/HDMI@/NOVPRO@/PD@/TBT@/UMA@/X76PAR@/X76SAM@/RF@
431A0NBOL03	SMT MB AD301 B4DBG QJKP 2.3G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@
431A0NBOL04	SMT MB AD301 B4DBG QJKK 2.5G DIS HDMI	3G@/CMC@/DA2@/SR@/EMC@/EMI@/ESD@/GC6@/HDMI@/PD@/SGT@/TBT@/VGA@/VGA_EMI@/VPRO@/X76PAR@/X76SAM@/RF@

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Title: Notes List

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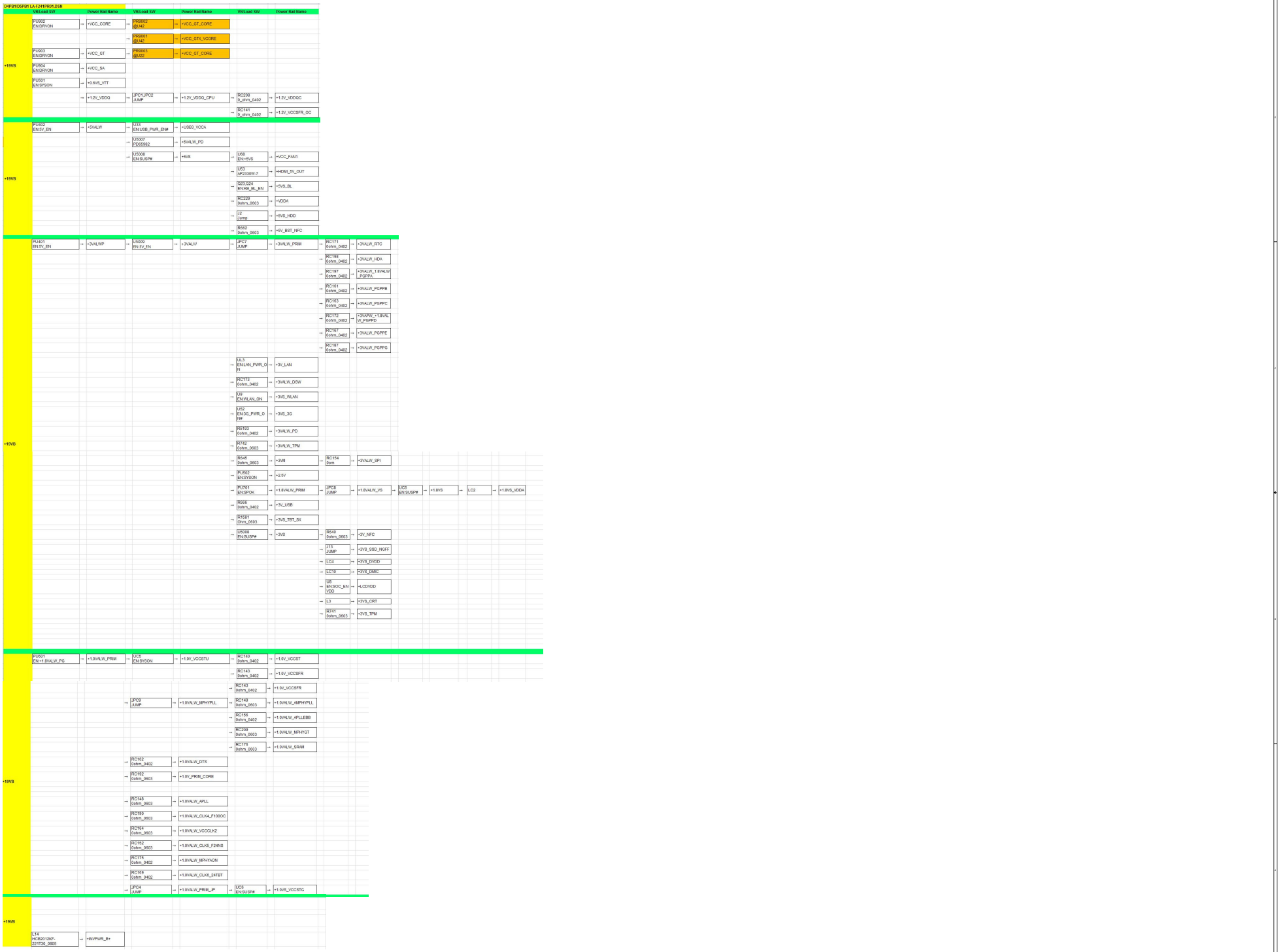
04PB10SP01 LA-F241P/R01.DSN
VR/Load SW
Power Rail Name
VR/Load SW
Power Rail Name
VR/Load SW
Power Rail Name
PU902 EN:DRVON
+VCC_CORE
PR9002 @U42
+VCC_GT_CORE
PR9001 @U42
+VCC_GTX_VCORE
PU903 EN:DRVON
+VCC_GT
PR9003 @U22
+VCC_GT_CORE
+19VB
PU904 EN:DRVON
+VCC_SA
PU931 EN:SYSON
+0.6VS_VTT
+1.2V_VDDQ
JPC1_JPC2 JUMP
+1.2V_VDDQ_CPU
RC208 0_ohm_0402
+1.2V_VDDQC
RC141 0_ohm_0402
+1.2V_VCCSFR_DC
PU402 EN:5V_EN
+5VALW
U33 EN:USB_PWR_EN#
+USB3_VCCA
U5007 PD65982
+5VALW_PD
U5008 EN:SUSP#
+5VS
U68 EN:+5VS
+VCC_FAN1
U83 4P2330W-7
+HDMI_5V_OUT
+19VB
Q23,Q24 EN:KB_BL_EN
+5VS_BL
RC229 0ohm_0603
+VDDA
J2 Jump
+5VS_HDD
RS52 0ohm_0603
+5V_BST_NFC
PU401 EN:5V_EN
+3VALWP
U5009 EN:3V_EN
+3VALW
JPC7 JUMP
+3VALW_PRIM
RC171 0ohm_0402
+3VALW_RTC
RC198 0ohm_0402
+3VALW_HDA
RC197 0ohm_0402
+3VALW_1.8VALW_PGPPA
RC161 0ohm_0402
+3VALW_PGPPB
RC163 0ohm_0402
+3VALW_PGPPC
RC172 0ohm_0402
+3VAPW_+1.8VALW_PGPPD
RC167 0ohm_0402
+3VALW_PGPPE
RC187 0ohm_0402
+3VALW_PGPPG
UL3 EN:LAN_PWR_ON
+3V_LAN
RC173 0ohm_0402
+3VALW_DSW
U9 EN:WLAN_ON
+3VS_WLAN
U52 EN:3G_PWR_ON#
+3VS_3G
RS193 0ohm_0402
+3VALW_PD
+19VB
R742 0ohm_0603
+3VALW_TPM
R645 0ohm_0603
+3VM
RC154 0om
+3VALW_SPI
PU926 EN:SYSON
+2.5V
PU701 EN:SPOK
+1.8VALW_PRIM
JPC8 JUMP
+1.8VALW_VS
UC5 EN:SUSP#
+1.8VS
LC2
+1.8VS_VDDA
RS56 0ohm_0402
+3V_USB
R1581 0hm_0603
+3VS_TBT_SX
U5006 EN:SUSP#
+3VS
R640 0ohm_0603
+3V_NFC
J13 JUMP
+3VS_SSD_NGFF
LC4
+3VS_DVDD
LC10
+3VS_DMIC
U8 EN:SOC_EN VDD
+LCDVDD
L3
+3VS_CRT
R741 0ohm_0603
+3VS_TPM
PU501 EN:+1.8VALW_PG
+1.0VALW_PRIM
UC5 EN:SYSON
+1.0V_VCCSTU
RC140 0ohm_0402
+1.0V_VCCST
RC143 0ohm_0402
+1.0V_VCCSFR
RC143 0ohm_0402
+1.0V_VCCSFR
JPC9 JUMP
+1.0VALW_MPHYPLL
RC149 0ohm_0603
+1.0VALW_AMPHYPLL
RC156 0ohm_0402
+1.0VALW_APLLEBB
RC209 0ohm_0603
+1.0VALW_MPHYGT
RC176 0ohm_0603
+1.0VALW_SRAM
RC162 0ohm_0402
+1.0VALW_DTS
RC192 0ohm_0603
+1.0V_PRIM_CORE
+19VB
RC148 0ohm_0603
+1.0VALW_APLL
RC190 0ohm_0603
+1.0VALW_CLK4_F100OC
RC164 0ohm_0603
+1.0VALW_VCCCLK2
RC152 0ohm_0603
+1.0VALW_CLK5_F24NS
RC175 0ohm_0402
+1.0VALW_MPHYAON
RC169 0ohm_0402
+1.0VALW_CLK6_24TBT
JPC4 JUMP
+1.0VALW_PRIM_IP
UC6 EN:SUSP#
+1.0VS_VCCSTG
+19VB
LT4 HC82012KF-22-T30_0805
+BWPWR_B+
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2011/02/22
Deciphered Date
2016/02/22
Compal Electronics, Inc.
Power Map
LA-F241P
Rev
1.0
Date: Sunday, May 15, 2022
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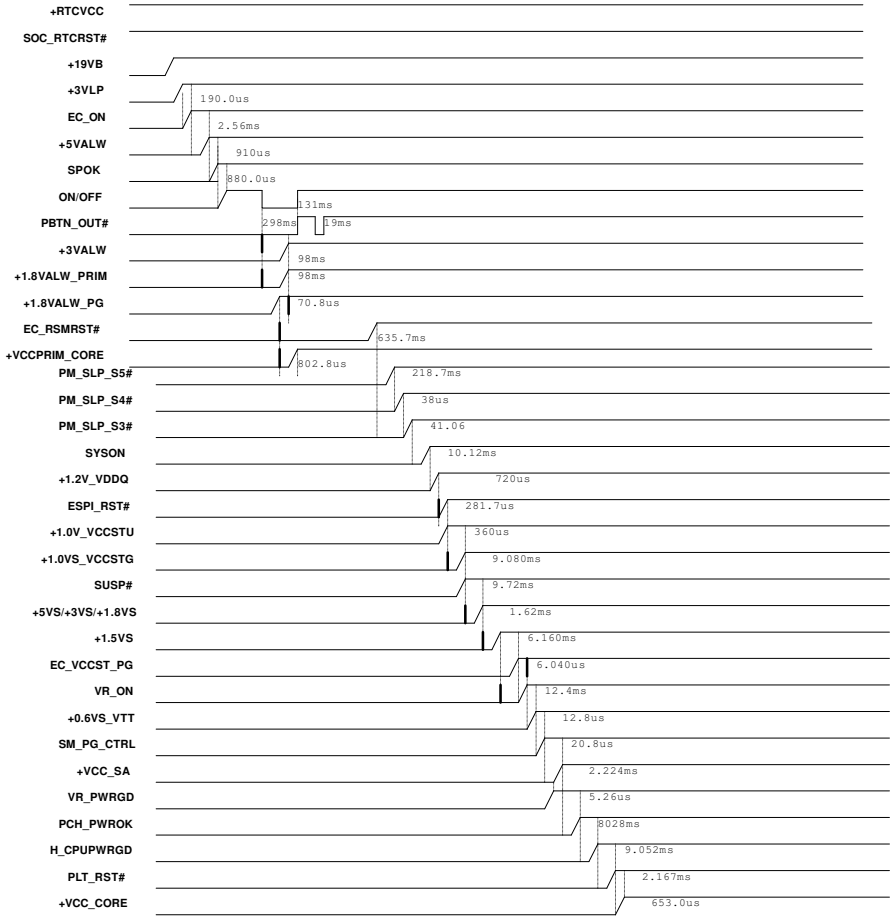
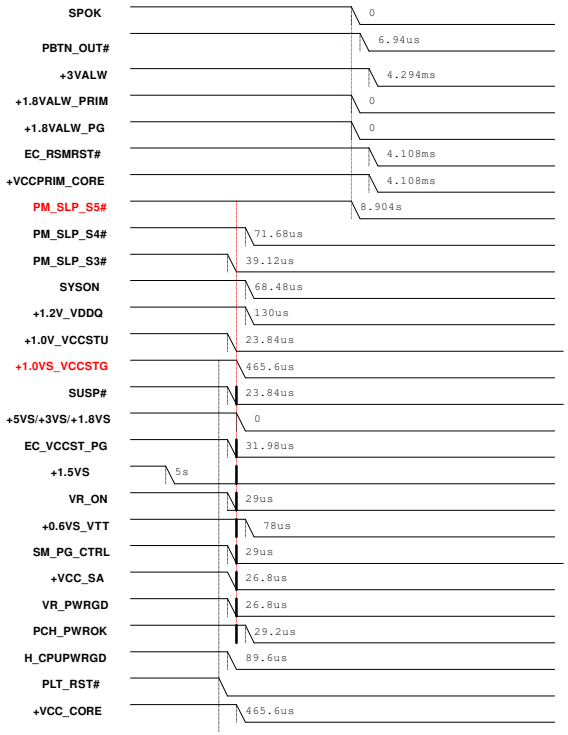
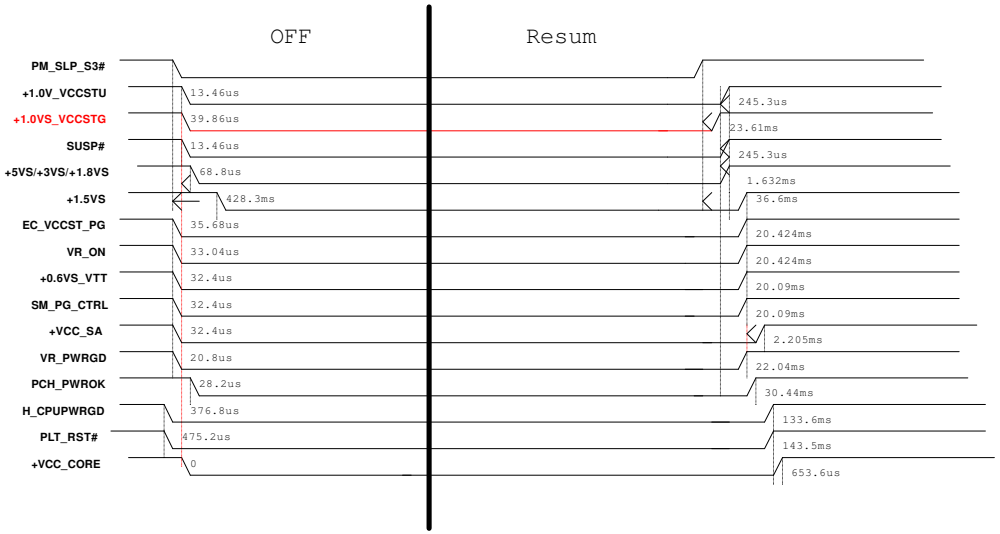
C4PB1/C5PB1 Power on sequence



C4PB1/C5PB1 Power OFF sequence



C4PB1/C5PB1 S3 sequence



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Title: Power Sequence

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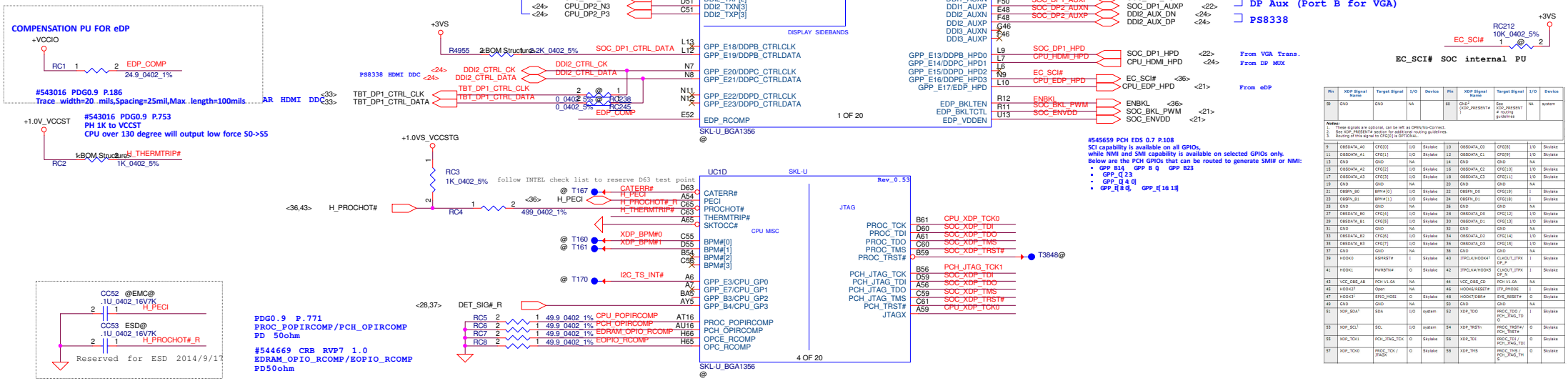
Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.

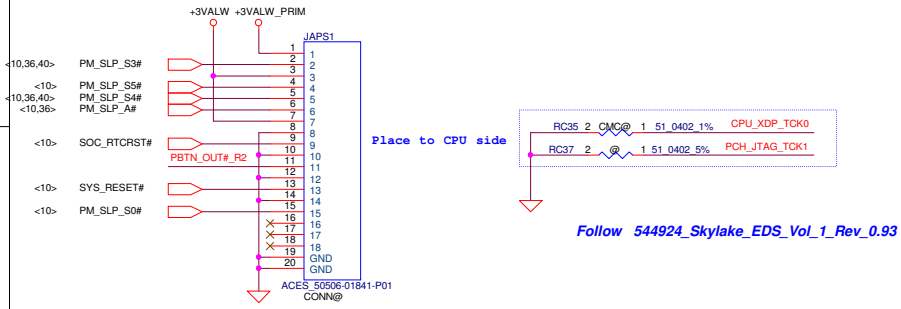


Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
59	GND	GND	NA		60	GND[2] (XDP_PRESENT#)	See XDP_PRESENT# routing guidelines	NA	system

Notes:
1. These signals are optional, can be left as OPEN/No-Connect.
2. See XDP_PRESENT# section for additional routing guidelines.
3. Routing of this signal to CPU[2] is OPTIONAL.

9	OBSDATA_A0	CPU[0]	I/O	Skylake	10	OBSDATA_C0	CPU[8]	I/O	Skylake
11	OBSDATA_A1	CPU[1]	I/O	Skylake	12	OBSDATA_C1	CPU[9]	I/O	Skylake
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2	CPU[2]	I/O	Skylake	16	OBSDATA_C2	CPU[10]	I/O	Skylake
17	OBSDATA_A3	CPU[3]	I/O	Skylake	18	OBSDATA_C3	CPU[11]	I/O	Skylake
19	GND	GND	NA		20	GND	GND	NA	
21	OBSPN_B0	BPM#[0]	I/O	Skylake	22	OBSPN_D0	CPU[19]	I	Skylake
23	OBSPN_B1	BPM#[1]	I/O	Skylake	24	OBSPN_D1	CPU[18]	I	Skylake
25	GND	GND	NA		26	GND	GND	NA	
27	OBSDATA_B0	CPU[4]	I/O	Skylake	28	OBSDATA_D0	CPU[12]	I/O	Skylake
29	OBSDATA_B1	CPU[5]	I/O	Skylake	30	OBSDATA_D1	CPU[13]	I/O	Skylake
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2	CPU[6]	I/O	Skylake	34	OBSDATA_D2	CPU[14]	I/O	Skylake
35	OBSDATA_B3	CPU[7]	I/O	Skylake	36	OBSDATA_D3	CPU[15]	I/O	Skylake
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	RSVRST#	I	Skylake	40	ITPCLK/HOOK4[1]	CLKOUT_ITPX_DP_P	I	Skylake
41	HOOK1	PWRBTN#	O	Skylake	42	ITPCLK#/HOOK5	CLKOUT_ITPX_DP_N	I	Skylake
43	VCC_DBS_AB	PCH V1.0A	NA		44	VCC_DBS_CD	PCH V1.0A	NA	
45	HOOK2[1]	Open	NA		46	HOOK6/RESET#	ITP_PMODE	I	Skylake
47	HOOK3[1]	SPIO_MOSI	O	Skylake	48	HOOK7/DBR#	SYS_RESET#	O	Skylake
49	GND	GND	NA		50	GND	GND	NA	
51	XDP_SDA[1]	SDA	I/O	system	52	XDP_TDO	PROC_TDO / PCH_JTAG_TDO	I	Skylake
53	XDP_SCL[1]	SCL	I/O	system	54	XDP_TRST#	PROC_TRST# / PCH_TRST#	O	Skylake
55	XDP_TCK1	PCH_JTAG_TCK	O	Skylake	56	XDP_TDI	PROC_TDI / PCH_JTAG_TDI	O	Skylake
57	XDP_TCK0	PROC_TCK / JTAGX	O	Skylake	58	XDP_TMS	PROC_TMS / PCH_JTAG_TMS	O	Skylake

APS CONN



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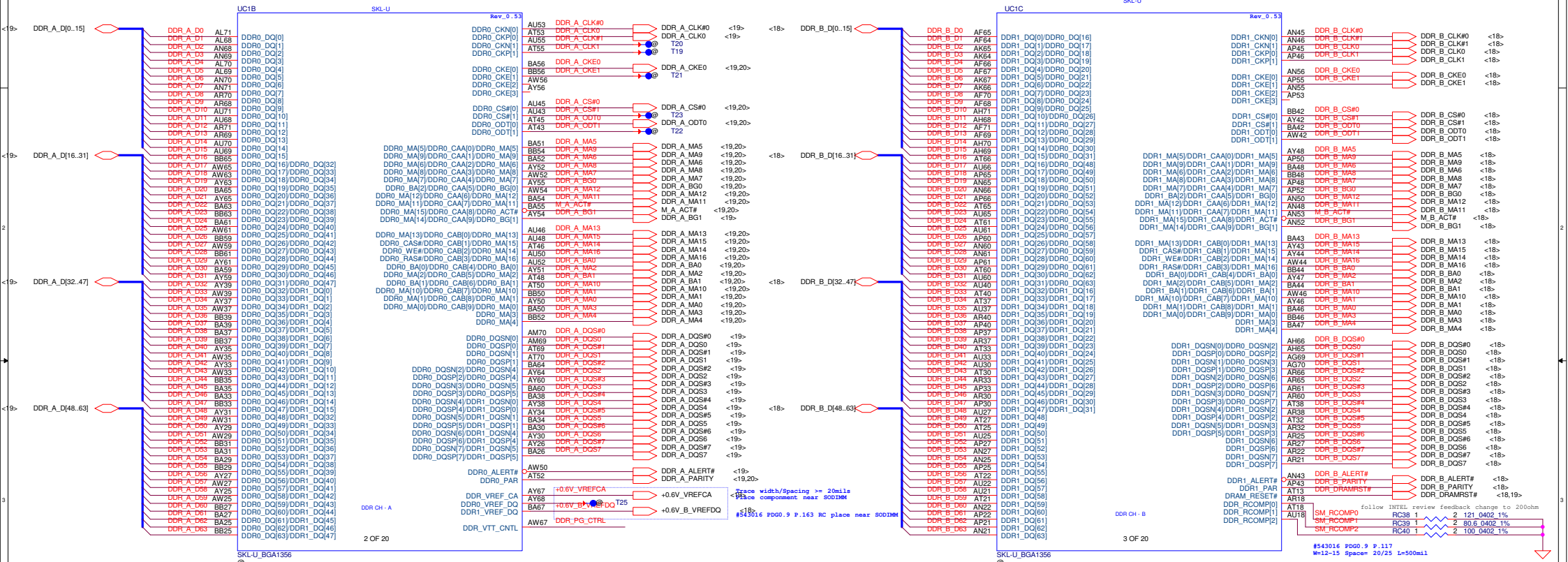
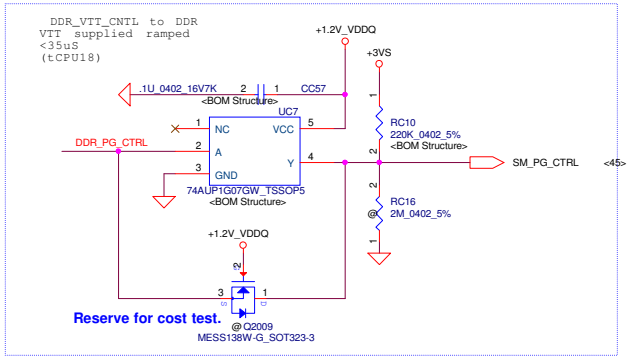
Interleaved Memory





ES Sample

UC1 CPU_QHMF_C0_2.3G QHMF@ SA00008M420

UC1 CPU_QHMG_C0_1.6G QHMG@ SA00008M320

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Title: SKL-U(2/12)DDR

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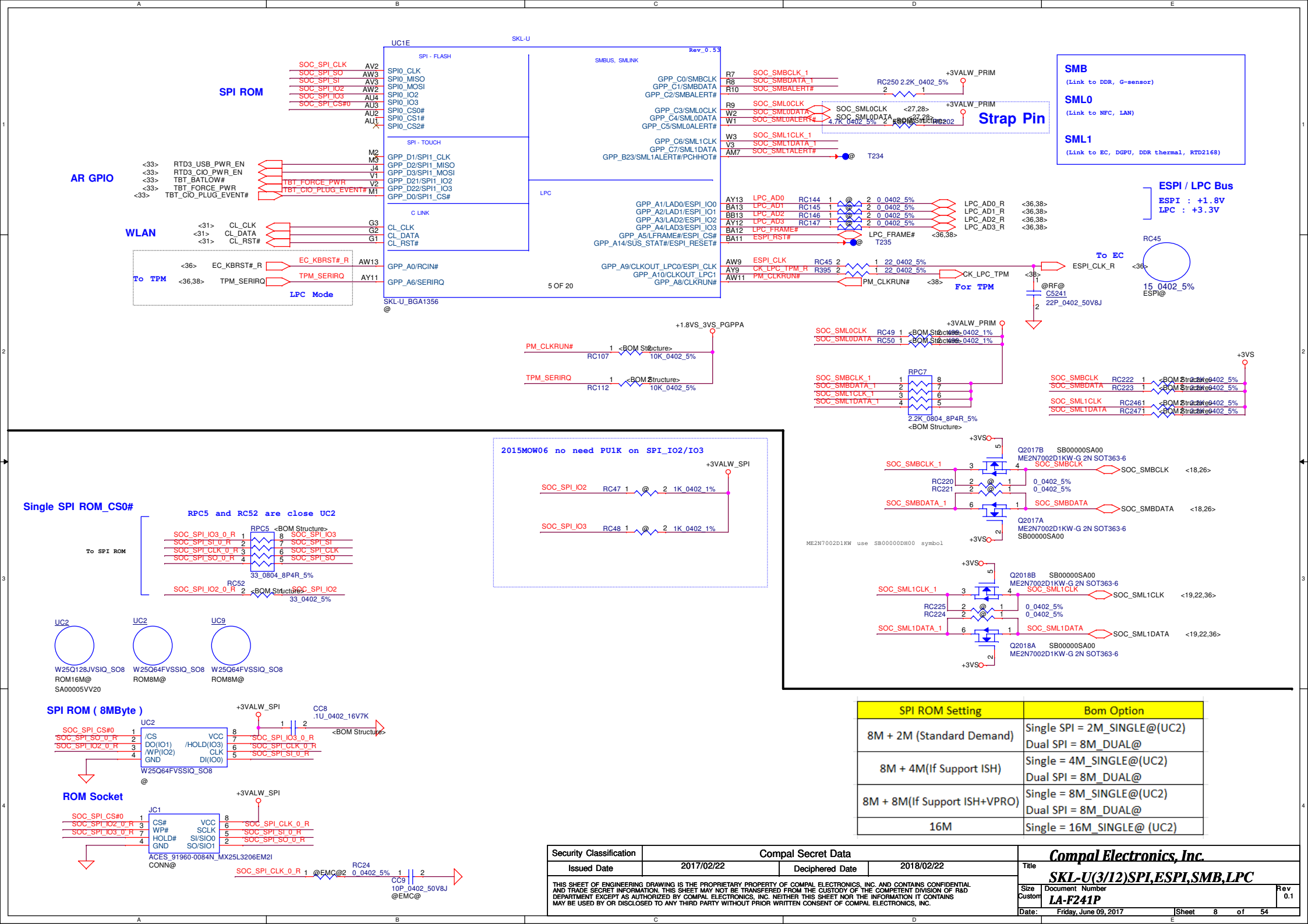

SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

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#545659 SKL_PCH_EDS_R0.7 P.84

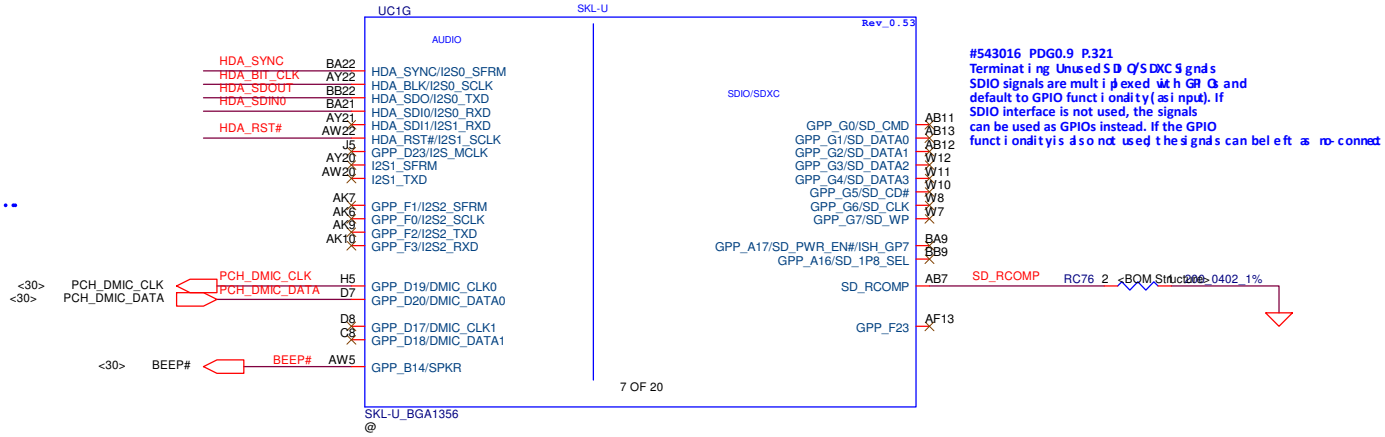
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.



#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect

SD_RCOMP RC76 2 <BOM Structure> 200_0402_1%

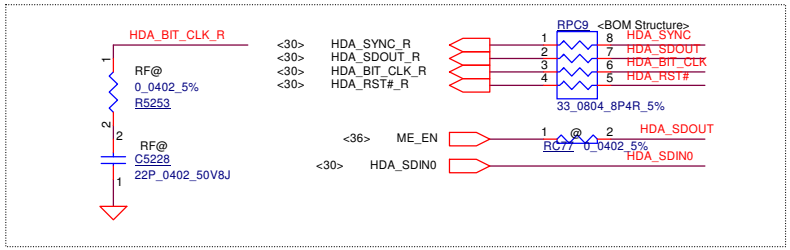
62.3.38 RCOMP Checklist

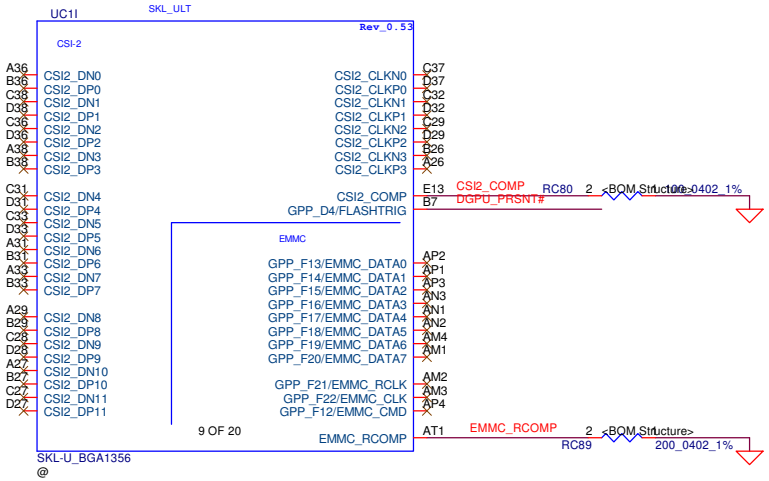
Table 62-48. RCOMP Checklist

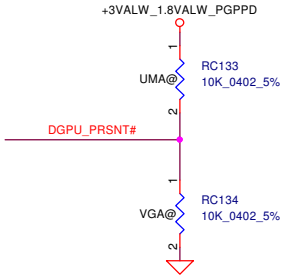
Component	Value	✓
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

HDA for AUDIO







	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data	
Issued Date	2017/02/22	Deciphered Date: 2018/02/22

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size	Document Number	Rev
Custom	LA-F241P	0.1

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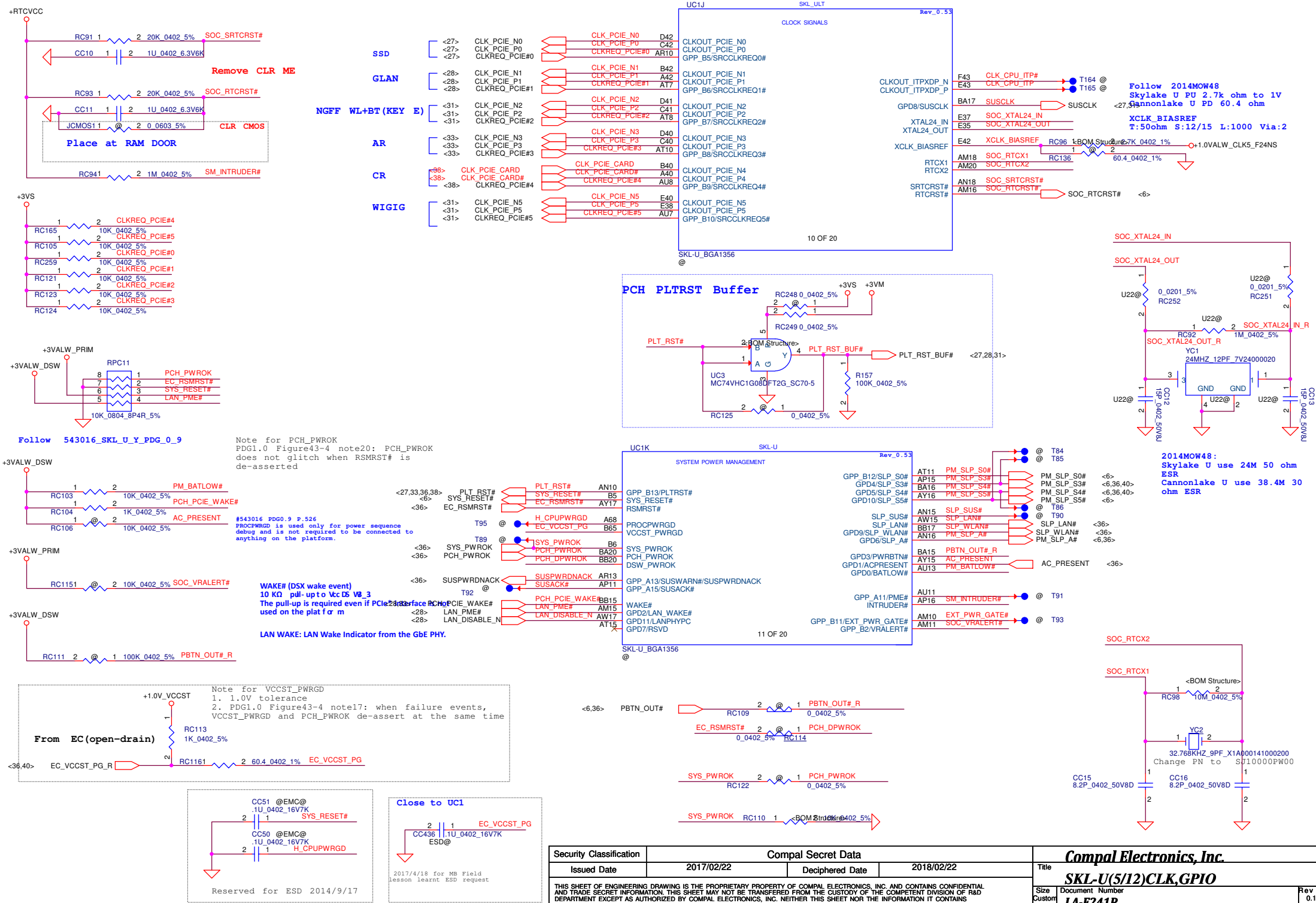

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,GPIO		
Size: Custom	Document Number: LA-F241P		Rev: 0.1
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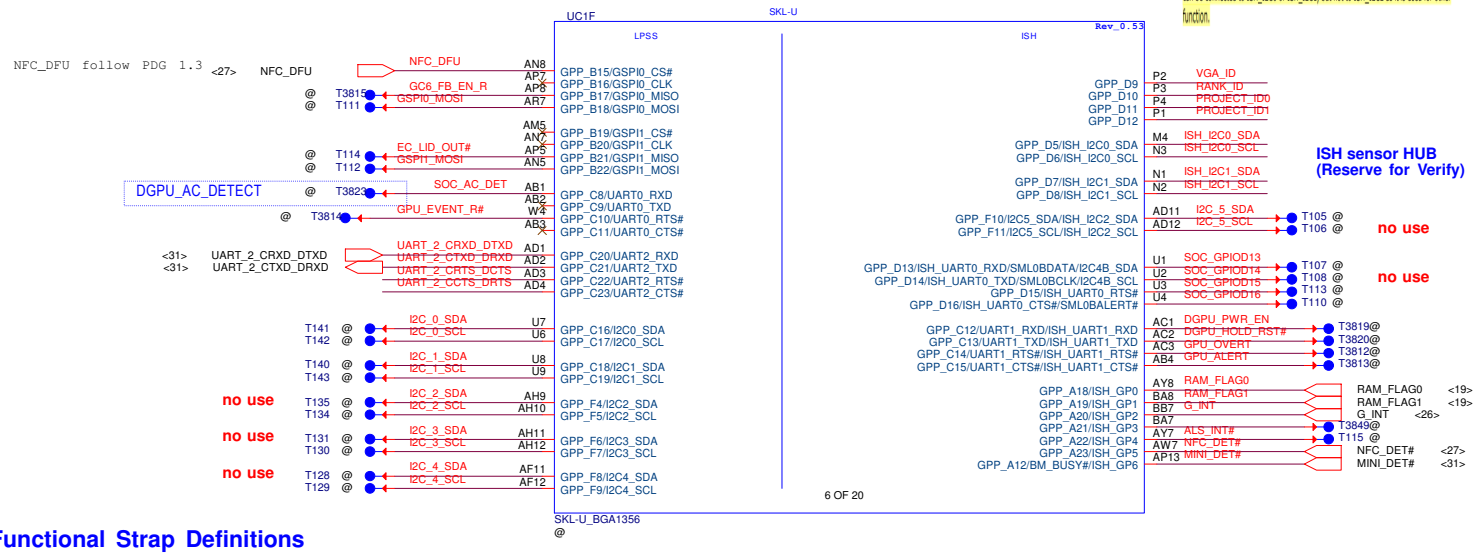
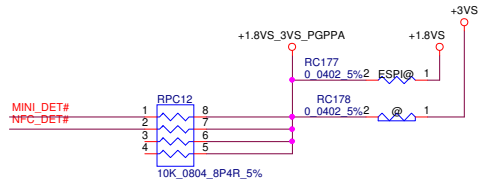
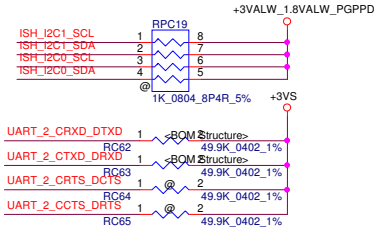
543016 SKY PDG 0.9 P.401

The sensors are connected to ISH through ISH I2C interface and ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but not to ISH_I2C2 as it is used for other function.







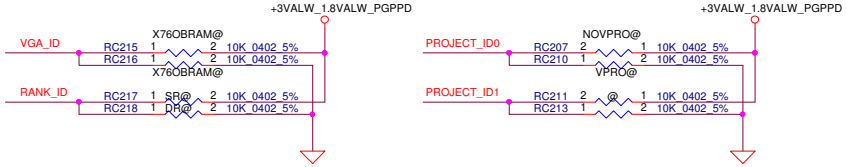
Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
0 = SPI Mode --> AAX05 Use
1 = LPC Mode

D4PB1/D5PB1	VGA_ID	GPP_D9
Change to On Borad Ram ID Page.19	GL	0
	GM	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*B4DBU+VPRO	0	0
B4DBU+NVPRO	0	1
Reserved	1	0
Reserved	1	1

SMLOALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

RANK_ID	GPP_D10
DR	0
SR	1

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

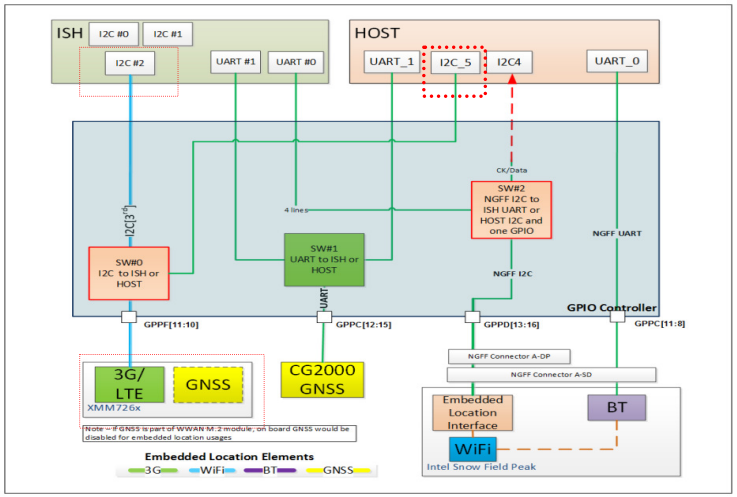
TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto (TLS) (with confidentiality).
Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port D is not detected.
1 =Port D is detected.

I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: SKL-U(6/12)GPIO			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Wednesday, June 14, 2017	Sheet 11 of 54		

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC / USB3

USB2

8 OF 20

SKL-U_BGA1356

@

CR

GLAN

NGFF WLAN+BT(Key E)

HDD

Wigig

Thunderbolt

SSD

#543016 P.239 PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12 S=12 R=100ohm

IO/B

USB3 MB

DOCKING

IO/B

IO/B

USB3 MB

Camera

FP

LTE

TS

BT

NFC

AG3,AG4 PD1K for DCI warm boot fail issue (follow PCH EDS1.2) 2015MOW10, USB2_ID connected to GND

NFC_IRQ,RST# follow PDG 1.3

Close to UC1

2017/4/18 for MB Field lesson learnt ESD request

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
•When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
•When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
•The processor provides three SATA general purpose input signals,SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
•When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
•If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

High Speed I/O (HSIO) Lane Multiplexing in SKL U

Acer HSIO def i ne

GPIO	DEVICE CONTROL
USB_OC0#	USB Port 1,2,4
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NFC
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	SSD
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

Security Classification	Compal Secret Data	
Issued Date	2017/02/22	Deciphered Date 2018/02/22

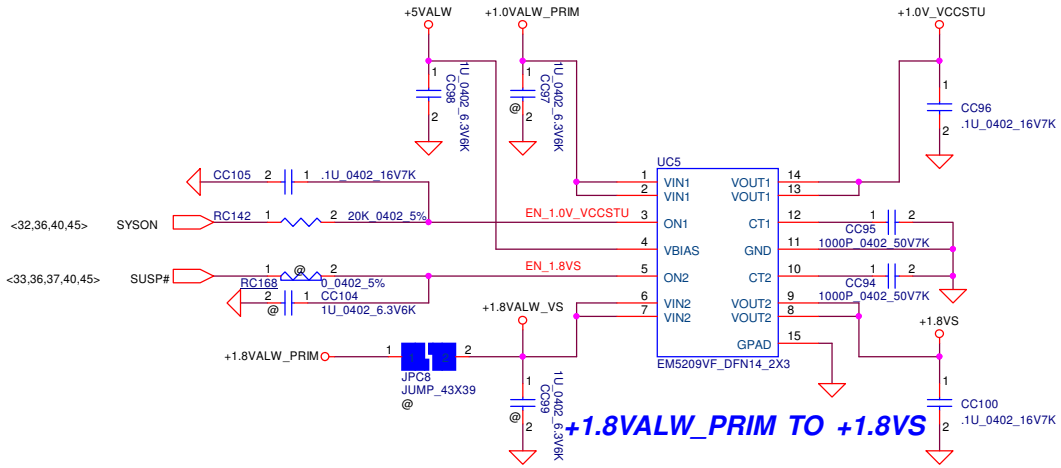
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size: Custom | Document Number: LA-F241P | Rev: 0.1

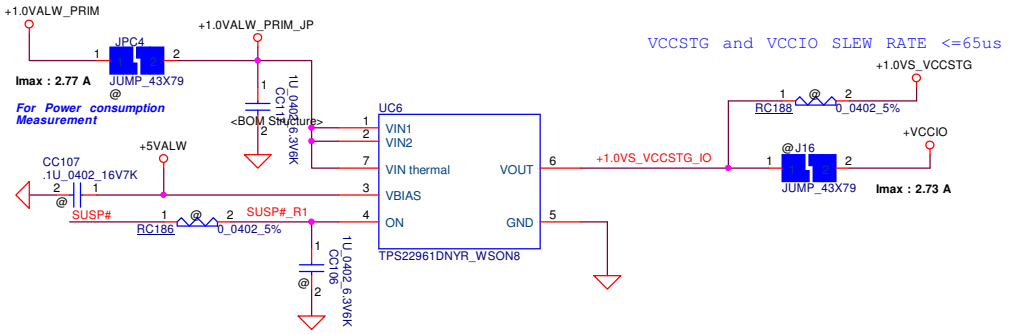
Date: Friday, June 09, 2017 | Sheet 12 of 54

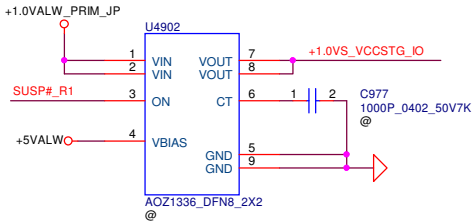
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

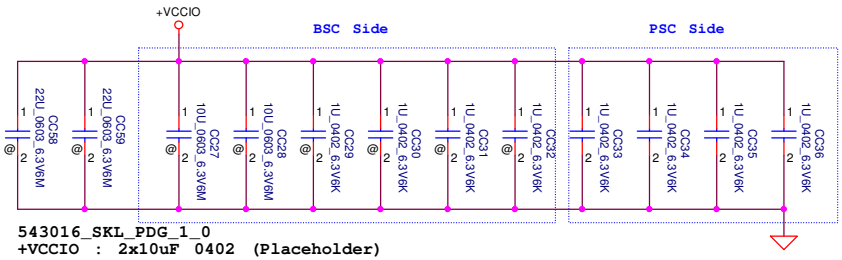


+1.8VALW_PRIM TO +1.8VS

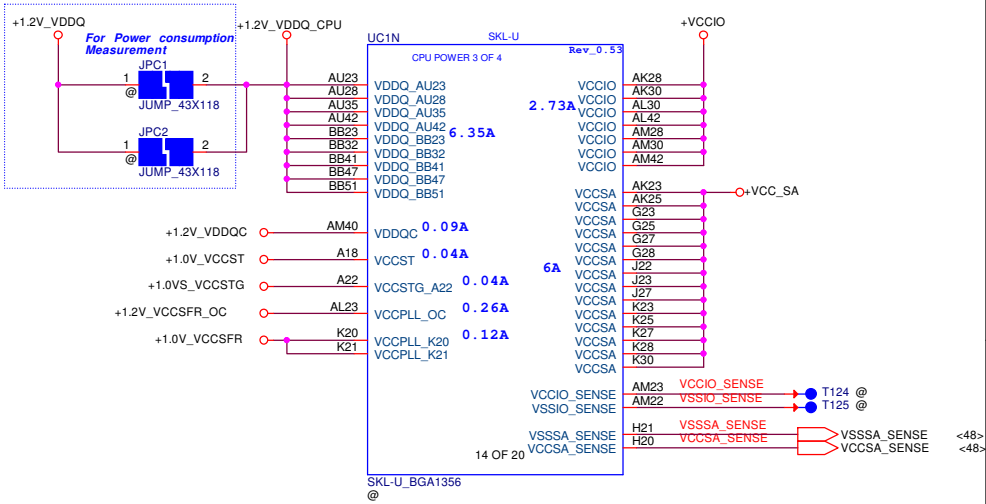
+1.0VALW_PRIM TO +1.0VS_VCCSTG

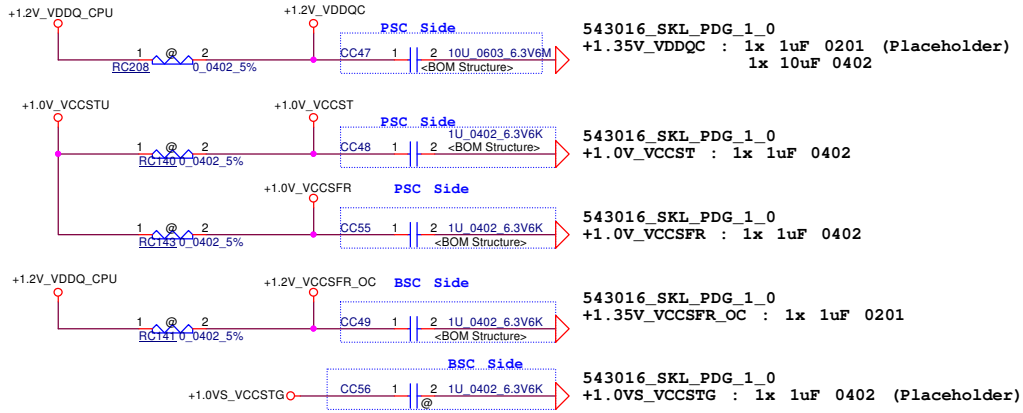


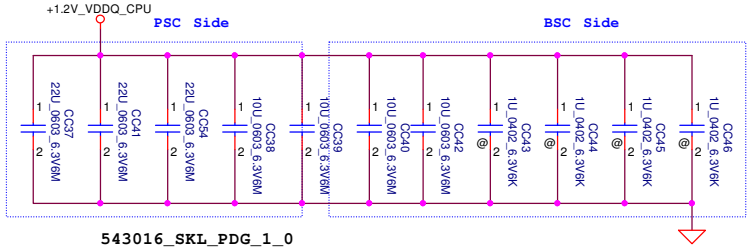




543016_SKL_PDG_1_0
+VCCIO : 2x10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 1uF 0402







543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402
3x 22uF 0603

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size	Document Number	Rev
Custom	LA-F241P	0.1

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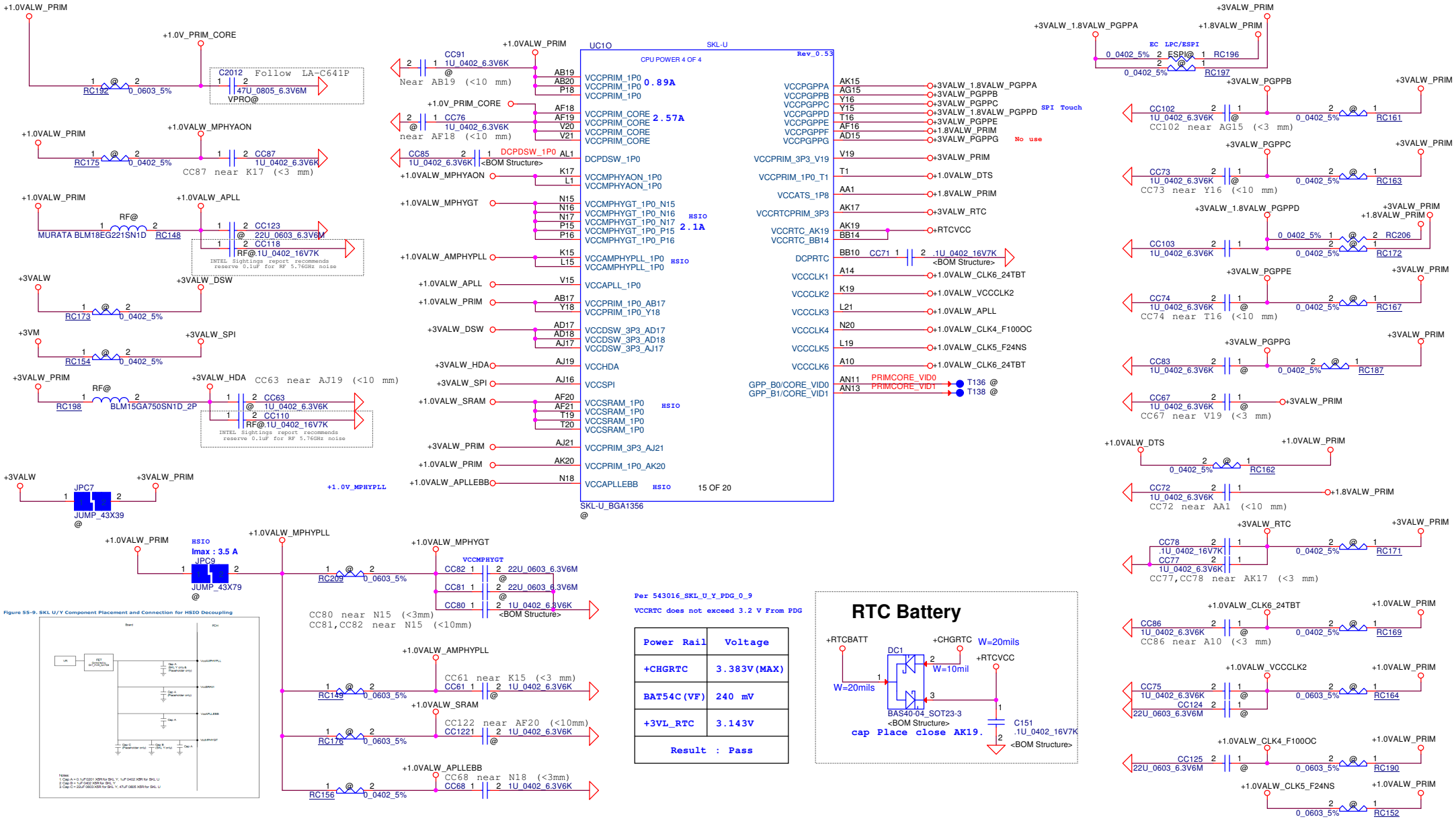

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size	Document Number	Rev
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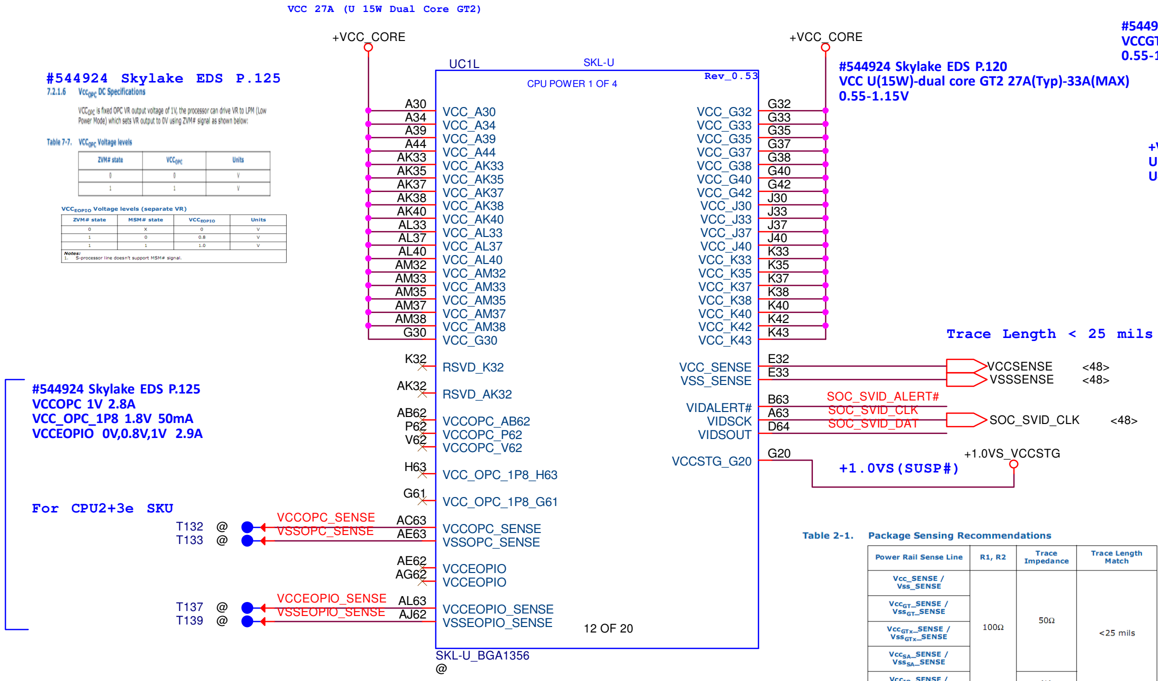


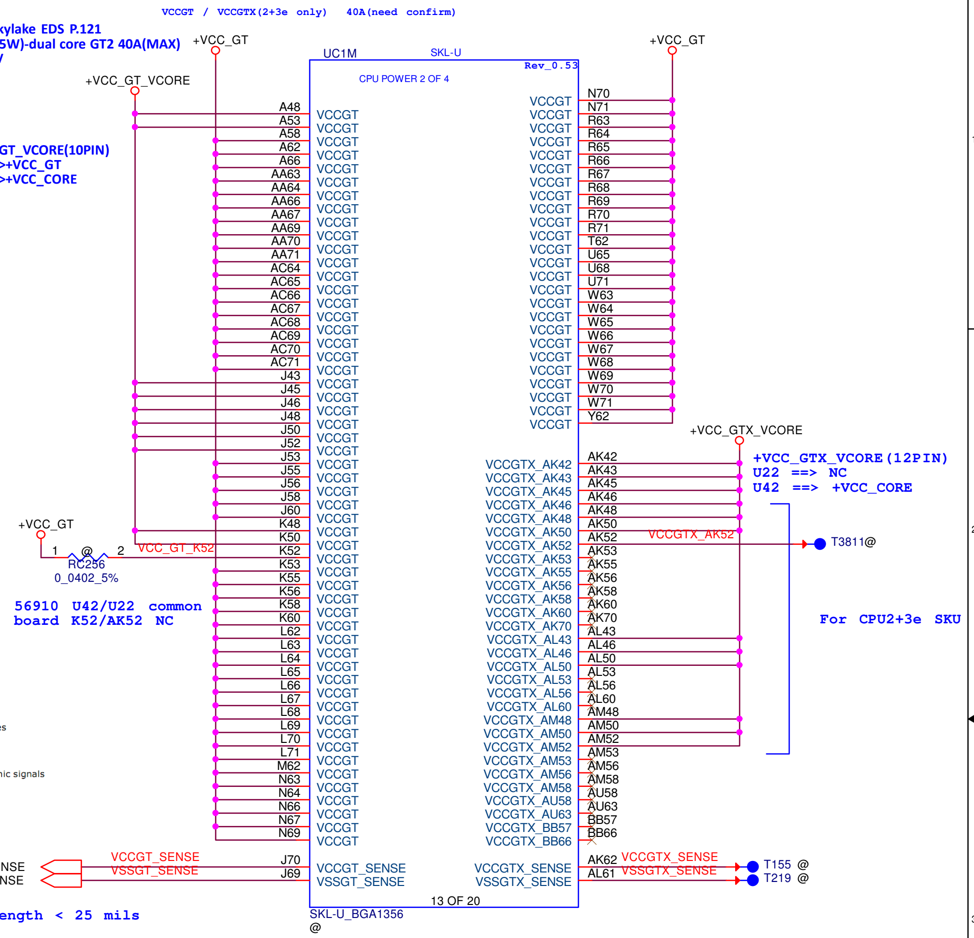
Table 2-1. Package Sensing Recommendations

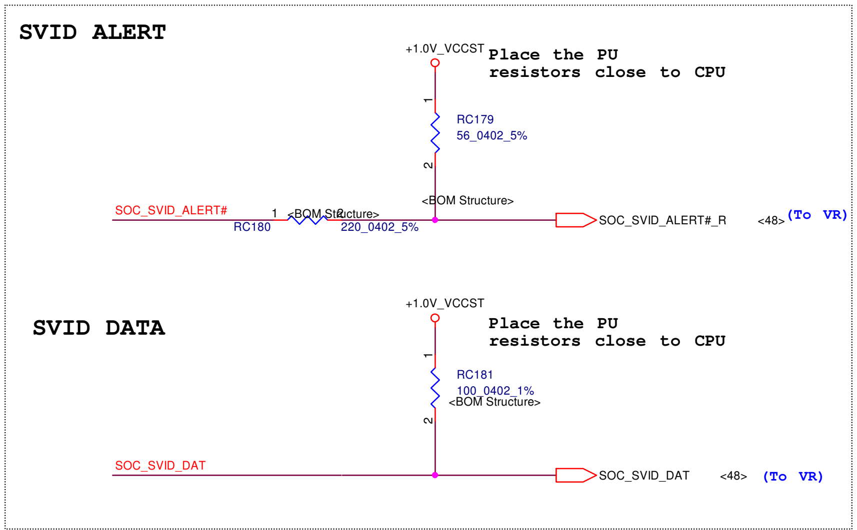
Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{GTx}_SENSE / Vss_{GTx}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals





543016 PDG0.9 P.189 Need check

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDSCK							100	100	0	10	
VIDALERT#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
V_{CCGT}	Processor Graphics Power Rails	SVID
V_{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V_{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V_{CCIO}	IO Power Rail	Fixed
V_{CCST}	Sustain Power Rail	Fixed
V_{CCPLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V_{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V_{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CCEOPIO}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **SKL-U(10/12)Power,SVID**

Size: Custom | Document Number: LA-F241P | Rev: 0.1

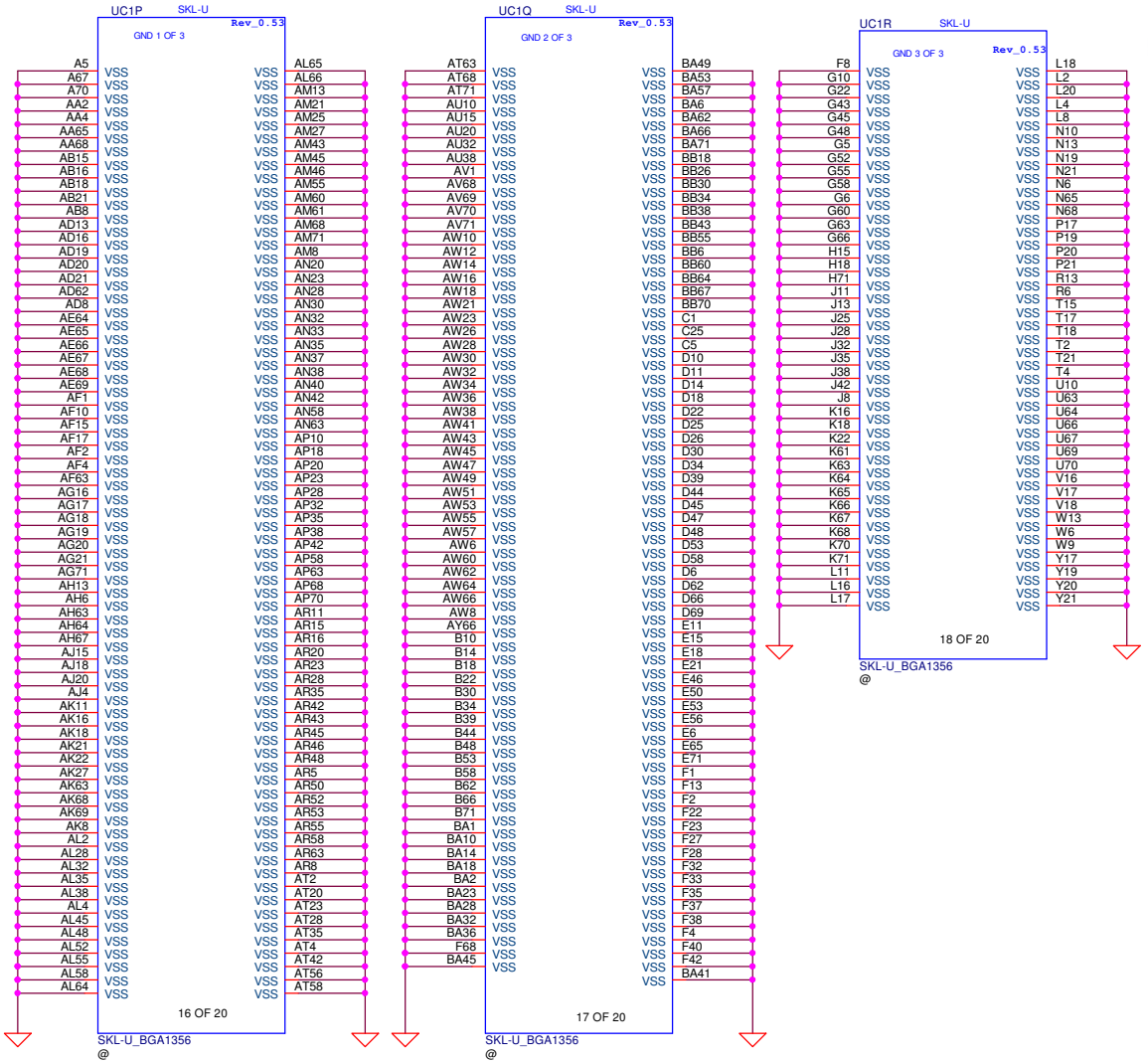
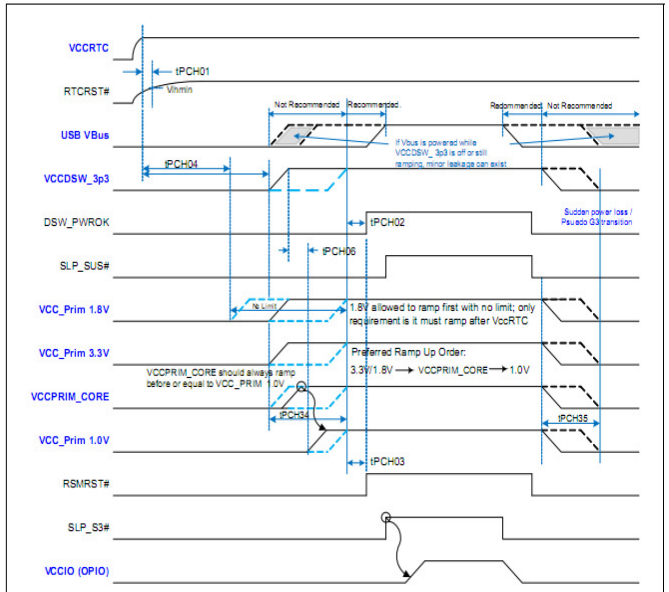


Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



Notes:

1. VCC_PRIM 1.8 V includes VCCPGPPF, VCCATS and may include VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCC_PRIM 3.3 V includes VCCPRIM_3p3 and VCCRTCPRIM_3p3.
3. VCCPRIM_CORE is only applicable on SKL U/Y. For SKL H, the rail is merged with VCCPRIM_1p0.
4. VCC_PRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: SKL-U(11/12)GND			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
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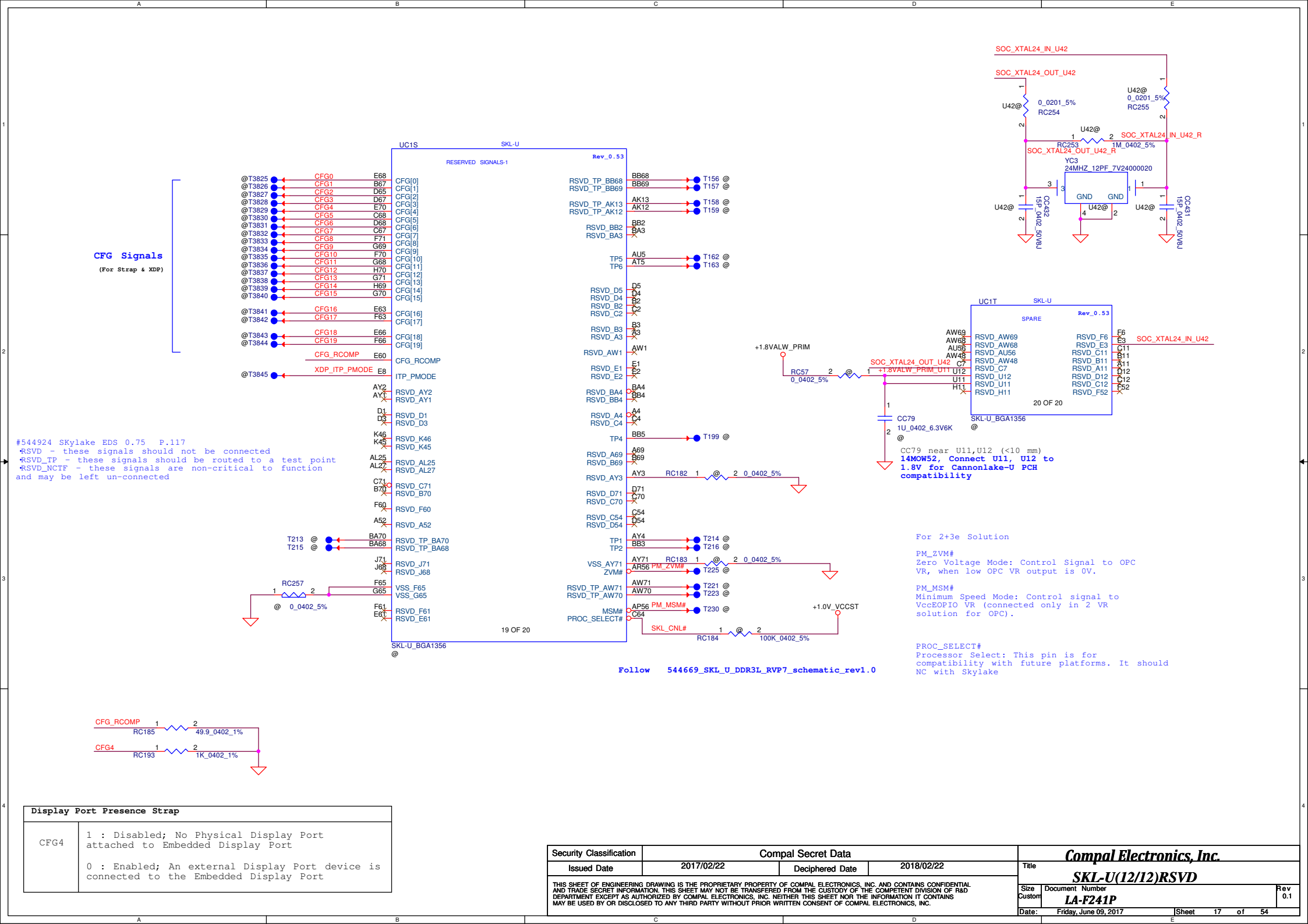

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: LA-F241P | Rev: 0.1

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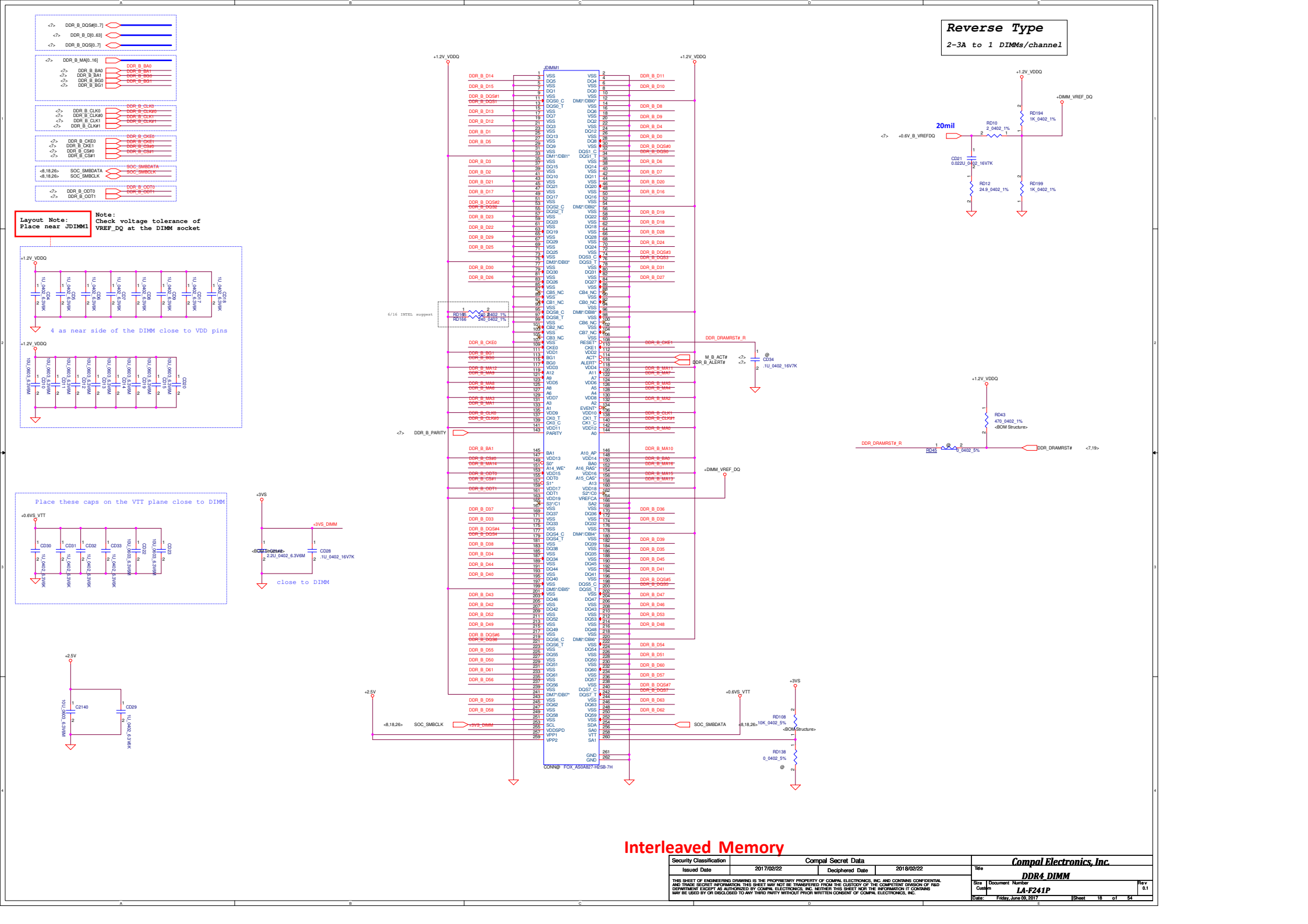
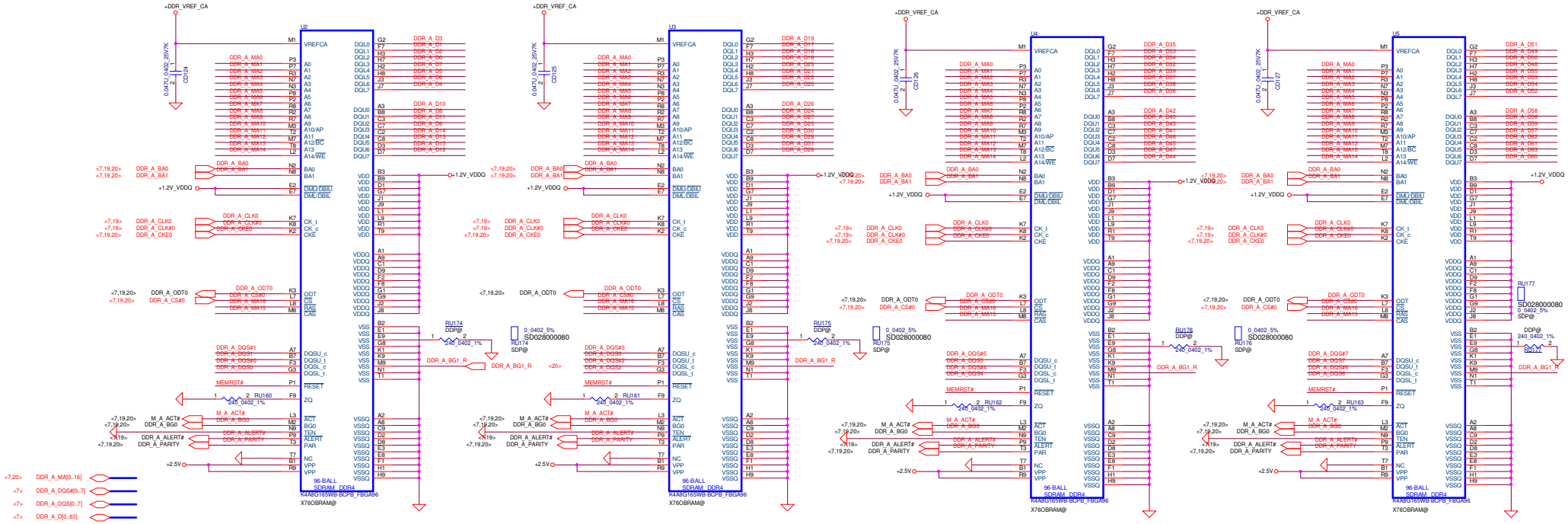
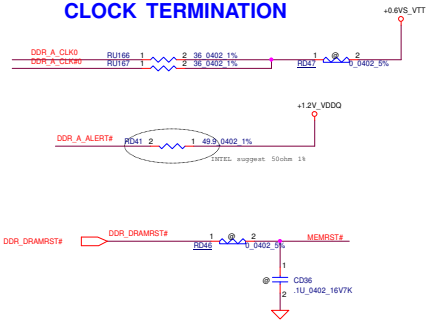

Reverse Type
2-3A to 1 DIMMs/channel
Layout Note:
Place near JDIMM1
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket
4 as near side of the DIMM close to VDD pins
Place these caps on the VTT plane close to DIMM
close to DIMM
20mil
JDIMM1
CONN@ FOX_AS0A827-HZSB-7H
Interleaved Memory
Compal Electronics, Inc.
DDR4 DIMM
LA-F241P
Security Classification
Compal Secret Data
Issued Date
2017/02/22
Deciphered Date
2018/02/22
Friday, June 09, 2017



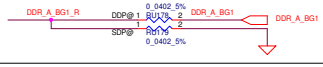
Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

CLOCK TERMINATION



Co-lay for SDP/DDP



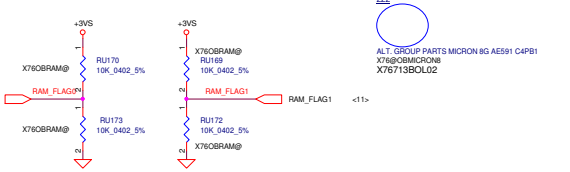
on board ram flag	VGA_ID (D4PB1/D5PB1)	FLAG1	FLAG0
hynix 8G(DDP) SA0000ARA10	0	0	0
Micron 4G(SDP) SA00009V220	0	0	1
hynix 4G(SDP) SA0000A1H20	0	1	0
MICRON 8G (DDP) SA0000A3120	0	1	1
No on baord RAM	1	0	0
	1	0	1
	1	1	0
	1	1	1

ZZZ
ALT_GROUP PARTS HYNIX 8G C4PB1
X76@OBHYNIX8
X76713BOL06

ZZZ
ALT_GROUP PARTS HYNIX 4G AE591 C4PB1
X76@OBHYNIX4
X76713BOL03

ZZZ
ALT_GROUP PARTS MICRON 4G AE591 C4PB1
X76@OBMICRON4
X76713BOL01

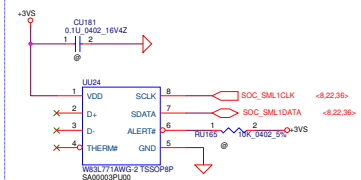
ZZZ
ALT_GROUP PARTS MICRON 8G AE591 C4PB1
X76@OBMICRON8
X76713BOL02



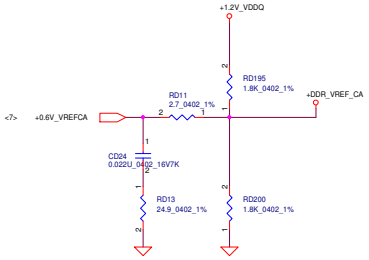
X76OBRAM@ Level includes U2~U5, RU169, RU170, RU172, RU173, RC215 and RC216

2017/6/8
confirm Thermal/EC change to reserve

External DDR Thermal Sensor



SA00003PU00
S IC W83L771AWG-2 TSSOP 8P SENSOR



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

LA-F411P

Title: **DDR4 ON BOARD CHIPS**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 14, 2017 | Sheet 19 of 54

<7,19> DDR_A_MA[0..16]

+1.2V_VDDQ

4 as near each on board RAM device as possible

Follow MA51

CU89 330U_D2_2V_Y
SCA00009S00
330U 2V H1.9
9mohm POLY

+2.5V

2 as near each on board RAM device as possible

<BOM Structure>

+0.6VS_VTT

2 as near each on board RAM device as possible

+0.6VS_VTT

RP17 DDR_A_MA9 DDR_A_MA5 DDR_A_MA0 DDR_A_MA1 36_0804_8P4R_5%

RP18 DDR_A_MA6 DDR_A_MA11 DDR_A_MA7 DDR_A_MA4 36_0804_8P4R_5%

RP19 DDR_A_MA14 DDR_A_MA13 DDR_A_BA0 DDR_A_BA1 36_0804_8P4R_5%

<7,19> DDR_A_BA0
<7,19> DDR_A_BA1

RP20 DDR_A_ODT0 DDR_A_CS#0 DDR_A_MA15 DDR_A_MA10 36_0804_8P4R_5%

<7,19> DDR_A_ODT0
<7,19> DDR_A_CS#0

RP21 DDR_A_BG0 DDR_A_MA12 M_A_ACT# DDR_A_CKE0 36_0804_8P4R_5%

<7,19> DDR_A_BG0
<7,19> M_A_ACT#
<7,19> DDR_A_CKE0

RP22 DDR_A_MA13 DDR_A_MA8 36_0804_8P4R_5%

RP24 DDR_A_MA3 DDR_A_MA2 DDR_A_PARITY 36_0804_8P4R_5%

<7,19> DDR_A_PARITY

<19> DDR_A_BG1_R

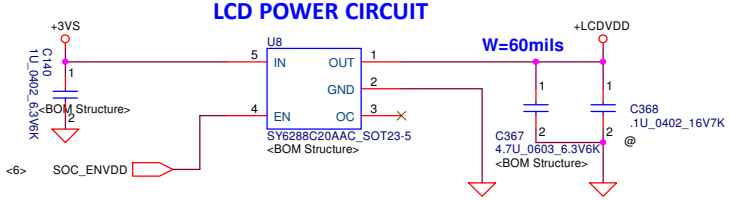
DDR_A_BG1_R RU180 DDP@ 36_0402_1%

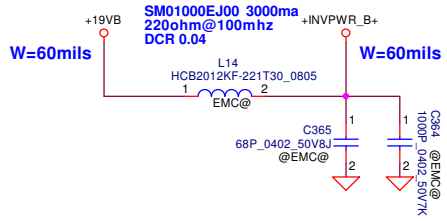
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

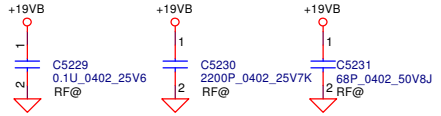
Title: DDRIII ON BOARD CHIPS

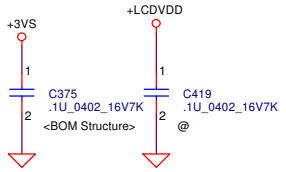
Size: Custom	Document Number	Rev: 0.1
Date: Friday, June 05, 2017	Sheet 20 of 54	

LCD POWER CIRCUIT

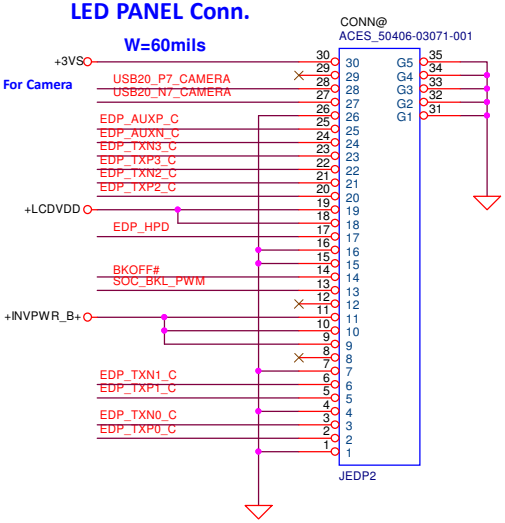


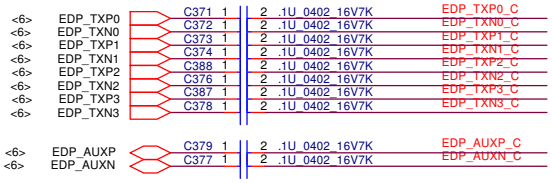


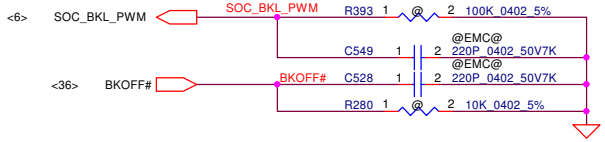


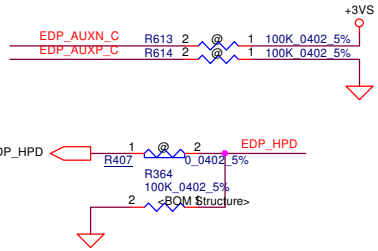


LED PANEL Conn.



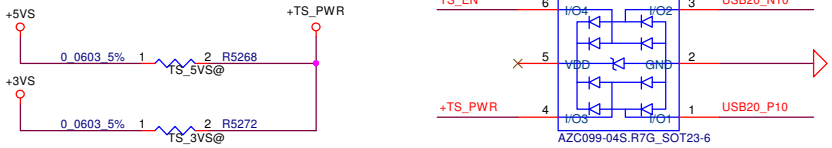


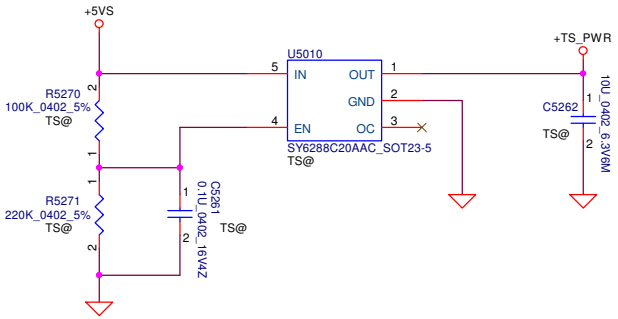


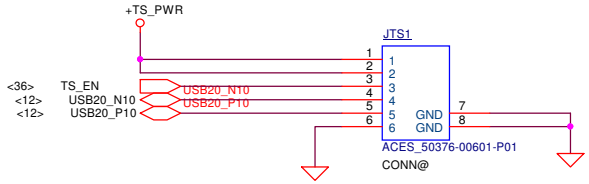


SP010011Z00

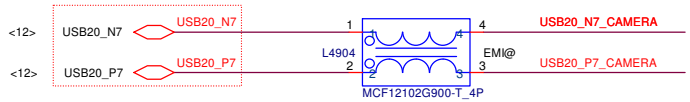
Touch Screen Conn.







Camera



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: eDP/TS Connector

Size	Document Number	Rev
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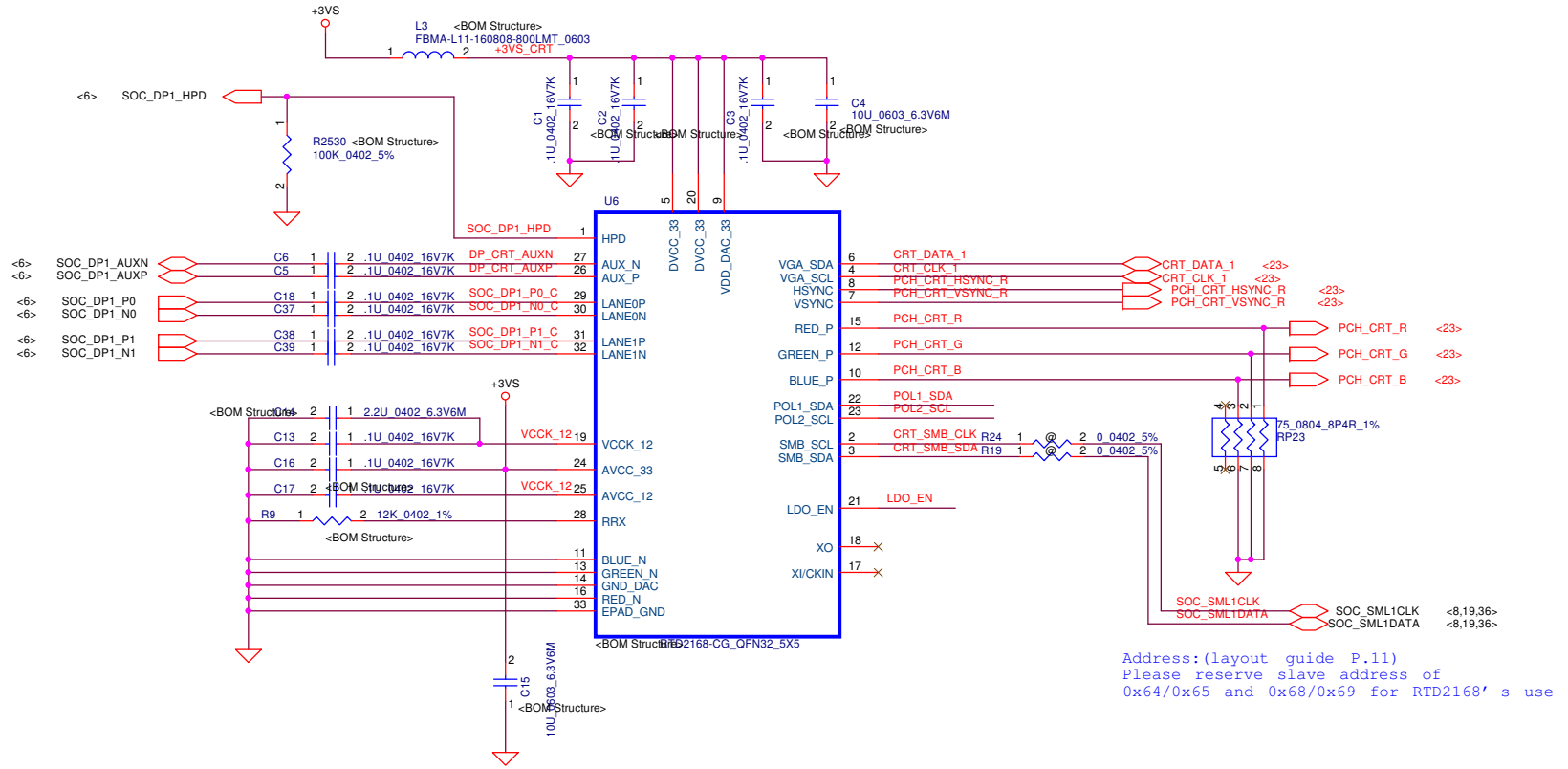
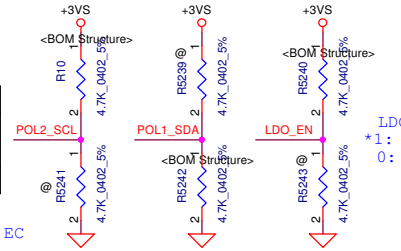


Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168' s use



		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

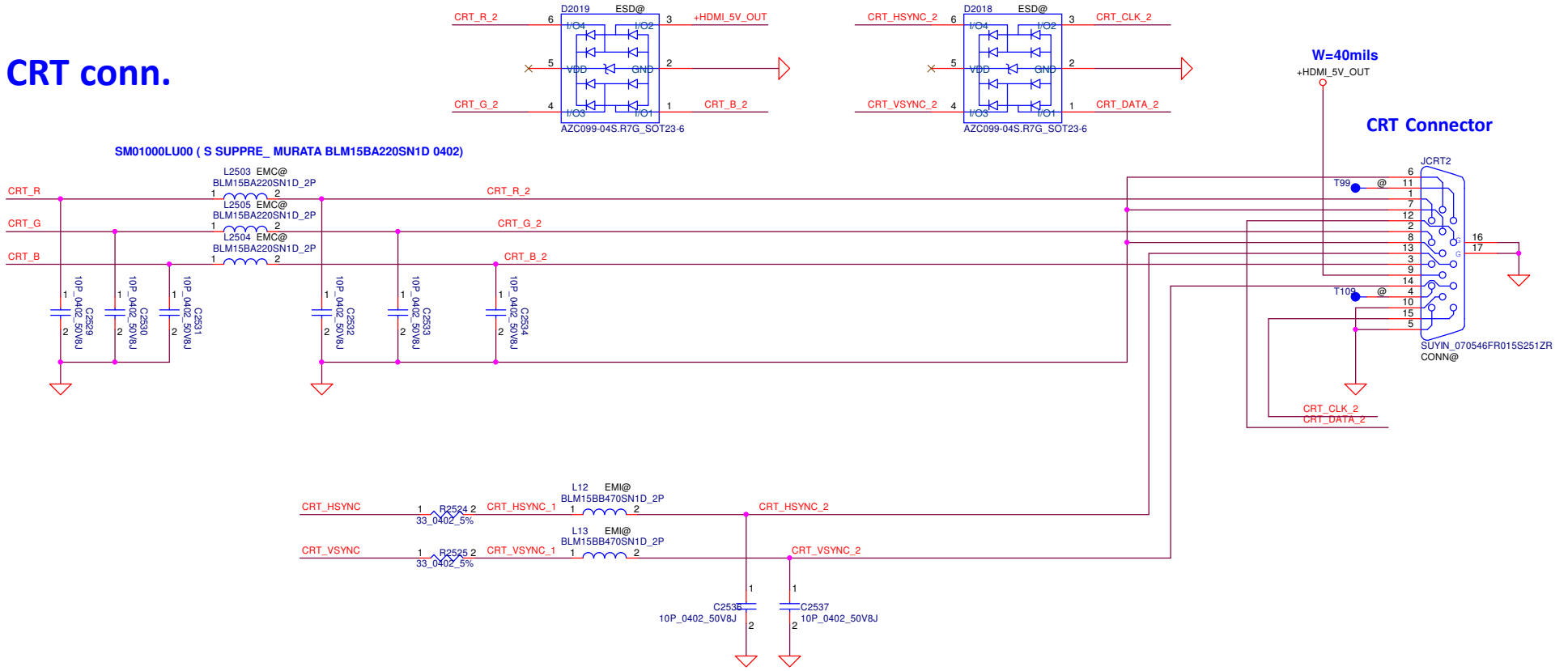
ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

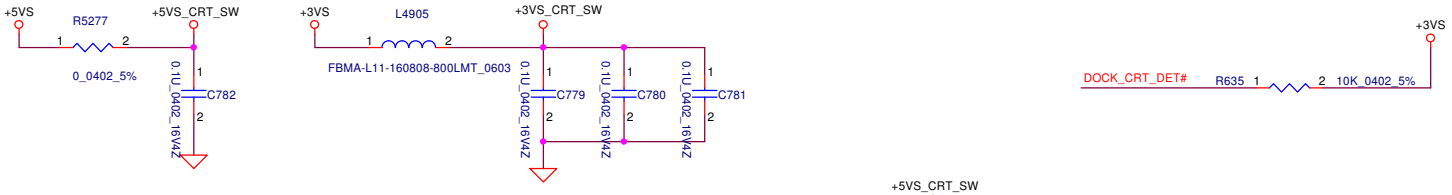
LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

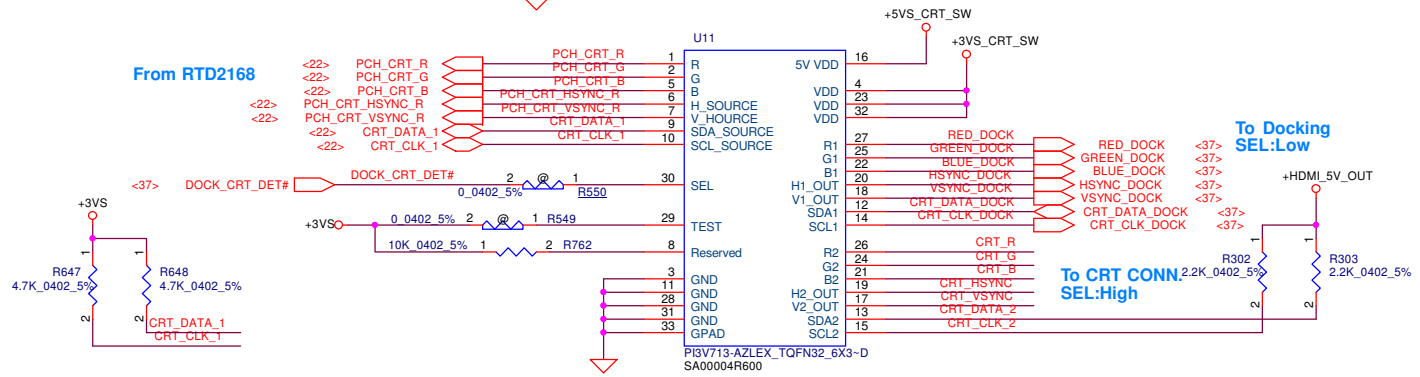
Compal Electronics, Inc.			
Title	Realtek RTD2168		
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 22 of 54		

CRT conn.





SELx	Function
L	port 1 is chose
H	port 2 is chose



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: CRT CONN.

Size	Document Number	Rev
Custom	LA-F241P	0.1

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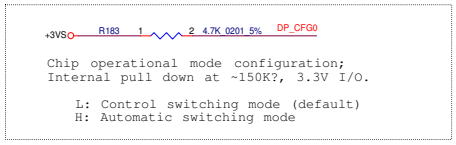
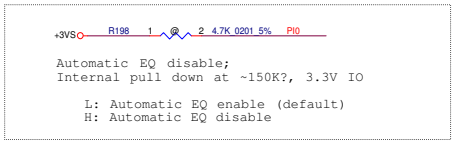


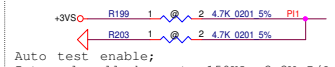
Chip operational mode configuration;
Internal pull down at ~150K?, 3.3V I/O.

L: Control switching mode (default)
H: Automatic switching mode

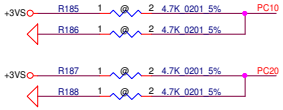


Automatic EQ disable;
Internal pull down at ~150K?, 3.3V IO

L: Automatic EQ enable (default)
H: Automatic EQ disable

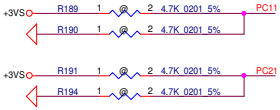


Auto test enable;
Internal pull down at ~150K?, 3.3V I/O.
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable



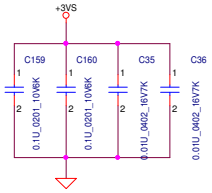
AUX interception disable for Port y (y=1,2)
Internal pull down at ~150K?, 3.3V I/O.

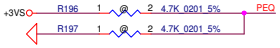
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mv and 0dB
M: AUX interception disable, driver output with fixed 400mv and 0dB



Output swing adjusment for Port y (y=1,2).
Internal pull down at ~150K?, 3.3V I/O.

L:default
H: +20%
M: -16.7%



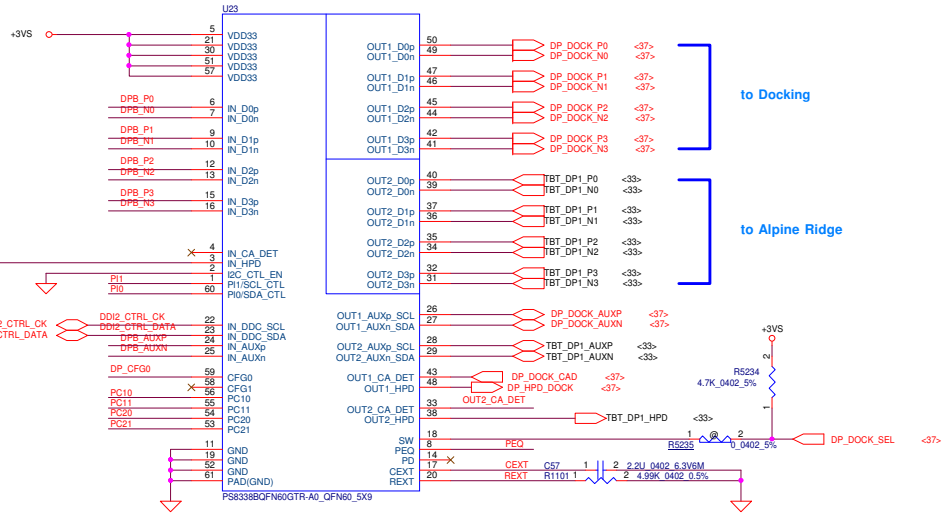


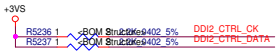
Programmable input equalization levels; Internal pull down at ~150K?, 3.3V I/O.

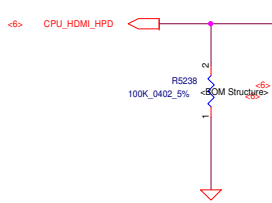
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

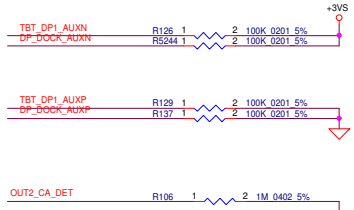
DP_MUX_SEL pin

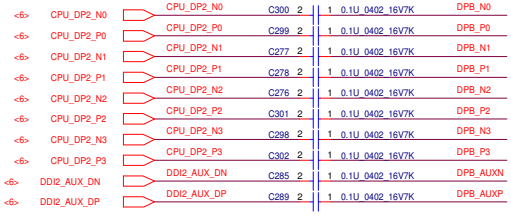
Port switching control or priority configuration;
Internal pull down at ~150K?, 3.3V I/O.
L: Port1 is selected or with higher priority (default)
H: Port2 is selected or with higher priority











Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **P32-DP MUX**

Size	Document Number	Rev
	LA-F241P	0.1

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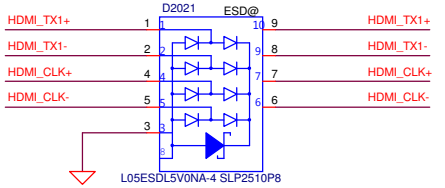
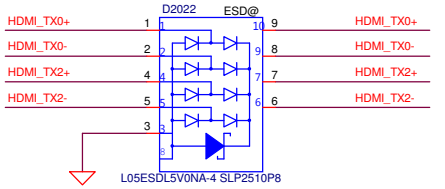
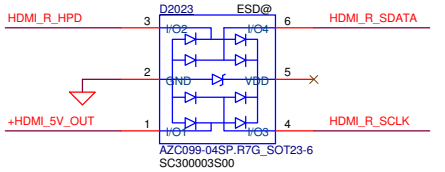
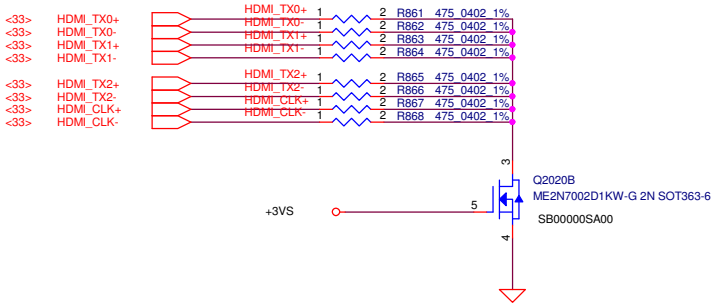
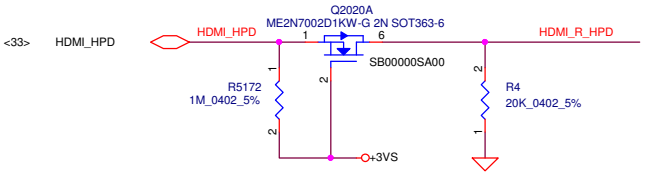
2017/4/17 add diode for ESD request

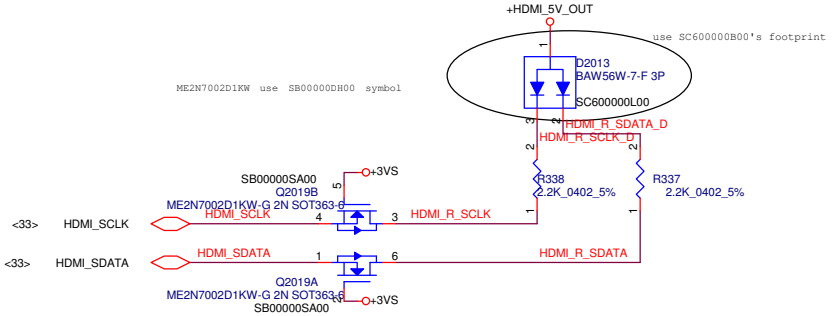


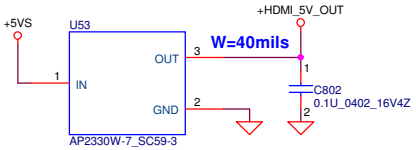




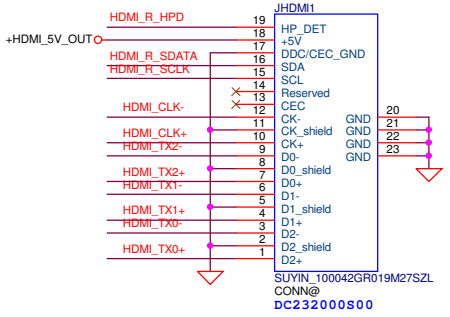








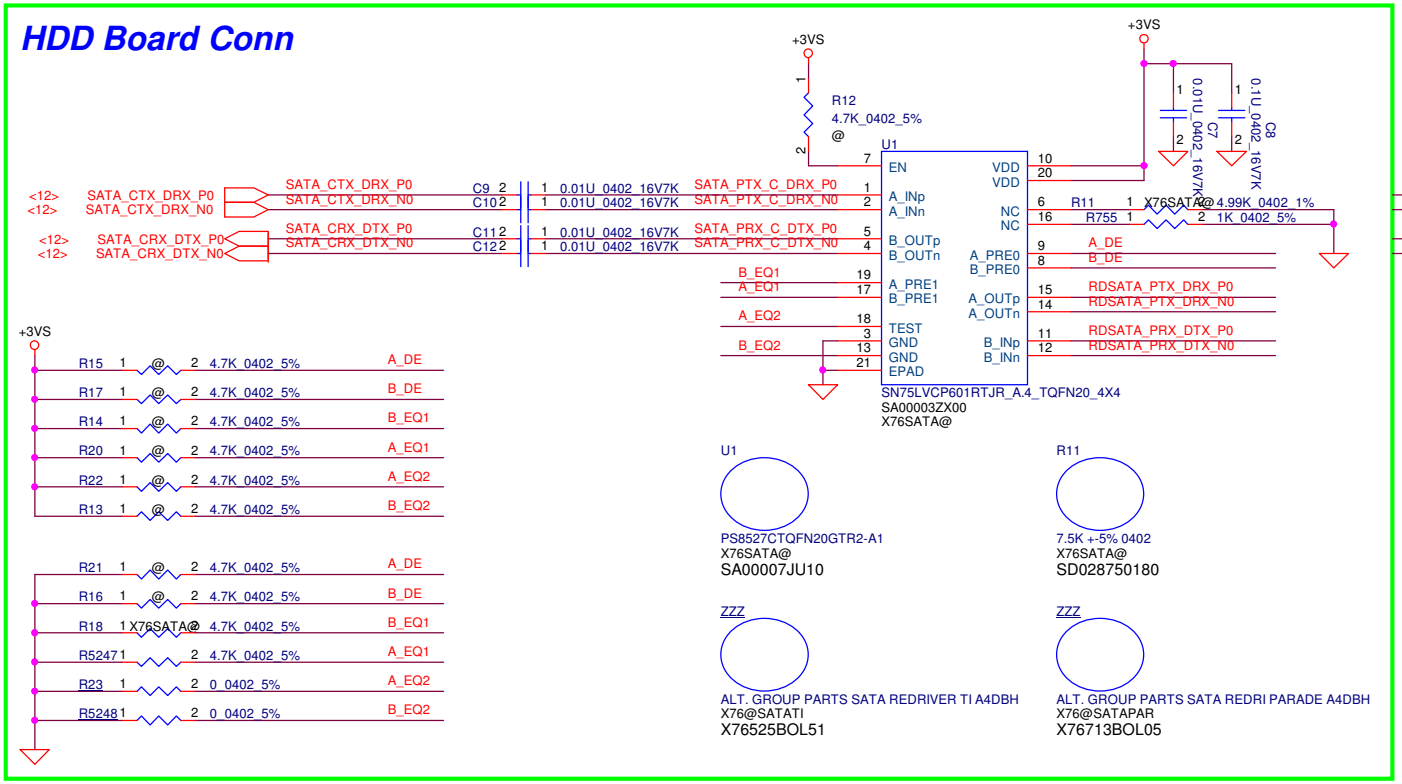
HDMI connector

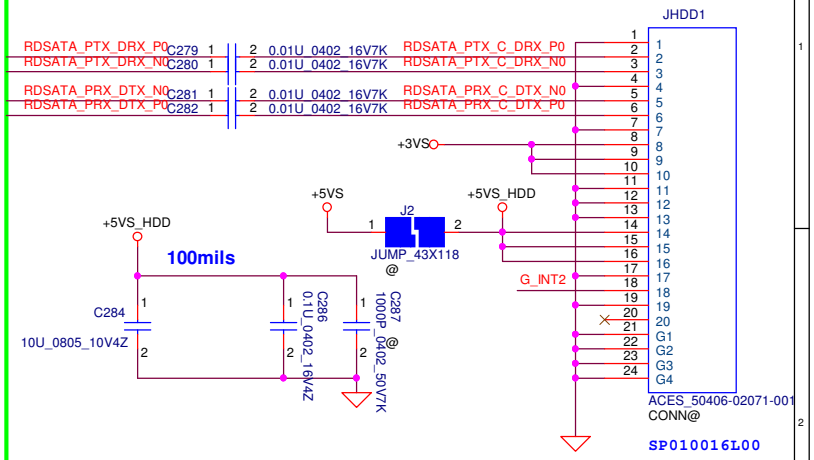


Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

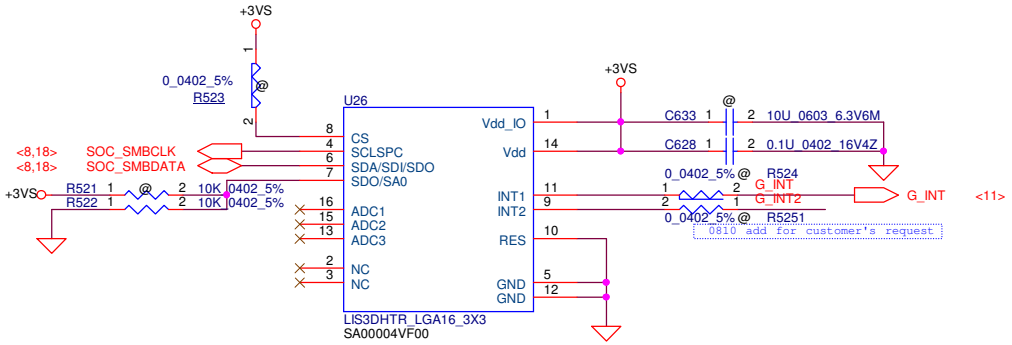
Compal Electronics, Inc.			
Title: HDMI CONN.			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 25 of 54		

HDD Board Conn





APS G-Sensor




```
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)
```

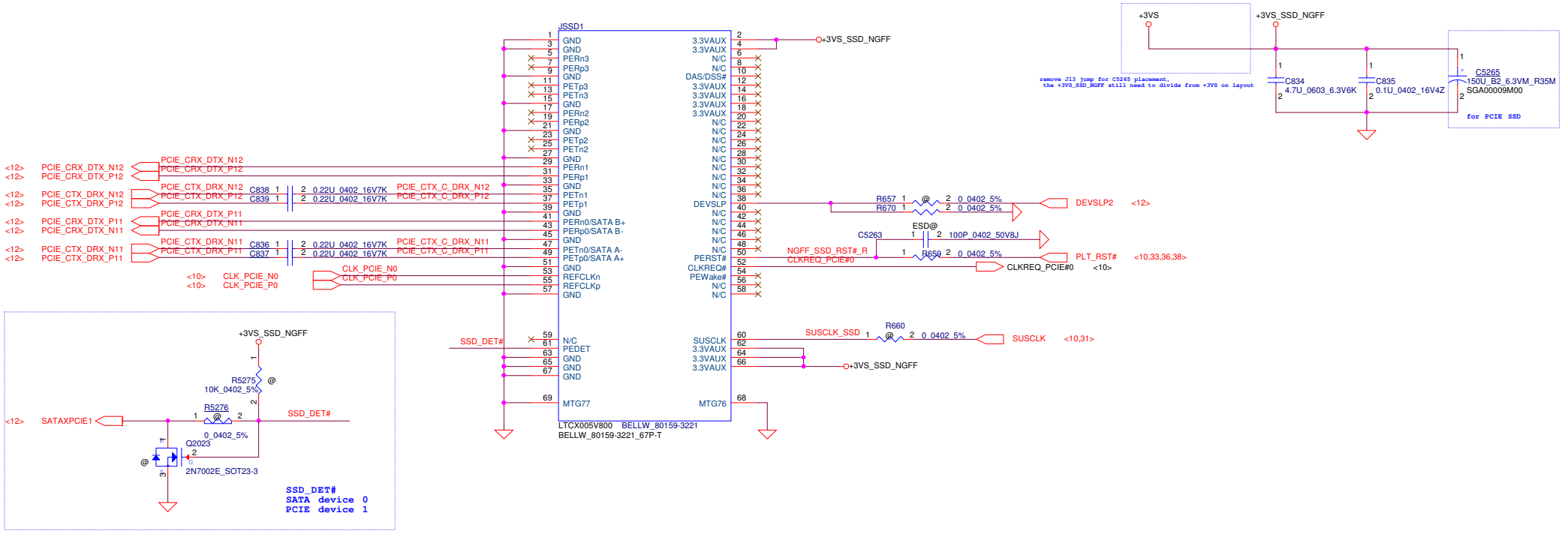
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

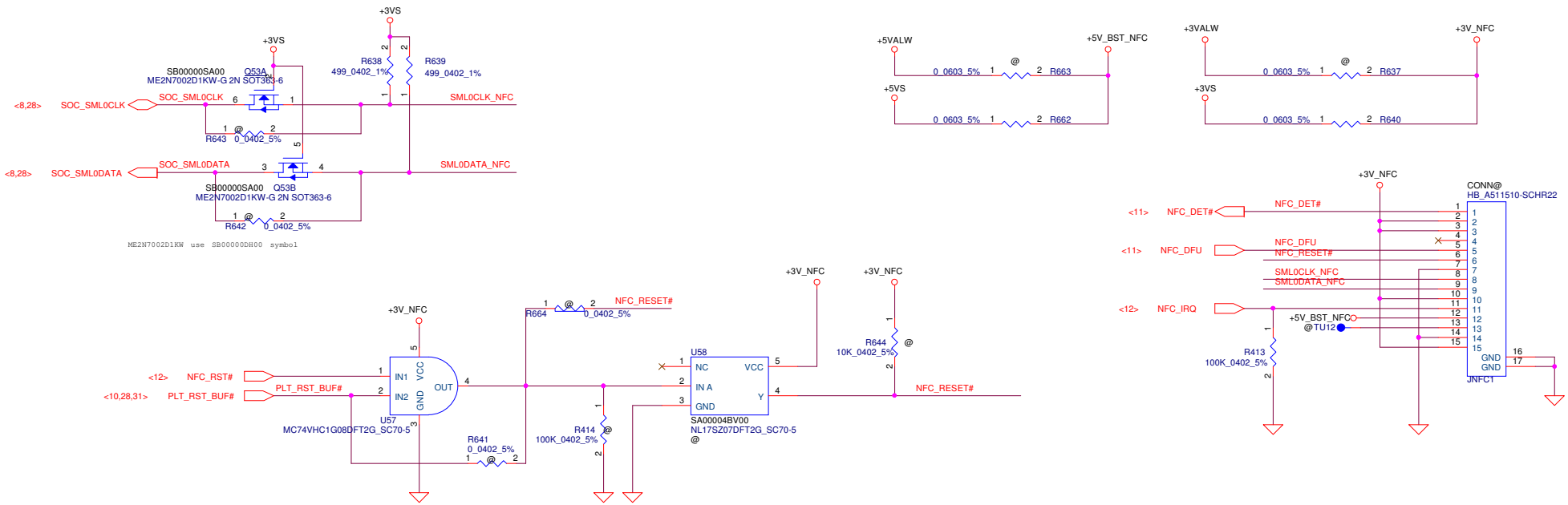
Compal Electronics, Inc.

Title: HDD & G-Sensor

Size	Document Number	Rev
Custom	LA-F241P	0.1

Date: Friday, June 09, 2017 Sheet 26 of 54





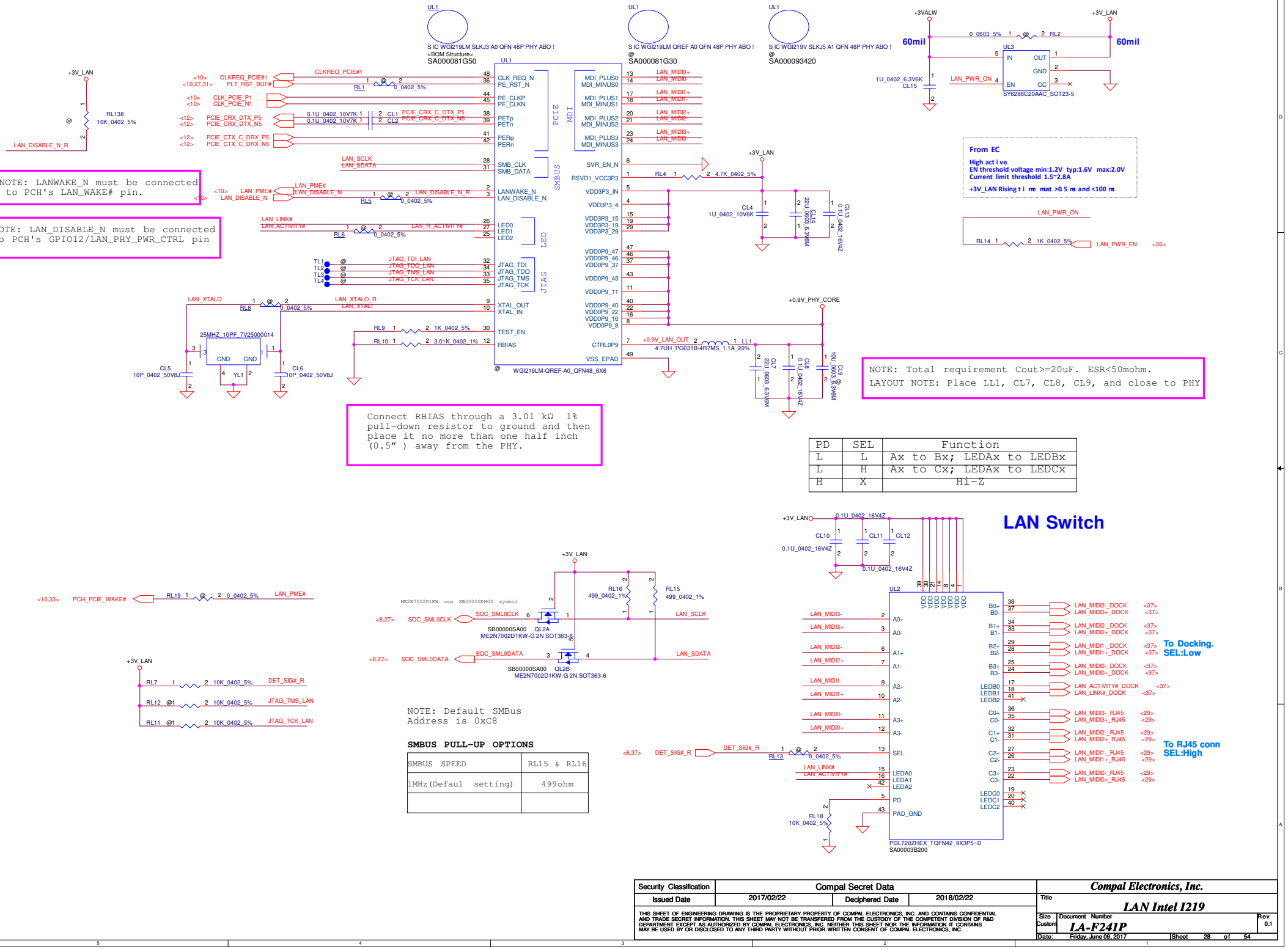
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **SSD & NFC**

Size	Document Number	Rev
Custom	LA-F241P	0.1

Date: Friday, June 09, 2017 Sheet 27 of 54



Security Classification	Compal Secret Data	
Issued Date	2017/02/22	Deciphered Date 2018/02/22

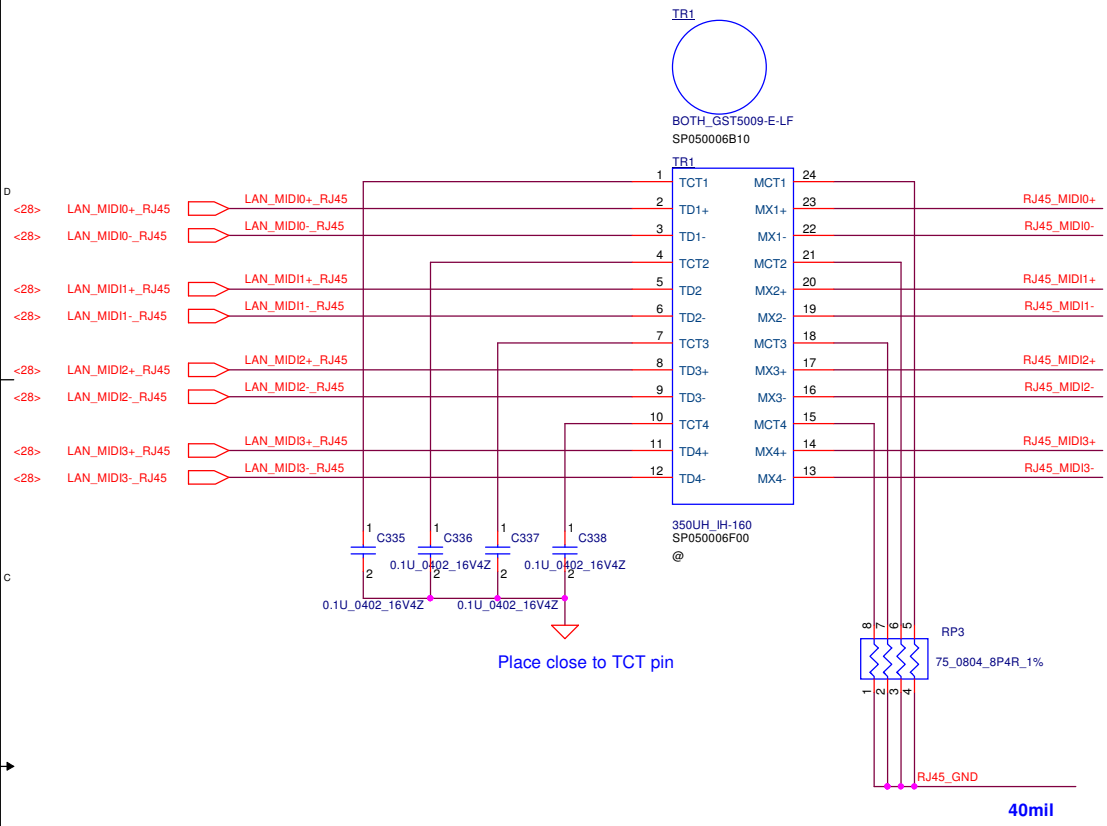
Compal Electronics, Inc.

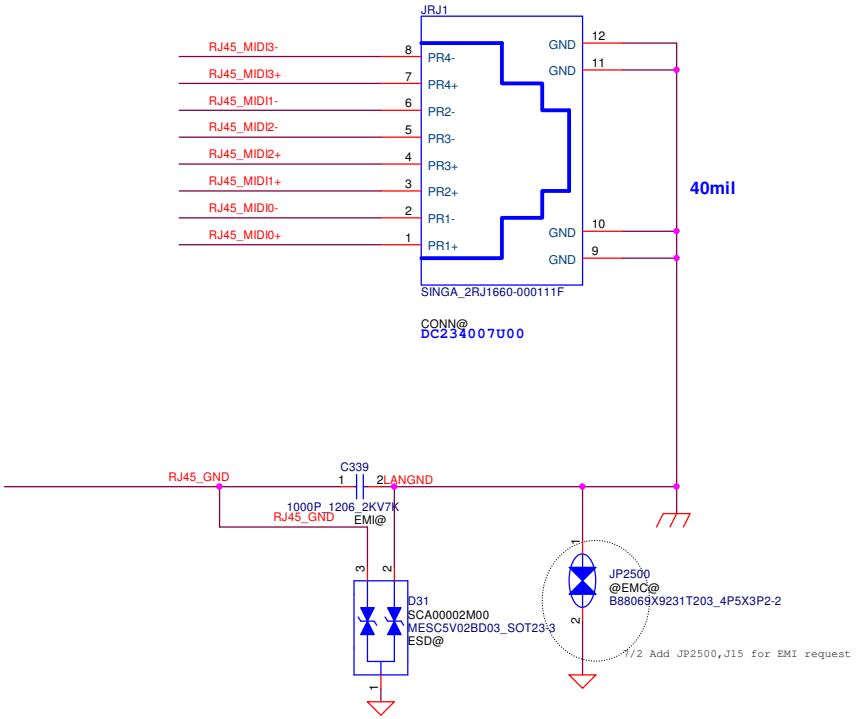
Title: LAN Intel I219

Size	Document Number	Rev
Custom	LA-F241P	0.1

Date: Friday, June 09, 2017 Sheet 28 of 54

LAN Connector





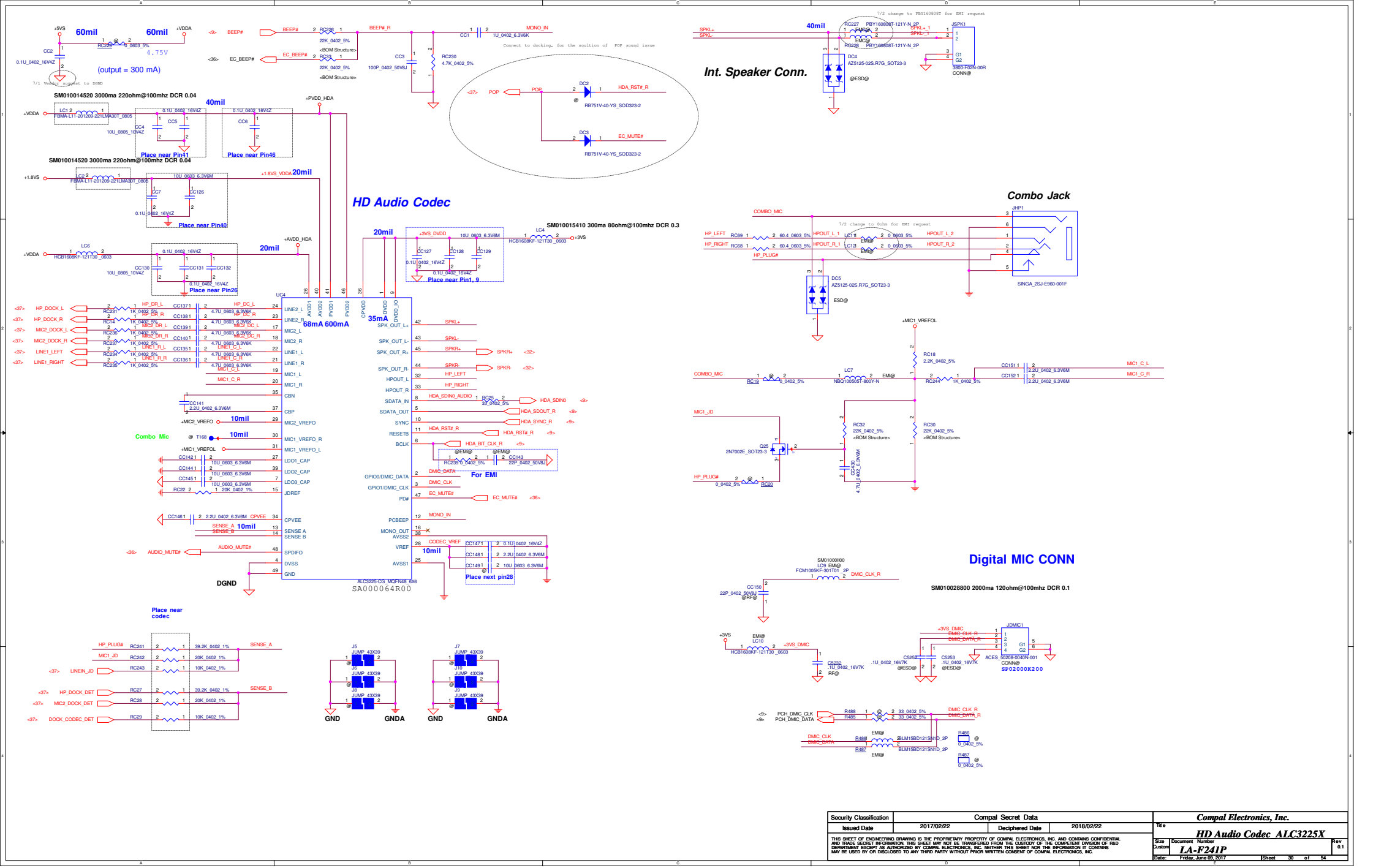
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **LAN Magnetic & RJ45**

Size	Document Number	Rev
Custom	LA-F241P	0.1

Date: Friday, June 09, 2017 Sheet 29 of 54

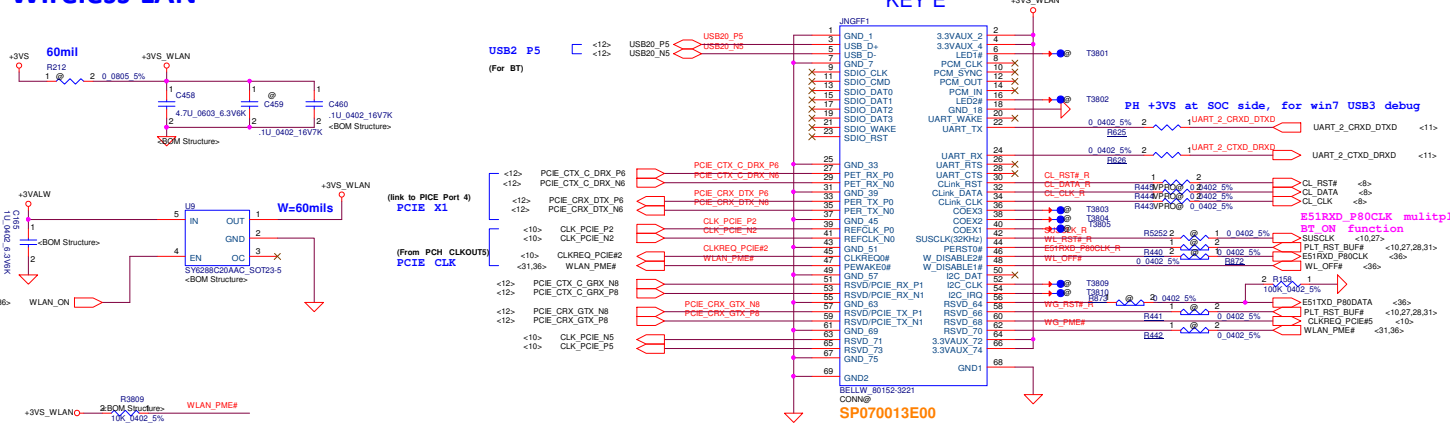


Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.			
Title: HD Audio Codec ALC3225X			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 30 of 54		

Wireless LAN

KEY E



NGFF WL+BT+WIGIG (KEY E)

WiGig/WLAN/BT Combo Host Pin Configuration

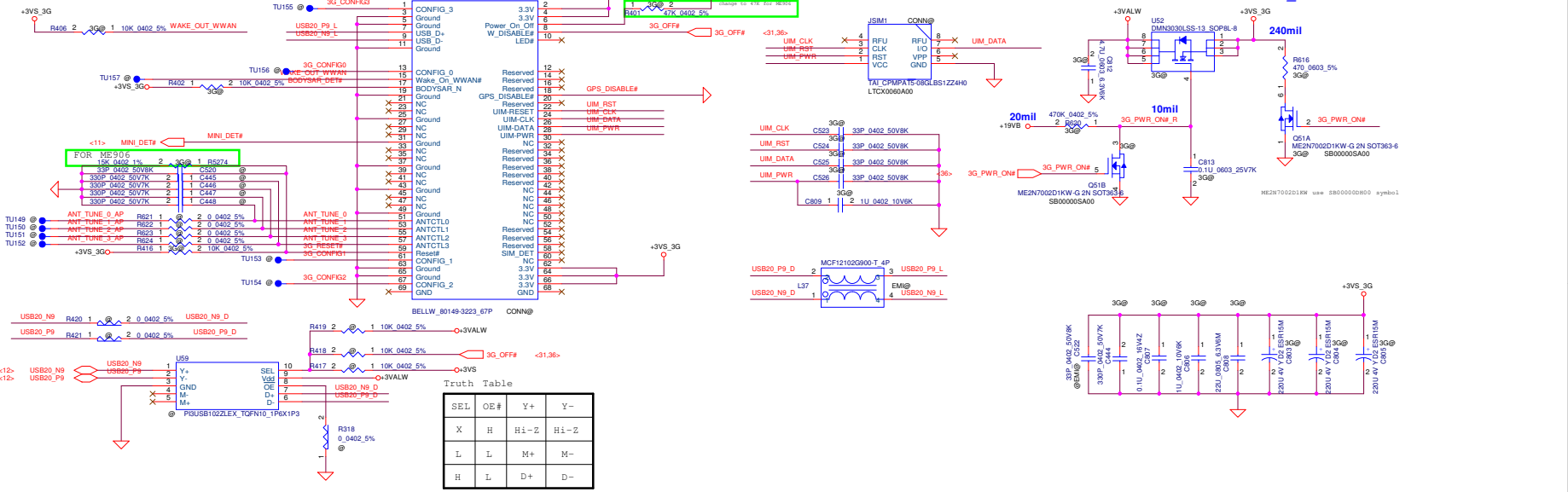
W0096	Pin#	Standard Definition	M.2 CONNECTOR	Standard Definition	Pin#	W0096
				GND	75	GND
VCC0_3V3	74	3.3V		REFCLKN1	73	11ac PE_REFCLKP
VCC0_3V3	72	3.3V		REFCLKP1	71	11ac PE_REFCLKN
11ad PE_WAKEN	70	PEWAKE1#		GND	69	GND
11ad PE_CLKREQN	68	CLKREQ1#		PETn1	67	11ac PE_TXN1
11ad PE_PERSTN	66	PERST1#		PETp1	65	11ac PE_TXP1
11ad_JTMS	64	Reserved		GND	63	GND
11ad_JTDI	62	ALERT#		PERn1	61	11ac PE_RXP0
11ad_JTDO	60	I2C CLK		PERp1	59	11ac PE_RXN0
11ad_JTCK	58	I2C DATA		GND	57	GND
EDGE_WDISABLEn1*	56	W_DISABLE1#		PEWAKE0#	55	11ac PE_WAKEN
EDGE_WDISABLEn2*	54	W_DISABLE2#		CLKREQ0#	53	11ac PE_CLKREQN
11ac_PE_PERSTN	52	PERST0#		GND	51	GND
SUSCLK	50	SUSCLK(32KHz)		REFCLKN0	49	11ac PE_REFCLKN
NC	48	COEX1		REFCLKP0	47	11ac PE_REFCLKP
NC	46	COEX2		GND	45	GND
NC	44	COEX3		PETn0	43	11ac PE_TXN
11ad PE_RXP1**	42	Reserved		PETp0	41	11ac PE_TXP
11ad PE_RXN1**	40	Reserved		GND	39	GND
GND	38	Reserved		PERn0	37	11ac PE_RXN
11ad PE_TXP1**	36	N/C		PERp0	35	11ac PE_RXP
11ad PE_TXN1**	34	N/C		GND	33	GND
GND	32	N/C		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		N/C	23	NC
11ad_JTRST	22	N/C		N/C	21	NC
NC	20	N/C		N/C	19	NC
GND	18	GND		N/C	17	NC
EDGE_LED2*	16	LED2#		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		NOTCH		NOTCH
NOTCH		NOTCH		GND	7	GND
EDGE_LED1*	6	LED1#		USB_D-	5	11ac USB_DNEG
VCC0_3V3	4	3.3V		USB_D+	3	11ac USB_DPOS
VCC0_3V3	2	3.3V		GND	1	GND

M.2 CONNECTOR

3.1.8.1.3.1.7.1. UART Wakeup

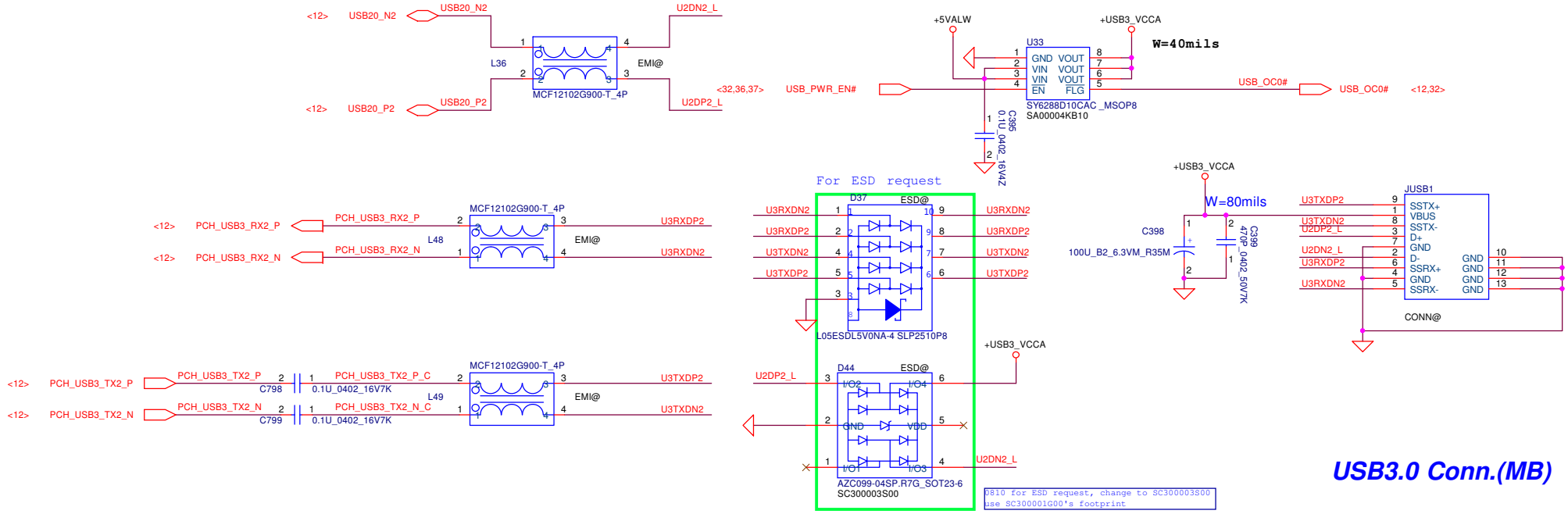
The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RDX~~ UART_RXD (Input): Receive Data
- ~~RTX~~ UART_TXD (Output): Transmit Data
- UART_RTS (Input): Request to Send (Host Flow Control)
- UART_CTS (Output): Clear to Send (Device Flow Control)
- ~~Host_Wake_Up~~UART_Wake# (Output): Host wake-up line is optional in the case the host support in band wake-up



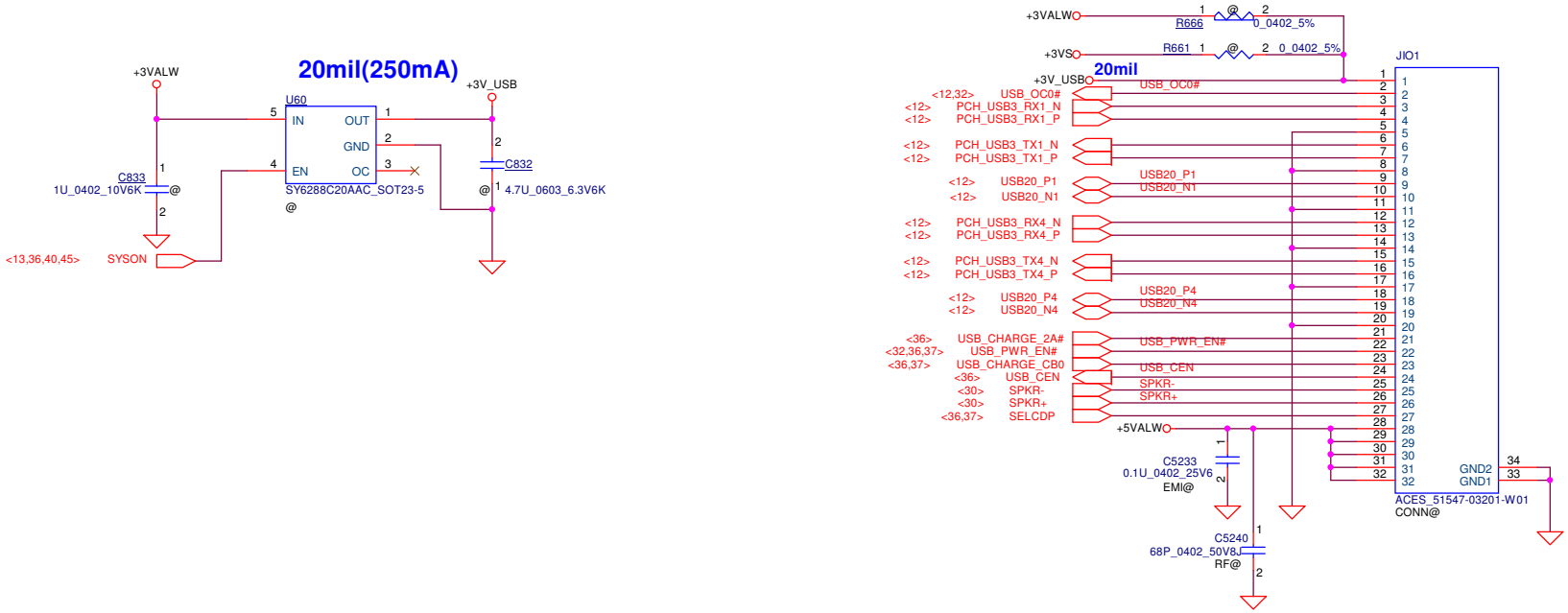
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.			
Title: mini Card & LTE CONN.			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 31 of 54		



USB3.0 Conn.(MB)

IO Board Conn(For FFC,FPC)



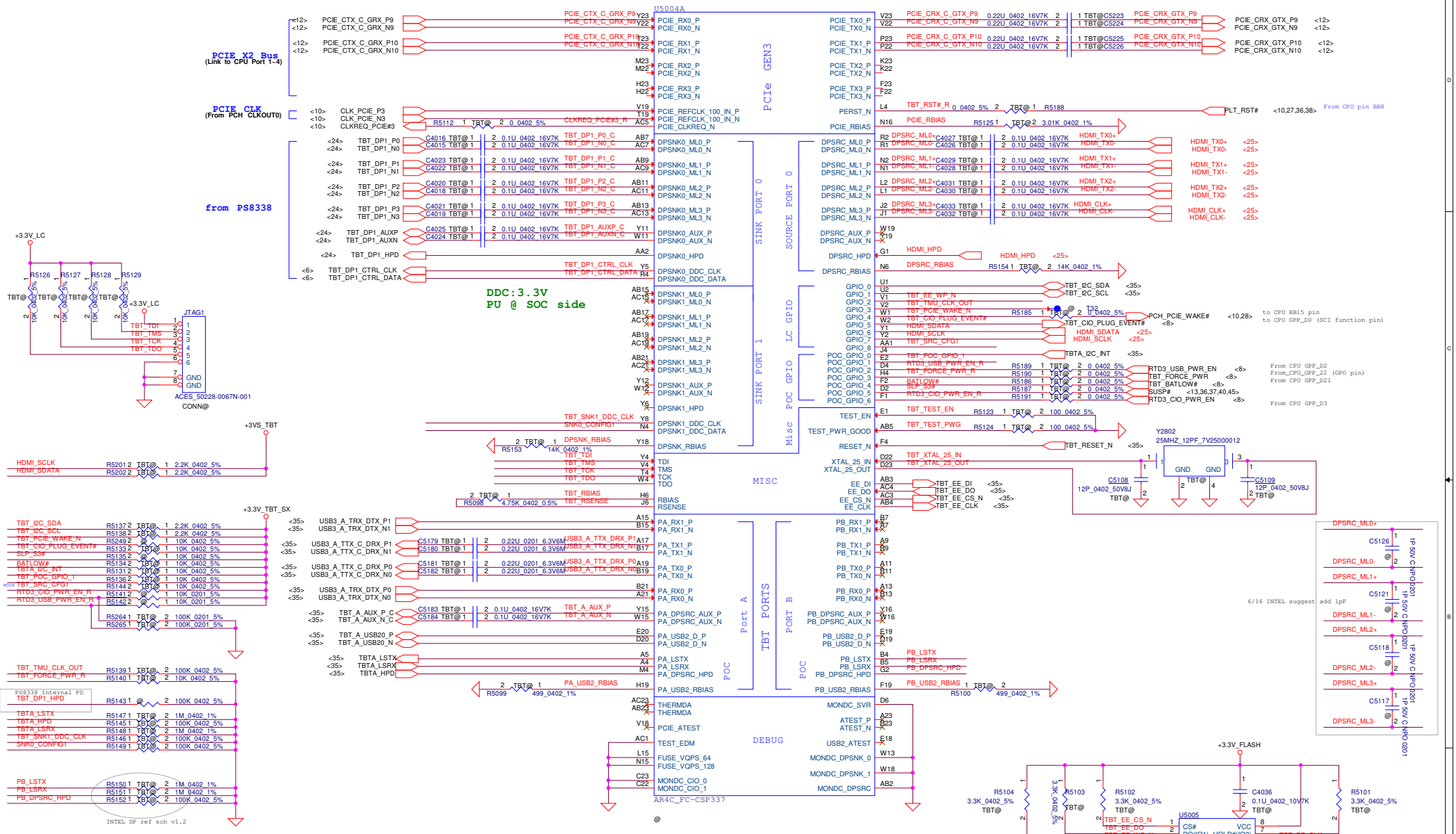
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: USB3.0 & IO/B

Size	Document Number	Rev
Custom	LA-F241P	0.1

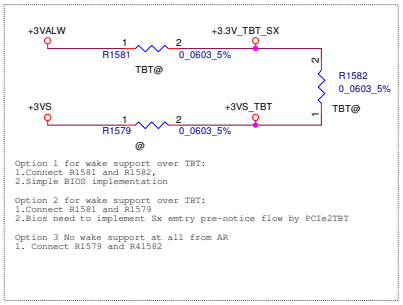
Date: Friday, June 09, 2017 Sheet 32 of 54



For BAD40_SL	For P6 EVT	For P6 PVT
U5004	U5004	U5004
S IC DSL6340 SLL3Z B1 THUNDERBOLT ABO ! @ SA000090N80	S IC JHL6340 QT5T C1 FCCSP THUNDERBOLT @ SA00009YL60	S IC JHL6340 SLLSQ C1 THUNDERBOLT ABO! TBT@ SA00009YL70

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.			
Title: Alpine Ridge			
Size: Custom	Document Number: LA-F241P		Rev: 0.1
Date: Friday, June 09, 2017	Sheet 33 of 54		



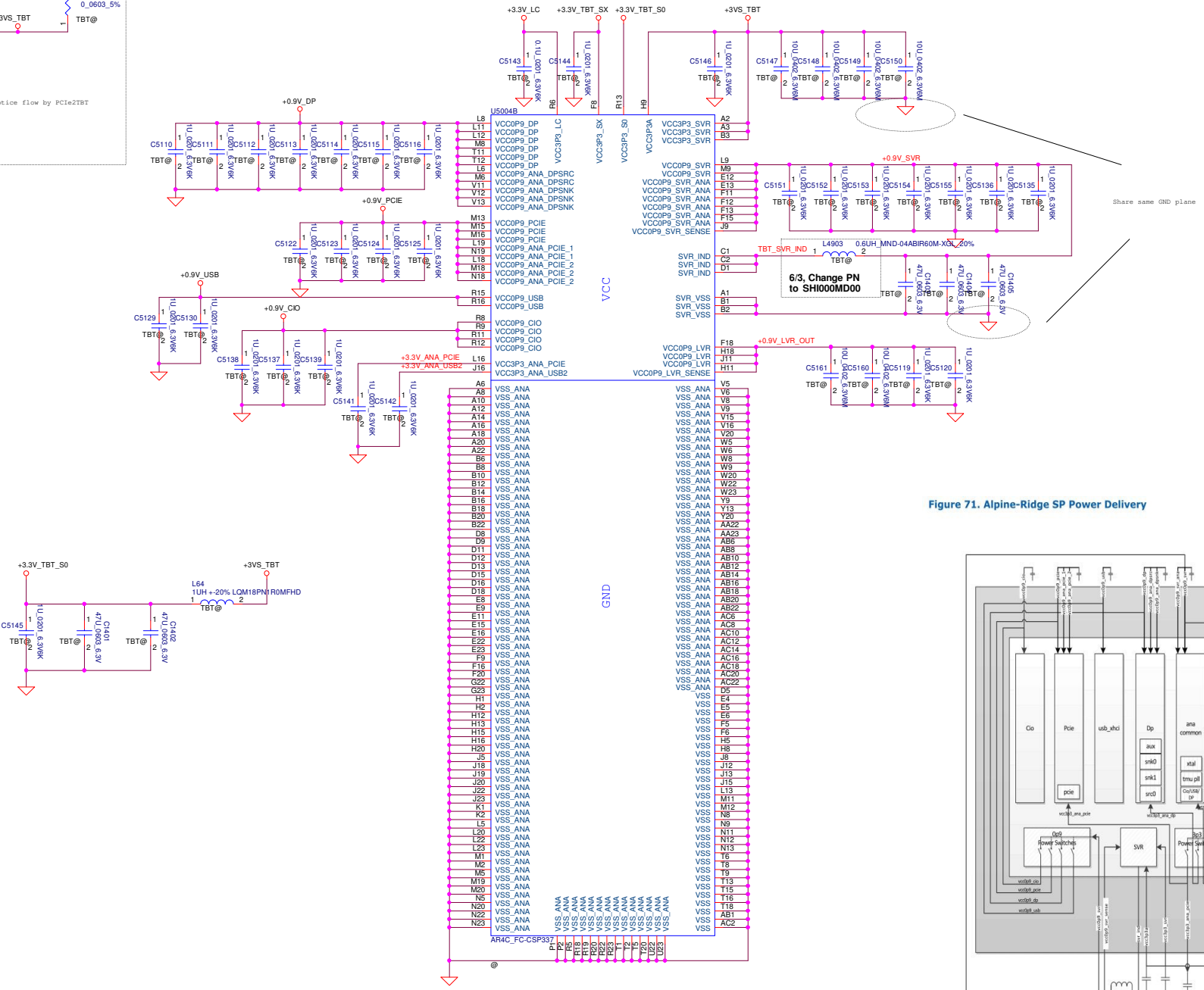
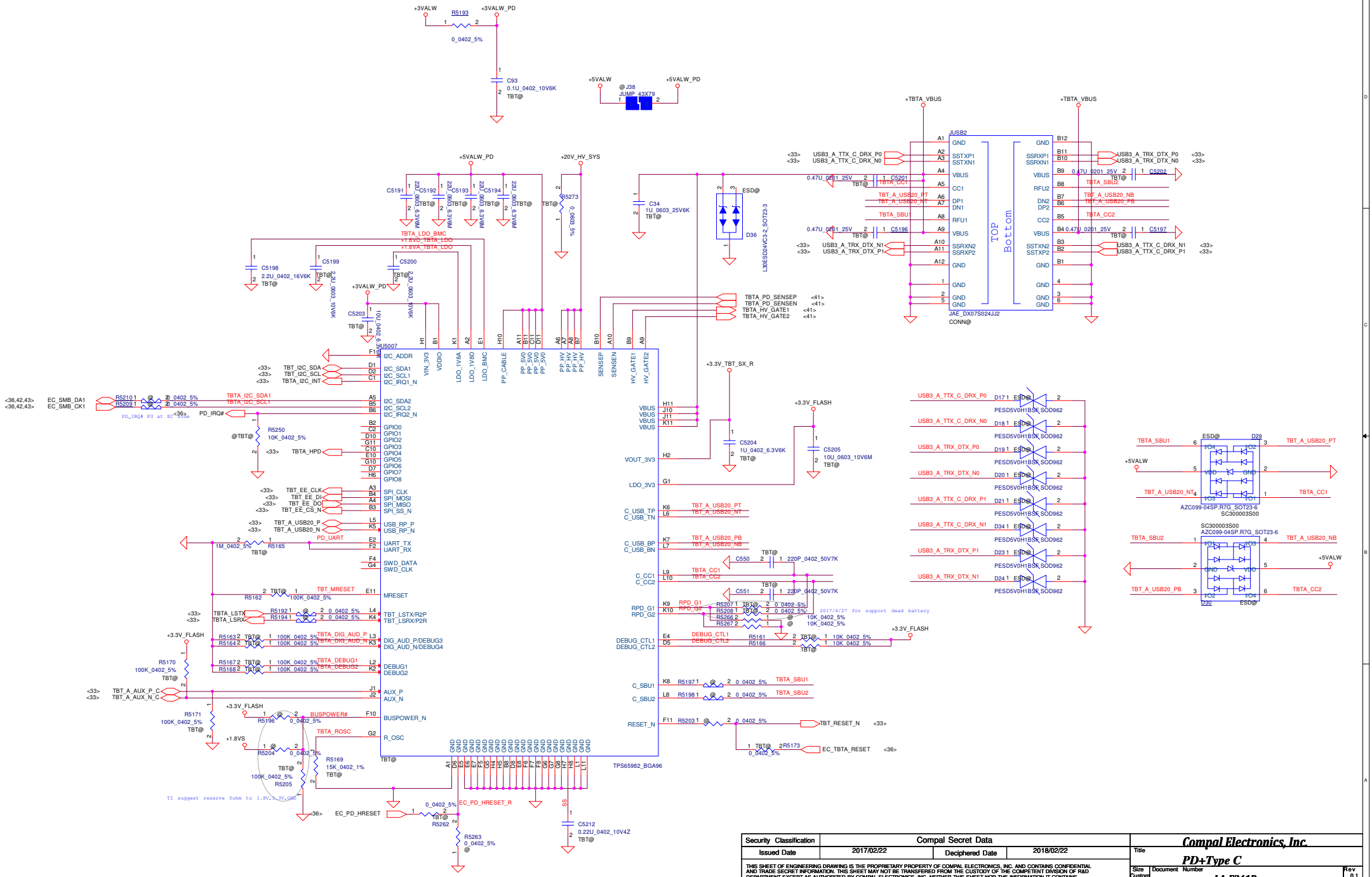


Figure 71. Alpine-Ridge SP Power Delivery

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Title	Compal Electronics, Inc.		
	Alpine Ridge-POWER		
Size	Document Number		Rev
Custom	LA-F241P		0.1
Date:	Friday, June 09, 2017	Sheet	34 of 54



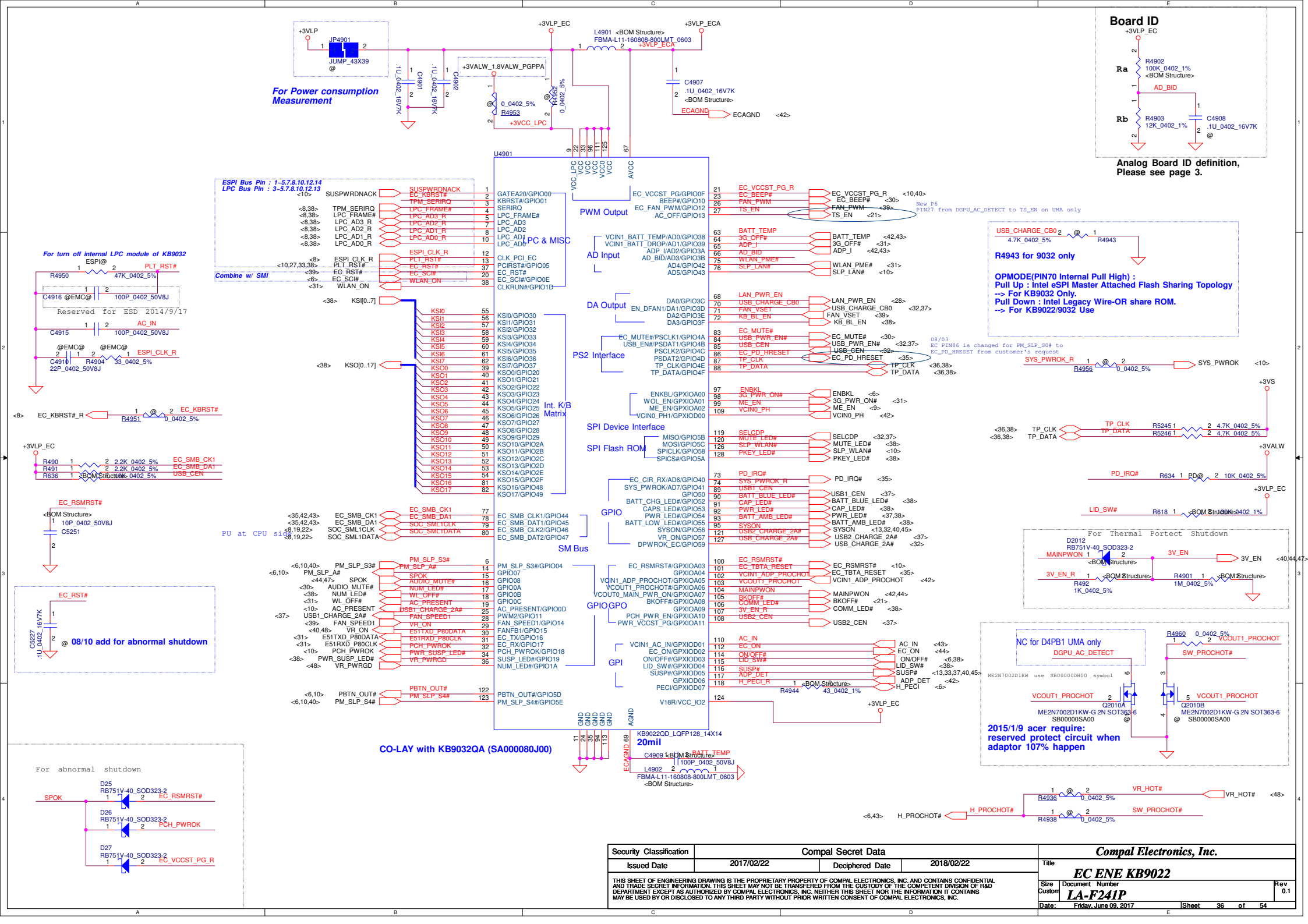
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **PD+Type C**

Size	Document Number	Rev
Custom	LA-F241P	0.1

Date: Friday, June 09, 2017 | Sheet 35 of 54



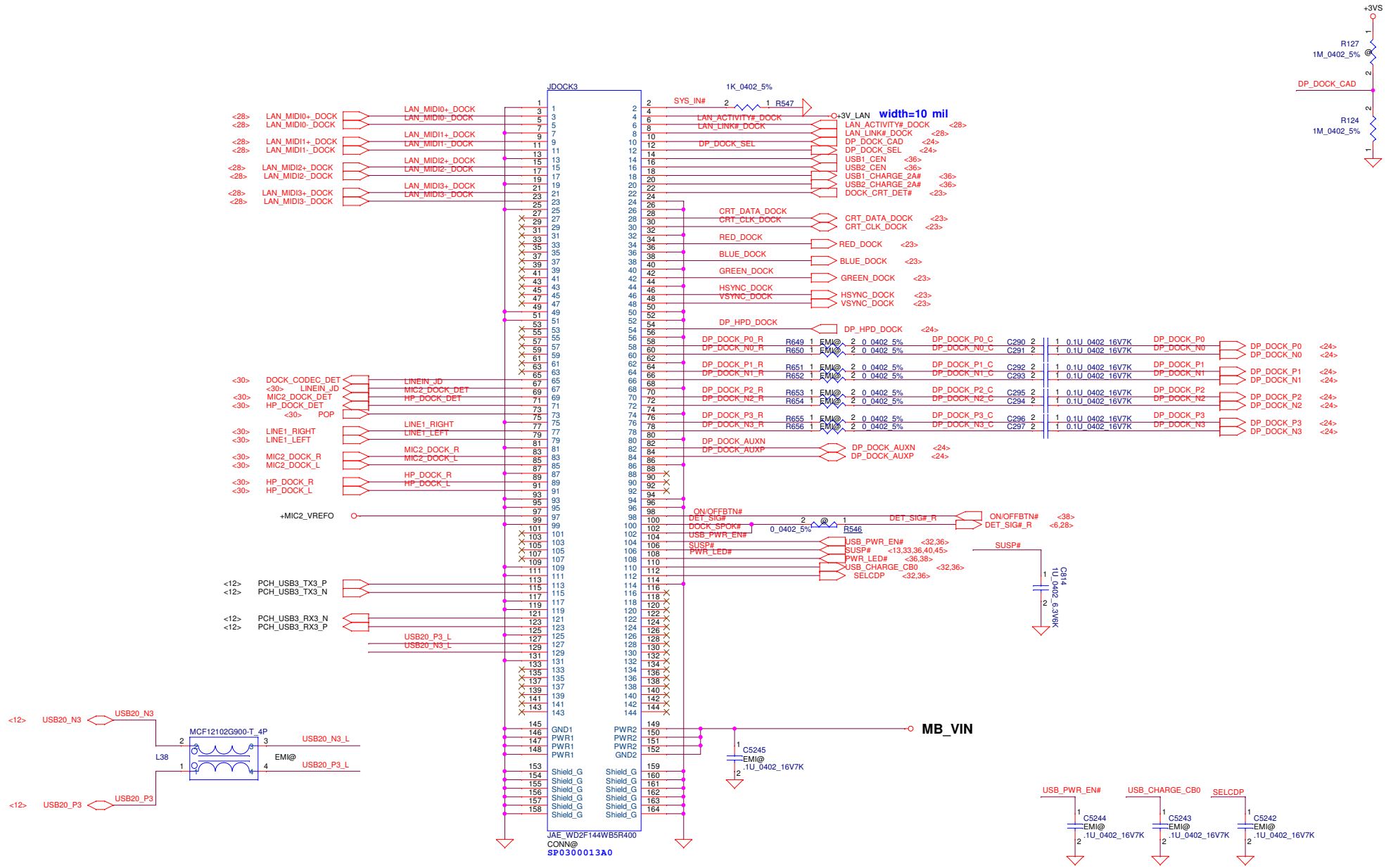
Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: EC ENE KB9022

Size: Custom | Document Number: LA-F241P | Rev: 0.1

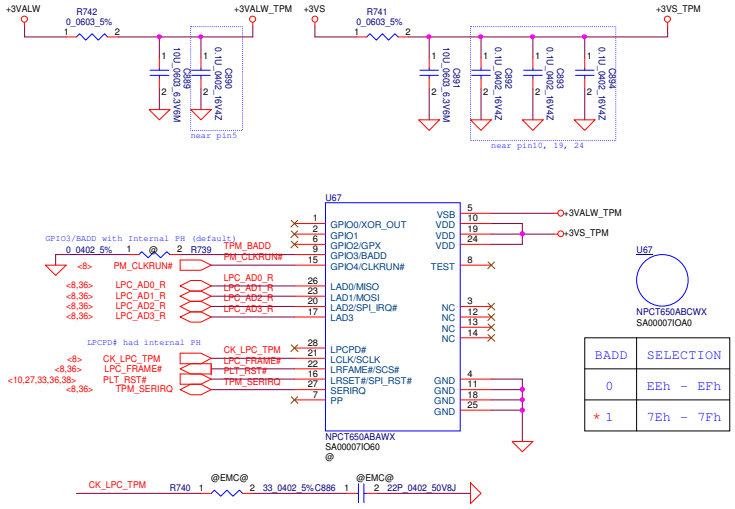
Date: Friday, June 09, 2017 | Sheet 36 of 54



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

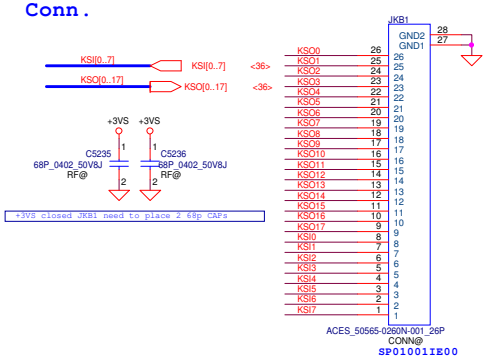
Compal Electronics, Inc.	
Title	E Series Dcok CONN.
Size: Custom	Document Number: LA-F241P
Rev	0.1
Date: Friday, June 09, 2017	Sheet 37 of 54

TPM

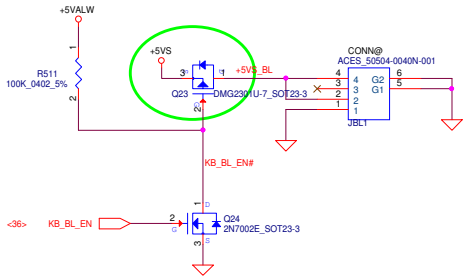


BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

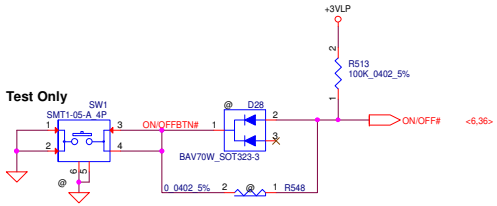
KB Conn.



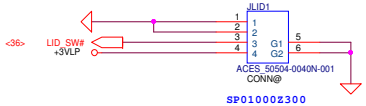
KB Backlight Conn



ON/OFF BTN

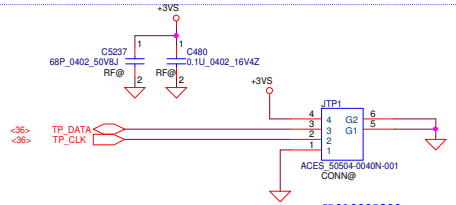


Lid Switch/B
(Hall Effect Switch)

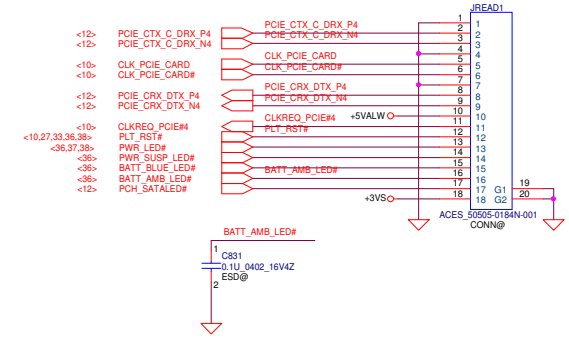


07/26 Add

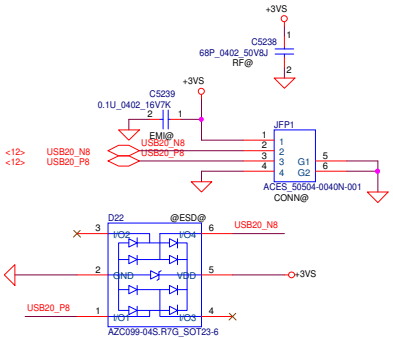
TP Conn.



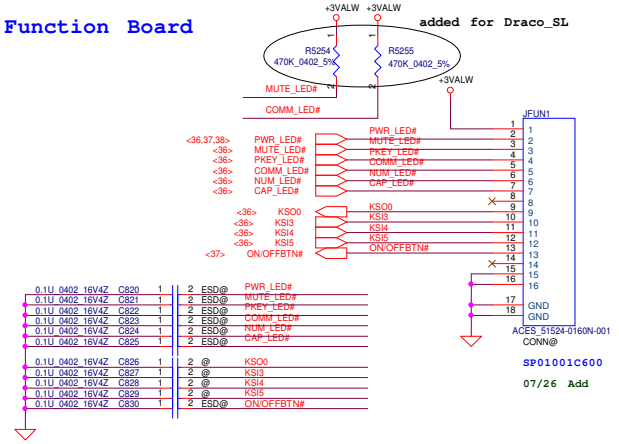
CardReader Board



FP Board



Function Board



07/26 Add

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: KB/TP/LID/TPM/FUN/FP/CARD

Size	Document Number	Rev
C	LA-F241P	0.1

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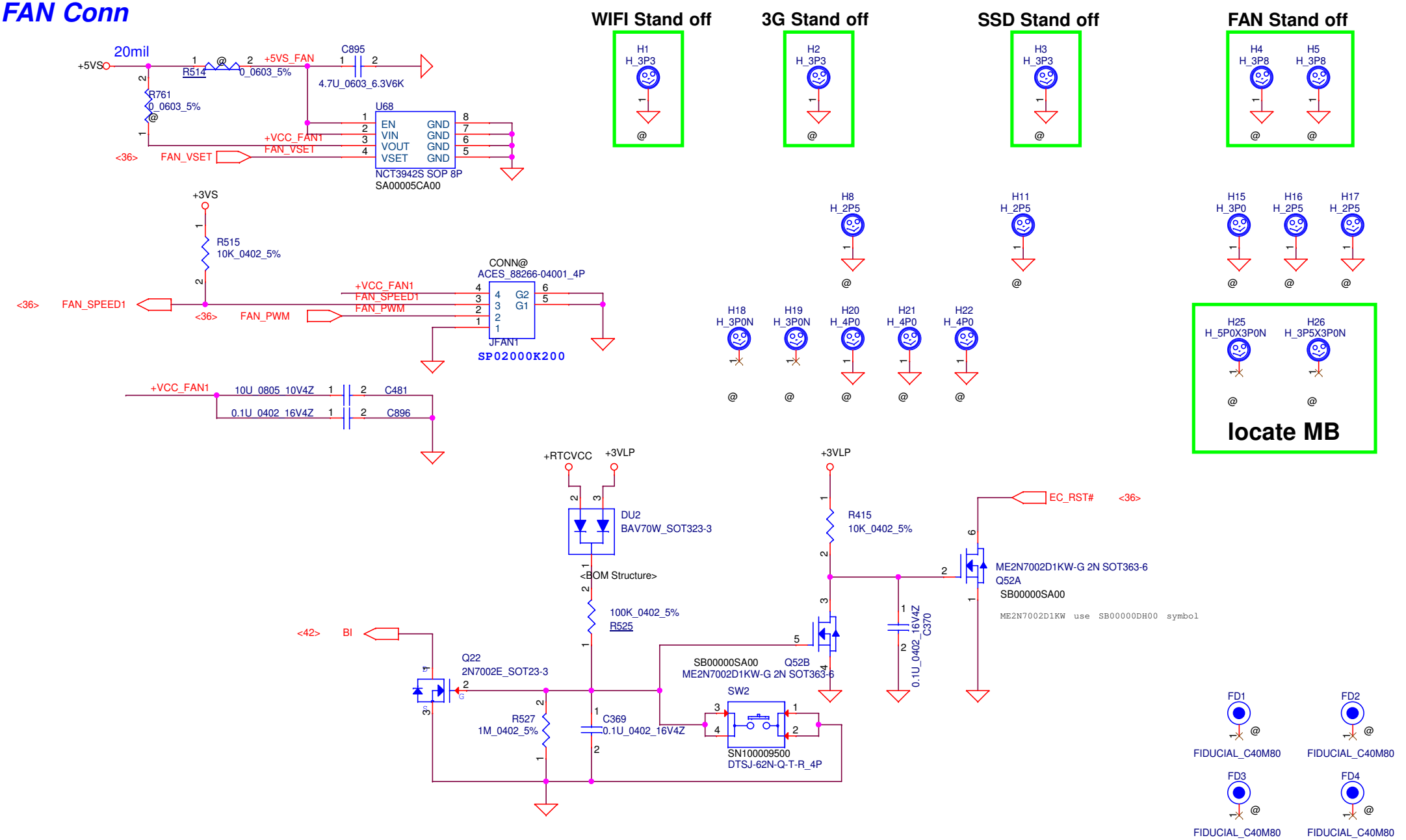
FAN Conn



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: **FAN & Screw**

Size	Document Number	Rev
Custom	LA-F241P	0.1

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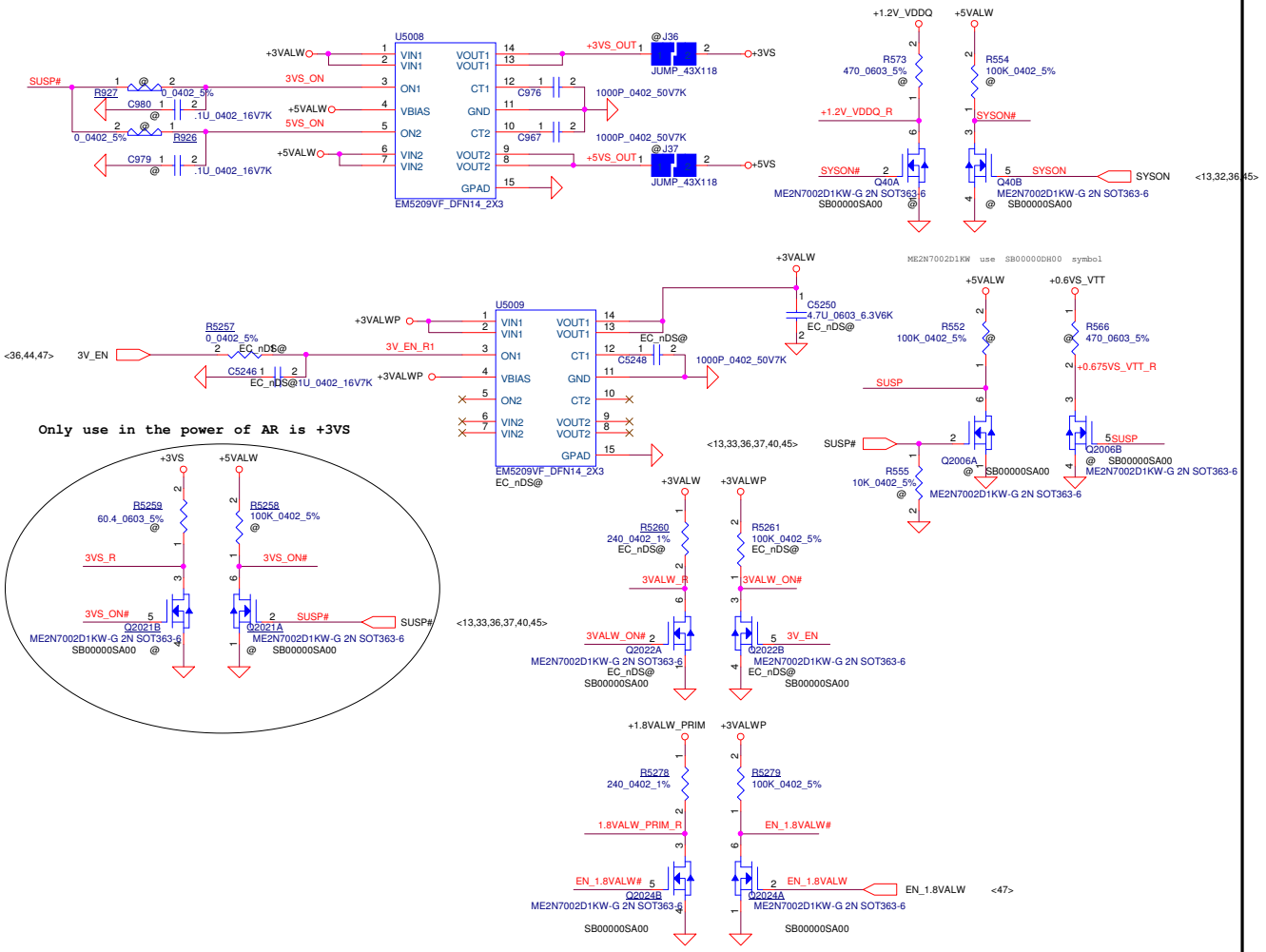
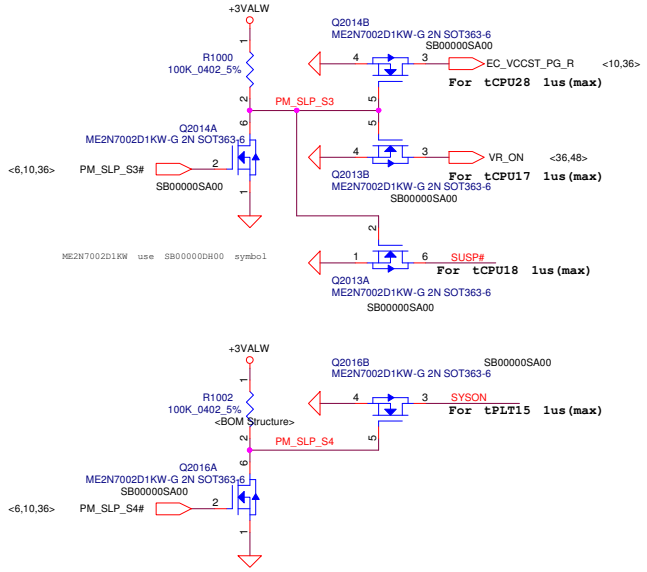
DC & VGA Interface

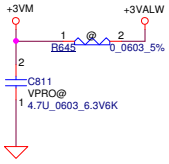


For Power Of f Sequence



+3VALW to +3VM for Intel AMT

20mil(68mA)



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-F241P	0.1

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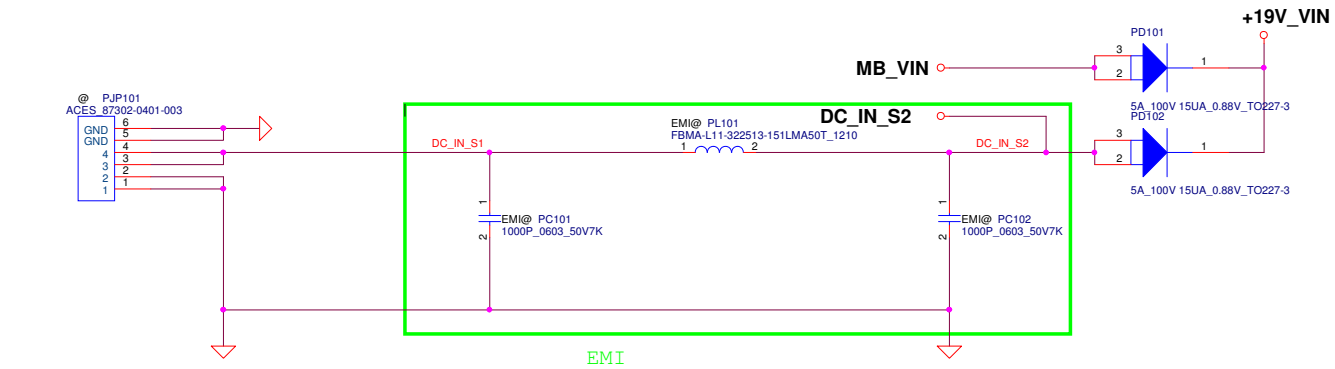
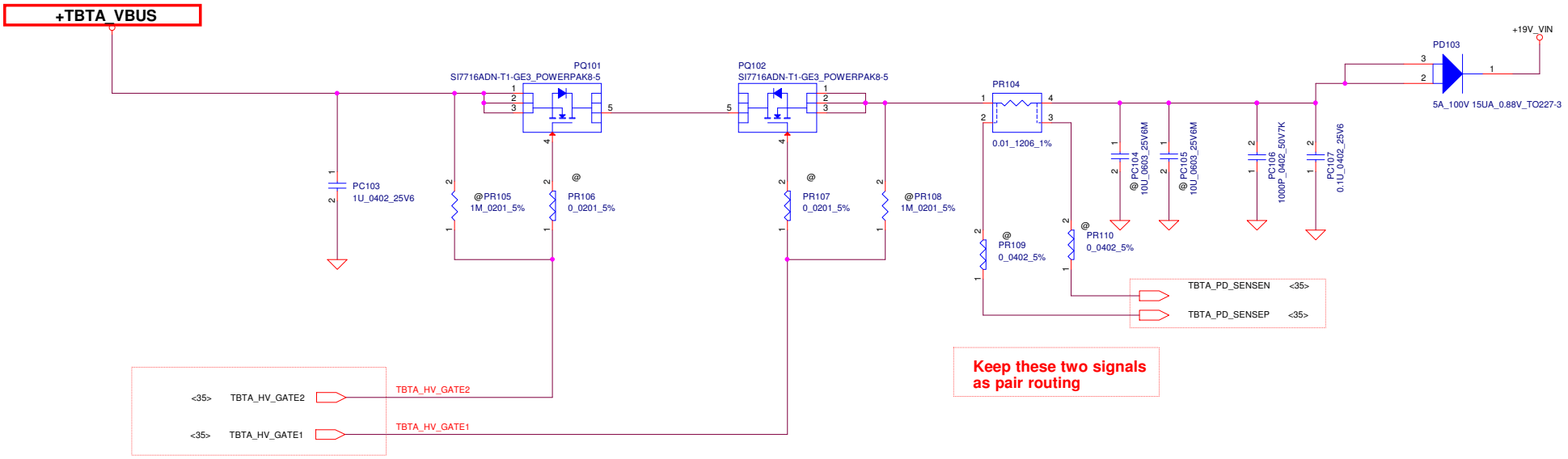
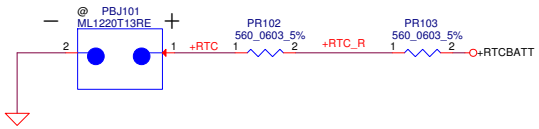
2015/7/8
PD101 and PD102 SCS00002F00 change to SCS00002M00





Keep these two signals as pair routing



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	LA-F241P	0.1

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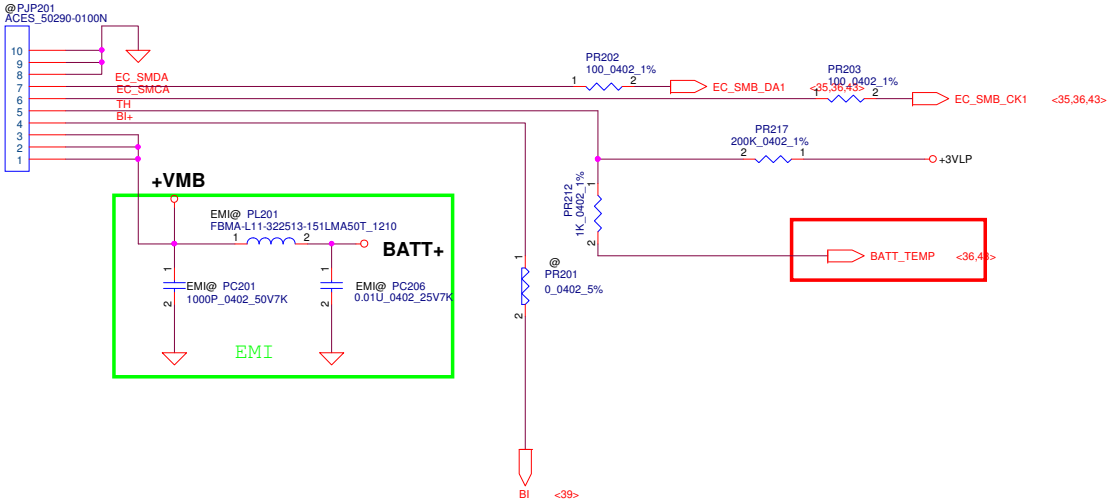
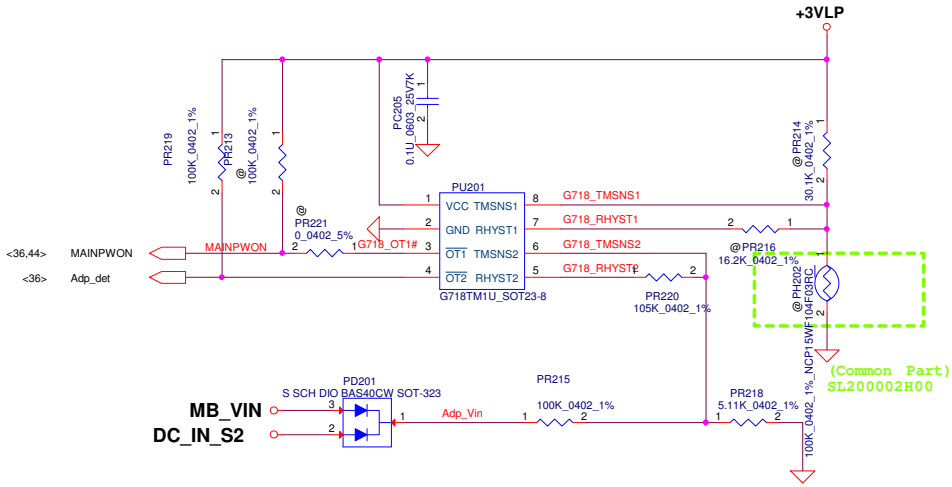
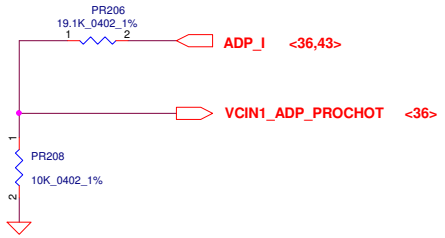


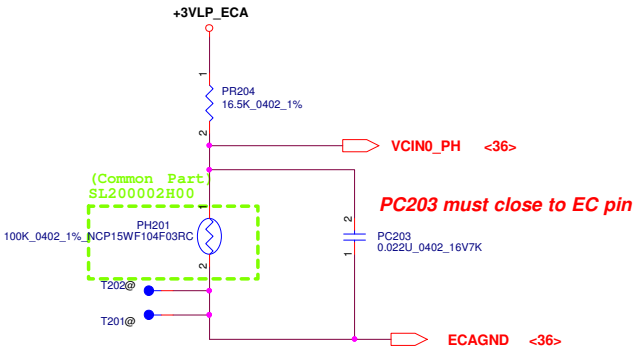


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

2015/07/09 update

For KB9022 sense 20mΩ	Active	Recovery
65W For AC IN	84.5W,0.61V	84.5W,0.61V
45W For PD IN	58.5W,0.40V	58.5W,0.40V



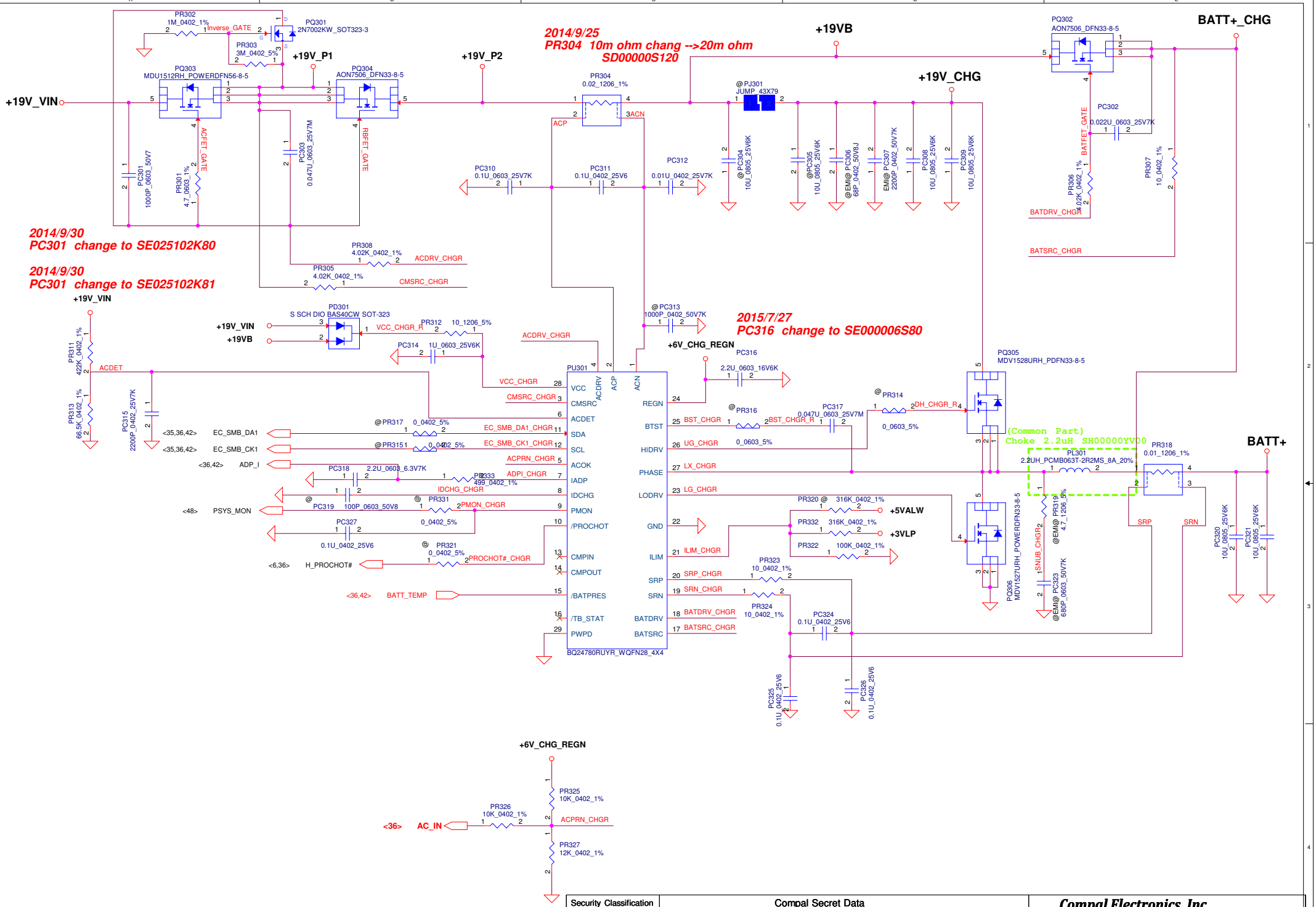


PC203 must close to EC pin

T202 T201 must close to PH201

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.	
Title	PWR-BATTERY CONN/OTP
Size: Custom	Document Number: LA-F241P
Rev	0.1
Date: Friday, June 09, 2017	Sheet 42 of 54



Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: BQ24780

Size	Document Number	Rev
Custom	LA-F241P	0.1

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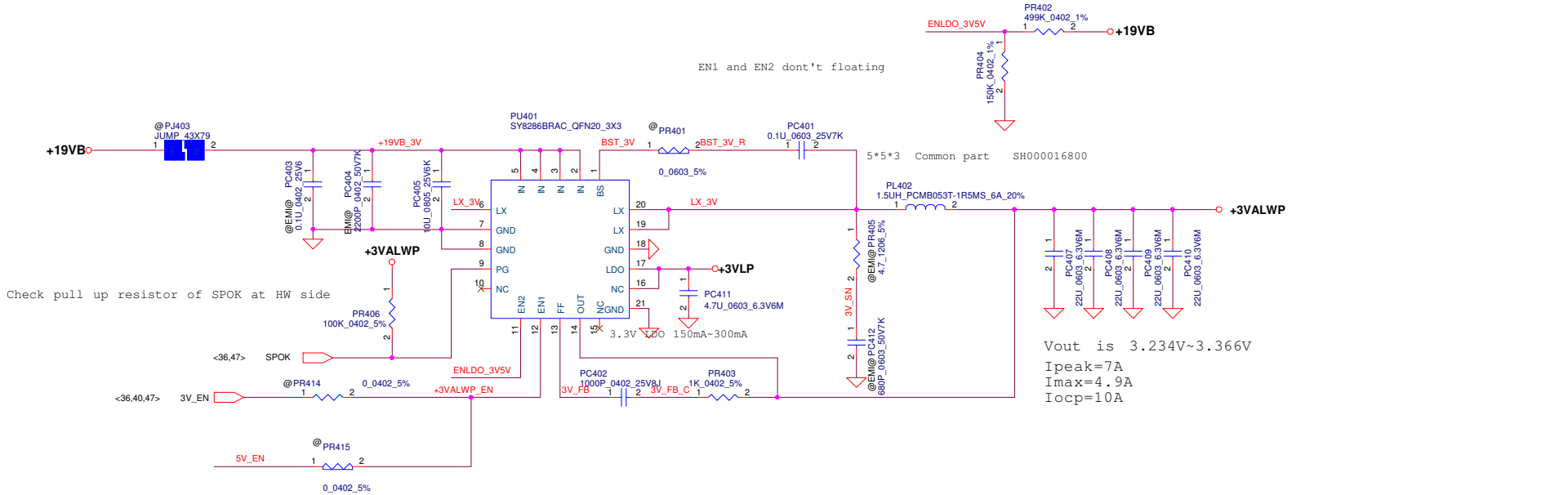

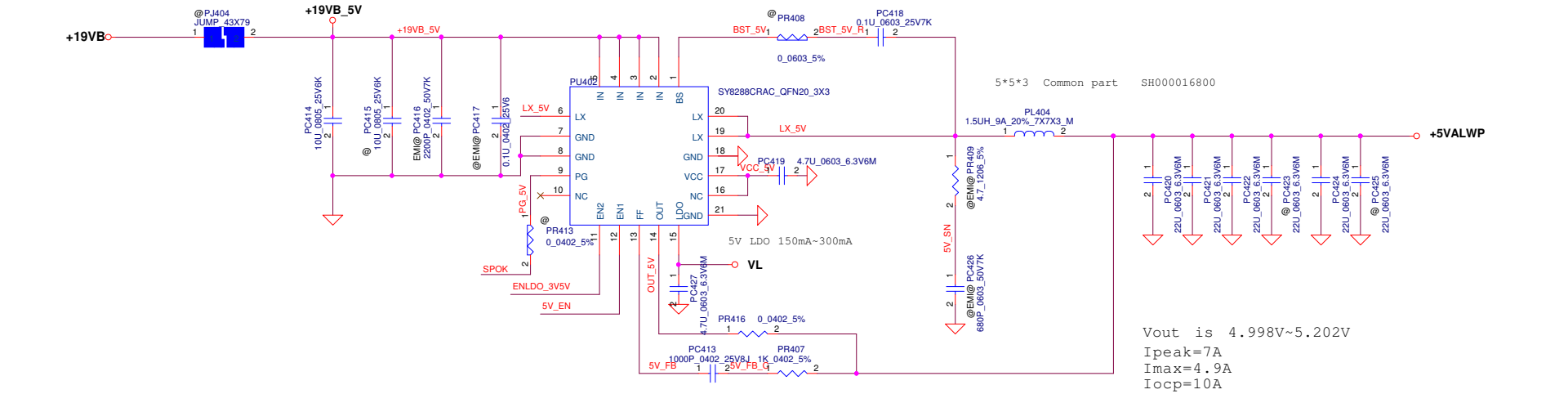

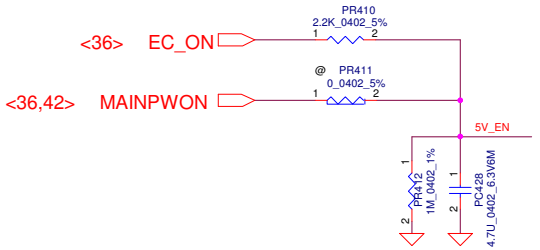

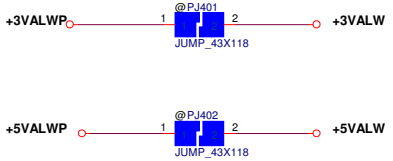

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA-F241P	0.1

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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question, you can change from +1.2VP to +1.2VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Choke 1.5uH SH000016700
Common Part 7*7*3

Update Pc510 change to Common Part SF000006S00 20141227

Change PR503 to 17.8K ohm
OCP setting 9.6A

change PQ502 form 7506 to 7716, 20150108

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(6.19/10))
=1.2V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 23.2mohm(Typ), 27.8mohm(Max)
Idsm: 10.1A@Ta=25C, 8.1A@Ta=70C

L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~9.6A
OVP: 110%~120%
VFB=0.75V, Vout=1.2V
MOSFET footprint: SIS412DN

3.8x3.8xH1.8
DCR: 20~25mohm
Idc / Isat: 3.8A

Iocp : 3.7A
FSW : 1MHz

Rdown

5/29 add PC526
In order to avoid capacitor decay

Vout=0.6V* (1+Rup/Rdown)
2.504V= 0.6V*(1+36.5K/11.5K)

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

Size	Document Number	Rev
Custom	LA-F241P	0.1

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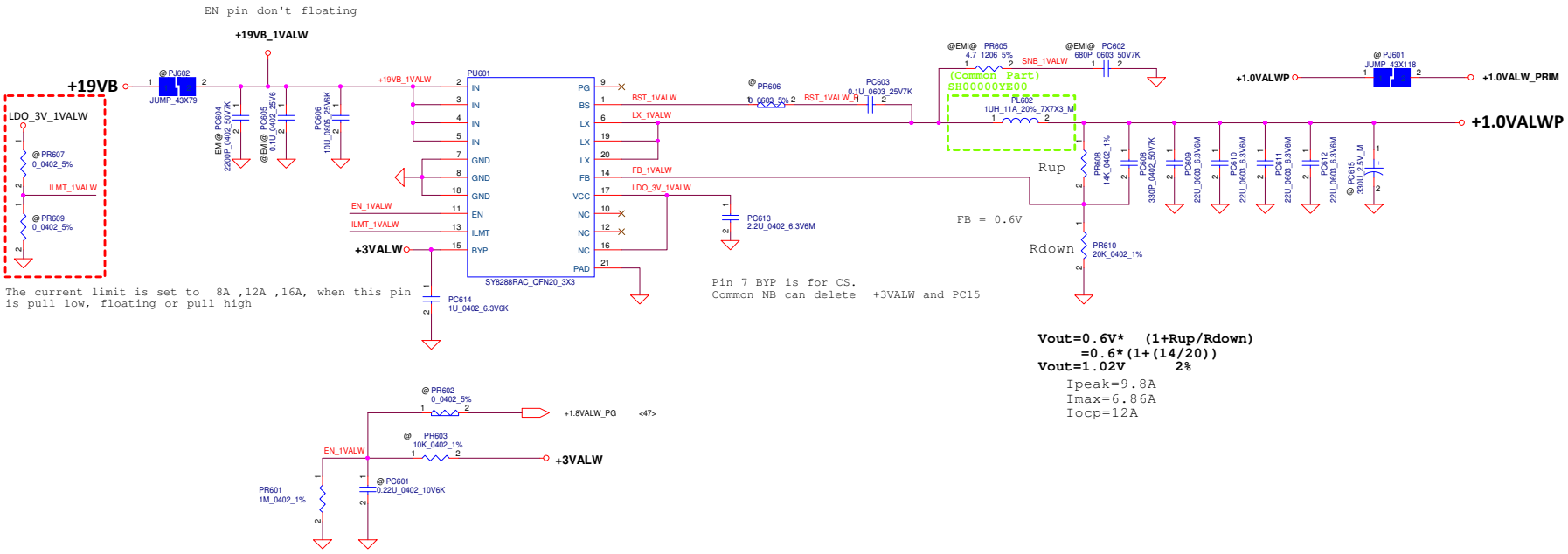


Compal Electronics, Inc.

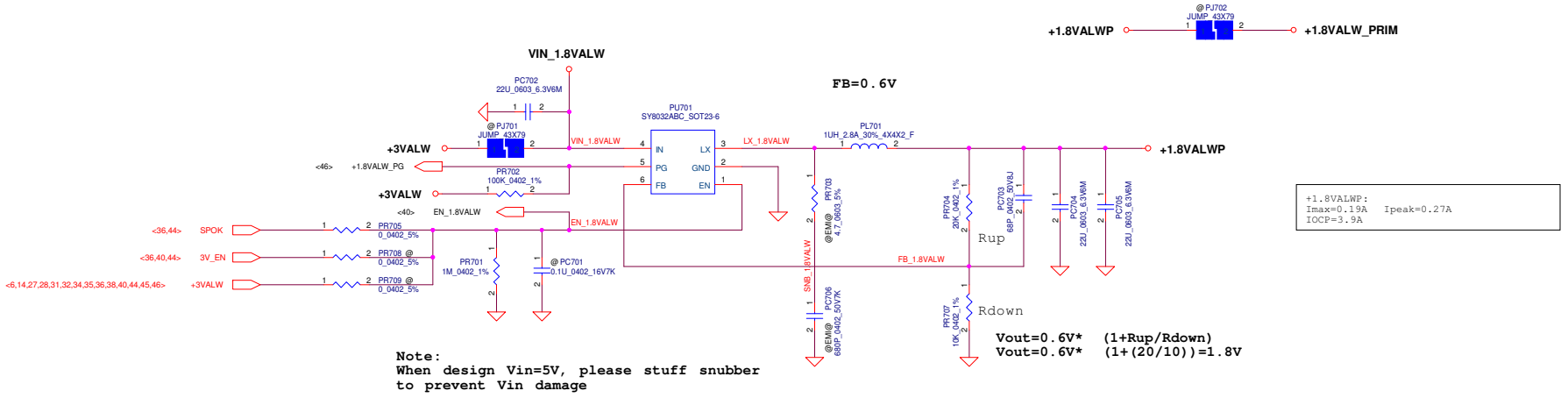
Title: +1.0VALWP

Size	Document Number	Rev
C	LA-F241P	0.1

Date: Friday, June 09, 2017 Sheet 46 of 54

Module model information

SY8032_V2.mdd



Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	LA-F241P	0.1

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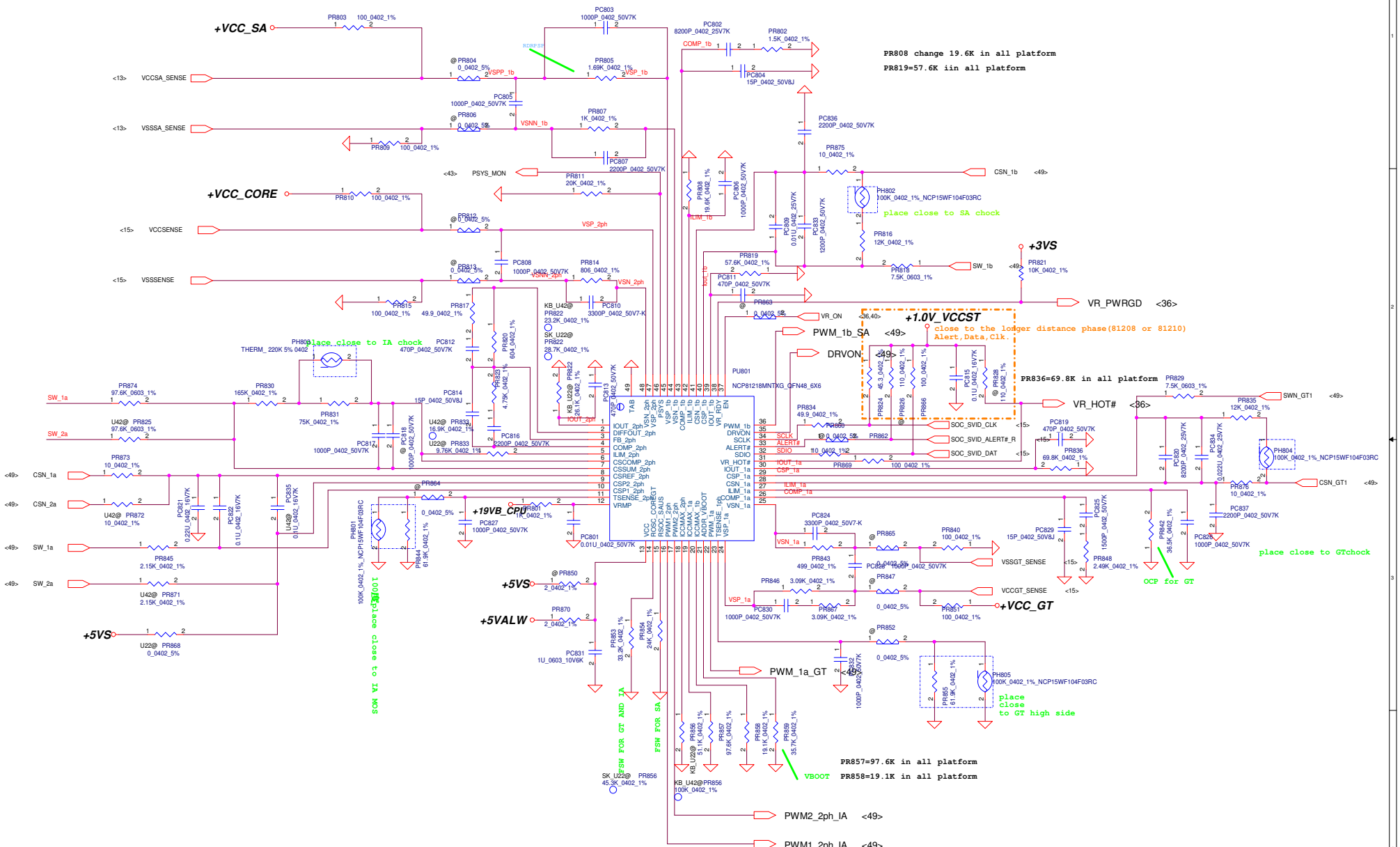

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.	
Title	IMVP8, NCP81206
Size	C
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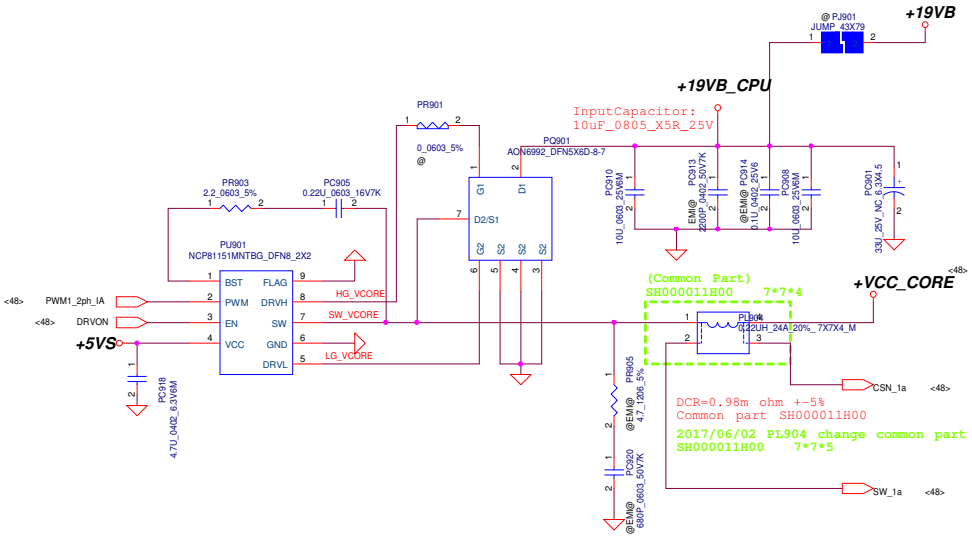
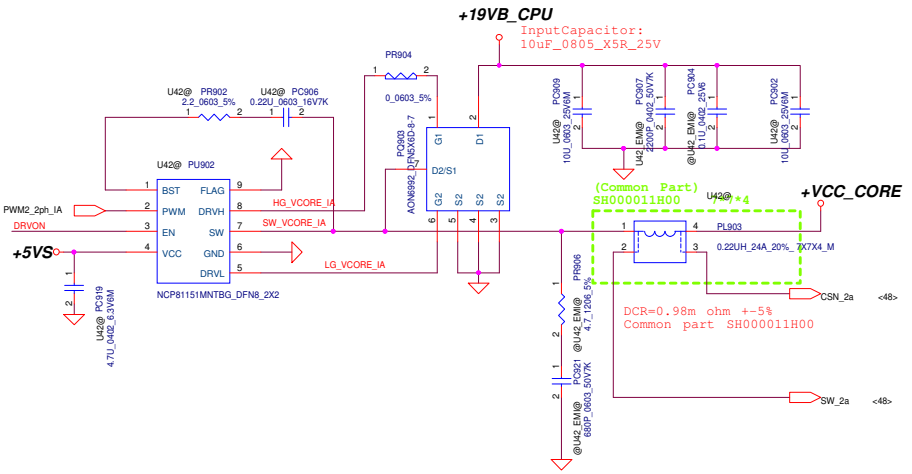
change PL9002, PL9003
SM01000C000 to comm
part SM01000P200



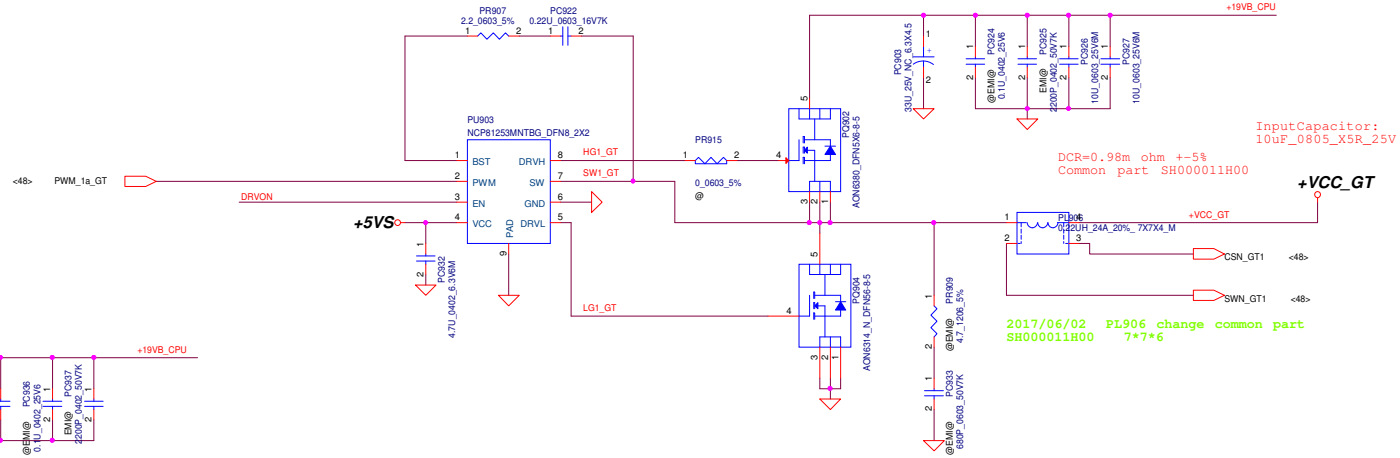


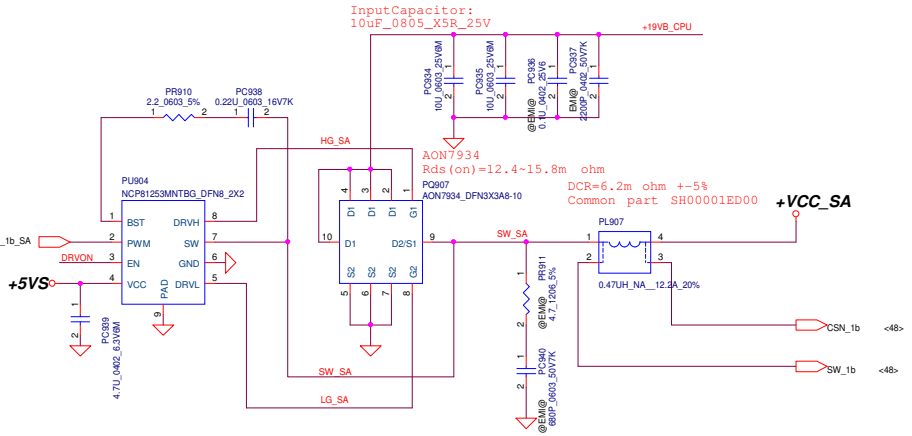
U22
VCC:
Imax=21A Ipeak=32A Iocp=40A

U42
VCC:
Imax=42A Ipeak=64A Iocp=70A

VCCGT:
Imax=18A Ipeak=31A Iocp=39A

VCCSA:
Imax=4A Ipeak=5A Iocp=9.5A





Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	LA-F241P	0.1

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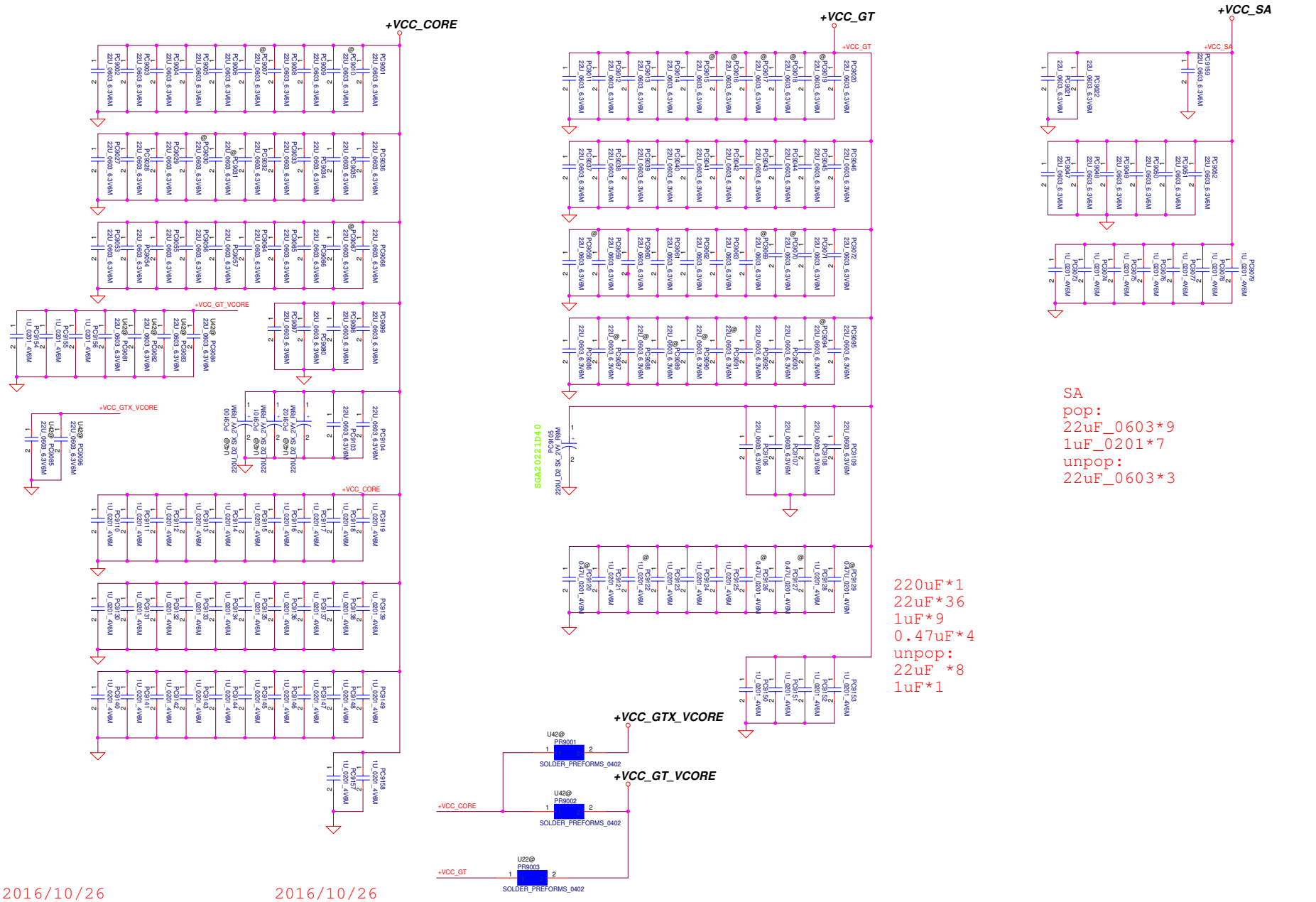

2016/10/26
VCORE Output Capacitor:
U42
22uF_0603*39
1uF_0201*35
220uF *3
UNPOP
22_0603*3

2016/10/26
VCORE Output Capacitor:
U22
22uF_0603*33
1uF_0201*35
UNPOP
22_0603*9
220uF *3

Security Classification	Compal Secret Data		
Issued Date	2017/02/22	Deciphered Date	2018/02/22

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	LA-F241P	0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	ON FAE suggest to modify Parts for Kaby lake CPU setting	0.2	55	PC818 change to 33 pF. PC834 Change to 8200pF PC820 Change to 0.033 uF PR857 Change to 73.2K ohm PR836 Change to 61.9K ohm	9/21	PVT
02							
03							
04							
05	Design Change.	For material issue, Changer main source part	0.2	56	PC9004,PC9079 change to SF000007700 (33 uF). PL9006 change to SH00000PK00 (0.47uH).	9/30	PVT
06							
07				48	PD101, PD102 change to SCS00005X00.		
08	Design Change.	For material issue, Changer main source part	1.0	52	PQ502 change to SB000010A00.	1/4	Pre-MP
09				50, 52	PQ305, PQ503 change to SB00000H800.		
10				56, 60	PQ1201,PQ1203,PQ9002,PQ9005 change to SB00000JZ00.		
11				56, 60	PQ1202,PQ1204,PQ9003,PQ9007 change to SB000017Q00.		
12	Design Change.	For PD power function, add 0 ohm	1.0	50	PQ303 change to SB000017B00.	1/4	Pre-MP
13				50	PQ306 change to SB00000H700.		
14							
14							

Compal Electronics, Inc.
Title: PIR
Size: Custom | Document Number: LA-F241P | Rev: 0.1
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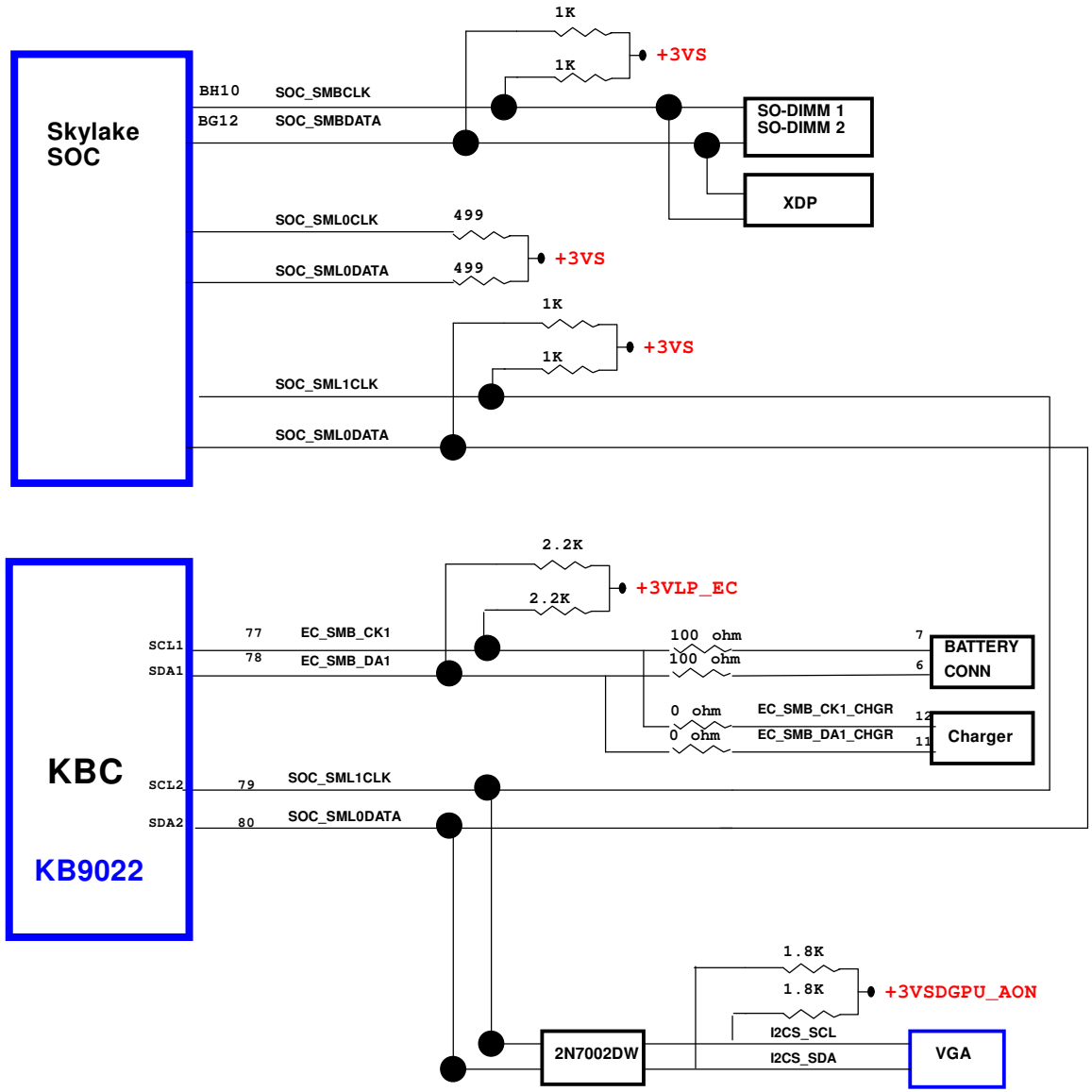

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SMBUS Routing Table

Size: Custom | Document Number: C4PB1/C5PB1 LA-591 | Rev: 0.1

Date: Friday, June 09, 2017 | Sheet 61 of 64

P6->P6 U42
EVT_R0.1

4/24
1. ADD TS conn. JTS1
2. Add USB PORT 10 for TS function
3. Reserve USB PORT 6 test point(T3821,T3822) for NFC
4. Remove GPU circuit
5. Support PD charger in
6. ADD U5010 circuit for TS function
7. Add 24M XTAL(YC3) for KBL U42
8. +VCC_GTX_CORE contact to CPU (UC1.M)
9. +VCC_GT_CORE contact to CPU (UC1.M)
10. Add RC256
11. Del UC9 circuit
12. DEL RC58 (direct contact U11, U12)
13. Add TBTA_HV_GATE1/2 for PD in
14. Add TBTA_PD_SENSEP/N for PD in
15. DEL H23,H24
16. DEL RC204, RC195
17. Reserve test point T3812~3815 for GPU
18. update PARADE X76, X76525BOL05
19. Change RC38 to 121ohm
20. DEL XDP circuit
21. change RC182 to 0ohm@
22. Add R5274 for ME906
23. ADD HYNIX 8G SA0000ARA10 on board ram
24. ADD T3849
25. ADD SATAXPCIE2
26. ADD R5276,R5275@, Q2023@ for PCIE SSD
27. Change Card reader to PCIE port4
28. ADD PCIE port 10 for PCIE_SSD
29. ADD CLK port 0 for PCIE_SSD
30. ADD D2018,D2019,D2020,D2021,D2022,D2023 for ESD
31. ADD CC435,CC436
32. ADD RC258

4/25
1. Q40,Q51,Q52,Q53,Q2006,Q2010,Q2013,Q2014,Q2016,
Q2017,Q2018,Q2019,Q2020,Q2021,QL2, change PN to SB00000SA00
2. Change U67 PN to SA00007IOA0 NPCT650ABCWX

4/26
Change U67 to SA00007IOA0

4/27
change R5207,R5208 to TBT@ and R5266,R5267 to @ for support dead battery

5/4
modify yellow BOM structure to meet white item
CC53,D17,D18,D19,D20,D21,D23,D24,R5196,R5204,R5207,R5208

PVT_R1.0

5/10
Swap JSSD1 PIN41,43 net

6/3
R401 chager to 47K for RF request(ME906)
Add RC 259 for CLKREQ_PCIE#0 pull up +3VS
change R5196,R4960 to @
change R5205 to 100Kohm TBT@
change R659 to mount
change UC2 PN to SA00005VV20
swap JSSD PCIE port 11,12
SSD_DET# connect to SATAXPCIE1
change R4903 to 12K
Add C5265 for PCIE SSD power
Add Adp_det
change R4938 to 0ohm
VCOUT1_PROCHOT connect to HPROCHOT#
remove J13 for C5265

6/8
Add R5277 for +5VS_CRT_SW
Add L4905 for +3VS_CRT_SW
SW_PROCHOT# connect to H_PROCHOT#
Change R4960 to mount
Change R523,R4938,R5276 to short pad
Change R5260 to 0ohm
Add Q2024,R5279,R5278 for +1.8VALW_PRIM discharge circuit
Change UU24, CU181, RU165 to @

6/8A
remove RC151

6/9
change R5193 to 0ohm_0402

Compal Electronics, Inc.

Title: HW PIR

Size	Document Number	Rev
Custom	C4PB1/C5PB1 LA-E591P	1.0

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DDR4 On Board RAM

X76713BOL03 Hynix

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U2
X76OBHY@

10K +-5% 0402
SD028100280
RU173
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U3
X76OBHY@

10K +-5% 0402
SD028100280
RU169
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U4
X76OBHY@

D4 512M16 H5AN8G6NAFR
SA0000A1H20
U5
X76OBHY@

X76713BOL01 micron 4G

D4 512M16 MT40A512M16JY
SA00009V220
U2
X76OBMACRON4@

10K +-5% 0402
SD028100280
RU170
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U3
X76OBMACRON4@

10K +-5% 0402
SD028100280
RU172
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U4
X76OBMACRON4@

D4 512M16 MT40A512M16JY
SA00009V220
U5
X76OBMACRON4@

X76713BOL02 micron 8G

D4 16G MT40A1G16WBU
SA0000A3120
U2
X76OBMACRON8@

10K +-5% 0402
SD028100280
RU169
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U3
X76OBMACRON8@

10K +-5% 0402
SD028100280
RU170
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U4
X76OBMACRON8@

D4 16G MT40A1G16WBU
SA0000A3120
U5
X76OBMACRON8@

X76713BOL06 HYNIX 8G

D4 16G/2400 H5ANAG6NAMR
SA0000ARA10
U2
X76OBHYNIX8@

10K +-5% 0402
SD028100280
RU173
X76OBHYNIX8@

D4 16G/2400 H5ANAG6NAMR
SA0000ARA10
U3
X76OBHYNIX8@

10K +-5% 0402
SD028100280
RU172
X76OBHYNIX8@

D4 16G/2400 H5ANAG6NAMR
SA0000ARA10
U4
X76OBHYNIX8@

D4 16G/2400 H5ANAG6NAMR
SA0000ARA10
U5
X76OBHYNIX8@

VRAM

X76614BOL54 Hynix

D3 256M16 H5TC4G63CFR
SA00008DN10
U2004
X76VHY@

30K +-1% 0402
SD034300280
R2044
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2005
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2006
X76VHY@

D3 256M16 H5TC4G63CFR
SA00008DN10
U2007
X76VHY@

X76614BOL58 SANSUNG

D3 256M16 K4W4G1646E
SA000076PB0
U2004
X76VSAM@

24.9K +-1% 0402
SD034249280
R2044
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2005
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2006
X76VSAM@

D3 256M16 K4W4G1646E
SA000076PB0
U2007
X76VSAM@

X76713BOL04 Hynix E-die

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2004
X76VHY_E@

10K_0402_1%
SD034100280
R2035
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2005
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2006
X76VHY_E@

S IC D3 256M16 H5TC4G63EFR-N0C
SA00008DN80
U2007
X76VHY_E@

SATA Redriver

X76525BOL51 TI

SN75LVCP601RTJR
SA00003ZX00
U1
X76SATATI@

4.99K +-1% 0402
SD034499180
R11
X76SATATI@

X76713BOL05 Parade

PS8527CTQFN20GTR2-A2
SA00007JU10
U1
X76SATAPAR@

4.7K +-5% 0402
SD028470180
R18
X76SATAPAR@

7.5K +-5% 0402
SD028100280
R11
X76SATAPAR@

X76525BOL52 Parade

PS8527CTQFN20GTR2-A1
SA00007JU00
U1
X76SATAPARa@

4.7K +-5% 0402
SD028470180
R18
X76SATAPARa@

7.5K +-5% 0402
SD028100280
R11
X76SATAPARa@

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **X76 Level Note**

Size: Custom | Document Number: C4PB1/C5PB1 LA-E591P | Rev: 1.0

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