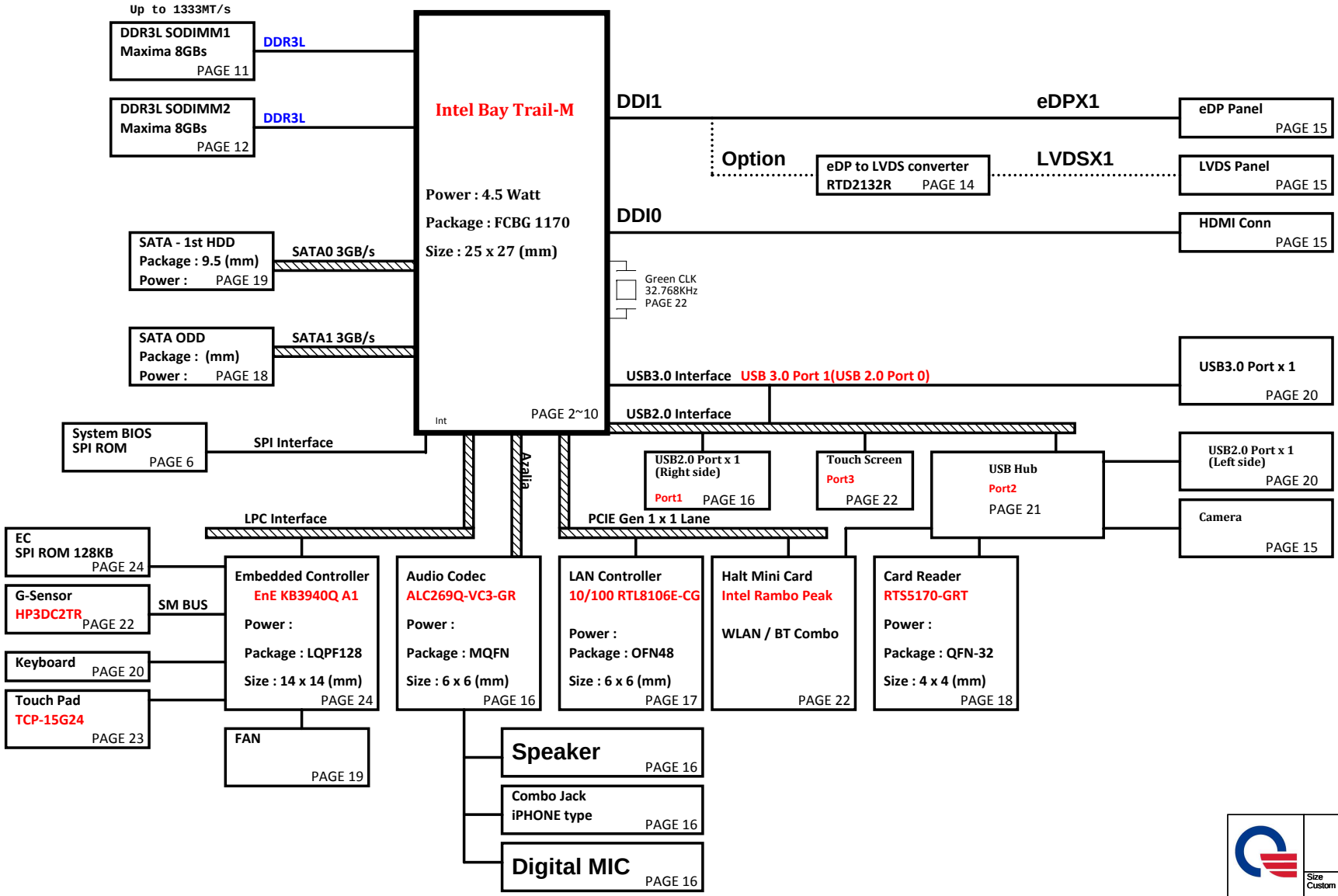
JWM UMA(14")
Intel Bay Trail-M Platform Block Diagram

PCB 6L STACK UP

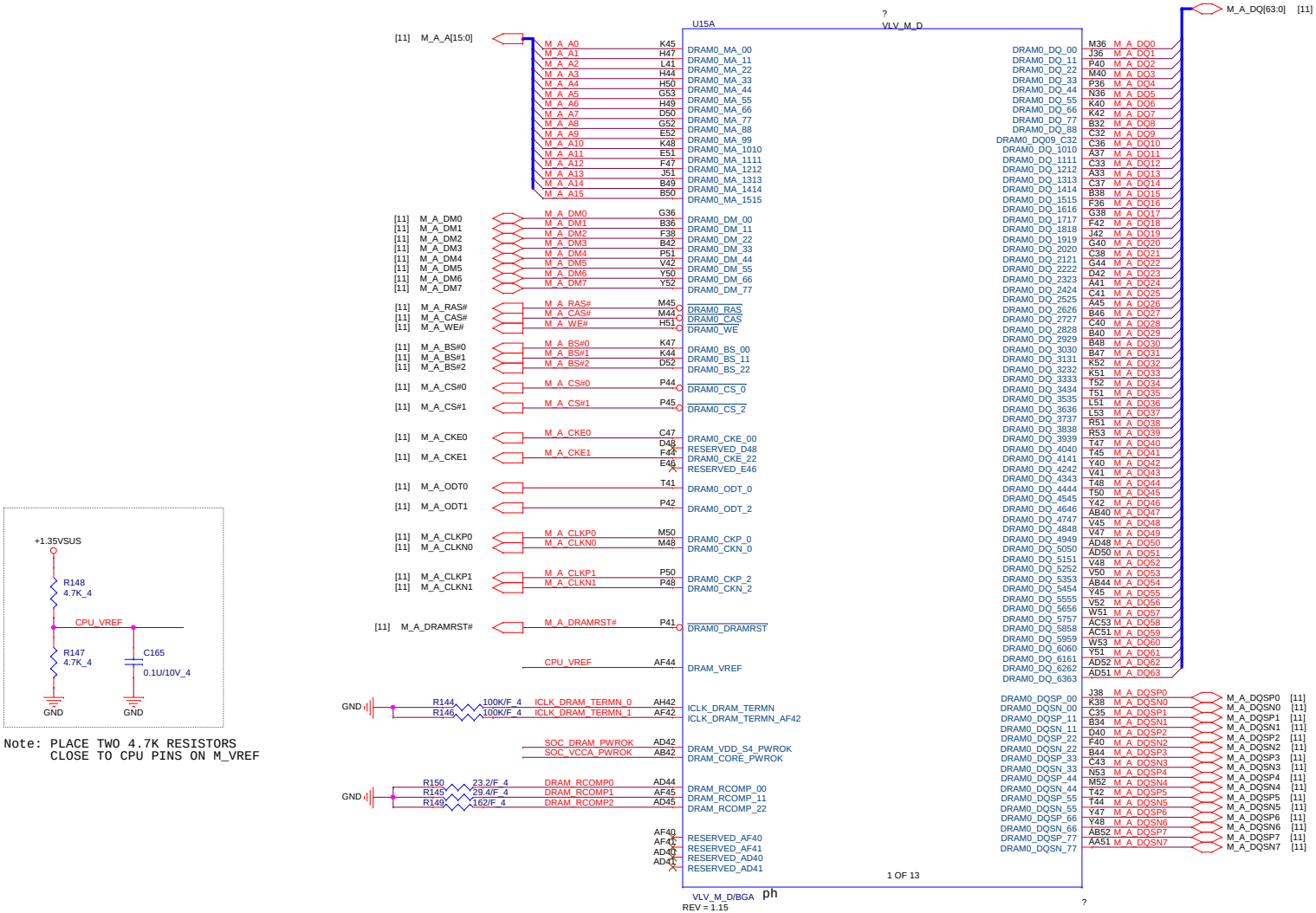
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



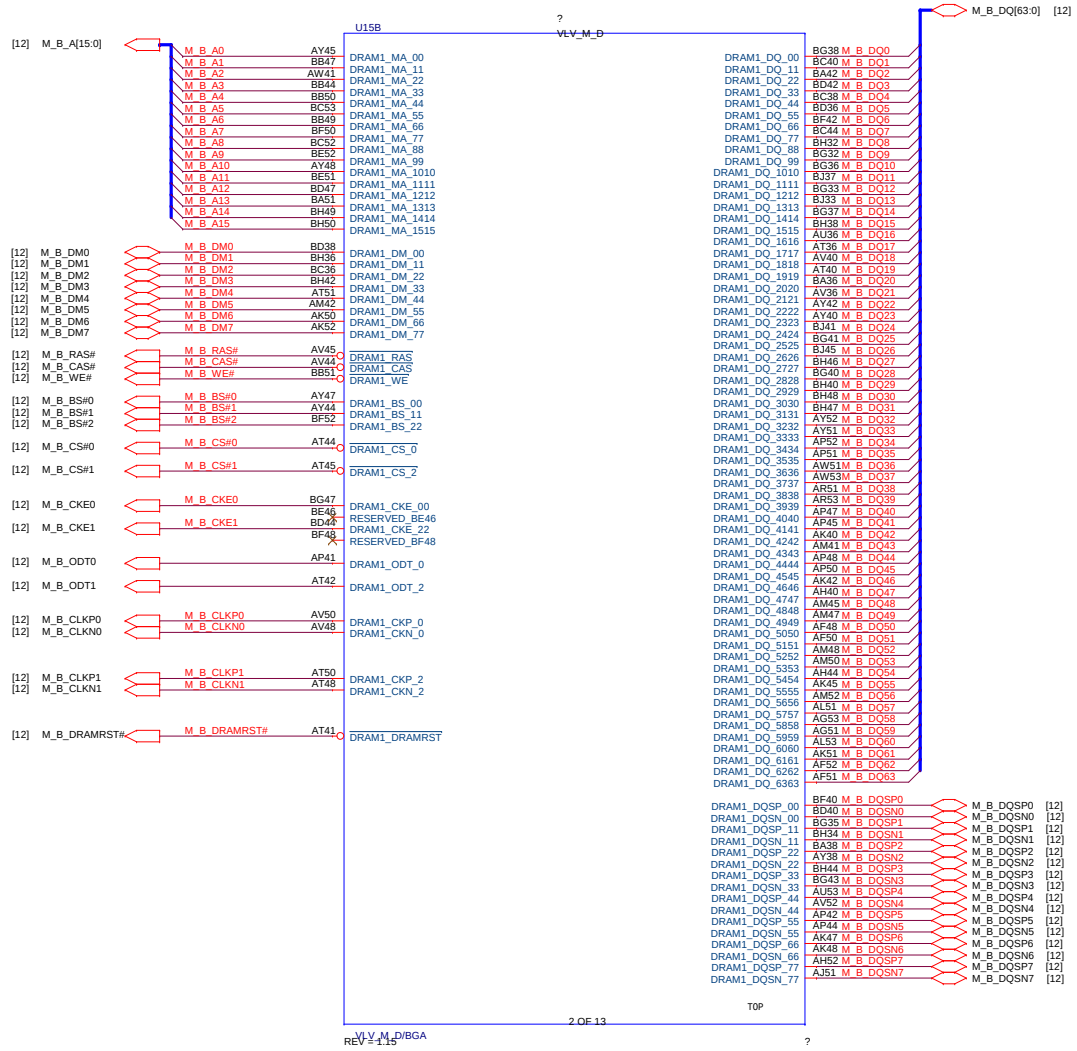
PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, August 20, 2013 Sheet 1 of 39

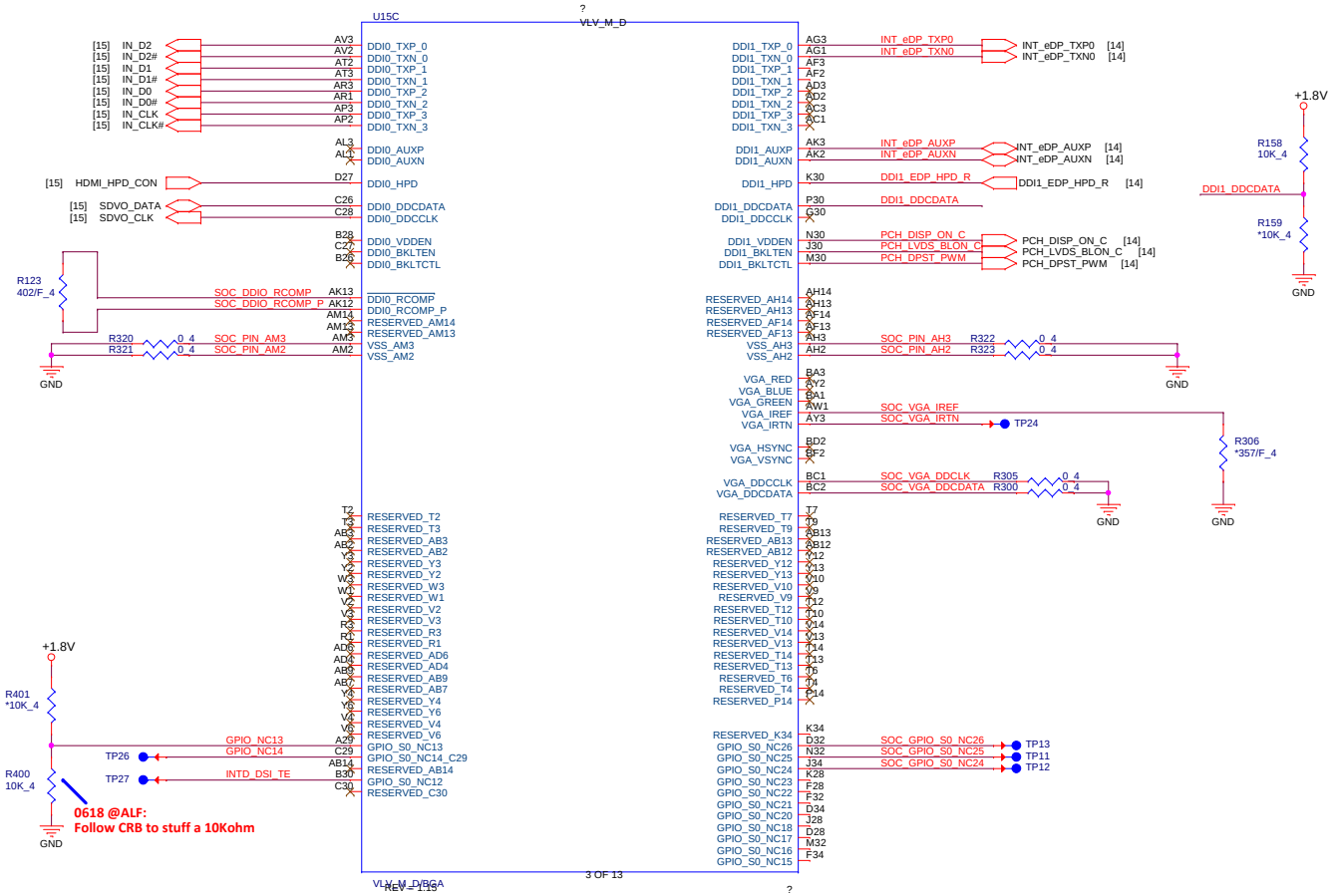


Quanta Computer Inc.	PROJECT :JWM	
Size: Custom	Document Number: Valley 1/9 (DDRA)	Rev: 1A
Date: Tuesday, August 20, 2013	Sheet 2 of 39	



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 2/9 (DDRB)	1A
Date: Tuesday, August 20, 2013	Sheet 3 of 39	



PROJECT :JWM Quanta Computer Inc.		
Size: Custom	Document Number: Valley 3/9 (Display)	Rev: 1A
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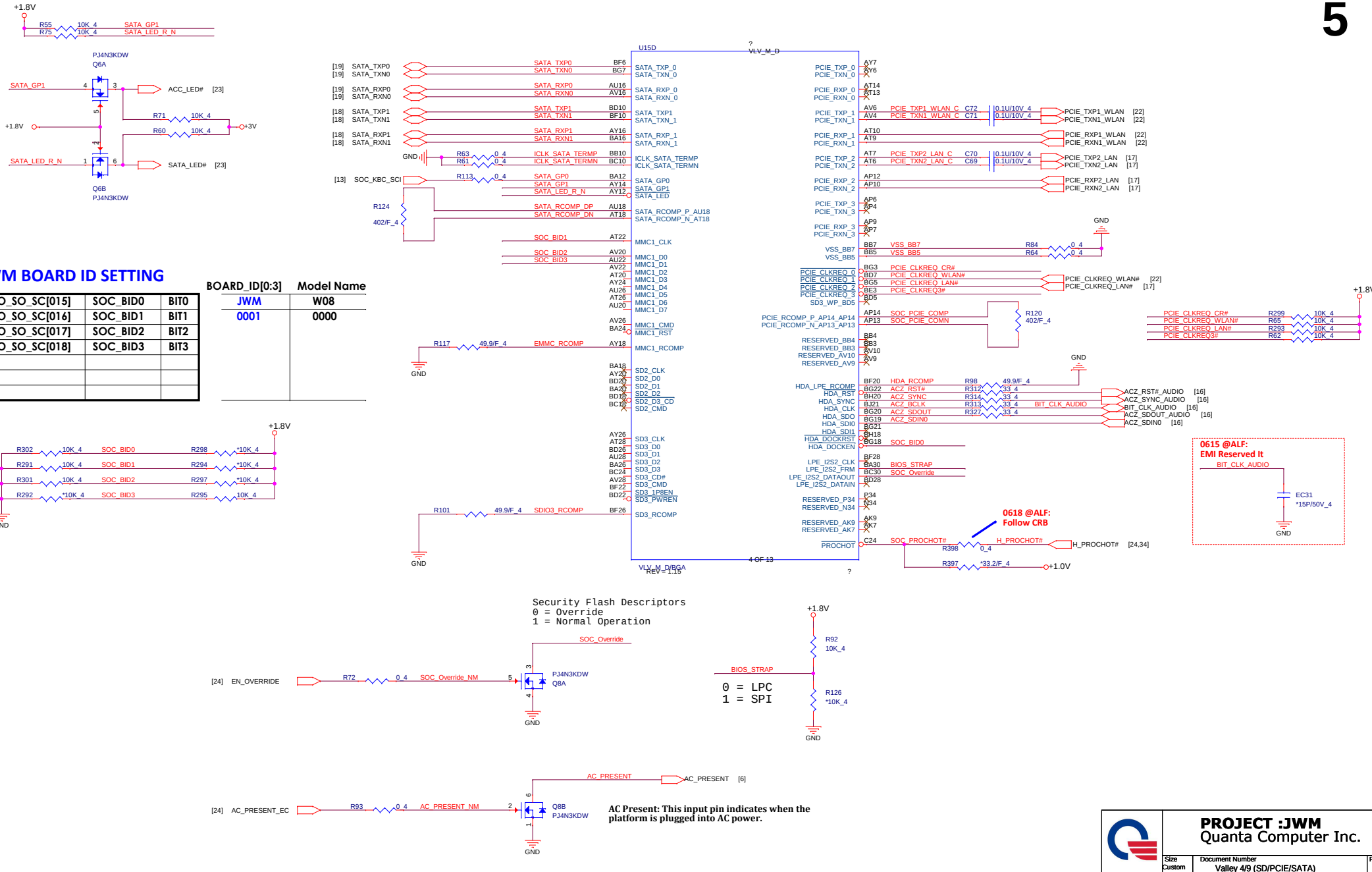
JWM BOARD ID SETTING

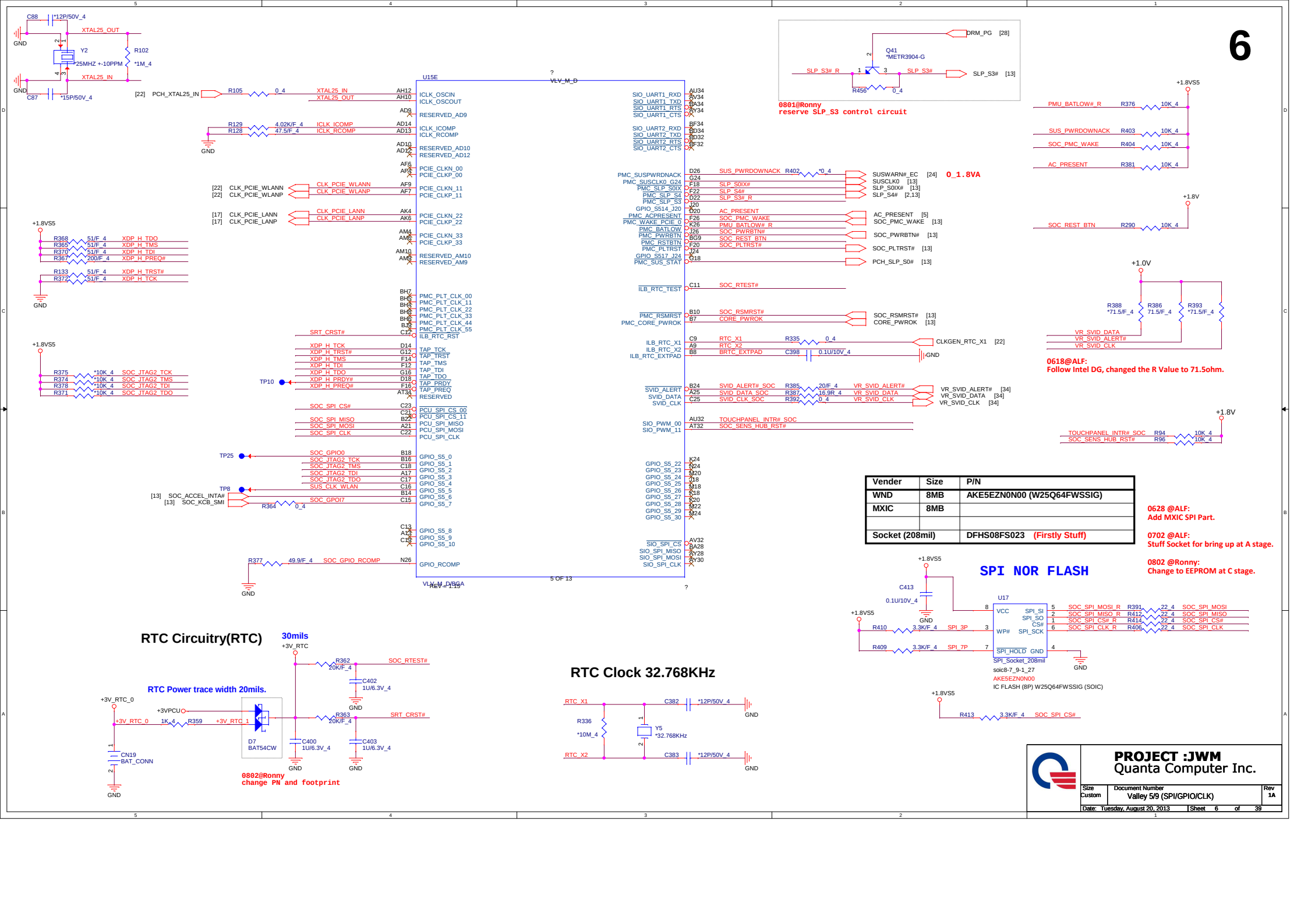
GPIO_SO_SC[015]	SOC_BID0	BIT0
GPIO_SO_SC[016]	SOC_BID1	BIT1
GPIO_SO_SC[017]	SOC_BID2	BIT2
GPIO_SO_SC[018]	SOC_BID3	BIT3

BOARD_ID[0:3]	Model Name
JWM	W08
0001	0000



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 4/9 (SD/PCIE/SATA)	1A
Date: Tuesday, August 20, 2013	Sheet 5 of 39	



Vender	Size	P/N
WND	8MB	AKE5EZN0N00 (W25Q64FWSSIG)
MXIC	8MB	
Socket (208mil)		DFHS08FS023 (Firstly Stuff)

+3V_WLAN_P
R344 10K_4
[22] BT_COMBO_EN#
Q27 2N7002E
BT_COMBO_EN
GND

+1.8VS5
R338 10K_4 BT_OFF
R343 10K_4 RF_OFF
R342 10K_4 BT_COMBO_EN
R309 10K_4 ODD_PRSNT#_R
R341 10K_4 SOC_PWR_BUT

+3V
[18] ZERO_ODD_DP#
ODD_PRSNT#_R
Q26 *2N7002E

U15F
VLV_M_D
GPIO_S5_31
[22] BT_OFF
[22] RF_OFF
BT_COMBO_EN
ODD_PRSNT#_R
SOC_PWR_BUT
GPIO_S5_32
GPIO_S5_33
GPIO_S5_34
GPIO_S5_35
GPIO_S5_36
GPIO_S5_37
GPIO_S5_38
GPIO_S5_39
GPIO_S5_40
GPIO_S5_41
GPIO_S5_42
GPIO_S5_43

RESERVED_M10
RESERVED_M9
RESERVED_P7
RESERVED_P6
RESERVED_M7
USB3_REXT0
R131 1.24K/F_4
RESERVED_P10
RESERVED_P12
RESERVED_M4
RESERVED_M6
USB3_RXP0
USB3_RXN0
USB30_RX1+ [20]
USB30_RX1- [20]
USB3_TXP0
USB3_TXN0
USB30_TX1+ [20]
USB30_TX1- [20]

USB 3.0
Daughtor Board USB (Debug Port)
HUB1
0603 @ALF: I/O Port (Upper-Right)
0607 @Ronny: TV Tuner

[20] USBP0+
[20] USBP0-
USB_DP0
USB_DN0
[16] USBP1+
[16] USBP1-
USB_DP1
USB_DN1
[21] USB_H1_P
[21] USB_H1_N
USB_DP2
USB_DN2
[20] USBP_MB+
[20] USBP_MB-
[19] USBP_TV+
[19] USBP_TV-
R213 0_4 USBP_H3+
R212 0_4 USBP_H3-
R216 *0_4
R215 *0_4
R132 1K/F_4 ICLK_USB_TERMN_0
R107 1K/F_4 ICLK_USB_TERMN_1
USB_DP3
USB_DN3
ICLK_USB_TERMN_D10
ICLK_USB_TERMN

RESERVED_H8
RESERVED_H7
RESERVED_H5
RESERVED_H4

0801 @Ronny: change USB2.0 port form Hub to SOC for USB wake up used

[20] SOC_USB_OC0
SOC_USB_OC0
SOC_USB_OC1
R380 10K_4
R382 10K_4
USB_OC_00
USB_OC_11

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted
R56 10K_4
R53 *10K_4

R347 45.3/F_4 USB_RCOMP
USB_RCOMPO
USB_RCOMPI
R108 *0_4
USB_PLL_MON
0621 @ALF: Follow Intel CRB

GPIO_S0_SC_55
GPIO_S0_SC_56
GPIO_S0_SC_57
GPIO_S0_SC_58
GPIO_S0_SC_59
GPIO_S0_SC_60
GPIO_S0_SC_61
GPIO_S0_SC_56
SOC_UART_TX
SOC_SENSOR_HUB_WAKE
TOUCH_PANEL_SOC_RST#
SOC_UART_RX

ILB_8254_SPKR
ACZ_SPKR [16]

TOUCH_PANEL_SOC_RST# R78 10K_4
SOC_SENSOR_HUB_WAKE R74 10K_4

SOC_UART_TX R109 *0_4 SOC_UART_RX
Un-Stuff for Test Only

USB_HSIC0_DATA
USB_HSIC0_STROBE
USB_HSIC1_DATA
USB_HSIC1_STROBE
R351 45.3/F_4 USB_HSIC_RCOMP
R118 49.9/F_4
USB_HSIC_RCOMP

0615 @ALF: EMI Reserved It
CLK_24M_KBC
EC32 *15P/50V_4
CLK_PCI_TPM
EC33 *15P/50V_4

LPC_RCOMP
[19,22,24] LAD0
[19,22,24] LAD1
[19,22,24] LAD2
[19,22,24] LAD3
[19,22,24] LFRAME#
[24] CLK_24M_KBC
ILB_LPC_AD_00
ILB_LPC_AD_11
ILB_LPC_AD_22
ILB_LPC_AD_33
ILB_LPC_FRAME
ILB_LPC_CLK_00
ILB_LPC_CLK_11
ILB_LPC_CLKRUN
ILB_LPC_SERIRQ
[19] CLK_PCI_TPM
[22] CLK_24M_DEBUG
R311 22_4 SOC_CLKOUT_0
R329 22_4 SOC_CLKOUT_1
[19,24] CLKRUN#
[13] SOC_SERIRQ
R328 22_4 SOC_CLKRUN#
SOC_SERIRQ

SIO_I2C0_DATA
SIO_I2C0_CLK
SIO_I2C1_DATA
SIO_I2C1_CLK
SIO_I2C2_DATA
SIO_I2C2_CLK
SIO_I2C3_DATA
SIO_I2C3_CLK
SIO_I2C4_DATA
SIO_I2C4_CLK
SIO_I2C5_DATA
SIO_I2C5_CLK
SIO_I2C6_DATA
SIO_I2C6_CLK
I2C_0_SDA
I2C_0_SCL
I2C_1_SDA
I2C_1_SCL
I2C_2_SDA_R
I2C_2_SCL_R
I2C_3_SDA
I2C_3_SCL
I2C_4_SDA
I2C_4_SCL
I2C_5_SDA
I2C_5_SCL
I2C_6_SDA
I2C_6_SCL

I2C_0_SDA R326 2.2K_4
I2C_0_SCL R325 2.2K_4
I2C_1_SDA R324 2.2K_4
I2C_1_SCL R310 2.2K_4
I2C_2_SDA_R R317 2.2K_4
I2C_2_SCL_R R316 2.2K_4
I2C_3_SDA R319 2.2K_4
I2C_3_SCL R318 2.2K_4
I2C_4_SDA R95 2.2K_4
I2C_4_SCL R97 2.2K_4
I2C_5_SDA R333 2.2K_4
I2C_5_SCL R332 2.2K_4
I2C_6_SDA R331 2.2K_4
I2C_6_SCL R330 2.2K_4
I2C_NFC_SOC_SDA R337 2.2K_4
I2C_NFC_SOC_SCL R339 2.2K_4

0615 @ALF: EMI Reserved It
CLK_24M_DEBUG
EC34 *15P/50V_4

+1.8V
R304 2.2K_4 SMB_SOC_DATA
R289 2.2K_4 SMB_SOC_CLK
R296 10K_4 SMB_SOC_ALERTB
PCU_SMB_DATA
PCU_SMB_CLK
PCU_SMB_ALERT

Q25
SMB_SOC_DATA 4
SMB_SOC_CLK 1
4.7K_4 R288 +3V
4.7K_4 R303 +3V
SMB_RUN_DAT
SMB_RUN_CLK
SMB_RUN_DAT [11,12,14,23]
SMB_RUN_CLK [11,12,14,23]
PJ4N3KDW

0625@ALF: Q7019 Changed the P/N from BAM70020003 to BAM4N3K0000. Because of the VGS, the range is 0.8~1.5V

VLV_M_D/BGA
REV = 1.15
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Quanta Computer Inc.
Size: Custom
Document Number: Valley 6/9 (USB/LPC/I2C)
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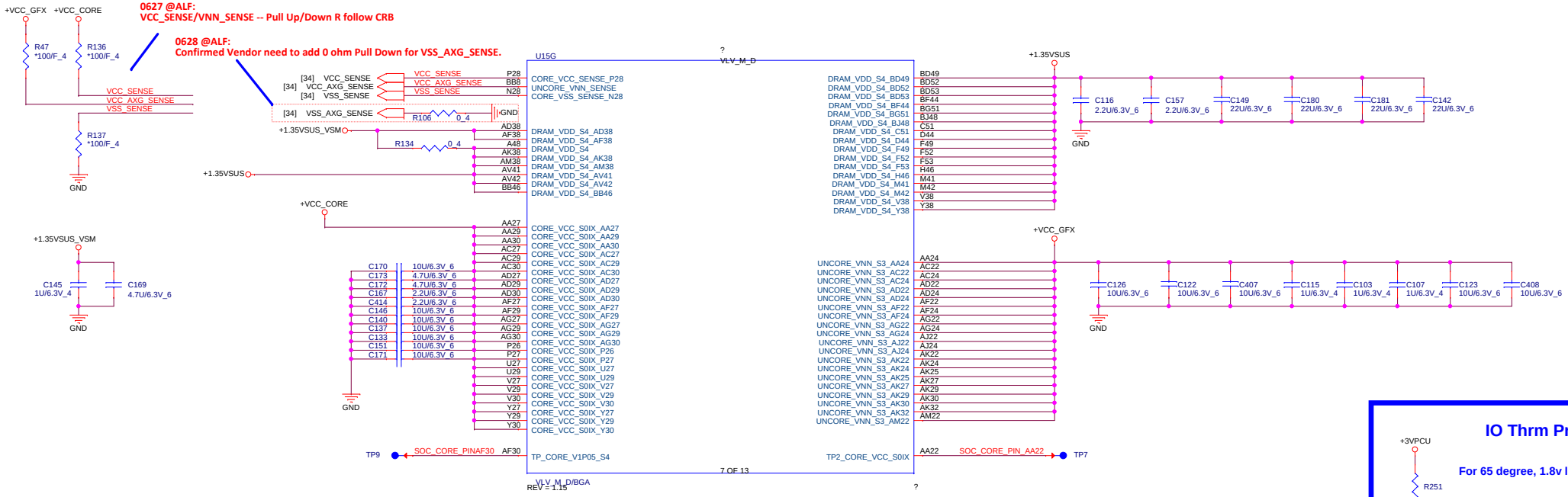
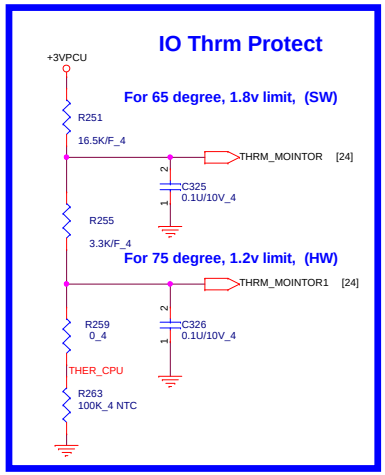
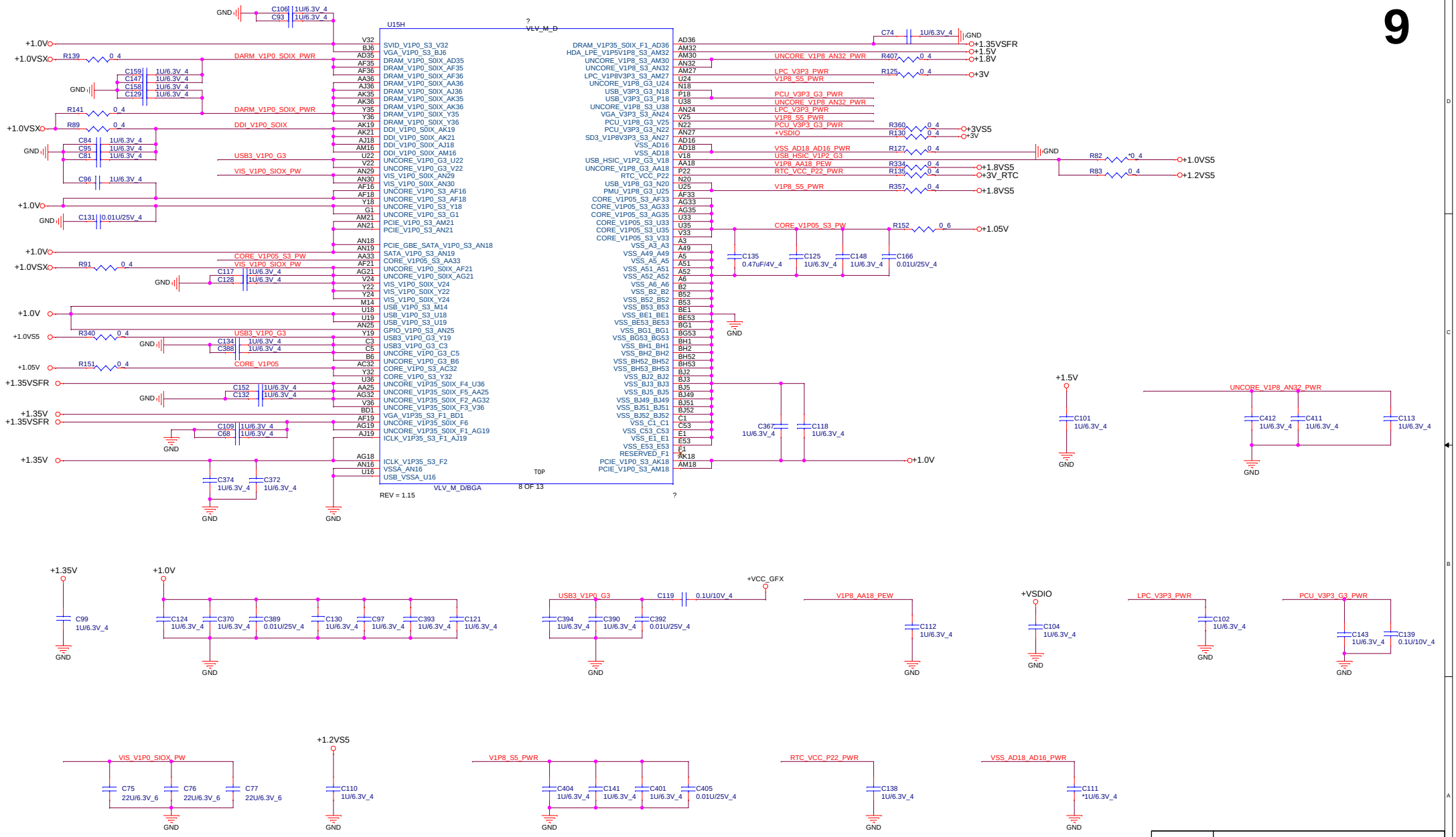




PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 7/9 (Power 1)	1A
Date: Tuesday, August 20, 2013	Sheet 8 of 39	


U15H
VLV_M_D
VLV_M_D/BGA
REV = 1.15
8 OF 13
T0P
+1.0V
+1.0VSX
+1.0VS5
+1.05V
+1.35VSFR
+1.35V
+1.5V
+1.8V
+3V
+3VS5
+1.8VS5
+3V_RTC
+1.2VS5
+VCC_GFX
+VSDIO
GND
DARM_V1P0_SOIX_PWR
DDI_V1P0_SOIX
USB3_V1P0_G3
VIS_V1P0_SIOX_PW
CORE_V1P05_S3_PW
CORE_V1P05
UNCORE_V1P8_AN32_PWR
LPC_V3P3_PWR
V1P8_S5_PWR
PCU_V3P3_G3_PWR
USB_HSIC_V1P2_G3
V1P8_AA18_PEW
RTC_VCC_P22_PWR
VSS_AD18_AD16_PWR
PCU_V3P3_G3_PWR
PROJECT :JWM
Quanta Computer Inc.
Valley 8/9 (Power 2)
Size Custom
Rev 1A
Date: Tuesday, August 20, 2013
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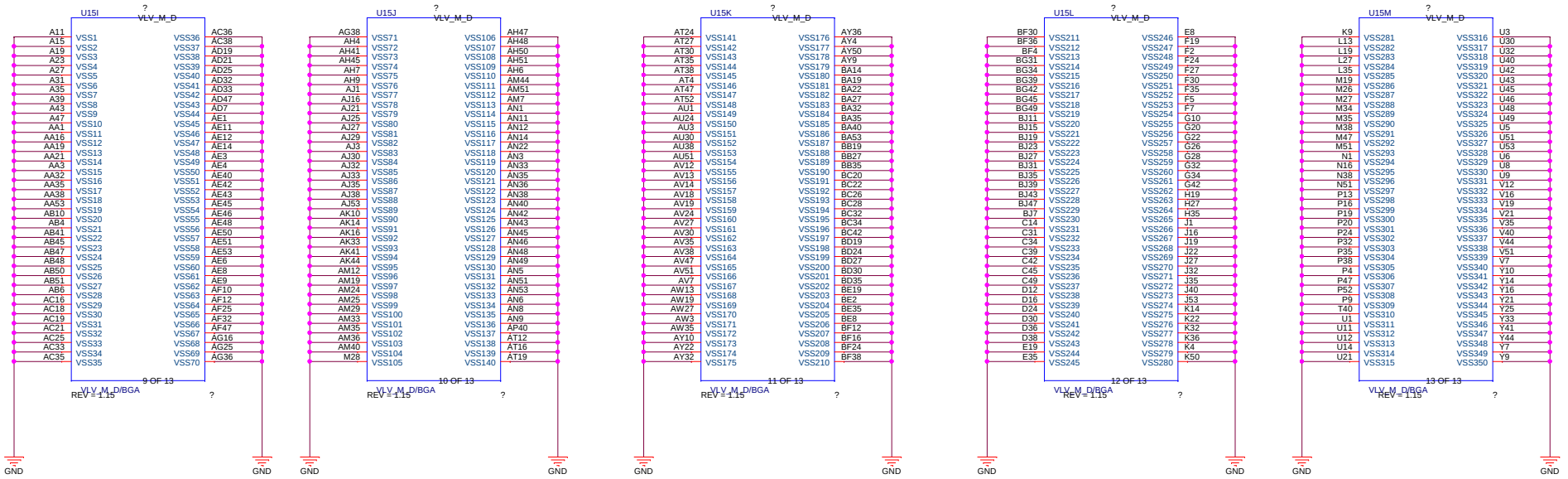

PROJECT :JWM
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Size	Document Number	Rev
Custom	Valley 9/9 (GND)	1A

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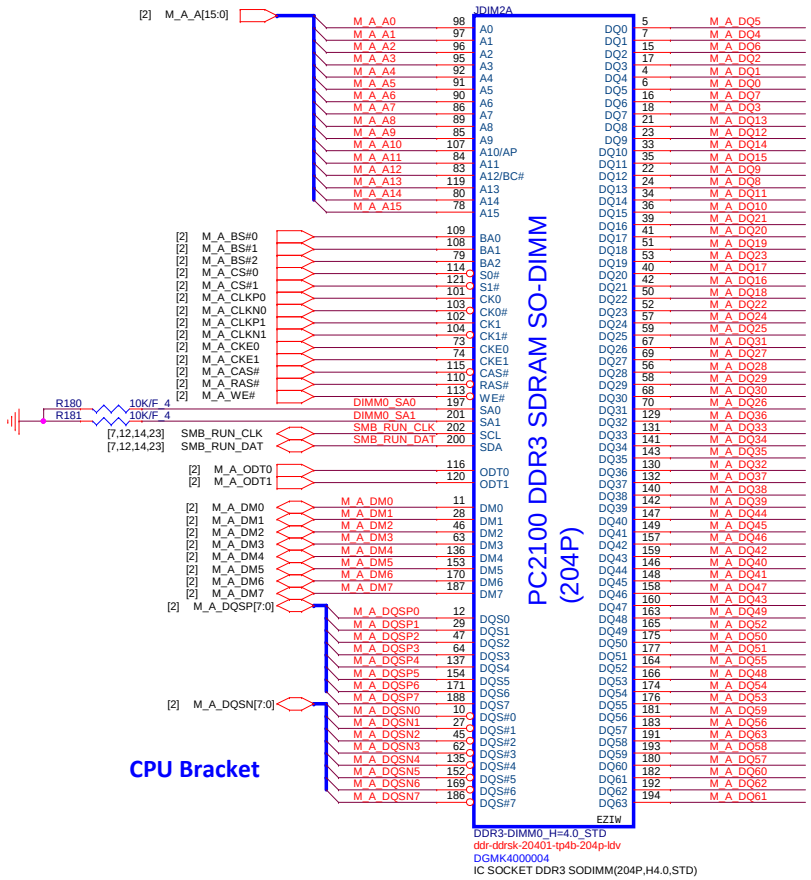
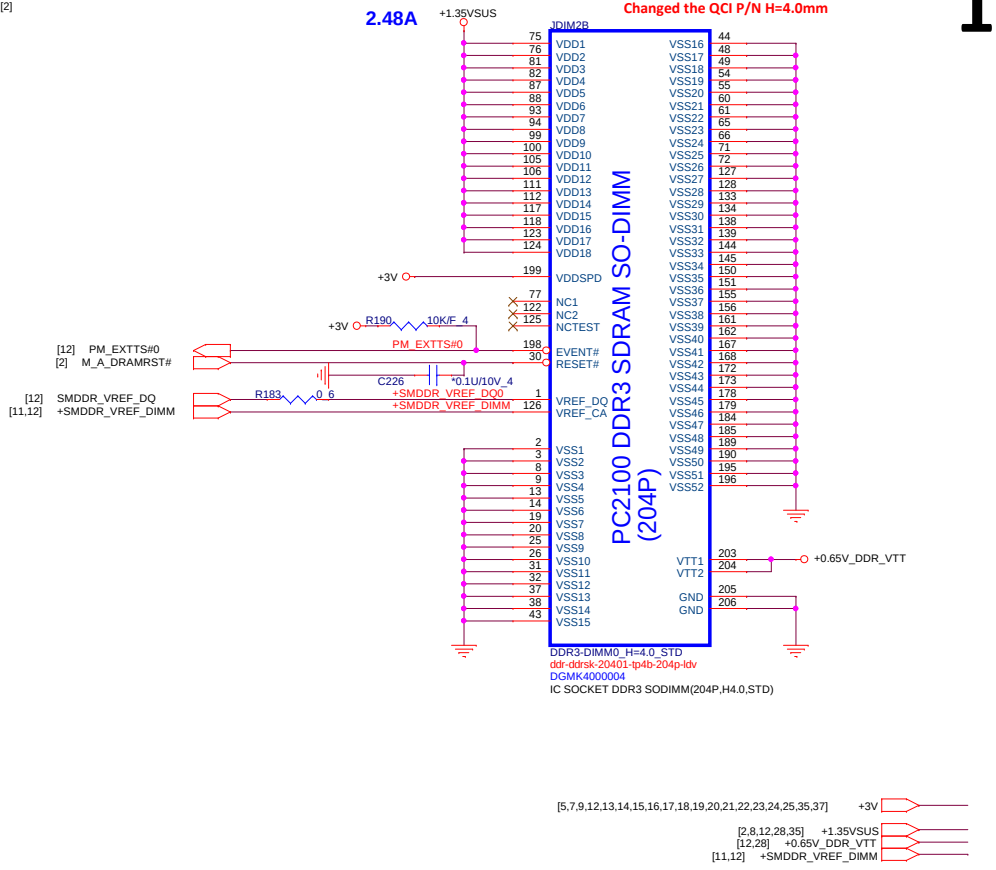
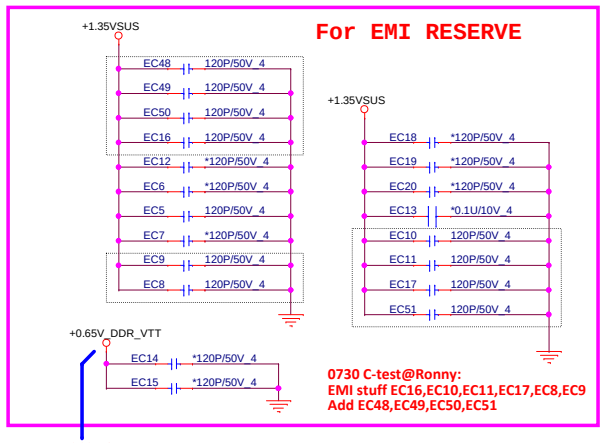
0617 @ALF:
Changed the QCI P/N H=4.0mm

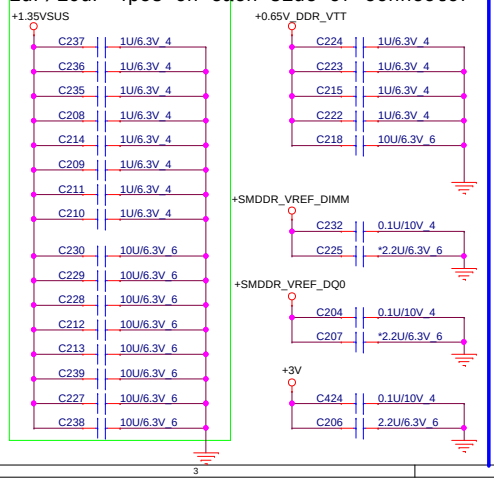


2.48A

0617 @ALF:
Changed the QCI P/N H=4.0mm







PROJECT :JWM
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Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
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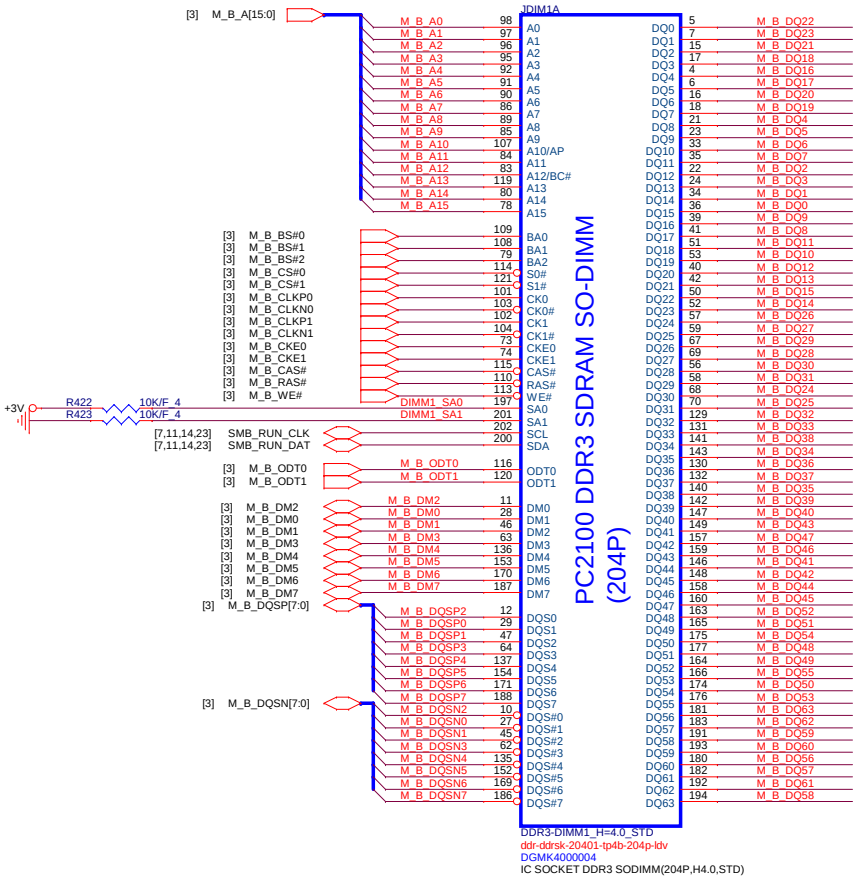
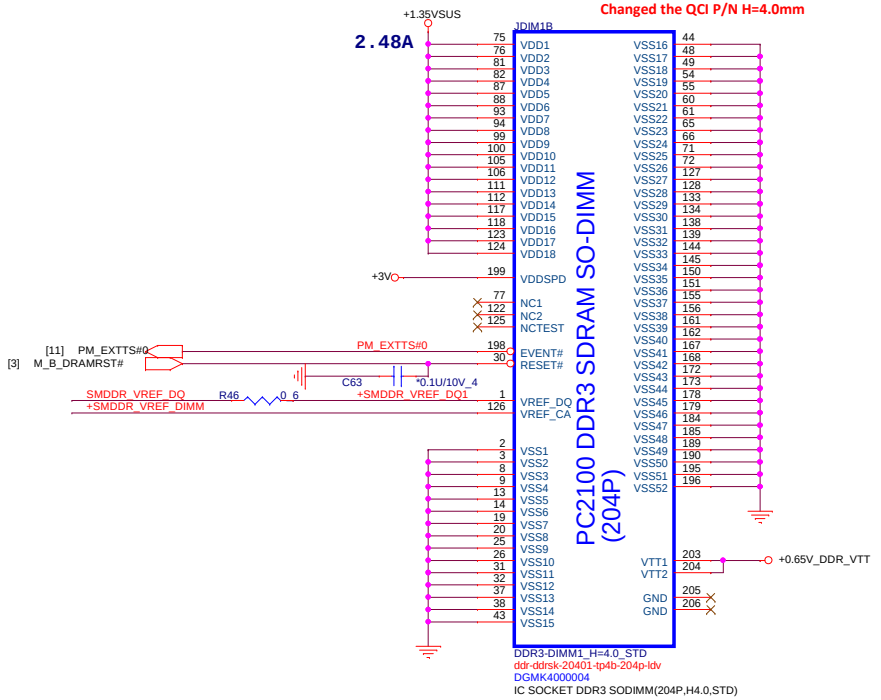
0617 @ALF:
Changed the QCI P/N H=4.0mm

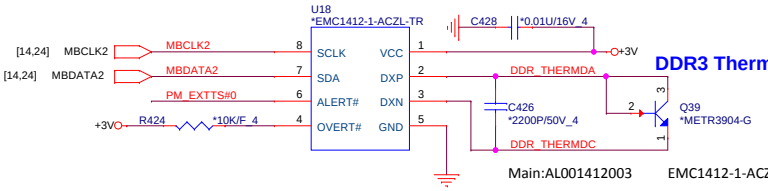


M_B_DQ[63:0] [3]

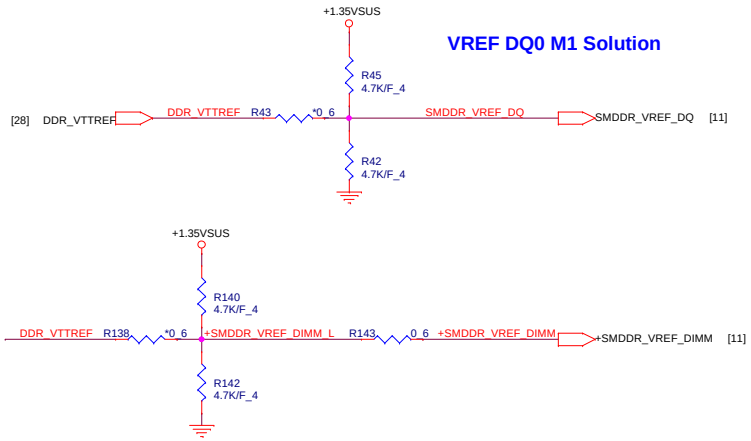
0617 @ALF:
Changed the QCI P/N H=4.0mm



Local Thermal Sensor

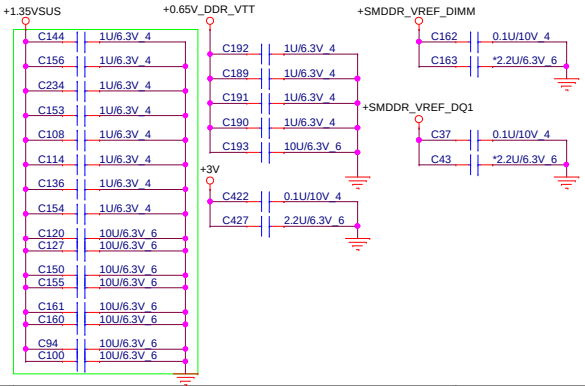


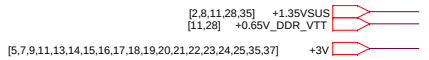
VREF DQ0 M1 Solution

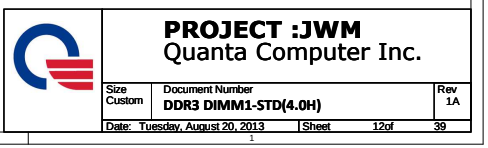


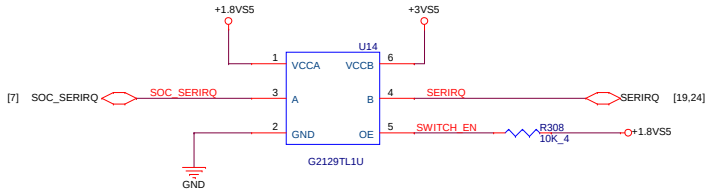
Place these Caps near So-Dimm1.

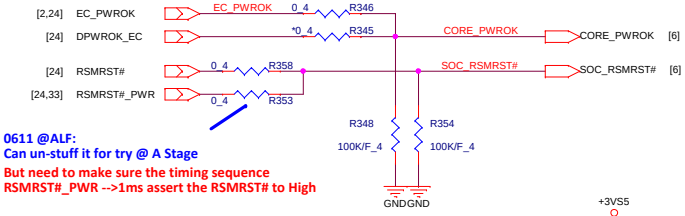
1uF/10uF 4pcs on each side of connector



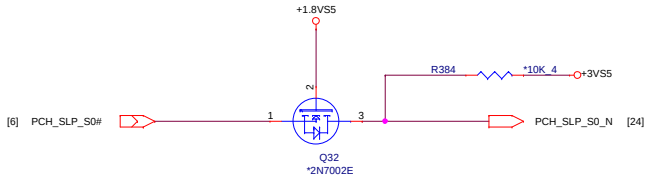


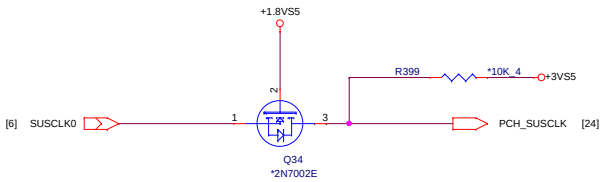


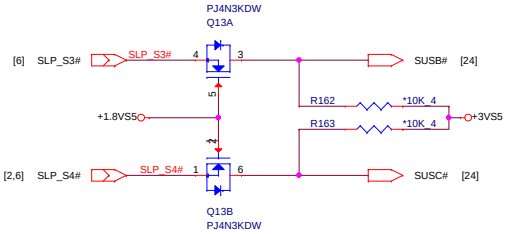


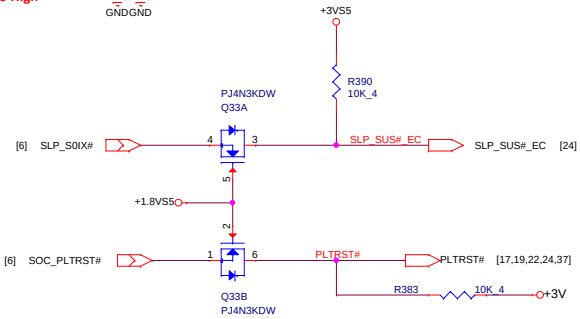


0611 @ALF:
Can un-stuff it for try @ A Stage
But need to make sure the timing sequence
RSMRST#_PWR -->1ms assert the RSMRST# to High

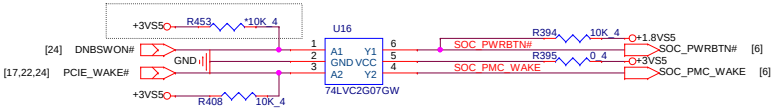




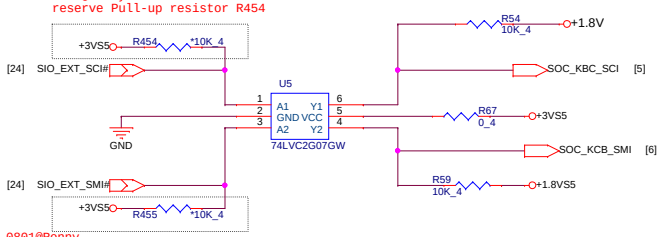




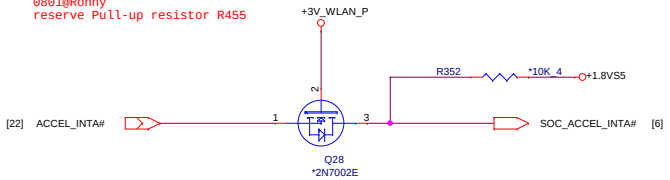
0801@Ronny
reserve Pull-up resistor R453



0801@Ronny
reserve Pull-up resistor R454



0801@Ronny
reserve Pull-up resistor R455



PROJECT :JWM
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Size	Document Number	Rev
Custom	Level Shfiter	1A
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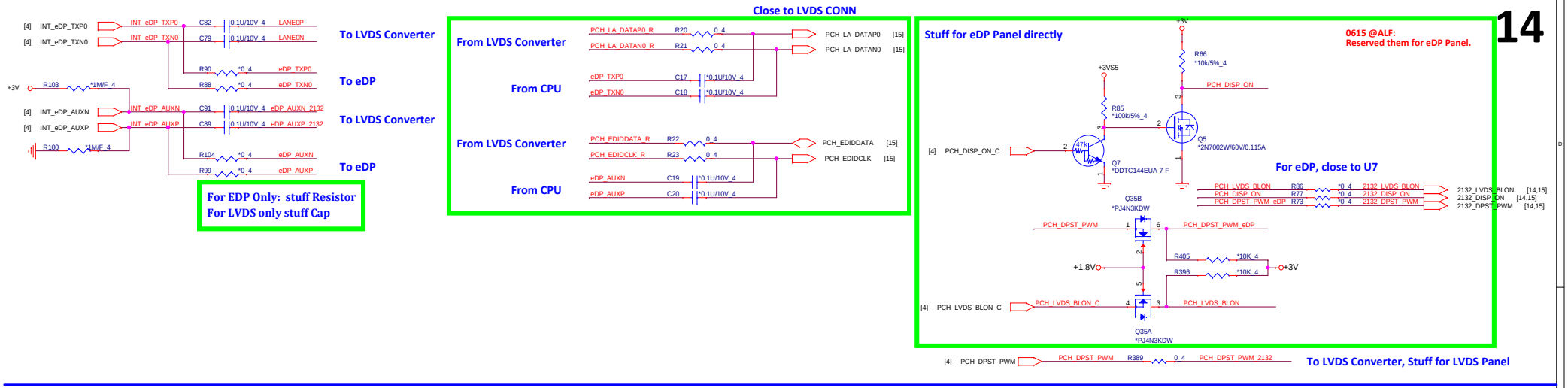

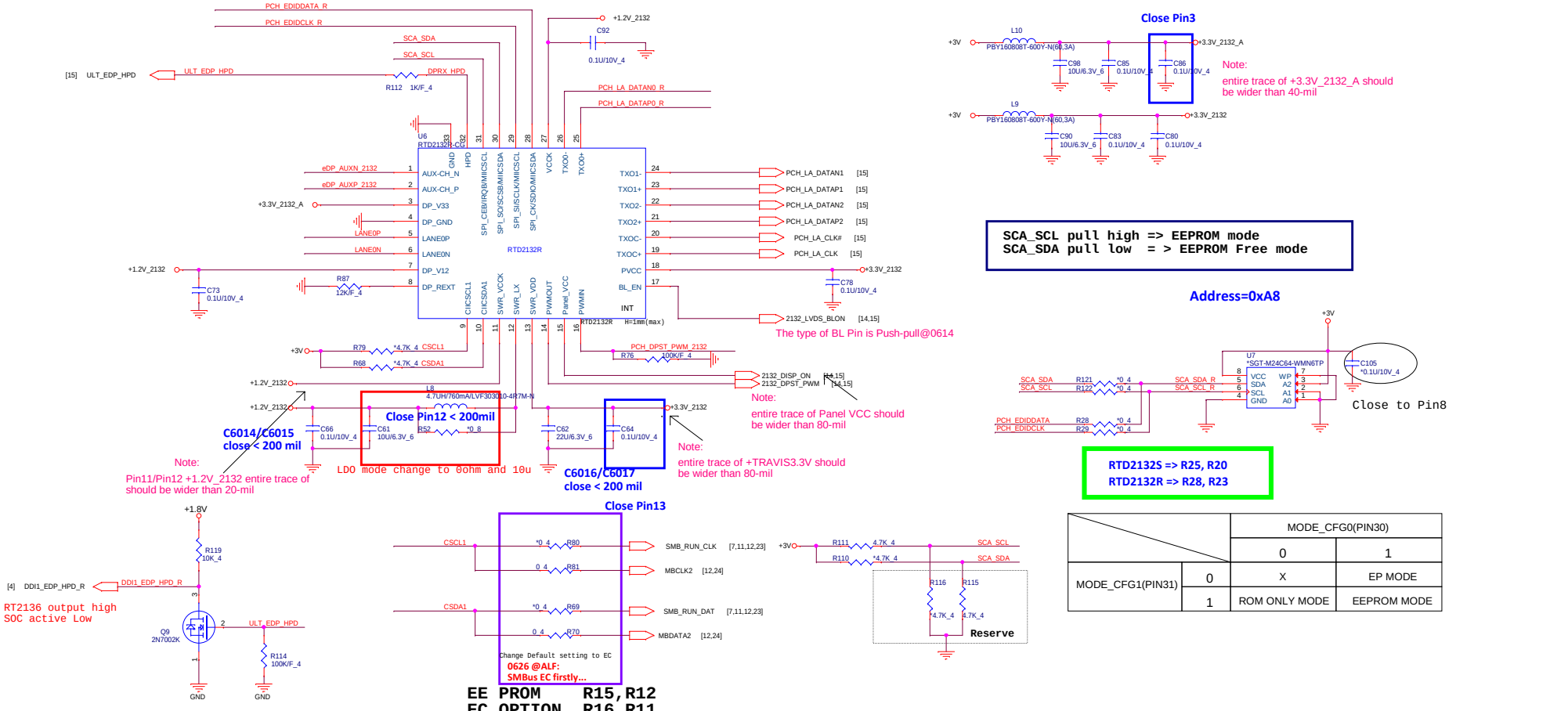

		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
C	LVDS converter RTD2132R	1A

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LVDS Conn.

80 mile trace

+3VLCD_CON
R12 0_8
+3V
C13 4.7U/6.3V_6
+LCDVCC
C23 *1U/6.3V_4
U1 *IC(5P) G5243AT11U
IN OUT GND ON/OFF INT
L2 *TI160808U600
C4 *10U/6.3V_6
C3 *0.01U/16V_4
C2 0.1U/10V_4
[14] 2132_DISP_ON
R16 100K/F_4

[14] 2132_DPST_PWM 0_4 R15 PCH_DPST_PWM_R
R6 100K/F_4
C12 *22P/50V_4

0615@ALF:
Need to Double check it,
does the Enable Signal can be a power supply for LVDS Panel?

Can't change to short
[24] EMU_LID
R18 0_4
D1 RB500V-40
R5 100K/F_4
C11 22P/50V_4
BLON_CON
[14] 2132_LVDS_BLON
R17 1K/F_4
R27 100K/F_4

D_MIC
[16] DIGITAL_D1 L6 FCM1608KF-301T02 DIGITAL_D1_R
[16] DIGITAL_CLK L5 FCM1608KF-301T02 DIGITAL_CLK_R
C26 *33P/50V_4 DIGITAL_D1
C25 *33P/50V_4 DIGITAL_CLK
C16 100P/50V_4 DIGITAL_D1_R
C21 100P/50V_4 DIGITAL_CLK_R

[14] PCH_EDIDDATA R31 4.7K/_4 Ra
[14] PCH_EDIDCLK R32 4.7K/_4 Rb
R33 *100K_4 Rc

For LVDS stuff Ra=4.7k,Rb=4.7k,Rc un-stuff
For eDP reserve Ra=100k,Rc=100k,Rb un-stuff

2132_LVDS_BLON R26 *1K_4
2132_DPST_PWM R30 *1K_4
Only for eDP reserve

0614 @ALF:
Changed the QCI P/N

CN1
LVDS CONN

[14] ULT_EDP_HPD
For EDP Only: Stuff Rd
For LVDS Only: Stuff Rc
R4 0_4
R11 *0_4
EDP_HPD_R
Rd
Rc

+3VLCD_CON
+3V
C24 1000P/50V_4
PCH_DPST_PWM_R
BLON_CON
PCH_EDIDCLK
PCH_EDIDDATA
[14] PCH_LA_DATAN0
[14] PCH_LA_DATAP0
[14] PCH_LA_DATAN1
[14] PCH_LA_DATAP1
[14] PCH_LA_DATAN2
[14] PCH_LA_DATAP2
[14] PCH_LA_CLK#
[14] PCH_LA_CLK
USBP_CCD- C
USBP_CCD+ C
DIGITAL_D1_R
DIGITAL_CLK_R
+3V
C6 0.01U/25V_4
C323 *4.7U/6.3V_6
C322 1000P/50V_4
+VIN_BLIGHT

DFWF30MR004
lvds-lvd-a30sfyg-30p-r
FOX DFWF30MR007 E0D
+VIN_BLIGHT

USB CAMERA
[21] USBP_CCD-
[21] USBP_CCD+
R25 *0_4
L4
USBP_CCD- C
USBP_CCD+ C
MCM2012B900GBE
R24 *0_4
SI modify

0625@ALF:
L12 changed to RC0805
footprint for A stage.
+VIN
L3 0_8
+VIN_BLIGHT
C15 0.1U/50V_6
C8 *4.7U/25V_8
C5 0.1U/50V_6
C1 0.01U/25V_4

HDMI Conn.

HDMI SMBus Isolation

+1.8V
R168 2.2K_4
Q15
[4] SDVO_CLK HDMI_SCL_R HDMI_SCLK
[4] SDVO_DATA HDMI_SDA_R HDMI_SDATA
R167 2.2K_4
PJ4N3KDW

Close to HDMI connector

0625@ALF:
Q32 Changed the P/N from BAM70020003 to BAM4N3K0000.
Because of the VGS, the range is 0.8~1.5V

PDG recommend 620ohm +/- 5%

+3V
Q16 2N7002K
DGPU_CI_HDMIP
R188 470/F_4 C_TX2_HDMI+
R186 470/F_4 C_TX2_HDMI-
R185 470/F_4 C_TX1_HDMI+
R182 470/F_4 C_TX1_HDMI-
R431 470/F_4 C_TX0_HDMI+
R429 470/F_4 C_TX0_HDMI-
R179 470/F_4 C_IN_CLK
R175 470/F_4 C_IN_CLK#
R189 100K/F_4
C221 0.1U/10V_4
Close to Q31

EMI Solution

C_TX2_HDMI+ R187 121/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R184 121/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R430 121/F_4 C_TX0_HDMI-
C_TXC_HDMI+ R177 121/F_4 C_TXC_HDMI-
R178 0_4
C_IN_CLK L14 C_TXC_HDMI+
C_IN_CLK# C_TXC_HDMI-
*MCM2012B900GBE
R176 0_4

+1.8V
R166 10K_4
[4] HDMI_HPD_CON
Q14 2N7002
HDMI_HPD
R169 100K/F_4

CN13
HDMI CONN
[4] IN_D2 C220 0.1U/10V_4 C_TX2_HDMI+
[4] IN_D2# C219 0.1U/10V_4 C_TX2_HDMI-
[4] IN_D1 C217 0.1U/10V_4 C_TX1_HDMI+
[4] IN_D1# C216 0.1U/10V_4 C_TX1_HDMI-
[4] IN_D0 C436 0.1U/10V_4 C_TX0_HDMI+
[4] IN_D0# C435 0.1U/10V_4 C_TX0_HDMI-
[4] IN_CLK C205 0.1U/10V_4 C_TXC_HDMI+ C_IN_CLK
[4] IN_CLK# C203 0.1U/10V_4 C_TXC_HDMI- C_IN_CLK#
RB500V-40
+5V_HDMIC
D3 D4 RB500V-40
5V_HSMBCK 5V_HSMBDT
R173 2.2K_4
R174 2.2K_4
HDMI_SCLK
HDMI_SDATA
C200 *10P/50V_4
C198 *10P/50V_4
+5V_HDMIC
HDMI_HPD L13 0_6 HDMI_DET_C
VC1 *TVM0G5R5M220R
C197 220P/50V_4
SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ GND2 D0 Shield D0- CK+ CK Shield CK- GND1 CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL2
20 23 22 21

0614 @ALF:
Changed the QCI P/N
& symbol to add 2 Pin for GNDs

40 MIL
40 mils
+5V
F1 FUSE1A6V_POLY
+5V_HDMIC
C201 0.1U/10V_4
VC2 *TVM0G5R5M220R
SSM14 spec is 40V 1A
[5,7,9,11,12,13,14,16,17,18,19,20,21,22,23,24,25,35,37] +3V
[6,8,19,20,22,23,24,26,27] +3VPCU
[16,18,19,20,22,25,35] +5V
[25,26,27,28,34,35] +VIN
[18,35] +12VALW
[16,20,25,27,28,29,32,33,34,35,37] +5VS5

+5V_HDMIC
C202 *0.01U/16V_4
for EMI request

PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD/HDMI/Camera/D-MIC	1A
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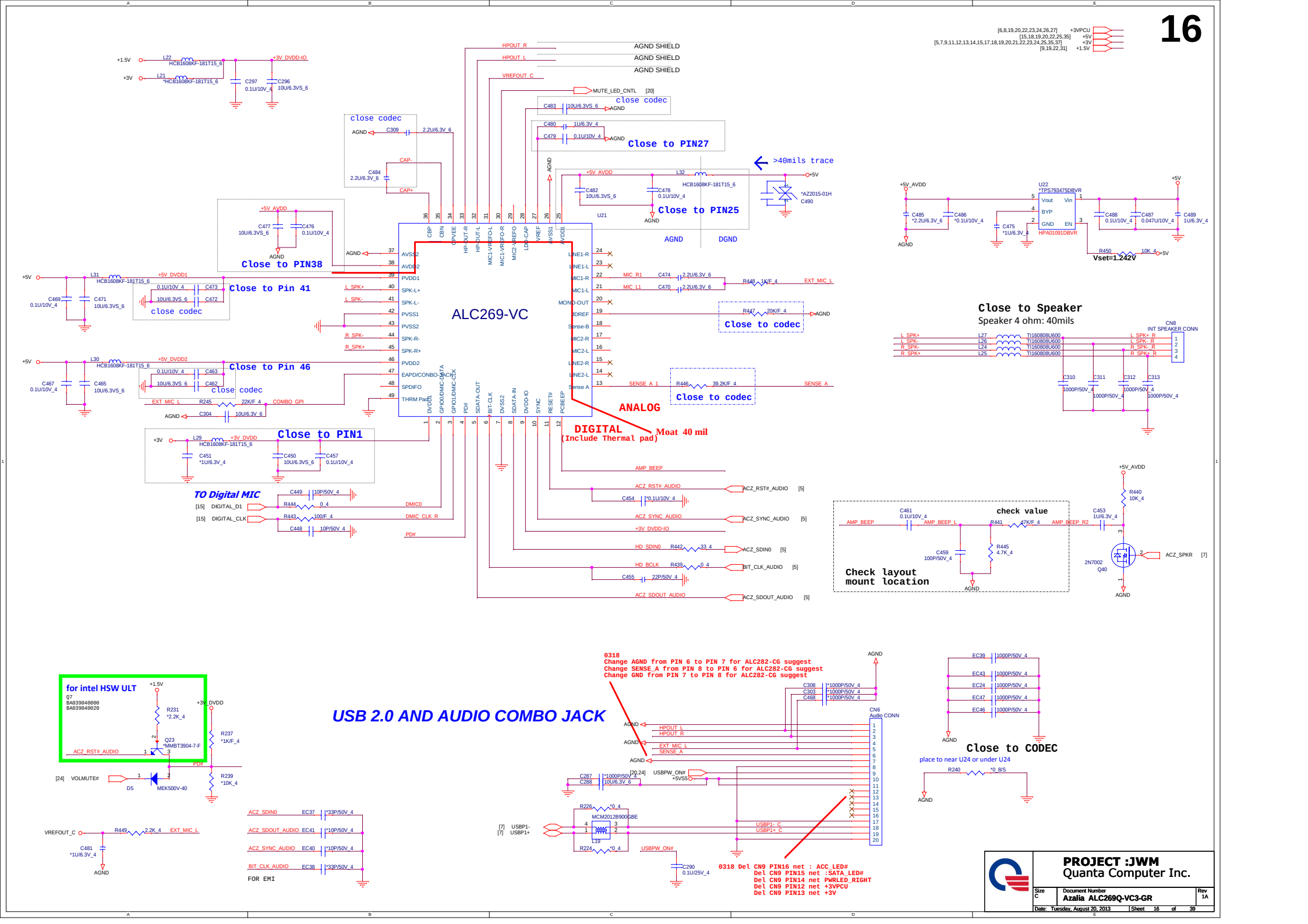

PROJECT :JWM Quanta Computer Inc.			
Size C	Document Number Azalia ALC269Q-VC3-GR		Rev 1A
Date: Tuesday, August 20, 2013	Sheet 16 of 39		

Does it need to reserver a EC Pin to control the ISOLATEB Pin?
Confirm it!! ALF@0531

For EMI 0 ~ 22 ohm

R49 *10/F_4 LAN_XTAL1 XTAL1
XTAL2 R48 0_4 LAN_XTAL25_IN [22]
Y1 *25MHZ +-10PPM
XTAL2
C54 *33P/50V_4
C48 *33P/50V_4

Switch Mode:Stuff L23 For RTL 8176
LDO Mode:Stuff R259 For RTL8166

Trace<30 mil
Width > 60 mil

Power trace Layout 寬度> 60mil

>60mil
+1.05V_LAN_REGOUT
*4.7UH,+-20%,650MA_1210
L7
>60mil
R51 *0_8
C65 *4.7U/6.3V_6
Cz C55 *0.1U/10V_4
Close to Choke L23
SWR mode need stuff C622 & Cz

Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3,8,22,30

+1.05V_LAN
Cc C47 *0.1U/10V_4
Cd C46 *0.1U/10V_4
Ce C58 0.1U/10V_4
Cf C39 0.1U/10V_4
Cg C44 1U/6.3V_4
C36 0.1U/10V_4

Place Cg & C621 close to each VDD10 pin30
*RTL8166EH Cg & C621 close pin30

U2
NS681684
MDI1+_1 TD+ TX+ MDI1+
MDI1-_1 TD- CMT TRA_V_DAC
R36 75/F_4 LAN_MCTG1 CT TX- MDI1-
MDI0+_1 RD+ RX- MDI0-
MDI0-_1 RD- CT TRA_V_DAC
R38 75/F_4 LAN_MCTG0 CT RX+ MDI0+
C332 10P/3KV_1808
C22 0.01U/25V_4

BOT: TST1284R LF DB0EL5LAN00

Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32

+3V_LAN
+3VLANVCC
C34 0.1U/10V_4 Ca
C42 0.1U/10V_4 Cb
C35 *4.7U/6.3V_6
C38 *4.7U/6.3V_6
Reserve

Place Cc and Cd close to each VDD33 pin-- 23, 32

C60 *4.7U/6.3V_6 Cc
C59 *0.1U/10V_4 Cd

Remove For Not Using SWR mode

[5,7,9,11,12,13,14,15,16,18,19,20,21,22,23,24,25,35,37] +3V
[22,35] +3VLANVCC

+1.05V_LAN
R41 2.49K/F_4 LANRSET
+3V_LAN
LAN_AMBLED# TP4
TP5
TP6
LAN_WLED#

U4
RTL8106E-CG
RSET VDD10 XTAL2 XTAL1 LED0
AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0/GPO LED2(LED1)
33 GND

Please add 9 GND VIAs
connection with thermal PAD

MDI0+ 1 MDIP0
MDI0- 2 MDIN0
VDD10 3 AVDD10(NC)
MDI1+ 4 MDIP1
MDI1- 5 MDIN1
6 MDIP2(NC)
7 MDIN2(NC)
8 AVDD10

RTL8106E-CG

REGOUT(NC) 24 +1.05V_LAN_REGOUT
VDDREG(VDD33) 23 DVDDL +3V_LAN
DVDD10(NC) 22 VDD10 +1.05V_LAN
LANWAKEB 21 PCIE_WAKE# PCIE_WAKE# [13,22,24]
ISOLATEB 20 ISOLATEB
PERSTB 19 P
HSON 18 PCIE_RXN2_LAN_L C57 0.1U/10V_4 PCIE_RXN2_LAN [5]
HSOP 17 PCIE_RXP2_LAN_L C56 0.1U/10V_4 PCIE_RXP2_LAN [5]
RSTB# PLTRST# [13,19,22,24,37]

MDIP3(NC) 9
MDIN3(NC) 10
AVDD33(NC) 11
CLKREQB 12
HSIP 13
HSIN 14
REFCLK_P 15
REFCLK_N 16

LAN_CLKRQ
CLK_PCIE_LANN CLK_PCIE_LANN [6]
CLK_PCIE_LANP CLK_PCIE_LANP [6]
PCIE_TXN2_LAN PCIE_TXN2_LAN [5]
PCIE_TXP2_LAN PCIE_TXP2_LAN [5]

+3V_LAN
[5] PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R40 0_4

+3V
R57 1K_4
ISOLATEB
R58 15K/F_4

if ISOLATEB pin
pull-low,the LAN
chip will not drive
it's PCI-E outputs
(excluding
PCIE_WAKE# pin)

LAN conn

TWD Type

RJ45

(White)
CN11
RJ45_CONN
LAN_WLED 9 LED_AMB_P A1
LAN_WLED# 10 LED_AMB_N A2
8 RX1-
7 RX1+
MDI1-_1 6 RX0-
5 TX1-
4 TX1+
MDI1+_1 3 RX0+
MDI0-_1 2 TX0-
MDI0+_1 1 TX0+
GND1 14
GND 13
LAN_AMBLED 11 LED_GRE_P B1
LAN_AMBLED# 12 LED_GRE_N B2
(Amber)
C339 68P/50V_4
R9 *0_6/S
R39 *0_6/S

+3VLANVCC R268 330_4 C336 1000P/50V_4 LAN_AMBLED
+3VLANVCC R273 330_4 C343 1000P/50V_4 LAN_WLED

PROJECT :JWM
Quanta Computer Inc.

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Reserve for EMI

SD_D0 EC23 *5.6P/16V_4
SD_D1 EC22 *5.6P/16V_4
SD_D2 EC26 *5.6P/16V_4
SD_D3 EC25 *5.6P/16V_4

	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

Share Pin SD / MMC

0625@ALF:
L5016 Swap Pin for Layout

[21] USBP_CRN
[21] USBP_CRP
R235 0_4
*MCM2012B900GBE
L23
R234 0_4
USBP_CRN_C
USBP_CRP_C

C307 1U/10V_4 V18

SD_D2_R R244 0_4 SD_D2
SD_D3_R R243 0_4 SD_D3

Close to chip pin

need colse to Chip
R242 6.2K/F_4
RTS5237_RREF
C301 *100P/50V_4

U10
RTS5170
RREF
DM
DP
3V3_IN
CARD_3V3
SDREG
GND
SP10 GPIO0 SP9 SP8 SP7 SP6
V18 XD_D7 SP14 SP13 SP12 SP11
XD_CD# SP1 SP2 SP3 SP4 SP5

SD_CMD_R R241 0_4 SD_CMD
SD_CLK_R R238 0_4 SD_CLK
C298 *5.6P/16V_4
SD_CD#

+3V
R236 0_8
+3VCARD
C293 4.7U/6.3V_6
C292 0.1U/10V_4
C291 1U/10V_4
USBP_CRN_C
USBP_CRP_C
3V3_IN

Close to chip pin

SD_WP
SD_D0_R R232 0_4 SD_D0
SD_D1_R R233 0_4 SD_D1

+3VCARD
C299 0.1U/10V_4
C300 *0.1U/10V_4
C306 10U/6.3V_6

CLOSE CONN

CARD READER

CN7
CARDREADER CONN
SD_D2 1 DAT2
SD_D3 2 DAT3
SD_CMD 3 CMD
SD_CD# 4 C/D
5 VSS1
+3VCARD 6 VDD
SD_CLK 7 CLK
8 VSS2
SD_D0 9 DAT0
SD_D1 10 DAT1
SD_WP 11 W/P
12 GND
13 GND
14 GND
15 GND

R3X Type

SATA ODD CONNECTOR

14" SATA ODD

Bypass CAP close conn

CN12
14 SATA ODD
TXP SATA_TXP14_C C430 0.01U/25V_4 SATA_TXP1 [5]
TXN SATA_TXN14_C C429 0.01U/25V_4 SATA_TXN1 [5]
RXN SATA_RXN14_C C425 0.01U/25V_4 SATA_RXN1 [5]
RXP SATA_RXP14_C C423 0.01U/25V_4 SATA_RXP1 [5]
DP ZERO_ODD_DP# R421 1 2 1K_4 ZERO_ODD_DP# [7]
+5V +5V_ODD
+5V
MD ZERO_ODD_DA# 0_4 R416
GND1
GND2
GND3
GND
GND
+3V
R417 10K_4
ODD_EJECT# [24]

+5V_ODD +5V
R420 0_8

0620@ALF:
Used the +5V Power Rail.

120 mils
+5V_ODD
C417 10U/6.3V_6
C416 0.1U/10V_4
C415 0.1U/10V_4
C420 0.1U/10V_4
C419 0.1U/10V_4

+12VALW
R419 *330K_6
Q38 *AO3404
C421 *0.1U/10V_4
+5V
+5V_ODD
R418 *22_8
C418 *0.027U/25V_6
Q37 *2N7002
Q36 *2N7002

0620@ALF:
BTM doesn't support Zero Power ODD.

[24] ZERO_PWR_ODD R415 *0_4

High : ODD power down
Low : ODD power on

TOP

PROJECT :JWM
Quanta Computer Inc.

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Custom	RTS5170-GRT&CR SOCKET	1A
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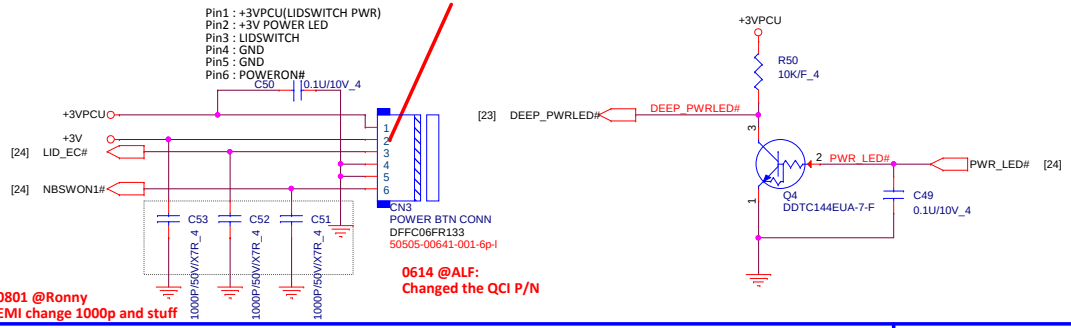
Power Botton Connector

0329
Change CN4 PIN2 from DEEP_PWRLED# to +3V for Power LED

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

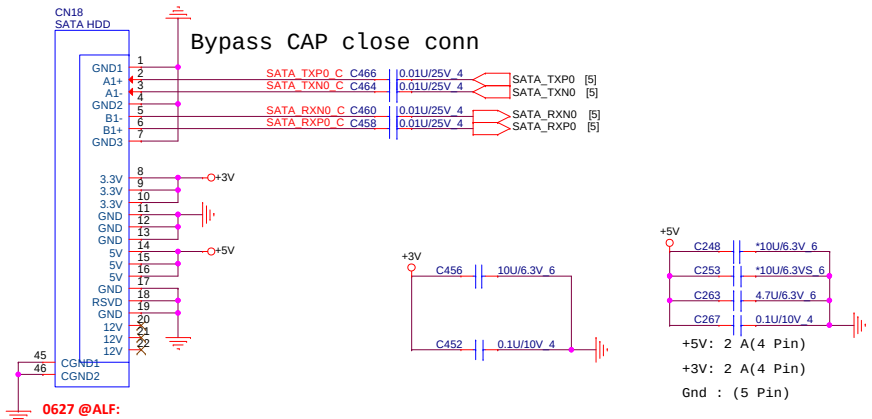


0801 @Ronny
EMI change 1000p and stuff

0614 @ALF:
Changed the QCI P/N

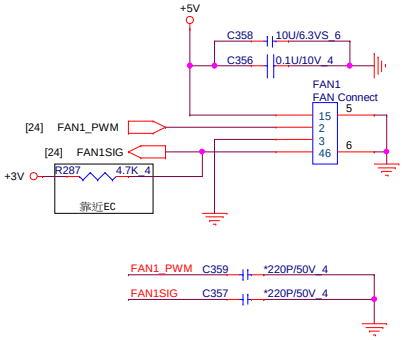
0327 :
DEL Touch Pad Connector CN7 for U83

SATA HDD Connector

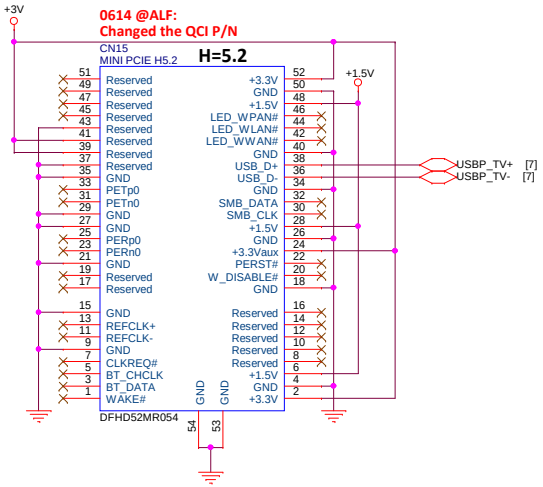


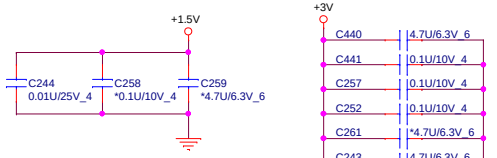
0627 @ALF:
Connect to GND PIN.

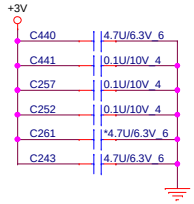
FAN



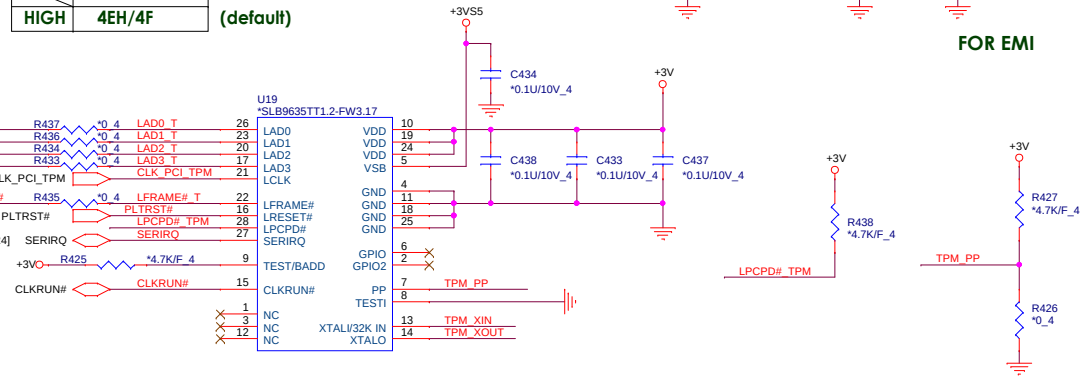
Mini PCI-E Card 2- Full size mSATA/TV Card







TPM (1.2)



[9,16,22,31] +1.5V
[5,7,9,11,12,13,14,15,16,17,18,20,21,22,23,24,25,35,37] +3V
[15,16,18,20,22,25,35] +5V
[6,8,20,22,23,24,26,27] +3VPCU
[18,35] +12VALW

PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/FAN/TPM	1A
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KEYBOARD Con.

0503 :
Change pin define and M/B keyboard connector follow R33

[24] MY[0..17] MY[0..17]
[24] MX[0..7] MX[0..7]

[16] MUTE_LED_CNTL
Q29 *2N7002K
MUTE_LED_CNTL_R1
R349 *10K/F_4

CN4 KB CONN
DFFC32FR027
bl135h-32rla-tand-32p-l-smt

MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17

[24] CAPSLED#
R356 *200/F_6 CAPSLED#_R
R361 *200/F_6 MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R
LED_PW
+3V

KEYBOARD PULL-UP

RP2 *10P8R-8.2K
RP1 *10P8R-8.2K
+3VPCU
MY13 MY12 MY3 MY6 MY14 MY11 MY10 MY15
MY1 MY5 MY0 MY9 MY2 MY4 MY7 MY8
R350 *8.2K_4 MY16
R355 *8.2K_4 MY17

0731@Ronny :
EC can internal pull-up, so un-stuff pull-up resistor

MY5 C373 220P/50V_4
MY6 C381 220P/50V_4
MY3 C384 220P/50V_4
MY7 C380 220P/50V_4
MY8 C379 220P/50V_4
MY9 C364 220P/50V_4
MY10 C395 220P/50V_4
MY11 C391 220P/50V_4
MY1 C375 220P/50V_4
MY2 C377 220P/50V_4
MY4 C378 220P/50V_4
MY0 C368 220P/50V_4
MX4 C365 220P/50V_4
MX6 C363 220P/50V_4
MX3 C371 220P/50V_4
MX2 C369 220P/50V_4
MX7 C362 220P/50V_4
MX0 C376 220P/50V_4
MX5 C366 220P/50V_4
MX1 C361 220P/50V_4
MY12 C385 220P/50V_4
MY13 C386 220P/50V_4
MY14 C387 220P/50V_4
MY15 C396 220P/50V_4
MY16 C397 220P/50V_4
MY17 C399 220P/50V_4

+5V
R369 *1K/F_4
R366 *200/F_6
WIRELESS_ON_R
[24] WIRELESS_ON
Q30 *DDTC144EUA-7-F

+5V
R373 *1K/F_4
R379 *200/F_6
WIRELESS_OFF_R
[24] WIRELESS_OFF
Q31 *DDTC144EUA-7-F

USB 2.0/3.0 Combo

0603 @ALF:
BTM only has one USB3.0 port, and define the CN20 (Bottom- left) at first

USB 3.0

C446 0.1U/10V_4
C447 470P/50V_4
VC4 *AVLC5S_4
C444 1000P/50V_4
L18 DLP11SN900HL2L
L20 *DLP11SN900HL2L
L17 *DLP11SN900HL2L
+5V_USBP0
1A
CN17 USB3.0 CONN
DFHS09FR442
usb-2ub4029-200201f-9p

[7] USBP0-
[7] USBP0+
USBP0-_C
USBP0+_C
[7] USB30_RX1-
[7] USB30_RX1+
USB30_RX1-_C
USB30_RX1+_C
[7] USB30_TX1-
[7] USB30_TX1+
C275 0.1U/10V_4 USB3_1-
C271 0.1U/10V_4 USB3_1+
USB30_TX1-_C
USB30_TX1+_C

USB3_1- R214 0_4 USB30_TX1-_C
USB3_1+ R210 0_4 USB30_TX1+_C
USB30_RX1- R228 0_4 USB30_RX1-_C
USB30_RX1+ R227 0_4 USB30_RX1+_C
USBP0- R223 *0_4 USBP0-_C
USBP0+ R225 *0_4 USBP0+_C
USBP_MB- R193 *0_4 USBP_MB-_C
USBP_MB+ R198 *0_4 USBP_MB+_C

0614 @ALF:
Changed the QCI P/N

USB 2.0

C240 0.1U/10V_4
C443 470P/50V_4
VC5 *AVLC5S_4
C445 1000P/50V_4
L15 DLP11SN900HL2L
+5V_USBP0
1A
CN14 USB2.0 CONN
DFHS04FR567
usb-2ub4029-200201f-9p

[7] USBP_MB-
[7] USBP_MB+
USBP_MB-_C
USBP_MB+_C

0617 @ALF:
Changed the QCI P/N for USB2.0 P/N

USB30_TX1-_C C276 *Clamp-Diode
USB30_TX1+_C C270 *Clamp-Diode
USBP0-_C C279 *Clamp-Diode
USBP0+_C C280 *Clamp-Diode
USB30_RX1-_C C284 *Clamp-Diode
USB30_RX1+_C C282 *Clamp-Diode
USBP_MB-_C C241 *Clamp-Diode
USBP_MB+_C C245 *Clamp-Diode

150 mils (Iout=3.7A)
U20
AP2820GMMTR-G1
VIN1 VIN2 EN GND OUT3 OUT2 OUT1 OC
+5VS5
+5V_USBP0
C442 220U/6.3V_6X4.5
[16,24] USBPW_ON#
Active Low
SI modify
VC3 *AVLC5S_4
C264 1U/6.3V_4
SOC_USB_OC0 [7]

0618 @ALF:
Add the OC PIN to Soc

0727 @Ronny:
change to 2.5A Power Switch

[16,25,27,28,29,32,33,34,35,37] +5VS5
[6,8,19,22,23,24,26,27] +3VPCU

PROJECT :JWM
Quanta Computer Inc.

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Custom	USB3.0/KB	1A
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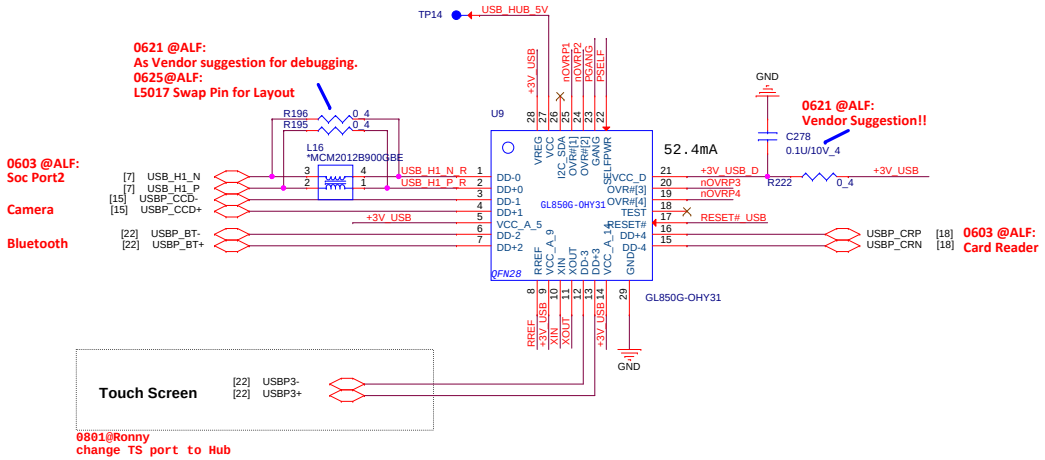

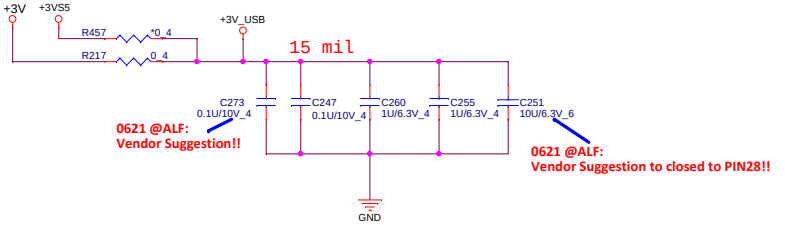

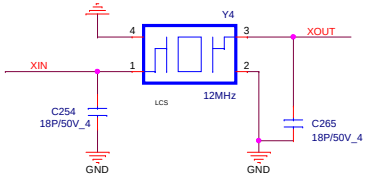

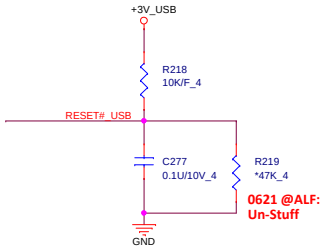

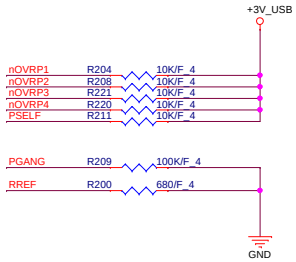

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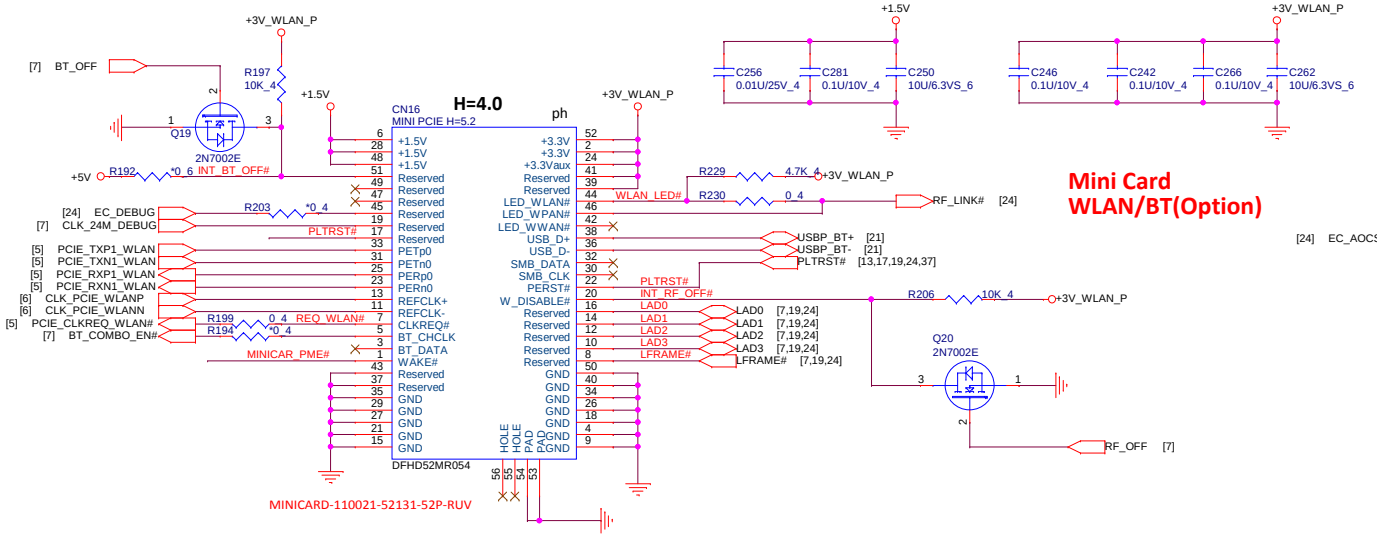
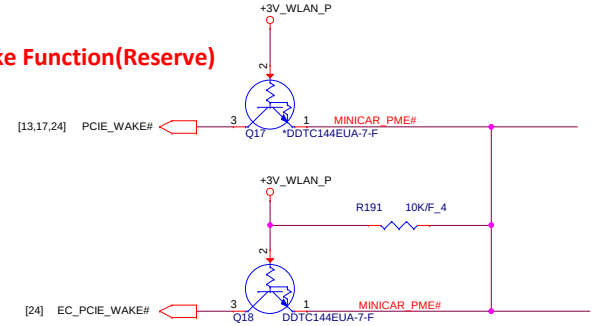
Mini Card WLAN/BT(Option)

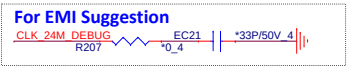


0614 @ALF:
Changed the QCI P/N

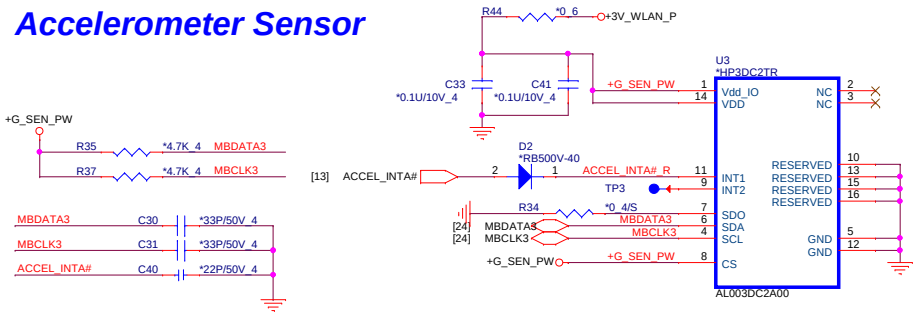
Support Wake Function(Reserve)



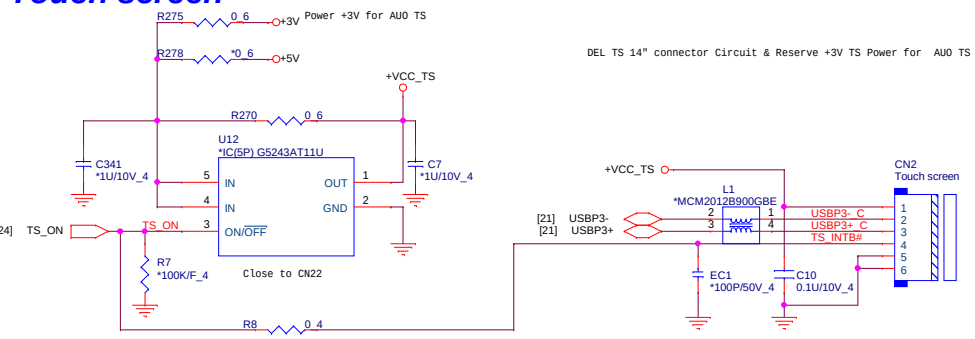
For EMI Suggestion



Accelerometer Sensor



Touch screen

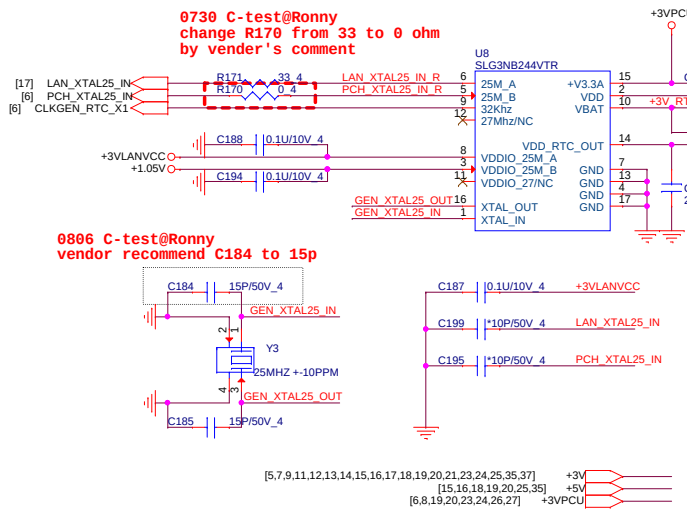


Green CLK Circuitry

0730 C-test@Ronny
change R170 from 33 to 0 ohm
by vender's comment

20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..

0806 C-test@Ronny
vendor recommend C184 to 15p



JWM	P/N
UMA	AL3NB244000

PROJECT :JWM
Quanta Computer Inc.

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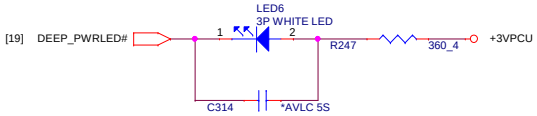
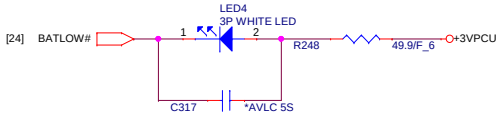
LED Status

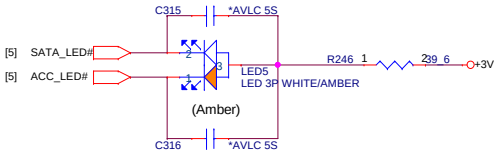
PWR LED



BAT LED



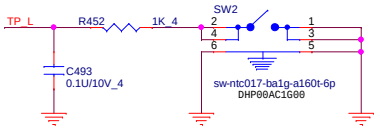
SATA LED



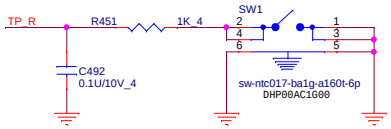
Function Botton

0327 :
ADD SW1/SW2/R14/R5/C14/C21 Function Botton for JWU

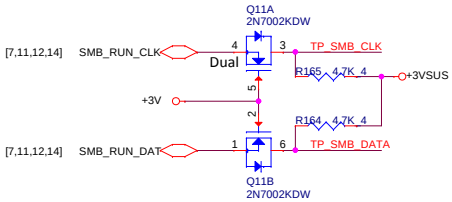
Left



Right

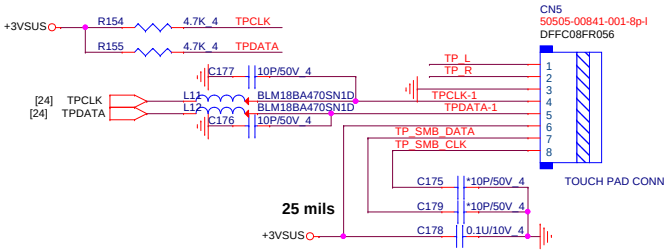


Touch Pad Connector



To Touch pad

0327 :
ADD Touch Pad Connector CN27 for JWU



TOP

U11
KB3940Q A1

+3VPCU

500mA

C321 0.1U/10V_4
C328 0.1U/10V_4
C351 0.1U/10V_4
C340 0.1U/10V_4
C338 0.1U/10V_4
C350 0.1U/10V_4
C342 0.1U/10V_4
C346 0.1U/10V_4
C345 0.1U/10V_4
C319 0.1U/10V_4

VCC1 9
VCC2 22
VCC3 33
VCC4 96
VCC5 111
VCC6 125
AVCC 67
+3VPCU_EC

+3VPCU_EC — L28 BLM18BA470SN1D — +3VPCU
C320 4.7U/6.3V_6

SERIRQ 3
LFRAME# 4
LAD0 10
LAD1 8
LAD2 7
LAD3 5
PCICLK 12
PCIRST#/GPIO5 13
CLKRUN# 38
SCI/GPIOE 20
GA20/GPIO0 1
KBRST/GPIO1 2
ECRST 37

[13,19] SERIRQ
[7,19,22] LFRAME#
[7,19,22] LAD0
[7,19,22] LAD1
[7,19,22] LAD2
[7,19,22] LAD3
[7] CLK_24M_KBC
[13,17,19,22,37] PLTRST#
[7,19] CLKRUN#
[13] SIO_EXT_SCI#
SIO_EXT_SCI#
R271 10K_4 EC_GA20
R269 10K_4 RCIN#
+3V
3920_RST#

0611 @ALF:
follow W03

KSI0/GPIO30 55
KSI1/GPIO31 56
KSI2/GPIO32 57
KSI3/GPIO33 58
KSI4/GPIO34 59
KSI5/GPIO35 60
KSI6/GPIO36 61
KSI7/GPIO37 62

[20] MX0
[20] MX1
[20] MX2
[20] MX3
[20] MX4
[20] MX5
[20] MX6
[20] MX7

KSO0/GPIO20 39
KSO1/GPIO21 40
KSO2/GPIO22 41
KSO3/GPIO23 43
KSO4/GPIO24 44
KSO5/GPIO25 45
KSO6/GPIO26 46
KSO7/GPIO27 47
KSO8/GPIO28 48
KSO9/GPIO29 49
KSO10/GPIO2A 50
KSO11/GPIO2B 51
KSO12/GPIO2C 52
KSO13/GPIO2D 53
KSO14/GPIO2E 54
KSO15/GPIO2F 81
KSO16/GPIO48 82
KSO17/GPIO49

[20] MY0
[20] MY1
[20] MY2
[20] MY3
[20] MY4
[20] MY5
[20] MY6
[20] MY7
[20] MY8
[20] MY9
[20] MY10
[20] MY11
[20] MY12
[20] MY13
[20] MY14
[20] MY15
[20] MY16
[20] MY17

AD0/GPI38 63 TEMP_MBAT — TEMP_MBAT [26]
AD1/GPI39 64 SOC_THERM_1
AD2/GPI3A 65 SOC_THERM_2
AD3/GPI3B 66 SYS_I — SYS_I [24,26]

DA0/GPO3C 68 — LAN_POWER [35]
DA1/GPO3D 70 DGPU_PROCHOT_EC# — TP16
DA2/GPO3E 71 BATSHIP — BATSHIP [26]
DA3/GPO3F 72 PCH_PCIE_WAKE# — PCIE_WAKE# [13,17,22]

PWM1/GPIOF 21 FB_CLAMP — TP18
PWM2/GPIO10 23 ZERO_PWR_ODD — ZERO_PWR_ODD [18]

FANPWM1/GPIO12 26 FAN1_PWM — FAN1_PWM [19]
FANPWM2/GPIO13 27 FB_CLAMP_TGL_REQ#_EC — TP17
FANFB1/GPIO14 28 FAN1SIG — FAN1SIG [19]
FANFB2/GPIO15 29 — TS_ON [22]

SCL1/GPIO44 77 MBCLK — MBCLK [26]
SDA1/GPIO45 78 MBDATA — MBDATA [26]
SCL2/GPIO46 79 MBCLK2 — MBCLK2 [12,14]
SDA2/GPIO47 80 MBDATA2 — MBDATA2 [12,14]

for Battery charge/charge
for DDR Thermal IC / eDP Convertor

GPIO4 6 SUSB# — SUSB# [13]
GPIO7 14 HWPG — HWPG [35,37]
GPIO8 15 H_PROCHOT#_EC

GPIOA 16 SUSC# — SUSC# [13]
GPIOB 17 SUSACK#_EC — TP19
GPIOC 18 — EC_AOCS# [22]
GPIOD 19 NBSWON1# — NBSWON1# [19]
GPIO11 25 — EMU_LID [15]
GPIO16 30 R253 *0_4/S — EC_DEBUG [22]
GPIO17 31 — RSMRST#_PWR [13,33]
GPIO18 32 SIO_EXT_SMI# — SIO_EXT_SMI# [13]

GPIO19 34 VRON — VRON [34]
GPIO1A 36 DGPU_PROCHOT# — TP15

For GPU thermal
For Gsensor
For Touch-Pad

TP20 TP21 EC_GPUT_CLK 83 EC_GPUT_DATA 84
[22] MBCLK3 85
[22] MBDATA3 86
[23] TPCLK TPCLK 87
[23] TPDATA TPDATA 88

PSCLK1/GPIO04A
PSDAT1/GPIO04B
PSCLK2/GPIO04C
PSDAT2/GPIO04D
PSCLK3/GPIO04E
PSDAT3/GPIO04F

RD/GPIO5B 119
WR/GPIO5C 120
SPICS/GPIO5A 128
SELIO/GPIO50 89
AD5/GPIO43 76
D0/GPXD0 109
D1/GPXD1 110
D2/GPXD2 112
D3/GPXD3 114
D4/GPXD4 115
D5/GPXD5 116
D6/GPXD6 117
D7/GPXD7 118

BIOS_RD# 119
BIOS_WR# 120
BIOS_CS# 128
SLP_S0#_EC 89
ACIN 76
PCI_SERR# 109
EC_GPXD1 110

[13] PCH_SLP_S0_N — R19 *0_4 — [26] ACIN
TP22
TP23
[6] SUSWARN#_EC
[22] RF_LINK#
[13] SLP_SUS#_EC
[5] EN_OVERRIDE
[13] DPWROK_EC
TP2
EN_OVERRIDE
EC_PECI_R

AD6/CIR_RX/GPIO40 73 EC_PCIE_WAKE# — EC_PCIE_WAKE# [22]
AD7/GPIO41 74 THRM_MOINTOR — THRM_MOINTOR [8]
AD4/GPIO42 75 GPIO42_EC
GPIO52 90 DNBSWON# — DNBSWON# [13]
GPIO53 91 CAPSLED# — CAPSLED# [20]
GPIO54 92 PWR_LED# — PWR_LED# [19]
GPIO55 93 EC_PWROK — EC_PWROK [2,13]
GPIO56 95 RSMRST# — RSMRST# [13]
GPIO57 121 VOLMUTE# — VOLMUTE# [16]
GPIO58 126 BIOS_SPI_CLK
GPIO59 127 LID_EC# — LID_EC# [19]

C344 *10P/50V_4

[16,20] USBPW_ON#
[28,35] SUSON
[26,34] MAINON
[28,35] SLP_SUS_ON
[27] S5_ON
USBPW_ON# 97
SUSON 98
MAINON 99
100
101
R282 102
R283 103
104
105
106
107
108

A0/GPXA0
A1/GPXA1
A2/GPXA2
A3/GPXA3
A4/GPXA4
A5/GPXA5
A6/GPXA6
A7/GPXA7
A8/GPXA8
A9/GPXA9
A10/GPXA10
A11/GPXA11

[8] THRM_MOINTOR1
[24,26] SYS_I
0_4 *0_4
New Thermal Protect
THRM_ALERT_HW#1
[18] ODD_EJECT#
TP1
MBATLED0#
[23] BATLOW#
[20] WIRELESS_ON
[20] WIRELESS_OFF

GPIO5E 123 CRY2 C352 *22P/50V_4
GPIO5D 122 CRY1 R284 0_4 — AC_PRESENT_EC [5]

GND1 11
GND2 24
GND3 35
GND4 94
GND5 113
AGND 69 R250 0_6

V18R 124
C28 0.1U/10V_4
C27 4.7U/6.3V_6

Need Change New PN

0325 :
Change U12 PIN105 from MBATLED0# to TP
Change U12 PIN106 from AC_LED_ON# to BATLOW#

0603 @ALF:
Already changed the EC Part Number to KB3940Q A1

CRY2 R286 *0_4 PCH_SUSCLK [13]
R285 *100K_4

THRM_MOINTOR
THRM_MOINTOR1
C349 0.1U/10V_4
C324 0.1U/10V_4

3920_RST# — Q24 METR3904-G — R280 4.7K_4 — +3V
OVT_DETC — D6 — EC_PWROK — MEK500V-40
R276 10K/F_4 — +3VPCU
THRM_ALERT_HW#1

Open Drain need pu high

0618 @ALF:
1. After meeting with NB5 EC and BIOS team,
aslo confirmed Intel Side, BTM doesn't support "THERMTRIP"
2. Delete all parts

H_PROCHOT# — H_PROCHOT# [5,34]
H_PROCHOT#_EC — R10 *10K/F_4 — Q3 2N7002K — C9 *47P/50V_4

+3VPCU
R261 10K/F_4 NBSWON1#
R258 4.7K_4 MBCLK
R260 4.7K_4 MBDATA
R254 10K/F_4 EC_PCIE_WAKE#
R277 47K/F_4 LID_EC#

+3V
R281 *10K_4 EN_OVERRIDE
R266 4.7K_4 EC_GPUT_CLK
R267 4.7K_4 EC_GPUT_DATA
R252 4.7K_4 DGPU_PROCHOT_EC#
R262 4.7K_4 MBCLK2
R264 4.7K_4 MBDATA2

HWPG C331 0.1U/10V_4
3920_RST#
+3VPCU R249 47K/F_4 C318 0.1U/10V_4
C335 *10P/50V_4 R265 *10_4 CLK_24M_KBC

Adapter Type check

0614 @ALF:
After meeting with NB5, reserved them first.
0617@ALF:
Delete all parts for CPU NTC thermal policy.

For SoC Thermal

Layout Notes:
Closed to Soc, one is on TOP, other is on Left

SOC_THERM_1
+3VPCU — R307 24.9K/F_4 — RT1 47K/F_4_NTC
R411 24.9K/F_4 — RT2 47K/F_4_NTC
SOC_THERM_2
GND

0617@ALF:
DTS Temp firstly for EC, this is backup solution if system hang up.
EC can compare this with DTS.

NBSWON1# — SW3 — C348 0.1U/10V_4
sw-ntc017-ba1g-a160t-6p
DHP00AC1G00

0620@ALF:
Add one power buttom for bring up.

Reserve for ENE Hold time issue

MBCLK2 C330 *10P/50V_4
MBDATA2 C333 *10P/50V_4
MBCLK C327 *10P/50V_4
MBDATA C329 *10P/50V_4
EC_GPUT_CLK C334 *10P/50V_4
EC_GPUT_DATA C337 *10P/50V_4

Vender	Size	P/N
WND	128KB	AKE35ZN0N00 (W25X10CLSNIG)
MAX	128KB	AKE35FN0Z02 (MX25L1006EMI-10G)
Socket		

Adapter select for EC

+3VPCU — R256 *10K_4 — GPIO42_EC — R257 *10K_4

DIS Hi ==> (90W)
UMA Low ==> (65W)

0614 @ALF:
After meeting with NB5, reserved them first.

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

0615 @ALF:
EMI Suggestion to add 22ohm

BIOS_CS# 1
BIOS_SPI_CLK 6 — BIOS_SPI_CLK_R
BIOS_WR# R274 22_4 5
BIOS_RD# 2
U13 AKE35ZN0N00 soic8-6-1_27-pm25lv010a
CE# VDD 8
SCK
SI
SO HOLD# 7 SPI_7P R279 10K/F_4
SPI_3P 3
WP# VSS 4
+3VPCU R272 10K/F_4
C347 0.1U/10V_4

0615 @ALF:
Changed the SPI Winbond Part

[5,7,9,11,12,13,14,15,16,17,18,19,20,21,22,23,25,35,37] +3V
[6,8,19,20,22,23,26,27] +3VPCU

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Screw Holes

Stuff NUT Location:

0625 @ALF:
Added 2 pcs Holes for JWM Fan Module.

H7
FBAJ2003010

H9
FBAJ2003010

0701 @ALF:
Same as BM5, Stuff NUT on TOP side

FAN nut
Nut PN:MBFF4001010

H6
H-TC393BIC315D146P2

0625 @ALF:
Modified the Hole's FP.

0729 @ALF:
change to BOT side

Mini-PCIe Nut for TV Card
Nut PN:MBZR7001010

0625 @ALF:
Modified the Hole's FP.

0729 @Ronny:
delete Hole

SoC Bracket

SOC Bracket

HOLE1
*INTEL-CPU-BKT-ULV

0626 @ALF:
New add

PCB Fan Hole (Internal)

H8
*o-jwm-1

0626 @ALF:
Modified the Hole's FP.

GND PAD

PAD3

PAD1

0729 :
ADD PAD3

0805 :
remove PAD2

0329 :
ADD H35,H36,H37,PAD1 HOLE

0402 :
ADD H38 HOLE

H13
*H-C236D118P2

H19
*H-TC118BIC197D118PB

H1
*H-C236D118P2

H3
*H-C315D118P2

0625 @ALF:
Modified the Hole's FP.

0625 @ALF:
Modified the Hole's FP.

H11
*H-C394D118P2

H10
*H-C394D118P2

H18
*H-C394D118P2

H15
*H-C236D98P2

0729 @Ronny:
Remove Hole H4.

H5
*H-C315D118P2

H12
*H-C393D354P2

H17
*H-C394D118P2

H16
*H-C394D118P2

H2
*H-C315D102P2

EMI

0626 @ALF:
EMI Suggestion for Power Shape

25

+VIN Shape on SVCC Layer

0.1uF Caps * 6pcs

+VIN	C272	0.1U/25V_4
+VIN	C274	0.1U/25V_4
+VIN	C182	0.1U/25V_4
+VIN	C491	0.1U/25V_4
+VIN	C67	0.1U/25V_4
+VIN	C14	0.1U/25V_4

+3VS5 Shape on SVCC Layer

0.1uF Caps * 4pcs

+3VS5	C355	0.1U/25V_4
+3VS5	C410	0.1U/25V_4
+3VS5	C231	0.1U/25V_4
+3VS5	C269	0.1U/25V_4

+5VS5 Shape on SVCC Layer

0.1uF Caps * 6pcs

+5VS5	C164	0.1U/25V_4
+5VS5	C295	0.1U/25V_4
+5VS5	C360	0.1U/25V_4
+5VS5	C29	0.1U/25V_4
+5VS5	C283	0.1U/25V_4
+5VS5	C286	0.1U/25V_4

+5V Shape on SVCC Layer

0.1uF Caps * 4pcs

+5V	C32	0.1U/25V_4
+5V	C233	0.1U/25V_4
+5V	C289	0.1U/25V_4
+5V	C302	0.1U/25V_4

+3V Shape on SVCC Layer

0.1uF Caps * 4pcs

+3V	C305	0.1U/25V_4
+3V	C294	0.1U/25V_4
+3V	C285	0.1U/25V_4
+3V	C45	0.1U/25V_4

+VCC_GFX Shape on SVCC Layer

1000PF Caps * 2pcs

+VCC_GFX	C409	1000P/50V/X7R_4
+VCC_GFX	C406	1000P/50V/X7R_4

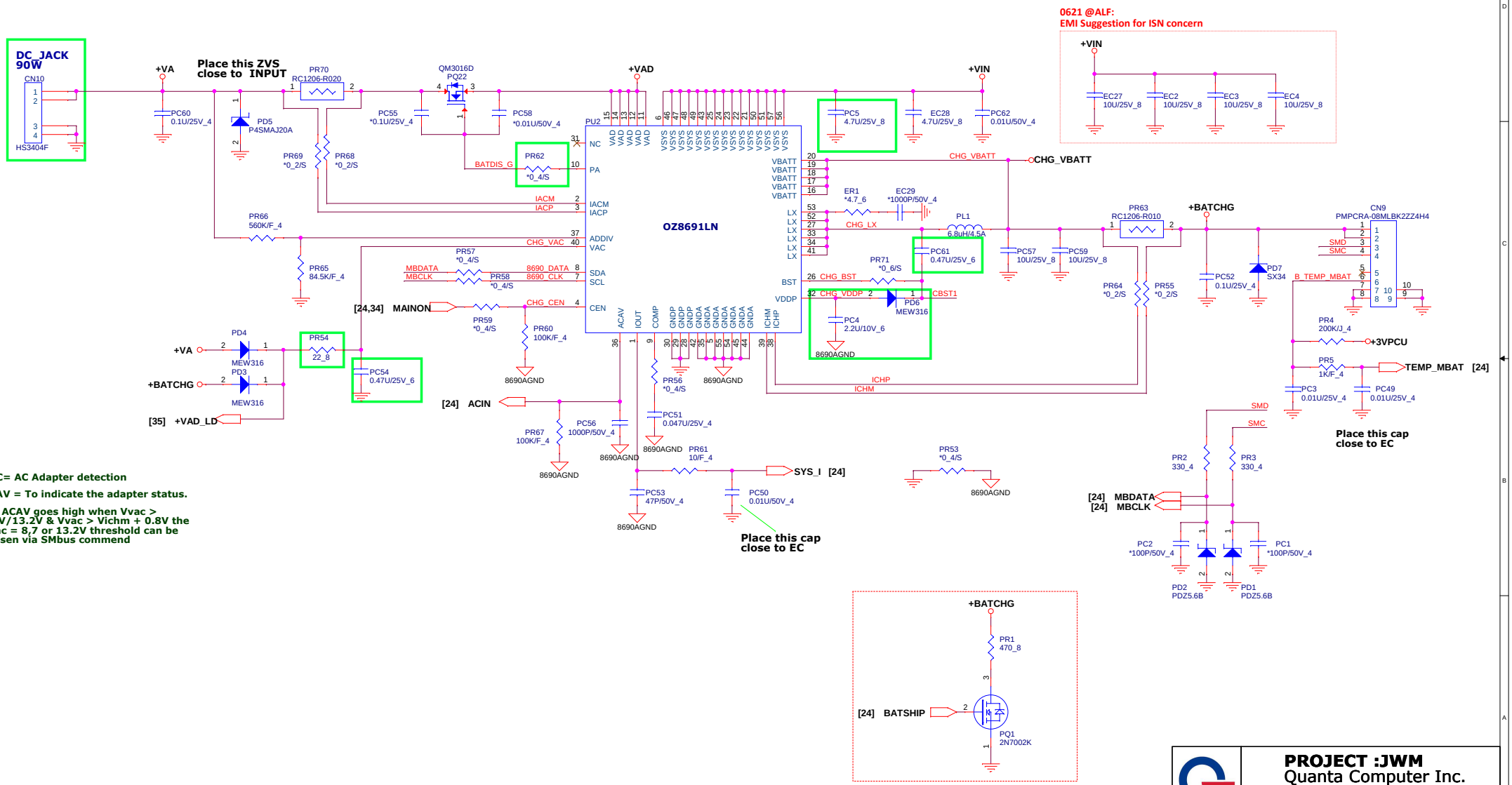
0731@Ronny: EMI add cap at Power source side

+VA	EC52	2200P/50V_4
+VAD	EC53	2200P/50V_4
+VAD	EC55	2200P/50V_4
+VAD	EC54	0.1U/25V_4
+VAD	EC56	0.1U/25V_4
CHG_VBATT	EC57	2200P/50V_4
CHG_VBATT	EC59	2200P/50V_4
CHG_VBATT	EC58	0.1U/25V_4
CHG_VBATT	EC60	0.1U/25V_4
+BATCHG	EC61	2200P/50V_4
+BATCHG	EC62	2200P/50V_4

PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
B	Screw HOLEs / EMI	1A

Date: Tuesday, August 20, 2013 | Sheet 25 of 39



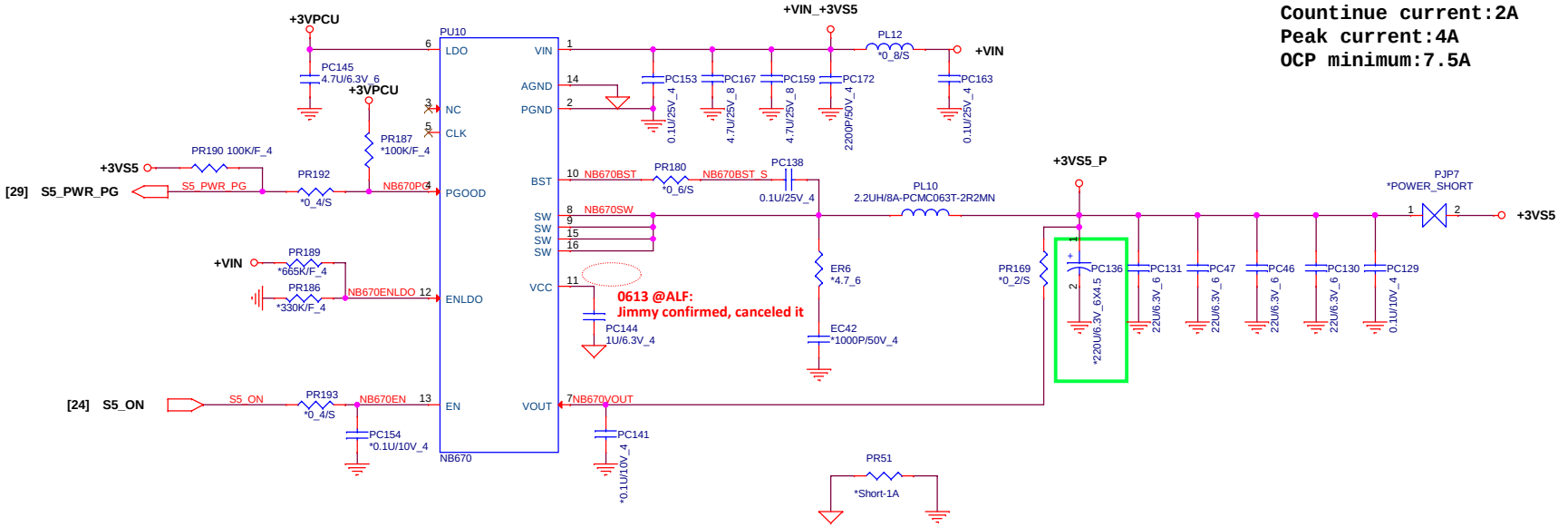
VAC= AC Adapter detection

ACAV = To indicate the adapter status.

Pin ACAV goes high when Vvac > 8.7V/13.2V & Vvac > Vichm + 0.8V the Vvac = 8,7 or 13.2V threshold can be chosen via SMbus commend

PROJECT :JWM Quanta Computer Inc.		
Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
Date: Tuesday, August 20, 2013	Sheet 26 of 39	

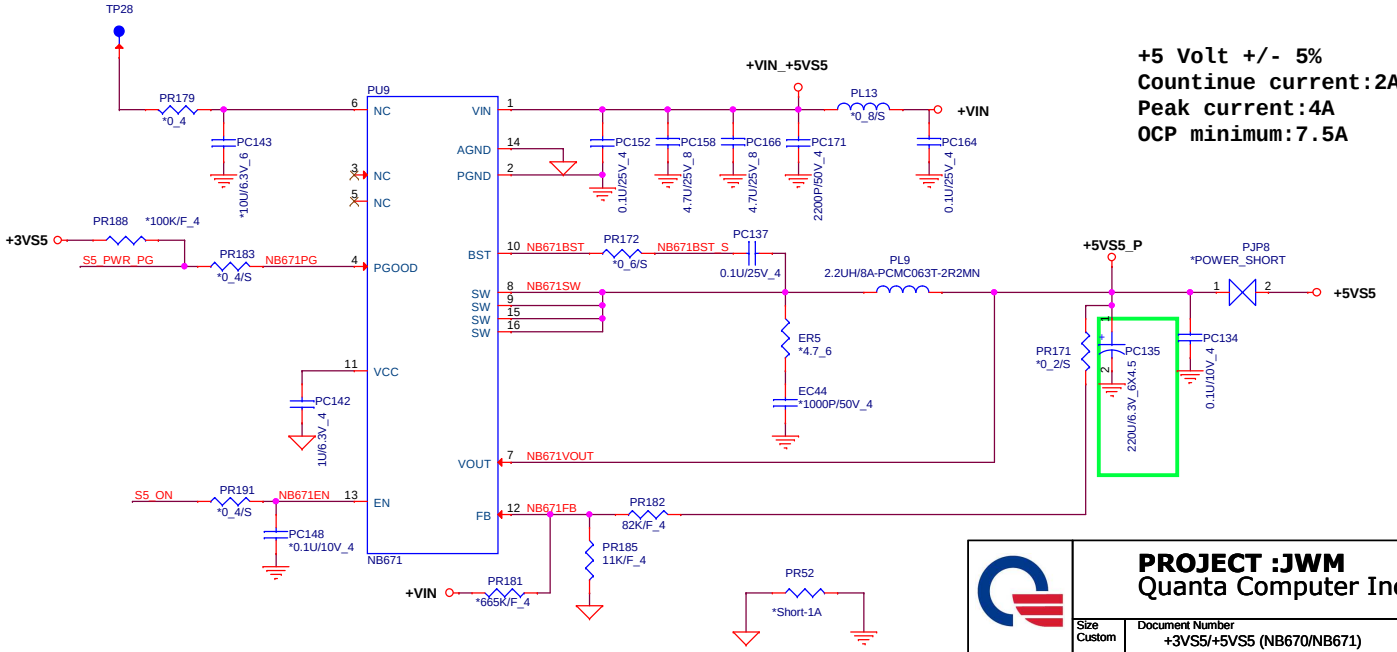
+3.3 Volt +/- 5%
Countinue current:2A
Peak current:4A
OCP minimum:7.5A



0613 @ALF:
Aftered Power Jimmy confirmed, it is no need.

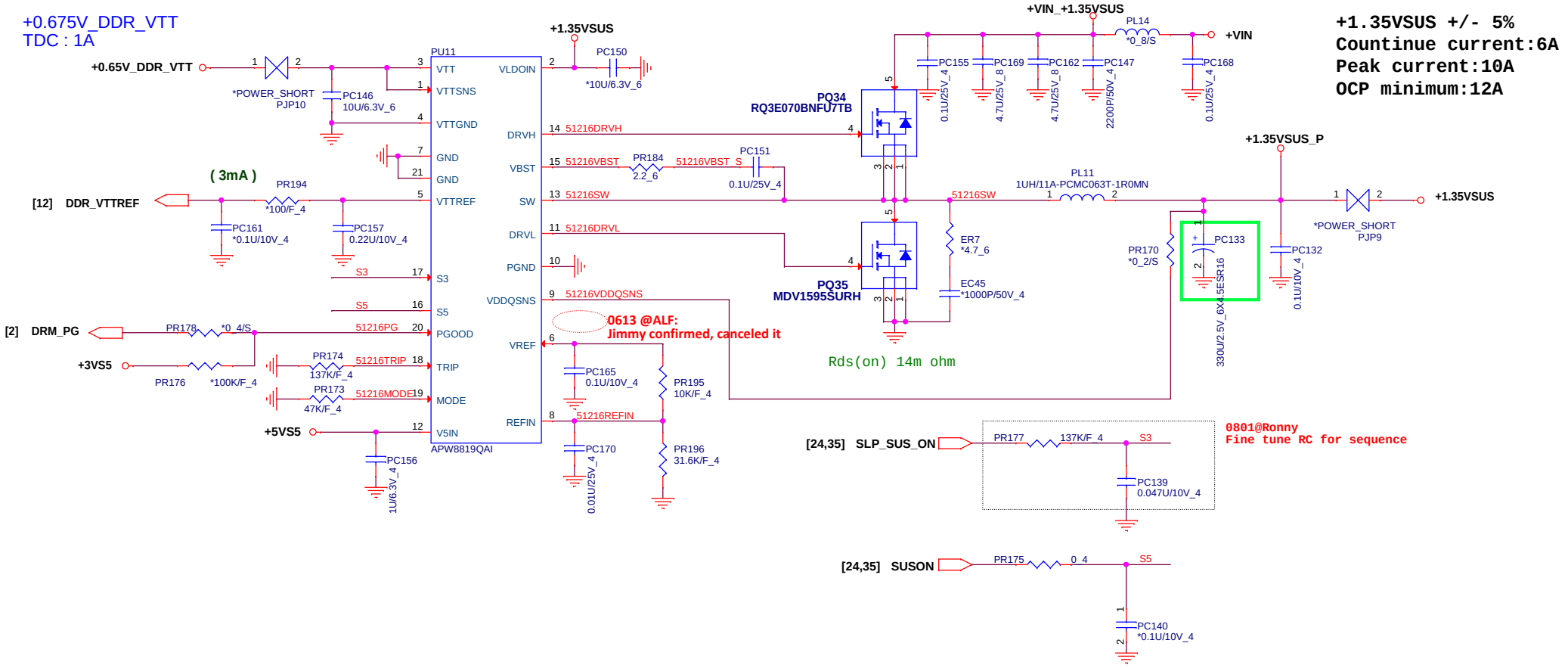
0611 @ALF:
Should be canceled, because has discharge IC.

+5 Volt +/- 5%
Countinue current:2A
Peak current:4A
OCP minimum:7.5A



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3VS5/+5VS5 (NB670/NB671)	1A
Date: Tuesday, August 20, 2013	Sheet 27 of 39	

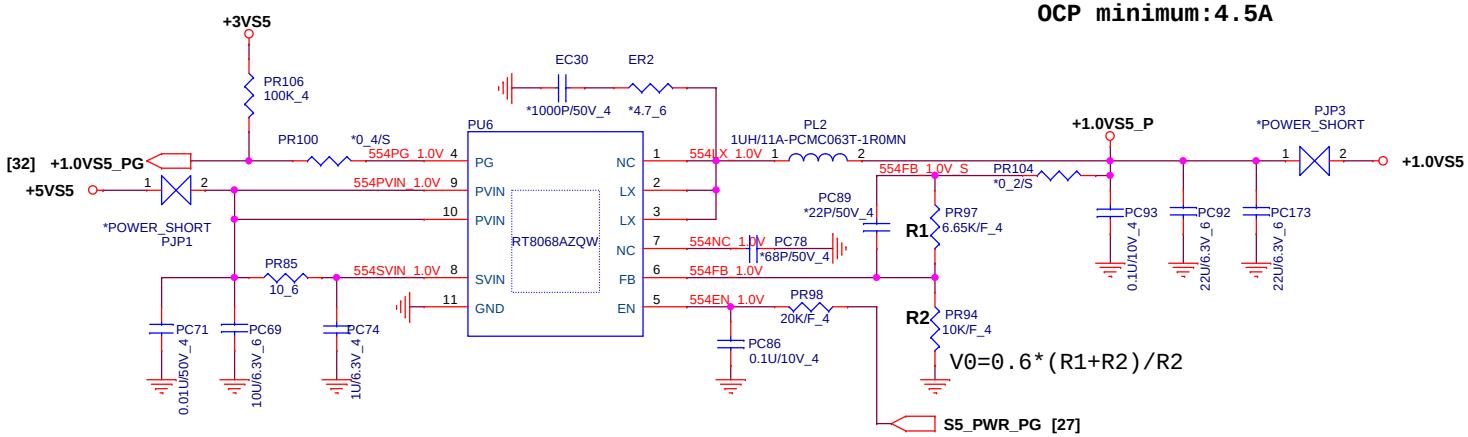


PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
B	1.35/0.675V(TPS51216RUKR)	1A

Date: Tuesday, August 20, 2013 Sheet 28 of 39

+1.0V_ALW Volt +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum:4.5A

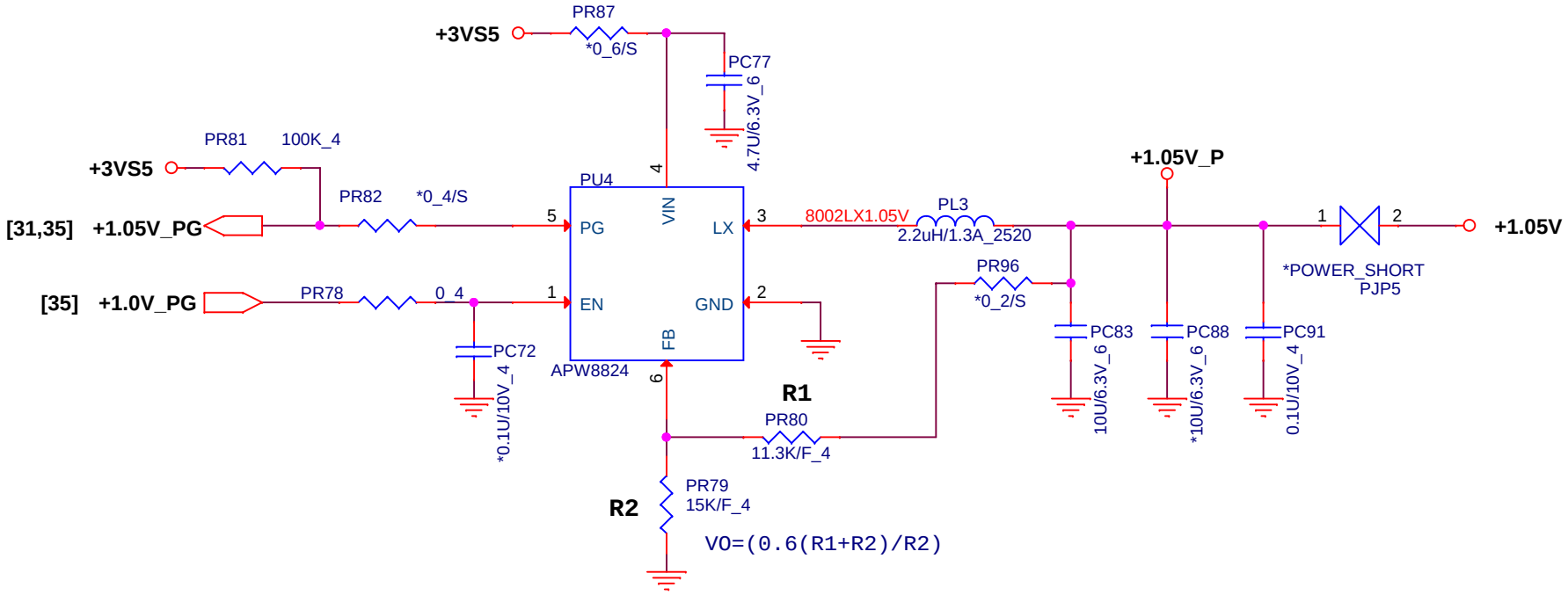


PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.0VS5(APW8804)	1A

Date: Tuesday, August 20, 2013 Sheet 29 of 39

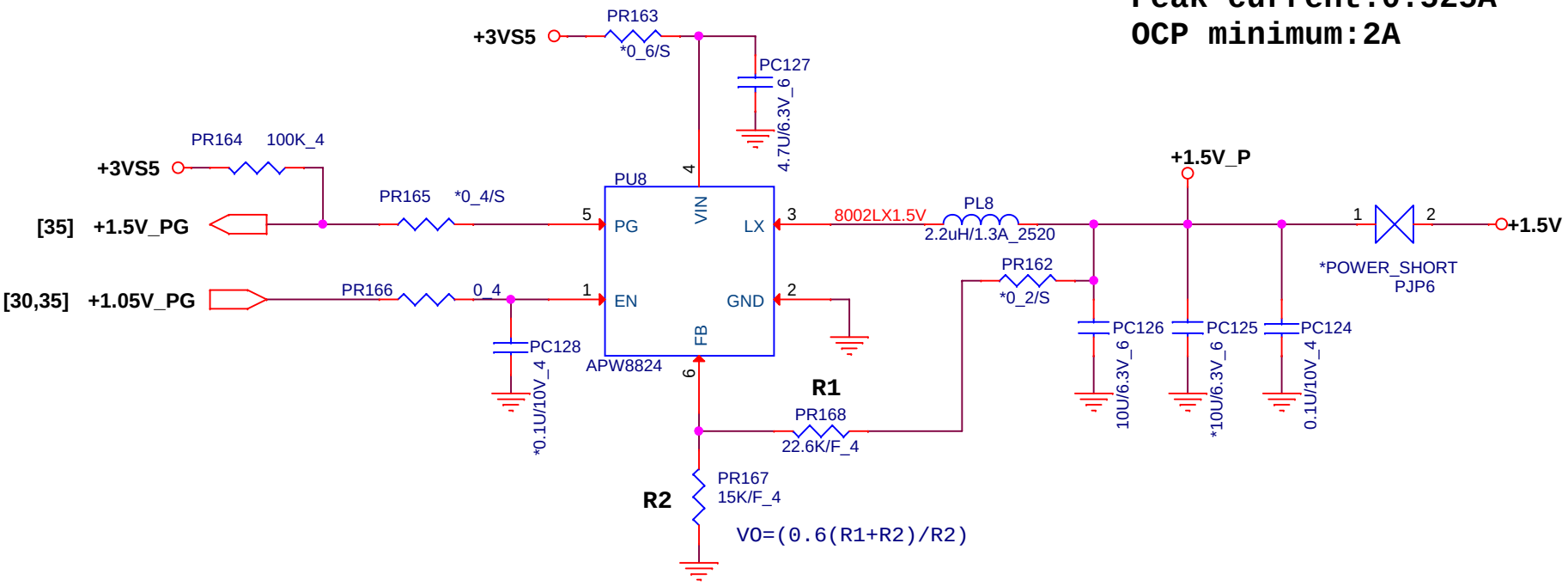
+1.05V Volt +/- 5%
Countinue current:1A
Peak current:1.0A
OCP minimum:2A



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
A	+1.05V (APW8824)	1A
Date: Tuesday, August 20, 2013	Sheet 30 of 39	

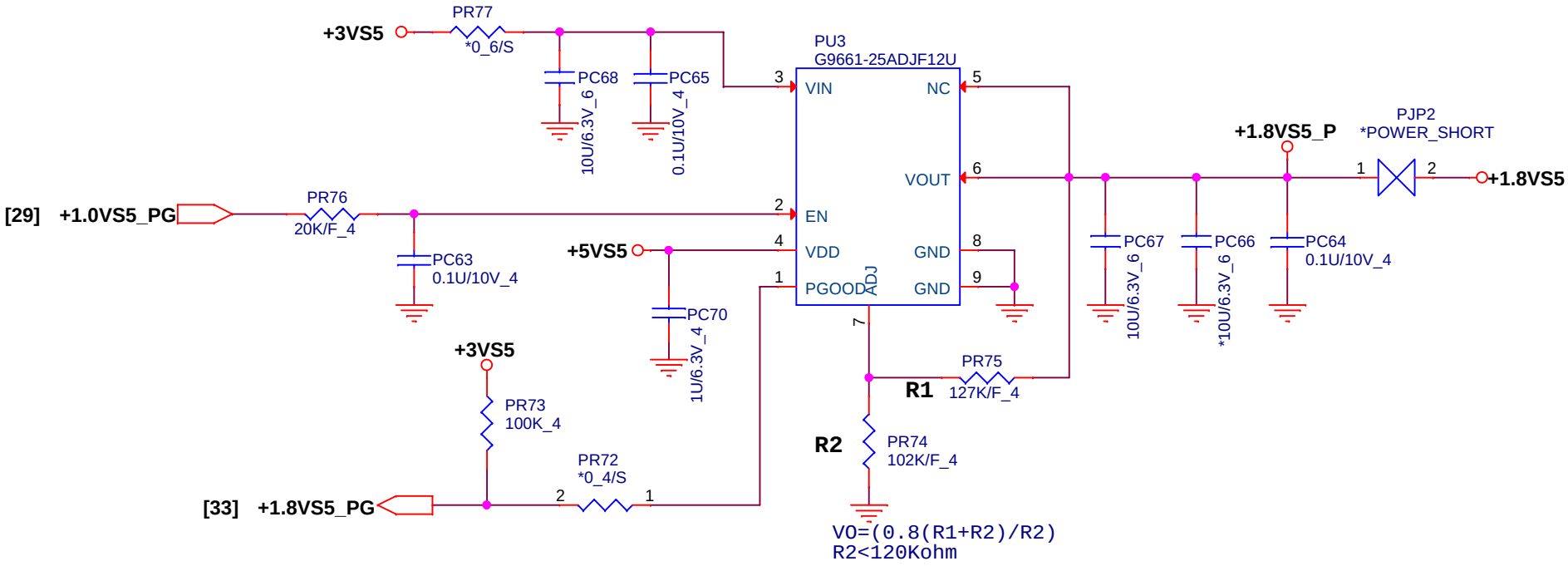
+1.5V +/- 5%
Countinue current:0.45A
Peak current:0.525A
OCP minimum:2A



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
A	+1.5V (APW8824)	1A
Date: Tuesday, August 20, 2013	Sheet 31 of 39	

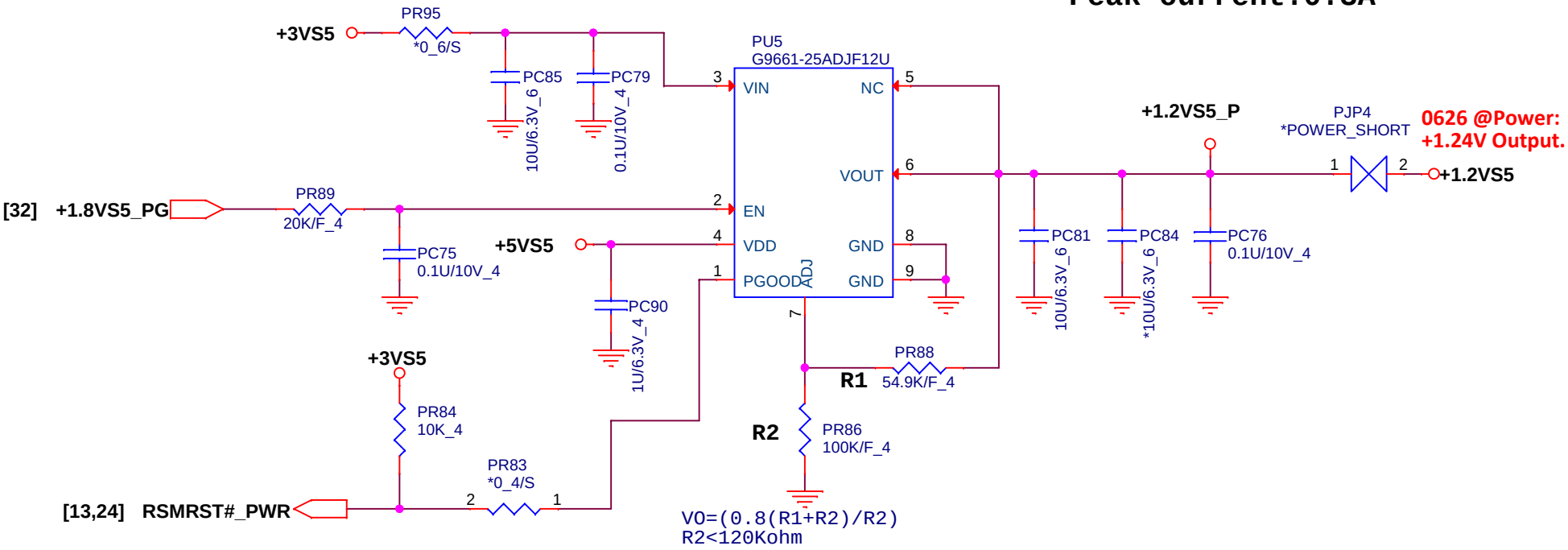
+1.8V Volt +/- 5%
Countinue current:0.105A
Peak current:0.3A



PROJECT :JWM
Quanta Computer Inc.

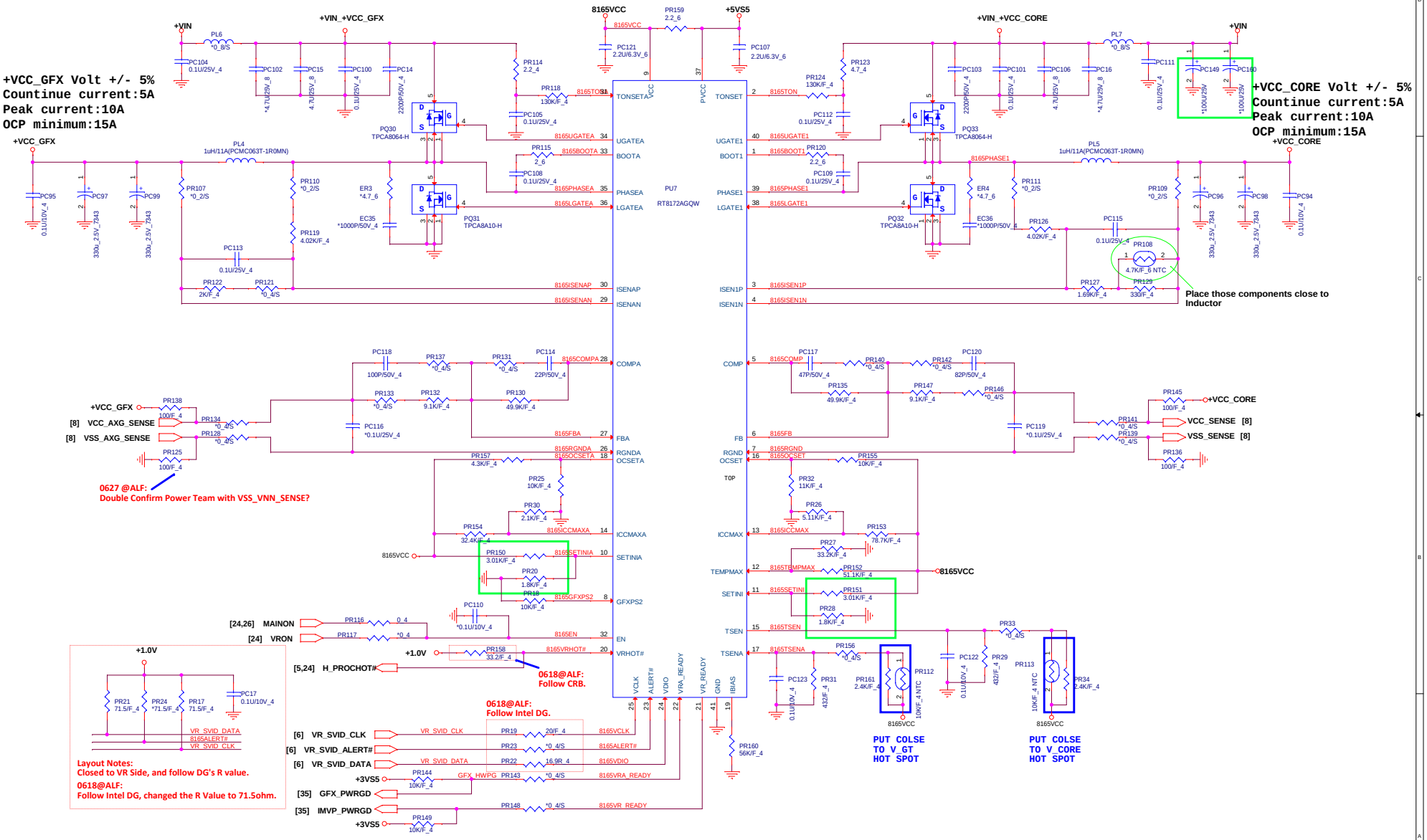
Size	Document Number	Rev
A	+1.8VS5(G9661)	1A
Date:Tuesday, August 20, 2013	Sheet 32 of 39	

+1.2VS5 Volt +/- 5%
Countinue current:35mA
Peak current:0.3A

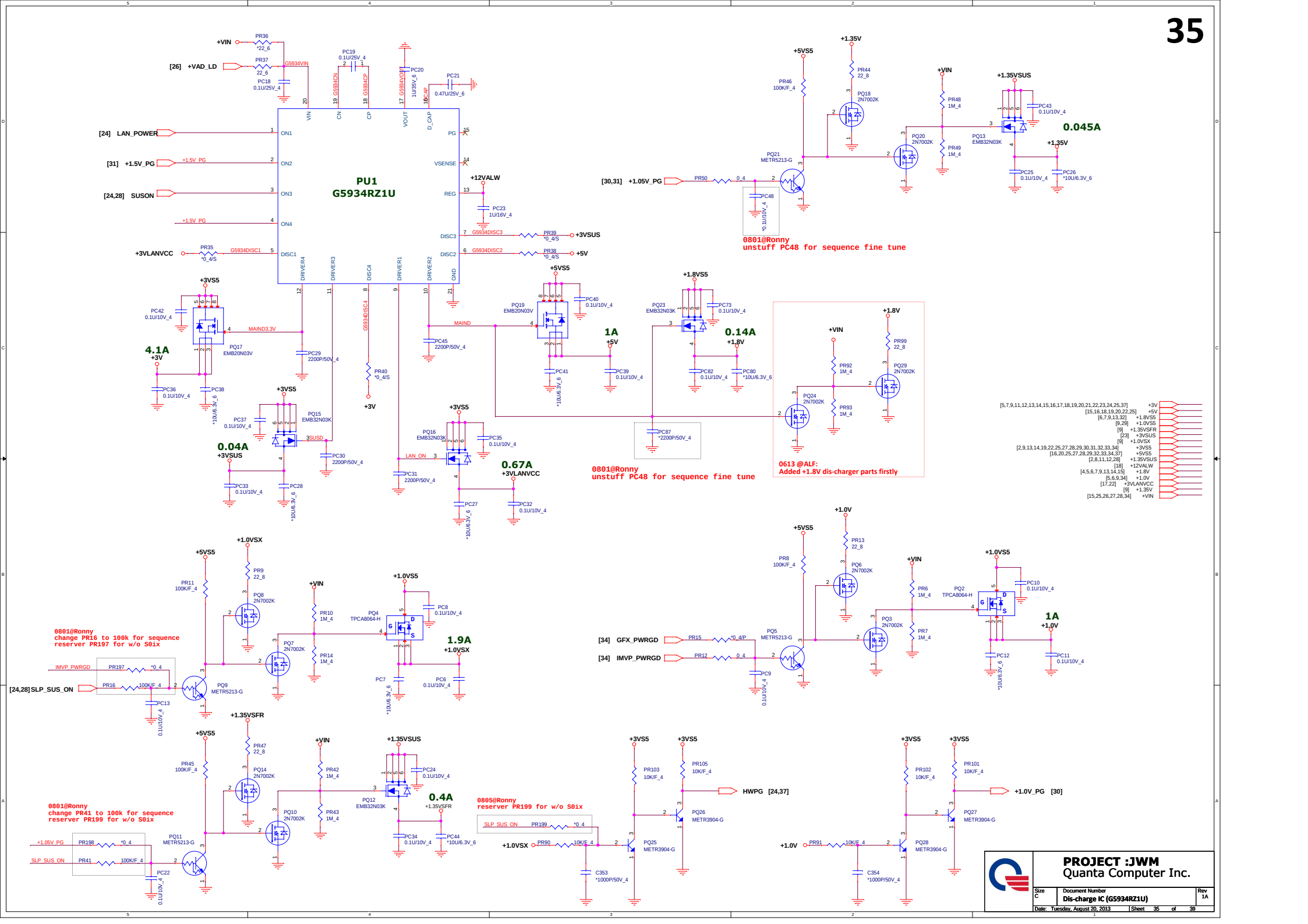


PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
A	+1.2VS5 (G9661)	1A
Date: Tuesday, August 20, 2013	Sheet 33 of 39	

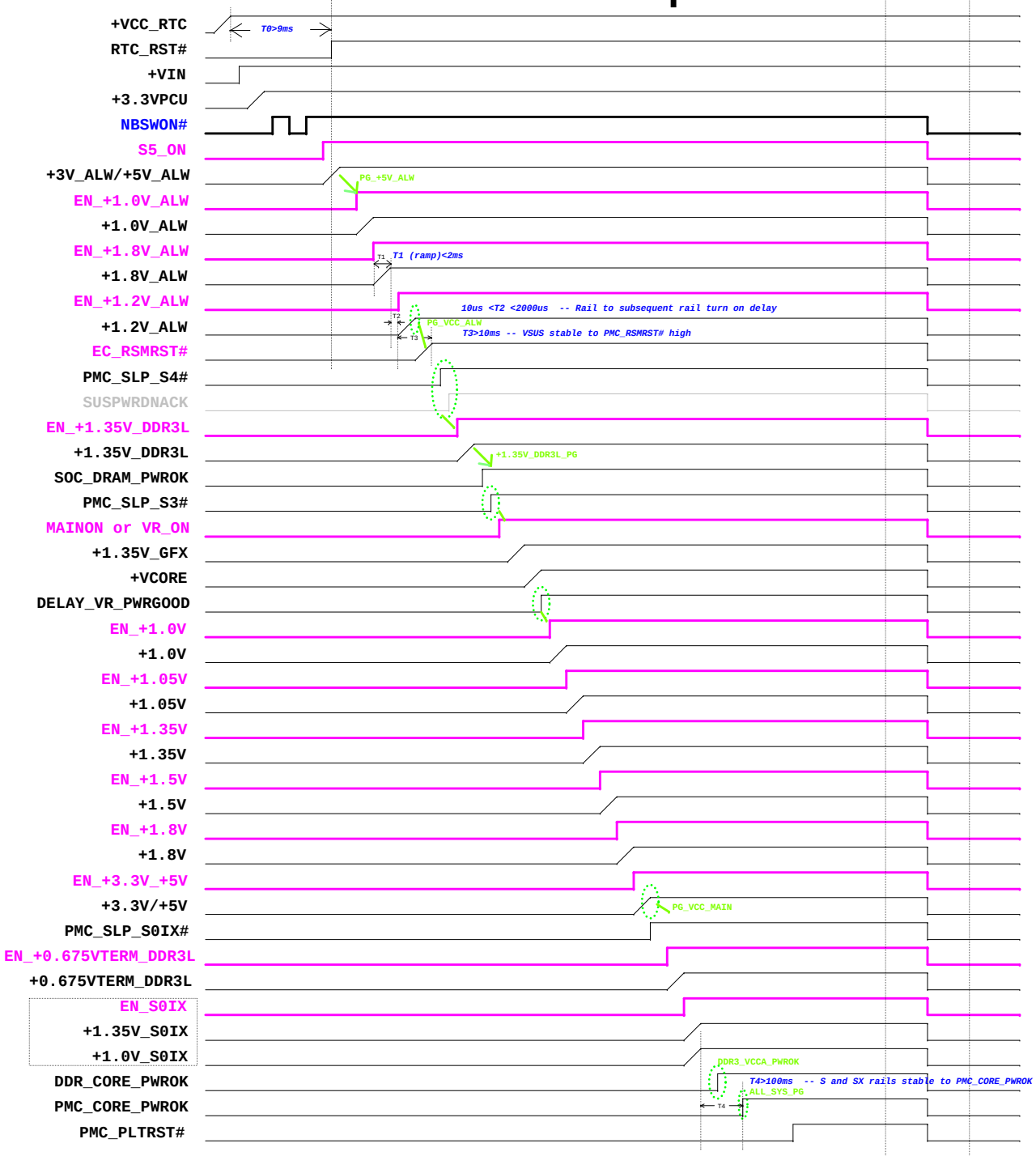


PROJECT :JWM Quanta Computer Inc.			
Size C	Document Number Vcore + Vgfx (TPS559641)		Rev 1A
Date:Tuesday, August 20, 2013	Sheet 34 of 39		



PROJECT :JWM	Quanta Computer Inc.
Size: C	Document Number: Dis-charge IC (G5934RZ1U)
Rev: 1A	
Date: Tuesday, August 20, 2013	Sheet 35 of 39

Power on sequence OFF



T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2 :Rail to subsequent rail turn on delay < 2ms
T3 :+VALWAS stable to EC_RSMRST# high > 10us
T4 :+VS rails stable to PMC_CORE_PWROK > TBD

NOTE:
1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

Green signals (PG) to EC
Blue timing -- Intel
Pink signals from EC

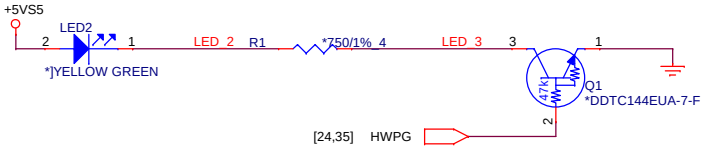
PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
C	POWER SEQUENCE TIMING	1A

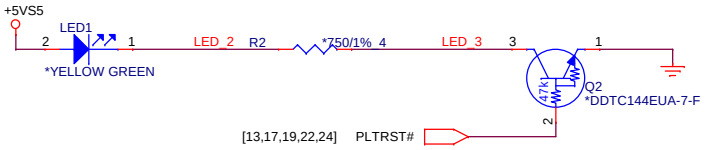
Date: Tuesday, August 20, 2013 Sheet 36 of 39

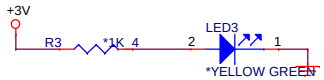
LED For bring-up

EC_ALL_SYS_PG LED



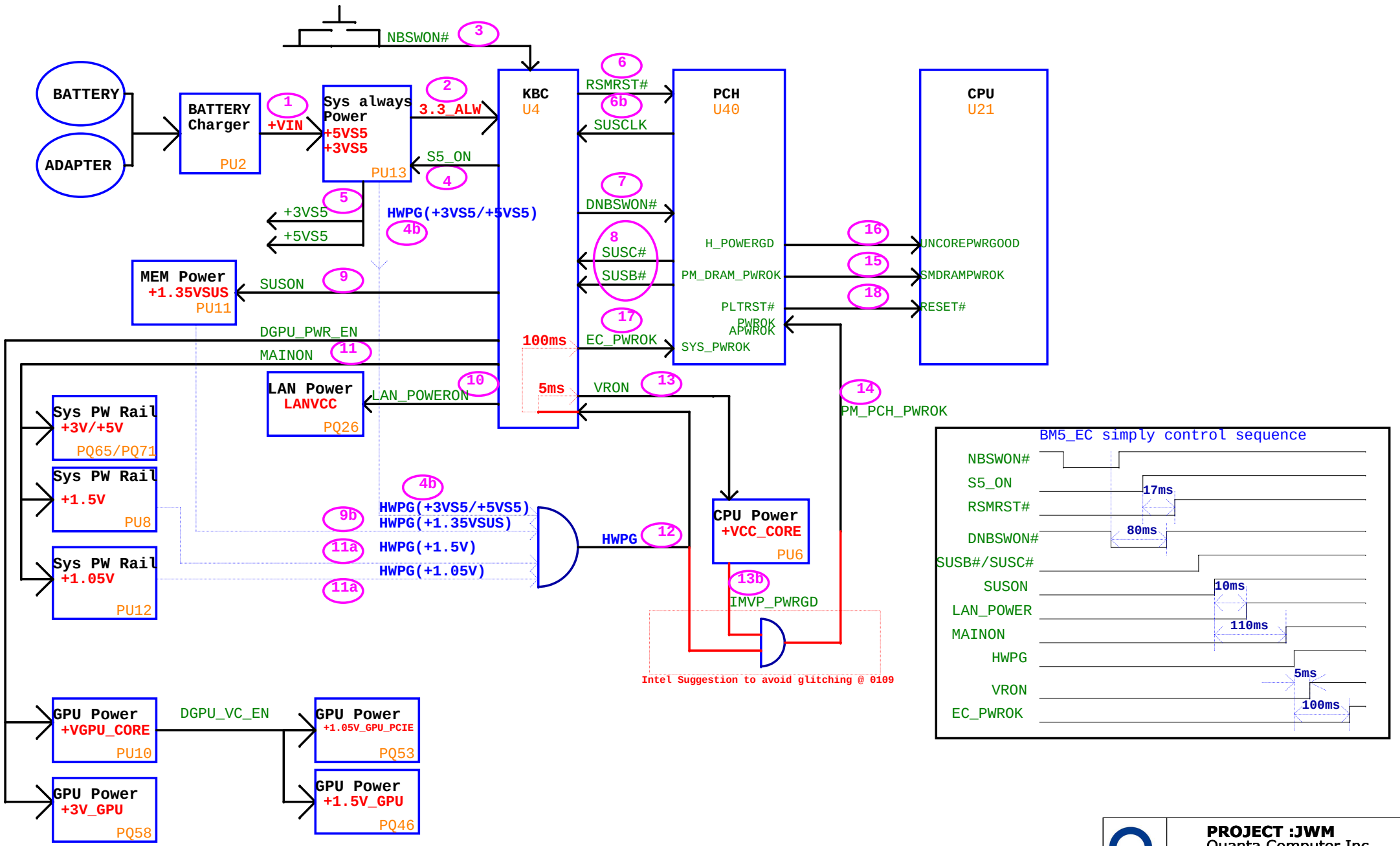
PLTRST# LED





PROJECT :JWM Quanta Computer Inc.		
Size B	Document Number LEDs For bring-up Debug	Rev 1A
Date: Tuesday, August 20, 2013	Sheet 37 of 39	

BM5/6 -- Intel Shark Bay mainly Power On Sequence(G3 to S0)



PROJECT :JWM
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Control Procesure CDP ROF	1A

Date: Tuesday, August 20, 2013 Sheet 38 of 39

JWC Bay Trail-M Schematic EC Tracking Record A-->B June. 03, 2013

EC #	Page	Description	Part Affected
EC-DV-01	10	Change component to "Stuff" to supply the power for VCCASW.	R301
EC-DV-02			
EC-DV-03			
EC-DV-04			
EC-DV-05			
EC-DV-06			
EC-DV-07			
EC-DV-08			
EC-DV-09			
EC-DV-10			
EC-DV-11			
EC-DV-12			