Compal Confidential

Kabylake-U M/B Schematics Document

Intel ULV Processor with DDR4 SODIMMx2

Date : 2016/05/11

Version : 1.0

Project :*Diner_Crepe1.1(15")*
CDL50 : LA-D707P

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				Date: Wednesday, May 11, 2016; Sheet 1 of 60

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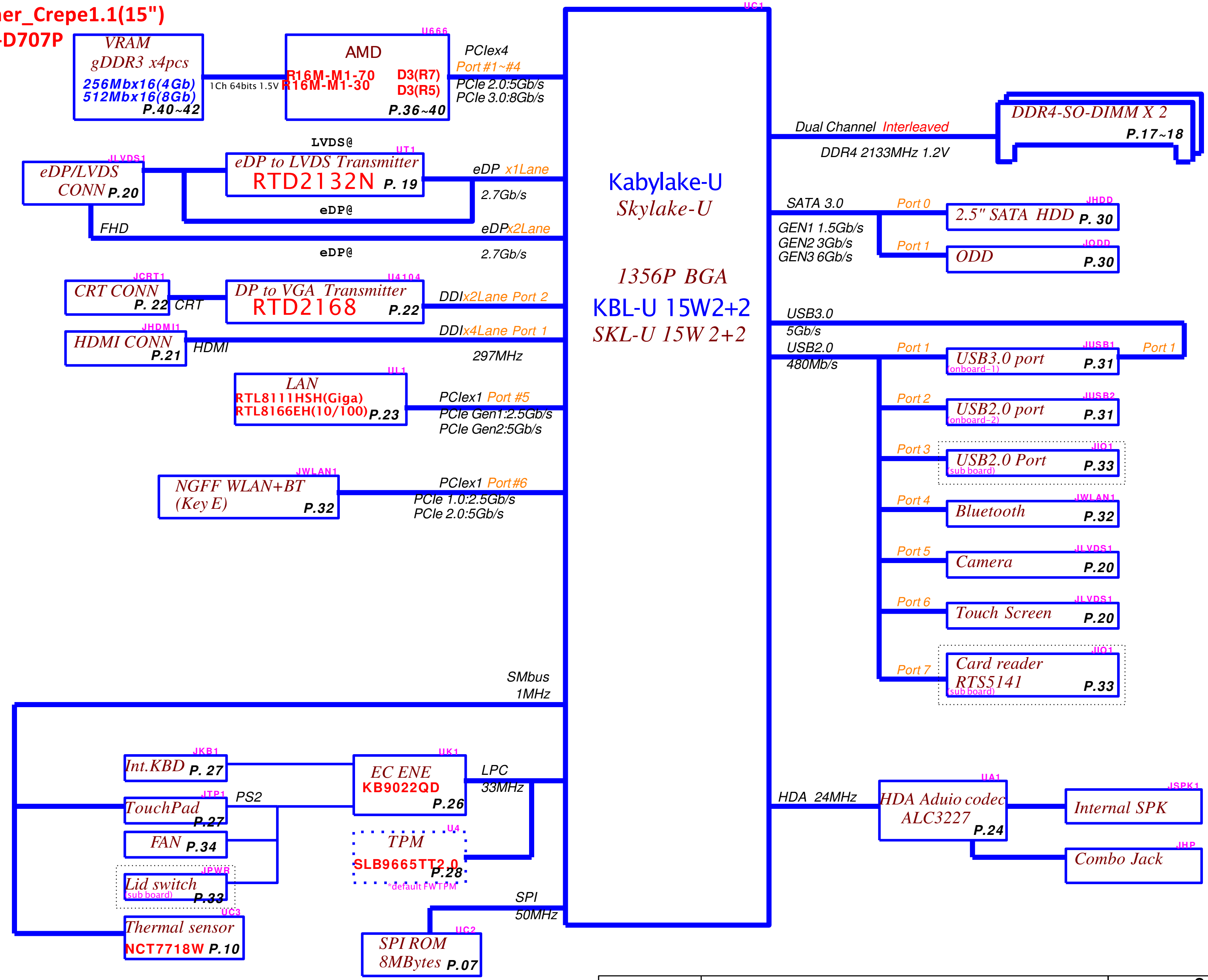
Model Name : Diner_Crepe1.1(15")

File Name : LA-D707P



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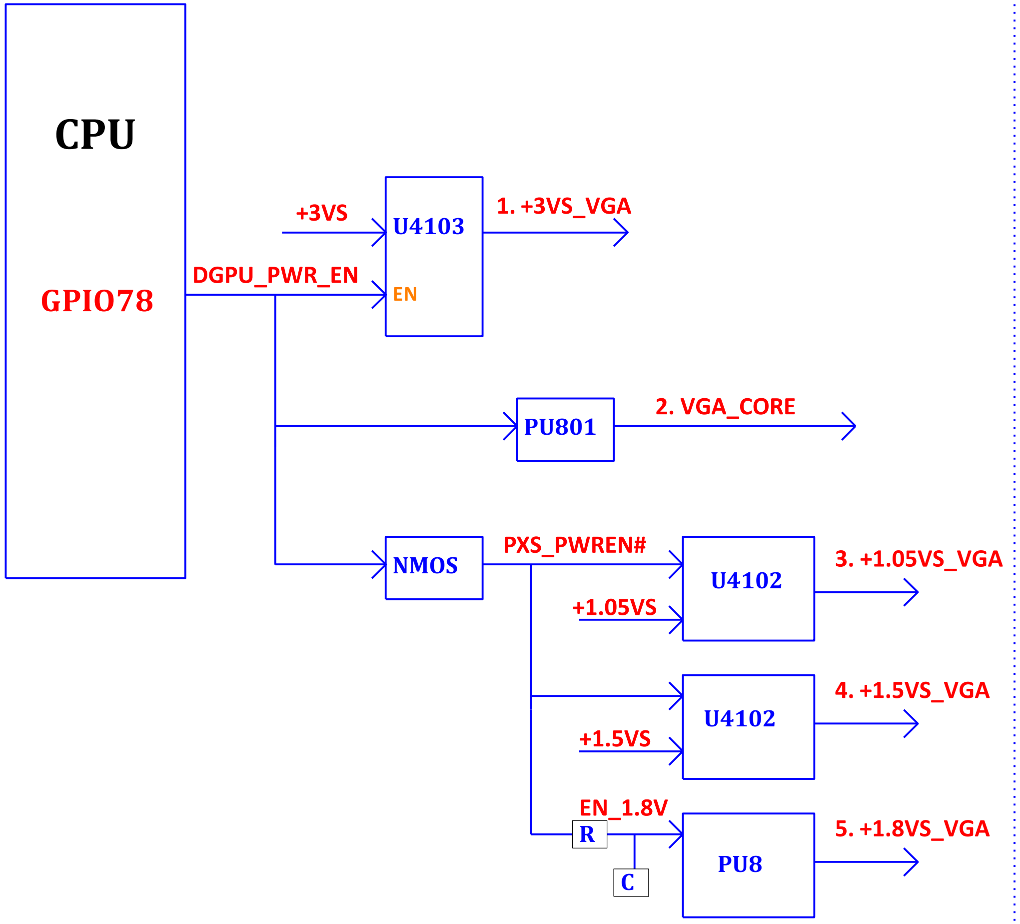

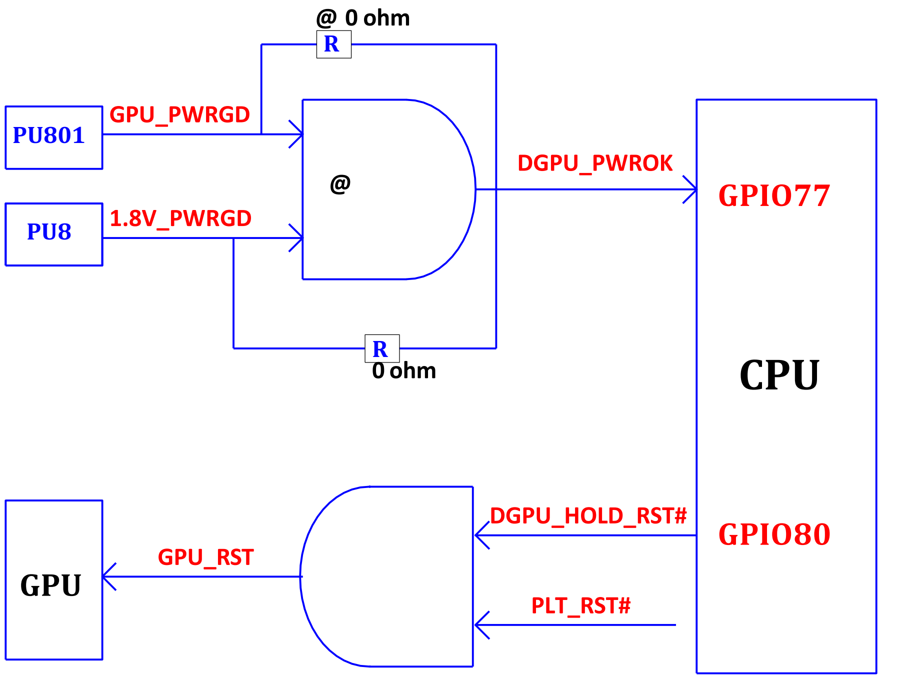

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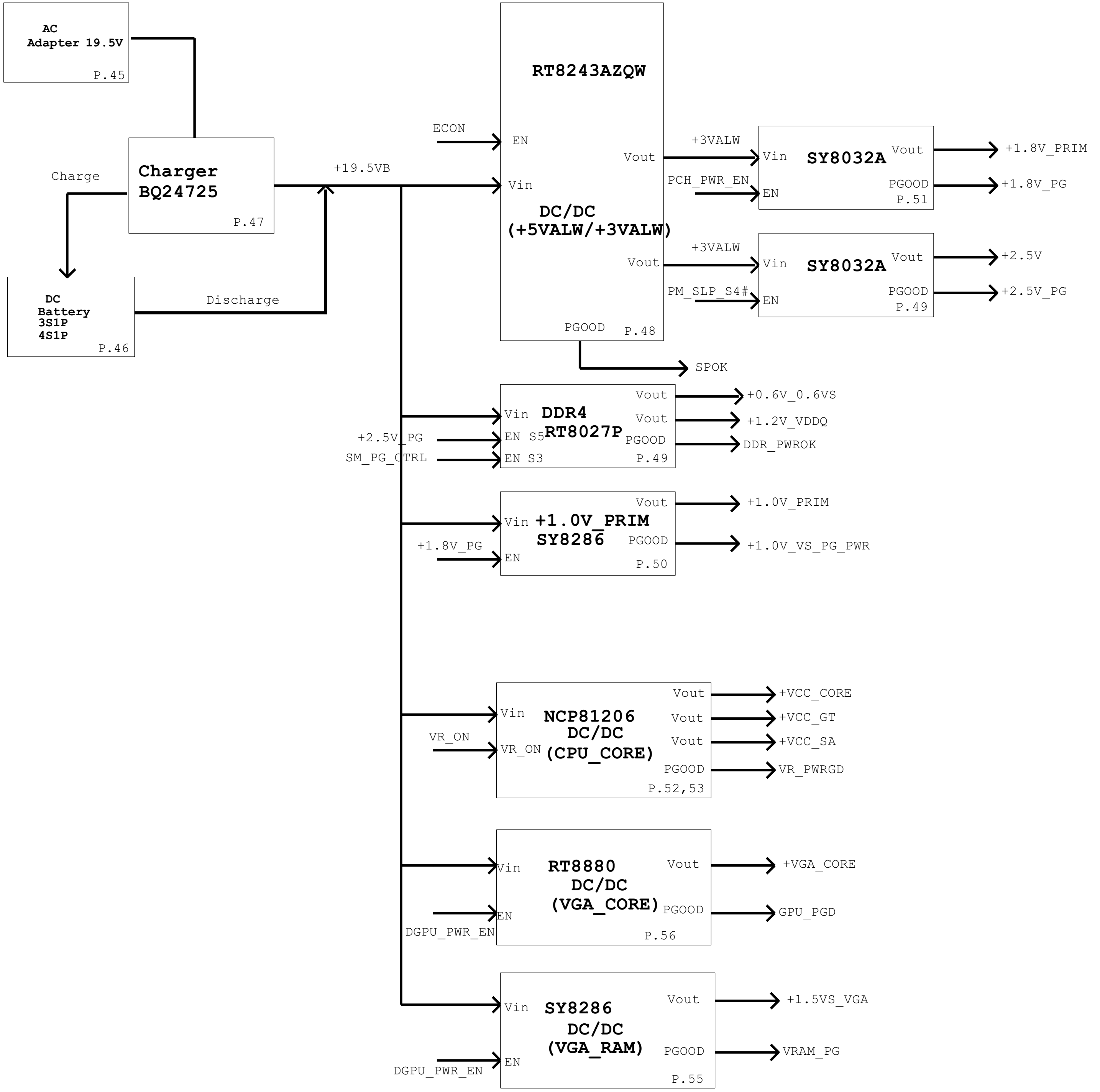


CPU DC/DC NCP81206	52~54
INPUTS	**OUTPUTS**
B+	VCC_SA VCC_GT VCC_VORE
SYSTEM DC/DC RT8243AZQW	48
INPUTS	**OUTPUTS**
B+	+5VALW/+3VALW
SYSTEM DC/DC RT8207P / 8032	49
INPUTS	**OUTPUTS**
B+	+1.2V_VDDQ +0.6V_0.6VS +2.5V
SYSTEM DC/DC SY8286	50
INPUTS	**OUTPUTS**
B+	+1.0V_PRIM
SYSTEM DC/DC SY8032A	51
INPUTS	**OUTPUTS**
+3VALW	+1.8V_PRIM
SYSTEM DC/DC RT8880	56~57
INPUTS	**OUTPUTS**
B+	+VGA_CORE
SYSTEM DC/DC SY8286	55
INPUTS	**OUTPUTS**
B+	+1.5VS_VGA

Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.2V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.6VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Read
SMBCLK SMBDATA	+3VS	DIMM1	TBC	TBC	0xA2
		Touch PAD	TBC	TBC	TBC
SML0CLK SML0DATA	+3VS	ME FW	0x48/0x49	TBC	0x90/0x92
SML1CLK SML1DATA	+3VS	EC	TBC	TBC	TBC
		DGPU	TBC	TBC	TBC
		PCH	TBC	TBC	TBC

EC SMBUS Address Table (TBC)

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VL_EC	BAT	0x16
		CHGR	0x12
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C
		PCH	TBC

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
DGPU SKU	PX@	
UMA SKU	UMA@	
SPI_IO3(MOW36)	ES@	
Crystal (DIS)	XTALPX@	
Crystal	XTAL@	
Green CLK(UMA)	GCLK@	
Green CLK(DIS)	GCLKPX@	
TPM	TPM@	

DAX
KBL
Part Number = DA6001LS000
PCB 1RU LA-D707P REV0 M/B 6

DAX
SKL
Part Number = DAZ1O200301
PCB BDL50 LA-D704P LS-C701P/C703P62
SKL@

45@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM

RO0000003HM

QKKS@ UC1 ES_QKKS SA00009PJ10 S IC A32 FJ8067702739720 QKKS G0 2.4G
QKJW@ UC1 ES_QKJW SA00009UR00 S IC A32 FJ8067702739718 QKJW G0 2.6G
SKLPV2@ UC1 SKY_i7_6500U_SR2EZ SA000092P60 S IC FJ8066201930408 SR2EZ D1 2.5G BGA

QS_i3@ UC1 i3_7100U_QS_QLDP SA0000A3810 S IC A32 FJ8067702739738 QLDP H0 2.4G
QS_i5@ UC1 i5_7200U_QLDM SA0000A3710 S IC A32 FJ8067702739739 QLDM H0 2.5G
QS_i7@ UC1 i7_7500U_QLDN SA0000A3420 S IC A32 FJ8067702739740 QLDN H0 2.7G

R30@ U666 R16M-M1-30 FCBGA SA000087T90 S IC A32 216-0867-071 R16M-M1-30 FCBGA
R70@ U666 R16M-M1-70 FCBGA SA000098V10 S IC A32 216-0864-032 R16M-M1-70FCBGA

R30R1@ U666 R16M-M1-30 FCBGA SA000087TC0 S IC A32 216-0867-071 R16M-M1-30 FCBGA
R70R1@ U666 R16M-M1-70 FCBGA SA000098V30 S IC A32 216-0864-032 R16M-M1-70FCBGA

R30R3@ U666 R16M-M1-30 FCBGA SA000087TB0 S IC A32 216-0867-071 R16M-M1-30 FCBGA
R70R3@ U666 R16M-M1-70 FCBGA SA000098V40 S IC A32 216-0864-032 R16M-M1-70FCBGA

i3R1@ UC1 ES_QKKS SA000092N70 S IC A32 FJ8067702739720 QKKS G0 2.4G
i5R1@ UC1 ES_QKKS SA000092O70 S IC A32 FJ8067702739720 QKKS G0 2.4G
i7R1@ UC1 ES_QKKS SA000092P60 S IC A32 FJ8067702739720 QKKS G0 2.4G

i3R3@ UC1 ES_QKKS SA000092N80 S IC A32 FJ8067702739720 QKKS G0 2.4G
i5R3@ UC1 ES_QKKS SA000092O80 S IC A32 FJ8067702739720 QKKS G0 2.4G
i7R3@ UC1 ES_QKKS SA000092P70 S IC A32 FJ8067702739720 QKKS G0 2.4G

ZZZ HY2@ 2G HYNIX X7667032L01
ZZZ MIC2@ 2G MICRON X7667032L02
ZZZ SAM2@ 2G SAMSUNG X7667032L05
ZZZ HY4@ 4G Hynix X7667032L03
ZZZ MIC4@ 4G Micron X7667032L04

ZZZ R3HY2@ 2G HYNIX X7667032L23
ZZZ R3MIC2@ 2G MICRON X7667032L24
ZZZ R3SAM2@ 2G SAMSUNG X7667032L25
ZZZ R3HY4@ 4G Hynix X7667032L21
ZZZ R3MIC4@ 4G Micron X7667032L22

Power State

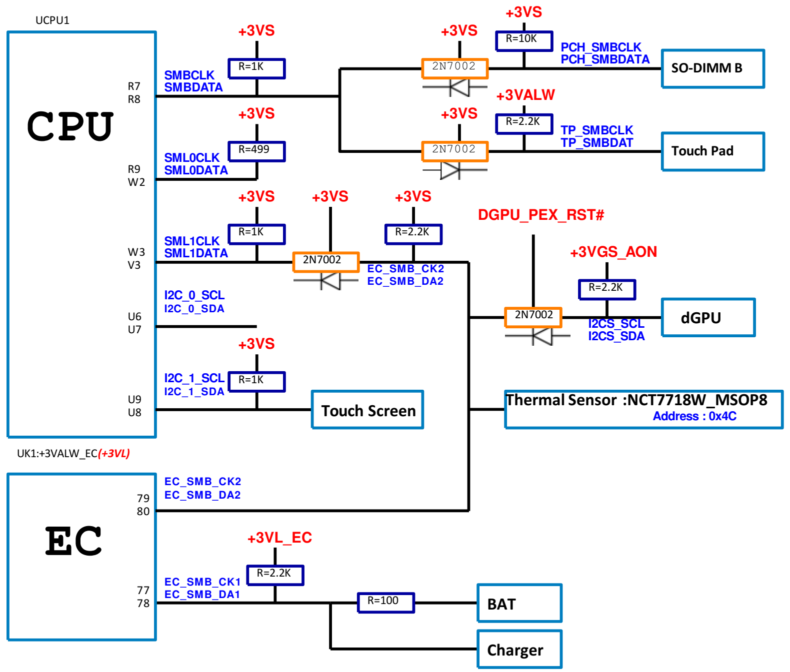
STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

<USB2.0 port>

USB2.0 port	DESTINATION UMA	Dis
1	USB 2.0/3.0	USB 2.0/3.0
2	USB 2.0/3.0	USB 2.0/3.0
3	USB 2.0 OFF BOARD	USB 2.0 OFF BOARD
4	WLAN	WLAN
5	Camera	Camera
6	TOUCH SCREEN	TOUCH SCREEN
7	CR	CR
8		
9		
10		

<PCI-E,SATA,USB3.0/CLK>

Lane#	PCI-E	SATA	USB3.0	DESTINATION UMA	Dis	CLK
1			1	USB3.0	USB3.0	X
2			2	USB3.0	USB3.0	X
3			3	USB3.0(Charger)	USB3.0(Charger)	X
4			4	USB3.0(IO Board)	USB3.0(IO Board)	X
5	1		5	X	GPU(DIS only)	CLK0
6	2		6	X	GPU(DIS only)	
7	3			X	GPU(DIS only)	
8	4			X	GPU(DIS only)	
9	5			LAN	LAN	CLK1
10	6			WLAN	WLAN	CLK2
11	7	0		2.5"HDD	2.5"HDD	X
12	8	1		ODD	ODD	X
13	9			Card reader(PCI-E)	Card reader(PCI-E)	CLK3
14	10			X	X	X
15	11	1*		X	X	X
16	12	2				X



Load BOM Option Table

BOM Number	Load BOM Option
4519YN32L01(UMA)	
4519YN32L02(DIS)	

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[Diner-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]

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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

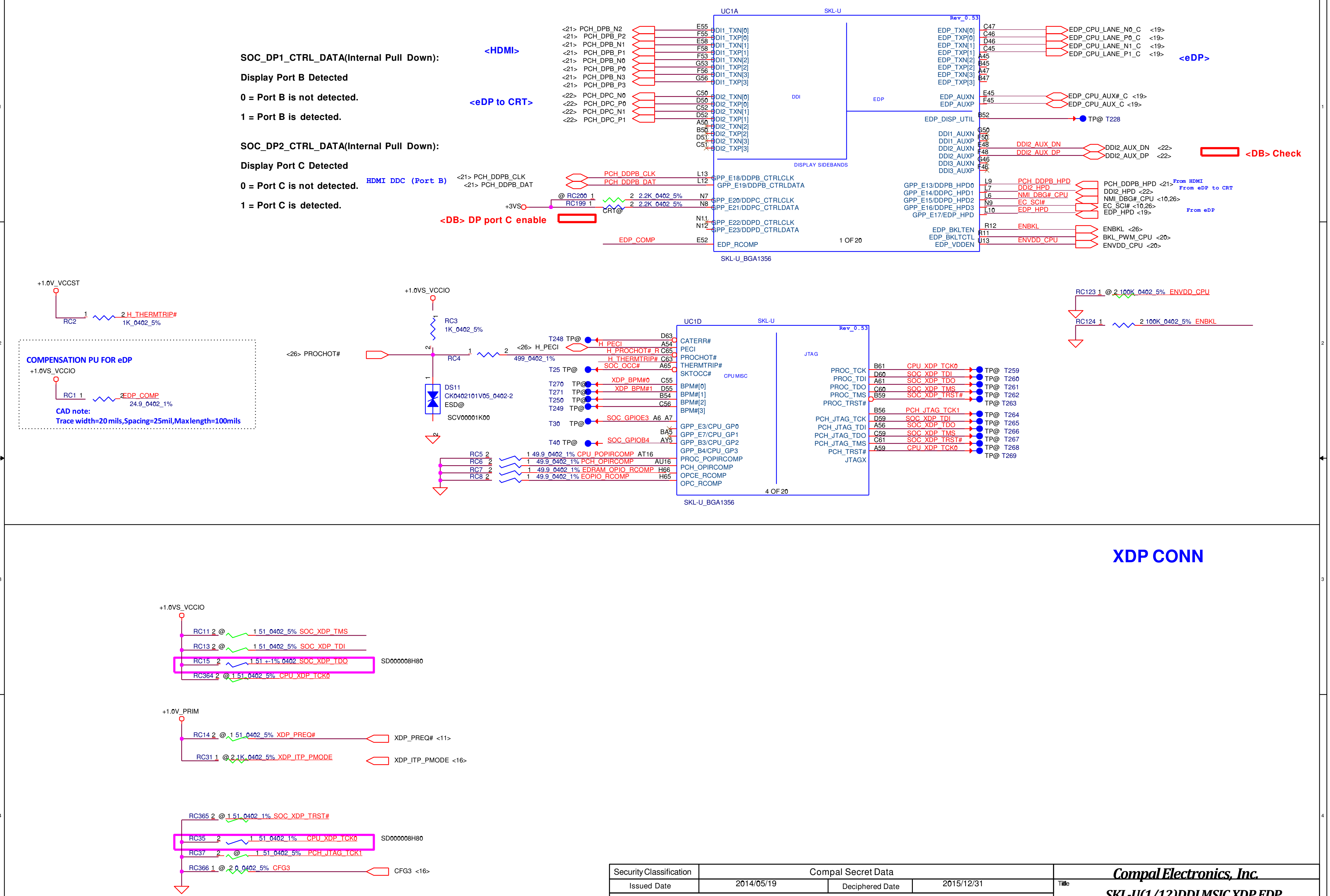
1 = Port B is detected.

SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.



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Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

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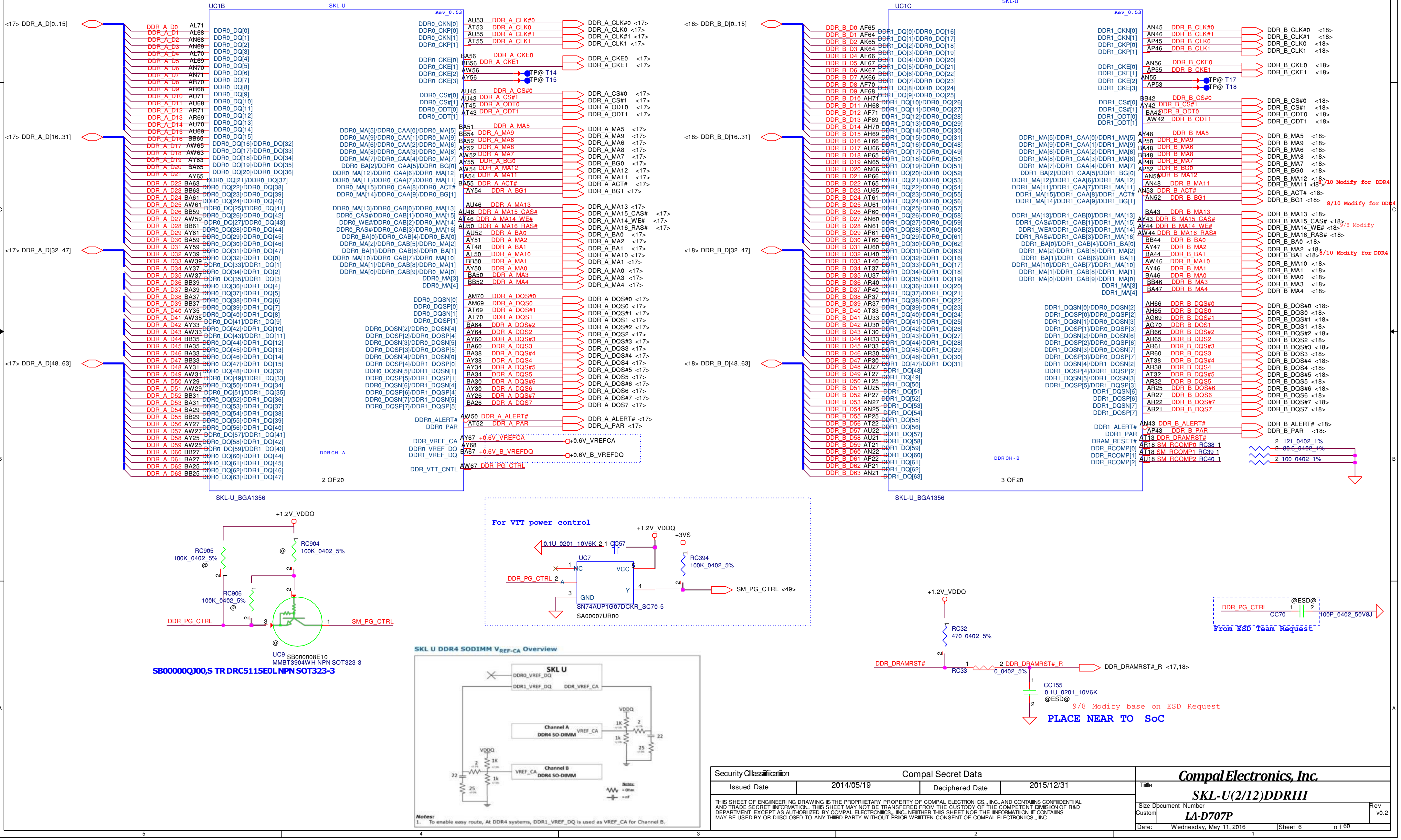
Interleaved Memory

Interleaved Memory

<Cocoa_1020>
PDG#543016, ODT: CPU side no connect, DRAM side connect to VDDQ(Memory down); FET+R(SO-DIMM)



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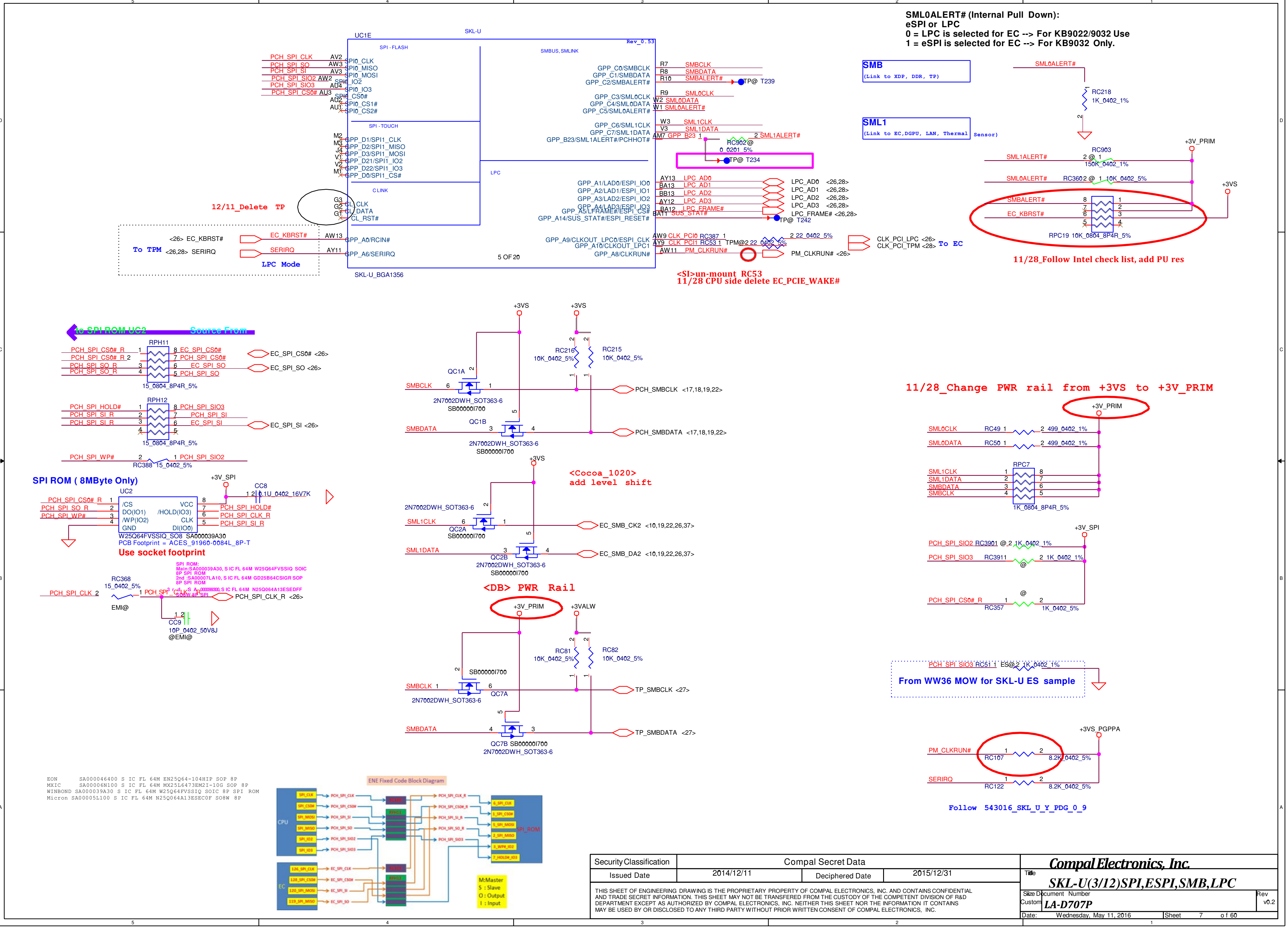
				Date: Wednesday, May 11, 2016; Sheet 6 of 60



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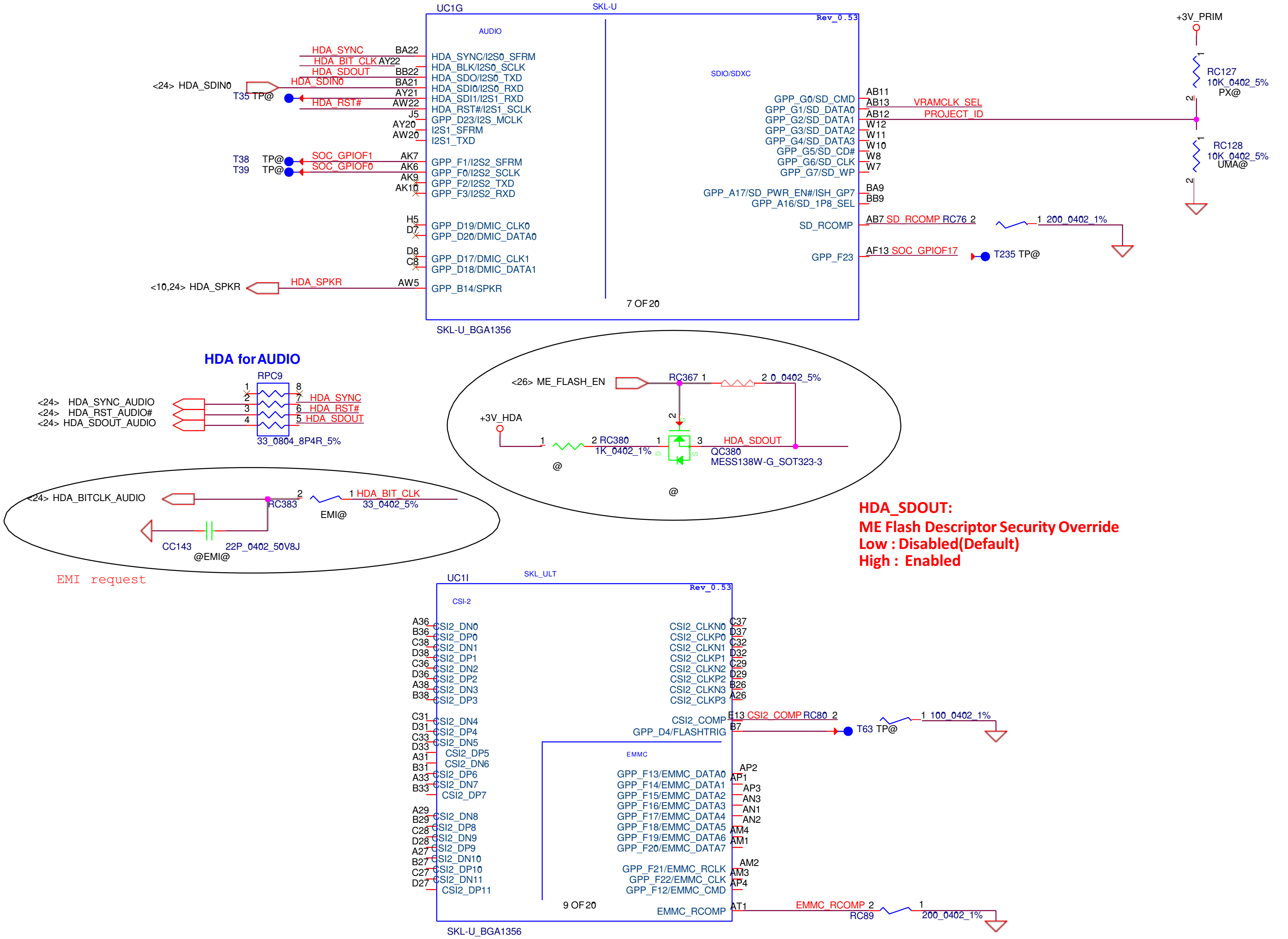
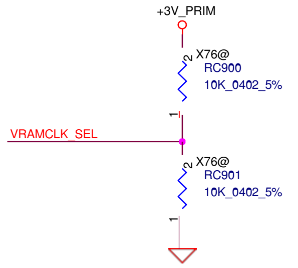
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: LA-D707P | Rev: v0.2





	UMA	DIS
PROJECT_ID	0	1

	900MHz	1000MHz
VRAM Clock	0	1

HDA_SDOUT:
ME Flash Descriptor Security Override
Low : Disabled(Default)
High : Enabled

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Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

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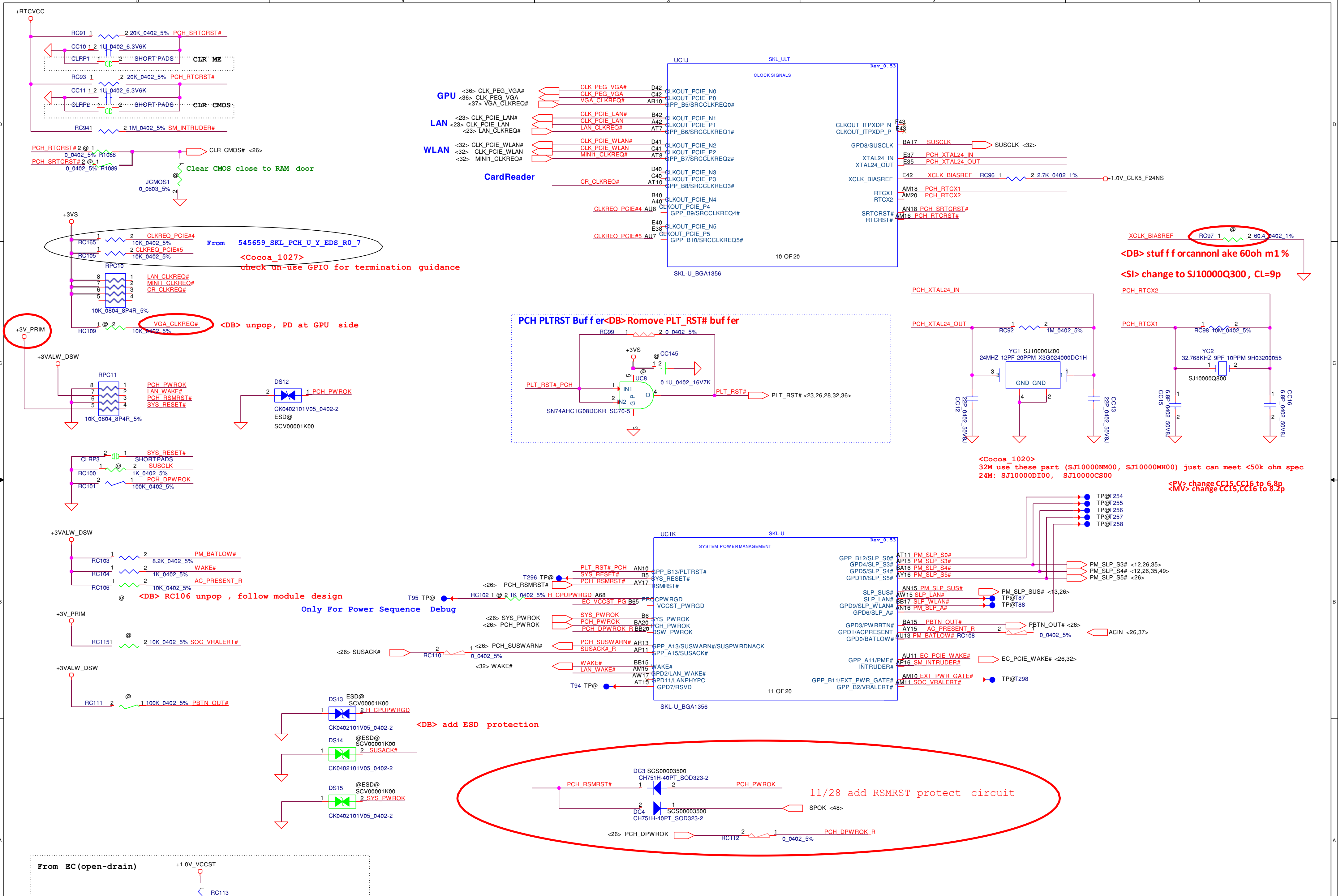

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Title: SKL-U(5/12)CLK,GPIO

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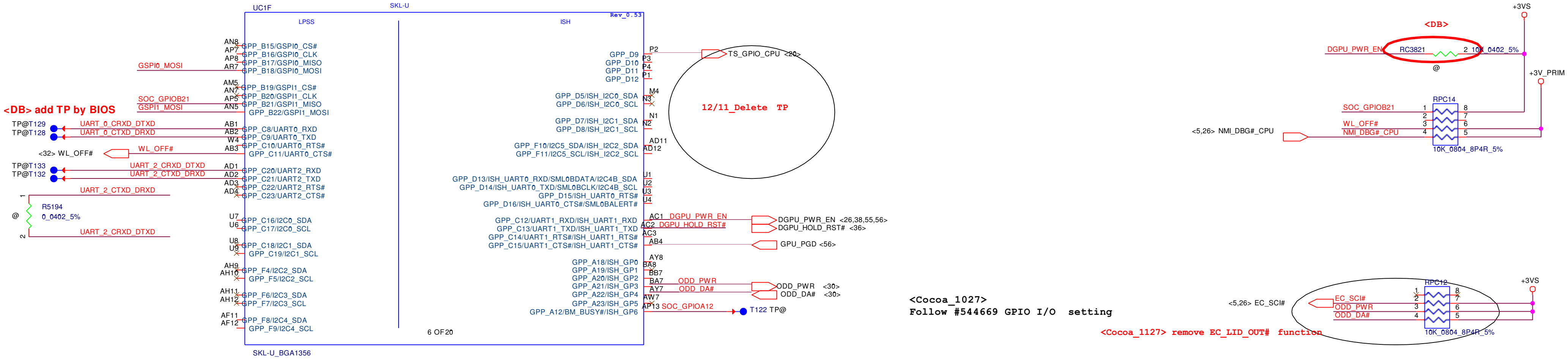
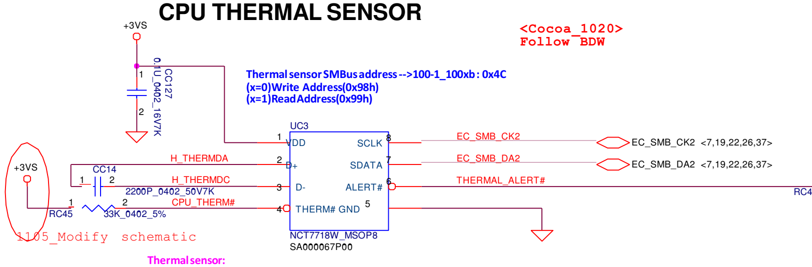


CPU THERMAL SENSOR



Thermal sensor:
Main:SA000067P00, S IC NCT7718W MSOP 8P THEMAL SENSOR(Nuvoton)
2nd : SA00007WP00, S IC F75397M MSOP 8P THEMAL SENSOR(Fintek)
3rd : SA007810140, S IC G781P8F MSOP 8P TEMP. SENSOR(GMT)

Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

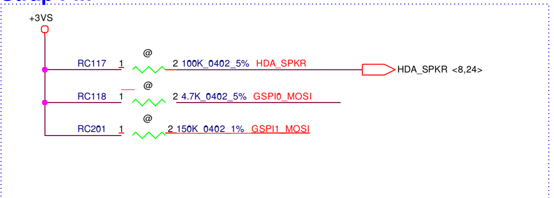
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode --> AAX05 Use

1 = LPC Mode

Strap Pin



<Cocoa_1020>
1K ohm for 400kHz speed/ 0.5k ohm for 1MHz speed

<DB>
Delete Win7 debug port

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Title: SKL-U(6/12)GPIO

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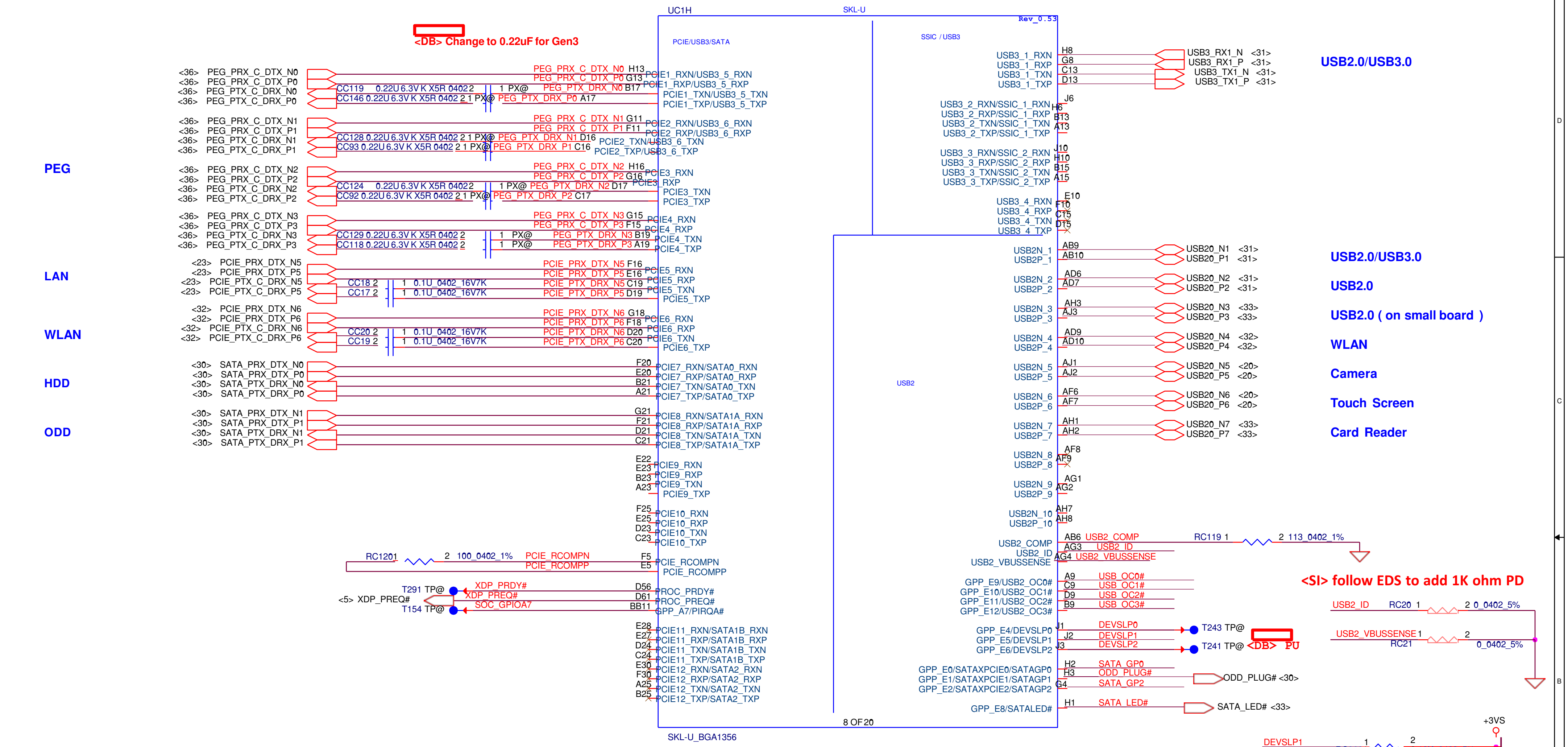
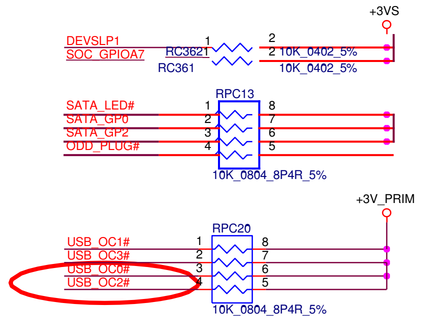
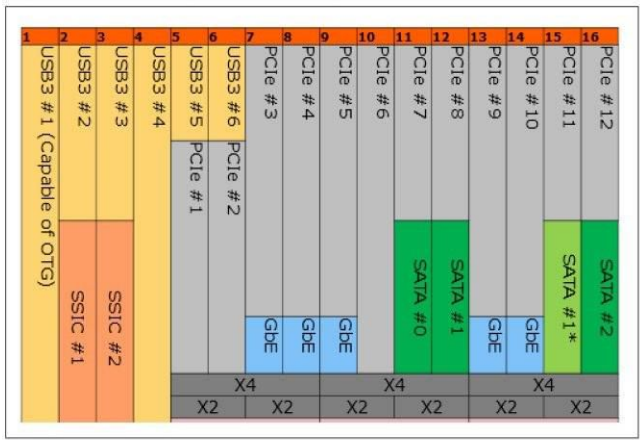




1128_Add pull high resistor

High Speed I/O (HSIO) Lane Multiplexing in SKL U



When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1 and Port 2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NGFF SSD KEY B
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	ODD_PLUG#

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Title: SKL-U(7/12)PCIE,USB,SATA

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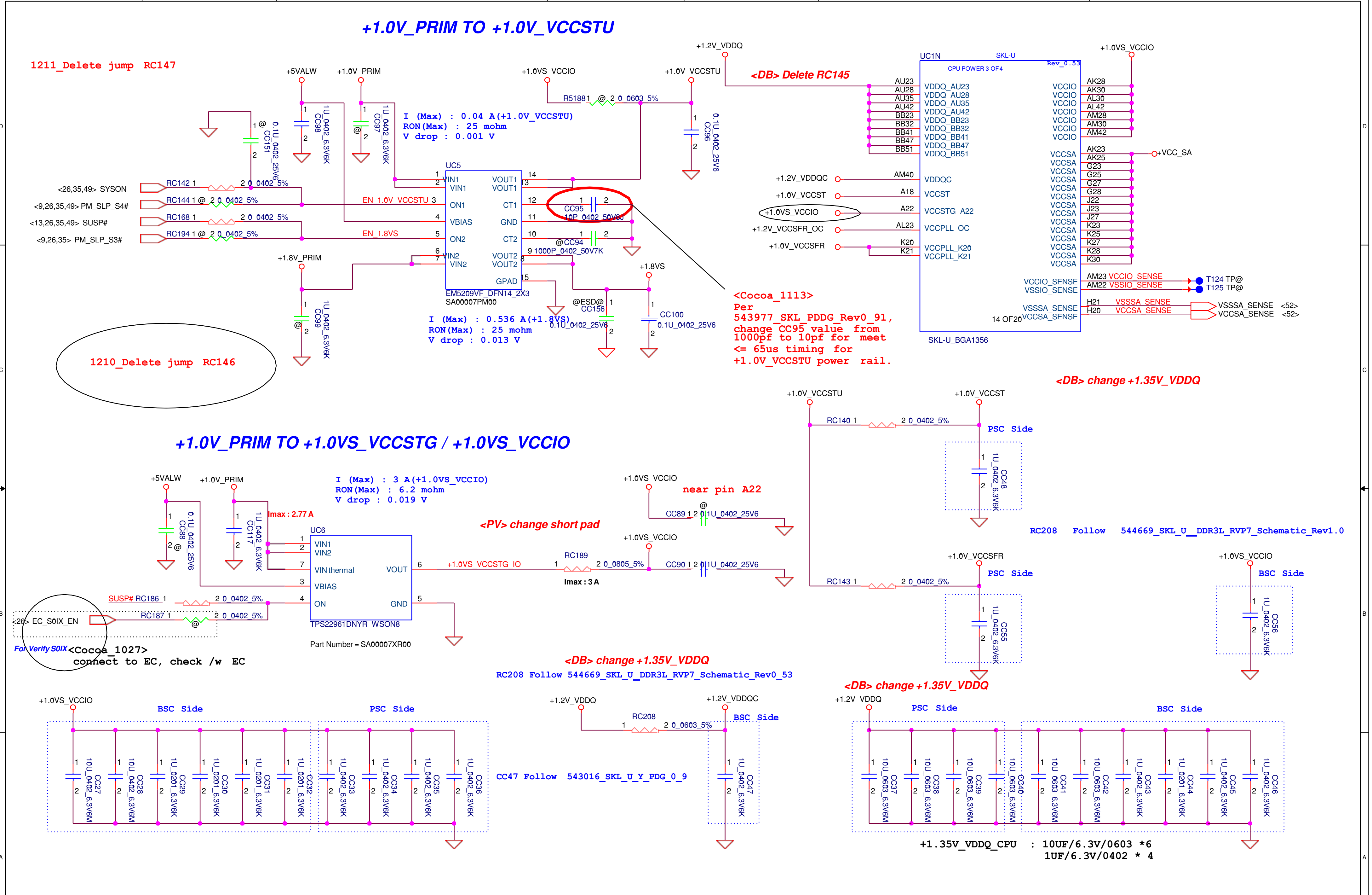

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Title: SKL-U(8/12)Power

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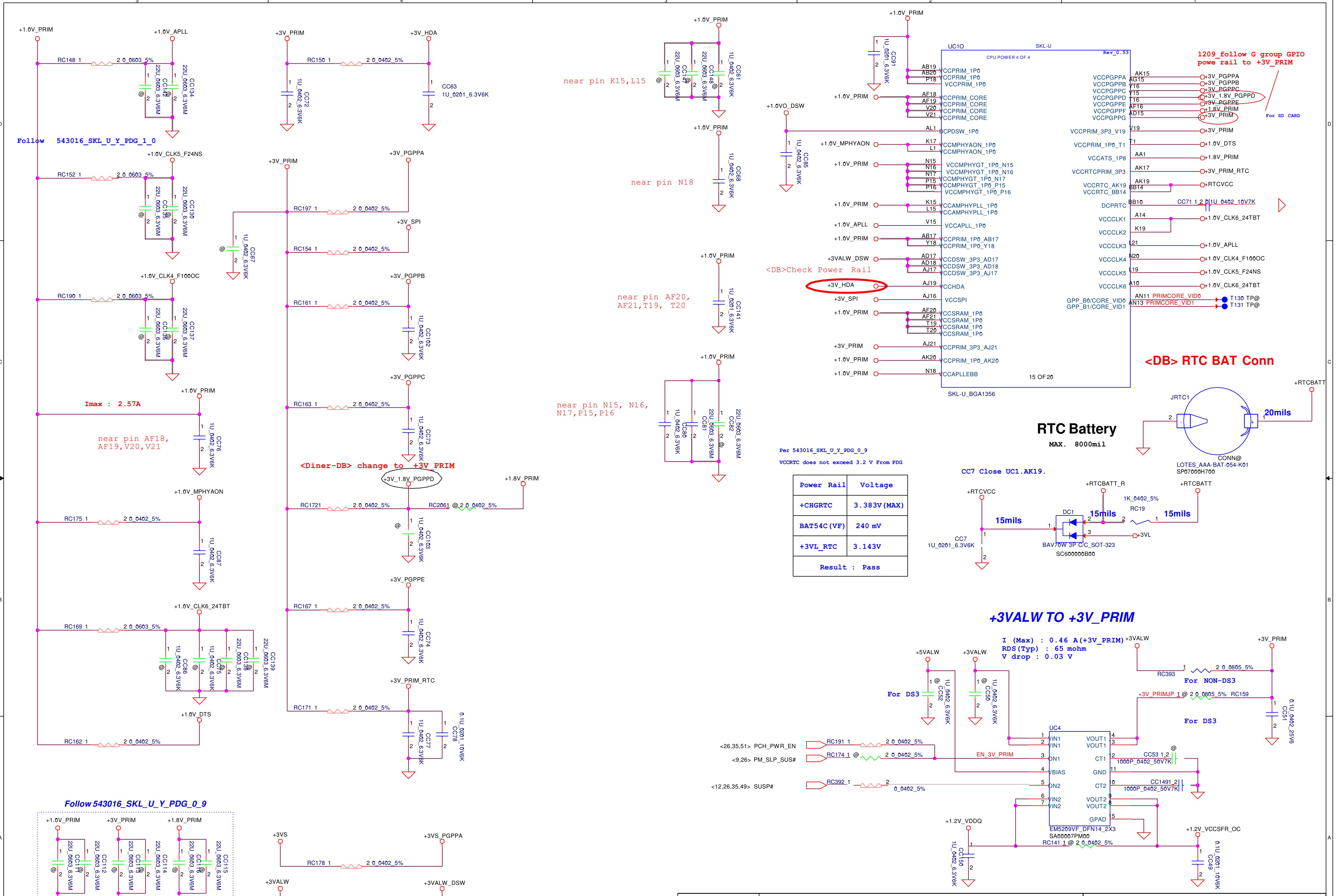

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	

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Title: SKL-U(9/12)Power

Size: Custom Document Number: LA-D707P Rev: v0.2

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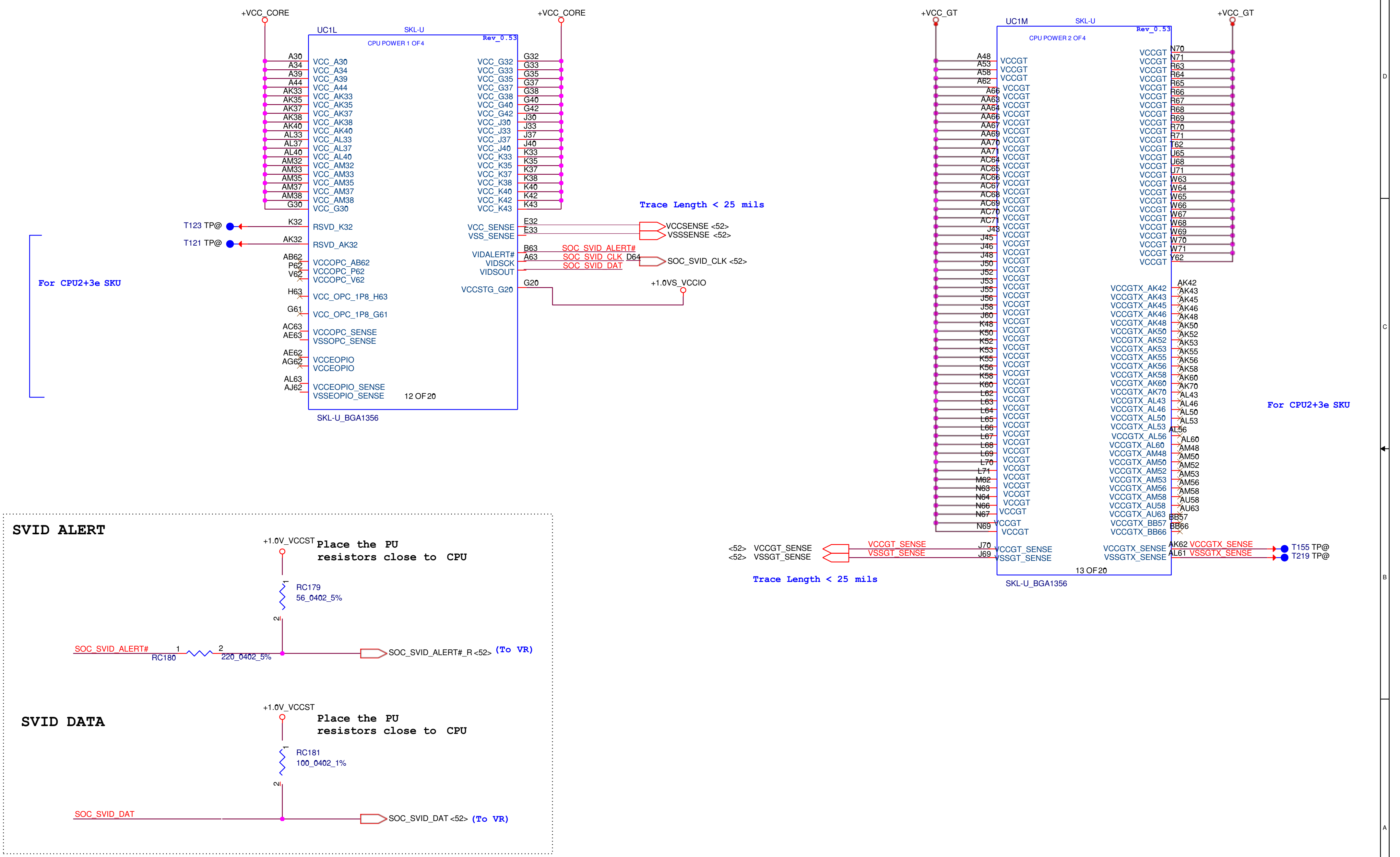

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Title: **SKL-U(10/12)Power,SVID**

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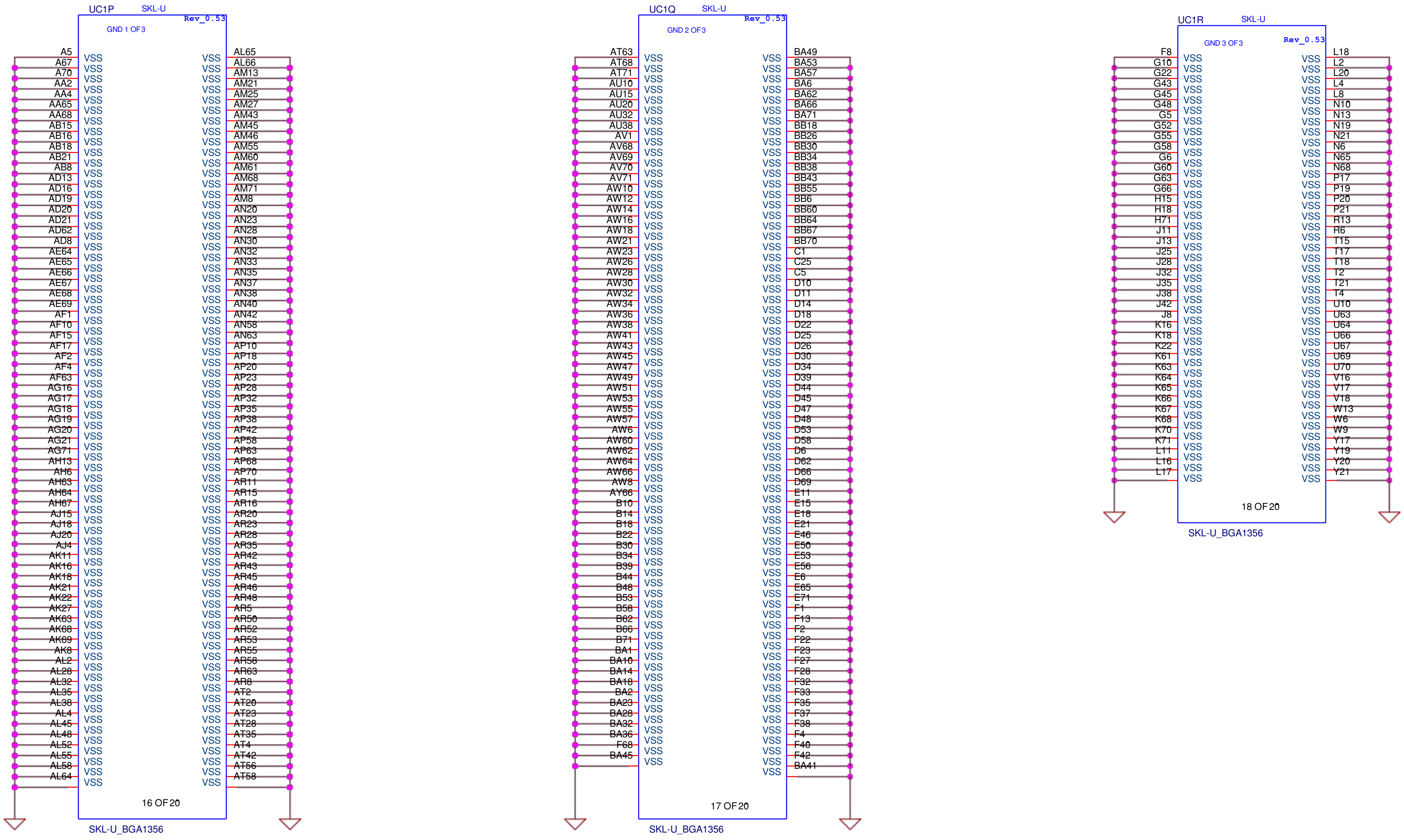

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Title: SKL-U(11/12)GND

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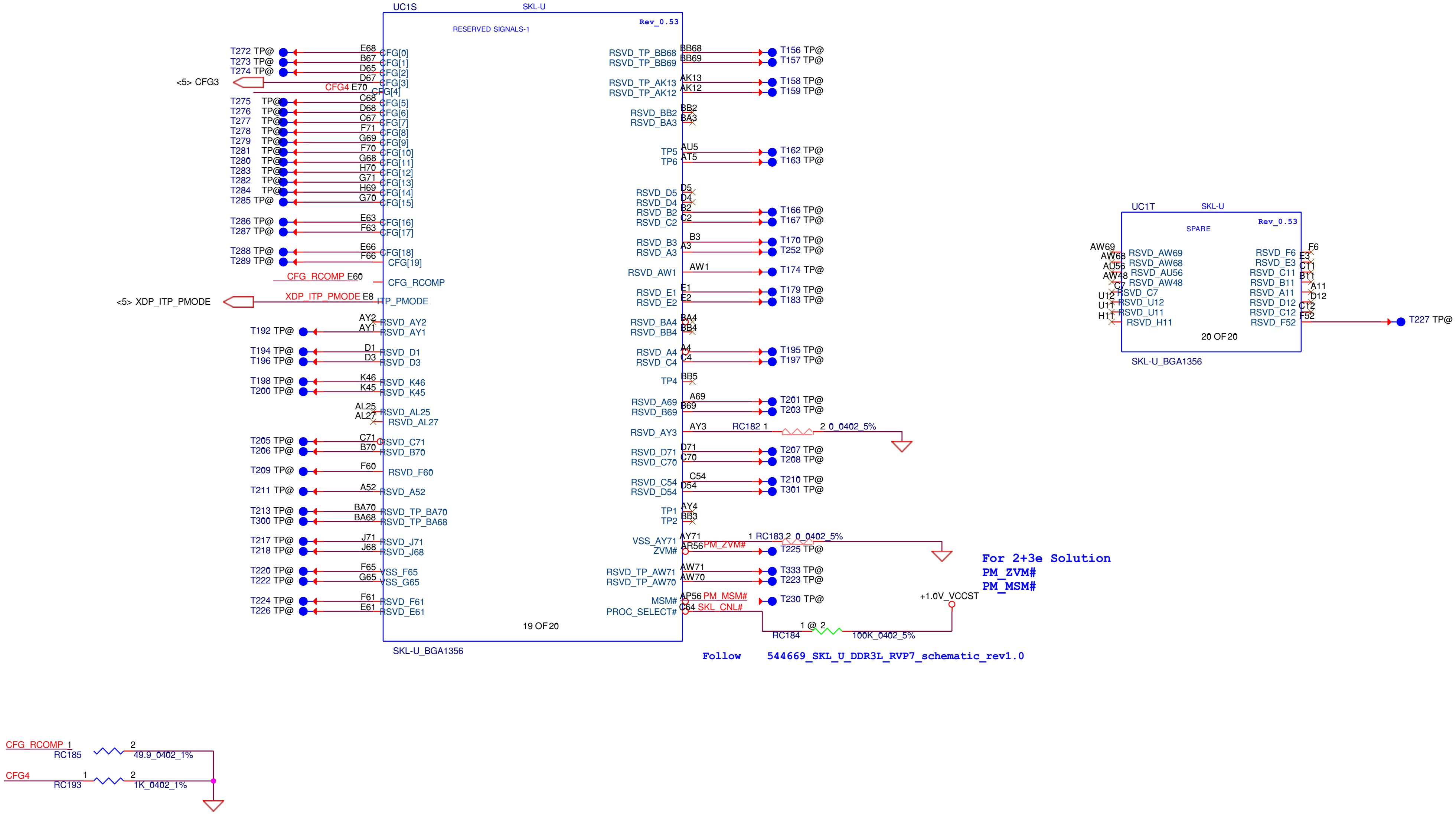

Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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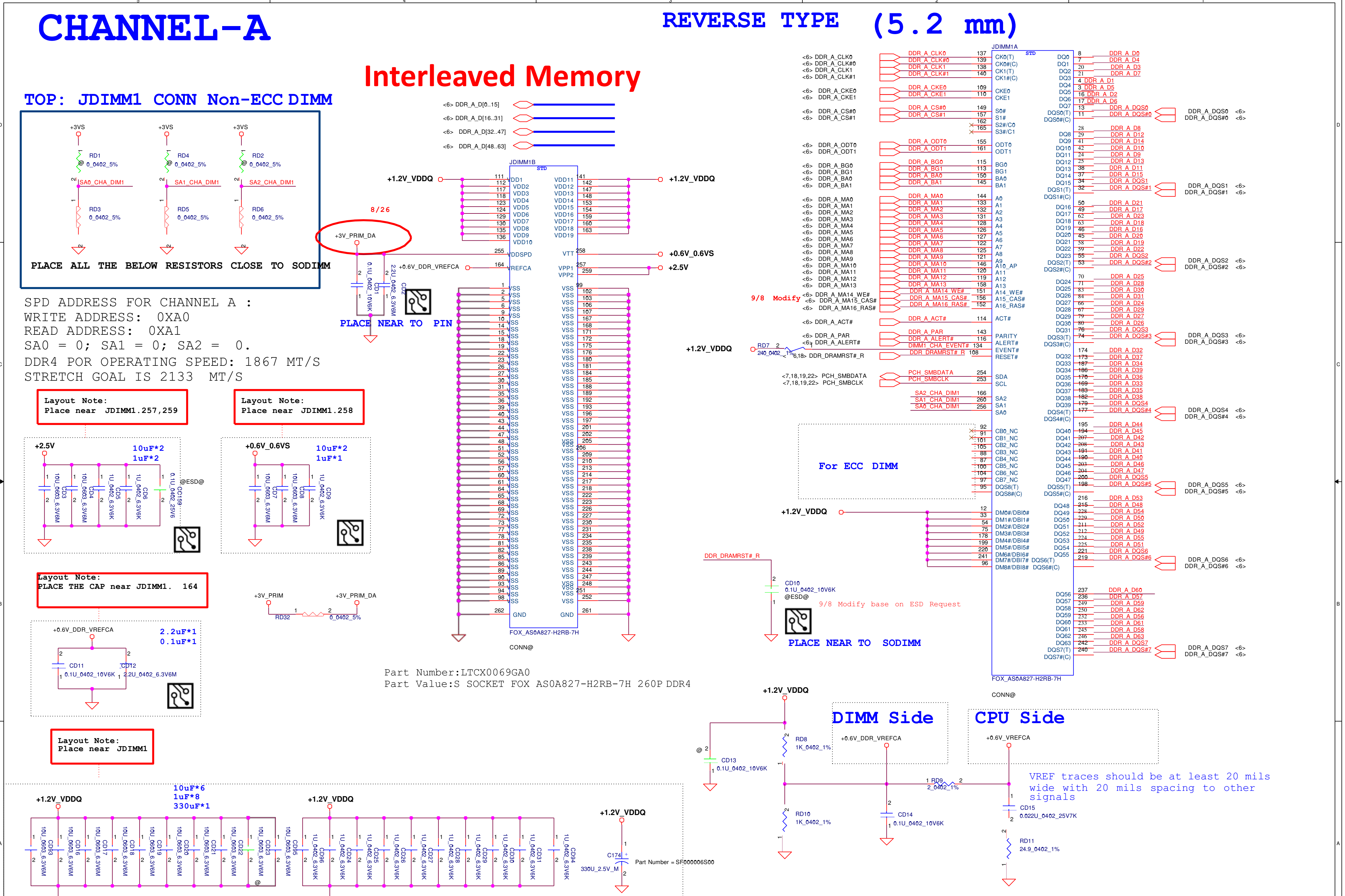
Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: LA-D707P | Rev: v0.2



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/08/03	Deciphered Date 2015/12/31	Title: P18-DDRIV_CHA:DIMM0
			Size / Document Number: LA-D707P / Rev v0.2
			Date: Wednesday, May 11, 2016 / Sheet 17 of 60

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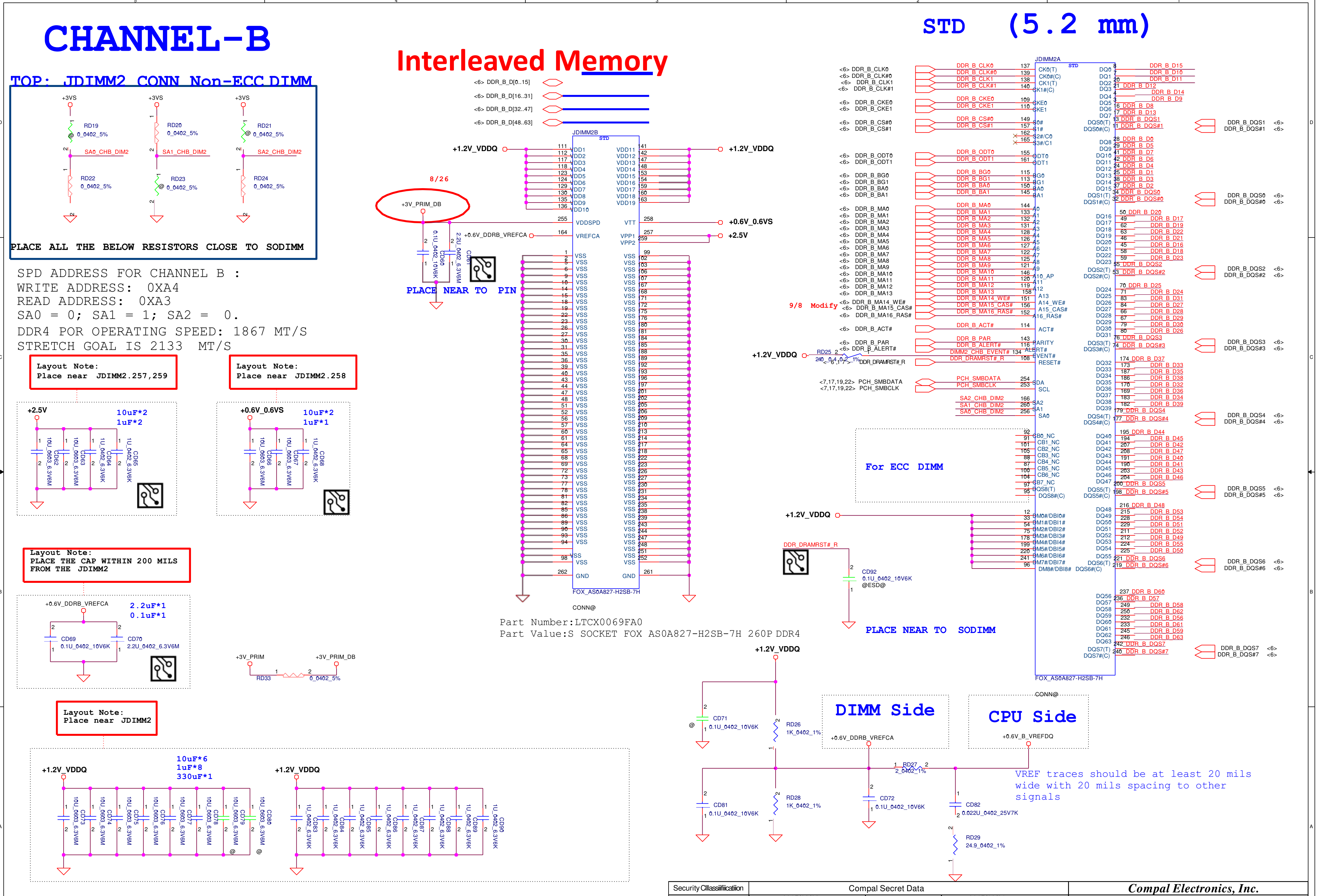
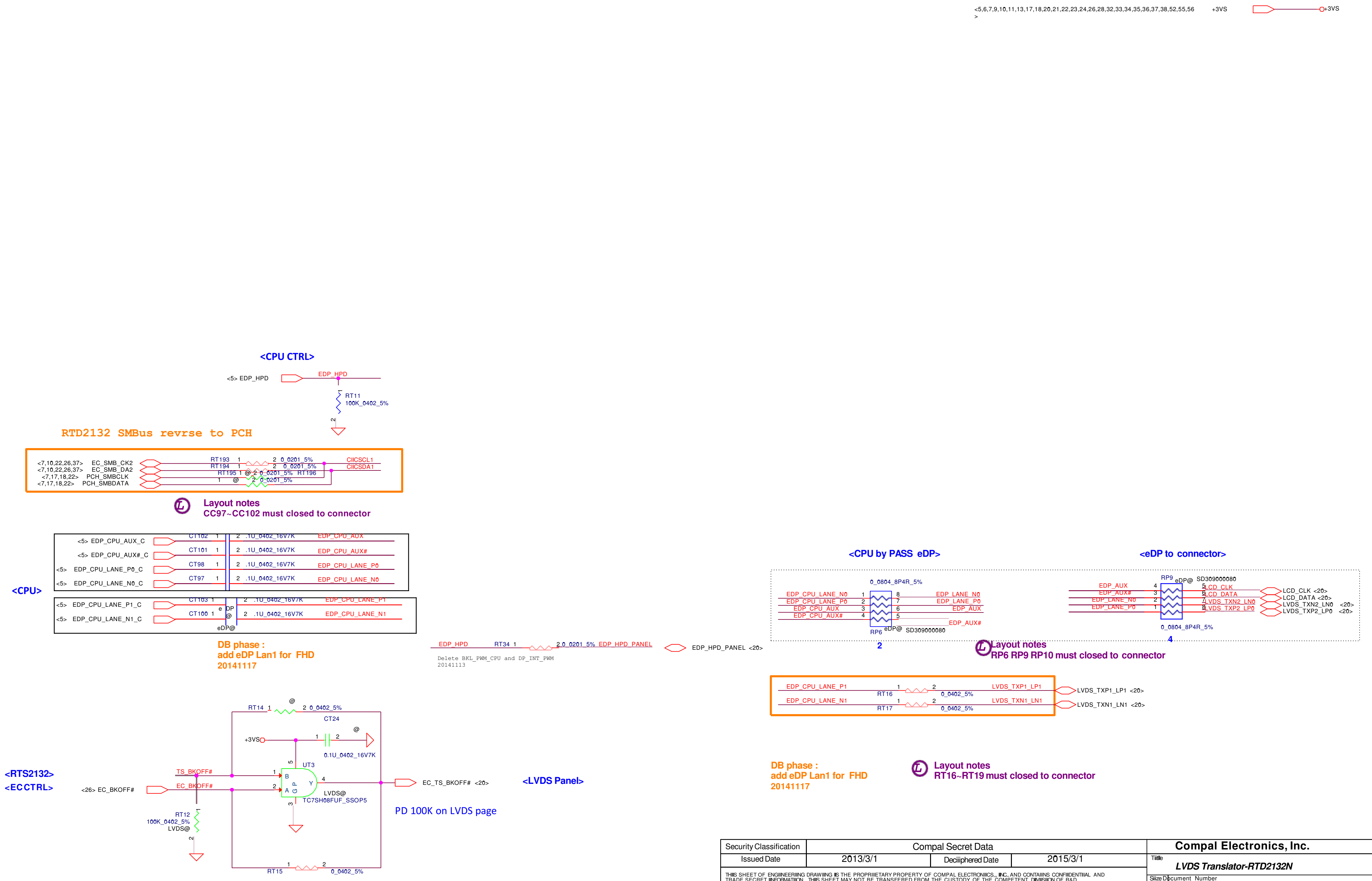


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/08/03	Deciphered Date	2015/12/31	Title: P19-DDRIV_CHB: DIMM0
				Size Document Number: LA-D707P Rev v0.2
				Date: Wednesday, May 11, 2016 Sheet 18 of 60



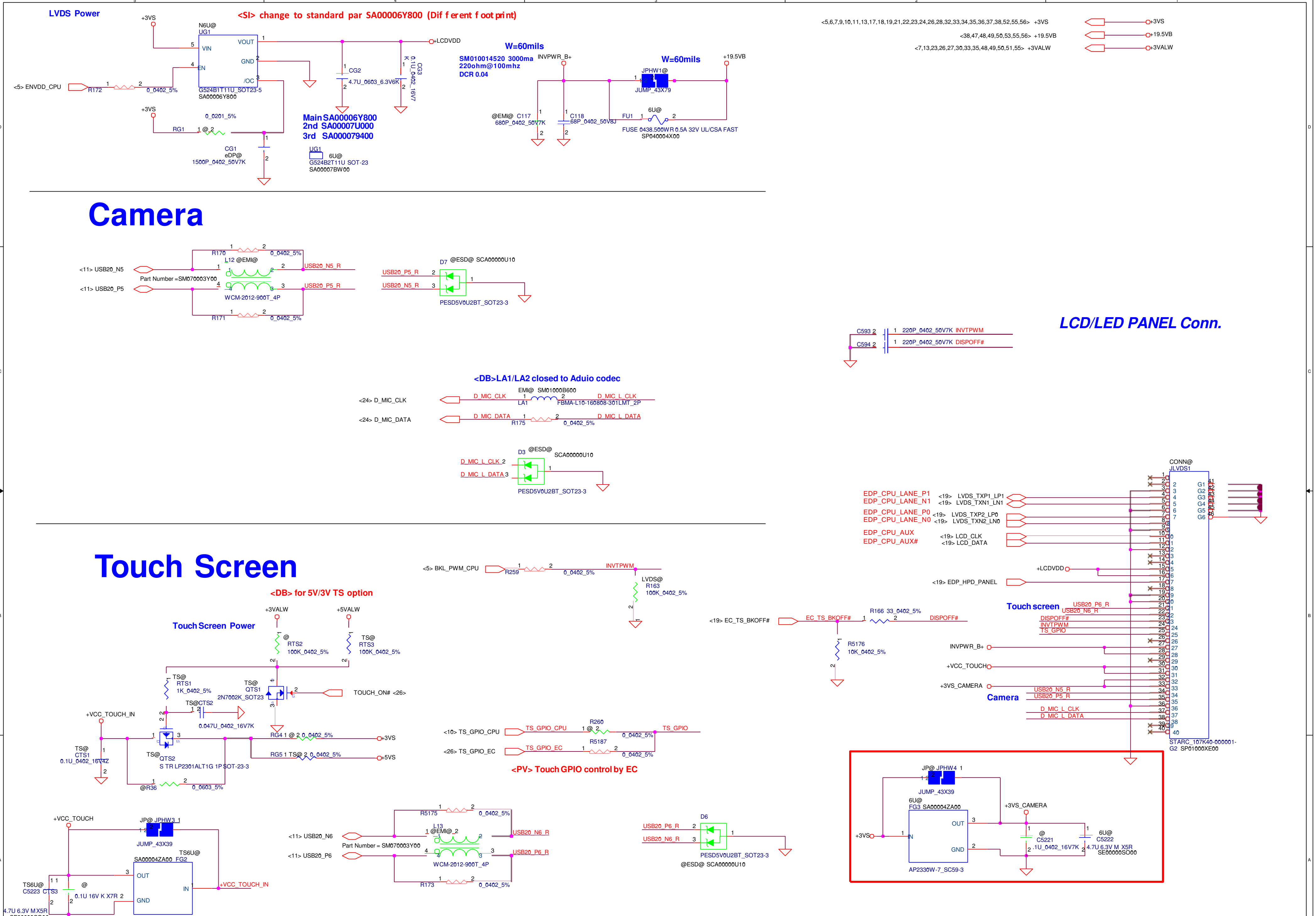
Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

Compal Electronics, Inc.

Title: *LVDS Translator-RTD2132N*

Size Document Number: LA-D707P — Rev v0.2

Date: Wednesday, May 11, 2016 — Sheet 19 of 60



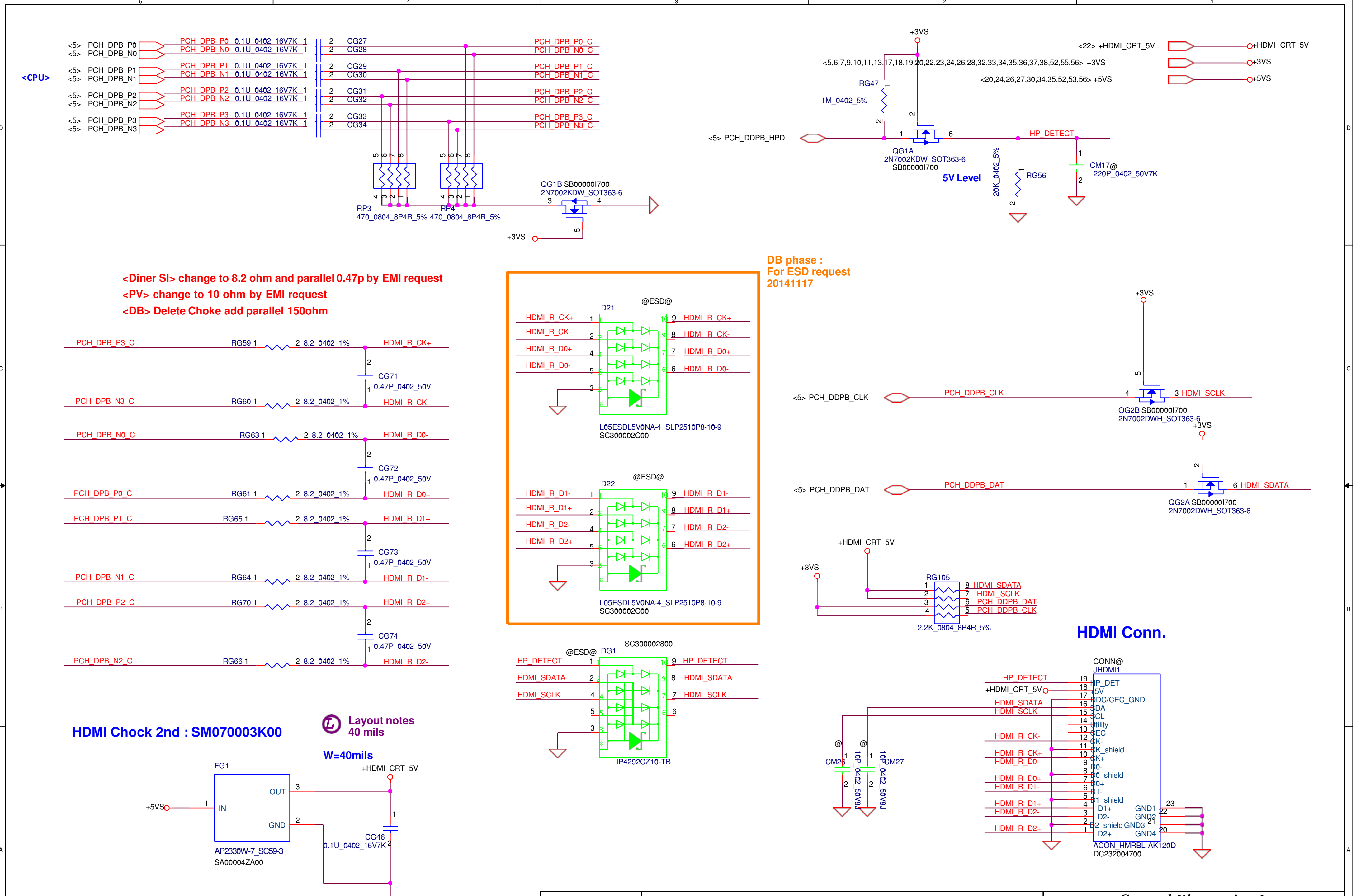
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: LVDS Connector

Size | Document Number: LA-C707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 20 of 60

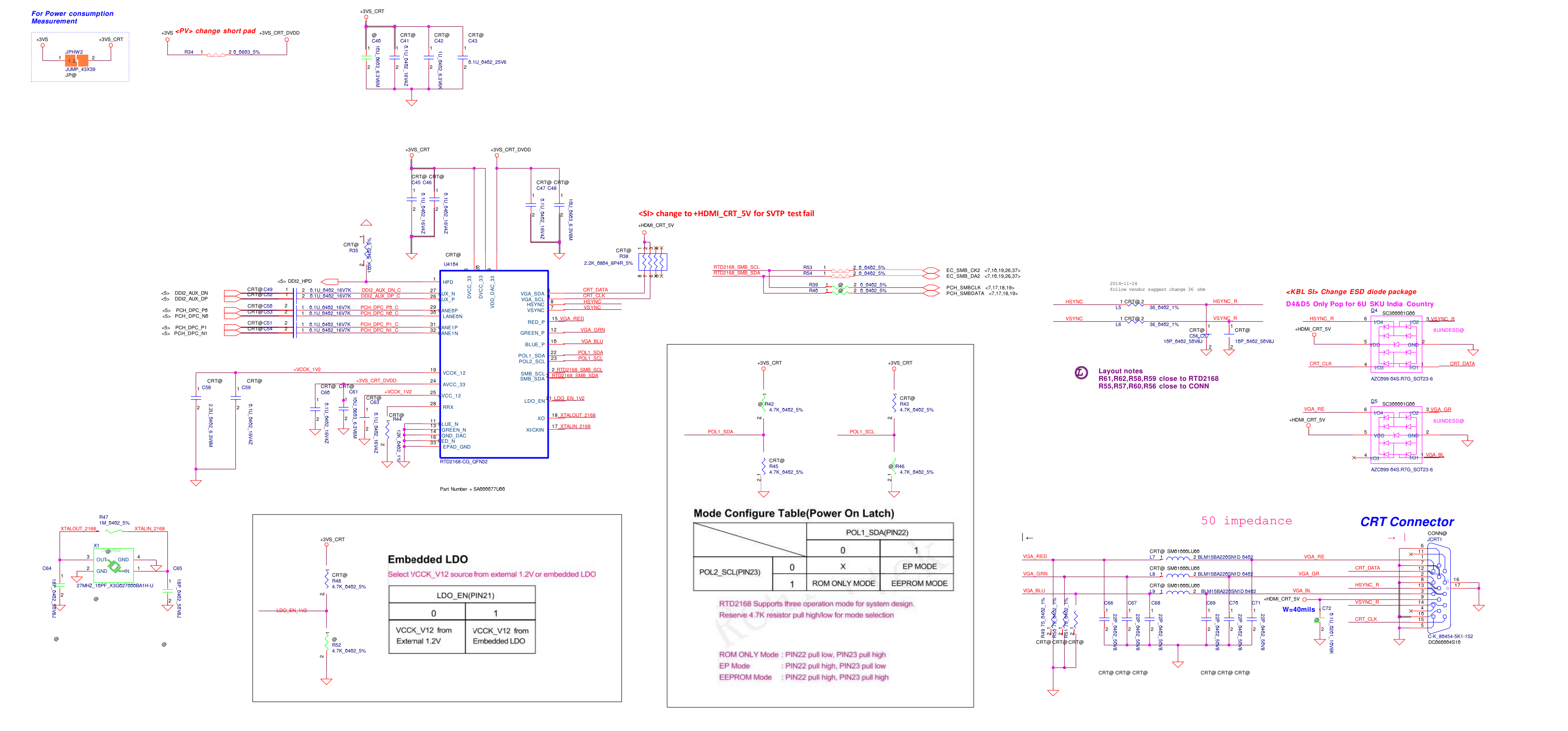


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date 2011/06/29	Title: HDMI Conn/Level shift

Size Document Number: LA-D707P — Rev v0.2

Date: Wednesday, May 11, 2016 — Sheet 21 of 60

DP to CRT converter



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

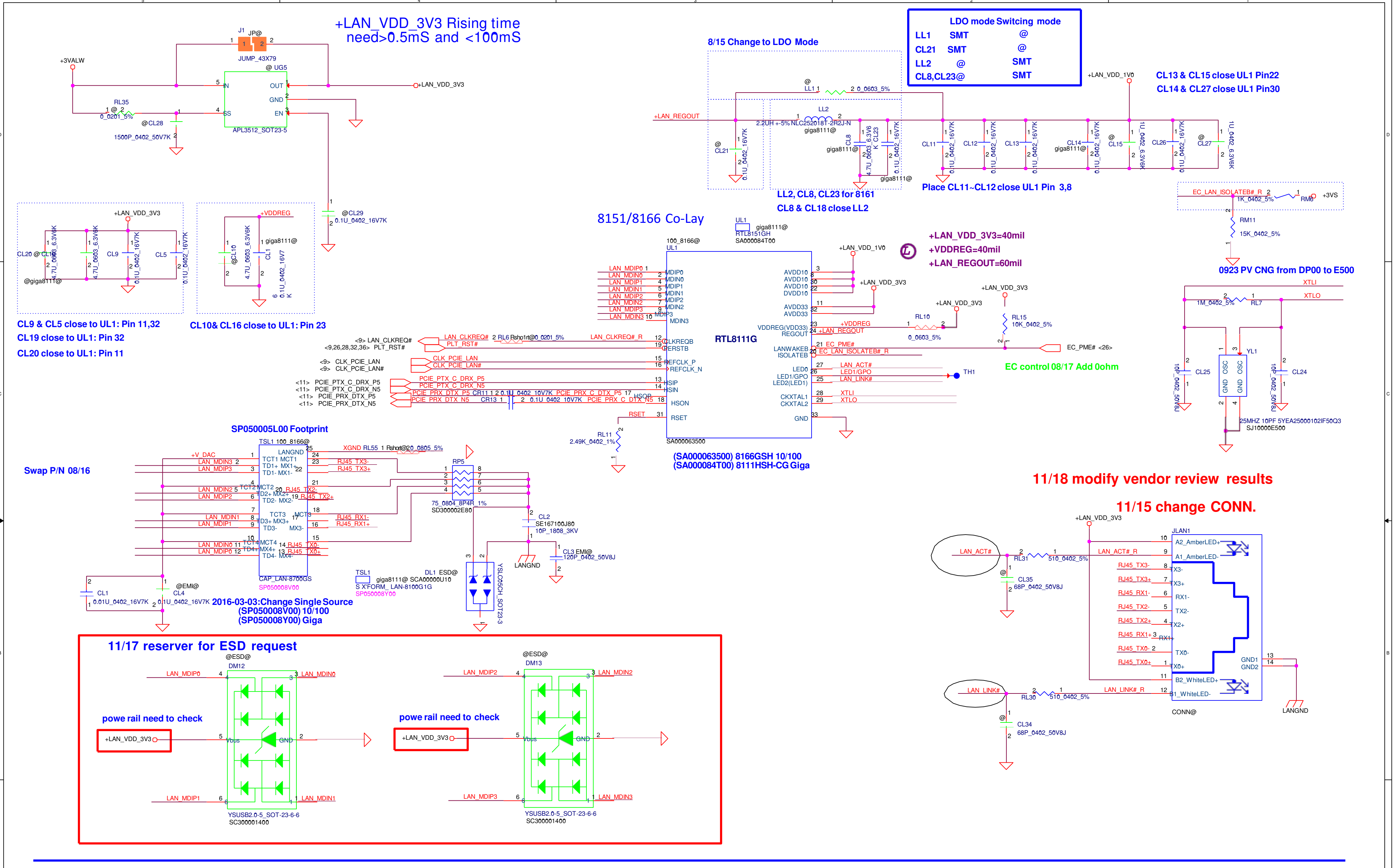
Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode : PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/02/18	Deciphered Date	2015/02/20	Title: DP to CRT RTD2168
				Size: Custom; Document Number: LA-D707P; Rev: v0.2
				Date: Wednesday, May 11, 2016; Sheet 22 of 60



CR RTS5237S move to S/B

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2015/07/08	Title: LAN 8151/8166_ CR RTS5238
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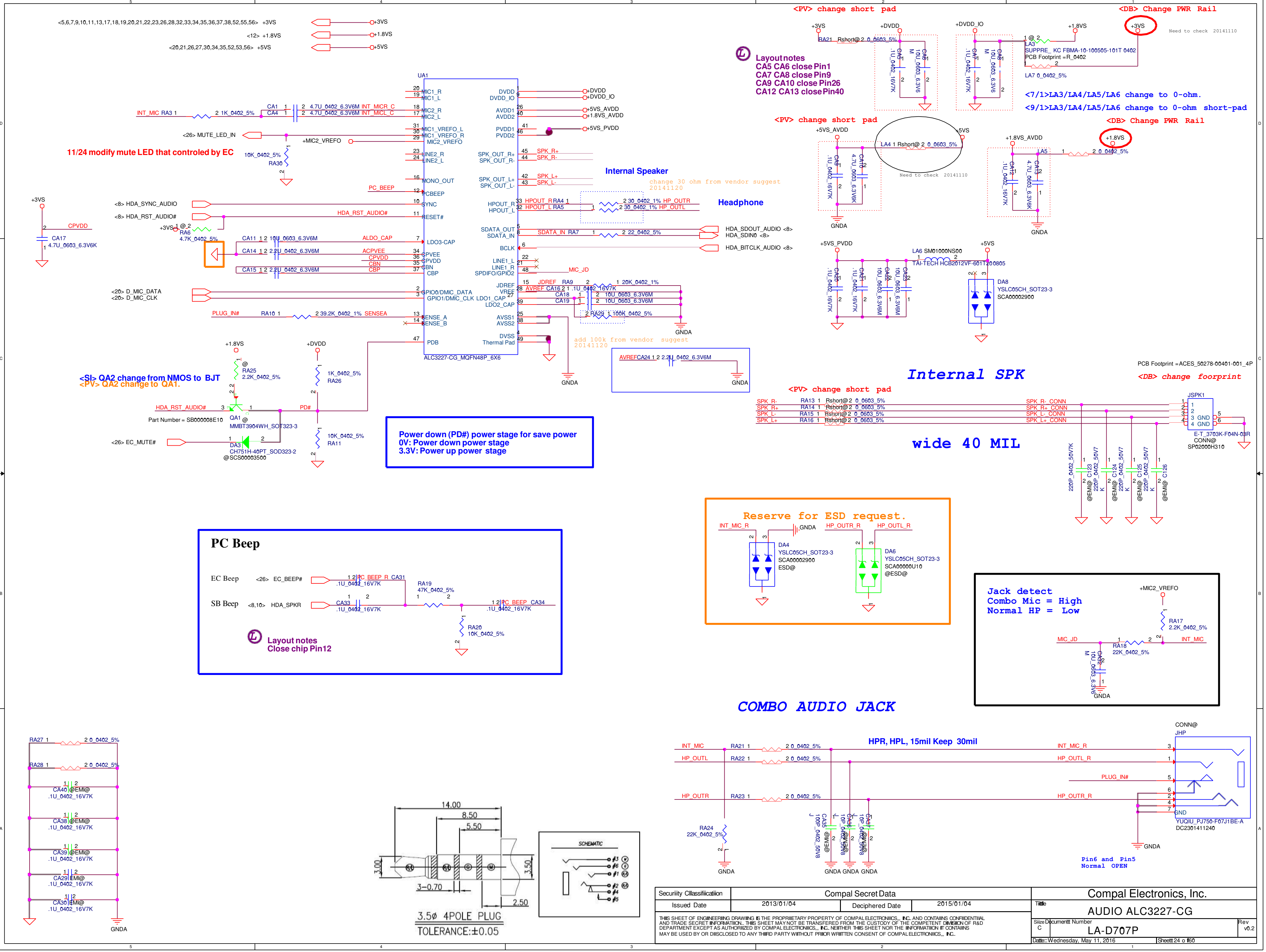
			Date: Wednesday, May 11, 2016 — Sheet 23 of 60



<PV> change short pad
<DB> Change PWR Rail
Need to check 20141110
Layout notes
CA5 CA6 close Pin1
CA7 CA8 close Pin9
CA9 CA10 close Pin26
CA12 CA13 close Pin40
<7/1>LA3/LA4/LA5/LA6 change to 0-ohm.
<9/1>LA3/LA4/LA5/LA6 change to 0-ohm short-pad
11/24 modify mute LED that controled by EC
Internal Speaker
change 30 ohm from vendor suggest 20141120
Headphone
add 100k from vendor suggest 20141120
ALC3227-CG_MQFN48P_6X6
<SI> QA2 change from NMOS to BJT
<PV> QA2 change to QA1.
Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage
Internal SPK
<DB> change foorprint
PCB Footprint = ACES_50278-00401-001_4P
wide 40 MIL
PC Beep
EC Beep
SB Beep
Layout notes
Close chip Pin12
Reserve for ESD request.
Jack detect
Combo Mic = High
Normal HP = Low
COMBO AUDIO JACK
HPR, HPL, 15mil Keep 30mil
Pin6 and Pin5
Normal OPEN
YUQIU_PJ750-F07J1BE-A
DC2301411240
SCHEMATIC
3.5ϕ 4POLE PLUG
TOLERANCE: ±0.05
Security Classification
Compal Secret Data
Issued Date 2013/01/04
Deciphered Date 2015/01/04
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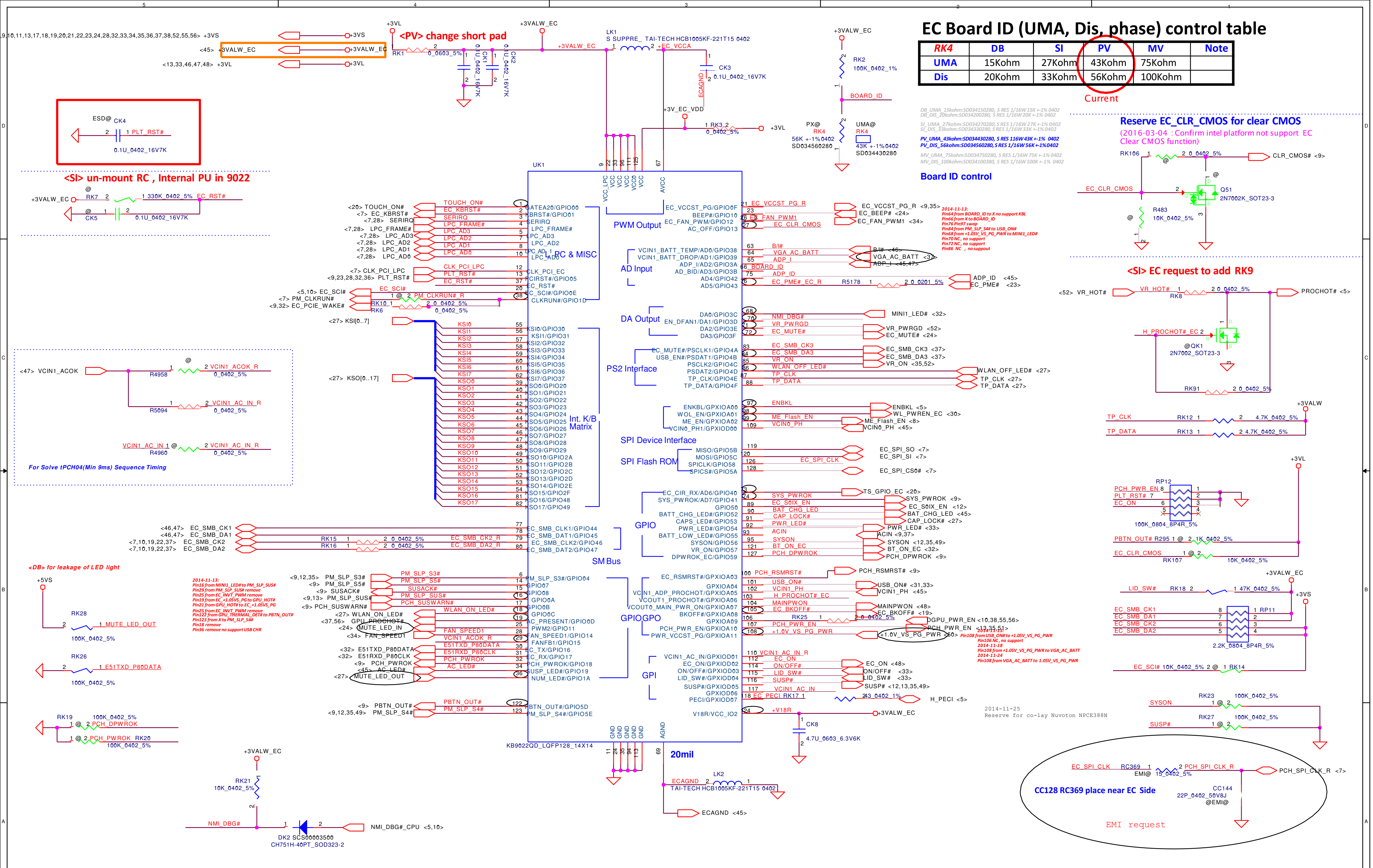
Compal Electronics, Inc.
Title AUDIO ALC3227-CG
Size C Document Number LA-D707P Rev v0.2
Date: Wednesday, May 11, 2016 Sheet 24 of 60



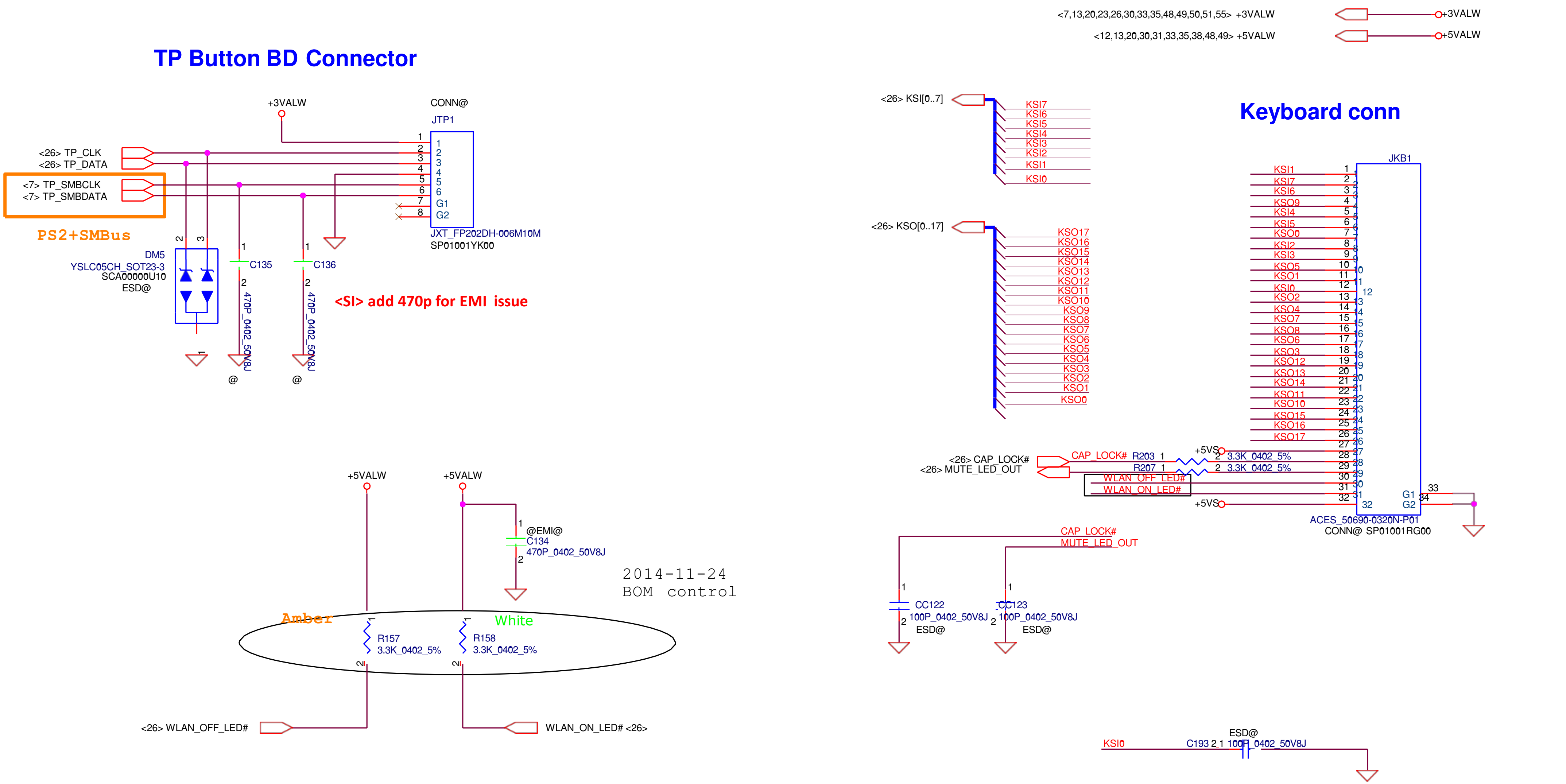
EC Board ID (UMA, Dis, phase) control table

RK4	DB	SI	PV	MV	Note
UMA	15Kohm	27Kohm	43Kohm	75Kohm	
Dis	20Kohm	33Kohm	56Kohm	100Kohm	

Current

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date 2011/06/29	Title: EC ENE-KB9022

Size: Custom Document Number: LA-D707P Rev: v0.2



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: KB/TP

Size	Document Number	Rev
B	LA-D707P	v0.2

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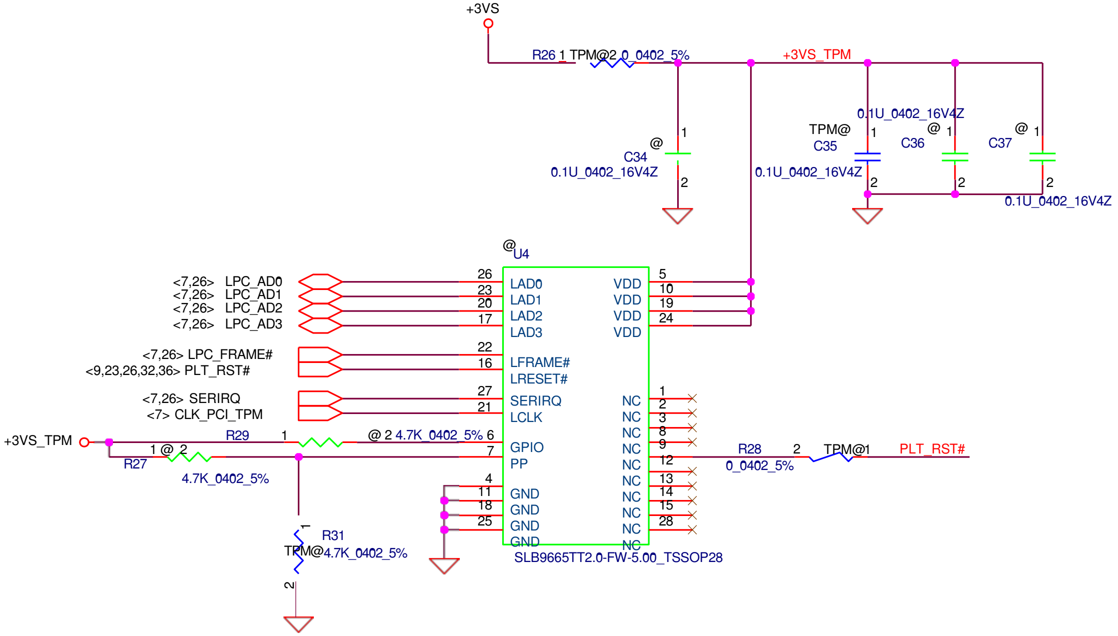
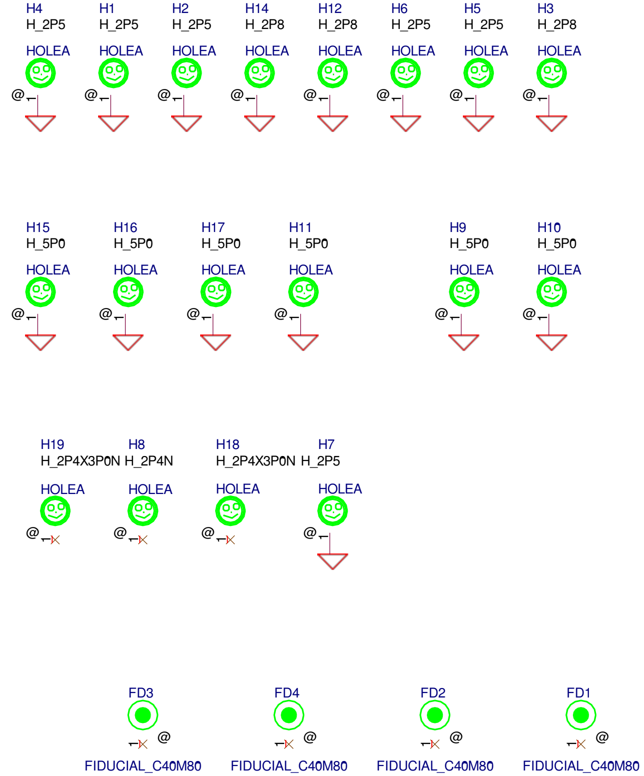
<5,6,7,9,10,11,13,17,18,19,20,21,22,23,24,26,32,33,34,35,36,37,38,52,55,56> +3VS +3VS

TPM2.0



SLB9665 (SA00007XU00)-->TPM2.0
SLB9660 (SA00007AB00) -->TPM1.2

Screw Hole



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: TPM/Screw
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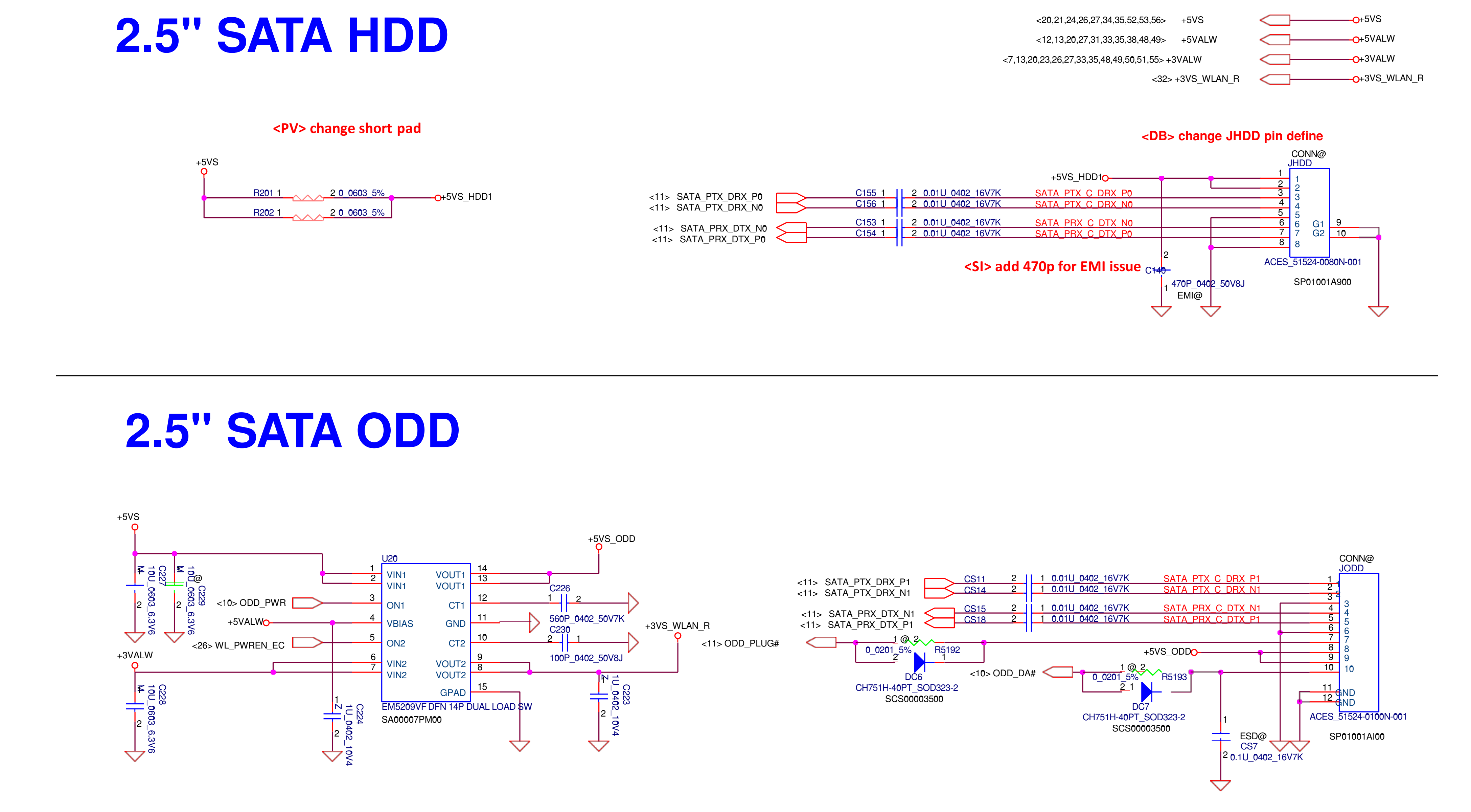
				Date: Wednesday, May 11, 2016; Sheet 28 of 60



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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: HDD/ODD Conn
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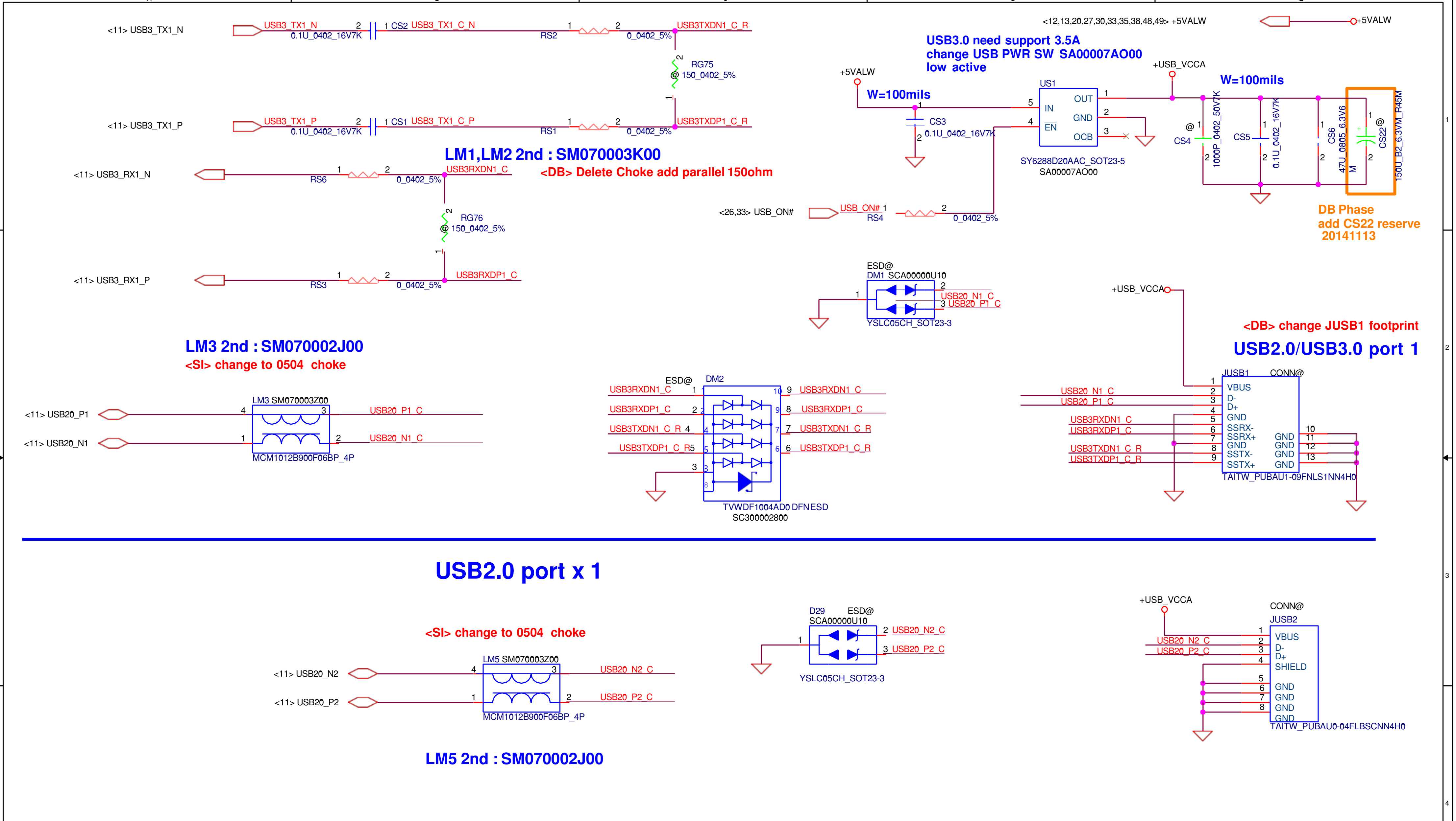
				Date: Wednesday, May 11, 2016; Sheet 30 of 60



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: USB 3.0/2.0 conn

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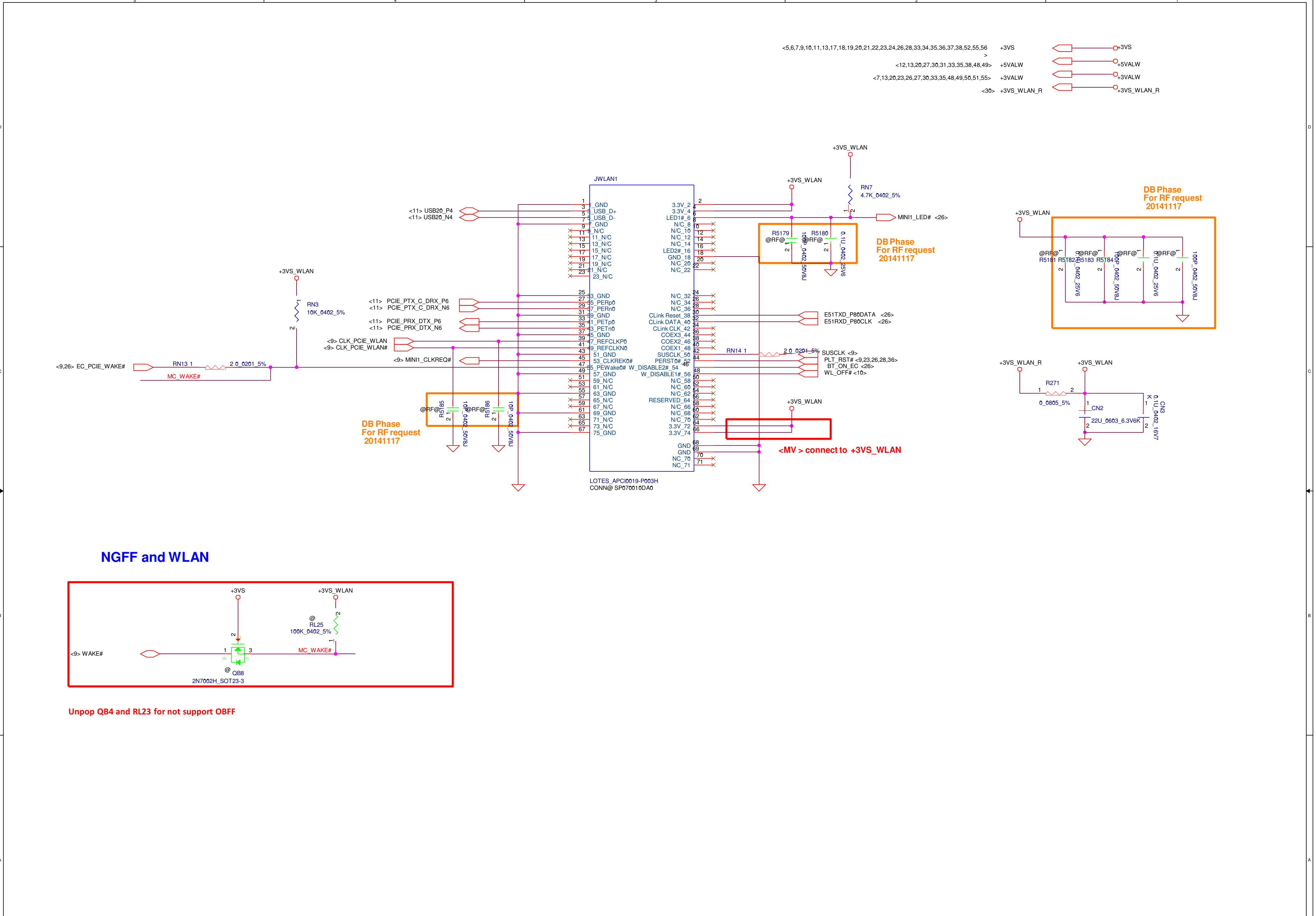
Size: B | Document Number: LA-D707P | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 31 of 60



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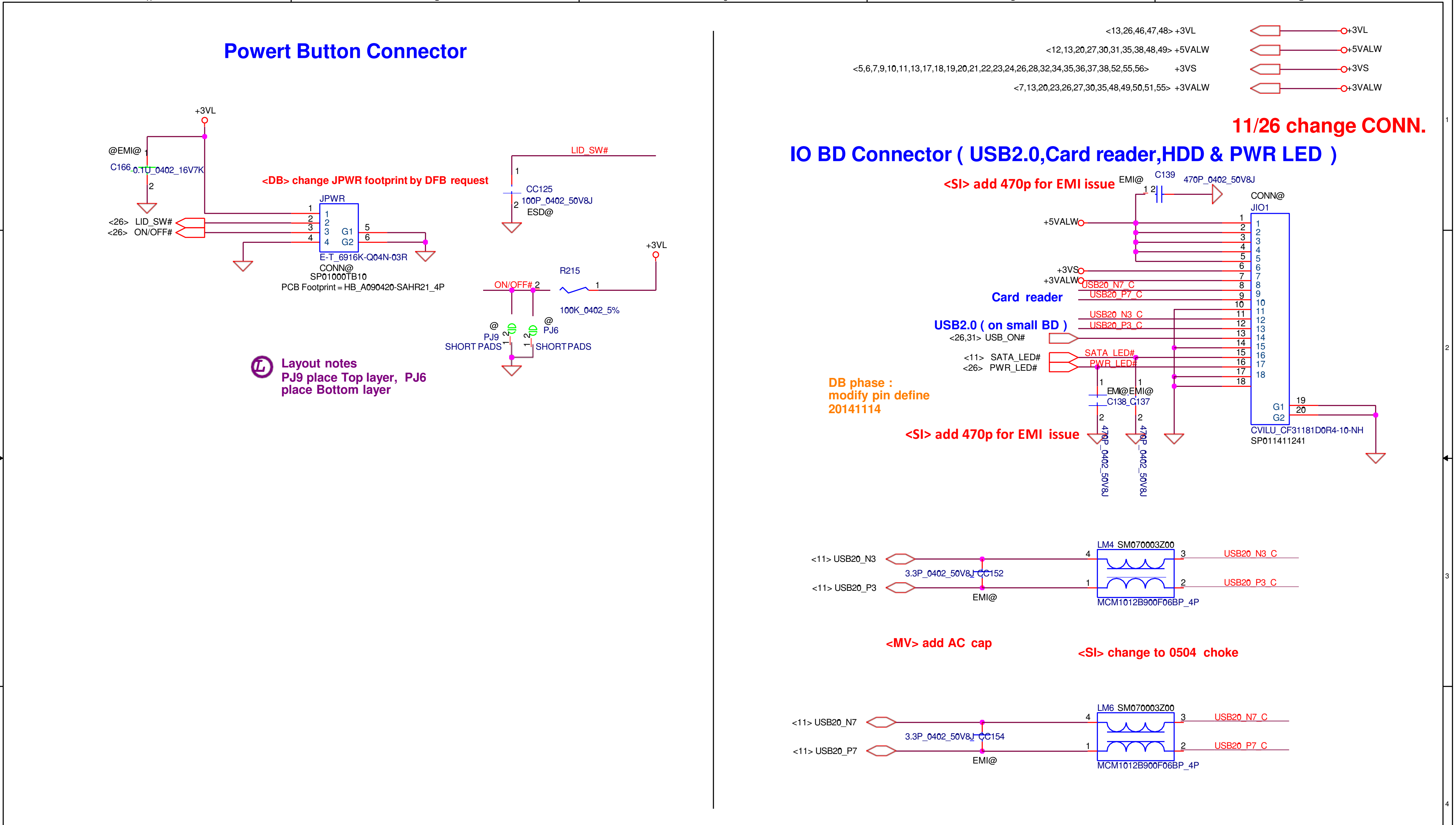
			Date: Wednesday, May 11, 2016 Sheet 32 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

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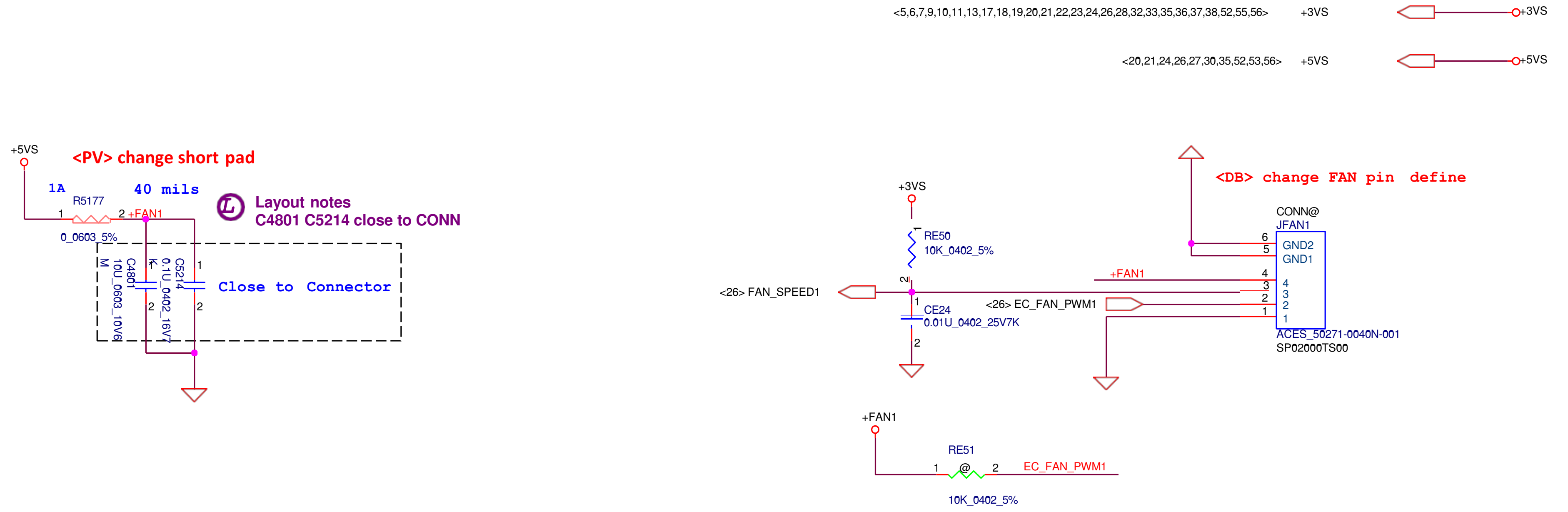
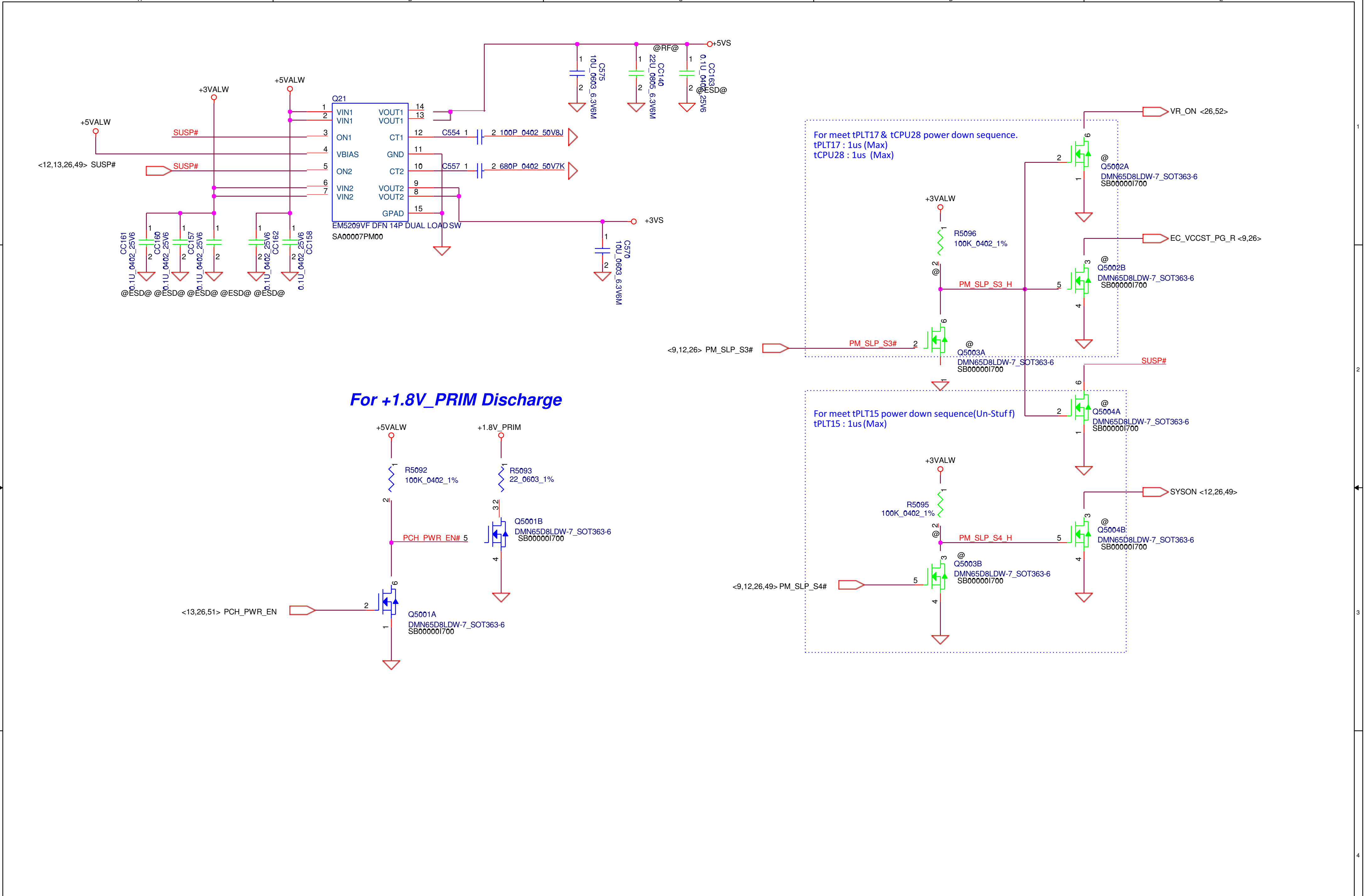
Title	IO CON	
Size B	Document Number LA-D707P	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 33 of 60	

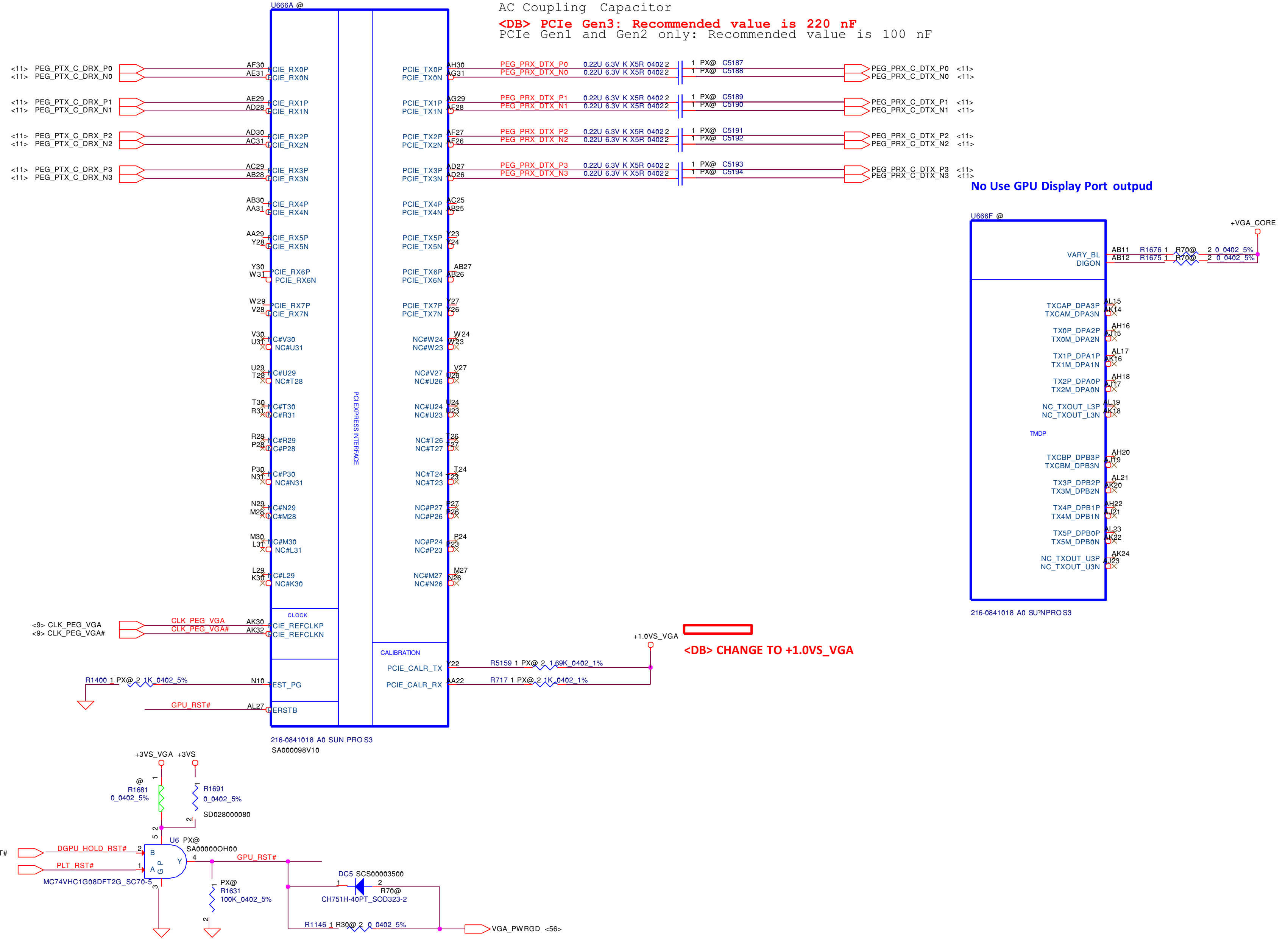


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title: FAN

Size	Document Number	Rev
B	LA-D707P	v0.2



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/10/09	Deciphered Date	2015/12/31	Title: DC Interface
				Size: Custom; Document Number: LA-D707P; Rev: v0.2
				Date: Wednesday, May 11, 2016; Sheet 35 of 60



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title: SUN_PCIE/DP
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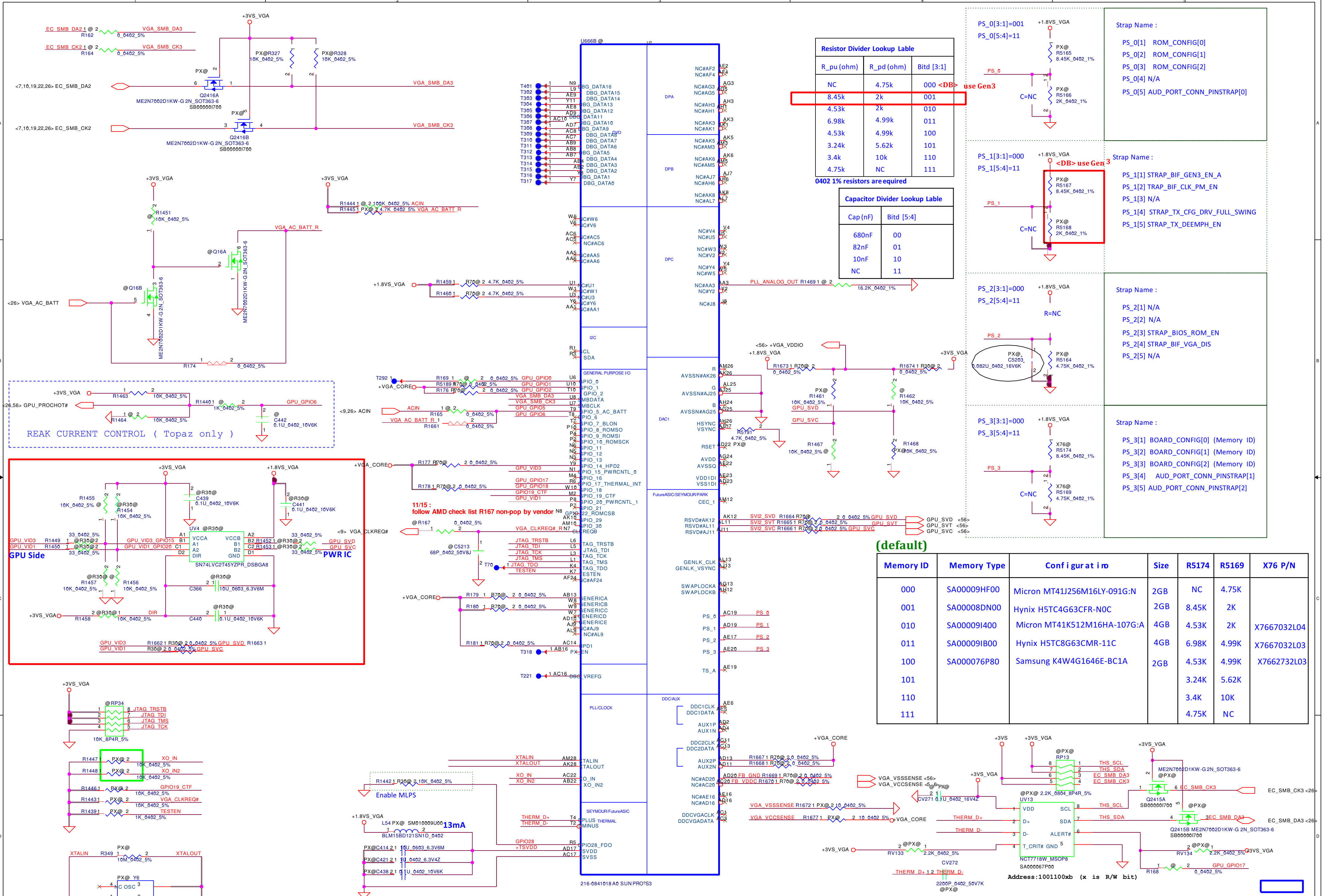
				Date: Wednesday, May 11, 2016; Sheet 36 of 60



Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000 <DB> use Gen3
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000
PS_1[5:4]=11
<DB> use Gen 3

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

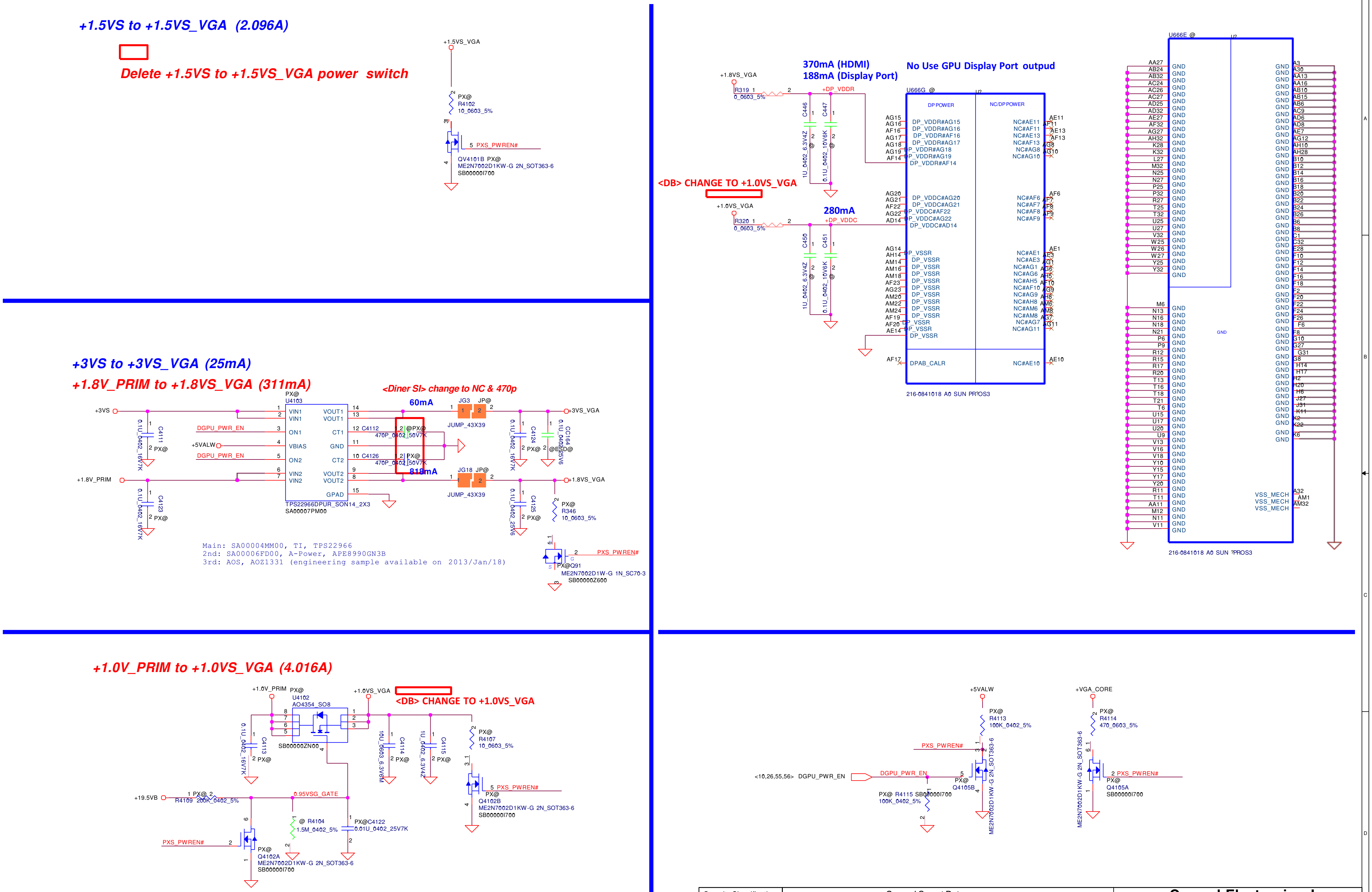
Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

(default)

Memory ID	Memory Type	Conf i gur at i m	Size	R5174	R5169	X76 P/N
000	SA00009HF00	Micron MT41J256M16LY-091G:N	2GB	NC	4.75K	
001	SA00008DN00	Hynix H5TC4G63CFR-N0C	2GB	8.45K	2K	
010	SA00009I400	Micron MT41K512M16HA-107G:A	4GB	4.53K	2K	X7667032L04
011	SA00009IB00	Hynix H5TC8G63CMR-11C	4GB	6.98K	4.99K	X7667032L03
100	SA000076P80	Samsung K4W4G1646E-BC1A	2GB	4.53K	4.99K	X7662732L03
101				3.24K	5.62K	
110				3.4K	10K	
111				4.75K	NC	



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title: SUN_Power/GND

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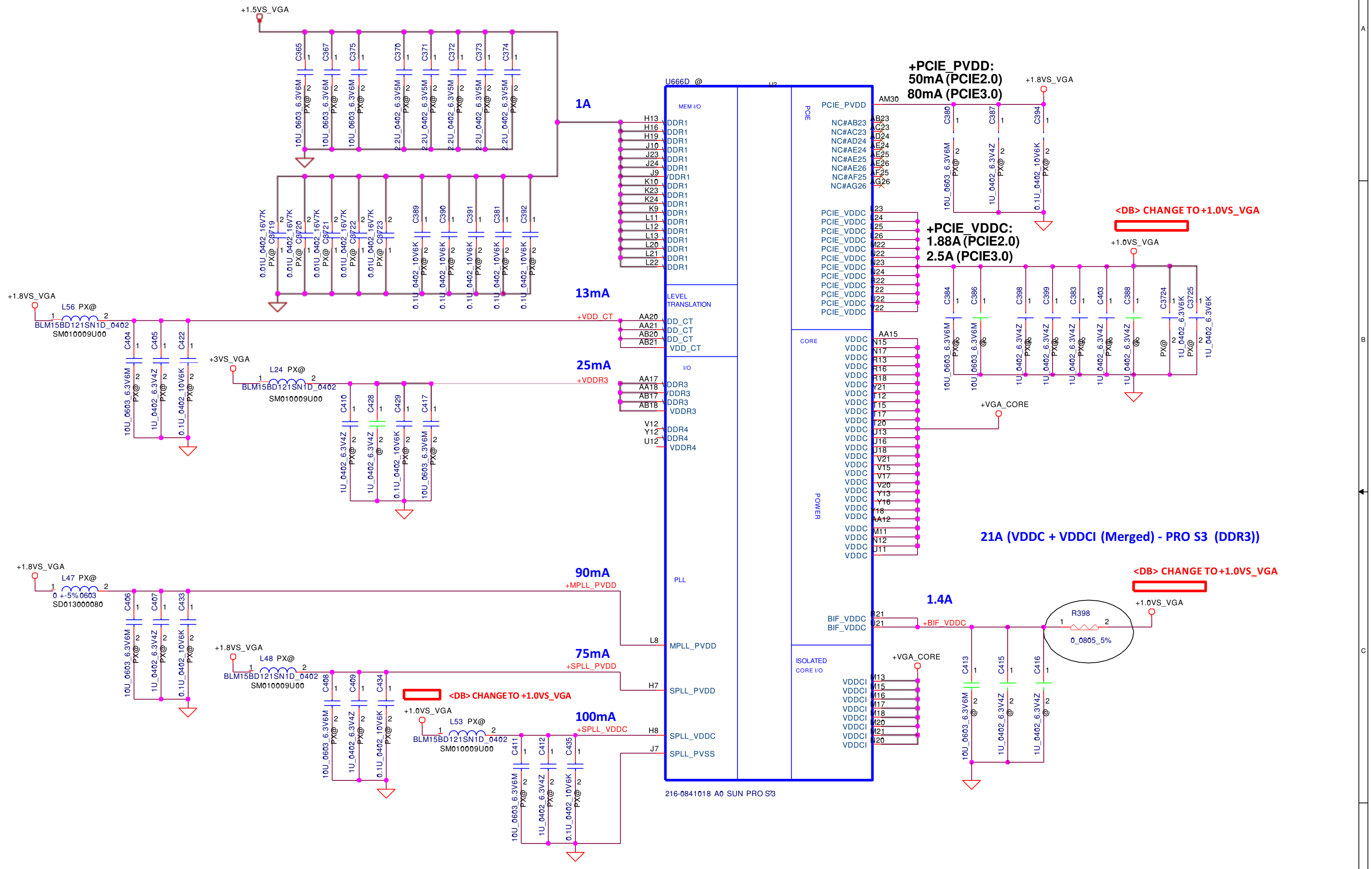
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+1.0VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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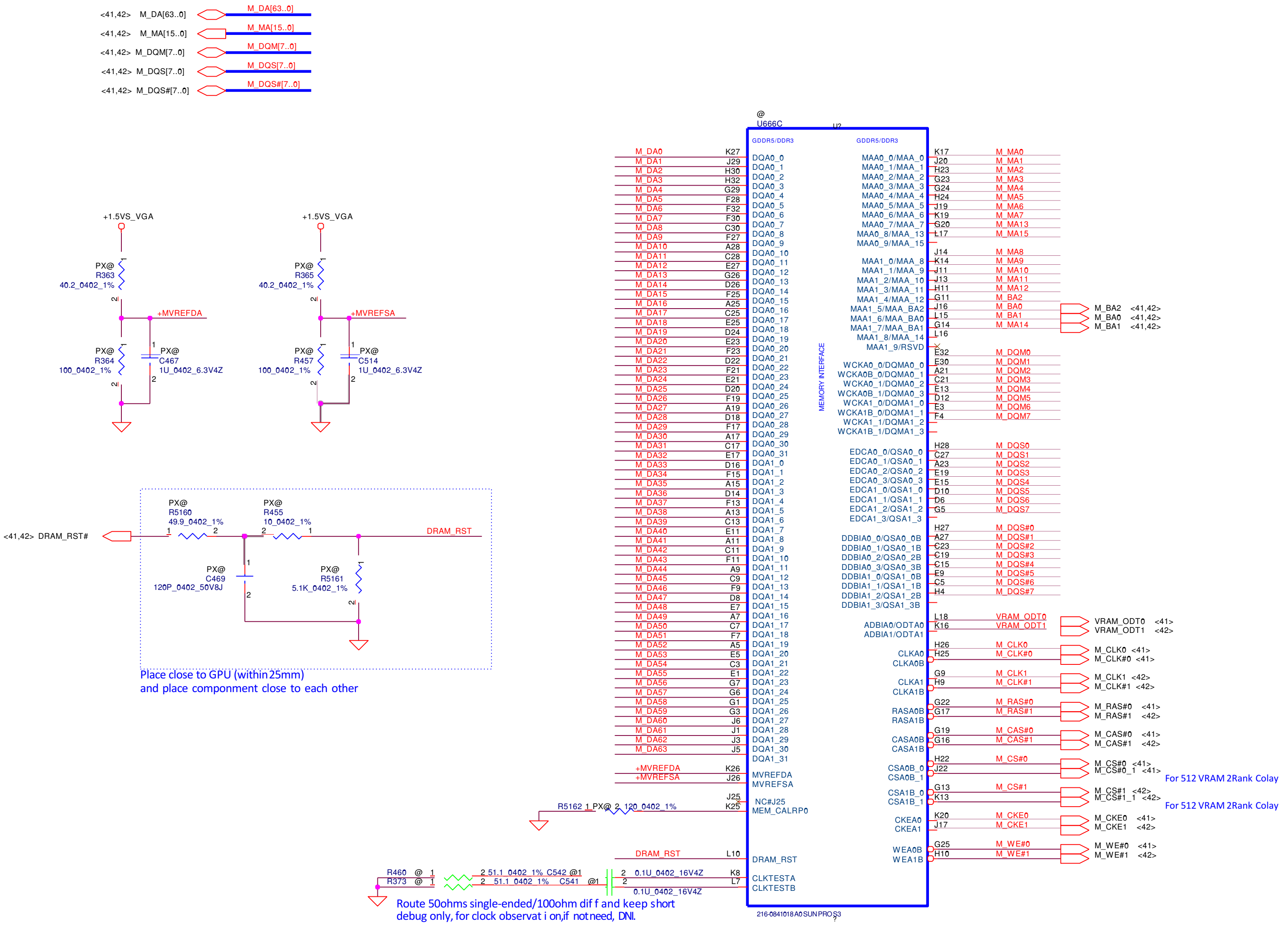
Compal Electronics, Inc.

Title: **SUN_Power**

Size: Custom | Document Number: **LA-D707P** | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 39 of 60



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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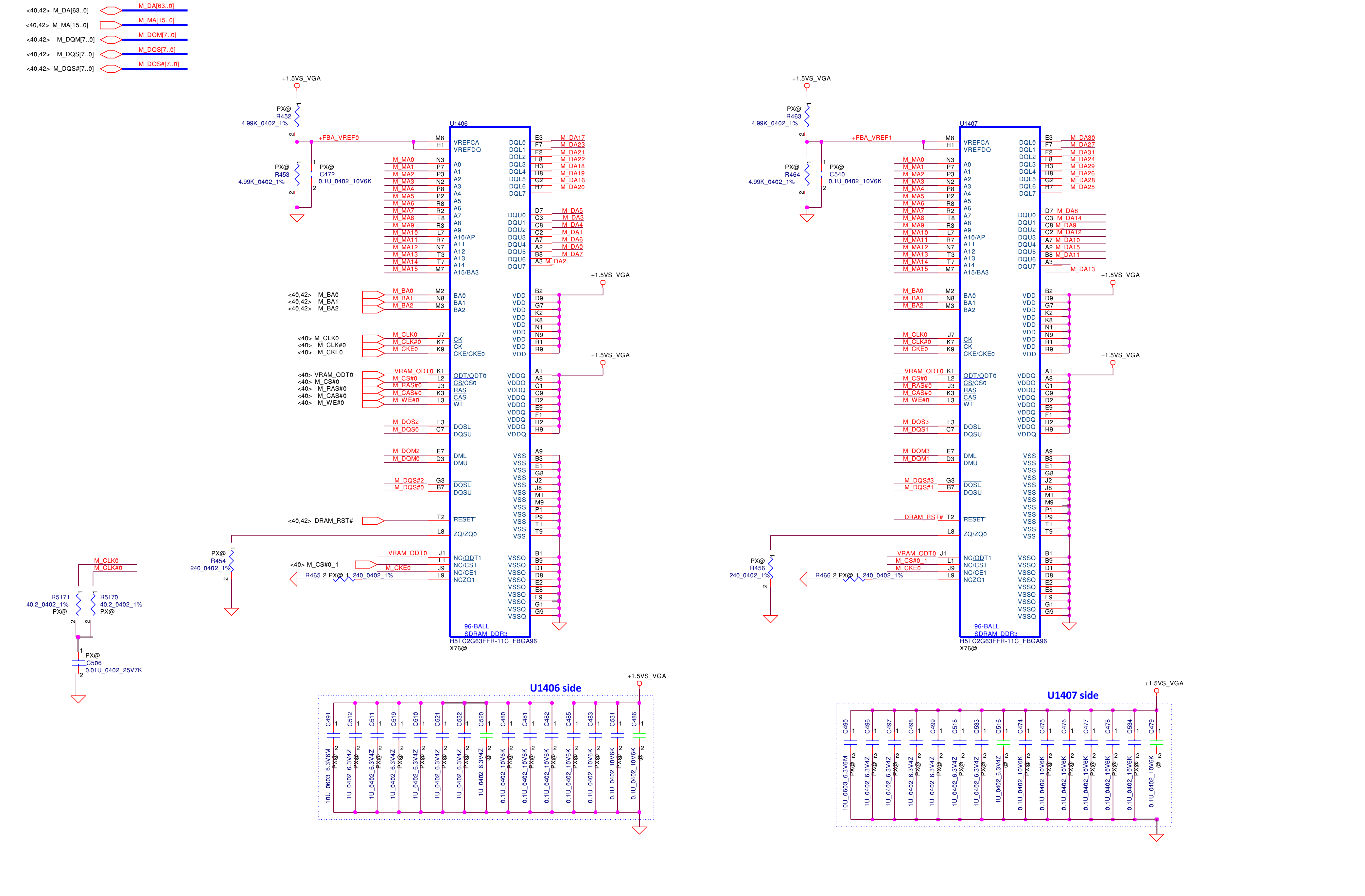
Compal Electronics, Inc.

Title: **SUN_MEM**

Size: Custom | Document Number: **LA-D707P** | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 40 of 60

Memory Partition A - Lower 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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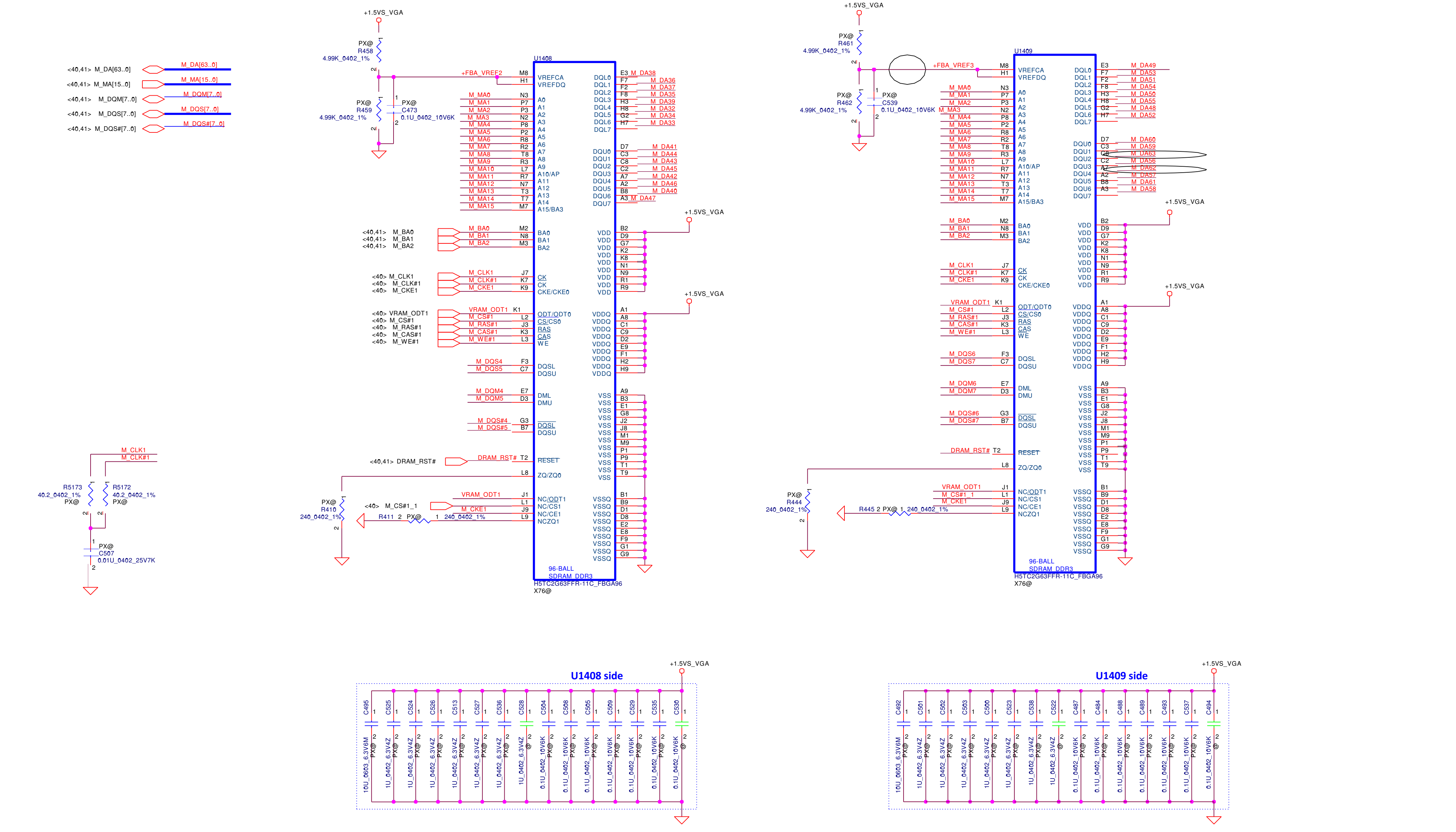
Compal Electronics, Inc.

Title: **SUN_VRAM A Lower**

Size: Custom | Document Number: **LA-D707P** | Rev: v0.2

Date: Wednesday, May 11, 2016 | Sheet 41 of 60

Memory Partition A - Upper 32 bits



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

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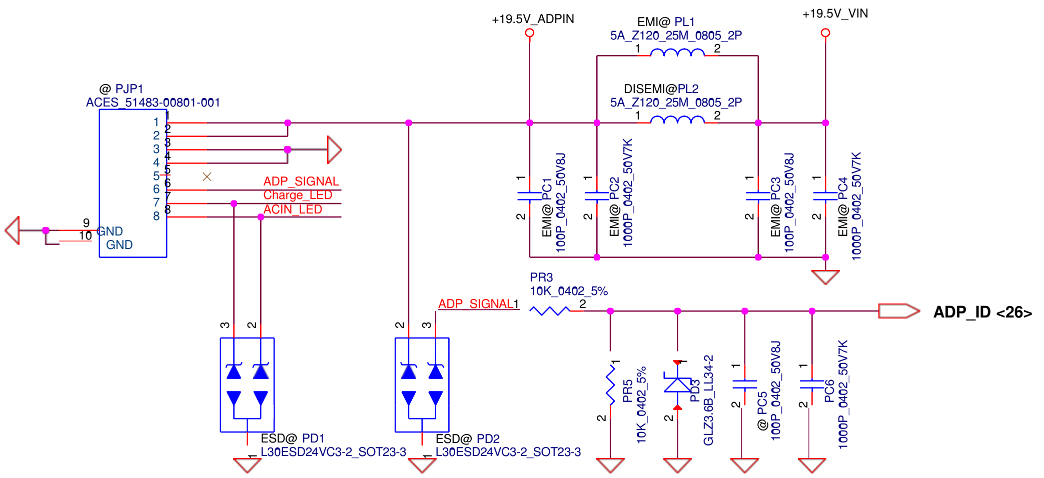
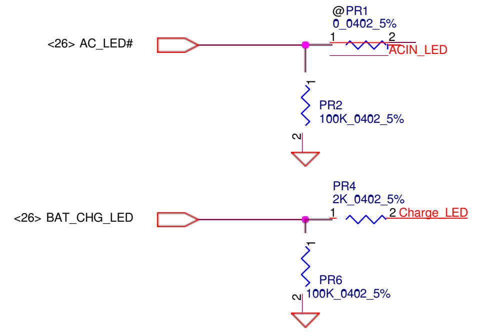
Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

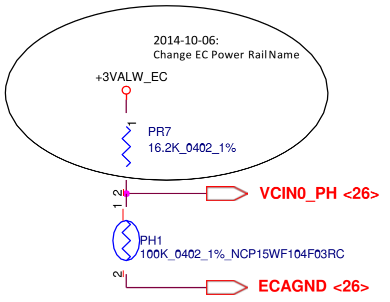
Size: Custom | Document Number: **LA-D707P** | Rev: v0.2

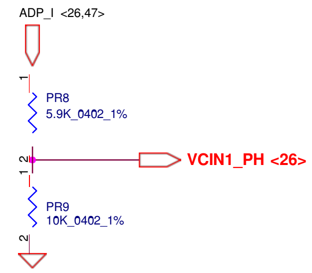
Date: Wednesday, May 11, 2016 | Sheet 42 of 60





ADP_ID			
Adapter Type		Voltage Range (Dec)	Voltage Range (Hex)
None	Normal Adapter	<0.211V	< 10
	Air-Line Apdater	<0.334V	< 1A
40W	Normal Adapter	>=0.211V ;<0.349V	>= 10 < 1A
45W	Normal Adapter	>=0.349 ;<0.442	>= 1A < 20
65W	Normal Adapter	>=0.442V ;<0.549V	>=20 <2A
	Air-Line Apdater	>=0.334V ;<0.425V	>= 1A < 21
90W	Normal Adapter	>=0.549V ;<0.710V	>= 2A < 36
	Air-Line Apdater	>=0.425 ;<1.391V	>= 21 < 6A
120W	Normal Adapter	>=0.710V ;<1.391V	>= 36 < 6A
ID is shorted to VIN		>=1.391V with Normal and Air-Line	>= 6A





	Initail	Recovery
OTP	92 C	56 C

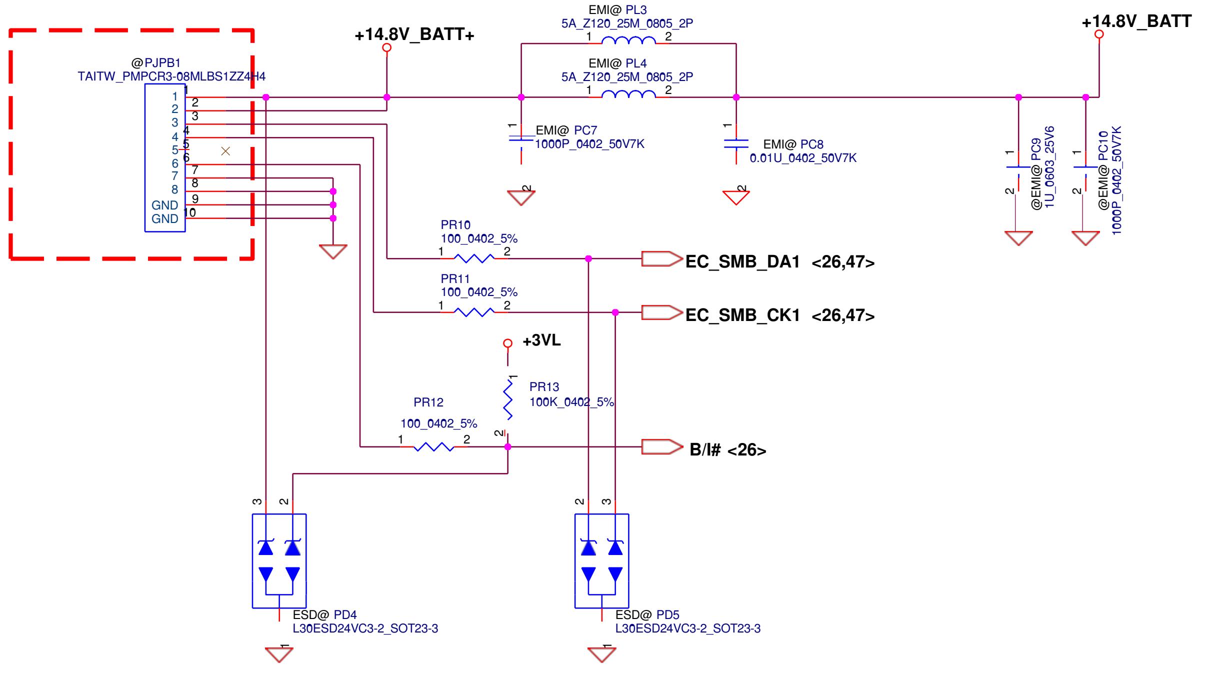
	Initail	Recovery
45W UMA	0.65V	0.45V
65W DIS	0.95V	0.67V

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

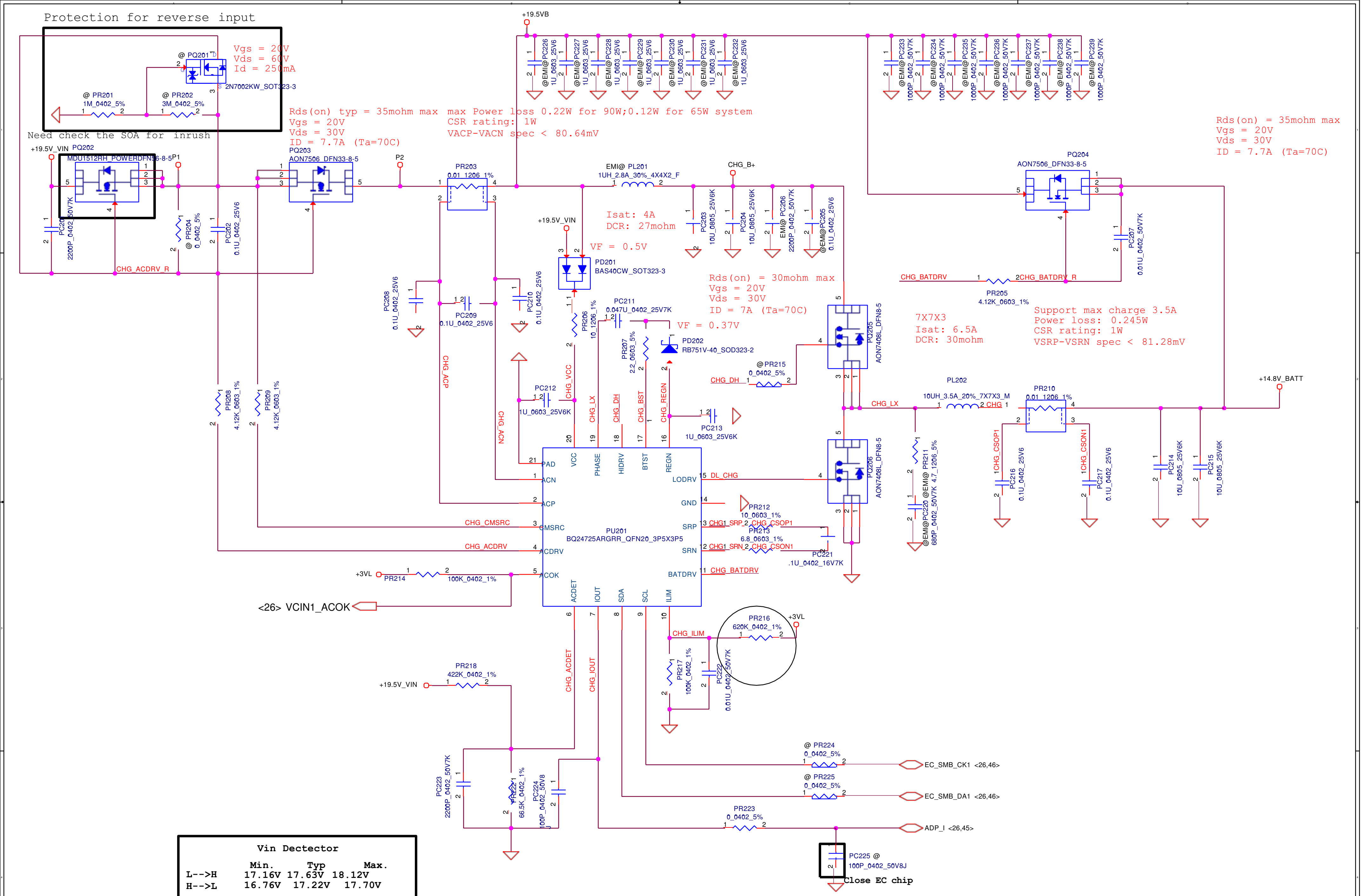
Compal Electronics, Inc.

Title: **DC Conn**

Size | Document Number: **LA-D707P** | Rev: v0.2



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/09	Deciphered Date	2018/10/09	Title: BATT Conn
				Size: Document Number: LA-D707P Rev: v0.2
				Date: Wednesday, May 11, 2016 Sheet 46 of 60



Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr

ILIM = 3.3*100/(100+620)/20/0.01

= 2.29 A

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: CHARGER(BQ24725)

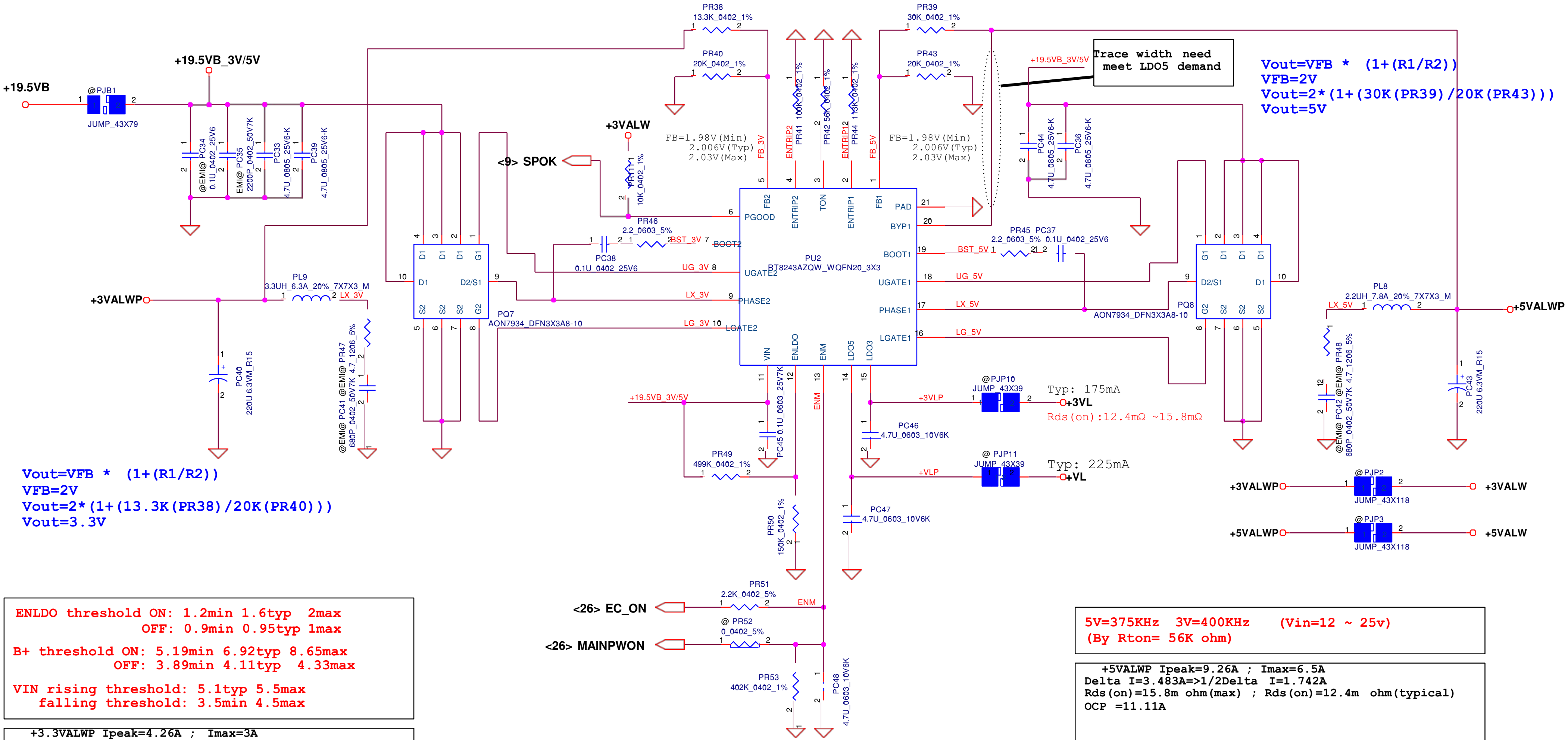
Size Document Number | Rev v0.2

Date: Wednesday, May 11, 2016 |

ENLDO (V)	ENM (V)	ENTRIP1 (V)	ENTRIP2 (V)	LDO5	LDO3	+5VALW	+3VALW
Low	Low	X	X	Off	Off	Off	Off
">1.6V" =>High	Low	X	X	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	Off	On	On	Off	Off
">1.6V" =>High	">2.3V" =>High	Off	On	On	On	Off	On
">1.6V" =>High	">2.3V" =>High	On	On	On	On	On	On
">1.6V" =>High	">2.3V" =>High	On	Off	On	On	On	Off

Module model information
RT8243A_V1.mdd

ENTRIPx adjustment range: 0.5V~3V, floating or over 4.5V will shutdown channel.



ENLDO threshold ON: 1.2min 1.6typ 2max
OFF: 0.9min 0.95typ 1max

B+ threshold ON: 5.19min 6.92typ 8.65max
OFF: 3.89min 4.11typ 4.33max

VIN rising threshold: 5.1typ 5.5max
falling threshold: 3.5min 4.5max

+3.3VALWP Ipeak=4.26A ; Imax=3A
Delta I=1.92A=>1/2Delta I=0.96A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP = 5.1A

TDC:4.31A Fsw:375KHz
H-MOS PD:0.3736W Δ T:12°C
L-MOS PD:0.2713W Δ T:7.9°C
Choke PD:1.5158W Δ T:24°C
OVP margin for Vos:8% @ 330uF cap, 6% @ 220uF

5V=375KHz 3V=400KHz (Vin=12 ~ 25v)
(By Rton= 56K ohm)

+5VALWP Ipeak=9.26A ; Imax=6.5A
Delta I=3.483A=>1/2Delta I=1.742A
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)
OCP =11.11A

TDC:4.9A Fsw:321KHz
H-MOS PD:0.4173W Δ T:13.4°C
L-MOS PD:0.3442W Δ T:10°C
Choke PD:1.9613W Δ T:30°C
OVP margin for Vos:9% @ 330uF cap, 8% @ 220uF

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

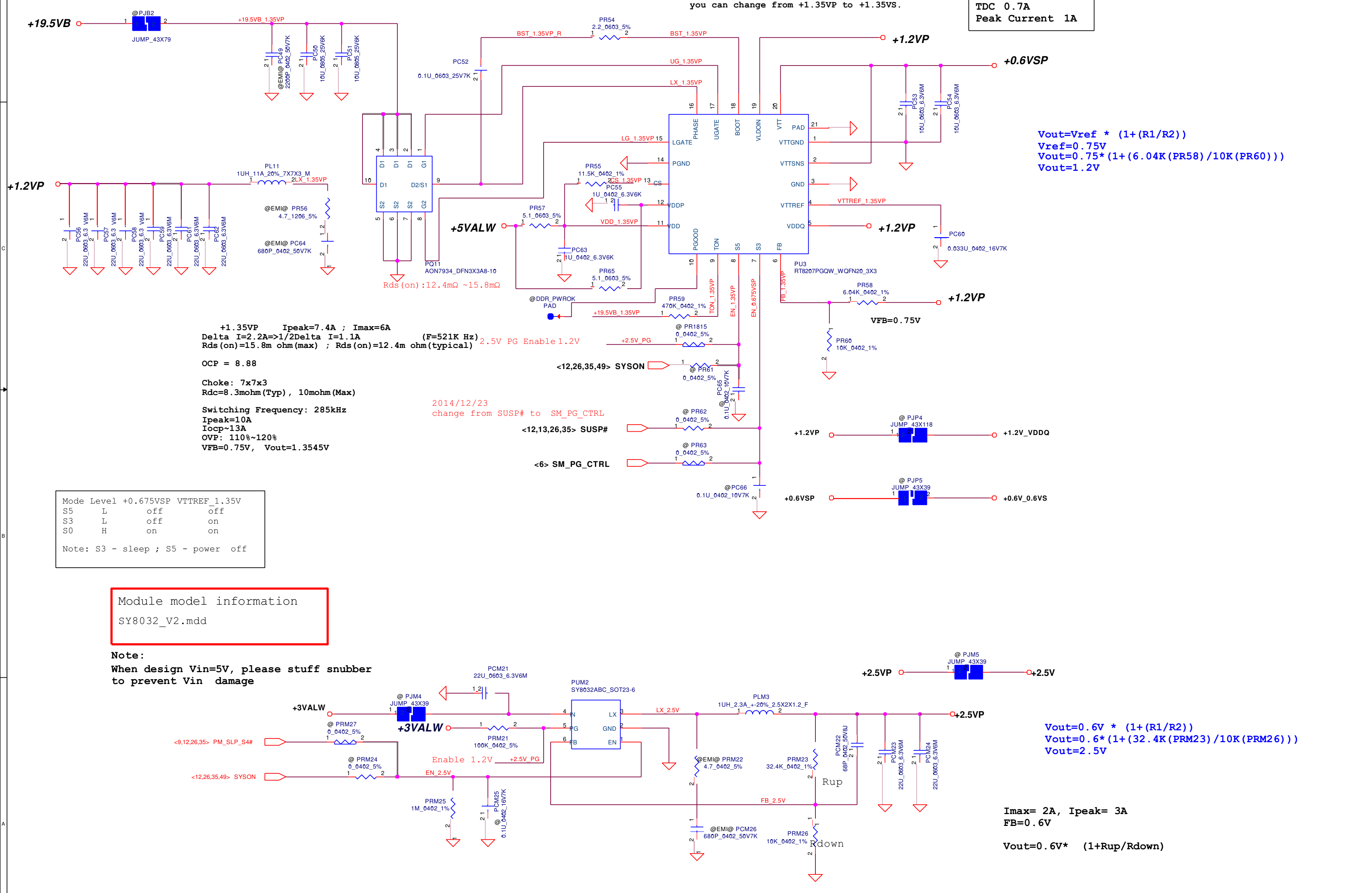
Compal Electronics, Inc.
Title: 3VALW/5VALW
Size: Custom; Document Number: LA-D707P; Rev: v0.2

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Vout=Vref * (1+(R1/R2))
Vref=0.75V
Vout=0.75*(1+(6.04K(PR58)/10K(PR60)))
Vout=1.2V

+1.35VP Ipeak=7.4A ; Imax=6A
Delta I=2.2A=>1/2Delta I=1.1A (F=521K Hz)
Rds(on)=15.8m ohm(max) ; Rds(on)=12.4m ohm(typical)

OCP = 8.88

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information

SY8032_V2.mdd

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V * (1+(R1/R2))
Vout=0.6*(1+(32.4K(PRM23)/10K(PRM26)))
Vout=2.5V

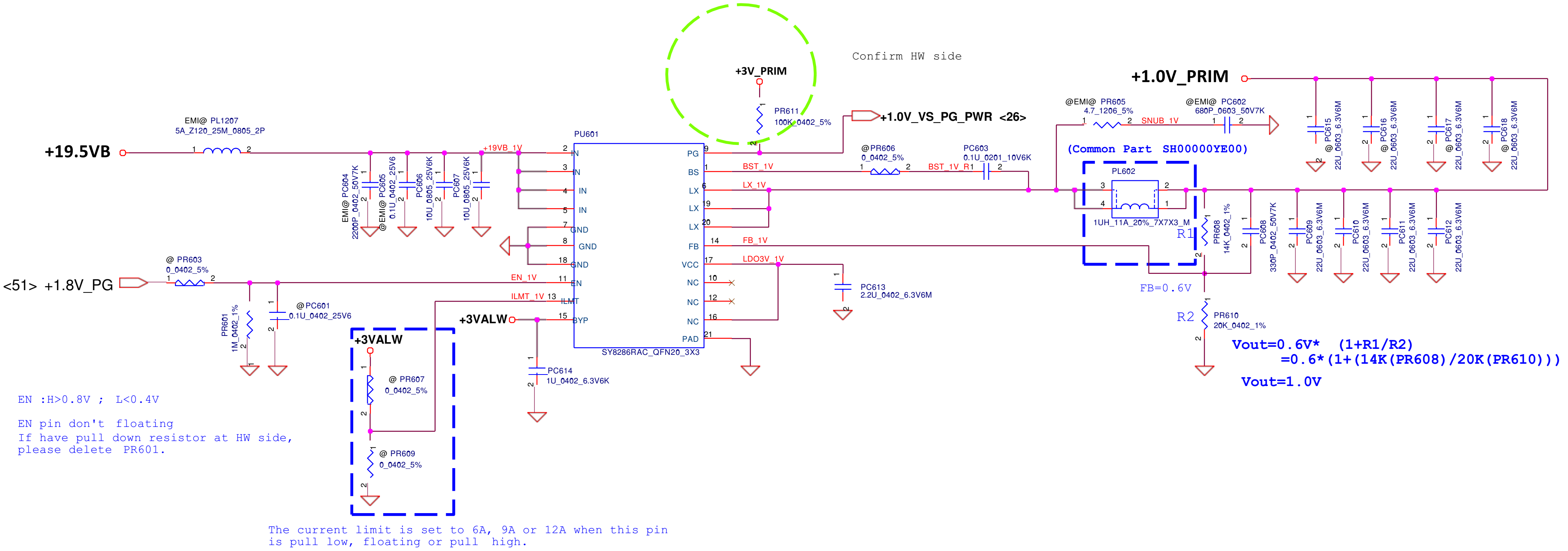
Imax= 2A, Ipeak= 3A
FB=0.6V

Vout=0.6V* (1+Rup/Rdown)

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5VP(RT8207P/SY8032A)

Size: Custom | Document Number | Rev: v0.2



Security Classification	Compal Secret Data			Title
Issued Date	2015/10/09	Deciphered Date	2018/10/09	1.0VS(SY8286)
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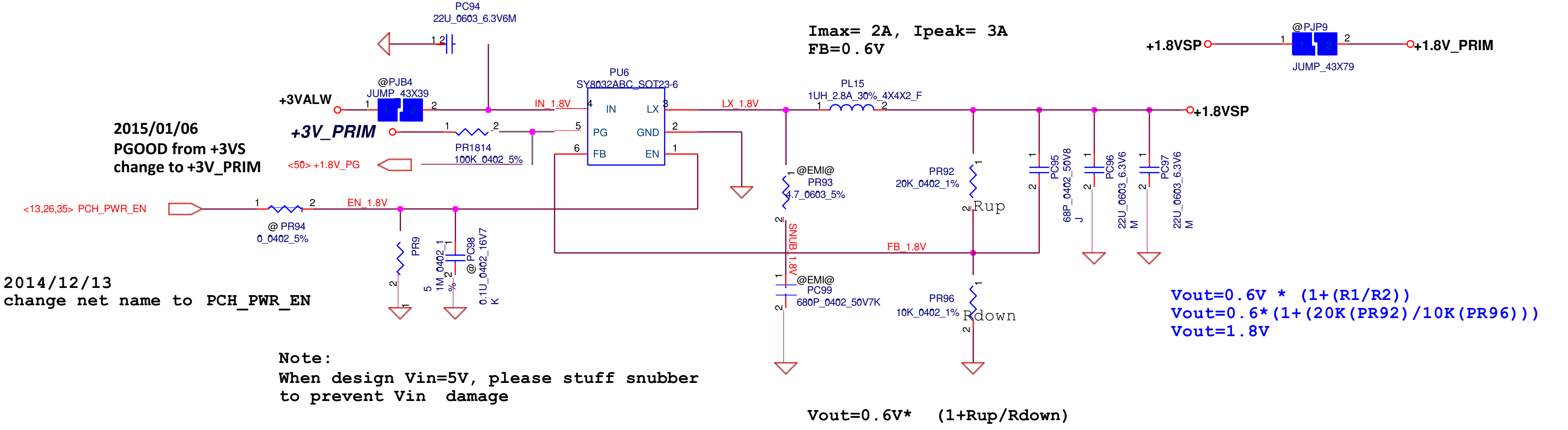
				Date: Wednesday, May 11, 2016; Sheet 50 of 60



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/09	Deciphered Date	2018/10/09	Title: 1.8VS(SY8032A)

Size	Document Number	Rev
B	LA-D707P	v0.2

Date: Sheet 51 of 60

PR1101=2*PR1106/(10*IOUTmax*Load line) RIccMAX2ph(PR1104)= (IccMAX2Ph+32)*200kohm/ 127
U22 Iout@GT=31A U22 IccMAX@GT=31A
PR1101=25.5kohm PR1104= 100K

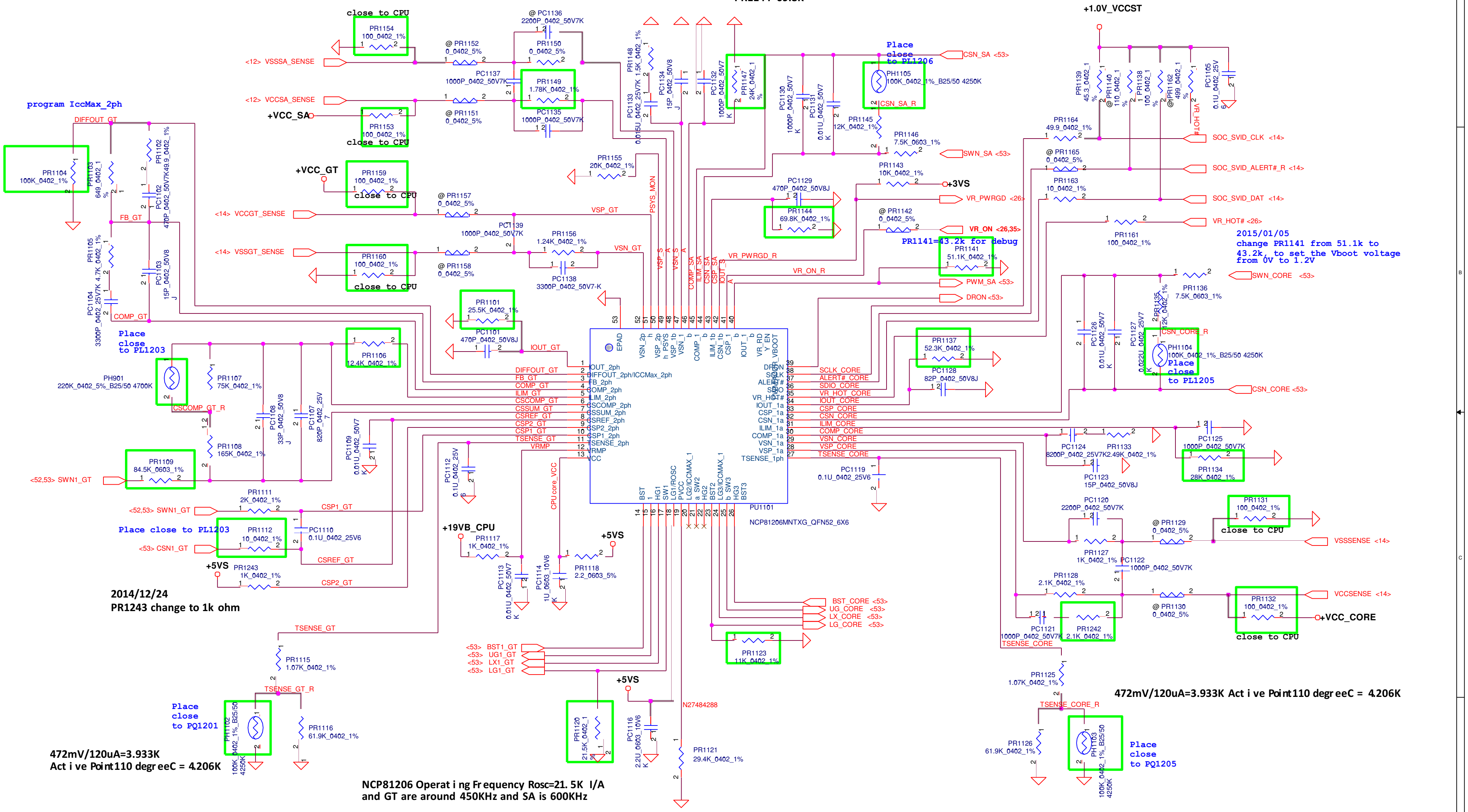
PR1106=Iout limit*Load line/10
U22 OCP@GT=40A
PR1106=12.4kohm

Load line=(PR1108+(PR1107+PH901/(PR1107*PH901)))*Iout tltal*DCR/PR1109
U22 Load line@GT= 3.1m
PR1109 ,PR1110@GT=84.5K

RDRPSP(PR1149)= Load line*(PR1146+PH1105+PR1145)/(gm * DCR) /(PH1105+PR1145)
Load line@SA= 10.3m
gm=1mS
PR1149=1.78K

RLIMSP(PR1147)= 1.3V/(gm*(PH1105+PR1145)*IoutLIMIT*DCR/(PR1146+PH1105+PR1145))
OCP@SA= 9.6A
gm=1mS
PR1147=24K

RIOUTSP(PR1144)= 2V/(gm*(PH1105+PR1145)*ICCMAX*DCR/(PR1146+PH1105+PR1145))
IOUTSP@SA= 5A
gm=1mS
PR1144=69.8K



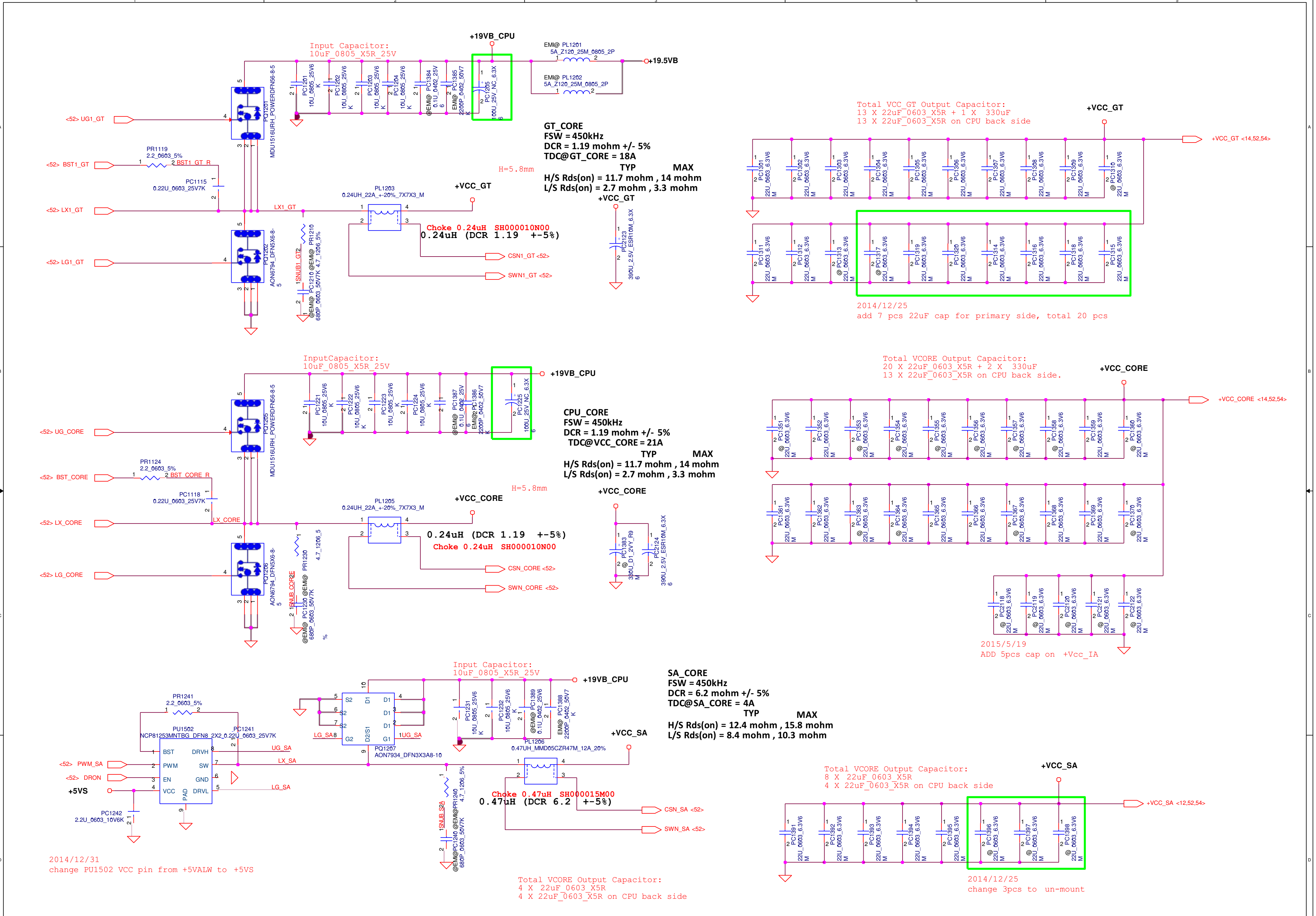
IccMAX@SA= 5A
PR1123= 11K
Refer IccMAX table in datasheet

IccMAX@VCORE= 28A
RIccMAX@VCORE= 24.9K
Refer IccMAX table in datasheet

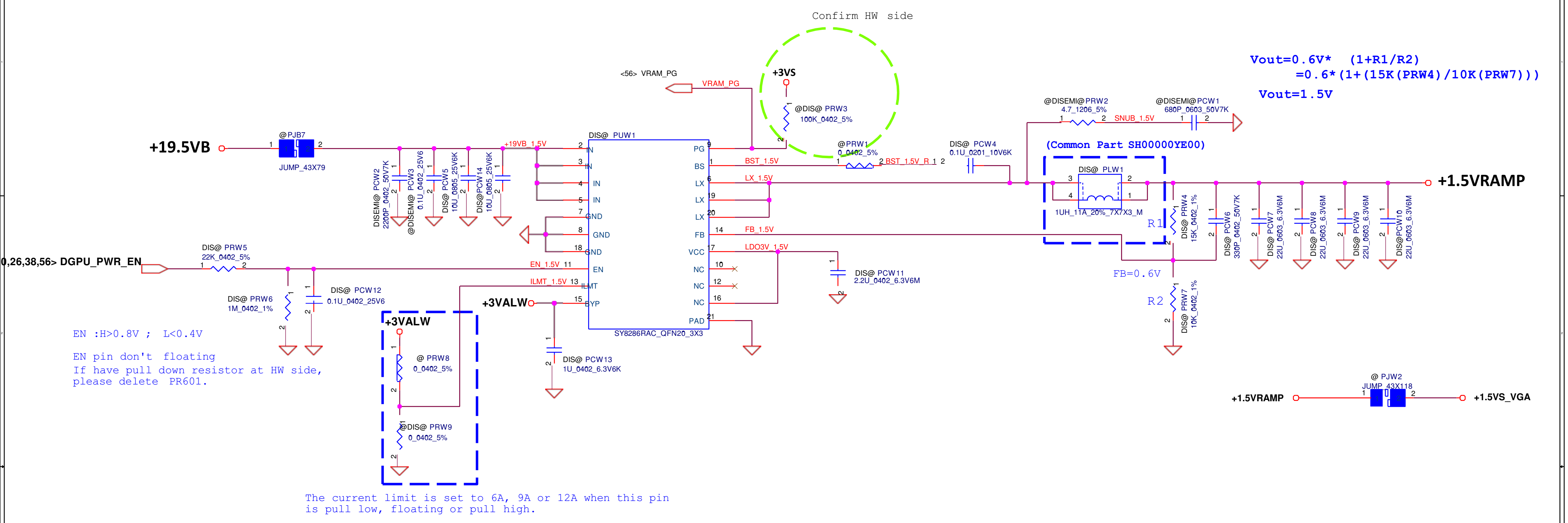
RDRPSP(PR1128)= Load line*(PR1136+PH1104+PR1135)/(gm * DCR) /(PH1104+PR1135)
Load line@VCORE= 2.1m
gm=1mS
PR1128=2.1K

RIOUTSP(PR1137)= 2V/(gm*(PH1104+PR1135)*ICCMAX*DCR/(PR1136+PH1104+PR1135))
IOUTSP@VCORE= 28A
gm=1mS
PR1137=64.9K

RLIMSP(PR1134)= 1.3V/(gm*(PH1104+PR1135)*IoutLIMIT*DCR/(PR1136+PH1104+PR1135))
OCP@VCORE= 35A
gm=1mS
PR1134=33.2K



Title	VCC_CORE_PowerStage	
Size	Document Number	Rev v0.2
Date: Wednesday, May 11, 2016	Sheet 53 of 60	



Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

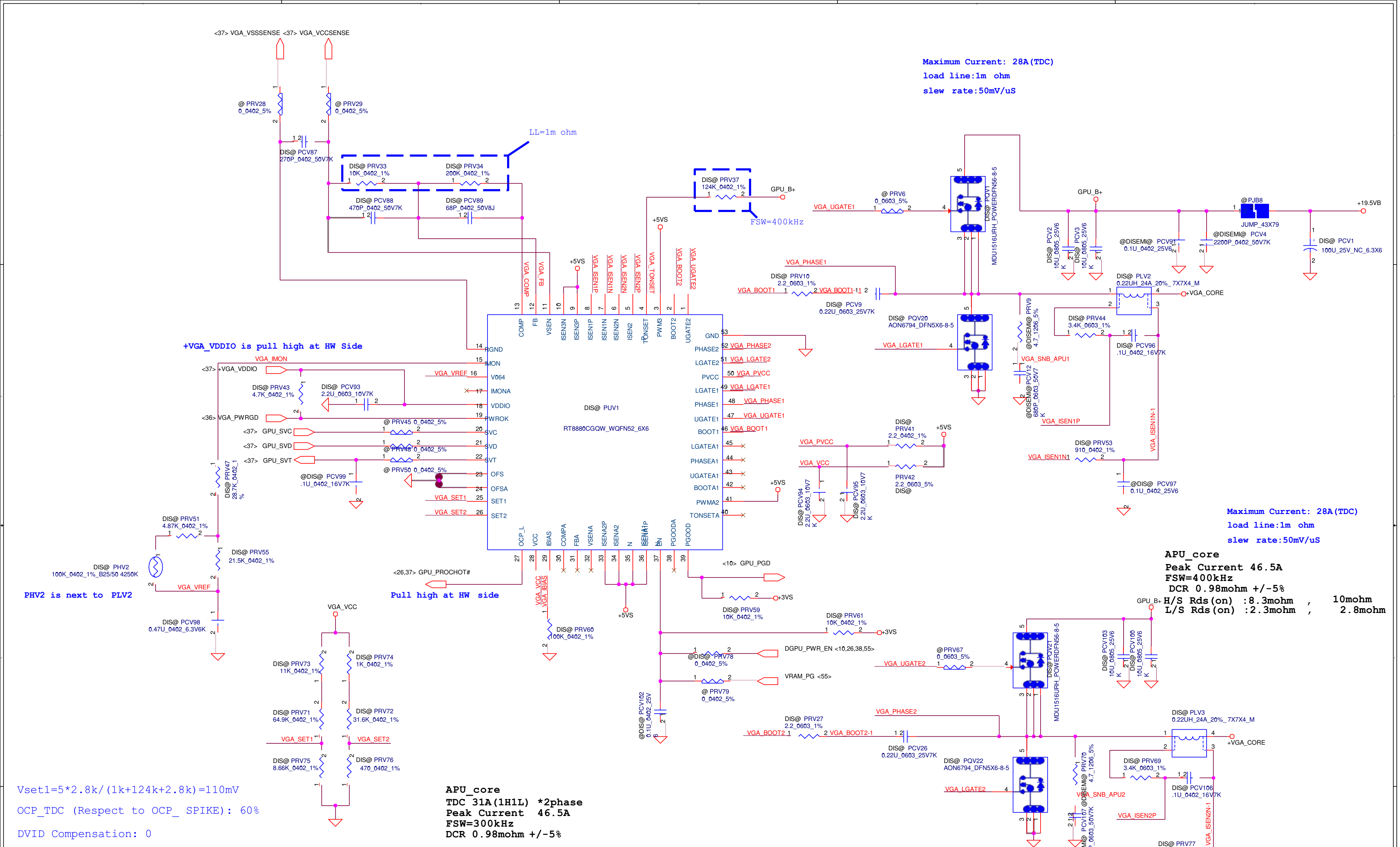
Compal Electronics, Inc.

Title: 1.5VS_VGA(SY8286)

Size Document Number: LA-D707P

Rev: v0.2

Date: Wednesday, May 11, 2016



Vset1=5*2.8k/(1k+124k+2.8k)=110mV

OCP_TDC (Respect to OCP_ SPIKE): 60%

DVID Compensation: 0

RSET:100%

DVID Boost Compensation:22.5mV

Vset2=5*470/(1K+31.6k+470)=71mV

QRTH (for VDD) :Disable

DVID Compensation : 0

NB OLL Setting :0

OCPTRGDELAY (for VDD/VDDNB) : 40ms

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Issued Date	2015/10/09	Deciphered Date 2018/10/09	Title: VGA_CORE(RT8880A)
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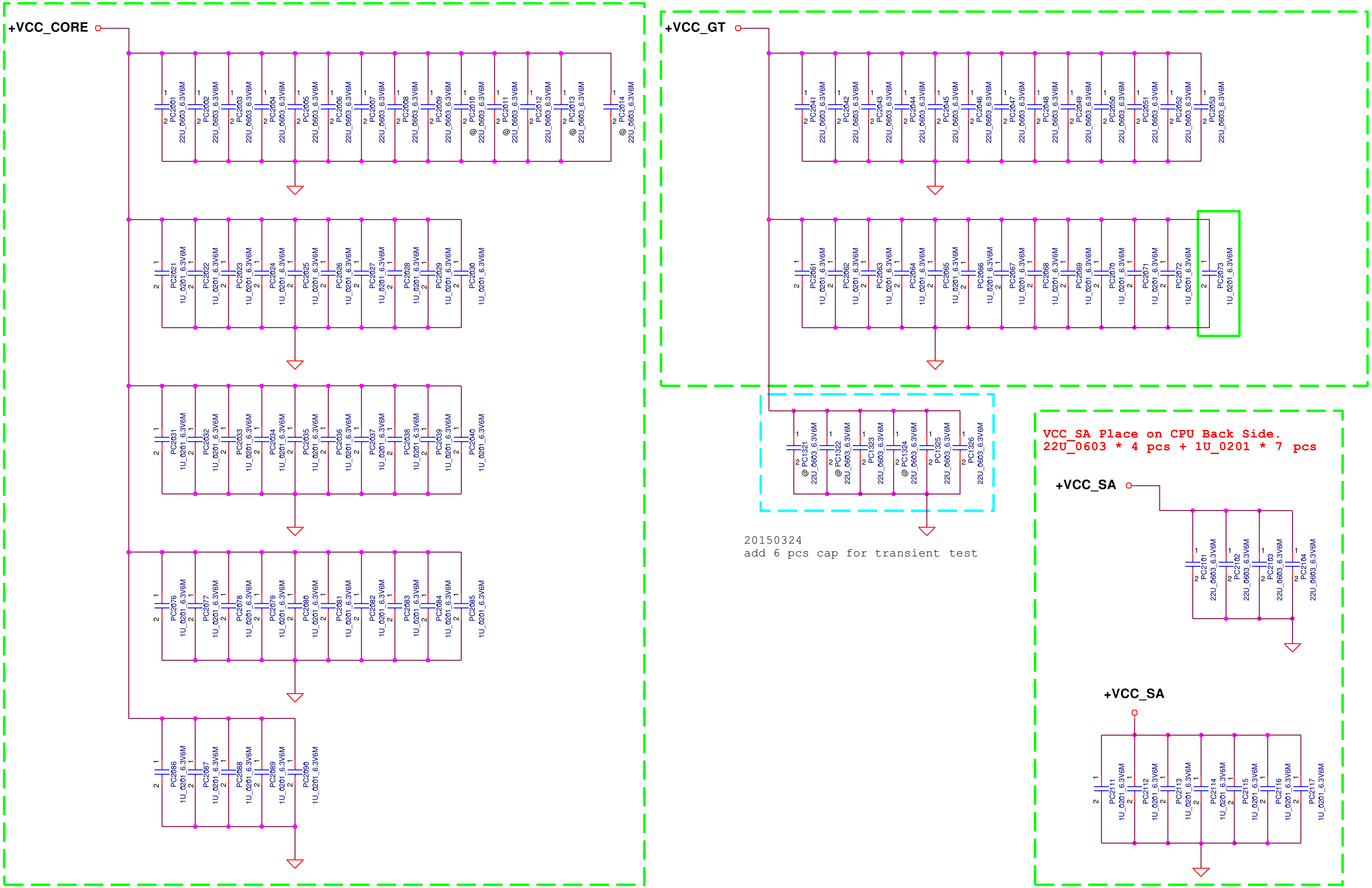
			Date: Wednesday, May 11, 2016; Sheet 56 of 60

VCC_CORE Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*35 pcs

VCC_GT Place on CPU Back Side.
22U_0603 * 13 pcs + 1U_0201*12 pcs

2014/12/25
add 1 pcs 1uF cap for back side, total 13 pcs



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2015/10/09	Deciphered Date	2018/10/09	Title: VCC_CORE_PROCESSOR DECOUPLING
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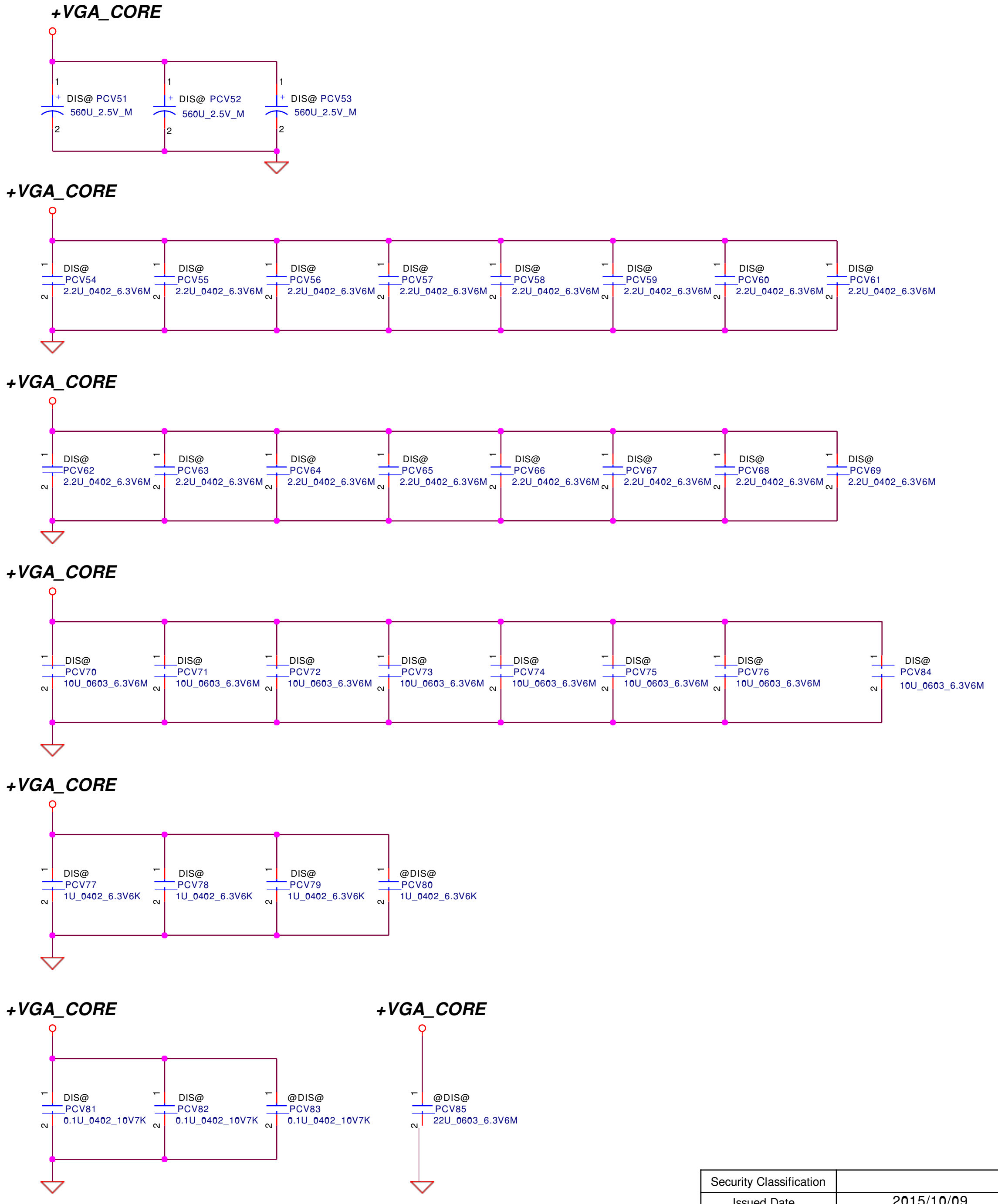
				Date: Wednesday, May 11, 2016; Sheet 54 of 60

Item	Page	Title	Change Description	Date
1	50,55	Change 0 ohm to short pad	Change PR607,PRV28,PRV29 from 0 ohm to short pad PRW8 from unpop to pop , change PRW8 from 0 ohm to short pad	2016-2-19
2	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000S800 to SB00000JZ00(Change to Main source)	2016-2-19
3	54	Add IA_Core Output capacitor	Add IA_Core Output capacitor 0603 22uF(PC2014) for IccMAX=32A	2016-2-24

Item	Page	Title	Change Description	Date
1	47	ADP_I resistance	Change PR223 from short pad to 0 ohm	2016-4-28
2	52	ICCmax from 29A to 32A	Change PR1121 from 20.5K to 29.4K Change PR1137 from 61.9K to 52.3K Change PR1134 from 33.2K to 28K	2016-4-28
3	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800(Change to 2nd source)	2016-4-28
4	49	Add 2nd source	Change PU3 from RT8207P (SA00007IH00) to G5616B (SA00008PH00)	2016-4-28
5	48	Add 2nd source	Change PU2 from RT8243A(SA00005VH00) to UP1590PQKF(SA00007DS00)	2016-4-28

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	Change Value	11/06	Power	(Set VR prochot# from 110C to 120C)	Change PR1115 and PR1125 Value 0 ohm to 1.07K ohm	
2	50	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PL602 part number from SH00000Z200 to SH00000YE00	
3	55	Change part number	11/06	Power	Change from 5x5 choke to 7x7 follow Candy design	Change PLW1 part number from SH00000Z200 to SH00000YE00	
4	48	Add Jump	11/18	Power	For easy debug	+3VL and +VL add Jump	
5	55	Add Net	11/18	EE	For VGA CORE sequence and VID error issue	Delete PG pin test point VRAM_PG Add Net VRAM_PG	
6	56	pop to unpop unpop to pop	11/18	EE	For VGA CORE sequence and VID error issue	PRV61 from unpop to pop PRV78 and PCV102 from pop to unpop	
7	56	Add Net and R	11/18	EE	For VGA CORE sequence and VID error issue	Add Net VRAM_PG Add PRV79	
8	47	Change jump to ISN choke	11/24	EMI	EMI ISN issue	Delete jump PJB9 Add ISN choke PL201	
9	48	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL7	
10	49	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL10	
11	50	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB3 Add Bead PL1207	
12	53	Change jump to Bead	11/24	EMI	EMI power noise issue	Delete jump PJB5 Add Bead PL1201 PL1202	
13	55	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1208	
14	56	colay bead	11/24	EMI	EMI power noise issue	Add Bead footprint PL1209 and PL1210	
15	55	Change R Value Change C unpop to pop	11/24	EE	HW f i net une VRA Mpo wersequence	Change PRW5 value from 0 ohm to 22K ohm Change PCW12 from unpop to pop (VGA sequence)	
16	53	Change Common part	11/6	Power	(Change to Common part)	Change PC1331 PC1383 PC1390 from SGA20331E10 to SGA00009S00	

Item	Page	Title	Change Description	Date
1	56	Modify VGA_CORE OCP	1.Change PRV73 Value 1K ohm to 11K ohm 2.Change PRV71 Value 124K ohm to 64.9K ohm 3.Change PRV75 Value 2.8K ohm to 8.66K ohm	2015-12-12
2	47	space saving	Change PC221 0603 to 0402 size	2015-12-12
3	47,49, 50,51, 52,56	Change 0 ohm to short pad	Change PR63,PR94,PR215,PR603,PR1129,PR1130,PR1142,PR1151,PR1152,PR1157,PR1158,PR1165,PR1815,PRM27,PRV45,PRV48,PRV50,PRV79,PRV6,PRV67 from 0 ohm to short pad	2016-1-4
4	48,49, 55,56	Delete Jump or Bead(Co-lay)	Delete Co-Lay Bead PL7,PL10,PL1208,PL1209,PL1210	2016-1-7
5	53	Delete VCC_GT,VCC_CORE Co-Lay caps	Delete Location PC1331 Footprint,PC2123 from unpop to pop Delete Location PC1390 Footprint,PC2124 from unpop to pop	2015-12-12
6	53,56	High Low Side MOS Matrix request	Change PQ1201,PQ1205,PQV1,PQV21 from SB00000JZ00 to SB00000S800	2015-12-12
7	52,53, 54	CPU transient request	Change PC1353,PC1363,PC1355,PC1356,PC1357,PC1354,PC1364,PC1358,PC1351,PC1370,PC1360,PC2010,PC2013,PC2011,PC1367 from pop to unpop Change PC1107 from 1000P to 820P PC1108 from 390P to 33P,PC1108 from unpop to pop PC1104 from 2200P to 3300P PR1103 from 1K to 649	2015-12-12
8	50	1V OVP issue (HW Low switch second source issue)	Delete jump PJ601 and add output MLCC PC615,PC616,PC617,PC618 PR607 from unpop to pop	2016-1-7



560u X 3
2.2u X 16
10u X 8
1u X 3
0.1u X 2

Security Classification	Compal Secret Data		
Issued Date	2015/10/09	Deciphered Date	2018/10/09

Compal Electronics, Inc.

Title: *VGA_CORE_CHIP DECOUPLING*

Size	Document Number	Rev
	LA-D707P	v0.2

Date: Wednesday, May 11, 2016 Sheet 57 of 60

BOM control

Plat f or m	Silego P/N	Compal PN	25MHz(A)	32.768KHz	24MHz(B)	27MHz	8MHz	Remark
Intel ULT UMA	SLG3NB3455VTR	SA00008IQ00	1	1	1	X	X	GCLKUMA@
Intel ULT Dis	SLG3NB3456VTR	SA00008J800	1	1	1	1	X	GCLKPX@

Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.