AMD AM4

MICRO-STAR INT'L CO.,LTD

MS-7B78

Size: Custom | Document Description: Cover Sheet | Rev: 11

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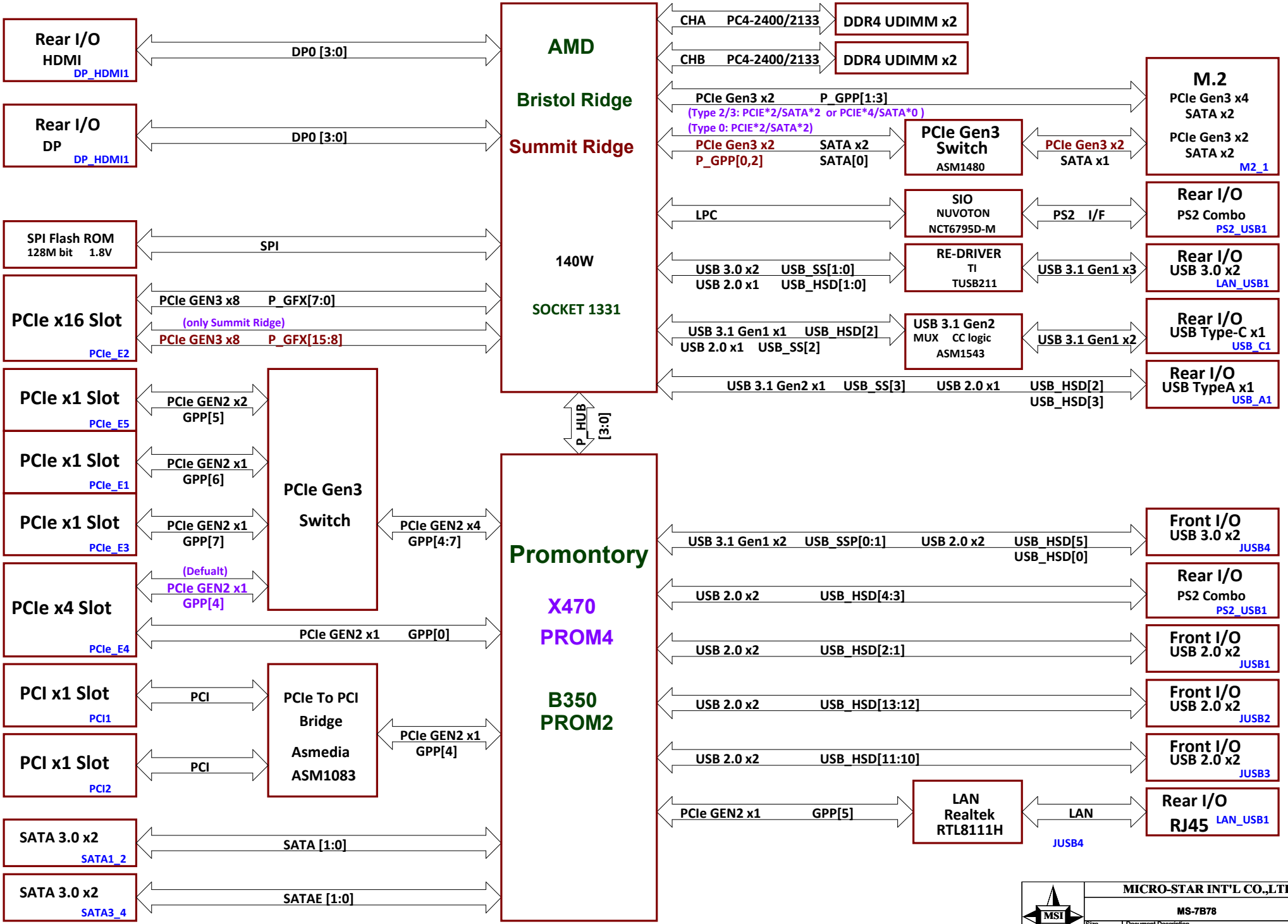

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Block Diagram	11

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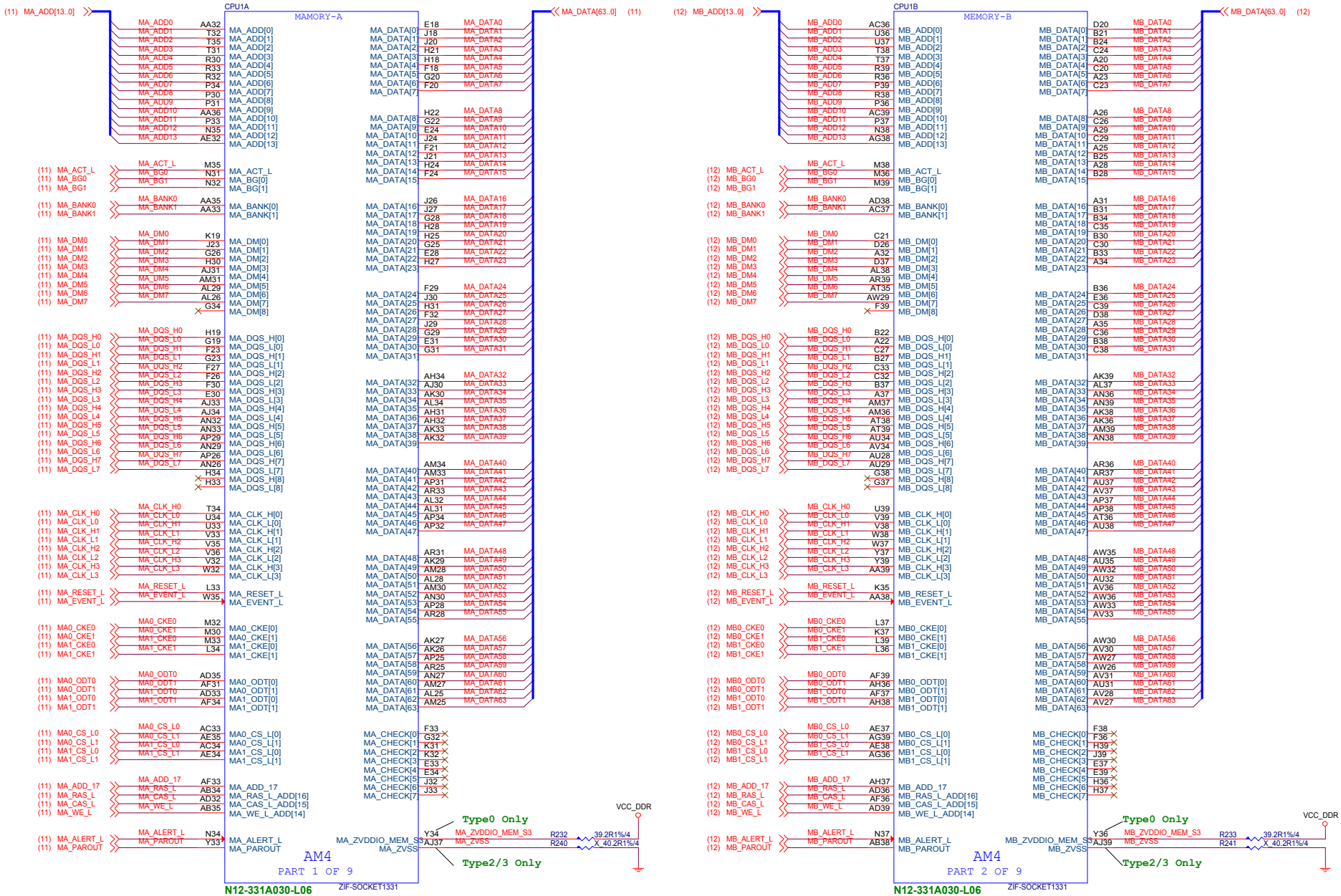

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	AM4 DDR4 I/F	11

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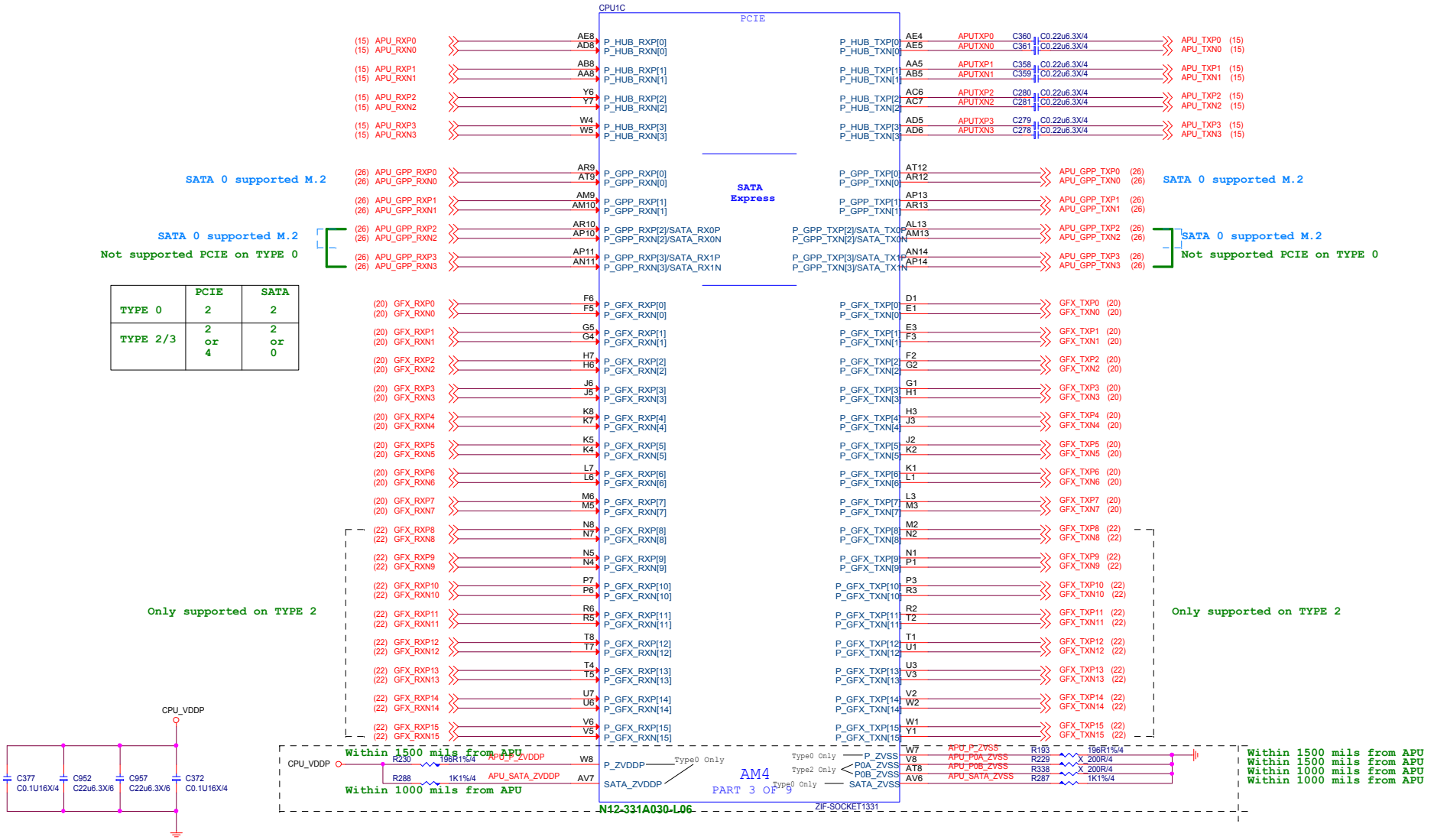

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

MICRO-STAR INT'L CO.,LTD	
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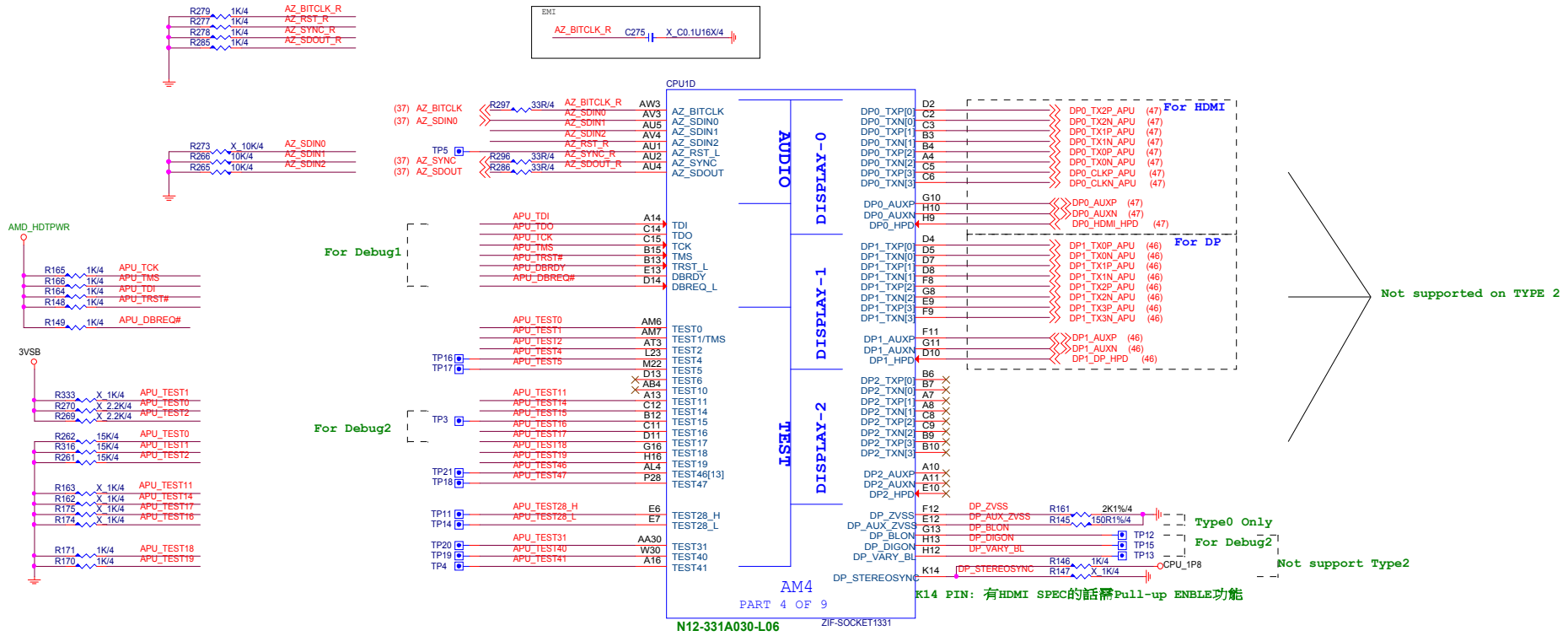
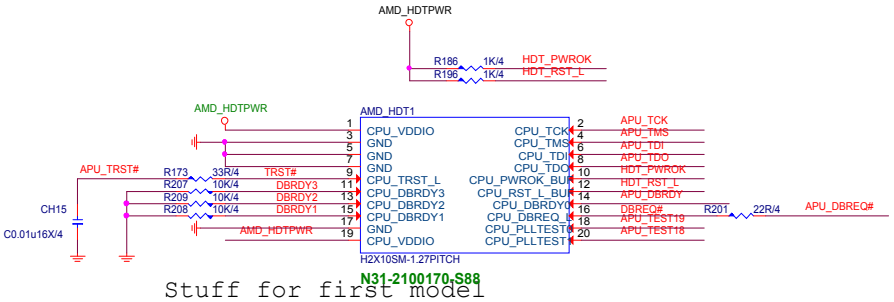
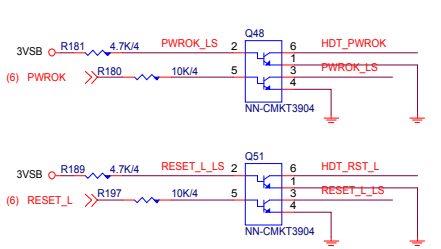






IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA

IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA

B*Ib>Ic=10*0.181=1.81>0.16

IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA

IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA

B*Ib>Ic=10*0.08=0.8>0.16

IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA

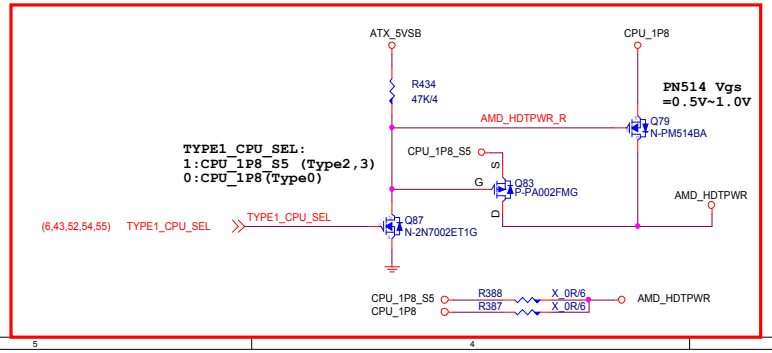
IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA

B*Ib>Ic=10*0.181=1.81>0.16

IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA

IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA

B*Ib>Ic=10*0.08=0.8>0.16



MICRO-STAR INT'L CO.,LTD	
MS-7B78	
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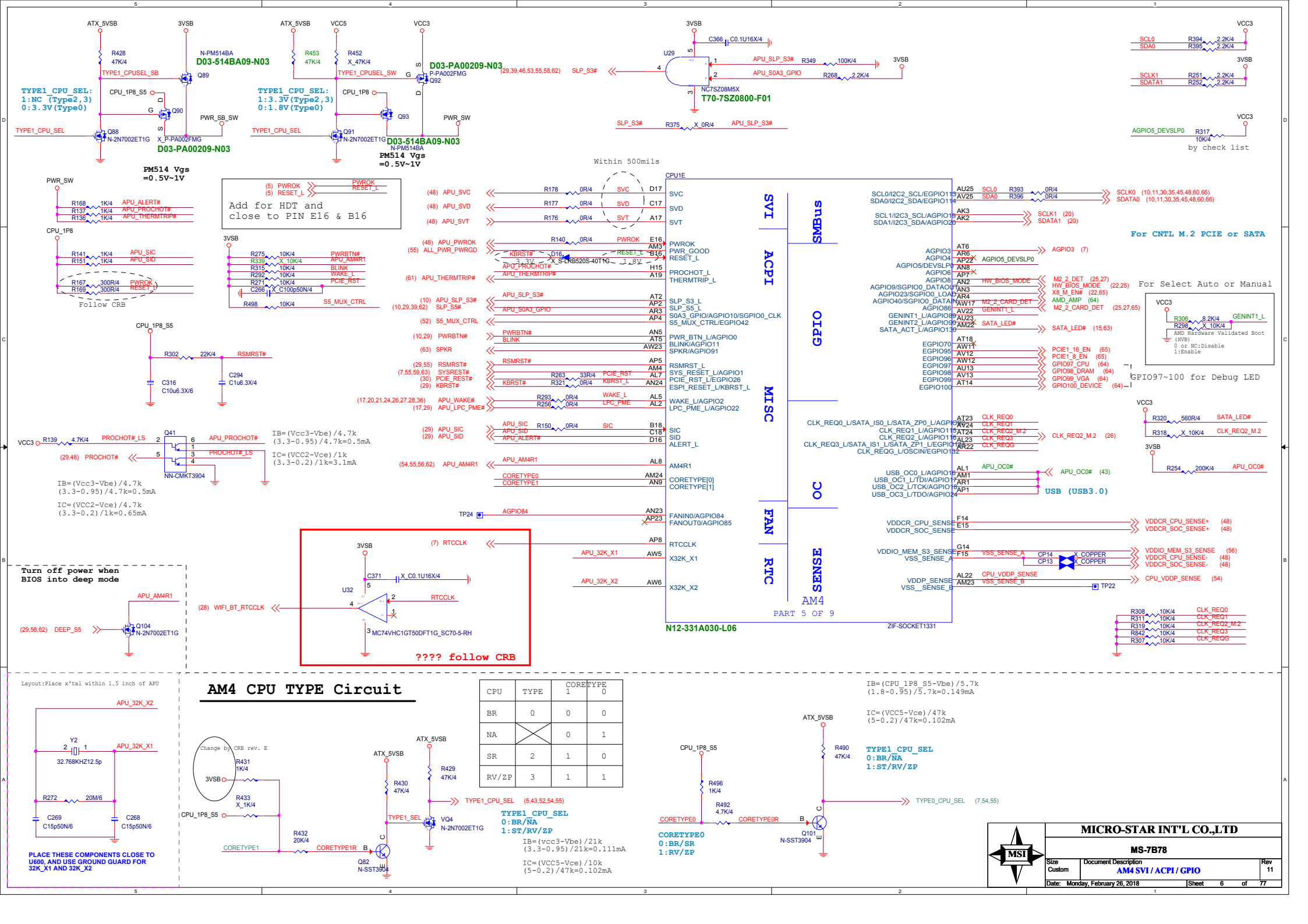
ATX_5VSB
3VSB
R428
47K/4
N-PM514BA
D03-514BA09-N03
Q89
TYPE1_CPUSEL_SB
TYPE1_CPU_SEL:
1:NC (Type2,3)
0:3.3V(Type0)
CPU_1P8_S5
Q90
PWR_SB_SW
TYPE1_CPU_SEL
Q88
N-2N7002ET1G
X_P-PA002FMG
D03-PA00209-N03
PM514 Vgs
=0.5V~1V
VCC5
VCC3
R453
47K/4
R452
X_47K/4
TYPE1_CPUSEL_SW
D03-PA00209-N03
P-PA002FMG
Q92
(29,39,46,53,55,58,62)
SLP_S3#
TYPE1_CPU_SEL:
1:3.3V(Type2,3)
0:1.8V(Type0)
CPU_1P8
Q93
PWR_SW
Q91
N-2N7002ET1G
D03-514BA09-N03
N-PM514BA
PM514 Vgs
=0.5V~1V
U29
C366
C0.1U16X/4
APU_SLP_S3#
R349
100K/4
APU_S0A3_GPIO
R268
2.2K/4
NC7SZ08M5X
T70-7SZ0800-F01
R375
X_0R/4
APU_SLP_S3#
SCL0
SDA0
R394
R395
2.2K/4
SCLK1
SDATA1
R251
R252
AGPIO5_DEVSLP0
R317
10K/4
by check list
PWR_SW
R168
R137
R136
1K/4
APU_ALERT#
APU_PROCHOT#
APU_THERMTRIP#
CPU_1P8
R141
R151
APU_SIC
APU_SID
R167
R169
300R/4
PWROK
RESET_L
Follow CRB
Add for HDT and
close to PIN E16 & B16
(5) PWROK
(5) RESET_L
3VSB
R275
R339
R315
R292
R271
R498
10K/4
X_10K/4
PWRBTN#
APU_AM4R1
BLINK
WAKE_L
PCIE_RST
C266
X_C100p50N/4
S5_MUX_CTRL
CPU_1P8_S5
R302
22K/4
RSMRST#
C316
C10u6.3X/6
C294
C1u6.3X/4
Within 500mils
CPU1E
(48) APU_SVC
(48) APU_SVD
(48) APU_SVT
R178
R177
R176
0R/4
SVC
SVD
SVT
D17
C17
A17
(48) APU_PWROK
(55) ALL_PWR_PWRGD
R140
PWROK
KBRST#
D16
S-LRB520S-40TG
APU_PROCHOT#
(61) APU_THERMTRIP#
APU_THERMTRIP#
E16
AM3
B16
H15
A19
PWROK
PWR_GOOD
RESET_L
PROCHOT_L
THERMTRIP_L
(10) APU_SLP_S3#
(10,29,39,62) SLP_S5#
APU_SLP_S3#
APU_S0A3_GPIO
AT2
AP2
AR3
AP4
SLP_S3_L
SLP_S5_L
S0A3_GPIO/AGPIO10/SGPIO0_CLK
S5_MUX_CTRL/EGPIO42
(52) S5_MUX_CTRL
(10,29) PWRBTN#
(63) SPKR
PWRBTN#
BLINK
AN5
AT5
AW23
PWR_BTN_L/AGPIO0
BLINK/AGPIO11
SPKR/AGPIO91
(29,55) RSMRST#
(7,55,59,63) SYSRESET#
(30) PCIE_REST#
(29) KBRST#
RSMRST#
KBRST#
R263
R321
33R/4
PCIE_RST
KBRST_L
AP5
AM4
AL7
AN24
RSMRST_L
SYS_RESET_L/AGPIO1
PCIE_RST_L/EGPIO26
ESPI_RESET_L/KBRST_L
(17,20,21,24,26,27,28,36) APU_WAKE#
(17,29) APU_LPC_PME#
R293
R256
WAKE_L
LPC_PME
AL5
AL2
WAKE_L/AGPIO2
LPC_PME_L/AGPIO22
(29) APU_SIC
(29) APU_SID
APU_SIC
APU_SID
APU_ALERT#
R150
SIC
B18
C18
D16
SIC
SID
ALERT_L
APU_AM4R1
(54,55,56,62) APU_AM4R1
AL8
AM4R1
CORETYPE0
CORETYPE1
AM24
AN9
CORETYPE[0]
CORETYPE[1]
TP24
AGPIO84
AN23
AP23
FANIN0/AGPIO84
FANOUT0/AGPIO85
(7) RTCCLK
APU_32K_X1
APU_32K_X2
AP8
AW5
AW6
RTCCLK
X32K_X1
X32K_X2
SVI
ACPI
GPIO
MISC
OC
FAN
RTC
SMBus
SENSE
AM4
PART 5 OF 9
N12-331A030-L06
ZIF-SOCKET1331
SCL0/I2C2_SCL/EGPIO115
SDA0/I2C2_SDA/EGPIO114
AU25
AV25
R393
R396
SCL0
SDA0
SCLK0 (10,11,30,35,45,48,60,66)
SDATA0 (10,11,30,35,45,48,60,66)
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20
AK3
AK2
SCLK1 (20)
SDATA1 (20)
For CNTL M.2 PCIE or SATA
AGPIO3
AGPIO4
AGPIO5/DEVSLP0
AGPIO6
AGPIO8
AGPIO9/SGPIO0_DATAOUT
AGPIO23/SGPIO0_LOAD
AGPIO40/SGPIO0_DATAIN
AGPIO86
GENINT1_L/AGPIO89
GENINT2_L/AGPIO90
SATA_ACT_L/AGPIO130
AT6
AR6
AP22
AN8
AP7
AN2
AN3
AR4
AW17
AV22
AU23
AM22
AGPIO5_DEVSLP0
HW_BIOS_MODE
M2_CARD_DET
GENINT1_L
SATA_LED#
AGPIO3 (7)
M2_2_DET (25,27)
HW_BIOS_MODE (22,25)
X8_M_EN# (22,65)
AMD_AMP (64)
M2_2_CARD_DET (25,27,65)
SATA_LED# (15,63)
For Select Auto or Manual
VCC3
R306
R298
8.2K/4
X_10K/4
GENINT1_L
AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable
EGPIO70
EGPIO95
EGPIO96
EGPIO97
EGPIO98
EGPIO99
EGPIO100
AT18
AW11
AV12
AW12
AU13
AV13
AT14
PCIE1_16_EN (65)
PCIE1_8_EN (65)
GPIO97_CPU (64)
GPIO98_DRAM (64)
GPIO99_VGA (64)
GPIO100_DEVICE (64)
GPIO97~100 for Debug LED
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO46
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO48
CLK_REQG_L/OSCIN/EGPIO152
AT23
AV24
AT24
AL23
AR22
CLK_REQ0
CLK_REQ1
CLK_REQ2_M.2
CLK_REQ3
CLK_REQG
CLK_REQ2_M.2 (26)
VCC3
R320
R318
560R/4
X_10K/4
SATA_LED#
CLK_REQ2_M.2
3VSB
R254
200K/4
APU_OC0#
USB_OC0_L/AGPIO10
USB_OC1_L/TDI/AGPIO17
USB_OC2_L/TCK/AGPIO18
USB_OC3_L/TDO/AGPIO24
AL1
AM1
AR1
AP1
APU_OC0#
APU_OC0# (43)
USB (USB3.0)
VDDCR_CPU_SENSE
VDDCR_SOC_SENSE
F14
E15
VDDCR_CPU_SENSE+ (48)
VDDCR_SOC_SENSE+ (48)
VDDIO_MEM_S3_SENSE
VSS_SENSE_A
G14
F15
CP14
CP13
X_COPPER
VDDIO_MEM_S3_SENSE (56)
VDDCR_CPU_SENSE- (48)
VDDCR_SOC_SENSE- (48)
VDDP_SENSE
VSS_SENSE_B
AL22
AM23
CPU_VDDP_SENSE
VSS_SENSE_B
CPU_VDDP_SENSE (54)
TP22
R308
R311
R319
R842
R307
10K/4
CLK_REQ0
CLK_REQ1
CLK_REQ2_M.2
CLK_REQ3
CLK_REQG
VCC3
R139
4.7K/4
PROCHOT#_LS
APU_PROCHOT#
(29,48) PROCHOT#
Q41
NN-CMKT3904
IB=(Vcc3-Vbe)/4.7k
(3.3-0.95)/4.7k=0.5mA
IC=(VCC2-Vce)/1k
(3.3-0.2)/1k=3.1mA
IB=(Vcc3-Vbe)/4.7k
(3.3-0.95)/4.7k=0.5mA
IC=(VCC2-Vce)/4.7k
(3.3-0.2)/1k=0.65mA
Turn off power when
BIOS into deep mode
APU_AM4R1
(29,58,62) DEEP_S5
Q104
N-2N7002ET1G
3VSB
C371
X_C0.1U16X/4
U32
RTCCLK
(28) WIFI_BT_RTCCLK
MC74VHC1GT50DFT1G_SC70-5-RH
???? follow CRB
Layout:Place x'tal within 1.5 inch of APU
APU_32K_X2
Y2
32.768KHZ12.5p
APU_32K_X1
R272
20M/6
C269
C15p50N/6
C268
C15p50N/6
PLACE THESE COMPONENTS CLOSE TO
U600, AND USE GROUND GUARD FOR
32K_X1 AND 32K_X2
AM4 CPU TYPE Circuit
Change by CRB rev. E
3VSB
R431
1K/4
R433
X_1K/4
CPU_1P8_S5
CORETYPE1
R432
20K/4
CORETYPE1R
Q82
N-SST3904
ATX_5VSB
R430
47K/4
TYPE1_SEL
VQ4
N-2N7002ET1G
R429
47K/4
TYPE1_CPU_SEL (5,43,52,54,55)
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
IB=(vcc3-Vbe)/21k
(3.3-0.95)/21k=0.111mA
IC=(VCC5-Vce)/10k
(5-0.2)/47k=0.102mA
CPU_1P8_S5
R496
1K/4
R492
4.7K/4
CORETYPE0
CORETYPE0R
Q101
N-SST3904
ATX_5VSB
R490
47K/4
TYPE0_CPU_SEL (7,54,55)
IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA
IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
CORETYPE0
0:BR/SR
1:RV/ZP
CPU TYPE TYPE CORETYPE 1 0
BR 0 0 0
NA X 0 1
SR 2 1 0
RV/ZP 3 1 1
MICRO-STAR INT'L CO.,LTD
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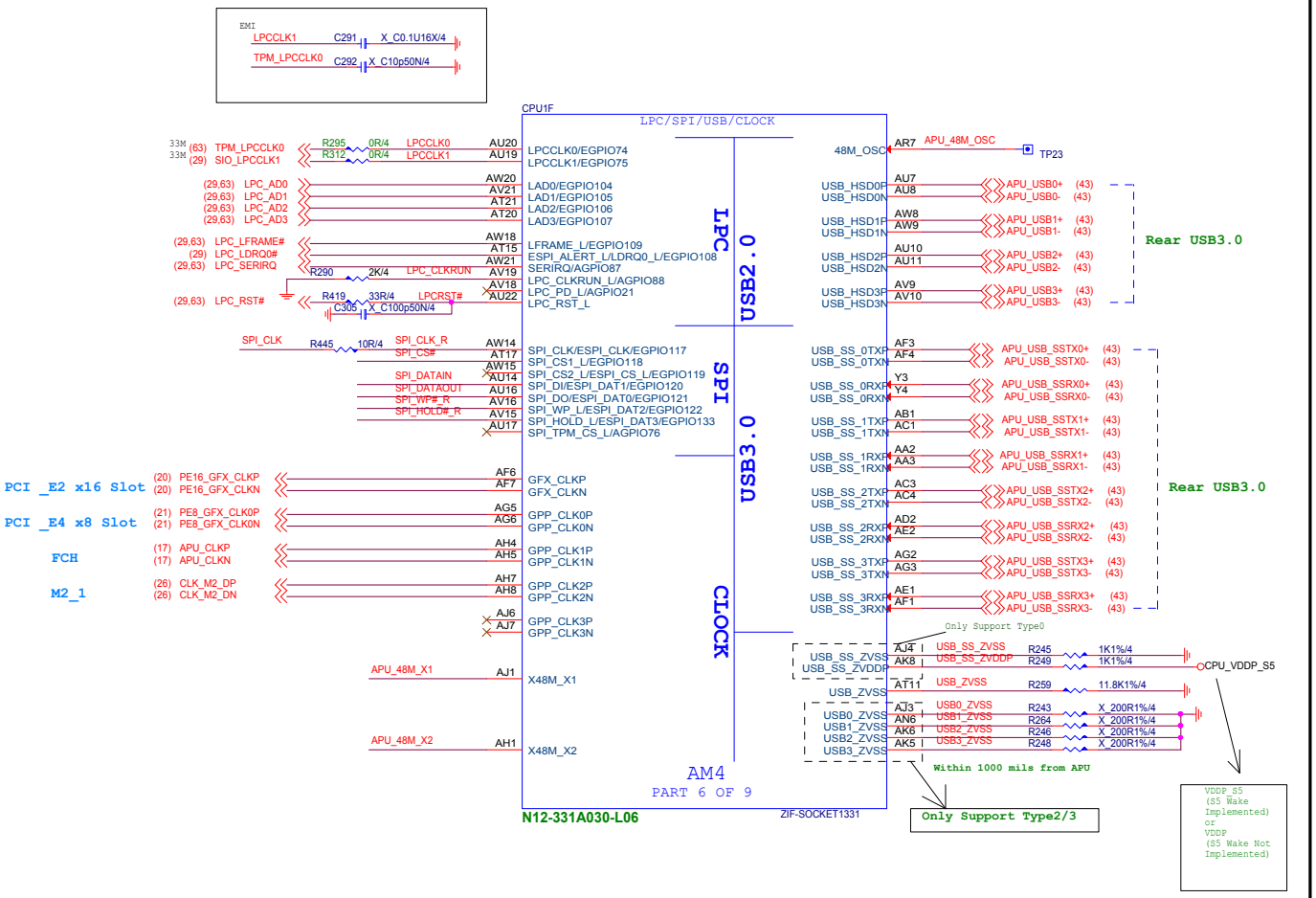
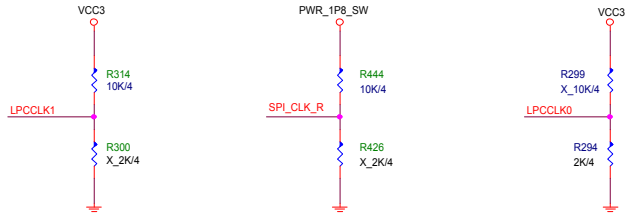
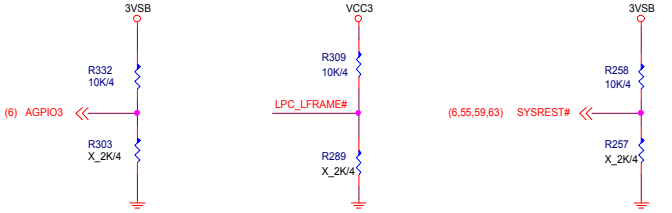


Strapping Options

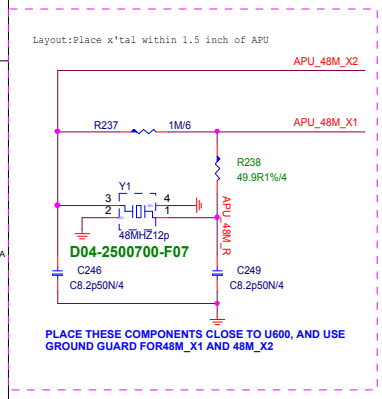


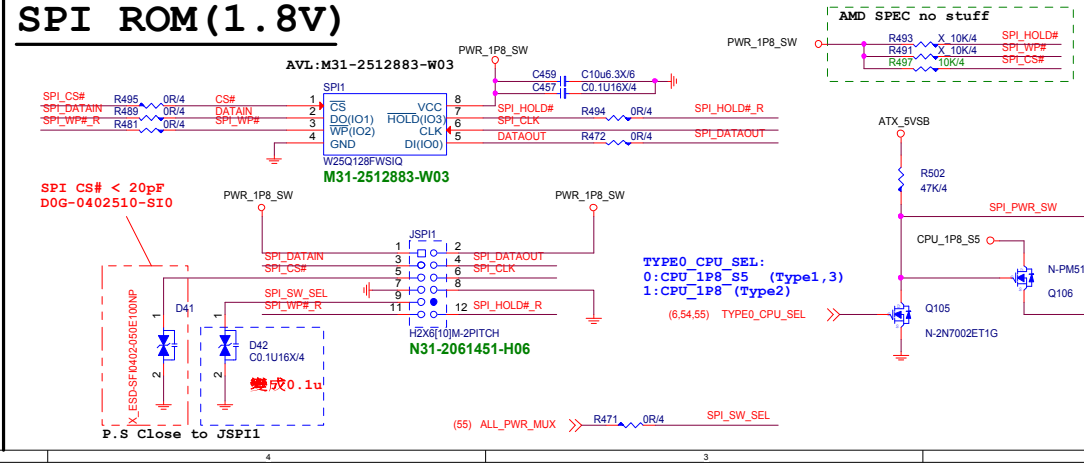
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled (Default)

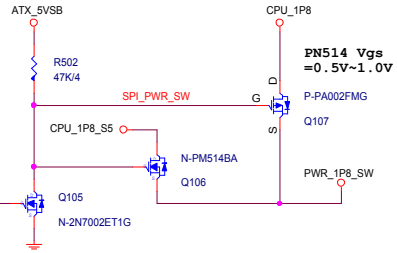


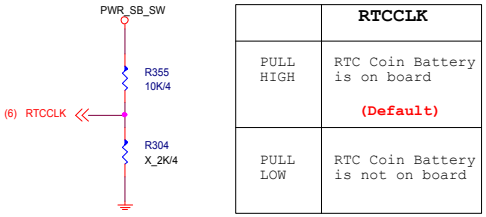
	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)









	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

MICRO-STAR INT'L CO.,LTD

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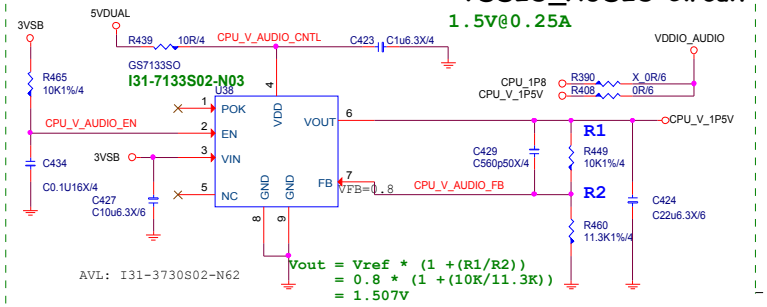
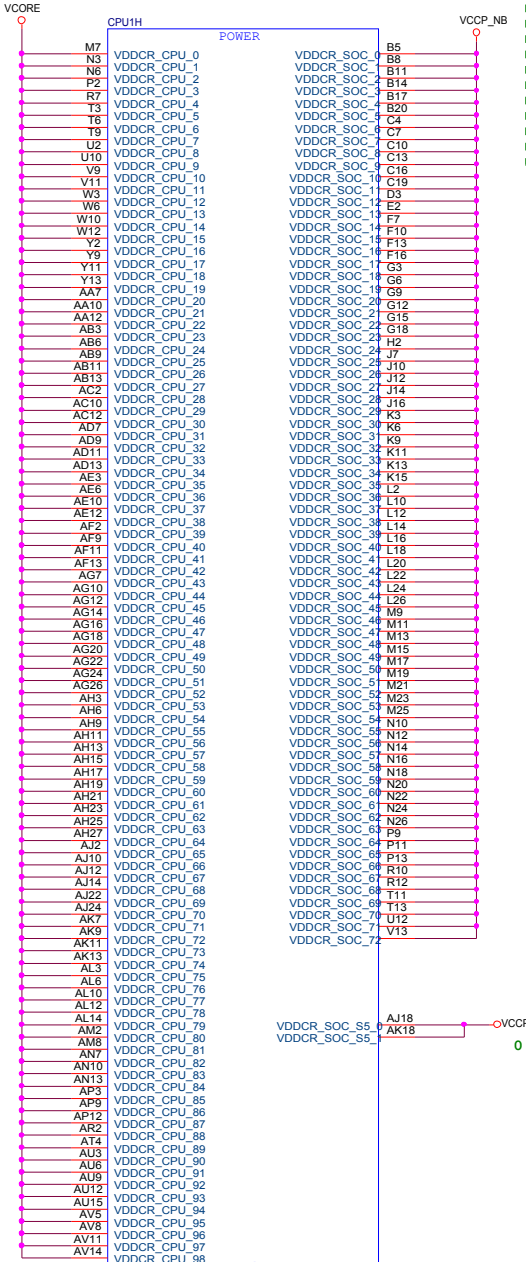
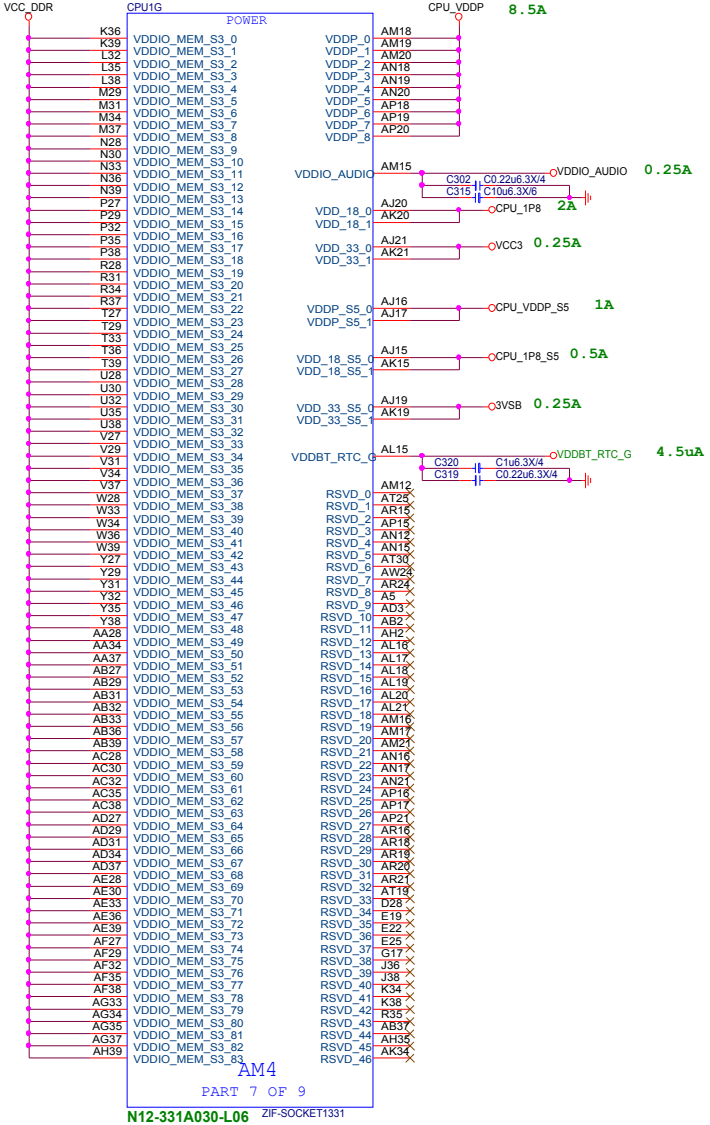
VDDIO_AUDIO Circuit

1.5V@0.25A





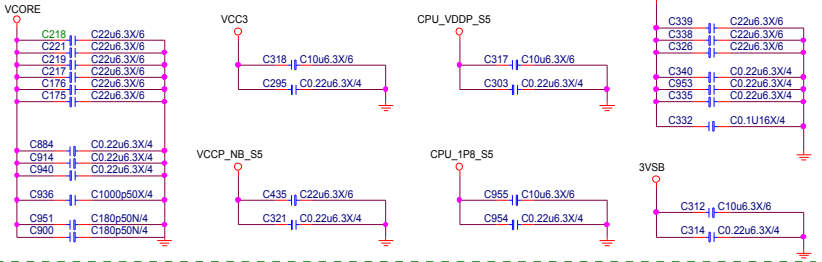
VDDCR_SOC_S5_0 / VDDCR_SOC_S5_1 — AJ18 / AK18 — VCCP_NB_S5 — 0.9A



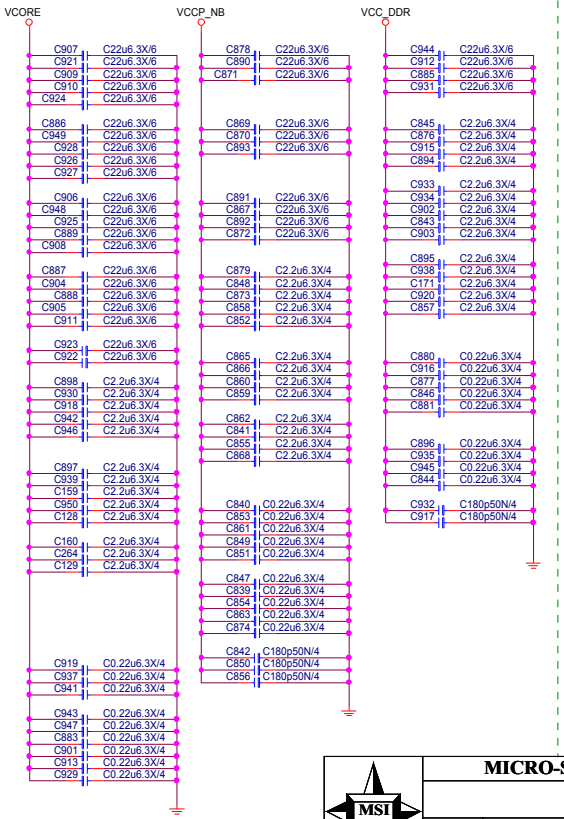
N12-331A030-L06

N12-331A030-L06

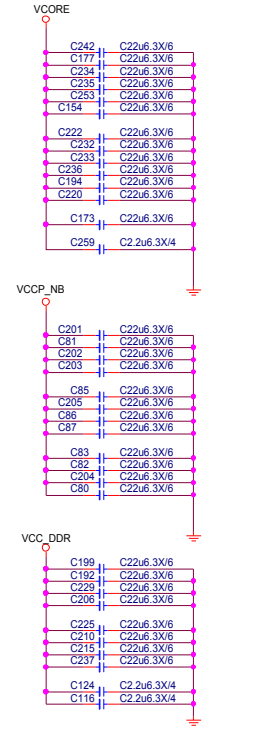
TOP SIDE



BOTTOM SIDE



TOP CAVITY



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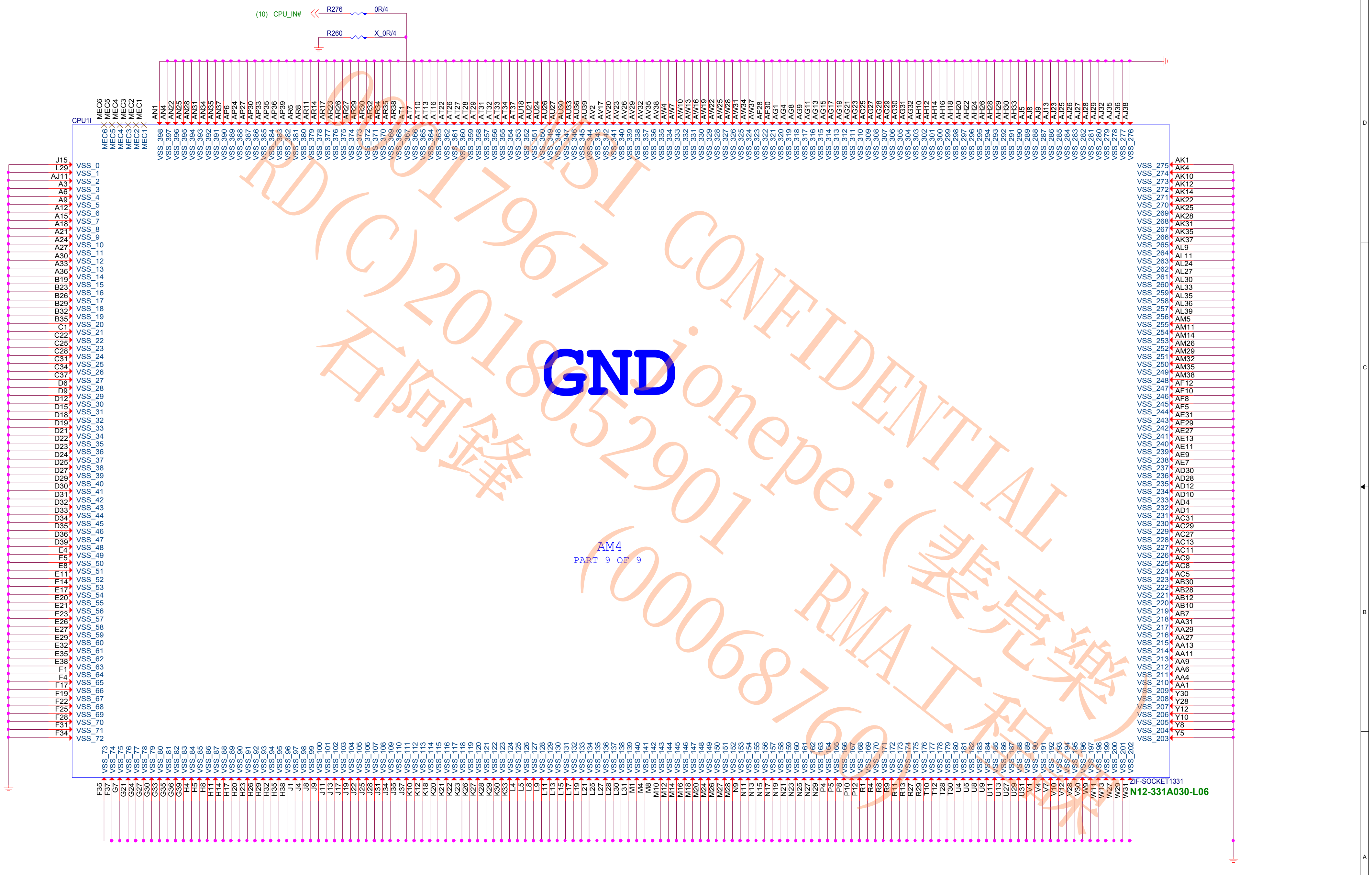

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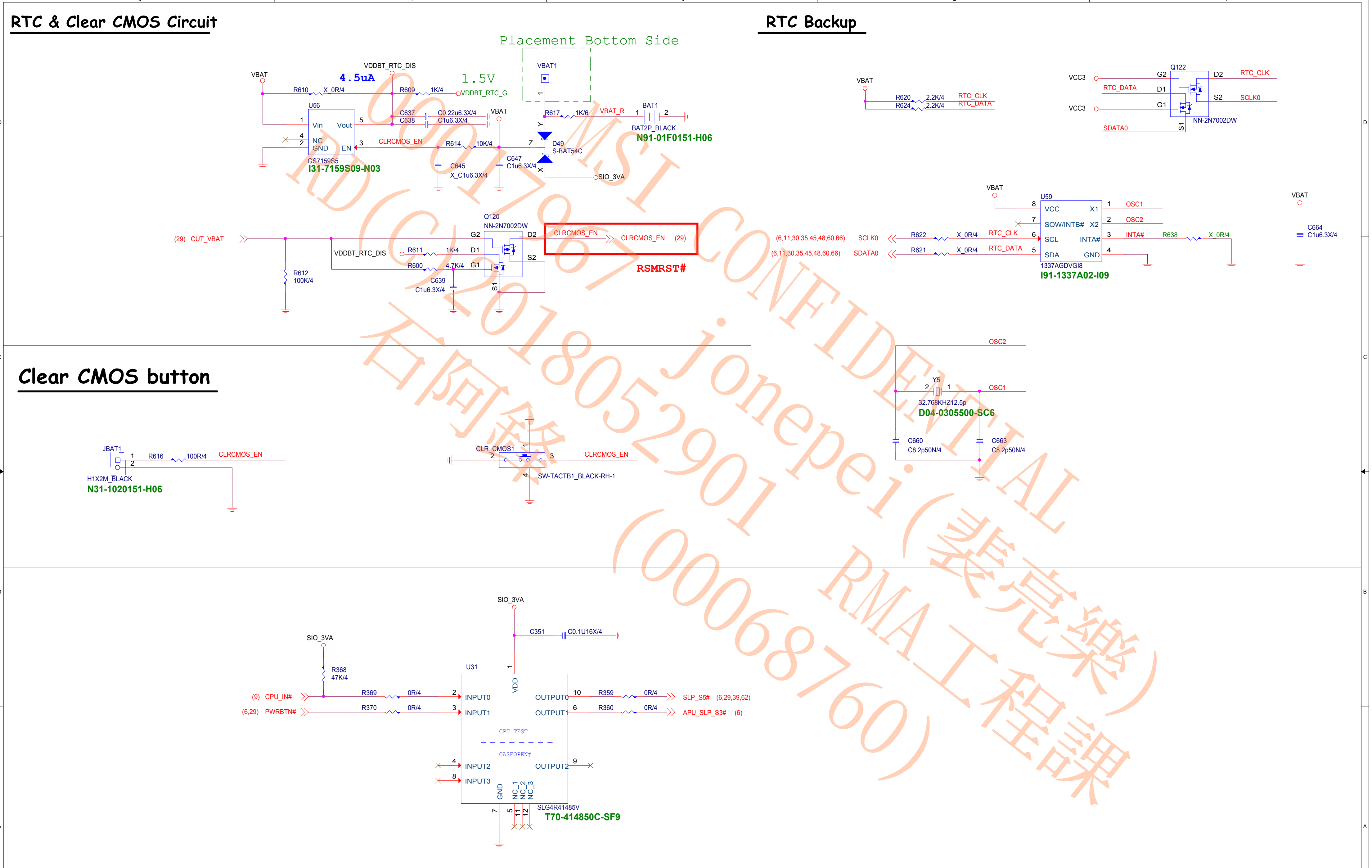
RTC & Clear CMOS Circuit

RTC Backup

Clear CMOS button



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Custom	RTC / CMOS	11

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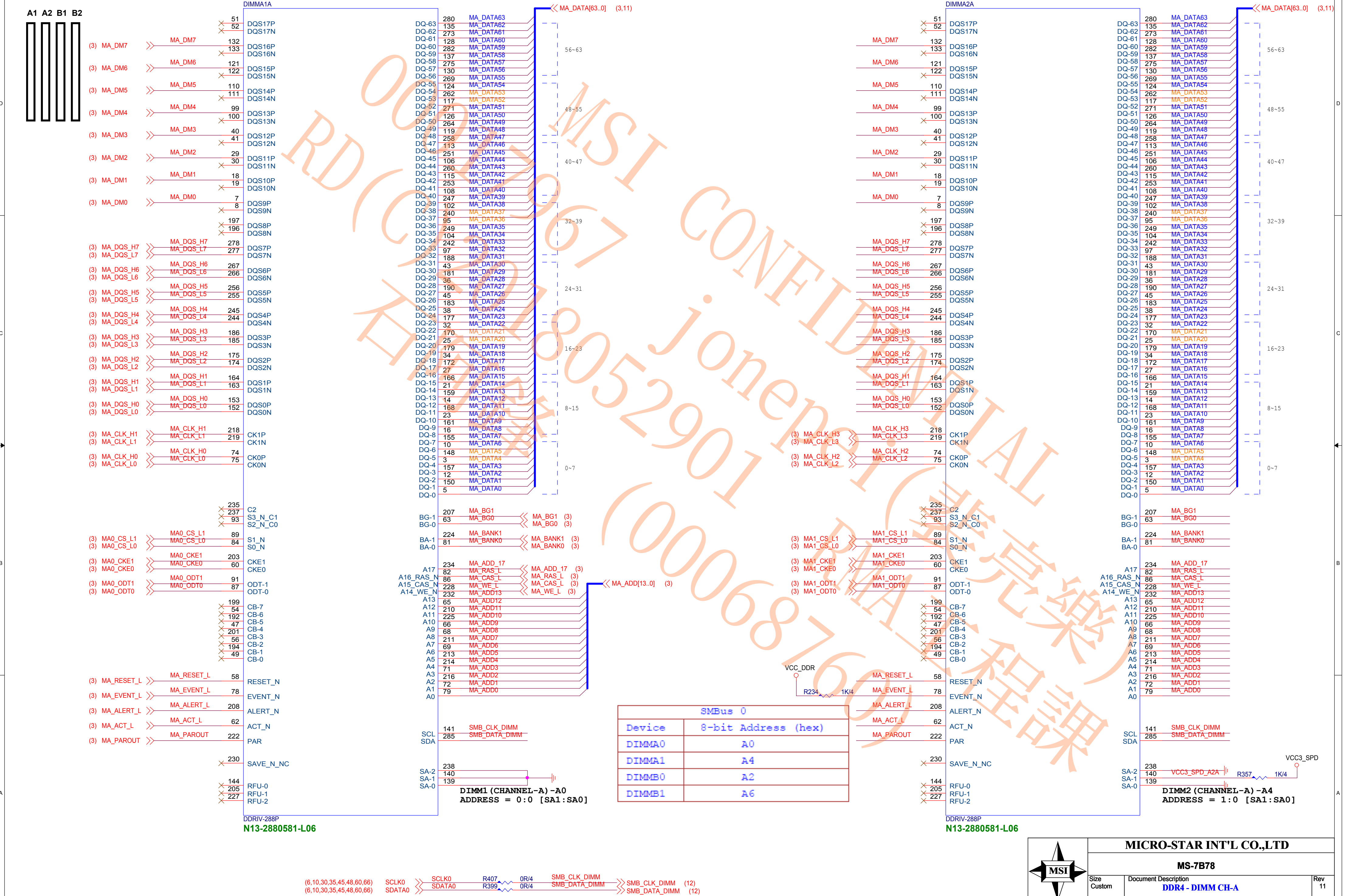

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

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Custom	DDR4 - DIMM CH-A	11

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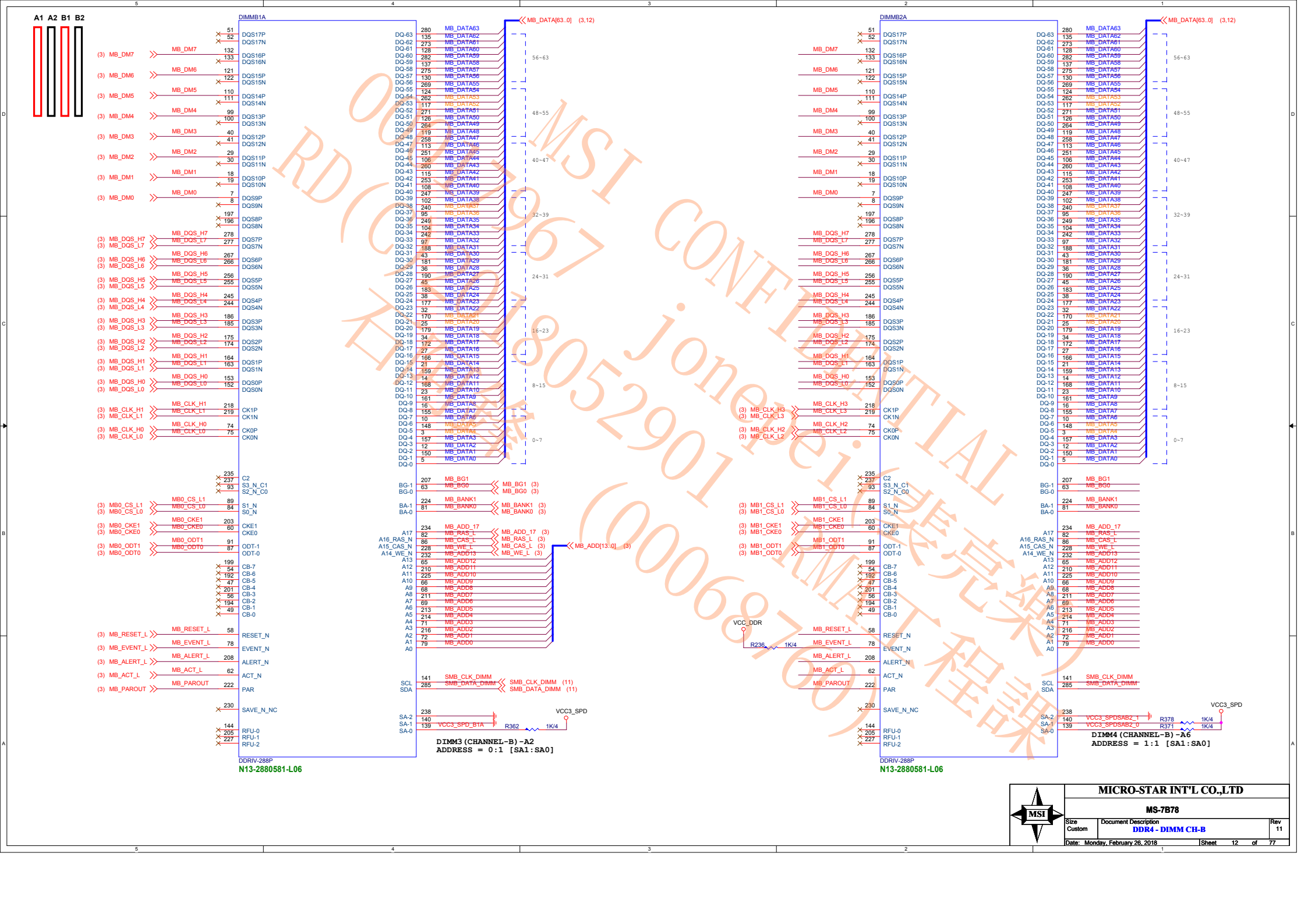
A1 A2 B1 B2
DIMMB1A
DIMMB2A
DDRIV-288P
N13-2880581-L06
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
MB_DATA[63..0] (3,12)
MB_ADD[13..0] (3)
VCC3_SPD
VCC_DDR
R362 1K/4
R236 1K/4
R378 1K/4
R371 1K/4
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avl:D08-0301100-B07

F6
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC

DIMMA1C
VCC_DDR
1 12V3_NC_1
145 12V3_NC_145
VCC3_SPD 284 VDDSPD
VPP25 142 143 286 287 288 VPP-1 VPP-2 VPP-3 VPP-4 VPP-5
VTT_DDR 77 221 VTT-1 VTT-2
DIMM_CA_VREF_A 146 VREFCA
MEC3 MEC2 MEC1 MEC3 MEC2 MEC1
VDD-0 236 233 231 229 226 223 220 217 215 212 209 206 204 92 90 88 85 83 80 76 73 70 67 64 61 59 VDD-25
DDRIV-288P
N13-2880581-L06

DIMMA2C
VCC_DDR
1 12V3_NC_1
145 12V3_NC_145
VCC3_SPD 284 VDDSPD
VPP25 142 143 286 287 288 VPP-1 VPP-2 VPP-3 VPP-4 VPP-5
VTT_DDR 77 221 VTT-1 VTT-2
DIMM_CA_VREF_A 146 VREFCA
MEC3 MEC2 MEC1 MEC3 MEC2 MEC1
VDD-0 236 233 231 229 226 223 220 217 215 212 209 206 204 92 90 88 85 83 80 76 73 70 67 64 61 59 VDD-25
DDRIV-288P
N13-2880581-L06

DDR VREF

(place resistors close to DIMMs)

DIMM_CA_VREF_A
C33 C0.1U16X/4
VCC_DDR

DIMM_CA_VREF_A
VCC_DDR
R62 1K1%/4
C31 C0.1U16X/4
C38 C1000p50X/4
C50 C0.1U16X/4
R70 1K1%/4

VCC3_SPD C380 C0.1U16X/4
DIMM_CA_VREF_A C60 C72 C2.2u6.3X/4 C0.1U16X/4
VTT_DDR C185 C0.1U16X/4
VPP25 C386 C388 C0.1U16X/4

VCC_DDR C158 C245 C145 C261 C167 C250 C256 C244 C1u6.3X/6 C0.1U16X/4

VCC3_SPD C373 C0.1U16X/4
DIMM_CA_VREF_A C71 C59 C2.2u6.3X/4 C0.1U16X/4
VTT_DDR C227 C0.1U16X/4
VPP25 C405 C418 C0.1U16X/4

VCC_DDR C144 C130 C131 C146 C1u6.3X/6
C165 C138 C157 C148 C0.1U16X/4

(65) DIMMA1_DET
D4 0.1u16X
DIMMA1B
VSS-93 VSS-92 VSS-91 VSS-90 VSS-89 VSS-88 VSS-87 VSS-86 VSS-85 VSS-84 VSS-83 VSS-82 VSS-81 VSS-80 VSS-79 VSS-78 VSS-77 VSS-76 VSS-75 VSS-74 VSS-73 VSS-72 VSS-71 VSS-70 VSS-69 VSS-68 VSS-67 VSS-66 VSS-65 VSS-64 VSS-63 VSS-62 VSS-61 VSS-60 VSS-59 VSS-58 VSS-57 VSS-56 VSS-55 VSS-54 VSS-53 VSS-52 VSS-51 VSS-50 VSS-49 VSS-48 VSS-47
VSS-46 VSS-45 VSS-44 VSS-43 VSS-42 VSS-41 VSS-40 VSS-39 VSS-38 VSS-37 VSS-36 VSS-35 VSS-34 VSS-33 VSS-32 VSS-31 VSS-30 VSS-29 VSS-28 VSS-27 VSS-26 VSS-25 VSS-24 VSS-23 VSS-22 VSS-21 VSS-20 VSS-19 VSS-18 VSS-17 VSS-16 VSS-15 VSS-14 VSS-13 VSS-12 VSS-11 VSS-10 VSS-9 VSS-8 VSS-7 VSS-6 VSS-5 VSS-4 VSS-3 VSS-2 VSS-1 VSS-0
DDRIV-288P
N13-2880581-L06

(65) DIMMA2_DET
D5 0.1u16X
DIMMA2B
VSS-93 VSS-92 VSS-91 VSS-90 VSS-89 VSS-88 VSS-87 VSS-86 VSS-85 VSS-84 VSS-83 VSS-82 VSS-81 VSS-80 VSS-79 VSS-78 VSS-77 VSS-76 VSS-75 VSS-74 VSS-73 VSS-72 VSS-71 VSS-70 VSS-69 VSS-68 VSS-67 VSS-66 VSS-65 VSS-64 VSS-63 VSS-62 VSS-61 VSS-60 VSS-59 VSS-58 VSS-57 VSS-56 VSS-55 VSS-54 VSS-53 VSS-52 VSS-51 VSS-50 VSS-49 VSS-48 VSS-47
VSS-46 VSS-45 VSS-44 VSS-43 VSS-42 VSS-41 VSS-40 VSS-39 VSS-38 VSS-37 VSS-36 VSS-35 VSS-34 VSS-33 VSS-32 VSS-31 VSS-30 VSS-29 VSS-28 VSS-27 VSS-26 VSS-25 VSS-24 VSS-23 VSS-22 VSS-21 VSS-20 VSS-19 VSS-18 VSS-17 VSS-16 VSS-15 VSS-14 VSS-13 VSS-12 VSS-11 VSS-10 VSS-9 VSS-8 VSS-7 VSS-6 VSS-5 VSS-4 VSS-3 VSS-2 VSS-1 VSS-0
DDRIV-288P
N13-2880581-L06

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DDR VREF

(place resistors close to DIMMs)

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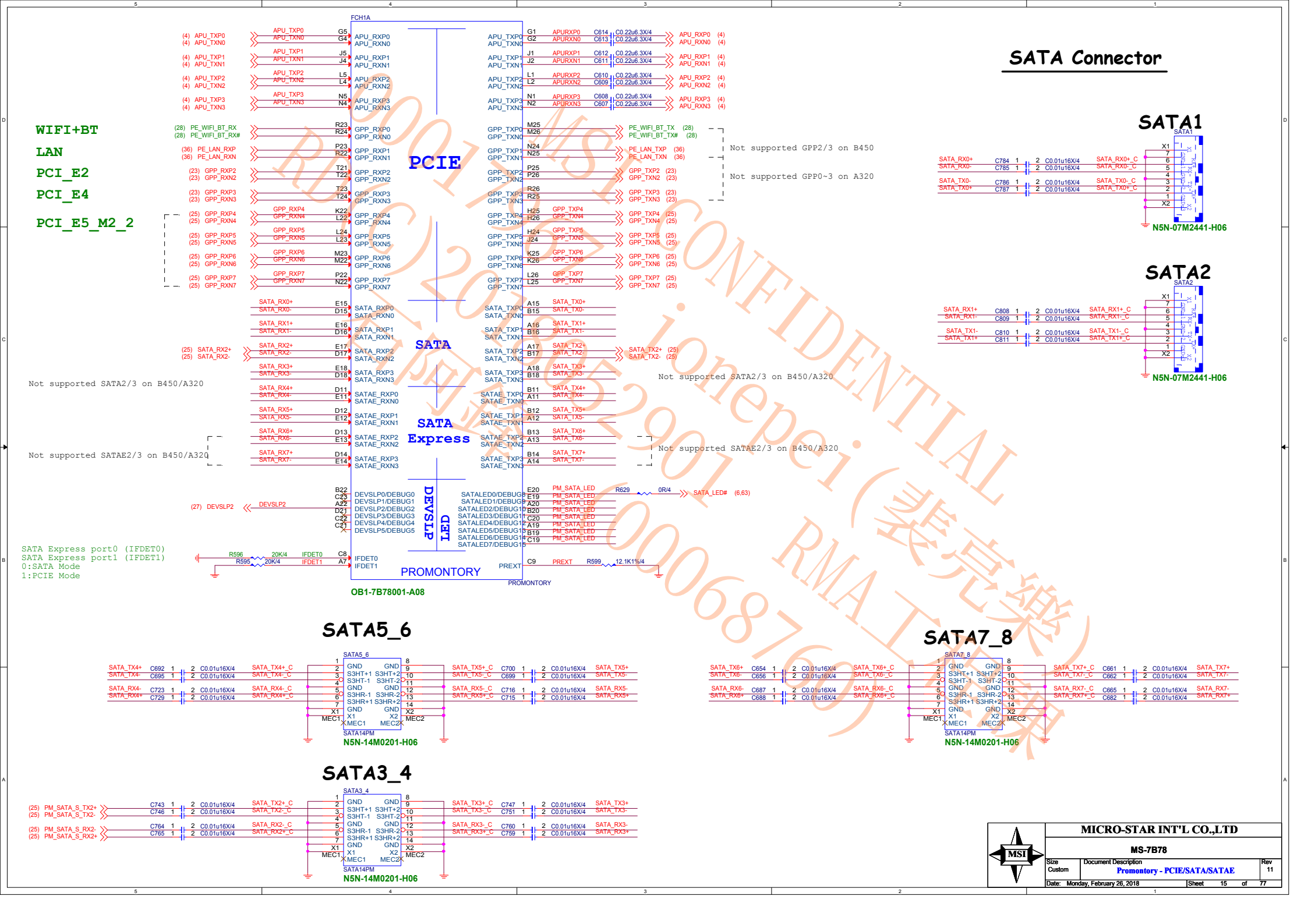
SATA Connector
WIFI+BT
LAN
PCI_E2
PCI_E4
PCI_E5_M2_2
FCH1A
PCIE
SATA
SATA Express
DEVSLP
LED
PROMONTORY
Not supported GPP2/3 on B450
Not supported GPP0~3 on A320
Not supported SATA2/3 on B450/A320
Not supported SATAE2/3 on B450/A320
SATA Express port0 (IFDET0)
SATA Express port1 (IFDET1)
0:SATA Mode
1:PCIE Mode
OB1-7B78001-A08
SATA1
N5N-07M2441-H06
SATA2
N5N-07M2441-H06
SATA5_6
N5N-14M0201-H06
SATA7_8
N5N-14M0201-H06
SATA3_4
N5N-14M0201-H06
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Promontory - PCIE/SATA/SATAE
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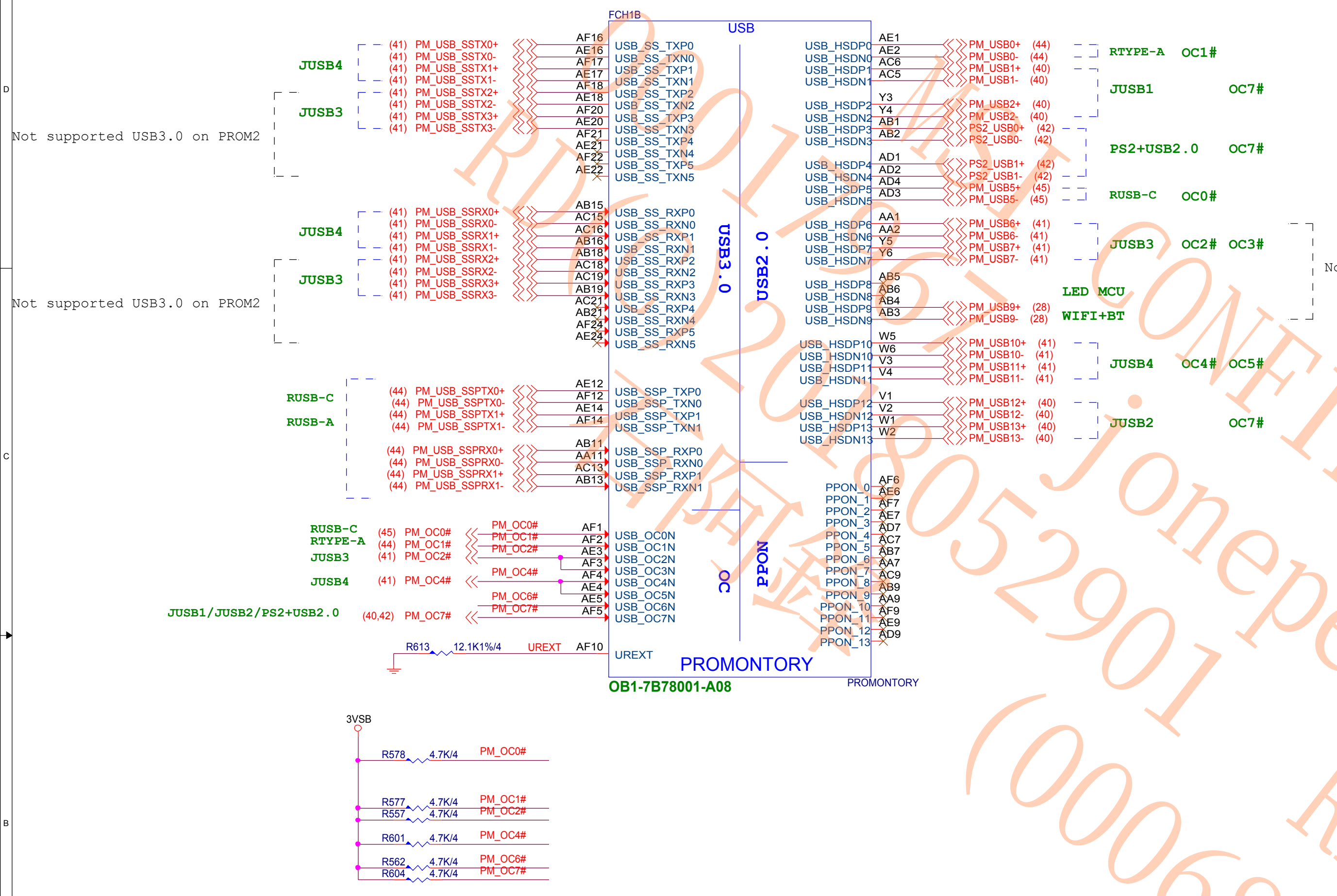

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

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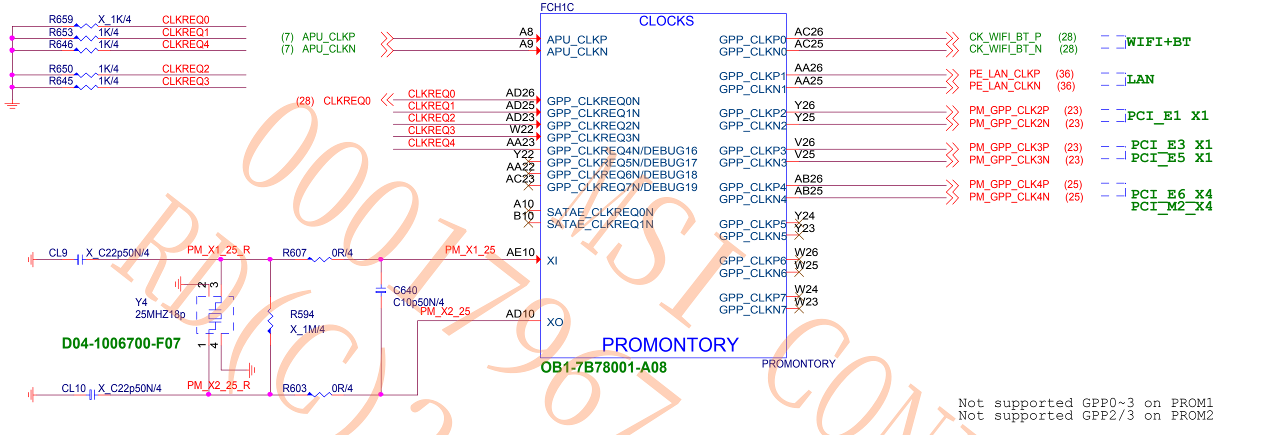
GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N

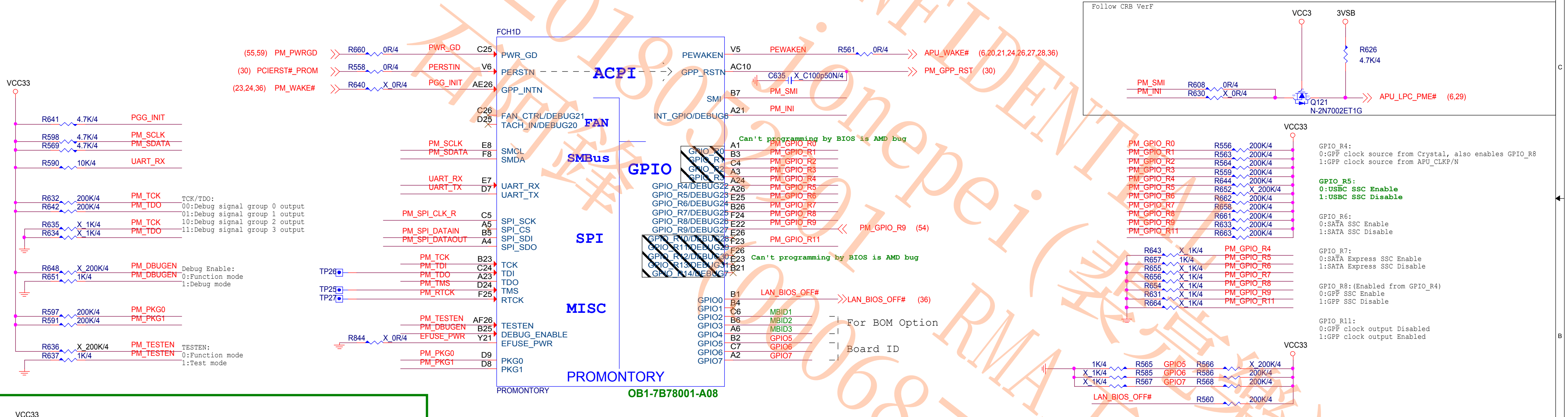


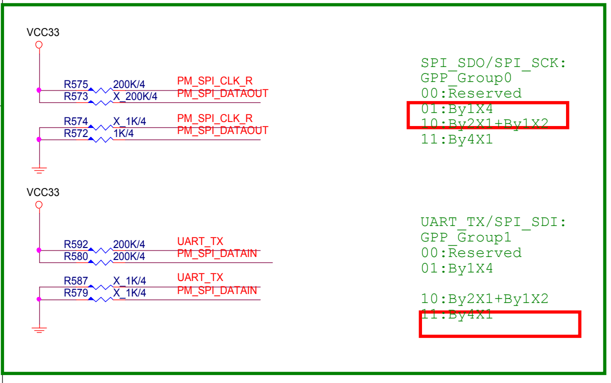
Not supported GPP0~3 on PROM1
Not supported GPP2/3 on PROM2

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

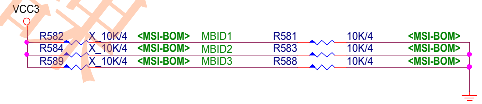
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK	
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7	
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7	CLK2.3不能用
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7	CLK1-3不能用





	MBID3	MBID2	MBID1
Z470	0	0	0

BOM OPTION



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Document Description: Promontory - CLK/ACPI/GPIO
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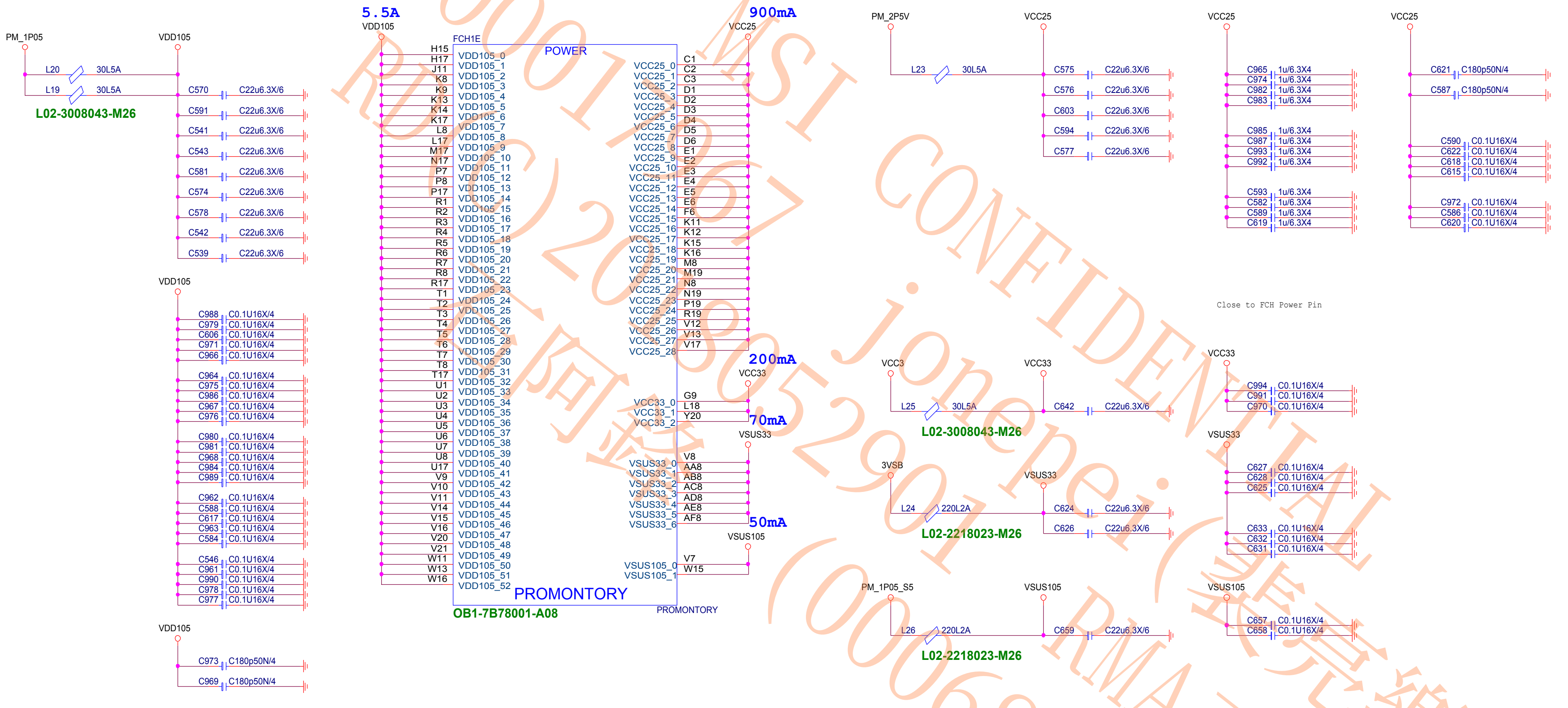

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Custom	Promontory - Power	11

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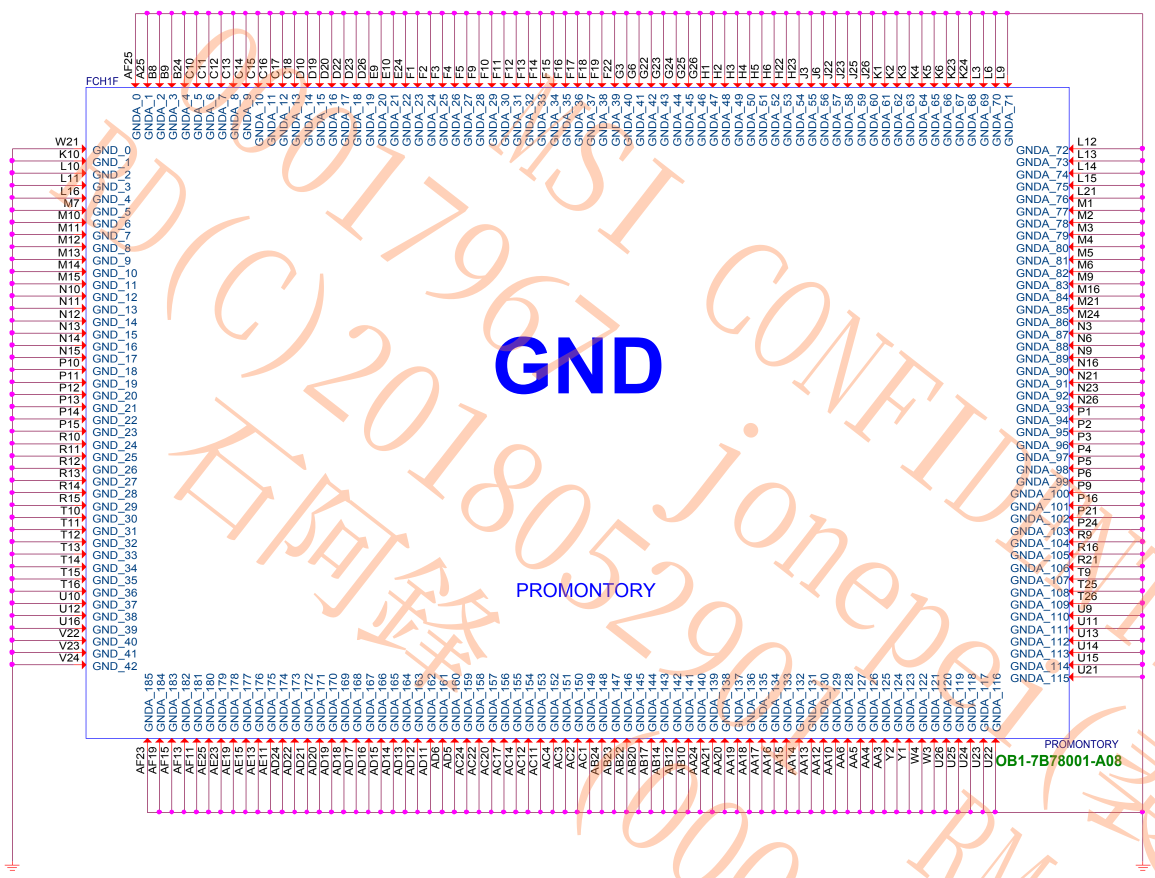

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Size: Custom	Document Description: Promontory - GND	Rev: 11
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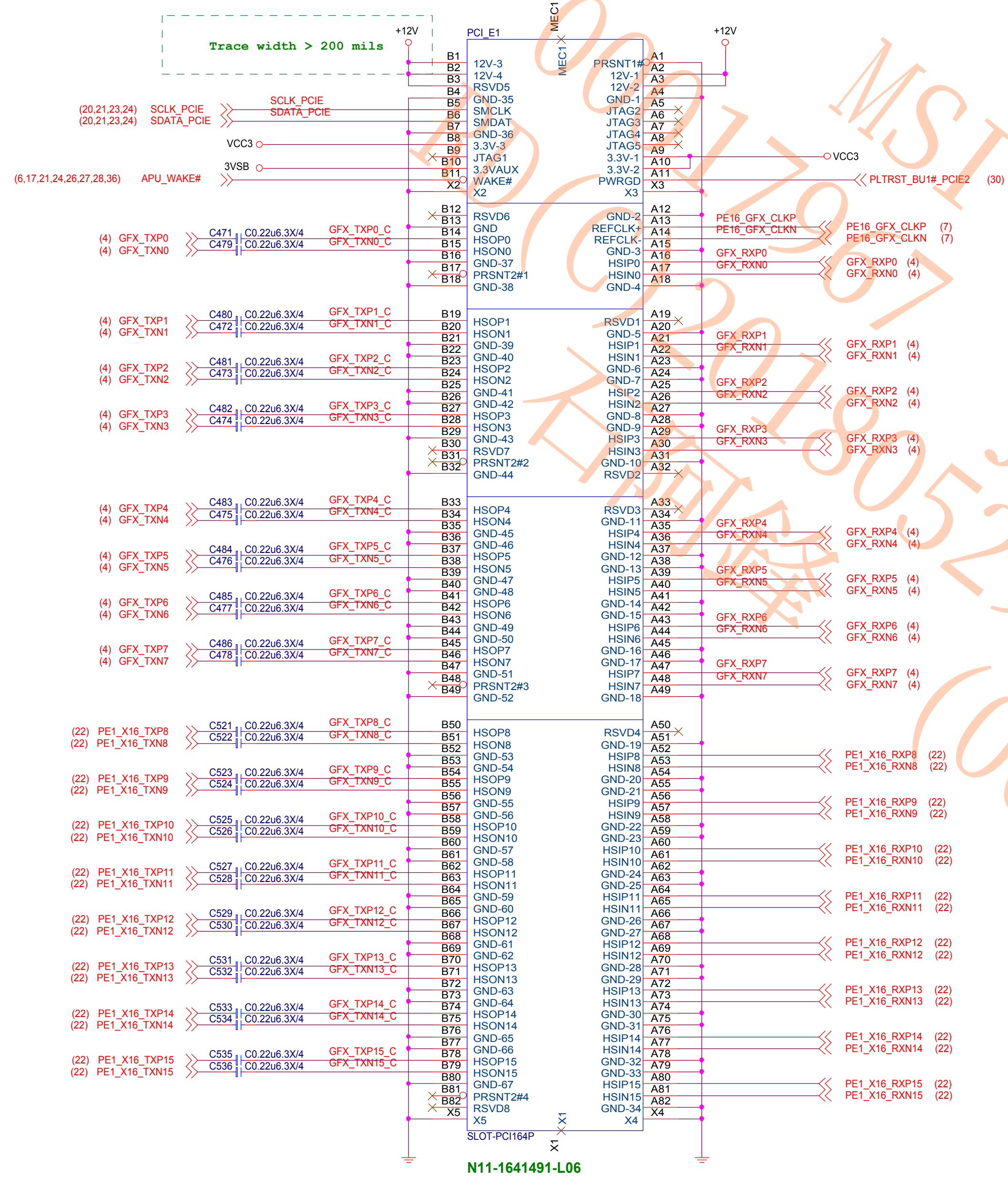
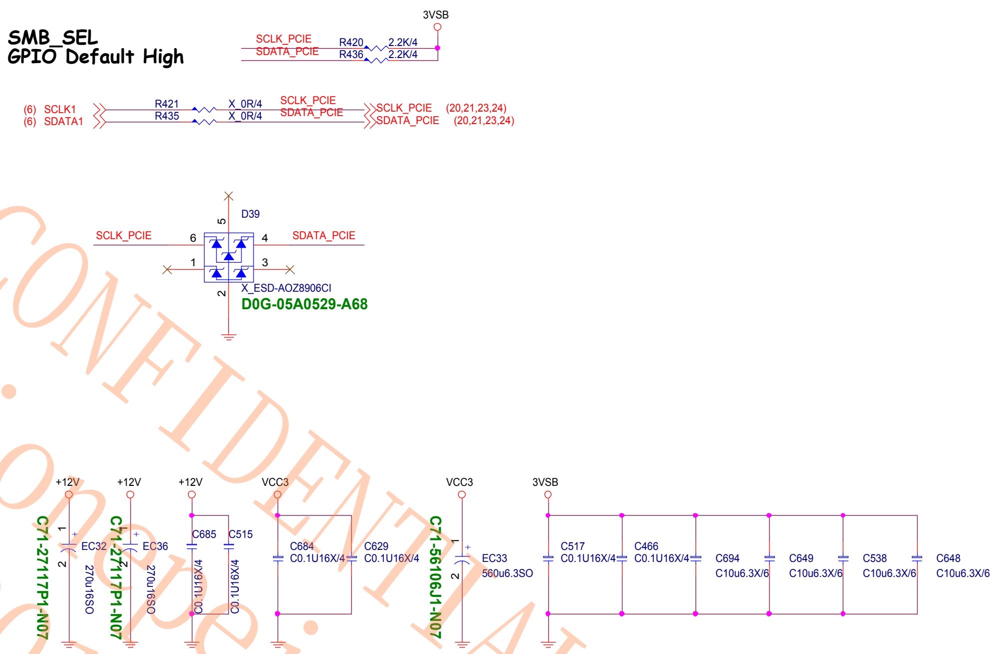
PCI EXPRESS x16 Slot

PCI_E1



SMB_SEL
GPIO Default High



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Custom	PCI_E2 (X16)	11

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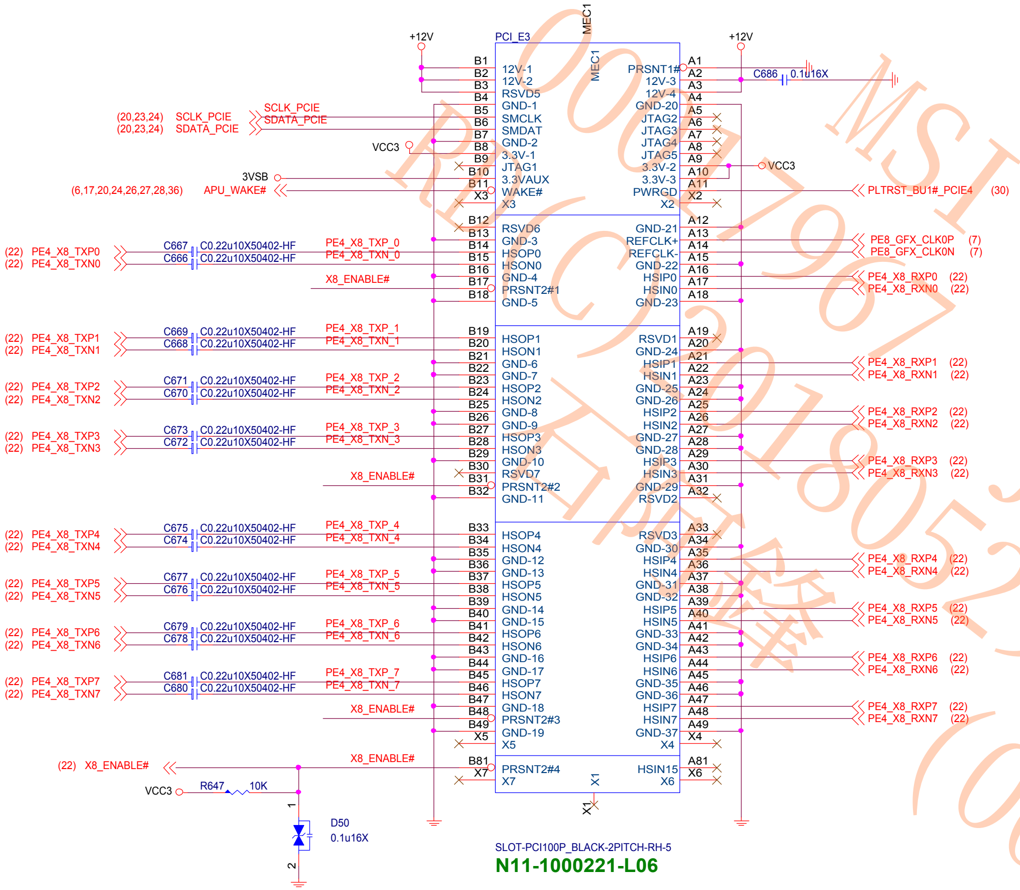
PCI EXPRESS x8 SLOT

PCI_E3



PCI Express x8 Slot		
+12V		- A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Custom	PCI_E4 (X8)	11

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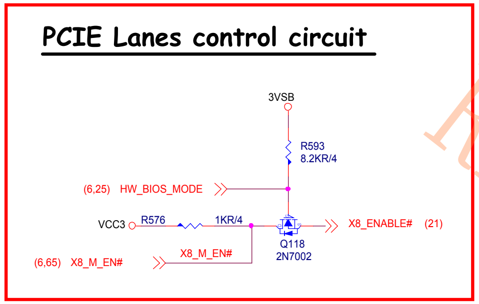
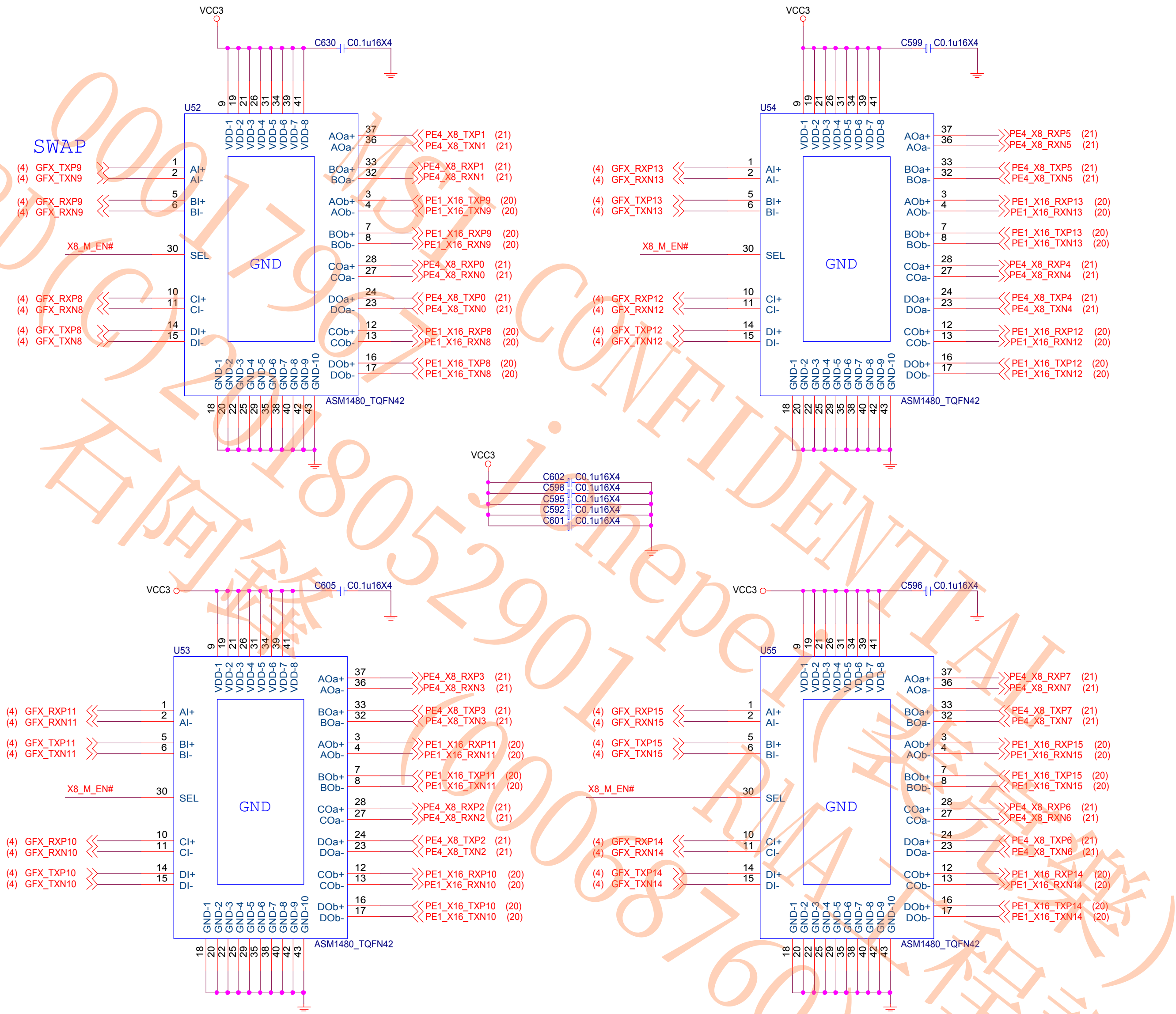
PCI EXPRESS Switch

For PCIE1 & PCIE3



	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0


SWAP
VCC3
U52
U53
U54
U55
ASM1480_TQFN42
GND
C630 C0.1u16X4
C599 C0.1u16X4
C605 C0.1u16X4
C596 C0.1u16X4
C602 C0.1u16X4
C598 C0.1u16X4
C595 C0.1u16X4
C592 C0.1u16X4
C601 C0.1u16X4
X8_M_EN#
SEL
(4) GFX_TXP9
(4) GFX_TXN9
(4) GFX_RXP9
(4) GFX_RXN9
(4) GFX_RXP8
(4) GFX_RXN8
(4) GFX_TXP8
(4) GFX_TXN8
PE4_X8_TXP1 (21)
PE4_X8_TXN1 (21)
PE4_X8_RXP1 (21)
PE4_X8_RXN1 (21)
PE1_X16_TXP9 (20)
PE1_X16_TXN9 (20)
PE1_X16_RXP9 (20)
PE1_X16_RXN9 (20)
PE4_X8_RXP0 (21)
PE4_X8_RXN0 (21)
PE4_X8_TXP0 (21)
PE4_X8_TXN0 (21)
PE1_X16_RXP8 (20)
PE1_X16_RXN8 (20)
PE1_X16_TXP8 (20)
PE1_X16_TXN8 (20)
(4) GFX_RXP13
(4) GFX_RXN13
(4) GFX_TXP13
(4) GFX_TXN13
(4) GFX_RXP12
(4) GFX_RXN12
(4) GFX_TXP12
(4) GFX_TXN12
PE4_X8_RXP5 (21)
PE4_X8_RXN5 (21)
PE4_X8_TXP5 (21)
PE4_X8_TXN5 (21)
PE1_X16_RXP13 (20)
PE1_X16_RXN13 (20)
PE1_X16_TXP13 (20)
PE1_X16_TXN13 (20)
PE4_X8_RXP4 (21)
PE4_X8_RXN4 (21)
PE4_X8_TXP4 (21)
PE4_X8_TXN4 (21)
PE1_X16_RXP12 (20)
PE1_X16_RXN12 (20)
PE1_X16_TXP12 (20)
PE1_X16_TXN12 (20)
(4) GFX_RXP11
(4) GFX_RXN11
(4) GFX_TXP11
(4) GFX_TXN11
(4) GFX_RXP10
(4) GFX_RXN10
(4) GFX_TXP10
(4) GFX_TXN10
PE4_X8_RXP3 (21)
PE4_X8_RXN3 (21)
PE4_X8_TXP3 (21)
PE4_X8_TXN3 (21)
PE1_X16_RXP11 (20)
PE1_X16_RXN11 (20)
PE1_X16_TXP11 (20)
PE1_X16_TXN11 (20)
PE4_X8_RXP2 (21)
PE4_X8_RXN2 (21)
PE4_X8_TXP2 (21)
PE4_X8_TXN2 (21)
PE1_X16_RXP10 (20)
PE1_X16_RXN10 (20)
PE1_X16_TXP10 (20)
PE1_X16_TXN10 (20)
(4) GFX_RXP15
(4) GFX_RXN15
(4) GFX_TXP15
(4) GFX_TXN15
(4) GFX_RXP14
(4) GFX_RXN14
(4) GFX_TXP14
(4) GFX_TXN14
PE4_X8_RXP7 (21)
PE4_X8_RXN7 (21)
PE4_X8_TXP7 (21)
PE4_X8_TXN7 (21)
PE1_X16_RXP15 (20)
PE1_X16_RXN15 (20)
PE1_X16_TXP15 (20)
PE1_X16_TXN15 (20)
PE4_X8_RXP6 (21)
PE4_X8_RXN6 (21)
PE4_X8_TXP6 (21)
PE4_X8_TXN6 (21)
PE1_X16_RXP14 (20)
PE1_X16_RXN14 (20)
PE1_X16_TXP14 (20)
PE1_X16_TXN14 (20)

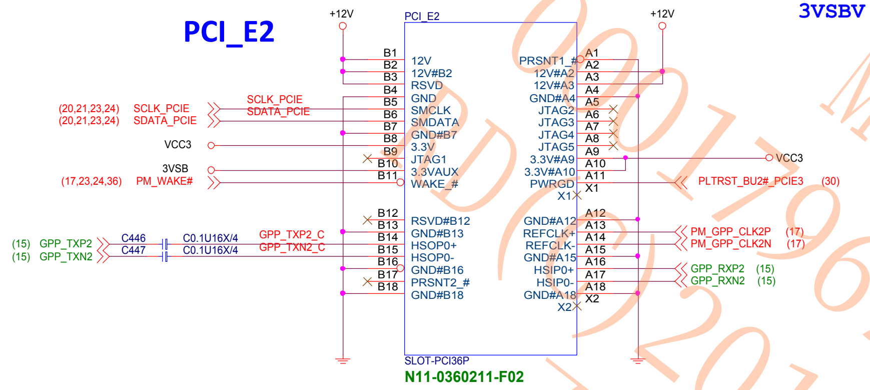
PCI EXPRESS X1 SLOT

12V - 0.5A

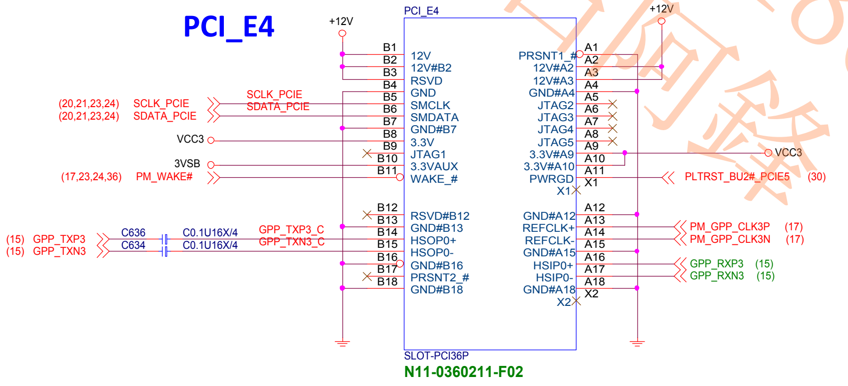
VCC3 - 3A

3VSBV - 375mA

PCI_E2



PCI_E4



PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

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Custom	PCI_E1_E3_E5 (X1)	11

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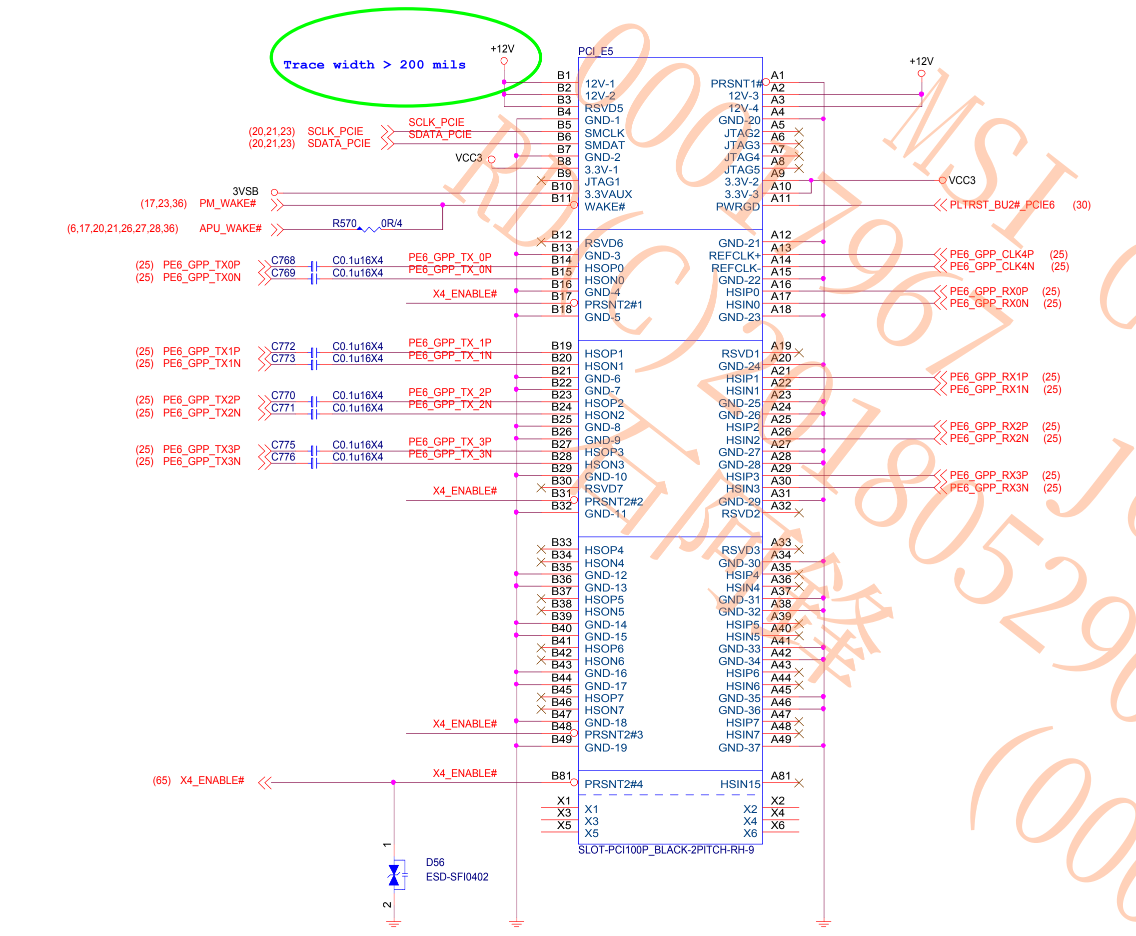
PCI EXPRESS X4 SLOT

PCI_E6



PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Size: Custom	Document Description: PCI_E6 (X4)	Rev: 11
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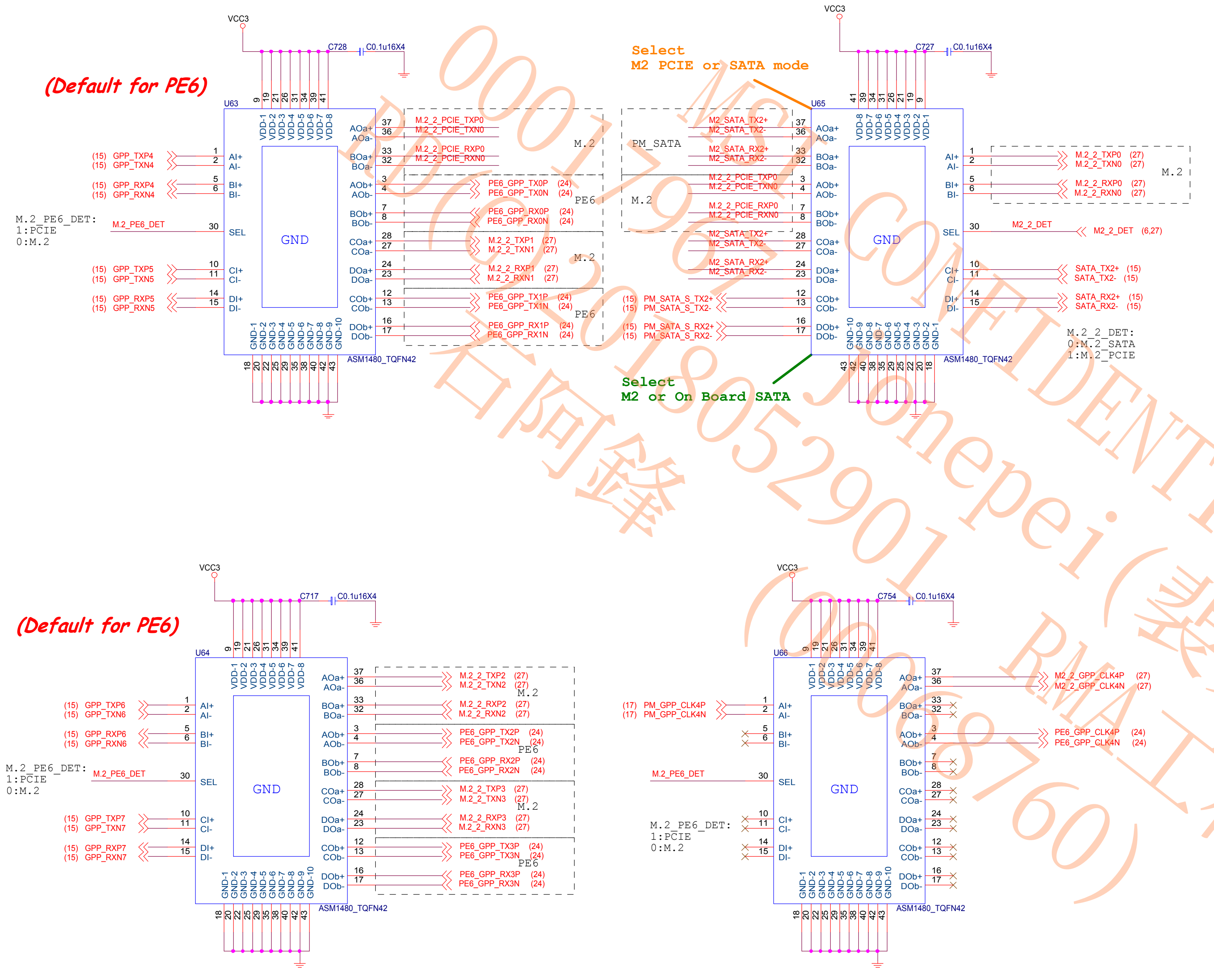
PCI_E6 and M2_2 and SATA1 Switch



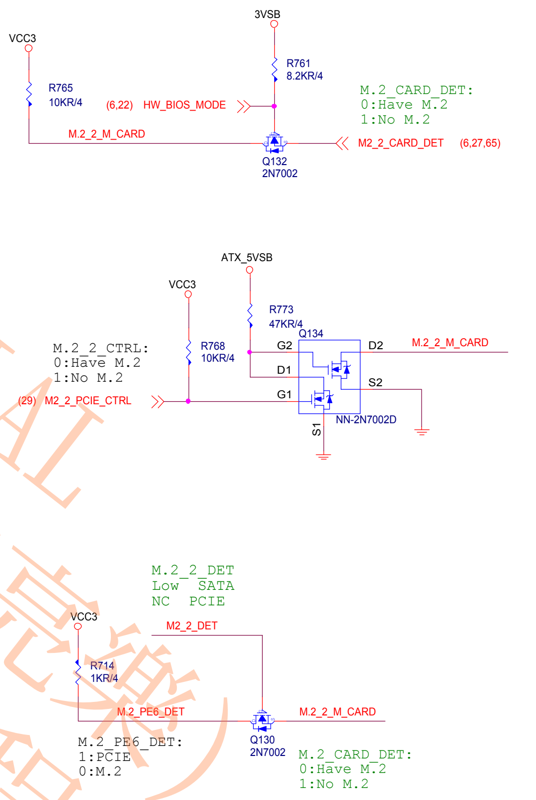
Manufature Control

	AUTO Mode	PCIE X4	M.2 X4	M.2 SATA	SATA5
HW_BIOS_MODE	1	0	0	1	
M2_2_PCIE_CTRL	0	1	0	0	

Device Detect

	AUTO Mode	PCIE X4	M.2 X4	M.2 SATA	SATA5
M2_2_CARD_DET		1 0	0	0	1 0
M2_2_DET		1 0	1	0	1

紅色數字為判抓到PCIE或SATA device時所要判斷的訊號



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Custom	PCIE Switch PE6 / M2_2	11

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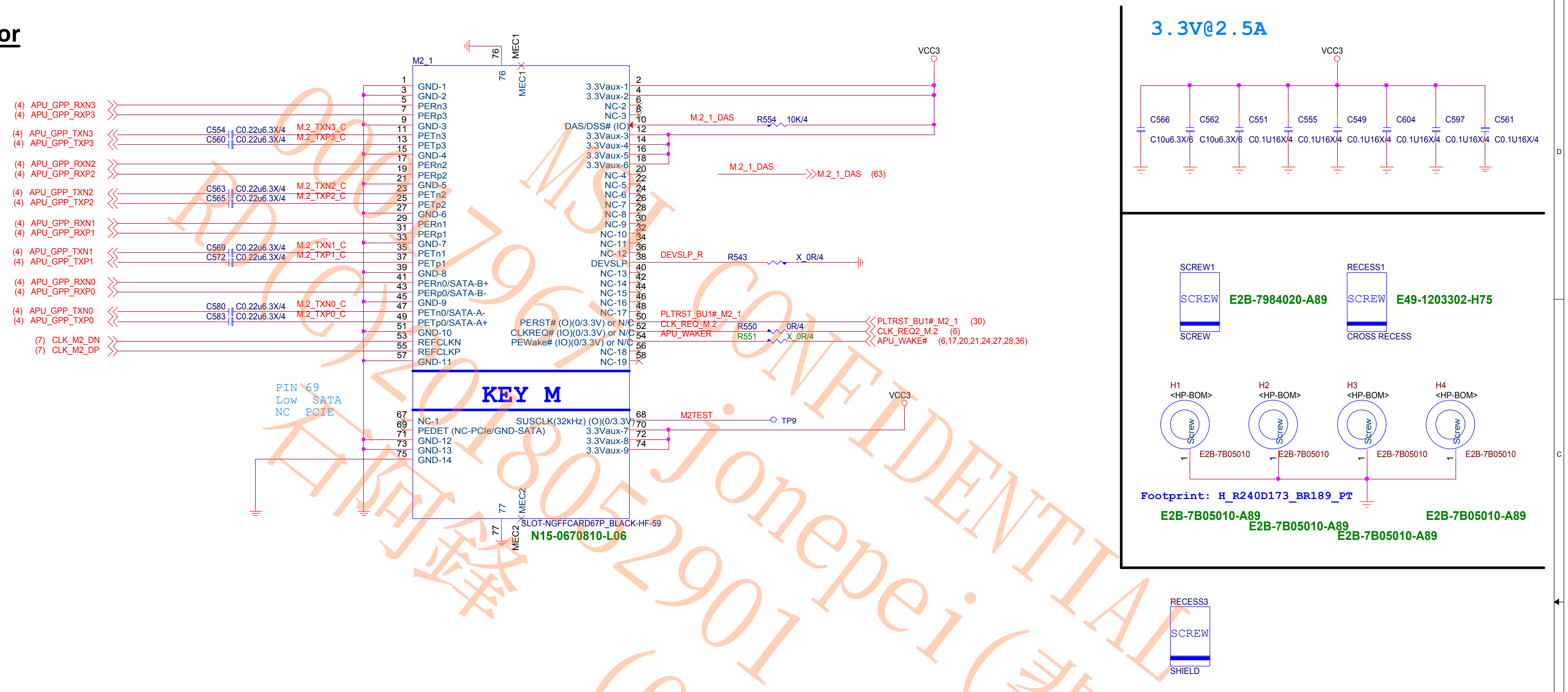
M.2_1 Connector

3.3V@2.5A



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Size: Custom	Document Description: M2_1		Rev: 11
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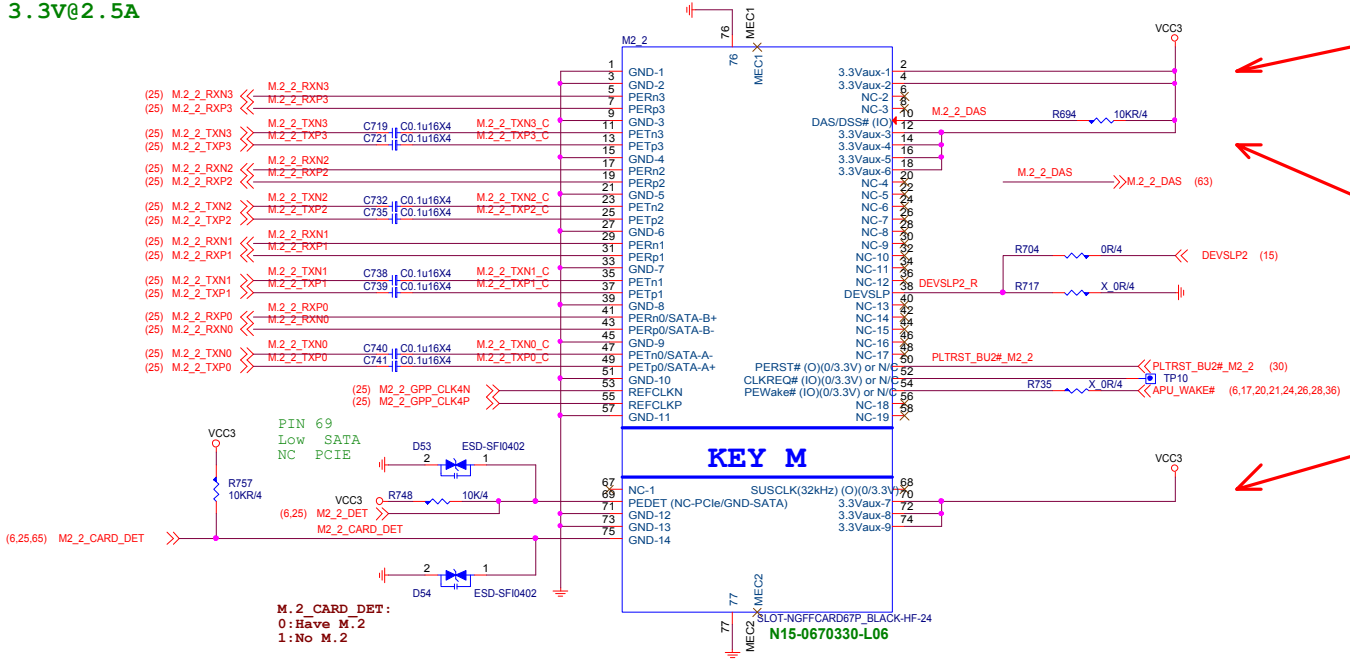
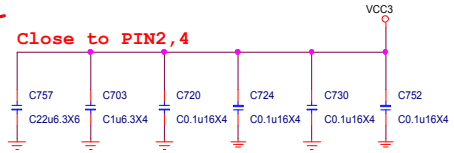
M.2_2 Connector

3.3V@2.5A

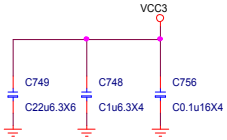


VCC3 2.5A

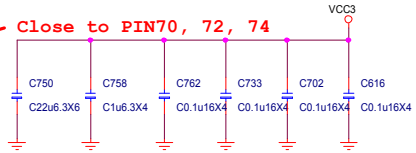
Close to PIN2,4

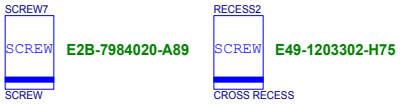


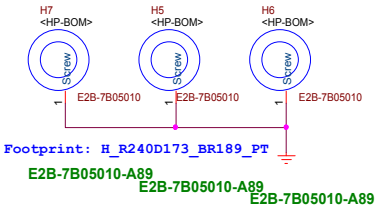
Close to PIN12, 14, 16, 18



Close to PIN70, 72, 74







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Size: Custom	Document Description: M2_2	Rev: 11
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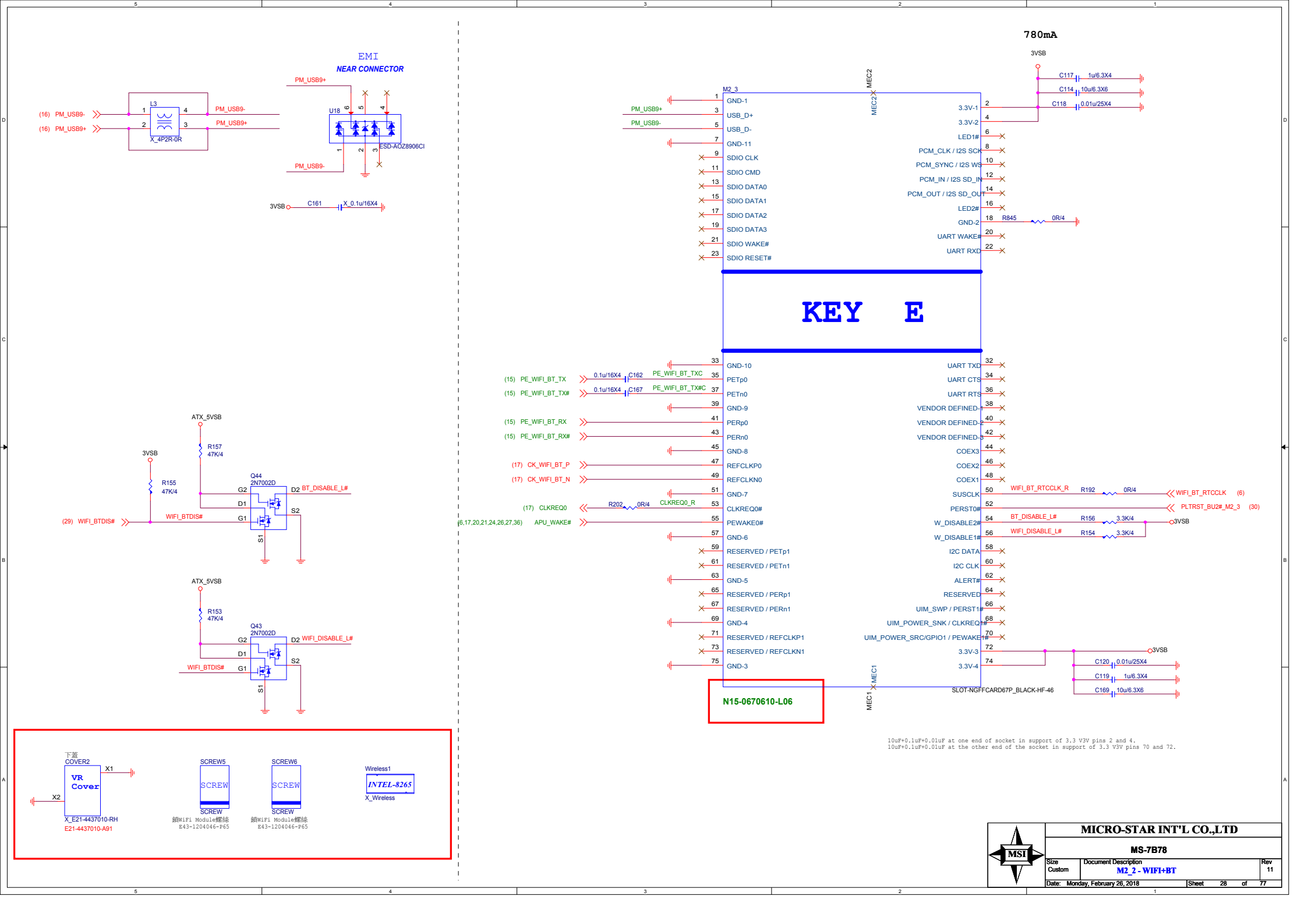
EMI
NEAR CONNECTOR
780mA
KEY E
M2_3
MEC2
MEC1
N15-0670610-L06
SLOT-NGFFCARD67P_BLACK-HF-46
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
PM_USB9+
PM_USB9-
3VSB
ATX_5VSB
BT_DISABLE_L#
WIFI_DISABLE_L#
WIFI_BTDIS#
WIFI_BT_RTCCLK_R
WIFI_BT_RTCCLK
PLTRST_BU2#_M2_3
APU_WAKE#
CLKREQ0_R
PE_WIFI_BT_TXC
PE_WIFI_BT_TX#C
10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.
下蓋
COVER2
VR Cover
X_E21-4437010-RH
E21-4437010-A91
SCREW5
SCREW6
SCREW
鎖WiFi Module螺絲
E43-1204046-P65
Wireless1
INTEL-8265
X_Wireless
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MS-7B78
Document Description
M2_2 - WIFI+BT
Rev
11
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Custom
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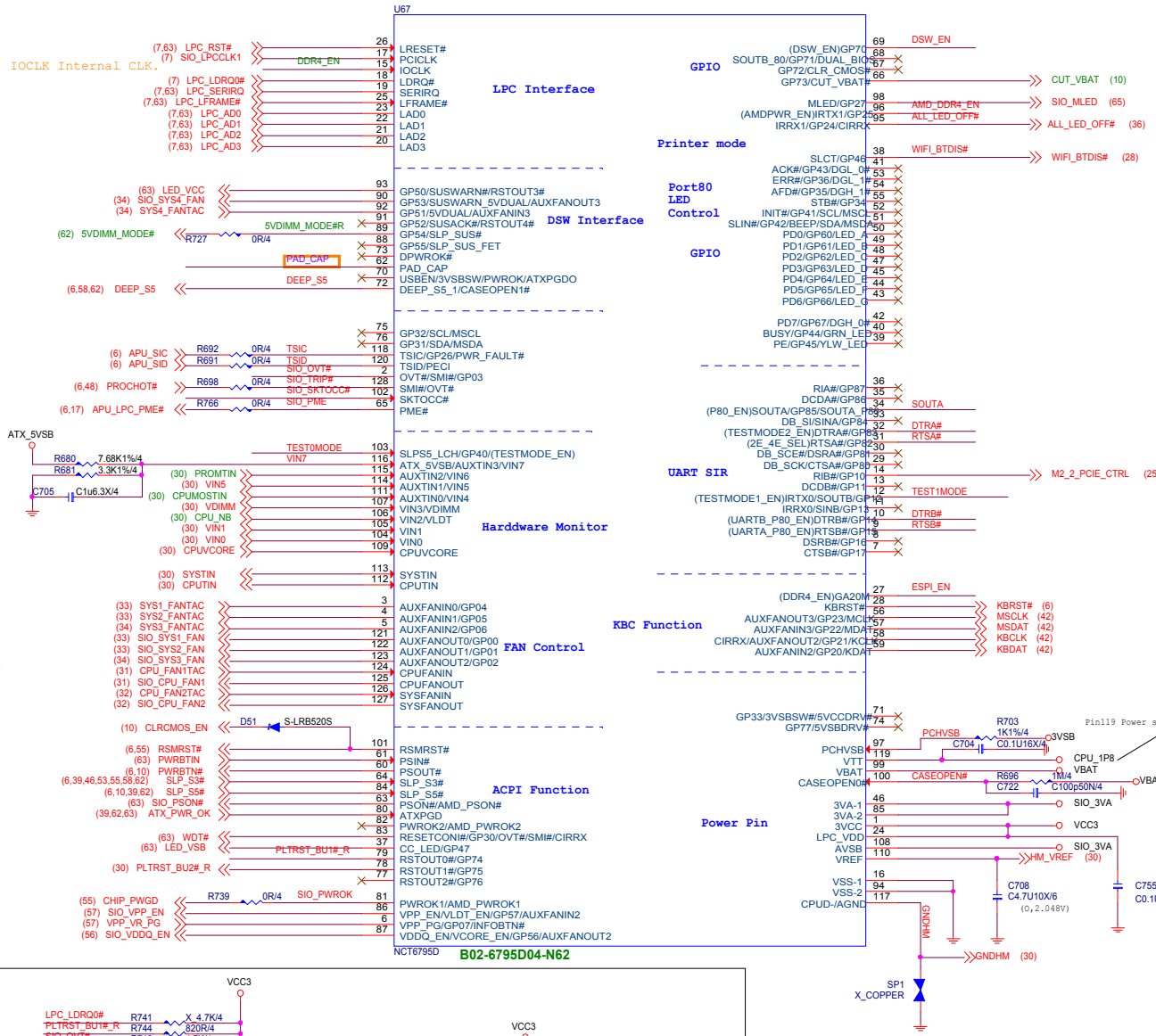
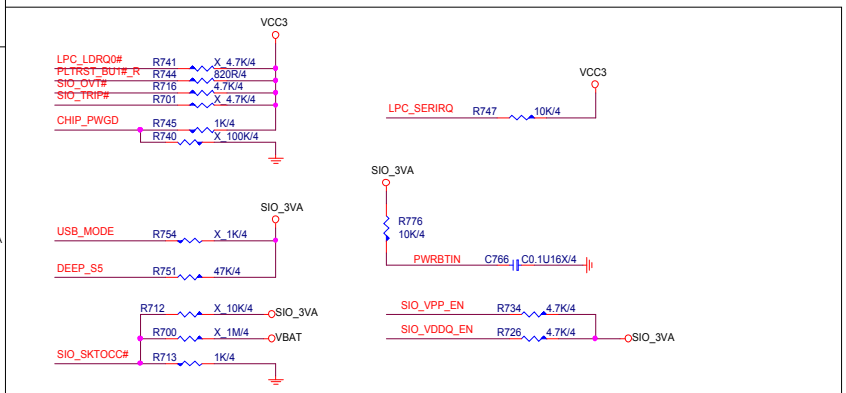
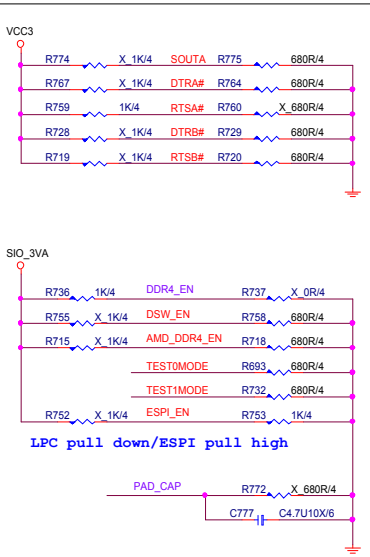
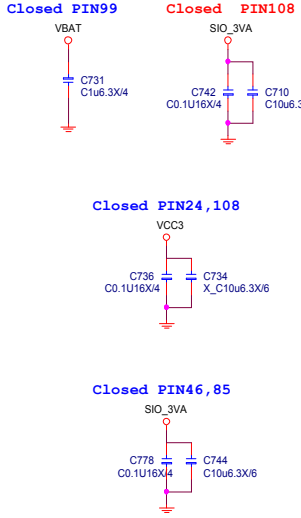


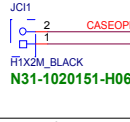


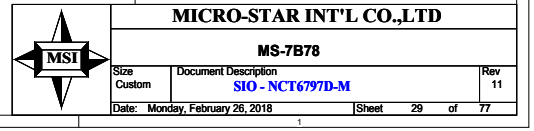
POWER ON STRAPPING PIN FOR NCT6797/6795					
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO



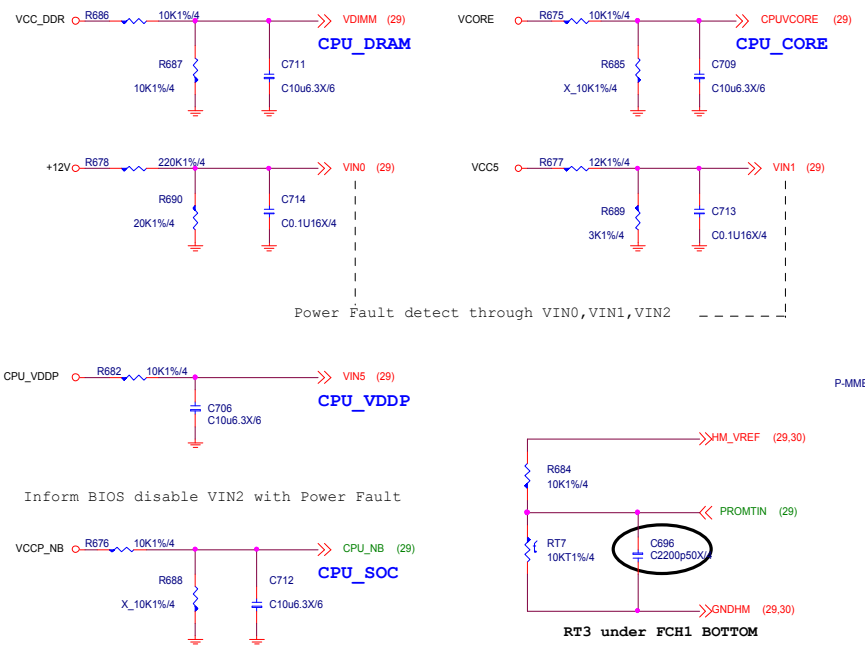




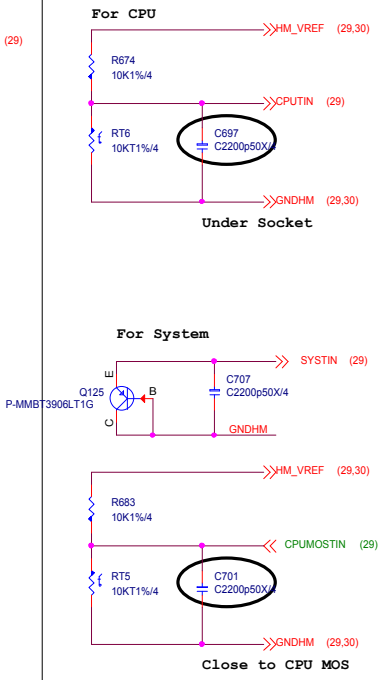


HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

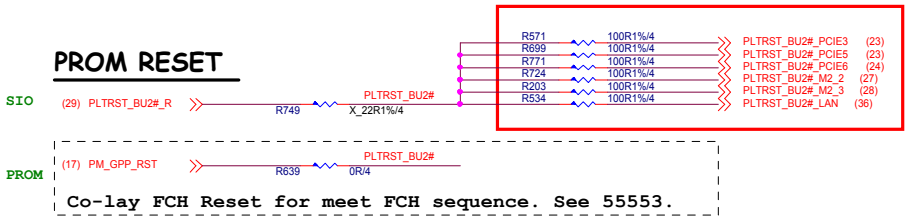


TEMP SENSOR

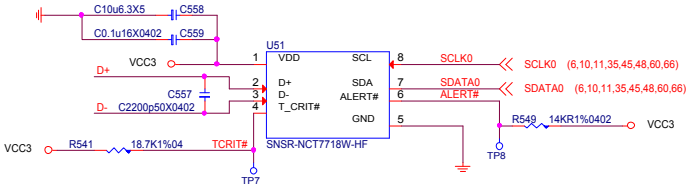


COM PORT

PROM RESET

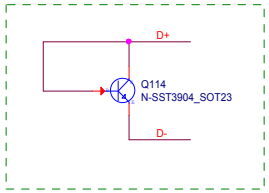


NCT7718W



NCT7718W SM Bus address is 98h (1001100xb)

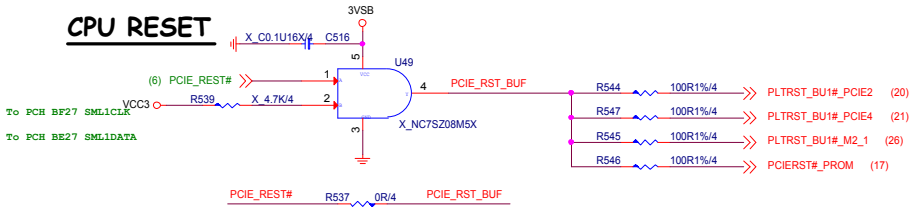
Default: ALERT# Output Comparator Mode



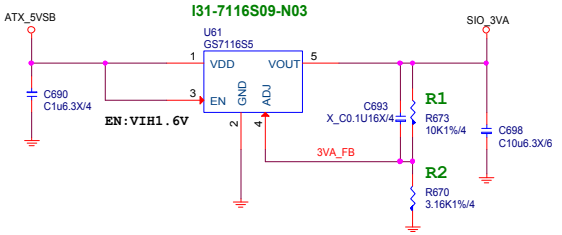
Layout notice:
1. Put the C1 2200pF to close the NCT7718W.
2. Add Ground Shielding For D+ and D- Traces.
3. D+/D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

CPU RESET



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

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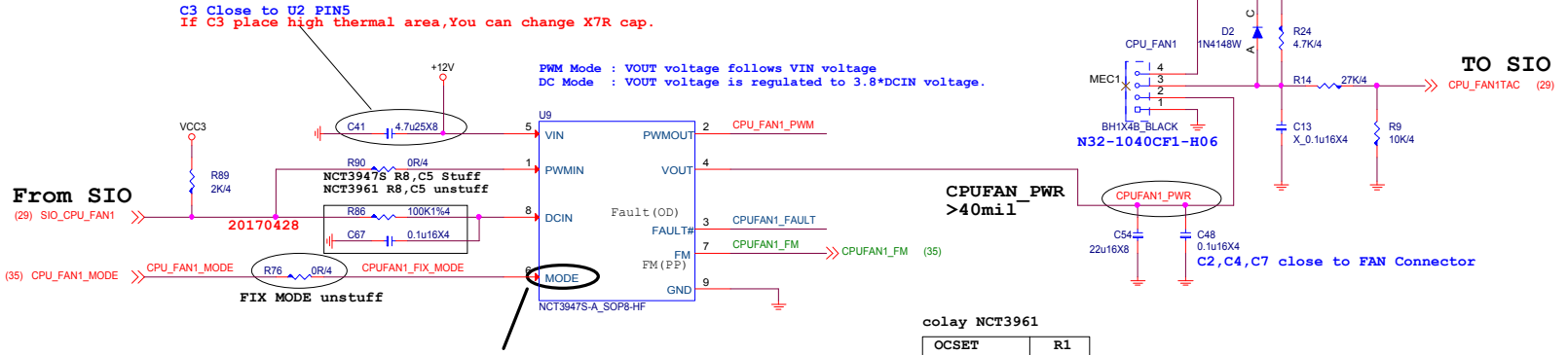
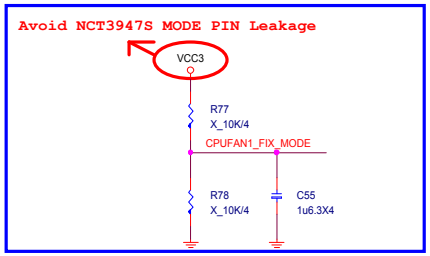
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can swtich PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1_LED_OFF_BLINK Use LED On/OFF

CPUFAN1





Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control

	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internall pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R84 100K/4 CPUFAN1_FAULT

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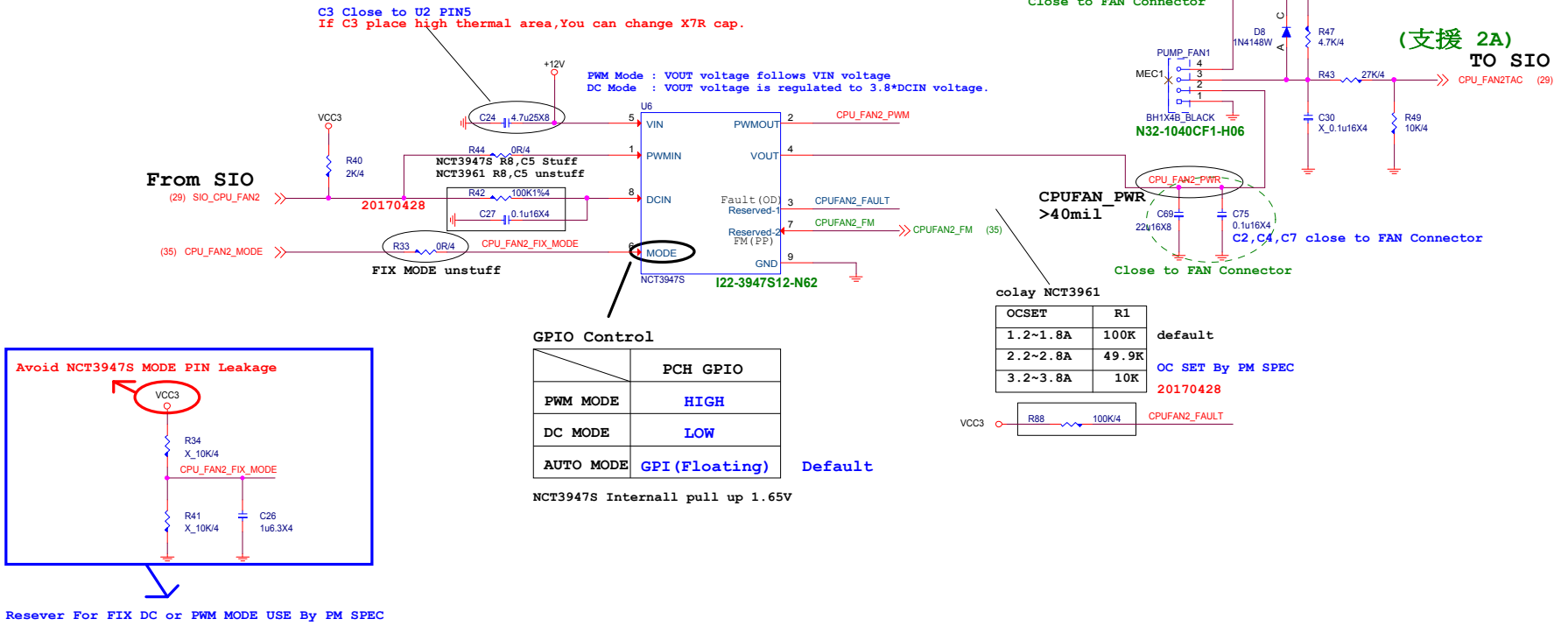
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can swtich PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1_LED_OFF_BLINK Use LED On/OFF



OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	
3.2~3.8A	10K	

GPIO Control

	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

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Size: Custom	Document Description: FAN TYPE-J PUMPFAN1	Rev: 11
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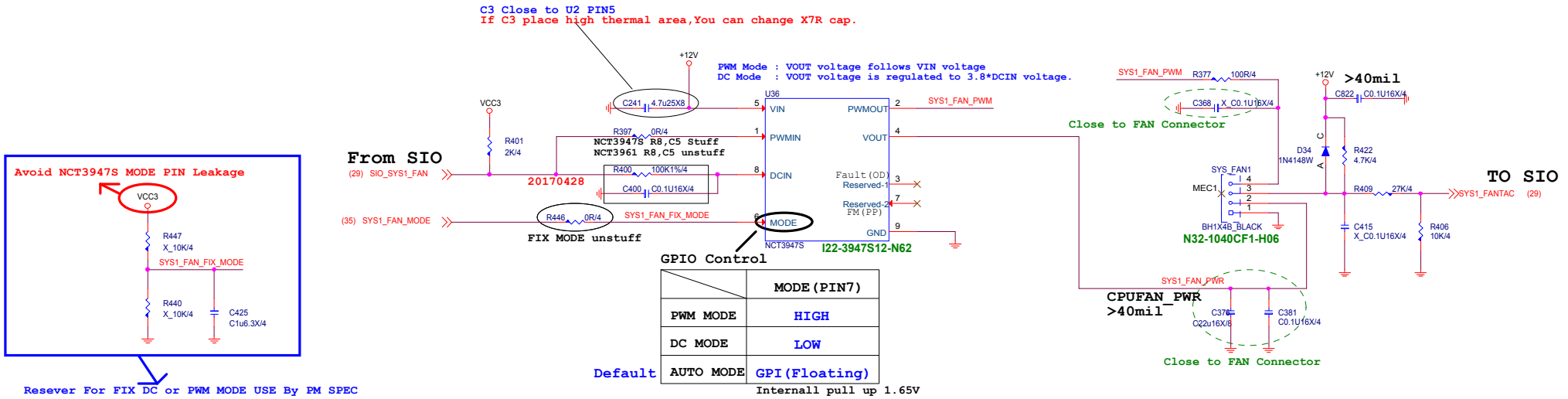
SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

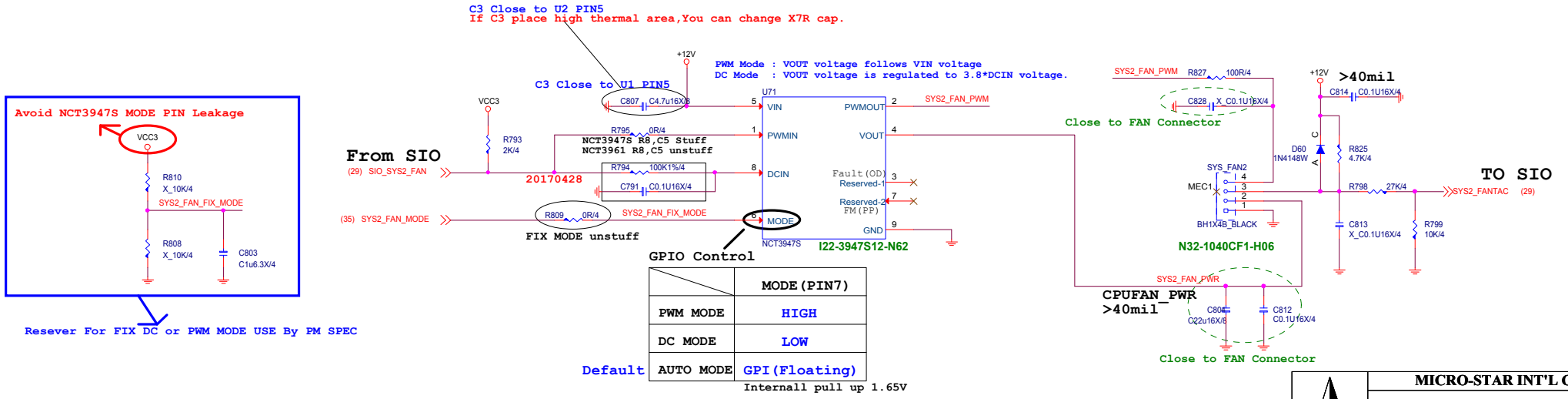
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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MS-7B78	
Size: Custom	Document Description: FAN TYPE-K SYSFAN1/2 — Rev: 11
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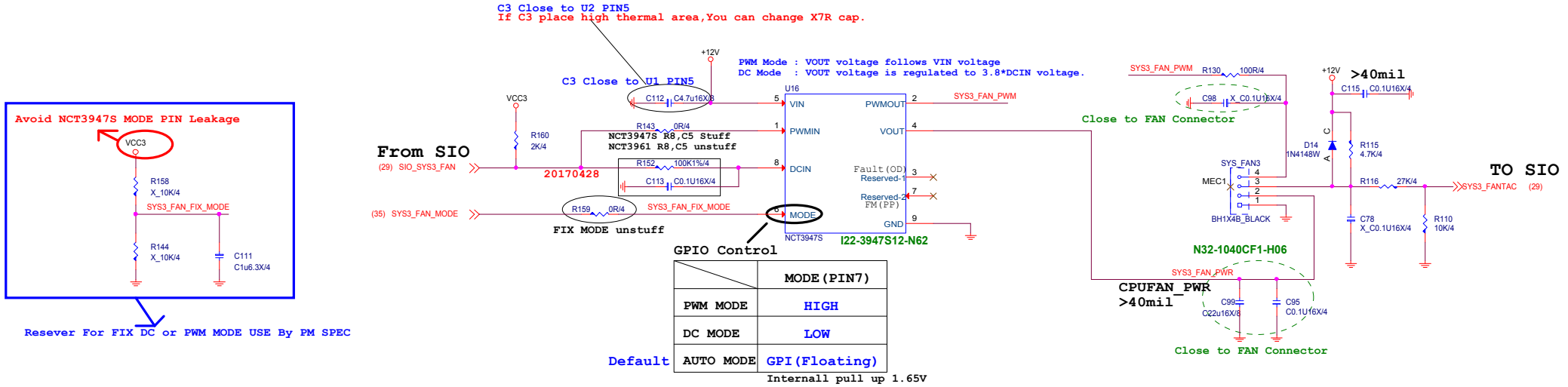
SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

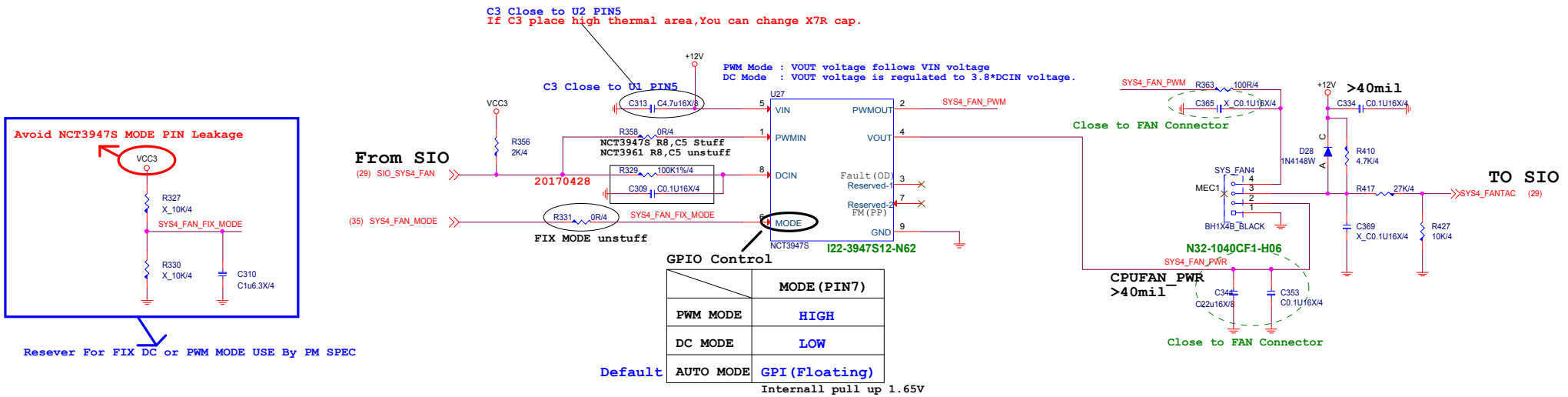
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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MS-7B78	
Size: Custom	Document Description: FAN TYPE-K SYSFAN3/4 — Rev: 11
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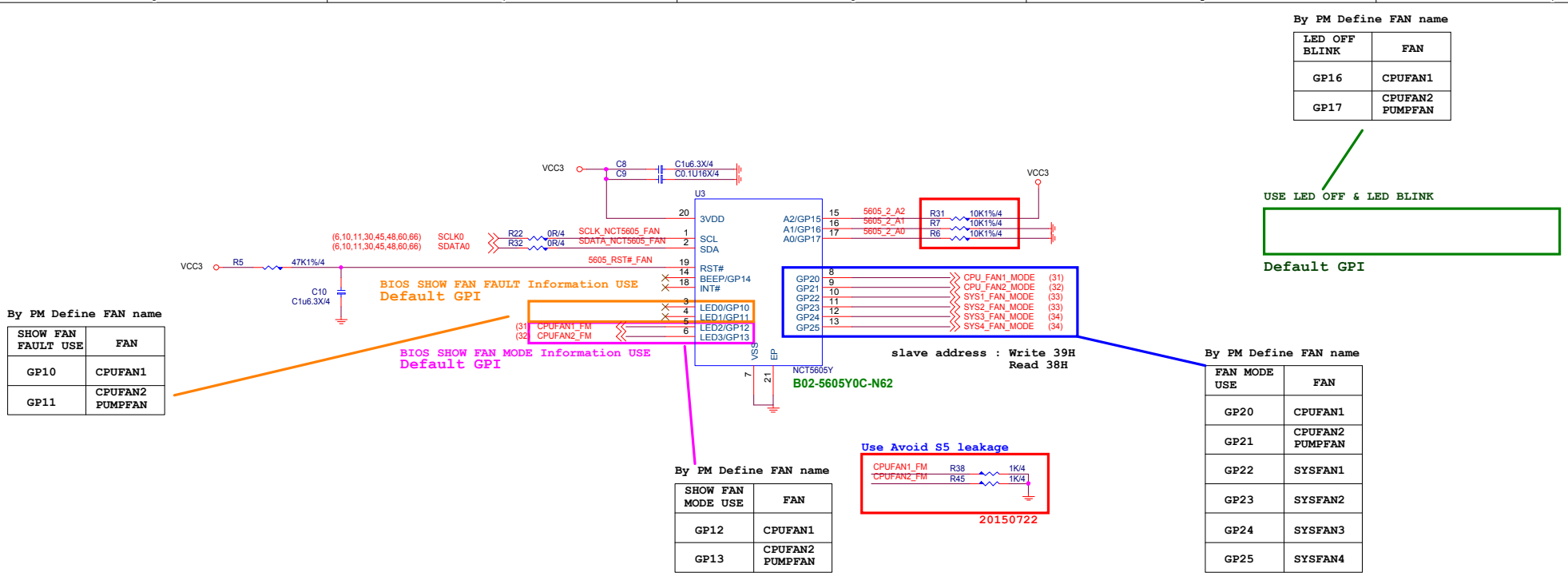


1. GENERAL DESCRIPTION

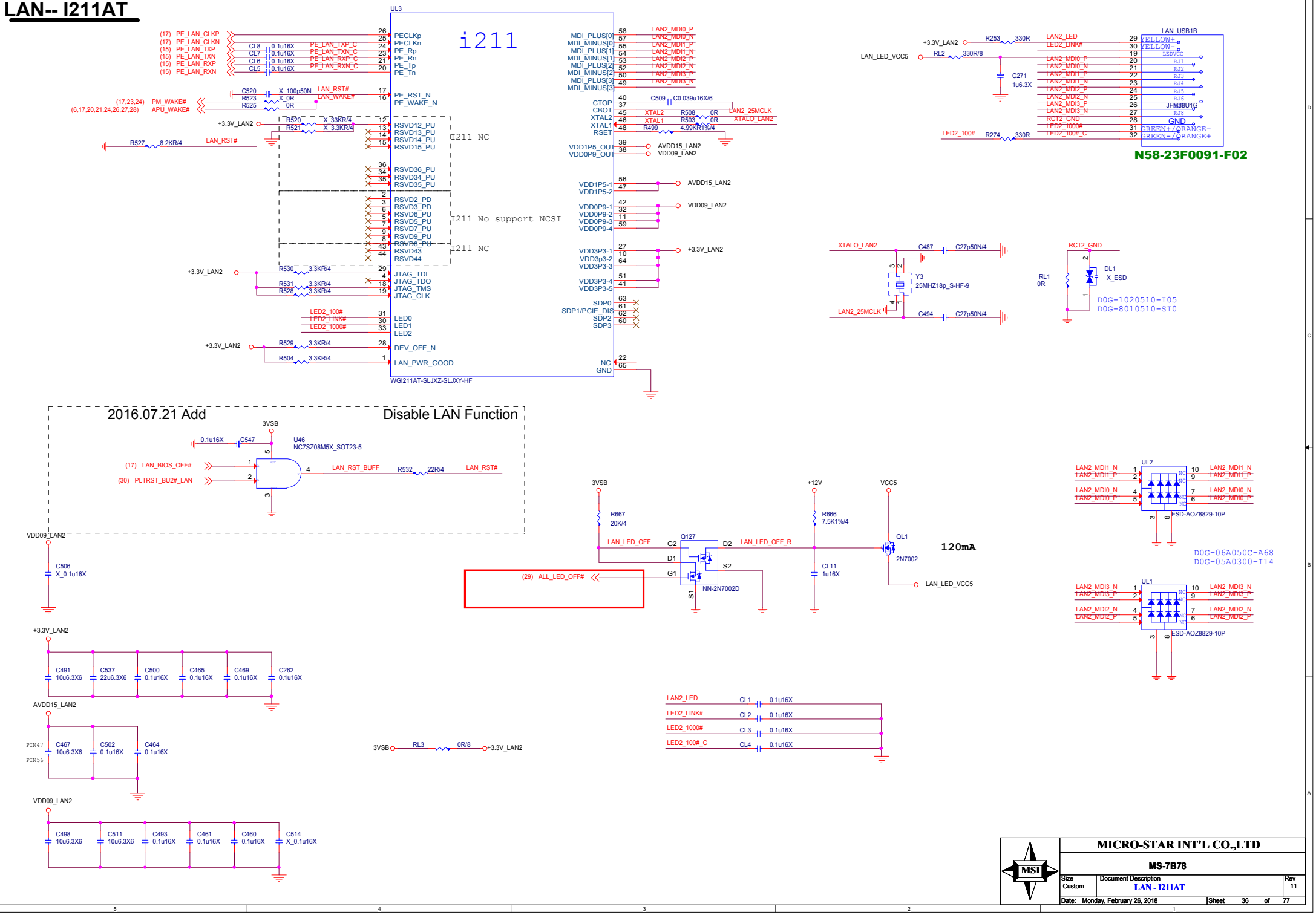
The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

R/W: 0 = write, 1 = read

LAN-- I211AT


UL3
i211
WGI211AT-SLJXZ-SLJXY-HF
I211 NC
I211 No support NCSI
I211 NC
2016.07.21 Add
Disable LAN Function
U46
NC7SZ08M5X_SOT23-5
Q127
NN-2N7002D
QL1
2N7002
120mA
UL2
UL1
ESD-AOZ8829-10P
LAN_USB1B
JFM38U1G
N58-23F0091-F02
Y3
25MHZ18p_S-HF-9
DL1
X_ESD
D0G-1020510-I05
D0G-8010510-SI0
D0G-06A050C-A68
D0G-05A0300-I14
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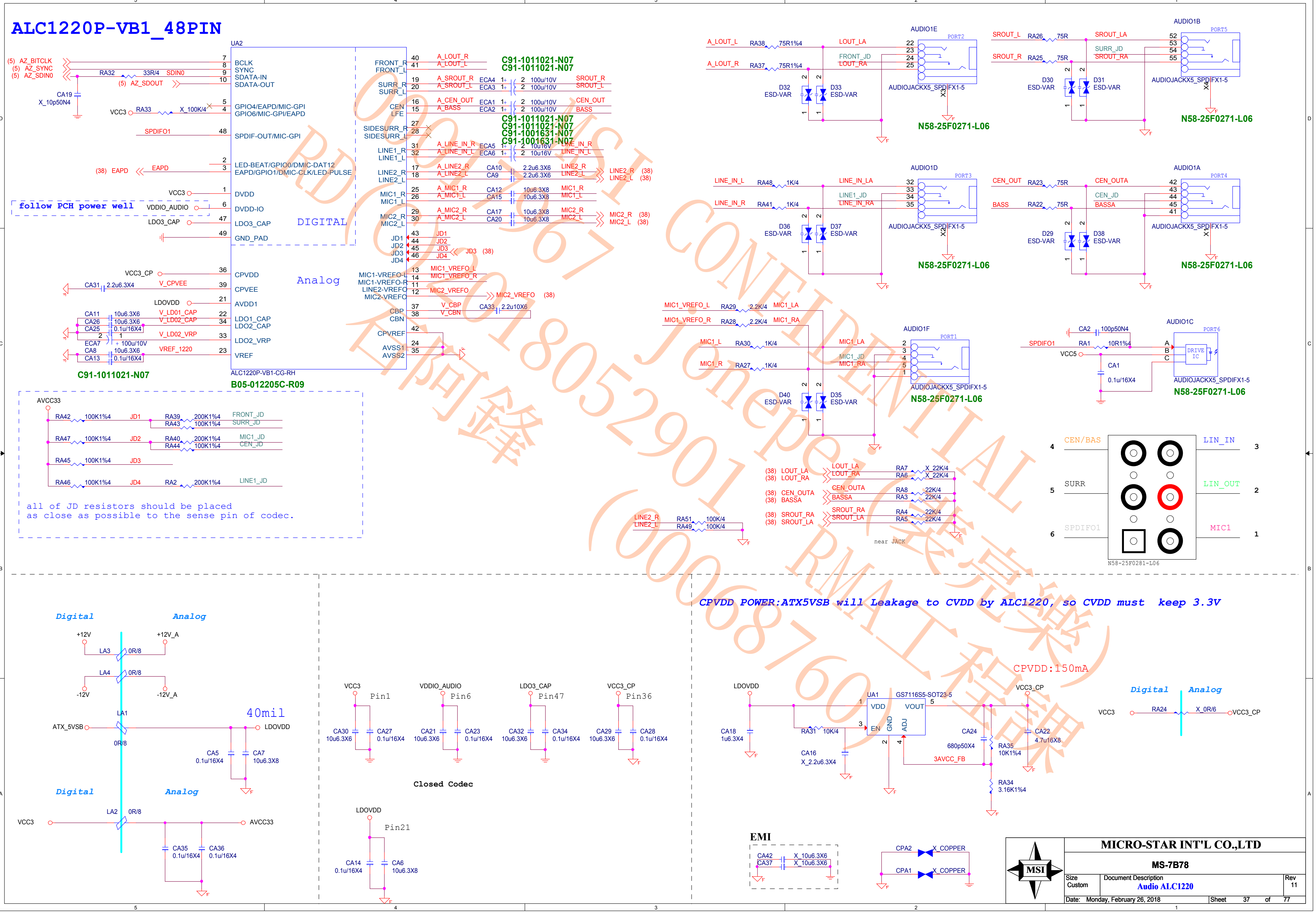
LAN - I211AT
Monday, February 26, 2018



ALC1220P-VB1_48PIN
UA2
ALC1220P-VB1-CG-RH
B05-012205C-R09
BCLK
SYNC
SDATA-IN
SDATA-OUT
GPIO4/EAPD/MIC-GPI
GPIO6/MIC-GPI/EAPD
SPDIF-OUT/MIC-GPI
LED-BEAT/GPIO0/DMIC-DAT12
EAPD/GPIO1/DMIC-CLK/LED-PULSE
DVDD
DVDD-IO
LDO3_CAP
GND_PAD
DIGITAL
Analog
CPVDD
CPVEE
AVDD1
LDO1_CAP
LDO2_CAP
LDO2_VRP
VREF
FRONT_R
FRONT_L
SURR_R
SURR_L
CEN
LFE
SIDESURR_R
SIDESURR_L
LINE1_R
LINE1_L
LINE2_R
LINE2_L
MIC1_R
MIC1_L
MIC2_R
MIC2_L
JD1
JD2
JD3
JD4
MIC1-VREFO-L
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
CBP
CBN
CPVREF
AVSS1
AVSS2
AZ_BITCLK
AZ_SYNC
AZ_SDIN0
AZ_SDOUT
SPDIFO1
EAPD
VCC3
VDDIO_AUDIO
LDO3_CAP
VCC3_CP
LDOVDD
follow PCH power well
C91-1011021-N07
C91-1001631-N07
AUDIO1E
AUDIO1B
AUDIO1D
AUDIO1A
AUDIO1F
AUDIO1C
AUDIOJACKX5_SPDIFX1-5
N58-25F0271-L06
ESD-VAR
DRIVE IC
near JACK
CEN/BAS
LIN_IN
SURR
LIN_OUT
SPDIFO1
MIC1
N58-25F0281-L06
AVCC33
FRONT_JD
SURR_JD
MIC1_JD
CEN_JD
LINE1_JD
all of JD resistors should be placed
as close as possible to the sense pin of codec.
Digital
Analog
+12V
+12V_A
-12V
-12V_A
ATX_5VSB
40mil
Pin1
Pin6
Pin47
Pin36
Pin21
Closed Codec
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V
CPVDD:150mA
UA1
GS7116S5-SOT23-5
VDD
VOUT
EN
GND
ADJ
3AVCC_FB
EMI
X_COPPER
MICRO-STAR INT'L CO.,LTD
MS-7B78
Size
Custom
Document Description
Audio ALC1220
Rev
11
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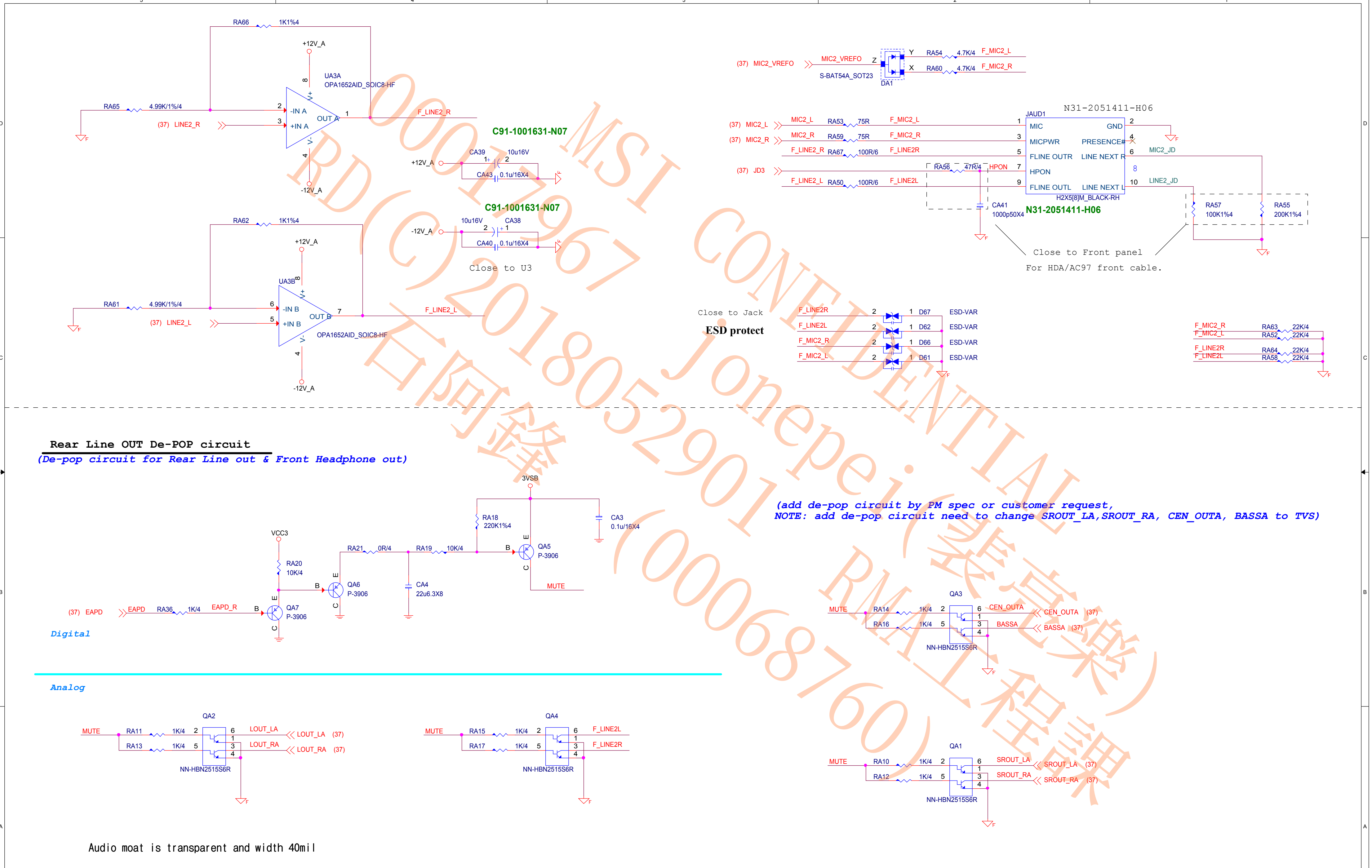

RA66 1K1%4
+12V_A
UA3A
OPA1652AID_SOIC8-HF
RA65 4.99K/1%/4
(37) LINE2_R
-IN A
+IN A
OUT A
F_LINE2_R
-12V_A
C91-1001631-N07
CA39 10u16V
+12V_A
CA43 0.1u/16X4
C91-1001631-N07
-12V_A
10u16V CA38
CA40 0.1u/16X4
Close to U3
RA62 1K1%4
UA3B
RA61 4.99K/1%/4
(37) LINE2_L
-IN B
+IN B
OUT B
OPA1652AID_SOIC8-HF
F_LINE2_L
(37) MIC2_VREFO
MIC2_VREFO
S-BAT54A_SOT23
DA1
RA54 4.7K/4 F_MIC2_L
RA60 4.7K/4 F_MIC2_R
N31-2051411-H06
JAUD1
(37) MIC2_L
(37) MIC2_R
(37) JD3
RA53 75R F_MIC2_L
RA59 75R F_MIC2_R
F_LINE2_R RA67 100R/6 F_LINE2R
RA56 47R/4 HPON
F_LINE2_L RA50 100R/6 F_LINE2L
MIC
MICPWR
FLINE OUTR
HPON
FLINE OUTL
GND
PRESENCE#
LINE NEXT R
LINE NEXT L
H2X5[8]M_BLACK-RH
N31-2051411-H06
CA41 1000p50X4
MIC2_JD
LINE2_JD
RA57 100K1%4
RA55 200K1%4
Close to Front panel
For HDA/AC97 front cable.
Close to Jack
ESD protect
F_LINE2R D67 ESD-VAR
F_LINE2L D62 ESD-VAR
F_MIC2_R D66 ESD-VAR
F_MIC2_L D61 ESD-VAR
F_MIC2_R RA63 22K/4
F_MIC2_L RA52 22K/4
F_LINE2R RA64 22K/4
F_LINE2L RA58 22K/4
Rear Line OUT De-POP circuit
(De-pop circuit for Rear Line out & Front Headphone out)
3VSB
RA18 220K1%4
CA3 0.1u/16X4
VCC3
RA20 10K/4
RA21 0R/4
RA19 10K/4
QA5 P-3906
QA6 P-3906
CA4 22u6.3X8
MUTE
(37) EAPD
EAPD RA36 1K/4 EAPD_R
QA7 P-3906
Digital
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA,SROUT_RA, CEN_OUTA, BASSA to TVS)
QA3
MUTE RA14 1K/4 CEN_OUTA CEN_OUTA (37)
RA16 1K/4 BASSA BASSA (37)
NN-HBN2515S6R
Analog
QA2
MUTE RA11 1K/4 LOUT_LA LOUT_LA (37)
RA13 1K/4 LOUT_RA LOUT_RA (37)
NN-HBN2515S6R
QA4
MUTE RA15 1K/4 F_LINE2L
RA17 1K/4 F_LINE2R
NN-HBN2515S6R
QA1
MUTE RA10 1K/4 SROUT_LA SROUT_LA (37)
RA12 1K/4 SROUT_RA SROUT_RA (37)
NN-HBN2515S6R

Audio moat is transparent and width 40mil

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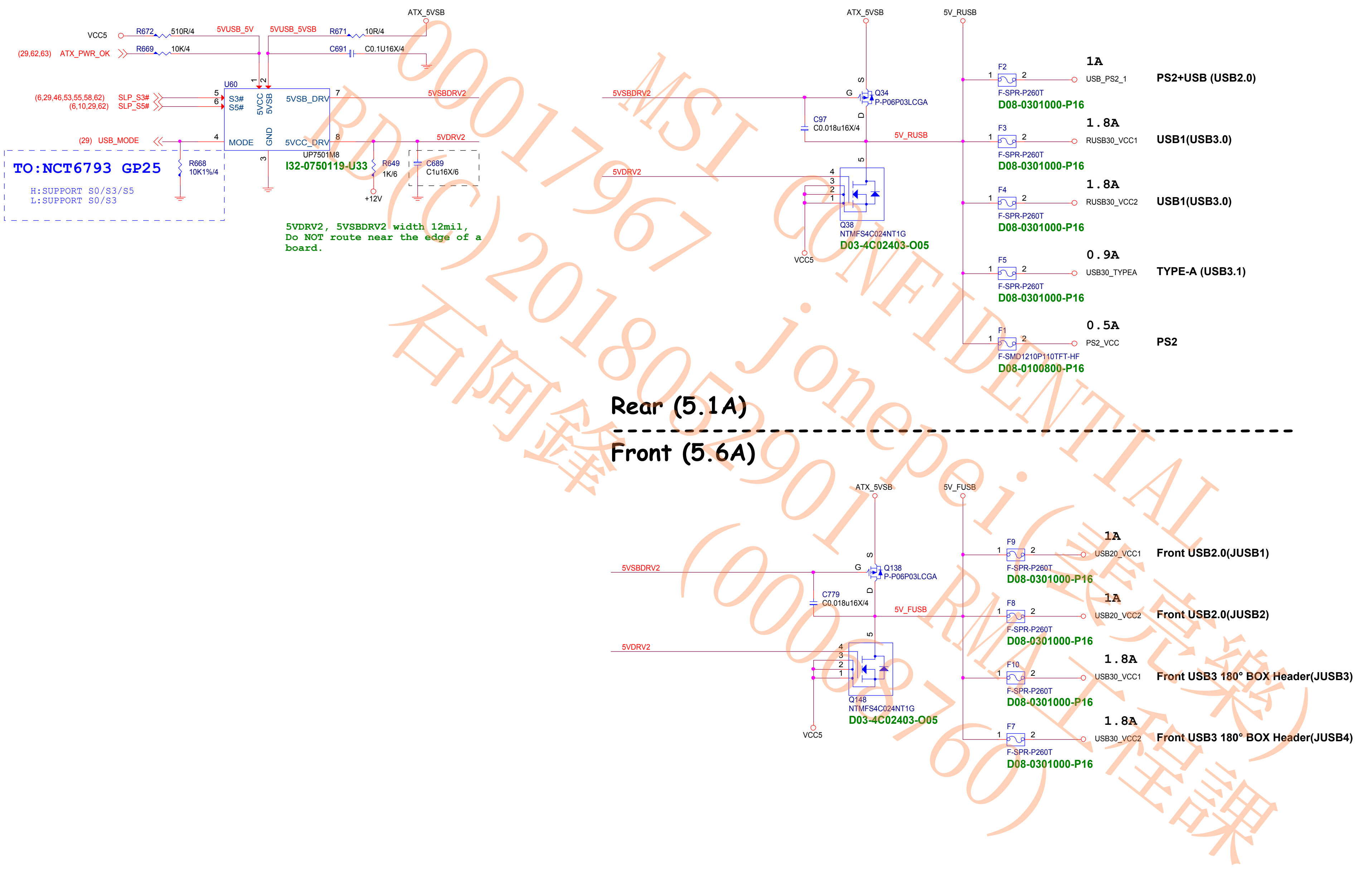
USB Power



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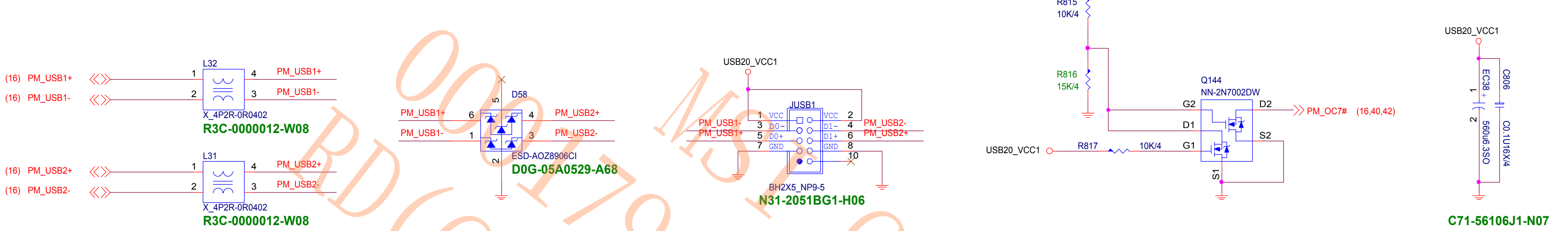
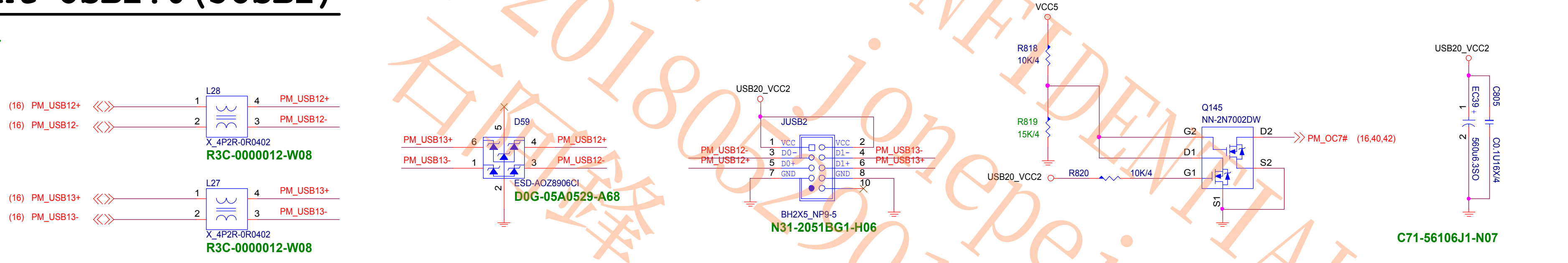
Front USB2.0(JUSB1)

5V@1A



Front USB2.0(JUSB2)

5V@1A



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: Front USB2.0 Header	Rev: 11
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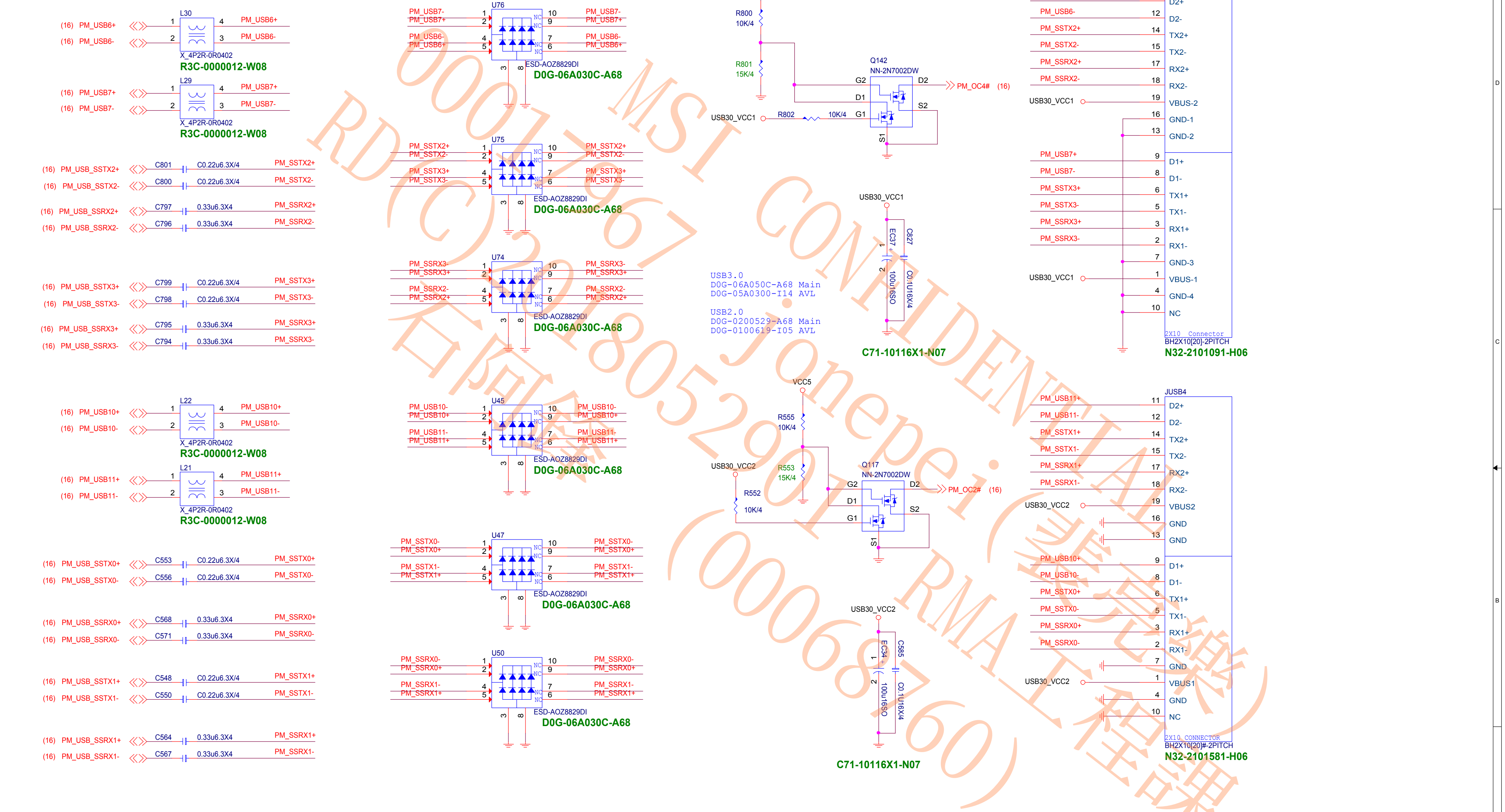
Front USB3 180° BOX Header(JUSB3)

5V@1.8A



MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size: Custom	Document Description: Front USB3.0 Header	Rev: 11
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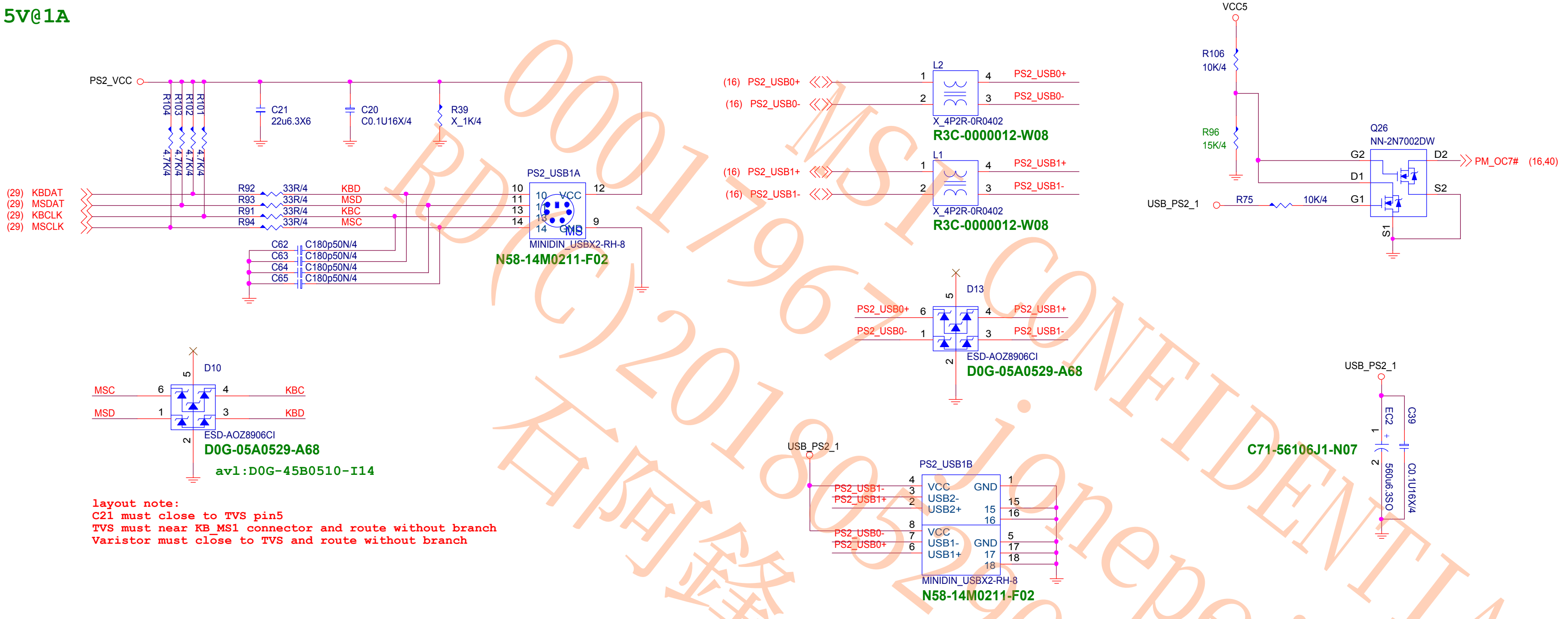
PS2+USB (USB2.0)

5V@1A



layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

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Custom	Rear USB2.0 + PS2	11

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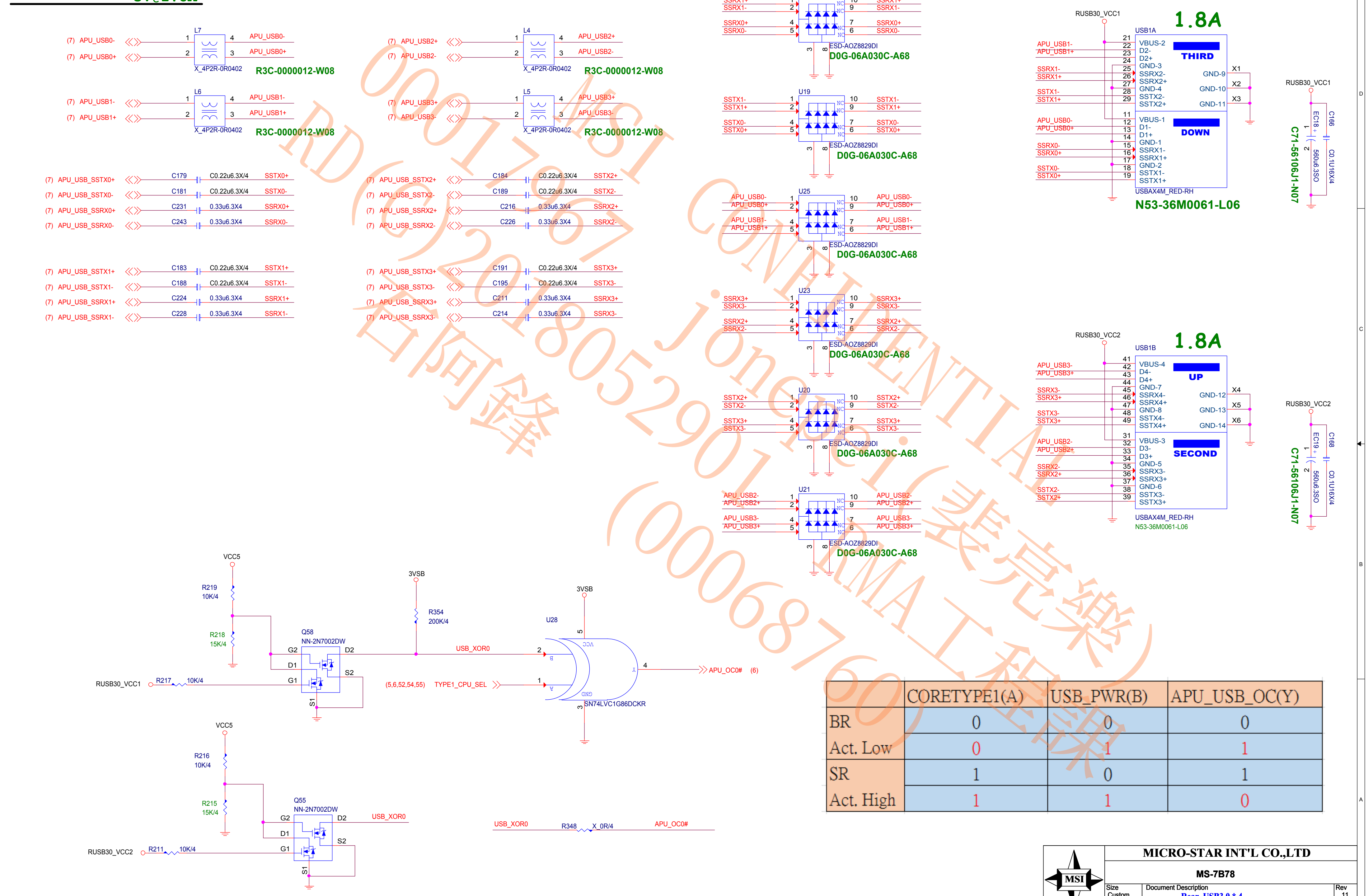
Rear USB3.0 GEN1 5V@1.8A



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

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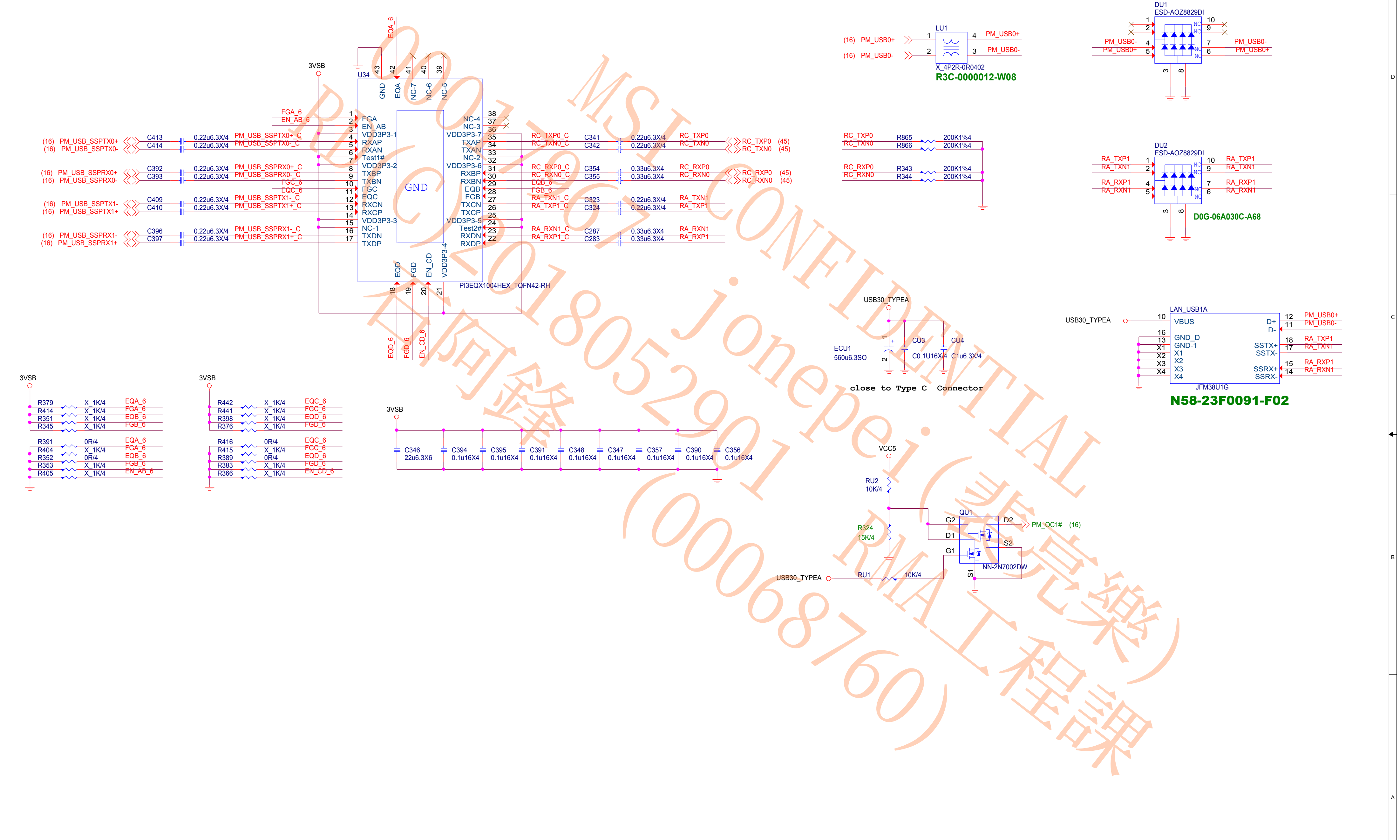
Size: Custom | Document Description: Rear_USB3.0 * 4 | Rev: 11

TYPE-A PI3EQX1004 Redriver



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Size	Document Description	Rev
Custom	Rear USB3.1 Type A / redrive	11

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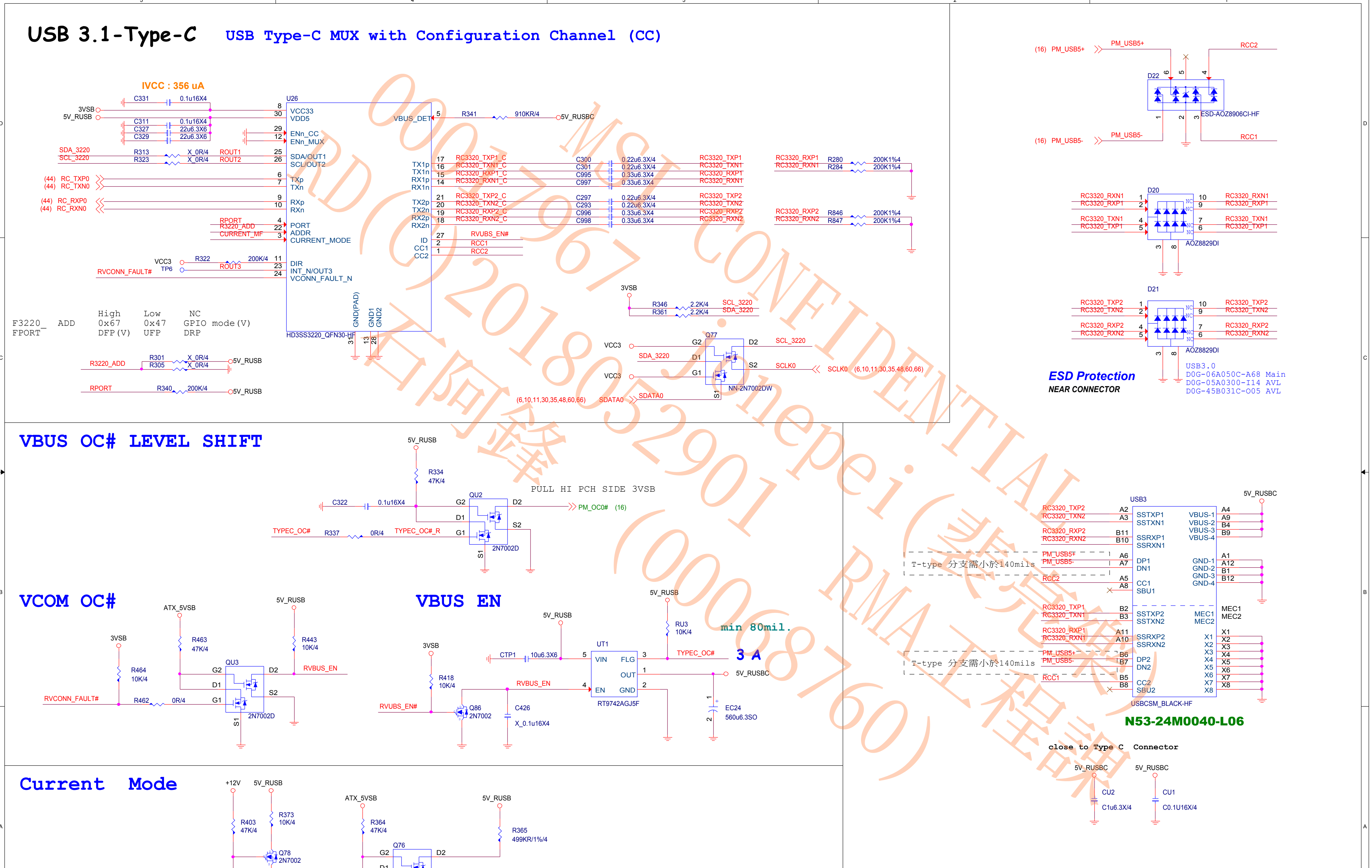

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Size	Document Description	Rev
Custom	Rear USB3.1 Type C / mux	11

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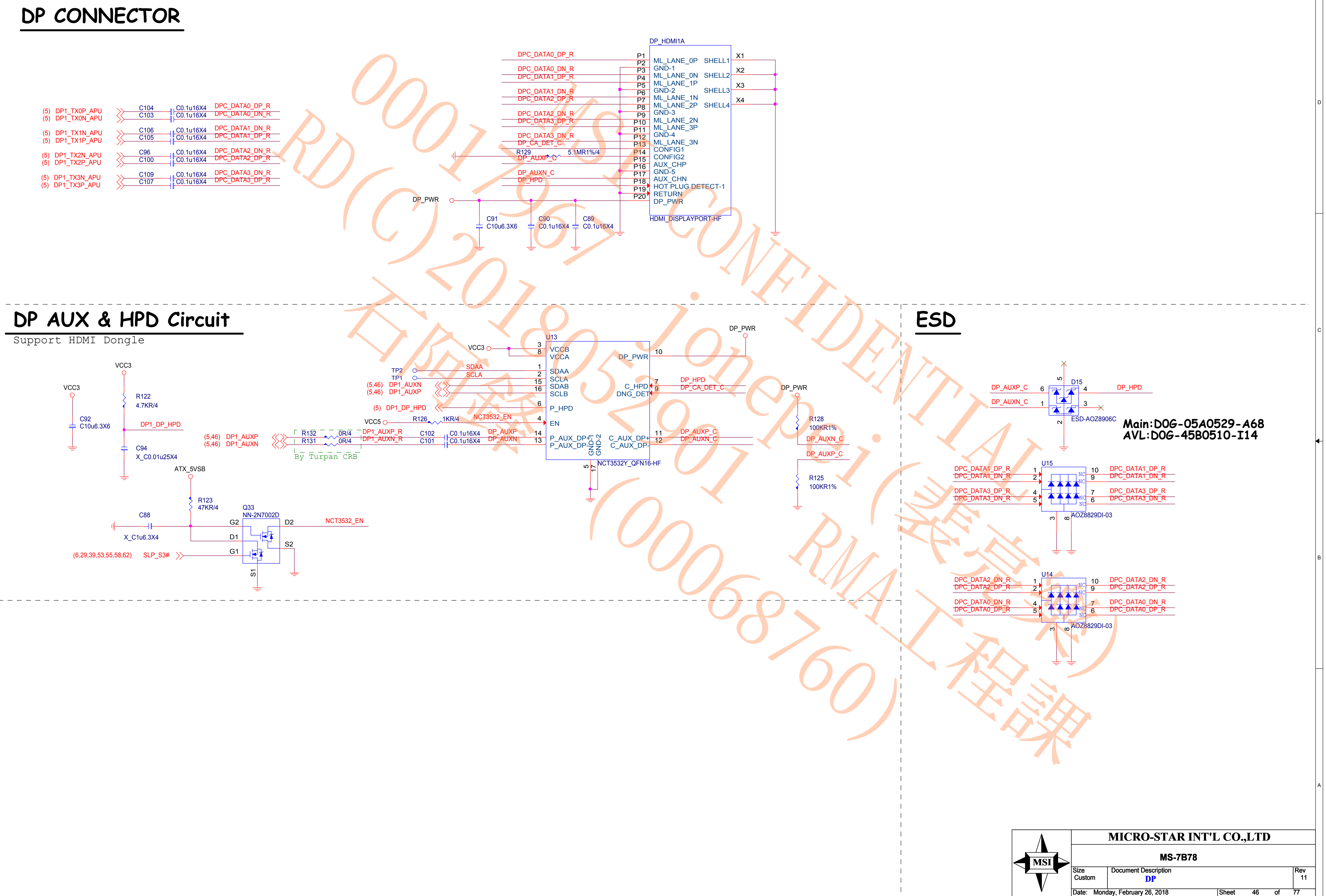

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Size	Document Description	Rev
Custom	DP	11

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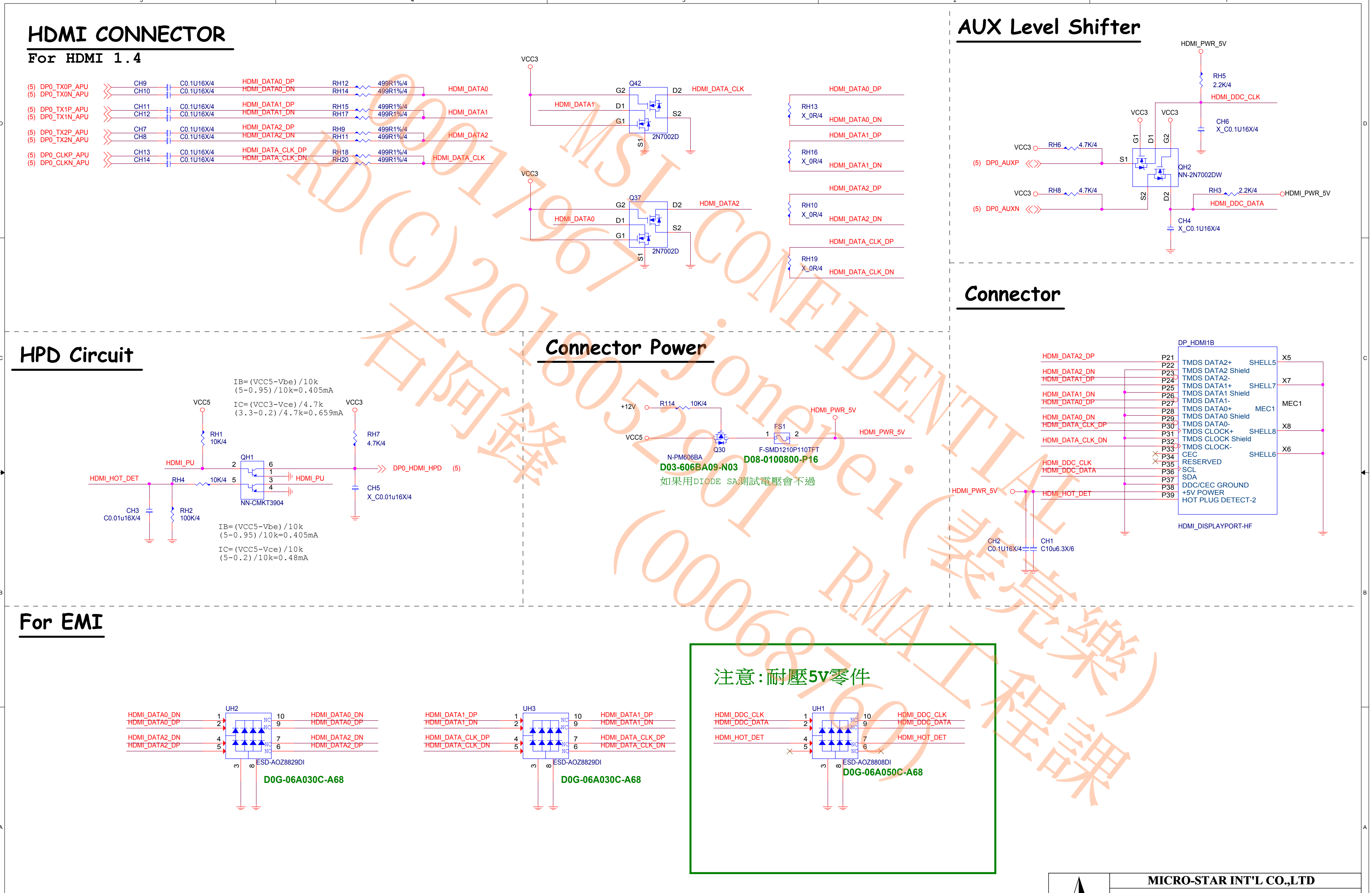

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Size	Document Description	Rev
Custom	HDMI	11

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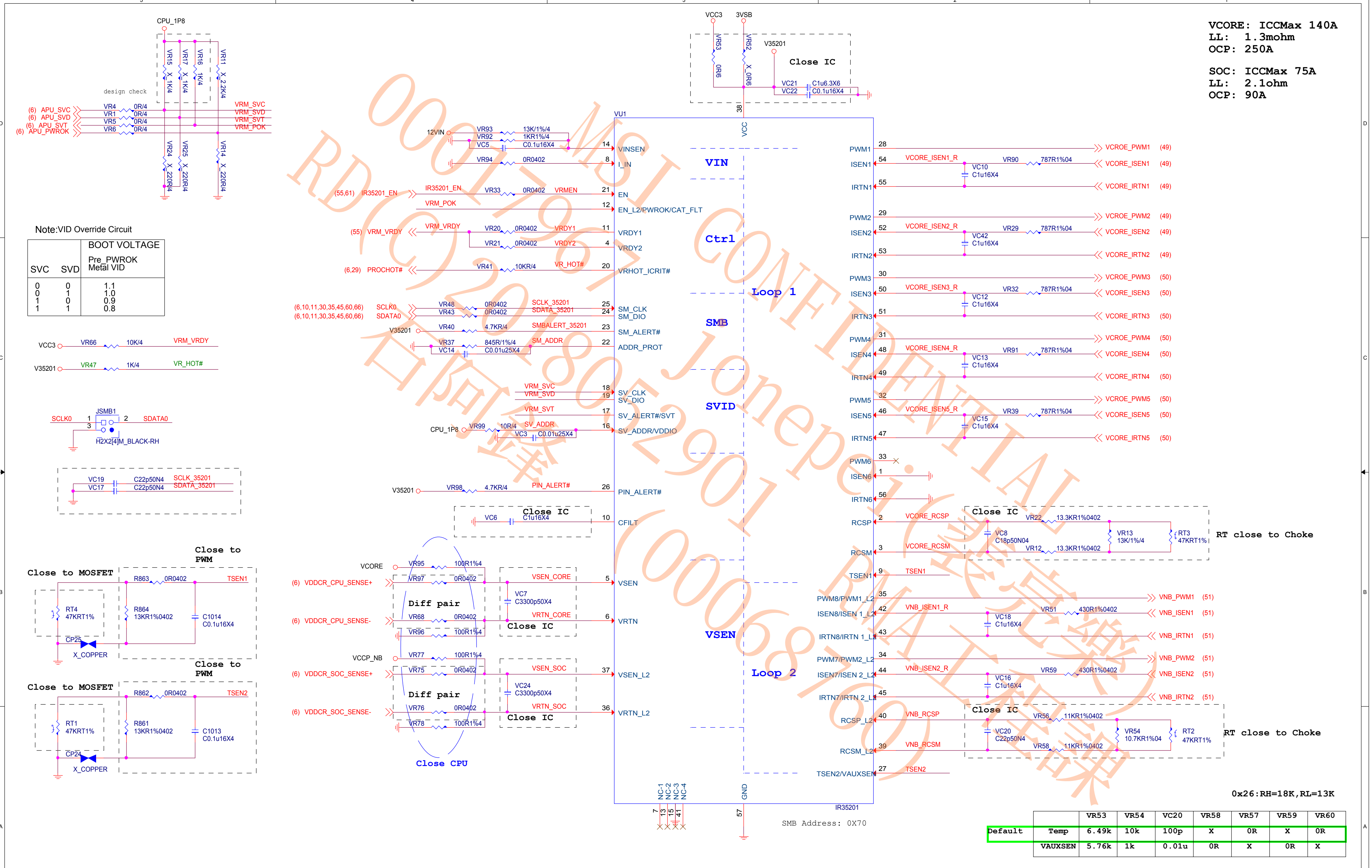

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

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Size: Custom | Document Description: CPU Power UP9505 10+2 | Rev: 11

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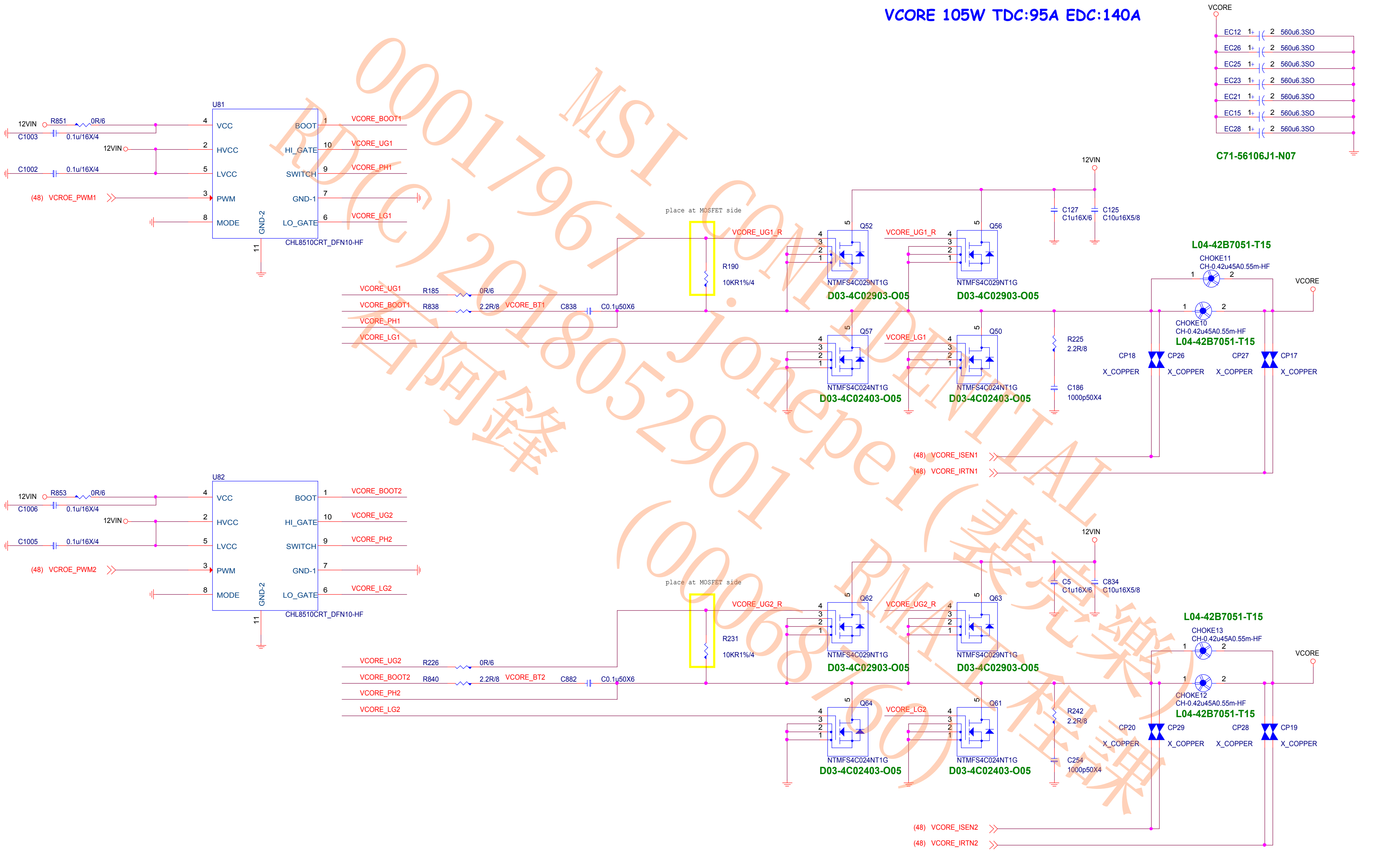

MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size: Custom	Document Description: CPU Power Phase 1 - 4	Rev: 11
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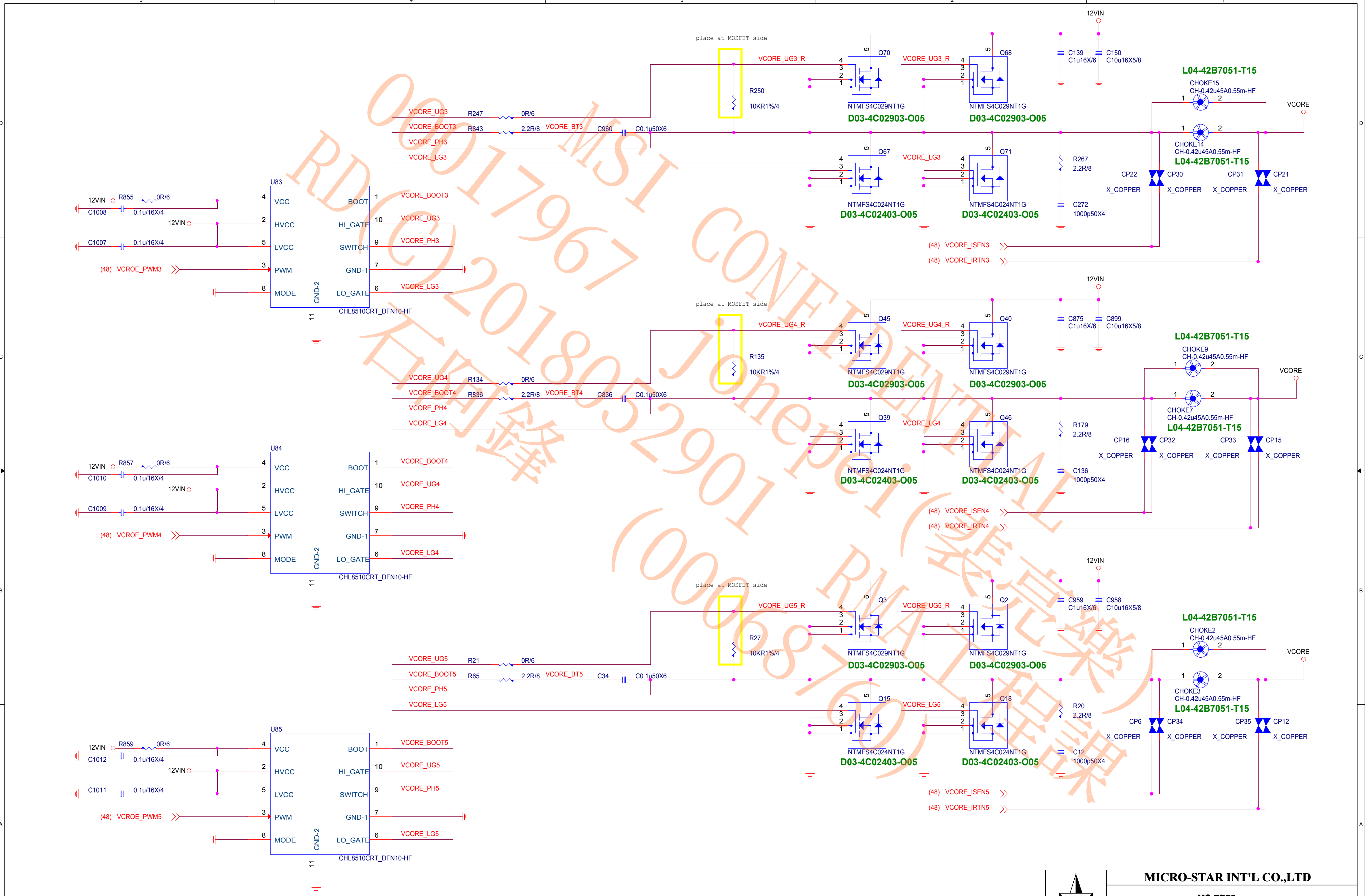

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MS-7B78

Size	Document Description	Rev
Custom	CPU Power Phase 5 - 10	11

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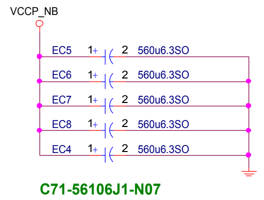
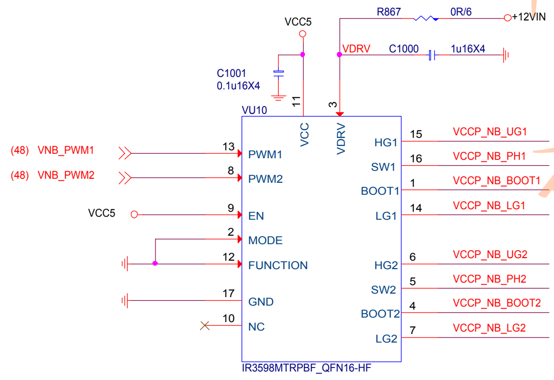
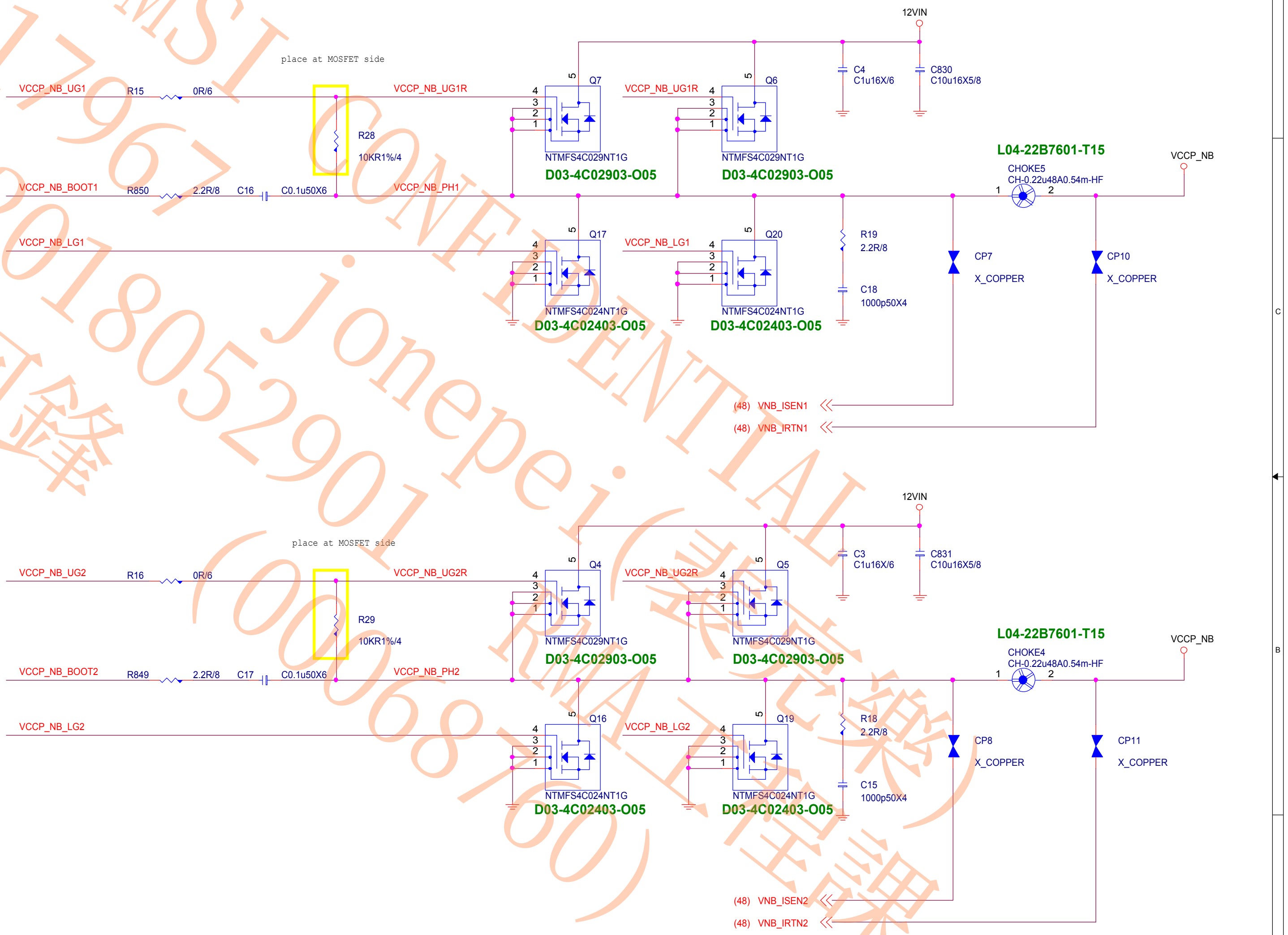
VCCP_NB 105W TDC:50A EDC:75A

Table for IR3598

Function	Mode	PWM Mode	Phase Mode	
0	1	IR ATL	Dual	
1	1	IR ATL	Doubler	
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore







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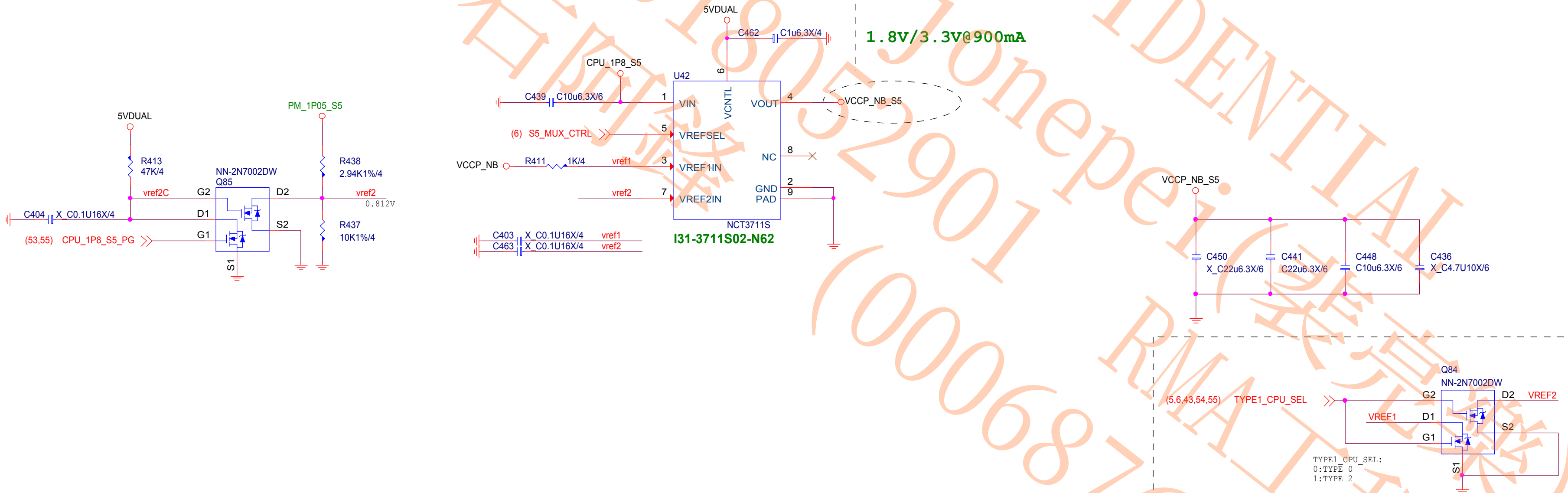
Size	Document Description	Rev
Custom	CPU Power NB 1 - 2	11

FOR VCCP_SOC_S5 0.9A

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)

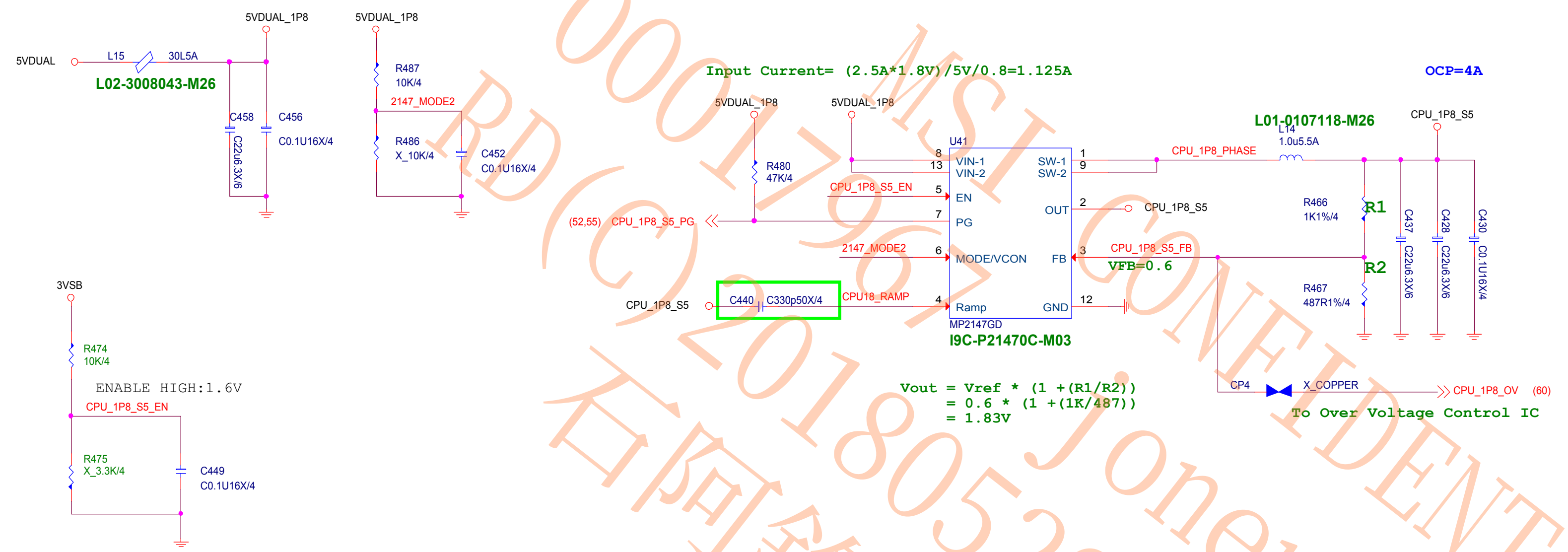


CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

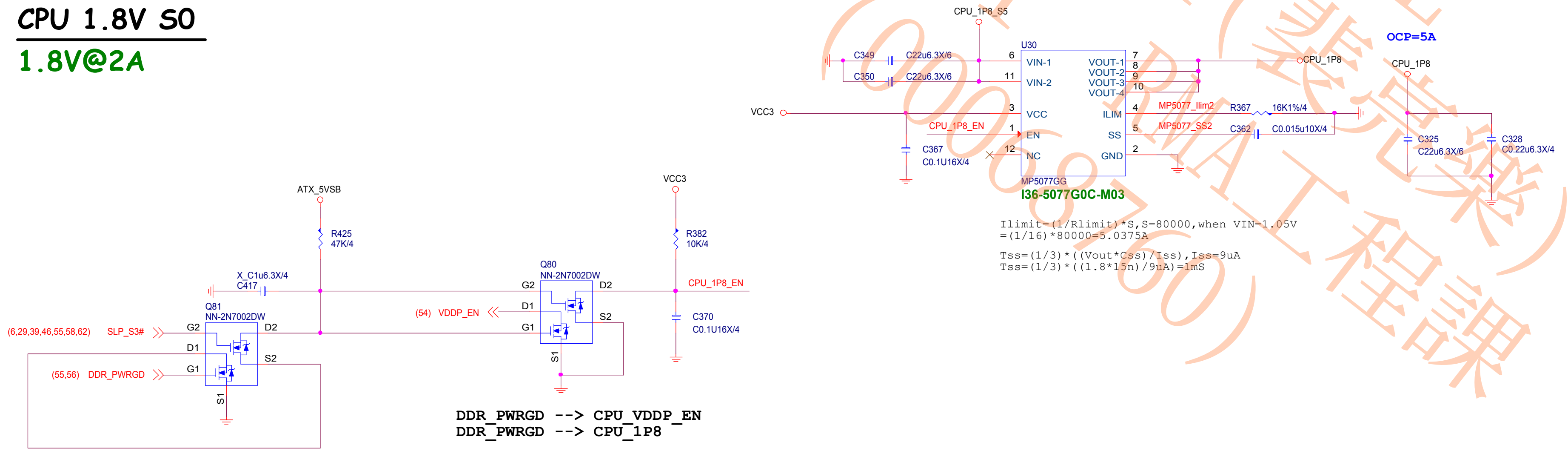
CPU 1.8V S5 @0.5A

1.8V S5@0.5A



CPU 1.8V S0

1.8V@2A



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CPU_VDDP_S0

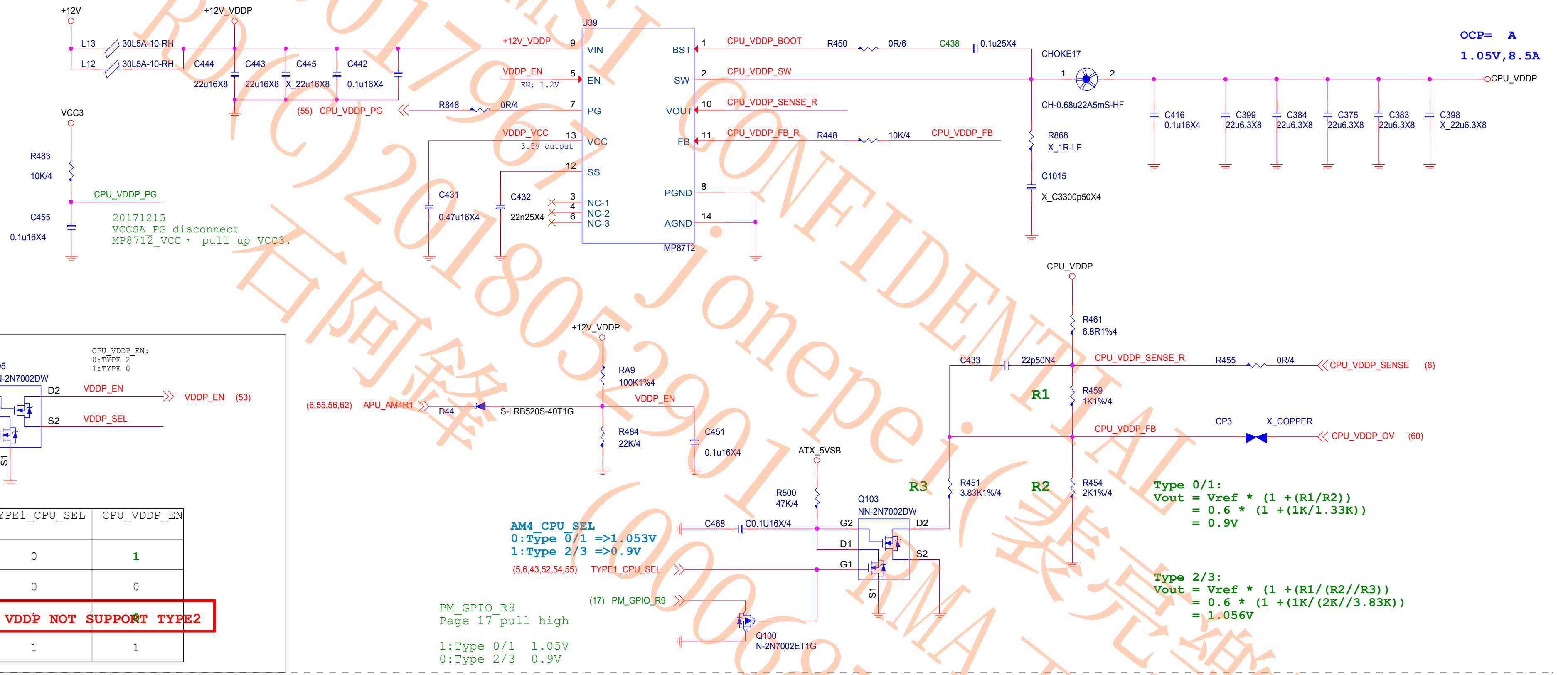
1.05V/0.9V@S0:8.5A

Input Current= (8.5A*1.05V)/12V/0.8=2.23A

S0:8.5A
S5:1A

OCP=14A

Iin=11.1A*1.05V/0.8/12V=1.21A
L02-3008043-M26
Over 85℃ ,Rated Current
1.5A.


+12V
+12V_VDDP
L13 30L5A-10-RH
L12 30L5A-10-RH
C444 22u16X8
C443 22u16X8
C445 X_22u16X8
C442 0.1u16X4
U39
+12V_VDDP 9 VIN
VDDP_EN 5 EN
EN: 1.2V
(55) CPU_VDDP_PG R848 0R/4 7 PG
VDDP_VCC 13 VCC
3.5V output
12 SS
C431 0.47u16X4
C432 22n25X4
3 NC-1
4 NC-2
6 NC-3
MP8712
BST 1 CPU_VDDP_BOOT R450 0R/6 C438 0.1u25X4
SW 2 CPU_VDDP_SW
VOUT 10 CPU_VDDP_SENSE_R
FB 11 CPU_VDDP_FB_R R448 10K/4 CPU_VDDP_FB
PGND 8
AGND 14
CHOKE17
CH-0.68u22A5mS-HF
R868 X_1R-LF
C1015 X_C3300p50X4
C416 0.1u16X4
C399 22u6.3X8
C384 22u6.3X8
C375 22u6.3X8
C383 22u6.3X8
C398 X_22u6.3X8
OCP= A
1.05V,8.5A
CPU_VDDP
VCC3
R483 10K/4
CPU_VDDP_PG
C455 0.1u16X4
20171215
VCCSA_PG disconnect
MP8712_VCC , pull up VCC3.
TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2
CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0
Q95 NN-2N7002DW
(6,7,55) TYPE0_CPU_SEL G2 D2 VDDP_EN VDDP_EN (53)
VDDP_SEL D1
(5,6,43,52,54,55) TYPE1_CPU_SEL G1 S2 VDDP_SEL
S1
TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2
+12V_VDDP
RA9 100K1%4
VDDP_EN
(6,55,56,62) APU_AM4R1 D44 S-LRB520S-40T1G
R484 22K/4
C451 0.1u16X4
CPU_VDDP
R461 6.8R1%4
C433 22p50N4
CPU_VDDP_SENSE_R R455 0R/4 CPU_VDDP_SENSE (6)
R1
R459 1K1%/4
CPU_VDDP_FB
CP3 X_COPPER CPU_VDDP_OV (60)
ATX_5VSB
R500 47K/4
Q103 NN-2N7002DW
C468 C0.1U16X/4
R3
R451 3.83K1%/4
R2
R454 2K1%/4
AM4_CPU_SEL
0:Type 0/1 =>1.053V
1:Type 2/3 =>0.9V
(5,6,43,52,54,55) TYPE1_CPU_SEL
(17) PM_GPIO_R9
Q100 N-2N7002ET1G
PM_GPIO_R9
Page 17 pull high
1:Type 0/1 1.05V
0:Type 2/3 0.9V
Type 0/1:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/1.33K))
= 0.9V
Type 2/3:
Vout = Vref * (1 +(R1/(R2//R3))
= 0.6 * (1 +(1K/(2K//3.83K))
= 1.056V

CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	1
NA		0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	0
RV/ZP	3	0	1	1

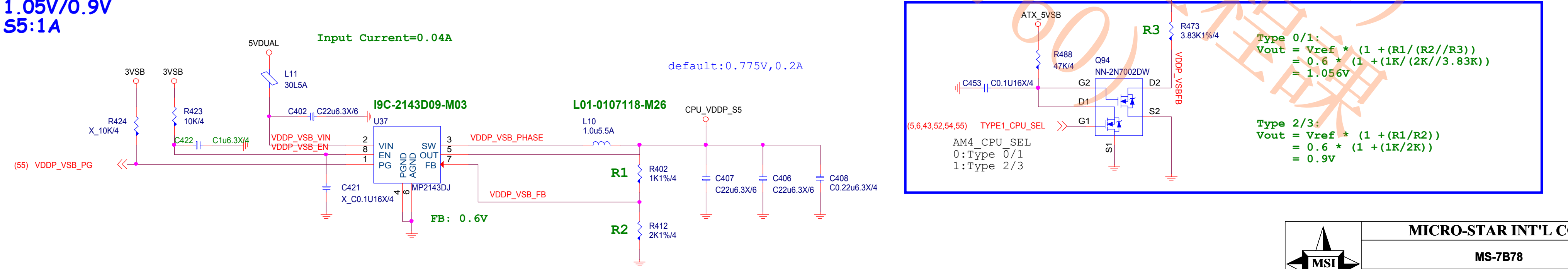
CPU_VDDP_S5

(VDDCR_SOC_S5)

1.05V/0.9V
S5:1A

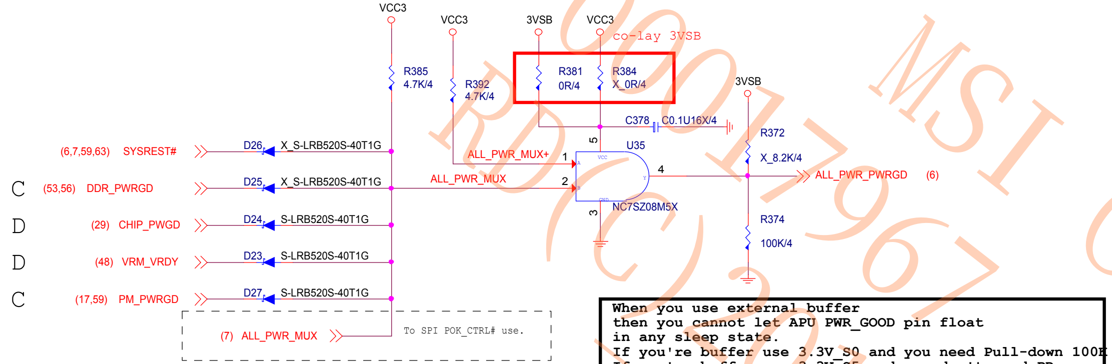
Input Current=0.04A

default:0.775V,0.2A


5VDUAL
3VSB
3VSB
L11 30L5A
R424 X_10K/4
R423 10K/4
C422 C1u6.3X/4
C402 C22u6.3X/6
I9C-2143D09-M03
U37
VDDP_VSB_VIN 2 VIN
VDDP_VSB_EN 8 EN
1 PG
PGND AGND
SW 3 VDDP_VSB_PHASE
OUT 5
FB 7
MP2143DJ
(55) VDDP_VSB_PG
C421 X_C0.1U16X/4
L01-0107118-M26
L10 1.0u5.5A
CPU_VDDP_S5
R1 R402 1K1%/4
R2 R412 2K1%/4
VDDP_VSB_FB
FB: 0.6V
C407 C22u6.3X/6
C406 C22u6.3X/6
C408 C0.22u6.3X/4
VDDP_VSB_FB
ATX_5VSB
R3 R473 3.83K1%/4
R488 47K/4
Q94 NN-2N7002DW
C453 C0.1U16X/4
VDDP_VSBFB
(5,6,43,52,54,55) TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3
Type 0/1:
Vout = Vref * (1 +(R1/(R2//R3))
= 0.6 * (1 +(1K/(2K//3.83K))
= 1.056V
Type 2/3:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/2K))
= 0.9V

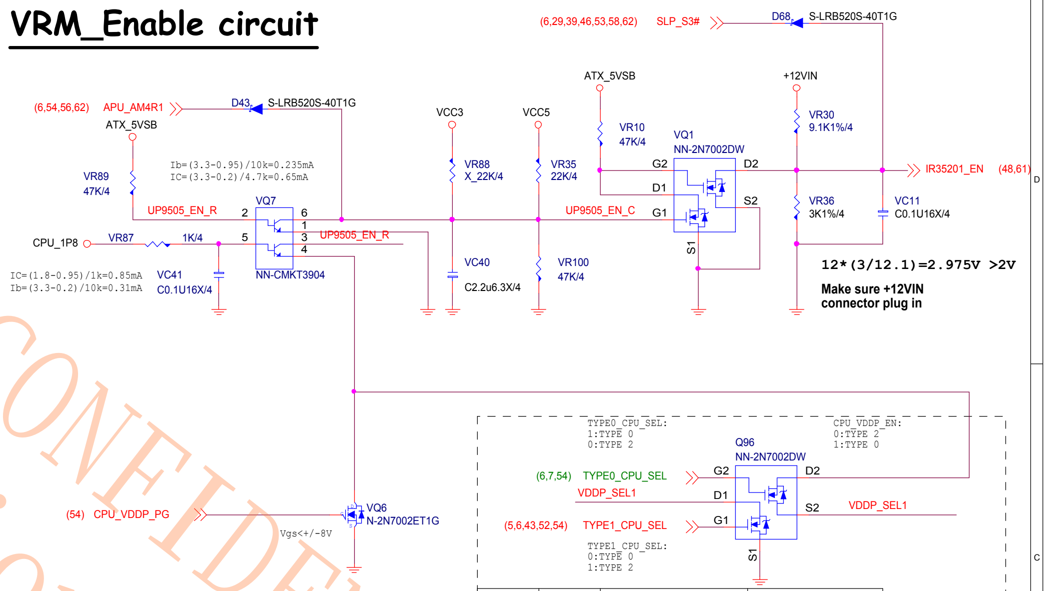
ALL POWER GOOD MUX

S0 PG



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

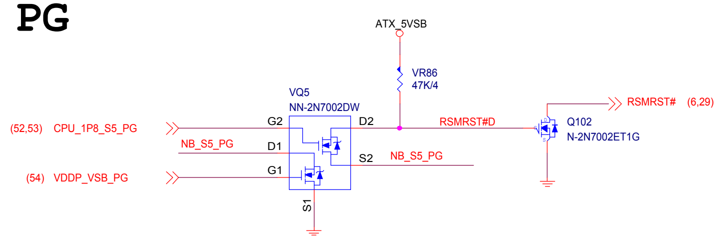
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

S5 PG



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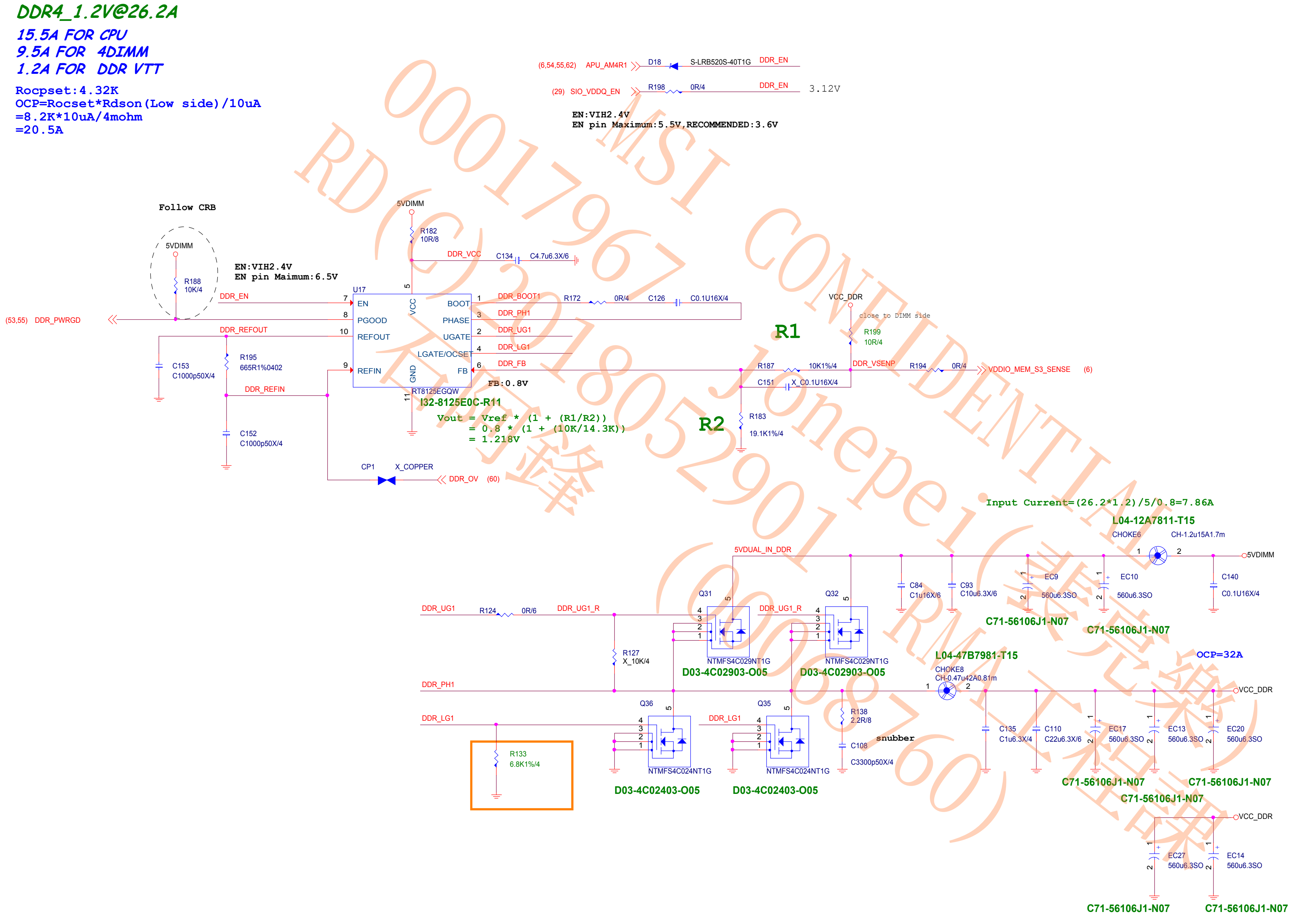

DDR4_1.2V@26.2A
15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT
Rocpset:4.32K
OCP=Rocset*Rdson(Low side)/10uA
=8.2K*10uA/4mohm
=20.5A
(6,54,55,62) APU_AM4R1
D18 S-LRB520S-40T1G DDR_EN
(29) SIO_VDDQ_EN
R198 0R/4 DDR_EN 3.12V
EN:VIH2.4V
EN pin Maximum:5.5V,RECOMMENDED:3.6V
Follow CRB
5VDIMM
R188 10K/4
EN:VIH2.4V
EN pin Maimum:6.5V
(53,55) DDR_PWRGD
DDR_EN
DDR_REFOUT
R182 10R/8
DDR_VCC
C134 C4.7u6.3X/6
U17
EN PGOOD REFOUT REFIN VCC GND BOOT PHASE UGATE LGATE/OCSET FB
RT8125EGQW
I32-8125E0C-R11
DDR_BOOT1 R172 0R/4 C126 C0.1U16X/4
DDR_PH1 DDR_UG1 DDR_LG1 DDR_FB
FB:0.8V
C153 C1000p50X/4
R195 665R1%0402
DDR_REFIN
C152 C1000p50X/4
Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/14.3K))
= 1.218V
CP1 X_COPPER DDR_OV (60)
VCC_DDR
close to DIMM side
R1
R199 10R/4
R187 10K1%/4
DDR_VSENP
R194 0R/4 VDDIO_MEM_S3_SENSE (6)
C151 X_C0.1U16X/4
R2
R183 19.1K1%/4
Input Current=(26.2*1.2)/5/0.8=7.86A
L04-12A7811-T15
CHOKE6 CH-1.2u15A1.7m
5VDIMM
5VDUAL_IN_DDR
C84 C1u16X/6
C93 C10u6.3X/6
EC9 560u6.3SO
EC10 560u6.3SO
C140 C0.1U16X/4
C71-56106J1-N07
C71-56106J1-N07
DDR_UG1 R124 0R/6 DDR_UG1_R
Q31 Q32
DDR_UG1_R
R127 X_10K/4
NTMFS4C029NT1G NTMFS4C029NT1G
D03-4C02903-O05 D03-4C02903-O05
L04-47B7981-T15
CHOKE8 CH-0.47u42A0.81m
OCP=32A
VCC_DDR
DDR_PH1
DDR_LG1
Q36 Q35
DDR_LG1
R133 6.8K1%/4
R138 2.2R/8
C108 C3300p50X/4
snubber
NTMFS4C024NT1G NTMFS4C024NT1G
D03-4C02403-O05 D03-4C02403-O05
C135 C1u6.3X/4
C110 C22u6.3X/6
EC17 560u6.3SO
EC13 560u6.3SO
EC20 560u6.3SO
C71-56106J1-N07
C71-56106J1-N07
C71-56106J1-N07
VCC_DDR
EC27 560u6.3SO
EC14 560u6.3SO
C71-56106J1-N07
C71-56106J1-N07

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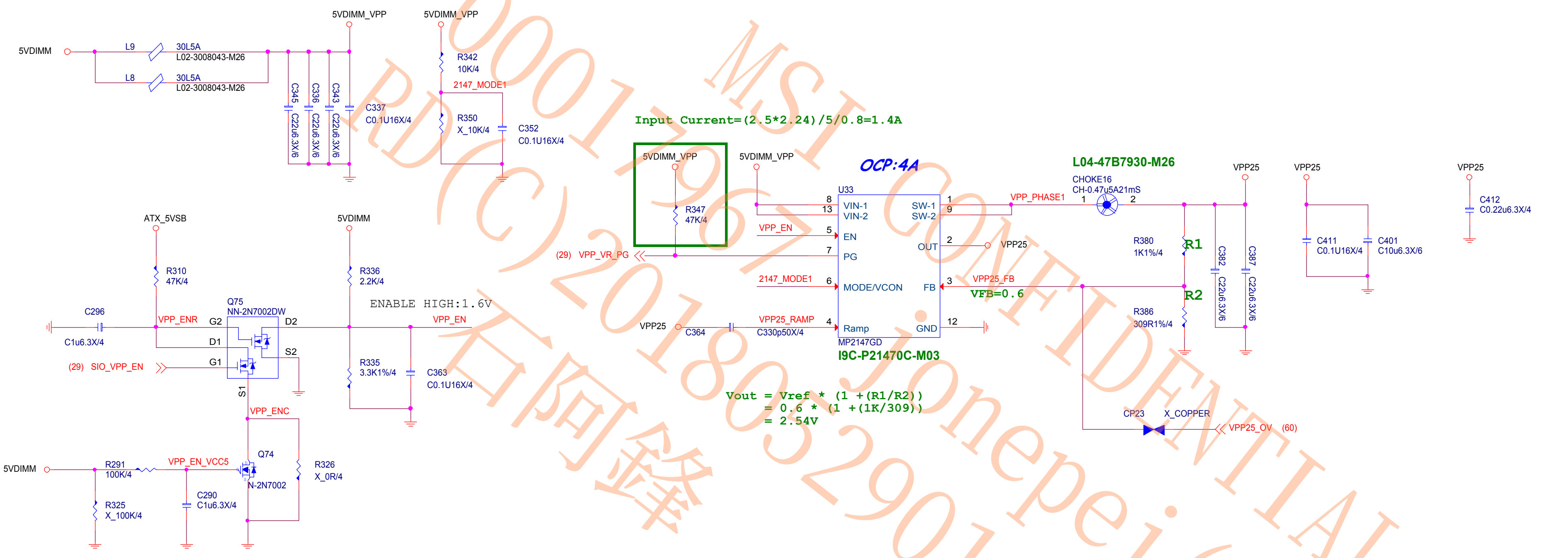
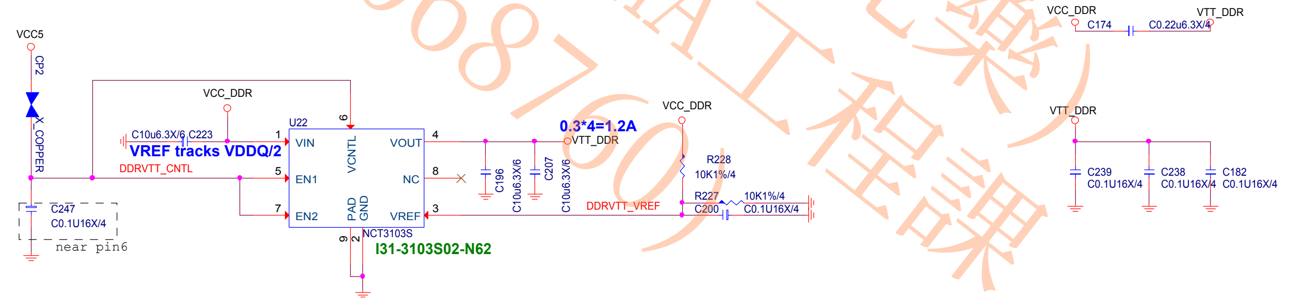
4DIMM : VPP25

2.5V@2.24A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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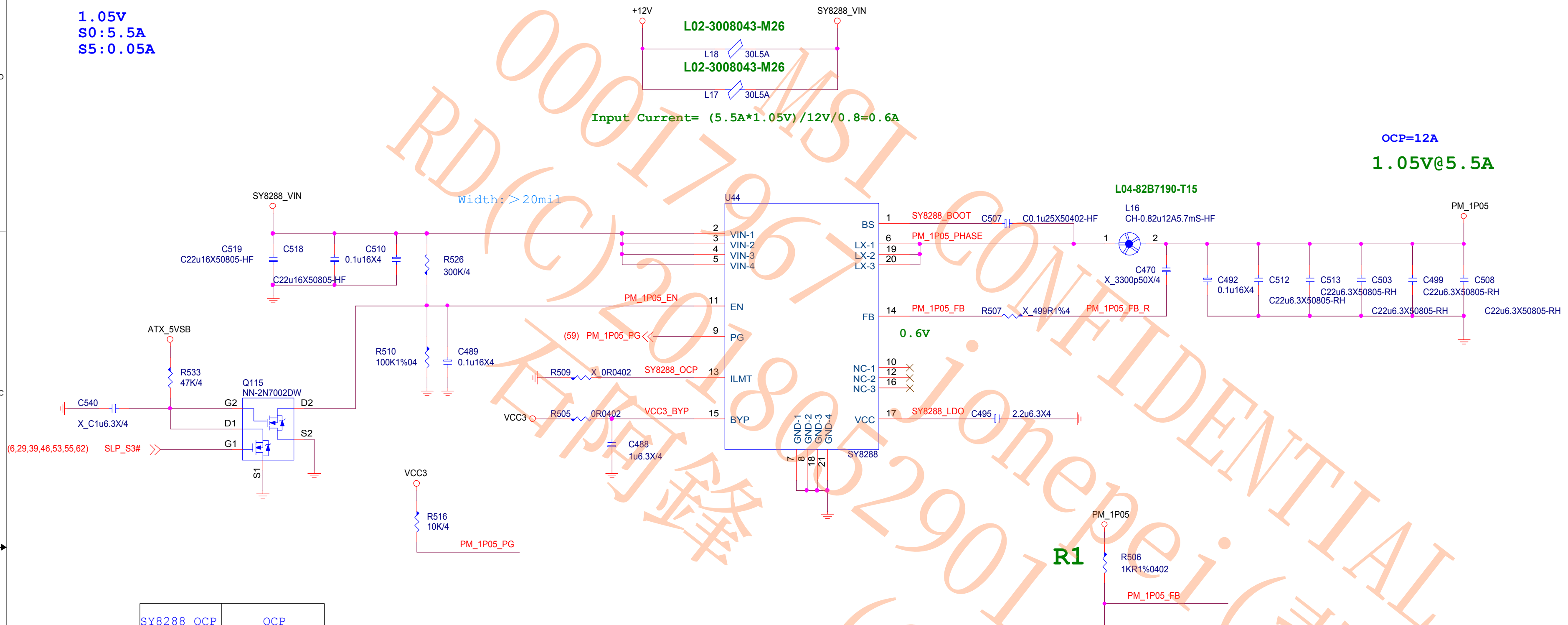
FOR Promontory 1.05V_S0

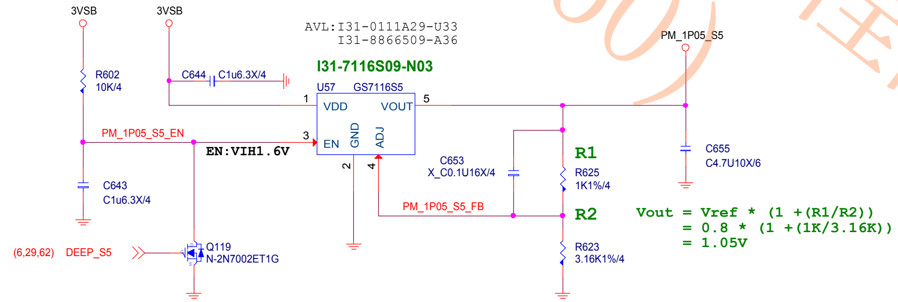
1.05V
S0:5.5A
S5:0.05A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

FOR Promontory 1.05V_S5

1.05V@0.05A



MICRO-STAR INT'L CO.,LTD

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Custom	PROM - SY8288RAC / 1.05V	11

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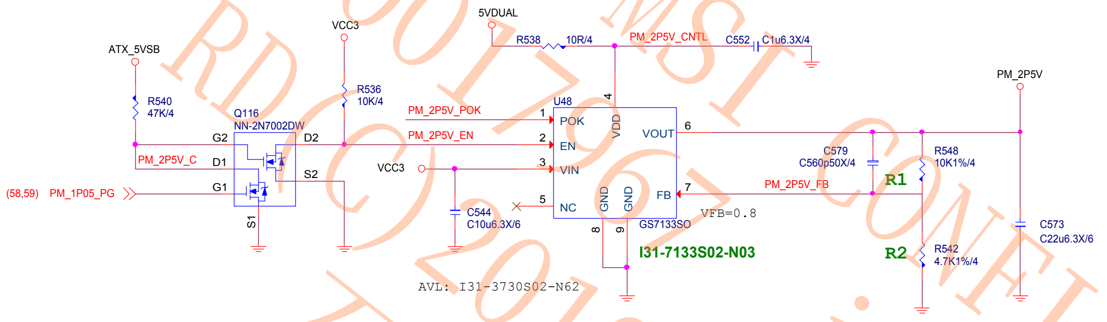
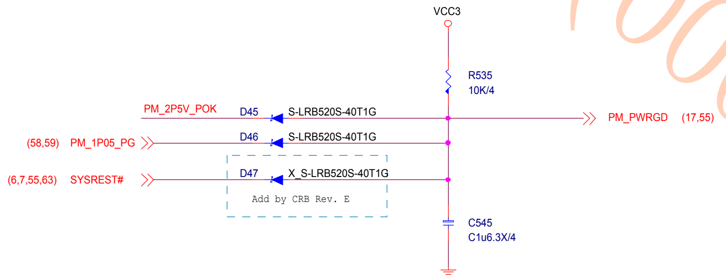
Promontory-2.5V

2.5V@900mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V



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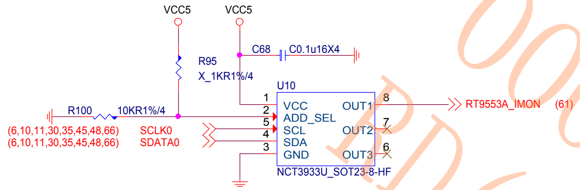
Over Voltage Control IC

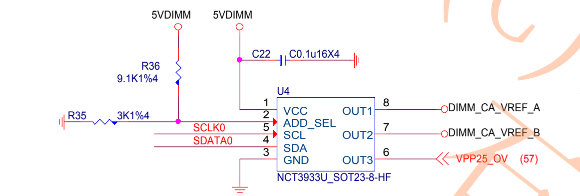
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

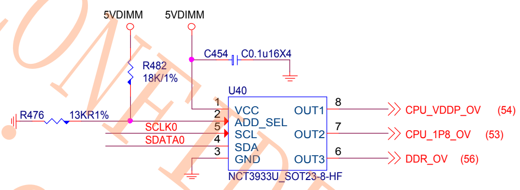
0x2A:RH=OPEN,RL=10K



0x28:RH=9.1K,RL=3K



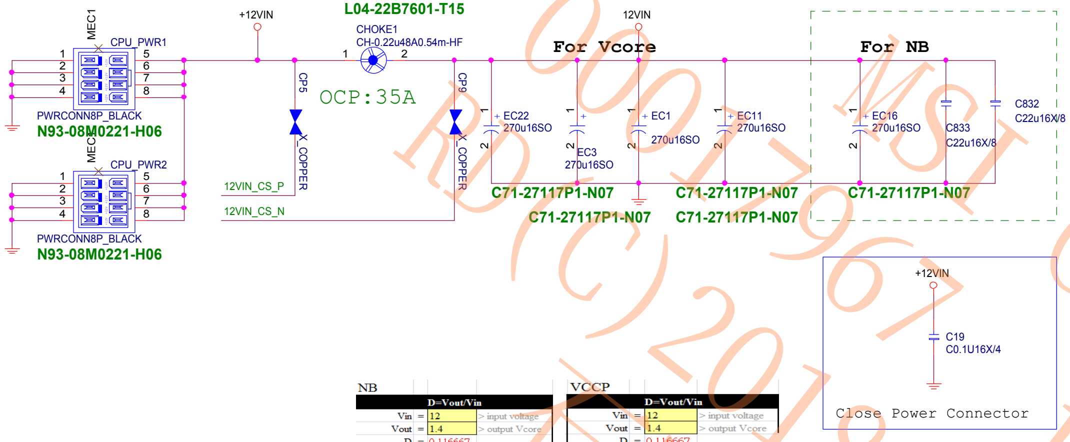
0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

CPU POWER CONNECTOR



NB

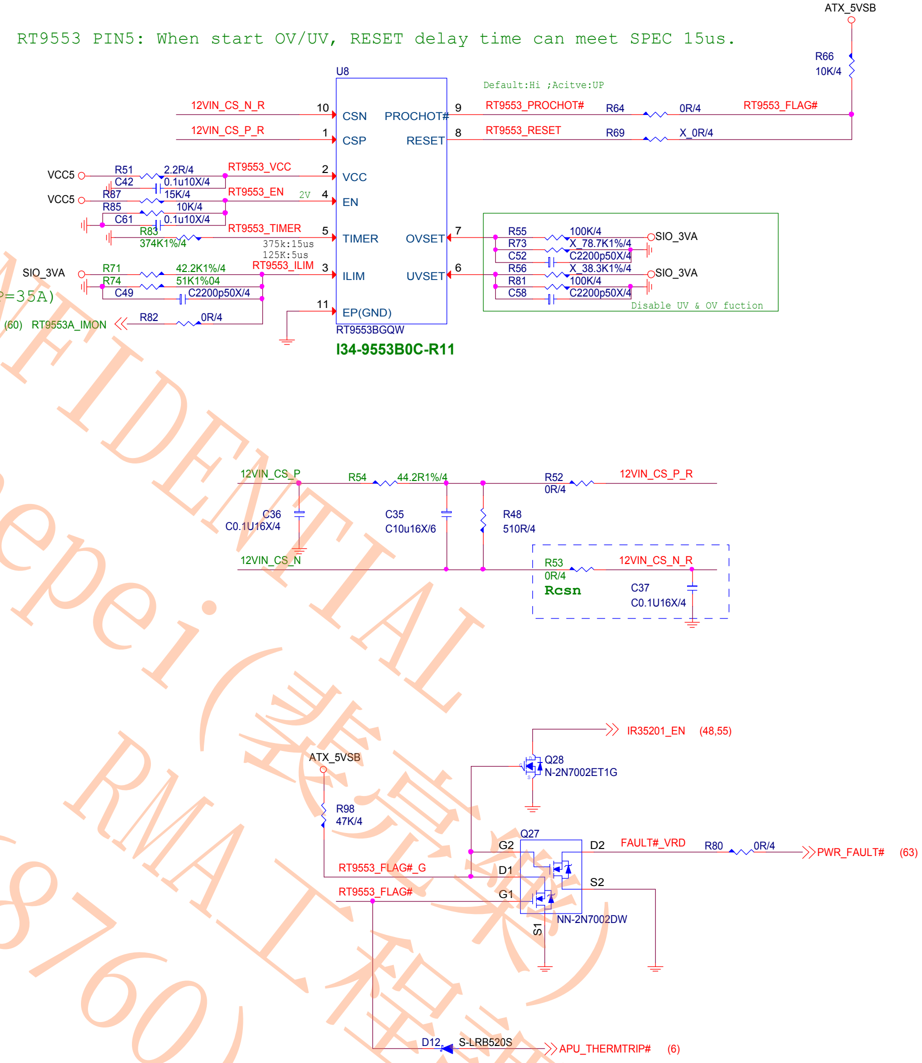
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.4	> output Vcore
D	=	0.116667	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	75	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	12.03835	A
How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

VCCP

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.4	> output Vcore
D	=	0.116667	
I o = Icore(max)*0.8			
I core(max)	=	125	> Vcore current
I avg.	=	125	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	4	phase
I ripple	=	10.03196	A
How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B78	
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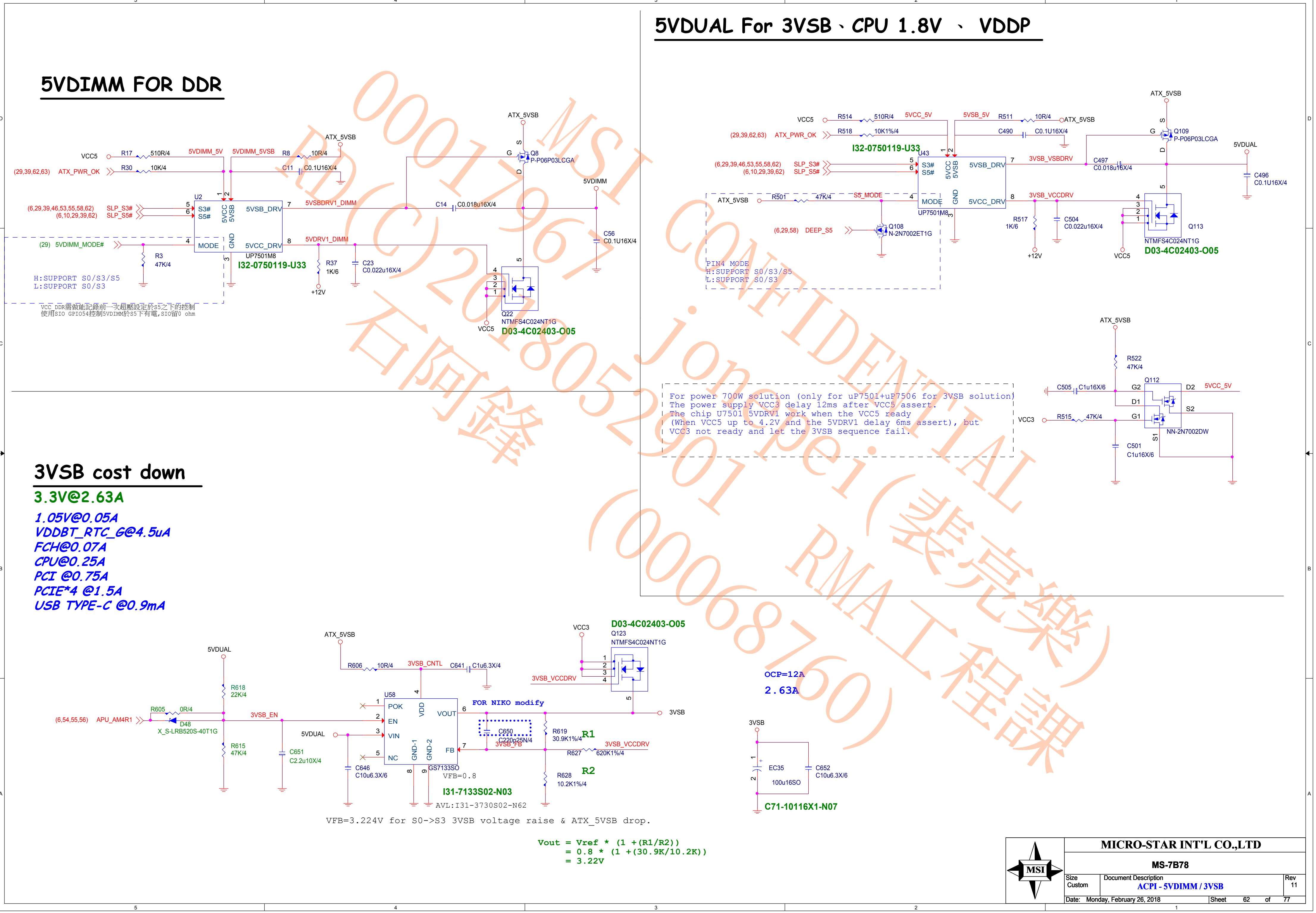
5VDUAL For 3VSB、CPU 1.8V 、 VDDP
5VDIMM FOR DDR
3VSB cost down
3.3V@2.63A
1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
PCI @0.75A
PCIE*4 @1.5A
USB TYPE-C @0.9mA
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
VCC_DDR需做能記錄前一次超壓設定於S5之下的控制
使用SIO GPIO54控制5VDIMM於S5下有電,SIO留0 ohm
I32-0750119-U33
D03-4C02403-O05
PIN4 MODE
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
FOR NIKO modify
OCP=12A
2.63A
I31-7133S02-N03
AVL:I31-3730S02-N62
C71-10116X1-N07
VFB=0.8
VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.
Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(30.9K/10.2K))
= 3.22V
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MS-7B78
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Document Description ACPI - 5VDIMM / 3VSB
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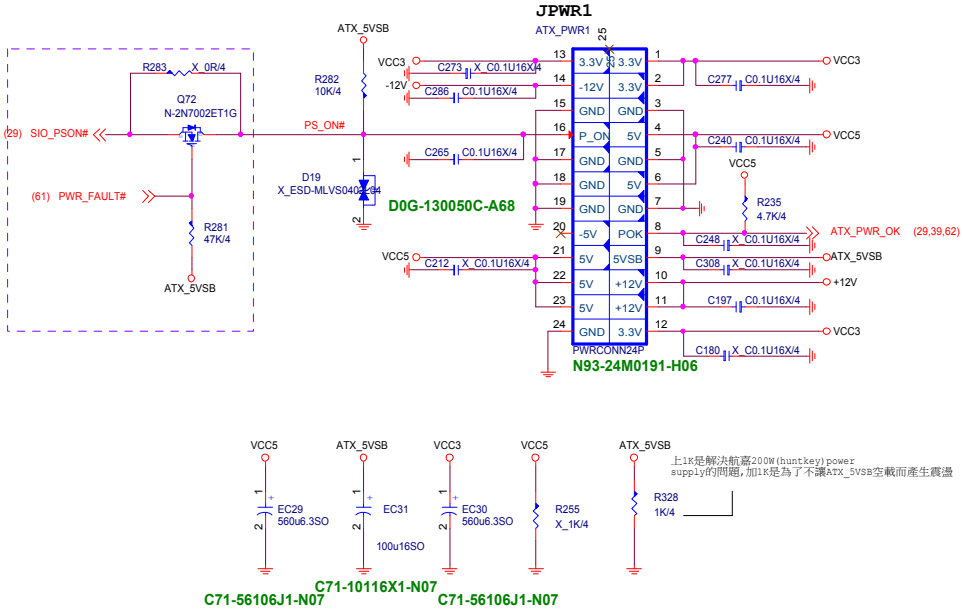
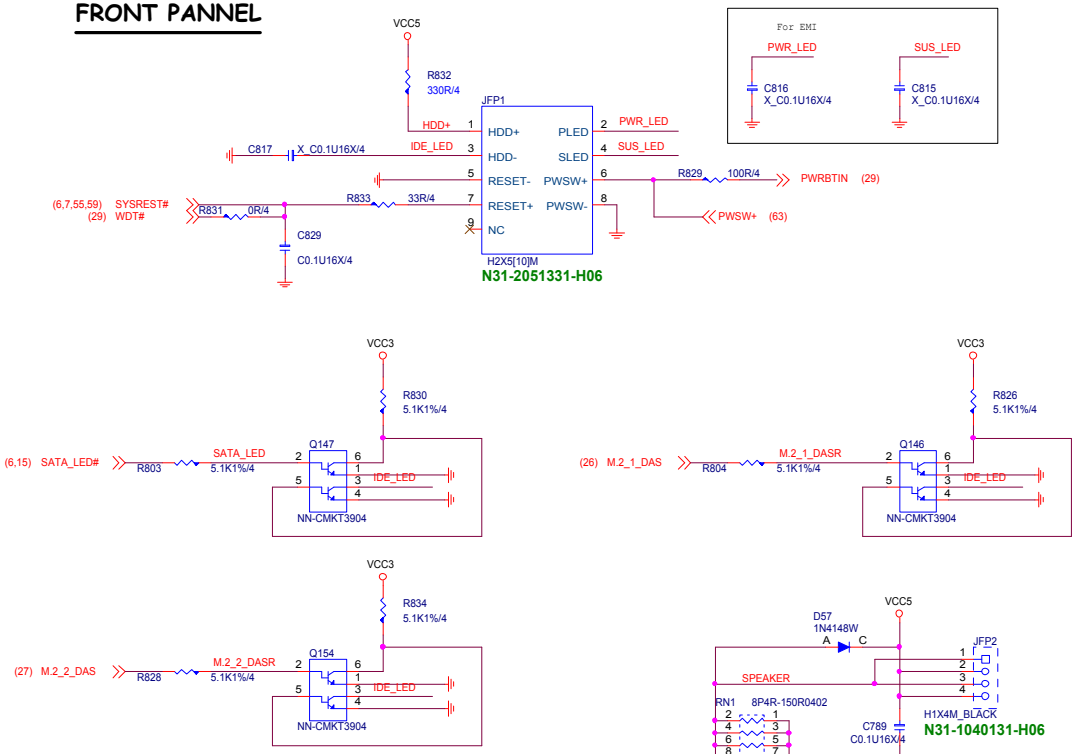
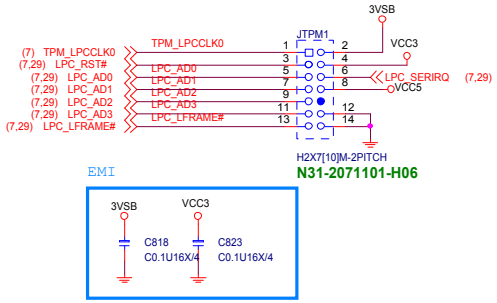
ATX POWER CONNECTOR



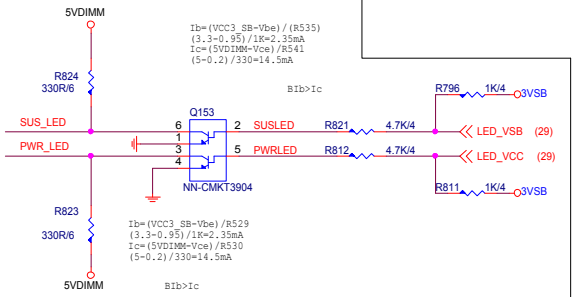
FRONT PANNEL



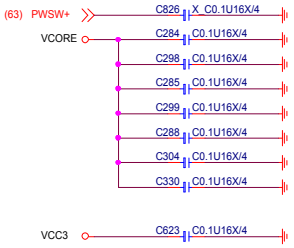
TPM



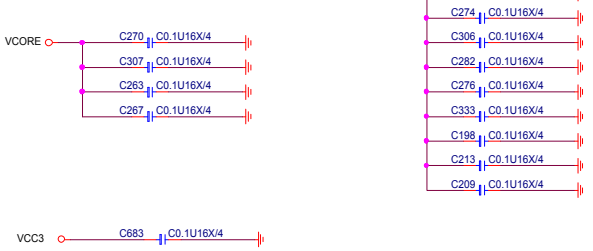
LED (for NCT6793D)



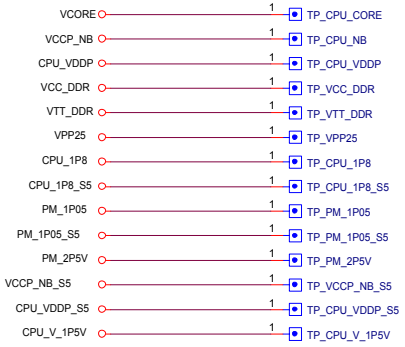
Add for EMI



return path



Voltage Mearsure Point



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MS-7B78		
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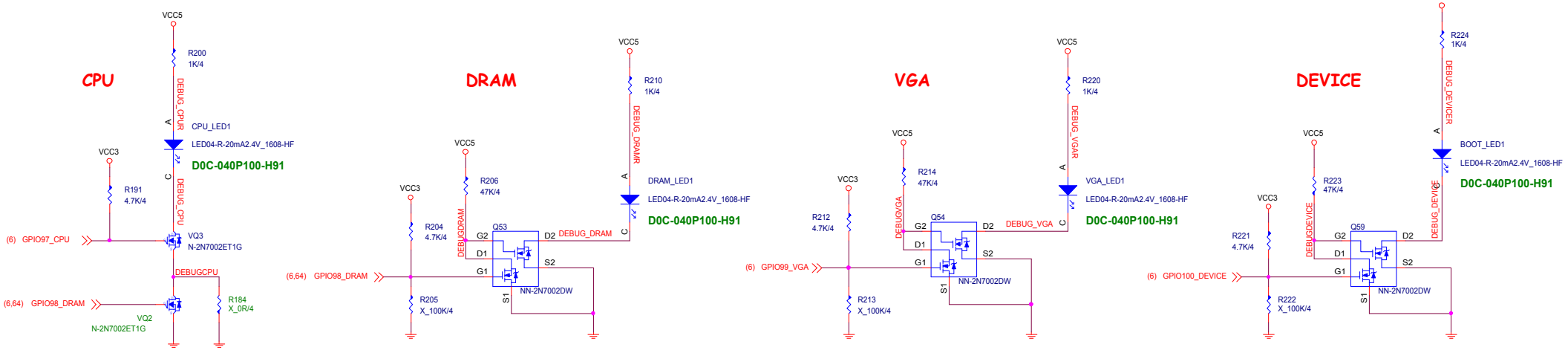
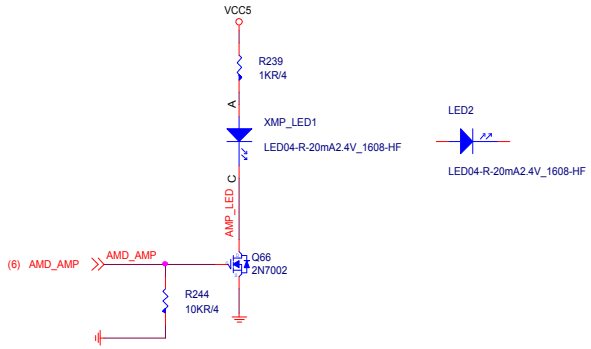
EZ Debug LED



LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

AMD AMP Detect LED



MICRO-STAR INT'L CO.,LTD

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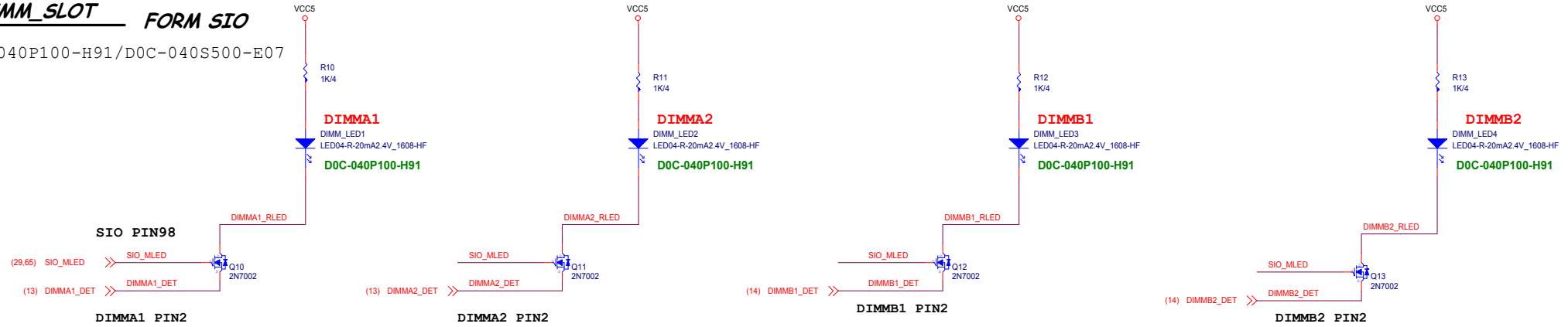
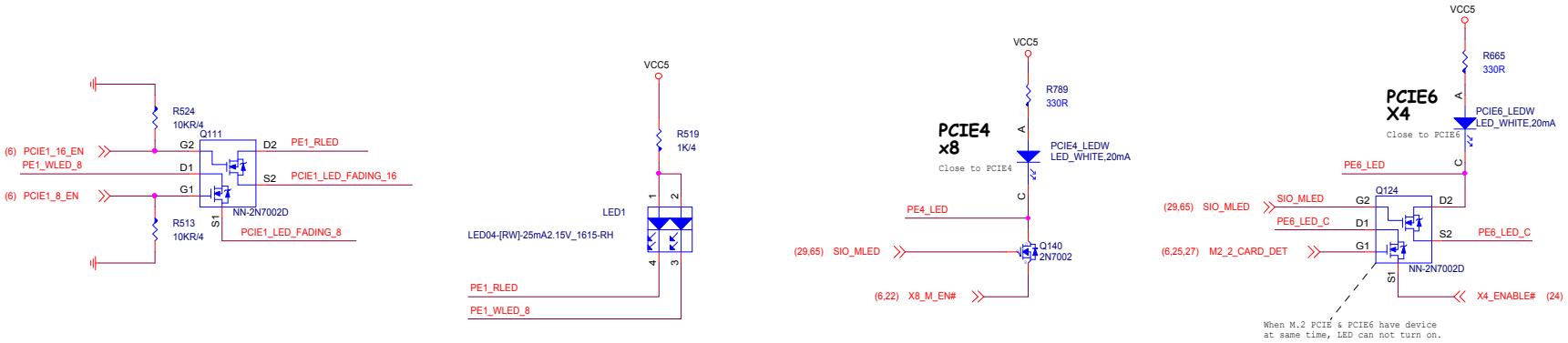
DIMM_SLOT FORM SIO

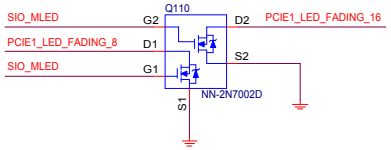
D0C-040P100-H91/D0C-040S500-E07



PCIE_SLOT LED FORM SIO



	x16	x8	x4
PCIE1	Red	X	X
PCIE1	X	White	X
PCIE4	X	White	X
PCIE6	X	X	White



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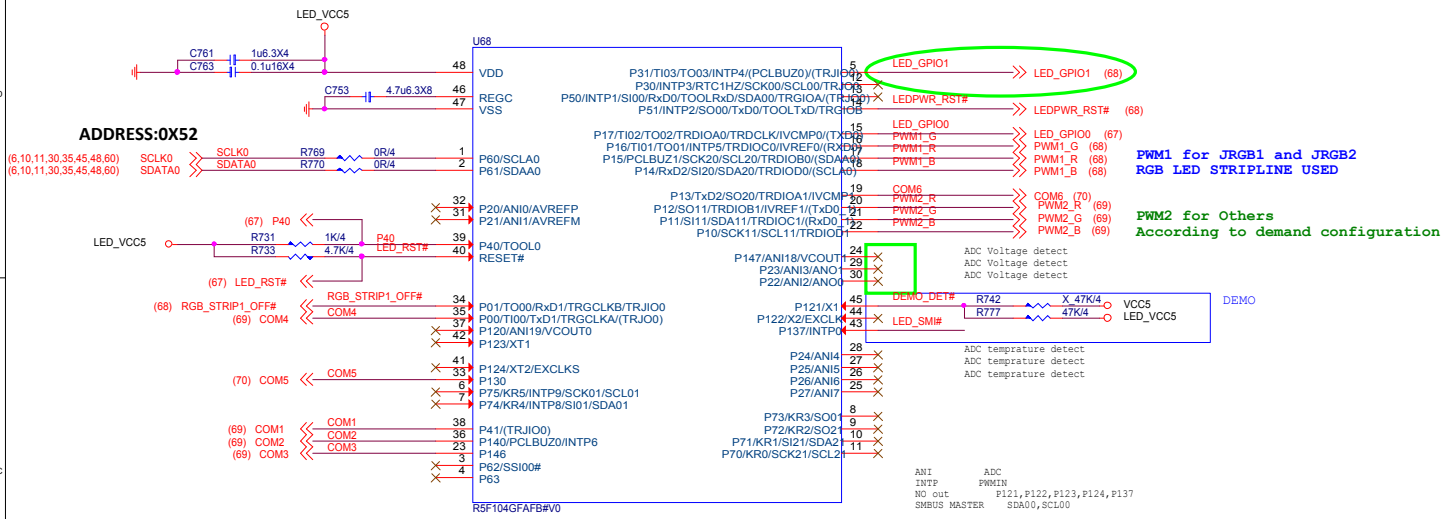
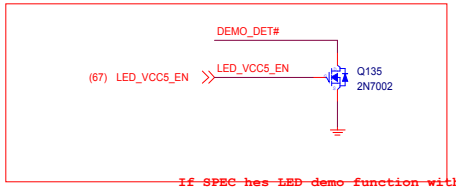
48 PIN LED MCU

C345 & C359 near VDD Pin.



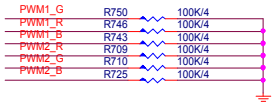
PWM1 for JRGB1 and JRGB2
RGB LED STRIPLINE USED

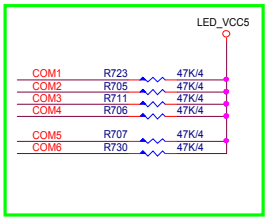
PWM2 for Others
According to demand configuration



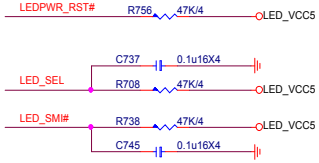
~~If SPEC hes LED demo function without demo button,~~
DEMO_DET# must pull up to LED_VCC5 and control by LED_VCC5_EN.
~~PS. R1000 remove, R1457 and Q296 need to stuff~~

Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~4	PWM2	RGB LED
Board Side LED	COM5~8	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED2
IO Cover	LED_GPIO0	No Use	JPIPE_LED1





COM1~8 for PWM2
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.



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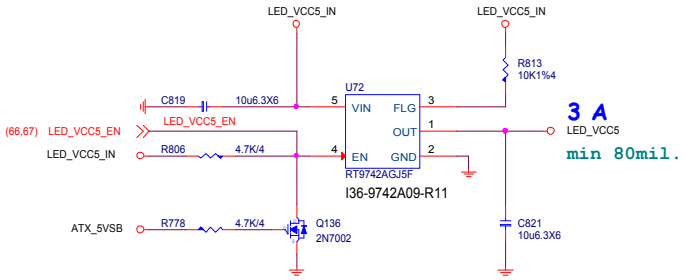
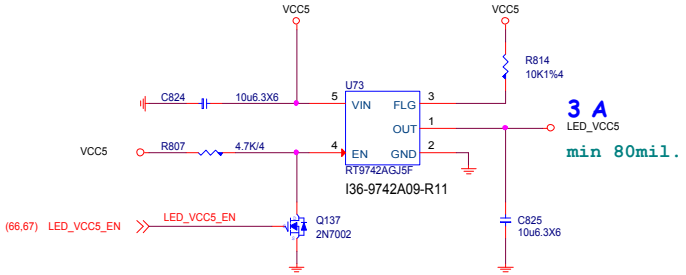
EXTERNAL POWER INPUT

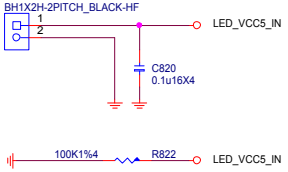




External Power

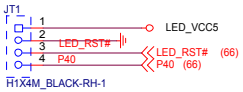
2A Connector

N32-1020CB1-H06



JT1 for FW update

For FW update.

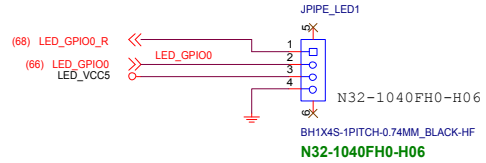


1027 Remove JT1

LED Demo Button

1 PCH HEATSINK LED
PCS LED*0.16W=W

2 AUDIO/IO Cover LED
PCS LED*0.16W=W



3 MOS HEATSINK LED
PCS LED*0.16W=W

Color Demo Jumper

JPIPE_LED3 no SPEC

JPIPE:PIN1:output ,PIN2:input

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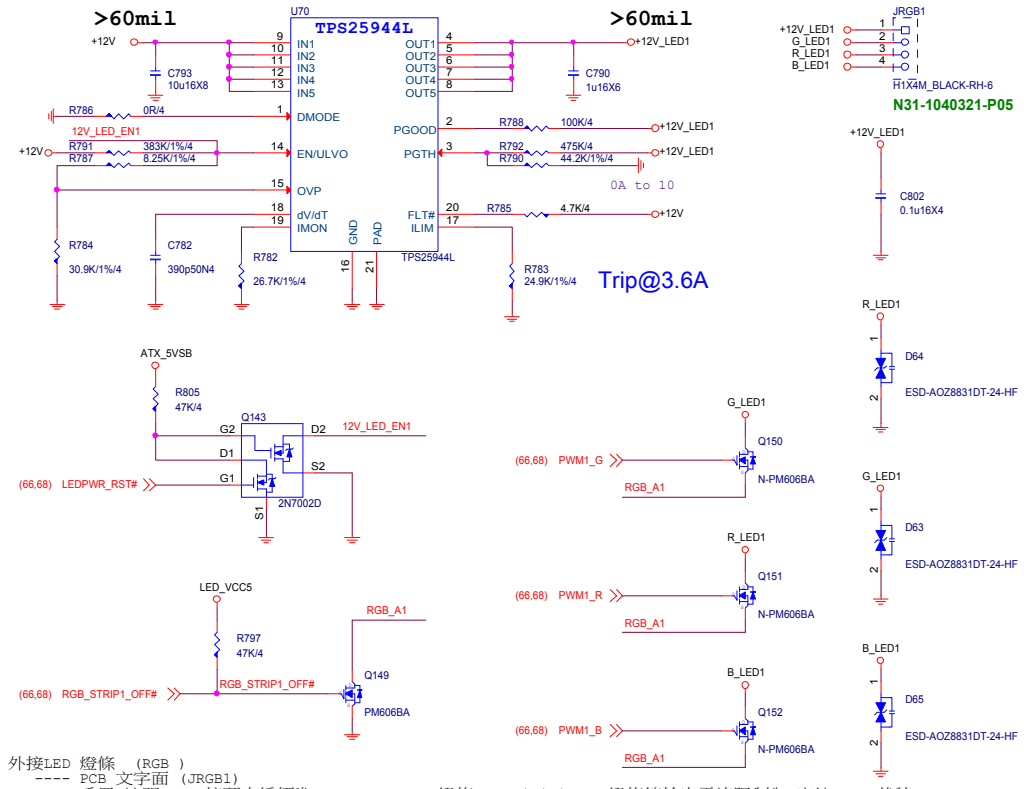
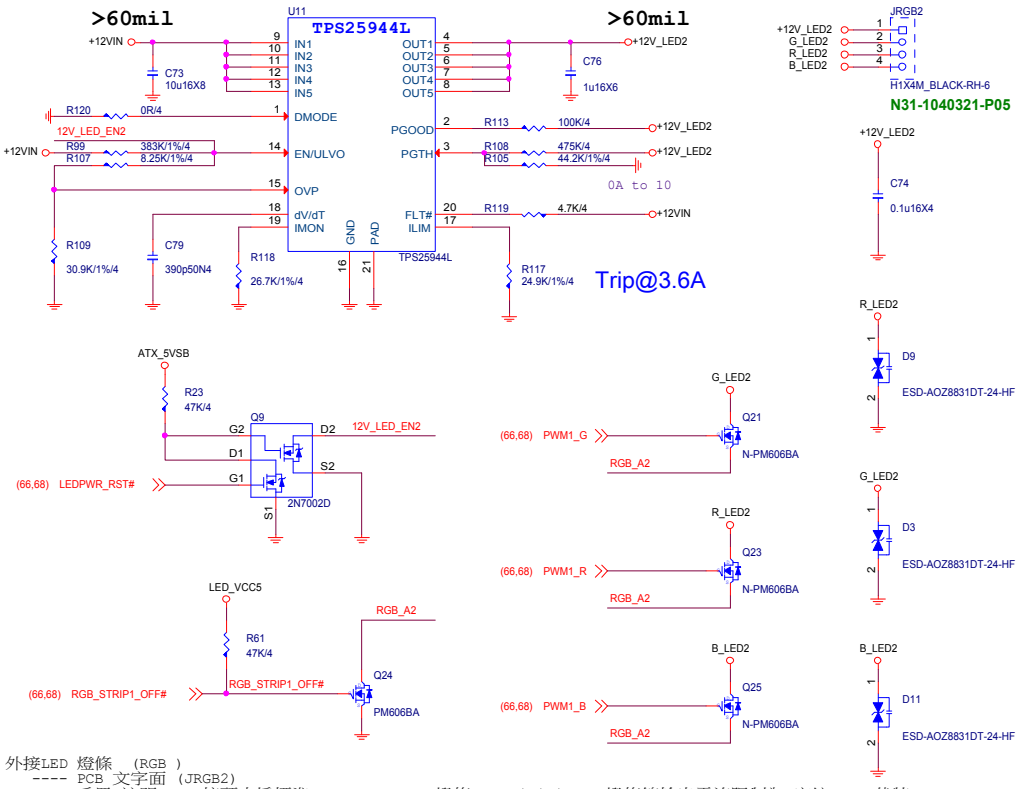
JRGB1



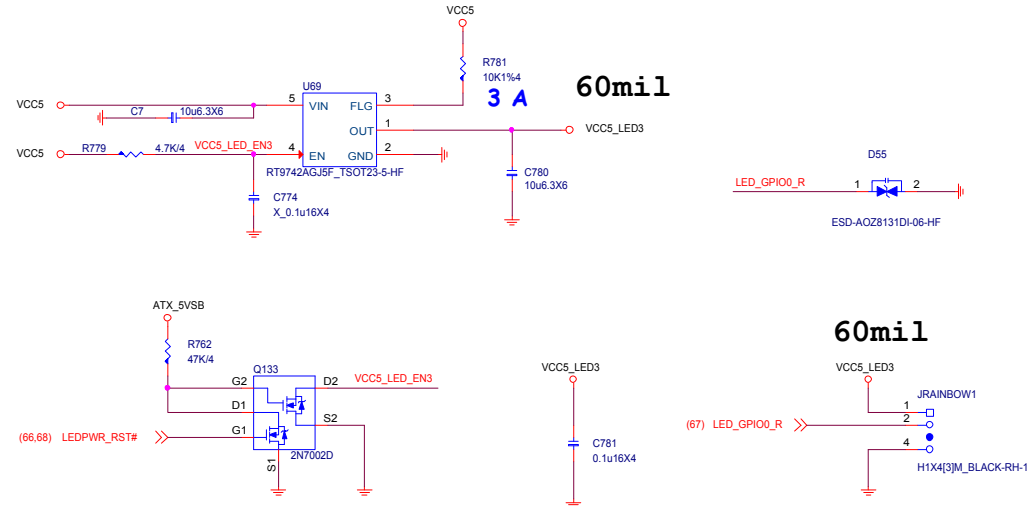
外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

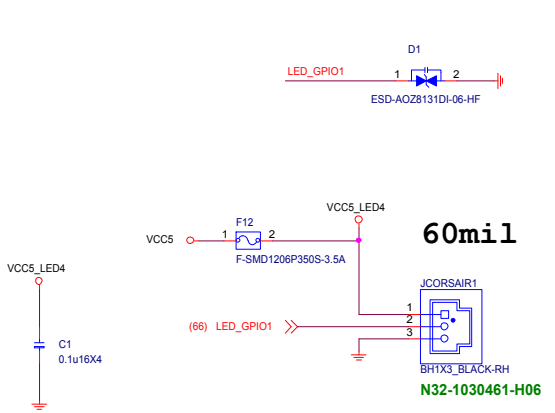


外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB2)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRAINBOW1



JCORSAIR1



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MS-7B78		
Size: Custom	Document Description: LED - JLED1 / 2 / 3 / 4	Rev: 11
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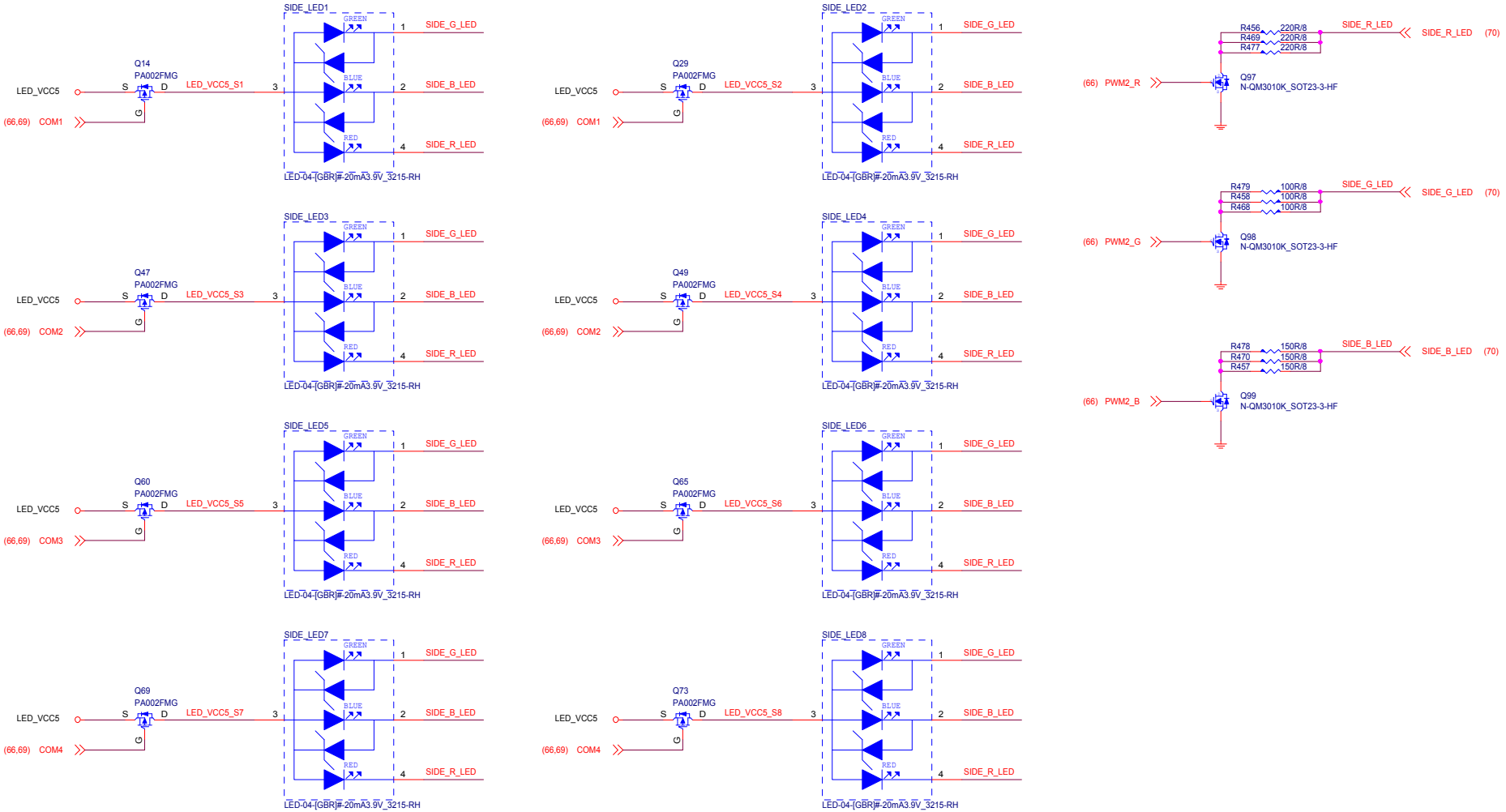
Right Track LED *8



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MS-7B78		
Size: Custom	Document Description: LED - Mystic Light - 1	Rev: 11
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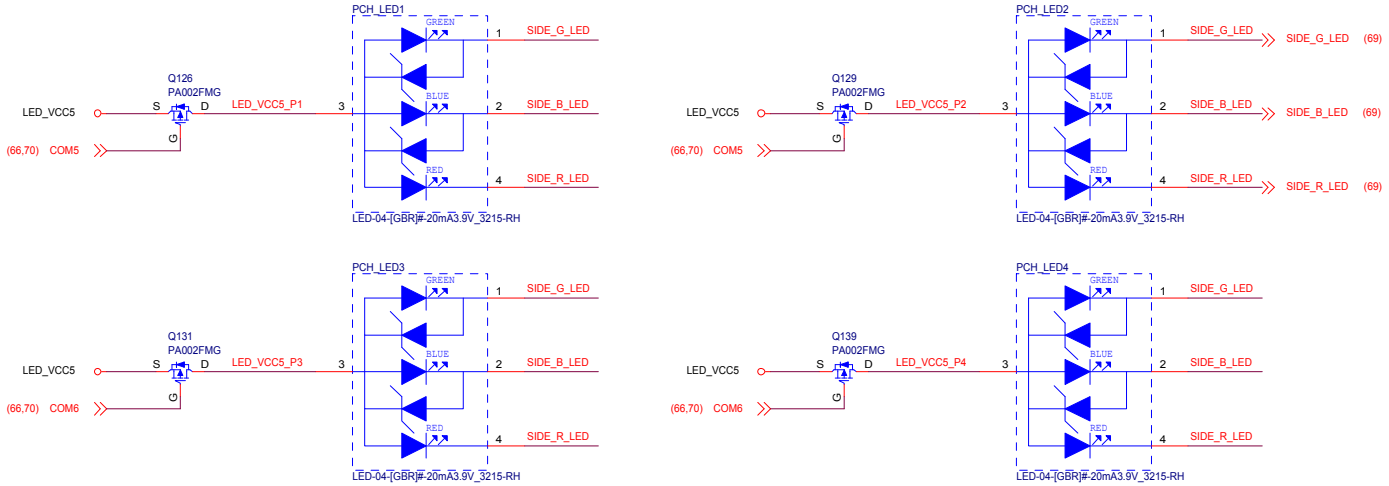
PCH LED *4



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MS-7B78			
Size: Custom	Document Description: LED - Mystic Light - 2		Rev: 11
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MS-7B78

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Custom	BOM Option	11

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CPU Socket

CPU3

E95-0000021-C22

E95-0000022-C22

Simulation

X_JS3 — SIM1 — X_PIN1*2

X_JS4 — SIM2 — X_PIN1*2

FM9, FM7, FM5, FM2, FM6, FM8, FM3, FM1 — X_FM120

Optics Orientation Holes

MH1, MH2, MH3, MH4, MH5, MH6, MH8, MH9, MH7 — X_MH001

C783 0.1u/16X4

C792 0.1u/16X4

MANUAL PART

UEFI1 — G51-M1SPXXA-A09 — **G51-M1SPXXA-A09**

CFOS <MSI-BOM> — Y02-MU00170-CFO — **Y02-MU00170-CFO**

XSPLIT <MSI-BOM> — X_Y02-MA00401-XSP — **Y02-MA00401-XSP**

HDMI_LA1 — Label — HDMI LABEL — **Y01-RHDMI03-000**

NAHIMIC <MSI-BOM> — Y02-MU00100-NAH — **Y02-MU00100-NAH**

SSE <MSI-BOM> — X_Y02-MA00101-SSE — **Y02-MA00101-SSE**

SLI <MSI-BOM> — Y01-RNVIDIL-000 — **Y01-RNVIDIL-000**

WIFI_MUDUAL <MSI-BOM> — WIFI — **604-4442-020**

BAT1_X1 — BAT-BCR2032P

LA6 — MKT — X470

AVL:
D06-0100161-F52
D06-0100101-K26

PCB

PCB

PCB1

7B78_11

PD0-07B7811-G37

MOS HEATSINK

HS_MOS1 — MEC1, MEC2 — E31-0505610-RH

HS_MOS2 — MEC1, MEC2, MEC3, MEC4, MEC5 — HS-0505620-RH

IO COVER+MOSA

PCH HEATSINK

PCH_HS1 — PCH Shink — MCE1, MCE2 — E31-0409590-RH

PCH Heatsink

Audio COVER

COVER1 — Audio Cover — E21-7A62010-RH

DDR COVER

DDR_COVER1 — DDR COVER — X1, X2, X3, X4, X5 — E21-7A63010-RH

0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

mos heatsink

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