Model Name : VILE1 & VILE2
File Name : NM-A043, NM-A044
BOM P/N:

VILE1:

VILE2:

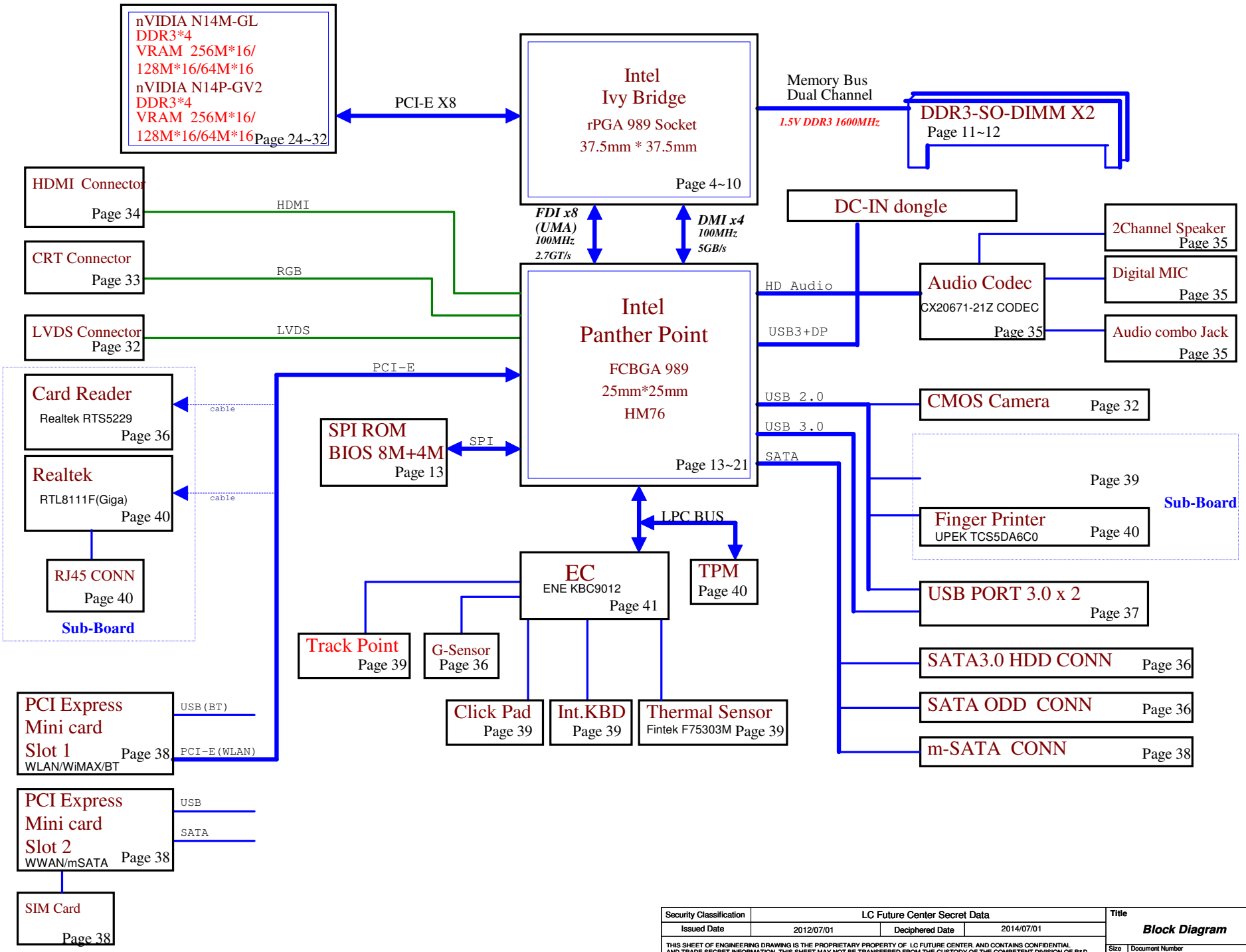
# M/B Schematics Document

## Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

## GPU nVIDIA N14M-GL / N14P-GV2

2012-11-07

REV:0.1

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| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: **Block Diagram**

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

Date: Thursday, November 01, 2012 Sheet 2 of 59

## Voltage Rails

| power plane / State | +B | +5VALW<br>+3VALW | +1.5V | +5VS<br>+3VS<br>+1.5VS<br>+VCCP<br>+CPU_CORE<br>+VGA_CORE<br>+VCC_GFXCORE_AXG<br>+1.8VS<br>+0.75VS<br>+1.05VS | +3VM<br>+1.05VM |
|---|---|---|---|---|---|
| S0 | O | O | O | O | O<br>M3 Supported |
| S3 | O | O | O | X | O<br>M3 Supported |
| S5 S4/AC | O | O | X | X | O<br>M3 Supported |
| S5 S4/ Battery only | X | X | X | X | |
| S5 S4/AC & Battery don't exist | X | X | X | X | |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011X b |

## EC SM Bus2 address

| Device | Address |
|---|---|
| Thermal Sensor Fintek F75303M | 1001_101xb |

## PCH SM Bus address

| Device | Address |
|---|---|
| DDR DIMM0 | 1001 000Xb |
| DDR DIMM2 | 1001 010Xb |

## USB Port Table

| | USB 2.0 | Port | 3 External USB Port |
|---|---|---|---|
| EHCI1<br>USB3.0 | UHCI0 | 0 | USB 3.0 Port (Left Side) |
| | | 1 | |
| | UHCI1 | 2 | USB 3.0 Port (Left Side) |
| | | 3 | USB 3.0 Port |
| | UHCI2 | 4 | Touch Panel |
| | | 5 | |
| | UHCI3 | 6 | |
| | | 7 | |
| EHCI2 | UHCI4 | 8 | |
| | | 9 | USB Port (Right Side) |
| | UHCI5 | 10 | Mini Card(WLAN/BT) |
| | | 11 | FPR |
| | UHCI6 | 12 | Mini Card(WWAN) |
| | | 13 | Camera |

## BOM Structure Table

| BTO Item | BOM Structure |
|---|---|
| Connector | ME@ |
| 45 LEVEL | 45@ |
| Unpop | @ |
| NVidia | DIS@ |
| | |
| PCH AUX Power | +3V_PCH@ |
| Intel UMA | UMA@ |
| VRAM Option | X76@ |
| Intel SBA | SBA@ |
| Intel AOAC | AOAC@ |
| TPM | TPM@ |
| GPU N14M-GL | N14MGL@ |
| GPU N14P-GV2 | N14PGV2@ |
| SIM Card Slot | 3G@ |
| Touch Panel | Touch@ |
| Finger Print Board | FP@ |
| SSD | SSD@ |
| | |

## SMBUS Control Table

| | SOURCE | VGA | BATT | KE9012 | SODIMM | WLAN WWAN | Thermal Sensor | PCH |
|---|---|---|---|---|---|---|---|---|
| SMB_EC_CK1<br>SMB_EC_DA1 | KB9012<br>+3VALW | X | V<br>+3VALW | X | X | X | X | X |
| SMB_EC_CK2<br>SMB_EC_DA2 | KB9012<br>+3VALW | X | X | X | X | X | X | V<br>+3VS |
| SMBCLK<br>SMBDATA | PCH<br>+3VALW | X | X | X | V<br>+3VS | V<br>+3VS | X | X |
| SML0CLK<br>SML0DATA | PCH<br>+3VALW | X | X | X | X | X | X | X |
| SML1CLK<br>SML1DATA | PCH<br>+3VALW | V<br>+3VS | X | V<br>+3VS | X | X | V<br>+3VS | X |

ZZZ5

DA PCB

DA80000TG00

NM-A043

B2 — 46J_BARCODE_16X7 @

B3 — UUID_BARCODE_16X7 @

| | | | |
|---|---|---|---|
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| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: Notes List

Size: Custom | Document Number: NM-A041 | Rev: 1.A

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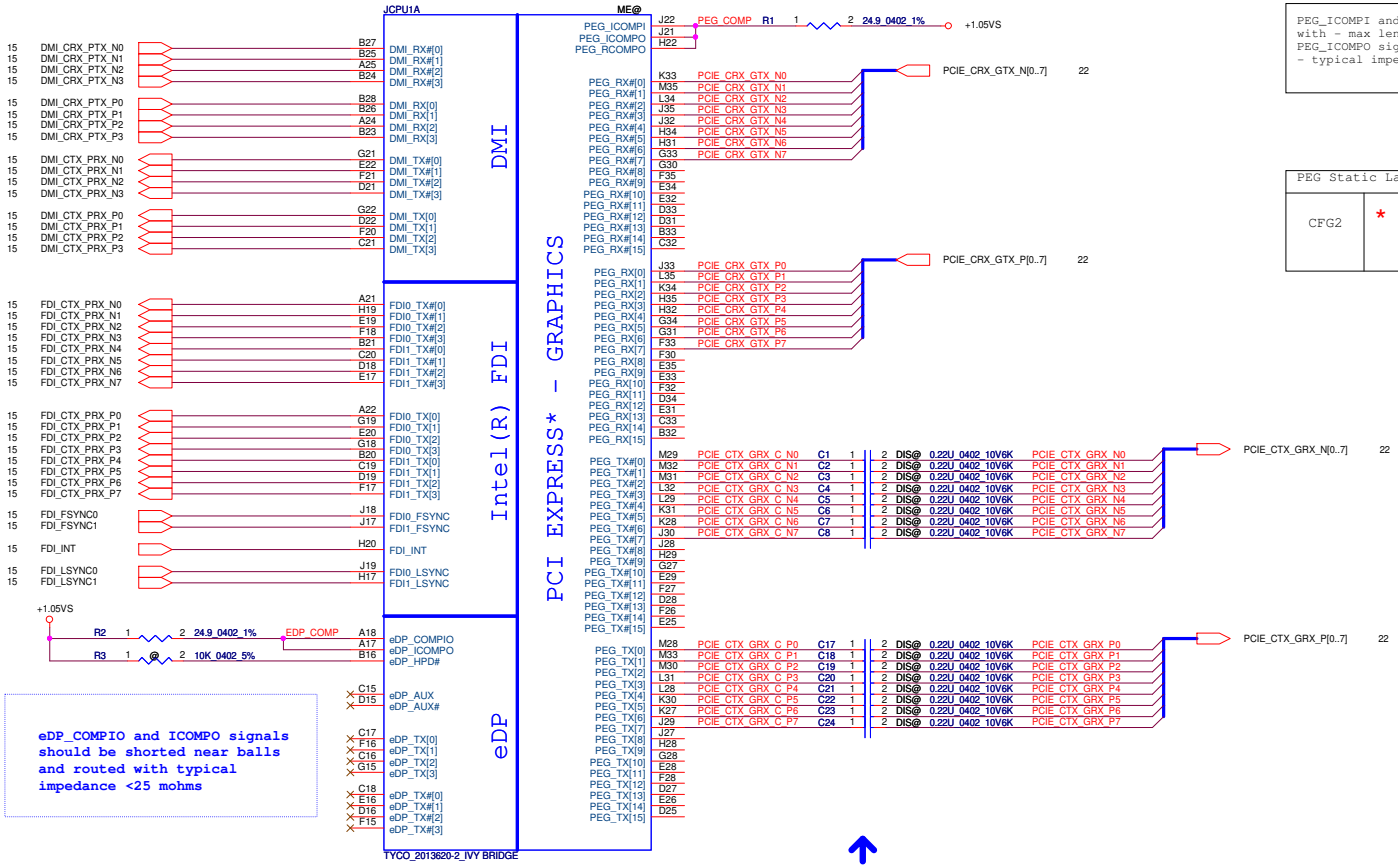



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x

| | |
|---|---|
| CFG2 | * 1: Normal Operation; Lane # definition matches socket pin map definition<br>0:Lane Reversed |

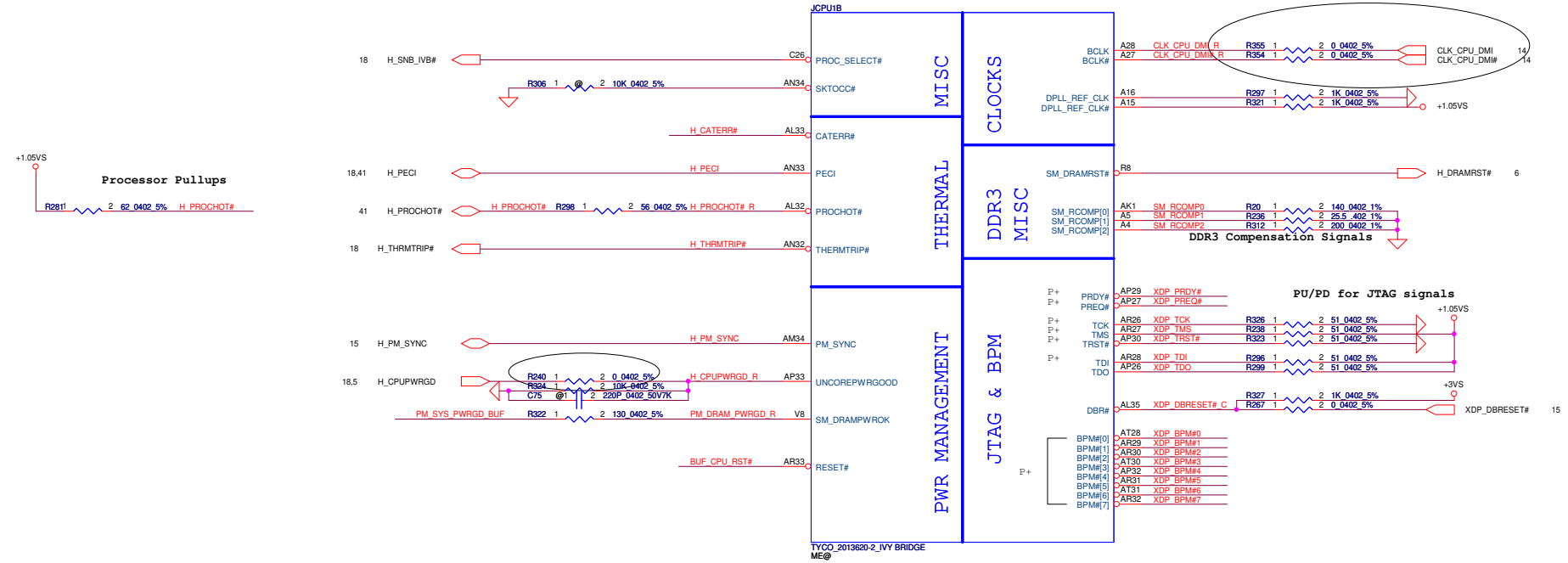
| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

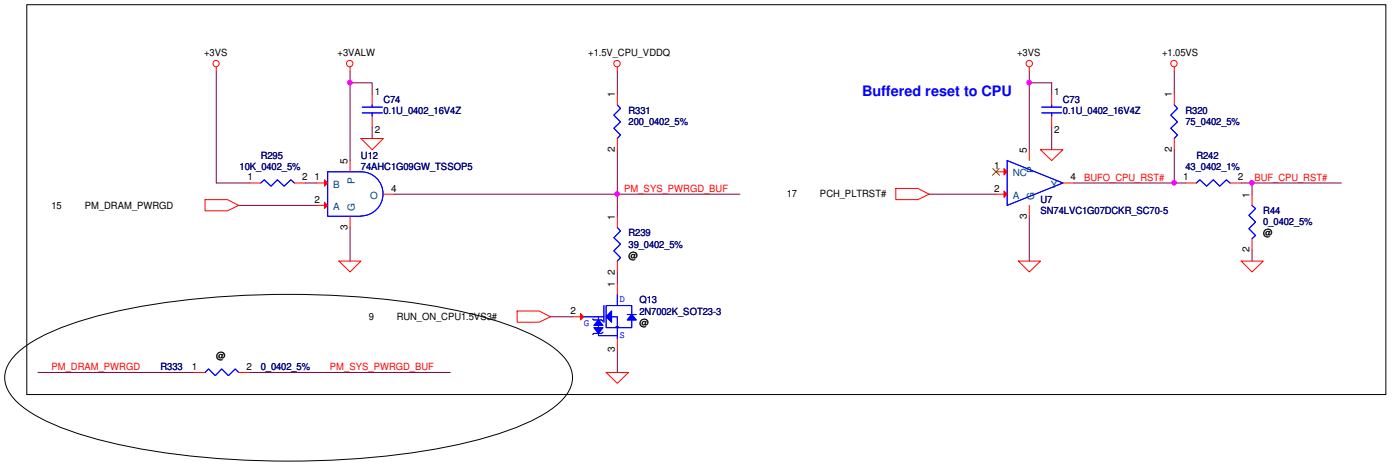


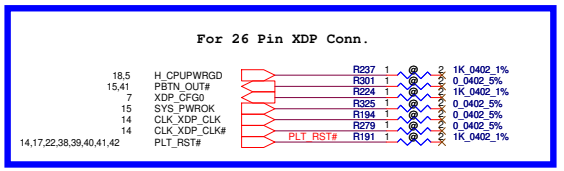
Title: PROCESSOR(1/7) DMI,FDI,PEG

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

Date: Thursday, November 01, 2012 Sheet 4 of 59



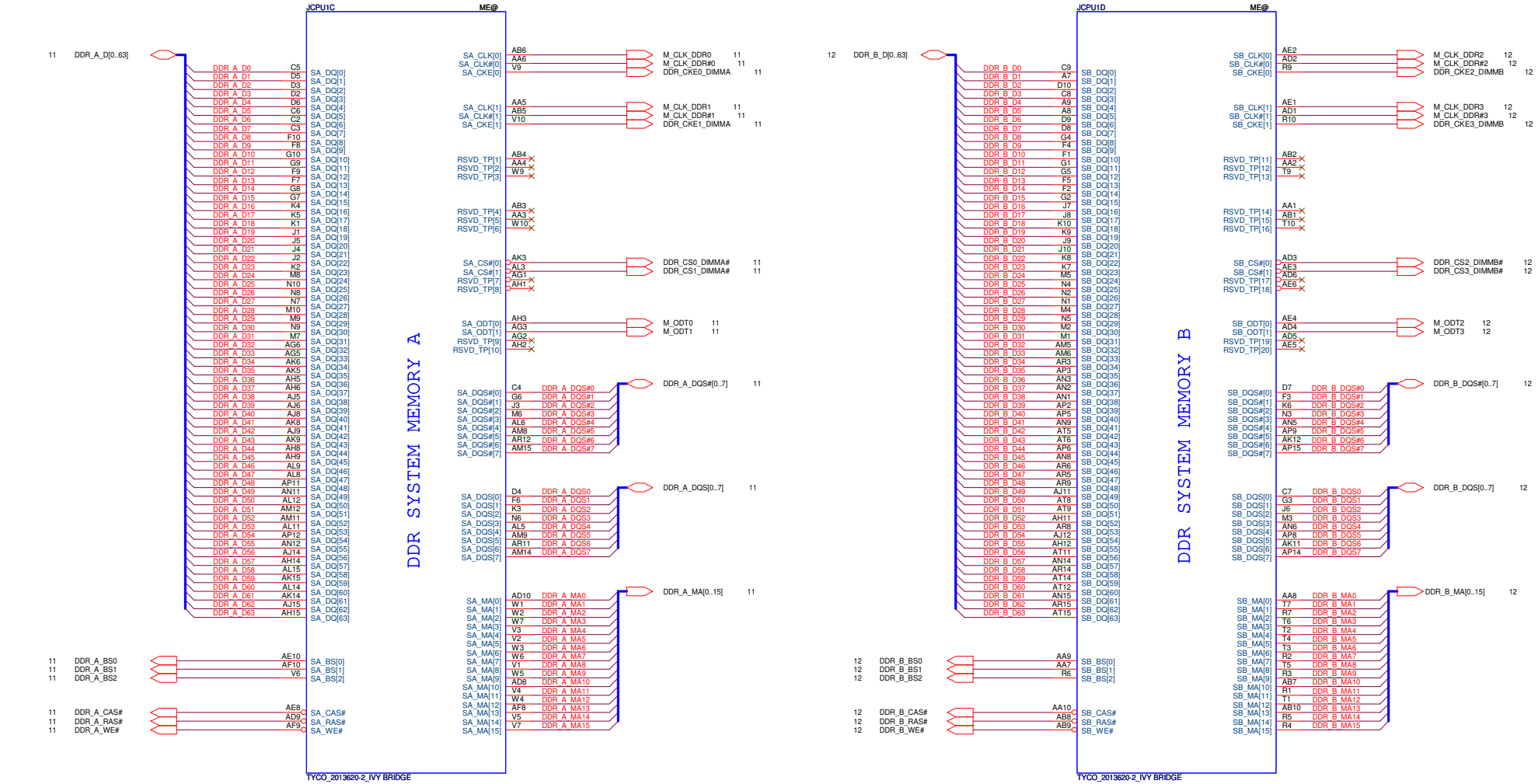

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

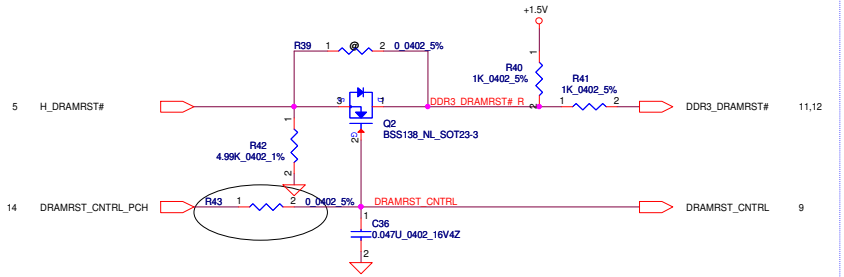


Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 5 of 59



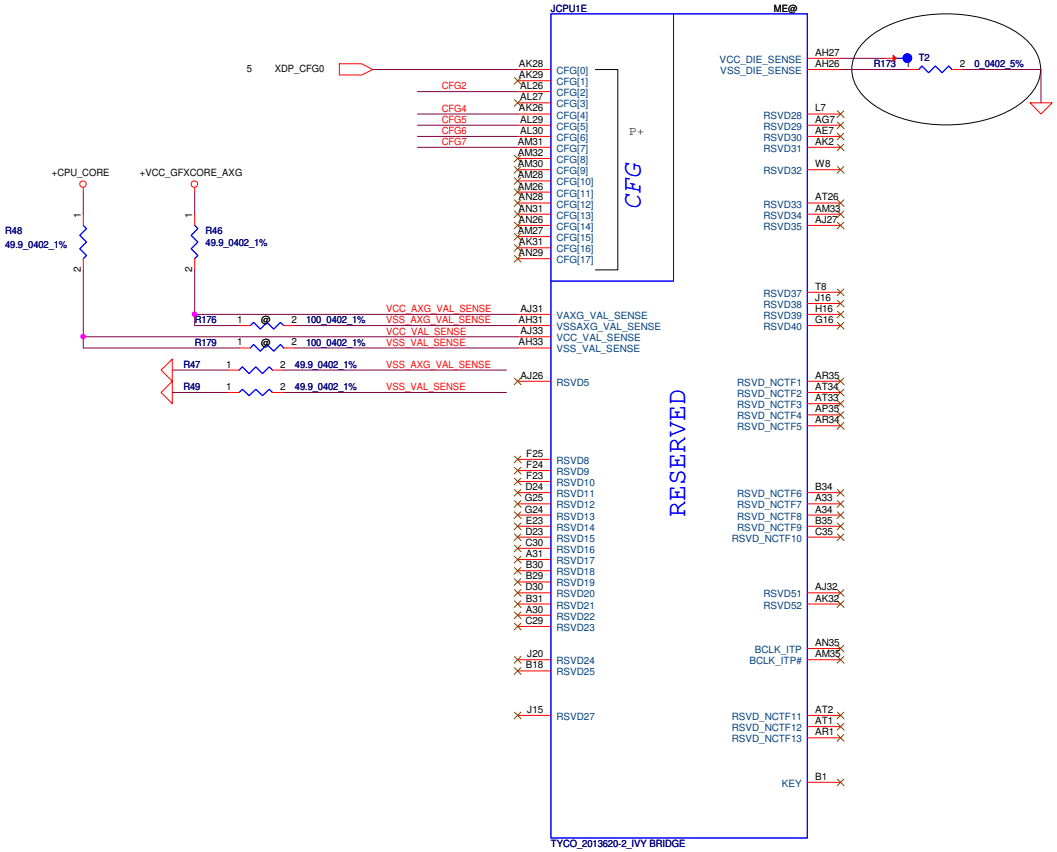

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



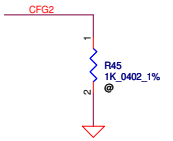
Title: PROCESSOR(3/7) DDRIII

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

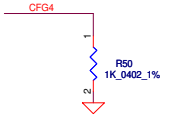
Date: Thursday, November 01, 2012 | Sheet 6 of 59



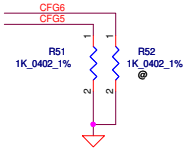

## CFG Straps for Processor



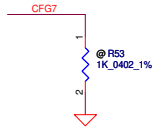

| PEG Static Lane Reversal – CFG2 is for the 16x | |
|---|---|
| CFG2 | * 1: Normal Operation; Lane # definition matches socket pin map definition<br>0:Lane Reversed |




| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |




| PCIE Port Bifurcation Straps | |
|---|---|
| CFG[6:5] | 11: (Default) x16 – Device 1 functions 1 and 2 disabled<br>*10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved – (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 – Device 1 functions 1 and 2 enabled |




| PEG DEFER TRAINING | |
|---|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |

| | | | |
|---|---|---|---|
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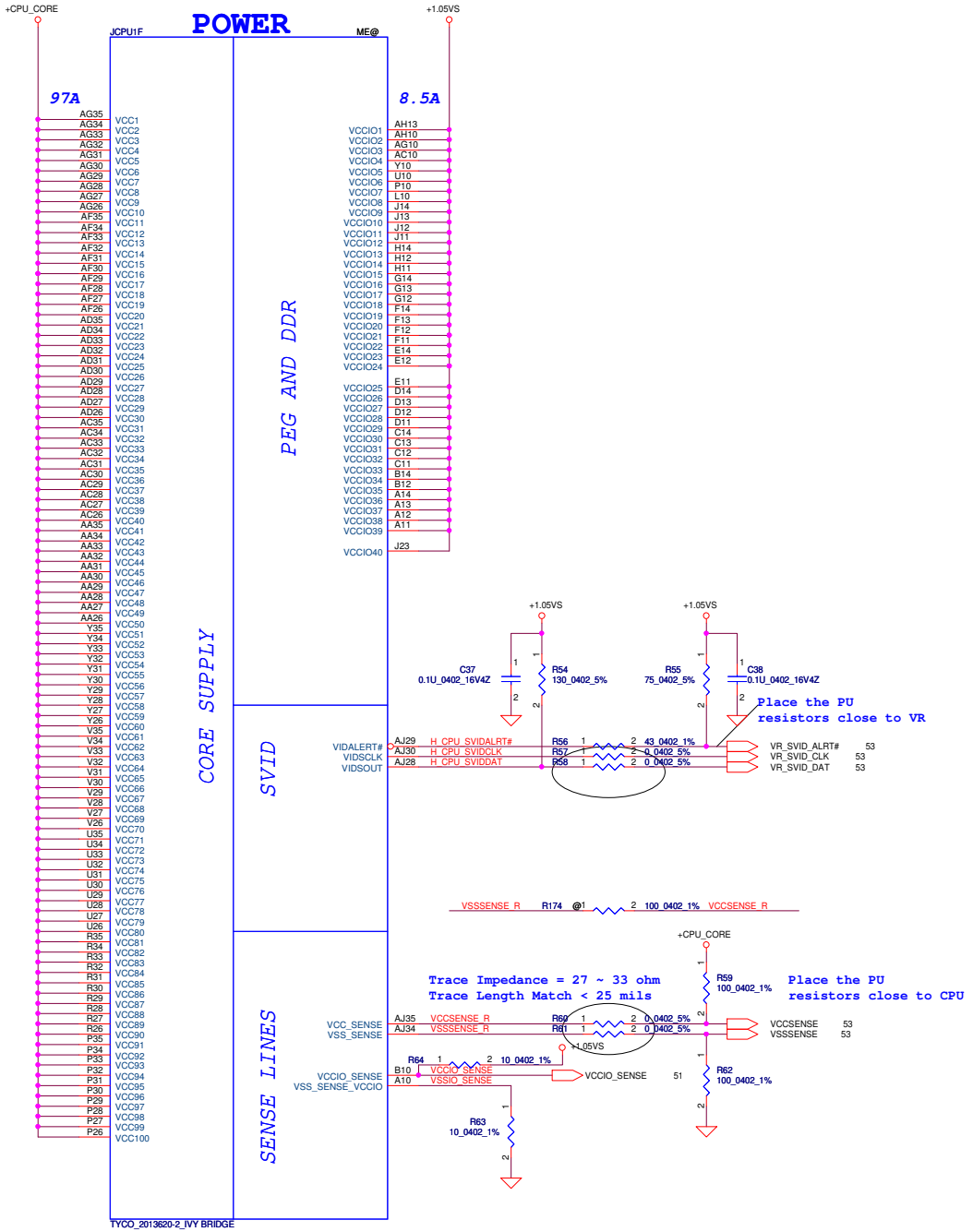
| | | | |
|---|---|---|---|
| Title | PROCESSOR(4/7) RSVD,CFG | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 7 of 59 | | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PROCESSOR(5/7) PWR,BYPASS

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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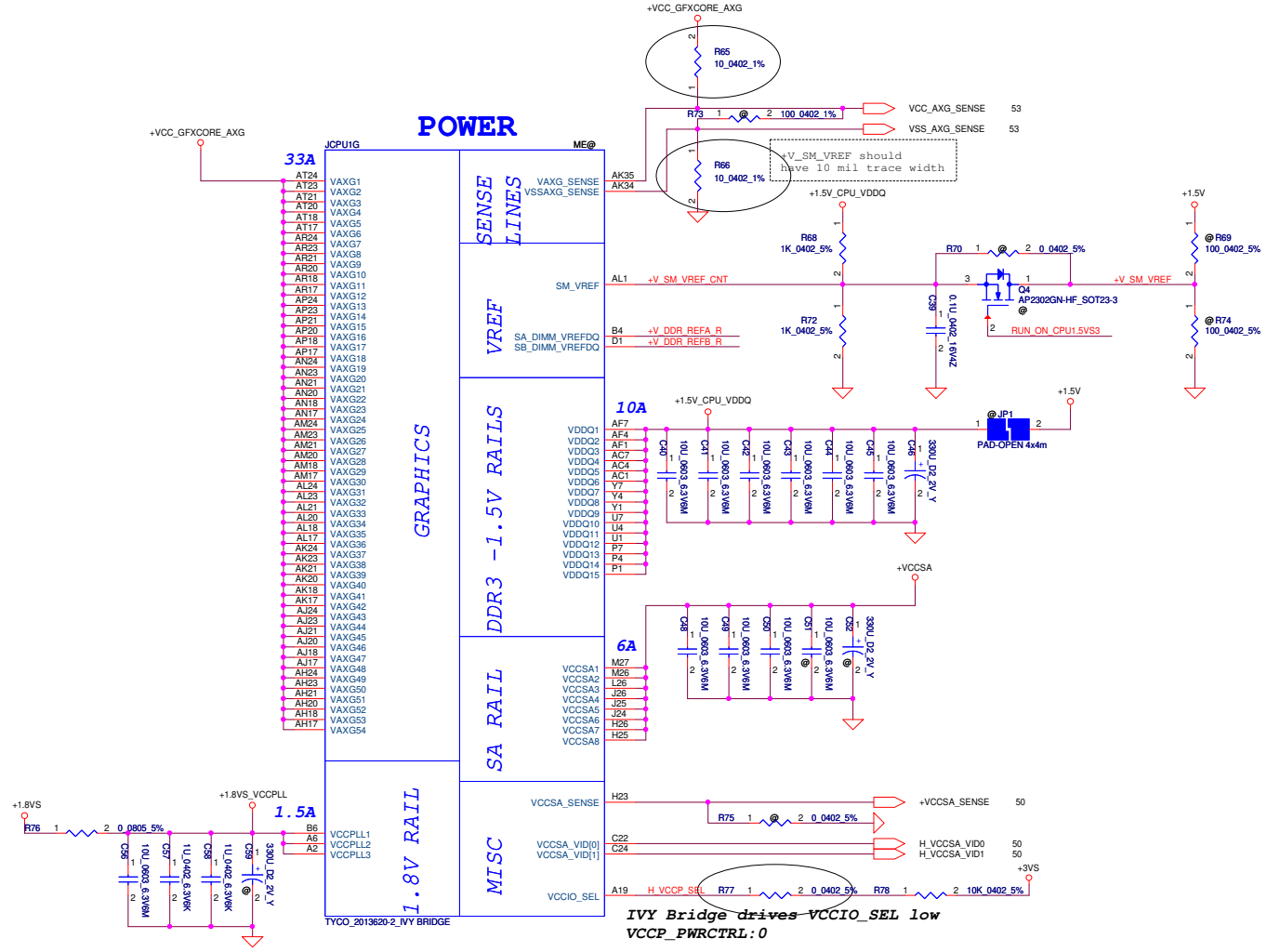
# POWER



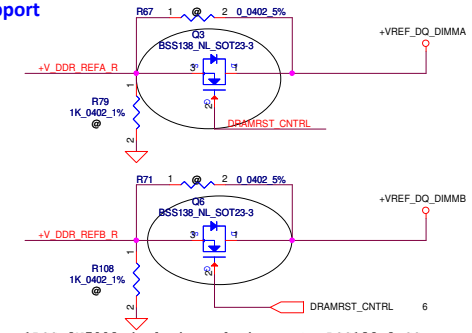

***IVY Bridge drives VCCIO_SEL low***
***VCCP_PWRCTRL:0***

***Sandy Bridge is NC for A19***
***VCCP_PWRCTRL:1***

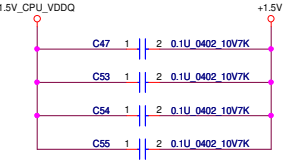
**Vaxg**

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

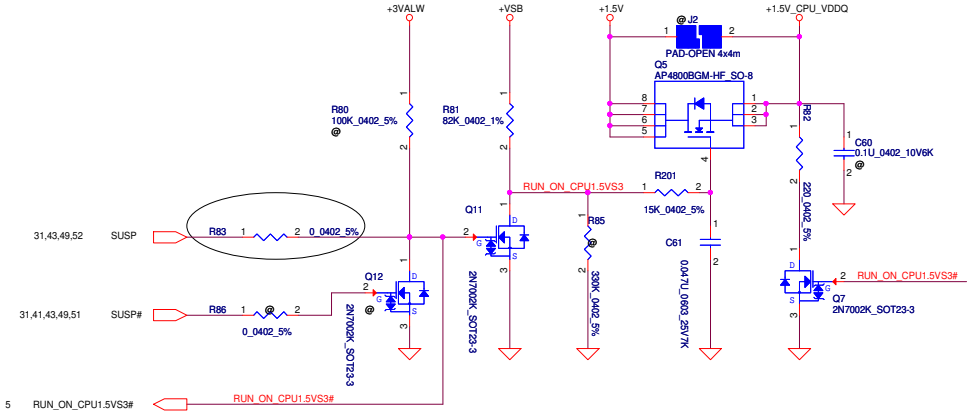
## M3 Support




from 1PCS 2N7002 dual channel change to BSS138 2pCS




## +1.5V_CPU_VDDQ Source

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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



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|---|---|---|---|
| Title | PROCESSOR(6/7) PWR | | |
| Size | Custom | Document Number | NM-A041 |
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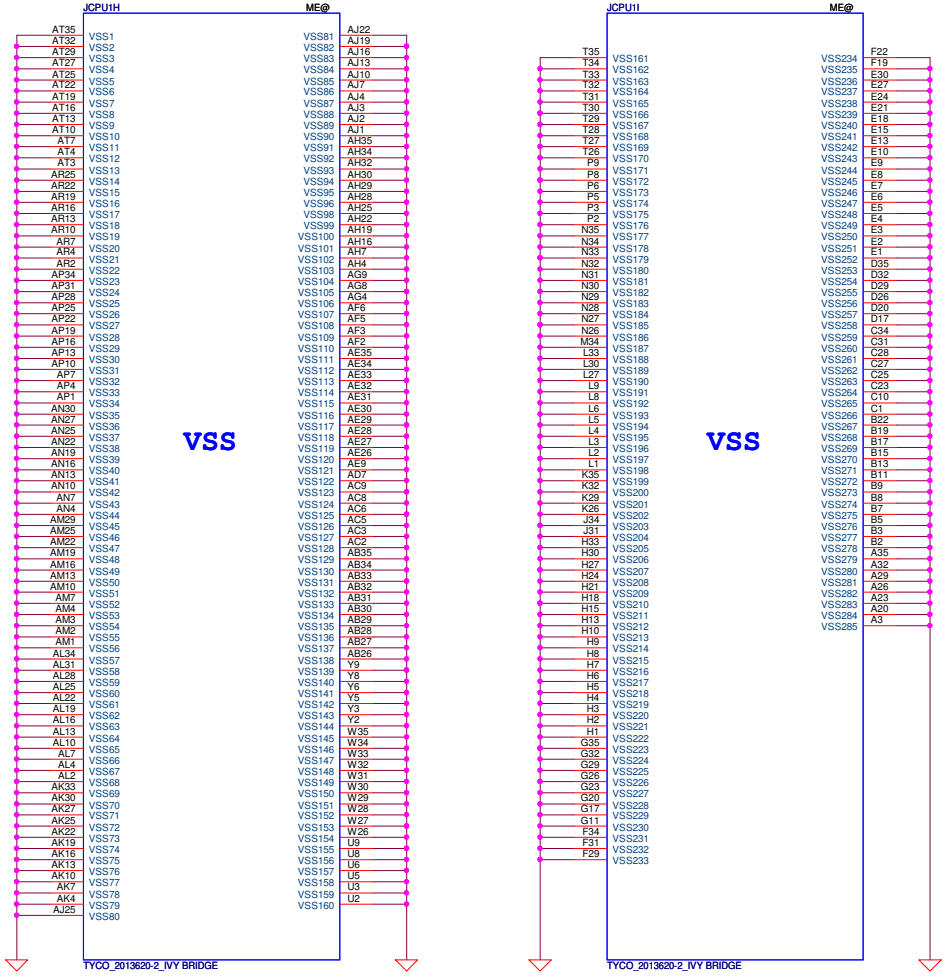
| Date: | Thursday, November 01, 2012 | Sheet | 9 of 59 |

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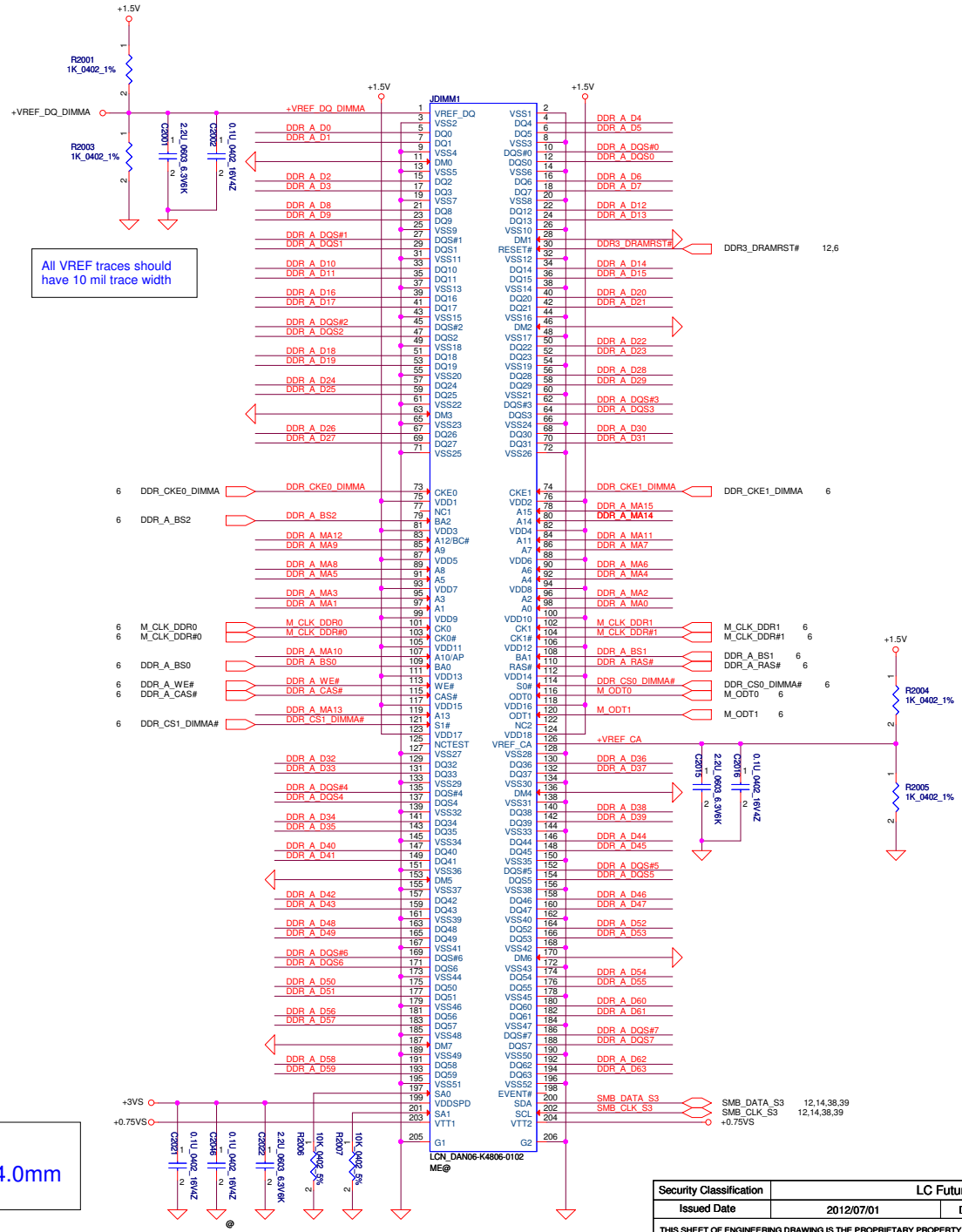
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PROCESSOR(7/7) VSS

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

Date: Thursday, November 01, 2012 | Sheet 10 of 59

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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: DDRIII DIMMA

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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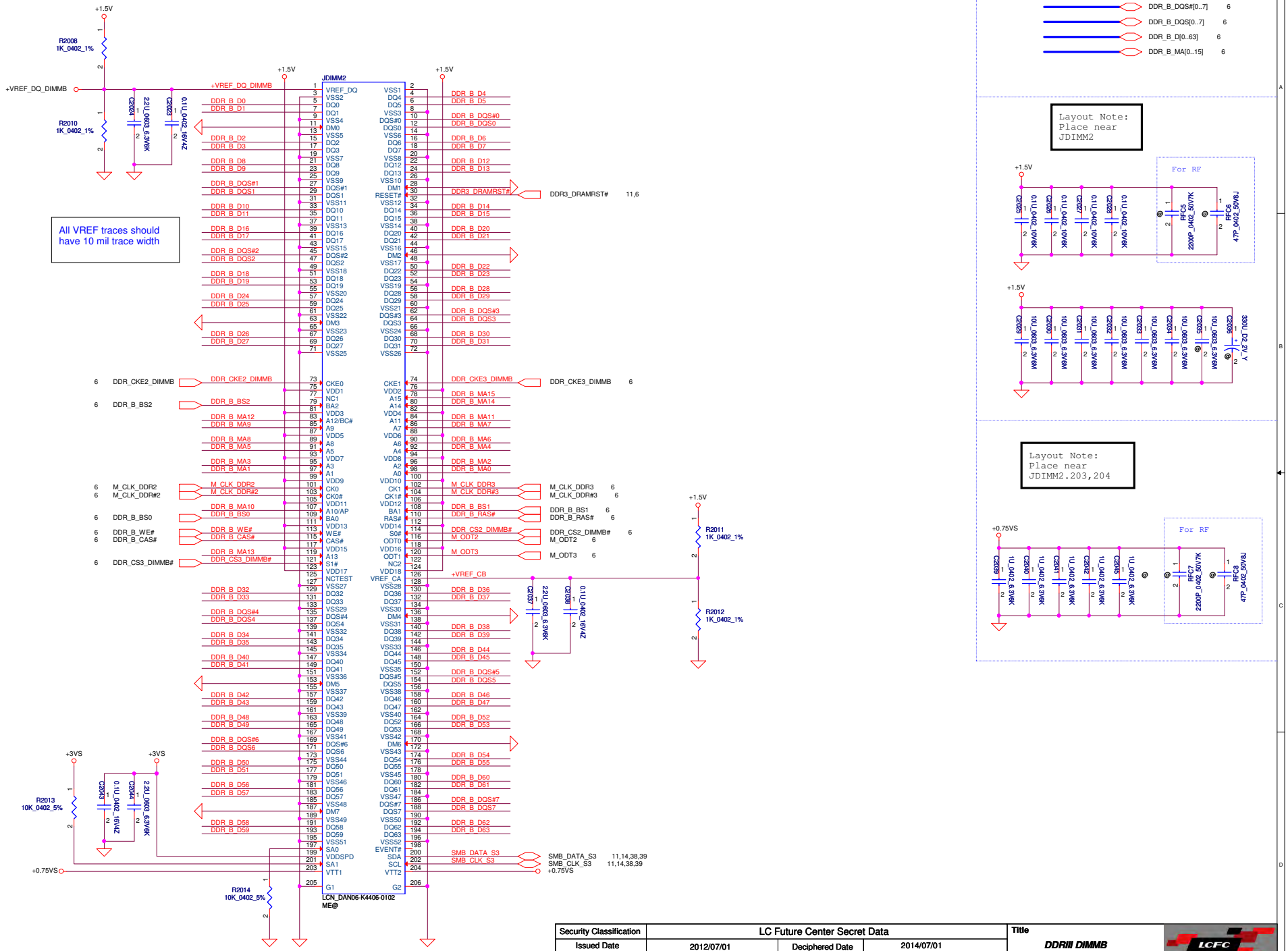


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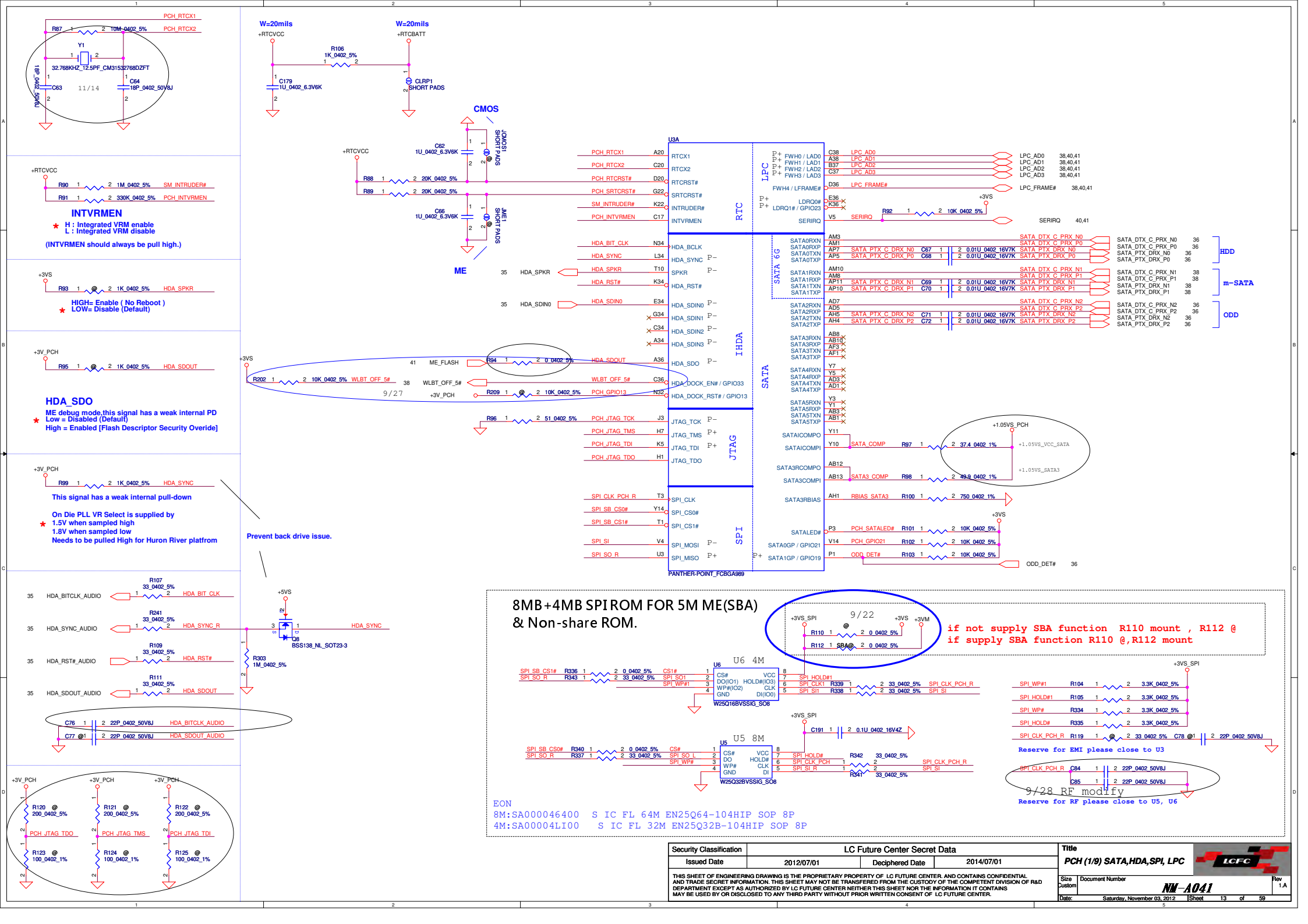
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | DDRIII DIMMB | | |
| Size Custom | Document Number NM-A041 | | Rev 1.A |
| Date: Thursday, November 01, 2012 | Sheet 12 of 59 | | |

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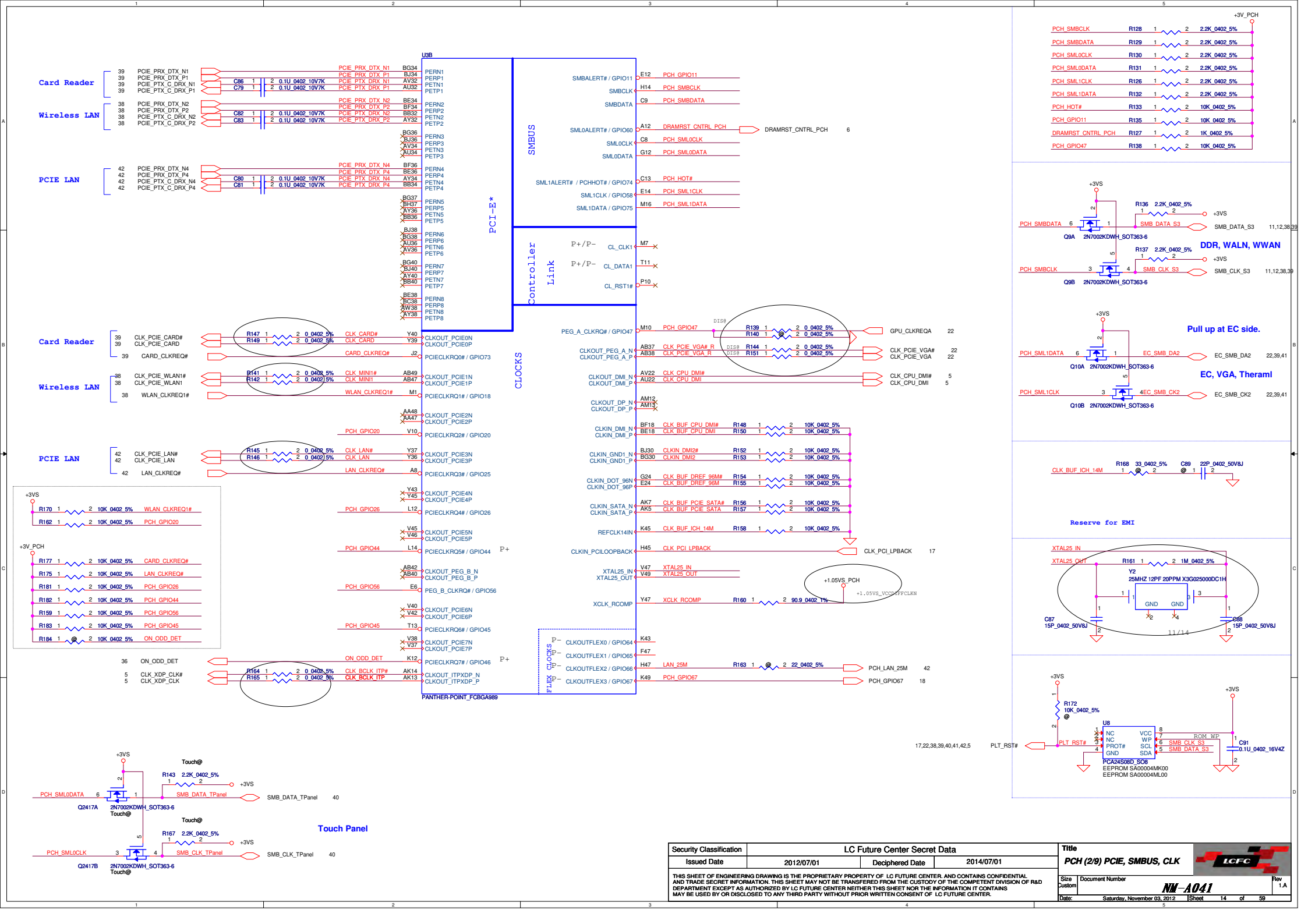
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PCH (1/9) SATA,HDA,SPI, LPC | | |
| Size | Custom | Document Number | NM-A041 |
| Rev | 1.A | | |
| Date: | Saturday, November 03, 2012 | Sheet | 13 of 59 |


Card Reader
Wireless LAN
PCIE LAN
Card Reader
Wireless LAN
PCIE LAN
U3B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PANTHER-POINT_FCBGA989
Touch Panel
DDR, WALN, WWAN
Pull up at EC side.
EC, VGA, Theraml
Reserve for EMI
PCH_SMBCLK
PCH_SMBDATA
PCH_SML0CLK
PCH_SML0DATA
PCH_SML1CLK
PCH_SML1DATA
PCH_HOT#
PCH_GPIO11
DRAMRST_CNTRL_PCH
PCH_GPIO47
SMB_DATA_S3
SMB_CLK_S3
EC_SMB_DA2
EC_SMB_CK2
CLK_BUF_ICH_14M
XTAL25_IN
XTAL25_OUT
Y2
25MHZ 12PF 20PPM X3G025000DC1H
PLT_RST#
PCA24S08D_SO8
EEPROM SA00004MK00
EEPROM SA00004ML00
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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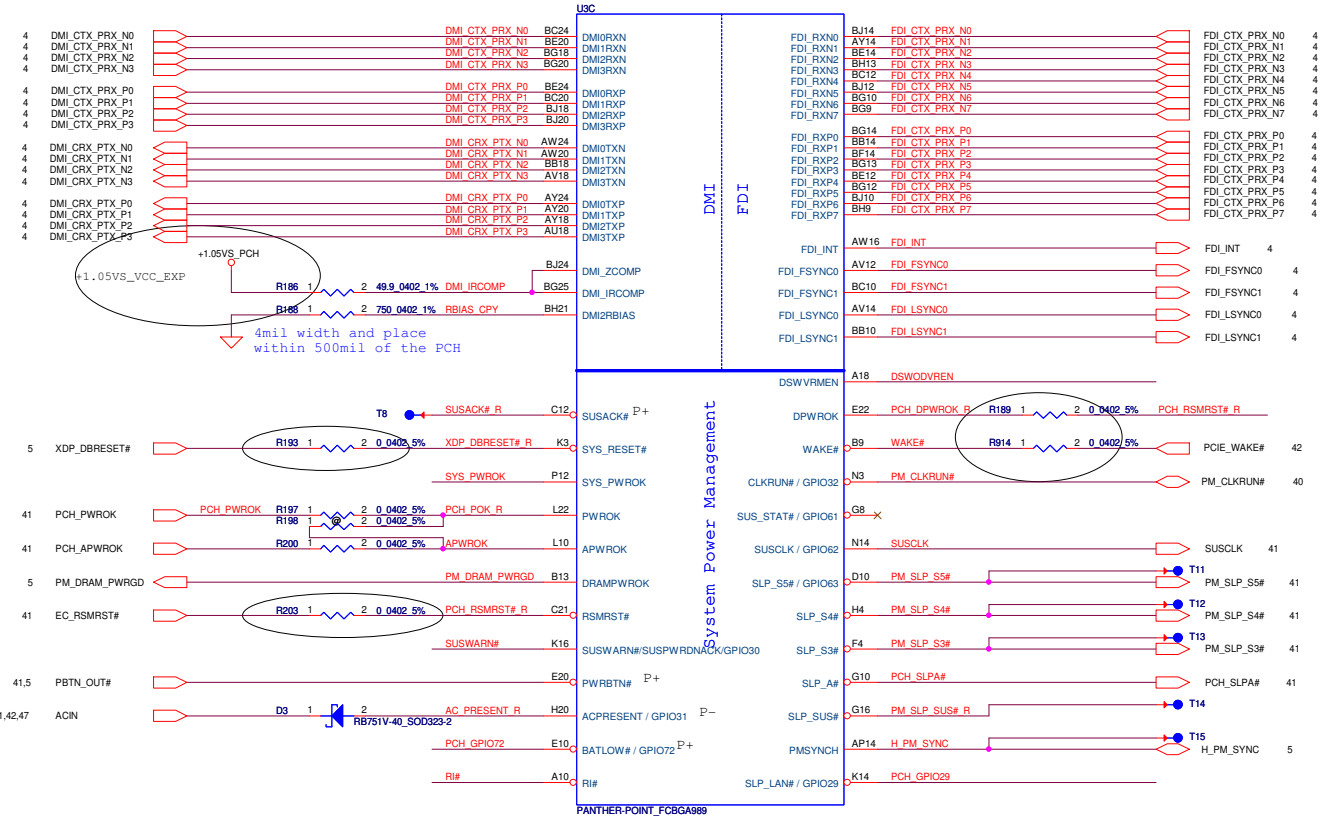
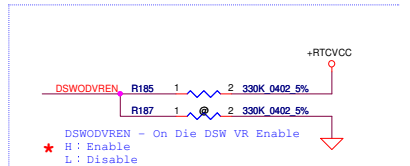
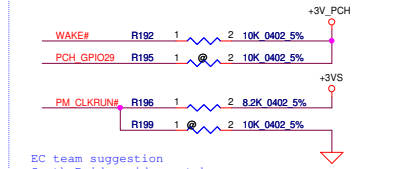
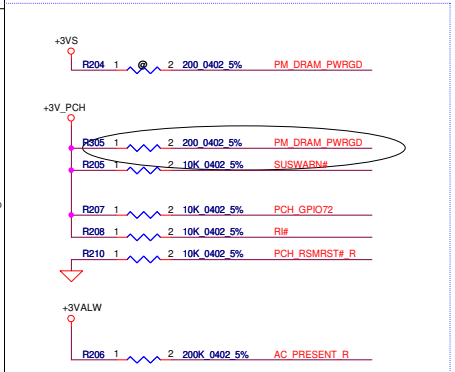
Title
PCH (2/9) PCIE, SMBUS, CLK
Size Custom
Document Number
NM-A041
Rev 1.A
Date: Saturday, November 03, 2012
Sheet 14 of 59

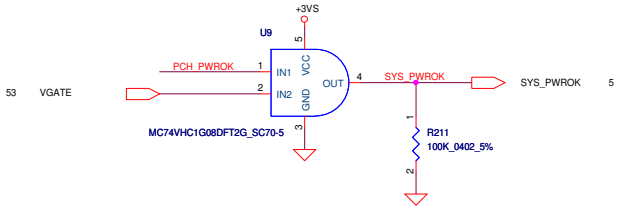



Can be left NC when
IAMT is not support on
the platfrom

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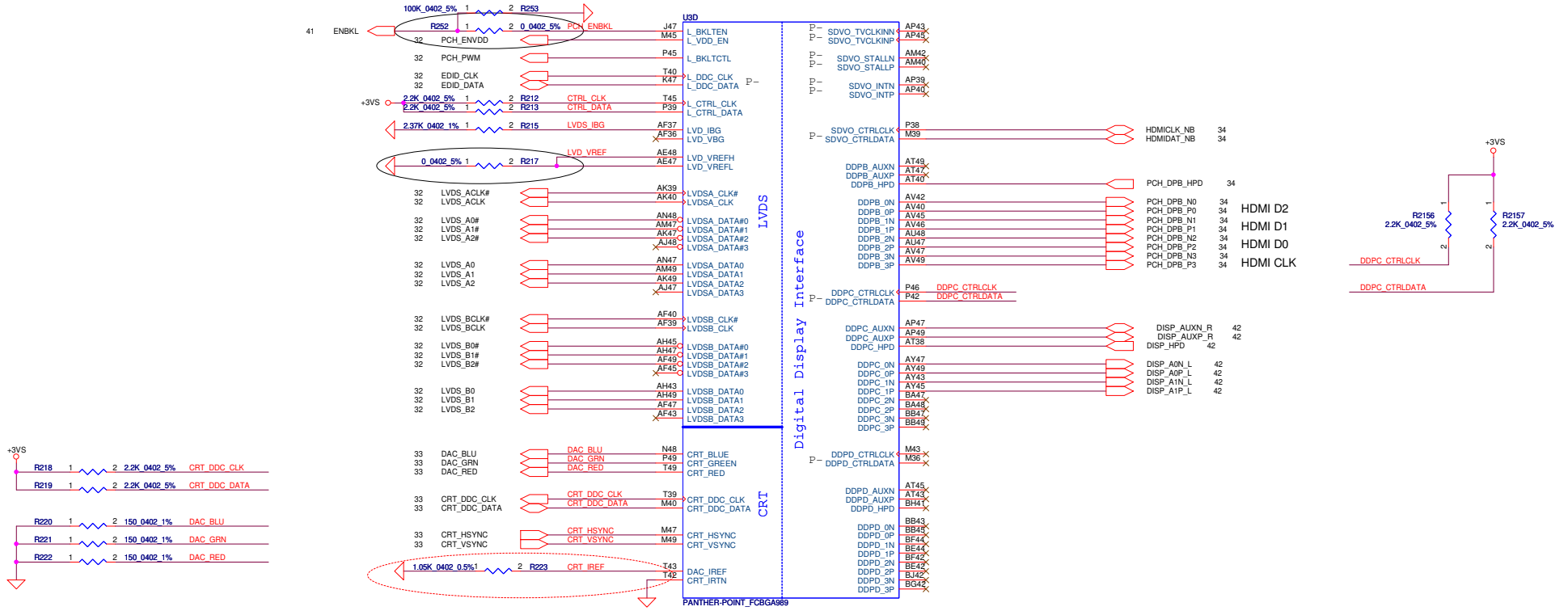
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PCH (3/9) DMI,FDI,PM | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Saturday, November 03, 2012 | Sheet 15 of 59 | | |



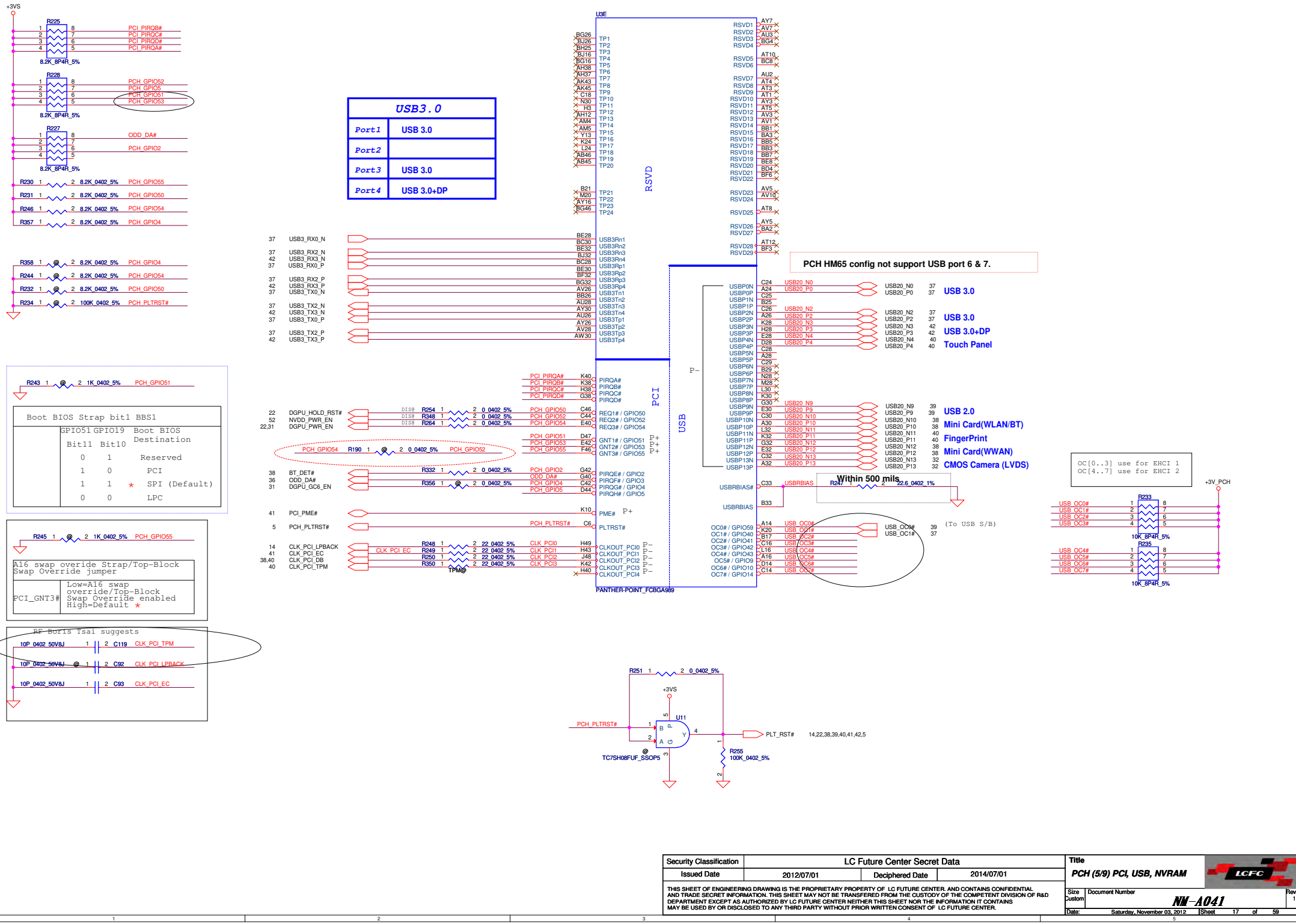

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PCH (4/9) LVDS,CRT,DP,HDMI

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

Date: Saturday, November 03, 2012 Sheet 16 of 59


USB3.0
Port1 USB 3.0
Port2
Port3 USB 3.0
Port4 USB 3.0+DP
PCH HM65 config not support USB port 6 & 7.
USB 3.0
USB 3.0
USB 3.0+DP
Touch Panel
USB 2.0
Mini Card(WLAN/BT)
FingerPrint
Mini Card(WWAN)
CMOS Camera (LVDS)
Within 500 mils
OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2
Boot BIOS Strap bit1 BBS1
GPIO51 GPIO19 Boot BIOS Destination
Bit11 Bit10
0 1 Reserved
1 0 PCI
1 1 SPI (Default)
0 0 LPC
A16 swap overide Strap/Top-Block Swap Override jumper
PCI_GNT3# Low=A16 swap override/Top-Block Swap Override enabled High=Default
RF Boris Tsai suggests
PANTHER-POINT_FCBGA989
TC7SH08FUF_SSOP5
Security Classification LC Future Center Secret Data
Issued Date 2012/07/01 Deciphered Date 2014/07/01
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Title PCH (5/9) PCI, USB, NVRAM
Size Custom Document Number NM-A041 Rev 1.A
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GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R265 1 @ 2 1K_0402_5% PCH_GPIO28

R274 1 @ 2 1K_0402_5% EC_SMI#

+3VS
R280 1 2 10K_0402_5%
R282 1 @ 2 10K_0402_5% WLBT_OFF_51#

For GC6

+3V_PCH
R288 1 2 10K_0402_5%
R290 1 @ 2 10K_0402_5% PCH_GPIO24

+3VS
R285 1 @ 2 10K_0402_5%
R284 1 @ 2 10K_0402_5% PCH_GPIO37

+3VS
R269 1 2 10K_0402_5% PCH_GPIO0
R270 1 2 10K_0402_5% PCH_GPIO1
R266 1 2 10K_0402_5% PCH_GPIO6
R344 1 2 10K_0402_5% EC_SCI#
R275 1 2 10K_0402_5% PCH_GPIO16
R268 1 2 10K_0402_5% DGPU_PWROK
R277 1 2 10K_0402_5% PCH_GPIO22
R346 1 2 10K_0402_5% PCH_GPIO34 GPIO34
R283 1 2 10K_0402_5% 3G_DET#
R287 1 2 10K_0402_5% 3G_OFF#
R289 1 2 10K_0402_5% GPS_OFF#
R291 1 2 10K_0402_5% PCH_GPIO49

+3V_PCH
R345 1 2 10K_0402_5% EC_SMI#
R271 1 2 10K_0402_5% PCH_GPIO12
R273 1 2 1K_0402_5% PCH_GPIO15
R347 1 2 10K_0402_5% PCH_GPIO28
R292 1 @ 2 10K_0402_5% PCH_GPIO57
R352 1 2 10K_0402_5% PCH_GPIO27

U3F

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 39 | FN_LED# | R359 1 2 0_0402_5% | PCH_GPIO0 | T7 | BMBUSY# / GPIO0 | P+ | TACH4 / GPIO68 |
| 39 | F1_LED# | R360 1 2 0_0402_5% | PCH_GPIO1 | A42 | TACH1 / GPIO1 | P+ | TACH5 / GPIO69 |
| 41 | EC_SCI# | | PCH_GPIO6 | H36 | TACH2 / GPIO6 | P+ | TACH6 / GPIO70 |
| 41 | EC_SMI# | | EC_SCI# | E38 | TACH3 / GPIO7 | P+ | TACH7 / GPIO71 |
| | | | EC_SMI# | C10 | GPIO8 | P+ | |
| 41 | EC_WAKE# | R178 1 2 0_0402_5% | PCH_GPIO12 | C4 | LAN_PHY_PWR_CTRL / GPIO12 | | |
| | | | PCH_GPIO15 | G2 | GPIO15 | P− | |
| | | | PCH_GPIO16 | U2 | SATA4GP / GPIO16 | | |
| 31,52 | DGPU_PWROK | | DGPU_PWROK | D40 | TACH0 / GPIO17 | | |
| 39 | F4_LED# | R361 1 2 0_0402_5% | PCH_GPIO22 | T5 | SCLOCK / GPIO22 | | |
| | | | PCH_GPIO24 | E8 | GPIO24 | | |
| 38 | mSATA_PCH | R293 1 2 0_0402_5% | PCH_GPIO27 | E16 | GPIO27 | P+ | |
| | | | PCH_GPIO28 | P8 | GPIO28 | P+ | |
| | | | PCH_GPIO34 | K1 | STP_PCI# / GPIO34 | | |
| 38 | 3G_DET# | | 3G_DET# | K4 | GPIO35 | | |
| 38 | WLBT_OFF_51# | | WLBT_OFF_51# | V8 | SATA2GP / GPIO36 | P− | |
| | | | PCH_GPIO37 | M5 | SATA3GP / GPIO37 | P− | |
| | | | PCH_GPIO38 | N2 | SLOAD / GPIO38 | | |
| 38 | 3G_OFF# | | 3G_OFF# | M3 | SDATAOUT0 / GPIO39 | | |
| 38 | GPS_OFF# | | GPS_OFF# | V13 | SDATAOUT1 / GPIO48 | | |
| | | | PCH_GPIO49 | V3 | SATA5GP / GPIO49 / TEMP_ALERT# | | |
| | | | PCH_GPIO57 | D6 | GPIO57 | | |

GPIO

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | C40 | ODD_EN# | | ODD_EN# | 36 |
| | | | B41 | PCH_GPIO69 | | | |
| | | | C41 | PCH_GPIO70 | | | |
| | | | A40 | CMOS_ON# | | CMOS_ON# | 32 |
| | | | P4 | | | GATEA20 | 41 |
| | | | AU16 | PCH_PECI_R | R307 1 @ 2 0_0402_5% | H_PECI | 41,5 |
| | | | P5 | KB_RST# | | KB_RST# | 41 |
| | | | AY11 | H_CPUPWRGD | | H_CPUPWRGD | 5 |
| | | | AY10 | R278 1 2 390_0402_5% H_THRMTRIP# | | H_THRMTRIP# | 5 |
| | | | | | | VGA_THRMTRIP# | 22 |
| | | | T14 | | | | |
| | | | AY1 | DF_TVS | | | |
| | | | AH8 | | | | |
| | | | AK11 | | | | |
| | | | AH10 | | | | |
| | | | AK10 | | | | |
| | | | P37 | | | | |

A20GATE
PECI
RCIN#
PROCPWRGD
THRMTRIP#
INIT3_3V#
DF_TVS
TS_VSS1
TS_VSS2
TS_VSS3
TS_VSS4
NC_1

CPU/MISC

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| T22 | A4 | VSS_NCTF_1 | | BG2 | VSS_NCTF_15 | | T18 |
| T24 | A44 | VSS_NCTF_2 | | BG48 | VSS_NCTF_16 | | T19 |
| T26 | A45 | VSS_NCTF_3 | | BH3 | VSS_NCTF_17 | | T20 |
| T28 | A46 | VSS_NCTF_4 | | BH47 | VSS_NCTF_18 | | T21 |
| T30 | A5 | VSS_NCTF_5 | | BJ4 | VSS_NCTF_19 | | T23 |
| T32 | A6 | VSS_NCTF_6 | | BJ44 | VSS_NCTF_20 | | T25 |
| T34 | B3 | VSS_NCTF_7 | | BJ45 | VSS_NCTF_21 | | T27 |
| T36 | B47 | VSS_NCTF_8 | | BJ46 | VSS_NCTF_22 | | T29 |
| T38 | BD1 | VSS_NCTF_9 | | BJ5 | VSS_NCTF_23 | | T31 |
| T40 | BD49 | VSS_NCTF_10 | | BJ6 | VSS_NCTF_24 | | T33 |
| T42 | BE1 | VSS_NCTF_11 | | C2 | VSS_NCTF_25 | | T35 |
| T44 | BE49 | VSS_NCTF_12 | | C48 | VSS_NCTF_26 | | T37 |
| T46 | BF1 | VSS_NCTF_13 | | D1 | VSS_NCTF_27 | | T39 |
| T48 | BF49 | VSS_NCTF_14 | | D49 | VSS_NCTF_28 | | T41 |
| | | | | E1 | VSS_NCTF_29 | | T43 |
| | | | | E49 | VSS_NCTF_30 | | T45 |
| | | | | F1 | VSS_NCTF_31 | | T47 |
| | | | | F49 | VSS_NCTF_32 | | T49 |

NCTF

PANTHER-POINT_FCBGA989

ODD_EN# R256 1 2 8.2K_0402_5%
R260 1 @ 2 8.2K_0402_5%

PCH_GPIO70 R258 2 1 10K_0402_5%
R262 1 @ 2 10K_0402_5%

CMOS_ON# R257 2 1 10K_0402_5%
R263 1 @ 2 10K_0402_5%

GATEA20 R272 1 2 10K_0402_5%
KB_RST# R276 1 2 10K_0402_5%

+1.8VS
R226 2.2K_0402_5%
DF_TVS R229 1 2 1K_0402_5% H_SNB_IVB# 5

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vcc when HIGH |
| | Set to Vss when LOW |

CLOSE TO THE BRANCHING POINT

For Edge code setting

| PCH_GPIO69 | PCH_GPIO38 | PCH_GPIO67 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Optimus |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | DIS |
| 0 | 1 | 1 | UMA |

+3VS
R259 10K_0402_5% @
R330 10K_0402_5% UMA@
R311 10K_0402_5% UMA@
R261 10K_0402_5%
R329 10K_0402_5% DIS@
R286 10K_0402_5% DIS@
PCH_GPIO69
PCH_GPIO38
PCH_GPIO67
PCH_GPIO67 14
(MB_ID_2)
(MB_ID_1)
(MB_ID_0)

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
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Title: PCH (6/9) GPIO, CPU, MISC

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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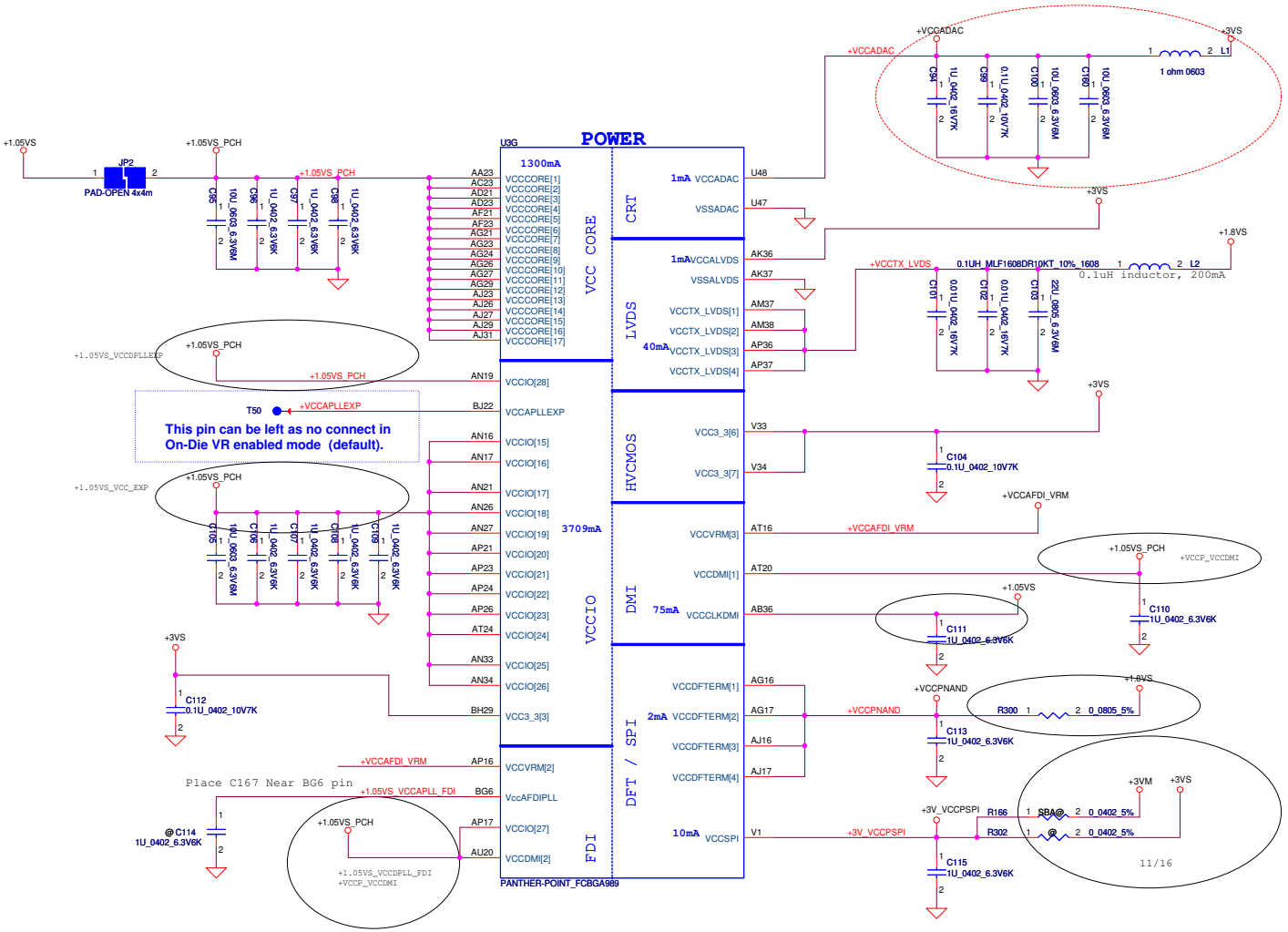


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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PCH (7/9) PWR

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Saturday, November 03, 2012 | Sheet 19 of 59

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U3J

PANTHER-POINT_FCBGA989

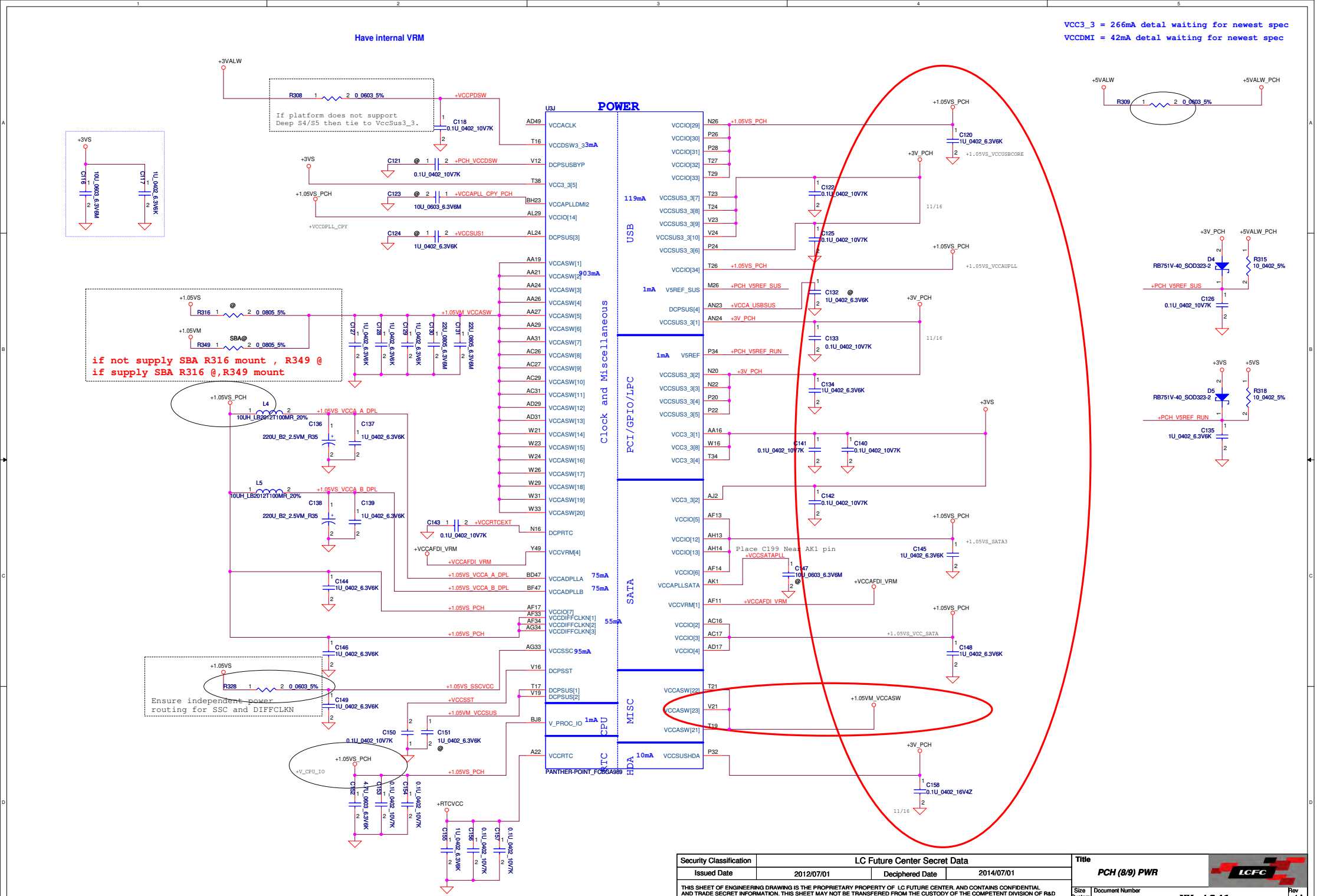
VCCACLK
VCCDSW3_3 3mA
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1]
VCCASW[2] 903mA
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA 75mA
VCCADPLLB 75mA
VCCIO[7]
VCCDIFFCLKN[1]
VCCDIFFCLKN[2]
VCCDIFFCLKN[3]
55mA
VCCSSC 95mA
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO 1mA
VCCRTC
VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCSUS3_3[7] 119mA
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[6]
VCCIO[34]
V5REF_SUS 1mA
DCPSUS[4]
VCCSUS3_3[1]
V5REF 1mA
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCC3_3[1]
VCC3_3[8]
VCC3_3[4]
VCC3_3[2]
VCCIO[5]
VCCIO[12]
VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
VCCSUSHDA 10mA

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA

Ensure independent power routing for SSC and DIFFCLKN

Place C199 Near AK1 pin

if not supply SBA R316 mount , R349 @
if supply SBA R316 @,R349 mount



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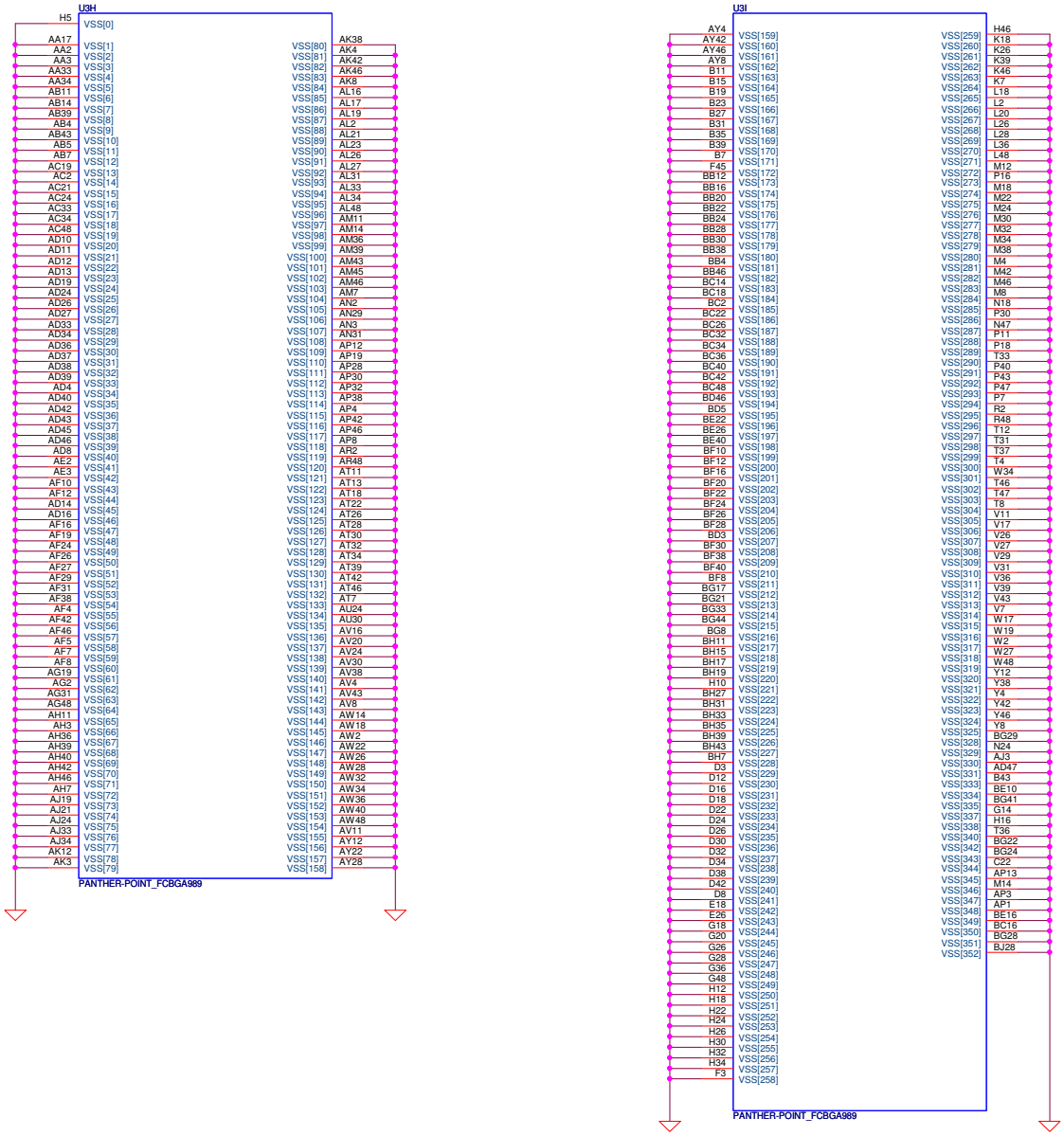
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PCH (8/9) PWR | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Saturday, November 03, 2012 | Sheet 20 of 59 | | |

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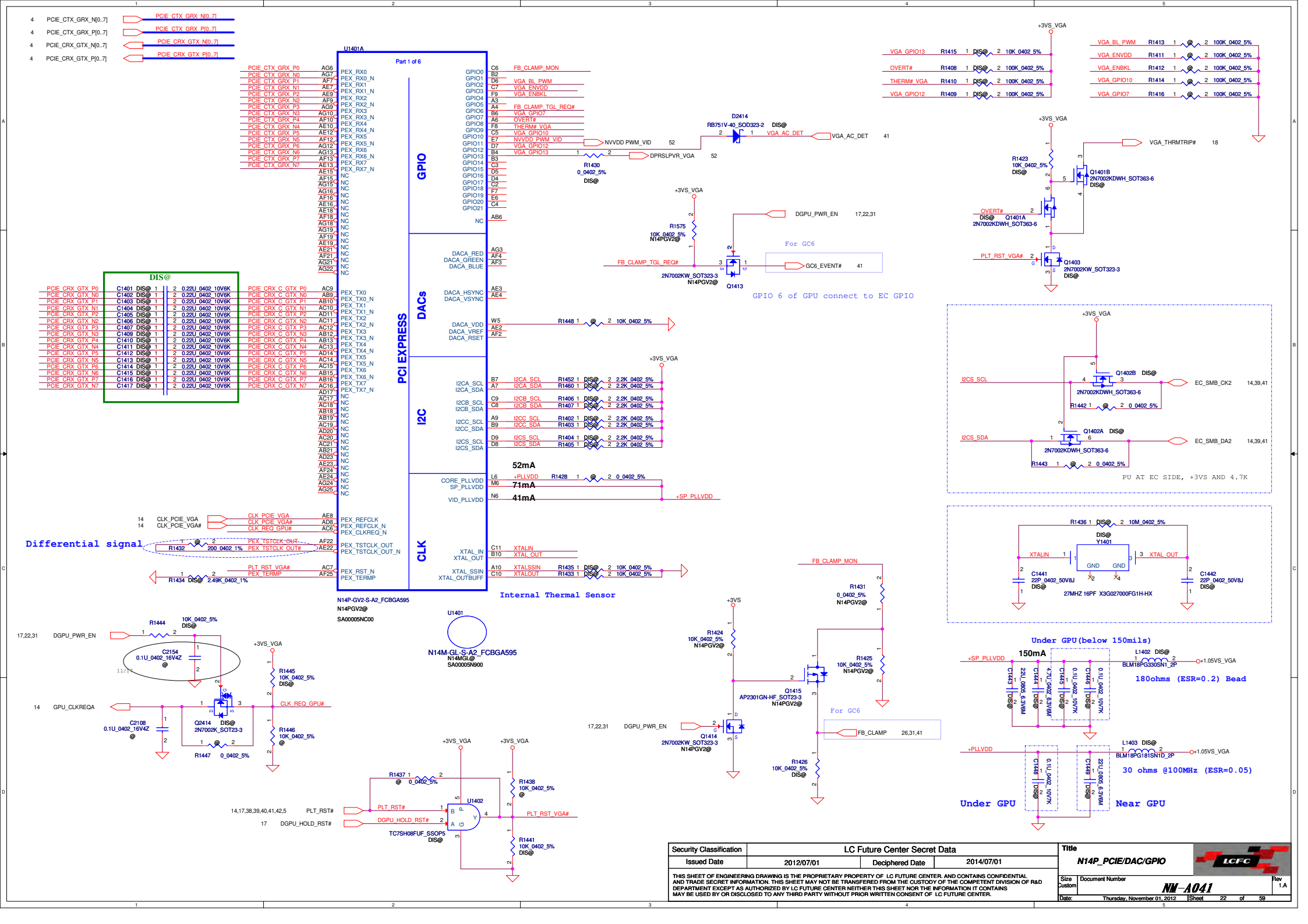
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PCH (9/9) VSS

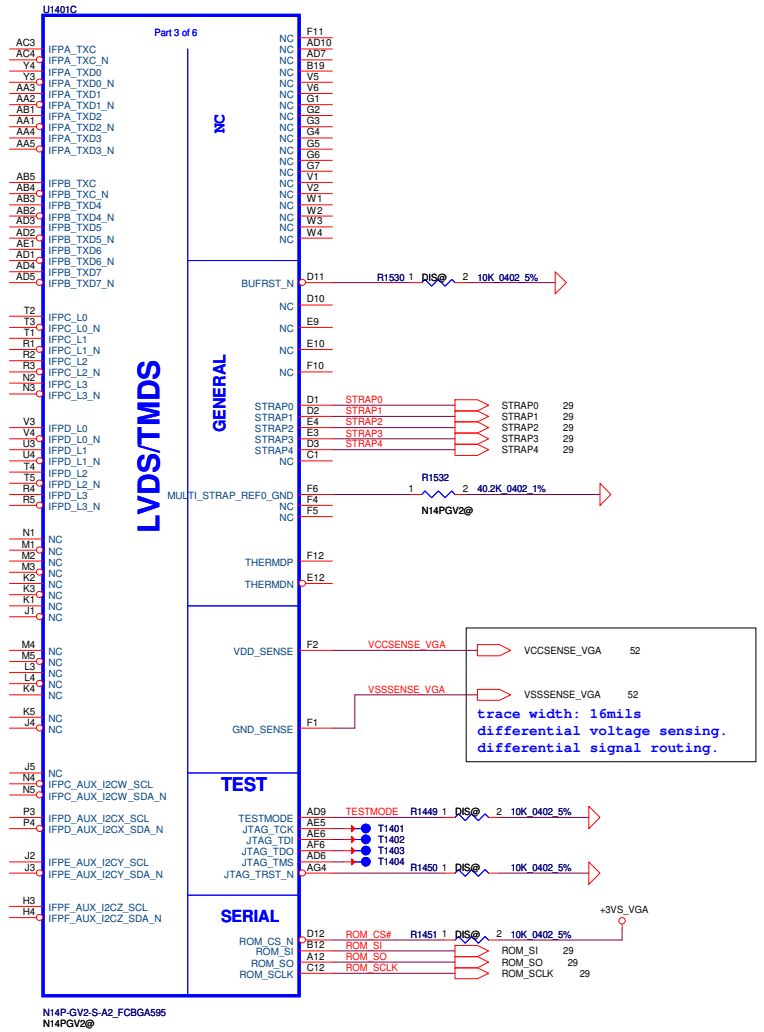
| | | |
|---|---|---|
| Size: Custom | Document Number: NM-A041 | Rev: 1.A |
| Date: Saturday, November 03, 2012 | Sheet 21 of 59 | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | N14P_PCIE/DAC/GPIO | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 22 of 59 | | |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: N14P_LVDS/HDMI/THERM

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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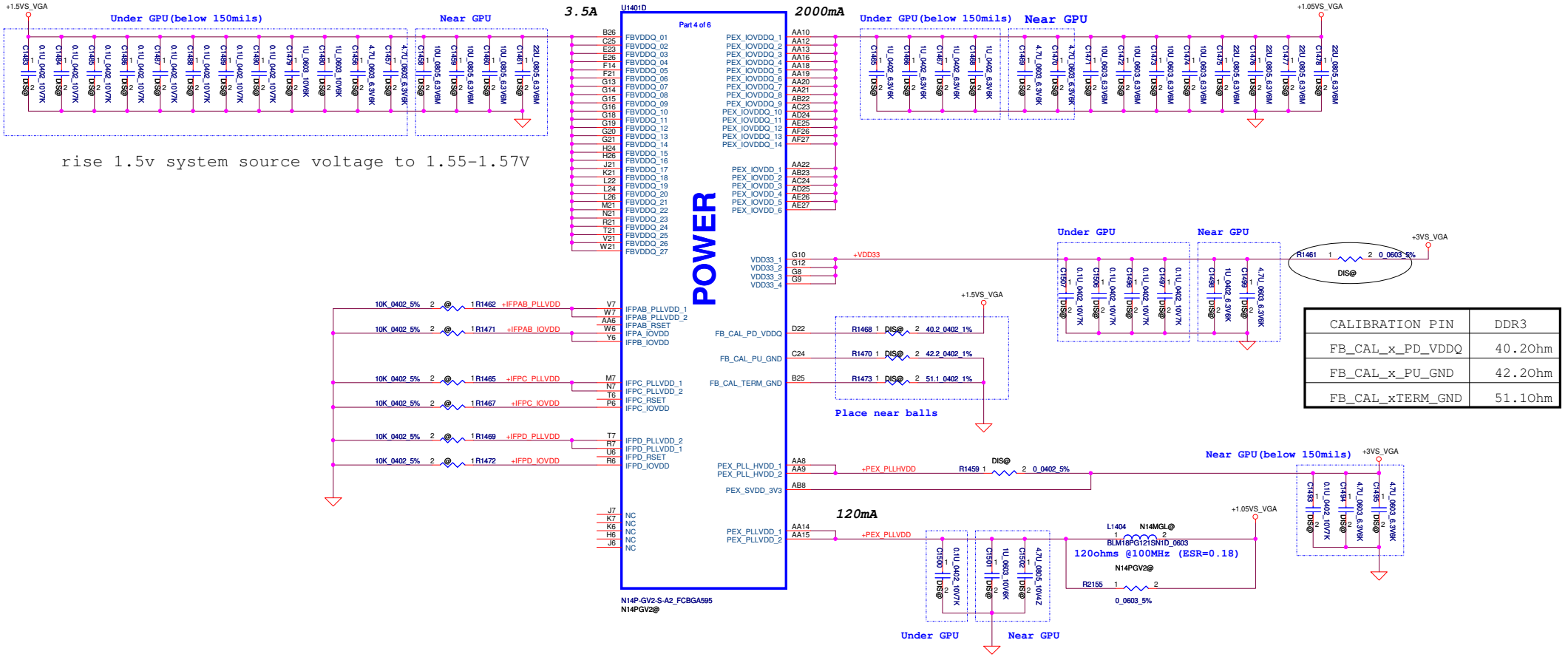


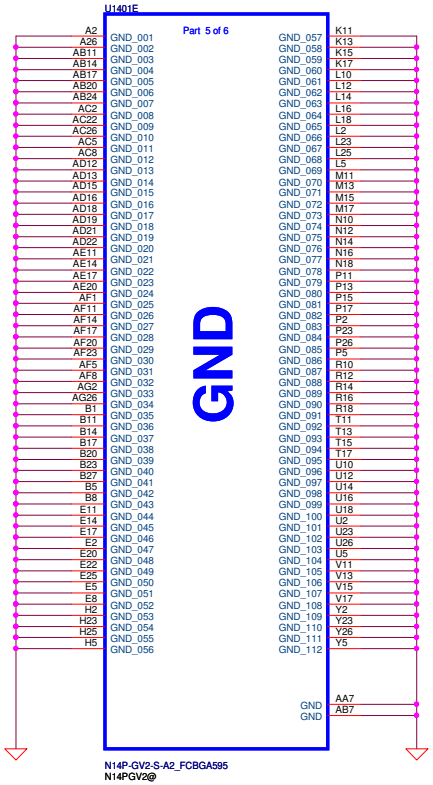

| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

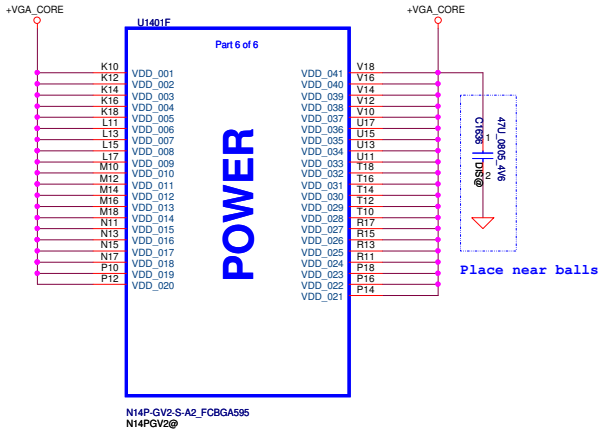


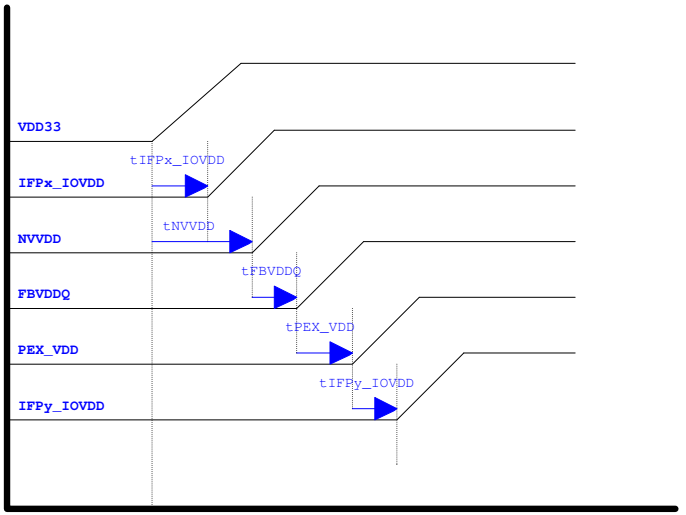
Title: N14P_Power

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 24 of 59




## NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

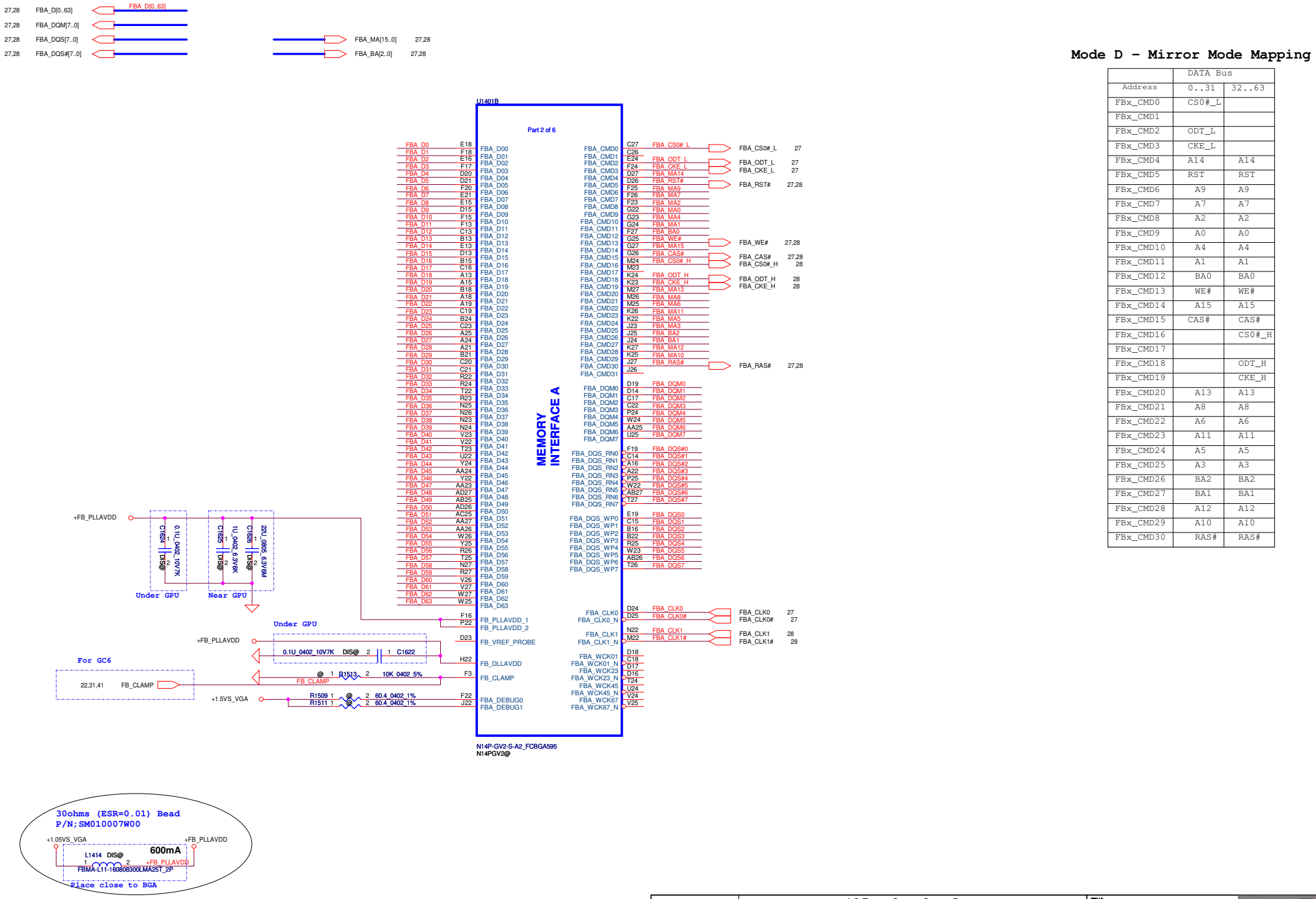
| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: N14P_VGA CORE, GND

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 25 of 59




## Mode D – Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |



| | | |
|---|---|---|
| Title | N14P_MEM Interface | |
| Size: Custom | Document Number: NM-A041 | Rev: 1.A |
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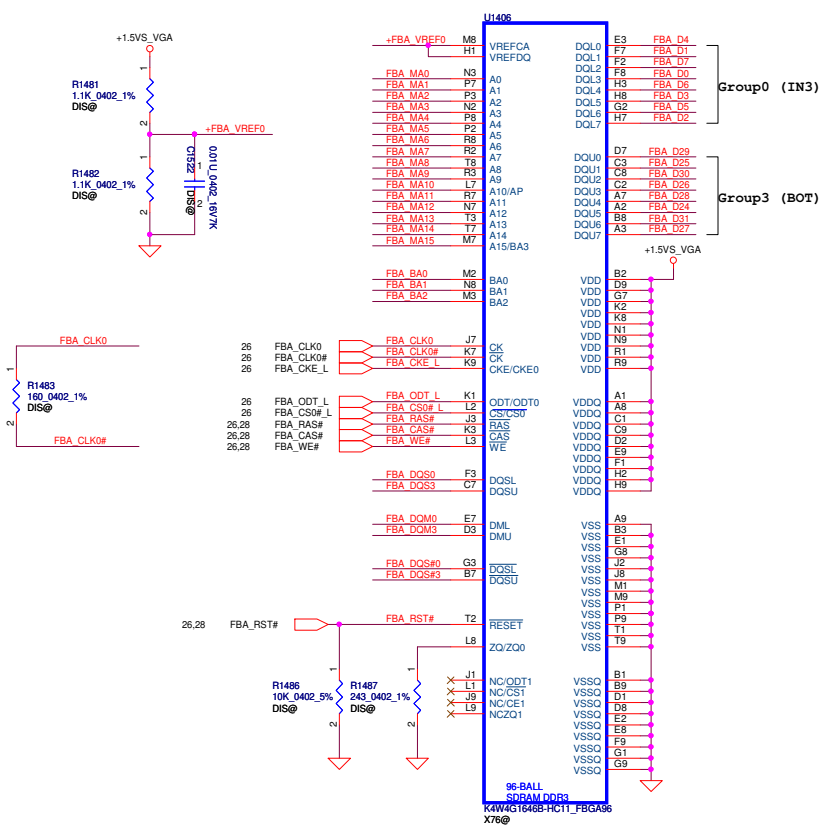
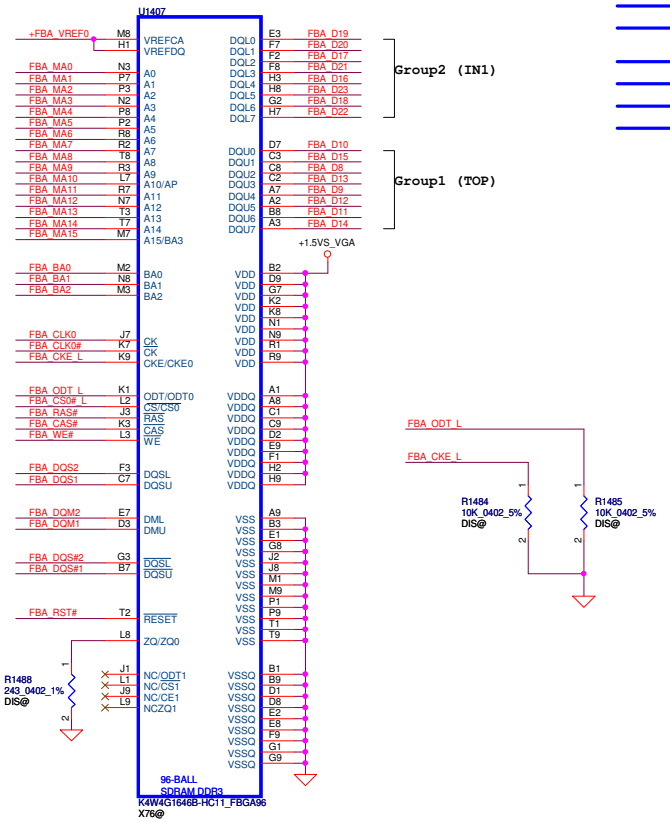
# Memory Partition A - Lower 32 bits



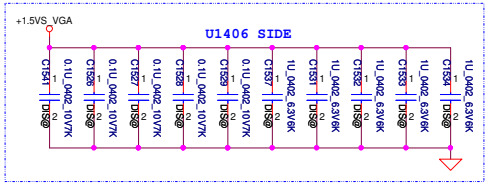


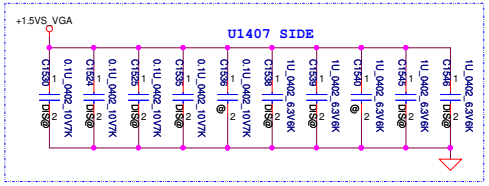





## Mode D - Mirror Mode Mapping

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |

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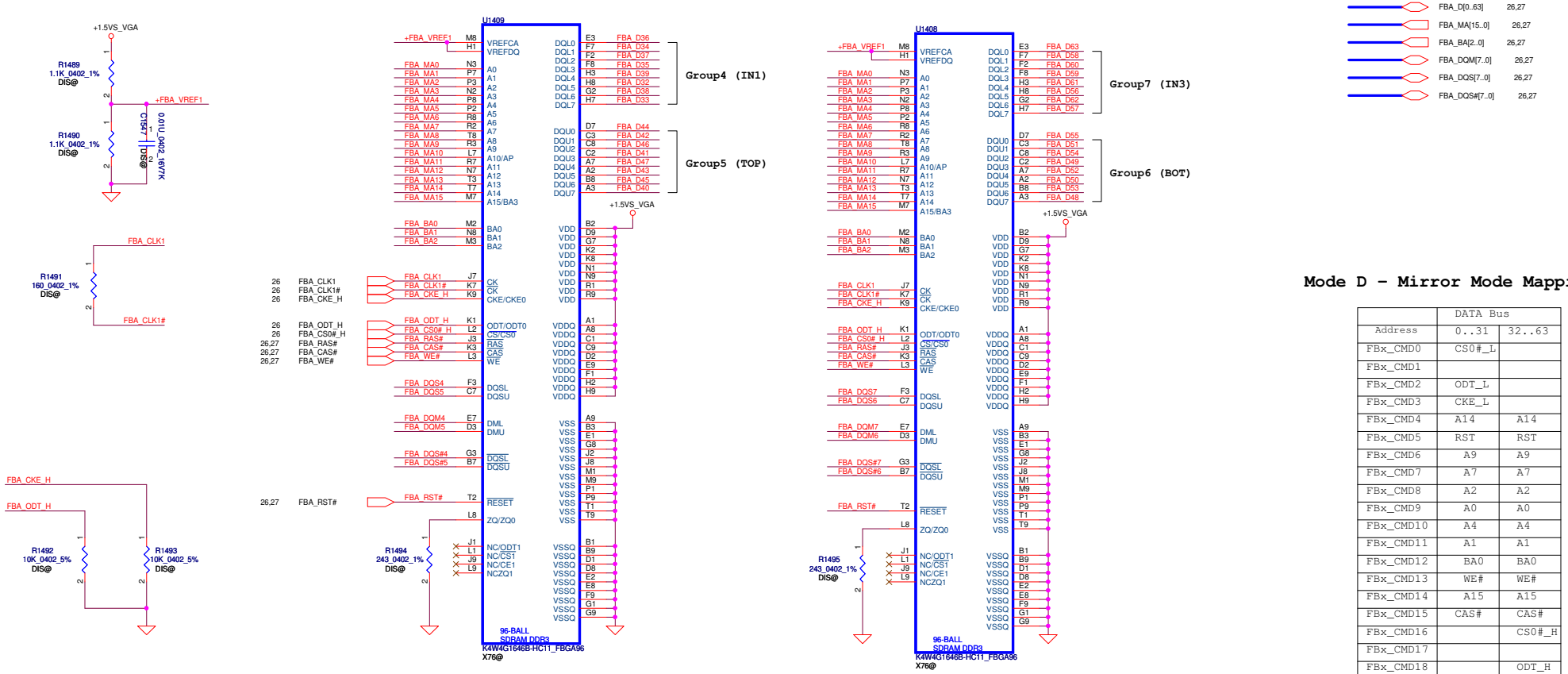
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| Title | | | |
|---|---|---|---|
| N14P_GDDR3_A Lower | | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 27 of 59 | | |

# Memory Partition A - Upper 32 bits

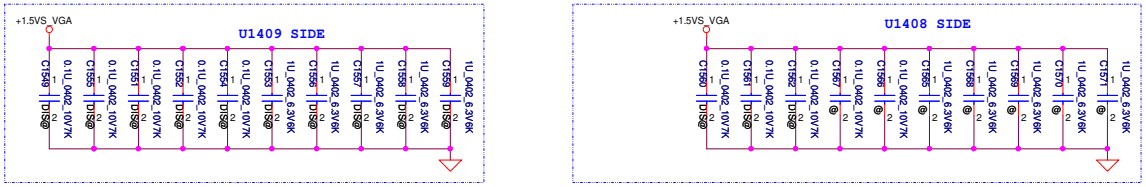






## Mode D - Mirror Mode Mapping

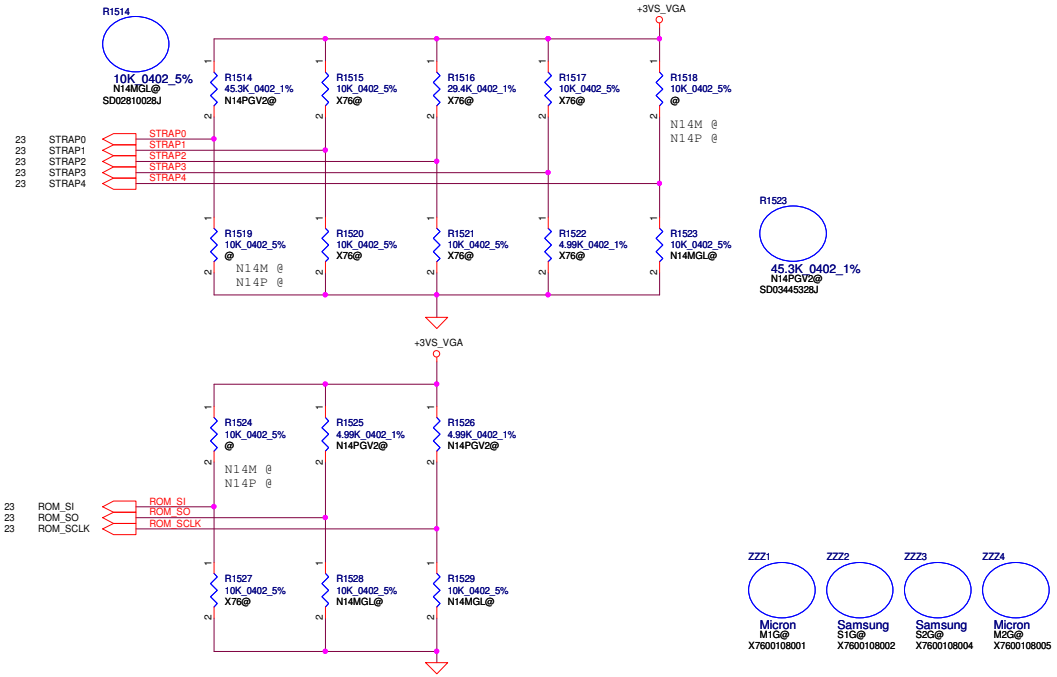
| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |




| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| Title | | |
|---|---|---|
| N14P_GDDR3_A Upper | | |
| Size: Custom | Document Number: NM-A041 | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 28 of 59 | |




| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|---|---|---|---|---|---|
| ROM_SCLK | +3VS_VGA | PCI_DEVID[4] | SUB_VENDOR | PCI_DEVID[5] | PEX_PLL_EN_TERM |
| ROM_SI | +3VS_VGA | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_VGA | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_VGA | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | +3VS_VGA | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP2 | +3VS_VGA | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | +3VS_VGA | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | +3VS_VGA | RESERVED | PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V |

| Resistor Values | Pull-up to +3VS_VGA | Pull-down to Gnd |
|---|---|---|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

| SUB_VENDOR | |
|---|---|
| 0 | No VBIOS ROM |
| 1 | BIOS ROM is present (Default) |

| 3GIO_PADCFG[3:0] | |
|---|---|
| 0110 | Gen1/Gen2 support only |
| 0000 | Gen3 support |

| FB[1:0] | |
|---|---|
| 0 | Reserved |
| 1 | Reserved |
| 2 | 256MB (Default) |
| 3 | Reserved |

| SMBUS_ALT_ADDR | |
|---|---|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

| VGA_DEVICE | |
|---|---|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

| PCIE_MAX_SPEED | |
|---|---|
| 0 | Limit booting to PCIE Gen1 |
| 1 | Allow booting to PCIE Gen 2/3 |

| PEX_PLL_EN_TERM | |
|---|---|
| 0 | Disable (Default) |
| 1 | Enable |

| USER Straps | |
|---|---|
| User[3:0] | |
| 1000-1100 | Customer defined |

| PCIE_SPEED_CHANGE_GEN3 | |
|---|---|
| 0 | Disable PCIE Gen3 operation |
| 1 | Enable PCIE Gen3 operation |

| DP_PLL_VDD33V | |
|---|---|
| 0 | Reserved |
| 1 | Default |

ZZZ6 MT41J128M16JT M1G@ SA00005M100
ZZZ7 K4W2G1646E S1G@ SA00005SH10
ZZZ8 K4W4G1646B S2G@ SA00005OM00
ZZZ9 MT41K256M16HA M2G@ SA0005ON00

For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K

| GPU | FB Memory gDDR3 | | ROM_SO | ROM_SCLK | ROM_SI | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N14P-GV2 | Samsung 1000MHz | K4W2G1646E-BC1A 128Mx16 | PU 5K | PU 5K | PD 45K | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K |
| | Micron 1000MHz | MT41J128M16JT-093G 128Mx16 | PU 5K | PU 5K | PD 30K | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K |
| | Samsung 900MHz | K4W4G1646B-HC11 256Mx16 | PU 5K | PU 5K | PD 20K | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K |
| | Micron 900MHz | MT41K256M16HA-107G 256Mx16 | PU 5K | PU 5K | PD 10K | PU 45K | PD 45K | PD 15K | PD 5K | PD 45K |

| GPU | FB Memory gDDR3 | | ROM_SO | ROM_SCLK | ROM_SI | STRAP0 | STRAP1 | STRAP2 | STRAP3 | STRAP4 |
|---|---|---|---|---|---|---|---|---|---|---|
| N14M-GL | Samsung 1000MHz | K4W2G1646E-BC1A 128Mx16 | PD 10K | PD 10K | PD 10K | PU 10K | PD 10K | PU 10K | PD 10K | PD 10K |
| | Hynix 1000MHz | H5TQ2G63DFR-N0C 128Mx16 | PD 10K | PD 10K | PD 10K | PD 10K | PU 10K | PU 10K | PD 10K | PD 10K |
| | Micron 1000MHz | MT41J128M16JT-093G 128Mx16 | PD 10K | PD 10K | PD 10K | PU 10K | PD 10K | PD 10K | PD 10K | PD 10K |
| | Samsung 900MHz | K4W4G1646B-HC11 256Mx16 | PD 10K | PD 10K | PD 10K | PU 10K | PU 10K | PD 10K | PU 10K | PD 10K |
| | Hynix 900MHz | H5TQ4G63MFR-11C 256Mx16 | PD 10K | PD 10K | PD 10K | PU 10K | PU 10K | PD 10K | PD 10K | PD 10K |
| | Micron 900MHz | MT41K256M16HA-107G 256Mx16 | PD 10K | PD 10K | PD 10K | PU 10K | PU 10K | PU 10K | PU 10K | PD 10K |

X76 X76

| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: N14P_MISC

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

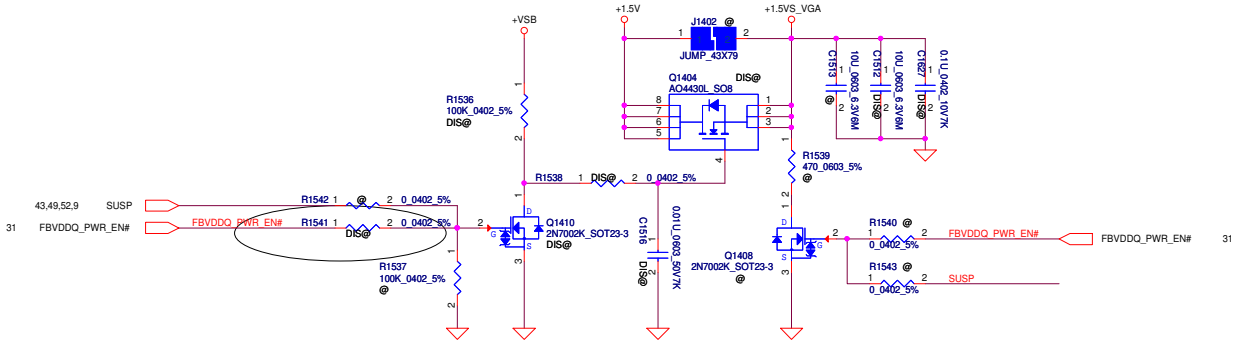


Title

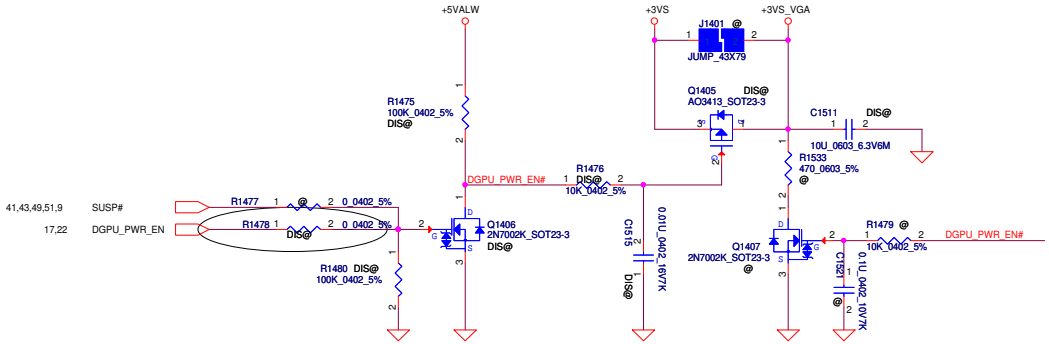
*XXX*

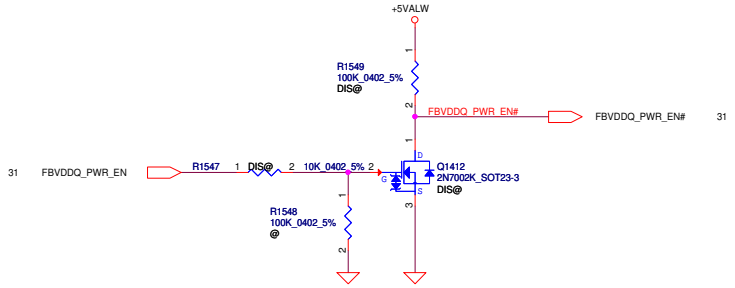
| | | |
|---|---|---|
| Size: Custom | Document Number: *NM-A041* | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 30 of 59 | |

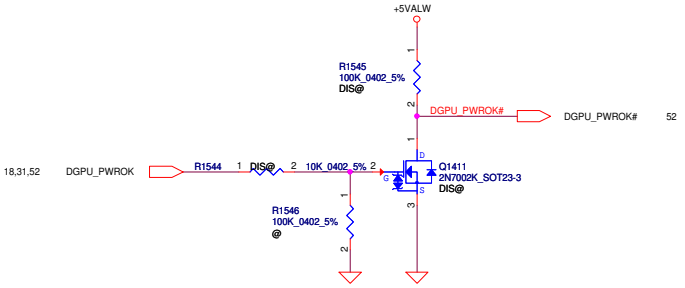
## +1.5V to +1.5VS_VGA

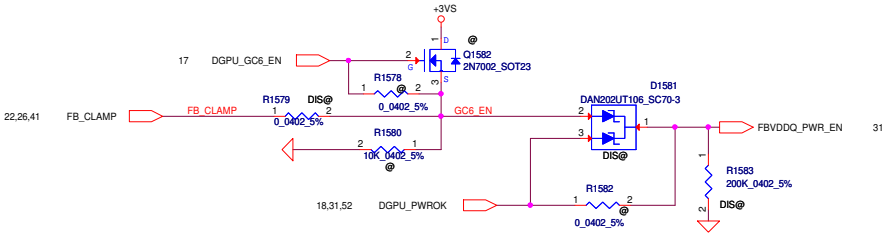



## +3VS to +3VS_VGA




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

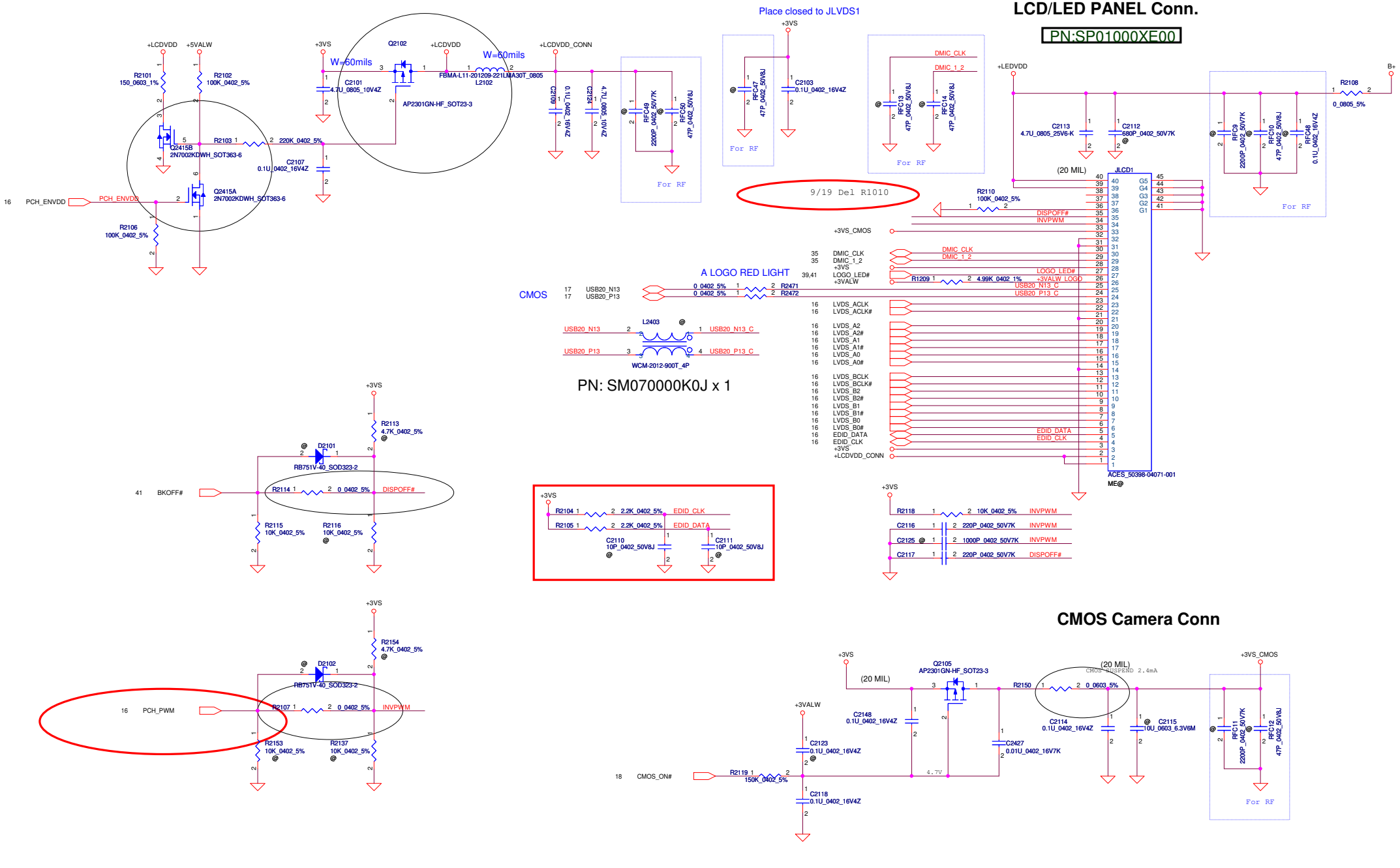


Title: N14P_+3VS/+1.05VS POWER

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

Date: Thursday, November 01, 2012 | Sheet 31 of 59

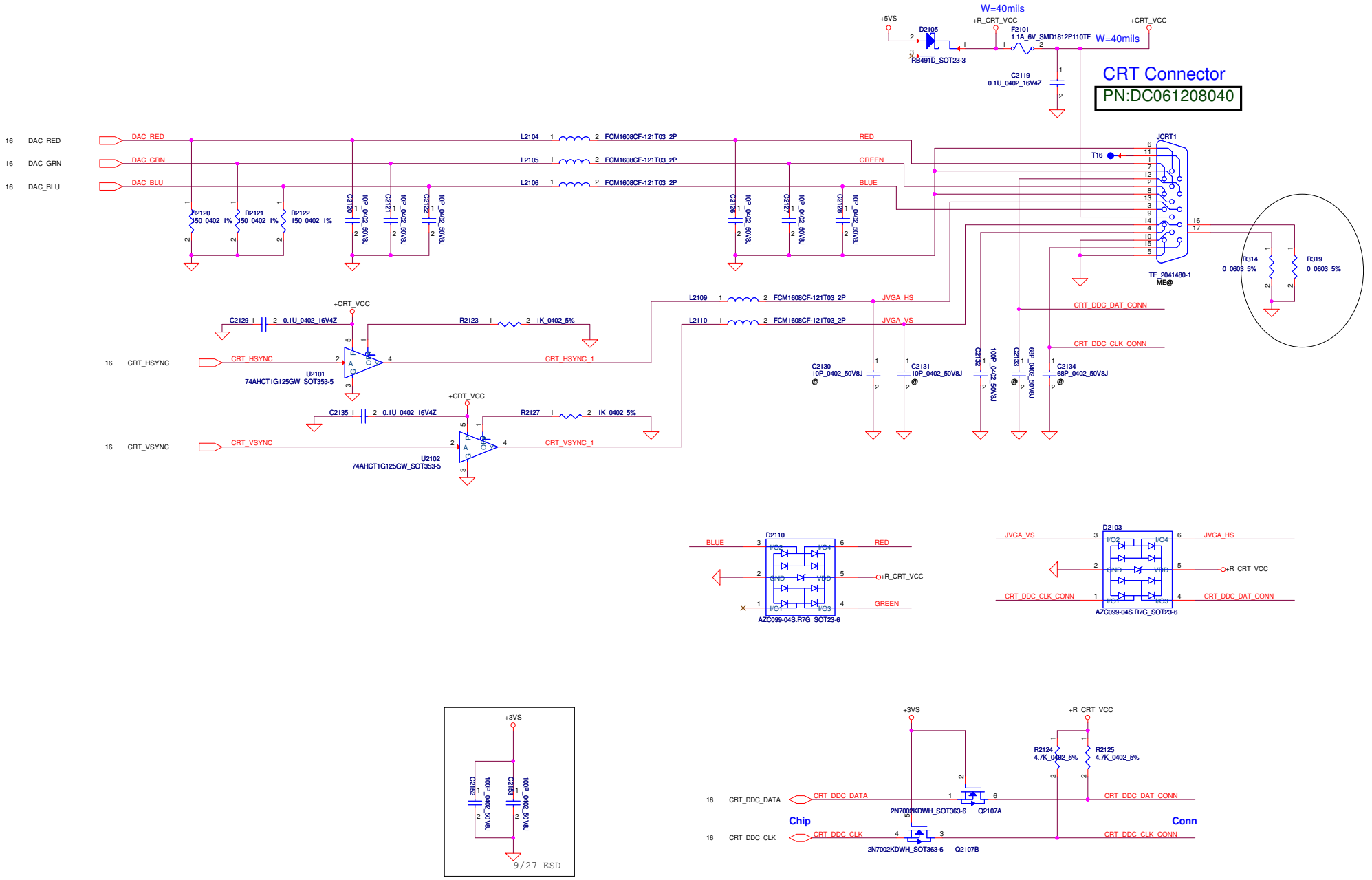
# LCD POWER CIRCUIT




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | LVDS CONN. | | |
| Size | Custom | Document Number | NM-A041 |
| Rev | 1.A | | |
| Date: | Saturday, November 03, 2012 | Sheet | 32 of 59 |




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | CRT CONN. | | |
| Size Custom | Document Number NM-A041 | | Rev 1.A |
| Date: Thursday, November 01, 2012 | Sheet 33 of 59 | | |

ESD request
Common mode choke 90ohm on these singals
Compal PN: SM070000K00
Vendor PN: WCM-2012-900T

16 PCH_DPB_P3 .1U_0402_16V7K C2145 HDMI_CLK+ R2128 0_0402_5% HDMI_R_CK+
L2111 WCM-2012HS-900T
16 PCH_DPB_N3 .1U_0402_16V7K C2144 HDMI_CLK- R2130 0_0402_5% HDMI_R_CK-
16 PCH_DPB_P2 .1U_0402_16V7K C2143 HDMI_TX0+ R2131 0_0402_5% HDMI_R_D0+
L2112 WCM-2012HS-900T
16 PCH_DPB_N2 .1U_0402_16V7K C2142 HDMI_TX0- R2132 0_0402_5% HDMI_R_D0-
16 PCH_DPB_P1 .1U_0402_16V7K C2141 HDMI_TX1+ R2133 0_0402_5% HDMI_R_D1+
L2113 WCM-2012HS-900T
16 PCH_DPB_N1 .1U_0402_16V7K C2140 HDMI_TX1- R2134 0_0402_5% HDMI_R_D1-
16 PCH_DPB_P0 .1U_0402_16V7K C2139 HDMI_TX2+ R2135 0_0402_5% HDMI_R_D2+
L2114 WCM-2012HS-900T
16 PCH_DPB_N0 .1U_0402_16V7K C2138 HDMI_TX2- R2136 0_0402_5% HDMI_R_D2-

HDMI_TX2- R2144 680_0402_5% HDMI_GND
HDMI_TX2+ R2152 680_0402_5%
HDMI_TX1- R2139 680_0402_5%
HDMI_TX1+ R2140 680_0402_5%
HDMI_TX0- R2141 680_0402_5%
HDMI_TX0+ R2142 680_0402_5%
HDMI_CLK- R2150 680_0402_5%
HDMI_CLK+ R2147 680_0402_5%
UMA 680_0402_5%
+3VS Q2110 2N7002K_SOT23-3

+3VS R2126 1M_0402_5% Q2109 2N7002K_SOT23-3
16 PCH_DPB_HPD R2129 20K_0402_5% C2137 220P_0402_50V7K @
+5VS D2106 RB491D-YS_SOT23-3 +HDMI_5V W=40mils
F2102 1.1A_6V_SMD1812P110TF +HDMI_5V_OUT W=40mils
C2136 0.1U_0402_16V4Z
R2149 0_0805_5%

HDMI Connector
PN:DC232001K00
JHDMI1 CONCR_099ATAC19NBLCNF ME@
HDMI_HPD HP_DET
+5V
HDMI_SDATA DDC/CEC_GND
HDMI_SCLK SDA
SCL
Reserved
HDMI_R_CK- CEC
CK-
HDMI_R_CK+ CK_shield
HDMI_R_D0- CK+
D0-
HDMI_R_D0+ D0_shield
HDMI_R_D1- D0+
D1-
HDMI_R_D1+ D1_shield
HDMI_R_D2- D1+
D2-
HDMI_R_D2+ D2_shield
D2+
GND GND GND GND
footprint check

+3VS +HDMI_5V
R2148 2.2K_0402_1% R2143 2.2K_0402_1% R2145 2.2K_0402_5% R2146 2.2K_0402_5%
16 HDMICLK_NB Q2111A 2N7002KDWH_SOT363-6 HDMI_SCLK
Chip Conn
16 HDMIDAT_NB Q2111B 2N7002KDWH_SOT363-6 HDMI_SDATA
Place closed to JHDMI1
C2146 @ 47P_0402_50V8J C2147 @ 47P_0402_50V8J

D2113 HDMI_HPD HDMI_SDATA HDMI_SCLK +HDMI_5V_OUT YSCLAMP0524P_SLP2510P8-10-9
9/27 ESD
D2112 HDMI_R_CK- HDMI_R_CK+ HDMI_R_D1- HDMI_R_D1+ YSCLAMP0524P_SLP2510P8-10-9
D2108 HDMI_R_D2- HDMI_R_D2+ HDMI_R_D0- HDMI_R_D0+ YSCLAMP0524P_SLP2510P8-10-9

| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: HDMI CONN.
Size: Custom
Document Number: NM-A041
Rev: 1.A
Date: Thursday, November 01, 2012
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Layout Note:Path from +5VS to Pin12, Pin15 must be very low resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powerd by a rail that is not removed unless AC power is removed.
*DSH page42 has more detail.

EC Beep
ICH Beep
PC Beep
Combo Jack detect (normal open)
Decoupling CAP
Internal DMIC
Internal SPEAKER
EMI
Internal Speaker
DC030008W00
Headphone
Port B
Port A
External MIC
Near Pin 29
Near Pin 18
Near Pin 2
Near Pin 27
Near Pin 7
Near Pin 28
Near Pin 3
Near Pin 26
Near Pin 17
Near Pin 12
Near Pin 15
Near Pin 21
For RF
EAPD active low
0=power down ex AMP
1=power up ex AMP
10K only needed if supply to VAUX_3.3 is removed during system re-start.
Sense resistors must be connected same power that is used for VAUX_3.3
AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.
Changed from 5.1ohm to 15ohm for "zi zi"noise.
EMC request
Bead 120ohm on these singals
JV PN: SM01001670J
Vendor PN: FBMA-L11-160808-121LMT
Rdc < 0.05 ohms
Rated Current > 2A
Width 20 mil
9/28 RF modify
U1101
CX20671-21Z_QFN40_6X6
SINGA_2SJ2326-001111
ACES_85204-02001
ACES_85205-02001

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: HD Audio Codec_CX20671
Size: Custom
Document Number: NM-A041
Rev: 1.A
Date: Thursday, November 01, 2012
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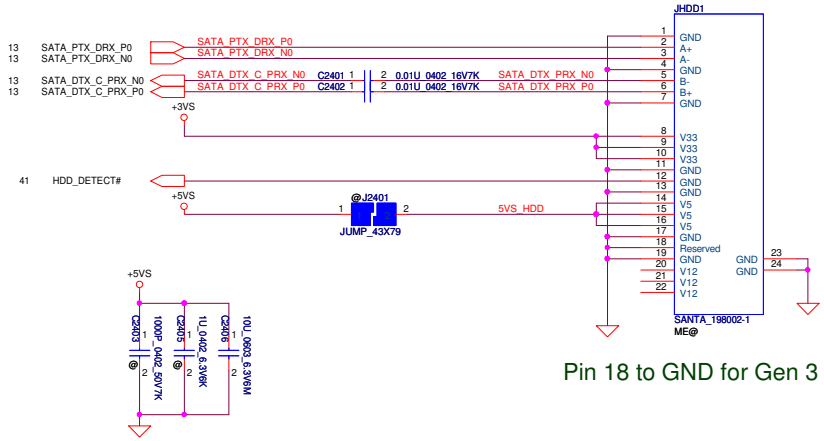
## SATA HDD CONN.

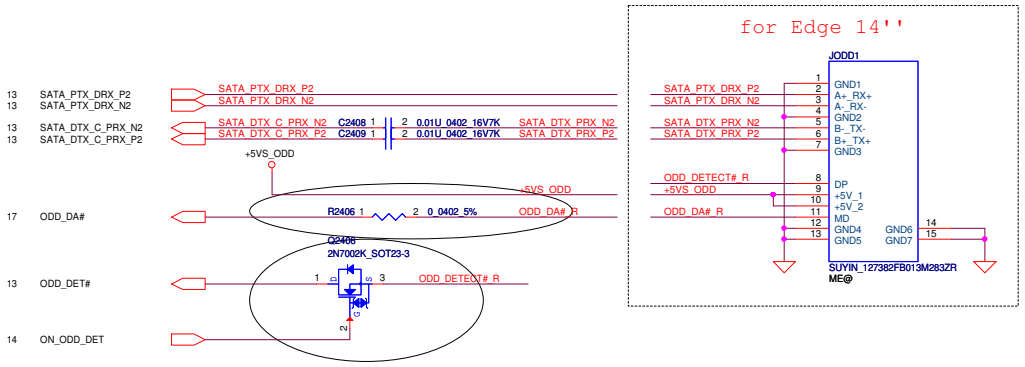
PN:SP01001HE00

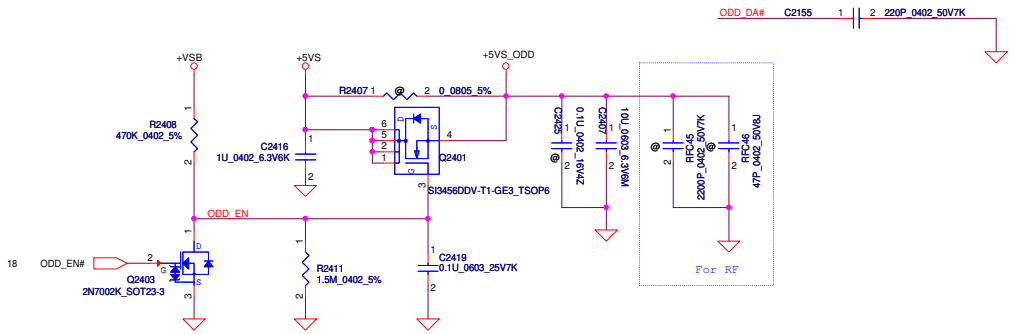



Pin 18 to GND for Gen 3

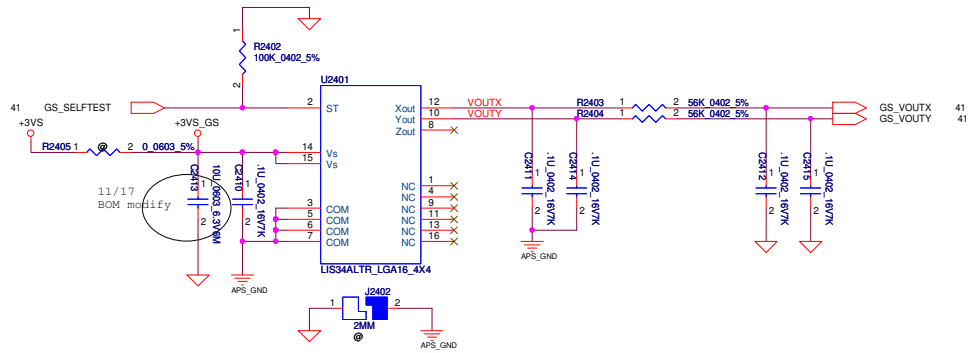
## SATA ODD CONN.

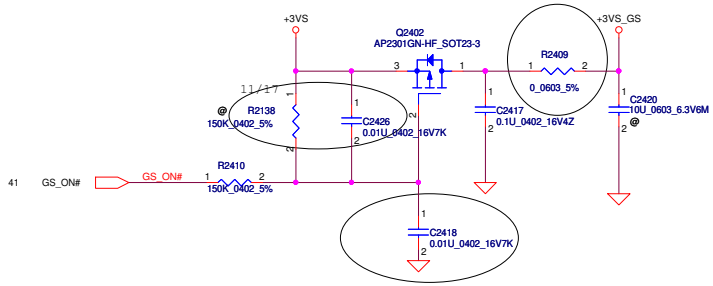
PN:SP01000TU10




## APS G-Sensor



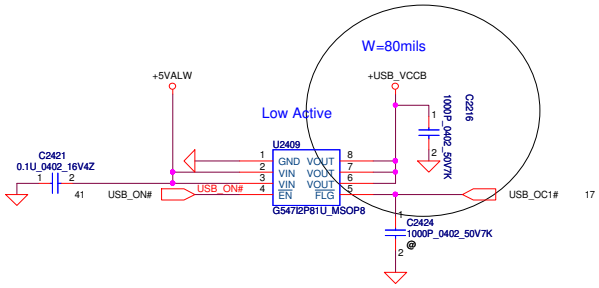



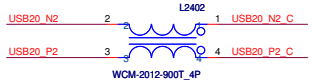

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



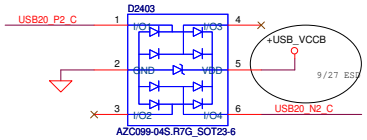
| | | | |
|---|---|---|---|
| Title | HDD/ODD/Card reader/G-Sen | | |
| Size | Custom | Document Number | NM-A041 |
| Rev | 1.A | | |
| Date: | Thursday, November 01, 2012 | Sheet | 36 of 59 |

# USB 3.0 Conn.

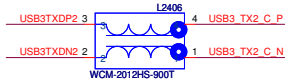



PN: SM070000K00 x 1

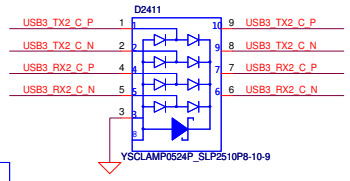



PN: SC300001G00

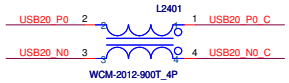



PN: SM070001S00 x 2

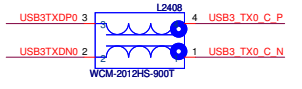



PN:DC233008A00

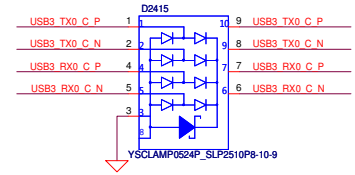



PN: SM070000K00 x 1

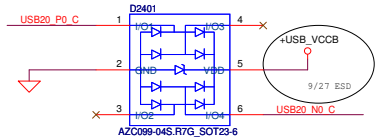



PN: SM070001S00 x 2




PN:DC233008A00




PN: SC300001G00

| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| Title | | | |
|---|---|---|---|
| USB 3.0 CONN. | | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 37 of 59 | | |

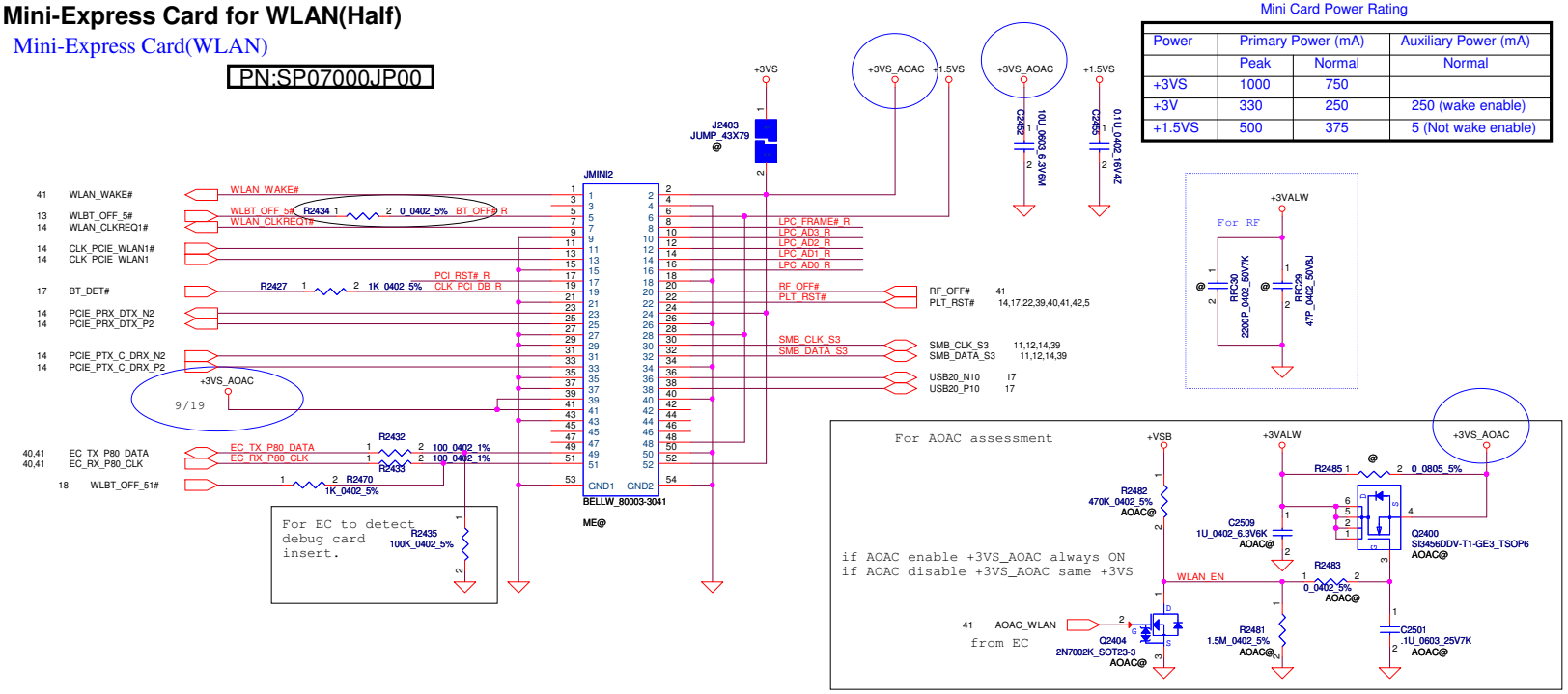
# Mini-Express Card for WLAN(Half)

Mini-Express Card(WLAN)

PN:SP07000JP00

Mini Card Power Rating

| Power | Primary Power (mA) | | Auxiliary Power (mA) |
|---|---|---|---|
| | Peak | Normal | Normal |
| +3VS | 1000 | 750 | |
| +3V | 330 | 250 | 250 (wake enable) |
| +1.5VS | 500 | 375 | 5 (Not wake enable) |

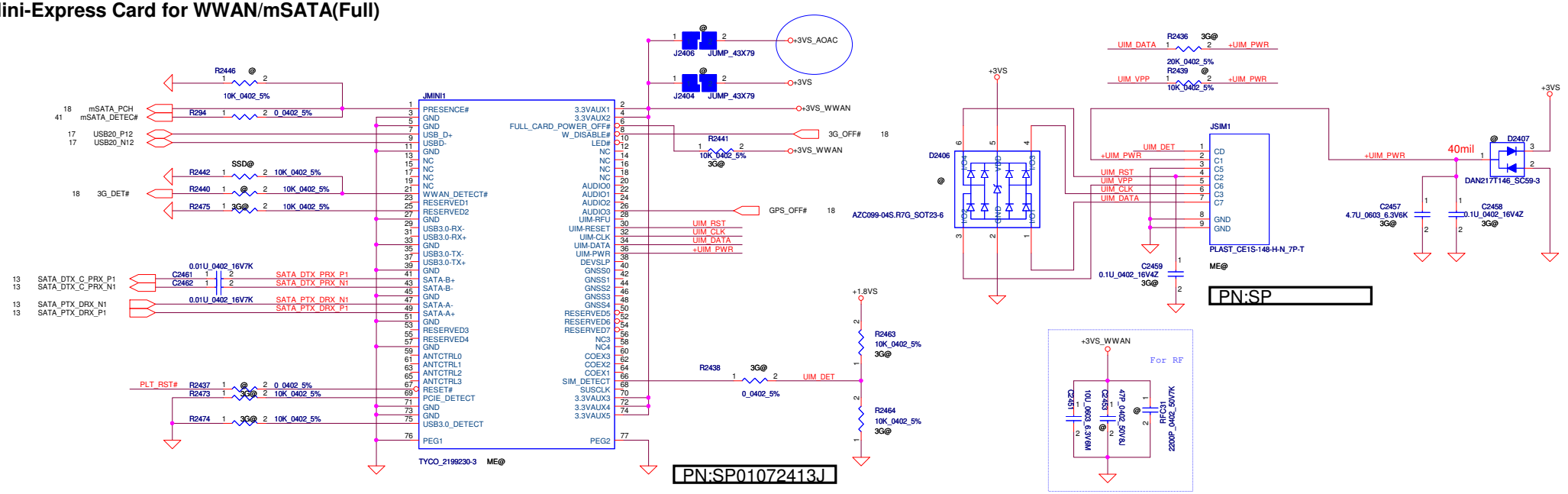



**Reserve for SW mini-pcie debug card.**
**Series resistors closed to KBC side.**

| | | | | |
|---|---|---|---|---|
| LPC_FRAME# R | R2449 | LPC_FRAME# | LPC_FRAME# | 13,40,41 |
| LPC_AD3_R | R2455 | LPC_AD3 | LPC_AD3 | 13,40,41 |
| LPC_AD2_R | R2456 | LPC_AD2 | LPC_AD2 | 13,40,41 |
| LPC_AD1_R | R2457 | LPC_AD1 | LPC_AD1 | 13,40,41 |
| LPC_AD0_R | R2458 | LPC_AD0 | LPC_AD0 | 13,40,41 |
| PCI_RST# R | R2459 | PLT_RST# | | |
| CLK_PCI_DB_R | R2428 | CLK_PCI_DB | CLK_PCI_DB | 17,40 |

# BT Connector

# Mini-Express Card for WWAN/mSATA(Full)



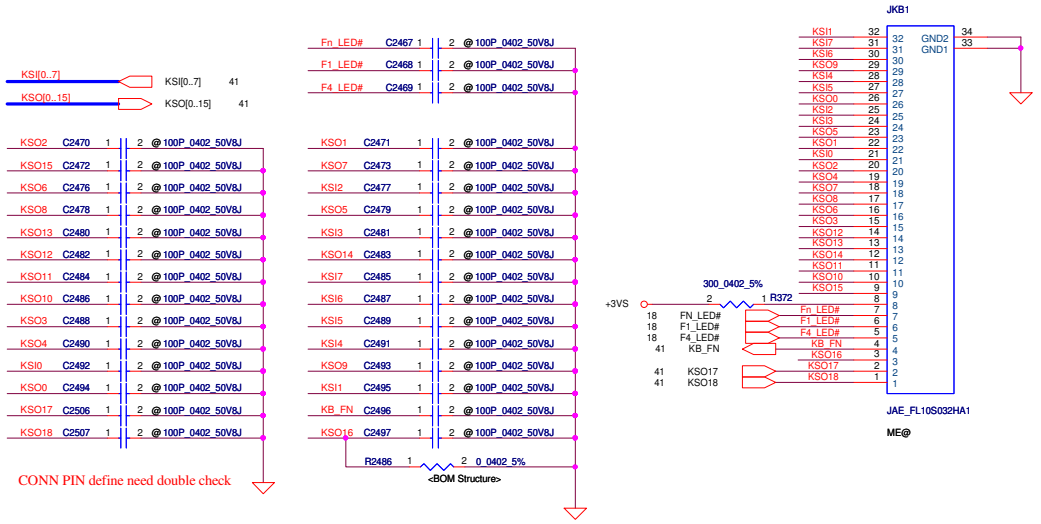

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PCIe-WLAN and WWAN_mSATA | | |
| Size | Custom | Document Number | NM-A041 |
| Rev | 1.A | | |
| Date: | Thursday, November 01, 2012 | Sheet | 38 of 59 |

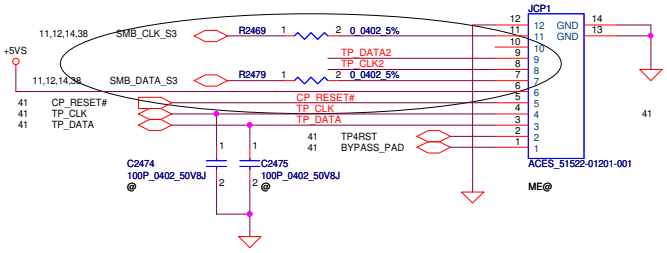
## INT_KBD Conn.

PN:SP011208010



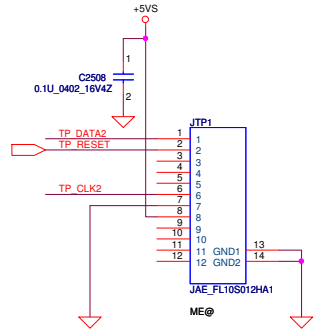

## Click pad

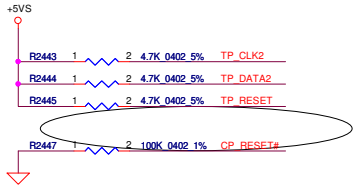
PN:SP01001BX00

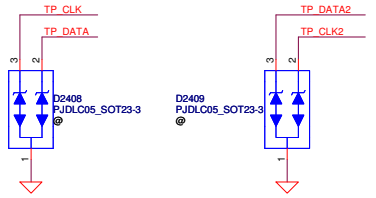



## Track point

PN:SP01120802J

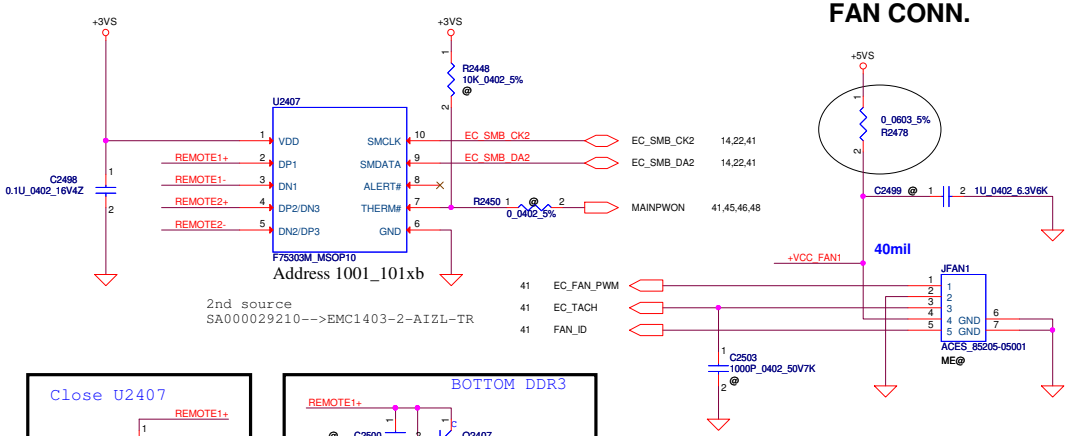



PN: SCA00000A0J X 2

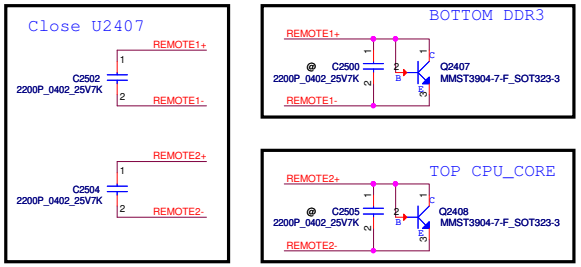
## Fintek thermal sensor placed near by TOP DDR3




## FAN CONN.




PN:SP02000U900



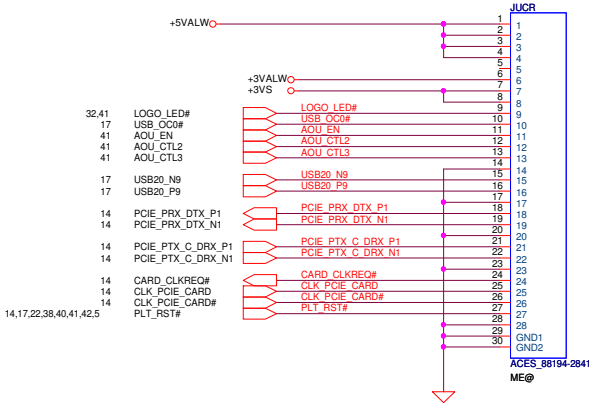







REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

## Audio+CR Board




need change to 28 Pin

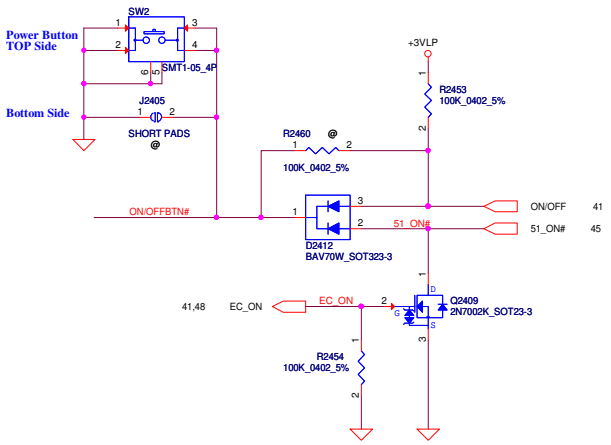
| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | KB/TP/Thermal Sensor/Audio | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 39 of 59 | | |

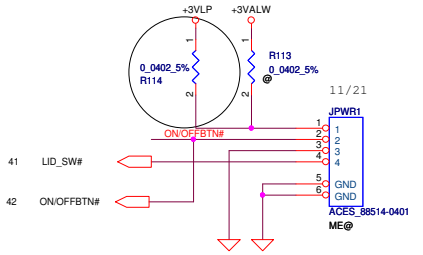
## Power Button

*ON/OFF switch*



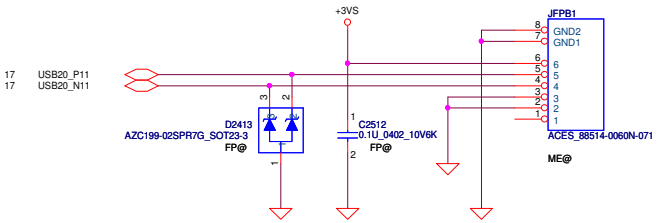

## Power Button CONN.

PN:SP01000R400

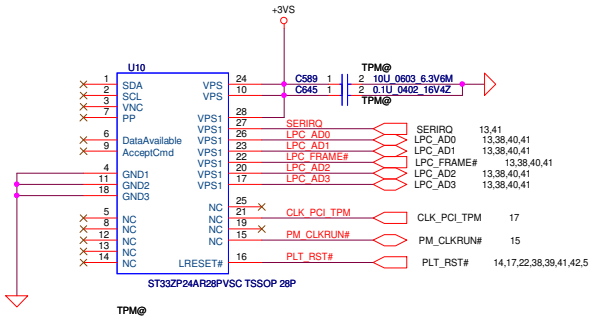


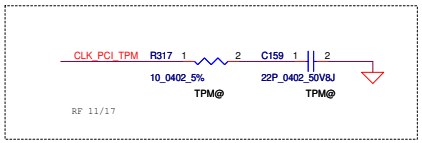

## Finger Print Board

PN:SP01000R400

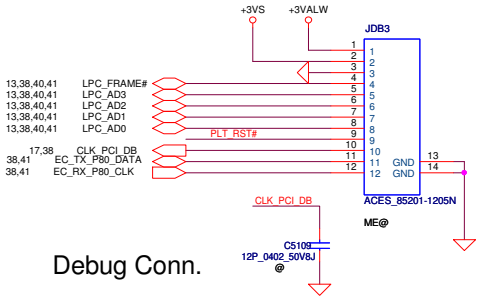



## TPM

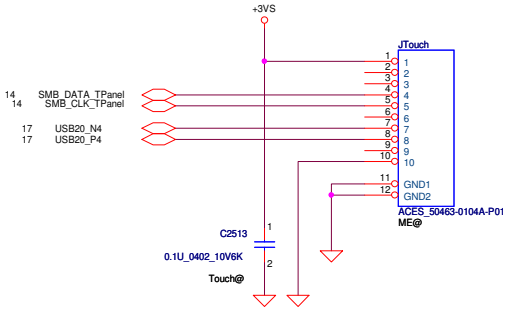



## Debug Conn.




## Touch Panel




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PWR S/B/LID SW/TPM/RJ45 | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Wednesday, November 07, 2012 | Sheet 40 of 59 | | |

| Vcc | 3.3V +/- 5% |
|---|---|
| R2210 | 100K +/- 1% |

| Board ID | R2213 | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | Phase |
|---|---|---|---|---|---|
| 0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | FVT |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | |
| 4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | |
| 5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V | |

SD028330280 S RES 1/16W 33K +-5% 0402
SD028180280 S RES 1/16W 18K +-5% 0402
SD02882018J S RES 1/16W 8.2K +-5% 0402
SD028470180 S RES 1/16W 4.7K +-5% 0402
SD028240280 S RES 1/16W 24K +-5% 0402

Definition FAN_ID (pin 5)
PCC 00
AVC 01
Delta 02

U2201 KB9012QF A3 LQFP 128P_14X14

PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI

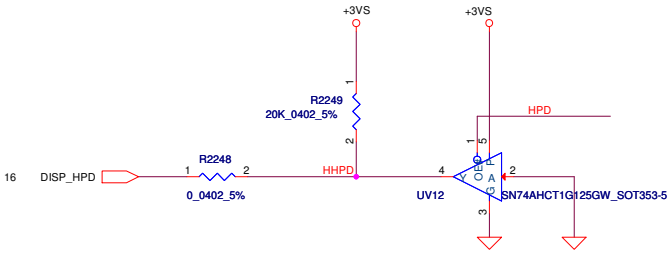
| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

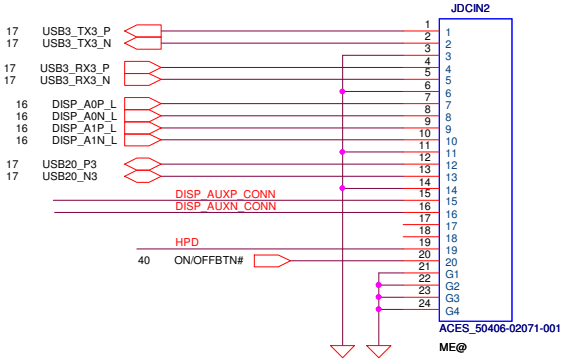


Title: EC ENE-KB9012

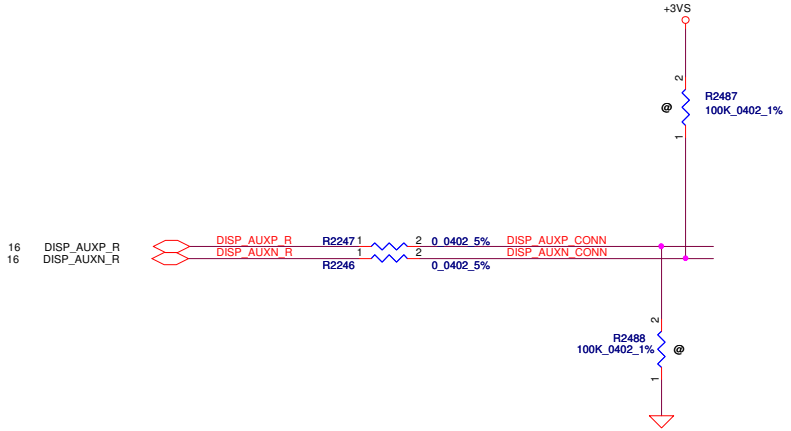
Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 41 of 59

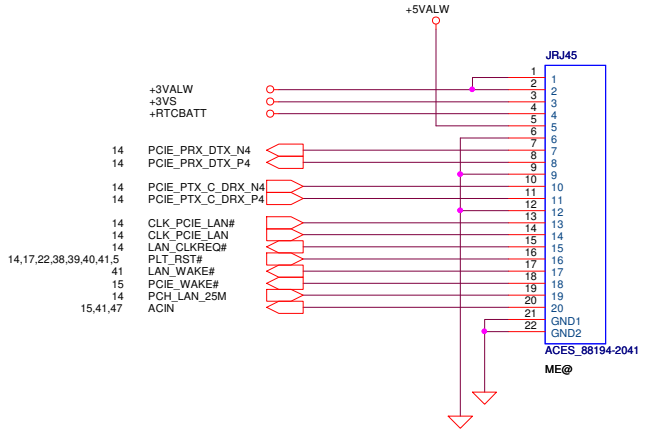



## DP/TMDS Switch Circuit (1)




## RJ45 Board

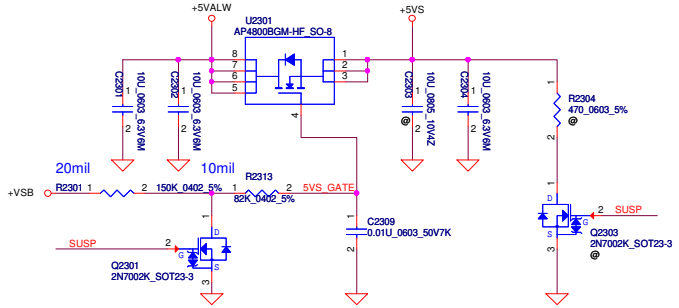



| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |

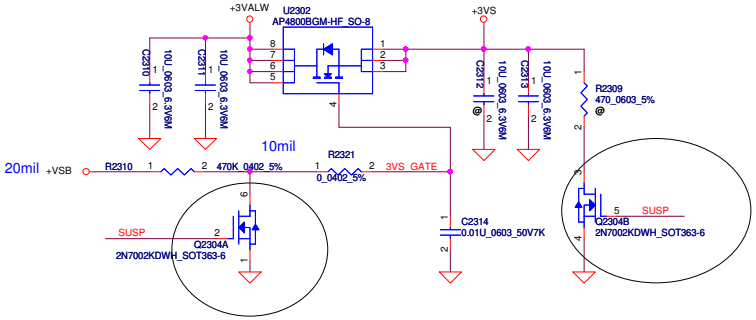


| | | | |
|---|---|---|---|
| Title | DP U3 CONN. | | |
| Size: Custom | Document Number: NW-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 42 of 59 | | |

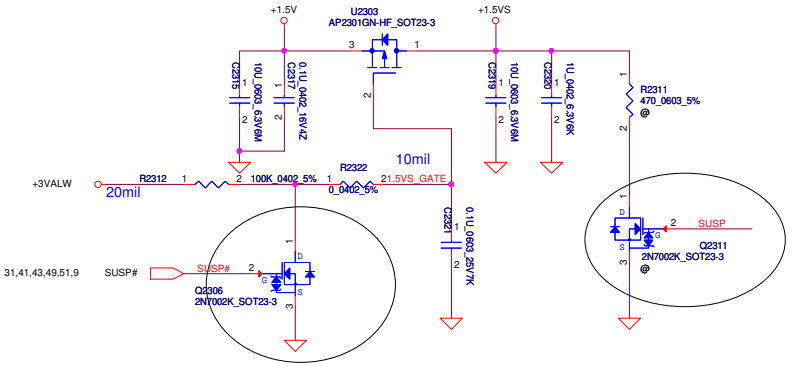
## +5VALW TO +5VS

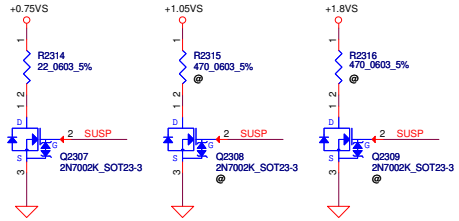


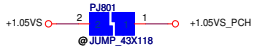

## +3VALW TO +3VS




## +1.5V to +1.5VS

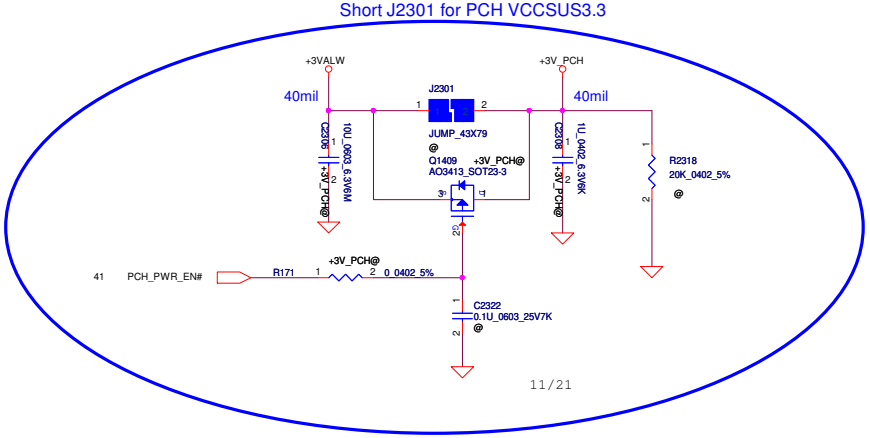


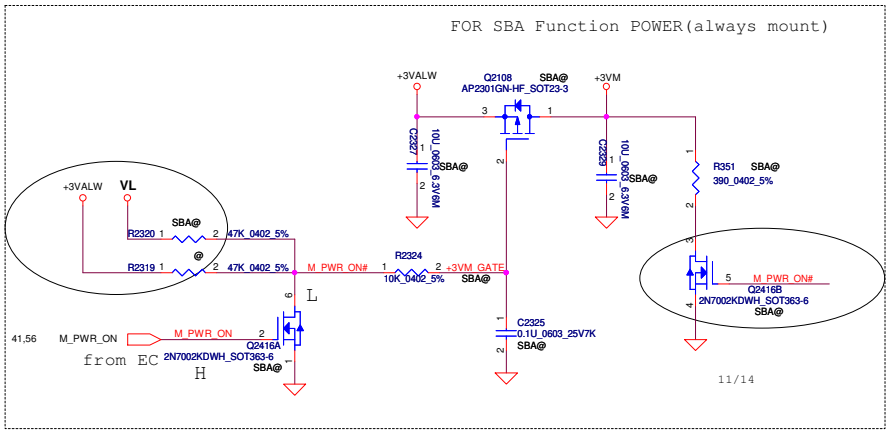



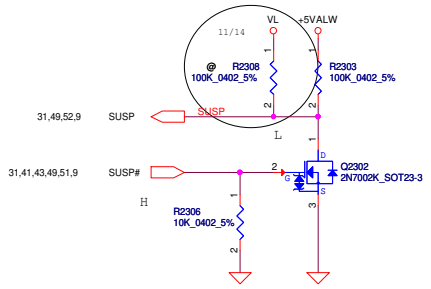




## +3VALW TO +3VALW(PCH AUX Power)

Short J2301 for PCH VCCSUS3.3



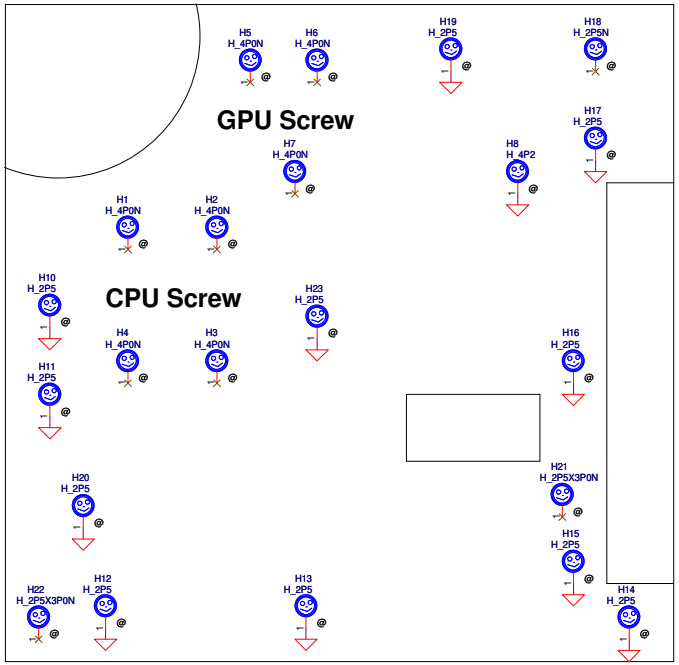



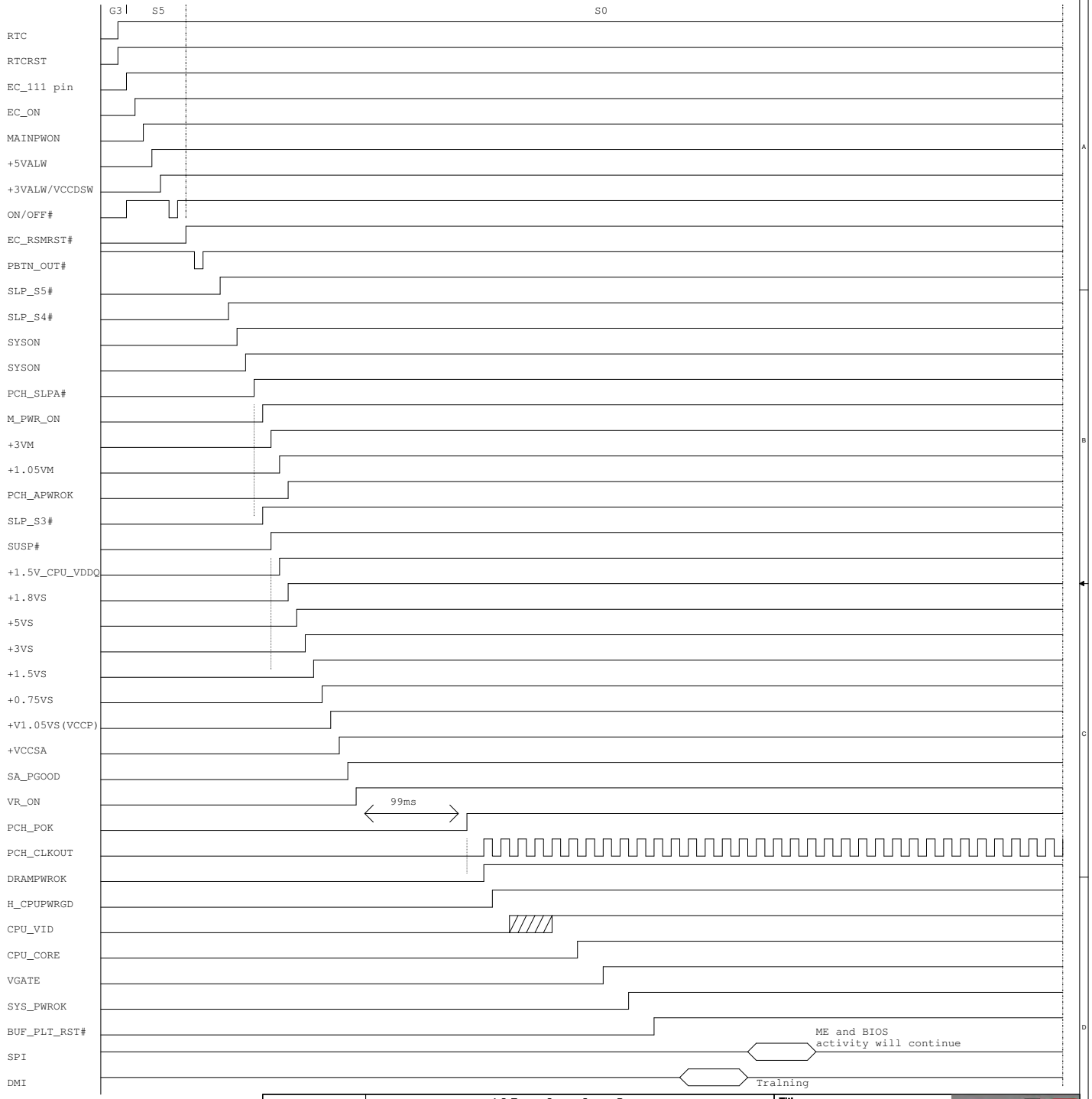

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | DC INTERFACE | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 43 of 59 | | |

## Screw Hole & FD

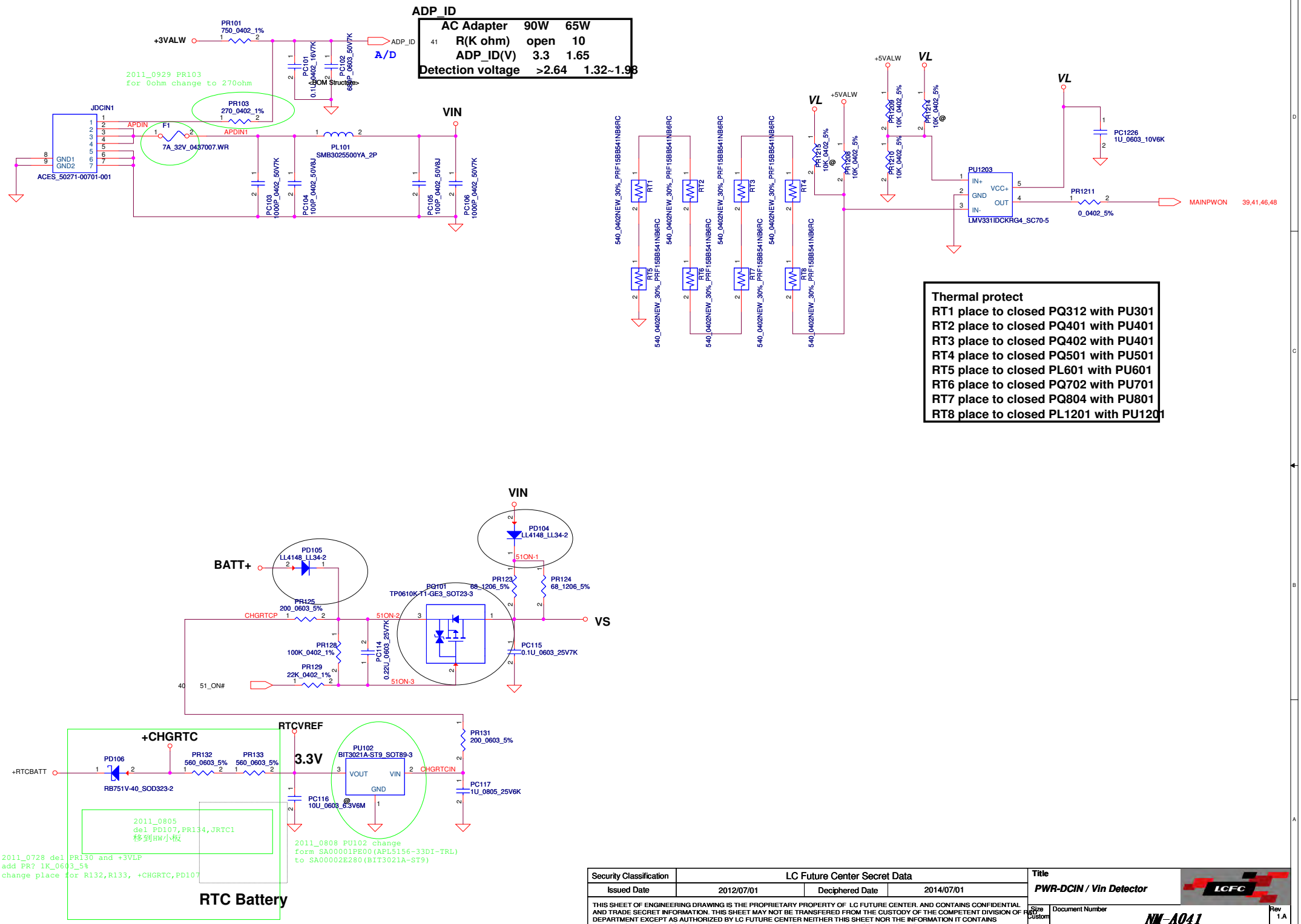




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | Screw Hole | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Monday, November 05, 2012 | Sheet 44 of 59 | | |



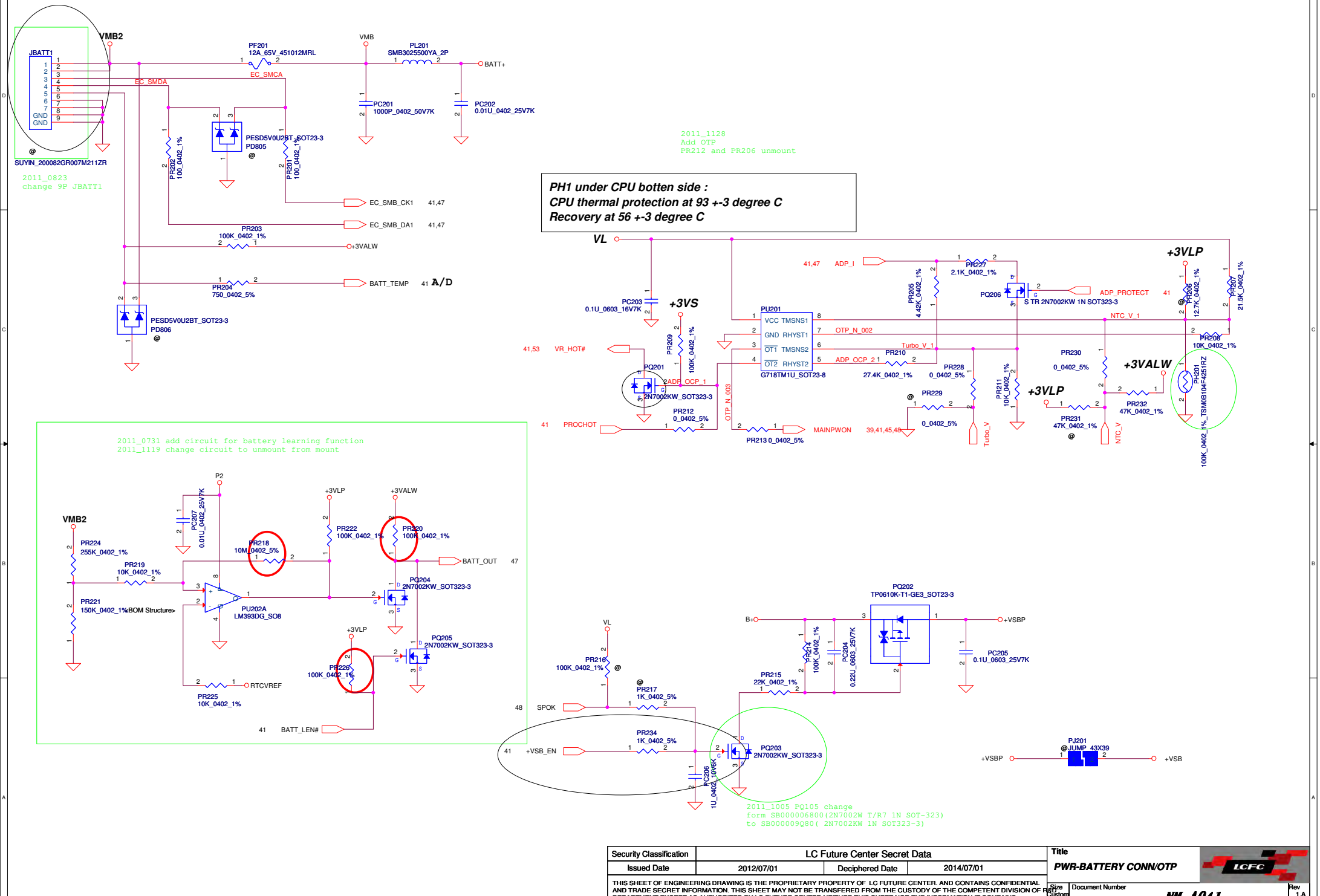

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-DCIN / Vin Detector

| Size | Document Number | Rev |
|---|---|---|
| Custom | NW-A041 | 1.A |

Date: Thursday, November 01, 2012 Sheet 45 of 59



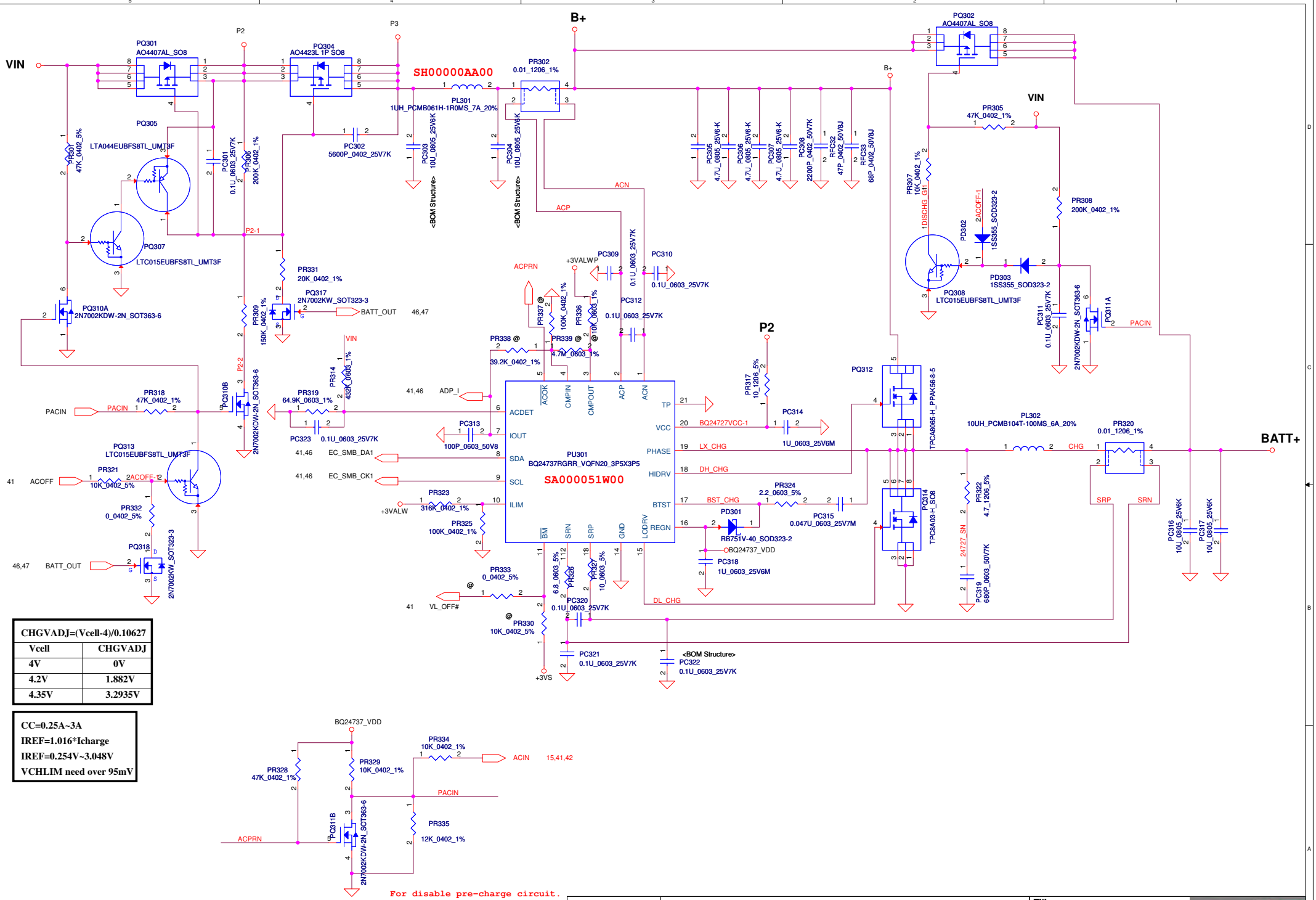

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-BATTERY CONN/OTP

| Size | Document Number | Rev |
|---|---|---|
| Custom | NW-A041 | 1.A |

Date: Thursday, November 01, 2012 Sheet 46 of 59




| CHGVADJ=(Vcell-4)/0.10627 | |
|---|---|
| Vcell | CHGVADJ |
| 4V | 0V |
| 4.2V | 1.882V |
| 4.35V | 3.2935V |

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

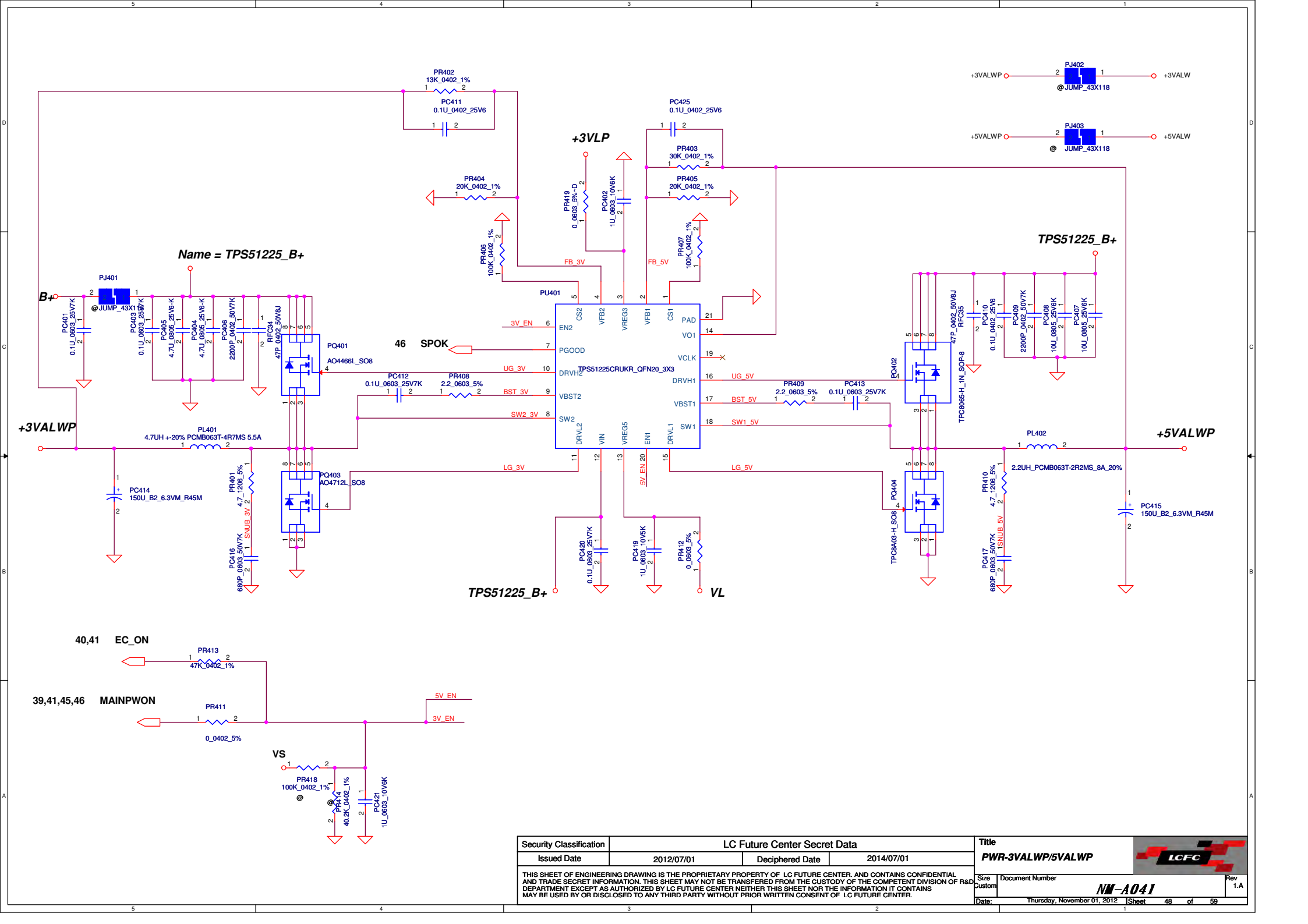
| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-CHARGER-BQ24737

Size: Custom | Document Number: NW-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 47 of 59



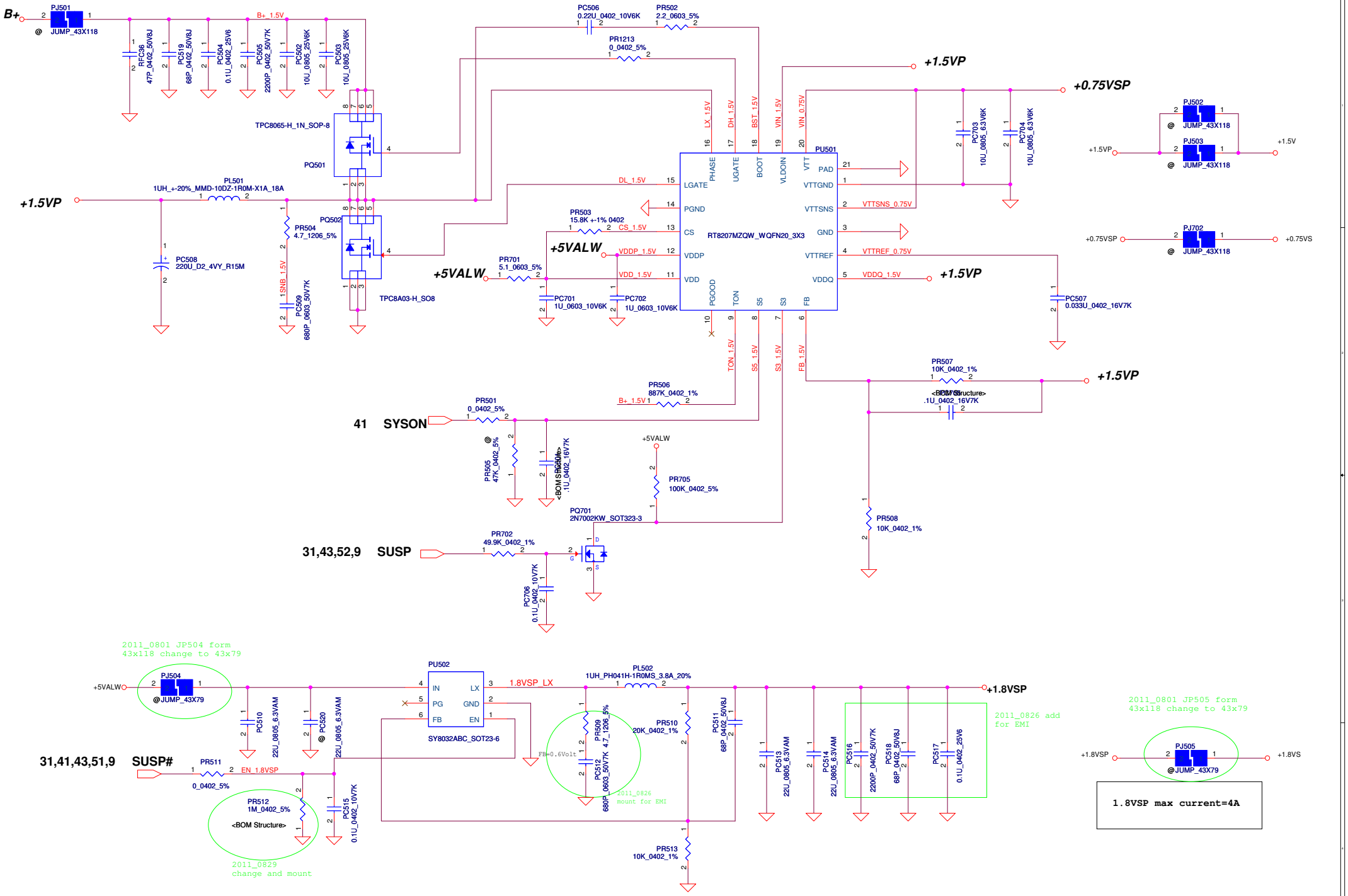

| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-3VALWP/5VALWP

Size: Custom | Document Number: NM-A041 | Rev: 1.A

Date: Thursday, November 01, 2012 | Sheet 48 of 59




| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



| | | | |
|---|---|---|---|
| Title | PWR-+1.5VP/+1.8VSP | | |
| Size | Document Number | | Rev |
| Custom | NM-A041 | | 1.A |
| Date: | Thursday, November 01, 2012 | Sheet | 49 of 59 |

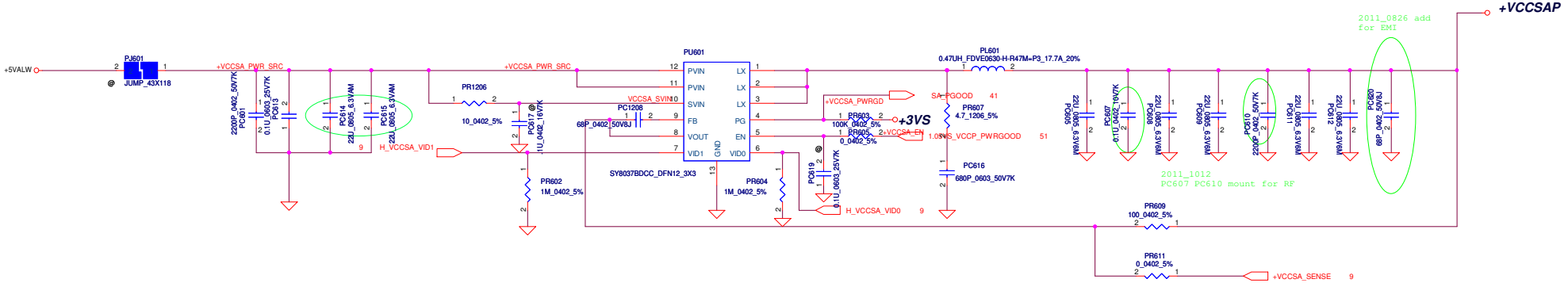
| VID [0] | VID[1] | VCCSA Vout |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

*output voltage adjustable network*

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSAP — PJ602 JUMP_43X118 — +VCCSA

*The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.*




| Security Classification | LC Future Center Secret Data | | |
|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-VCCSAP

| Size | Document Number | Rev |
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| C | NM-A041 | 1.A |

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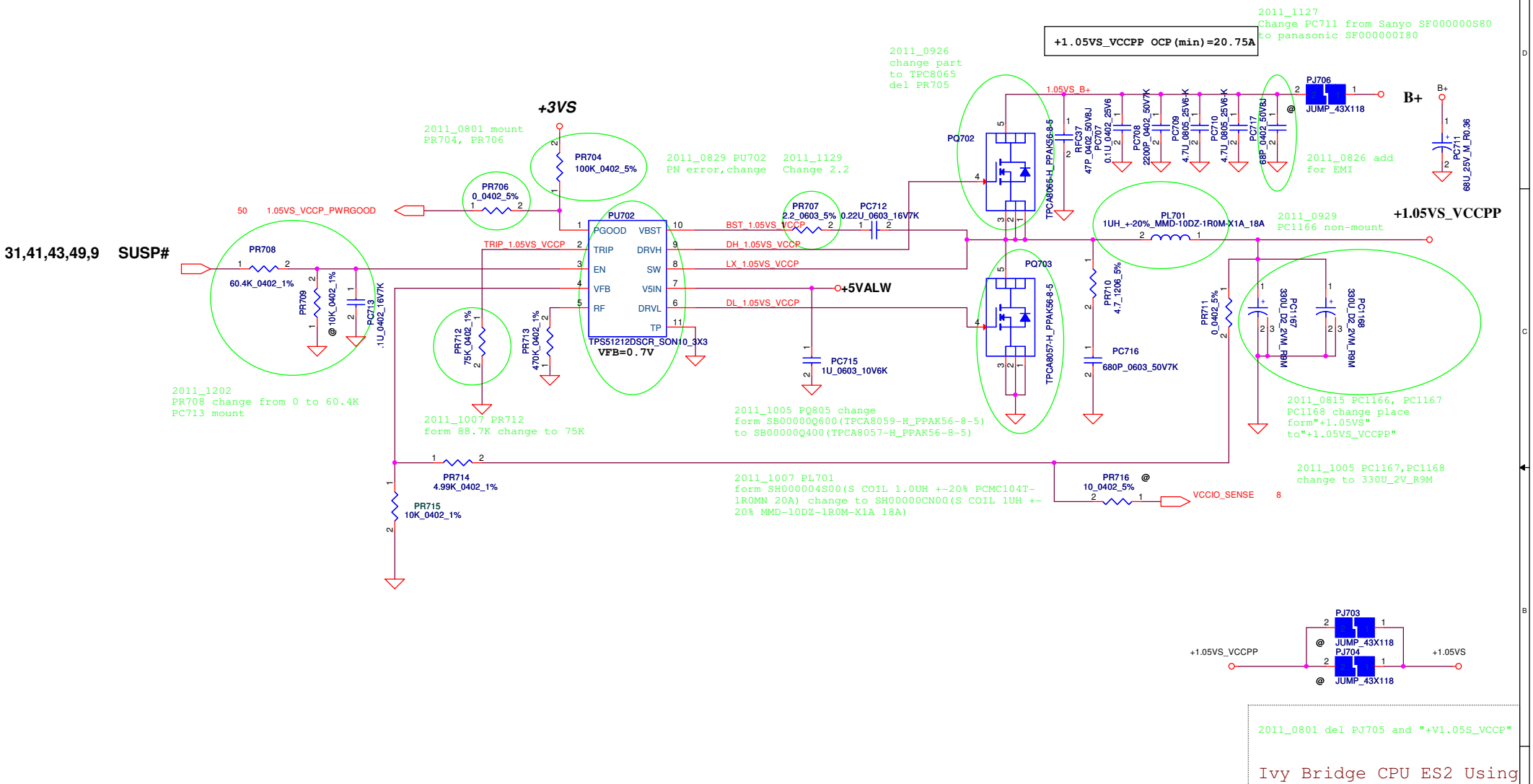


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| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



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|---|---|---|---|
| Title | PWR-+1.05VS_VCCP/+0.75VSP | | |
| Size | Document Number | | Rev |
| Custom | NM-A041 | | 1.A |
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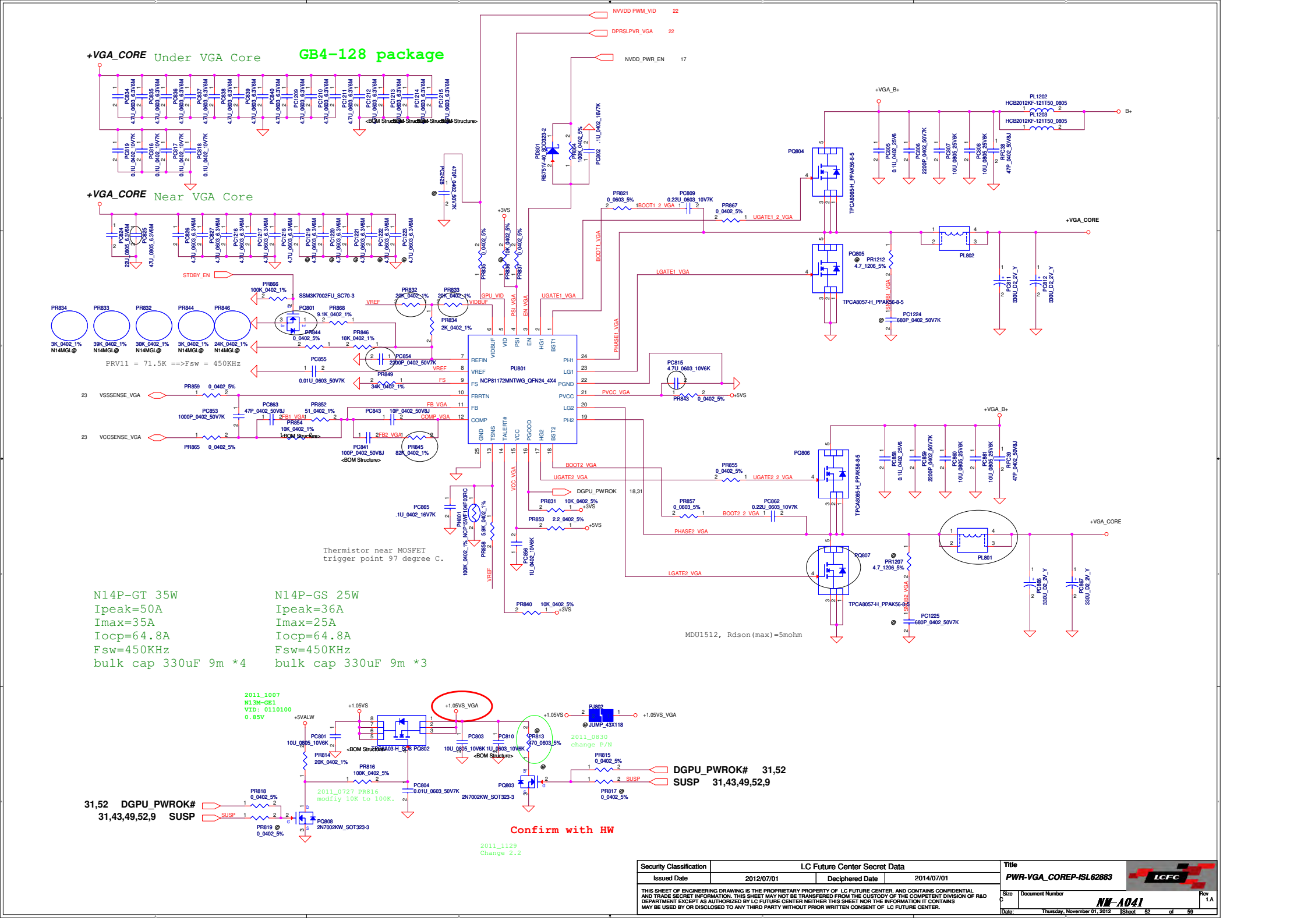


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| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



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|---|---|---|---|
| Title | PWR-VGA_COREP-ISL62883 | | |
| Size | Document Number | NM-A041 | Rev 1.A |
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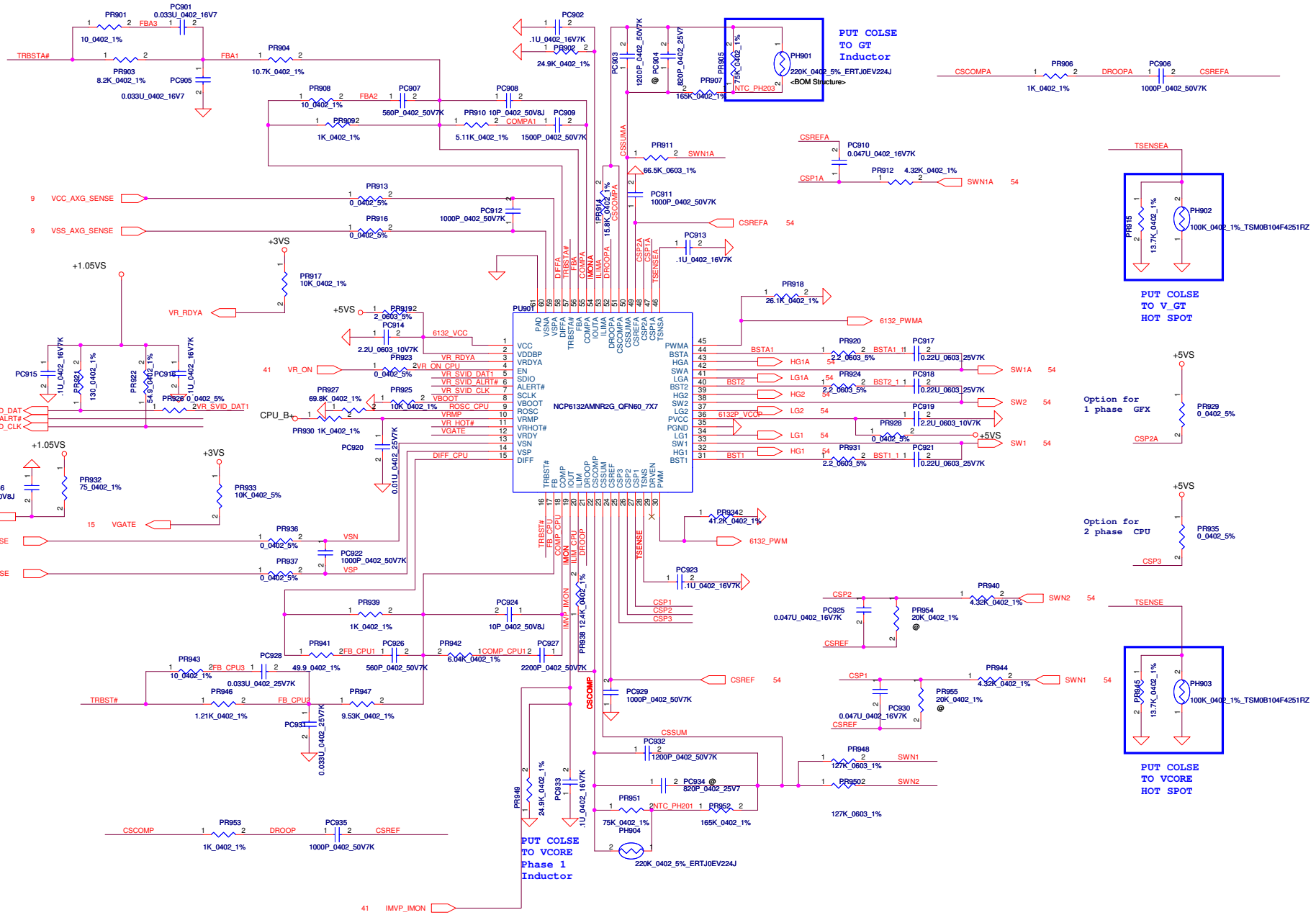


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|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-CPU_CORE1

| Size | Document Number | Rev |
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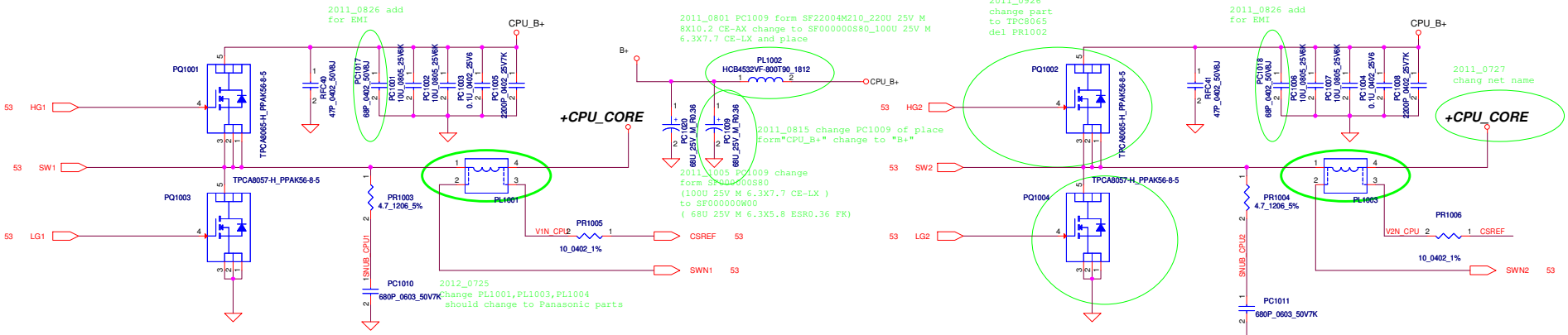
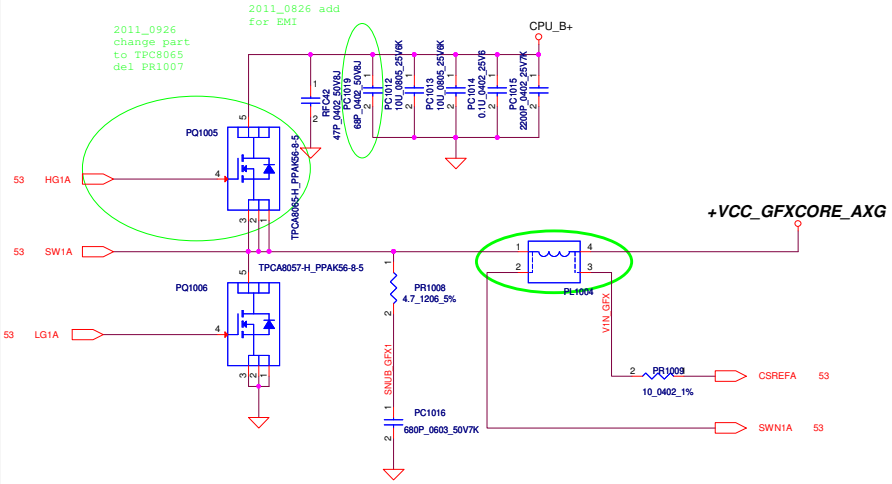



**QC 45W CPU**
**VID1=0.9V**
**IccMax=94A**
**Icc_Dyn=66A**
**Icc_TDC=52A**
**R_LL=1.9m ohm**
**OCP~110A**

**DC 35W CPU**
**VID1=1.05V**
**IccMax=53A**
**Icc_Dyn=43A**
**Icc_TDC=36A**
**R_LL=1.9m ohm**
**OCP~65A**




**QC 45W GT2**
**VID1=1.23V**
**IccMax=46A**
**Icc_Dyn=37A**
**Icc_TDC=38A**
**R_LL=3.9m ohm**
**OCP~55A**

**DC 35W GT2**
**VID1=1.23V**
**IccMax=33A**
**Icc_Dyn=20.2A**
**Icc_TDC=21.5A**
**R_LL=3.9m ohm**
**OCP~40A**

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|---|---|---|---|
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-CPU_CORE2

| Size | Document Number | Rev |
|---|---|---|
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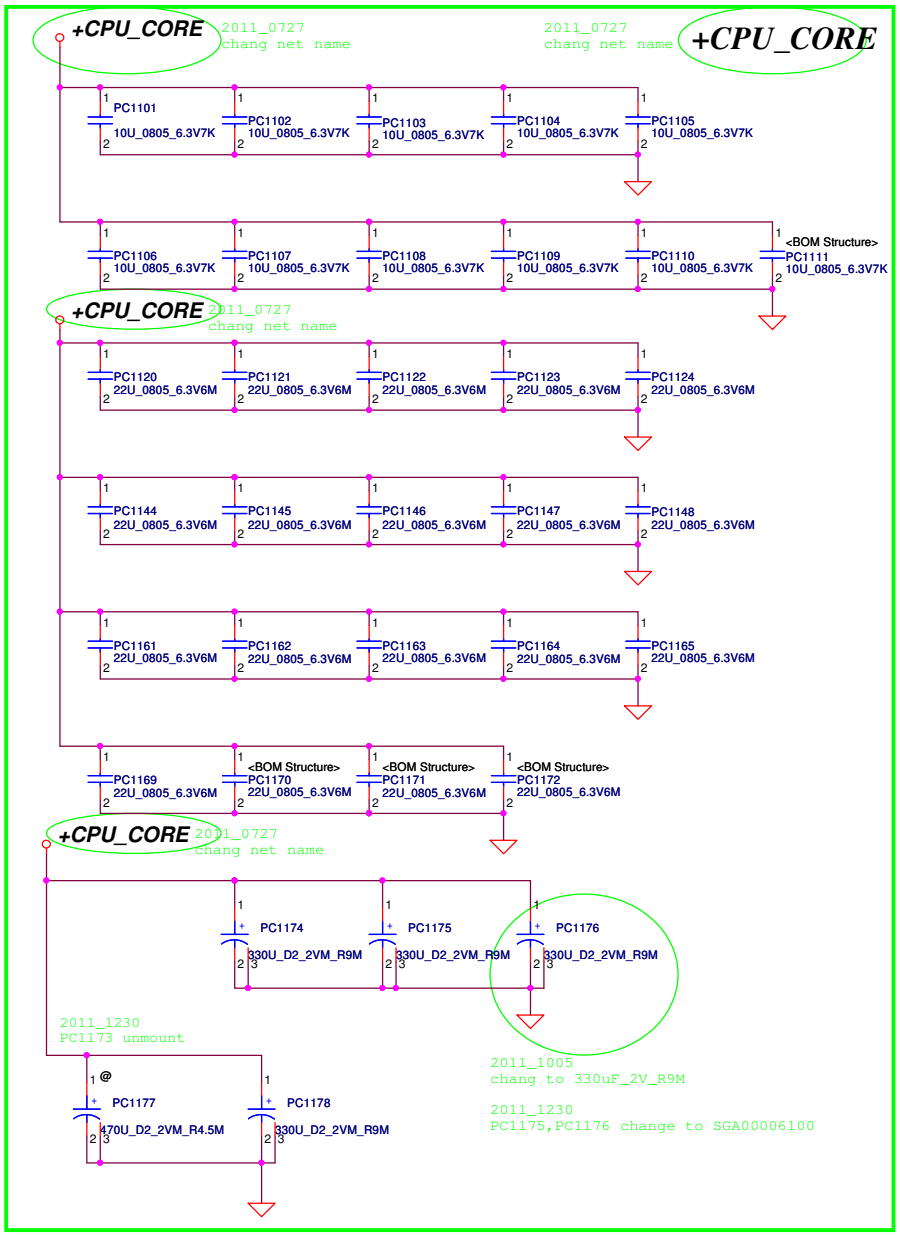
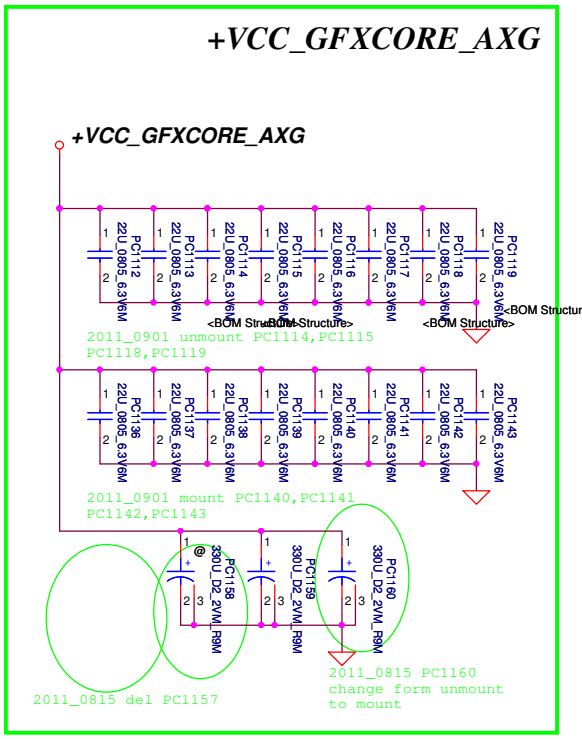
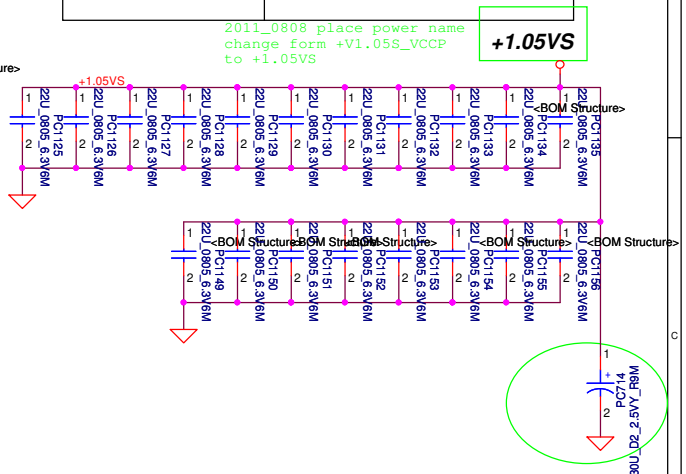



Below is 458544_CRV_PDDG_0.5 Table 5-8.

| | |
|---|---|
| Socket Bottom | 5 x 22 µF (0805)<br>5 x (0805) no-stuff sites |
| Socket Top | 7 x 22 µF (0805)<br>2 x (0805) no-stuff sites |

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| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-PROCESSOR DECOUPLING

| | | | |
|---|---|---|---|
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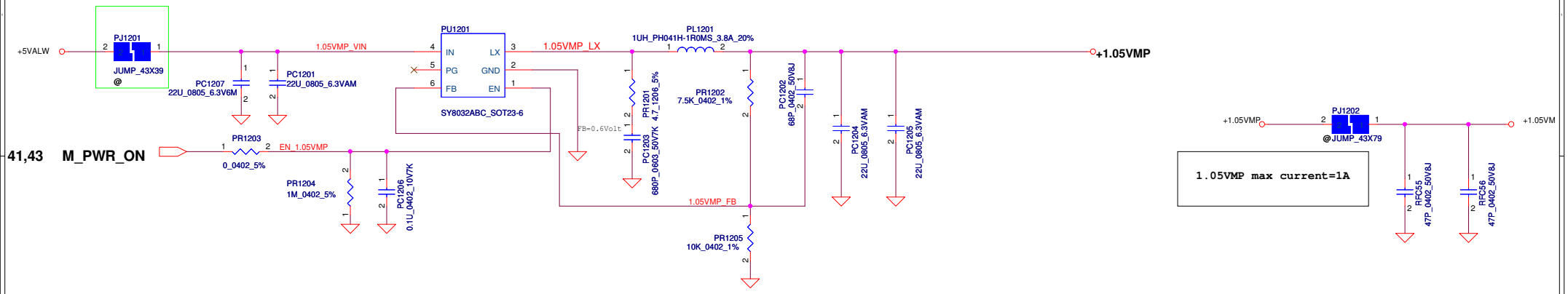
2011_0923 JUMP form 43X79 change to 43X79







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| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: PWR-+1.05VMP

| Size | Document Number | Rev |
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| | | | |
|---|---|---|---|
| Security Classification | LC Future Center Secret Data | | |
| Issued Date | 2012/07/01 | Deciphered Date | 2014/07/01 |



Title: *PWR-Thermal Protect-NA*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *NW-A041* | 1.A |

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# Version change list (P.I.R. List)

| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | | | | | |
| 2 | | | | | |
| 3 | | | | | |
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| 17 | | | | | |



| Title | | | |
|---|---|---|---|
| PWR-PIR | | | |
| Size: Custom | Document Number: NM-A041 | | Rev: 1.A |
| Date: Thursday, November 01, 2012 | Sheet 58 of 59 | | |

# Version Change List (P.I.R. List)

| Phase | Date | No. | BOM | Sch | Layout | Description | function |
|---|---|---|---|---|---|---|---|
| | 2012/09/XX | No1 | V | V | V | Add CXXX,CXXX | Add XXX function |



Title: EE P.I.R.

| Size | Document Number | Rev |
|---|---|---|
| Custom | NM-A041 | 1.A |

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