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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

MI 2.0Refresh

Main Board

DB BUILD
2018.04.13

	BUILD_ID1	BUILD_ID0
DB	0 >>R4626	0 >>R4622
SI	0 >>R4626	1 >>R4621
PV	1 >>R4624	0 >>R4622
MV	1 >>R4624	1 >>R4621

Dis/UMA

	DIS	UMA
R4623	Mount	NC
R4625	NC	Mount

DGPU_PWROK

	DIS	UMA
R4591	NC	MOUNT

DGPU_PRSNT# :

	DIS	UMA
R4590	Mount	NC
R4589	NC	Mount

GPU_UMA_SEL

	DIS	UMA
R307	Mount	NC
R309	NC	Mount

Phase_ID

	SI	DB	PV/MV
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short

CPU

I3-6100U QJFC QS	6025B0280401	2.3GHz Dual core
I5-6200U QJ8N QS	6025B0280501	2.3GHz Dual core
I7-6500UQJ8L QS	6025B0280801	2.5GHz Dual core
3855U QJ8S QS	6025B0292301	1.6GHz Dual core 15W

BOM CHANGE
UMA => C4835~C4842 NC
U4500 => 6025B0268201
VRAM IC
VRAM ID
U66000 => 6019B1315701

DATE	CHANGE NO.	REV
08-APR-2016	2015-ECO-023844	A

DESIGN / DRAWER	Wang,Abel	DATE	08-APR-2016
CHECK	Chih Johnson		
APPROVAL	Chih Johnson		
FILE NAME	14" MI2.0 Intel Kabylake		
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE	14" MI 2.0		
Main Board	14 MI1.0 Intel Skylake-U		
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A
SHEET	of	1	67

07e20411070e0102900018f4ea003be7

Index

INVENTEC

TITLE	14" MI 2.0 INDEX		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET	of 2 67		

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6PNQA2811101	PCB VER	A01

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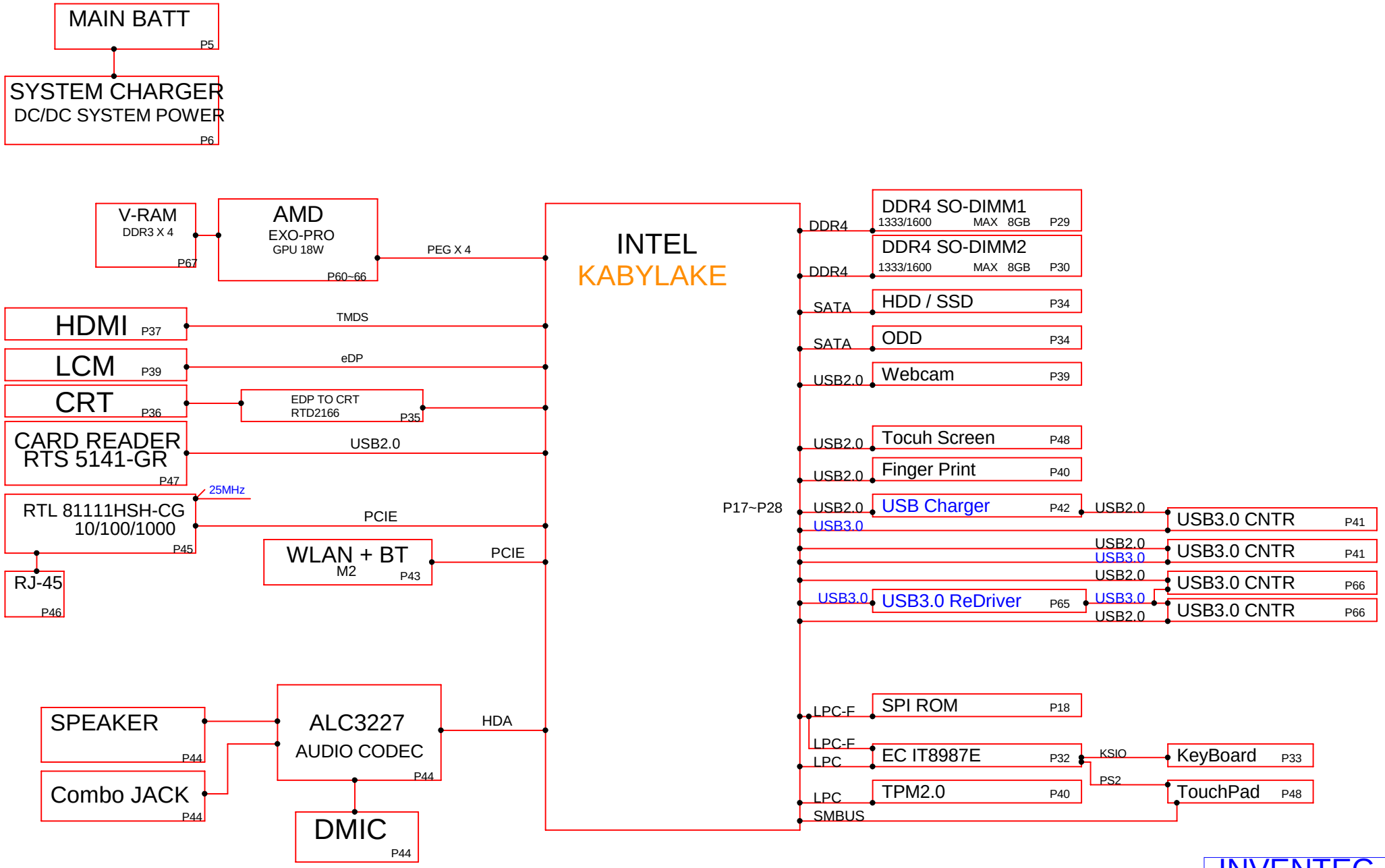

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET 3 of 67			

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

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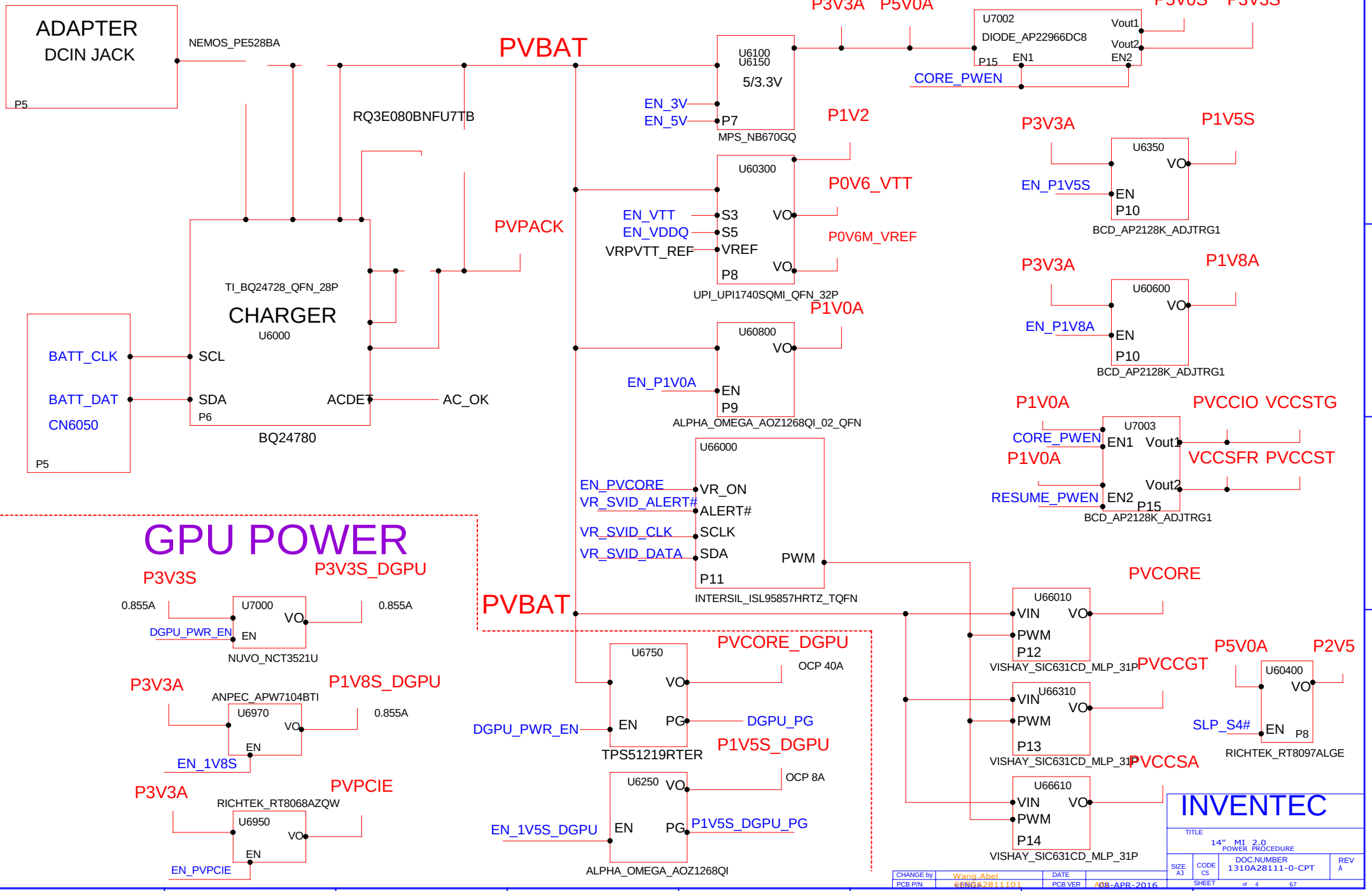

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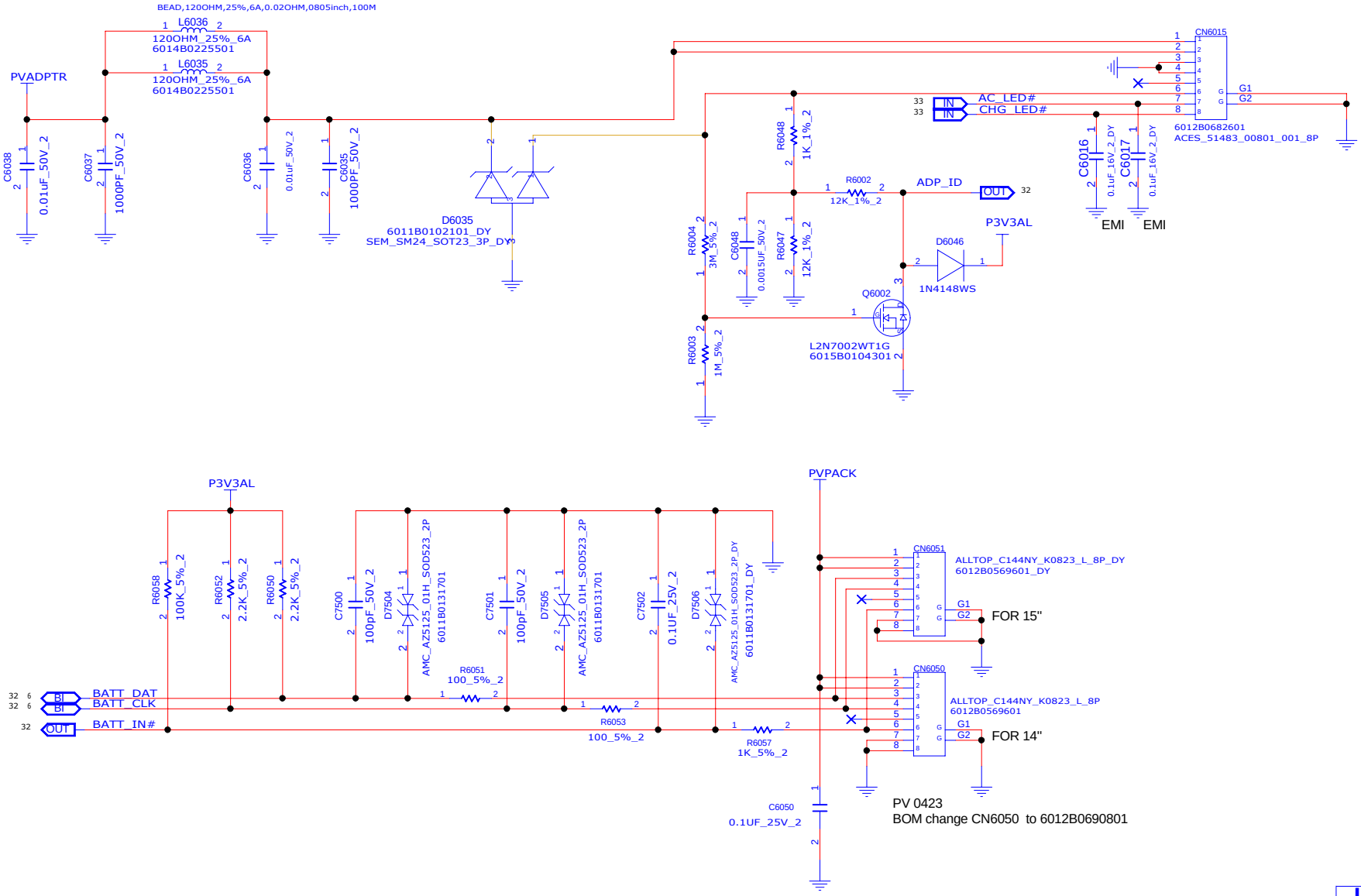

INVENTEC

TITLE	14" MI 2.0 Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT			REV A
CHANGE by	Wang,Abel <ENG>	DATE	08-APR-2016	SHEET 5 of 67	
PCB P/N	6050A2811101	PCB VER	A01 <VER>		

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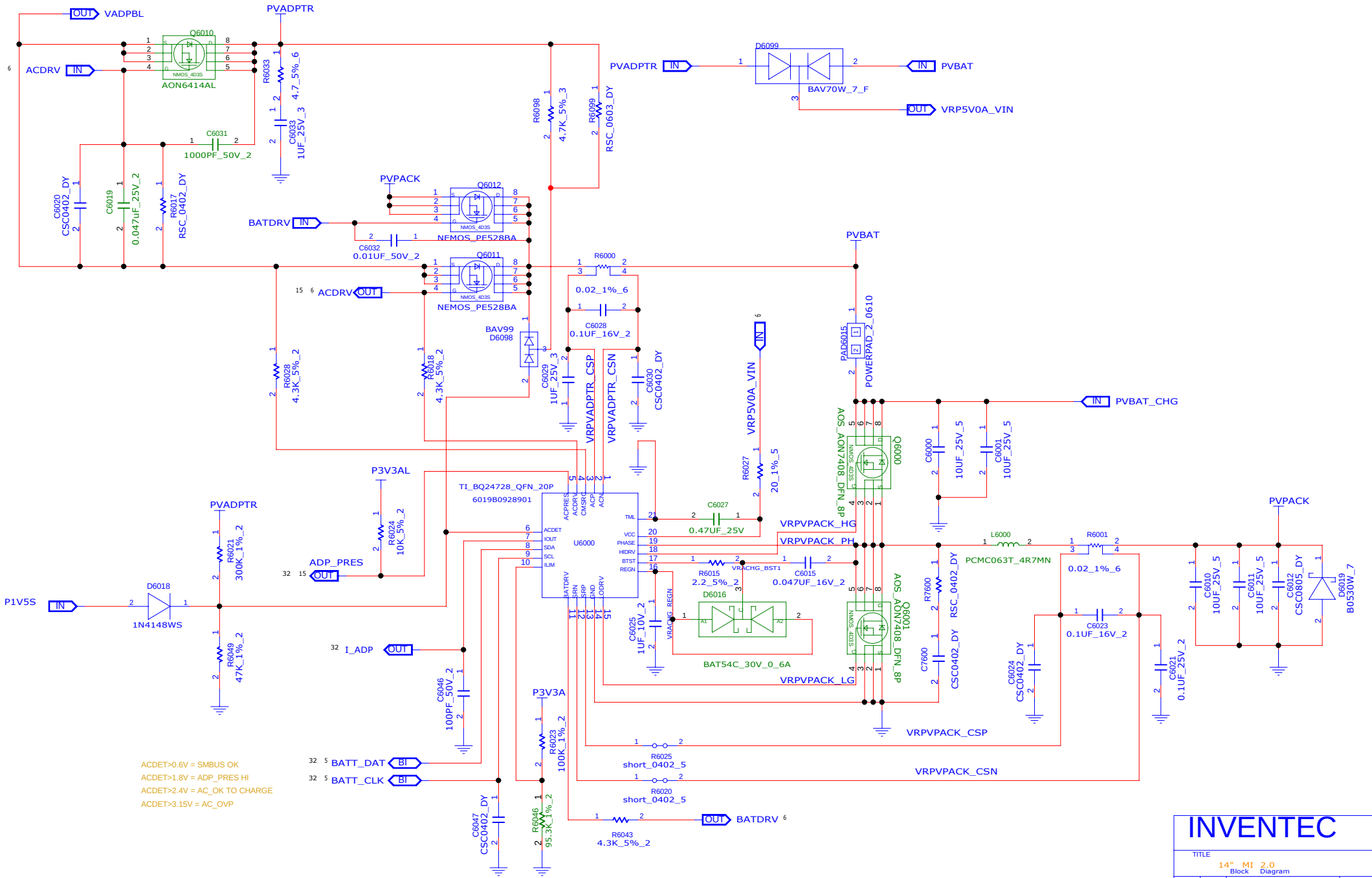

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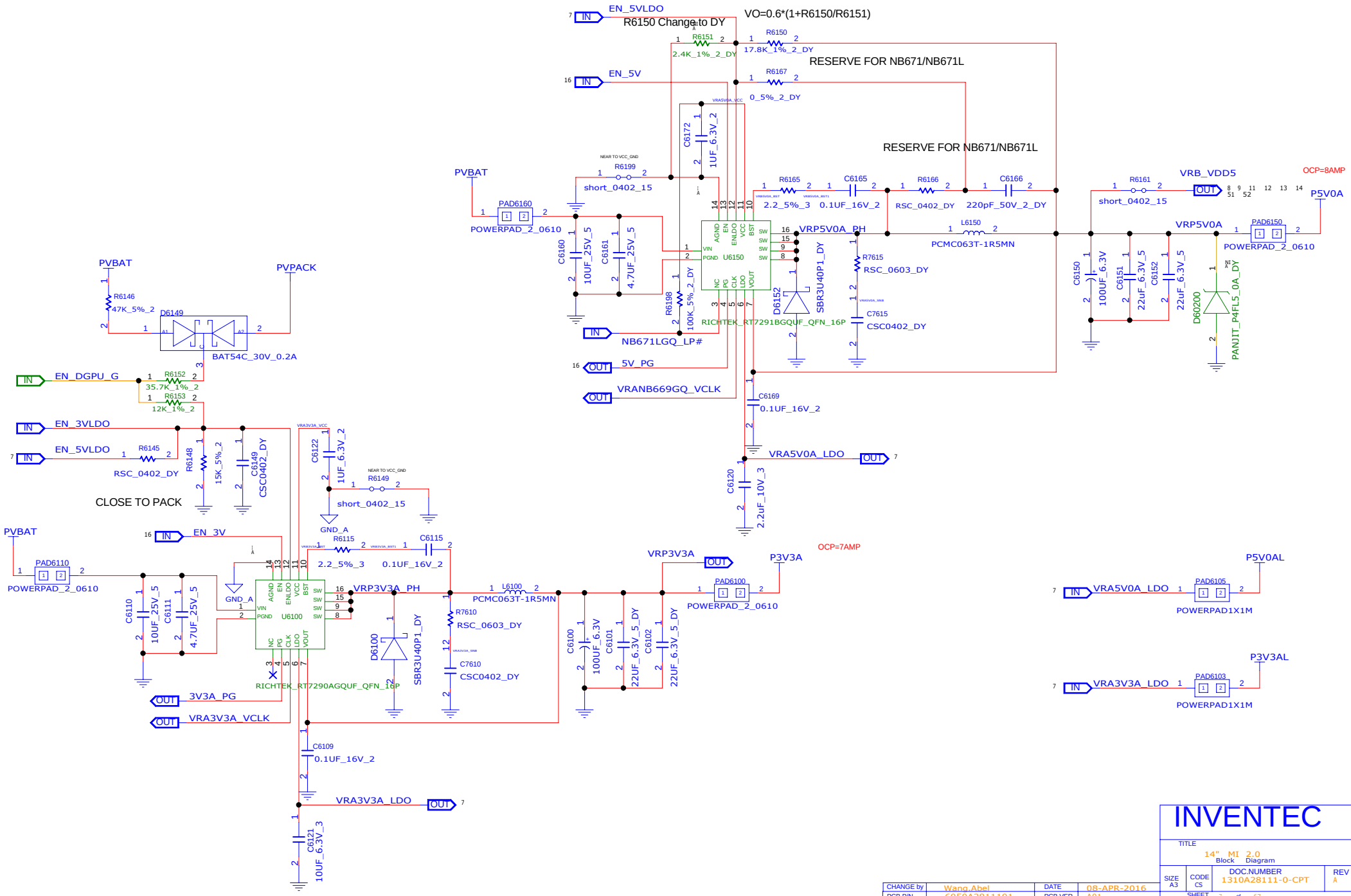

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

RCS=10K
RTON=511K

R60306 511K_1%_2
VRAVDDQ_TON
VRPVDDQ_VIN
PVBAT
PAD60310 POWERPAD_2_0610
C60310 10UF_25V_5
C60311 10UF_25V_5_DY

U60300
ANPEC_APW8863QBI_TRG_TQFN_32P

EN_VTT
EN_VDDQ
VDDQ_PG
VRAVDDQ_CS
VRB_VDD5
R60309 2.2_5%_2
R60305 6.04K_1%_1/16W_2
VRB_VCC
C60306 1UF_6.3V_2
VRPVDDQ
VRPVDDQ_VLDOIN
R60359 short_0402_15
VRPVTT
C60350 10UF_6.3V_3
VRPVTT_REF
C60351 0.1UF_16V_2
R60315 0_5%_3
C60315 0.1UF_16V_2
VRAVDDQ_BST
VRAVDDQ_BST1
VRPVDDQ_PH
L60300 PCMC063T_1R0MN
R60316 RSC_0603_DY
C60316 CSC0402_DY
VRAVDDQ_SNB
C60300 22uF_6.3V_5
C60301 22uF_6.3V_5
C60302 22uF_6.3V_5
C60303 22UF_6.3V_5_DY
VRPVDDQ
PAD60300 POWERPAD_2_0610
P1V2
OCP=13A
FSW=463KHZ
VO=0.75*(1+R30300/R60301)
VRAVDDQ_SET
R60300 6.19K_1%_2
C60304 0.022UF_16V_2_DY
R60301 10K_1%_2
PAD60350 POWERPAD1X1M
P0V6_VTT

P5V0A
PAD60410 POWERPAD_2_0610
VRP2V5_VIN
C60410 22uF_6.3V_5
U60400
NRS5020T2R2N
L60400
VRP2V5_PH
EN_2V5
2V5_PG
RICHTEK_RT8097ALGE_TSOT23_6P
R60400 324K_1%_2
C60402 22pF_50V_2
R60401 100K_1%_2
VOUT=0.6*(1+(R60400/R60401))
C60400 22uF_6.3V_5
C60401 22uF_6.3V_5
VRP2V5
PAD60400 POWERPAD_2_0610
P2V5

INVENTEC
TITLE 14" MI 2.0 Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310A28111-0-CPT | REV A
SHEET 8 of 67
CHANGE by Wang.Abel | DATE 08-APR-2016
PCB P/N 6050A2811101 | PCB VER A01

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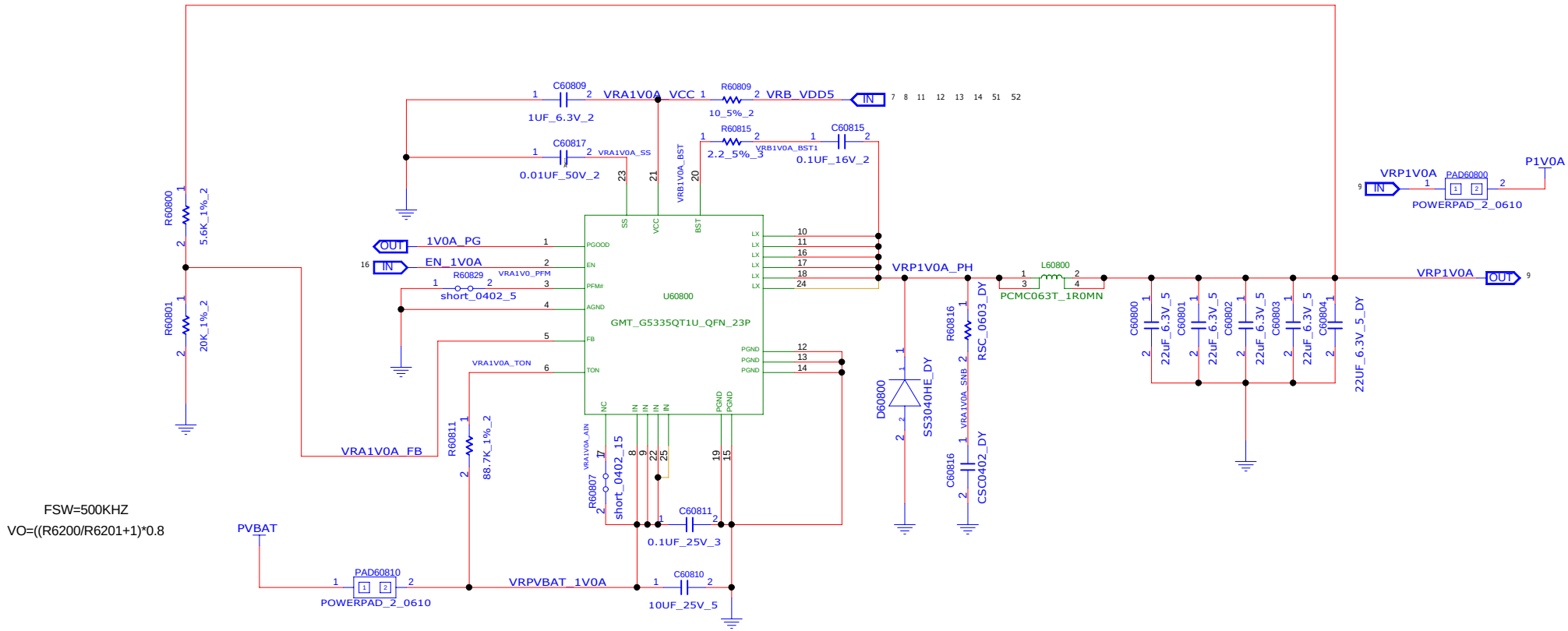

FSW=500KHZ

VO=((R6200/R6201+1)*0.8

CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 9 of 67

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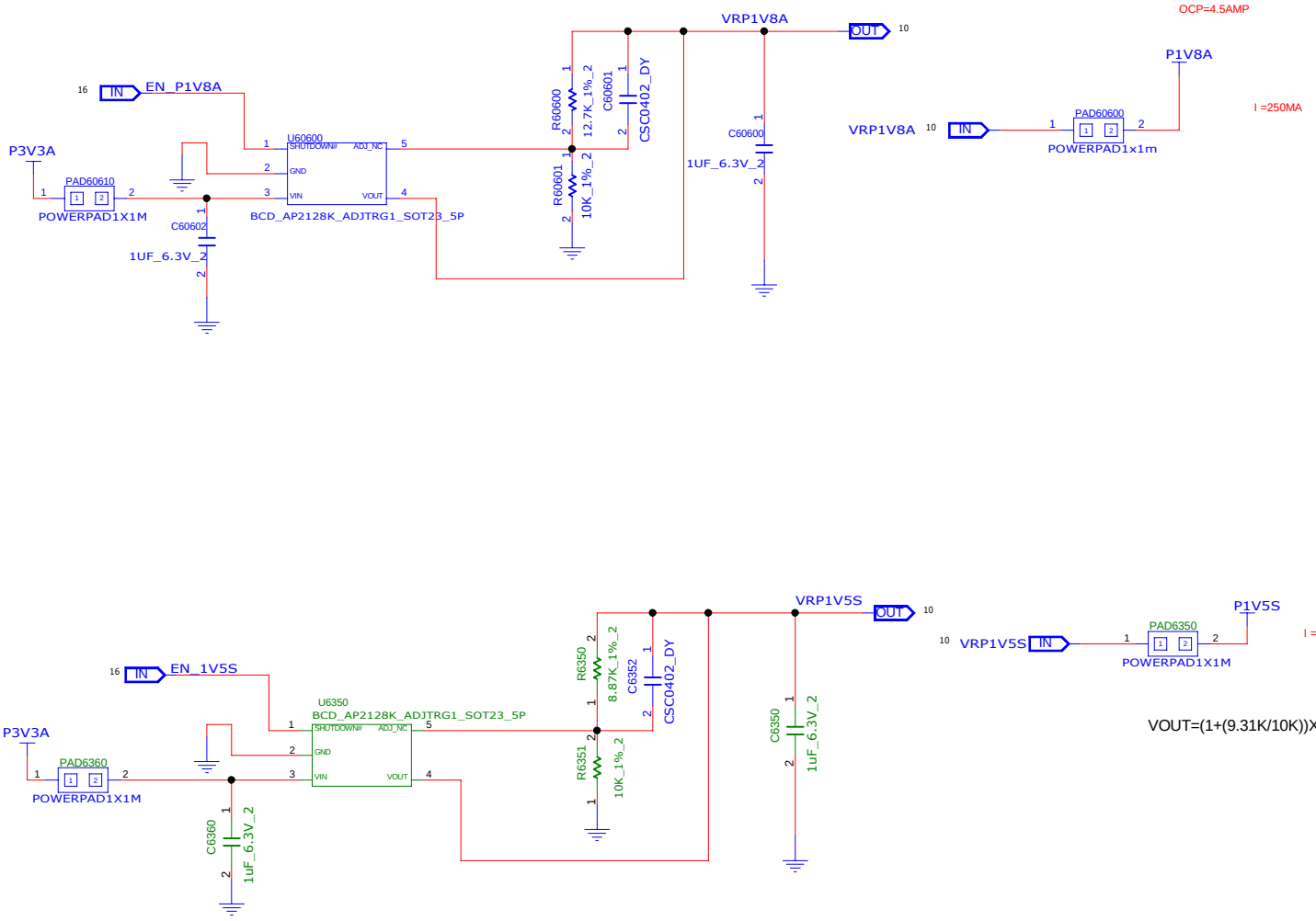

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 10 of 67

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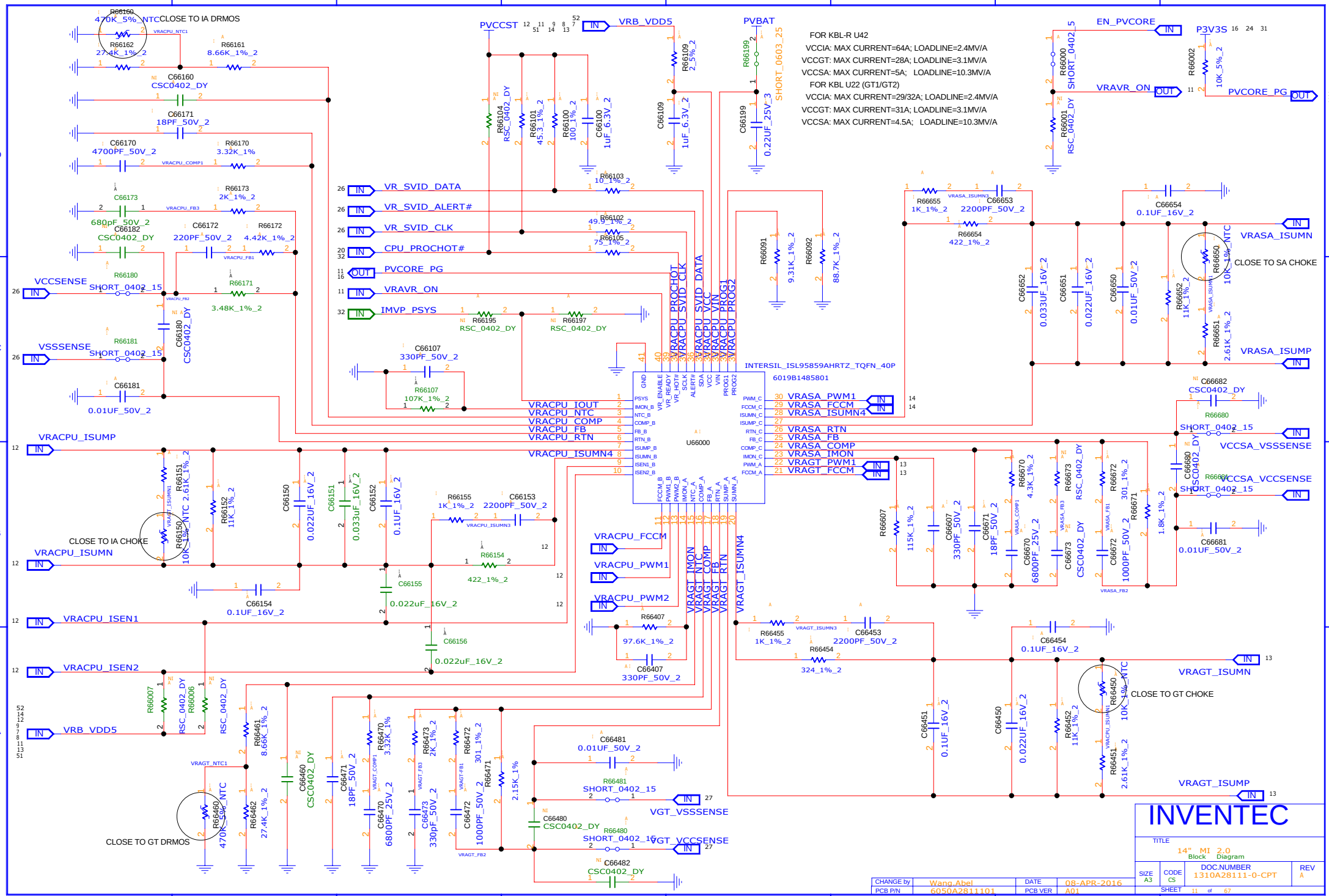

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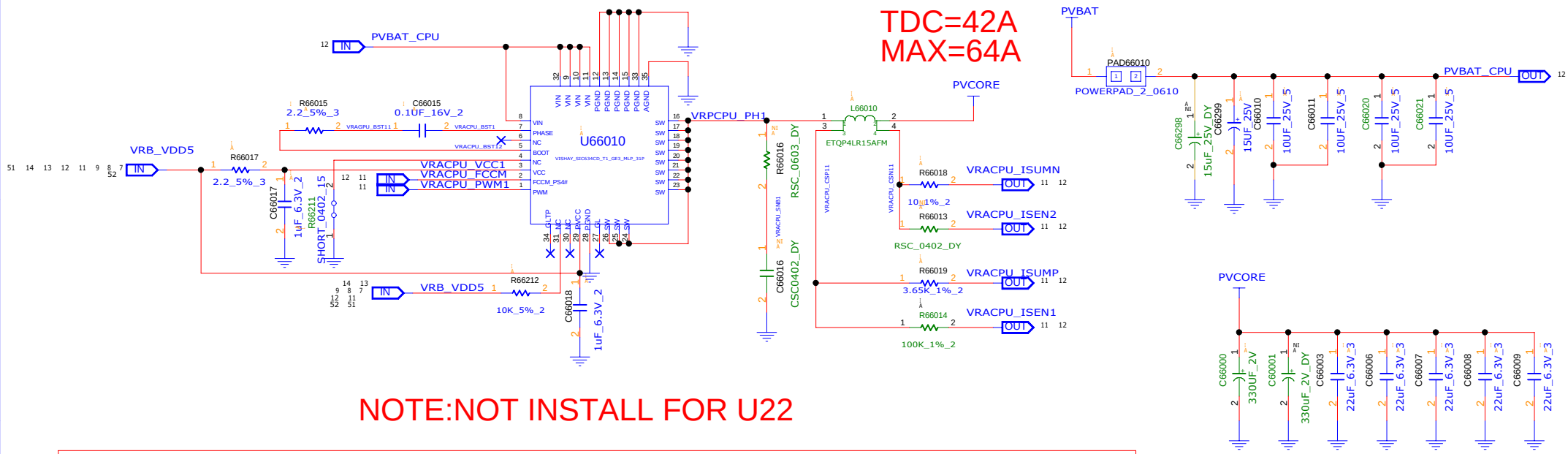
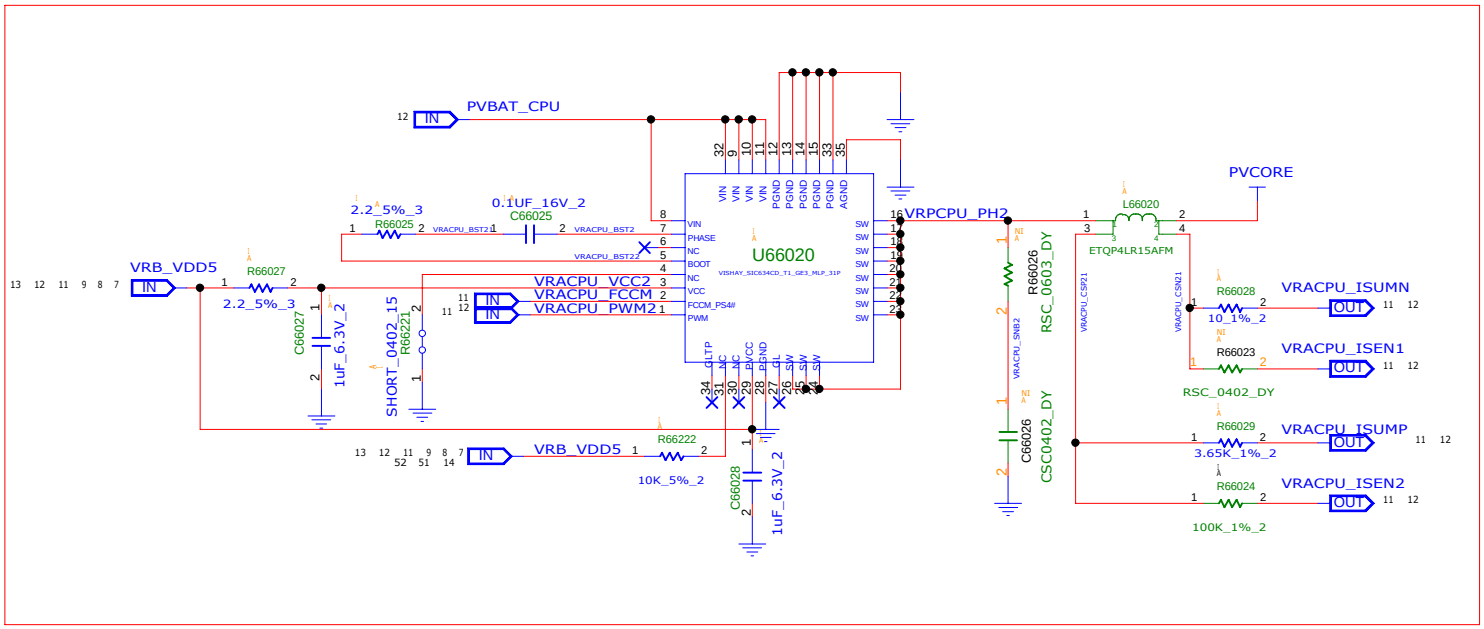
07e20411070e0102900018f4ea003be7

NOTE:ONE PHASE FOR U22

TDC=42A
MAX=64A



NOTE:NOT INSTALL FOR U22



INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01
SHEET 12 of 67			

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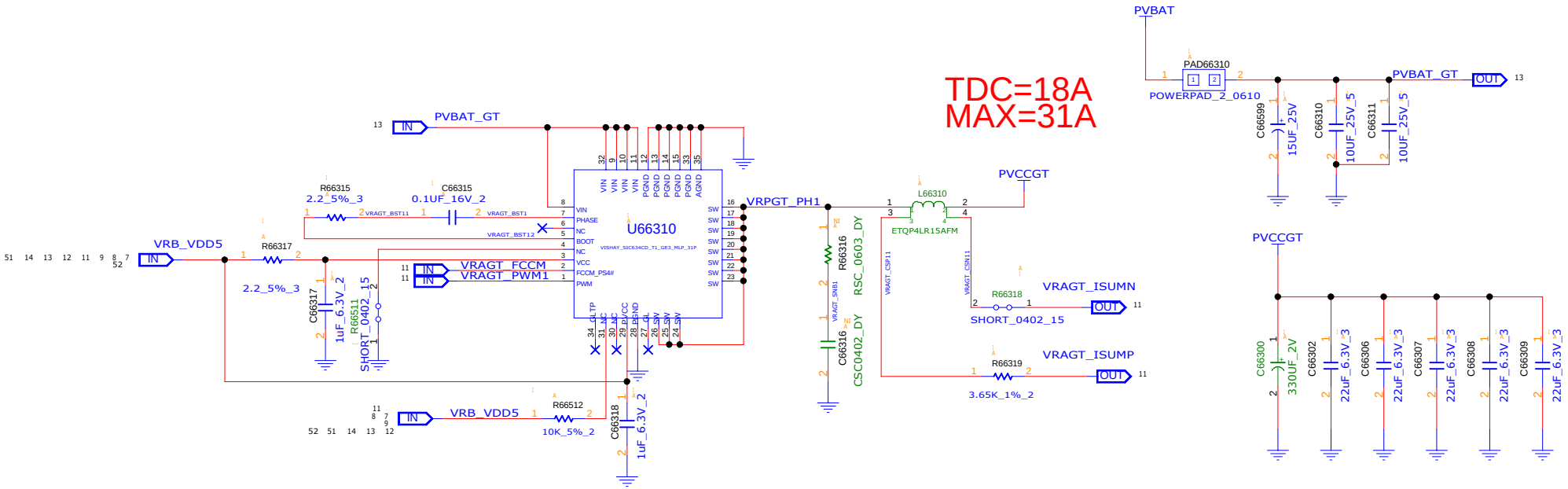

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 13 of 67

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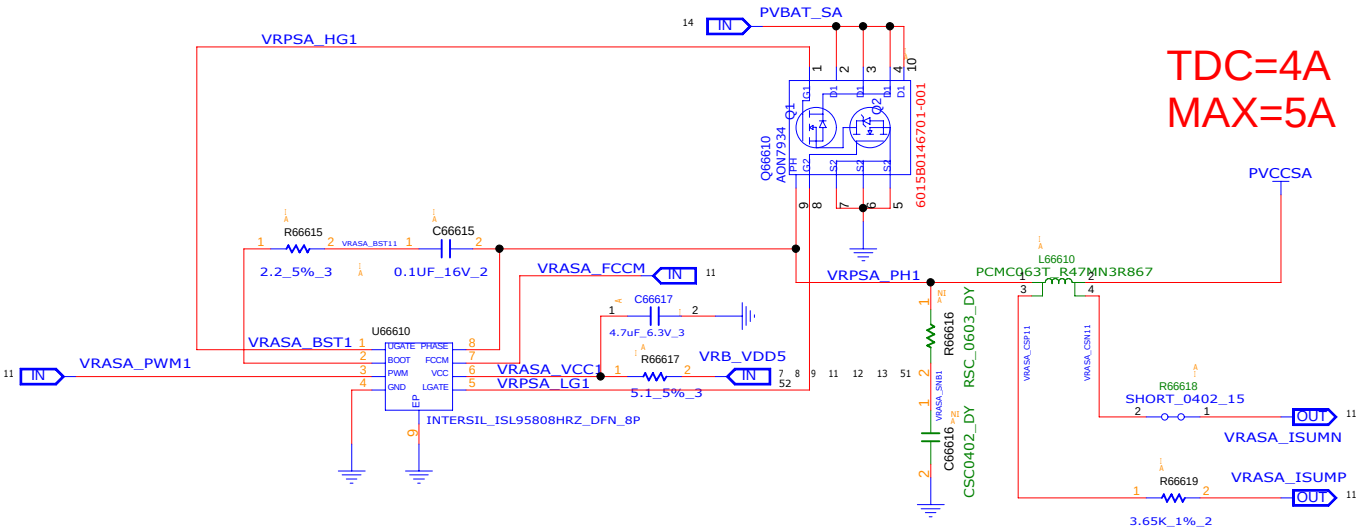

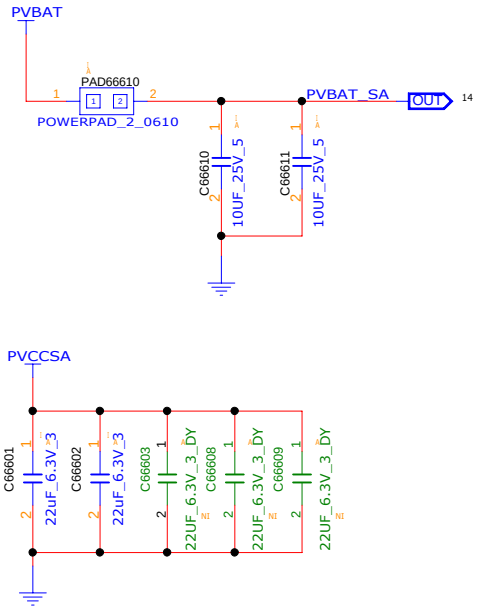

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET 14 of 67			

CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

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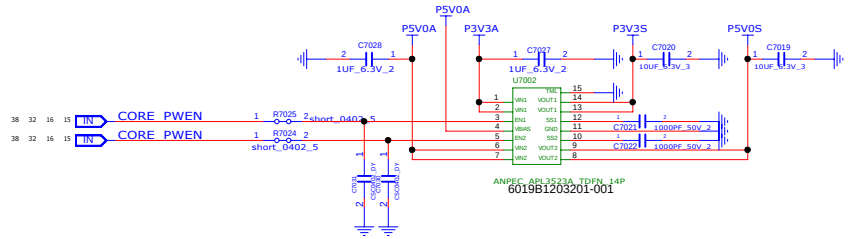
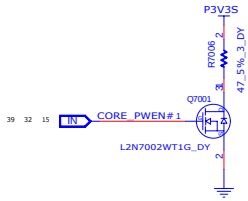
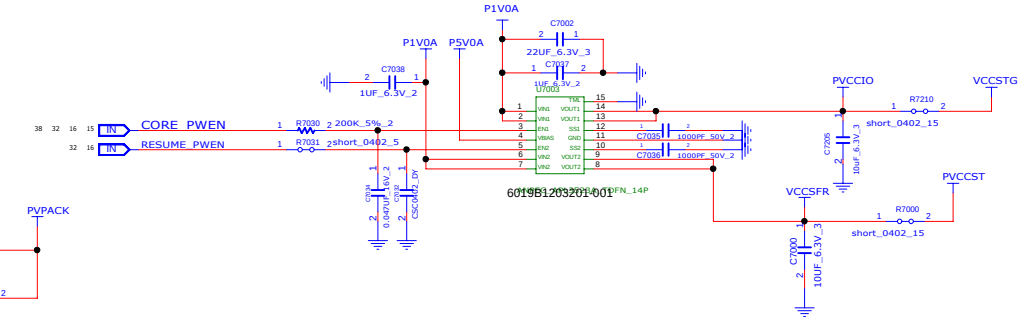


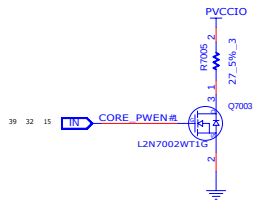
ADD DISCHARGE FOR ES CPU

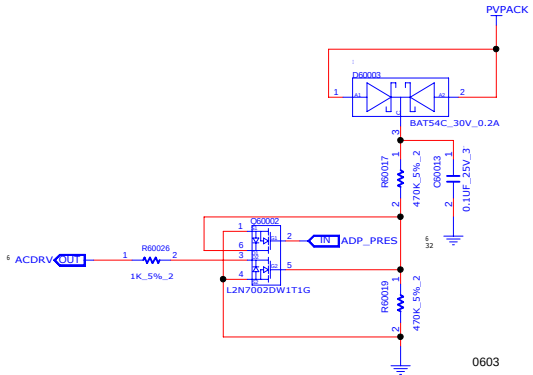


IEC PN	Vendor	Vendor PN	
6019B1203201	Diodes	AP22966DC8-7	Main source
6019B1270101	AOS	AOZ1331	2nd
6019B1184301	Anpec	APL3523AQBI-TRG	3rd



ADD DISCHARGE FOR ES CPU





0603

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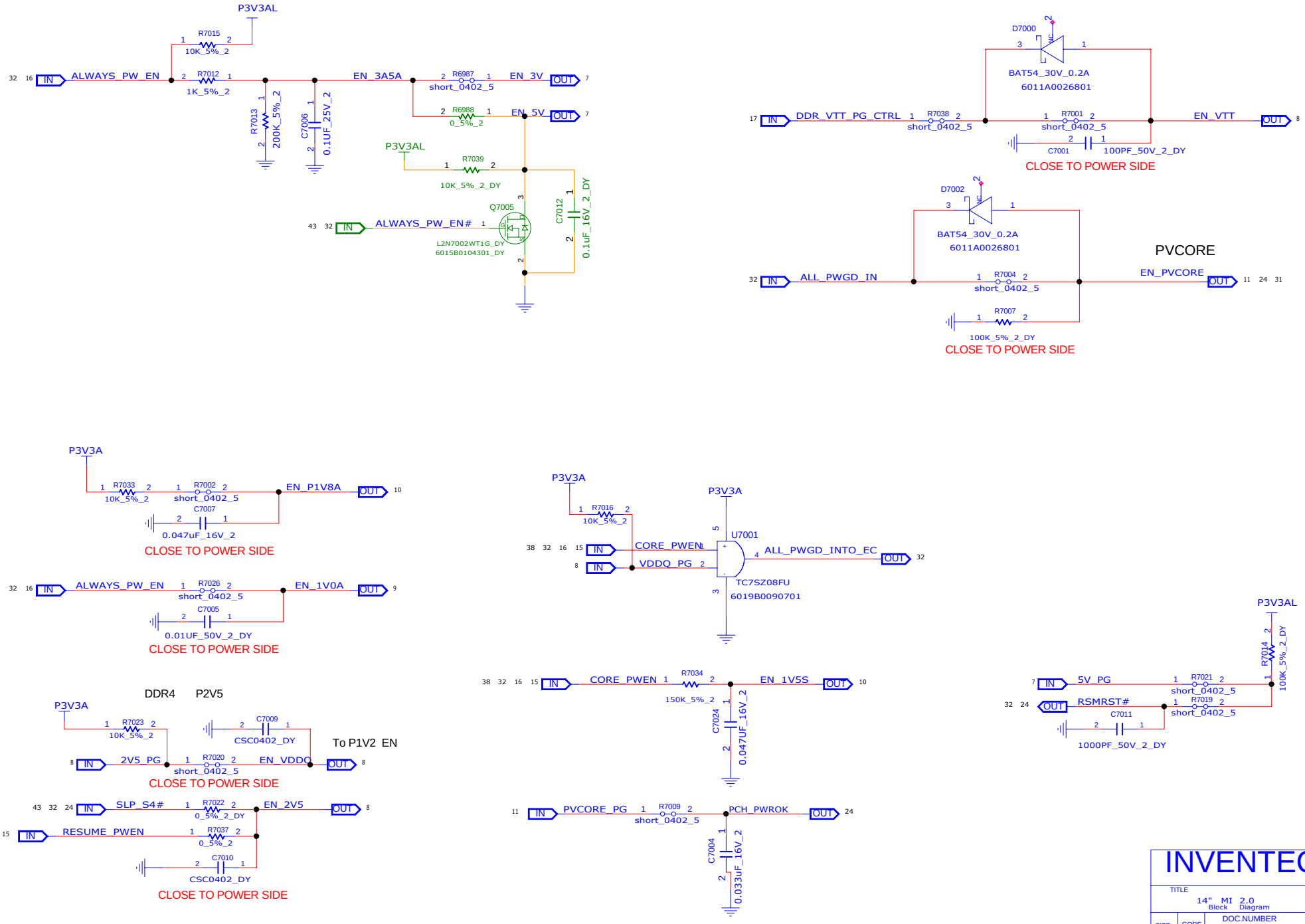

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
CHANGE by	Wang,Abel	DATE	
PCB P/N	6050A2811101	PCB VER	A00
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET	of 16	67	

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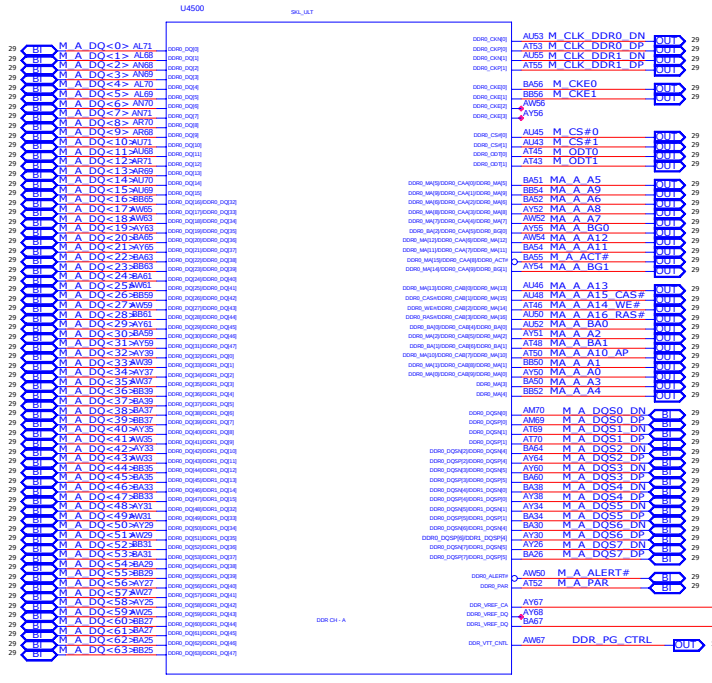
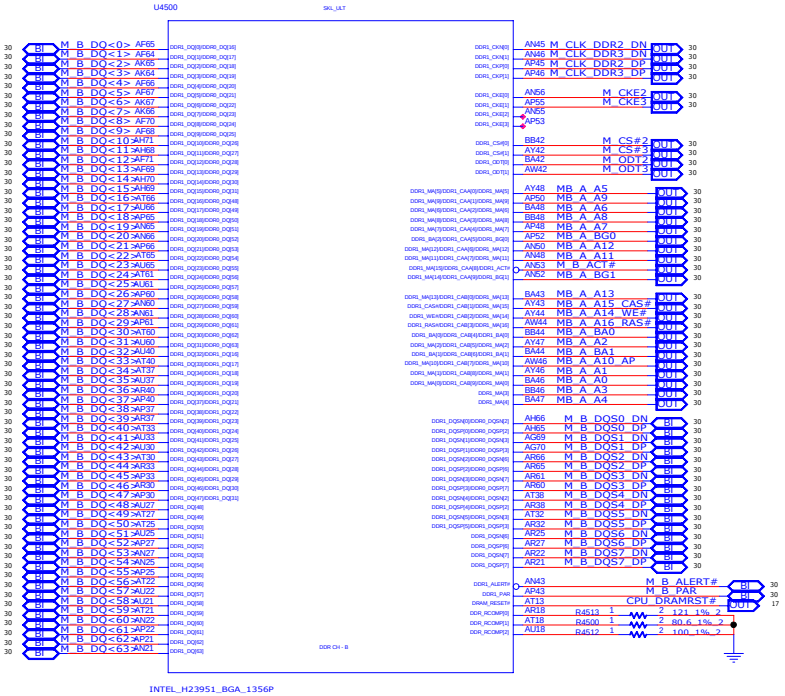
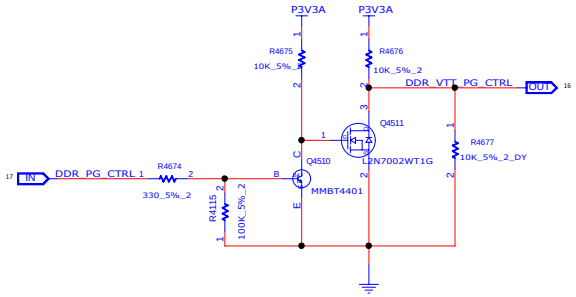
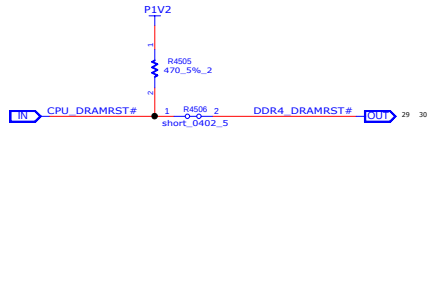
REFERENCE:4500~4949









INVENTEC

14" MI 2.0
DDR3_SO-DIMM0

SIZE	CODE	DOC NUMBER	REV
C	CS	1310A28111-0-CPT	A

SHEET 17 of 67

CHANGE ID		DATE	
PCB P/N	6052M28111101	PCB VER	0A

07e20411070e0102000018f4ea003be7

07e20411070e0102900018f4ea003be7

543016 60.3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

P3V3A

TLS CONFIDENTIALITY GPP_C2
(INTERNAL PULL DOWN 20K)
18 OUT TLS 1 R4537 2 1K_5%_2

GPP_C5
18 OUT GPP_C5 1 R4545 2 1K_5%_2_DY

32 IN SPI_EC_CLK 1 R4565 2 33_5%_2 PCH_SPI_CLK OUT 48
32 IN SPI_EC_CS0# 1 R4566 2 33_5%_2 PCH_SPI_CS0# OUT 18
32 IN SPI_EC_SI 1 R4567 2 33_5%_2 PCH_SPI_SI OUT 48
32 IN SPI_EC_SO 1 R4568 2 33_5%_2 PCH_SPI_SO OUT 48

BLM15AG121SN1D_500mA
18 BI PCH_3A_SMCLK_R 1 L4606 2 PCH_3A_SMCLK BI 18 49
18 BI PCH_3A_SMDATA_R 1 L4605 2 PCH_3A_SMDATA BI 18 49
EMI
BOM : 6014B0029801

U4500 SKL_ULT

SPI - FLASH
48 OUT PCH_SPI_CLK R4560 15_5%_2 AV2 SPI0_CLK
48 OUT PCH_SPI_SO R4559 15_5%_2 AW3 SPI0_MISO
48 OUT PCH_SPI_SI R4561 15_5%_2 AV3 SPI0_MOSI
18 OUT PCH_SPI_IO2 R4563 15_5%_2 AW2 SPI0_IO2
18 OUT PCH_SPI_IO3 R4562 15_5%_2 PCH_SPI_IO3_R AU4 SPI0_IO3
18 OUT PCH_SPI_CS0# AU3 SPI0_CS0#
OUT TPM_SPI_CS2# TP4500 1 AU2 SPI0_CS1#
AU1 SPI0_CS2#
R4569 1K_5%_2_DY
ES CPU ONLY

SPI - TOUCH
32 IN EC_SMI# M2 GPP_D1/SPI1_CLK
32 IN EC_SCI# M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#
GPPD

C LINK
G3 CL_CLK
G2 CL_DATA
G1 CL_RST#

TOUCH PANEL :
SPI INTERFACE

P3V3S
1 R4573 2 10K_5%_2 KB_RST# OUT 18 32
1 R4571 2 10K_5%_2 SERIRQ OUT 18 32
32 18 IN KB_RST# AW13 GPP_A0/RCIN#
32 18 OUT SERIRQ AY11 GPP_A6/SERIRQ
GPPA 3V3S

SMBUS, SMLINK
GPP_C0/SMBCLK R7 PCH_3A_SMCLK_R BI 18
GPP_C1/SMBDATA R8 PCH_3A_SMDATA_R BI 18
GPP_C2/SMBALERT# R10 TLS IN 18
GPPC 3V3A?
CHECK
GPP_C3/SML0CLK R9
GPP_C4/SML0DATA W21 TP4511 GPP_C5 IN 18
GPP_C5/SML0ALERT# W1
GPP_C6/SML1CLK W31 TP4508
GPP_C7/SML1DATA V3 1 TP4510
GPP_B23/SML1ALERT#/PCHHOT# AM7 1 R4576 2 150K_5%_2
P3V3A

LPC
GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD<0> BI 32 44
GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD<1> BI 32 44
GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD<2> BI 32 44
GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD<3> BI 32 44
GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# OUT 32 44
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 LPC_ESPI_REST# OUT 32
GPPA 3V3S

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 CLK_KBPCI_R R4551 1 2 33_5%_2
GPP_A10/CLKOUT_LPC1 AY9 CLK_PCI_DEBUG_R R4550 1 2 33_5%_2
GPP_A8/CLKRUN# AW11 R4554 1 2 0_5%_2_DY
9/10 68ohm to 33ohm

P3V3S
18 OUT PCI_3S_CLKRUN# 1 R4577 2 8.2K_5%_2
CLK_LPC_EC OUT 32
CLK_LPC_DEBUG_R OUT 44
CLK_TPM OUT
PCI_3S_CLKRUN# IN 18
C4564 CSC0402_DY

INTEL_H23951_BGA_1356P

MI 8MB SPI ROM
W25Q64FVSSIQ_6019B1039601

SPI_VCC OUT 18 25
0.1 AMP
R4574 10K_5%_2_DY
R4575 1K_5%_2
R4564 1K_5%_2
18 BI PCH_SPI_CS0# 1 CS
48 BI PCH_SPI_SO 2 DO_IO1
18 BI PCH_SPI_IO2 3 WP_IO2
4 GND
U4503
8 VCC
7 HOLD_IO3 PCH_SPI_IO3 BI 18
6 CLK PCH_SPI_CLK BI 48
5 DI_IO0 PCH_SPI_SI BI 48
SPI_VCC OUT 18 25
C4565 0.1uF_16V_2
WINB_W25Q64JVSSIQ_SOIC_8P
BIOS ROM

P3V3S P3V3A P3V3S
R4558 2.2K_5%_2
R4557 2.2K_5%_2
R4556 2.2K_5%_2
R4555 2.2K_5%_2
30 29 BI PCH_3S_SMCLK
49 18 BI PCH_3A_SMCLK
49 18 BI PCH_3A_SMDATA
30 29 BI PCH_3S_SMDATA
Q4501
L2N7002DW1T1G
6015B0098401

INVENTEC
TITLE 14" MI 2.0 Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310A28111-0-CPT | REV A
SHEET 18 of 67
CHANGE by <ENG>Abel | DATE 08-APR-2016
PCB P/N 6050A2811101 | PCB VER <VER>

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

REFERENCE 4700~4949(PCH)

543016 60.3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION

P3V3A
R4594 1 2 10K_5%_2 HDD_LOCK_LED# OUT 19 49

P3V3S
R4548 1 2 10K_5%_2 ODD_PWREN OUT 19 35
R4546 1 2 10K_5%_2 ODD_MD# OUT 19 35
R4547 1 2 10K_5%_2 ODD_PRSNT# OUT 19 35
R4593 1 2 10K_5%_2 DGPU_HOLD_RST# OUT 19 55
R4595 1 2 10K_5%_2 GPU_EVENT_PCH# OUT 19 59
R4596 1 2 1K_5%_2_DY GPP_B18 59 OUT
R2 1 2 100K_5%_2_DY GC6_FB_EN_PCH
32 OUT PCI_SERR#
R4598 1 2 10K_5%_2
R4597 1 2 1K_5%_2_DY BBS GPP_B22

U4500 SKL_ULT
LPSS
AN8 GPP_B15/GSPI0_CS#
AP7 GPP_B16/GSPI0_CLK
AP8 GPP_B17/GSPI0_MISO
AR7 GPP_B18/GSPI0_MOSI
AM5 GPP_B19/GSPI1_CS#
AN7 GPP_B20/GSPI1_CLK
AP5 GPP_B21/GSPI1_MISO
AN5 GPP_B22/GSPI1_MOSI
59 19 IN GPU_EVENT_PCH# AB1 GPP_C8/UART0_RXD
19 OUT DGPU_HOLD_RST# R W4 AB2 GPP_C9/UART0_TXD
49 19 IN HDD_LOCK_LED# AB3 GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
19 IN UART2_RXD AD1 GPP_C20/UART2_RXD
19 OUT UART2_TXD AD2 GPP_C21/UART2_TXD
19 OUT UART2_RTS_N AD3 GPP_C22/UART2_RTS#
19 IN UART2_CTS_N AD4 GPP_C23/UART2_CTS#
35 19 OUT USB_UART_SEL U7 GPP_C16/I2C0_SDA
35 19 OUT ODD_MD# U6 GPP_C17/I2C0_SCL
35 19 OUT ODD_PRSNT# U8 GPP_C18/I2C1_SDA
35 19 OUT ODD_PWREN U9 GPP_C19/I2C1_SCL
Check
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL
3V3
F 1V8

ISH
INTEGRATED SENSOR HUB
3V3
GPP_D9 P2 BOARD_ID0 IN 19
GPP_D10 P3 BOARD_ID1 IN 19
GPP_D11 P4 BOARD_ID2 IN 19
GPP_D12 P1
GPP_D5/ISH_I2C0_SDA M4
GPP_D6/ISH_I2C0_SCL N3
GPP_D7/ISH_I2C1_SDA N1
GPP_D8/ISH_I2C1_SCL N2
1V8 F
GPP_F10/I2C5_SDA/ISH_I2C2_SDA AD11
GPP_F11/I2C5_SCL/ISH_I2C2_SCL AD12
WIRELESS LAN RF OFF
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA U1 WLAN_RF_OFF# OUT 19
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL U2 DGPU_PRSNT# IN 19
GPP_D15/ISH_UART0_RTS# U3 DGPU_PWROK IN 19 32 54
GPP_D16/ISH_UART0_CTS#/SML0BALERT# U4 FP_LOCK_N OUT 19 41
BLUEBOOTH RF OFF
GPP_C12/UART1_RXD/ISH_UART1_RXD AC1 FP_OFF IN 19 41
GPP_C13/UART1_TXD/ISH_UART1_TXD AC2 BUILD_ID0 IN 19
GPP_C14/UART1_RTS#/ISH_UART1_RTS# AC3 BUILD_ID1 IN 19
GPP_C15/UART1_CTS#/ISH_UART1_CTS# AB4 BUILD_ID2 IN 19
3V3
GPP_A18/ISH_GP0 AY8
GPP_A19/ISH_GP1 BA8
GPP_A20/ISH_GP2 BB7
GPP_A21/ISH_GP3 BA7
GPP_A22/ISH_GP4 AY7
GPP_A23/ISH_GP5 AW7
GPP_A12/BM_BUSY#/ISH_GP6 AP13

INTEL_H23951_BGA_1356P

P3V3S
R4504 1 2 49.9K_1%_2_DY UART2_RXD IN 19
R4511 1 2 49.9K_1%_2_DY UART2_TXD OUT 19
R4514 1 2 49.9K_1%_2_DY UART2_RTS_N OUT 19
R4516 1 2 49.9K_1%_2_DY UART2_CTS_N IN 19

P3V3S
R4531 1 2 10K_5%_2
55 19 OUT DGPU_HOLD_RST# R4522 0_5%_2_DY DGPU_HOLD_RST#_R IN 19
Q4500
PANJIT_2N7002KW_3P
6015B0167001

P3V3A
19 OUT BUILD_ID0 R4621 10K_5%_2
19 OUT BUILD_ID1 R4624 10K_5%_2
R4622 10K_5%_2_DY
R4626 10K_5%_2_DY

	BUILD_ID1	BUILD_ID0
DB	0	0
SI	0	1
PV	1	0
MV	1	1

P3V3A
19 OUT BUILD_ID2 R4623 10K_5%_2
R4625 10K_5%_2_DY

Dis/UMA

	DIS	UMA
R4623	Mount	NC
R4625	NC	Mount

P3V3A
19 OUT WLAN_RF_OFF# 1 R4584 2 10K_5%_2_DY

P3V3S
19 OUT DGPU_PRSNT# 1 R4589 2 10K_5%_2_DY
1 R4590 2 10K_5%_2
DGPU_PRSNT# :
UMA : Pull high
DIS : Pull down
BOM Change
BOM OPTION6

54 32 19 OUT DGPU_PWROK 1 R4591 2 100K_5%_2_DY
BOM OPTION3
DIS UMA
R4591 UNMOUNT MOUNT

P3V3S
41 19 OUT FP_LOCK_N 1 R4587 2 10K_5%_2_DY
P3V3A
41 19 OUT FP_OFF 2 R4553 1 10K_5%_2_DY

PLATFORM ID
P3V3A
19 OUT BOARD_ID0 R4610 10K_5%_2_DY
19 OUT BOARD_ID1 R4535 10K_5%_2_DY
19 OUT BOARD_ID2 R4599 10K_5%_2_DY
R4615 10K_5%_2
R4536 10K_5%_2
R4618 10K_5%_2

INVENTEC
TITLE 14" MI 2.0 Block Diagram
SIZE A3 | CODE CS | DOC.NUMBER 1310A28111-0-CPT | REV A
SHEET 19 of 67
CHANGE by <ENG>Abel | DATE 08-APR-2016
PCB P/N 6050A2811101 | PCB VER <VER>

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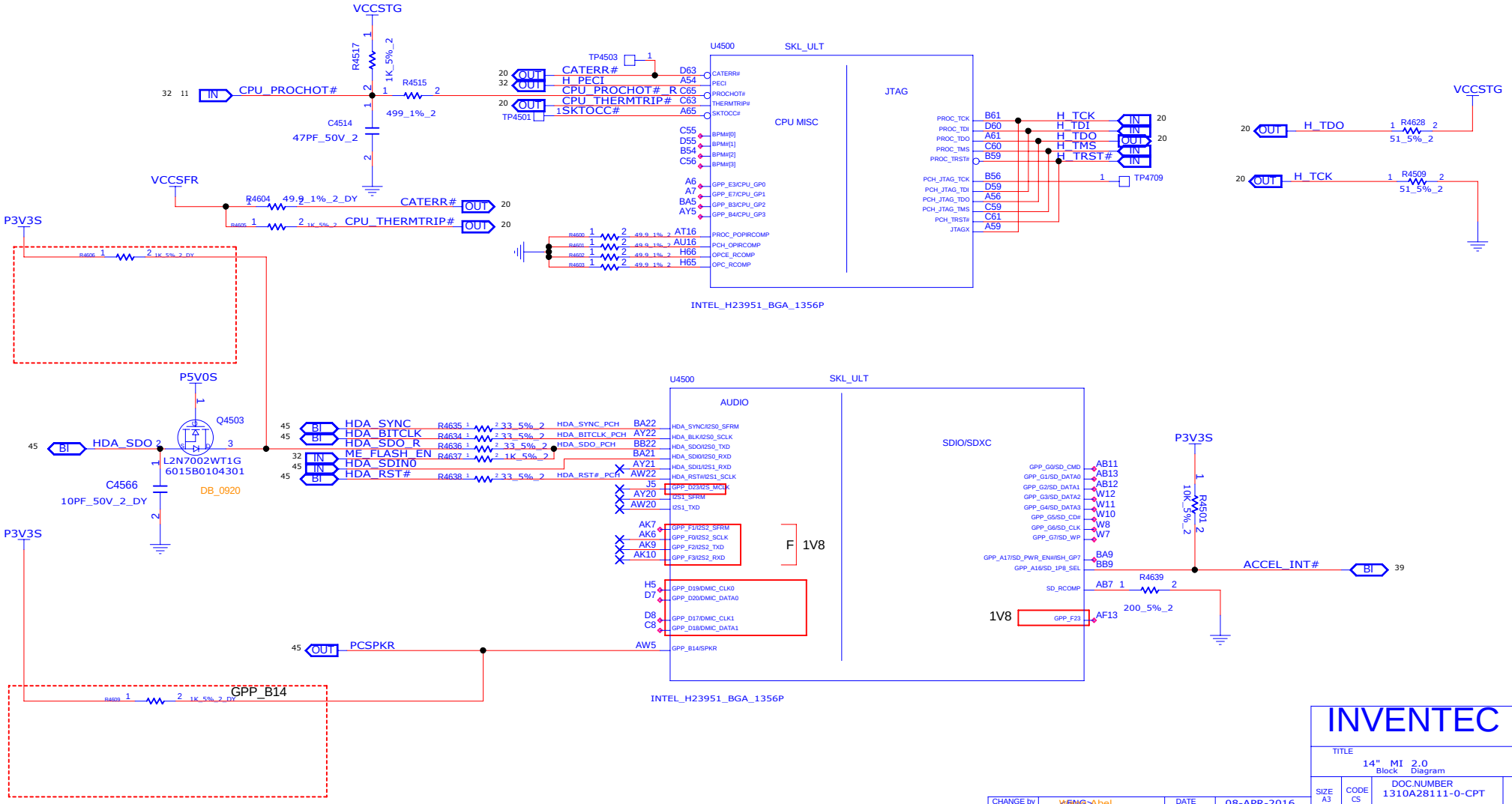
543016 60.3.31: ALL UNUSED GPIOS (WHICH DEFAULT TO GPIO FUNCTIONALITY) DO NOT NEED TERMINATION



CHANGE by	<ENG> Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 20 of 67

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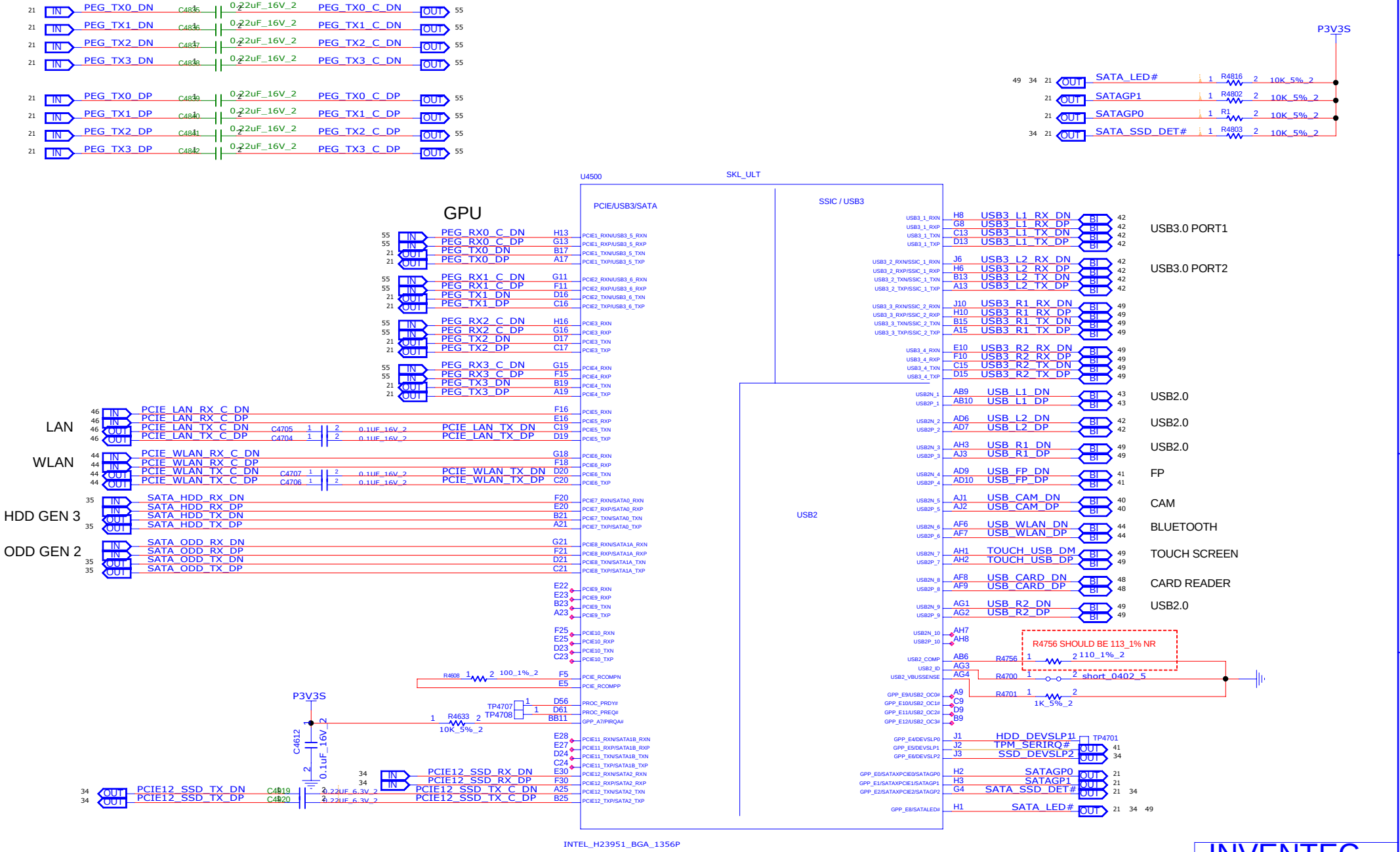

CHANGE by	<ENG> Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 21 of 67

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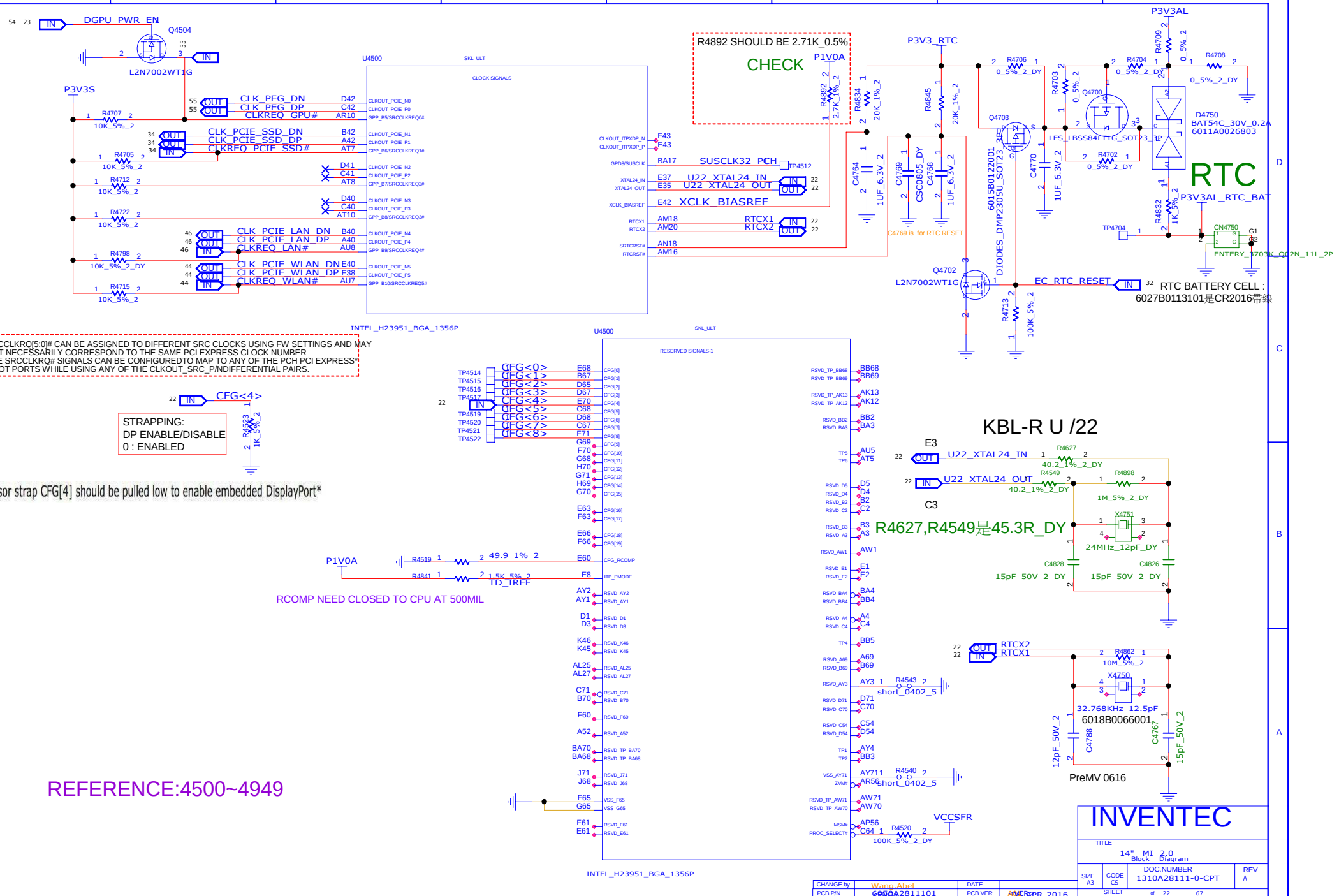

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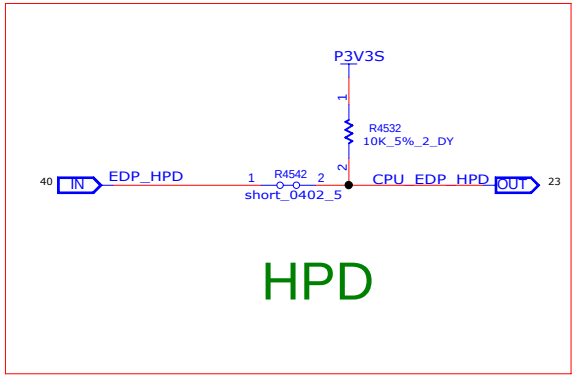

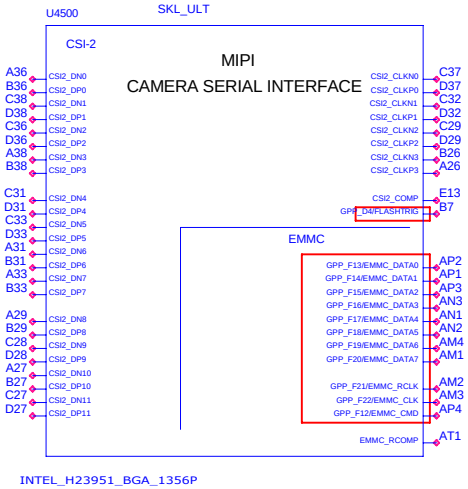

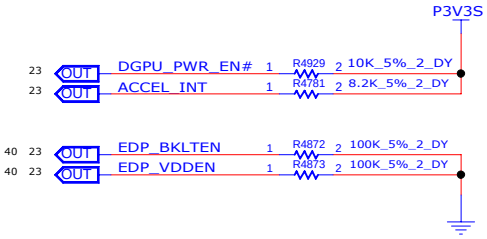

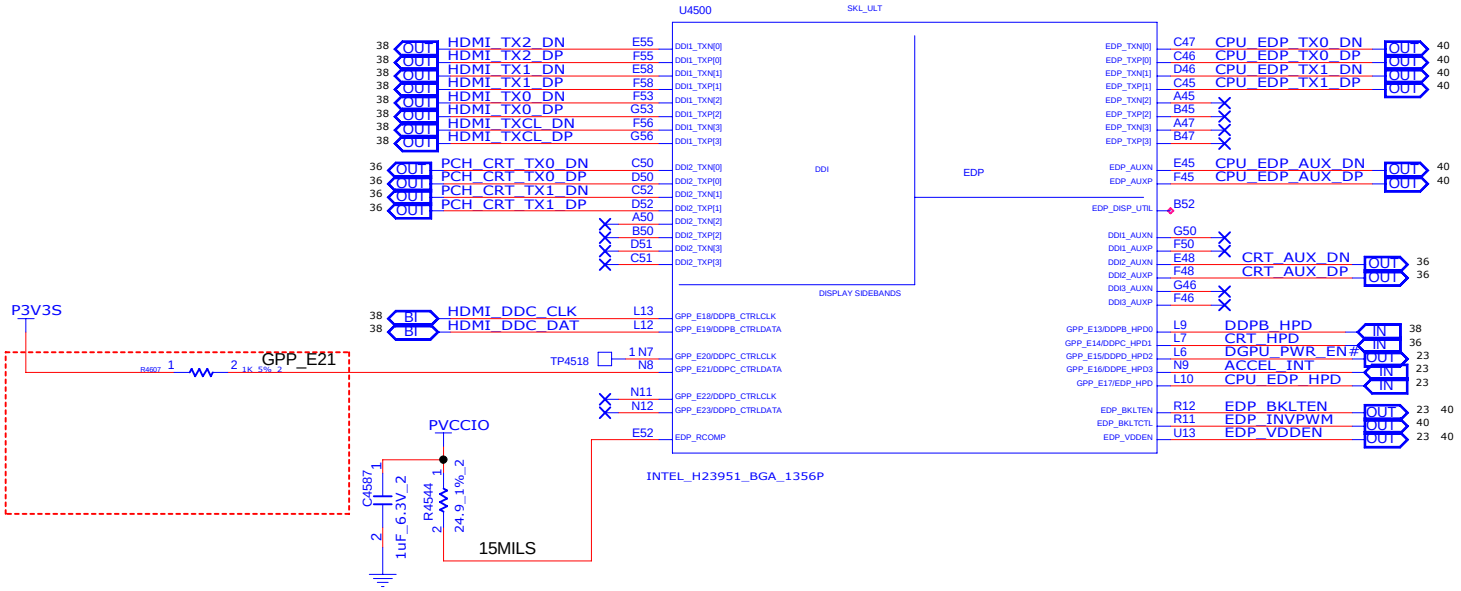

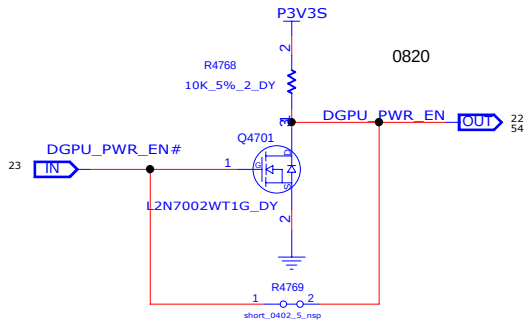

CHANGE by	<ENG>Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 23 of 67

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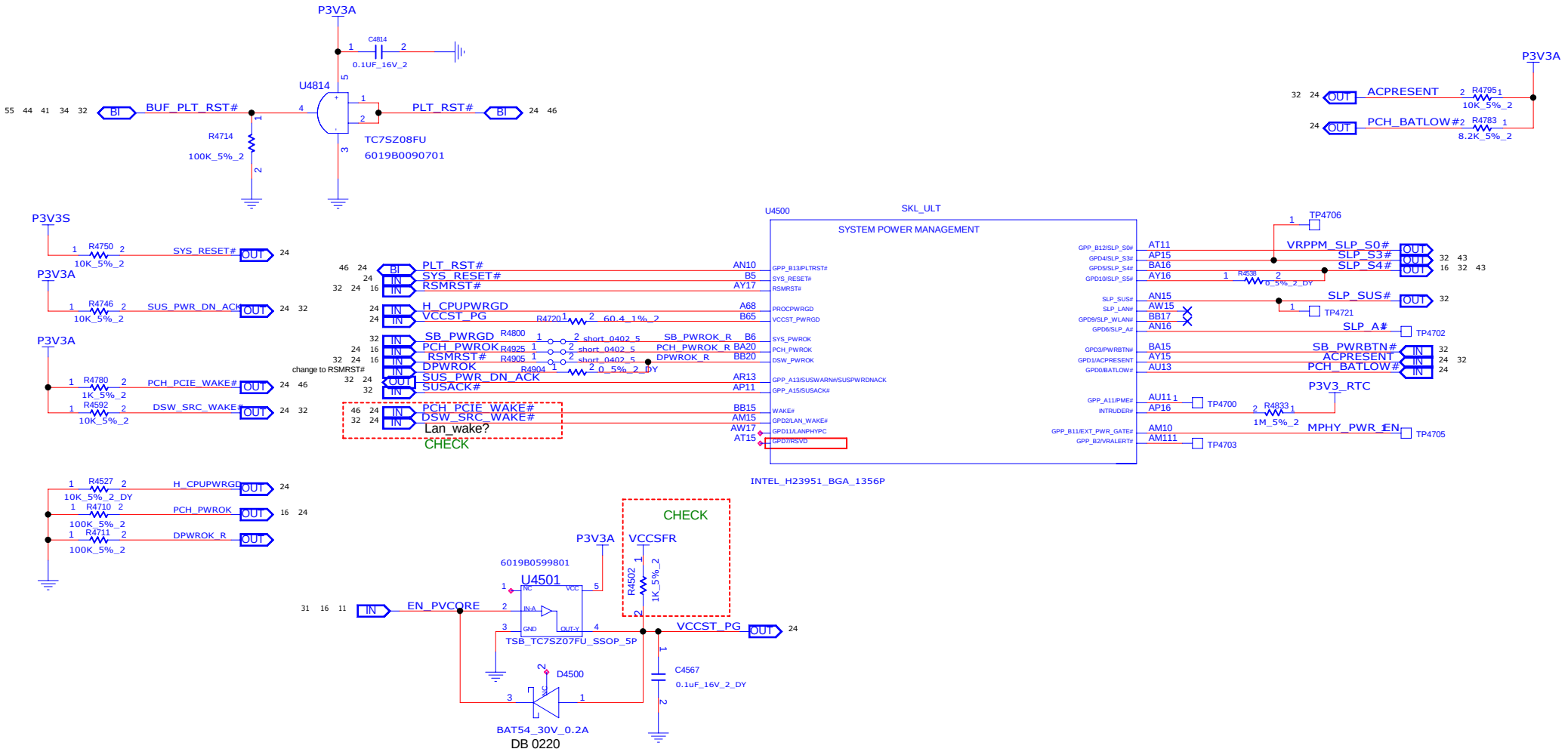

CHANGE by	<VENG>Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 24 of 67

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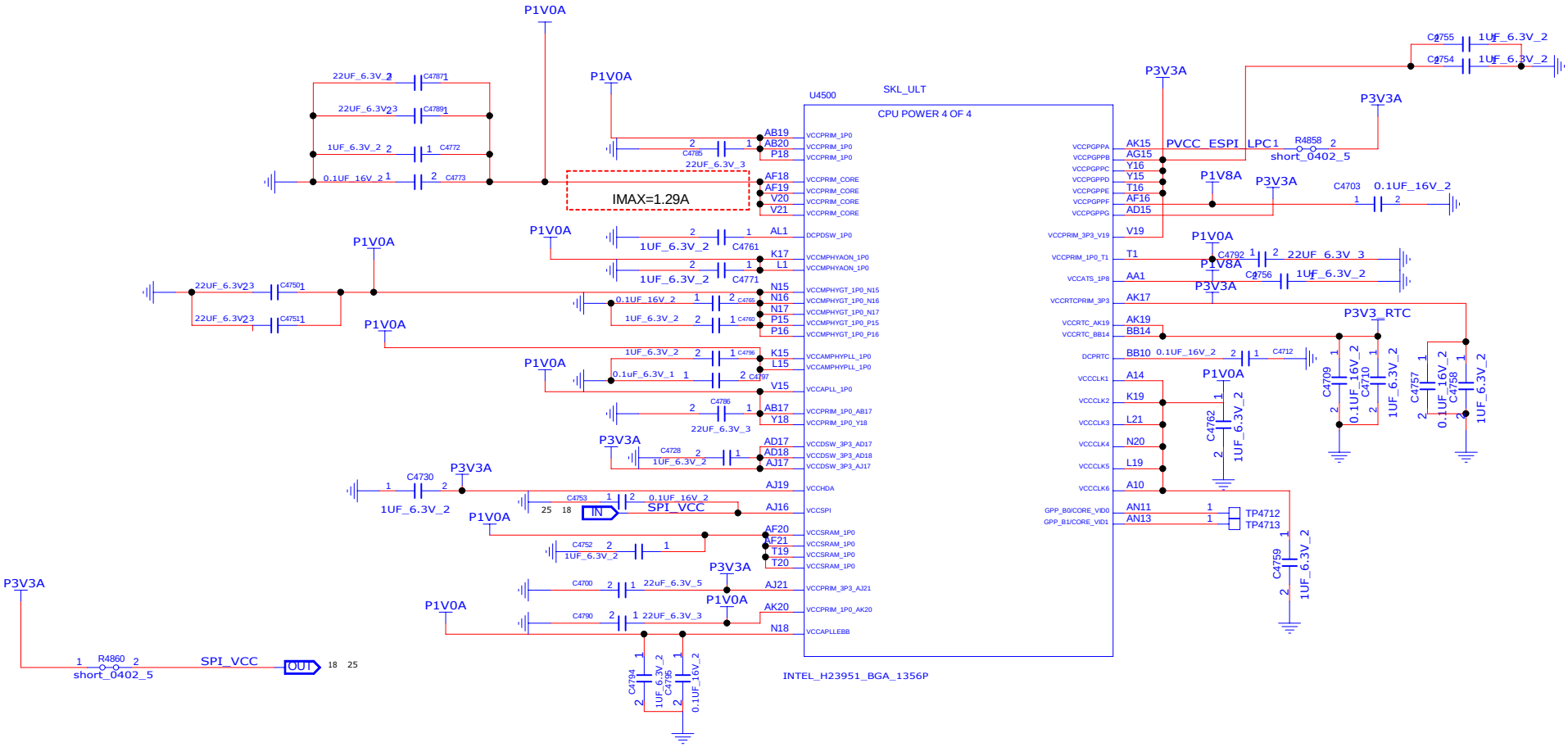
REFERENCE 4700~4949(PCH)



CHANGE by	Wang,Abel	DATE	
PCB P/N	6050A2811101	PCB VER	A

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET of 25 67

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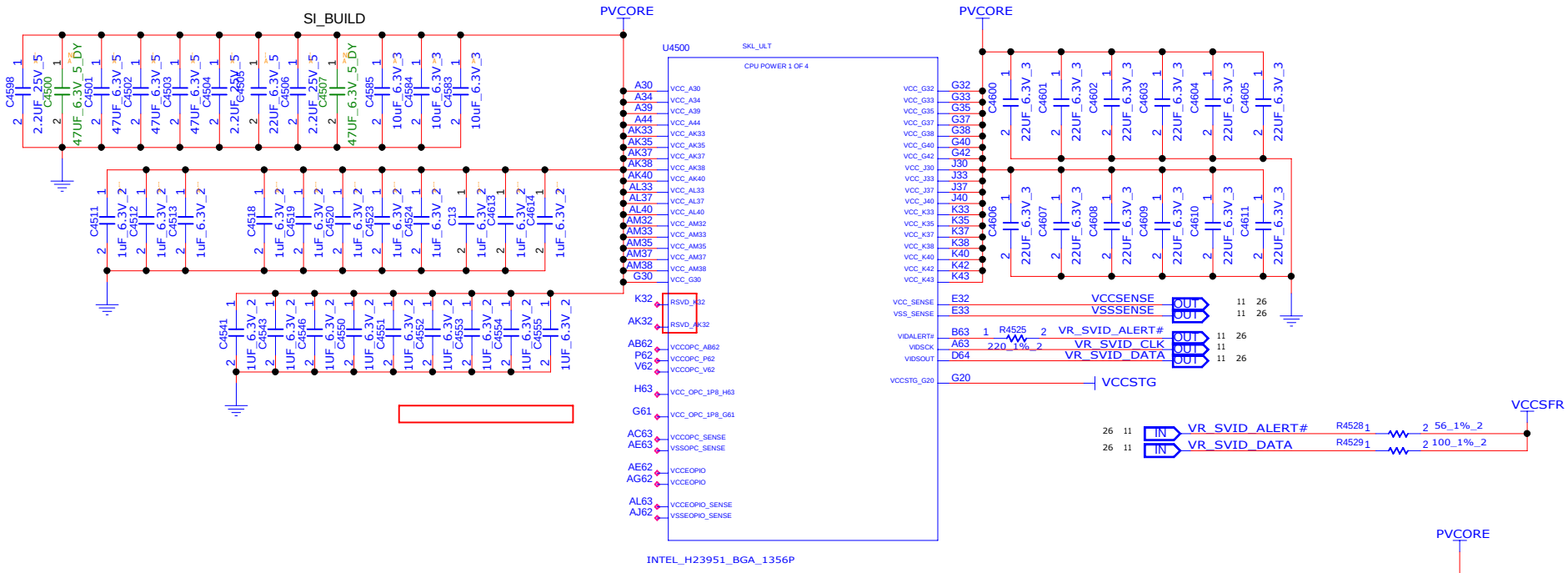

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	<ENG>	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>
SHEET 26 of 67			

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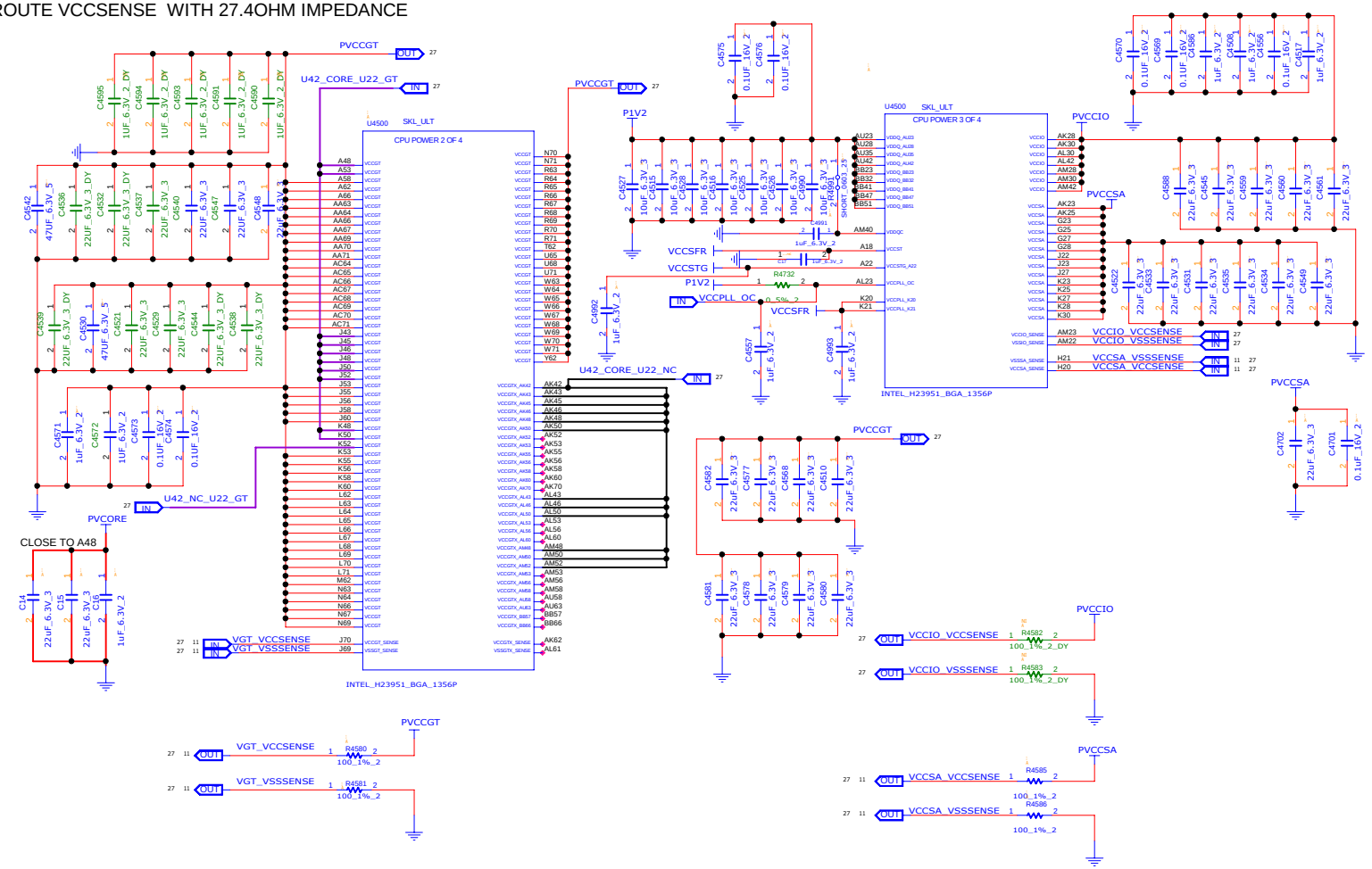
ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



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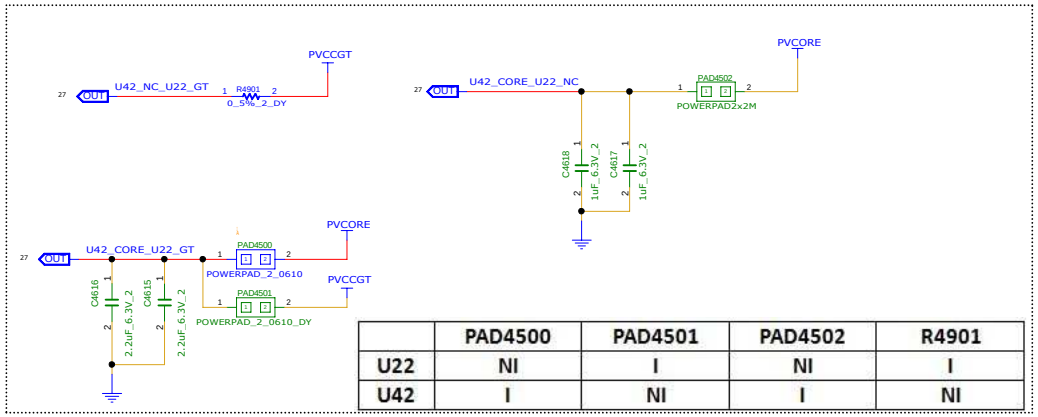

	PAD4500	PAD4501	PAD4502	R4901
U22	NI	I	NI	I
U42	I	NI	I	NI

INVENTEC

14" MI 2.0
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 27 of 67

CHANGE SE		DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A

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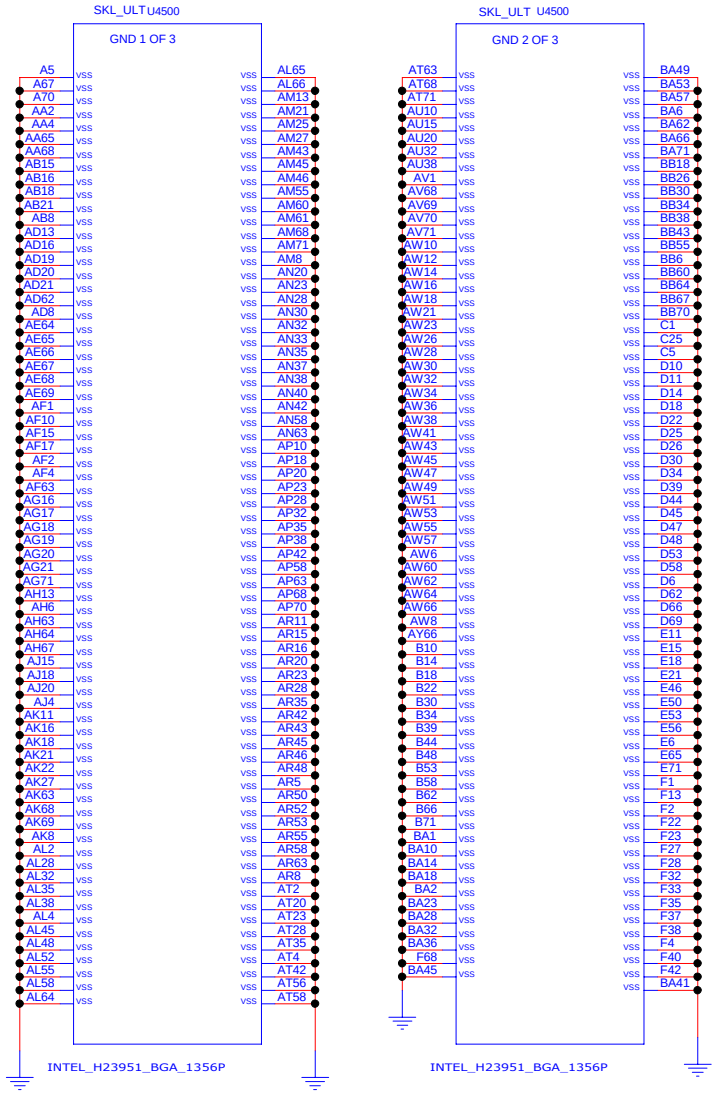

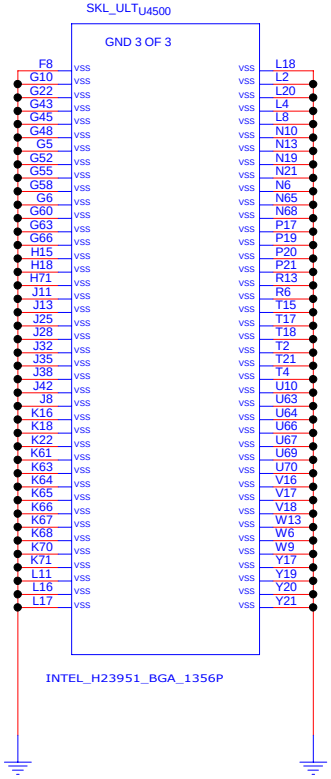

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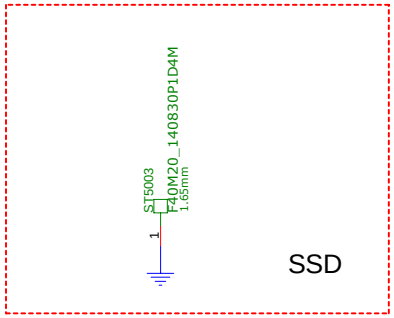
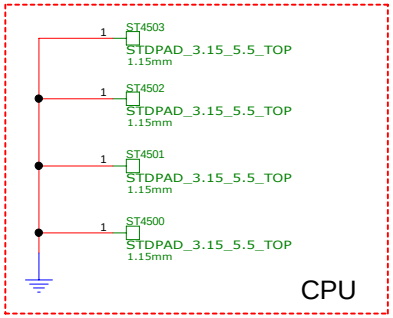
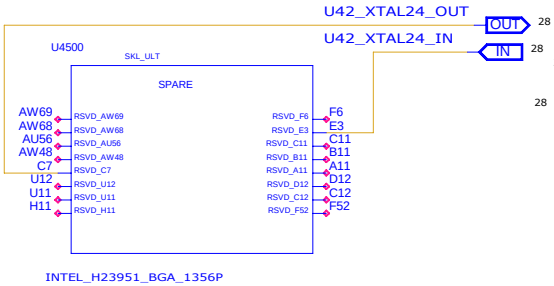
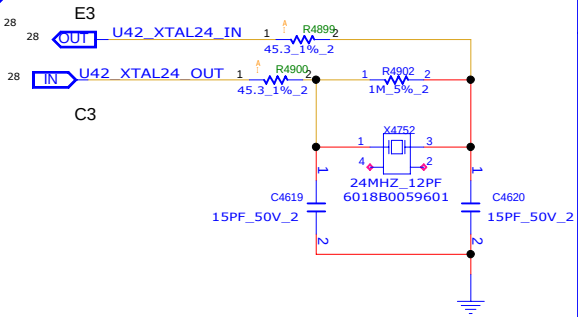






KBL-R U /42



INVENTEC

TITLE	14" MI 2.0 Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT			REV A
CHANGE by	<ENG> Abel	DATE	08-APR-2016	SHEET 28 of 67	
PCB P/N	6050A2811101	PCB VER	<VER>		

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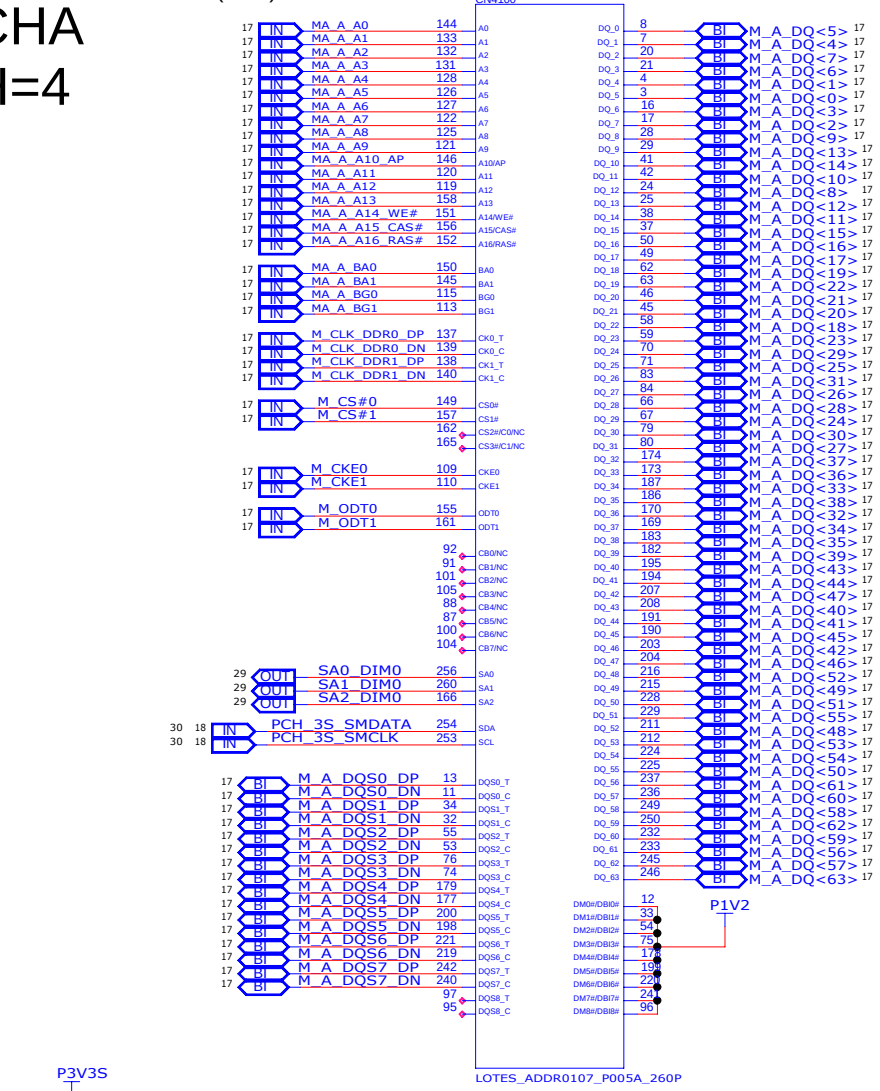
07e20411070e0102900018f4ea003be7

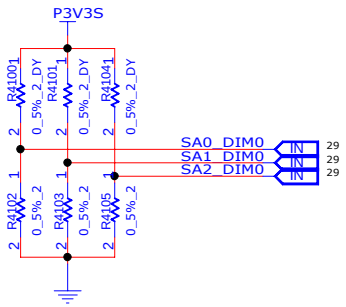
REFERENCE 4100~4299(DDR)

CHA

H=4

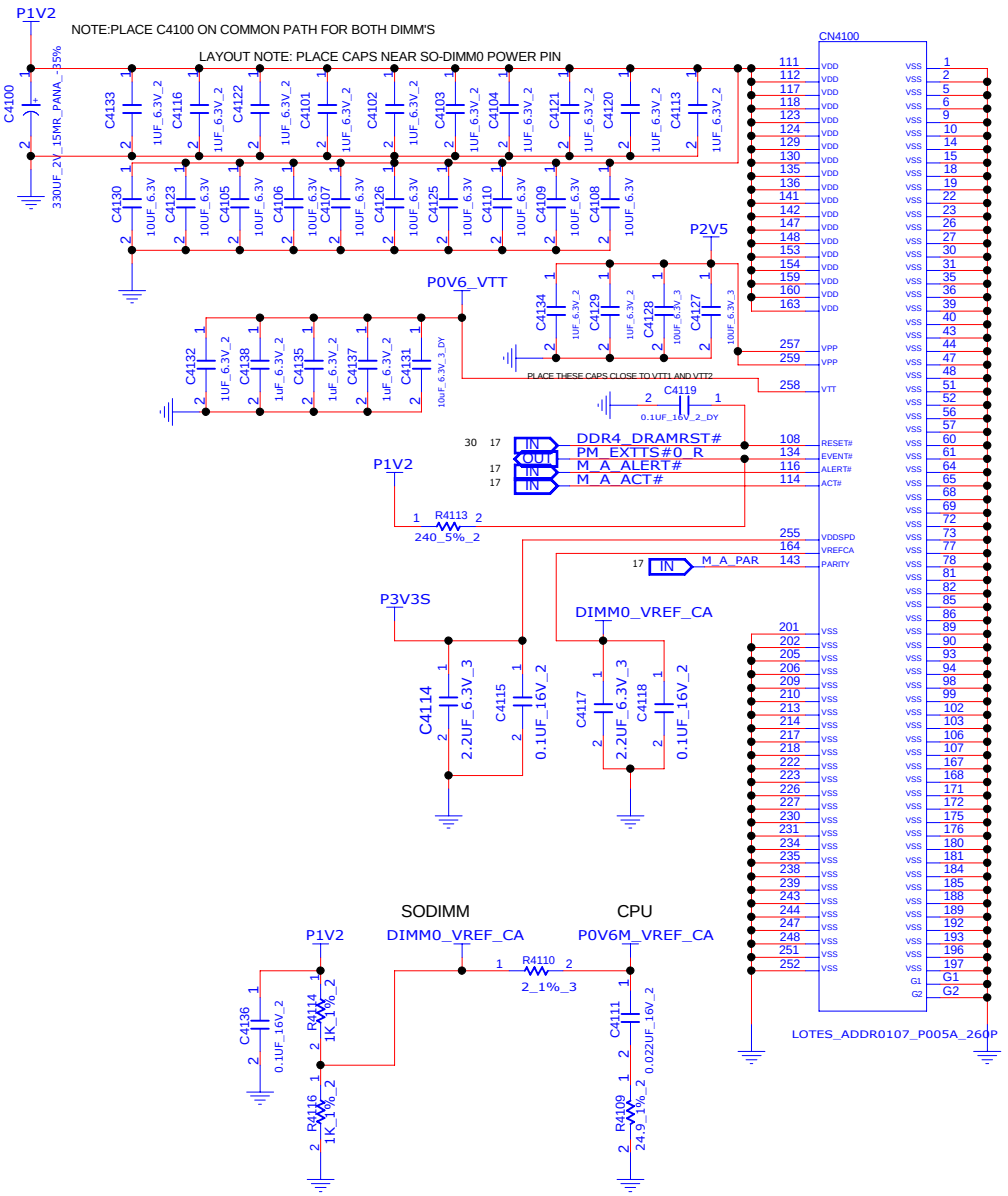
CN4100 6026B0328101 SOCKET,DDD4-DIMM,260P,0.5mm,GOLD,10U,4.8MM,90D,SMD,REVERSE,TR





SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS:0XA0
RED ADDRESS :0XA1
SA0=0,SA1=0,SA2=0
DDR4 FOR OPERATING SPEED:1867 MT/S

STRETCH GOAL IS 2133 MT/S
EVENT_N: INDICATES THERMAL EVENT ON DIMM.
EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH



CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 29 of 67

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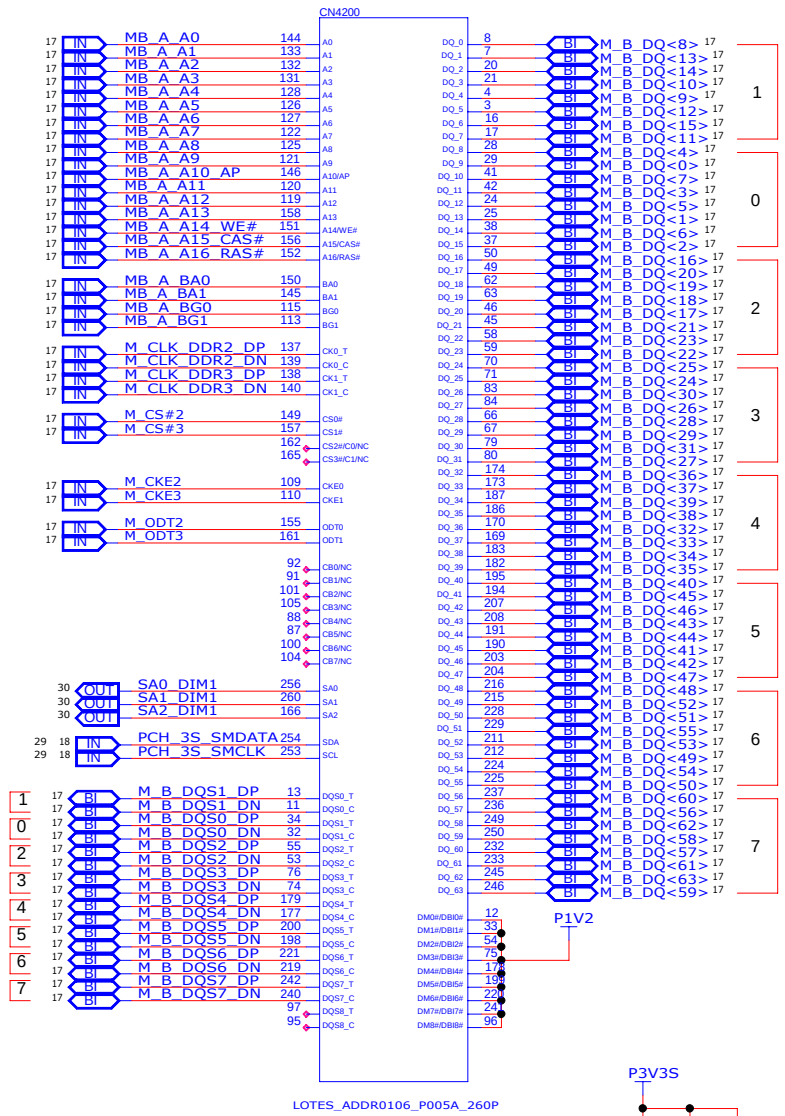
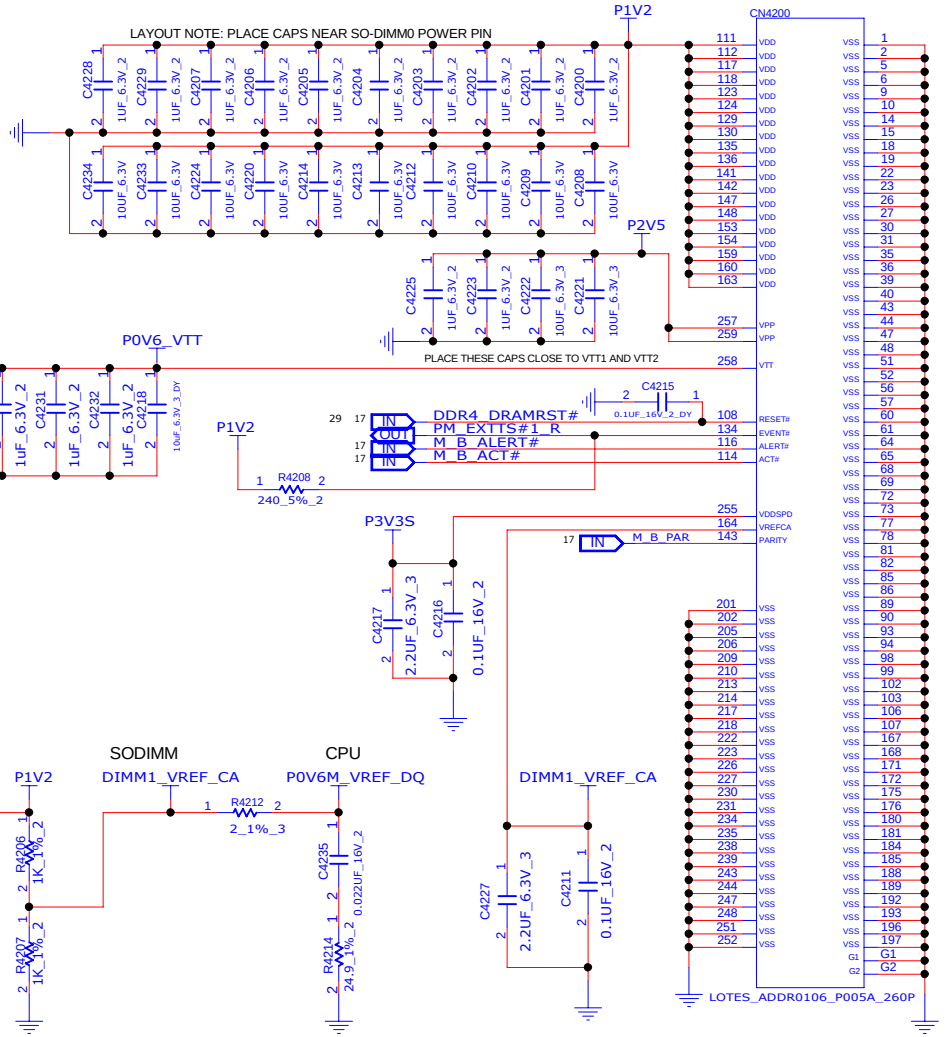
07e20411070e0102900018f4ea003be7

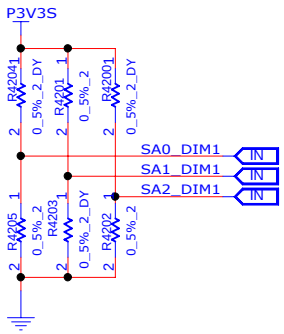
REFERENCE 4100~4299(DDR)

CHB
H=4

CN4200 6026B0328201 SOCKET,DDR4-DIMM,260P,0.5mm,GOLD,10U,4.0MM,90D,SMD,STANDARD,TR







SPD ADDRESS FOR CHANNEL-1
WRITE ADDRESS:0XA4
RED ADDRESS :0XA3
SA0=0,SA1=1,SA2=0

DDR4 FOR OPERATING SPEED:1867 MT/S
STRETCH GOAL IS 2133 MT/S

EVENT_N: INDICATES THERMAL EVENT ON DIMM.
EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01
SHEET 30 of 67			

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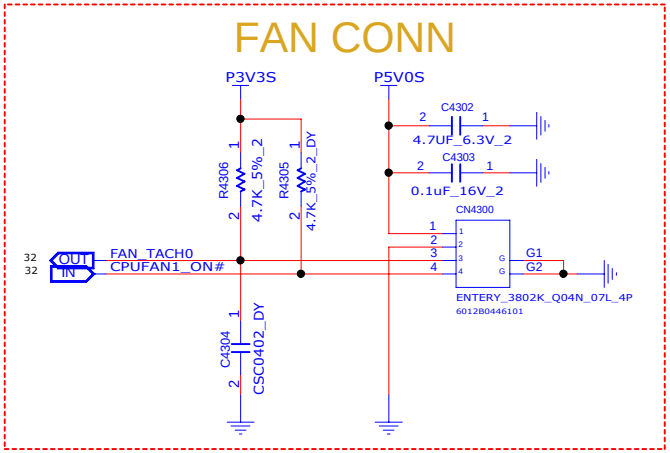

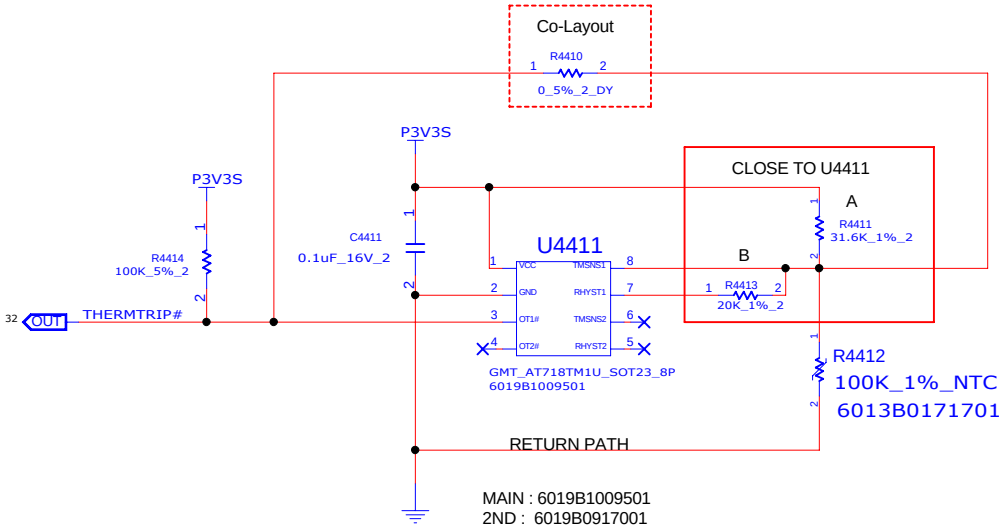

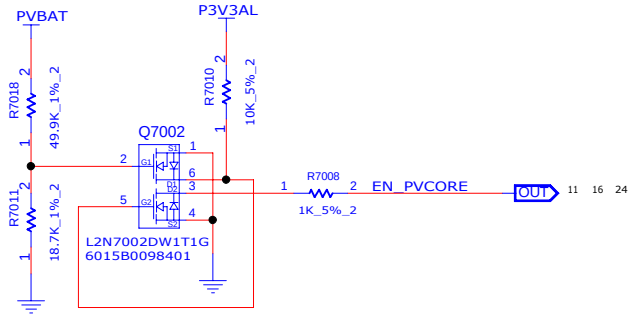

INVENTEC

TITLE	14" MI 2.0 THERMAL & FAN		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET 31 of 67			

CHANGE by	<ENG> Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

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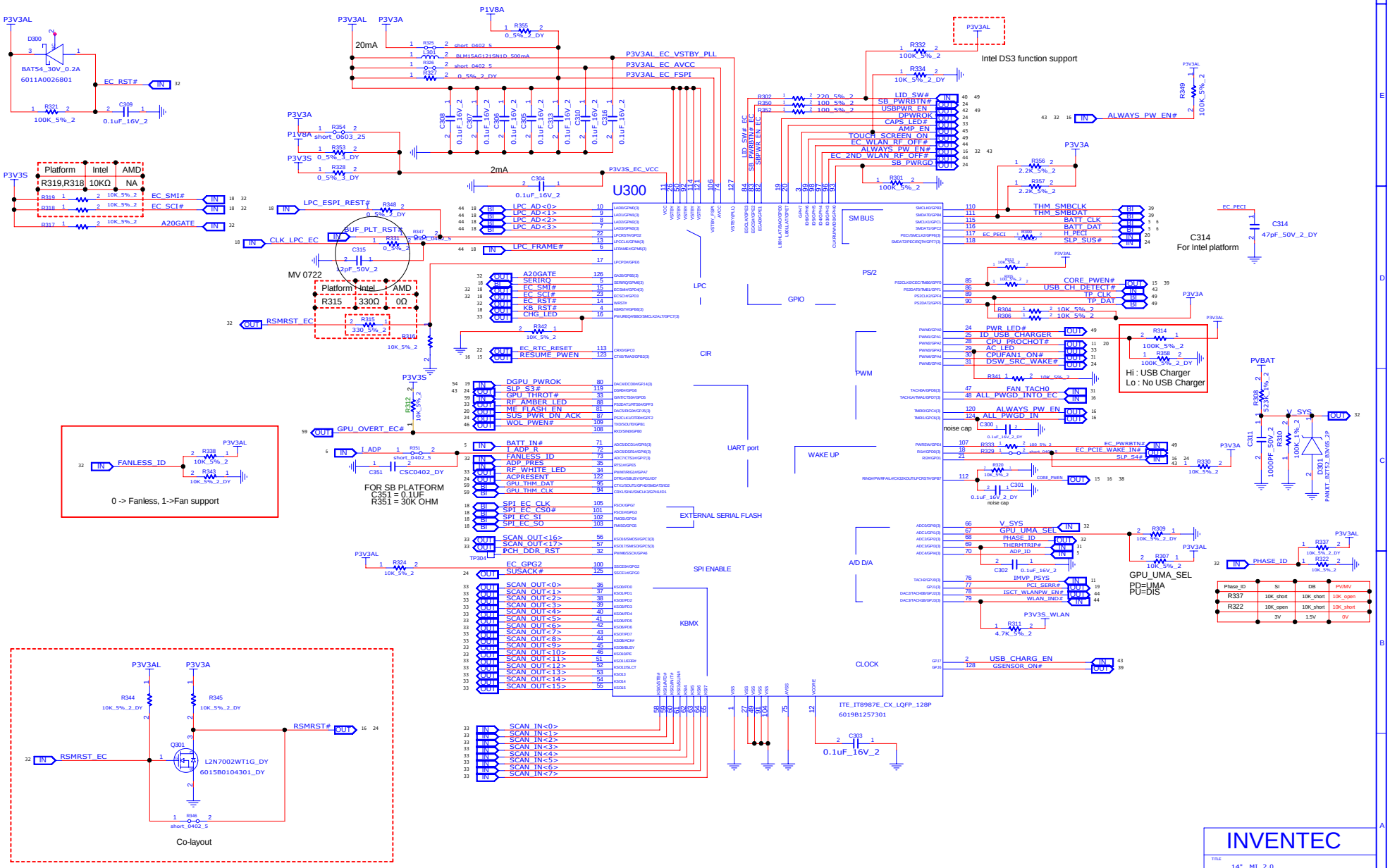
EC

Location 300 ~ 389

2013EE1B

Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5



Platform	Intel	AMD
R319,R318	10KΩ	NA

Platform	Intel	AMD
R315	330Ω	0Ω

Phase_ID	SI	DB	PVMV
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

INVENTEC

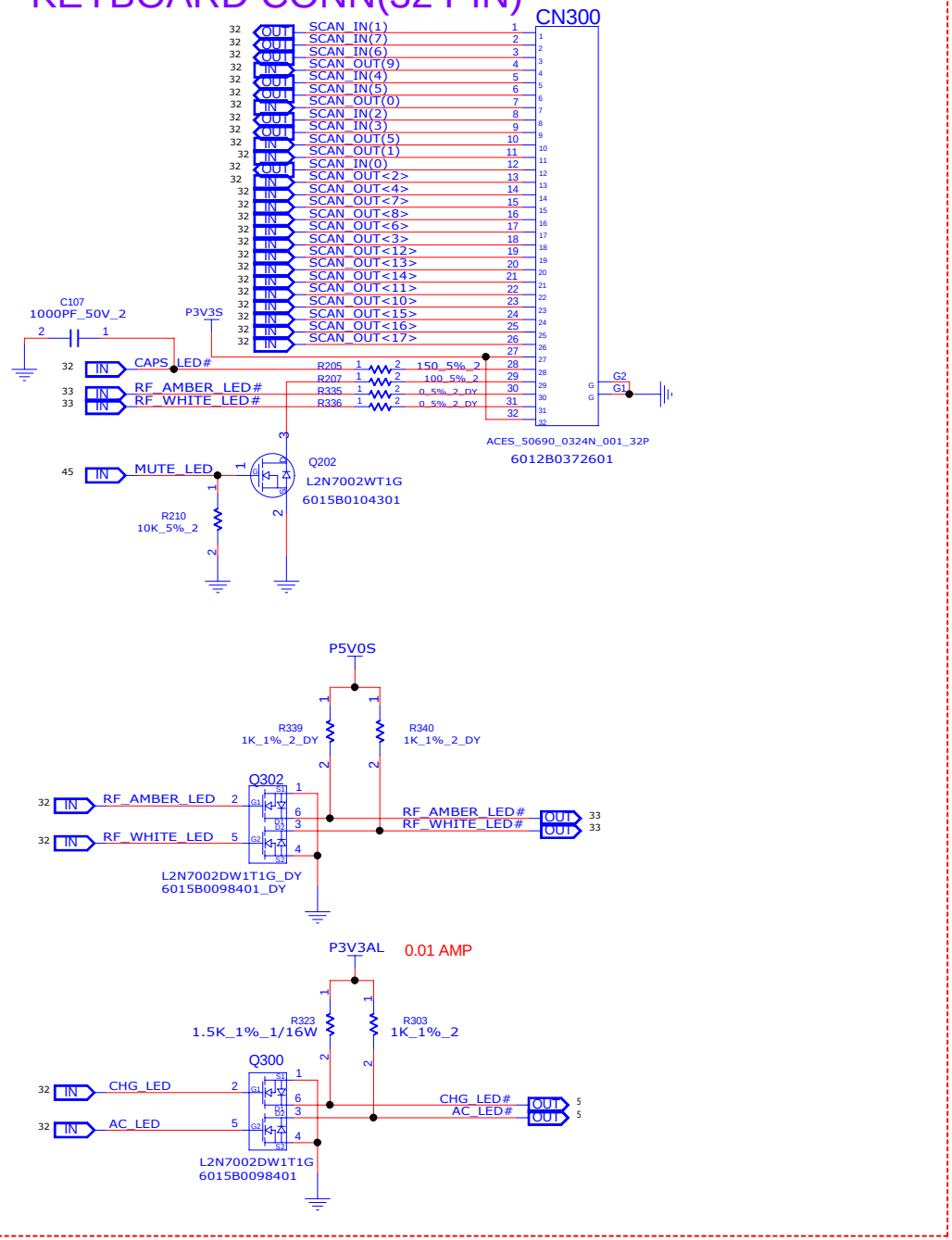
14" MI 2.0 Block Diagram

CHANGE NO		DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A0ER2

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A2811-0-CPT	A
SHEET	32	of	67

07e20411070e0102900018f4ea003be7

KEYBOARD CONN(32 PIN)



CHANGE by	<ENG> Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 KB CONN & LED

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 33 of 67

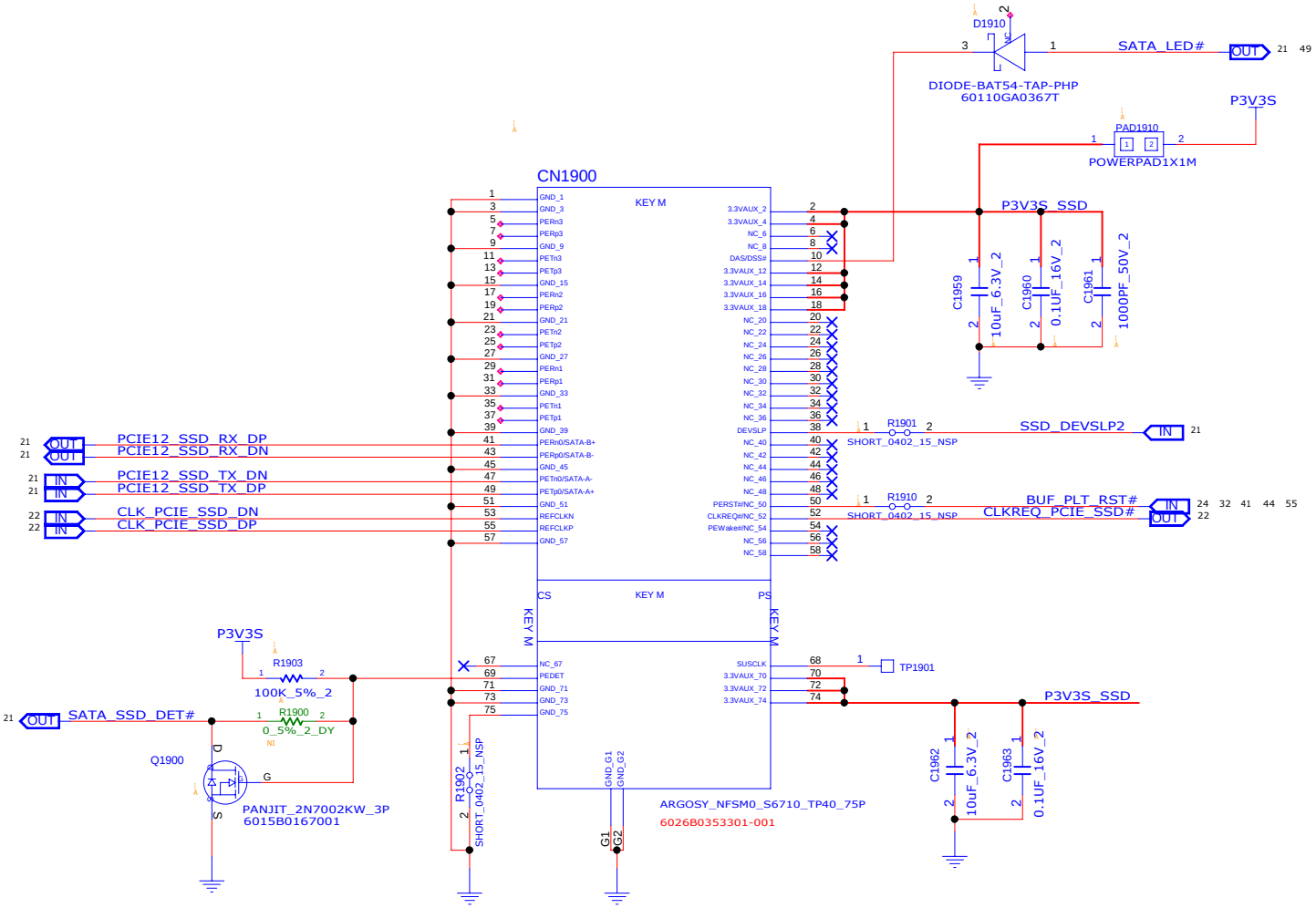
07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

M.2 SSD

REFERENCE NUMBER:1900~1949

Pin	Type	Description
1	CONFIG_3	Ground (according to M.2 configurations for SSD-SATA definition)
2	3.3V	Supply Pin, 3.3V
3	GND	Ground
4	3.3V	Supply pin, 3.3V
5	No connect	No connect
6	Not available	No connect (used for other purposes)
7	Not available	No connect (used for other purposes)
8	Not available	No connect (used for other purposes)
9	No connect	No connect
10	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
11	No connect	No connect (used for other purposes)
12	(removed for key)	Mechanical notch B
13	(removed for key)	Mechanical notch B
14	(removed for key)	Mechanical notch B
15	(removed for key)	Mechanical notch B
16	(removed for key)	Mechanical notch B
17	(removed for key)	Mechanical notch B
18	(removed for key)	Mechanical notch B
19	(removed for key)	Mechanical notch B
20	Not available	No connect (used for other purposes)
21	CONFIG_0	Ground (according to M.2 configurations for SSD-SATA definition)
22	Not available	No connect (used for other purposes)
23	Not available	No connect (used for other purposes)
24	Not available	No connect (used for other purposes)
25	Not available	No connect (used for other purposes)
26	Not available	No connect (used for other purposes)
27	GND	Ground
28	Not available	No connect (used for other purposes)
29	PERn1	Not used
30	Not available	No connect (used for other purposes)
31	PERp1	Not used
32	Not available	No connect (used for other purposes)
33	GND	Ground
34	Not available	No connect (used for other purposes)
35	PETn1	Not used
36	Not available	No connect (used for other purposes)
37	PETp1	Not used
38	DEVSLP	Device Sleep, input. If driven high the host is informing the SSD to enter a low power state (optional)
39	GND	Ground
40	Not available	No connect (used for other purposes)
41	SATA-Rx+	Host receiver differential signal pair
42	Not available	No connect (used for other purposes)
43	SATA-Rx-	Host receiver differential signal pair
44	Not available	No connect (used for other purposes)
45	GND	Ground
46	Not available	No connect (used for other purposes)
47	SATA-Tx-	Host transmitter differential pair
48	Not available	No connect (used for other purposes)
49	SATA-Tx+	Host transmitter differential pair
50	PERST#	Not used
51	GND	Ground
52	CLKREQ#	Not used
53	REFCLKN	Not used
54	PEWAKE#	Not used
55	REFCLKP	Not used
56	MFG1	Manufacturing pin. Use determined by vendor (no connect on a host)
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor (no connect on a host)
59	(removed for key)	Mechanical notch B
60	(removed for key)	Mechanical notch B
61	(removed for key)	Mechanical notch B
62	(removed for key)	Mechanical notch B
63	(removed for key)	Mechanical notch B
64	(removed for key)	Mechanical notch B
65	(removed for key)	Mechanical notch B
66	(removed for key)	Mechanical notch B
67	Not available	No connect (used for other purposes)
68	SUSCLK	Not used
69	CONFIG_1	Ground
70	3.3V	Supply pin, 3.3V
71	GND	Ground
72	3.3V	Supply pin, 3.3V
73	GND	Ground
74	3.3V	Supply pin, 3.3V
75	CONFIG_2	Ground



CHANGE by	WENG>Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 NGFF- SSD

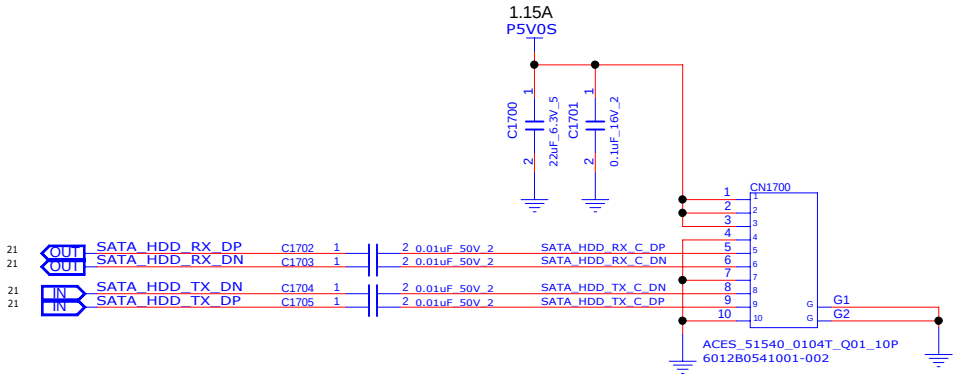
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET of 34 67

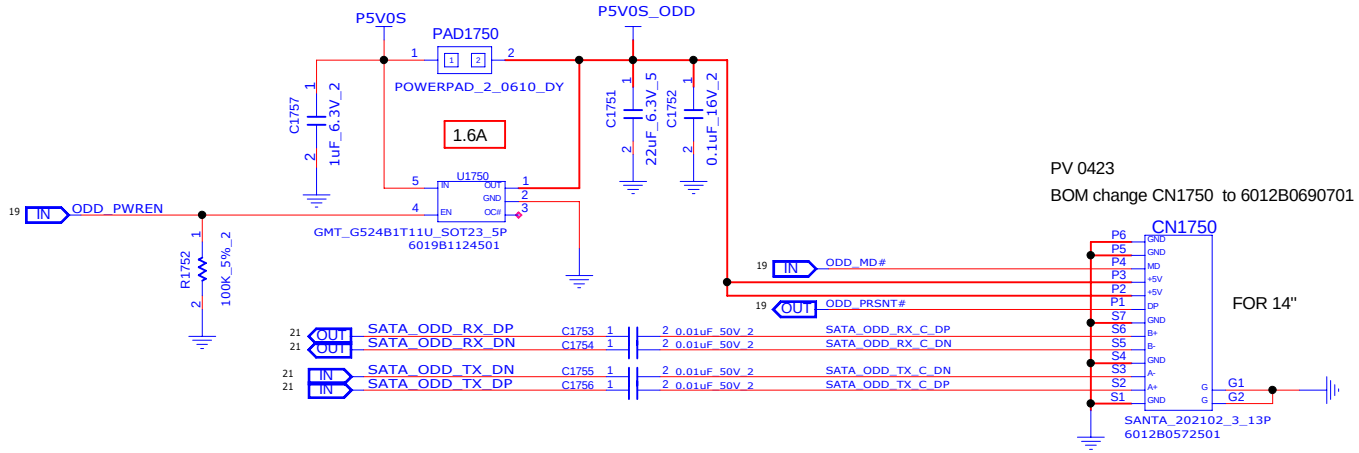
07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

SATA HDD CABLE CONN on MB



Zero Power ODD CONN on MB



CHANGE by	Wang,Abel	DATE	
PCB P/N	6050A2811101	PCB VER	A

INVENTEC

TITLE: 14" MI 2.0 SATA HDD & SATA ODD

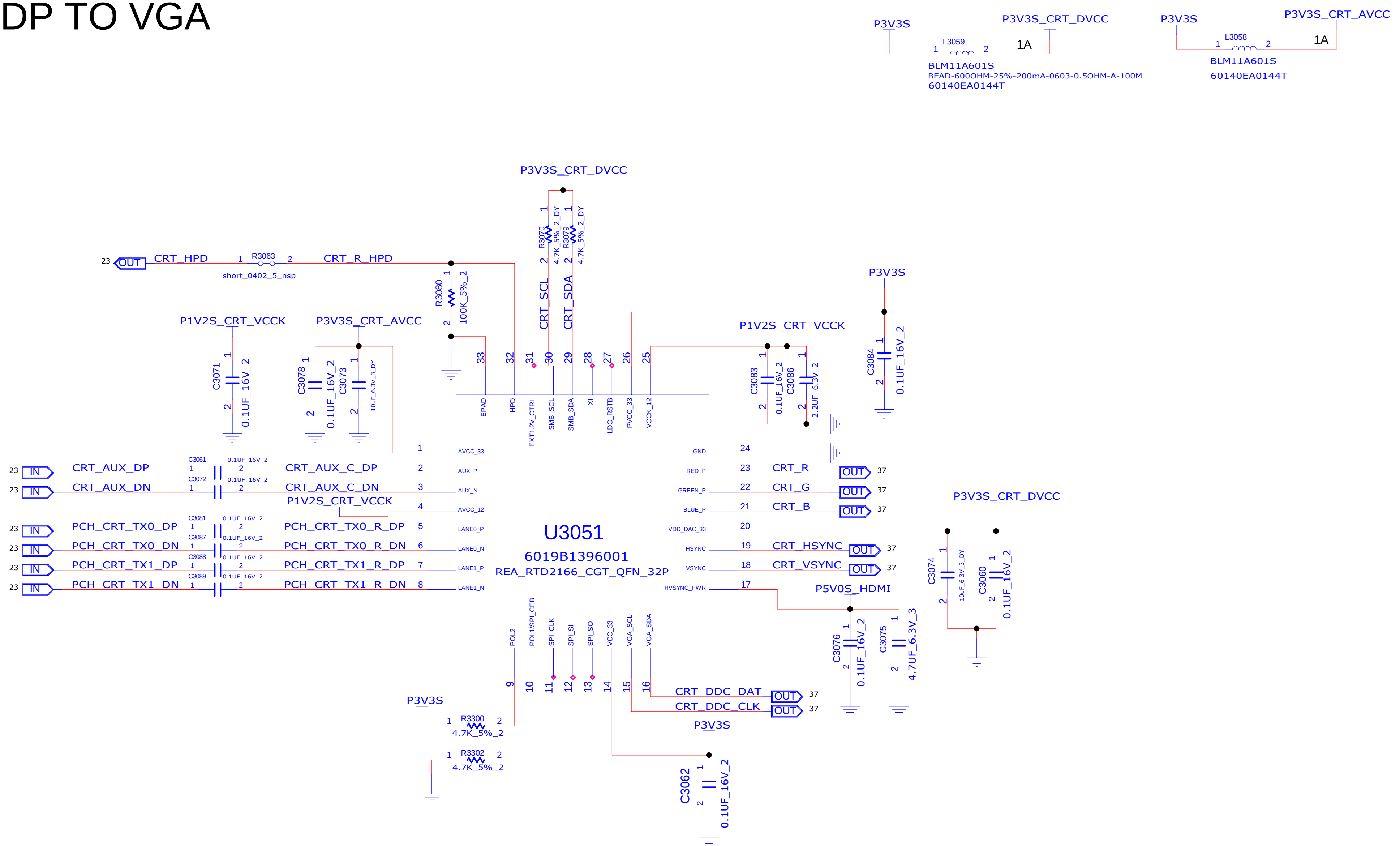
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET of 35 67

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

EDP TO VGA



		POL1	
		0	1
POL2	0	X	X
	1	ROM Mode	Ext. Flash Mode

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE: A3 | CODE: CS | DOC.NUMBER: 1310A28111-0-CPT | REV: A

CHANGE by: Wang.Abel | DATE: 08-APR-2016

PCB P/N: 6050A2811101 | PCB VER: A00

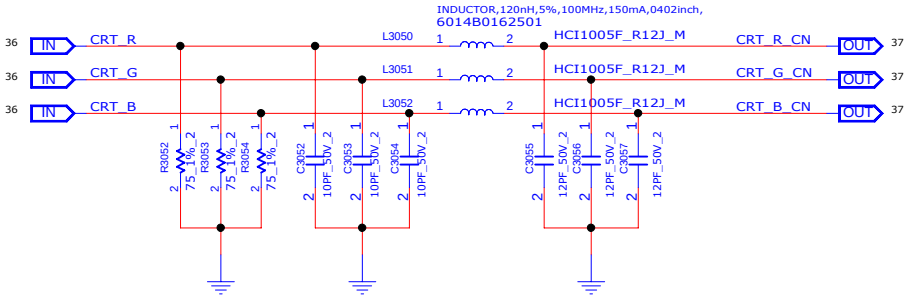
SHEET 36 of 67

07e20411070e0102900018f4ea003be7

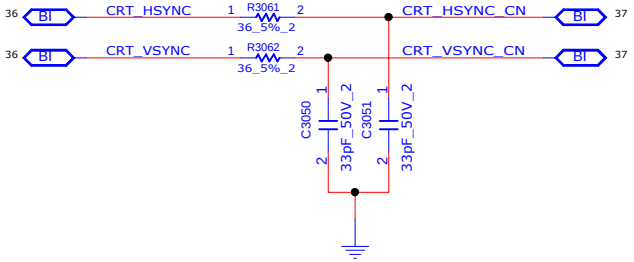
07e20411070e0102900018f4ea003be7

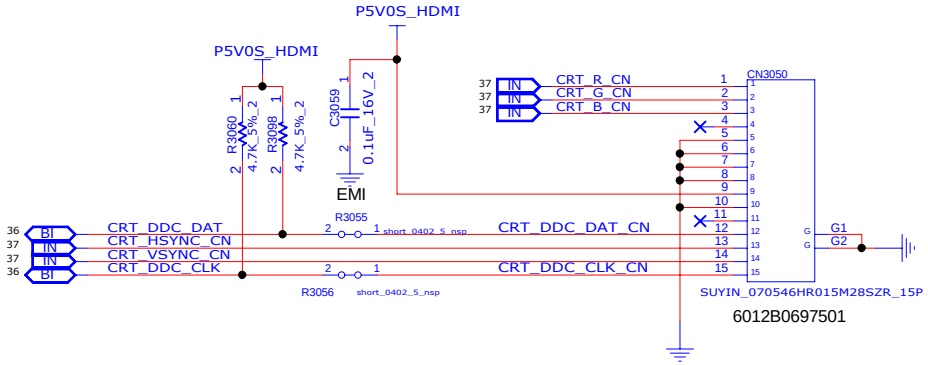
CRT

LOCATION 3050~3099
VER.01_20120807

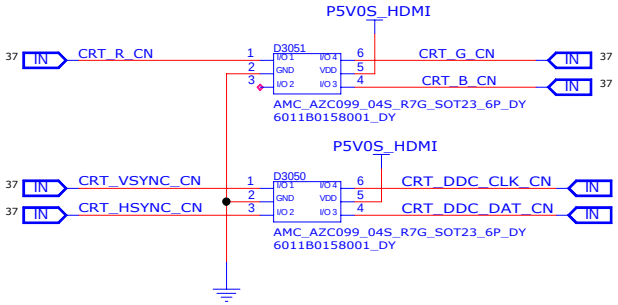


R3052, R3053, R3054 :
Intel---> 75ohm
AMD---> 150ohm





Close to CN3050



INVENTEC

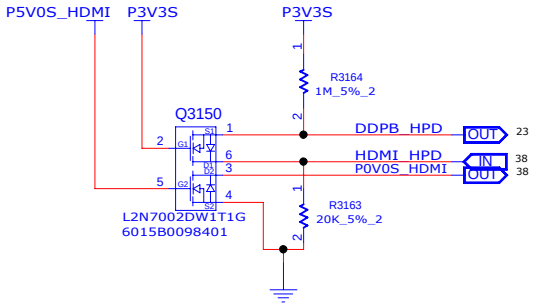
TITLE	14" MI 2.0 CRT CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01
SHEET 37 of 67			

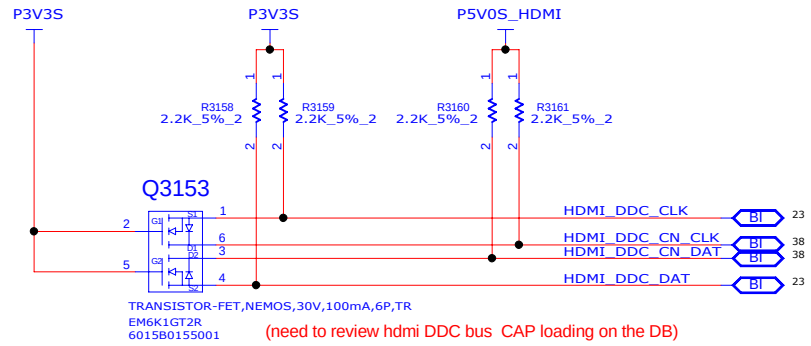
07e20411070e0102900018f4ea003be7

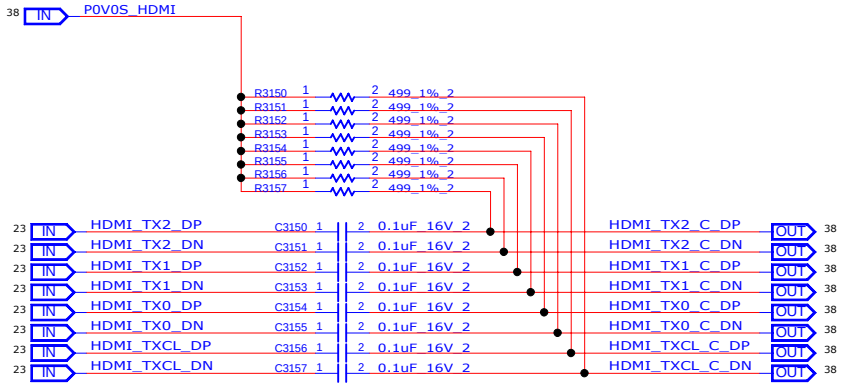
07e20411070e0102900018f4ea003be7

HDMI

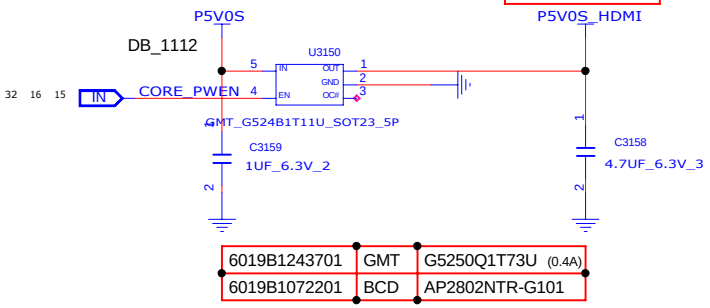
Location 3150 ~ 3199
Ver.01_20120807



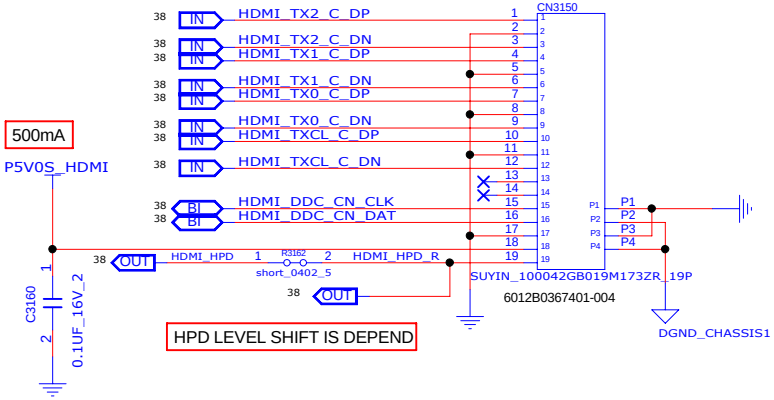


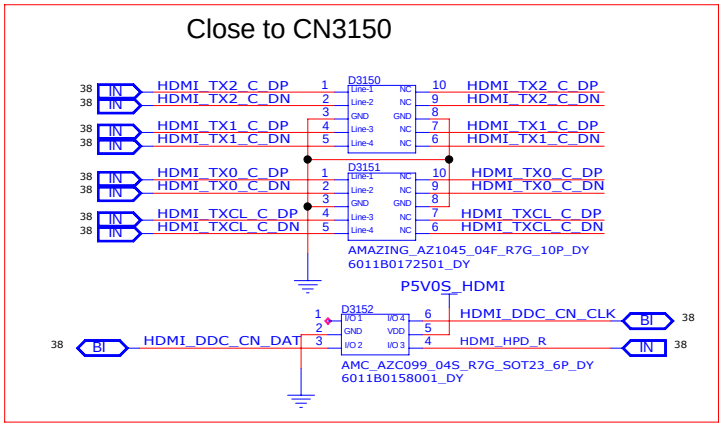


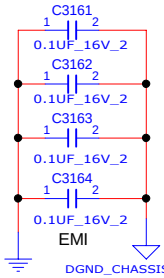
For CRT & HDMI



6019B1243701	GMT	G5250Q1T73U (0.4A)
6019B1072201	BCD	AP2802NTR-G101







INVENTEC

TITLE	14" MI 2.0 HDMI CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	<ENG> Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>
SHEET 38 of 67			

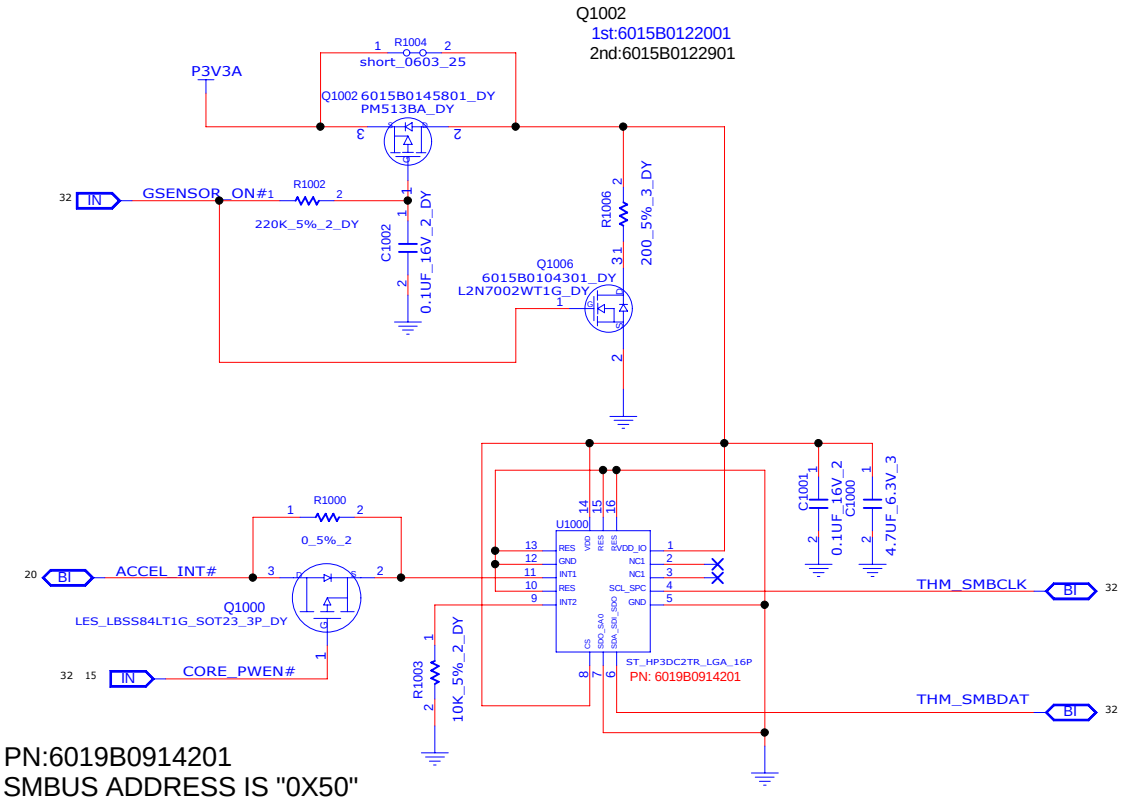
07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

G-Sensor

Loctaion 1000 ~ 1099
Ver.01_20120807

HARDDRIVE PROTECTION



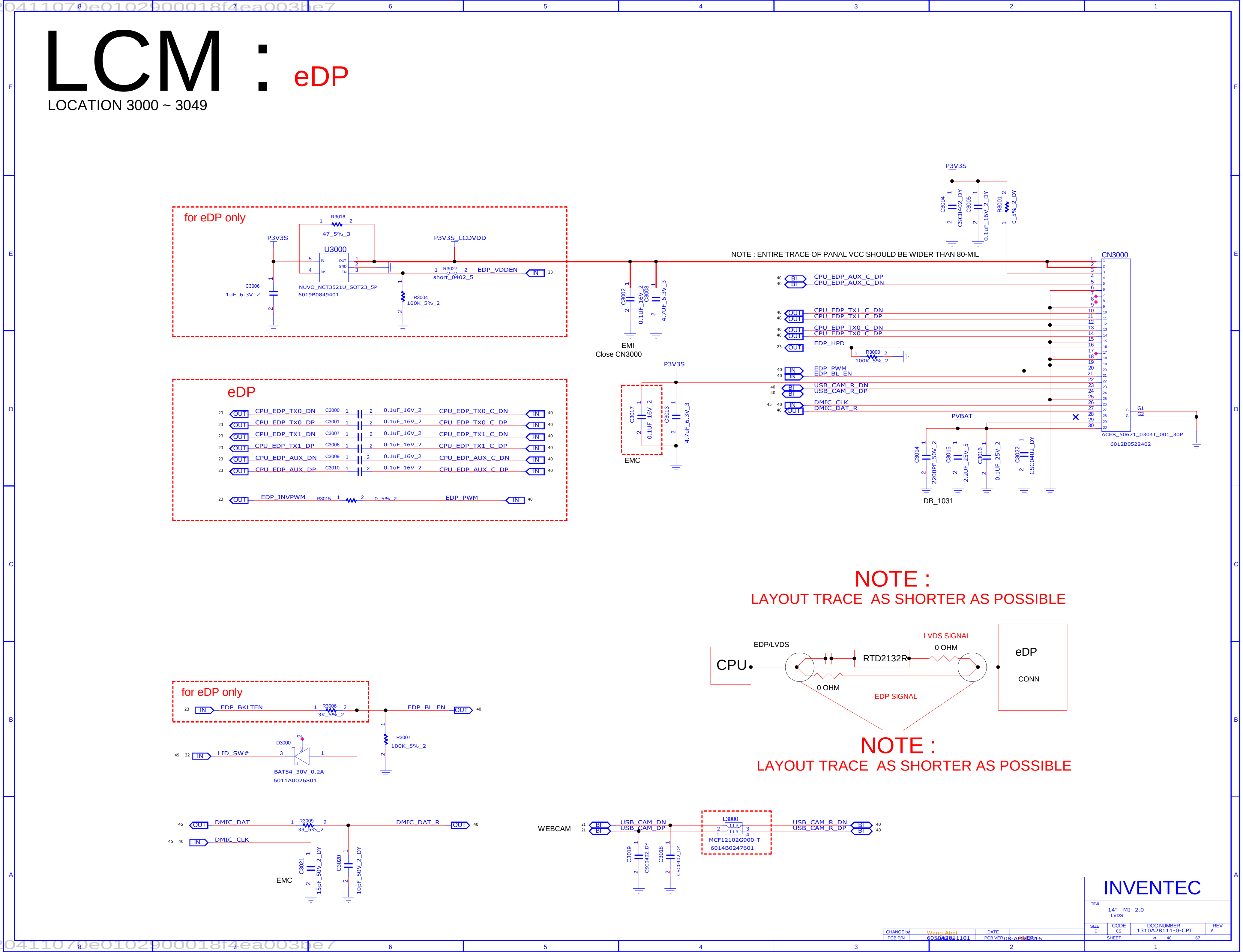
PN:6019B0914201
SMBUS ADDRESS IS "0X50"

INVENTEC

TITLE	14" MI 2.0 Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET 39 of 67			

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

07e20411070e0102900018f4ea003be7



LCM : eDP
LOCATION 3000 ~ 3049
for eDP only
P3V3S
R3016
47_5%_3
U3000
NUVO_NCT3521U_SOT23_5P
6019B0849401
C3006
1uF_6.3V_2
P3V3S_LCDVDD
R3027
short_0402_5
EDP_VDDEN
R3004
100K_5%_2
NOTE : ENTIRE TRACE OF PANAL VCC SHOULD BE WIDER THAN 80-MIL
C3002
0.1UF_16V_2
C3003
4.7UF_6.3V_3
EMI
Close CN3000
C3004
CSC0402_DY
C3005
0.1UF_16V_2_DY
R3001
0_5%_2_DY
CN3000
CPU_EDP_AUX_C_DP
CPU_EDP_AUX_C_DN
CPU_EDP_TX1_C_DN
CPU_EDP_TX1_C_DP
CPU_EDP_TX0_C_DN
CPU_EDP_TX0_C_DP
EDP_HPD
R3000
100K_5%_2
EDP_PWM
EDP_BL_EN
USB_CAM_R_DN
USB_CAM_R_DP
DMIC_CLK
DMIC_DAT_R
ACES_50671_0304T_001_30P
6012B0522402
PVBAT
C3014
2200PF_50V_2
C3015
2.2UF_25V_5
C3016
0.1UF_25V_2
C3022
CSC0402_DY
DB_1031
eDP
CPU_EDP_TX0_DN
CPU_EDP_TX0_DP
CPU_EDP_TX1_DN
CPU_EDP_TX1_DP
CPU_EDP_AUX_DN
CPU_EDP_AUX_DP
C3000
C3001
C3007
C3008
C3009
C3010
0.1uF_16V_2
EDP_INVPWM
R3015
0_5%_2
C3017
0.1UF_16V_2
C3013
4.7uF_6.3V_3
EMC
NOTE :
LAYOUT TRACE AS SHORTER AS POSSIBLE
CPU
EDP/LVDS
RTD2132R
0 OHM
LVDS SIGNAL
EDP SIGNAL
eDP
CONN
NOTE :
LAYOUT TRACE AS SHORTER AS POSSIBLE
for eDP only
EDP_BKLTEN
R3006
3K_5%_2
EDP_BL_EN
R3007
100K_5%_2
LID_SW#
D3000
BAT54_30V_0.2A
6011A0026801
DMIC_DAT
R3009
33_5%_2
DMIC_DAT_R
DMIC_CLK
C3021
15pF_50V_2_DY
C3020
10pF_50V_2_DY
EMC
WEBCAM
USB_CAM_DN
USB_CAM_DP
C3019
CSC0402_DY
C3018
CSC0402_DY
L3000
MCF12102G900-T
6014B0247601
USB_CAM_R_DN
USB_CAM_R_DP
INVENTEC
TITLE
14" MI 2.0
LVDS
SIZE C
CODE CS
DOC.NUMBER 1310A28111-0-CPT
REV A
SHEET 40 of 67
CHANGE by Wang.Abel
DATE

07e20411070e0102900018f4ea003be7

Commerical &Consumer module co-lay

FINGER PRINTER

VFS495 Commerical FPR

VFS495 Commerical FPR

P3V3S

C2200 10uF_6.3V_3

CN2200 6012B0245911-003 ENTERY_6916K_Q06M_00L_6P

Close to CN2200

AMC_AZ5125_01H_SOD523_2P 6011B0131701

P3V3A

SPI_TPM_VCC

SHORT_0402_15

1002 MODIFY

U3500 6019B1702601

INFINEON_SLB9670VQ2_0_FW_7_63_VQFN_32P

FW 7.60

CHANGE by	<ENG> Abel
PCB P/N	6050A2811101
DATE	08-APR-2016
PCB VER	<VER>

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 41 of 67

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

USB3.0

LOCATION 2400~2499
VER.01_20120807

C2418 0.1uF_16V_2
C2419 0.1uF_16V_2
C2420 0.1uF_16V_2
C2421 0.1uF_16V_2
EMI
DGND_CHASSIS2

2.5A for USB3.0 x2

P5V0A
P5V0A_USB3
U2400
GM G524B1T11U_SOT23_5P
USBPWR_EN
C2410 1UF_6.3V_2
C2409 22uF_6.3V_5_DY
C2408 22uF_6.3V_5_DY

USB Charger
P5V0A_USB3_2
R2439 0.01_1%_5
6013B0467701
R2440 0.01_1%_5_DY
P5V0A_USB3
C2401 0.1uF_16V_2
C2400 22uF_6.3V_5
C2416 22uF_6.3V_5_DY

Charger port
L2404 MCF12102G900-T
6014B0247601
USB_L1_IC_DN
USB_L1_IC_DP
USB3_L1_RX_DN
USB3_L1_RX_DP
USB3_L1_TX_DN
USB3_L1_TX_DP
C2406 0.1UF_16V_2
C2404 0.1UF_16V_2
R2400 short_0402_5_nsp
R2403 short_0402_5_nsp
R2405 short_0402_5_nsp
R2404 short_0402_5_nsp
USB3_P1_TX_C_DN
USB3_P1_TX_C_DP
USB_P2_L_DN
USB_P2_L_DP
USB3_P1_RX_L_DN
USB3_P1_RX_L_DP
USB3_P1_TX_L_DN
USB3_P1_TX_L_DP
CN2400
SINGA_2UB4055_100101F_9P
6012B0612601
DGND_CHASSIS2
D2400 AMC_AZC099_04S_R7G_SOT23_6P
D2401 AMAZING_AZ1045_04F_R7G_10P
P5V0A_USB3
C2403 0.1uF_16V_2
C2402 22uF_6.3V_5
C2417 22uF_6.3V_5_DY

L2405 MCF12102G900-T
6014B0247601
USB_L2_DN
USB_L2_DP
USB3_L2_RX_DN
USB3_L2_RX_DP
USB3_L2_TX_DN
USB3_L2_TX_DP
C2407 0.1UF_16V_2
C2405 0.1UF_16V_2
R2410 short_0402_5_nsp
R2409 short_0402_5_nsp
R2408 short_0402_5_nsp
R2411 short_0402_5_nsp
USB3_P2_TX_C_DN
USB3_P2_TX_C_DP
USB_P1_L_DN
USB_P1_L_DP
USB3_P2_RX_L_DN
USB3_P2_RX_L_DP
USB3_P2_TX_L_DN
USB3_P2_TX_L_DP
CN2402
SINGA_2UB4055_100101F_9P
DGND_CHASSIS2
D2402 AMAZING_AZ1045_04F_R7G_10P

CN2402 BOM : 6012B0678501 (USB2.0)

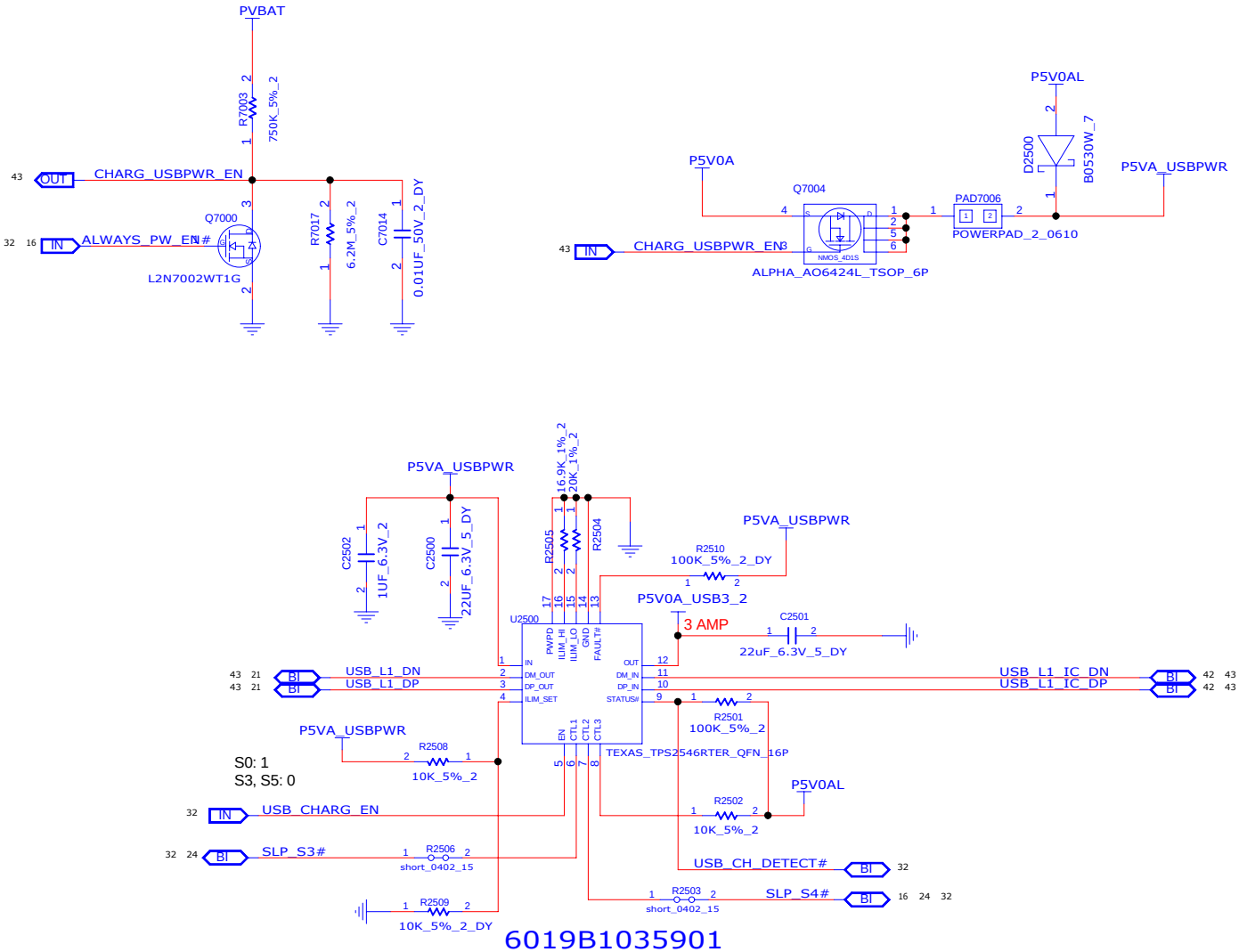
INVENTEC

TITLE	14" MI 2.0 USB 3.0 CONN & M/B TO D/B CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET	of 42	67	

CHANGE by	Wang,Abel	DATE	
PCB P/N	6013A2811101	PCB VER	A

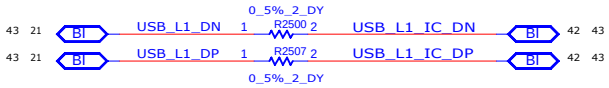
07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7



6019B1035901

USB CHARGING TPS2546



BOM CHANGE TO STC2540

6019B1124601

CHANGE by	Wang,Abel	DATE	
PCB P/N	6019B2811101	PCB VER	A00

08-APR-2016

INVENTEC

TITLE: 14" MI 2.0 USB 3.0 CONN & M/B TO D/B CONN

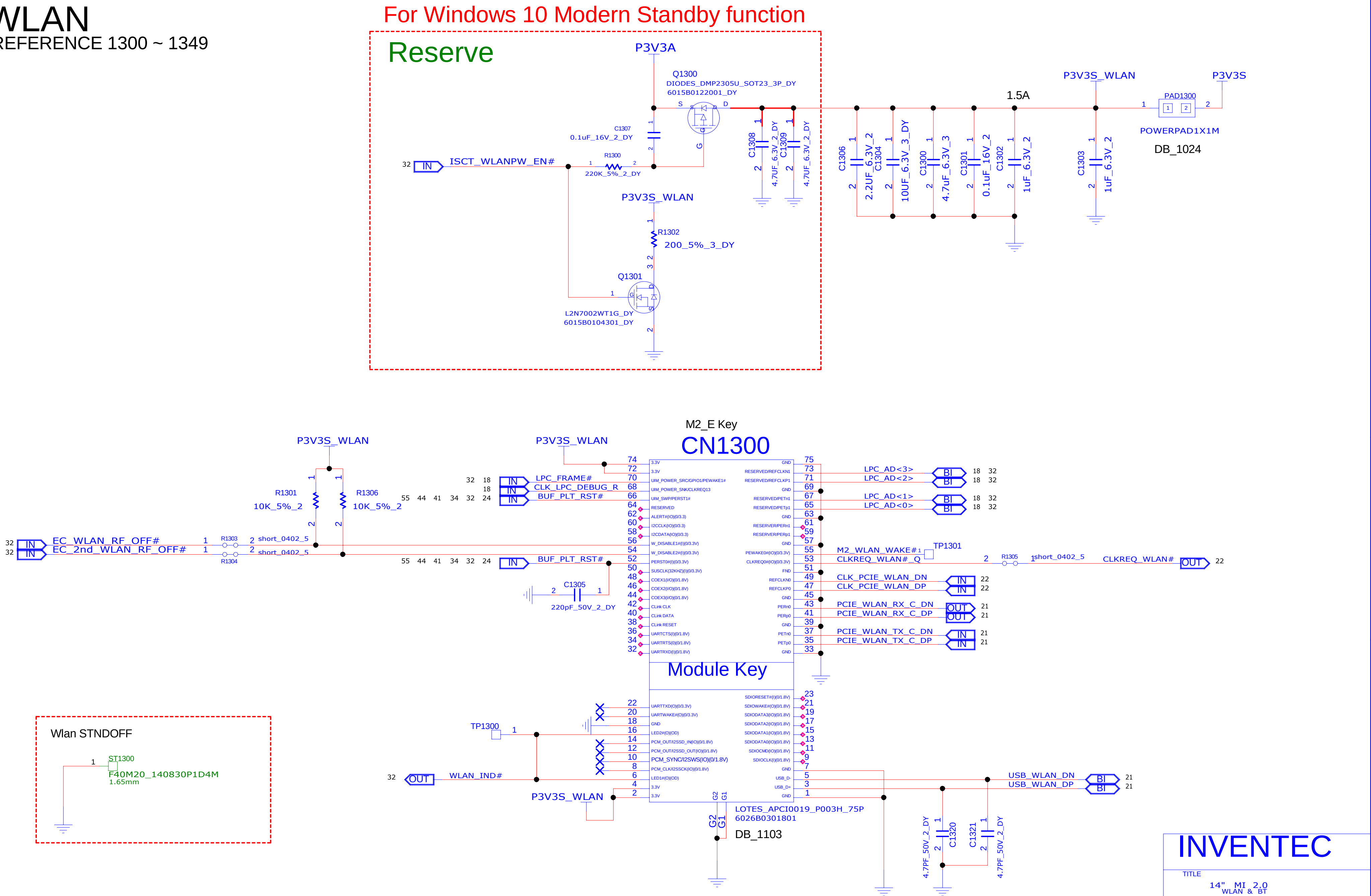
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET of 43 67

07e20411070e0102900018f4ea003be7

WLAN

REFERENCE 1300 ~ 1349



INVENTEC

TITLE: 14" MI 2.0 WLAN & BT

SIZE	CODE	DOC.NUMBER	REV
3	CS	1310A28111-0-CPT	A

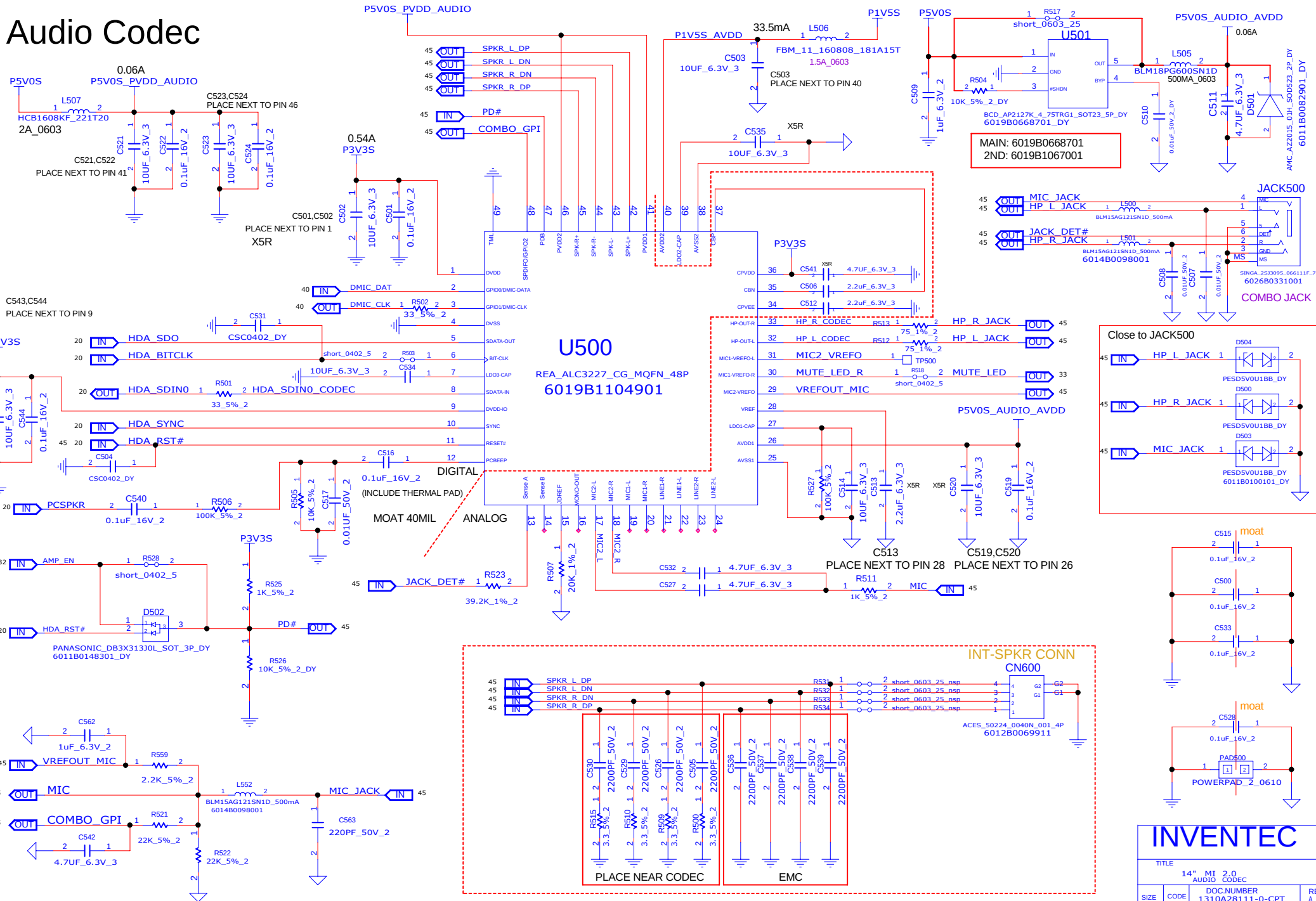
SHEET 44 of 67

CHANGE by: Wang.Abel — DATE: 06-APR-2016

PCB P/N: 6050A2811101 — PCB VER

07e20411070e0102900018f4ea003be7

Audio Codec



07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

LAN (Controller)

Location 400 ~ 469
Ver.03_210120807

Co-Layout

6019B1277901	RTL8166EH-CG	10/100
★6019B1264001	RTL8111HSH-CGT	10/100/1000

P1V0_LAN_REG

L400
TAITECH_SWF2520CF-2R2M-R15
6014B0200401

Switch MODE(RTL8111HSH-CG)
L400,C414,C415 mount

LDO MODE(RTL8166EH-CG)
L400,C414,C415 OPEN

L400
1ST : 6014B0200401
2ND : 6014B0190301

C421 10uF_6.3V_3
C414 4.7uF_6.3V_3
C415 0.1uF_16V_2

P1V0_LAN

Close to LAN chip

Pin3 C400 0.1uF_16V_2
Pin8 C406 0.1uF_16V_2
Pin30 C408 0.1uF_16V_2 — FOR RTL8111HSH
Pin30 C412 1uF_6.3V_2_DY
Pin30 C420 0.1uF_16V_2_DY — FOR RTL8166EH
Pin 22 C407 0.1uF_16V_2
Pin 22 C413 1uF_6.3V_2
Pin 22 C424 0.1uF_16V_2 — FOR RTL8111HSH

P3V3A

32 IN WOL_PWEN# 1 R406 2 220K_5%_2

Q400 DIODES_DMP2305U_SOT23_3P 6015B0122001
G S D
C411 0.1UF_16V_2

Q400
1st : 6015B0122001
2nd: 6015B0122901

P3V3A_LAN Rising time (10%~90%)要>1mS and <100mS

P3V3A_LAN
0.5A
Pin11 C404 0.1uF_16V_2 — FOR RTL8111
Pin32 C418 4.7uF_6.3V_3
C405 0.1UF_16V_2
C419 4.7uF_6.3V_3 — FOR RTL8111

R407 short_0603_25_nsp

P3V3_LAN_REG
C416 4.7uF_6.3V_3 — FOR RTL8111
C417 0.1UF_16V_2

P1V0_LAN
R401 2.49K_1%_2

XTAL25LAN2 IN 46
XTAL25LAN1 IN 46
LED_LANRXACT# TP9000 OUT 47
GPO TP9001
LED_LANLINK# OUT 47 TP9002

P3V3A_LAN

32 AVDD33
31 RSET
30 AVDD10
29 CKXTAL2
28 CKXTAL1
27 LED0
26 LED1/GPO
25 LED2(LED1)

33 GND

U400
REA_RTL8111HSH_CG_QFN_32P

47 BI LAN_TRD0_DP 1 MDIP0
47 BI LAN_TRD0_DN 2 MDIN0
3 AVDD10(NC)
47 BI LAN_TRD1_DP 4 MDIP1
47 BI LAN_TRD1_DN 5 MDIN1
47 BI LAN_TRD2_DP 6 MDIP2(NC)
47 BI LAN_TRD2_DN 7 MDIN2(NC)
8 AVDD10

P1V0_LAN

REGOUT(NC) 24
VDDREG(DVDD33) 23
DVDD10(NC) 22
LANWAKEB 21
ISOLATEB 20
PERSTB 19 PLT_RST#_R
HSON 18 PCIE_LAN_RX_DN
HSOP 17 PCIE_LAN_RX_DP

P1V0_LAN_REG P3V3_LAN_REG P1V0_LAN P3V3A_LAN

P3V3S
R404 1K_5%_2
R403 15K_5%_2

R409 10K_5%_2_DY

PCH_PCIE_WAKE# OUT 24
PLT_RST# IN 24
PCIE_LAN_RX_C_DN OUT 21
PCIE_LAN_RX_C_DP OUT 21

R402 short_0402_15_nsp
C402 0.1UF_16V_2
C403 0.1UF_16V_2

PLACE CLOSE TO PIN 17,18

C401 CSC0402_DY

9 MDIP3(NC)
10 MDIN3(NC)
11 AVDD33(NC)
12 CLKREQB
13 HSIP
14 HSIN
15 REFCLK_P
16 REFCLK_N

47 BI LAN_TRD3_DP
47 BI LAN_TRD3_DN

P3V3A_LAN

22 OUT CLKREQ_LAN# 1 R400 2 CLKREQ_LAN#_R
short_0402_15_nsp

P3V3S
R408 10K_5%_2

21 IN PCIE_LAN_TX_C_DP
21 IN PCIE_LAN_TX_C_DN
22 IN CLK_PCIE_LAN_DP
22 IN CLK_PCIE_LAN_DN

46 OUT XTAL25LAN2 R405 1K_5%_2
46 OUT XTAL25LAN1

X400 25MHz_10pF 6018B0054701

C409 15PF_50V_2
C410 15PF_50V_2

	RTL8166EH-CG	RTL8111HSH-CGT
C404	X	V
C418	X	V
C405	V	V
C419	X	V
C416	X	V
C417	V	V
C420(Pin30)	V	X
L400	X	V
C414	X	V
C415	X	V
C400(Pin3)	X	V
C406(Pin8)	V	V
C408(Pin30)	V	V
C424(Pin22)	X	V
C407(Pin22)	X	V
C413(Pin22)	X	V
C412(Pin30)	V	X
U470 6016B0000201	X	V
U471 6016B0008101	V	X

BOM Change

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

CHANGE by	<ENG>	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>

SIZE A3 | CODE CS | DOC.NUMBER 1310A28111-0-CPT | REV A

SHEET 46 of 67

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

LAN (Transformer & RJ45)

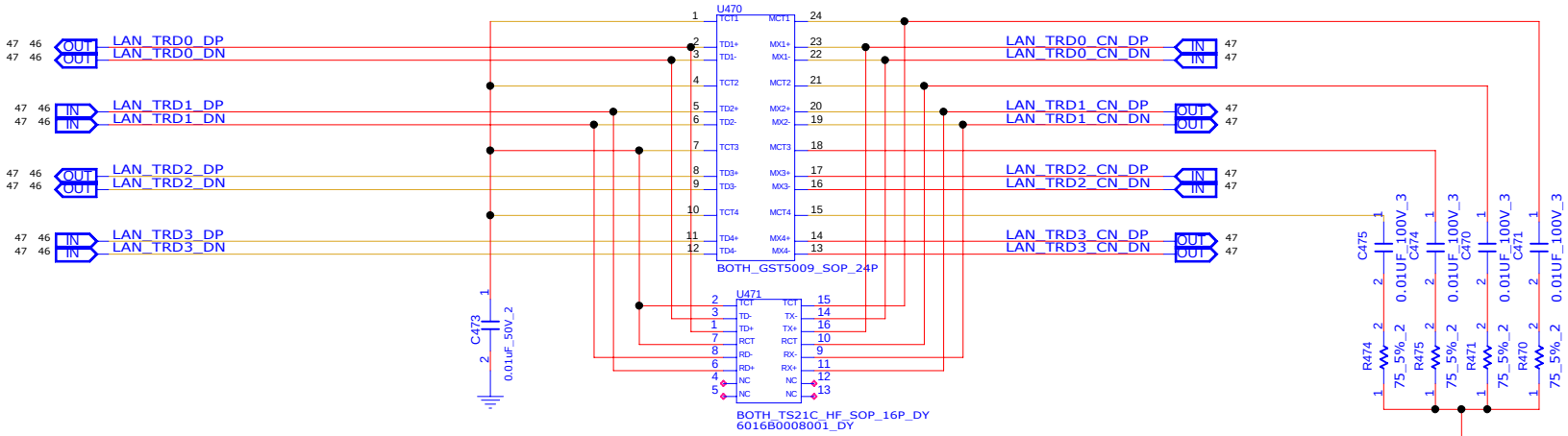
Location 470 ~ 499

Ver.01_20120801

FOR 10/100/1000 LAN

10/100/1000 MAIN===> Bothhand P/N : 6016B0000201 GST5009

10/100/1000 2ND ===>Lankom P/N : 6016B0019701 L22N001-1

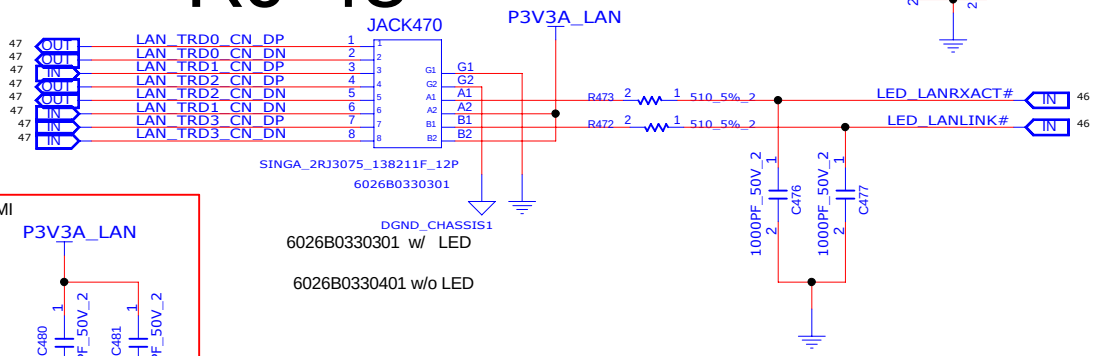


For 10/100 LAN

10/100 Main===> 6016B0008001

10/100 2nd ===> 6016B0011801

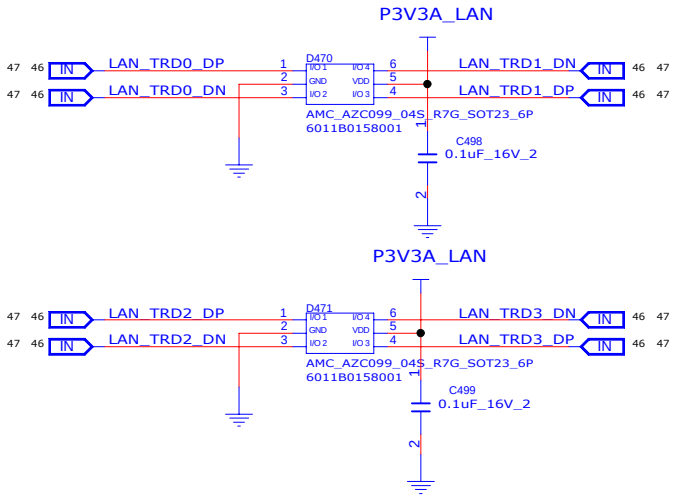
RJ-45



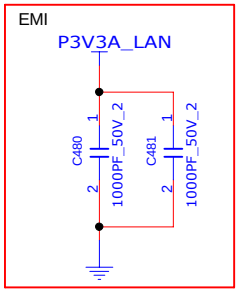
6026B0330301 w/ LED

6026B0330401 w/o LED

Close to U470/U471 input side.



EMI



CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 47 of 67

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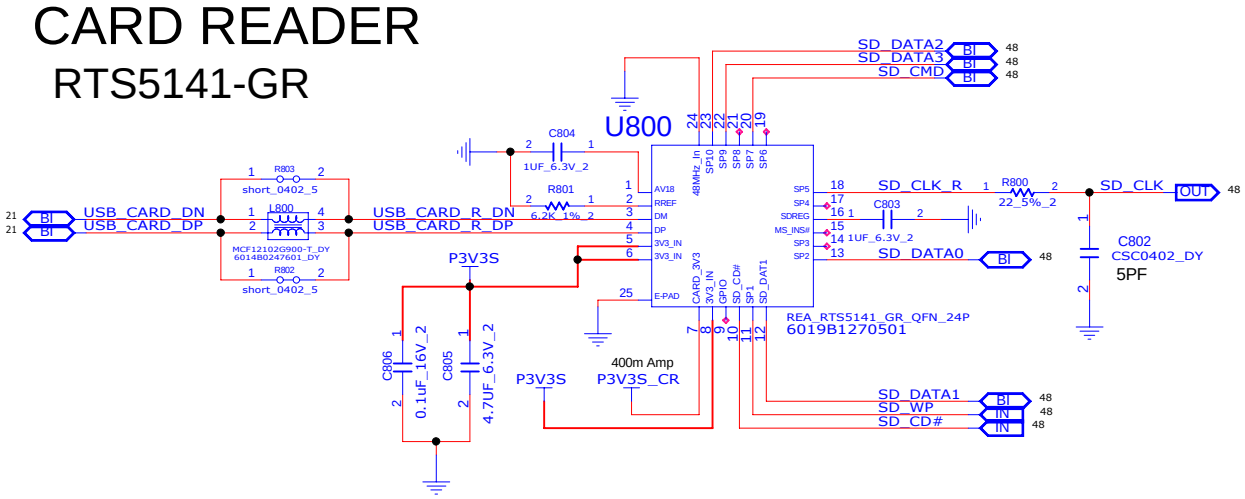
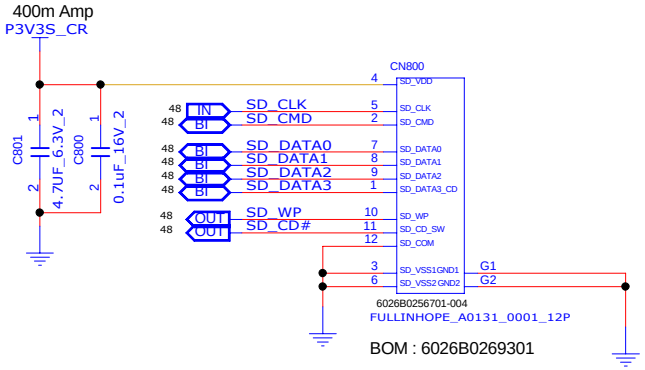
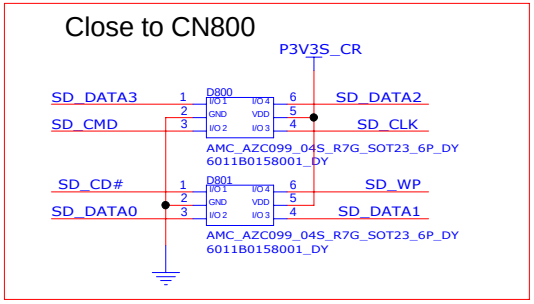
07e20411070e0102900018f4ea003be7

CARD READER

RTS5141-GR







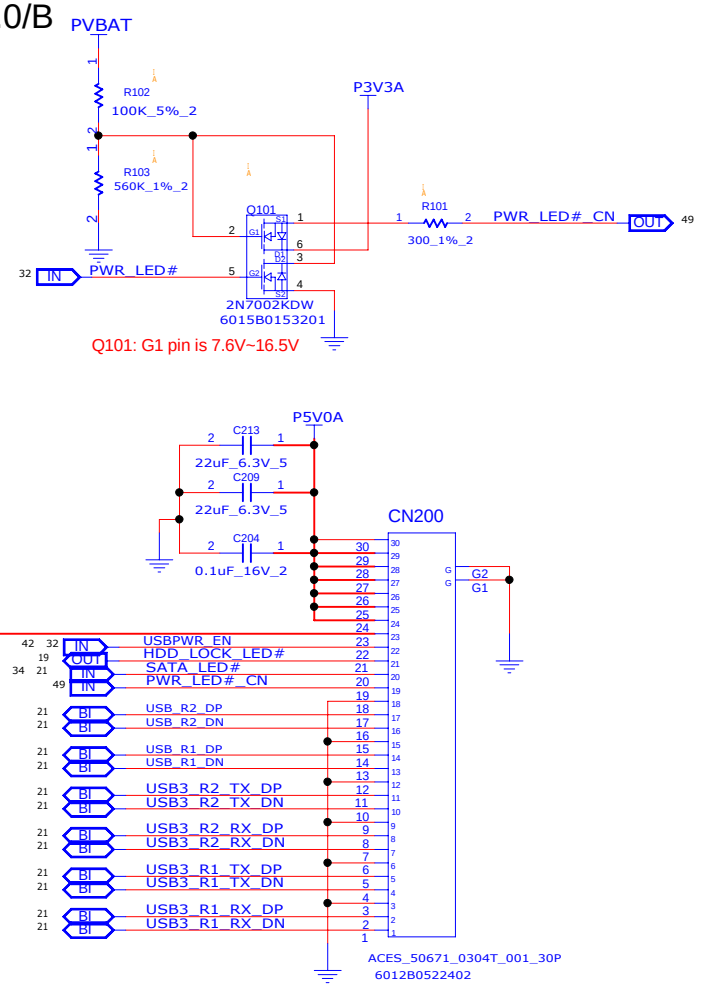
INVENTEC

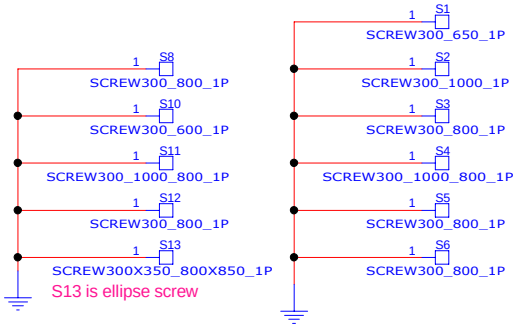
TITLE	14" MI 2.0 CRT CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by	<ENG>Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	<VER>
SHEET 48 of 67			

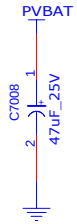
07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

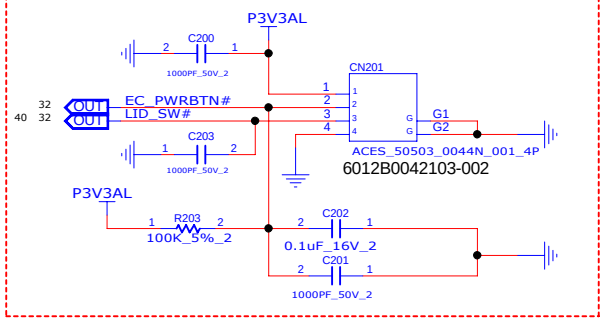
To USB3.0/B



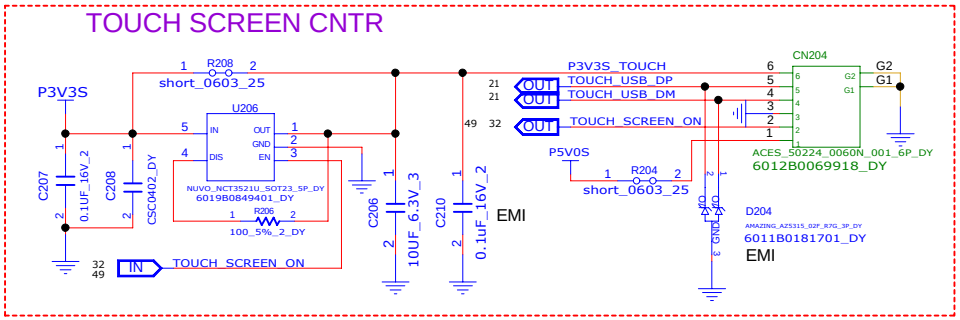




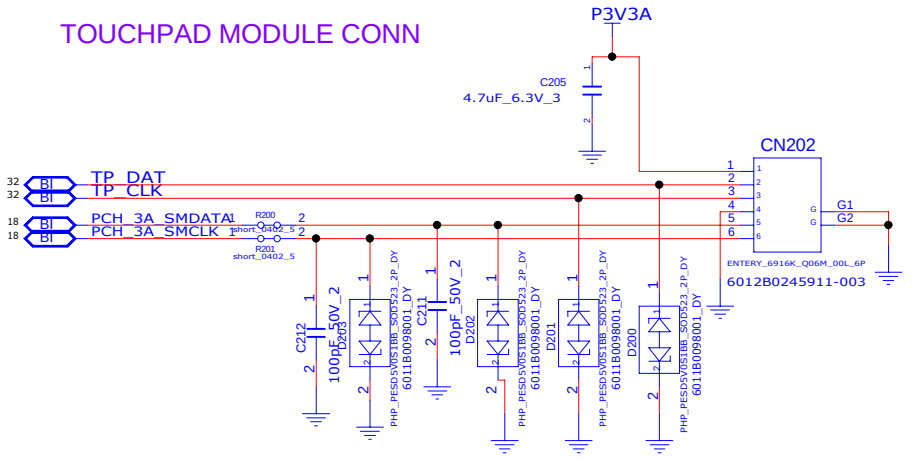
POWER BUTTON CONN ON MB



TOUCH SCREEN CNTR



TOUCHPAD MODULE CONN



FIX3 FIX_MASK FIX4 FIX_MASK FIX1 FIX_MASK FIX2 FIX_MASK
FIX7 FIX_MASK FIX8 FIX_MASK FIX5 FIX_MASK FIX6 FIX_MASK

INVENTEC

TITLE	14" MI 2.0 POWER BUTTON		
SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
CHANGE by Wang.Abel	DATE		
PCB P/N 6050A2811101	PCB VER	SHEET 49 of 67	

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

NVIDIA N16

DATE	CHANGE NO.	REV
08-APR-2016		
08-APR-2016	2013-ECO-002392	A

DESIGN / DRAWER	Chan, Shane / Wang.Abel	DATE	08-APR-2016
CHECK	Huang, Vens		
APPROVAL			A01
FILE NAME			
PCB P/N	6050A2811101 <FNO>	PCB VER	A01

INVENTEC

TITLE	14" MI 2.0		
SIZE 3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A

07e20411070e0102900018f4ea003be7

07e20411070e0102900018f4ea003be7

VMAX=1.2V BY PWM D=100%
VMIN=0.6V PWM D=0%
VBOOT=0.875~0.9V BY PWM TRISTATE
VSTB=0.3V BY EXT MOS INPUT
FPWM=1.125MHZ
PWM PULSE MIN.=9.26NS
VID TRANS. TIME=90US

MAX=26A
OCP=55A

PVBAT
VRB_VDD5
VRPVBAT_DGPU
VRPVCORE_DGPU_PH1
VRPVCORE_DGPU_HG1
VRPVCORE_DGPU_LG1
VRPVCORE_DGPU_BST1
PVCORE_DGPU
DGPU_PG
EN_DGPU
DGPU_PSI
DGPU_PWMVID
GPU_VSS_SENSE
GPU_VCC_SENSE
GPU_SENSE
RGND
U6750
RICHTEK_RT8812AGQW_QFN_20P
Q6750
Q6751
TOSHIBA_TPH8R903NL
TOSHIBA_TPCA8A10_H
L6750
PCMC104T_R36MN
PAD6760 POWERPAD_2_0610
PAD6750 POWERPAD_2_0610
PAD6751 POWERPAD_2_0610

CHANGE by	Wang.Abel
PCB P/N	6050A2811101
DATE	08-APR-2016
PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 51 of 67

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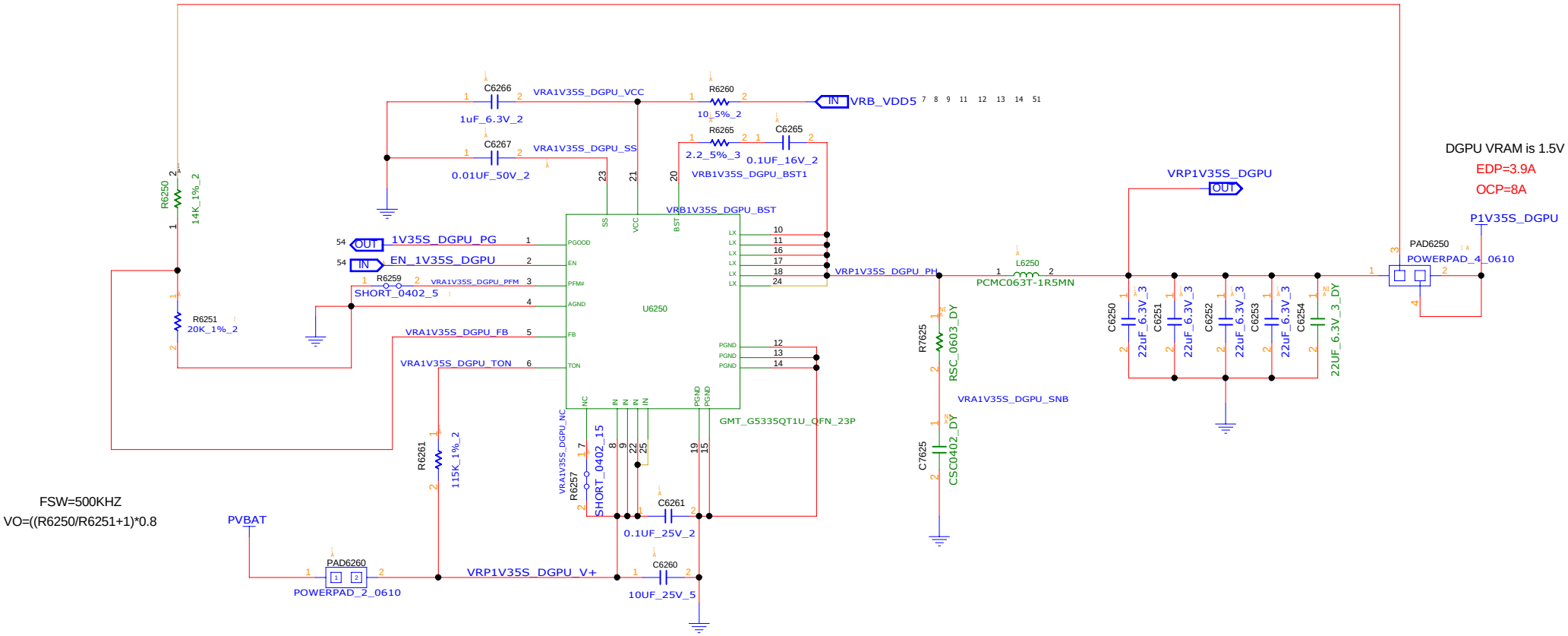
07e20411070e0102900018f4ea003be7



CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 52 of 67

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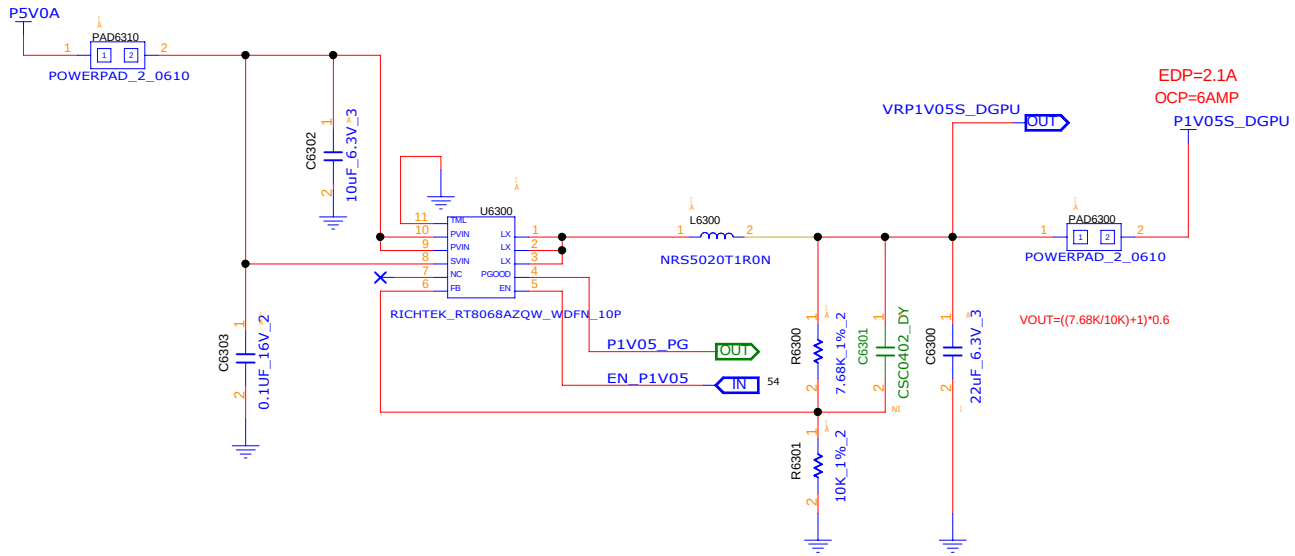

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 53 of 67

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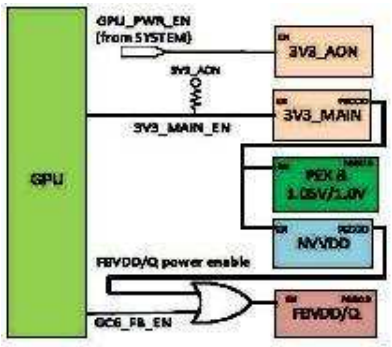

Figure 18-8. GC6 2.0 Voltage Regulator Complex Signal Connection

- Cold boot/Options: 3V3_AON & 3V3_MAIN → NVVDD → PEX_VDD → FBVDD/Q
- GC6 2.0 Exit: 3.3V_MAIN → NVVDD → PEX_VDD

FOR GC6 2.0 FUNCTION
CONTROL BY PCH

R7465
NA --> ENABLE GC62.0
MOUNT -->DISABLE GC62.0

FOR GC6 2.0

SI_BUILD

CHANGE by	Wang,Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

INVENTEC

TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310A28111-0-CPT	A

SHEET 54 of 67

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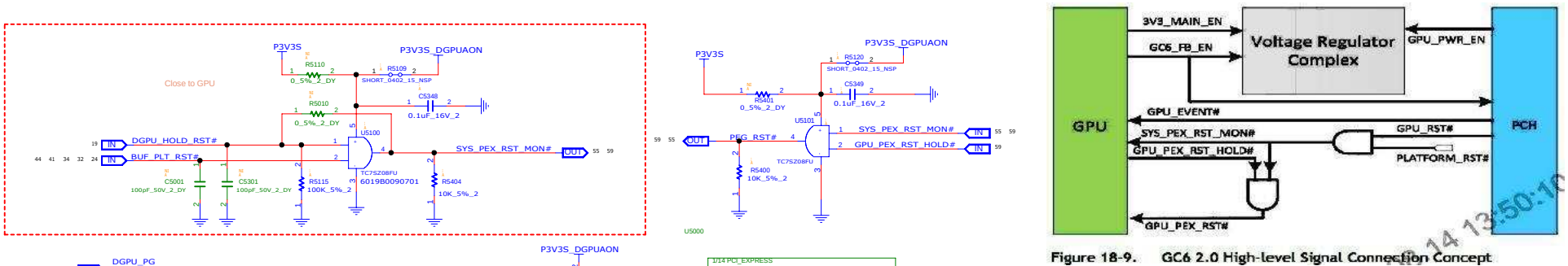


Figure 18-9. GC6 2.0 High-level Signal Connection Concept

Feb 14 13:50:19

NVIDIA
N16S-GTR-S
(HP PN: NA)
6019B1409001

BOM change

CHANGE SI	Wang Abel	DATE	08-APR-2016	
PCB P/N	6050A2811101	PCB VER	A01	

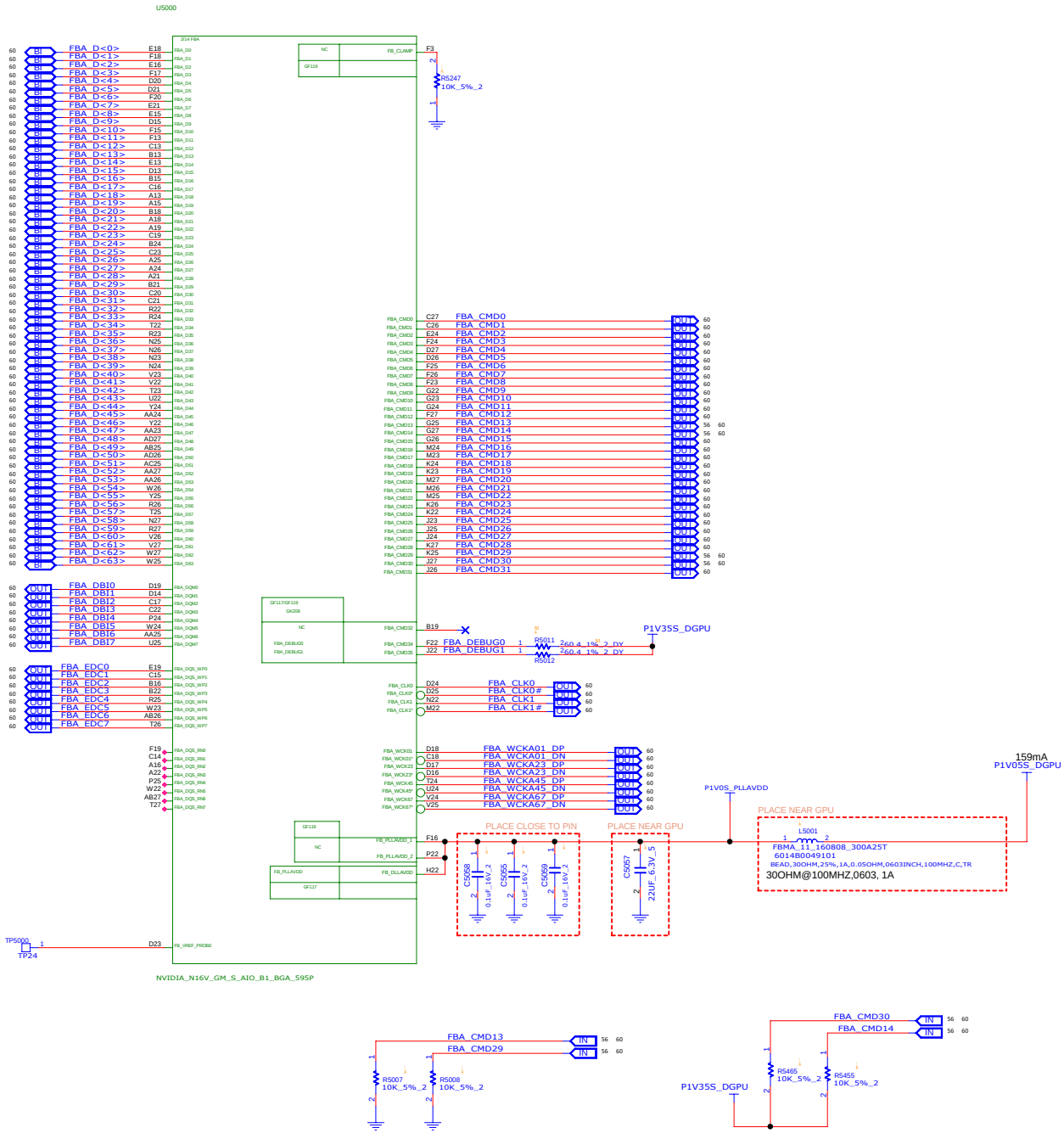
INVENTEC

14" MI 2.0
GPU-1

SIZE	CODE	DOC NUMBER	REV
C	CS	1310A28111-0-CPT	A

SHEET 55 of 67

07e2041107de0102000018f4ea003be7



N14x DDR3 mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6

NVIDIA Confidential 2012.07.1

INVENTEC

14" MI 2.0
GPU-2

SIZE	CODE	DOC NUMBER	REV
C	CS	1310A2811-0-CPT	A

SHEET 56 of 67

CHANGE NO		DATE	08-APR-2016
PCB P/N	60NA02811101	PCB VER	A01

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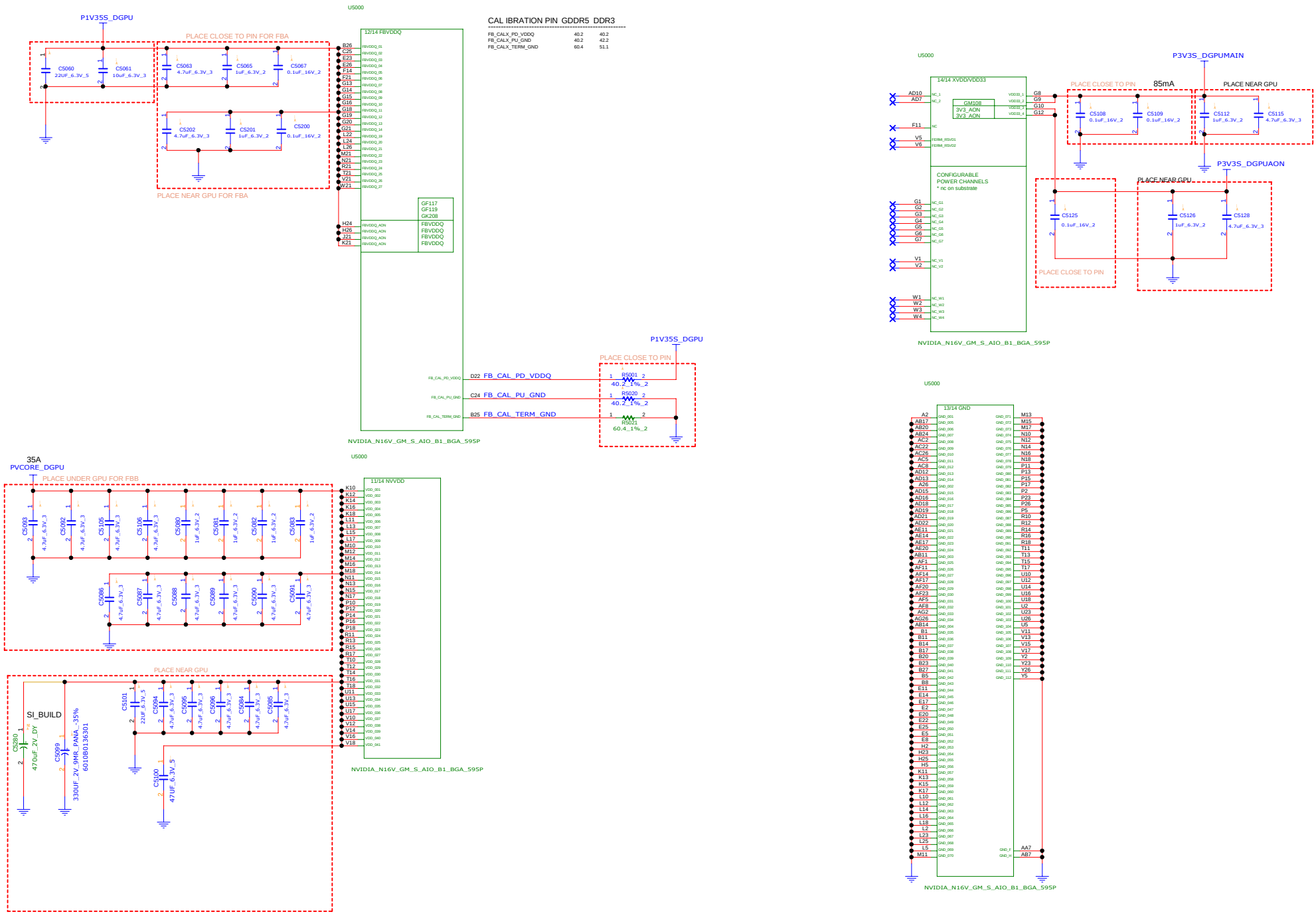


CHANGE SE	Wang Abel	DATE	08-APR-2016	
PCB P/N	6J0JA2811101	PCB VER	A01	

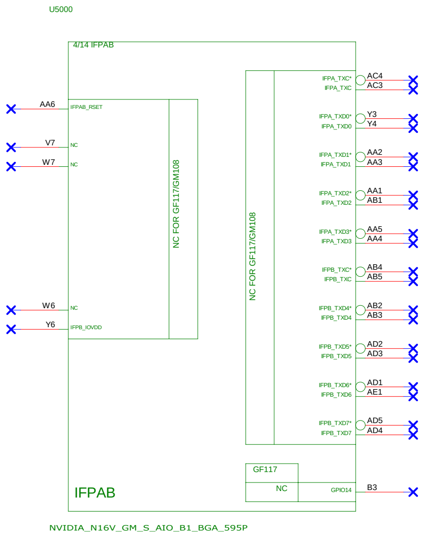
INVENTEC

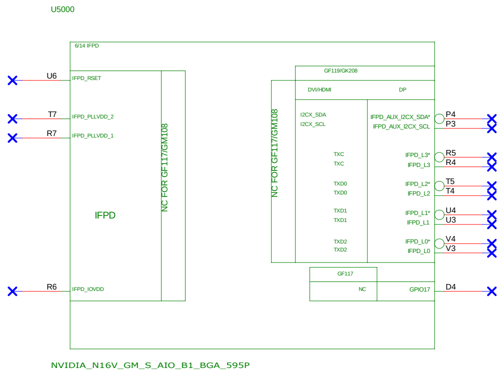
TITLE: 14" MI 2.0 GPU-3

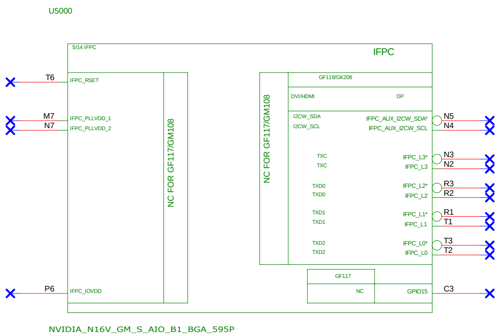
SIZE	CODE	DOC NUMBER	REV
C	CS	1310A2811-0-CPT	A

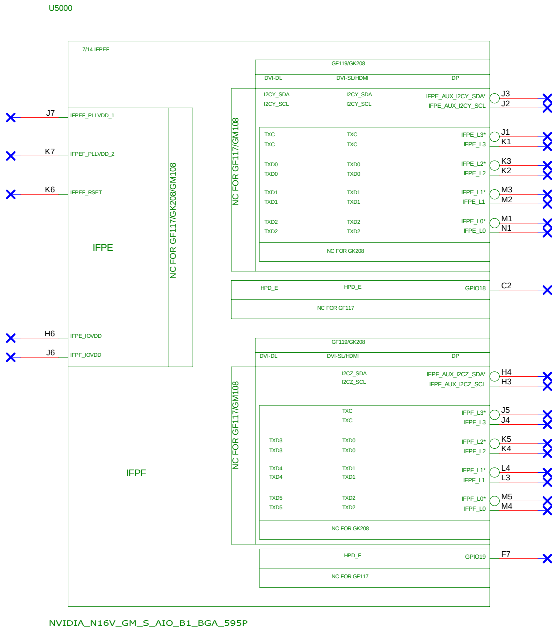
SHEET 52 of 67

07e2041107de0102000018f4ea003be7









4 PCS

STRAP FOR 1.5V   SINGLE RANK STUFFING FOR DUAL RANK

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	PU R5056	PD R5061
SAMSUNG	256MX16	K4W4G1646E-BC1A	6019B1275901	0X4	NI	24.9K
Hynix	256MX16	H5TC4G63EFR-N0C	6019B1536801	0X9	10.0K	NI
MICRON	256MX16	MT41J256M16LY-091G:N	6019B1402201	0X3	NI	20.0K

8PCS

STRAP FOR 1.5V   DUAL RANK

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	PU R5056	PD R5061
SAMSUNG	256MX16	K4W4G1646E-BC1A	6019B1275901	0xD	30.1k ohm	NI
Hynix	256MX16	H5TC4G63EFR-N0C	6019B1536801	0x0	NI	4.99k ohm
MICRON	256MX16	MT41J256M16LY-091G:N	6019B1402201	0x7	NI	45.3k ohm

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

N16S-GM/-GT/-LP DDR3 AND DDR3L MEMORY RVL

NVIDIA recommends the following DDR3 and DDR3L memories for use in conjunction with notebook designs using N16S-GM/-GT/-LP.

Table 3. N16S-GM/-GT DDR3 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
DDR3	1.5V/ 1.5V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x6	1000	N/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0x7	1000	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x8	1000	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x4	1000	N/A	Post production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0x5	1000	N/A	Post production ready
				Micron	MT41J256M16LY-091G:N	N-die	0x3	1000	N/A	Post-production ready
				Hynix	H5TC4G63EFR-N0C	E-die	0x9	1000	N/A	Post production ready
			Dual Rank	Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xD	1000	N/A	Post production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0xC	1000	N/A	Post production ready
				Micron	MT41J256M16LY-091G:N	N-die	0x7	1000	N/A	Post-production ready
				Hynix	H5TC4G63EFR-N0C	E-die	0x0	1000	N/A	Post production candidate

Note: For N16S-GM/-GT/-LP, the maximum allowable memory case temperature is 85 °C.

AndyTC Hsu NVIDIA Confidential Inventec HP Notebook 2016-11-01 19:47:15

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Table 10. Multi-Level Strap Differences

Physical Strapping Pin	GPU	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	N15S-GV	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
	N15S-GM/-GT	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	All GB2-64 N14 and GB2B-64 N15	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	N15S-GV	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	N15S-GM/-GT	DEVID_SEL	PCIE_CFG		
STRAP0	N15S-GV	USER[3]	USER[2]	USER[1]	USER[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and stuff 50kΩ pull-up)			
STRAP1	N15S-GV	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP2	N15S-GV	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP3	N15S-GV	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			
STRAP4	N15S-GV	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V
	N15S-GM/-GT	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)			

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing 3GIO_PADCFG. This strap only exists in the GB2B-64 and GB4B-128 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific *Platform Update Notification* for the latest configuration.

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the I2CS address of a GPU or the I2CS slave address.

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

15.5.5 VGA_DEVICE Strap

The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set 3D Acceleration Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

Table 15-15. SORx_EXPOSED - Display Link to Usage Bit Mapping

Displays		HDMI/DP	DVI	LVDS	eDP	Not in Use
Standard Mode	IFPAB		SOR0_EXP = 1	SOR0_EXP = 0		SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
Split Mode AB	IFPA	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPB	SOR0_EXP = 1	SOR0_EXP = 1			SOR0_EXP = 0
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPEF					
Split Mode EF	IFPAB					
	IFPC	SOR1_EXP = 1				SOR1_EXP = 0
	IFPD	SOR2_EXP = 1			SOR2_EXP = 0	SOR2_EXP = 0
	IFPE	SOR3_EXP = 1	SOR3_EXP = 1			SOR3_EXP = 0
	IFPF	SOR0_EXP = 1	SOR0_EXP = 1		SOR0_EXP = 0	SOR0_EXP = 0

Note: GB2B-64 package GPUs are configured with no display output so all links are considered Not in Use.

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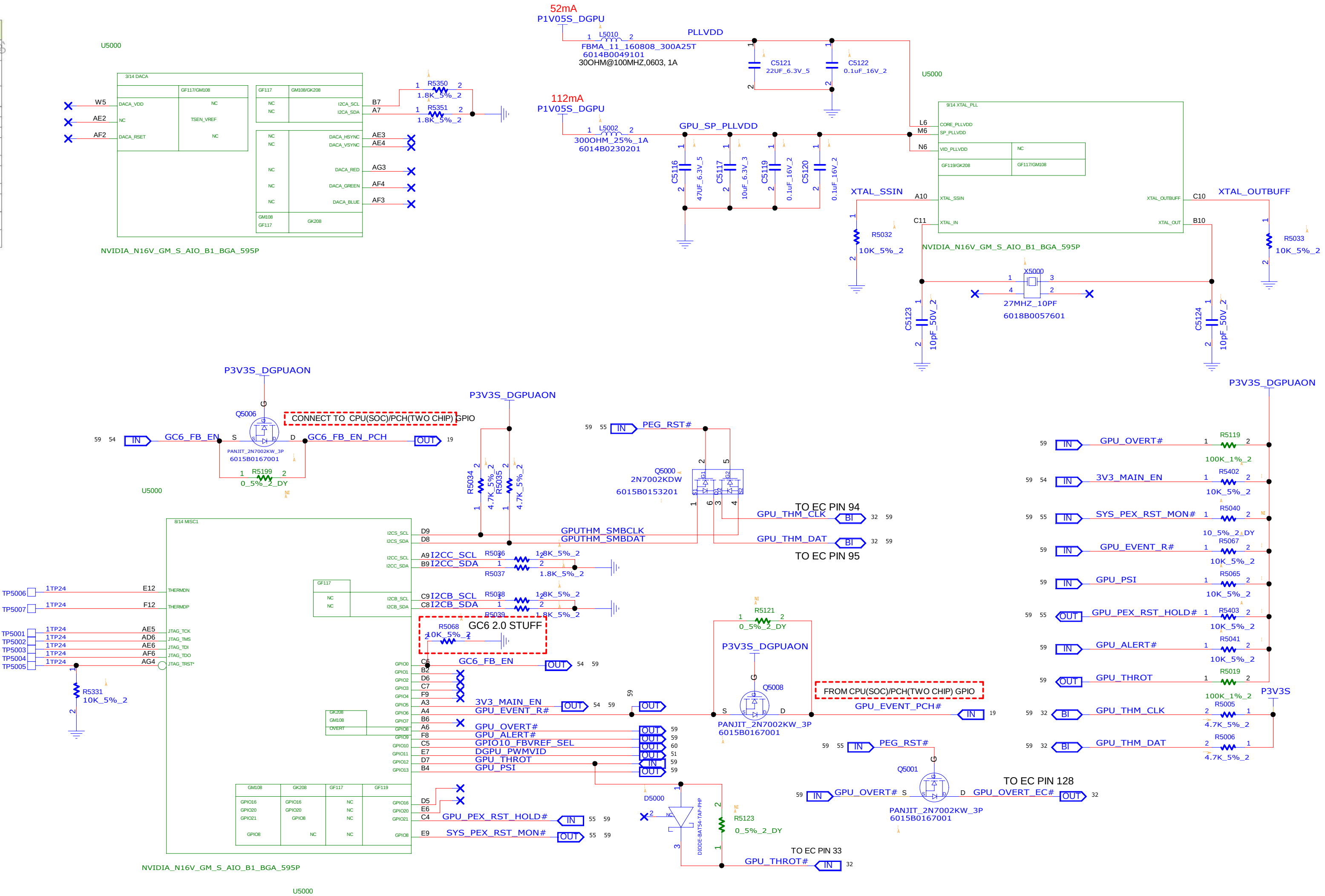

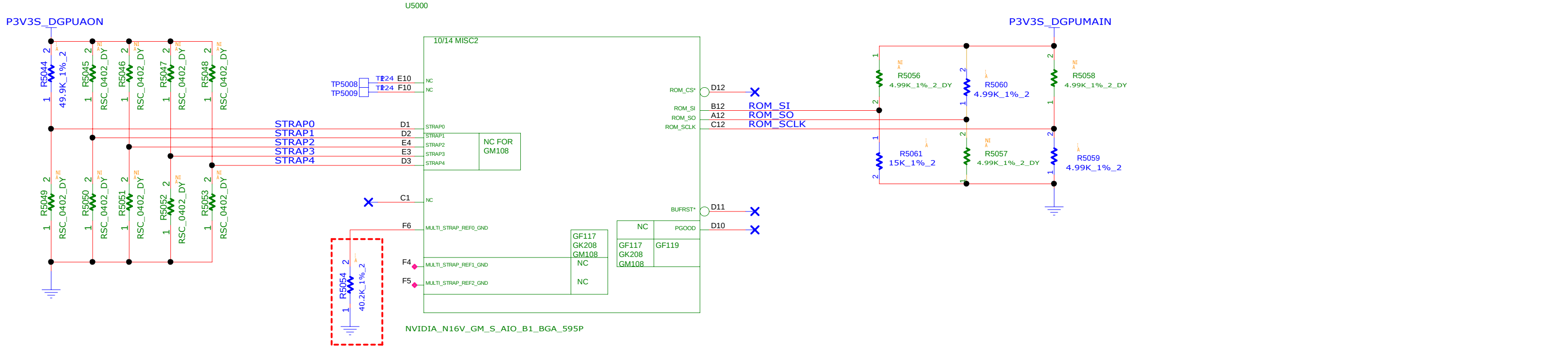

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GDDR5 - 256Mx32/512Mx16, 1.5V 7Gbps / 1.35V 6Gbps	198247	Samsung	900852-971	K4G80325FB-HC28	B	20nm
GDDR5 - 256Mx32/512Mx16, 1.5V 7Gbps / 1.35V 6Gbps	198248	Micron	900852-671	MT51J256M32HF-70:A	A	20nm

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TITLE: 14" MI 2.0 GPU-5

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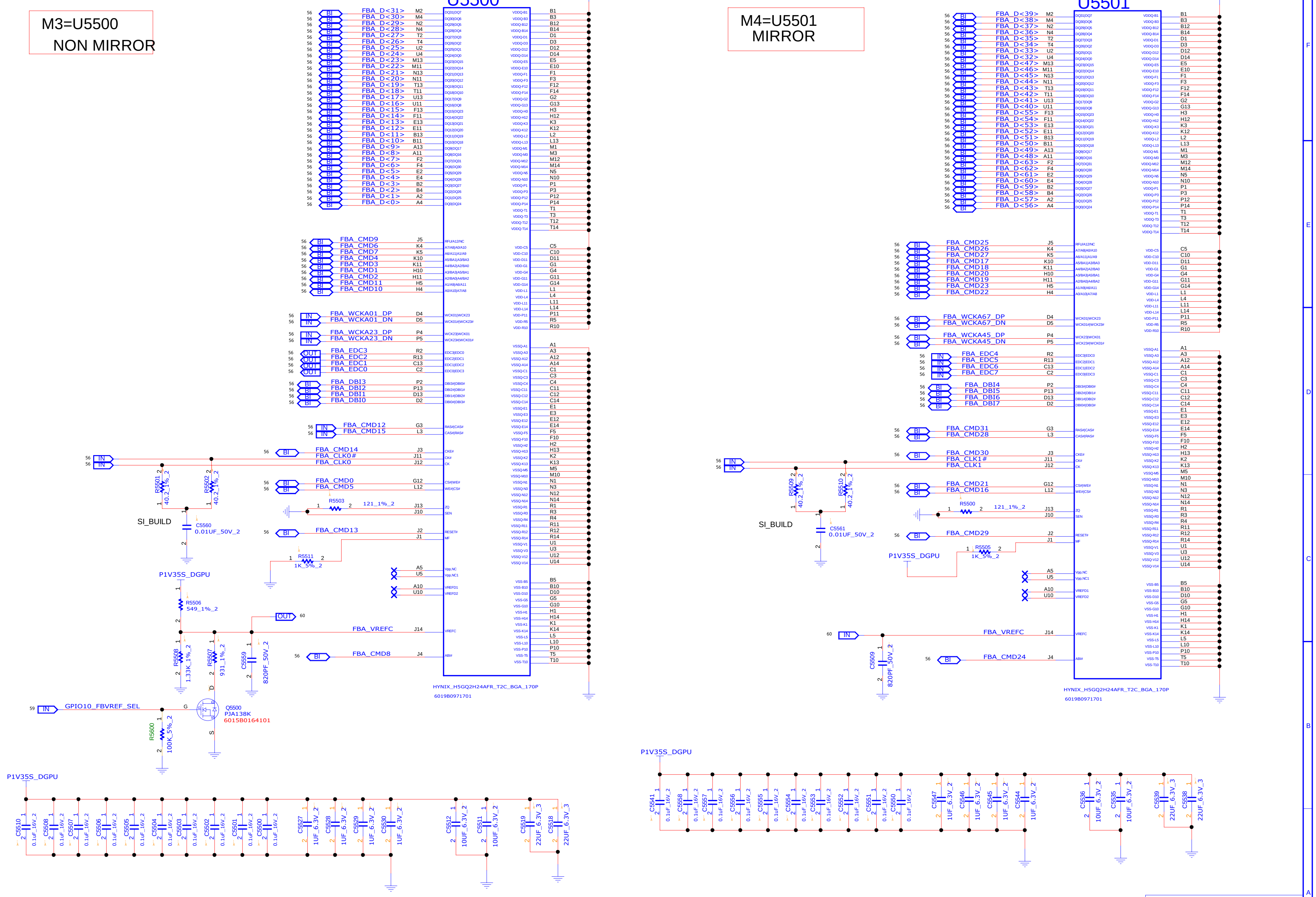
MEMORY: FBA Partition 63..32



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NON MIRROR
U5500
P1V35S_DGPU
M4=U5501
MIRROR
U5501
FBA_D<31> … FBA_D<0>
FBA_D<39> … FBA_D<56>
FBA_CMD9
FBA_CMD6
FBA_CMD7
FBA_CMD4
FBA_CMD3
FBA_CMD1
FBA_CMD2
FBA_CMD11
FBA_CMD10
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD17
FBA_CMD18
FBA_CMD20
FBA_CMD19
FBA_CMD23
FBA_CMD22
FBA_WCKA01_DP
FBA_WCKA01_DN
FBA_WCKA23_DP
FBA_WCKA23_DN
FBA_WCKA67_DP
FBA_WCKA67_DN
FBA_WCKA45_DP
FBA_WCKA45_DN
FBA_EDC3
FBA_EDC2
FBA_EDC1
FBA_EDC0
FBA_EDC4
FBA_EDC5
FBA_EDC6
FBA_EDC7
FBA_DBI3
FBA_DBI2
FBA_DBI1
FBA_DBI0
FBA_DBI4
FBA_DBI5
FBA_DBI6
FBA_DBI7
FBA_CMD12
FBA_CMD15
FBA_CMD31
FBA_CMD28
FBA_CMD14
FBA_CLK0#
FBA_CLK0
FBA_CMD30
FBA_CLK1#
FBA_CLK1
FBA_CMD0
FBA_CMD5
FBA_CMD21
FBA_CMD16
FBA_CMD13
FBA_CMD29
FBA_VREFC
FBA_CMD8
FBA_CMD24
SI_BUILD
C5560
0.01UF_50V_2
C5561
0.01UF_50V_2
R5501
R5502
R5509
R5510
40.2_1%_2
R5503
R5500
121_1%_2
R5511
R5505
1K_5%_2
R5506
549_1%_2
R5508
1.33K_1%_2
R5507
931_1%_2
C5559
C5509
820PF_50V_2
GPIO10_FBVREF_SEL
Q5500
PJA138K
6015B0164101
R5600
100K_5%_2
HYNIX_H5GQ2H24AFR_T2C_BGA_170P
6019B0971701
C5510
C5508
C5507
C5506
C5505
C5504
C5503
C5502
C5501
C5500
0.1uF_16V_2
C5527
C5528
C5529
C5530
1UF_6.3V_2
C5512
C5511
10UF_6.3V_2
C5519
C5518
22UF_6.3V_3
C5541
C5558
C5557
C5556
C5555
C5554
C5553
C5552
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C5547
C5546
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C5544
C5536
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C5539
C5538

GDDR5 - 256Mx32/512Mx16, 1.5V 7Gbps / 1.35V 6Gbps	198244	Hynix	900852-371	H5GC8H24MJR-R0C	M	21nm
GDDR5 - 256Mx32/512Mx16, 1.5V 7Gbps / 1.35V 6Gbps	198247	Samsung	900852-971	K4G80325FB-HC28	B	20nm
GDDR5 - 256Mx32/512Mx16, 1.5V 7Gbps / 1.35V 6Gbps	198248	Micron	900852-671	MT51J256M32HF-70:A	A	20nm

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TITLE: 14" MI 2.0 Block Diagram

SIZE C | CODE CS | DOC.NUMBER 1310A28111-0-CPT | REV A

CHANGE by Wang.Abel | DATE 08-APR-2016

SHEET 60 of 67

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Small Board

CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

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TITLE: 14" MI 2.0 Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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SHEET 61 of 67

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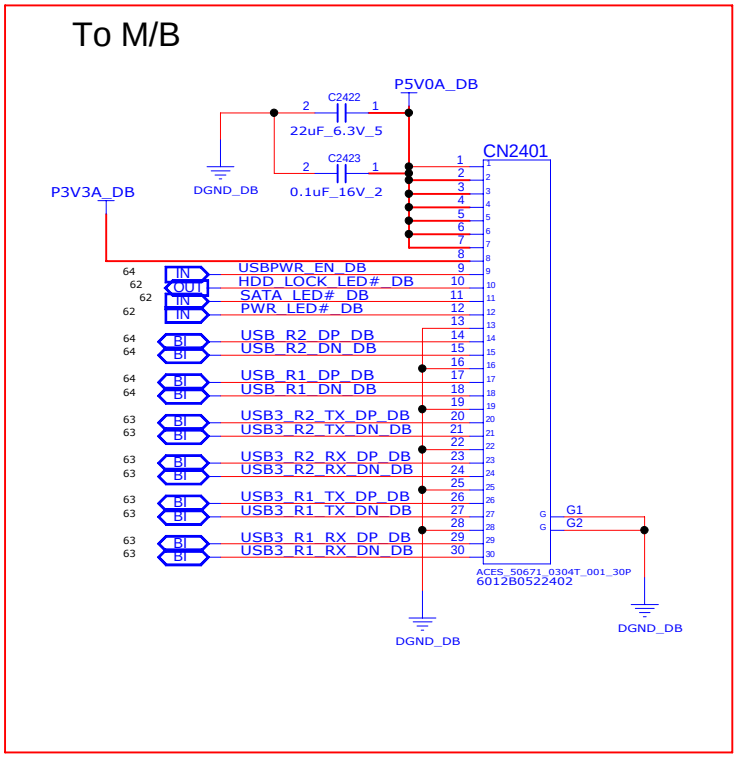
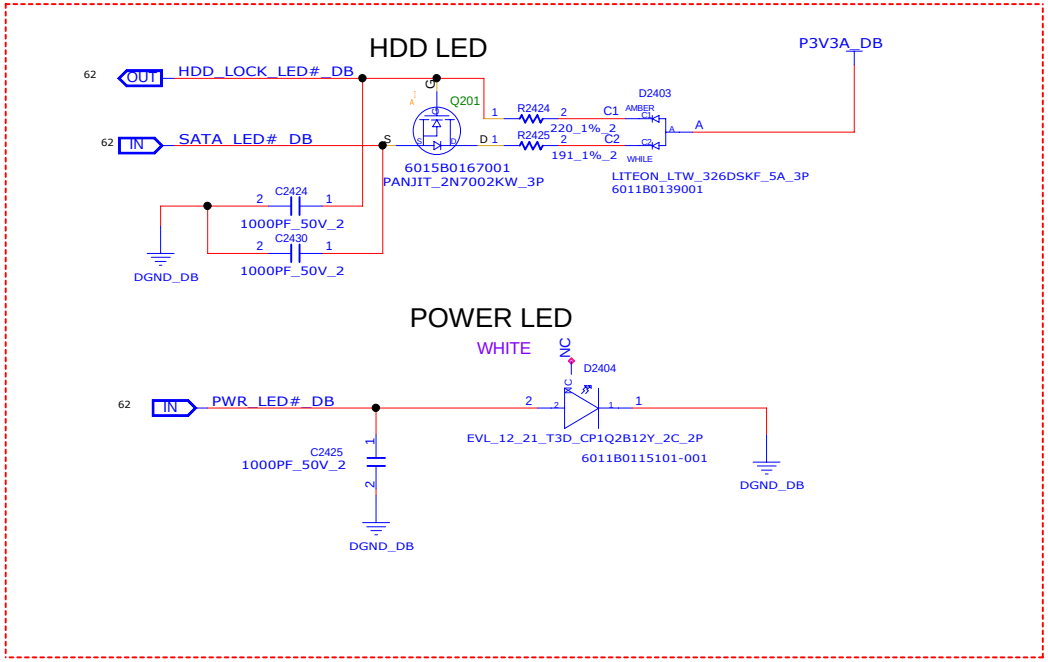
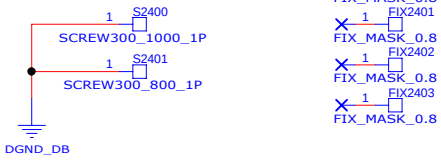
USB3.0 Board







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PCB P/N	6050A2811101	PCB VER	A

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SHEET of 62 67

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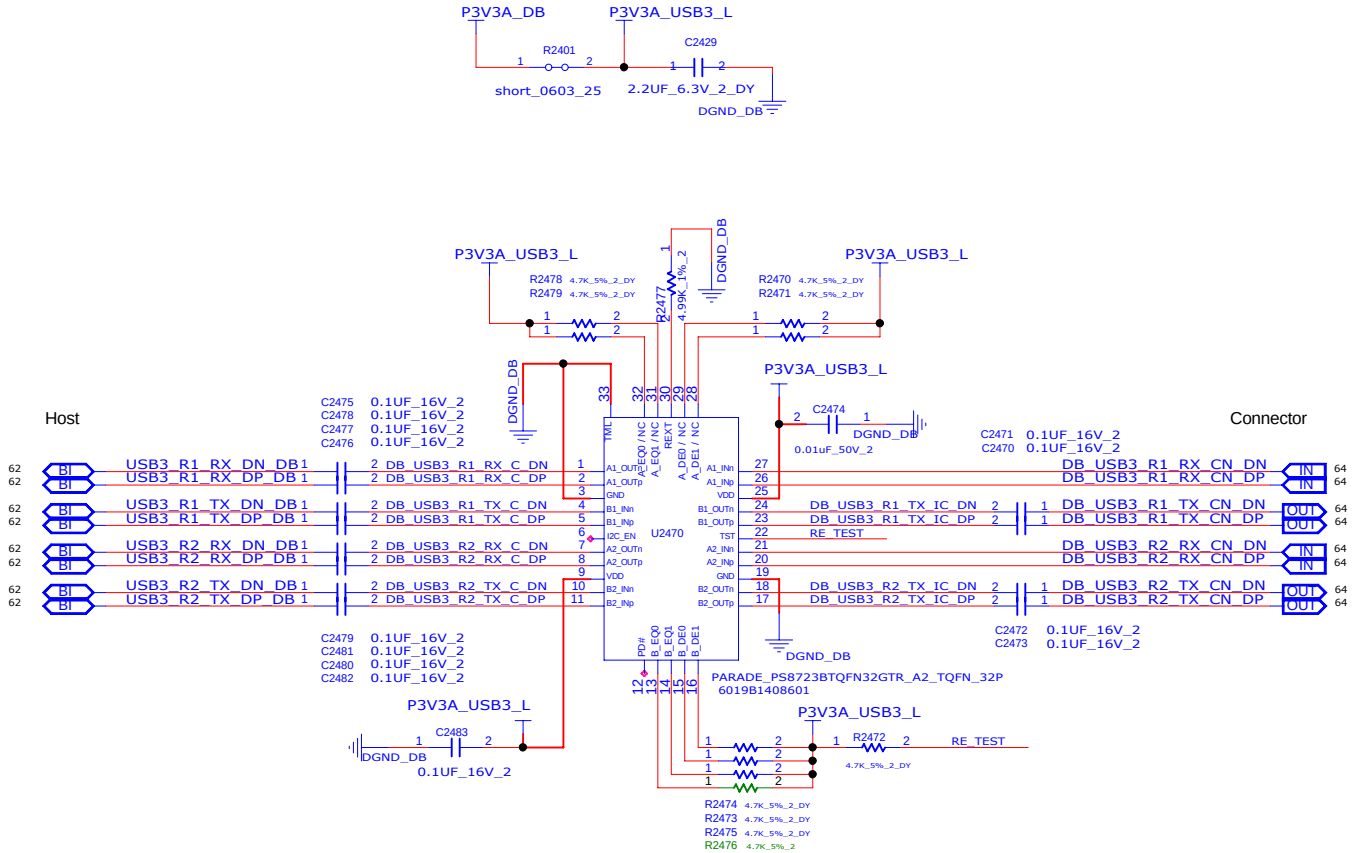
USB 3.0 ReDriver 2 Port



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A3	CS	1310A28111-0-CPT	A

SHEET 63 of 67

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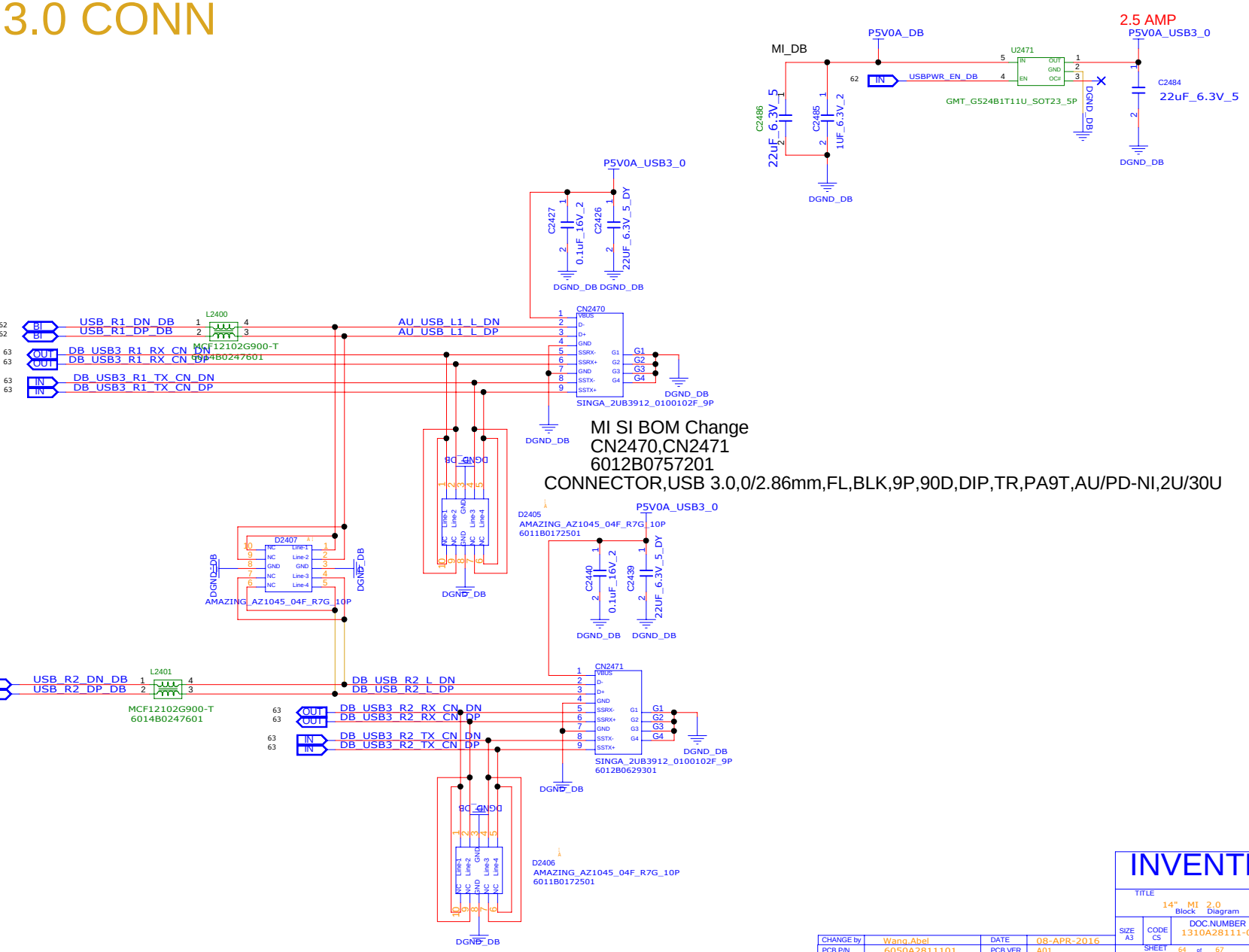
USB 3.0 CONN



MI SI BOM Change
CN2470,CN2471
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CONNECTOR,USB 3.0,0/2.86mm,FL,BLK,9P,90D,DIP,TR,PA9T,AU/PD-NI,2U/30U

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SIZE A3	CODE CS	DOC.NUMBER 1310A28111-0-CPT	REV A
SHEET 64 of 67			
CHANGE by Wang.Abel	DATE 08-APR-2016		
PCB P/N 6050A2811101	PCB VER A01		

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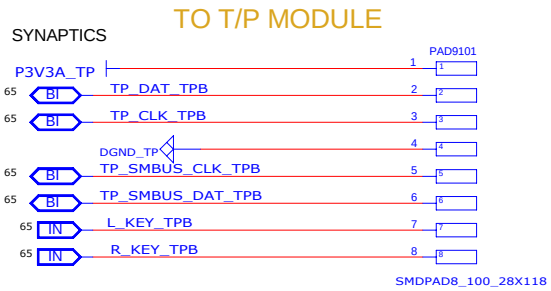
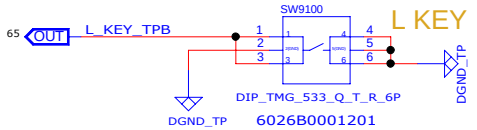
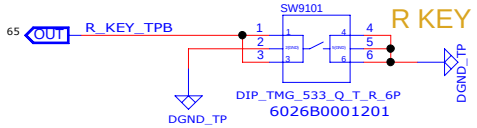
Pick button

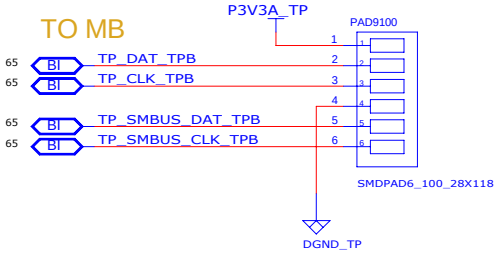
TOUCHPAD R / L BOARD

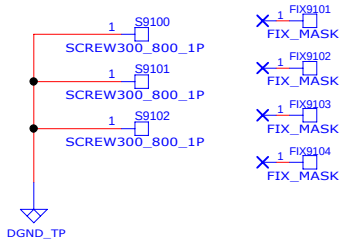




SW9000,SW9001
★PIN2,5 IS GND







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SHEET 65 of 67

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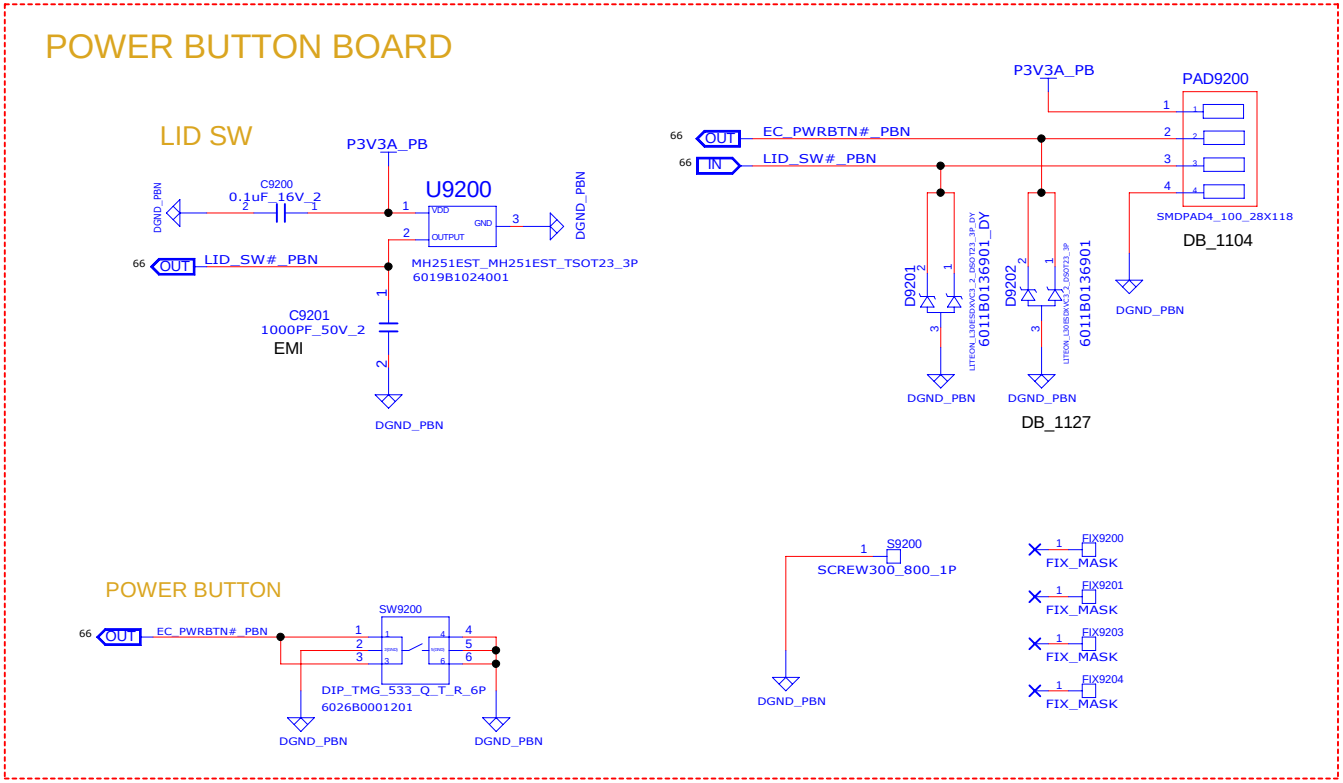
POWER BUTTON BOARD



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SHEET 66 of 67			

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CHANGE by	Wang.Abel	DATE	08-APR-2016
PCB P/N	6050A2811101	PCB VER	A01

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TITLE
14" MI 2.0
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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SHEET 67 of 67

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