

Project Name : A14IM01\_DDR3

Platform : Montevina Penryn(CPU)+Cantiga(NB)+ICH9M(SB)

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26.	0.75VS/+1.8VS/1.05V(OZ8116)
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M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

A14IMXX M/B V1.0 DDR3 (01 SLOT DDR3)

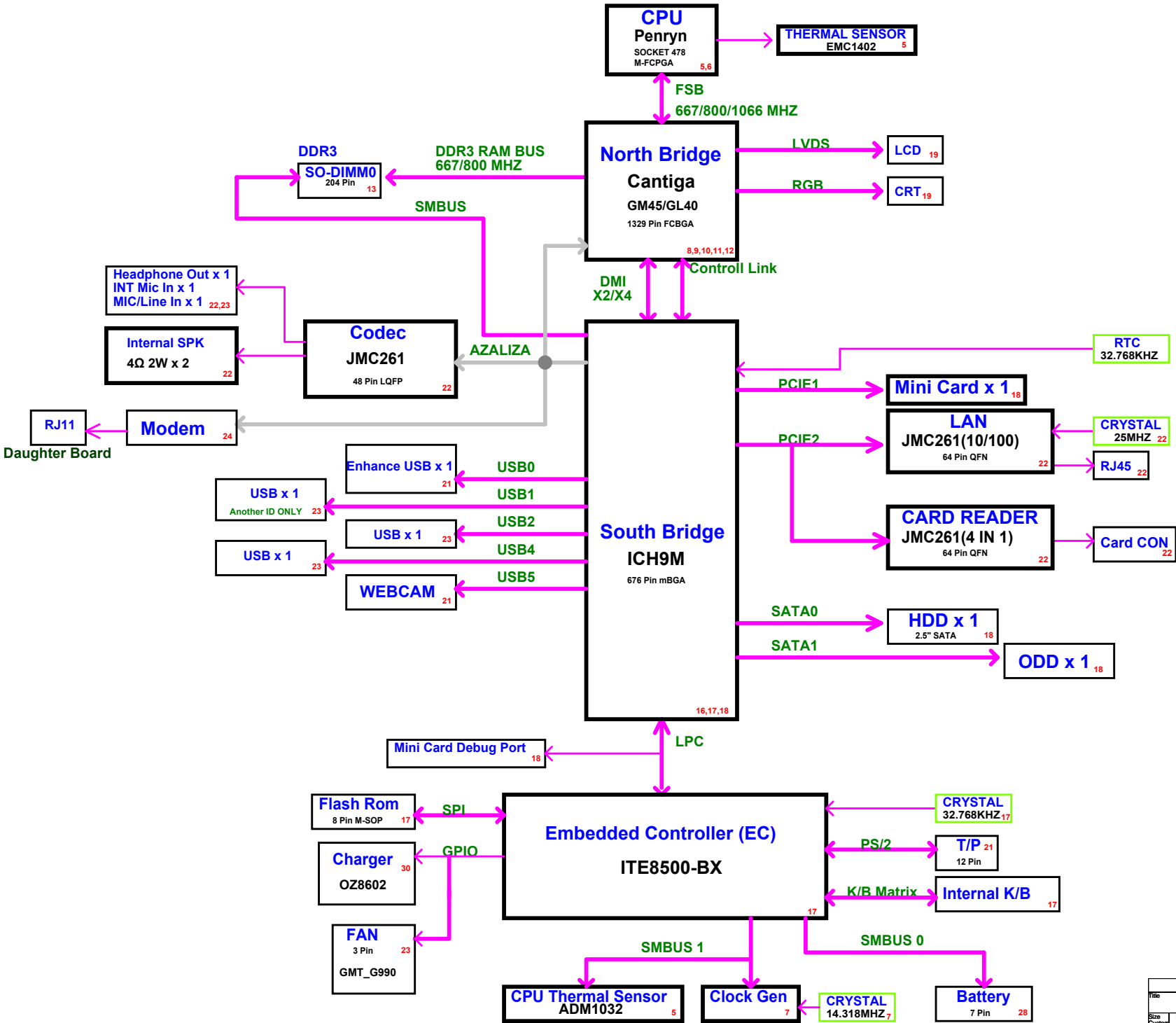
71R-R14IM0-T810

Esquemático REV A

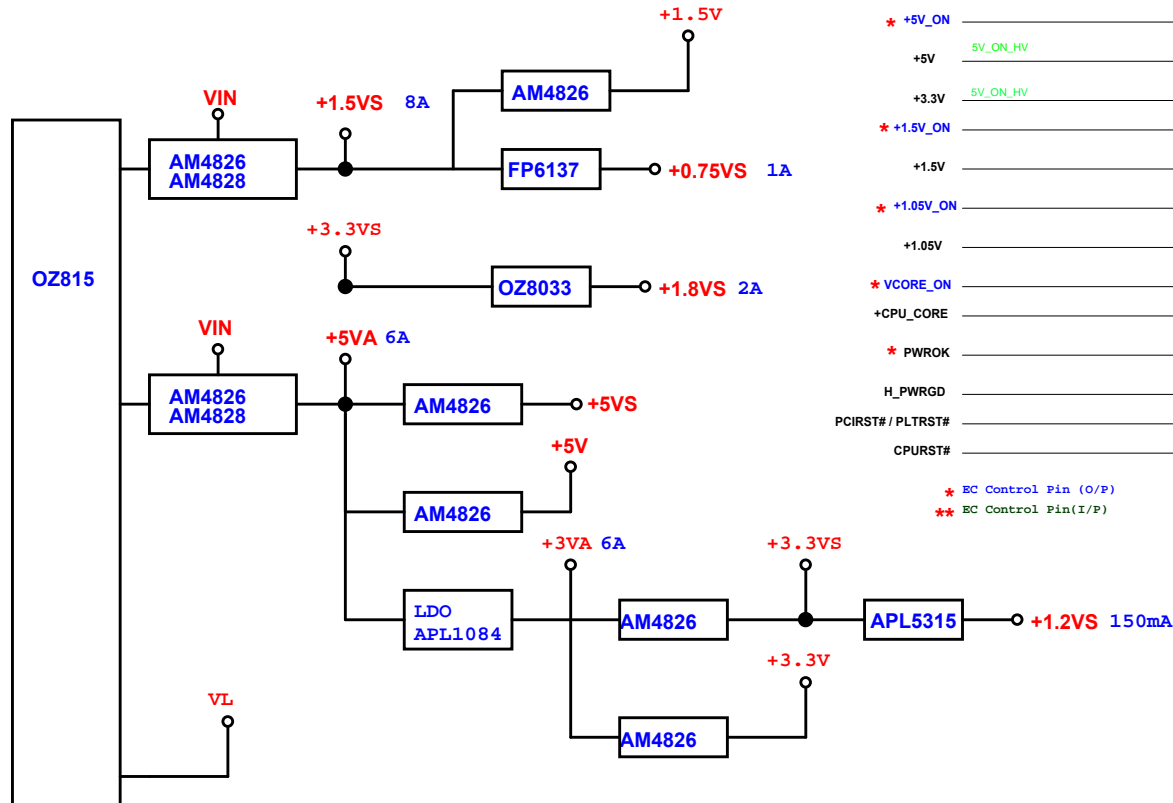
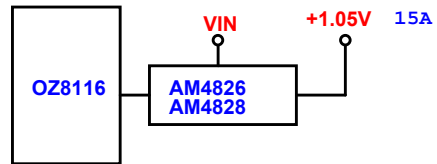
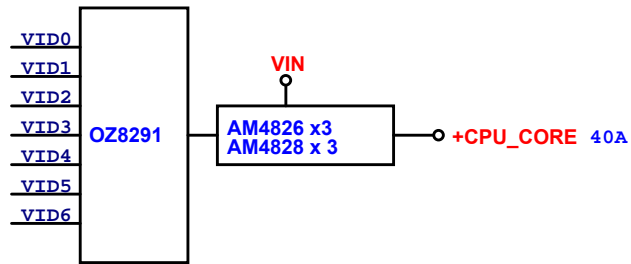
Na página 30 lista com as modificações REV B

A14IMXX A14IM01

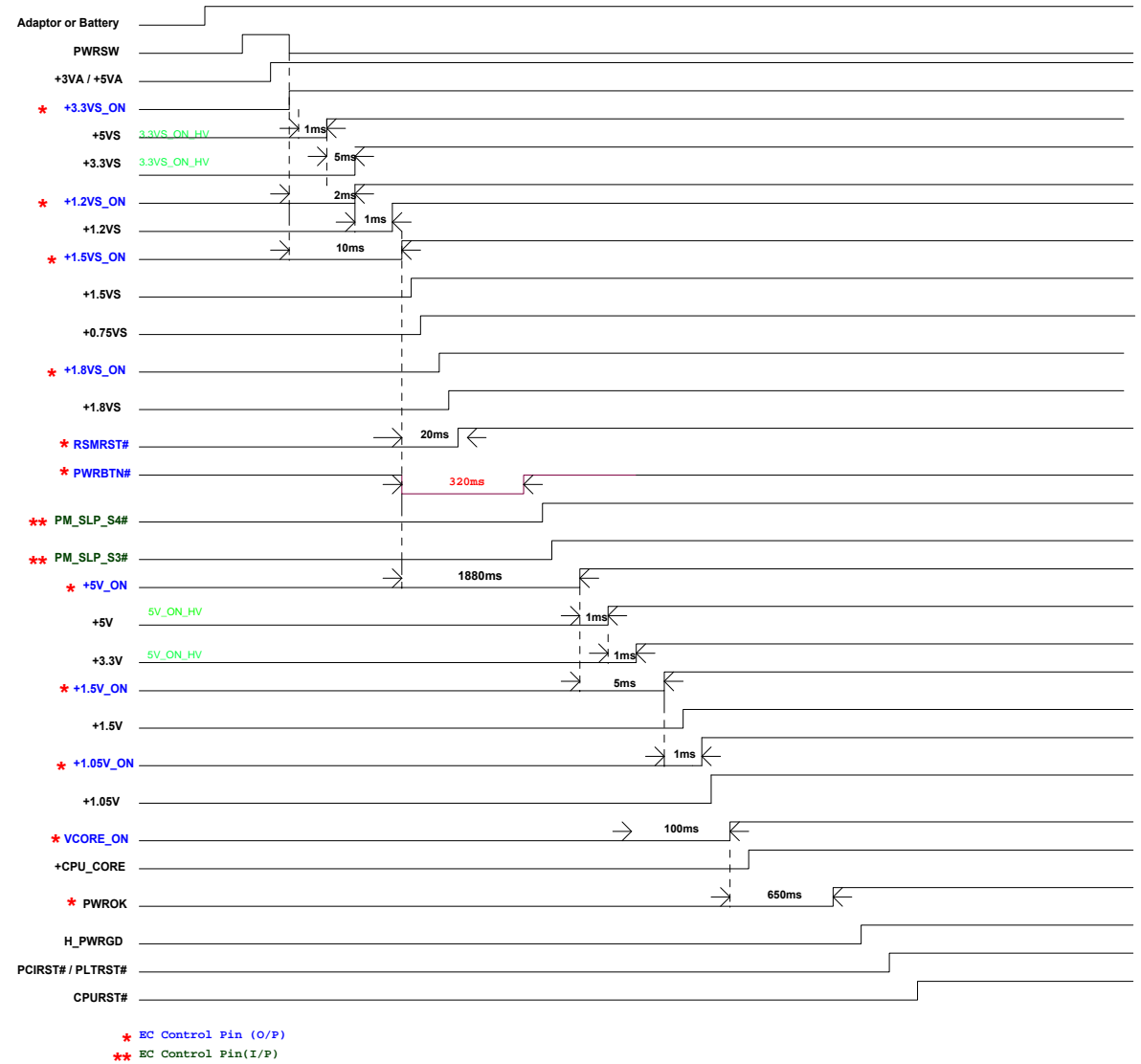
SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM



# System Poewr On Sequence



ICH9M GPIO	
GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	<b>N.C</b> (TACH3)
GPIO8	<b>N.C</b>
GPIO9	<b>N.C</b> (WOL_EN)
GPIO10	<b>N.C</b> (ALERT#)
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	<b>N.C</b> (GLAN_DOCK#)
GPIO14	<b>N.C</b> (NETDETECT)
GPIO15	PM_STPPCI#
GPIO17	<b>N.C</b> (TACH0)
GPIO18	<b>N.C</b>
GPIO19	SATA1GP
GPIO21	SATA0GP
GPIO22	<b>N.C</b> (SCLOCK)
GPIO23	LDRQ1#
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	QRT_STATE0
GPIO28	QRT_STATE1
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN
GPIO34	<b>N.C</b> (HDA_DOCK_RST)
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3

ITE8510 GPIO		Default Pull/Mode
GPA0	RF_LED#	UP / GPI
GPA1	EC_BSEL1	UP / GPI
GPA2	BT_L_BEEP	UP / GPI
GPA3	WLAN_PWR#	UP / GPI
GPA4	P_ID0	UP / GPI
GPA5	P_ID1	UP / GPI
GPA6	PM_RSMRST#	UP / GPI
GPA7	EC_BL_PWM	UP / GPI
GPB0	PM_SLP_S4#	UP / GPI
GPB1	PM_SLP_S3#	UP / GPI
GPB2	+1.05V_ON	Dn / GPI
GPB3	BAT_SMBCLK	/ GPI
GPB4	BAT_SMBDAT	/ GPI
GPB5	H_A20GATE	/ GPO
GPB6	H_RCIN#	UP / Funcl
GPB7	ENHANCE_USB#	Dn / GPI
GPC0	+1.5V_ON	Dn / GPI
GPC1	SMB_CLK_EC	/ GPI
GPC2	SMB_DAT_EC	/ GPI
GPC3	<b>N.C</b>	Dn / GPI
GPC4	SAVE_POWER	Dn / GPI
GPC5	SLP_S4_COY	Dn / GPI
GPC6	+3.3VS_ON	Dn / GPI
GPC7	CRT_DETECT	UP / GPI
GPD0	ADAP_IN	UP / GPI
GPD1	PWRBTN#	UP / GPI
GPD2	PLT_RST#	UP / Funcl
GPD3	<b>N.C</b>	UP / GPI
GPD4		UP / GPI
GPD5	PWR_USB_LED#	UP / GPI
GPD6	<b>N.C</b>	Dn / GPI
GPD7	SET_V	Dn / GPI
GPE0	LID#	Dn / GPI
GPE1	Fastcharge_EN	Dn / GPI
GPE2	PWROK	Dn / GPI
GPE3	Vcore_ON	Dn / GPI
GPE4	PWRSW	UP / GPI
GPE5	+1.2VS_ON	Dn / GPI
GPE6	WLAN_ON	Dn / GPI
GPE7	AMP_MUTE#	UP / GPI
GPF0	<b>N.C</b>	UP / GPI
GPF1	<b>N.C</b>	UP / GPI
GPF2	<b>N.C</b>	UP / GPI
GPF3	CHG_ON#	UP / GPI
GPF4	TP_CLK	UP / GPI
GPF5	TP_DATA	UP / GPI
GPF6	<b>N.C</b>	UP / GPI
GPF7	<b>N.C</b>	UP / GPI
GPG0	+3.3VA	Dn/GPO/TM
GPG1	+5V_ON	Dn/GPO/ID7
GPG2	<b>N.C</b>	
GPG6	WEBCAN_ON	Dn / GPI
GPH0	SAFETY_PROTECT	Dn/GPI/ID0
GPH1	+1.8VS_ON	Dn/GPI/ID1
GPH2	SENBAT_V	Dn/GPI/ID2
GPH3	CHG_G_LED	Dn/GPI/ID3
GPH4	CHG_R_LED	Dn/GPI/ID4
GPH5	BATOFF	Dn/GPI/ID5
GPH6	PWR_LED	Dn/GPI/ID6

ITE8510 GPIO		Default Pull/Mode
GPI0	<b>N.C</b>	/GPI/ADC
GPI1	LCDSW0	/GPI/ADC
GPI2	LCDSW1	/GPI/ADC
GPI3	<b>N.C</b>	/GPI/ADC
GPI4	BAT_I	/GPI/ADC
GPI5	BATT_TEMP	/GPI/ADC
GPI6	ADAPTOR_1	/GPI/ADC
GPI7	BAT_V	/GPI/ADC
GPJ0	EC_BL_ON	/GPI/DAC
GPJ1	EC_PROCHOT	/GPI/DAC
GPJ2	FAN_CTRL0	/GPI/DAC
GPJ3	CHG_REF	/GPI/DAC
GPJ4	CHG_I	/GPI/DAC
GPJ5	PM_THROTTLING#	/GPI/DAC

Penryn CPU				
	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-6+	1.05	44.0	36	

Cantiga			
VCC	ICC(mA)	W	TEMP(℃)
+3.3V	262	0.87	105
+1.8VS	3249	5.73	
+1.5V	86	0.129	
+1.05	14688.52	15.43	

ICH9M			
VCC	ICC(mA)	mW	TEMP(℃)
+5V	4	20	70
+5VS	2	10	
+3.3V	347	1145.1	
+3.3VS	212	699.6	
+1.5V	1988	2982	
+1.05V	1634	1715.7	

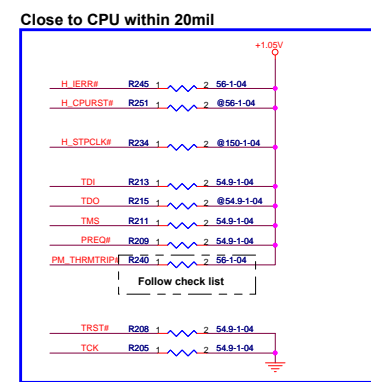
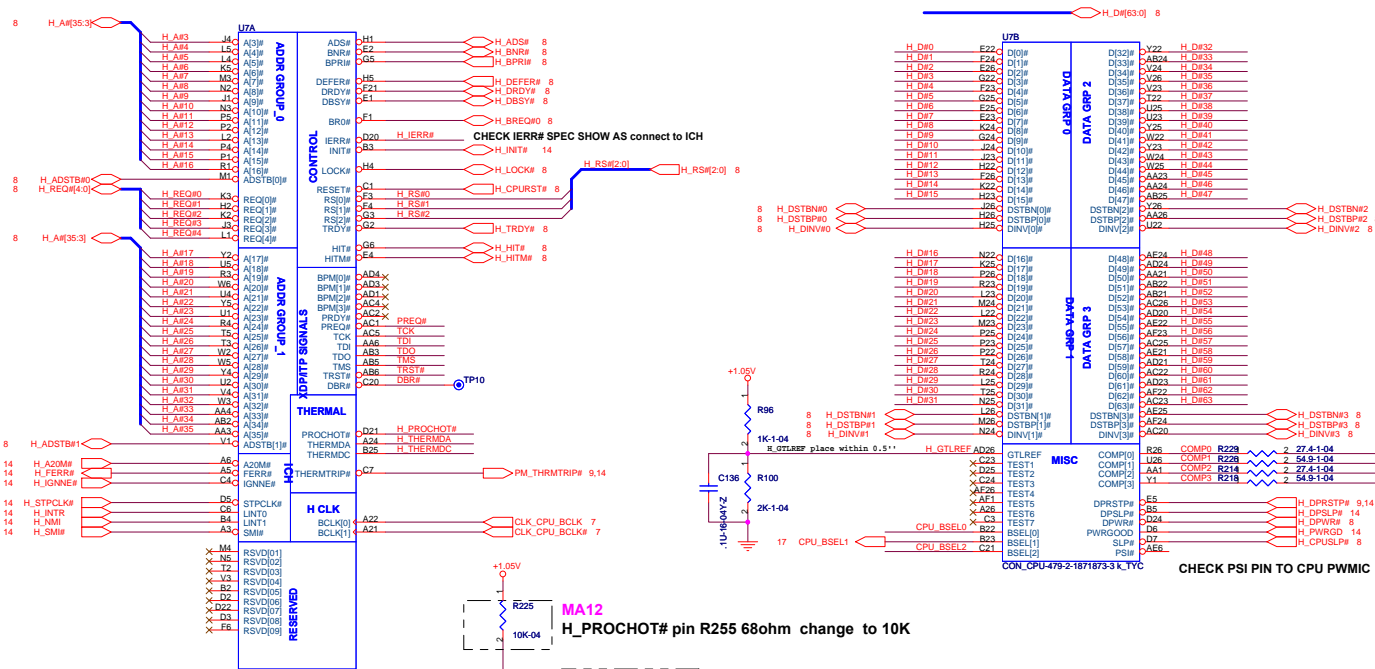
ITE8500			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	100	330	70

CLOCK GENERATOR			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	1000	3300	70

IDT92HD81			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V(DVDD)	200	660	70
+5V(AVDD)	1000	5000	

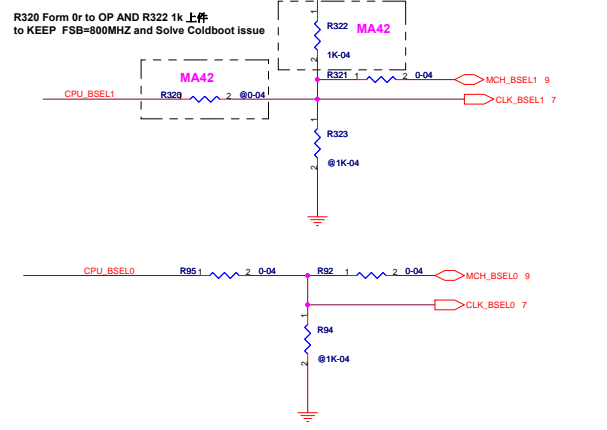
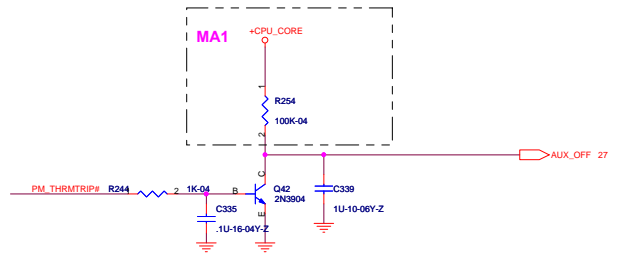
ADM1032			
VCC	ICC	mW	TEMP(℃)
+3.3V	170uA	0.56	150

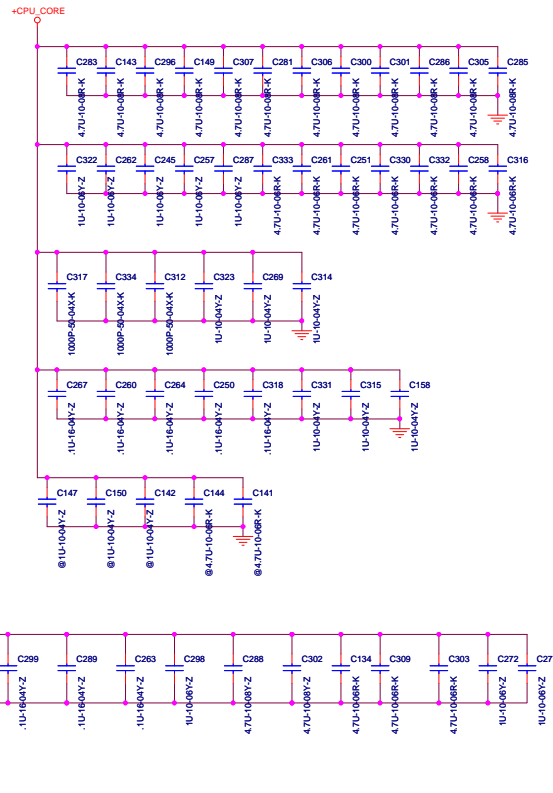
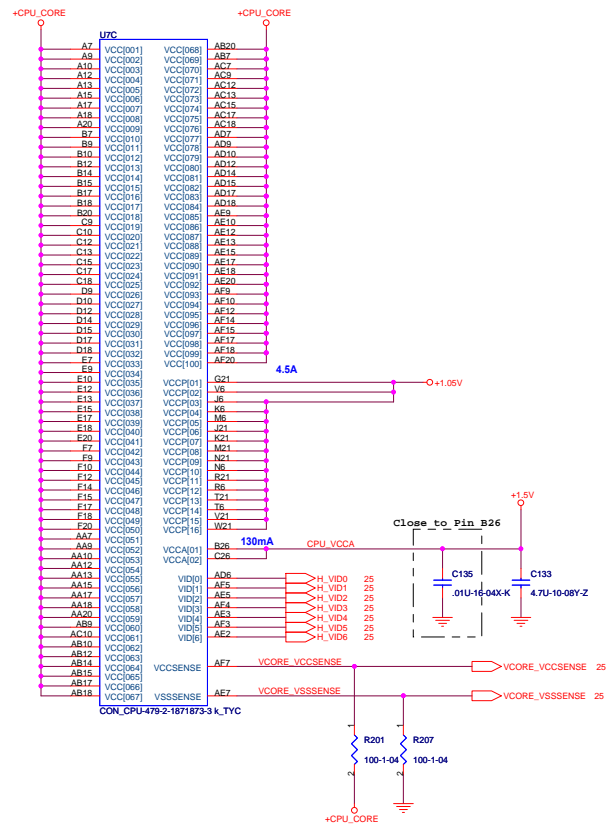
JMC261			
VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	300	990	70
+1.2VS	150	180	



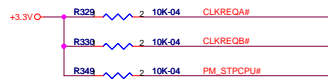
FSB	BSEL	BSEL2	BSEL1	BSEL0	MHZ
FSB667	0	1	1	1	166
FSB800	0	1	1	0	200
FSB1066	0	0	0	0	266

**R254 Change power plane form +3.3v to VCORE Solve +5VA drop by AUX\_OFF issue**

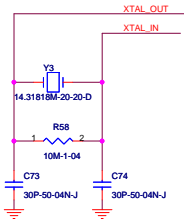
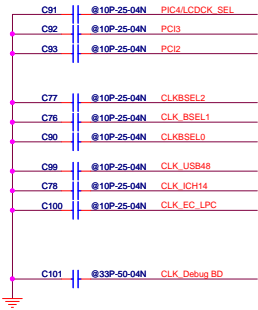




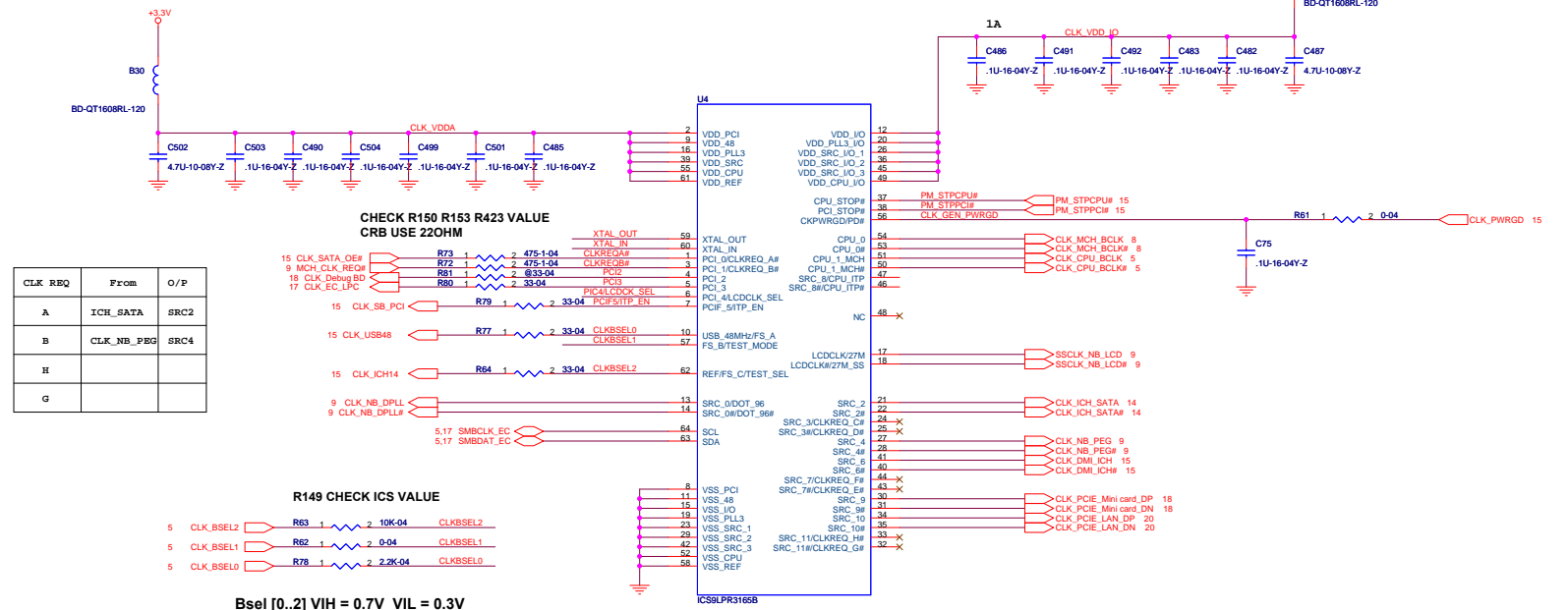
UTD		
A4	VSS[001]	VSS[082]
A5	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A15	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
A24	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C6	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D6	VSS[027]	VSS[108]
D11	VSS[028]	VSS[109]
D13	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D23	VSS[032]	VSS[113]
D26	VSS[033]	VSS[114]
E3	VSS[034]	VSS[115]
E6	VSS[035]	VSS[116]
E8	VSS[036]	VSS[117]
E11	VSS[037]	VSS[118]
E14	VSS[038]	VSS[119]
E16	VSS[039]	VSS[120]
E19	VSS[040]	VSS[121]
E23	VSS[041]	VSS[122]
E26	VSS[042]	VSS[123]
F3	VSS[043]	VSS[124]
F6	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F23	VSS[050]	VSS[131]
F26	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G11	VSS[053]	VSS[134]
G13	VSS[054]	VSS[135]
G16	VSS[055]	VSS[136]
G19	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H11	VSS[059]	VSS[140]
H13	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J6	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N11	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
P4	VSS[082]	VSS[163]



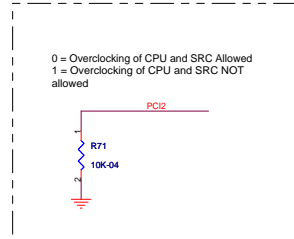
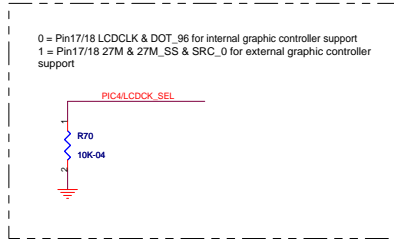
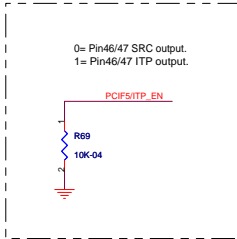
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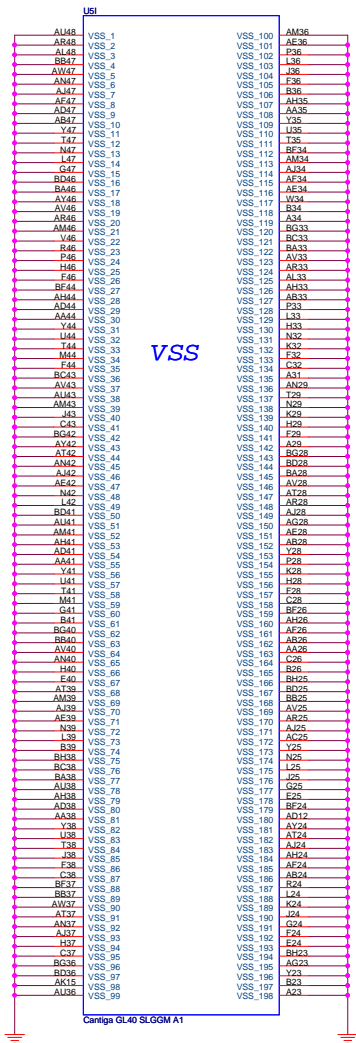


$C_e = 2 * C_L - (C_s + C_i)$   
 $C_L$  = Crystal Load Cap = 20P  
 $C_i$  = IC internal Cap = 5P  
 $C_s$  = 2P  
 $C_e$  = Crystal external Cap = 33P

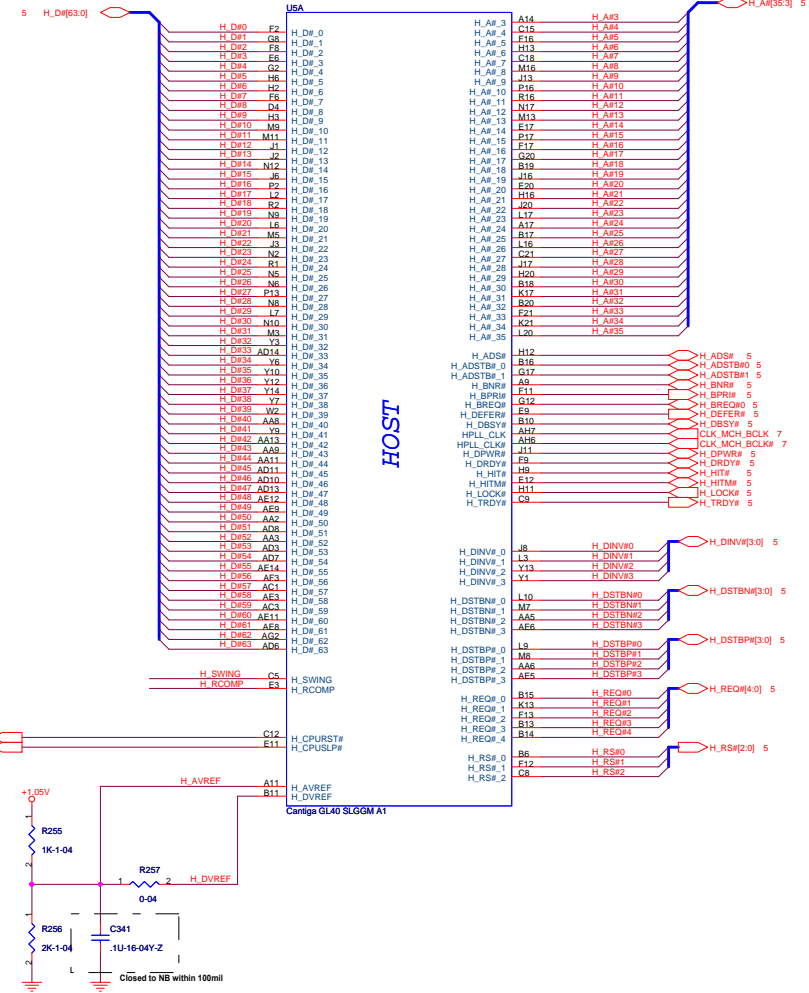
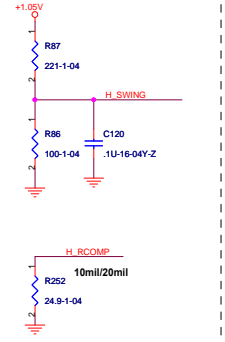


\*Need reserved space for 72Pin CLOCK GEN\*



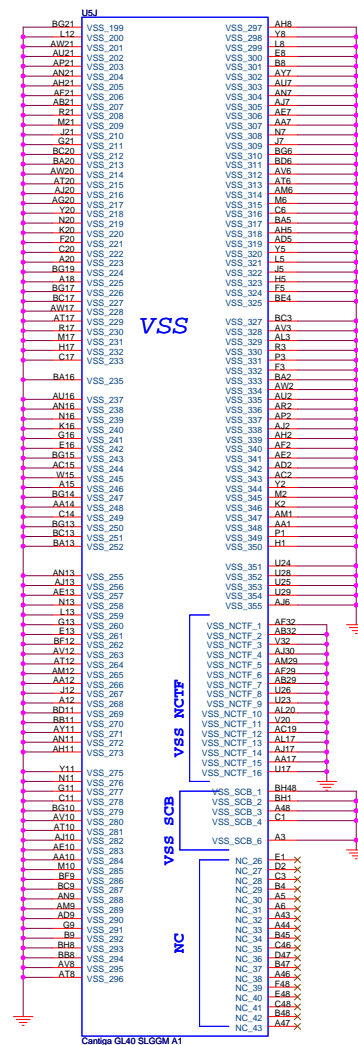
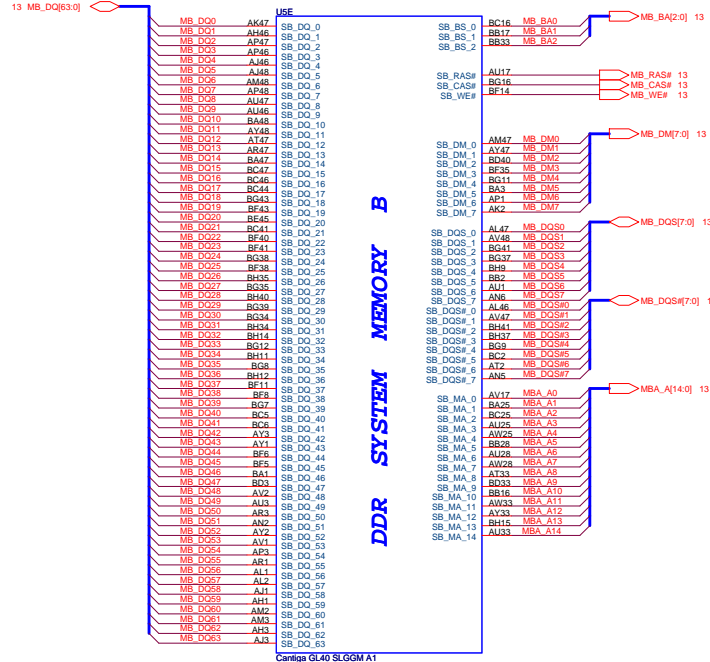
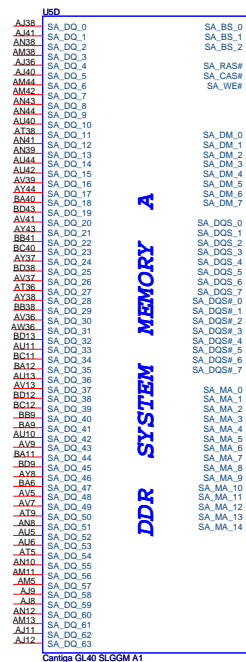


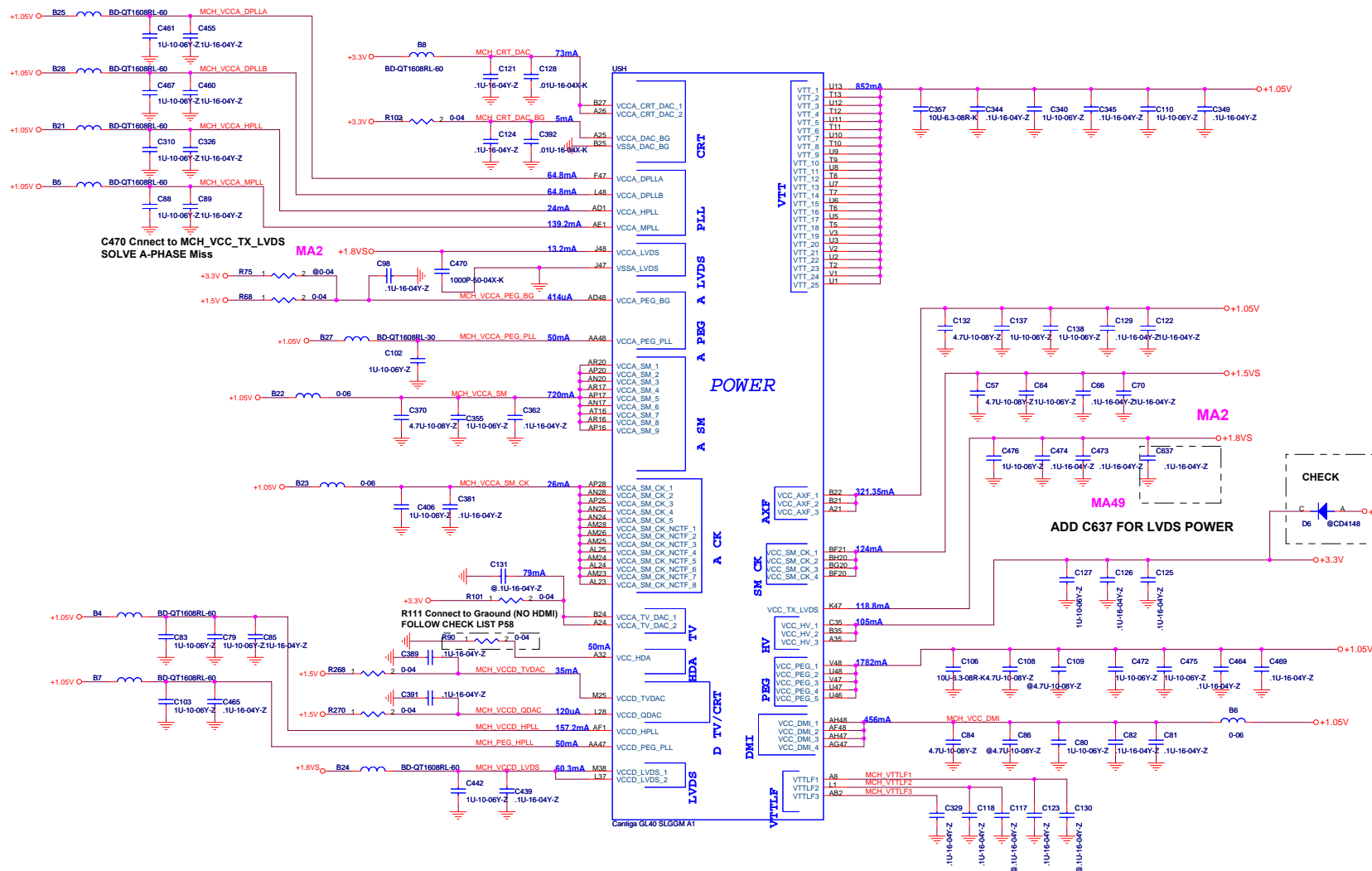
### Reference Voltage for RCOMP





SHUTTLE INC			
Title			
A14IM01			
Size	Document Number	Rev	
Custom	SCHEMATIC1	A	
NB DDR BUS / GPU / PCIE			
Date:	Tuesday, November 24, 2009	Sheet	9 of 30

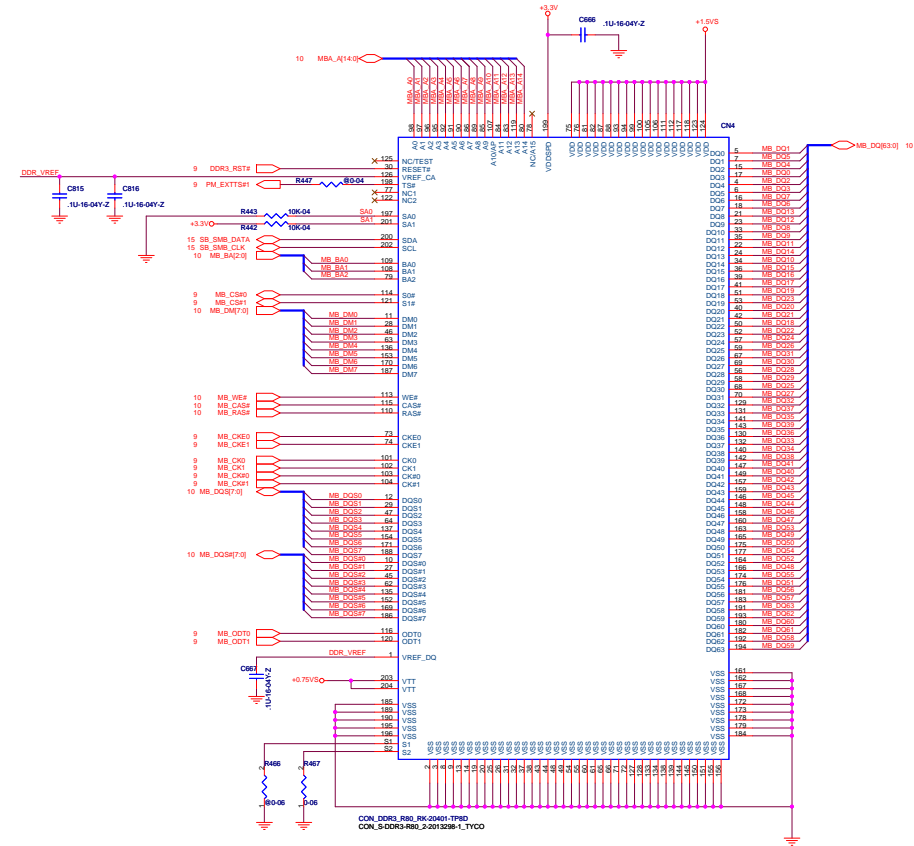
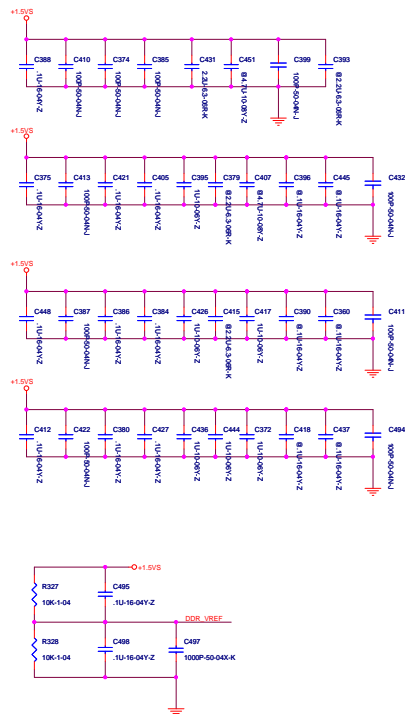


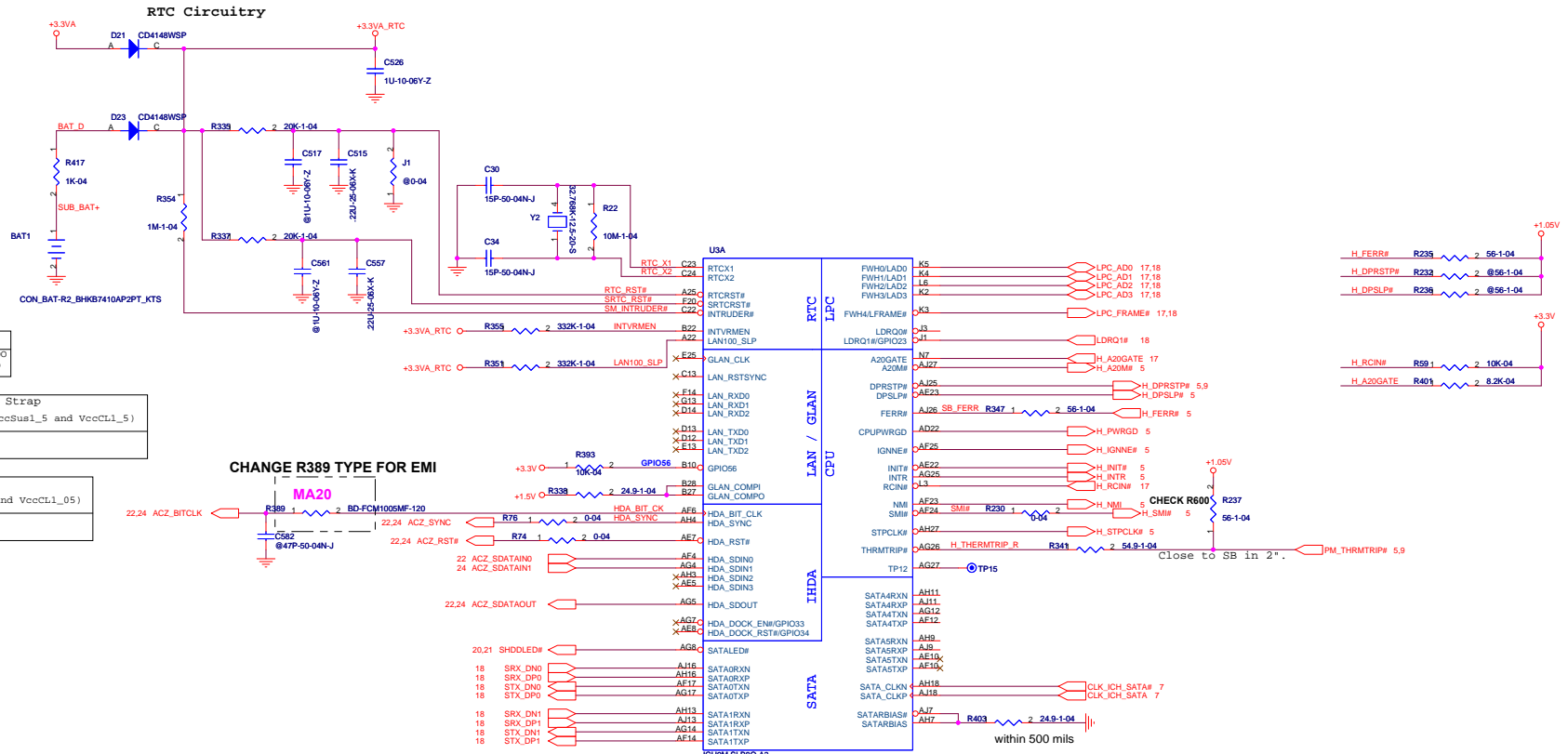




## DDR Termination

The diagram illustrates the termination of a 33-MHz signal path. It shows two 33-MHz buffers, MS\_C12SPR\_04 and MS\_C12SPR\_04, connected to a 33-MHz clock source. The buffers are terminated with 33-ohm resistors. The diagram also shows the connection of the buffers to the DDR memory array, which is terminated with 33-ohm resistors. The termination is implemented using a 33-ohm resistor network connected to the 33-MHz clock source.

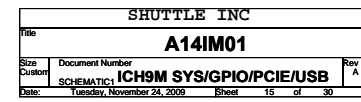




SM\_INTRUDER#  
0 = Disable Internal 1.5Vs LDO  
1 = Enable Internal 1.5Vs LDO

ICH9-M Internal VR Enable Strap  
(Internal VR for VccSusi\_05, VccSusi\_5 and VccCL1\_5)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)

ICH9-M LAN100\_SLP Strap  
(Internal VR for VccLAN1\_05 and VccCL1\_05)  
Low = Internal VR Disabled  
High = Internal VR Enabled  
(Default)



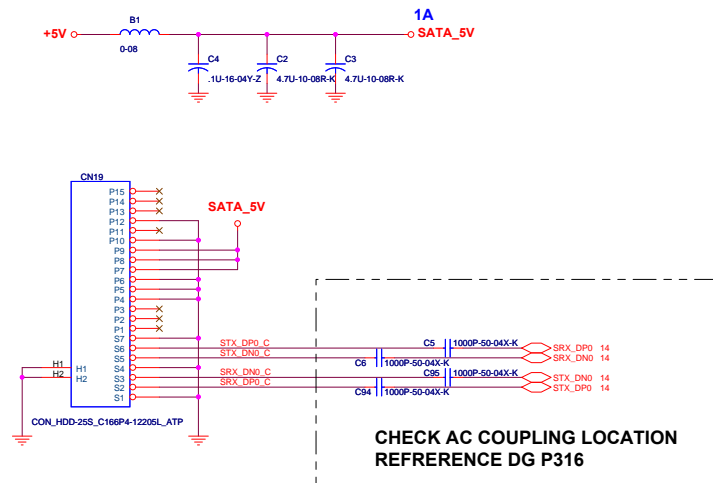




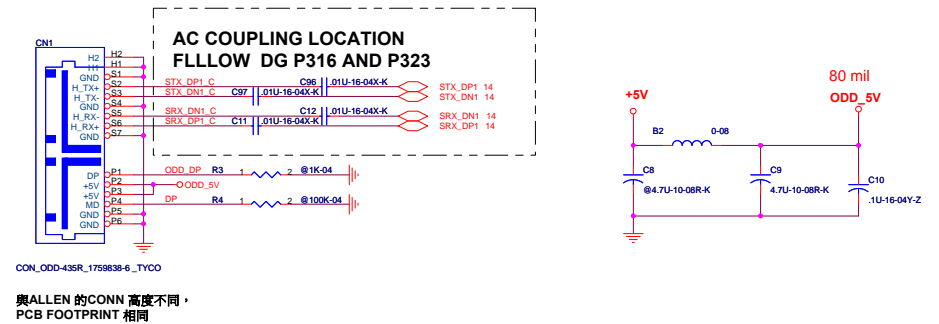




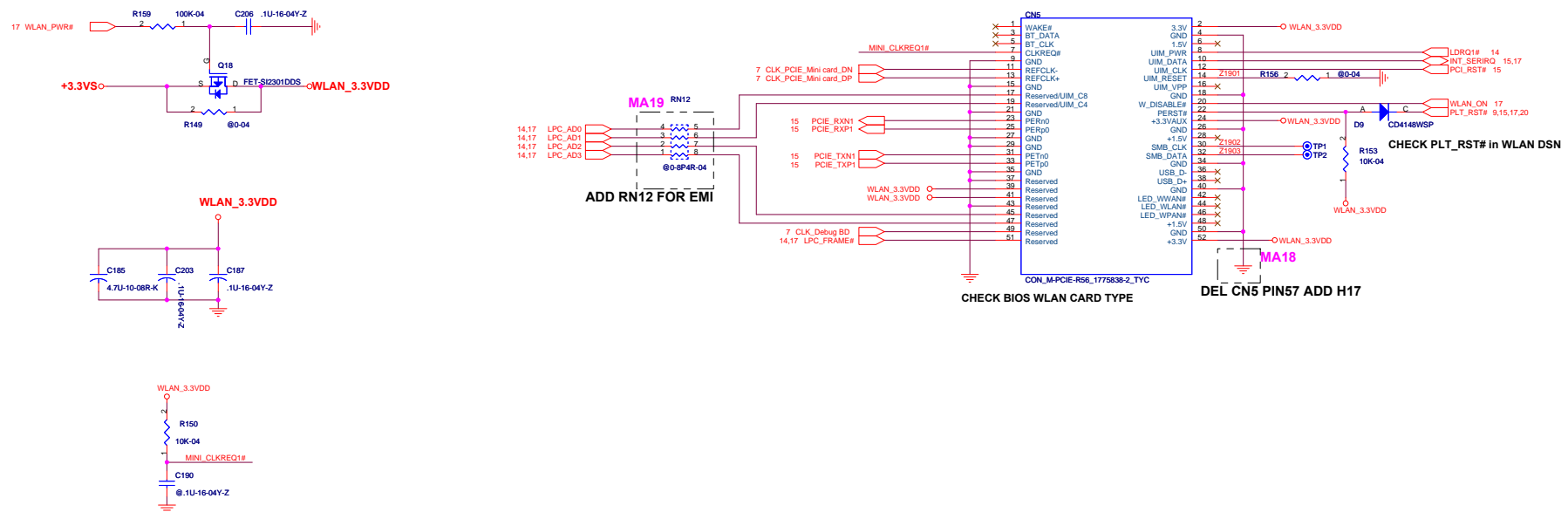
## SATA-HDD



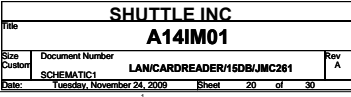
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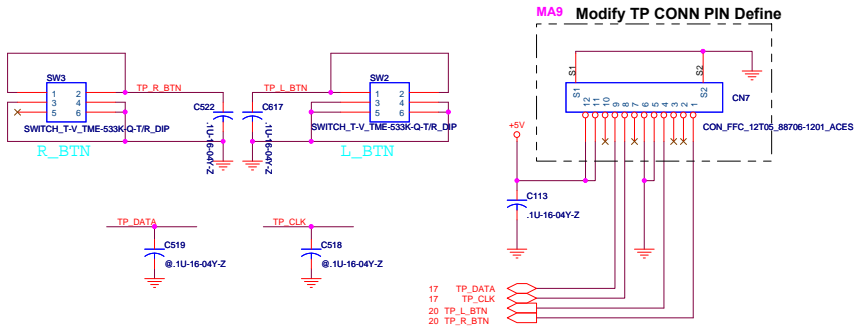
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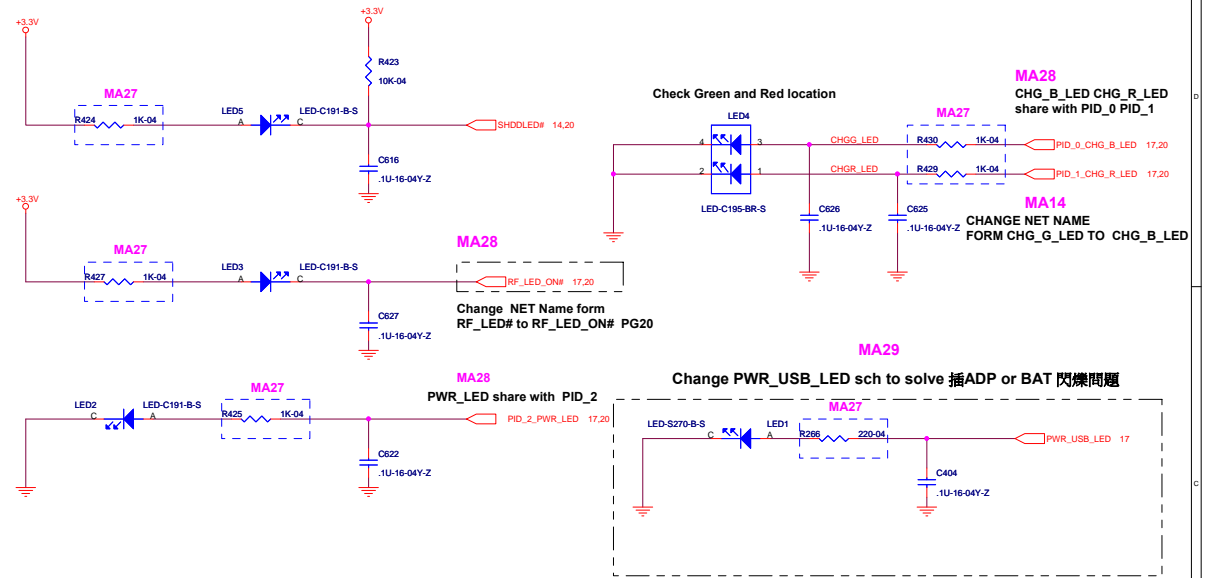




## Touch Pad

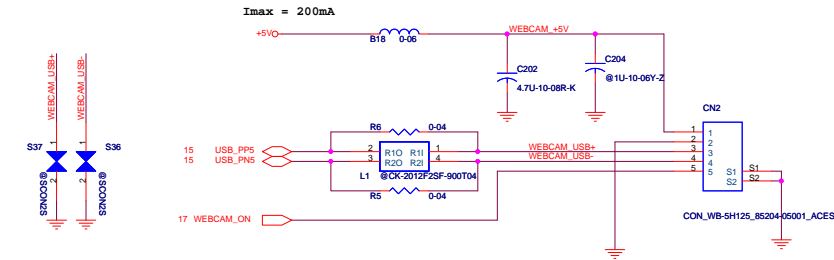


## LED MA27 - R424,R427,R425,R430,R429,R266 Change to 220-04

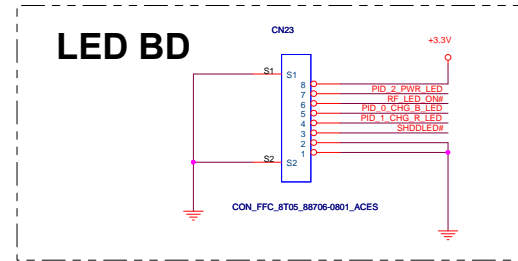


## WEBCAM CON

WEBCAM_ON	
1	ON
0	OFF

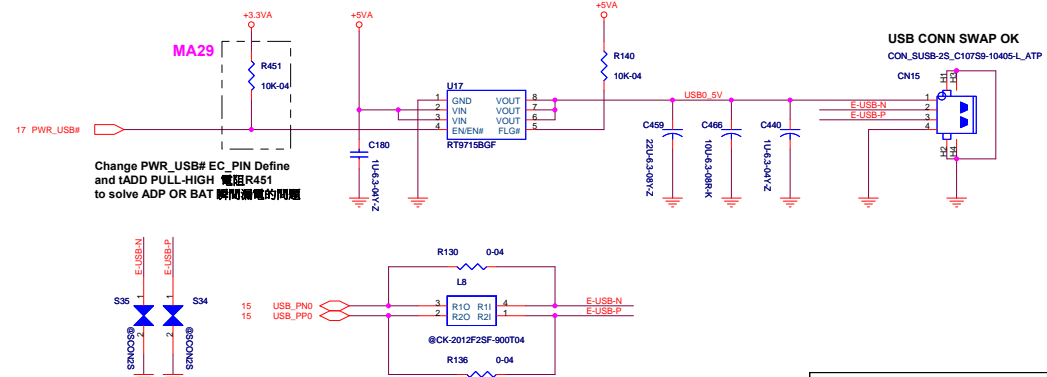


## LED BD



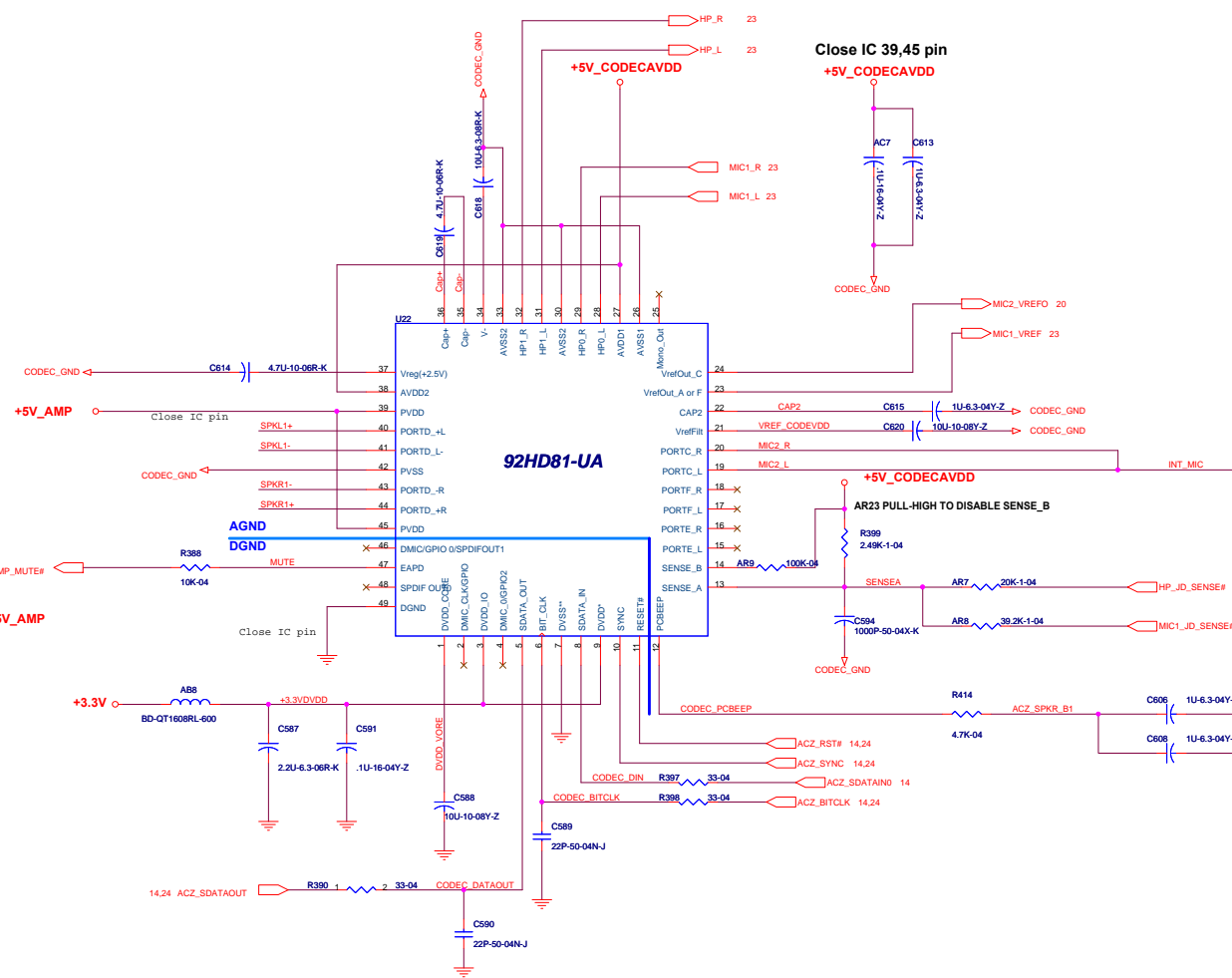
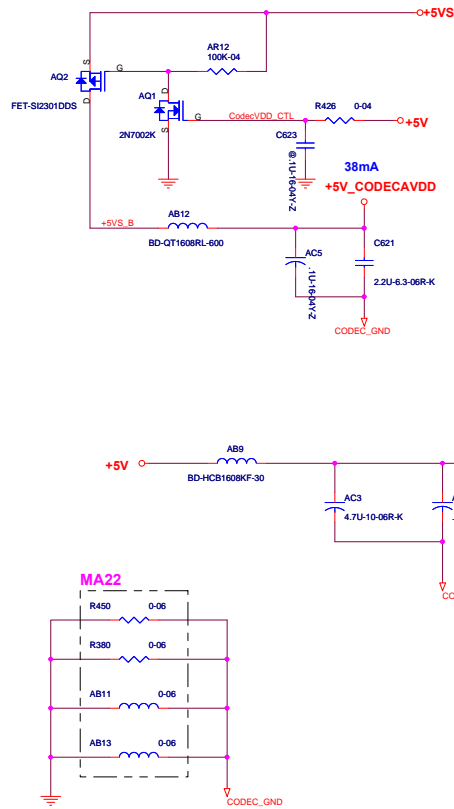
- MA14 ADD LED CONN CN23
- MA28 Change CN23 PIN7 NET Name form RF\_LED# to RF\_LED\_ON# PG20
- CHG\_B\_LED CHG\_R\_LED PWR\_LED share with PID\_0 PID\_1 PID\_2
- MA14 CHANGE CN23 PIN5 DEFINE FORM CHG\_G\_LED TO CHG\_B\_LED

## ENHANCE USB Port

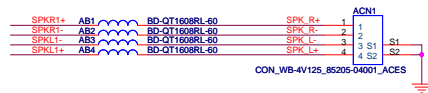


# CODEC 92HD81

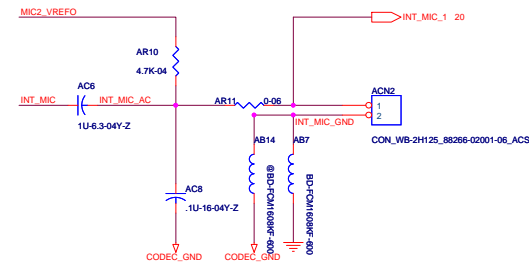
## AMP VDD



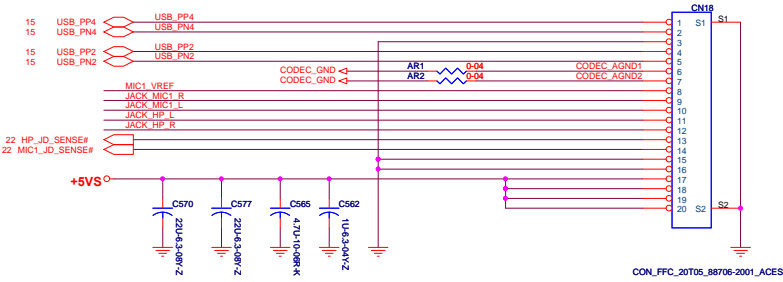
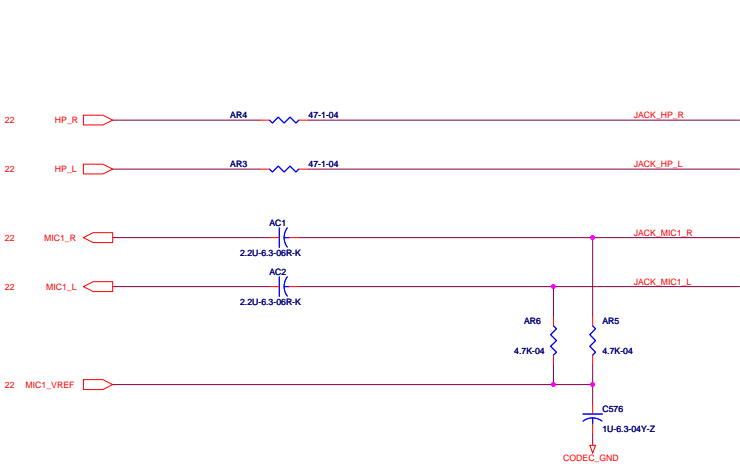
## INT\_SPEAKER



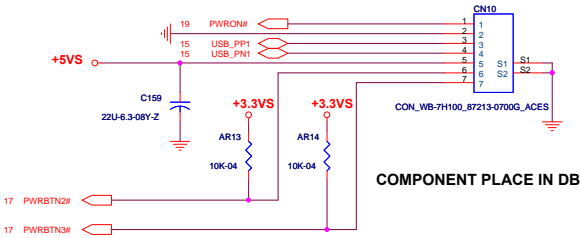
## INT\_MIC



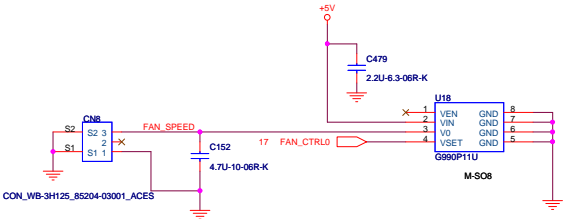
# EXT MIC/EXT Line In/ EXT USB JACK



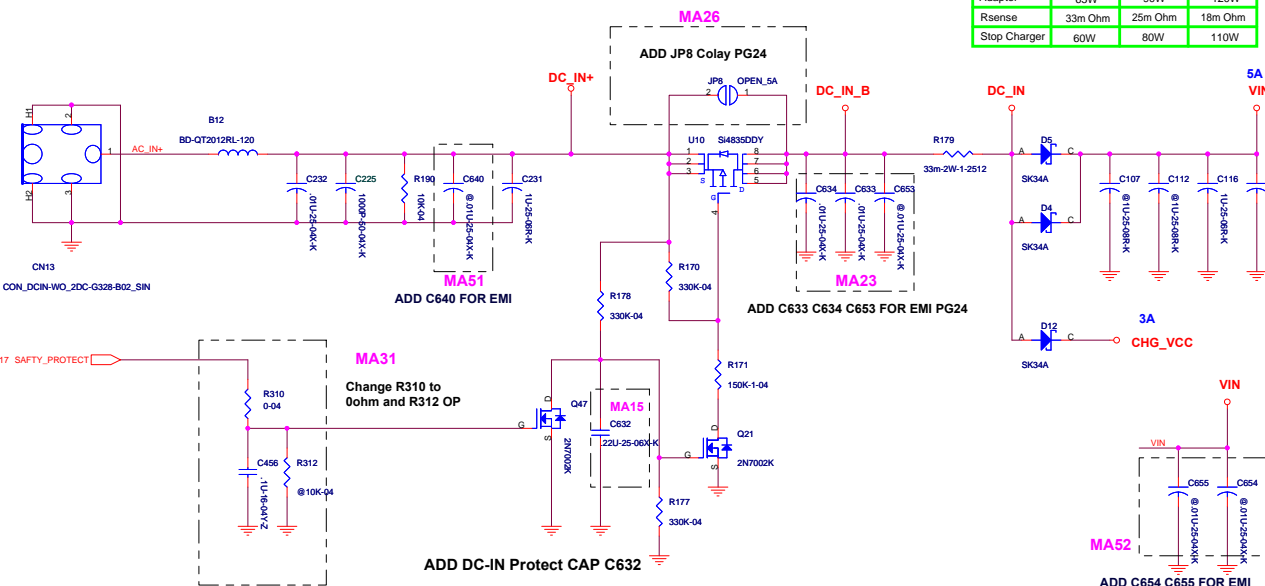
## EXT USB PORT 4



## CPU FAN CONTROL

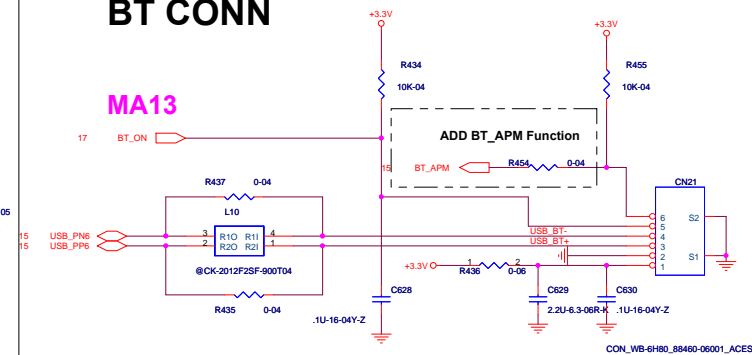


# DC IN



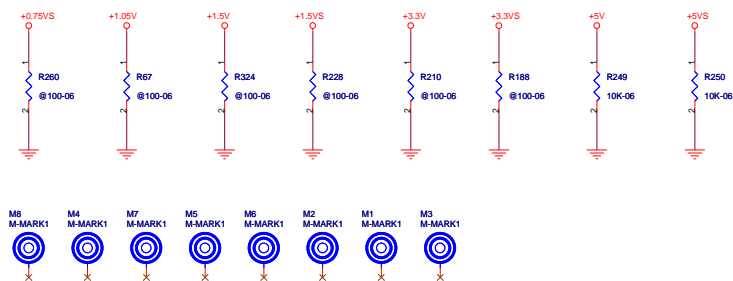
PROJECT	F50I0	F50I0	F50I5
Adaptor	65W	90W	120W
Rsense	33m Ohm	25m Ohm	18m Ohm
Stop Charger	60W	80W	110W

# BT CONN

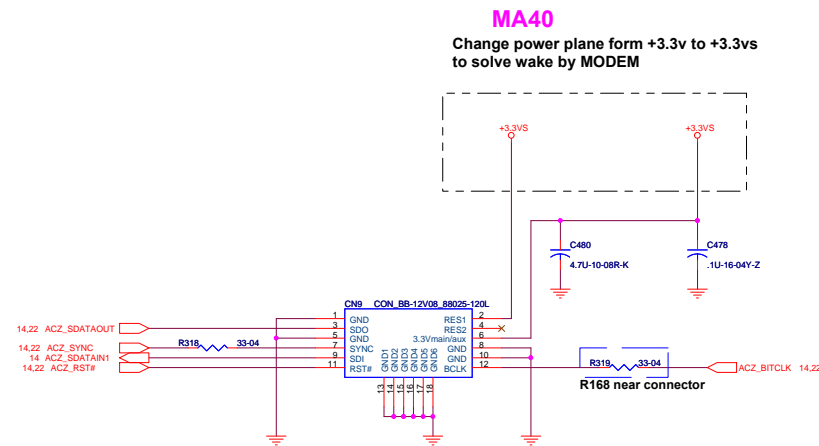


CHECK BT TYPE AND Life power function

# Discharge Resistor



# MDC





VID: 0.8~1.175V  
Icc max: 40A  
LLS: set to 2.1mV/A

ADD R432 Pull-High to +3.3V in DELAY\_VR\_PWRGOOD solve open issue

B16 上件 , JP2 OPEN FOR EMI

CHECK BATTERY Leacking current

MA45 ADD C641 C642 FOR EMI

OCP:50A

MA45 Change C201 to 0402 type

DEL-CSN-Connect-to-GND NET

MA45 ADD JP9 FOR EMI

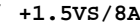
Change C215 Location BY O2

VID TABLE

	6	5	4	3	2	1	0	Vcore	Status
0	0	0	1	0	0	0	0	1.2875	(HFM)
0	0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	1	0.0000	Shut down

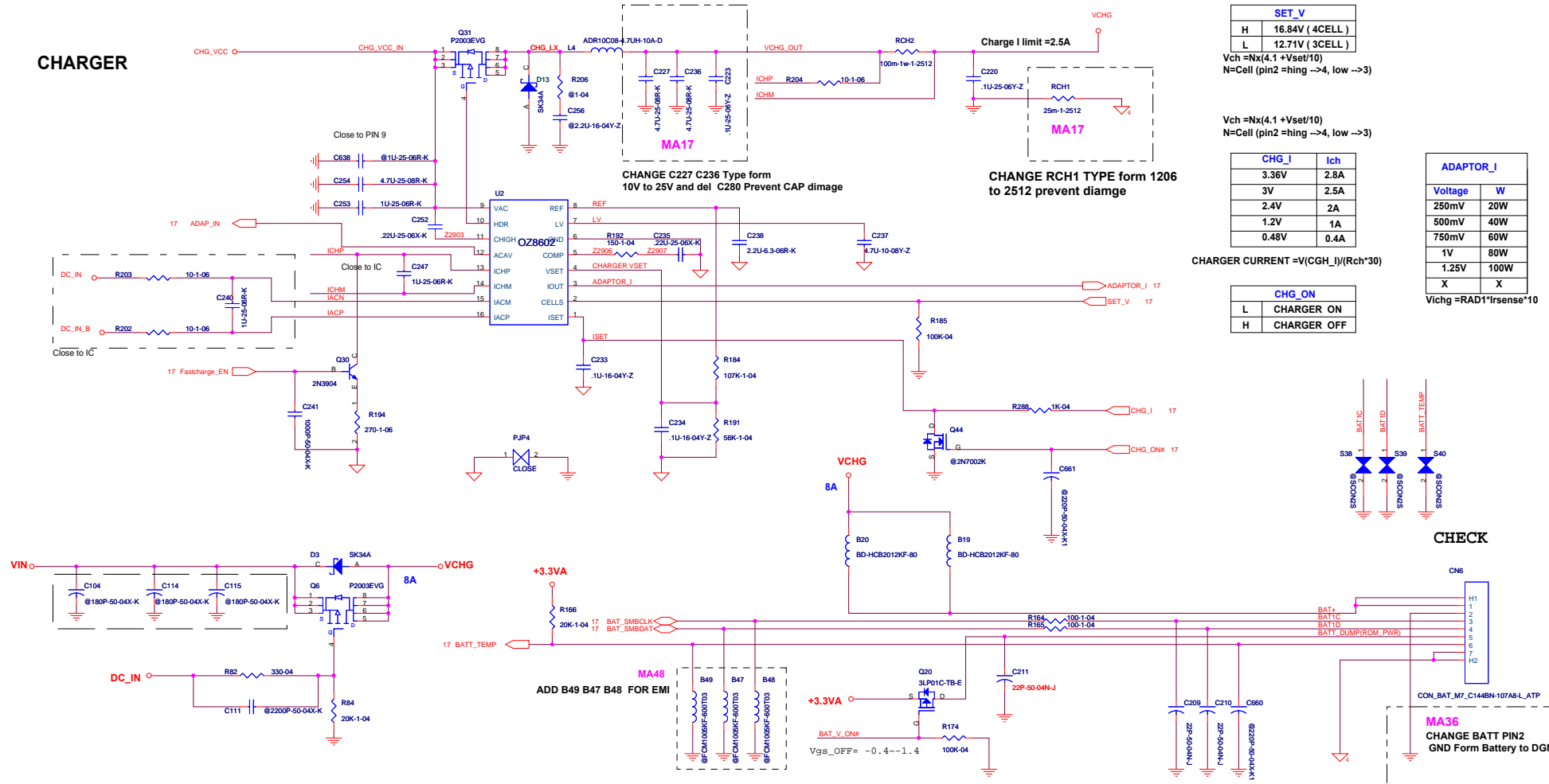


**Output Voltage = [ Vref x R2/(R1+R2) ] x 2**

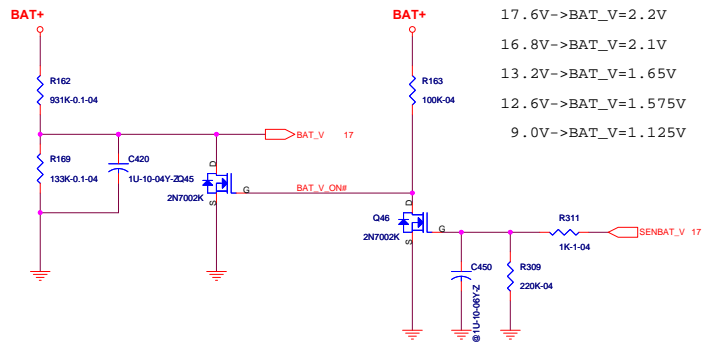


+5VA/ 8A

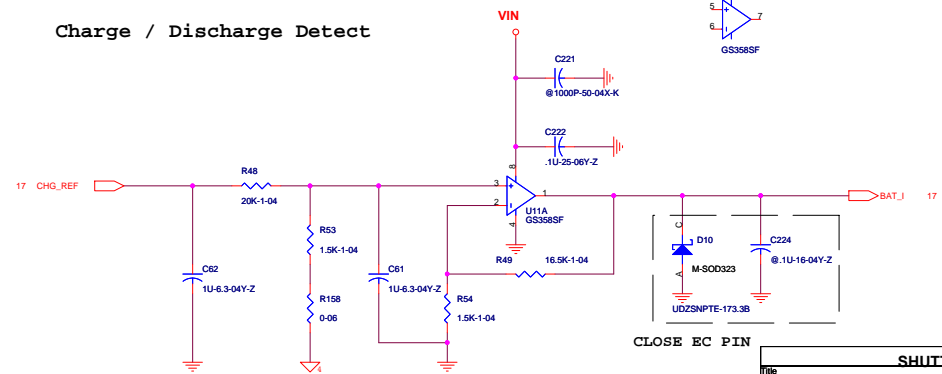
## CHARGER



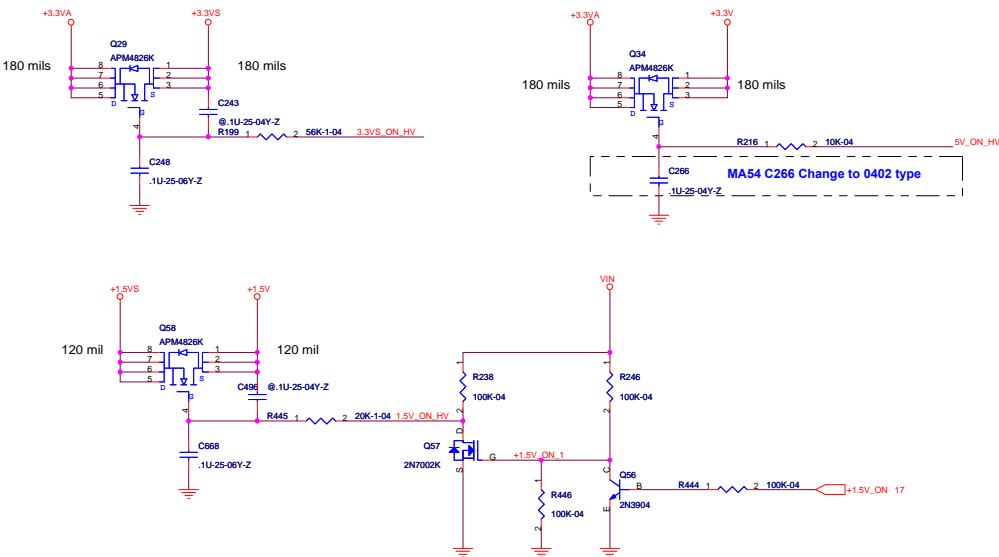
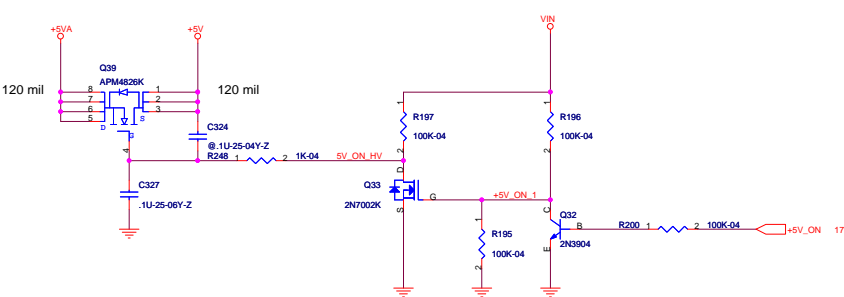
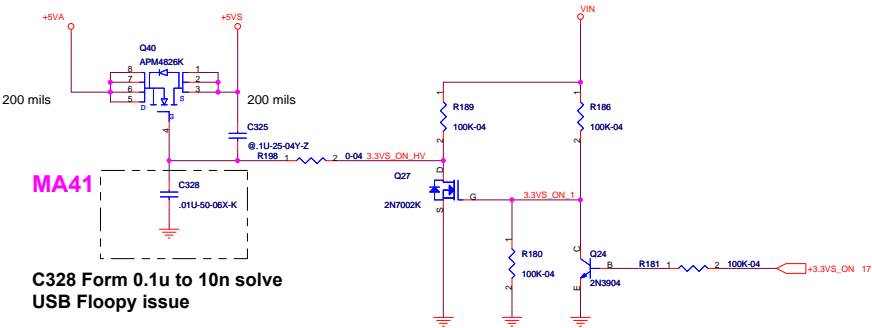
## Battery Voltage Detect



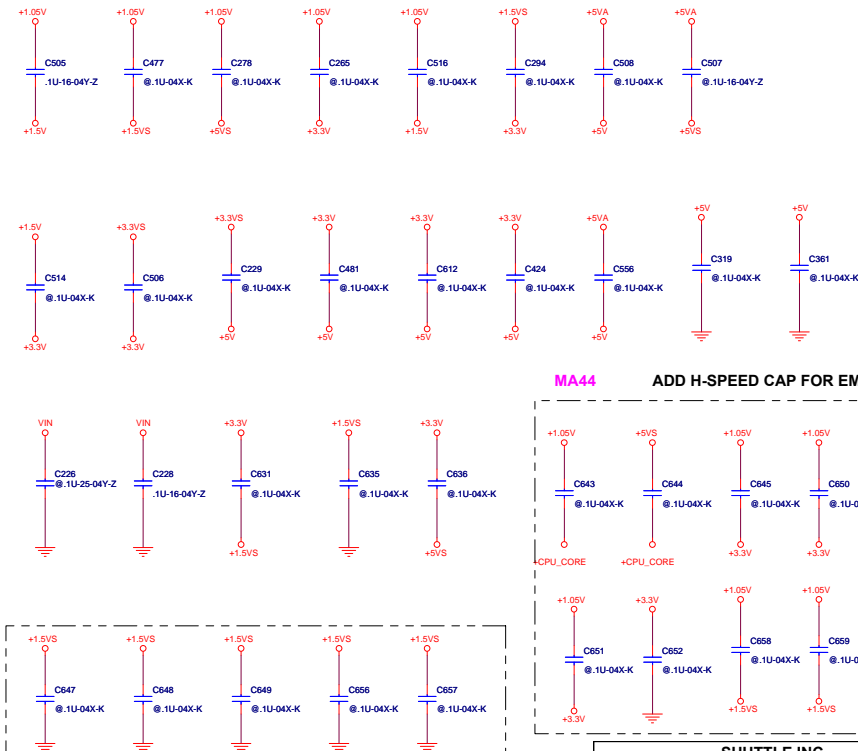
## Charge / Discharge Detect



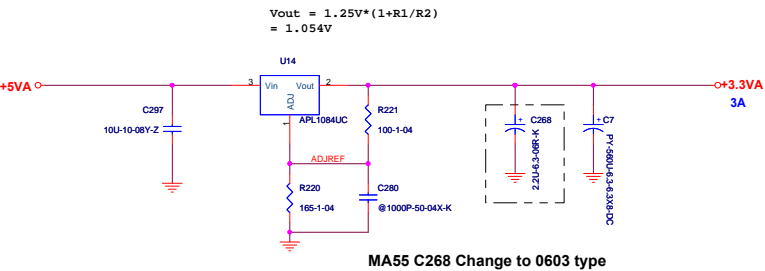
VCCSW



HIGH-SPEED CAP



LDO



RA to RB Modify list:

[illegible]