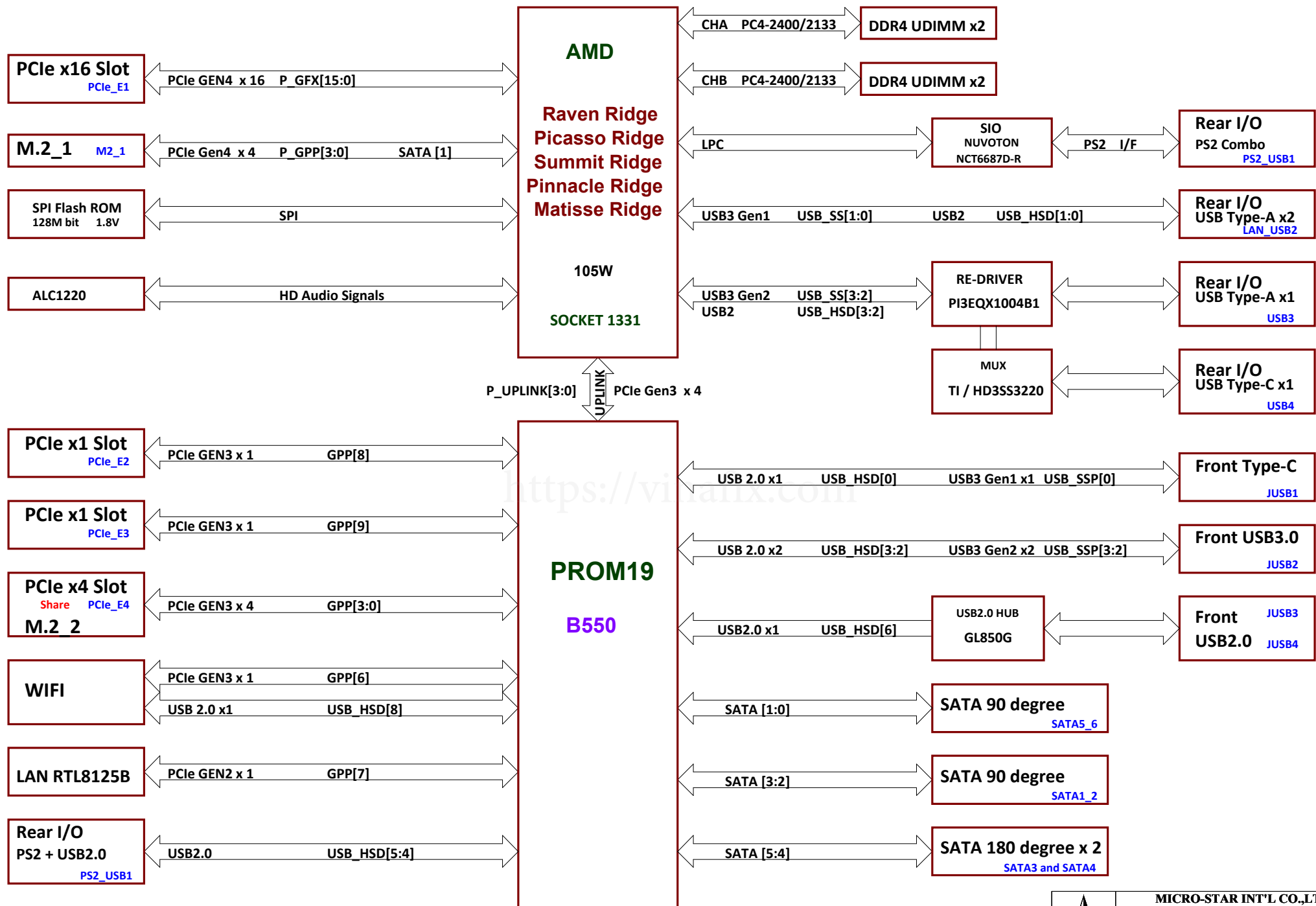


# AMD AM4 B550

M-ATX (243.84 X 243.84)

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Cloude Lai



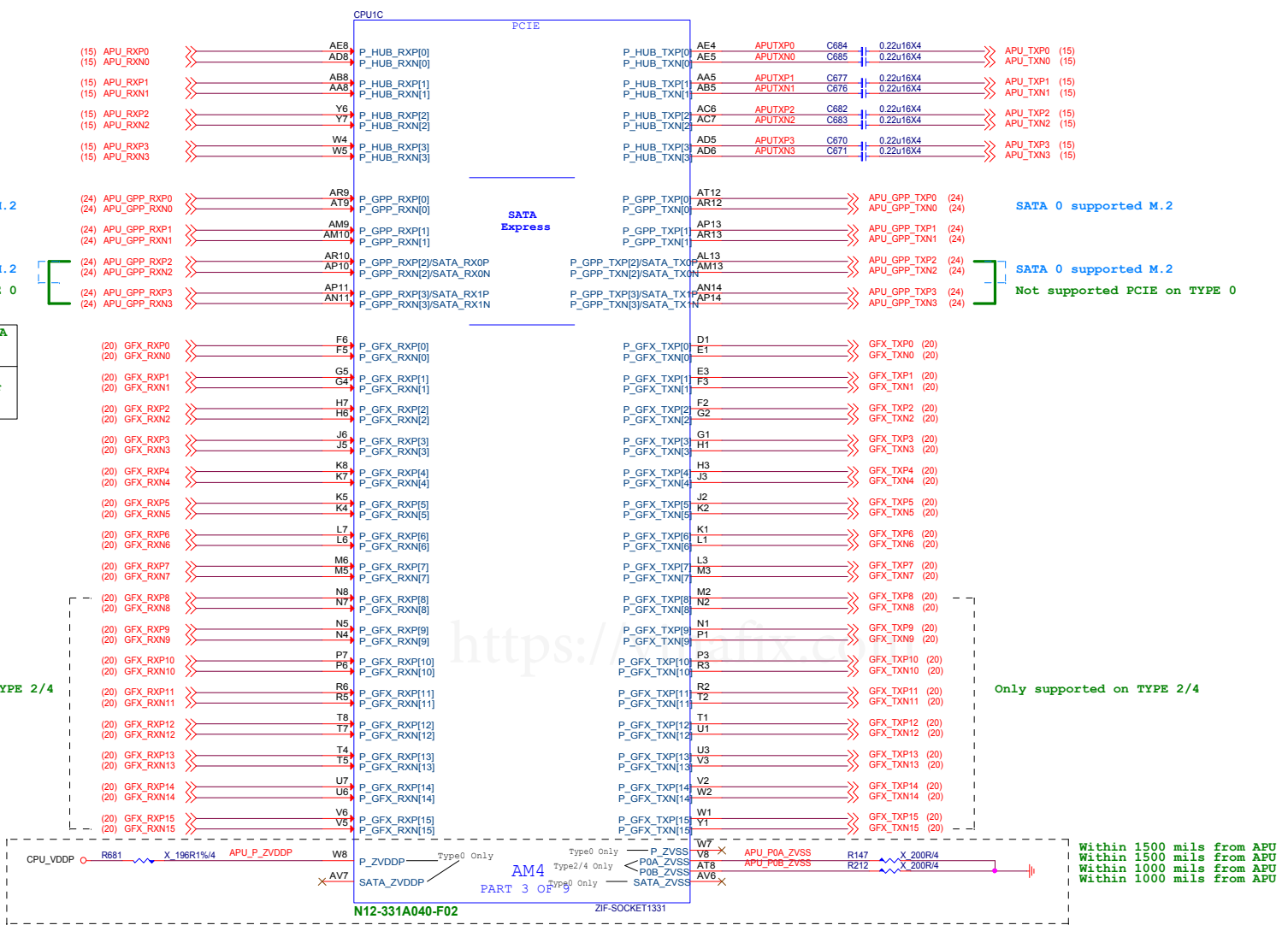
MICRO-STAR INT'L CO.,LTD		
MS-7C94		
Size Custom	Document Description Block Diagram	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 2 of 76	



TYPE 0/1	PCIE	SATA
	2	2
TYPE 2/3/4	2 or 4	2 or 0

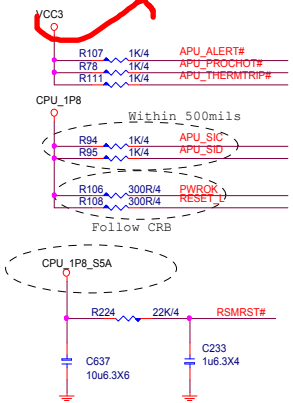
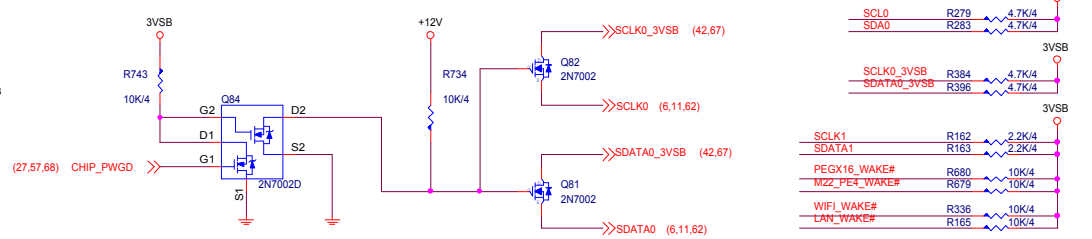
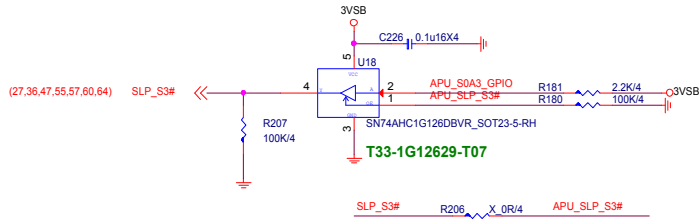
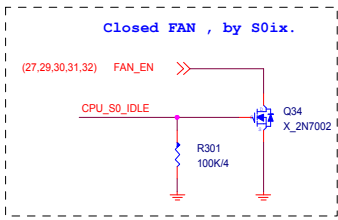
Only supported on TYPE 2/4

Within 1500 mils from APU  
Within 1000 mils from APU



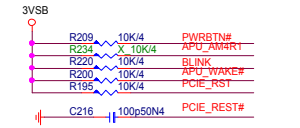
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<b>MS-7C94</b>		
Size Custom	Document Description <b>AM4 PCIE / SATAE</b>	Rev 1.0
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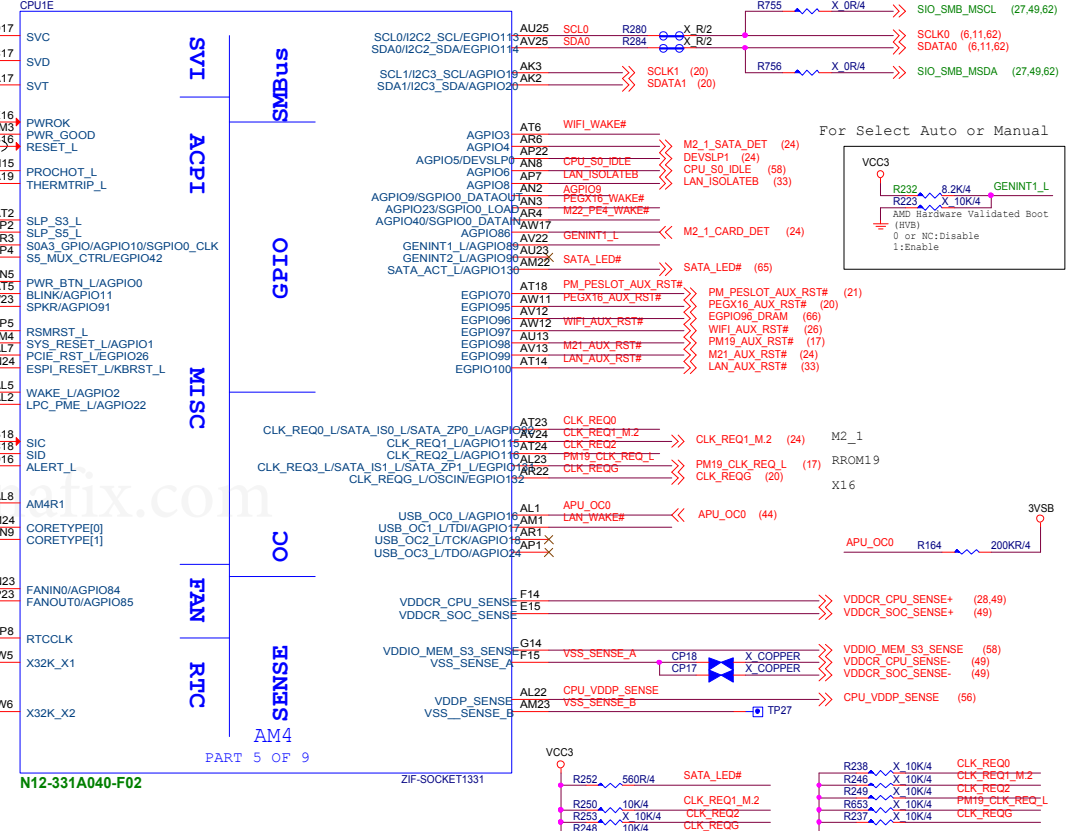
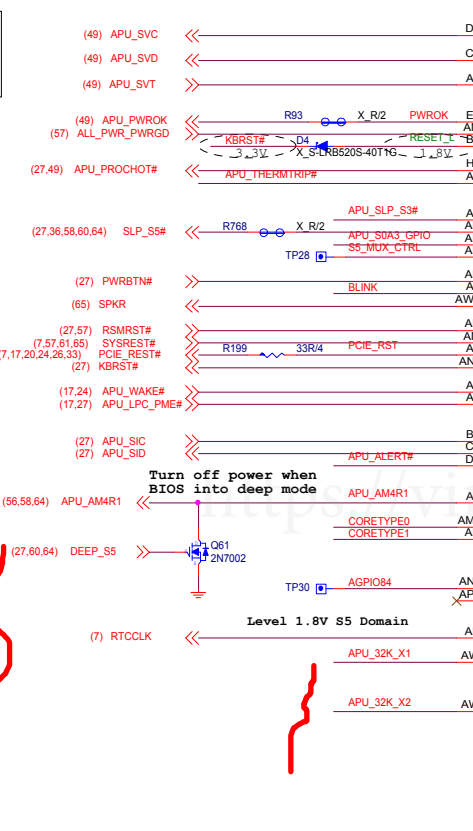
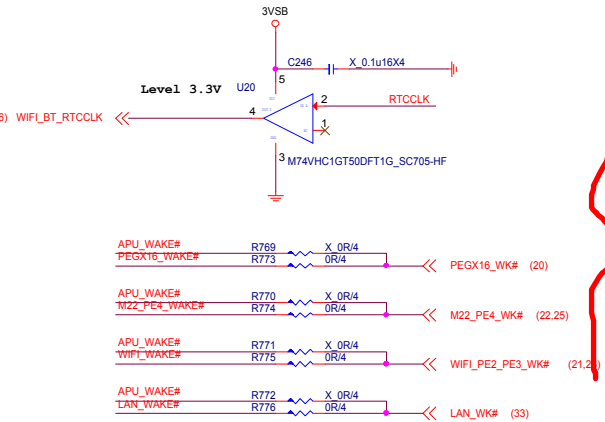
Add for HDT and close to PIN E16 & B16

(5) PWROK  
(5) RESET\_L



最新公板Qoqir\_RevD, 新增C2470, 請預留不上件

(5) APU\_PWROK



For Select Auto or Manual

VCC3

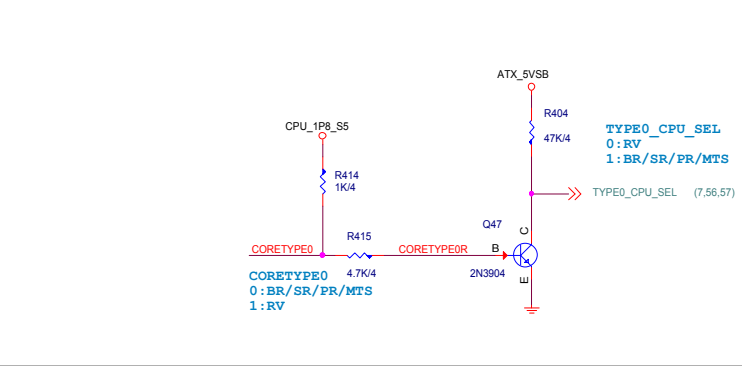
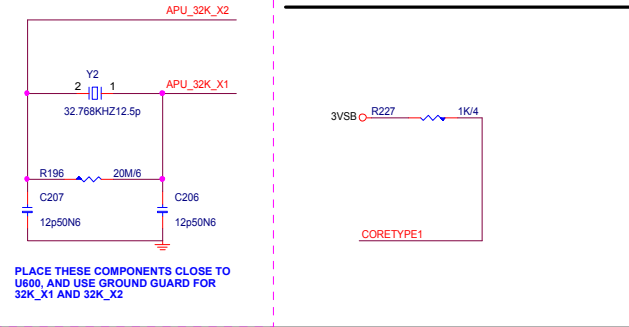
R232 X 8.2K/4

R223 X 10K/4

AWD Hardware Validated Boot (HWB)  
0 or NC: Disable  
1: Enable

Layout: Place x'tal within 1.5 inch of APU

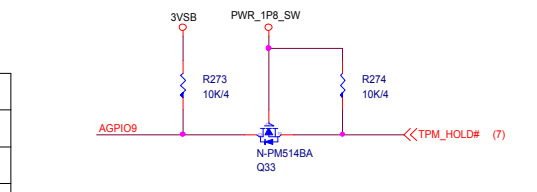
**AM4 CPU TYPE Circuit**



IB = (CPU\_1P8\_S5 - Vbe) / 5.7k  
(1.8 - 0.95) / 5.7k = 0.149mA

IC = (VCC5 - Vce) / 47k  
(5 - 0.2) / 47k = 0.102mA

CPU	TYPE	CORETYPE1	CORETYPE0
BR	0	0	0
NA	X	1	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	0

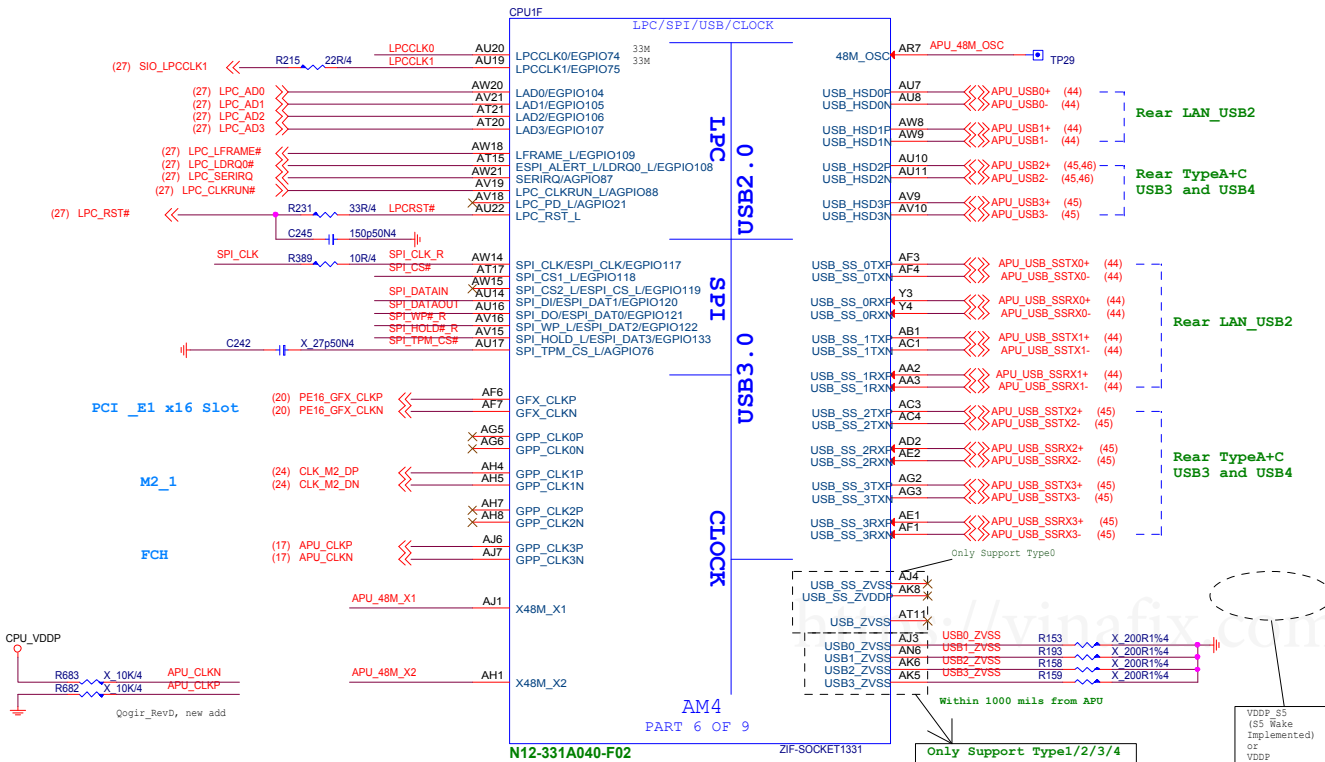
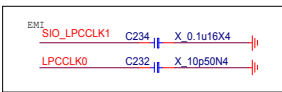


**MICRO-STAR INT'L CO.,LTD**

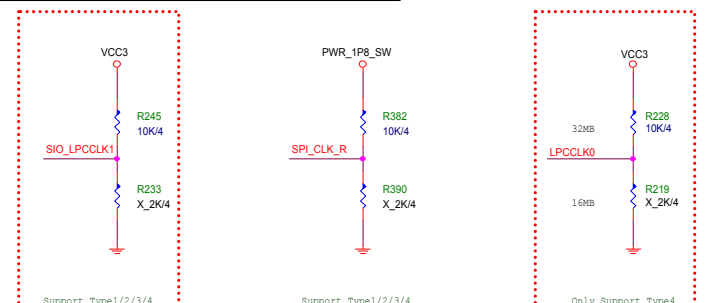
**MS-7C94**

Size	Document Description	Rev
Custom	AM4 SVI/ACPI/GPIO	1.0

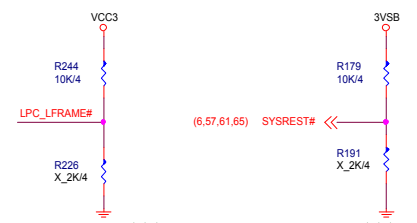
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# Strapping Options



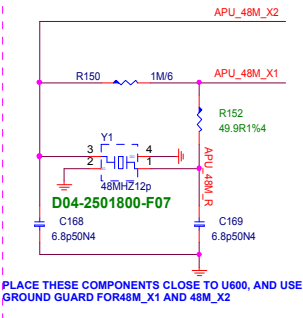
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator <b>(Default)</b>	Use 48Mhz crystal clock and generate both internal and external clocks. <b>(Default)</b>	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image. <b>(Default)</b>
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



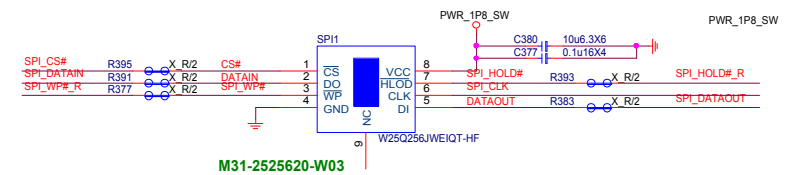
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic	SPI ROM <b>(Default)</b>	Normal reset mode <b>(Default)</b>
PULL LOW	<b>(Default)</b> Traditional Reset logic	LPC ROM	short reset mode

## SPI ROM (1.8V)

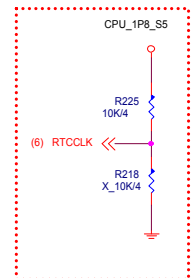
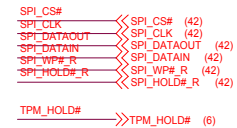
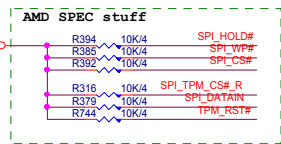
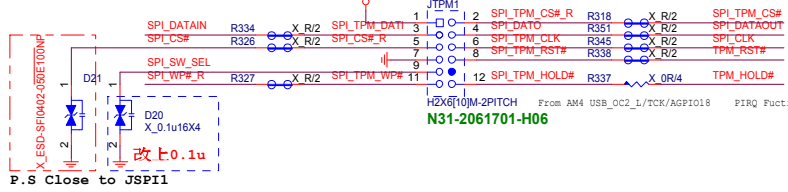
Layout: Place x'tal within 1.5 inch of APU



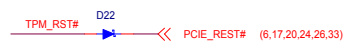
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 48M\_X1 AND 48M\_X2



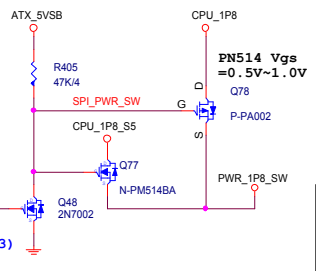
SPI CS# < 20pF  
D0G-0402510-SIO



	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock <b>(Default)</b>
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock



VDDP\_18 - Type 0, 2, and 4  
VDD\_18\_S5 - Type 1 and 3

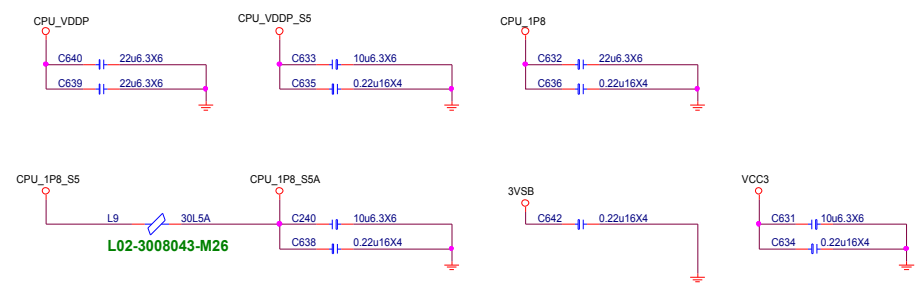
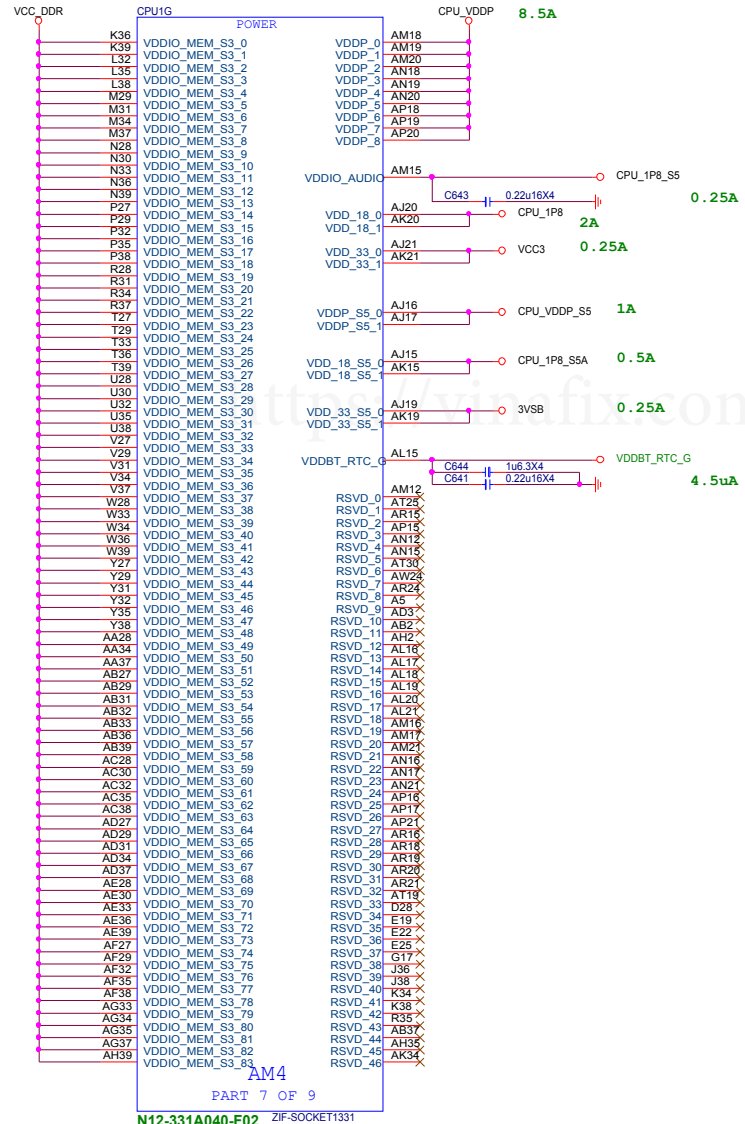
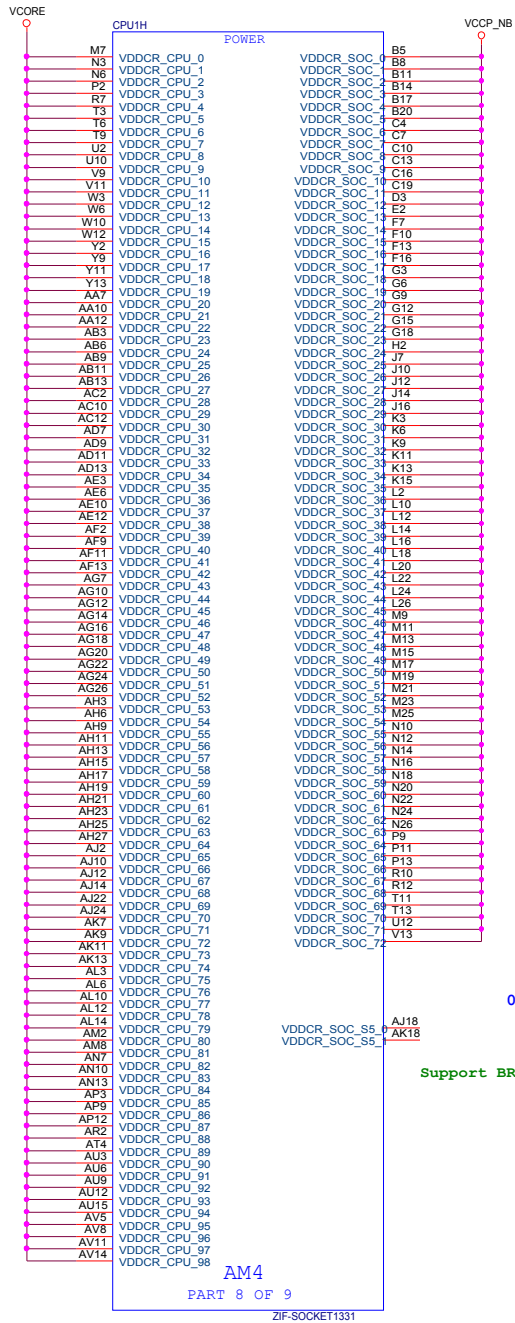


(6,56,57) TYPE0\_CPU\_SEL >>> Q48 2N7002  
TYPE0 CPU SEL:  
0: CPU\_1P8\_S5 (Type1,3)  
1: CPU\_1P8 (Type0,2,4)



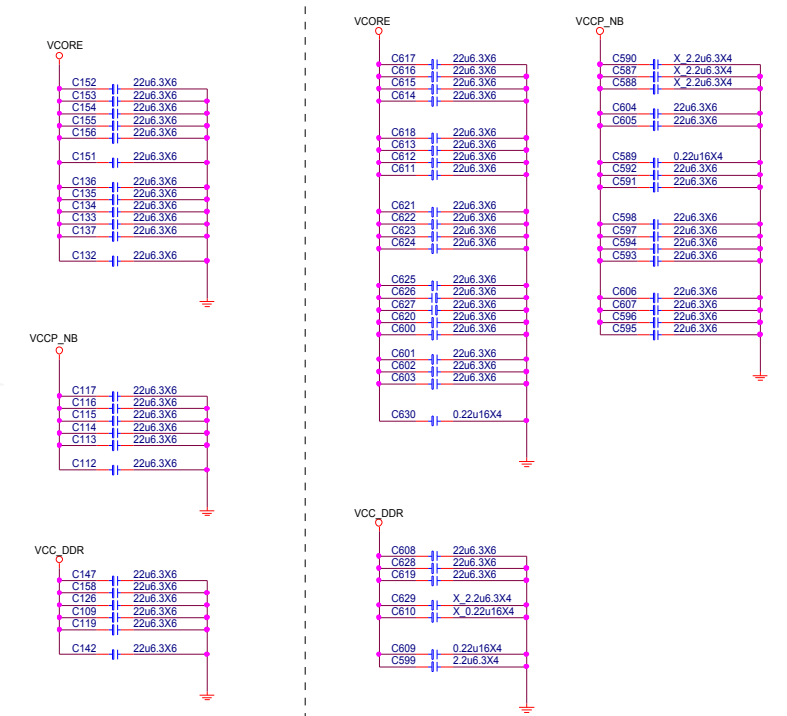
MICRO-STAR INT'L CO.,LTD		
MS-7C94		
Size Custom	Document Description	Rev 1.0
AM4 LPC / SPI / USB / CLK / STRAP		
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TOP and BOTTOM SIDE

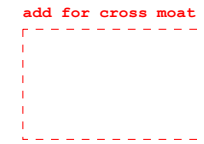


TOP CAVITY

BOTTOM CAVITY



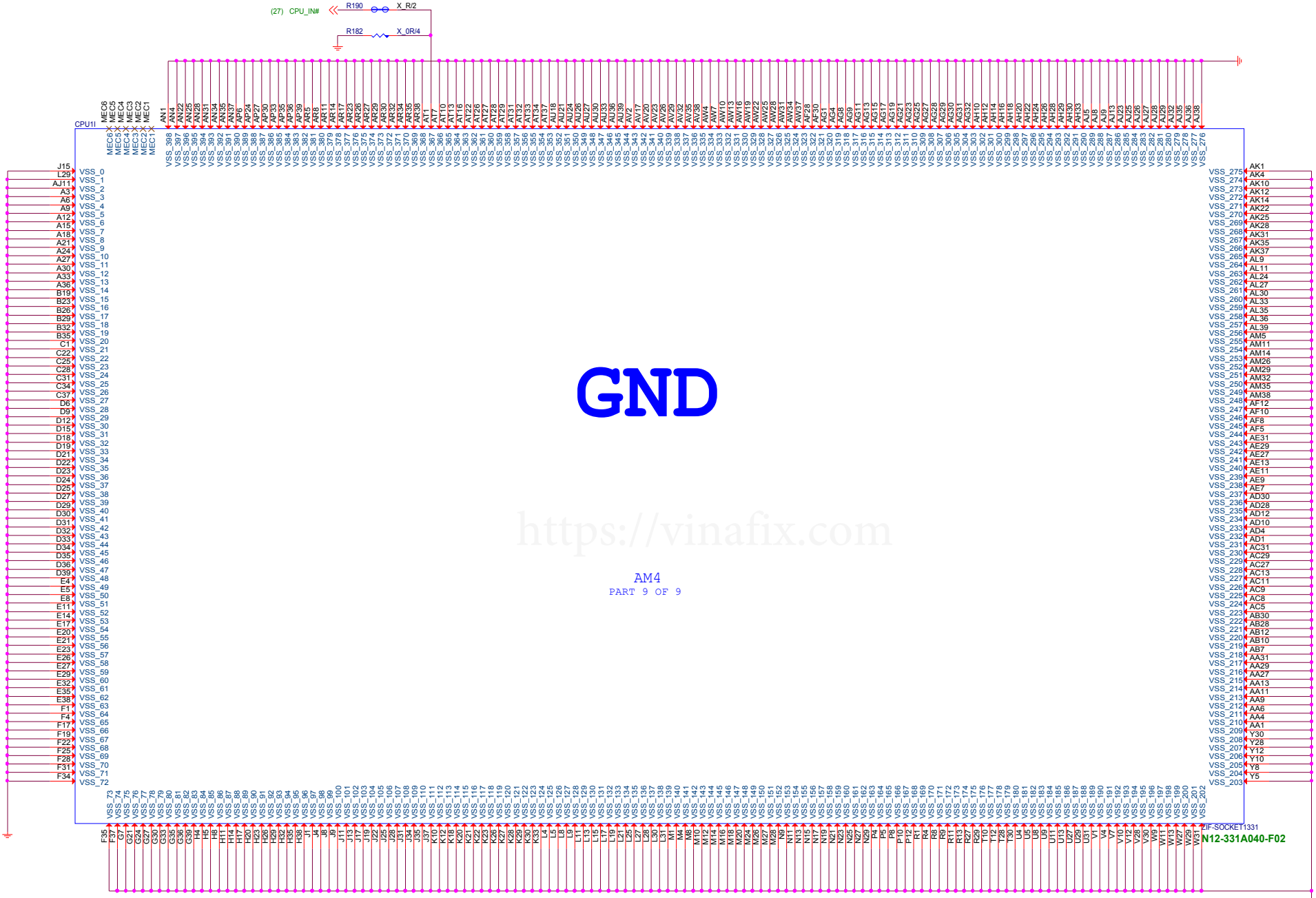
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<b>MS-7C94</b>		
Size	Document Description	Rev
Custom	<b>AM4 Power / VDDIO_AUDIO</b>	1.0
Date: Tuesday, April 28, 2020		
Sheet	8	of 76




# GND

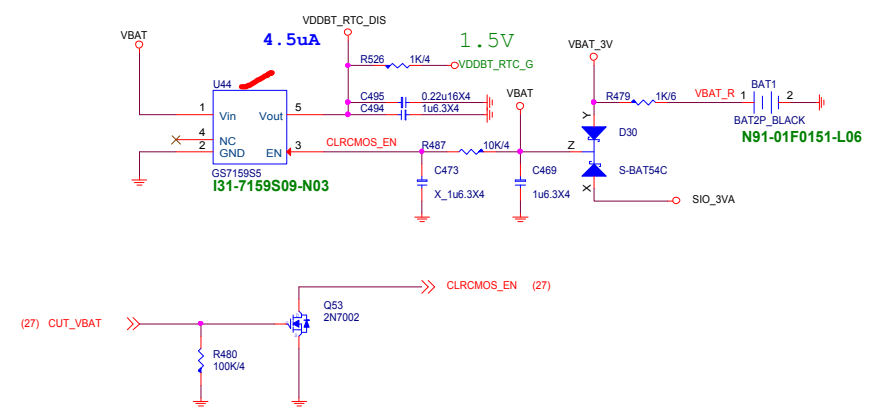
<https://vinafix.com>

AM4  
PART 9 OF 9



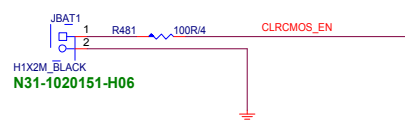
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			<b>MS-7C94</b>	
Size	Document Description		Rev	
Custom	AM4 GND		1.0	
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**RTC & Clear CMOS Circuit**

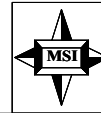


**RTC Backup**

**Clear CMOS button**

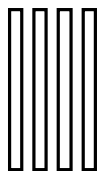


<https://vinafix.com>

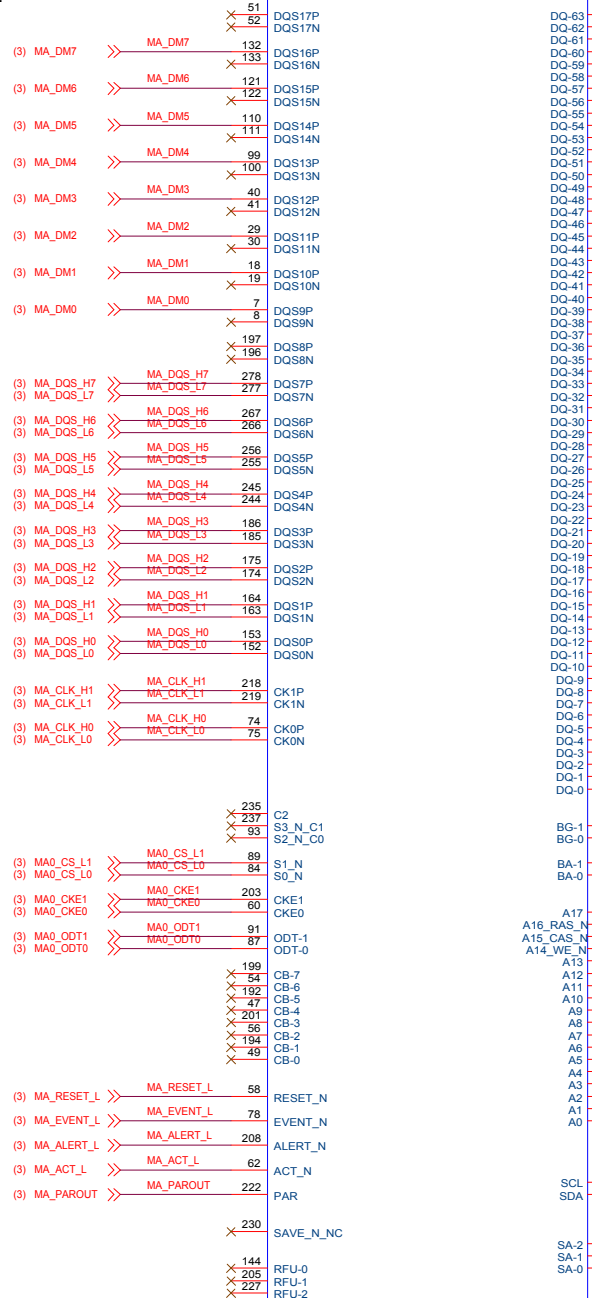


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>RTC / CMOS</b>	Rev 1.0
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A1 A2 B1 B2

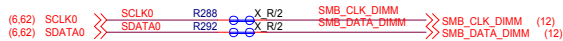


DIMMA1A

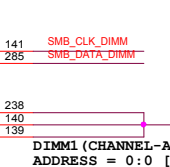
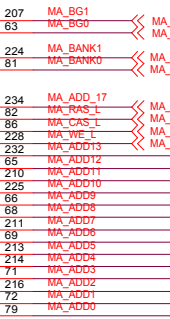
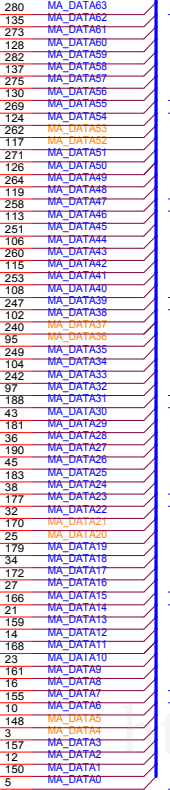


DDR4-288P\_BLACK-RH-9  
N13-2881271-L06

AVL: N13-2880441-F02

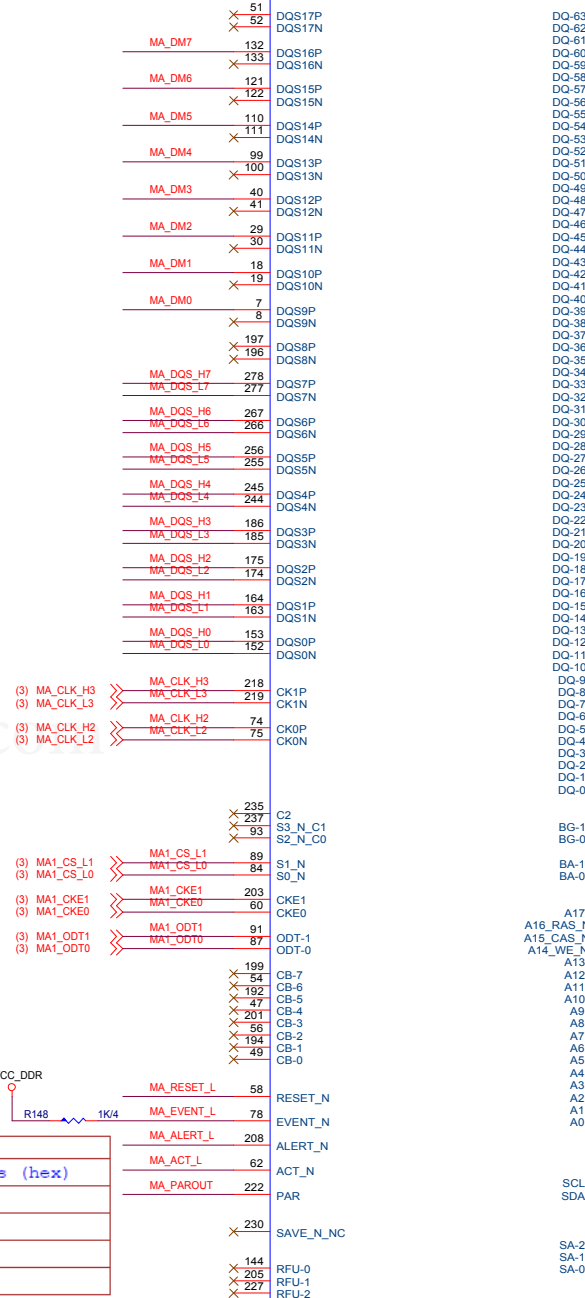


<< MA\_DATA[63..0] (3,11)



SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

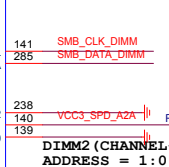
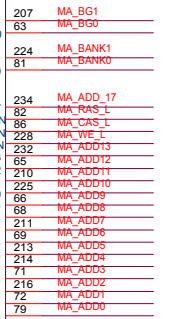
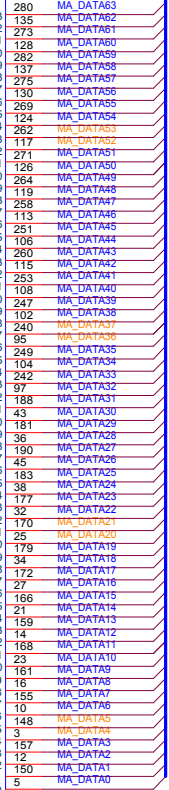
DIMMA2A



DDR4-288P\_BLACK-RH-9  
N13-2881271-L06

AVL: N13-2880441-F02

<< MA\_DATA[63..0] (3,11)

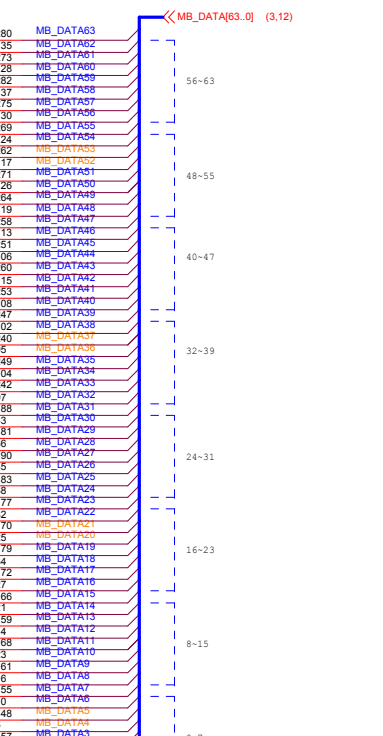
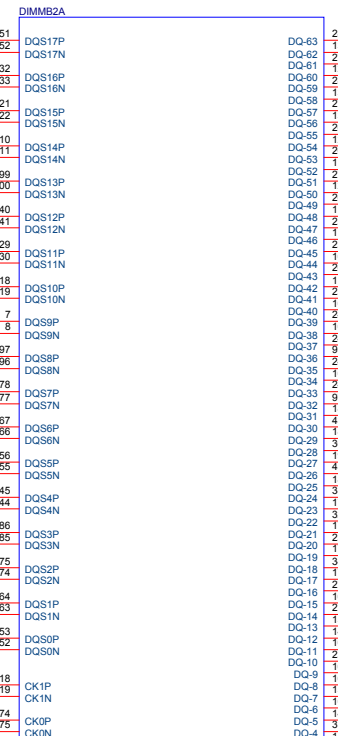
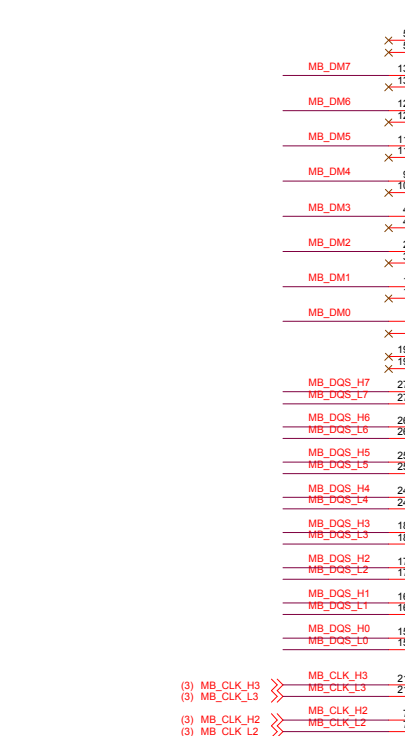
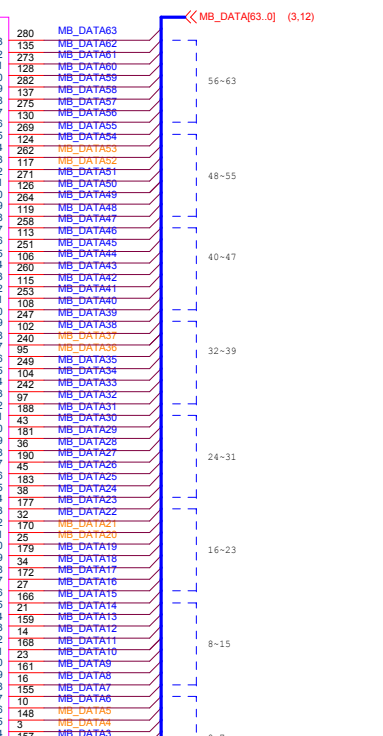
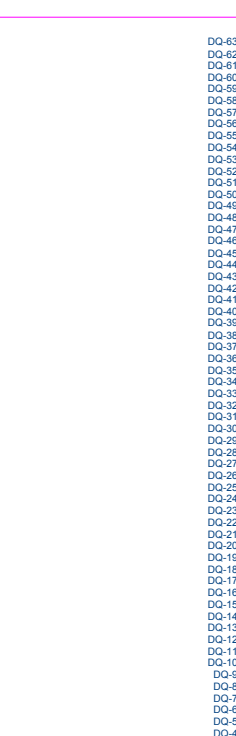
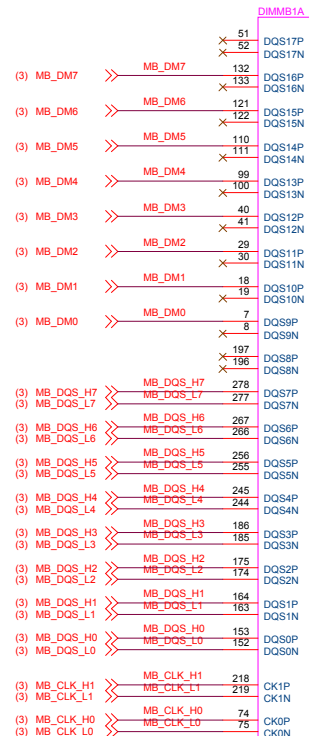
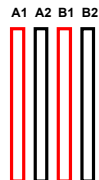


DDR4-288P\_BLACK-RH-9  
N13-2881271-L06

AVL: N13-2880441-F02



MICRO-STAR INT'L CO.,LTD		
MS-7C94		
Size	Document Description	Rev
Custom	DDR4 - DIMM CH-A	1.0
Date: Tuesday, April 28, 2020	Sheet 11 of 76	



**DIMM3 (CHANNEL-B) -A2**  
ADDRESS = 0:1 [SA1:SA0]

**DIMM4 (CHANNEL-B) -A6**  
ADDRESS = 1:1 [SA1:SA0]

DDR4-288P\_BLACK-RH-9  
N13-2881271-L06

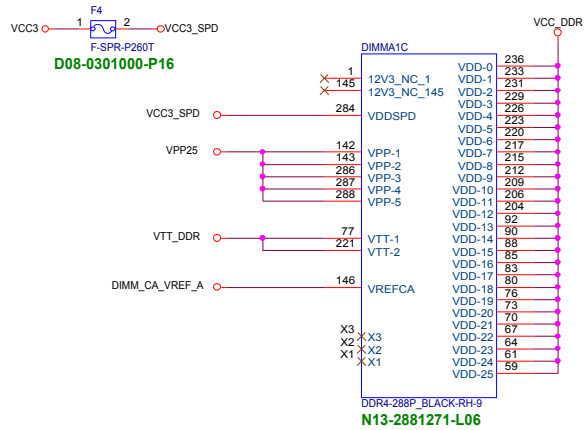
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N13-2881271-L06

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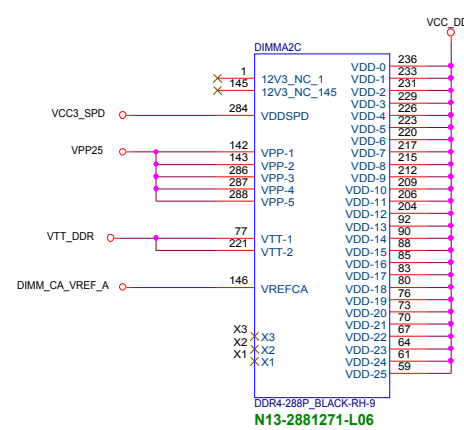


MICRO-STAR INT'L CO.,LTD		
<b>MS-7C94</b>		
Size Custom	Document Description	Rev 1.0
<b>DDR4 - DIMM CH-B</b>		
Date: Tuesday, April 28, 2020	Sheet 12	of 76

av1:D08-0301100-B07

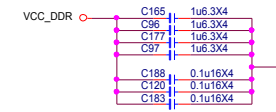
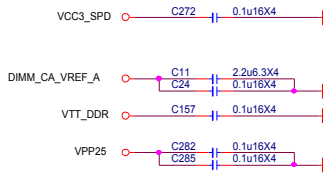
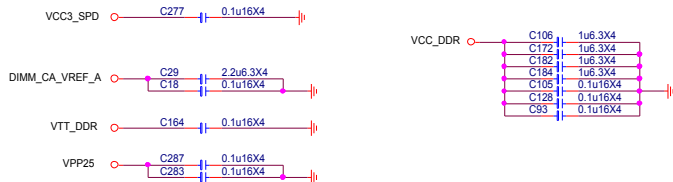
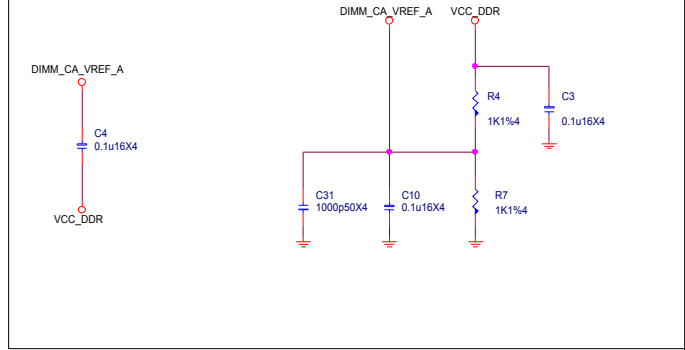


DIMM SLOT PN BY SPEC

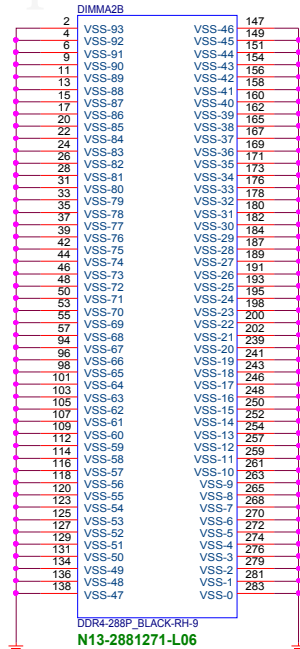
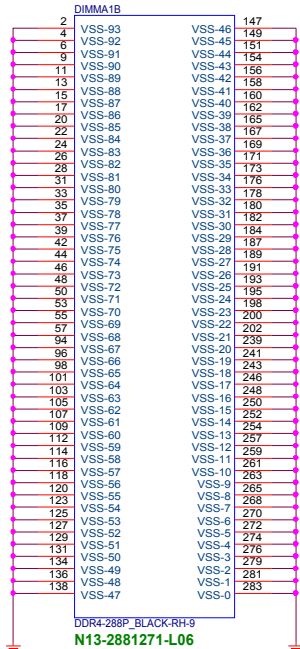


DDR VREF

(place resistors close to DIMMs)



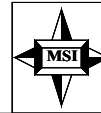
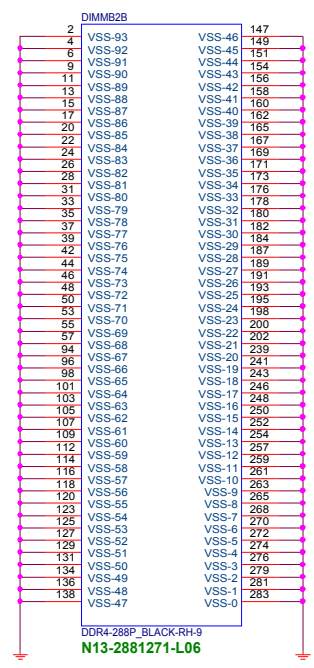
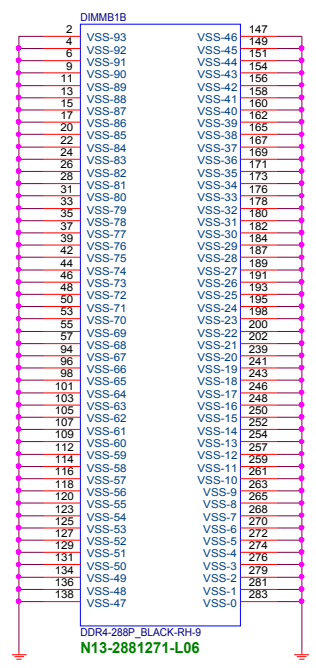
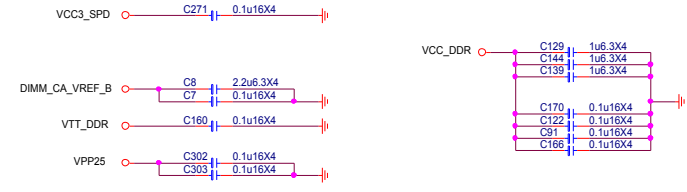
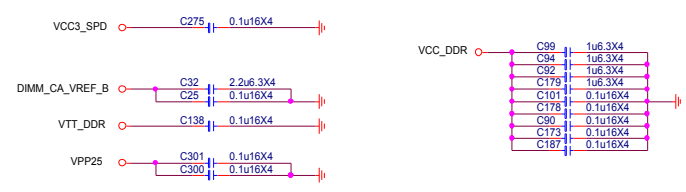
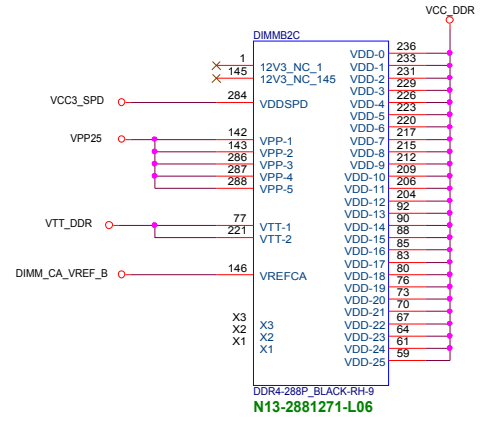
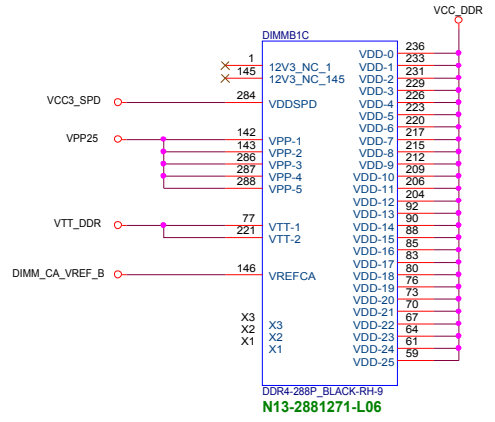
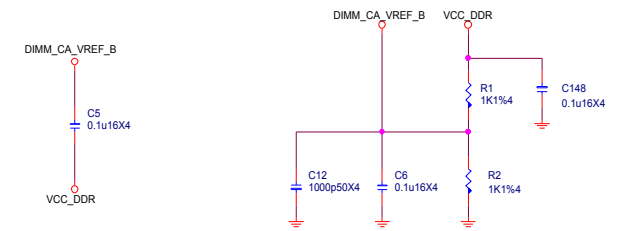
<https://vinafix.com>



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>DDR4 - POWER/GND-1</b>	Rev 1.0
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# DDR VREF

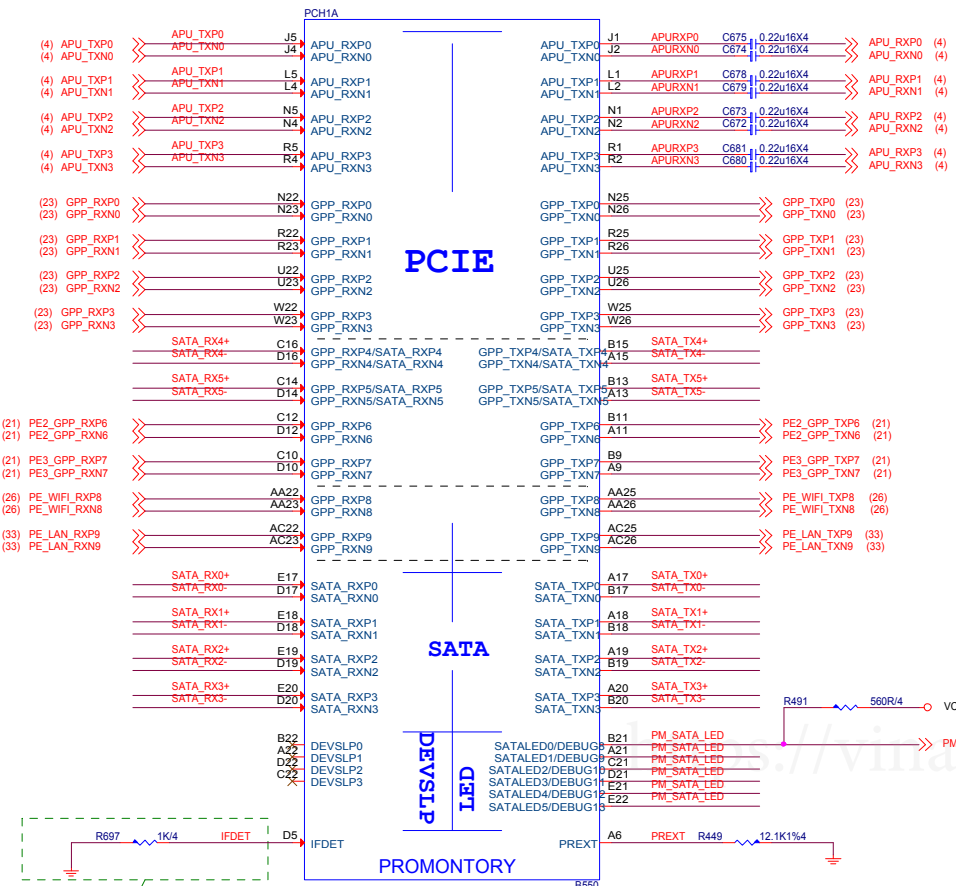
(place resistors close to DIMMs)



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>DDR4 - POWER/GND-2</b>	Rev 1.0
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M2 2  
PCI\_E4

SATA5  
SATA6  
PCI\_E2  
PCI\_E3  
WIFI+BT  
2.5G LAN

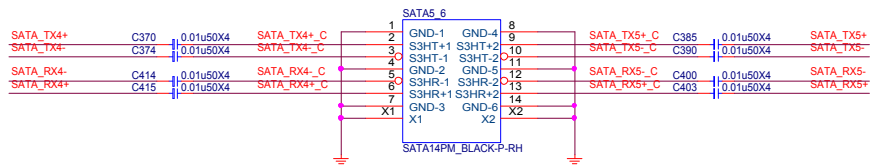


PCIE/SATA combo mode select (GPP[5:4]/SATA[5:4])  
0:SATA Mode  
1:PCIE Mode

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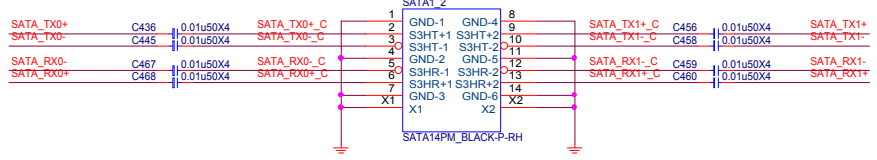
### SATA Connector

#### SATA1\_2



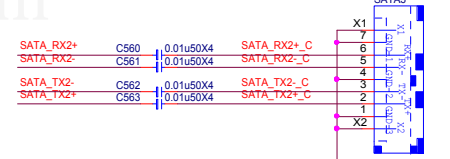
AVL:N5N-14M0201-L06

#### SATA3\_4



AVL:N5N-14M0201-L06

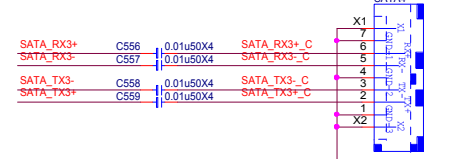
#### SATA5



N5N-07M2441-L06

AVL:N5N-14M0201-L06

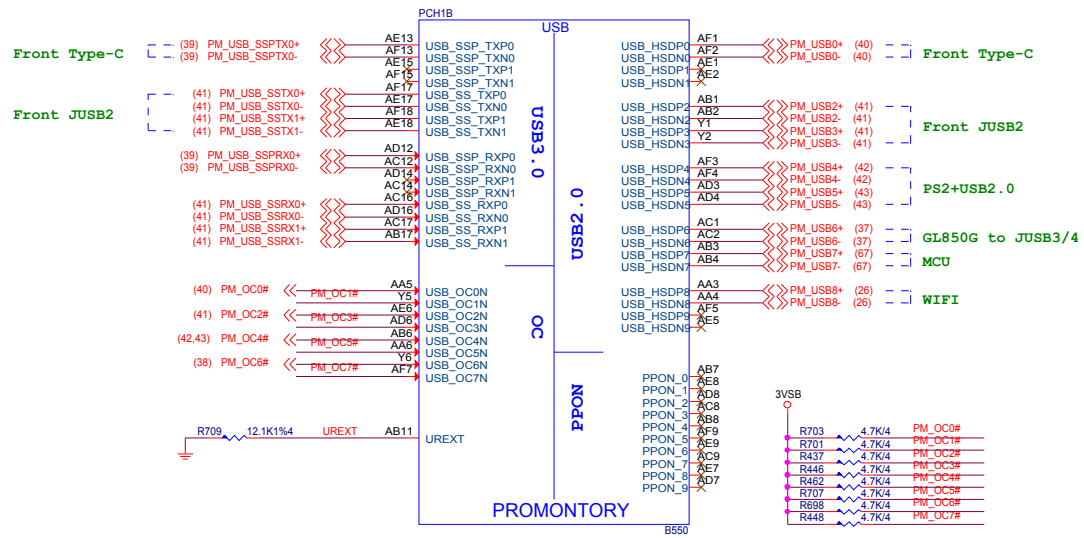
#### SATA6



N5N-07M2441-L06

AVL:N5N-14M0201-L06

<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>Premium - PCIE/SATA</b>	Rev 1.0
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**USB mapping**

USB\_SSP\_TX/RX[0] + USB\_HSDP/N[0] + USB\_OC0N  
 USB\_SSP\_TX/RX[1] + USB\_HSDP/N[1] + USB\_OC1N

USB\_SS\_TX/RX[0] + USB\_HSDP/N[2] + USB\_OC2N  
 USB\_SS\_TX/RX[1] + USB\_HSDP/N[3] + USB\_OC3N

USB\_HSDP/N[4] + USB\_OC4N

USB\_HSDP/N[5] + USB\_OC5N

USB\_HSDP/N[6] + USB\_OC6N

USB\_HSDP/N[7] + USB\_OC7N

USB\_HSDP/N[8] + USB\_OC7N

USB\_HSDP/N[9] + USB\_OC7N

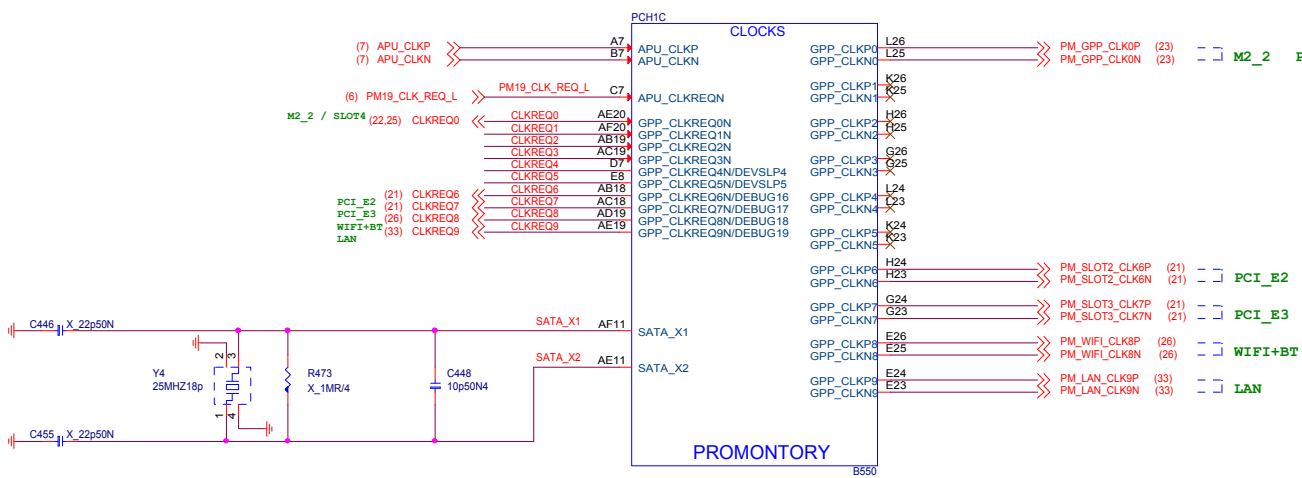
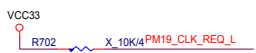
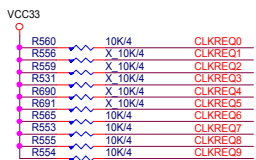
<https://vinafix.com>



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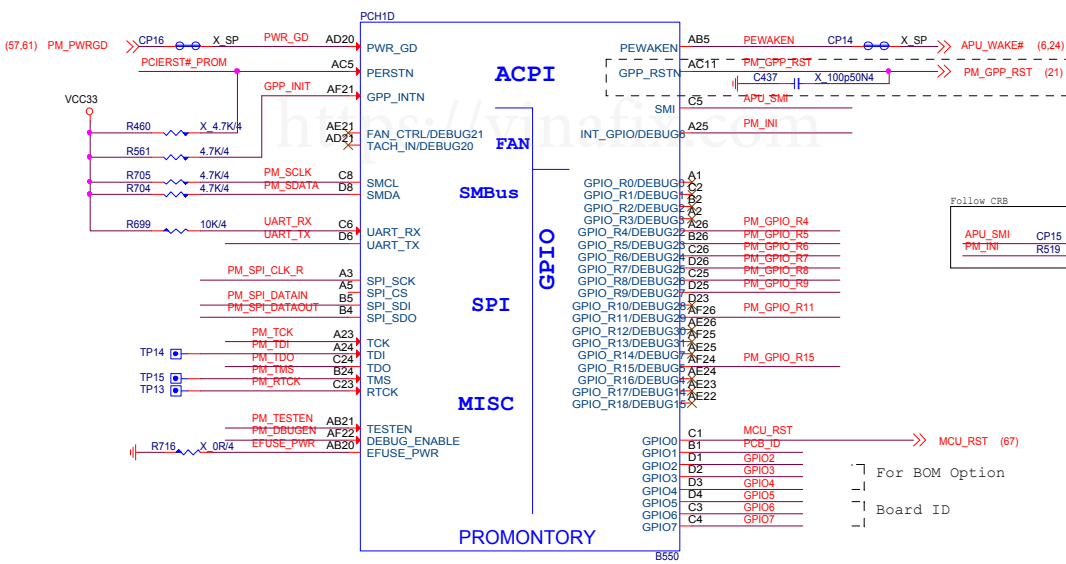
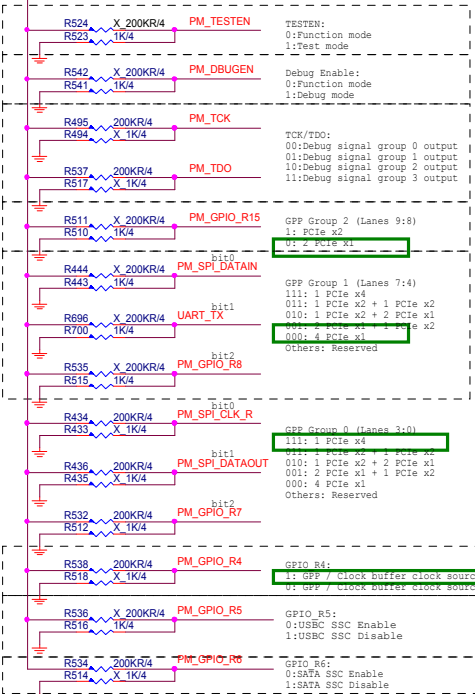
**MS-7C94**

Size	Document Description	Rev
Custom	Premium - USB/OC	1.0
Date:	Tuesday, April 28, 2020	Sheet 16 of 76

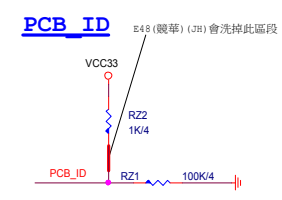
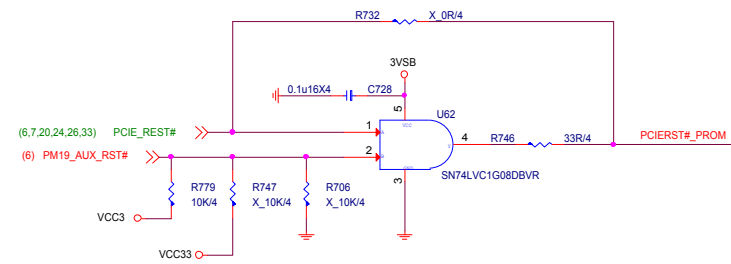
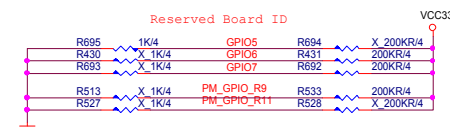
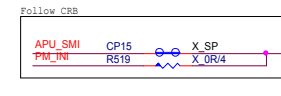


### Strap Information

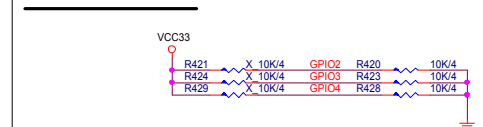
Vih = 2V Voh = 2.4V  
 Vil = 0.8V Vol = 0.4V



Co-lay GPP\_RSTN Reset for meet FCH sequence. See 55553.



### BOM OPTION



	WIFI	NON-WIFI
GPIO2	0	1
GPIO3	0	0
GPIO4	0	0

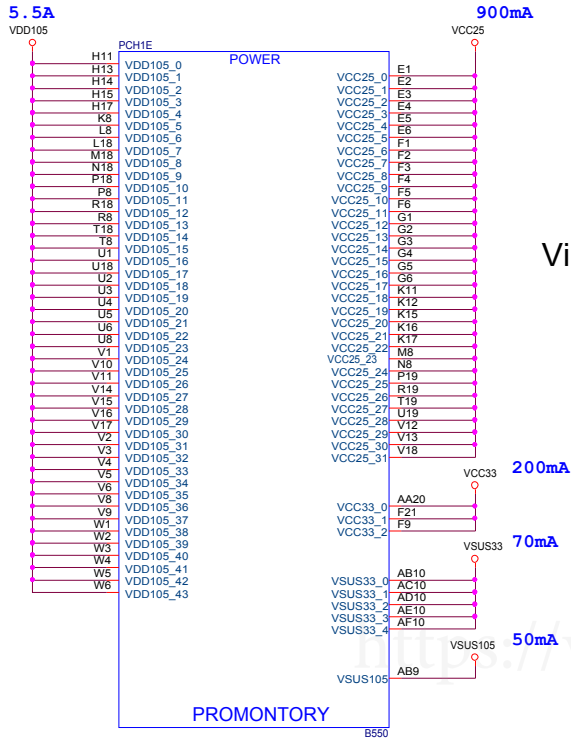
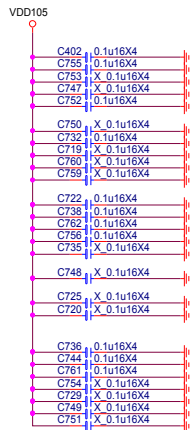
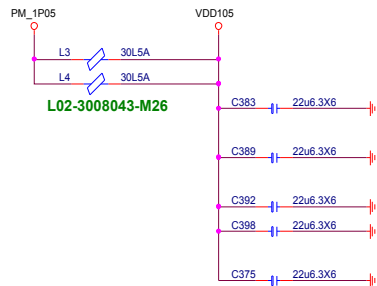
**MICRO-STAR INT'L CO.,LTD**

**MS-7C94**

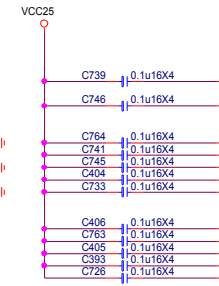
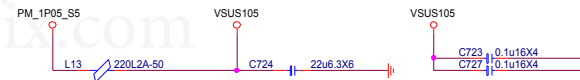
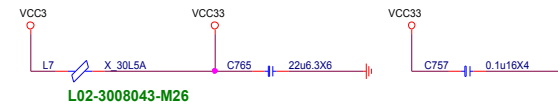
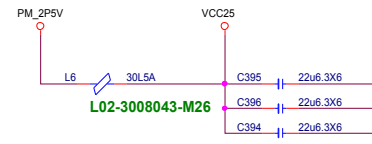
Premium - CLK/ACPI/GPIO

Size Custom Document Description Rev 1.0

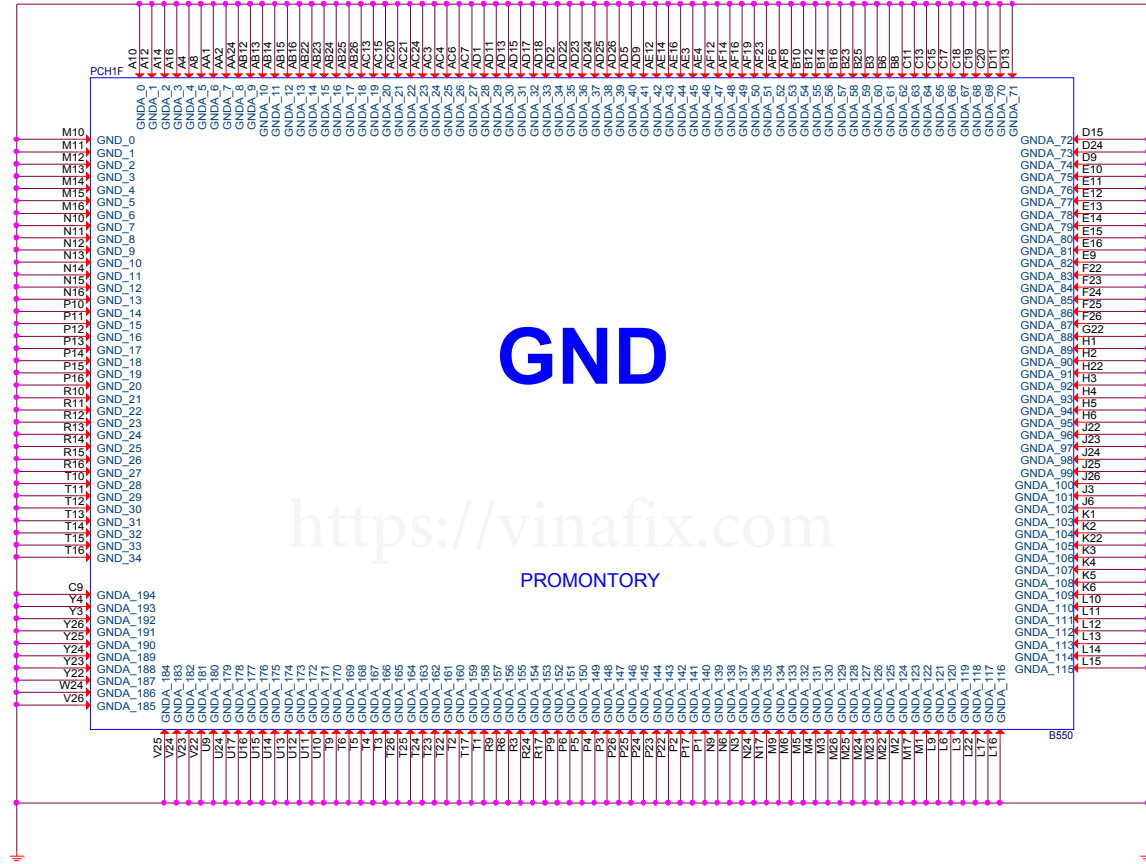
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<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
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Custom	Premium - Power	1.0
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**GND**

<https://vinafix.com>

PROMONTORY



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MS-7C94

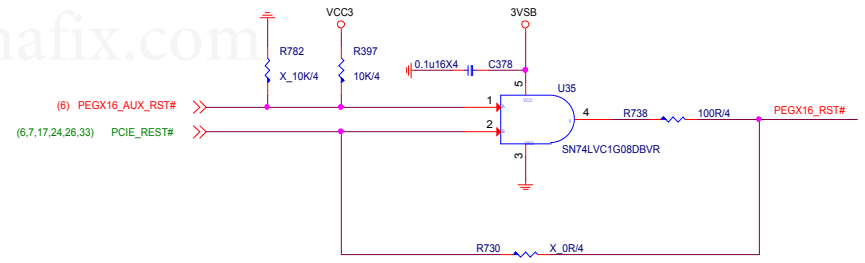
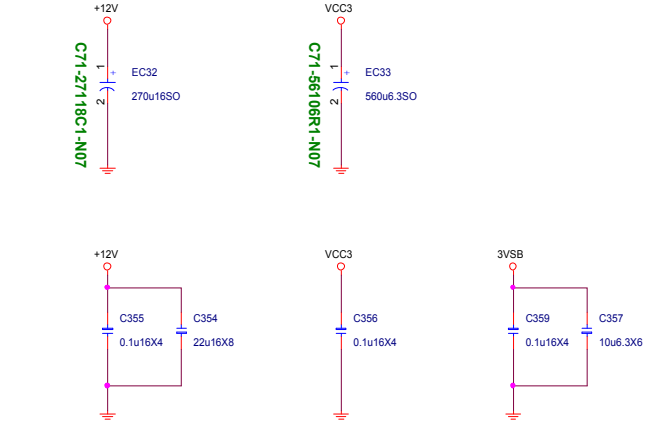
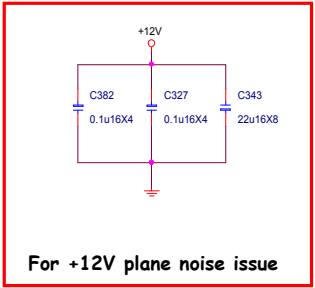
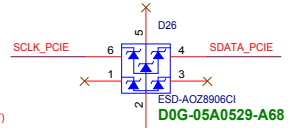
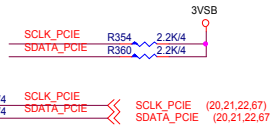
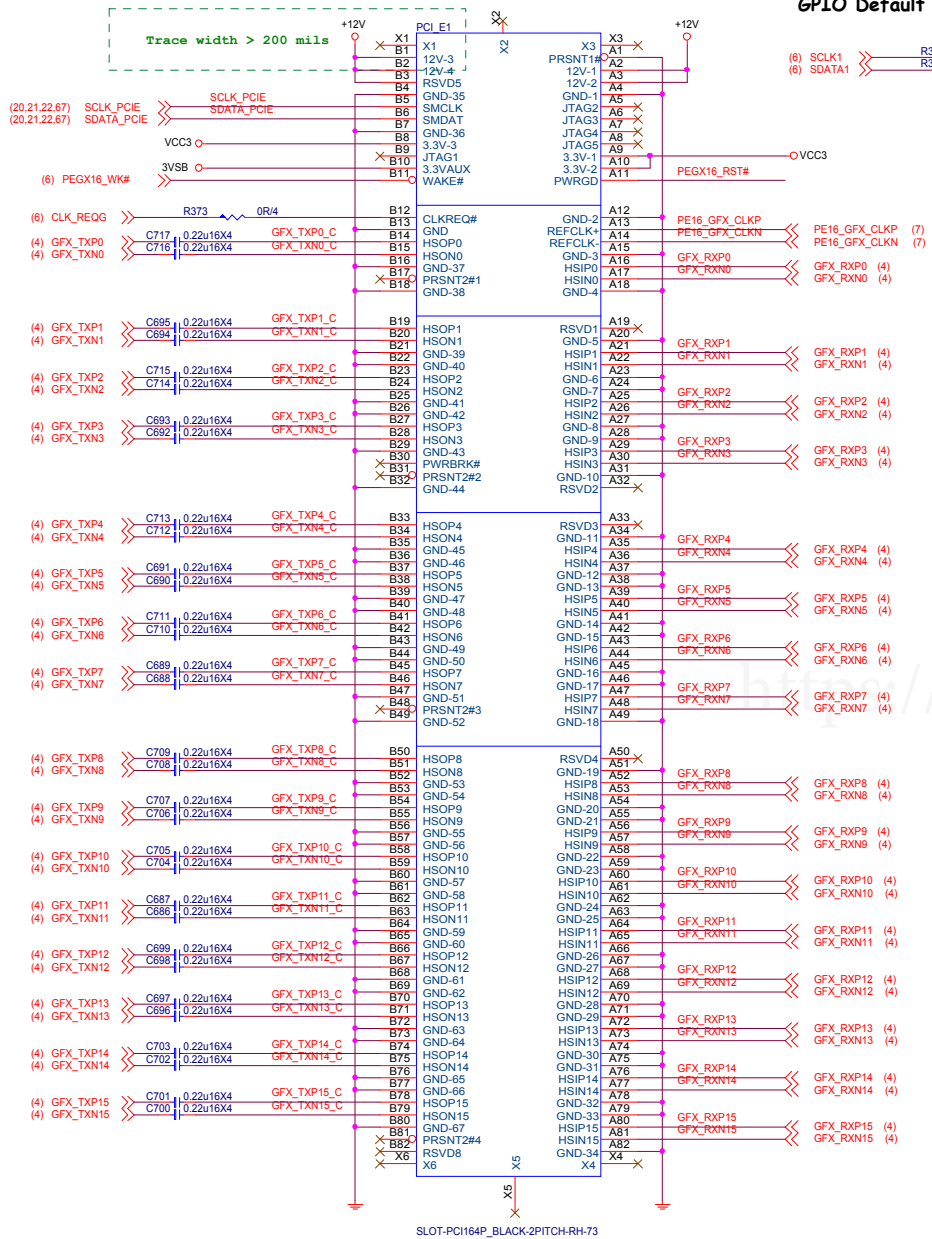
Size Custom Document Description Premium - GND Rev 1.0

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# PCI EXPRESS x16 Slot

## PCI\_E1

### SMB\_SEL GPIO Default High



PCI Express x16 Slot	
+12V	- 5.5 A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA

**MICRO-STAR INT'L CO.,LTD**

**MS-7C94**

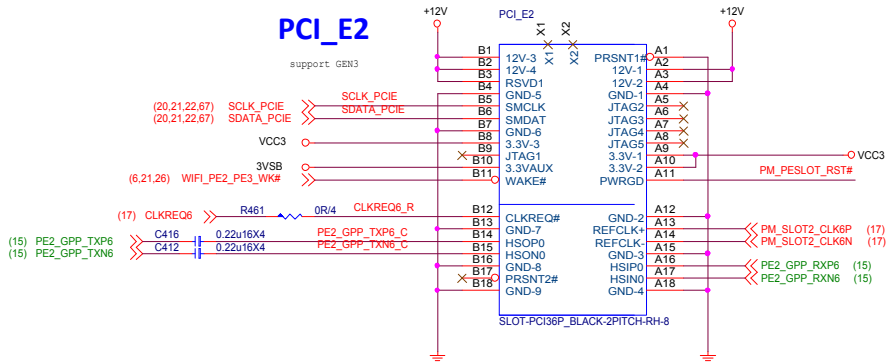
Size Custom Document Description **PCI\_E1 (X16)** Rev 1.0

Date: Tuesday, April 28, 2020 Sheet 20 of 76

# PCI EXPRESS X1 SLOT

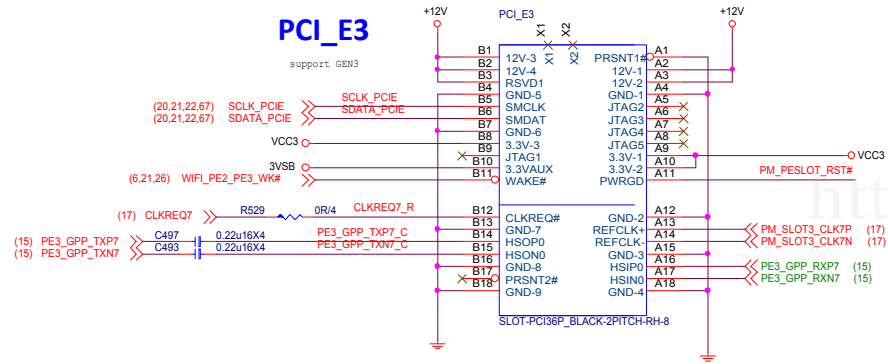
## PCI\_E2

support GEN3



## PCI\_E3

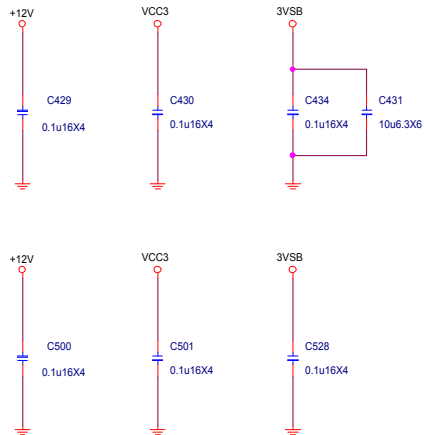
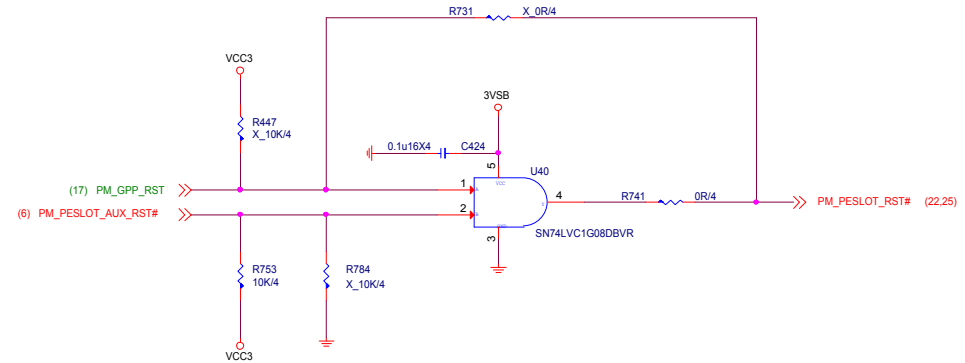
support GEN3



12V - 0.5A

VCC3 - 3A

3VSBV - 375mA



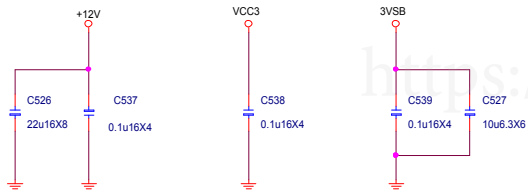
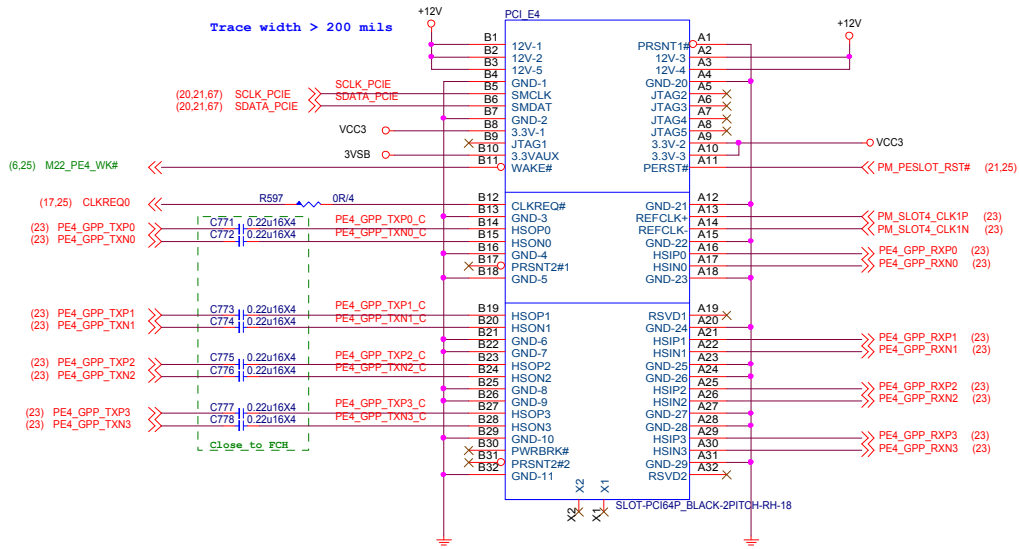
Vinafix.com

PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 20mA

	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7C94</b>		
Size Custom	Document Description <b>PCL E2 (X1) / PCL E3 (X1)</b>	Rev 1.0	
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# PCI EXPRESS x4 SLOT

# PCI\_E4 X4

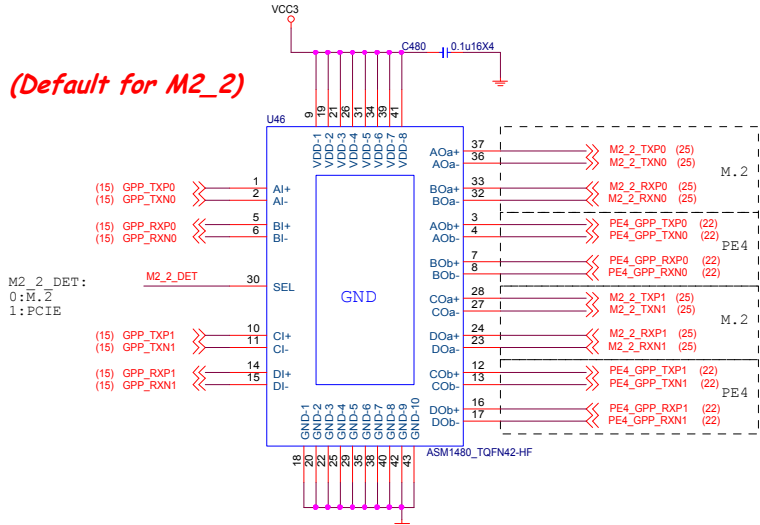


PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

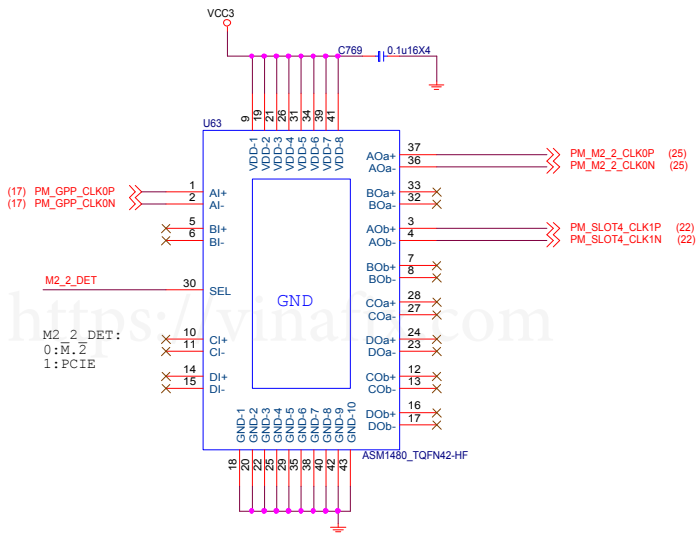
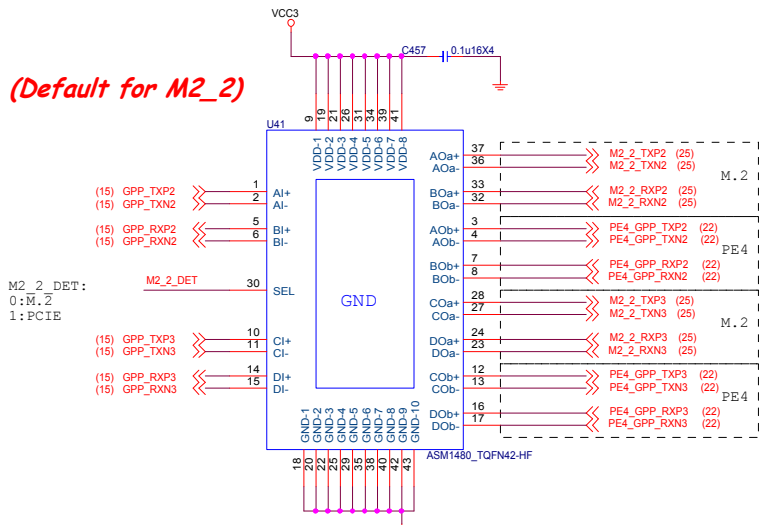
	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-7C94</b>	
Size Custom	Document Description <b>PCI_E4 (X4)</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 22 of 76	

# PCI E4 and M2 2 Switch

(Default for M2\_2)



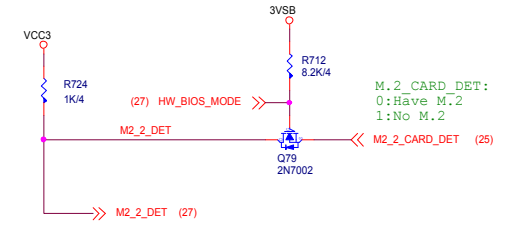
(Default for M2\_2)



Manufacture Control		Default PCIE_X4			
	AUTO Mode	PCIE X4	M.2 X4		
HW_BIOS_MODE	1	0	0		
M2_2_DET	input	1	0		

Device Detect **紅字為偵測PCIE或SATA device**

M2_2_DET					
		1	0		

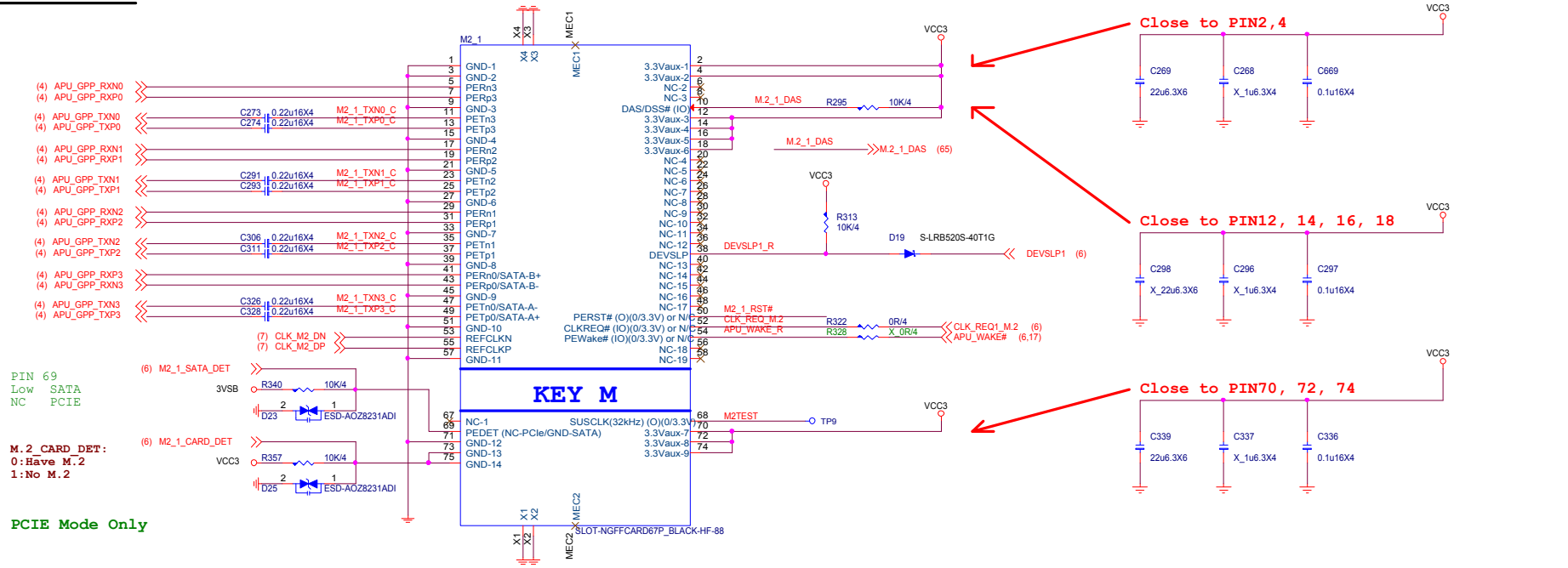


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>PCL E4 / M2_2 SWITCH</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 23	of 76

# M.2 1 Connector

M2下方零件擺放限高要小於0.9mm的零件

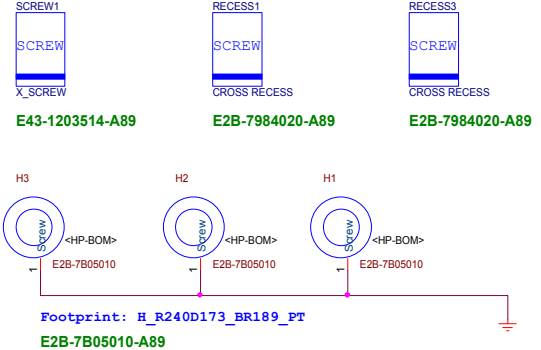
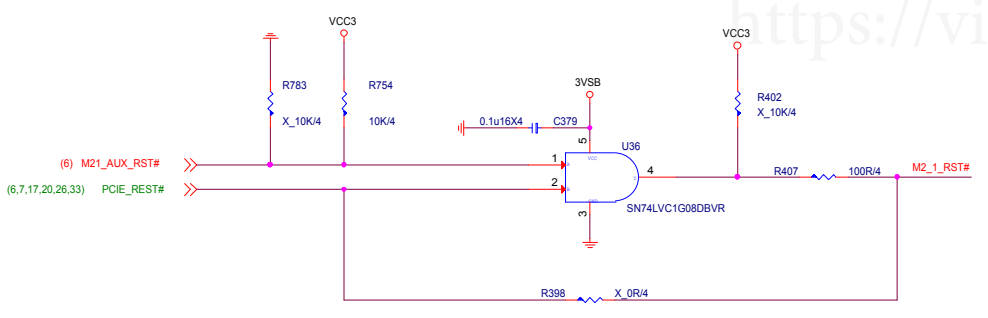
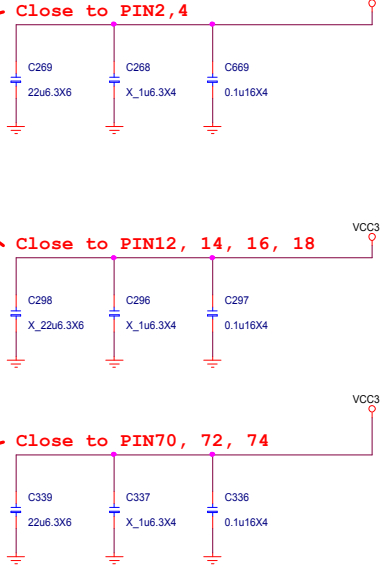
VCC3 4.25A  
Max: 14W



PIN 69  
Low SATA  
NC PCIE

M.2\_CARD\_DET:  
0: Have M.2  
1: No M.2

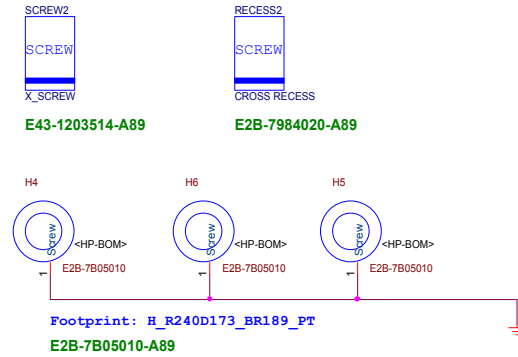
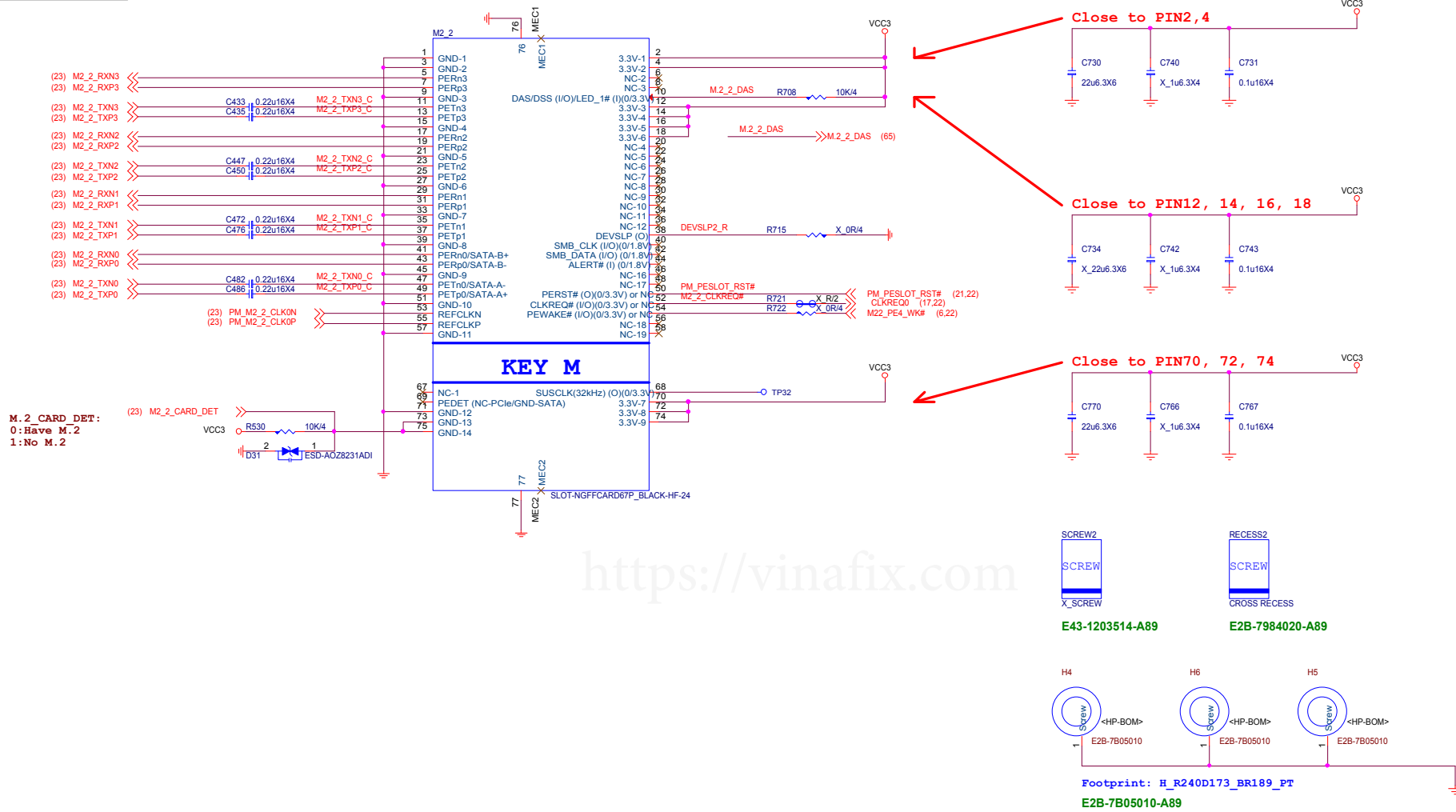
PCIE Mode Only



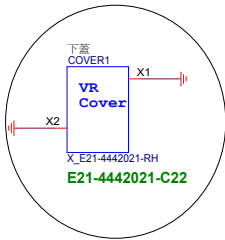
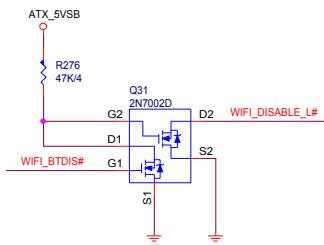
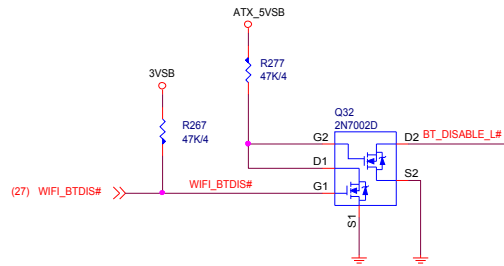
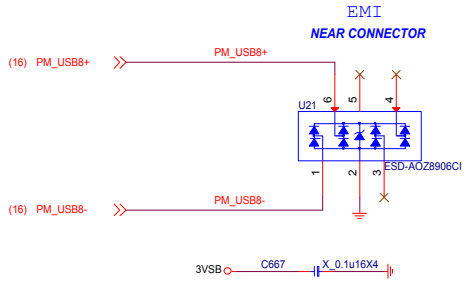
# M.2 2 Connector

M2下方零件擺放限高要小於0.9mm的零件

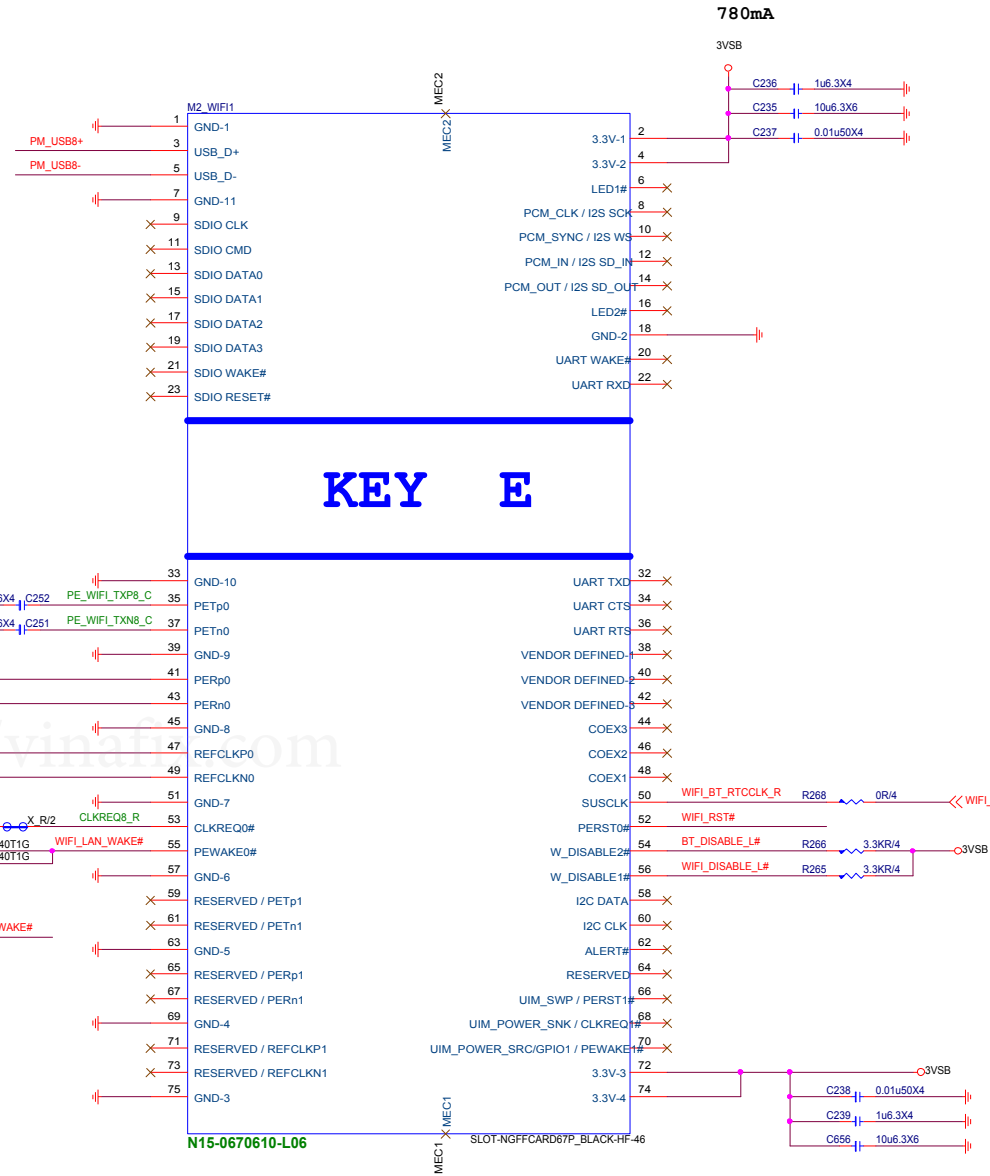
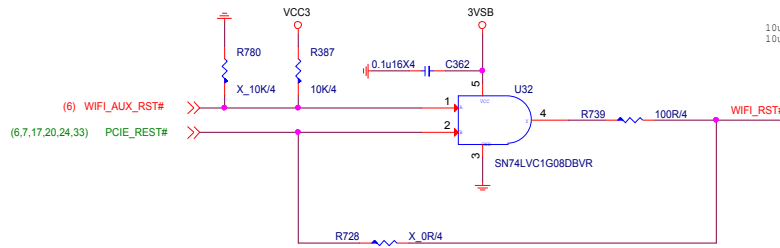
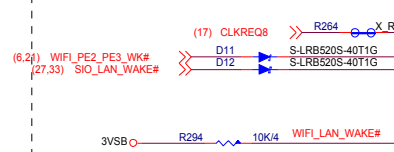
VCC3 4.25A  
Max: 14W



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Wireless1  
INTEL-AX200  
MS-4467 Wireless  
604-4467-020



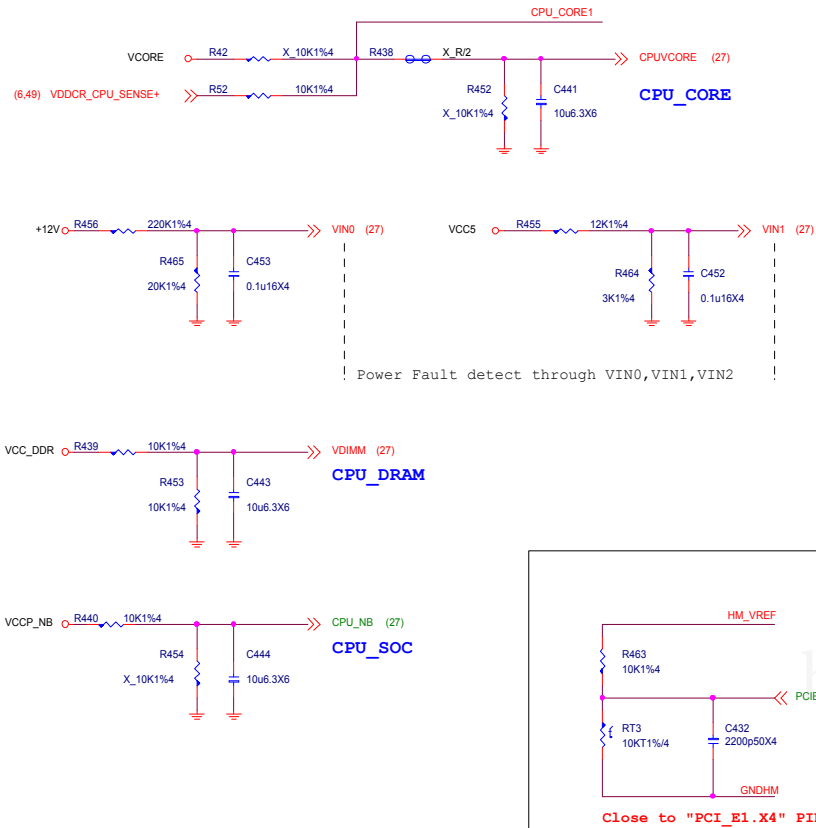
10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

<b>MSI</b>		
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>M2_WIFI1 (KEY_E)</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 26 of 76	

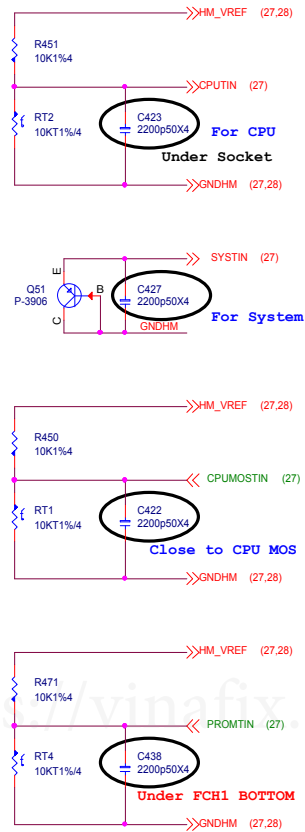


# HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect



# TEMP SENSOR



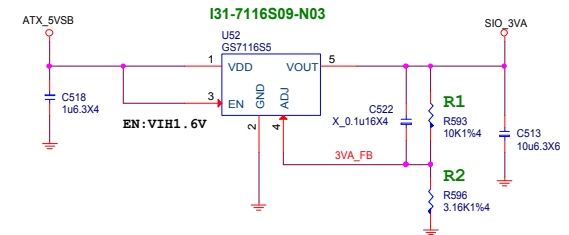
# PM RESET

# CPU RESET

# SIO PLN



# SIO\_3VA



$$\begin{aligned}
 V_{out} &= V_{ref} * (1 + (R1/R2)) \\
 &= 0.8 * (1 + (10K/3.16K)) \\
 &= 3.33V
 \end{aligned}$$

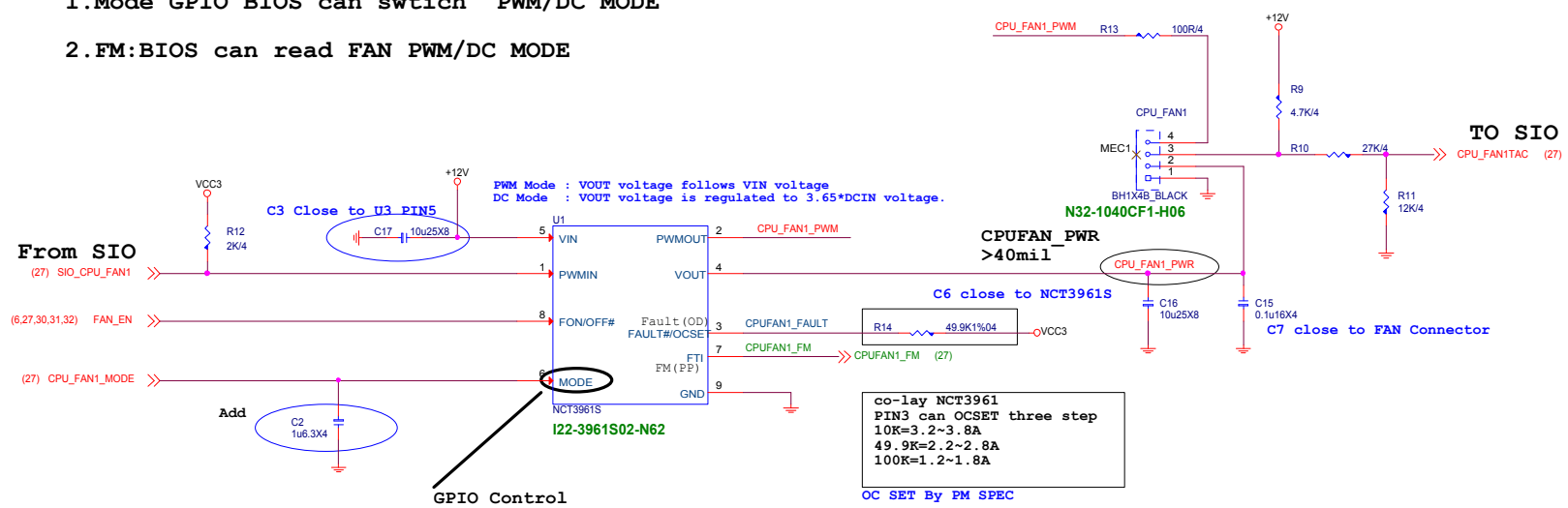


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>SIO - HW Monitor / RESET</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 28	of 76

# CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI (Floating)

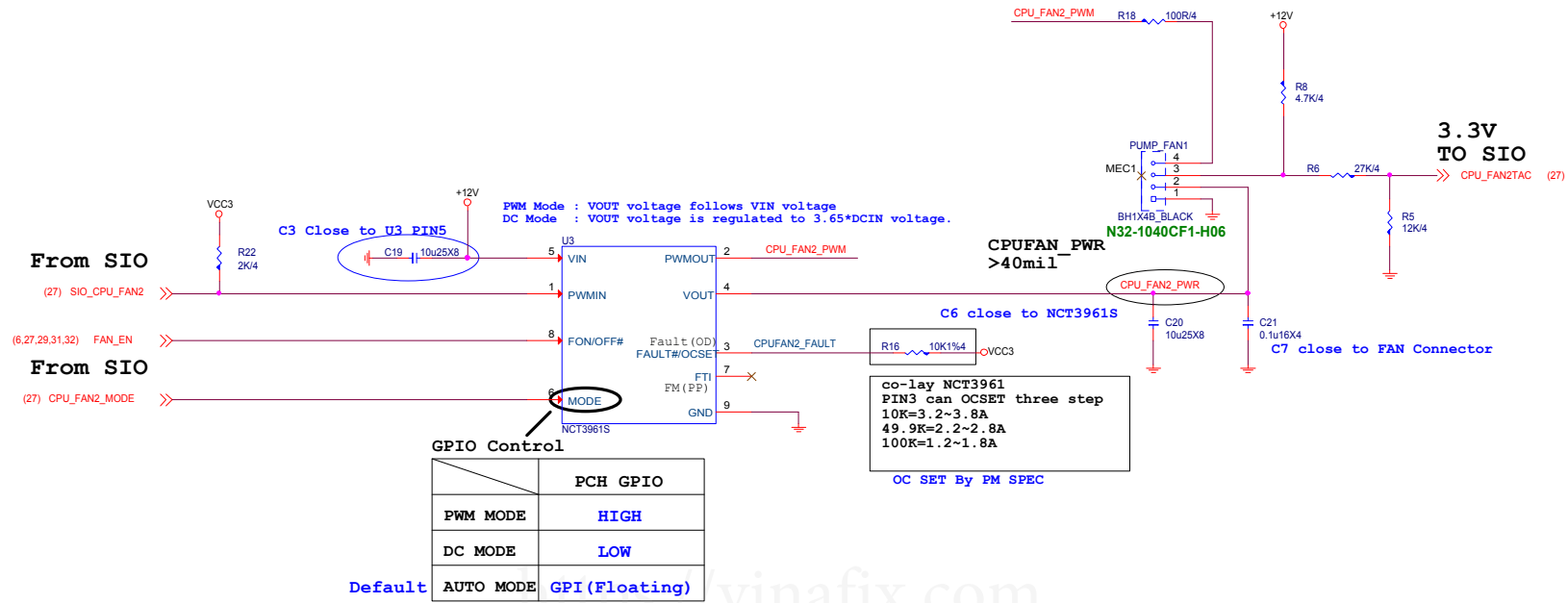
<https://vinafix.com>

Vinafix.com

# PUMPFAN1

## TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

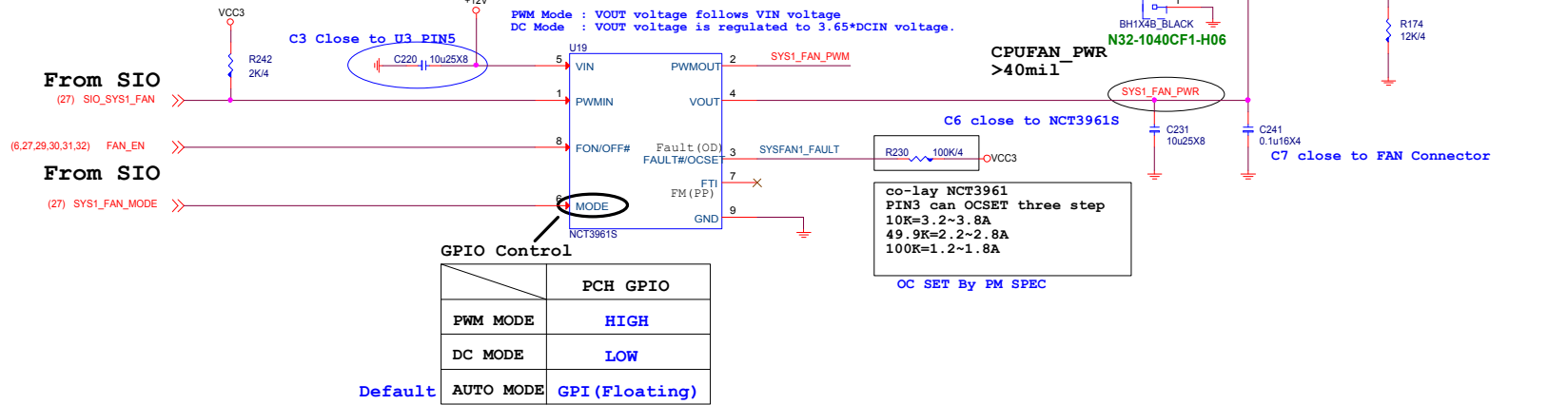
1.Mode GPIO BIOS can switch PWM/DC MODE



# SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

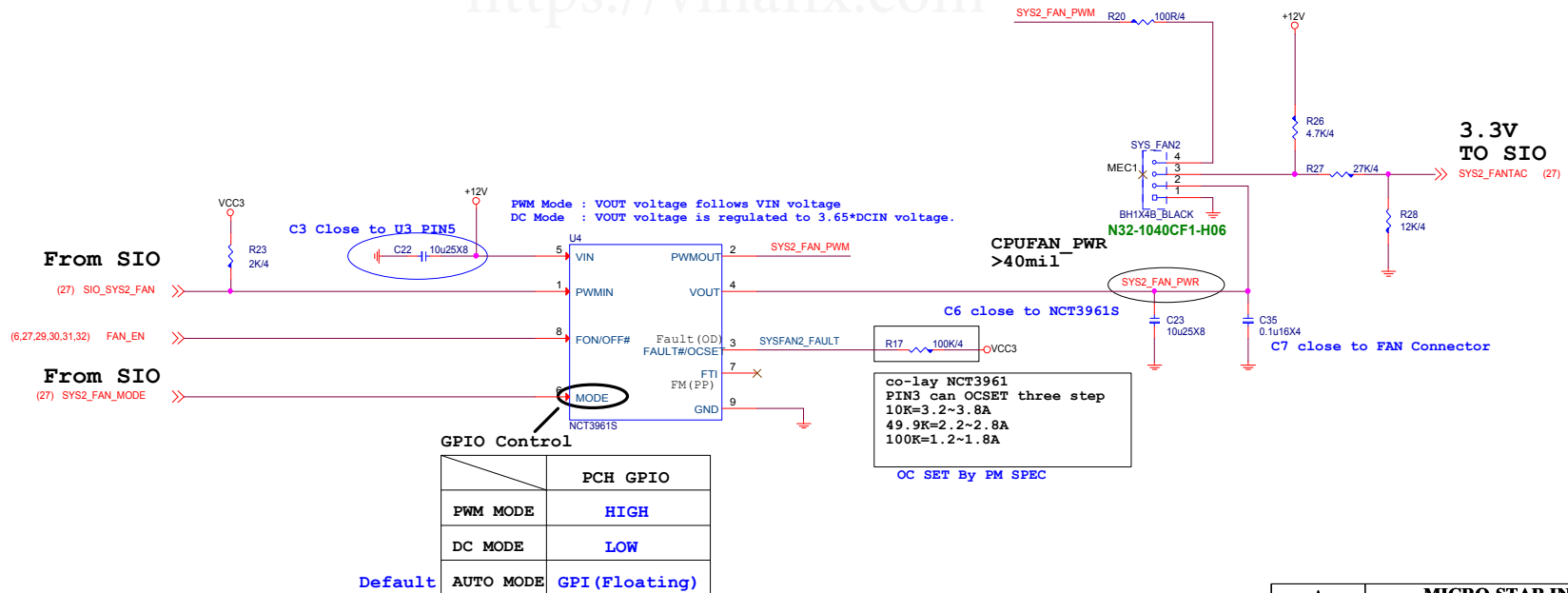
1.Mode GPIO BIOS can switch PWM/DC MODE



# SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

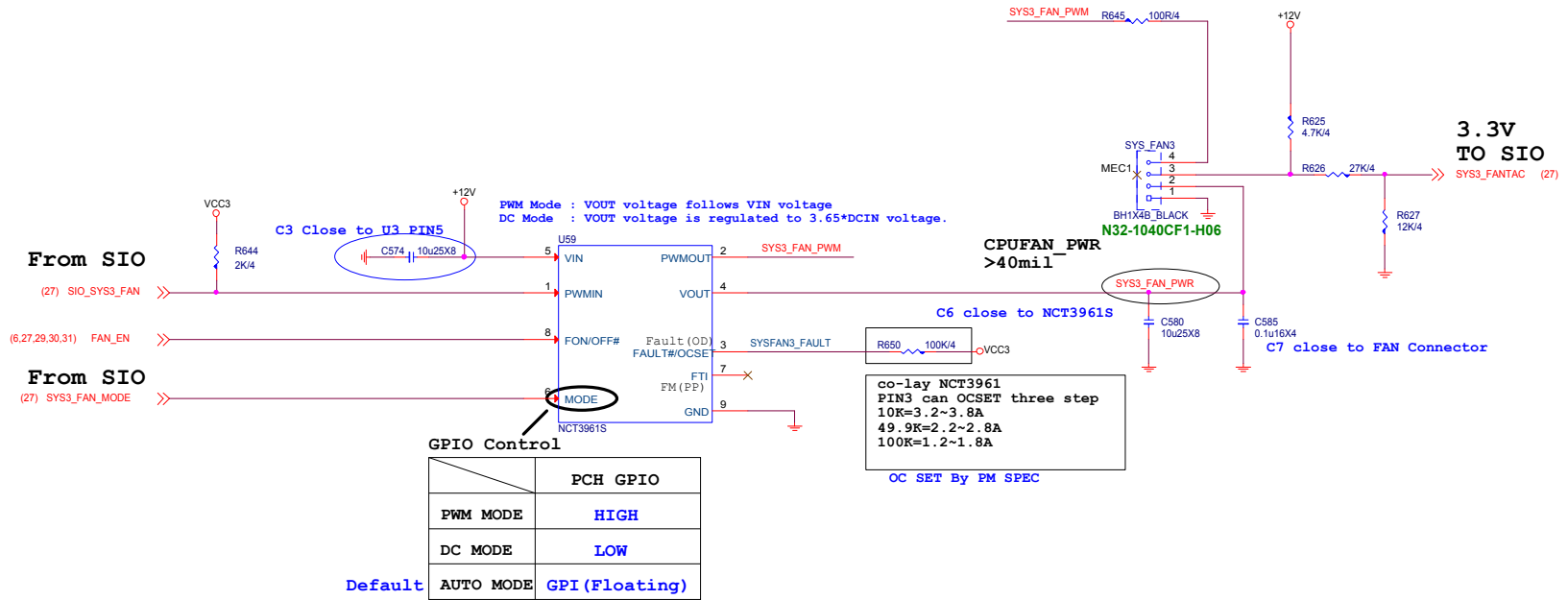


MICRO-STAR INT'L CO.,LTD		
MS-7C94		
Size Custom	Document Description FAN TYPE-M SYSFANI / 2	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 31	of 76

# SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can switch PWM/DC MODE

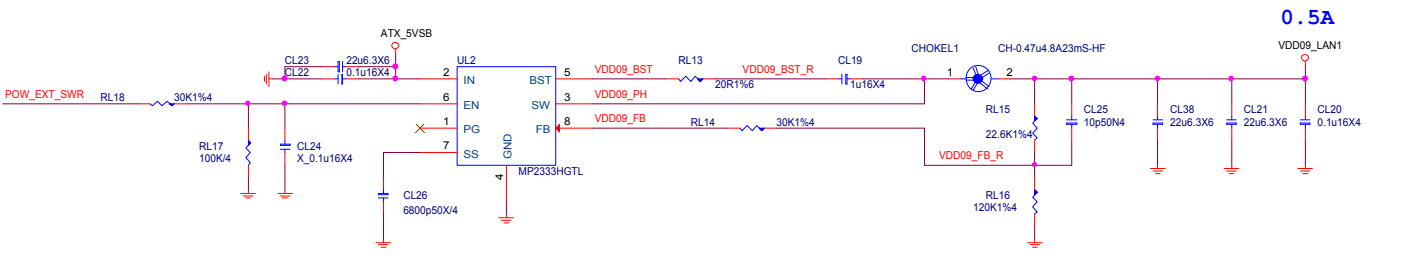
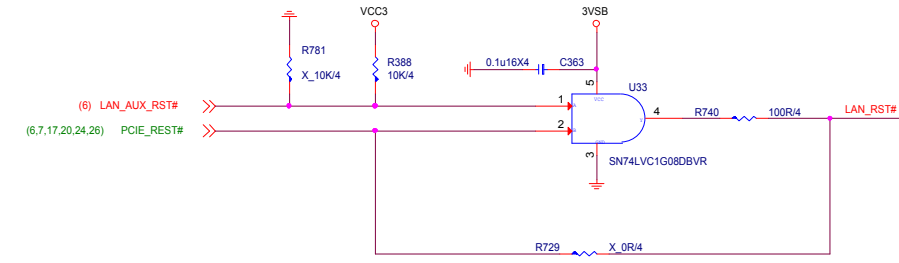
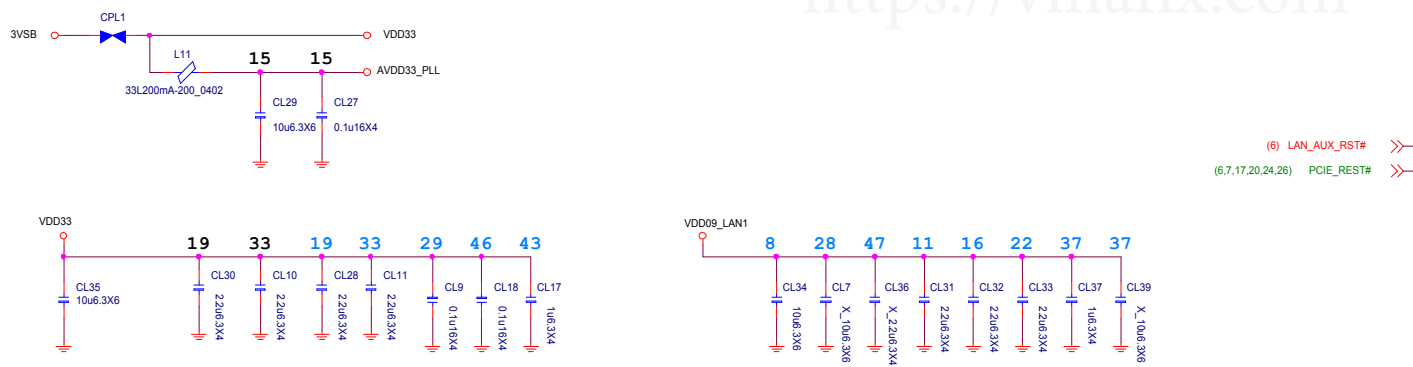
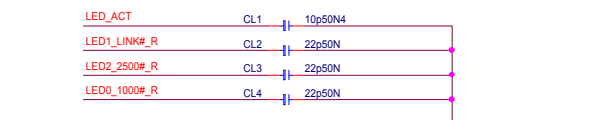
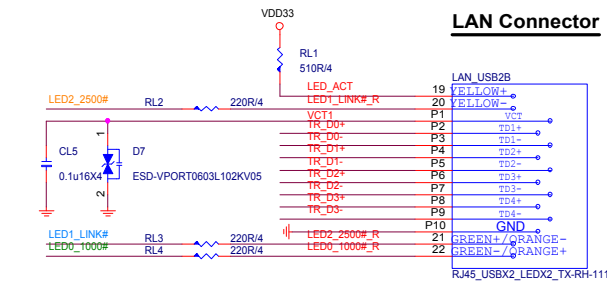
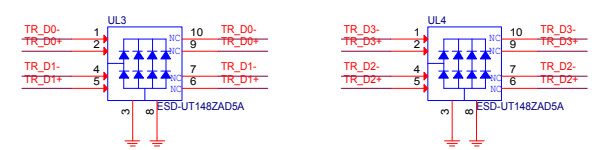
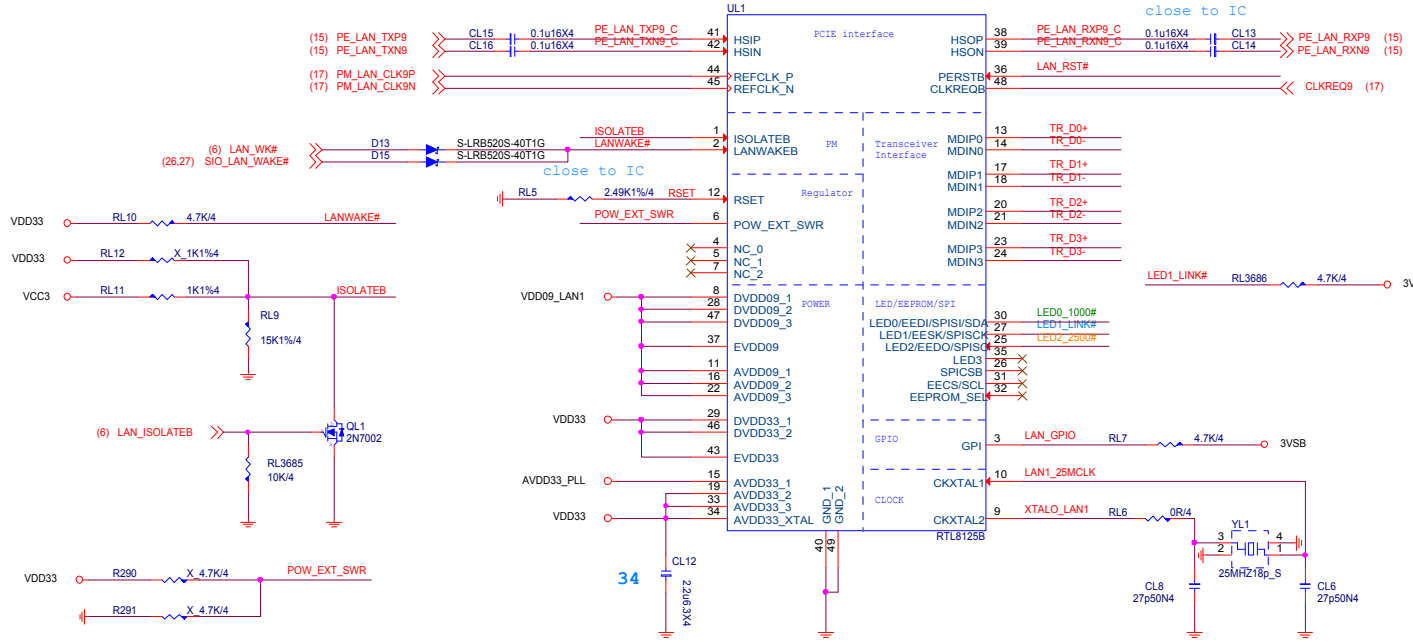


<https://vinafix.com>

Vinafix.com

# Realtek Lan1-RTL8125B(2.5G)

ESD Protect  
close to connector



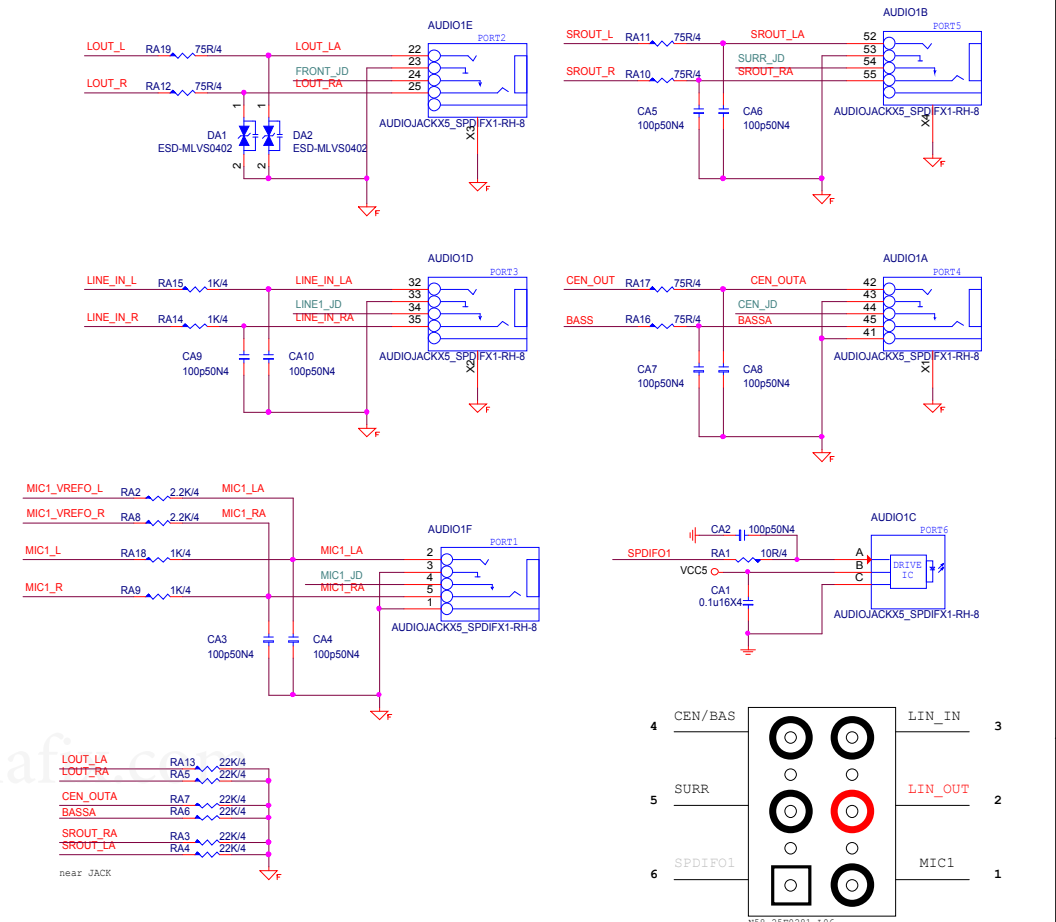
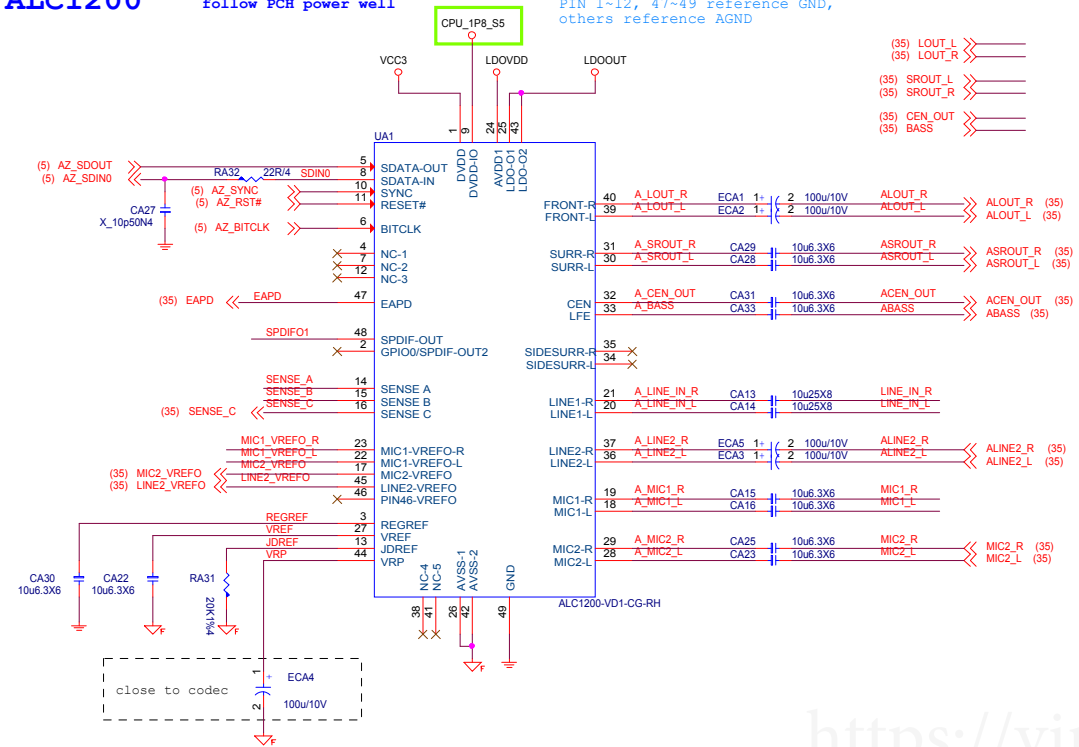
<https://vinafix.com>

<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>LAN - RTL8125B</b>	Rev 1.0
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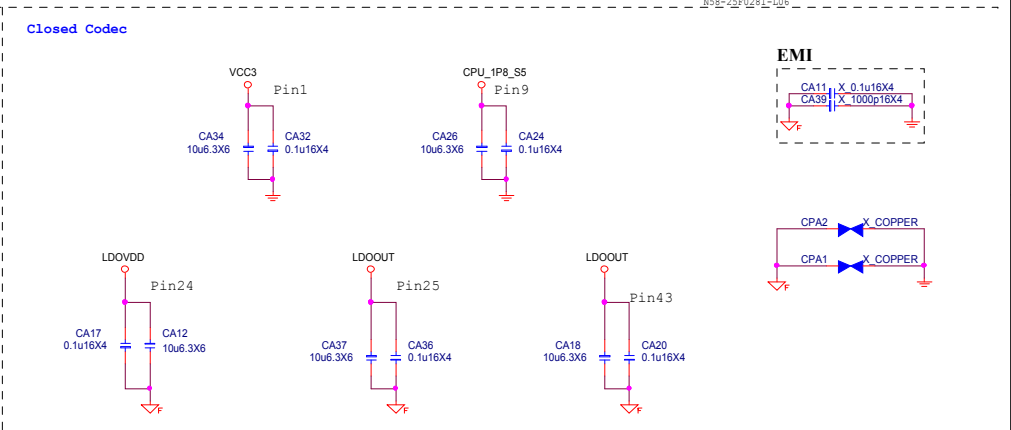
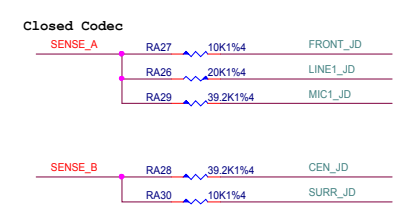
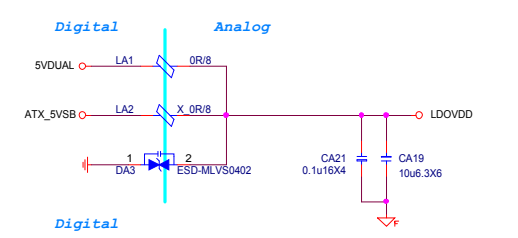
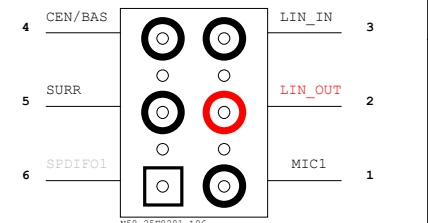
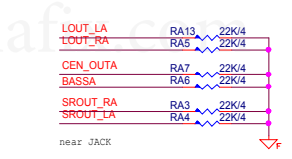
# ALC1200

follow PCH power well

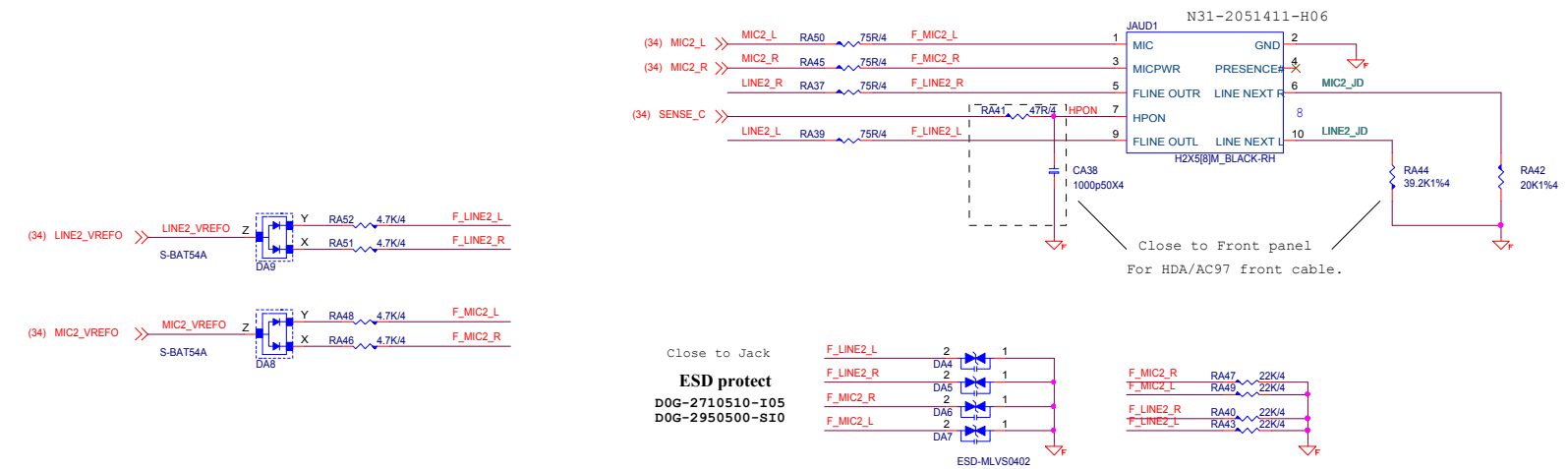
PIN 1~12, 47~49 reference GND, others reference AGND



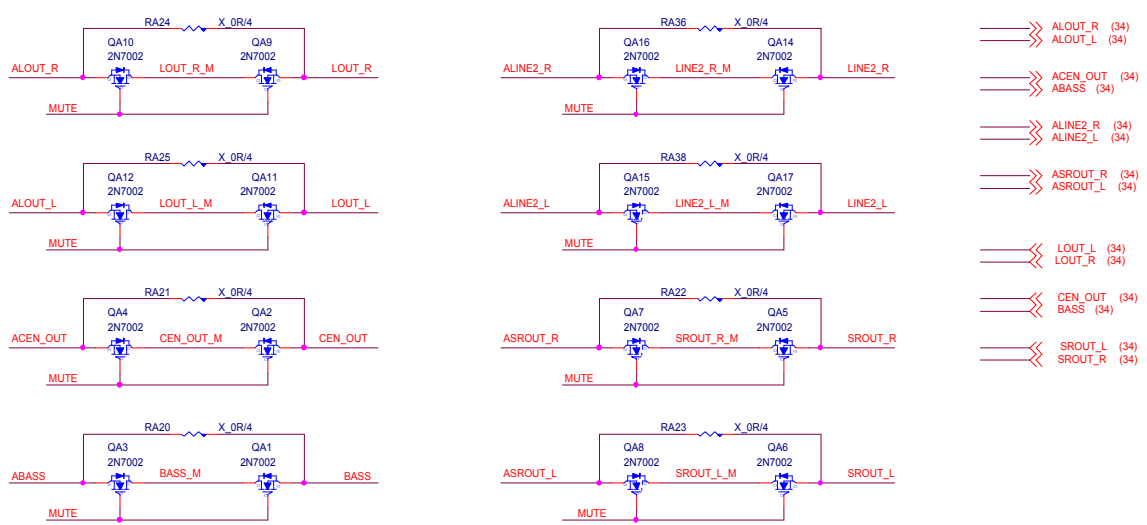
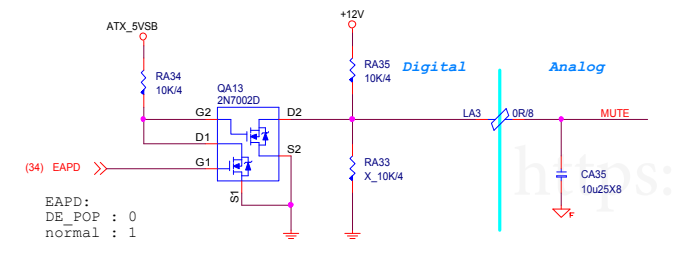
<https://vinaf.com>



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>Audio ALC1200</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 34 of 76	



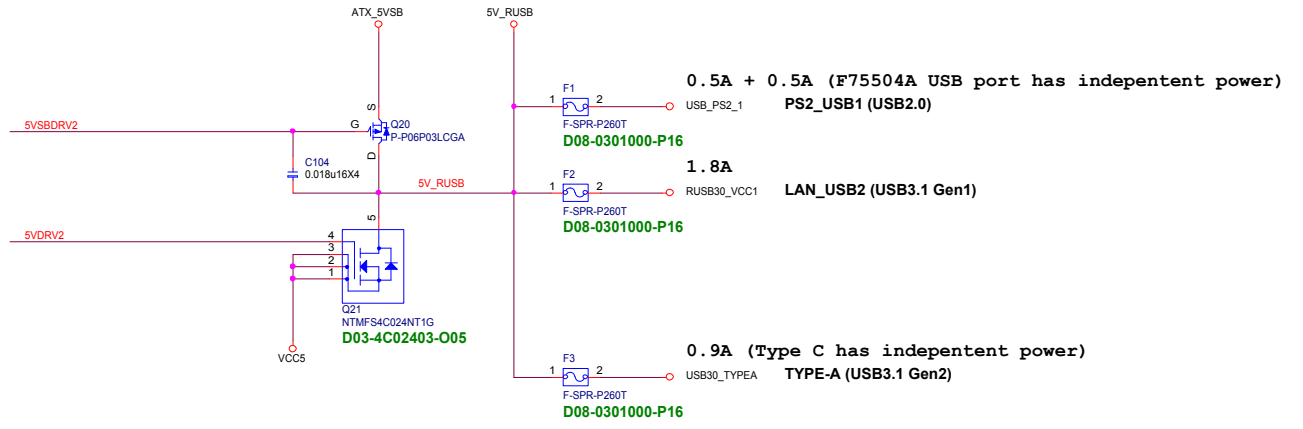
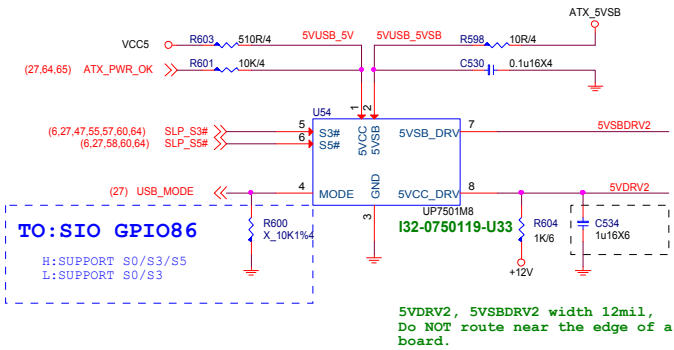
**De-POP circuit**



Vinafix.com

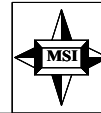
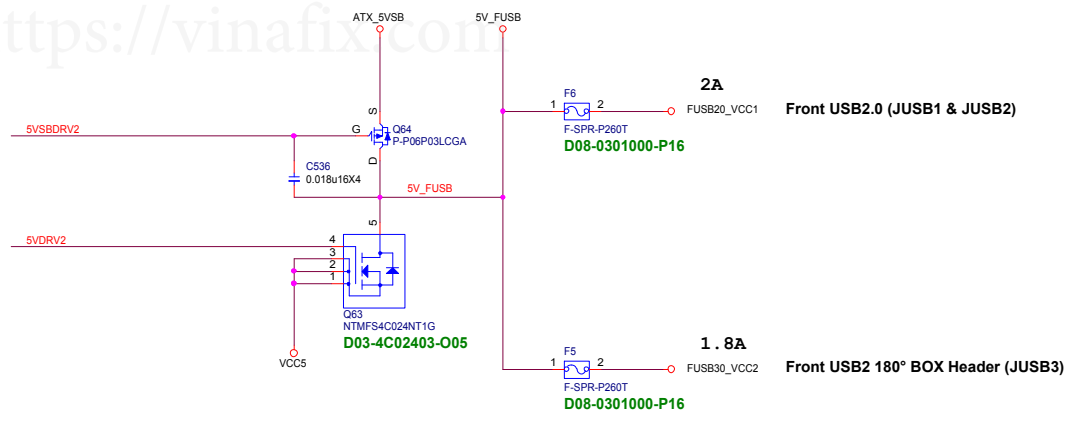
	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-7C94</b>	
Size Custom	Document Description <b>Audio DePoP</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 35 of 76	

# USB Power



## Rear (6A)

## Front (5.6A)

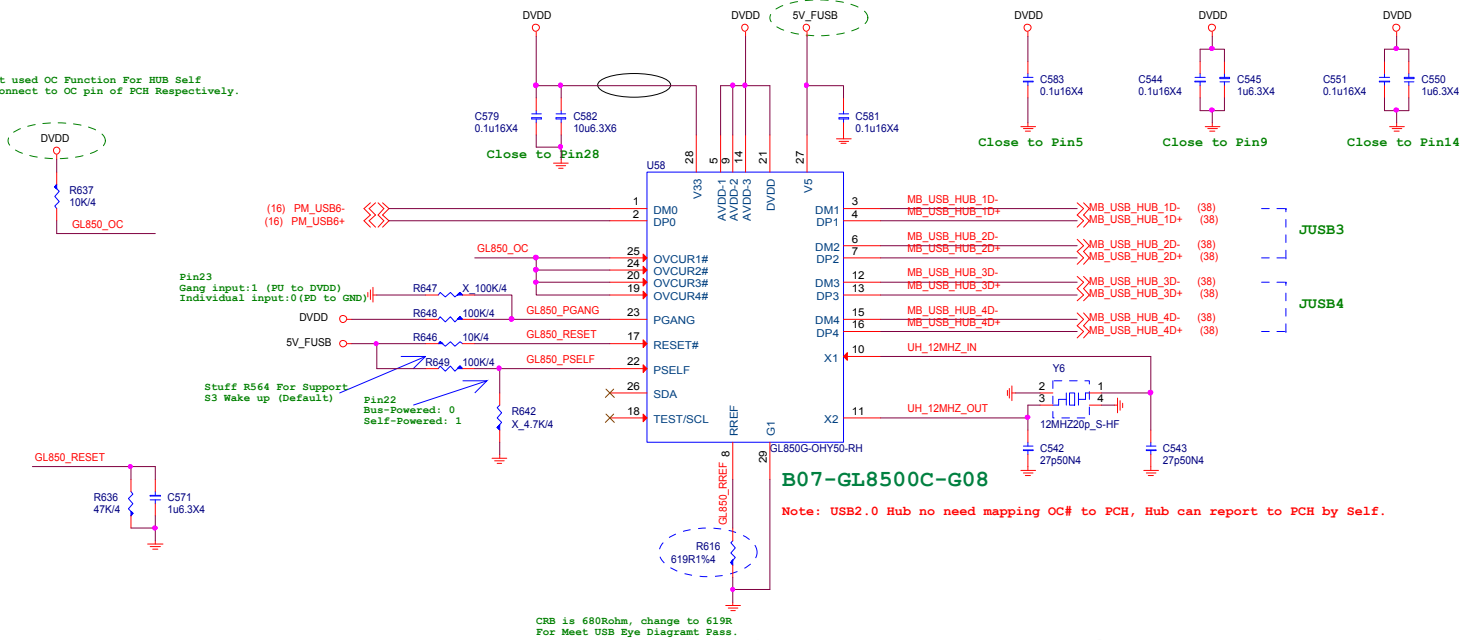


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>USB Power - UP7501</b>	Rev 1.0
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# GL850G USB2.0 HUB

Note: Not used OC Function For HUB Self  
Please connect to OC pin of PCH Respectively.

Note: Please connect to USB Power Source.



**B07-GL8500C-G08**

Note: USB2.0 Hub no need mapping OC# to PCH, Hub can report to PCH by Self.

CRB is 680Rohm, change to 619R  
For Meet USB Eye Diagram Pass.

<https://vinafix.com>



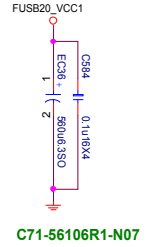
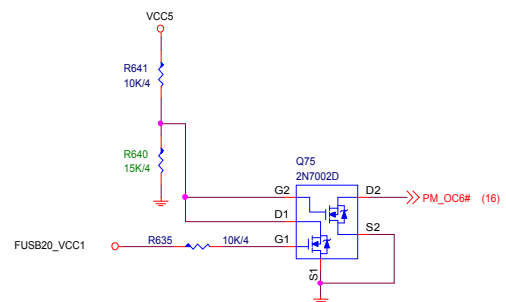
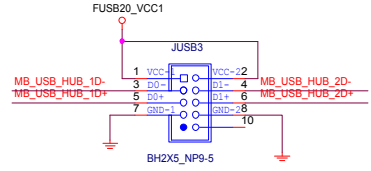
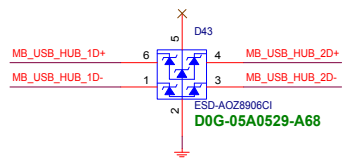
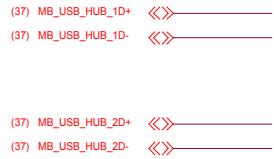
MICRO-STAR INT'L CO.,LTD

MS-7C94

Size Custom	Document Description <b>Front USB2.0 GL850G</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 37 of 76	

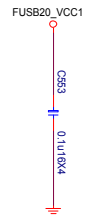
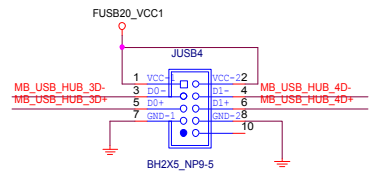
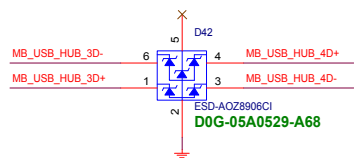
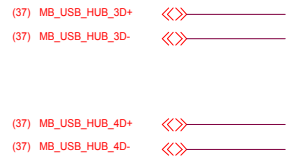
# Front USB2.0 (JUSB1) Form GL850G USB2.0 HUB

5V@1A



# Front USB2.0 (JUSB2) Form GL850G USB2.0 HUB

5V@1A



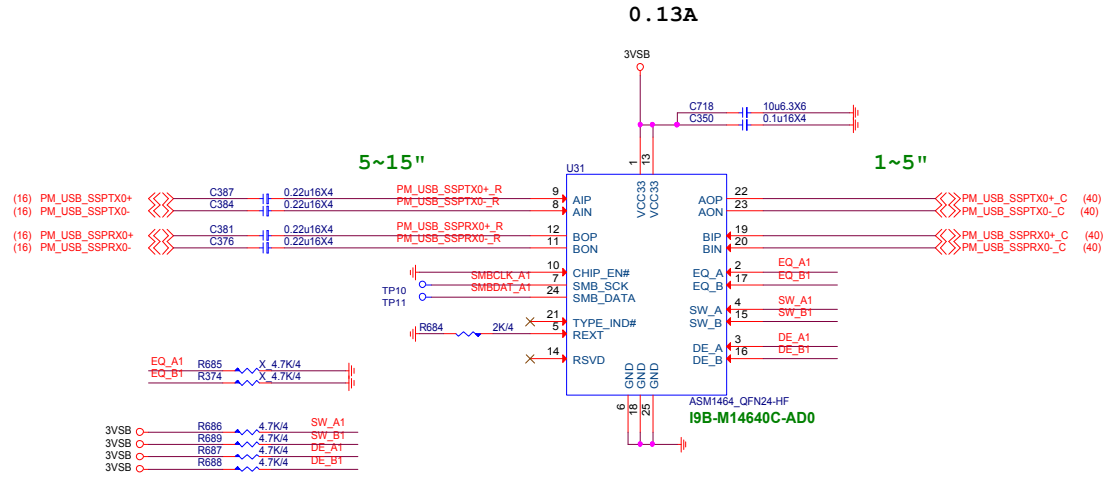
<https://vinafix.com>

Vinafix.com



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>Front USB2.0 Header</b>	Rev 1.0
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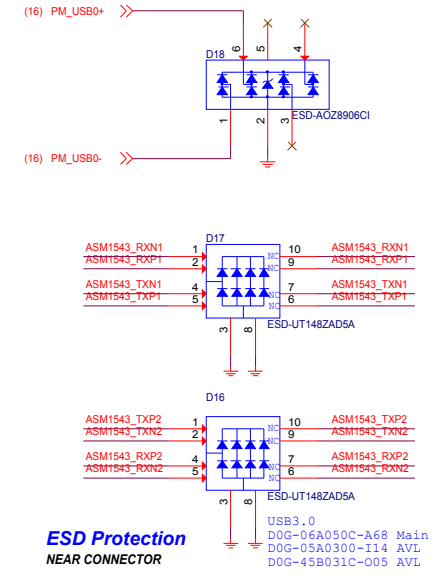
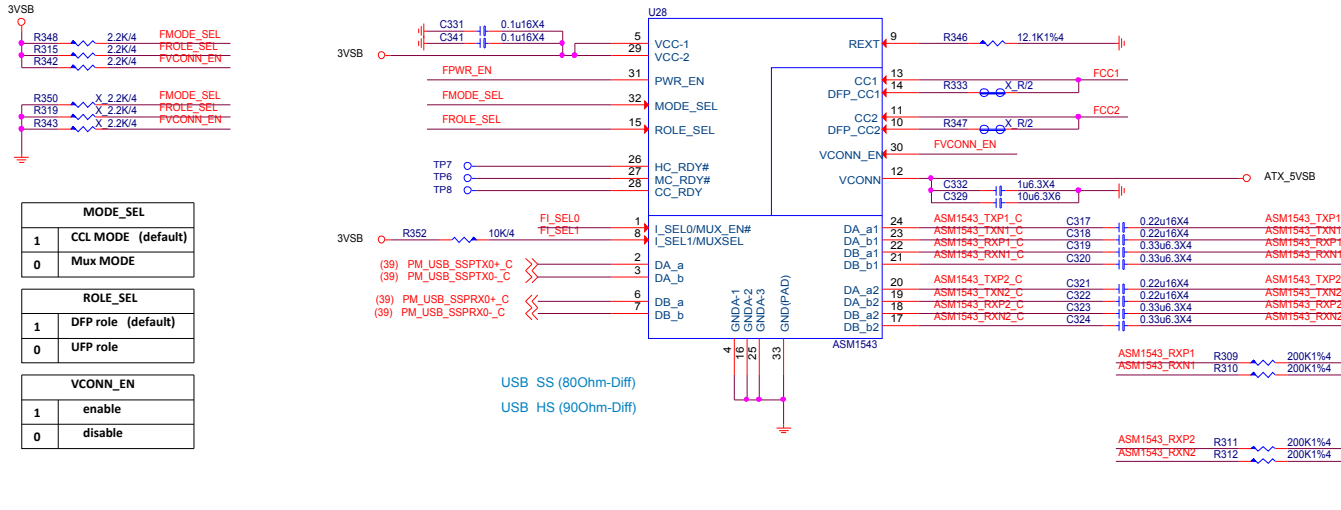
USB3.1 Gen1 Redriver for Type-C



<https://vinafix.com>

# USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)

Vinafix.com

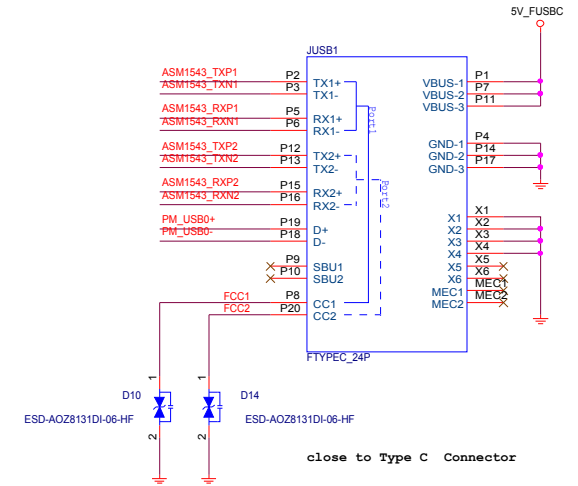
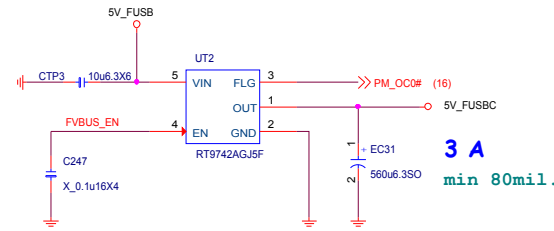
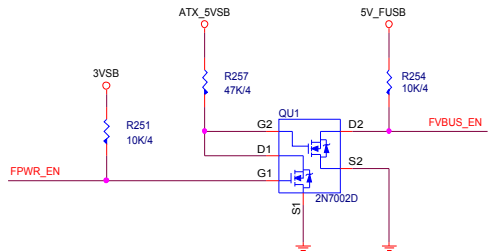


## VBUS OC# LEVEL SHIFT

## VBUS EN

## VCOM OC#

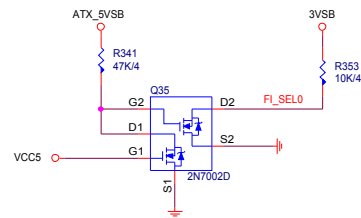
<https://vinafix.com>



## Current Mode

I_SEL0	I_SEL1	
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode  
3A under S0 mode



**MICRO-STAR INT'L CO.,LTD**

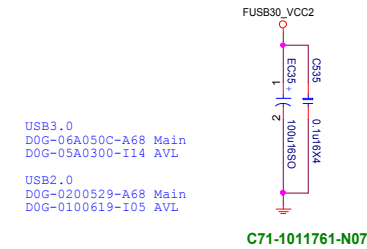
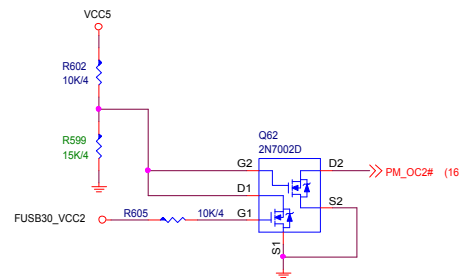
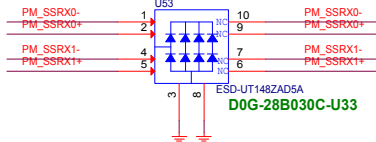
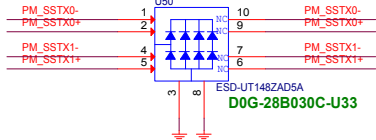
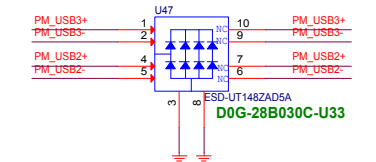
**MS-7C94**

Size	Document Description	Rev
Custom	Front USB3.0 Type C	1.0

Date: Tuesday, April 28, 2020 | Sheet 40 of 76

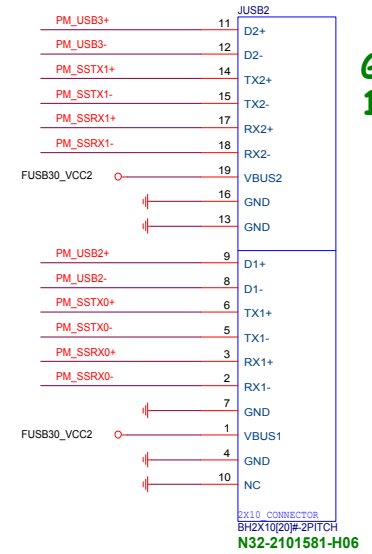
**Front USB3 180° BOX Header(JUSB3)**

**5V@1.8A**



USB3.0  
 D0G-06A050C-A68 Main  
 D0G-05A0300-I14 AVL

USB2.0  
 D0G-0200529-A68 Main  
 D0G-0100619-I05 AVL



**GEN1  
 1.8A**

<https://vinafix.com>

	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-7C94</b>	
Size Custom	Document Description <b>Front USB3.0 Header</b>	Rev 1.0
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# F75504A colay F75504

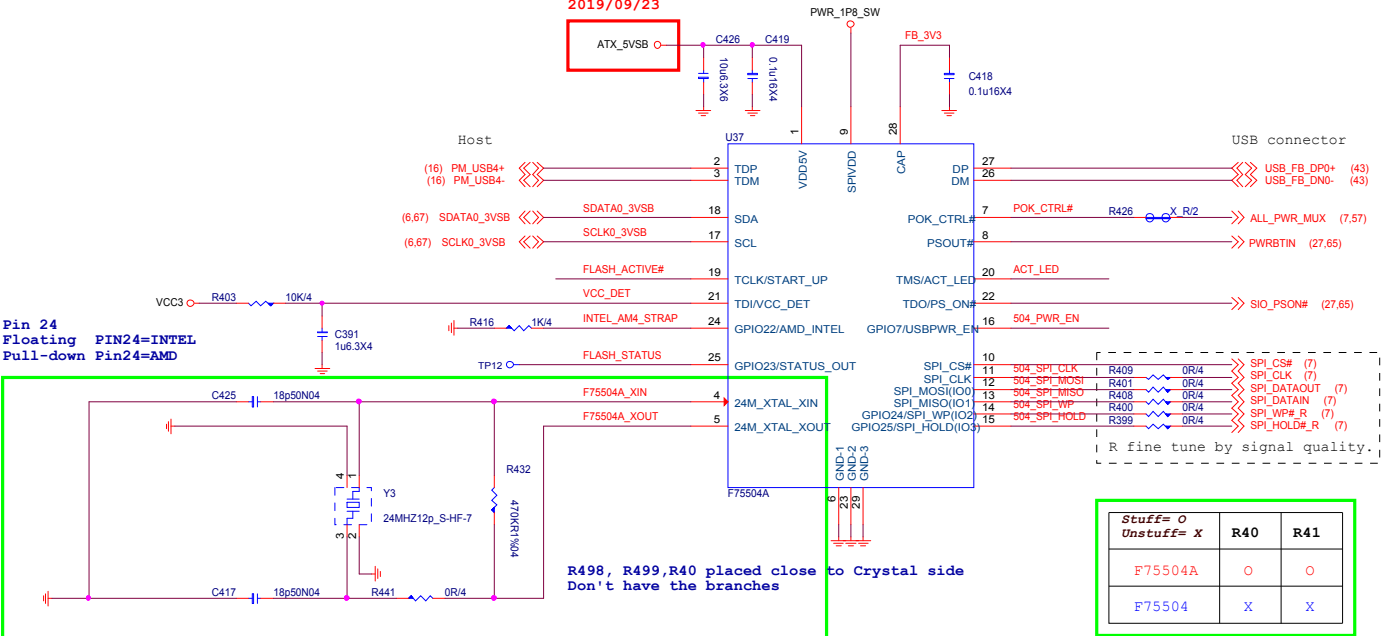
F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.

Fix intel 3VSB drop  
2019/09/23

Fix intel 3VSB drop  
2019/09/23

Fix intel 3VSB drop  
2019/09/23

Pin 24  
Floating PIN24=INTEL  
Pull-down Pin24=AMD



R498, R499, R40 placed close to Crystal side  
Don't have the branches

R503 placed close R40

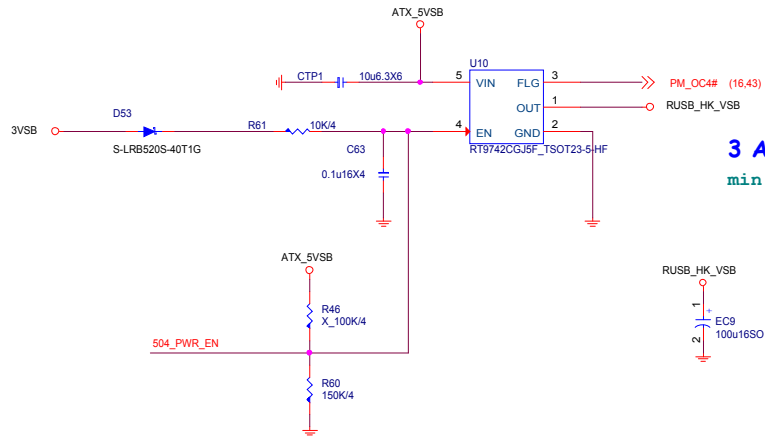
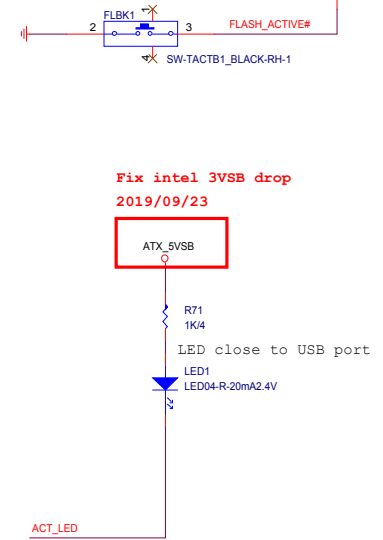
Stuff= 0 Unstuff= X	R495	R498	R499	R503	C436	R496	R497	R502	Y1
F75504A	O	O	X	X	10pF	0R	X	O	D04-3902700-F07
F75504	X	X	O	O	X	0.1uF	O	X	D05-1100600-F07

Stuff= 0 Unstuff= X	R40	R41
F75504A	O	O
F75504	X	X

2019/06/17

<https://vinafix.com>

Colay 75504  
2019/06/17

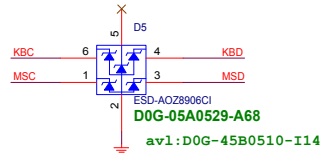
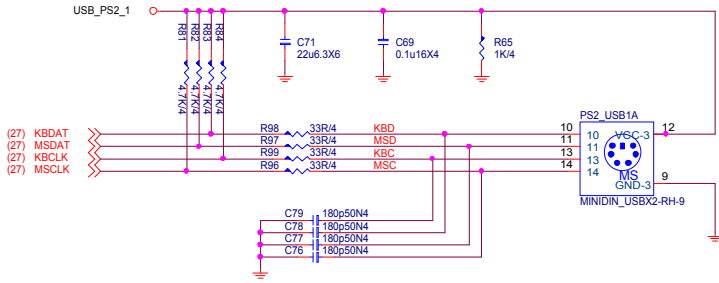


3 A  
min 80mil.

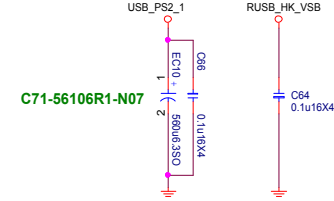
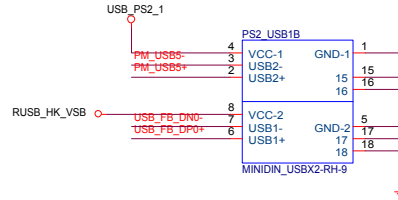
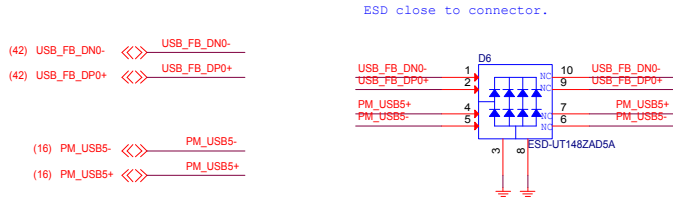
# PS2+USB (USB2.0)

5V@1A

layout note:  
 C21 must close to TVS pin5  
 TVS must near KB\_MS1 connector and route without branch  
 Varistor must close to TVS and route without branch

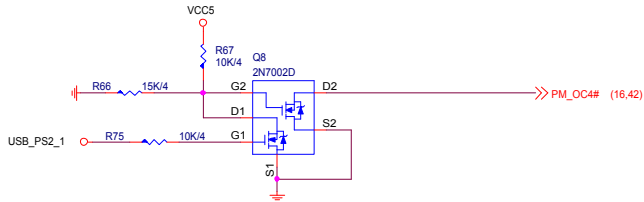


Vinafix.com



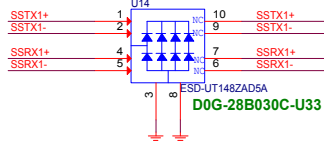
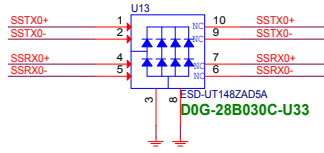
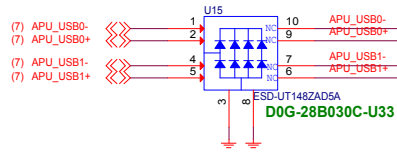
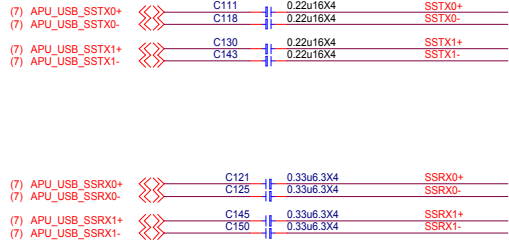
1A USB Flash BIOS

<https://vinafix.com>



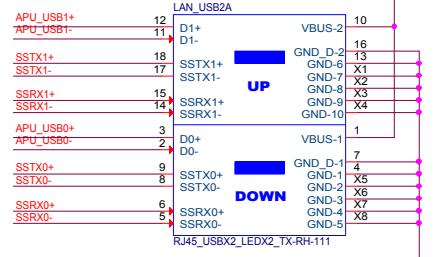
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>Rear USB2.0 + PS2</b>	Rev 1.0
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**Rear USB3.1 GEN1 5V@1.8A**  
**TYPE-A X2 from CPU**

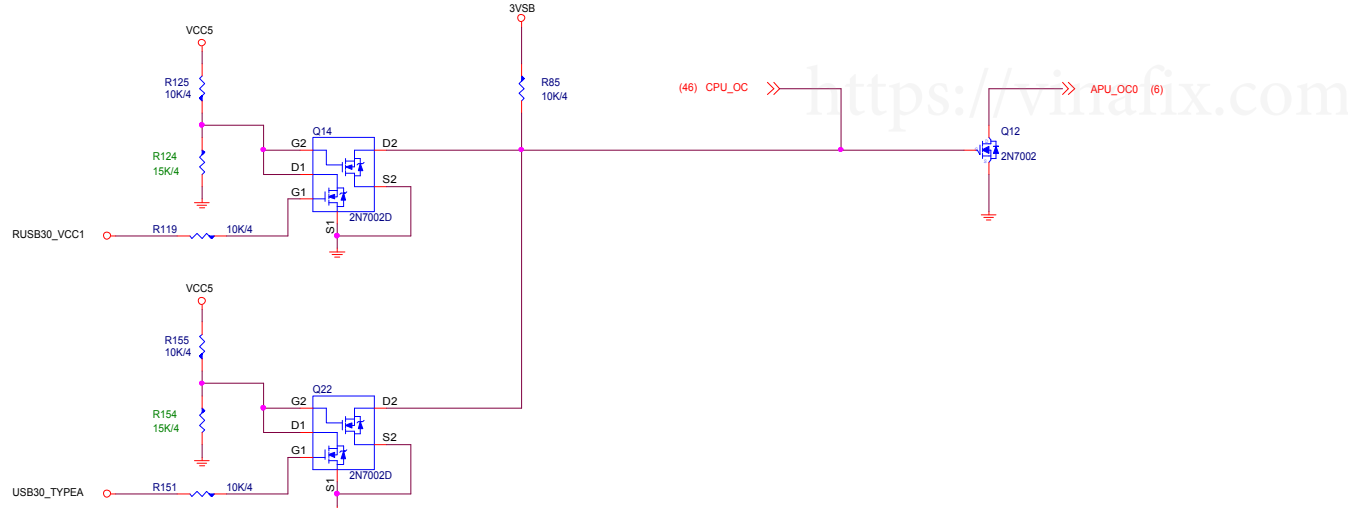


LAN下方  
**GEN1**

**1.8A**



**CPU OC Logic**



Type1/2/3/4 High Active

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

**MICRO-STAR INT'L CO.,LTD**

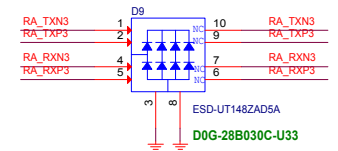
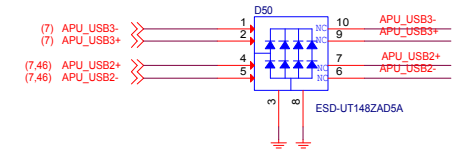
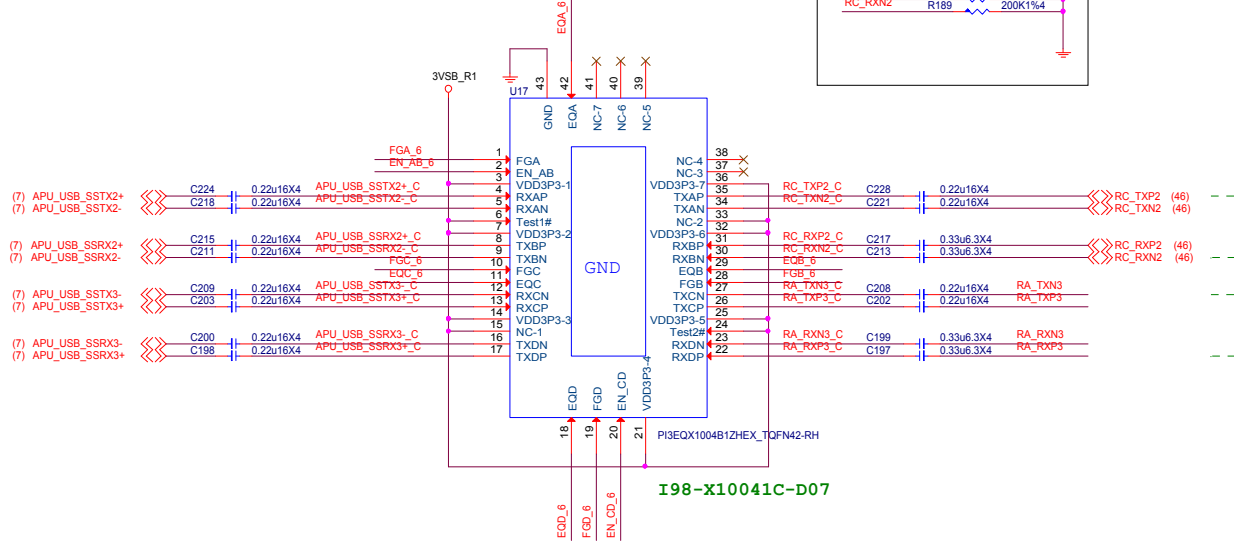
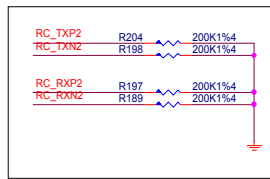
**MS-7C94**

Size Custom	Document Description <b>Rear USB3.0 / OC Logic</b>	Rev 1.0
Date: Tuesday, April 28, 2020		Sheet 44 of 76

Rear USB3.1 GEN2 5V@1.8A

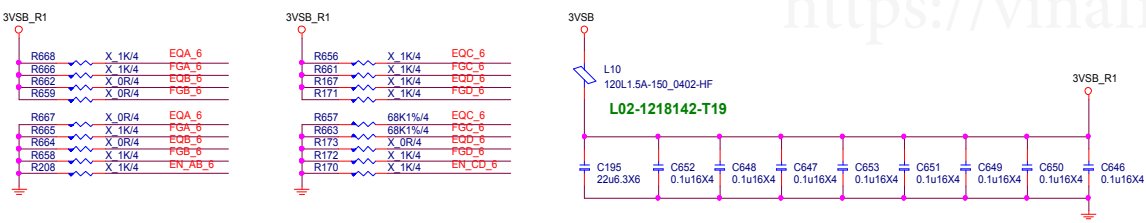
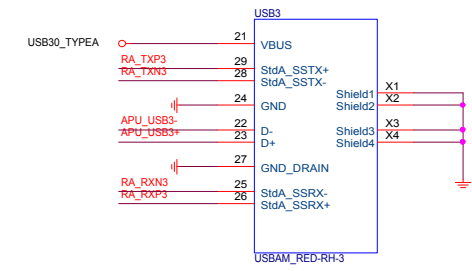
TYPE A+C from CPU

PI3EQX1004 Redriver



0.9A

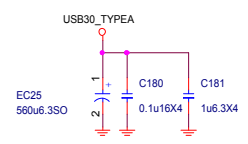
GEN2



EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD



C71-56106R1-N07  
close to Type C Connector

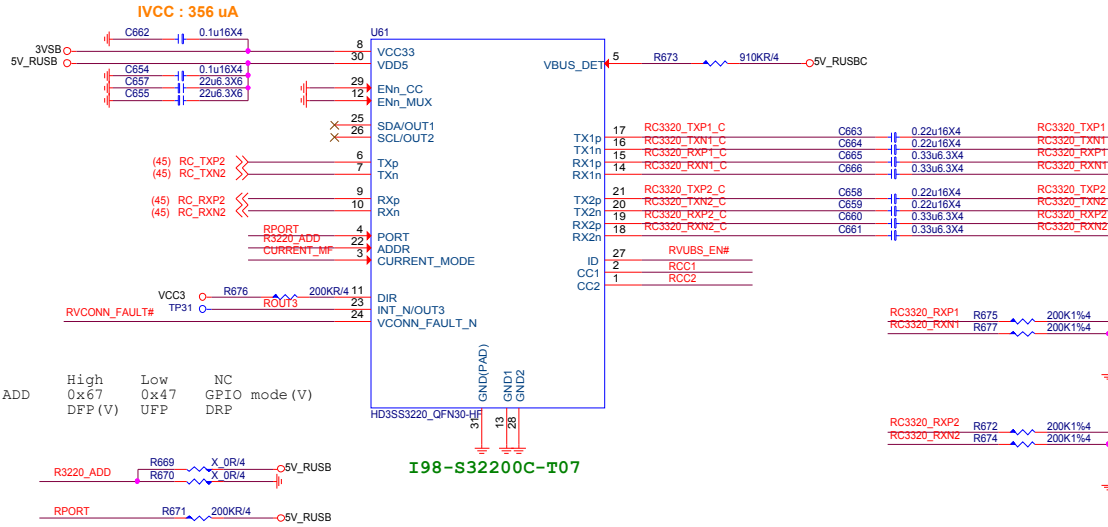
<https://vinafix.com>

**MICRO-STAR INT'L CO.,LTD**

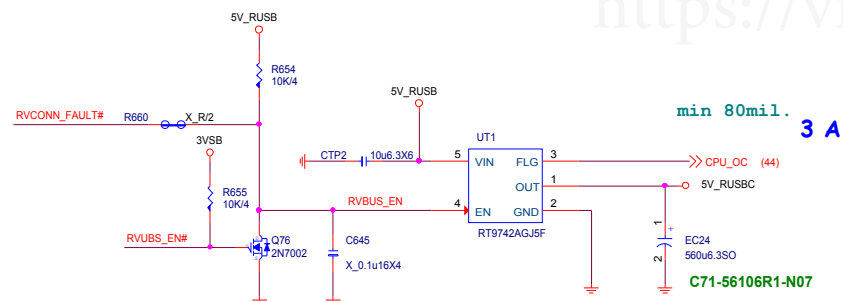
**MS-7C94**

Size	Document Description	Rev
Custom	Rear USB3.1 Type A / Redrive	1.0
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# USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)

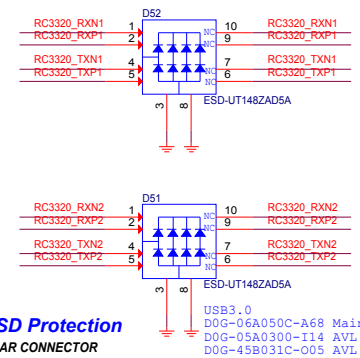
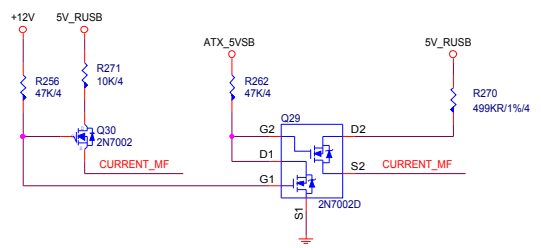


## VBUS EN

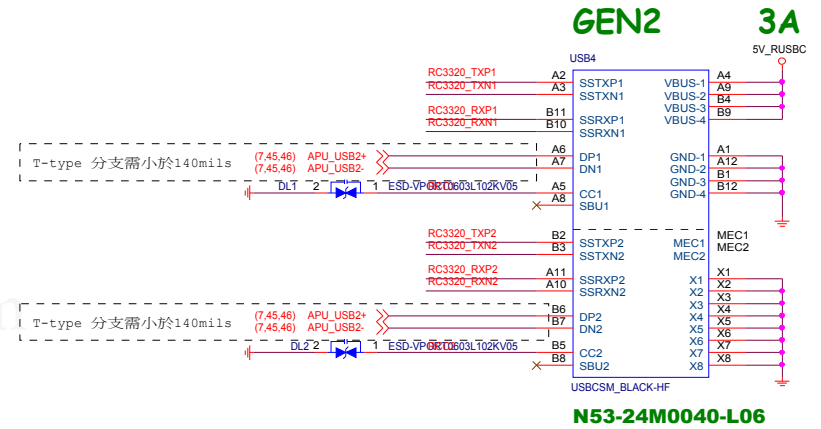


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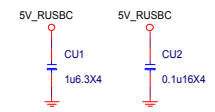
## Current Mode



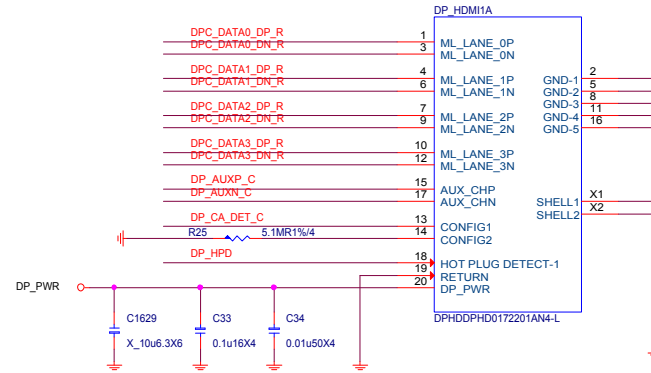
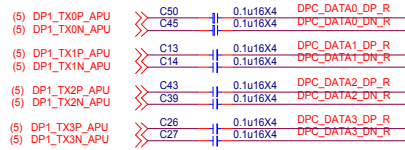
ESD Protection NEAR CONNECTOR



close to Type C Connector

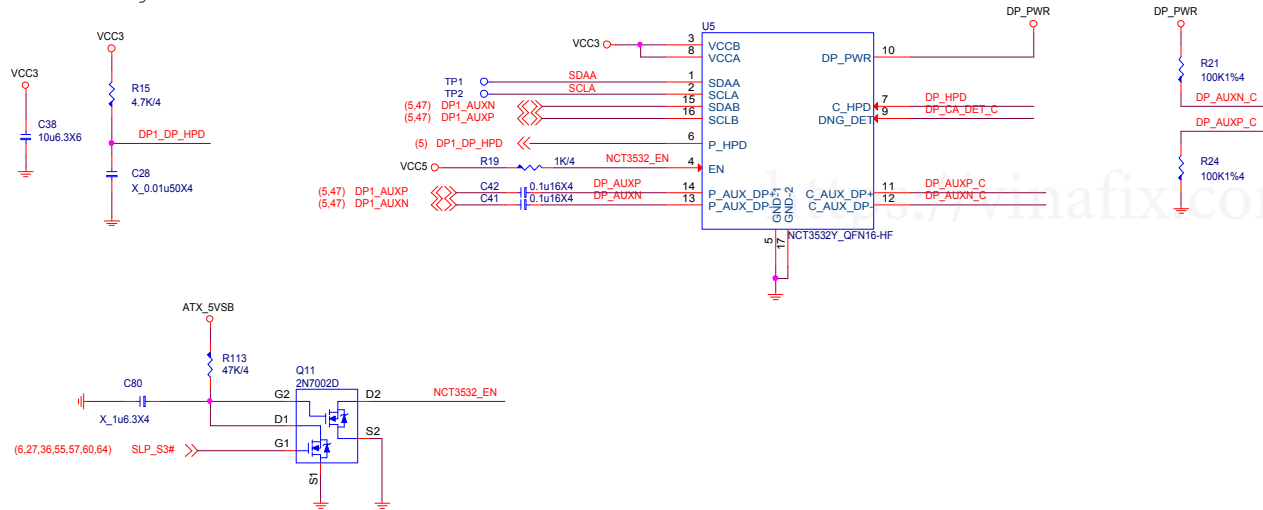


# DP CONNECTOR

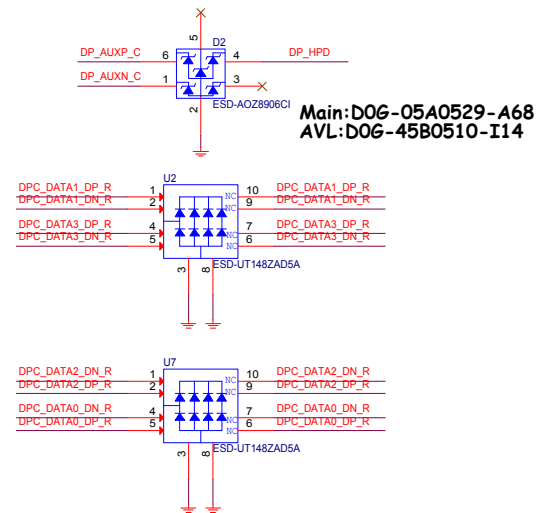


## DP AUX & HPD Circuit

Support HDMI Dongle



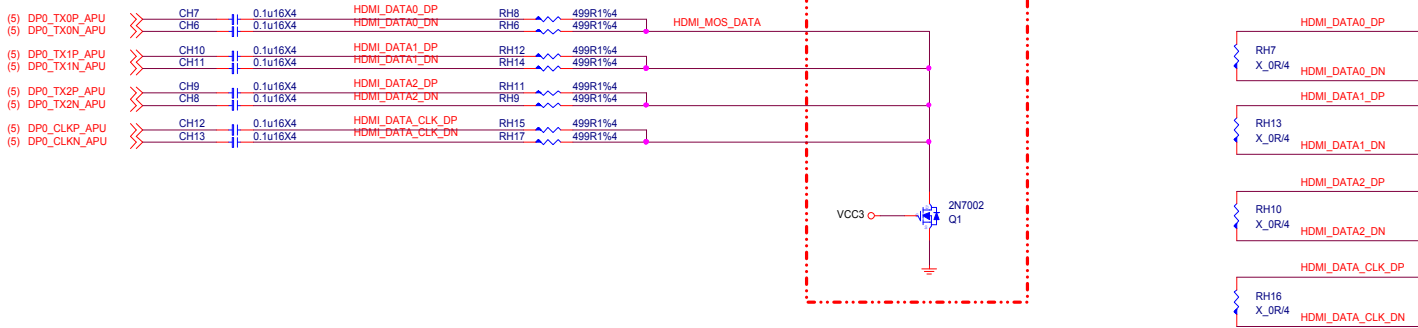
## ESD



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
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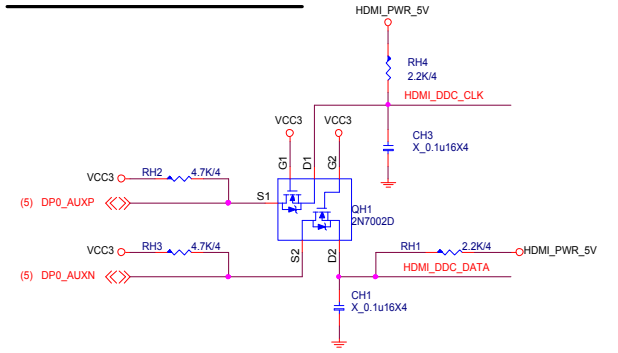
# HDMI CONNECTOR

For HDMI 1.4

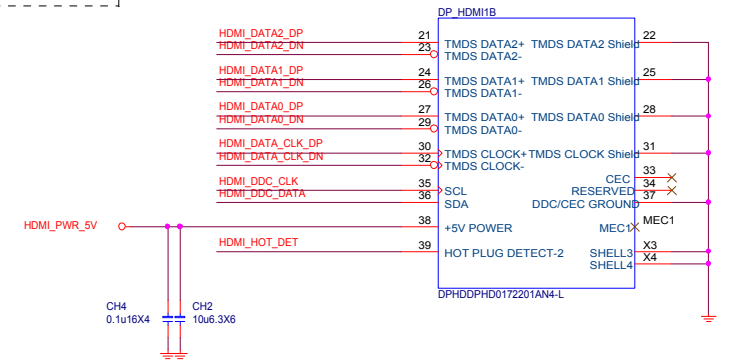


HDMI\_MOS\_DATA trace length <500mil  
other platform please check design guide

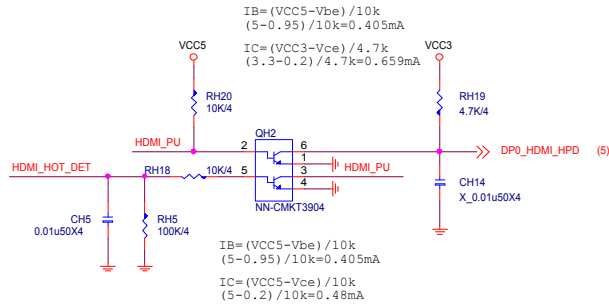
# AUX Level Shifter



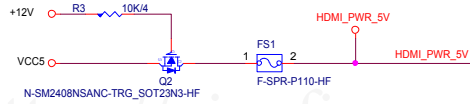
# Connector



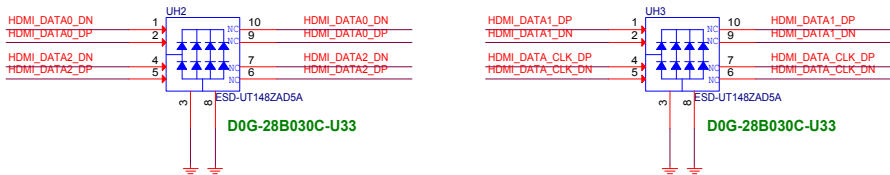
# HPD Circuit



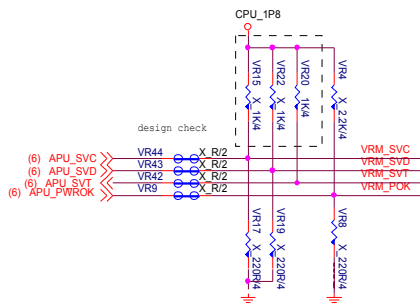
# Connector Power



# For EMI

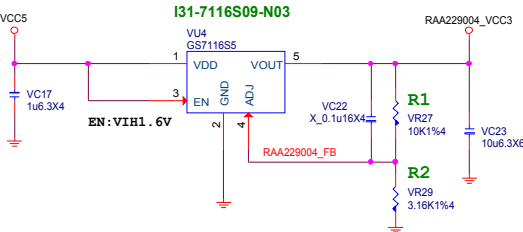
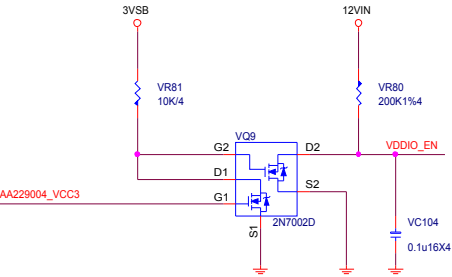
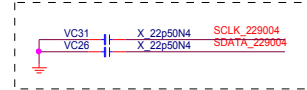
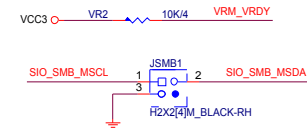


注意: 耐壓5V零件



Note: VID Override Circuit

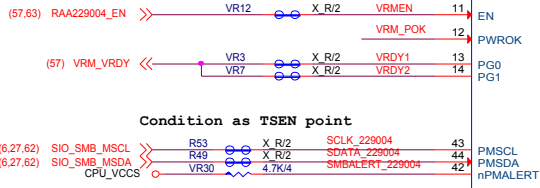
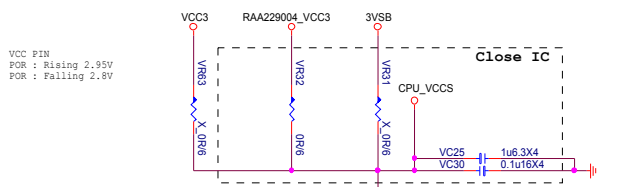
BOOT VOLTAGE		
SVC	SVD	Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



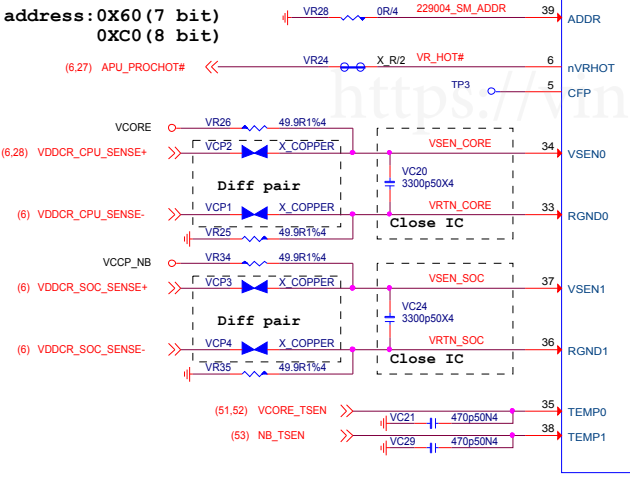
$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.8 * (1 + (10K/3.16K))$$

$$= 3.33V$$

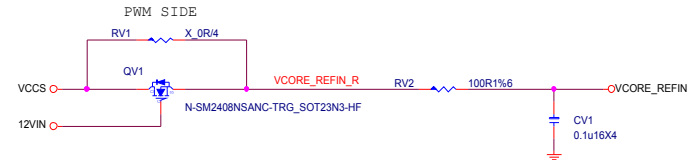
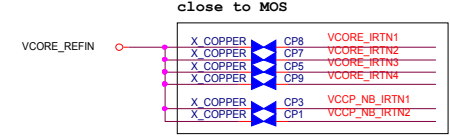


SMBUS address: 0X60 (7 bit)  
0XC0 (8 bit)



<https://www.vinafix.com>

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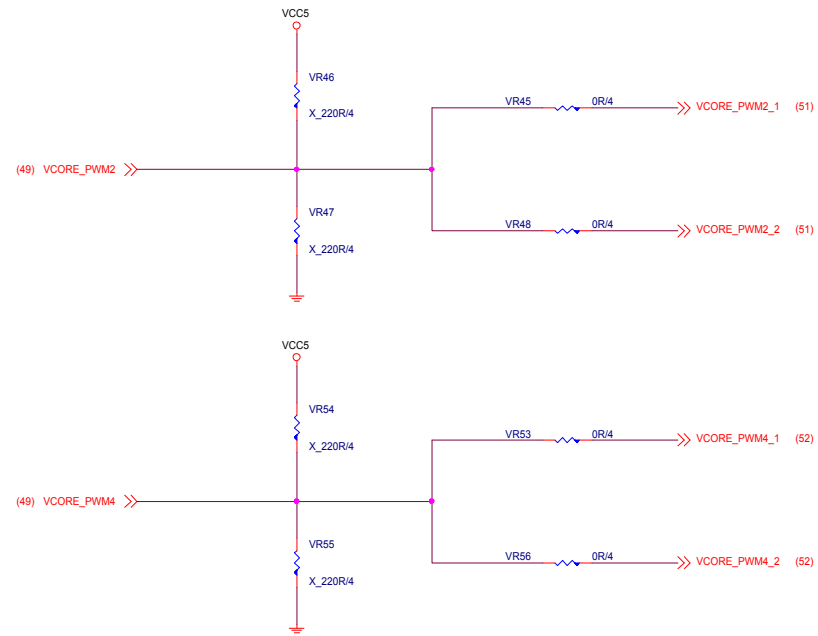
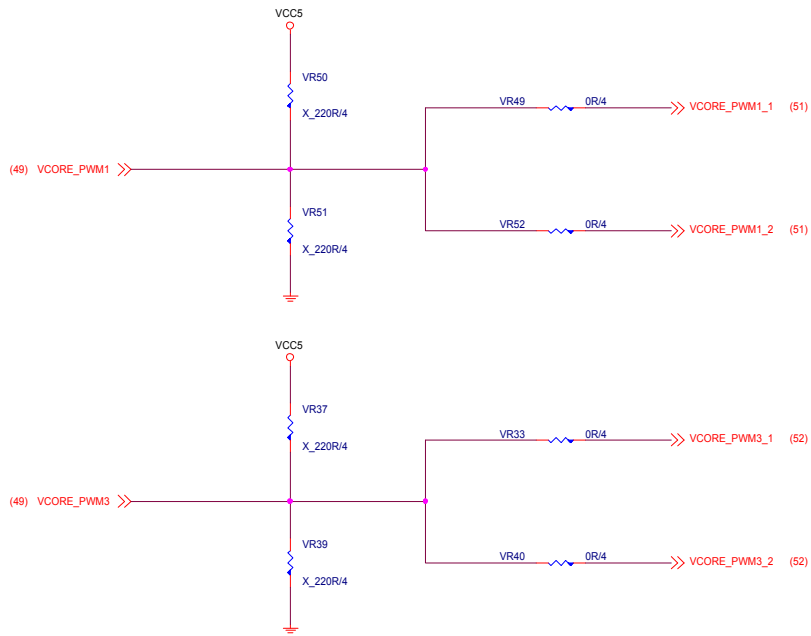
VCORE: ICCMax 140A  
LL: 1.3mohm  
OCP: 400A  
  
SOC: ICCMax 75A  
LL: 2.1ohm  
OCP: 100A




<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>CPU Power RAA229004 8+2</b>	Rev 1.0
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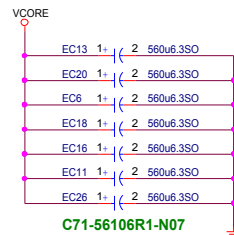
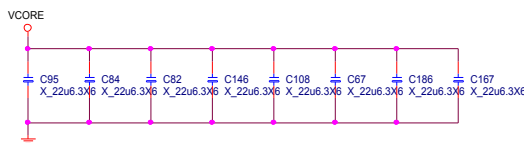
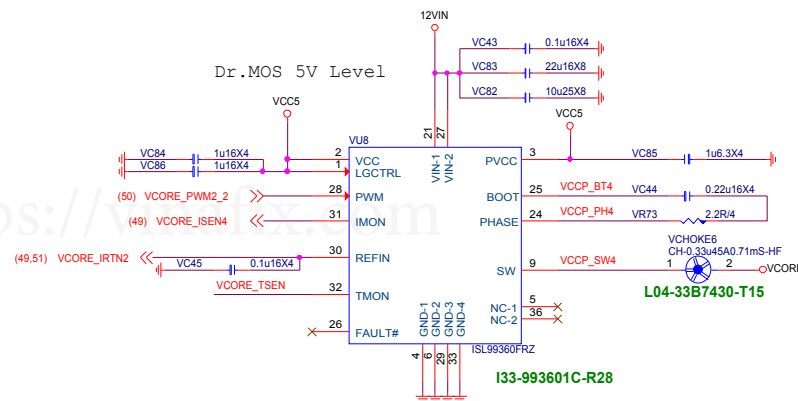
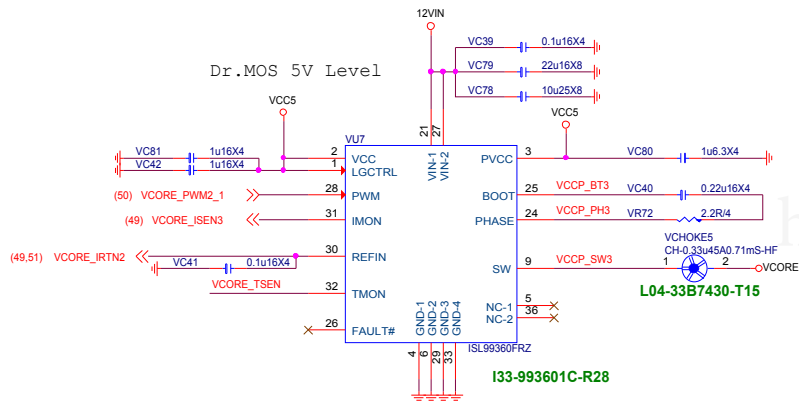
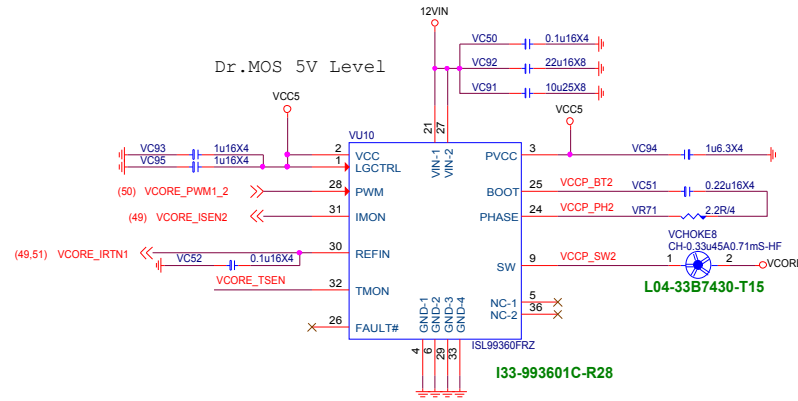
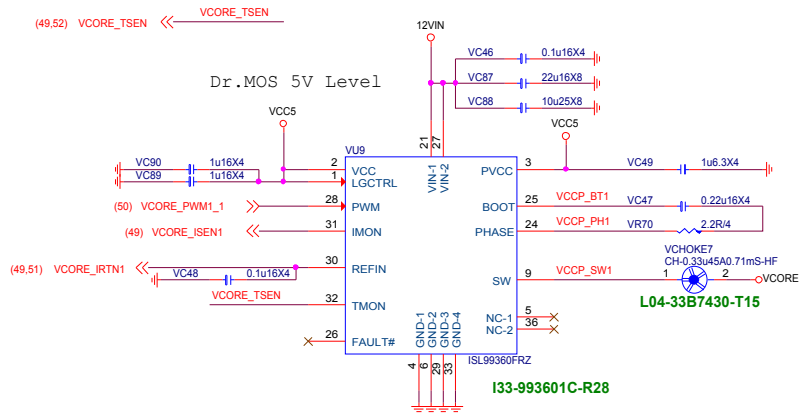
# CPU\_CORE Driver IC

## VCORE Double 8-PHASE

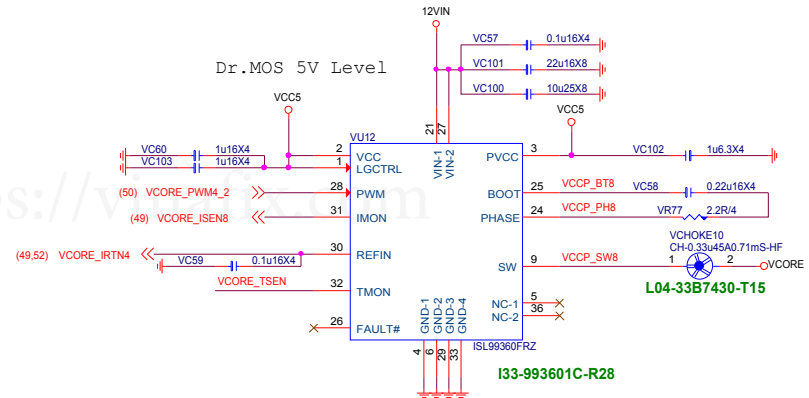
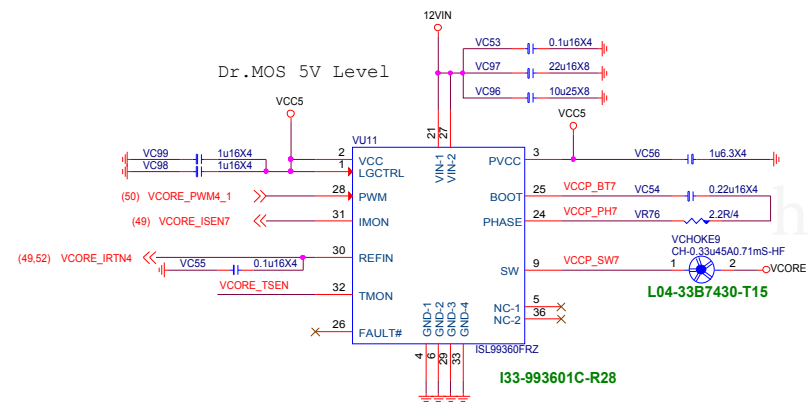
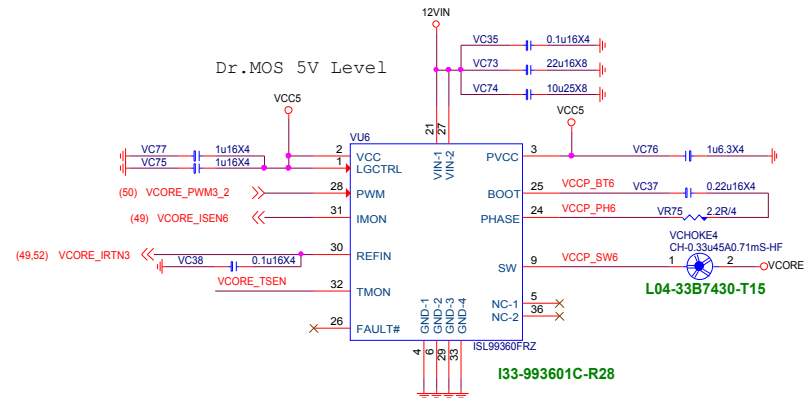
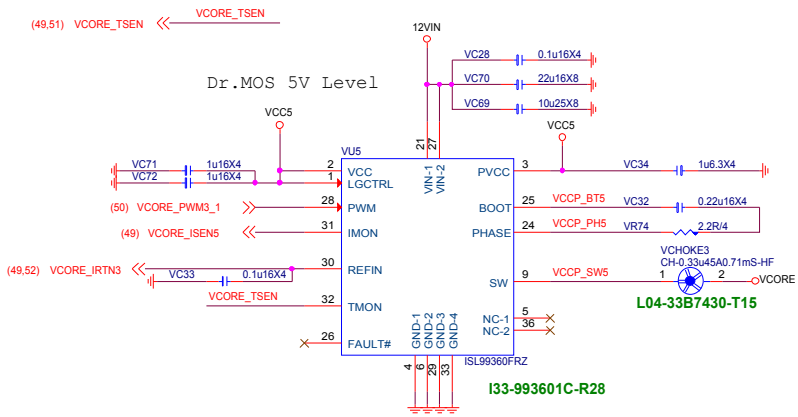


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	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7C94</b>		
Size Custom	Document Description <b>CPU PWR ISL6617A Extend</b>	Rev 1.0	
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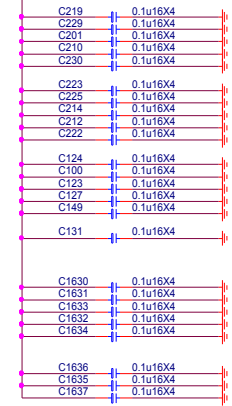
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size	Document Description	Rev
Custom	CPU Power Vcore Phase 1 - 4	1.0
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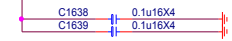
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>CPU Power Vcore Phase 4 - 8</b>	Rev 1.0
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VCORE



VCCP\_NB



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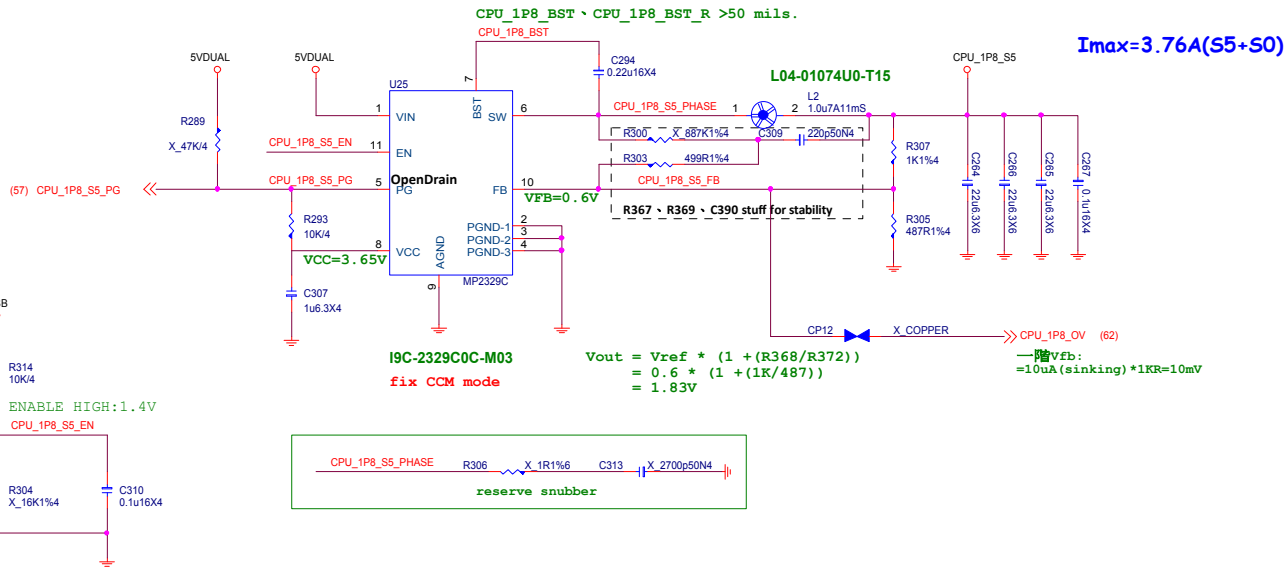


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>CPU Power NB_S5</b>	Rev 1.0
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# CPU 1.8V S5

CPU\_1.8V → 2A  
 CPU\_VDDP\_S5 → 1A  
 VDD\_1.8V\_S5 → 0.5A  
 CHIP\_1.8V\_S5 → 0.1A  
 AUDIO1.8V → 0.25A

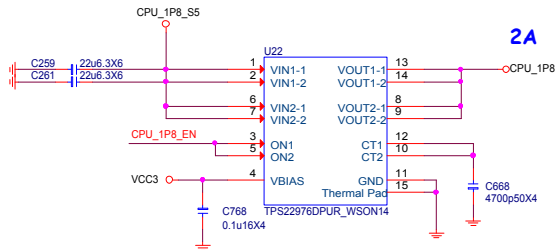
Continuous Conduction Mode (CCM)



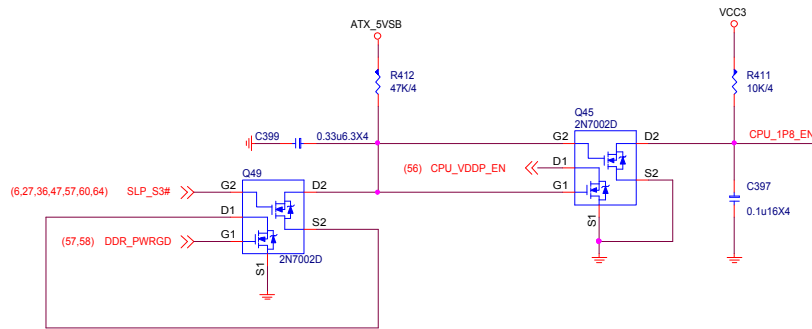
# CPU 1.8V S0

CPU 1.8V\_S0@2A

<https://vinafix.com>



Adjustable Rise Time  
 $SR = 0.42 * CT + 66$   
 SR is the slew rate in (μs/V)  
 CT is constant value on CT pin (in pF)  
 The units for the constant 66 is in (μs/V)

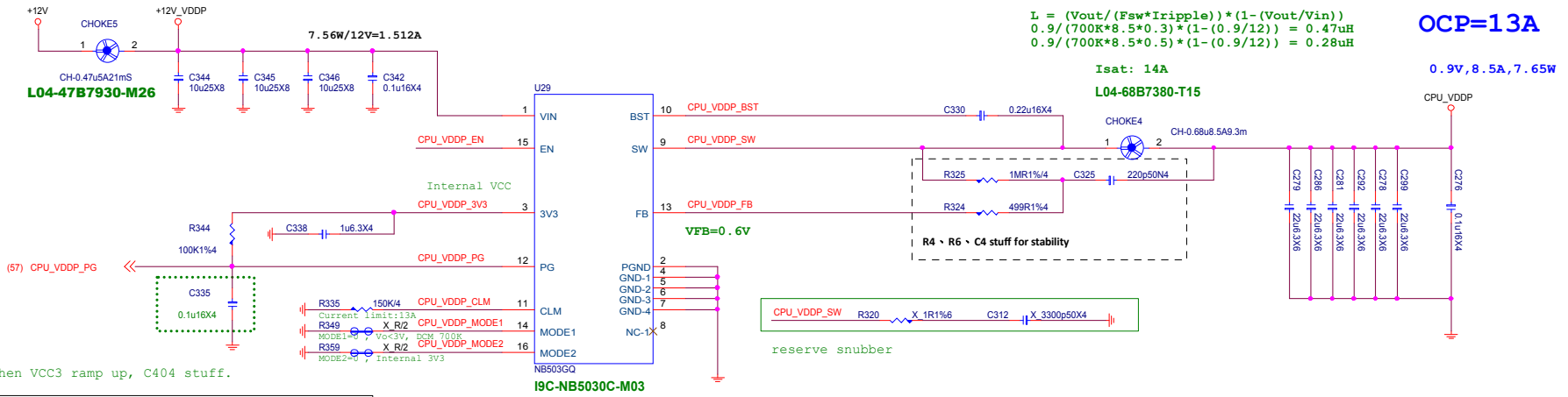


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>CPU Power 1.8 S0 / S5</b>	Rev 1.0
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# CPU\_VDDP\_S0

0.9V@S0:8.5A  
S0:8.5A

Input Current =  $(13A \cdot 0.9V) / 12V / 0.8 = 1.22A$   
 Choke Isat = 8A  
 $I_{rms} = I_{out} \cdot \sqrt{((V_o/V_i) \cdot (1 - (V_o/V_i)))}$   
 $= 13 \cdot \sqrt{(0.9/12) \cdot (1 - (0.9/12))} = 3.42A$   
 Choke Irms = 5A



$$I = (V_{out} / (F_{sw} \cdot \text{Tripple})) \cdot (1 - (V_{out} / V_{in}))$$

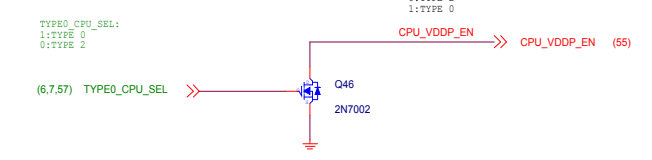
$$0.9 / (700K \cdot 8.5 \cdot 0.3) \cdot (1 - (0.9 / 12)) = 0.47 \mu H$$

$$0.9 / (700K \cdot 8.5 \cdot 0.5) \cdot (1 - (0.9 / 12)) = 0.28 \mu H$$

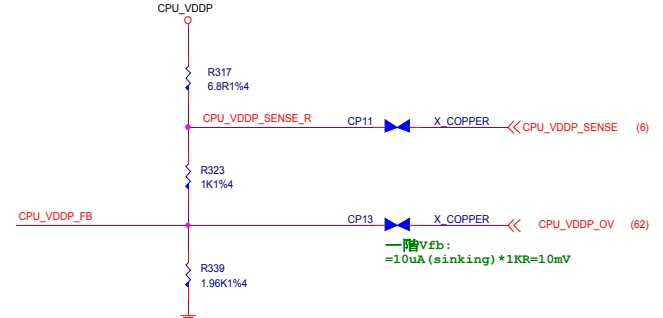
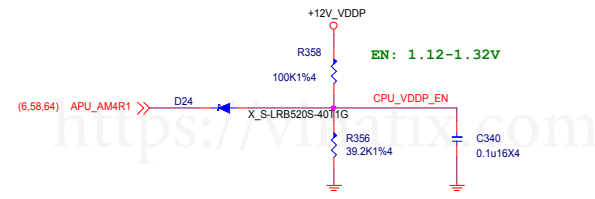
OCP=13A

20180822  
fix PG glitch when VCC3 ramp up, C404 stuff.

## No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN	
BR	0	1	0	1	SPEC no Support
NA	<del>1</del>	0	0	0	
SR	2	1	1	0	NOT SUPPORT TYPE2
RV/ZP	3	0	1	1	
MTS	4	1	1	1	NOT SUPPORT TYPE4



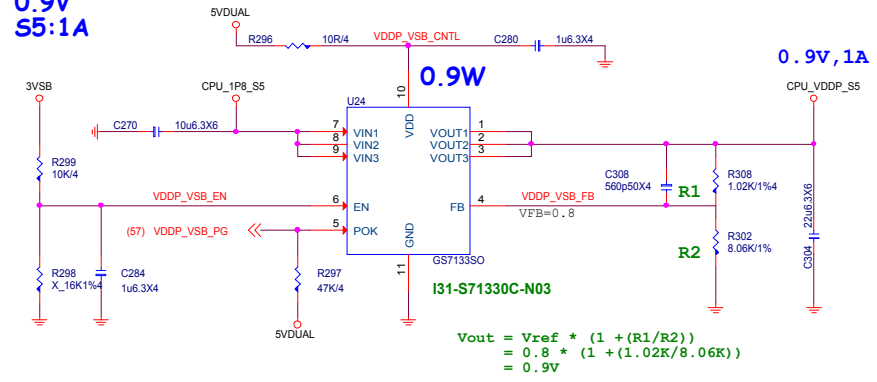
$$V_{out} = V_{ref} + (R1 \cdot R4 \cdot V_{ref}) / (R2 \cdot (R1 + R4))$$

$$= 0.6 + (1k \cdot 1000k \cdot 0.6) / (1.96k \cdot (1k + 1000k))$$

$$= 0.9058V$$

# CPU\_VDDP\_S5

0.9V  
S5:1A



$$V_{out} = V_{ref} \cdot (1 + (R1/R2))$$

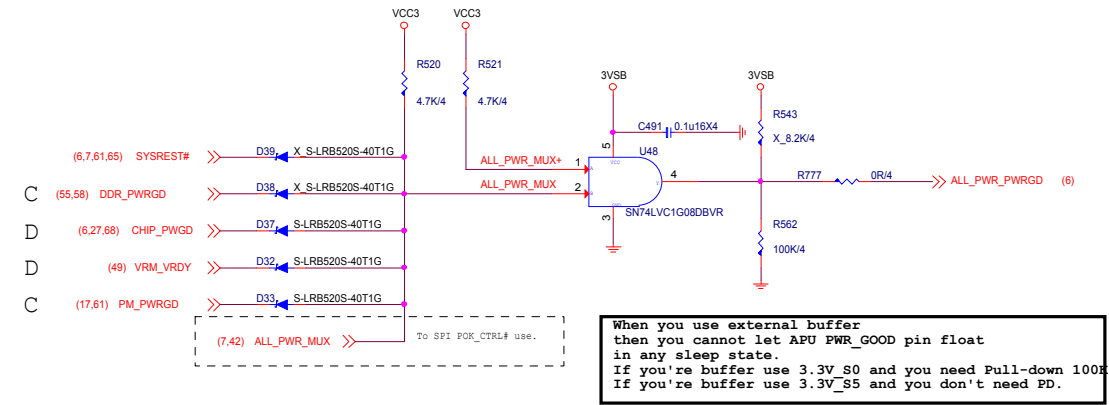
$$= 0.8 \cdot (1 + (1.02K/8.06K))$$

$$= 0.9V$$

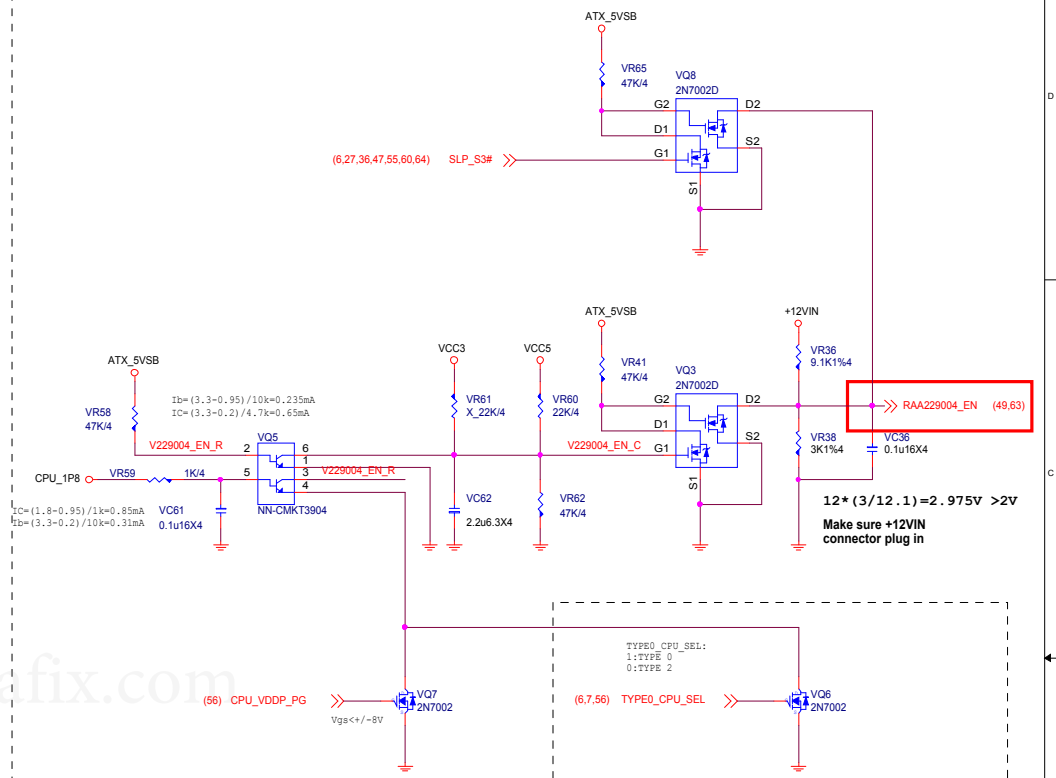
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size	Document Description	Rev
Custom	CPU Power VDDP-NB503/GS7133	1.0
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# ALL POWER GOOD MUX

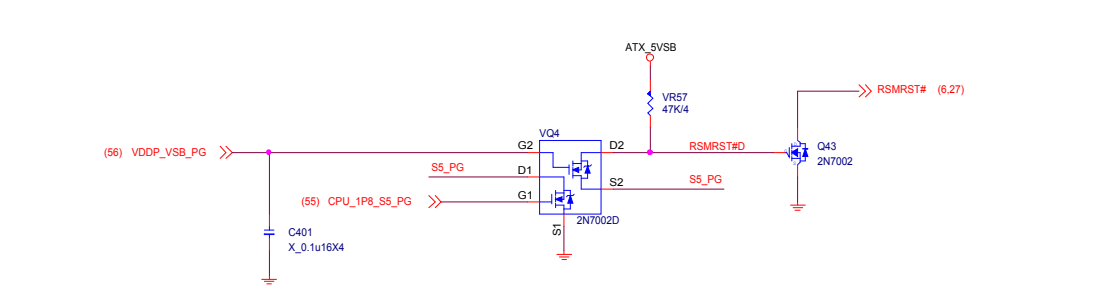
## S0 PG



# VRM\_Enable circuit



## S5 PG



SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

CPU VDDP NOT SUPPORT TYPE4

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

# DDR4\_1.2V@28.7A

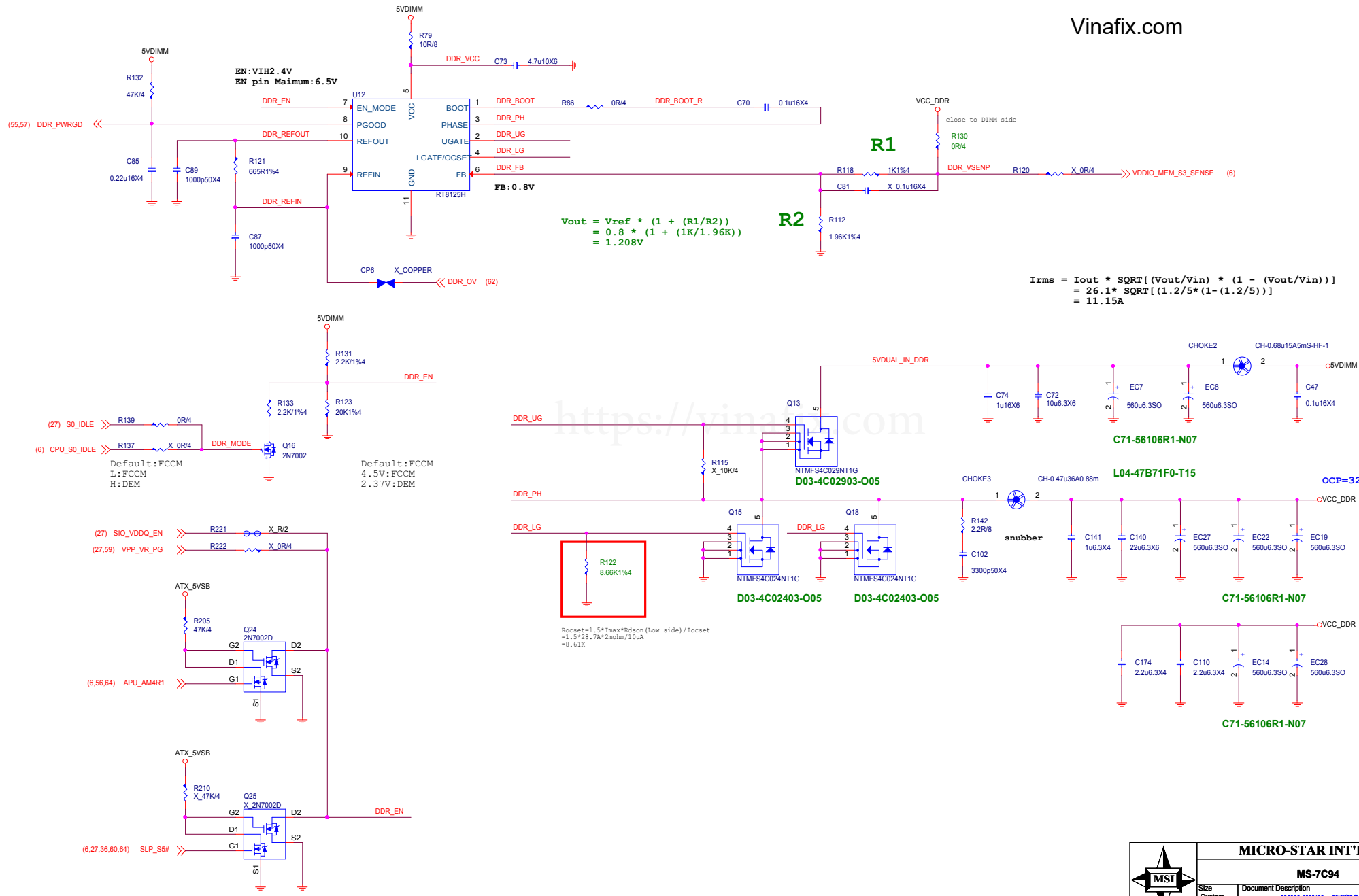
18A FOR CPU  
9.5A FOR 4DIMM  
1.2A FOR DDR VTT

OCP = 39.3A; Choke Isat=42A

Rocset =  $1.5 * I_{max} * R_{dson(Low)} / I_{ocset}$   
R649 =  $1.5 * 28.7 * 2m\Omega / 10\mu A$   
R649 = 8.61K

Rdson(Low Side) 5V  
D03-4C02403-O05:3.3 ~ 4mohm

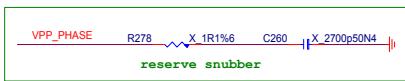
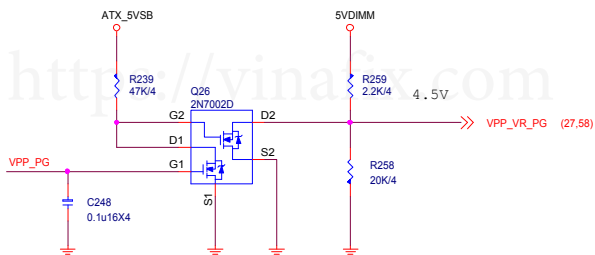
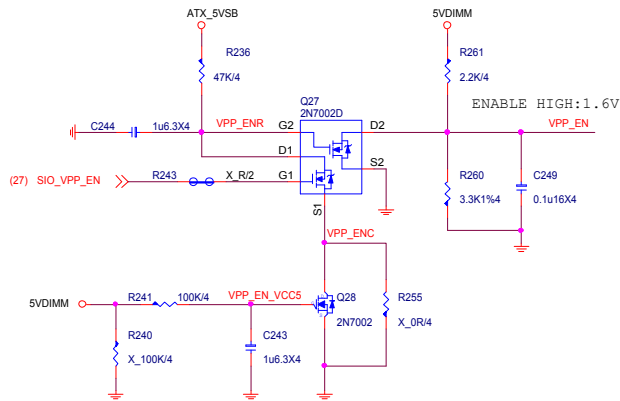
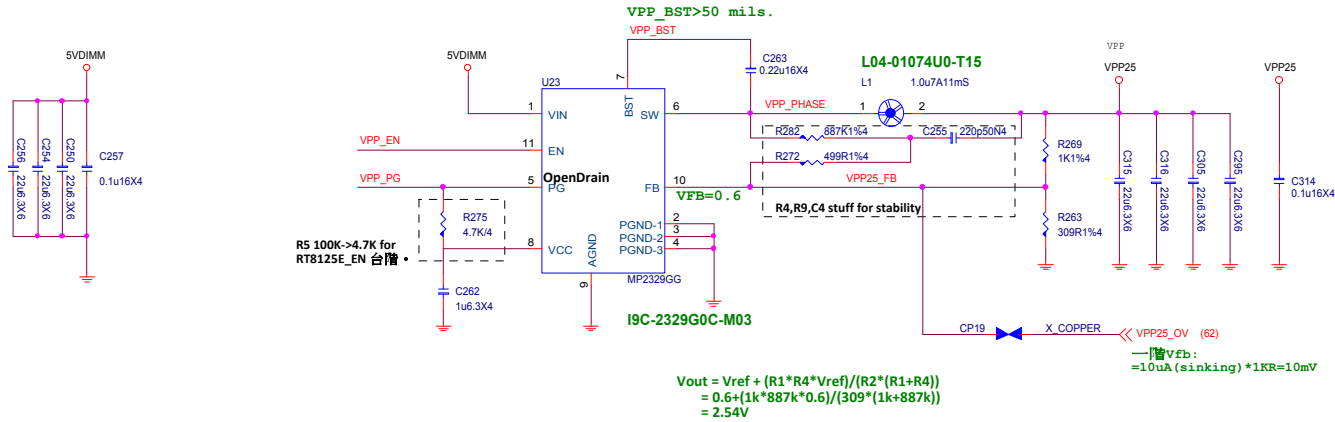
Vinafix.com



<b>MSI</b>		
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size	Document Description	Rev
Custom	<b>DDR PWR - RT8125E</b>	1.0
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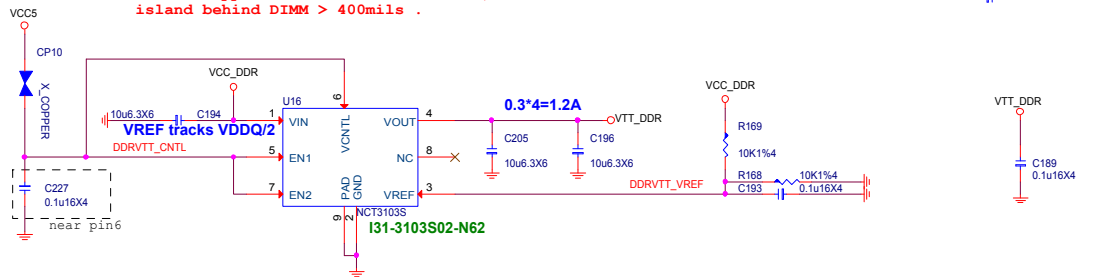
# 4DIMM : VPP25

2.5V@2.24A



## DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.



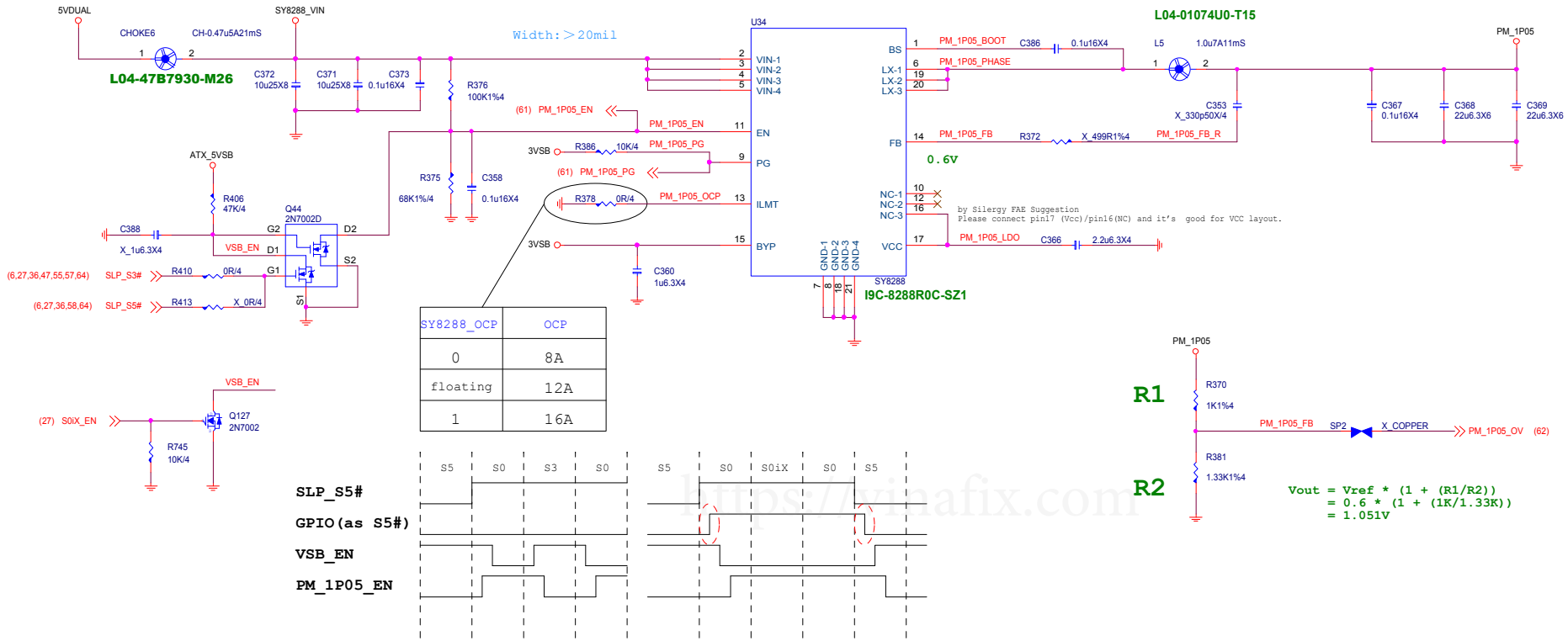
# FOR Promontory 1.05V\_S0

1.05V  
S0: 5.5A

Input Current =  $(5.5A * 1.05V) / 12V / 0.8 = 0.625A$

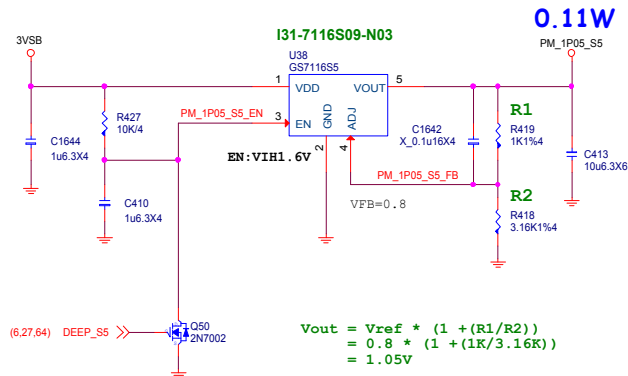
OCP=8A

1.05V@5.5A



# FOR PROM PM\_1P05\_S5

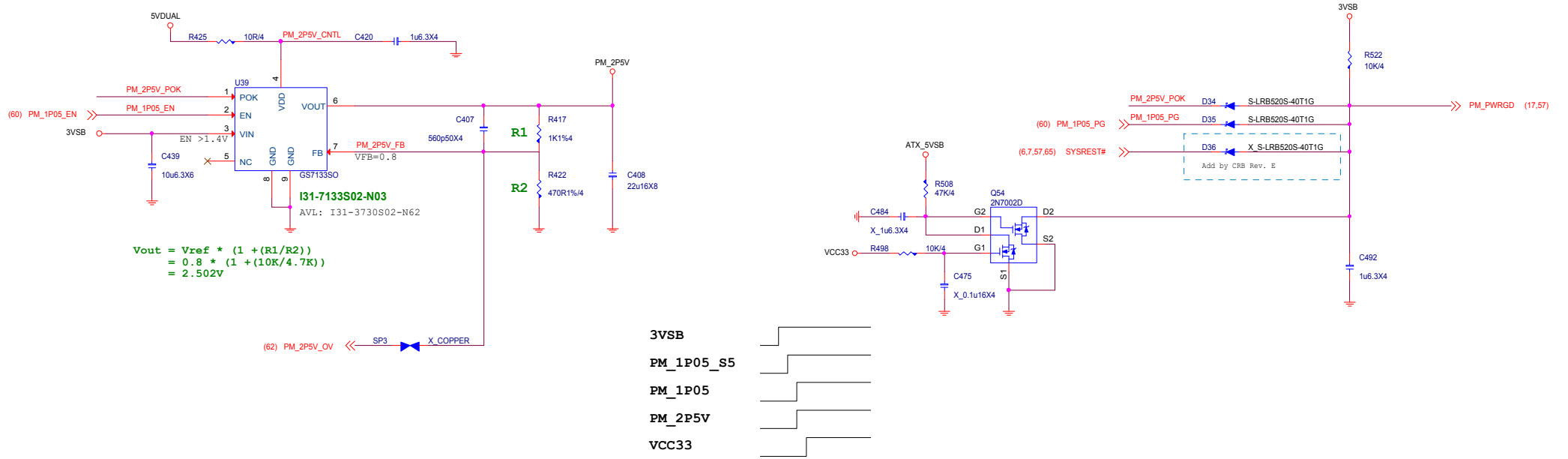
1.05V@0.05A



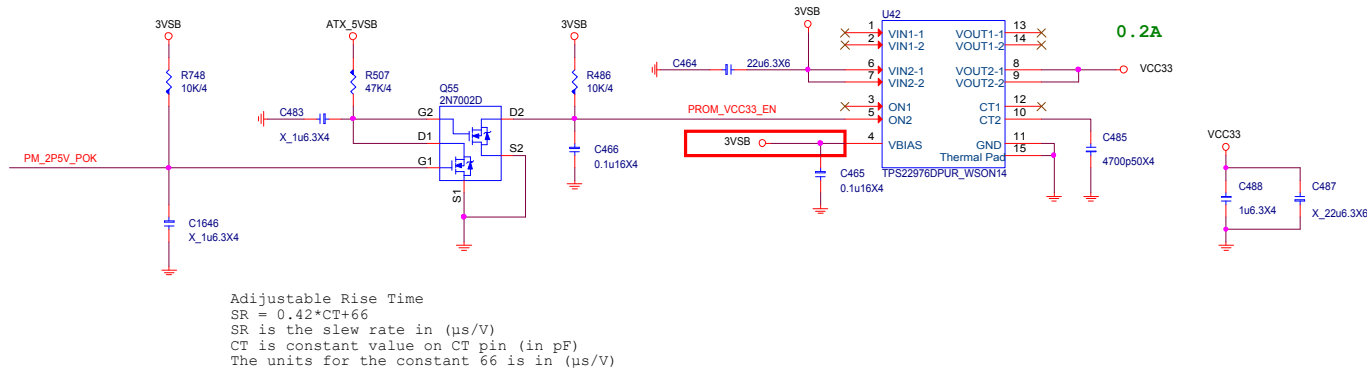
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>PM - SY8288/PM_1P05</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 60	of 76

# Promontory-2.5V

2.5V@900mA



## VCC33 VCC33@0.2A

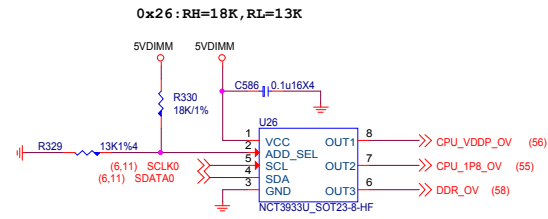
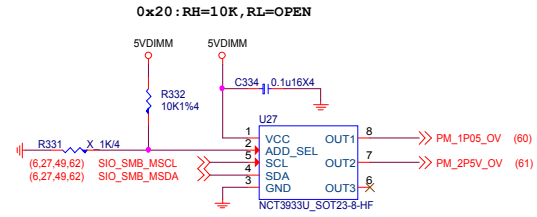
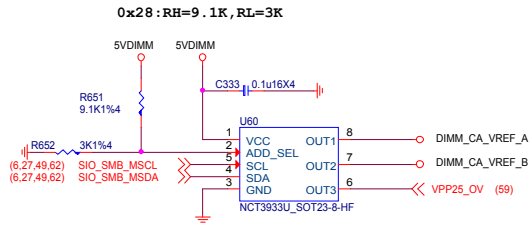
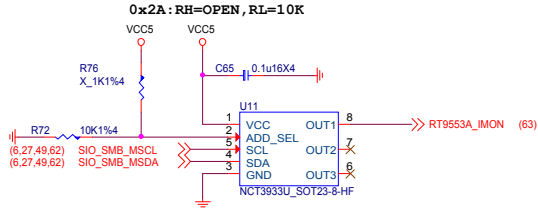


<https://vinafix.com>

# Over Voltage Control IC

## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



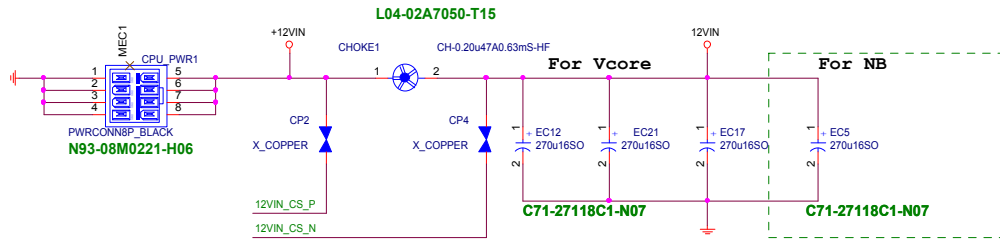
<https://vinafix.com>

Vinafix.com

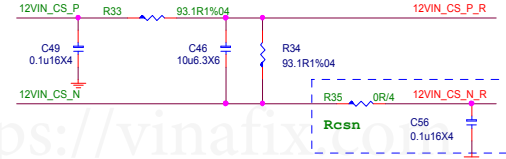
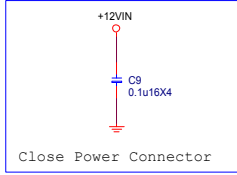


<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>OV Control - NCT3933</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 62	of 76

# CPU POWER CONNECTOR

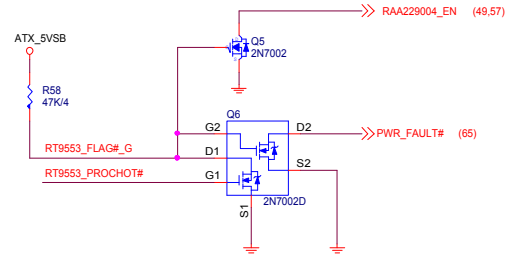
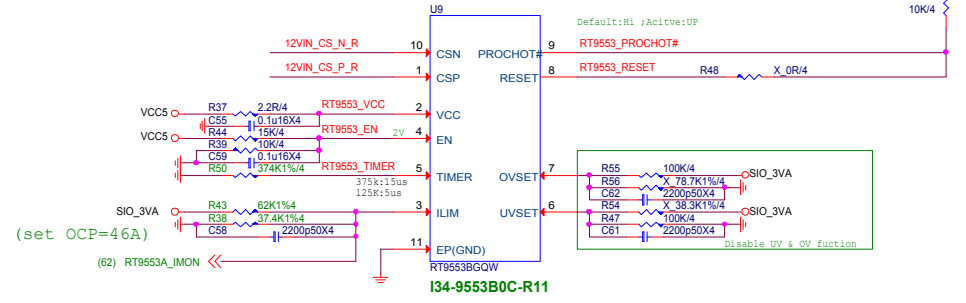


Vcore		SOC	
D = Vout/Vin		D = Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple = {Io*sqrt(D)*sqrt(1-D)} / Phase		I ripple = {Io*sqrt(D)*sqrt(1-D)} / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.



# RT9553B CURRENT SENSE

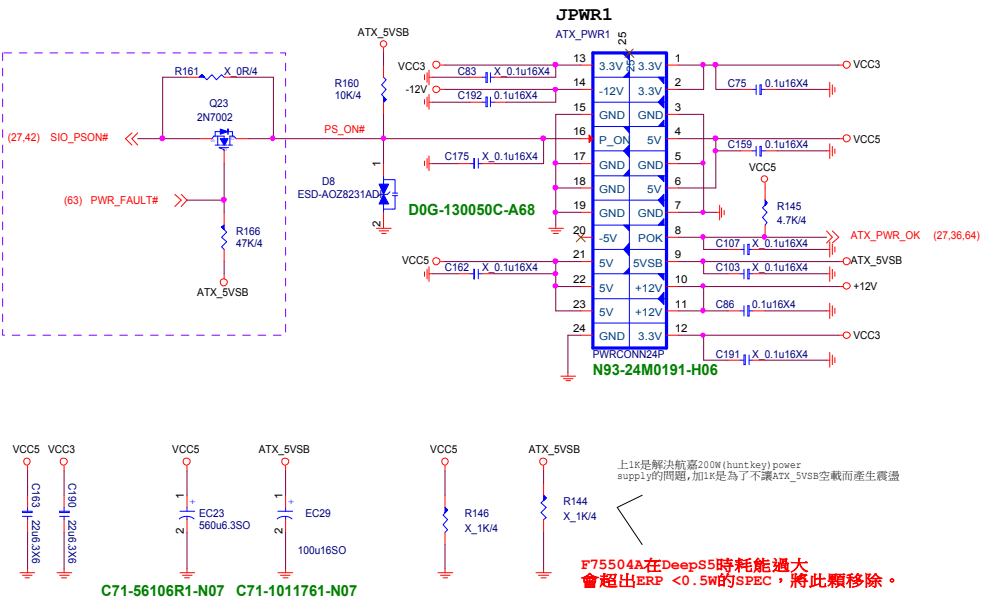
RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.



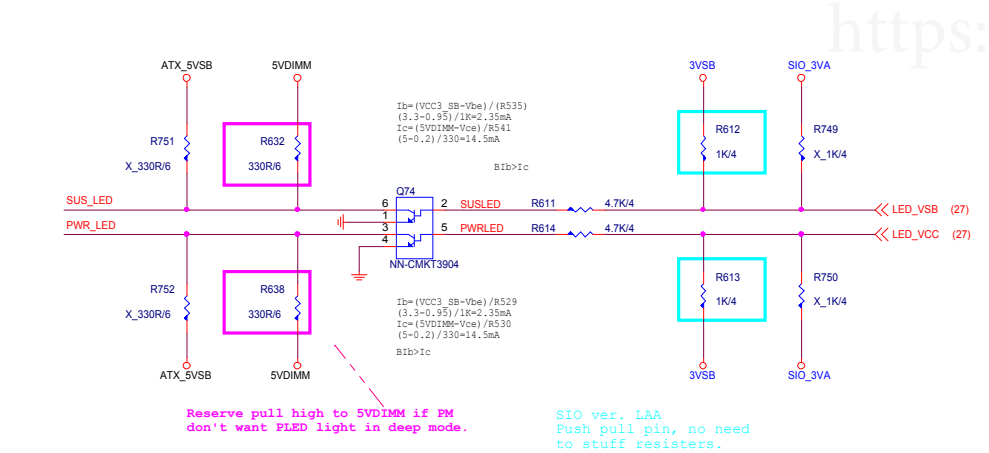
<https://vinafix.com>



# ATX POWER CONNECTOR

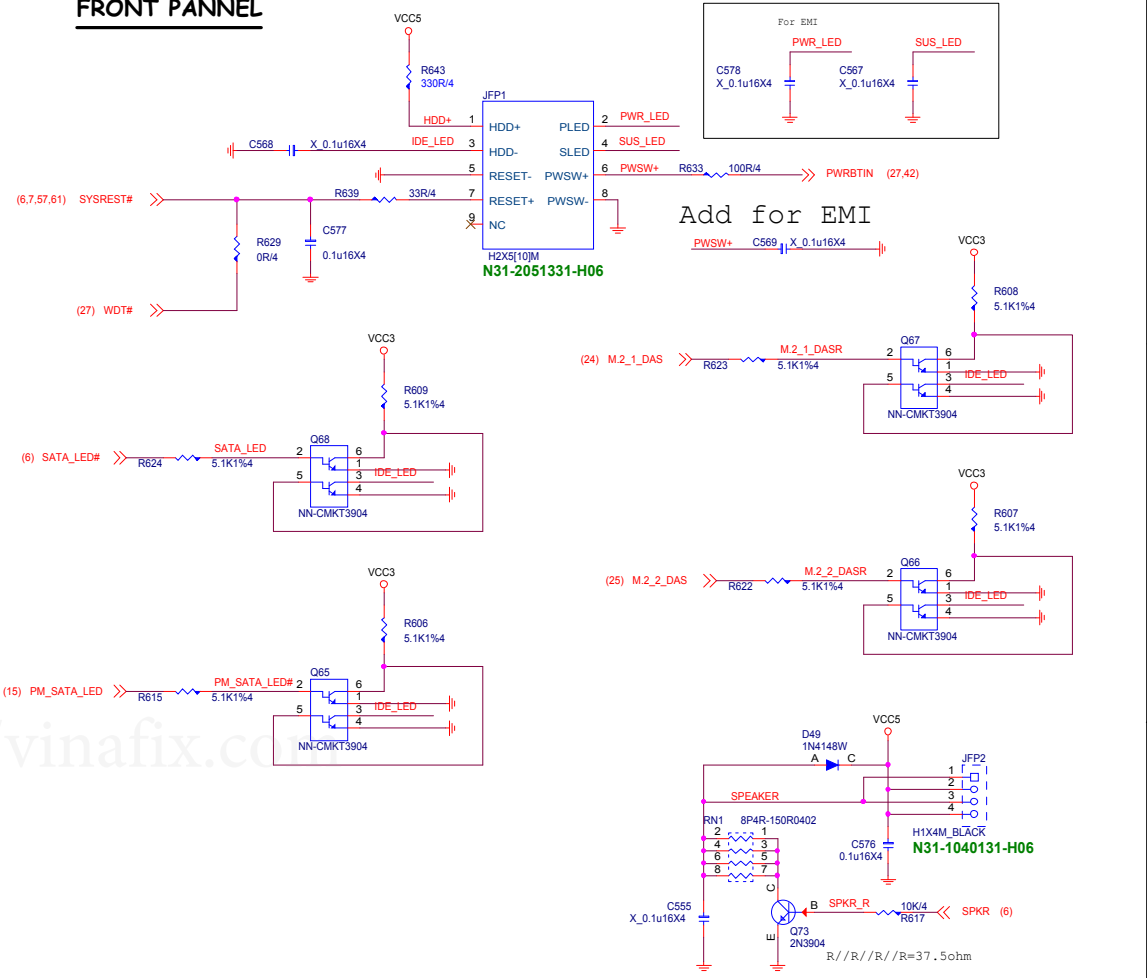


# LED ( for NCT6797D)



# TPM

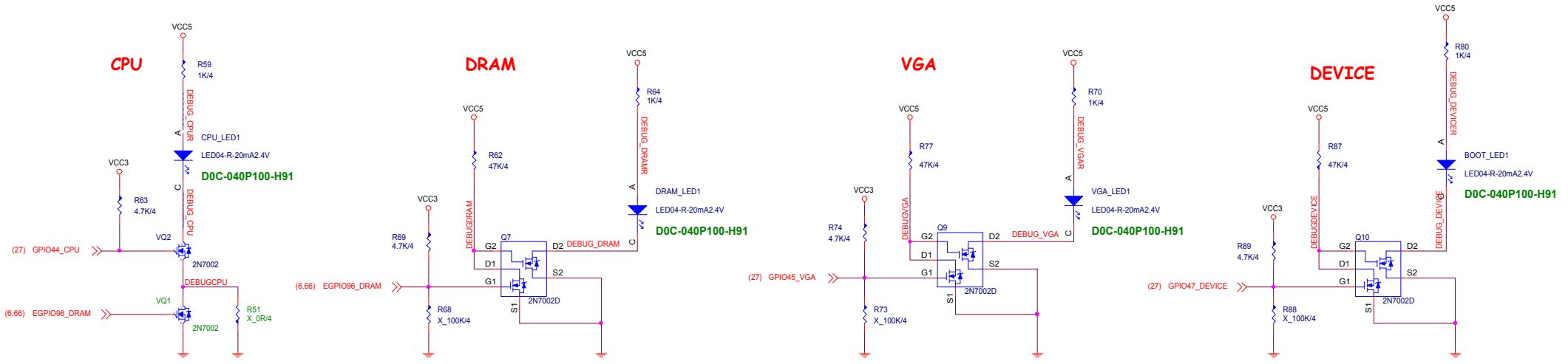
# FRONT PANNEL



# Voltage Mearsure Point

<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>ATX Power - FrontPanel / EMI</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 65	of 76

# EZ Debug LED



LEDGPIO	GPIO46	EGPIO96	GPIO44	GPIO13	default Input
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW	
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain	

LED亮燈時同時將CPU LED關掉


## DIMM\_SLOT FORM SIO

DOC-040P100-H91/DOC-040S500-E07

<https://vinafix.com>

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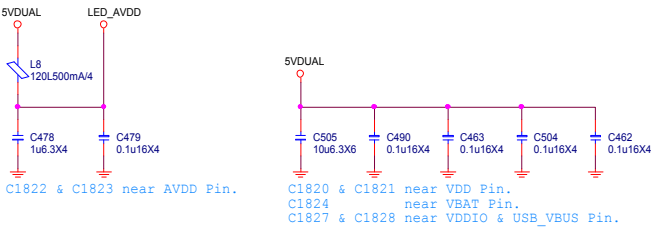
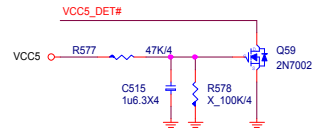
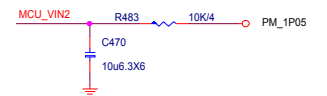
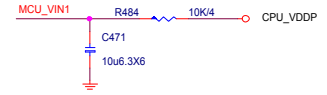
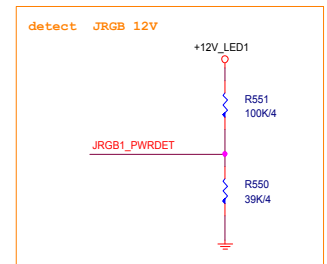
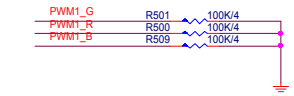
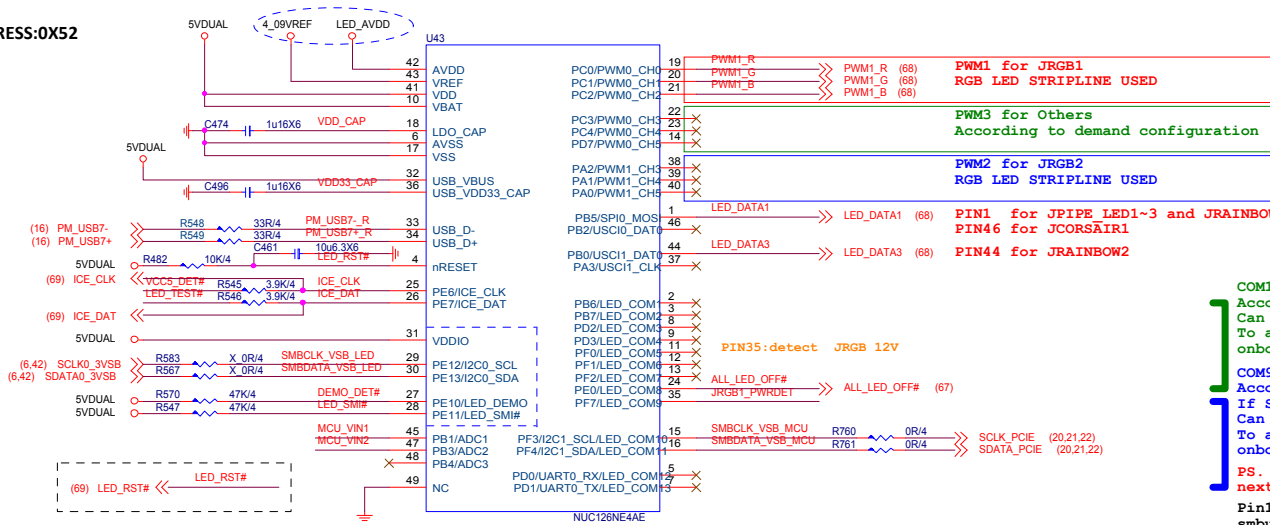
## AMD AMP Detect LED

	<b>MICRO-STAR INT'L CO.,LTD</b>	
	<b>MS-7C94</b>	
Size Custom	Document Description <b>LED - EZ DEBUG / AMP</b>	Rev 1.0
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# 48 PIN LED MCU

If you use ADC function, need to separate VREF from AVDD and 4\_09VREF stuff for VREF.

ADDRESS:0X52



COM1-8 for PWM3  
According to demand configuration.  
Can configuration COM1-8,  
To achieve 8 group Non-synchronized  
onboard LED control.

COM9-13 for PWM2  
According to demand configuration.  
If SPEC. don't have JRGB2,  
Can configuration COM9-13,  
To achieve 5 group Non-synchronized  
onboard LED control.

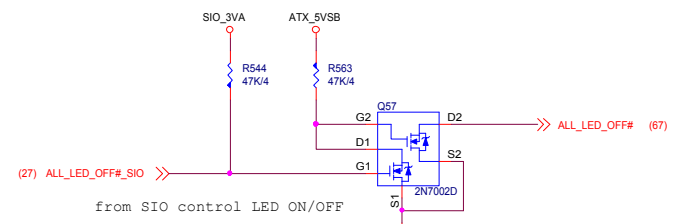
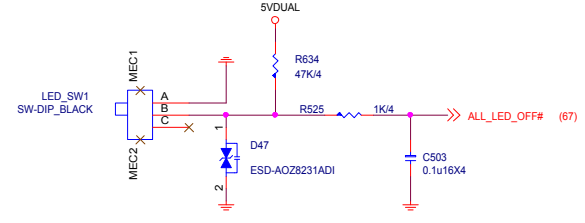
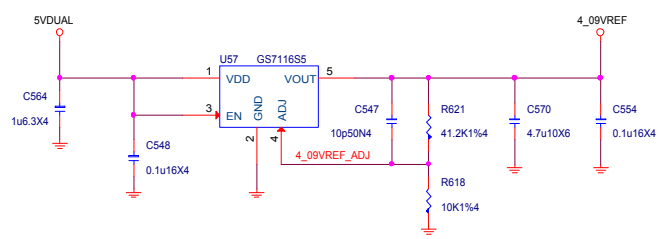
PS. COM1 is the first action block,  
next is COM2, and so on.

Pin15,16 can configure to master  
smbus if spec requirement.

<https://vinafix.com>

## LED SW1 for ALL LED OFF

B-C: LED ON(default)  
B-A: LED OFF

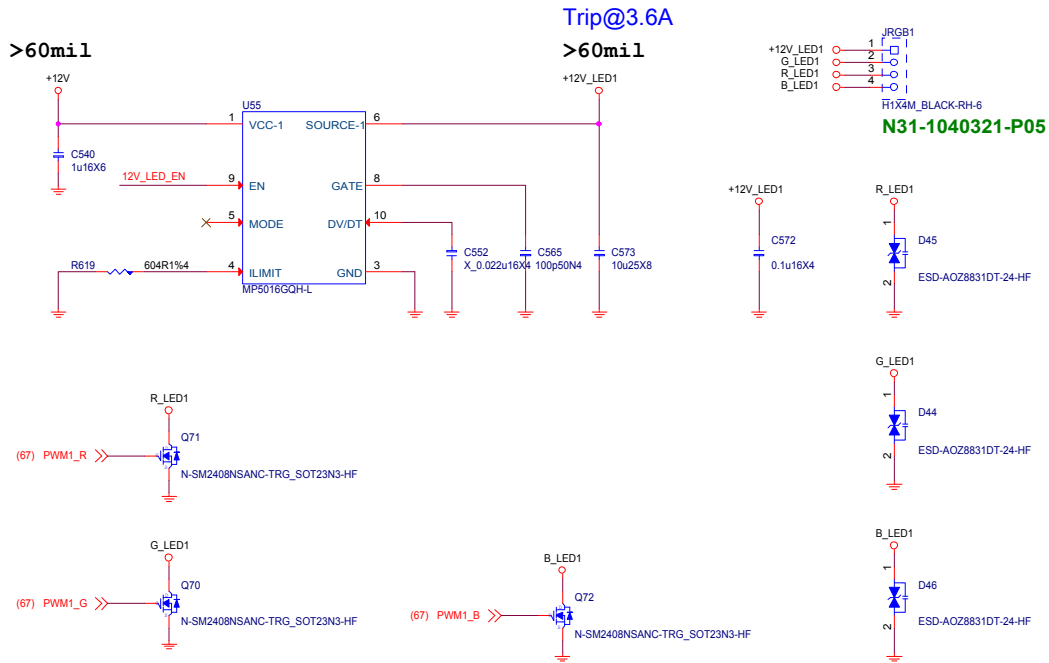


Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-13	PWM2



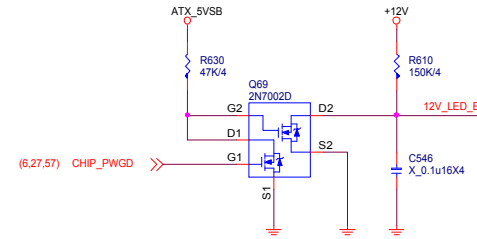
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>MCU - LED Control</b>	Rev 1.0
Date: Tuesday, April 28, 2020	Sheet 67	of 76

### JRGB1



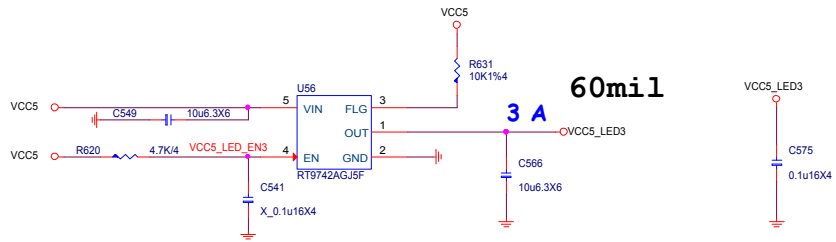
外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB2)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

### JRGB2

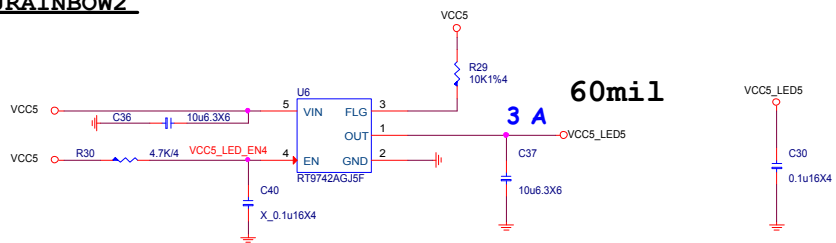


外接LED 燈條 (RGB )  
 ---- PCB 文字面 (JRGB2)  
 ---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

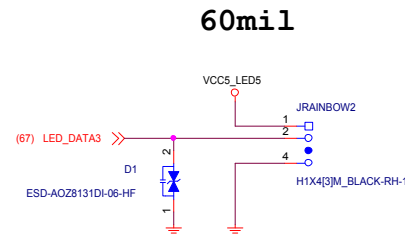
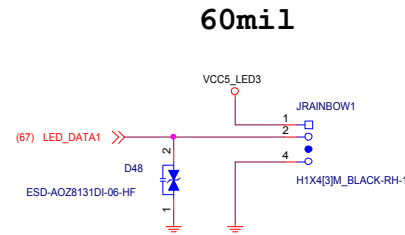
### JRAINBOW1



### JRAINBOW2



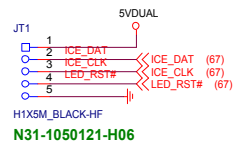
### JCORSAIR1



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7C94</b>		
Size Custom	Document Description <b>LED - JLED1/2/3/4</b>	Rev 1.0
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## JT1 for FW update

## EXTERNAL POWER INPUT



IF no JPWRLED1 & JPIPE\_LED spec  
MCU can powered by 5VDUAL directly.  
LED\_VCC5 replace with 5VDUAL.



## JF1 for Factory test

<https://vinafix.com>

	MICRO-STAR INT'L CO.,LTD		
	MS-7C94		
Size Custom	Document Description LED - JT1 / JF	Rev 1.0	
Date: Tuesday, April 28, 2020	Sheet 69 of 76		

<https://vinafix.com>

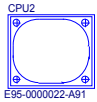


**MICRO-STAR INT'L CO.,LTD**

**MS-7C94**

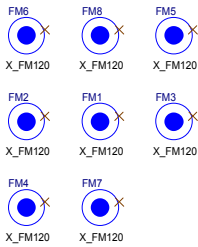
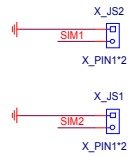
Size Custom	Document Description <b>BOM Option</b>	Rev 1.0
Date: Tuesday, April 28, 2020		Sheet 70 of 76

## CPU Socket

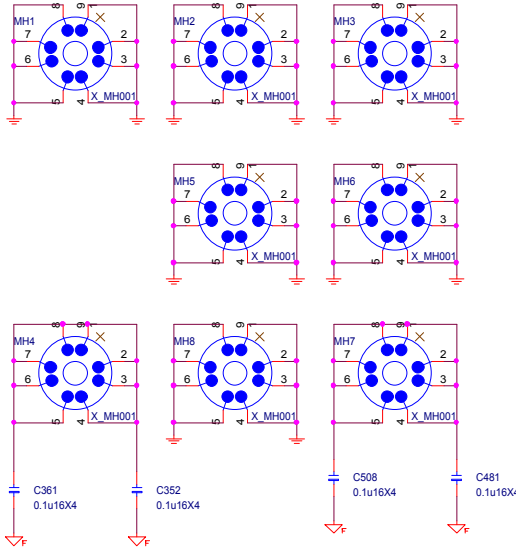


E95-000022-A91

## Simulation



## Optics Orientation Holes



## MANUAL PART

UEFI1  
G51-MTSPXXA-A09  
**G51-M1SPXXA-A09**

CFOS <MSI-BOM>  
Y02-MU00170-CFO  
**Y02-MU00170-CFO**

HDMI\_LA1  
**Label**  
HDMI  
X\_HDMI LABEL  
**Y01-RHDMI03-000**

NAHIMIC1 <MSI-BOM>  
X\_Y02-MU00100-NAH  
**Y02-MU00100-NAH**

MARKET1  
G51-M1SP79-Q13  
**G51-M1SP79-Q13**



BAT1\_X1  
BAT-BCR2032P

MARKET2  
X\_G51-M1SPQ03-Q13  
**G51-M1SPQ03-Q13**

## Moat CAP

## PCB

PCB



PD0-07C9410-G37

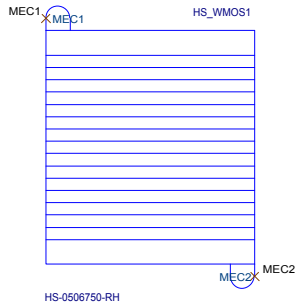
## PCH HEATSINK



HS-0410520-RH

HS\_PCH2  
X\_E31-0410500-A87

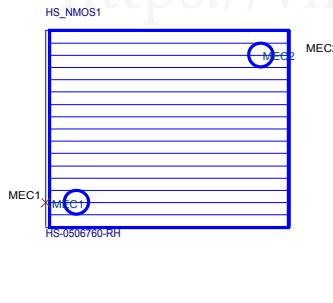
## MOS HEATSINK



HS-0506750-RH

HS\_WMOS2  
X\_E31-0506710-A87

## M.2 HEATSINK



HS\_NMOS2  
X\_E31-0506720-A87

M2\_HS1  
E31-0002680-A87

M2\_HS2  
X\_E31-0002630-A87

IO\_Shell1  
E21-7C94010-A91

IO\_Shell2  
X\_E21-7C94020-A91

## IO COVER

## DDR COVER

## Audio COVER