Discrete/UMA /Muxless Schematics Document

AMD LIANO CPU FS1

AMD GPU Manhattan(Park/Madison M2) and Vancouver(Seymour/Whistler M2)

<Variant Name>

緯創資通

Title	Cover Page	
Size A4	Document Number JE40-SB	Rev SB
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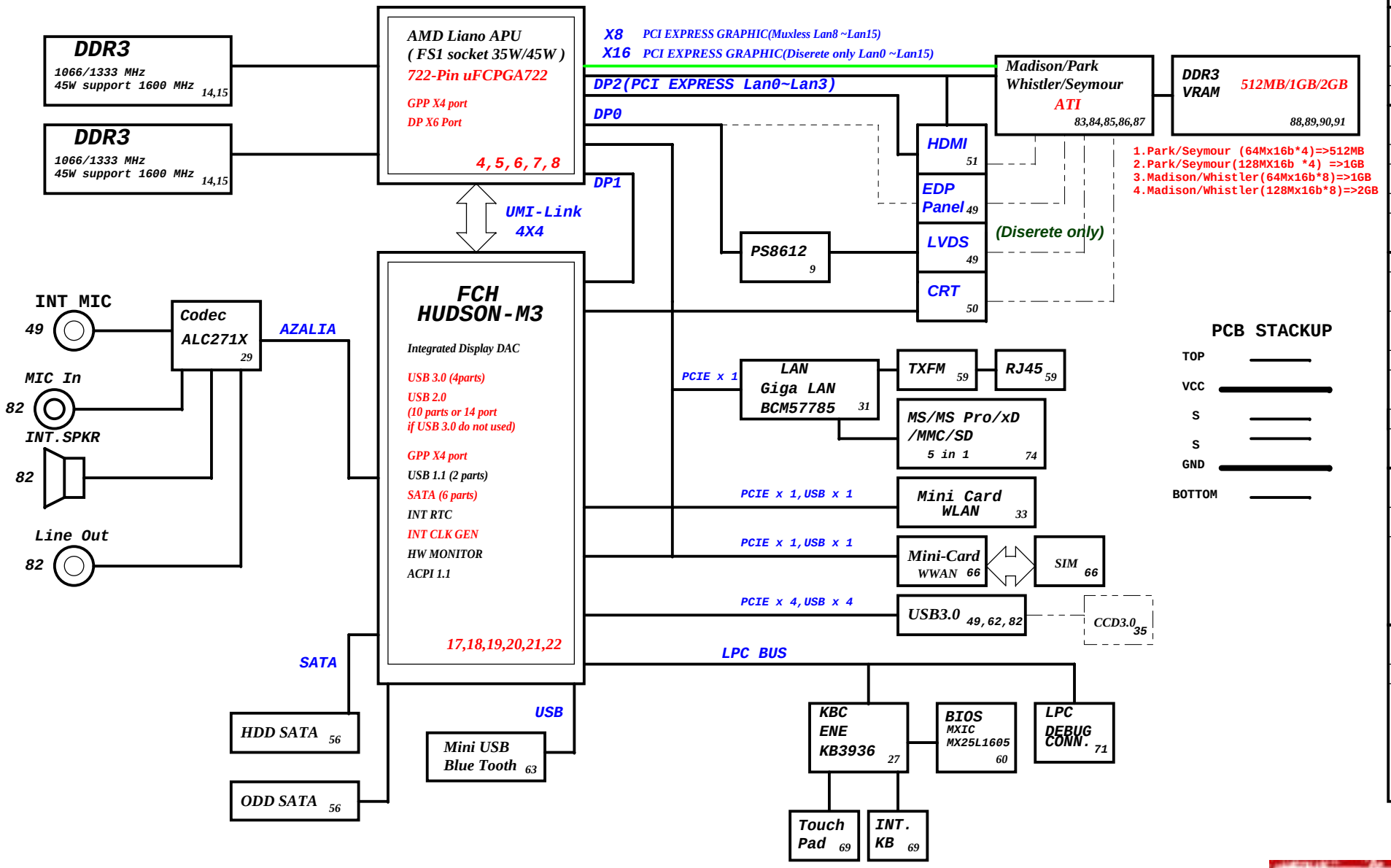
JE40-SB Block Diagram

JE40-SB Project code: 91.4PQ01.001
SJV40_SBM Project code:
SJV40_SBP Project code:



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
RT8239 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5.5A) 3D3V_S5(5A)

SYSTEM DC/DC
RT8207 44

5V_S5	1D5V_S3(15A)

RT8207 44

5V_S5	0D75_S0(1.2A)

SYSTEM DC/DC
RT8238 46

INPUTS	OUTPUTS
5V_S5	1D1V_S5(1.4A)

RT8238 45

5V_S5	1D2V_S0(5.2A)

RT9025 93

3D3V_S5	1D8V_VGA_S0
1D5V_S3	1V_VGA_S0

RT9025 48

3D3V_S0	2D5V_S0 (200mA)

RT8208 92

5V_S5	VGA_CORE

CHARGER
BQ24745 40

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC
ISL6267 42,43

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.55V 18A VDDNB 0~1.55V 4A

<Variant Nar

Title: Block Diagram

Size	Document Number	Rev
A3	JE40-SB	SB

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Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB 2.0(For SW Debug)
1	WLAN
2	NC
3	WWAN
4	BT
5	3G SIM Card
6	USB 2.0 Small BD
7	CCD
8	NC
9	NC
10	USB 3.0 CCD(Reserve)
11	USB 3.0 (M/B USB1)
12	NC
13	NC

PCIE Routing

	APU
LANE0	LAN + Cardreader
LANE1	WWAN
LANE2	WLAN
LANE3	

	FCH
LANE0	
LANE1	
LANE2	
LANE3	

<Variant Nar

Title: Table of Content

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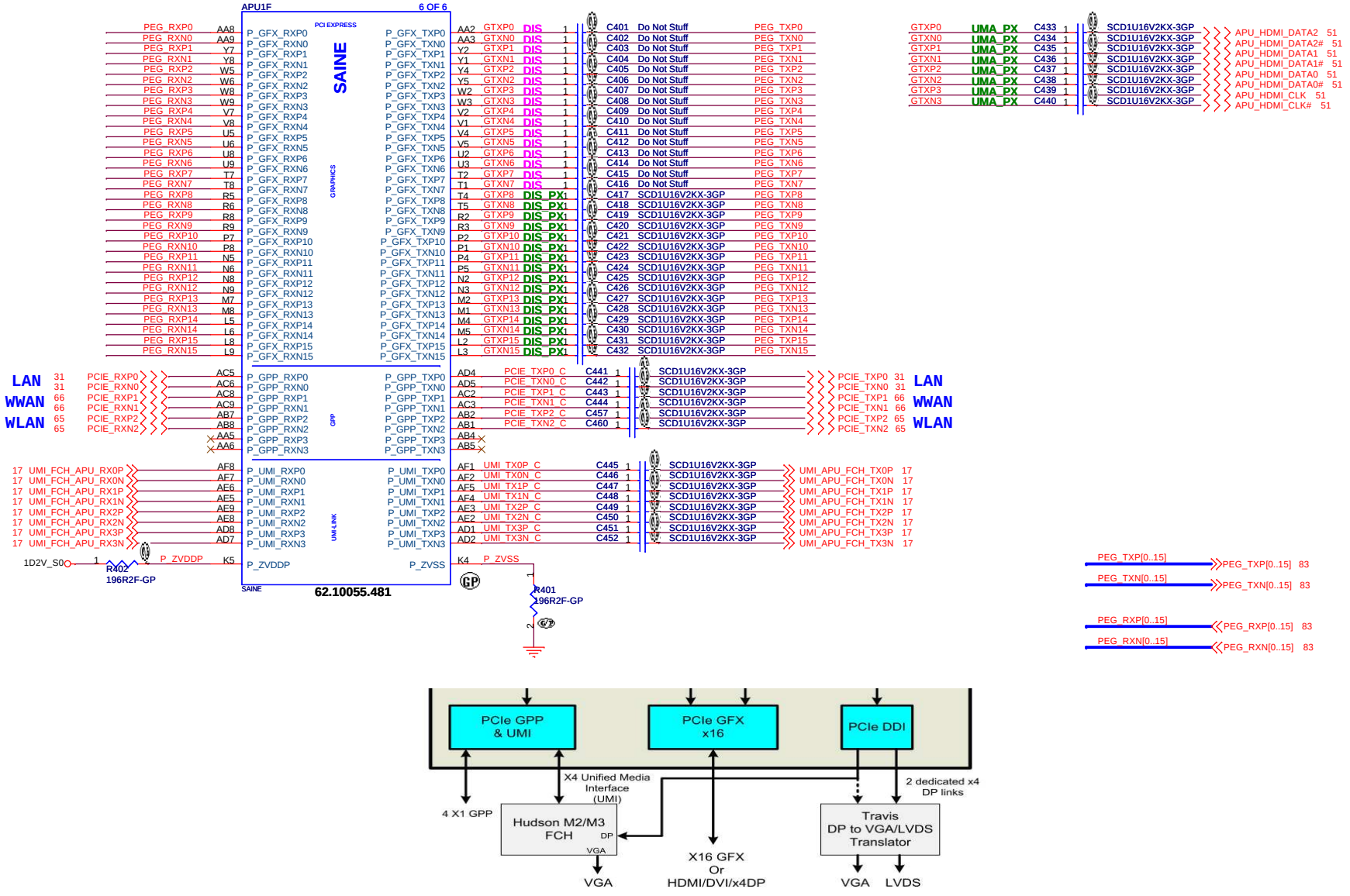

Title	APU_PCIE(1/5)
Size A3	Document Number JE40-SB
Rev	SB
Date:	Monday, March 28, 2011
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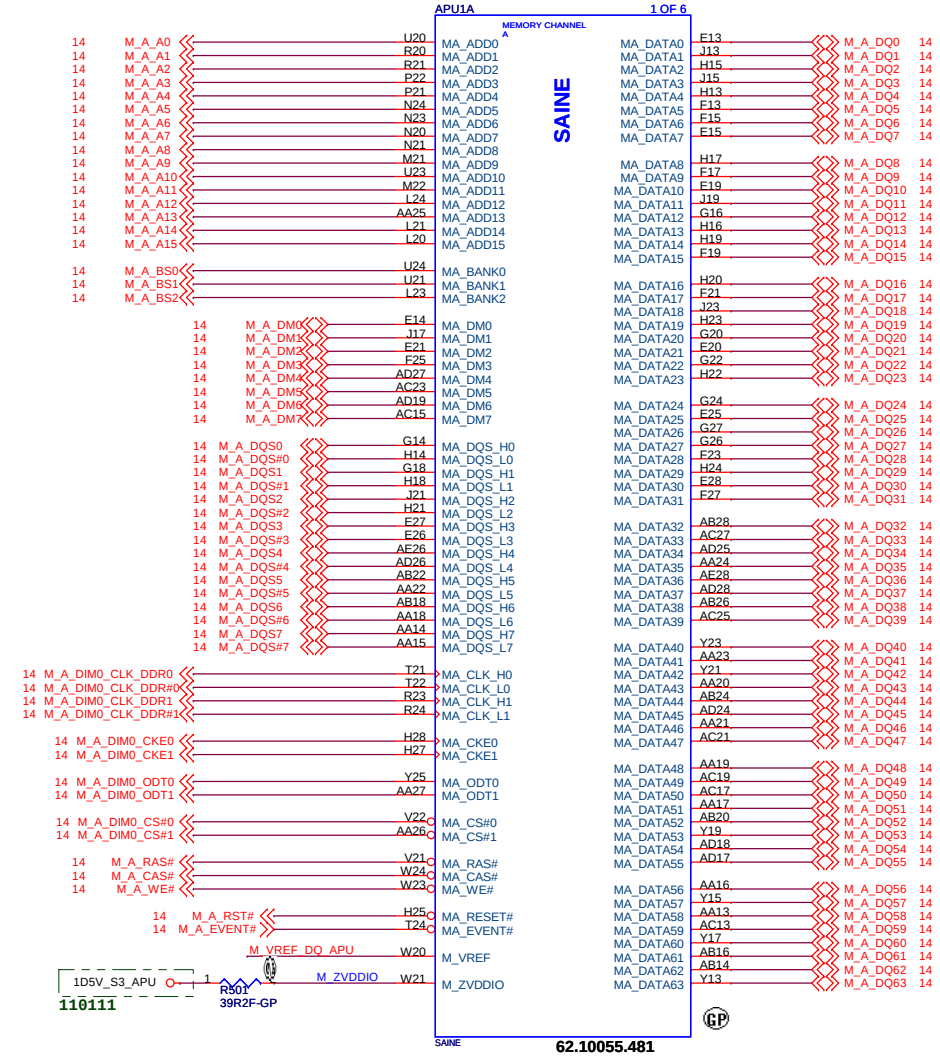
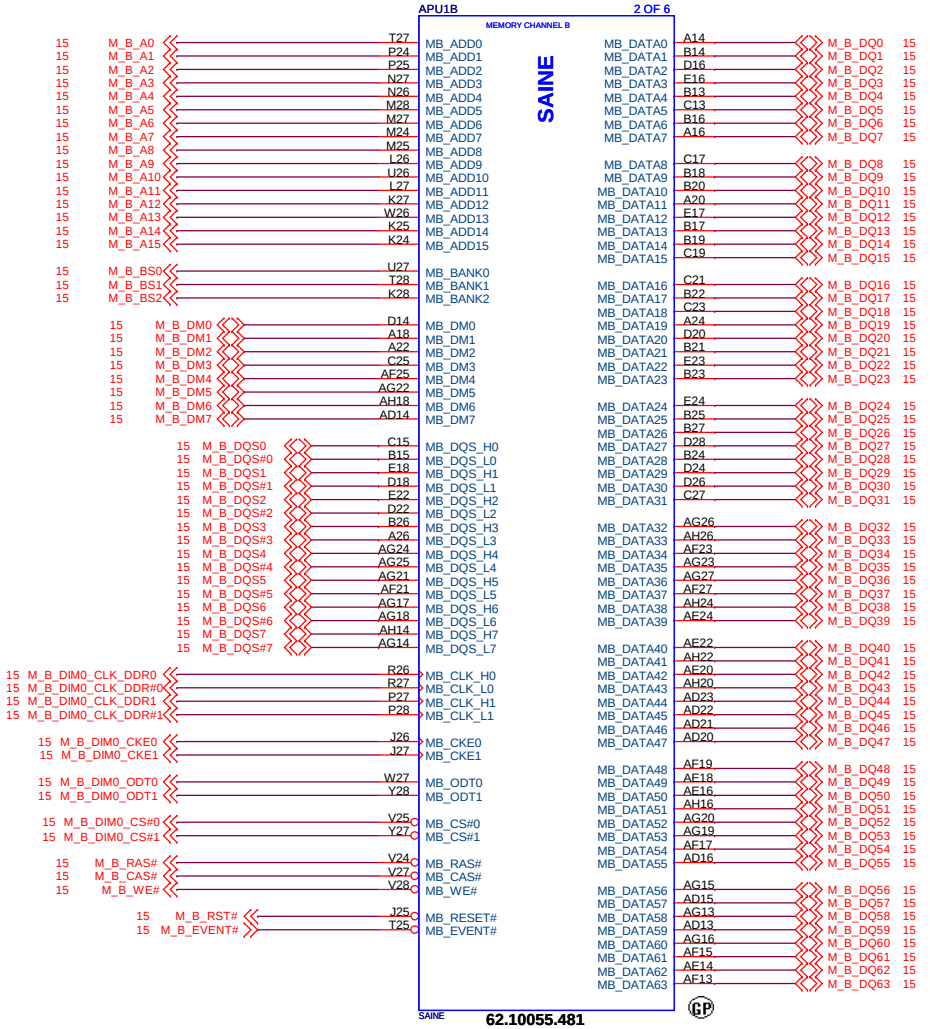
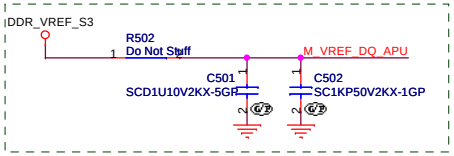
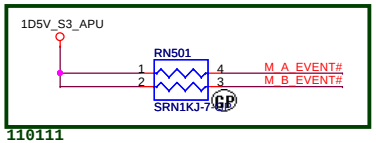


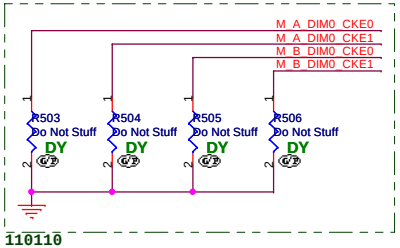


APU_VREF_DQ



LAYOUT: place them close to APU





Title	APU_DDR(2/5)	
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SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9

EDP

TRAVIS LVDS Panel

TRAVIS 110107

VGA output from FCH

100MHz

100MHz

101129

1008-SA

110323-1

SAINE

62.10055.481

[AMD FAE Frank]:
this is electrical key
do not allow power to turn on if this pin is still "L"
FS1 package is open pin
in the futur,FS1r2 will have this pin tied to VSS
if the wrong processor is plugged the socket
This is more of a problem on desktop platforms
(changing CPUs)

[AMD HDMI desing guidance]

Strap define PU :Enable HDMI
PD:Disable HDMI

1007-SA

1004-SA

1021-SA

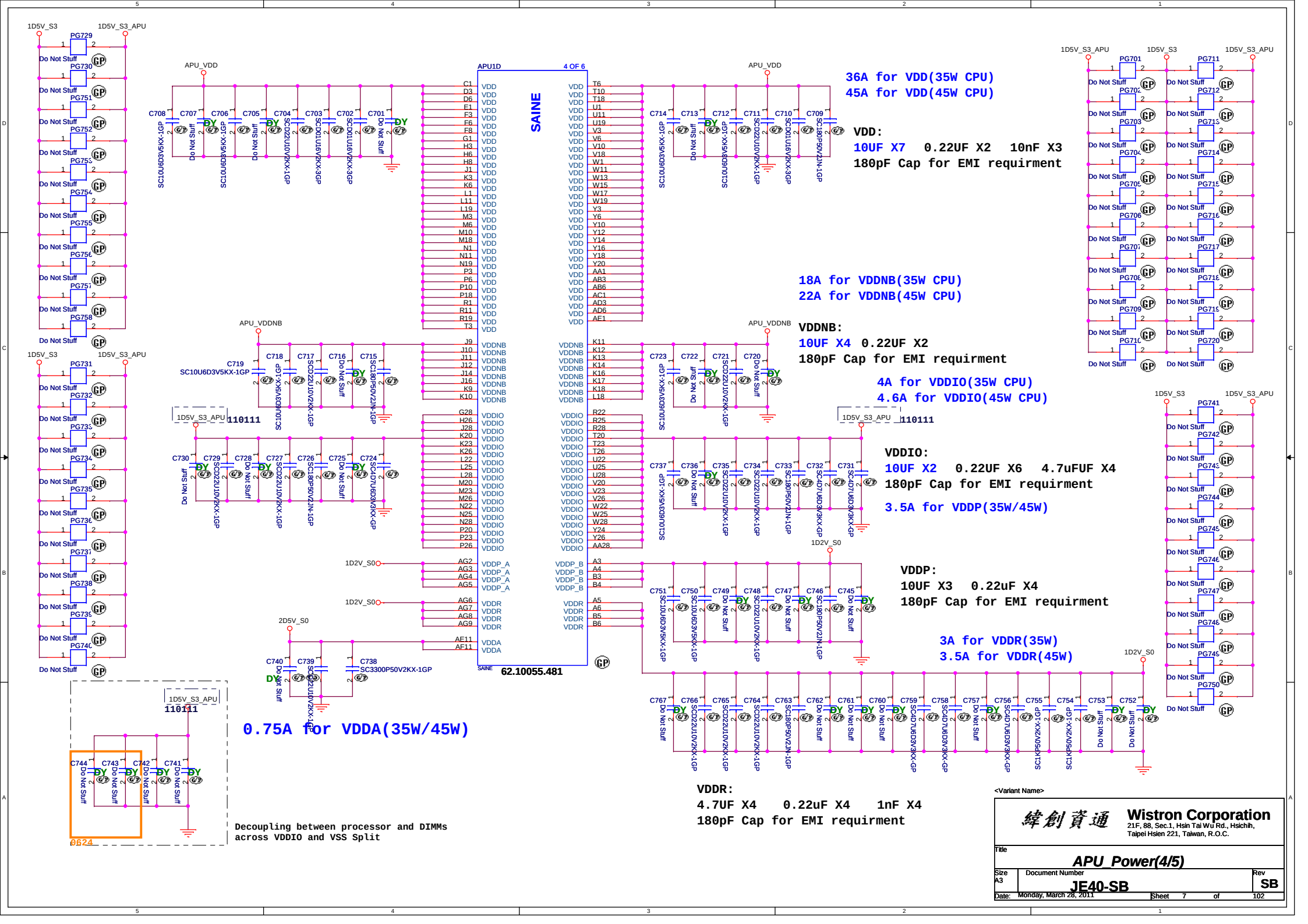
1006-SA

0920-SA

0924-SA

S3 Power

CPU exceeds to 125℃


APU1D
4 OF 6
SAINE
62.10055.481
36A for VDD(35W CPU)
45A for VDD(45W CPU)
VDD:
10UF X7 0.22UF X2 10nF X3
180pF Cap for EMI requirment
18A for VDDNB(35W CPU)
22A for VDDNB(45W CPU)
VDDNB:
10UF X4 0.22UF X2
180pF Cap for EMI requirment
4A for VDDIO(35W CPU)
4.6A for VDDIO(45W CPU)
VDDIO:
10UF X2 0.22UF X6 4.7uFUF X4
180pF Cap for EMI requirment
3.5A for VDDP(35W/45W)
VDDP:
10UF X3 0.22uF X4
180pF Cap for EMI requirment
3A for VDDR(35W)
3.5A for VDDR(45W)
VDDR:
4.7UF X4 0.22uF X4 1nF X4
180pF Cap for EMI requirment
0.75A for VDDA(35W/45W)
Decoupling between processor and DIMMs
across VDDIO and VSS Split
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
APU_Power(4/5)
Size A3
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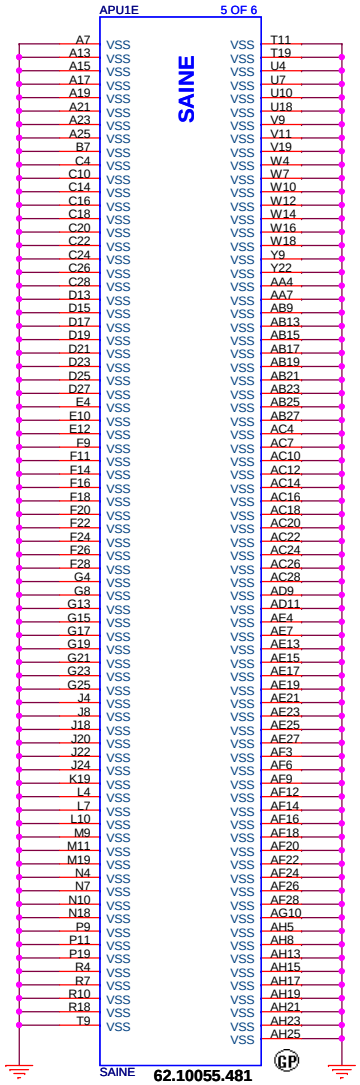

<Variant Name>

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Title: APU_VSS(5/5)

Size	Document Number	Rev
A3	JE40-SB	SB

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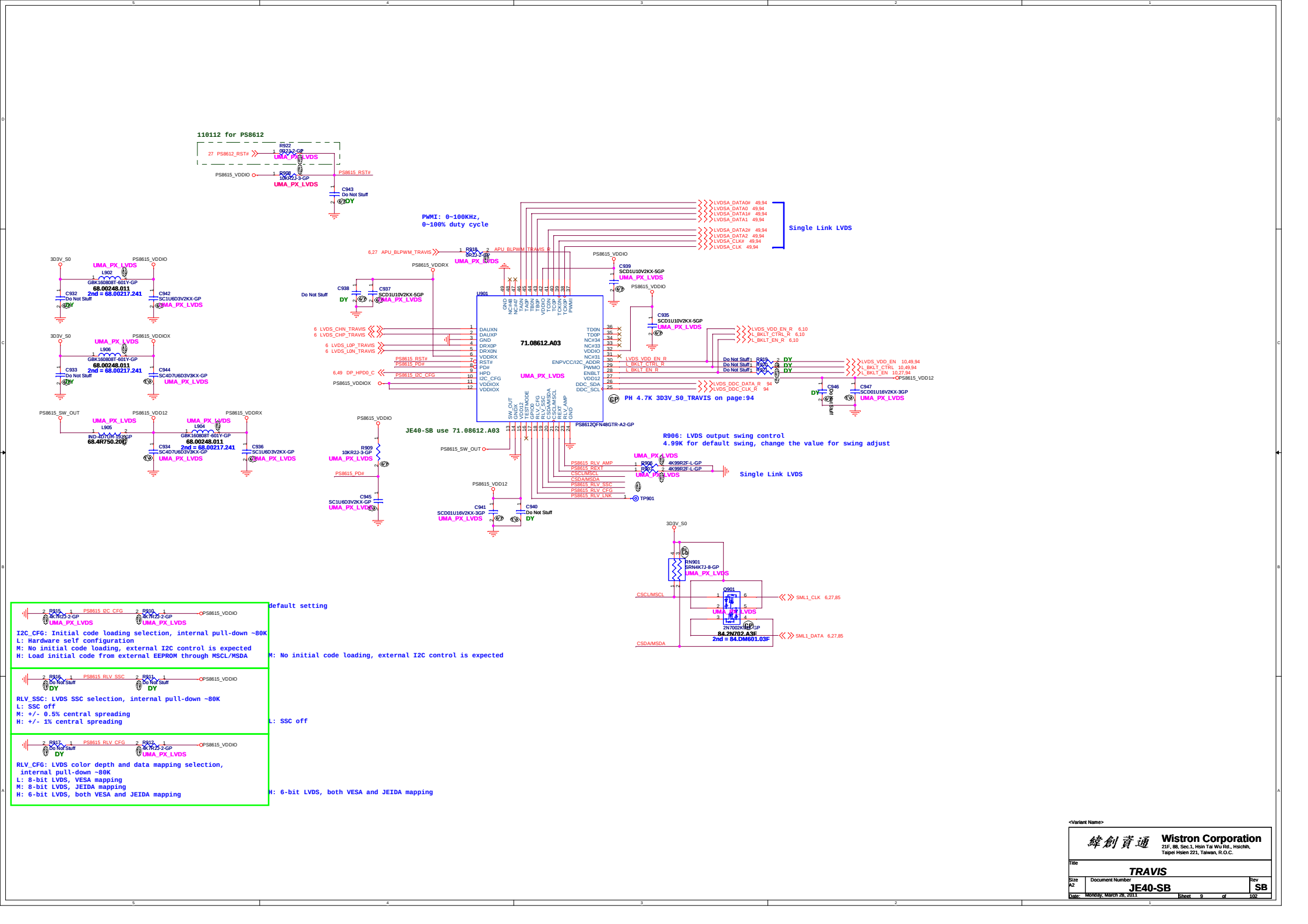

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TRAVIS**

Size: A2 | Document Number: **JE40-SB** | Rev: **SB**

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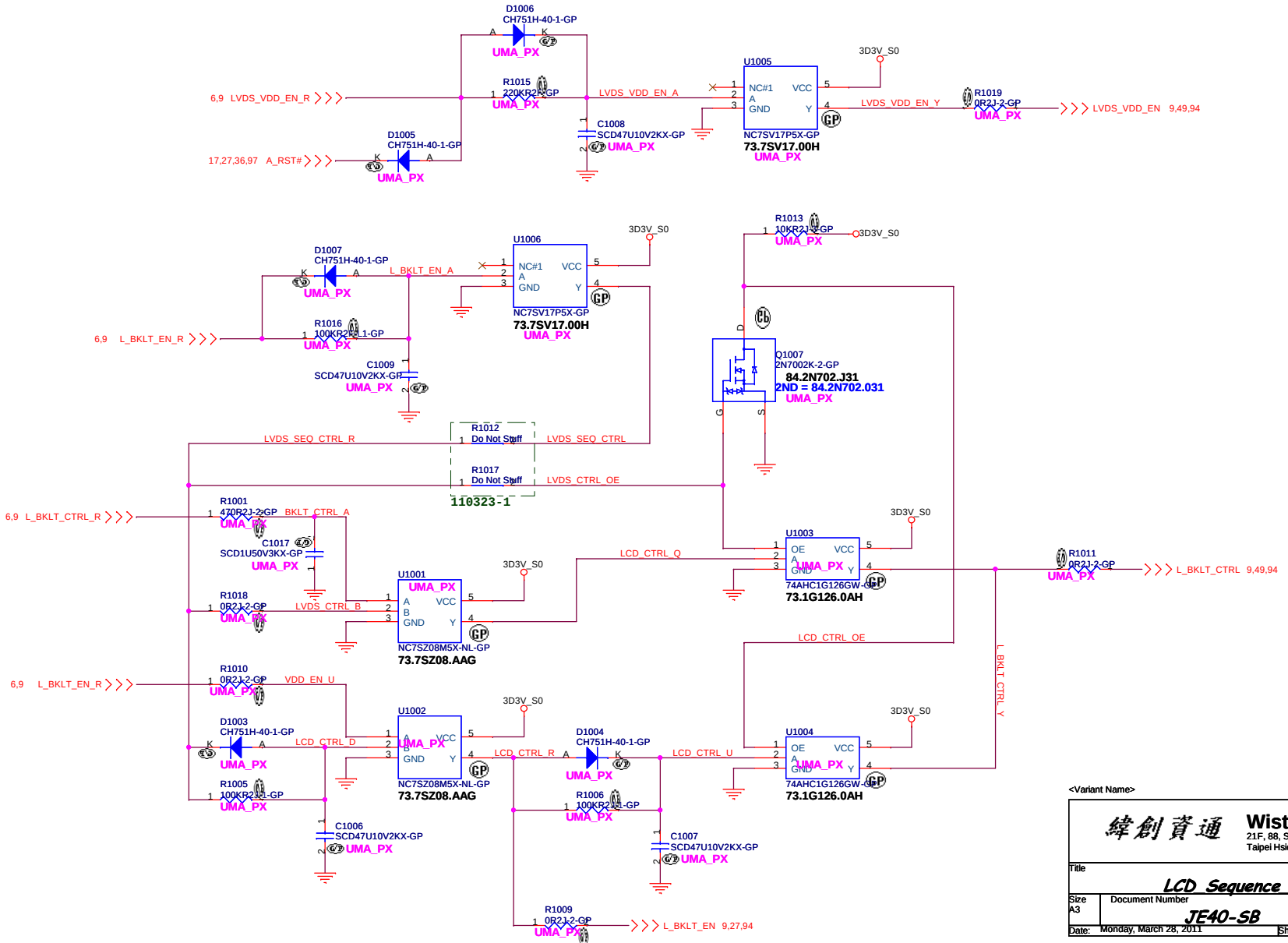

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD_Sequence_Control

Size: A3 | Document Number: JE40-SB | Rev: SB

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<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
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<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 12 of 102

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<Variant Name>

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-SB	SB

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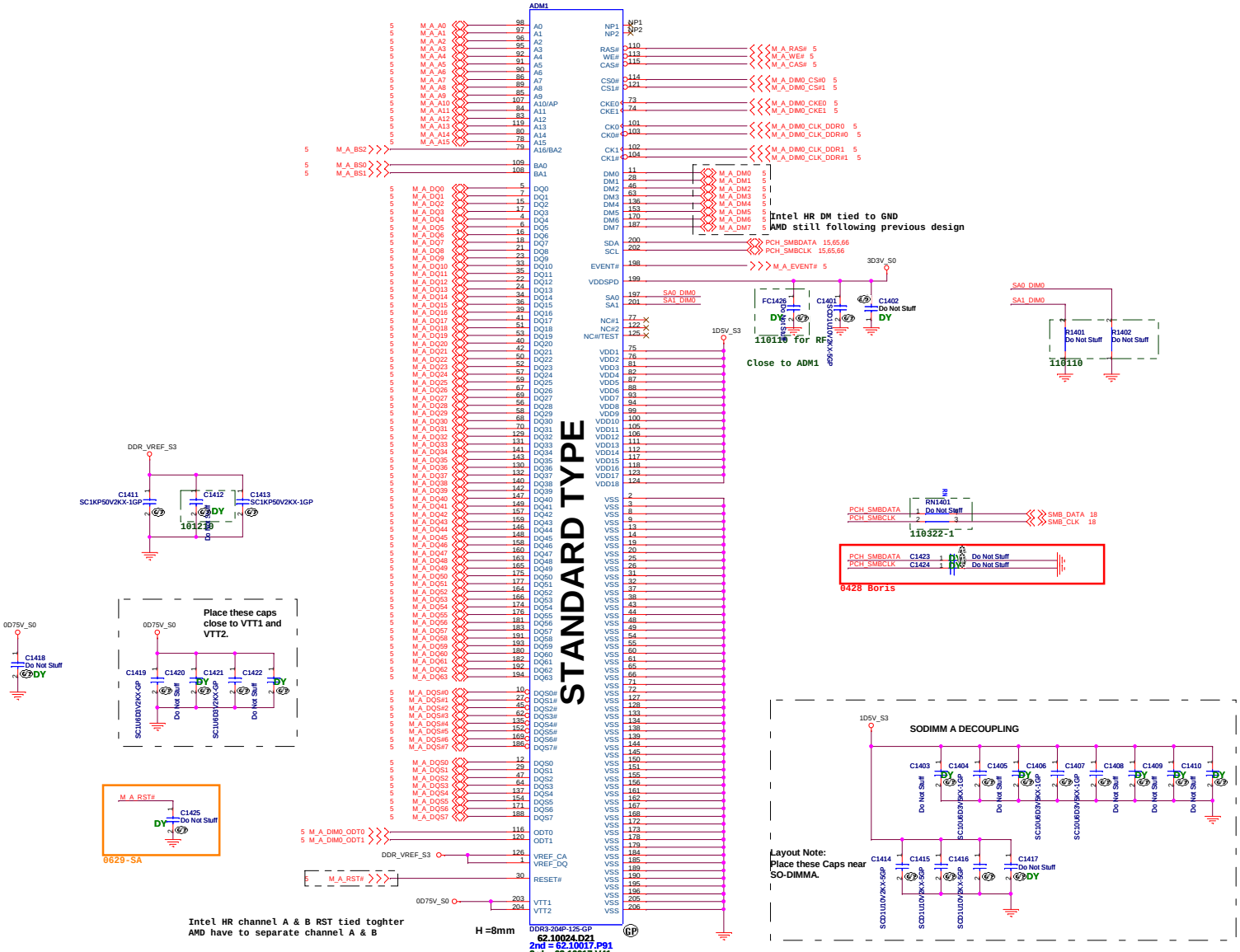

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	DDR3-SODIMM1	
Size: A2	Document Number: JE40-SB	Rev: SB
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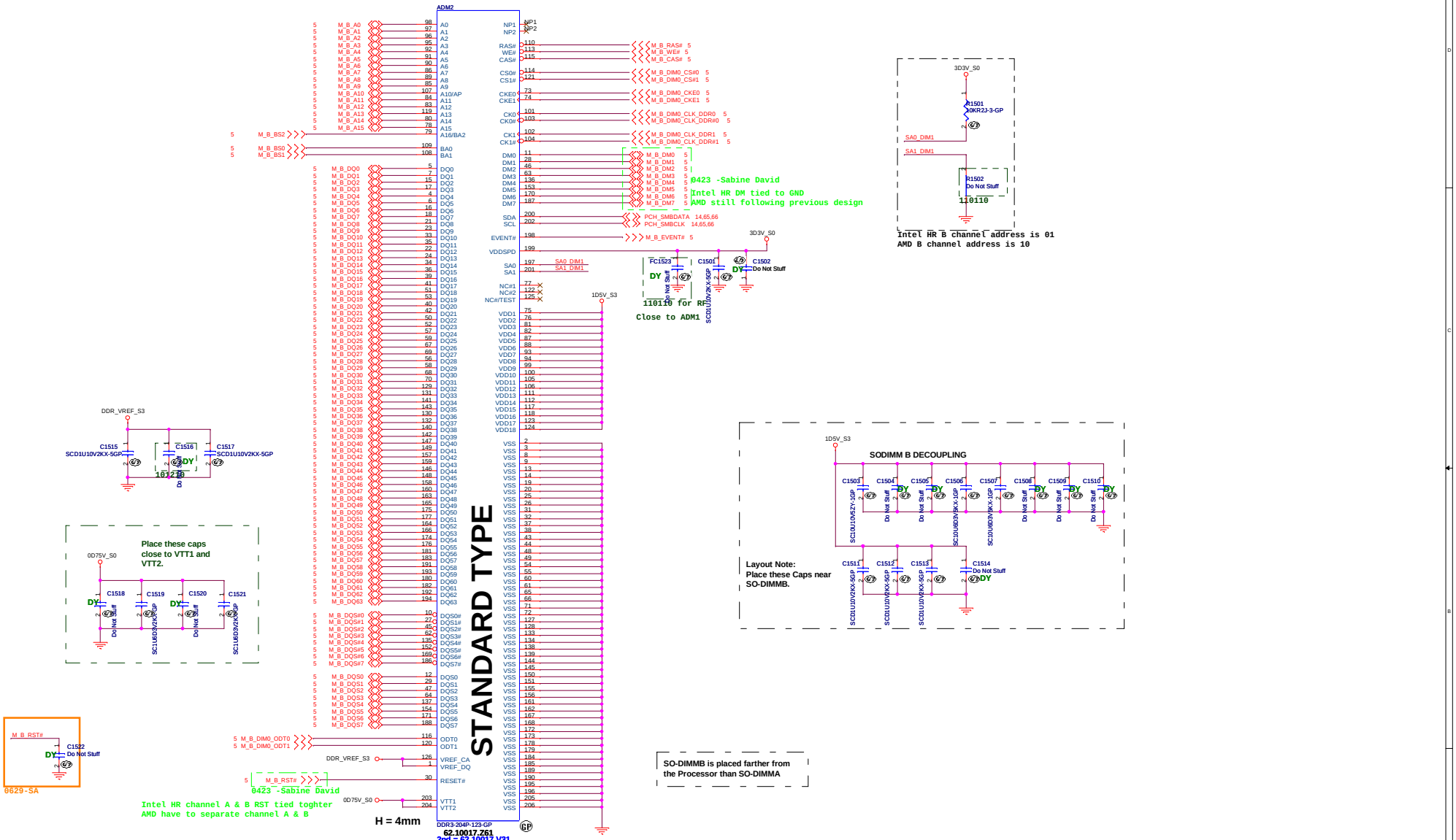

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: A2 | Document Number: JE40-SB | Rev: SB

Date: Monday, March 28, 2011 | Sheet 15 of 102

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<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-SB	SB

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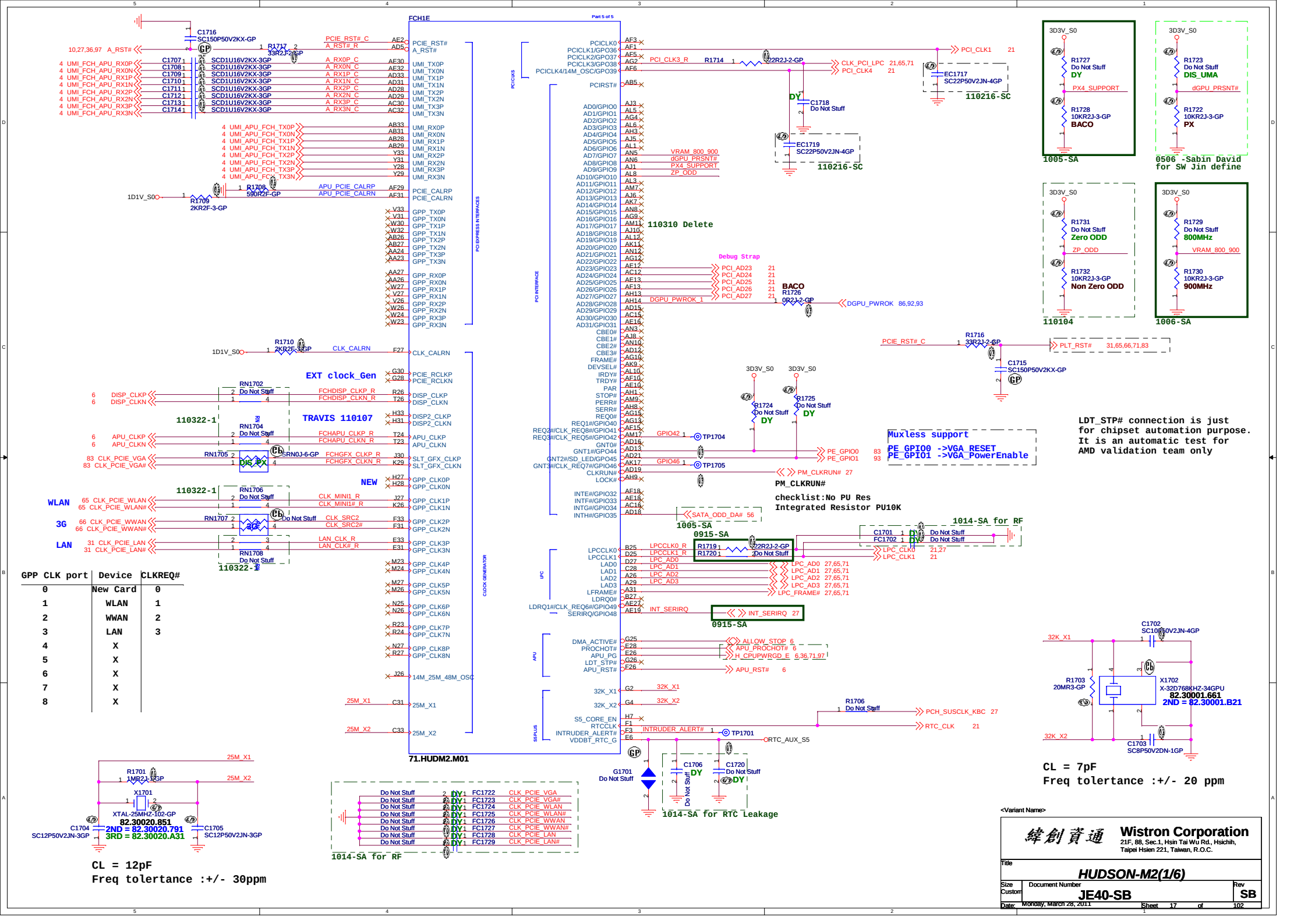
FCH1E
Part 5 of 5
71.HUDM2.M01
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
SB-FLUS
PCICLKS
Debug Strap
110310 Delete
EXT clock_Gen
TRAVIS 110107
NEW
110322-1
DIS_EX
WLAN
3G
LAN
RN1702
RN1704
RN1705
RN1706
RN1707
RN1708
SRN0J-6-GP
Do Not Stuff
GPP CLK port | Device | CLKREQ#
0 | New Card | 0
1 | WLAN | 1
2 | WWAN | 2
3 | LAN | 3
4 | X
5 | X
6 | X
7 | X
8 | X
X1701
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
3RD = 82.30020.A31
CL = 12pF
Freq tolertance :+/- 30ppm
1014-SA for RF
1014-SA for RTC Leakage
BACO
R1726
0R2J-2-GP
DGPU_PWROK_1
DGPU_PWROK 86,92,93
110216-SC
EC1717
SC22P50V2JN-4GP
EC1719
1005-SA
0915-SA
0506 -Sabin David
for SW Jin define
R1727
Do Not Stuff
DY
PX4_SUPPORT
R1728
10KR2J-3-GP
BACO
R1723
DIS_UMA
dGPU_PRSNT#
R1722
PX
110104
1006-SA
R1731
Zero ODD
ZP_ODD
R1732
Non Zero ODD
R1729
800MHz
VRAM_800_900
R1730
900MHz
Muxless support
PE_GPIO0 ->VGA_RESET
PE_GPIO1 ->VGA_PowerEnable
LDT_STP# connection is just
for chipset automation purpose.
It is an automatic test for
AMD validation team only
PM_CLKRUN#
checklist:No PU Res
Integrated Resistor PU10K
R1716
3R2J-2-GP
PLT_RST#
C1715
SC150P50V2KX-GP
R1724
R1725
C1716
C1717
C1718
C1719
C1720
G1701
R1706
R1719
R1720
C1701
C1702
FC1701
FC1702
R1703
20MR3-GP
X1702
X-32D768KHZ-34GPU
82.30001.661
2ND = 82.30001.B21
C1703
SC8P50V2DN-1GP
CL = 7pF
Freq tolertance :+/- 20 ppm
R1701
1MR2J-1-GP
C1704
SC12P50V2JN-3GP
C1705
SC12P50V2JN-3GP
<Variant Name>
緯創資通
Wistron Corporation
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Title
HUDSON-M2(1/6)
Size
Custom
Document Number
JE40-SB
Rev
SB
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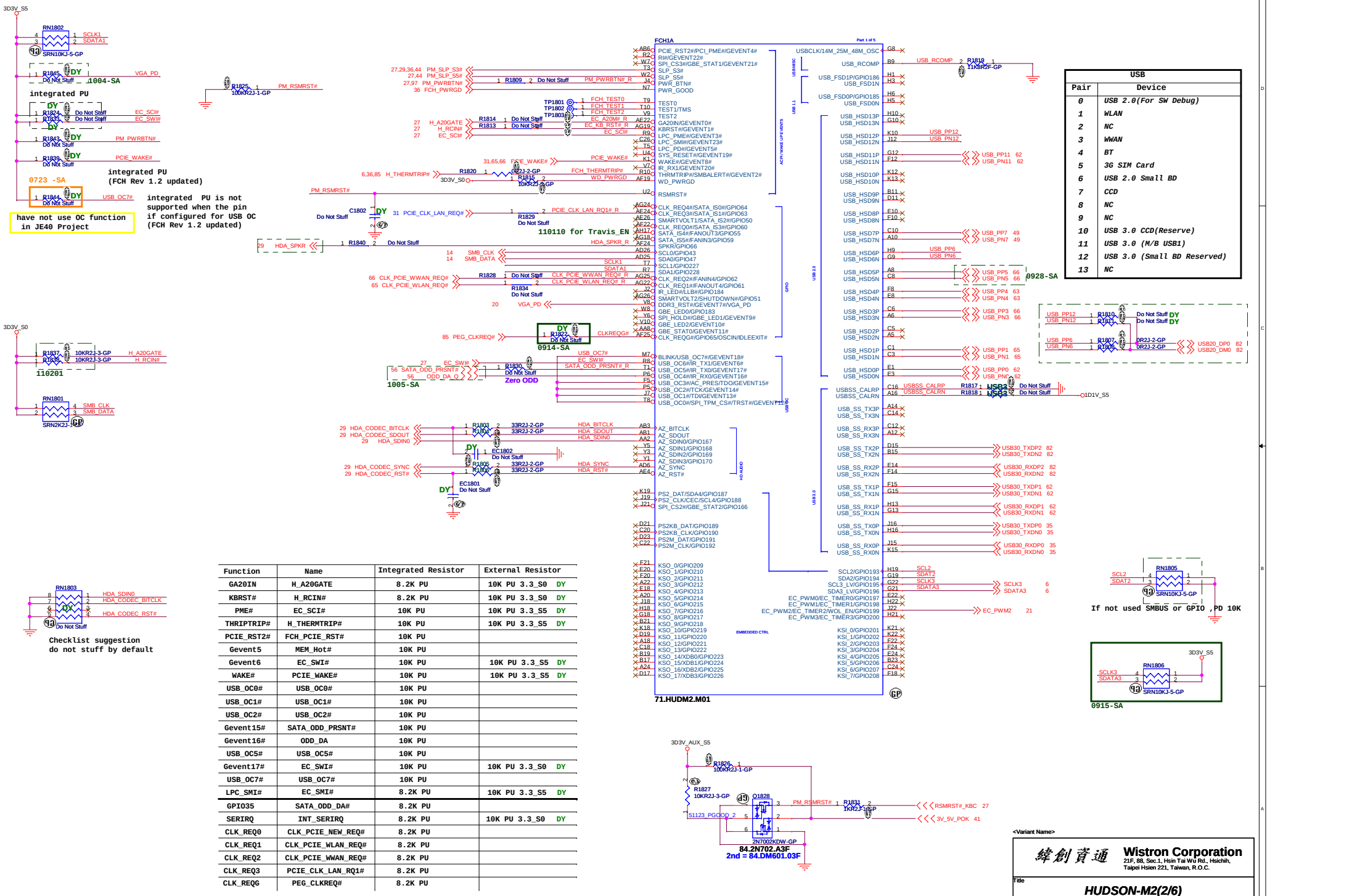

Function	Name	Integrated Resistor	External Resistor	
GA20IN	H_A20GATE	8.2K PU	10K PU 3.3_S0	DY
KBRST#	H_RCIN#	8.2K PU	10K PU 3.3_S0	DY
PME#	EC_SCI#	10K PU	10K PU 3.3_S5	DY
THRIPTRIP#	H_THERMTRIP#	10K PU	10K PU 3.3_S5	DY
PCIE_RST2#	FCH_PCIE_RST#	10K PU		
Gevent5	MEM_Hot#	10K PU		
Gevent6	EC_SWI#	10K PU	10K PU 3.3_S5	DY
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_S5	DY
USB_OC0#	USB_OC0#	10K PU		
USB_OC1#	USB_OC1#	10K PU		
USB_OC2#	USB_OC2#	10K PU		
Gevent15#	SATA_ODD_PRSNT#	10K PU		
Gevent16#	ODD_DA	10K PU		
USB_OC5#	USB_OC5#	10K PU		
Gevent17#	EC_SWI#	10K PU	10K PU 3.3_S0	DY
USB_OC7#	USB_OC7#	10K PU		
LPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_S5	DY
GPIO35	SATA_ODD_DA#	8.2K PU		
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_S0	DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU		
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU		
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU		
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU		
CLK_REQ6	PEG_CLKREQ#	8.2K PU		

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Title: HUDSON-M2(2/6)

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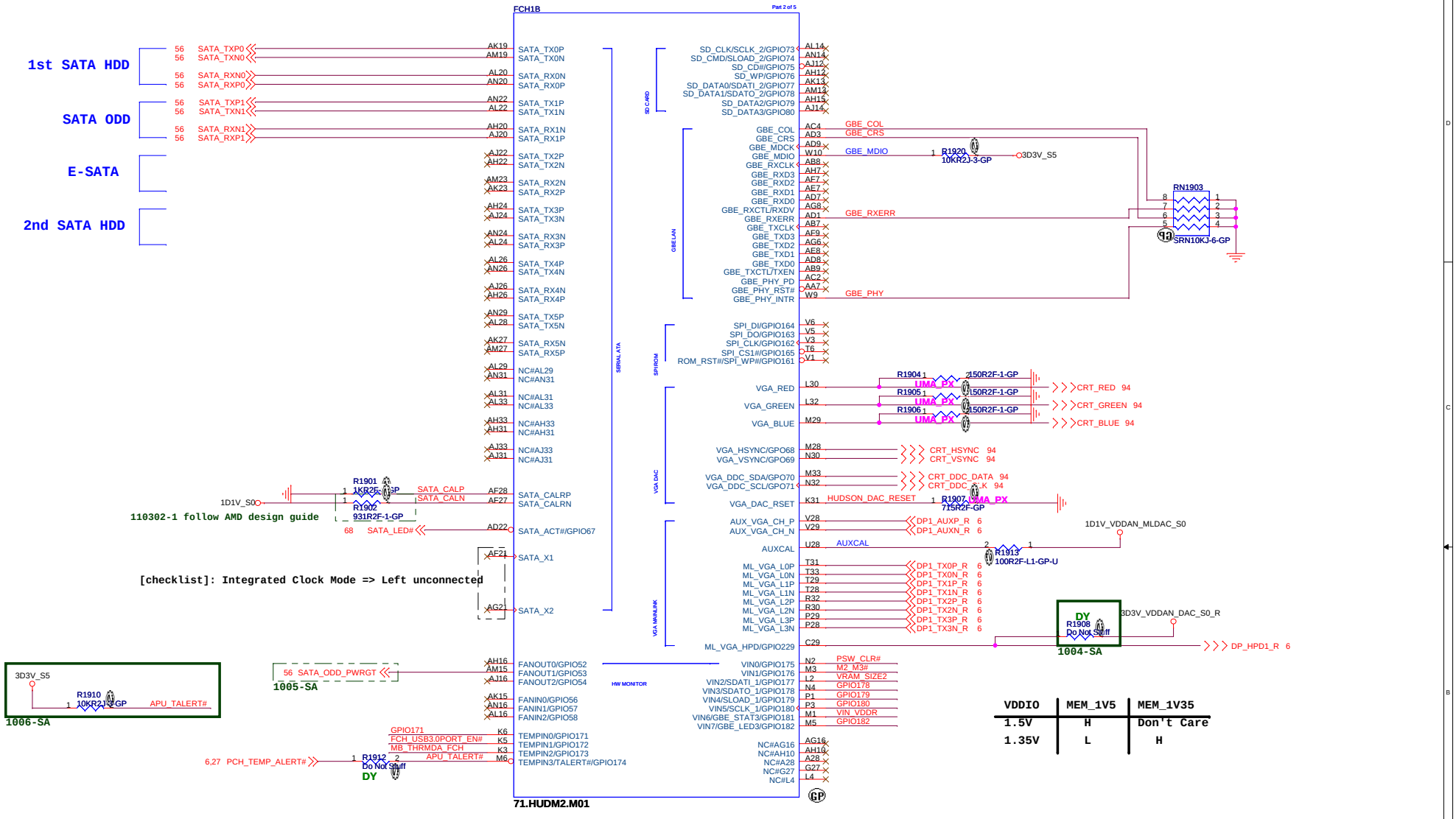
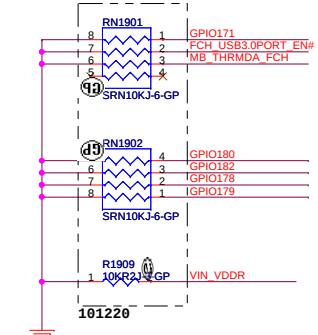
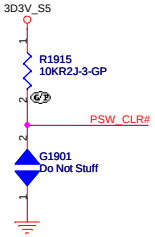
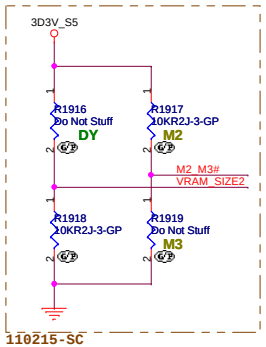


VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H



If not used HWM or GPIO ,PD 10K





VRAM Size	GPIO176	GPIO177
512MB	L	L
1GB	H	H
2GB	H	L
Undefine	L	H

<Variant Name>

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Title: HUDSON-M2(3/6)

Size	Document Number	Rev
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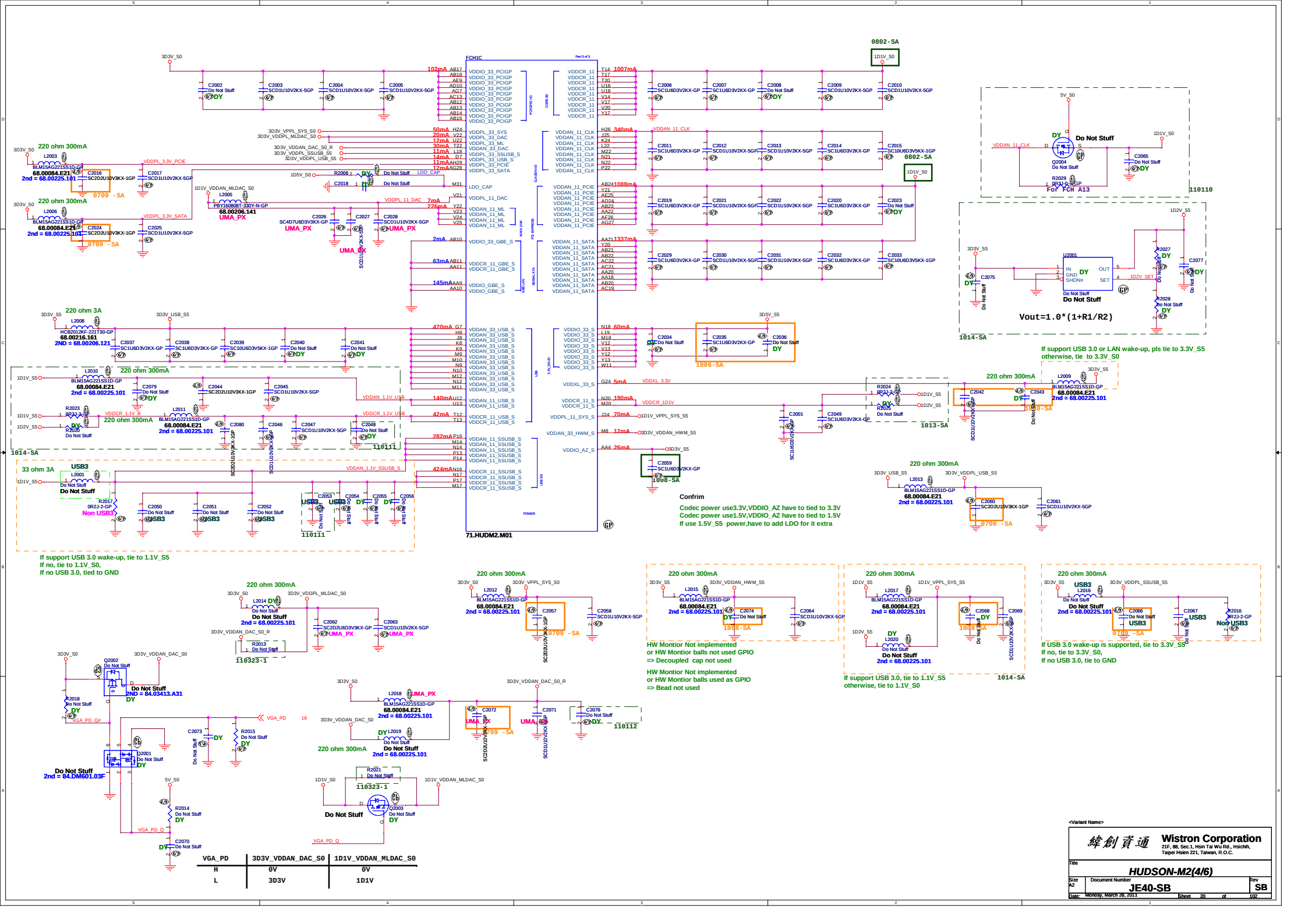

<Variant Name>
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Title: HUDSON-M2(4/6)

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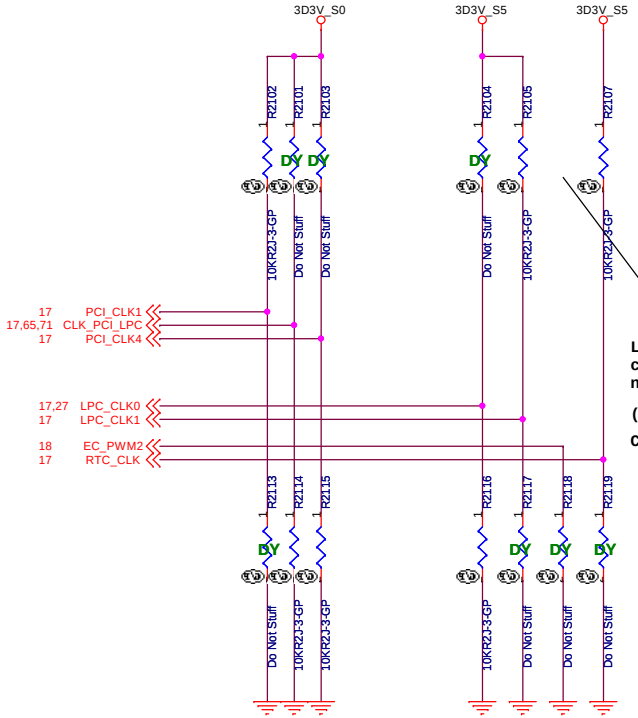
SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5
checklist:PU 3.3V_S5
no support S5 PLUS funciton,PU 3.3V_S5



LPC ROM implemented
checklistsuggestion:
no PU or PD required

(integrated PU 10K)

CRB: do not stuff PU Res

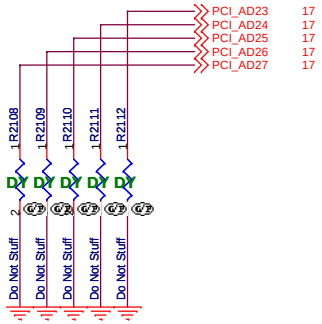
USE this pin to determine INT/EXT CLK

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

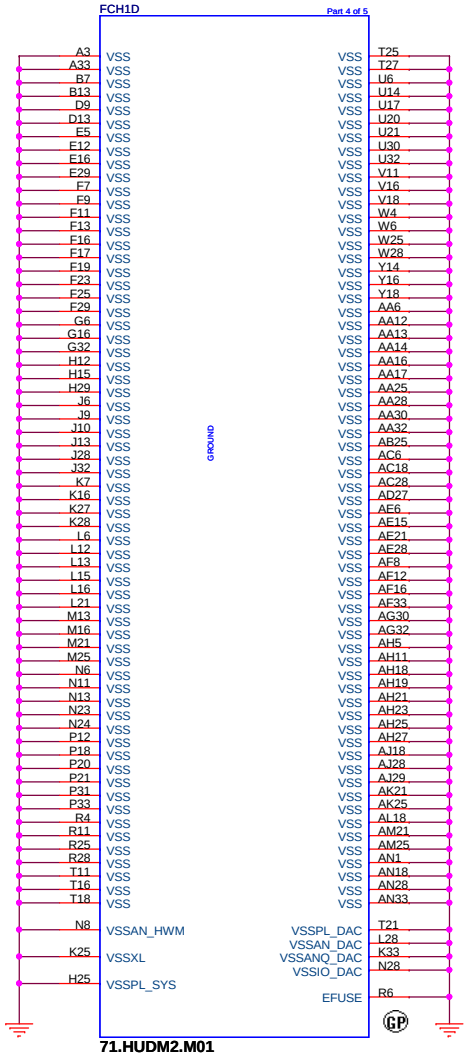
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(5/6)

Size: A3 | Document Number: JE40-SB | Rev: SB

Date: Monday, March 28, 2011 | Sheet 21 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HUDSON-M2(6/6)*

Size	Document Number	Rev
A3	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 22 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 23 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 24 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	JE40-SB	SB

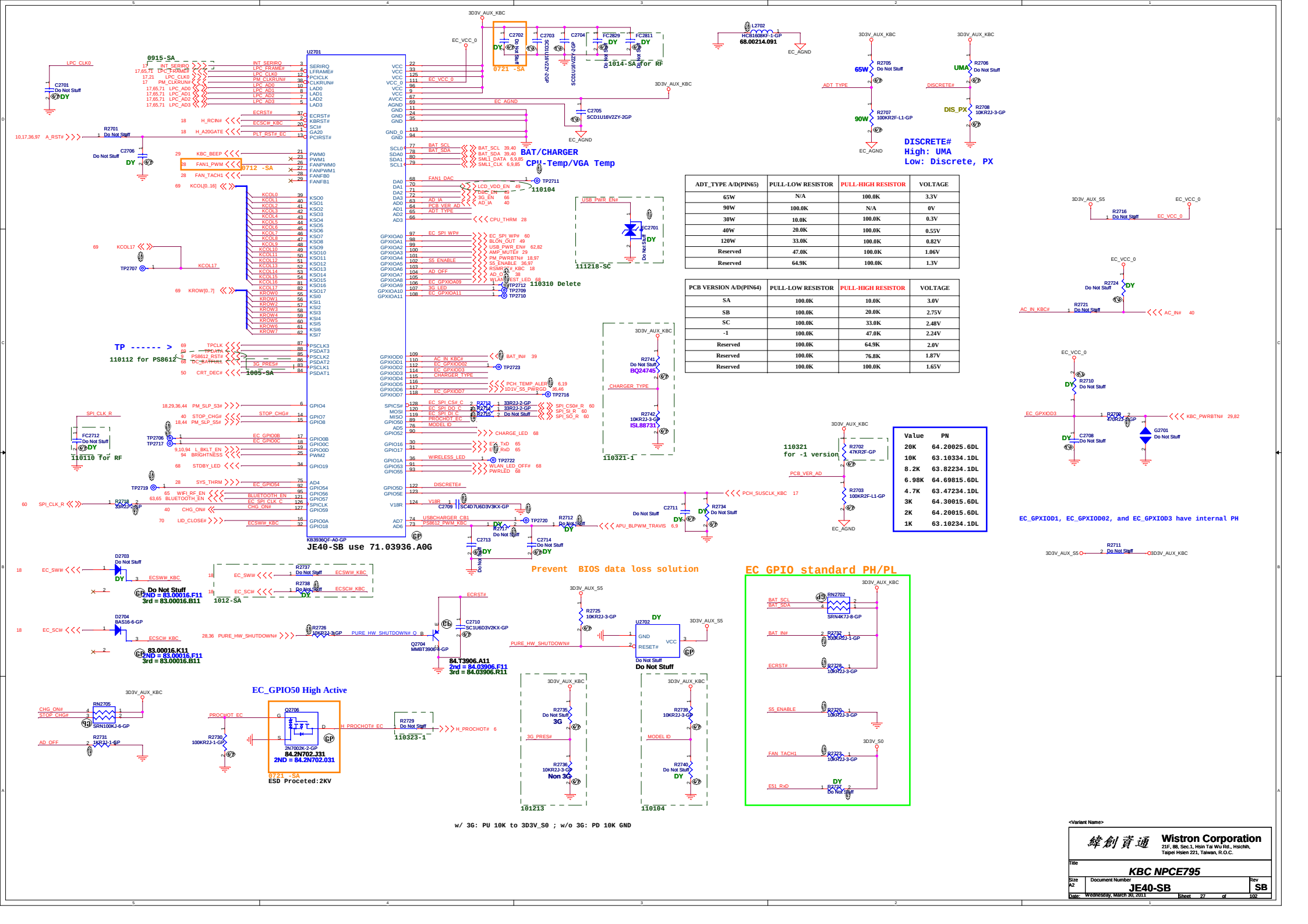
Date: Friday, March 25, 2011 Sheet 25 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 26 of 102	



ADT_TYPE A/D(PIN65)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

PCB VERSION A/D(PIN64)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

Value	PN
20K	64.20025.6DL
10K	63.10334.1DL
8.2K	63.82234.1DL
6.98K	64.69815.6DL
4.7K	63.47234.1DL
3K	64.30015.6DL
2K	64.20015.6DL
1K	63.10234.1DL

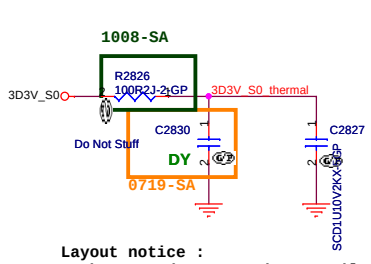
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

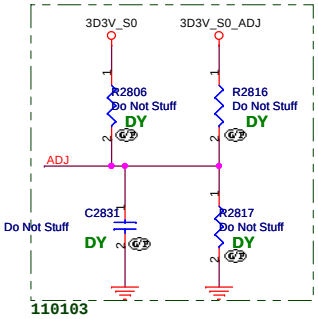
Title: KBC NPCE795

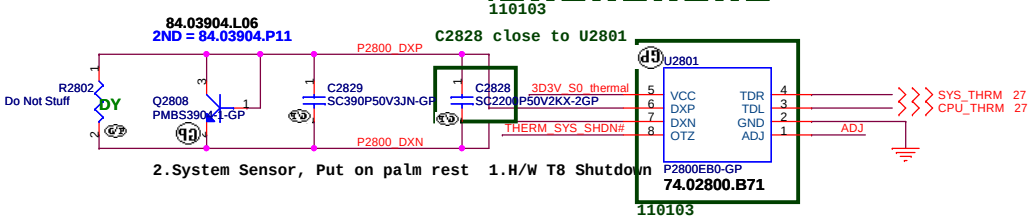
Size: A2 | Document Number: JE40-SB | Rev: SB

Date: Wednesday, March 30, 2011 | Sheet 27 of 102

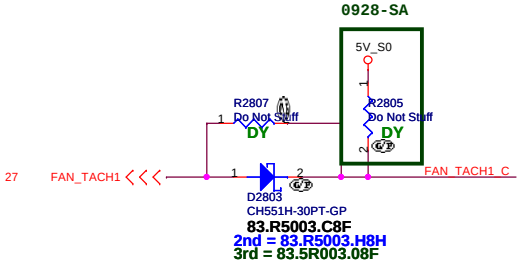


Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

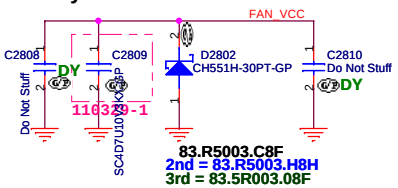


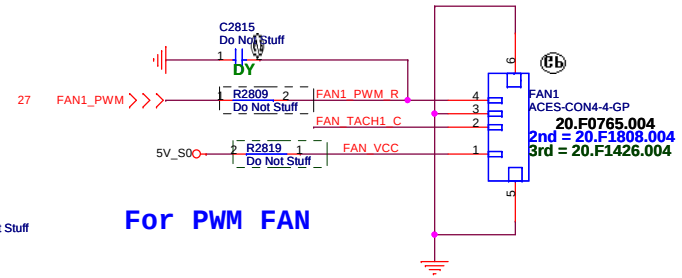


2.System Sensor, Put on palm rest 1.H/W T8 Shutdown



Layout 15 mil

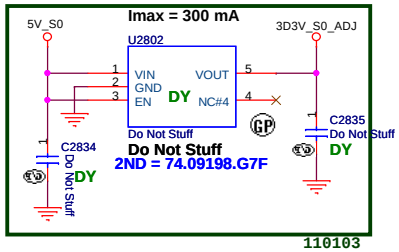




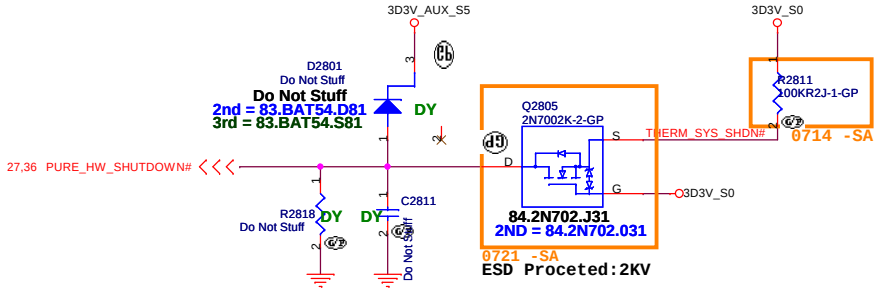
For PWM FAN

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



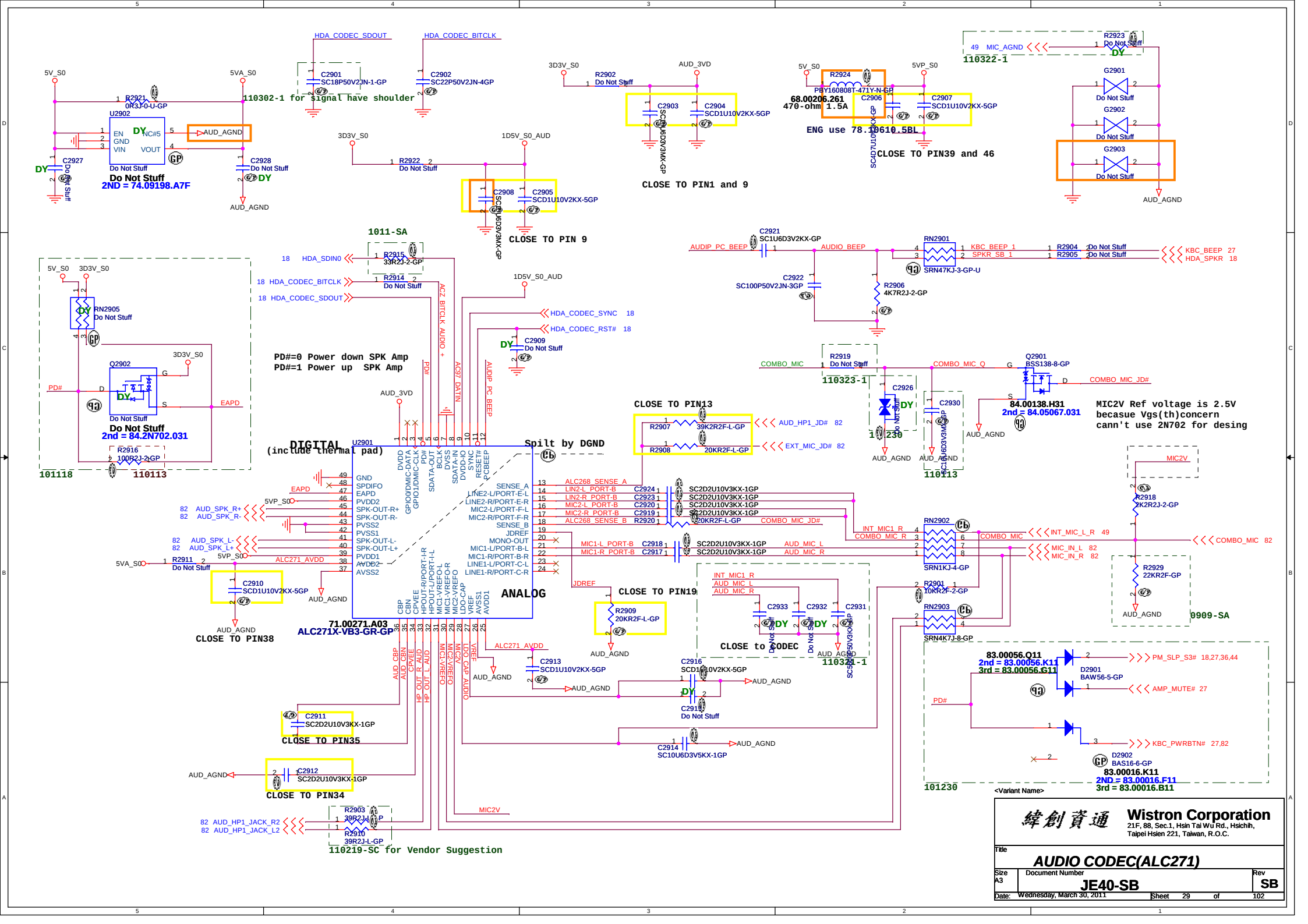
VGA Thermal sensor P2800



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal P2800	
Size A3	Document Number JE40-SB	Rev SB
Date: Wednesday, March 30, 2011	Sheet 28 of 102	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO CODEC(ALC271)***	
Size A3	Document Number **JE40-SB**	Rev **SB**
Date: Wednesday, March 30, 2011	Sheet 29 of 102	

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMP

Size: A3 | Document Number: JE50-SB | Rev: SB

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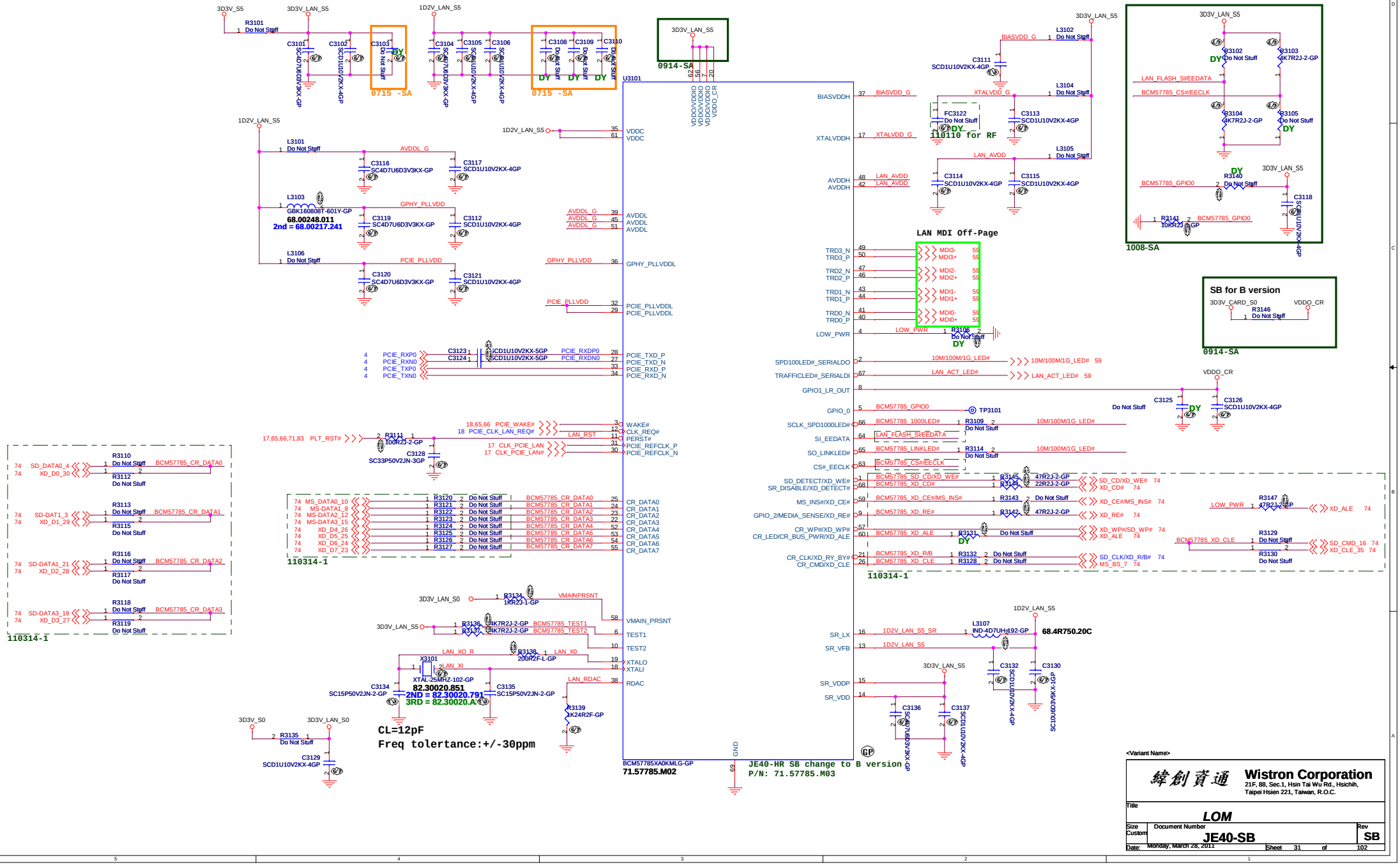

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LOM

Size: Custom | Document Number: JE40-SB | Rev: SB

Date: Monday, March 28, 2011 | Sheet 31 of 102

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RTS5138

Size	Document Number	Rev
A3	**JE40-SB**	**SB**

Date: Friday, March 25, 2011 Sheet 32 of 102

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	JE40-SB	SB

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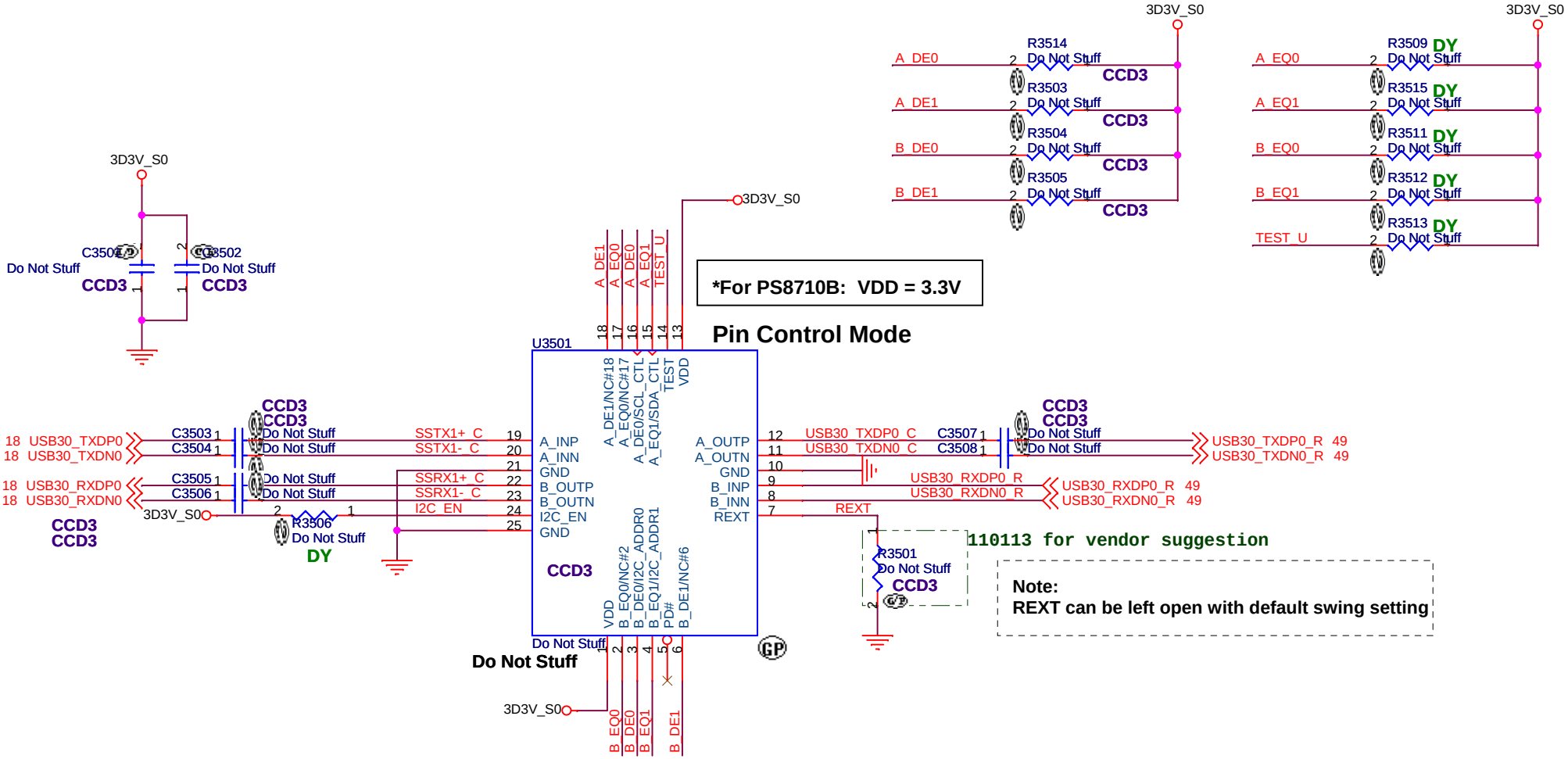
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 34 of 102	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

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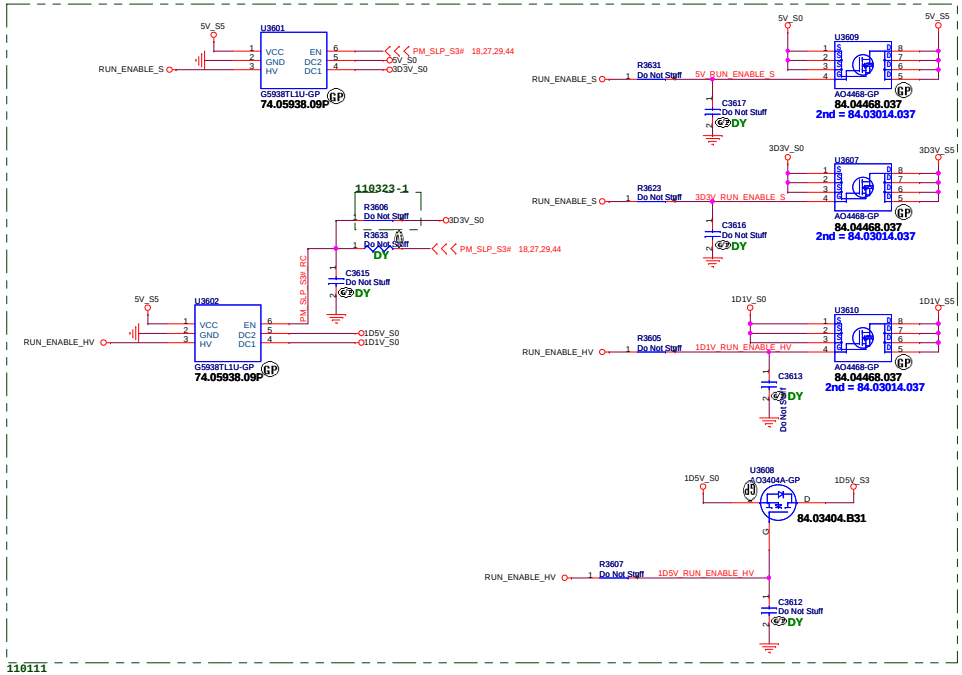
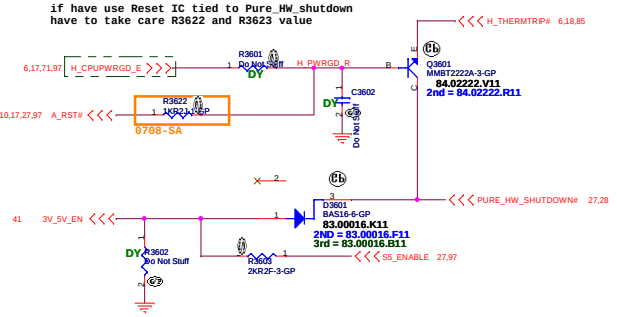
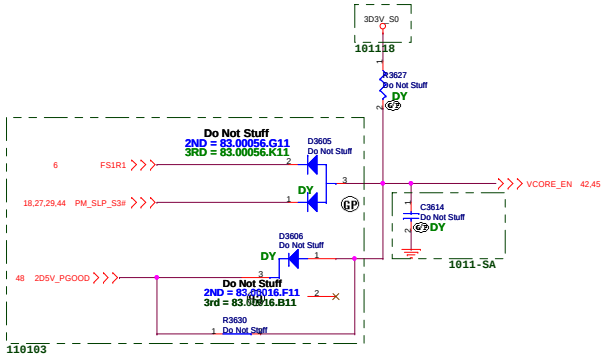
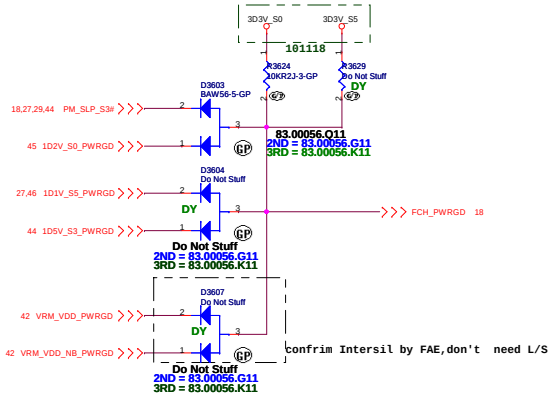


if have use Reset IC tied to Pure_HW_shutdown
have to take care R3622 and R3623 value



Power Sequence





confrim Intersil by FAE,don't need L/S

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Power On Logic***
Size: Custom	Document Number: **JE40-SB** Rev: **SB**
Date: Monday, March 28, 2011	Sheet 36 of 102

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-SB	SB

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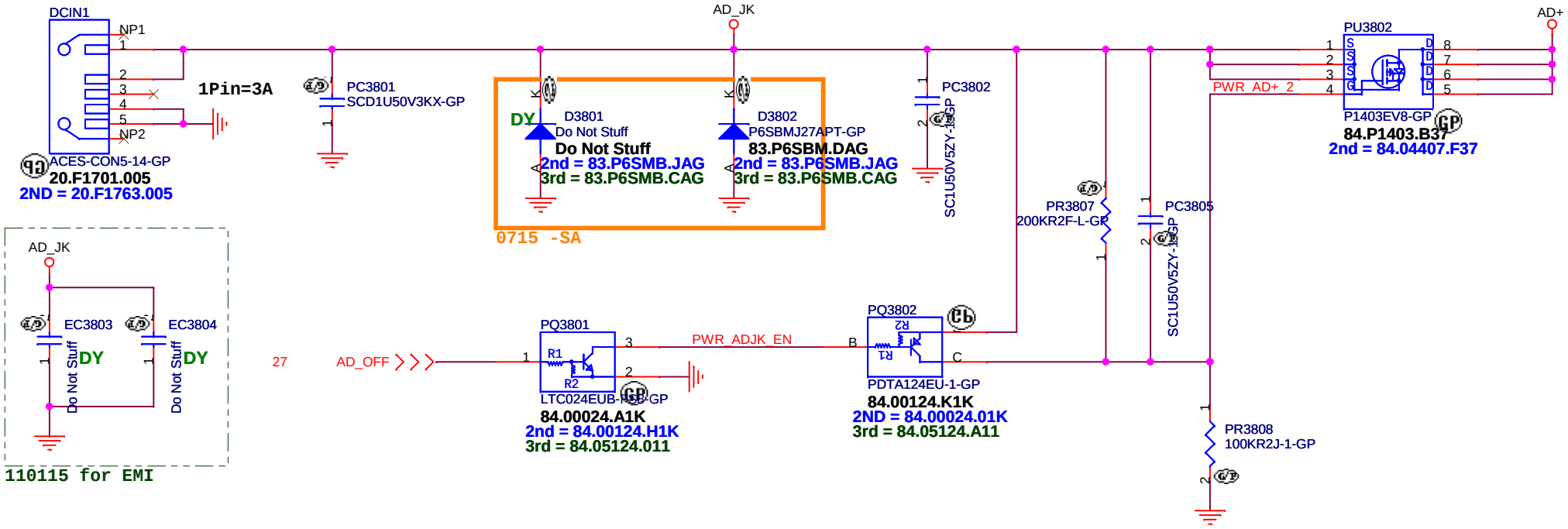
Adaptor in to generate DCBATOUT



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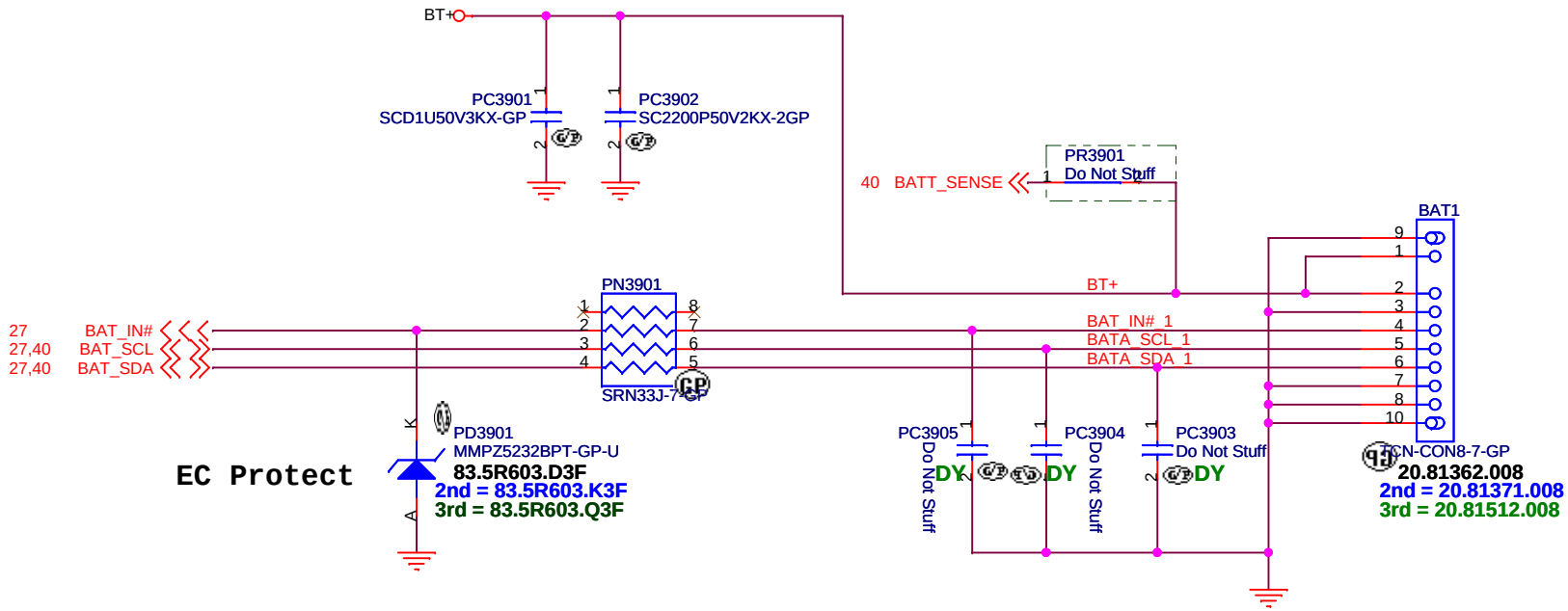
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN_JACK	
Size A4	Document Number JE40-SB	Rev SB
Date: Monday, March 28, 2011	Sheet 38 of 102	

BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT_CONN***

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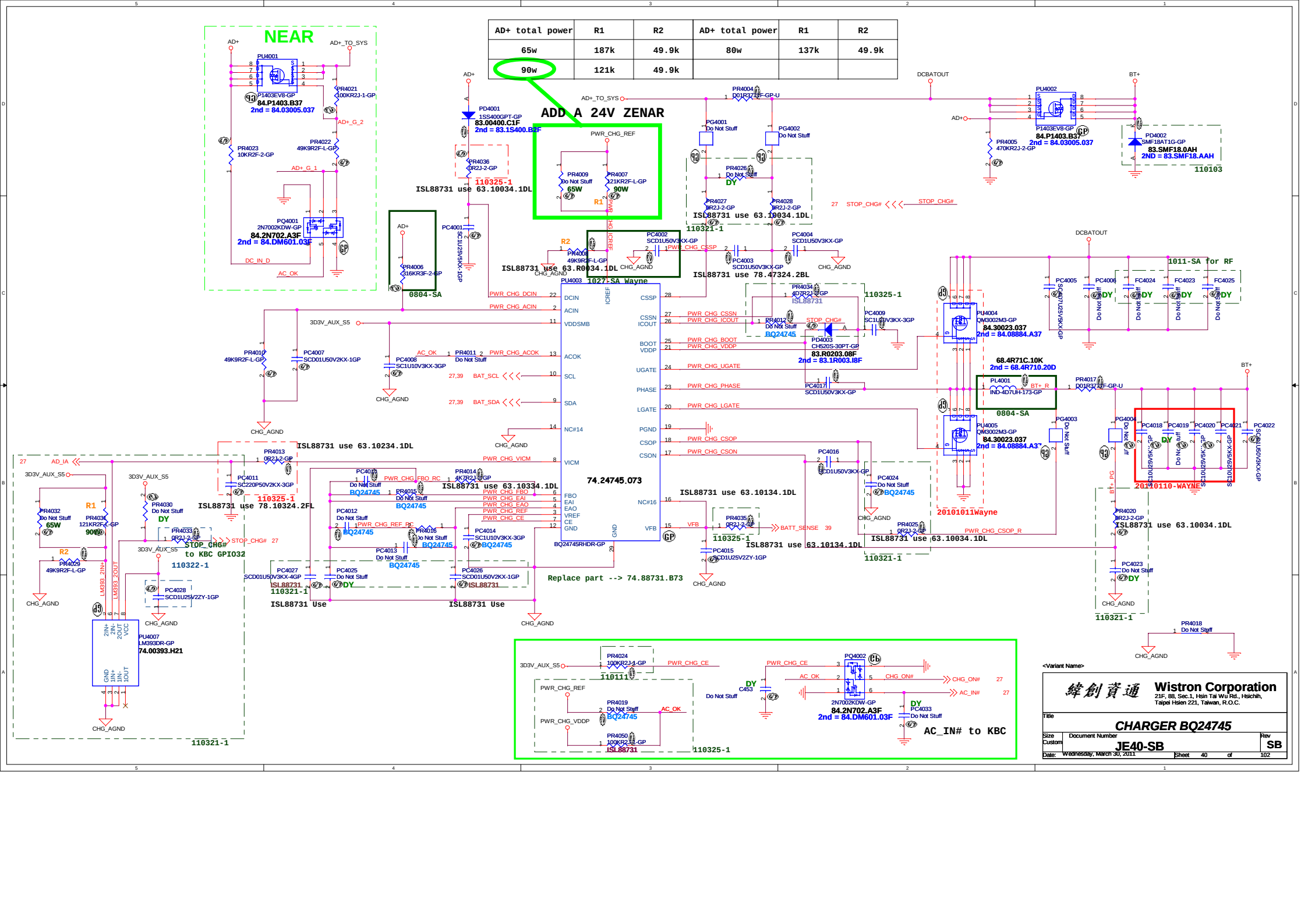
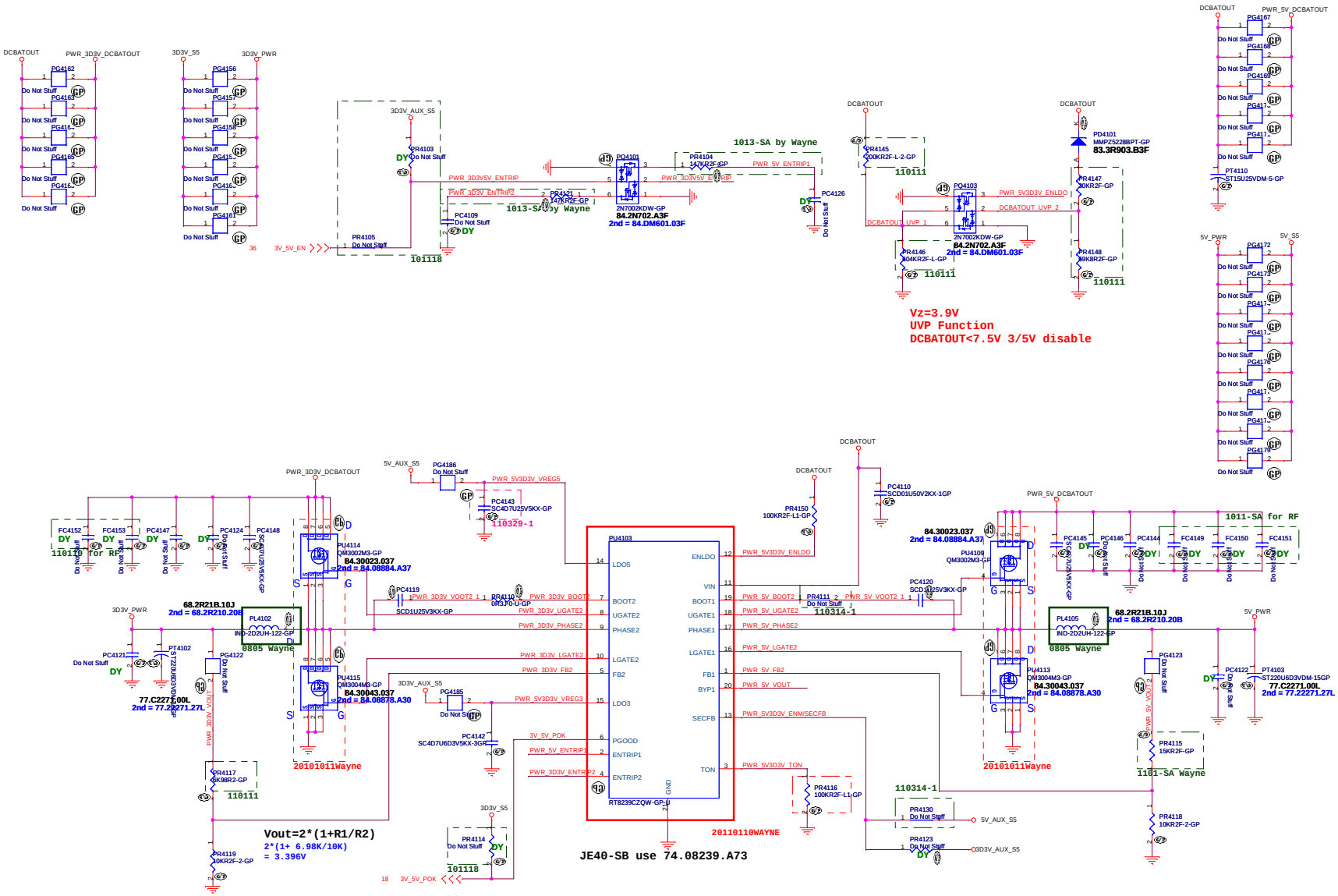


AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



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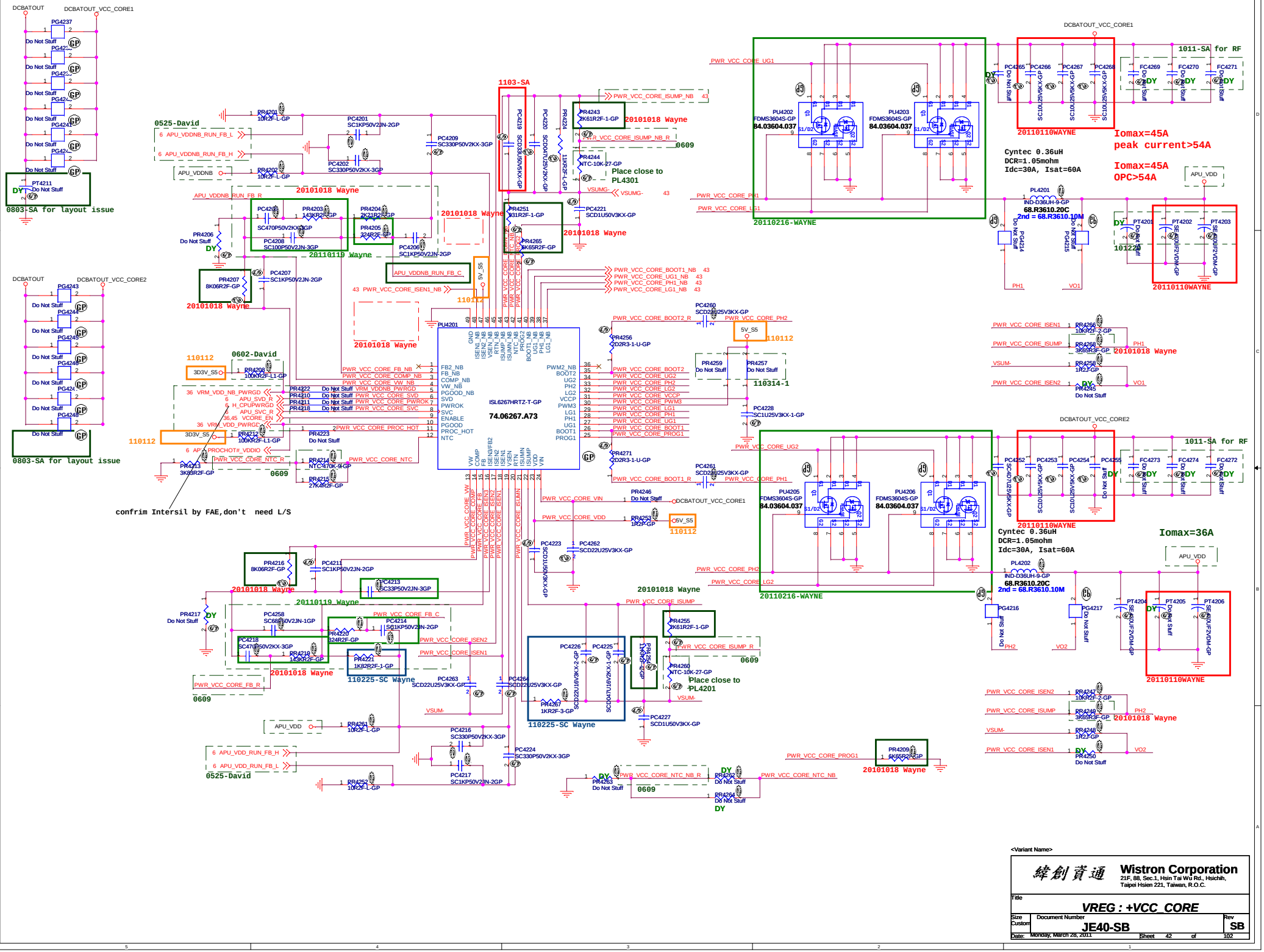
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8239	
Size: A2	Document Number: JE40-SB	Rev: SB
Date: Tuesday, March 29, 2011	Sheet 41 of 102	


DCBATOUT
DCBATOUT_VCC_CORE1
DCBATOUT_VCC_CORE2
0803-SA for layout issue
1103-SA
0525-David
0602-David
20101018 Wayne
20110119 Wayne
20110216-WAYNE
20110110WAYNE
1011-SA for RF
Iomax=45A
peak current>54A
Iomax=45A
OPC>54A
Iomax=36A
Cyntec 0.36uH
DCR=1.05mohm
Idc=30A, Isat=60A
2nd = 68.R3610.10M
68.R3610.20C
ISL6267HRTZ-T-GP
74.06267.A73
confrim Intersil by FAE,don't need L/S
Place close to PL4301
Place close to PL4201
110225-SC Wayne
101220
0609
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VREG : +VCC_CORE
JE40-SB
Monday, March 28, 2011
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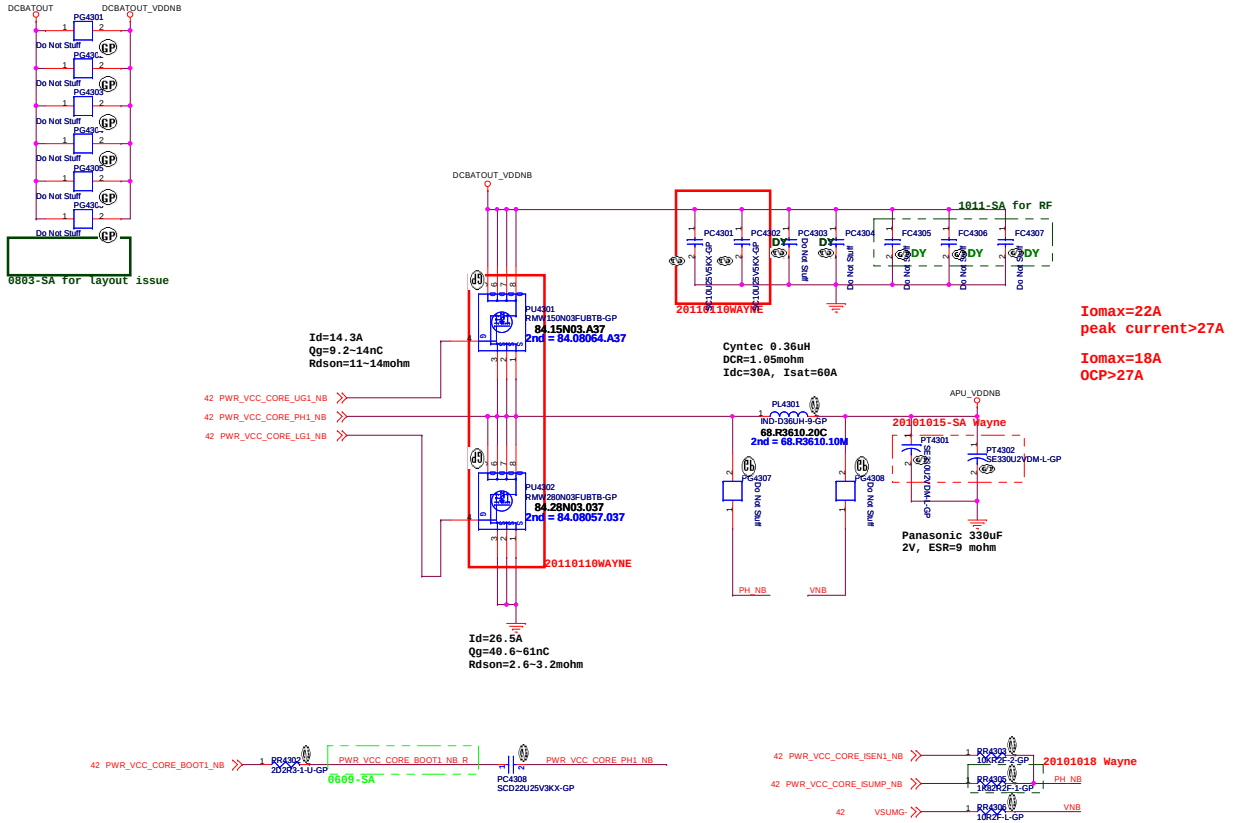

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VREG : +VCC_NB

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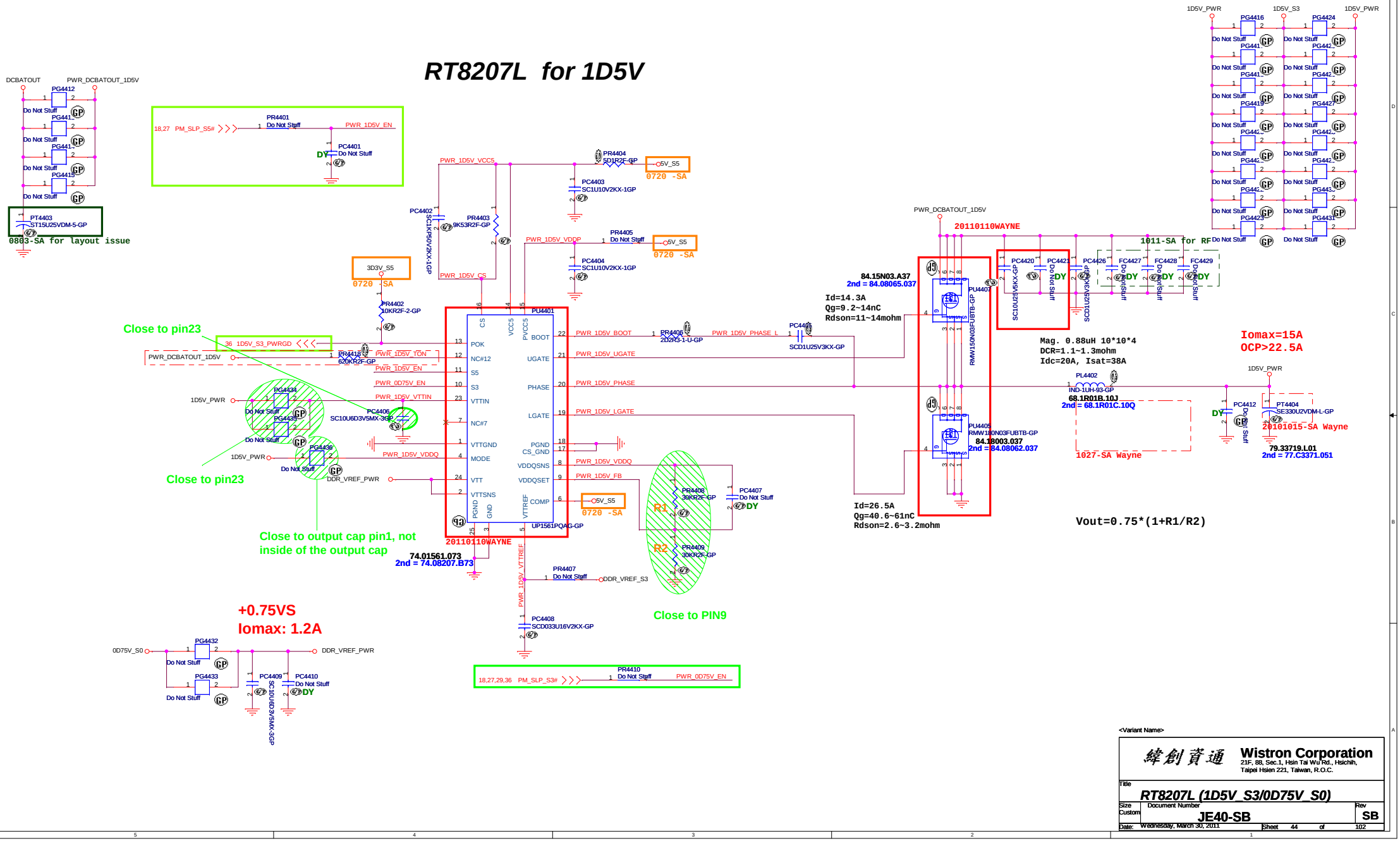
RT8207L for 1D5V



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207L (1D5V_S3/0D75V_S0)

Size: Custom | Document Number: JE40-SB | Rev: SB

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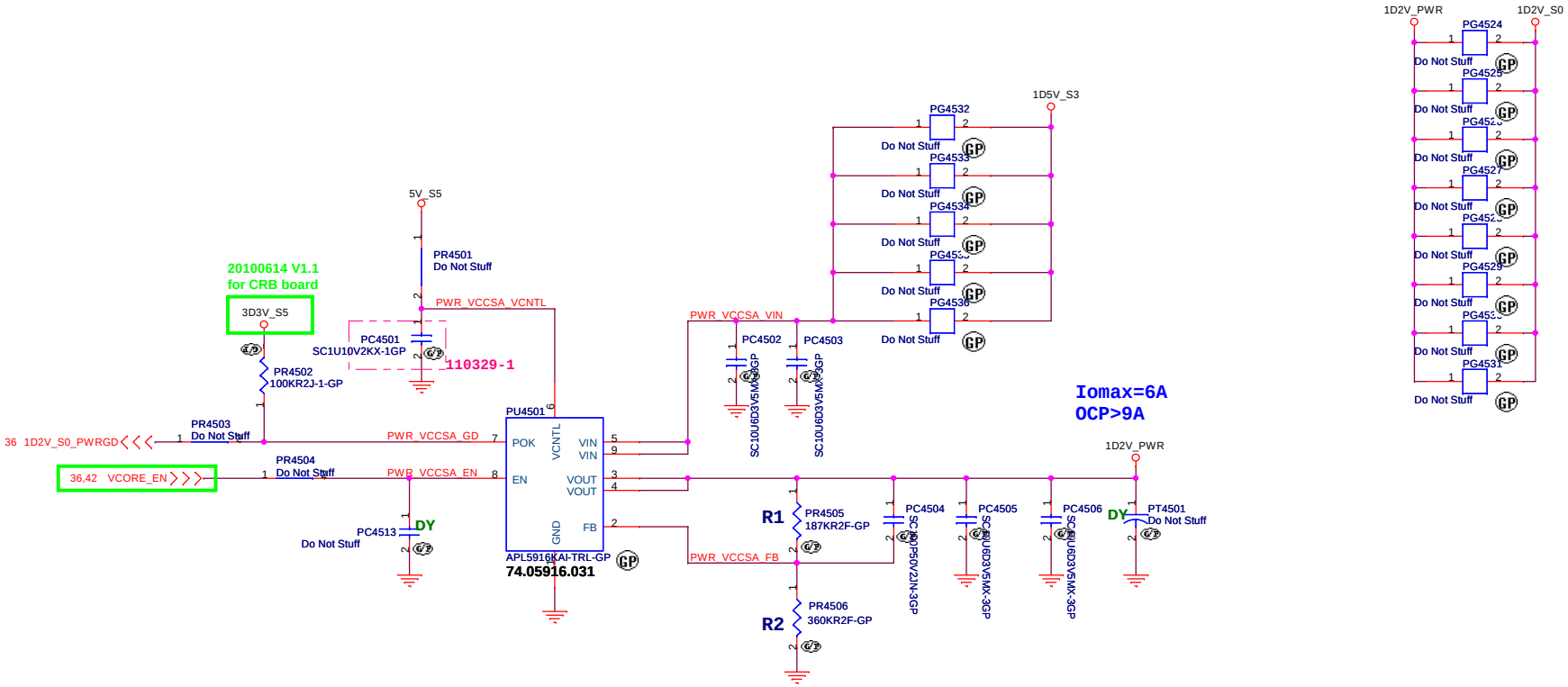
APL5916 for VDDR&VDDP(1D2V_S0)



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Title: APL5916(1D2V_S0)		
Size: A3	Document Number: JE40-SB	Rev: SB
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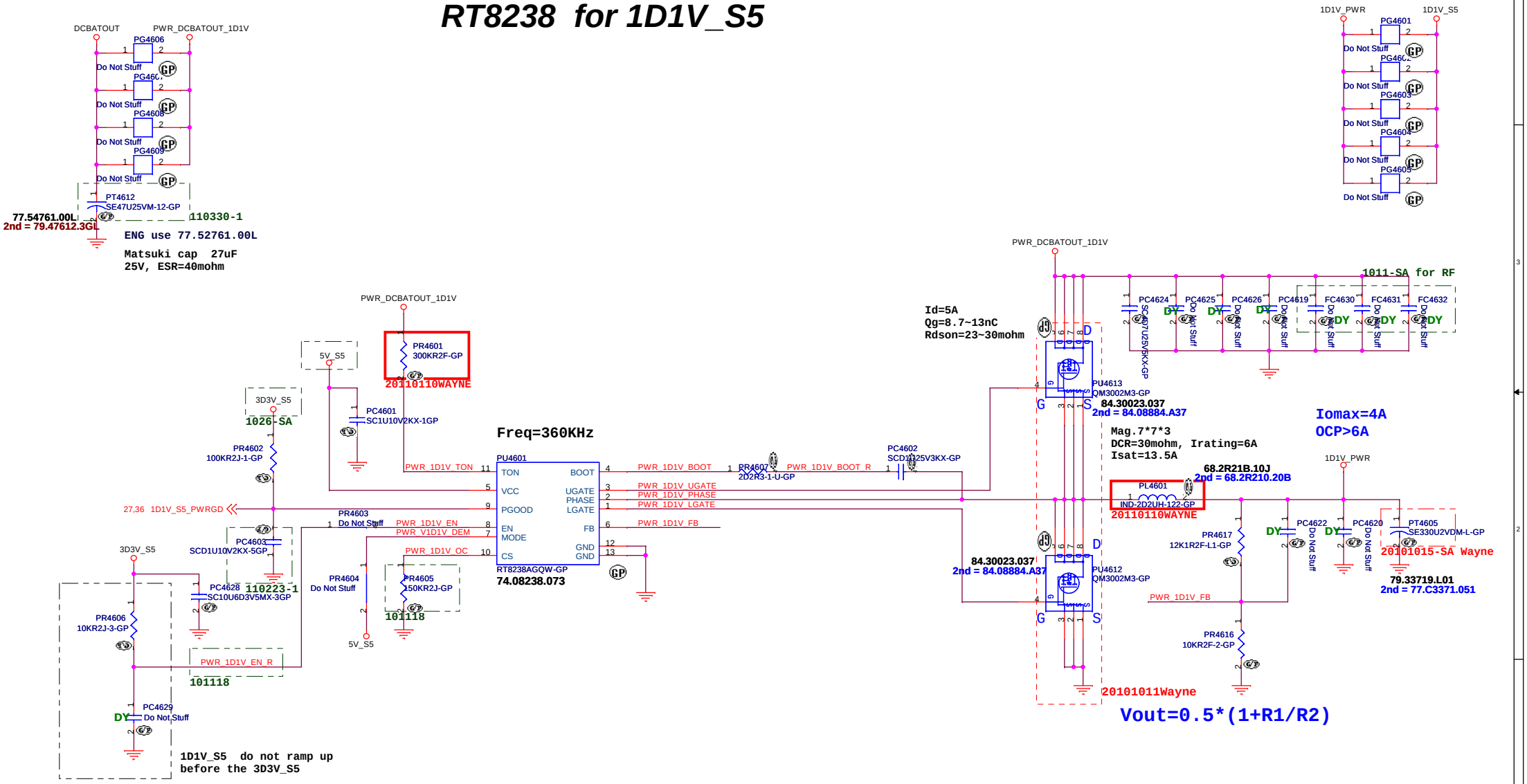
RT8238 for 1D1V_S5



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8238 (1D1V_S5)		
Size: A3	Document Number: JE40-SB	Rev: SB
Date: Wednesday, March 30, 2011	Sheet 46 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
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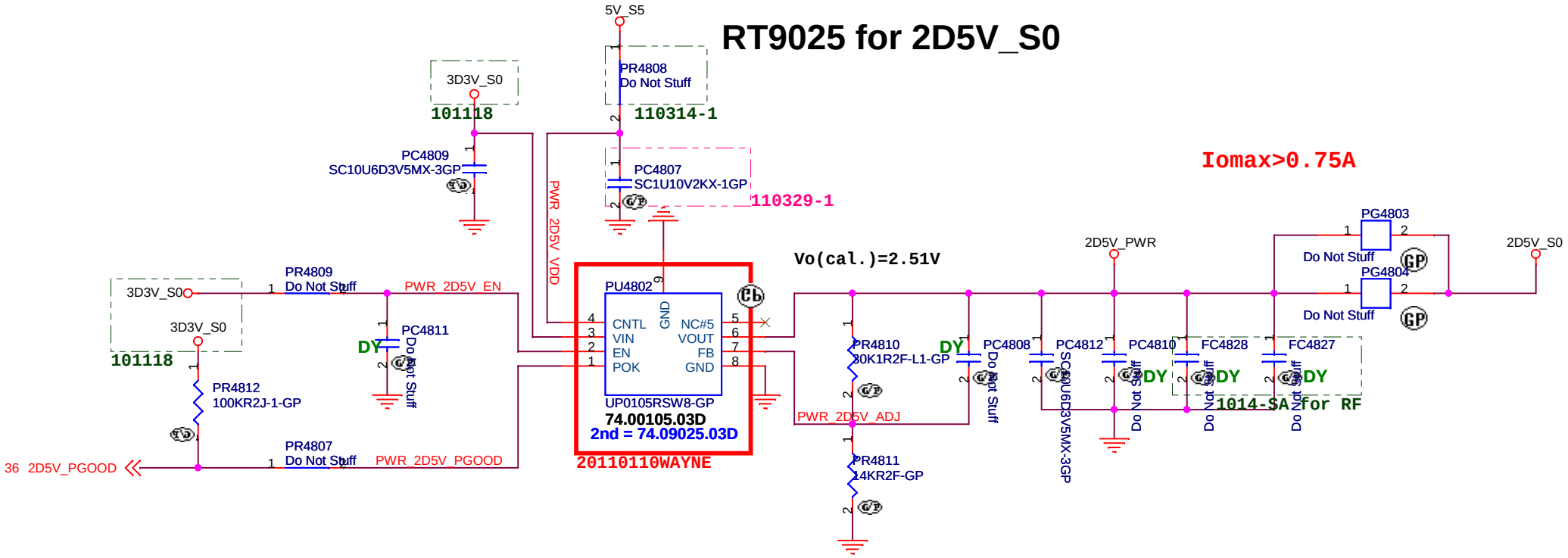
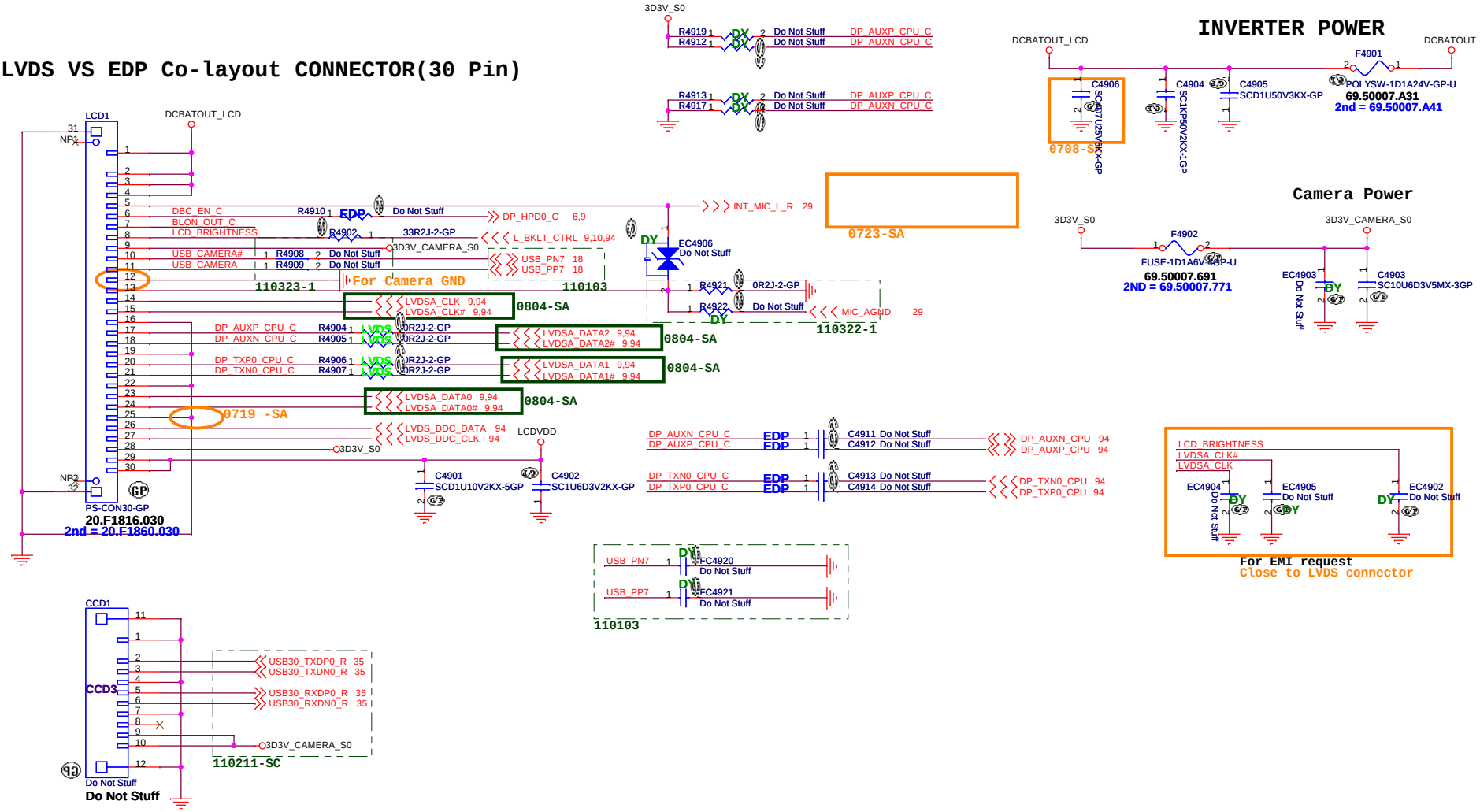
RT9025 for 2D5V_S0



<Variant Name>

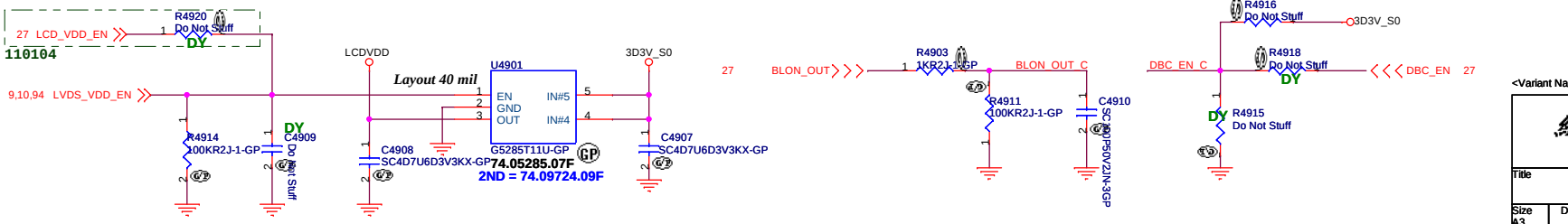
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RT9025(2D5V_S0)***
Size: A4	Document Number: **JE40-SB**
Rev: **SB**	
Date: Tuesday, March 29, 2011	Sheet 48 of 102

LVDS VS EDP Co-layout CONNECTOR(30 Pin)



INVERTER POWER

Camera Power



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size	Document Number	Rev
A3	JE40-SB	SB

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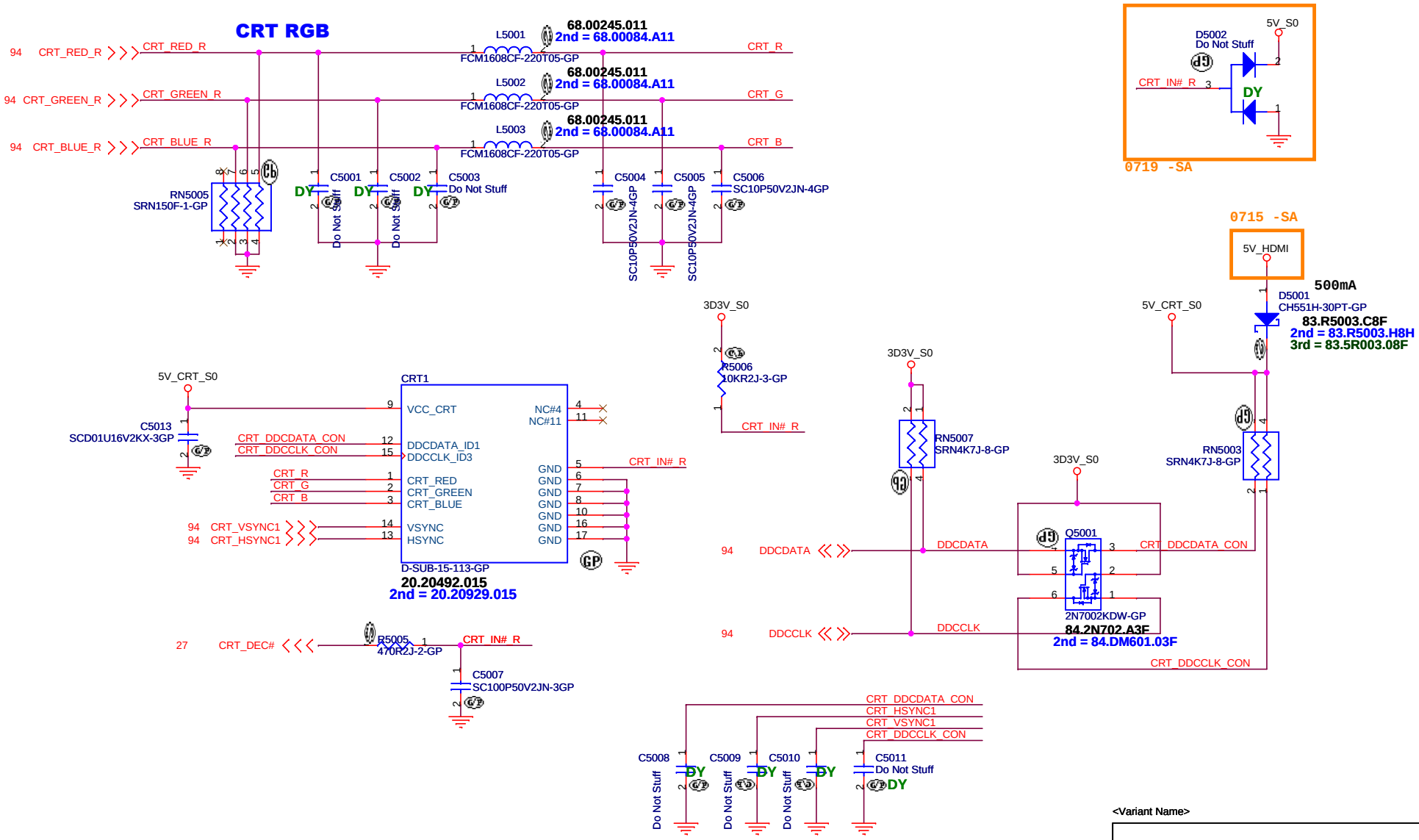

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT Connector***

Size	Document Number	Rev
Custom	JE40-SB	SB

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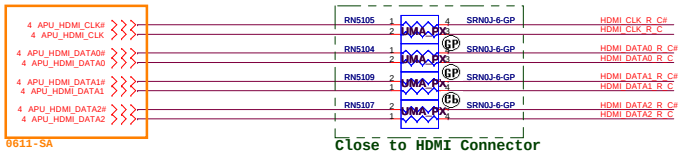
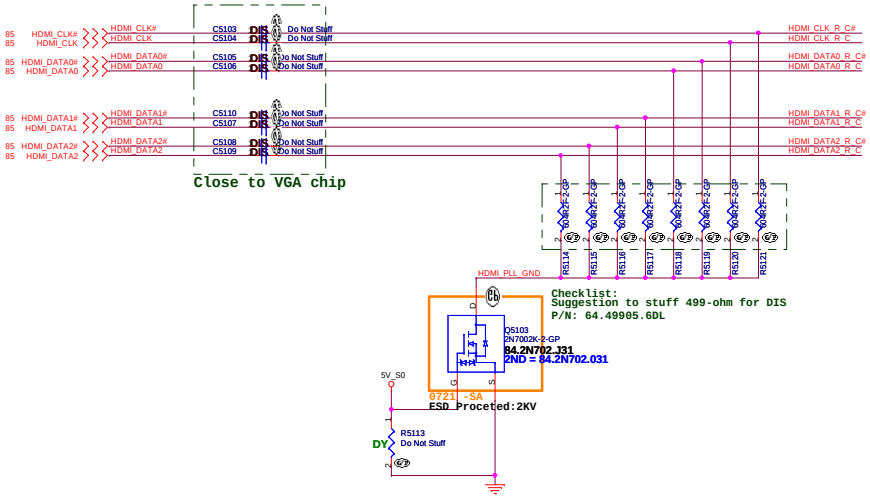
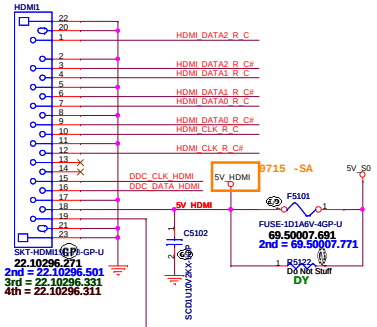
HDMI CONN

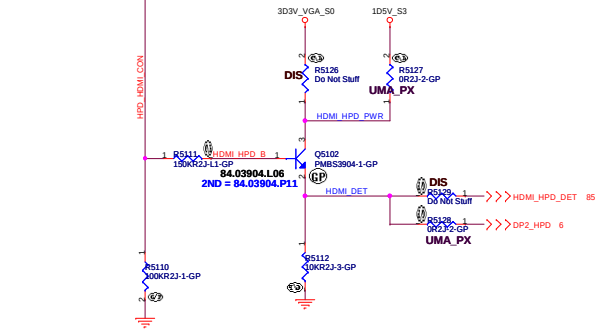
HDMI Level Shifter & CONNECTOR

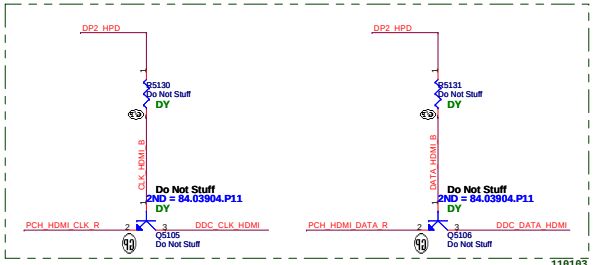


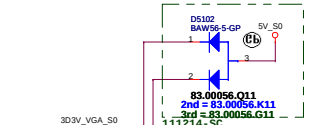
HDMI DISCRETE/ UMA Co-lay

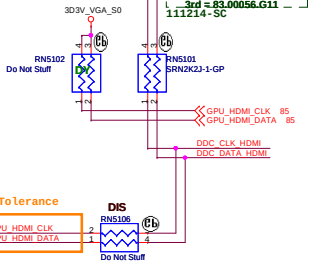


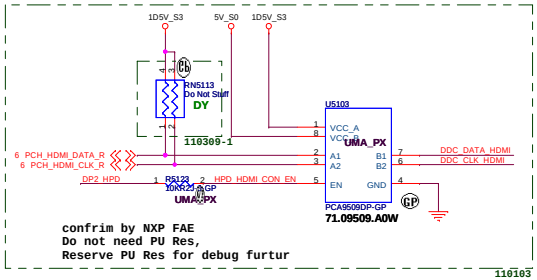




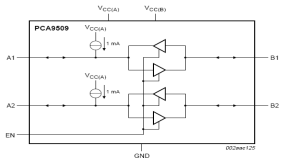








Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.



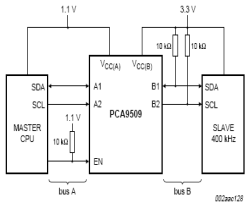


Fig 4. Typical application

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A2	JE40-SB	SB

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(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 52 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

Date: Friday, March 25, 2011 Sheet 53 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

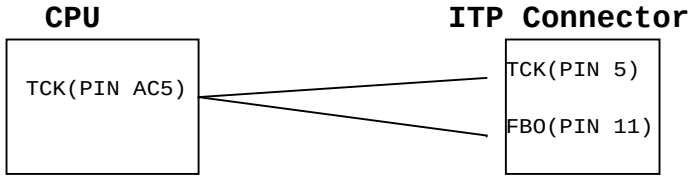
Reserved

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



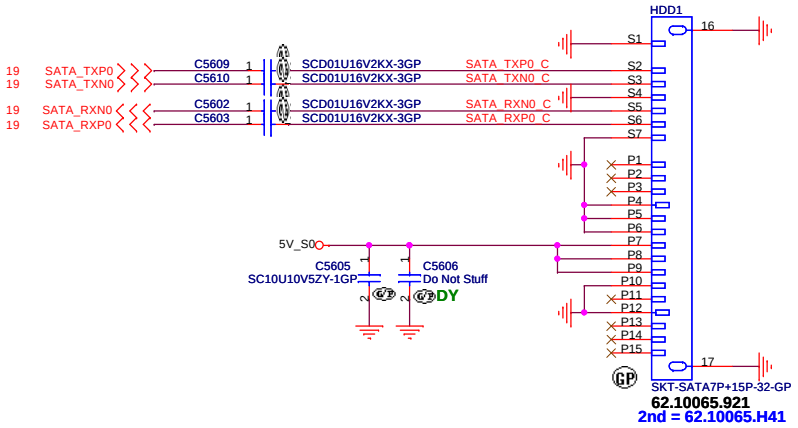
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP*		
Size: A4	Document Number: JE40-SB	Rev: SB
Date: Friday, March 25, 2011	Sheet 55 of 102	

SSID = SATA

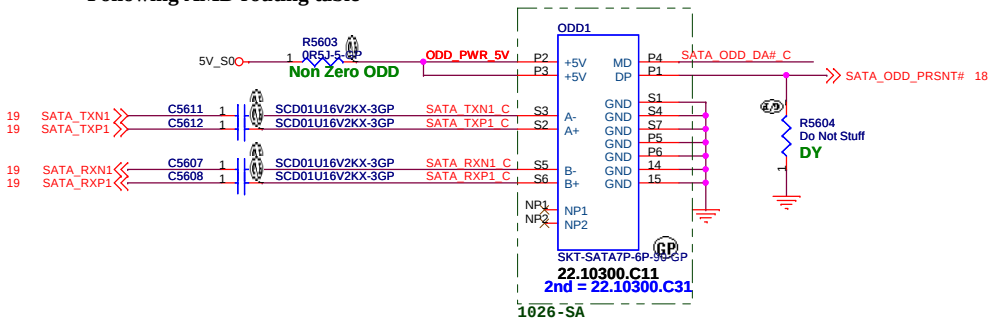
SATA HDD Connector

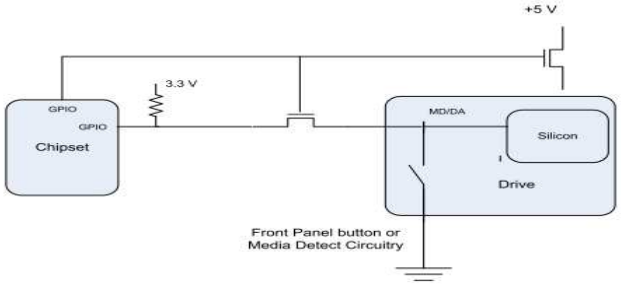


ODD Connector

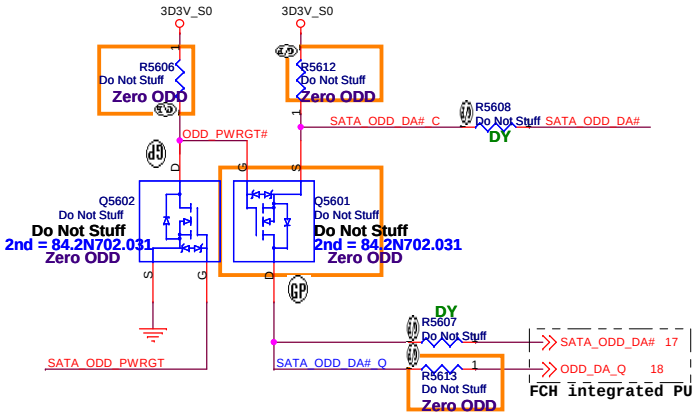
SATA_RX- and SATA_RX+ Trace
Length match within 10 mil

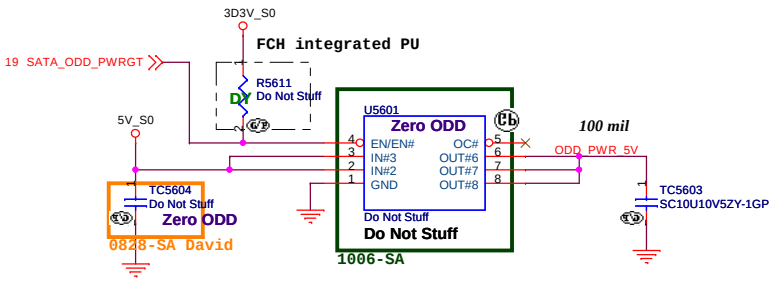
Following AMD routing table





When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON





Current limit
Active High
typ =>2.5A

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: JE40-SB	Rev: SB
Date: Monday, March 28, 2011	Sheet 56 of 102	

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ESATA/USB Charger*

Size	Document Number	Rev
A3	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 57 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio Jack

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

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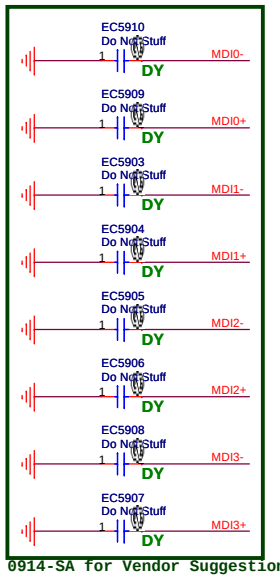
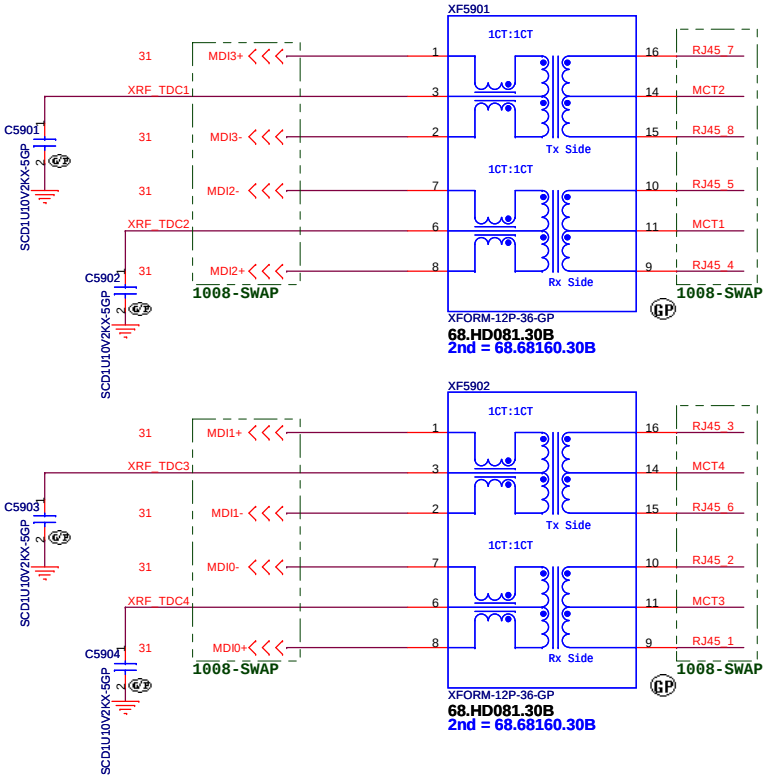
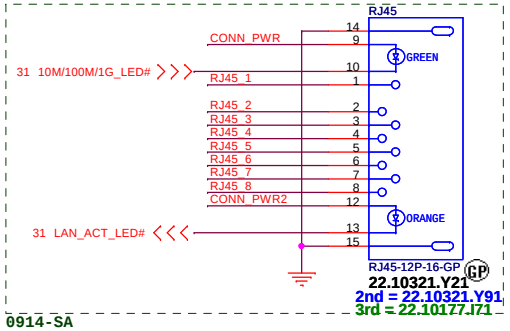
GIGA Lan Transformer

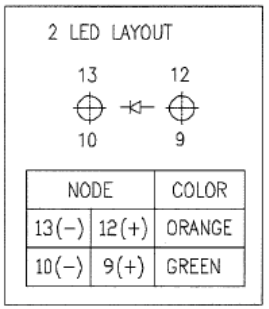


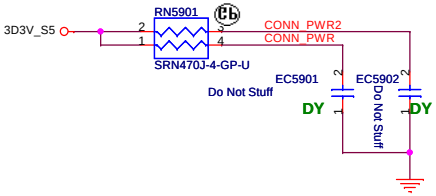
0914-SA for Vendor Suggestion

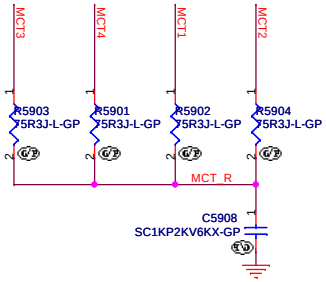


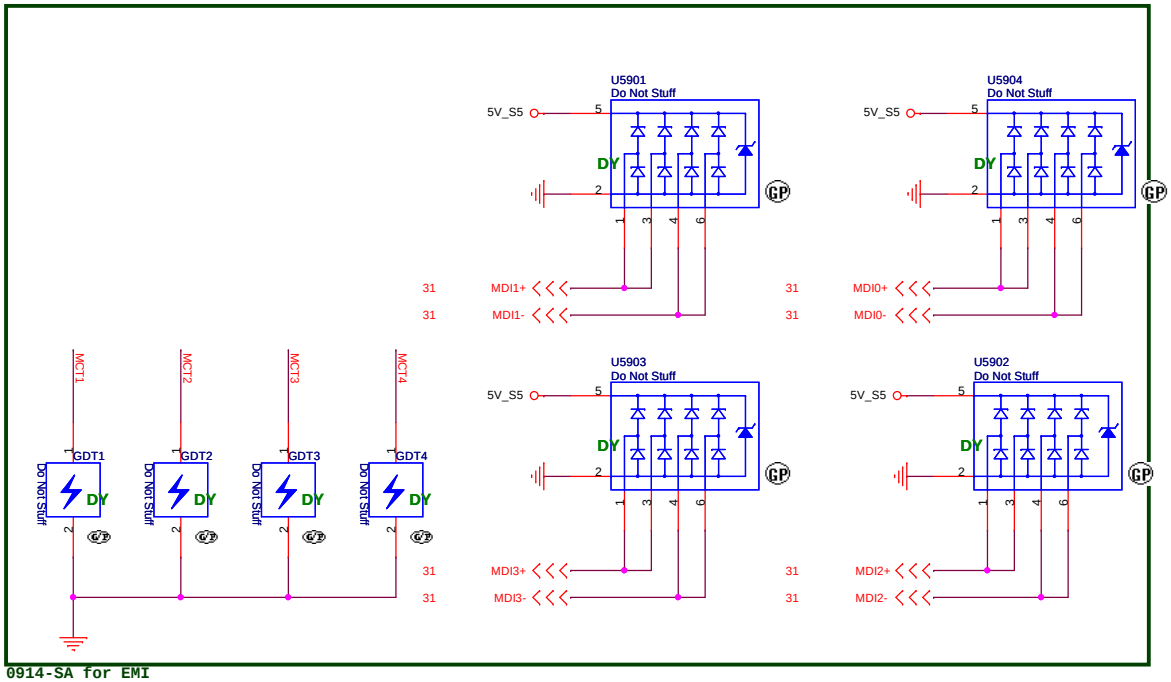


0914-SA

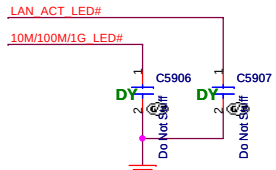








0914-SA for EMI



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN_CONN**

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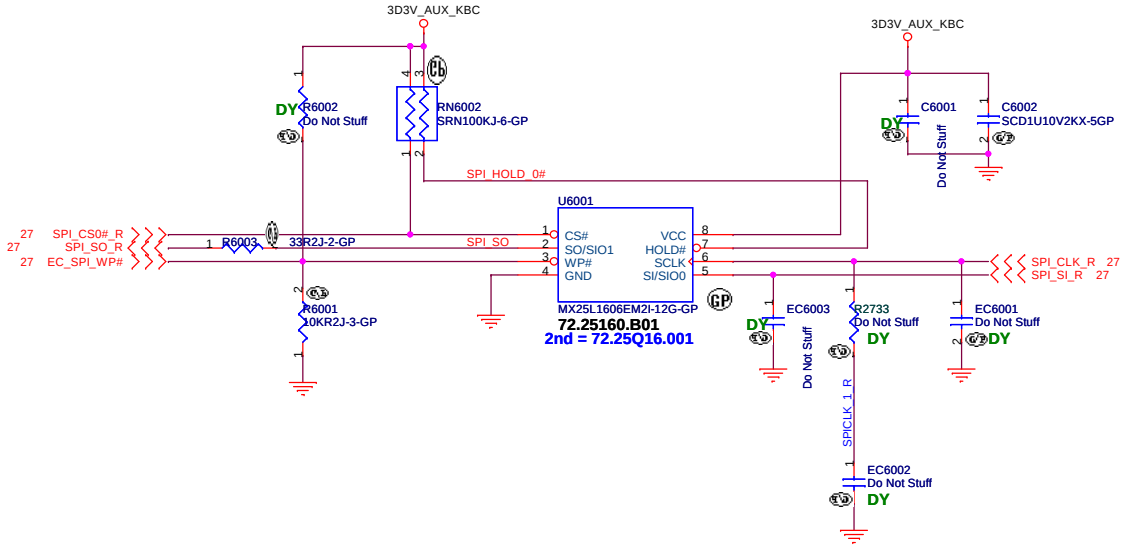
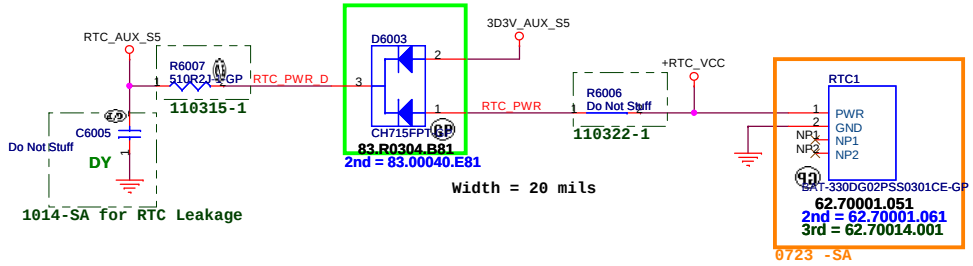
SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Flash/RTC	
Size A3	Document Number JE40-SB	Rev SB
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size	Document Number	Rev
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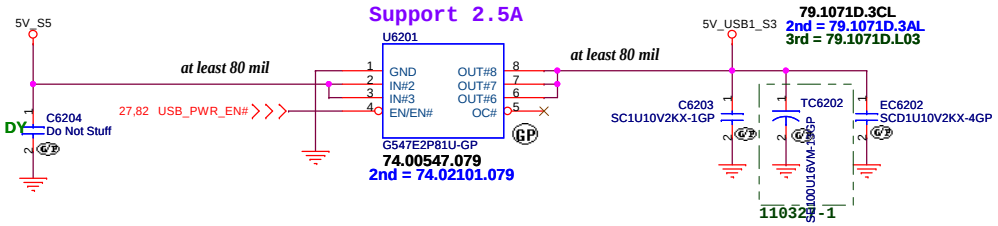
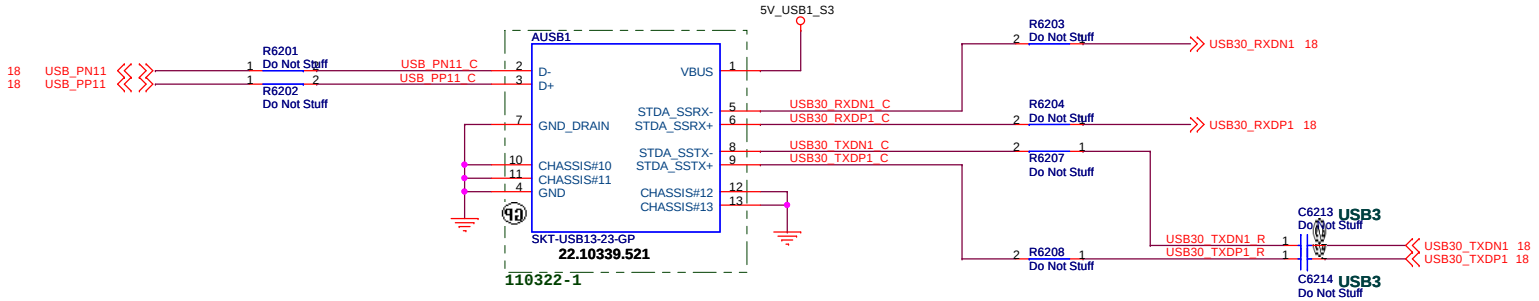
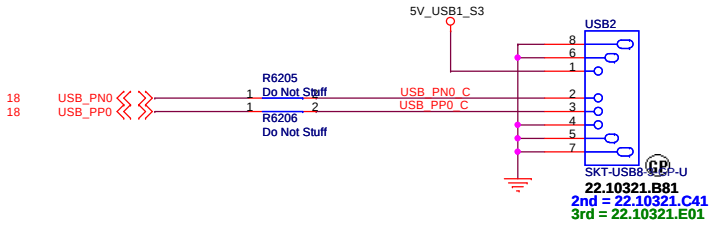


USB3.0 CONNECTOR





USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0

Size: A3 | Document Number: JE40-SB | Rev: SB

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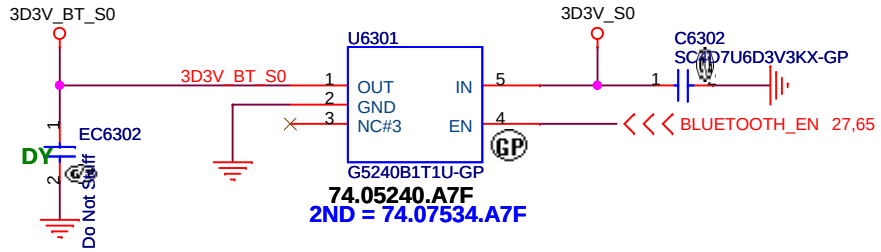
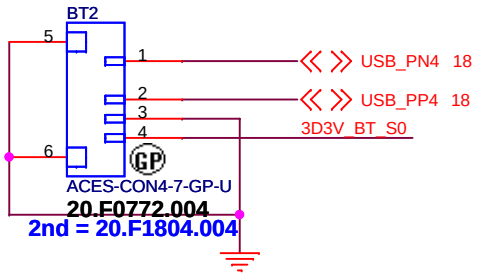
ANNIE Bluetooth Module

1.5A / High Active Voltage 2V



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLUE TOOTH**		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	F/P	
Size A4	Document Number JE40-SB	Rev SB
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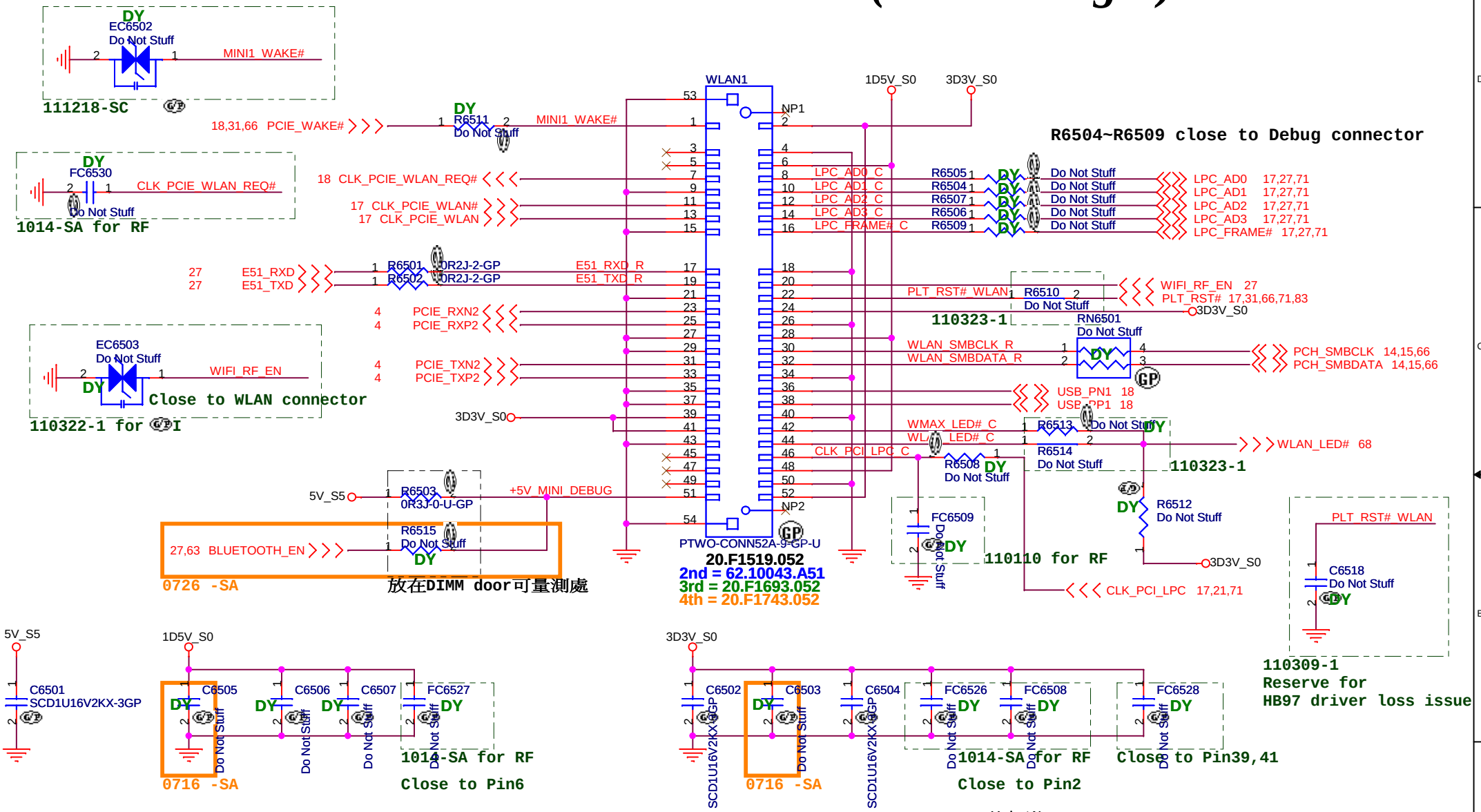
Mini Card Connector(802.11a/b/g/n)



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WLAN**

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A4	JE40-SB	SB

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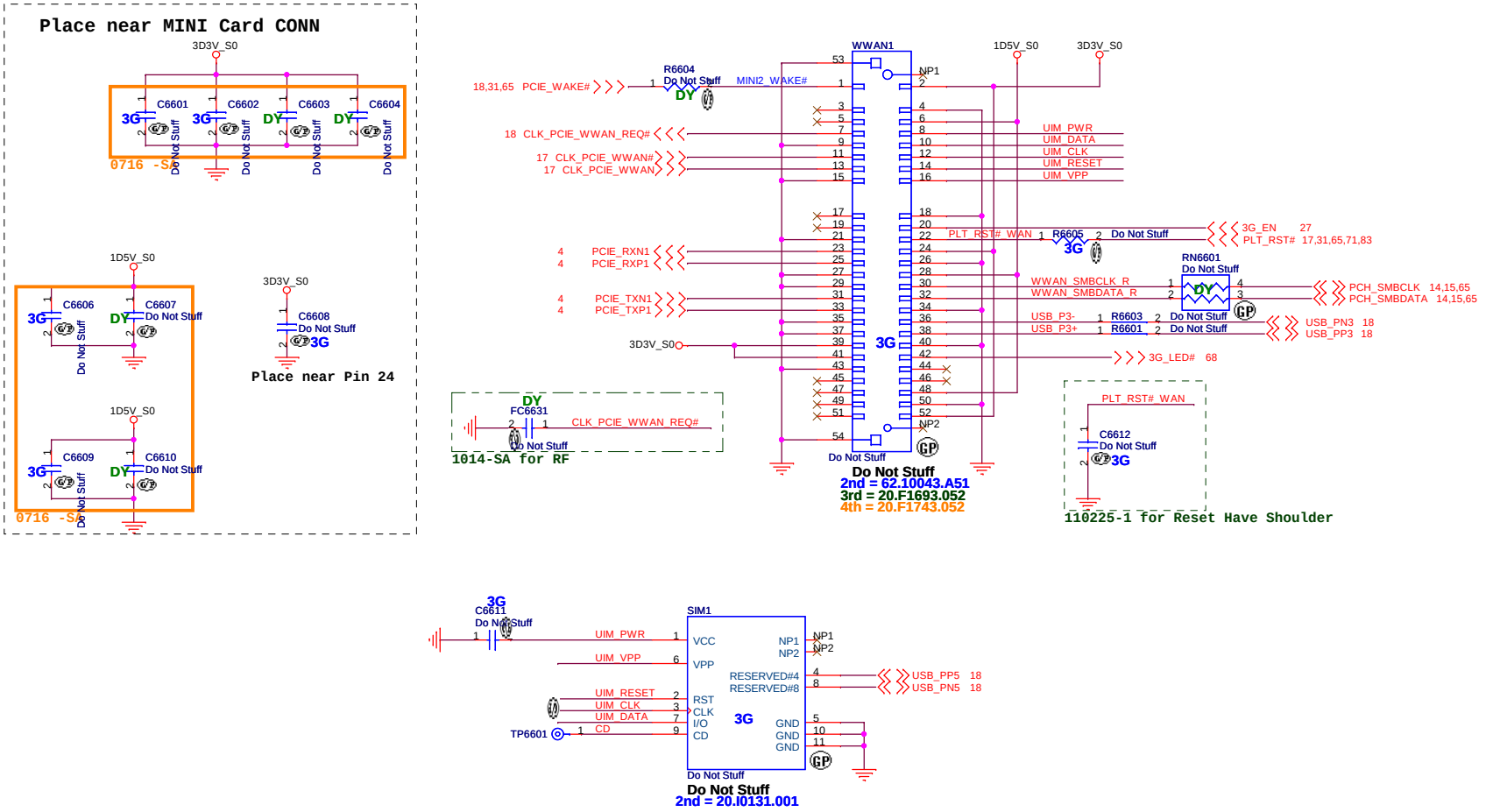
Mini Card Connector(WWAN)



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **WWAN**		
Size: A3	Document Number: **JE40-SB**	Rev: **SB**
Date: Wednesday, March 30, 2011	Sheet 66 of 102	

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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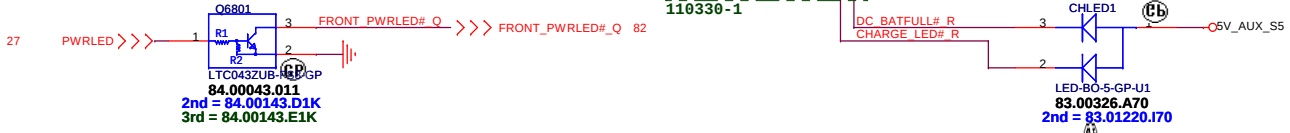
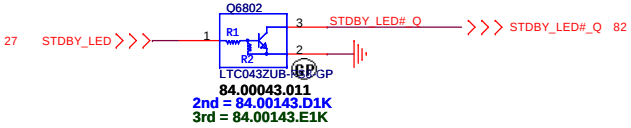
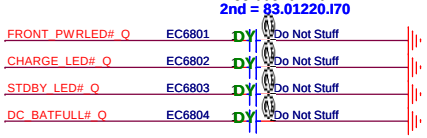
Power button LED

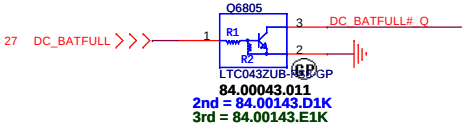


Power STDBY_LED

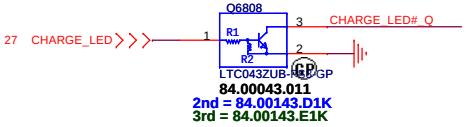




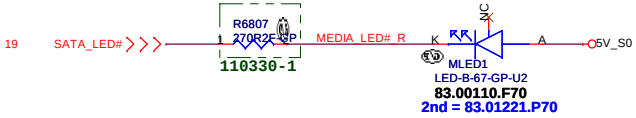
Battery LED2(DC_BATFULL)

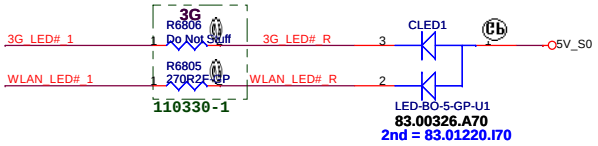


Battery LED1(CHARGE)

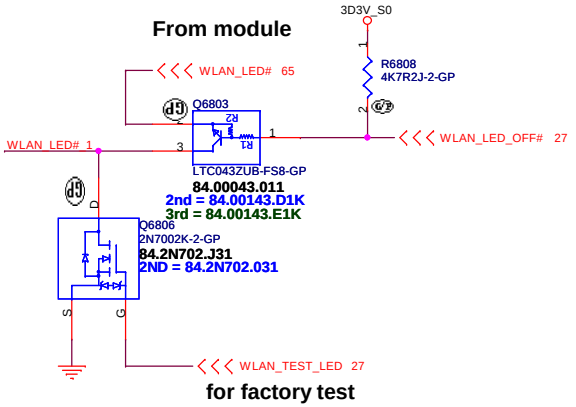


SATA HDD LED

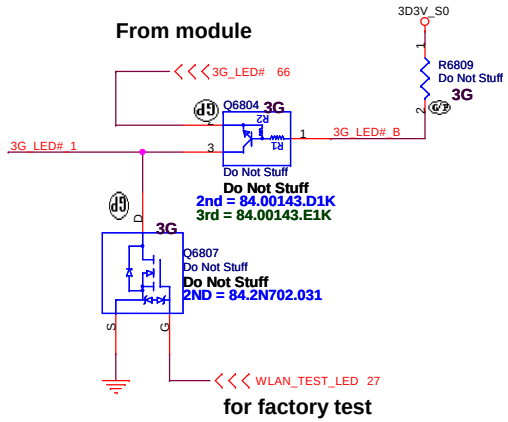




WLAN_LED



3G LED



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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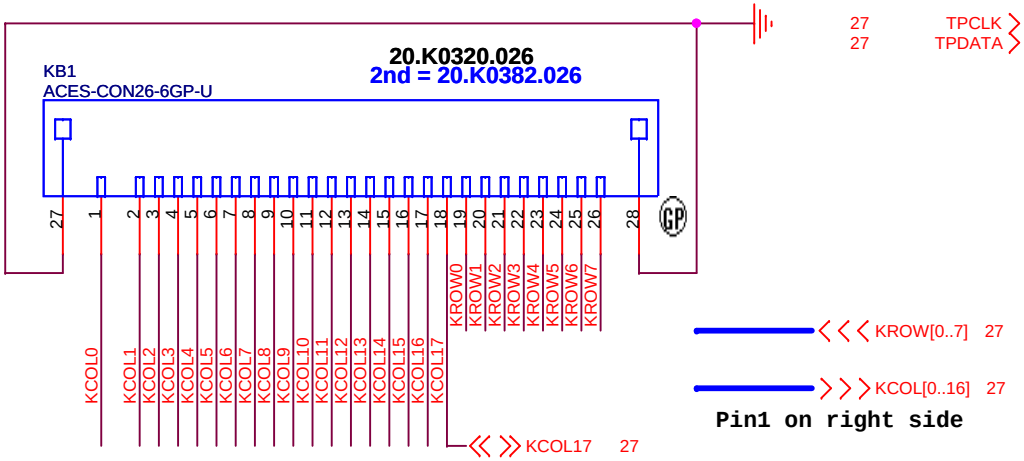
Internal KeyBoard Connector

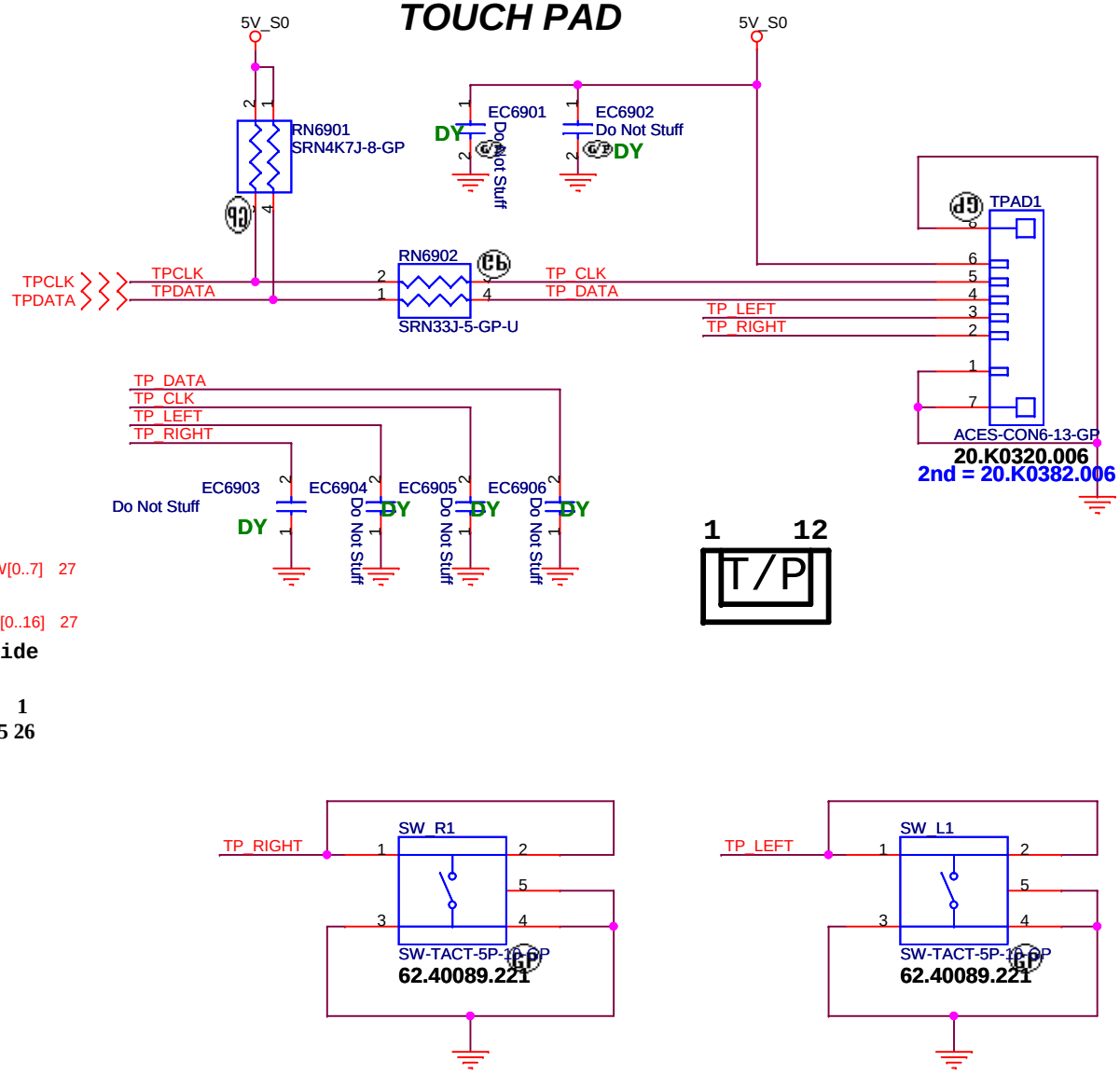


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

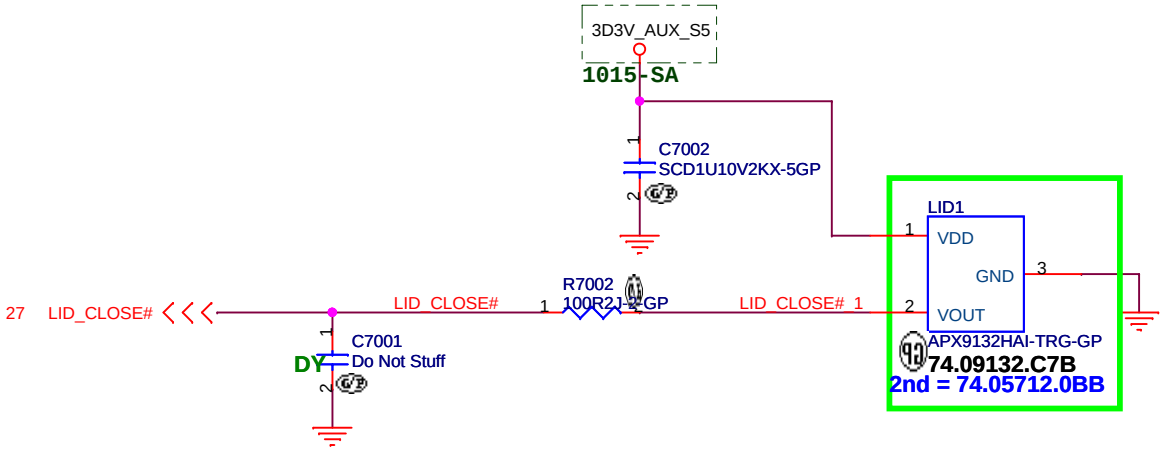
TOUCH PAD



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Key Board/Touch Pad**	
Size A4	Document Number **JE40-SB**	Rev **SB**
Date: Monday, March 28, 2011	Sheet 69 of 102	



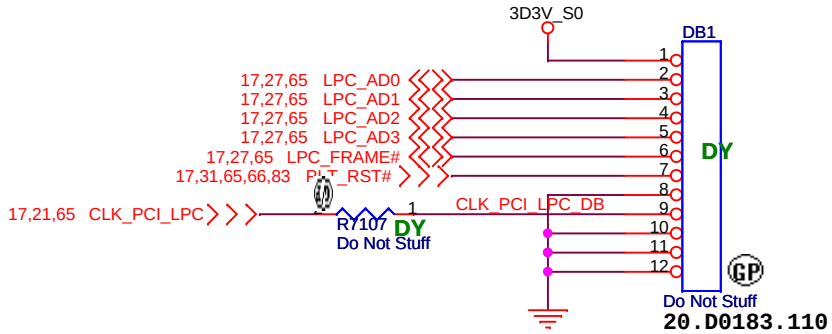
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

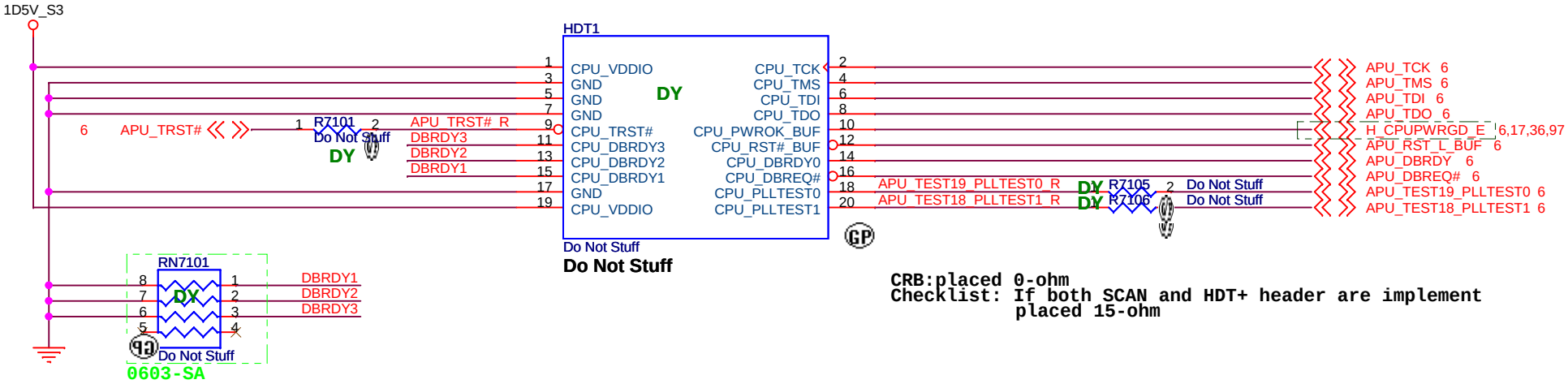
Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

Date: Monday, March 28, 2011 Sheet 70 of 102



HDT+ Connectors



Do Not Stuff

```
CRB:placed 0-ohm
Checklist: If both SCAN and HDT+ header are implement
           placed 15-ohm
```

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Dubug connector***	
Size A4	Document Number **JE40-SB**	Rev **SB**
Date: Monday, March 28, 2011	Sheet 71 of 102	

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<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 72 of 102	

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<Variant Name>

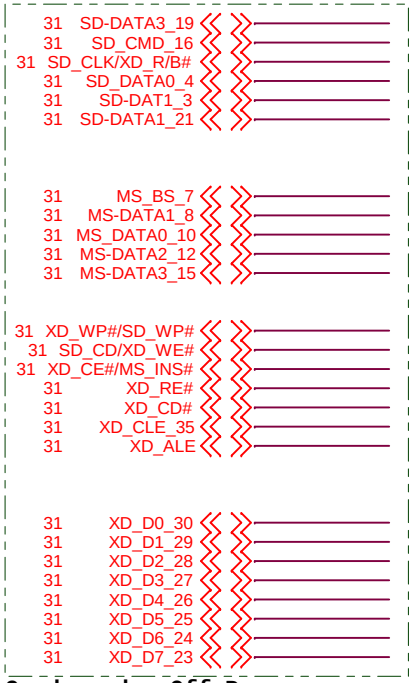
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

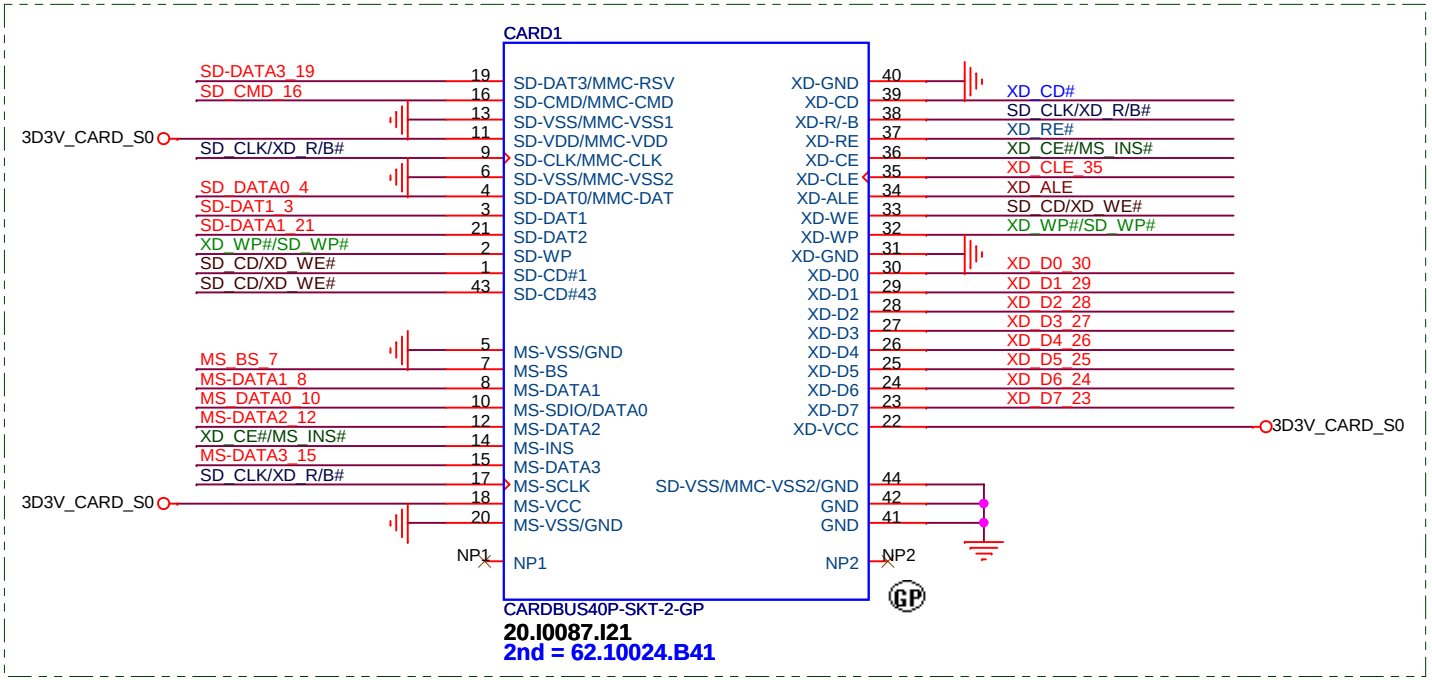
Size	Document Number	Rev
A4	**JE40-SB**	**SB**

Date: Friday, March 25, 2011 Sheet 73 of 102

SD/XD/MS Card Reader



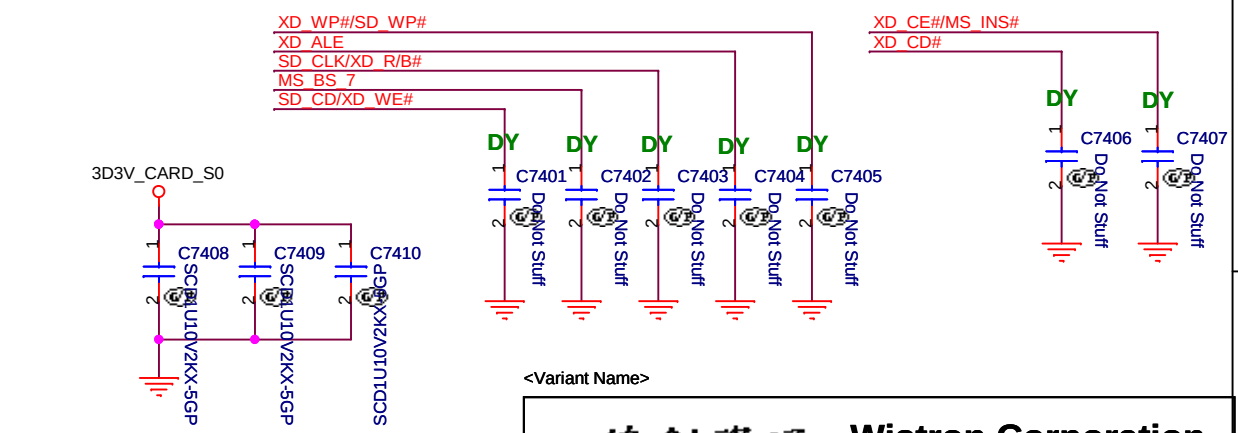
Card-reader Off-Page



110112

Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-D0		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P 1P/9P
P14	MS-VCC		9P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/6P	1P/10P 1P/9P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	XD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	



Near CARD1 Pin11, Pin18, Pin22

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 74 of 102

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<Variant Name>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Express Card

Size	Document Number	Rev
A4	**JE40-SB**	**SB**

Date: Friday, March 25, 2011 Sheet 75 of 102

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 76 of 102	

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<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 77 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 78 of 102

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<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-SB**	Rev: **SB**
Date: Friday, March 25, 2011	Sheet 79 of 102	

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A	JE40-SB	SB

Date: Friday, March 25, 2011 Sheet 80 of 102

(Blanking)

<Variant Name>

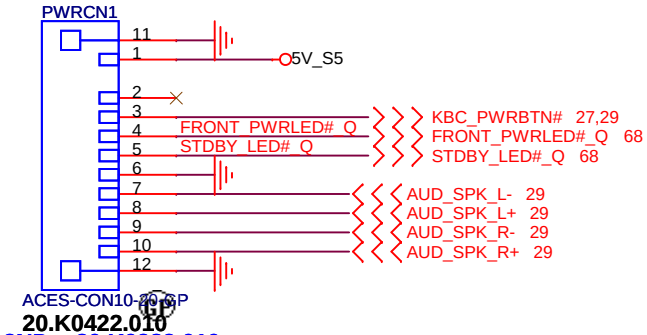
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
UNUSED PARTS/EMI Capacitors

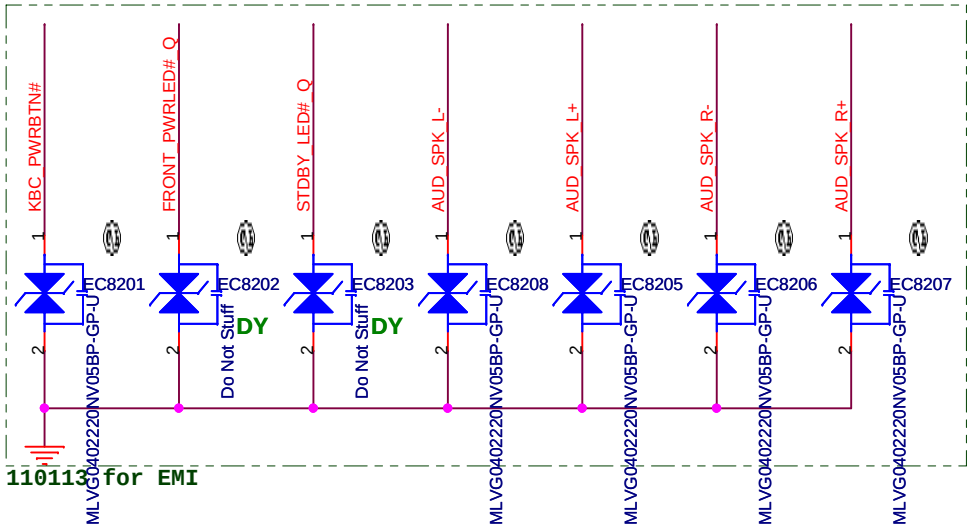
Size	Document Number	Rev
A4	**JE40-SB**	**SB**

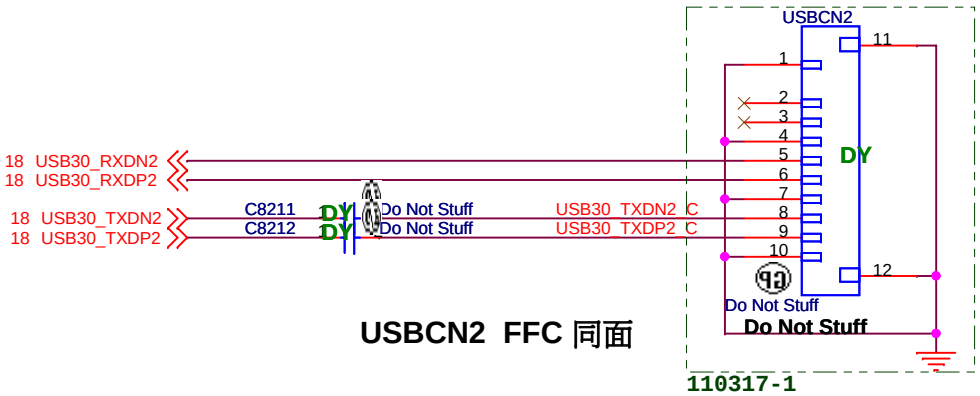
Date: Friday, March 25, 2011 Sheet 81 of 102

PWRCN1 FFC 異面

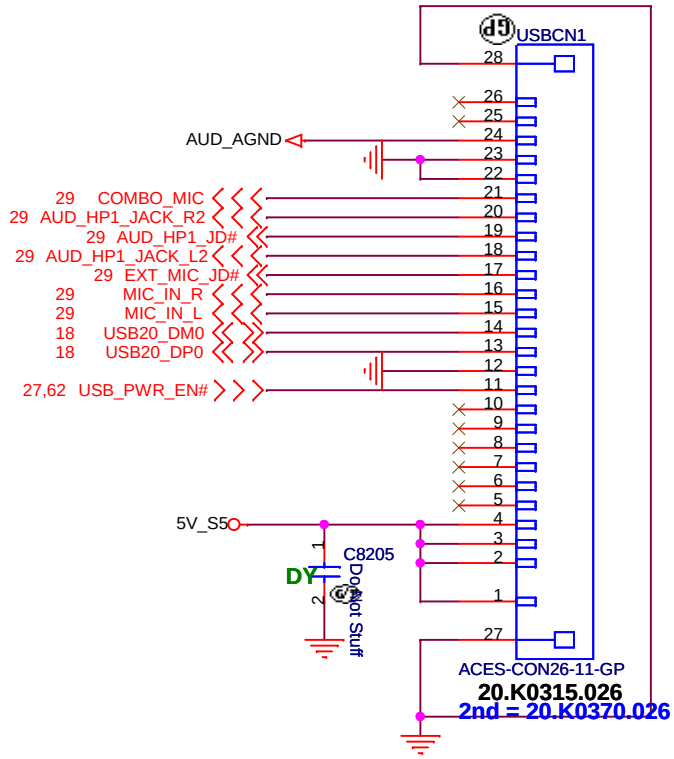


Pin 1 Right side





USBCN2 FFC 同面



USBCN1 FFC 同面

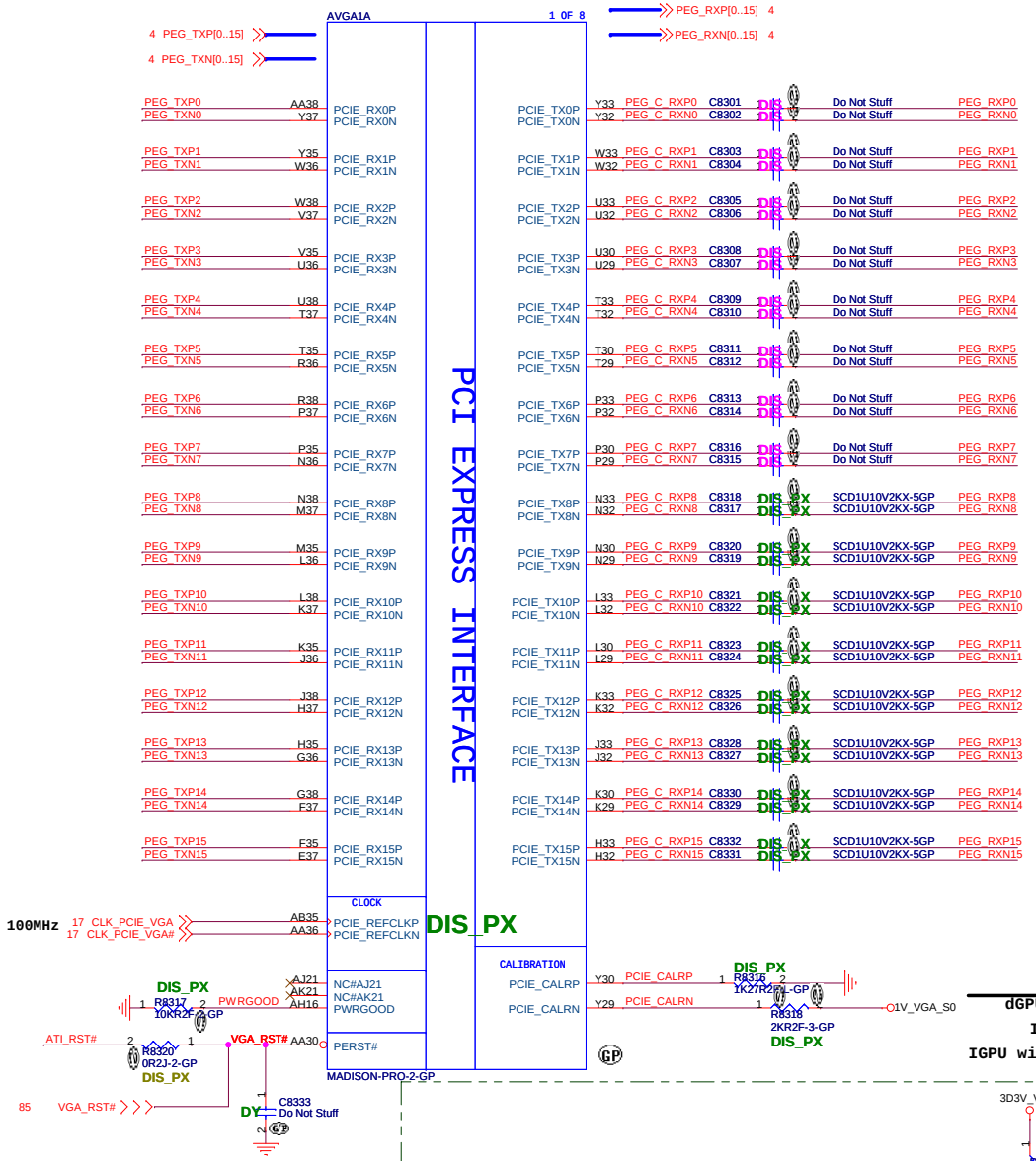
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A4	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 82 of 102



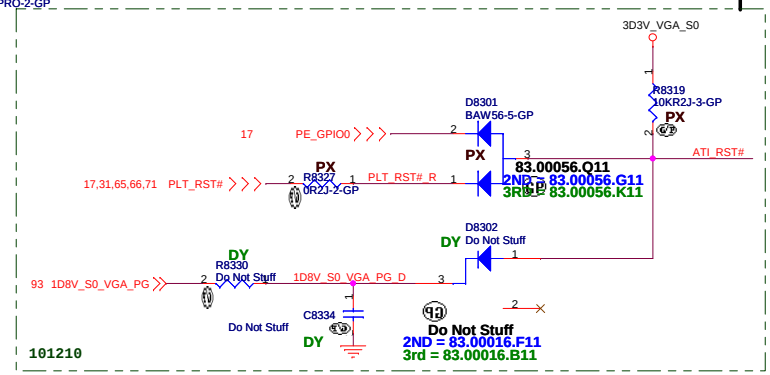
CONFIGURATION STRAPS

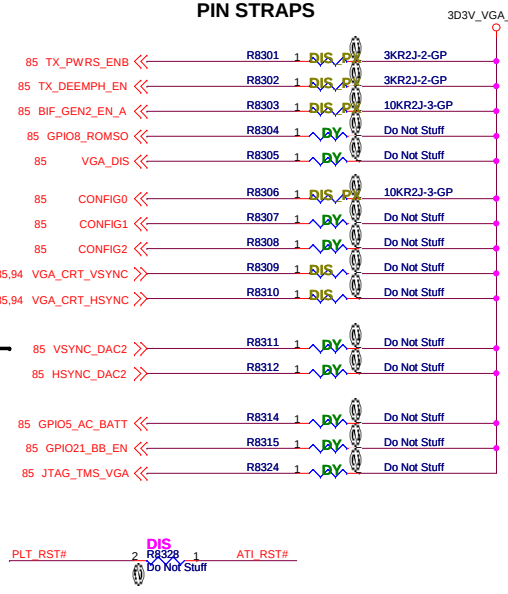
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

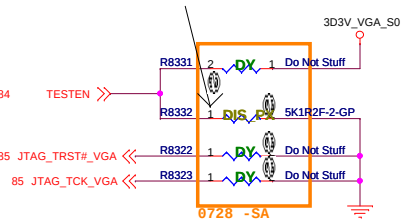
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PE_GPIO0	
dGPU mode	H
IGPU	L
IGPU with BACO	H







JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

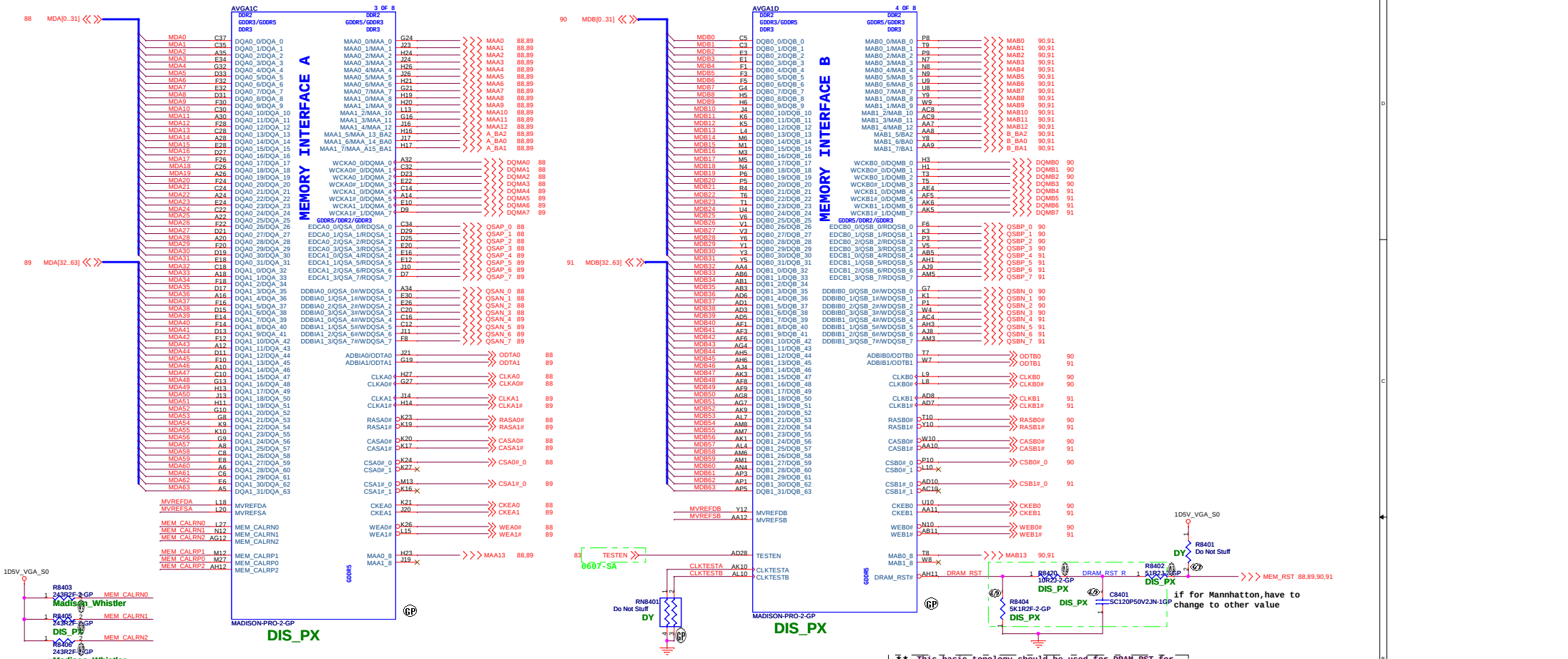
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_PCIE/STRAPPING(1/5)**

Size: Custom | Document Number: **JE40-SB** | Rev: **SB**

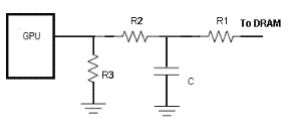
Date: Monday, March 28, 2011 | Sheet 83 of 102



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

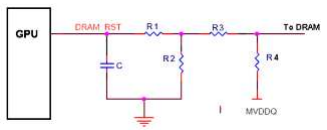
** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Vancouver



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

Mannhatton



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size	Document Number	Rev
Custom	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 84 of 102

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

Address	DVPDATA[3:0]	Vender	PN	Speed	
0	0 0 0 0	Hynix	H5TQ1G63DFR-11C	1Gb(64Mx16)	900Mhz	Rev D Die NEW ! !
1	0 0 0 1	Hynix	H5TQ2G63BFR-11C	2Gb(128Mx16)	900Mhz	Rev B Die
2	0 0 1 0	Reserve			
3	0 0 1 1	Hynix	H5TQ1G63DFR-12C	1Gb(64Mx16)	800Mhz	Rev D Die NEW ! !
4	0 1 0 0	Hynix	H5TQ1G63BFR-12C	1Gb(64Mx16)	800Mhz	Rev B Die
5	0 1 0 1	Reserve			
6	0 1 1 0	Reserve			
7	0 1 1 1	Hynix	H5TQ2G63BFR-11C	2Gb(128Mx16)	800Mhz	Rev B Die
8	1 0 0 0	Samsung	K4W1G1646E-HC12	1Gb(64Mx16)	800Mhz	Rev E Die
9	1 0 0 1	Samsung	K4W2G1646C-HC11	2Gb(128Mx16)	900Mhz	Rev C Die NEW ! !
10	1 0 1 0	Reserve			
11	1 0 1 1	Samsung	K4W2G1646B-HC12	2Gb(128Mx16)	800Mhz	Rev B Die
12	1 1 0 0	Samsung	K4W1G1646G-BC11	1Gb(64Mx16)	900Mhz	Rev G Die NEW ! !
13	1 1 0 1	Reserve			
14	1 1 1 0	ATI	23EY4187MA11 2Gb (128x16)		900Mhz	
15	1 1 1 1	Samsung	K4W1G1646G-BC12	1Gb(64Mx16)	800Mhz	Rev G Die NEW ! !

LVDS Interface

I2C Bus for LVDS

Straps

110111 delete

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Bead:470-ohm 1.5A

1022-SA
Use same parts for VGA DPPower

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

1022-SA
TM Derek Hsieh suggestion

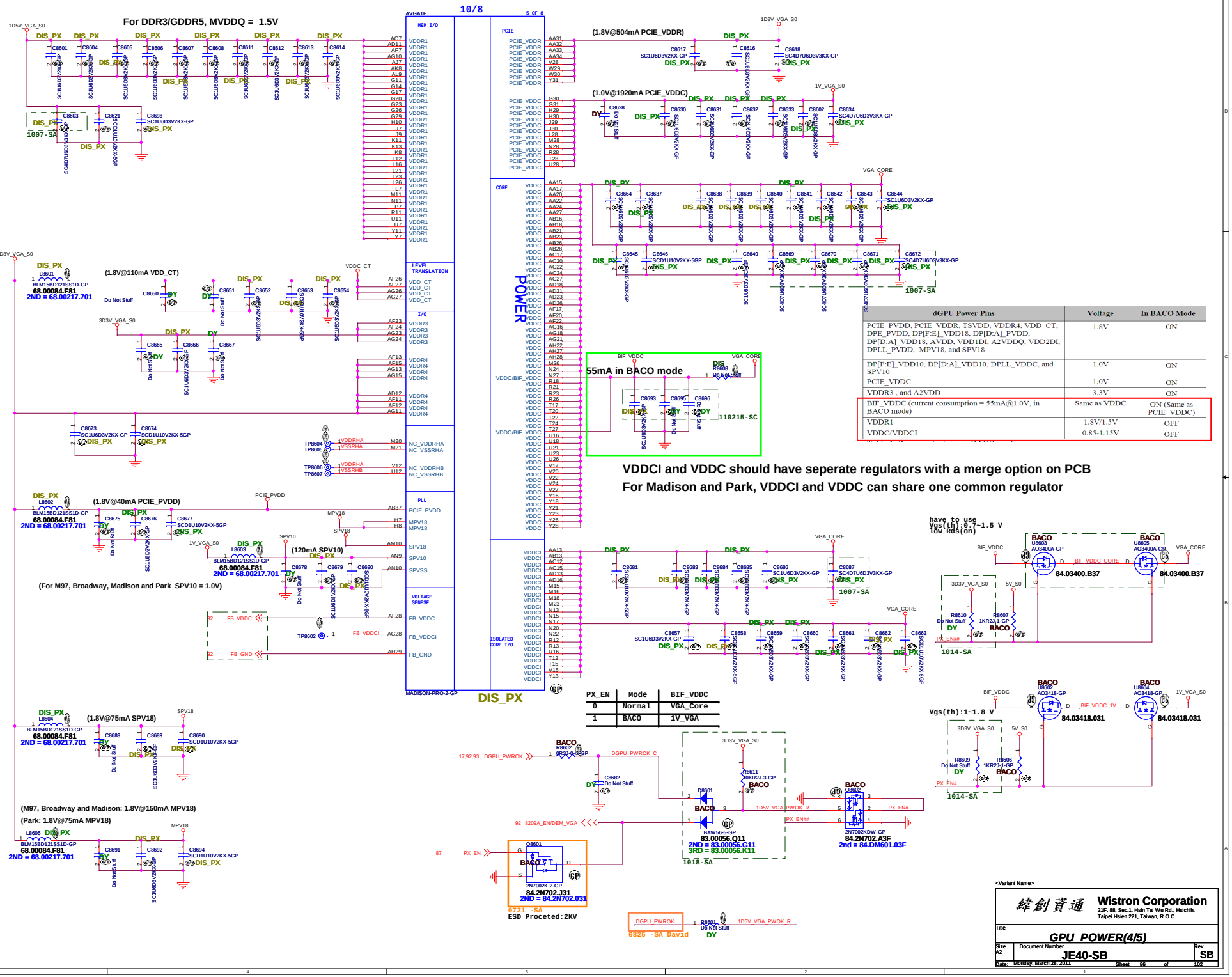
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
A2	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 85 of 102



dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 , and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85~1.15V	OFF

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

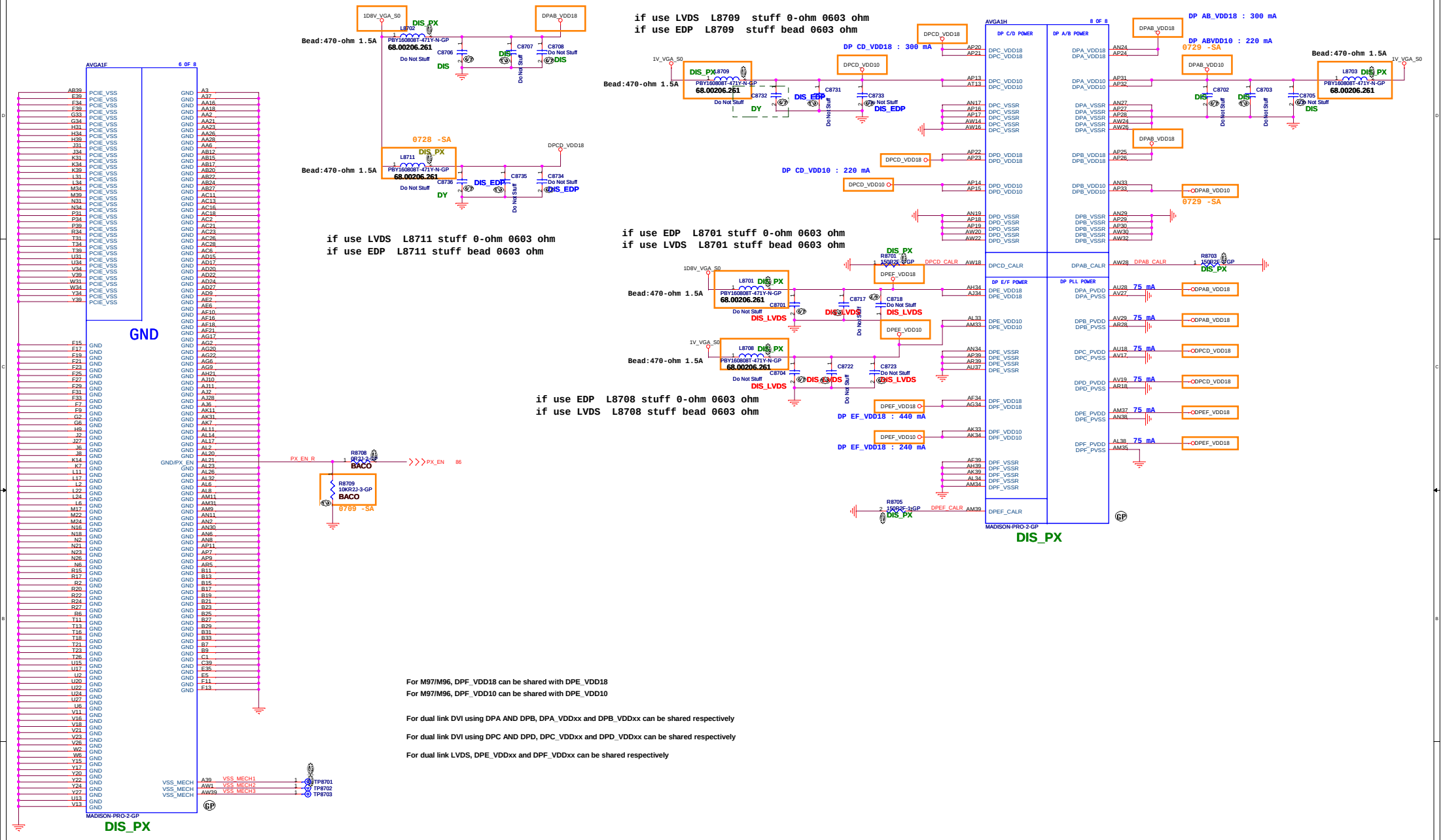
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

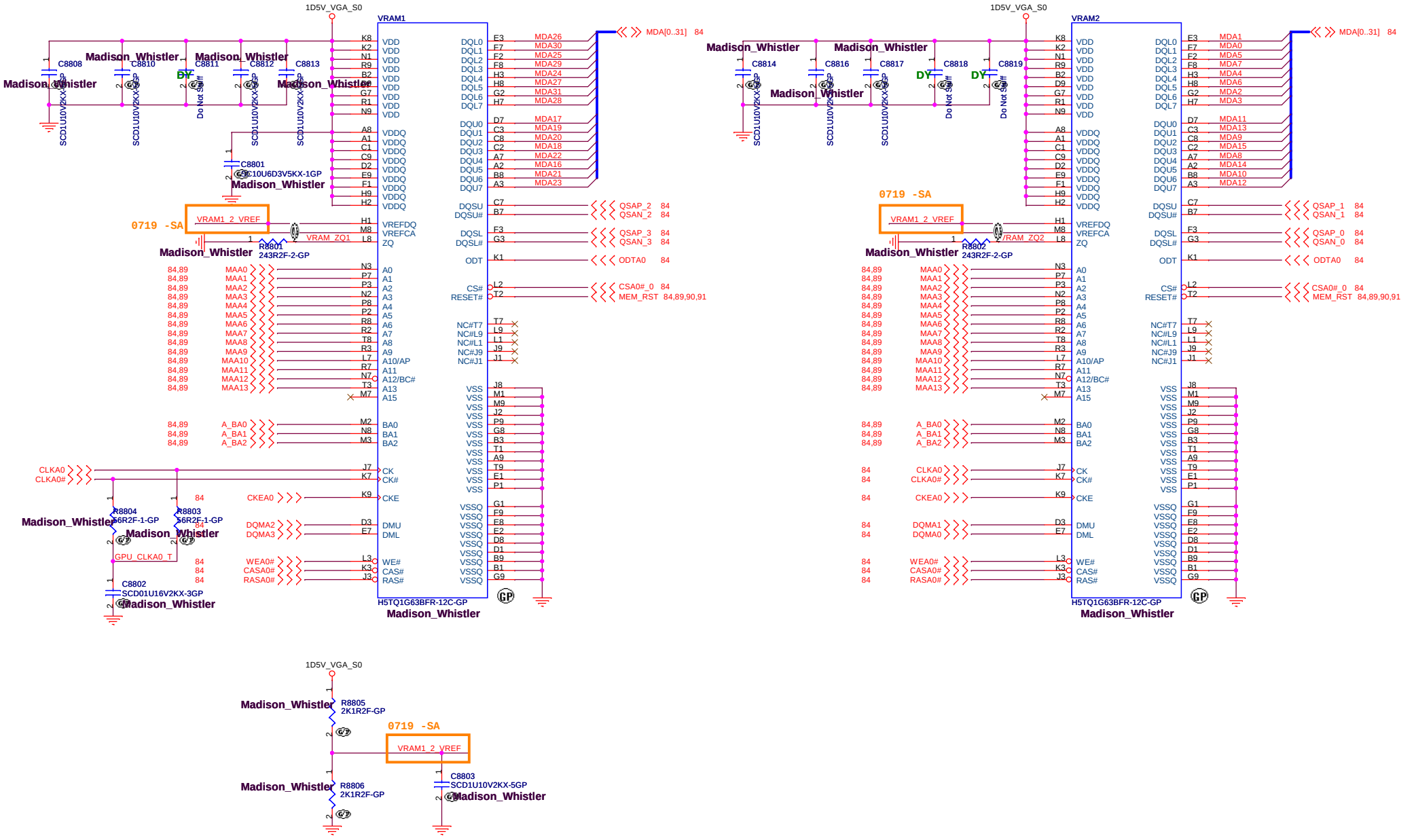
Size	Document Number	Rev
A2	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 86 of 102



<variant_name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU_DPPWR/GND(5/5)	
Size A2	Document Number JE40-SB	Rev SB
Date: Monday, March 28, 2011	Sheet 87 of 102	



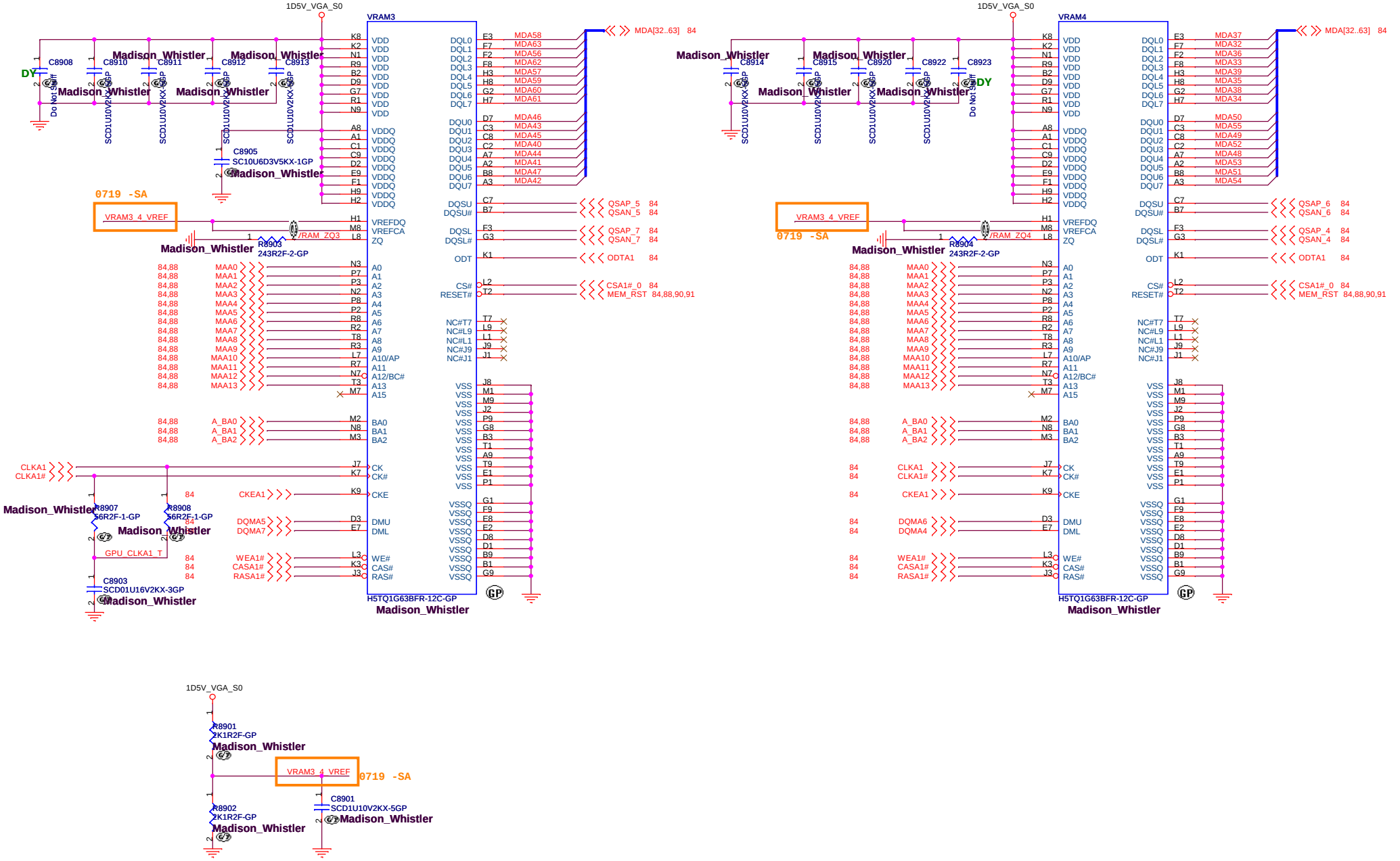
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
A3	JE40-SB	SB

Date: Monday, March 28, 2011 Sheet 88 of 102



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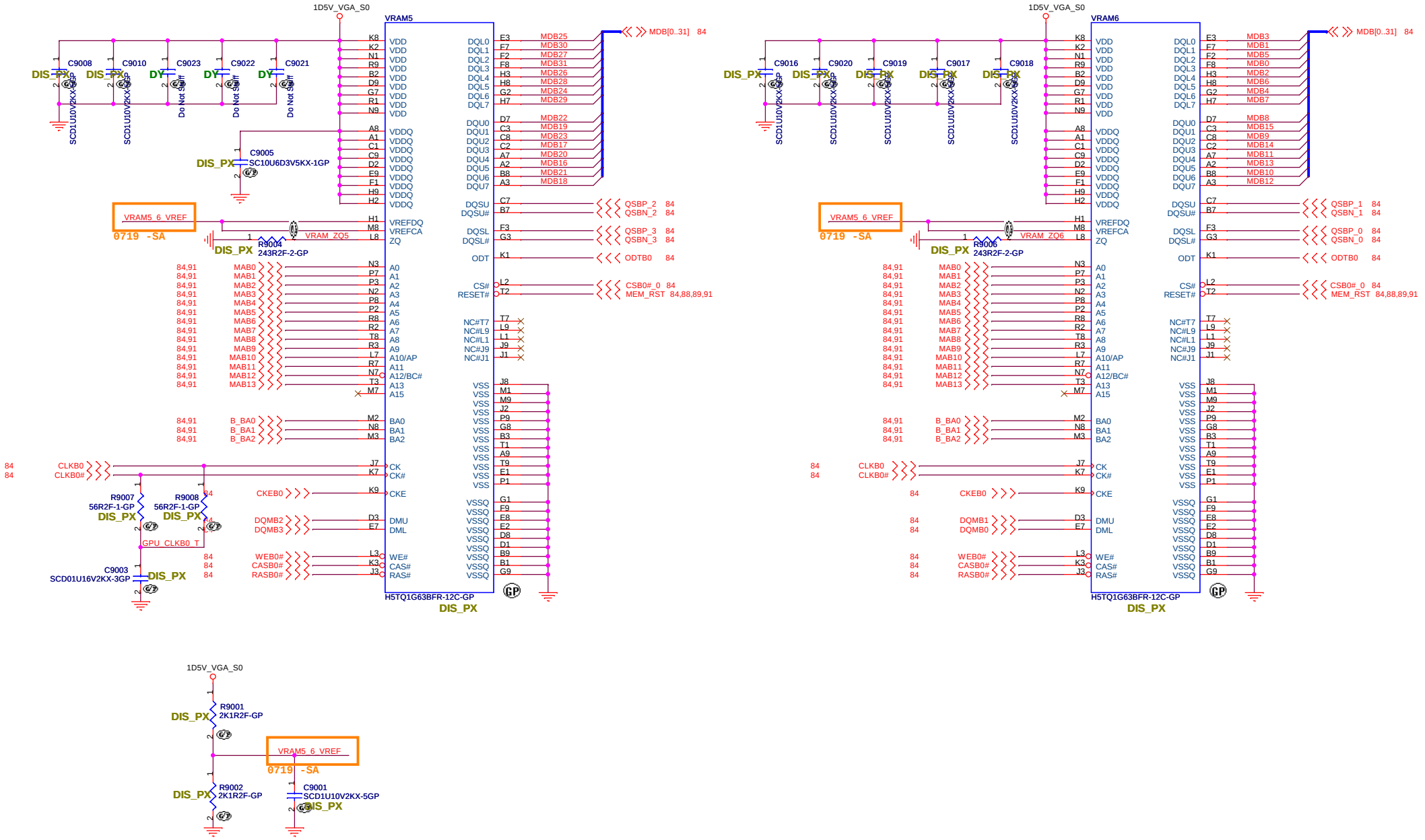
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM3,4 (2/4)***	
Size A3	Document Number **JE40-SB**	Rev **SB**
Date: Monday, March 28, 2011	Sheet 89 of 102	



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM5,6 (3/4)***
Size A3	Document Number **JE40-SB** Rev **SB**
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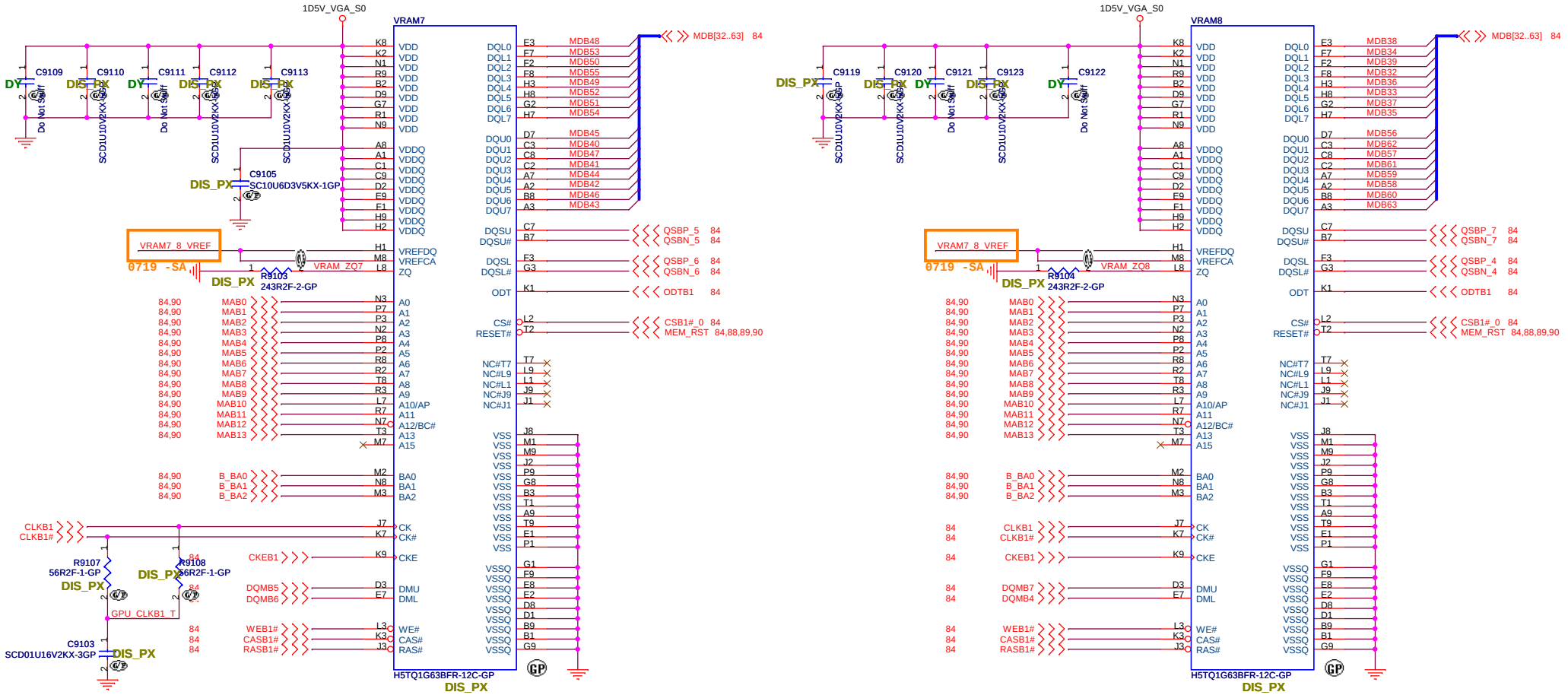

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	JE40-SB	SB

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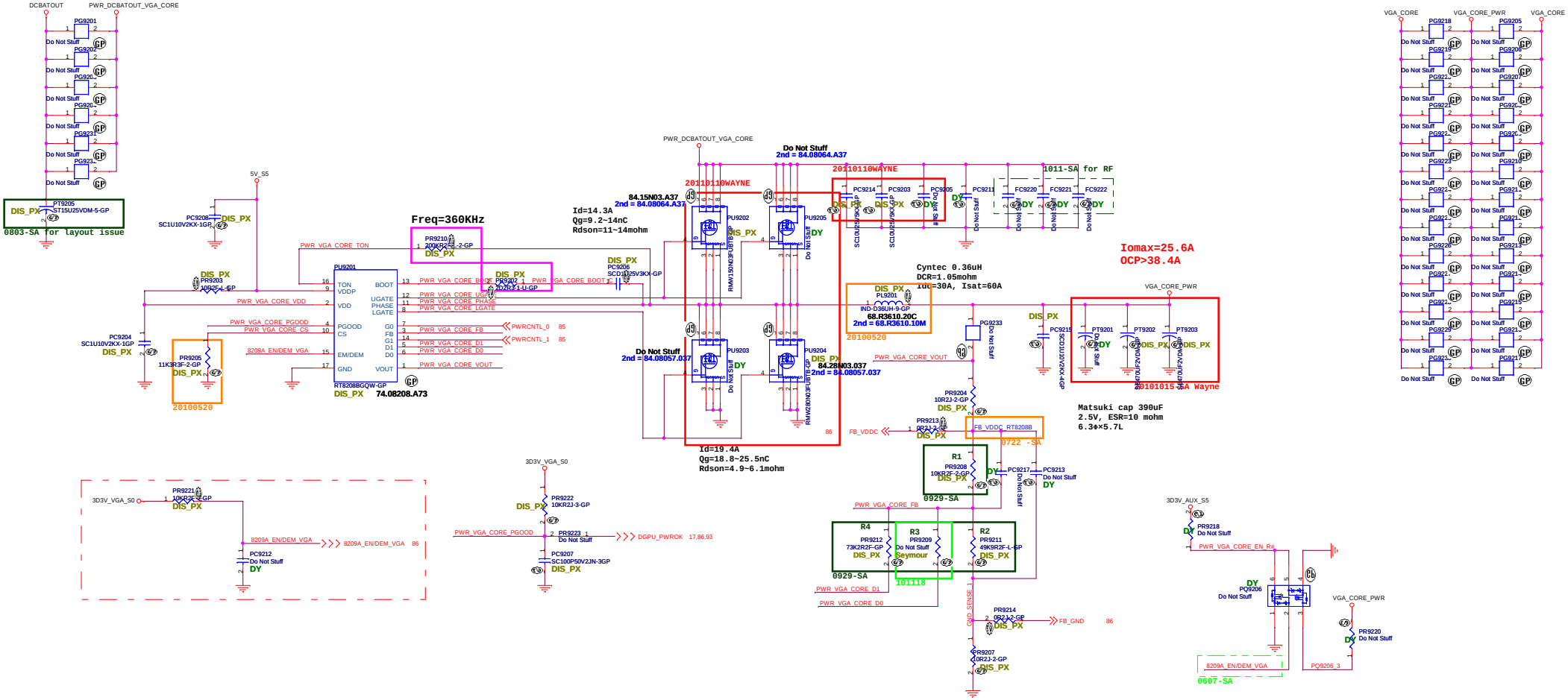

PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Whistler Pro	
H	L	High	1V	Vout = 0.75V * [1+R1/(R2//R4)]
H	L	Medium	1V	
H	H	Low	0.9V	Vout = 0.75V * (1+R1//R2)

PWR_VGA_CORE_D0	PWR_VGA_CORE_D1	Level	Seymour XT	
L	L	High	1.1V	Vout = 0.75V * [1+R1/(R2//R3//R4)]
L	H			
H	L	Medium	1V	Vout = 0.75V * [1+R1/(R2//R4)]
H	H	Low	0.9V	Vout = 0.75V * (1+R1//R2)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size	Document Number	Rev
A2	JE40-SB	SB

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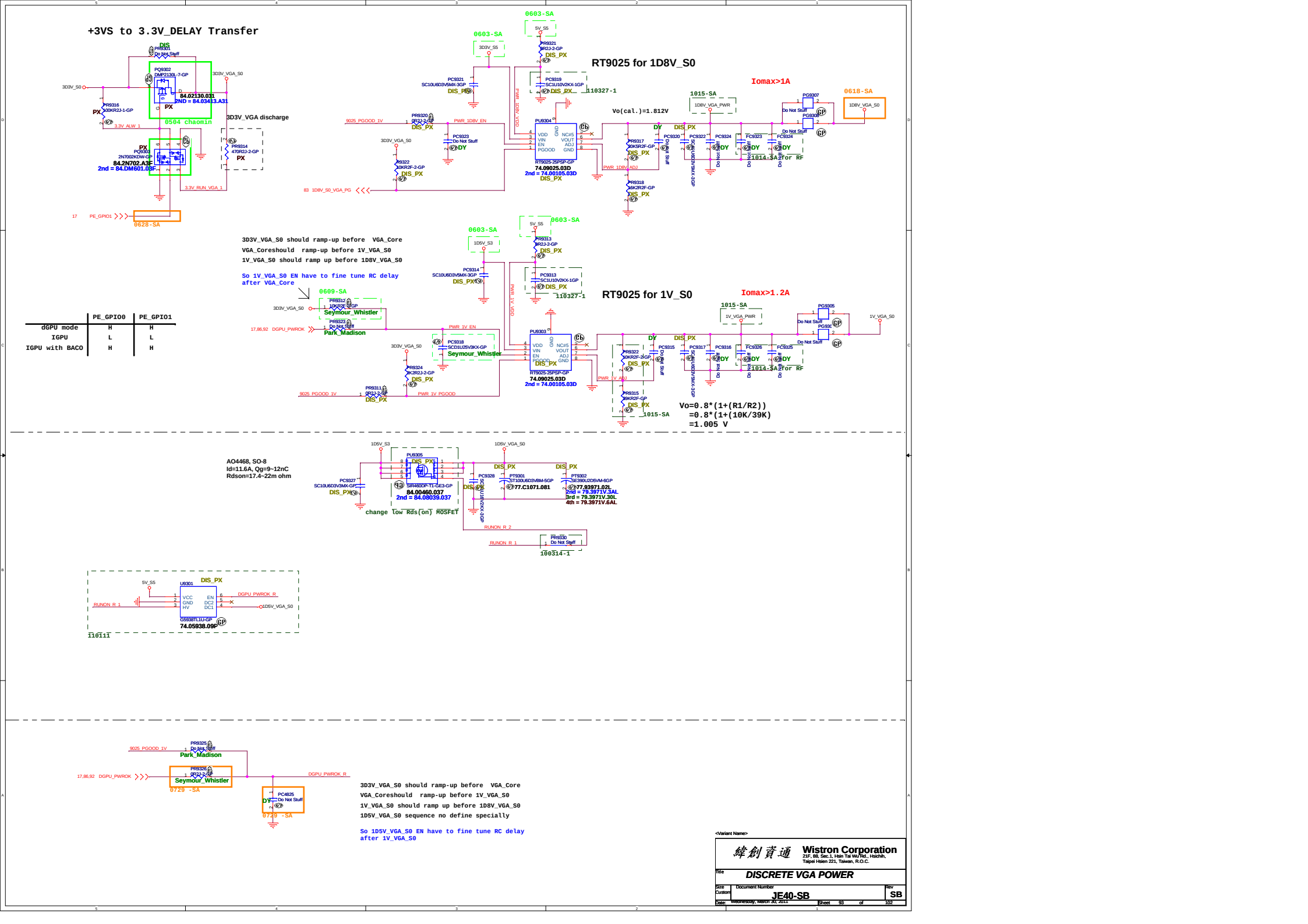
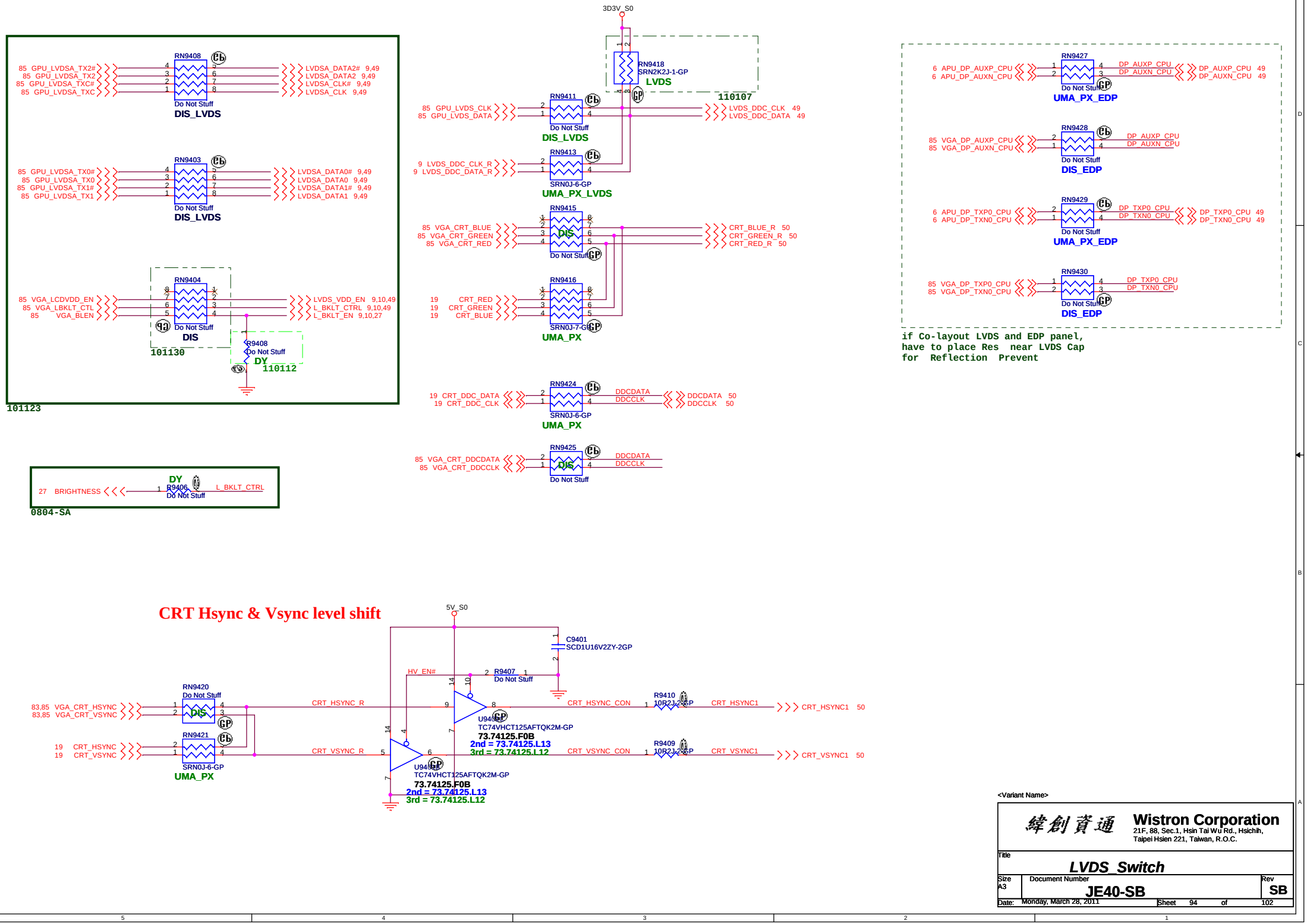

+3VS to 3.3V_DELAY Transfer
3D3V_VGA discharge
0504 chaomin
0628-SA
RT9025 for 1D8V_S0
Iomax>1A
Vo(cal.)=1.812V
1014-SA for RF
0618-SA
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Coreshould ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
So 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core
Seymour_Whistler
Park_Madison
RT9025 for 1V_S0
Iomax>1.2A
Vo=0.8*(1+(R1/R2))
=0.8*(1+(10K/39K))
=1.005 V
dGPU mode H H
IGPU L L
IGPU with BACO H H
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm
change low Rds(on) MOSFET
110111
0729 -SA
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Coreshould ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0
1D5V_VGA_S0 sequence no define specially
So 1D5V_VGA_S0 EN have to fine tune RC delay after 1V_VGA_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DISCRETE VGA POWER
JE40-SB
SB



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size	Document Number	Rev
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Date: Monday, March 28, 2011 Sheet 94 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch Panel*

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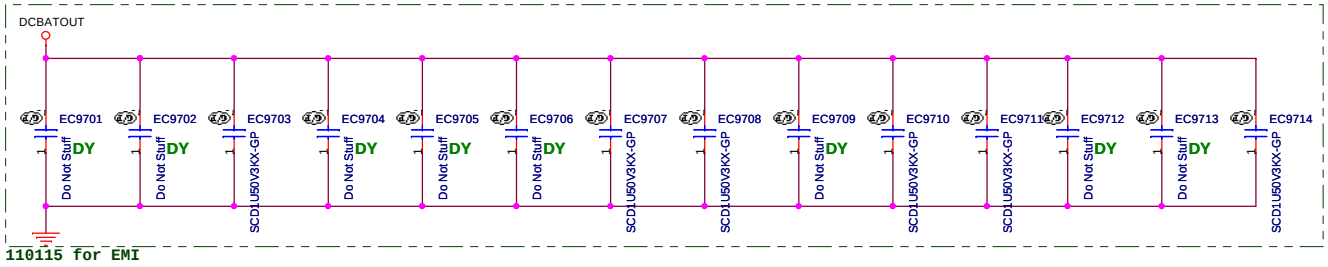
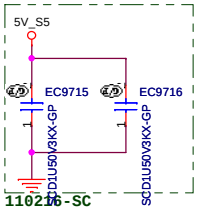
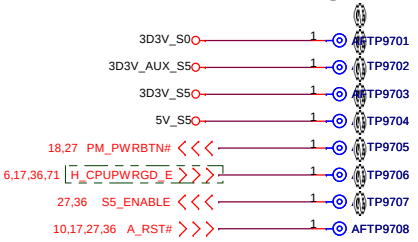
EMI CAP

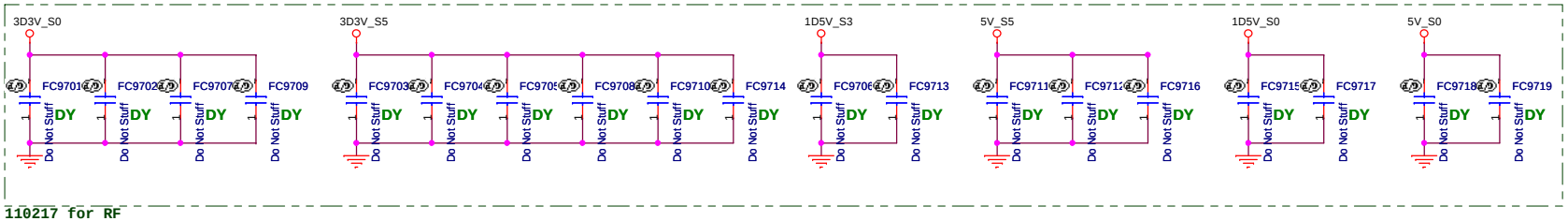




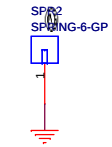
Check test point



Test Point放在Dimm Door打開可量測處

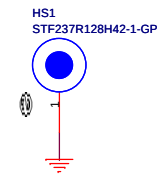


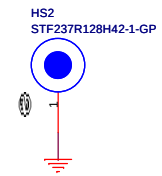
SPRING

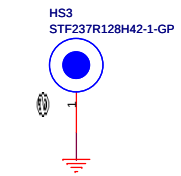


BOSS

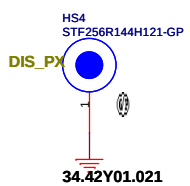
CPU

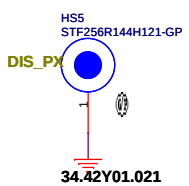




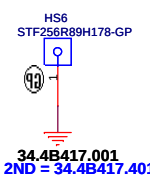


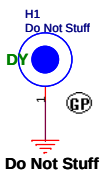
VGA

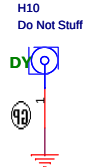


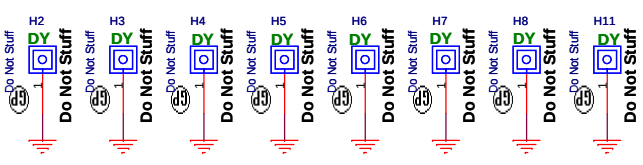


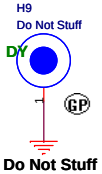
WLAN











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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/CAP

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Modify list

65 W: PR4007 -> 187K(64.18735.6DL)
90 W: PR4007 -> 121K (64.12135.6DL)

UMA and PX R5114 ~ R5121   -> 604-ohm (64.60405.6DL)
Diserete -> R5114 ~ R5121-> 499-ohm(64.49905.6DL)

R8332 stuff 1K   for Mannhatton VGA
      stuff 5.1K(64.51015.6DL) for Vancouver VGA

if use LVDS L8711,L8709 stuff 0-ohm 0603
if use LVDS L8701,L8708 stuff bead 0603

if use EDP L8711,L8709 stuff bead 0603 ohm
if use EDP L8701,L8708 stuff 0-ohm 0603

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

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POWER SEQUENCE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER SEQUENCE***

Size	Document Number	Rev
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<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

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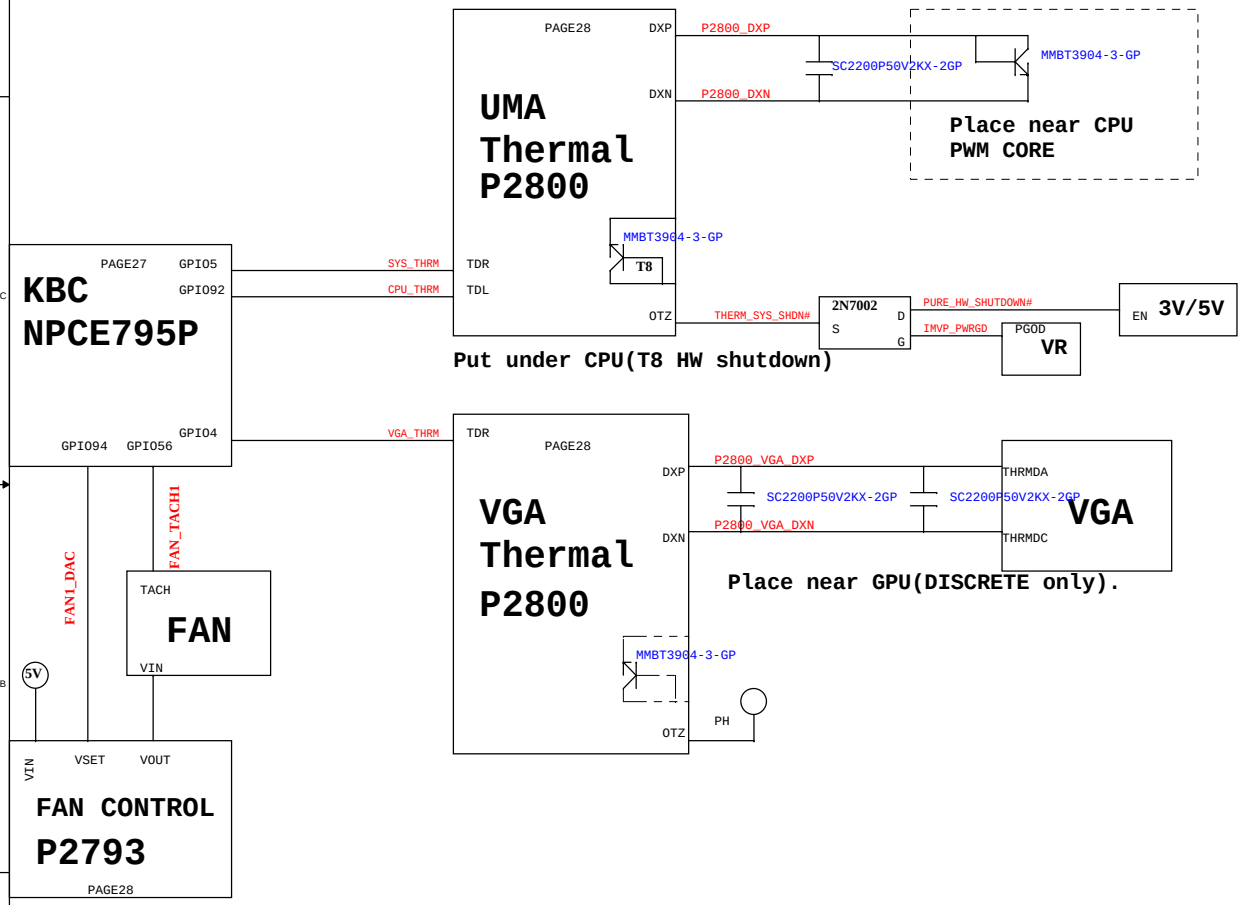
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***SMBUS BLOCK DIAGRAM***
Size: A2	Document Number: **JE40-SB** Rev: **SB**
Date: Friday, March 25, 2011	Sheet 101 of 102

Thermal Block Diagram



Audio Block Diagram

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size: Custom	Document Number: JE40-SB	Rev: SB
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