Loveland BDW Schematics
Broadwell-ULT

2015-05-11

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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Title	*Cover Page*	
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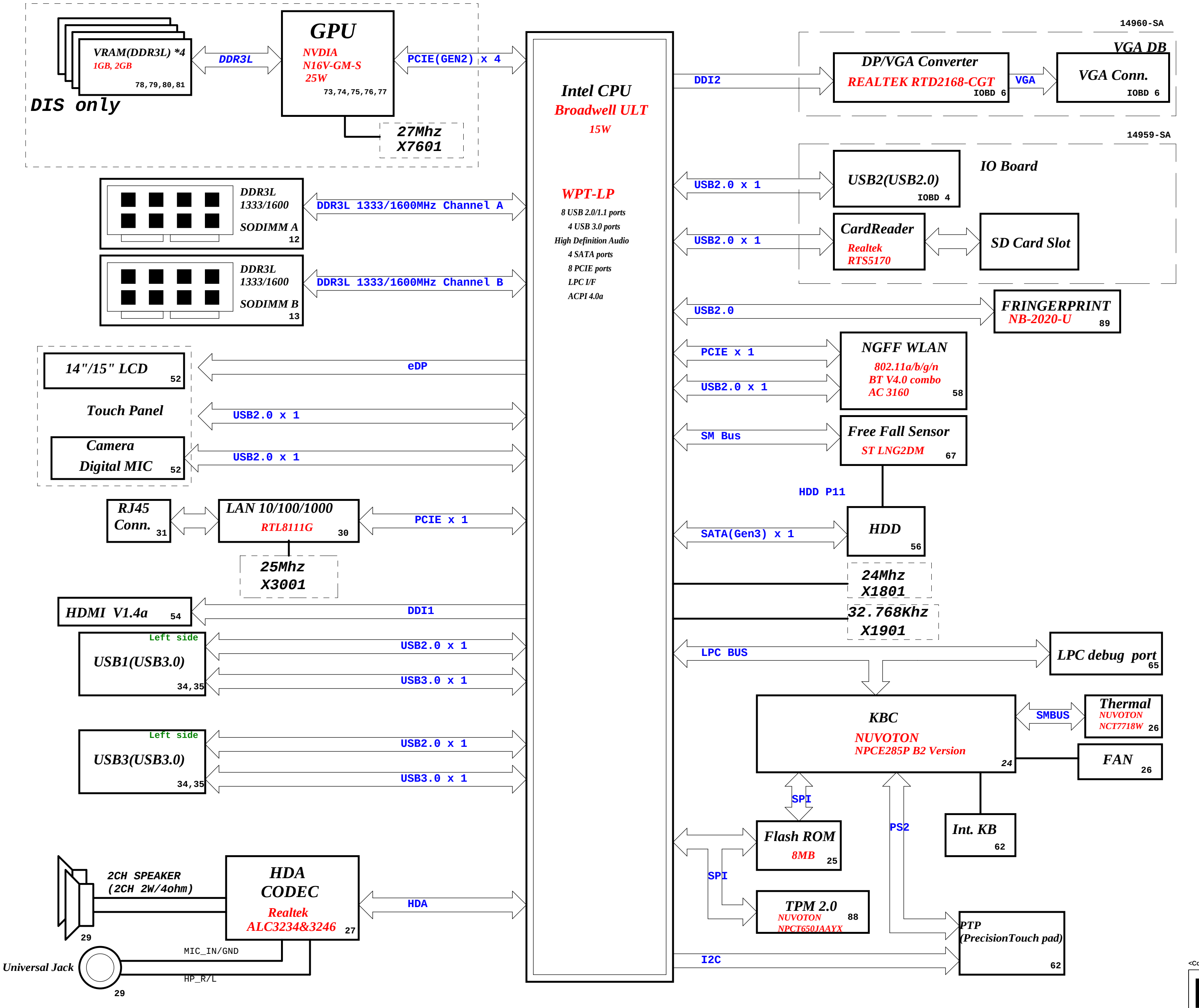
Project code:
Love14 BDW --> 4PD057010001
Love15 BDW --> 4PD059010001
PCB P/N: 14290-SC
Revision: X00

Loveland BDW Block Diagram



CHARGER
BQ24780RUYR-1-GP 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC
TPS51225RUKR-GP 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power
TPS51624RSMR-GP-U 46,47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

DDR3L SUS
TPS51716RUKR-GP 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

CPU 1.05V
RT8237CZQW-2-GP 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU 1D5V_S0
TLV70215DBVR-GP 51

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

Switches
36 83

INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D05V_S0	1D05V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
	1D8V_S0

PCB LAYER

L1:Top
L2:VCC/GND
L3:Signal
L4:Signal
L5:GND
L6:Signal

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Title: Block Diagram

Size: A2 | Document Number: Loveland BDW | Rev: A00

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Title	***(Reserved)***
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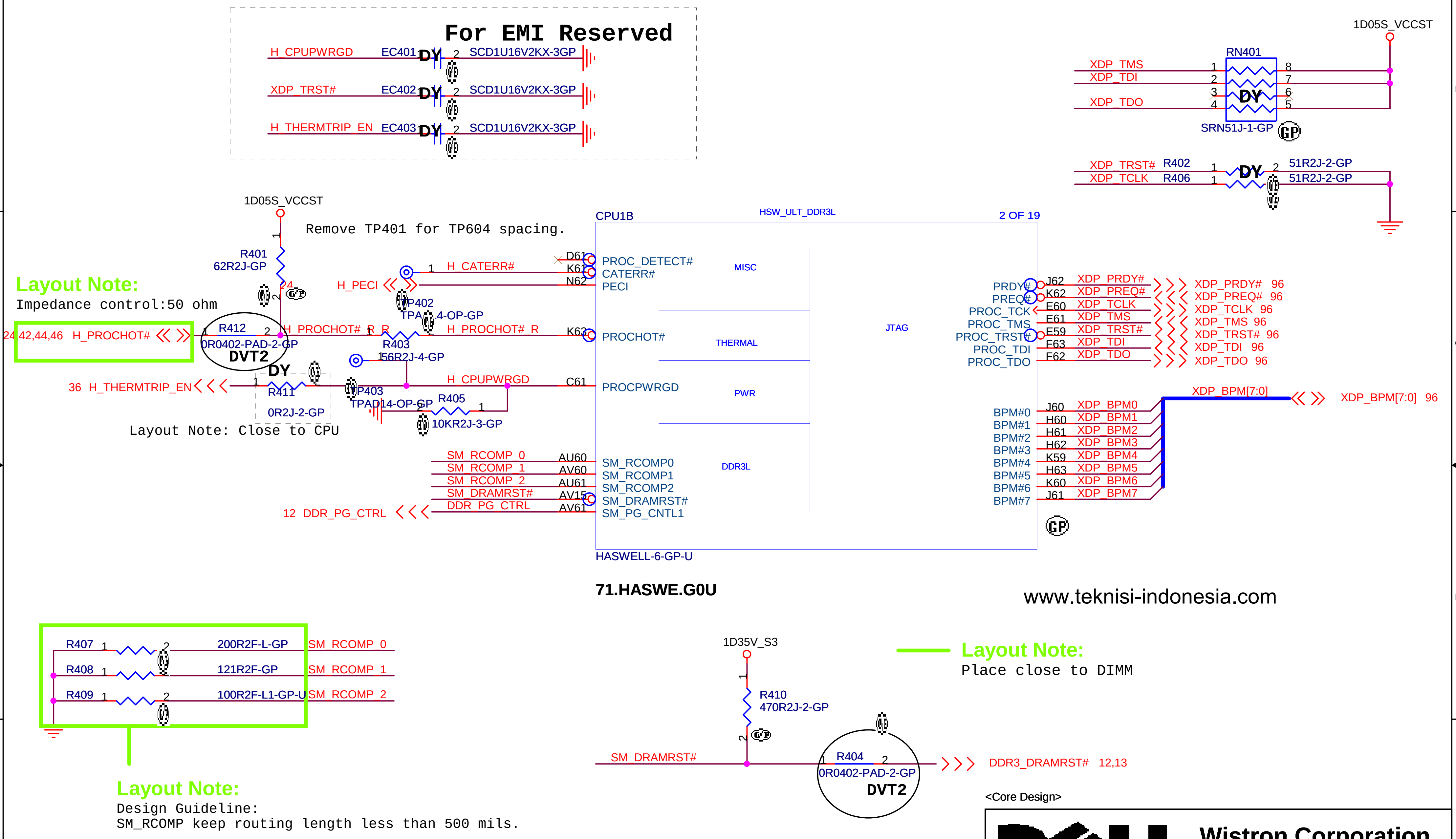
Main Func = CPU



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Title	*CPU (THERMAL/MISC/PM)*	
Size A4	Document Number *Loveland BDW*	Rev *A00*
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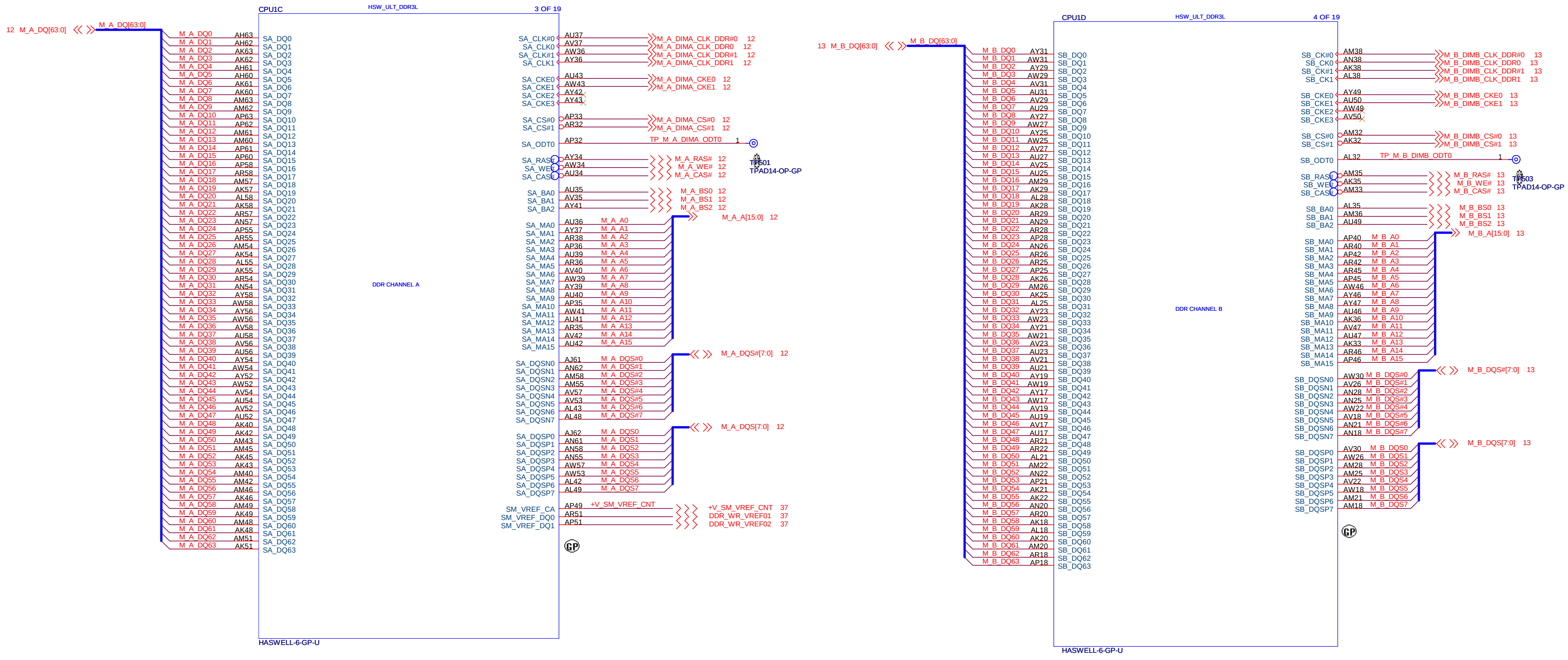
Main Func = CPU

DDR3L ball type: Non-Interleaved Type



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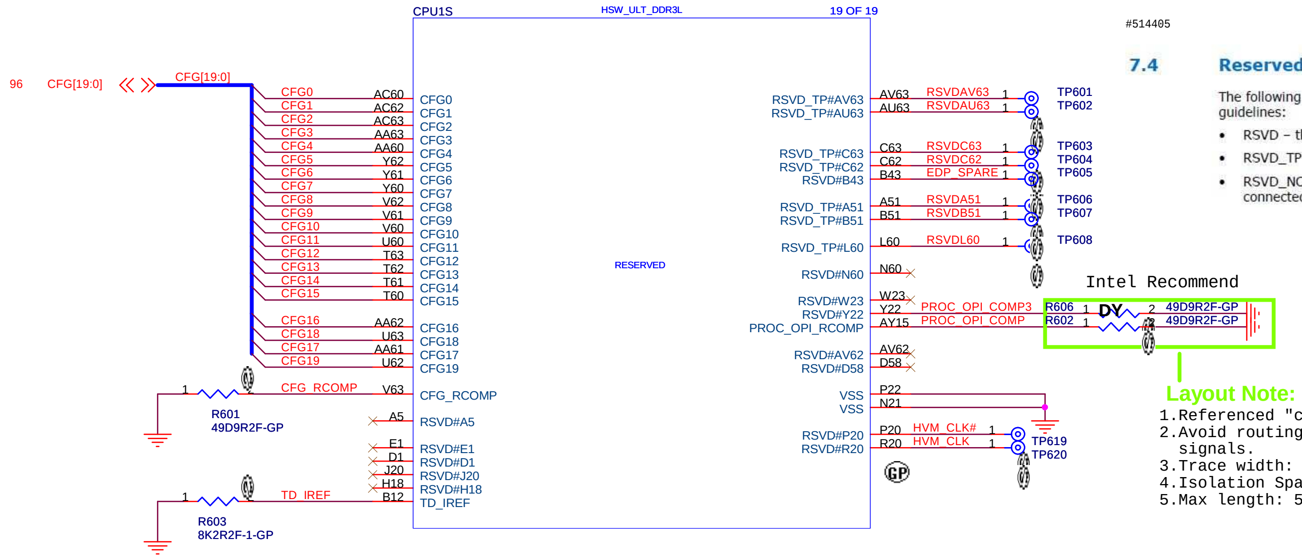
Title	CPU (DDR)	
Size: Custom	Document Number: Loveland BDW	Rev: X02
Date: Tuesday, May 12, 2015	Sheet 5 of 102	

Main Func = CPU



#514405

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

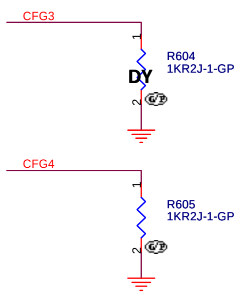
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 **PCH strap pin:**

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. • **CFG[2:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[3]: MSR Privacy Bit Feature** — 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting — 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **CFG[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)
Size: A3 | Document Number: Loveland BDW | Rev: A00
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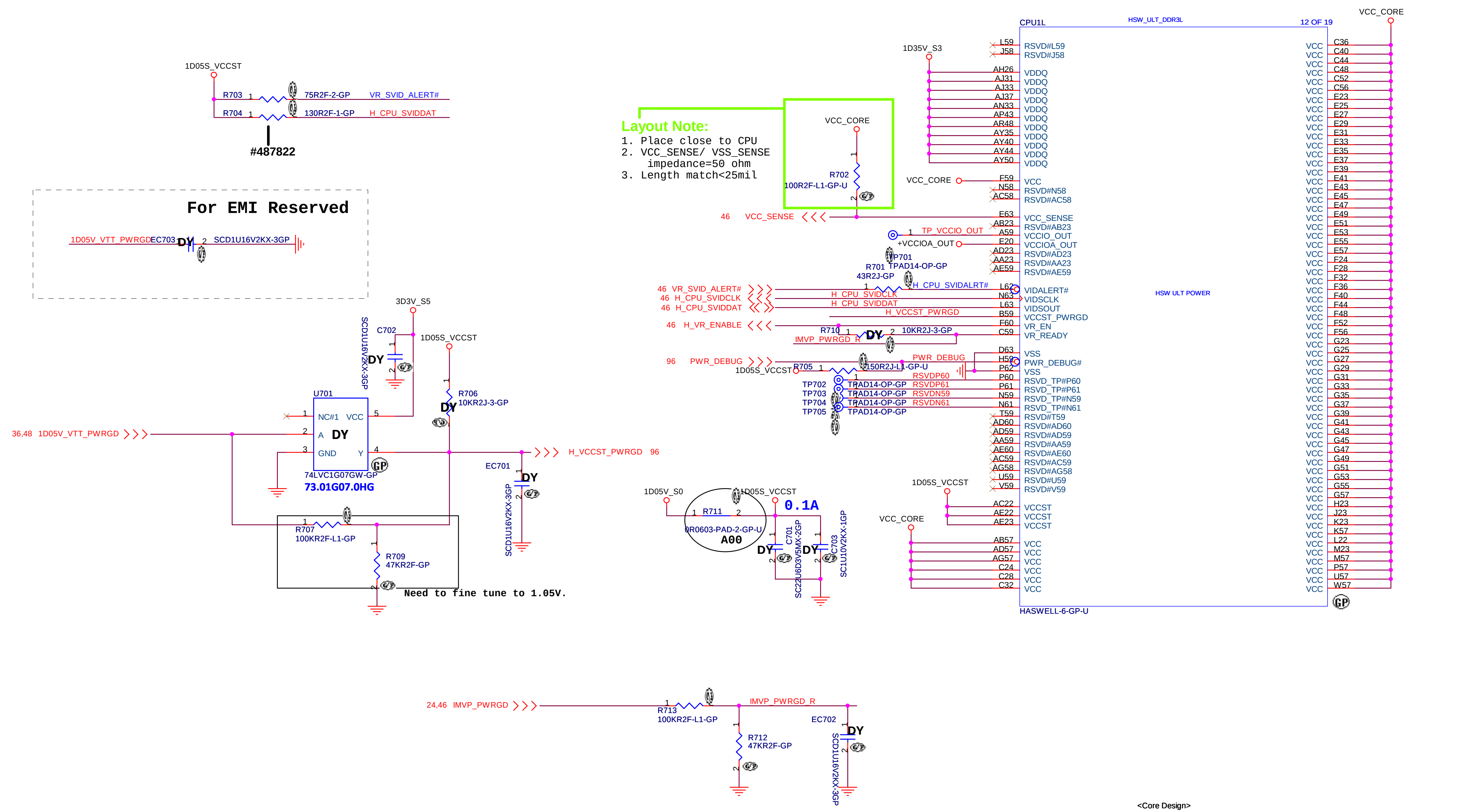
Main Func = CPU



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Title	CPU (VCC CORE)	
Size A3	Document Number Loveland BDW	Rev X02
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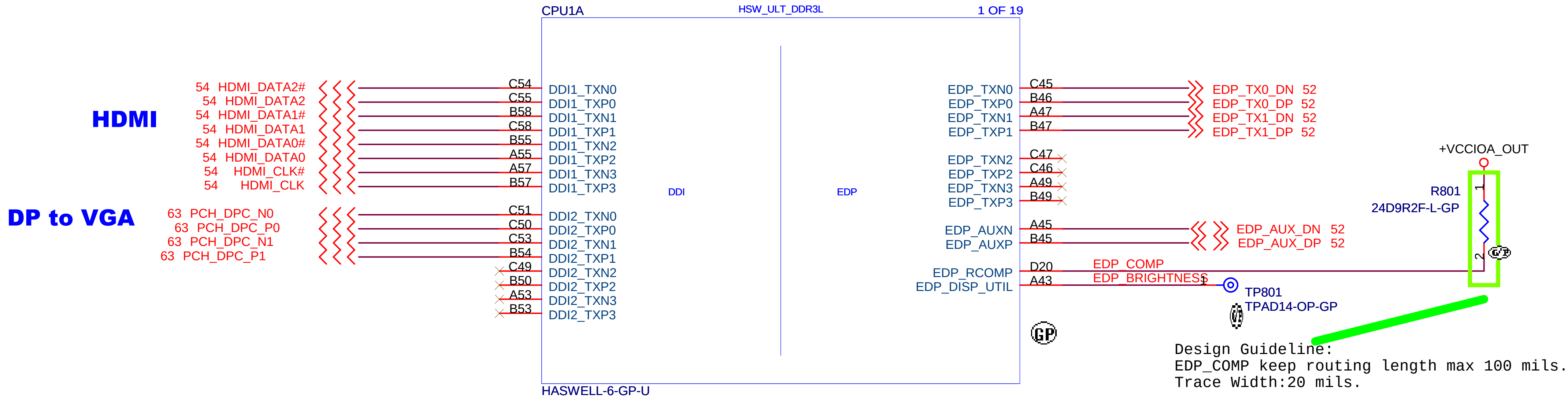
Main Func = CPU



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Title		
CPU (DDI/EDP)		
Size: A4	Document Number: Loveland BDW	Rev: A00
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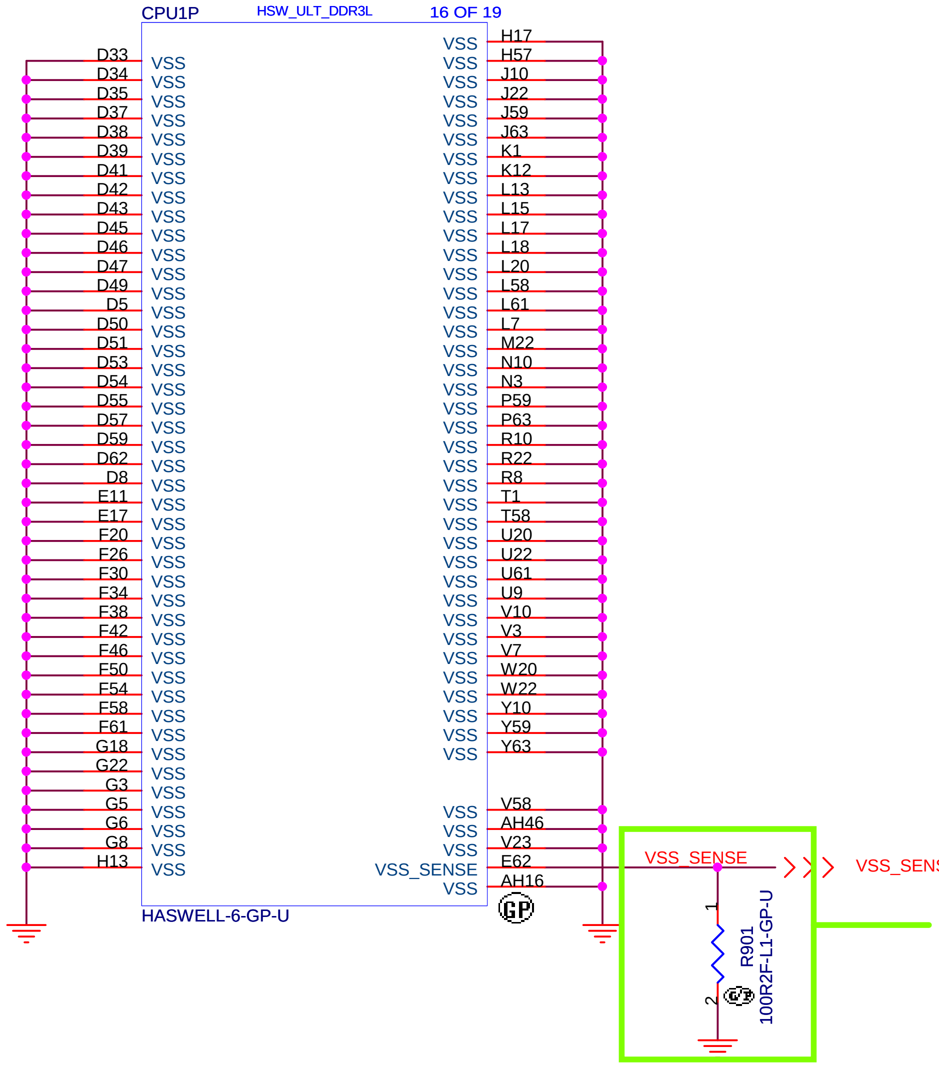
Main Func = CPU



Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

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Title	CPU (VSS)	
Size A4	Document Number: Loveland BDW	Rev A00
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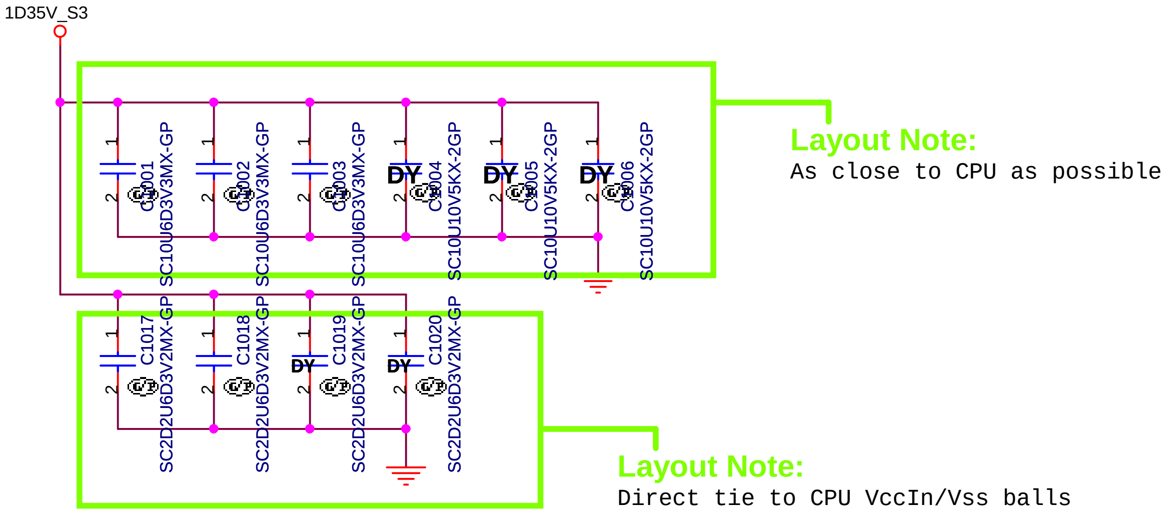
Main Func = CPU



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Title	CPU (Power CAP1)	
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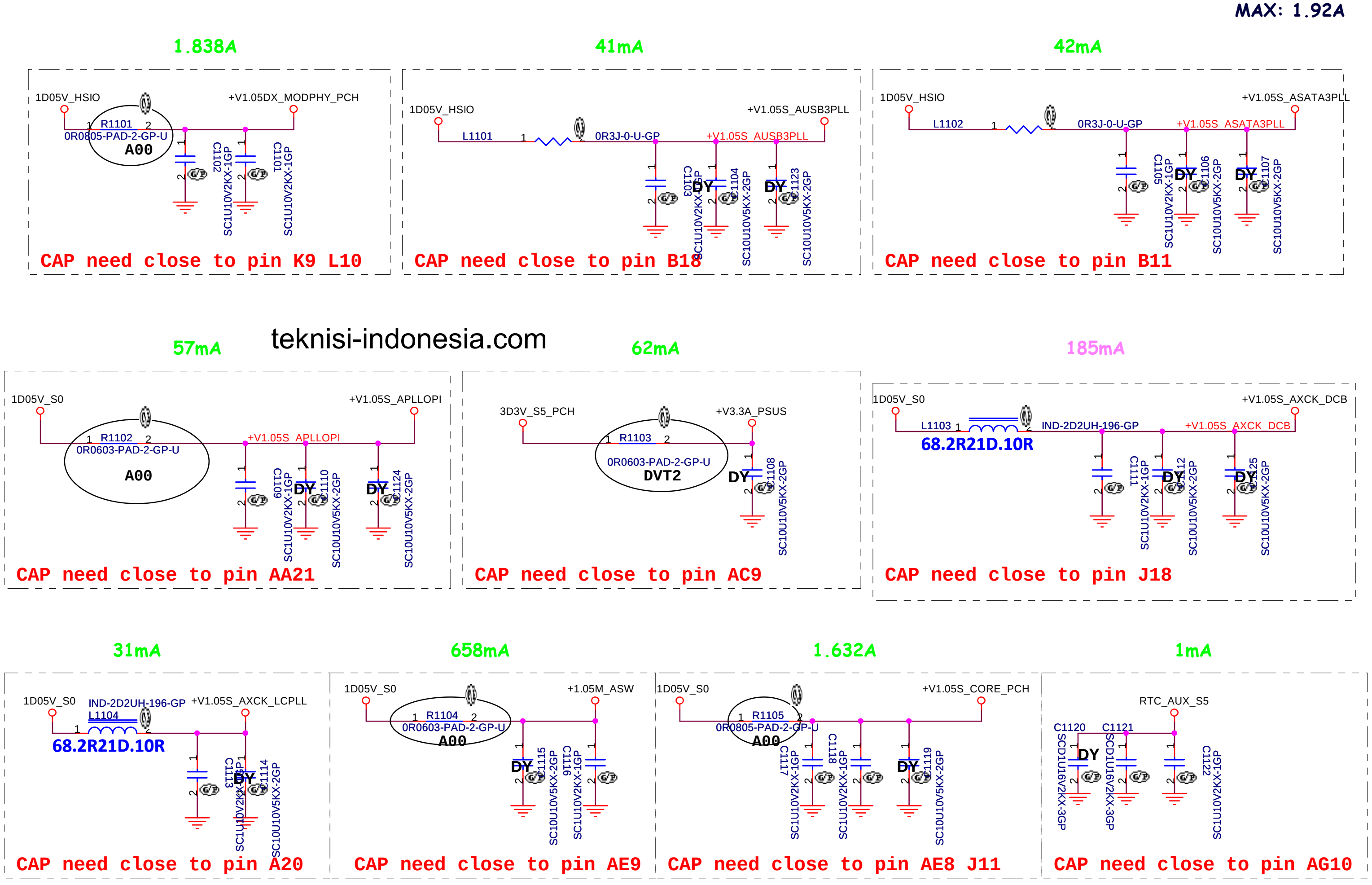
Main Func = CPU



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Title			
CPU (Power CAP2)			
Size: A3	Document Number: Loveland BDW		Rev: A00
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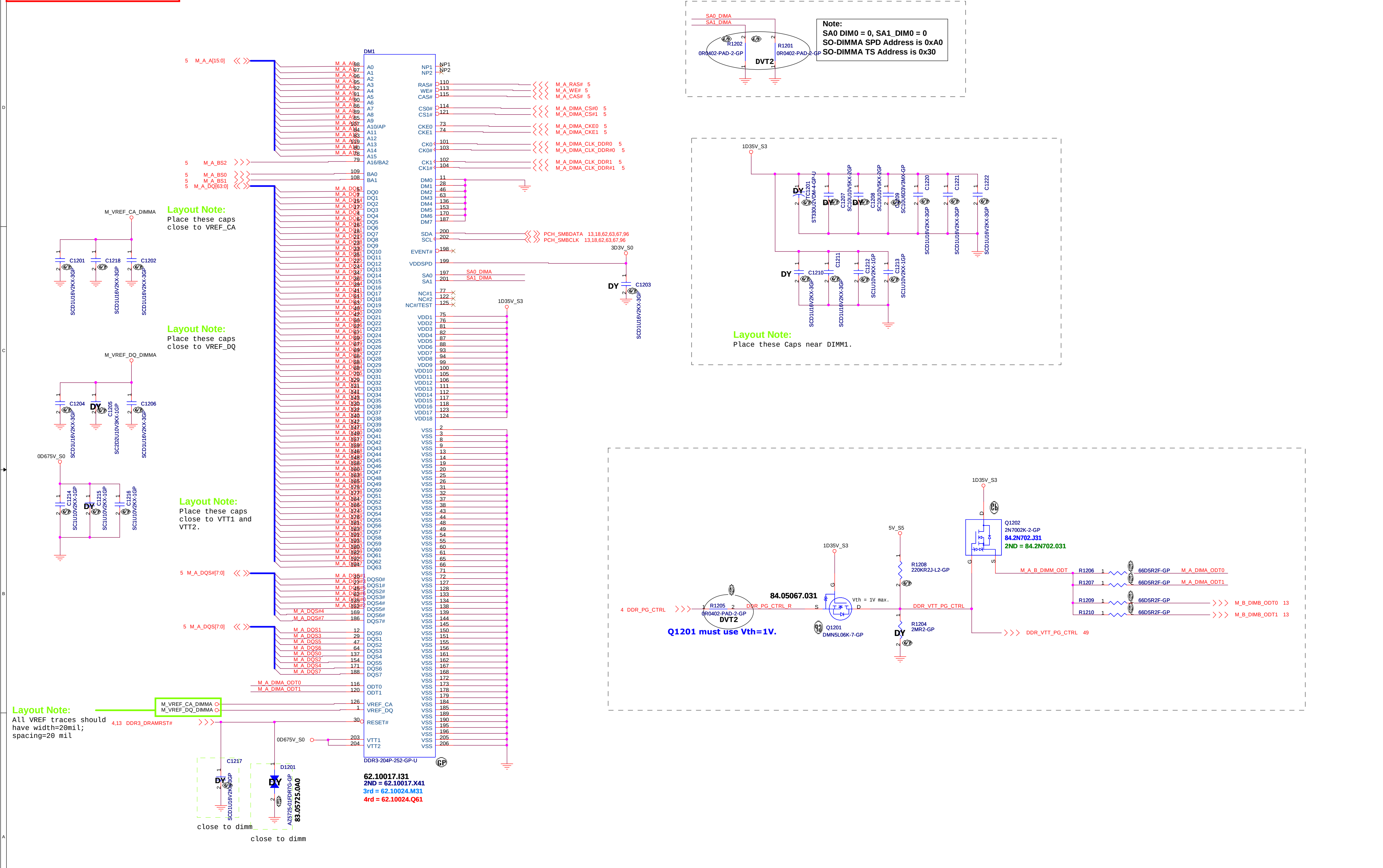
Main Func = DIMM1



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Title	DDR3L_SODIMM1	
Size A2	Document Number: Loveland BDW	Rev A00
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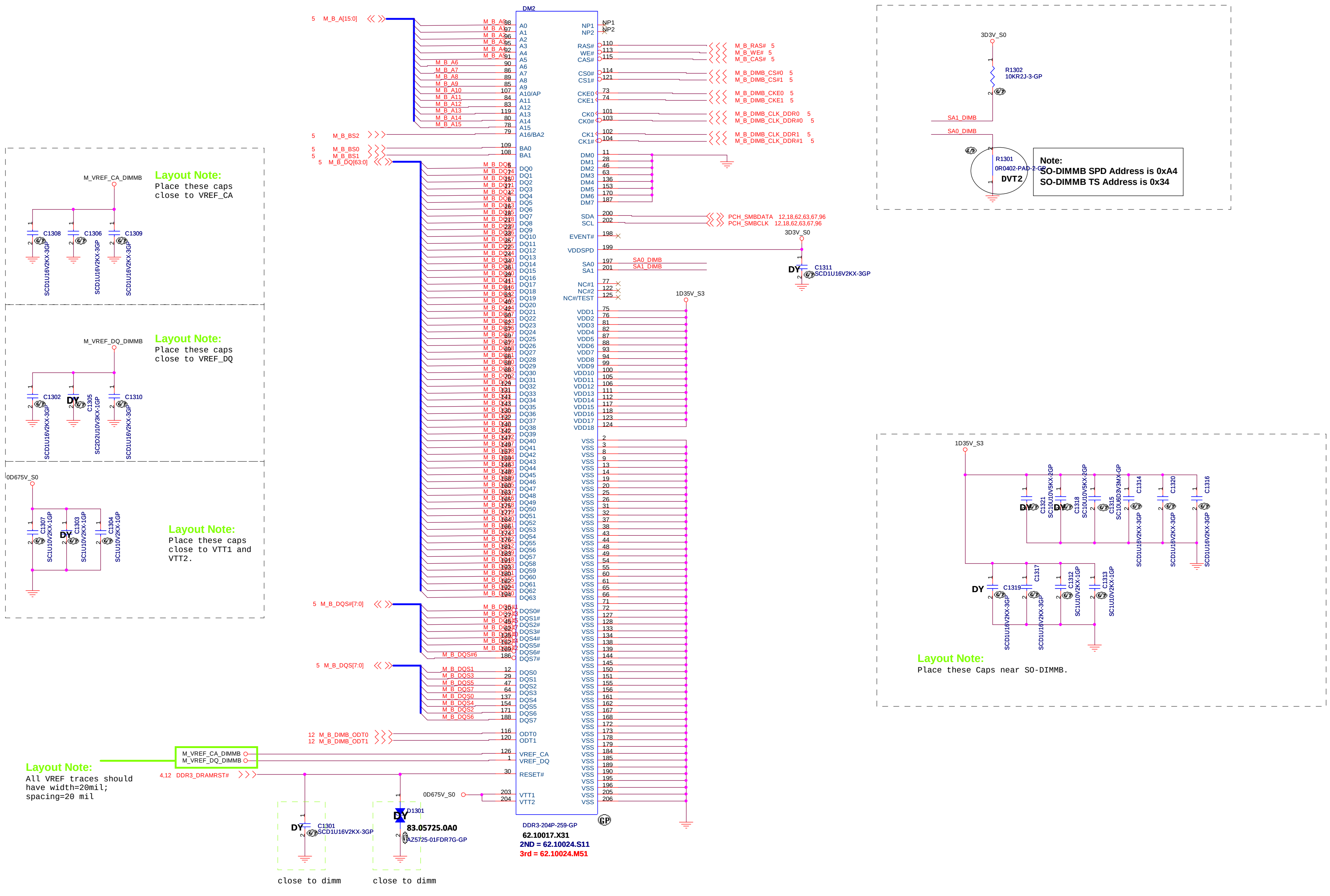
Main Func = DIMM2



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Title	DDR3L_SODIMM2	
Size A2	Document Number: Loveland BDW	Rev A00
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5 4 3 2 1

D D

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C C

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B B

A A

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Title	*(Reserved)_SODIMM _SODIMM4*	
Size A4	Document Number *Loveland BDW*	Rev *A00*
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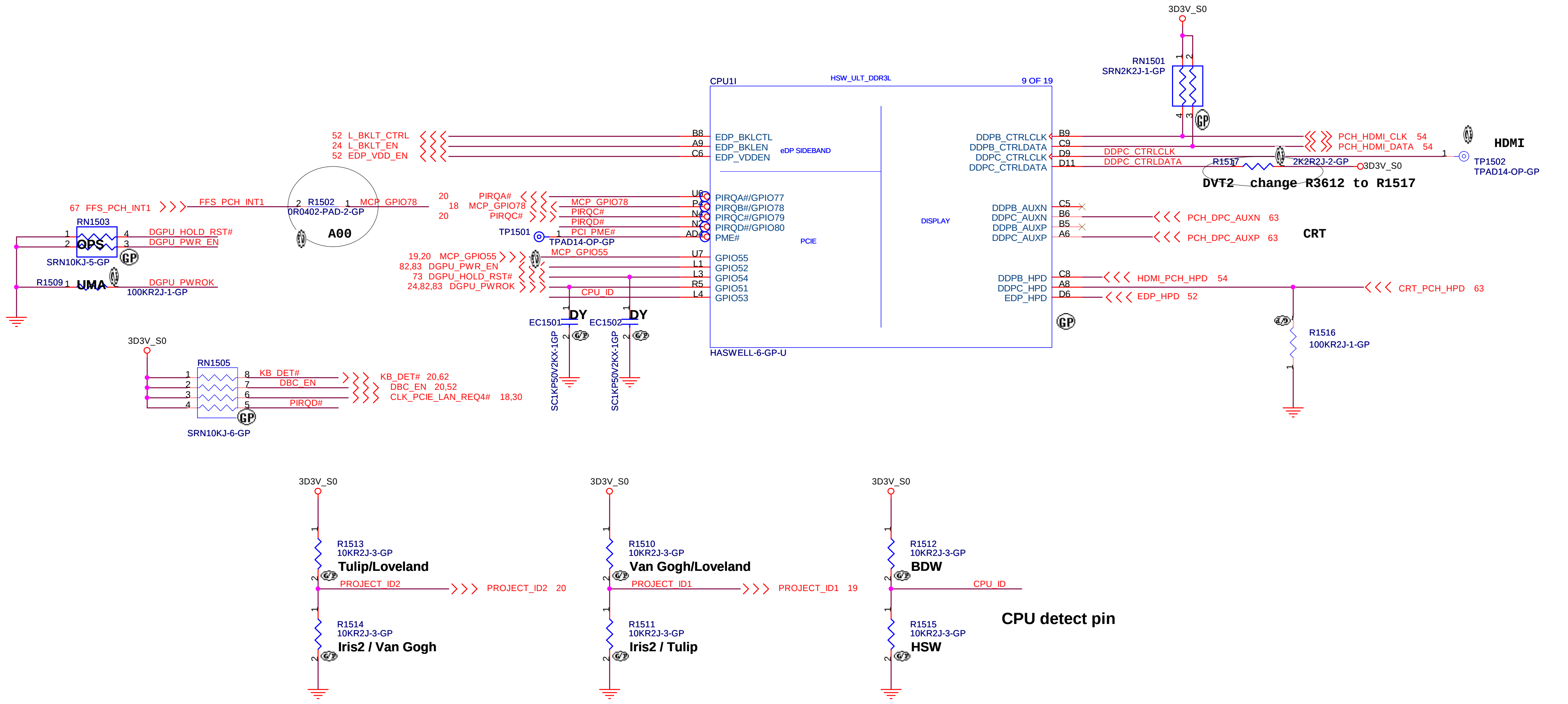
5 4 3 2 1

Main Func = PCH

PCH strap pin:

Port B Detected	
DDPB_CTRLDATA	* Low = Disable Port B (default) High = Enable Port B
DDPC_CTRLDATA	* Low = Disable Port C (default) High = Enable Port C

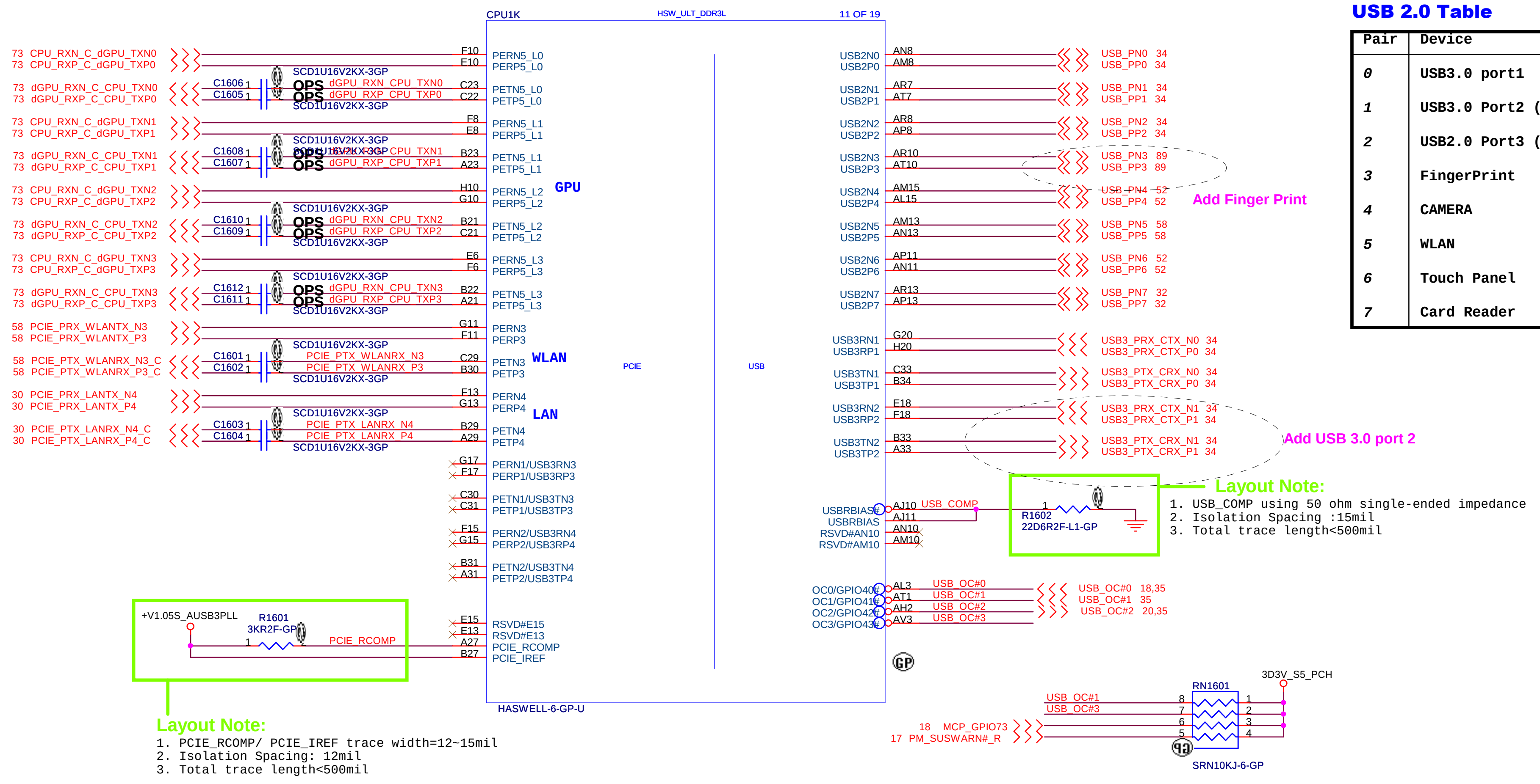
The internal pull-down is disabled after PLTRST# deasserts



BIOS strap pin:

BIOS VRAM Size Strap pin	PROJECT_ID2 (GPIO38)	PROJECT_ID1 (GPIO37)
Iris2	0	0
Van Gogh	0	1
Tulip	1	0
Loveland	1	1

Main Func = PCH



Layout Note:
1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB2.0 Port3 (IOBD)
3	FingerPrint
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	N/A	
6(L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port5 Lane 2 GPU	PCIe* Port5 Lane 3 GPU	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD							PCIe* Port6 Lane 0 SSD	PCIe* Port6 Lane 1 SSD	PCIe* Port6 Lane 2	PCIe* Port6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port3	USB 3.0 Port4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD GPU	PCIe* Port 5 Lane 1 SSD GPU	PCIe* Port5 Lane 2 GPU	PCIe* Port5 Lane 3 GPU	PCIe* Port6 Lane 0 SSD	PCIe* Port6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										

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Title: PCH (PCIE/USB)

Size: A3 | Document Number: Loveland BDW | Rev: A00

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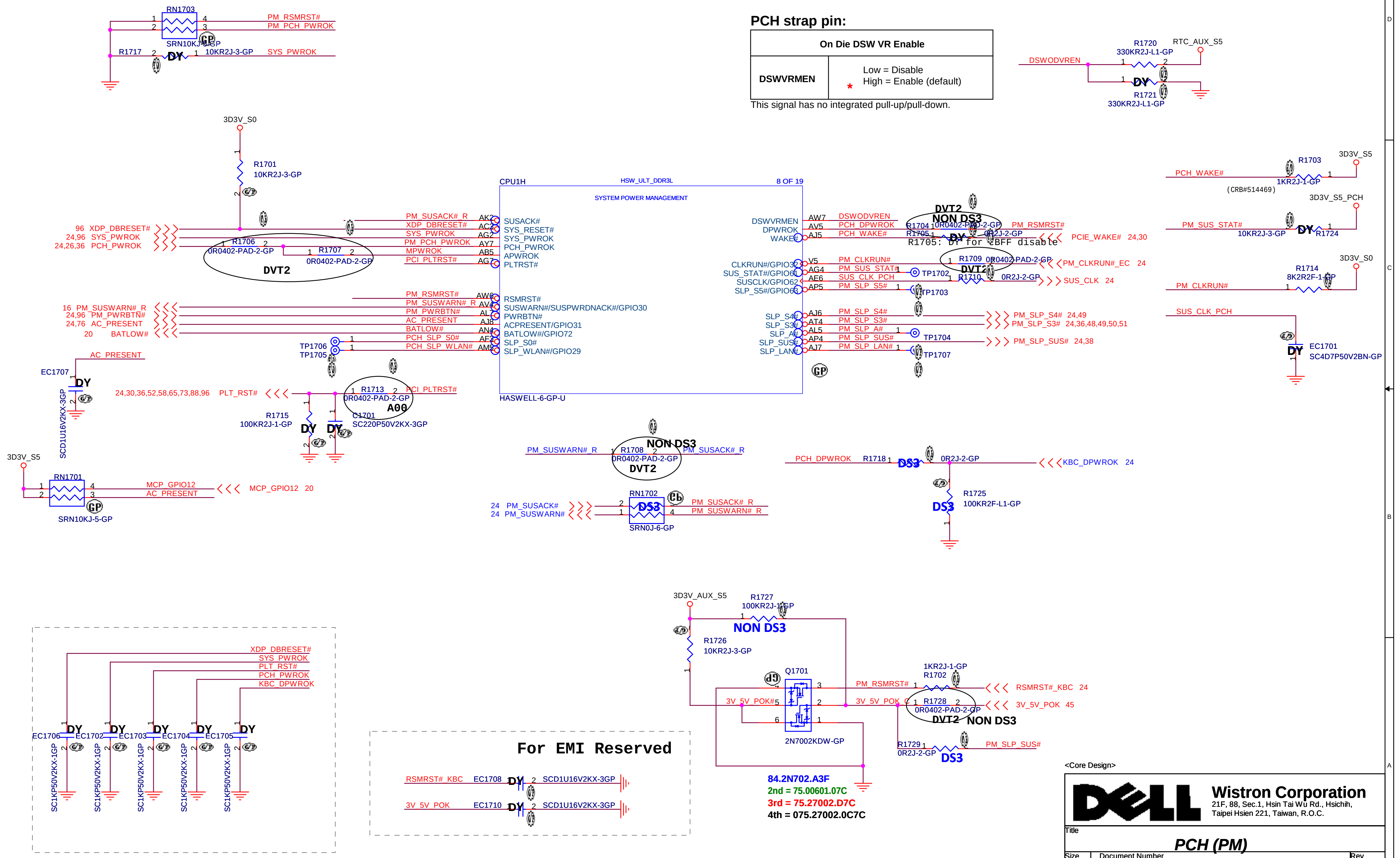
Main Func = PCH

PCH strap pin:

On Die DSW VR Enable	
DSWVRMEN	Low = Disable * High = Enable (default)

This signal has no integrated pull-up/pull-down.



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Title		
PCH (PM)		
Size: A3	Document Number: Loveland BDW	Rev: A00
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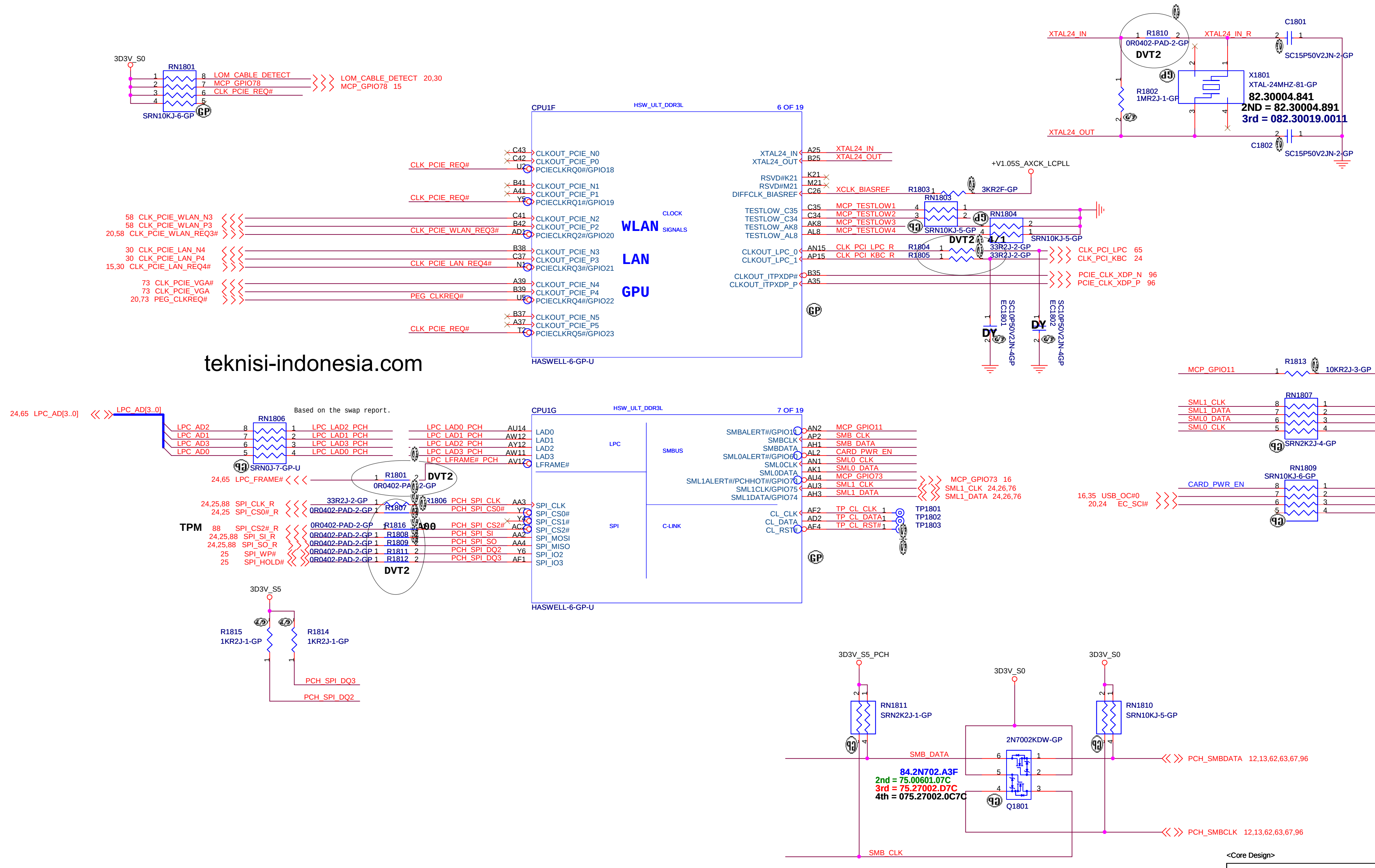
Main Func = PCH



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Title	CPU (PCI-E/SMBUS/CLOCK/CL)
Size	Custom
Document Number	Loveland BDW
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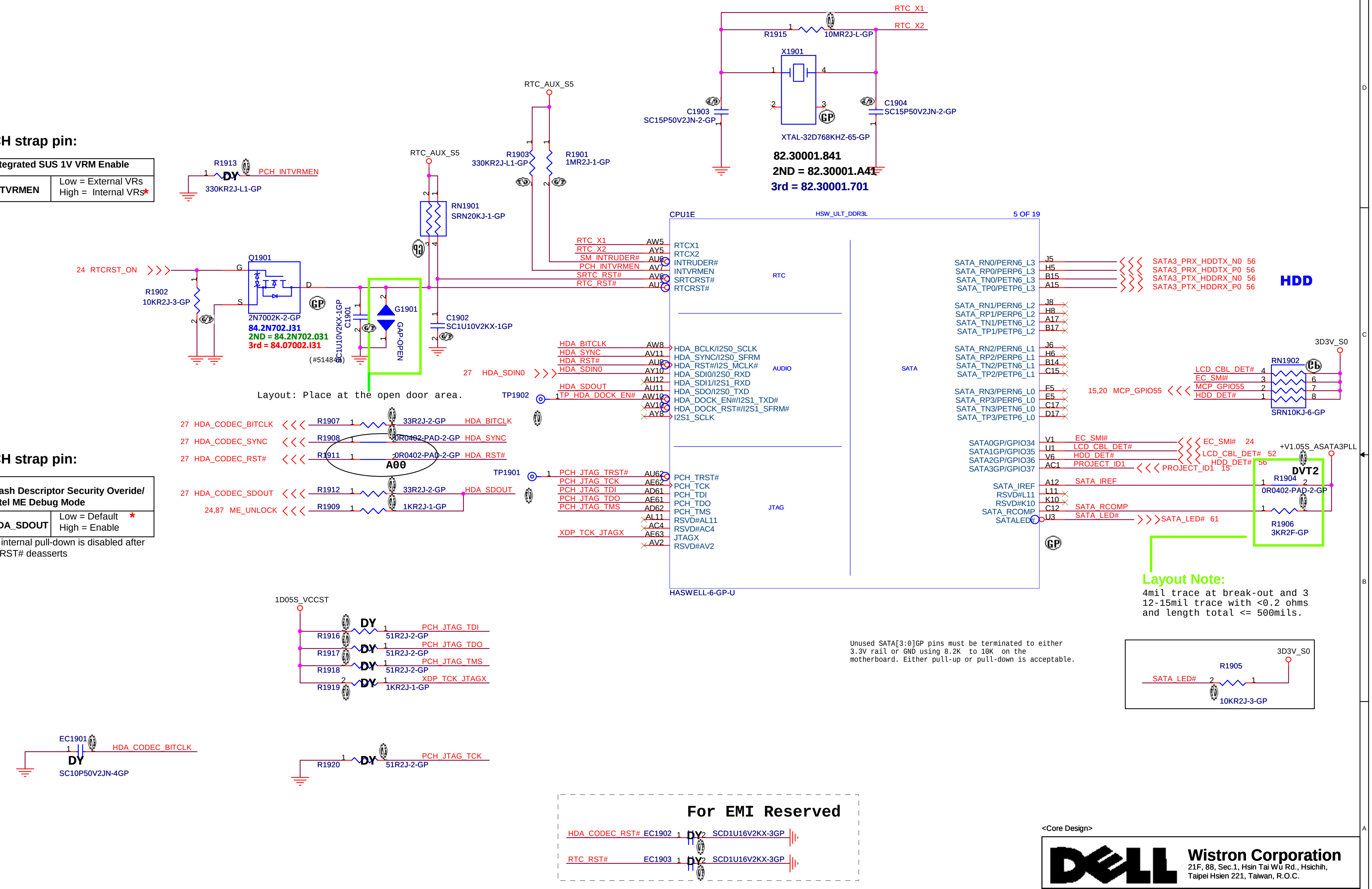
Main Func = PCH



PCH strap pin:

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.

Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2K to 10K on the motherboard. Either pull-up or pull-down is acceptable.

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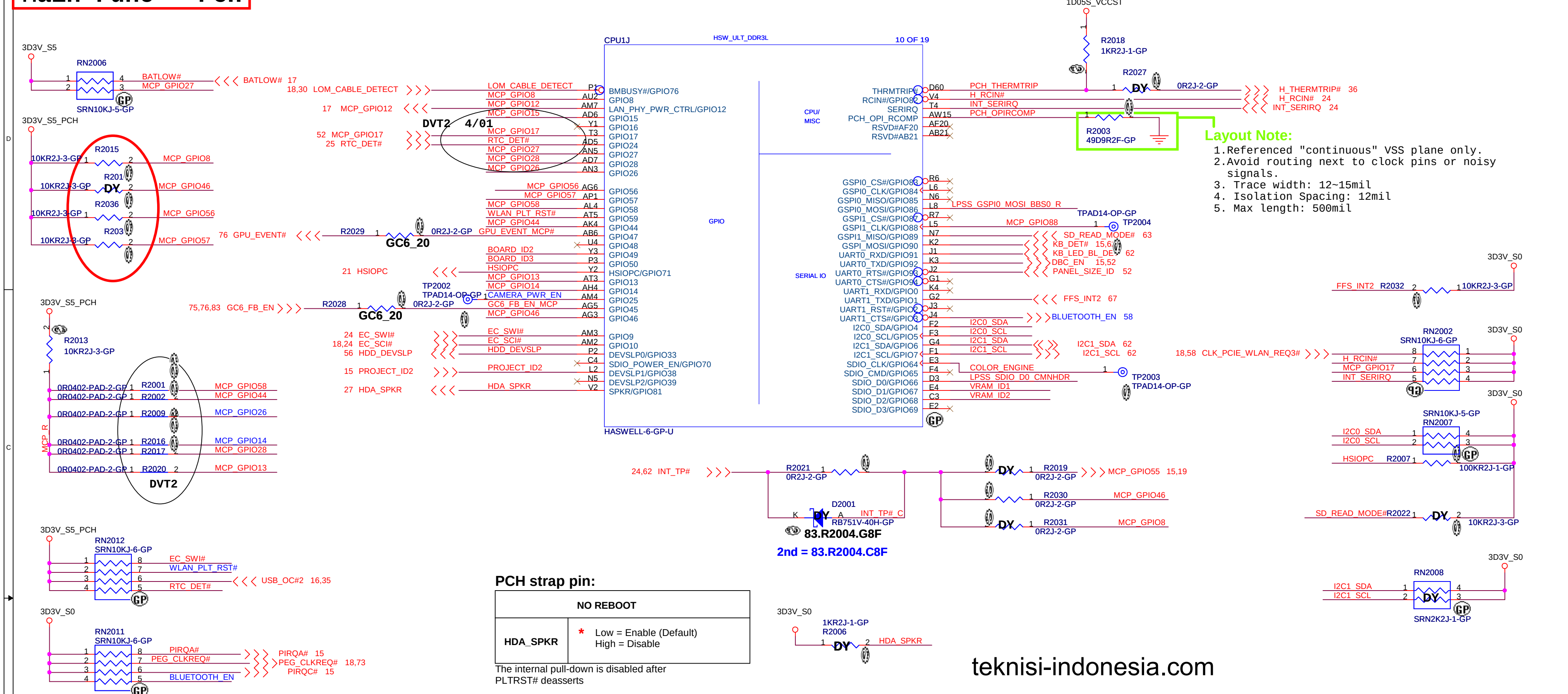
Title	CPU (RTC/SATA/IHDA/JTAG)	
Size A3	Document Number: Loveland BDW	Rev A00
Date: Friday, June 05, 2015	Sheet 19 of 102	

Main Func = PCH



Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

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PCH strap pin:

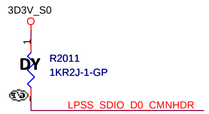
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode * Low = Disable "Top-Block swap" mode (Default)

The internal pull-down is disabled after PLTRST# deasserts

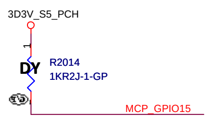


Need SW double confirm if that's needed Top-Block swap

PCH strap pin:

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS (Default) High = Enable Intel ME Crypto TLS

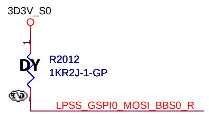
The internal pull-down is disabled after RSMRST# deasserts.



PCH strap pin:

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI (Default) High = LPC

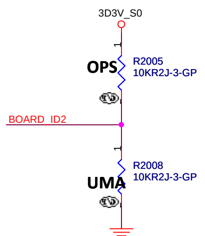
The internal pull-down is disabled after PLTRST# deasserts



Need double confirm, GPIO table set to GPI if that's needed PH or PL

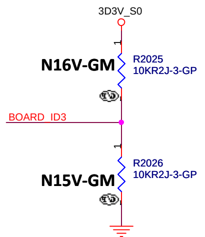
BIOS strap pin:

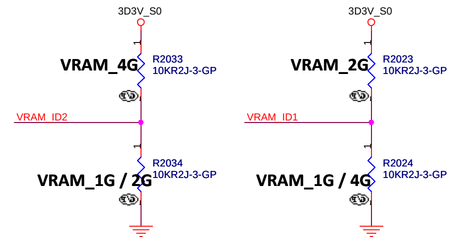
BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1



BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID3
N15V-GM-S	0
N16V-GM-B1	1

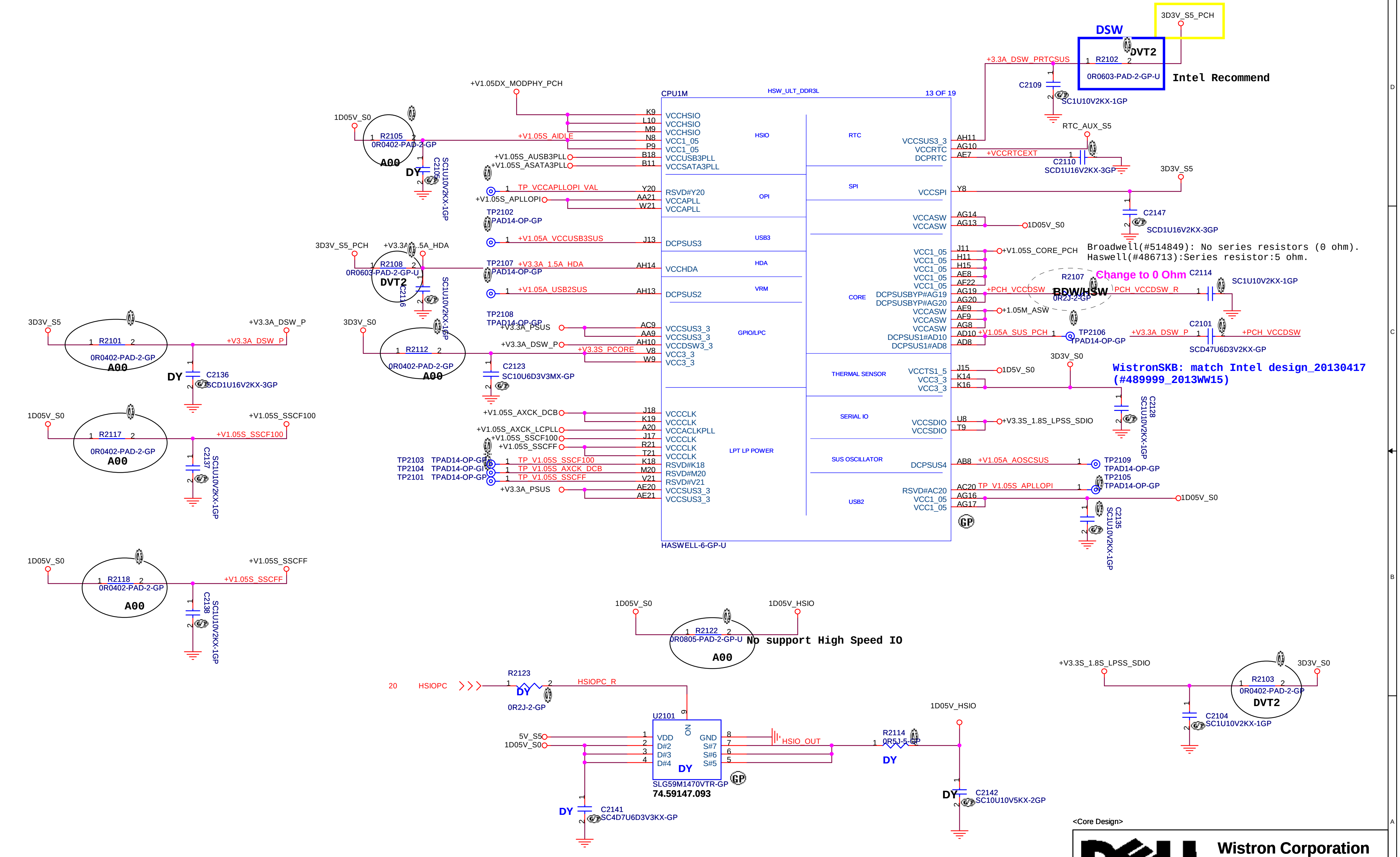




BIOS strap pin:

BIOS VRAM Size Strap pin	VRAM_ID2 (GPIO68)	VRAM_ID1 (GPIO67)
1G	0	0
2G	0	1
4G	1	0

Main Func = PCH



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Title		
CPU (POWER1)		
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Main Func = PCH

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Title	CPU (RSVD)	
Size A4	Document Number: Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 22 of 102	

Main Func = PCH

CPU1N HSW_ULT_DDR3L 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

HASWELL-6-GP-U

GP

CPU1O HSW_ULT_DDR3L 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

HASWELL-6-GP-U

GP

<Core Design>

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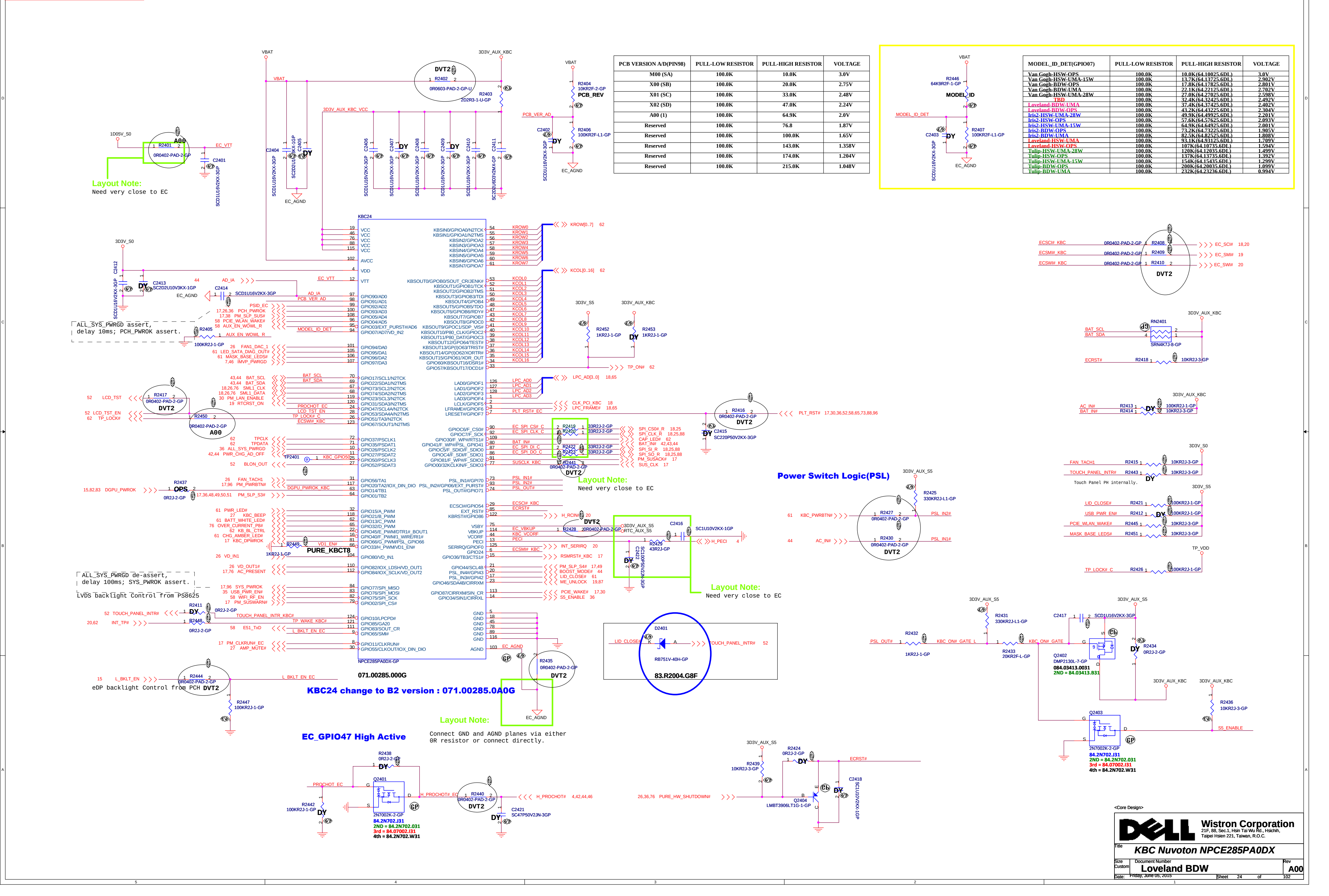
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VSS)

Size	Document Number	Rev
A4	Loveland BDW	A00

Date: Wednesday, May 27, 2015 Sheet 23 of 102

Main Func = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X00 (SB)	100.0K	20.0K	2.75V
X01 (SC)	100.0K	33.0K	2.48V
X02 (SD)	100.0K	47.0K	2.24V
A00 (1)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Van Gogh-HSW-OPS	100.0K	10.0K(64.10025.6DL)	3.0V
Van Gogh-HSW-UMA-15W	100.0K	13.7K(64.13725.6DL)	2.902V
Van Gogh-BDW-OPS	100.0K	17.8K(64.17825.6DL)	2.801V
Van Gogh-BDW-UMA	100.0K	22.1K(64.22125.6DL)	2.702V
Van Gogh-HSW-UMA-28W	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
Loveland-BDW-UMA	100.0K	37.4K(64.37425.6DL)	2.402V
Loveland-BDW-OPS	100.0K	43.2K(64.43225.6DL)	2.304V
Iris2-HSW-UMA-28W	100.0K	49.9K(64.49925.6DL)	2.201V
Iris2-HSW-OPS	100.0K	57.6K(64.57625.6DL)	2.093V
Iris2-HSW-UMA-15W	100.0K	64.9K(64.64925.6DL)	2.001V
Iris2-BDW-OPS	100.0K	73.2K(64.73225.6DL)	1.905V
Iris2-BDW-UMA	100.0K	82.5K(64.82525.6DL)	1.808V
Loveland-HSW-UMA	100.0K	93.1K(64.93125.6DL)	1.709V
Loveland-HSW-OPS	100.0K	107K(64.10735.6DL)	1.594V
Tulip-HSW-UMA-28W	100.0K	120K(64.12035.6DL)	1.499V
Tulip-HSW-OPS	100.0K	137K(64.13735.6DL)	1.392V
Tulip-HSW-UMA-15W	100.0K	154K(64.15435.6DL)	1.299V
Tulip-BDW-OPS	100.0K	200K(64.20035.6DL)	1.099V
Tulip-BDW-UMA	100.0K	232K(64.23236.6DL)	0.994V

<Core Design>

Wistron Corporation
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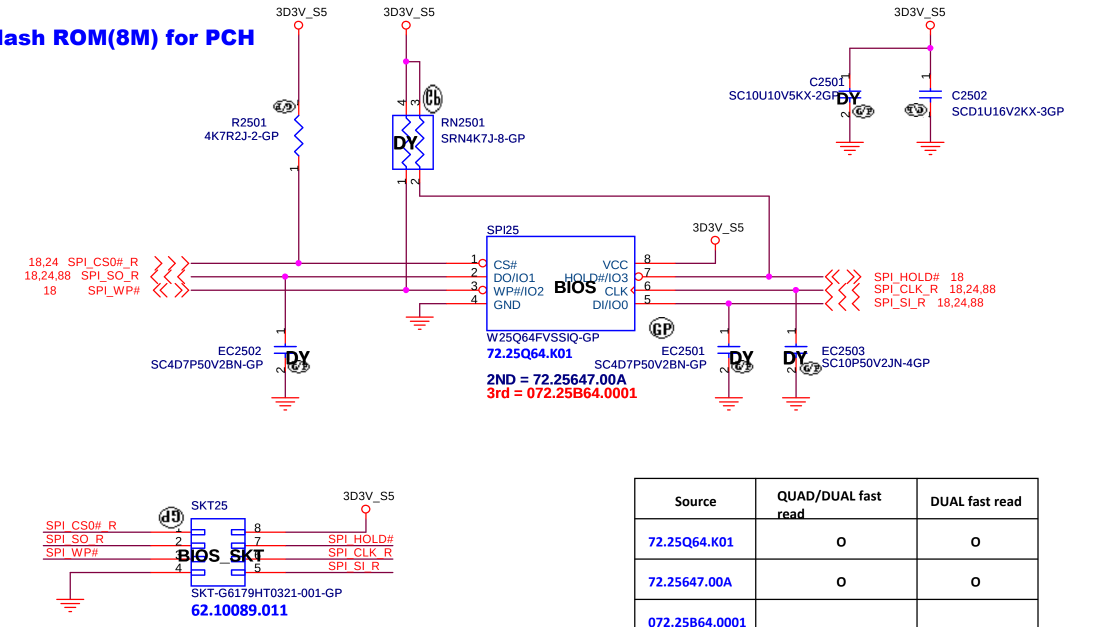
Title: KBC Nuvoton NPCE285PA0DX

Size: Custom | Document Number: Loveland BDW | Rev: A00

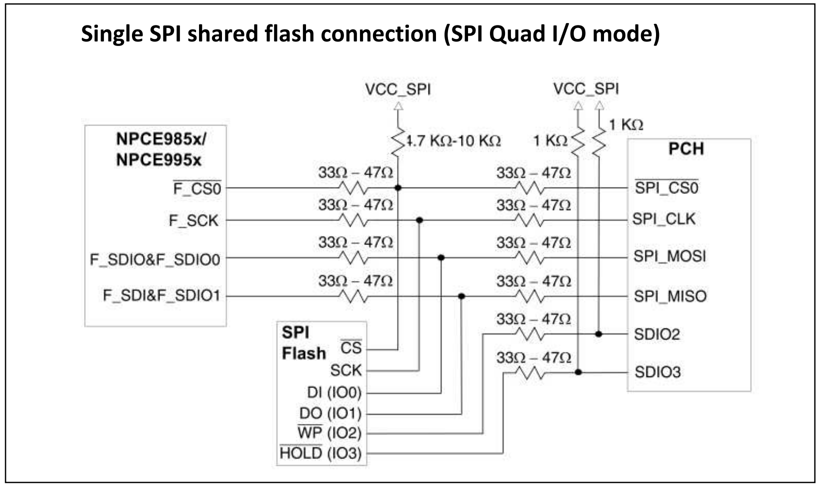
Date: Friday, June 05, 2015 | Sheet 24 of 102

Main Func = SPI Flash

SPI Flash ROM(8M) for PCH

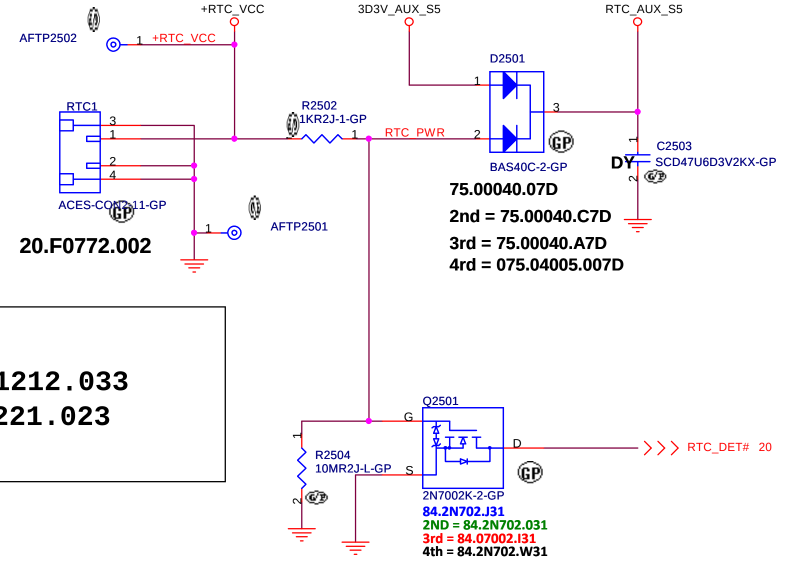


Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O
072.25B64.0001	O	O



Refer to "NCPE985x/ NPCE995x board design reference guide"

Main Func = RTC



RTC:
main:23.21212.033
2nd:23.21221.023

<Core Design>

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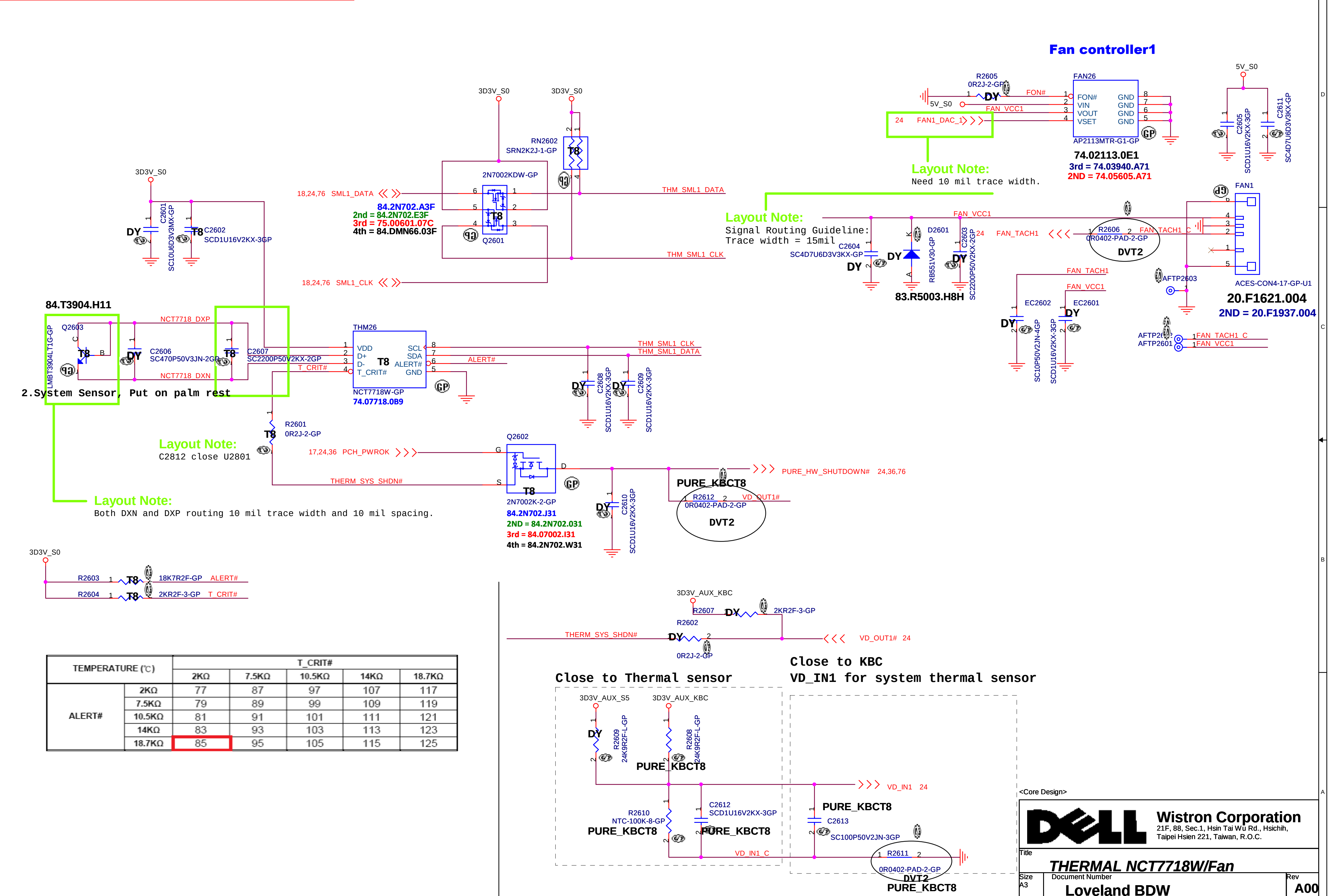
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A3	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 25 of 102	

Main Func = Thermal Sensor



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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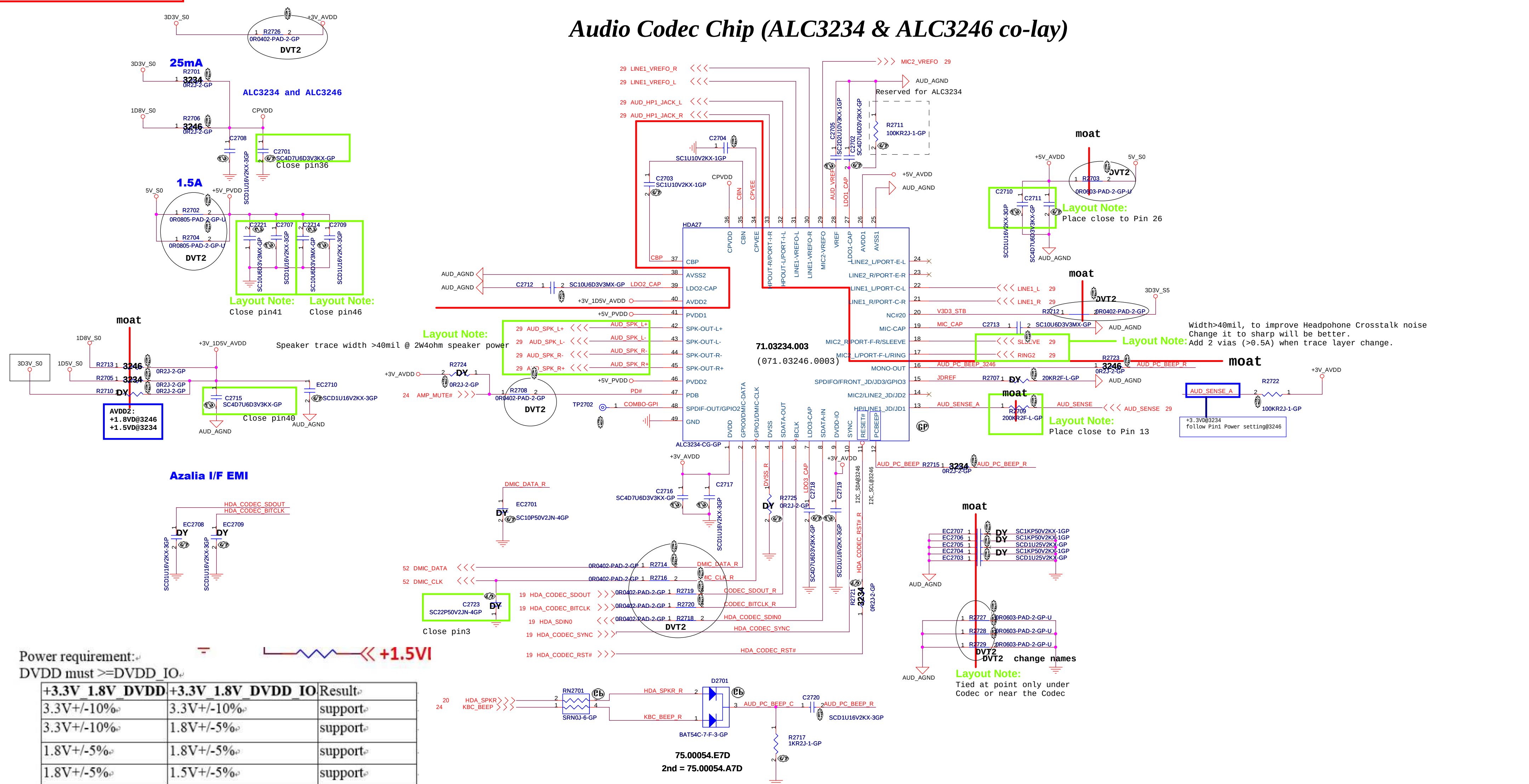
Title: **THERMAL NCT7718W/Fan**

Size: A3 | Document Number: **Loveland BDW** | Rev: **A00**

Date: Monday, June 08, 2015 | Sheet 26 of 102

Main Func = Audio

Audio Codec Chip (ALC3234 & ALC3246 co-lay)



Power requirement:
DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

<Core Design>

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Title: Audio Codec ALC3234

Size: A2 | Document Number: Loveland BDW | Rev: A00

Date: Monday, June 08, 2015 | Sheet 27 of 102

5 4 3 2 1

D D

(Blanking)

C C

B B

A A

<Core Design>

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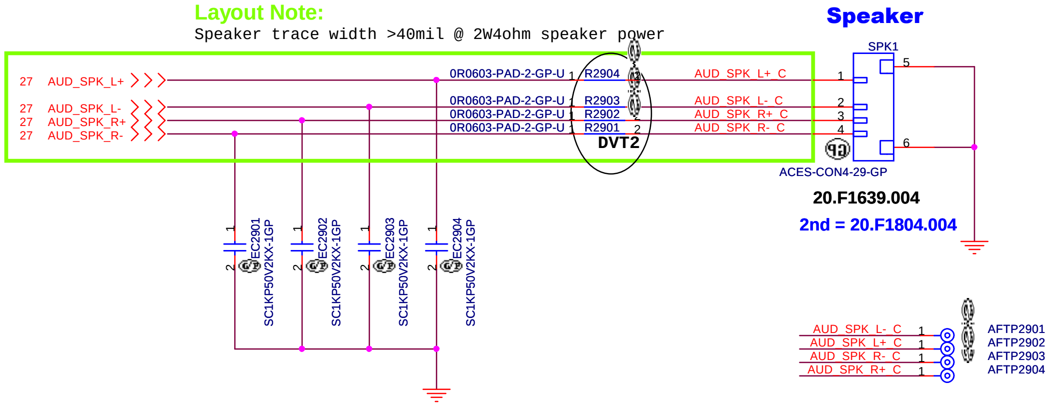
Title	**Reserved**	
Size A4	Document Number **Loveland BDW**	Rev **A00**
Date: Wednesday, May 27, 2015	Sheet 28 of 102	

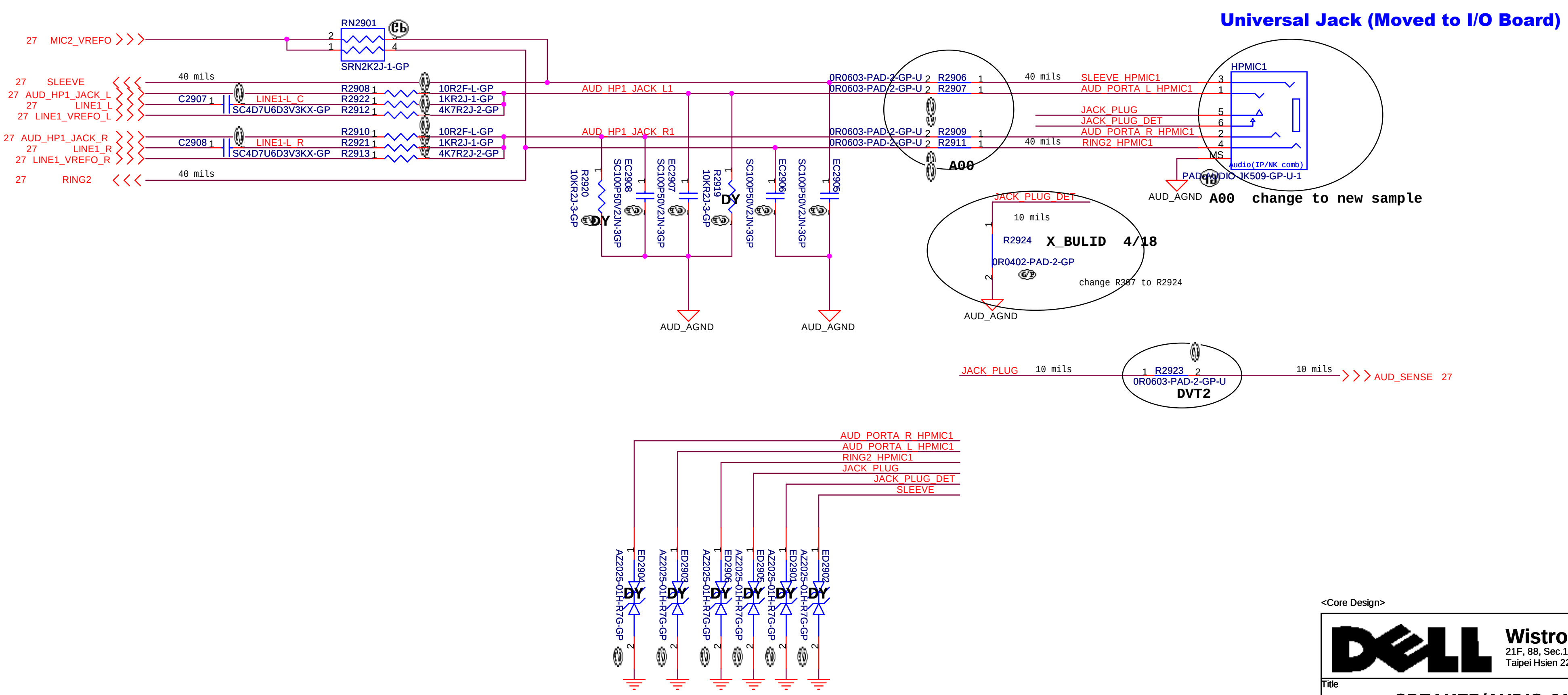
5 4 3 2 1

Main Func = Audio



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

Universal Jack (Moved to I/O Board)



<Core Design>

Wistron Corporation
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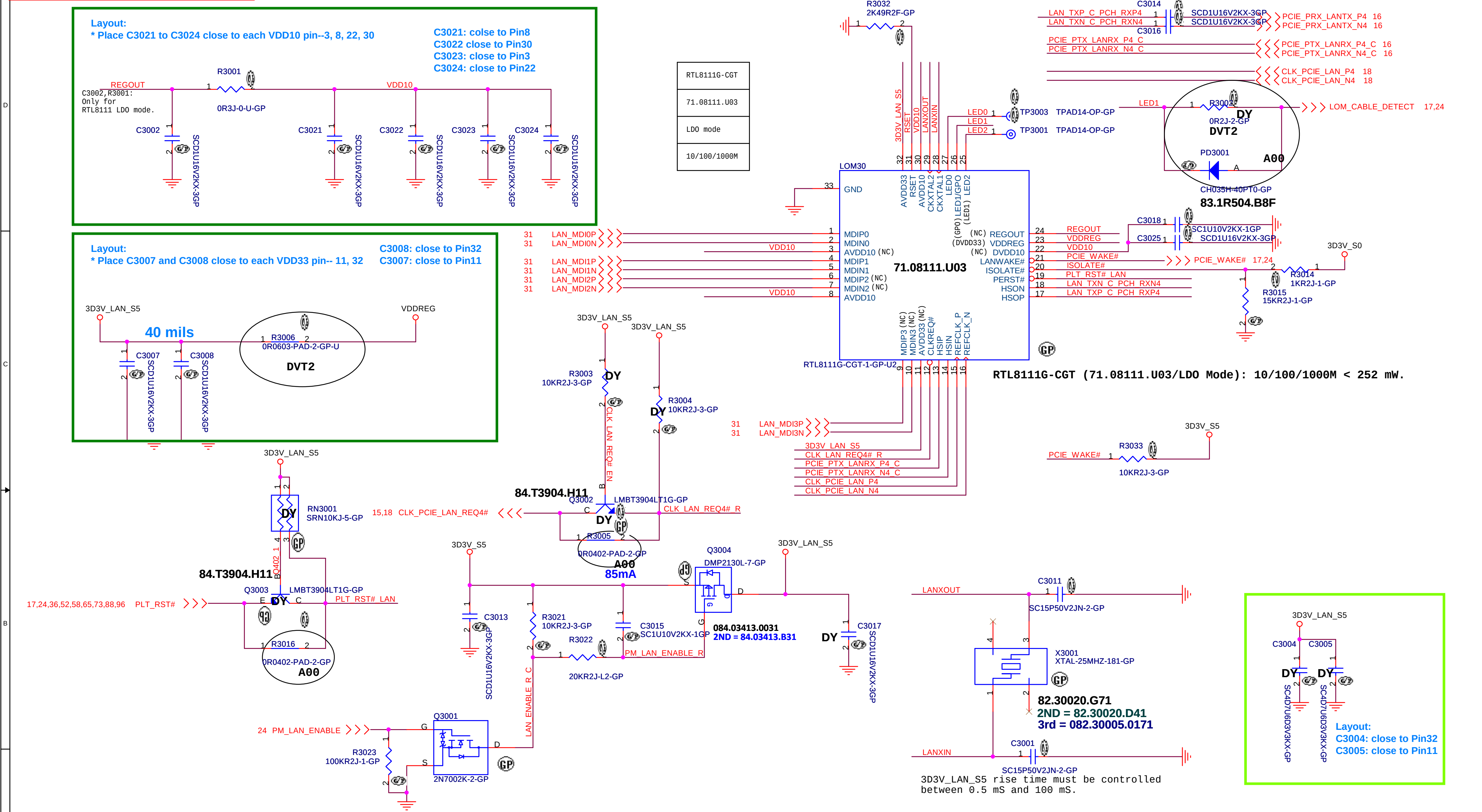
Title: **SPEAKER/AUDIO JACK**

Size: A3 | Document Number: **Loveland BDW** | Rev: A00

Date: Thursday, June 18, 2015 | Sheet 29 of 102

Main Func = LAN



	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X

<Core Design>

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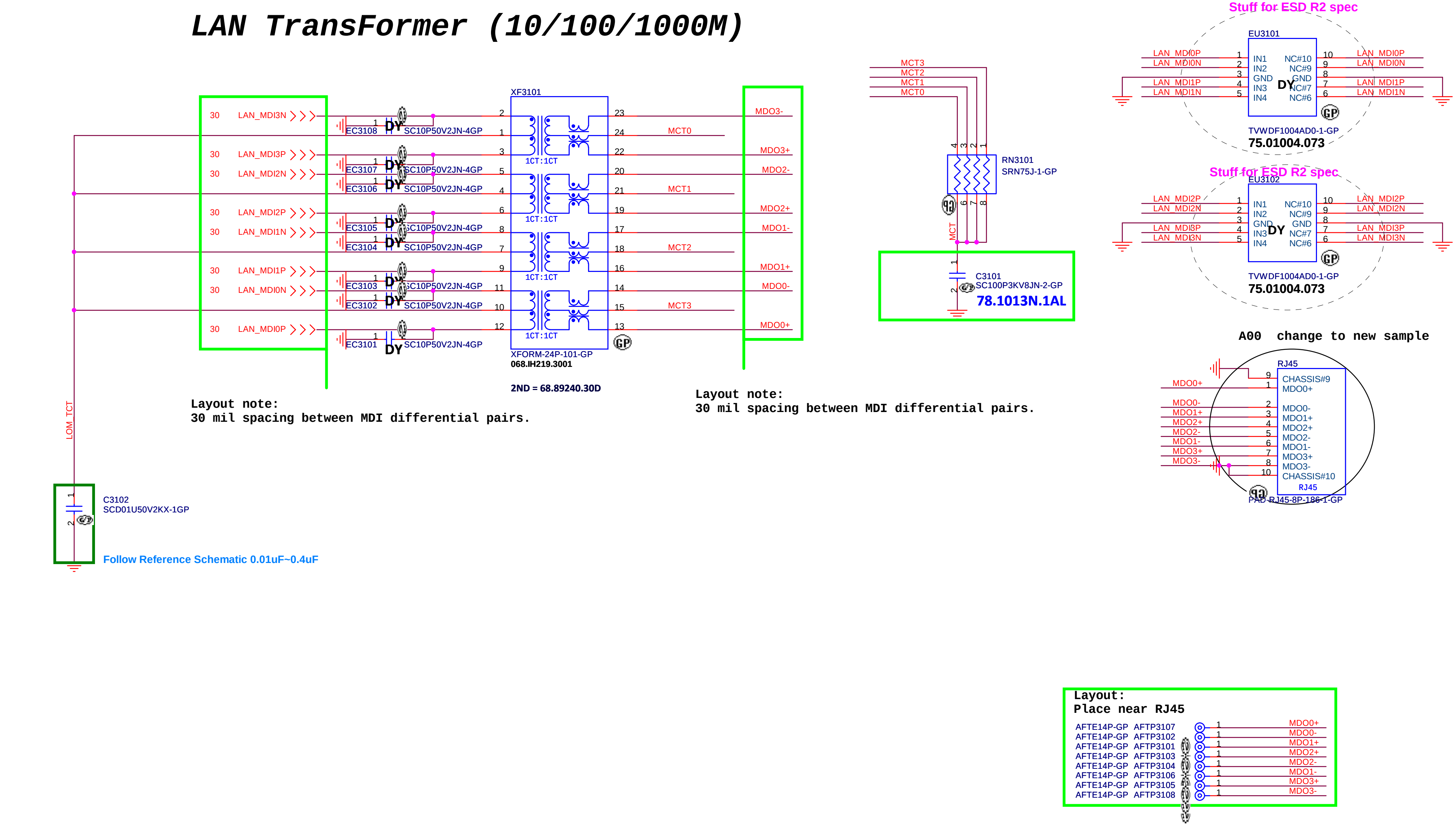
Title: LAN RTL8111
Size: A3
Document Number: Loveland BDW
Rev: A00
Date: Friday, June 05, 2015

Main Func = LAN

LAN TransFormer (10/100/1000M)



<Core Design>

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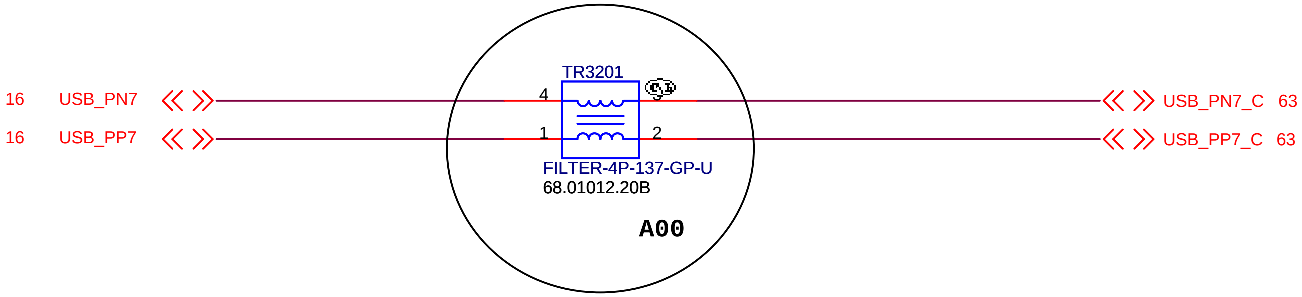
Title	XFOM&RJ45	
Size A3	Document Number Loveland BDW	Rev A00
Date: Friday, July 24, 2015	Sheet 31 of 102	

Main Func = Card Reader



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Card Reader-RTS5170***	
Size: A4	Document Number: ***Loveland BDW***	Rev: ***A00***
Date: Wednesday, May 27, 2015	Sheet 32 of 102	

Main Func = Card Reader

(Blanking)

<Core Design>

Wistron Corporation
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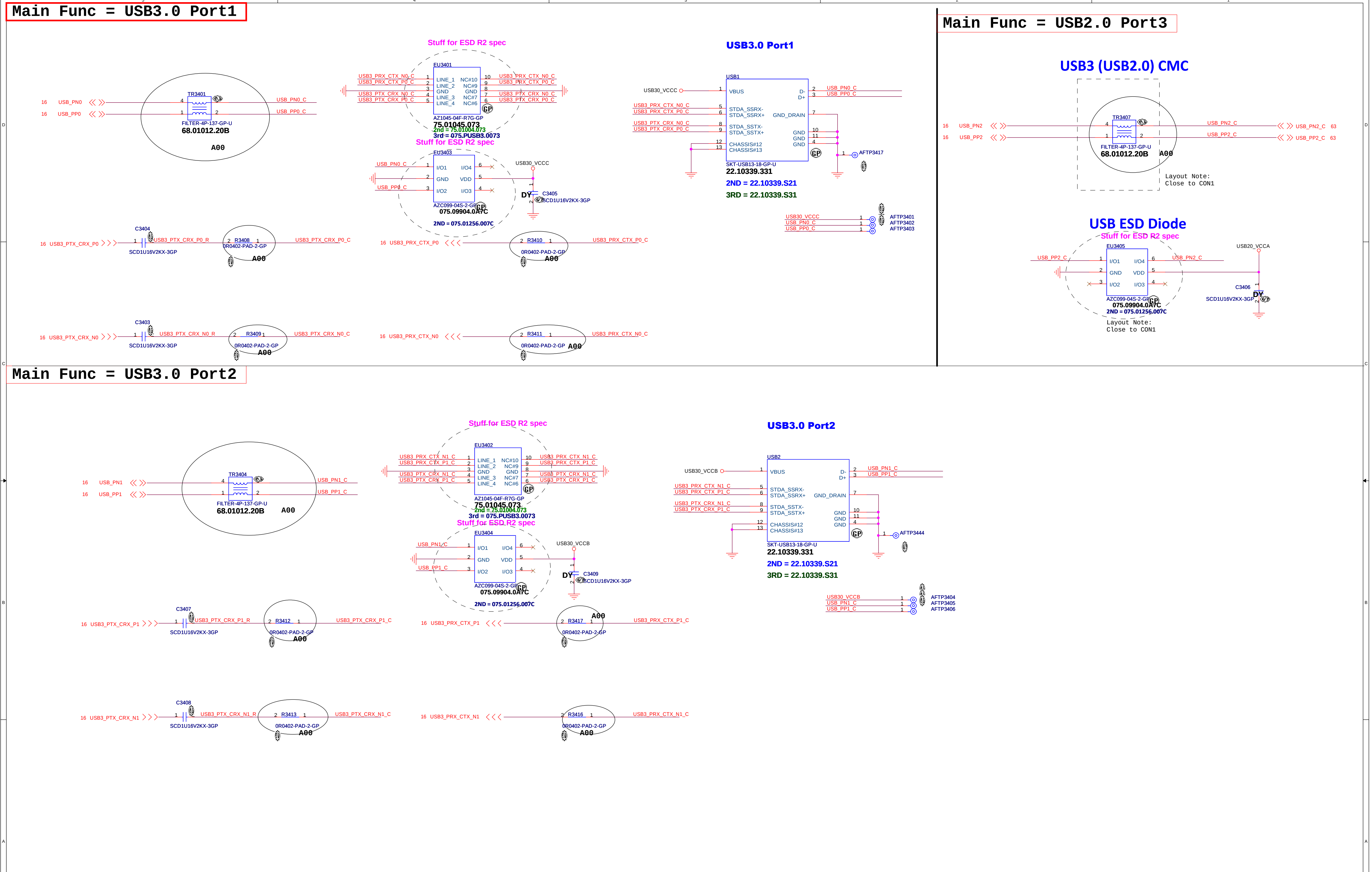
Taipei Hsien 221, Taiwan, R.O.C.

Title	*reserved*	
Size A4	Document Number *Loveland BDW*	Rev *A00*
Date: Wednesday, May 27, 2015	Sheet 33 of 102	

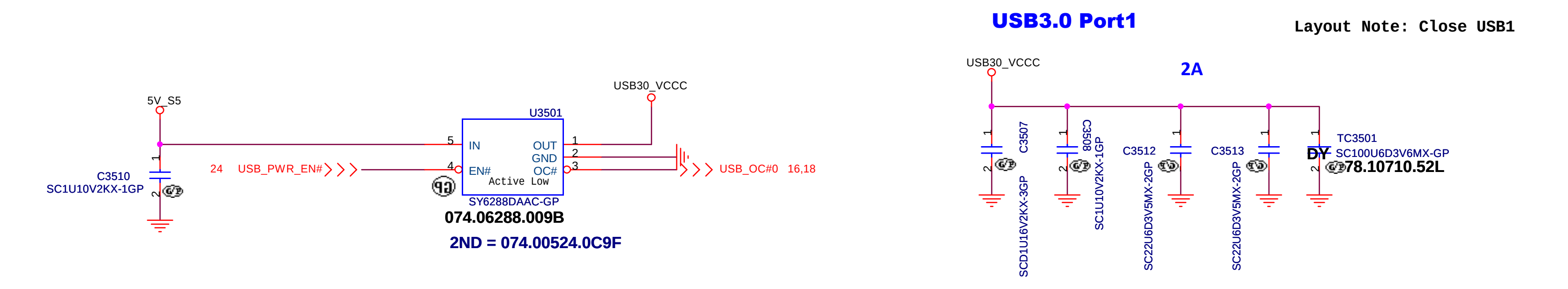


<Core Design>

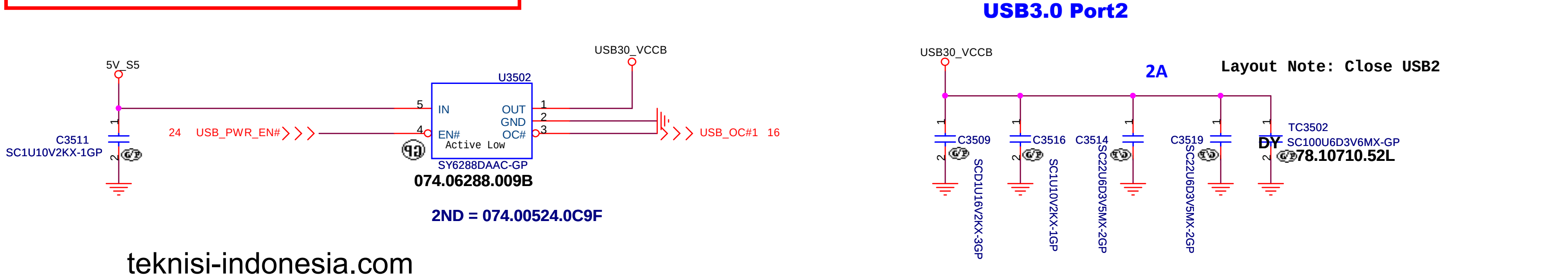
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 CONN		
Size A2	Document Number: Loveland BDW		Rev A00
Date: Monday, June 08, 2015	Sheet 34	of 102	

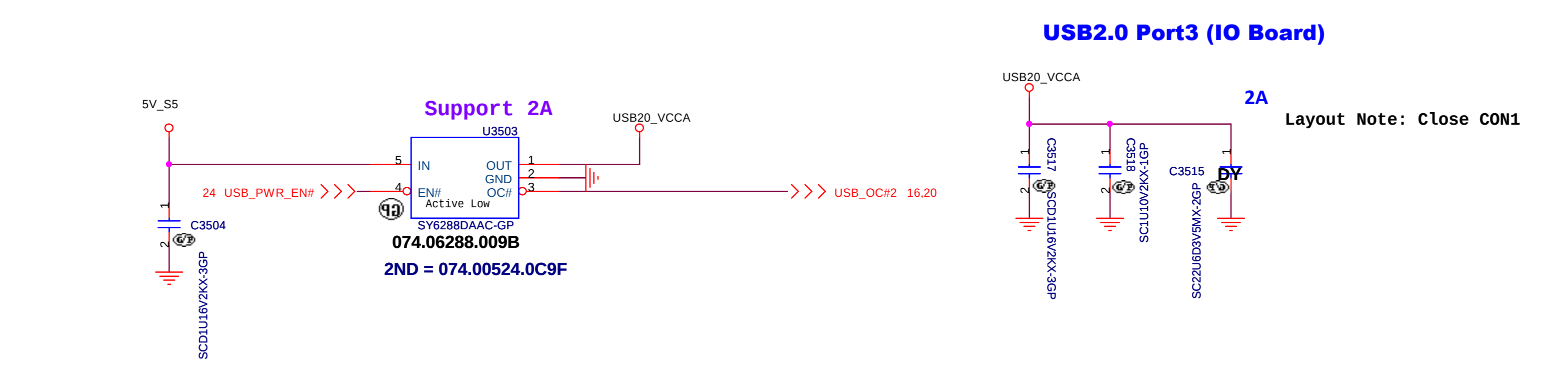
Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



Main Func = USB2.0 Port3



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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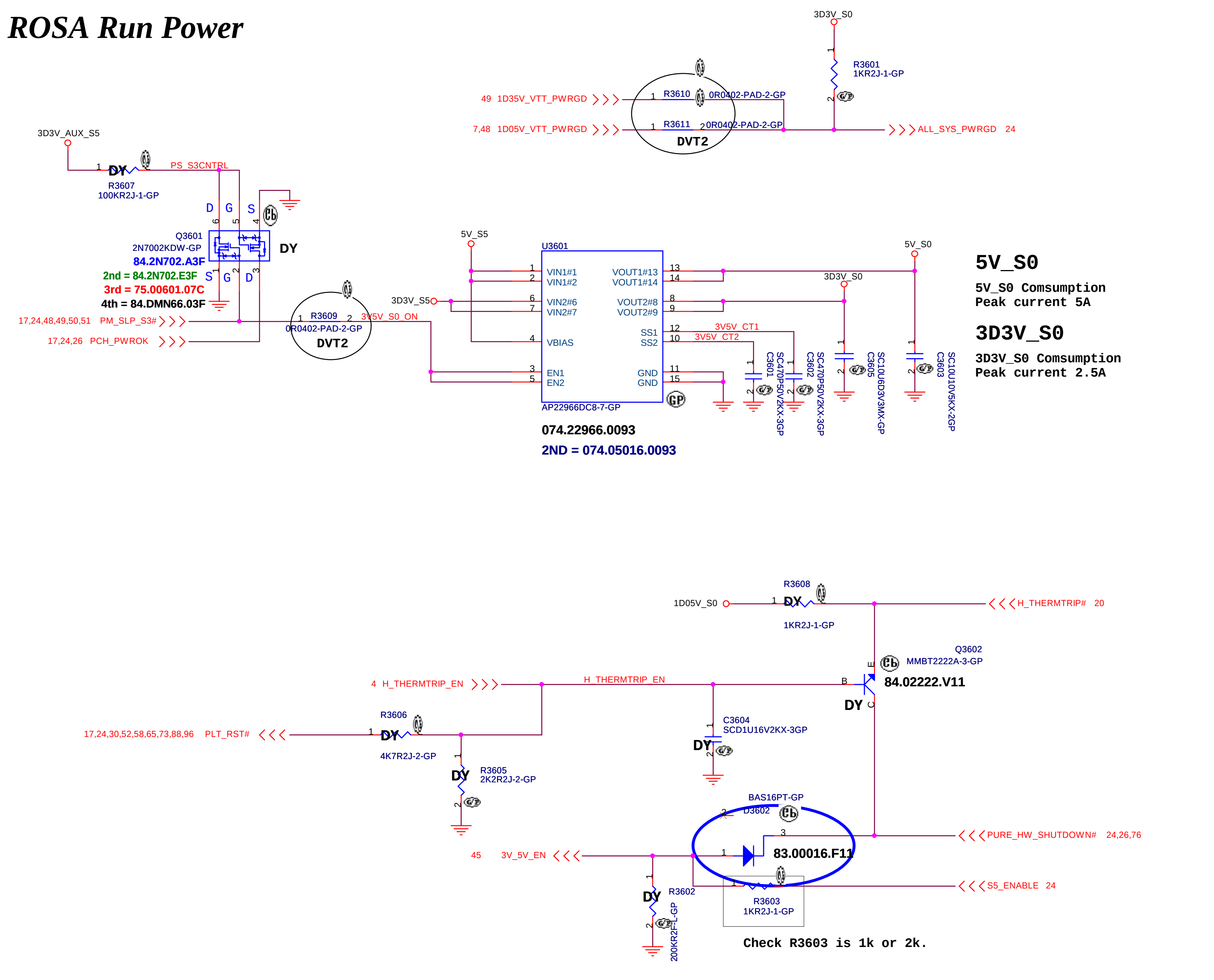
Title	USB Power SW	
Size	Document Number: Loveland BDW	Rev: A00
Date: Friday, June 05, 2015	Sheet 35 of 102	

Main Func = Power Plane & Sequence

Power Good

ROSA Run Power

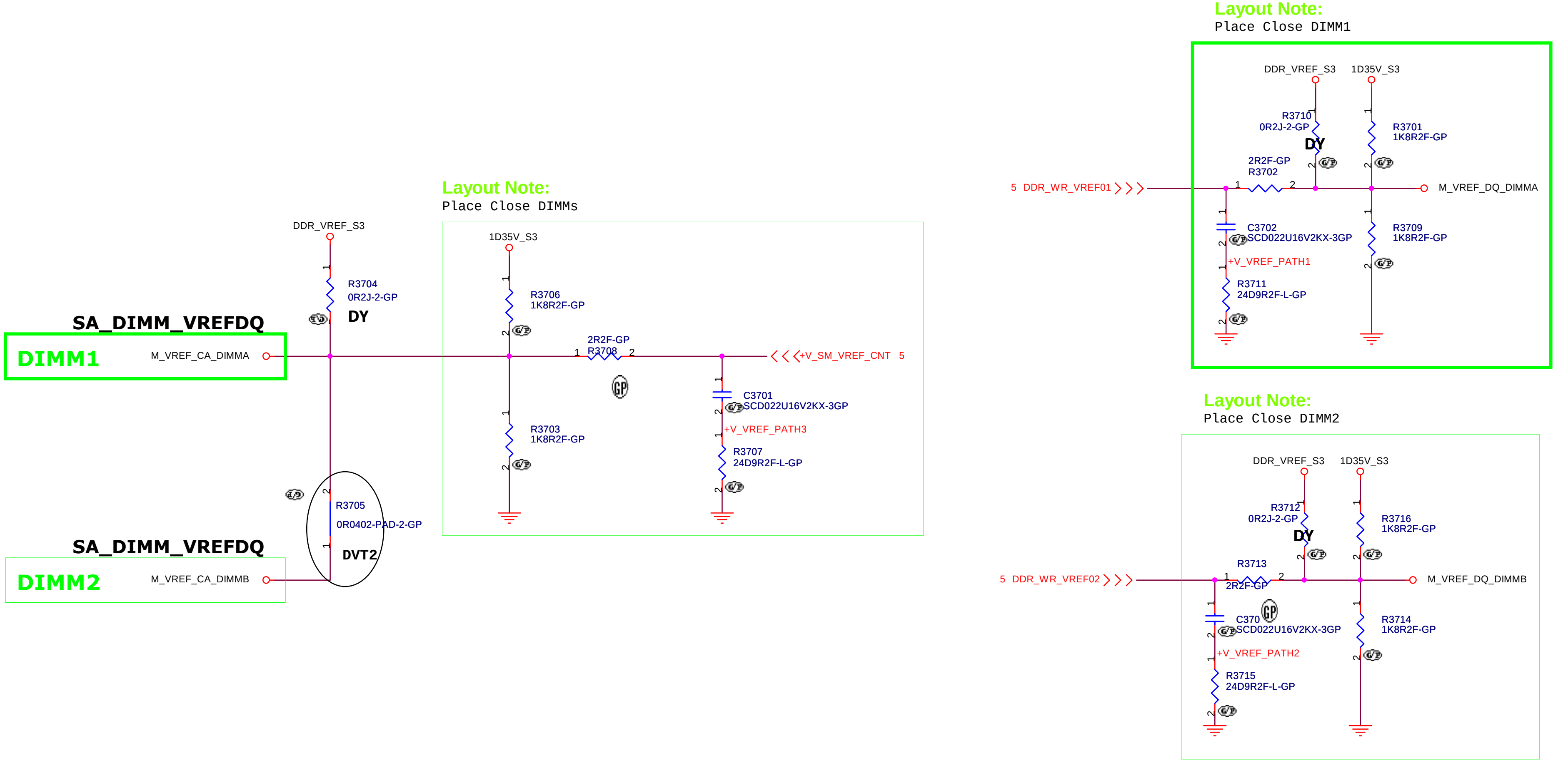


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Power Plane Enable*
Size	A3
Document Number	Loveland BDW
Rev	A00
Date:	Friday, June 05, 2015
Sheet	36 of 102

Main Func = DIMM1
Main Func = DIMM2

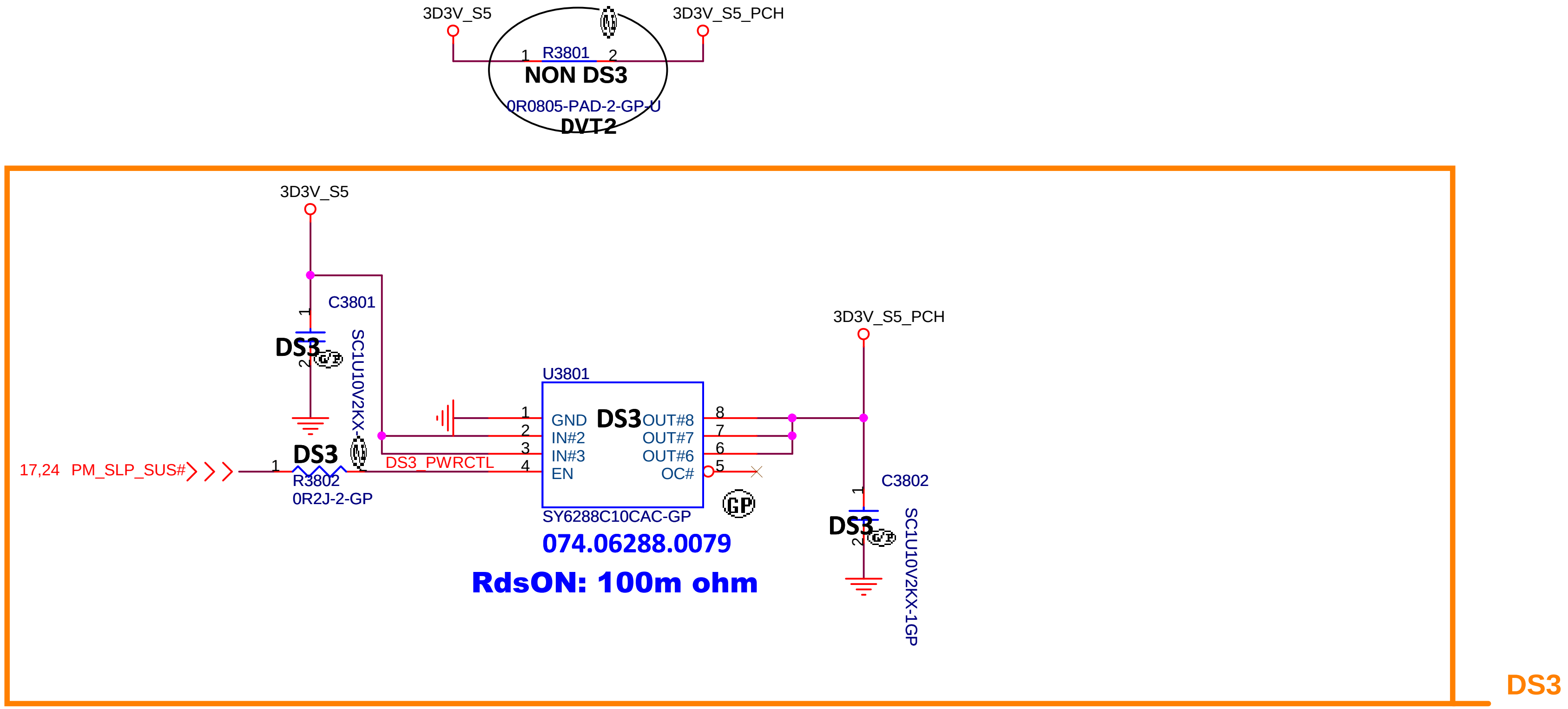


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S3 Reduction Circuit	
Size A3	Document Number: Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 37 of 102	

Main Func = Power Plane & Sequence



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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DSW**

Size: A4 | Document Number: **Loveland BDW** | Rev: **A00**

Date: Wednesday, May 27, 2015 | Sheet 38 of 102

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<Core Design>

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Title	(Reserved)	
Size A4	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 39 of 102	

(Blanking)

<Core Design>

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Title		
	Reserved	
Size: A4	Document Number: ***Loveland BDW***	Rev: ***A00***
Date: Wednesday, May 27, 2015	Sheet 40 of 102	

(Blanking)

<Core Design>

Wistron Corporation
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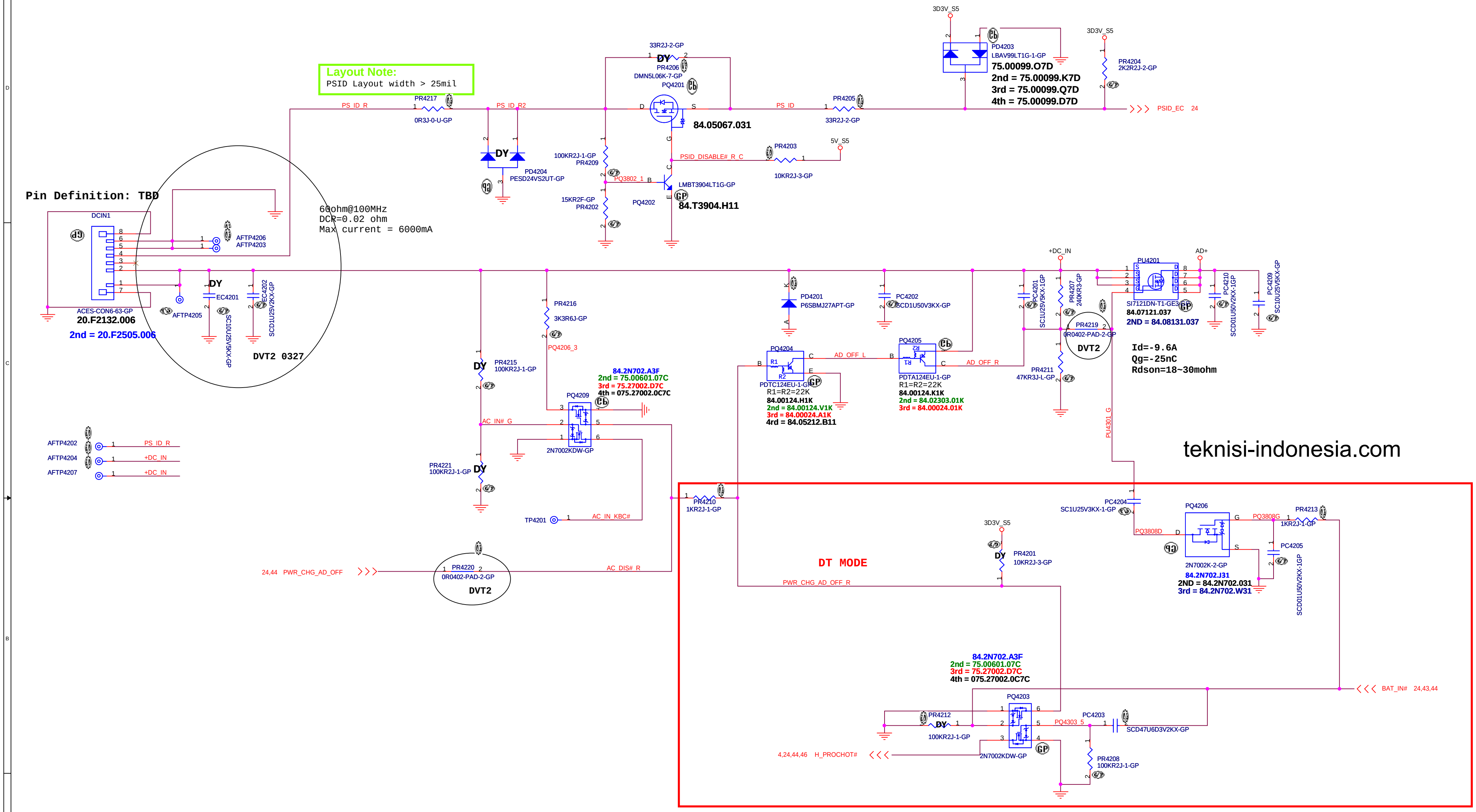
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved		
Size: A4	Document Number: Loveland BDW	Rev: A00
Date: Wednesday, May 27, 2015	Sheet 41 of 102	

Main Func = ADT Input

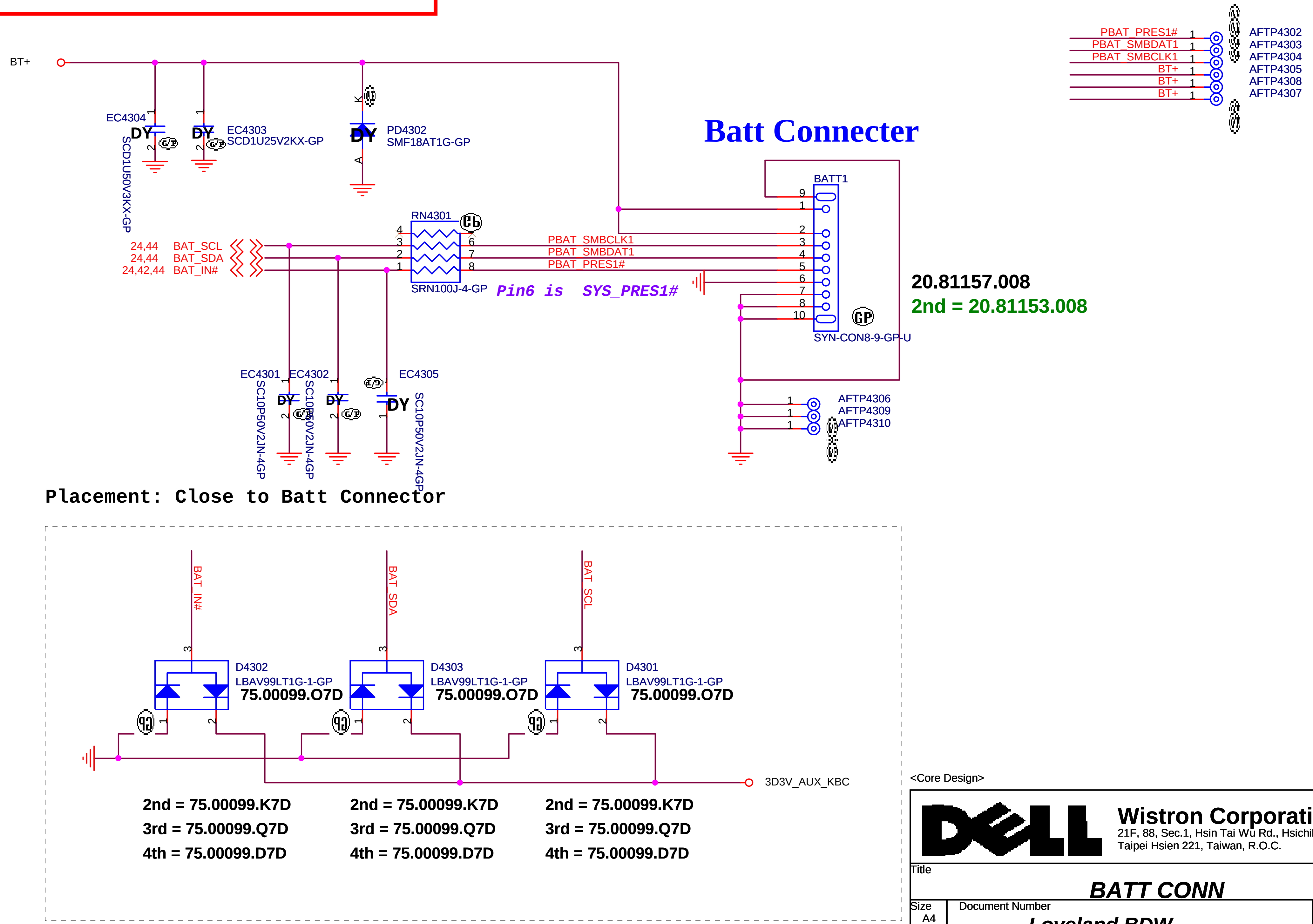


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size: C	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 42 of 102	

Main Func = M-BAT Input



<Core Design>

Wistron Corporation
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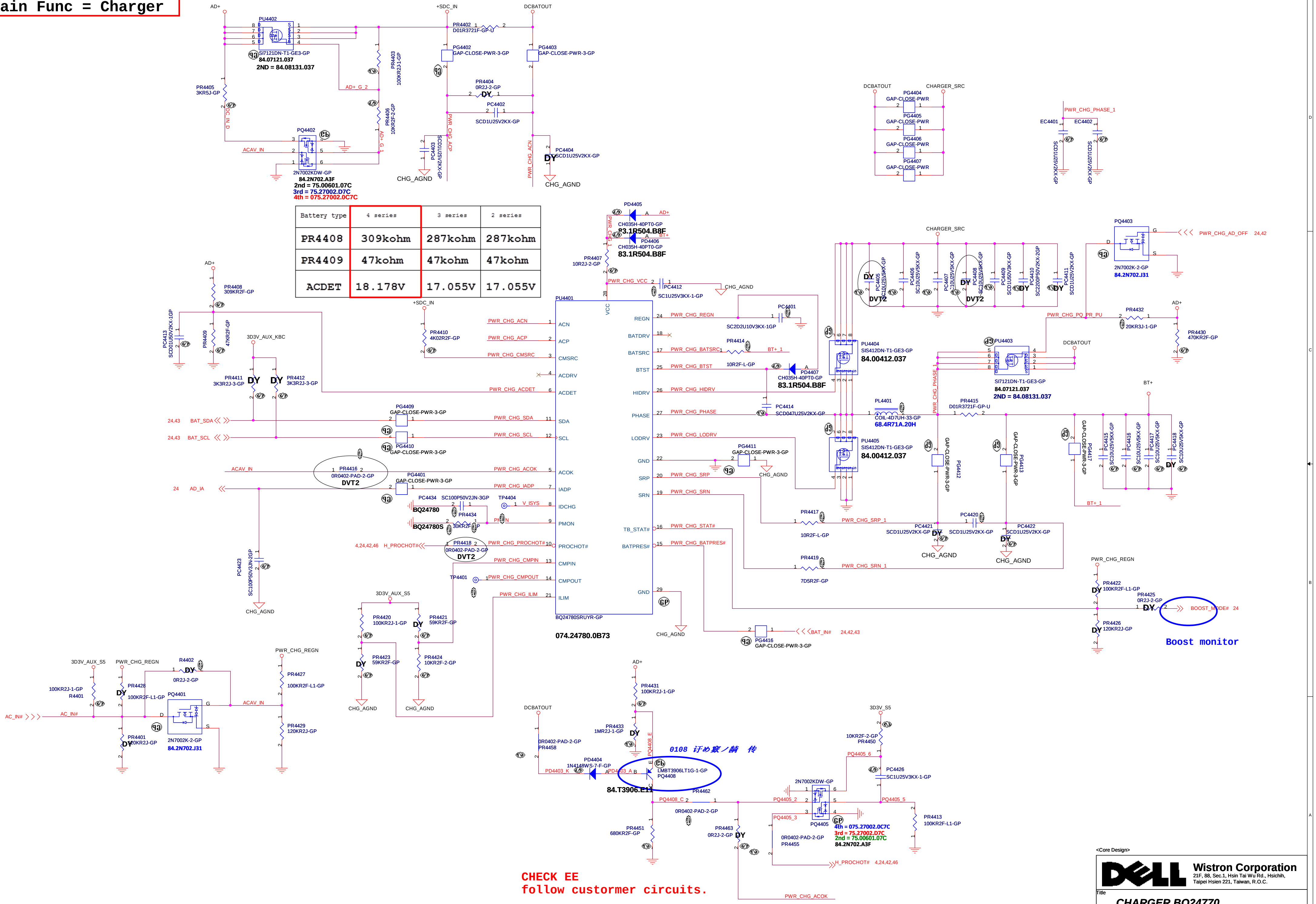
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATT CONN		
Size: A4	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 43 of 102	

Main Func = Charger

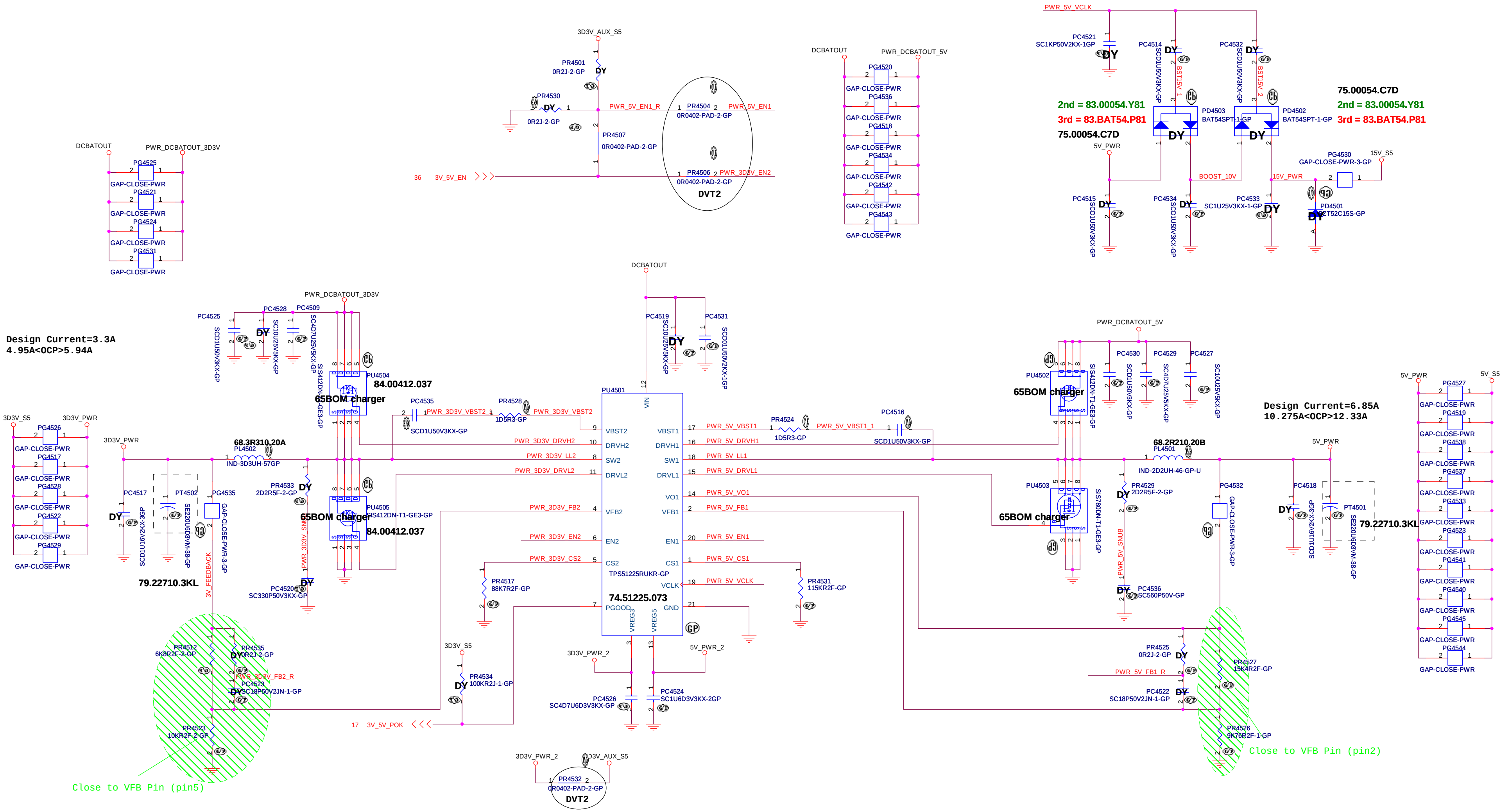
Battery type	4 series	3 series	2 series
PR4408	309kohm	287kohm	287kohm
PR4409	47kohm	47kohm	47kohm
ACDET	18.178V	17.055V	17.055V



Boost monitor

CHECK EE
follow custormer circuits.

Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

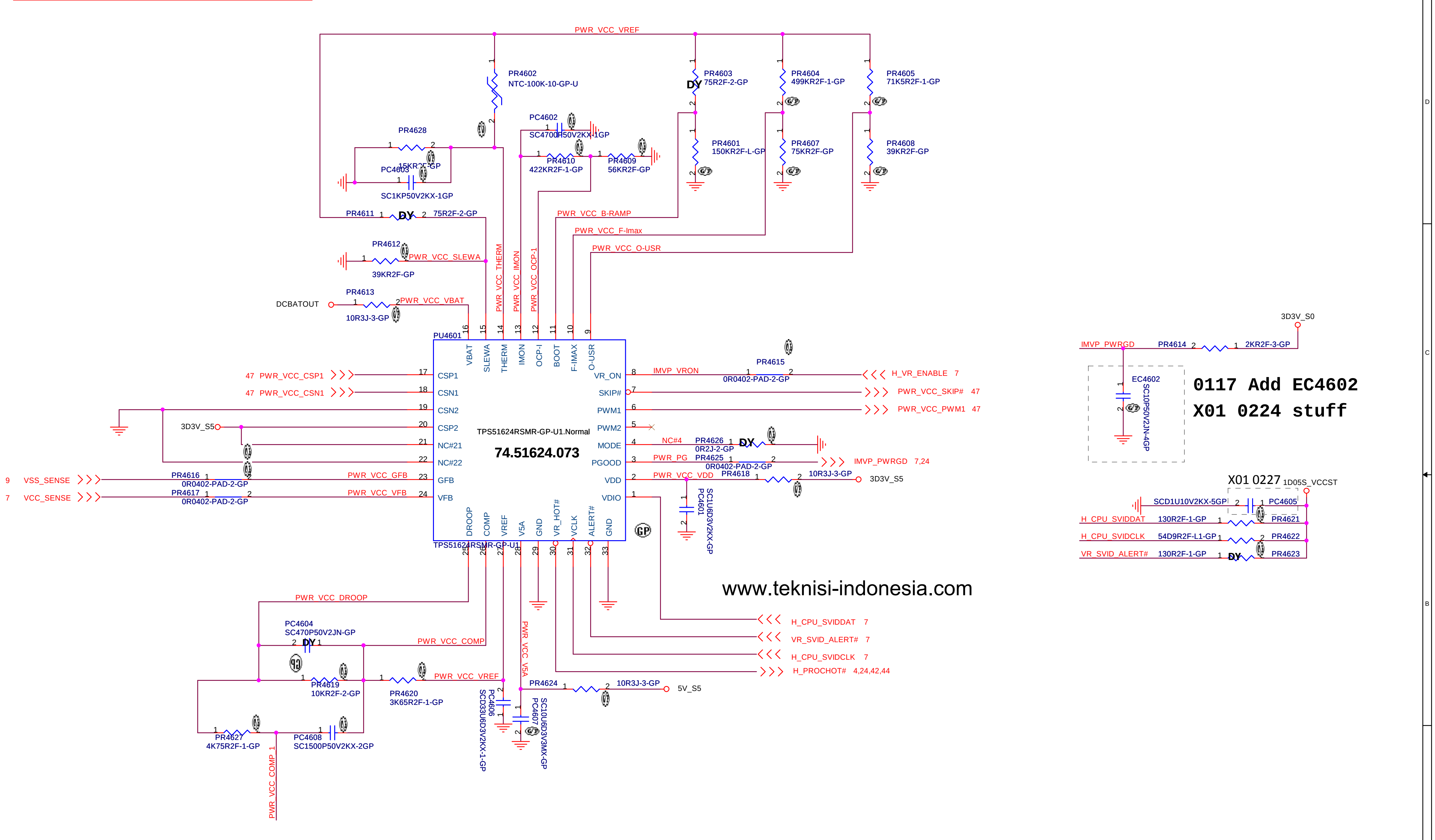
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51225_5V/3D3V	
Size A2	Document Number: Loveland BDW	Rev A00
Date: Thursday, July 02, 2015	Sheet 45 of 102	

SSID = CPU.Regulator

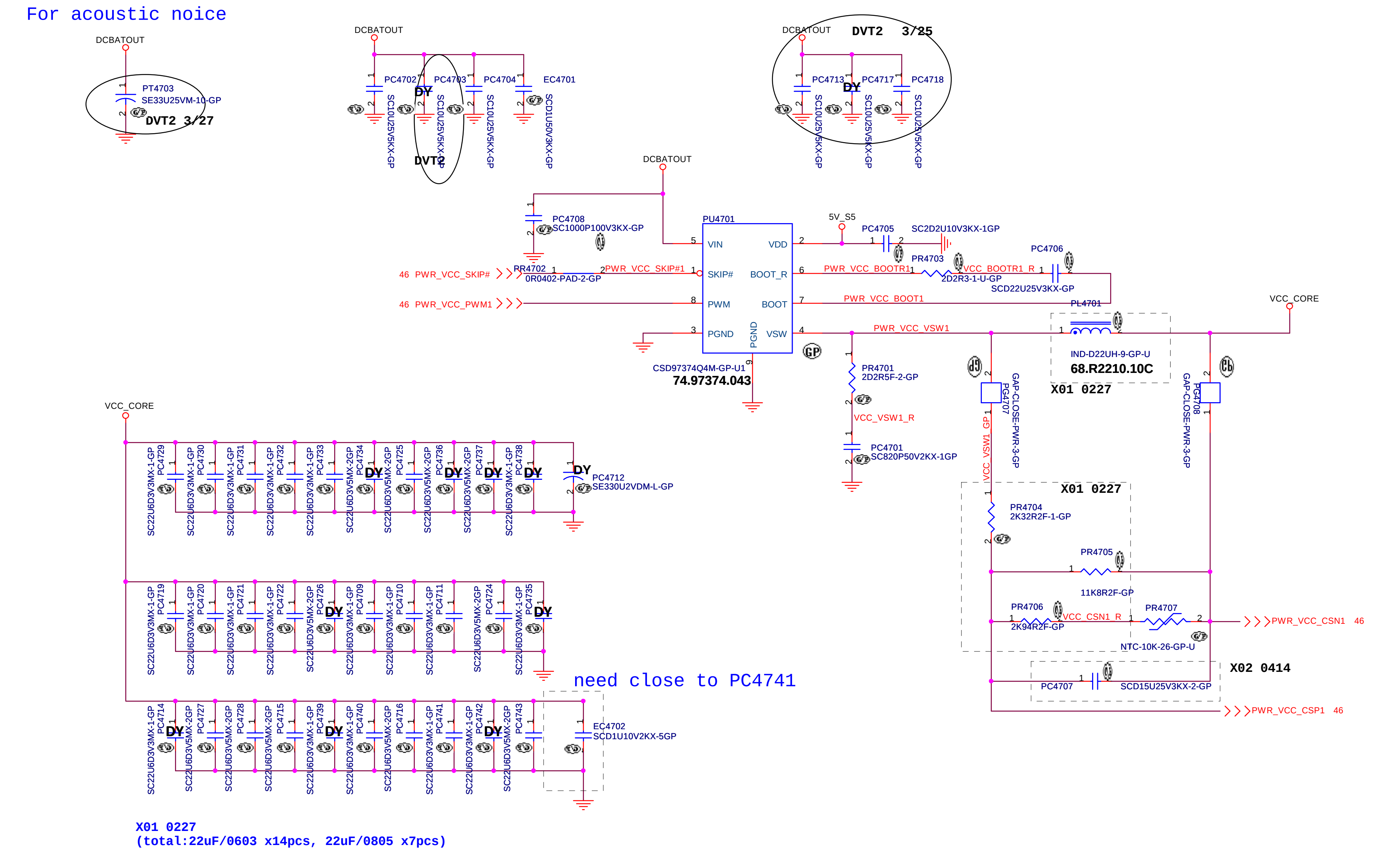


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51624_CPUCORE(1/2)	
Size A3	Document Number: Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 46 of 102	

SSID = CPU.Regulator

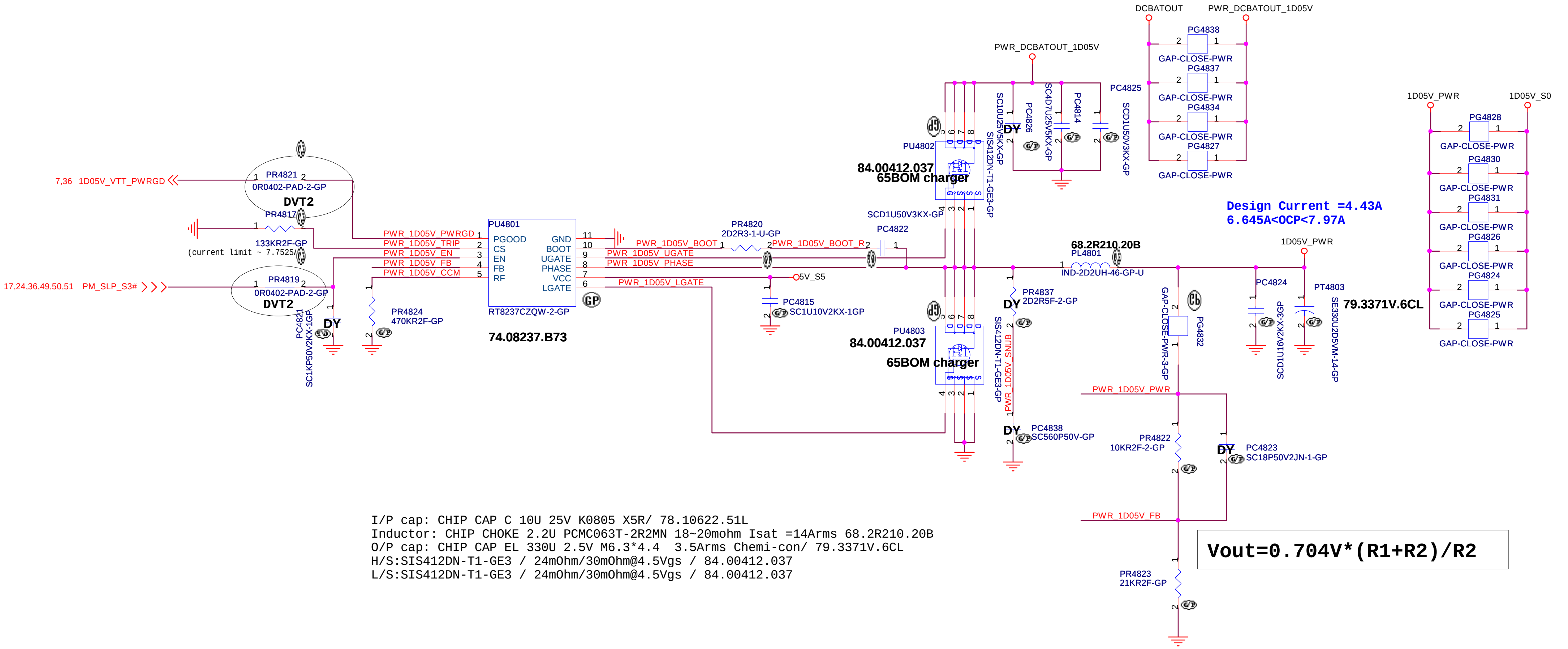


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51624_CPUCORE(2/2)
Size	A3
Document Number	Loveland BDW
Rev	A00
Date:	Wednesday, May 27, 2015
Sheet	47 of 102

Main Func = 1D05V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/ 79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

Vout=0.704V*(R1+R2)/R2

<Core Design>

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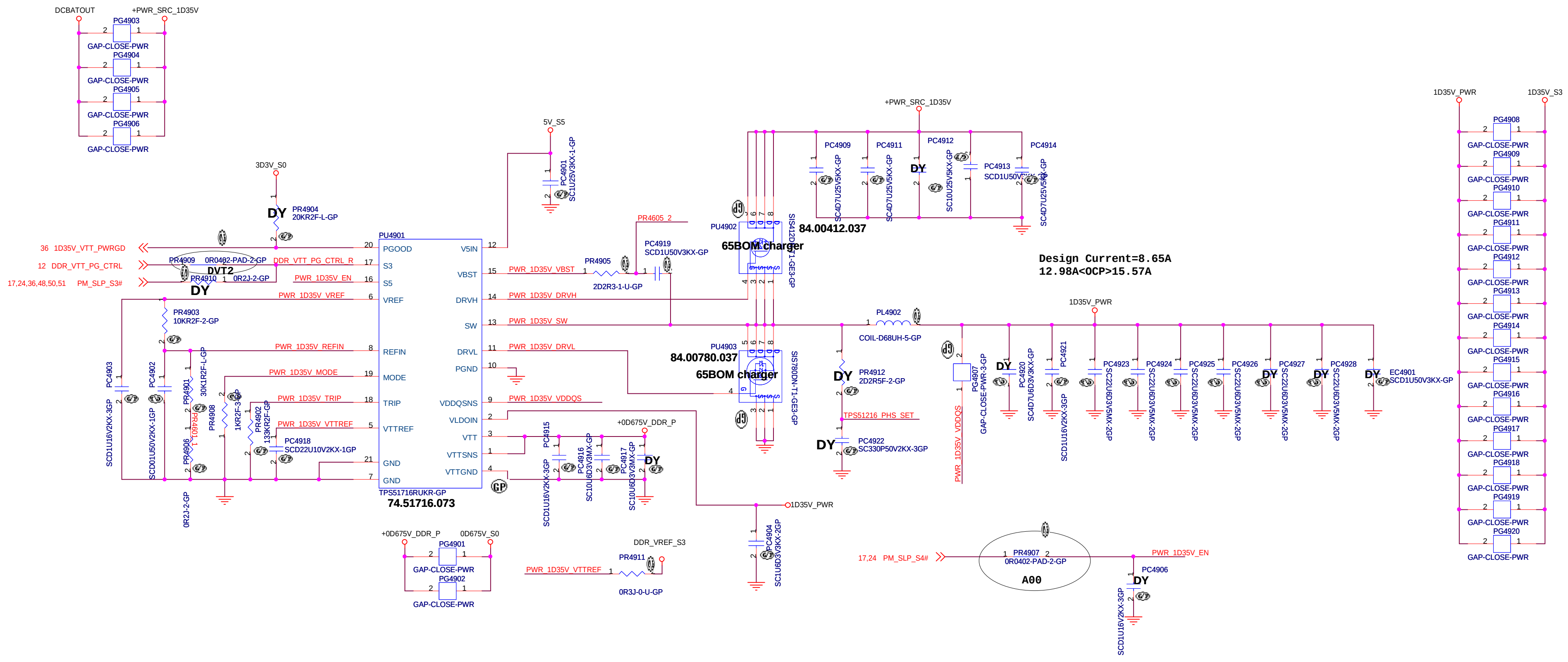
Title	RT8237_1D05V	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 48 of 102	

Main Func = VDDQ



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.5U PCMC063T-1R5MN 14~15mohm Isat =18Arms 68.1R510.10K
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

Component value	VRAM 4pcs (desugn current=8.65A)	VRAM 8pcs (desugn current=10.5A)	
PR4902	133K 64.13335.6DL	191K 64.19135.6DL	OCP setting
PC4927	DY	Stuff	output MLCC
PC4928	DY	Stuff	output MLCC

<Core Design>

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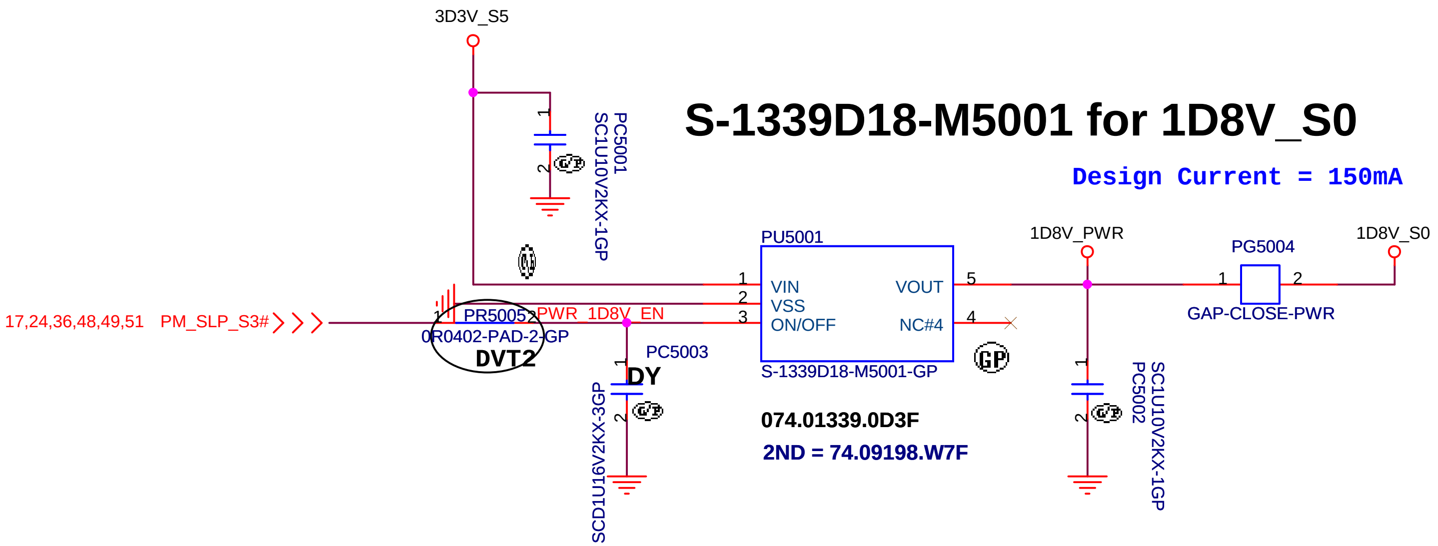
Title	**TPS51716_VDDQ_VTT**	
Size C	Document Number **Loveland BDW**	Rev **A00**
Date: Wednesday, May 27, 2015	Sheet 49 of 102	

S-1339D18-M5001 for 1D8V_S0

Design Current = 150mA



074.01339.0D3F

2ND = 74.09198.W7F

<Core Design>

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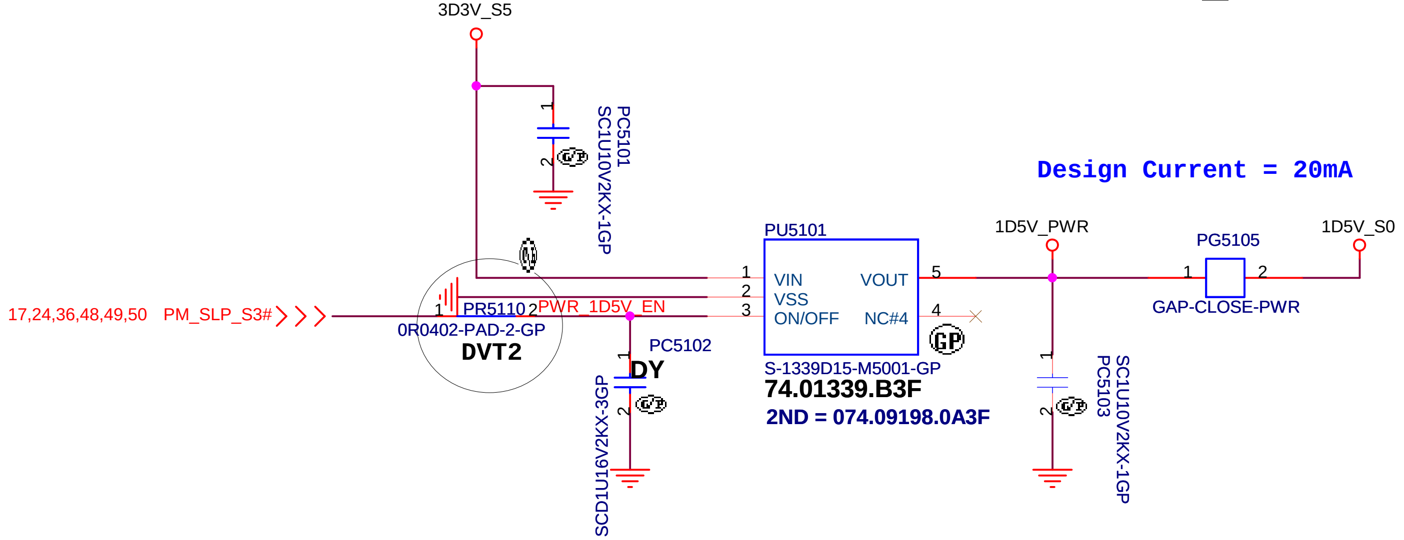
Title: ***Reserved***		
Size: A4	Document Number: ***Loveland BDW***	Rev: ***A00***
Date: Monday, June 08, 2015	Sheet 50 of 102	

Main Func = 1D5V

S-1339D15-M5001 for 1D5V_S0



<Core Design>

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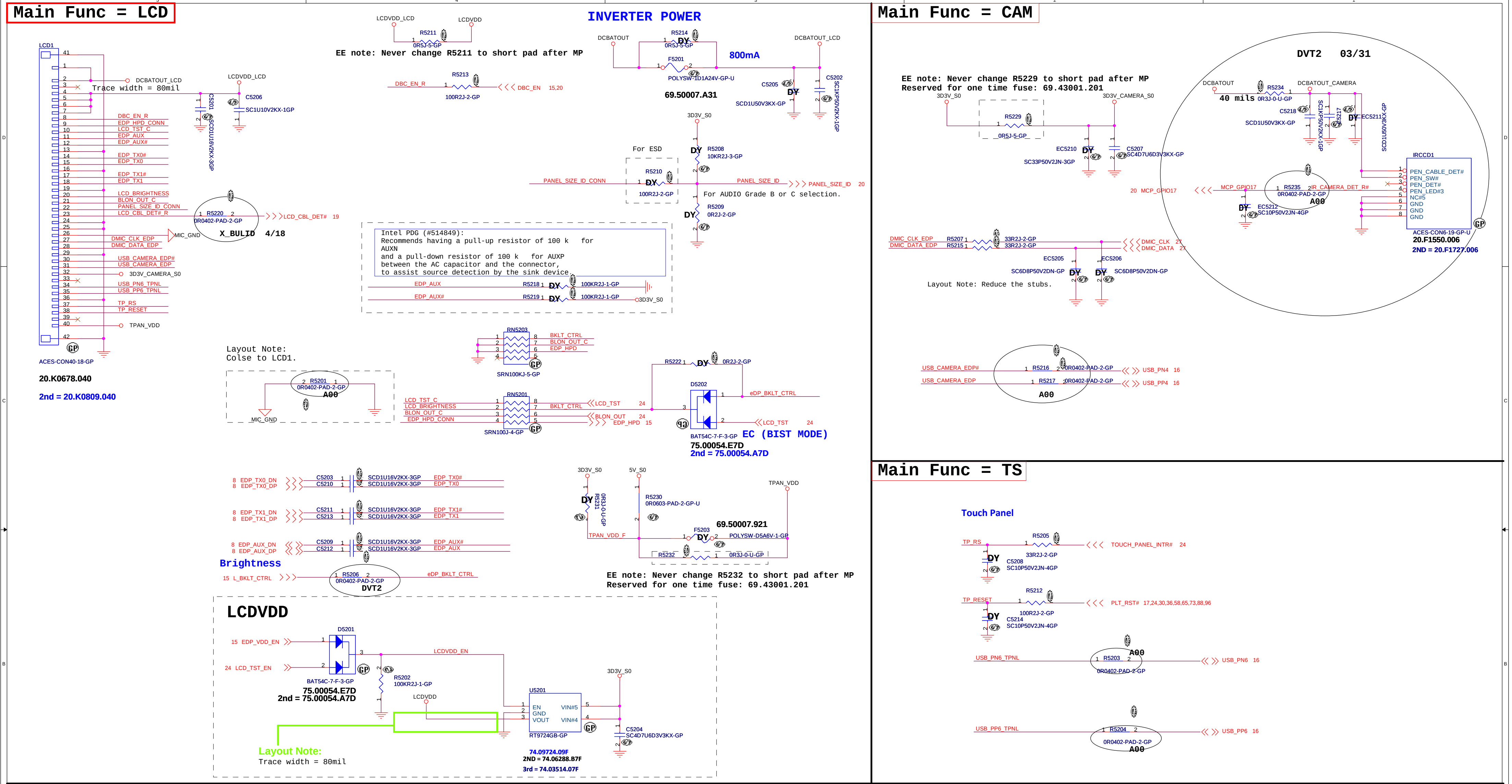
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TLV70215_1D5V	
Size: A4	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 51 of 102	



<Core Design>

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Title	LCD/Inverter CONN		
Size A2	Document Number: Loveland BDW		Rev A00
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<Core Design>

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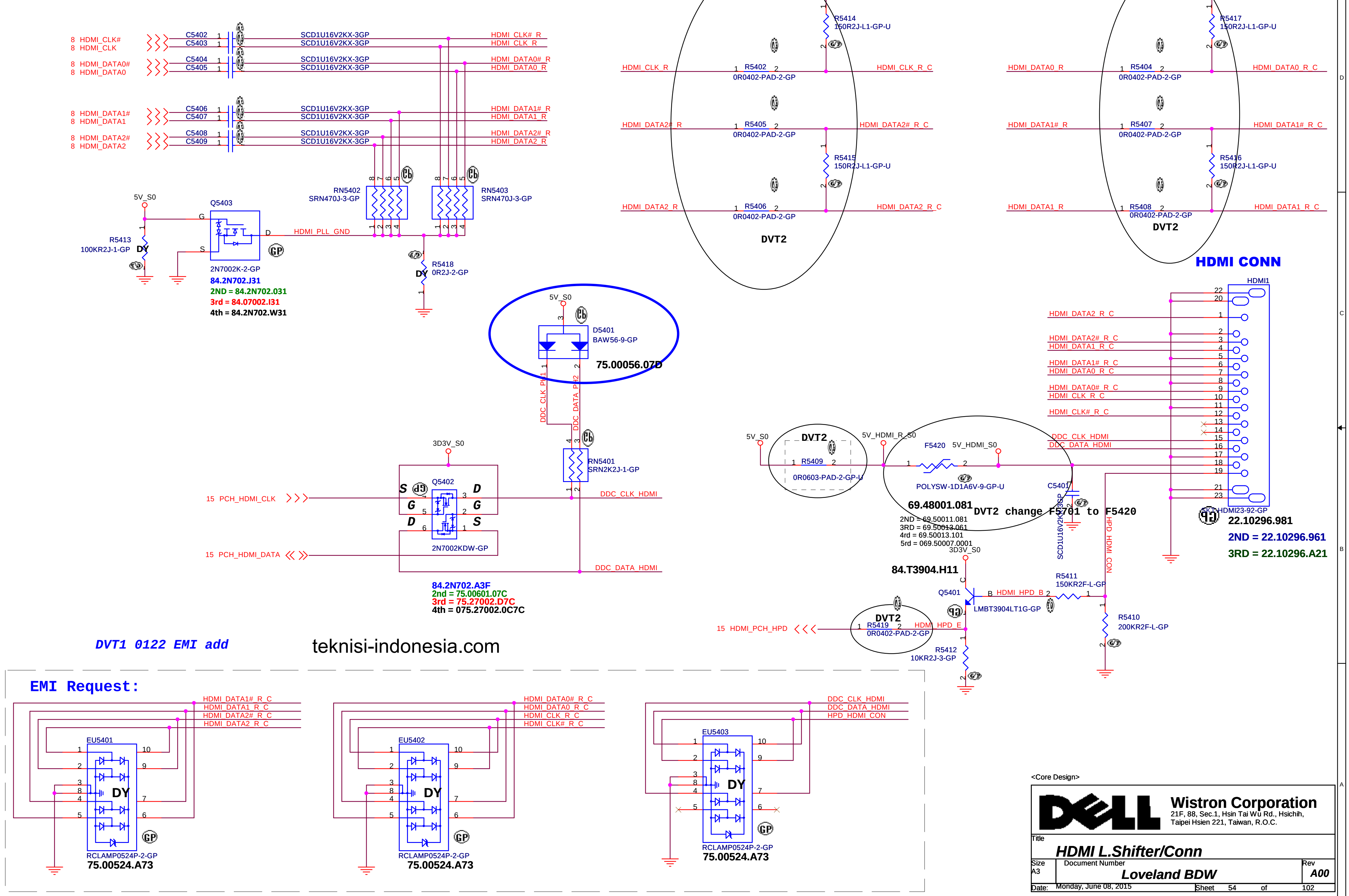
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 53 of 102	

Main Func = HDMI



<Core Design>

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Title	HDMI L.Shifter/Conn	
Size A3	Document Number: Loveland BDW	Rev A00
Date: Monday, June 08, 2015	Sheet 54 of 102	

5 4 3 2 1

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B

A

<Core Design>

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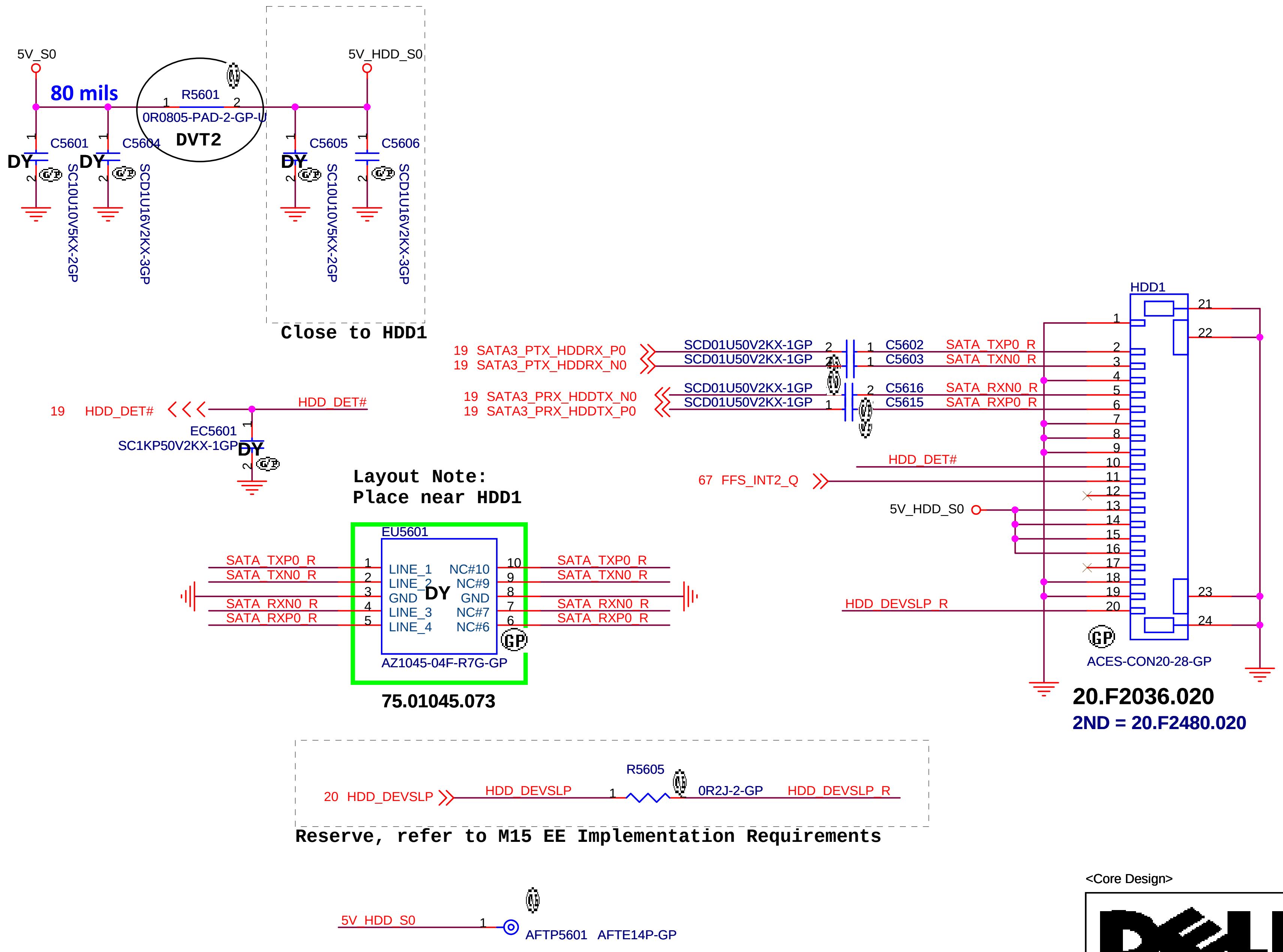
Title		
	(Reserved)	
Size: A4	Document Number: *Loveland BDW*	Rev: *A00*
Date: Wednesday, May 27, 2015	Sheet 55 of 102	

5 4 3 2 1

Main Func = HDD

SATA HDD Connector



<Core Design>

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Title: *HDD/ODD*		
Size: A4	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 56 of 102	

(Blanking)

<Core Design>

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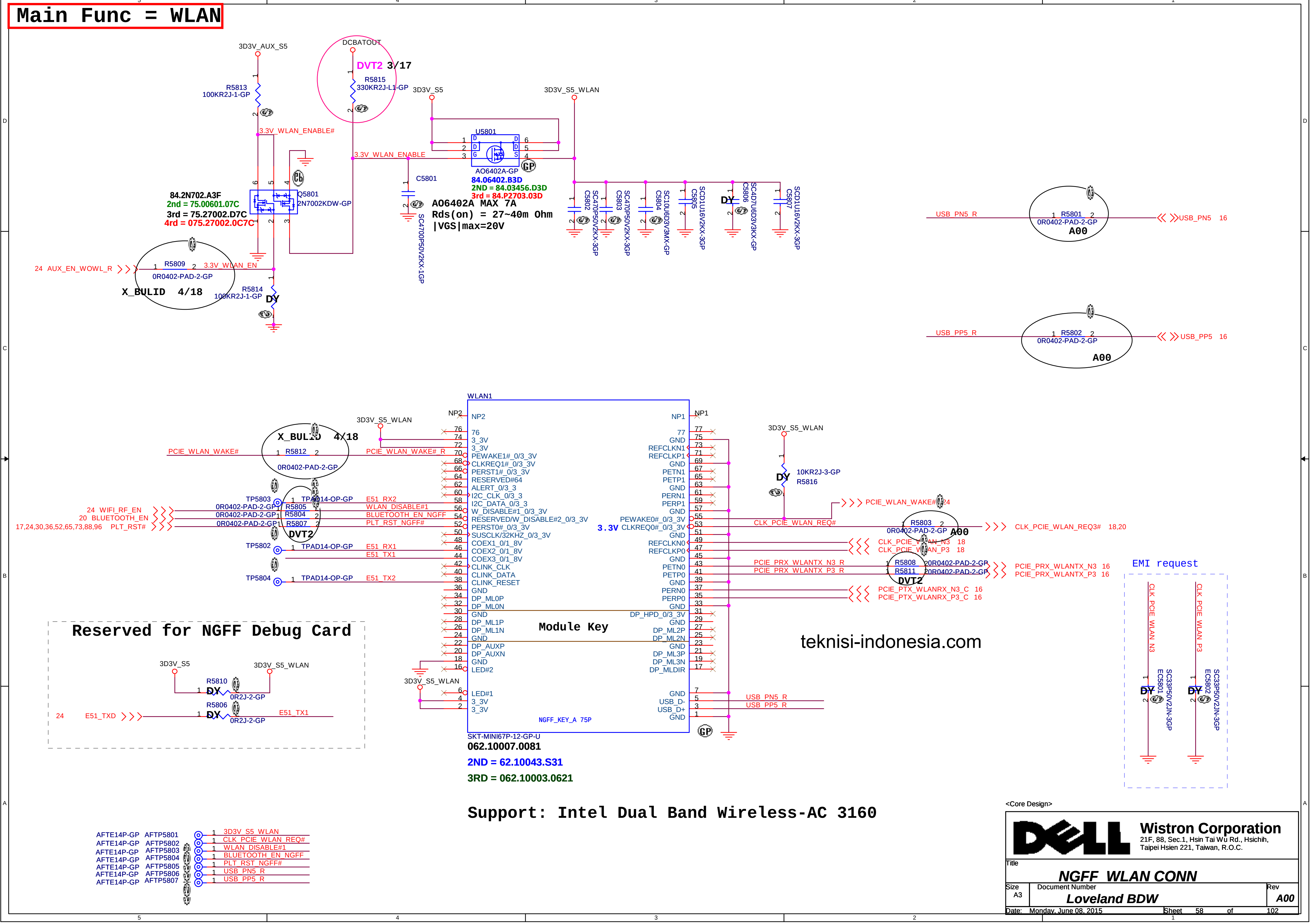
Title	Reserved	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 57 of 102	


Main Func = WLAN
3D3V_AUX_S5
R5813
100KR2J-1-GP
3.3V_WLAN_ENABLE#
DCBATOUT
DVT2 3/17
R5815
330KR2J-L1-GP
3D3V_S5
3D3V_S5_WLAN
U5801
AO6402A-GP
84.06402.B3D
2ND = 84.03456.D3D
3rd = 84.P2703.03D
3.3V_WLAN_ENABLE
C5801
SC4700P50V2KX-1GP
AO6402A MAX 7A
Rds(on) = 27~40m Ohm
|VGS|max=20V
84.2N702.A3F
2nd = 75.00601.07C
3rd = 75.27002.D7C
4rd = 075.27002.0C7C
Q5801
2N7002KDW-GP
C5802 SC470P50V2KX-3GP
C5803 SC470P50V2KX-3GP
C5804 SC10U6D3V3MX-GP
C5805 SCD1U16V2KX-3GP
C5806 SC4D7U6D3V3KX-GP
C5807 SCD1U16V2KX-3GP
DY
24 AUX_EN_WOWL_R
R5809
0R0402-PAD-2-GP
3.3V_WLAN_EN
X_BULID 4/18
R5814
100KR2J-1-GP
USB_PN5_R
R5801
0R0402-PAD-2-GP
A00
USB_PN5 16
USB_PP5_R
R5802
0R0402-PAD-2-GP
A00
USB_PP5 16
WLAN1
NP2
NP1
3D3V_S5_WLAN
X_BULID 4/18
PCIE_WLAN_WAKE#
R5812
0R0402-PAD-2-GP
PCIE_WLAN_WAKE#_R
TP5803
TPAD14-OP-GP
E51_RX2
24 WIFI_RF_EN
20 BLUETOOTH_EN
17,24,30,36,52,65,73,88,96 PLT_RST#
R5805
R5804
R5807
WLAN_DISABLE#1
BLUETOOTH_EN_NGFF
PLT_RST_NGFF#
DVT2
TP5802
E51_RX1
E51_TX1
TP5804
E51_TX2
76 3_3V 3_3V PEWAKE1#_0/3_3V CLKREQ1#_0/3_3V PERST1#_0/3_3V RESERVED#64 ALERT_0/3_3 I2C_CLK_0/3_3 I2C_DATA_0/3_3 W_DISABLE#1_0/3_3V RESERVED/W_DISABLE#2_0/3_3V PERST0#_0/3_3V SUSCLK/32KHZ_0/3_3V COEX1_0/1_8V COEX2_0/1_8V COEX3_0/1_8V CLINK_CLK CLINK_DATA CLINK_RESET GND DP_ML0P DP_ML0N GND DP_ML1P DP_ML1N GND DP_AUXP DP_AUXN GND LED#2 LED#1 3_3V 3_3V
77 GND REFCLKN1 REFCLKP1 GND PETN1 PETP1 GND PERN1 PERP1 GND PEWAKE0#_0/3_3V CLKREQ0#_0/3_3V GND REFCLKN0 REFCLKP0 GND PETN0 PETP0 GND PERN0 PERP0 GND DP_HPD_0/3_3V GND DP_ML2P DP_ML2N GND DP_ML3P DP_ML3N DP_MLDIR GND USB_D- USB_D+ GND
3.3V
Module Key
NGFF_KEY_A 75P
SKT-MINI67P-12-GP-U
062.10007.0081
2ND = 62.10043.S31
3RD = 062.10003.0621
3D3V_S5_WLAN
R5816
10KR2J-3-GP
PCIE_WLAN_WAKE# 24
CLK_PCIE_WLAN_REQ#
R5803
0R0402-PAD-2-GP
A00
CLK_PCIE_WLAN_REQ3# 18,20
CLK_PCIE_WLAN_N3 18
CLK_PCIE_WLAN_P3 18
PCIE_PRX_WLANTX_N3_R
PCIE_PRX_WLANTX_P3_R
R5808
R5811
0R0402-PAD-2-GP
PCIE_PRX_WLANTX_N3 16
PCIE_PRX_WLANTX_P3 16
PCIE_PTX_WLANRX_N3_C 16
PCIE_PTX_WLANRX_P3_C 16
USB_PN5_R
USB_PP5_R
EMI request
CLK_PCIE_WLAN_N3
CLK_PCIE_WLAN_P3
EC5801 SC3P50V2JN-3GP
EC5802 SC3P50V2JN-3GP
teknisi-indonesia.com
Reserved for NGFF Debug Card
3D3V_S5
3D3V_S5_WLAN
R5810
0R2J-2-GP
R5806
0R2J-2-GP
24 E51_TXD
E51_TX1
Support: Intel Dual Band Wireless-AC 3160
AFTE14P-GP AFTP5801 3D3V_S5_WLAN
AFTE14P-GP AFTP5802 CLK_PCIE_WLAN_REQ#
AFTE14P-GP AFTP5803 WLAN_DISABLE#1
AFTE14P-GP AFTP5804 BLUETOOTH_EN_NGFF
AFTE14P-GP AFTP5805 PLT_RST_NGFF#
AFTE14P-GP AFTP5806 USB_PN5_R
AFTE14P-GP AFTP5807 USB_PP5_R
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
NGFF_WLAN CONN
Size A3
Document Number
Loveland BDW
Rev A00
Date: Monday, June 08, 2015
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A B C D E

4 4

3 3

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2 2

1 1

<Core Design>

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Title	***Reserved***	
Size A4	Document Number ***Loveland BDW***	Rev ***A00***
Date: Wednesday, May 27, 2015	Sheet 59 of 102	

A B C D E

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<Core Design>

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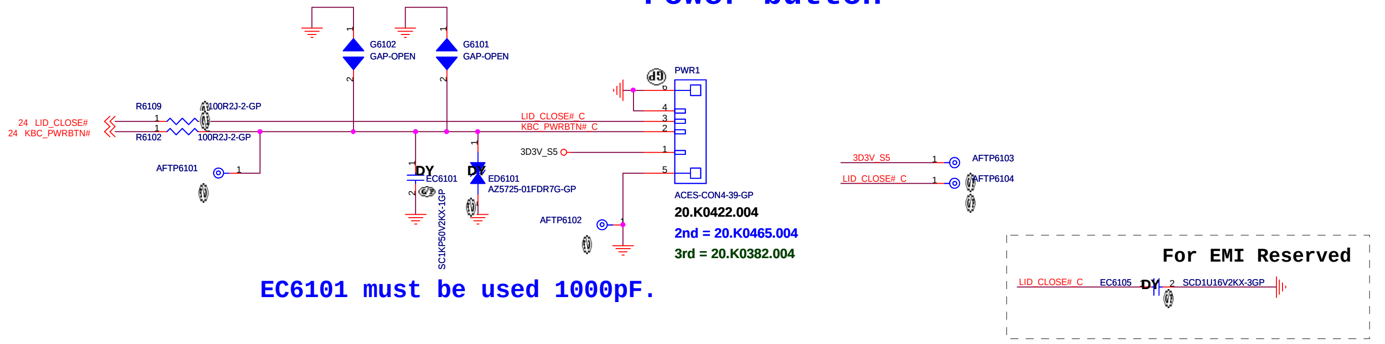
Title	*(Reserved)*	
Size A4	Document Number *Loveland BDW*	Rev *A00*
Date: Wednesday, May 27, 2015	Sheet 60 of 102	

Main Func = Power BTN

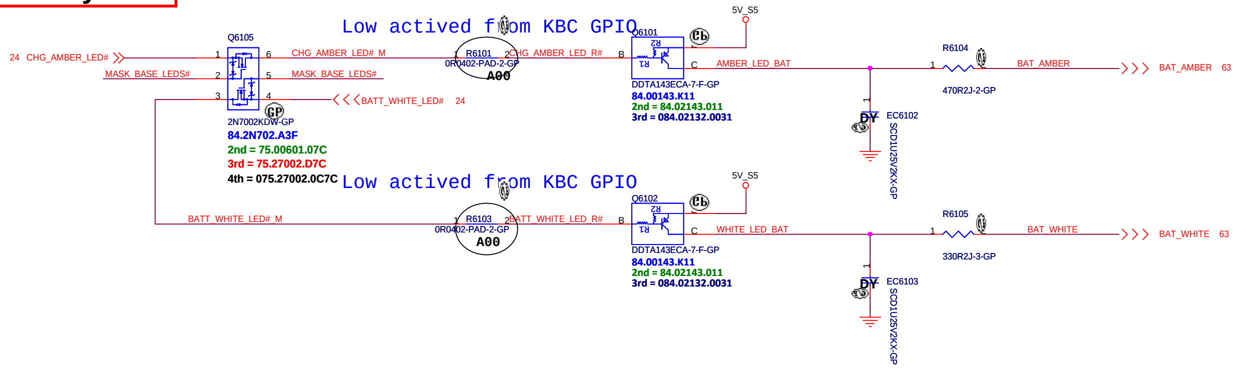
Power button



EC6101 must be used 1000pF.

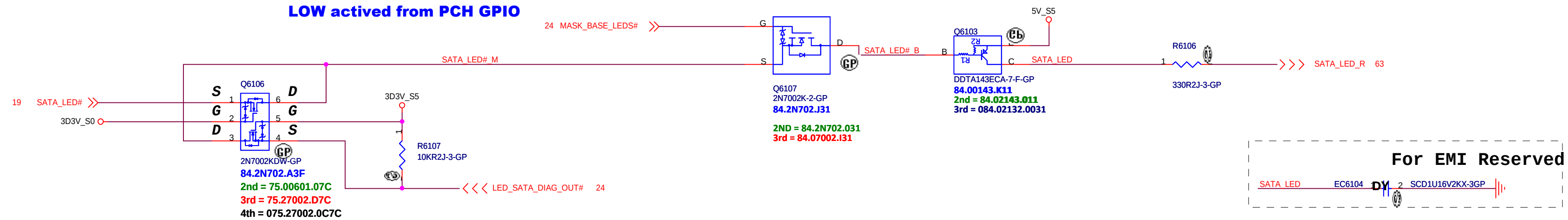
Main Func = Battery LED

Low actived from KBC GPIO

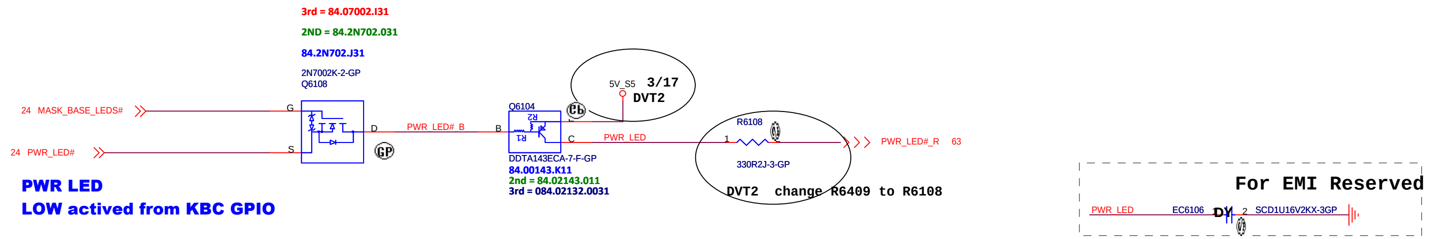


Main Func = HDD LED

SATA HDD LED
LOW actived from PCH GPIO



Main Func = PWR LED



PWR LED
LOW actived from KBC GPIO

<Core Design>

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Title	LED Bard/Power Button	
Size C	Document Number Loveland BDW	Rev A00
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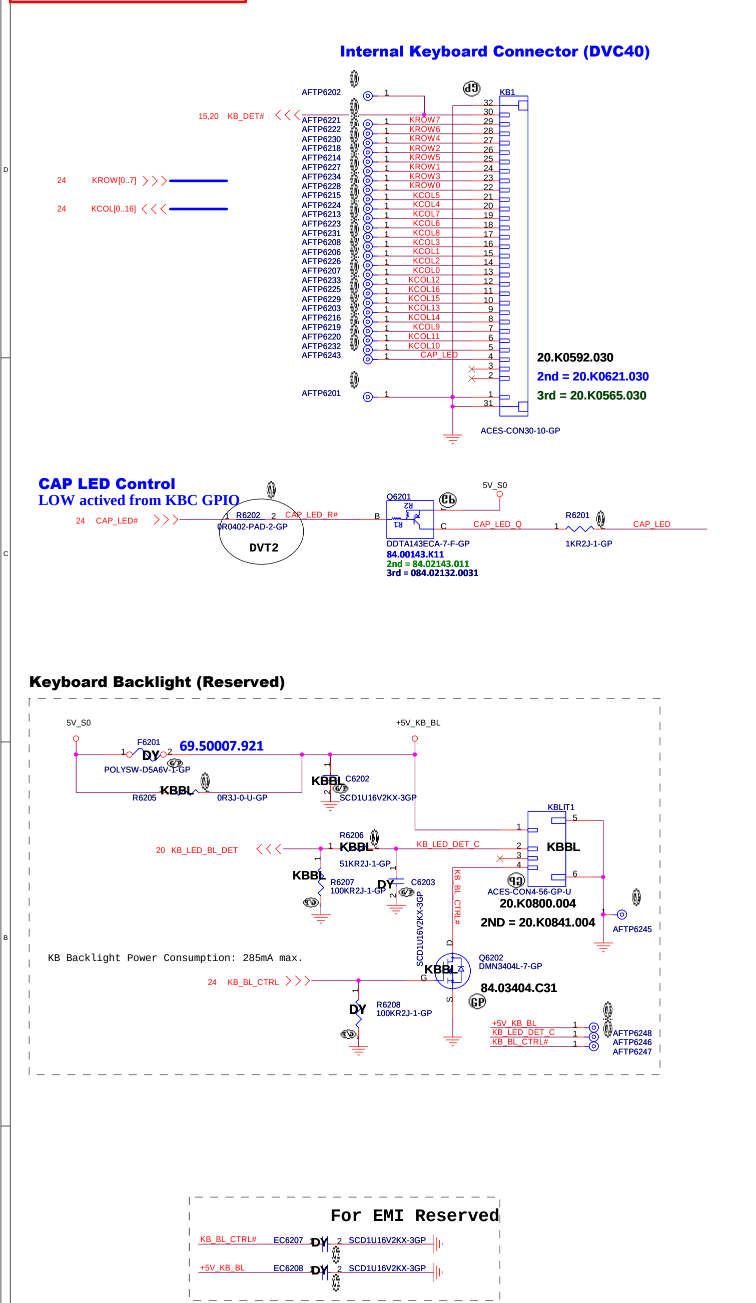
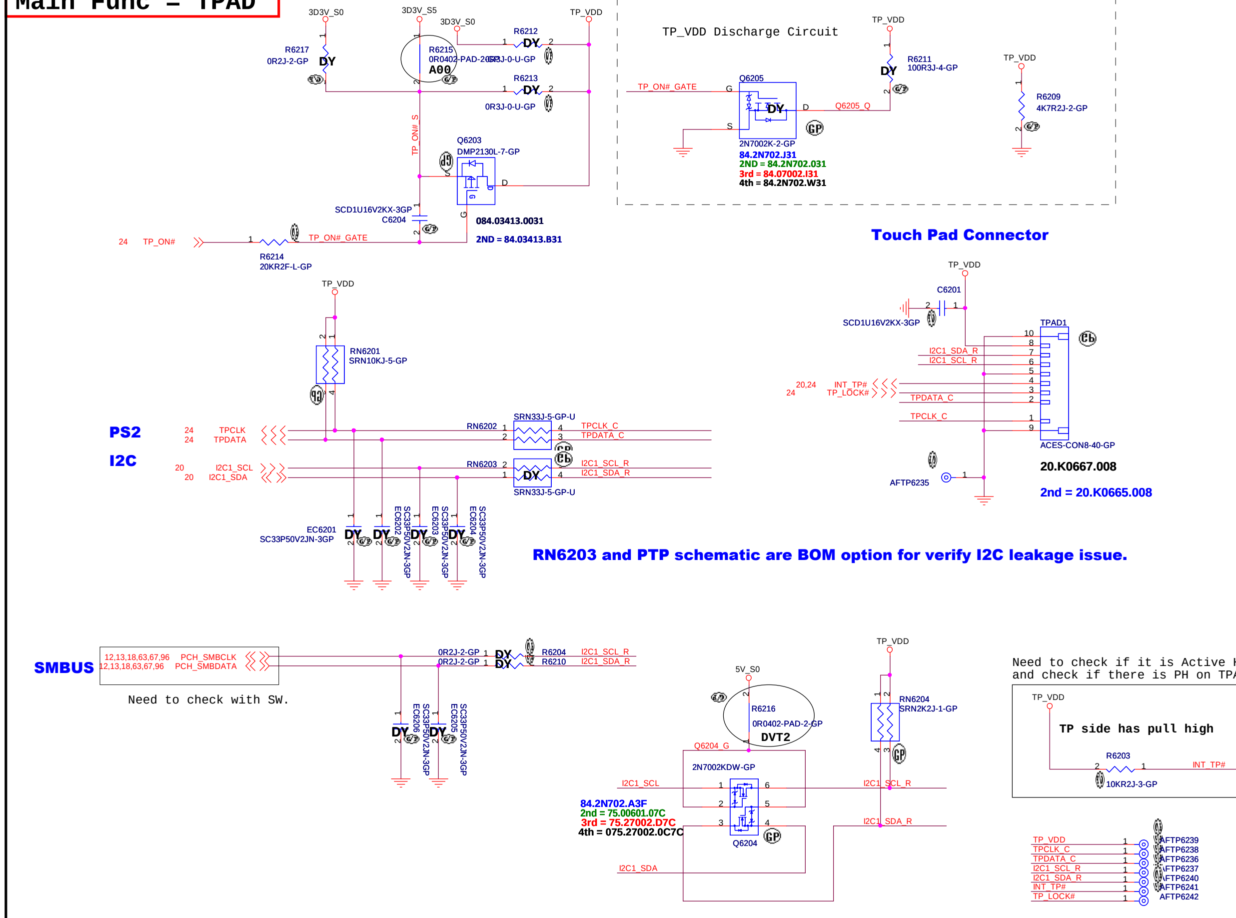
Main Func = KB



Main Func = TPAD



Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)

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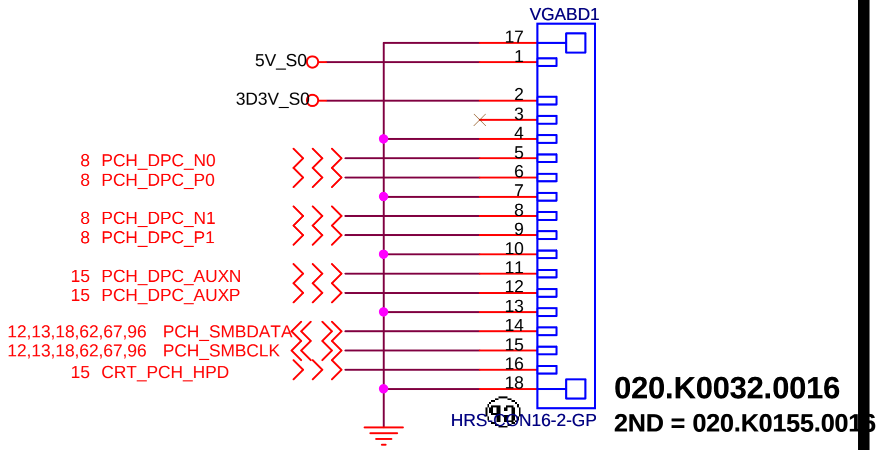
Title: Keyboard/Touch Pad

Size: A2 | Document Number: Loveland BDW | Rev: A00

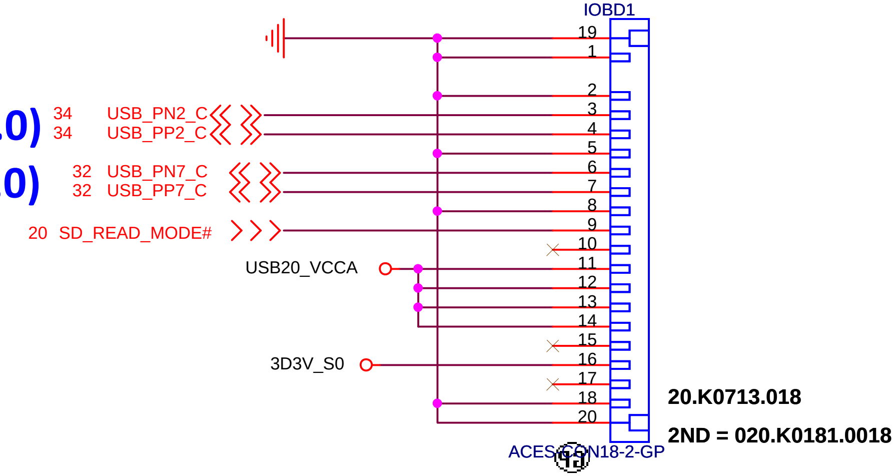
Date: Monday, June 08, 2015 | Sheet 62 of 102

Main Func = IO/VGA/LED Connector

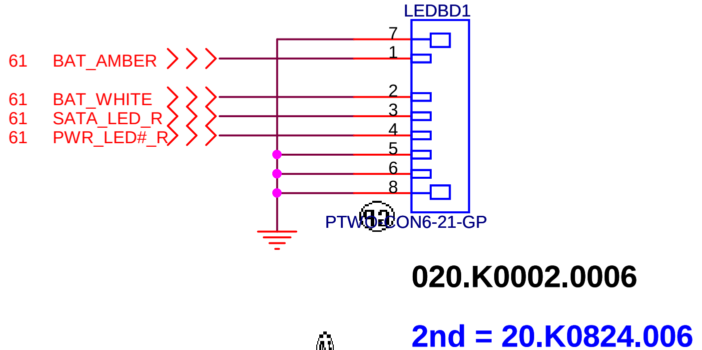
VGA Connector

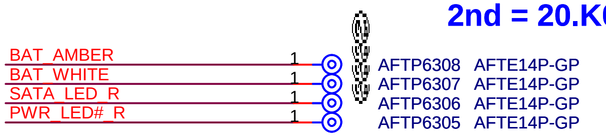


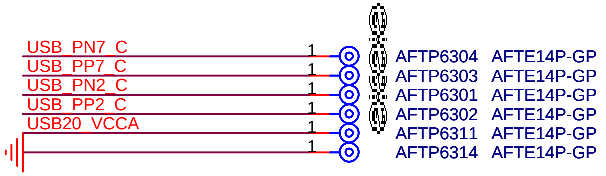
I/O Board Connector



LED Connector







Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins

<Core Design>

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Title: *IO Board Connector*		
Size: A4	Document Number: Loveland BDW	Rev: A00
Date: Monday, June 08, 2015	Sheet 63 of 102	

Main Func = Hall Sensor

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<Core Design>

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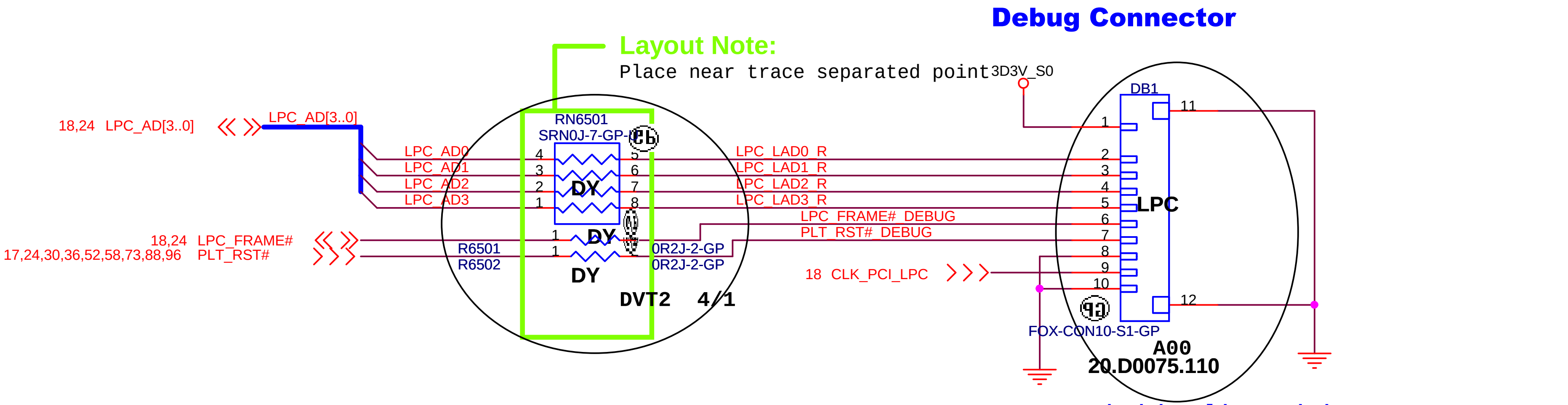
Title	reserved	
Size A4	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 64 of 102	

Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

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Title	*Dubug connector*	
Size: A4	Document Number: *Loveland BDW*	Rev: *A00*
Date: Wednesday, May 27, 2015	Sheet 65 of 102	

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<Core Design>

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Title		
Reserved		
Size: A4	Document Number: Loveland BDW	Rev: A00
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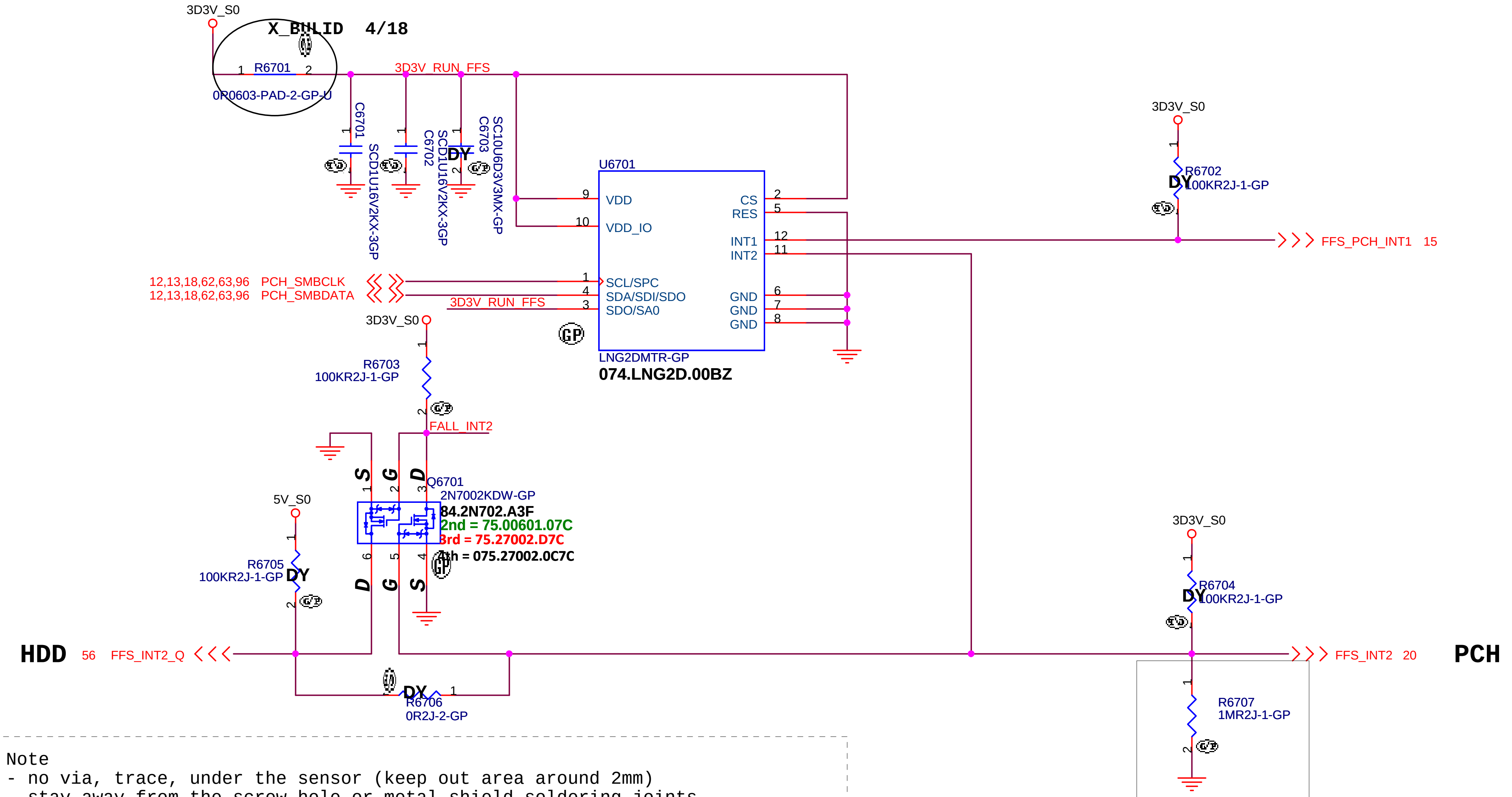
SSID = FFS

Free Fall Sensor



2014.04.24 Venrer suggest,reserve to prevent error trigger

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title		
	Free Fall Sensor	
Size A4	Document Number *Loveland BDW*	Rev *A00*
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<Core Design>

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RESERVED***	
Size A4	Document Number ***Loveland BDW***	Rev ***A00***
Date: Wednesday, May 27, 2015	Sheet 68 of 102	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 PORT	
Size A4	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 69 of 102	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 70 of 102	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
	Reserved	
Size: A3	Document Number: Loveland BDW	Rev: A00
Date: Wednesday, May 27, 2015	Sheet 71 of 102	

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<Core Design>

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Title	Reserved	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 72 of 102	

Main Func = dGPU

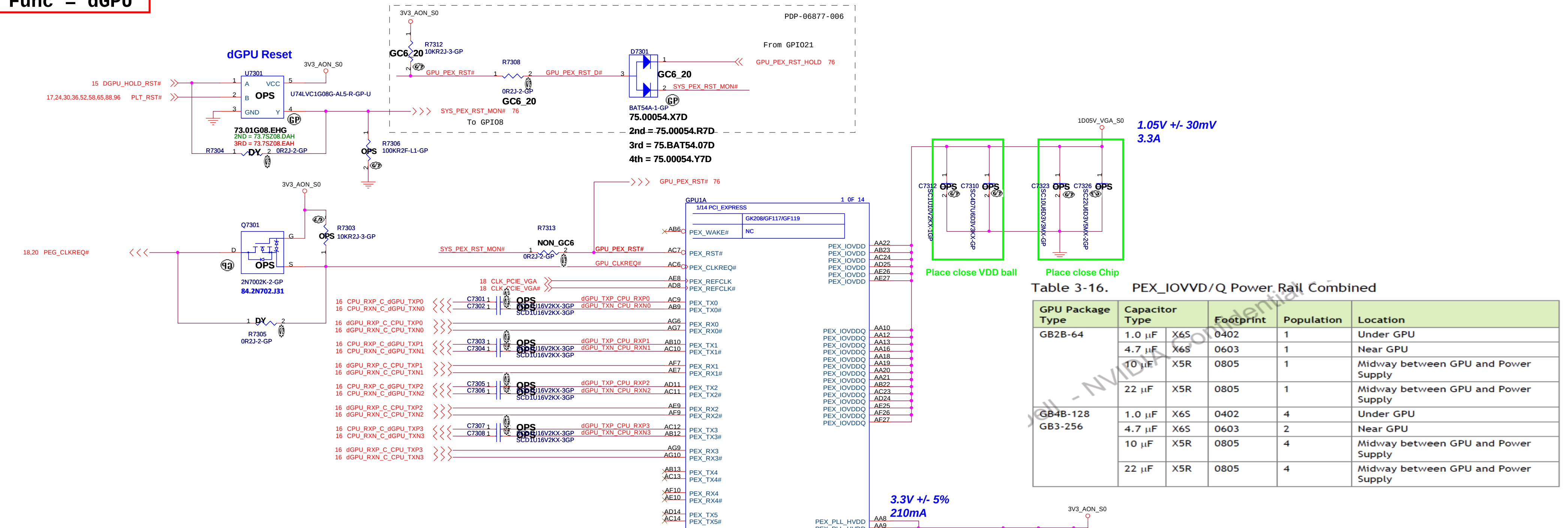
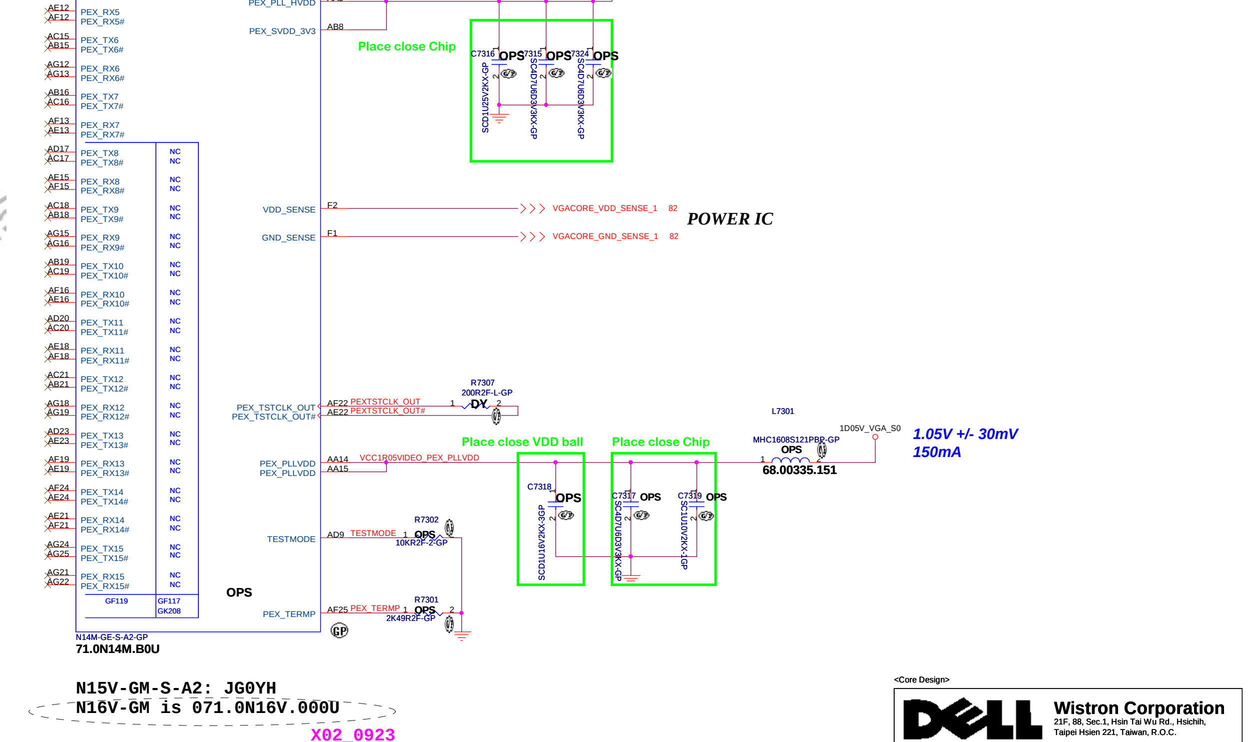


Table 3-16. PEX_IOVVD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 µF	X6S	0402	4	Under GPU
	4.7 µF	X6S	0603	2	Near GPU
	10 µF	X5R	0805	4	Midway between GPU and Power Supply
	22 µF	X5R	0805	4	Midway between GPU and Power Supply



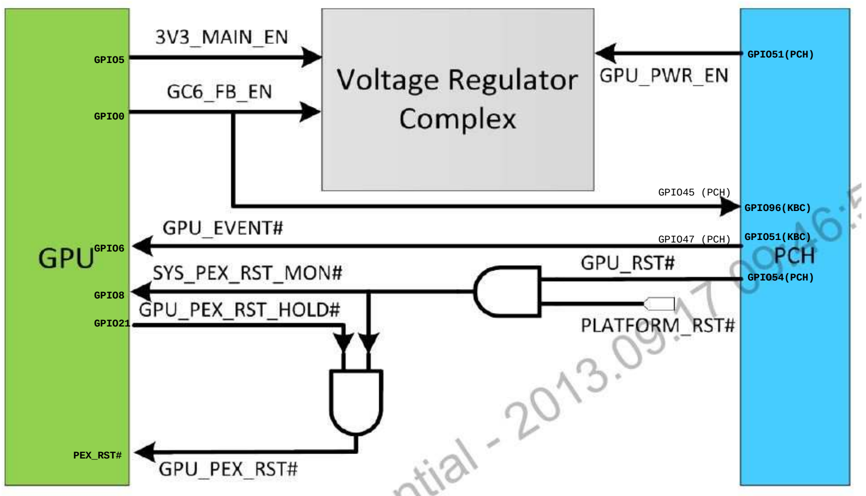
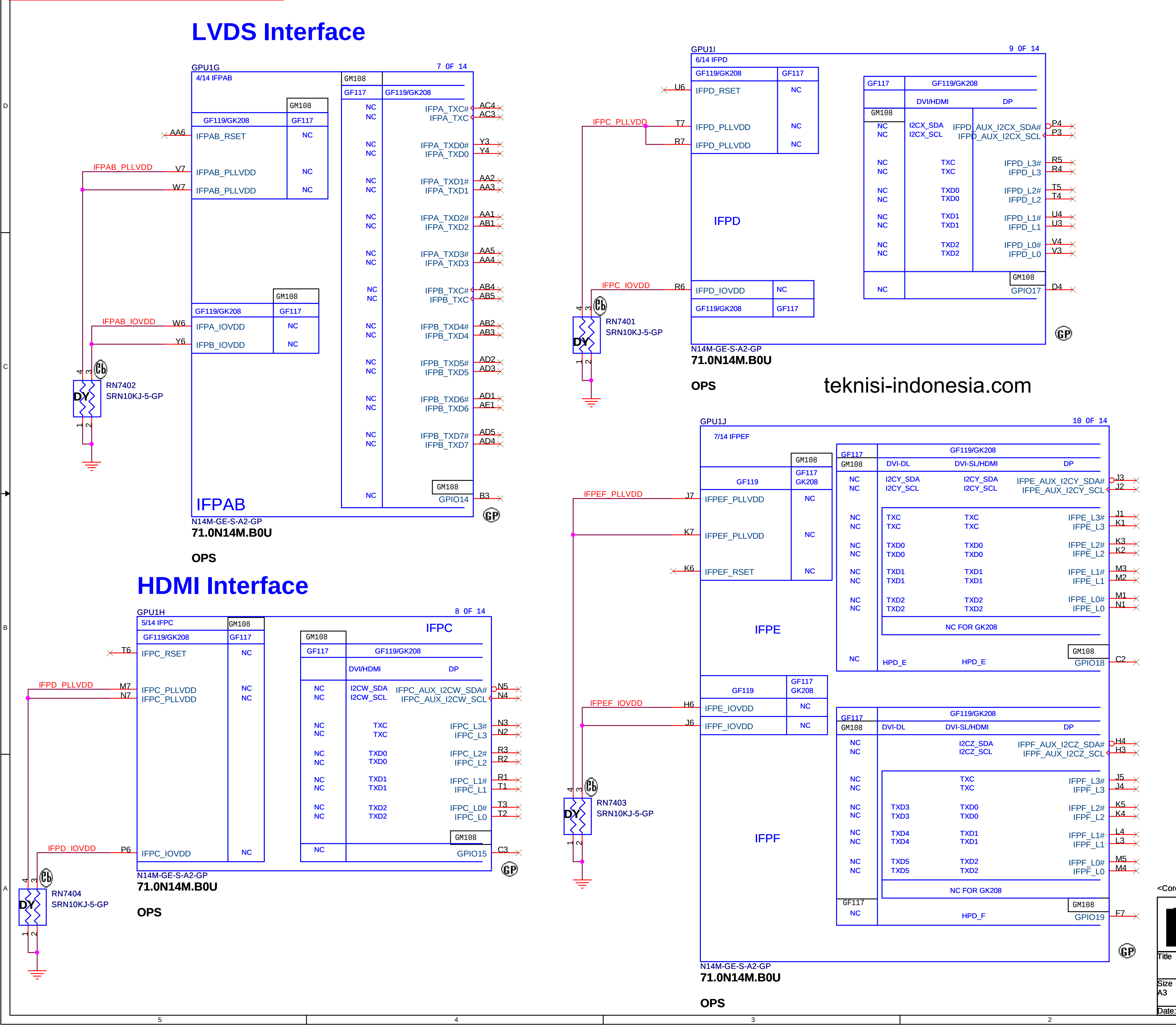


Figure 18-11. GC6 2.0 High-level Signal Connection Concept

Main Func = dGPU



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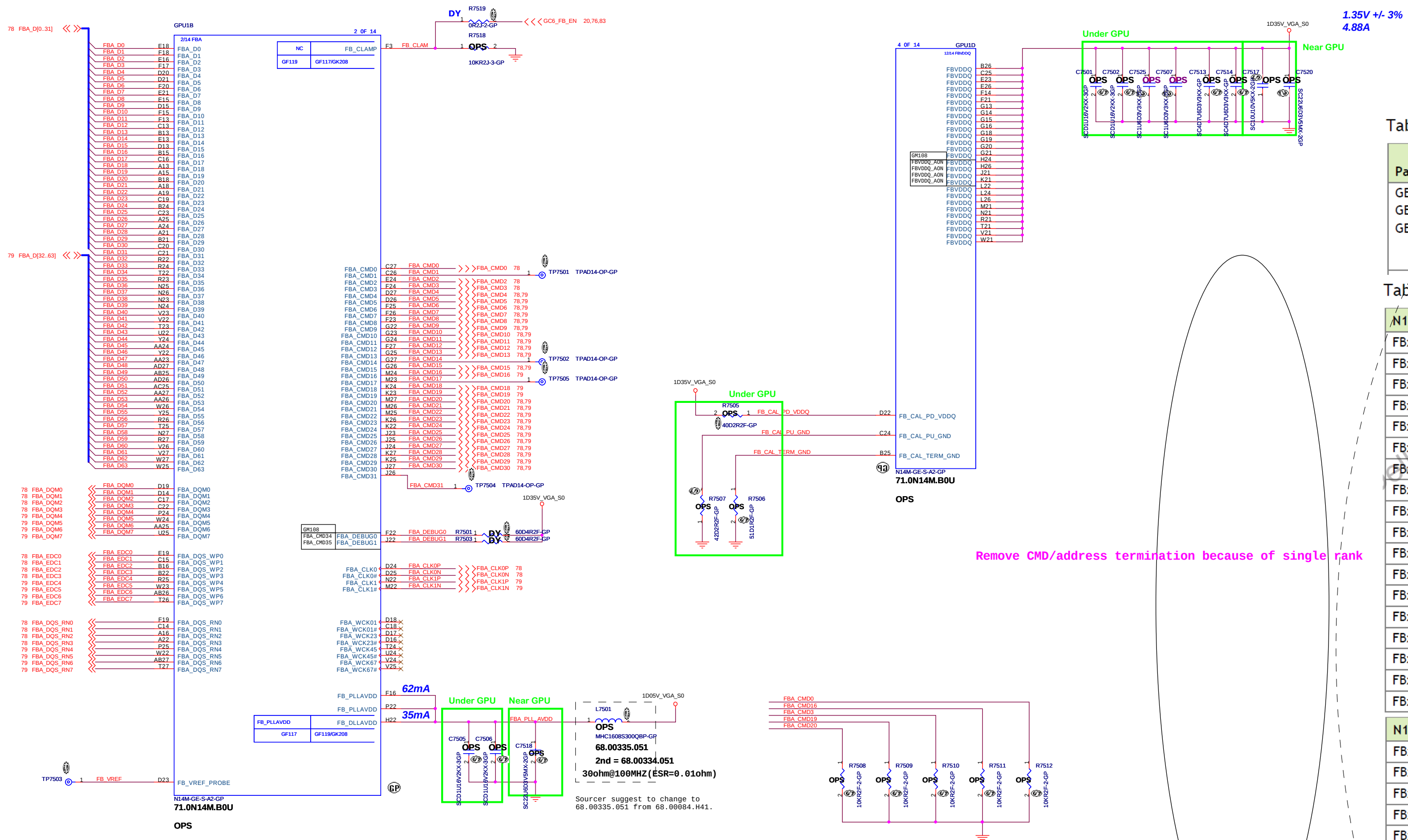
Title	GPU(2/5)DIGITALOUT	
Size A3	Document Number Loveland BDW	Rev A00
Date: Wednesday, May 27, 2015	Sheet 74 of 102	

Main Func = dGPU



N16x single rank SPEC

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2-64 GB2B-64 GB4B-128	D	Mode D is optimized for N16x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1 μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU
GB4B-128 DDR3	0.1 μF	X7R	0402	4	4	Under GPU
	1 μF	X7R	0603	4	4	Under GPU
	4.7 μF	X6S	0603	4	4	Under GPU
	10 μF	X5R	0805	2	2	Near GPU
	22 μF	X5R	0805	2	2	Near GPU

Notes:
1. The decoupling in this table applies to both single rank and dual rank designs.
2. If a single partition 64-bit GPU in the GB4B-128 package is used, populate only half of the recommended number of decoupling capacitors of GB4B-128.

Table 3-9. DDR3 GPU-side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1 μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

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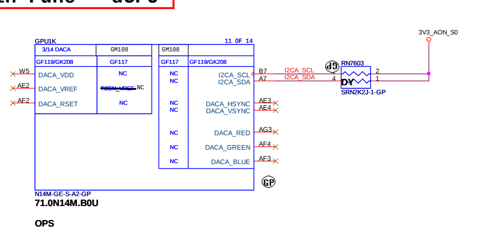
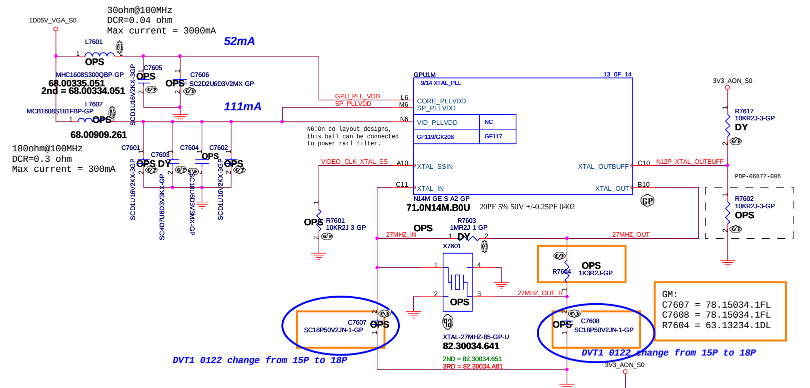
Title	GPU(3/5)VRAMI/F
Size A1	Document Number: Loveland BDW — Rev A00
Date: Wednesday, May 27, 2015	Sheet 75 of 102

Main Func = dGPU





Straps

(DS-06814-001)

Table 9. N15V-GM Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10kΩ	Pull-down to GND
ROM_SI	SUB_VENDOR	10kΩ	• Pull-up to 3V3 if VBIOS ROM exists • Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10kΩ	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10kΩ	See note below
STRAP1	RAM_CFG[1]	10kΩ	See note below
STRAP2	RAM_CFG[2]	10kΩ	See note below
STRAP3	RAM_CFG[3]	10kΩ	See note below
STRAP4	PCIE_MAX_SPEED	10kΩ	Pull-down to GND

(RVL-06891-001)N15V-GM-S DDR3L Recommended Memories

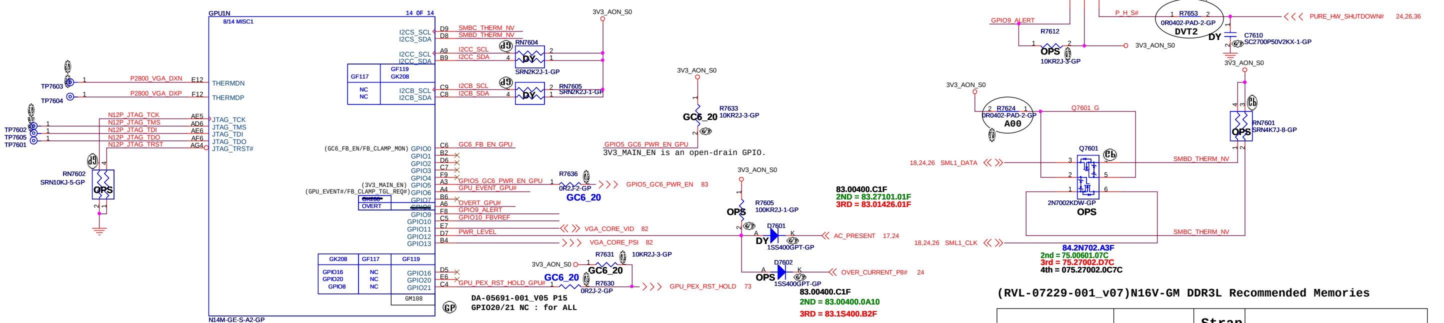
		Strap		STRAP3	STRAP2	STRAP1	STRAP0
128Mx16 DDR3L	Hynix	0xC	H5TC2G63FFR-11C	1	1	0	0
	Micron	0x1	MT41K128M16JT-107G:K	0	0	0	1
	Samsung	0x5	K4W2G1646E-BY11	0	1	0	1
256Mx16 DDR3L	Hynix	0x4	H5TC4G63AFR-11C	0	1	0	0
	Micron	0xD	MT41K256M16HA-107G:E	1	1	0	1
	Samsung	0x9	K4W4G1646D-BC1A	1	0	0	1

Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05)		0402	1	Near GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

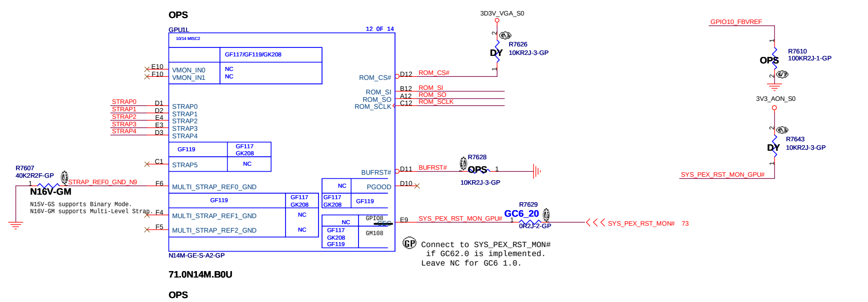
GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	SP_PLLVDD + VID_PLLVDD	0.1 µF	X7R	0402	1 per ball	Under GPU
		4.7 µF	X5R	0603	1	Near GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		180 Ω (ESR=0.2)		0603	1	Near GPU



(DG-07158-001)

Table 15-4 GB2-64 Multi-Level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V



(RVL-07229-001_v07)N16V-GM DDR3L Recommended Memories

		Strap	
128Mx16 DDR3L	Hynix	0xB	H5TC2G63FFR-11C
	Micron	0x8	MT41J128M16JT-093G:K
	Samsung	0x7	K4W2G1646Q-BC1A
256Mx16 DDR3L (4 pcs VRAM)	Hynix	0xE	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0x5	K4W4G1646D-BC1A
256Mx16 DDR3L (8 pcs VRAM)	Hynix	0xE	H5TC4G63AFR-11C
	Micron	0xD	MT41J256M16HA-093G:E
	Samsung	0xC	K4W4G1646D-BC1A

Table 15-2. Resistance Mapping to Hex Values

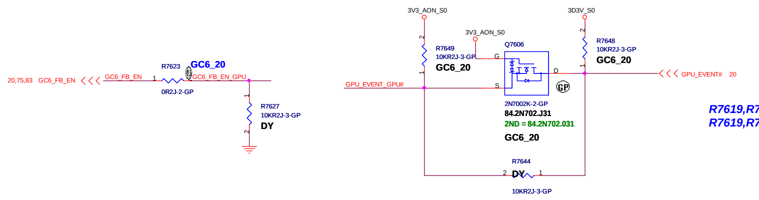
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

NPN-06912

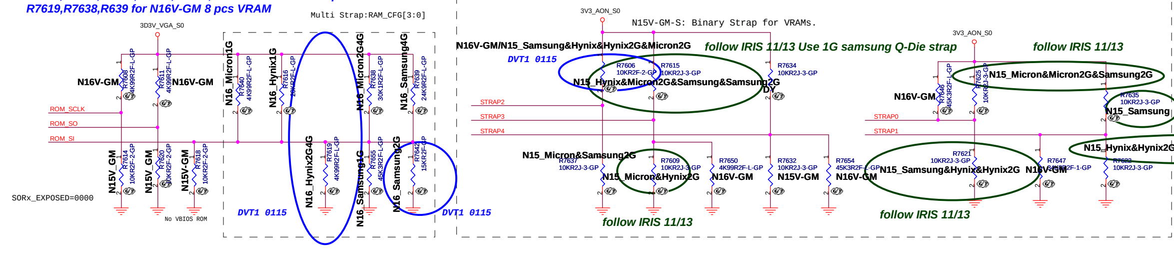
	N15V-GM
Chip	N15V-GM
Device ID	0x1140
Memory interface	sDDR3
Package	595 ball BGA 23x23mm

NPN-07376

	N16V-GM
Chip	GK208-620-B1
Device ID	0x1299
Core clock (MHz)	Variable
Memory interface	64b DDR3
Core voltage (NVVDD)	Variable
Package	GB2-64 (23 mm × 23 mm 595 balls)



R7619,R7638,R7642,R7616,R7640,R7655 for N16V-GM 4 pcs VRAM
R7619,R7638,R639 for N16V-GM 8 pcs VRAM



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Title: GPU(4/5)GPIO/STRAP
Size: Custom | Document Number: Loveland BDW | Rev: A00
Date: Monday, June 08, 2015 | Sheet 76 of 102

Main Func = dGPU

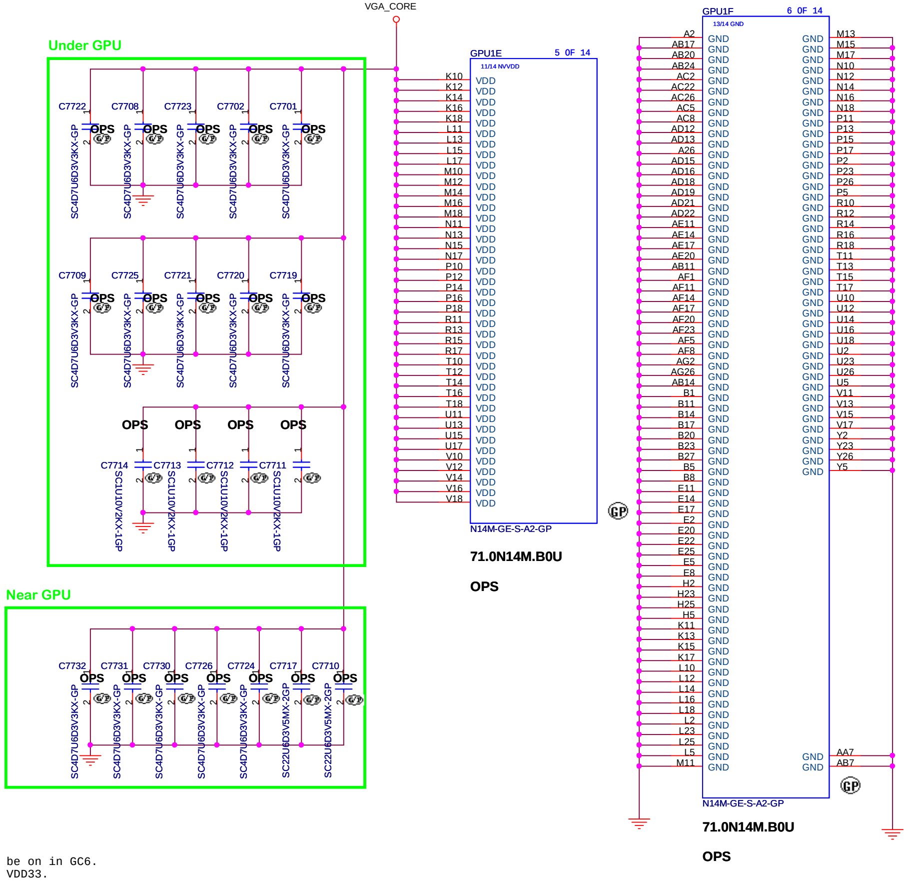
Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

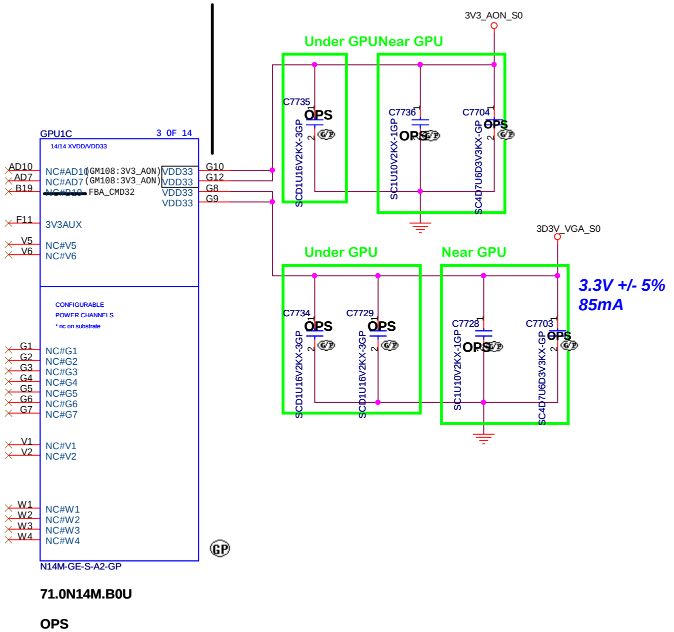
Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.



G10,G12:
If GC62.0 is implemented, connect to a 3V3 rail that will be on in GC6.
If GC62.0 is NOT implemented, connect to the same rail as VDD33.



teknisi-indonesia.com

1GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	2Gb DDR3L:(1.35v/900Mhz)	DPN	WPN	Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5TC2G63FFR-11C	X1PRC	72.52G63.N0U	1.35V	
		Samsung	K4W2G1646Q-BC1A	D0DP7	072.2G164.0A0U	1.35V	
		Micron	MT41K128M16JT-107G:K	HKKF2	72.41128.N0U	1.35V	

2GB, Single Rank, 4 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15V-GM-S-A2 GB2-64 FCBGA595P	JG0YH	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41K256M16HA-107G:E	R5RH5	72.41K26.00U	1.35V	Build in EVT

4GB, Dual Rank, 8 pcs VRAM							
GPU	GPU DPN	Memory Vendor	4Gb DDR3L:(1.35v/900Mhz)	DPN		Voltage	Note
IC VGA N15S-GT-S-A2 GB2-64 FCBGA595	PXP79	Hynix	H5TC4G63AFR-11C	021N2	72.05463.D0U	1.35V	Build in EVT
		Samsung	K4W4G1646D-BC1A	07XGT	072.4G164.0A0U	1.35V	
		Micron	MT41J256M16HA-093G:E	PP8TP	072.41256.0B0U	1.35V	

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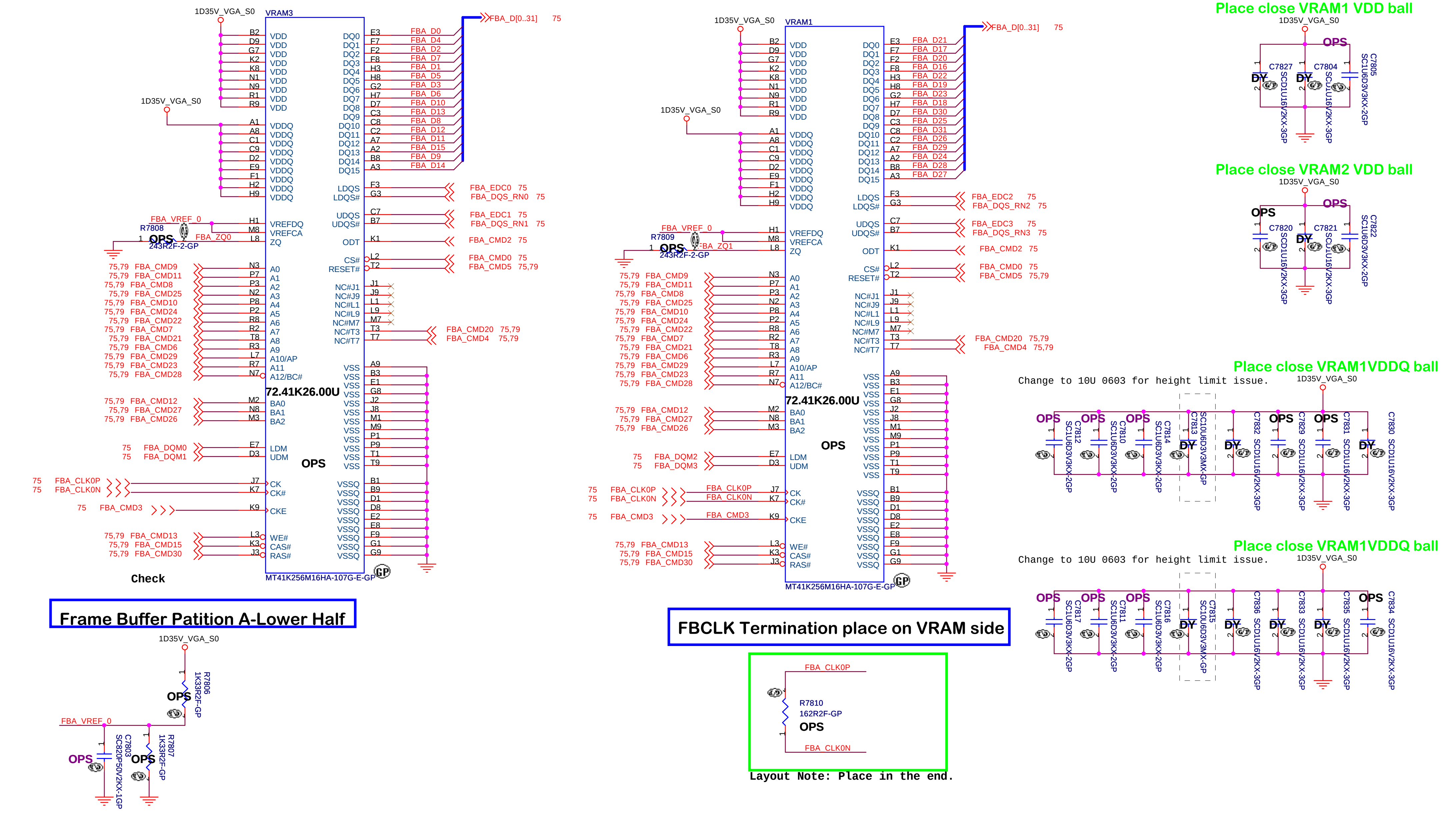

FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

20110613

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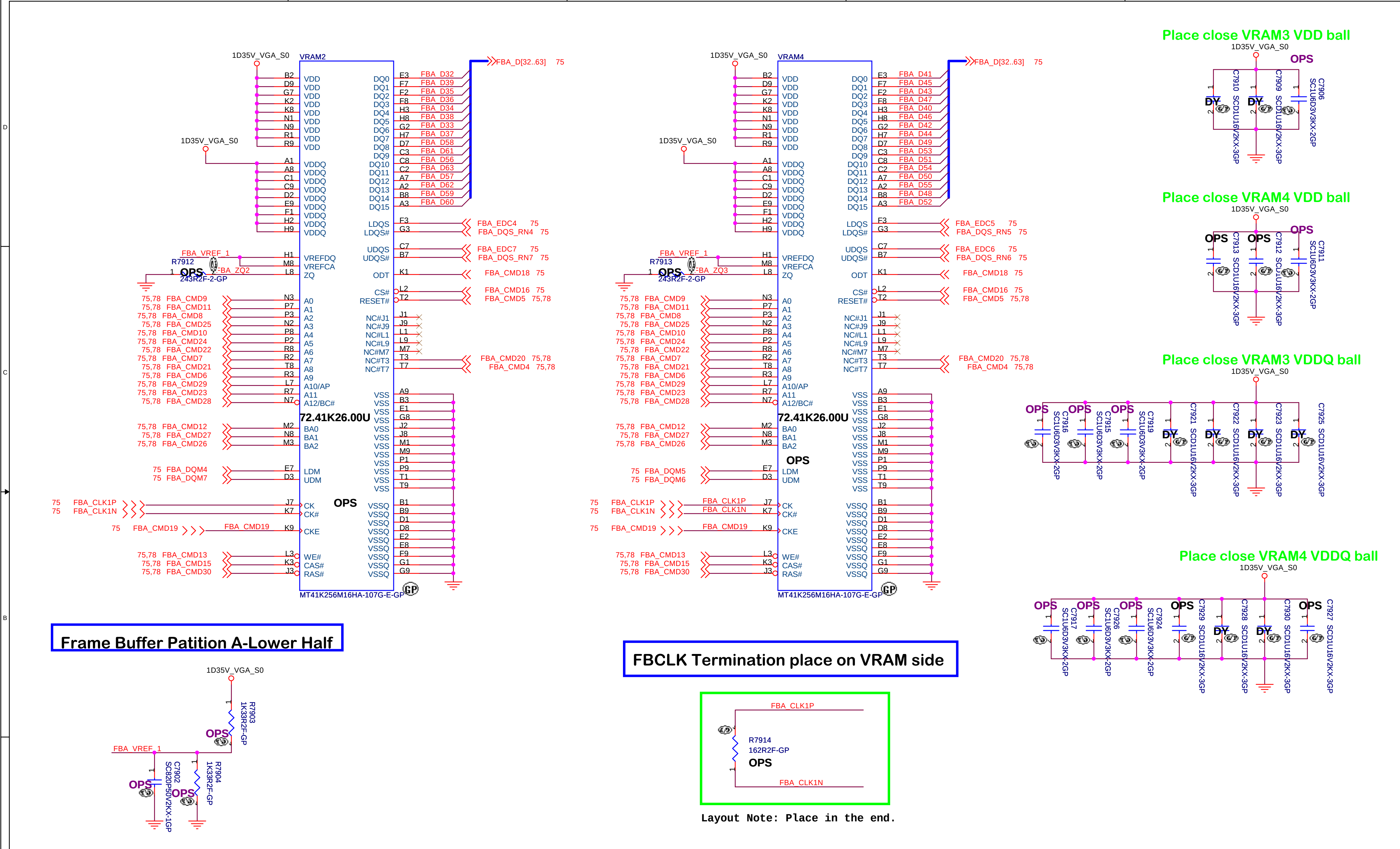
Title: GPU-VRAM1,2 (1/4)

Size: A3 | Document Number: Loveland BDW | Rev: A00

Date: Wednesday, May 27, 2015 | Sheet 78 of 102



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Title
GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	Loveland BDW	A00

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5 4 3 2 1

D D

(Blanking)

C C

B B

A A

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Title	***GPU-VRAM5,6 (3/4)***
Size A4	Document Number **Loveland BDW**	Rev **A00**
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5 4 3 2 1

5 4 3 2 1

D D

C C

B B

A A

<Core Design>

DELL

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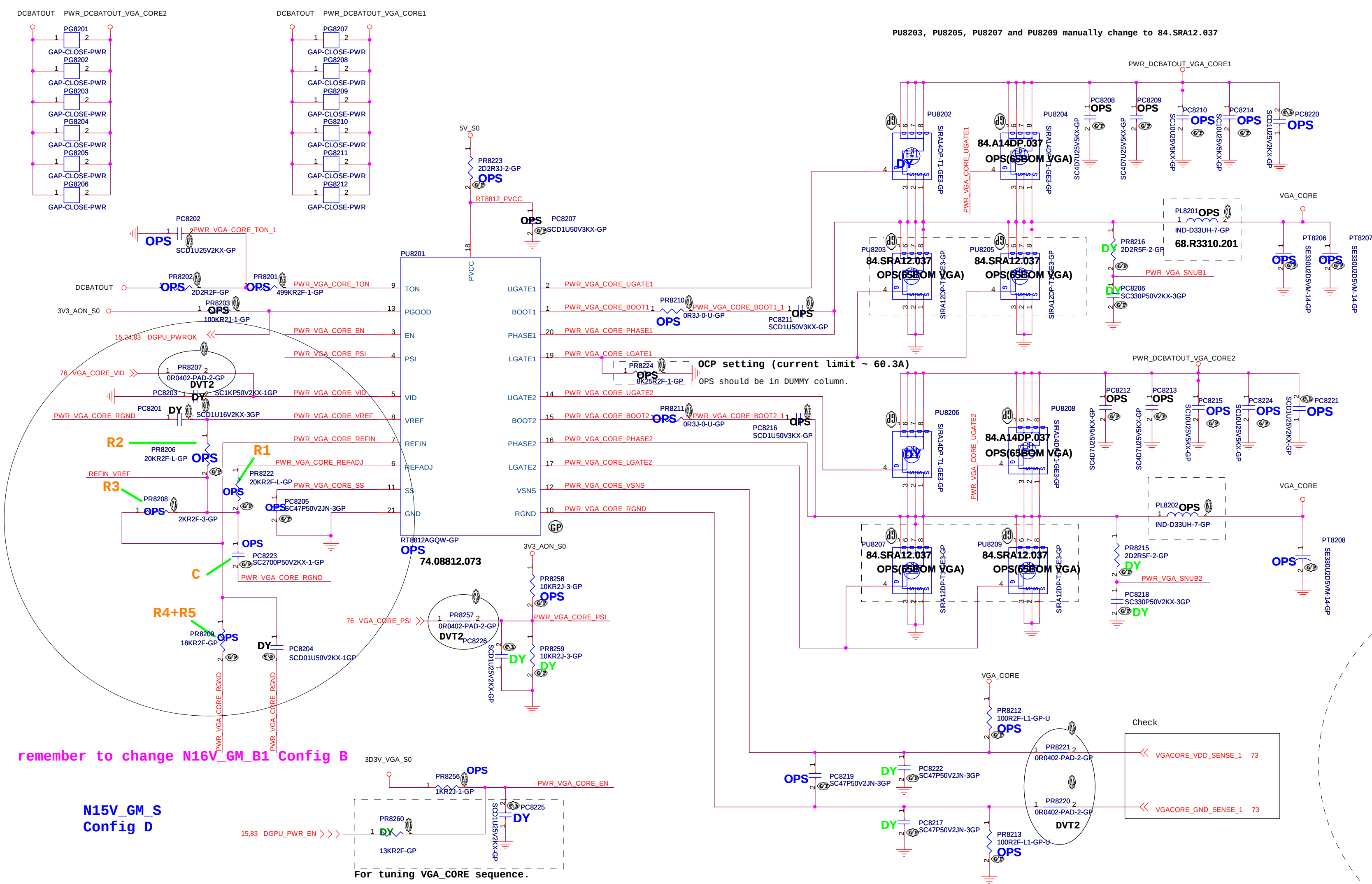
Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A3	**Loveland BDW**	**A00**

5 4 3 2 1

Main Func = dGFX_CORE



N15V_GM_S
Config D

Design Current=33.5A
56.65A <OCP< 66.7A

Component value	N15V-GM-S Config D	N16V-GM-B1 Config B
R1 (PR8222)	27K 64.27025.6DL	20K 64.20025.6DL
R2 (PR8206)	7.5K 64.75015.6DL	20K 64.20025.6DL
R3 (PR8208)	0 63.R0034.1DL	2K 64.20015.6DL
R4+R5 (PR8209)	7.87K 64.78715.6DL	18K 64.18025.6DL
C (PC8223)	5.6nF 78.56222.2FL	2.7nF 78.27224.2FL

78.56222.2FL:OBS REASON: 50V is more popular, chage to 78.56224.2FL

N16V_GM_B1
Config B

Table 1. PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B
Vmin	V	0.6	0.6
Vmax	V	1.2	1.2
Vboot	V	0.875	0.9
Voltage Step Vstep	mV	6.25	6.25
Number of Voltage Levels N	level	96	96
PWM Frequency F_{PWM}	MHz	1.125	1.125
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26
VID Transient Time T	us	<100	<100
Component Value			
R1 (1%)	KΩ	39	20
R2 (1%)	KΩ	39	20
R3 (1%)	KΩ	1.5	2
R4 (1%)	KΩ	30	18
R5 (1%)	KΩ	1.5	0
C	nF	1.5	2.7

X02_0922

PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 0.22UH PCMC104T-R22/ 1mohm/ Isat =60A rms /68.R2210.10C
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 Chemi-con/79.3371V.6CL
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S:SIRA06DP-T1-GE3 / 2.75mohm/3.5mOhm@4.5Vgs/ 84.SRA06.037

<Core Design>

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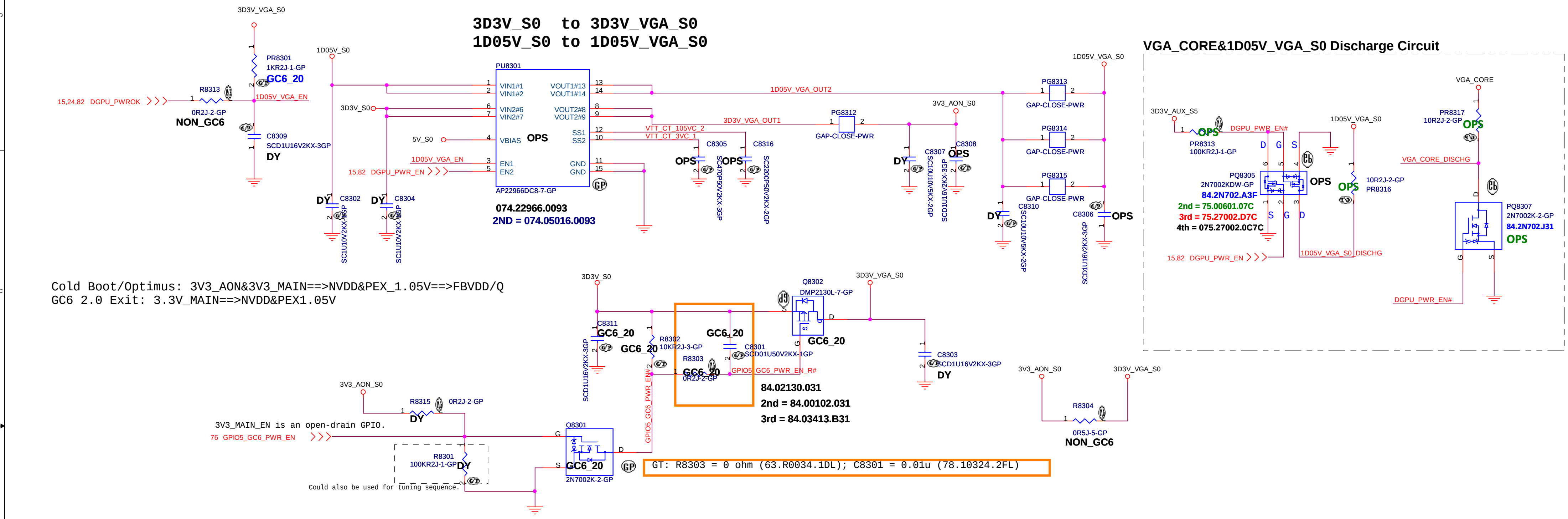
Title: RT8812_VGACORE
Size: A2 | Document Number: Loveland BDW | Rev: A00
Date: Wednesday, May 27, 2015 | Sheet 82 of 102

Main Func = dGPU

3D3V_VGA_S0
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



Cold Boot/Optimus: 3V3_AON&3V3_MAIN==>NVDD&PEX_1.05V==>FBVDD/Q
GC6 2.0 Exit: 3.3V_MAIN==>NVDD&PEX1.05V

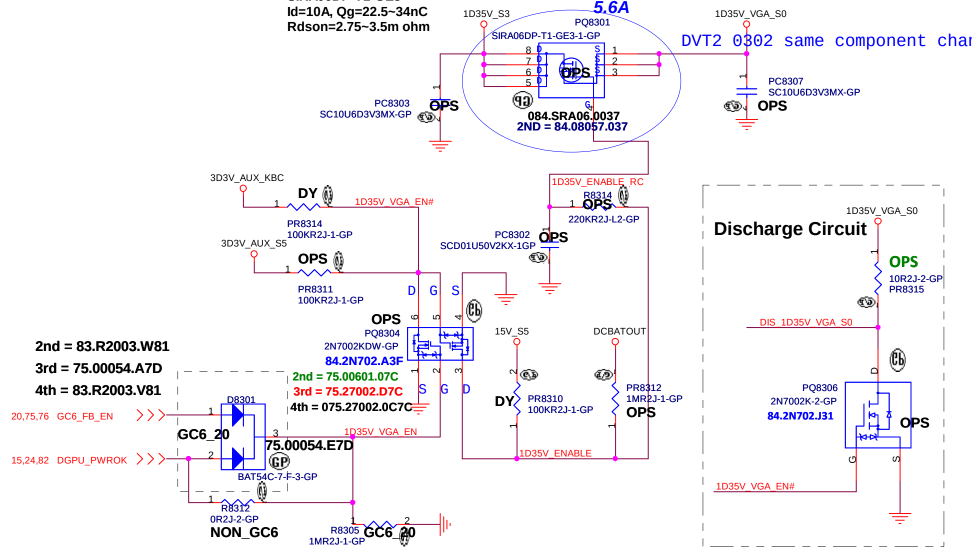
GT: R8303 = 0 ohm (63.R0034.1DL); C8301 = 0.01u (78.10324.2FL)

1D35V_VGA_S0

SIRA06DP-T1-GE3
Id=10A, Qg=22.5~34nC
Rdson=2.75~3.5m ohm

1.35V +/- 3%.
5.6A

DVT2 0302 same component change different part number



CTx (pF)	Rise Time (μs) 10% - 90%, COUT = 0.1μF @ VIN; VOUT=0 ohm load Typical values @ 25°C, 25V X7R 10% ceramic cap 5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

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Title: **DISCRETE VGA POWER**
Size: Custom | Document Number: **Loveland BDW** | Rev: A00
Date: Monday, June 08, 2015 | Sheet 83 of 102

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Title	Reserved	
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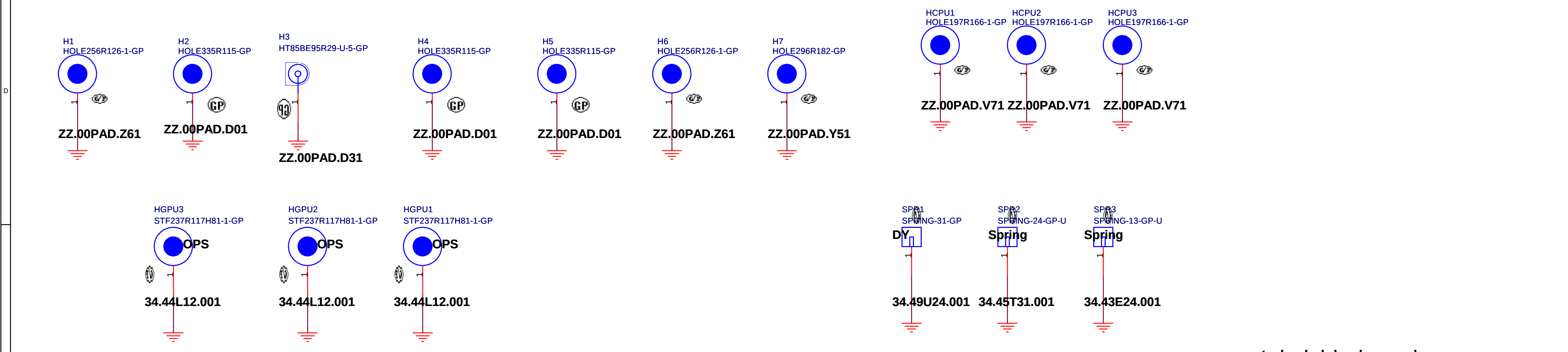
Main Func = UnusedParts



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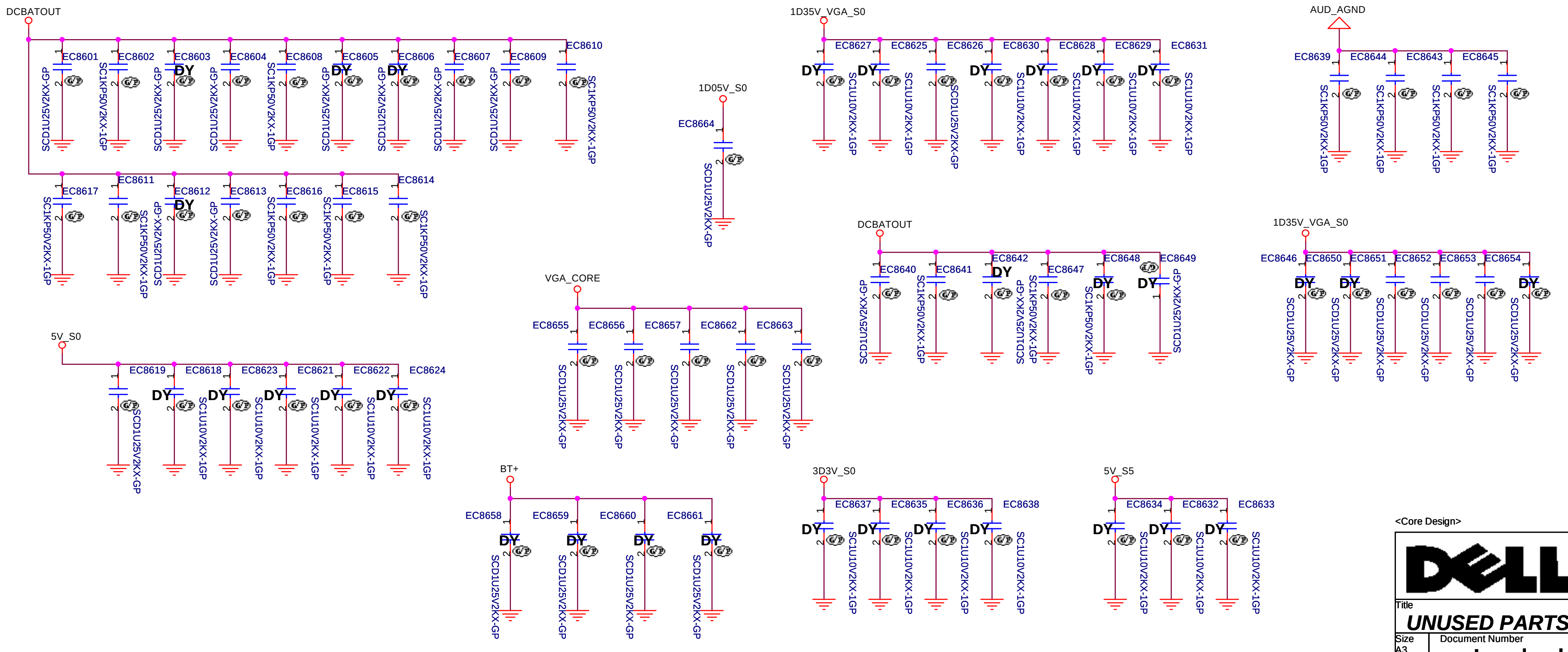
Main Func = EMICapacitors

Mind the voltage rating of the caps.



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Title: *UNUSED PARTS/EMI Capacitors*

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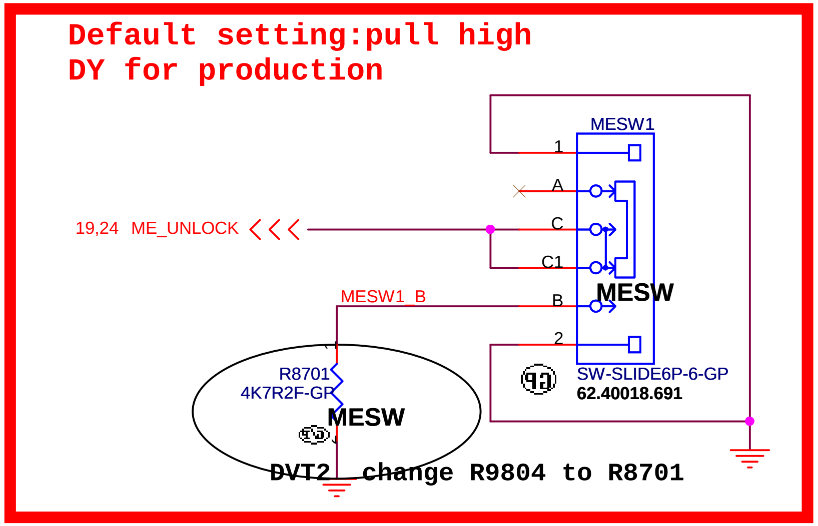
SSID = MESW

Firmware SW



	A	B
ME_FWP_SOC	High	Low
	Normal Operation (Default)	Override

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Title	Firmware SW	
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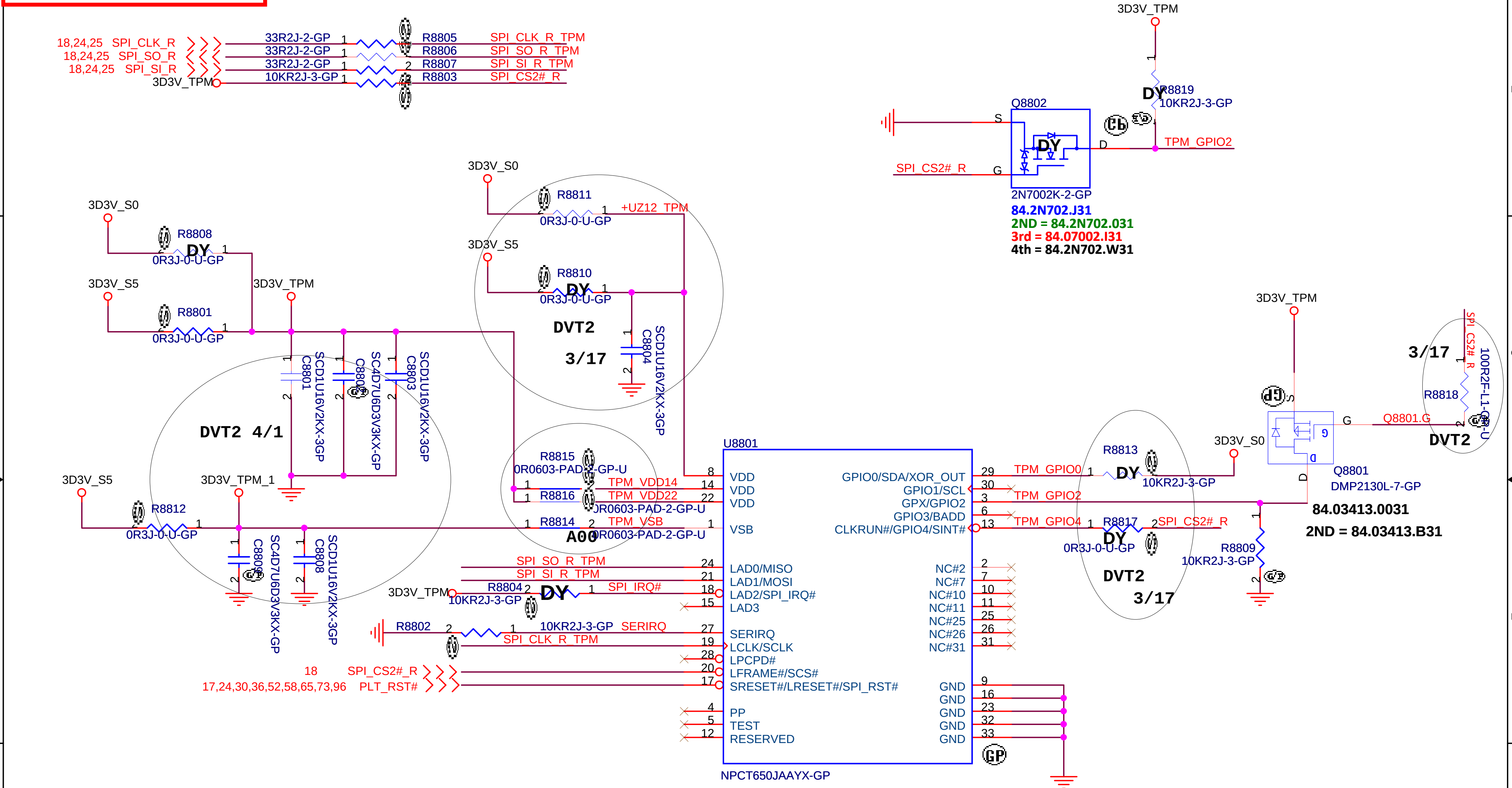
SSID = TPM



TPM version change from 2.0 to 1.2 : 071.00650.0B03

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Title	TPM	
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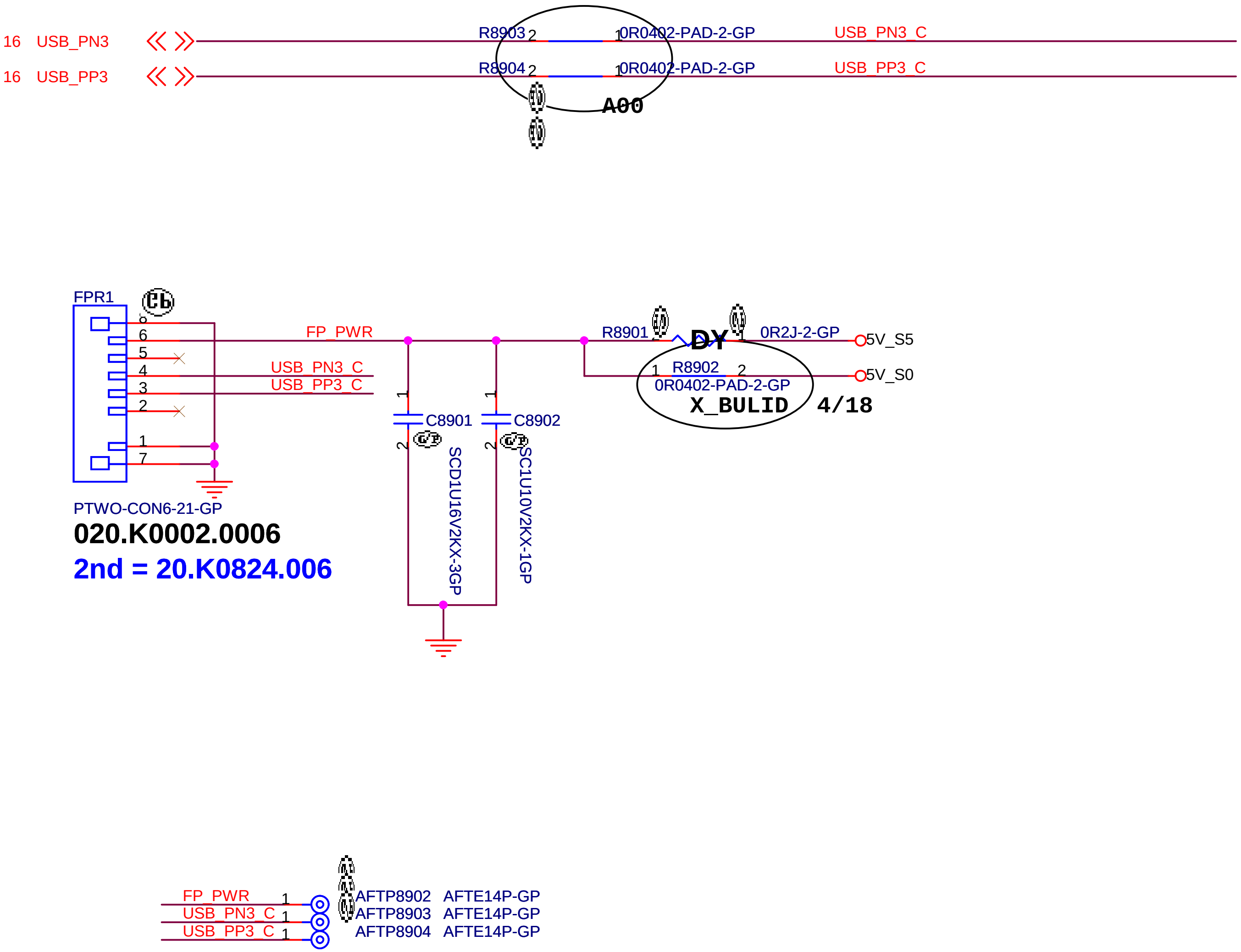
SSID = Finger Print



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Title: **Finger Print**		
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Title		
Free Fall Sensor		
Size: A3	Document Number: *Loveland BDW*	Rev: *A00*
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Title	Reserved	
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Title		
Reserved		
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Title	Express Card	
Size A3	Document Number Loveland BDW	Rev A00
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Title	LVDS_Switch	
Size A3	Document Number: Loveland BDW	Rev A00
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Title	CRT_Switch	
Size A3	Document Number Loveland BDW	Rev A00
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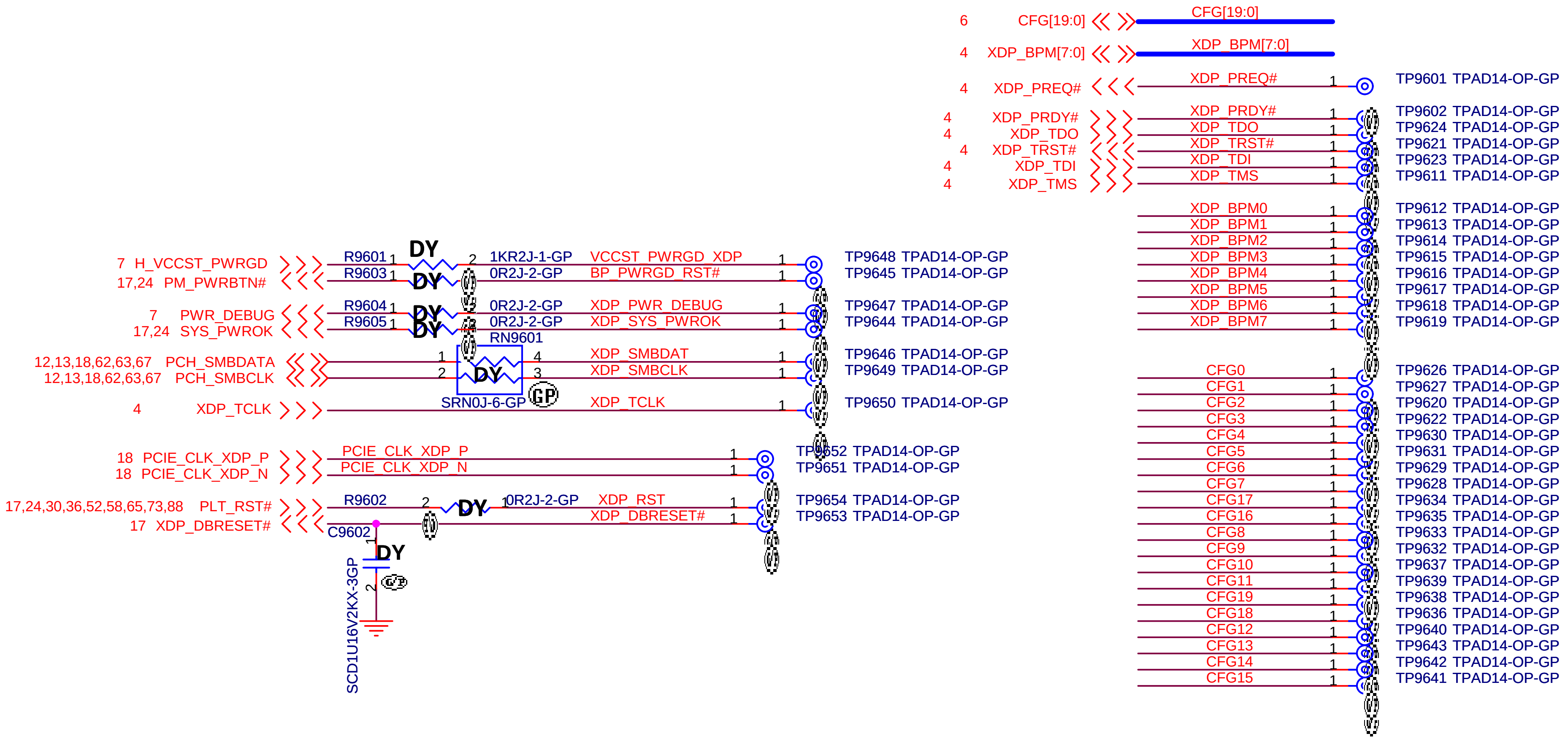
Main Func = Debug

CPU XDP



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Title	CPU_XDP;PCH_XDP	
Size A4	Document Number: Loveland BDW	Rev A00
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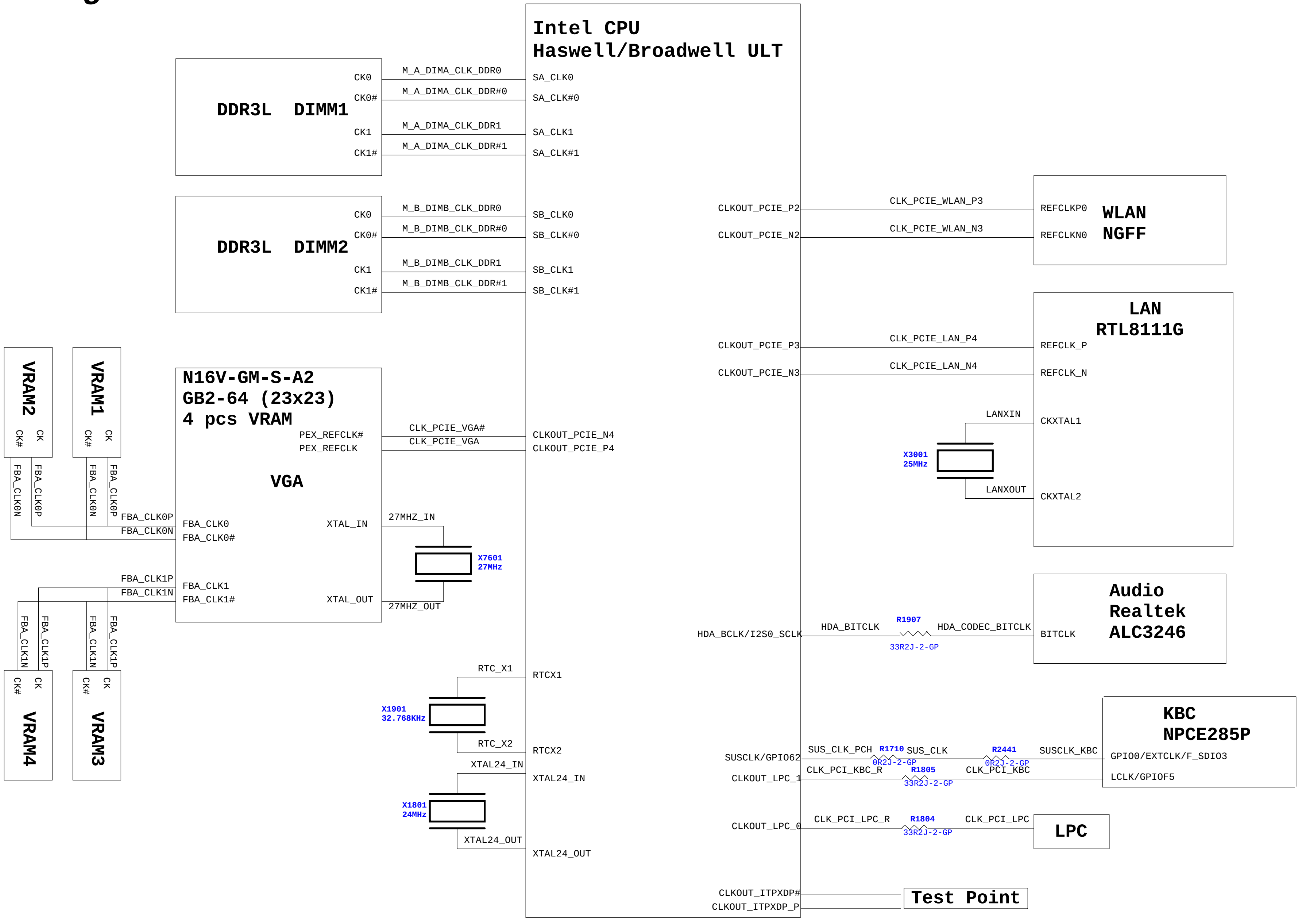
CLK Block Diagram



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Title: *CLK Block Diagram*

Size: A2 | Document Number: *Loveland BDW* | Rev: A00

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Change notes -

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Title		
Change History		
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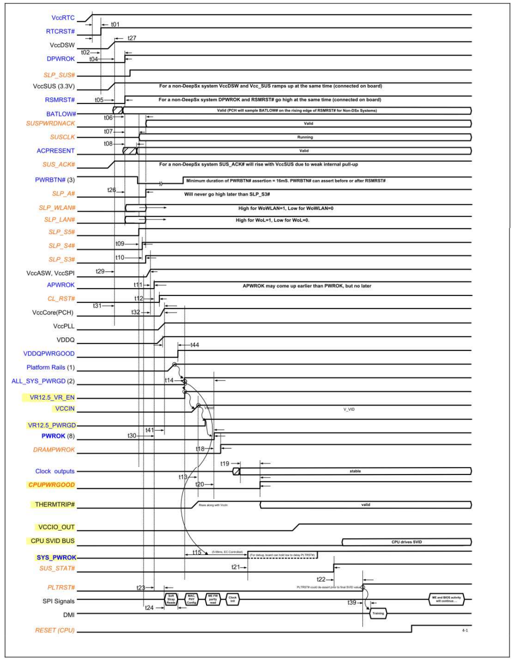
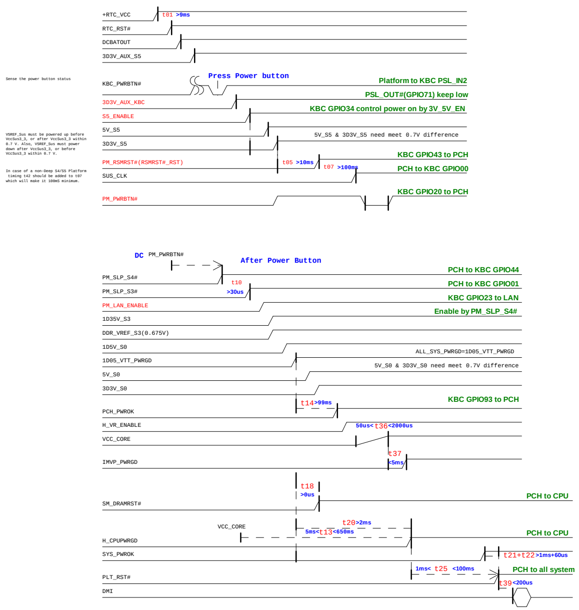
Shark Bay Platform Power Sequence

Timing Diagram for G3 to S0/M0 [non Deep Sx Platform]

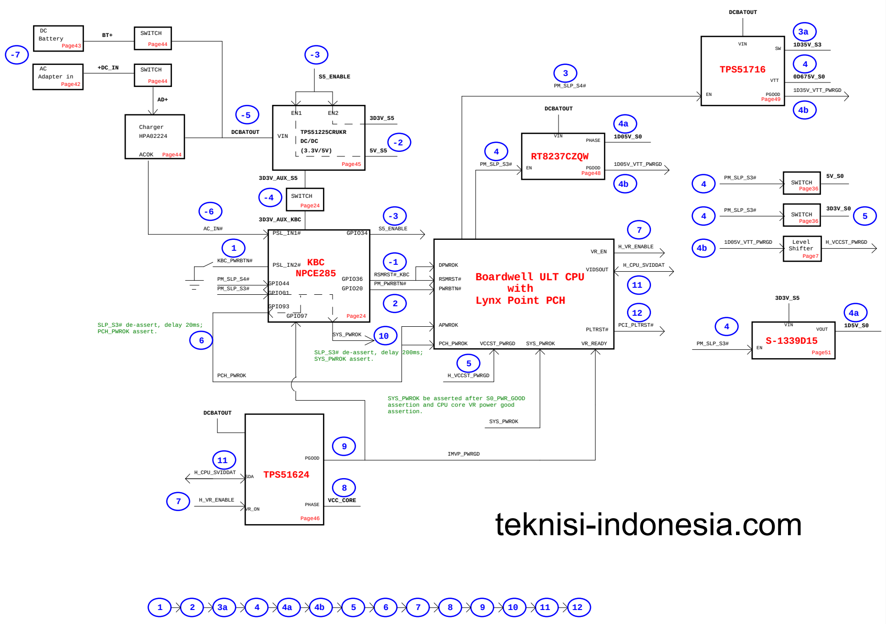


(DC mode)

Red Words: Controlled by EC GPIO



Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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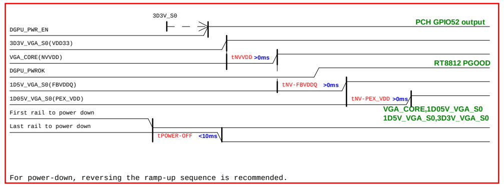
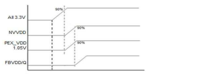
N16V-GM Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

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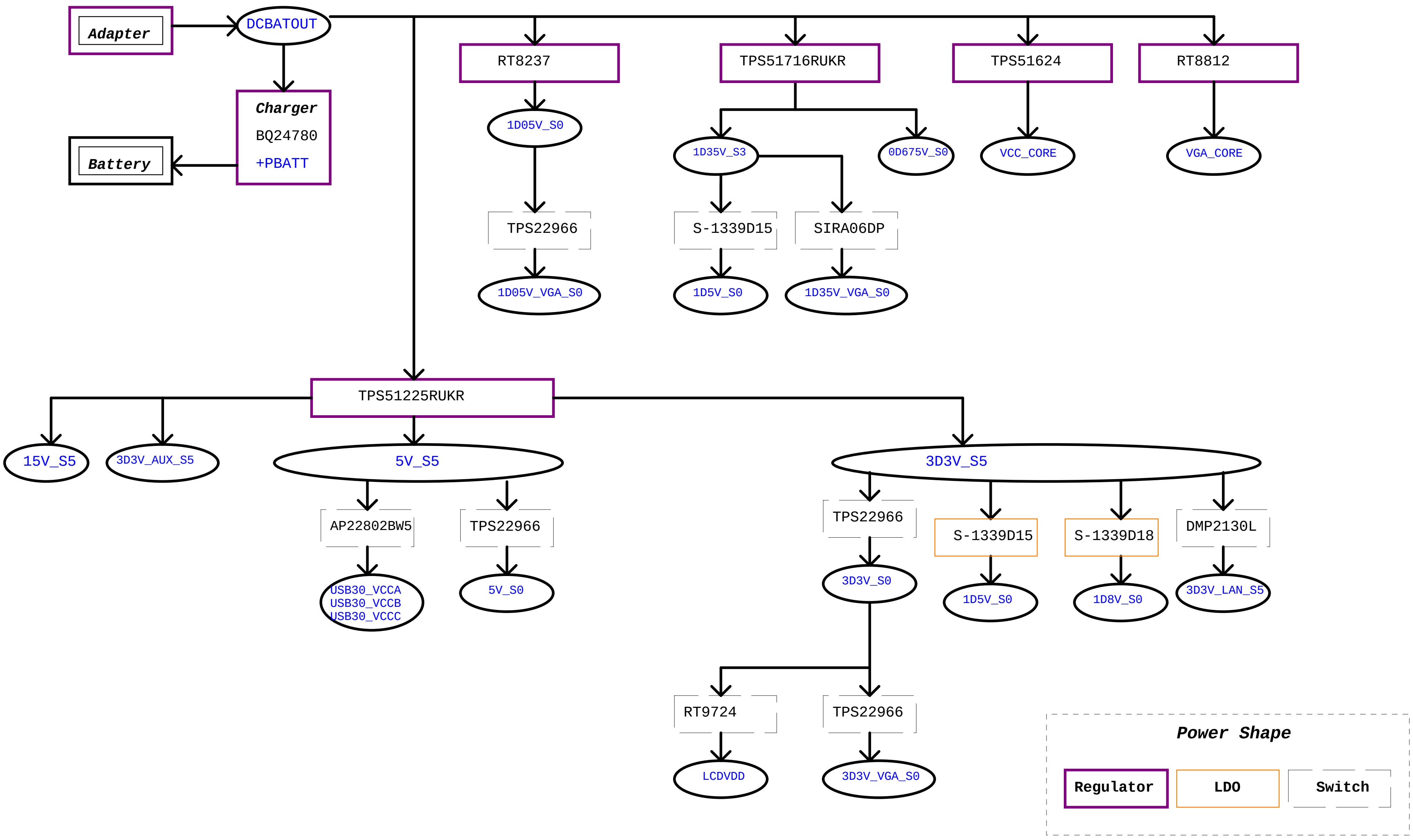
Power Sequence

Loveland BDW



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Title
Power Block Diagram

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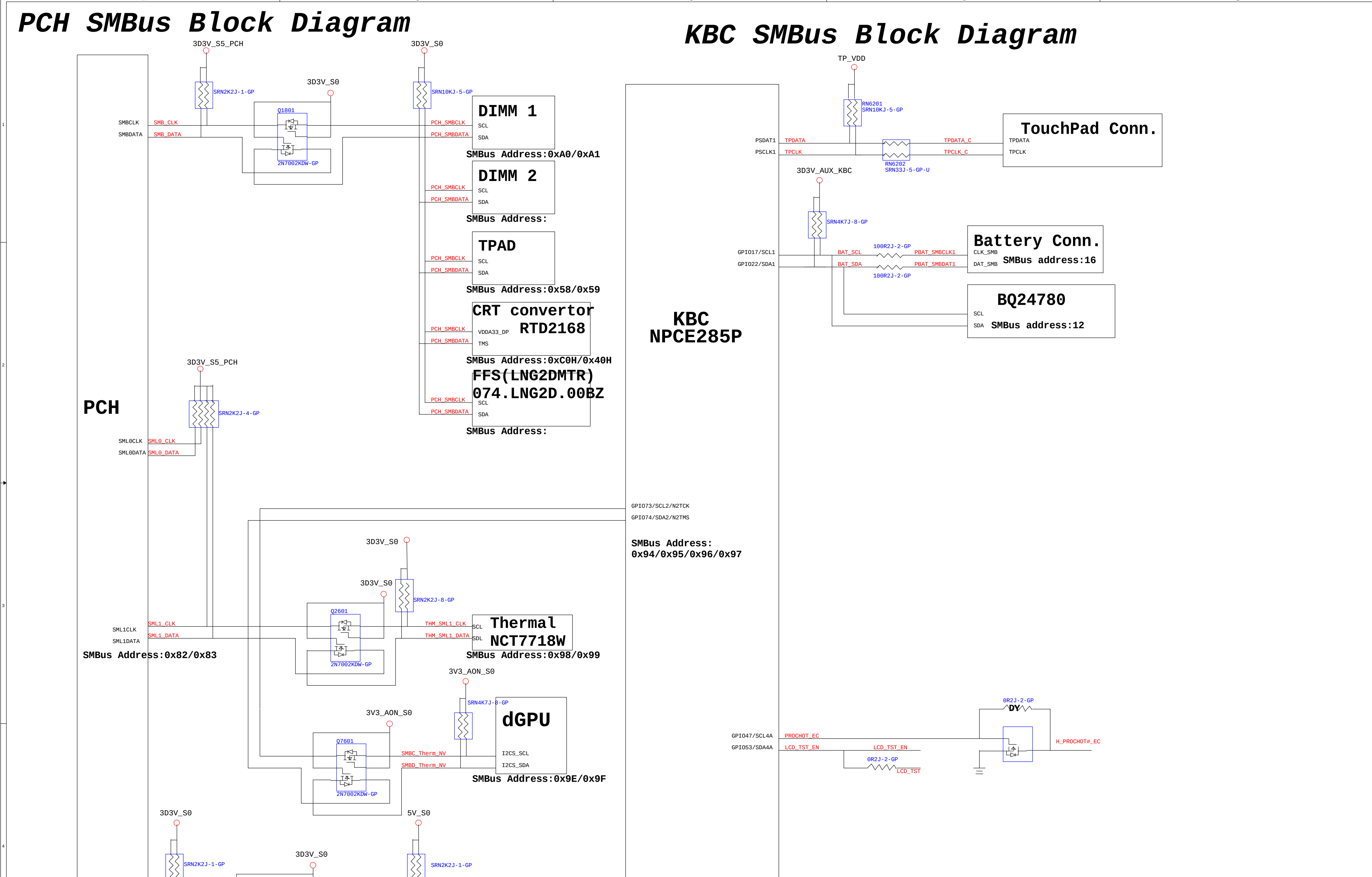

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Title		
SMBUS Block Diagram		
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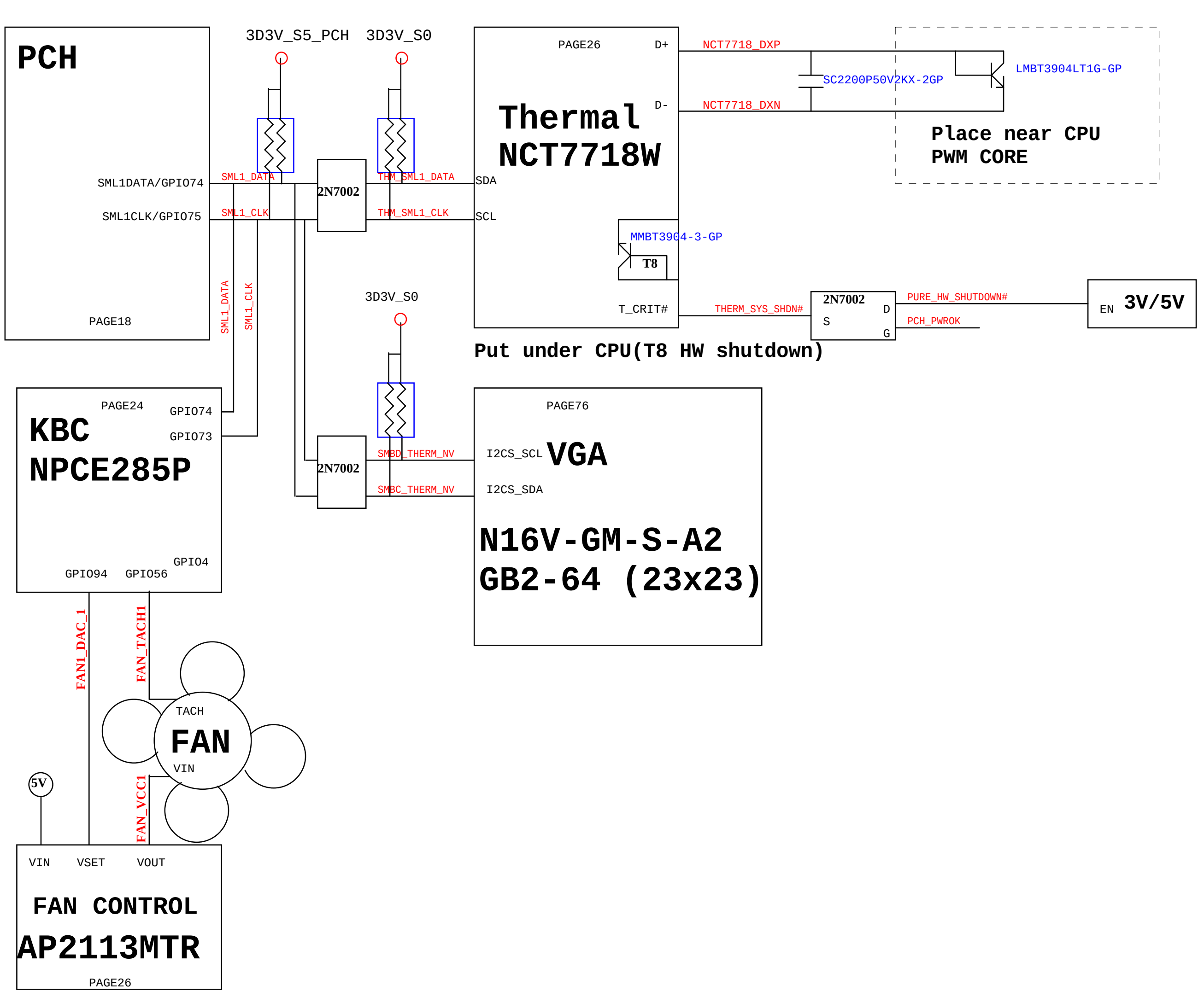
Thermal Block Diagram

Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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