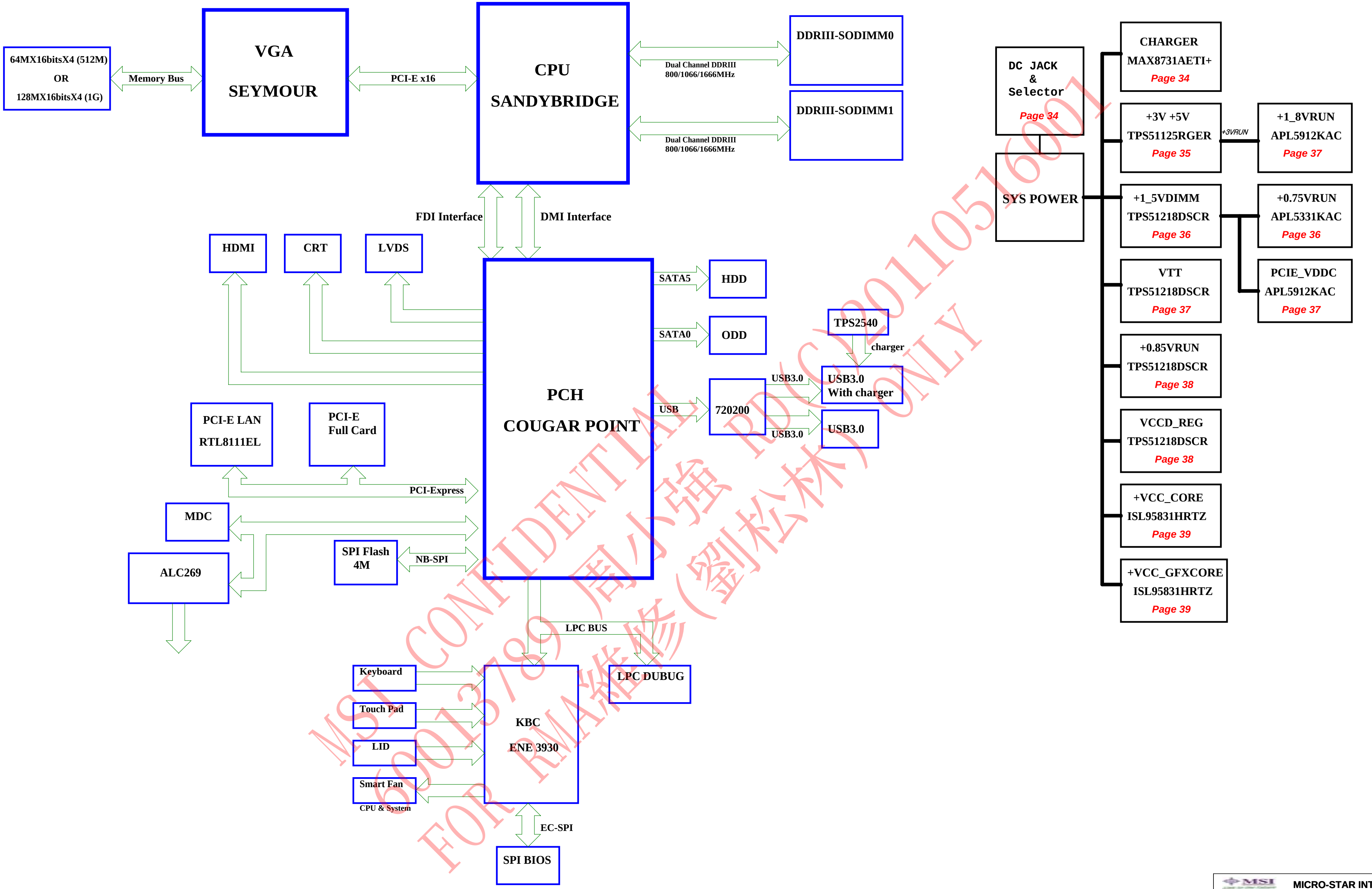

MICRO-STAR INT'L CO.,LTD.

Title: BLCOK

Size	Document Number	Rev
A2	MS-1482	1.0

Date: Friday, December 17, 2010 Sheet 1 of 44

20101122 刪 ME Myler.
20101123 Page32 Change PX4.0 BACO
Add C477.

Page38 Change PQ15
PCIE_VDDC_PWG--->RUN_ON

Page 37 PCIE_VDDC_PWG ->PR141-->+3VRUN
PR141 Change

Page 14 Remove R60 ,Q10 ,
+0.85V_PWRGD->GPU_PWRGD-->Q25 G1

20101201 Page 16~24 Change PCH 新版的
OB1-1484002
20101202 Change R4,R5,R7,R11,R37,R77,R78,R101,
R104,R109,R171,R251,R297,R304,
R305,R348,RA12,RA10,RA6,RA3,RA5

20101203 Page28 換 USB3.0 料號

20101203 Page26 U4 kbc B0->A1

20101208 Page27 HP_DET 端 R152,C234 上件
Q18,R172,R144 上件, R171 不上件

20101213 Page37 PC46 上件
20101208 Page32 CON3 Pin14 -->USBEN_EC
20101208 Page41 CONA1 Pin19 -->USBEN_EC_A

20101208 Page29 Q34 Move ,Q34 Change
20101208 Page25 U32 Pin4 Dele Resistor
20101208 Page21 add HOST_ALERT#2, ICC_EN# &
SMIB ,R400不上件,R401上件

20101208 Page25 USB3.0 P4 add SMIB

20101208 Page13 Change SMB_CPU_CLK &
SMB_CPU_DATA

20101208 Page39 ADD PEC17 FOR POWER NOSIE
20101215 Page11~14 PM Change GPU U30
20101208 Page31 Con5 ,C52 上件
20101208 Page21 R308 1K -->10k
20101208 Page21 R401 上件

20101208 Page25 L20,L31 上件
L32,L33 不上件 Spec. Change
CI36, C479, C480 不上件

20101209 Page31 DC4 C52 CON5 上件

20101209 Page43 PM Change DC4 要上件
Page31 C52, CON5要上件

20101209 Page40 ME Change UME1,PCIE_H1 上件

20101209 Power Team Change list
Page34 PQ4 更改料號:D03-0431702-A30
PQ18更改料號:D03-0492702-A30

Page36 PQ11 更改不上件
PR26 更改爲39 Kohm 料號 :R11-0393T12-W08

Page37 PR99 更改爲9.53 Kohm 料號:R11-9531T12-W08

Page38 PR44 更改爲 6.2 Kohm 料號:R11-0622T12-W08

Page39 PR117更改爲 14Kohm 料號:R11-0143T12-W08
PC78 更改爲0.068uF,料號:C11-6832512-W08

20101215 Page34 ME Change CN2 Battery Con. 換料
Footprint 用新的BATHOLD_D9_9
(ME 解 Battery 去接觸不良)

20101215 Power Team Change
Page34 PQ18,PQ1 更改料號: D03-0492702-A30

201012XX Change Page13 R394,R395,
Page21 R308,
Page39 PC78
Page34 PQ2, PQ3
Page36 Q1
Page28 Q11
Page33 Q21, Q22, Q33
Page28 Q8
Page36 PR26
Page38 PR44

20101111 Page25 與 U2 區隔換料號Change U20

20101027 Page26 change Y1

Page16 change Y5

Page27 change Q31

Page37 PQ29, PR103, PR100, PR102,
PC111不上件, H_SNB_IVB#_PWRCTRL 不再有作用

Page34 change PQ21

Page13 change Q29

20101271 Page31 建 1.0 PCB 料號

MSI	MICRO-STAR INT'L CO.,LTD.		
Title	STORY		
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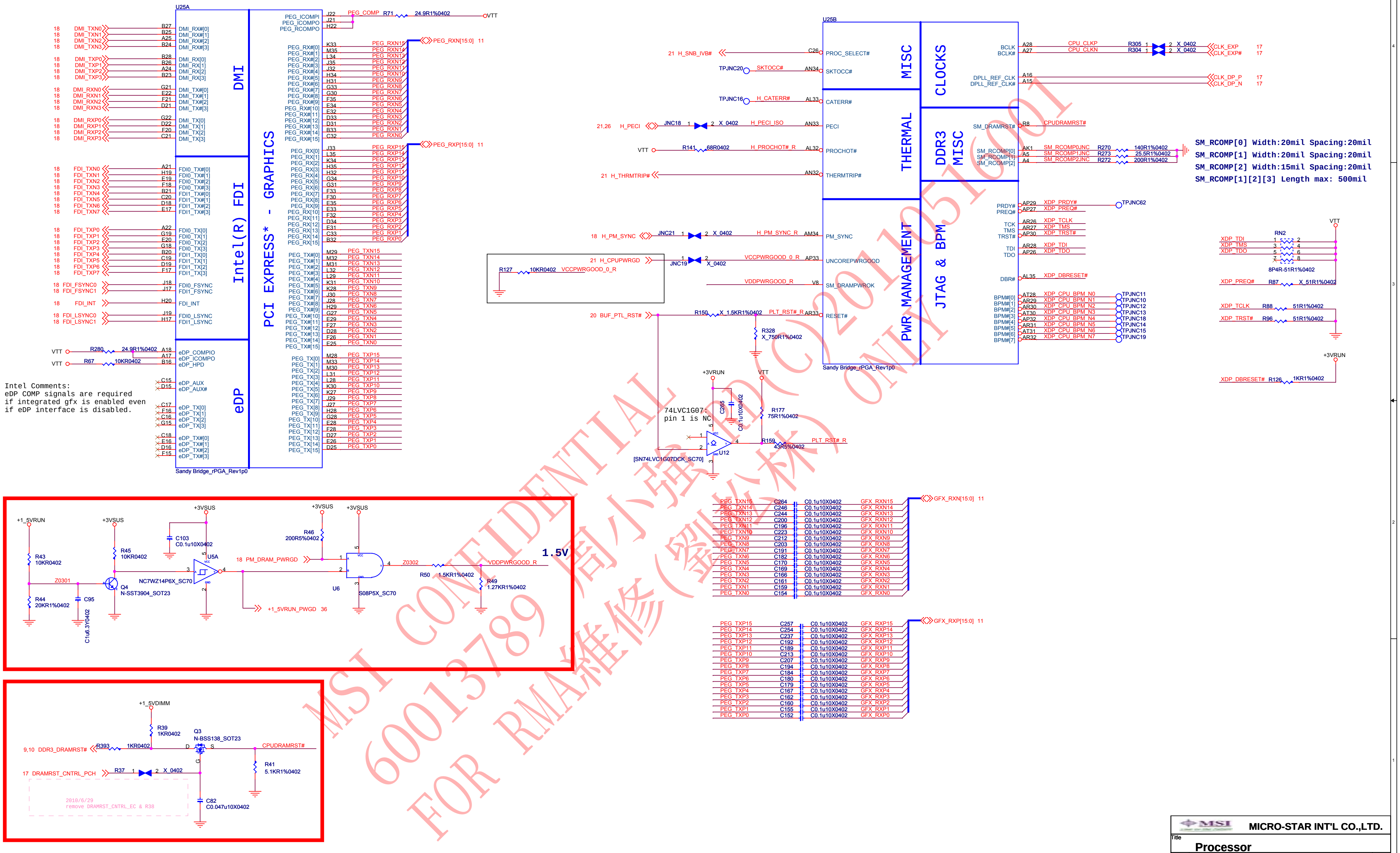
SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)



SM_RCOMP[0] Width:20mil Spacing:20mil
SM_RCOMP[1] Width:20mil Spacing:20mil
SM_RCOMP[2] Width:15mil Spacing:20mil
SM_RCOMP[1][2][3] Length max: 500mil

Intel Comments:
eDP COMP signals are required
if integrated gfx is enabled even
if eDP interface is disabled.

MICRO-STAR INT'L CO.,LTD.

Title	Processor	
Size: Custom	Document Number: MS-1482	Rev 1.0
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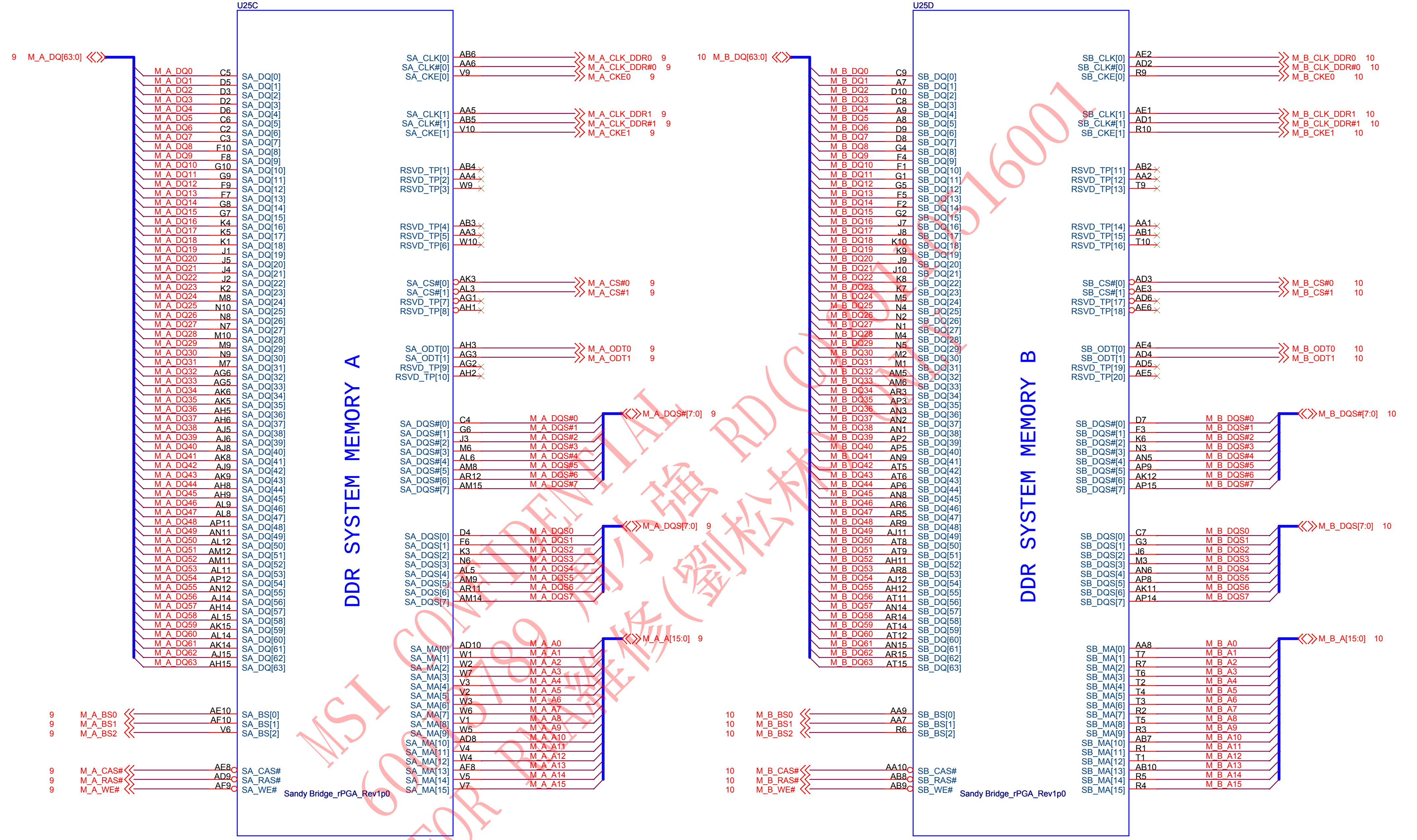
SANDYBRIDGE PROCESSOR (DDR3)



MICRO-STAR INT'L CO.,LTD.

Title: Memory

Size: Custom | Document Number: MS-1482 | Rev: 1.0

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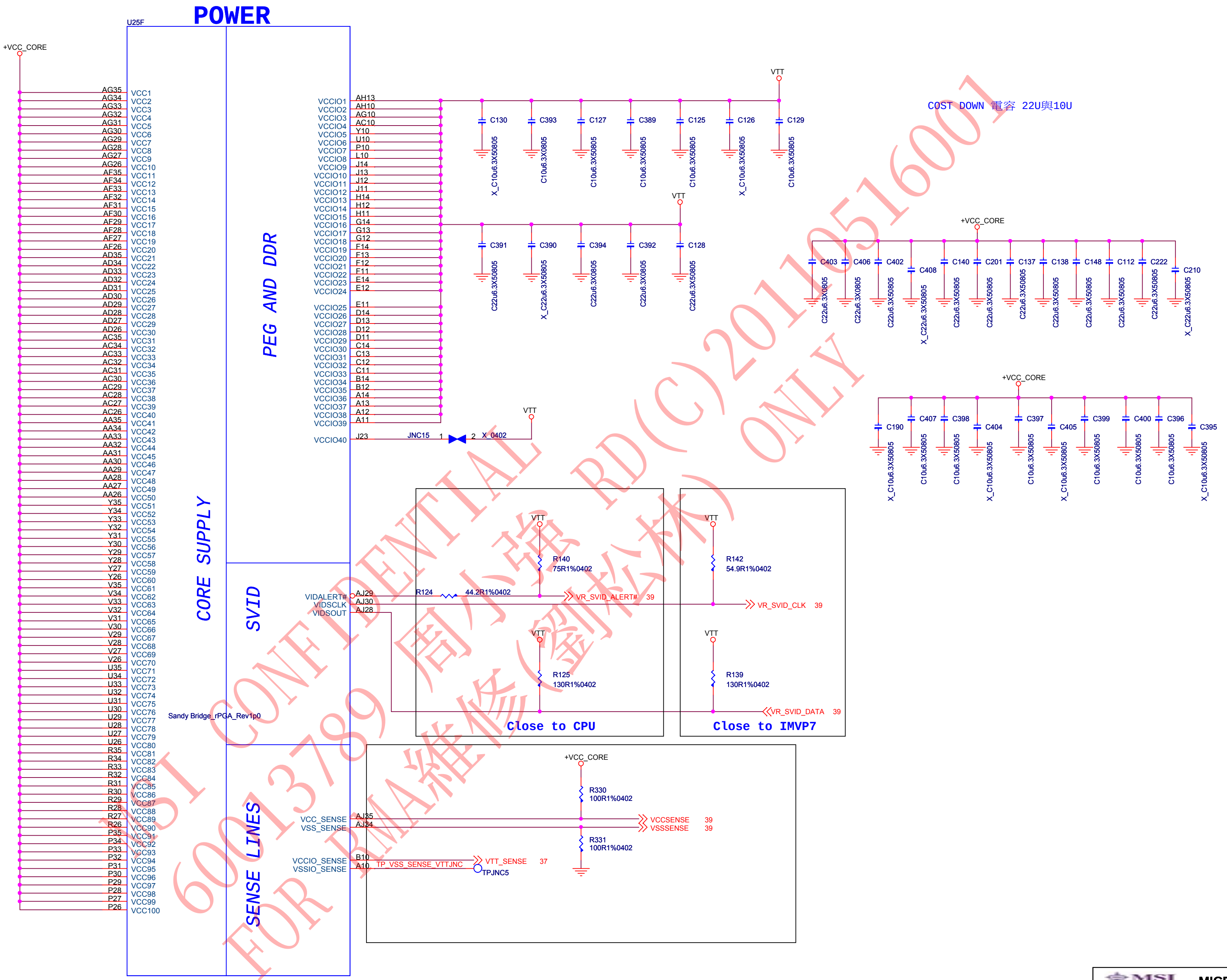
SANDYBRIDGE PROCESSOR (POWER)



MICRO-STAR INT'L CO.,LTD.

Title: Processor power

Size: Custom | Document Number: MS-1482 | Rev: 1.0

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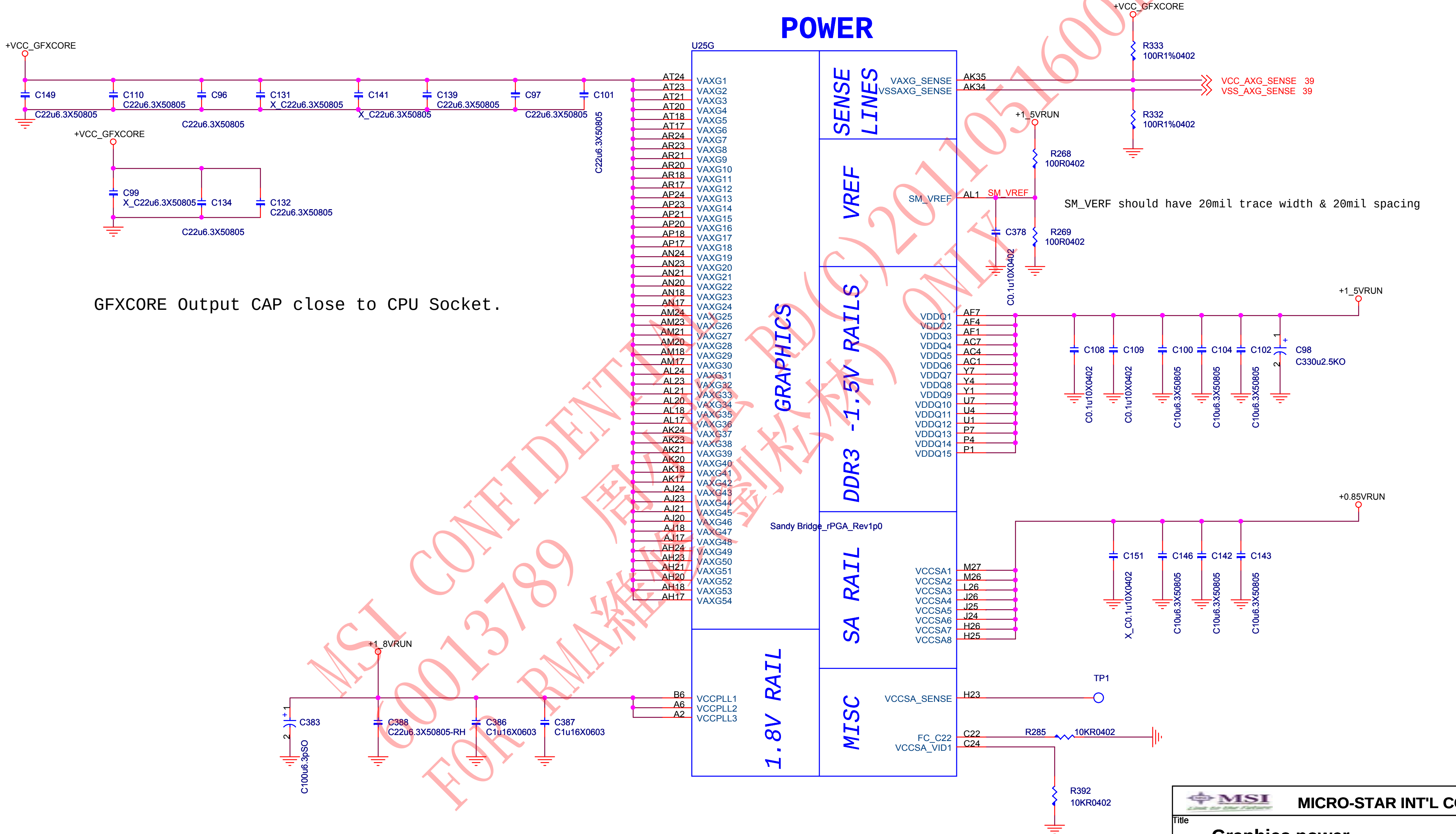
SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



SM_VERF should have 20mil trace width & 20mil spacing

GFXCORE Output CAP close to CPU Socket.

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	Graphics power	
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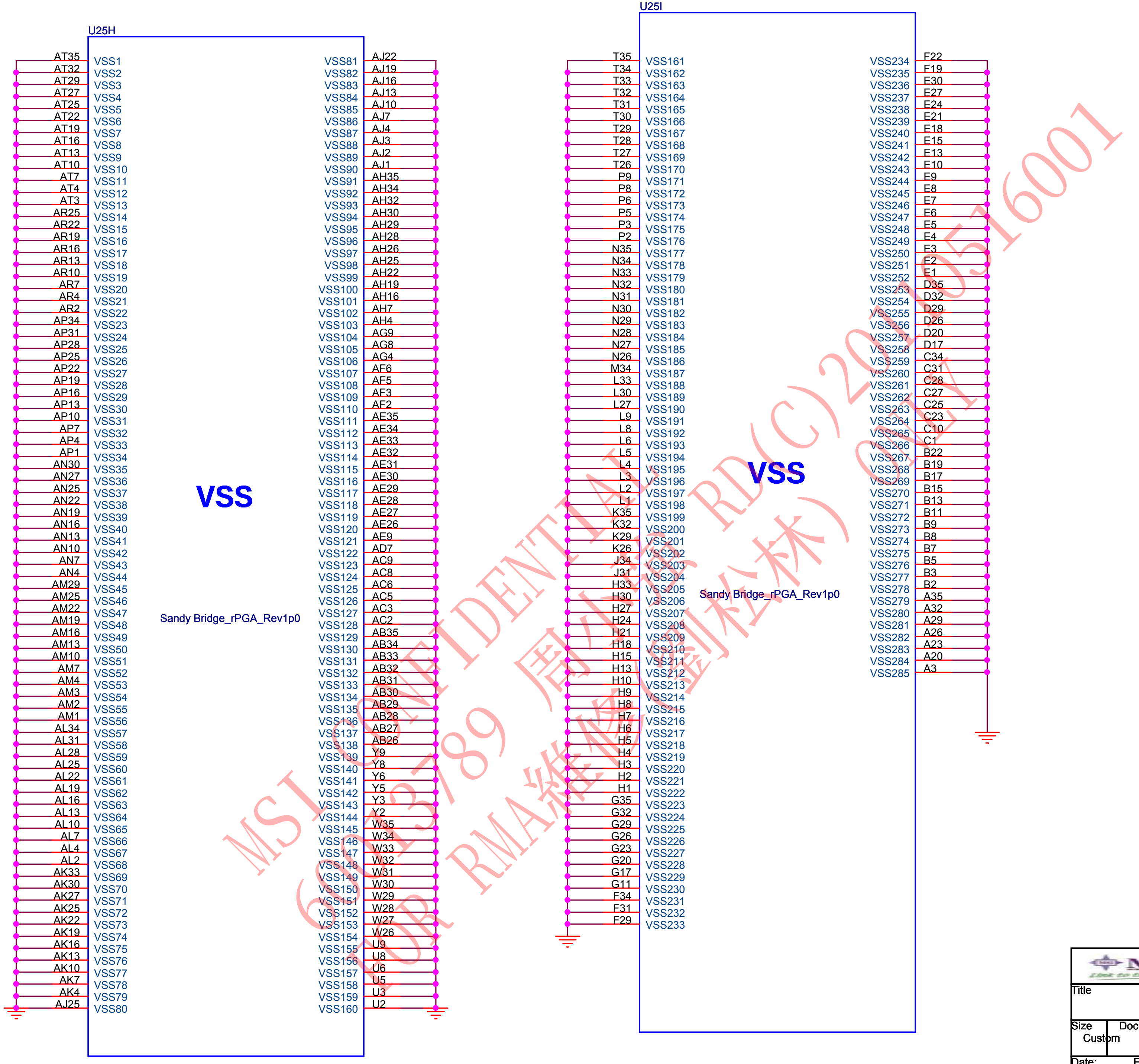
SANDYBRIDGE PROCESSOR (GND)



MICRO-STAR INT'L CO.,LTD.

Title: GND		
Size: Custom	Document Number: MS-1482	Rev: 1.0
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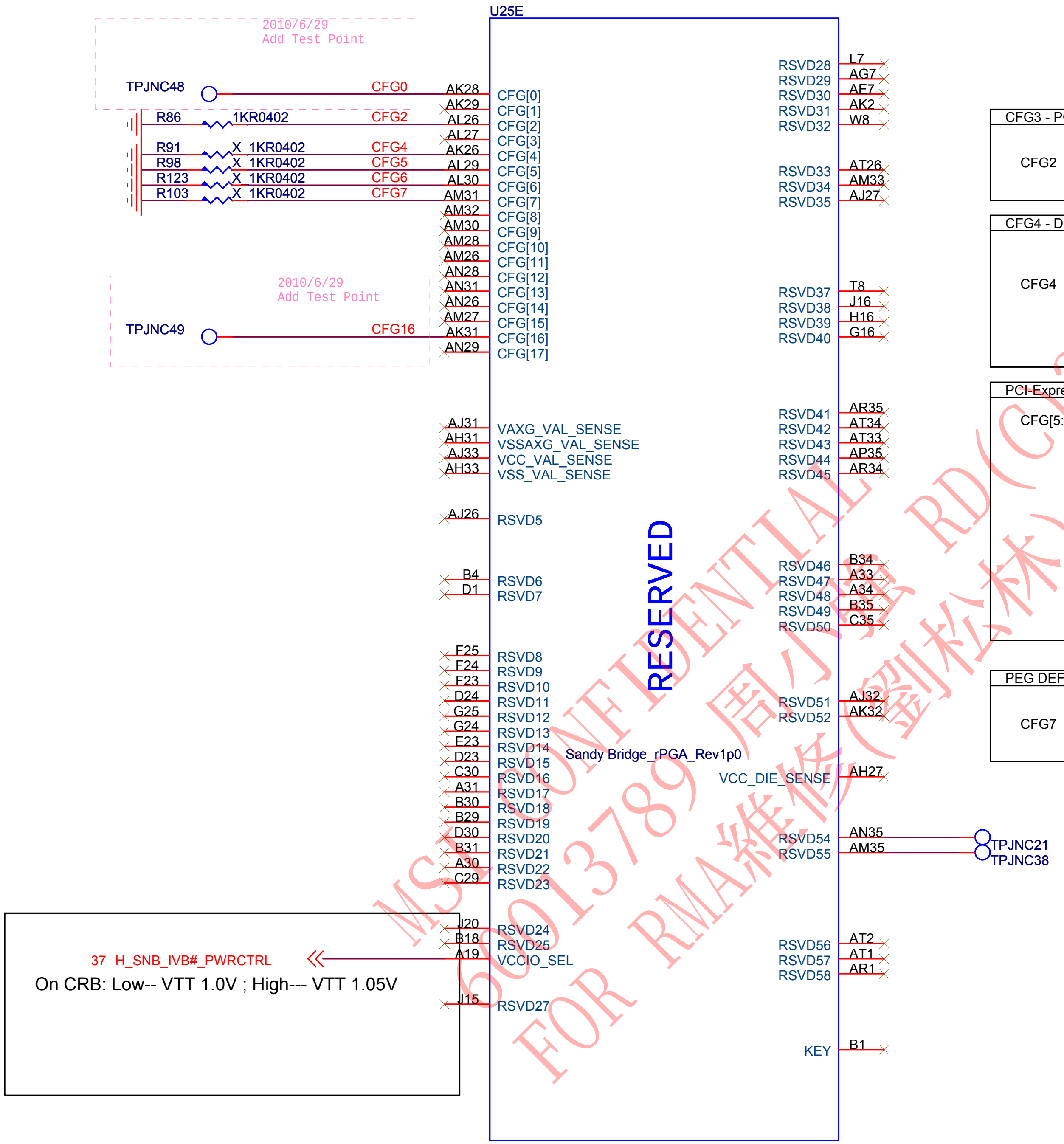
SANDYBRIDGE PROCESSOR (RESERVED)



CFG3 - PCI-Express Static Lane Reversal

CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select

CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING

CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

MICRO-STAR INT'L CO.,LTD.

Title	CFG RSVD		
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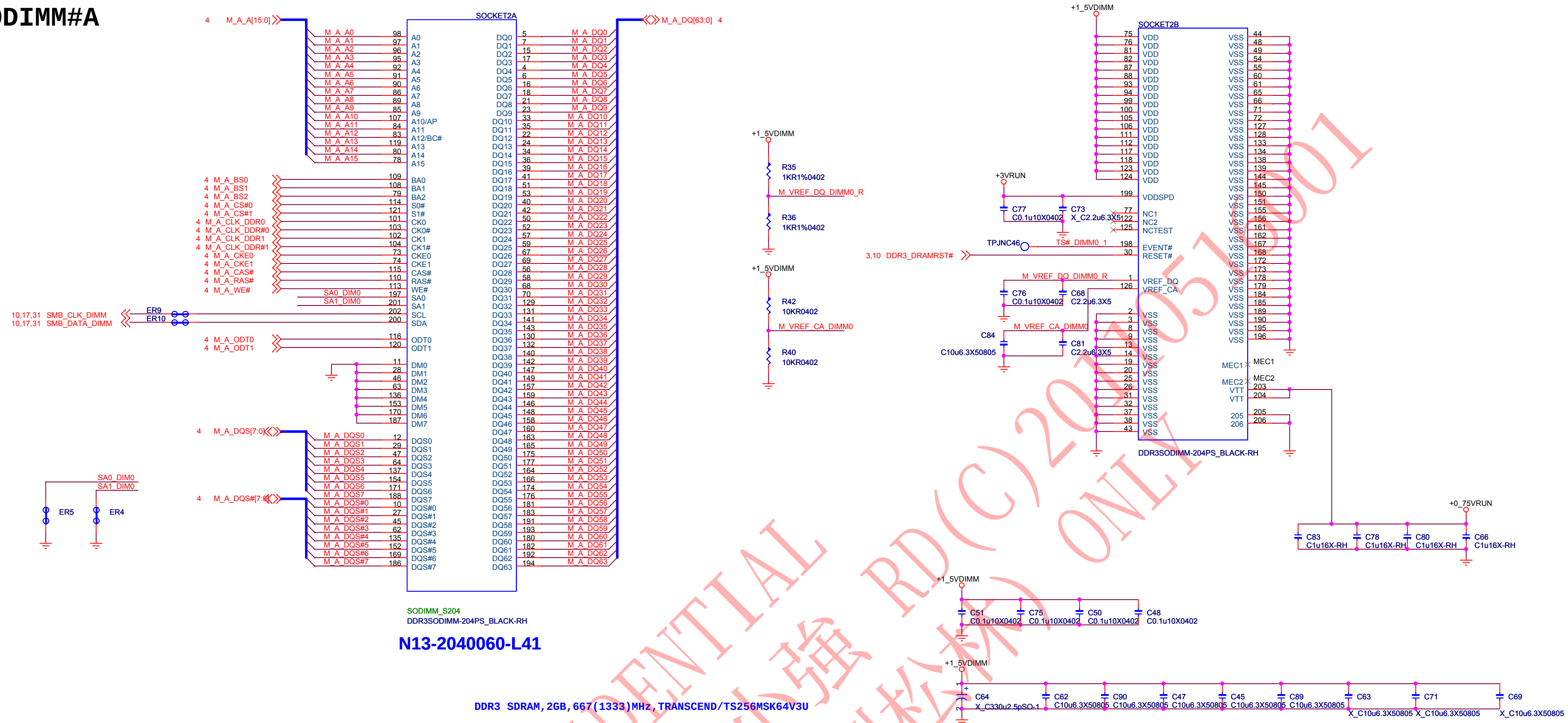
SODIMM#A



DDR3 SDRAM,2GB,667(1333)MHz,TRANSCEND/TS256MSK64V3U

IDD Specification parameters Definition
(IDD values are for full operating range of voltage and Temperature)

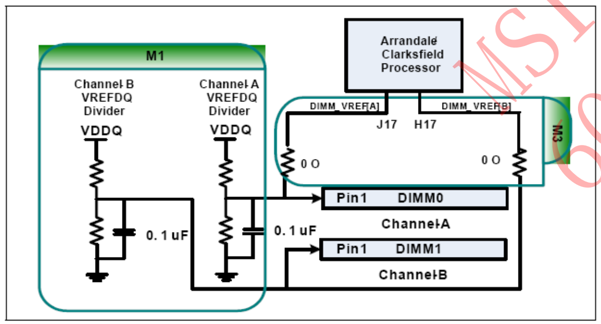
Parameter	Symbol	Max.	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1,200	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	1,360	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	800	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	960	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	960	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	800	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	1,000	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	2,120	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	2,320	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	2,240	mA
Self refresh current; CK and /CKat 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	160	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R	IDD7	3,400	mA

2.5.4 DDR3 VREFDQ Design Implementation

Intel is requesting that customers implement two methods (M1 and M3) to generate and control the DDR3 SO-DIMM Reference voltage for Data/Strobe inputs (V_{REFDQ}) on Arrandale- and Clarksfield-based platforms. For Arrandale, M1 should be used. For Clarksfield only designs and common motherboard designs (which support both Arrandale and Clarksfield processors), both M1 and M3 methods should be con- currently implemented.

Note: DDR3 V_{REFDQ} recommendation outlined above in this document, V_{REFCA} and V_{REFDQ} on SO-DIMM cannot be tied together any more for Clarksfield only and Common motherboard designs in order to support M3 and M1/M3 co-existence.

Figure 33. Clarksfield DDR3 SO-DIMM VREF_DQ Design Requirements



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Title	DDR3 SODIMM0
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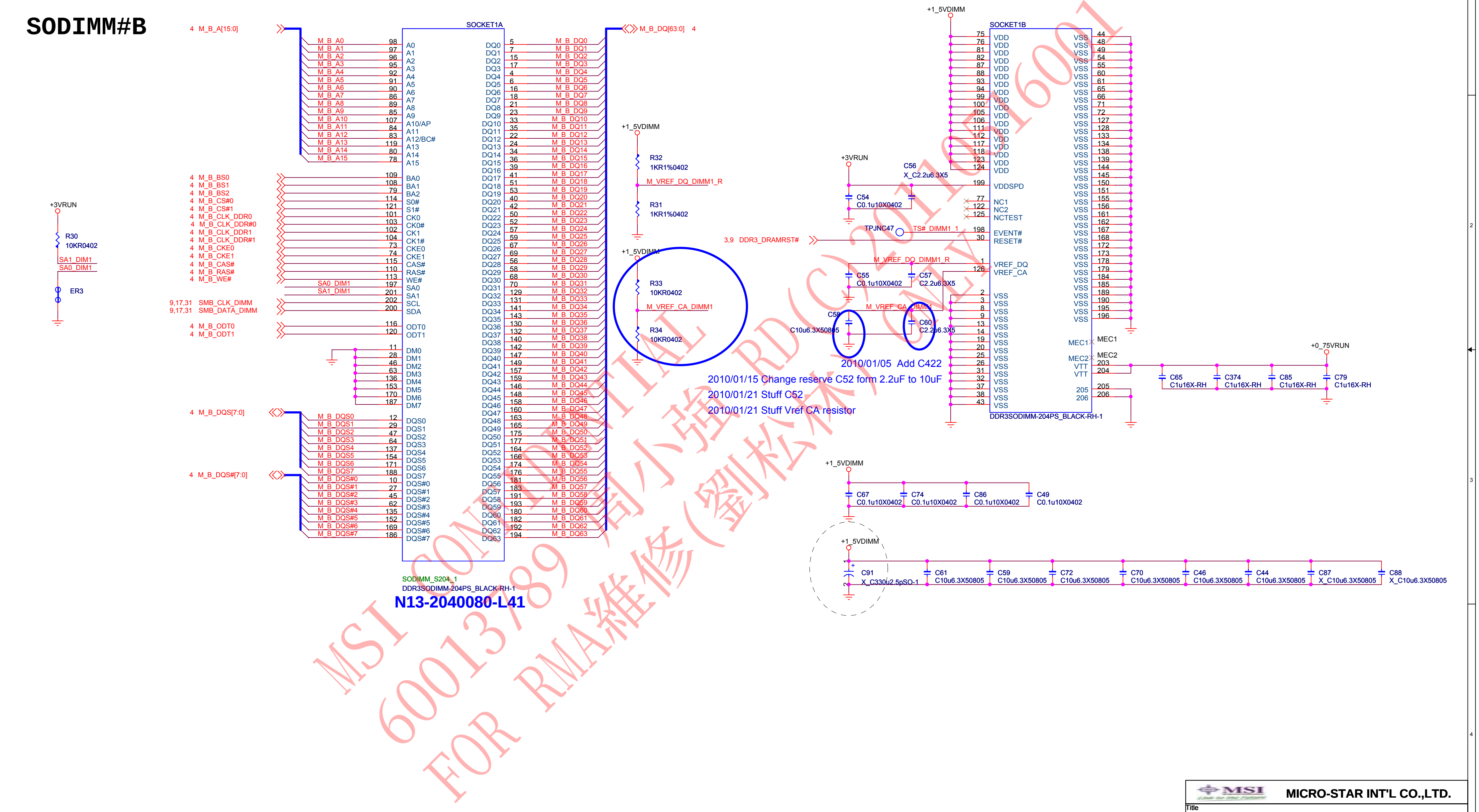
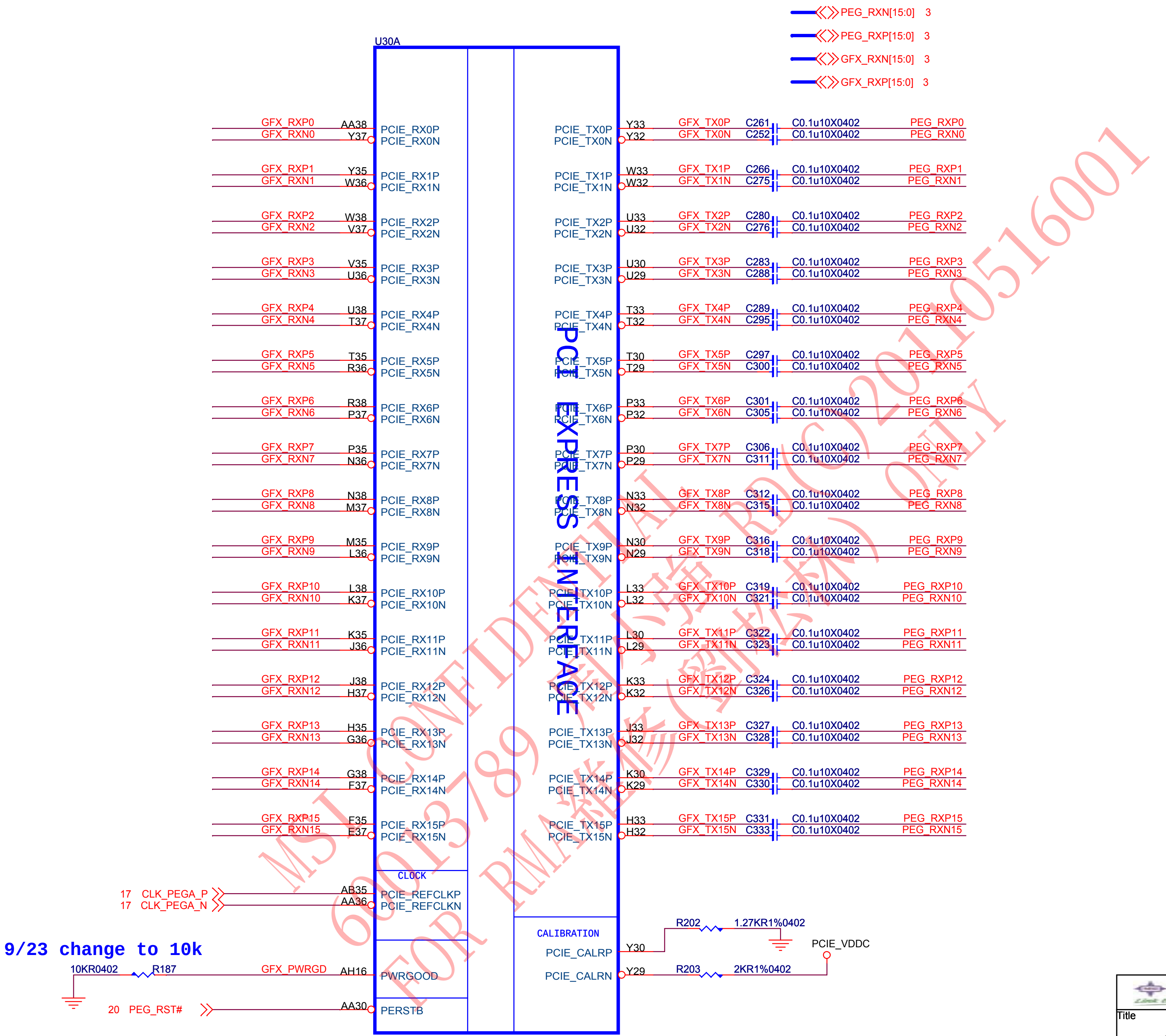
SODIMM#B



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	DDR3 SODIMM1	
Size Custom	Document Number MS-1482	Rev 1.0
Date: Friday, December 17, 2010	Sheet 10 of 44	

5 4 3 2 1

D C B A



MICRO-STAR INT'L CO.,LTD.

Title: ATI VGA PCIE

Size	Document Number	Rev
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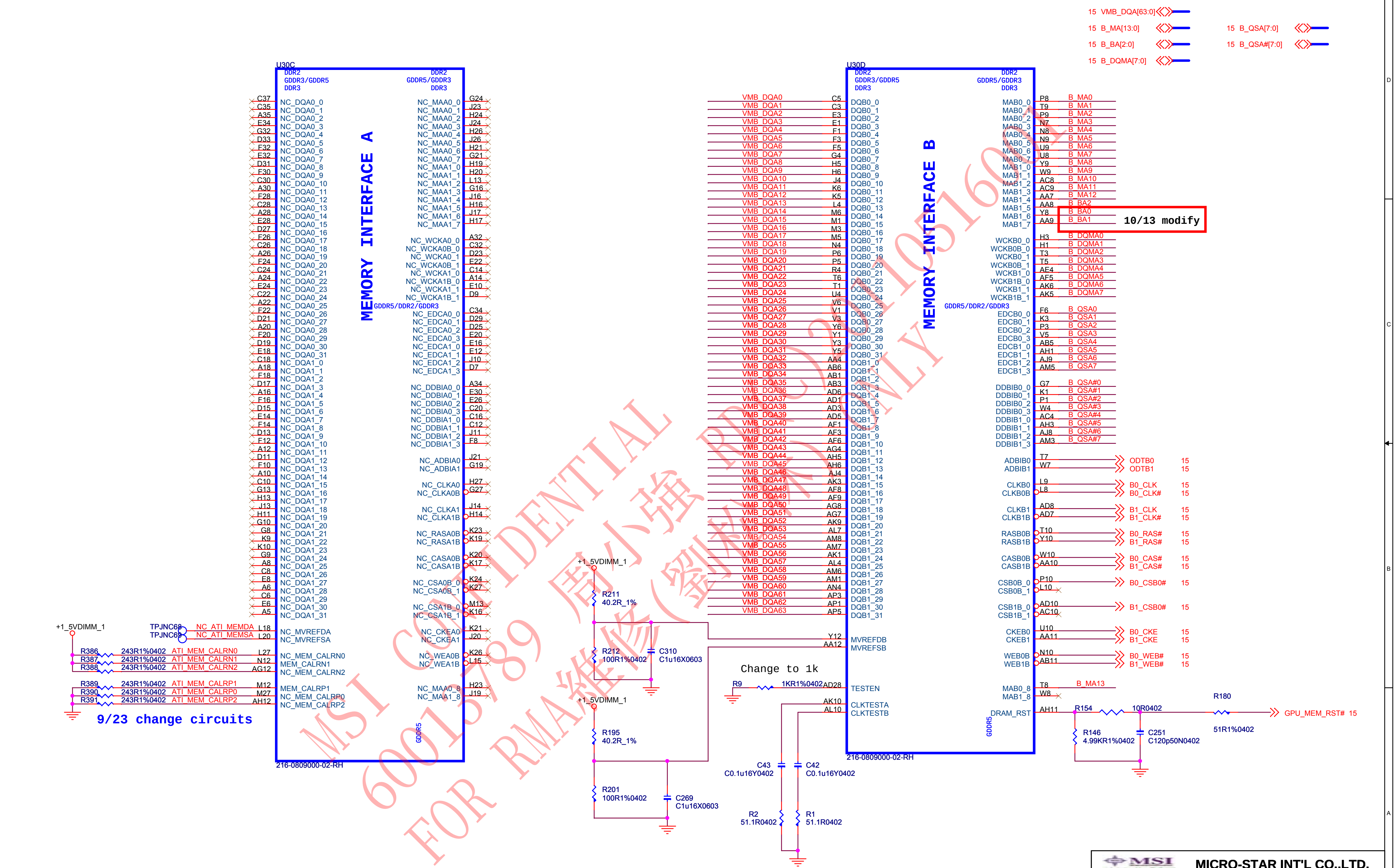
5 4 3 2 1



MSI	MICRO-STAR INT'L CO.,LTD.
Title	ATI VGA MEM
Size: Custom	Document Number: MS-1482 — Rev 1.0
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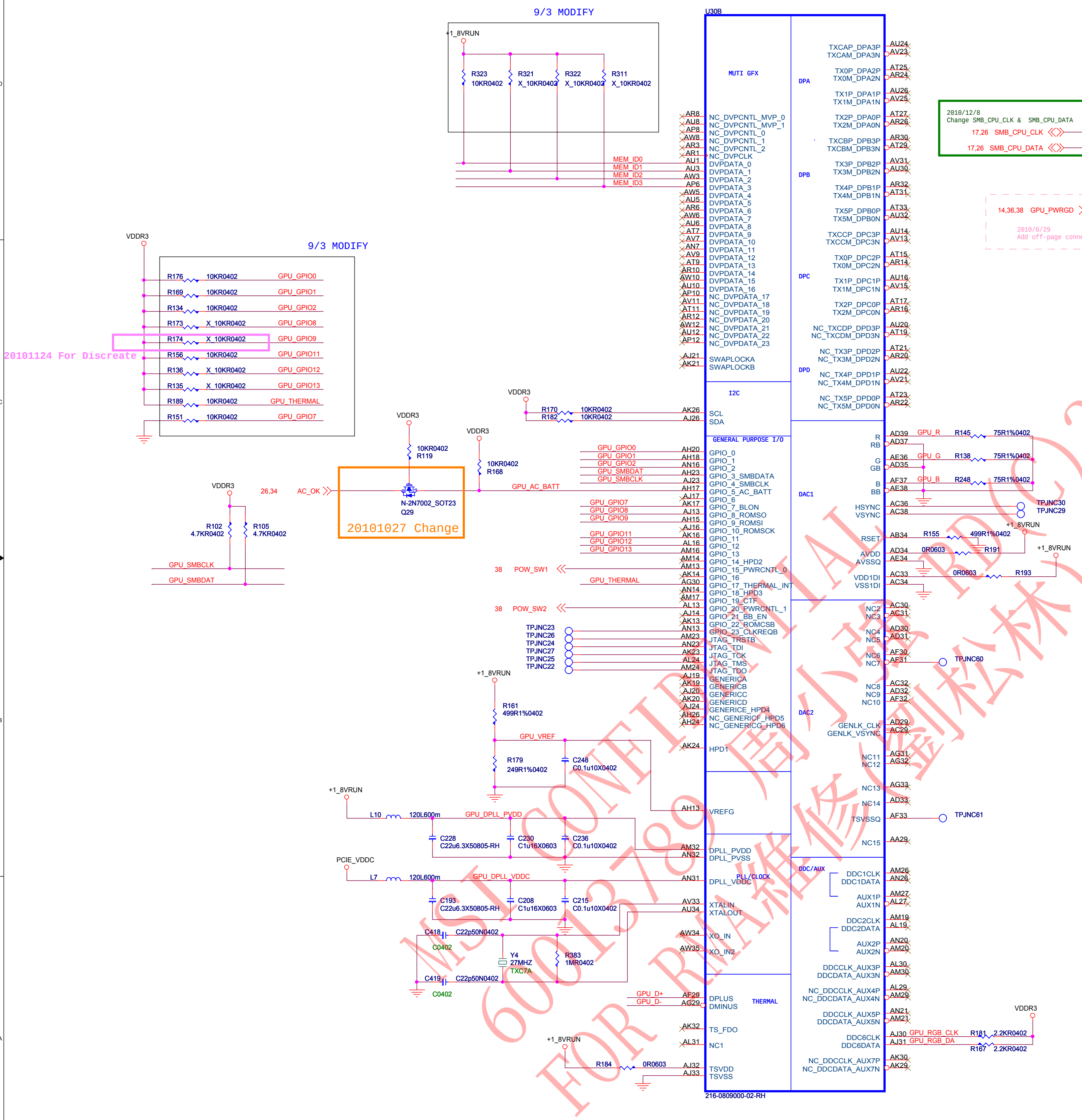

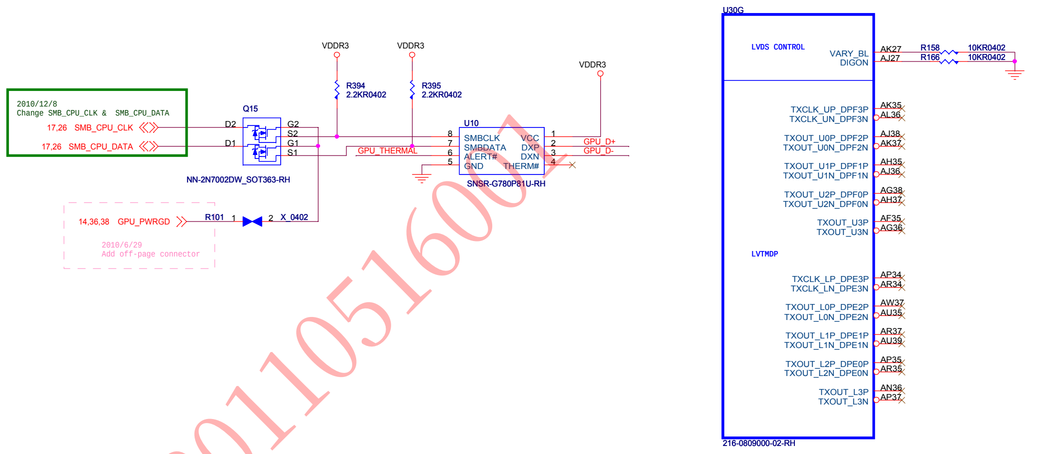

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

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Title	ATI VGA DP		
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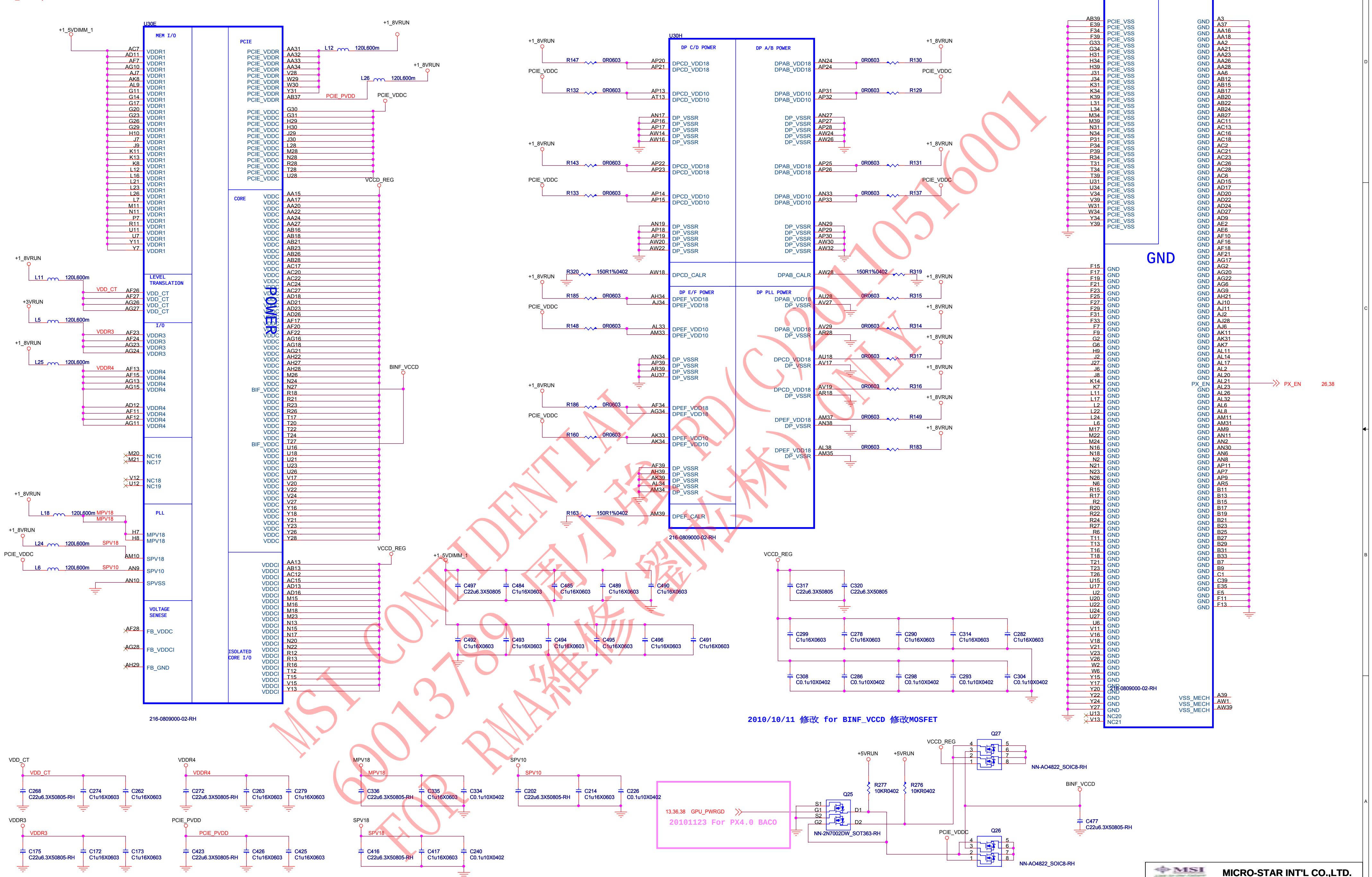
BACO enable just close the core power

PX_EN=0, for Normal Operation

PX_EN =1, for BACO MODE



2010/10/11 修改 for BINF_VCCD 修改MOSFET

20101123 For PX4.0 BACO

MICRO-STAR INT'L CO.,LTD.

Title	ATI VGA PWR GND		
Size A2	Document Number MS-1482		Rev 1.0
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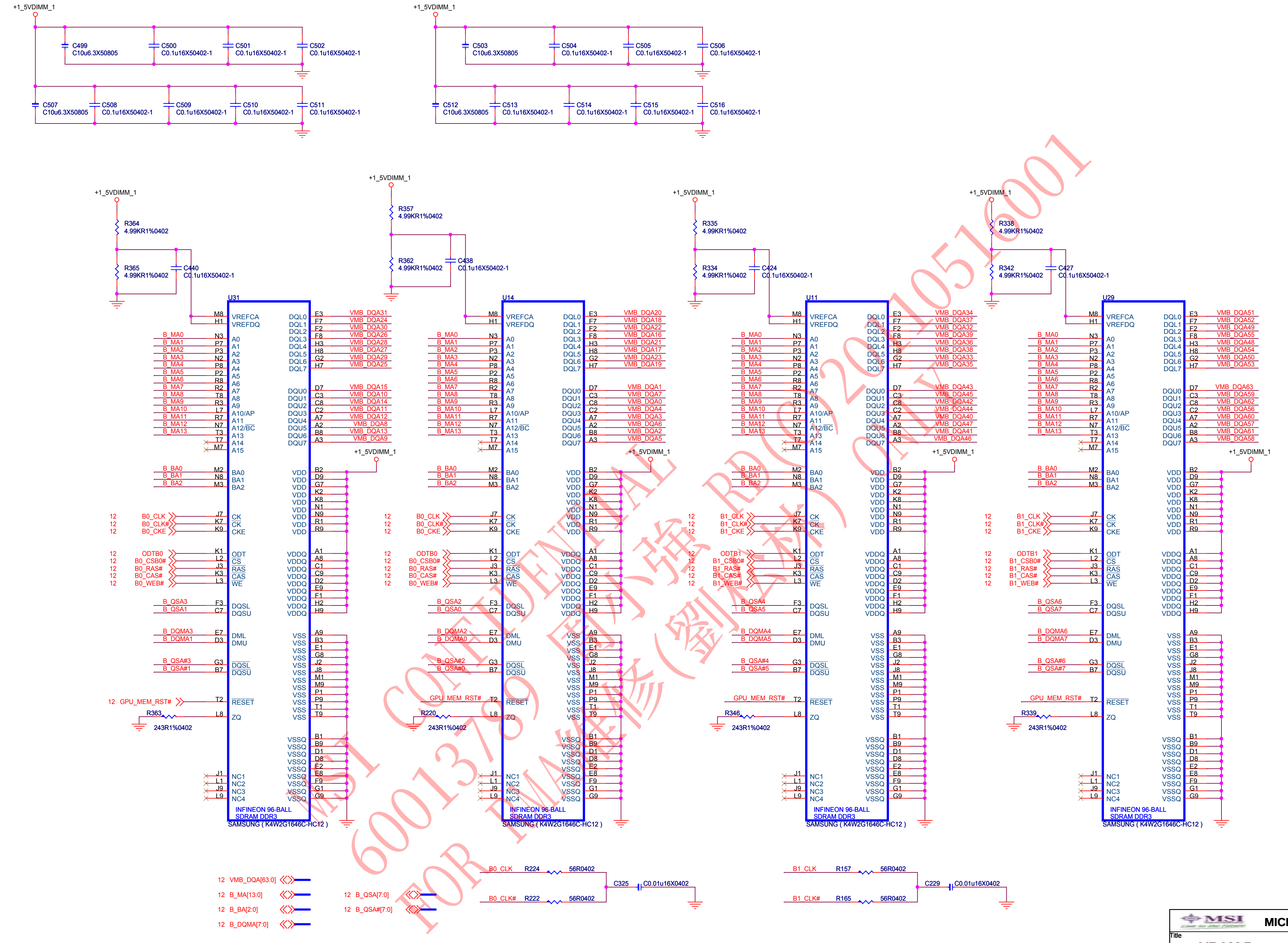

MICRO-STAR INT'L CO.,LTD.

Title	VRAM B	
Size: Custom	Document Number: MS-1482	Rev 1.0
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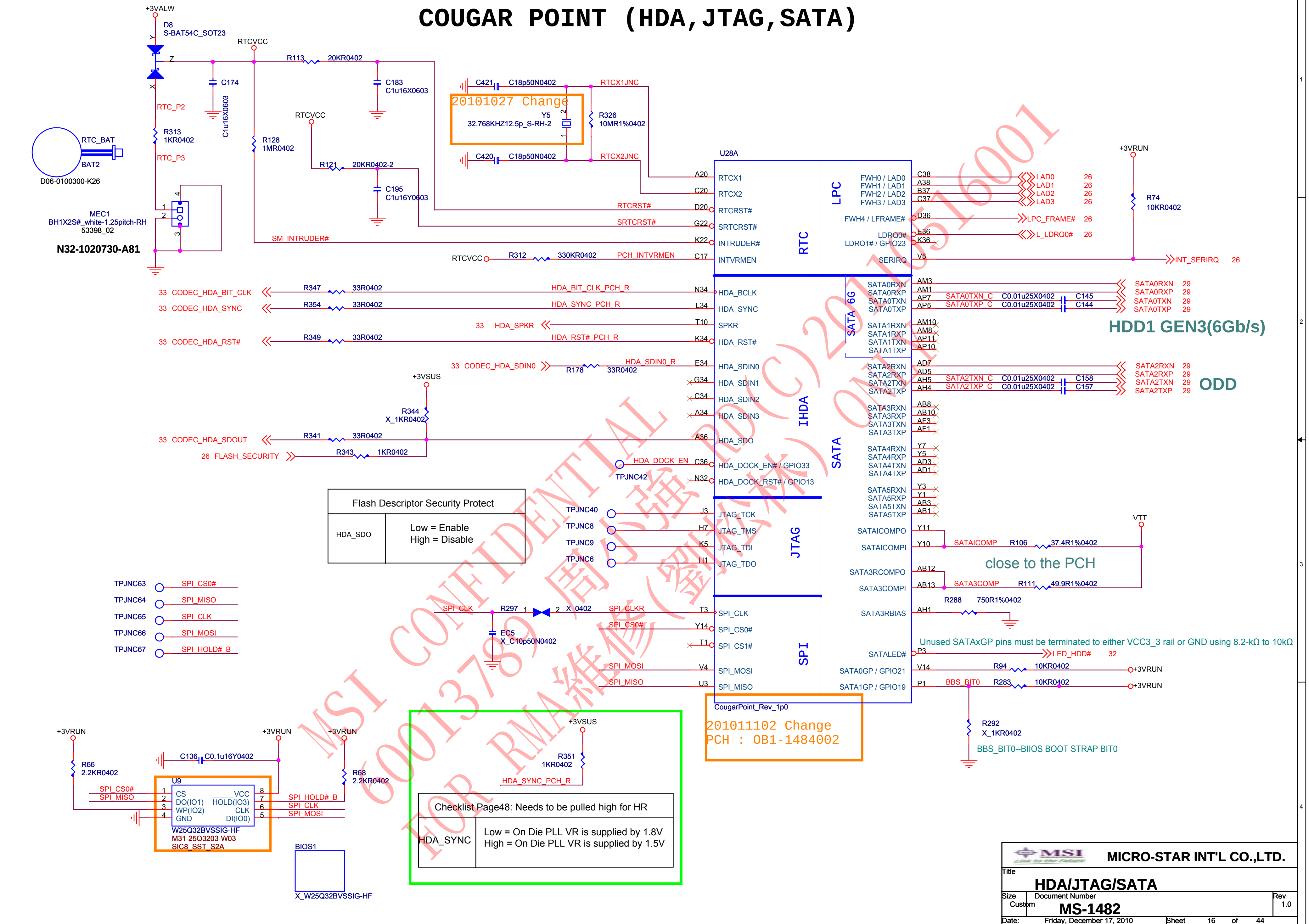
COUGAR POINT (HDA,JTAG,SATA)



Flash Descriptor Security Protect

HDA_SDO	Low = Enable High = Disable

Checklist Page48: Needs to be pulled high for HR

HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V

MICRO-STAR INT'L CO.,LTD.

Title	HDA/JTAG/SATA	
Size: Custom	Document Number: MS-1482	Rev: 1.0
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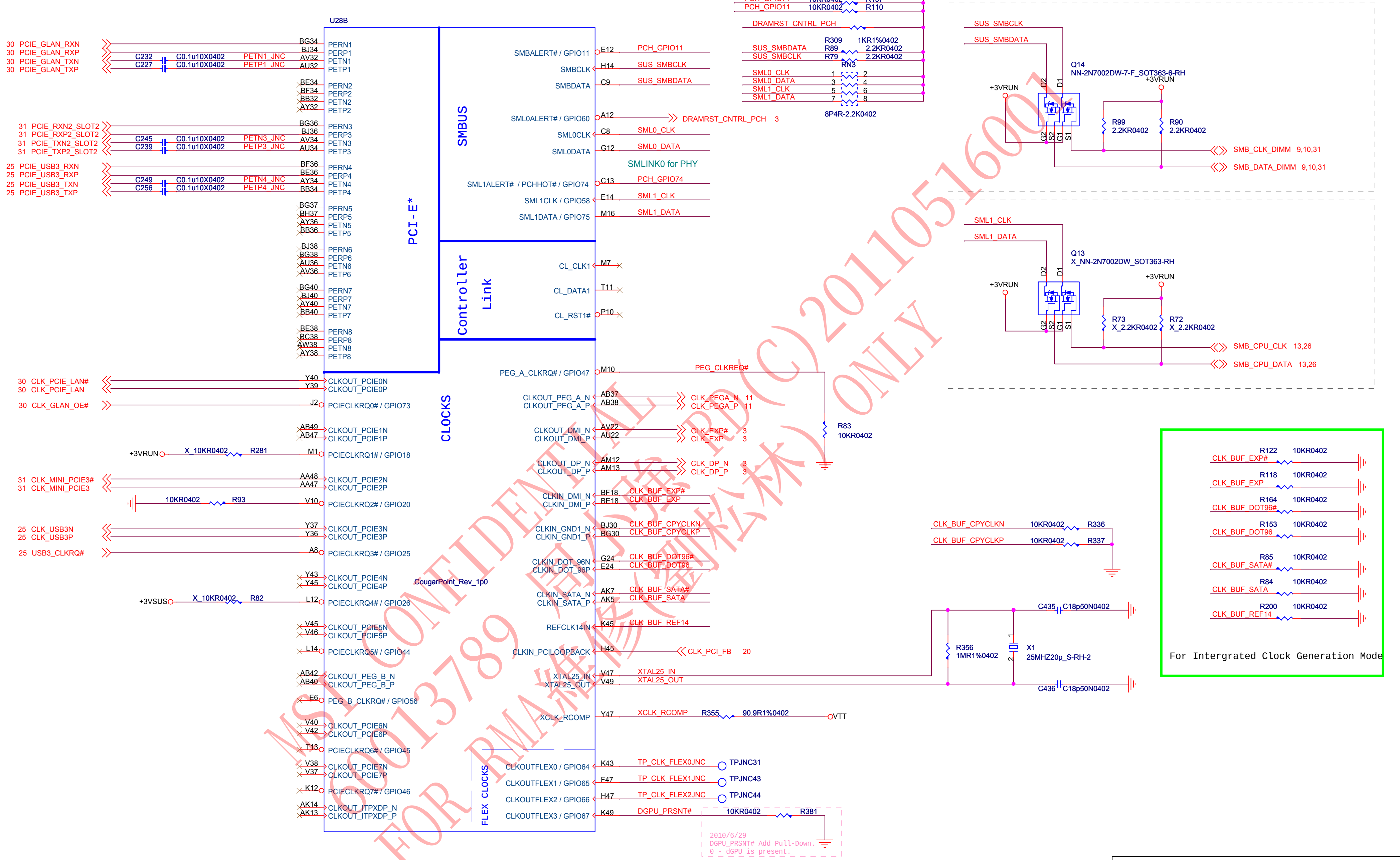
COUGAR POINT (PCI-E,SMBUS,CLK)



MICRO-STAR INT'L CO.,LTD.

Title	PCI-E/SMBUS/CLK
Size	Custom
Document Number	MS-1482
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Date:	Friday, December 17, 2010
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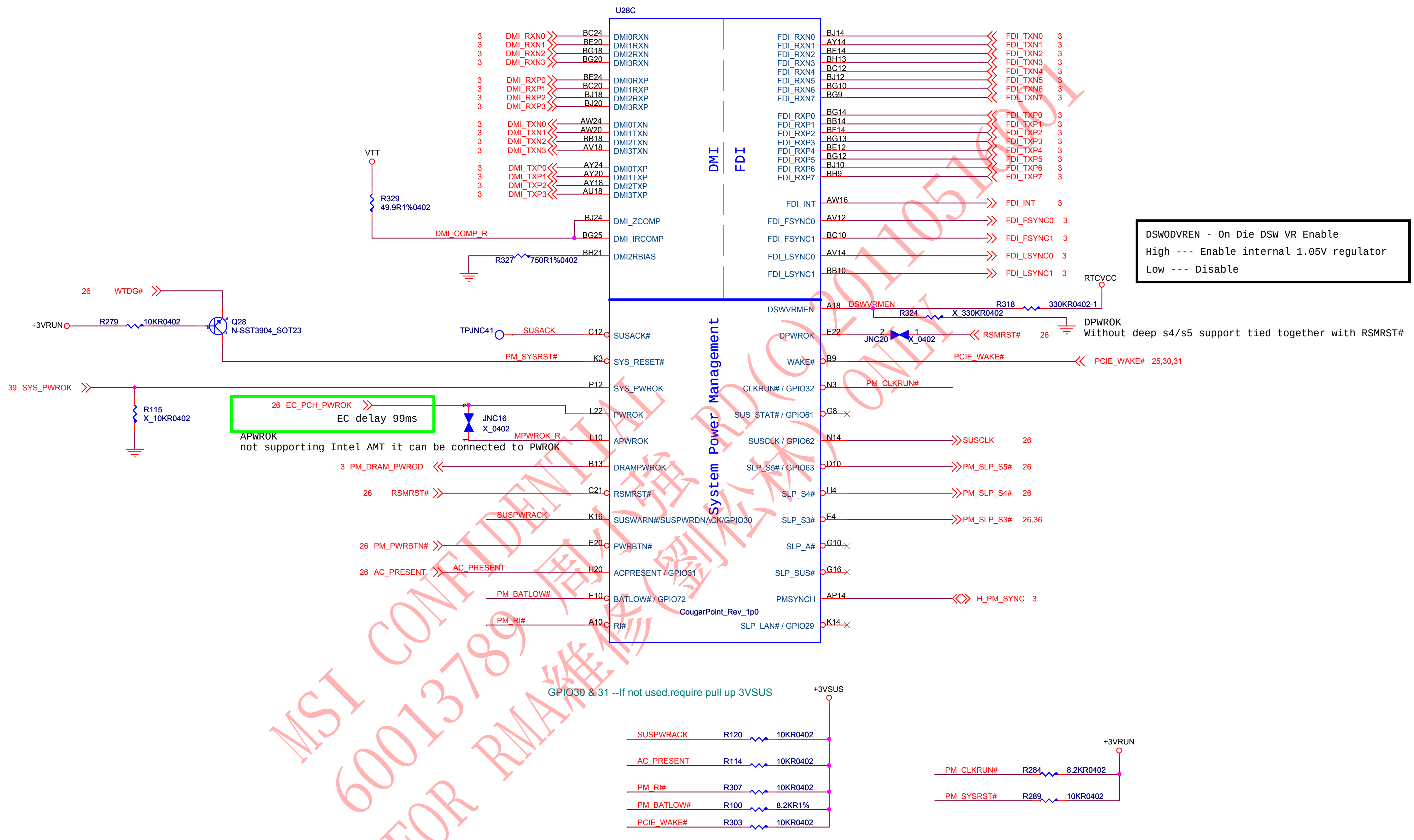
COUGAR POINT (DMI,FDI,GPIO)



DSWODVREN - On Die DSW VR Enable
High --- Enable internal 1.05V regulator
Low --- Disable

MICRO-STAR INT'L CO.,LTD.

Title	DMI/FDI/GPIO	
Size: Custom	Document Number: MS-1482	Rev: 1.0
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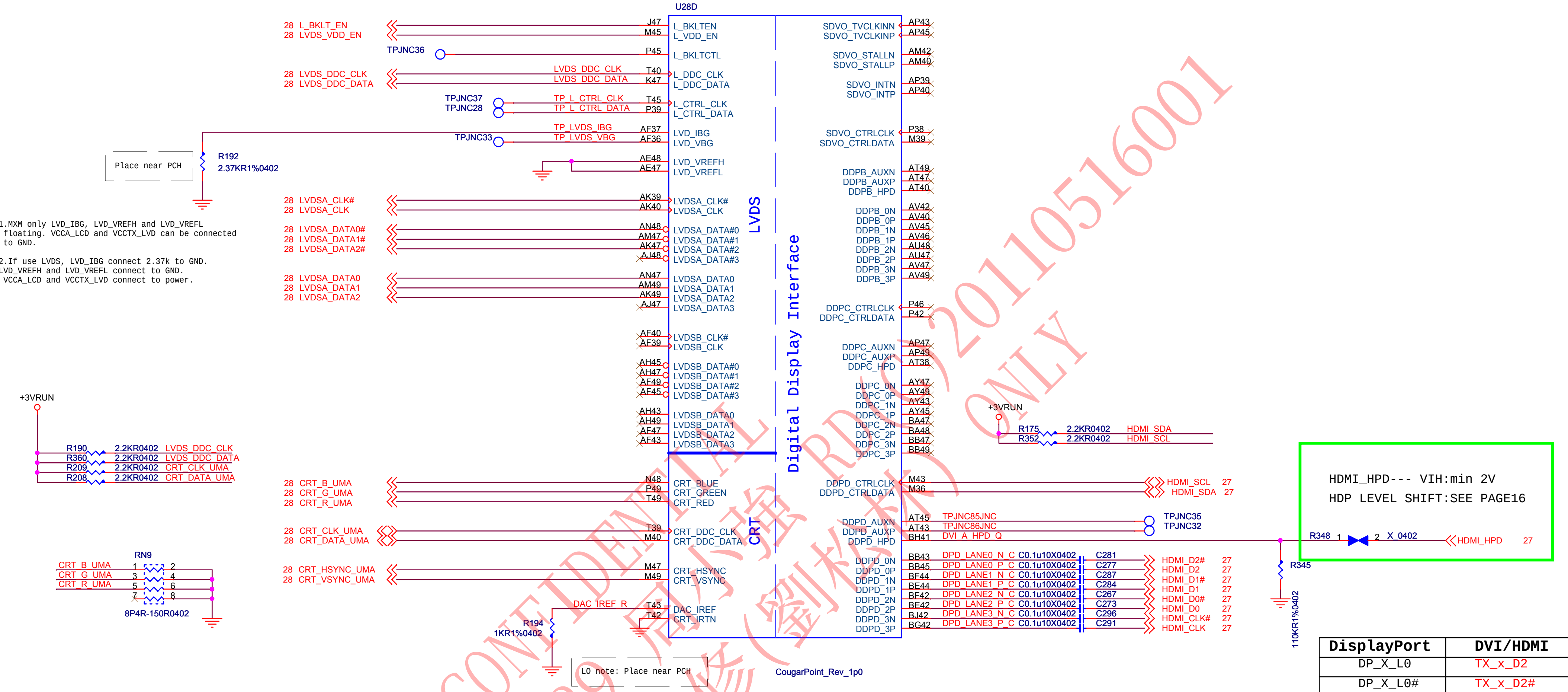
COUGAR POINT (LVDS,DDI)

1.MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.

2.If use LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

MICRO-STAR INT'L CO.,LTD.

Title: PCH_LVDS/DDI

Size: Custom | Document Number: MS-1482 | Rev 1.0

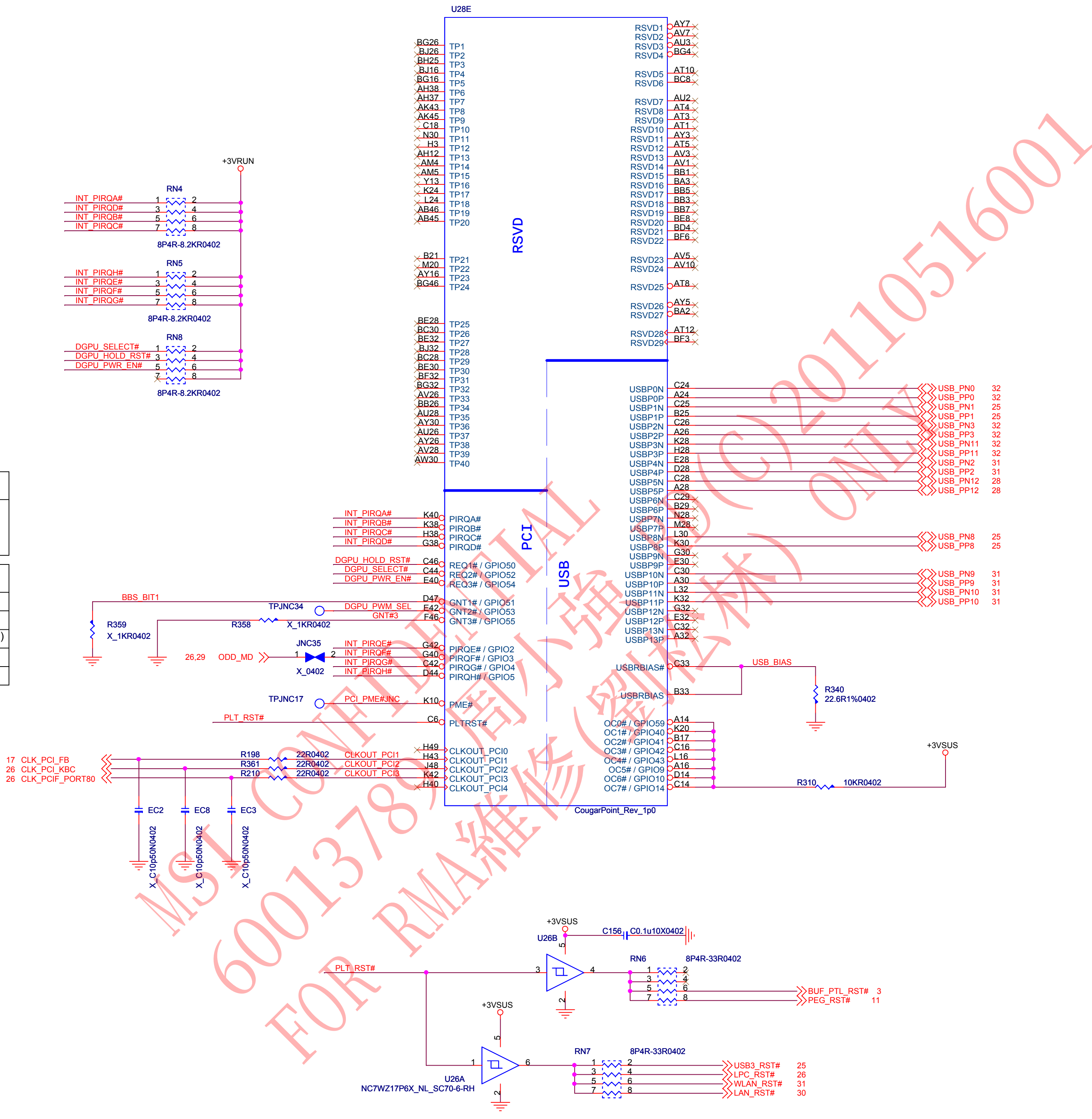
Date: Friday, December 17, 2010 |

COUGAR POINT (PCI,USB,NVRAM)

A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	_
1	1	SPI



MICRO-STAR INT'L CO.,LTD.

Title: PCH_PCI/USB/NVRAM

Size: Custom | Document Number: MS-1482 | Rev 1.0

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GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN

GPIO57 --If not used,require pull up 3VSUS

GPIO15--High is support TLS,internal pull-down

GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin

GPIO35 --Define to EDID Select (If not used,require pull down)

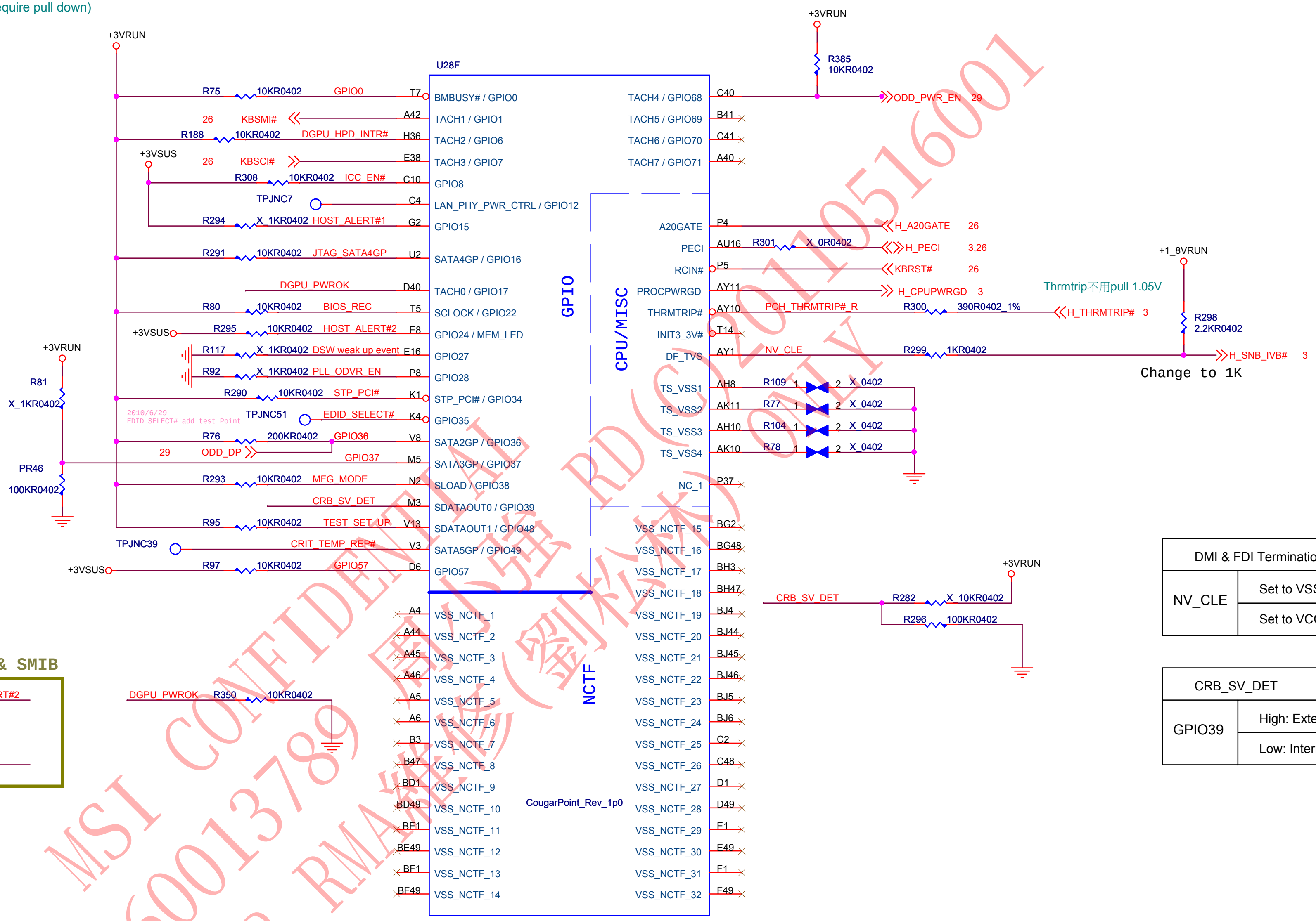
COUGAR POINT (GPIO,VSS_NCTF,RSVD)

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

GPIO36 --CRB connector to 3V

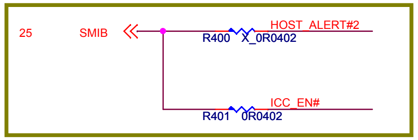
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default



DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

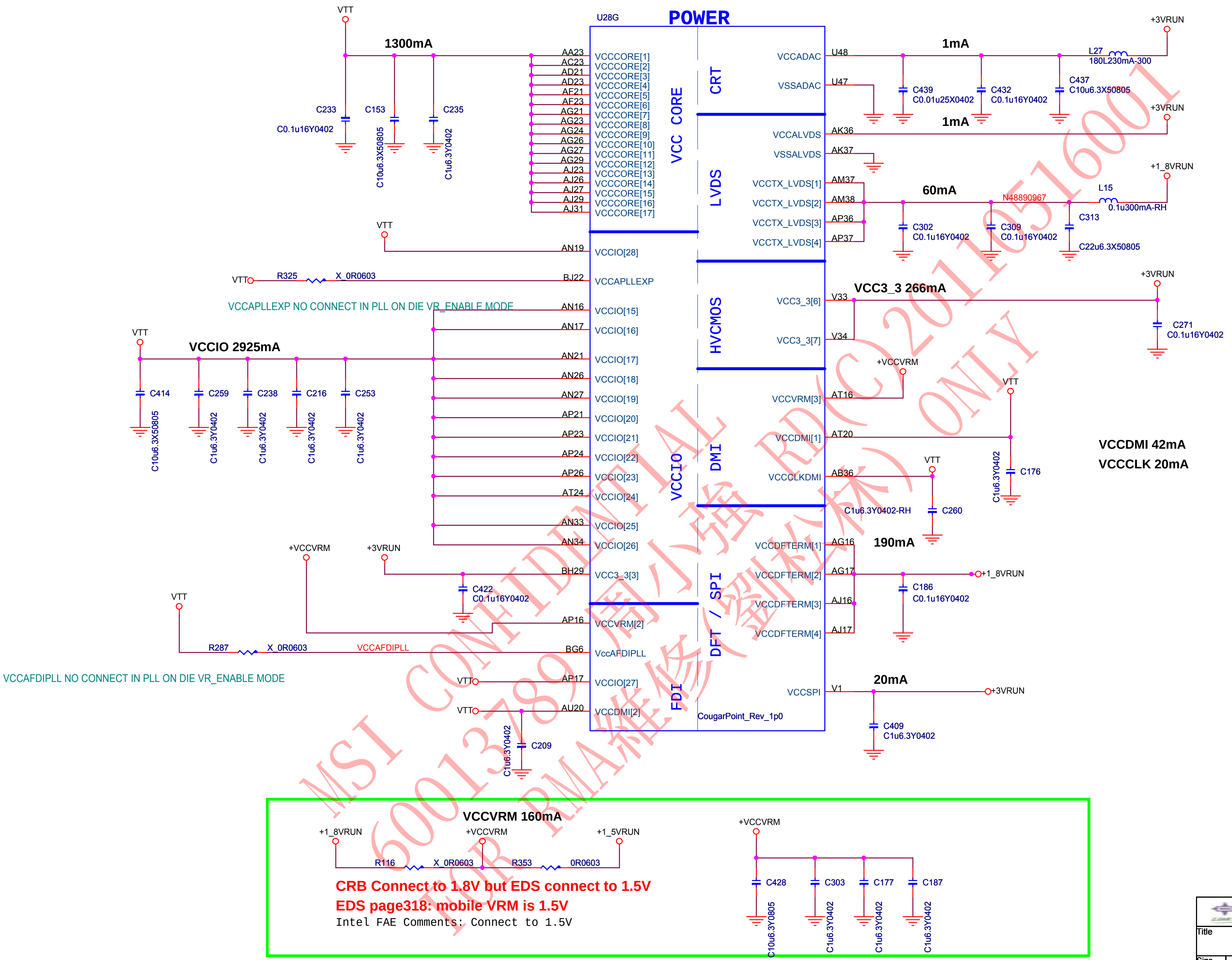
CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX

2010/12/8
add HOST_ALERT#2, ICC_EN# & SMIB



MICRO-STAR INT'L CO.,LTD.		
Title: PCH_GPIO/NCTF/RSVD		
Size: Custom	Document Number: MS-1482	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 21 of 44	

COUGAR POINT (POWER)



MSI MICRO-STAR INT'L CO.,LTD.

Title	PCH_POWER
Size	Custom
Document Number	MS-1482
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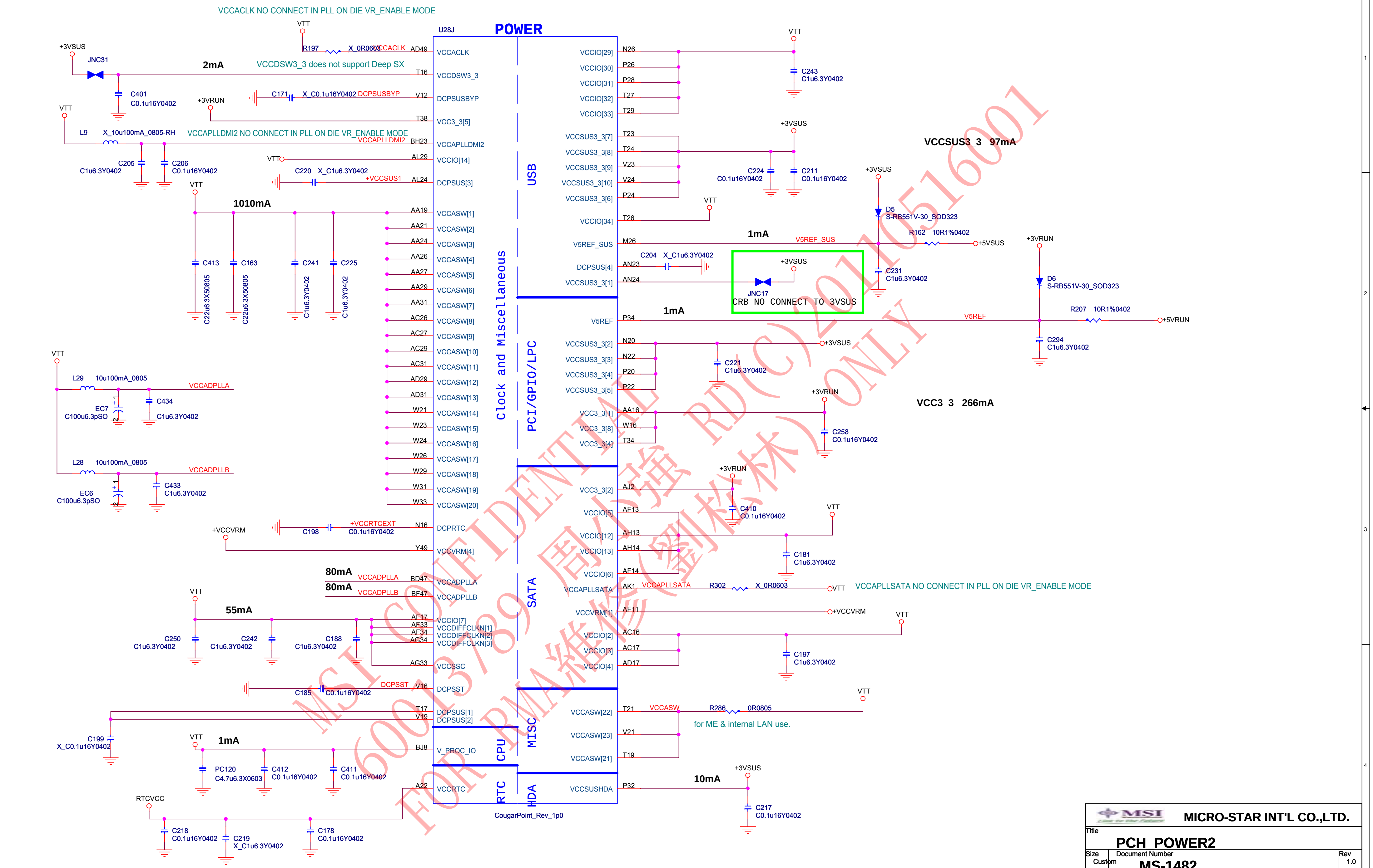
COUGAR POINT (POWER)



MICRO-STAR INT'L CO.,LTD.

Title	PCH_POWER2	
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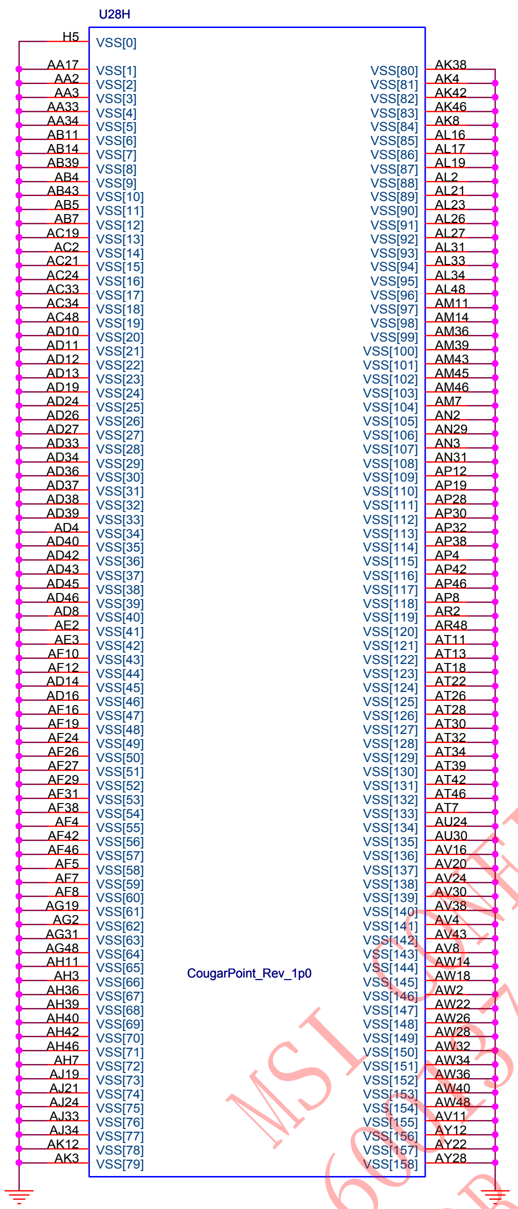
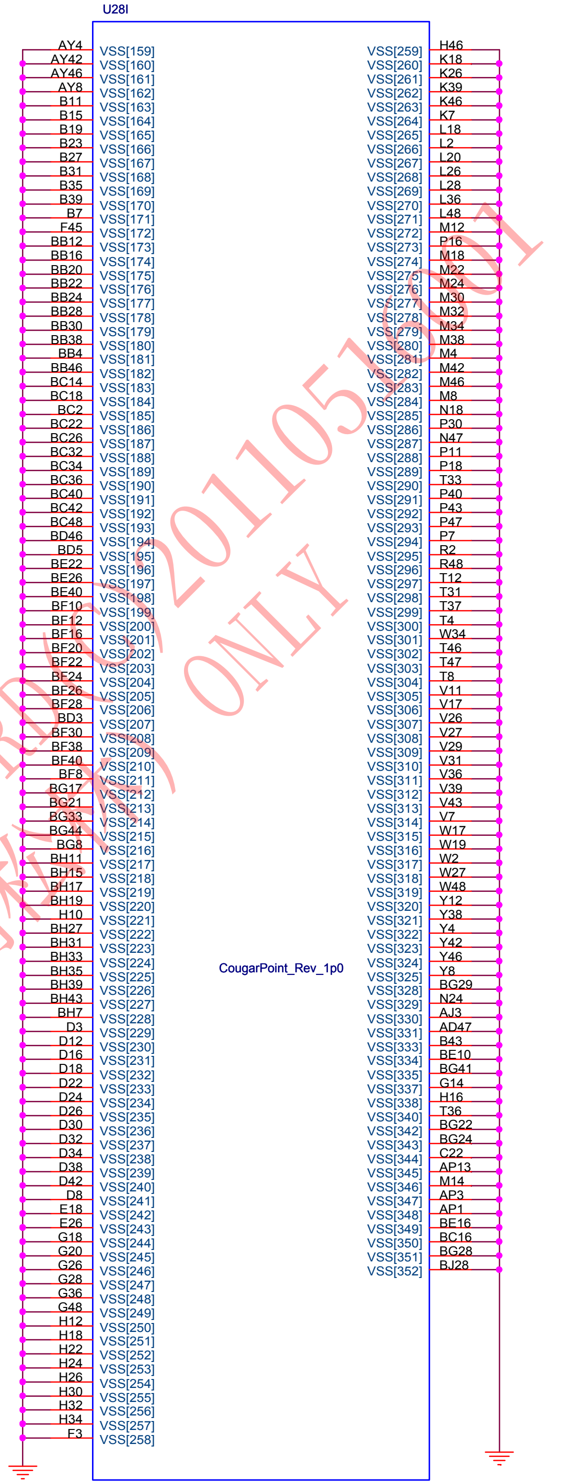
Cougar Point (GND)





MICRO-STAR INT'L CO.,LTD.

Title	PCH_GND	
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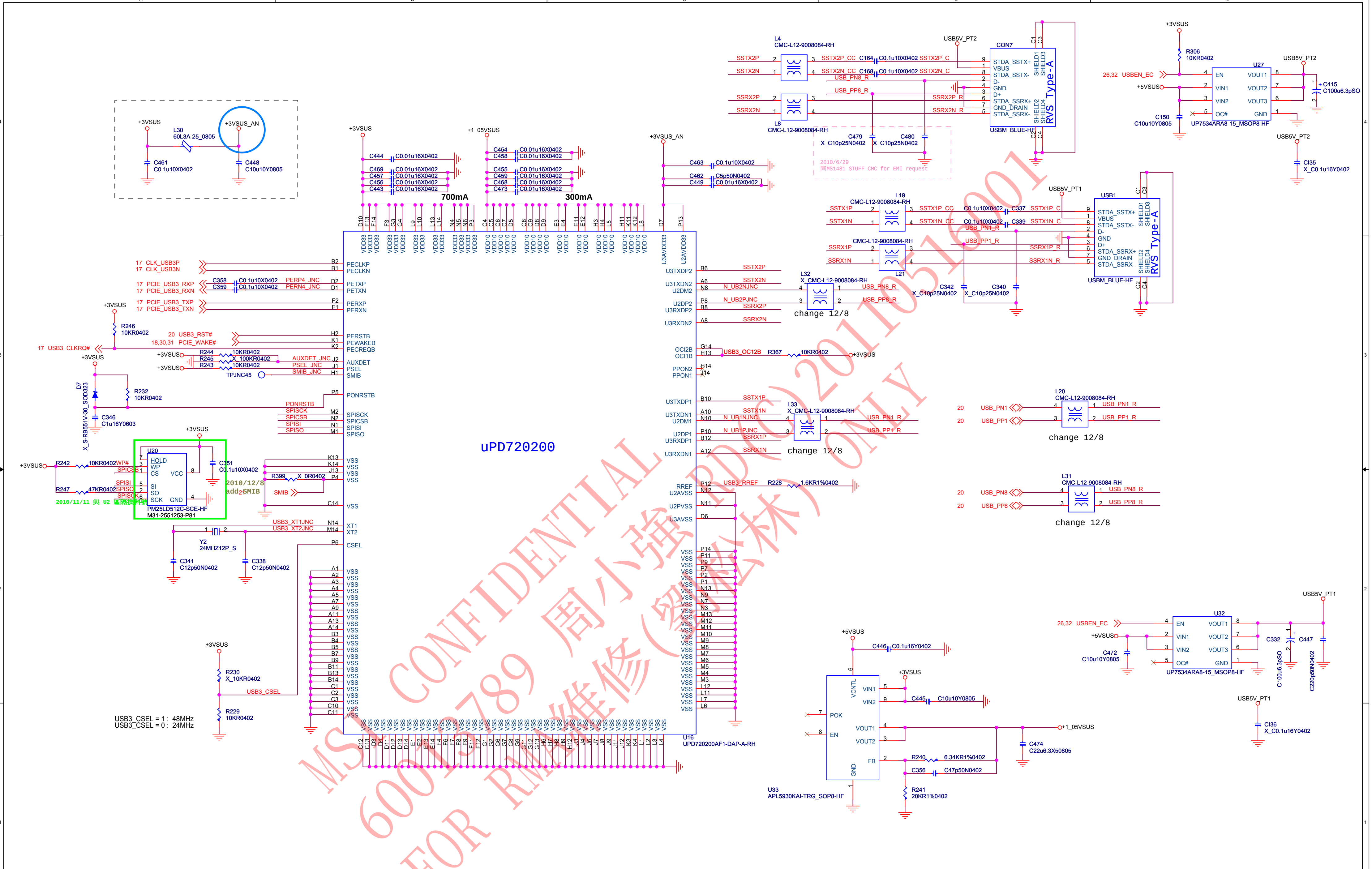

MICRO-STAR INT'L CO.,LTD.

Title: USB3.0 (uPD720200)

Size: Custom | Document Number: MS-1482 | Rev: 1.0

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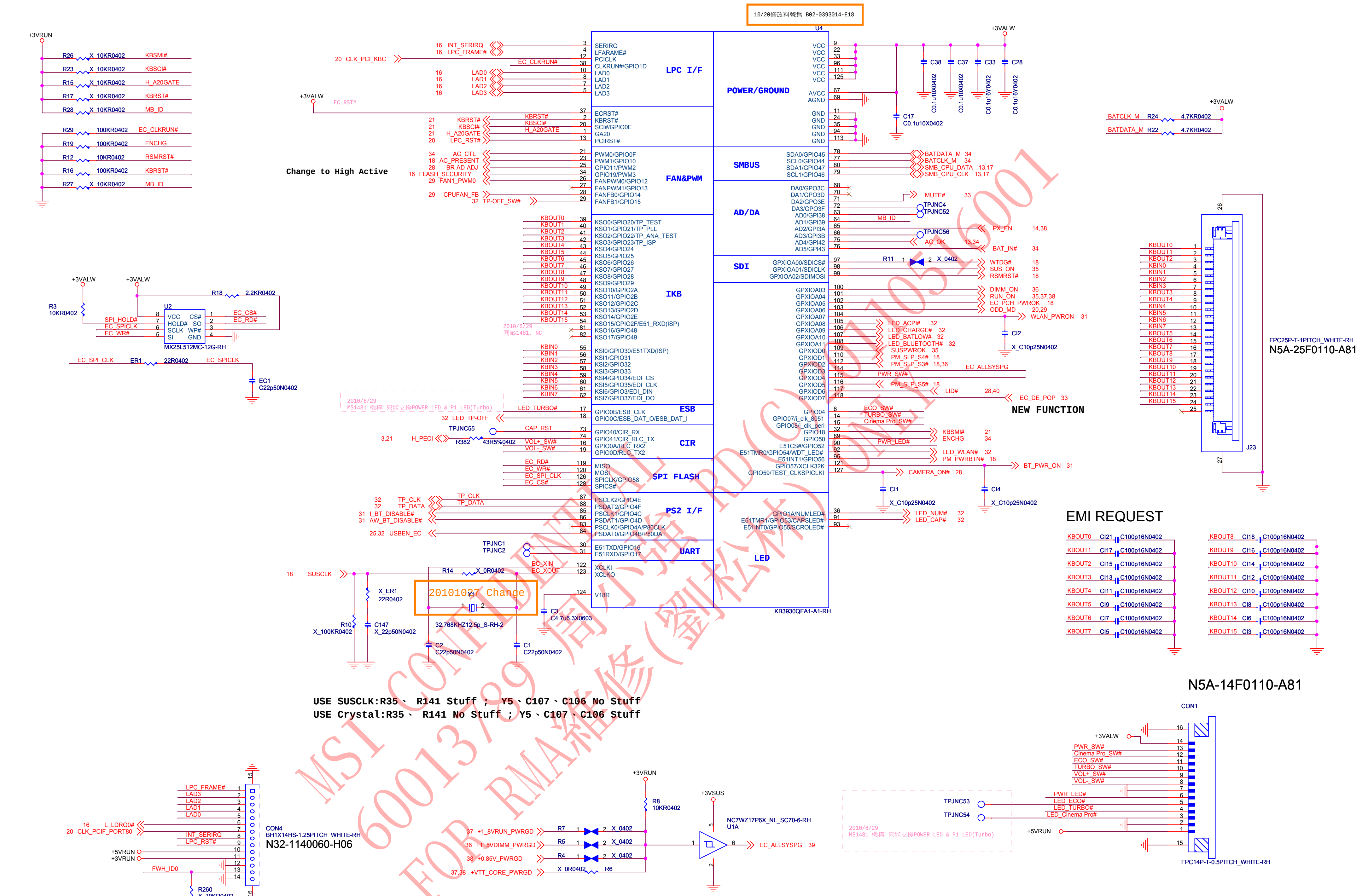
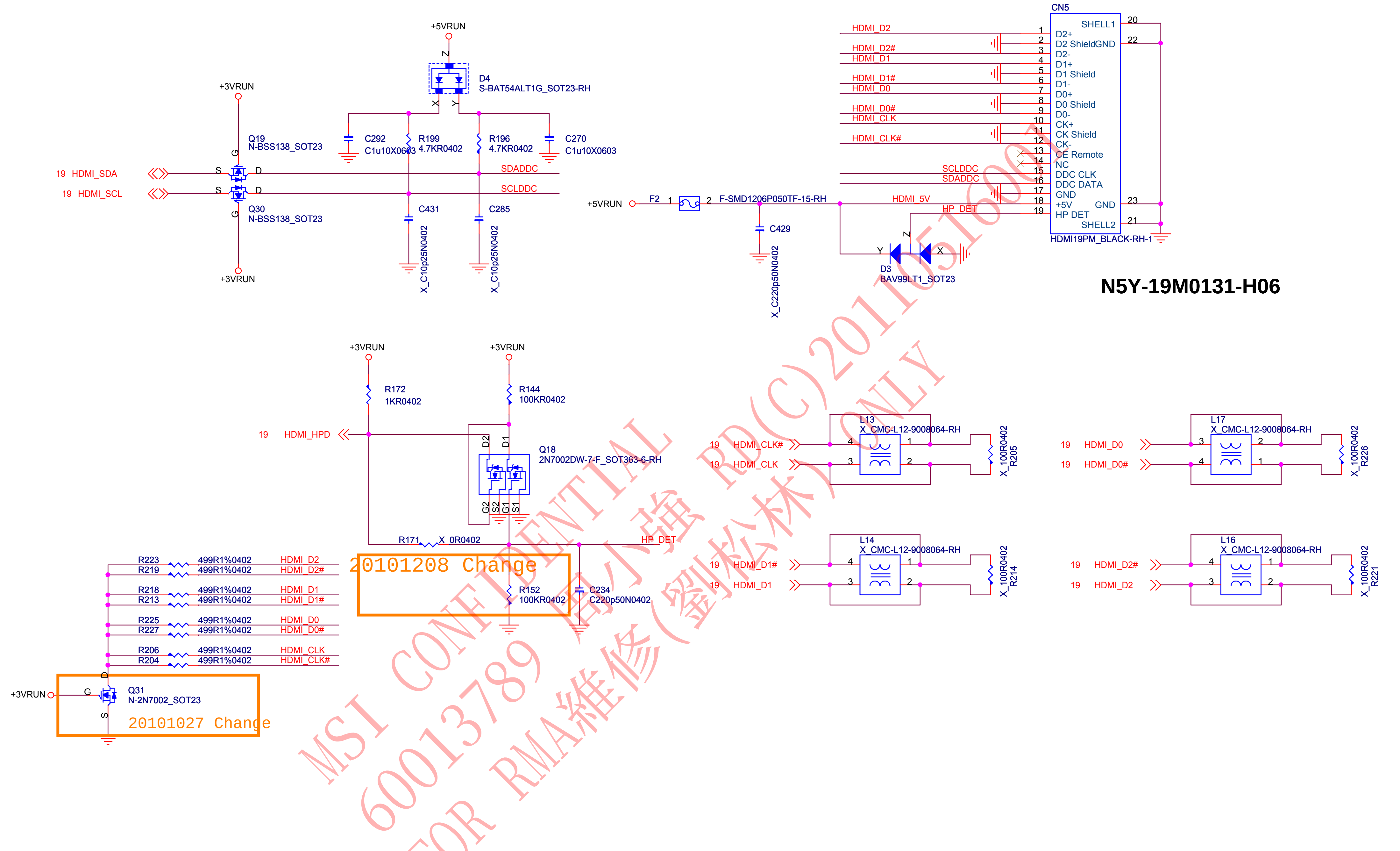


MICRO-STAR INT'L CO.,LTD.

Title	KBC 3930	
Size: Custom	Document Number: MS-1482	Rev: 1.0
Date: Friday, December 17, 2010	Sheet 26 of 44	



MICRO-STAR INT'L CO.,LTD.

Title: **HDMI**

Size	Document Number	Rev
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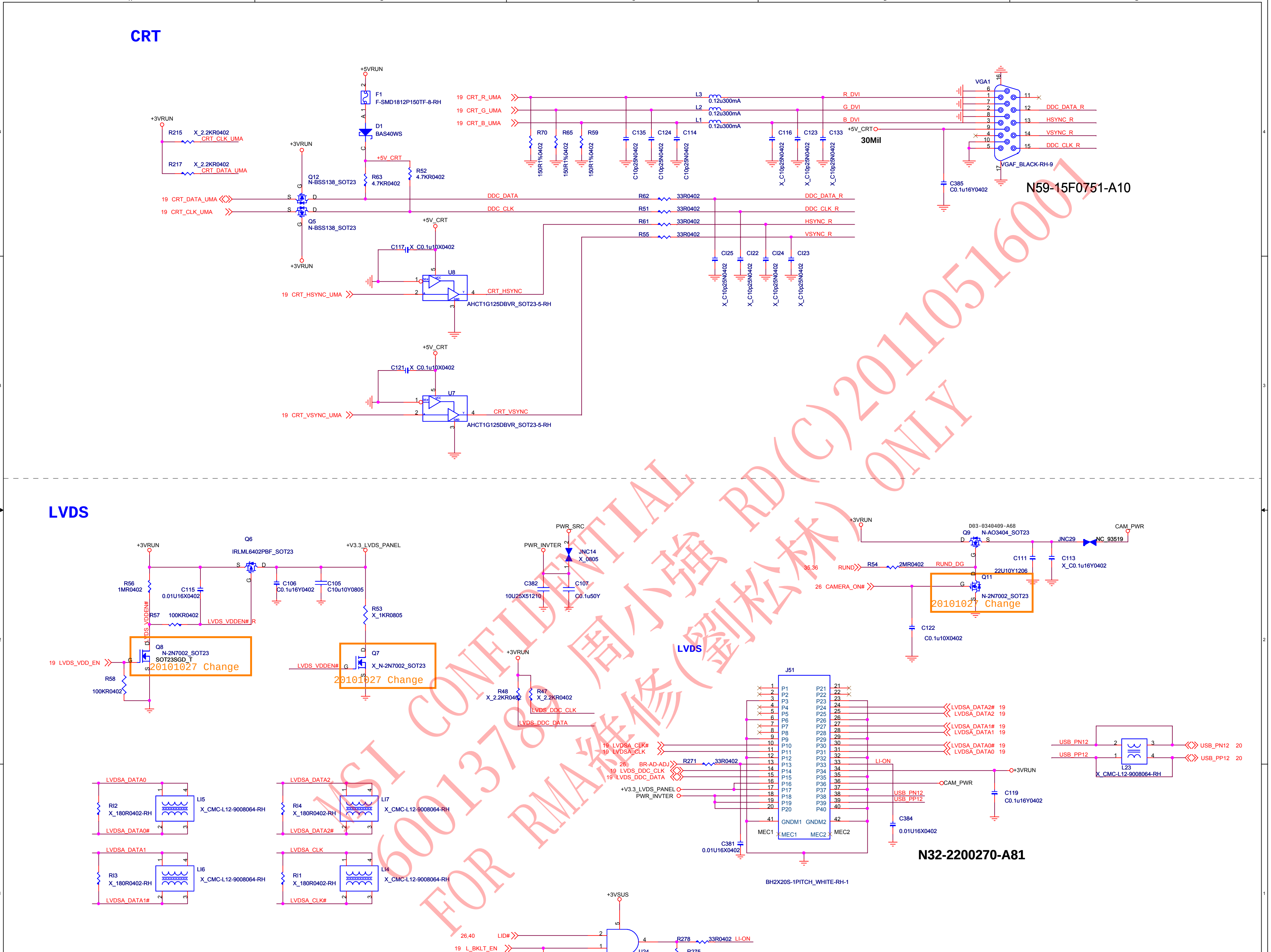

MICRO-STAR INT'L CO.,LTD.

Title	CRT,LVDS,CAMERA	
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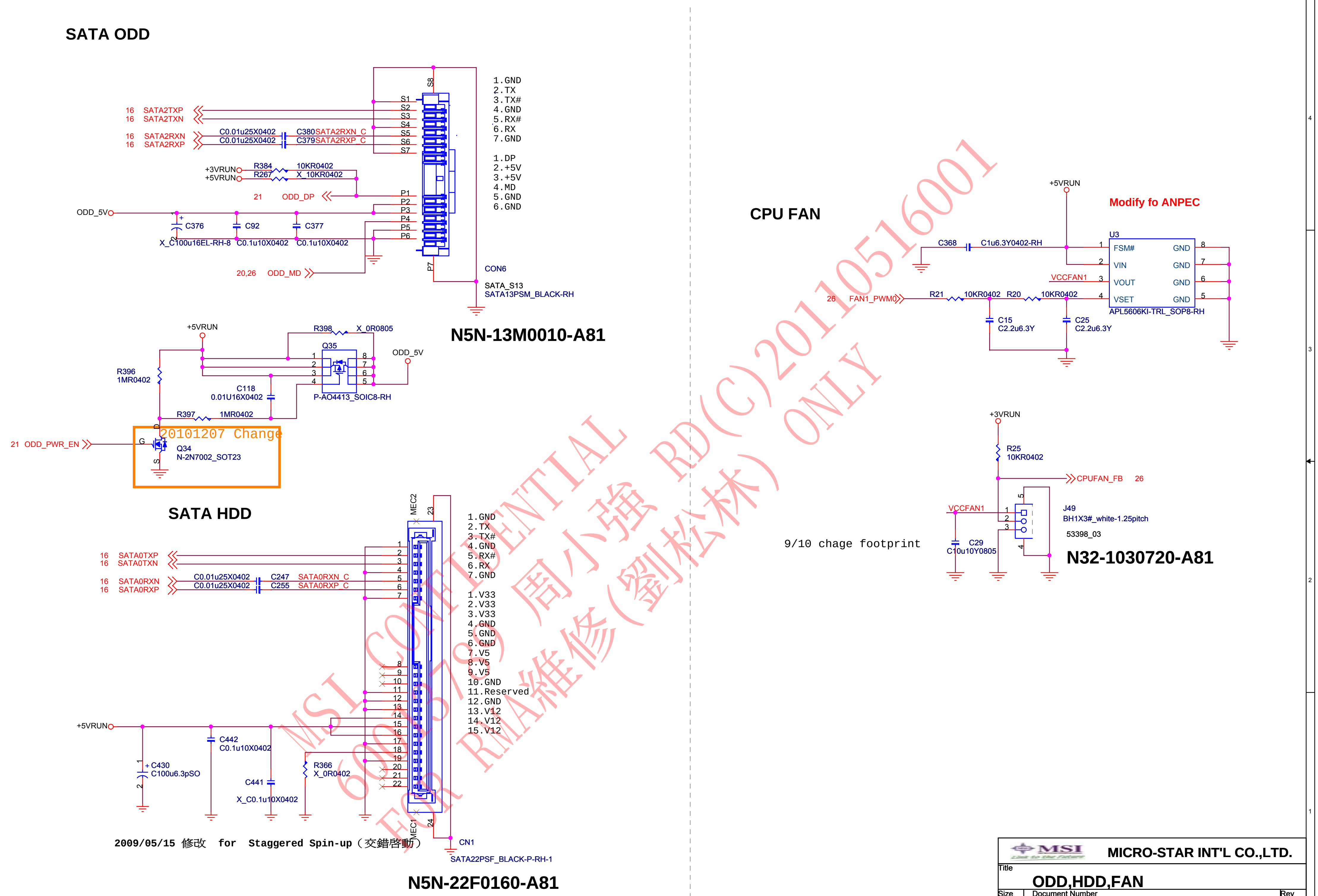
SATA ODD



MICRO-STAR INT'L CO.,LTD.

Title: ODD,HDD,FAN

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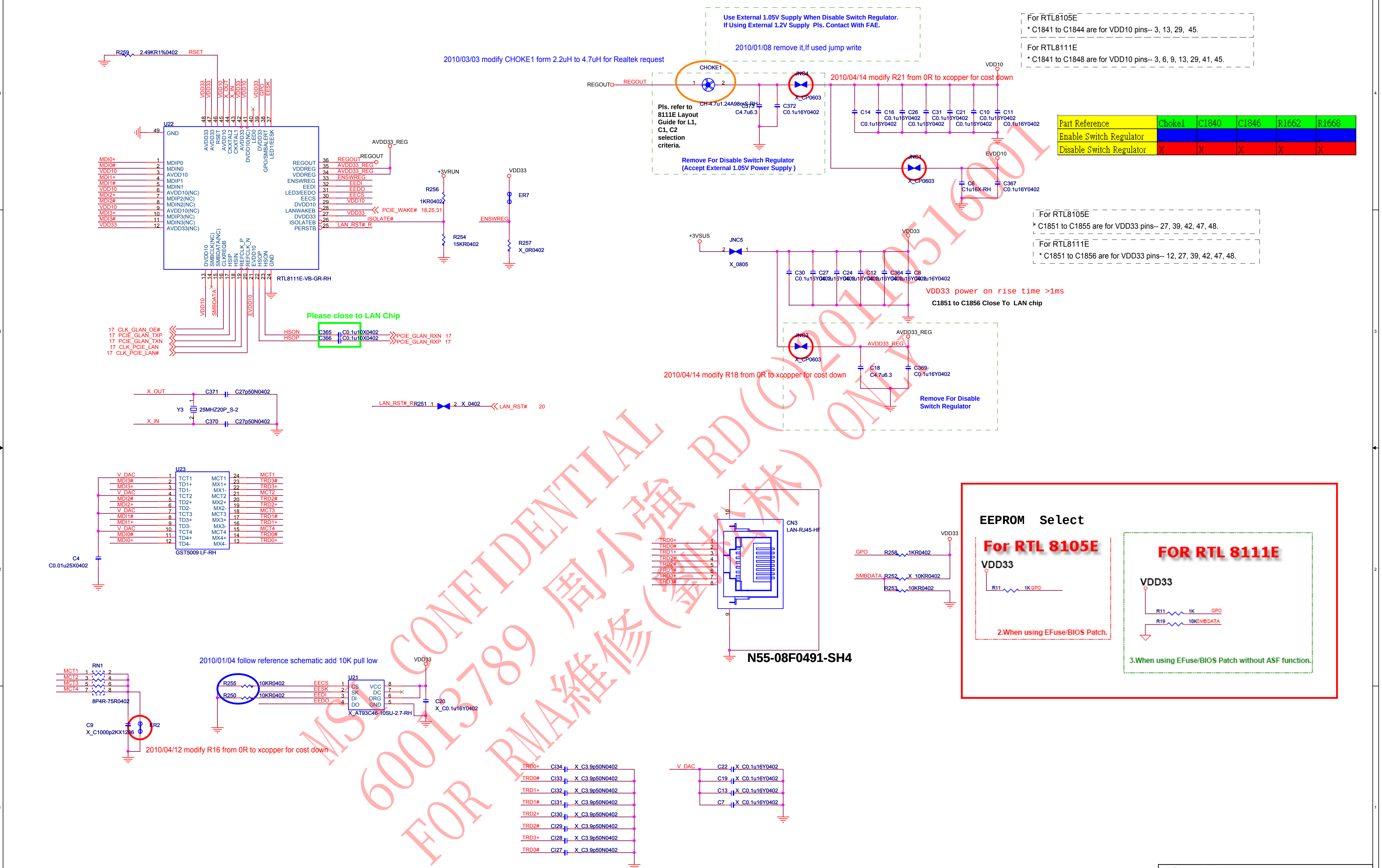
Note: add 0.1u cap at each power pin of LAN, please don't save.



MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(RTL 8111EL)

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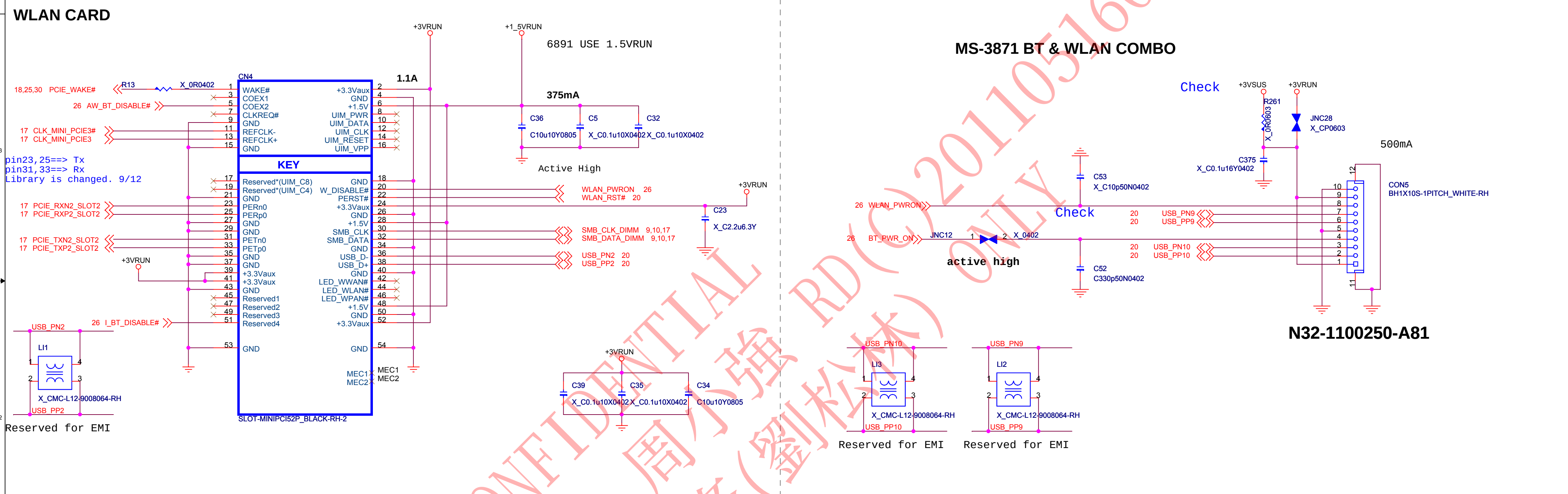
WLAN CARD

MS-3871 BT & WLAN COMBO



MICRO-STAR INT'L CO.,LTD.

Title: WLAN,BT,Combo

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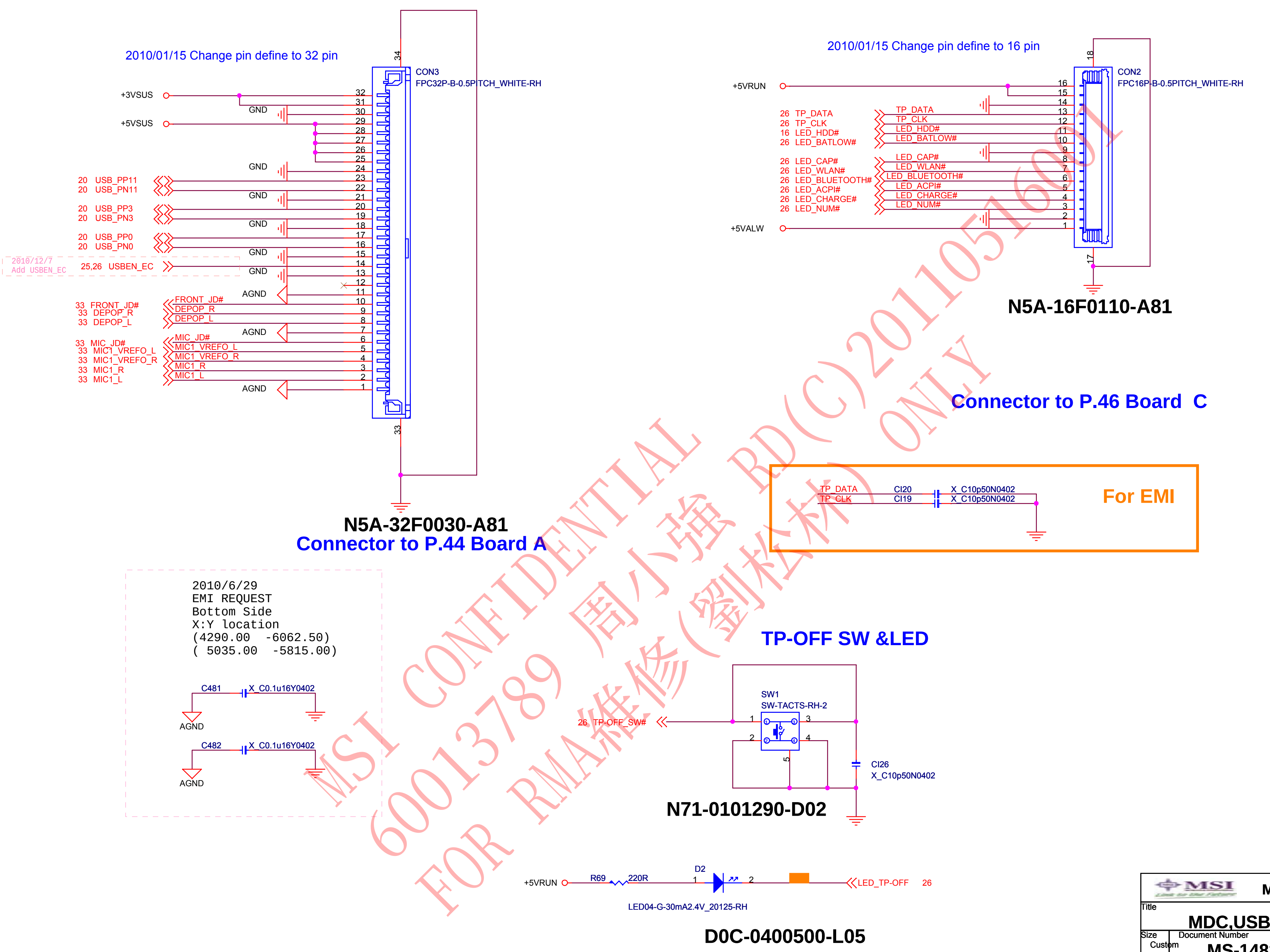
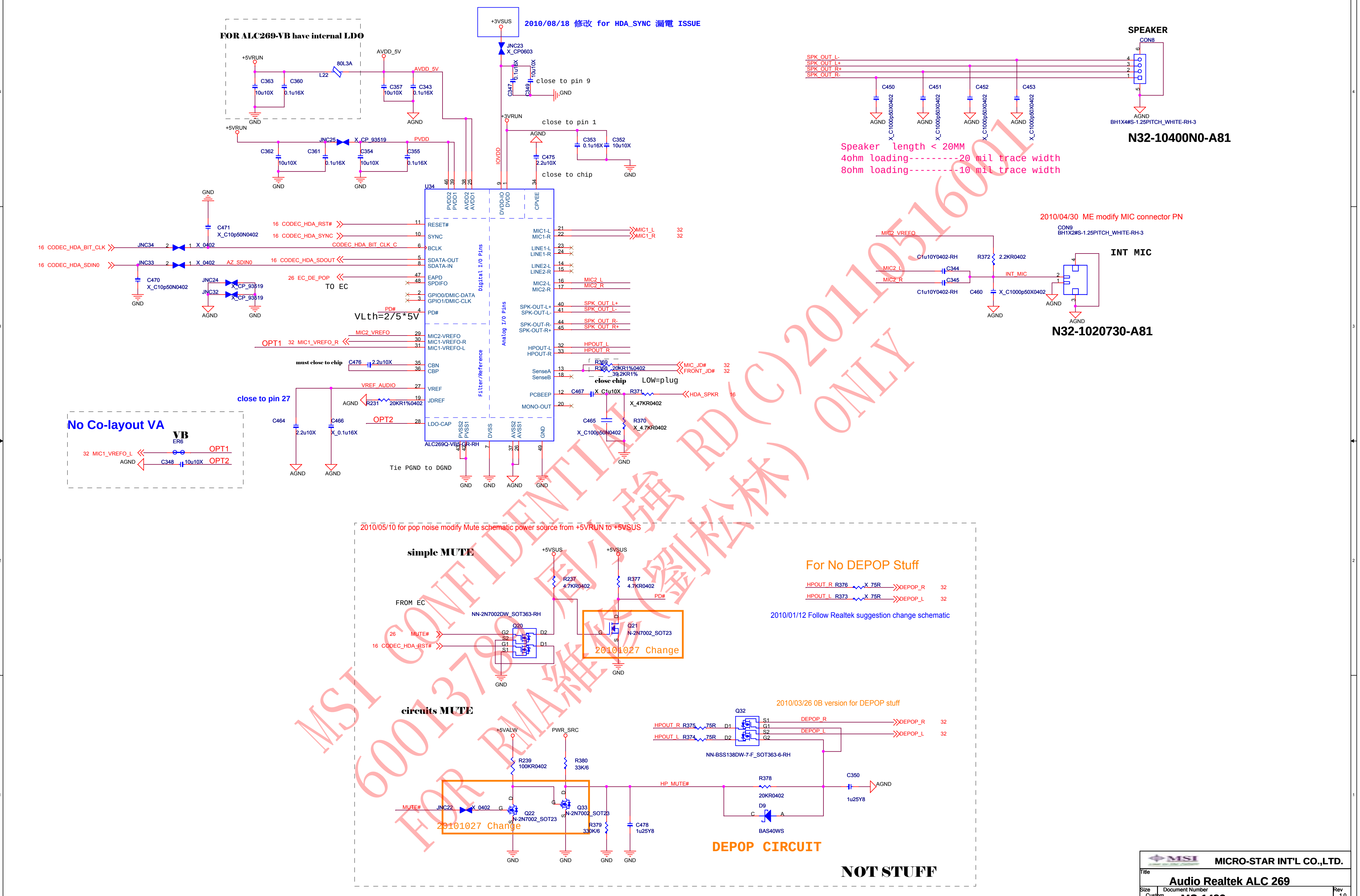


MICRO-STAR INT'L CO.,LTD.

Title: MDC,USB,CONN

Size	Document Number	Rev
Custom	MS-1482	1.0

Date: Friday, December 17, 2010



MICRO-STAR INT'L CO.,LTD.

Title: Audio Realtek ALC 269

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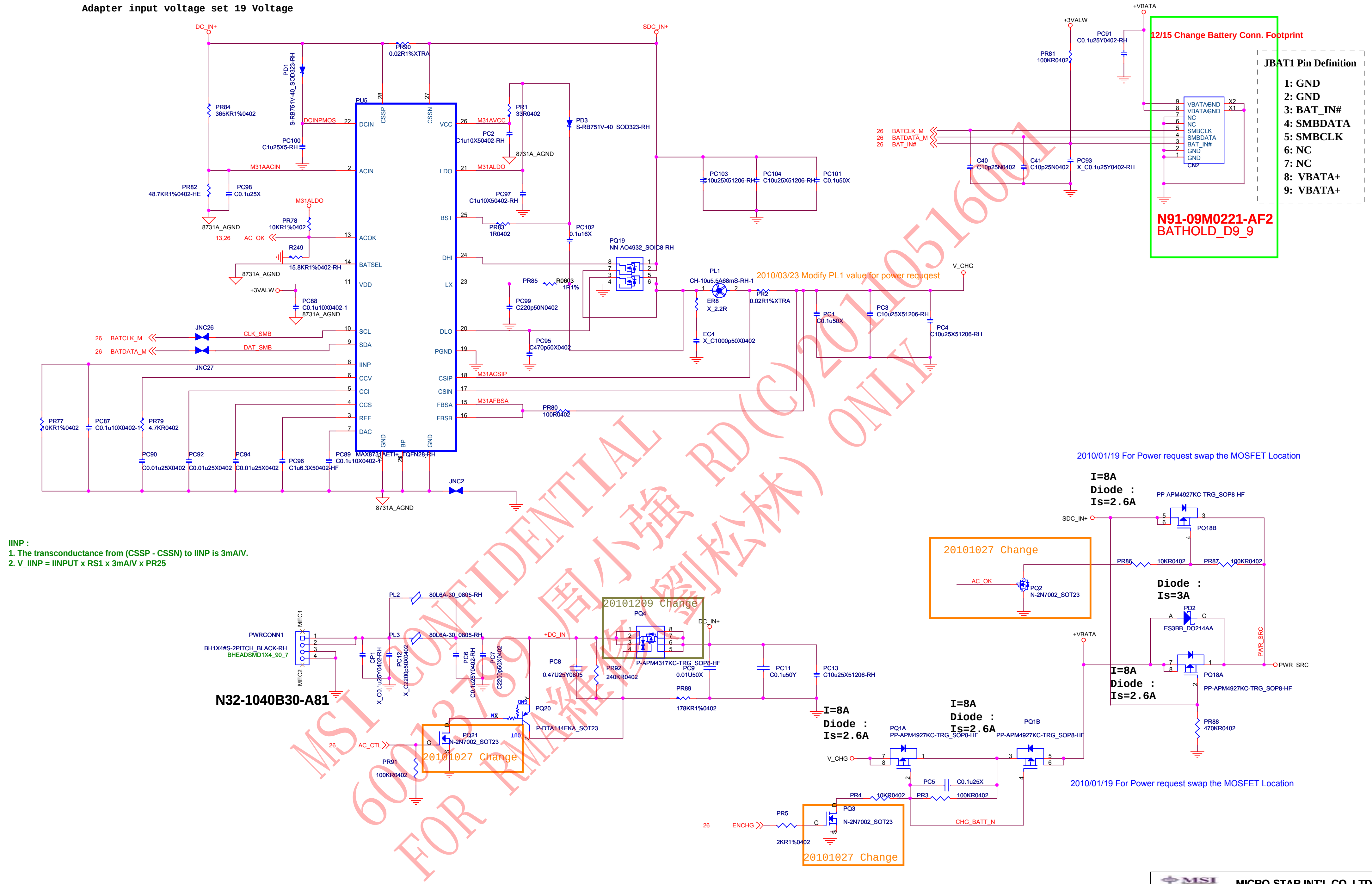

MICRO-STAR INT'L CO.,LTD.

Title: BATTERY SELETC/ CHARGER

Size	Document Number	Rev
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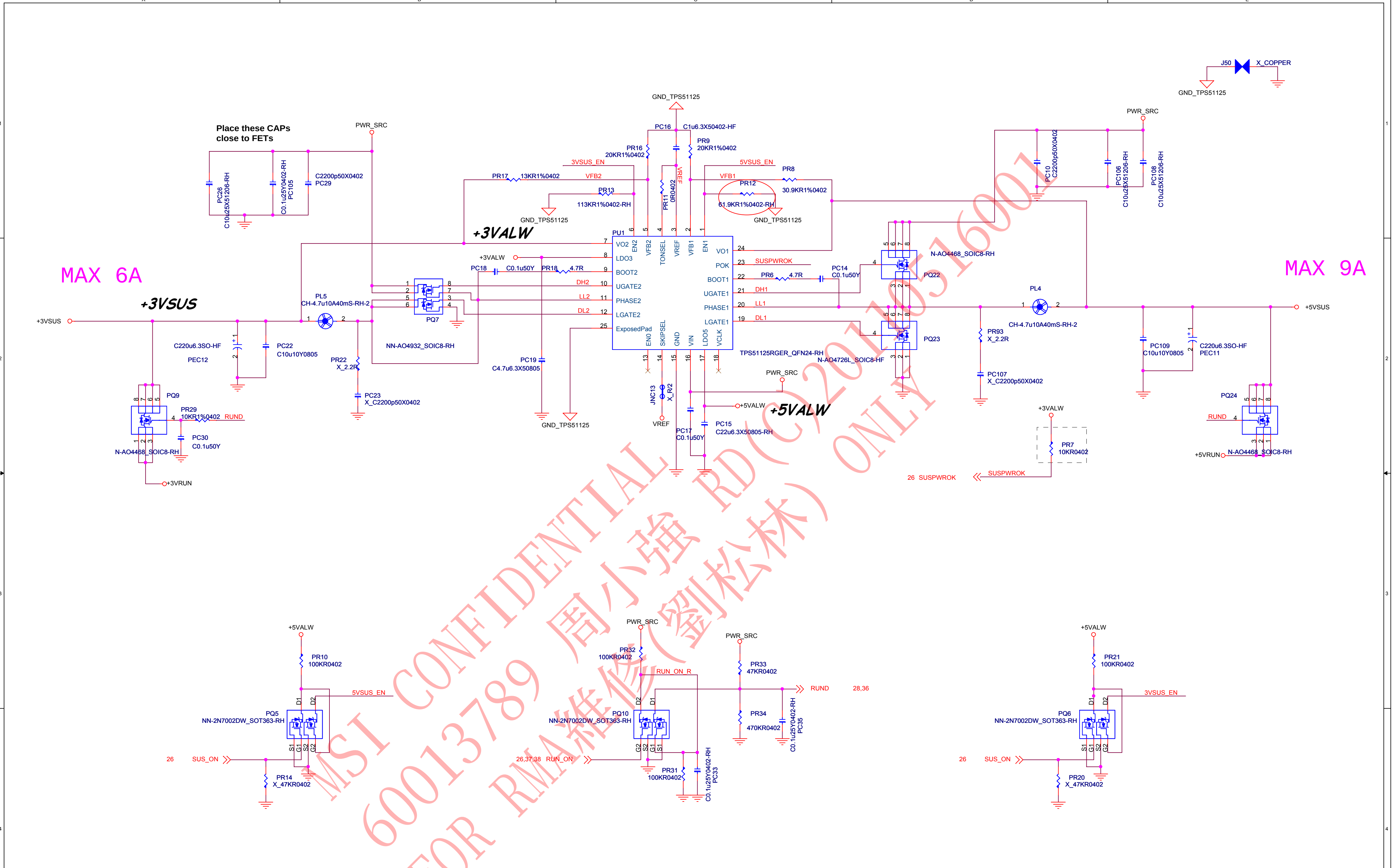

MICRO-STAR INT'L CO.,LTD.

Title	SYSTEM POWER	
Size Custom	Document Number MS-1482	Rev 1.0
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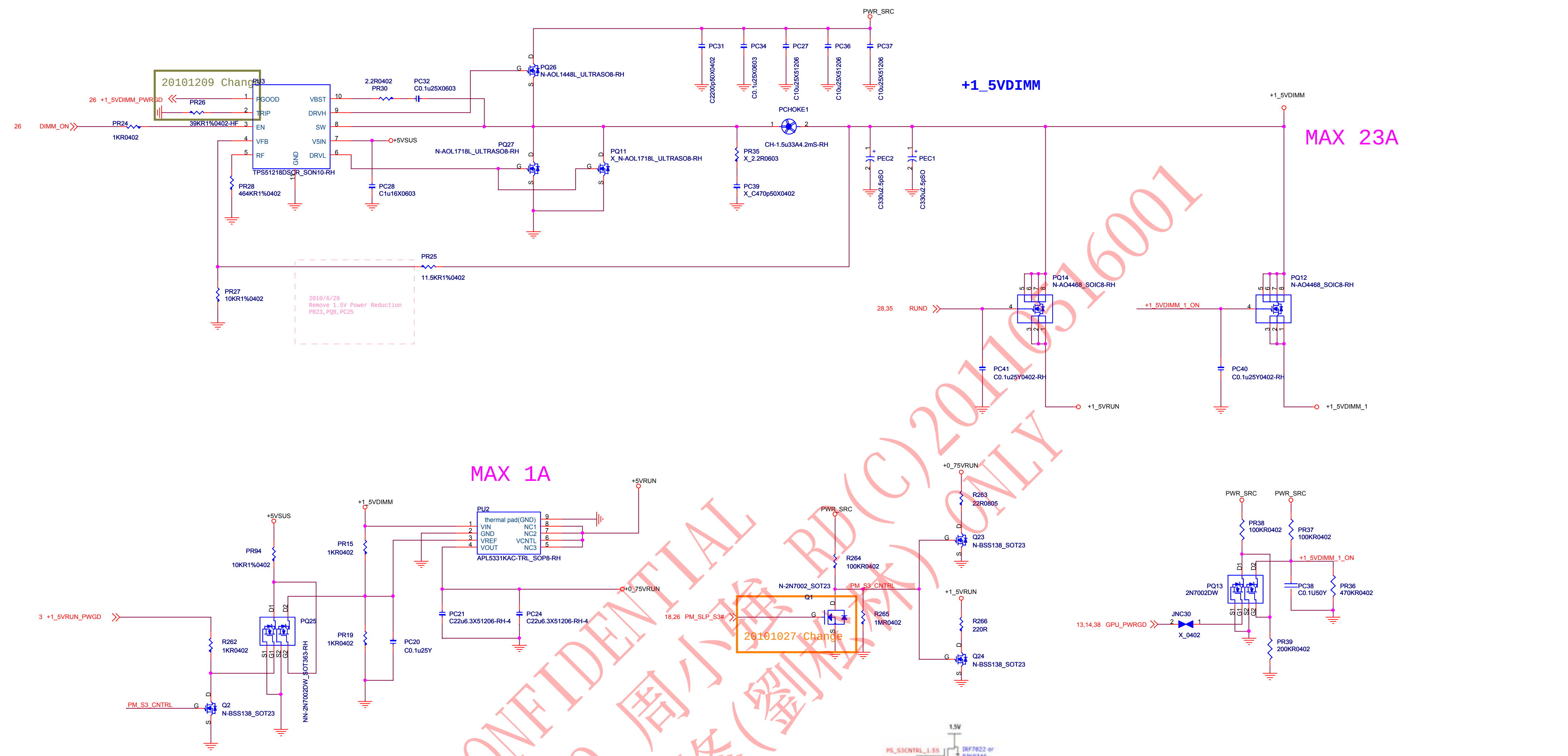
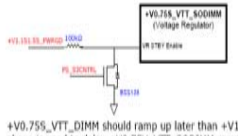
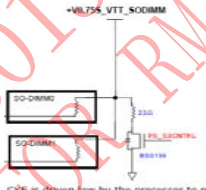


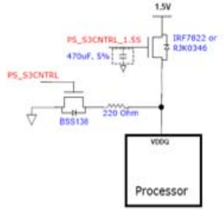


+V0.75S_VTT_DIMM should ramp up later than +V1.5S_CPU_VDDQ. Circuit shown above is used to delay +V0.75V_VTT_SODIMM ramp with respect to +V1.5S_CPU_VDDQ.

100-kΩ isolation resistor is used in reference design so that when gate is turned on, it does not pull +V1.151.5S_PWRGD signal to low which may impact other functionality on the board. To ensure +V1.151.5S_PWRGD signal levels maintained, comparator pull-up has been changed from 100 kΩ to 1 kΩ (R2F2 in Intel CRB schematic).

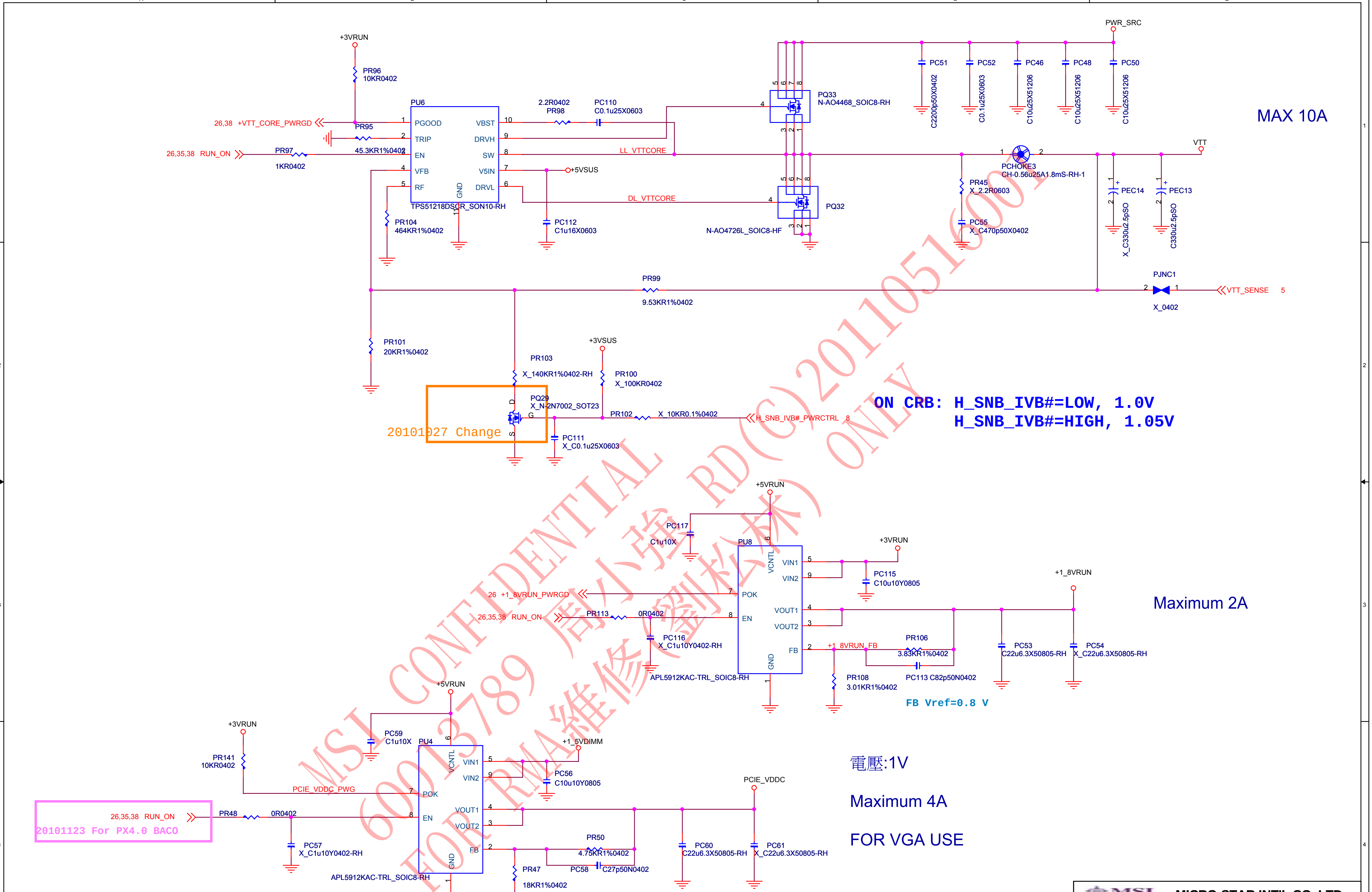


CKE is driven low by the processor to put the memory in self refresh while entering S3. When the processor +V1.5_CPU_VDDQ power is turned off, the discharge path on +V0.75S ensures CKE stays low during S3. To avoid any glitch on CKE signals during S3 entry, faster (22 Ω) discharge circuitry ensures +V0.75 ramps down before processor +V1.5S_CPU_VDDQ is turned off.



In current designs, Processor V_{DDQ} is powered with +V1.5, which is "ON" in S3. This is changed to a switching rail which is "OFF" during S3. A power FET is required to control the Processor V_{DDQ} (1.5 V) power. For N-FET (e.g., IRF7822 or RJK0346), gate voltage of FET (PS_S3CNTRL_1.5S) is derived from SLP_S3# and at 12-V logic. RDS(ON) of the FET used in CRB is in the range of 5 mΩ. Every design is different and designer should select an appropriate FET so that the required voltage rail specification is maintained at the Processor V_{DDQ} pins.

Signal Name	Source	Voltage Level	Comments
PS_S3CNTRL	Inverted SLP_S3# signal	In CRB, it is a 3.3-V signal.	Voltage should be high enough to turn ON or OFF the MOSFET. When selecting the MOSFET, insure $V_{gs}>V_{gsth}$.
PS_S3CNTRL_1.5S	Buffered SLP_S3# signal	In Intel CRB it is a 12-V signal.	Voltage should be high enough to turn ON or OFF the Power MOSFET. When selecting the MOSFET, insuree $V_{gs}>V_{gsth}$.



MICRO-STAR INT'L CO.,LTD.

Title: VTT,+1.8VRUN,PCIE_VDDC

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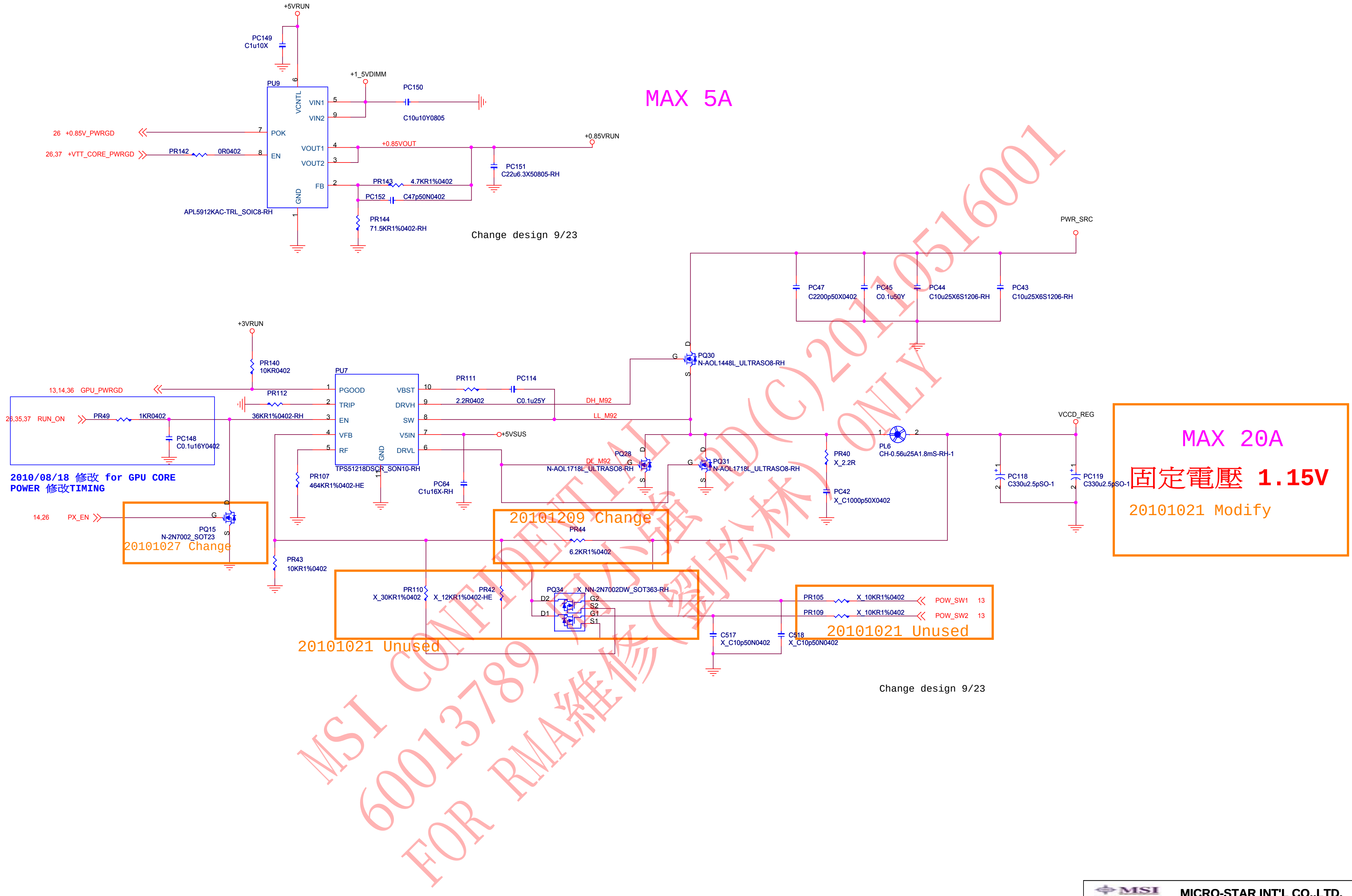

MICRO-STAR INT'L CO.,LTD.	
Title	+0.85VRUN/VGA CORE
Size: Custom	Document Number: MS-1482
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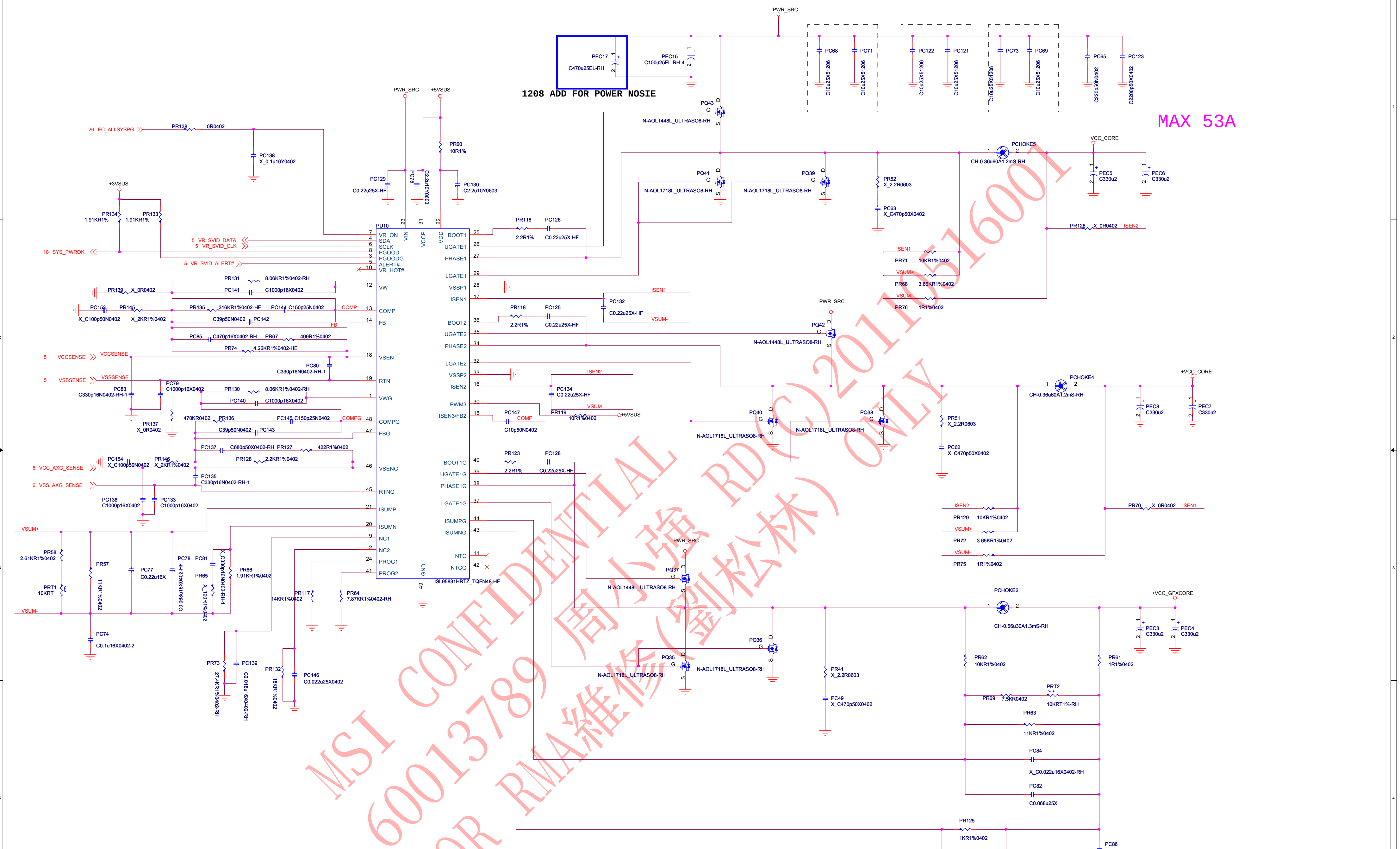

MICRO-STAR INT'L CO.,LTD.

Title	CPU CORE/GCORE	
Size: Custom	Document Number: MS-1482	Rev: 1.0
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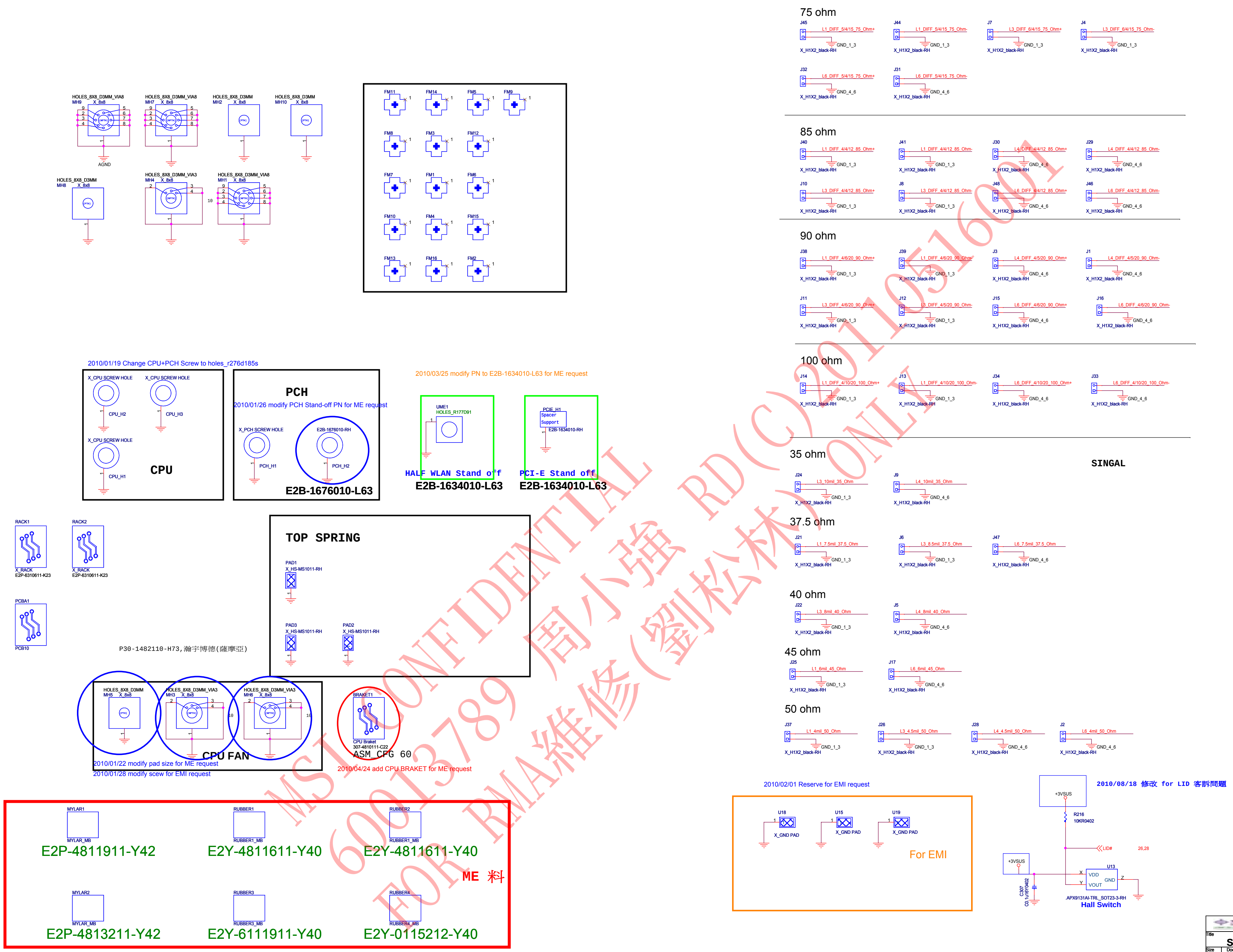

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME
Size	Custom
Document Number	MS-1482
Rev	1.0
Date:	Friday, December 17, 2010
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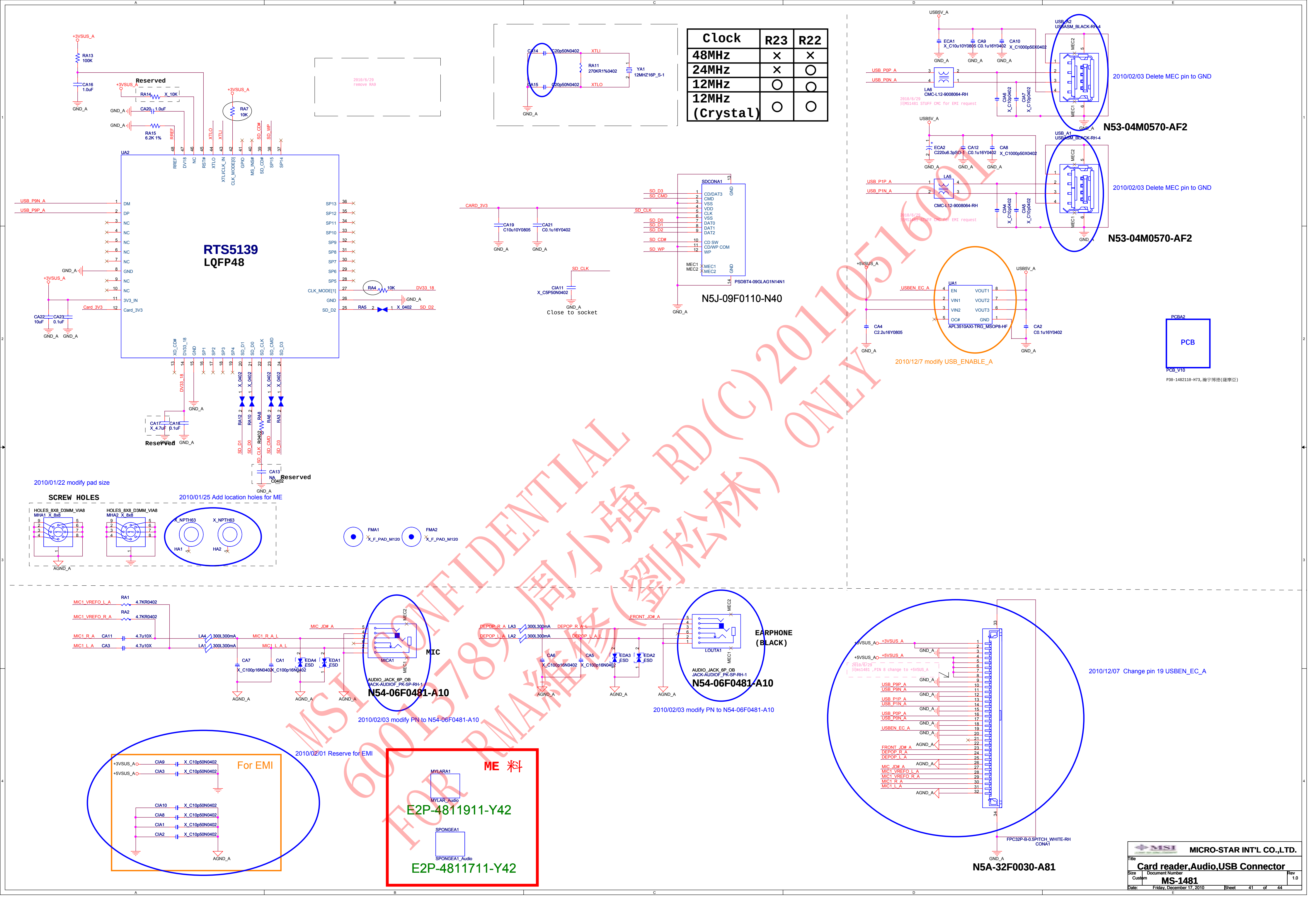

Clock	R23	R22
48MHz	×	×
24MHz	×	○
12MHz	○	○
12MHz (Crystal)	○	○

MICRO-STAR INT'L CO.,LTD.

Title: Card reader,Audio,USB Connector

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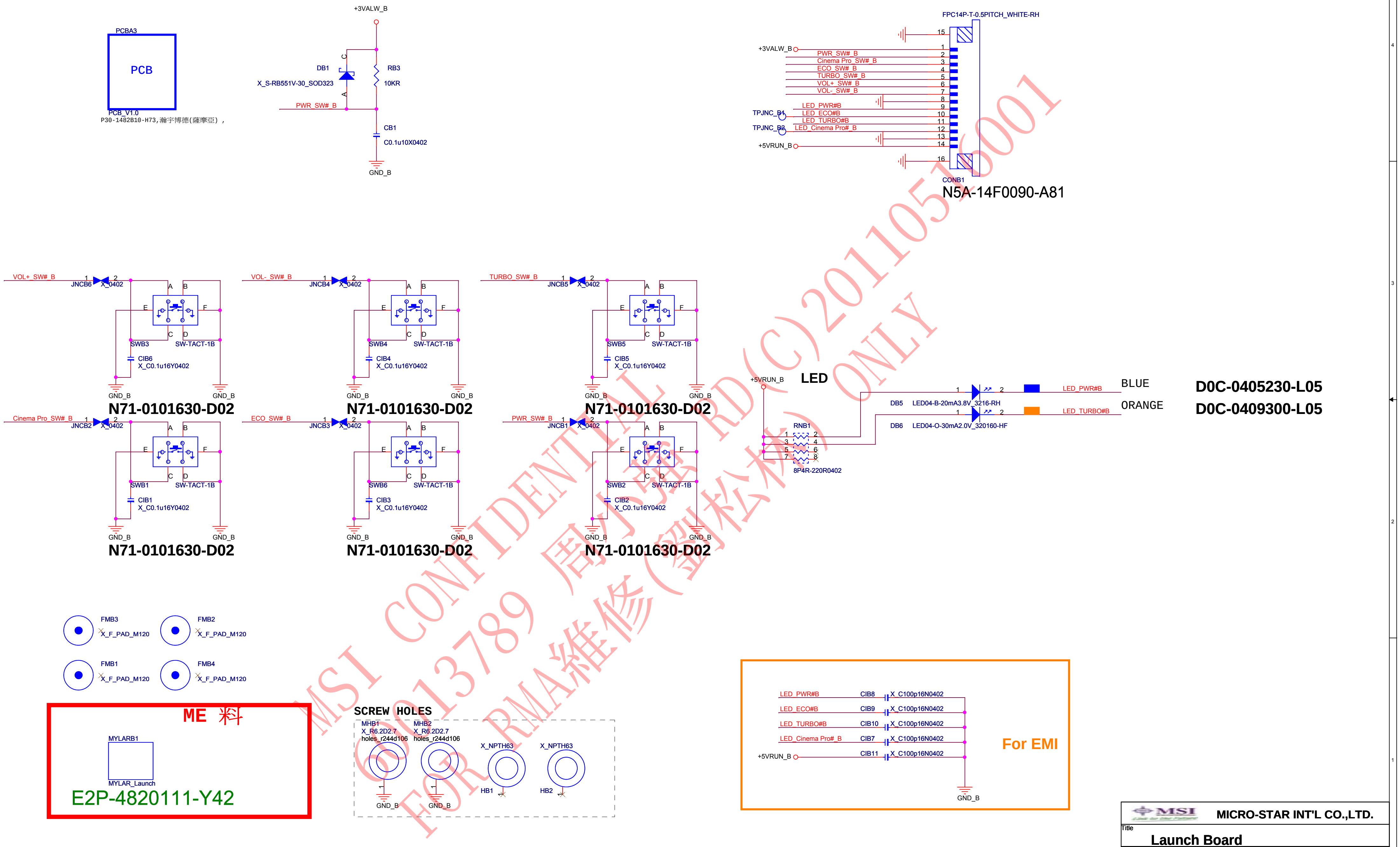

MICRO-STAR INT'L CO.,LTD.

Title: **Launch Board**

Size	Document Number	Rev
Custom	MS-1481	1.0

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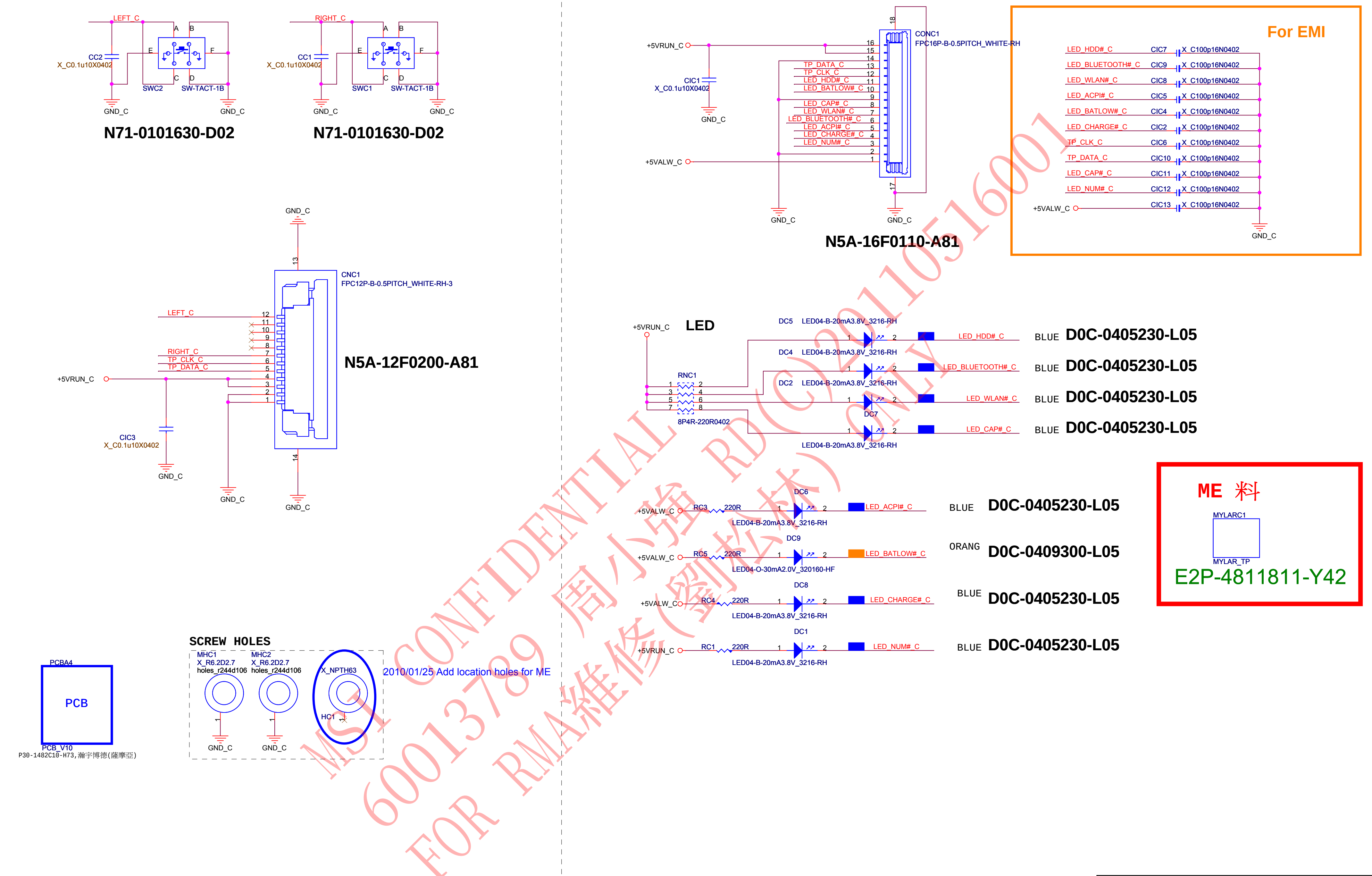

MICRO-STAR INT'L CO.,LTD.

Title: TP,LEDBOARD

Size: Custom | Document Number: MS-1481 | Rev: 1.0

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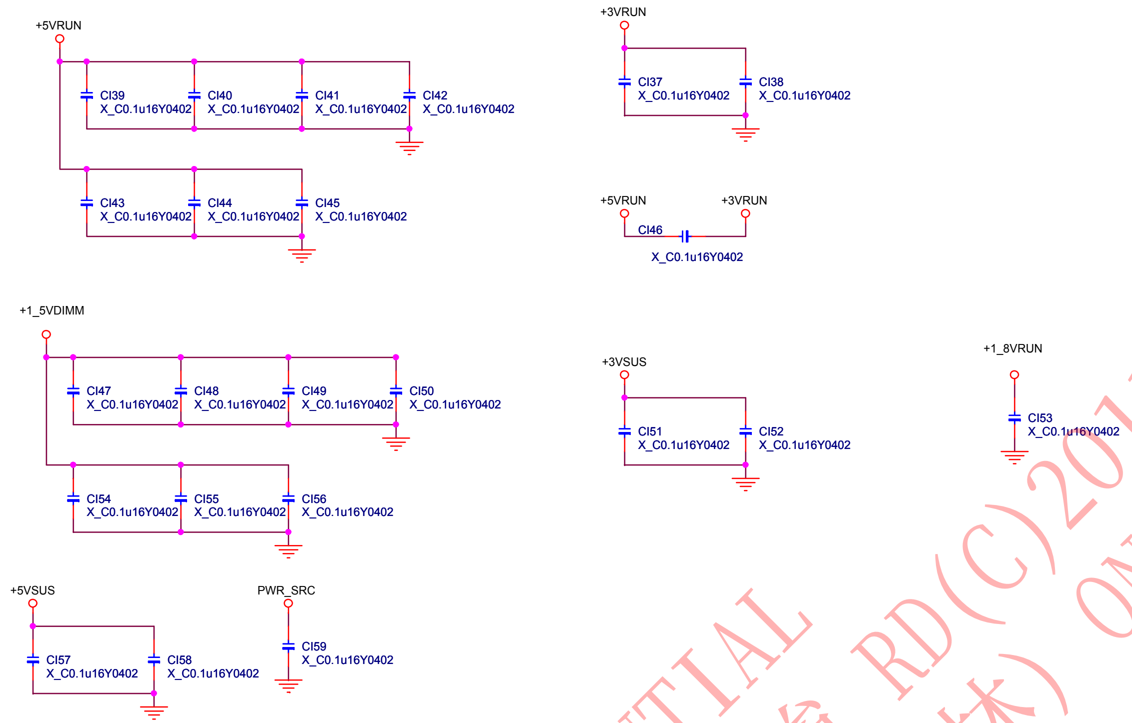

Title
<Title>

Size	Document Number	Rev
A3	<Doc>	1.0

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