COMPAL CONFIDENTIAL

MODEL NAME : FDX50

PCB NO : LA-J171P

BOM P/N : 431AK131L01~431AK131L31

GPIO MAP: EC- X11_CML_U_CSLP GPIO map Rev0.6_20190725
PCH- X11_CMLH_GPIO map Rev0.3_20190729

Rialto 15

Comet Lake H

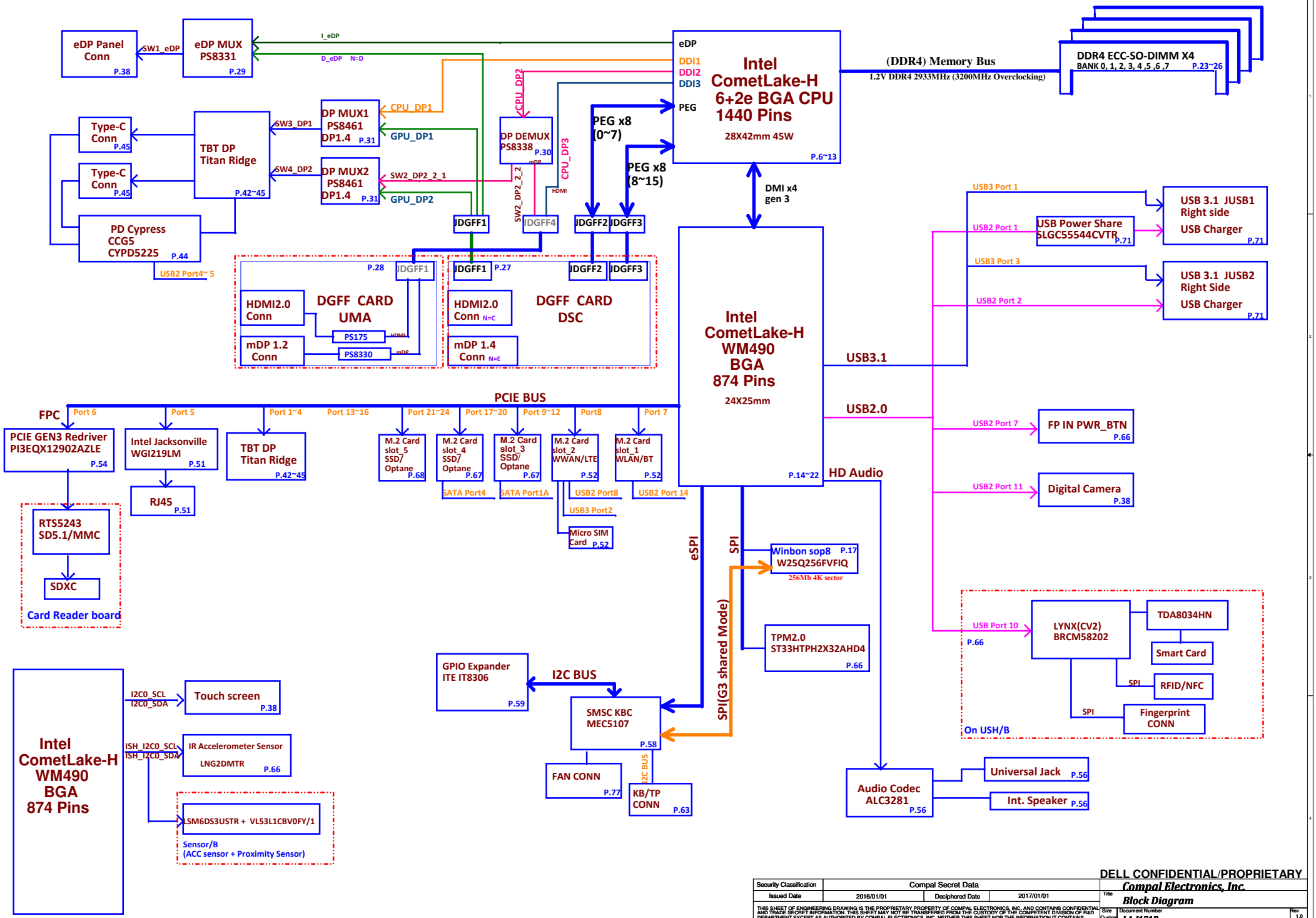
REV : 1.0(A00)

2020.8.26

EMI@, ESD@ , RF@ : EMI/ESD/RF Component
@EMI@,@ESD@,@RF@ : EMI/ESD/RF Nonpop Component
CONN@ : Connector
XDP@ : XDP Component (pop them until ST)
DS3@ : Deep sleep support
NDS3@ : Non-Deep sleep Support
@NDS3@: Non-Deep sleep Nonpop Component
RTD3@ : TBT RTD3 Support
NRTD3@ : Non TBT RTD3 support
eSPI@ : eSPI interface
JUMP@: PJP Component
@JUMP@: PJP Nopop Component
@ : Nopop Component

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: Cover		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 1 of 104	



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Compal Electronics, Inc.

Title: Block Diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	ON	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF

PM TABLE

State \ power plane	+PWR_SRC +5V_ALW +3.3V_ALW +3.3V_ALW2 +3.3V_ALW_DSW +3.3V_ALW_PCH +3.3V_RTC_LDO +1.8V_ALW +1.0V_PRIM +1.8V_PRIM	+3.3V_SUS +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +1.2V_RUN +3.3V_DGFF +5V_DGFF +DGFF_PWR_SRC +0.675V_DDR_VTT	(M-OFF) +VCC_CORE +VCC_GT +VCC_IO +VCC_SA +1.0V_VCCSTG +1.8V_RUN
S0	ON	ON	ON	ON
S3	ON	ON	OFF	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC don't exist	ON	OFF	OFF	OFF

USB3.0	DESTINATION
Port 1	JUSB1
Port 2	M.2 Slot-2 (WWAN/LTE)
Port 3	JUSB2
Port 4	NA
Port 5	NA
Port 6	NA

SATA	DESTINATION
SATA 0B	NA
SATA 1A	Slot-3 SSD
SATA 2	NA
SATA 3	NA
SATA 4	Slot-4 SSD
SATA 5	NA

	USB2 PORT#	DESTINATION
PCH	1	JUSB1
	2	JUSB2
	3	NA
	4	Cypress PD
	5	Cypress PD
	6	NA
	7	FP IN PWR_BTN
	8	M.2 Slot-2 (WWAN/LTE)
	9	NA
	10	USH
	11	Camera
	12	NA
	13	NA
	14	M.2 Slot-1 (BT)

USH	0	BIO
	1	NA

Thickness=1.6mm+/-10% FR4 Tg150 GA-150LL		DK	DF	delay time	Stack up	3/6 new requirement	Thickness
	Soldermask	3.7	0.03		Soldermask		0.5
L1	TOP			152.8	0.5oz + Plating	0.5oz + Plating	1.55
		3.7	0.0189		PP 1086	PP 1086	2.55
L2	Sig/Gnd/VCC				1oz	1oz	1.3
		3.7	0.0194		3mil core		3
L3	IN1			164.5	0.5oz	0.5oz	0.65
		3.8	0.0183		PP 2116HR		4.71
L4	Sig/Gnd/VCC				0.5oz	0.5oz	0.65
		3.7	0.0194		3mil core		3
L5	IN2			164.2	0.5oz	0.5oz	0.65
		3.8	0.0183		PP 2116		4.1
L6	Sig/GND/VCC				1oz	1oz	1.3
		3.7	0.0194		core		3
L7	Sig			165	1oz	1oz	1.3
		4	0.0169		PP7628 HRC		7.3
L8	Sig			165	1oz	1oz	1.3
		3.7	0.0194		core		3
L9	Sig/GND/VCC				1oz	1oz	1.3
		3.8	0.0183		PP 2116		4.1
L10	IN3			164.2	0.5oz	0.5oz	0.65
		3.7	0.0194		3mil core		3
L11	Sig/GND/VCC				0.5oz	0.5oz	0.65
		3.8	0.0183		PP 2116HR		4.71
L12	IN4			164.5	0.5oz	0.5oz	0.65
		3.7	0.0194		3mil core		3
L13	Sig/Gnd/VCC				1oz	1oz	1.3
		3.7	0.0189		PP 1086	PP 1086	2.55
L14	Bottom			152.8	0.5oz + Plating	0.5oz + Plating	1.55
	Soldermask	3.7	0.03		Soldermask		0.5
							63.82
							1.62

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0a	SATA 1a	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7				
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

PCI EXPRESS	DESTINATION
PORT 1~4	TBT-Titan Ridge
PORT 5	10/100/1G LOM
PORT 6	MMI(Card Reader)
PORT 7	M.2 Slot-1 (WLAN/CNVi)
PORT 8	M.2 Slot-2 (WWAN/LTE)
PORT9~12	Slot-3 SSD 2280/ Optane
PORT13~16	NA
PORT17~20	Slot-4 SSD 2280/ Optane
PORT21~24	Slot-5 PCIE ONLY 2280

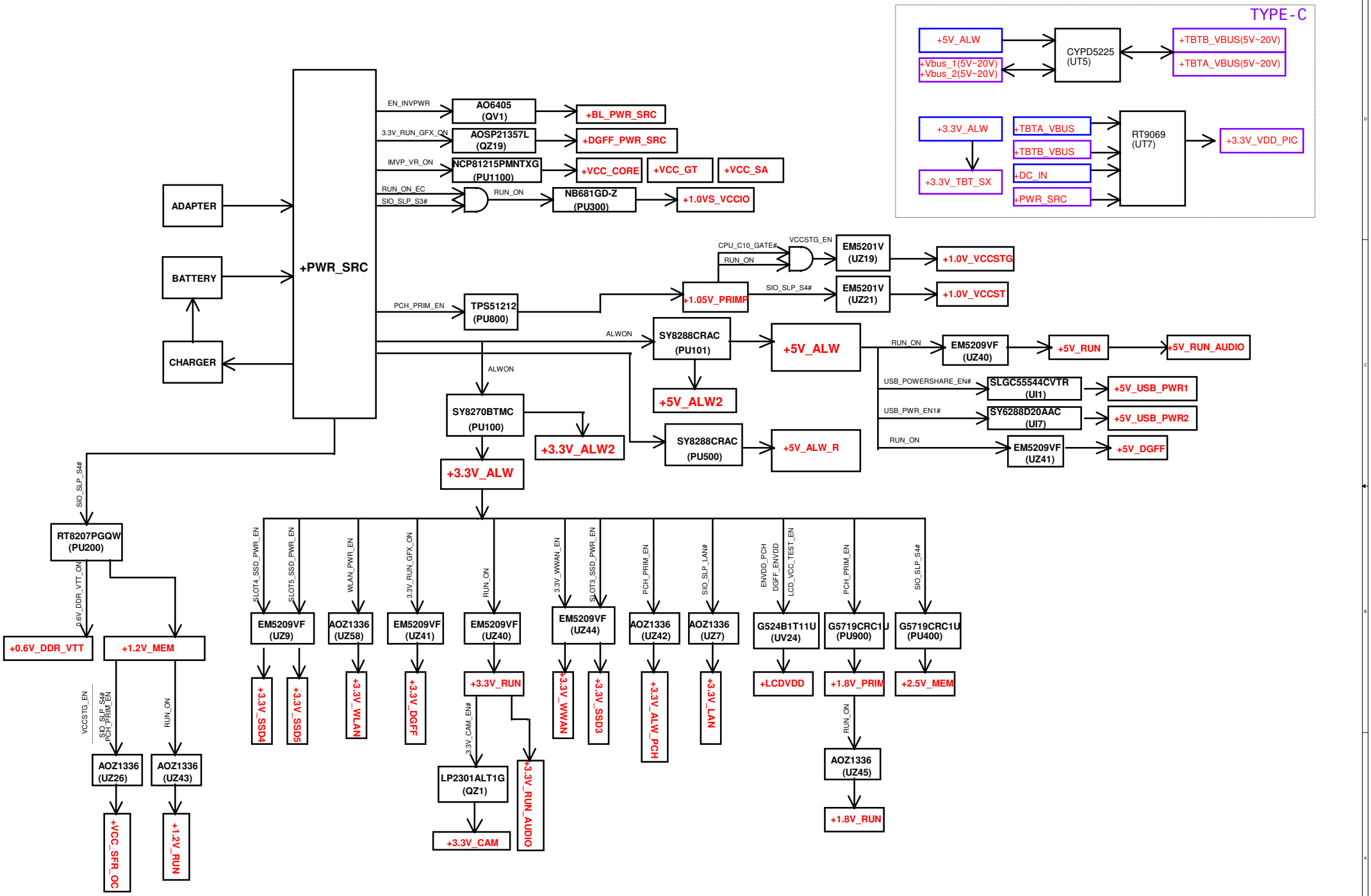
Security Classification	Compal Secret Data	
Issued Date	2016/01/01	Deciphered Date 2017/01/01

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 3 of 104



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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: Power MAP

Size	Document Number	Rev
Custom	LA-J171P	1.0

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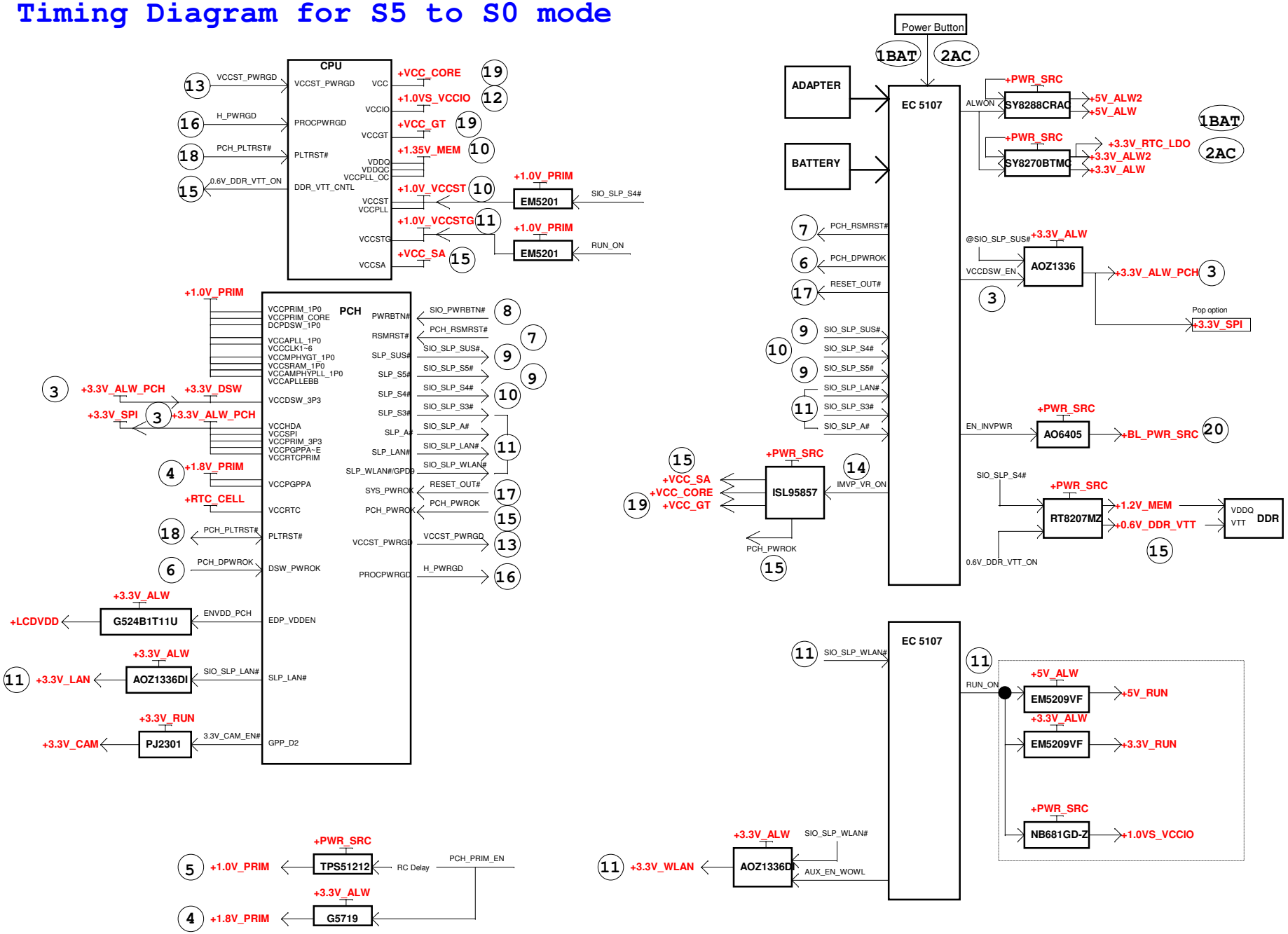
Timing Diagram for S5 to S0 mode



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Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML-H(1/8)DMI,PEG

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CFG11	
DMI_AC_coupled	
HALF-SWING DC coupled	1
FULL-SWING AC coupling	0

CFG10	
SAFE mode boot	
enable	1
disable	0

CFG12	
PMSYNC2.0	1
LEGACY	0

CFG9	
SVID NOT Present	
Present	1
Not presnet	0

CFG13	
SYNC & AYNC MODE	
ASYNCHRONOUS	1
SYNCHRONOUS	0

CFG8	
CFG UNLOCK	
disable	1
enable	0

CFG1	
PCHLESS MODE (CRB) Reserved CFG lane (EDS)	
NORMAL	1
PCHLESS	0

CFG0	
Stall reset sequence after PCU PLL lock until de-asserted	
No Stall	1
Stall	0

CFG2	
PEG LANE REVERSAL	
NORMAL	1
LANE REVERSED	0

CFG4	
eDP enable	
Disabled	1
Enabled	0

CFG5	
PCI Express* Bifurcation [6:5]	
1x8, 2x4	00
Reserved	01
2x8	10
1x16	11

CFG7	
PEG Training	
(default) PEG Train immediately following RESET# de-assertion	1
PEG Wait for BIOS for training	0

UC1E

BCLKP, BCLKN, PCI_BCLKP, PCI_BCLKN, CLK24P, CLK24N, VIDALERT#, VIDSCK, VIDSOUT, PROCHOT#, DDR_VTT_CNTL, VCCST_PWRGD, PROCPWRGD, RESET#, PM_SYNC, PM_DOWN, PECI, THERMTRIP#, SKTOCC#, PROC_SELECT#, CATERR#, ZVM#, MSM#, RSVD1, RSVD2, CFG_RCOMP

CFG_0 … CFG_19, PROC_TDO, PROC_TDI, PROC_TMS, PROC_TCK, PROC_TRST#, PROC_PREQ#, PROC_PRDY#, BPM#_0 … BPM#_3

5 OF 13

CML-H_BGA1440

pop RC171 for CNL
depop RC171 for SKL & KBL (CFL CRB rev0.7)

RF Request

VR_SVID_CLK — CC325 @RF@ — 33P_0201_50V8J

Place close CPU side

ESD Request place near CPU side

H_PWRGD — CC2300 100P_0201_50V8J ESD@

VCCST_PWRGD — CC2301 100P_0201_50V8J ESD@

H_THERMTRIP# — CC323 0.1U_0201_25V6K @ESD@

PROCHOT# — CC324 0.1U_0201_25V6K @ESD@

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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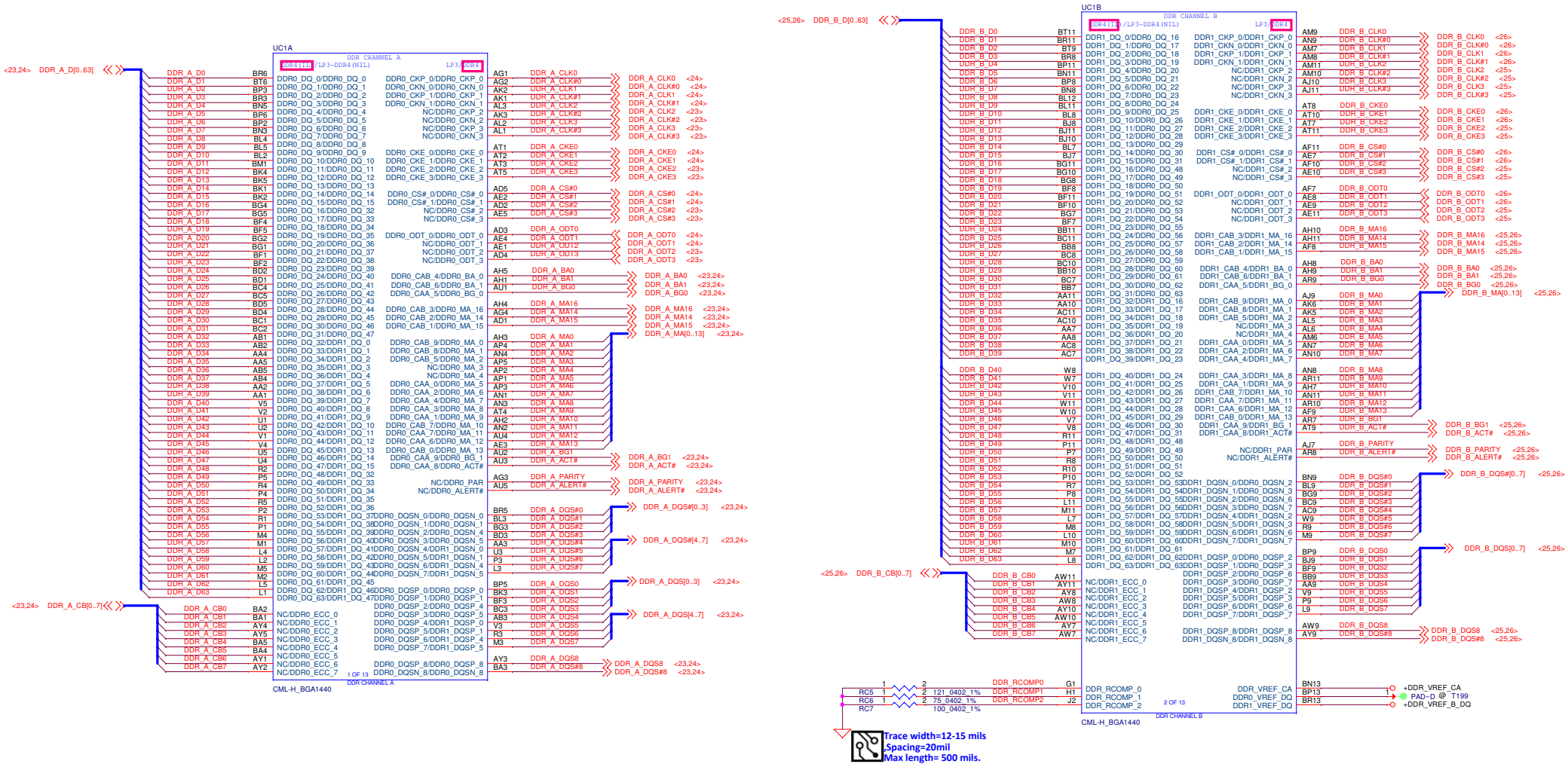
Compal Electronics, Inc.

Title: CML-H(2/8)XDP

Size: B | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 7 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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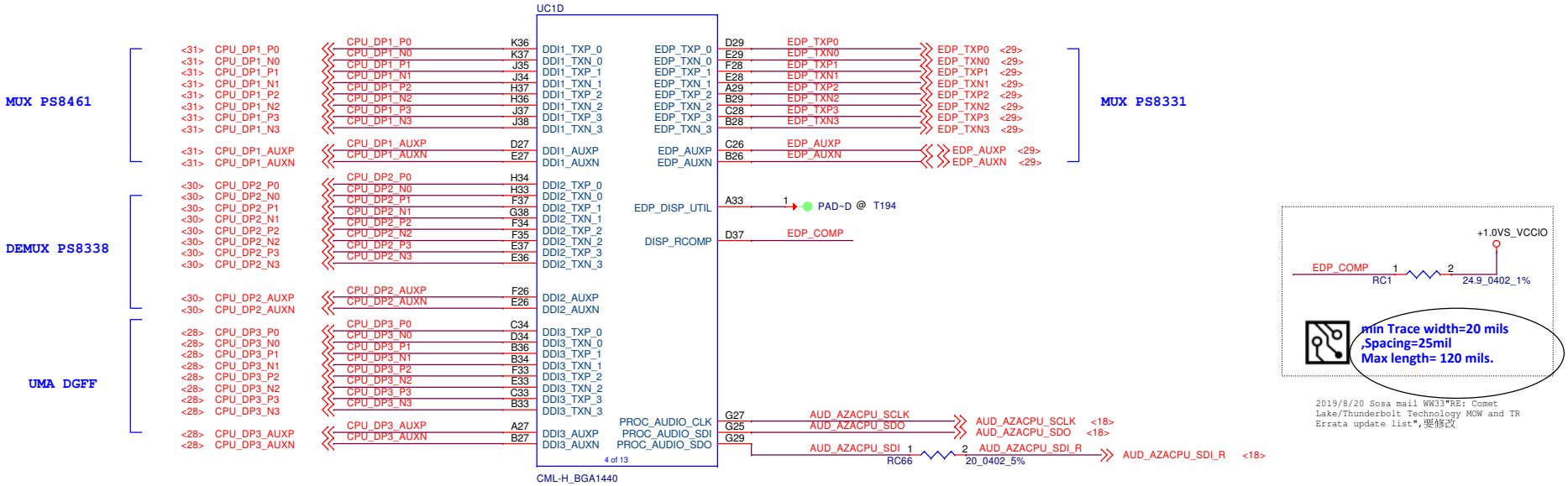
Compal Electronics, Inc.

Title: **CML-H(3/8)DDR4**

Size	Document Number	Rev
B	LA-J171P	1.0

Date: Wednesday, August 26, 2020 | Sheet 8 of 104



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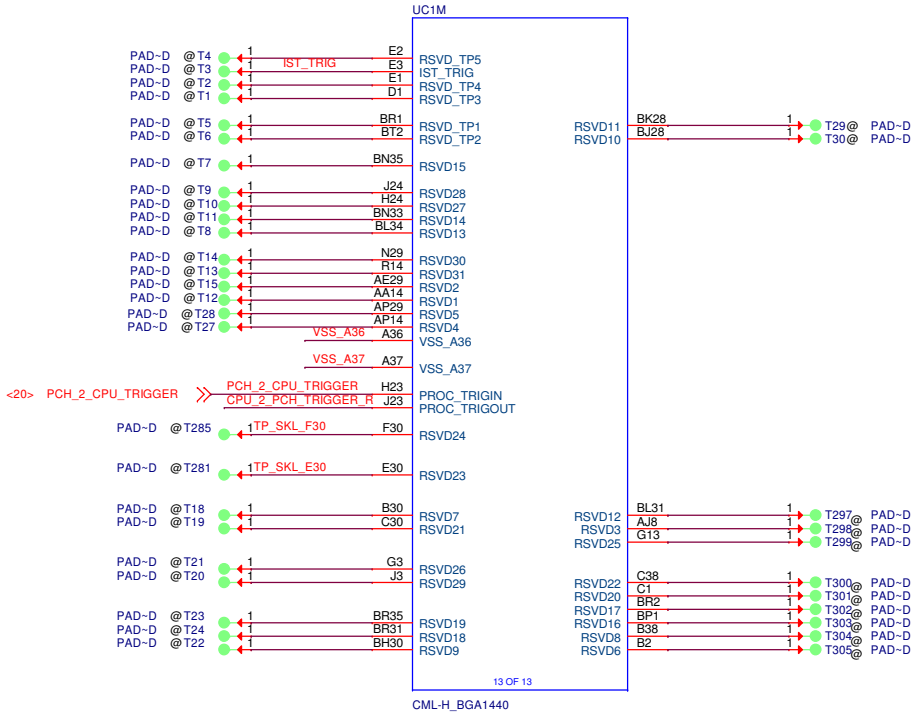
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

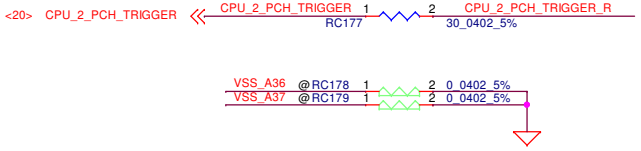
Compal Electronics, Inc.

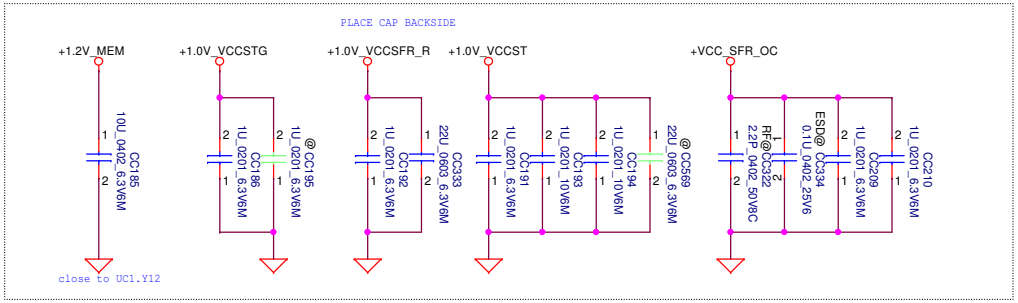
Title: CML-H(4/8)DDI,eDP

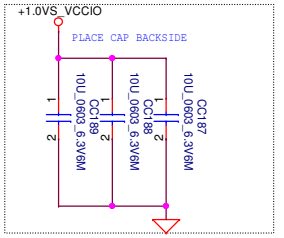
Size: A | Document Number: LA-J171P | Rev: 1.0

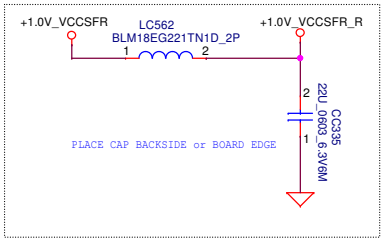
Date: Wednesday, August 26, 2020 | Sheet 9 of 104

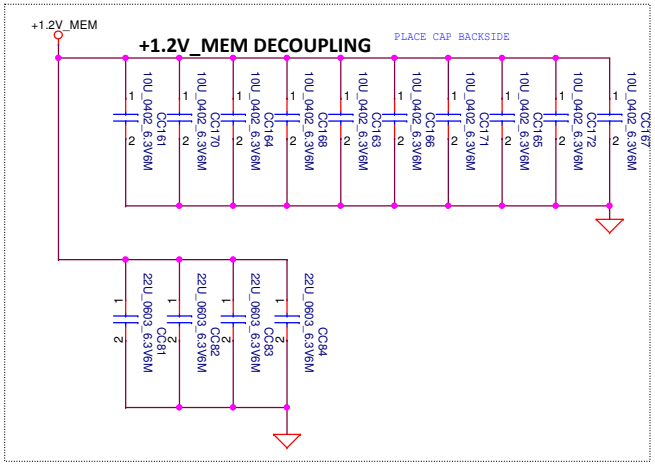












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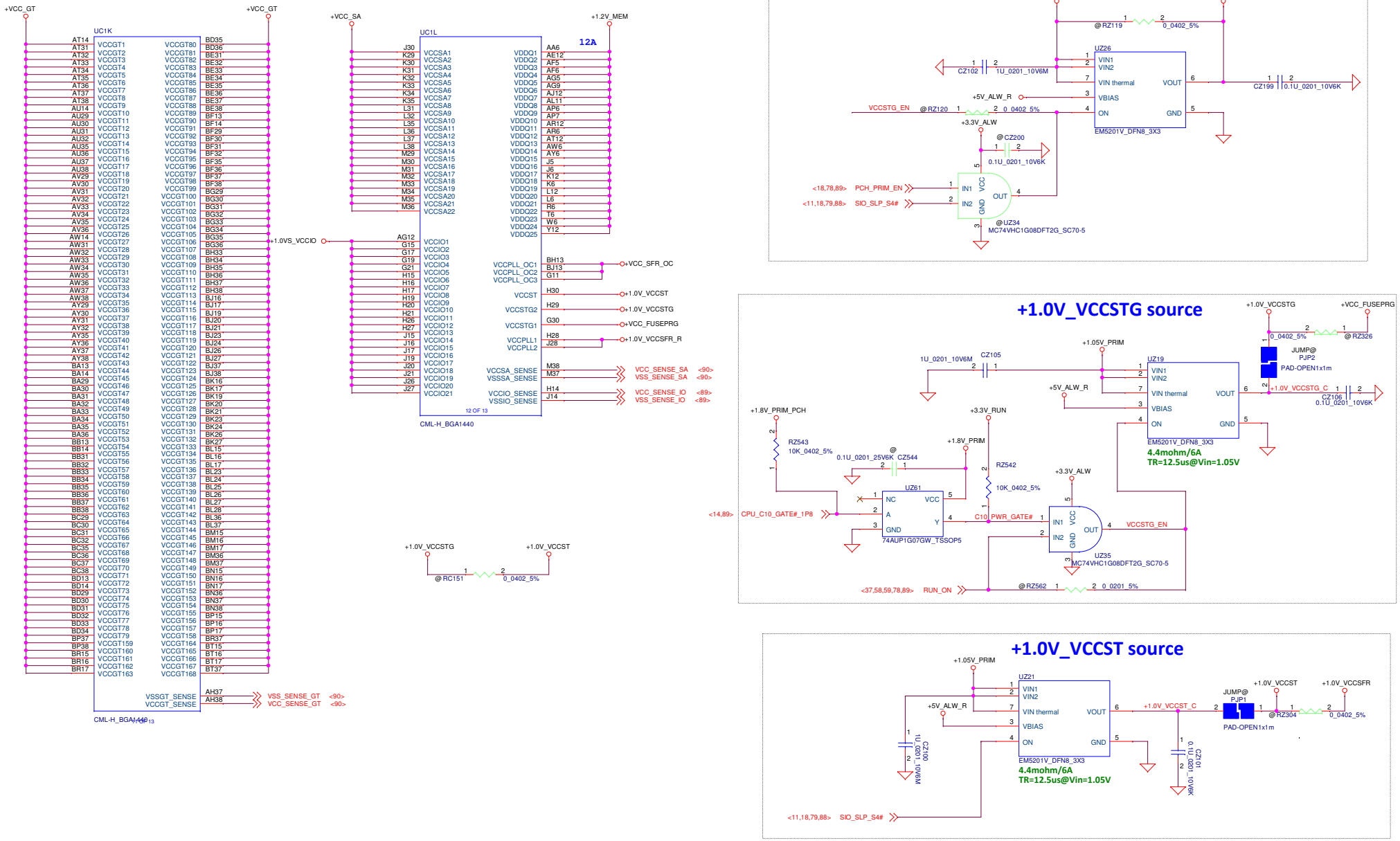
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML-H(5/8)RSVD,Decoupling

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 10 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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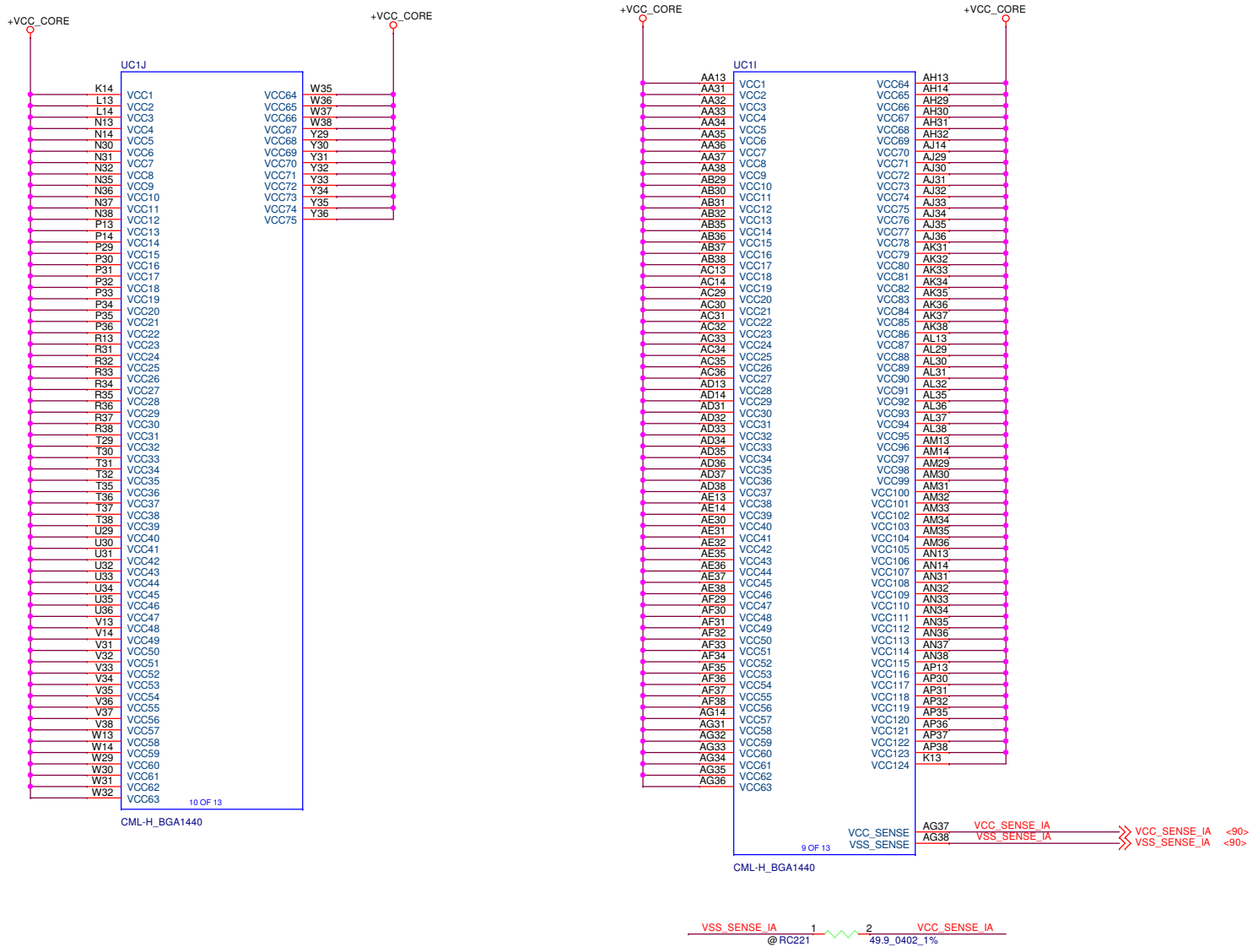
Compal Electronics, Inc.

Title: *CML-H(6/8)PWR*

Size	Document Number	Rev
B	*LA-J171P*	1.0

Date: Wednesday, August 26, 2020 | Sheet 11 of 104



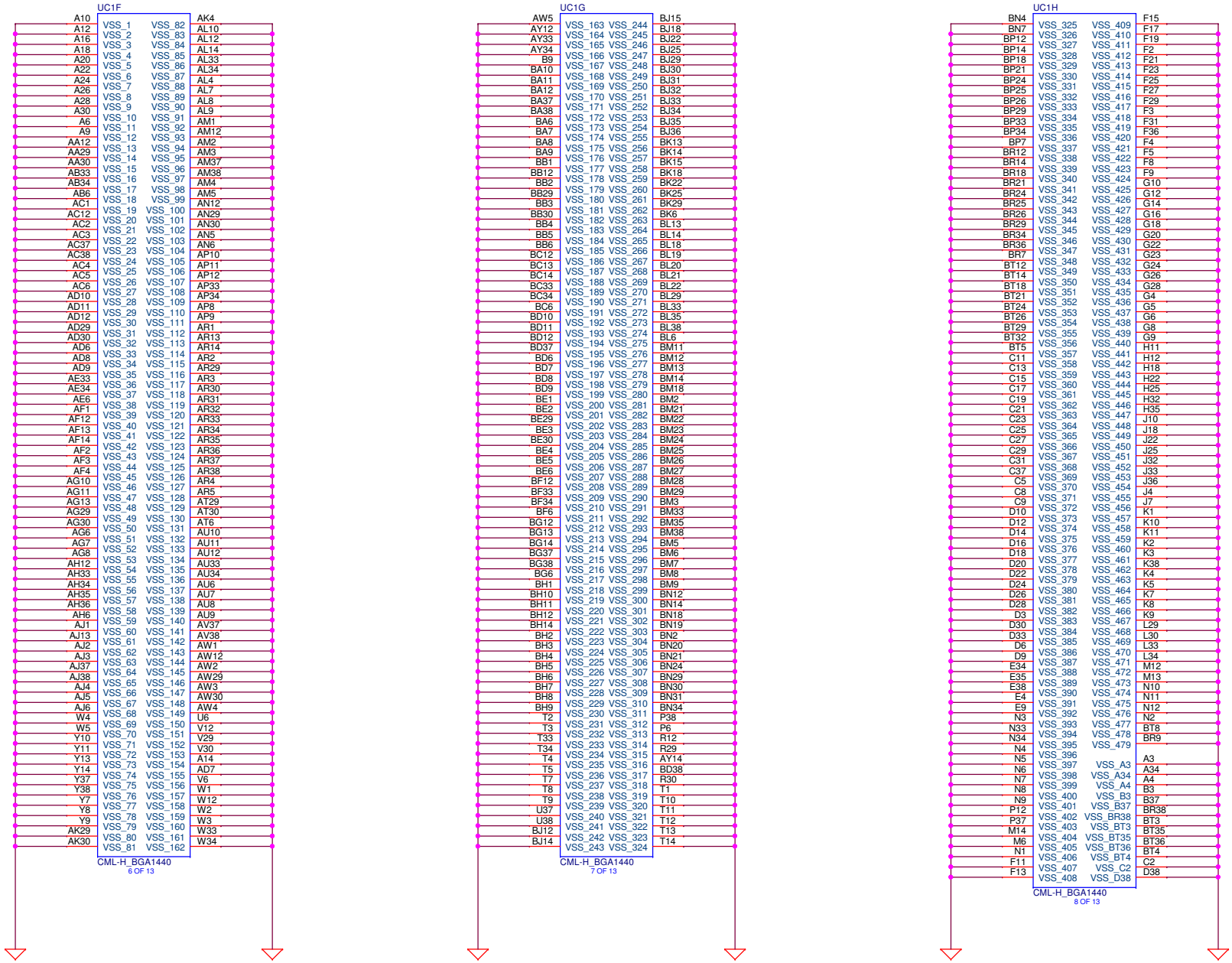
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML-H(7/8)PWR

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 12 of 104



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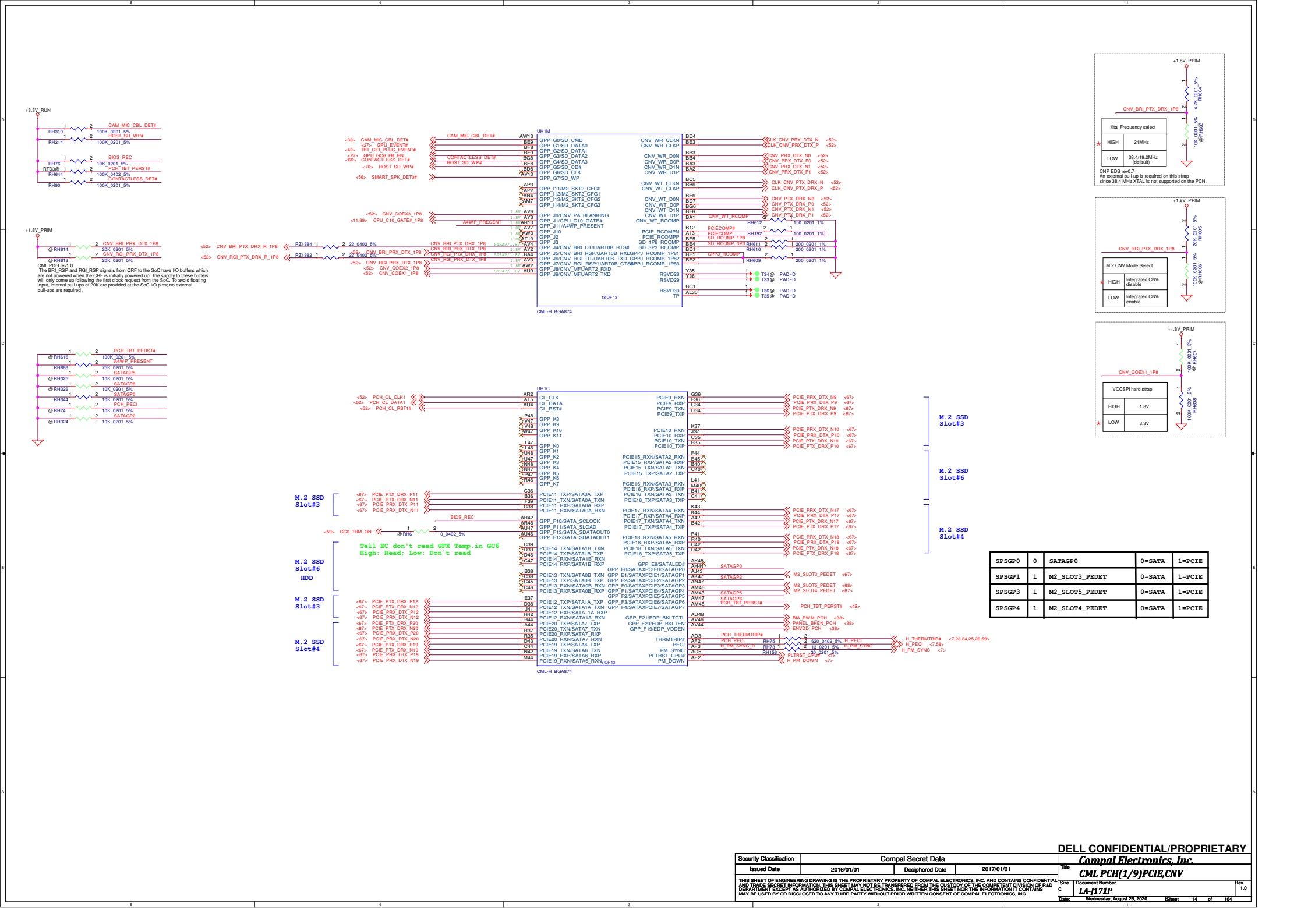
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML-H(8/8)GND

Size: A | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 13 of 104



SPSGP0	0	SATAGP0	0=SATA	1=PCIE
SPSGP1	1	M2_SLOT3_PEDET	0=SATA	1=PCIE
SPSGP3	1	M2_SLOT5_PEDET	0=SATA	1=PCIE
SPSGP4	1	M2_SLOT4_PEDET	0=SATA	1=PCIE

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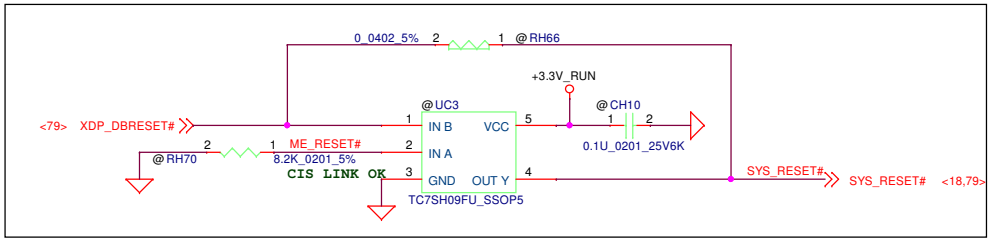
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

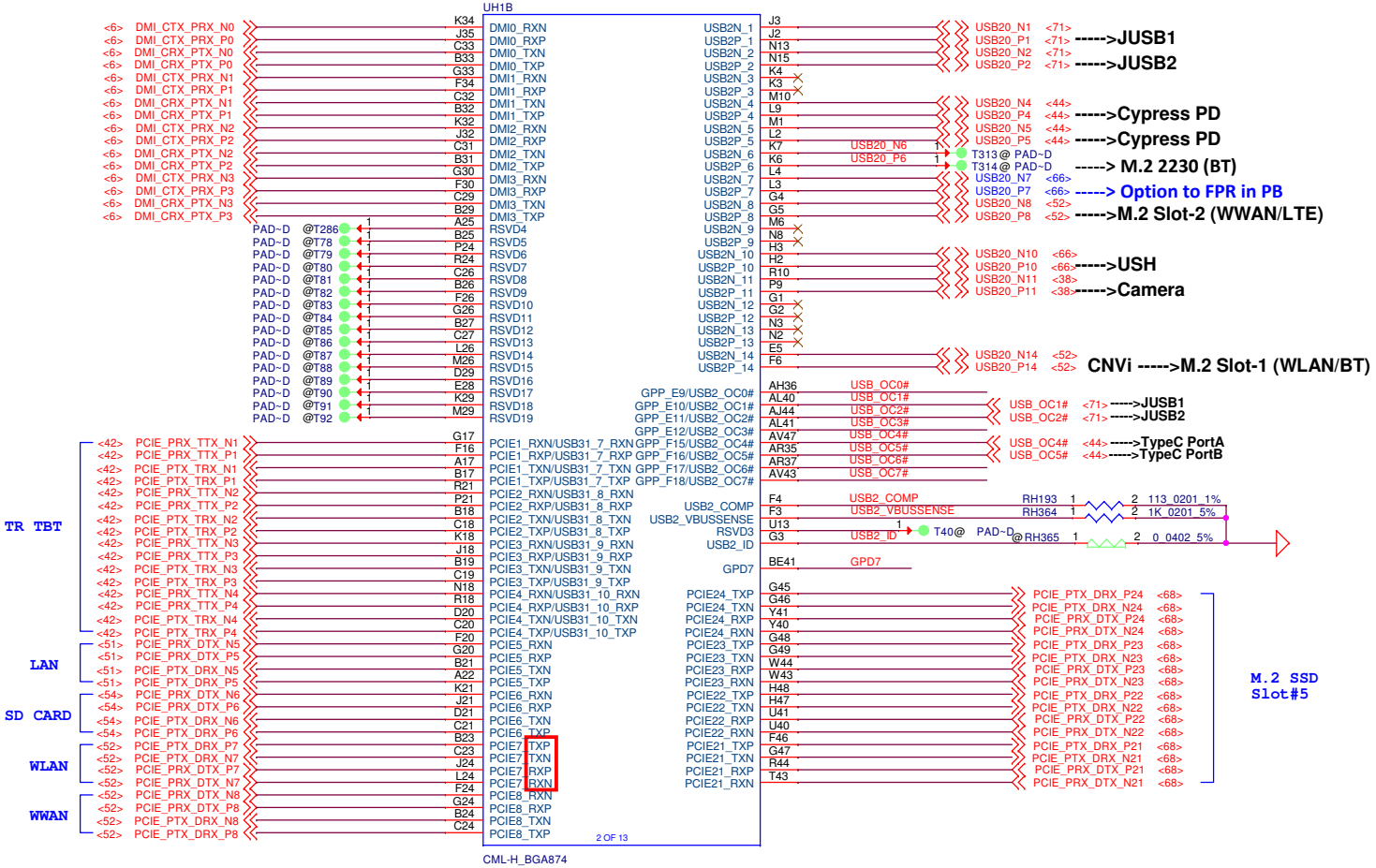
Compal Electronics, Inc.

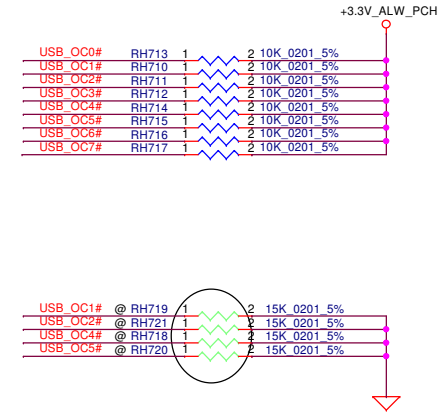
Title: CML PCH(1/9)PCIE,CNV

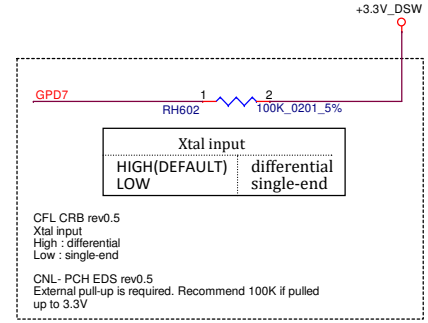
Size	Document Number	Rev
C	LA-J171P	1.0

Date: Wednesday, August 26, 2020 Sheet 14 of 104









Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML PCH(2/9)PCIE,DMI,USB

Size	Document Number	Rev
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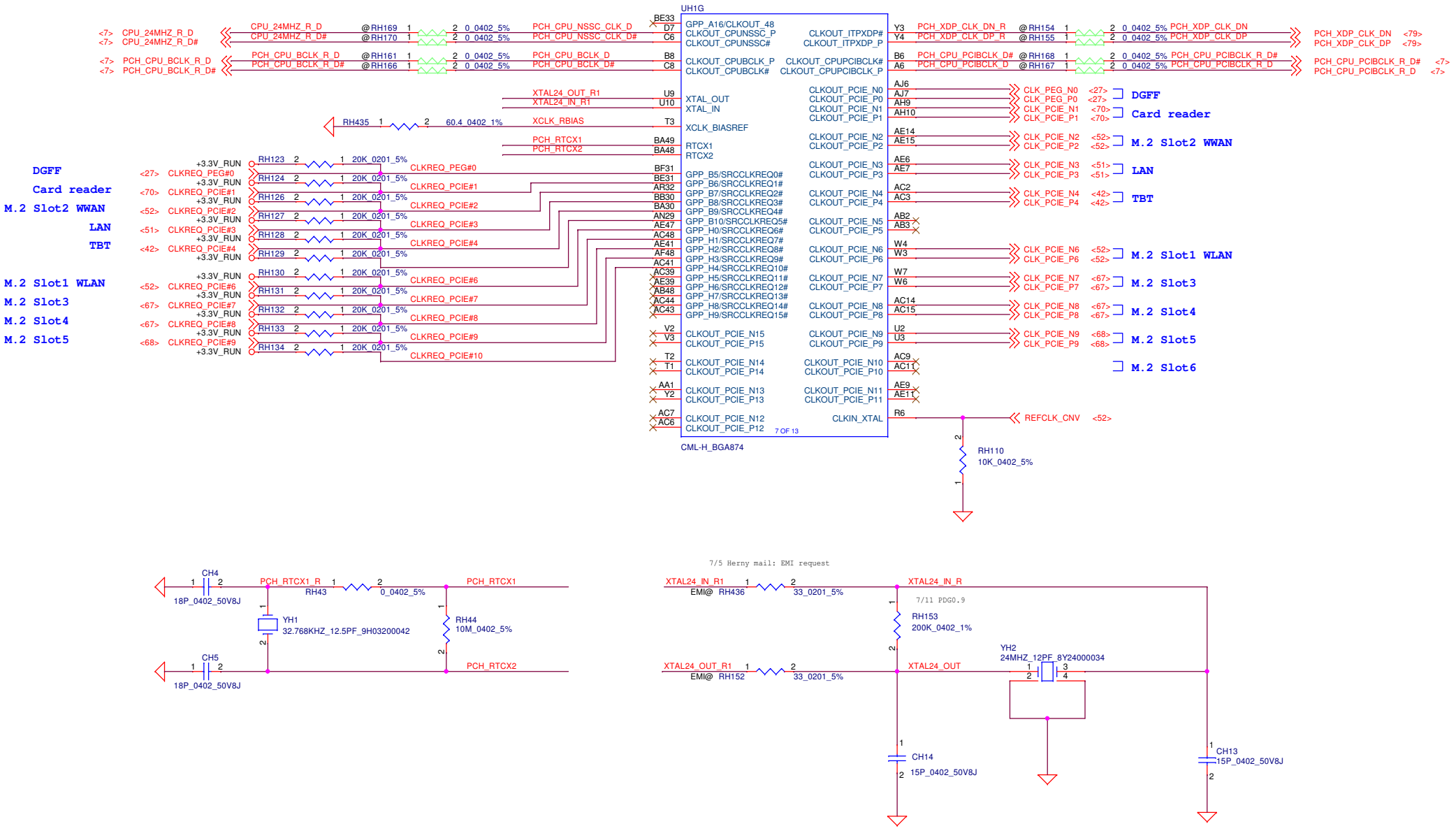


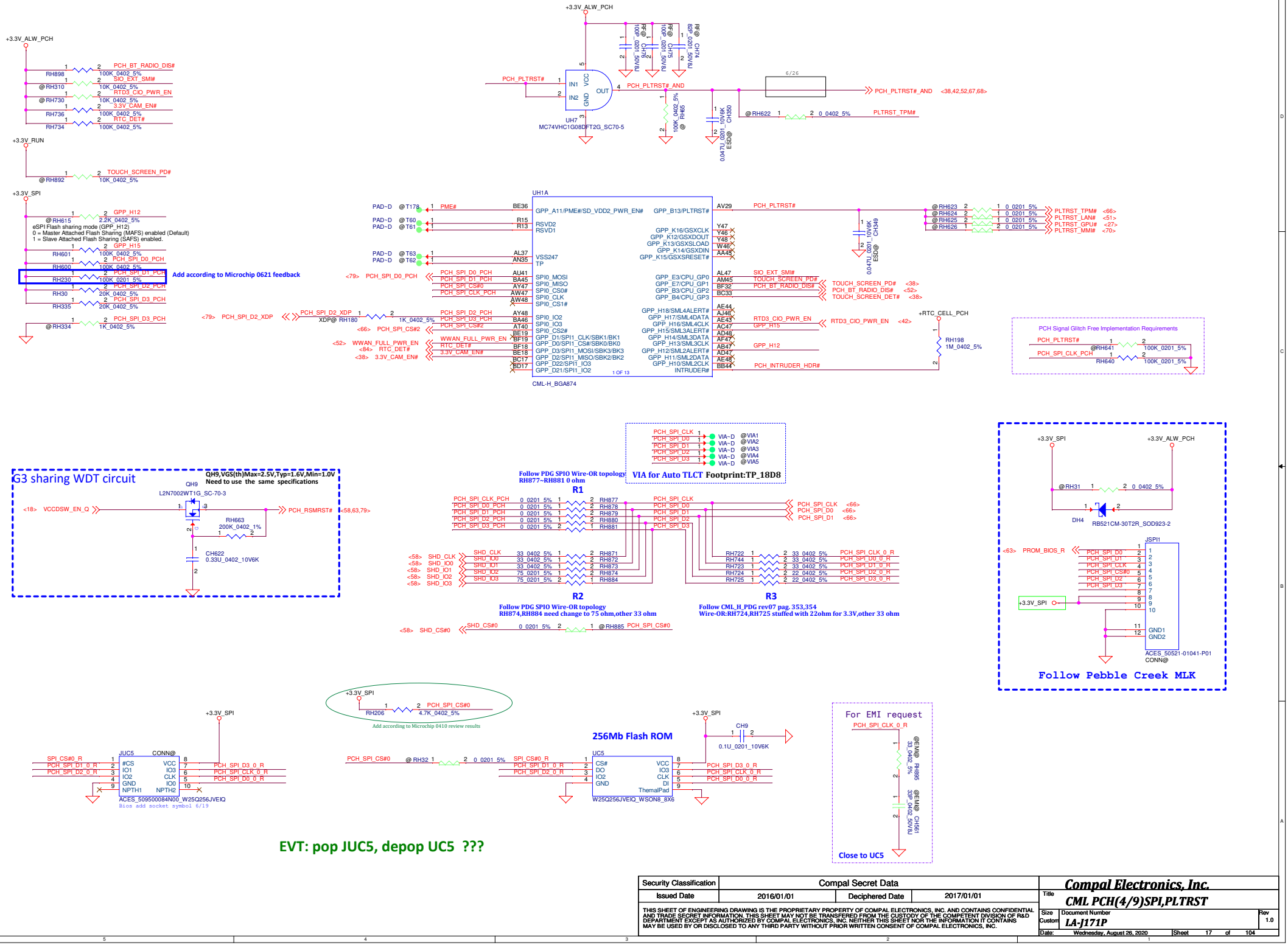
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML PCH(3/9)CLK

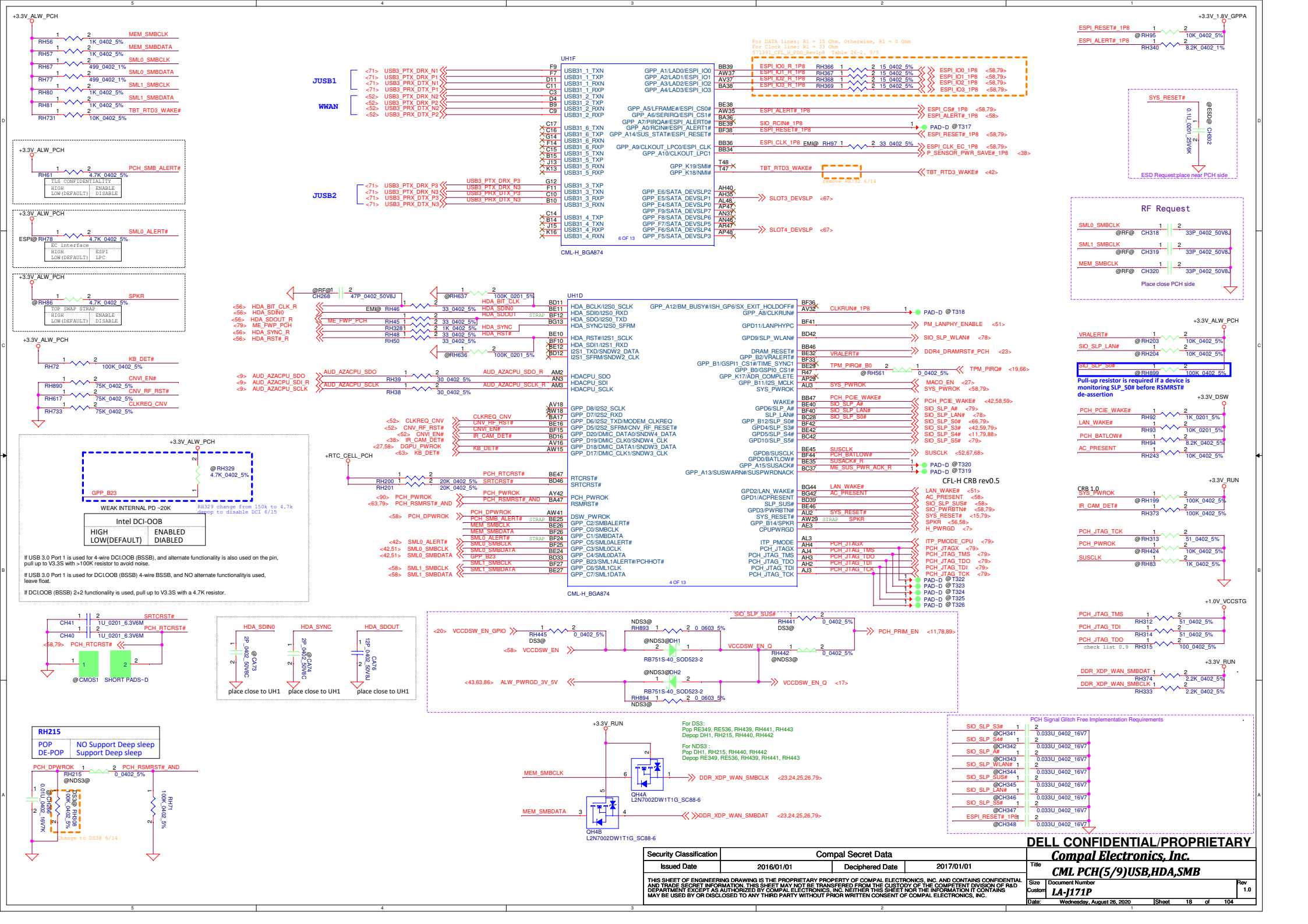
Size: Custom | Document Number: LA-J171P | Rev: 1.0

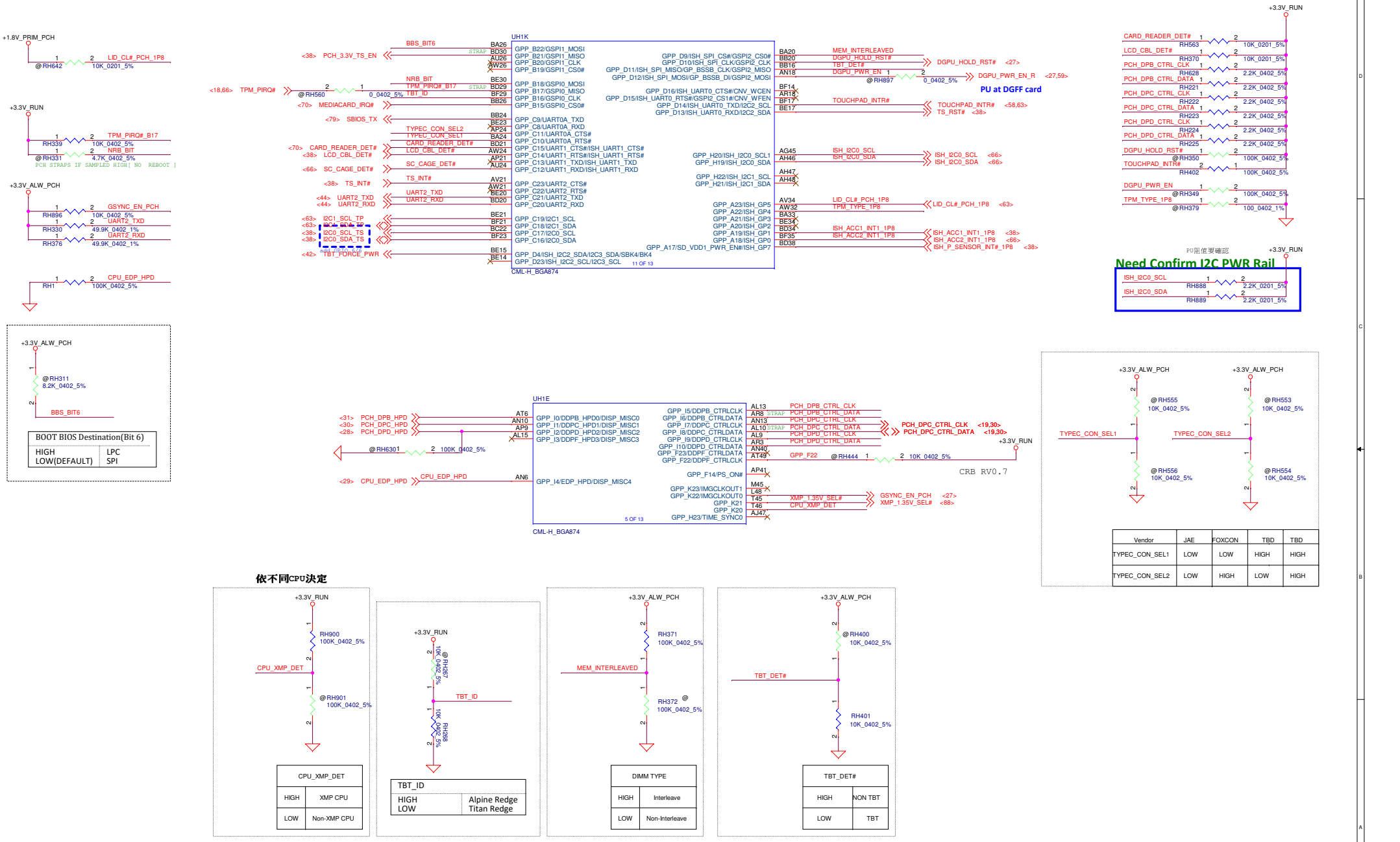
Date: Wednesday, August 26, 2020 | Sheet 16 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	CML PCH(4/9)SPI,PLTRST
Size: Custom	Document Number: LA-J171P
Rev	1.0
Date: Wednesday, August 26, 2020	Sheet 17 of 104


+3.3V_ALW_PCH
MEM_SMBCLK
MEM_SMBDATA
SML0_SMBCLK
SML0_SMBDATA
SML1_SMBCLK
SML1_SMBDATA
TBT_RTD3_WAKE#
PCH_SMB_ALERT#
SML0_ALERT#
SPKR
KB_DET#
CNVI_EN#
CNV_RF_RST#
CLKREQ_CNV
+3.3V_1.8V_GPPA
ESPI_RESET#_1P8
ESPI_ALERT#_1P8
SYS_RESET#
ESD Request:place near PCH side
RF Request
Place close PCH side
JUSB1
WWAN
JUSB2
UH1F
CML-H_BGA874
6 OF 13
UH1D
4 OF 13
CFL-H CRB rev0.5
+3.3V_DSW
+3.3V_RUN
+1.0V_VCCSTG
+RTC_CELL_PCH
GPP_B23
WEAK INTERNAL PD ~20K
Intel DCI-OOB
HIGH ENABLED
LOW(DEFAULT) DISABLED
If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionalityis used, leave float.
If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.
@CMOS1 SHORT PADS~D
place close to UH1
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
QH4A L2N7002DW1T1G_SC88-6
QH4B L2N7002DW1T1G_SC88-6
DDR_XDP_WAN_SMBCLK
DDR_XDP_WAN_SMBDAT
PCH_PRIM_EN
VCCDSW_EN_GPIO
VCCDSW_EN
VCCDSW_EN_Q
ALW_PWRGD_3V_5V
RB751S-40_SOD523-2
PCH Signal Glitch Free Implementation Requirements
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
CML PCH(5/9)USB,HDA,SMB
Security Classification: Compal Secret Data
Issued Date: 2016/01/01
Deciphered Date: 2017/01/01
Size: Custom
Document Number: LA-J171P
Rev: 1.0
Date: Wednesday, August 26, 2020
Sheet 18 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

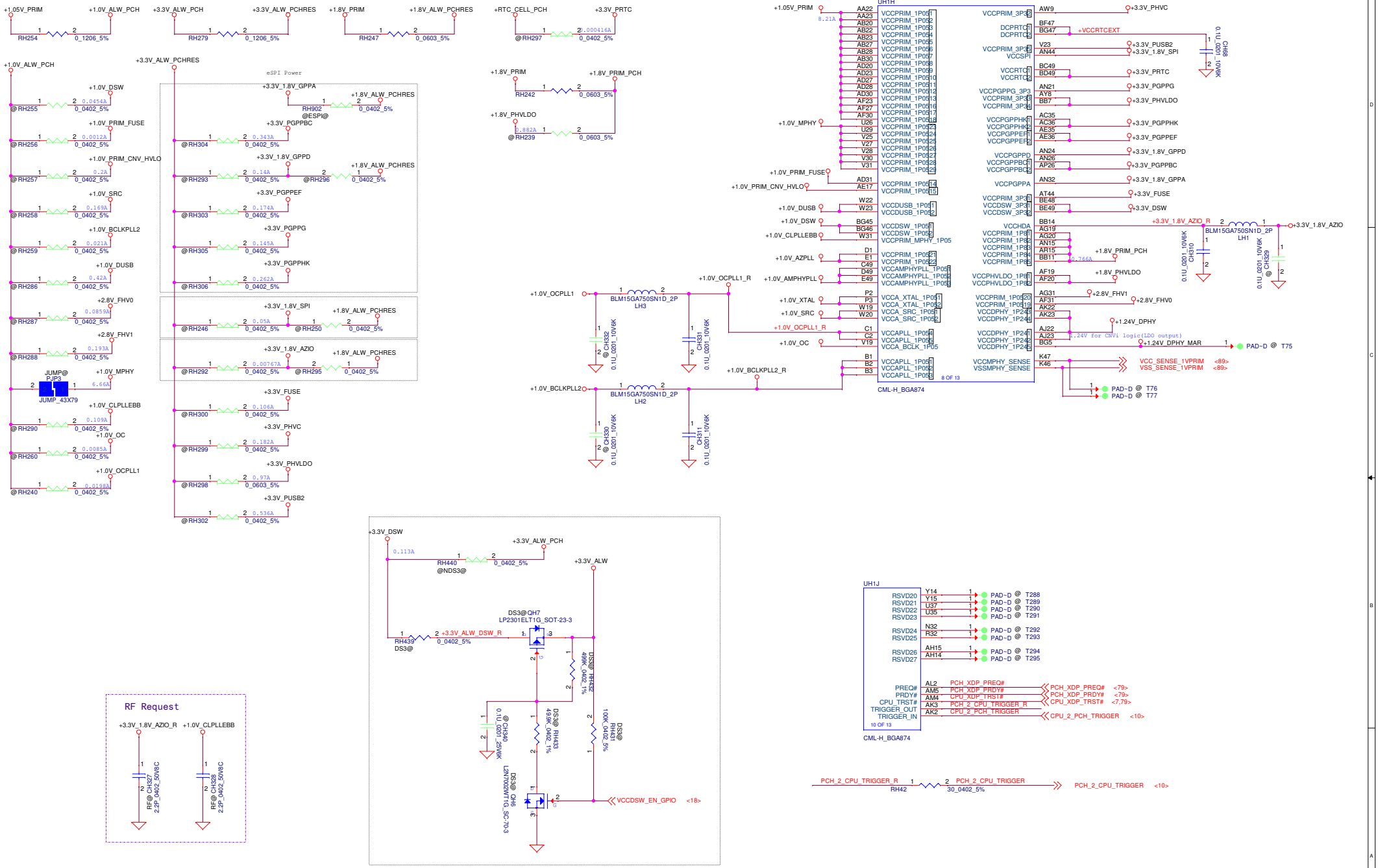
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: *CML PCH(6/9)GPIO,HPD,DDC*

Size	Document Number	Rev
Custom	*LA-J171P*	1.0

Date: Wednesday, August 26, 2020 | Sheet 19 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

DELL CONFIDENTIAL/PROPRIETARY

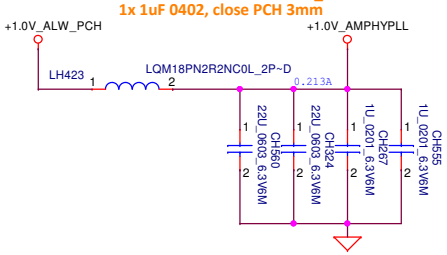
Compal Electronics, Inc.

Title: **CML PCH(7/9)PWR,RSVD**

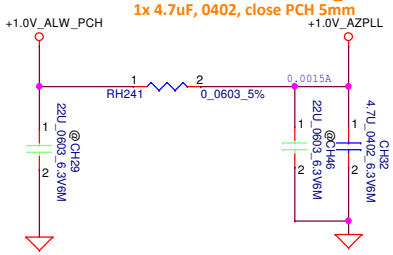
Size	Document Number	Rev
Custom	LA-J171P	1.0

Date: Wednesday, August 26, 2020 | Sheet 20 of 104

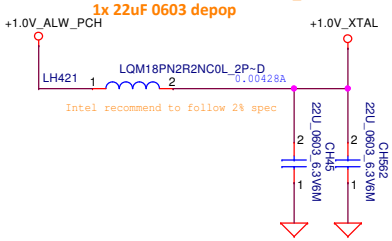
PDG V1P8 Table 50-8 +1.0V_AMPHYPLL
1x 1uF 0402, close PCH 3mm



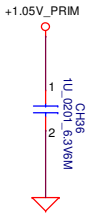
PDG V1P8 Table 50-8. +1.0V_AZPLL
1x 4.7uF, 0402, close PCH 5mm



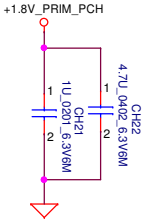
PDG V1P8 Table 50-9. +1.0V_XTAL
1x 22uF 0603 depop



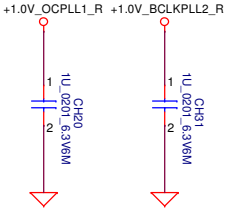
PDG V1P8 Table 50-8 +1.05V_PRIM
1x 1uF, 0402, close PCH 3mm



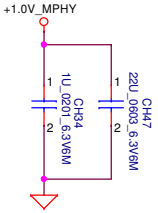
PDG V1P8 Table 50-8 +VCCPRIM_1P8
1x 4.7uF 0603, close PCH 3mm
1x 1uF 0402, close PCH 3mm



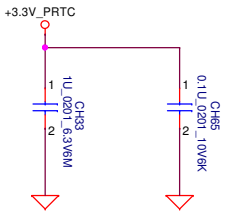
PDG V1P8 Table 50-8 VCCAPLL_1P05
1x 1uF, 0402, close PCH 5mm



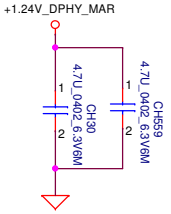
PDG V1P8 Table 50-8 +VCCPRIM_1P05
1x 1uF 0402, 3mm, close PCH 5mm
1x 22uF 0805, 5mm, close PCH 5mm



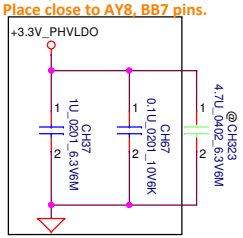
PDG V1P8 Table 50-8 +VCCRTC
1x 0.1uF 0402, close PCH 3mm
1x 1uF 0402, close PCH 5mm



PDG V1P8 Table 50-8 +VCCDPHY_1P24
1x 4.7uF 0402, close PCH 5mm

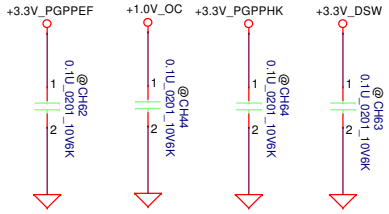


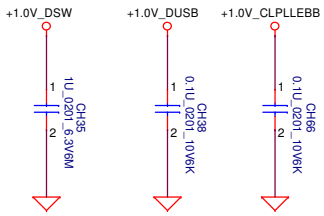
PDG V1P8 Table 50-8 +VCCPRIM_3P3
1x 1uF, 0603, close PCH 3mm
Place close to AY8, BB7 pins.



CFL-H PDG rev0.5 4.7uF x1
CRB-H rev0.7 0.1uF x1, 1uF x1

PDG V1P8 Table 50-8 depop, but reserved





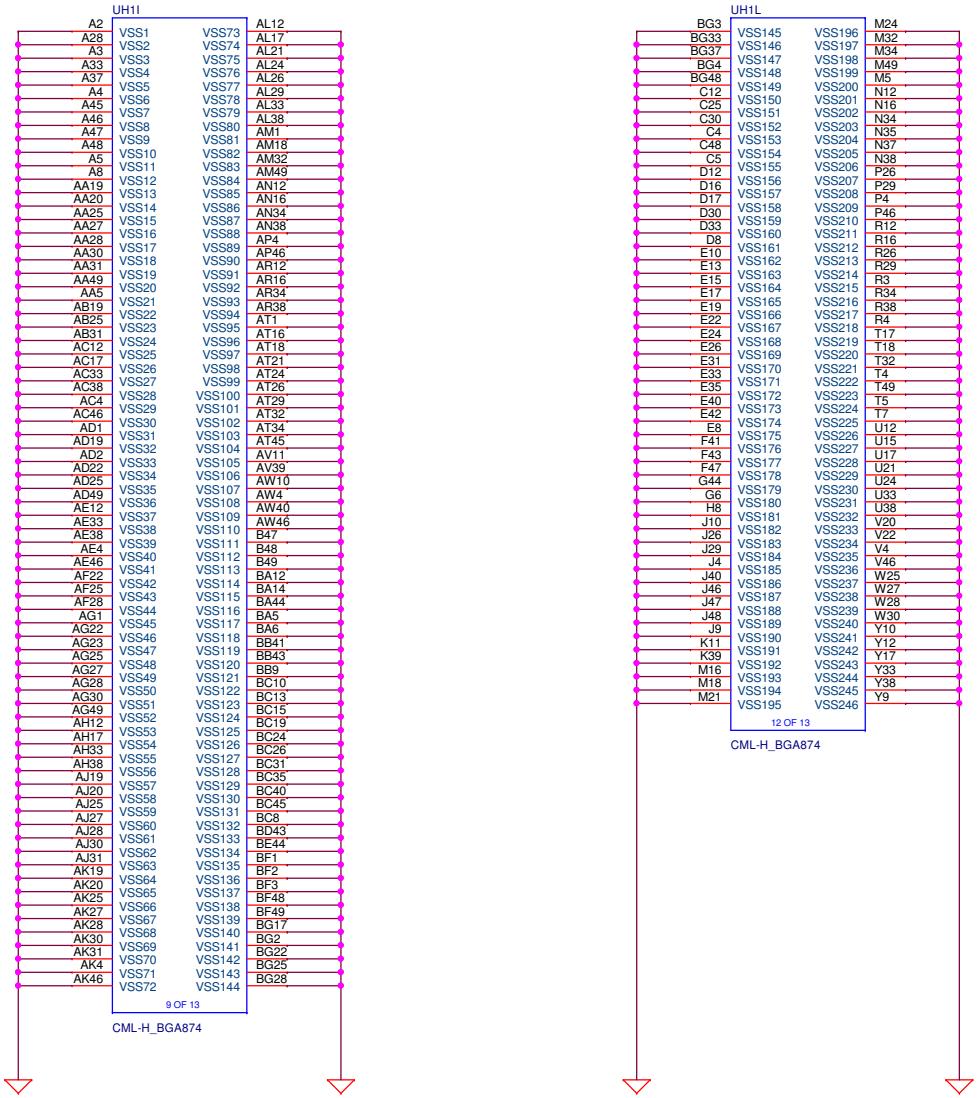
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML PCH(8/9)PWR CAP

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 21 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: CML PCH(9/9)GND

Size: Custom | Document Number: LA-J171P | Rev: 1.0

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All VREF traces should have 10 mil trace width

JDIMM1 REV Type H=4

CH-B REV JDIMM4 -->CKE0,1 | CH-A STD JDIMM2 -->CKE0,1

CPU D C B A

Bottom Side

Top Side

CH-B STD JDIMM3 -->CKE2,3 | CH-A REV JDIMM1 -->CKE2,3

<8,24> DDR_A_CB[0..7]
<8,24> DDR_A_DQS#[0..3]
<8,24> DDR_A_DQS[0..3]
<8,24> DDR_A_DQS#[4..7]
<8,24> DDR_A_DQS[4..7]
<8,24> DDR_A_D[0..63]
<8,24> DDR_A_MA[0..13]

+2.5V_MEM

+1.2V_MEM

Layout Note: Place near JDIMM1.258

+0.6V_DDR_VTT

+V_DDR_REFCA_A

DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
* DIMM1	1	0	0
DIMM3	1	1	0

+3.3V_RUN

DIMM1_SA0
DIMM1_SA1
DIMM1_SA2

+3.3V_RUN_DIMM1

JDIMM1A REVERSE

JDIMM1B REVERSE

LOTES_ADDR0206-P001A02~D
CONN@

+0.6V_DDR_VTT
+2.5V_MEM
+V_DDR_REFCA_A

DDR_XDP_WAN_SMBDAT
DDR_XDP_WAN_SMBCLK

DDR_A_DRAMRST#_PCH
DDR_A_DRAMRST#
DDR_B_DRAMRST#

JDIMM1_EVENT#
H_THERMTRIP#

+V_DDR_REFCA_B
+V_DDR_REFCA_A
+DDR_VREF_CA

DDR_VTT_CTRL
0.6V_DDR_VTT_ON

74AUP1G07GW_TSSOP5

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

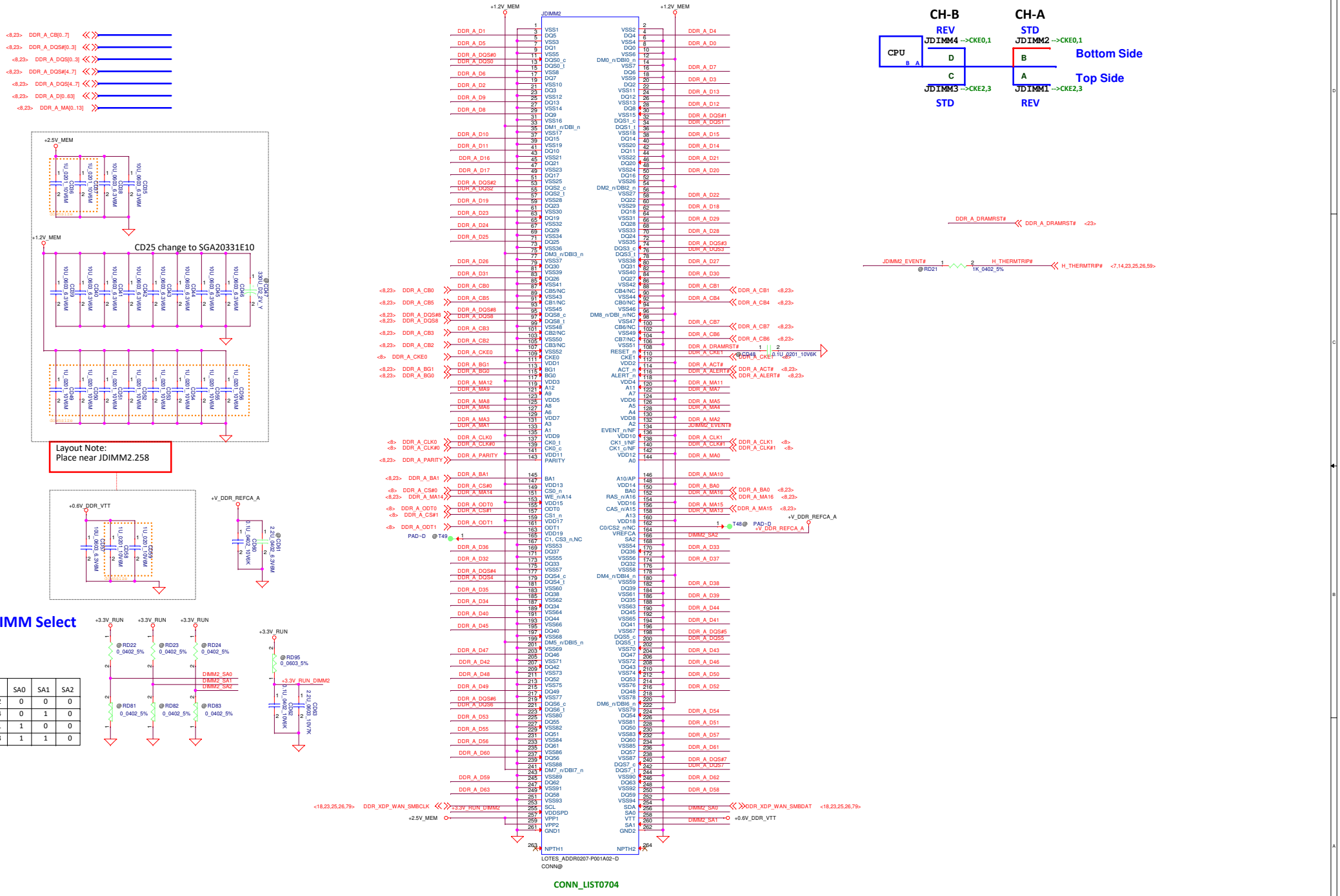
Compal Electronics, Inc.

Title: DDR4_DIMM1

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 23 of 104

JDIMM2 STD Type H=5.2



	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title	*DDR4_DIMM2*
Size	Custom
Document Number	*LA-J171P*
Rev	1.0
Date:	Wednesday, August 26, 2020
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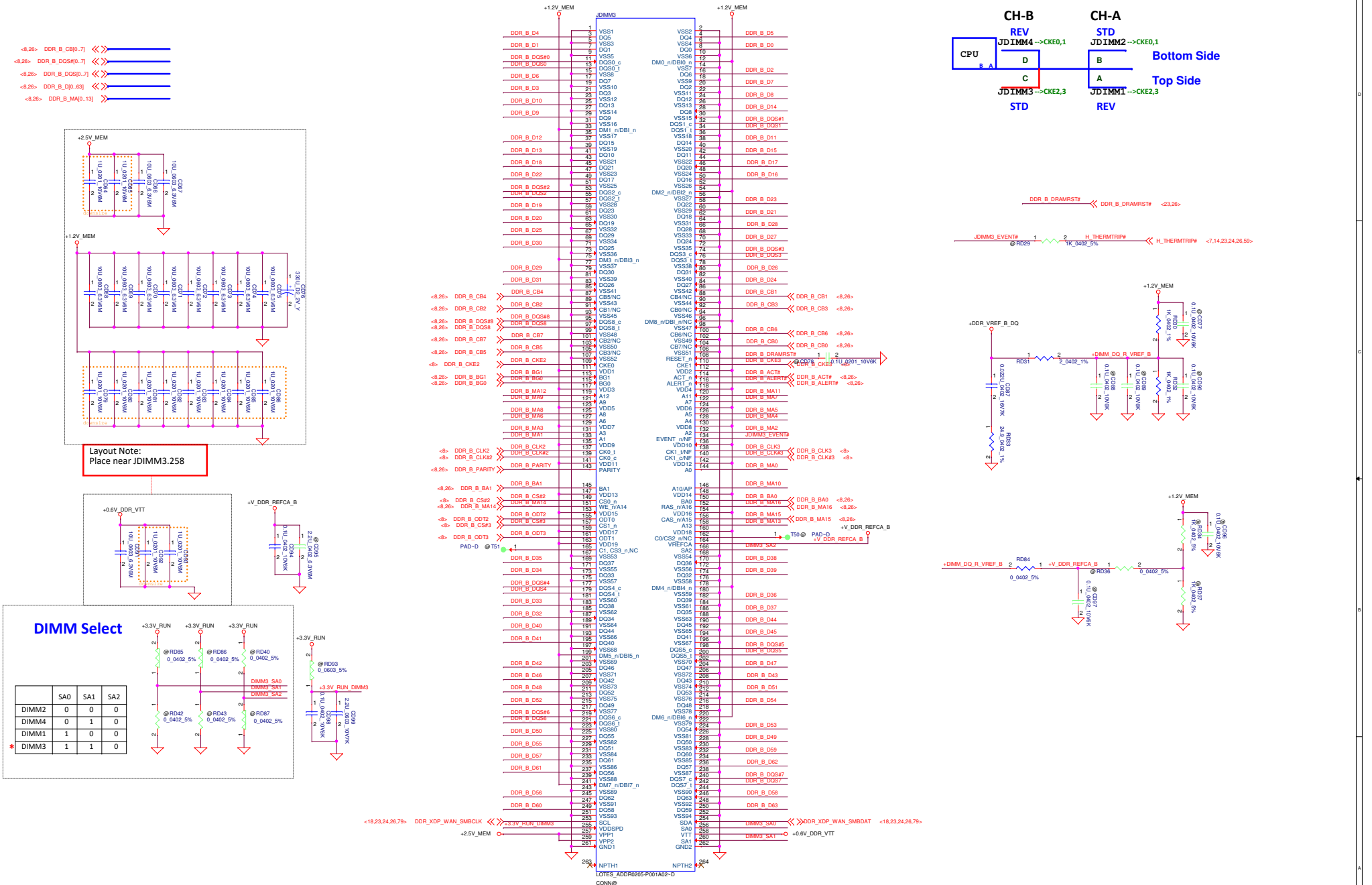
JDIMM3 STD Type H=4



	SA0	SA1	SA2
DIMM2	0	0	0
DIMM4	0	1	0
DIMM1	1	0	0
* DIMM3	1	1	0

CONN_LIST0704

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	DDR4_DIMM3		
Size	Document Number		Rev
Custom	LA-J171P		1.0
Date:	Wednesday, August 26, 2020	Sheet	25 of 104

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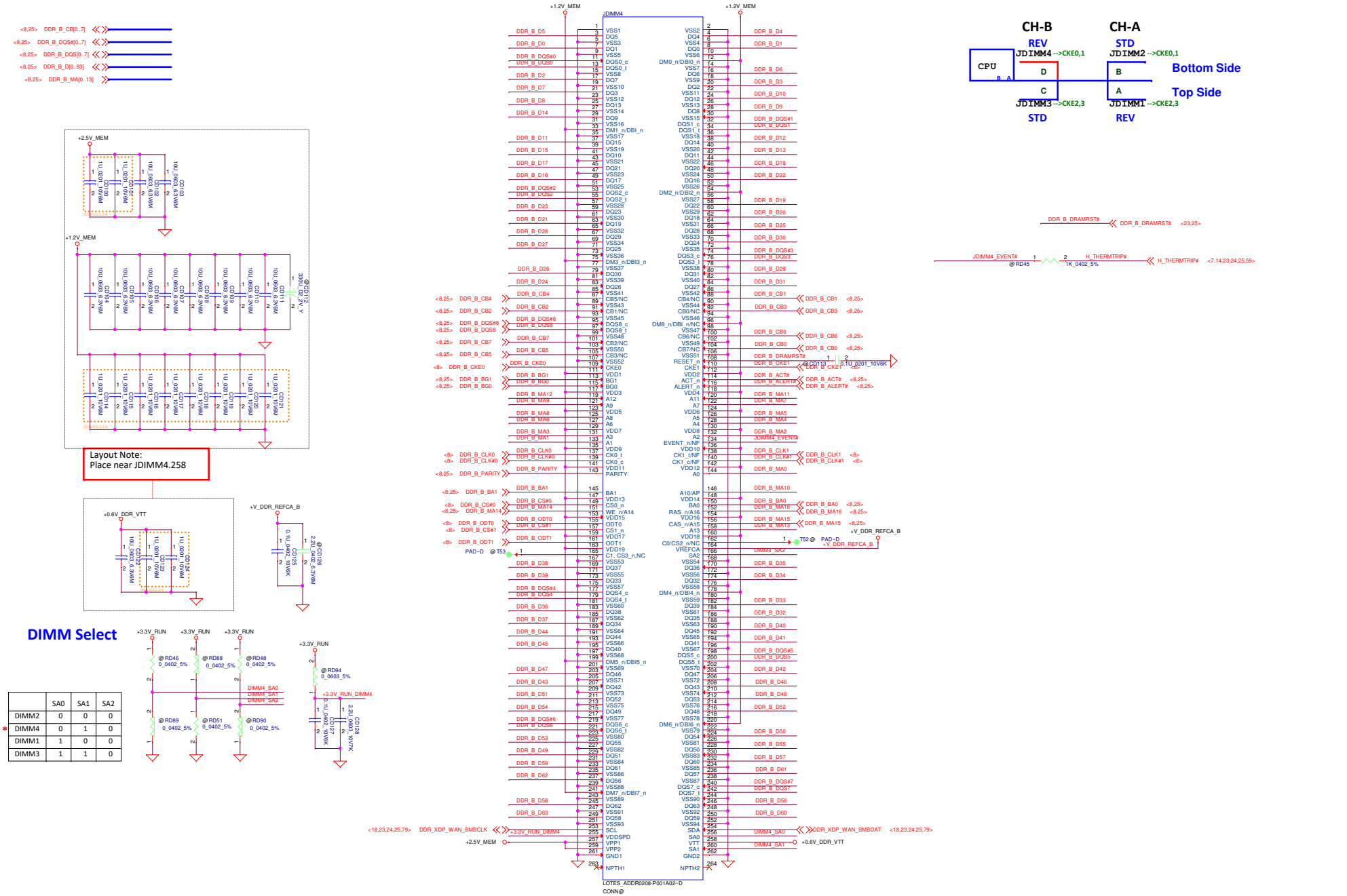
JDIMM4 REV Type H=5.2



Layout Note:
Place near JDIMM4.258

DIMM Select

	SA0	SA1	SA2
DIMM2	0	0	0
* DIMM4	0	1	0
DIMM1	1	0	0
DIMM3	1	1	0

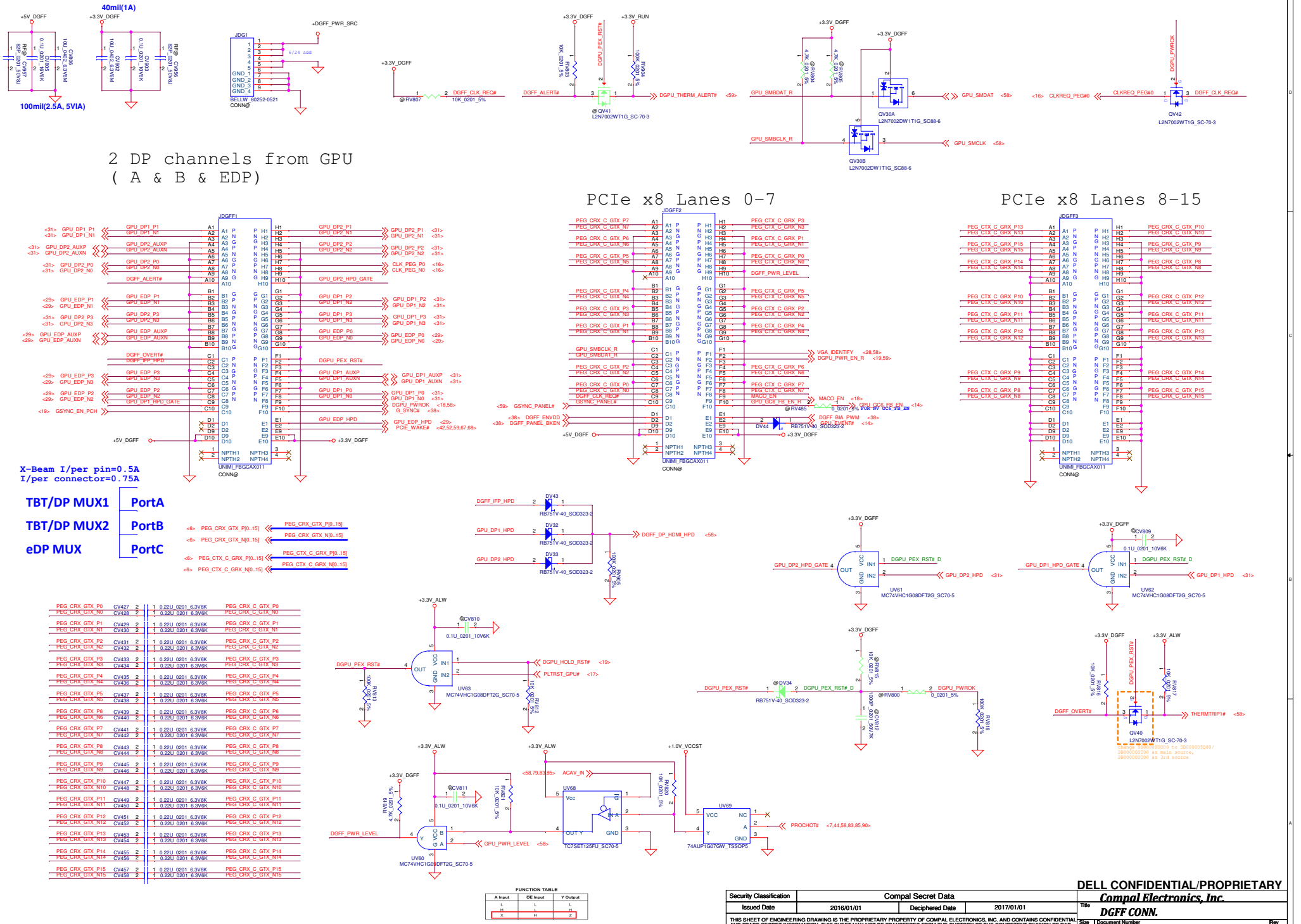
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DDR4_DIMM4

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 26 of 104


40mil(1A)
100mil(2.5A, 5VIA)
2 DP channels from GPU
(A & B & EDP)
PCIe x8 Lanes 0-7
PCIe x8 Lanes 8-15
X-Beam I/per pin=0.5A
I/per connector=0.75A
TBT/DP MUX1 PortA
TBT/DP MUX2 PortB
eDP MUX PortC
FUNCTION TABLE
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
DGFF CONN.
Security Classification
Compal Secret Data
Issued Date
2016/01/01
Deciphered Date
2017/01/01
LA-J171P
Rev 1.0
Wednesday, August 26, 2020
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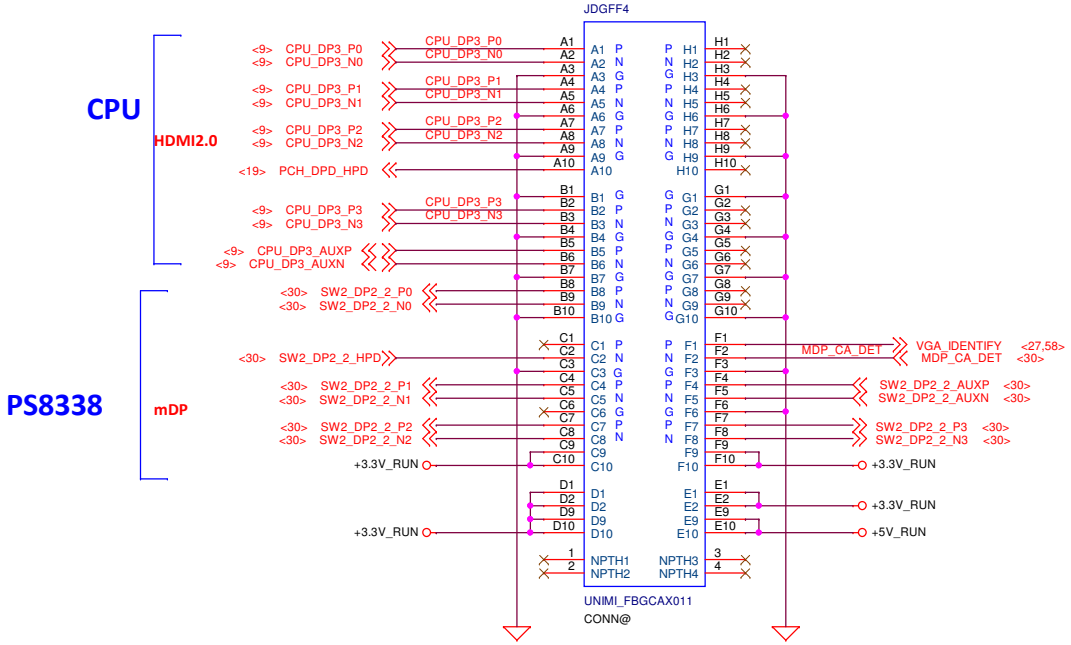
UMA DGFF CON.



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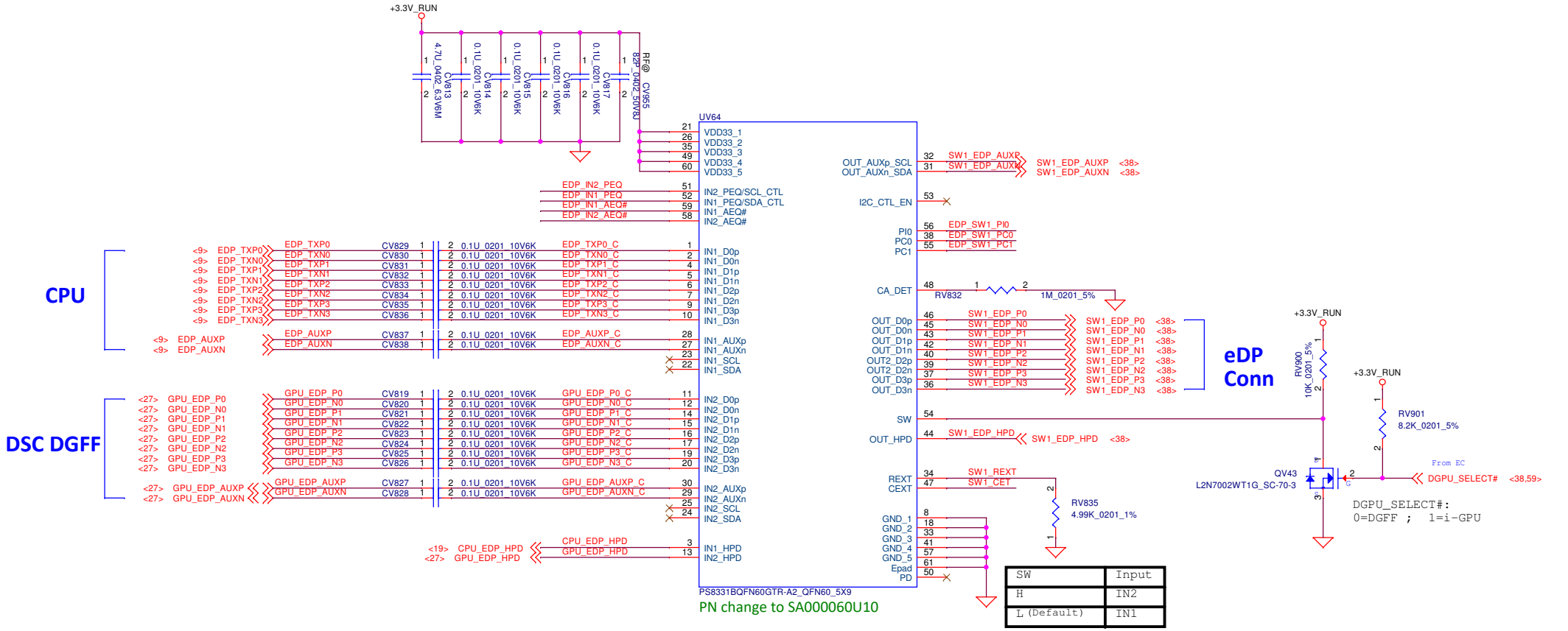
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DGFF CONN.

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 28 of 104



INy_PEQ = Programmable input equalization levels
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
H: HEQ, compensate channel loss up to 14.5dB @ HBR2
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

INy_AEQ# = Automatic EQ disable
L: Automatic EQ enable (default)
H: Automatic EQ disable

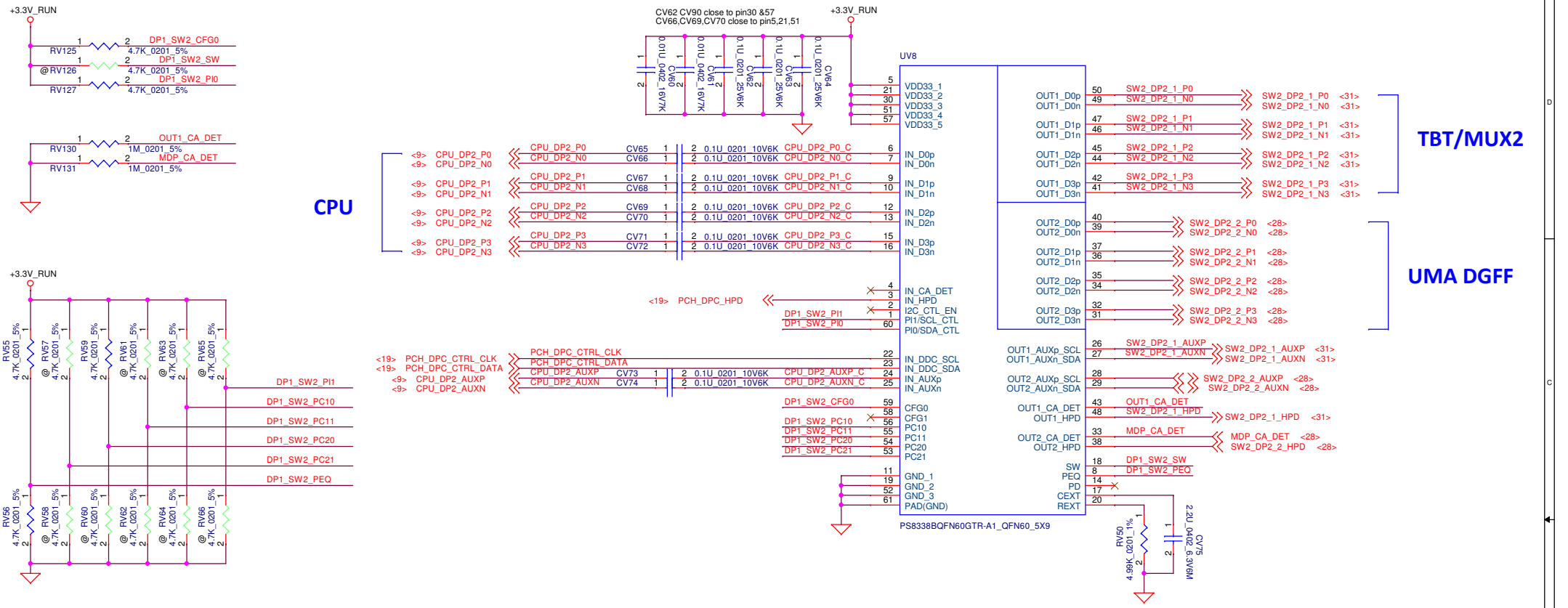
PI0 = Auto test enable
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

PC0 = AUX interception disable
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

PC1 = Output swing adjustment
L: default
H: +20%
M: -16.7%

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: eDP MUX (PS8331)			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 29 of 104		



PCy0 (3 level input)	I	AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O; PCy0 = L: AUX interception enable, driver configuration is set by link training (default) H: AUX interception disable, driver output with fixed 800mV and 0dB M: AUX interception disable, driver output with fixed 400mV and 0dB ***Overwritten by I2C register in I2C Control Mode***
PCy1 (3 level input)	I	Output swing adjustment for Port y (y = 1, 2). Internal pull down at ~150KΩ, 3.3V I/O; PCy0 = L: default H: +20% M: -16.7% ***Overwritten by I2C register in I2C Control Mode***

Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H): (By OUT1_HPD and OUT2_HPD)
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

	H	L
CFG0	V	
SW		V

Programmable input equalization levels. Internal pull down at ~150KΩ, 3.3V I/O

PEQ =

L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2

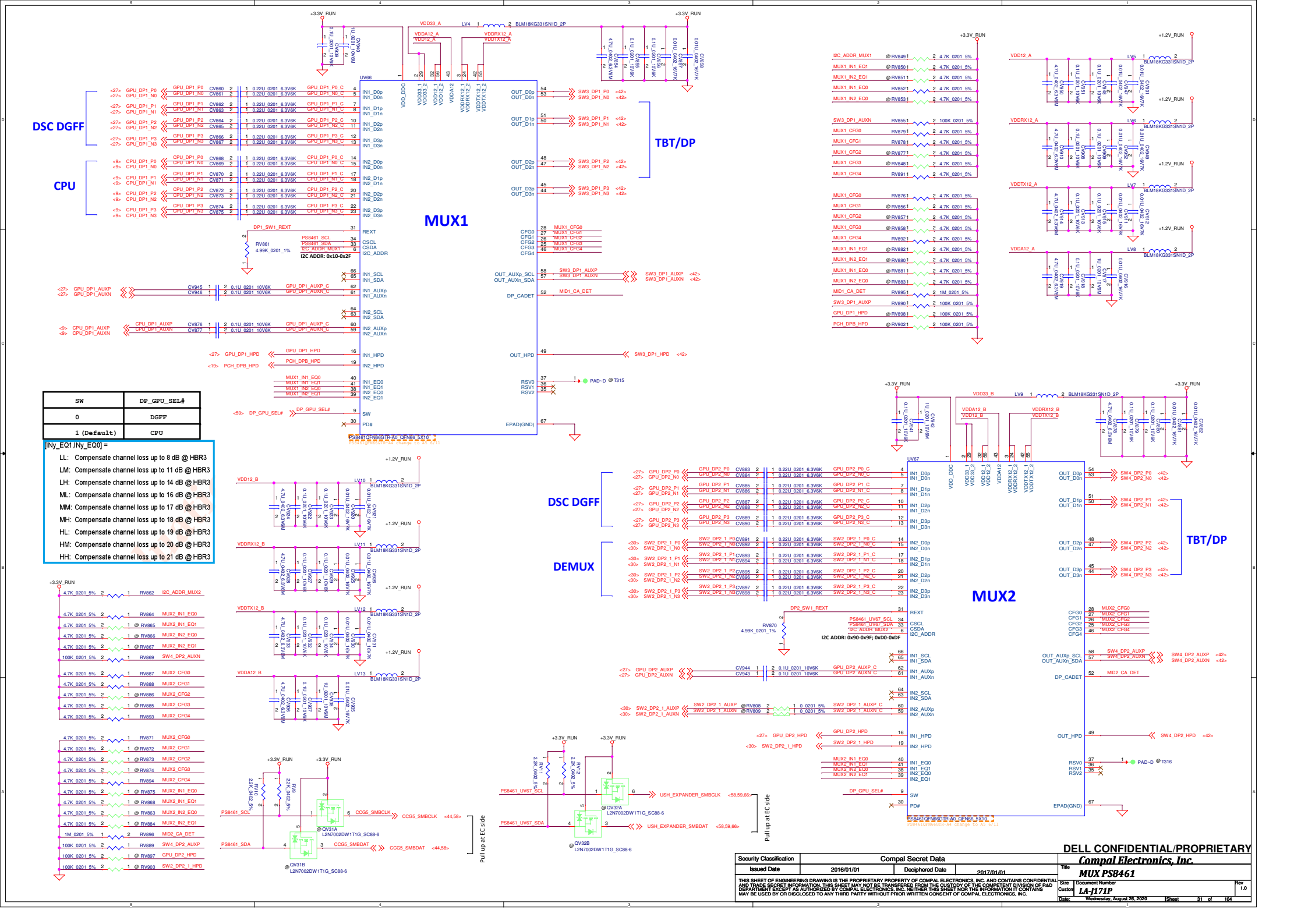
H: HEQ, compensate channel loss up to 14.5dB @ HBR2

M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

Overwritten by I2C register in I2C Control Mode

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: DP DeMUX (PS8338)			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 30 of 104		



SW	DP_GPU_SEL#
0	DGFF
1 (Default)	CPU

[INy_EQ1,INy_EQ0] =

LL: Compensate channel loss up to 8 dB @ HBR3
LM: Compensate channel loss up to 11 dB @ HBR3
LH: Compensate channel loss up to 14 dB @ HBR3
ML: Compensate channel loss up to 16 dB @ HBR3
MM: Compensate channel loss up to 17 dB @ HBR3
MH: Compensate channel loss up to 18 dB @ HBR3
HL: Compensate channel loss up to 19 dB @ HBR3
HM: Compensate channel loss up to 20 dB @ HBR3
HH: Compensate channel loss up to 21 dB @ HBR3

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: MUX PS8461

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 31 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: DGPU		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 32 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: DGPU		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 33 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: DGPU		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 34 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: DGPU		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 35 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: DGPU		
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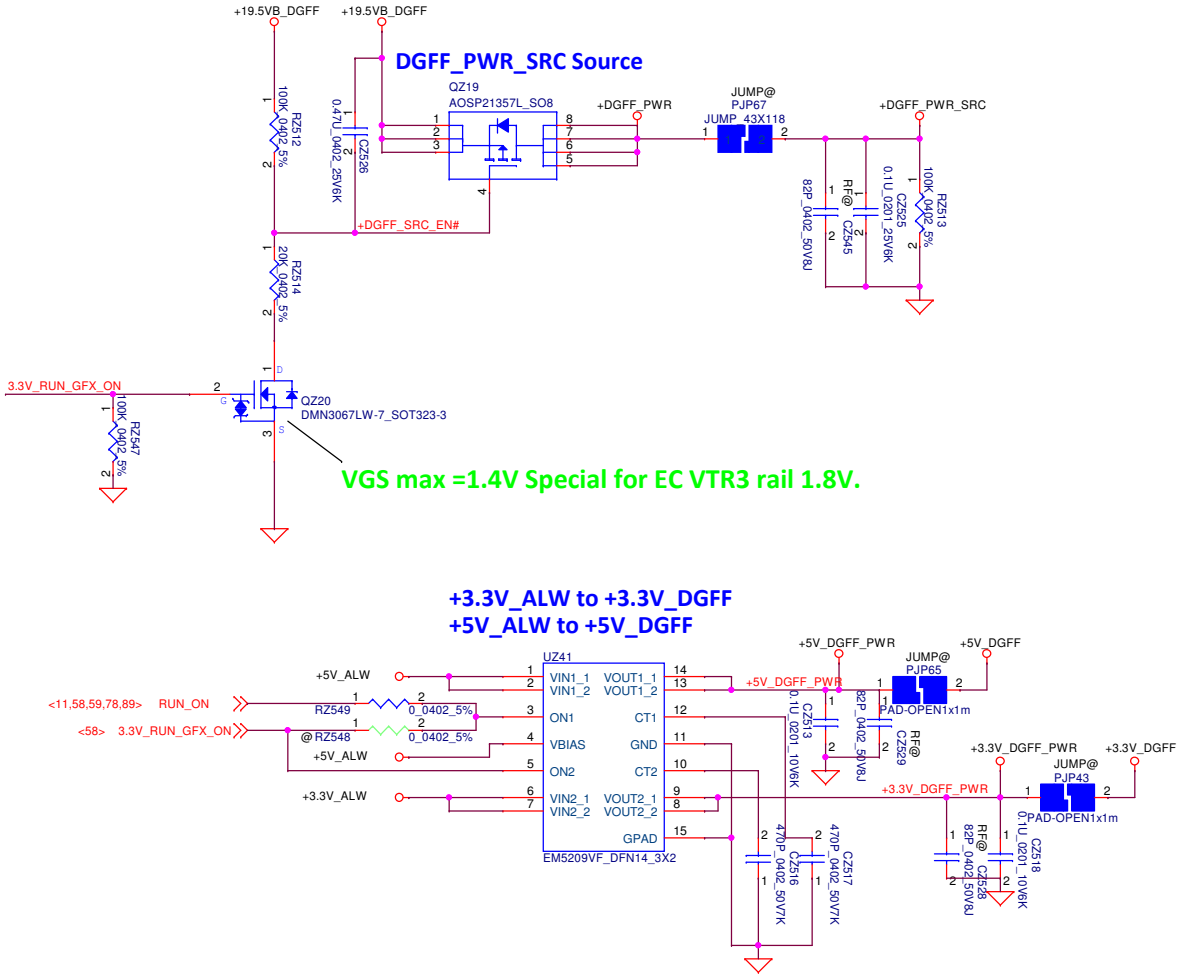

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DGFF DC/DC Interface

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 37 of 104

same 111H40-100100-G4-R

TOUCH SCREEN & IR CAMERA connector

140mA

Touch pull up at the panel side

For ESD request

6/27 for layout routing change

Close to JEDP1

PS8331 HPD input internal PD 150K

Close to JEDP1

Webcam PWR CTRL

Close to JIR1 pin5,pin6

Close to JIR1 pin26,pin27

Soft start

LCD Power

60mil

60mil

RF require

RF require

Panel backlight power control by EC

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: eDP / CAM / TS/ IR

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 38 of 104

Reserve

Compal Electronics, Inc.		
Title: IR/TS/LCD Monitor		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 39 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: HDMI2.0		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 40 of 104	

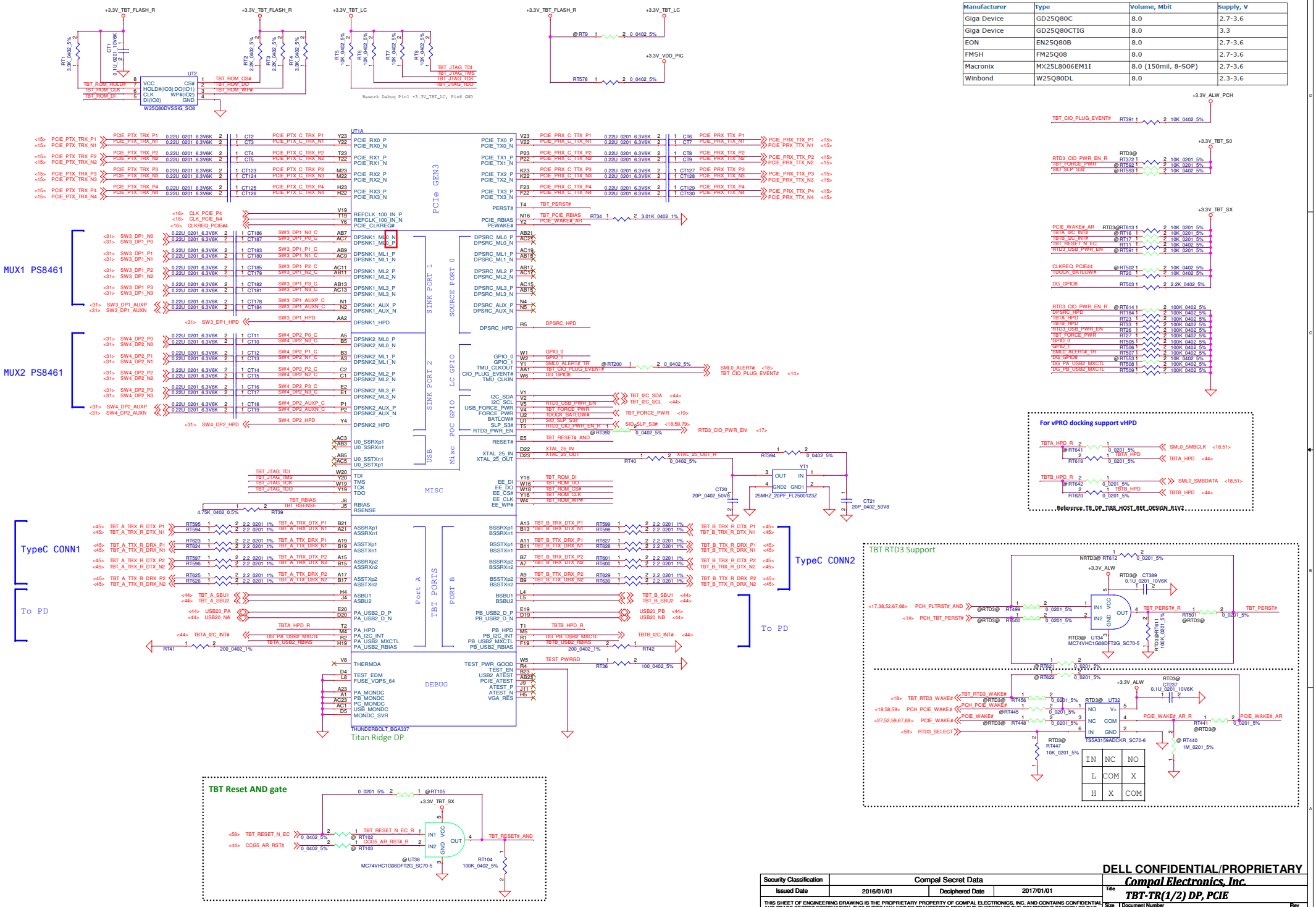
Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: CRT		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 41 of 104	

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6



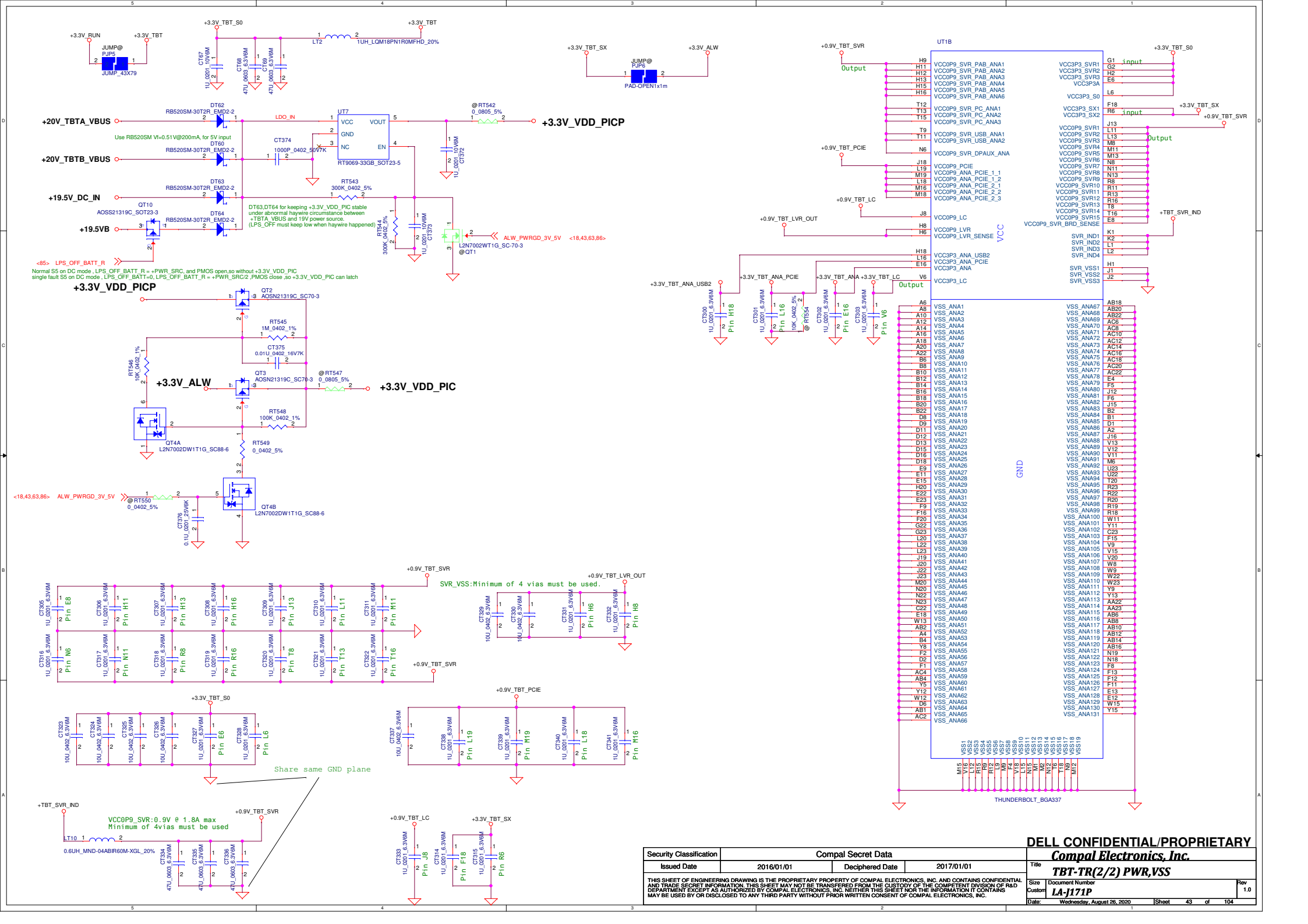
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: TBT-TR(1/2) DP, PCIE

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 42 of 104



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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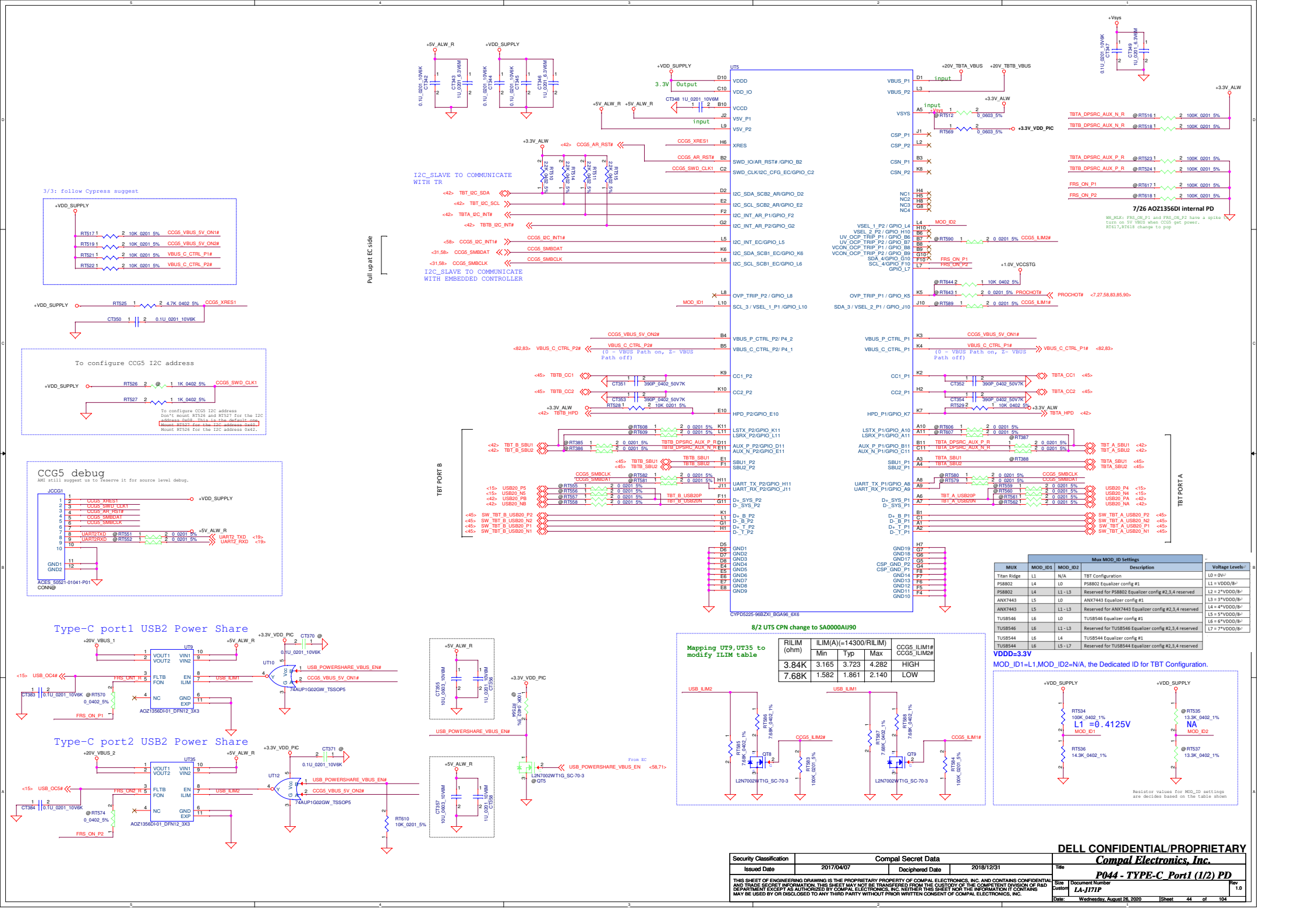
Compal Electronics, Inc.

Title: *TBT-TR(2/2) PWR,VSS*

Size	Document Number	Rev
Custom	*LA-J171P*	1.0

Date: Wednesday, August 26, 2020 | Sheet 43 of 104



Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

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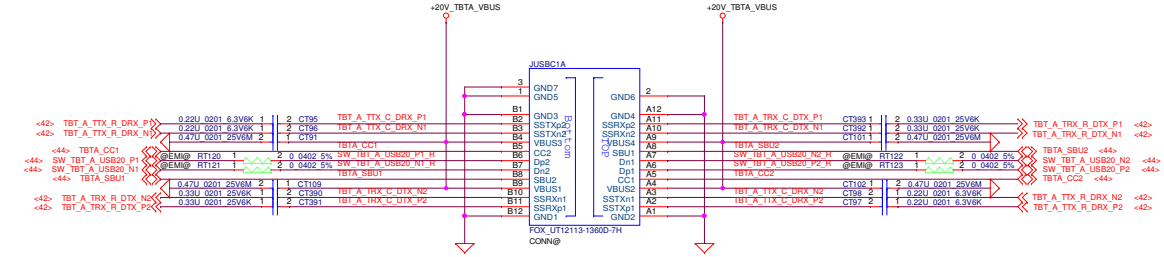
Compal Electronics, Inc.

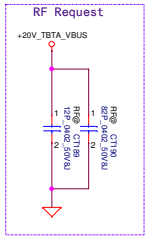
Title: **P044 - TYPE-C_Port1 (1/2) PD**

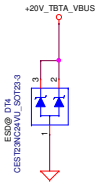
Size	Document Number	Rev
Custom	LA-J171P	1.0

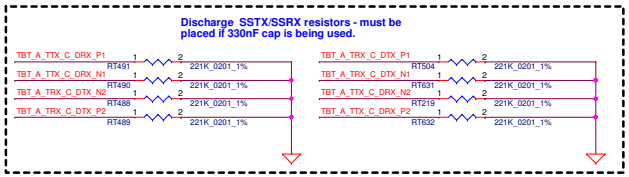
Date: Wednesday, August 26, 2020 | Sheet 44 of 104

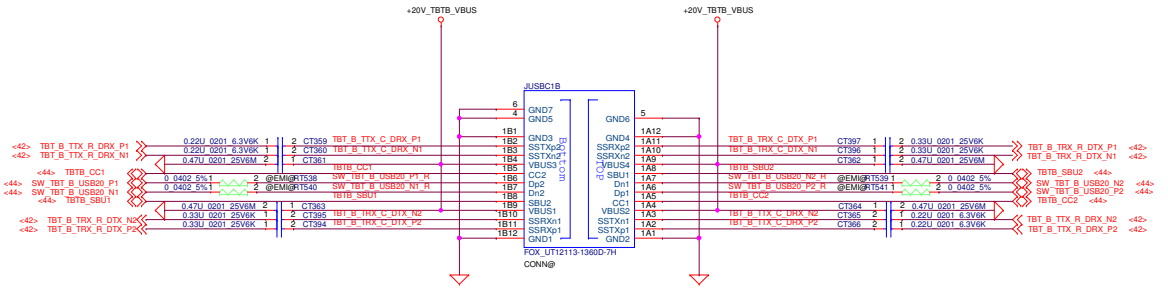


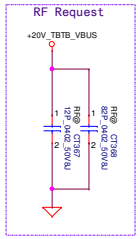
CONN_LIST0702

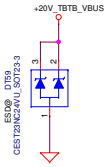


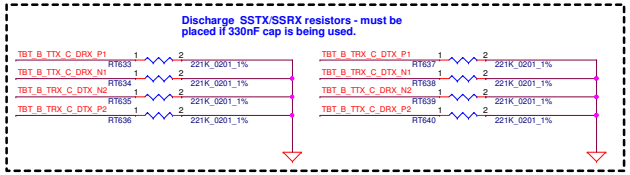


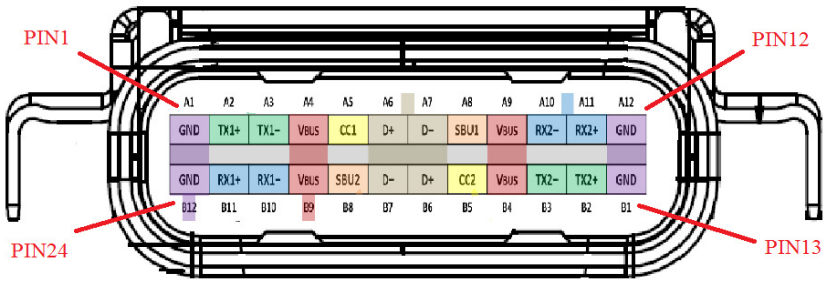


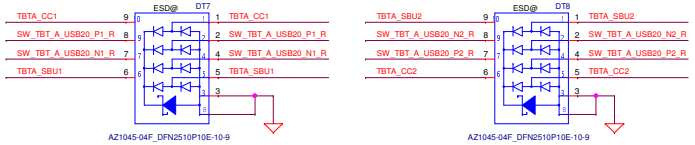


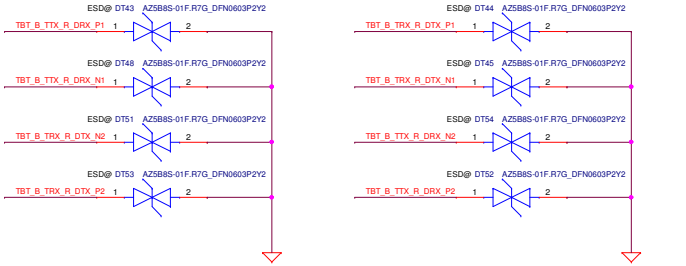


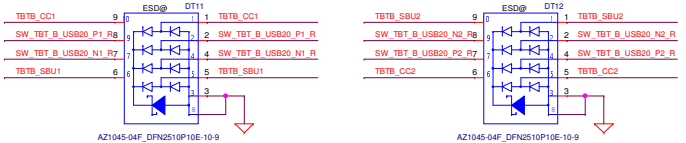












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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: TYPE-C_Port1 (2/2) CONN

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 45 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: *TYPE-C_Port2-1*

Size: Custom | Document Number: *LA-J171P* | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 46 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: TYPE-C_Port2-2			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 47 of 104		

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: TYPE-C_Port3-1			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 48 of 104		

Reserve

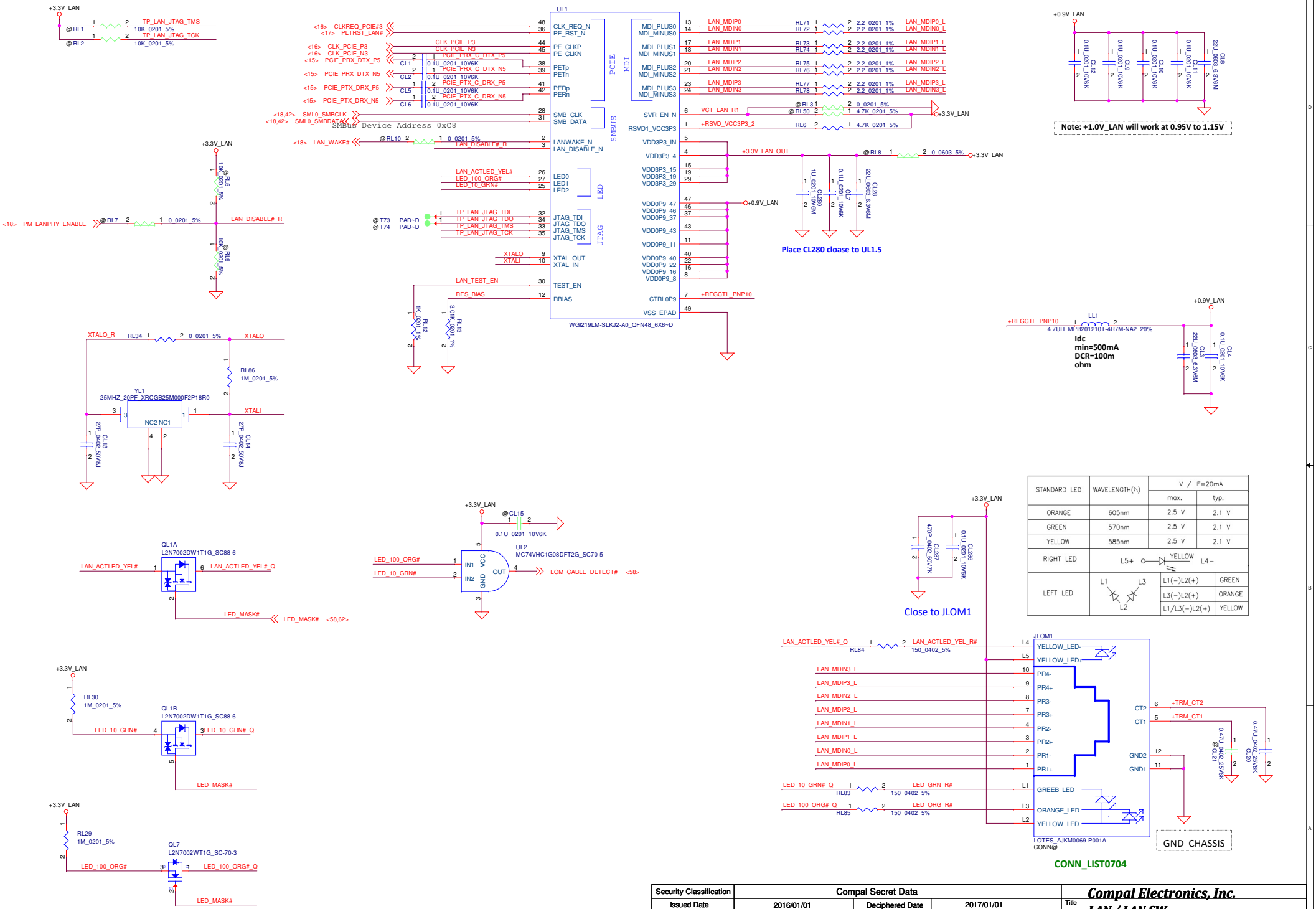
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: TYPE-C_Port3-2		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 49 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: TYPE-C_PWR Path			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 50 of 104		



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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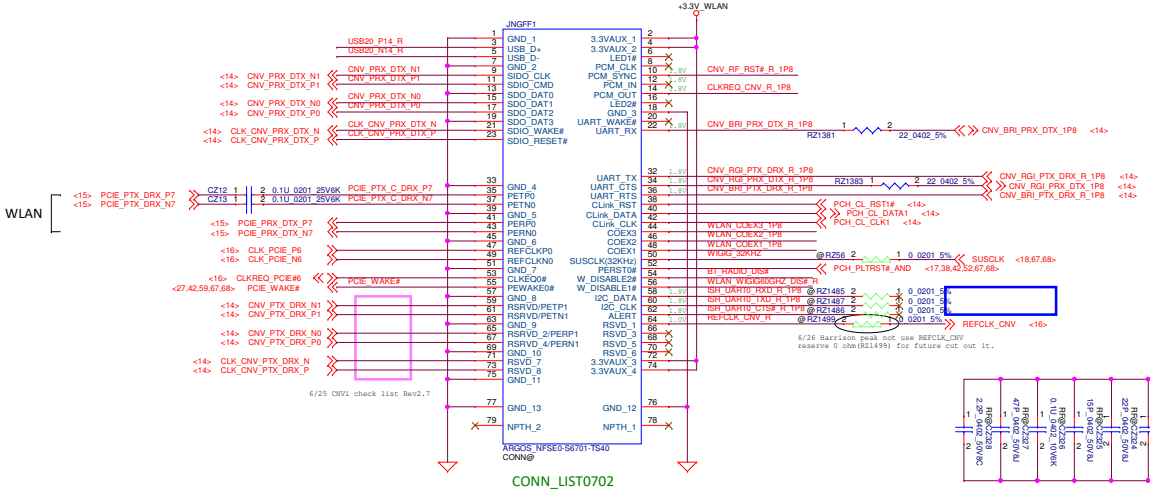
Compal Electronics, Inc.

Title: **LAN / LAN SW**

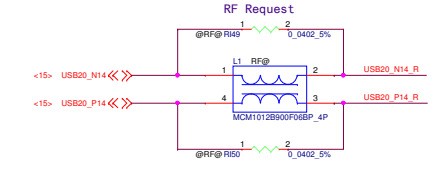
Size	Document Number	Rev
Custom	LA-J171P	1.0

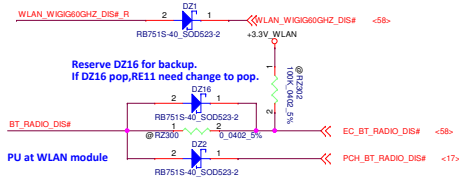
Date: Wednesday, August 26, 2020 | Sheet 51 of 104

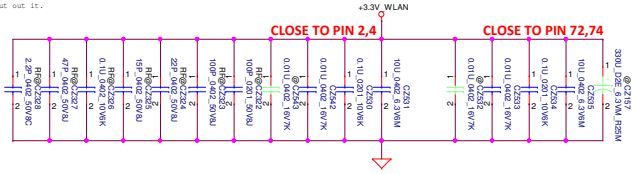
WLAN/CNVi
NGFF slot_1 Key E

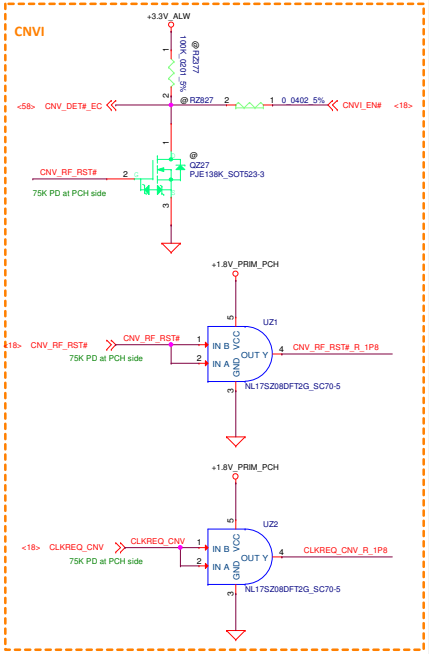


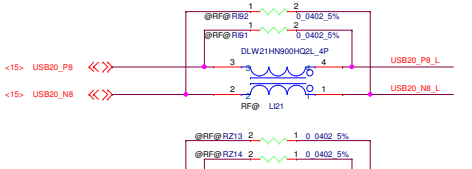
CONN_LIST0702

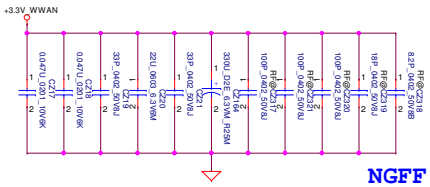




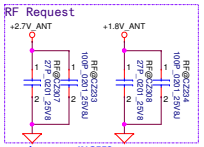


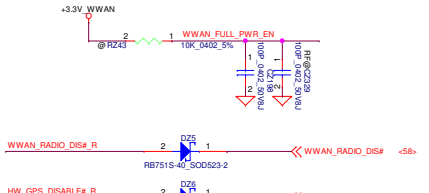


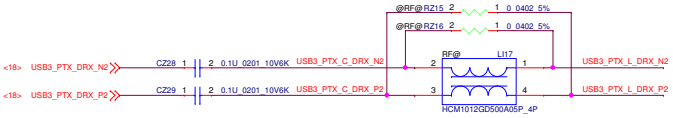


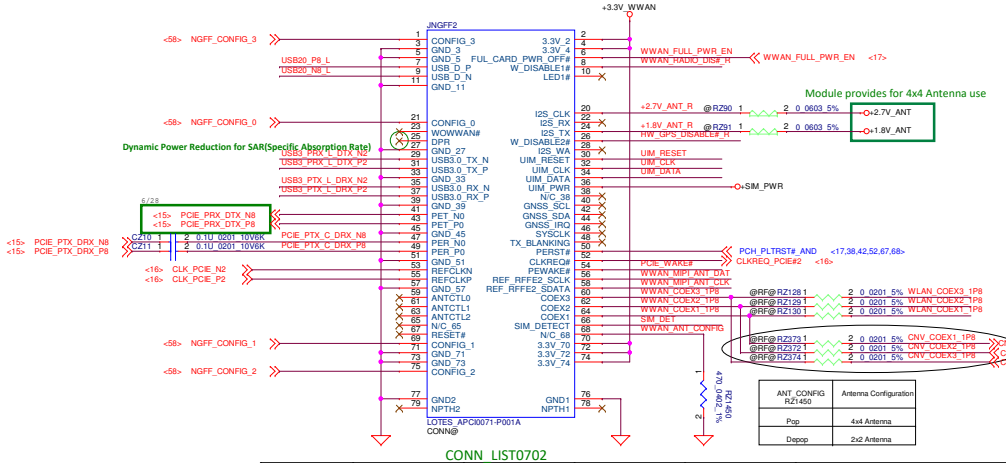


WWAN/LTE
NGFF slot_2 Key B



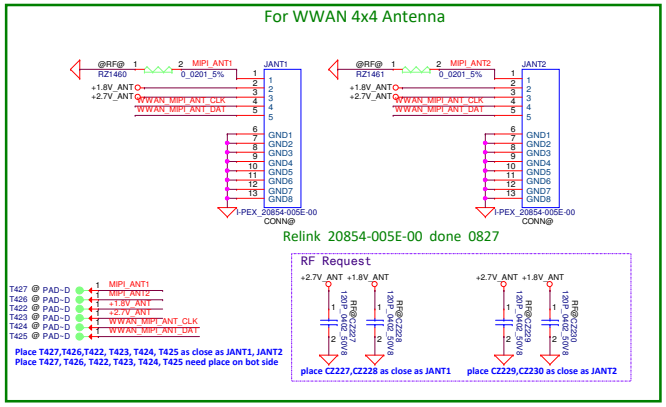




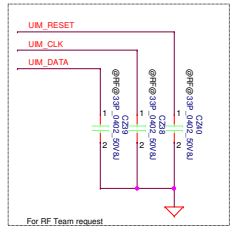


CONN_LIST0702

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
4	0	0	0	1	WWAN-USB3.1 Gen1



WWAN_MIPI_ANT_DAT and WWAN_MIPI_ANT_CLK
(1)The trace length < 30cm
This max length guidance is practical level of definition.
(2)Spacing to all other signal need 4x line width



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title: WLAN (w/ CNVi) / WWAN
Size: Custom | Document Number: LA-J171P | Rev: 1.0
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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: WIGIG / WIDI			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
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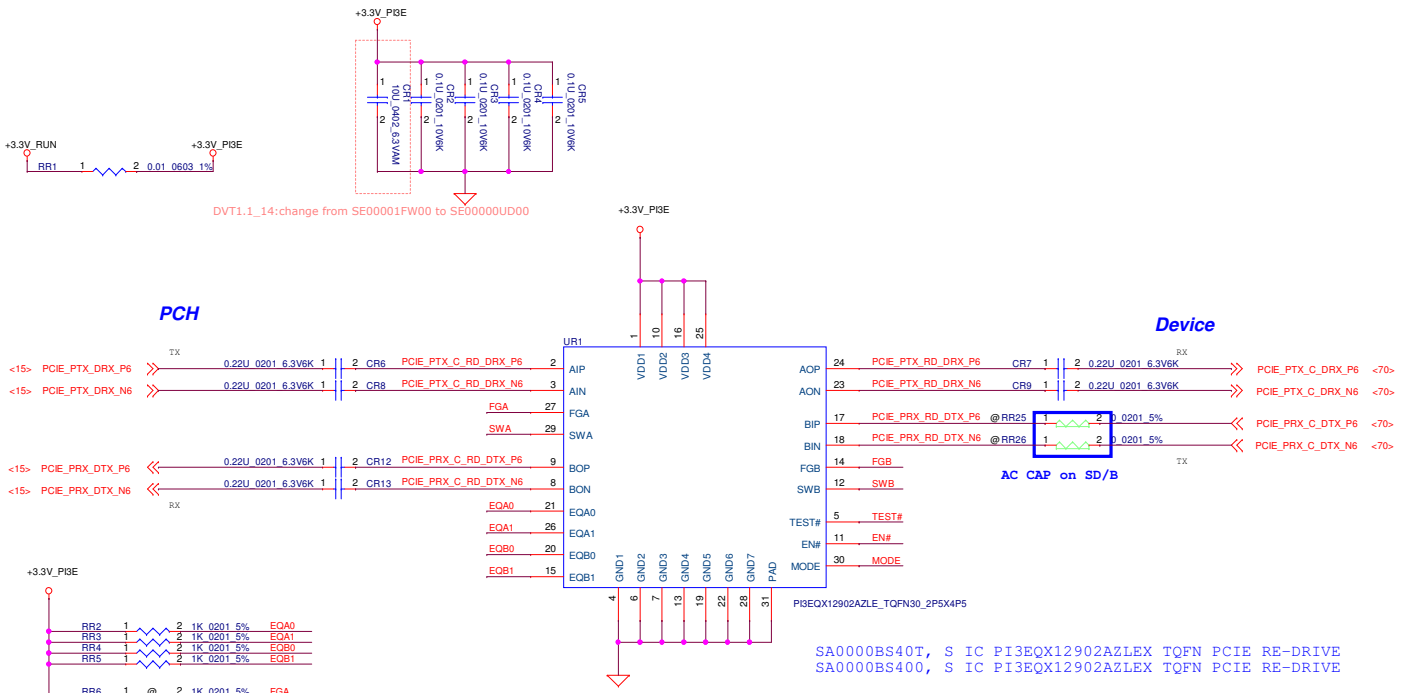
Card reader PCIE Redirver



SA0000BS40T, S IC PI3EQX12902AZLEX TQFN PCIE RE-DRIVE
SA0000BS400, S IC PI3EQX12902AZLEX TQFN PCIE RE-DRIVE

Operation MODE pin.
"High" - For PCIe applications.
"Low" - For SATA applications

Test mode Enable pin. With internal 300kΩ pull-up resistor.
"High" - Test mode disabled.
"Low" - Test mode enabled.

Channel Enable pin. With internal 300kΩ pull down resistor.
"High" - Channel is in power down mode.
"Low" - Channel is in normal operation.

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	Redriver-PI3EQX12902AZLE		
Size	Document Number		Rev
Custom	LA-J171P		1.0
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Reserve

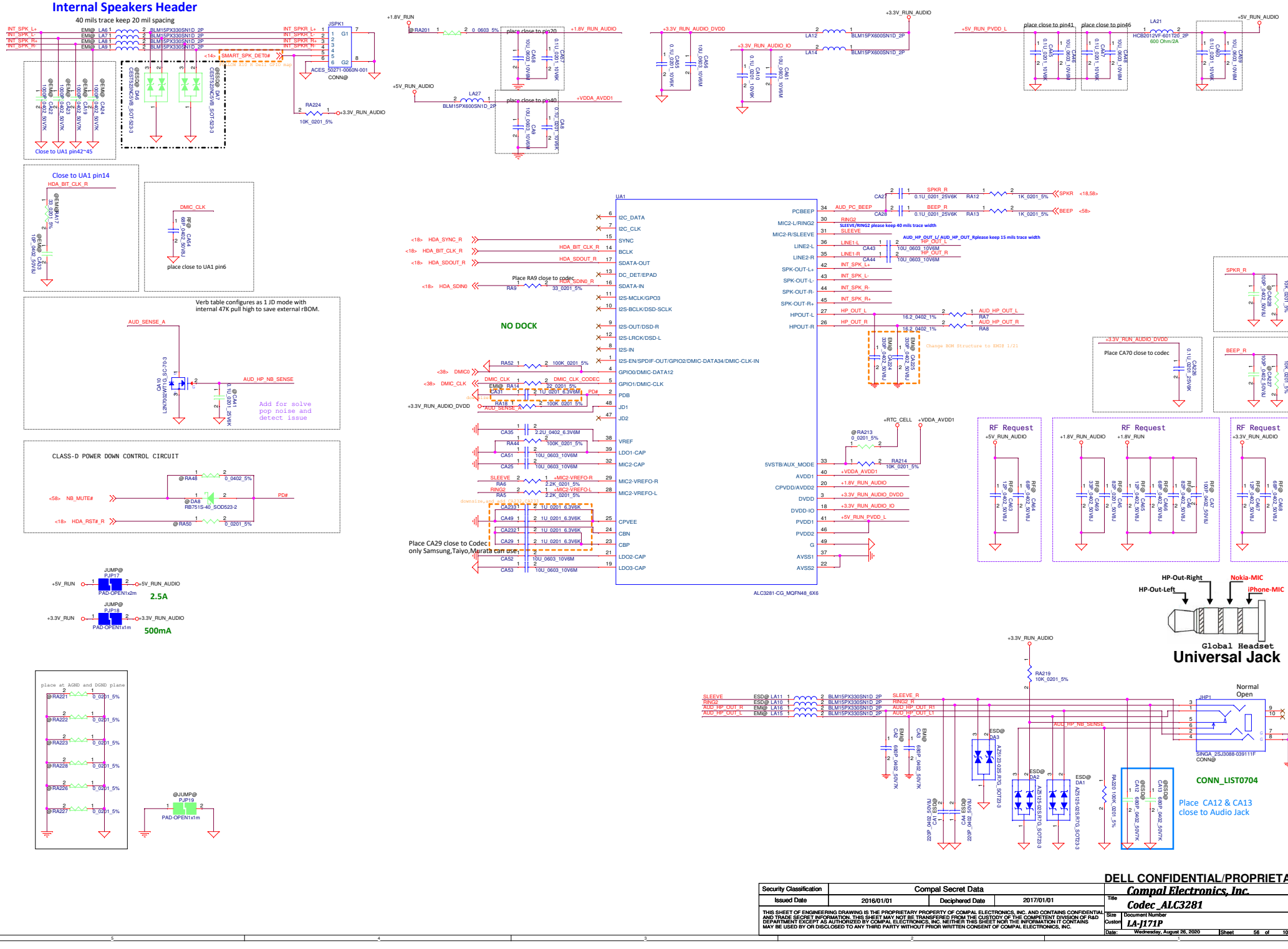
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: PCIE device			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 55 of 104		

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing



Compal Electronics, Inc.

Title: Codec_ALC3281

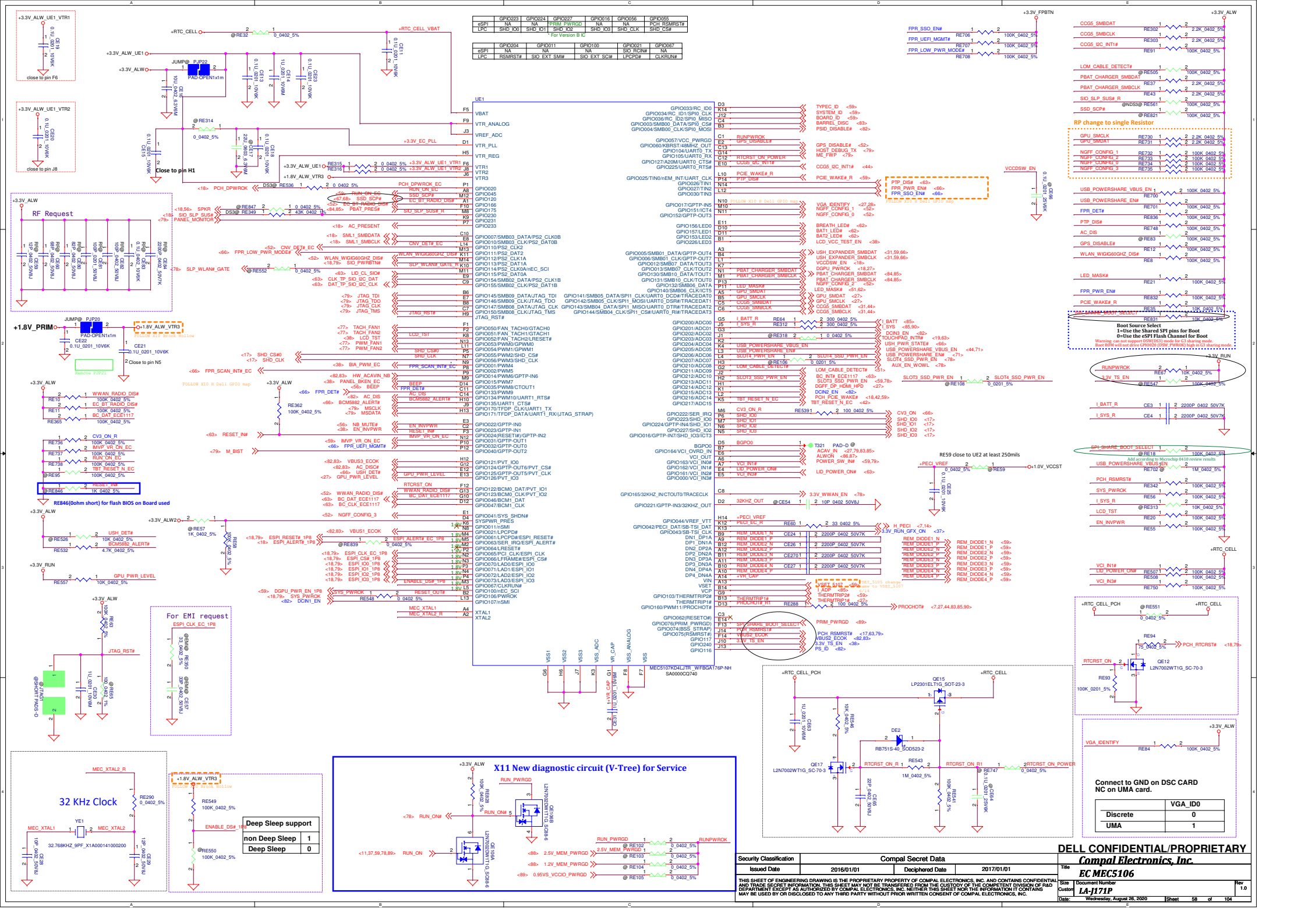
Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 56 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: Audio Ampfilper		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 57 of 104	



	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

Deep Sleep support	
non Deep Sleep	1
Deep Sleep	0

	VGA_ID0
Discrete	0
UMA	1

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Compal Electronics, Inc.

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: EC MEC5106

Size: Custom | Document Number: LA-J171P | Rev: 1.0

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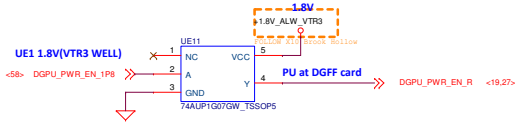
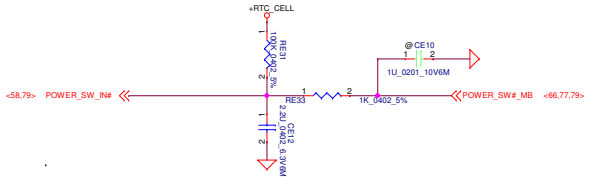
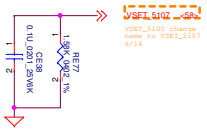
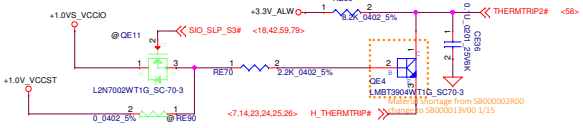
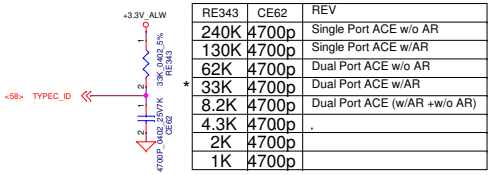


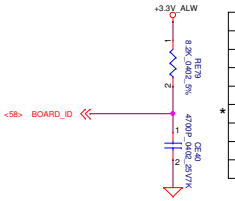




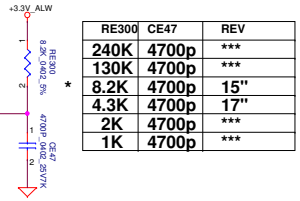




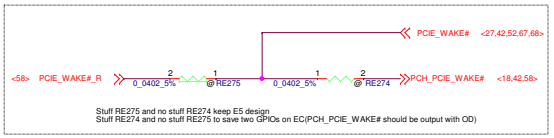
RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	



RE79	CE40	REV
240K	4700p	X00(EVT1.0)
130K	4700p	X01(DVT1.0)
62K	4700p	X01(DVT1.1)
33K	4700p	X02(DVT2.0)
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	



RE300	CE47	REV
240K	4700p	***
130K	4700p	***
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	***
1K	4700p	***

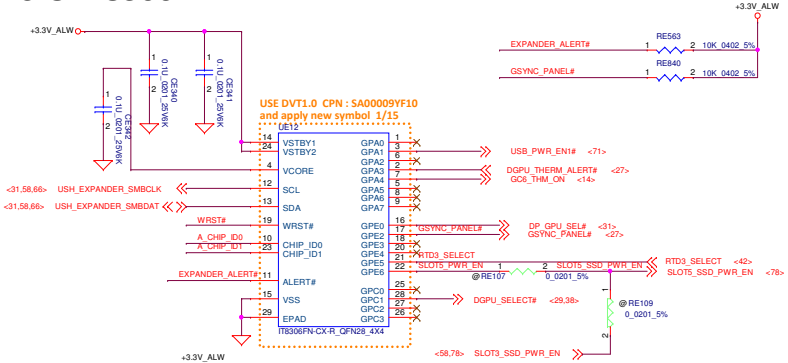


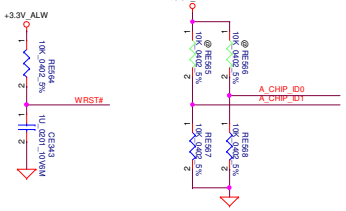
TypeC_ID rise time is measured from 5%~68%.

BOARD_ID rise time is measured from 5%~68%.

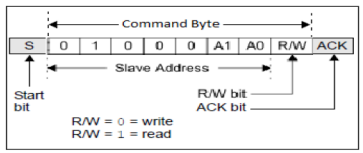
PANEL_ID rise time is measured from 5%~68%

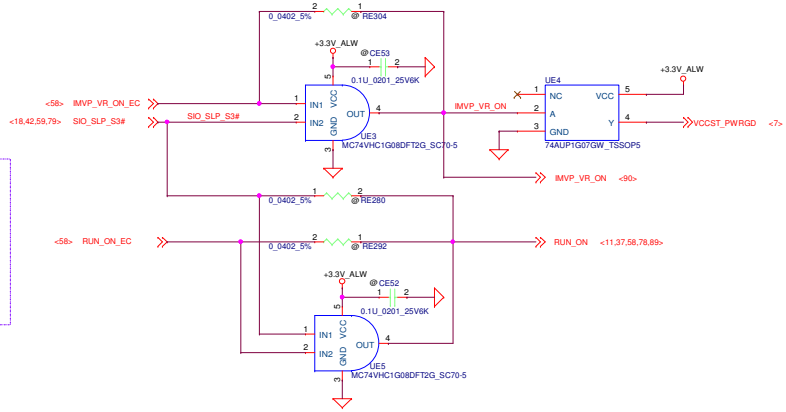
SIO IT8306






```
For I2C SAD+Read/Write patterns
Command SAD[7:3],ID[1],ID[0],R/W=  SAD+R/W
 Read    01000    0    0    1    01000001 (41h)
 Write   01000    0    0    0    01000000 (40h)
 Read    01000    0    1    1    01000011 (43h)
 Write   01000    0    1    0    01000010 (42h)
 Read    01000    1    0    1    01000101 (45h)
 Write   01000    1    0    0    01000100 (44h)
 Read    01000    1    1    1    01000111 (47h)
 Write   01000    1    1    0    01000110 (46h)
```

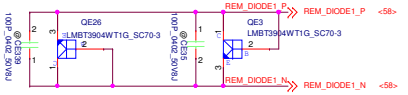




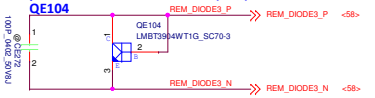
Channel	Location
DP1/DN1	CPU OTP
DP1A/DN1A	CPU VR
DP2A/DN2A	M.2 2280
DP3/DN3	DIMM(TOP)
DP4/DN4	WWAN

DP1/DN1 for CPU OTP on QE3, place QE3 close to CPU and CE35 close to QE3.

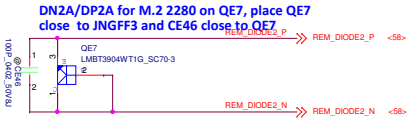
DN1a/DP1a for CPU VR(PU1100) on QE26, place QE26 close to CPU and CE339 close to QE26



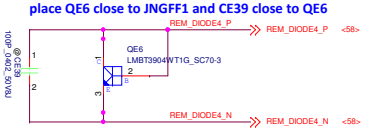
DP3/DN3 for SODIMM(TOP) on QE104, place QE104 close to SODIMM(TOP) and CE272 close to QE104



DN2A/DP2A for M.2 2280 on QE7, place QE7 close to JNGFF3 and CE46 close to QE7



DP4/DN4 for WWAN on QE6, place QE6 close to JNGFF1 and CE39 close to QE6



QE26,QE3,QE104,QE7,QE6 change from SB000008P00 to SB000013V00

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: EC MEC5106 SUPPORT

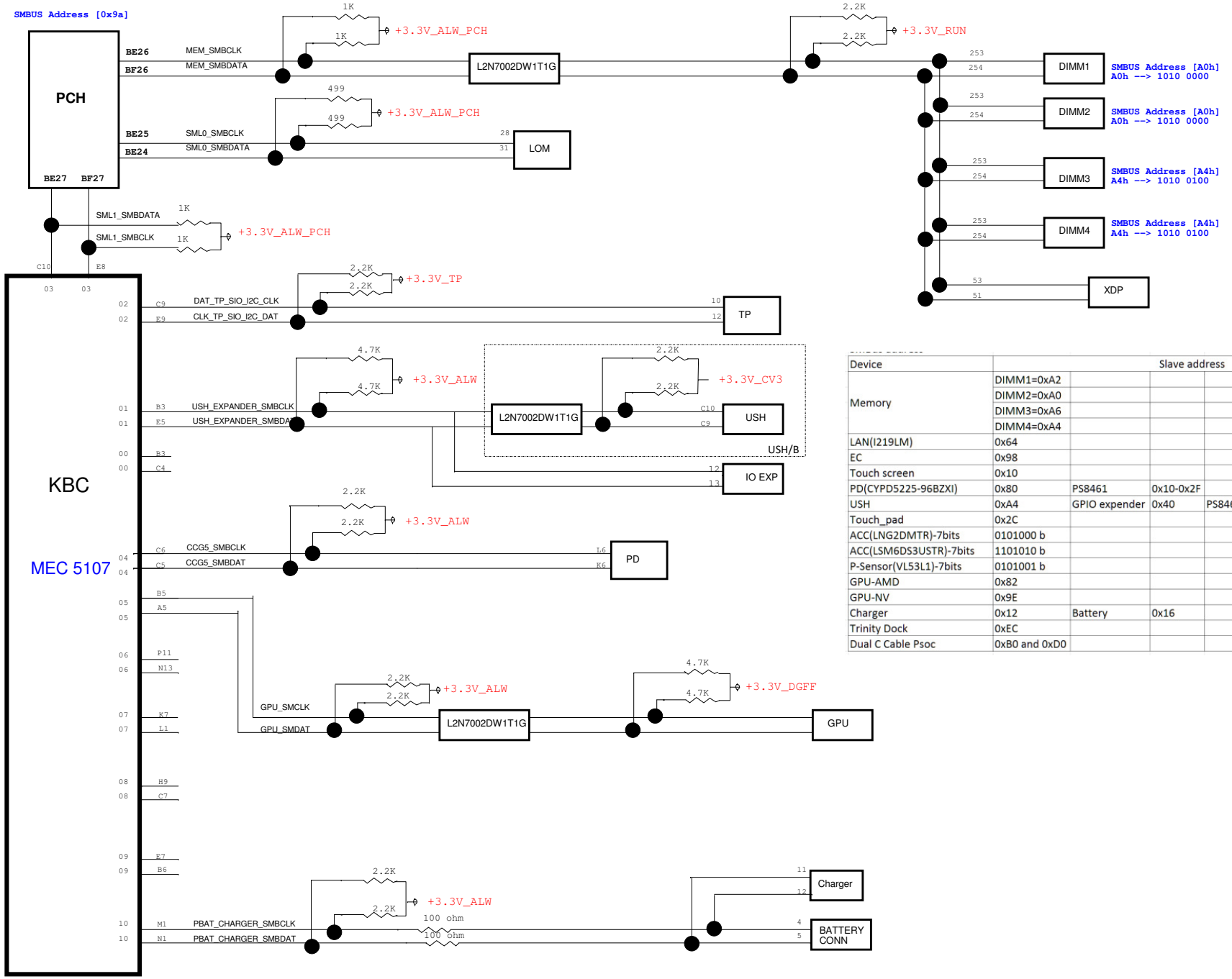
Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 59 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: Secure & Reset IC		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 60 of 104	



Device	Slave address				
Memory	DIMM1=0xA2				
	DIMM2=0xA0				
	DIMM3=0xA6				
	DIMM4=0xA4				
LAN(I219LM)	0x64				
EC	0x98				
Touch screen	0x10				
PD(CYPD5225-96BZXI)	0x80	PS8461	0x10-0x2F		
USH	0xA4	GPIO expender	0x40	PS8461_UV67	0x90-0x9F,0xD0-0xDF
Touch_pad	0x2C				
ACC(LNG2DMTR)-7bits	0101000 b				
ACC(LSM6DS3USTR)-7bits	1101010 b				
P-Sensor(VL53L1)-7bits	0101001 b				
GPU-AMD	0x82				
GPU-NV	0x9E				
Charger	0x12	Battery	0x16		
Trinity Dock	0xEC				
Dual C Cable Psoc	0xB0 and 0xD0				

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

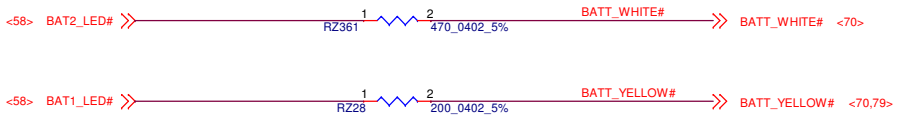
Compal Electronics, Inc.

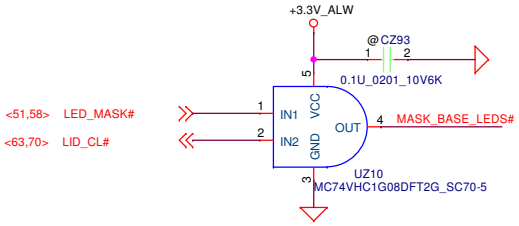
Title: SMbus Block Diagrams

Size	Document Number	Rev
C	LA-J171P	1.0

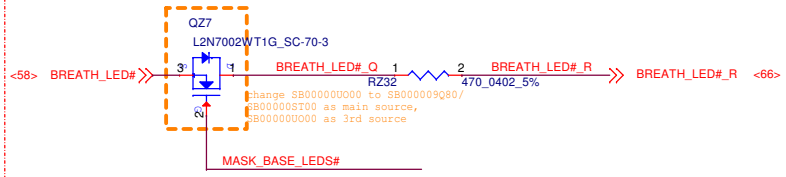
Date: Wednesday, August 26, 2020 Sheet 61 of 104

Battery LED





Breath LED



LED Circuit Control Table		
	LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

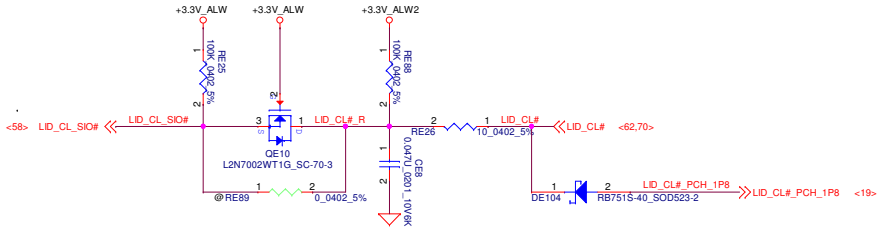
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

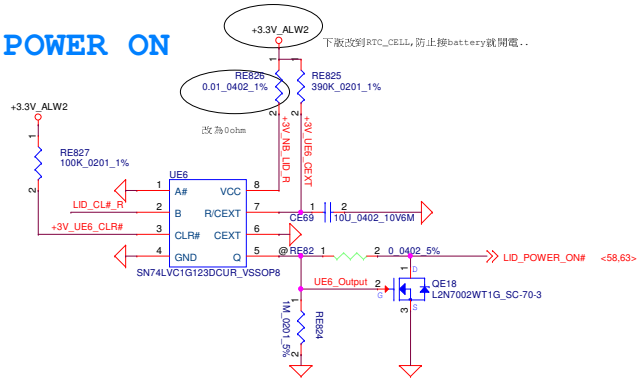
Title: LEDs Controller

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 62 of 104



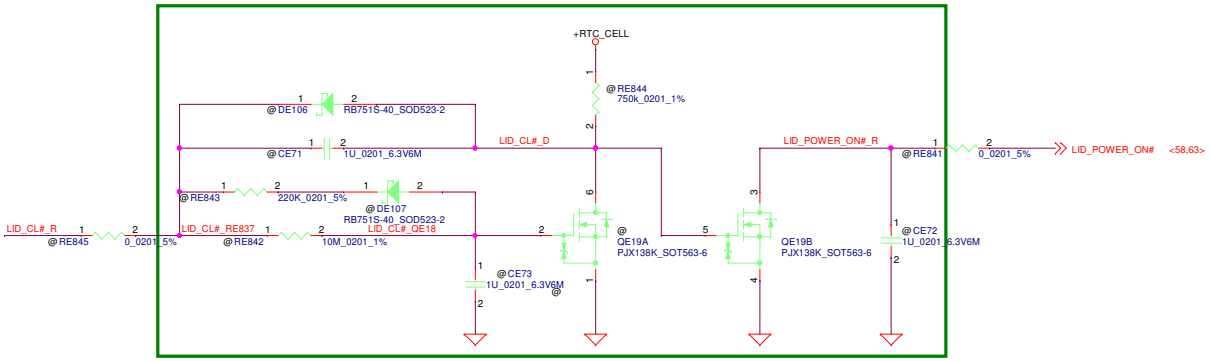
S5 LID OPEN POWER ON



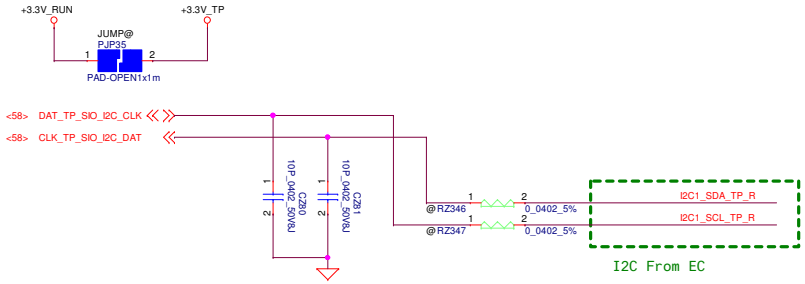
FUNCTION TABLE

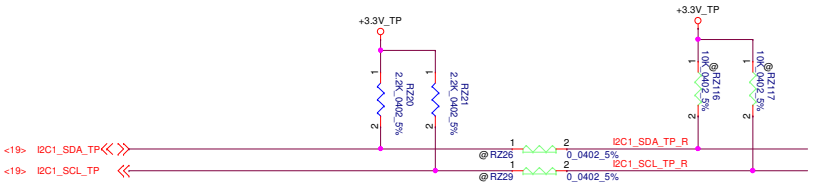
INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

S5 LID OPEN POWER ON(Other Solution)



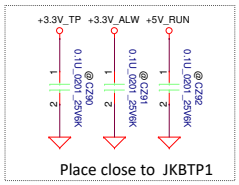
Touch Pad

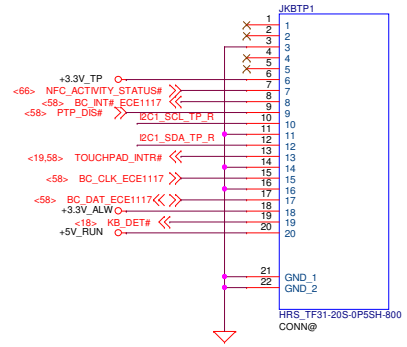




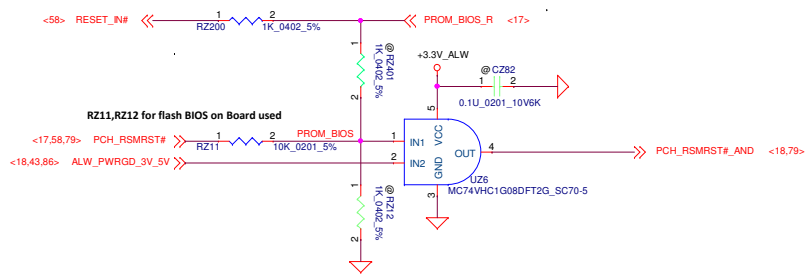
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

Keyboard





RSMRST circuit



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: KB/TP/ LID			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet: 63	of	104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: KB / TP / LED / LID		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 64 of 104	

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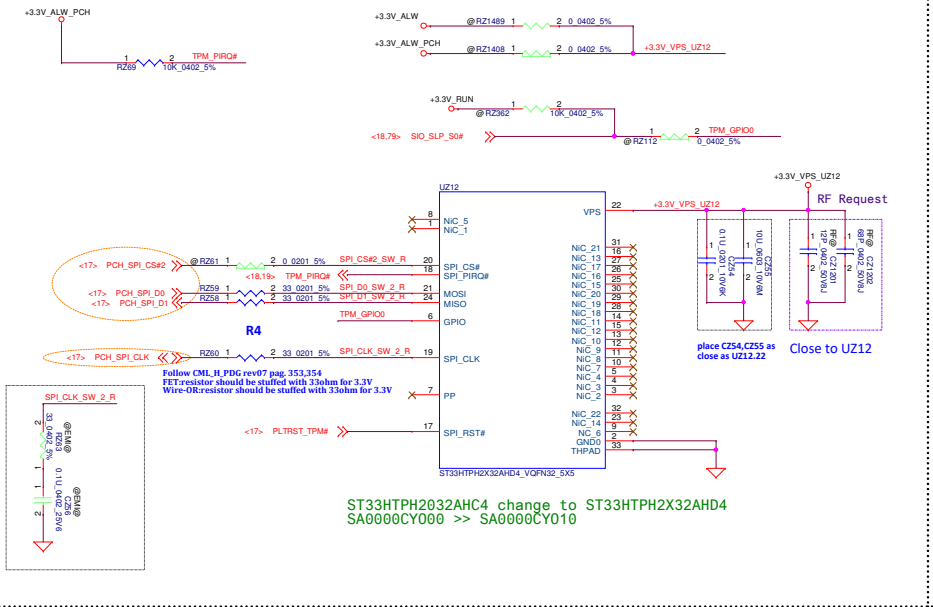
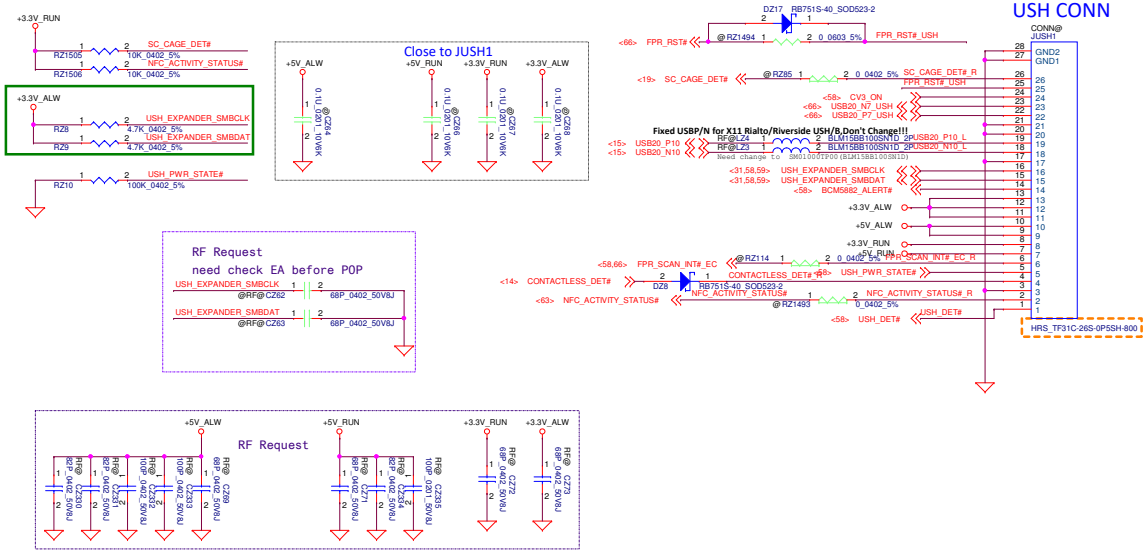
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

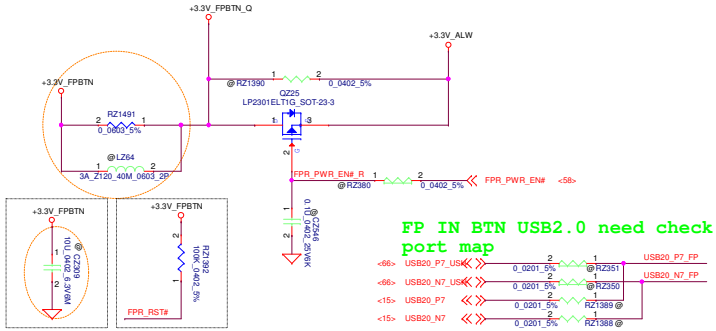
Compal Electronics, Inc.		
Title: HDD/ODD/FFS Conn		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 65 of 104	

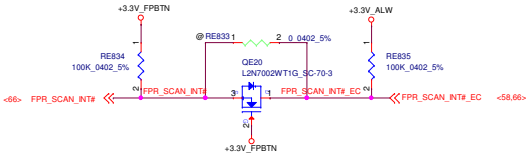
For ST TPM

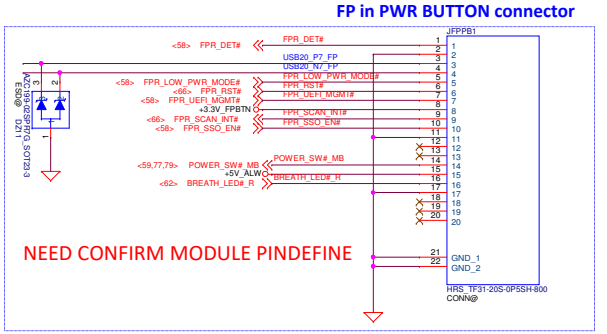


ST33HTPH2032AHC4 change to ST33HTPH2X32AHD4
SA0000CY000 >> SA0000CY010

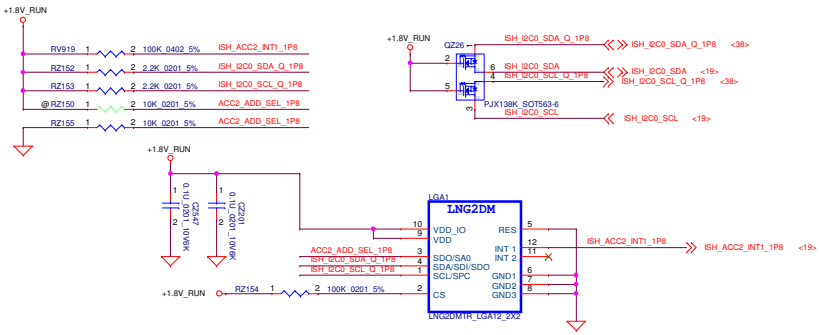








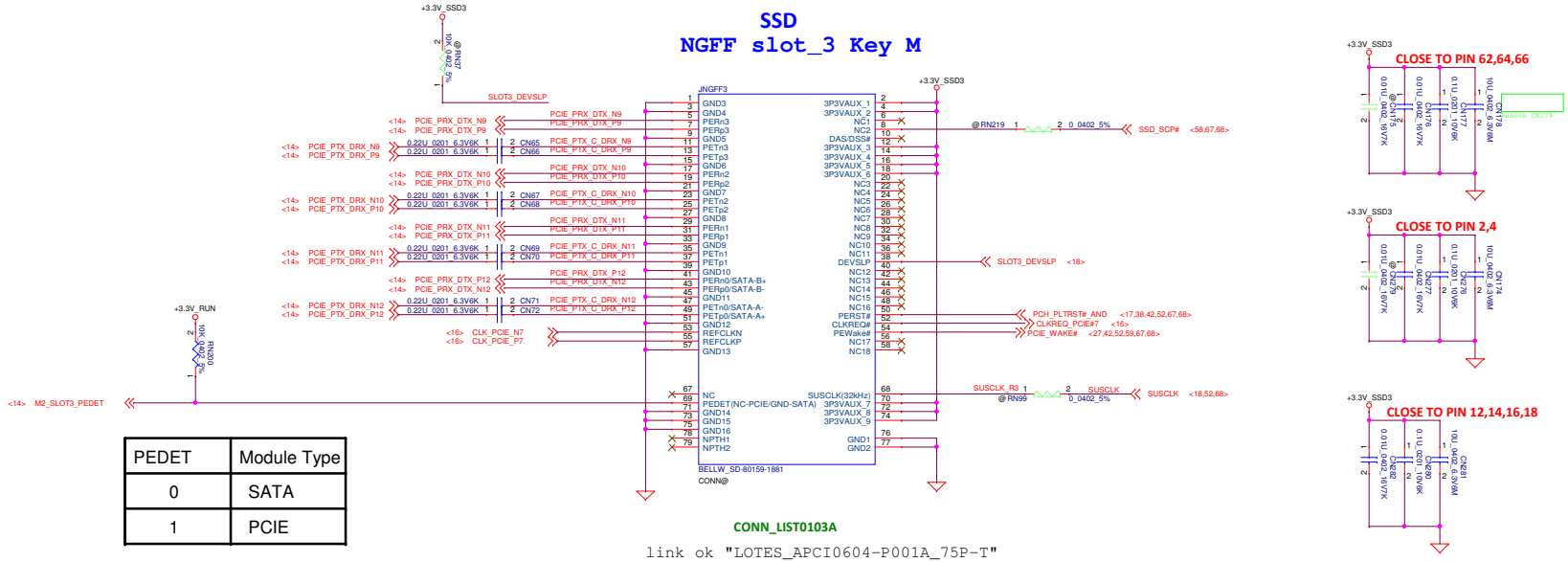
Accelerometer



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.	
Title	TPM/USH/FP/ACC
Size: Custom	Document Number: LA-J171P
Rev	1.0
Date:	Wednesday, August 26, 2020
Sheet	66 of 104

SSD
NGFF slot_3 Key M

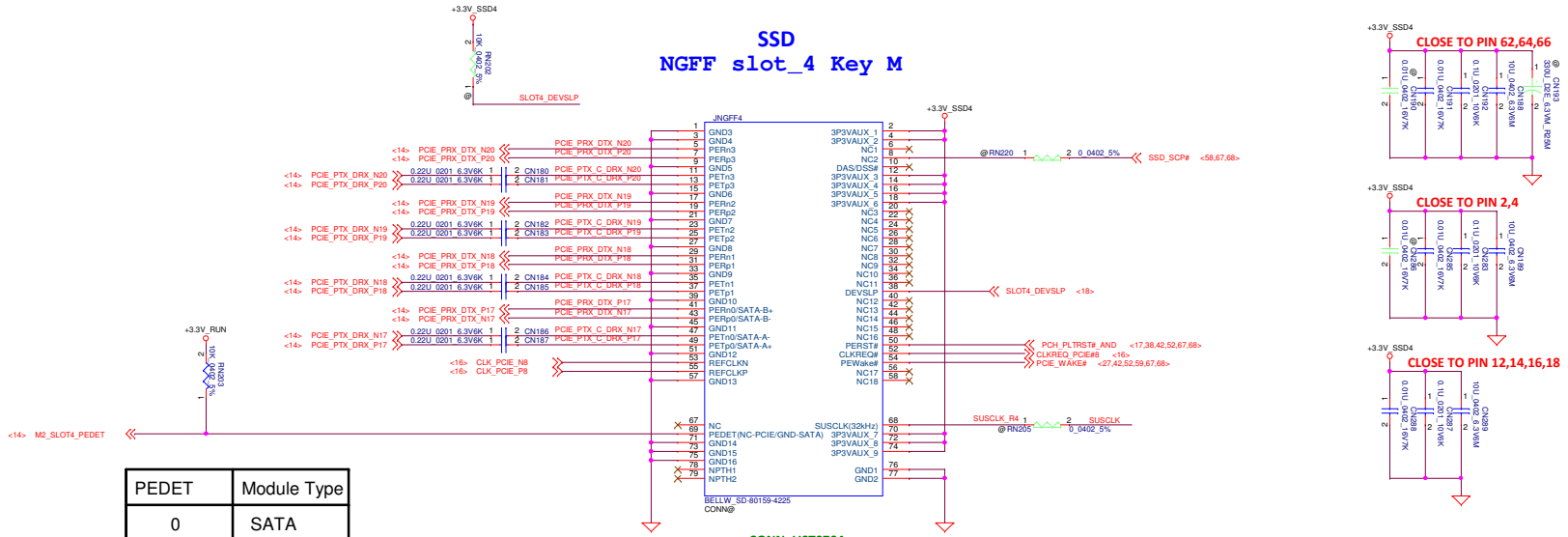


PEDET	Module Type
0	SATA
1	PCIE

CONN_LIST0103A

link ok "LOTES_APCI0604-P001A_75P-T"

SSD
NGFF slot_4 Key M



PEDET	Module Type
0	SATA
1	PCIE

CONN_LIST0704

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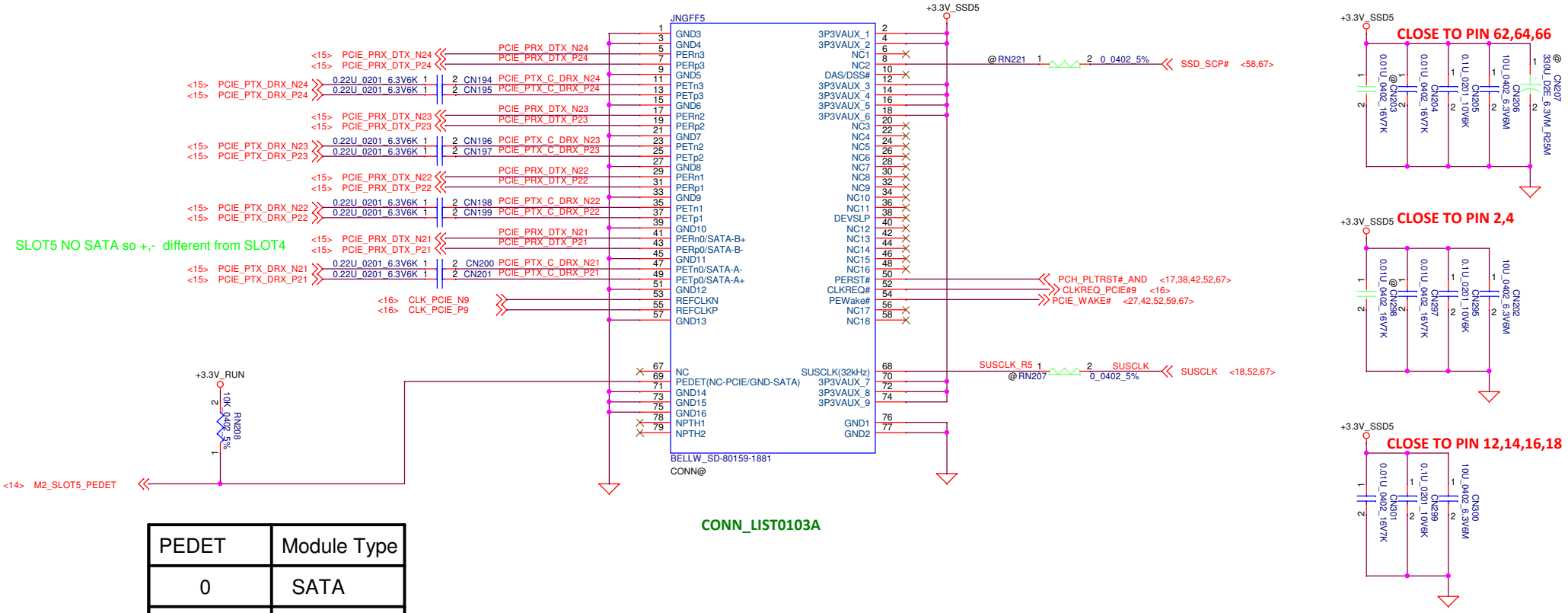
Compal Electronics, Inc.

Title: SSD SLOT3 / 4

Size: Custom | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 67 of 104

SSD
NGFF slot_5 Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

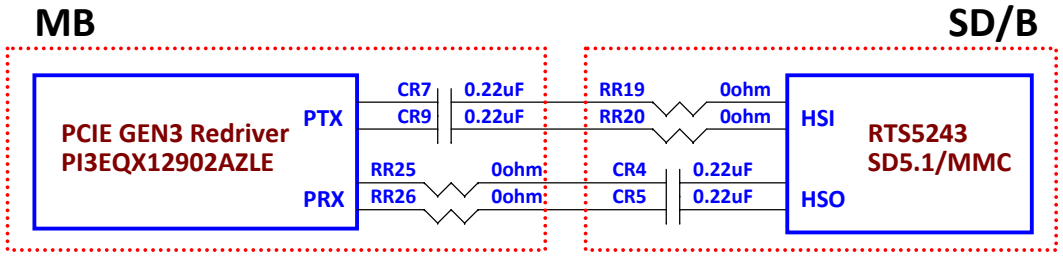
Title	SSD SLOT5	
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 68 of 104	

Reserve

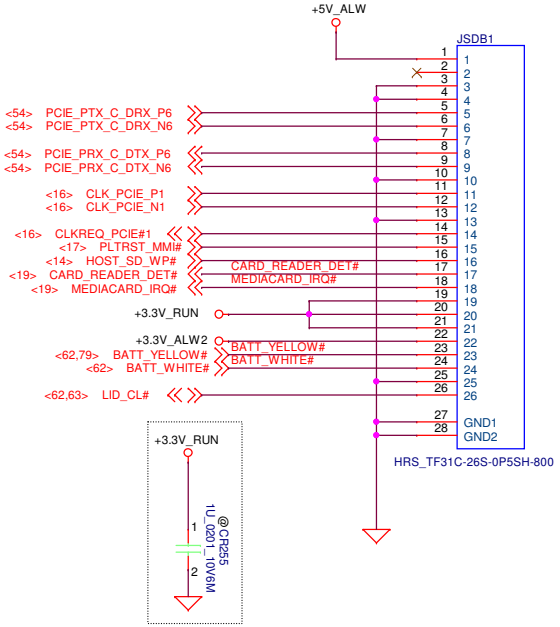
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: eMMC / UFS		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 69 of 104	

Card Reader PCIE Redriver Topology



To Card Reader & LED/B Conn

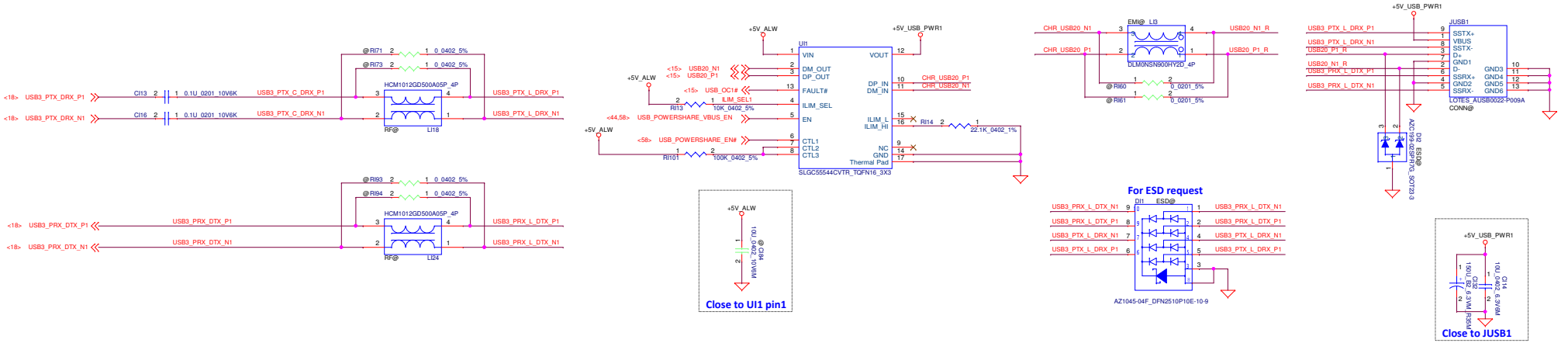


Place close to JSDB1 pin 19,20,21

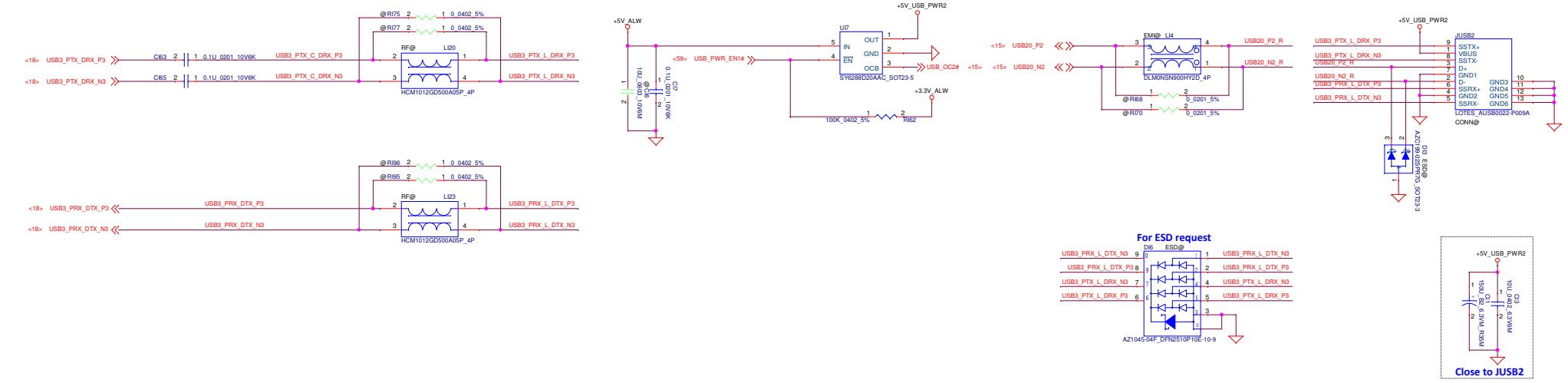
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: Card reader			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 70 of 104		

JUSB1



JUSB2



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: USB2/USB3 TYPEA

Size	Document Number	Rev
Custom	LA-J171P	1.0

Date: Wednesday, August 26, 2020 Sheet 71 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: *USB2/USB3 TYPEA*

Size: Custom | Document Number: *LA-J171P* | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 72 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: *USB2/USB3 DB*

Size: Custom | Document Number: *LA-J171P* | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 73 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: Dock		
Size: Custom	Document Number: LA-J171P	Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 74 of 104	

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: *USB*

Size: Custom | Document Number: *LA-J171P* | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 75 of 104

Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

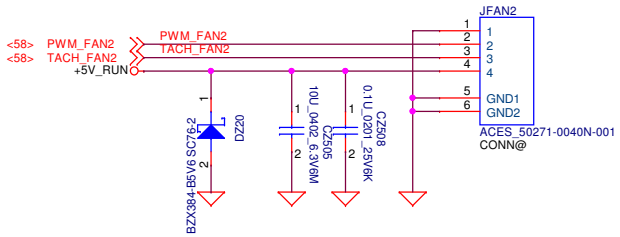
Compal Electronics, Inc.

Title: *USB*

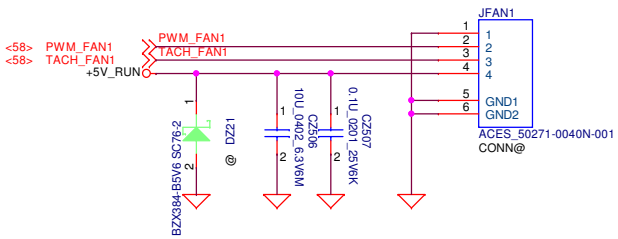
Size: Custom | Document Number: *LA-J171P* | Rev: 1.0

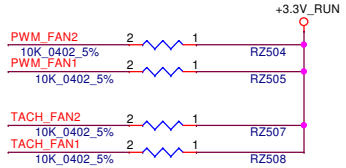
Date: Wednesday, August 26, 2020 | Sheet 76 of 104

DGFF FAN

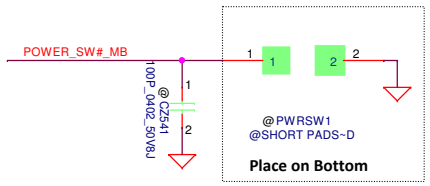


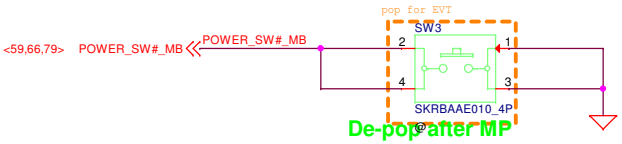
CPU FAN



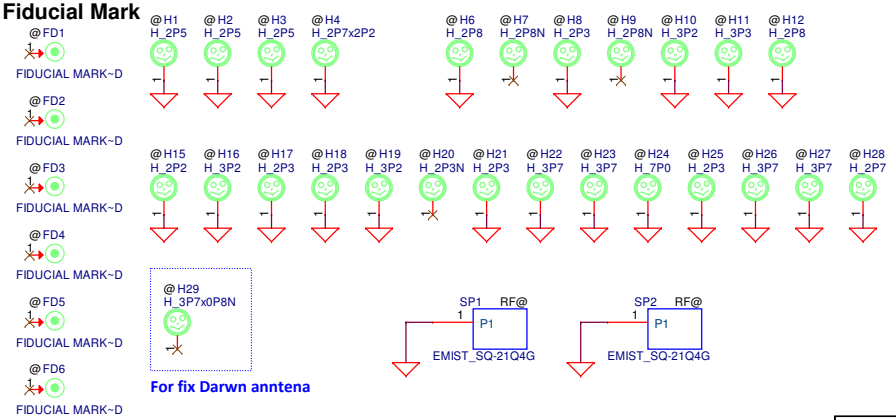


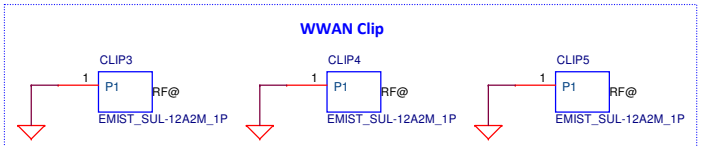
Power Switch for debug

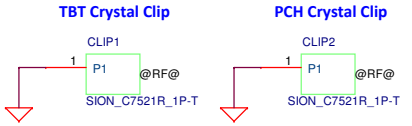




Fiducial Mark







Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1707-03

PCB 2V7 LA-J171P REV0 M/B 2 S

Part Number	Description
DAC00010000	PCB 2V7 LA-J171P REV0 M/B 2 S

Power CKT: 0108

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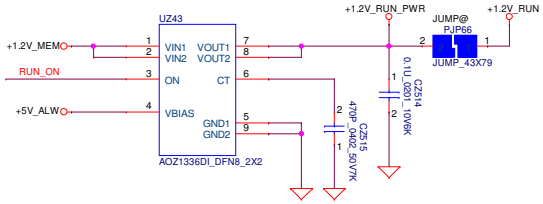
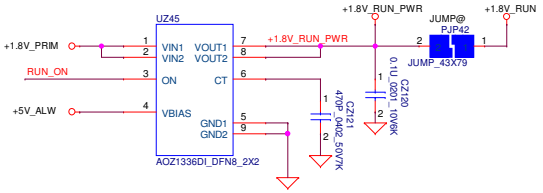
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: Cover			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 77 of 104		

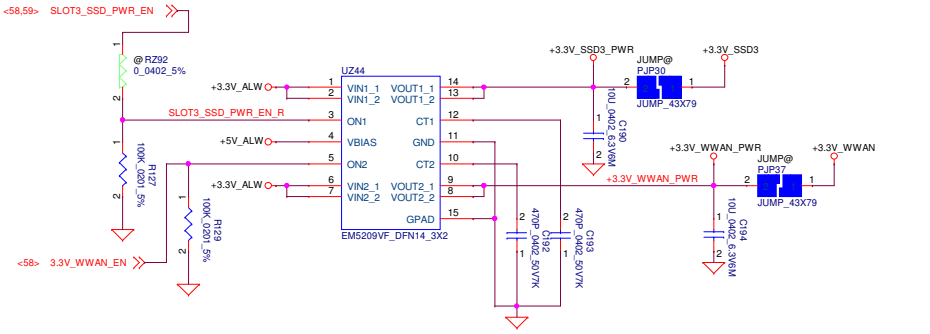
+1.2V_RUN Source



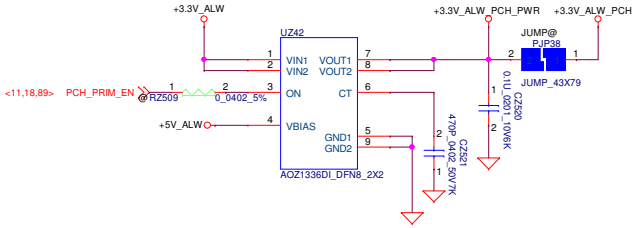
+1.8V_RUN Source



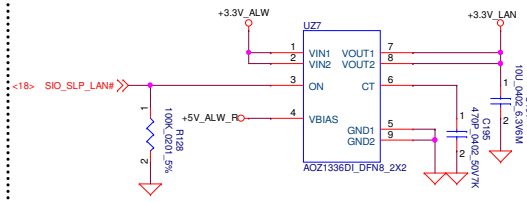
Power Control for M.2 SLOT3 &WWAN



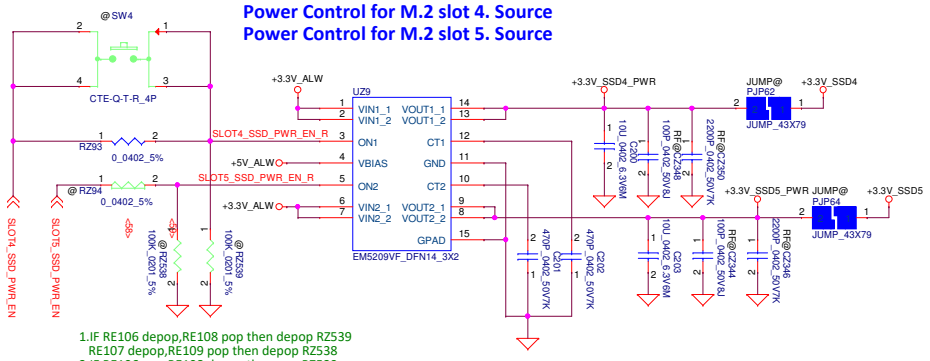
+3.3V_ALW_PCH Source



Power Control for LAN

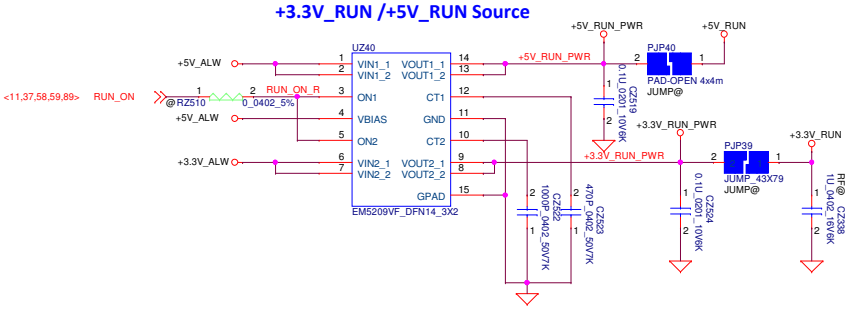


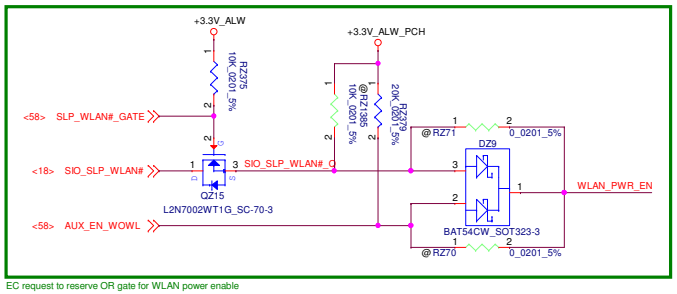
Power Control for M.2 slot 4. Source
Power Control for M.2 slot 5. Source



1.IF RE106 depop,RE108 pop then depop RZ539
RE107 depop,RE109 pop then depop RZ538
2.IF RE106 pop,RE108 depop then pop RZ539
RE107 pop,RE109 depop then pop RZ538

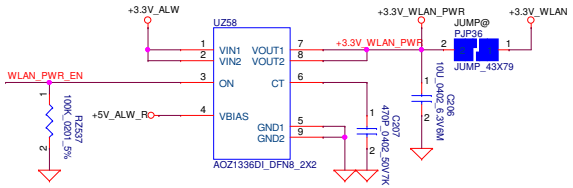
+3.3V_RUN /+5V_RUN Source



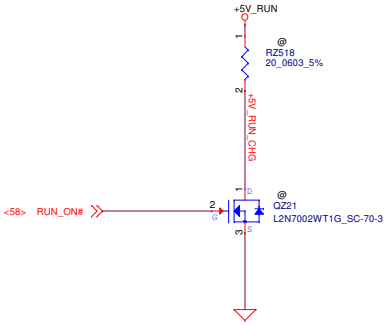


EC request to reserve OR gate for WLAN power enable

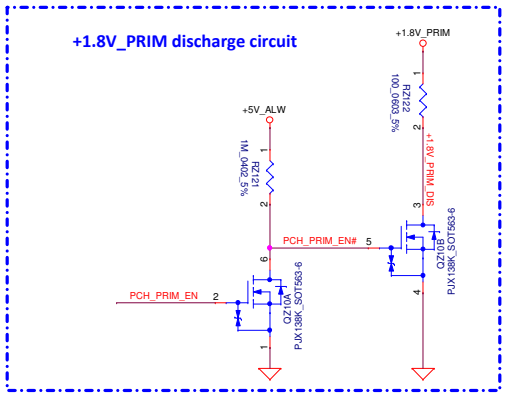
Power Control for WLAN



Discharge Circuit



+1.8V_PRIM discharge circuit



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: ***Power Control***

Size	Document Number	Rev
Custom	*LA-J171P*	1.0

Date: Wednesday, August 26, 2020 | Sheet 78 of 104

Check ME about wire to board PN

Intel Management Engine Test Suite

RP change to single Resistor

For BL_PWR_SRC & LCDVDD monitor

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

ME_FWP PCH has internal 20K PD.
(suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin2 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin1 & Pin2 short

M BIST

CPU XDP

Place near JXDP1

Place near JXDP1.41

Place near JXDP1.47

ESD request,Place near JXDP1 side.

ESD request,Place near JXDP1 side

RF Request

place as close as QV18

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: XDP/CMC/APS...debug

Size	Document Number	Rev
Custom	LA-J171P	1.0

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

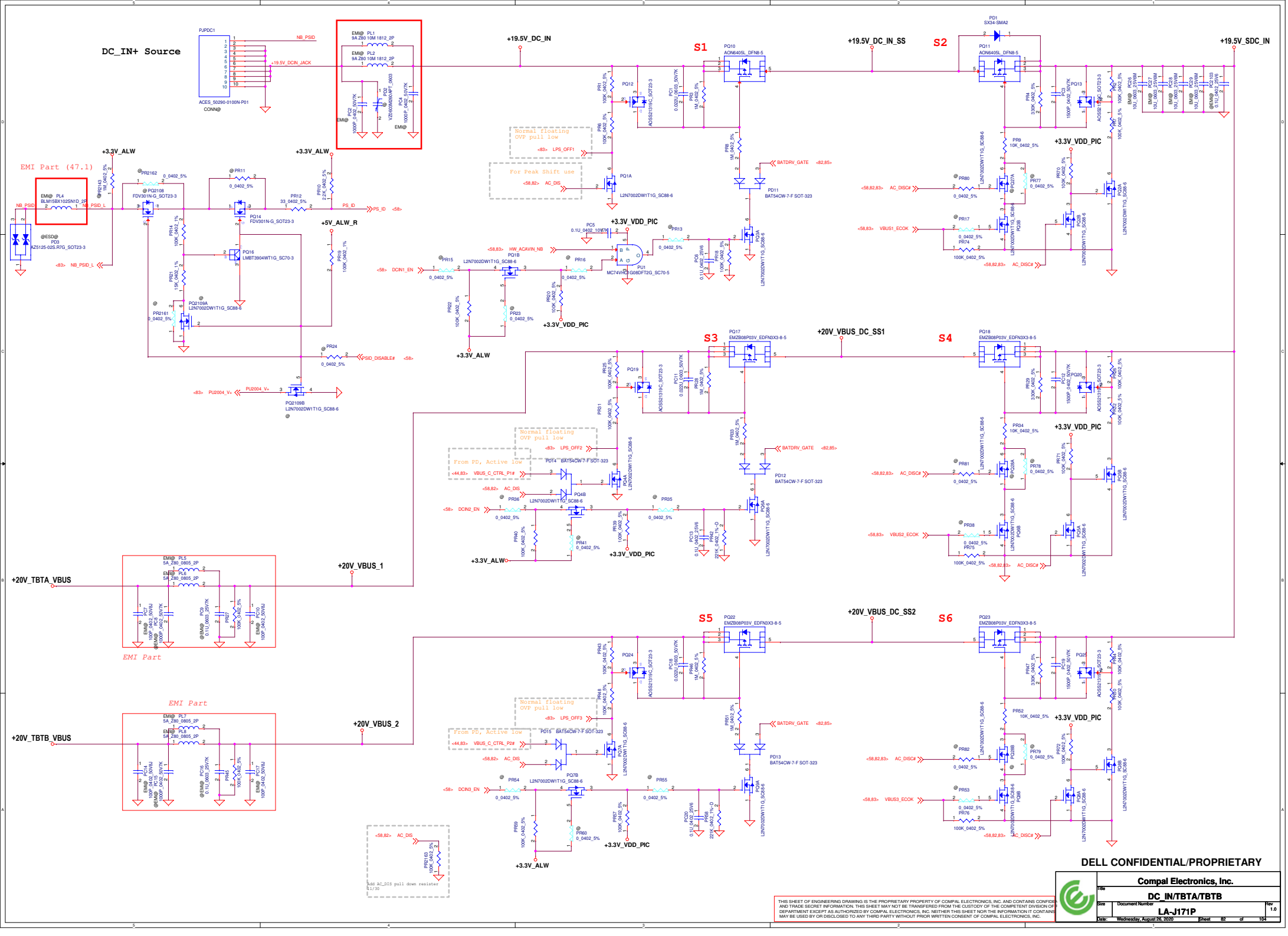
Compal Electronics, Inc.			
Title: Google Debug & INAs			
Size: Custom	Document Number: LA-J171P		Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 80 of 104		

Compal Electronics, Inc.

Title: Reserve

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 81 of 104


DC_IN+ Source
PJPDC1
ACES_50290-0100N-P01
CONN@
NB_PSID
+19.5V_DCIN_JACK
+19.5V_DC_IN
+19.5V_DC_IN_SS
+19.5V_SDC_IN
S1
S2
S3
S4
S5
S6
EMI Part (47.1)
+3.3V_ALW
+5V_ALW_R
+3.3V_VDD_PIC
+20V_VBUS_DC_SS1
+20V_VBUS_DC_SS2
+20V_TBTA_VBUS
+20V_TBTB_VBUS
+20V_VBUS_1
+20V_VBUS_2
EMI Part
Normal floating
OVP pull low
For Peak Shift use
From PD, Active low
PS_ID
PSID_DISABLE#
DCIN1_EN
DCIN2_EN
DCIN3_EN
HW_ACAVIN_NB
LPS_OFF1
LPS_OFF2
LPS_OFF3
AC_DIS
VBUS_C_CTRL_P1#
VBUS_C_CTRL_P2#
BATDRV_GATE
AC_DISC#
VBUS1_ECOK
VBUS2_ECOK
VBUS3_ECOK
Add AC_DIS pull down resister
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Compal Electronics, Inc.
DC_IN/TBTA/TBTB
LA-J171P
Wednesday, August 26, 2020
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AC_UVP_Protect
Barrel disconncet detect (co-lay unpop)

DCIN_AC_Detector

Vbus1_AC_Detector

Vbus2_AC_Detector

S3 OVP

S5 OVP

If Cypress is sure CC disconnect will detect disconnect within 700us, these comparators can be eliminated.

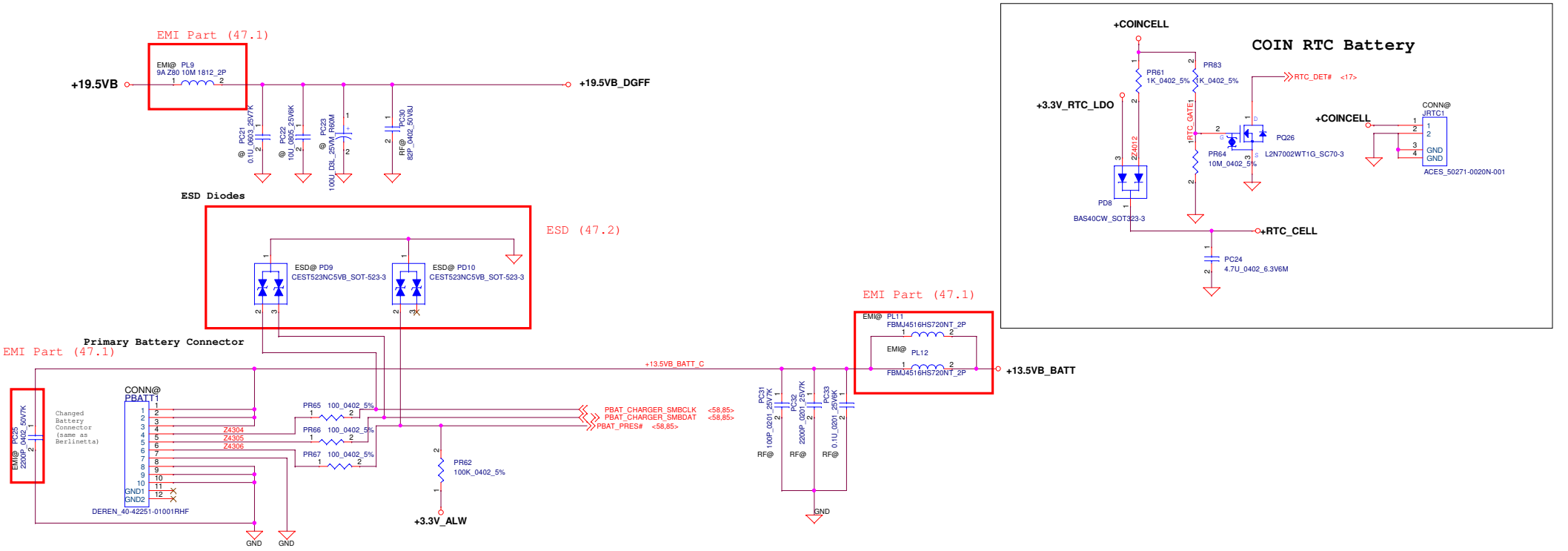
Fast swap(follow WH_MLK) :
PR3016 100K
PR3019 200K
PR3017 200K
PR3015 100K
PC3016 100P
PC3017 220P
PR2148 1M
PR3014 0
PR3018 221K
PC3018 1200P

UVP :
PR3016 100K
PR3019 82.5K
PR3017 237K
PR3015 84.5K
PR3016 100P
PC3017 220P
PR2148 1M(depop)
PR3014 0
PR3018 49.9K
PC3018 1200P
V+ :1.5V
V- :<1.5V when V<5.7V
latch V+ :1.87V
latch V- : 0.87V

OVP pull high to 3.3V_VDD_PIC because WH need to concern battery mode to latch LPS, and need to remove all source to reset LPS function

S3_OVP / S5_OVP setting
V- : 0.88V
V+ : >0.88V when VBUS >5.4V
latch V+ : 1.85V

Compal Electronics, Inc.	
Title: AC DET/LPS circuit	
Size:	Document Number: LA-J171P Rev: 1.0
Date: Wednesday, August 26, 2020	Sheet 83 of 104

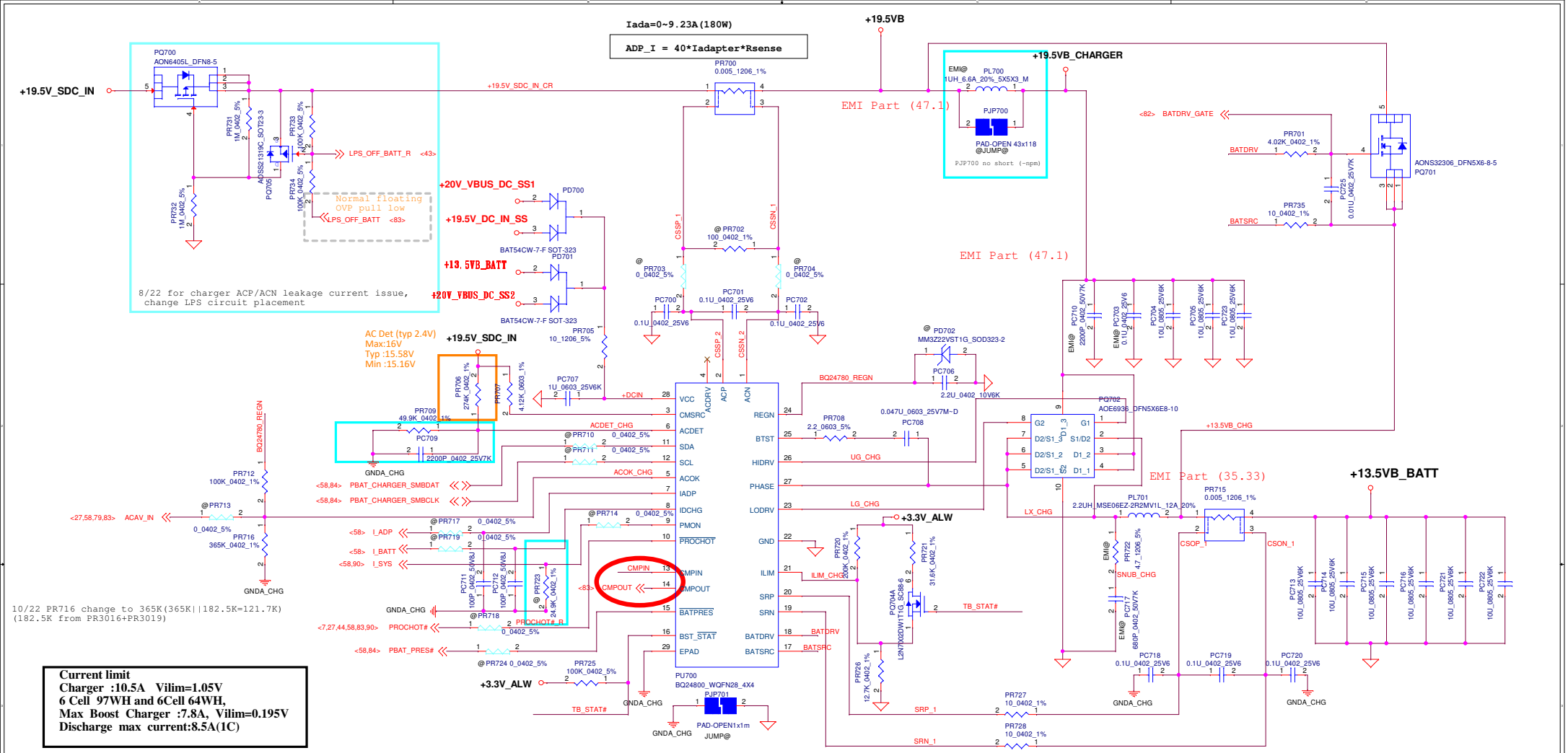


Compal Electronics, Inc.

Title: BATT/DGFF/RTC/5V_VBUS

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 84 of 104



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Compal Electronics, Inc.	
Title	Charger
Size	Document Number: LA-J171P
Rev	1.0
Date:	Wednesday, August 26, 2020
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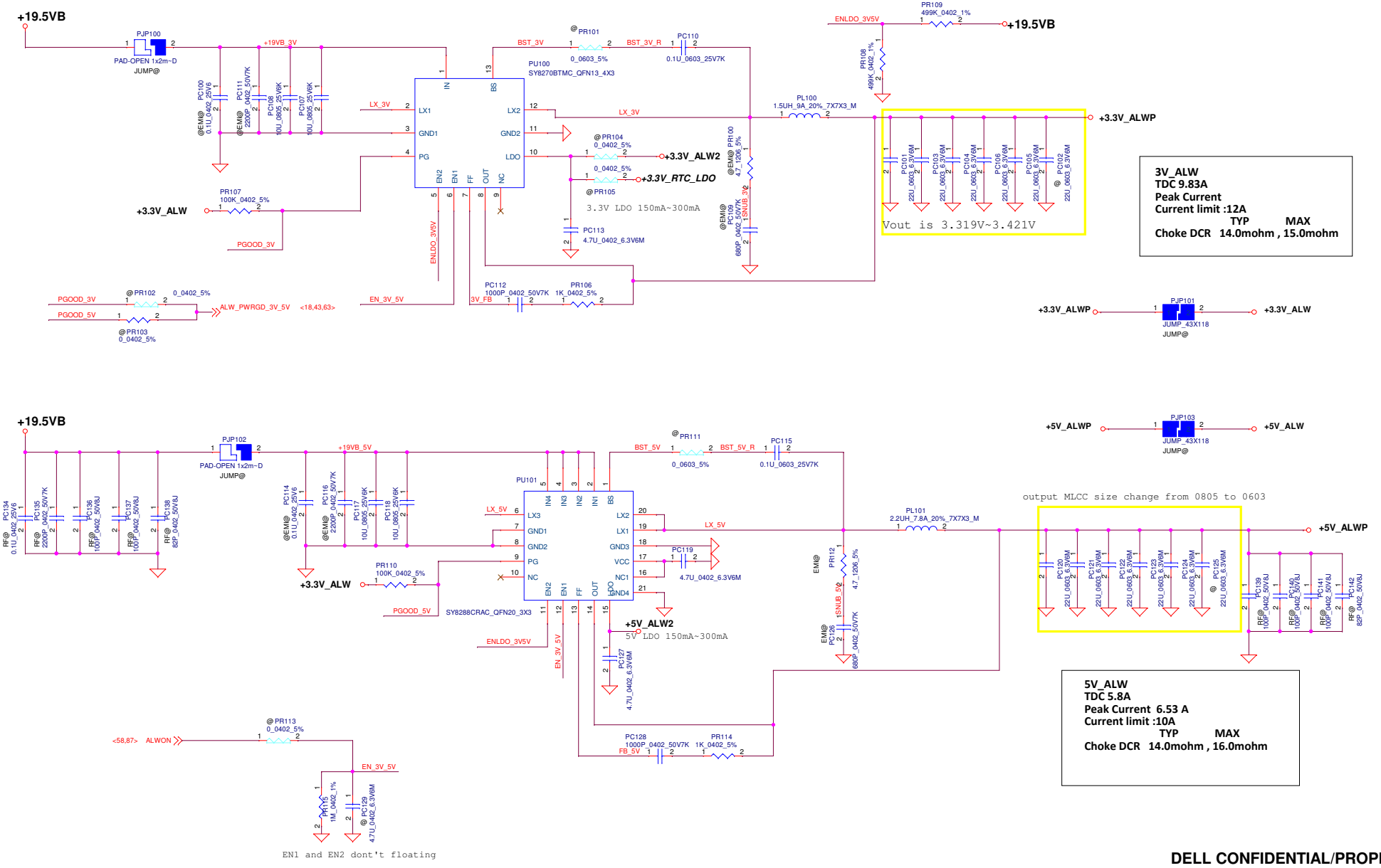

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Compal Electronics, Inc.	
Title	5V_ALW/3V_ALW
Size	Document Number: LA-J171P
Rev	1.0
Date:	Wednesday, August 26, 2020
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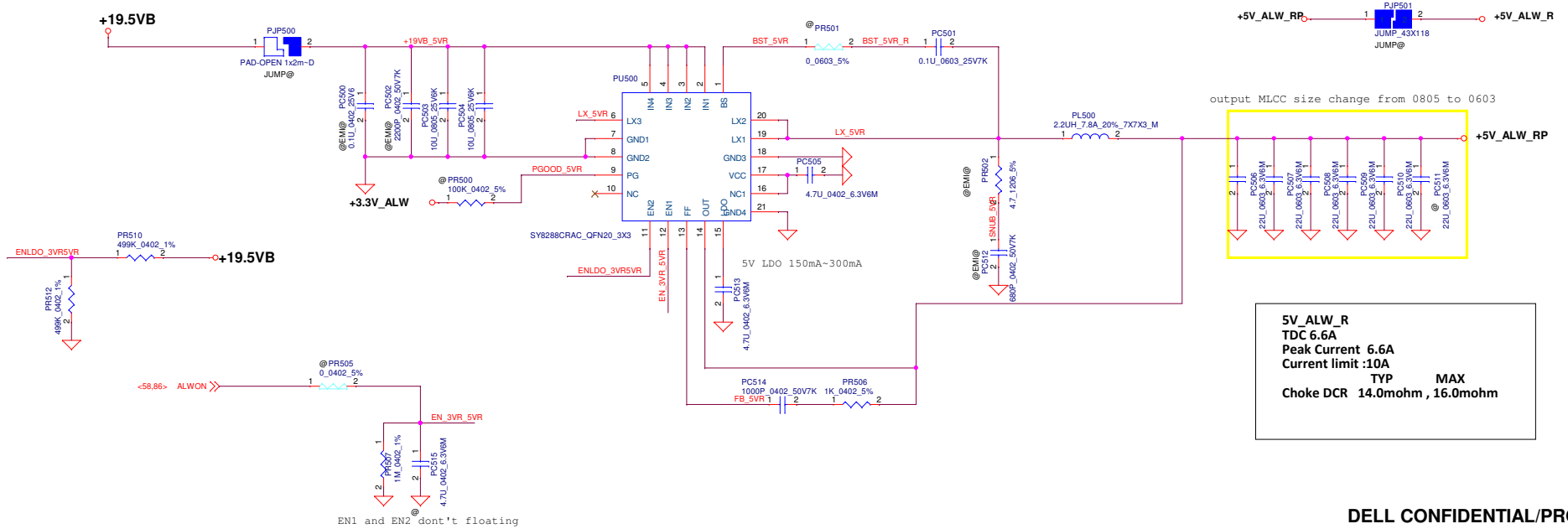

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Compal Electronics, Inc.	
Title	5V_ALW_R/3V_ALW_R
Size	Document Number: LA-J171P
Rev	1.0
Date:	Wednesday, August 26, 2020
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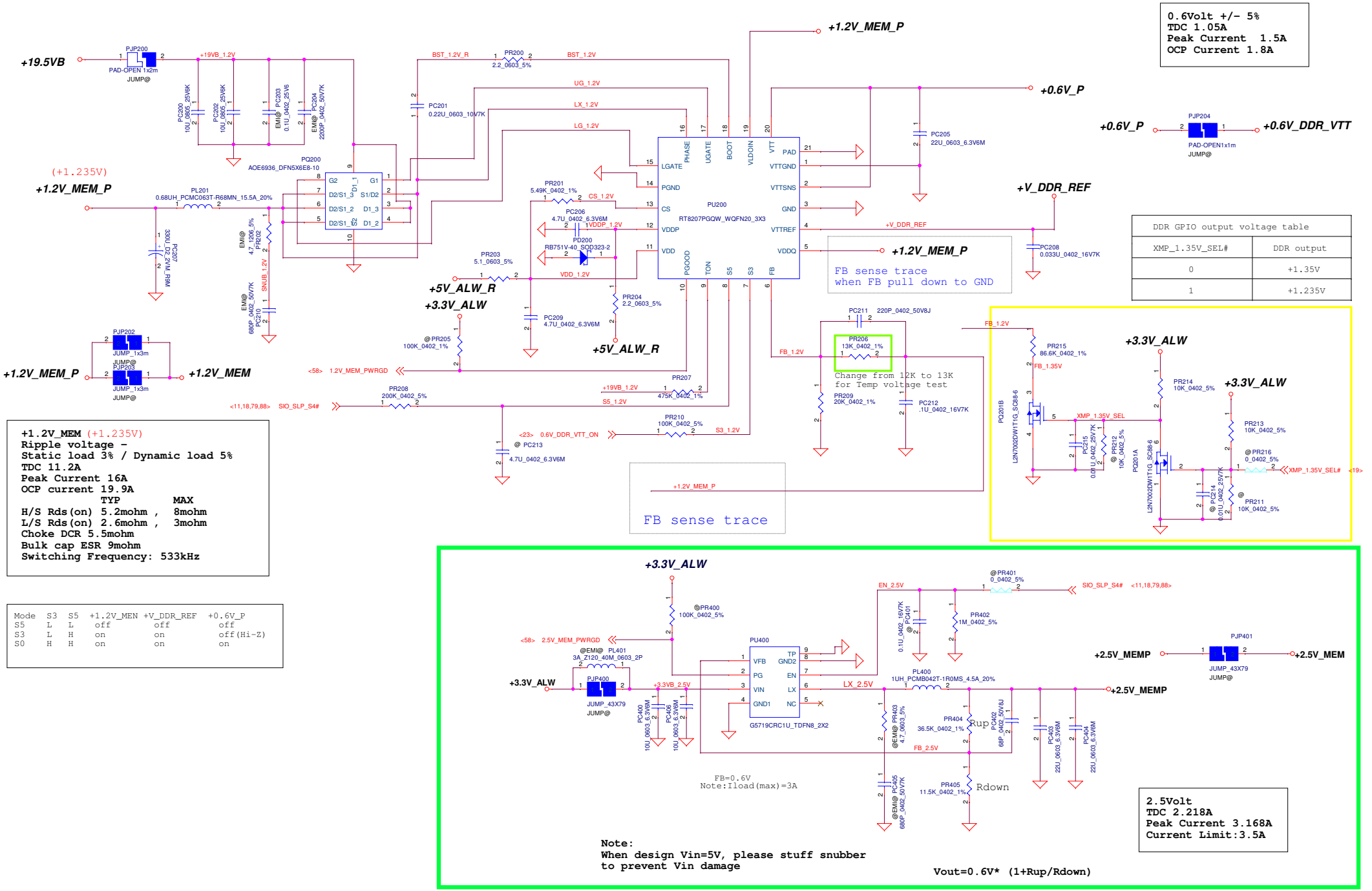

Compal Electronics, Inc.

Title: 1.2VP/0.6V/2.5V

Size: | Document Number: LA-J171P | Rev: 1.0

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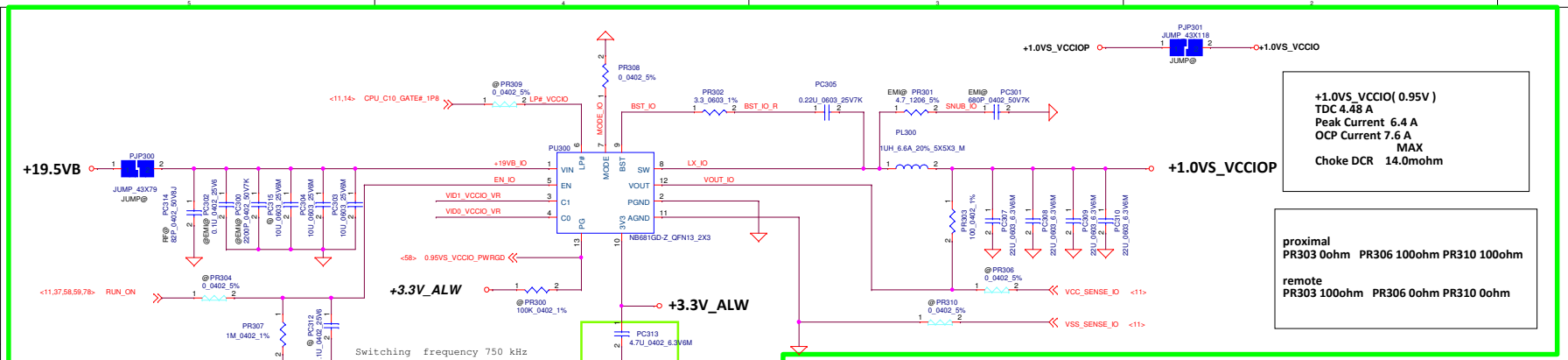

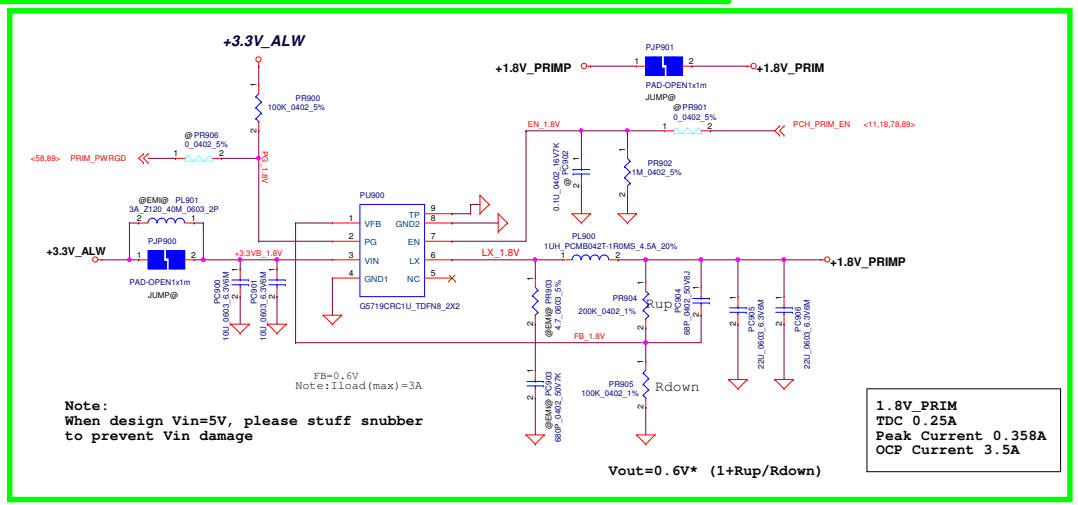

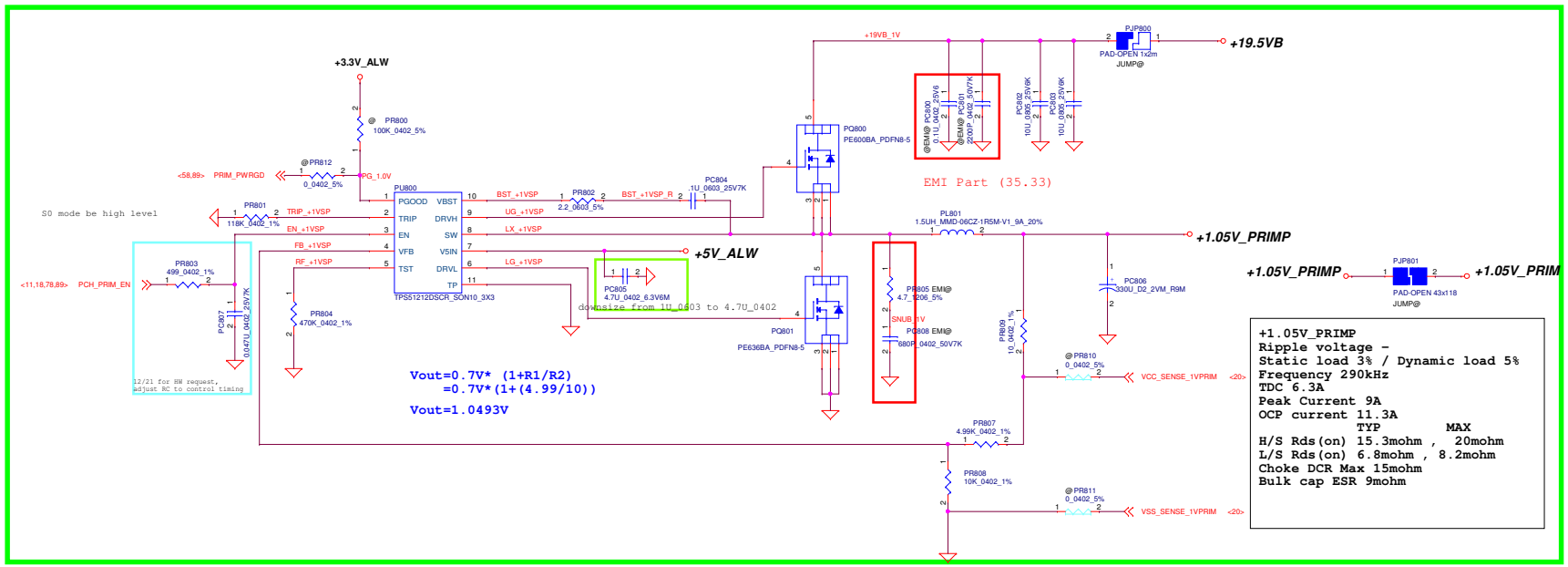

Compal Electronics, Inc.

Title: VCC_IO/1.8V/1.0VPRIM

Size: | Document Number: LA-J171P | Rev: 1.0

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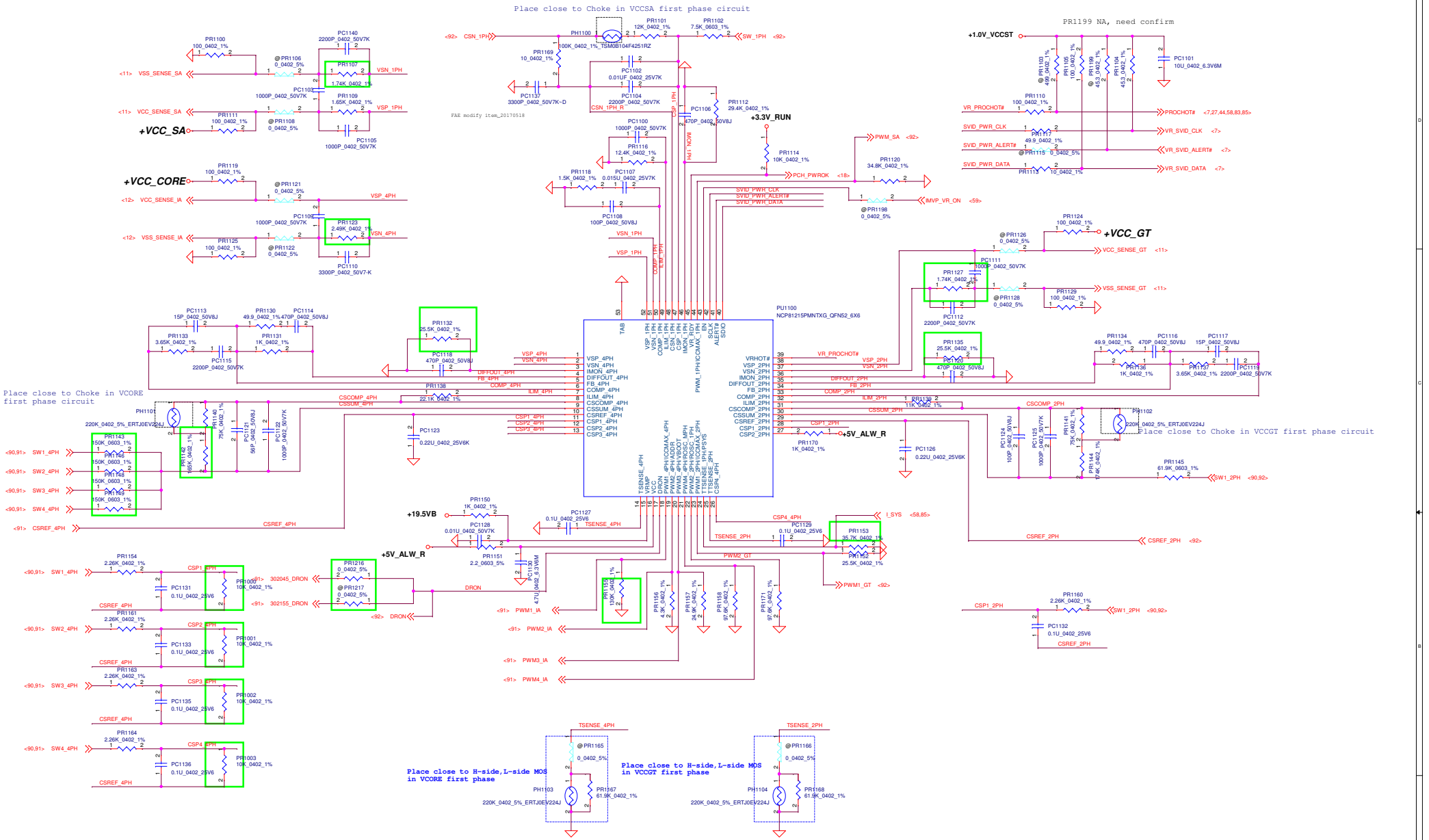
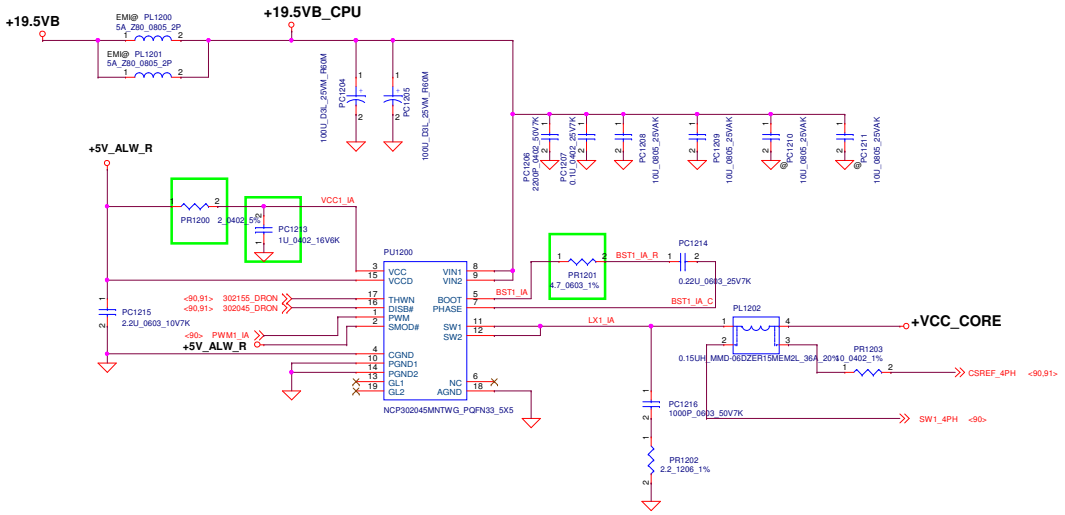
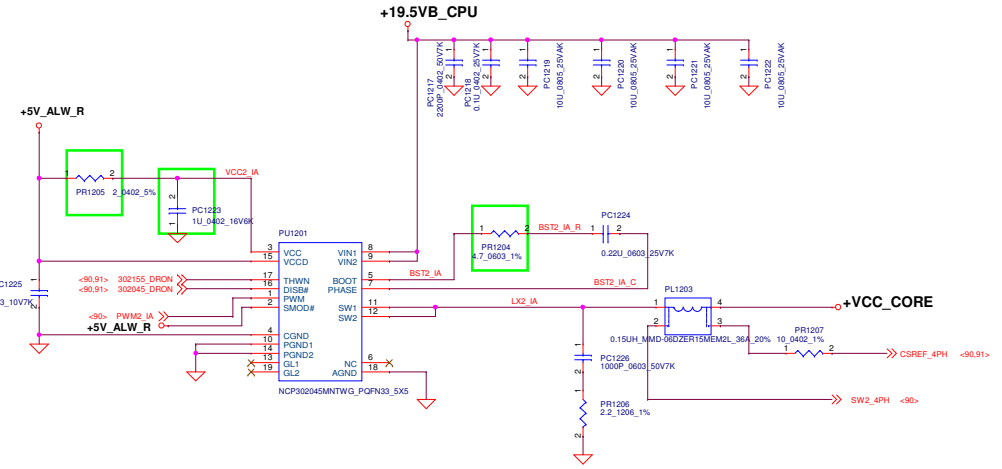
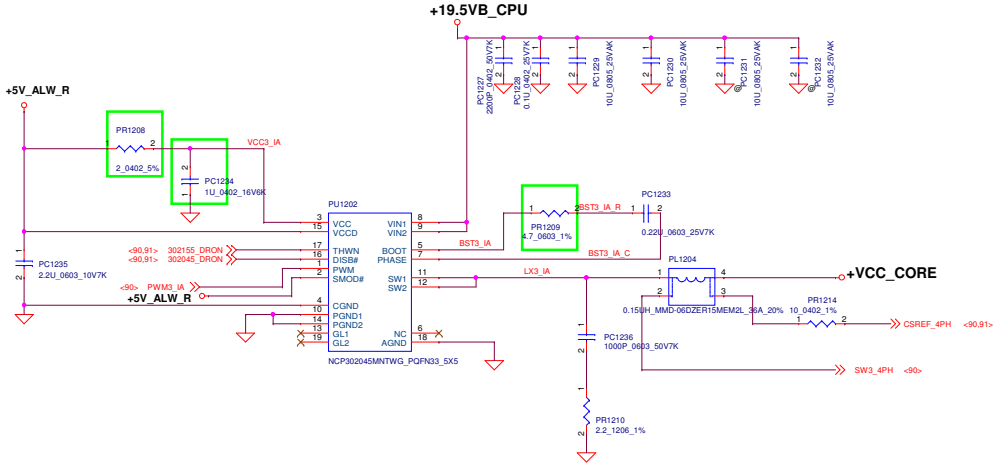

Place close to Choke in VCCSA first phase circuit
PR1199 NA, need confirm
+1.0V_VCCST
+VCC_SA
+VCC_CORE
+VCC_GT
+3.3V_RUN
+5V_ALW_R
+19.5VB
PU1100
NCP81215PMNTXG_QFN52_6X6
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
FAE modify item_20170518
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
VCORE controller
LA-J171P
Wednesday, August 26, 2020
VX wxdn168888

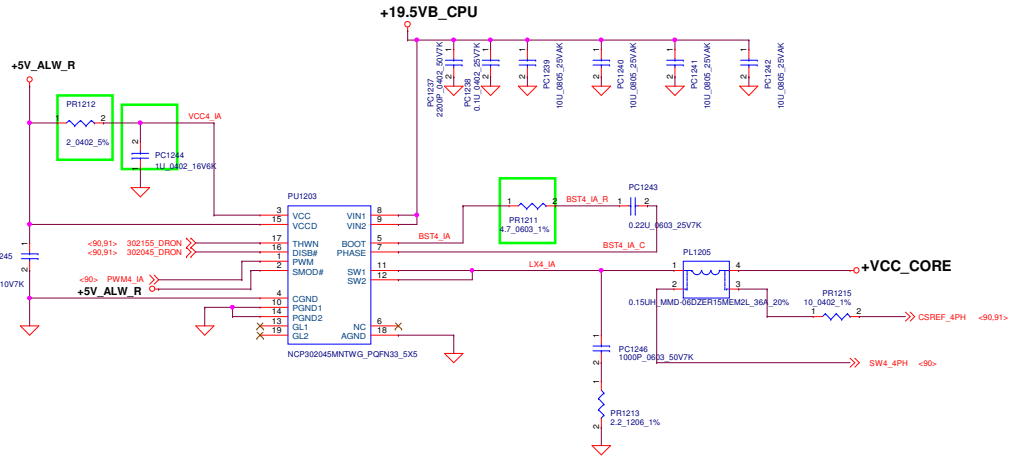
PC1221/PC1222/PC1241/PC1242
Put at MOS backside

PC1210/PC1211/PC1231/PC1232
Depop









Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	+VCC_CORE		
Size	Document Number		Rev
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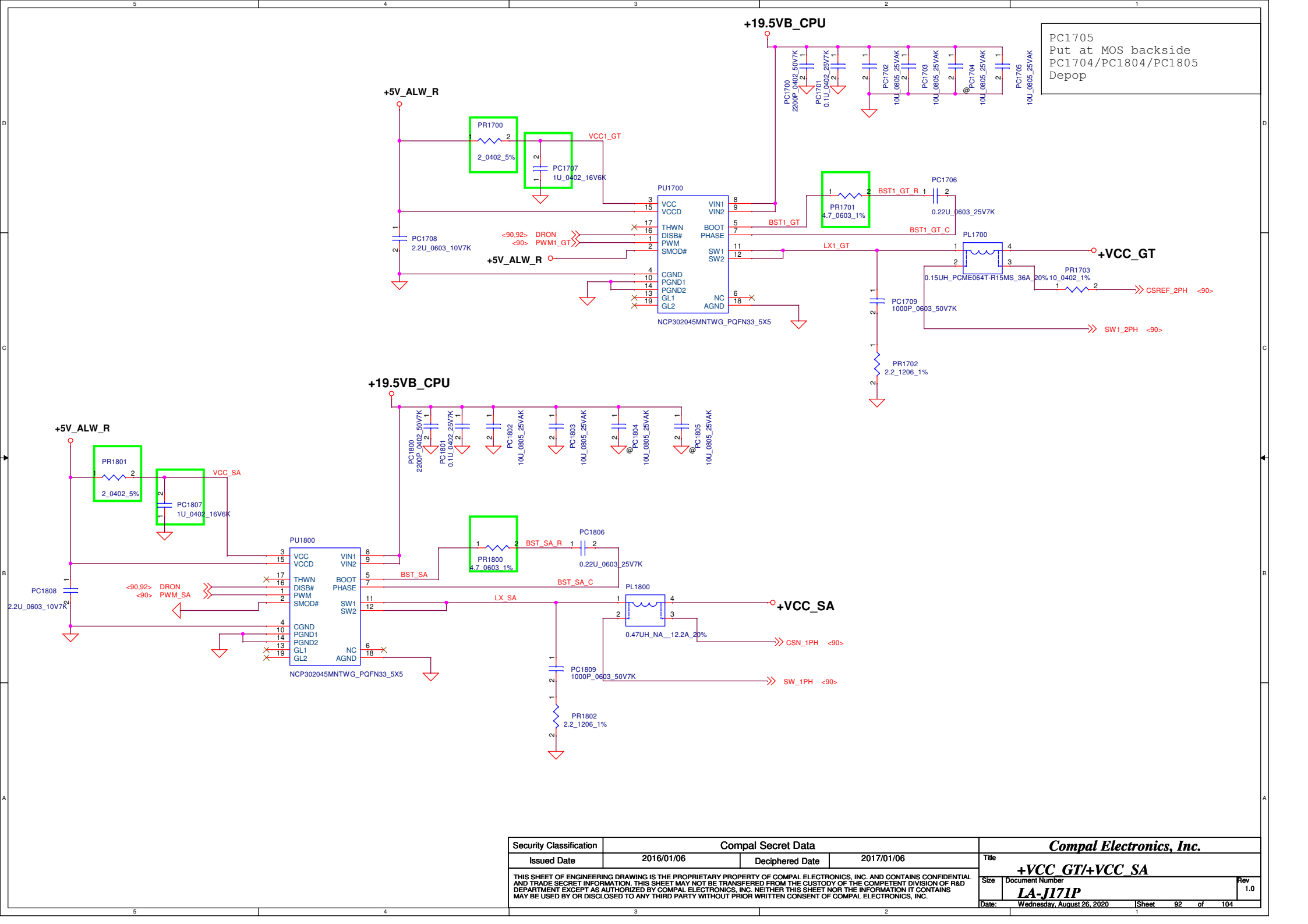

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: **+VCC_GT/+VCC_SA**

Size | Document Number: **LA-J171P** | Rev: 1.0

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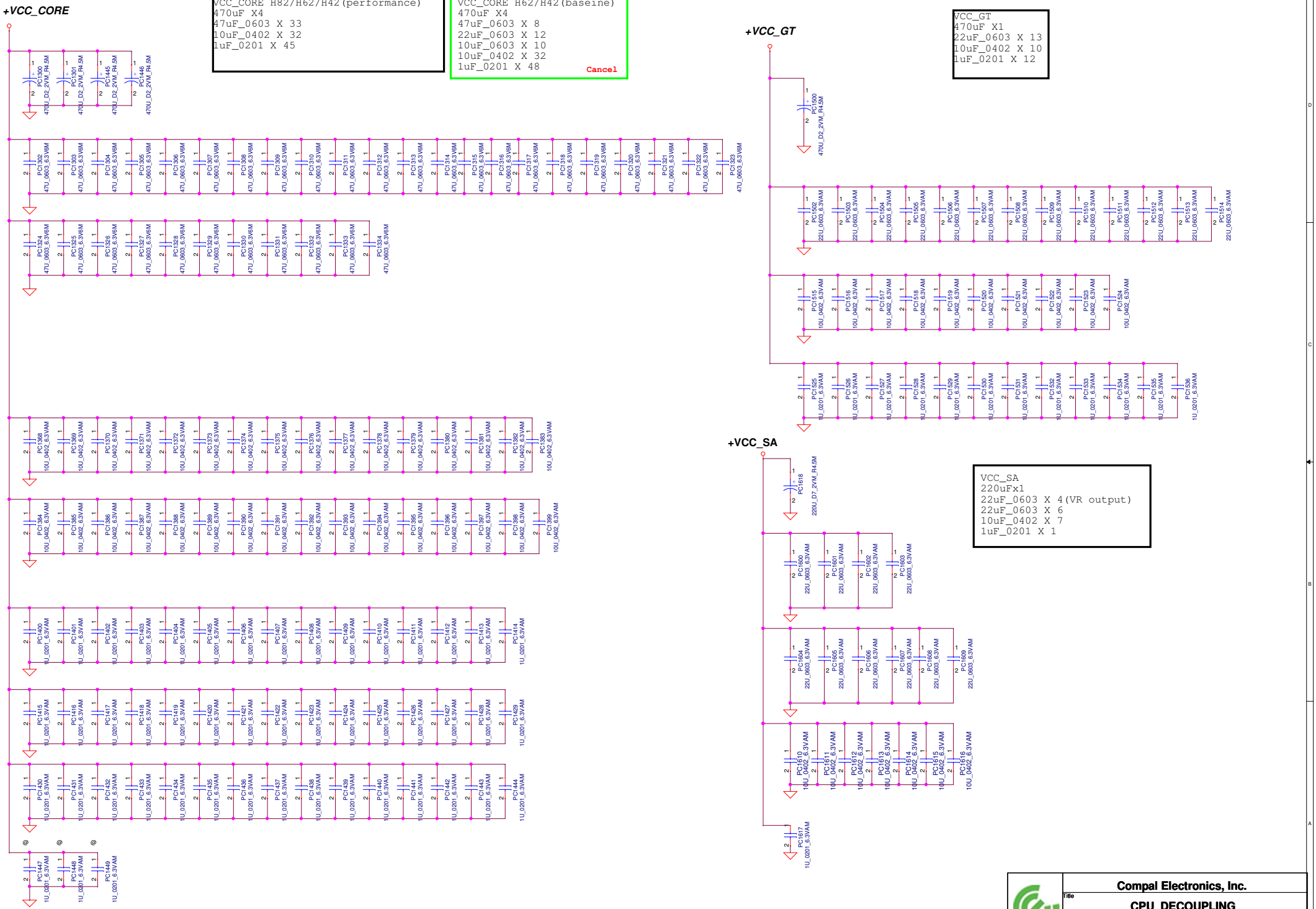
+VCC_CORE
VCC_CORE H82/H62/H42(performance)
470uF X4
47uF_0603 X 33
10uF_0402 X 32
1uF_0201 X 45
VCC_CORE H62/H42(baseine)
470uF X4
47uF_0603 X 8
22uF_0603 X 12
10uF_0603 X 10
10uF_0402 X 32
1uF_0201 X 48
Cancel
+VCC_GT
VCC_GT
470uF X1
22uF_0603 X 13
10uF_0402 X 10
1uF_0201 X 12
+VCC_SA
VCC_SA
220uFx1
22uF_0603 X 4(VR output)
22uF_0603 X 6
10uF_0402 X 7
1uF_0201 X 1
Compal Electronics, Inc.
CPU_DECOUPLING
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	Compal Electronics, Inc.	
	Title: Reserve	
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Compal Electronics, Inc.

Title: Reserve

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Date: Wednesday, August 26, 2020 | Sheet 95 of 104

Compal Electronics, Inc.

Title: Reserve

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 96 of 104

Compal Electronics, Inc.

Title: Reserve

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 97 of 104

Compal Electronics, Inc.

Title: Reserve

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 98 of 104

Compal Electronics, Inc.

Title: Reserve

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Date: Wednesday, August 26, 2020 | Sheet 99 of 104

Compal Electronics, Inc.

Title: Reserve

Size | Document Number: LA-J171P | Rev: 1.0

Date: Wednesday, August 26, 2020 | Sheet 100 of 104

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	88	POWER	9/19	COMPAL	For XMP3600, need use 1.35V_ DDR to support this function	add voltage switch circuit PR211~PR216/PC214~PC215/PQ201	0.2(X01)
2	93	POWER	9/19	COMPAL	H62/H42 CPU decoupling reduce for intel SPEC, reserve 0201 MLCC	add PC1447/PC1448/PC1449	0.2(X01)
3	84	POWER	9/25	COMPAL	For RTC detect issue ,change circuit	change circuit and PR64/PR83 change to 1M	0.2(X01)
4	84	POWER	10/7	COMPAL	For RF request , add MLCC on battery input side	add PC31/PC32/PC33	0.2(X01)
5	86	POWER	10/7	COMPAL	For RF request , add MLCC on 5V input side and output side	add PC134/PC135/PC136/PC137/PC138 on input PC139/PC140/PC141/PC142 on output	0.2(X01)
6	90	POWER	10/7	COMPAL	Follow Load line test, change VR IC parameter for FAE suggestion	Change PR1107/PR1127 to 1.74K PR1132/PR1135 to 25.5K PR1123 to 2.49K,PR1142 to 165K	0.2(X01)
7	85	POWER	10/22	COMPAL	charger IC change to new IC for ARD define part	Change PU700 from SA00008OM00 to SA0000D7R10	0.2(X01)
8	83	POWER	10/22	COMPAL	RTC detect circuit change resister for meeting with TDC	Change PR83 to 1K , PR64 to 10M	0.2(X01)
9	85	POWER	11/27	COMPAL	For MODS , need to reduce 3.3V power consumption	Change PR720 to 200K from 20K PR721 to 31.6K from 3.16K PR725 to 100K from 10K PR726 to 12.7K from 1.27K	0.3(X01)
10	82	POWER	11/27	COMPAL	For MODS , need to reduce 3.3V power consumption	Change PR19 to 100K from 10K	0.3(X01)
11	89	POWER	11/27	COMPAL	For DIDT requet , change source to meet HBM >500	Change PQ800 to SB000010S00 from SB00000H800 PQ801 to SB000016F00 from SB000010U00	0.3(X01)
12	84	POWER	11/27	COMPAL	Align with EMI , change Bead to H=1.1	Change from SM010006680 to SM010009C80	0.3(X01)
13	83	POWER	11/27	COMPAL	For UVP Improve , add circuit to aviod turn on MOS after system short to GND	add PQ2113 PD3004/PD3005/PD3006 PR3027/PR3028/PR3029/PR3030/PR3031/PR3032	0.3(X01)
14	85	POWER	11/29	COMPAL	For EMI team request , add ISN choke on charger input side	remove Bead PL700/PL702 SM01000U600 add ISN choke PL700 SH00000Z200	0.3(X01)
15	90	POWER	1/14	COMPAL	For Psys setting , adjust resister to meet Psys voltage	change PR1153 from 17.8K to 35.7K	0.4(X02)
16	83	POWER	2/14	COMPAL	1.To reduce leakage current on S5 DC mode,adjust resister value 2. To fix OVP issue with IOGEAR, adjust parameter to increase delay time	1. PR3017 from 237K to 1M PR3015 from 84.5K to 332K 2. PR2047/PR2051 from 287K to 499K PR2059/PR2060 from 82.5Kto 97.6k PR2048/PR2050 from 137K to 115K PR2061/PR2062 from 84.5 to 42.2K PC2021/PC2025 from 2.2uF to 10uF	0.4(X02)

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1	58	HW	2019/08/22	Compal	Support EC inform PCH ROM TOP SWAP function	Add RE847 between UH1.AW29 and UE1.M8.	0.2(X01)
2	52	HW	2019/08/22	DELL	BT_RADIO_DIS#_R change to PCH control from EC	Pop RZ301,depop RZ300	0.2(X01)
3	43	HW	2019/08/22	INTEL	Vender review feedback	Depop RT554	0.2(X01)
4	16	HW	2019/08/22	Compal	Align NB_MLK PCIE_CLKREQ# PU change to 20Kohm for reduce power consumption	RH123,RH124,RH126,RH127,RH128,RH129,RH130,RH131,RH132,RH133,RH134 change to 20Kohm(SD043200280) from 10Kohm(SD043100280)	0.2(X01)
5	56	HW	2019/08/22	Compal	Align NB_MLK RA18 change to 100Kohm for power consumption	RA18 change to 100Kohm(SD043100380)from 10Kohm(SD043100280)	0.2(X01)
6	62	HW	2019/08/22	factory	Connector location reduce to under 6 character	JSDLED1 change to JSDB1	0.2(X01)
7	71	HW	2019/08/26	Compal	Layout routing	Add RI101	0.2(X01)
8	51	HW	2019/08/28	Compal	LAN Crystal down size	Add RL86,change location Y1 to YL1.change YL1 to SJ10000UH00(1206 size) from SJ10000E910(3225 size)	0.2(X01)
9	71	HW	2019/08/29	Compal	Stable voltage rolling for USB charger	Add CI84 to UI1 pin1.	0.2(X01)
10	59,62	Buyers	2019/09/04	Compal	buyers cost plan	DE104,DE106,DE107,DZ12 change to SCS00006300 from SC100000S00.	0.2(X01)
11	42	HW	2019/09/16	Compal	CRB"TR_DP_TI83_HOST_REF_DESIGN_R2V0"	Change @RT592 PU to +3.3V_TBT_S0	0.2(X01)
12	17	HW	2019/09/16	Compal	PDG0.91 page 171	Pop RH640	0.2(X01)
13	79	HW	2019/09/16	Compal	Incomplete replacement	Change DV11,DV12 to SCS00006300 from SCS00003700	0.2(X01)
14	52	HW	2019/09/20	Compal	BT_RADIO_DIS# control by EC & PCH	Change DZ2 connect between BT_RADIO_DIS# and PCH_BT_RADIO_DIS#,pop RZ300,add reserve RZ302,remove RZ301,rename JNGFF1 pin54 to BT_RADIO_DIS#.	0.2(X01)
15	58	HW	2019/09/20	Compal	WLAN module's EC_BT_RADIO_DIS# has internal PU	Depop RE11	0.2(X01)
16	44	HW	2019/09/20	Compal	Adjust TYPE-C PWR switch ILIM(A)	Change RT585,RT587 to 7.68Kohm from 56Kohm, RT586,RT588 to 7.68Kohm from 64.9Kohm	0.2(X01)
17	58	HW	2019/09/20	Compal	Change EC CPN	Change UE1 to SA0000CQ730 from SA0000CQ720	0.2(X01)
18	19,38	HW	2019/09/20	Compal	Follow Spyglass,TS_RST# has independent RESET# to PCH GPIO pin	Add TS_RST# to PCH GPP_D13 and connect to JIRTS1 pin2,add RZ303,RZ304	0.2(X01)
19	71	ESD	2019/09/20	Compal	Follow ESD suggest to change ESD part main source	Change DI2,DI3 to SC600001600 from SCA00004300	0.2(X01)
20	38	HW	2019/09/23	Compal	Follow NB_MLK add RC delay to +LCDVDD enable.	Add RV180,CV80	0.2(X01)
21	59	HW	2019/09/23	Compal	Board_ID change to X01	Change RE79 to 130Kohm(SD028130380) from 240Kohm(SD028240380)	0.2(X01)
22	77	ME	2019/10/03	Compal	SCREW HOLE	Change H7 to 2P8N,H9 to 2P8N,H24 to 7P0,H28 to 2P7,H20 to 2P3N.	0.2(X01)
23	62	HW	2019/09/27	Compal	Adjust JSDB1 pin define to factory DFB		0.2(X01)
24	70	HW	2019/09/27	Compal	Add PCIE GEN3 redriver for Card Reader	Add CR1~CR6,CR8,CR12,CR13,RR1~RR26,UR1	0.2(X01)
25	51	Sourcer	2019/09/27	Compal	sourcer request	Change CL20,CL21 to 0.47uF_0402(SE00000WA00)from 0.47uF_0201.	0.2(X01)
26	14	HW	2019/09/27	Compal	CRB"TR_DP_TI83_HOST_REF_DESIGN_R2V0"	Remove RH618,change RT593 pull up to +3.3V_TBT_S0.	0.2(X01)
27	18	HW	2019/09/27	Compal	CML PDG1.0	Remove RH327	0.2(X01)
28	18	HW	2019/09/27	Compal	Dynamic RTD3 support for WHL mobile platforms POV - V1.0	Change RH731 to 10Kohm(SD028100280)from 1Kohm.	0.2(X01)
29	11,14,17,18, 19,27,38	HW	2019/09/27	Compal	Align BH_MLK	Change RH319,RH734,RV8,RH72 to 100Kohm, Change RV812,RH400,RH401,RH731 to 10Kohm, Remove RV806,Change RZ543 PWR rail to +1.8V_PRIM_PCH	0.2(X01)
30	10	HW	2019/09/27	Compal	CML PDG1.0	Remove CC272,CC568	0.2(X01)
31	56	ESD	2019/09/27	Compal	ESD request	Change CA1,CA4 connect between LA11.2/LA10.2 and JHP1.4/JHP1.3.	0.2(X01)
32	42	HW	2019/10/01	Compal	vHPD and vPRO docking support	Depop RT619,RT620(vHPD), pop RT641,RT642(vPRO docking)	0.2(X01)
33	51	EMI	2019/10/01	Compal	EMI request	Change RL71~RL78 to 15ohm(SD00001QG80) from 0ohm.	0.2(X01)
34	77	DFB	2019/10/03	Compal	DFB request to change Clip to one unit.	Remove Clip6~Clip9.	0.2(X01)
35	52	HW	2019/10/01	Compal	CML-H platform met black screen issue with CNVi or AX201 WLAN	Change RZ378 to 10Kohm(SD043100280) from 100Kohm.	0.2(X01)
36	19	HW	2019/10/01	Compal	New feature: CPU_XMP_DET and XMP PWR select.	Add RH900,RH901 for CPU_XMP_DET,add XMP_1.35V_SEL# for XMP PWR switch.	0.2(X01)
37	31	EC	2019/10/01	Compal	UV67 I2C address clash with PD.	Add RV11,RV12,QV32 and I2C share with USH/EXPENSOR	0.2(X01)
38	65	HW	2019/10/03	Compal	DFB request	Change UZ12 footprint to ST33HTPH2032AHC1_VQFN32_5X5	0.2(X01)
39	17	Sourcer	2019/10/03	Compal	Sourcer request for muti source.	Change RH874,RH884 to SD000012A80 from SD000012AZ0.	0.2(X01)
40	58	HW	2019/10/03	Compal	Only reserve support EC inform PCH ROM TOP SWAP function	Depop RE847	0.2(X01)
41	27,38	Sourcer	2019/10/03	Compal	Sourcer request	Change DV32,DV33,DV34,DV37,DV39,DV42,DV43,DV44,DV45,DV46,DV47,DV48 to SCS00000Z00 from SCS00005T00.	0.2(X01)
42	38	ESD	2019/10/08	Compal	ESD request	Add DZ3,DZ4,DZ7,DZ10	0.2(X01)
43	70	Vender	2019/10/04	Pericom	TX AC cap. location close at redriver output side(AOP and AON) is better.	Change RR23,RR24(0ohm) to CR7,CR9(0.22uF).	0.2(X01)
44	51	HW	2019/10/07	Compal	544506 i219 checklist rev1.2	Change location CL7 to CL280,CL280 to CL7,and CL7,CL28 connect to +3.3V_LAN_OUT	0.2(X01)
45	52	DELL	2019/10/07	Customer	BT_RADIO_DIS# reserve diode for co-lay on RZ300	Add DZ16 colay on RZ300.	0.2(X01)
46	38	HW	2019/10/07	Compal	Reserve 0.01uF_0402 to LCDVDD load switch input.	Add CV17 to UV24 pin5.	0.2(X01)
47	52	HW	2019/10/07	Compal	CNVi's RST and CLKREQ levelshift circuit modify	Del RZ378,QZ17,RZ376,RZ381,QZ18,depop RZ377,add RZ827,QZ27,UZ1,UZ2	0.2(X01)

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48	38	HW	2019/10/09	Compal	Remove RF choke cloay circuit to aviod impendance discontinuous	Remove RV921~RV928,LV14~LV17	0.2(X01)
49	51	HW	2019/10/09	Compal	Align NB_MLK to follow CML-U_RVP rev2.0	Change CL3 to 22uF(SE00000M000)from 10uF.	0.2(X01)
50	14	HW	2019/10/16	Compal	PDG1.0 P.337	Depop RH613,RH614	0.2(X01)
51	52,58	HW	2019/10/16	Compal	BT_RADIO_DIS#_R routing to PCH and EC through diode	Pop DZ16,RE11,depop RZ300	0.2(X01)
52	70	HW	2019/10/16	Compal	Adjust Card reader PCIE GEN3 redriver setting	Pop RR2,RR3(TX EQ=Max),RR4,RR5(RX EQ=Max),RR8,RR9(Output swing=1120)	0.2(X01)
53	38	HW	2019/10/25	Compal	ESD request	Pop DZ7,DZ10	0.2(X01)
54	18	HW	2019/11/18	Compal	Audio chip can't detect about RF component	Remove CH71	0.3(X01)
55	71	DFB	2019/11/18	Compal	choke colay 0402 R cause open soldering,need change to colay 0201 R.	Change RI60,RI61,RI68,RI70 to 0201 size from 0402 size.	0.3(X01)
56	38	HW	2019/11/21	Compal	Add soft start to touch screen power control pin	Remove RV546,add RV400,change CV635 connect between +3.3V_RUN and QV8.2,change RV6.2 connect to +3.3V_RUN from +5V_RUN	0.3(X01)
57	67,68	ME	2019/11/21	Compal	Change NGFF connector type for user insert /remove SSD card more easily.	Change JNGFF3,JNGFF5 to LOTES_APCI0604-P001A_75P-T from LOTES_YPCI0020-P001A_75P	0.3(X01)
58	59	HW	2019/11/22	Compal	Board ID	Change RE79 to 62Kohm(SD028620280)from 130Kohm.	0.3(X01)
59	66	HW	2019/11/26	Compal	Avoid voltage leakage for No FPR or disable FPR function	Add DZ17 between FPR_RST# and FPR_RST#_USH and change RZ1494 to 0603 size and depop it for colay with DZ17.	0.3(X01)
60	52	HW	2019/11/26	Compal	Solve material single source issue	Change CZ324 to 0402 from 0201	0.3(X01)
61	38	HW	2019/12/2	Compal	Sync up touch and BL function BL on-->touch function enable BL off-->touch function disable	Add DV4,reserve RV13	0.3(X01)
62	20,37,38,43,58,66	HW	2019/11/29	Compal	FET change component to meet customer spec(HBM>500)	Change QT2,QT3 to SB00001SU00 from SB000006O00 Change QV26,QV45,QZ25 to SB00001L800 from SB00000QP00 Change QE15,QH7,QV8,QZ1 to SB00001L800 from SB00000T900 Change QT10 to SB00001ST00 from SB00001GQ00 Change QV1 to SB00001SE00 from SB000008S80	0.3(X01)
63	66	HW	2019/12/5	Compal	TPM change to ST33HTPH2X32AHD4	Change UZ12 to SA0000CYO10 from SA0000CYO00	0.3(X01)
64	17,58	HW	2019/12/16	Compal	Align BH	depop RH310,RE561	0.3(X01)
65	77	HW	2019/12/24	Compal	ADD screw hole	Add H29(H_3P7x0P8N)	0.4(X02)
66	78	HW	2020/1/8	Compal	SSD power off protect	Add SW4	0.4(X02)
67	59	HW	2020/1/8	Compal	Board ID	Change RE79 to 33Kohm(SD028330280)from 62Kohm.	0.4(X02)
68	37	HW	2020/1/15	Compal	FET change component to meet customer spec(HBM>500)	Change QZ20 to SB00001SP10 from SB00001OO00	0.4(X02)
69	67,68	HW	2020/1/15	Compal	Connector list 0103A	Change JNGFF3/JNGFF5 to BELLW_SD-80159-1881 from LOTES_APCI0604-P001A	0.4(X02)
70	51	HW	2020/1/15	Compal	LAN EA	Change RL71,RL72,RL73,RL74,RL75,RL76,RL77,RL78 to 2.2ohm(SD000017H00) from 15ohm.	0.4(X02)
71	77	RF	2020/1/17	Compal	ADD EMI spring	Add SP1,SP2	0.4(X02)
72	38	ESD	2020/1/20	Compal	ESD request	Depop DZ3,DZ4	0.4(X02)
73	18	HW	2020/2/21	Compal	Fix Audio lost	Depop CH268, pop CA76	0.4(X02)
74	42	HW	2020/2/25	Compal	Reserve TBT physical HPD	Depop RT641,RT642, pop RT619,RT620.	0.4(X02)
75	79	HW	2020/2/25	Compal	Reduce power consumption	Change RV625 to 100Kohm(SD028100380)from 47Kohm.	0.4(X02)
76	59	HW	2020/3/18	Compal	Board ID	Change RE79 to 8.2Kohm(SD028820180)from 33Kohm.	1.0(A00)
77	18,52,66,71	HW	2020/3/18	Compal	Modify colay part to cover green paint avoid component shift when SMT.	Change RZ13,RZ14,RI49,RI50,RI75,RI77,RI91,RI92,RI95,RI96,RI93,RI94, RZ15,RZ16,RI71,RI73,RI60,RI61,RI68,RI70,DH1,DH2,RZ1494 footprint to add -NPM.	1.0(A00)
78	29	HW	2020/3/23	Compal	0.4 pitch QFN Symbol modify for SMT solder lack risk.	Change UV64 footprint to PS8331BQFN60GTR-A0_QFN60_5X9 from PS8331BQFN60GTR-A0_QFN60_5X9-S	1.0(A00)
79	63	HW	2020/4/1	Compal	DC-S5 RTC power rail leakage fix.	Depop DE106,DE107,CE71,CE72,CE73,QE19,RE842,RE843,RE844	1.0(A00)
80	79	HW	2020/4/1	Compal	Default ME enable for MP.	Depop SWME1,RH101. pop RH100.	1.0(A00)
81	77	HW	2020/4/1	Compal	Depop debug component for MP.	Depop SW3.	1.0(A00)
82	58	HW	2020/4/2	Compal	EC Change to sign EC for MP	Change UE1 to SA0000CQ740 from SA0000CQ730.	1.0(A00)
83	38	HW	2020/5/8	Compal	for HDR600 panel power consumption support	Change FZ2 to SP04000AZ00 from SP040007G00.	1.0(A00)
84	38,79	HW	2020/8/26	Compal	BITS463365 PRTS_RT15] Sharp UHD_5785V_SUT will found LED behavior abnormal(2A8W)	Change FZ2 to SP040009U00 from SP04000AZ00, RV623 to SD028100280 from SD028100380, RV624 to SD028100380 from SD028100480.	1.0(A00)

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