1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2016-08-30

X748 MLB

LAST_MODIFIED=Tue Aug 30 19:51:23 2016

LAST_MODIFICATION=Tue Aug 30 19:51:23 2016

LAST_MODIFICATION=Tue Aug 30 19:51:23 2016

AARON_MLB 07/29/2016

DRAWING
TITLE=X748 MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Aug 30 19:51:23 2016

SCHEM,KBL-U,MLB

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

DRAWING TITLE
SCHEM,MLB,X748

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D
REVISION 3.13.0
BRANCH
PAGE 1 OF 105
SHEET 1 OF 70

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-01543	1	SCHEM,MLB,X748	SCH	CRITICAL	
820-00629	1	PCBF,MLB,X748	PCB	CRITICAL	
685-00110	1	PCBA,MLB,X748,COMMON PARTS	CMNPTS		MLB_CMNPTS

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00159	PCBA,MLB,DEV,X748	DEVELOPMENT,X748_DEVEL
685-00110	PCBA,MLB,X748,COMMON PARTS	X748_COMMON
639-02230	PCBA,MLB,SSD,X748	MLB_CMNPTS,ALTERNATE,CPU:ULT,SSD:Y
639-02258	PCBA,MLB,HDD,X748	MLB_CMNPTS,ALTERNATE,CPU:ULT,SSD:N
639-02806	PCBA,MLB,SSD,X748,SOCKET	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,SSD:Y
639-02807	PCBA,MLB,HDD,X748,SOCKET	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,SSD:N

BOM Groups

BOM GROUP	BOM OPTIONS
X748_COMMON	COMMON,ALTERNATE,X748_PROGPARTS,SMCREG:SUP,XDP,USB_OC_ISO:Y,SMBUS1:ISOL,RTCRST:Y,BOARD_ID:3,USB2_PCH
X748_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
X748_DEVEL	XDP_CONN,SAMCONN

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA13156	U0500	CRITICAL	CPU:SOCKET
337S00323	1	CPU,KBL,QL9J,ES,J0,1.8,15W,.95,BGA1356	U0500	CRITICAL	CPU:ULT

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00711	1	IC,EFI,VTBD,EVT,X748	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,SERIAL FLASH,64MBIT,3V,8P,WSON,QE=1	U5210	CRITICAL	BOOTROM:BLANK
341S00566	1	IC,SMC-81,EXTERNAL,2.36A5,X748	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-81,40MHZ/50MIPS,MCU,1578GA	U5000	CRITICAL	SMC:BLANK
341S00653	1	IC,CAMERA,FLASH,VTBD,PROTO 1,748	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00705	1	IC,AR,VTBD,EVT,X748	U2890	CRITICAL	TBTROM:PROG
335S00133	1	IC,SPI FLASH,8MBIT,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET SPI ROM,NYMONYX,V1.15,J16/J16G/J17	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-00053	1	CONN,RCPT,USBC,DUAL,X648	J3300	CRITICAL	

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0124	377S0057		ALL	TVS
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0479	197S0478		ALL	12 MHz Cam. Xtal
197S0486	197S0478		ALL	12 MHz Cam. Xtal
107S0251	107S0249		ALL	Sense resistor
197S0481	197S0480		ALL	25MHz Xtal
197S0343	197S0480		ALL	25MHz Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
378S0391	378S0390		ALL	Debug LEDs
341S00016	341S3912		ALL	ENET ROM,ADESTO,V1.15
197S0542	197S0544		ALL	24 MHz PCH XTal
197S0545	197S0544		ALL	24 Mhz PCH XTal
197S0369	197S0392		ALL	32 KHz PCH Xtal
197S0399	197S0392		ALL	32 KHz PCH Xtal
376S0572	376S0659		ALL	Single P-Ch FET
376S00001	376S0659		ALL	Single P-Ch FET
376S0972	376S00075		ALL	Single N-Ch FET
132S0401	132S00012		ALL	0.22uF,X7R,0402
155S0830	155S0316		ALL	FER BD,600 OHM,0.5A,0603
155S00076	155S0546		ALL	FER BD,600 OHM,300MA,402
128S0444	128S0323		ALL	CAP,330UF,6.3V,25MOHM
128S0311	128S0329		ALL	CAP,220UF,6.3V,35MOHM
128S00042	128S0329		ALL	CAP,220UF,6.3V,35MOHM
371S00043	371S0463		ALL	DIODE,SCHOTTKY,30V,100MA
371S0567	371S00095		ALL	DIODE,100V,0.25A
152S00358	152S00208		ALL	IND,1UH,2.1A,128MOHM
138S00084	138S00060		ALL	CAP,47UF,6.3V,0603
138S0714	138S0713		ALL	CAP,10UF,6.3V,0402
152S00403	152S00322		ALL	IND,0.68UH,20%,6.1A,20MOHM
138S00093	138S00035		ALL	CAP,20UF,20%,2.5V,0402
116S0175	116S00006		ALL	RES,0OHM,3A,0402
138S0676	138S0691		ALL	CAP,CER,22UF,20%,6.3V
152S1499	152S0864		ALL	IND,47UH,0.58MOHM,0402
138S0641	138S0700		ALL	CAP,CER,2.2UF,0402
138S0739	138S0706		ALL	CAP,CER,1UF,0201
353S00712	353S2216		ALL	INA211,CURRENT SENSE
152S00604	152S1175		ALL	IND,2.2UH,10A
371S0684	371S0495		ALL	DIODE,DUAL SCHOTTKY,SOT363
377S0184	377S00031		ALL	DIODE,5.3V,0.2PF,201
197S00089	197S0369		ALL	XTAL,32.768,20PPM,12.5PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0660	155S0513		ALL	220HM EMI BEAD
376S00074	376S0855		ALL	Dual N-Ch FET
376S1129	376S0855		ALL	Dual N-Ch FET
376S00074	376S0855	SSD:Y	ALL	Dual N-Ch FET
376S1129	376S0855	SSD:Y	ALL	Dual N-Ch FET
311S0649	311S0541		ALL	Single AND Gate
353S4376	353S3384		ALL	HDD OOBv1 comparator
311S00014	311S0515		ALL	TBT JTAG ISOLATION BUFFER
311S00013	311S0508		ALL	Single Buffer Driver OD
371S00019	371S0463		ALL	Rohm Schottky Barrier Diode
138S0746	138S0705		ALL	CAP,CER,X5R,10uF,20%,10V,402
311S00004	311S0370		ALL	SPI Quad I/O MUX
311S00072	311S0657		ALL	AND gate
376S1184	376S1183		ALL	BLC replacement FETs
353S00519	353S00831		ALL	DCDC CPU DRMOS
152S00182	152S00388		ALL	DCDC 2.2UH 4.5A INDUCTOR
138S00015	138S0777		ALL	DCDC 10UF 16V X6S 0603
124-0492	124-0403		ALL	DCDC 180UF 16V TH POLY CAP
353S2220	353S00034		ALL	IC,SPDT,SW/2:1 MUX
311S00120	311S0457		ALL	IC74AUG2G14,SCH-TR
376S0977	376S00078		ALL	XSTR,FET,N-CH,DUAL,20V,2.2OHM
155S00007	155S0667		ALL	FLTR,COMMON,MODE,90OHM,100MA
155S0935	155S0667		ALL	FLTR,COMMON MODE,90OHM,100MA
353S00854	353S4342		ALL	ICREF3330,V-REF,3V,5MA
155S0659	155S0382		ALL	FLTR,EMI,FERR,BD,30OHMS,1.7A
197S00047	197S00036		ALL	XTAL,25MHZ,15PPM,20PF,50OHM
107S00030	107S00029		ALL	RES,DCDC SENSE,0.005OHM,1%
107S00087	107S00029		ALL	RES,DCDC SENSE,0.005OHM,1%
107S00015	107S00011		ALL	RES,DCDC SENSE,0.75MOHM,1%
152S1804	152S1876		ALL	IND,DCDC,1UH,11A
152S00601	152S1289		ALL	IND,DCDC,0.47UH,9A
155S00155	155S0441		ALL	FLTR,EMI,FER BD,220OHM,1.4A
371S0718	371S0531		ALL	DIODE,BAT54,SHOTTKY,30V
353S00769	353S4398		ALL	IC,TPS22966,LOADSW,6A
311S0536	311S0341		ALL	IC,SNGL BUFFER W/OD
353S00993	353S2541		ALL	IC,NCS20081,OP-AMP,R-R
740S00035	740S0115		ALL	FUS,FAST-ACTING,32V,2A,0603

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00111	08	CPU,BDW-ULT,2+GT3
338S1247	02	TBT,Falcon Ridge-4c
341S00158	07	IC,SERIAL FLASH,Quad-IO
333S0784	07	32Gb,25nm LPDDR3-1866
333S0786	07	16Gb,29nm LPDDR3-1866
333S0790	07	32Gb,25nm LPDDR3-1866
333S0792	07	16Gb,25nm LPDDR3-1866
333S00004	07	16Gb,23nm LPDDR3-1866

SYNC_MASTER=VINCE_MLB SYNC_DATE=04/05/2016

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

REVISION 3.13.0

BRANCH

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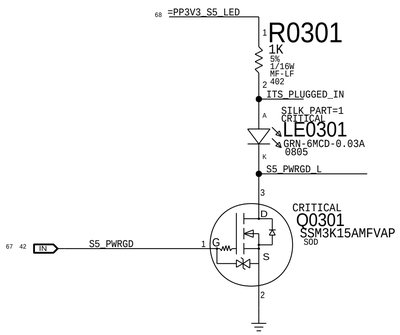
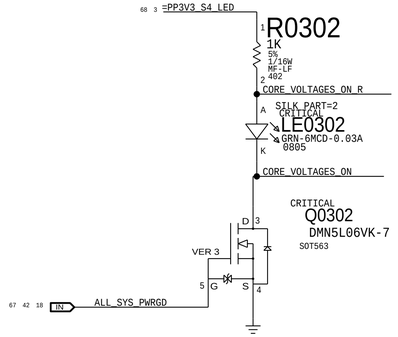
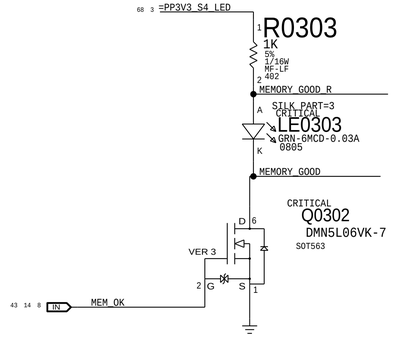
S5 Led



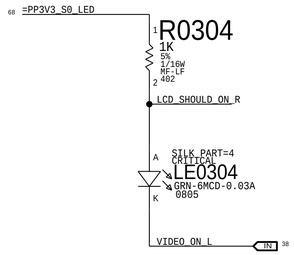
ALL_SYS_PWRGD Led



MEM_GOOD Led



VIDEO ON Led



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SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=02/18/2016

PAGE TITLE

LEDS

Apple Inc.

DRAWING NUMBER 051-01543

SIZE D

REVISION 3.13.0

BRANCH

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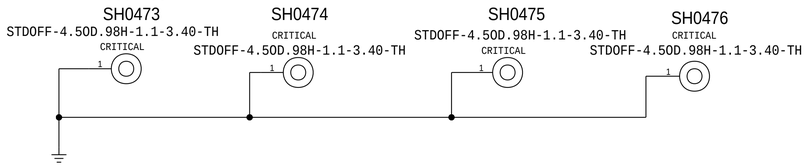
CPU HEATSINK MOUNTING FEATURES

APN:860-1532

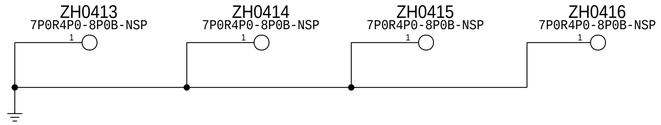


HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

Rear Cover

APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)

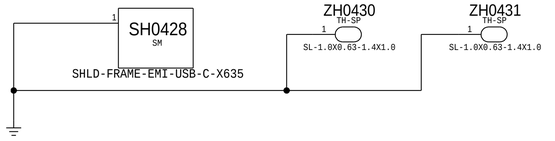


WIRELESS CARD MTG HOLES

APN:998-06186 (PLATED THRU HOLES, DIAMS 3.30 AND 3.20)

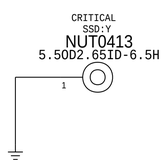
USB-C EMI SHIELD

APN:806-07338



SSD STANDOFF

APN: 860-00314



BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

BRANCH:

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CRITICAL

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 1 OF 20

26	OUT	DP_DDI1_ML_C_N<0>	E55	DDI1_TXN[0]	C47	DP_INT_ML_N<0>	OUT 39
26	OUT	DP_DDI1_ML_C_P<0>	F55	DDI1_TXP[0]	C46	DP_INT_ML_P<0>	OUT 39
26	OUT	DP_DDI1_ML_C_N<1>	E58	DDI1_TXN[1]	D46	DP_INT_ML_N<1>	OUT 39
26	OUT	DP_DDI1_ML_C_P<1>	F58	DDI1_TXP[1]	C45	DP_INT_ML_P<1>	OUT 39
26	OUT	DP_DDI1_ML_C_N<2>	F53	DDI1_TXN[2]	A45	DP_INT_ML_N<2>	OUT 39
26	OUT	DP_DDI1_ML_C_P<2>	G53	DDI1_TXP[2]	B45	DP_INT_ML_P<2>	OUT 39
26	OUT	DP_DDI1_ML_C_N<3>	F56	DDI1_TXN[3]	A47	DP_INT_ML_N<3>	OUT 39
26	OUT	DP_DDI1_ML_C_P<3>	G56	DDI1_TXP[3]	B47	DP_INT_ML_P<3>	OUT 39
				DDI	EDP		
26	OUT	DP_DDI2_ML_C_N<0>	C50	DDI2_TXN[0]	E45	DP_INT_AUX_N	BI 39
26	OUT	DP_DDI2_ML_C_P<0>	D50	DDI2_TXP[0]	F45	DP_INT_AUX_P	BI 39
26	OUT	DP_DDI2_ML_C_N<1>	C52	DDI2_TXN[1]	B52	NC	
26	OUT	DP_DDI2_ML_C_P<1>	D52	DDI2_TXP[1]	G50	DP_DDI1_AUXCH_C_N	BI 26
26	OUT	DP_DDI2_ML_C_N<2>	A50	DDI2_TXN[2]	F50	DP_DDI1_AUXCH_C_P	BI 26
26	OUT	DP_DDI2_ML_C_P<2>	B50	DDI2_TXP[2]	E48	DP_DDI2_AUXCH_C_N	BI 26
26	OUT	DP_DDI2_ML_C_N<3>	D51	DDI2_TXN[3]	F48	DP_DDI2_AUXCH_C_P	BI 26
26	OUT	DP_DDI2_ML_C_P<3>	C51	DDI2_TXP[3]			

DISPLAY SIDEBANDS

68 10 8 =PP0V95_S0_CPU_VCCIO

R0530 1
24.9
1%
1/20W
MF
201
2
PLACE_NEAR=U0500.E52:15.24MM

17 5	IN	XDP_USB_EXTD_OC_L	B9	GPP_E12/USB2_OC3*	A7	XDP_PCH_OBSDATA_A3	OUT 17
19	IN	DP_DDPB_HPD	L9	GPP_E13/DDPB_HPD0	H1	XDP_PCH_OBSDATA_B0	OUT 17
				GPP_E9/USB2_OC0*	A9	XDP_USB_EXTA_OC_L	IN 5 17
19	IN	DP_DDPC_HPD	L7	GPP_E14/DDPC_HPD1	C9	XDP_USB_EXTB_OC_L	IN 5 17
NO_TEST=1		NC_PCH_GPP_E15	L6	GPP_E15/DDPD_HPD2		GPP_E10/USB2_OC1*	
				GPP_E11/USB2_OC2*	D9	XDP_USB_EXTC_OC_L	IN 5 17
19 5	IN	JTAG_ISP_TDO	N9	GPP_E16/DDPE_HPD3	R12	EDP_BKLT_EN	OUT 5 19
39	IN	DP_INT_HPD	L10	GPP_E17/EDP_HPD	R11	NC_EDP_BKLT_PWM	NO_TEST=1
		EDP_COMP	E52	EDP_RCOMP	U13	EDP_PANEL_PWR_EN	OUT 5 19
				EDP_VDDEN			

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 20 OF 20
SPARE

FOR FUTURE PRODUCT PER PDG

12 =PP1V8_SUS_PCH_VCC1P8_U12
12 =PP1V8_SUS_PCH_VCC1P8_U11

NC	AW69	RSVD	F6	RSVD	NC
NC	AW68	RSVD	E3	RSVD	NC
NC	AU56	RSVD	C11	RSVD	NC
NC	AW48	RSVD	B11	RSVD	NC
NC	C7	RSVD	A11	RSVD	NC
	U12	RSVD	D12	RSVD	NC
	U11	RSVD	C12	RSVD	NC
NC	H11	RSVD	F52	RSVD	NC
NC	G46	RSVD	F46	RSVD	NC

=PP3V3_SUS_PCH_VCCPRIM 8 12 68

BOMOPTION=USB_OC_ISO:N	R0550	100K	1 2	5% 1/20W MF 201	XDP_USB_EXTA_OC_L		5 17
BOMOPTION=USB_OC_ISO:N	R0551	100K	1 2	5% 1/20W MF 201	XDP_USB_EXTB_OC_L		5 17
BOMOPTION=USB_OC_ISO:N	R0552	100K	1 2	5% 1/20W MF 201	XDP_USB_EXTC_OC_L		5 17
BOMOPTION=USB_OC_ISO:N	R0553	100K	1 2	5% 1/20W MF 201	XDP_USB_EXTD_OC_L		5 17

=PP3V3_S0_PCH 6 13 14 15 16 18 19 68

R0554	10K	1 2	5% 1/20W MF 201	JTAG_ISP_TDO		5 19
R0560	100K	1 2	5% 1/20W MF 201	EDP_BKLT_EN		5 19
R0561	100K	1 2	5% 1/20W MF 201	EDP_PANEL_PWR_EN		5 19

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Aug 18 12:55:20 2015

PAGE TITLE
CPU GFX

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
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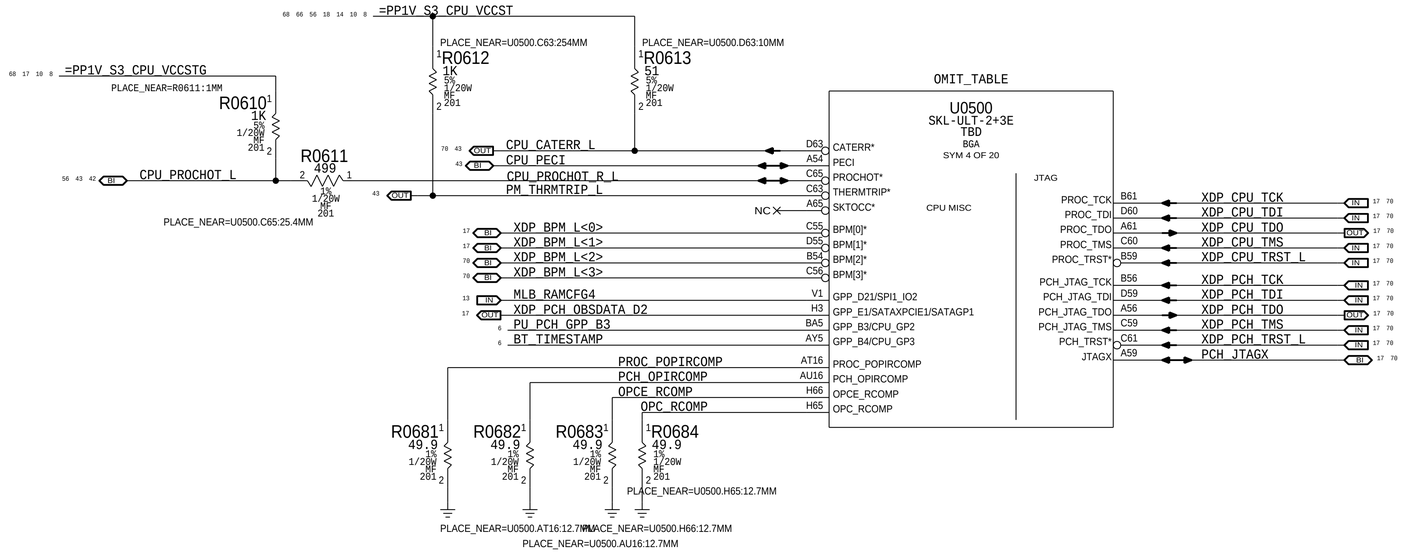

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue Aug 18 12:55:20 2015

PAGE TITLE
CPU MISC/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER 051-01543
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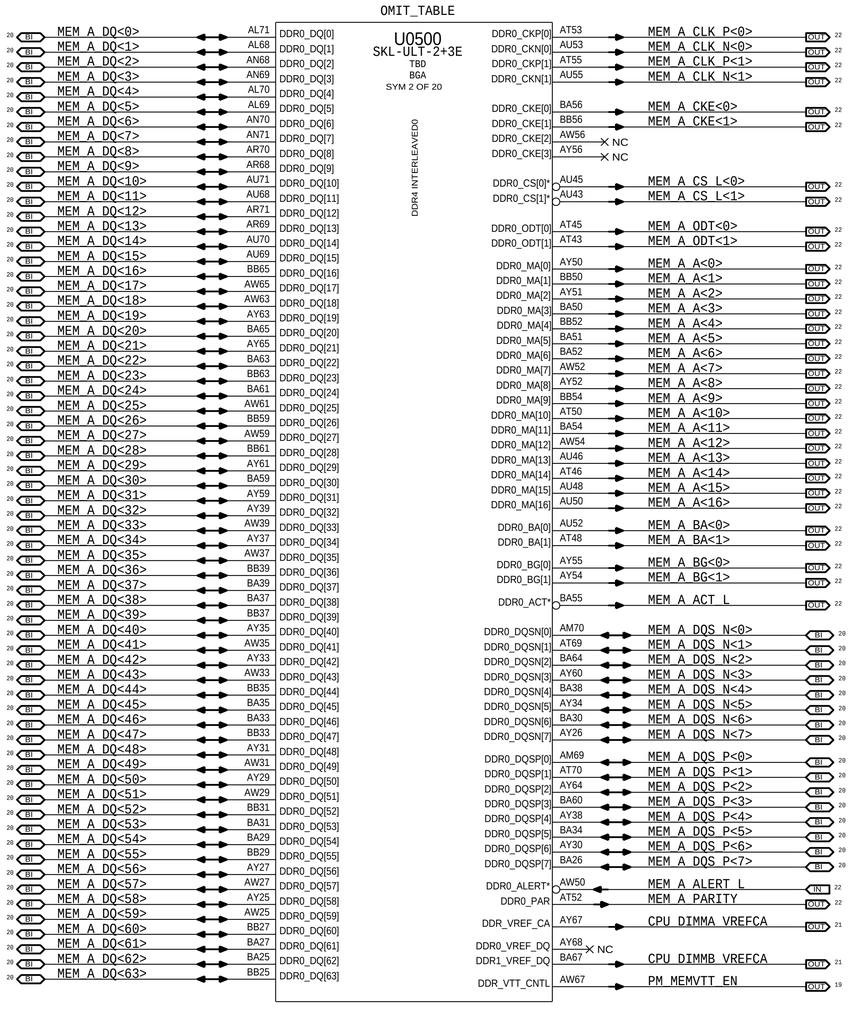

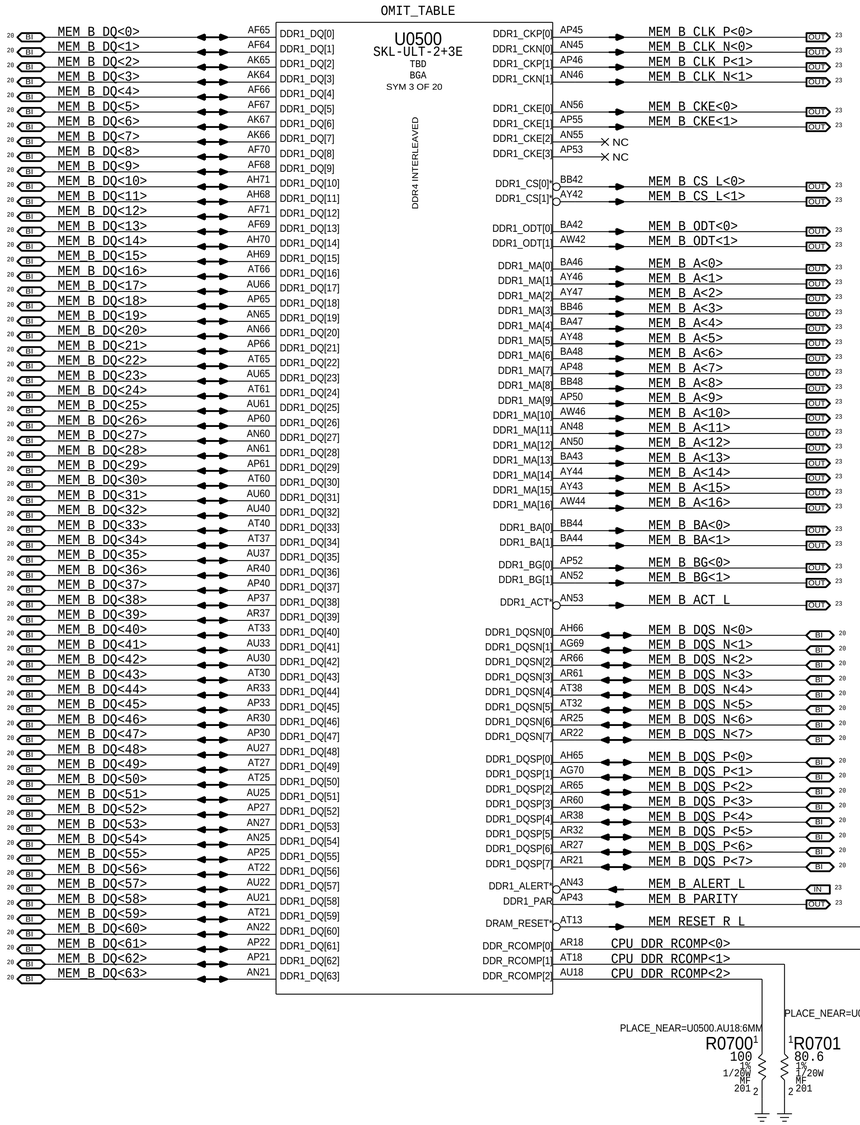

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AARON_MLB SYNC_DATE=03/21/2016

PAGE TITLE

CPU DDR4 Interface

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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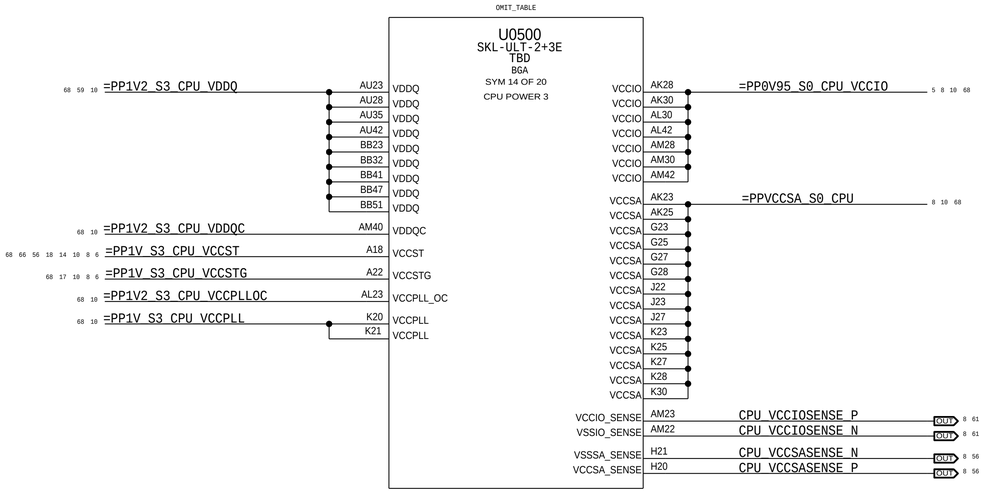
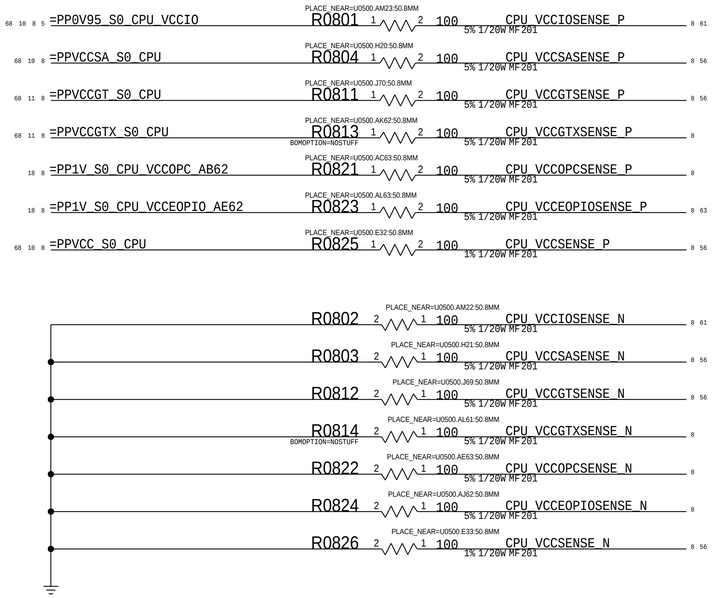
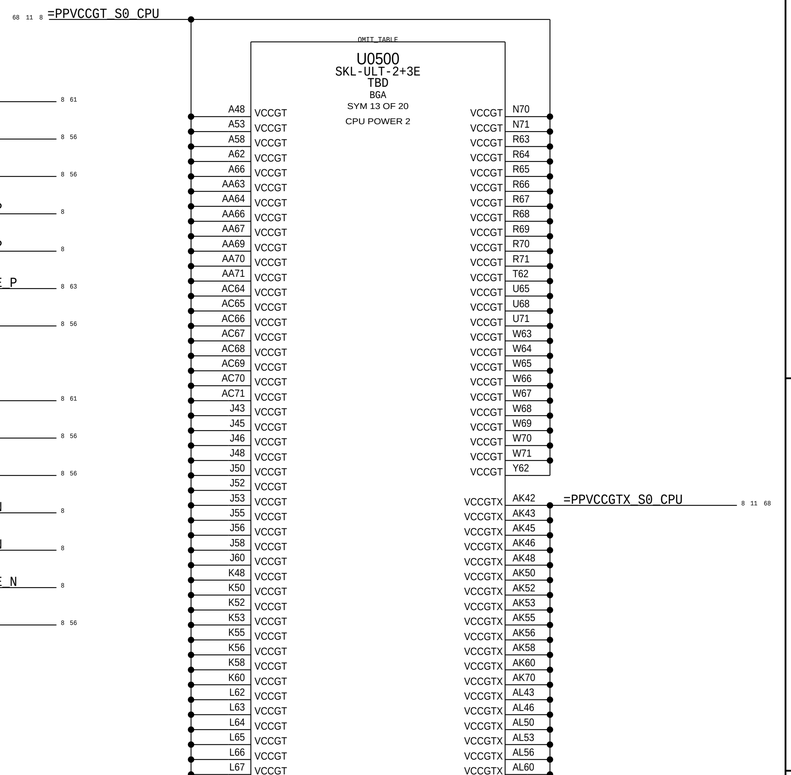
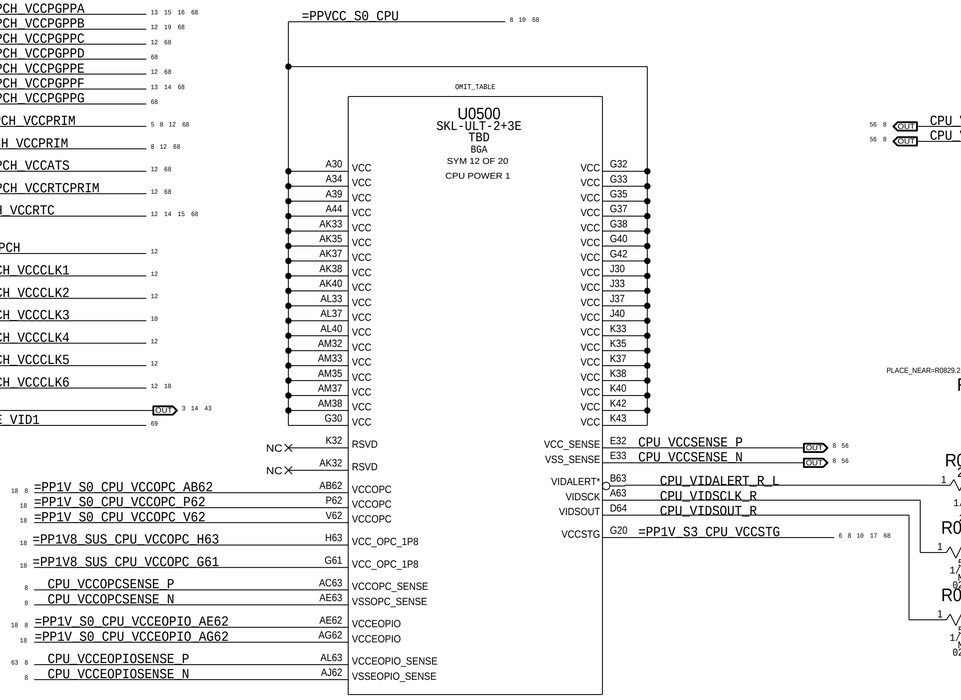
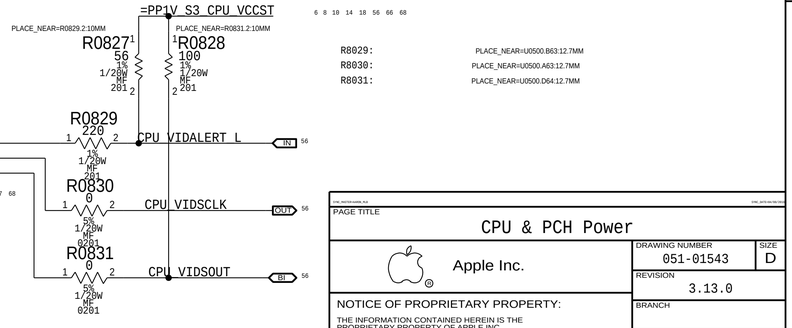
SHEET 7 OF 70











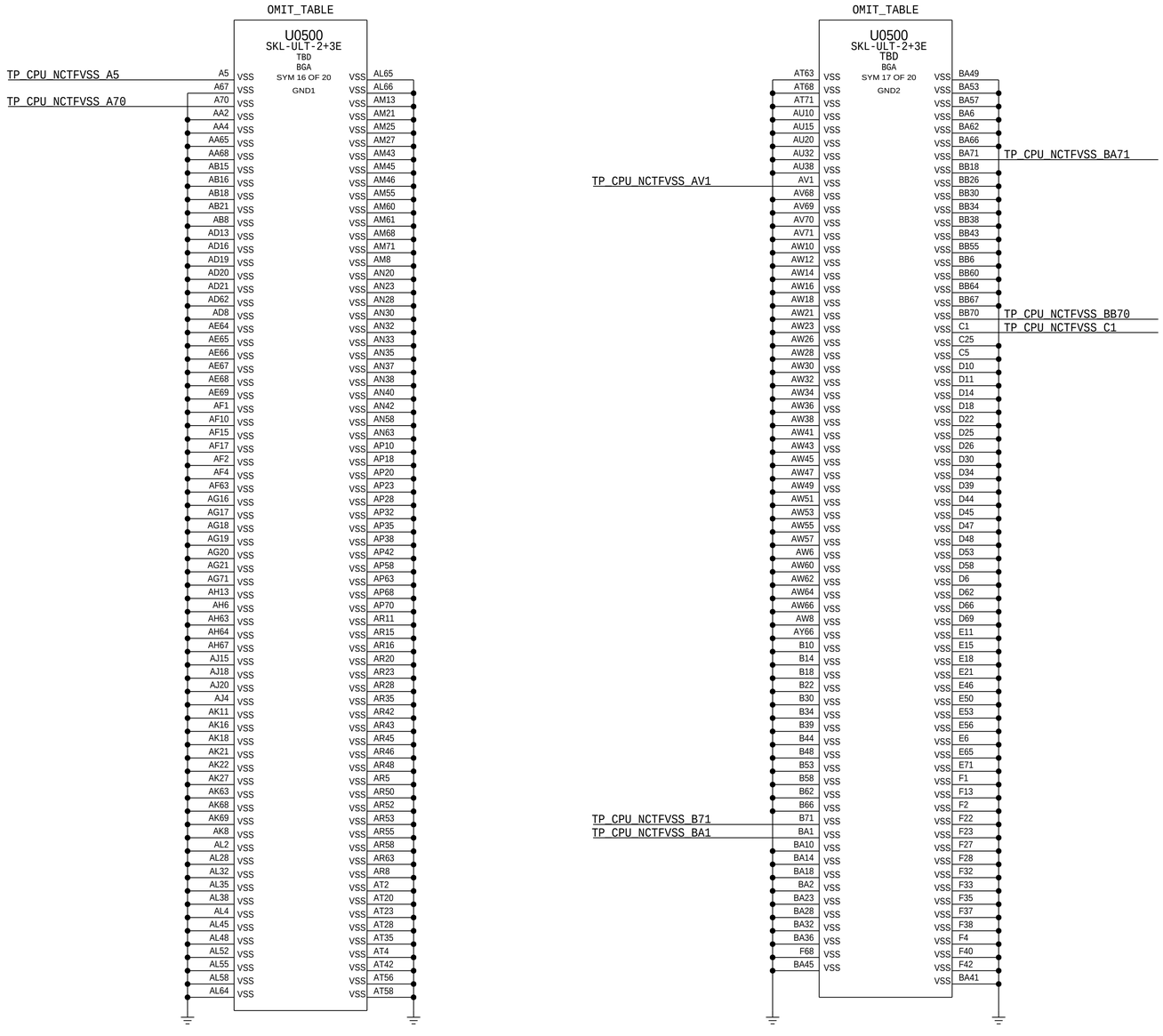
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU & PCH Power

Apple Inc.

DRAWING NUMBER	051-01543
SIZE	D
REVISION	3.13.0
BRANCH	
PAGE	8 OF 105
SHEET	8 OF 70



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J13B_MLB SYNC_DATE=11/18/2016

PAGE TITLE

CPU & PCH Grounds

Apple Inc.

DRAWING NUMBER 051-01543

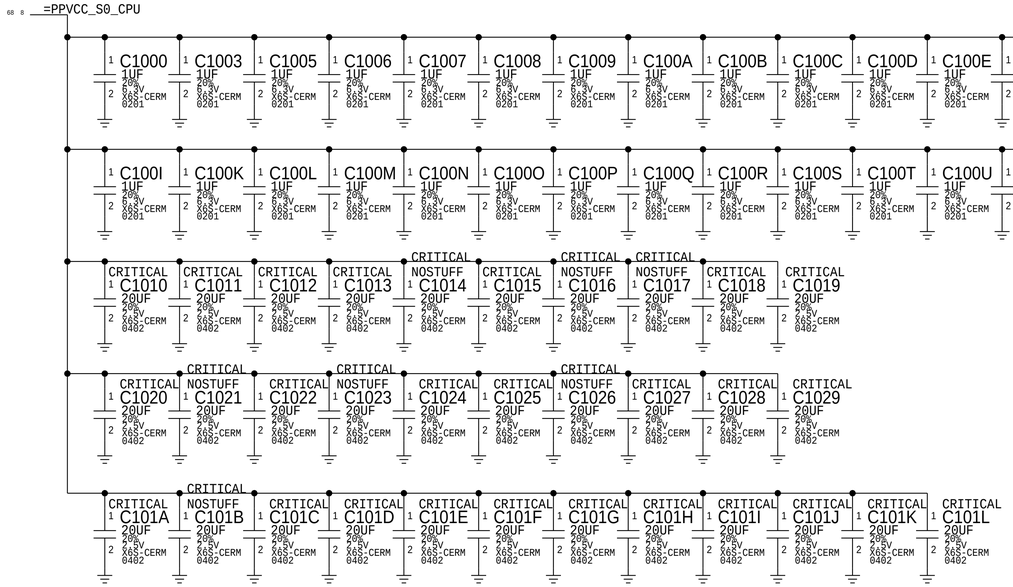
SIZE D

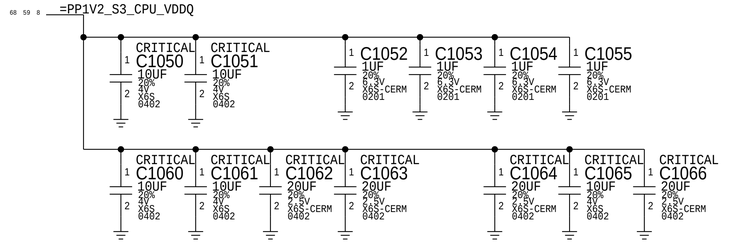
REVISION 3.13.0

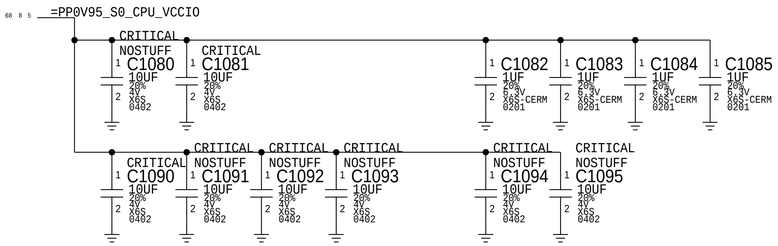
BRANCH

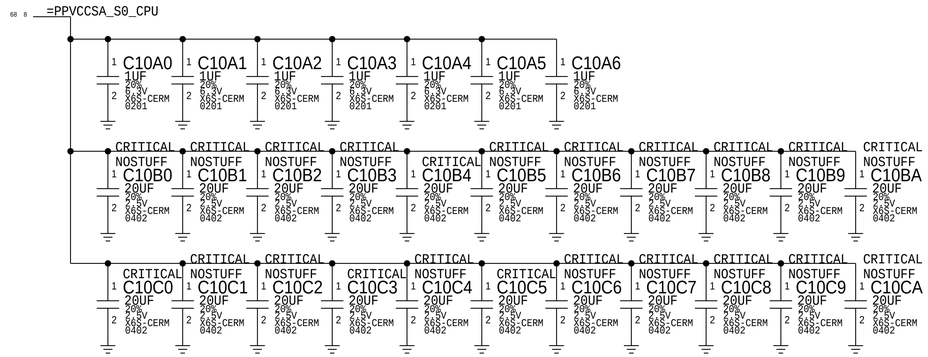
PAGE 9 OF 105

SHEET 9 OF 70









BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AARON_HLB SYNC_DATE=02/23/2016

PAGE TITLE

CPU Core Decoupling

Apple Inc.

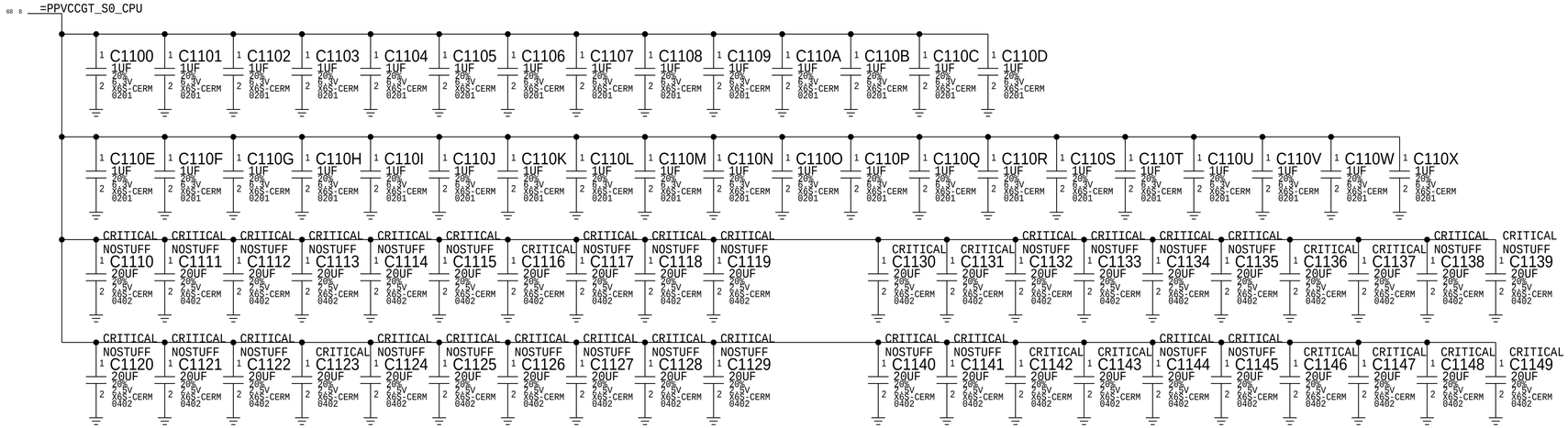
DRAWING NUMBER 051-01543 SIZE D

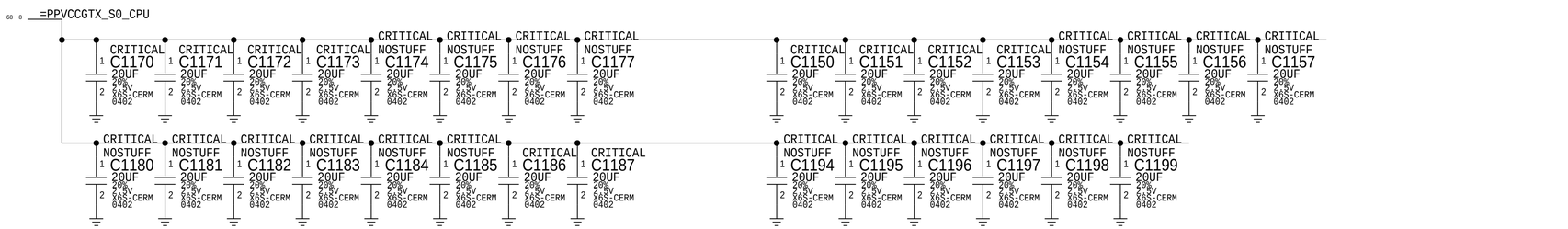
REVISION 3.13.0

BRANCH

PAGE 10 OF 105

SHEET 10 OF 70





BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU GT Decoupling

Apple Inc.

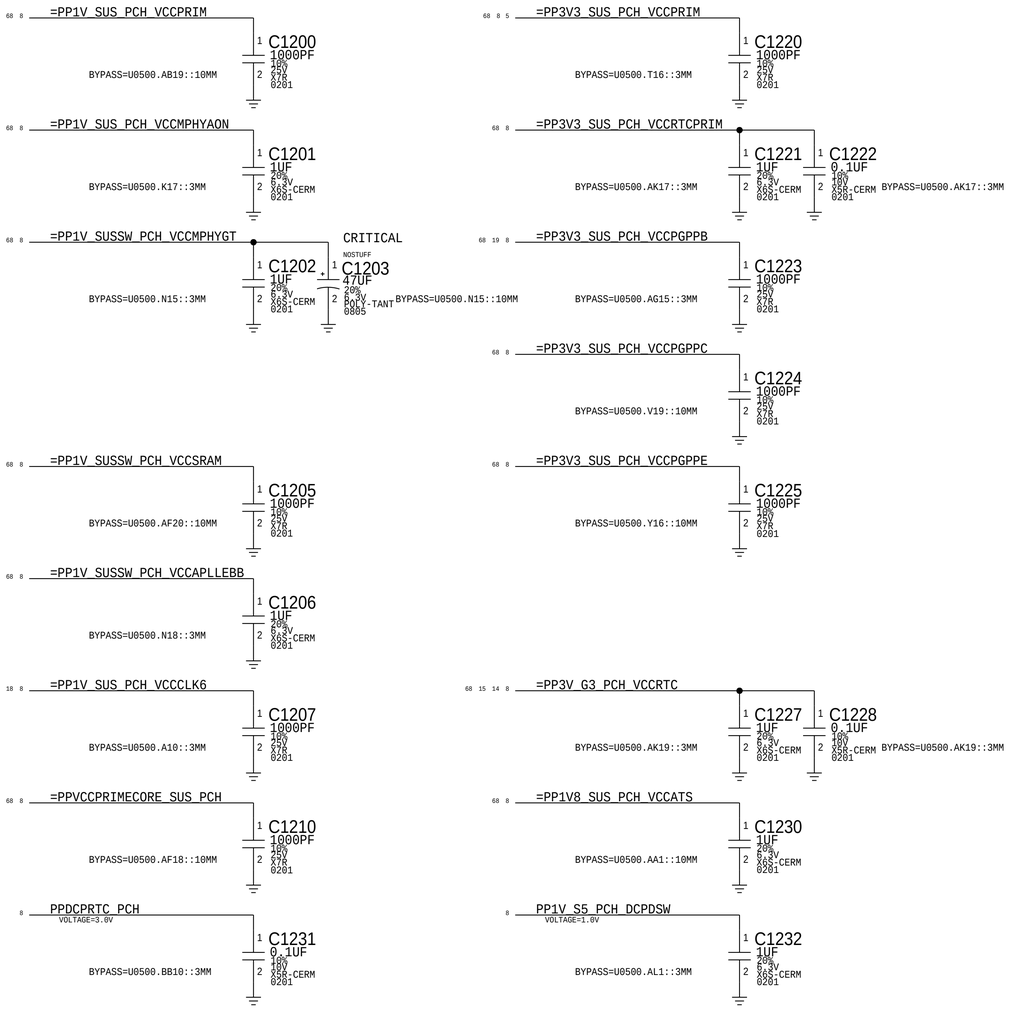
DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

BRANCH:

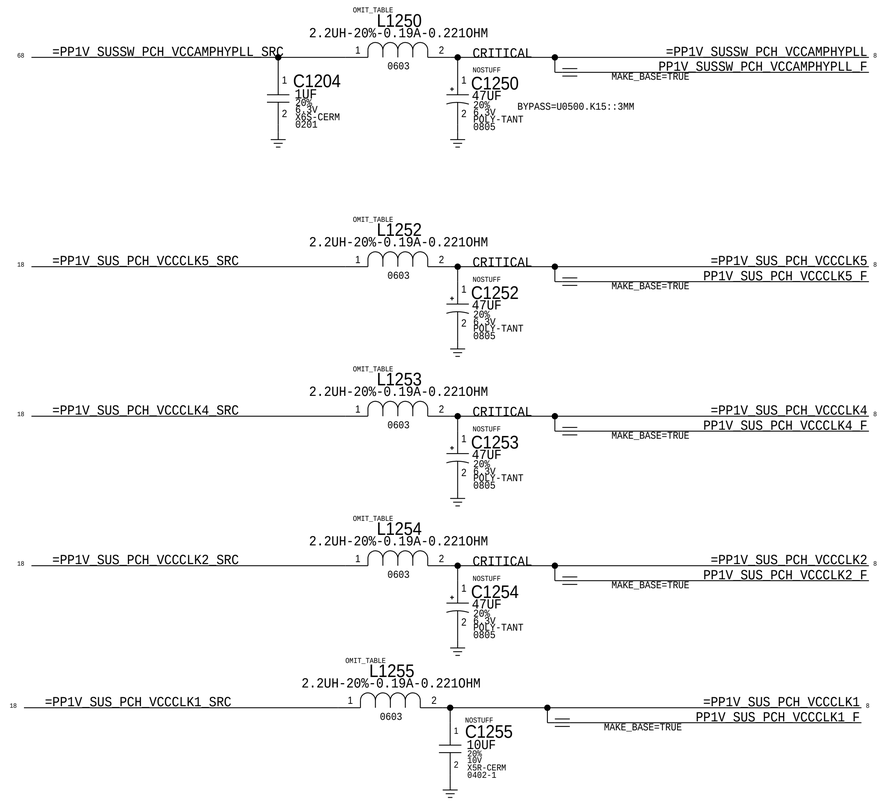
PAGE: 11 OF 105

SHEET: 11 OF 70

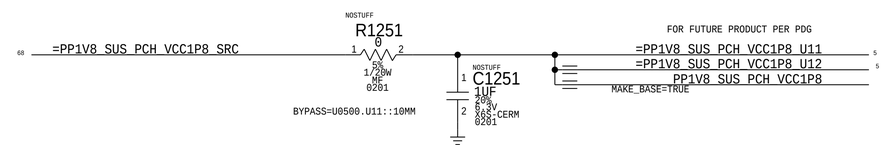


FILTER PLACEHOLDERS ONLY

RAIL SIDE PCH SIDE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	5	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254,L1255		



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Decoupling

Apple Inc.

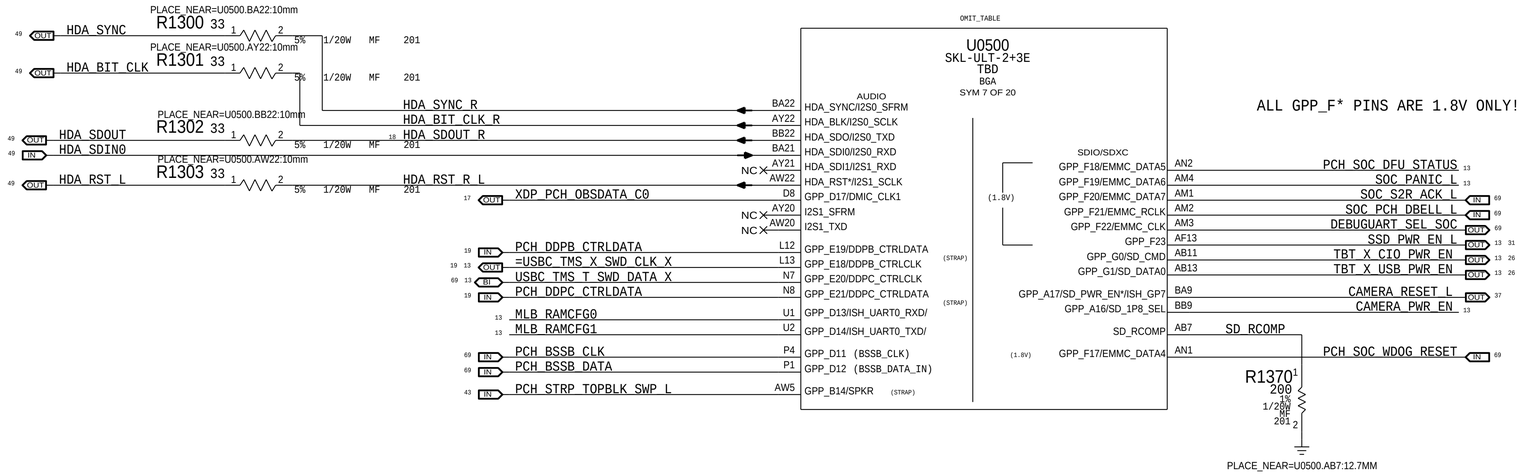
DRAWING NUMBER: 051-01543 SIZE: D

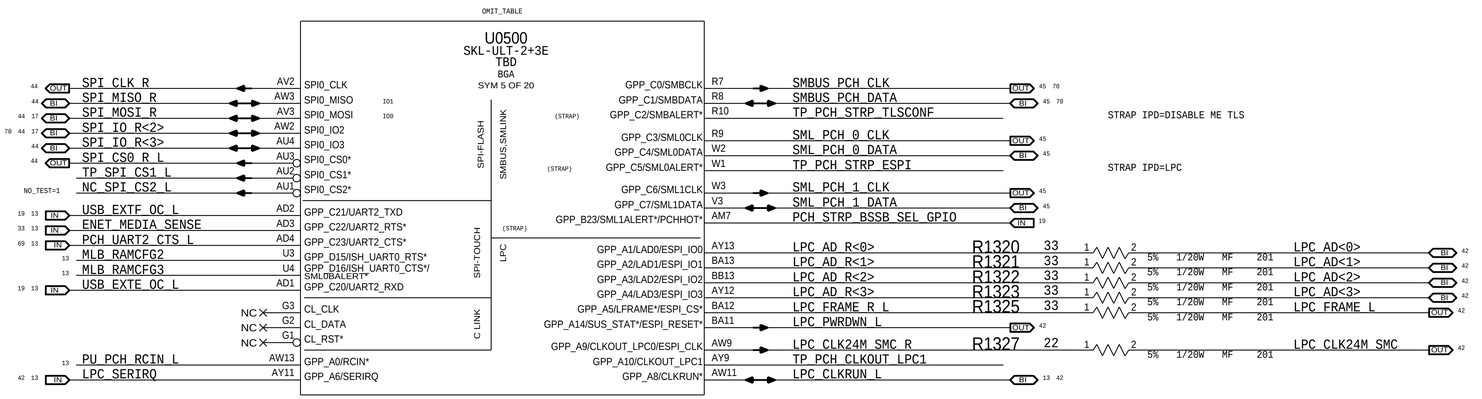
REVISION: 3.13.0

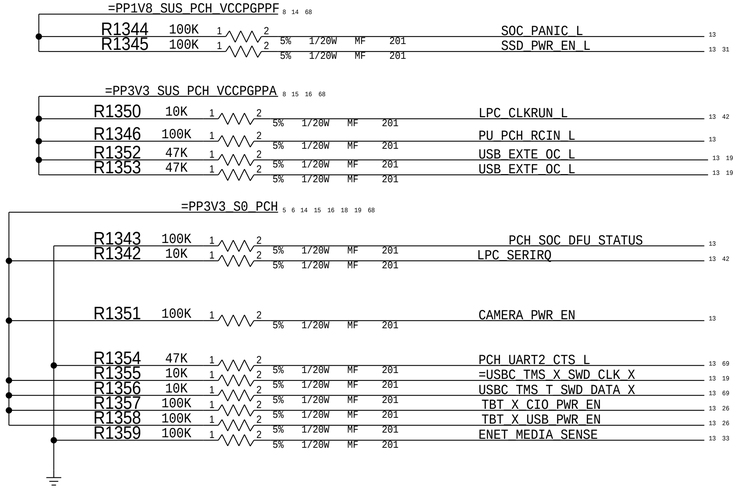
BRANCH:

PAGE: 12 OF 105

SHEET: 12 OF 70

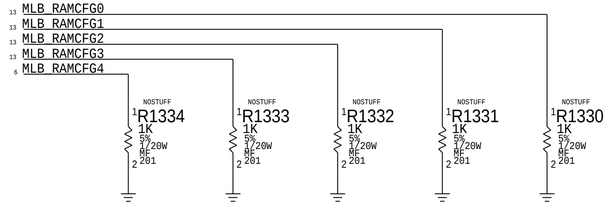






MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM_COST_GROUP=CPU & CHIPSET

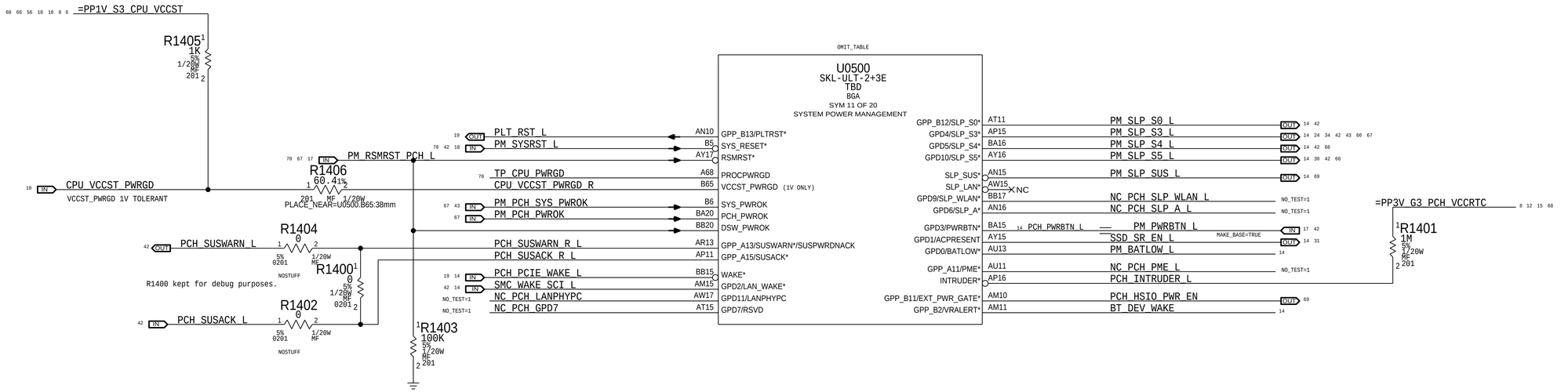
DESIGN: X502/MLB
LAST CHANGE: Wed Sep 30 12:58:31 2015

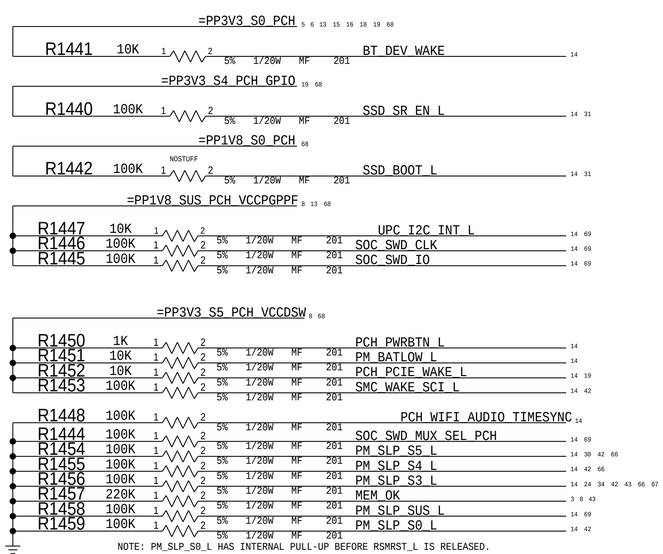
PAGE TITLE
PCH Audio/LPC/SPI/SMBus

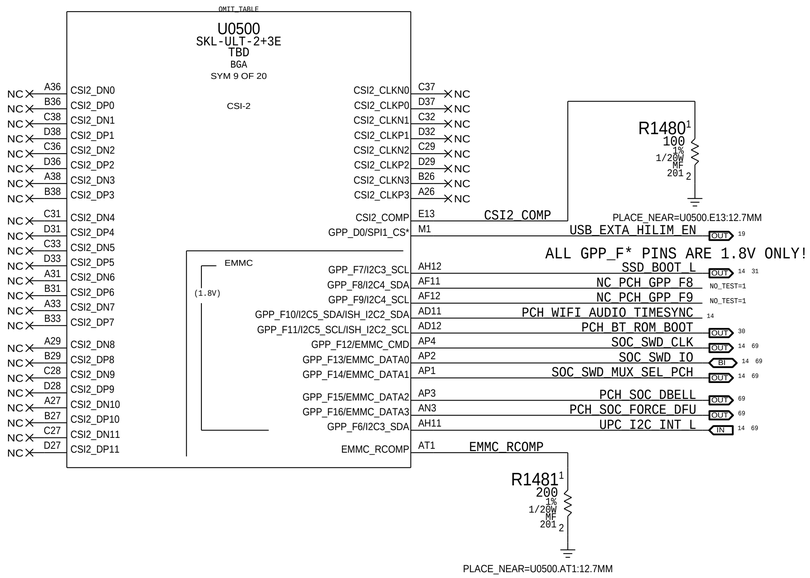
Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
BRANCH
PAGE 13 OF 105
SHEET 13 OF 70

PCH Reset Button







BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Thu Sep 24 14:34:44 2015

PAGE TITLE
PCH Power Management

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
BRANCH
PAGE 14 OF 105
SHEET 14 OF 70

PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

SSD LANE 0
- PCIE_SSD_D2R_N<0> — H13 — PCIE1_RXN/USB3_5_RXN
- PCIE_SSD_D2R_P<0> — G13 — PCIE1_RXP/USB3_5_RXP
- PCIE_SSD_R2D_N<0> — B17 — PCIE1_TXN/USB3_5_TXN
- PCIE_SSD_R2D_P<0> — A17 — PCIE1_TXP/USB3_5_TXP

SSD LANE 1
- PCIE_SSD_D2R_N<1> — G11 — PCIE2_RXN/USB3_6_RXN
- PCIE_SSD_D2R_P<1> — F11 — PCIE2_RXP/USB3_6_RXP
- PCIE_SSD_R2D_N<1> — D16 — PCIE2_TXN/USB3_6_TXN
- PCIE_SSD_R2D_P<1> — C16 — PCIE2_TXP/USB3_6_TXP

SSD LANE 2
- PCIE_SSD_D2R_N<2> — H16 — PCIE3_RXN
- PCIE_SSD_D2R_P<2> — G16 — PCIE3_RXP
- PCIE_SSD_R2D_N<2> — D17 — PCIE3_TXN
- PCIE_SSD_R2D_P<2> — C17 — PCIE3_TXP

SSD LANE 3
- PCIE_SSD_D2R_N<3> — G15 — PCIE4_RXN
- PCIE_SSD_D2R_P<3> — F15 — PCIE4_RXP
- PCIE_SSD_R2D_N<3> — B19 — PCIE4_TXN
- PCIE_SSD_R2D_P<3> — A19 — PCIE4_TXP

Thunderbolt X lane 0
- PCIE_TBT_X_D2R_N<0> — F16 — PCIE5_RXN
- PCIE_TBT_X_D2R_P<0> — E16 — PCIE5_RXP
- PCIE_TBT_X_R2D_C_N<0> — C19 — PCIE5_TXN
- PCIE_TBT_X_R2D_C_P<0> — D19 — PCIE5_TXP

Thunderbolt X lane 1
- PCIE_TBT_X_D2R_N<1> — G18 — PCIE6_RXN
- PCIE_TBT_X_D2R_P<1> — F18 — PCIE6_RXP
- PCIE_TBT_X_R2D_C_N<1> — D20 — PCIE6_TXN
- PCIE_TBT_X_R2D_C_P<1> — C20 — PCIE6_TXP

Thunderbolt X lane 2
- PCIE_TBT_X_D2R_N<2> — F20 — PCIE7_RXN/SATA0_RXN
- PCIE_TBT_X_D2R_P<2> — E20 — PCIE7_RXP/SATA0_RXP
- PCIE_TBT_X_R2D_C_N<2> — B21 — PCIE7_TXN/SATA0_TXN
- PCIE_TBT_X_R2D_C_P<2> — A21 — PCIE7_TXP/SATA0_TXP

Thunderbolt X lane 3
- PCIE_TBT_X_D2R_N<3> — G21 — PCIE8_RXN/SATA1A_RXN
- PCIE_TBT_X_D2R_P<3> — F21 — PCIE8_RXP/SATA1A_RXP
- PCIE_TBT_X_R2D_C_N<3> — D21 — PCIE8_TXN/SATA1A_TXN
- PCIE_TBT_X_R2D_C_P<3> — C21 — PCIE8_TXP/SATA1A_TXP

AirPort
- PCIE_AP_D2R_N — E22 — PCIE9_RXN
- PCIE_AP_D2R_P — E23 — PCIE9_RXP
- PCIE_AP_R2D_C_N — B23 — PCIE9_TXN
- PCIE_AP_R2D_C_P — A23 — PCIE9_TXP

ETHERNET AND SD CARD
- PCIE_ENET_D2R_N — F25 — PCIE10_RXN
- PCIE_ENET_D2R_P — E25 — PCIE10_RXP
- PCIE_ENET_R2D_C_N — D23 — PCIE10_TXN
- PCIE_ENET_R2D_C_P — C23 — PCIE10_TXP

PLACE_NEAR=U0500.F5:12.7mm
R1504 100 1% 1/20W MF 201
- PCH_PCIE_RCOMP_N — F5 — PCIE_RCOMPN
- PCH_PCIE_RCOMP_P — E5 — PCIE_RCOMPP

- XDP_CPU_PRDY_L — D56 — PROC_PRDY*
- XDP_CPU_PREQ_L — D61 — PROC_PREQ*
- SMC_RUNTIME_SCI_L — BB11 — GPP_A7/PIRQA*

Thunderbolt T lane 0
- NC_PCIE_TBT_T_D2R_N<0> — E28 — PCIE11_RXN/SATA1B_RXN
- NC_PCIE_TBT_T_D2R_P<0> — E27 — PCIE11_RXP/SATA1B_RXP
- NC_PCIE_TBT_T_R2D_N<0> — D24 — PCIE11_TXN/SATA1B_TXN
- NC_PCIE_TBT_T_R2D_P<0> — C24 — PCIE11_TXP/SATA1B_TXP

PRIMARY HDD (SATA)
- SATA_HDD_D2R_N — E30 — PCIE12_RXN/SATA2_RXN
- SATA_HDD_D2R_P — F30 — PCIE12_RXP/SATA2_RXP
- SATA_HDD_R2D_C_N — A25 — PCIE12_TXN/SATA2_TXN
- SATA_HDD_R2D_C_P — B25 — PCIE12_TXP/SATA2_TXP

PCIE/USB3/SATA

SSIC/USB3
- USB3_1_RXN — H8 — USB3_EXTD_D2R_N — EXT D (SS, DCI)
- USB3_1_RXP — G8 — USB3_EXTD_D2R_P
- USB3_1_TXN — C13 — USB3_EXTD_R2D_CF_N
- USB3_1_TXP — D13 — USB3_EXTD_R2D_CF_P
- USB3_2_RXN/SSIC_RXN — J6 — USB3_EXTB_D2R_N — EXT B (SS)
- USB3_2_RXP/SSIC_RXP — H6 — USB3_EXTB_D2R_P
- USB3_2_TXN/SSIC_TXN — B13 — USB3_EXTB_R2D_CF_N
- USB3_2_TXP/SSIC_TXP — A13 — USB3_EXTB_R2D_CF_P
- USB3_3_RXN — J10 — USB3_EXTA_D2R_N — EXT A (SS)
- USB3_3_RXP — H10 — USB3_EXTA_D2R_P
- USB3_3_TXN — B15 — USB3_EXTA_R2D_CF_N
- USB3_3_TXP — A15 — USB3_EXTA_R2D_CF_P
- USB3_4_RXN — E10 — USB3_EXTC_D2R_N — EXT C (SS)
- USB3_4_RXP — F10 — USB3_EXTC_D2R_P
- USB3_4_TXN — C15 — USB3_EXTC_R2D_CF_N
- USB3_4_TXP — D15 — USB3_EXTC_R2D_CF_P

USB2
- USB2N_1 — AB9 — USB_EXTA_N — EXT A (LS/FS/HS)
- USB2P_1 — AB10 — USB_EXTA_P
- USB2N_2 — AD6 — USB_EXTB_N — EXT B (LS/FS/HS)
- USB2P_2 — AD7 — USB_EXTB_P
- USB2N_3 — AH3 — USB_CAMERA_N — CAMERA (VI MICRO)
- USB2P_3 — AJ3 — USB_CAMERA_P
- USB2N_4 — AD9 — TP_USB_TESTERN
- USB2P_4 — AD10 — TP_USB_TESTERP
- USB2N_5 — AJ1 — USB_EXTC_N — EXT C (LS/FS/HS)
- USB2P_5 — AJ2 — USB_EXTC_P
- USB2N_6 — AF6 — USB_EXTD_N — EXT D (LS/FS/HS)
- USB2P_6 — AF7 — USB_EXTD_P
- USB2N_7 — AH1 — USBC_EXTB_N
- USB2P_7 — AH2 — USBC_EXTB_P
- USB2N_8 — AF8 — NC_USB2_08N (NO_TEST=1)
- USB2P_8 — AF9 — NC_USB2_08P (NO_TEST=1)
- USB2N_9 — AG1 — USB_BT_N — BLUETOOTH (X238D)
- USB2P_9 — AG2 — USB_BT_P
- USB2N_10 — AH7 — USBC_EXTA_N
- USB2P_10 — AH8 — USBC_EXTA_P
- USB2_COMP — AB6 — PCH_USB2_COMP
- USB2_ID — AG3
- USB2_VBUSSENSE — AG4 — PCH_USB2_VBUSSENSE

GROUNDED PER SKYLAKE MOW 2015WW10.

R1501 113 1% 1/20W MF 201 — PLACE_NEAR=U0500.AB6:12.7MM

GPP_E3/CPU_GP0 — A6 — XDP_PCH_OBSFN_C1
GPP_E4/DEVSLP0 — J1 — XDP_JTAG_ISP_TCK
GPP_E5/DEVSLP1 — J2 — XDP_JTAG_ISP_TDI
GPP_E6/DEVSLP2 — J3 — XDP_PCH_OBSDATA_A2

R1503 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.AG4:12.7MM

GPP_D22/SPI1_IO3 — V2 — SPKR_ID0
GPP_D23/I2S_MCLK — J5 — XDP_PCH_OBSDATA_D0
GPP_E0/SATAXPCIE0/SATAGP0 — H2 — XDP_PCH_OBSDATA_D1
GPP_D18/DMIC_DATA1 — C8 — XDP_PCH_OBSDATA_C1
GPP_D19/DMIC_CLK0 — H5 — XDP_PCH_OBSDATA_C2
GPP_D20/DMIC_DATA0 — D7 — XDP_PCH_OBSDATA_C3
GPP_E2/SATAXPCIE2/SATAGP2 — G4 — XDP_PCH_OBSDATA_D3

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20
CLOCK SIGNALS

- PCIE_CLK100M_SSD_N — D42 — CLKOUT_PCIE_N0
- PCIE_CLK100M_SSD_P — C42 — CLKOUT_PCIE_P0
- SSD_CLKREQ_L — AR10 — GPP_B5/SRCCLKREQ0*
- PCIE_CLK100M_TBT_X_N — B42 — CLKOUT_PCIE_N1
- PCIE_CLK100M_TBT_X_P — A42 — CLKOUT_PCIE_P1
- TBT_X_CLKREQ_L — AT7 — GPP_B6/SRCCLKREQ1*
- TP_PCIE_CLK100M2N — D41 — CLKOUT_PCIE_N2
- TP_PCIE_CLK100M2P — C41 — CLKOUT_PCIE_P2
- TBT_T_CLKREQ2_L — AT8 — GPP_B7/SRCCLKREQ2*
- PCIE_CLK100M_AP_N — D40 — CLKOUT_PCIE_N3
- PCIE_CLK100M_AP_P — C40 — CLKOUT_PCIE_P3
- AP_CLKREQ_L — AT10 — GPP_B8/SRCCLKREQ3*
- PCIE_CLK100M_ENET_N — B40 — CLKOUT_PCIE_N4
- PCIE_CLK100M_ENET_P — A40 — CLKOUT_PCIE_P4
- ENETSD_CLKREQ_L — AU8 — GPP_B9/SRCCLKREQ4*
- TP_PCIE_CLK100M5N — E40 — CLKOUT_PCIE_N5
- TP_PCIE_CLK100M5P — E38 — CLKOUT_PCIE_P5
- TP_PCH_CLKREQ5_L — AU7 — GPP_B10/SRCCLKREQ5*

- CLKOUT_ITPXDP_N — F43 — ITPXDP_CLK100M_N
- CLKOUT_ITPXDP_P — E43 — ITPXDP_CLK100M_P
- GPD8/SUSCLK — BA17 — PM_CLK32K_SUSCLK_R
- XTAL24_IN — E37 — PCH_CLK24M_XTALIN
- XTAL24_OUT — E35 — PCH_CLK24M_XTALOUT
- XCLK_BIASREF — E42 — PCH_DIFFCLK_BIASREF
- RTCX1 — AM18 — PCH_CLK32K_RTCX1
- RTCX2 — AM20 — PCH_CLK32K_RTCX2
- SRTCRST* — AN18 — PCH_SRTCRST_L
- RTCRST* — AM16

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PLACE_NEAR=U0500.E42:2.54mm
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=PP3V_G3_PCH_VCCRTC
R1530 20K 1% 1/20W MF 201
R1531 20K 1% 1/20W MF 201
RTC_RESET_L

C1530 1UF 20% 6.3V X6S-CERM 0201
C1531 1UF 20% 6.3V X6S-CERM 0201

=PP3V3_SUS_PCH_VCCPGPPA
R1550 100K 5% 1/20W MF 201 — SMC_RUNTIME_SCI_L

=PP3V3_S0_PCH
- R1560 10K 5% 1/20W MF 201 — SSD_CLKREQ_L
- R1561 100K 5% 1/20W MF 201 — TBT_X_CLKREQ_L
- R1564 100K 5% 1/20W MF 201 — ENETSD_CLKREQ_L
- R1565 10K 5% 1/20W MF 201 — AP_CLKREQ_L

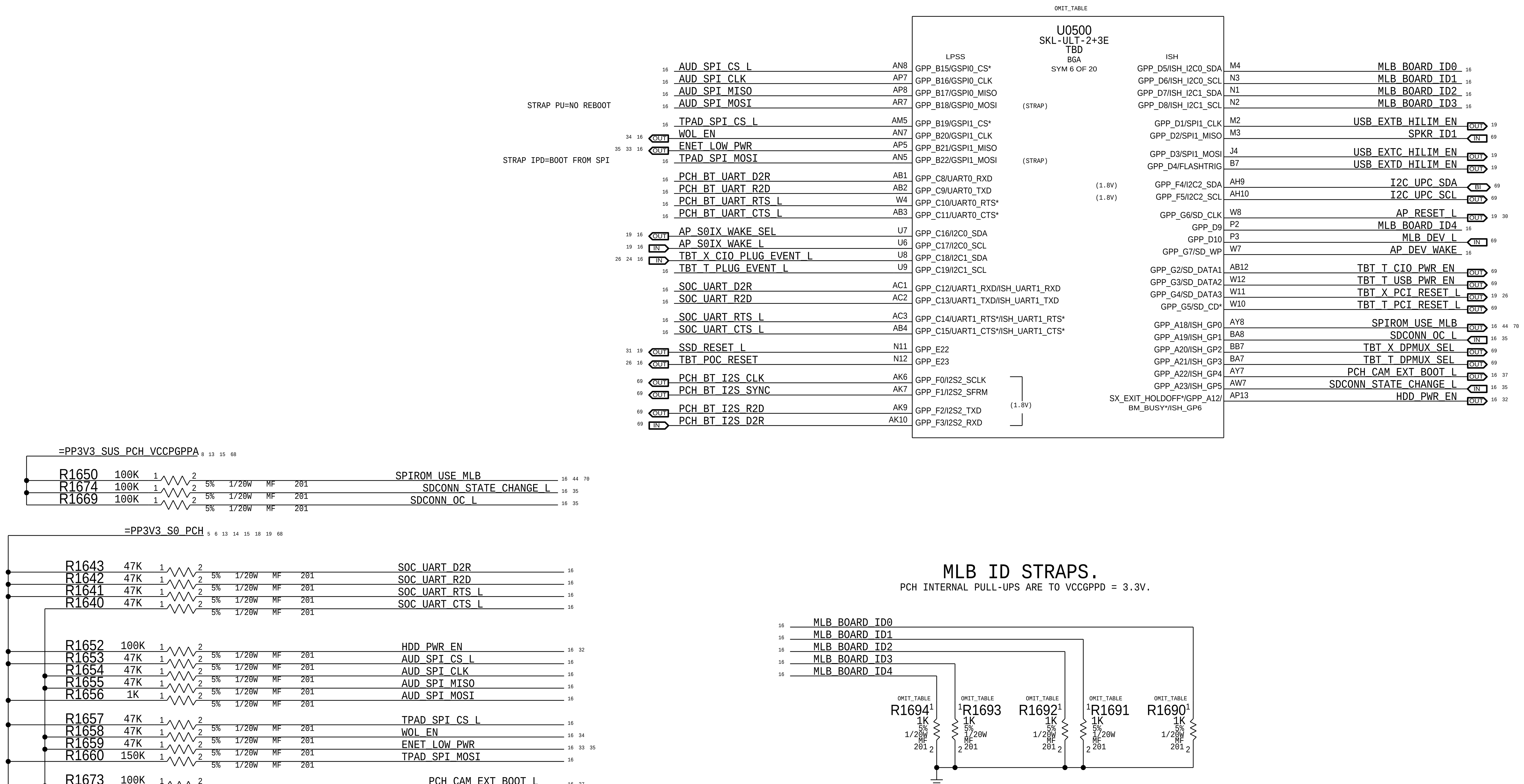
BOM_COST_GROUP=CPU & CHIPSET

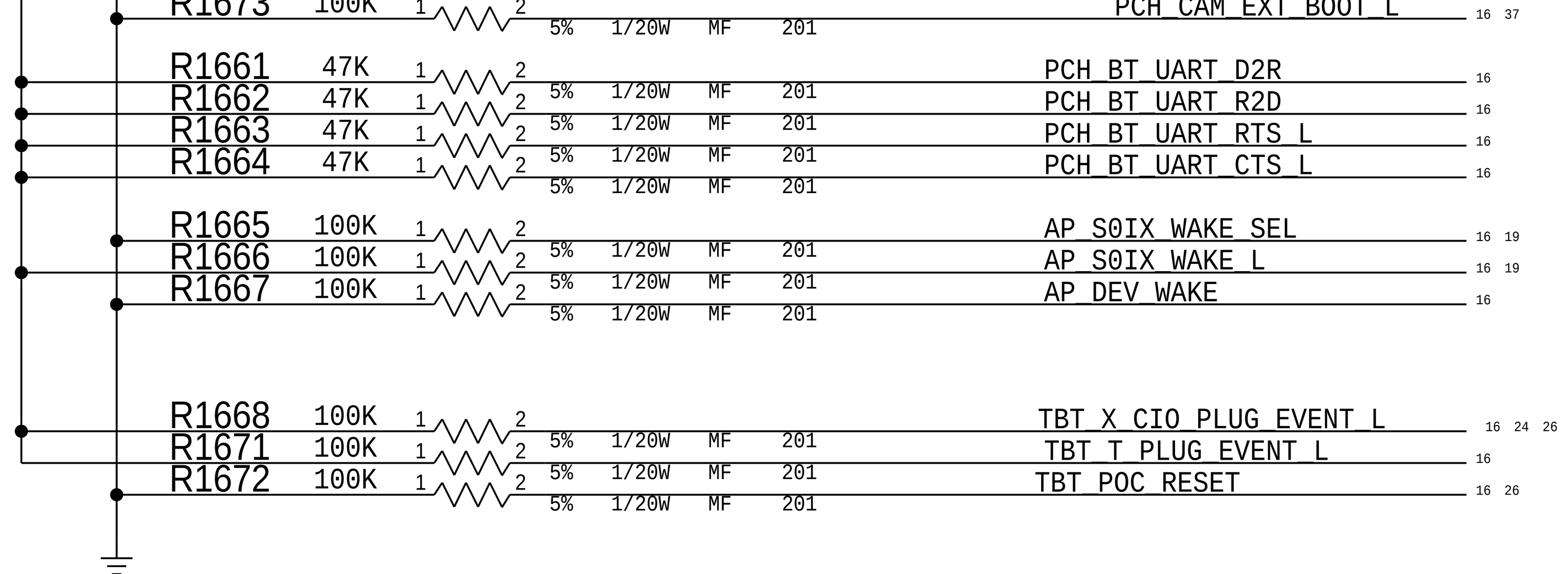
DESIGN: X502/MLB
LAST CHANGE: Tue Aug 18 12:55:20 2015
PAGE TITLE
PCH PCIE/USB/CLKS

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
BRANCH
PAGE 15 OF 105
SHEET 15 OF 70

ALL GPP_F* PINS ARE 1.8V ONLY!


OMIT_TABLE
U0500
SKL-ULT-2+3E
TBD
BGA
SYM 6 OF 20
LPSS
ISH
STRAP PU=NO REBOOT
STRAP IPD=BOOT FROM SPI
AUD_SPI_CS_L
AUD_SPI_CLK
AUD_SPI_MISO
AUD_SPI_MOSI
TPAD_SPI_CS_L
WOL_EN
ENET_LOW_PWR
TPAD_SPI_MOSI
PCH_BT_UART_D2R
PCH_BT_UART_R2D
PCH_BT_UART_RTS_L
PCH_BT_UART_CTS_L
AP_S0IX_WAKE_SEL
AP_S0IX_WAKE_L
TBT_X_CIO_PLUG_EVENT_L
TBT_T_PLUG_EVENT_L
SOC_UART_D2R
SOC_UART_R2D
SOC_UART_RTS_L
SOC_UART_CTS_L
SSD_RESET_L
TBT_POC_RESET
PCH_BT_I2S_CLK
PCH_BT_I2S_SYNC
PCH_BT_I2S_R2D
PCH_BT_I2S_D2R
GPP_B15/GSPI0_CS*
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B18/GSPI0_MOSI
GPP_B19/GSPI1_CS*
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI
(STRAP)
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS*
GPP_C11/UART0_CTS*
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
GPP_C18/I2C1_SDA
GPP_C19/I2C1_SCL
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS*/ISH_UART1_RTS*
GPP_C15/UART1_CTS*/ISH_UART1_CTS*
GPP_E22
GPP_E23
GPP_F0/I2S2_SCLK
GPP_F1/I2S2_SFRM
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
(1.8V)
GPP_D5/ISH_I2C0_SDA
GPP_D6/ISH_I2C0_SCL
GPP_D7/ISH_I2C1_SDA
GPP_D8/ISH_I2C1_SCL
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D4/FLASHTRIG
GPP_F4/I2C2_SDA
GPP_F5/I2C2_SCL
GPP_G6/SD_CLK
GPP_D9
GPP_D10
GPP_G7/SD_WP
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD*
GPP_A18/ISH_GP0
GPP_A19/ISH_GP1
GPP_A20/ISH_GP2
GPP_A21/ISH_GP3
GPP_A22/ISH_GP4
GPP_A23/ISH_GP5
SX_EXIT_HOLDOFF*/GPP_A12/BM_BUSY*/ISH_GP6
MLB_BOARD_ID0
MLB_BOARD_ID1
MLB_BOARD_ID2
MLB_BOARD_ID3
USB_EXTB_HILIM_EN
SPKR_ID1
USB_EXTC_HILIM_EN
USB_EXTD_HILIM_EN
I2C_UPC_SDA
I2C_UPC_SCL
AP_RESET_L
MLB_BOARD_ID4
MLB_DEV_L
AP_DEV_WAKE
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
TBT_X_PCI_RESET_L
TBT_T_PCI_RESET_L
SPIROM_USE_MLB
SDCONN_OC_L
TBT_X_DPMUX_SEL
TBT_T_DPMUX_SEL
PCH_CAM_EXT_BOOT_L
SDCONN_STATE_CHANGE_L
HDD_PWR_EN
=PP3V3_SUS_PCH_VCCPGPPA
R1650 100K
R1674 100K
R1669 100K
=PP3V3_S0_PCH
R1643 47K
R1642 47K
R1641 47K
R1640 47K
R1652 100K
R1653 47K
R1654 47K
R1655 47K
R1656 1K
R1657 47K
R1658 47K
R1659 47K
R1660 150K
R1673 100K
R1661 47K
R1662 47K
R1663 47K
R1664 47K
R1665 100K
R1666 100K
R1667 100K
R1668 100K
R1671 100K
R1672 100K
5% 1/20W MF 201
TBT_POC_RESET
MLB ID STRAPS.
PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.
OMIT_TABLE
R1694 1K
R1693 1K
R1692 1K
R1691 1K
R1690 1K
5% 1/20W MF 201



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE	BUILD
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>	POC
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>	PROTO 0
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>	PROTO 1
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>	EVT
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>	
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>	
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>	
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>	
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>	
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>	
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>	
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>	
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>	

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Wed Oct 28 12:50:22 2015

PAGE TITLE
PCH SPI/UART/GPIO

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D
REVISION 3.13.0
BRANCH

Primary Micro2-XDP

NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: This is not the standard XDP pinout, there is a horizontal mirroring for use with 921-0133 Adapter Flex to support chipset debug.

68 17 =PP1V0_S5_XDP

XDP_PIN1

R1831 1K 5% 1/10W MF-LF 402 XDP — NO_XNET_CONNECTION

CRITICAL

XDP_CONN J1800 DF40RC-60DP-0.4V M-ST-SM

998-2516

70 15 BI XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17> IN 6
70 15 IN XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16> IN 6
6 IN CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8> IN 6
6 IN CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9> IN 6
6 IN CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10> IN 6
70 6 IN CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11> IN 6
6 IN XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19> IN 6
6 IN XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18> IN 6
6 IN CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12> IN 6
6 IN CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13> IN 6
6 IN CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14> IN 6
6 IN CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15> IN 6
XDP_HOOK0	PWRGD/HOOK0	ITPCLK/HOOK4	ITPXDP_CLK100M_P IN 15
XDP_HOOK1	HOOK1	ITPCLK#/HOOK5	ITPXDP_CLK100M_N IN 15
	VCC_OBS_AB	VCC_OBS_CD	
XDP_CPU_HOOK2_R	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_HOOK3	HOOK3	DBR#/HOOK7	XDP_DBRESET_L OUT 18
	SDA	TDO	XDP_CPU_PCH_TDO
	SCL	TRSTn	XDP_CPU_PCH_TRST_L
	TCK1	TDI	XDP_CPU_PCH_TDI
	TCK0	TMS	XDP_CPU_PCH_TMS
		XDP_PRESENT#	

XDP_DBRESET_L (PM_SYSRST_L) PULLED UP ON CPU SUPPORT PAGE

68 44 =PP3V3_S5_ROM

R1801 2.2K 5% 1/20W MF 201

R1806 1K 5% 1/20W MF 201 XDP PLACE_NEAR=U0500.AY17:16.5MM

70 67 17 14 IN PM_RSMRST_PCH_L

42 14 OUT PM_PWRBTN_L — R1802 0 5% MF 1/20W 0201 XDP

44 13 OUT SPI_MOSI_R — R1826 1K 1% MF 1/20W 201 XDP

C1805 0.1UF 20% 10V CERM 402 XDP

45 17 BI =SMBUS_XDP_SDA

45 17 IN =SMBUS_XDP_SCL

R1828 0 XDP_PCH_TCK_R 5% 1/20W MF 0201

70 6 OUT XDP_PCH_TCK

70 6 OUT XDP_CPU_TCK

70 6 IN PCH_JTAGX — R1822 0 5% MF 1/20W 0201 XDP PLACE_NEAR=J1800.58:5MM

NOSTUFF R1866 51 5% 1/20W MF 201 PLACE_NEAR=U0500.B56:28MM

R1823 51 5% 1/20W MF 201 XDP PLACE_NEAR=U0500.B61:28.0MM

C1800 0.1UF 20% 10V CERM 402 XDP

C1801 0.1UF 20% 10V CERM 402 XDP

C1806 0.1UF 20% 10V CERM 402 XDP

R1825 1K 1% MF 1/20W 201 XDP — XDP_CPU_PRESENT_L — SPI_IO_R<2> IN 13 44

NOSTUFF R1839 1K 5% 1/20W MF 201

R1808 2.2K 5% 1/20W MF 201 =PP1V0_S5_XDP 17 68

R1807 0 5% MF 1/20W 0201 XDP — ITP_PMODE IN 6 70

=PP1V_S3_CPU_VCCSTG 68 10 8 6

C1898 0.1UF 20% 10V CERM 402 XDP

R1860 100 5% 1/20W MF 201 XDP U0500.A56:50.0MM

R1861 51 5% 1/20W MF 201 XDP U0500.D59:4MM

R1862 51 5% 1/20W MF 201 XDP U0500.C59:3.5MM

R1837 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.51:5MM — XDP_PCH_TDO IN 6 70

R1845 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.53:5MM — XDP_PCH_TRST_L OUT 6 70

R1844 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.55:5MM — XDP_PCH_TDI OUT 6 70

R1836 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.57:5MM — XDP_PCH_TMS IN 6 70

R1820 100 5% 1/20W MF 201 XDP U0500.A61:50.0MM

R1829 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.51:5MM — XDP_CPU_TDO IN 6 70

R1824 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.53:5MM — XDP_CPU_TRST_L OUT 6 70

R1843 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.55:5MM — XDP_CPU_TDI OUT 6 70

R1838 0 5% MF 1/20W 0201 PLACE_NEAR=U1800.57:5MM — XDP_CPU_TMS IN 6 70

NOTE: TDI and TMS are terminated in CPU.

PCH SIGNALS

19 15 BI	XDP_JTAG_ISP_TCK	OMIT	R1894	SHORT	XDP_PCH_OBSDATA_A0 17
19 15 BI	XDP_JTAG_ISP_TDI	OMIT	R1895	SHORT	XDP_PCH_OBSDATA_A1 17
5 BI	XDP_USB_EXTA_OC_L	OMIT	R1897	SHORT	XDP_PCH_OBSDATA_B1 17
40 IN	USB_EXTA_OC_L MAKE_BASE=TRUE				
5 BI	XDP_USB_EXTB_OC_L	OMIT	R1872	SHORT	XDP_PCH_OBSDATA_B2 17
40 IN	USB_EXTB_OC_L MAKE_BASE=TRUE				
5 BI	XDP_USB_EXTC_OC_L	OMIT	R1873	SHORT	XDP_PCH_OBSDATA_B3 17
41 IN	USB_EXTC_OC_L MAKE_BASE=TRUE				
5 BI	XDP_USB_EXTD_OC_L	OMIT	R1882	SHORT	XDP_PCH_OBSFN_C0 17
41 IN	USB_EXTD_OC_L MAKE_BASE=TRUE				

XDP SIGNALS

Secondary (PCH) Micro2-XDP

68 17 =PP1V0_S5_XDP

CRITICAL

XDP_CONN J1850 DF40RC-60DP-0.4V M-ST-SM

998-2516

NOTE: This is not the standard XDP pinout, there is a horizontal mirroring for use with 921-0133 Adapter Flex to support chipset debug.

	OBSFN_A0	OBSFN_C0	XDP_PCH_OBSFN_C0 17
	OBSFN_A1	OBSFN_C1	XDP_PCH_OBSFN_C1 IN 15
17 XDP_PCH_OBSDATA_A0	OBSDATA_A0	OBSDATA_C0	XDP_PCH_OBSDATA_C0 IN 13
17 XDP_PCH_OBSDATA_A1	OBSDATA_A1	OBSDATA_C1	XDP_PCH_OBSDATA_C1 IN 15
15 IN XDP_PCH_OBSDATA_A2	OBSDATA_A2	OBSDATA_C2	XDP_PCH_OBSDATA_C2 IN 15
5 IN XDP_PCH_OBSDATA_A3	OBSDATA_A3	OBSDATA_C3	XDP_PCH_OBSDATA_C3 IN 15
	OBSFN_B0	OBSFN_D0	
	OBSFN_B1	OBSFN_D1	
5 IN XDP_PCH_OBSDATA_B0	OBSDATA_B0	OBSDATA_D0	XDP_PCH_OBSDATA_D0 IN 15
17 XDP_PCH_OBSDATA_B1	OBSDATA_B1	OBSDATA_D1	XDP_PCH_OBSDATA_D1 IN 15
17 XDP_PCH_OBSDATA_B2	OBSDATA_B2	OBSDATA_D2	XDP_PCH_OBSDATA_D2 IN 5
17 XDP_PCH_OBSDATA_B3	OBSDATA_B3	OBSDATA_D3	XDP_PCH_OBSDATA_D3 IN 15
70 67 17 14 IN PM_RSMRST_PCH_L — R1881 1K XDP PLACE_NEAR=U0500.AY17:16.5MM — XDP_PCH_RSMRST_L	PWRGD/HOOK0	ITPCLK/HOOK4	
	HOOK1	ITPCLK#/HOOK5	
	VCC_OBS_AB	VCC_OBS_CD	
	HOOK2	RESET#/HOOK6	
	HOOK3	DBR#/HOOK7	
45 17 BI =SMBUS_XDP_SDA	SDA		
45 17 IN =SMBUS_XDP_SCL	SCL		
		XDP_PRESENT#	

C1880 0.1UF 20% 10V CERM 402 XDP

C1881 0.1UF 20% 10V CERM 402 XDP

PCH/XDP Signal Isolation Notes:

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

BOM_COST_GROUP=DEBUG

SYNC_MASTER=AARON_MLB SYNC_DATE=06/14/2010

PAGE TITLE: CPU & CHIPSET: XDP

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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BRANCH

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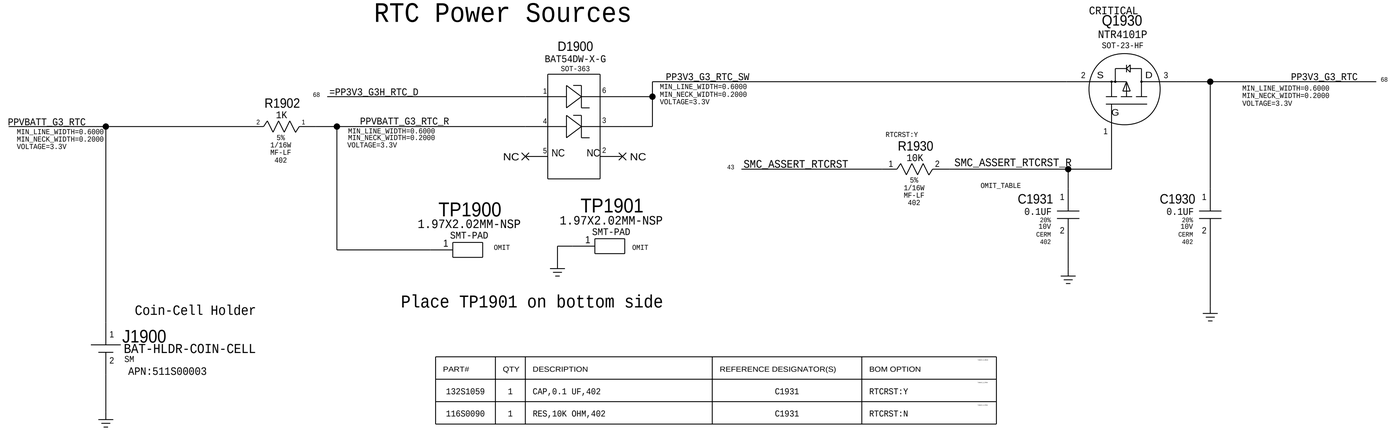
RTC Power Sources



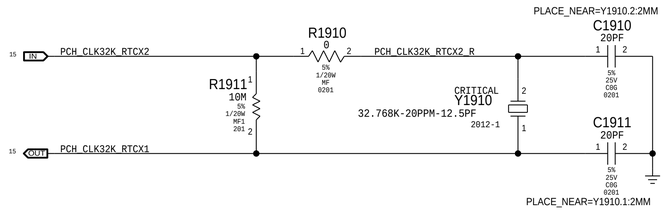
Place TP1901 on bottom side

Coin-Cell Holder

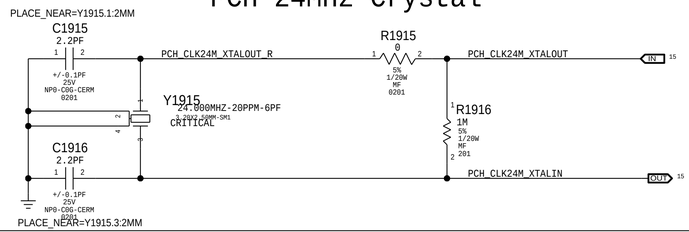
J1900
BAT-HLDR-COIN-CELL
SM
APN:511S00003

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K OHM,402	C1931	RTCRST:N

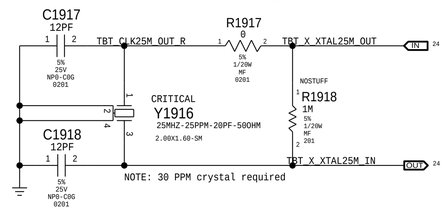
PCH RTC Crystal



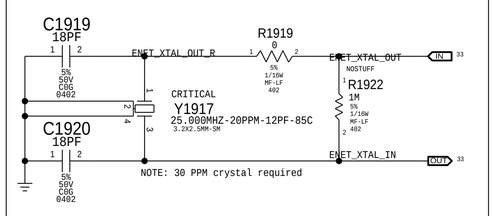
PCH 24MHz Crystal



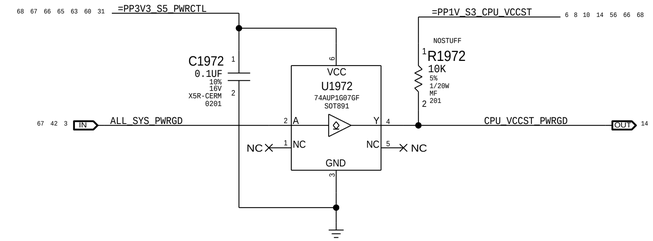
TBT 25MHz Crystal



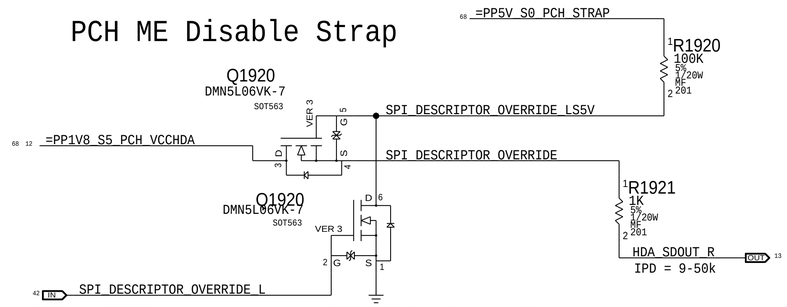
Ethernet 25MHz Crystal



ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter

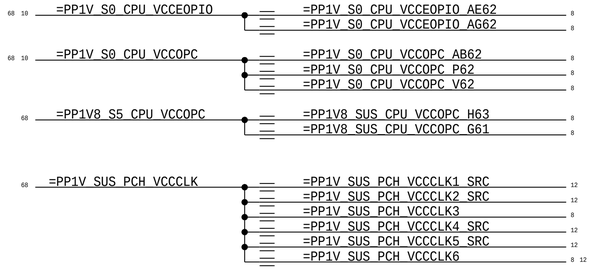


PCH ME Disable Strap

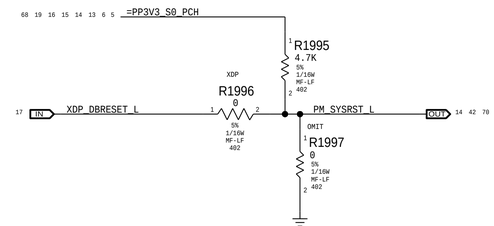


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

RAIL DIS-AMBIGUATION



PCH Reset Button



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AARON_MLB SYNC_DATE=04/06/2010

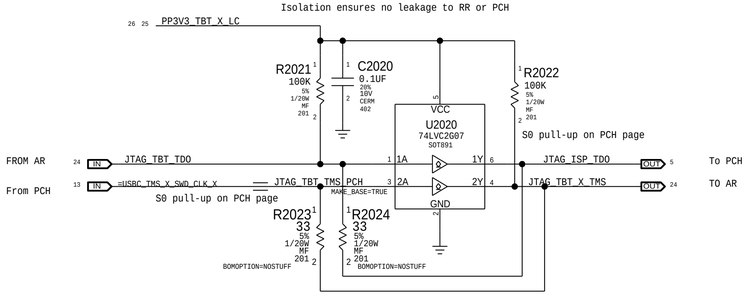
PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 19 OF 105
SHEET: 18 OF 70

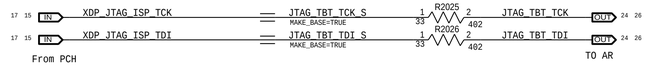
Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH



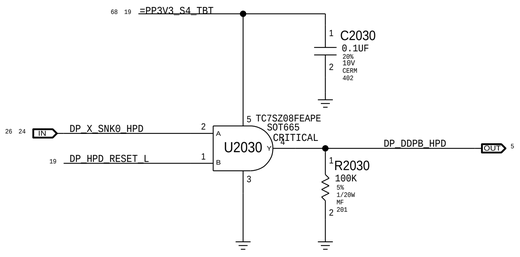
NOTE: Solution shown is for WPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

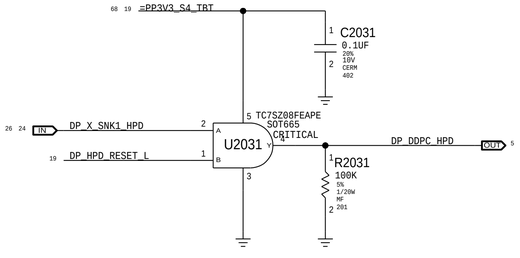
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.



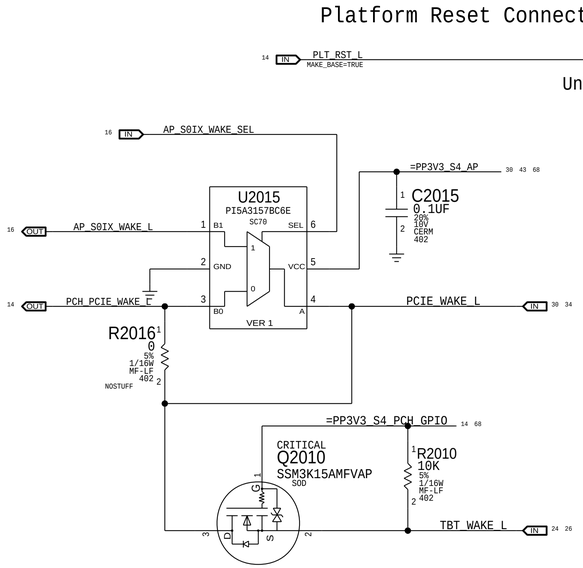
Falcon Ridge HPD Isolation

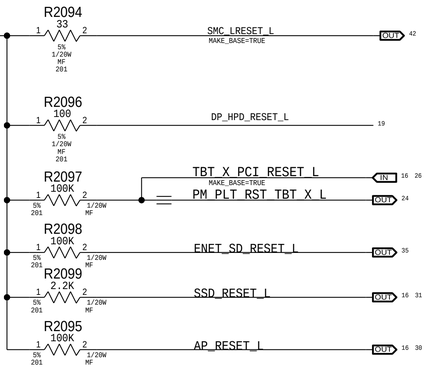
NOTE: PLT_RESET_L used as the other input to the AND gate so that HPD is only driven high to the PCH in S0.

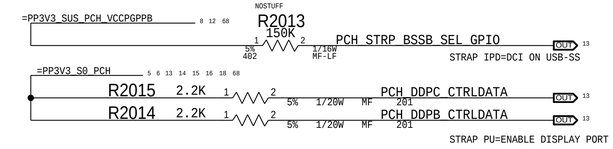


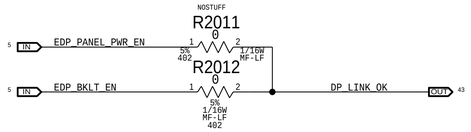


Platform Reset Connections



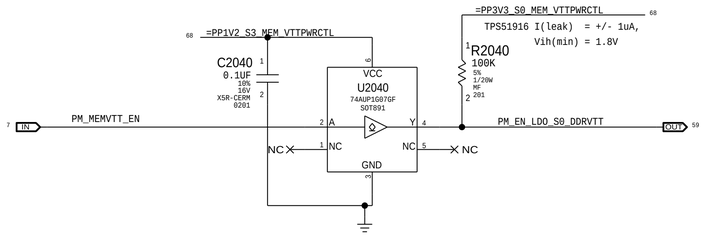


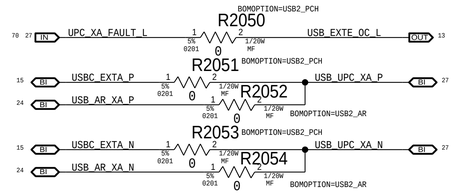


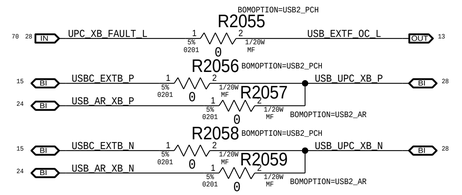


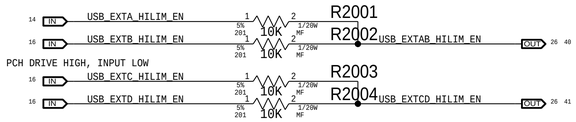
Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).









BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Project Chipset Support

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
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PAGE 20 OF 105
SHEET 19 OF 70

Memory Bit/Byte Swizzle

MAKE_BASE

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MAKE_BASE

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SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: DDR4 SO-DIMM SIGNAL ALIASES

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 21 OF 105

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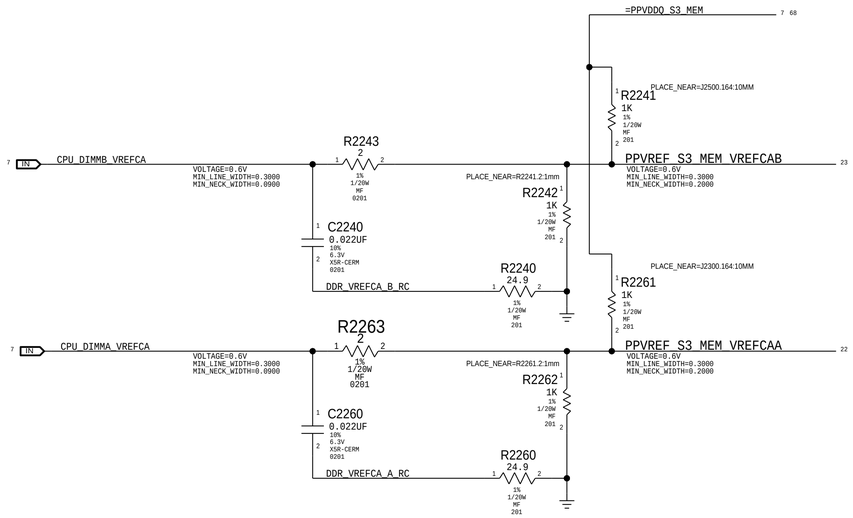
VRef Dividers



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PAGE TITLE

DDR4 VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

REVISION 3.13.0

BRANCH

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Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

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C2350 10UF 20% 6.3V CERM X5R 0603-1
C2351 1UF 10% 10V CERM X5R 402
C2352 1UF 10% 10V CERM X5R 402
C2353 1UF 10% 10V CERM X5R 402
C2354 12PF 5% 25V CERM 0201

=PPDDRVPP_S3_MEM_A

C2320 10UF 20% 6.3V CERM X5R 0402-1
C2321 1UF 10% 10V CERM X5R 402
C2322 12PF 5% 25V CERM 0201

BYPASS=J2300.257::2MM

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

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C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402
C2318 12PF 5% 25V CERM 0201
C2319 12PF 5% 25V CERM 0201

C2300 10UF 20% 6.3V CERM X5R 603
C2301 10UF 20% 6.3V CERM X5R 603
C2302 10UF 20% 6.3V CERM X5R 0402-1
C2303 10UF 20% 6.3V CERM X5R 0402-1
C2304 10UF 20% 6.3V CERM X5R 0402-1
C2305 10UF 20% 6.3V CERM X5R 0402-1
C2306 10UF 20% 6.3V CERM X5R 0402-1
C2307 10UF 20% 6.3V CERM X5R 0402-1
C2360 270UF-0.006OHM 20% 2V TANT CASE-D2

PPVREF_S3_MEM_VREFCAA

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402

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R2341 10K 5% 1/16W MF-LF 402
R2342 10K 5% 1/16W MF-LF 402
C2340 2.2UF 20% 6.3V CERM 402-LF
C2341 0.1UF 20% 10V CERM 402

P/N: 998-05061

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 1 OF 3

CRITICAL

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NC	162	C0/CS2*/NC	
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NC	100	CB6/NC	
NC	87	CB5/NC	
NC	88	CB4/NC	
NC	105	CB3/NC	
NC	101	CB2/NC	
NC	91	CB1/NC	
NC	92	CB0/NC	
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MEM_A_ALERT_L	116	ALERT*	

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DQ41	194	=MEM_A_DQ<41>	
DQ40	195	=MEM_A_DQ<40>	
DQ39	182	=MEM_A_DQ<39>	
DQ38	183	=MEM_A_DQ<38>	
DQ37	169	=MEM_A_DQ<37>	
DQ36	170	=MEM_A_DQ<36>	
DQ35	186	=MEM_A_DQ<35>	
DQ34	187	=MEM_A_DQ<34>	
DQ33	173	=MEM_A_DQ<33>	
DQ32	174	=MEM_A_DQ<32>	
DQ31	80	=MEM_A_DQ<31>	
DQ30	79	=MEM_A_DQ<30>	
DQ29	67	=MEM_A_DQ<29>	
DQ28	66	=MEM_A_DQ<28>	
DQ27	84	=MEM_A_DQ<27>	
DQ26	83	=MEM_A_DQ<26>	
DQ25	71	=MEM_A_DQ<25>	
DQ24	70	=MEM_A_DQ<24>	
DQ23	59	=MEM_A_DQ<23>	
DQ22	58	=MEM_A_DQ<22>	
DQ21	45	=MEM_A_DQ<21>	
DQ20	46	=MEM_A_DQ<20>	
DQ19	63	=MEM_A_DQ<19>	
DQ18	62	=MEM_A_DQ<18>	
DQ17	49	=MEM_A_DQ<17>	
DQ16	50	=MEM_A_DQ<16>	
DQ15	37	=MEM_A_DQ<15>	
DQ14	38	=MEM_A_DQ<14>	
DQ13	25	=MEM_A_DQ<13>	
DQ12	24	=MEM_A_DQ<12>	
DQ11	42	=MEM_A_DQ<11>	
DQ10	41	=MEM_A_DQ<10>	
DQ9	29	=MEM_A_DQ<9>	
DQ8	28	=MEM_A_DQ<8>	
DQ7	17	=MEM_A_DQ<7>	
DQ6	16	=MEM_A_DQ<6>	
DQ5	3	=MEM_A_DQ<5>	
DQ4	4	=MEM_A_DQ<4>	
DQ3	21	=MEM_A_DQ<3>	
DQ2	20	=MEM_A_DQ<2>	
DQ1	7	=MEM_A_DQ<1>	
DQ0	8	=MEM_A_DQ<0>	
EVENT*/NF	134	MEM_EVENT_L	

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 2 OF 3

DM8*/DBI*/NC	96	=PP_VDDQ_S3_MEM_A
DM7*/DBI7*	241	
DM6*/DBI6*	220	
DM5*/DBI5*	199	
DM4*/DBI4*	178	
DM3*/DBI3*	75	
DM2*/DBI2*	54	
DM1*/DBI*	33	
DM0*/DBI0*	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	=MEM_A_DQS_P<7>
DQS7_C	240	=MEM_A_DQS_N<7>
DQS6_T	221	=MEM_A_DQS_P<6>
DQS6_C	219	=MEM_A_DQS_N<6>
DQS5_T	200	=MEM_A_DQS_P<5>
DQS5_C	198	=MEM_A_DQS_N<5>
DQS4_T	179	=MEM_A_DQS_P<4>
DQS4_C	177	=MEM_A_DQS_N<4>
DQS3_T	76	=MEM_A_DQS_P<3>
DQS3_C	74	=MEM_A_DQS_N<3>
DQS2_T	55	=MEM_A_DQS_P<2>
DQS2_C	53	=MEM_A_DQS_N<2>
DQS1_T	34	=MEM_A_DQS_P<1>
DQS1_C	32	=MEM_A_DQS_N<1>
DQS0_T	13	=MEM_A_DQS_P<0>
DQS0_C	11	=MEM_A_DQS_N<0>

=PPVDDQ_S3_MEM_A

J2300
ASAA827-EASB0-7H
F-RT-SM
SYM 3 OF 3

251	VSS	VDD	163
247	VSS	VDD	159
243	VSS	VDD	153
239	VSS	VDD	147
235	VSS	VDD	141
231	VSS	VDD	135
227	VSS	VDD	129
223	VSS	VDD	123
217	VSS	VDD	117
213	VSS	VDD	111
209	VSS	VDD	112
205	VSS	VDD	118
201	VSS	VDD	124
197	VSS	VDD	130
193	VSS	VDD	136
189	VSS	VDD	142
185	VSS	VDD	148
181	VSS	VDD	154
175	VSS	VDD	160
171	VSS		
167	VSS	VTT	258
107	VSS		
103	VSS	IO261	261
99	VSS	IO262	262
93	VSS		
89	VSS		
85	VSS		
81	VSS		
77	VSS	VSS	60
73	VSS	VSS	64
69	VSS	VSS	68
65	VSS	VSS	72
61	VSS	VSS	78
57	VSS	VSS	82
51	VSS	VSS	86
47	VSS	VSS	90
43	VSS	VSS	94
39	VSS	VSS	98
35	VSS	VSS	102
31	VSS	VSS	106
27	VSS	VSS	168
23	VSS	VSS	172
19	VSS	VSS	176
15	VSS	VSS	180
9	VSS	VSS	184
5	VSS	VSS	188
1	VSS	VSS	192
2	VSS	VSS	196
6	VSS	VSS	202
10	VSS	VSS	206
14	VSS	VSS	210
18	VSS	VSS	214
22	VSS	VSS	218
26	VSS	VSS	222
30	VSS	VSS	226
36	VSS	VSS	230
40	VSS	VSS	234
44	VSS	VSS	238
48	VSS	VSS	244
52	VSS	VSS	248
56	VSS	VSS	252

BOM_COST_GROUP=DRAM

PAGE TITLE: DRAM: SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER: 051-01543
SIZE: D
REVISION: 3.13.0
BRANCH:
PAGE: 23 OF 105
SHEET: 22 OF 70

Page Notes

Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP3V3_S0_MEM_B_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA

BOM options provided by this page:
(NONE)

=PPDDRVTT_S0_MEM_B

C2550 10UF 20% 6.3V X5R 0603-1
C2551 1UF 10% 10V X5R 402
C2552 1UF 10% 10V X5R 402
C2553 1UF 10% 10V X5R 402
C2554 12PF 5% 25V CERM 0201

=PPDDRVPP_S3_MEM_B

BYPASS=J2500.257::2MM

C2520 10UF 20% 6.3V CERM-X5R 0402-1
C2521 1UF 10% 10V X5R 402
C2522 12PF 5% 25V CERM 0201

DDR4 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402
C2514 0.1UF 20% 10V CERM 402
C2515 0.1UF 20% 10V CERM 402
C2516 0.1UF 20% 10V CERM 402
C2517 0.1UF 20% 10V CERM 402
C2518 12PF 5% 25V CERM 0201
C2519 12PF 5% 25V CERM 0201

C2500 10UF 20% 6.3V CERM-X5R 0402-1
C2501 10UF 20% 6.3V CERM 603
C2502 10UF 20% 6.3V CERM-X5R 0402-1
C2503 10UF 20% 6.3V CERM-X5R 0402-1
C2504 10UF 20% 6.3V CERM-X5R 0402-1
C2505 10UF 20% 6.3V CERM-X5R 0402-1
C2506 10UF 20% 6.3V CERM-X5R 0402-1
C2507 10UF 20% 6.3V CERM-X5R 0402-1
C2560 270UF-0.0060HM 20% 2V TANT CASE-D2

PPVREF_S3_MEM_VREFCAB

BYPASS=J2500.164::2MM

C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 20% 10V CERM 402

R2541 10K 5% 1/16W ME-LF 402
=PP3V3_S0_MEM_B_SPD
MEM_DIMMB_SA<2>
MEM_DIMMB_SA<1>
MEM_DIMMB_SA<0>
R2540 10K 5% 1/16W ME-LF 402
R2542 10K 5% 1/16W ME-LF 402
C2540 2.2UF 20% 6.3V CERM 402-LF
C2541 0.1UF 20% 10V CERM 402

P/N: 998-05060

J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 1 OF 3
CRITICAL

MEM_B_A<16>	152	RAS*/A16	
MEM_B_A<15>	156	CAS*/A15	
MEM_B_A<14>	151	WE*/A14	
MEM_B_A<13>	158	A13	
MEM_B_A<12>	119	A12	
MEM_B_A<11>	120	A11	
MEM_B_A<10>	146	A10/AP	
MEM_B_A<9>	121	A9	
MEM_B_A<8>	125	A8	
MEM_B_A<7>	122	A7	
MEM_B_A<6>	127	A6	
MEM_B_A<5>	126	A5	
MEM_B_A<4>	128	A4	
MEM_B_A<3>	131	A3	
MEM_B_A<2>	132	A2	
MEM_B_A<1>	133	A1	
MEM_B_A<0>	144	A0	
MEM_B_BA<1>	145	BA1	
MEM_B_BA<0>	150	BA0	
MEM_B_CLK_P<1>	138	CK1_T/NF	
MEM_B_CLK_N<1>	140	CK1_C/NF	
MEM_B_CLK_P<0>	137	CK0_T	
MEM_B_CLK_N<0>	139	CK0_C	
NC	165	C1/CS3*/NC	
NC	162	C0/CS2*/NC	
MEM_B_CS_L<1>	157	CS1*/NC	
MEM_B_CS_L<0>	149	CS0*	
MEM_B_CKE<1>	110	CKE1/NC	
MEM_B_CKE<0>	109	CKE0	
MEM_B_BG<1>	113	BG1	
MEM_B_BG<0>	115	BG0	
MEM_B_ODT<1>	161	ODT1/NC	
MEM_B_ODT<0>	155	ODT0	
MEM_B_PARITY	143	PARITY	
NC	104	CB7/NC	
NC	100	CB6/NC	
NC	87	CB5/NC	
NC	88	CB4/NC	
NC	105	CB3/NC	
NC	101	CB2/NC	
NC	91	CB1/NC	
NC	92	CB0/NC	
MEM_RESET_L	108	RESET*	
=PP3V3_S0_MEM_B_SPD	255	VDDSPD	
MEM_DIMMB_SA<2>	166	SA2	
MEM_DIMMB_SA<1>	260	SA1	
MEM_DIMMB_SA<0>	256	SA0	
=I2C_SODIMMB_SDA	254	SDA	
=I2C_SODIMMB_SCL	253	SCL	
PPVREF_S3_MEM_VREFCAB	164	VREFCA	
=PPDDRVPP_S3_MEM_B	257	VPP	
	259	VPP	
MEM_B_ACT_L	114	ACT*	
MEM_B_ALERT_L	116	ALERT*	

J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 2 OF 3

DM8*/BDI*/NC	96	=PPVDDQ_S3_MEM_B
DM7*/DBI7*	241	
DM6*/DBI6*	220	
DM5*/DBI5*	199	
DM4*/DBI4*	178	
DM3*/DBI3*	75	
DM2*/DBI2*	54	
DM1*/DBI*	33	
DM0*/DBI0*	12	
DQS8_T	97	NC
DQS8_C	95	NC
DQS7_T	242	=MEM_B_DQS_P<7>
DQS7_C	240	=MEM_B_DQS_N<7>
DQS6_T	221	=MEM_B_DQS_P<6>
DQS6_C	219	=MEM_B_DQS_N<6>
DQS5_T	200	=MEM_B_DQS_P<5>
DQS5_C	198	=MEM_B_DQS_N<5>
DQS4_T	179	=MEM_B_DQS_P<4>
DQS4_C	177	=MEM_B_DQS_N<4>
DQS3_T	76	=MEM_B_DQS_P<3>
DQS3_C	74	=MEM_B_DQS_N<3>
DQS2_T	55	=MEM_B_DQS_P<2>
DQS2_C	53	=MEM_B_DQS_N<2>
DQS1_T	34	=MEM_B_DQS_P<1>
DQS1_C	32	=MEM_B_DQS_N<1>
DQS0_T	13	=MEM_B_DQS_P<0>
DQS0_C	11	=MEM_B_DQS_N<0>

DQ63	246	=MEM_B_DQ<63>
DQ62	245	=MEM_B_DQ<62>
DQ61	233	=MEM_B_DQ<61>
DQ60	232	=MEM_B_DQ<60>
DQ59	250	=MEM_B_DQ<59>
DQ58	249	=MEM_B_DQ<58>
DQ57	236	=MEM_B_DQ<57>
DQ56	237	=MEM_B_DQ<56>
DQ55	225	=MEM_B_DQ<55>
DQ54	224	=MEM_B_DQ<54>
DQ53	212	=MEM_B_DQ<53>
DQ52	211	=MEM_B_DQ<52>
DQ51	229	=MEM_B_DQ<51>
DQ50	228	=MEM_B_DQ<50>
DQ49	215	=MEM_B_DQ<49>
DQ48	216	=MEM_B_DQ<48>
DQ47	204	=MEM_B_DQ<47>
DQ46	203	=MEM_B_DQ<46>
DQ45	190	=MEM_B_DQ<45>
DQ44	191	=MEM_B_DQ<44>
DQ43	208	=MEM_B_DQ<43>
DQ42	207	=MEM_B_DQ<42>
DQ41	194	=MEM_B_DQ<41>
DQ40	195	=MEM_B_DQ<40>
DQ39	182	=MEM_B_DQ<39>
DQ38	183	=MEM_B_DQ<38>
DQ37	169	=MEM_B_DQ<37>
DQ36	170	=MEM_B_DQ<36>
DQ35	186	=MEM_B_DQ<35>
DQ34	187	=MEM_B_DQ<34>
DQ33	173	=MEM_B_DQ<33>
DQ32	174	=MEM_B_DQ<32>
DQ31	80	=MEM_B_DQ<31>
DQ30	79	=MEM_B_DQ<30>
DQ29	67	=MEM_B_DQ<29>
DQ28	66	=MEM_B_DQ<28>
DQ27	84	=MEM_B_DQ<27>
DQ26	83	=MEM_B_DQ<26>
DQ25	71	=MEM_B_DQ<25>
DQ24	70	=MEM_B_DQ<24>
DQ23	59	=MEM_B_DQ<23>
DQ22	58	=MEM_B_DQ<22>
DQ21	45	=MEM_B_DQ<21>
DQ20	46	=MEM_B_DQ<20>
DQ19	63	=MEM_B_DQ<19>
DQ18	62	=MEM_B_DQ<18>
DQ17	49	=MEM_B_DQ<17>
DQ16	50	=MEM_B_DQ<16>
DQ15	37	=MEM_B_DQ<15>
DQ14	38	=MEM_B_DQ<14>
DQ13	25	=MEM_B_DQ<13>
DQ12	24	=MEM_B_DQ<12>
DQ11	42	=MEM_B_DQ<11>
DQ10	41	=MEM_B_DQ<10>
DQ9	29	=MEM_B_DQ<9>
DQ8	28	=MEM_B_DQ<8>
DQ7	17	=MEM_B_DQ<7>
DQ6	16	=MEM_B_DQ<6>
DQ5	3	=MEM_B_DQ<5>
DQ4	4	=MEM_B_DQ<4>
DQ3	21	=MEM_B_DQ<3>
DQ2	20	=MEM_B_DQ<2>
DQ1	7	=MEM_B_DQ<1>
DQ0	8	=MEM_B_DQ<0>
EVENT*/NF	134	MEM_EVENT_L

J2500
AS0A827-H2SB-7H
F-RT-SM
SYM 3 OF 3

=PPVDDQ_S3_MEM_B

VSS	251	
VSS	247	
VSS	243	
VSS	239	
VSS	235	
VSS	231	
VSS	227	
VSS	223	
VSS	217	
VSS	213	
VSS	209	
VSS	205	
VSS	201	
VSS	197	
VSS	193	
VSS	189	
VSS	185	
VSS	181	
VSS	175	
VSS	171	
VSS	167	
VSS	107	
VSS	103	
VSS	99	
VSS	93	
VSS	89	
VSS	85	
VSS	81	
VSS	77	
VSS	73	
VSS	69	
VSS	65	
VSS	61	
VSS	57	
VSS	51	
VSS	47	
VSS	43	
VSS	39	
VSS	35	
VSS	31	
VSS	27	
VSS	23	
VSS	19	
VSS	15	
VSS	9	
VSS	5	
VSS	1	
VSS	2	
VSS	6	
VSS	10	
VSS	14	
VSS	18	
VSS	22	
VSS	26	
VSS	30	
VSS	36	
VSS	40	
VSS	44	
VSS	48	
VSS	52	
VSS	56	
VDD	163	
VDD	159	
VDD	153	
VDD	147	
VDD	141	
VDD	135	
VDD	129	
VDD	123	
VDD	117	
VDD	111	
VDD	112	
VDD	118	
VDD	124	
VDD	130	
VDD	136	
VDD	142	
VDD	148	
VDD	154	
VDD	160	
VTT	258	=PPDDRVTT_S0_MEM_B
IO261	261	
IO262	262	
VSS	60	
VSS	64	
VSS	68	
VSS	72	
VSS	78	
VSS	82	
VSS	86	
VSS	90	
VSS	94	
VSS	98	
VSS	102	
VSS	106	
VSS	168	
VSS	172	
VSS	176	
VSS	180	
VSS	184	
VSS	188	
VSS	192	
VSS	196	
VSS	202	
VSS	206	
VSS	210	
VSS	214	
VSS	218	
VSS	222	
VSS	226	
VSS	230	
VSS	234	
VSS	238	
VSS	244	
VSS	248	
VSS	252	

BOM_COST_GROUP=DRAM

PAGE TITLE
DRAM: SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
BRANCH
PAGE 25 OF 105
SHEET 23 OF 70

=PP3V3_TBT_X_FLASH

R2890 3.3K 5% 1/20W MF 201

R2891 3.3K 5% 1/20W MF 201

R2893 3.3K 5% 1/20W MF 201

R2892 3.3K 5% 1/20W MF 201

C2890 1UF 10% 6.3V X5R-CERM 402

U2890 8MBIT-3.0V W25Q80DVUXIE USON OMIT_TABLE CRITICAL

TBT_X_SPI_CLK	CLK	DI(IO0)	TBT_X_SPI_MOSI
TBT_X_SPI_CS_L	CS*	DO(IO1)	TBT_X_SPI_MISO
TBT_X_ROM_WP_L	WP*(IO2)		
TBT_X_ROM_HOLD_L	HOLD*(IO3)		
	VCC		
	GND EPAD		

SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820 0.1UF	DP_X_SNK0_ML_P<0>
DP_X_SNK0_ML_C_N<0>	C2821 0.1UF	DP_X_SNK0_ML_N<0>
DP_X_SNK0_ML_C_P<1>	C2822 0.1UF	DP_X_SNK0_ML_P<1>
DP_X_SNK0_ML_C_N<1>	C2823 0.1UF	DP_X_SNK0_ML_N<1>
DP_X_SNK0_ML_C_P<2>	C2824 0.1UF	DP_X_SNK0_ML_P<2>
DP_X_SNK0_ML_C_N<2>	C2825 0.1UF	DP_X_SNK0_ML_N<2>
DP_X_SNK0_ML_C_P<3>	C2826 0.1UF	DP_X_SNK0_ML_P<3>
DP_X_SNK0_ML_C_N<3>	C2827 0.1UF	DP_X_SNK0_ML_N<3>
DP_X_SNK0_AUXCH_C_P	C2828 0.1UF	DP_X_SNK0_AUXCH_P
DP_X_SNK0_AUXCH_C_N	C2829 0.1UF	DP_X_SNK0_AUXCH_N

GND_VOID=TRUE; 10% 16V X5R-CERM 0201

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830 0.1UF	DP_X_SNK1_ML_P<0>
DP_X_SNK1_ML_C_N<0>	C2831 0.1UF	DP_X_SNK1_ML_N<0>
DP_X_SNK1_ML_C_P<1>	C2832 0.1UF	DP_X_SNK1_ML_P<1>
DP_X_SNK1_ML_C_N<1>	C2833 0.1UF	DP_X_SNK1_ML_N<1>
DP_X_SNK1_ML_C_P<2>	C2834 0.1UF	DP_X_SNK1_ML_P<2>
DP_X_SNK1_ML_C_N<2>	C2835 0.1UF	DP_X_SNK1_ML_N<2>
DP_X_SNK1_ML_C_P<3>	C2836 0.1UF	DP_X_SNK1_ML_P<3>
DP_X_SNK1_ML_C_N<3>	C2837 0.1UF	DP_X_SNK1_ML_N<3>
DP_X_SNK1_AUXCH_C_P	C2838 0.1UF	DP_X_SNK1_AUXCH_P
DP_X_SNK1_AUXCH_C_N	C2839 0.1UF	DP_X_SNK1_AUXCH_N

GND_VOID=TRUE; 10% 16V X5R-CERM 0201

R2862 100K 5% 1/20W MF 201	DP_XA_HPD
R2872 100K 5% 1/20W MF 201	DP_XB_HPD
R2860 1M 5% 1/20W MF 201	TBT_XA_LSTX
R2861 1M 5% 1/20W MF 201	TBT_XA_LSRX
R2870 1M 5% 1/20W MF 201	TBT_XB_LSTX
R2871 1M 5% 1/20W MF 201	TBT_XB_LSRX

U2800 TBT-AR-4C-CNTRL SYM 1 OF 2 FCBGA OMIT_TABLE CRITICAL

PCIE_TBT_X_R2D_P<0>	Y23	PCIE_RX0_P	PCIE_TX0_P	V23	PCIE_TBT_X_D2R_C_P<0>
PCIE_TBT_X_R2D_N<0>	Y22	PCIE_RX0_N	PCIE_TX0_N	V22	PCIE_TBT_X_D2R_C_N<0>
PCIE_TBT_X_R2D_P<1>	T23	PCIE_RX1_P	PCIE_TX1_P	P23	PCIE_TBT_X_D2R_C_P<1>
PCIE_TBT_X_R2D_N<1>	T22	PCIE_RX1_N	PCIE_TX1_N	P22	PCIE_TBT_X_D2R_C_N<1>
PCIE_TBT_X_R2D_P<2>	M23	PCIE_RX2_P	PCIE_TX2_P	K23	PCIE_TBT_X_D2R_C_P<2>
PCIE_TBT_X_R2D_N<2>	M22	PCIE_RX2_N	PCIE_TX2_N	K22	PCIE_TBT_X_D2R_C_N<2>
PCIE_TBT_X_R2D_P<3>	H23	PCIE_RX3_P	PCIE_TX3_P	F23	PCIE_TBT_X_D2R_C_P<3>
PCIE_TBT_X_R2D_N<3>	H22	PCIE_RX3_N	PCIE_TX3_N	F22	PCIE_TBT_X_D2R_C_N<3>
PCIE_CLK100M_TBT_X_P	V19	PCIE_REFCLK_100_IN_P			
PCIE_CLK100M_TBT_X_N	T19	PCIE_REFCLK_100_IN_N			
TBT_X_CLKREQ_L	AC5	PCIE_CLKREQ*	PERST*	L4	PM_PLT_RST_TBT_X_L
			PCIE_RBIAS	N16	TBT_X_PCIE_BIAS

PCIE GEN3

10K PU ON CLOCKS PAGE

PLACE_NEAR=U2800.N16:2MM

R2851 3.01K 1% 1/20W MF 201

DP_X_SNK0_ML_P<0>	AB7	DPSNK0_ML0_P	DPSRC_ML0_P	R2	=DP_X_SRC_ML_P<0>
DP_X_SNK0_ML_N<0>	AC7	DPSNK0_ML0_N	DPSRC_ML0_N	R1	=DP_X_SRC_ML_N<0>
DP_X_SNK0_ML_P<1>	AB9	DPSNK0_ML1_P	DPSRC_ML1_P	N2	=DP_X_SRC_ML_P<1>
DP_X_SNK0_ML_N<1>	AC9	DPSNK0_ML1_N	DPSRC_ML1_N	N1	=DP_X_SRC_ML_N<1>
DP_X_SNK0_ML_P<2>	AB11	DPSNK0_ML2_P	DPSRC_ML2_P	L2	=DP_X_SRC_ML_P<2>
DP_X_SNK0_ML_N<2>	AC11	DPSNK0_ML2_N	DPSRC_ML2_N	L1	=DP_X_SRC_ML_N<2>
DP_X_SNK0_ML_P<3>	AB13	DPSNK0_ML3_P	DPSRC_ML3_P	J2	=DP_X_SRC_ML_P<3>
DP_X_SNK0_ML_N<3>	AC13	DPSNK0_ML3_N	DPSRC_ML3_N	J1	=DP_X_SRC_ML_N<3>
DP_X_SNK0_AUXCH_P	Y11	DPSNK0_AUX_P	DPSRC_AUX_P	W19	=DP_X_SRC_AUX_P
DP_X_SNK0_AUXCH_N	W11	DPSNK0_AUX_N	DPSRC_AUX_N	Y19	=DP_X_SRC_AUX_N
DP_X_SNK0_HPD	AA2	DPSNK0_HPD	DPSRC_HPD	G1	DP_X_SRC_HPD
=DP_X_SNK0_DDC_CLK	Y5	DPSNK0_DDC_CLK	DPSRC_RBIAS	N6	DP_X_SRC_RBIAS
=DP_X_SNK0_DDC_DATA	R4	DPSNK0_DDC_DATA			
DP_X_SNK1_ML_P<0>	AB15	DPSNK1_ML0_P	GPIO_0	U1	I2C_TBT_X_SDA
DP_X_SNK1_ML_N<0>	AC15	DPSNK1_ML0_N	GPIO_1	U2	I2C_TBT_X_SCL
DP_X_SNK1_ML_P<1>	AB17	DPSNK1_ML1_P	GPIO_2	V1	TBT_X_ROM_WP_L
DP_X_SNK1_ML_N<1>	AC17	DPSNK1_ML1_N	GPIO_3	V2	=TBT_X_TMU_CLK_OUT
DP_X_SNK1_ML_P<2>	AB19	DPSNK1_ML2_P	GPIO_4	W1	TBT_WAKE_L
DP_X_SNK1_ML_N<2>	AC19	DPSNK1_ML2_N	GPIO_5	W2	TBT_X_CIO_PLUG_EVENT_L
DP_X_SNK1_ML_P<3>	AB21	DPSNK1_ML3_P	GPIO_6	Y1	TBT_X_HDMI_DDC_DATA
DP_X_SNK1_ML_N<3>	AC21	DPSNK1_ML3_N	GPIO_7	Y2	TBT_X_HDMI_DDC_CLK
DP_X_SNK1_AUXCH_P	Y12	DPSNK1_AUX_P	GPIO_8	AA1	=TBT_X_GPIO_8
DP_X_SNK1_AUXCH_N	W12	DPSNK1_AUX_N	POC_GPIO_0	J4	I2C_TBT_XA_INT_L
DP_X_SNK1_HPD	Y6	DPSNK1_HPD	POC_GPIO_1	E2	I2C_TBT_XB_INT_L
=DP_X_SNK1_DDC_CLK	Y8	DPSNK1_DDC_CLK	POC_GPIO_2	D4	TBT_X_RTD3_USB_PWR_EN
=DP_X_SNK1_DDC_DATA	N4	DPSNK1_DDC_DATA	POC_GPIO_3	H4	TBT_X_FORCE_PWR
DP_X_SNK_RBIAS	Y18	DPSNK_RBIAS	POC_GPIO_4	F2	=TBT_X_BATLOW_L
JTAG_TBT_TDI	Y4	TDI	POC_GPIO_5	D2	PM_SLP_S3_L
JTAG_TBT_X_TMS	V4	TMS	POC_GPIO_6	F1	TBT_X_RTD3_CIO_PWR_EN
JTAG_TBT_TCK	T4	TCK	TEST_EN	E1	TBT_X_TEST_EN
JTAG_TBT_TDO	W4	TDO	TEST_PWR_GOOD	AB5	TBT_X_TEST_PWR_GOOD
TBT_X_RBIAS	H6	RBIAS	RESET*	F4	USBC_X_RESET_L
TBT_X_RSENSE	J6	RSENSE	XTAL_25_IN	D22	TBT_X_XTAL25M_IN
			XTAL_25_OUT	D23	TBT_X_XTAL25M_OUT
			EE_DI	AB3	=UPC_X_SPI_MOSI
			EE_DO	AC4	=UPC_X_SPI_MISO
			EE_CS*	AC3	=UPC_X_SPI_CS_L
			EE_CLK	AB4	=UPC_X_SPI_CLK
USB_AR_XA_P	E20	PA_USB2_D_P	PB_USB2_D_P	E19	USB_AR_XB_P
USB_AR_XA_N	D20	PA_USB2_D_N	PB_USB2_D_N	D19	USB_AR_XB_N
TBT_XA_LSTX	A5	PA_LSTX	PB_LSTX	B4	TBT_XB_LSTX
TBT_XA_LSRX	A4	PA_LSRX	PB_LSRX	B5	TBT_XB_LSRX
DP_XA_HPD	M4	PA_DPSRC_HPD	PB_DPSRC_HPD	G2	DP_XB_HPD
TBT_XA_USB2_RBIAS	H19	PA_USB2_RBIAS	PB_USB2_RBIAS	F19	TBT_XB_USB2_RBIAS
TBT_X_THERM_D_P	AC23	THERMDA	MONDC_SVR	D6	
	AB23	THERMDA	ATEST_P	A23	NC
	V18	PCIE_ATEST	ATEST_N	B23	NC
	AC1	TEST_EDM	USB2_ATEST	E18	NC
	L15	FUSE_VQPS_64	MONDC_DPSNK_0	W13	
	N15	FUSE_VQPS_128	MONDC_DPSNK_1	W18	
	C23	MONDC_CIO_0	MONDC_DPSRC	AB2	
	C22	MONDC_CIO_1			

SINK PORT 0; SOURCE PORT 0; SINK PORT 1; LC GPIO; POC GPIO; MISC; PORT A; PORT B; TBT PORTS; DEBUG

R2830 100K 5% 1/20W MF 201

R2831 100K 5% 1/20W MF 201

R2850 14K 1% 1/20W MF 201 PLACE_NEAR=U2800.Y18:2MM

R2855 4.75K TF 1/20W 0.5% 0201 PLACE_NEAR=U2800.H6:2MM PLACE_NEAR=U2800.J6:2MM

R2854 499 1% 1/20W MF 201 PLACE_NEAR=U2800.H19:2MM

USE NEAREST GND BALL (AC22) FOR THERM_D_N

R2852 14K 1% 1/20W MF 201 PLACE_NEAR= U2800.N6:2MM

R2853 499 1% 1/20W MF 201 PLACE_NEAR=U2800.F19:2MM

R2834 2.2K 5% 1/20W MF 201 =PP3V3_TBT_X_SX

R2835 2.2K 5% 1/20W MF 201 =PP3V3_TBT_X_SX

R2836 2.2K 5% 1/20W MF 201 =PP3V3_TBT_X_SX

R2837 2.2K 5% 1/20W MF 201 =PP3V3_TBT_X_SX

R2827 100K 5% 1/20W MF 201 not used

R2829 100 5% 1/20W MF 201 To SPI Flash

R2825 100 5% 1/20W MF 201

C2810 0.1UF 0201 16V 10% X5R-CERM GND_VOID=TRUE

C2811 0.1UF 0201 16V 10% X5R-CERM GND_VOID=TRUE

C2812 0.1UF GND_VOID=TRUE DP_XB_AUXCH_P

C2813 0.1UF GND_VOID=TRUE DP_XB_AUXCH_N

BOM_COST_GROUP=TBT

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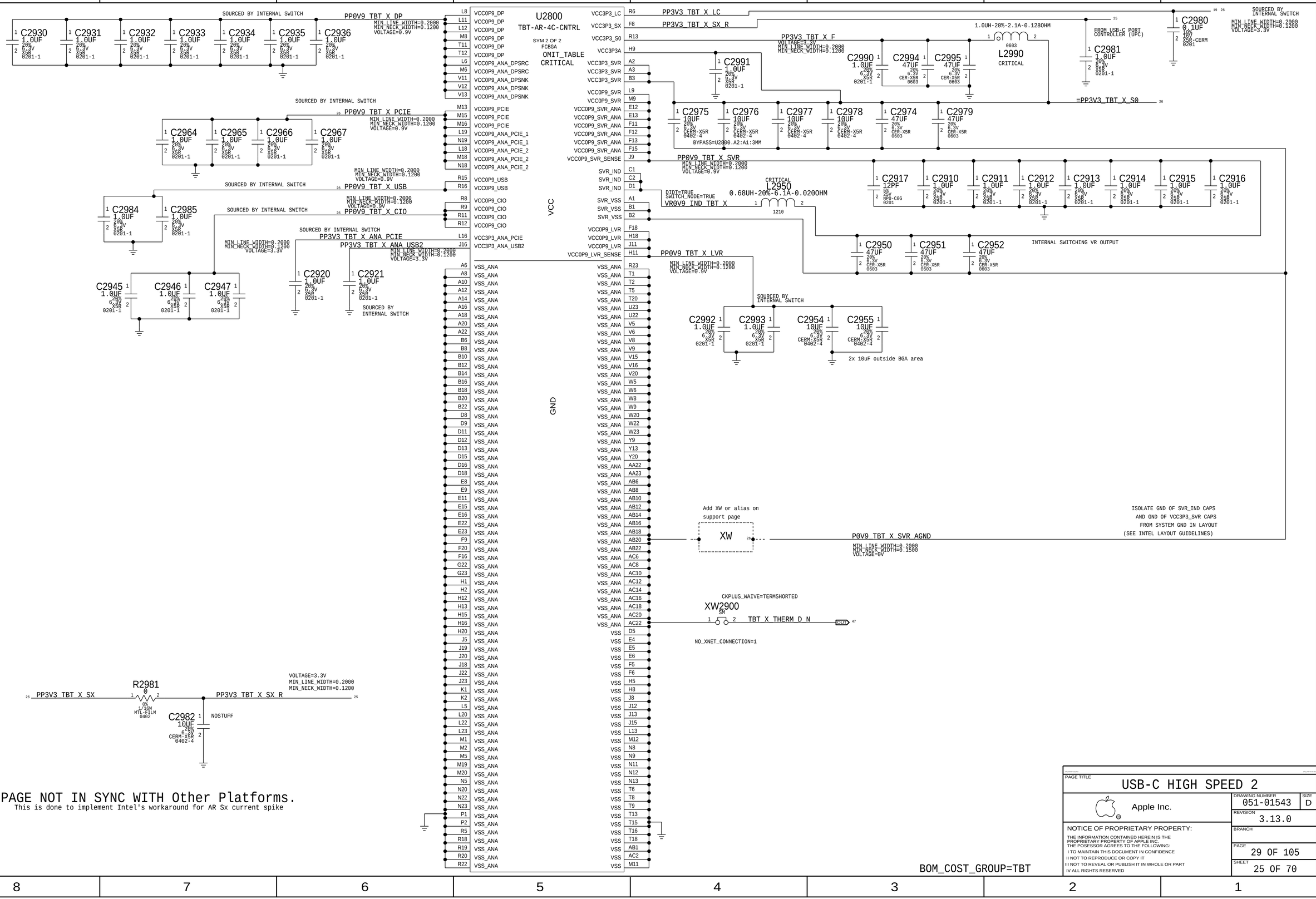

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USB-C HIGH SPEED 2

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RIDGE AC COUPLING

R2D

PCIE_TBT_X_R2D_C_P<0>	C3040	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_N<0>	C3041	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_P<1>	C3042	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_N<1>	C3043	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_P<2>	C3044	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_N<2>	C3045	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_P<3>	C3046	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_R2D_C_N<3>	C3047	0201	X5R	20% 6.3V	0.22UF

PCIE_TBT_X_R2D_C_P<0> → PCIE_TBT_X_R2D_P<0>
PCIE_TBT_X_R2D_C_N<0> → PCIE_TBT_X_R2D_N<0>
PCIE_TBT_X_R2D_C_P<1> → PCIE_TBT_X_R2D_P<1>
PCIE_TBT_X_R2D_C_N<1> → PCIE_TBT_X_R2D_N<1>
PCIE_TBT_X_R2D_C_P<2> → PCIE_TBT_X_R2D_P<2>
PCIE_TBT_X_R2D_C_N<2> → PCIE_TBT_X_R2D_N<2>
PCIE_TBT_X_R2D_C_P<3> → PCIE_TBT_X_R2D_P<3>
PCIE_TBT_X_R2D_C_N<3> → PCIE_TBT_X_R2D_N<3>

D2R

PCIE_TBT_X_D2R_C_P<0>	C3050	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_N<0>	C3051	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_P<1>	C3052	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_N<1>	C3053	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_P<2>	C3055	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_N<2>	C3056	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_P<3>	C3057	0201	X5R	20% 6.3V	0.22UF
PCIE_TBT_X_D2R_C_N<3>	C3054	0201	X5R	20% 6.3V	0.22UF

PCIE_TBT_X_D2R_C_P<0> → PCIE_TBT_X_D2R_P<0>
PCIE_TBT_X_D2R_C_N<0> → PCIE_TBT_X_D2R_N<0>
PCIE_TBT_X_D2R_C_P<1> → PCIE_TBT_X_D2R_P<1>
PCIE_TBT_X_D2R_C_N<1> → PCIE_TBT_X_D2R_N<1>
PCIE_TBT_X_D2R_C_P<2> → PCIE_TBT_X_D2R_P<2>
PCIE_TBT_X_D2R_C_N<2> → PCIE_TBT_X_D2R_N<2>
PCIE_TBT_X_D2R_C_P<3> → PCIE_TBT_X_D2R_P<3>
PCIE_TBT_X_D2R_C_N<3> → PCIE_TBT_X_D2R_N<3>

ACE RPD, BUSPOWERZ, & HPD STRAPPING

CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE

USBC_XA_RPD_G1	R3026	0	5% 1/20W MF 0201
USBC_XA_RPD_G2	R3022	0	5% 1/20W MF 0201
USBC_XB_RPD_G1	R3011	0	5% 1/20W MF 0201
USBC_XB_RPD_G2	R3024	0	5% 1/20W MF 0201

PU BUSPOWERZ TO LDO_3V3 TO NOT PASS VBUS TO SYS UNDER DB CASE

PU BUSPOWERZ TO 1V8D TO PASS VBUS TO SYS UNDER DB CASE USES INT POWER PATH

GND BUSPOWERZ TO PASS VBUS TO SYS UNDER DB CASE USES EXT POWER PATH

RIDGE DEBUG CONN

J3099 505070-1220 M-ST-SN — BOMOPTION=DEVELOPMENT — 516S00115

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
ARKANOID_P5	5	6	PP3V3_TBT_X_SX
ARKANOID_P7	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO
	13	14	
	15	16	

R3082 0 0201 MF 1/20W 5% DP_XA_HPD
R3083 0 0201 MF 1/20W 5% SMC_DEBUGPRT_TX_L — PLACE_NEAR=U4610.5:10MM NOSTUFF NO_XNET_CONNECTION=1
R3080 0 0201 MF 1/20W 5% DP_X_SNK1_HPD
R3081 0 0201 MF 1/20W 5% SMC_DEBUGPRT_RX_L — PLACE_NEAR=U4610.4:10MM NOSTUFF NO_XNET_CONNECTION=1

ACE DEBUG CONN

J3098 505070-1220 M-ST-SN — BOMOPTION=DEVELOPMENT — 516S00115

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
=I2C_UPC_XA_SCL2	3	4	I2C_TBT_X_SDA
=I2C_UPC_XA_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XB_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XB_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX
	13	14	
	15	16	

USB-C DEBUG CONN

J3095 505070-1220 M-ST-SN — BOMOPTION=DEVELOPMENT — 516S00115

UPC_XA_RESET	1	2	DP_XB_HPD
TBT_X_SPI_CLK	3	4	USB_EXTAB_HILIM_EN
TBT_X_SPI_MOSI	5	6	USB_EXTCD_HILIM_EN
TBT_X_SPI_MISO	7	8	TBT_XA_LSTX
TBT_X_SPI_CS_L	9	10	TBT_XA_LSRX
TBT_XB_LSTX	11	12	TBT_XB_LSRX
	13	14	
	15	16	

LOCAL POWER ALIASES

=PP3V3_UPC_XA_LDO	MAKE_BASE=TRUE VOLTAGE=3.3V	PP3V3_UPC_XA_LDO
=PP3V3R1V8_UPC_XA		
=PP3V3_TBT_X_FLASH		
=PP3V3_UPC_XB_LDO	MAKE_BASE=TRUE VOLTAGE=3.3V	PP3V3_UPC_XB_LDO
=PP3V3R1V8_UPC_XB		
=PP3V3_TBT_X_SX	MAKE_BASE=TRUE VOLTAGE=3.3V	PP3V3_TBT_X_SX
=PP3V3_UPC_XA_SX		
=PP3V3_UPC_XB_SX		

GLOBAL POWER ALIASES

=PP3V3_G3H_UPC_XA		=PP3V3_G3H_USBC
=PP3V3_G3H_UPC_XB		
=PP3V3_TBT_X_S0		=PP3V3_S0_TBT_X
=PP5V_USBC_XA		=PP5V_S4_USBC
=PP5V_USBC_XB		

MISC ALIASES

TBT_WAKE_L		=UPC_WAKE_L
USBC_X_POC_RESET	MAKE_BASE=TRUE	TBT_POC_RESET
=UPC_X_SPI_CLK	MAKE_BASE=TRUE	UPC_X_SPI_CLK
=UPC_X_SPI_CS_L	MAKE_BASE=TRUE	UPC_X_SPI_CS_L
=UPC_X_SPI_MOSI	MAKE_BASE=TRUE	UPC_X_SPI_MOSI
=UPC_X_SPI_MISO	MAKE_BASE=TRUE	UPC_X_SPI_MISO
TBT_X_RTD3_CIO_PWR_EN	MAKE_BASE=TRUE	TBT_X_CIO_PWR_EN
UPC_XB_GPIO2		
TBT_X_RTD3_USB_PWR_EN	MAKE_BASE=TRUE	TBT_X_USB_PWR_EN
UPC_XB_GPIO3		
UPC_XB_SPI_CLK		
UPC_XB_SPI_CS_L		
UPC_XB_SPI_MISO		
UPC_XB_SPI_MOSI		
UPC_XB_RESET		
UPC_XA_RESET	MAKE_BASE=TRUE	

R3051 1K 5% 1/20W MF 201

XW3001 SM — PLACE_NEAR=U2800.A1:5MM NO_XNET_CONNECTION=1 — P0V9_TBT_X_SVR_AGND — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500

DP / USB SOURCE ALIASES

DP_X_SRC_ML_P<1..0>	MAKE_BASE=TRUE	=DP_X_SRC_ML_P<1..0>
DP_X_SRC_ML_N<1..0>	MAKE_BASE=TRUE	=DP_X_SRC_ML_N<1..0>
DP_X_SRC_AUX_P	MAKE_BASE=TRUE	=DP_X_SRC_AUX_P
DP_X_SRC_AUX_N	MAKE_BASE=TRUE	=DP_X_SRC_AUX_N

DP_DDI2_ML_C_P<0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<3>
DP_DDI2_ML_C_P<1>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<0>
DP_DDI2_ML_C_P<2>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<2>
DP_DDI2_ML_C_P<3>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<1>
DP_DDI2_ML_C_N<0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<3>
DP_DDI2_ML_C_N<1>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<0>
DP_DDI2_ML_C_N<2>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<2>
DP_DDI2_ML_C_N<3>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<1>
DP_DDI2_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_P
DP_DDI2_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_N
DP_DDI1_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_P
DP_DDI1_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_N
DP_DDI1_ML_C_P<0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<2>
DP_DDI1_ML_C_P<1>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<0>
DP_DDI1_ML_C_P<2>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<3>
DP_DDI1_ML_C_P<3>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<1>
DP_DDI1_ML_C_N<0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<2>
DP_DDI1_ML_C_N<1>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<0>
DP_DDI1_ML_C_N<2>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<3>
DP_DDI1_ML_C_N<3>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<1>

I2C_TBT_X_SDA / I2C_TBT_X_SCL / I2C_TBT_XA_INT_L / I2C_TBT_XB_INT_L

TBT - MASTER
ALPINE RIDGE - U2800

UPC XA - U3100		=I2C_UPC_XA_SDA1
		=I2C_UPC_XA_SCL1
(WRITE: 0X70 READ: 0X71)		=I2C_UPC_XA_INT1_L
		=I2C_UPC_XB_SDA1
UPC XB - U3200		=I2C_UPC_XB_SCL1
(WRITE: 0X7E READ: 0X7F)		=I2C_UPC_XB_INT1_L

SPI ROM

TBT_X_SPI_CLK	R3098 100 5% 1/20W MF 201	TBT_X_SPI_CLK_DBG
TBT_X_SPI_CS_L	R3090 15 5% 1/20W MF 201	UPC_XA_SPI_CLK
TBT_X_SPI_MOSI	R3091 15 5% 1/20W MF 201	UPC_XA_SPI_CS_L
TBT_X_SPI_MISO	R3092 15 5% 1/20W MF 201	UPC_XA_SPI_MOSI
	R3093 15 5% 1/20W MF 201	UPC_XA_SPI_MISO
	R3094 15 5% 1/20W MF 201	=UPC_X_SPI_CLK
	R3095 15 5% 1/20W MF 201	=UPC_X_SPI_CS_L
	R3096 15 5% 1/20W MF 201	=UPC_X_SPI_MOSI
	R3097 15 5% 1/20W MF 201	=UPC_X_SPI_MISO

ACE

AR

R3099 5% 201 10K 1/20W MF
=USBC_XA_RESET_L → USBC_X_RESET_R_L (MAKE_BASE=TRUE) → USBC_X_RESET_L
D3099 SM-201 RB521ZS-30
C3099 1.0UF 20% 6.3V X5R 0201-1

UPC_XA_DBG1	MAKE_BASE=TRUE	SMC_TCK
UPC_XA_DBG2	MAKE_BASE=TRUE	SMC_TMS
UPC_XA_DBG3	MAKE_BASE=TRUE	SMC_DEBUGPRT2_TX_L
UPC_XA_DBG4	MAKE_BASE=TRUE	SMC_DEBUGPRT2_RX_L

SMC SWD ON USB-C A

PPVBUS_USBC_XA	MAKE_BASE=TRUE	TP_PPVBUS_USBC_XA
PPVBUS_USBC_XB	MAKE_BASE=TRUE	TP_PPVBUS_USBC_XB

=I2C_UPC_XB_SDA2_R	R3033 33 5% 1/20W MF 201 PLACE_NEAR=U5600:5MM	=I2C_UPC_XB_SDA2
=I2C_UPC_XA_SDA2_R		=I2C_UPC_XA_SDA2
I2C_UPC_X_SDA2_R		I2C_UPC_X_SDA2
=I2C_UPC_XA_SCL2_R	R3034 33 5% 1/20W MF 201 PLACE_NEAR=U5800:5MM	=I2C_UPC_XA_SCL2
=I2C_UPC_XB_SCL2_R		=I2C_UPC_XB_SCL2
I2C_UPC_X_SCL2_R		I2C_UPC_X_SCL2

R3032 100K 5% 1/20W MF 201 NOSTUFF
UPC_XB_HPD_RX → SMC_RESET_L

UPC_XB_DBG3	R3078 0 5% 1/20W MF 0201 NOSTUFF	SMC_DEBUGPRT_TX_L
UPC_XB_DBG4	R3077 0 5% 1/20W MF 0201 NOSTUFF	SMC_DEBUGPRT_RX_L

R3085 100K 5% 1/16W MF-LF 402
R3086 100K 5% 1/16W MF-LF 402

PP3V3_TBT_X_LC → R3071 100K 5% 1/20W MF 201 → TBT_X_HDMI_DDC_CLK

PP3V3_TBT_X_SX → R3073 100K 5% 1/20W MF 201 → TBT_X_BATLOW_L (MAKE_BASE=TRUE) → =TBT_X_BATLOW_L

R3035 100K 5% 1/20W MF 201	JTAG_TBT_TCK	
R3036 100K 5% 1/20W MF 201	JTAG_TBT_TDI	
R3075 100K 5% 1/20W MF 201	UPC_XB_DBG1	
R3076 100K 5% 1/20W MF 201	UPC_XB_DBG2	
R3072 100K 5% 1/20W MF 201	TBT_X_HDMI_DDC_DATA	
R3020 100K 5% 1/20W MF 201	DP_X_SRC_HPD	

LOCAL BULK CAP

=PP5V_S4_USBC → C3000 220UF-35MOHM 20% 35V POLY-TANT CASE-B2-SM1

R3066 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	DP_X_SNK0_DDC_DATA	=DP_X_SNK0_DDC_DATA
R3067 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	DP_X_SNK0_DDC_CLK	=DP_X_SNK0_DDC_CLK
R3069 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	DP_X_SNK1_DDC_CLK	=DP_X_SNK1_DDC_CLK
R3070 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	DP_X_SNK1_DDC_DATA	=DP_X_SNK1_DDC_DATA
R3040 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_UPC_XA_GPIO5	UPC_XA_HPD_RX
R3041 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_UPC_XB_GPIO5	UPC_XB_HPD_RX
R3042 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_UPC_XA_GPIO6	UPC_XA_5V_EN
R3043 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_UPC_XB_GPIO6	UPC_XB_5V_EN
R3049 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_TBT_X_TMU_CLK_OUT	=TBT_X_TMU_CLK_OUT
R3050 100K 5% 1/20W MF 201 (MAKE_BASE=TRUE)	PD_TBT_X_GPIO_8	=TBT_X_GPIO_8

PD WHEN NOT USED

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB	
LAST CHANGE: Mon Nov 2 17:15:56 2015	
PAGE TITLE	USB-C SUPPORT
Apple Inc.	DRAWING NUMBER 051-01543 · SIZE D
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PRIMARY ACE USB-C PORT CONTROLLER (UPC)

PPVBUS_USBC_XA
C3101
1UF
=PP3V3R1V8_UPC_XA
PP3V3_G3H_UPC_XA_R
=PPHV_TBT_XA
=PP5V_USBC_XA
=PP3V3_G3H_UPC_XA
R3189
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
C3198
C3199
C3100
=PP3V3_UPC_XA_LDO
=PP3V3_UPC_XA_SX
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_XA_LDOA
PP1V8_UPC_XA_LDOD
PP1V1_UPC_XA_LDO_BMC
C3105
C3108
C3104
C3106
PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES
R3109
I2C_UPC_XA_DBG_CTL_SCL
R3108
I2C_UPC_XA_DBG_CTL_SDA
R3105
UPC_XA_UART_RX
TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS
USE GPIO5 for SMC RESET after boot.
U3100
CD3215A
BGA
OMIT_TABLE
CRITICAL
PRIMARY ONLY
USBC_X_POC_RESET
=USBC_XA_RESET_L
TP_UPC_XA_DBG_UART_TX
TP_UPC_XA_DBG_UART_RX
TBT_X_RTD3_CIO_PWR_EN
TBT_X_RTD3_USB_PWR_EN
DP_XA_HPD
UPC_XA_HPD_RX
UPC_XA_5V_EN
=UPC_WAKE_L
UPC_XA_FAULT_L
UPC_XA_SS
C3109
NC_UPC_XA_HV_GATE1
NC_UPC_XA_HV_GATE2
USBC_XA_CC1
USBC_XA_CC2
USBC_XA_RPD_G1
USBC_XA_RPD_G2
USBC_XA_USB_TOP_P
USBC_XA_USB_TOP_N
USBC_XA_USB_BOT_P
USBC_XA_USB_BOT_N
USBC_XA_SBU1
USBC_XA_SBU2
C3114
C3113
NC or GND to dissipate heat
GND I2C ADDR PRIMARY ONLY
R3102
R3103
NEED 0.1%
UPC_XA_I2C_ADDR
UPC_XA_R_OSC
I2C_UPC_XA_DBG_CTL_SCL
I2C_UPC_XA_DBG_CTL_SDA
=I2C_UPC_XA_SDA1
=I2C_UPC_XA_SCL1
=I2C_UPC_XA_INT1_L
=I2C_UPC_XA_SDA2
=I2C_UPC_XA_SCL2
=I2C_UPC_XA_INT2_L
TO SMC
UPC_XA_SPI_CLK
UPC_XA_SPI_MOSI
UPC_XA_SPI_MISO
UPC_XA_SPI_CS_L
REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI
TP_UPC_XA_SWD_DATA
TP_UPC_XA_SWD_CLK
UPC_XA_UART_RX
UPC_XA_UART_TX
TBT_XA_LSTX
TBT_XA_LSRX
L3100
90-OHM-0.1A
EXCX4CE
RIDGE/PCH USB2
USB_UPC_XA_P
USB_UPC_XA_N
USB_UPC_XA_F_P
USB_UPC_XA_F_N
PLACE_NEAR=U3100:5mm
DP_XA_AUXCH_P
DP_XA_AUXCH_N
=PP3V3_UPC_XA_AUX
PU to PP3V3_S4 if convenient for layout, Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3110
100K
UPC_XA_DBG1
UPC_XA_DBG2
UPC_XA_DBG3
UPC_XA_DBG4
R3111
100K
UPC_XA_RESET
PIN D6 IS UNDOCUMENTED RESET. CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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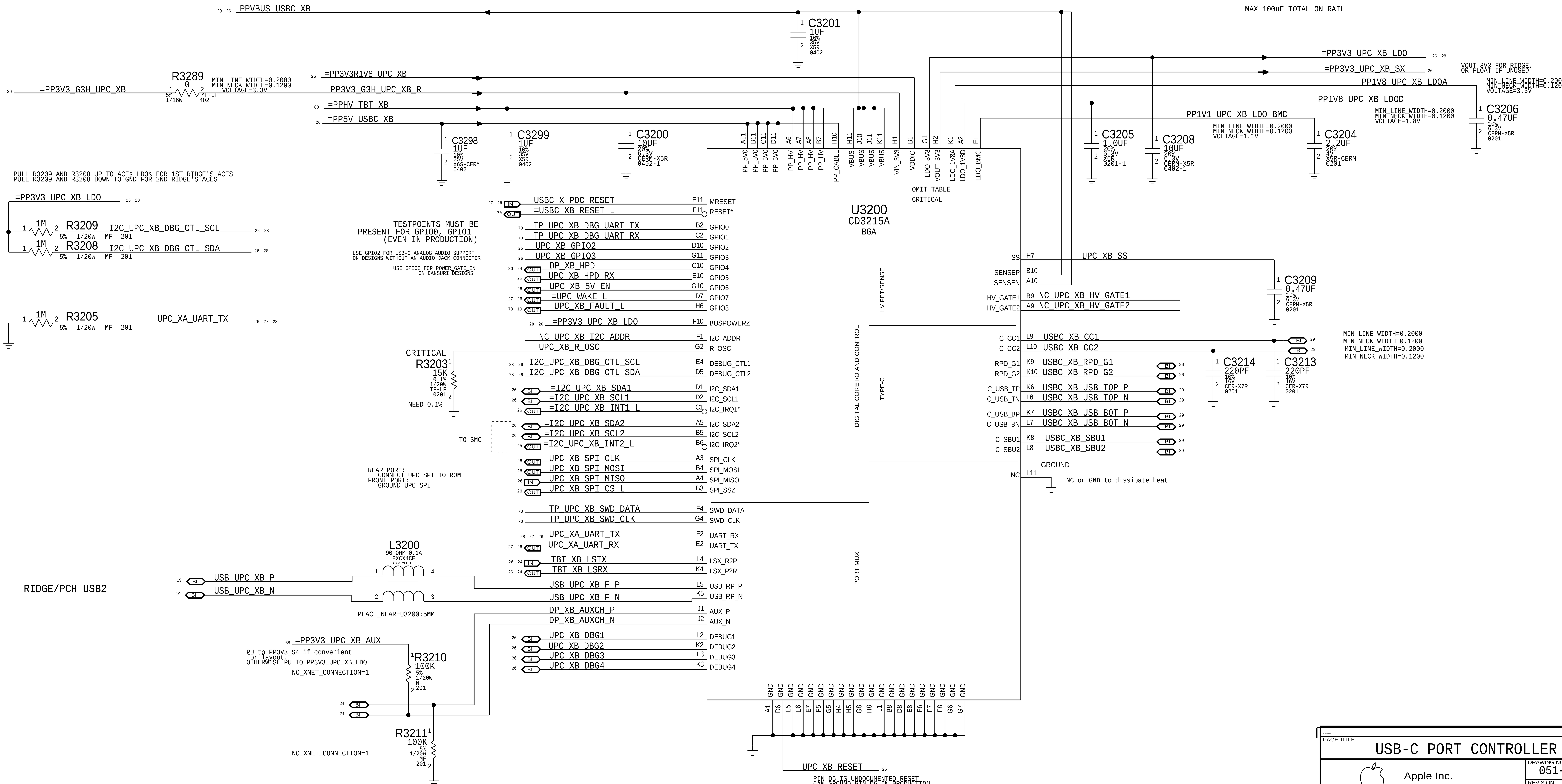
SECONDARY ACE USB-C PORT CONTROLLER (UPC)


PPVBUS_USBC_XB
C3201
1UF
MAX 100uF TOTAL ON RAIL
=PP3V3_UPC_XB_LDO
=PP3V3_UPC_XB_SX
VOUT_3V3 FOR RIDGE,
OR FLOAT IF UNUSED
PP1V8_UPC_XB_LDOA
PP1V8_UPC_XB_LDOD
PP1V1_UPC_XB_LDO_BMC
C3206
0.47UF
R3289
=PP3V3_G3H_UPC_XB
=PP3V3R1V8_UPC_XB
PP3V3_G3H_UPC_XB_R
=PPHV_TBT_XB
=PP5V_USBC_XB
C3298
1UF
C3299
1UF
C3200
10UF
C3205
1.0UF
C3208
10UF
C3204
2.2UF
PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES
=PP3V3_UPC_XB_LDO
R3209
I2C_UPC_XB_DBG_CTL_SCL
R3208
I2C_UPC_XB_DBG_CTL_SDA
R3205
UPC_XA_UART_TX
TESTPOINTS MUST BE
PRESENT FOR GPIO0, GPIO1
(EVEN IN PRODUCTION)
USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT
ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR
USE GPIO3 FOR POWER_GATE_EN
ON BANSURI DESIGNS
U3200
CD3215A
BGA
OMIT_TABLE
CRITICAL
USBC_X_POC_RESET
=USBC_XB_RESET_L
TP_UPC_XB_DBG_UART_TX
TP_UPC_XB_DBG_UART_RX
UPC_XB_GPIO2
UPC_XB_GPIO3
DP_XB_HPD
UPC_XB_HPD_RX
UPC_XB_5V_EN
=UPC_WAKE_L
UPC_XB_FAULT_L
=PP3V3_UPC_XB_LDO
NC_UPC_XB_I2C_ADDR
UPC_XB_R_OSC
CRITICAL
R3203
15K
NEED 0.1%
I2C_UPC_XB_DBG_CTL_SCL
I2C_UPC_XB_DBG_CTL_SDA
=I2C_UPC_XB_SDA1
=I2C_UPC_XB_SCL1
=I2C_UPC_XB_INT1_L
=I2C_UPC_XB_SDA2
=I2C_UPC_XB_SCL2
=I2C_UPC_XB_INT2_L
TO SMC
UPC_XB_SPI_CLK
UPC_XB_SPI_MOSI
UPC_XB_SPI_MISO
UPC_XB_SPI_CS_L
REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI
TP_UPC_XB_SWD_DATA
TP_UPC_XB_SWD_CLK
UPC_XA_UART_TX
UPC_XA_UART_RX
TBT_XB_LSTX
TBT_XB_LSRX
L3200
90-OHM-0.1A
RIDGE/PCH USB2
USB_UPC_XB_P
USB_UPC_XB_N
USB_UPC_XB_F_P
USB_UPC_XB_F_N
PLACE_NEAR=U3200:5MM
DP_XB_AUXCH_P
DP_XB_AUXCH_N
=PP3V3_UPC_XB_AUX
PU to PP3V3_S4 if convenient
for layout,
OTHERWISE PU TO PP3V3_UPC_XB_LDO
NO_XNET_CONNECTION=1
R3210
100K
UPC_XB_DBG1
UPC_XB_DBG2
UPC_XB_DBG3
UPC_XB_DBG4
R3211
100K
NO_XNET_CONNECTION=1
UPC_XB_SS
C3209
0.47UF
NC_UPC_XB_HV_GATE1
NC_UPC_XB_HV_GATE2
USBC_XB_CC1
USBC_XB_CC2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
USBC_XB_RPD_G1
USBC_XB_RPD_G2
C3214
220PF
C3213
220PF
USBC_XB_USB_TOP_P
USBC_XB_USB_TOP_N
USBC_XB_USB_BOT_P
USBC_XB_USB_BOT_N
USBC_XB_SBU1
USBC_XB_SBU2
GROUND
NC or GND to dissipate heat
HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX
UPC_XB_RESET
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

REVISION 3.13.0

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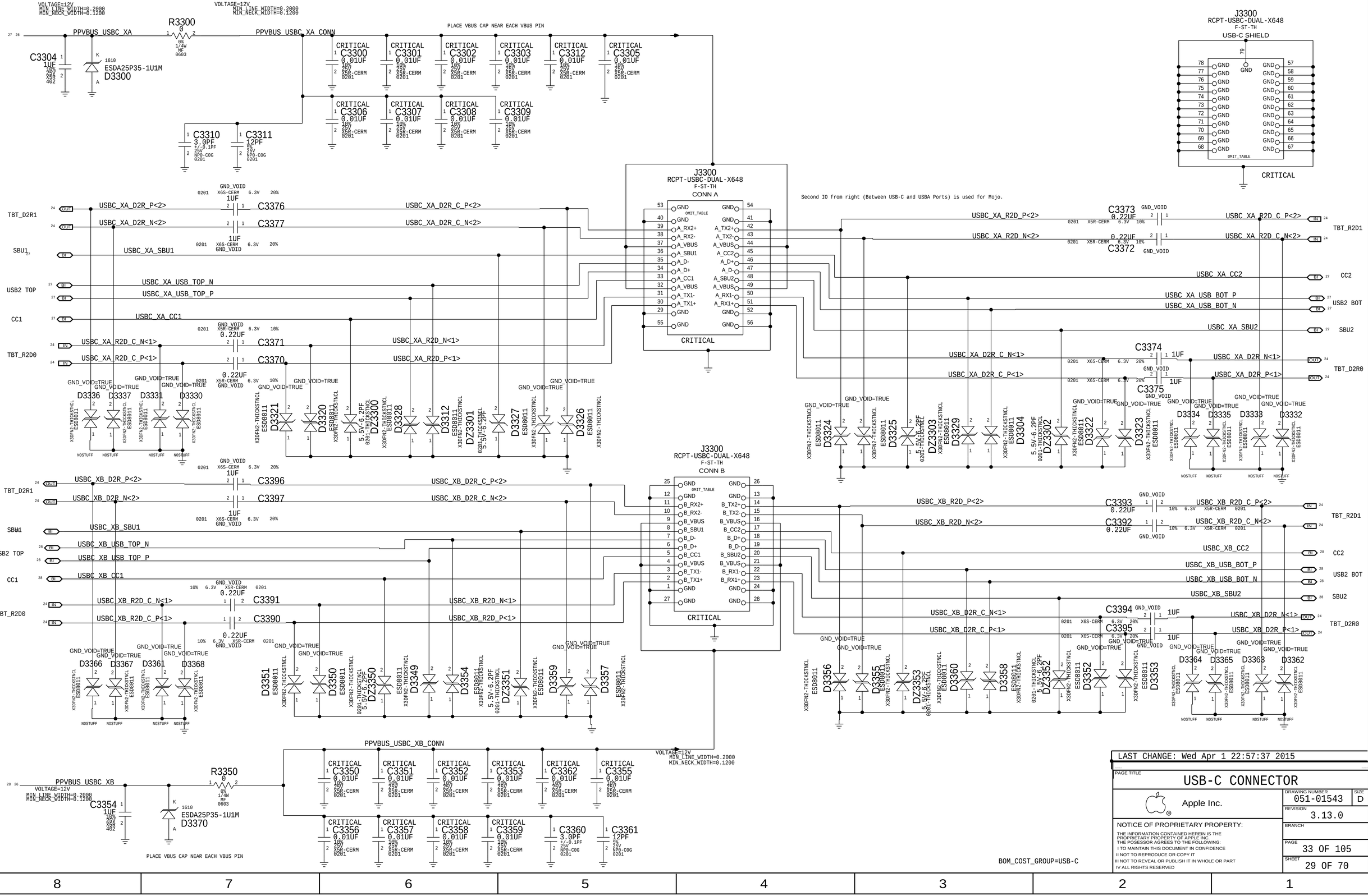
R3300
0
PPVBUS_USBC_XA
PPVBUS_USBC_XA_CONN
C3304
1UF
ESDA25P35-1U1M
D3300
PLACE VBUS CAP NEAR EACH VBUS PIN
C3300
C3301
C3302
C3303
C3312
C3305
C3306
C3307
C3308
C3309
C3310
3.0PF
C3311
12PF
J3300
RCPT-USBC-DUAL-X648
F-ST-TH
CONN A
CRITICAL
USB-C SHIELD
GND_VOID
C3376
C3377
C3371
C3370
C3396
C3397
C3391
C3390
USBC_XA_D2R_P<2>
USBC_XA_D2R_N<2>
USBC_XA_D2R_C_P<2>
USBC_XA_D2R_C_N<2>
USBC_XA_SBU1
USBC_XA_USB_TOP_N
USBC_XA_USB_TOP_P
USBC_XA_CC1
USBC_XA_R2D_C_N<1>
USBC_XA_R2D_C_P<1>
USBC_XA_R2D_N<1>
USBC_XA_R2D_P<1>
TBT_D2R1
TBT_R2D0
USB2 TOP
CC1
SBU1
D3336
D3337
D3331
D3330
D3321
D3320
DZ3300
D3328
D3312
DZ3301
D3327
D3326
D3366
D3367
D3361
D3368
D3351
D3350
DZ3350
D3349
D3354
DZ3351
D3359
D3357
J3300
RCPT-USBC-DUAL-X648
F-ST-TH
CONN B
USBC_XB_D2R_P<2>
USBC_XB_D2R_N<2>
USBC_XB_D2R_C_P<2>
USBC_XB_D2R_C_N<2>
USBC_XB_SBU1
USBC_XB_USB_TOP_N
USBC_XB_USB_TOP_P
USBC_XB_CC1
USBC_XB_R2D_C_N<1>
USBC_XB_R2D_C_P<1>
USBC_XB_R2D_N<1>
USBC_XB_R2D_P<1>
PPVBUS_USBC_XB_CONN
PPVBUS_USBC_XB
R3350
C3354
ESDA25P35-1U1M
D3370
C3350
C3351
C3352
C3353
C3362
C3355
C3356
C3357
C3358
C3359
C3360
3.0PF
C3361
12PF
PLACE VBUS CAP NEAR EACH VBUS PIN
Second IO from right (Between USB-C and USBA Ports) is used for Mojo.
C3373
C3372
C3374
C3375
C3393
C3392
C3394
C3395
USBC_XA_R2D_P<2>
USBC_XA_R2D_N<2>
USBC_XA_R2D_C_P<2>
USBC_XA_R2D_C_N<2>
USBC_XA_CC2
USBC_XA_USB_BOT_P
USBC_XA_USB_BOT_N
USBC_XA_SBU2
USBC_XA_D2R_C_N<1>
USBC_XA_D2R_C_P<1>
USBC_XA_D2R_N<1>
USBC_XA_D2R_P<1>
TBT_R2D1
TBT_R2D0
CC2
USB2 BOT
SBU2
D3324
D3325
DZ3303
D3329
D3304
DZ3302
D3322
D3323
D3334
D3335
D3333
D3332
D3356
D3355
DZ3353
D3360
D3358
DZ3352
D3352
D3353
D3364
D3365
D3363
D3362
BOM_COST_GROUP=USB-C
LAST CHANGE: Wed Apr 1 22:57:37 2015
PAGE TITLE
USB-C CONNECTOR
Apple Inc.
DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
BRANCH
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WLAN
BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

CRITICAL L3502 FERR-220-OHM-2.5A 0603
PP3V3_S4_AP_FET — MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000
PP3V3_S4_AP_FLT — MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603
C3505 0.1UF 10% 6.3V X5R-CERM 0201
C3506 0.1UF 10% 6.3V X5R-CERM 0201

PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

PCH_BT_ROM_BOOT_L_R
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P

U3510 TPS22966 DPU

=PP3V3_G3H_BT	1	VIN1	VOUT1 13
SMC_BT_PWR_EN	3	ON1	
BT_PWR_SS	12	CT1	
=PP3V3_G3H_BT	4	VBIAS	
=PP3V3_S4_AP	6	VIN2	VOUT2 8
AP_PWR_EN	5	ON2	
WL_PWR_SS	10	CT2	
	11	GND	
	15	THRM PAD	

C3511 0.001UF 10% 50V X7R-CERM 0402
C3510 0.1UF 10% 16V X7R-CERM 0402
C3512 0.001UF 10% 50V X7R-CERM 0402

CRITICAL L3501 FERR-220-OHM-2.5A 0603
PP3V3_G3H_BT_FET — VOLTAGE=3.3V MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000
PP3V3_G3H_BT_FLT — VOLTAGE=3.3V MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

=PP3V3_G3H_BT
R3502 10K 5% 1/20W MF 201
NOSTUFF R3504 0 5% 1/10W MF-LF 603
PCH_BT_ROM_BOOT_L
CRITICAL Q3502
R3503 10K 5% 1/20W MF 201 NOSTUFF
PCH_BT_ROM_BOOT
R3505 100K 5% 1/20W MF 201

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K 1% 1/10W MF-LF 402
R3531 232K 1% 1/10W MF-LF 402
P3V3AP_VMON
CRITICAL U3530 SLG4AP041V TDFN
C3530 0.1uF 20% 10V CERM 402
AP_RESET_CONN_R_L
R3533 33 5% 1/20W MF 201
R3532 100K 1% 1/10W MF-LF 402

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L
CRITICAL Q3501
=PP3V3_G3H_BT
C3500 0.1UF 10% 10V X5R-CERM 0201
U3501 PI3USB102EZLE TQFN
USB_BT_WAKEN
USB_BT_P
USB_BT_N
USB_BT_MUX_P
USB_BT_MUX_N
PM_SLP_S5_L
R3501 15K 1% 1/20W MF 201

CRITICAL Q3570
PP3V3_S4_AP_FLT
R3570 10K 5% 1/10W MF-LF 402
PCIE_WAKE_L
AP_WAKE_L

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J135_MLB SYNC_DATE=06/08/2015

PAGE TITLE: WIRELESS: Airport/Bluetooth

Apple Inc.

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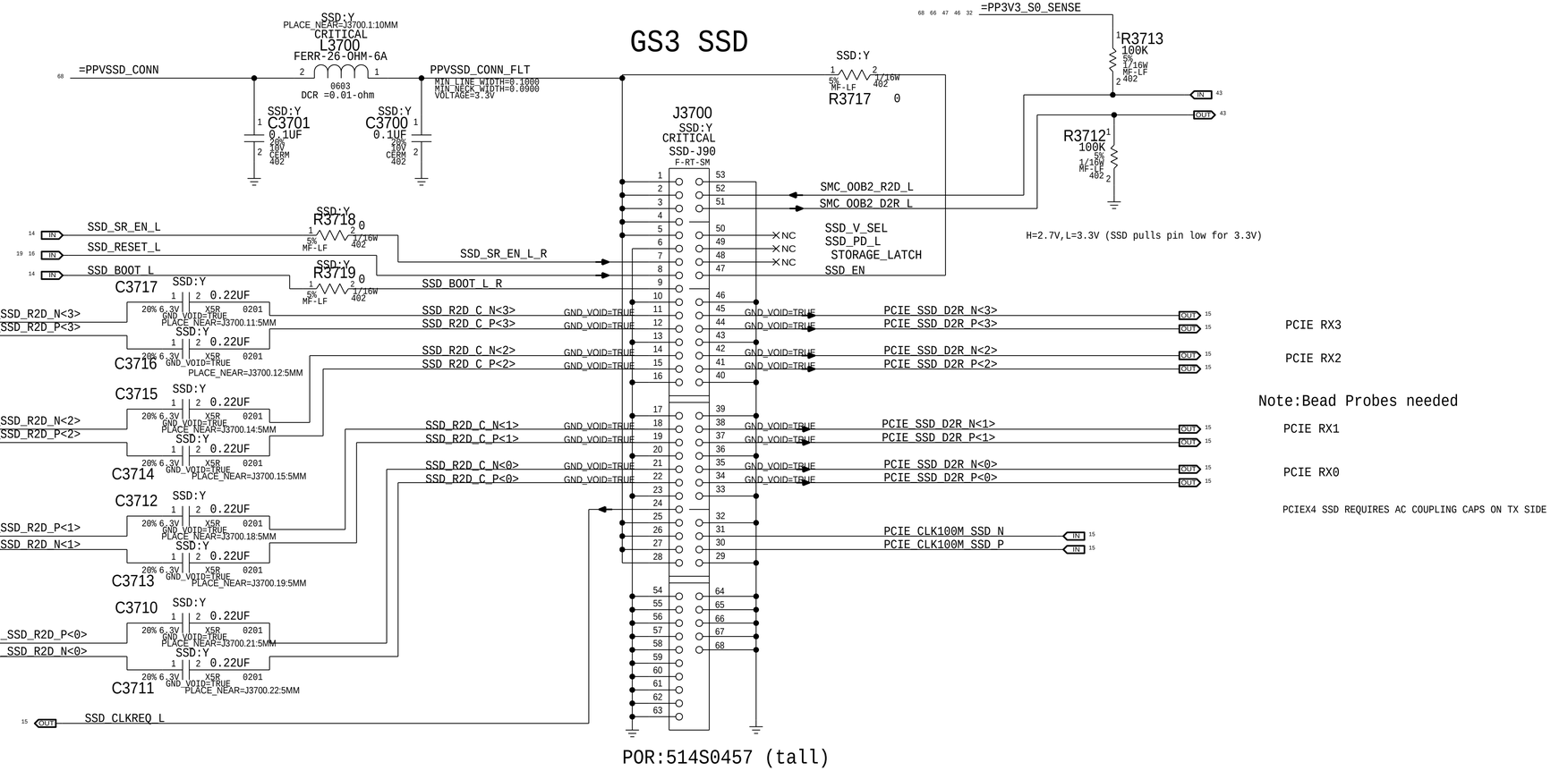
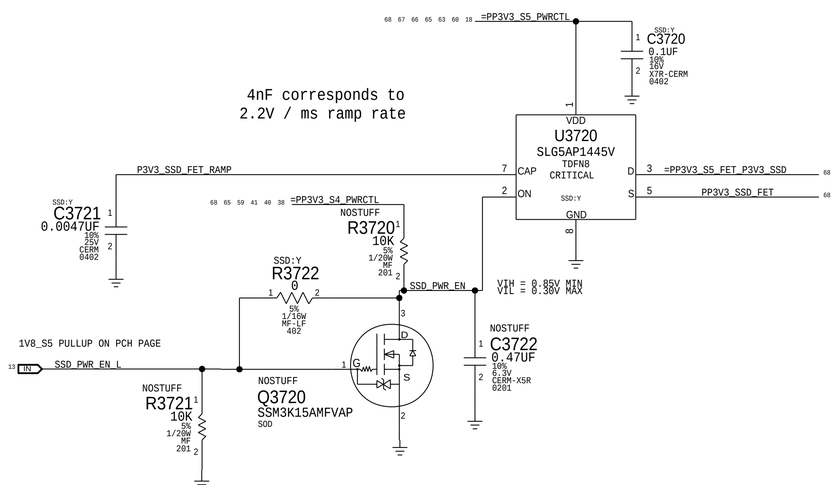
GS3 SSD



POR:514S0457 (tall)

3V3 SSD FET



BOM_COST_GROUP=SSD

SYNC_MASTER=DTUZMAN_MLB	SYNC_DATE=04/08/2016
PAGE TITLE	SSD Connectors
Apple Inc.	DRAWING NUMBER 051-01543 · SIZE D
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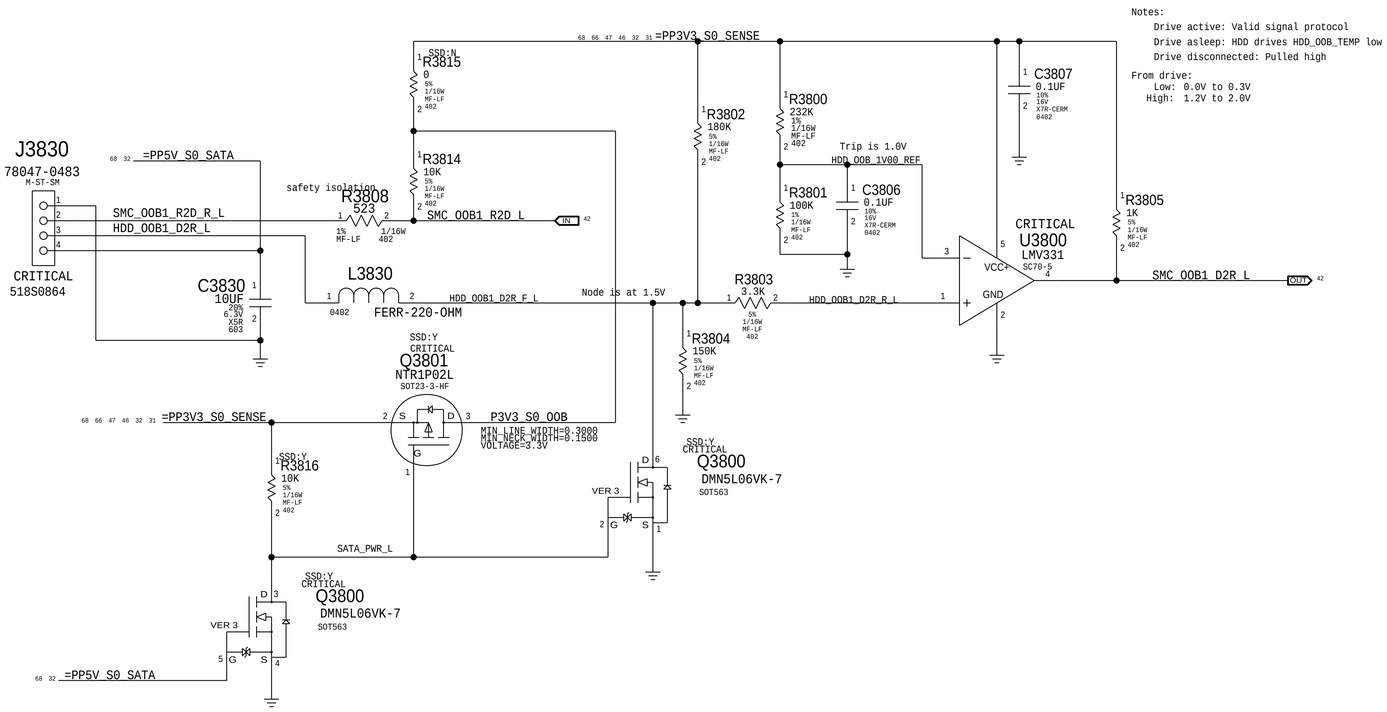
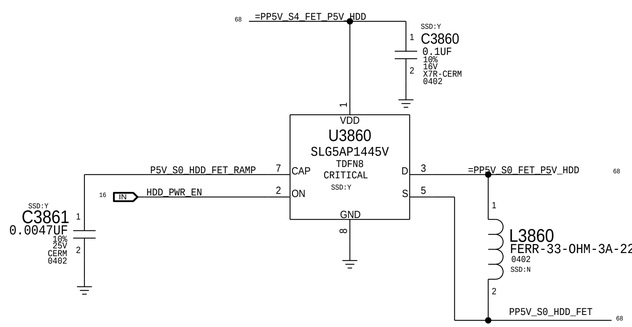
HDD POWER/OOB CONNECTOR

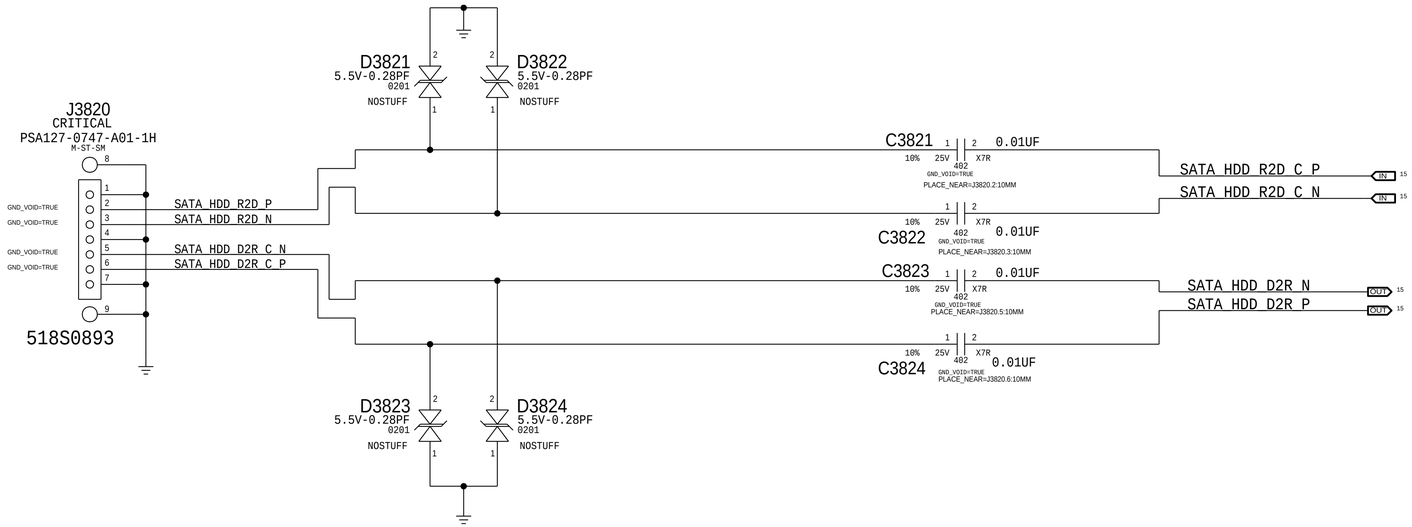
HDD Out-of-Band Temperature Sensing



5V HDD FET



HDD SIGNAL CONNECTOR



BOM_COST_GROUP=HDD

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: HDD Connector

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

BRANCH:

PAGE: 38 OF 105

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

68 34 33 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
33 =PP3V3R1V8_CR_VDDIO

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402 MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/10W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/10W MF-LF 402
R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM 402
C3916 0.1UF 10% 16V X5R-CERM 0201

ENET_SR_LX 34
=ENET_SR_VFB 34
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 34
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

42 48 37 17 20 56 62 14 15 16 13 39 45 51 29 32 36 35 61
AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

68 =PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

OMIT_TABLE
U3900 BCM57766C0KMLKG QFN-8X8

15 OUT PCIE_ENET_D2R_N — C3950 0.1UF 10% 16V X5R-CERM 0201 — 58 VMAIN_PRSNT (IPD-ENET) ENET_VMAIN_PRSNT
15 OUT PCIE_ENET_D2R_P — C3951 0.1UF 10% 16V X5R-CERM 0201 — 27 PCIE_TXD_N PCIE_ENET_D2R_C_N; 28 PCIE_TXD_P PCIE_ENET_D2R_C_P
15 IN PCIE_ENET_R2D_C_P — C3955 0.1UF 10% 16V X5R-CERM 0201 — 33 PCIE_RXD_P PCIE_ENET_R2D_P; 34 PCIE_RXD_N PCIE_ENET_R2D_N
15 IN PCIE_ENET_R2D_C_N — C3956 0.1UF 10% 16V X5R-CERM 0201 — 31 PCIE_REFCLK_P PCIE_CLK100M_ENET_P; 30 PCIE_REFCLK_N PCIE_CLK100M_ENET_N
34 OUT =ENET_WAKE_L (See note) — 3 WAKE* (OD)
35 16 IN ENET_LOW_PWR — 4 LOW_PWR (IPD)
35 IN ENET_RESET_L — 11 PERST* (IPD)
15 OUT ENETSD_CLKREQ_L — 12 CLKREQ* (OD)
SMB_ENET_SCL — 6 SMB_CLK
SMB_ENET_SDA — 10 SMB_DATA (IPD-ENETM)
33 ENET_SCLK — 66 SCLK_SPD1000LED*
33 ENET_MISO — 64 SI/EEDATA
33 ENET_MOSI — 65 SO_LINKLED*
33 ENET_CS_L — 63 CS*/EECLK
(IPU)
NC — 2 SPD100LED*/SERIAL_DO (OD)
34 OUT ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
18 IN ENET_XTAL_IN — 18 XTALI
18 OUT ENET_XTAL_OUT — 19 XTALO
ENET_RDAC — 38 RDAC
R3965 1.24K 1% 1/16W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

TRD0_P 40 ENETCONN_MDI_P<0> 34 BI
TRD0_N 41 ENETCONN_MDI_N<0> 34 BI
TRD1_P 44 ENETCONN_MDI_P<1> 34 BI
TRD1_N 43 ENETCONN_MDI_N<1> 34 BI
TRD2_P 46 ENETCONN_MDI_P<2> 34 BI
TRD2_N 47 ENETCONN_MDI_N<2> 34 BI
TRD3_P 50 ENETCONN_MDI_P<3> 34 BI
TRD3_N 49 ENETCONN_MDI_N<3> 34 BI

PP3V3R1V8_ENET_LR_OUT MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3R1V8_CR_VDDIO 33
C3980 4.7UF 20% 6.3V X5R-CERM1 402
C3981 0.1UF 10% 16V X5R-CERM 0201
C3982 0.1UF 10% 16V X5R-CERM 0201

(IPD) GPIO_0/CR_ACT_LED* 5 — NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_MEDIA_SENSE OUT 13
(IPx-ENET) SD_DETECT 0 1 — ENET_SD_DETECT_L IN 35
(IPU-ENET) CR_CMD 26 — ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — SDCONN_CMD IN 35
CR_CLK 21 — ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — SDCONN_CLK OUT 35
(IPU-ENET) CR_DATA0 25 — ENET_CR_DATA<0> — R3971 33 — SDCONN_DATA<0> BI 35
CR_DATA1 24 — ENET_CR_DATA<1> — R3972 33 — SDCONN_DATA<1> BI 35
CR_DATA2 23 — ENET_CR_DATA<2> — R3973 33 — SDCONN_DATA<2> BI 35
CR_DATA3 22 — ENET_CR_DATA<3> — R3974 33 — SDCONN_DATA<3> BI 35
CR_DATA4 52 — ENET_CR_DATA<4> — R3975 33 — SDCONN_DATA<4> BI 35
CR_DATA5 53 — ENET_CR_DATA<5> — R3976 33 — SDCONN_DATA<5> BI 35
CR_DATA6 54 — ENET_CR_DATA<6> — R3977 33 — SDCONN_DATA<6> BI 35
CR_DATA7 55 — ENET_CR_DATA<7> — R3978 33 — SDCONN_DATA<7> BI 35
(IPU-ENET) MS_INS* 59 — NC
CR_LED*/CR_BUS_PWR 60 — ENET_CR_PWREN OUT 35
CR_WP* 57 — SDCONN_WP IN 35
SR_DISABLE 68 — ENET_SR_DISABLE (See note) — R3981 1K 5% 1/16W MF-LF 402

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

ENET 1.2V SR IS ENABLED IF FLOATING.

THRM_PAD 69

ENET_SR_DISABLE
(See note)
ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

BOM_COST_GROUP=ETHERNET

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

68 34 33 =PP3V3_ENET_PHY
R3998 0 5% 1/16W MF-LF 402 NOSTUFF
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC 6 SCK 2 CS* 4 WP* 5 RESET* 3 SI 1 SO 8 GND 7
33 ENET_SCLK
33 ENET_CS_L
ENET_WP_L
ENET_MOSI 33
ENET_MISO 33
R3999 0 5% 1/16W MF-LF 402 NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402 NOSTUFF
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015
PAGE TITLE: PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-01543 SIZE D
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CAESAR IV 1.2V INT.VR CMPTS
=PP3V3_ENET_PHY
Power decoupling
C4010
4.7UF
20%
6.3V
X5R-CERM1
402
C4011
0.1UF
10%
16V
X7R-CERM
0402
ENET_SR_LX
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE
CRITICAL
L4010
4.7UH-0.8A
PCAA031B-SM
C4012
10UF
20%
6.3V
X5R
603
C4013
0.1UF
10%
16V
X7R-CERM
0402
Feedback loop
PP1V2_ENET_INTREG
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_ENET_PHY
=ENET_SR_VFB
ENET Enable Generation
ENET is enabled when in S0 or when (S4 & WOL_EN) is present
3.3V ENET FET
CRITICAL
Q4020
NTR4101P
SOT-23-HF
=PP3V3_S4_FET_ENET
PP3V3_ENET_FET
R4020
10K
5%
1/16W
MF-LF
402
C4020
0.033UF
10%
16V
X5R
402
R4021
100K
5%
1/16W
MF-LF
402
C4021
0.01UF
10%
25V
X7R
402
PM_EN_ENET_L
P3V3ENET_SS
CRITICAL
Q4021
DMN5L06VK-7
SOT563
VER 3
WOL_EN
PM_SLP_S3_L
CAESAR IV ACTIVITY LED
=PP3V3_ENET_PHY
DEVELOPMENT
R4050
330
5%
1/16W
MF-LF
402
ENET_ACT
DEVELOPMENT
LED4050
GRN-GMCD-0.03A
0805
ENET_TRAFFICLED_L
CAESAR IV WAKE# ISOLATION
=PP3V3_ENET_PHY
R4070
10K
5%
1/16W
MF-LF
402
PCIE_WAKE_L
ENET_WAKE_L
MAKE_BASE=TRUE
=ENET_WAKE_L
Q4070
SSM3K15AMFVAP
SOD
157S00005
T4000
LC607-AP
SM
155S00056
L4000
370-OHM
HCMC0805-4SM
ENETCONN_MDI_N<2>
ENETCONN_MDI_X_N<2>
ENETCONN_MCT2
ENETCONN_MDI_P<2>
ENETCONN_MDI_X_P<2>
ENETCONN_MDI_T_N<2>
ENETCONN_MDI_T_P<2>
T4005
LC607-AP
SM
L4005
370-OHM
HCMC0805-4SM
ENETCONN_MDI_N<0>
ENETCONN_MDI_X_N<0>
ENETCONN_MCT0
ENETCONN_MDI_P<0>
ENETCONN_MDI_X_P<0>
ENETCONN_MDI_T_N<0>
ENETCONN_MDI_T_P<0>
T4020
LC607-AP
SM
L4020
370-OHM
HCMC0805-4SM
ENETCONN_MDI_P<1>
ENETCONN_MDI_X_P<1>
ENETCONN_MCT1
ENETCONN_MDI_N<1>
ENETCONN_MDI_X_N<1>
ENETCONN_MDI_T_P<1>
ENETCONN_MDI_T_N<1>
T4025
LC607-AP
SM
L4025
370-OHM
HCMC0805-4SM
ENETCONN_MDI_P<3>
ENETCONN_MDI_X_P<3>
ENETCONN_MCT3
ENETCONN_MDI_N<3>
ENETCONN_MDI_X_N<3>
ENETCONN_MDI_T_P<3>
ENETCONN_MDI_T_N<3>
514-0822
CRITICAL
J4000
K70-K72
F-ANG-TH
ENET_MDI
ENET_MDI_TRAN3-
ENET_MDI_TRAN3+
ENET_MDI_TRAN1-
ENET_MDI_TRAN2-
ENET_MDI_TRAN2+
ENET_MDI_TRAN1+
ENET_MDI_TRAN0-
ENET_MDI_TRAN0+
SHIELD
PINS
ENETCONN_TCT
C4001
0.1UF
C4002
0.1UF
C4003
0.1UF
C4004
0.1UF
20%
10V
CERM
402
ENETCONN_MCT2
ENETCONN_MCT0
ENETCONN_MCT1
ENETCONN_MCT3
R4000
75
R4001
75
R4002
75
R4003
75
5%
1/20W
MF
201
ENETCONN_MCT_SS
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
C4000
1000PF
10%
3KV
X7R
1808
BOM_COST_GROUP=ETHERNET

SYNC_MASTER=J134_MLB SYNC_DATE=06/09/2016

PAGE TITLE

Ethernet Support & Connector

Apple Inc.

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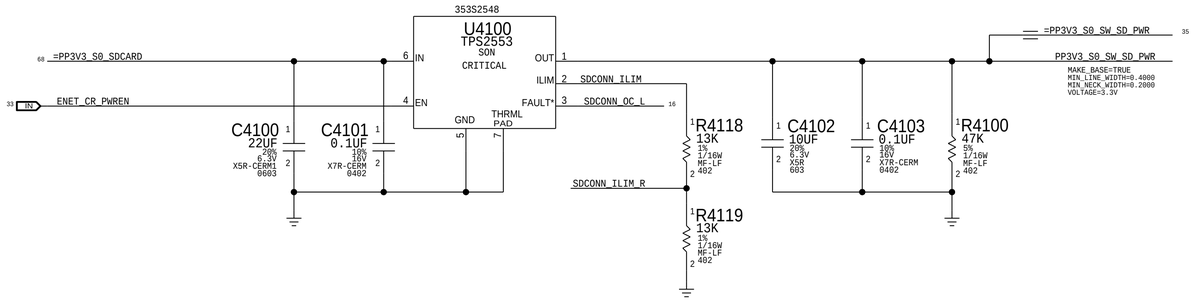
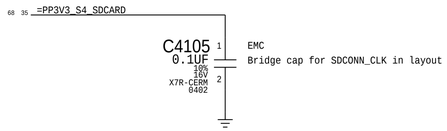
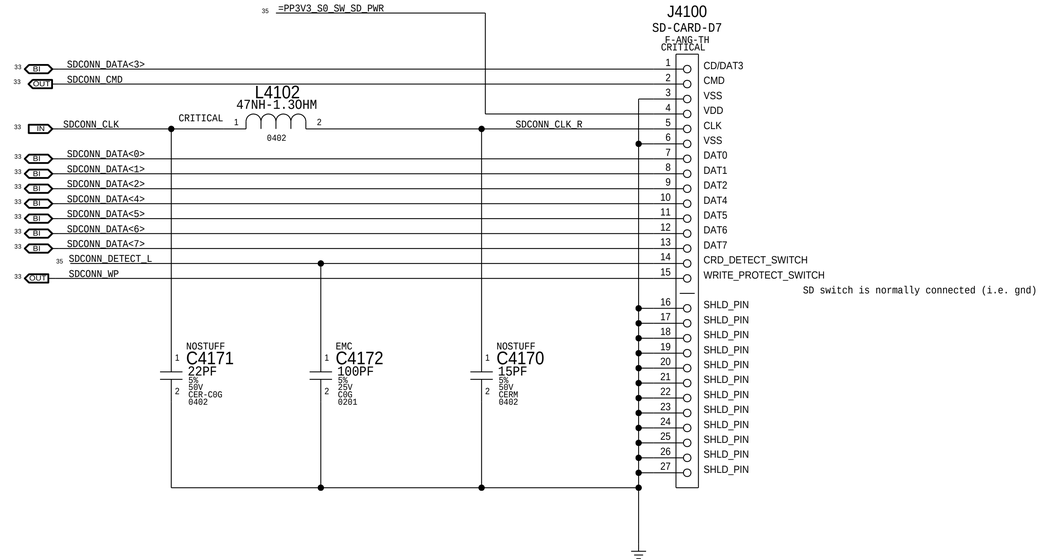
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



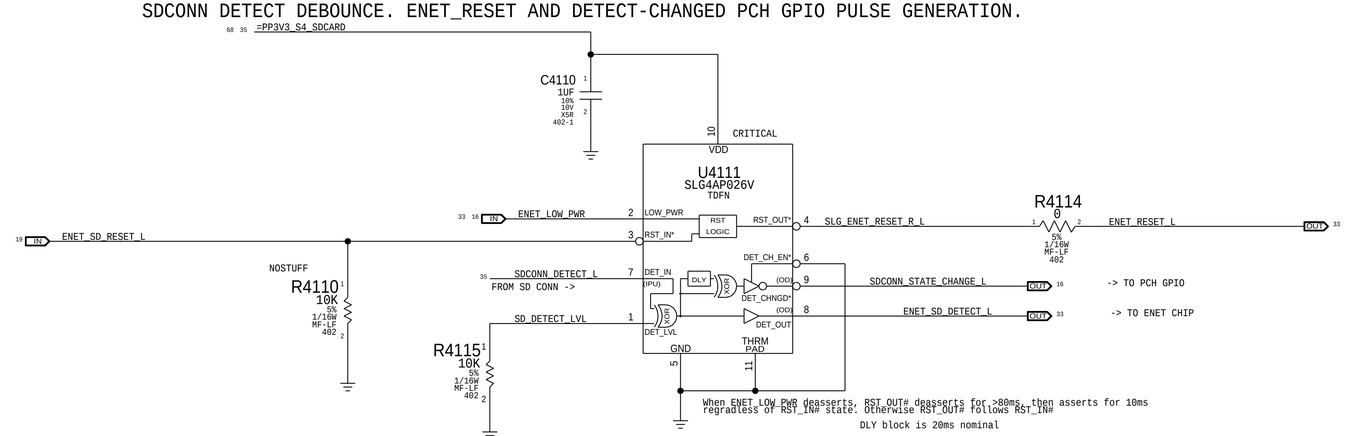


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



BOM_COST_GROUP=SD CARD

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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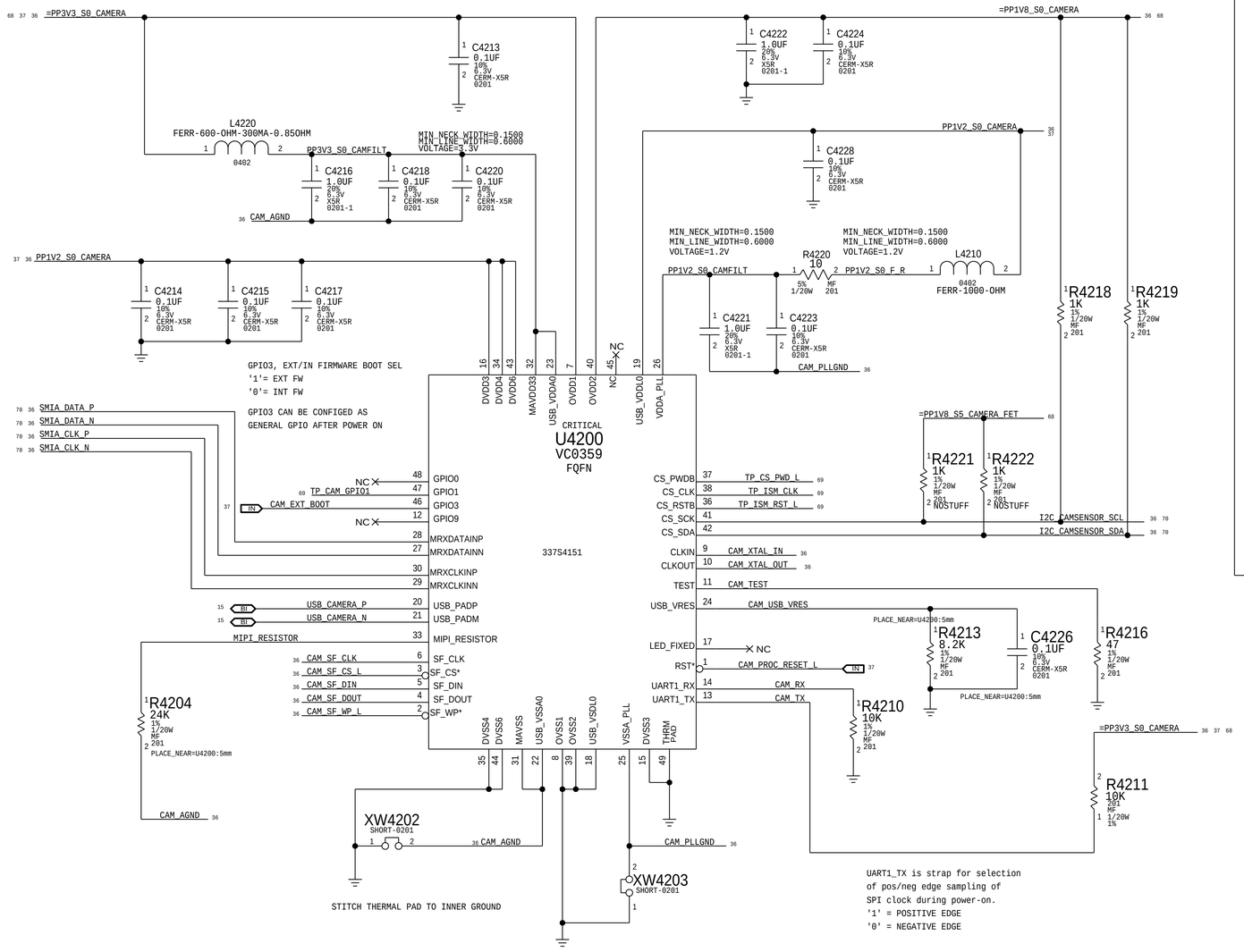
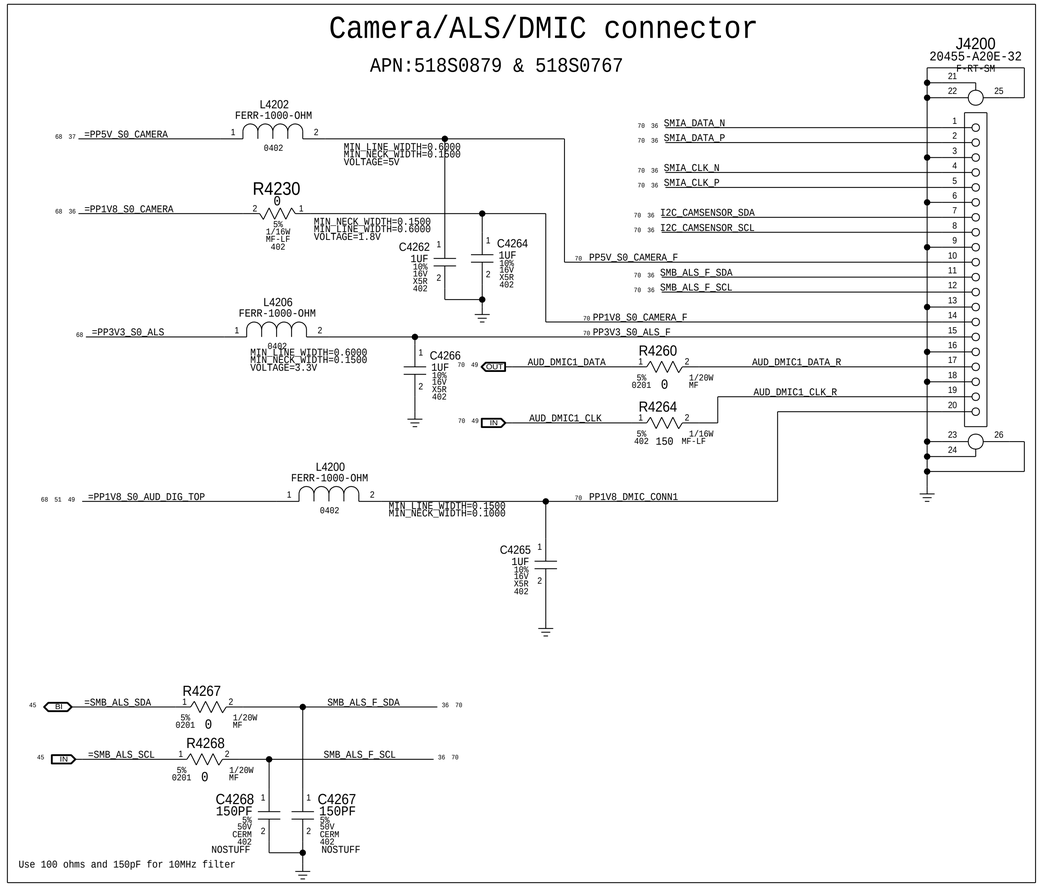
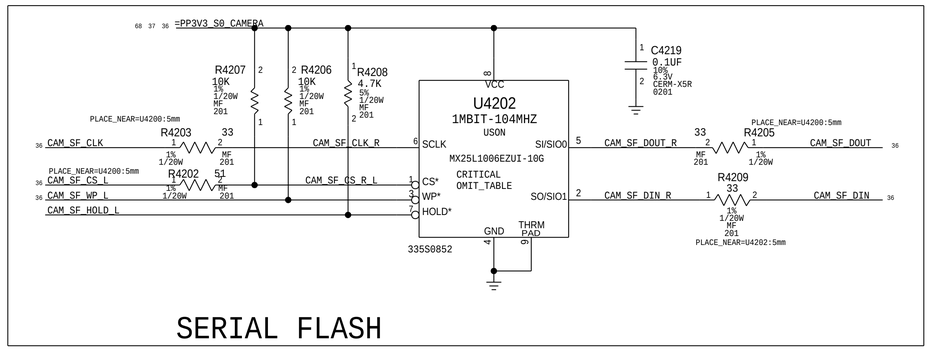
USB CAMERA CONTROLLER



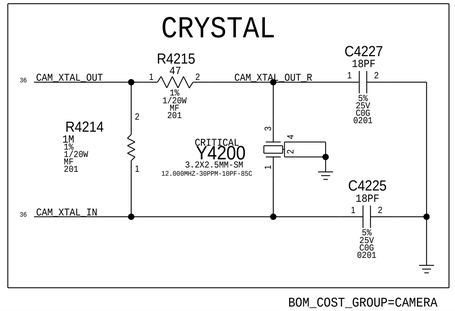
Camera/ALS/DMIC connector

APN:518S0879 & 518S0767





SERIAL FLASH



SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=08/26/2016

PAGE TITLE

Camera Controller

Apple Inc.

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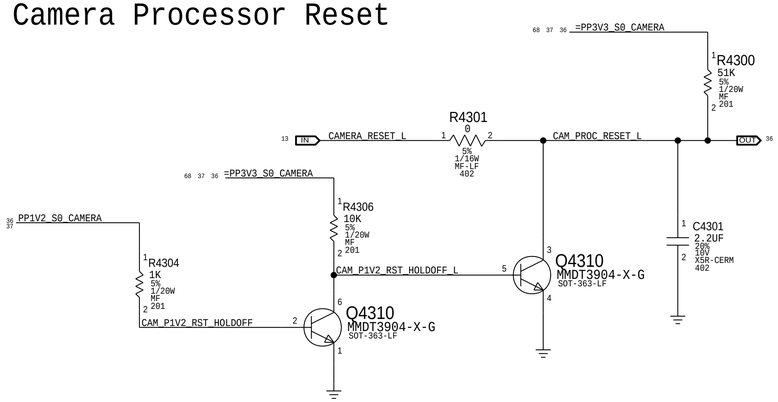
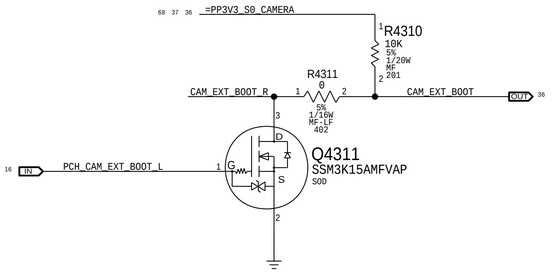
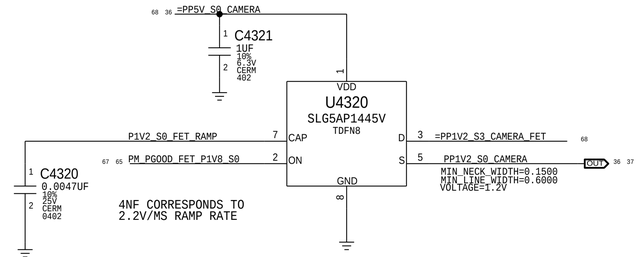
Camera Processor Reset



Camera Processor ExtBoot Cntl



1.2V S0 LOAD SWITCH



BOM_COST_GROUP=CAMERA

SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=04/26/2016

PAGE TITLE: Camera Controller Support

Apple Inc.

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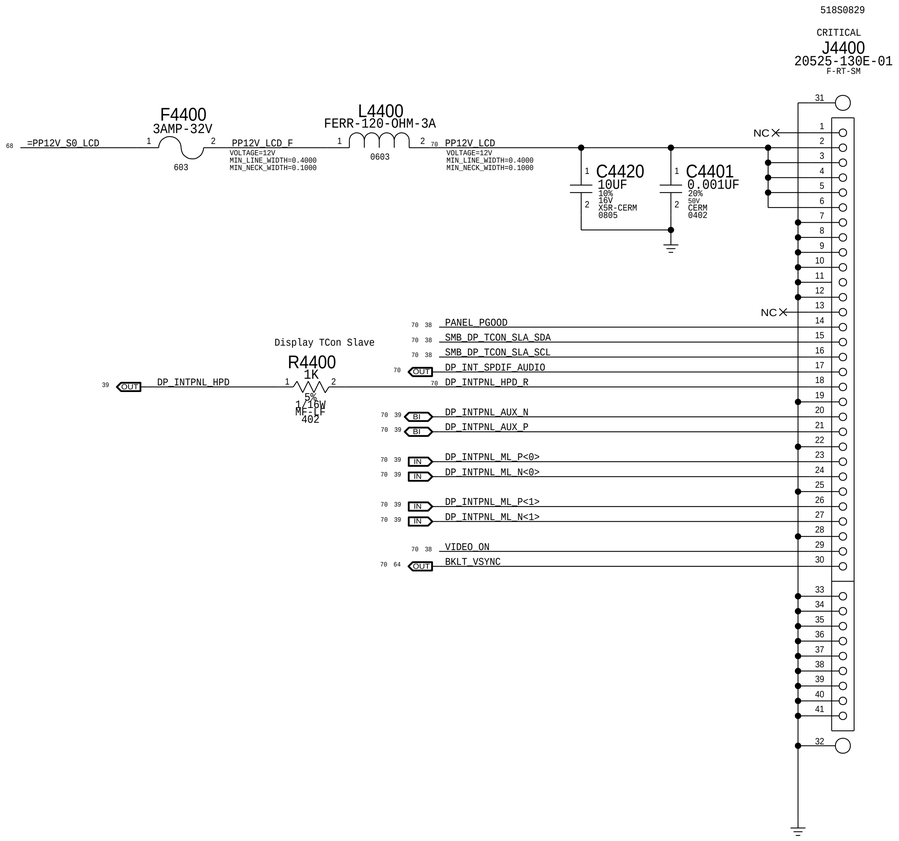
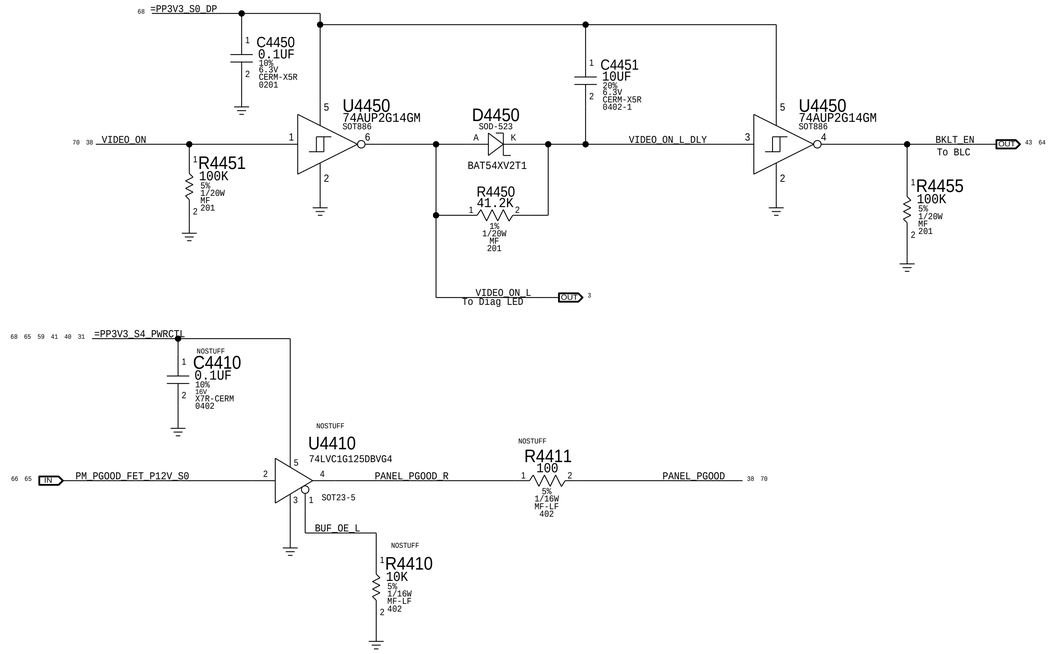
Internal DP Connector

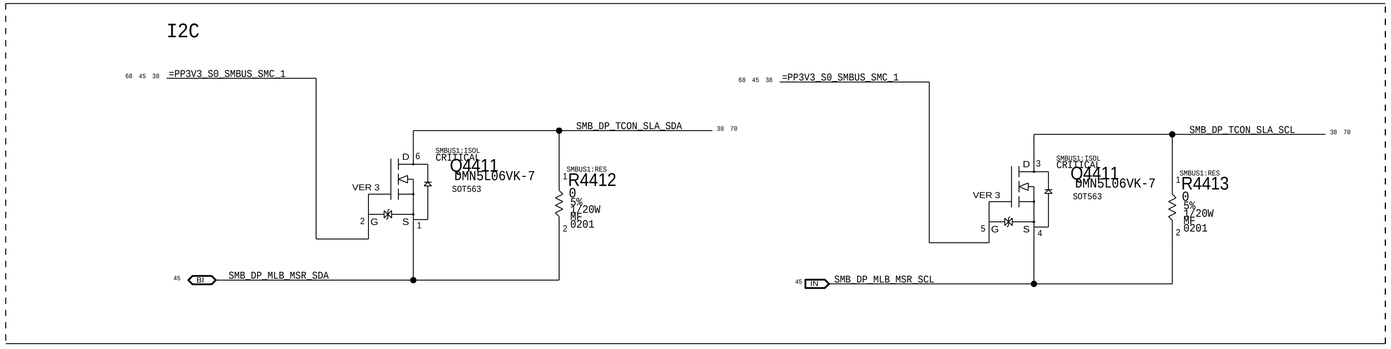


Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video



SMBus Isolation



BOM_COST_GROUP=DISPLAY

SYNC_MASTER=AARON_MLB SYNC_DATE=04/15/2016

PAGE TITLE: Internal DP Support

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

BRANCH:

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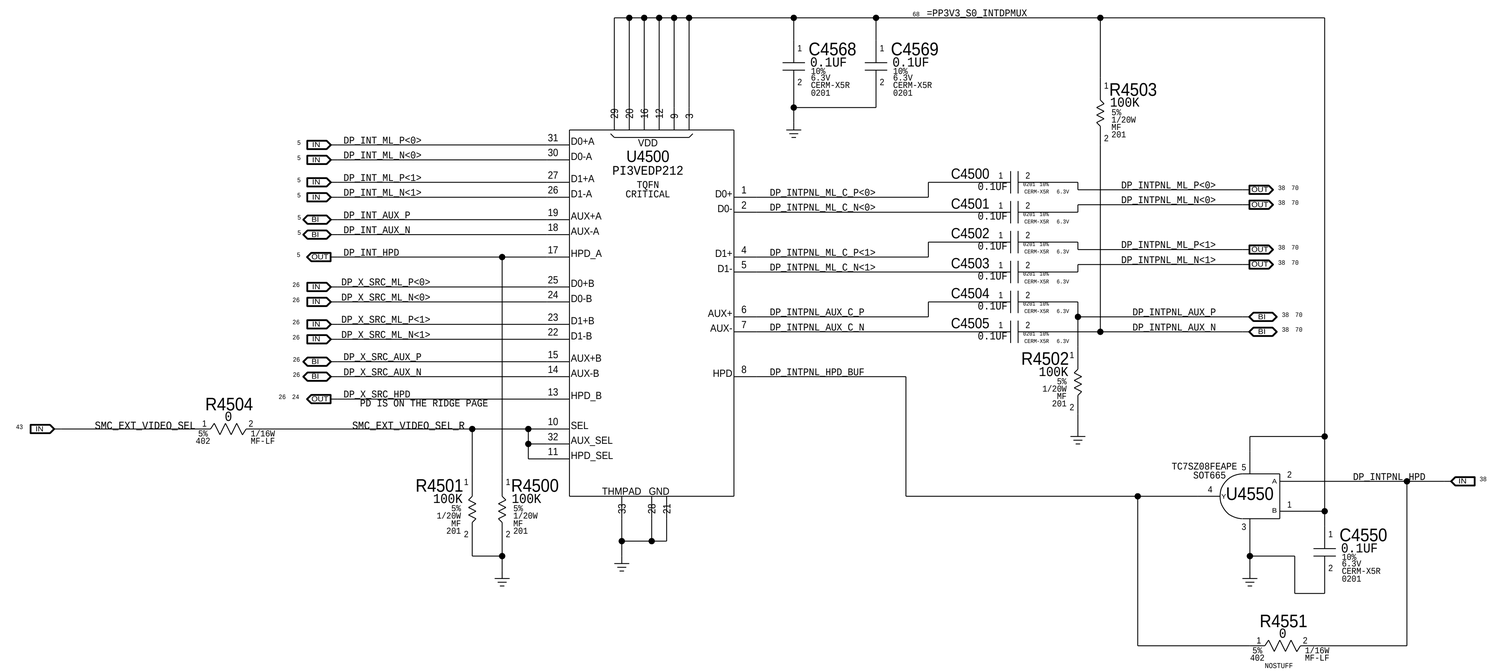
NC aliases

24	IN	=DP_X_SRC_ML_P<2>	NC_DP_TBTSRC_ML_P<2>	NO_TEST=1, MAKE_BASE=TRUE
24	IN	=DP_X_SRC_ML_N<2>	NC_DP_TBTSRC_ML_N<2>	NO_TEST=1, MAKE_BASE=TRUE
24	IN	=DP_X_SRC_ML_P<3>	NC_DP_TBTSRC_ML_P<3>	NO_TEST=1, MAKE_BASE=TRUE
24	IN	=DP_X_SRC_ML_N<3>	NC_DP_TBTSRC_ML_N<3>	NO_TEST=1, MAKE_BASE=TRUE
5	IN	DP_INT_ML_P<2>	NC_DP_INT_ML_P<2>	NO_TEST=1, MAKE_BASE=TRUE
5	IN	DP_INT_ML_N<2>	NC_DP_INT_ML_N<2>	NO_TEST=1, MAKE_BASE=TRUE
5	IN	DP_INT_ML_P<3>	NC_DP_INT_ML_P<3>	NO_TEST=1, MAKE_BASE=TRUE
5	IN	DP_INT_ML_N<3>	NC_DP_INT_ML_N<3>	NO_TEST=1, MAKE_BASE=TRUE



BOM_COST_GROUP=DISPLAY

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: Internal DP MUXing

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

REVISION: 3.13.0

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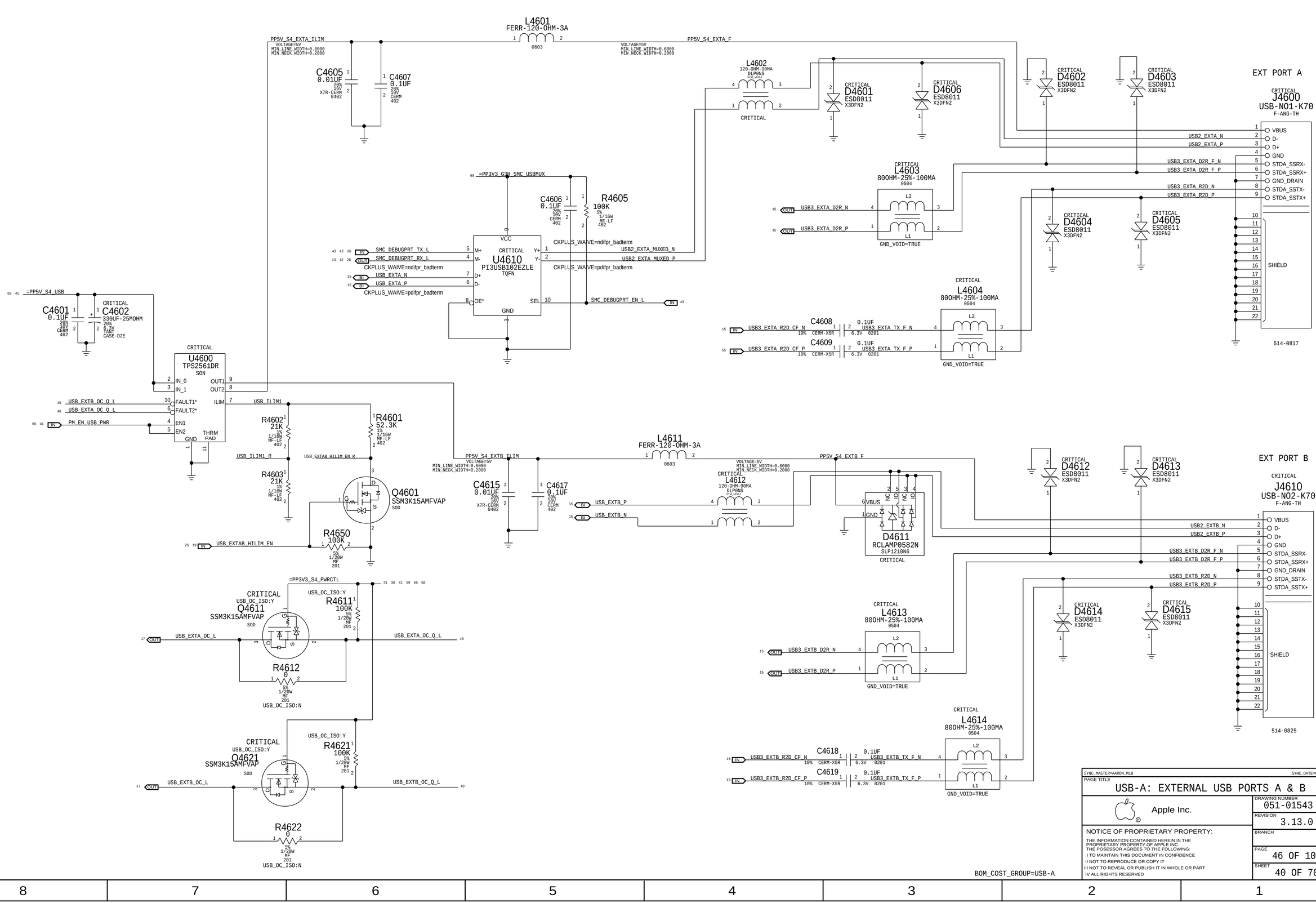
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
C4605
0.01UF
20%
16V
X7R-CERM
0402
C4607
0.1UF
20%
10V
CERM
402
PP5V_S4_EXTA_F
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
ESD8011
X3DFN2
D4606
ESD8011
X3DFN2
D4602
ESD8011
X3DFN2
D4603
ESD8011
X3DFN2
EXT PORT A
J4600
USB-NO1-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_D2R_F_N
USB3_EXTA_D2R_F_P
USB3_EXTA_R2D_N
USB3_EXTA_R2D_P
L4603
80OHM-25%-100MA
0504
GND_VOID=TRUE
D4604
ESD8011
X3DFN2
D4605
ESD8011
X3DFN2
C4606
0.1UF
20%
10V
CERM
402
R4605
100K
5%
1/16W
MF-LF
402
=PP3V3_G3H_SMC_USBMUX
VCC
U4610
PI3USB102EZLE
TQFN
GND
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_N
USB_EXTA_P
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U4600
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
GND
THRM PAD
ILIM
OUT1
OUT2
USB_EXTB_OC_Q_L
USB_EXTA_OC_Q_L
PM_EN_USB_PWR
USB_ILIM1
R4602
21K
R4601
52.3K
USB_ILIM1_R
USB_EXTAB_HILIM_EN_R
R4603
21K
Q4601
SSM3K15AMFVAP
SOD
R4650
100K
USB_EXTAB_HILIM_EN
L4604
80OHM-25%-100MA
0504
C4608
0.1UF
C4609
0.1UF
USB3_EXTA_R2D_CF_N
USB3_EXTA_R2D_CF_P
USB3_EXTA_TX_F_N
USB3_EXTA_TX_F_P
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_ILIM
PP5V_S4_EXTB_F
C4615
0.01UF
C4617
0.1UF
L4612
120-OHM-90MA
DLP0NS
USB_EXTB_P
USB_EXTB_N
D4611
RCLAMP0582N
SLP1210N6
EXT PORT B
J4610
USB-NO2-K70
F-ANG-TH
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_D2R_F_N
USB3_EXTB_D2R_F_P
USB3_EXTB_R2D_N
USB3_EXTB_R2D_P
514-0825
D4612
ESD8011
X3DFN2
D4613
ESD8011
X3DFN2
D4614
ESD8011
X3DFN2
D4615
ESD8011
X3DFN2
L4613
80OHM-25%-100MA
0504
L4614
80OHM-25%-100MA
0504
C4618
0.1UF
C4619
0.1UF
USB3_EXTB_R2D_CF_N
USB3_EXTB_R2D_CF_P
USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P
=PP3V3_S4_PWRCTL
Q4611
SSM3K15AMFVAP
R4611
100K
R4612
0
USB_OC_ISO:Y
USB_OC_ISO:N
USB_EXTA_OC_L
USB_EXTA_OC_Q_L
Q4621
SSM3K15AMFVAP
R4621
100K
R4622
0
USB_EXTB_OC_L
USB_EXTB_OC_Q_L
BOM_COST_GROUP=USB-A
SYNC_MASTER=AARON_MLB
SYNC_DATE=07/29/2016
PAGE TITLE
USB-A: EXTERNAL USB PORTS A & B
Apple Inc.
DRAWING NUMBER
051-01543
SIZE
D
REVISION
3.13.0
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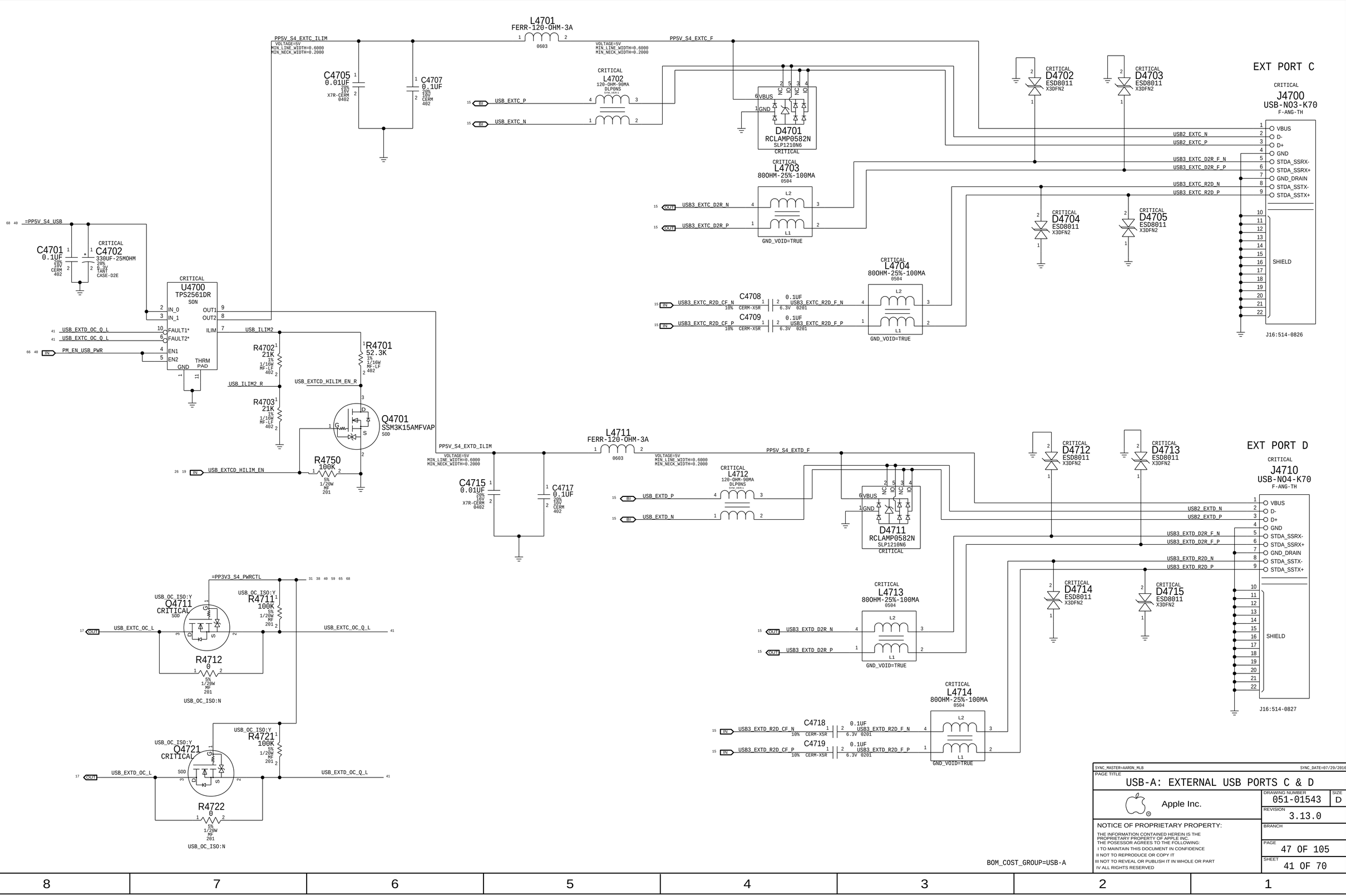
L4701
FERR-120-OHM-3A
0603
PP5V_S4_EXTC_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
PP5V_S4_EXTC_F
C4705
0.01UF
20%
16V
X7R-CERM
0402
C4707
0.1UF
20%
10V
CERM
402
CRITICAL
L4702
120-OHM-90MA
DLP0NS
USB_EXTC_P
USB_EXTC_N
CRITICAL
D4701
RCLAMP0582N
SLP1210N6
CRITICAL
D4702
ESD8011
X3DFN2
D4703
ESD8011
X3DFN2
EXT PORT C
CRITICAL
J4700
USB-NO3-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
J16:514-0826
USB2_EXTC_N
USB2_EXTC_P
USB3_EXTC_D2R_F_N
USB3_EXTC_D2R_F_P
USB3_EXTC_R2D_N
USB3_EXTC_R2D_P
CRITICAL
L4703
80OHM-25%-100MA
0504
USB3_EXTC_D2R_N
USB3_EXTC_D2R_P
GND_VOID=TRUE
D4704
D4705
C4708
0.1UF
USB3_EXTC_R2D_CF_N
USB3_EXTC_R2D_F_N
C4709
USB3_EXTC_R2D_CF_P
USB3_EXTC_R2D_F_P
CRITICAL
L4704
80OHM-25%-100MA
0504
=PP5V_S4_USB
C4701
0.1UF
C4702
330UF-25MOHM
CASE-D2E
CRITICAL
U4700
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
EN1
EN2
GND
THRM PAD
ILIM
USB_EXTD_OC_Q_L
USB_EXTC_OC_Q_L
PM_EN_USB_PWR
USB_ILIM2
R4702
21K
R4701
52.3K
USB_ILIM2_R
USB_EXTCD_HILIM_EN_R
R4703
21K
Q4701
SSM3K15AMFVAP
SOD
R4750
100K
USB_EXTCD_HILIM_EN
L4711
FERR-120-OHM-3A
0603
PP5V_S4_EXTD_ILIM
PP5V_S4_EXTD_F
C4715
0.01UF
C4717
0.1UF
CRITICAL
L4712
120-OHM-90MA
DLP0NS
USB_EXTD_P
USB_EXTD_N
CRITICAL
D4711
RCLAMP0582N
SLP1210N6
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D4712
ESD8011
X3DFN2
D4713
ESD8011
X3DFN2
EXT PORT D
CRITICAL
J4710
USB-NO4-K70
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
J16:514-0827
USB2_EXTD_N
USB2_EXTD_P
USB3_EXTD_D2R_F_N
USB3_EXTD_D2R_F_P
USB3_EXTD_R2D_N
USB3_EXTD_R2D_P
CRITICAL
L4713
80OHM-25%-100MA
0504
USB3_EXTD_D2R_N
USB3_EXTD_D2R_P
GND_VOID=TRUE
D4714
D4715
C4718
0.1UF
USB3_EXTD_R2D_CF_N
USB3_EXTD_R2D_F_N
C4719
USB3_EXTD_R2D_CF_P
USB3_EXTD_R2D_F_P
CRITICAL
L4714
80OHM-25%-100MA
0504
=PP3V3_S4_PWRCTL
USB_OC_ISO:Y
Q4711
CRITICAL
SOD
R4711
100K
USB_EXTC_OC_L
USB_EXTC_OC_Q_L
R4712
0
USB_OC_ISO:N
Q4721
CRITICAL
SOD
R4721
100K
USB_EXTD_OC_L
USB_EXTD_OC_Q_L
R4722
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SYNC_MASTER=AARON_MLB
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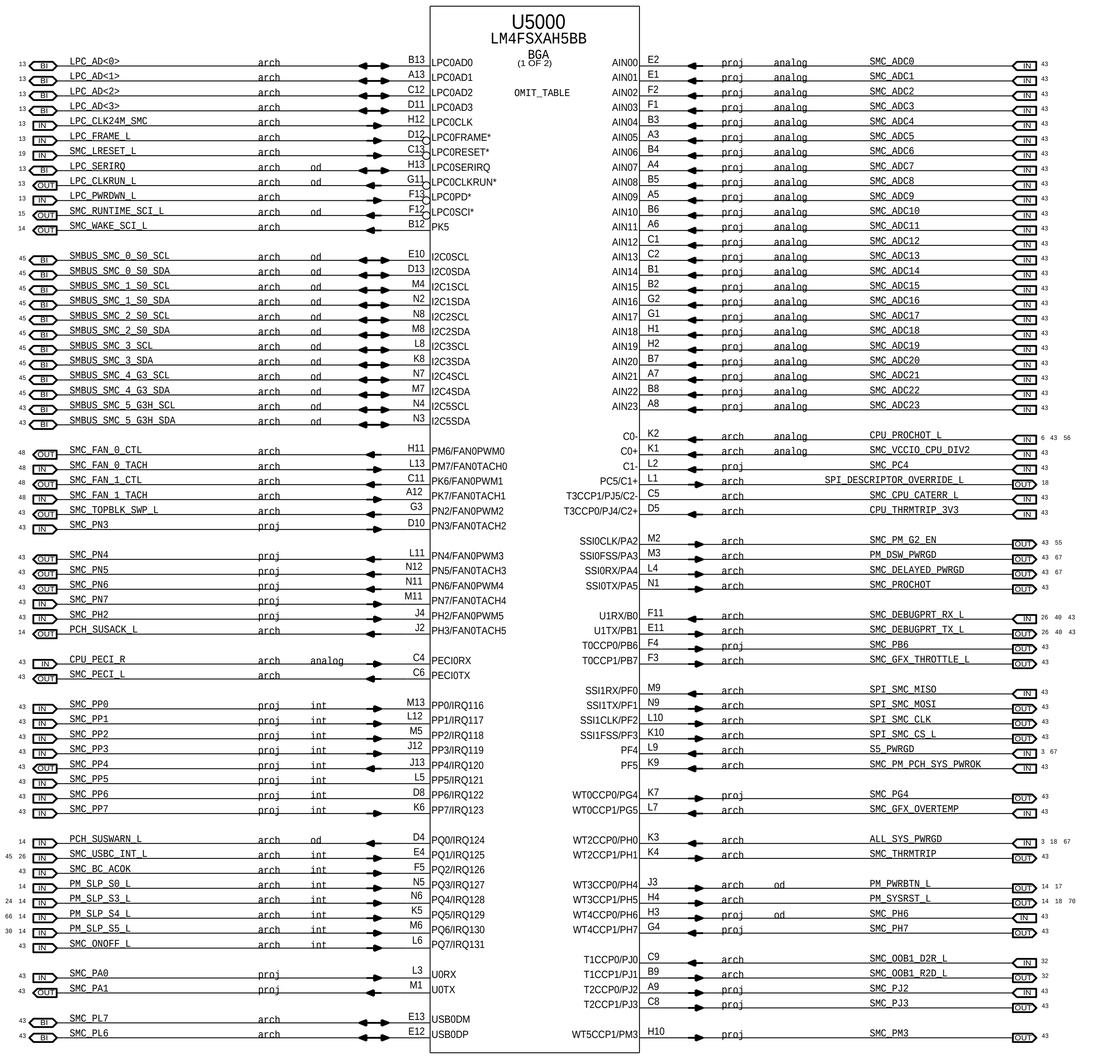
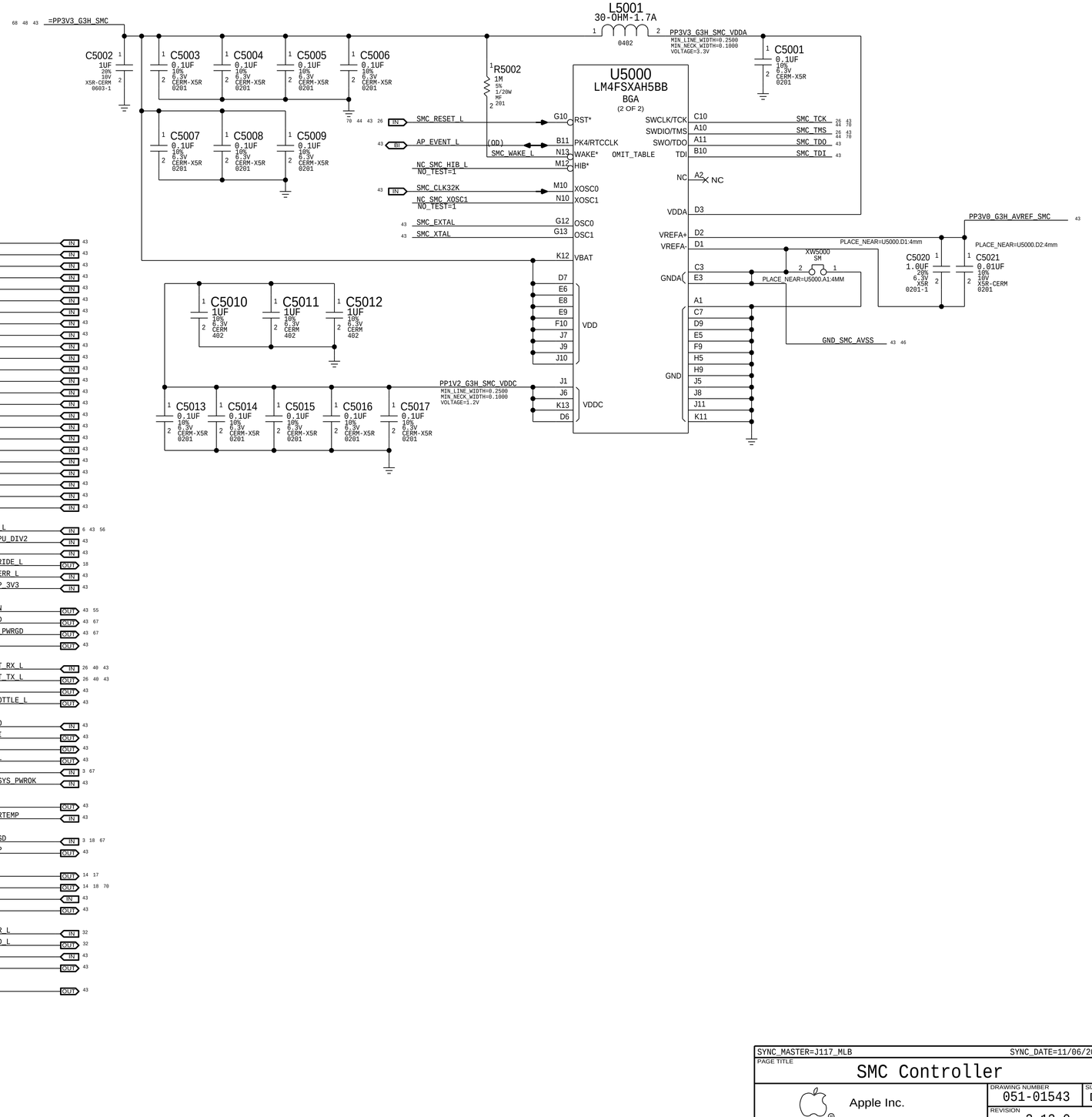
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





BOM_COST_GROUP=SMC

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: SMC Controller

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

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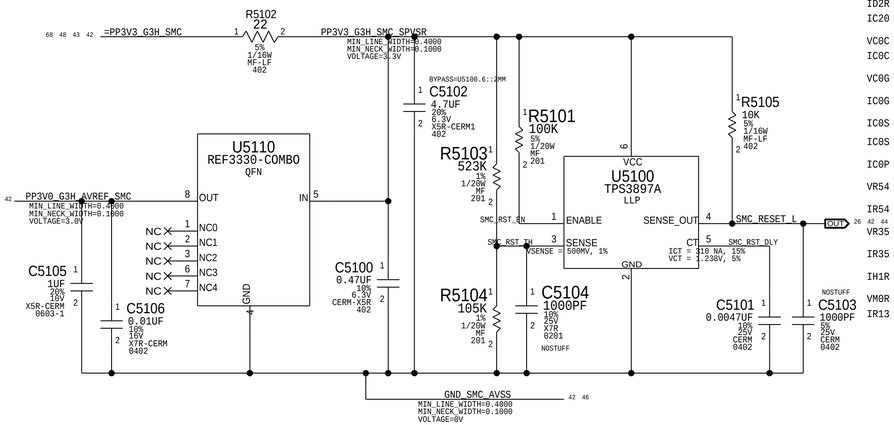
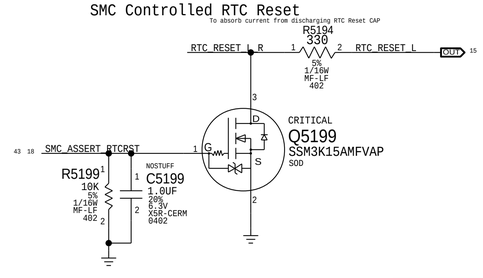
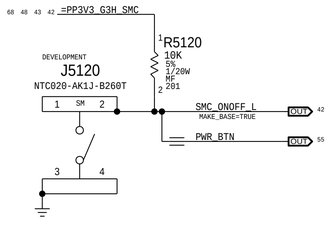
SMC Supervisor and AVREF Supply



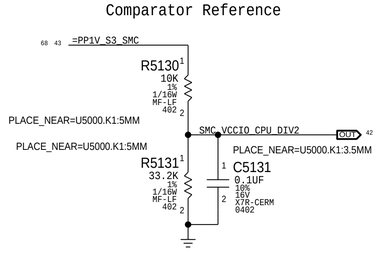
SMC Controlled RTC Reset



Power Button

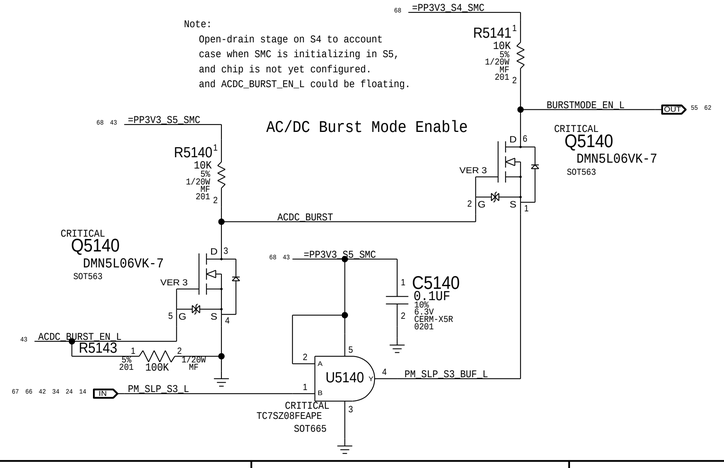


Comparator Reference



AC/DC Burst Mode Enable

Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.



ADC Channel Aliases

VD2R	SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
ID2R	SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
IC20	SMC_ADC3	ISNS_P12VS0_CPUCORE	MAKE_BASE=TRUE
VC0C	SMC_ADC4	VSNS_CPUVCC	MAKE_BASE=TRUE
IC0C	SMC_ADC5	ISNS_CPUVCC	MAKE_BASE=TRUE
VC0G	SMC_ADC6	VSNS_CPUVCC_GT	MAKE_BASE=TRUE
IC0G	SMC_ADC7	ISNS_CPUVCC_GT	MAKE_BASE=TRUE
IC0S	SMC_ADC9	ISNS_OPC_VCC1V0	MAKE_BASE=TRUE
IC0S	SMC_ADC10	ISNS_CPUVCC_SA	MAKE_BASE=TRUE
IC0P	SMC_ADC11	ISNS_PCH_VCC1V0	MAKE_BASE=TRUE
VR54	SMC_ADC16	VSNS_P5VS4	MAKE_BASE=TRUE
IR54	SMC_ADC17	ISNS_P5VS4	MAKE_BASE=TRUE
VR35	SMC_ADC18	VSNS_P3V3S5	MAKE_BASE=TRUE
IR35	SMC_ADC19	ISNS_P3V3S5	MAKE_BASE=TRUE
IH1R	SMC_ADC21	ISNS_SSD_S4	MAKE_BASE=TRUE
VM0R	SMC_ADC22	VSNS_P1V2_S3_DDR	MAKE_BASE=TRUE
IR13	SMC_ADC23	ISNS_P1V2_S3_DDR	MAKE_BASE=TRUE

Unused ADC Channels

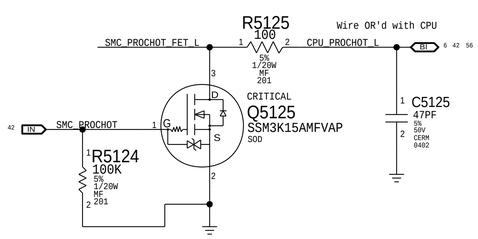
SMC_ADC2	NC_ISNS_P12VS0_GPU	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC8	NC_VSNS_FBVDDQ	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC12	NC_VSNS_CPU_VDDCI	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC13	NC_ISNS_GPU_VDDCI	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC14	NC_VSNS_CPU_VDDCI	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC15	NC_ISNS_GPU_VDDCI	MAKE_BASE=TRUE	NO_TEST=1
SMC_ADC20	NC_ISNS_P5VS4_USB	MAKE_BASE=TRUE	NO_TEST=1

SPI_SMC_MISO	NC_SPI_SMC_MISO	MAKE_BASE=TRUE	NO_TEST=1
SPI_SMC_MOSI	NC_SPI_SMC_MOSI	MAKE_BASE=TRUE	NO_TEST=1
SPI_SMC_CLK	NC_SPI_SMC_CLK	MAKE_BASE=TRUE	NO_TEST=1
SPI_SMC_CS_L	NC_SPI_SMC_CS_L	MAKE_BASE=TRUE	NO_TEST=1

Platform Thermal Control

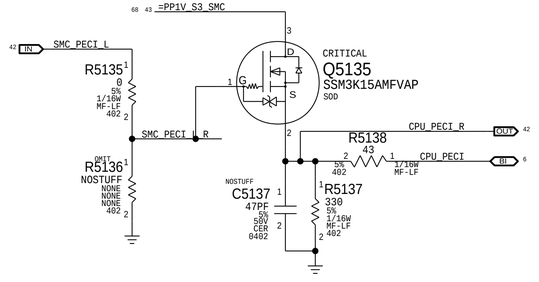
PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT



PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



Unused Project-specific

SMC_PH7	NC_GFX_OK_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN4	NC_SMC_GFX_ALERT	MAKE_BASE=TRUE	NO_TEST=1
SMC_PN6	NC_SMC_G3_WAKESRC_EN	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP3	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP5	NC_SMC_HI_PWR_GFX	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=1
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=1
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE	NO_TEST=1
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE	NO_TEST=1
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1

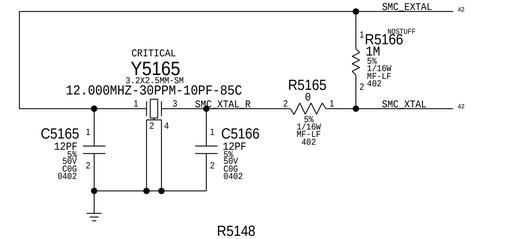
Project-specific Aliases

SMC_PA0	SMC_DEBUGPRT2_RX_L	MAKE_BASE=TRUE	26 43
SMC_PA1	SMC_DEBUGPRT2_TX_L	MAKE_BASE=TRUE	26 43
SMC_PC4	MEM_OK	MAKE_BASE=TRUE	3 8 14
SMC_PG4	SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE	40
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE	18 43
SMC_PH6	MEM_EVENT_L	MAKE_BASE=TRUE	22 23 43
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE	31
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE	31
SMC_PL6	=SMC_WIFI_PWR_EN	AP_PWR_EN MAKE_BASE=TRUE	30 43
SMC_PL7	SMC_BT_PWR_EN	MAKE_BASE=TRUE	30 43
SMC_PM3	PSU_OCP_ACTIVE	MAKE_BASE=TRUE	43
SMC_PN3	=TCON_BLC_EN	BKLT_EN MAKE_BASE=TRUE	38 64
SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE	43
SMC_PN7	DP_LINK_OK	MAKE_BASE=TRUE	19
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE	55 70
SMC_PP1	PM_EPO_L	MAKE_BASE=TRUE	43 55
SMC_PP2	SMC_PME_S4_WAKE_L	MAKE_BASE=TRUE	30 43
SMC_PB6	SMC_EXT_VIDEO_SEL	MAKE_BASE=TRUE	39

SMC 32KHz Clock

SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



R5148	0	PM_PCH_SYS_PWROK	SMC_PM_PCH_SYS_PWROK
R5149	0	CPU_CATERR_L	SMC_CPU_CATERR_L
R5154	1K	SMC_TOPBLK_SWP_L	PCH_STRP_TOPBLK_SWP_L

Arch Pull Up/Down

SMC_TOPBLK_SWP_L	R5171	1K	=PP3V3_S0_SMC
SMC_BC_ACOK	R5178	100K	=PP3V3_G3H_SMC
SMC_PME_S4_WAKE_L	R5181	10K	
AP_EVENT_L	R5185	10K	=PP3V3_S4_AP
SMC_DELAYED_PWRGD	R5186	100K	
PM_DSW_PWRGD	R5184	100K	
SMC_PM_G2_EN	R5187	100K	

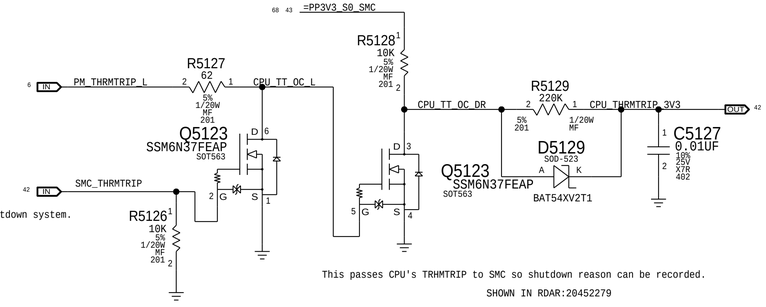
PROJ PULL UP/DOWN

MEM_EVENT_L	R5170	100K	=PP3V3_S0_SMC
PM_EPO_L	R5182	100K	=PP3V3_G3H_SMC NOSTUFF
AP_PWR_EN	R5142	100K	
SMC_BT_PWR_EN	R5119	100K	
PSU_OCP_ACTIVE	R5183	100K	

Serial/JTAG Interface Pull-ups

SMC_DEBUGPRT_TX_L	R5192	20K	
SMC_DEBUGPRT_RX_L	R5193	20K	
SMC_DEBUGPRT2_TX_L	R5190	10K	=PP3V3_G3H_SMC
SMC_DEBUGPRT2_RX_L	R5191	100K	
SMC_TCK	R5195	10K	
SMC_TDI	R5196	10K	
SMC_TDO	R5197	10K	
SMC_TMS	R5198	10K	

AC/DC Burst Mode Enable



BOM_COST_GROUP=SMC

SYNC_MASTER=AARON_MLB SYNC_DATE=05/11/2016

PAGE TITLE

SMC Support

Apple Inc.

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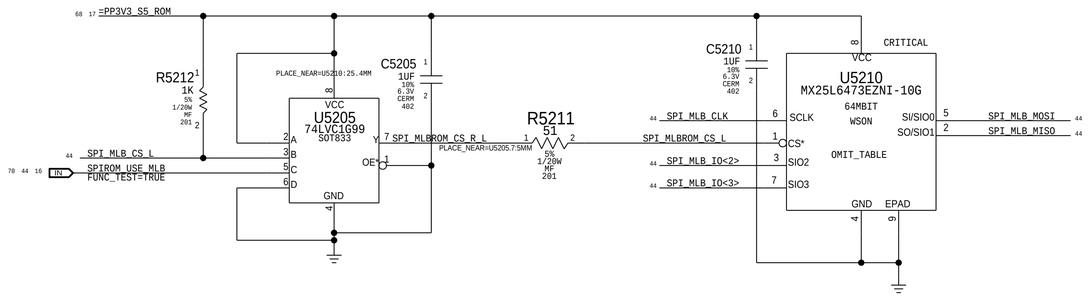
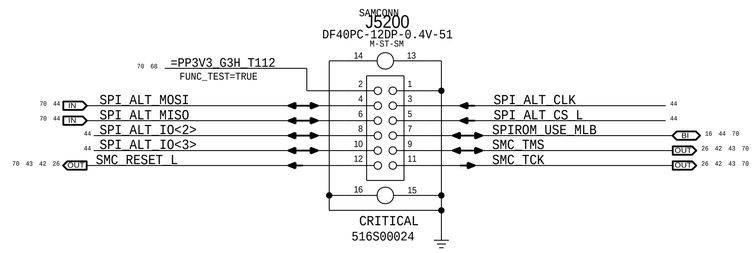
SPI BootROM

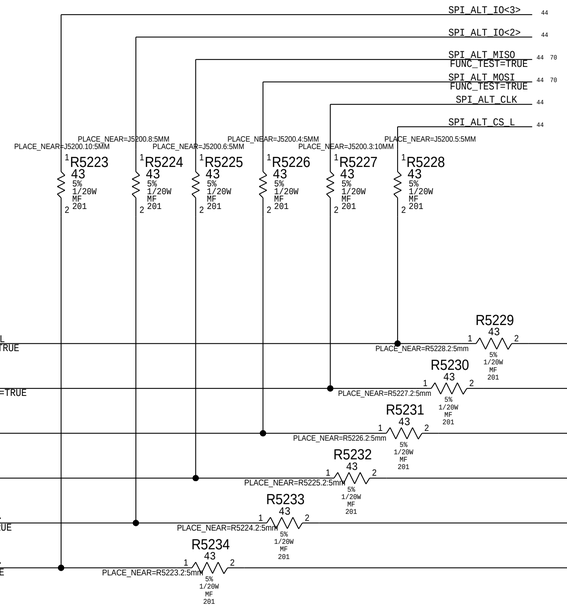
Quad_IO Mode (Mode 0 & 3) supported
SPI Freq: 50MHz for PCH, 20 MHz for SMC



SPI+SWD SAM Connector



SPI Series Termination



SAM Card ROM slave

BOOTROM SPI FLASH

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=06/14/2016

PAGE TITLE
SPI and Debug Connector

Apple Inc.

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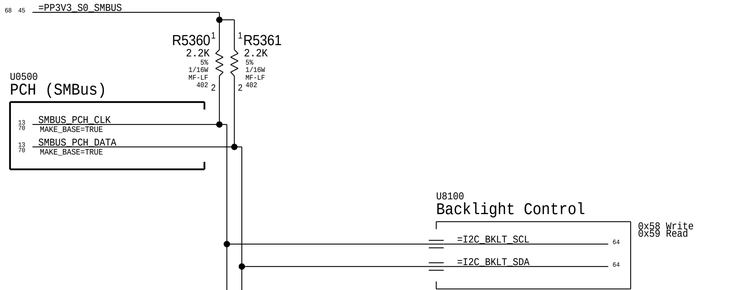
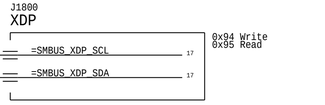
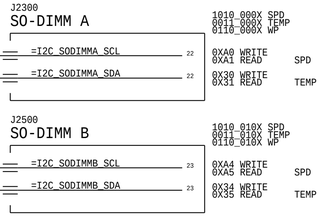
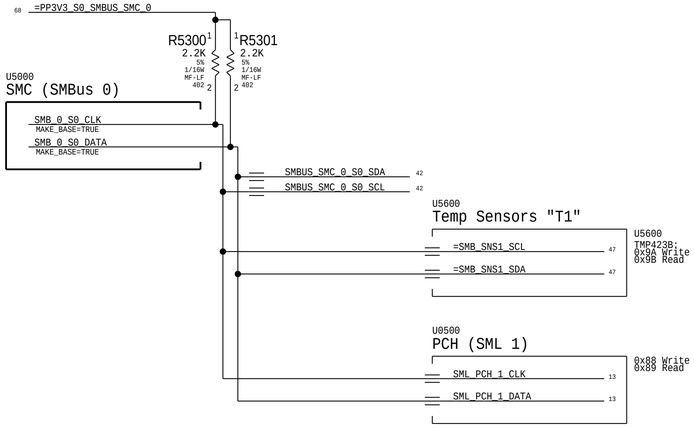
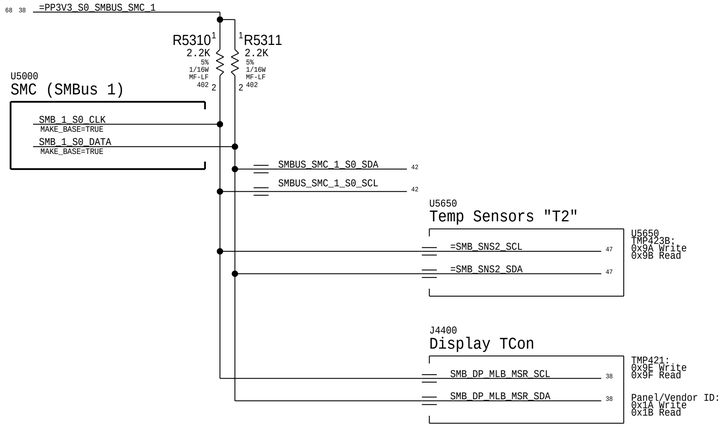
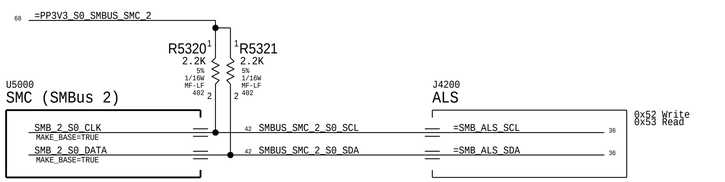


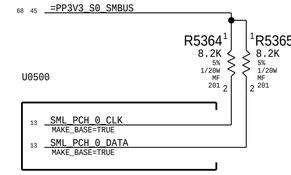




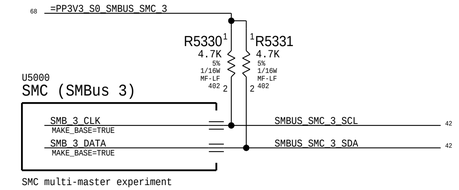




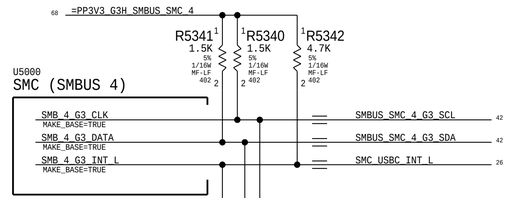


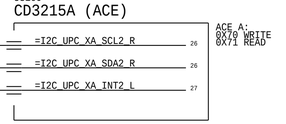


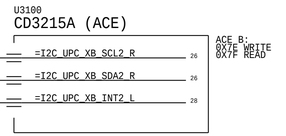
Unused PCH SM Link



SMC multi-master experiment







Line Legend
- Master
- Slave
- Mux

BOM_COST_GROUP=SMC

SYNC_MASTER=AARON_MLB SYNC_DATE=02/29/2016

PAGE TITLE
SMBus Connections

Apple Inc.

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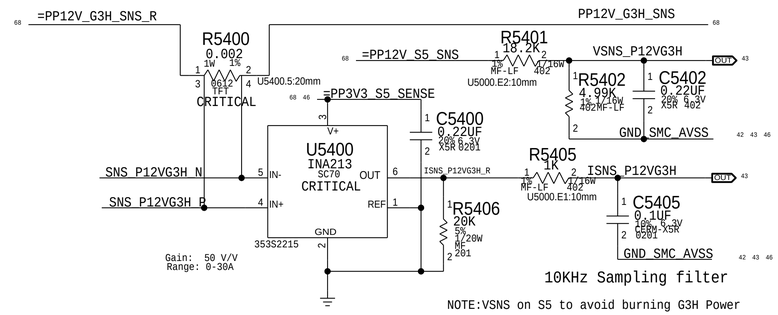
12V G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



10KHz Sampling filter

NOTE:VSNS on S5 to avoid burning G3H Power

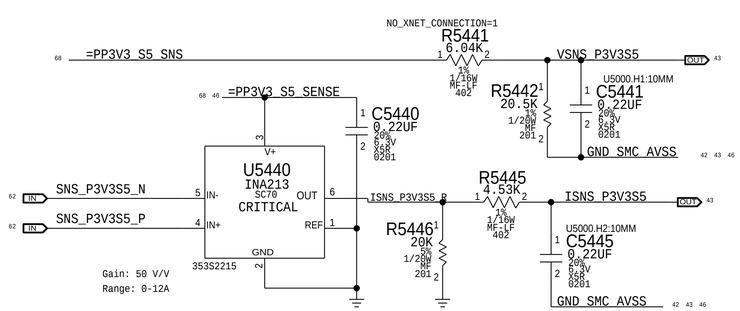
PP12V_S0_CPU (VD2R/IC20:ADC3)

CPU highside sense for CPU Core Regulator

10KHz Sampling filter

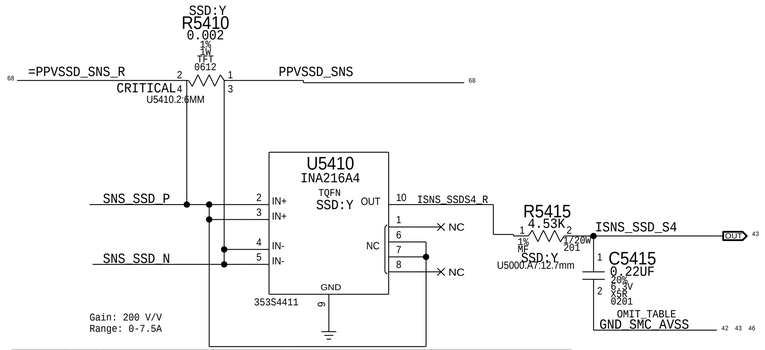
PP3V3_S5 (VR35:ADC18/IR35:ADC19)

PP3V3 S5 low side power distribution



SSD S4 (VR35/IH1R:ADC21)

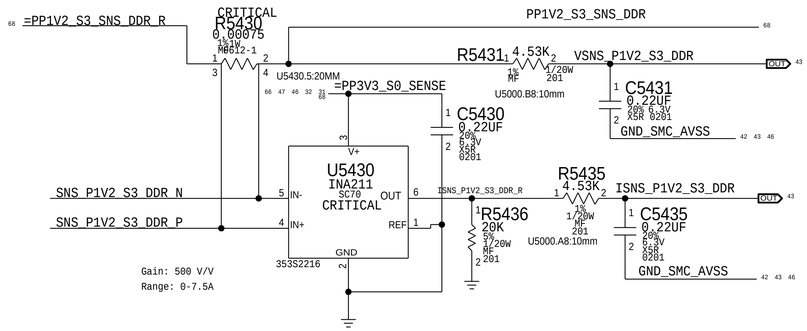
I-Sense for SSD / V-Sense for PPSSD)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5415	SSD:Y
117S0201	1	RES,0 OHM,201	C5415	SSD:N

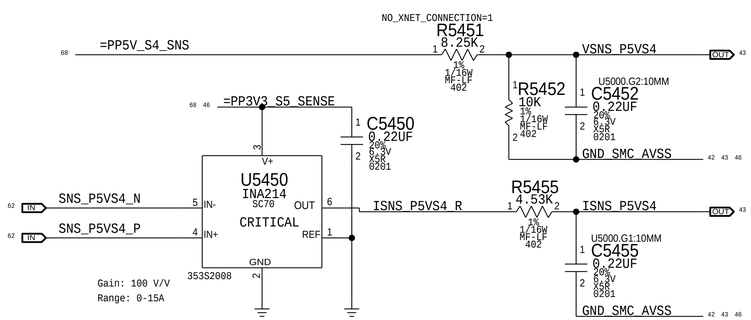
VDDQ S3 (VM0R:ADC22/IR13:ADC23)

VDDQ Lowside sense for CPU & SO-DIMM Modules

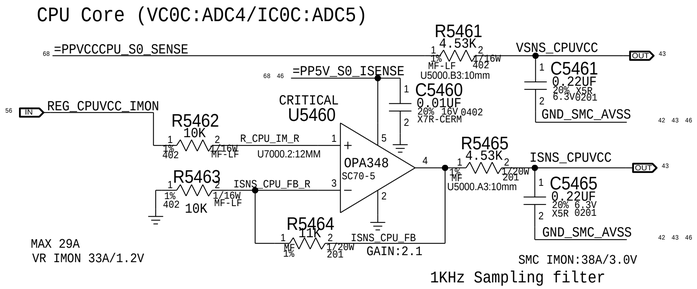


PP5V_S4 (VR54:ADC16/IR54:ADC17)

PP5V S4 low side power distribution

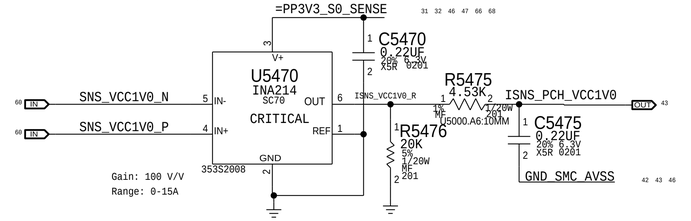


CPU Core (VC0C:ADC4/IC0C:ADC5)

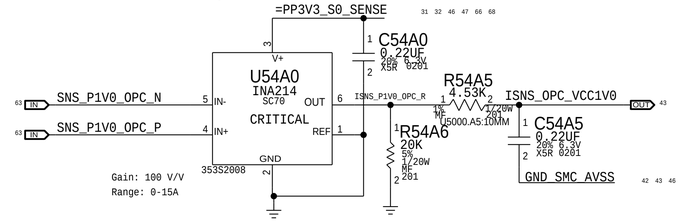


1KHz Sampling filter

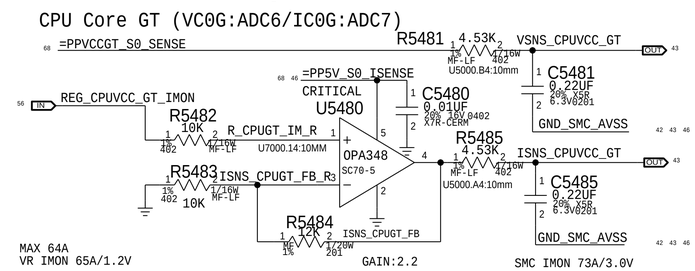
PCH VCC 1.0 (1.0V/IC0P:ADC11)



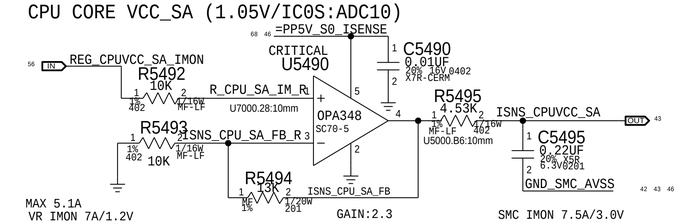
EDRAM VCC 1.0 (1.0V/IC0E:ADC9)



CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU CORE VCC_SA (1.05V/IC0S:ADC10)



BOM_COST_GROUP=SENSORS

SYNC_MASTER=AARON_HLB SYNC_DATE=04/08/2010

PAGE TITLE

Sensors: I and V Sense

Apple Inc.

DRAWING NUMBER 051-01543

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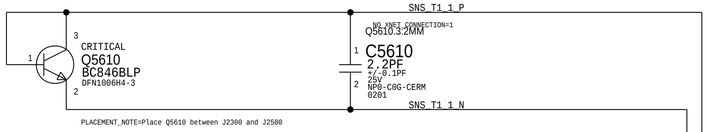
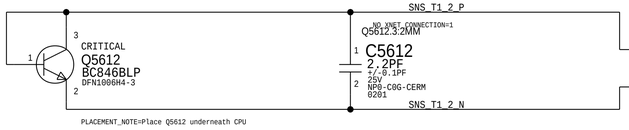
Temperature Sensor T1

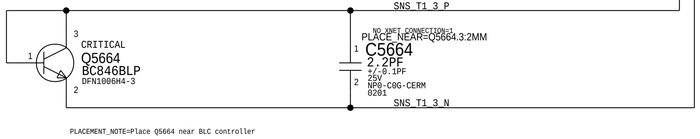
DDR4 SO-DIMM Proximity

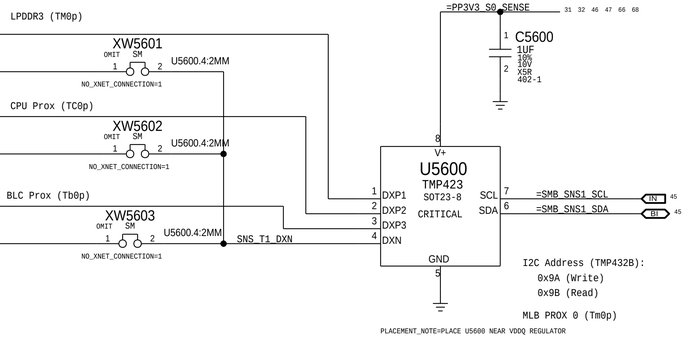


CPU Proximity



BLC Proximity

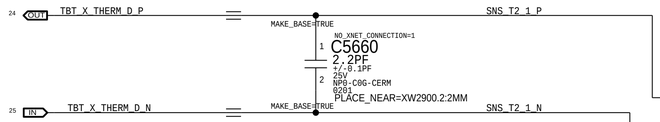




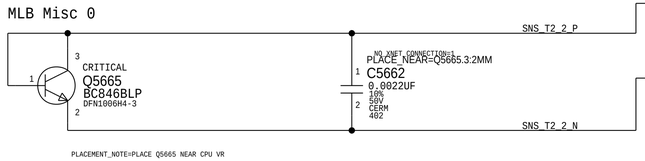
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

Temperature Sensor T2

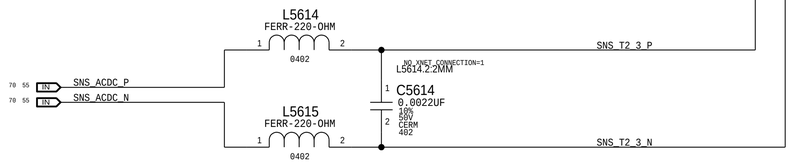
TBT On Die

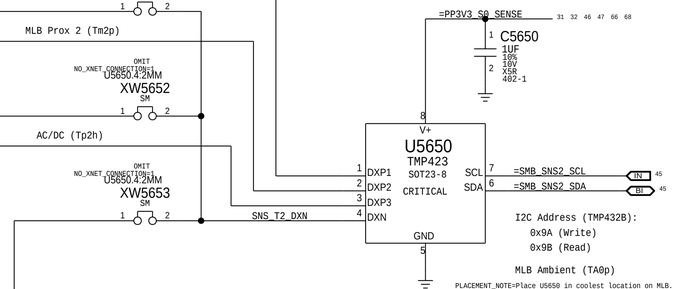


MLB Misc 0



AC/DC Diode on supply





Note:
Internal Sensor of the T2 Sensor will be used as the ambient sensor. Place U5600 at the coolest location on the MLB.

BOM_COST_GROUP=SENSORS

SYNC_MASTER=AARON_MLB SYNC_DATE=03/25/2016

PAGE TITLE: Temperature Sensors

Apple Inc.

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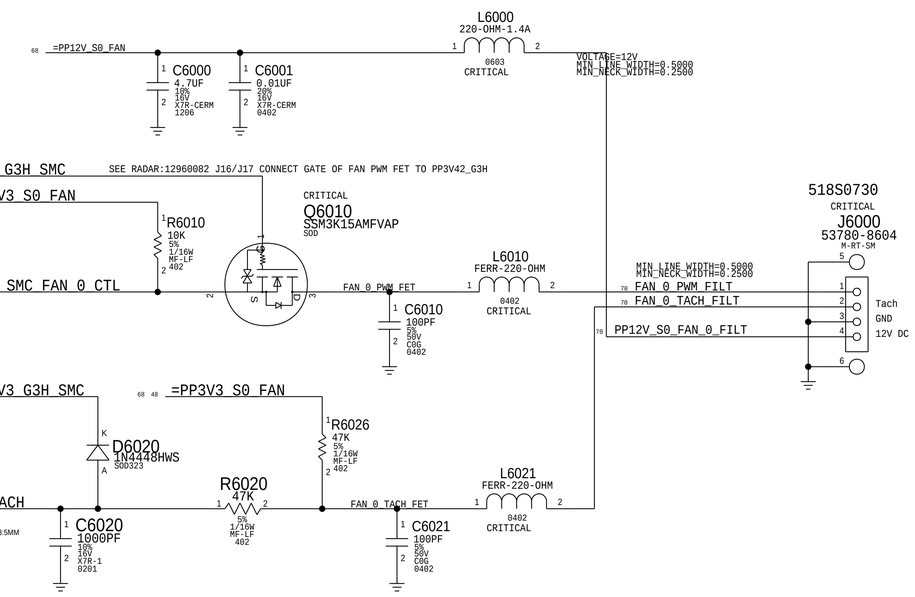
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

BOM_COST_GROUP=FAN

SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=04/08/2016

PAGE TITLE
System Fan

Apple Inc.

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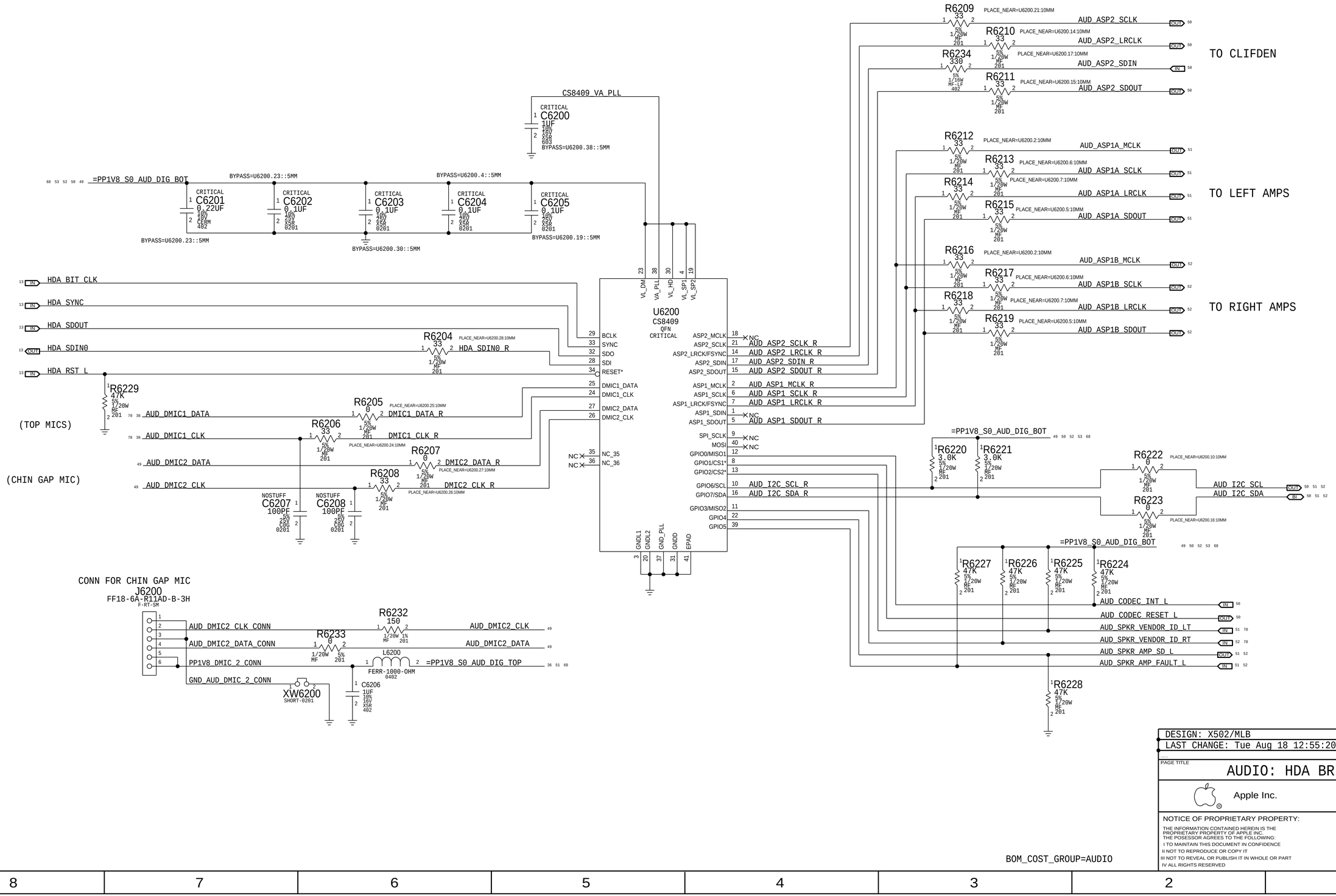

DESIGN: X502/MLB

LAST CHANGE: Tue Aug 18 12:55:20 2015

PAGE TITLE

AUDIO: HDA BRIDGE

Apple Inc.

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SIZE D

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AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B

L6304 FERR-22-OHM-1A-0.055OHM 0201
=PP3V3_S0_AUDIO → PP3V3_S0_AUDIO_BUFF
CRITICAL C6319 0.1UF 10% 25V X5R 0201

L6305 FERR-22-OHM-1A-0.055OHM 0201
=PP1V8_S0_AUD_DIG_BOT → PP1V8_S0_AUD_DIG_BUFF
CRITICAL C6318 0.1UF 10% 25V X5R 0201

PP1V8_S0_AUDIO
CRITICAL BYPASS=U6300.33::5MM C6300 2.2UF 10% 10V X5R-CERM 0402 → GND_AUDIO_CODEC

L6300 FERR-22-OHM-1A-0.055OHM 0201
PP1V8_S0_AUDIO → PP1V8_S0_AUDIO_L83_VCP

L6301 FERR-22-OHM-1A-0.055OHM 0201
PP1V8_S0_AUDIO → PP1V8_S0_AUDIO_L83_VL
CRITICAL BYPASS=U6300.39::5MM C6301 0.1UF 10% 16V X5R 0201

L6302 FERR-22-OHM-1A-0.055OHM 0201
=PP3V3_S0_AUDIO → PP3V3_S0_AUDIO_L83_VP
CRITICAL BYPASS=U6300.6::5MM C6302 10UF 20% 16V X5R-CERM 0402-7

U6301 74AUP1T34GF SOT891
AUD_SPDIF_OUT → A; A → Y → AUD_SPDIF_OUT_BUFF_R
NC → NC
GND
R6311 33 5% 1/10W MF-LF 201 → AUD_SPDIF_OUT_BUFF
NOSTUFF C6320 15PF 5% 50V CERM 402

U6300 CS42L83 QFN CRITICAL
APN:338SXXXXX

VP	6		
VL	39		
VD_FILT	47		NC
VA	33		
VCP	7		
+VCP_FILT	10		
-VCP_FILT	13		
GNDCP	12		
VL_SEL	48		
DIGLDO_PDN*	4		
INT*	2		
WAKE*	3		
RESET*	1		
SPDIF_TX	45		
SWIRE_SEL	40		
ASP_LRCK/FSYNC	43		
SWIRE_SD/ASP_SDIN	44		
ASP_SDOUT	41		
SWIRE_CLK/ASP_SCLK	42		
AD0	35		
AD1	34		
SDA	36		
SCL	37		
FLYP	8		
FLYC	9		
FLYN	11		
FILT_P	32		
GNDL	38		
GNDD	5		
GNDHS	46		
GNDA	25		
EPAD	31		
	49		
HPSENSA	14		
HPOUTA	15		
HPSENSB	17		
HPOUTB	16		
HS4	28		
HS_CLAMP2	27		
HSIN+	29		
HS3	24		
HS_CLAMP1	26		
HSIN-	30		
HS4_REF	20		
HS3_REF	19		
RING_SENSE	21		
TIP_SENSE	18		
HSBIAS_FILT	22		
HSBIAS_FILT_REF	23		

AUD_HP_PORT_LT → R6301 1K 1% 1/20W MF 201 → GND_AUDIO_CODEC
AUD_HP_PORT_RT → R6302 1K 1% 1/20W MF 201 → GND_AUDIO_CODEC
AUD_HP_SENSE_LT → HPSENSA
AUD_HP_SENSE_RT → HPSENSB
AUD_HP_PORT_CH_GND → HS4
AUD_HP_PORT_US_GND → HS_CLAMP2
HS_MICP → HSIN+
HS_MICN → HSIN-
AUD_HS_MICP → R6303 2.2K 1% 1/20W MF 201 → CRITICAL C6303 27PF 5% 25V C0G 0201 → GND_AUDIO_CODEC
CRITICAL C6304 3300PF 10% 10V X7R-CERM 0201 → R6305 100K 5% 1/20W MF 201 → GND_AUDIO_CODEC
AUD_HS_MICN → R6304 2.2K 1% 1/20W MF 201 → HS_MICN
R/C FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)
AUD_RING_SENSE → RING_SENSE
AUD_TIP_SENSE → TIP_SENSE
L83_HSBIAS_FILT → HSBIAS_FILT
CRITICAL C6305 4.7UF 20% 6.3V X5R 402 → L83_HSBIAS_FILT_REF
BYPASS=U6300.22::7MM

C6308 2.2UF 10% 10V X5R-CERM 0402 — BYPASS=U6300.7::5MM CRITICAL
C6309 4.7UF 20% 10V X5R-CERM 0402 — L83_VCP_FILTP → BYPASS=U6300.10::5MM CRITICAL
C6310 4.7UF 20% 10V X5R-CERM 0402 — L83_VCP_FILTN → BYPASS=U6300.13::5MM CRITICAL PLACE_NEAR=U6300.12:5MM
XW6301 SM — L83_GNDCP

=PP3V3_S0_AUDIO → R6307 47K 5% 1/20W MF 201
AUD_CODEC_INT_L → OUT
AUD_CODEC_RESET_L → IN → C6311 1000PF 10% 25V X5R 0201 / R6309 47K 5% 1/20W MF 201
AUD_CODEC_WAKE_L
R6308 33 5% 1/20W MF 201 → AUD_SPDIF_OUT
AUD_SPDIF_OUT_R — PLACE_NEAR=U6300.43:10MM
R6313 330 5% 1/10W MF-LF 402 → AUD_ASP2_LRCLK_RR → AUD_ASP2_LRCLK
R6314 330 5% 1/10W MF-LF 402 → AUD_ASP2_SDOUT_RR → AUD_ASP2_SDOUT
PLACE_NEAR=U6300.41:10MM
R6310 33 5% 1/20W MF 201 → L83_ASP_SDOUT_R → AUD_ASP2_SDIN
R6315 330 5% 1/10W MF-LF 402 → AUD_ASP2_SCLK_RR → AUD_ASP2_SCLK
PLACE_NEAR=U6300.42:10MM
AUD_I2C_SDA
AUD_I2C_SCL
L83_FLYP
L83_FLYC
L83_FLYN
L83_FILTP
C6312 2.2UF 10% 10V X5R-CERM 0402 — BYPASS=U6300.8::5MM CRITICAL
C6313 2.2UF 10% 10V X5R-CERM 0402 — BYPASS=U6300.11::5MM CRITICAL
CRITICAL C6314 10UF 20% 10V X5R 0603-1 — BYPASS=U6300.32::5MM
C6315 100PF 5% 25V C0G 0201
C6316 100PF 5% 25V C0G 0201
GND_AUDIO_CODEC — MIN_LINE_WIDTH=0.1000

PM_PGOOD_FET_P3V3_S0 → R6317 0 1/20W 5% MF 0201 → LDO0_ENA_R
L6303 FERR-22-OHM-1A-0.055OHM 0201
=PP3V3_S0_AUDIO → PP3V3_S0_AUDIO_LDO0
U6360 LP5907MFX-1.8V SOT23-5
VIN ← PP3V3_S0_AUDIO_LDO0; VOUT → PP1V8_S0_AUDIO
EN ← PP3V3_S0_AUDIO_LDO0; GND → GND_AUDIO_CODEC; NC1 → NC
R6316 0 1/20W 5% MF 0201 NOSTUFF
CRITICAL C6306 1.0UF 20% 10V X5R-CERM 0201-1
C6317 0.1UF 10% 16V X5R-CERM 0201 NOSTUFF
CRITICAL C6307 1.0UF 20% 10V X5R-CERM 0201-1
XW6300 SM — PLACE_NEAR=U6360.5MM

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB
LAST CHANGE: Tue Sep 22 14:30:15 2015
PAGE TITLE
AUDIO: AUDIO JACK CODEC
Apple Inc.
DRAWING NUMBER 051-01543
SIZE D
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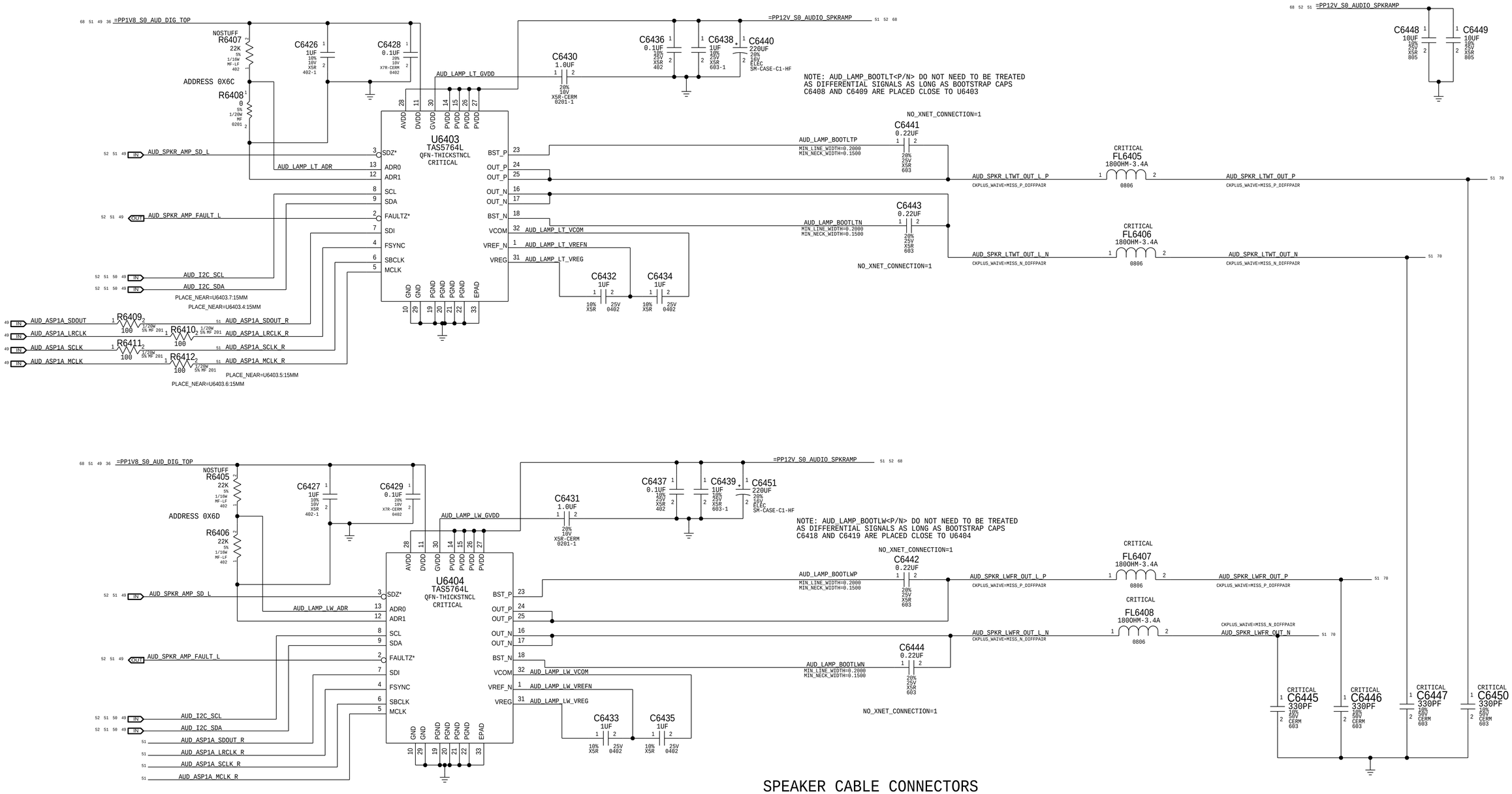
BRANCH
PAGE 63 OF 105
SHEET 50 OF 70

2X MONO SPEAKER AMPLIFIERS (TAS5764L)

APN:353S00875

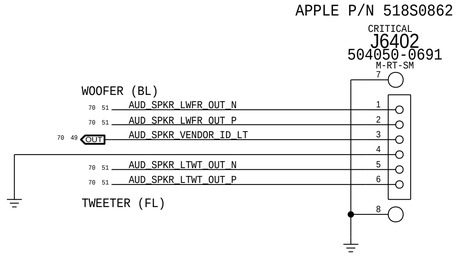
GAIN = TBD

SPEAKER AMPLIFIERS - LEFT CHANNEL



SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE

AUDIO: LEFT SPKR AMP

Apple Inc.

DRAWING NUMBER 051-01543

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REVISION 3.13.0

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2X MONO SPEAKER AMPLIFIERS (TAS5764L)

APN:353S00875

GAIN = TBD

SPEAKER AMPLIFIERS - RIGHT CHANNEL

=PP1V8_S0_AUD_DIG_BOT

R6501 22K 5% 1/16W MF-LF 402

ADDRESS 0X6E

NOSTUFF R6502 22K 5% 1/16W MF-LF 402

C6501 1UF 10% 10V X5R 402-1

C6503 0.1UF 20% 10V X7R-CERM 0402

AUD_RAMP_RT_GVDD

C6505 1.0UF 20% 10V X5R-CERM 0201-1

=PP12V_S0_AUDIO_SPKRAMP

C6511 0.1UF 10% 25V X5R 402

C6513 1UF 10% 25V X5R 603-1

C6515 220UF 20% 16V ELEC SM-CASE-C1-HF

C6523 10UF 10% 25V X5R 805

C6524 10UF 10% 25V X5R 805

NOTE: AUD_LAMP_BOOTRT<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6408 AND C6409 ARE PLACED CLOSE TO U6501

U6501 TAS5764L QFN-THICKSTNCL CRITICAL

AVDD	28		
DVDD	11		
GVDD	30		
PVDD	14		
PVDD	15		
PVDD	26		
PVDD	27		
SDZ*	3	IN	AUD_SPKR_AMP_SD_L
ADR0	13		AUD_RAMP_RT_ADR
ADR1	12		
SCL	8		AUD_I2C_SCL
SDA	9		AUD_I2C_SDA
FAULTZ*	2	OUT	AUD_SPKR_AMP_FAULT_L
SDI	7		
FSYNC	4		AUD_ASP1B_LRCLK_R
SBCLK	6		AUD_ASP1B_SCLK_R
MCLK	5		AUD_ASP1B_MCLK_R
BST_P	23		
OUT_P	24		AUD_SPKR_RTWT_OUT_L_P
OUT_P	25		
OUT_N	16		AUD_SPKR_RTWT_OUT_L_N
OUT_N	17		
BST_N	18		
VCOM	32		AUD_RAMP_RT_VCOM
VREF_N	1		AUD_RAMP_RT_VREFN
VREG	31		AUD_RAMP_RT_VREG
GND	10		
GND	29		
PGND	19		
PGND	20		
PGND	21		
PGND	22		
PGND	33		
EPAD			

PLACE_NEAR=U6501.7:15MM

PLACE_NEAR=U6501.4:15MM

PLACE_NEAR=U6501.5:15MM

PLACE_NEAR=U6501.6:15MM

R6509 100 1/20W 5% MF 201 — AUD_ASP1B_SDOUT → AUD_ASP1B_SDOUT_R

R6510 100 1/20W 5% MF 201 — AUD_ASP1B_LRCLK → AUD_ASP1B_LRCLK_R

R6511 100 1/20W 5% MF 201 — AUD_ASP1B_SCLK → AUD_ASP1B_SCLK_R

R6512 100 1/20W 5% MF 201 — AUD_ASP1B_MCLK → AUD_ASP1B_MCLK_R

C6507 1UF 10% 25V X5R 0402

C6509 1UF 10% 25V X5R 0402

AUD_RAMP_BOOTRTP — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500

C6516 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_RAMP_BOOTRTN — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500

C6518 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

CRITICAL FL6501 180OHM-3.4A 0806

CRITICAL FL6502 180OHM-3.4A 0806

AUD_SPKR_RTWT_OUT_L_P — CKPLUS_WAIVE=MISS_P_DIFFPAIR — AUD_SPKR_RTWT_OUT_P — CKPLUS_WAIVE=MISS_P_DIFFPAIR

AUD_SPKR_RTWT_OUT_L_N — CKPLUS_WAIVE=MISS_N_DIFFPAIR — AUD_SPKR_RTWT_OUT_N — CKPLUS_WAIVE=MISS_N_DIFFPAIR

=PP1V8_S0_AUD_DIG_BOT

R6503 0 5% 1/20W MF 0201

ADDRESS 0X6F

NOSTUFF R6504 22K 5% 1/16W MF-LF 402

C6502 1UF 10% 10V X5R 402-1

C6504 0.1UF 20% 10V X7R-CERM 0402

AUD_RAMP_RW_GVDD

C6506 1.0UF 20% 10V X5R-CERM 0201-1

=PP12V_S0_AUDIO_SPKRAMP

C6512 0.1UF 10% 25V X5R 402

C6514 1UF 10% 25V X5R 603-1

C6526 220UF 20% 16V ELEC SM-CASE-C1-HF

NOTE: AUD_LAMP_BOOTRW<P/N> DO NOT NEED TO BE TREATED AS DIFFERENTIAL SIGNALS AS LONG AS BOOTSTRAP CAPS C6418 AND C6419 ARE PLACED CLOSE TO U6502

U6502 TAS5764L QFN-THICKSTNCL CRITICAL

AVDD	28		
DVDD	11		
GVDD	30		
PVDD	14		
PVDD	15		
PVDD	26		
PVDD	27		
SDZ*	3	IN	AUD_SPKR_AMP_SD_L
ADR0	13		AUD_RAMP_RW_ADR
ADR1	12		
SCL	8		AUD_I2C_SCL
SDA	9		AUD_I2C_SDA
FAULTZ*	2	OUT	AUD_SPKR_AMP_FAULT_L
SDI	7		AUD_ASP1B_SDOUT_R
FSYNC	4		AUD_ASP1B_LRCLK_R
SBCLK	6		AUD_ASP1B_SCLK_R
MCLK	5		AUD_ASP1B_MCLK_R
BST_P	23		
OUT_P	24		AUD_SPKR_RWFR_OUT_L_P
OUT_P	25		
OUT_N	16		AUD_SPKR_RWFR_OUT_L_N
OUT_N	17		
BST_N	18		
VCOM	32		AUD_RAMP_RW_VCOM
VREF_N	1		AUD_RAMP_RW_VREFN
VREG	31		AUD_RAMP_RW_VREG
GND	10		
GND	29		
PGND	19		
PGND	20		
PGND	21		
PGND	22		
PGND	33		
EPAD			

C6508 1UF 10% 25V X5R 0402

C6510 1UF 10% 25V X5R 0402

AUD_RAMP_BOOTRWP — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500

C6517 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

AUD_RAMP_BOOTRWN — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1500

C6519 0.22UF 20% 25V X5R 603

NO_XNET_CONNECTION=1

CRITICAL FL6503 180OHM-3.4A 0806

CRITICAL FL6504 180OHM-3.4A 0806

AUD_SPKR_RWFR_OUT_L_P — CKPLUS_WAIVE=MISS_P_DIFFPAIR — AUD_SPKR_RWFR_OUT_P — CKPLUS_WAIVE=MISS_P_DIFFPAIR

AUD_SPKR_RWFR_OUT_L_N — CKPLUS_WAIVE=MISS_N_DIFFPAIR — AUD_SPKR_RWFR_OUT_N — CKPLUS_WAIVE=MISS_N_DIFFPAIR

C6520 330PF 10% 50V CERM 603

C6521 330PF 10% 50V CERM 603

C6522 330PF 10% 50V CERM 603

C6525 330PF 10% 50V CERM 603

SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862

CRITICAL J6502 504050-0691 M-RT-SM

WOOFER (BR)		
AUD_SPKR_RWFR_OUT_N	1	
AUD_SPKR_RWFR_OUT_P	2	
AUD_SPKR_VENDOR_ID_RT	3	OUT
	4	
AUD_SPKR_RTWT_OUT_N	5	
AUD_SPKR_RTWT_OUT_P	6	
TWEETER (FR)		
	7	
	8	

BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE: AUDIO: RIGHT SPKR AMP

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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BRANCH

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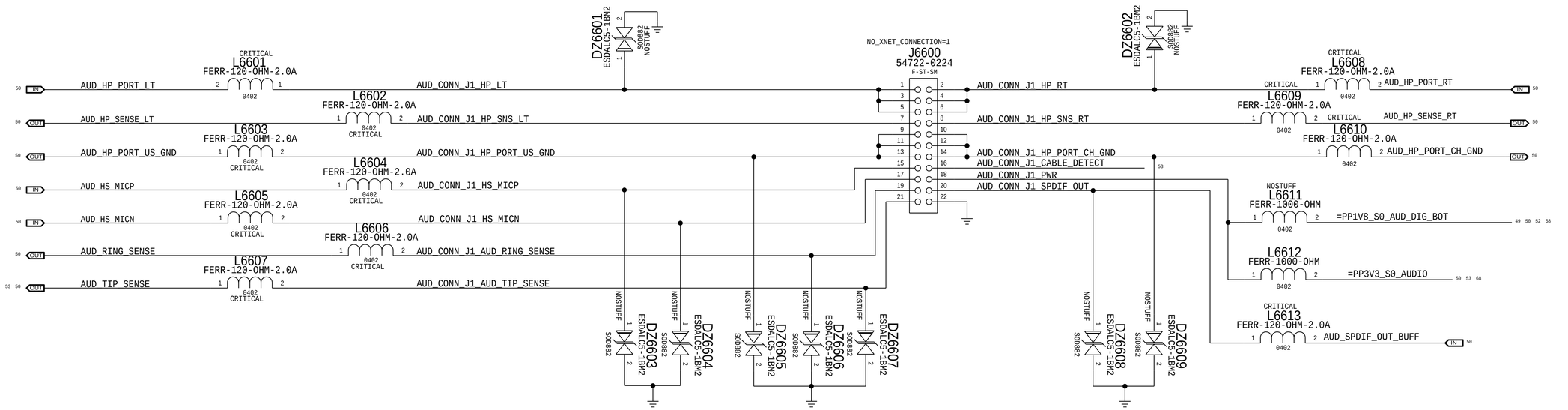
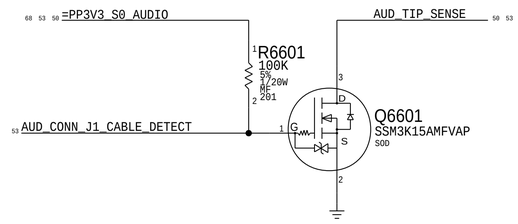


AUDIO JACK FLEX CABLE DETECT



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO: AUDIO JACK CONN

Apple Inc.

DRAWING NUMBER 051-01543

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

SYNC_MASTER=J135_MLB SYNC_DATE=12/03/2015

PAGE TITLE

AUDIO: EMPTY

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

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3.3V "G3HOT" REGULATOR

1.25MHZ SWITCHING FREQ

C6936/C6937 ARE MIRRORED AS A provision for acoustic noise

C6908/C6909 ARE MIRRORED AS A provision for acoustic noise

C6932/C6933 AND C6934/C6935 ARE MIRRORED AS A PROVISION FOR ACOUSTIC NOISE

353S4322 TPS3847085

8.5V VCC FALLING RESET THRESHOLD

+/- 0.2125V

VOL-MAX = 0.4V

VOH-MAX = 4V

SMC VIL-MAX = 1V
(FOR 3V3-SUPERVISOR MIN)

VOUT = 0.8V * (1 + RA / RB)

MLB to AC-DC Supplemental Signal Connector

MLB to AC-DC Connector

C6917/C6918 are mirrored as a provision for acoustic noise to replace C6911 if needed

12V S5 FET

SMC_PM_G2_EN IS PULLED DOWN ON SMC PAGE

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	Power Connectors / VReg G3Hot
	Apple Inc.
DRAWING NUMBER	051-01543
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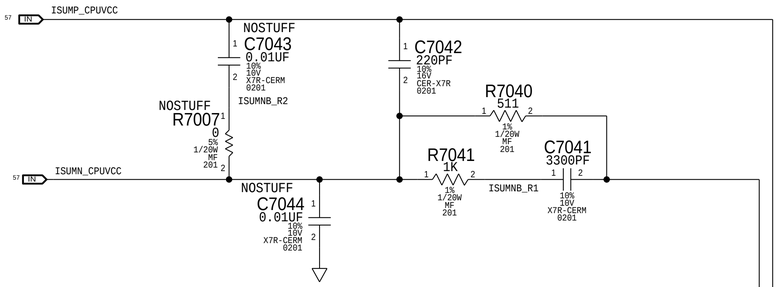
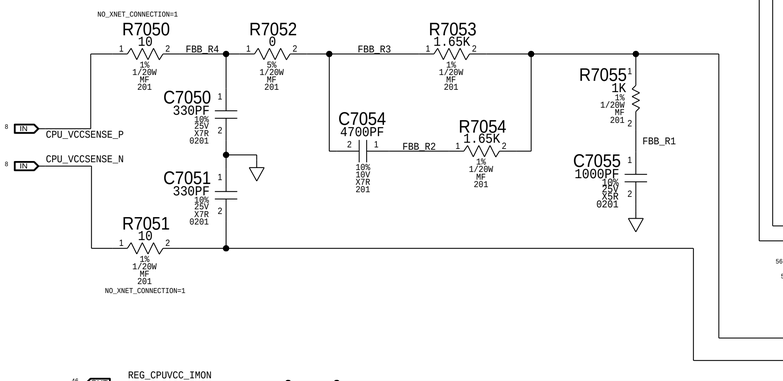
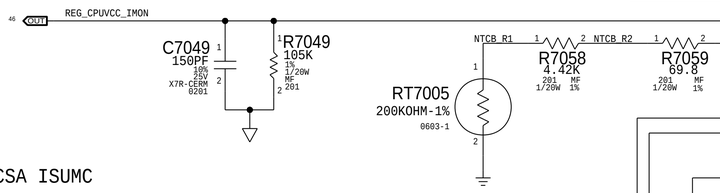
CPUVCC ISUMB

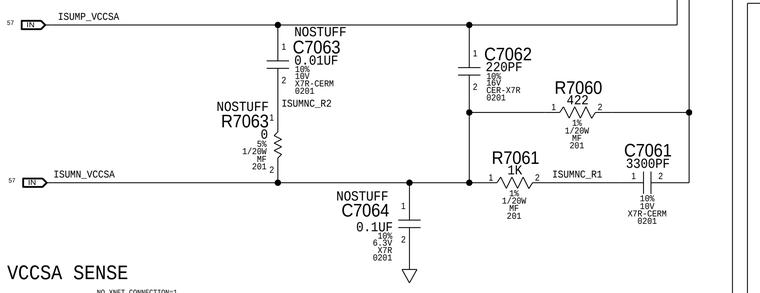


CPUVCC SENSE

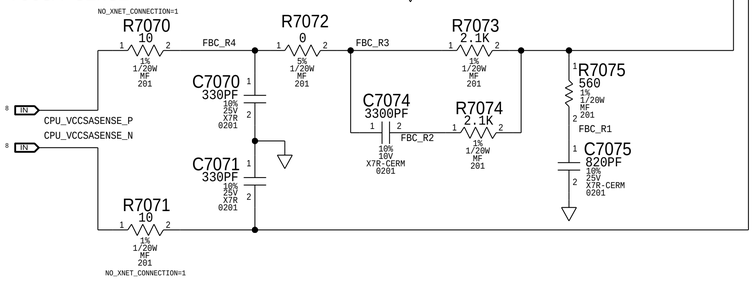


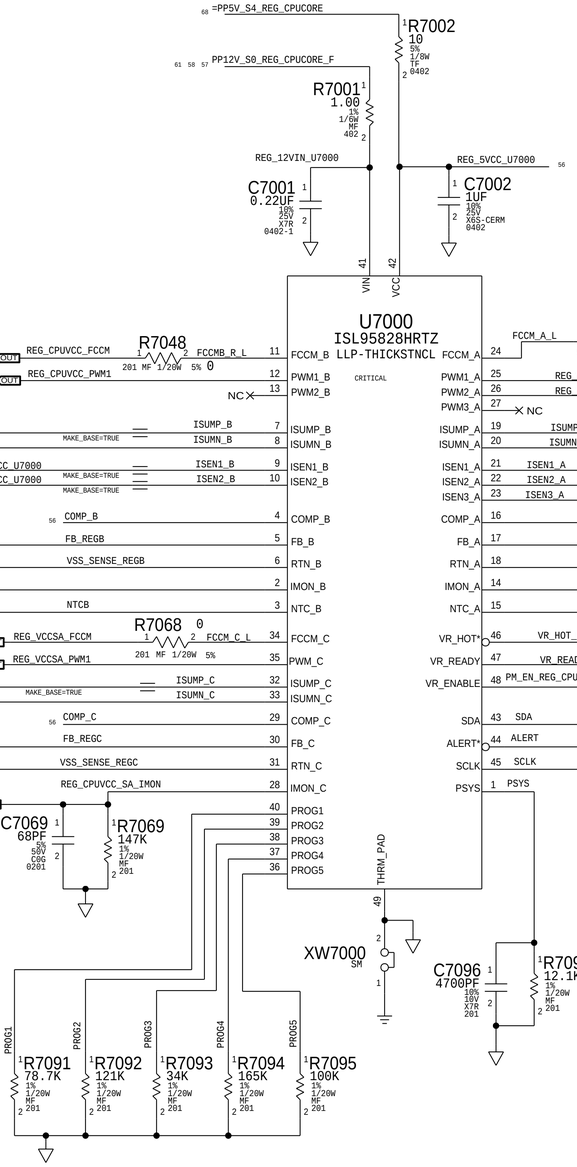


VCCSA ISUMC



VCCSA SENSE

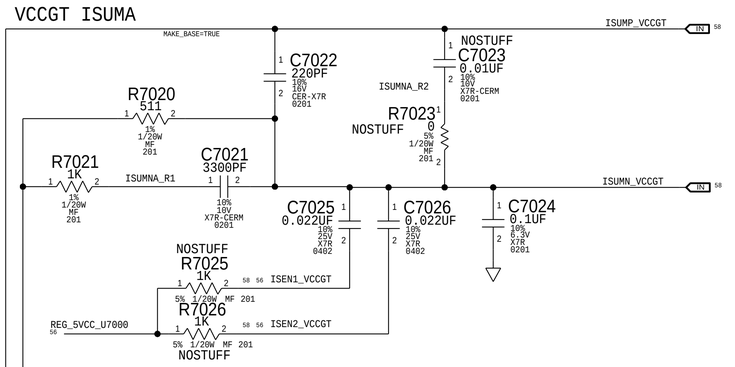




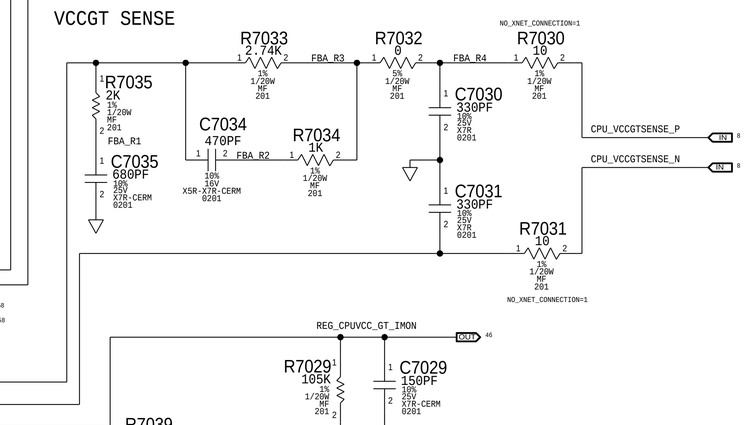
PR0G1 (78.7K) : 0V BOOT & 0.03V/US SLEW RATE
REGA=GT, REGB=IA, REGC=SA

PROG2 (121K) : 65A ICCMAX REGA & 1PH PS1
PROG3 (34K) : 33A ICCMAX REGB
PROG4 (165K) : 583KHZ REGA & REGB
PROG5 (100K) : 7A ICCMAX REGC & 750KHZ REGC

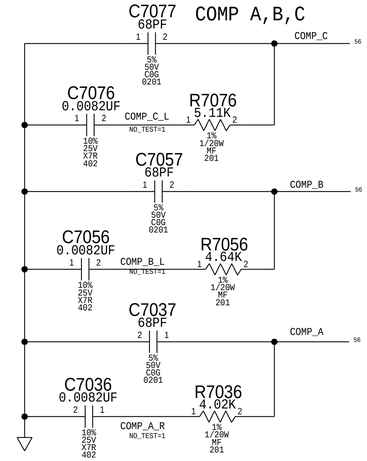
VCCGT ISUMA



VCCGT SENSE



COMP A,B,C



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU IMVP8 SKL Regulator

Apple Inc.

DRAWING NUMBER	051-01543
SIZE	D
REVISION	3.13.0
BRANCH	
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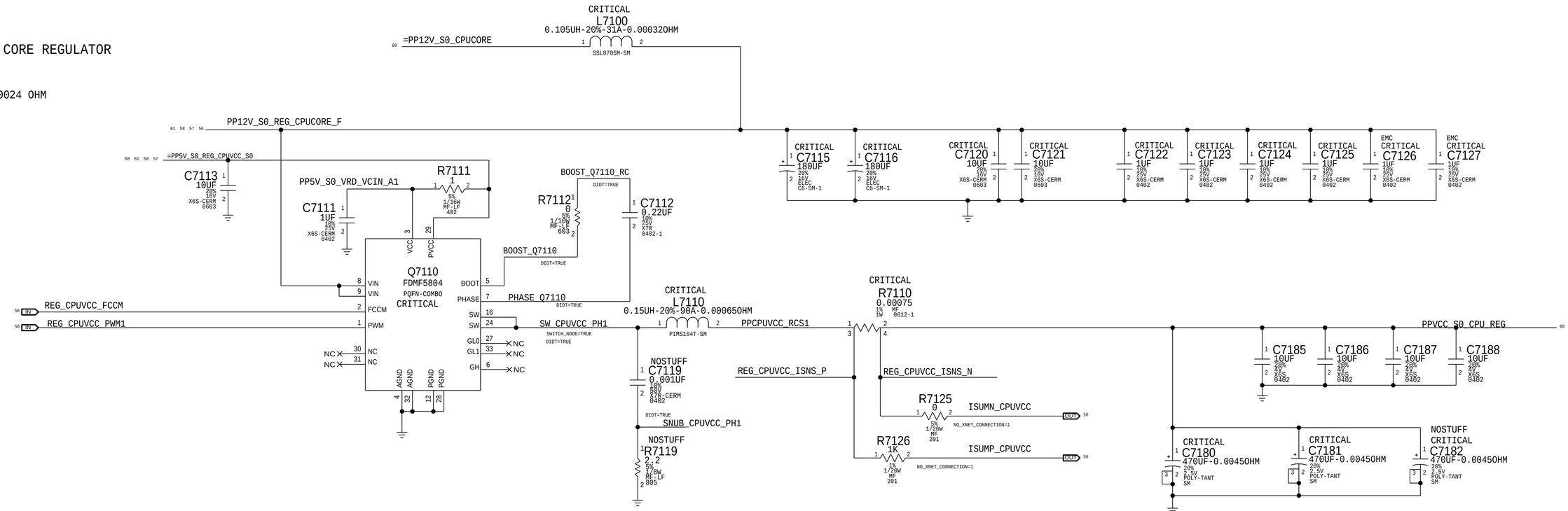
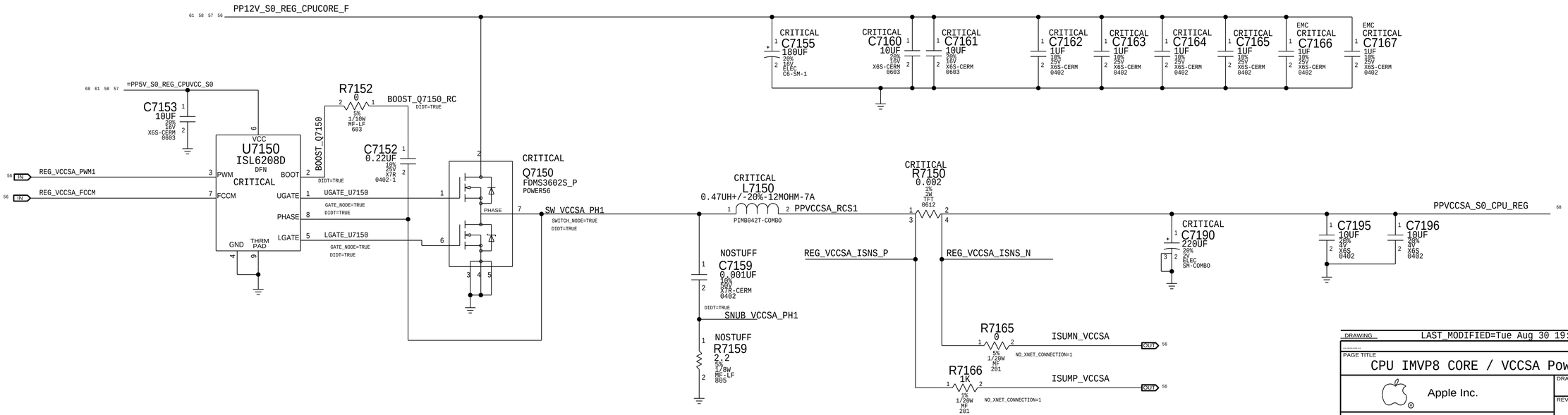
CPU VCC CORE REGULATOR

EDC = 32A
TDC = 23A
DCLL = 0.0024 OHM



CPU VCCSA REGULATOR

EDC = 5.5A
TDC = 5.0A
DCLL = 0.0103 OHM



BOM_COST_GROUP=CPU & CHIPSET

DRAWING: LAST_MODIFIED=Tue Aug 30 19:52:22 2016

PAGE TITLE: CPU IMVP8 CORE / VCCSA Power Stage

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D
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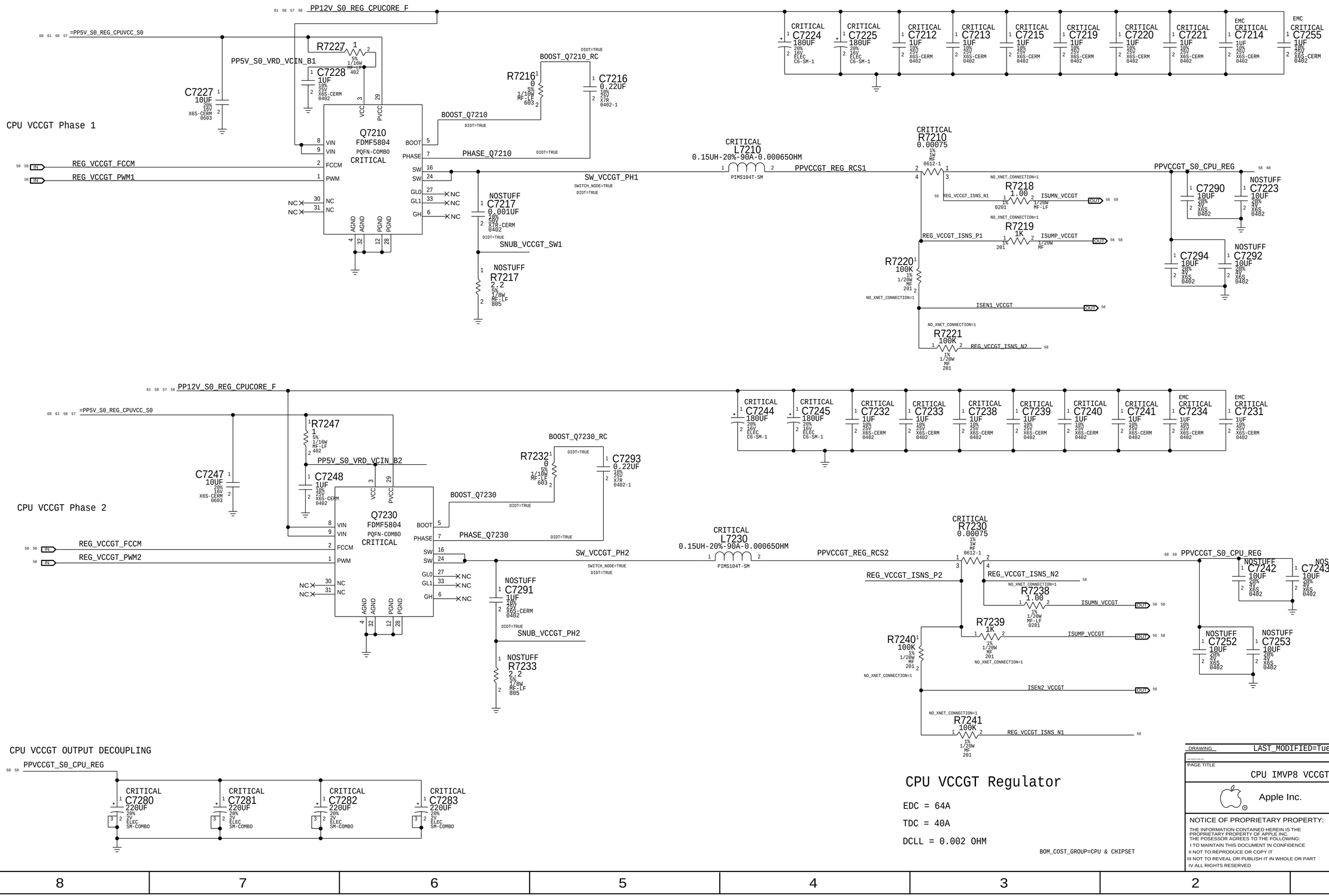

DRAWING LAST_MODIFIED=Tue Aug 30 19:52:28 2016

PAGE TITLE: CPU IMVP8 VCCGT Power Stage

Apple Inc.

DRAWING NUMBER 051-01543 | SIZE D

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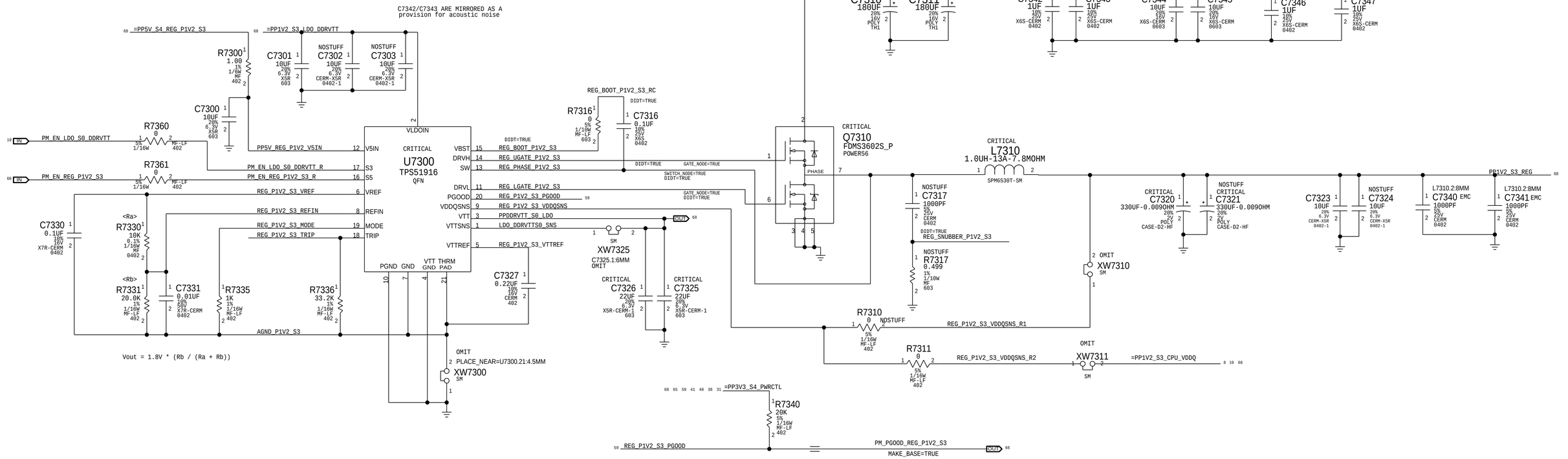
VDDQ 1.2V S3 Regulator

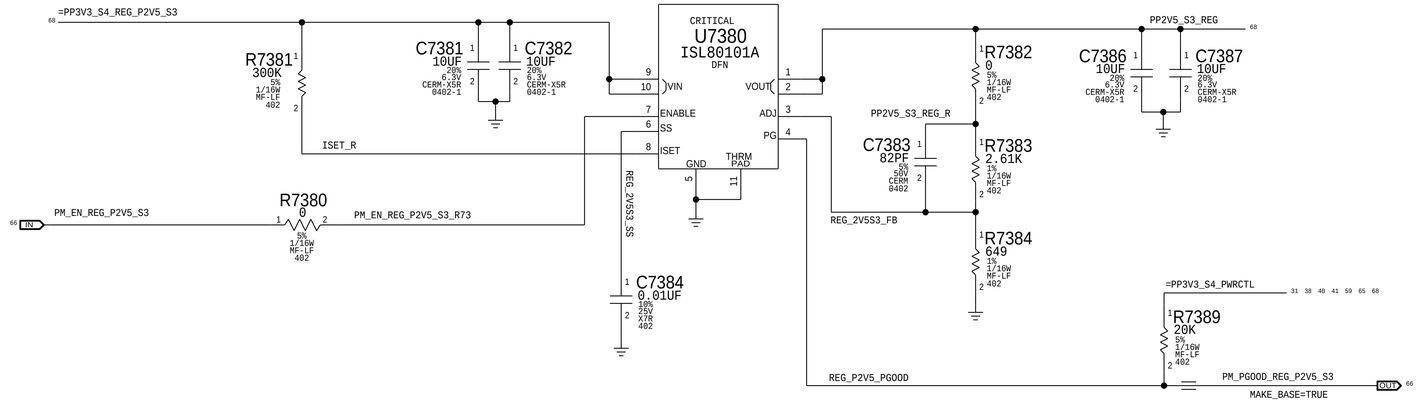
OC trip point: TBD A VDDQ = $\frac{\text{R7306}}{\text{8 E5 * Rds(Q7310)}} + \frac{\text{0.65625}}{\text{L7310 * f(switch)}}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



DDR4 VPP 2.5V REGULATOR



BOM_COST_GROUP=DRAM

SYNC_MASTER=VINCE_MLB SYNC_DATE=04/05/2010

PAGE TITLE: DDR Regulators VDDQ / VTT / VPP

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D
REVISION: 3.13.0
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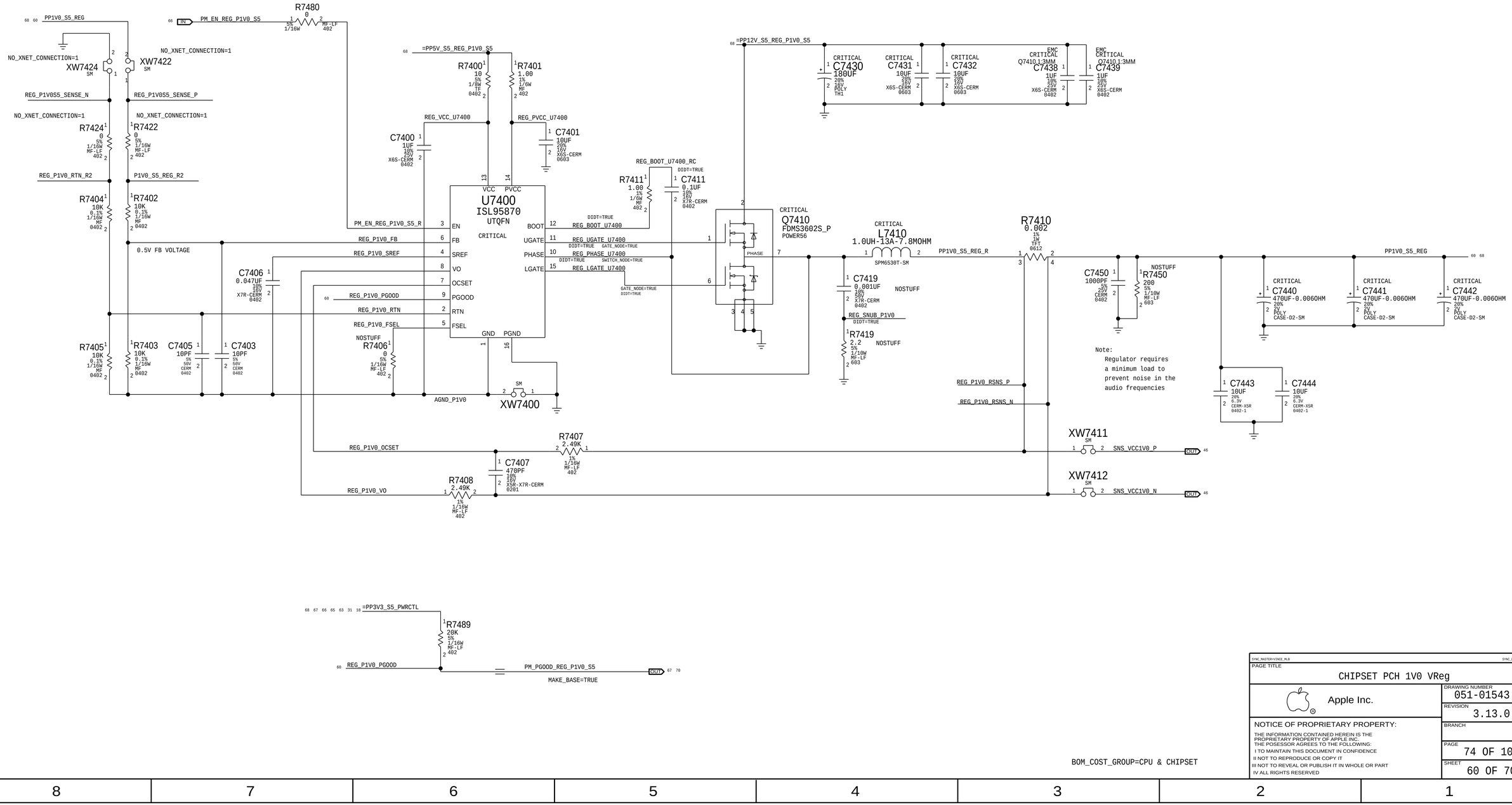
1.0V S5 REGULATOR

FSEL STRAP	SW FREQ
GND	300 kHz
FLOAT	500 kHz
100k to GND	600 kHz

OCP CURRENT LIMIT (TYP): 10.6 A = $\frac{\text{R7407} * 8.5\text{ E-6}}{\text{R7410}}$

SOFT START TIME: 0.00138 SEC = $\frac{\text{C7406} * 0.5\text{V}}{17\text{UA}}$



SYNC_MASTER=J7NGE_MLB SYNC_DATE=05/31/2013

PAGE TITLE

CHIPSET PCH 1V0 VReg

Apple Inc.

DRAWING NUMBER 051-01543

SIZE D

REVISION 3.13.0

BRANCH

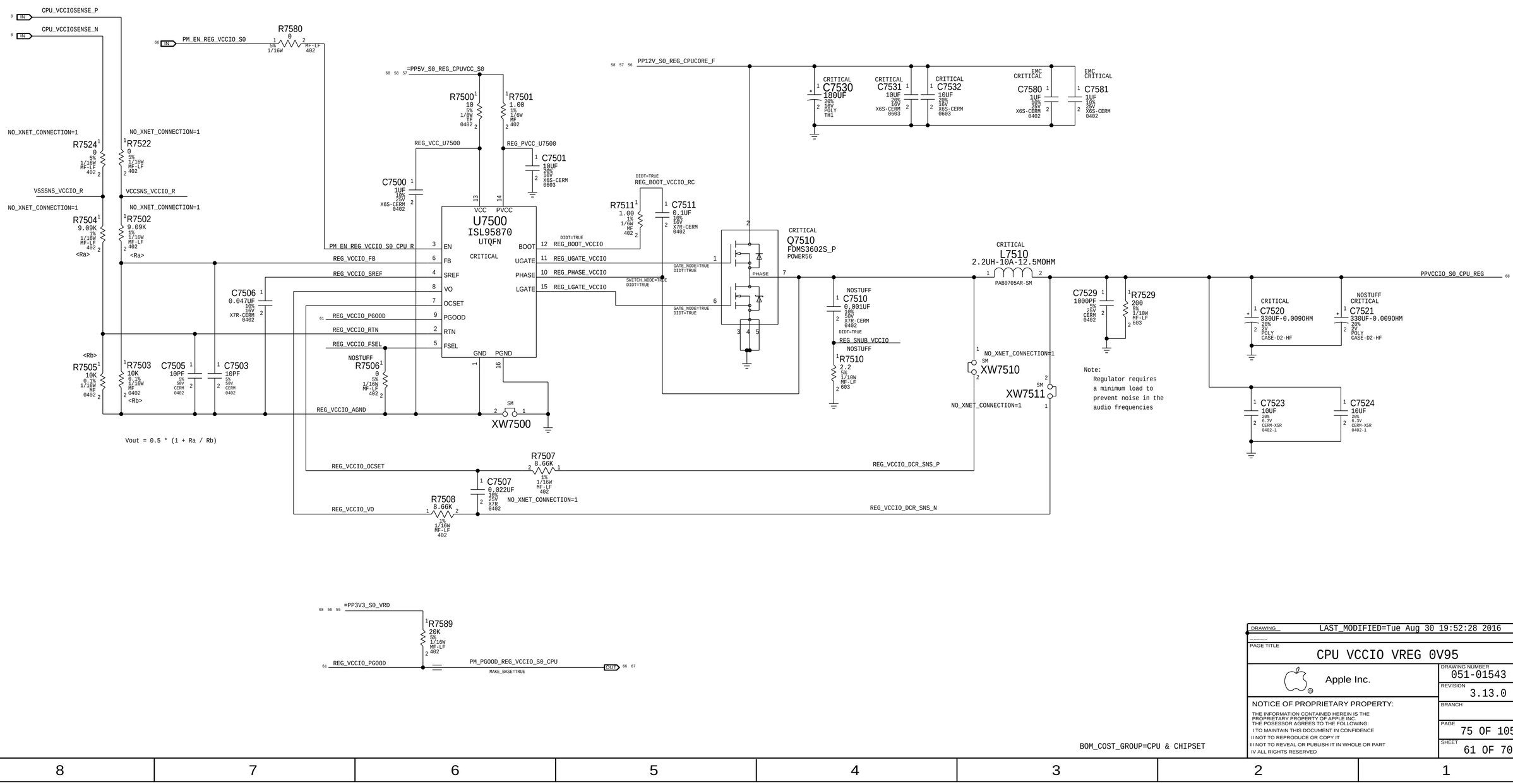
PAGE 74 OF 105

SHEET 60 OF 70

VCCIO 0V95 S0 REGULATOR

FSEL STRAP	SW FREQ
GND	300 kHz
FLOAT	500 kHz
100k to GND	600 kHz

OCP CURRENT LIMIT: 5.9 A = R7407 * 8.5 E-6 / DCR(L7510)



BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Tue Aug 30 19:52:28 2016

PAGE TITLE: CPU VCCIO VREG 0V95

Apple Inc.

DRAWING NUMBER 051-01543 | SIZE D

REVISION 3.13.0

BRANCH

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SHEET 61 OF 70

3.3V S5 Regulator

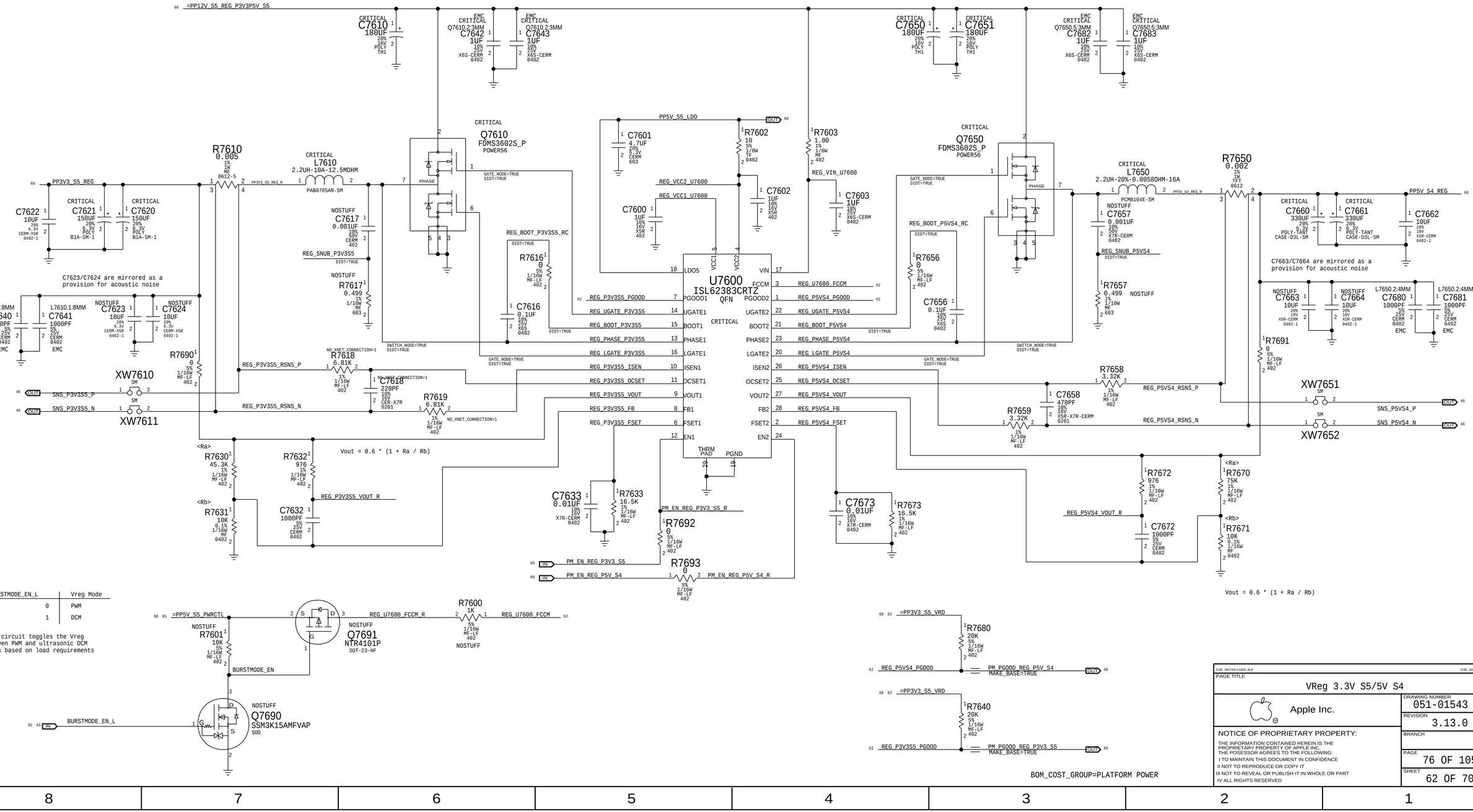
OC TRIP POINT (TYP): 13.6 A = $\frac{\text{R7618} * 10\text{ E-6}}{\text{R7610}}$

Switching freq: 356 kHz = $\frac{1}{170\text{ E-12} * \text{R7633}}$

5V S4 Regulator

OC trip point: 16.6 A = $\frac{\text{R7658} * 10\text{ E-6}}{\text{R7650}}$

Switching freq: 356 kHz = $\frac{1}{170\text{ E-12} * \text{R7673}}$



SYNC_MASTER=SYNCE_MLB SYNC_DATE=05/31/2010

PAGE TITLE

VReg 3.3V S5/5V S4

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D

REVISION 3.13.0

BRANCH

PAGE 76 OF 105

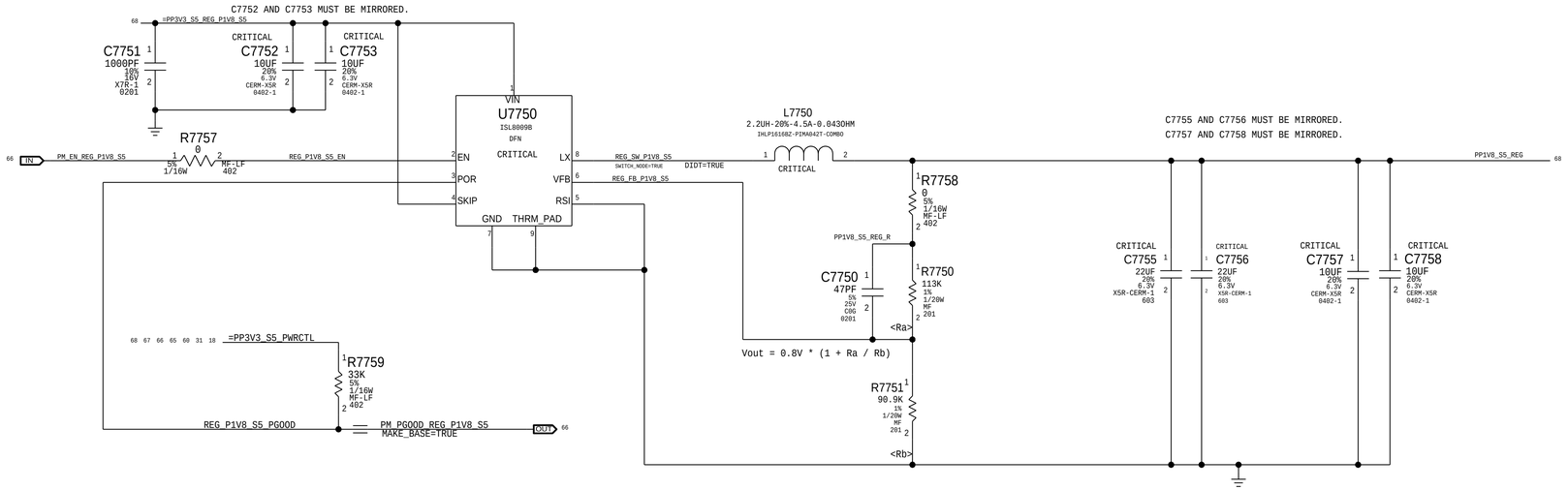
SHEET 62 OF 70

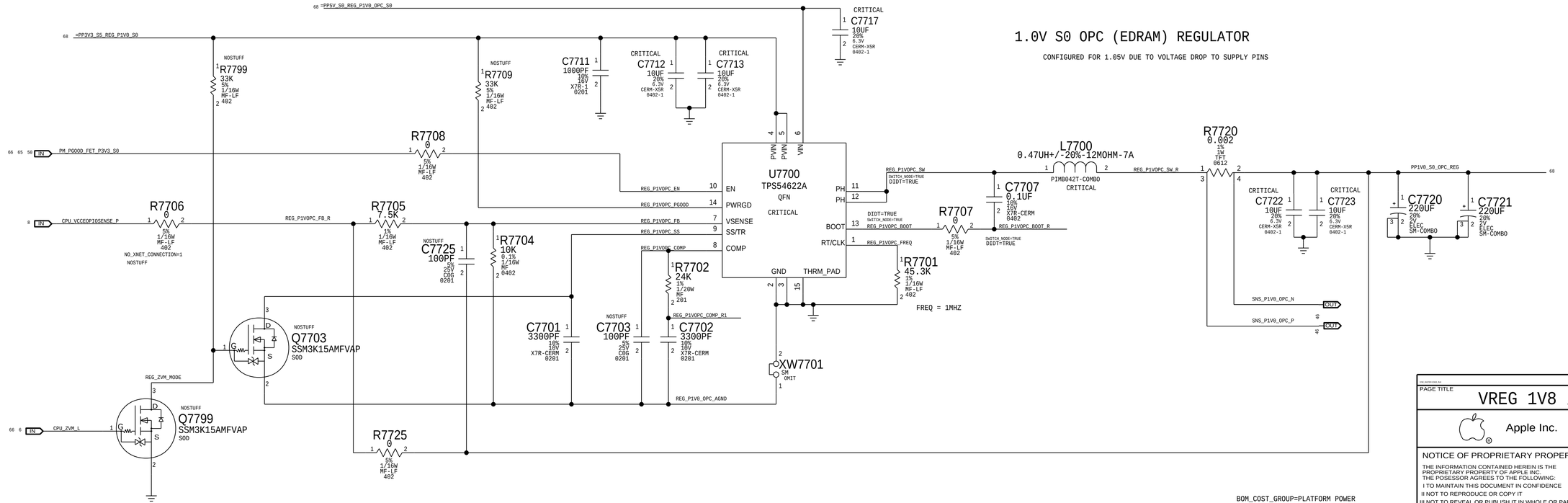
1.8V S5 REGULATOR

Vout = 1.794V

Max Current = 1.8A

Freq = 1 MHz





PAGE TITLE

VREG 1V8 / MISC POWER

Apple Inc.

DRAWING NUMBER 051-01543

SIZE D

REVISION 3.13.0

BRANCH

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SHEET 63 OF 70

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0648	371S0694		D8100	BLC Switch Diode

ACOUSTICS E-NOISE COMPONENTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0748	371S0731		D8101	INPUT DIODE
138S1078	138S0810		2.2UF_CAP	BLC 2.2uF OUTPUT CAPS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=J117_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LCD Backlight Driver (LP8561)

Apple Inc.

DRAWING NUMBER: 051-01543 SIZE: D

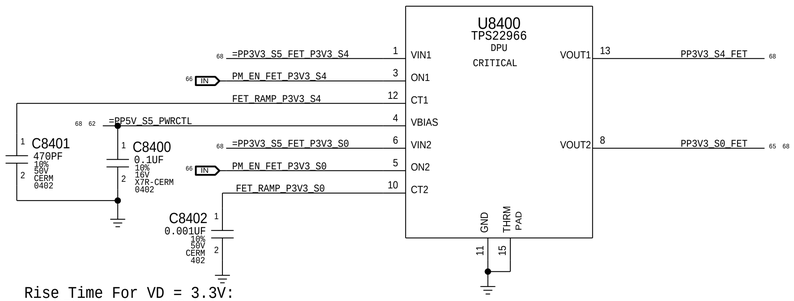
REVISION: 3.13.0

BRANCH:

PAGE: 81 OF 105

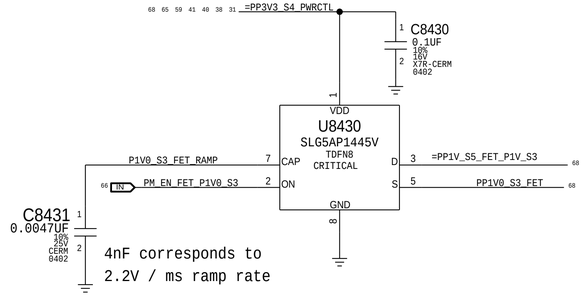
SHEET: 64 OF 70

3.3V S4/S0 FET



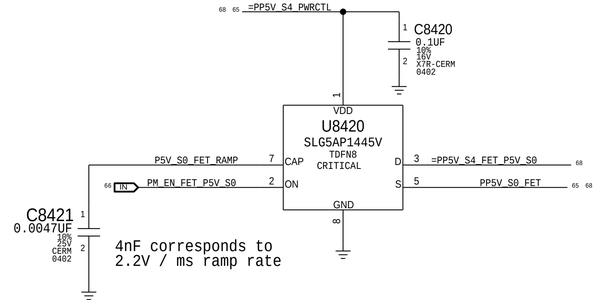
Rise Time For VD = 3.3V:
470 pF -- 603 us
1000 pF -- 1185 us

1.0V S3 FET



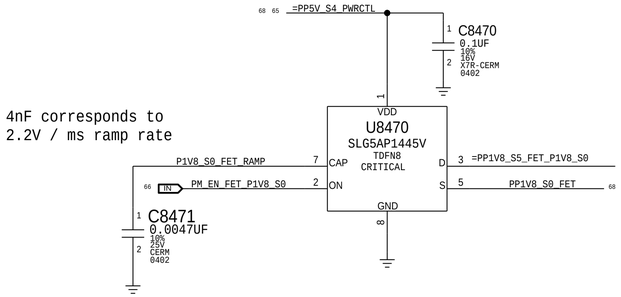
4nF corresponds to
2.2V / ms ramp rate

5V S0 FET

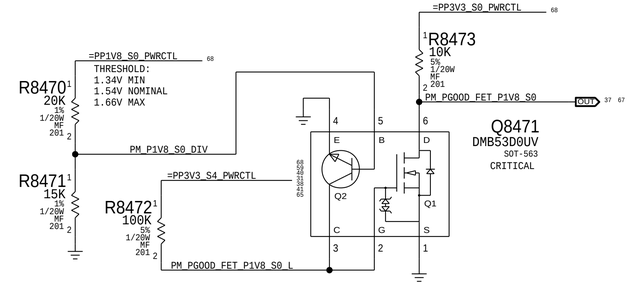


4nF corresponds to
2.2V / ms ramp rate

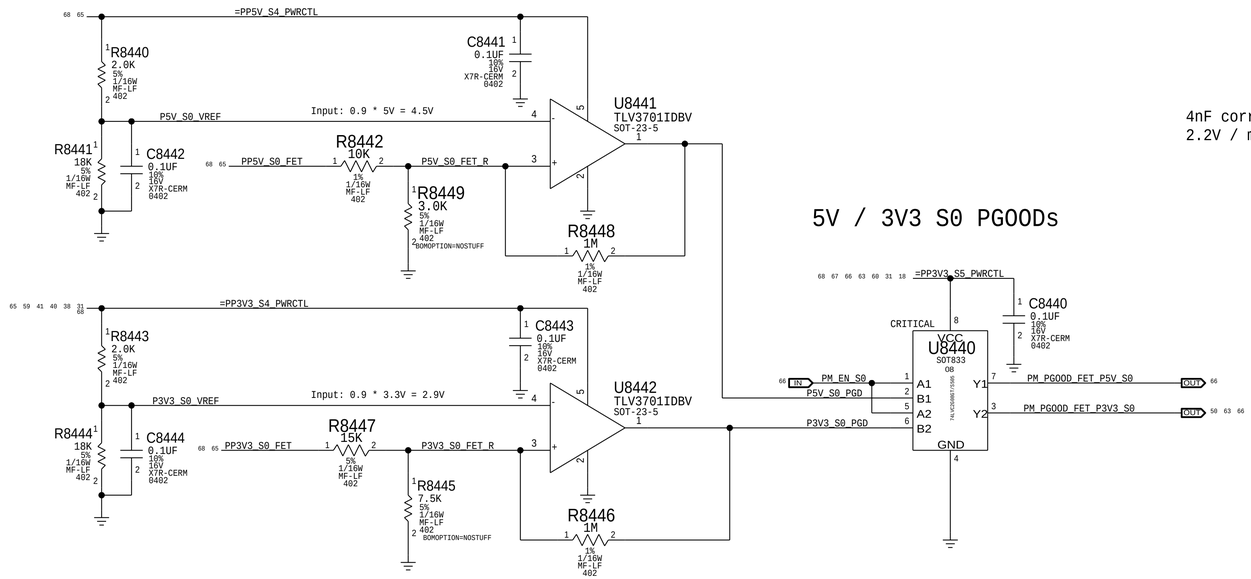
1.8V S0 FET & PGOOD



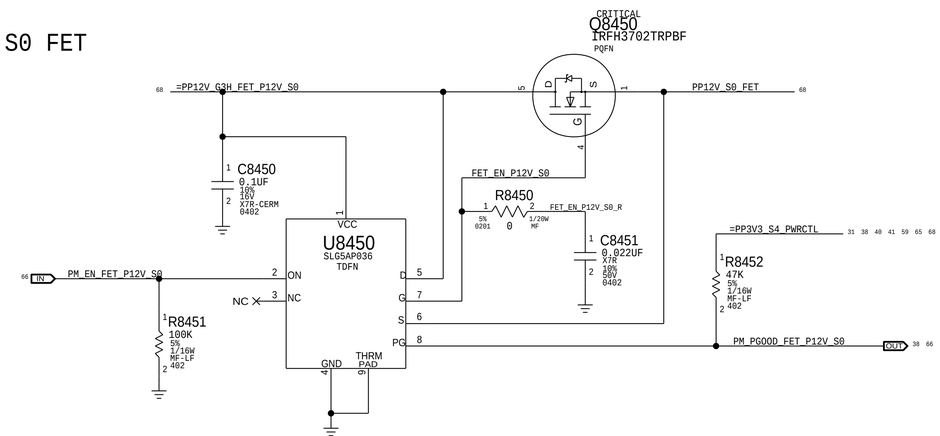
4nF corresponds to
2.2V / ms ramp rate



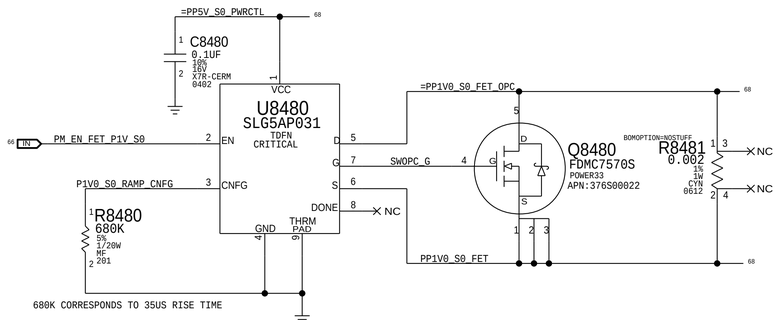
5V / 3V3 S0 PGOODs



12V S0 FET



1.0V S0 FET

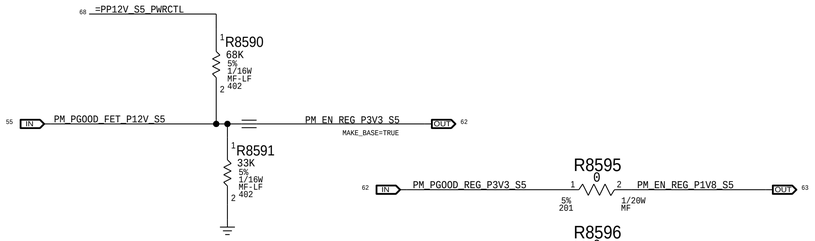


680K CORRESPONDS TO 35US RISE TIME

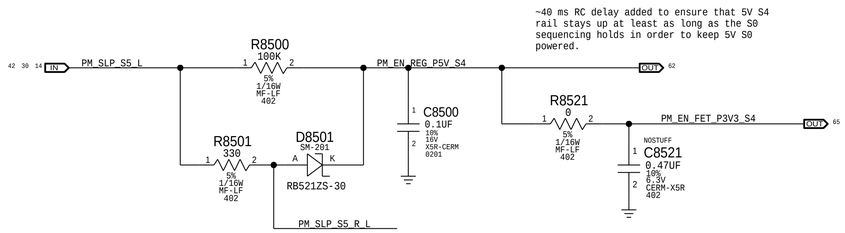
BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DTUZMAN_MLB	SYNC_DATE=05/24/2016
PAGE TITLE: PM FETs/PGoods	
Apple Inc.	DRAWING NUMBER: 051-01543 · SIZE: D
	REVISION: 3.13.0
	BRANCH:
	PAGE: 84 OF 105
	SHEET: 65 OF 70

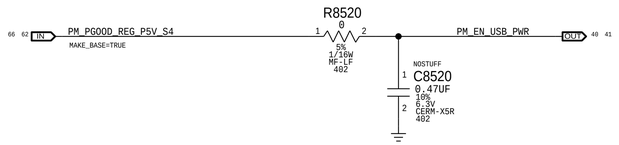
S5 Enable



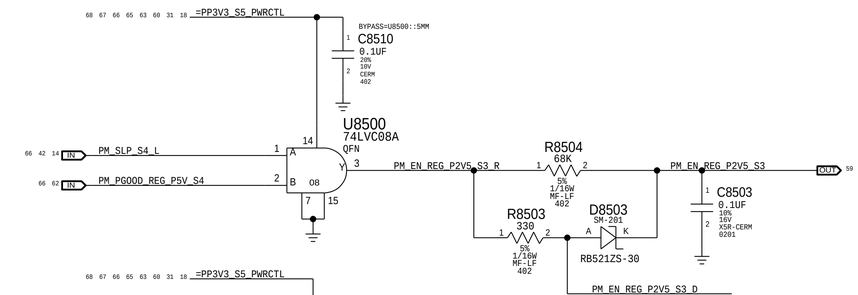
S4 Enables



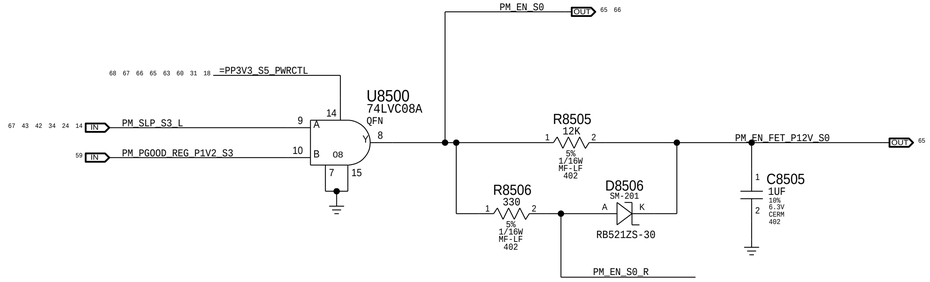
S4 USB Enable



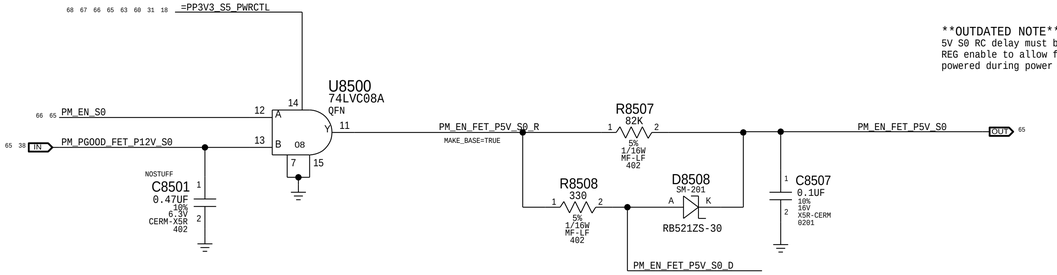
S3 Enables



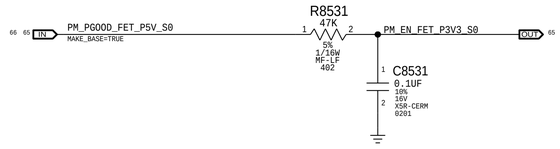
S0 Enables



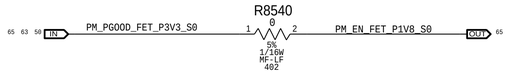
OUTDATED NOTE
12V S0 EN RC delay must be >= downstream delay on 4.5V REG enable which in turn enables 1.05V S0. This allows for 12V S0 to hold as long as 1.05V S0 regulator is powered.

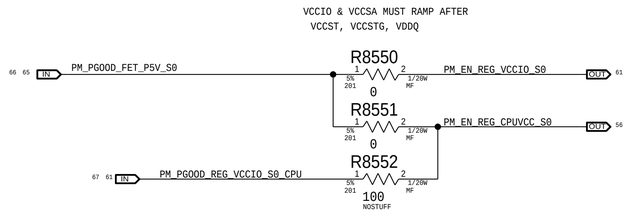


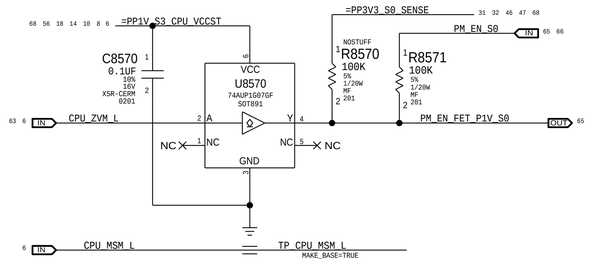
OUTDATED NOTE
5V S0 RC delay must be >= downstream delay on 4.5V REG enable to allow for 4.5V regulator to remain powered during power down sequence.



OUTDATED NOTE
No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 5V S0 on 1.05V VR page competing with logic turn on time.

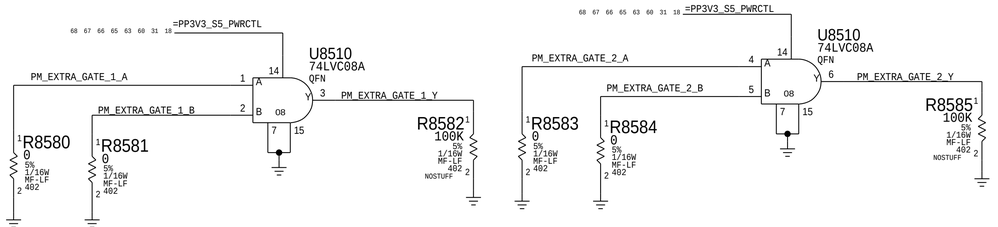






EXTRA GATES

CONSIDER REPLACING U8510 WITH DUAL-GATE



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DTUZMAN_MLB
SYNC_DATE=04/11/2016

PAGE TITLE
PM Regulator Enables

Apple Inc.

DRAWING NUMBER 051-01543
SIZE D
REVISION 3.13.0
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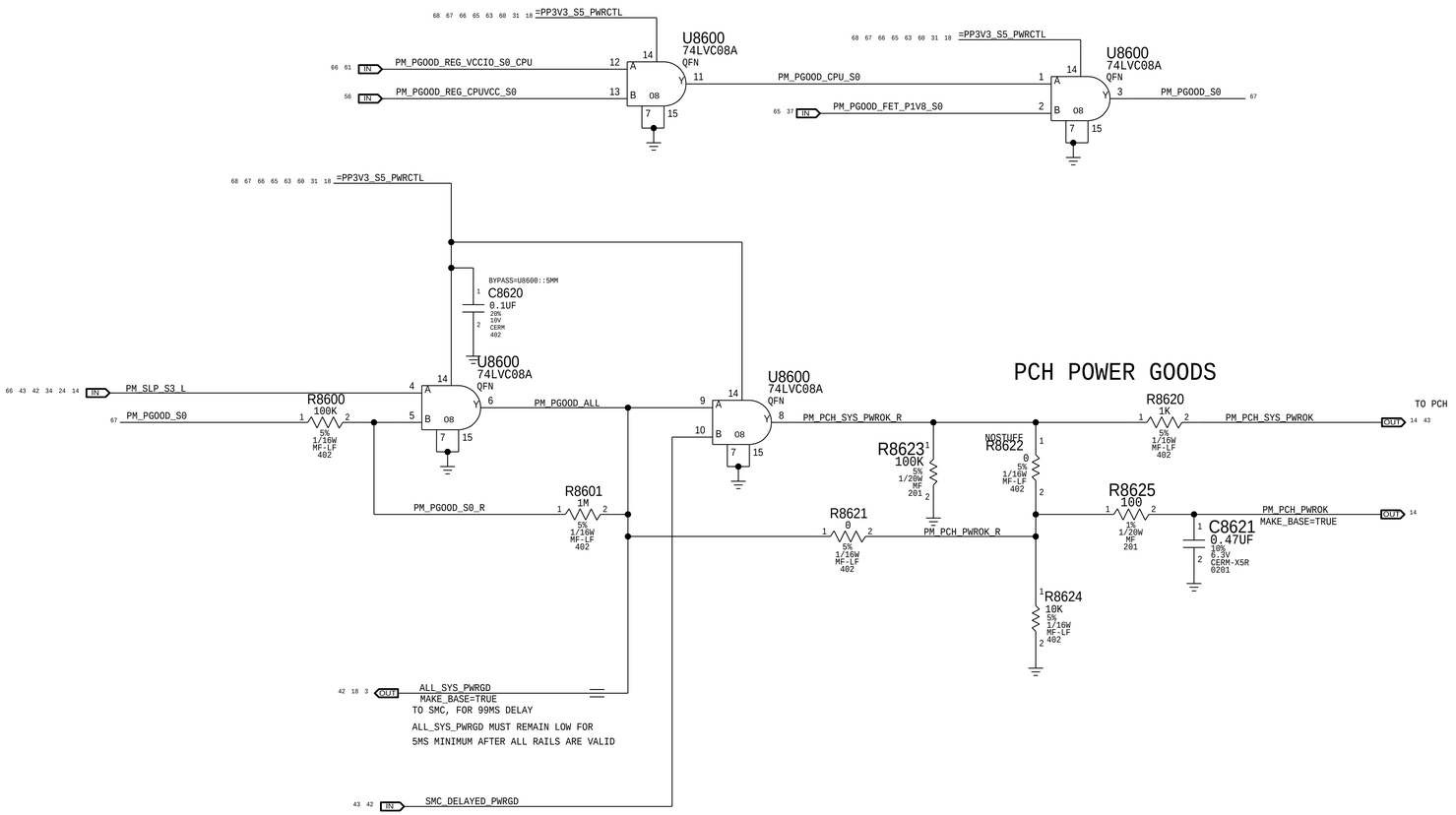
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



PCH POWER GOODS

Resume Reset

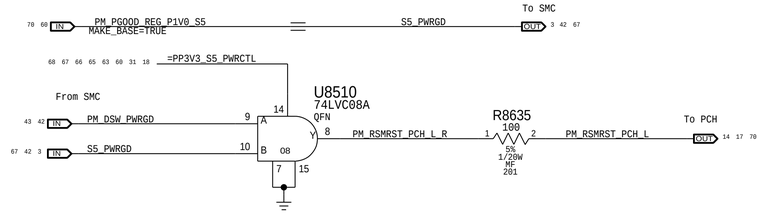
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



OUTDATED NOTES

Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 1.8V and 1.2V for DDR3

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DTUZMAN_MLB SYNC_DATE=04/05/2010

PAGE TITLE: PM Power Good

Apple Inc.

DRAWING NUMBER 051-01543 SIZE D
REVISION 3.13.0
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G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 18
- =PP3V_G3_PCH_VCCRTC — 8 12 14 15

G3H Rails

PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 55
- =PP12V_G3H_SNS_R — 46

PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 46
- =PP12V_G3H_REG_3V3_G3H — 55
- =PP12V_G3H_FET_P12V_S5 — 55
- =PP12V_G3H_FET_P12V_S0 — 65

PP3V3_G3H (MAKE_BASE=TRUE)
- PP3V3_G3H_REG — 55
- =PP3V3_G3H_BT — 30
- =PP3V3_G3H_SMC — 42 43 48
- =PP3V3_G3H_RTC_D — 18
- =PP3V3_G3H_T112 — 44 70
- =PP3V3_G3H_SMC_USBMUX — 40
- =PP3V3_G3H_SMBUS_SMC_4 — 45
- =PP3V3_G3H_USBC — 26

S5 Rails

Enabled when system has AC and is in S5

PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 55
- =PP12V_S5_REG_P3V3P5V_S5 — 62
- =PP12V_S5_REG_P1V2_S3 — 59
- =PP12V_S5_REG_P1V0_S5 — 60
- =PPHV_TBT_XA — 27
- =PPHV_TBT_XB — 28
- =PP12V_S5_SNS — 46
- =PP12V_S5_PWRCTL — 66

PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 62
- NBC =PP5V_S5_PWRCTL — 62 65
- =PP5V_S5_REG_P1V0_S5 — 60

PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG — 62
- =PP3V3_S5_SNS — 46
- =PP3V3_S5_FET_P3V3_S4 — 65
- =PP3V3_S5_FET_P3V3_S0 — 65
- =PP3V3_S5_FET_P3V3_SSD — 31
- =PP3V3_S5_REG_P1V8_S5 — 63
- =PP3V3_S5_PWRCTL — 18 31 60 63 65 66 67
- =PP3V3_S5_VRD — 62
- =PP3V3_S5_LED — 3
- =PP3V3_S5_PCH_VCCDSW — 8 14
- =PP3V3_SUS_PCH_VCCPRIM — 5 8 12
- =PP3V3_SUS_PCH_VCCSPI — 8
- =PP3V3_SUS_PCH_VCCRTCPRIM — 8 12
- =PP3V3_SUS_PCH_VCCPGPPA — 8 13 15 16
- =PP3V3_SUS_PCH_VCCPGPPB — 8 12 19
- =PP3V3_SUS_PCH_VCCPGPPC — 8 12
- =PP3V3_SUS_PCH_VCCPGPPD — 8
- =PP3V3_SUS_PCH_VCCPGPPE — 8 12
- =PP3V3_SUS_PCH_VCCPGPPG — 8
- =PP3V3_S5_ROM — 17 44
- =PP3V3_S5_SENSE — 46
- =PP3V3_S5_SMC — 43
- =PP3V3_S5_REG_P1V0_S0 — 63

PP1V8_S5 (MAKE_BASE=TRUE)
- PP1V8_S5_REG — 63
- =PP1V8_SUS_PCH_VCCPGPPF — 8 13 14
- =PP1V8_SUS_PCH_VCC1P8_SRC — 12
- =PP1V8_SUS_PCH_VCCATS — 8 12
- =PP1V8_S5_CPU_VCCOPC — 18
- =PP1V8_S5_FET_P1V8_S0 — 65
- =PP1V8_S5_CAMERA_FET — 36
- =PP1V8_S5_PCH_VCCHDA — 12 18

PP1V0_S5 (MAKE_BASE=TRUE)
- PP1V0_S5_REG — 60
- =PP1V_SUS_PCH_VCCPRIM — 8 12
- =PPVCCPRIMECORE_SUS_PCH — 8 12
- =PP1V_SUS_PCH_VCCMPHYAON — 8 12
- =PP1V_SUS_PCH_VCCAPLL — 12 15
- =PP1V_SUS_PCH_VCCCLK — 18
- =PP1V_SUSSW_PCH_VCCSRAM — 8 12
- =PP1V_SUSSW_PCH_VCCMPHYGT — 8 12
- =PP1V_SUSSW_PCH_VCCAMPHYPLL_SRC — 12
- =PP1V_SUSSW_PCH_VCCAPLLEBB — 8 12
- =PP1V0_S5_XDP — 17
- =PP1V_S5_FET_P1V_S3 — 65

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG — 62
- =PP5V_S4_SNS — 46
- =PP5V_S4_REG_P1V2_S3 — 59
- =PP5V_S4_FET_P5V_S0 — 65
- =PP5V_S4_PWRCTL — 65
- =PP5V_S4_USB — 40 41
- =PP5V_S4_USBC — 26
- =PP5V_S4_FET_P5V_HDD — 32
- =PP5V_S4_REG_CPUCORE — 56

PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 65
- =PP3V3_S4_FET_ENET — 34
- =PP3V3_S4_PWRCTL — 31 38 40 41 59 65
- =PP3V3_S4_LED — 3
- =PP3V3_S4_PCH_GPIO — 14 19
- =PP3V3_S4_SDCARD — 35
- =PP3V3_S4_SMC — 43
- =PP3V3_S4_TBT — 19
- =PP3V3_S4_AP — 19 30 43
- =PP3V3_UPC_XA_AUX — 27
- =PP3V3_UPC_XB_AUX — 28
- =PP3V3_S4_REG_P2V5_S3 — 59

PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 34
- =PP3V3_ENET_PHY — 33 34

S3 Rails

Enabled when system is in run or sleep

PP2V5_S3 (MAKE_BASE=TRUE, VOLTAGE=2.5V)
- PP2V5_S3_REG — 59
- =PPDDRVPP_S3_MEM_A — 22
- =PPDDRVPP_S3_MEM_B — 23

PP1V2_S3 (MAKE_BASE=TRUE)
- PP1V2_S3_REG — 59
- =PP1V2_S3_SNS_DDR_R — 46

PP1V2_S3_DDR (MAKE_BASE=TRUE)
- PP1V2_S3_SNS_DDR — 46
- =PP1V2_S3_LDO_DDRVTT — 59
- =PPVDDQ_S3_MEM — 7 21
- =PPVDDQ_S3_MEM_A — 22
- =PPVDDQ_S3_MEM_B — 23
- =PP1V2_S3_CPU_VDDQC — 8 10
- =PP1V2_S3_CPU_VDDQ — 8 10 59
- =PP1V2_S3_CPU_VCCPLLOC — 8 10
- =PP1V2_S3_MEM_VTTPWRCTL — 19
- =PP1V2_S3_CAMERA_FET — 37

PP1V0_S3 (MAKE_BASE=TRUE)
- PP1V0_S3_FET — 65
- =PP1V_S3_CPU_VCCST — 6 8 10 14 18 56 66
- =PP1V_S3_CPU_VCCPLL — 8 10
- =PP1V_S3_CPU_VCCSTG — 6 8 10 17
- =PP1V_S3_SMC — 43

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 65
- =PP12V_S0_SNS_CPUCORE_R — 46
- =PP12V_S0_AUDIO_SPKRAMP — 51 52
- =PP12V_S0_BKLT — 64
- =PP12V_S0_FAN — 48
- =PP12V_S0_LCD — 38

PP12V_S0_CPU (MAKE_BASE=TRUE)
- PP12V_S0_SNS — 46
- =PP12V_S0_CPUCORE — 57

PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 65
- =PP5V_S0_REG_CPUVCC_S0 — 57 58 61
- =PP5V_S0_BKLT — 64
- =PP5V_S0_FET_P5V_HDD — 32
- =PP5V_S0_CAMERA — 36 37
- =PP5V_S0_PCH_STRAP — 18
- =PP5V_S0_PWRCTL — 65
- =PP5V_S0_ISENSE — 46
- =PP5V_S0_REG_P1V0_OPC_S0 — 63

PP5V_S0_HDD (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 32
- =PP5V_S0_SATA — 32

PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 65
- =PP3V3_S0_VRD — 55 56 61
- =PP3V3_S0_AUDIO — 50 53
- =PP3V3_S0_DP — 38
- =PP3V3_S0_ENET — 33
- =PP3V3_S0_FAN — 48
- =PP3V3_S0_INTDPMUX — 39
- =PP3V3_S0_LED — 3
- =PP3V3_S0_TBT_X — 26
- =PP3V3_S0_PCH — 5 6 13 14 15 16 18 19
- =PP3V3_S0_MEM_A_SPD — 22
- =PP3V3_S0_MEM_B_SPD — 23
- =PP3V3_S0_SDCARD — 35
- =PP3V3_S0_SENSE — 31 32 46 47 66
- =PP3V3_S0_SMBUS — 45
- =PP3V3_S0_SMBUS_SMC_0 — 45
- =PP3V3_S0_SMBUS_SMC_1 — 38 45
- =PP3V3_S0_SMBUS_SMC_2 — 45
- =PP3V3_S0_SMBUS_SMC_3 — 45
- =PP3V3_S0_SMC — 43
- =PP3V3_S0_BKLT_VDDIO — 64
- =PP3V3_S0_CAMERA — 36 37
- =PP3V3_S0_ALS — 36
- =PP3V3_S0_MEM_VTTPWRCTL — 19
- =PP3V3_S0_PWRCTL — 65

PP3V3_SSD (MAKE_BASE=TRUE)
- PP3V3_SSD_FET — 31
- =PPVSSD_SNS_R — 46

PPVSSD (MAKE_BASE=TRUE)
- PPVSSD_SNS — 46
- =PPVSSD_CONN — 31

PP1V8_S0 (MAKE_BASE=TRUE)
- PP1V8_S0_FET — 65
- =PP1V8_S0_PCH — 14
- =PP1V8_S0_AUD_DIG_TOP — 36 49 51
- =PP1V8_S0_AUD_DIG_BOT — 49 50 52 53
- =PP1V8_S0_PWRCTL — 65
- =PP1V8_S0_CAMERA — 36

PP1V0_S0 (MAKE_BASE=TRUE)
- PP1V0_S0_OPC_REG — 63
- =PP1V0_S0_FET_OPC — 65

PP1V0_S0_OPC (MAKE_BASE=TRUE)
- PP1V0_S0_FET — 65
- =PP1V_S0_CPU_VCCOPC — 10 18
- =PP1V_S0_CPU_VCCEOPIO — 10 18

PP0V6_S0_DDRVTT (MAKE_BASE=TRUE)
- PPDDRVTT_S0_LDO — 59
- =PPDDRVTT_S0_MEM_A — 22
- =PPDDRVTT_S0_MEM_B — 23

PPVCCC_S0_CPU (MAKE_BASE=TRUE, VOLTAGE=0.9V)
- PPVCCC_S0_CPU_REG — 57
- =PPVCCCPU_S0_SENSE — 46
- =PPVCCC_S0_CPU — 8 10

PPVCCGT_S0_CPU (MAKE_BASE=TRUE, VOLTAGE=0.9V)
- PPVCCGT_S0_CPU_REG — 58
- =PPVCCGT_S0_CPU — 8 11
- =PPVCCGTX_S0_CPU — 8 11
- =PPVCCGT_S0_SENSE — 46

PPVCCSA_S0_CPU (MAKE_BASE=TRUE, VOLTAGE=0.9V)
- PPVCCSA_S0_CPU_REG — 57
- =PPVCCSA_S0_CPU — 8 10

PPVCCIO_S0_CPU (MAKE_BASE=TRUE, VOLTAGE=0.95V)
- PPVCCIO_S0_CPU_REG — 61
- =PP0V95_S0_CPU_VCCIO — 5 8 10

Ground/Common

GND\G (MAKE_BASE=TRUE, VOLTAGE=0V)

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PCH Miscellaneous

13	PCH_BSSB_CLK		NC_PCH_BSSB_CLK	MAKE_BASE=TRUE NO_TEST=1
13	PCH_BSSB_DATA		NC_PCH_BSSB_DATA	MAKE_BASE=TRUE NO_TEST=1
13	USBC_TMS_T_SWD_DATA_X		PU_USBC_TMS_T_SWD_DATA_X	MAKE_BASE=TRUE NO_TEST=1
15	TP_PCIE_CLK100M5P		NC_PCIE_CLK100M_FWP	MAKE_BASE=TRUE NO_TEST=1
15	TP_PCIE_CLK100M5N		NC_PCIE_CLK100M_FWN	MAKE_BASE=TRUE NO_TEST=1
15	TP_PCH_CLKREQ5_L		NC_PCH_CLKREQ5_L	MAKE_BASE=TRUE NO_TEST=1
15	TP_PCIE_CLK100M2P		NC_PCIE_CLK100M_CAMP	MAKE_BASE=TRUE NO_TEST=1
15	TP_PCIE_CLK100M2N		NC_PCIE_CLK100M_CAMN	MAKE_BASE=TRUE NO_TEST=1
15	TBT_T_CLKREQ2_L		NC_TBT_T_CLKREQ2_L	MAKE_BASE=TRUE NO_TEST=1
16	I2C_UPC_SDA		NC_I2C_UPC_SDA	MAKE_BASE=TRUE NO_TEST=1
16	I2C_UPC_SCL		NC_I2C_UPC_SCL	MAKE_BASE=TRUE NO_TEST=1
14	UPC_I2C_INT_L		PU_UPC_INT_L	MAKE_BASE=TRUE NO_TEST=1
16	TBT_T_PCI_RESET_L		NC_TBT_T_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=1
16	TBT_T_CIO_PWR_EN		NC_TBT_T_CIO_PWR_EN	MAKE_BASE=TRUE NO_TEST=1
16	TBT_T_USB_PWR_EN		NC_TBT_T_USB_PWR_EN	MAKE_BASE=TRUE NO_TEST=1
16	TBT_T_DPMUX_SEL		NC_TBT_T_DPMUX_SEL	MAKE_BASE=TRUE NO_TEST=1
15	SPKR_ID0		NC_SPKR_ID0	MAKE_BASE=TRUE NO_TEST=1
16	SPKR_ID1		NC_SPKR_ID1	MAKE_BASE=TRUE NO_TEST=1
16	TBT_X_DPMUX_SEL		NC_TBT_X_DPMUX_SEL	MAKE_BASE=TRUE NO_TEST=1
14	PCH_SOC_FORCE_DFU		NC_PCH_SOC_FORCE_DFU	MAKE_BASE=TRUE NO_TEST=1
14	PCH_SOC_DBELL		NC_SOC_WAKE_L	MAKE_BASE=TRUE NO_TEST=1
13	DEBUGUART_SEL_SOC		NC_DEBUGUART_SEL_SOC	MAKE_BASE=TRUE NO_TEST=1
13	PCH_SOC_WDOG_RESET		NC_PCH_SOC_WDOG	MAKE_BASE=TRUE NO_TEST=1
13	PCH_UART2_CTS_L		PD_PCH_UART2_CTS_L	MAKE_BASE=TRUE NO_TEST=1
14	SOC_SWD_CLK		PU_PCH_SWD_CLK	MAKE_BASE=TRUE NO_TEST=1
14	SOC_SWD_IO		PU_PCH_SWD_IO	MAKE_BASE=TRUE NO_TEST=1
14	SOC_SWD_MUX_SEL_PCH		PD_PCH_SWD_MUX_SEL	MAKE_BASE=TRUE NO_TEST=1
13	SOC_S2R_ACK_L		NC_SOC_S2R_ACK_L	MAKE_BASE=TRUE NO_TEST=1
13	SOC_PCH_DBELL_L		NC_SOC_SLEEP_L	MAKE_BASE=TRUE NO_TEST=1
14	PM_SLP_SUS_L		PD_PM_SLP_SUS_L	MAKE_BASE=TRUE
14	PCH_HSIO_PWR_EN		NC_PCH_HSIO_PWR_EN	MAKE_BASE=TRUE NO_TEST=1
8	VCCPRIM_CORE_VID1		NC_VCCPRIM_CORE_VID1	MAKE_BASE=TRUE NO_TEST=1
16	MLB_DEV_L		NC_MLB_DEV_L	MAKE_BASE=TRUE NO_TEST=1
16	PCH_BT_I2S_CLK		NC_BT_I2S_CLK	MAKE_BASE=TRUE NO_TEST=1
16	PCH_BT_I2S_SYNC		NC_BT_I2S_SYNC	MAKE_BASE=TRUE NO_TEST=1
16	PCH_BT_I2S_R2D		NC_BT_I2S_R2D	MAKE_BASE=TRUE NO_TEST=1
16	PCH_BT_I2S_D2R		NC_BT_I2S_D2R	MAKE_BASE=TRUE NO_TEST=1
36	TP_CS_PWD_L		NC_CS_PWD_L	MAKE_BASE=TRUE NO_TEST=1
36	TP_ISM_CLK		NC_ISM_CLK	MAKE_BASE=TRUE NO_TEST=1
36	TP_ISM_RST_L		NC_ISM_RST_L	MAKE_BASE=TRUE NO_TEST=1
36	TP_CAM_GPIO1		NC_CAM_GPIO1	MAKE_BASE=TRUE NO_TEST=1

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Unused Signal Aliases

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XDP DEBUG TEST POINTS

		FUNC_TEST		
I1	XDP_CPU_PRDY_L	TRUE	15	17
I2	XDP_CPU_PREQ_L	TRUE	15	17
I54	XDP_CPU_TCK	TRUE	6	17
I55	PCH_JTAGX	TRUE	6	17
I56	XDP_PCH_TCK	TRUE	6	17
I57	XDP_CPU_TMS	TRUE	6	17
I58	XDP_PCH_TMS	TRUE	6	17
I59	XDP_CPU_TRST_L	TRUE	6	17
I60	XDP_PCH_TRST_L	TRUE	6	17
I61	XDP_CPU_TDI	TRUE	6	17
I62	XDP_PCH_TDI	TRUE	6	17
I63	XDP_CPU_TDO	TRUE	6	17
I64	XDP_PCH_TDO	TRUE	6	17
I65	CPU_CFG<3>	TRUE	6	17
I66	SPI_IO_R<2>	TRUE	13	17 44
I71	ITP_PMODE	TRUE	6	17
I72	PM_RSMRST_PCH_L	TRUE	14	17 67

I53	CPU_CATERR_L	TRUE	6	43
I69	SMBUS_PCH_CLK	TRUE	13	45
I70	SMBUS_PCH_DATA	TRUE	13	45
I123	TP_CPU_PWRGD	TRUE	14	

TPA550 TP TP-P6 — XDP_BPM_L<2> — 6

TPA551 TP TP-P6 — XDP_BPM_L<3> — 6

TPA557 TP TP-P6 — PM_SYSRST_L — 14 18 42

USB-C TEST POINTS

		FUNC_TEST		
I79	TP_UPC_XA_DBG_UART_TX	TRUE	27	
I80	TP_UPC_XA_DBG_UART_RX	TRUE	27	
I81	TP_UPC_XB_DBG_UART_TX	TRUE	28	
I82	TP_UPC_XB_DBG_UART_RX	TRUE	28	
I83	TP_UPC_XA_SWD_CLK	TRUE	27	
I84	TP_UPC_XA_SWD_DATA	TRUE	27	
I85	TP_UPC_XB_SWD_CLK	TRUE	28	
I86	TP_UPC_XB_SWD_DATA	TRUE	28	
I76	UPC_XA_FAULT_L	TRUE	19	27
I77	UPC_XB_FAULT_L	TRUE	19	28

28 I78 =USBC_XB_RESET_L — TP_USBC_XB_RESET_L (MAKE_BASE=TRUE)

TPA560 TP TP-P6 — DP_INT_SPDIF_AUDIO — 38

TPA561 TP TP-P6 — PM_PGOOD_REG_P1V0_S5 — 60 67

Connector FuncTest Points

		FUNC_TEST		
I89	SMIA_DATA_N	TRUE	36	
I90	SMIA_DATA_P	TRUE	36	
I92	SMIA_CLK_N	TRUE	36	
I91	SMIA_CLK_P	TRUE	36	
I93	I2C_CAMSENSOR_SDA	TRUE	36	
I94	I2C_CAMSENSOR_SCL	TRUE	36	
I95	PP5V_S0_CAMERA_F	TRUE	36	
I96	SMB_ALS_F_SDA	TRUE	36	
I97	SMB_ALS_F_SCL	TRUE	36	
I98	PP1V8_S0_CAMERA_F	TRUE	36	
I99	PP3V3_S0_ALS_F	TRUE	36	
I100	AUD_DMIC1_DATA	TRUE	36	49
I101	AUD_DMIC1_CLK	TRUE	36	49
I124	PP1V8_DMIC_CONN1	TRUE	36	
I102	PP12V_LCD	TRUE	38	
I103	PANEL_PGOOD	TRUE	38	
I104	SMB_DP_TCON_SLA_SDA	TRUE	38	
I105	SMB_DP_TCON_SLA_SCL	TRUE	38	
I106	DP_INTPNL_HPD_R	TRUE	38	
I107	DP_INTPNL_AUX_N	TRUE	38	39
I108	DP_INTPNL_AUX_P	TRUE	38	39
I109	DP_INTPNL_ML_P<0>	TRUE	38	39
I110	DP_INTPNL_ML_N<0>	TRUE	38	39
I111	DP_INTPNL_ML_P<1>	TRUE	38	39
I112	DP_INTPNL_ML_N<1>	TRUE	38	39
I113	VIDEO_ON	TRUE	38	
I114	BKLT_VSYNC	TRUE	38	64
I120	=PP3V3_G3H_I112	TRUE	44	68
I126	SPI_CLK	TRUE	44	
I127	SPI_ALT_MOSI	TRUE	44	
I128	SPI_CS0_L	TRUE	44	
I129	SPI_ALT_MISO	TRUE	44	
I131	SPIROM_USE_MLB	TRUE	16	44
I132	SPI_IO<2>	TRUE	44	
I133	SMC_TMS	TRUE	26	42 43 44
I134	SPI_IO<3>	TRUE	44	
I135	SMC_TCK	TRUE	26	42 43 44
I136	SMC_RESET_L	TRUE	26	42 43 44
I115	FAN_0_PWM_FILT	TRUE	48	
I116	FAN_0_TACH_FILT	TRUE	48	
I117	PP12V_S0_FAN_0_FILT	TRUE	48	
I137	AUD_SPKR_LWFR_OUT_N	TRUE	51	
I138	AUD_SPKR_LWFR_OUT_P	TRUE	51	
I139	AUD_SPKR_VENDOR_ID_LT	TRUE	49	51
I141	AUD_SPKR_LTWT_OUT_N	TRUE	51	
I140	AUD_SPKR_LTWT_OUT_P	TRUE	51	
I143	AUD_SPKR_RWFR_OUT_N	TRUE	52	
I144	AUD_SPKR_RWFR_OUT_P	TRUE	52	
I145	AUD_SPKR_VENDOR_ID_RT	TRUE	49	52
I146	AUD_SPKR_RTWT_OUT_N	TRUE	52	
I142	AUD_SPKR_RTWT_OUT_P	TRUE	52	
I119	PWR_BTN_R	TRUE	55	
I118	SNS_ACDC_N	TRUE	47	55
I121	SNS_ACDC_P	TRUE	47	55
I125	BURSTMODE_EN_R_L	TRUE	55	
I122	SMC_ACDC_ID	TRUE	43	55
I148	PGND_BKLT	TRUE	64	
I150	LED_RETURN_6	TRUE	64	
I151	LED_RETURN_5	TRUE	64	
I149	LED_RETURN_4	TRUE	64	
I147	BKLT_BOOST_1	TRUE	64	
I152	BKLT_BOOST_2	TRUE	64	
I153	LED_RETURN_3	TRUE	64	
I154	LED_RETURN_2	TRUE	64	
I155	LED_RETURN_1	TRUE	64	

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Functional / ICT Test

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