Layout Dell logo

REV: X00
PWB: XXXXX
DATE: 1450-06

PCB R3: 20201124 PCB R3 PN

ZZZ1 PCBT@
PCB 3AA LA-K741P REV1 M/B TRIPOD A31 !
DAB00087011

ZZZ1 PCBU@
PCB 3AA LA-K741P REV1 M/B UNITECH A31 !
DAB00087012

ZZZ1 PCBG@
PCB 3AA LA-K741P REV1 M/B GOLD A31 !
DAB00087013

ZZZ1 PCBC@
PCB 3AA LA-K741P REV1 M/B COMPEQ A31 !
DAB00087014

Dell/Compal Confidential

Schematic Document

(Viper Comet Lake H-R with nVIDIA GN20)

2020-12-03
Rev: 1.0 (A00)

BOM Structure

PCB@/PCBG@/PCBT@/PCBU@/PCBC@ : PCB PN
PCH@: PCH P/N
EC@: EC Chip P/N
NV@: BIOS board ID (GPU type)
GN20_E3@/GN20_E4@/GN20_E5@/GN20_E7@/N20YES@/: GPU_ID & GPU Chip
VRAM_S8@/VRAM_M8@/VRAM_H8@/VRAM_S16@/VRAM_M16@/VRAM_H16@: VRAM Strap Pin
TYPEC@/RTD3@: TBT
LCDTESTEC@: LCD Test
CMC@: CMC Debug Port
128@/256@: ROM Type
RF@/EMI@/ESD@/ TYPEC@RF@ : EMI, ESD and RF Component
CML@: CML platform
CONN@:Connector
DDP16G@/SDP8G@: DDR4 DDP & SDP
SAM8G@/HYX8G@/MCN8G@/MCN8G1@/SAM16G@/HYX16G@/MCN16G@/MCN16G1@/SAM32G@/MCN32G@: DDR4 Chip
S_8G@/H_8G@/M_8G@/M_8G1@/S_16G@/S_16G1@/H_16G@/H_16G1@/M_16G@/M_16G1@/S_32G@/S_32G1@/H_32G@/M_32G@: PCH DDR4 ID Strap pin
@RTD3@/@TBT@:TBT RTD3 Un-POP Component
HMO16S32@: Hynix/Micron old die 16G & S32G T7 pin
MCNGD8A@/MCNGD6A@/SAMGD6A@/SAMGD8A@/
VM6GR3@/VS6GR3@/VH6GR3@/VM8GR3@/VS8GR3@/VH8GR3@/VS16GR3@:VRAM CHIP @: Un-pop Component

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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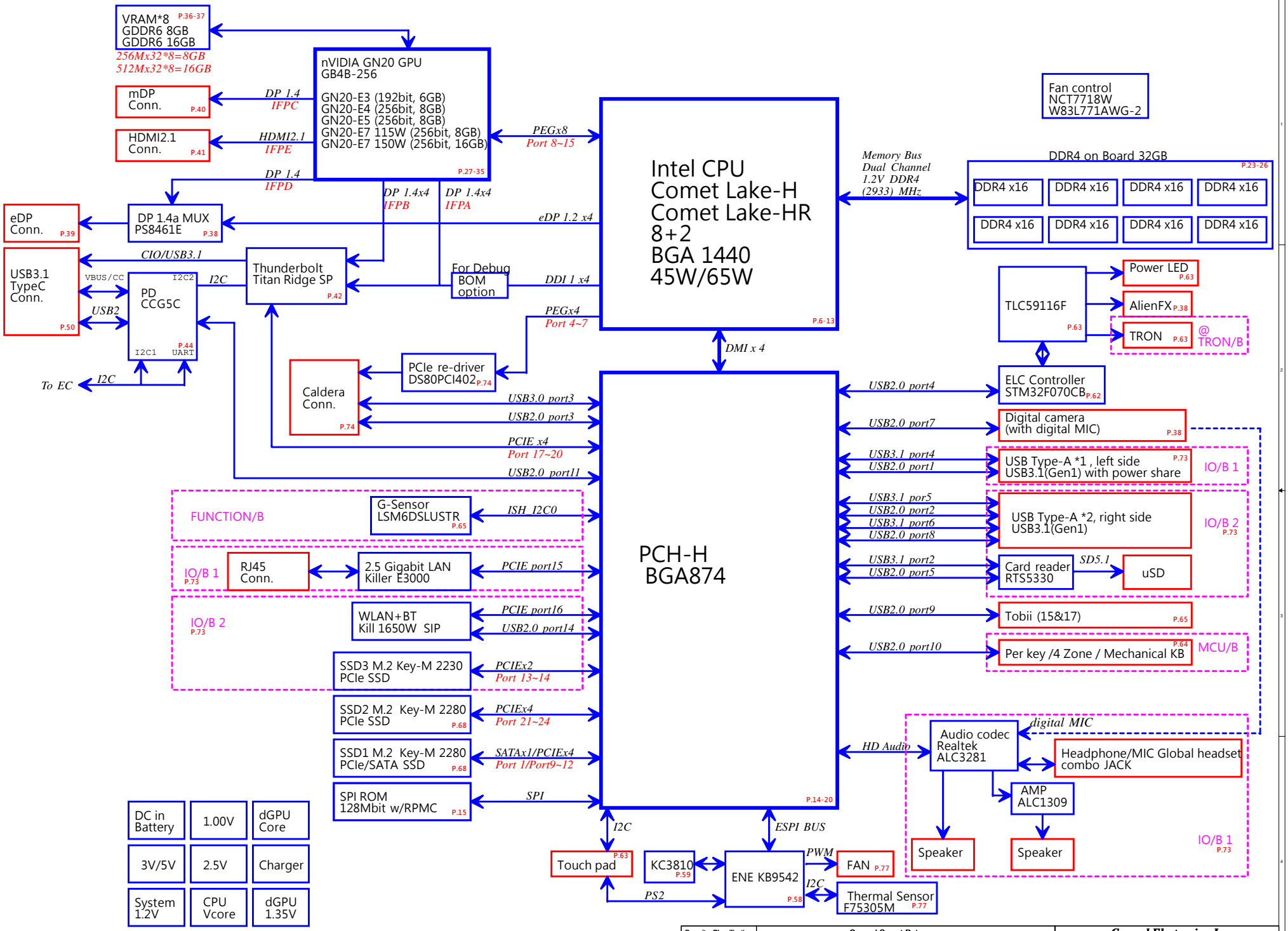
Title: *Cover Page*

Size | Document Number: *LA-K741P* | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 1 of 114



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **Block Diagram**

Size: | Document Number: **LA-K741P** | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 2 of 114

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 – 0x13	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 – 0x1E	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F – 0x25	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 – 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 – 0x3A	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B – 0x45	NVIDIA Graphic
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 – 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 – 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 – 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 – 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 – 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 – 0xA4	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 – 0xAF	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 – 0xB7	AMD Graphic
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 – 0xBF	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 – 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA – 0xD4	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 – 0xDD	Reserve
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE – 0xF0	
19	1.2M +/- 1%	3.020V	3.046V	3.067V	0xF1 – 0xFF	

PCIE CLK table

PCIE CLK	PCB Revision
0	GPU
1	SSD2
2	SSD3/WWAN
3	TBT
4	LAN
5	WLAN
6	caldera
7	SSD1

Board ID table

NVIDIA			AMD	PCB Revision
N18P	N18E		Navi14	
	2 Stage	1 Stage		
0	4	8	12	EVT-1
1	5	9	13	DVT-1
2	6	10	14	DVT-2
3	7	11	15	Pilot
16	17	18	19	Reserved

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

PCH-H CM246

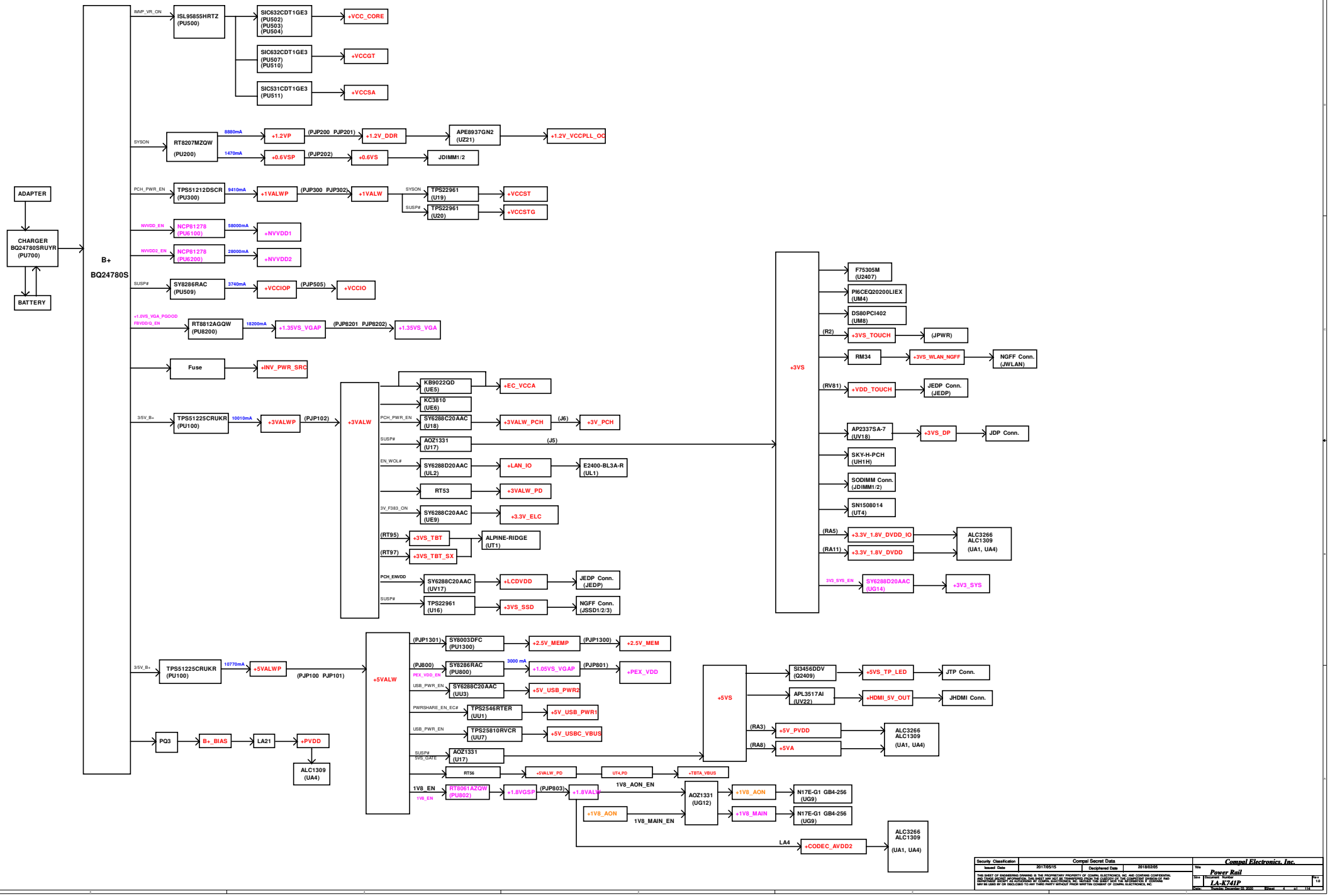
HSIO	USB3.1	PCIe	SATA3	Function	
0	1				
1	2			Card reader	
2	3			Caldera	
3	4			JUSB3 left side	
4	5			JIO right side USB2	
5	6			JIO right side USB1	
6	7	1			
7	8	2			
8	9	3			
9	10	4			
10		5			
11		6			
12		7			
13		8			
14		9		JSSD1 , 2280 SATA/PCIe x4	
15		10			
16		11	0a		
17		12	1a		
18		13	0b	WWAN	JSSD3 PCIE X2
19		14	1b		
20		15	2	LAN	
21		16	3	WLAN	
22		17	4	TBT PCIE X4	
23		18	5		
24		19			
25		20			
26		21		JSSD2 , 2280 PCIe x4	
27		22			
28		23			
29		24			

USB2	Function
1	JUSB3 left side
2	JIO right side USB1
3	Caldera
4	ELC
5	Card reader
6	WWAN
7	Camera
8	JIO right side USB2
9	Tobii
10	Per Key
11	Thunderbolt PD
12	Tron light
13	
14	Bluetooth

Symbol Note :

Digital Ground

Analog Ground



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Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title: Power Rail
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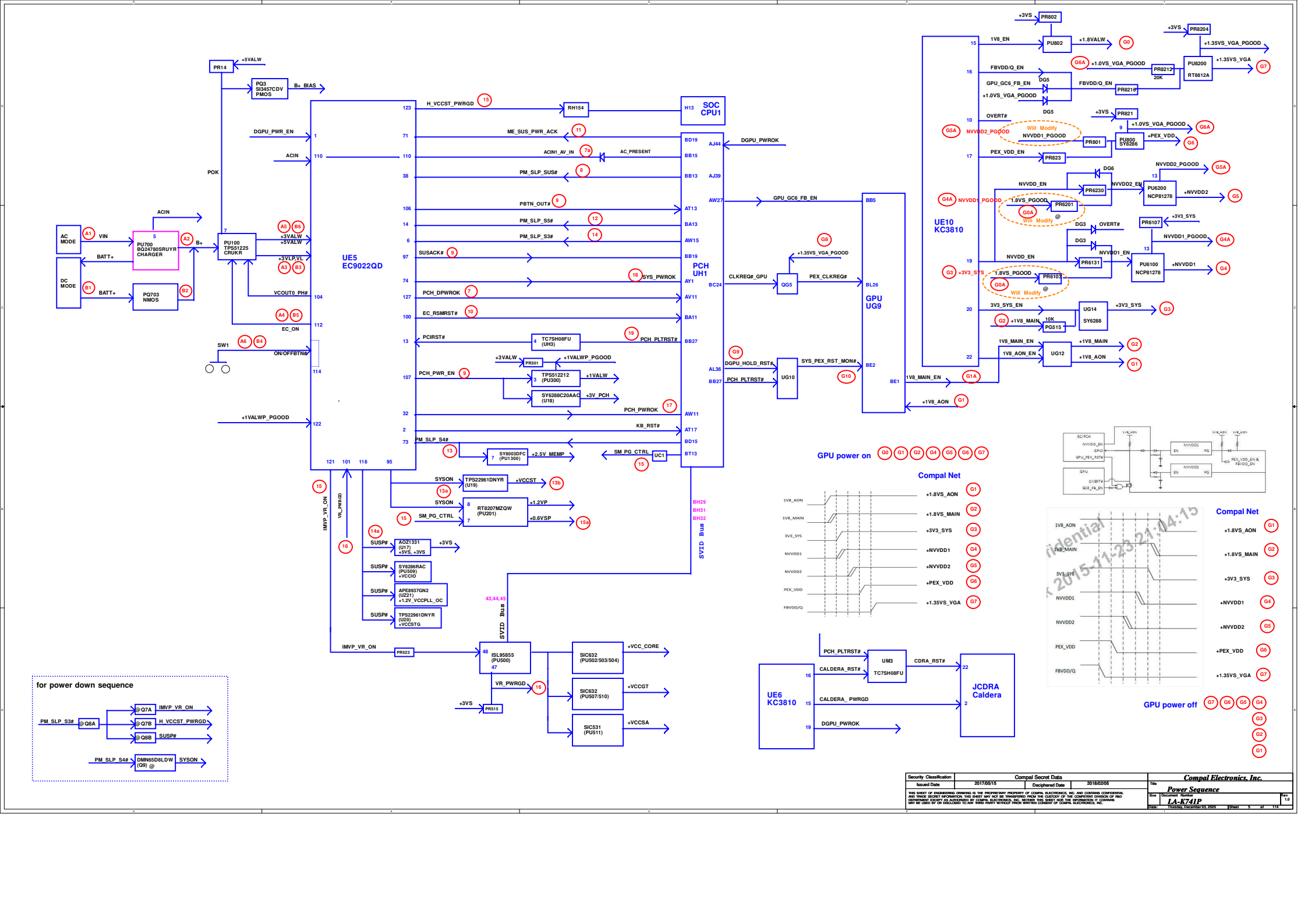
			Date: Thursday, December 28, 2017 Sheet: 4 of: 114



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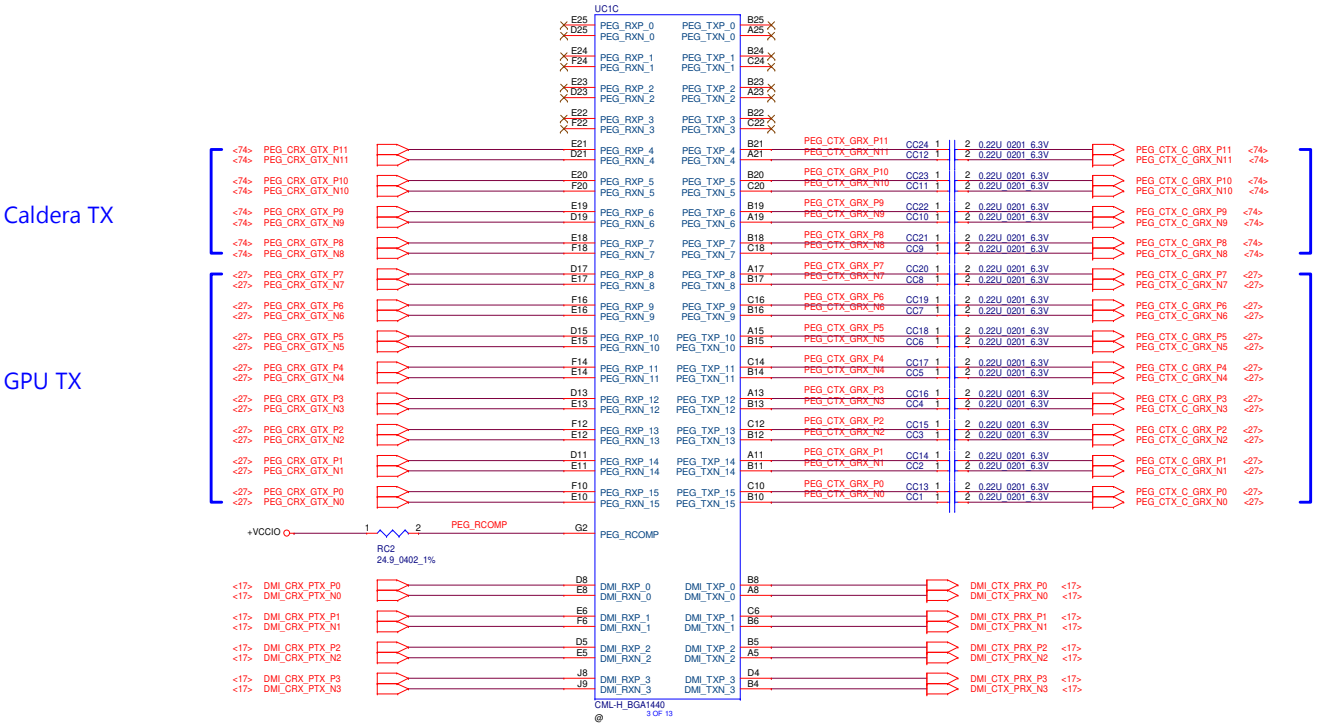
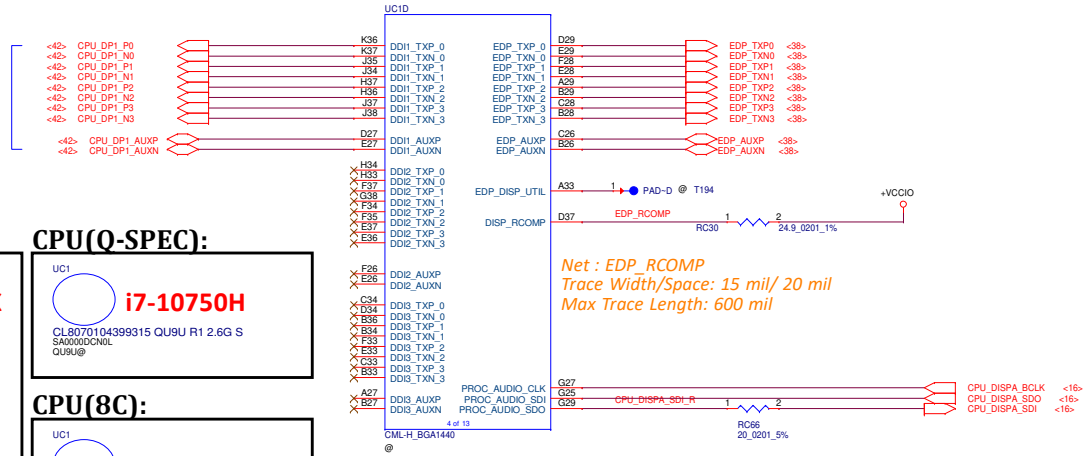
Issued Date	2017/05/15	Deciphered Date	2018/02/05
Title	Power Sequence		
Size	Document Number		Rev
	LA-K741P		1.0
Date: Thursday, December 03, 2020	Sheet 5 of 114		





CPU(S-SPEC):

FOR TBT DDI1

UC1

i7-10870H(Refersh)

S IC CL8070104399317 SRK3Y R1 2.2G A31 !
SA0000DW22L
SRK3Y@

CPU R1:

UC1 **i9-10980HK**
CL8070104502004 SRH8T R1 2.4G
SA0000DCE1L
SRH8TR1@

UC1 **i7-10750H**
CL8070104399315 SRH8Q R1 2.6G FCBGA
SA0000DCN1L
SRH8QR1@

UC1 **i5-10300H**
CL8070104399510 SRH84 R1 2.5G FCBGA
SA0000DCP1L
SRH84R1@

CPU R3:

UC1 **i9-10980HK**
CL8070104502004 SRH8T R1 2.4G A31 !
SA0000DCE2L
SRH8TR3@

UC1 **i7-10750H**
CL8070104399315 SRH8Q R1 2.6G A31 !
SA0000DCN2L
SRH8QR3@

UC1 **i5-10300H**
CL8070104399510 SRH84 R1 2.5G A31!
SA0000DCP2L
SRH84R3@

CPU(Q-SPEC):

UC1 **i7-10750H**
CL8070104399315 QU9U R1 2.6G S
SA0000DCN0L
QU9U@

CPU(8C):

UC1 **i7-10875H (8C)**
CL8070104399111 SRJ8F R1 2.3G A31 !
SA0000DIQ1L
SRJ8FR3@

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(1/7) DMI,PEG,DDI,EDP**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 6 of 114

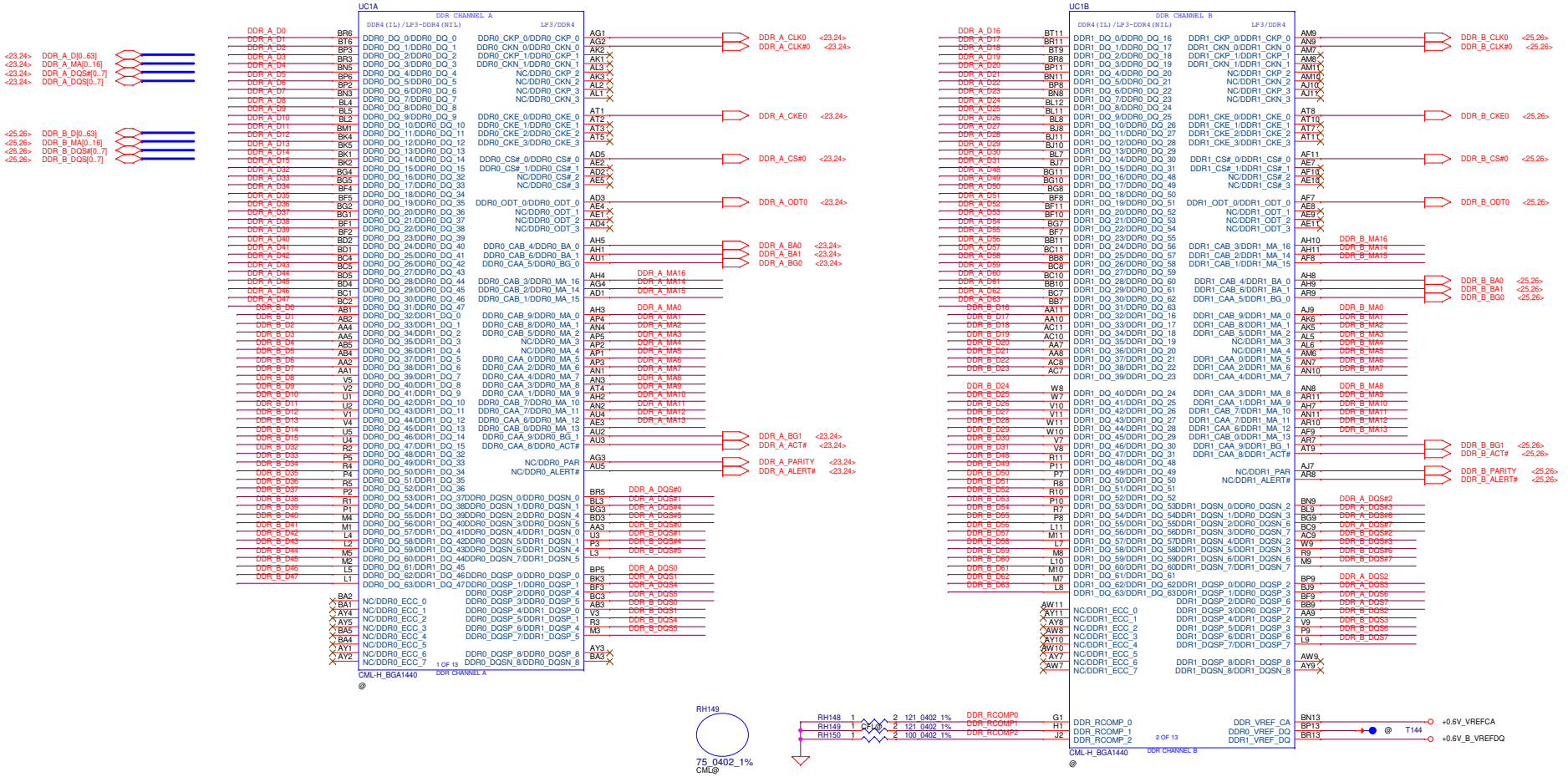
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CMC Conn**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 7 of 114



Net : DDR_RCOMP0
Net : DDR_RCOMP1
Net : DDR_RCOMP2
Trace Width/Space: 15 mil/ 25 mil
Max Trace Length: 500 mil

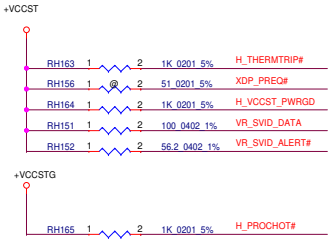
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

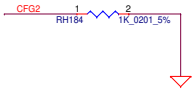
Title: **CPU(2/7) DDR4**

Size	Document Number	Rev
	LA-K741P	1.0

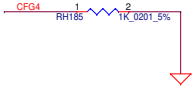
Date: Thursday, December 03, 2020 | Sheet 8 of 114



PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

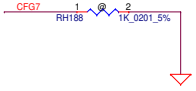


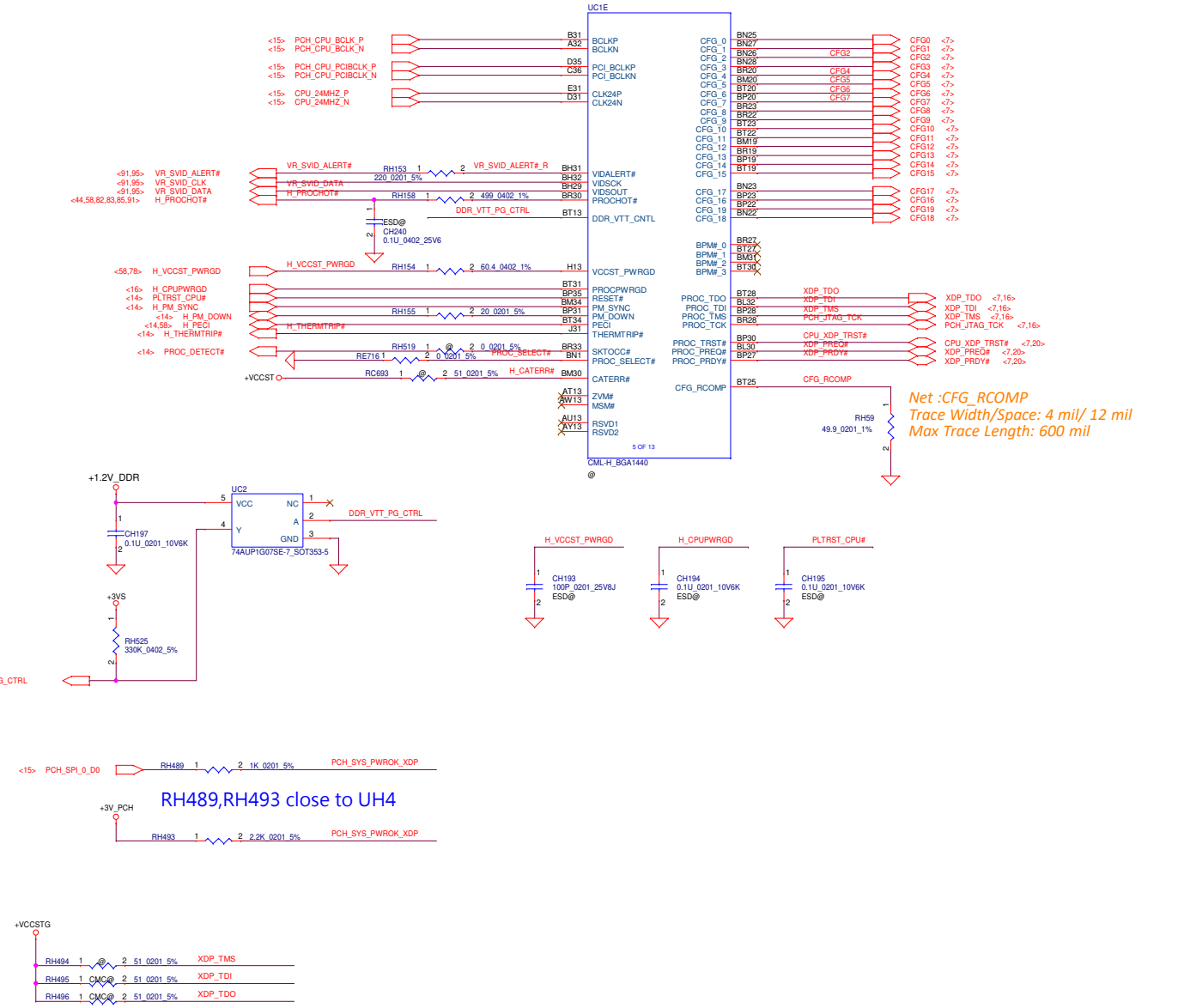
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) *00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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Issued Date	2017/05/15	Deciphered Date	2018/02/05

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Title: CPU(3/7) CFG,XDP

Size	Document Number	Rev
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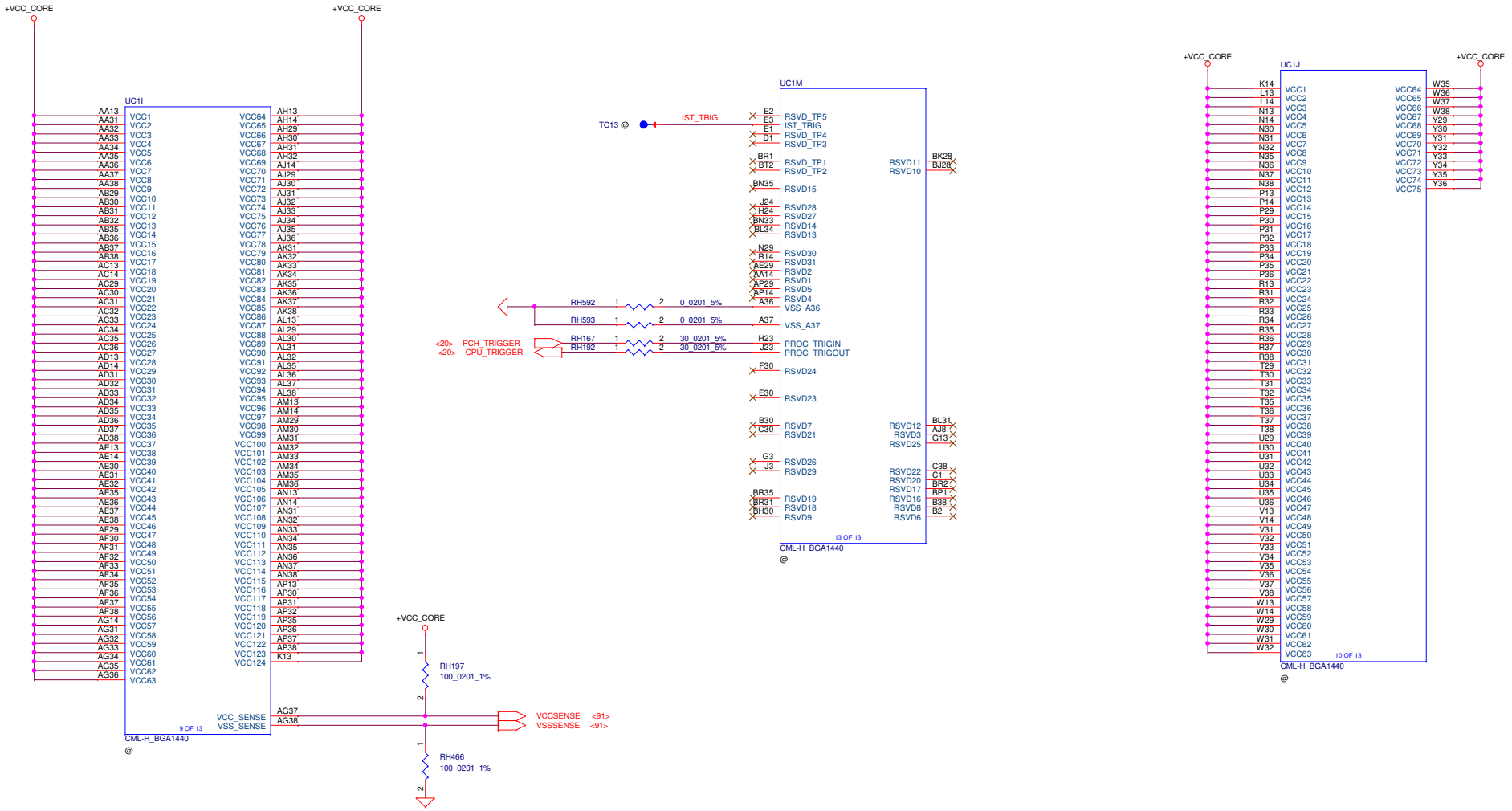
Date: Thursday, December 03, 2020 | Sheet 9 of 114



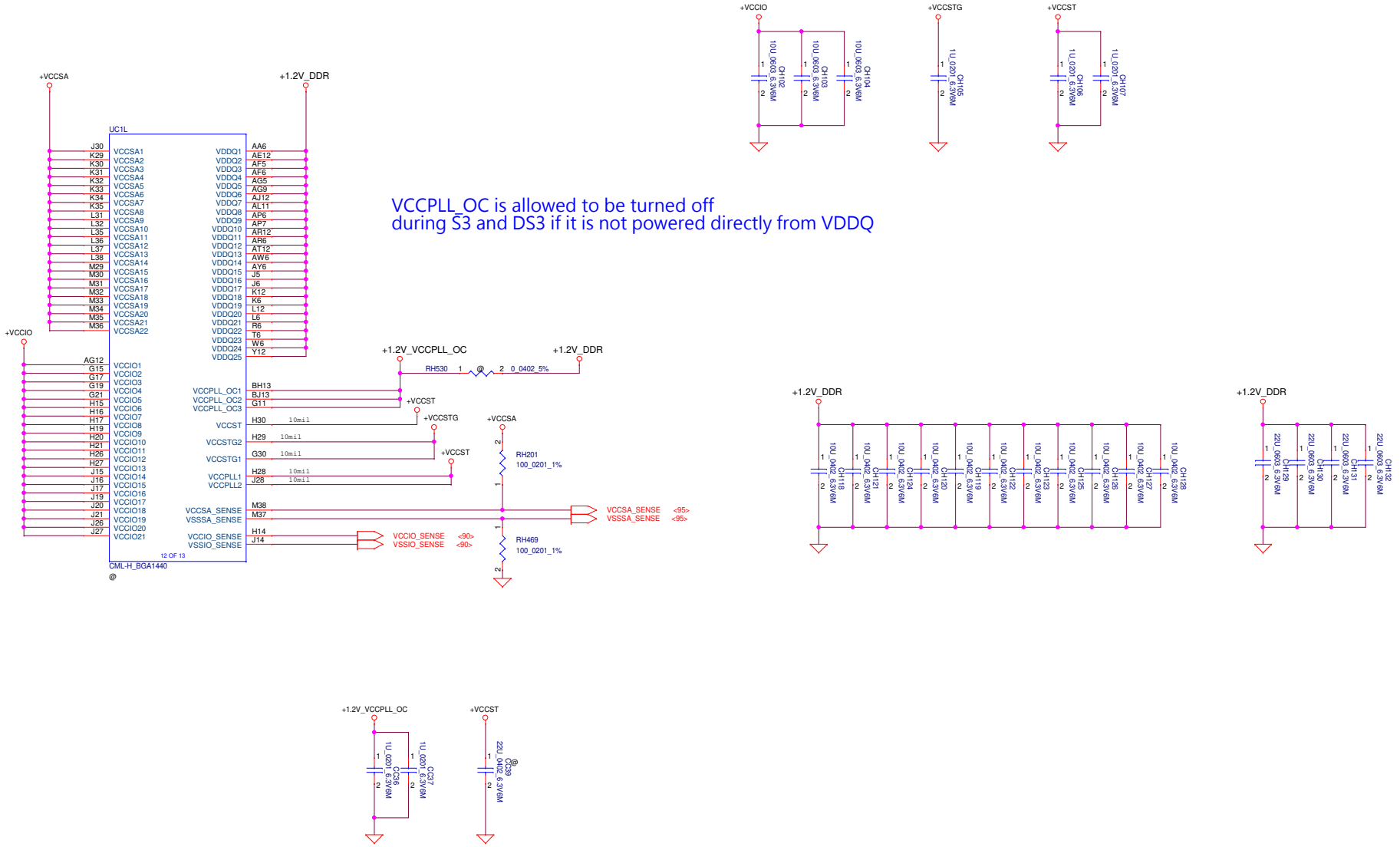
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(4/7) +VCC_CORE,RSVD**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 10 of 114



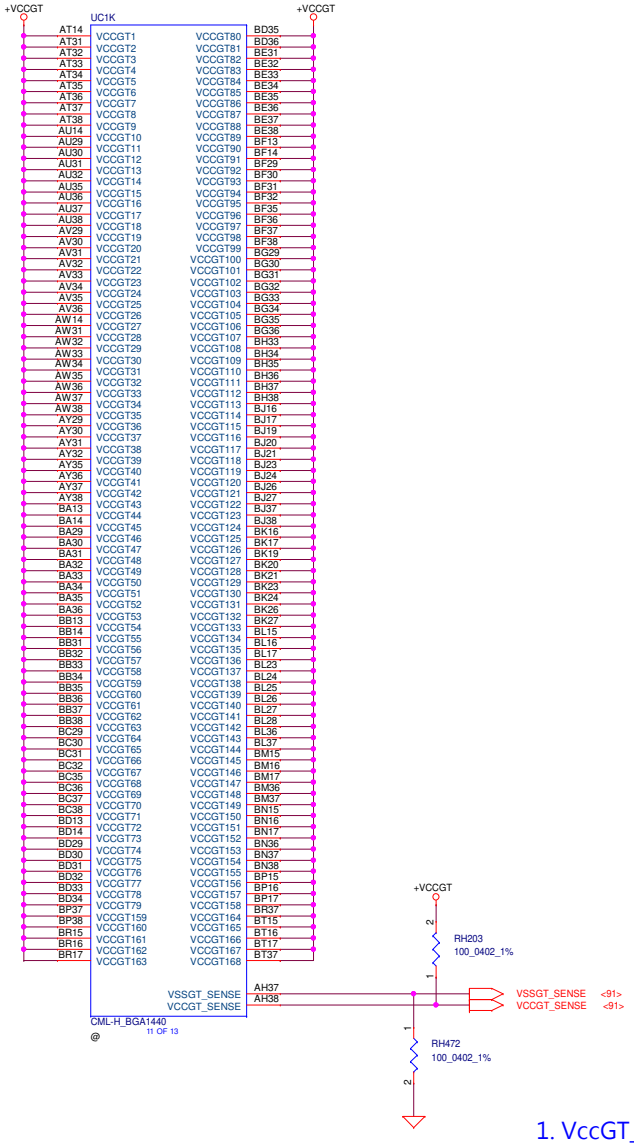
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(5/7) +VCCSA,+VCCIO**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 11 of 114



1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(6/7) +VCCGT**

Size	Document Number	Rev
	LA-K741P	1.0

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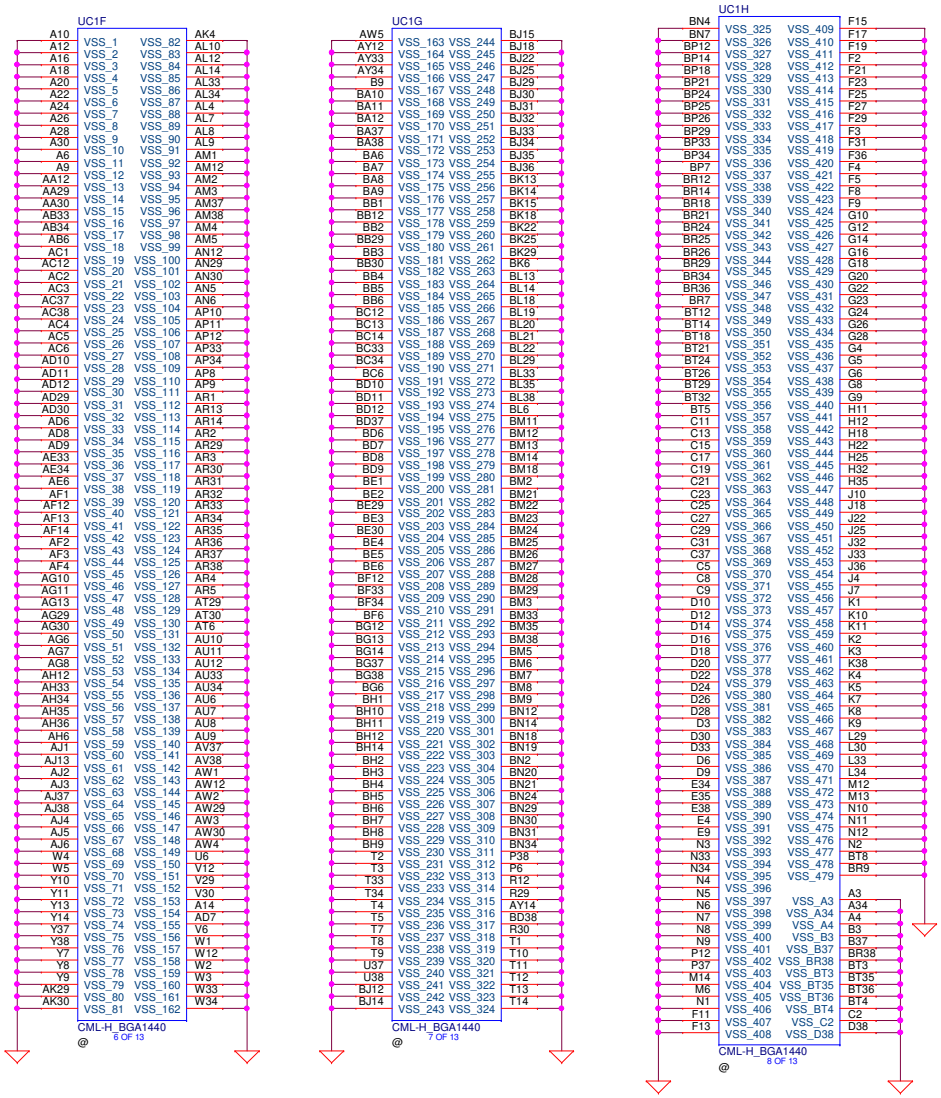


Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **CPU(7/7) VSS**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 13 of 114

PCH:

UH1

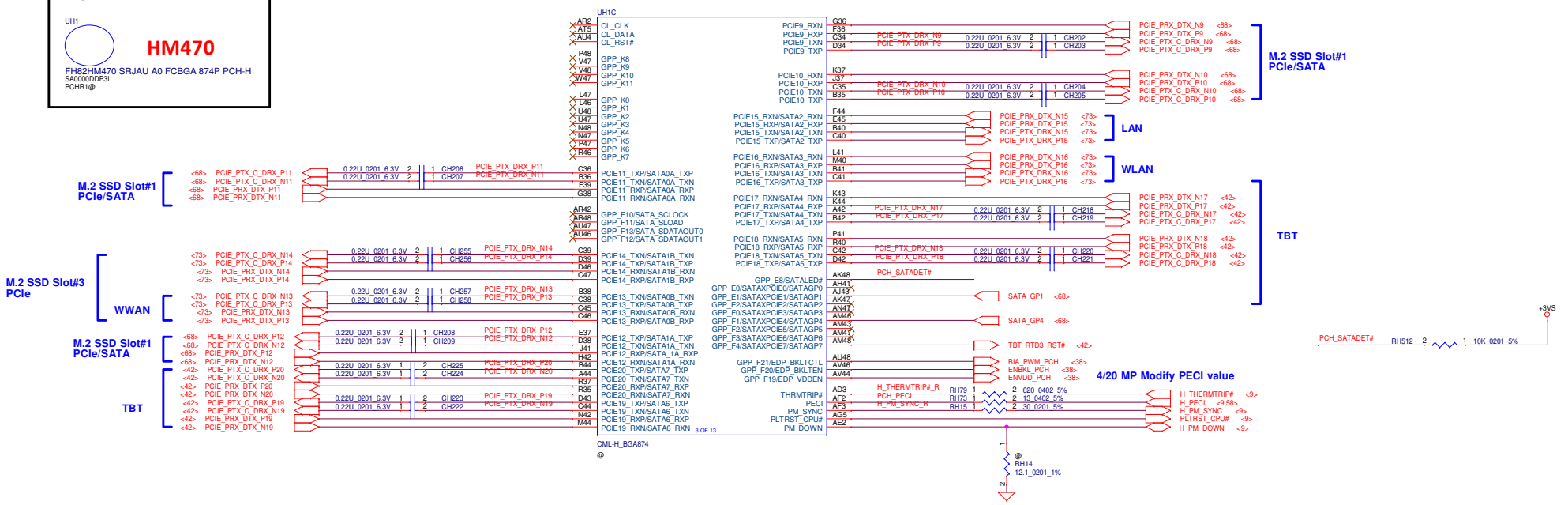
HM470

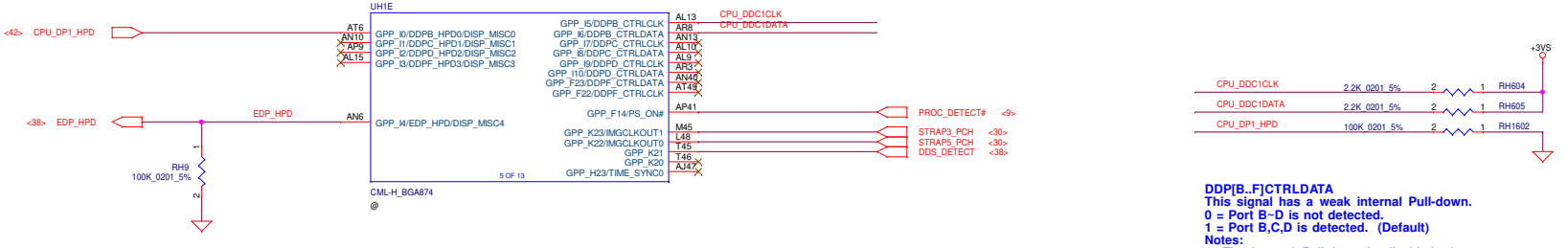
FH82HM470 SRJAU A0 FCBGA PCH-H A31!
SA0000DDP4L
PCH@

UH1

HM470

FH82HM470 SRJAU A0 FCBGA 874P PCH-H
SA0000DDP3L
PCHR1@





20200908, modify power rail to +3V_PCH

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (1/7) SATA,DDC,PCIE**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 14 of 114

Net : XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PEG(dGPU)
SSD2
SSD3/WWAN
Thunderbolt
LAN
WLAN
Caldera
SSD1

#571182_CNL_PCH_H_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
571007_CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

RH1 close to UH4

6/12 check with BIOS

GPP_B3 for enable chA.
GPP_B4 for enable chB.
Active high.

This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to ' 0 if the eSPI or LPC strap is configured to ' 0

RPMC ROM

WSON8/SOIC8 footprint co-lay

20200728, change main to SA0000DL800 (GD), due to Winbond has driving strength issue.

Close RH1606

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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Compal Electronics, Inc.

Title: PCH (2/7) CLK,SPI,PLTRST

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 15 of 114

EC interface

Low(default)	LPC
High	eSPI

This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

4/20 MP Modify WAKE# value

Top Swap Override

0 = Disable ,Top Swap mode. (Default)
1 = Enable, Top Swap mode.
The internal Pull-down is disabled after PCH_PWROK is high.

CLRP1 SHORT PADS **CLRP1 in DIMM door**

10/2 FR update Reserve

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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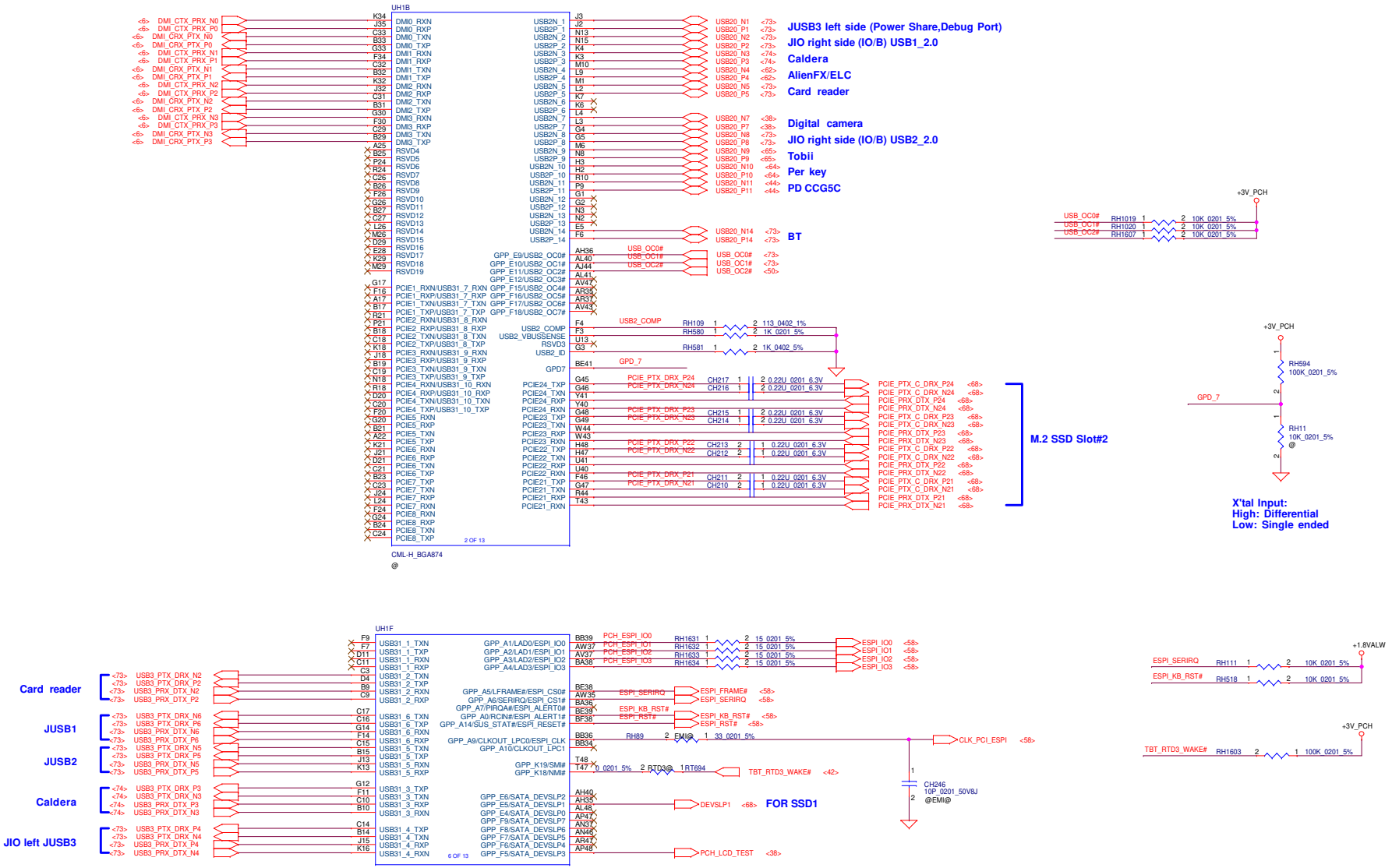
Compal Electronics, Inc.

Title: **PCH (3/7) PM,HDA,SMB,JTAG**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 16 of 114



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 17 of 114

Samsung_8G	S_8G@ RH1024 10K_0201_5%	S_8G@ RH1025 10K_0201_5%	S_8G@ RH1027 10K_0201_5%	S_8G@ RH1029 10K_0201_5%	S_8G@ RH1635 10K_0201_5%
Samsung_16G(ODIE)	S_16G@ RH1024 10K_0201_5%	S_16G@ RH1025 10K_0201_5%	S_16G@ RH1028 10K_0201_5%	S_16G@ RH1029 10K_0201_5%	S_16G@ RH1635 10K_0201_5%
Samsung_16G(NDIE)	S_16G1@ RH1024 10K_0201_5%	S_16G1@ RH1025 10K_0201_5%	S_16G1@ RH1028 10K_0201_5%	S_16G1@ RH1029 10K_0201_5%	S_16G1@ RH1636 10K_0201_5%
Samsung_32G(ODIE)	S_32G@ RH1024 10K_0201_5%	S_32G@ RH1025 10K_0201_5%	S_32G@ RH1027 10K_0201_5%	S_32G@ RH1030 10K_0201_5%	S_32G@ RH1635 10K_0201_5%
Samsung_32G(NDIE)	S_32G1@ RH1024 10K_0201_5%	S_32G1@ RH1025 10K_0201_5%	S_32G1@ RH1027 10K_0201_5%	S_32G1@ RH1030 10K_0201_5%	S_32G1@ RH1636 10K_0201_5%
Hynix_8G	H_8G@ RH1023 10K_0201_5%	H_8G@ RH1025 10K_0201_5%	H_8G@ RH1027 10K_0201_5%	H_8G@ RH1029 10K_0201_5%	H_8G@ RH1635 10K_0201_5%
Hynix_16G(ODIE)	H_16G@ RH1023 10K_0201_5%	H_16G@ RH1025 10K_0201_5%	H_16G@ RH1028 10K_0201_5%	H_16G@ RH1029 10K_0201_5%	H_16G@ RH1635 10K_0201_5%
Hynix_16G(NDIE)	H_16G1@ RH1023 10K_0201_5%	H_16G1@ RH1025 10K_0201_5%	H_16G1@ RH1028 10K_0201_5%	H_16G1@ RH1029 10K_0201_5%	H_16G1@ RH1636 10K_0201_5%
Hynix_32G	H_32G@ RH1023 10K_0201_5%	H_32G@ RH1025 10K_0201_5%	H_32G@ RH1027 10K_0201_5%	H_32G@ RH1030 10K_0201_5%	H_32G@ RH1635 10K_0201_5%
Micron_8G(ODIE)	M_8G@ RH1024 10K_0201_5%	M_8G@ RH1026 10K_0201_5%	M_8G@ RH1027 10K_0201_5%	M_8G@ RH1029 10K_0201_5%	M_8G@ RH1635 10K_0201_5%
Micron_8G(NDIE)	M_8G1@ RH1024 10K_0201_5%	M_8G1@ RH1026 10K_0201_5%	M_8G1@ RH1027 10K_0201_5%	M_8G1@ RH1029 10K_0201_5%	M_8G1@ RH1636 10K_0201_5%
Micron_16G(ODIE)	M_16G@ RH1024 10K_0201_5%	M_16G@ RH1026 10K_0201_5%	M_16G@ RH1028 10K_0201_5%	M_16G@ RH1029 10K_0201_5%	M_16G@ RH1635 10K_0201_5%
Micron_16G(NDIE)	M_16G1@ RH1024 10K_0201_5%	M_16G1@ RH1026 10K_0201_5%	M_16G1@ RH1028 10K_0201_5%	M_16G1@ RH1029 10K_0201_5%	M_16G1@ RH1636 10K_0201_5%
Micron_32G(ODIE)	M_32G@ RH1024 10K_0201_5%	M_32G@ RH1026 10K_0201_5%	M_32G@ RH1027 10K_0201_5%	M_32G@ RH1030 10K_0201_5%	M_32G@ RH1635 10K_0201_5%

N20Y-ES-A1	N20YES@ RH29 10K_0201_5%	N20YES@ RH1608 10K_0201_5%	N20YES@ RH26 10K_0201_5%	N20YES@ RH28 10K_0201_5%
GN20-E7	GN20_E7@ RH29 10K_0201_5%	GN20_E7@ RH1609 10K_0201_5%	GN20_E7@ RH25 10K_0201_5%	GN20_E7@ RH27 10K_0201_5%
GN20-E5	GN20_E5@ RH29 10K_0201_5%	GN20_E5@ RH1609 10K_0201_5%	GN20_E5@ RH25 10K_0201_5%	GN20_E5@ RH28 10K_0201_5%
GN20-E4	GN20_E4@ RH29 10K_0201_5%	GN20_E4@ RH1609 10K_0201_5%	GN20_E4@ RH26 10K_0201_5%	GN20_E4@ RH27 10K_0201_5%
GN20-E3	GN20_E3@ RH29 10K_0201_5%	GN20_E3@ RH1609 10K_0201_5%	GN20_E3@ RH26 10K_0201_5%	GN20_E3@ RH28 10K_0201_5%
N18E-G1-B	N18EG1B@ RH30 10K_0201_5%	N18EG1B@ RH1608 10K_0201_5%	N18EG1B@ RH25 10K_0201_5%	N18EG1B@ RH28 10K_0201_5%
N18E-G3	N18EG3@ RH30 10K_0201_5%	N18EG3@ RH1608 10K_0201_5%	N18EG3@ RH26 10K_0201_5%	N18EG3@ RH27 10K_0201_5%
N18E-G2	N18EG2@ RH30 10K_0201_5%	N18EG2@ RH1608 10K_0201_5%	N18EG2@ RH26 10K_0201_5%	N18EG2@ RH28 10K_0201_5%
N18E-G1	N18EG1@ RH30 10K_0201_5%	N18EG1@ RH1609 10K_0201_5%	N18EG1@ RH25 10K_0201_5%	N18EG1@ RH27 10K_0201_5%
N18E-G0	N18EG0@ RH30 10K_0201_5%	N18EG0@ RH1609 10K_0201_5%	N18EG0@ RH25 10K_0201_5%	N18EG0@ RH28 10K_0201_5%
N18P-G62	N18PG0@ RH30 10K_0201_5%	N18PG0@ RH1609 10K_0201_5%	N18PG0@ RH26 10K_0201_5%	N18PG0@ RH27 10K_0201_5%
Navi 14 XTM	AMD@ 10K_0201_5%	AMD@ 10K_0201_5%	AMD@ RH26 10K_0201_5%	AMD@ RH28 10K_0201_5%

DDR_ID	DDRID_0 (AW13)	DDRID_1 (BE9)	DDRID_2 (BF8)	DDRID_3 (BF9)	DDRID_4 (BG8)	DDRID_5 (BE8)
Micron_32G(O)	L	H	L	H	L	R
Micron_16G(N)	L	H	H	L	H	R
Micron_16G(O)	L	H	H	L	L	R
Micron_8G(N)	L	H	L	L	H	R
Micron_8G(O)	L	H	L	L	L	R
Hynix_32G	H	L	L	H	L	R
Hynix_16G(N)	H	L	H	L	H	R
Hynix_16G(O)	H	L	H	L	L	R
Hynix_8G	H	L	L	L	L	R
Samsung_32G(N)	L	L	L	H	H	R
Samsung_32G(O)	L	L	L	H	L	R
Samsung_16G(N)	L	L	H	L	H	R
Samsung_16G(O)	L	L	H	L	L	R
Samsung_8G	L	L	L	L	L	R

GPU_ID	GSYNC_ID (BF17)	N18_ID2 (BF14)	N18_ID1 (AR18)	N18_ID0 (BF17)
N20Y-ES-A1	H	H	L	L
GN20-E7	H	L	H	H
GN20-E5	H	L	H	L
GN20-E4	H	L	L	H
GN20-E3	H	L	L	L
N/A	L	H	H	H
N18E-G1B	L	H	H	L
N18E-G3	L	H	L	H
N18E-G2	L	H	L	L
N18E-G1	L	L	H	H
N18E-G0	L	L	H	L
N18P-G62	L	L	L	H
Navi 14 XTM	L	L	L	L

+1.8VALW

RH595 2 — 1 10K_0201_5% — CNV_RGI_PTX_DRX

RH168 2 — @ 1 10K_0201_5%

M.2 CNV Mode Select

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

+1.8VALW

RH603 1 — 2 4.7K 0402_5% — CNV_BRI_PTX_DRX

This signal has a weak internal pull-down 20K.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8VALW

RH218 2 — @ 1 10K 0402_5% — GPP_J9

The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a 1 for the proper functionality of the SPI (Flash) I/Os

+1.8VALW

RH181 1 — @ 2 20K 0402_1% — CNV_BRI_PRX_DTX

RH182 1 — @ 2 20K 0402_1% — CNV_RGI_PRX_DTX

571391_CFL_H_PDG_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

For BIOS UART debug

+5VALW

JWDB

UART_2_PTXD_DRXD

UART_2_PRXD_DTXD

ACES_88266-04001 CONN@

UH1K

BBS_BIT0 — EC_SCI# — NRB_BIT — WL_OFF# — BT_OFF# — UART_2_PTXD_DRXD — UART_2_PRXD_DTXD — I2C_1_SCL — I2C_1_SDA — I2C_0_SCL — I2C_0_SDA — TP_INT#

GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS0#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS0#
GPP_C9/UART0A_TXD
GPP_C8/UART0A_RXD
GPP_C11/UART0A_CTS#
GPP_C10/UART0A_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
GPP_D23/ISH_I2C2_SCL/I2C3_SCL
11 OF 13
CML-H_BGA874

20200716, add GC6_FB_EN_MCP to leverage Viper BIOS

GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
GPP_D10/ISH_SPI_CLK/GSPI2_CLK
GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO
GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI
GPP_D16/ISH_UART0_CTS#/CNV_WCEN
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
GPP_D14/ISH_UART0_TXD/I2C2_SCL
GPP_D13/ISH_UART0_RXD/I2C2_SDA
GPP_H20/ISH_I2C0_SCL1
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

BOARD_ID — PEX_RST# — DGPU_PWR_EN — DGPU_ID2 — DGPU_ID1 — DGPU_ID0 — GSYNC_ID

To G+Gyro sensor

ISH_I2C0_SCL — ISH_I2C0_SDA

PCH_ACC1_INT1 — PCH_GYRO_INT2 — ISH_GP1

UH1M

SD_READ_MODE — SD_WP# — RTC_DET# — RTD3_USB_PWR_EN

GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_I11/M2_SKT2_CFG0
GPP_I12/M2_SKT2_CFG1
GPP_I13/M2_SKT2_CFG2
GPP_I14/M2_SKT2_CFG3
GPP_J0/CNV_PA_BLANKING
GPP_J1/CPU_C10_GATE#
GPP_J11/A4WP_PRESENT
GPP_J10
GPP_J2
GPP_J3
GPP_J4/CNV_BRI_DT/UART0B_RTS#
GPP_J5/CNV_BRI_RSP/UART0B_RXD
GPP_J6/CNV_RGI_DT/UART0B_TXD
GPP_J7/CNV_RGI_RSP/UART0B_CTS#
GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WR_D0N
CNV_WR_D0P
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_D0N
CNV_WT_D0P
CNV_WT_D1N
CNV_WT_D1P
CNV_WT_RCOMP
PCIE_RCOMPN
PCIE_RCOMPP
SD_1P8_RCOMP
SD_3P3_RCOMP
GPPJ_RCOMP_1P81
GPPJ_RCOMP_1P82
GPPJ_RCOMP_1P83
RSVD28
RSVD29
RSVD30
TP
13 OF 13
CML-H_BGA874

CNV_BRI_PTX_DRX — CNV_BRI_PRX_DTX — CNV_RGI_PRX_DTX — GPP_J9

RH213 1 — 2 150 0201 1%

RH193 1 — 2 100 0402 1%

RH214 1 — 2 200 0402 1%

RH215 1 — 2 200 0402 1%

GPPJ_RCOMP_1P8

RH216 1 — 2 200 0201 1%

T135 PAD~D @

DDRID STRAP

DDRID_0 — DDRID_1 — DDRID_2 — DDRID_3 — DDRID_4 — DDRID_5

RH1023 10K_0201_5% — RH1026 10K_0201_5% — RH1028 10K_0201_5% — RH1030 10K_0201_5% — RH1636 10K_0201_5% — RH1638 10K_0201_5%

RH1024 10K_0201_5% — RH1025 10K_0201_5% — RH1027 10K_0201_5% — RH1029 10K_0201_5% — RH1635 10K_0201_5% — RH1637 10K_0201_5%

Vendor	DDRID_0	DDRID_1
Samsung	L	L
Hynix	H	L
Micron	L	H

Vendor	DDRID_2	DDRID_3
8G	L	L
16G	H	L
32G	L	H

Vendor	DDRID_4	DDRID_5
8G	L(1st die) H(2nd die)	RSVD
16G		RSVD
32G		RSVD

+3VS

RH517 1 — @ 2 8.2K 0201_5% — BT_OFF#
RH520 1 — @ 2 8.2K 0201_5% — WL_OFF#
RH521 1 — 2 10K 0201_5% — EC_SCI#
RC62 2 — 1 49.9K 0201_1% — UART_2_PRXD_DTXD
RC63 2 — 1 49.9K 0201_1% — UART_2_PTXD_DRXD
RH1626 1 — @ 2 10K 0201_5% — SD_WP#

+3V_PCH

RH1608 10K_0201_5% — RH25 10K_0201_5% — RH27 10K_0201_5% — RH29 10K_0201_5%

DGPU_ID2
DGPU_ID1
DGPU_ID0
GSYNC_ID

RH1609 10K_0201_5% — RH26 10K_0201_5% — RH28 10K_0201_5% — RH30 10K_0201_5%

+3VS

DGPU_PWR_EN — RH537 1 — 2 10K_0201_5%
GC6_FB_EN_MCP — RH1643 1 — 2 10K_0201_5%

20200716, Pull up at PCH side to leverage Viper BIOS

+3V_PCH

BOARD_ID — RH21 1 — NV@ 2 10K_0201_5%

BOARD_ID — RH1601 1 — @ 2 10K_0201_5%

+3VS

I2C_0_SDA — RH1617 1 — 2 10K_0201_5%
I2C_0_SCL — RH1618 1 — 2 10K_0201_5%

+3V_PCH

BBS_BIT0 — RH130 2 — @ 1 1K 0402_5%

Boot BIOS Strap Bit (internal PD)

HIGH	LPC
LOW(DEFAULT)	SPI

+3V_PCH

NRB_BIT — RH524 2 — @ 1 1K 0201_5%

NO REBOOT mode (internal PD)

HIGH	Enable
LOW(DEFAULT)	Disable

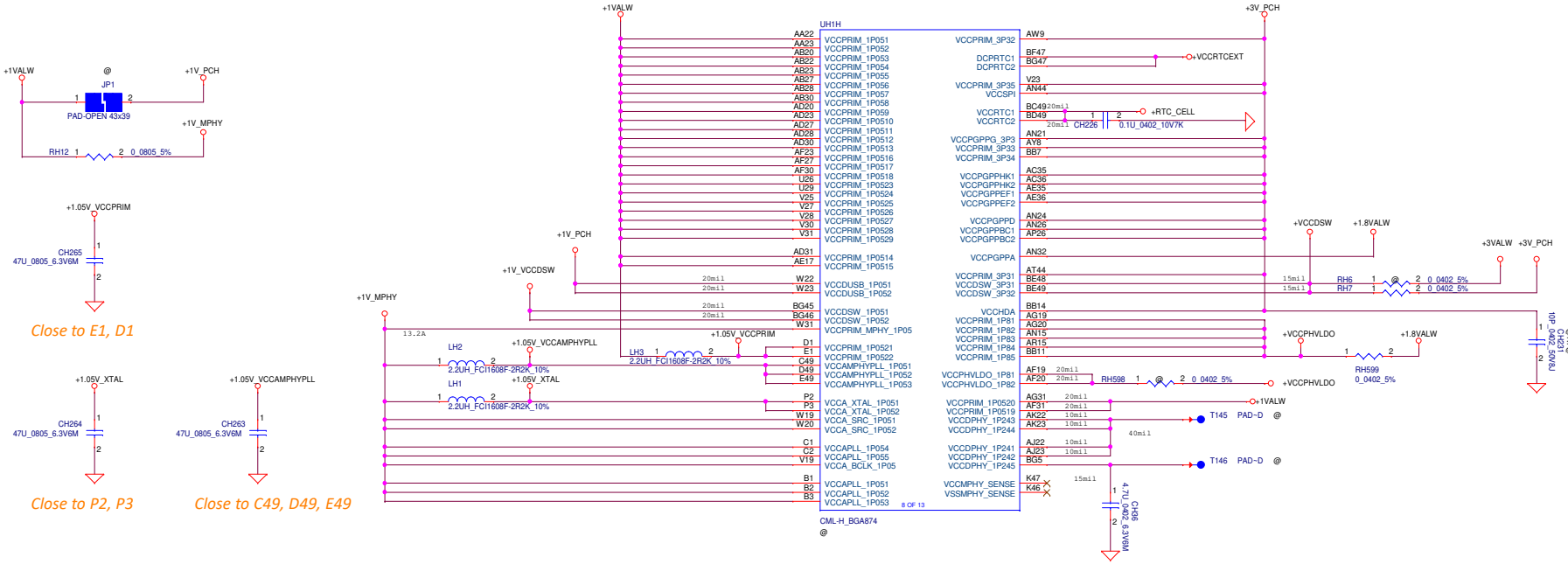
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

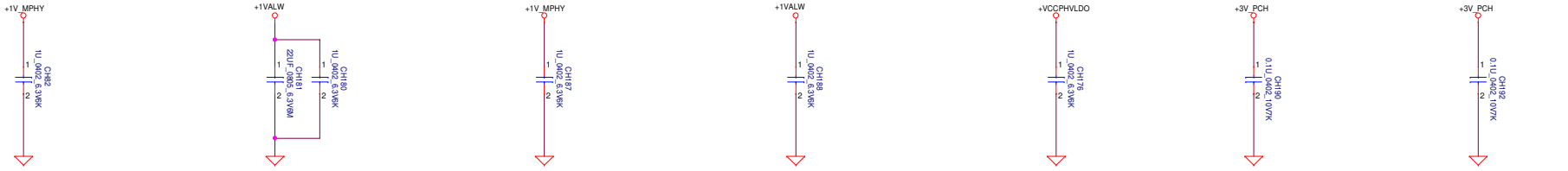
Compal Electronics, Inc.

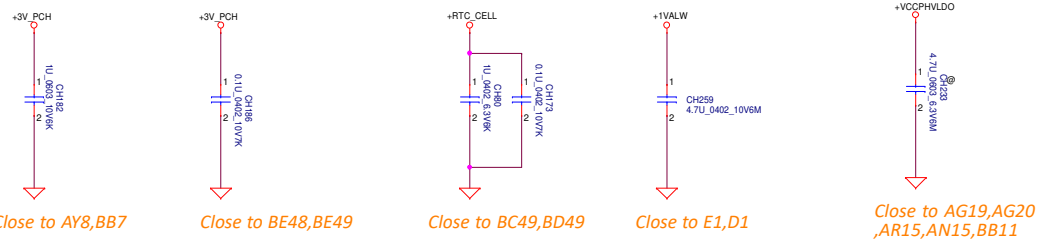
Title: PCH (5/7) I2C,GPIO

Size: — Document Number: LA-K741P — Rev: 1.0

Date: Thursday, December 03, 2020 — Sheet 18 of 114







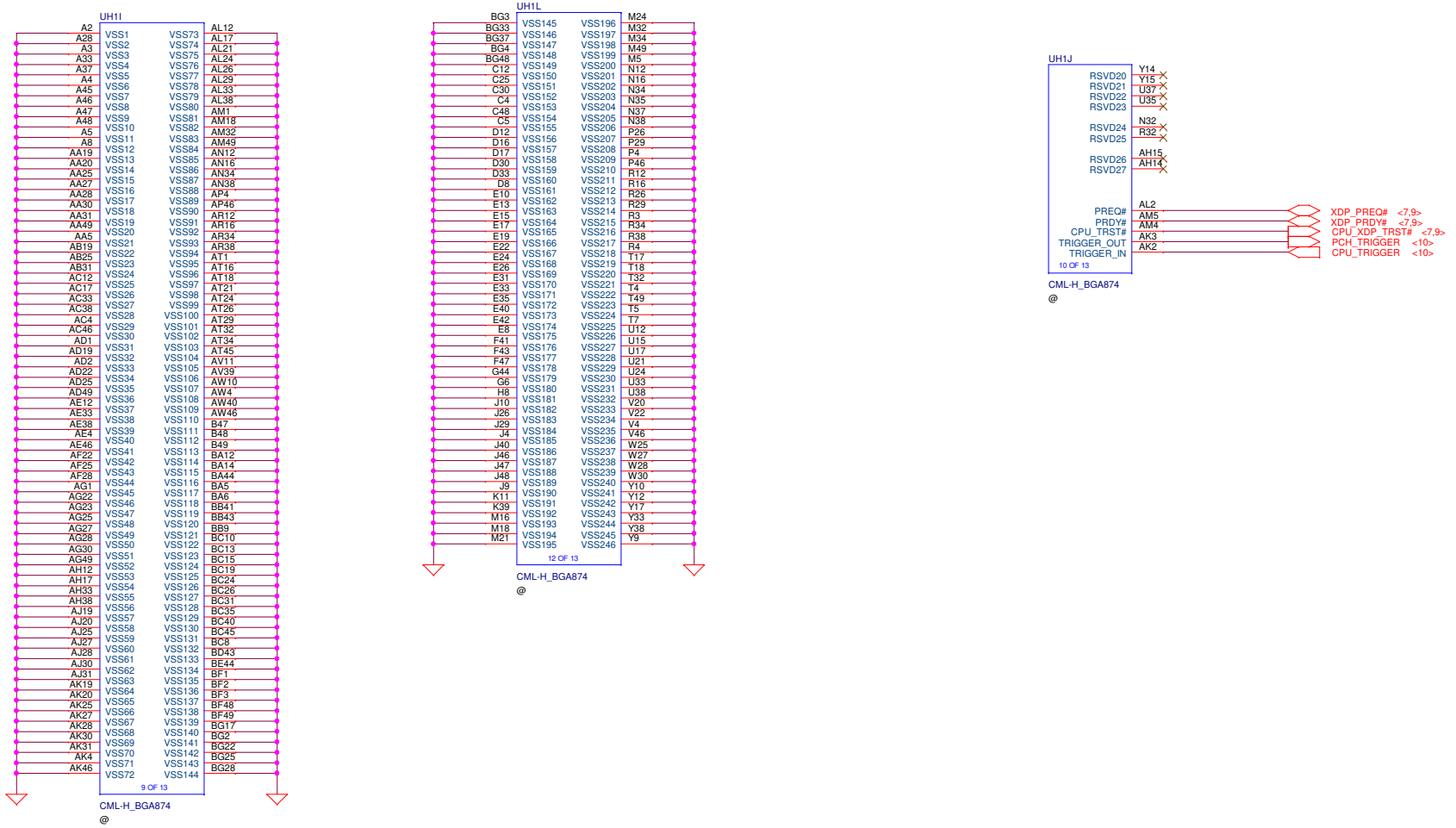
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **PCH (6/7) PWR**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 19 of 114



Compal Electronics, Inc.

Title: **PCH (7/7) VSS**

Size	Document Number	Rev
	LA-K741P	1.0

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DRAM X76:

ZZ22 X76DS16@
ALT. GROUP PARTS 16G SAMSUNG 2933 GDR51
X76852311B0

ZZ23 X76DM16@
ALT. GROUP PARTS 16G MICRON 2933 GDR51
X76852311B1

ZZ24 X76DH16@
ALT. GROUP PARTS 16G HYNIX 2933 GDR51
X76852311B2

ZZ25 X76DS32@
ALT. GROUP PARTS 32G SAMSUNG 2933 GDR51
X76852311B3

ZZ13 X76DM32@
ALT. GROUP PARTS 32G MICRON 2933 GDR51
X76852311B8

ZZ14 X76DH32@
ALT. GROUP PARTS 32G HYNIX 2933 GDR51
X76852311B2

ZZ15 X76DM16R3@
ALT. GROUP PARTS DRAM 16G MIC R3 GDR51
X76852311BJ

16G bit (2G Byte) 3200Mhz

Micron		Hynix		Samsung	
R1 SA0000D3U0L	R3 SA0000D3U1L	R1 SA0000CZ13L	R3 SA0000CZ14L	R1 SA0000CZ20L	R3 SA0000CZ21L
UD1 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD1 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD1 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD1 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD1 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD1 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD5 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD5 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD5 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD5 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD5 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD5 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD2 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD2 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD2 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD2 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD2 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD2 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD6 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD6 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD6 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD6 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD6 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD6 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD3 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD3 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD3 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD3 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD3 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD3 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD7 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD7 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD7 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD7 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD7 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD7 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD4 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD4 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD4 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD4 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD4 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD4 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L
UD8 DM16GR1@ MT40A1G16KD-062E:E SA0000D3U0L	UD8 DM16GR3@ MT40A1G16KD-062E:E SA0000D3U1L	UD8 DH16GR1@ H5ANAG6NCMR-XNC SA0000CZ13L	UD8 DH16GR3@ H5ANAG6NCMR-XNC SA0000CZ14L	UD8 DS16GR1@ K4AAG165WA-BCWE SA0000CZ20L	UD8 DS16GR3@ K4AAG165WA-BCWE SA0000CZ21L

32G bit (4G Byte) 3200Mhz

Samsung		Micron		Hynix	
R1 SA0000DAS0L	R3 SA0000DAS1L	R1 SA0000CYF0L	R3 SA0000CYF1L	R1 SA0000DAU0L	R3 SA0000DAU1L
UD1 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD1 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD1 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD1 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD1 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD1 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD5 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD5 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD5 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD5 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD5 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD5 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD2 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD2 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD2 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD2 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD2 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD2 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD6 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD6 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD6 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD6 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD6 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD6 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD3 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD3 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD3 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD3 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD3 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD3 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD7 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD7 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD7 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD7 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD7 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD7 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD4 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD4 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD4 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD4 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD4 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD4 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L
UD8 DS32GR1@ K4ABG165WA-MCWE SA0000DAS0L	UD8 DS32GR3@ K4ABG165WA-MCWE SA0000DAS1L	UD8 DM32GR1@ MT40A2G16SKL-062E:B SA0000CYF0L	UD8 DM32GR3@ MT40A2G16SKL-062E:B SA0000CYF1L	UD8 DH32GR1@ H5ANBG6NAMR-XNC SA0000DAU0L	UD8 DH32GR3@ H5ANBG6NAMR-XNC SA0000DAU1L

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			Size: Document Number: LA-K741P Rev: 1.0
			Date: Thursday, December 03, 2020 Sheet 21 of 114

VRAM X76:

ZZ26 X76S6G@
ALT_GROUP PARTS 6GB SAM CRMV1 GDR51
X7685231LB4

ZZ27 X76S8G@
ALT_GROUP PARTS 8GB SAM CRMV1 GDR51
X7685231LB5

ZZ28 X76M6G@
ALT_GROUP PARTS 6GB MICRON 0H98D GDR51
X7685231LB6

ZZ29 X76M8G@
ALT_GROUP PARTS 8GB MICRON 0H98D GDR51
X7685231LB7

ZZ210 X76H6G@
ALT_GROUP PARTS 6GB HYNIX 4T0DJ GDR51
X7685231LB8

ZZ211 X76H8G@
ALT_GROUP PARTS 8GB HYNIX 4T0DJ GDR51
X7685231LB9

ZZ212 X76S16G@
ALT_GROUP PARTS 8GB SAM DVFT2 GDR51
X7685231LBA

8G bit GDDR6(GN20-E3)

Micron 6G Byte

R1 SA0000BND6L

UG11 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UG15 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UG12 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UG16 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UG13 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UG14 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L

R3 SA0000BND7L

UG11 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UG15 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UG12 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UG16 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UG13 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UG14 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L

Samsung 6G Byte

R1 SA0000C625L

UG11 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L
UG15 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L
UG12 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L
UG16 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L
UG13 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L
UG14 VS6GR1@ K4ZB0325BC-HC14 SA0000C625L

R3 SA0000C626L

UG11 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L
UG15 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L
UG12 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L
UG16 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L
UG13 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L
UG14 VS6GR3@ K4ZB0325BC-HC14 SA0000C626L

Hynix 6G Byte

R1 SA0000DUW0L

UG11 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG15 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG12 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG16 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG13 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG14 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L

R3 SA0000DUW1L

UG11 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG15 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG12 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG16 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG13 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG14 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L

8G bit GDDR6 GN20-E4/E5/E7(120W)

Micron 8G Byte

R1 SA0000BND6L

UG11 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG15 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG12 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG16 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG13 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG17 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG14 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UG18 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L

R3 SA0000BND7L

UG11 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG15 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG12 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG16 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG13 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG17 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG14 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UG18 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L

Samsung 8G Byte

R1 SA0000C625L

UG11 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG15 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG12 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG16 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG13 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG17 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG14 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L
UG18 VS8GR1@ K4ZB0325BC-HC14 SA0000C625L

R3 SA0000C626L

UG11 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG15 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG12 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG16 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG13 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG17 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG14 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L
UG18 VS8GR3@ K4ZB0325BC-HC14 SA0000C626L

Hynix 8G Byte

R1 SA0000DUW0L

UG11 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG15 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG12 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG16 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG13 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG17 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG14 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UG18 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L

R3 SA0000DUW1L

UG11 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG15 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG12 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG16 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG13 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG17 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG14 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UG18 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L

16G bit GDDR6 GN20-E7(150W)

Samsung 16G Byte

R1 SA0000CBG0L

UG11 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG15 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG12 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG16 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG13 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG17 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG14 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UG18 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L

R3 SA0000CBG2L

UG11 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG15 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG12 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG16 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG13 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG17 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG14 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UG18 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L

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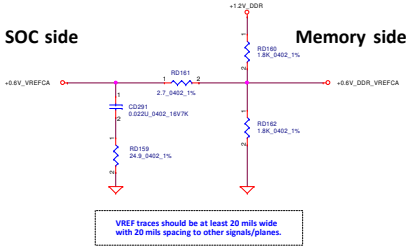
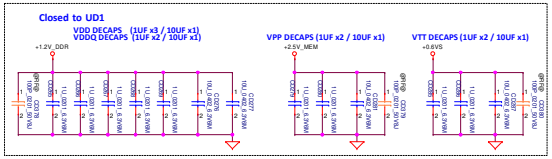
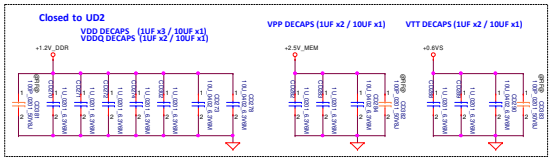
DDR4 Memory Down_CHA

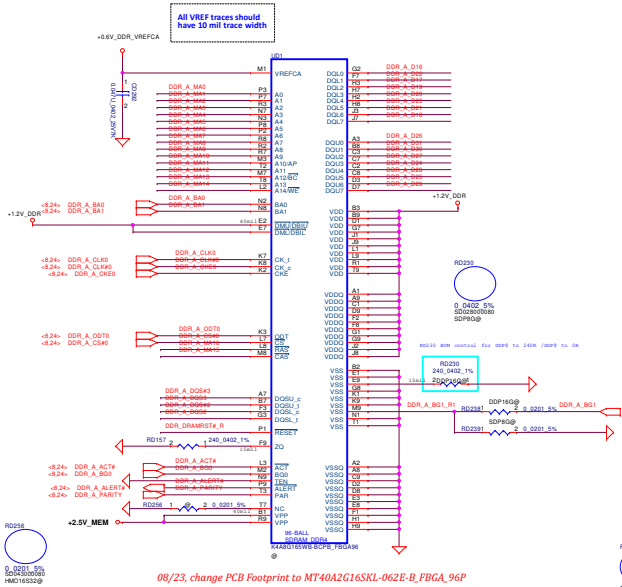
Non-Interleave Memory

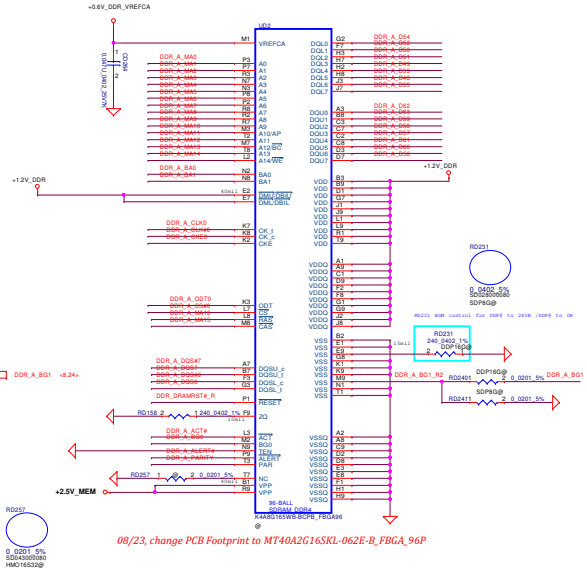
DDR4 Memory Down_CHA

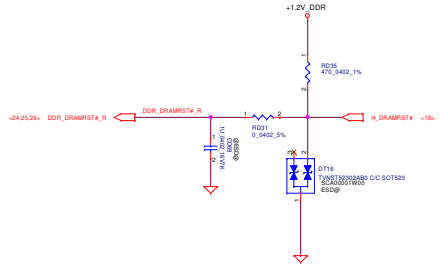


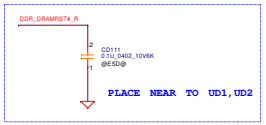












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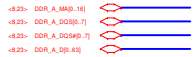
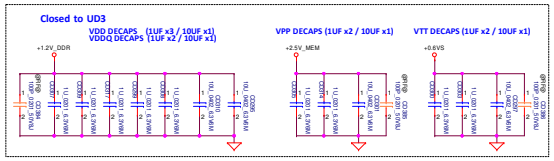
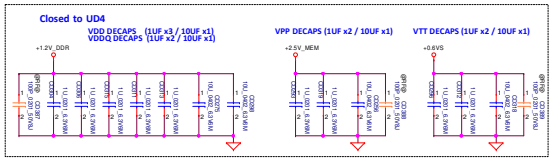
			Date: Thursday, December 03, 2020; Sheet 23 of 114

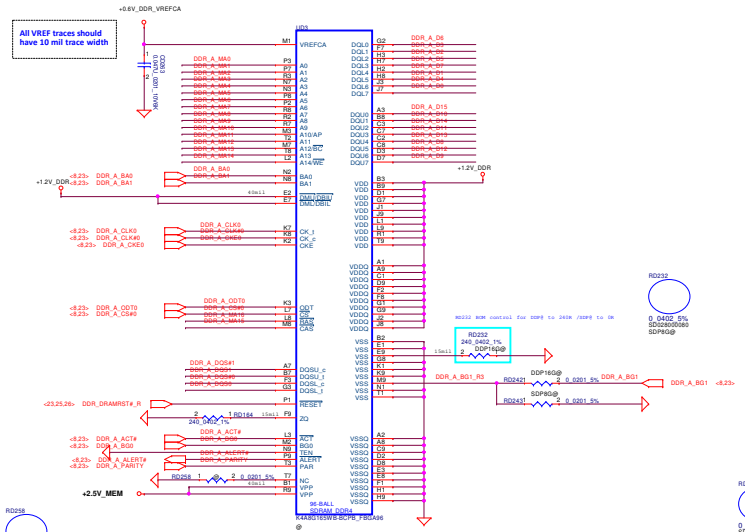
DDR4 Memory Down_CHA

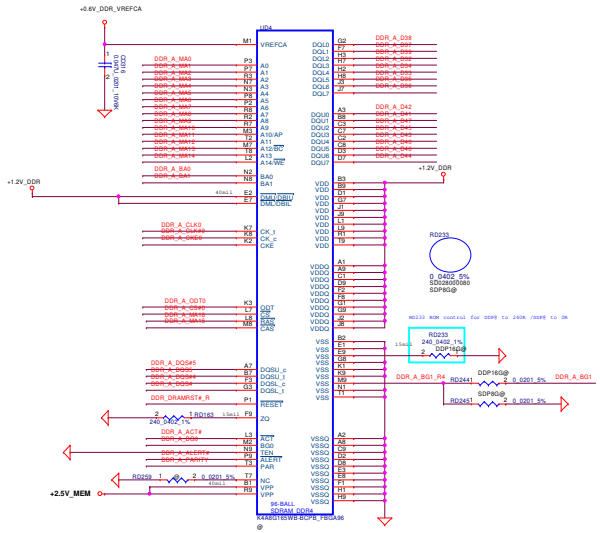
Non-Interleave Memory

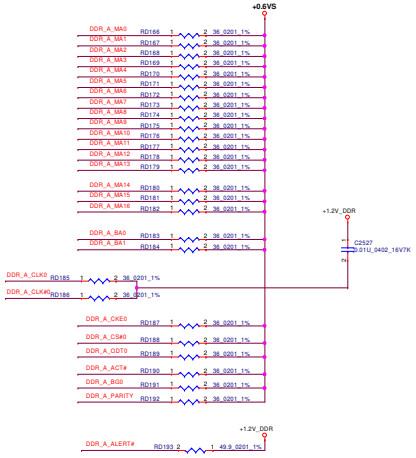












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Issued Date	2017/04/07	Deciphered Date	2018/12/31

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Title: DDR4 Memory Down_CHA			
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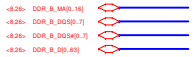
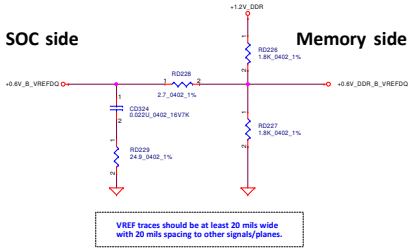
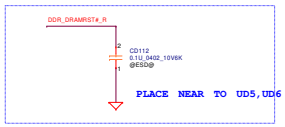
DDR4 Memory Down_CHB

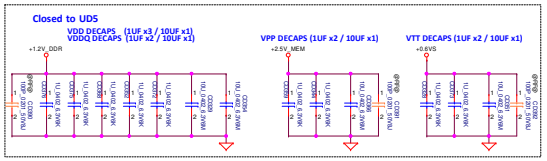
Non-Interleave Memory

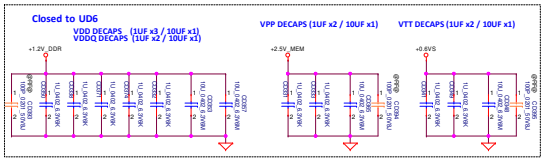


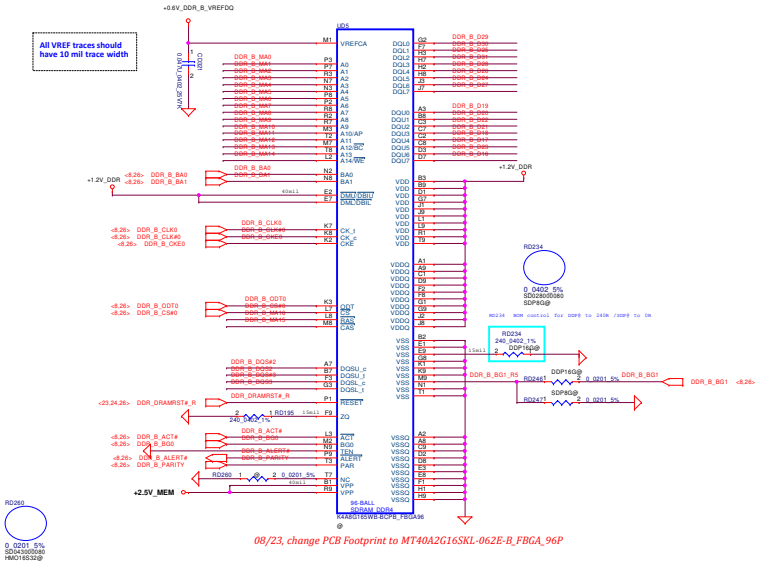
DDR4 Memory Down_CHB

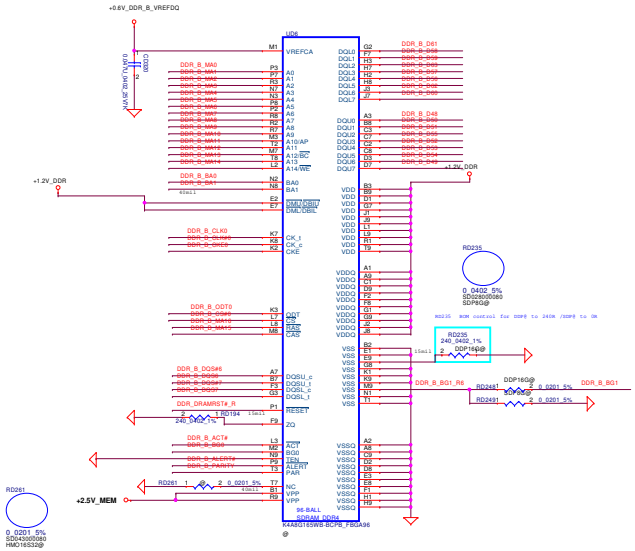












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Issued Date	2017/04/07	Deciphered Date	2018/12/31
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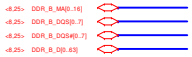
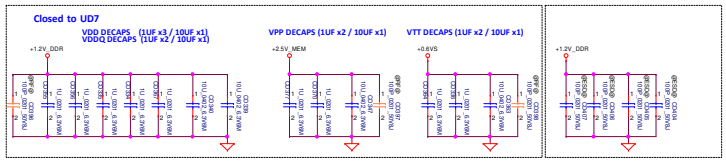
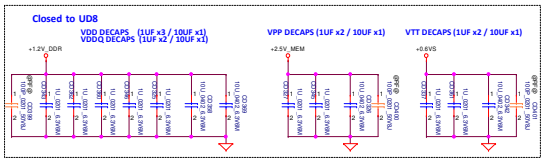
			Size: D — Document Number: LA-K741P — Rev: 1.0
			Date: Thursday, December 03, 2020 — Sheet 25 of 114

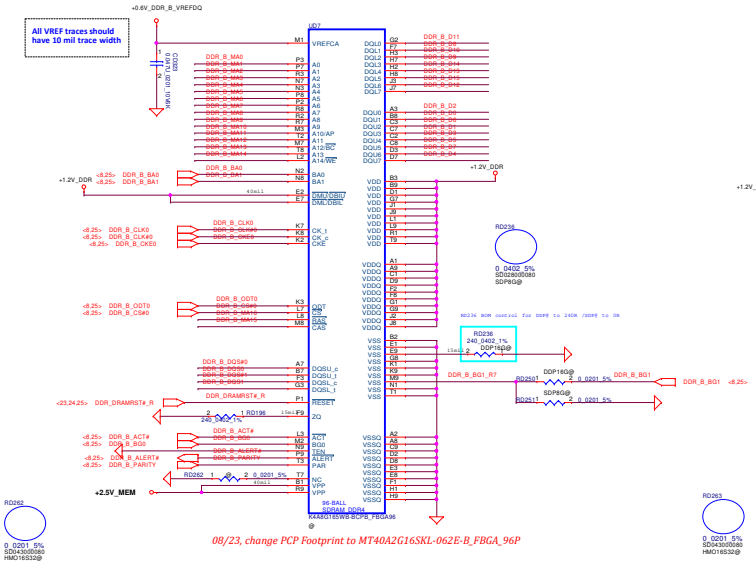
DDR4 Memory Down_CHB

Non-Interleave Memory

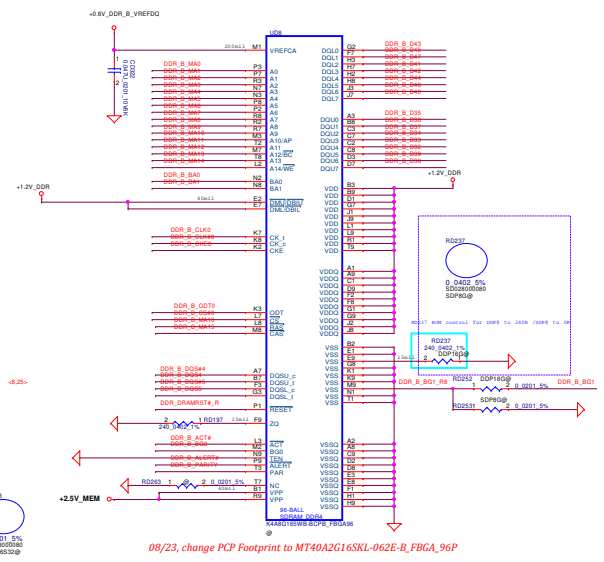








08/23, change PCP Footprint to MT40A2G16SKL-062E-B_FBGA_96P



08/23, change PCP Footprint to MT40A2G16SKL-062E-B_FBGA_96P

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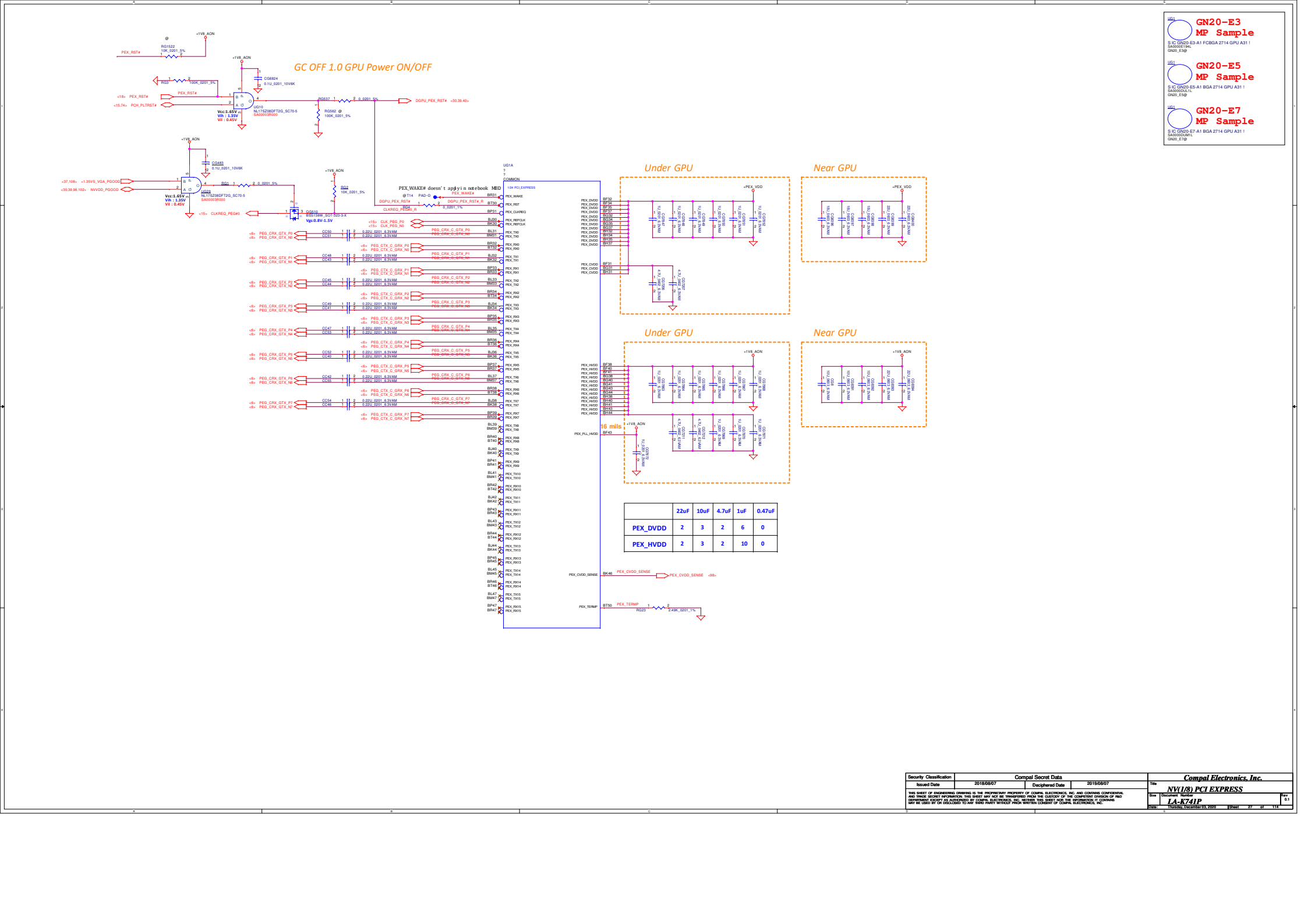
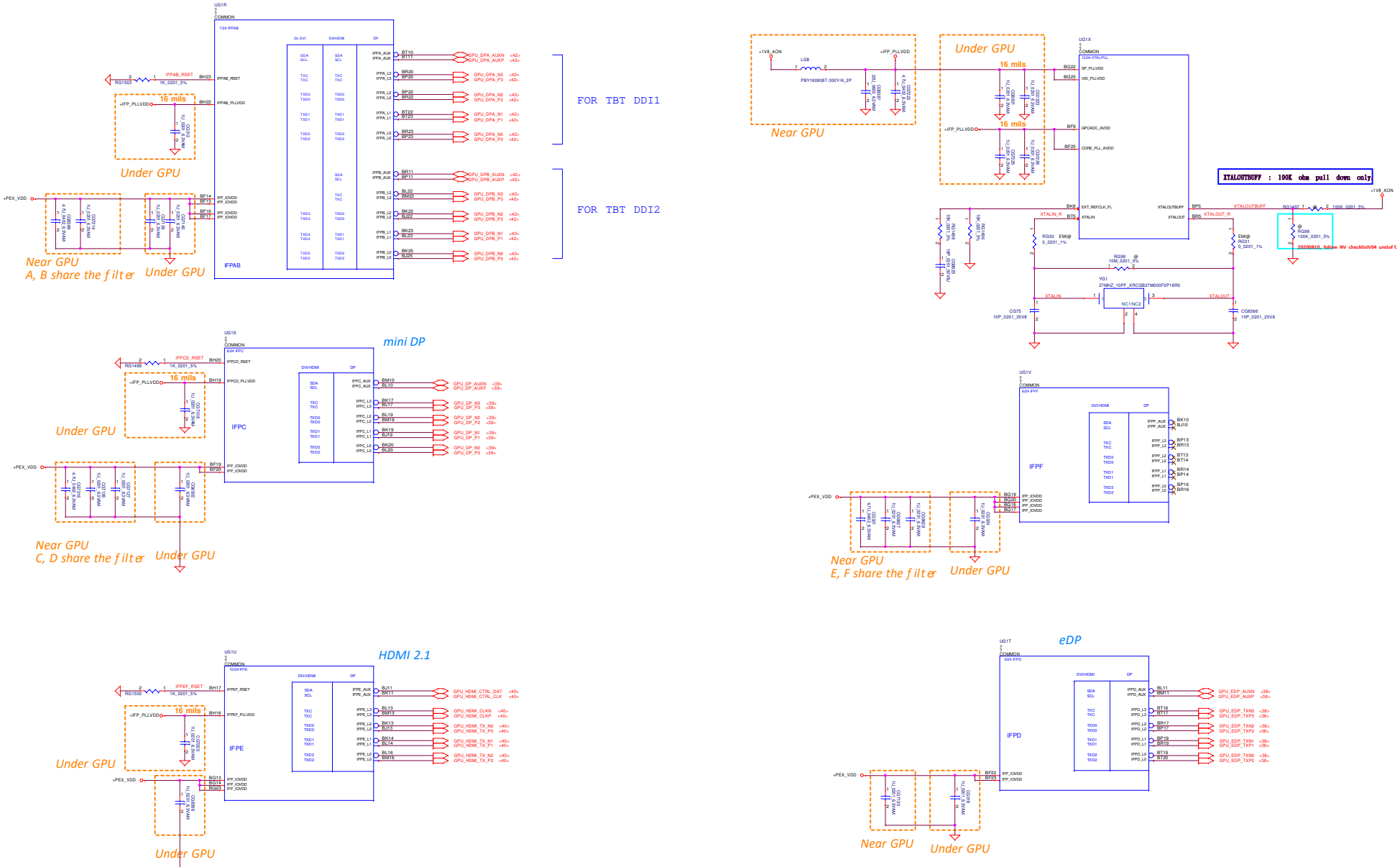
			Date: Thursday, December 03, 2020; Sheet 26 of 114



	22uF	10uF	4.7uF	1uF	0.47uF
PEX_DVDD	2	3	2	6	0
PEX_HVDD	2	3	2	10	0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date 2019/08/07	Title: NV(1/8) PCI EXPRESS
			Size: Document Number: LA-K741P Rev: 0.1
			Date: Thursday, December 03, 2020 Sheet 27 of 114

6/15 Modify



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

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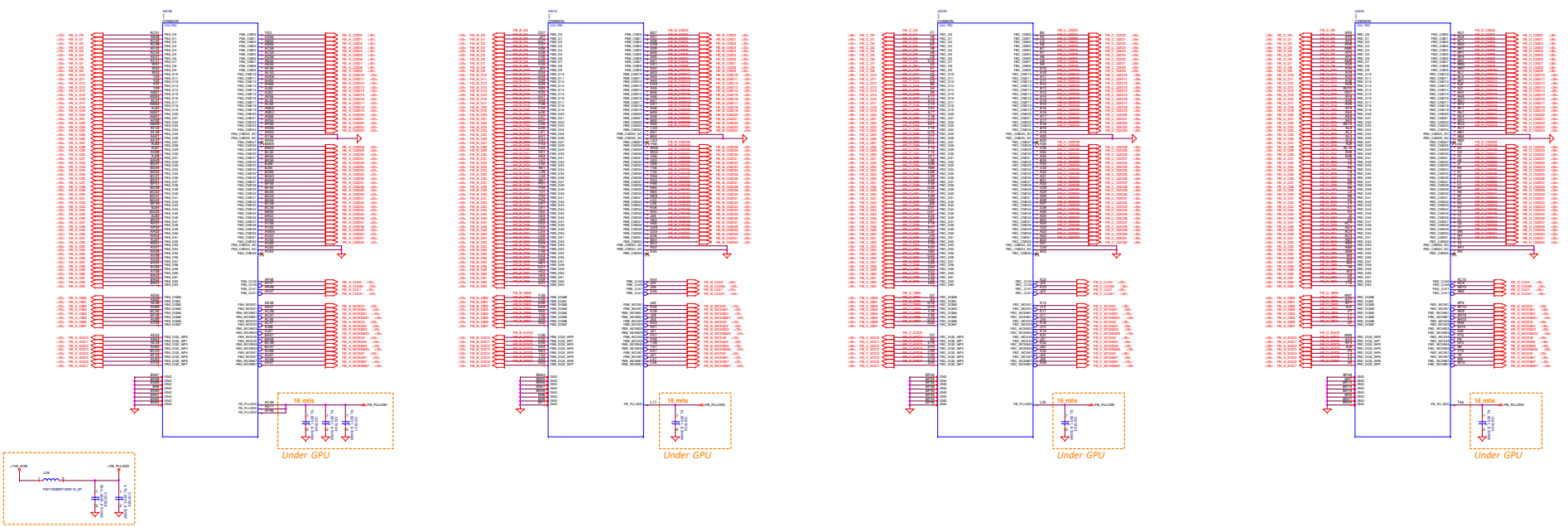
Compal Electronics, Inc.

Title: NV(2/8) IFP ABCDEF

Size: Document Number: LA-K741P Rev: 0.1

Date: Thursday, December 03, 2020 Sheet 28 of 114

6/15 Modify



Security Classification	Compal Secret Data		Compal Electronics, Inc.
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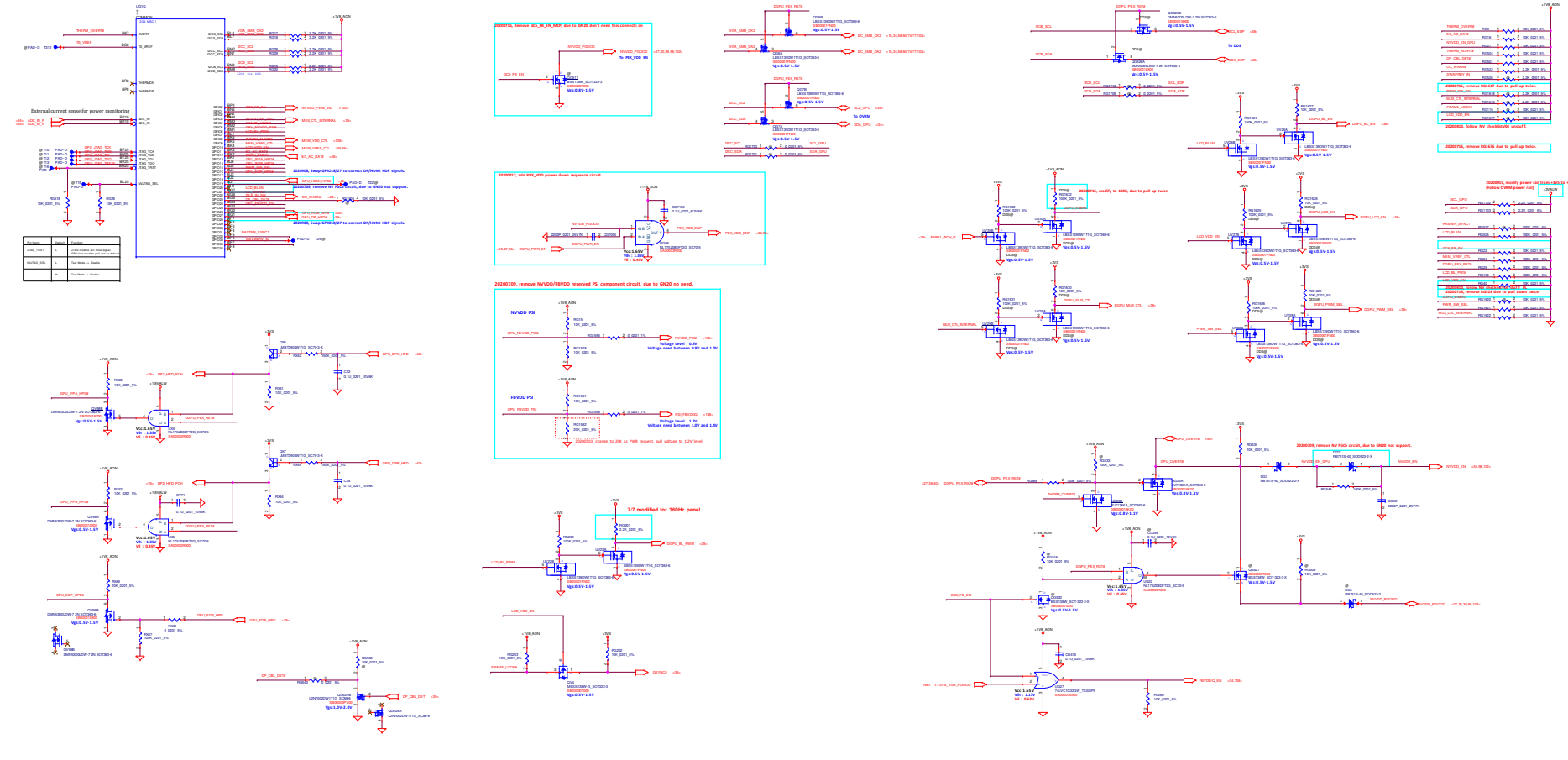
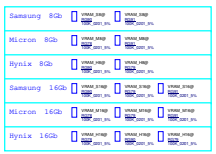
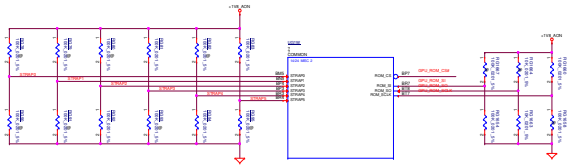
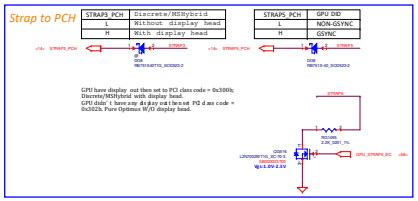
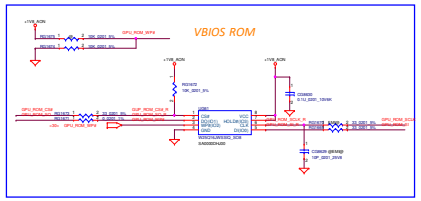
Size: Custom	Document Number: LA-K741P		Rev: 0.3
Date: Monday, May 16, 2016	Sheet: 38 of 53		











9.2.2.3 Failsafe Over-Temperature Protection Strap

The FS_OVERT* strap is configured with the ROM_SO, ROM_SI, and ROM_CLK signal levels.

The FS_OVERT* strap enables the Failsafe_OVERT* function, which extends the over-temperature protection provided by the normal OVERT* input and external temperature monitoring hardware. The Failsafe_OVERT* function monitors a temperature sensor inside the GPU. If it detects an over-temperature condition but the external circuitry has not asserted the OVERT* bidirectional open-drain signal, it proactively asserts that open-drain OVERT* signal, to disable the NVVDD power supply. The Failsafe_OVERT* function maintains assertion of the OVERT* bidirect even after the main power partitions of the GPU have powered down. The Failsafe_OVERT* function is reset when a PCIe reset is received by the GPU (after re-ramp-up of NVVDD).

The FS_OVERT* strap should be configured to ENABLE the Failsafe_OVERT* function. See the L-L-H row of Table 9.4.

Table 9.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function DISABLED
L	L	H	FS_OVERT* function ENABLED (default)
all other configurations			(Invalid; do not configure)

Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by Tie-Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

▶ DEVID_SEL: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').

Table 9.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	M	L	14 (0x000E)
M	M	H	15 (0x000F)

Table 9.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H	L	M	14 (0x001E)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	L	25 (0x0019)
M	H	M	26 (0x001A)

Table 1. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
16 Gb	2Chx512Mx16	1.35V	Samsung	KAZAF335BM-HC14	M-die	0x5	14 Gbps	2001	Full	Production candidate
		1.25V	Micron	TBD	TBD	N/A	14 Gbps	N/A	Full	Production candidate
		1.2V	Hynix	TBD	TBD	0x0	14 Gbps	N/A	Full	Production candidate
8 Gb	2Chx256Mx16	1.35V	Samsung	KAZB0325BC-HC14	C-die	0x0	14 Gbps	1901	Full	Production candidate
		1.25V	Hynix	H54G28H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[1]	Full	Production candidate

Notes:
1. Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
2. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
3. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E7, the maximum allowable memory case temperature is 95 °C.

Table 2. GN20-E5/E4 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V	Samsung	KAZB0325BC-HC14	C-die	0x0	14 Gbps	1901	Full	Production candidate
		1.25V	Hynix	H54G28H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V[1]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[2]	Full	Production candidate

Notes:
1. Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
2. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
3. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E5/E4, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.35V	Samsung	KAZB0325BC-HC14	C-die	0x0	14 Gbps	1901	Full	Production candidate
		1.25V	Hynix	H54G28H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
		1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[1]	Full	Production candidate

Notes:
1. Refer to GN20-E GeForce Product Spec for memory voltages and clocks.
2. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
3. Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-E3, the maximum allowable memory case temperature is 95 °C.

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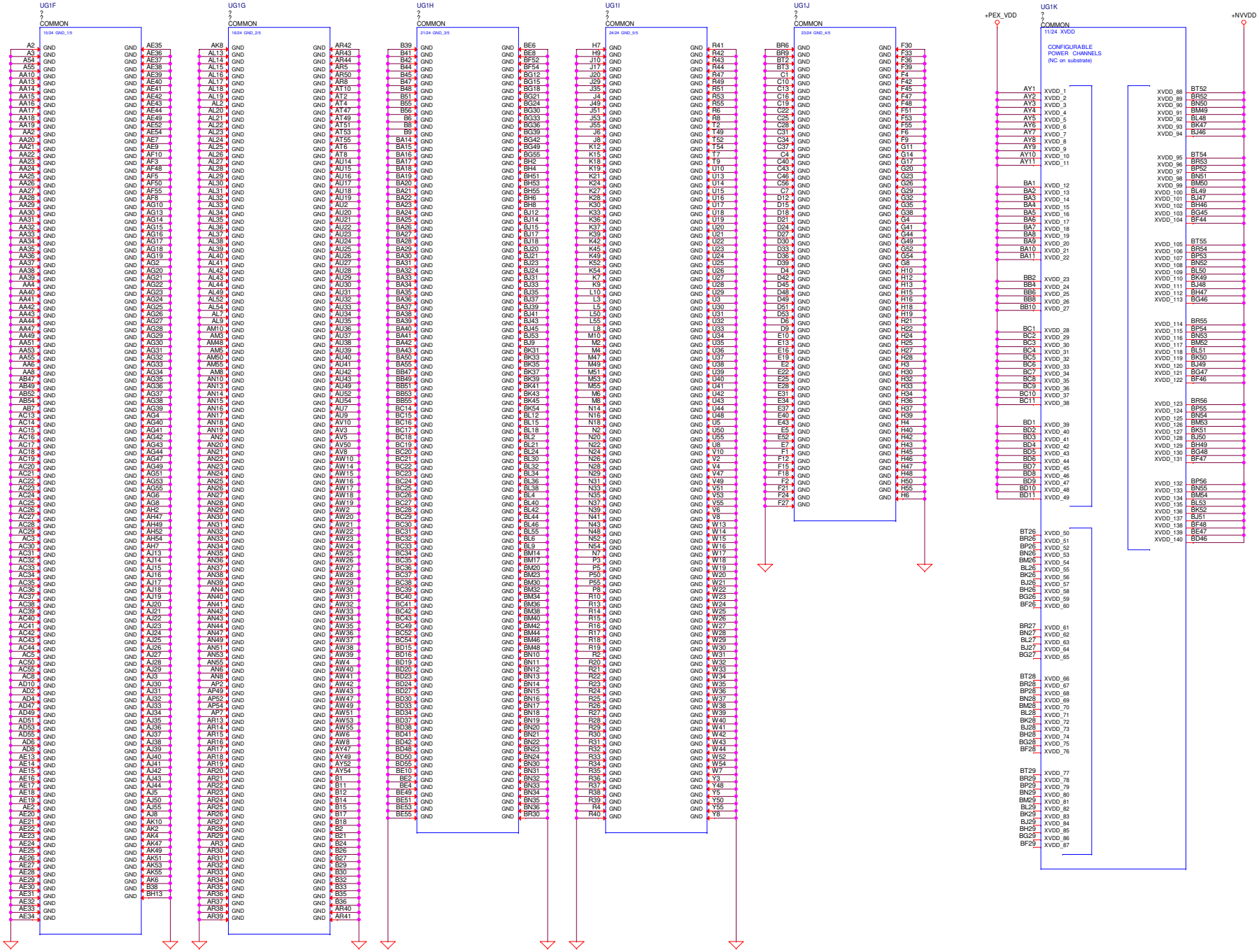
Title: NV44(8) GPIO
Size: A3 | Document Number: LA-K741P | Rev: 0.1
Date: Monday, May 04, 2020 | Sheet 36 of 109



Security Classification	Compal Secret Data		
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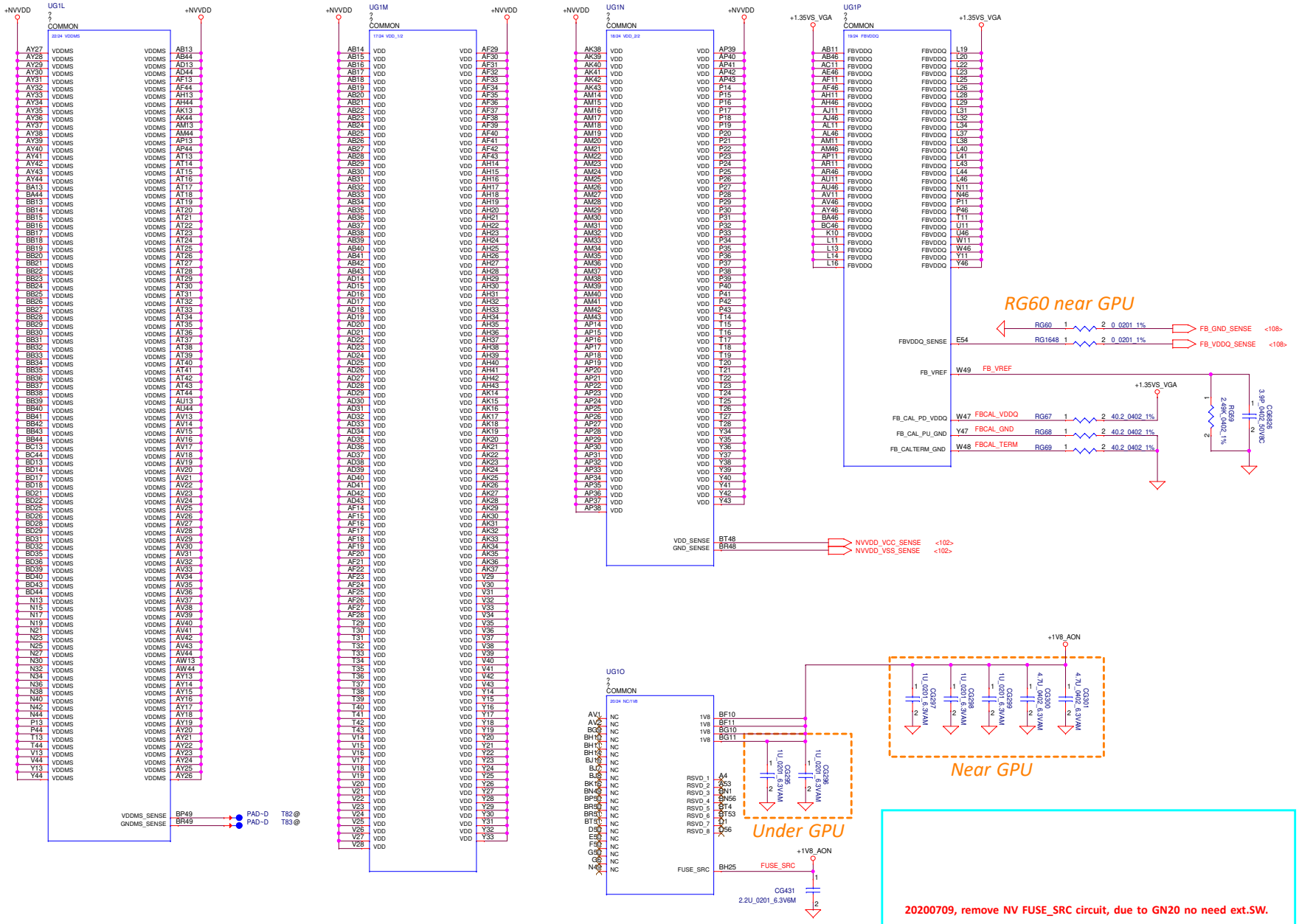
Compal Electronics, Inc.

Title: **NV(6/8) GND, RFUs**

Size	Document Number	Rev
	LA-K741P	0.1

Date: Thursday, December 03, 2020 | Sheet 31 of 114



Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: NV(7/8) POWERS

Size	Document Number	Rev
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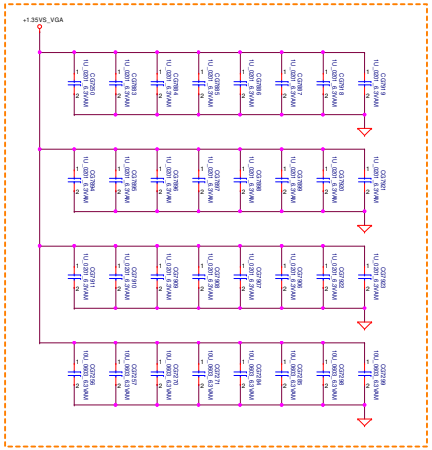
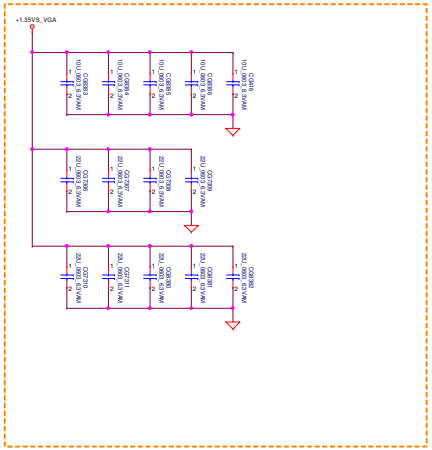
Date: Thursday, December 03, 2020 | Sheet 32 of 114

FBVDDQ_GPU

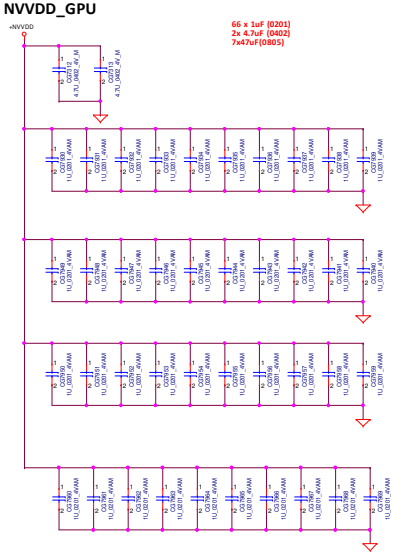
Under GPU



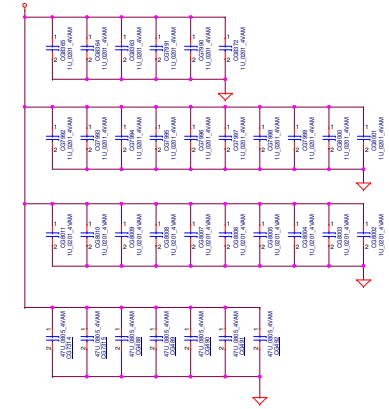
Near GPU



NVVDD_GPU



NVVDD_GPU



20200709, remove NV FGC6 circuit, due to GN20 not support.

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			Size: Document Number: LA-K741P Rev: 0.1
			Date: Thursday, December 03, 2020 Sheet 33 of 114

UG37
NCP45492XMNTWG_QFN32_4X4
SA0000CQX00
OVRMG1@

UG37
NCP45495XMNTWG_QFN32_4X4
SA0000DUX00
OVRMG2@

+3V_OC_PWR

RG1699 0_0402_5% BS_IN3
RG1698 0_0402_5% BS_IN4
RG1562 10K_0402_5% BS_OK
RG1692 10K_0402_5% SKIP
RG1686 10K_0201_5% ADRS0
RG1682 10K_0402_5% ADRS1
RG1694 10K_0402_5% MODE_SEL
RG1687 10K_0201_5% ADRS0
RG1565 10K_0402_5% MODE_SEL

+3VALW +3V3_SYS
RG1609 0_0402_5%
RG1608 0_0402_5%
+3V_OC_PWR 20mil
CG6802 1U_0402_25V6K

20200714, Follow ONsemi recommend.
0ohm to 49.9ohm
680pF to 0.1uF

<103> CSSN_B+ RG62 49.9 0402 1% CSSN_B+ VIN1N
<103> CSSP_B+ RG1501 49.9 0402 1% CSSP_B+ VIN1P
<103> CSSP_FBVDD RG64 49.9 0402 1% CSSP_FBVDD VIN2P
<103> CSSN_FBVDD RG66 49.9 0402 1% CSSN_FBVDD VIN2N
CG6632 0.1U 0402 25V6
CG6633 0.1U 0402 25V6

Unused SH_Ox, Connect to SH_P2 or VCC.

+3V_OC_PWR RG1697 0_0402_5% CSSP_FBVDD RG1696 0_0402_5%

20209015 follow NV recommend
RG1697 to unstuf f ed
RG1696 to stuf f ed

<30> ADC_IN_P
<30> ADC_IN_N
BS_OK
ADRS0 ADRS1
PAD~D T311
OVRM_SCL OVRM_SDA BS_REF
GND_FET
RG1539 0_0402_5%

@ UG37
VCC IN_N1 IN_P1 IN_P2 IN_N2 IN_P3 IN_N3 IN_P4 IN_N4 DIFF_OUT_P DIFF_OUT_N BG_REF_OUT BV_OK ADRS[0] ADRS[1] SYNC SCL SDA BS_REF RGND GND
BV_IN1 BV_IN2 BV_IN3 BV_IN4 IMON_IN1 MUX_SEL EN_B SKIP IMON_IN2 NC1 NC2 NC3
NCP45495XMNTWG_QFN32_4X4
SA0000DUX00

Address:0x6A

GND_FET
RG1542 750_0402_1% CG7115 1000P_0402_50V
RG1543 750_0402_1% CG7116 1000P_0402_50V
RG1540 0_0402_5%
RG1541 0_0402_5%
BS_IN1 CSSP_B+ CSSP_FBVDD

BS_IN3 RG1705 0_0402_5%
BS_IN4 RG1704 0_0402_5% BS_IN1

OVRM_IMON1 RG1691 0_0402_5%

2020903, follow NV recommend
RG1691 to stuf f ed

SH_O4
ADC_MUX_SEL RG1537 0_0402_5% OC_WARN# <30>
RG1538 10K_0402_5%
SKIP RG1693 30.1K_0402_1%

OVRM_IMON2 RG1695 0_0402_5%

2020903, follow NV recommend
RG1695 to stuf f ed

SH_O3
MODE_SEL
SH_O1

SH_O1 RG1563 237_0402_1% CG7120 0.015U_0402_25V7K
SH_O3 RG1689 0_0402_5% CG8637 0.015U_0402_25V7K
SH_O4 RG1690 0_0402_5% CG8638 0.015U_0402_25V7K

OVRM_SCL OVRM_SDA 0_0402_5% RG1684 RG1685 SCL_GPU SDA_GPU <30>

BS_REF RG1680 0_0402_5% CG7122 1000P_0402_50V
OVRM_SDA RG1681 0_0402_5% RG193 31.6K_0402_1% CG1567 10K_0402_5%

20200714, Follow ONsemi recommend.
RG1688 to Stuf f ed

SH_O4 RG1688 0_0402_5% CG7123 1000P_0402_50V
OVRM_SCL RG1683 0_0402_5% RG1568 365K_0402_1% RG1569 10K_0402_5%
ADRS1 CG7124 1000P_0402_50V

20200716, update circuit, add 0ohm and 0.015uF to OVRM

SH_O1 RG1707 0_0402_5% SWTGP@
OVRM_IMON1 RG1708 0_0402_5% SWTGP@
SWTGP@ CG8640 0.015U_0402_25V7K

UG49 SWTGP@
HA LA WA HB LB WB A2 VDD A0 A1 GND SCL SDA VSS
TPL0102-100PWR_TSSOP14
SA0000DVP00

SWTGP@ RG1591 0_0402_5%
SWTGP@ CG8571 10U_0603_6.3V6M
SWTGP@ CG8570 0.1U_0201_6.3V6K
EC_SMB_CK2 <16,30,58,64,74,77,102>
EC_SMB_DA2 <16,30,58,64,74,77,102>
SWTGP@ CG8569 10U_0603_6.3V6M
SWTGP@ CG8568 0.1U_0201_6.3V6K

+NVVDD
+5VALW
RG544 10K_0402_5% 20200908, change to 0402.
RG543 10K_0201_5%
QG508B DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
QG508A DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
<30,98,102> NVVDD_EN

+1V8_AON
+5VALW
RG510 10_0402_1%
RG509 10K_0402_5%
QG503B DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
QG503A DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
<37> 1V8_AON_EN

20200629 remove +1V8_MAIN discharge circuit.

+1.35VS_VGA
+5VALW
RG1605 10_0402_1% 20200908, change to 0402.
RG1604 10K_0201_5%
QG522B DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
QG522A DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
<30,108> FBVDD/Q_EN

+PEX_VDD
+5VALW
RG1607 3_0402_5%
RG1606 10K_0201_5%
QG523B DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
QG523A DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
<30,98> PEX_VDD_ENP

20200720, change bakc to PEX_VDD_ENP for power down sequence modif i ed

+3V3_SYS
+5VALW
RG514 10_0402_1%
RG513 10K_0402_5%
QG505B DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
QG505A DMN53D0LDW-7 2N SOT363-6 SB000018X00 Vgs:0.5V-1.5V
<37> 3V3_SYS_EN

Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

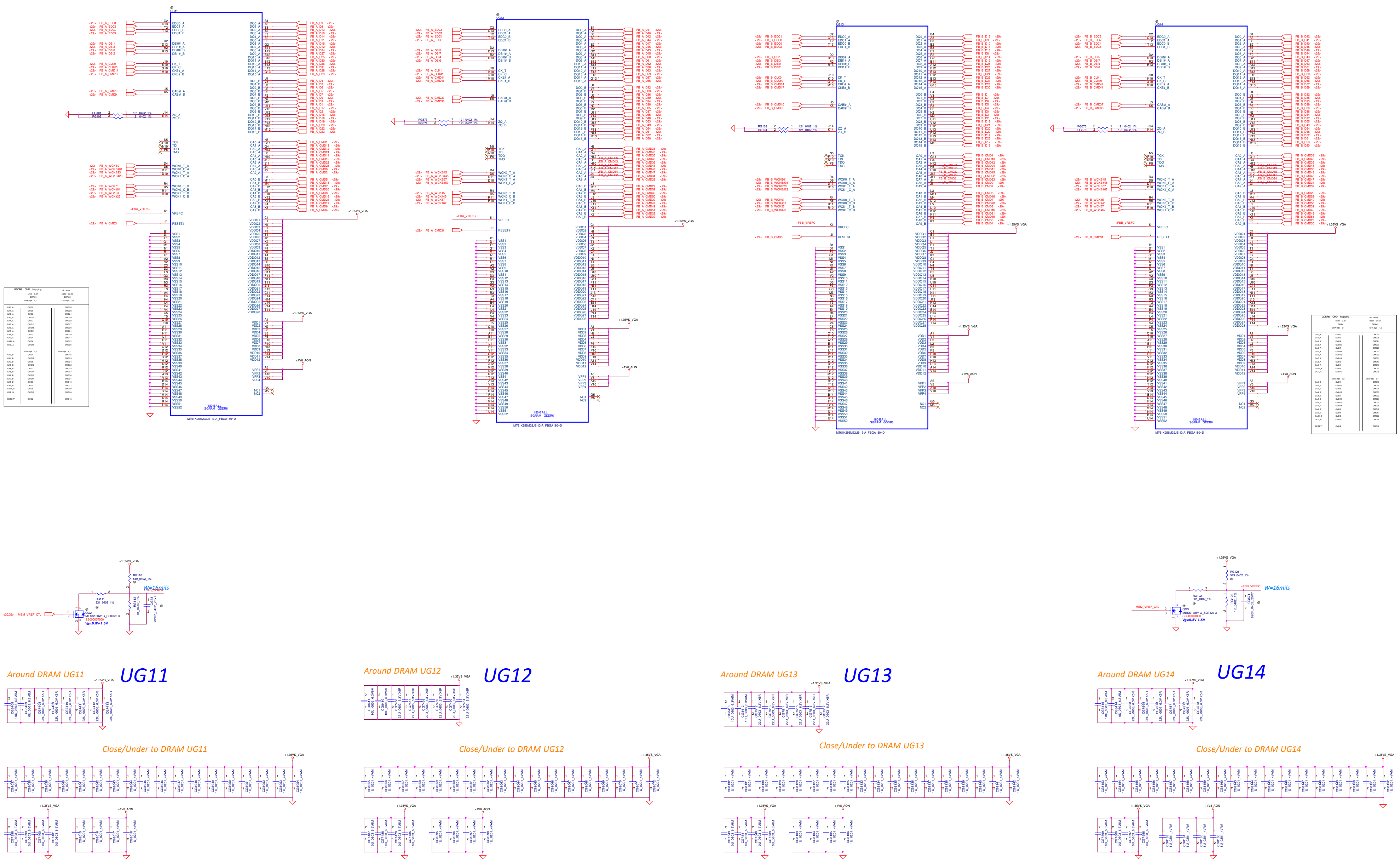
Compal Electronics, Inc.

Title: OC, Discharging

Size | Document Number: LA-K741P | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 34 of 114

6/15 Modify



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title: VRAM_GDDR6_AB
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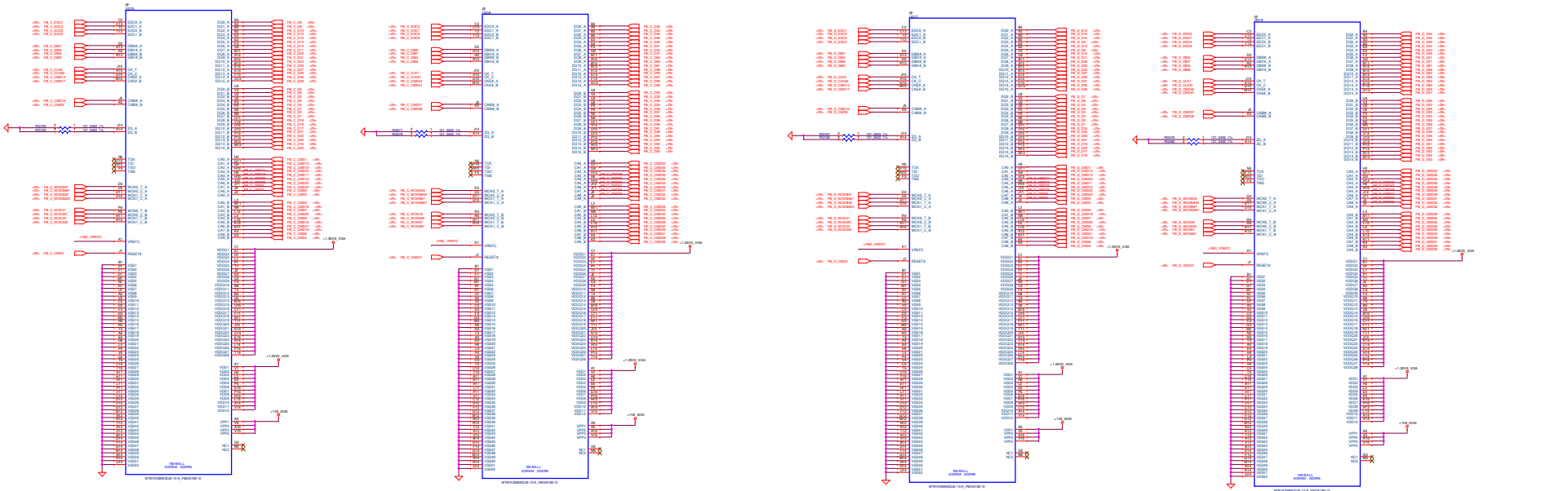
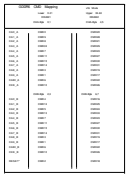
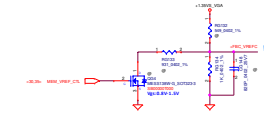
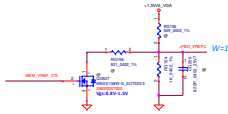
				Date: Thursday, December 03, 2020 / Sheet 35 of 114

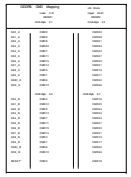
6/15 Modify





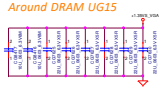




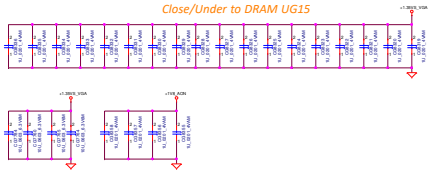


UG15

Around DRAM UG15

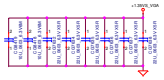


Close/Under to DRAM UG15

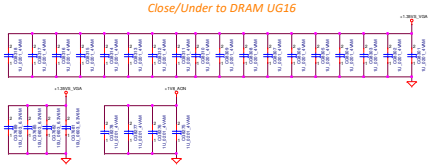


UG16

Around DRAM UG16

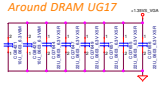


Close/Under to DRAM UG16

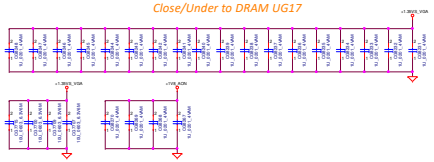


UG17

Around DRAM UG17

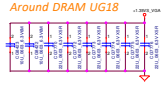


Close/Under to DRAM UG17

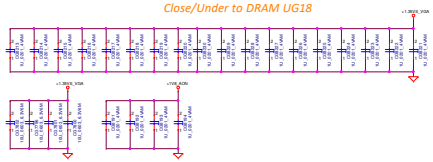


UG18

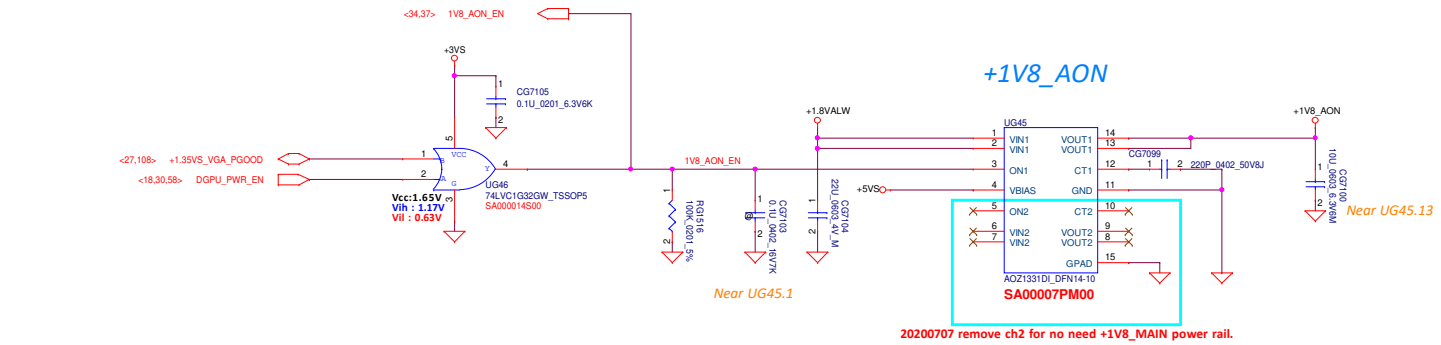
Around DRAM UG18

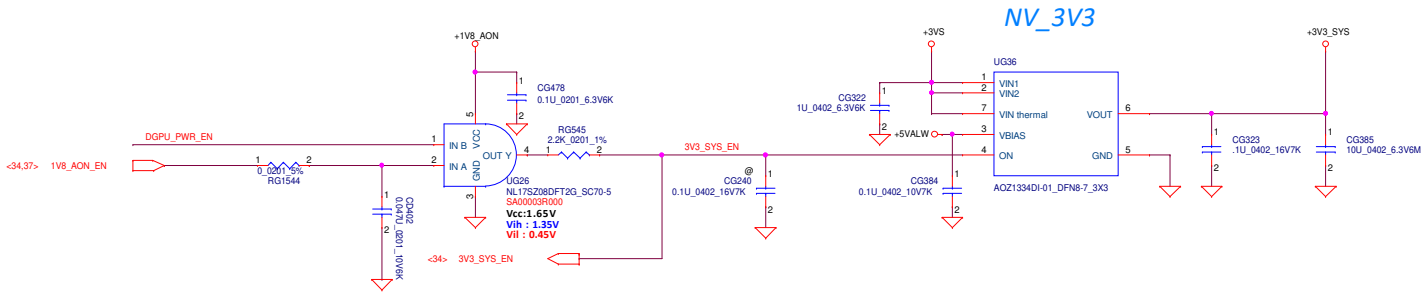


Close/Under to DRAM UG18



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/08/07	Deciphered Date	2016/08/07	Title: VRAM_GDDR5_CD
Size: A3	Document Number: LA-K741P	Rev: 1.0
Date: Wednesday, May 04, 2016	Sheet: 36 of 53	





Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: **DGPU_DC/DC Interface**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 37 of 114

Main Func = LCD

LCD power control

W=80 mils

W=80 mils

Place close to JEDP

SA000070V00

Vonh : 1.2V

Vonl : 0.5V

LCD backlight power control

W=80 mils

W=80 mils

W=60 mils

Main Func = CAM

CAMERA POWER

Main Func = DDS

Panel RST

EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

Main Func = eDP MUX

CPU

GPU IFPD

EDP_MUX_SW	Input	Function
L	IN1	IGPU
H	IN2	DGPU

SA0000DY10

20201013, change A0 ver. to A2 ver.

20201119 add DV18 as ESD requirement.

20200908, DV12 layout add.

20200908, modify GPU LCD_EN to 3.3V input

20200709, add DDS_DETEST to control UV21 enable status.

SA00002KE00

S1	OE	Output	Function	UV21
L	L	A=B1	Non DDS-IGPU	Enable
H	L	A=B2	Non DDS-DGPU	Enable
X	H	A=X	DDS	Disable

Main Func = DDS Auto Detect

EN#	IN (DDS_DETECT)	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	Non-DDS
L	H	OFF	ON	DDS
H	X	OFF	OFF	X

20201116, modify to SA000014500, due to GPU ENVDD power level change to 3.3V

DDS_Detect

DDS_DETECT_EC	GPU DID
L	DDS
H	Non-DDS

GSYNC_DET	GSYNC
0 (G-Sync Cable)	0 (GSYNC)
1 (M/B Default)	1 (NGSYNC)

DDS_DETECT	DDS
1 (MOS_UV68)	1 (DDS)
0 (MOS_UV68)	0 (NDDS)

Security Classification	Compal Secret Data	
Issued Date	2017/05/15	Deciphered Date 2018/02/05

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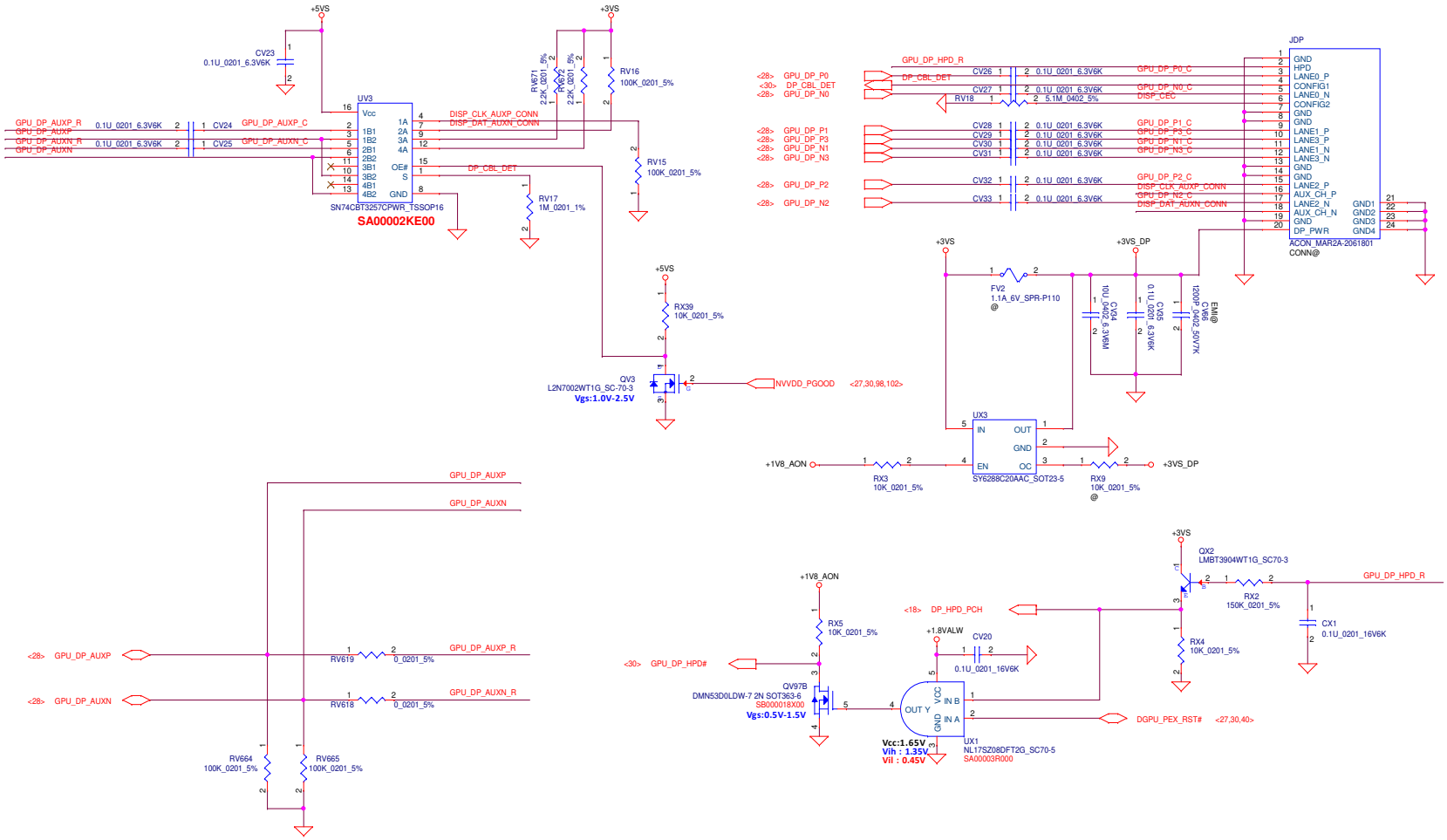
Compal Electronics, Inc.

Title: eDP/Camera/TS

Size: LA-K741P | Document Number | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 38 of 114



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **Mini DP**

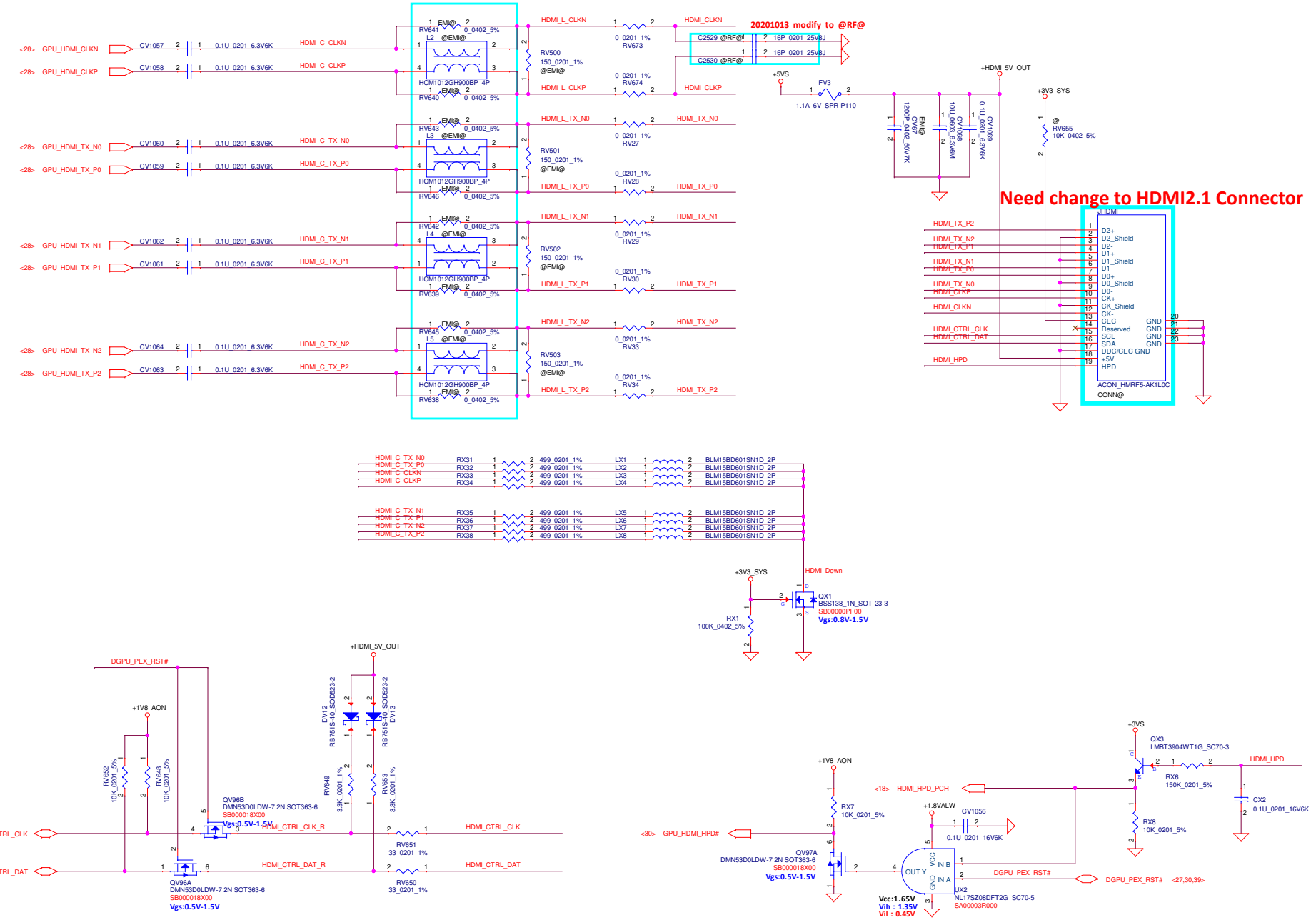
Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 39 of 114

20200708, EMI modify CMC part to SM070003V00 as reserved
20201118, modify L2-L5 footprint to -NPM.
20201202, modify series resistor t o 0ohm.

20201013 modify to @RF@

Need change to HDMI2.1 Connector



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-K741P | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 40 of 114

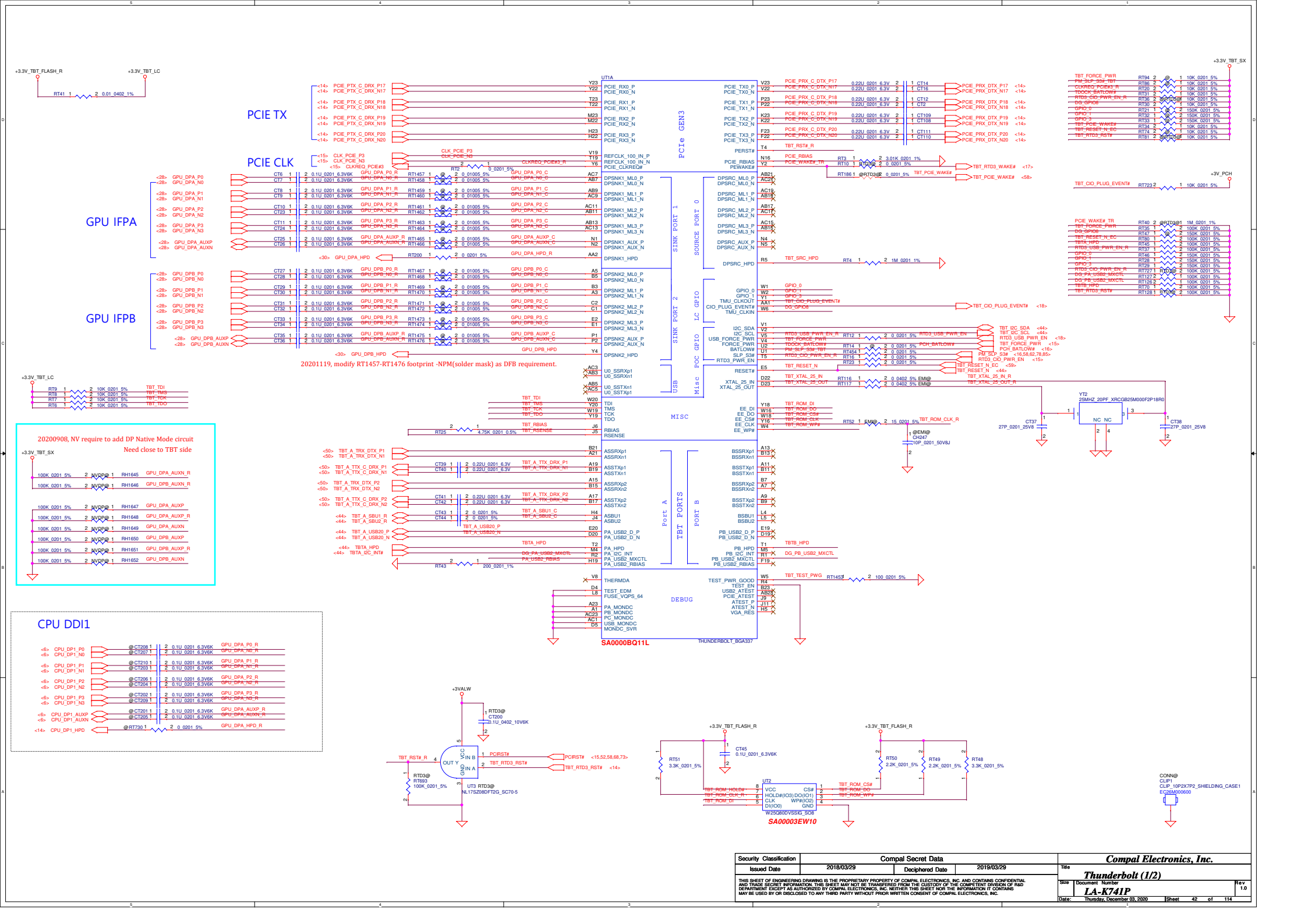
Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

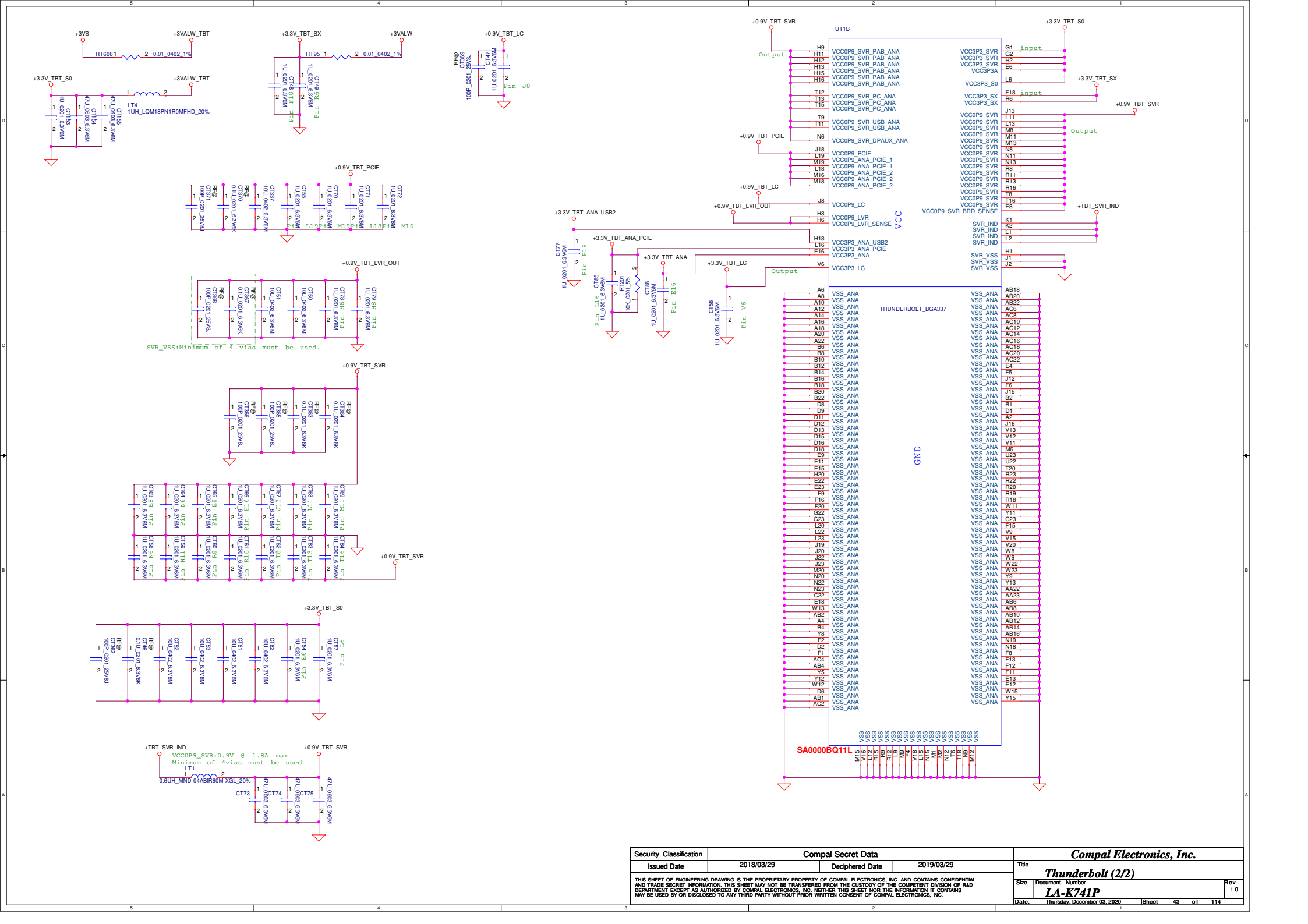
Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 41 of 114



Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

Compal Electronics, Inc.	
Title	Thunderbolt (1/2)
Size	Document Number: LA-K741P
Rev	1.0
Date:	Thursday, December 03, 2020
Sheet	42 of 114



Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

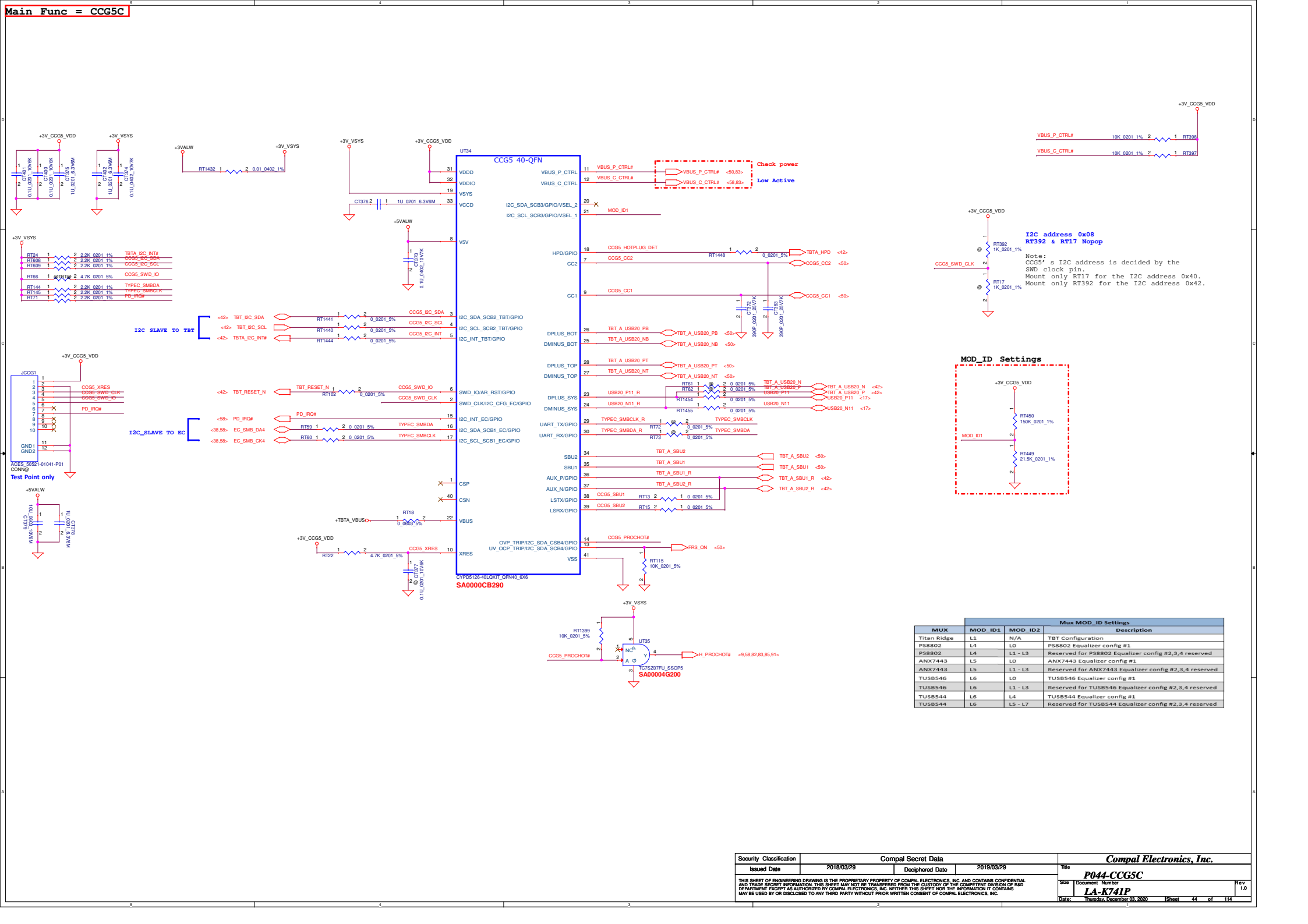
Compal Electronics, Inc.

Title: **Thunderbolt (2/2)**

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 | Sheet 43 of 114

Main Func = CCG5C



Mux MOD_ID Settings			
MUX	MOD_ID1	MOD_ID2	Description
Titan Ridge	L1	N/A	TBT Configuration
PS8802	L4	L0	PS8802 Equalizer config #1
PS8802	L4	L1 - L3	Reserved for PS8802 Equalizer config #2,3,4 reserved
ANX7443	L5	L0	ANX7443 Equalizer config #1
ANX7443	L5	L1 - L3	Reserved for ANX7443 Equalizer config #2,3,4 reserved
TUSB546	L6	L0	TUSB546 Equalizer config #1
TUSB546	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved
TUSB544	L6	L4	TUSB544 Equalizer config #1
TUSB544	L6	L5 - L7	Reserved for TUSB544 Equalizer config #2,3,4 reserved

Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

Compal Electronics, Inc.

Title: P044-CCG5C

Size: | Document Number: LA-K741P | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 44 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 45 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 46 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 47 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 48 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

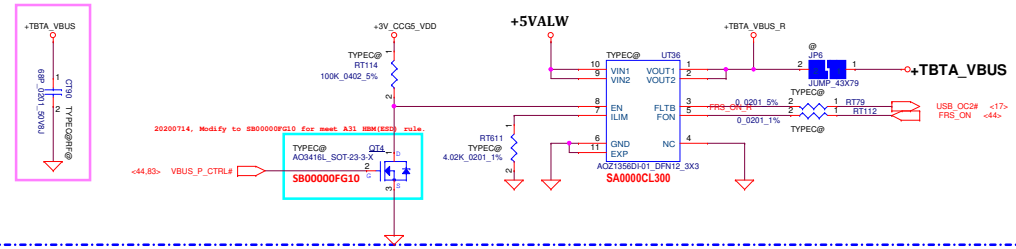
Date: Thursday, December 03, 2020 Sheet 49 of 114

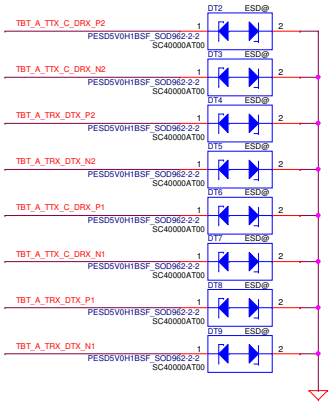
CCG5 Power path Port1

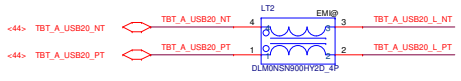
Type-C 5V Provide Path Control

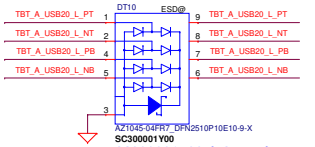
Support PD3.0

5V@3A



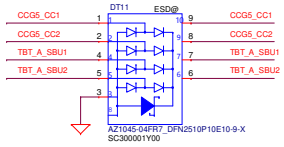


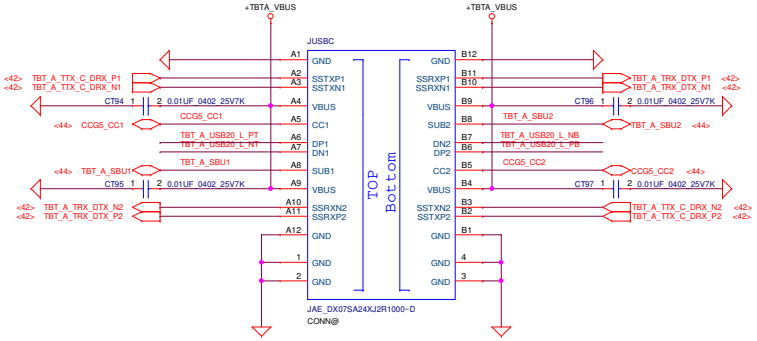


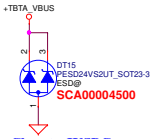


SC300001Y00 (ESD use)
SC300002800 (symbol)

20200803, modify DT10 to SC300001Y00, due to SA00003Z00 removed from A31 pool.







Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

Compal Electronics, Inc.	
Title	PD+USB3.1 type C
Size	Document Number: LA-K741P
Rev	1.0
Date:	Thursday, December 03, 2020
Sheet	50 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

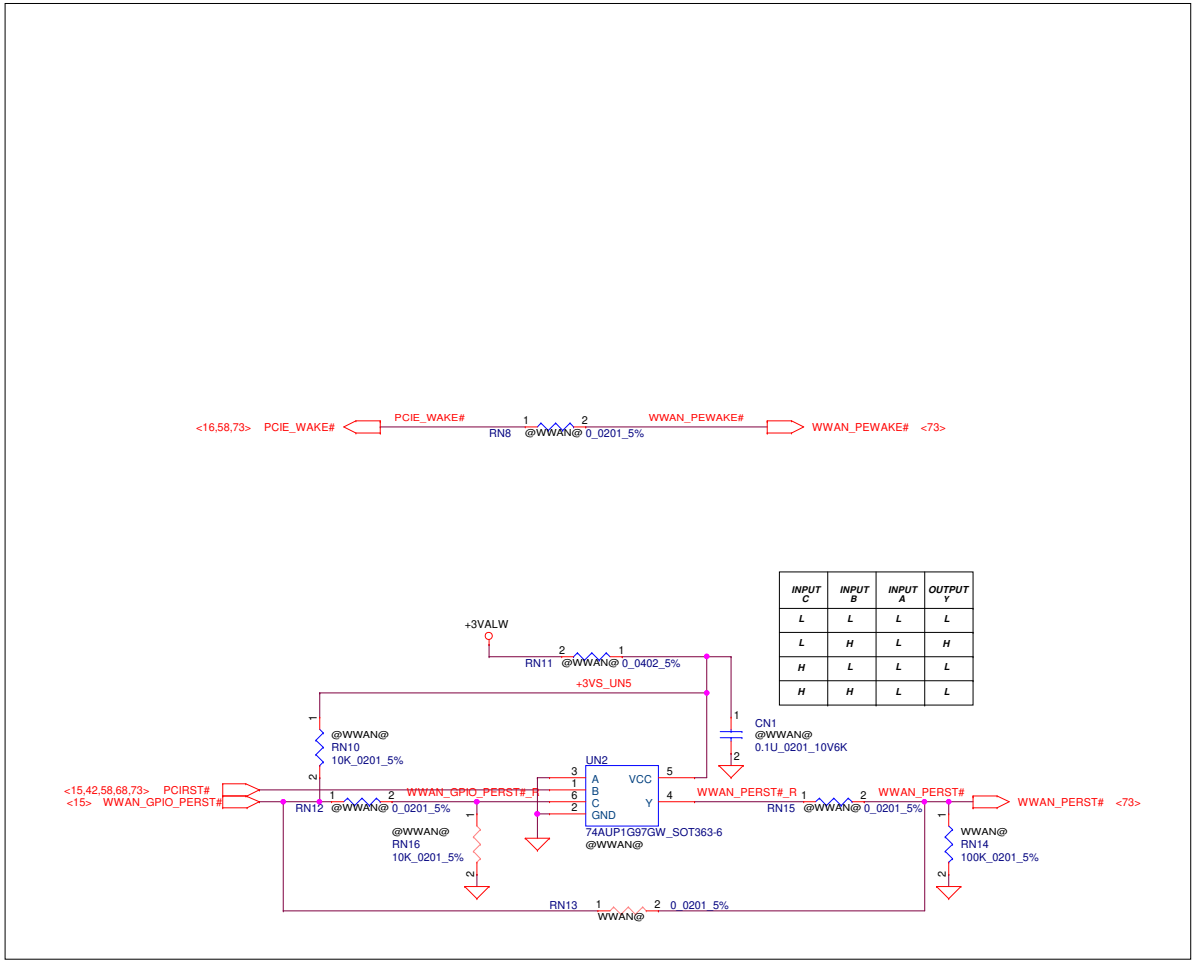
Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 51 of 114

Main Func = WWAN



Security Classification	Compal Secret Data		
Issued Date	2018/08/31	Deciphered Date	2019/08/06

Compal Electronics, Inc.

Title: **P052-WWAN**

Size | Document Number: **LA-K741P** | Rev: 1.0

Date: Thursday, December 03, 2020 | Sheet 52 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 53 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 54 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 55 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 56 of 114

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-K741P	1.0

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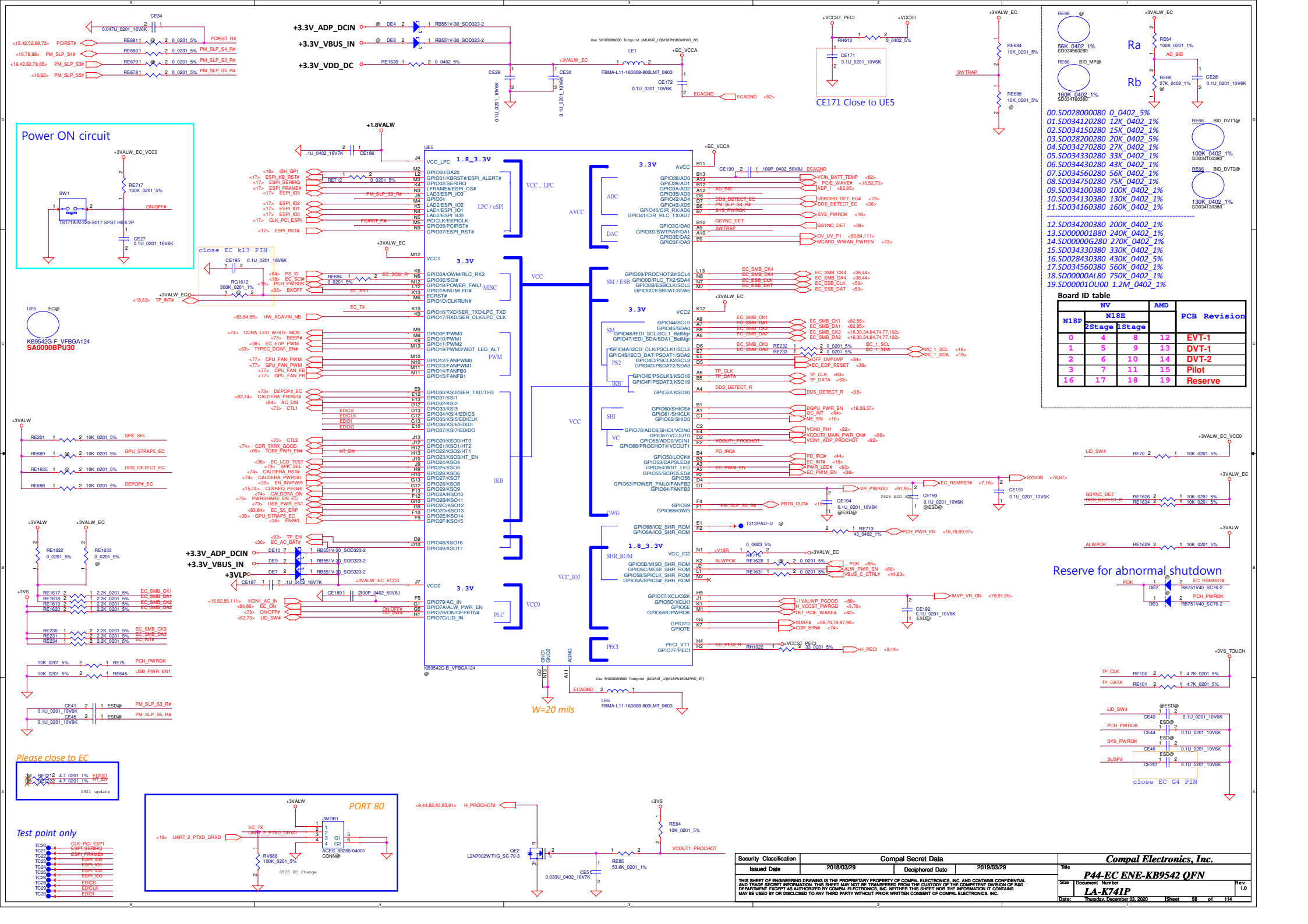

Board ID table

NV			AMD	PCB Revision
N18P	N18E			
	2Stage	1Stage		
0	4	8	12	EVT-1
1	5	9	13	DVT-1
2	6	10	14	DVT-2
3	7	11	15	Pilot
16	17	18	19	Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

Compal Electronics, Inc.

Title: P44-EC ENE-KB9542 QFN

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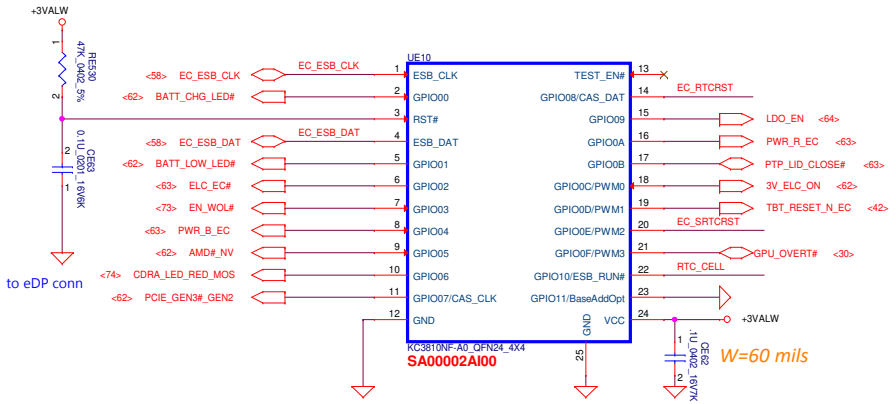
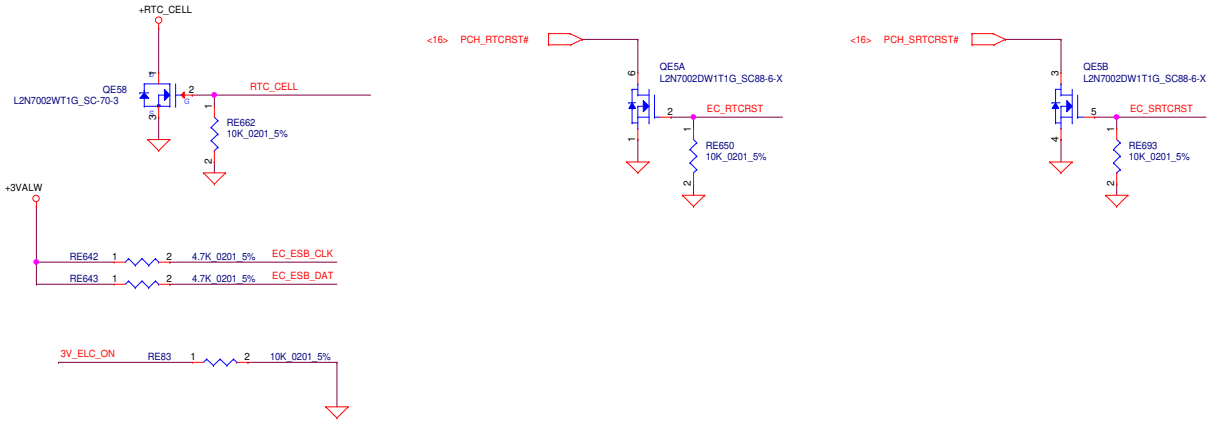
Main Func = EC ENE-KC3810



Main Func = S5 Lid



Security Classification	Compal Secret Data		
Issued Date	2018/03/29	Deciphered Date	2019/03/29

Compal Electronics, Inc.

Title: **EC ENE-KB9022/S5 LID**

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Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

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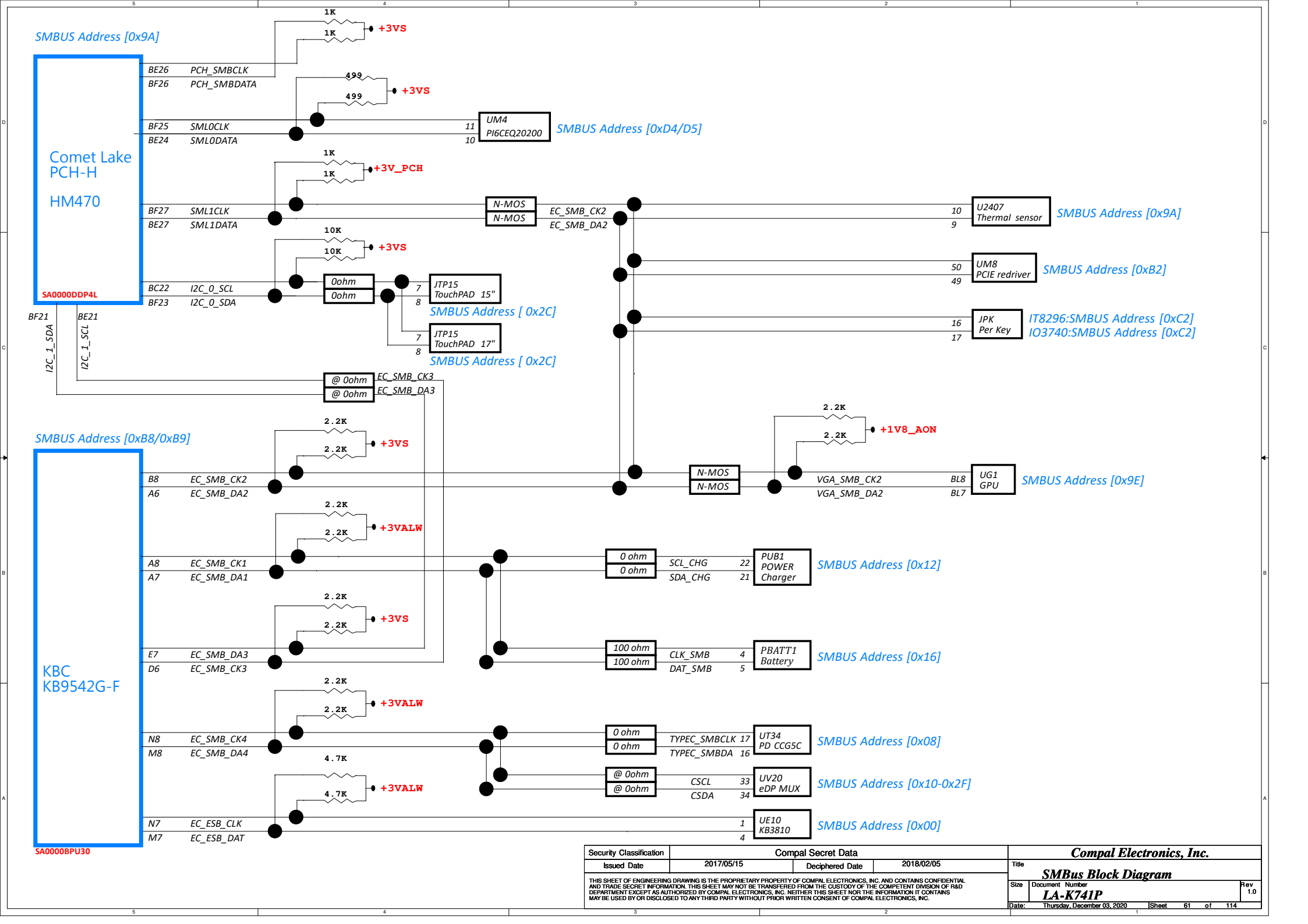

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: SMBus Block Diagram

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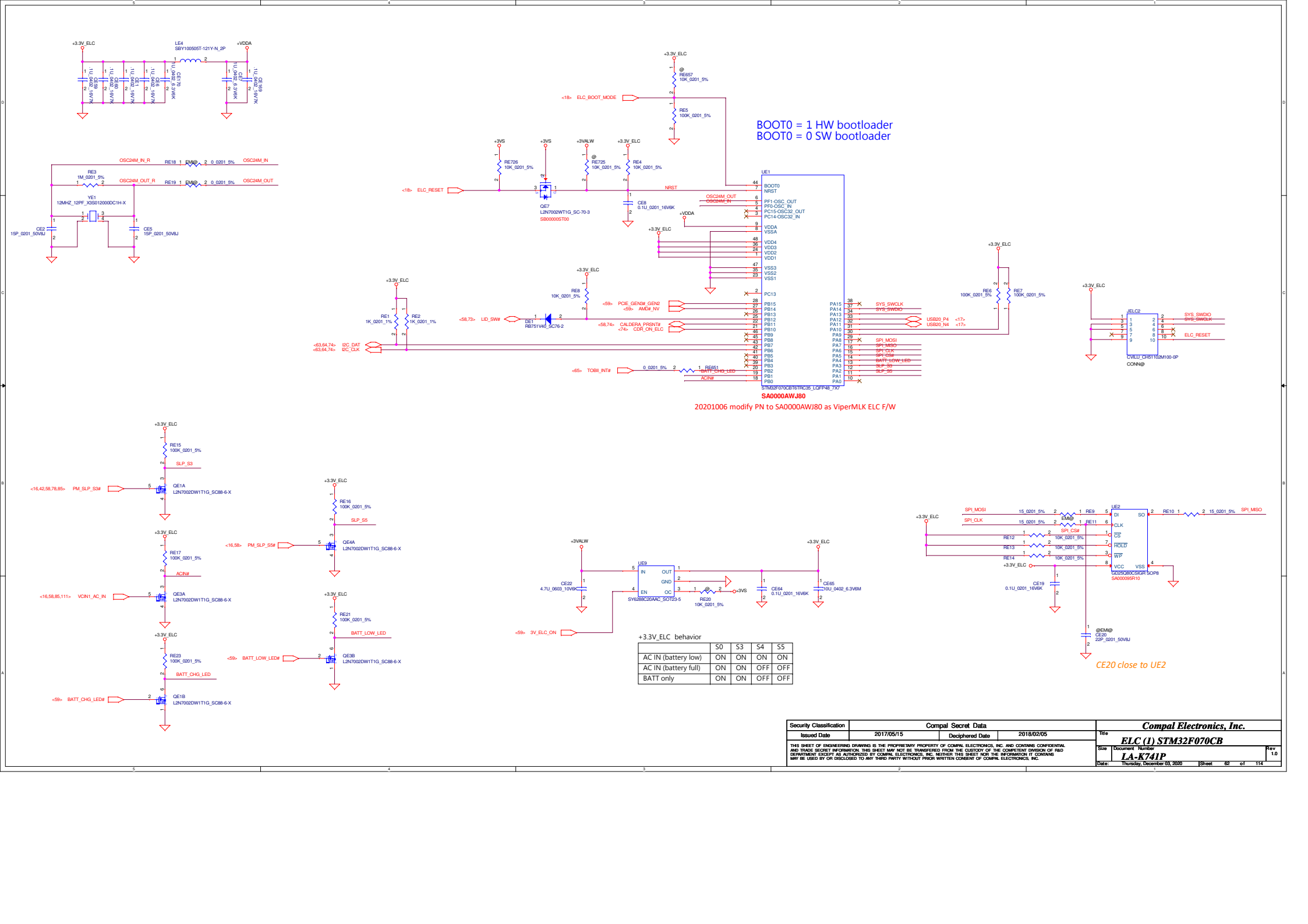
BOOT0 = 1 HW bootloader
BOOT0 = 0 SW bootloader
SA0000AWJ80
20201006 modify PN to SA0000AWJ80 as ViperMLK ELC F/W
+3.3V_ELC behavior
S0 S3 S4 S5
AC IN (battery low) ON ON ON ON
AC IN (battery full) ON ON OFF OFF
BATT only ON ON OFF OFF
CE20 close to UE2
Security Classification
Compal Secret Data
Issued Date
2017/05/15
Deciphered Date
2018/02/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
ELC (1) STM32F070CB
Size
Document Number
LA-K741P
Rev
1.0
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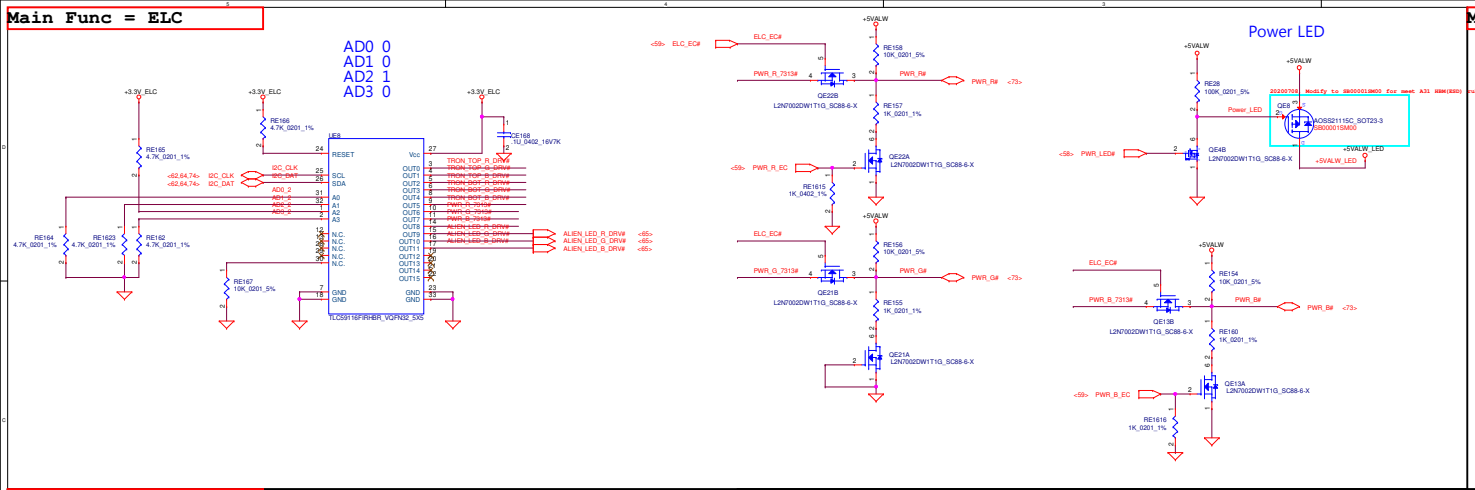
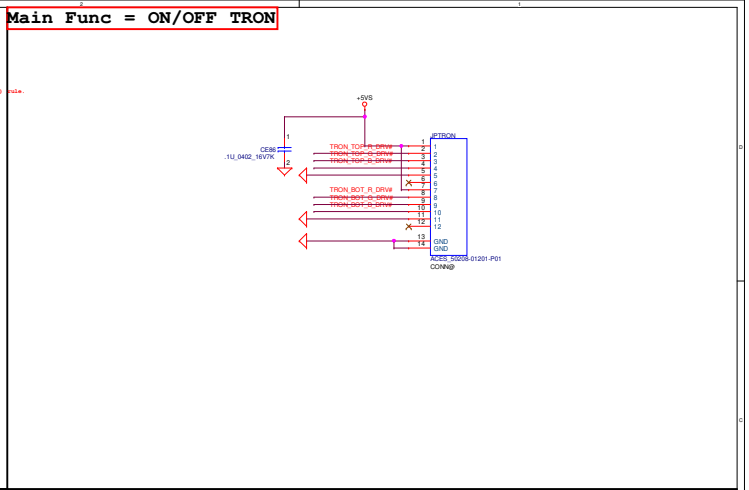
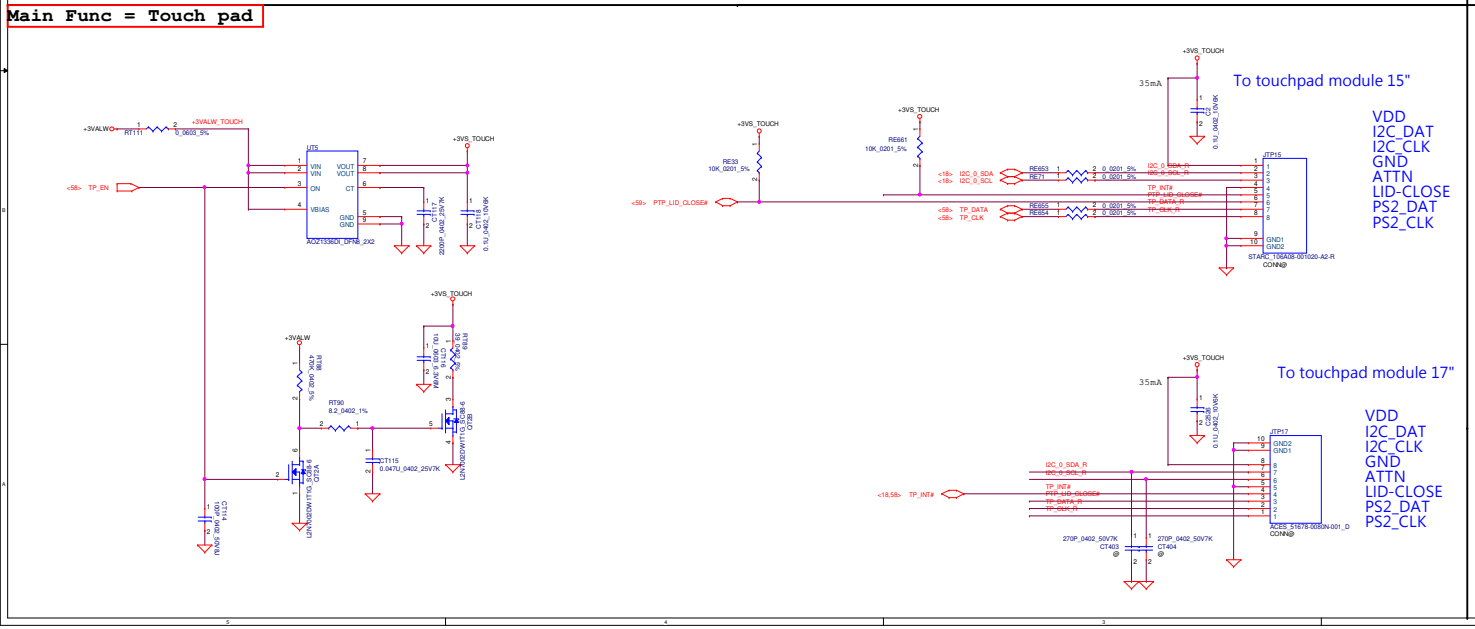
Main Func = ELC



Main Func = ON/OFF TRON



Main Func = Touch pad



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/05/15	Deciphered Date	2018/02/05
Title	ELC (2) TP/PW/LOGO/TRON		
Size	Document Number		Rev
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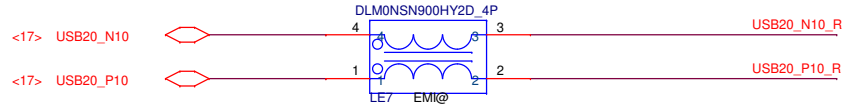
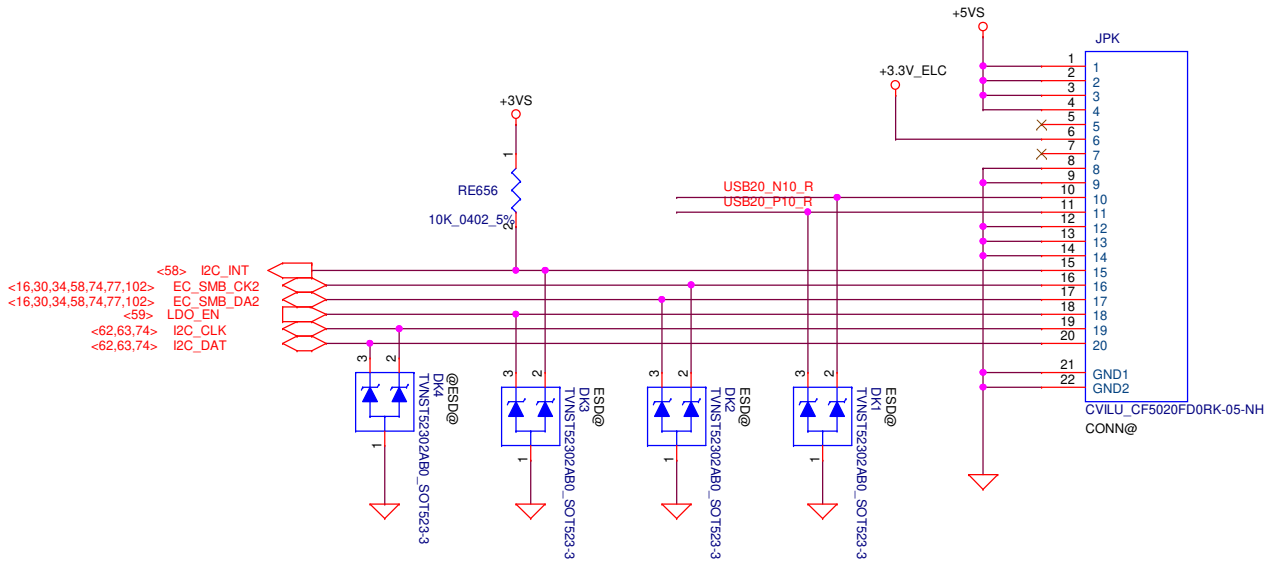
11/26 update





Per Key pin define

Pin1~4	VBUS
Pin5	NC
Pin6	+3.3V_ELC
Pin7	NC
Pin8~9	GND
Pin10	D-
Pin11	D+
Pin12~14	GND
Pin15	I2C_INT
Pin16	I2C_CLK(EC)
Pin17	I2C_DAT(EC)
Pin18	LDO_EN
Pin19	I2C_CLK(ELC)
Pin20	I2C_DAT(ELC)

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Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **ELC (3) KBBL/Per Key**

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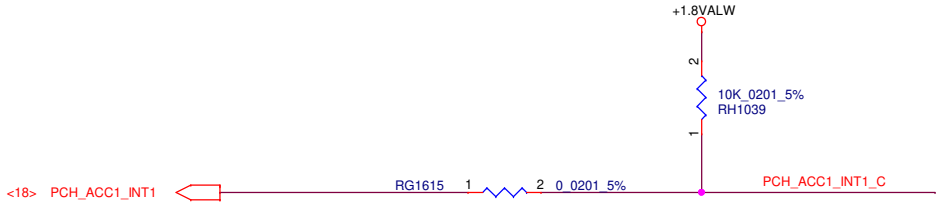

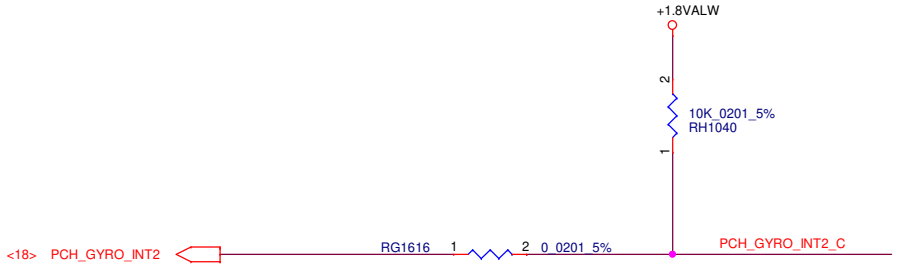

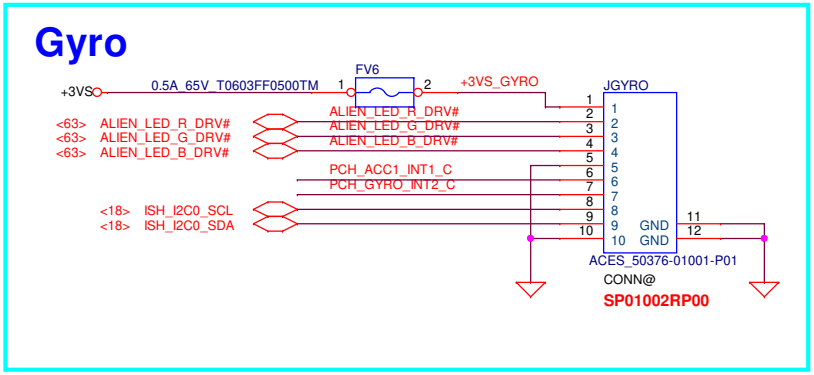

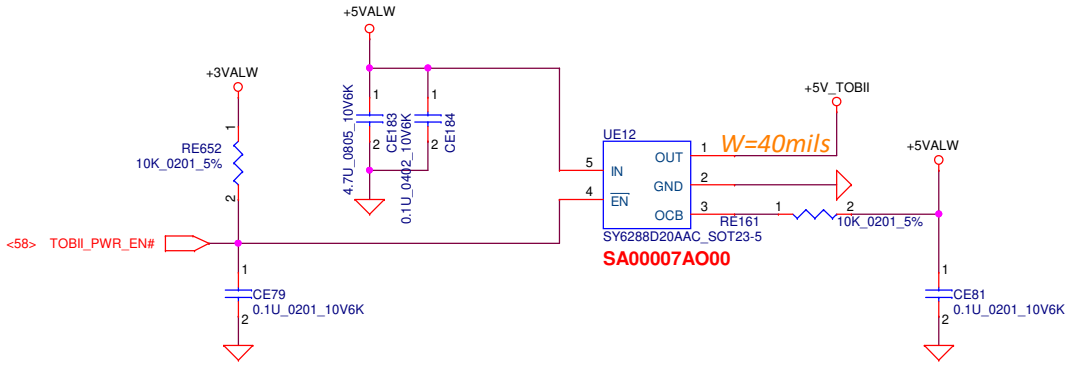

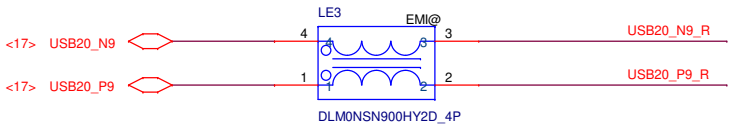

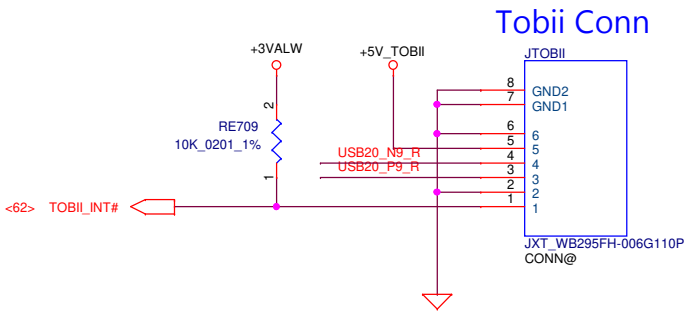

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **ELC (4) NKRO KB**

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Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title

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Compal Electronics, Inc.

Title

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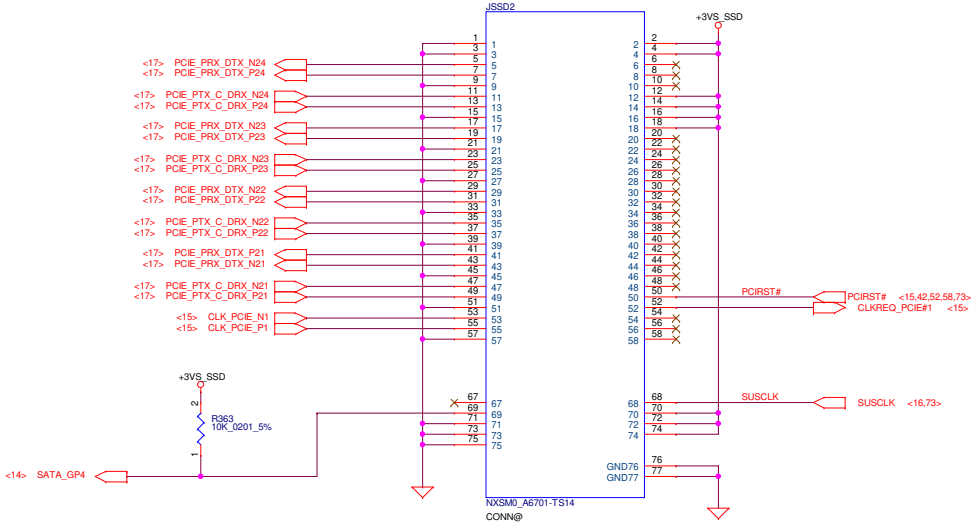
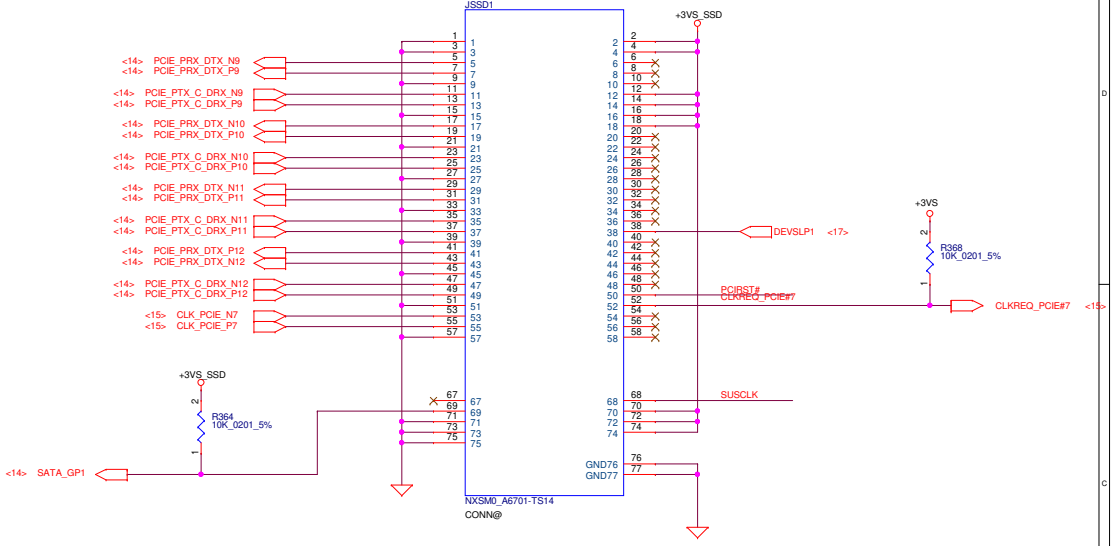
PCIe
SSD#2 , 2280

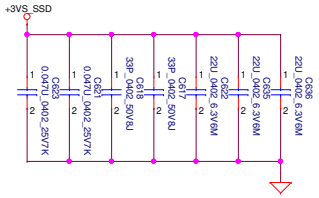


PEDET	Module Type
0	SATA
1	PCIe

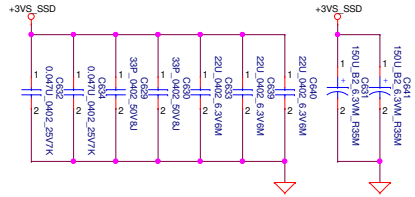
PCIe / SATA SSD
SSD#1 , 2280

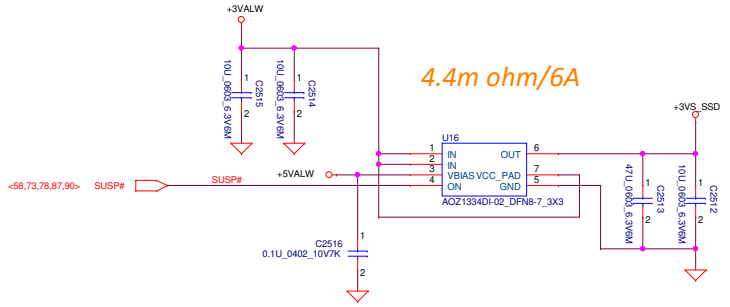


JSSD2



JSSD1





Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

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Title: **NGFF SSD**

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Compal Electronics, Inc.

Title

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Compal Electronics, Inc.

Title

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Compal Electronics, Inc.

Title

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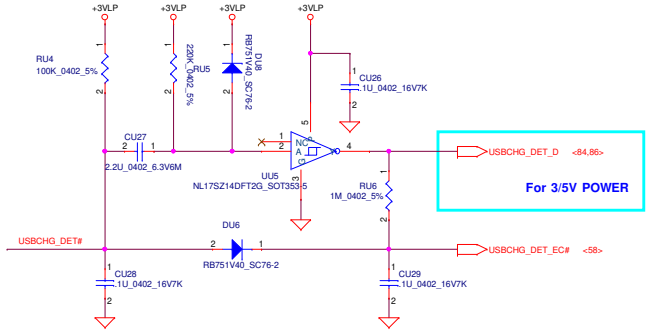
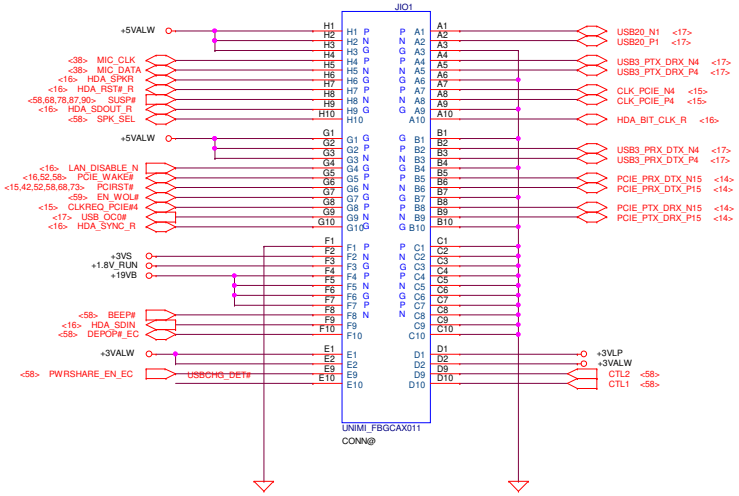
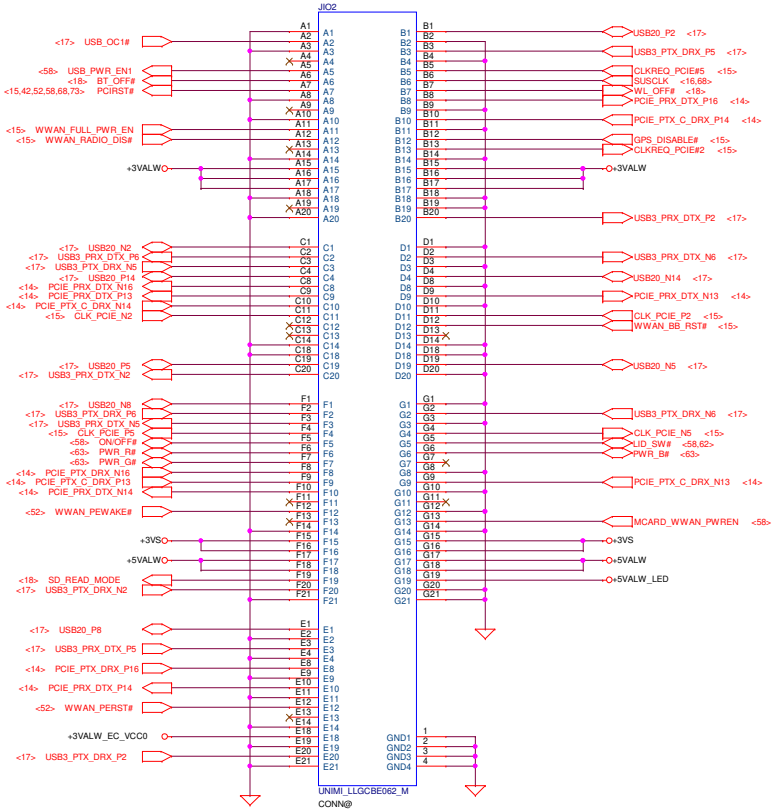
USB charge for DC S5





For Audio DB conn



For USB DB conn

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title: IO/B			
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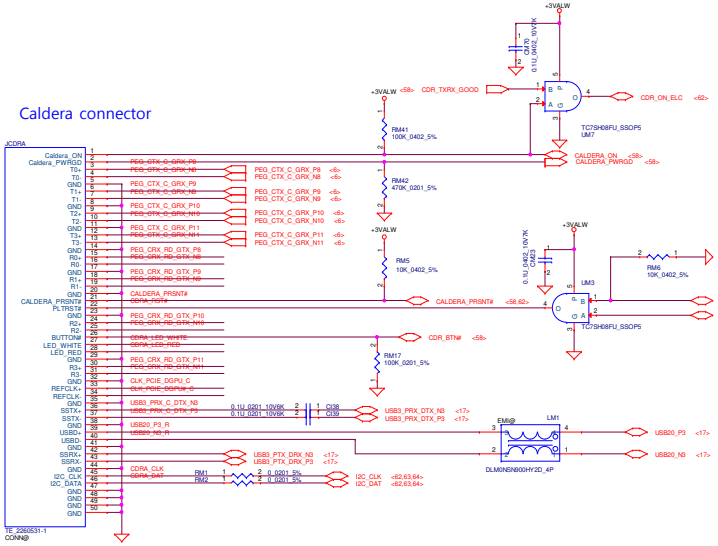
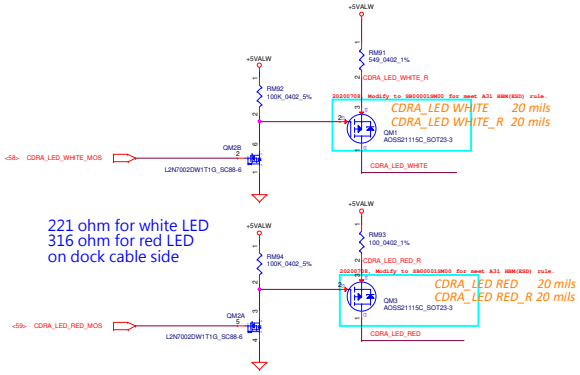
Caldera connector



221 ohm for white LED
316 ohm for red LED
on dock cable side

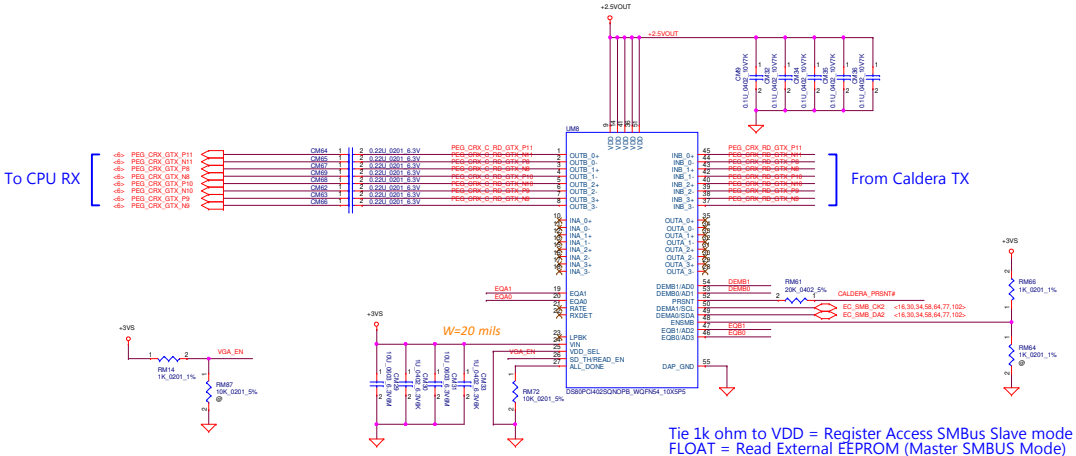


Main	2nd
ZZZ X76PER@	ZZZ X76IDT@
ALT_GROUP PARTS PCIE PERICOM FDQ51 X7885231L14	ALT_GROUP PARTS PCIE IDT FDQ51 X7885231L15
UM4 PERICOM@ PI6CEQ20200LIEX TSSOP20 PCIE BUFFER SA00007JZ00	UM4 IDT@ 9DB233AGLFT TSSOP 20P SA00007ZU00
CM16 PERICOM@ 1U 0402 10V7K SE102104K00	CM16 IDT@ 1U 10V 0402 SE000000QL10
RM25 PERICOM@ 475 0201 1% SD00001NZ00	RM25 IDT@ 412 +-1% 0201 SD00002CH60
CM98 PERICOM@ 0.01U 0402 16V7K SE076103KB0	CM98 IDT@ 0.1U 0402 16V7K SE076104KB0
RM27 PERICOM@ 33 +-1% 0201 SD041330AB0	RM27 IDT@ 27 +-1% 0201 SD00000IV00
CM99 PERICOM@ 0.01U 0402 16V7K SE076103KB0	CM99 IDT@ 0.1U 0402 16V7K SE076104KB0
RM28 PERICOM@ 33 +-1% 0201 SD041330AB0	RM28 IDT@ 27 +-1% 0201 SD00000IV00

PCIe Clock Buffer	RM25	RM27 / RM28	CM16	CM98 / CM99
* Pericom (SA00007JZ00) X7885231L14	SD00001NZ00 (475 +-1% 0201)	SD041330A80 (33 +-1% 0201)	SE102104K00 (0.1U +-10% 0402)	SE076103KB0 (0.01U 16V K X7R 0402)
IDT (SA00007ZU00) X7885231L15	SD00002CH00 (412 +-1% 0201)	SD00000IV00 (27 +-1% 0201)	SE000000QL10 (1U +-10% 0402)	SE076104KB0 (0.1U 16V K X7R 0402)

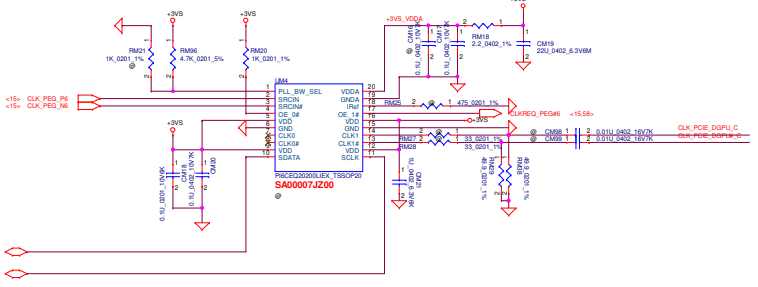
To CPU RX

From Caldera TX

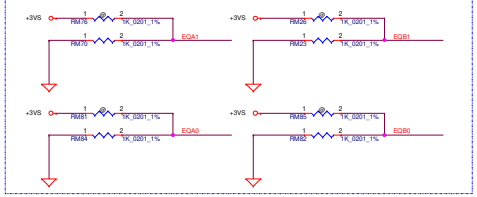


Tie 1k ohm to VDD = Register Access SMBus Slave mode
FLOAT = Read External EEPROM (Master SMBUS Mode)
Tie 1k ohm to GND = Pin Mode

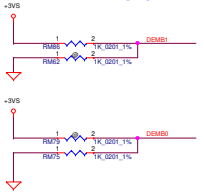
PCIE_CLK_BUFFER



EQ*MB



DEM*EGPU



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/05/15	Deciphered Date 2018/02/05	Title: Caldera Docking
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Compal Electronics, Inc.

Title

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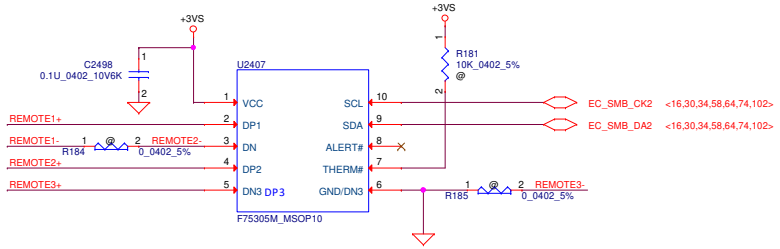
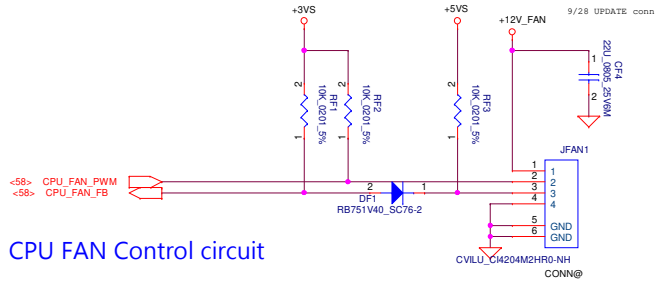
Fintek thermal sensor---> CPU core, DIMM

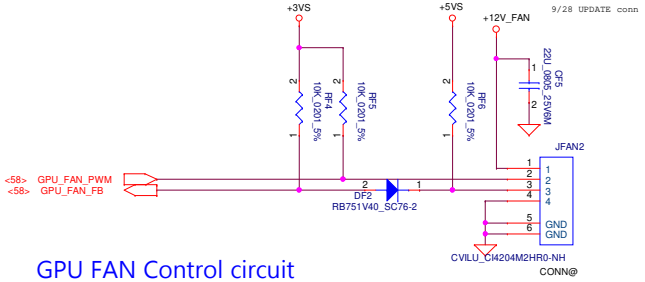


Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR

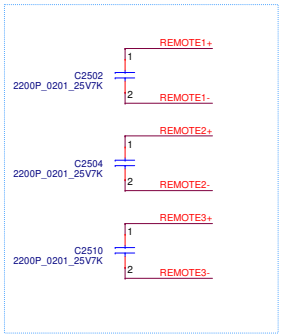


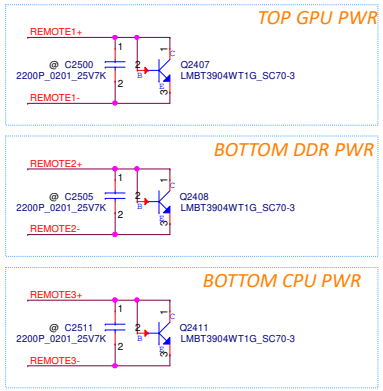
CPU FAN Control circuit



GPU FAN Control circuit

Close U2407





REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.

Title: **FAN/Thermal**

Size	Document Number	Rev
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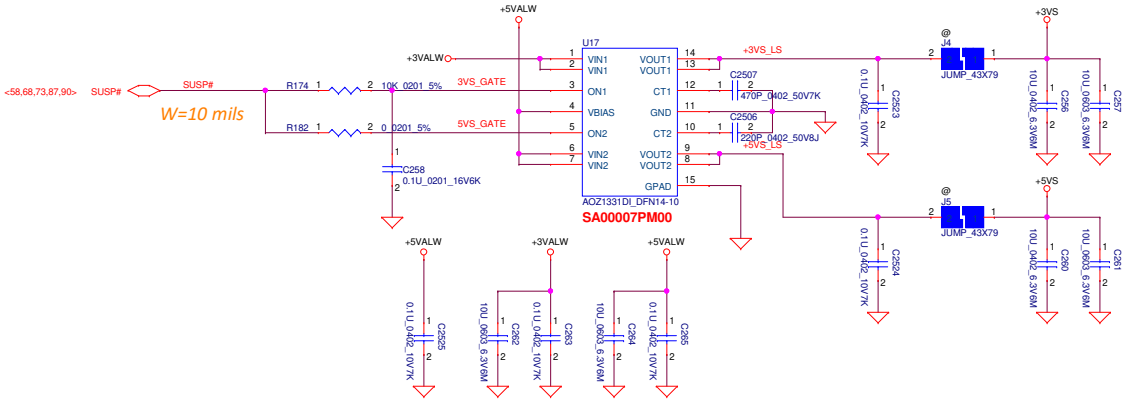
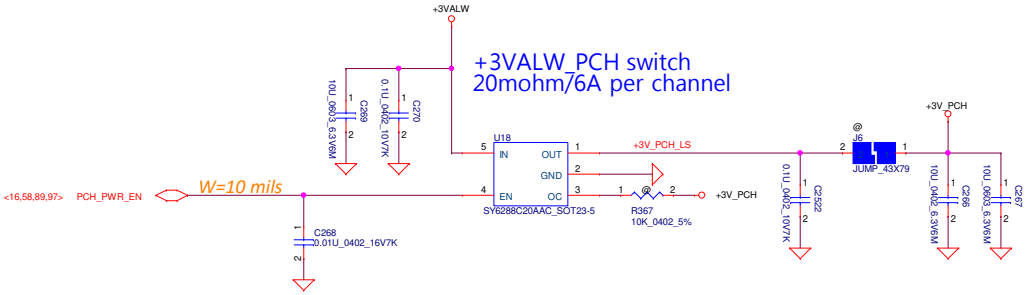
+5VS and +3VS switch
20mohm/6A per channel



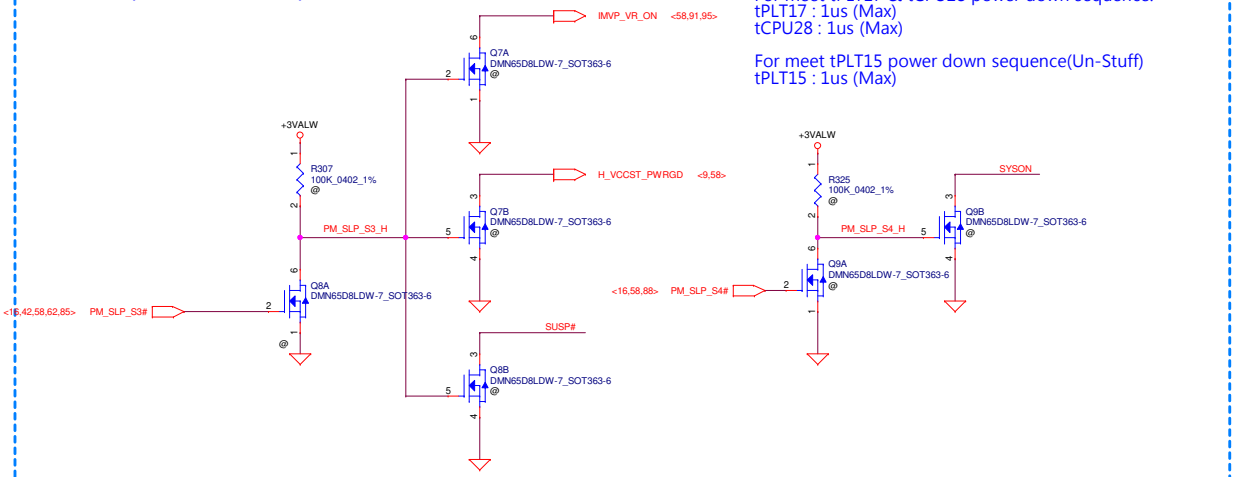
+3VALW_PCH switch
20mohm/6A per channel



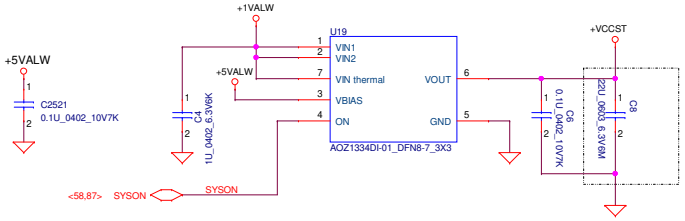
Add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuff)
tPLT15 : 1us (Max)

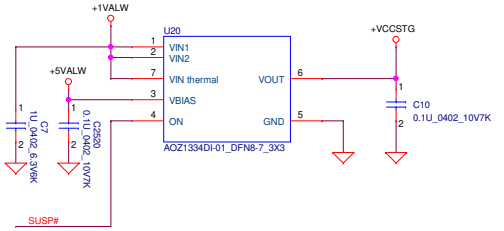


+VCCST switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

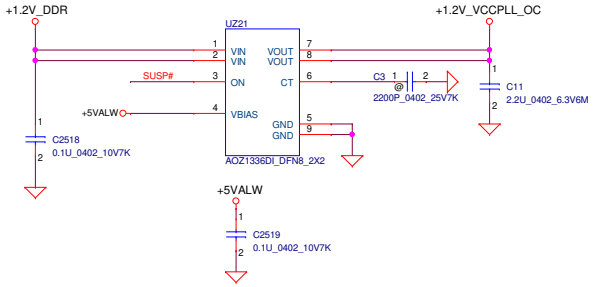


Main source AOS SA00008A800 (SIC AOZ1334DI-01 DFN8P SINGLE LOADSW
2nd source APEC SA00006V300 (SIC APE8939GNB DFN8P LOADSWITCH)
3rd source EMC SA00008R600 (SIC EM5201V DFN3X3 8P LOADSWITCH)

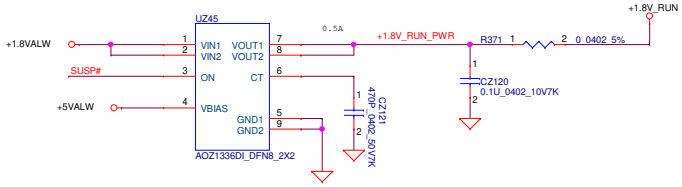
+VCCSTG switch
4.4mohm/6A
TR=12.5us@Vin=1.05V



+1.2V_VCCPLL_OC switch
4.4mohm/6A
TR=12.5us@Vin=1.05V



+1.8V_RUN Source



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: LA-K741P		Rev: 1.0
Date: Thursday, December 03, 2020	Sheet 78 of 114		

Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

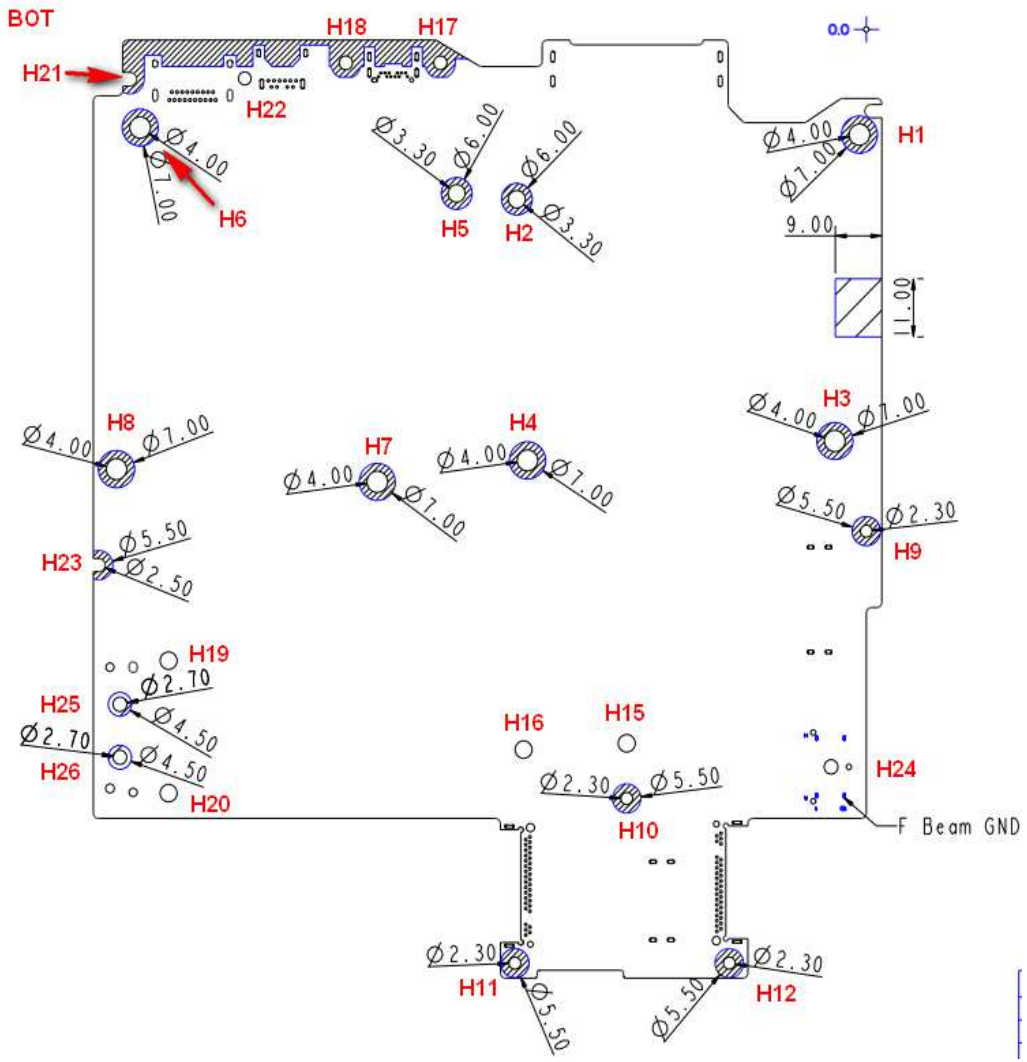
Compal Electronics, Inc.

Title

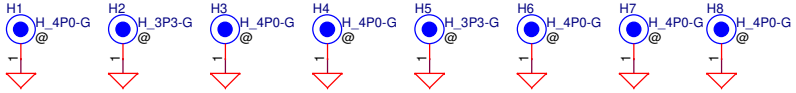
Size	Document Number	Rev
	LA-K741P	1.0

Date: Thursday, December 03, 2020 Sheet 79 of 114

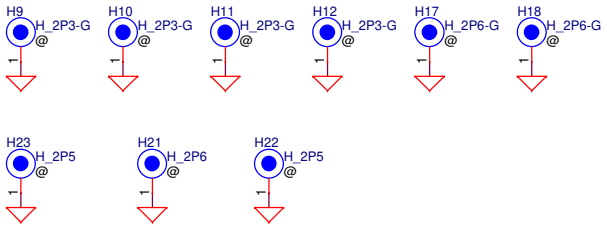
Main Func = Screw



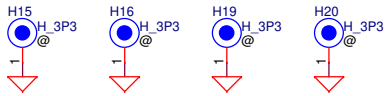
CPU & GPU



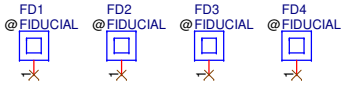
PTH



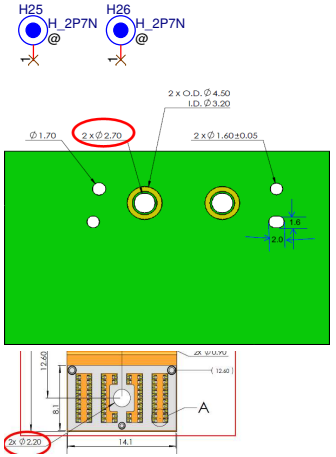
Stand-off



Fiducial Mark



PC-Beam (Stand-off)



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2018/02/05

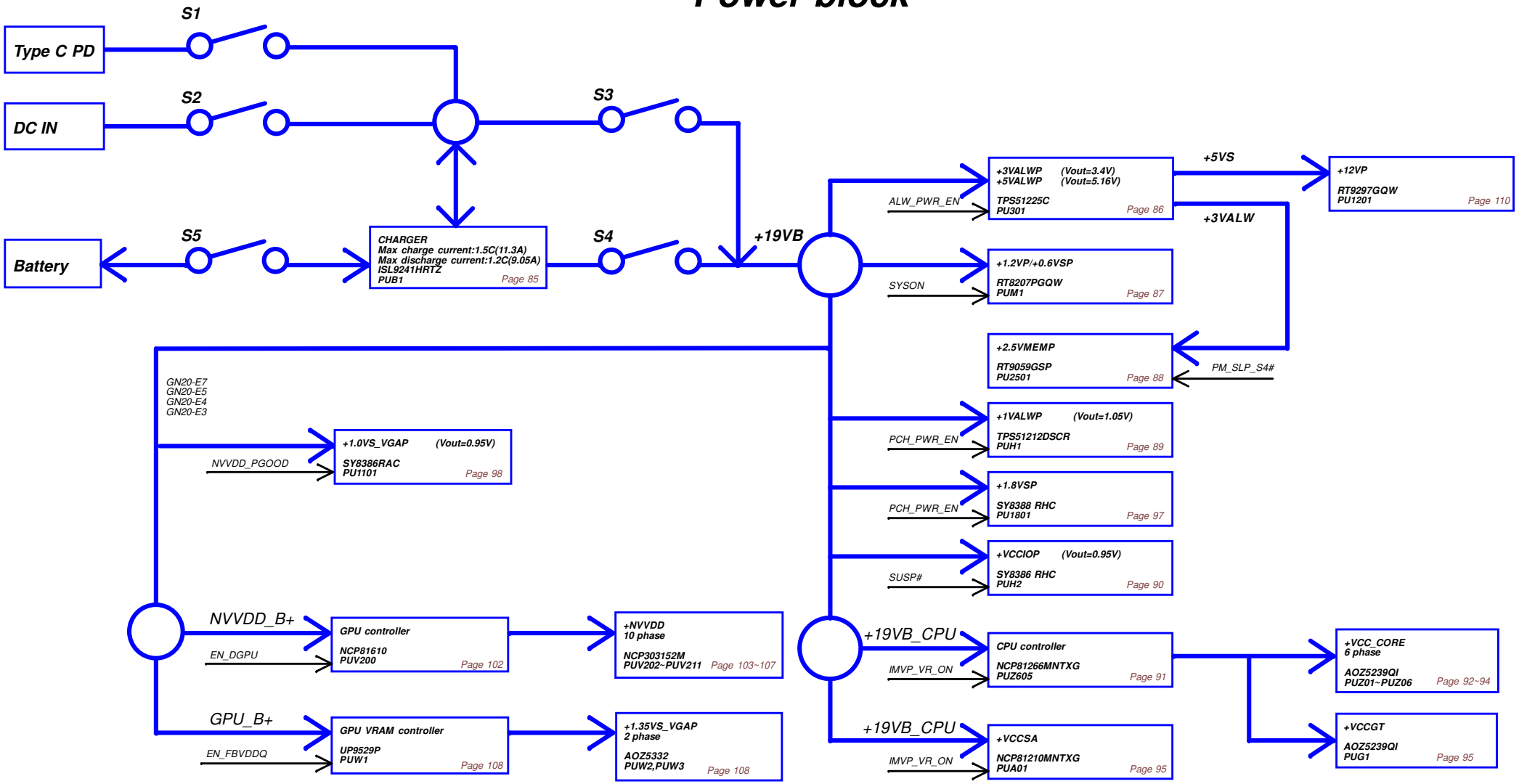
Compal Electronics, Inc.

Title: **Screw Hole**

Size | Document Number: **LA-K741P** | Rev: 1.0

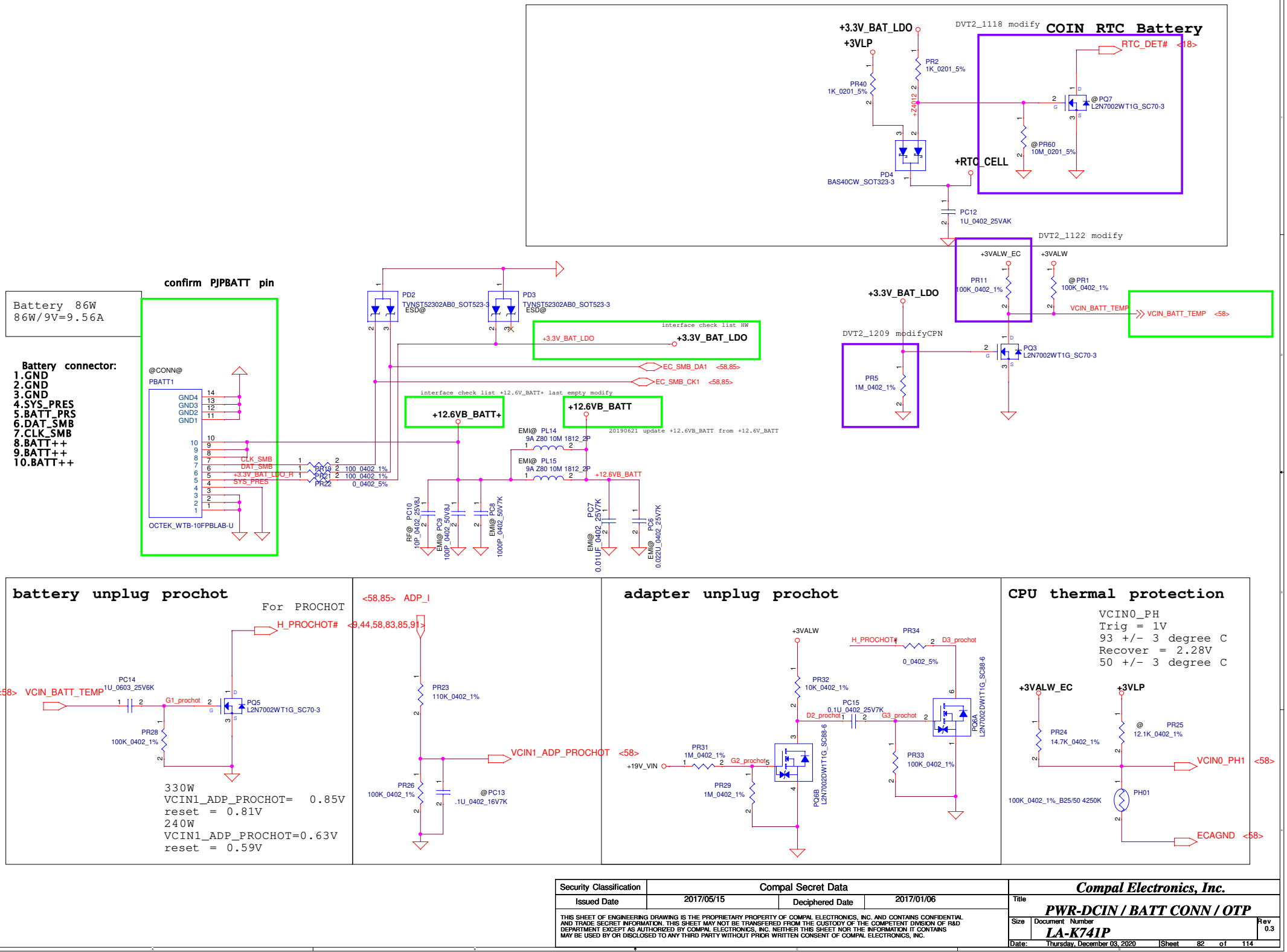
Date: Thursday, December 03, 2020 | Sheet 80 of 114

Power block



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev 0.3
	LA-K741P		
Date: Thursday, December 03, 2020	Sheet 81 of 114		



Security Classification	Compal Secret Data		
Issued Date	2017/05/15	Deciphered Date	2017/01/06

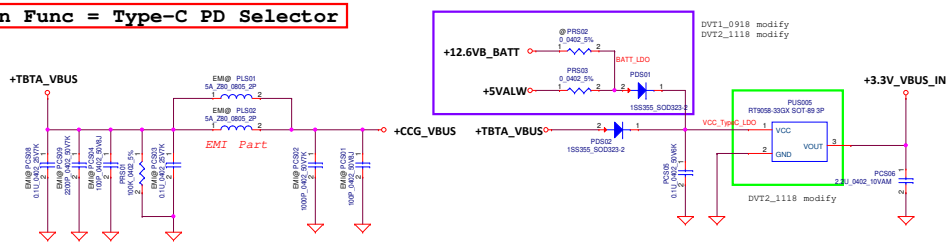
Compal Electronics, Inc.

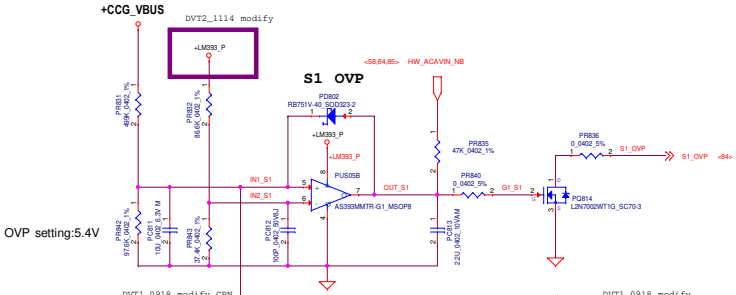
Title: PWR-DCIN / BATT CONN / OTP

Size	Document Number	Rev
	LA-K741P	0.3

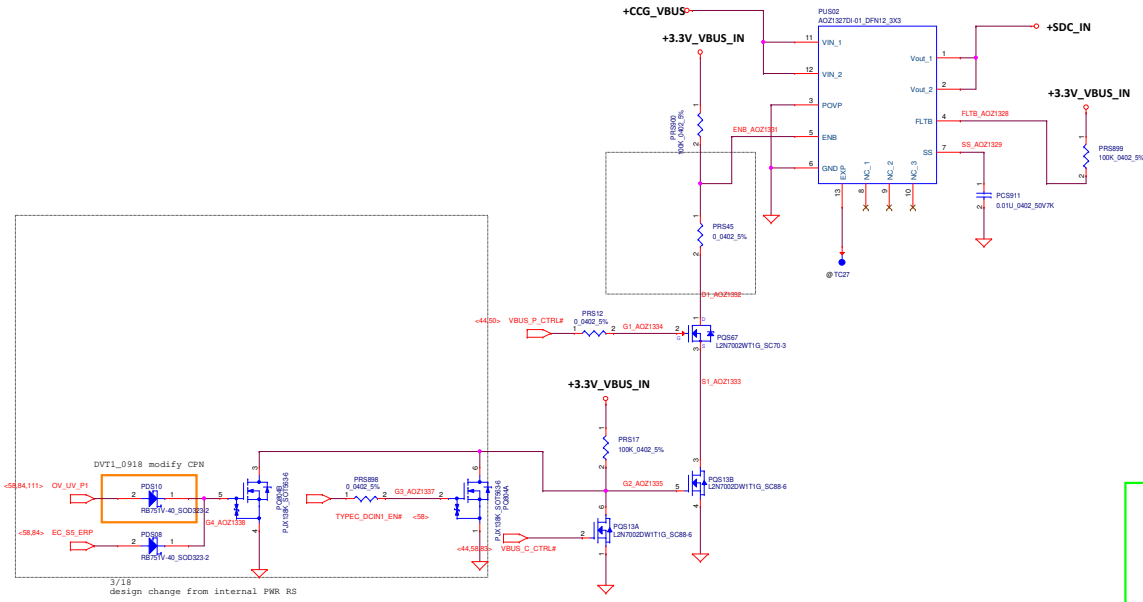
Date: Thursday, December 03, 2020 Sheet 82 of 114

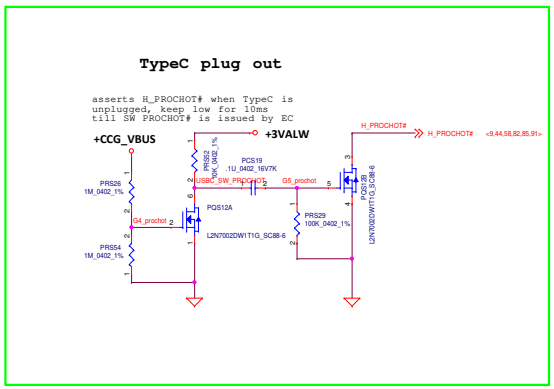
Main Func = Type-C PD Selector



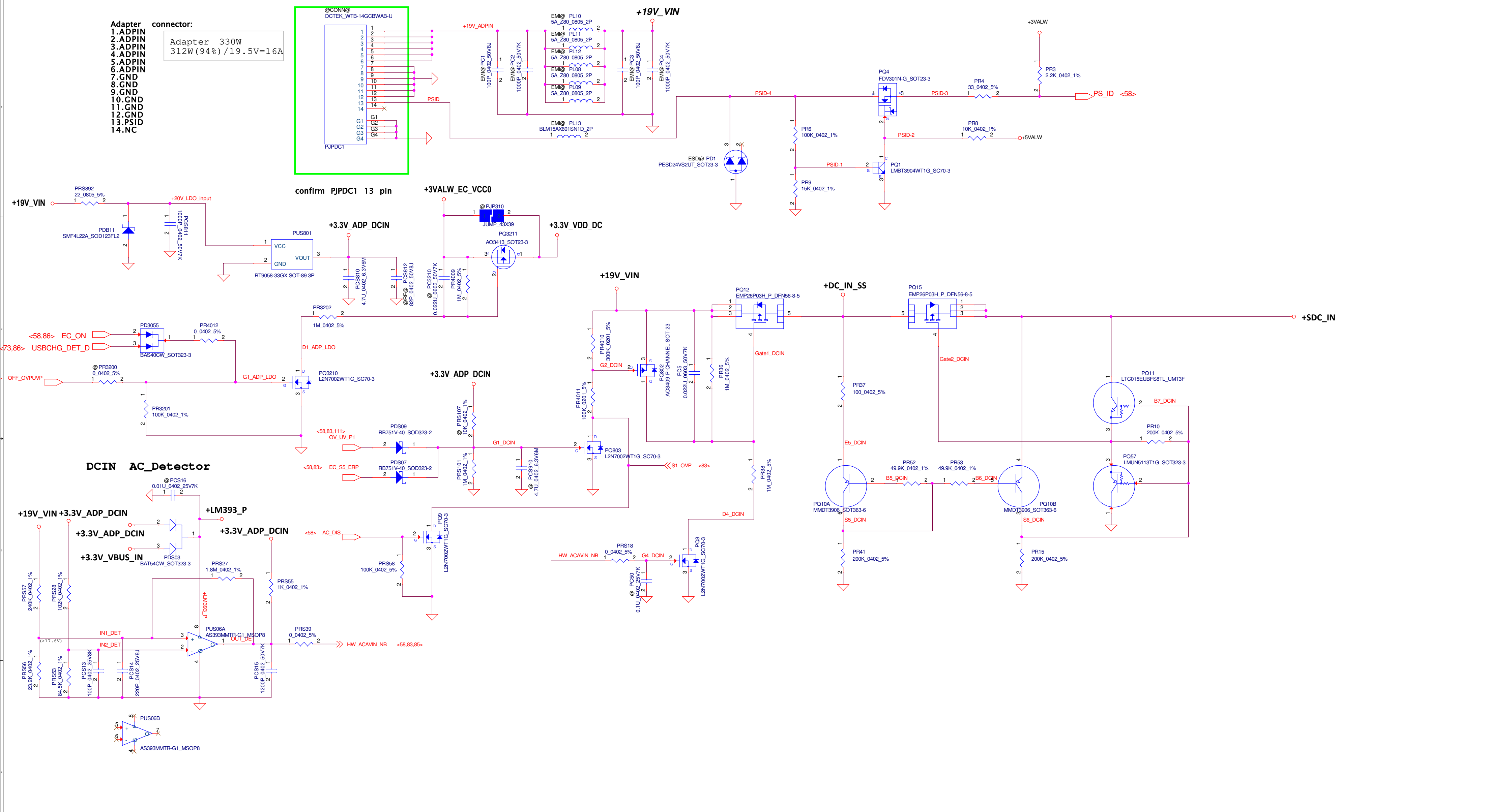


Change to AOZ1327





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: PWR Type-C PD Selector
			Size: Document Number: LA-K741P Rev: 0.3
			Date: Thursday, December 03, 2020 Sheet 83 of 114


Adapter connector:
1.ADPIN
2.ADPIN
3.ADPIN
4.ADPIN
5.ADPIN
6.ADPIN
7.GND
8.GND
9.GND
10.GND
11.GND
12.GND
13.PSID
14.NC
Adapter 330W
312W(94%)/19.5V=16A
@CONN@
OCTEK_WTB-14GCBWAB-U
PJPDC1
confirm PJPDC1 13 pin
+19V_ADPIN
PSID
+19V_VIN
EMI@ PL10 5A_Z80_0805_2P
EMI@ PL11 5A_Z80_0805_2P
EMI@ PL12 5A_Z80_0805_2P
EMI@ PL08 5A_Z80_0805_2P
EMI@ PL09 5A_Z80_0805_2P
EMI@ PL13 BLM15AX601SN1D_2P
EMI@PC1 100P_0402_50V8J
EMI@PC2 1000P_0402_50V7K
EMI@PC3 100P_0402_50V8J
EMI@PC4 1000P_0402_50V7K
+3VALW
PQ4 FDV301N-G_SOT23-3
PR4 33_0402_5%
PR3 2.2K_0402_1%
PS_ID <58>
PSID-4
PSID-3
PSID-2
PSID-1
PR8 10K_0402_1%
+5VALW
PR6 100K_0402_1%
PR9 15K_0402_1%
ESD@ PD1 PESD24VS2UT_SOT23-3
PQ1 LMBT3904WT1G_SC70-3
+19V_VIN
PRS892 22_0805_5%
+20V_LDO_input
PDB11 SMF4L22A_SOD123FL2
PCS811 1000P_0402_50V7K
PUS801
VCC
GND
VOUT
RT9058-33GX SOT-89 3P
+3.3V_ADP_DCIN
PCS810 4.7U_0402_6.3V6M
@RF@ PCS812 82P_0402_50V8J
+3VALW_EC_VCC0
@PJP310 JUMP_43X39
+3.3V_VDD_DC
PQ3211 AO3413_SOT23-3
@ PC3210 0.022U_0603_50V7K
PR4009 1M_0402_5%
PR3202 1M_0402_5%
D1_ADP_LDO
<58,86> EC_ON
<73,86> USBCHG_DET_D
PD3055 BAS40CW_SOT323-3
PR4012 0_0402_5%
OFF_OVPUVP
@PR3200 0_0402_5%
PR3201 100K_0402_1%
G1_ADP_LDO
PQ3210 L2N7002WT1G_SC70-3
+3.3V_ADP_DCIN
<58,83,111> OV_UV_P1
PDS09 RB751V-40_SOD323-2
<58,83> EC_S5_ERP
PDS07 RB751V-40_SOD323-2
@ PRS107 10K_0402_1%
PRS101 1M_0402_1%
G1_DCIN
@ PCS910 4.7U_0402_6.3V6M
PQ803 L2N7002WT1G_SC70-3
S1_OVP <83>
+19V_VIN
PR4010 300K_0201_5%
G2_DCIN
PQ802 AO3409 P-CHANNEL SOT-23
PC5 0.022U_0603_50V7K
PR36 1M_0402_5%
PR4011 100K_0201_5%
PQ12 EMP26P03H_P_DFN56-8-5
Gate1_DCIN
PR38 1M_0402_5%
D4_DCIN
+DC_IN_SS
PQ15 EMP26P03H_P_DFN56-8-5
Gate2_DCIN
+SDC_IN
PR37 100_0402_5%
E5_DCIN
PQ11 LTC015EUBFS8TL_UMT3F
B7_DCIN
PR10 200K_0402_5%
PR52 49.9K_0402_1%
PR53 49.9K_0402_1%
B5_DCIN
B6_DCIN
PQ57 LMUN5113T1G_SOT323-3
PQ10A MMDT3906_SOT363-6
PQ10B MMDT3906_SOT363-6
S5_DCIN
S6_DCIN
PR41 200K_0402_5%
PR15 200K_0402_5%
HW_ACAVIN_NB
PRS18 0_0402_5%
G4_DCIN
@ PC50 0.1U_0402_25V7K
PQ8 L2N7002WT1G_SC70-3
DCIN AC_Detector
@PCS16 0.01U_0402_25V7K
+19V_VIN
+3.3V_ADP_DCIN
+LM393_P
+3.3V_ADP_DCIN
+3.3V_VBUS_IN
PDS03 BAT54CW_SOT323-3
+3.3V_ADP_DCIN
<58> AC_DIS
PQ9 L2N7002WT1G_SC70-3
PRS58 100K_0402_5%
PRS27 1.8M_0402_1%
PRS55 1K_0402_1%
PRS57 240K_0402_1%
PRS28 102K_0402_1%
IN1_DET
IN2_DET
(>17.6V)
PUS06A AS393MMTR-G1_MSOP8
OUT_DET
PRS39 0_0402_5%
HW_ACAVIN_NB <58,83,85>
PRS56 23.2K_0402_1%
PRS53 84.5K_0402_1%
PCS13 100P_0402_25V8K
PCS14 220P_0402_25V8J
PCS15 1200P_0402_50V7K
PUS06B
AS393MMTR-G1_MSOP8

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title: PWR_DCIN CONN

Size | Document Number | Rev 0.3

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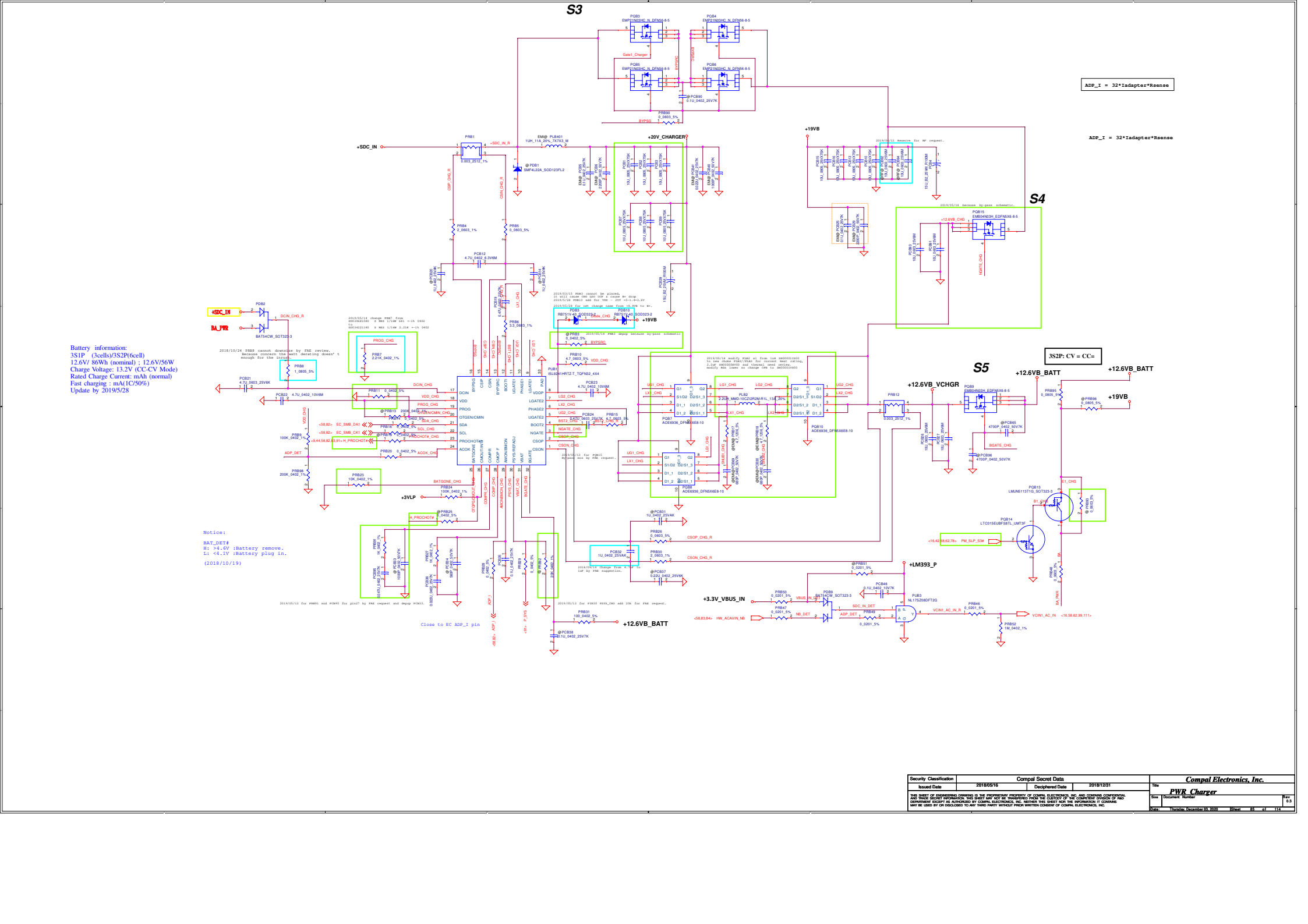
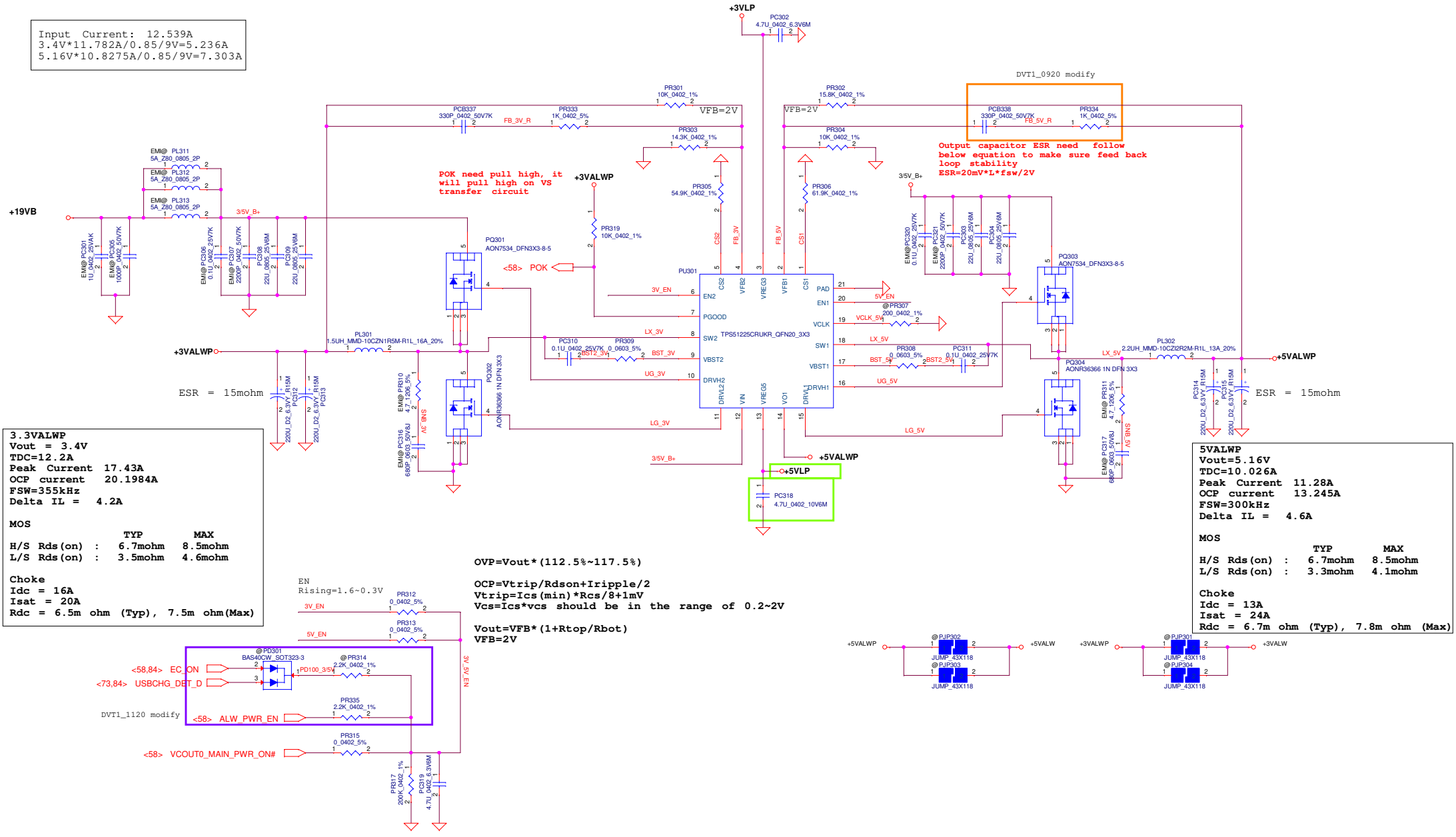

S3
S4
S5
ADP_I = 32*Iadapter*Rsense
3S2P: CV = CC=
+20V_CHARGER
+SDC_IN
+19VB
+12.6VB_BATT
+12.6VB_VCHGR
+3.3V_VBUS_IN
+3VLP
+LM393_P
Battery information:
3S1P (3cells)/3S2P(6cell)
12.6V/ 86Wh (nominal) ; 12.6V/56W
Charge Voltage: 13.2V (CC-CV Mode)
Rated Charge Current: mAh (normal)
Fast charging : mA(1C/50%)
Update by 2019/5/28
Notice:
BAT_DET#
H: >4.6V :Battery remove.
L: <4.1V :Battery plug in.
(2018/10/19)
Close to EC ADP_I pin
Security Classification
Compal Secret Data
Issued Date
2018/05/16
Deciphered Date
2018/12/31
Compal Electronics, Inc.
PWR_Charger
Size
Document Number
Rev
0.3
Date:
Thursday, December 03, 2020
Sheet
85
of
114

Input Current: 12.539A
3.4V*11.782A/0.85/9V=5.236A
5.16V*10.8275A/0.85/9V=7.303A

DVT1_0920 modify

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit



3.3VALWP
Vout = 3.4V
TDC=12.2A
Peak Current 17.43A
OCP current 20.1984A
FSW=355kHz
Delta IL = 4.2A

MOS

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	3.5mohm	4.6mohm

Choke
Idc = 16A
Isat = 20A
Rdc = 6.5m ohm (Typ), 7.5m ohm(Max)

5VALWP
Vout=5.16V
TDC=10.026A
Peak Current 11.28A
OCP current 13.245A
FSW=300kHz
Delta IL = 4.6A

MOS

	TYP	MAX
H/S Rds(on) :	6.7mohm	8.5mohm
L/S Rds(on) :	3.3mohm	4.1mohm

Choke
Idc = 13A
Isat = 24A
Rdc = 6.7m ohm (Typ), 7.8m ohm (Max)

OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

Security Classification	Compal Secret Data		
Issued Date	2018/05/16	Deciphered Date	2018/12/31

Compal Electronics, Inc.

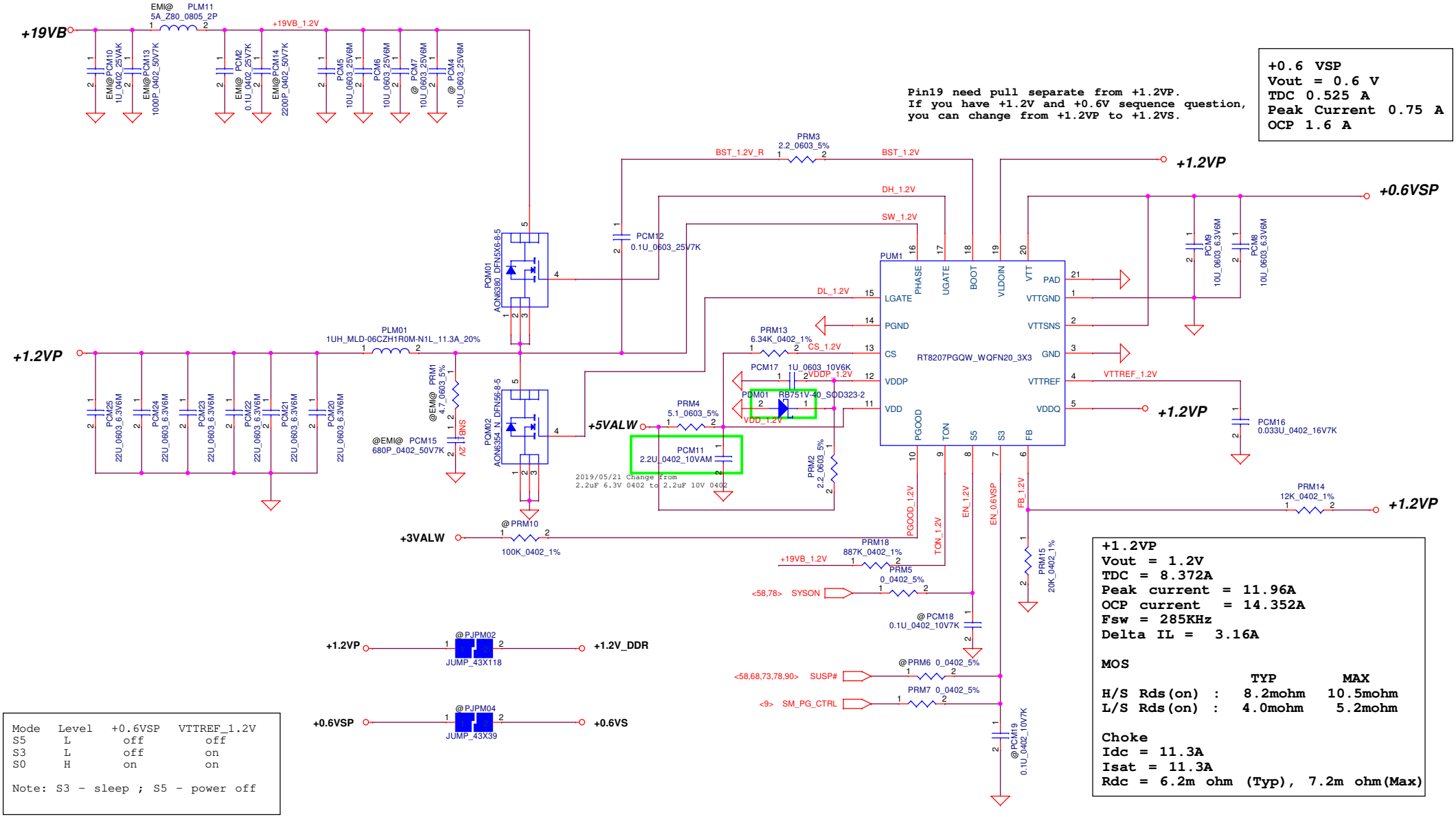
Title: **PWR_+3.3VALWP/+5VALWP**

Size	Document Number	Rev
		0.3

Date: Thursday, December 03, 2020 Sheet 86 of 114

Input Current: 1.047A

1.2V*6.68A/0.85/9V=1.047A



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Compal Electronics, Inc.

Title: PWR_1.2VP/0.6VSP

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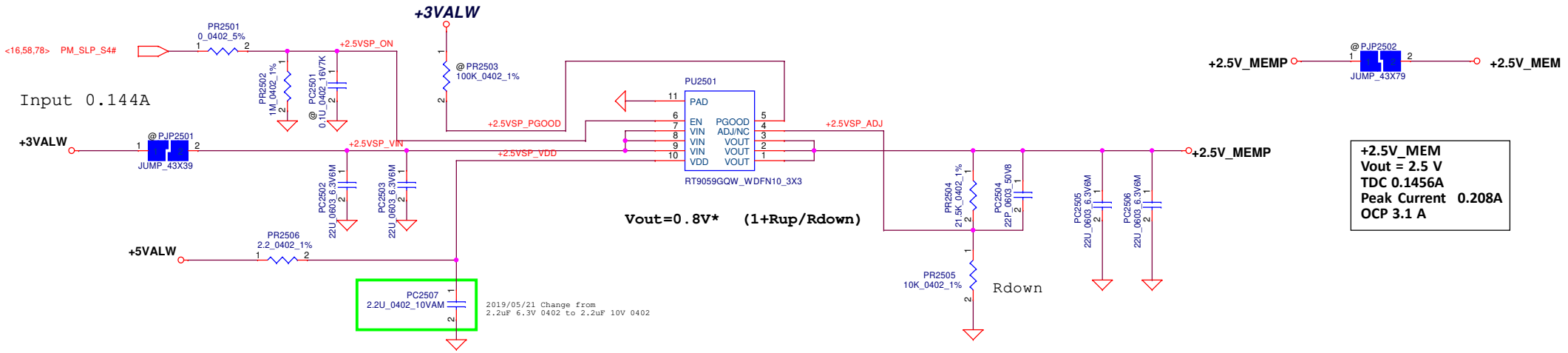
Input Peak Current:0.153A
25*0.208/3.4=0.153A

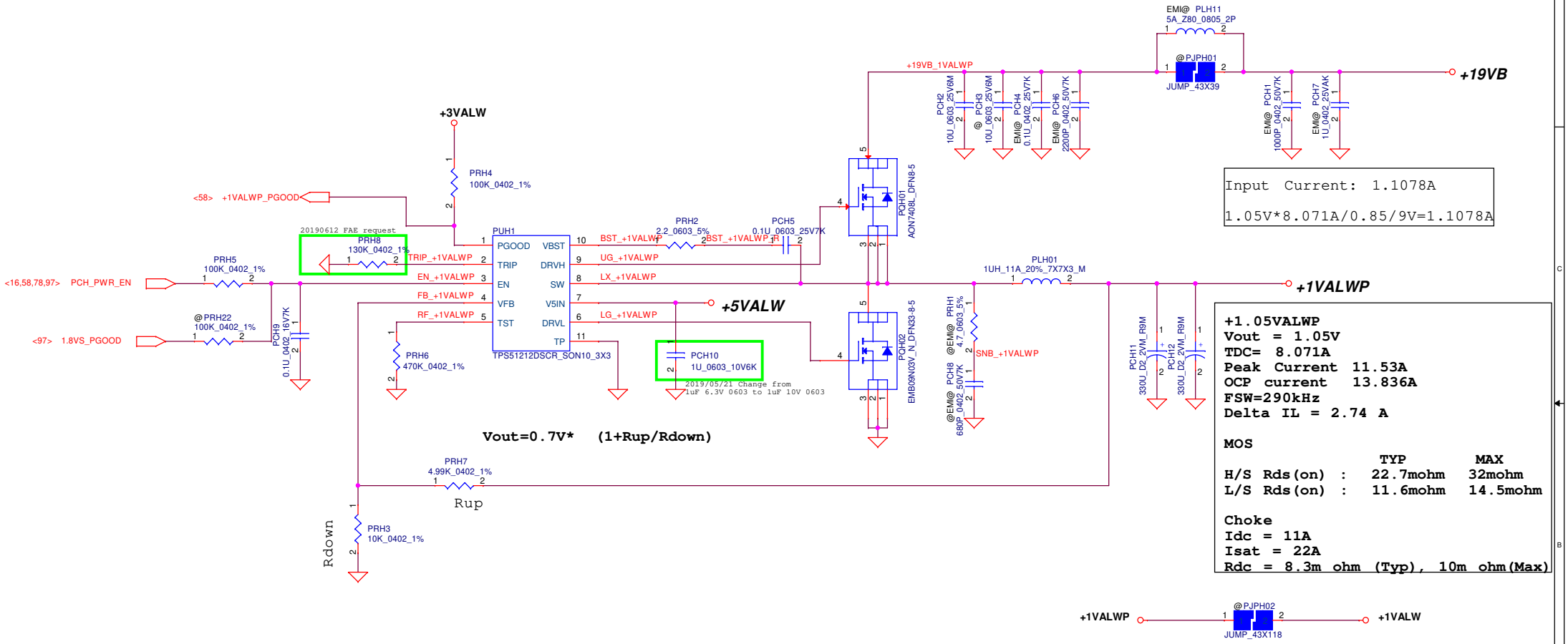


Compal Electronics, Inc.

Title: PWR_+2.5V_MEM

Size | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 88 of 114



Security Classification	Compal Secret Data		
Issued Date	2018/05/16	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: PWR_+1VALWP			
Size	Document Number: LA-K741P		Rev: 0.3
Date: Thursday, December 03, 2020	Sheet 89 of 114		

+VCCIO
Vout = 0.954V
TDC = 4.48A
Peak current = 6.4A
OCP current = 8A
Fsw = 500KHz
Delta IL = 1.45A

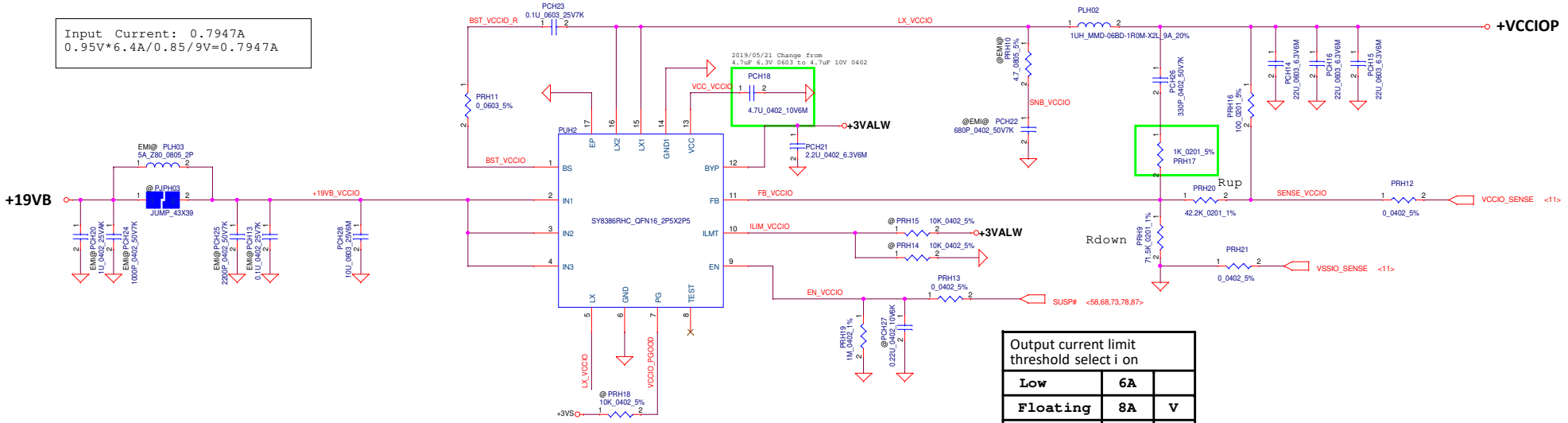
Converter

	TYP
H/S Rds(on) :	38mohm
L/S Rds(on) :	19mohm

Choke
Idc = 9A
Isat = 16A
Rdc = 11.2m ohm (Typ), 13.5m ohm(Max)

+VCCIOP — @ PJPH04 JUMP_43X118 — +VCCIO

Input Current: 0.7947A
0.95V*6.4A/0.85/9V=0.7947A



Output current limit threshold select i on		
Low	6A	
Floating	8A	V
High	10A	

Compal Electronics, Inc.

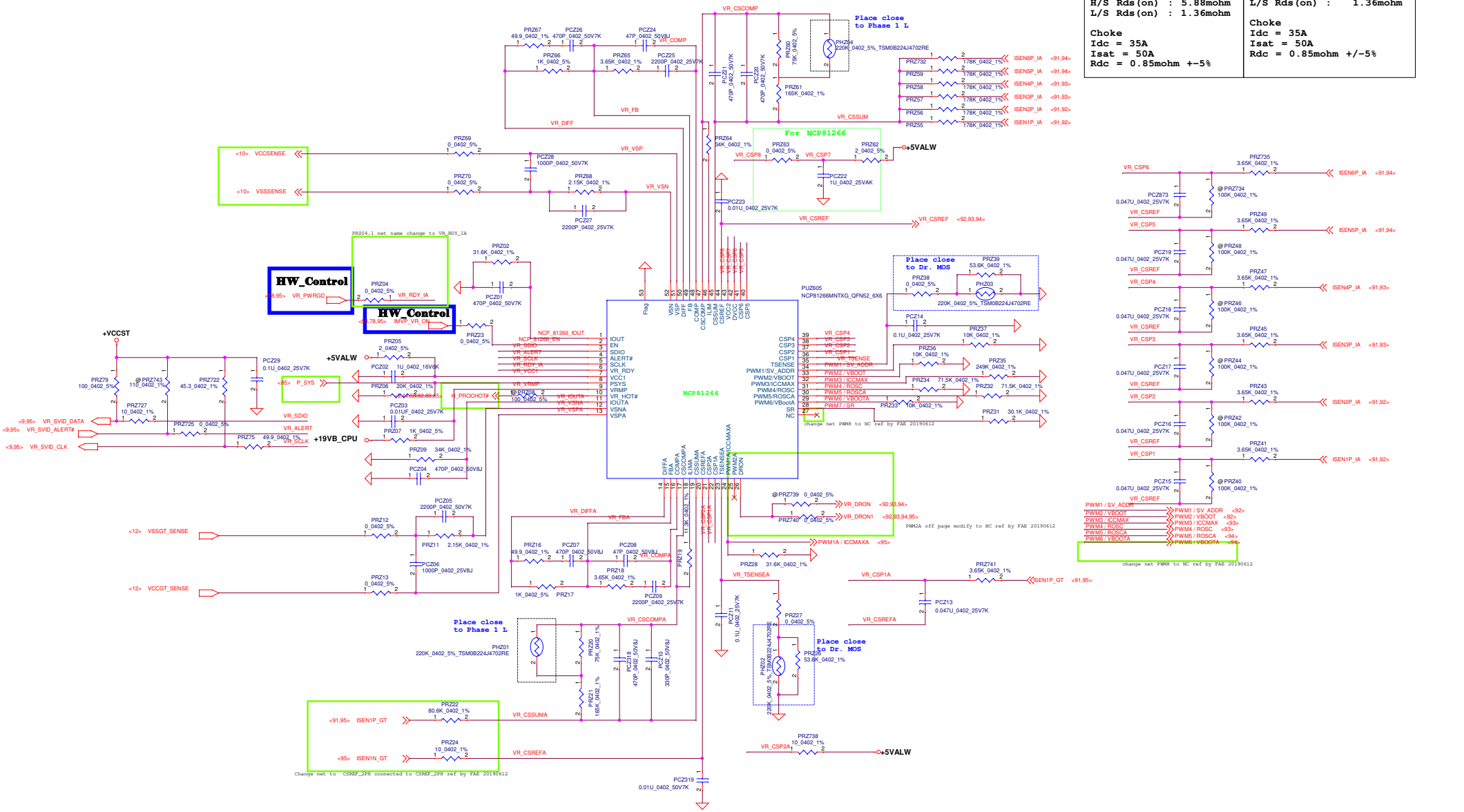
Title: PWR_+VCCIO

Size | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 90 of 114

Main Func = VCORE

+VCC_CORE	+VCCGT
TDC = 146A (I_PL2)	TDC = 25A (I_PL2)
Peak current = 254A	Peak current = 32A
OCP current = 322A	OCP current = 38.4A
Fsw = 540KHz	Fsw = 540KHz
Delta IL = 12.27A	Delta IL = 12.27A
DC Load line : 1.1m V/A	
DRMOS	DRMOS
H/S Rds(on) : 5.88mohm	H/S Rds(on) : 5.88mohm
L/S Rds(on) : 1.36mohm	L/S Rds(on) : 1.36mohm
Choke	Choke
Idc = 35A	Idc = 35A
Isat = 50A	Isat = 50A
Rdc = 0.85mohm +-5%	Rdc = 0.85mohm +/-5%



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCORE_NCP81266

Size: | Document Number: LA-K741P | Rev: 3

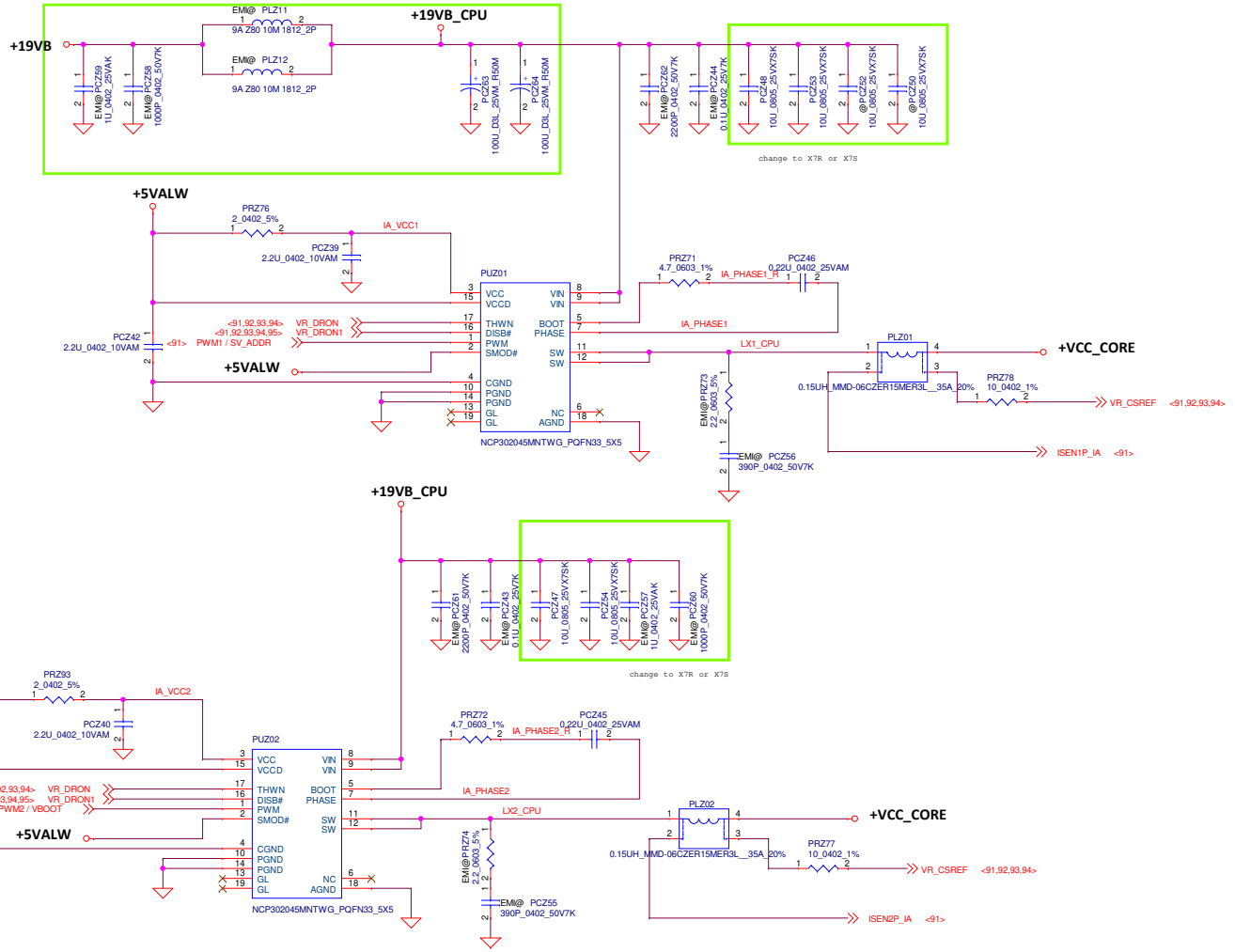
Date: Thursday, December 03, 2020 | Sheet 91 of 114

Main Func = CORE_Phase1&2

+VCC_CORE
TDC = 146A (I_PL2)
Peak current = 254A
OCP current = 322A
Fsw = 540KHz
Delta IL = 12.27A
DC Load line : 1.1m V/A

DRMOS
H/S Rds(on) : 5.88mohm
L/S Rds(on) : 1.36mohm

Choke
Idc = 35A
Isat = 50A
Rdc = 0.85mohm +-5%



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCC_CORE_Phase1&2

Size: | Document Number: LA-K741P | Rev: 0.3

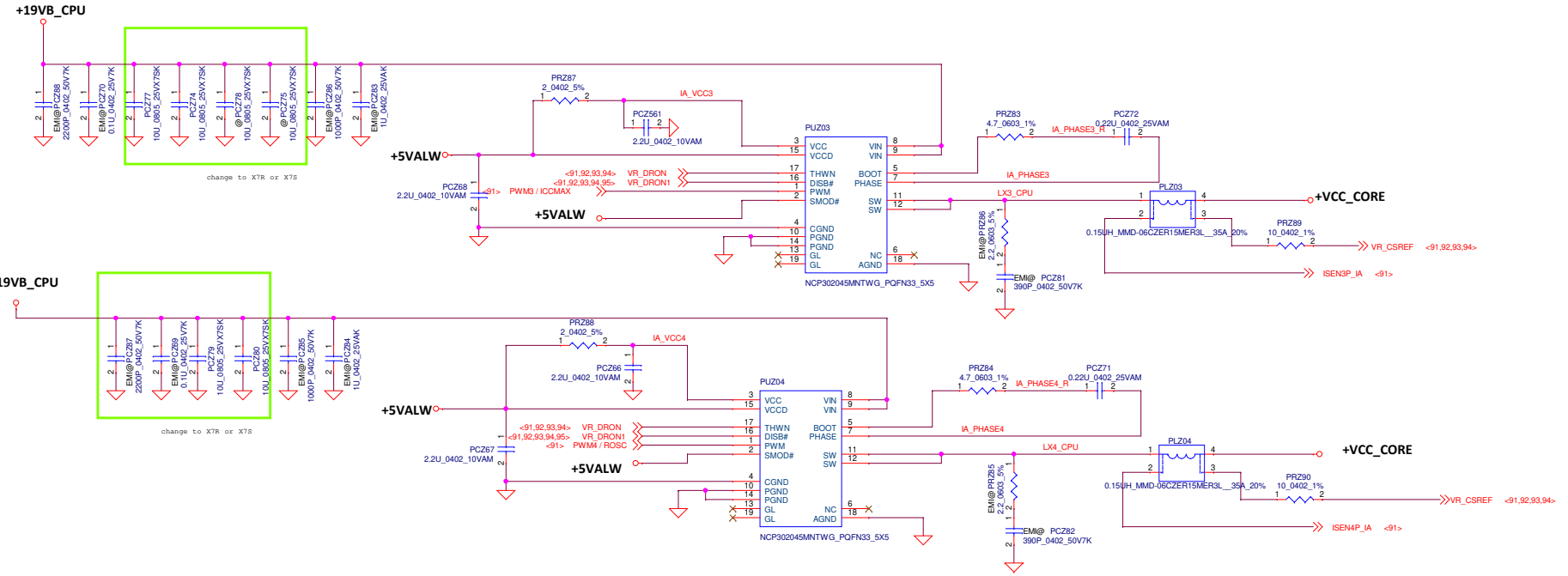
Date: Thursday, December 03, 2020 | Sheet 92 of 114

Main Func = CORE_Phase3&4

+VCC_CORE
TDC = 146A (I_PL2)
Peak current = 254A
OCP current = 322A
Fsw = 540KHz
Delta IL = 12.27A
DC Load line : 1.1m V/A

DRMOS
H/S Rds(on) : 5.88mohm
L/S Rds(on) : 1.36mohm

Choke
Idc = 35A
Isat = 50A
Rdc = 0.85mohm +-5%



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: +VCC_CORE_Phase3&4

Size	Document Number	Rev
	LA-K741P	0.3

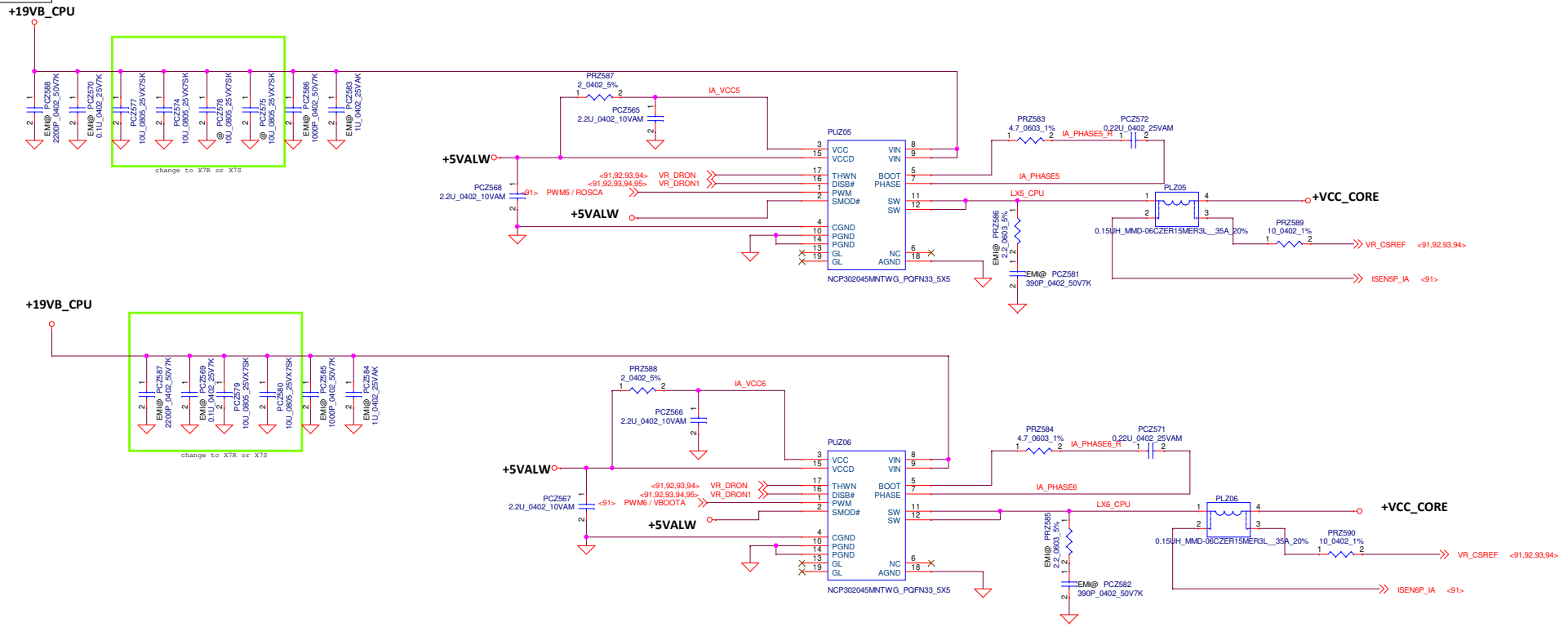
Date: Thursday, December 03, 2020 | Sheet 93 of 114

Main Func = CORE_Phase5&6

+VCC_CORE
TDC = 146A (I_PL2)
Peak current = 254A
OCP current = 322A
Fsw = 540KHz
Delta IL = 12.27A
DC Load line : 1.1m V/A

DRMOS
H/S Rds(on) : 5.88mohm
L/S Rds(on) : 1.36mohm

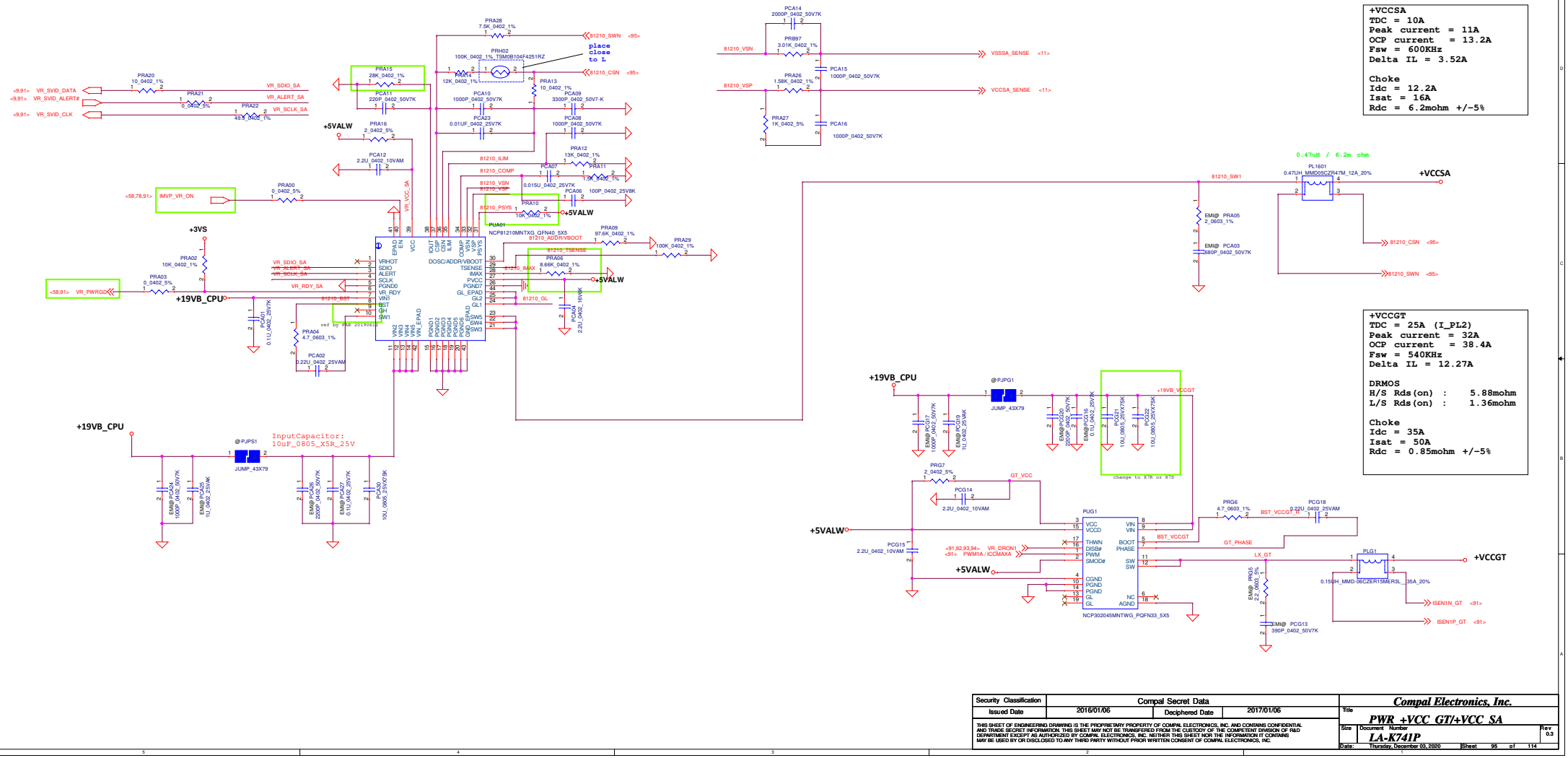
Choke
Idc = 35A
Isat = 50A
Rdc = 0.85mohm +-5%



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title: +VCC_CORE_Phase5&6			
Size	Document Number: LA-K741P		Rev: 0.3
Date: Thursday, December 03, 2020	Sheet 94 of 114		

Main Func =+VCCSA



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.	
Title	PWR +VCC_GT/+VCC_SA
Size	Document Number: LA-K741P
Rev	0.3
Date:	Thursday, December 03, 2020
Sheet	95 of 114

+VCC_CORE

delete 470uF_D2 x1 add 22uF x22
20190618

+VCC_CORE
470uF_D2 x5
22uF 0603 x26 + Reserve x22
10uF 0805 x35
1uF 0201 x48

+VCCGT

+VCCGT
470uF_D2 x1
22uF 0603 x21

+VCCSA

+VCCSA
220uF_D7 x1
22uF 0805 x14
10uF 0805 x1

X7S Change to X7T_Part number applying

X7S Change to X7T_Part number applying

+VCC_CORE

delete 470uF_D2 x1 add 22uF x22
20190618

+VCCGT

X7S Change to X7T_Part number applying

Security Classification	Compal Secret Data		
Issued Date	2018/05/16	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: PWR_CPU DECOUPLING

Size: | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 96 of 114

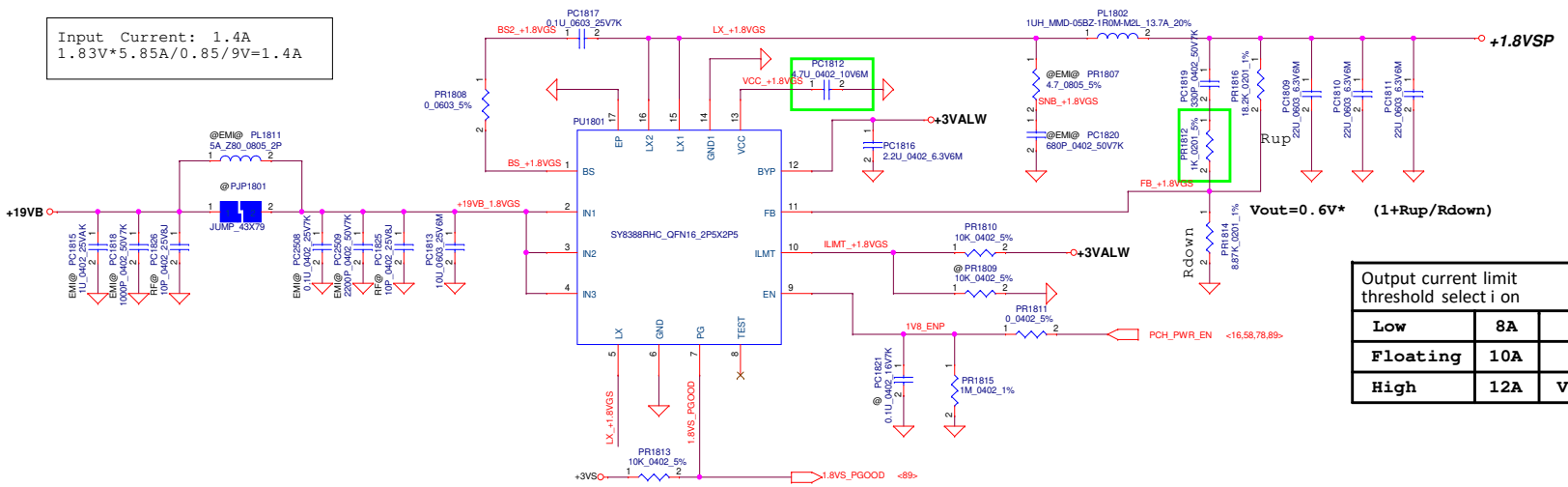
20200903 Follow SP-09948-001_v04
Edp-c 3.5A -> 2.9A
TDC=2.9+0.330*5= 4.55A
Edp-p 4.4A->5.9A
Peak current=5.9+0.330*5=7.55A

+1.8VSP
Vout = 1.83V
TDC 4.55A
Peak Current 7.55A
OCP current 12A
FSW=500kHz
Delta IL = 3.27A

Converter
TYP
H/S Rds(on) : 22mohm
L/S Rds(on) : 11mohm

Choke
Idc = 7A
Isat = 13.7A
Rdc = 18.9m ohm (Typ), 20m ohm(Max)

Input Current: 1.4A
1.83V*5.85A/0.85/9V=1.4A



Output current limit threshold select i on		
Low	8A	
Floating	10A	
High	12A	V

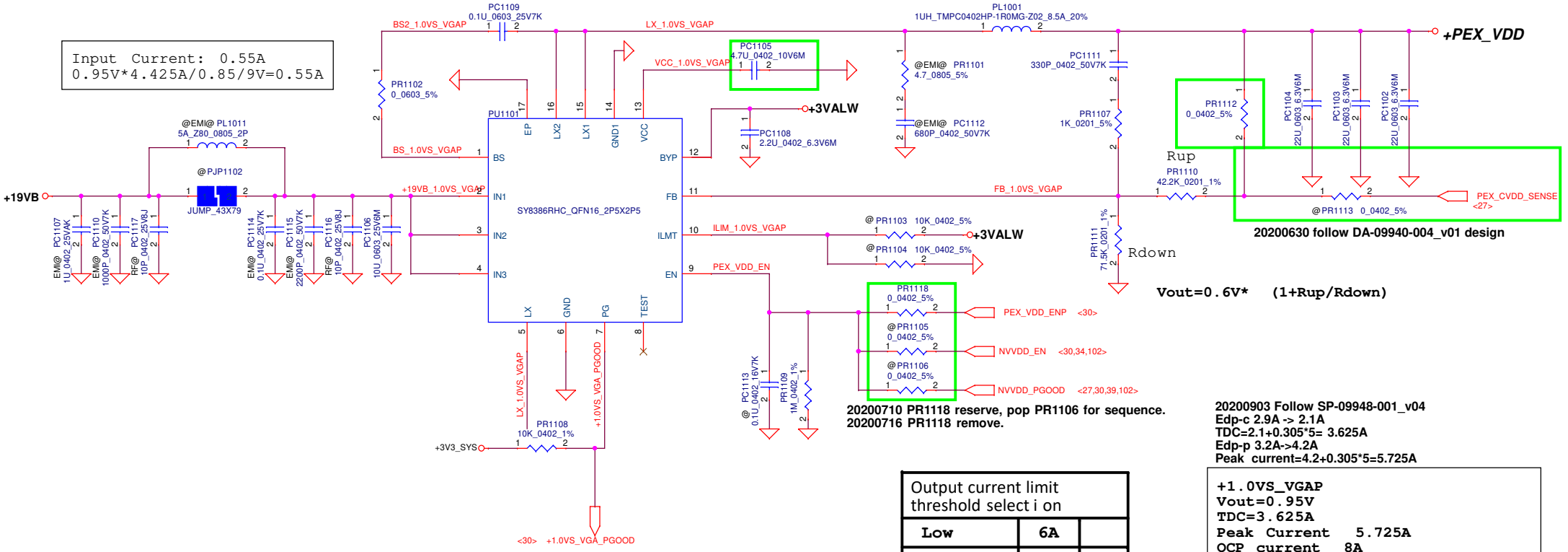
Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: PWR +1.8VSP

Size | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 97 of 114



20200903 Follow SP-09948-001_v04
Edp-c 2.9A -> 2.1A
TDC=2.1+0.305*5= 3.625A
Edp-p 3.2A->4.2A
Peak current=4.2+0.305*5=5.725A

Output current limit threshold select i on		
Low	6A	
Floating	8A	V
High	10A	

+1.0VS_VGAP
Vout=0.95V
TDC=3.625A
Peak Current 5.725A
OCP current 8A
FSW=500kHz
Delta IL = 1.8A

Converter

	TYP
H/S Rds(on) :	38mohm
L/S Rds(on) :	19mohm

Choke
Idc = 5A
Isat = 8.5A
Rdc = 22m ohm (Typ), 27m ohm(Max)

Security Classification	Compal Secret Data		
Issued Date	2018/08/07	Deciphered Date	2019/08/07

Compal Electronics, Inc.

Title: PWR_+1.0VS_VGAP

Size | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 98 of 114

Reserve

Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: *PWR_UP9530 Controller*

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 99 of 114

Reserve

Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: ***PWR_2 stages***

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 100 of 114

Reserve

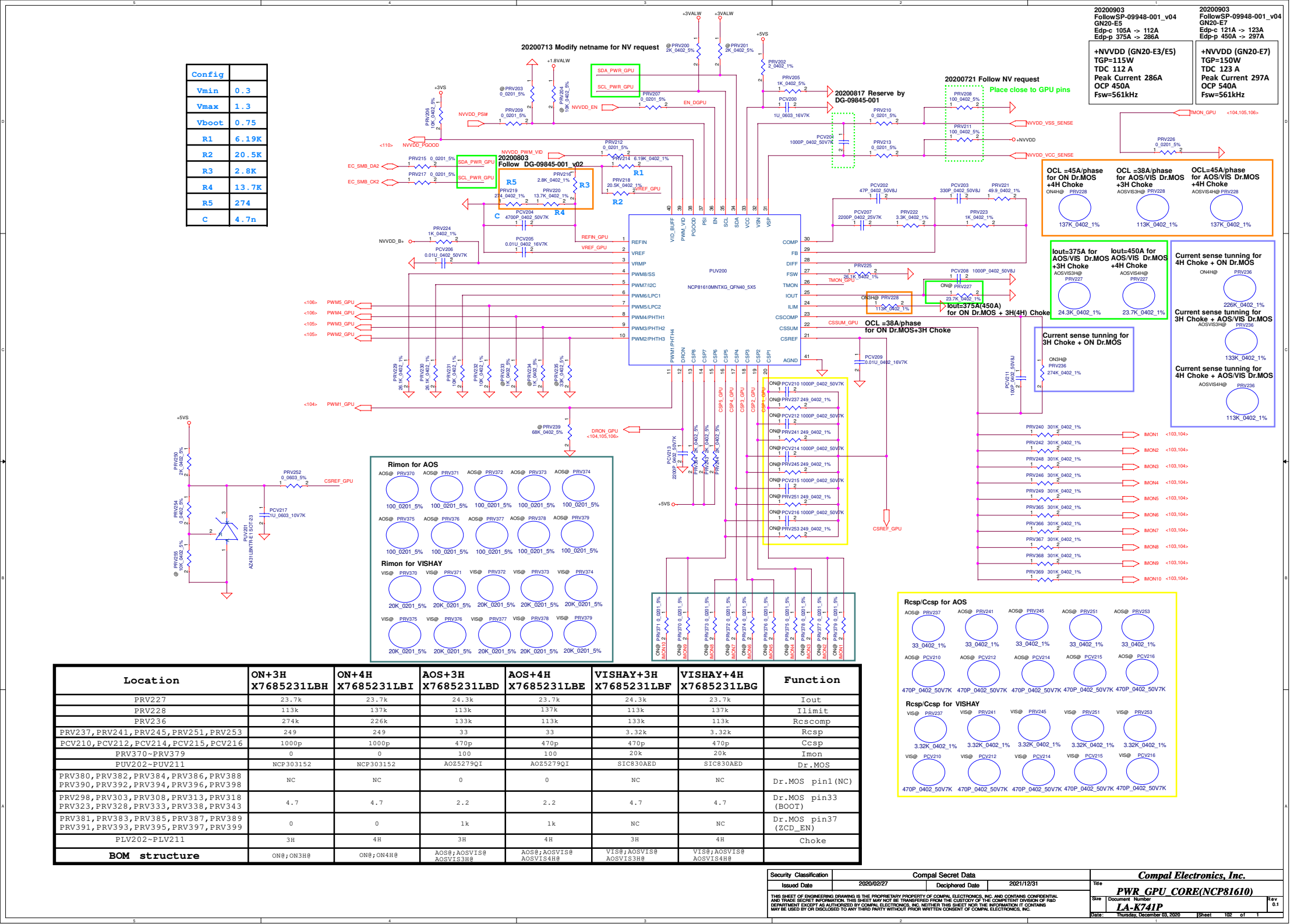
Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: *PWR_2 stages*

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 101 of 114



Location	ON+3H X7685231LBH	ON+4H X7685231LBI	AOS+3H X7685231LBD	AOS+4H X7685231LBE	VISHAY+3H X7685231LBF	VISHAY+4H X7685231LBG	Function
PRV227	23.7k	23.7k	24.3k	23.7k	24.3k	23.7k	Iout
PRV228	113k	137k	113k	137k	113k	137k	Ilimit
PRV236	274k	226k	133k	113k	133k	113k	Rcscomp
PRV237,PRV241,PRV245,PRV251,PRV253	249	249	33	33	3.32k	3.32k	Rcsp
PCV210,PCV212,PCV214,PCV215,PCV216	1000p	1000p	470p	470p	470p	470p	Ccsp
PRV370~PRV379	0	0	100	100	20k	20k	Imon
PUV202~PUV211	NCP303152	NCP303152	AOZ5279QI	AOZ5279QI	SIC830AED	SIC830AED	Dr.MOS
PRV380,PRV382,PRV384,PRV386,PRV388 PRV390,PRV392,PRV394,PRV396,PRV398	NC	NC	0	0	NC	NC	Dr.MOS pin1(NC)
PRV298,PRV303,PRV308,PRV313,PRV318 PRV323,PRV328,PRV333,PRV338,PRV343	4.7	4.7	2.2	2.2	4.7	4.7	Dr.MOS pin33 (BOOT)
PRV381,PRV383,PRV385,PRV387,PRV389 PRV391,PRV393,PRV395,PRV397,PRV399	0	0	1k	1k	NC	NC	Dr.MOS pin37 (ZCD_EN)
PLV202~PLV211	3H	4H	3H	4H	3H	4H	Choke
BOM structure	ON@;ON3H@	ON@;ON4H@	AOS@;AOSVIS@ AOSVIS3H@	AOS@;AOSVIS@ AOSVIS4H@	VIS@;AOSVIS@ AOSVIS3H@	VIS@;AOSVIS@ AOSVIS4H@	

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_GPU_CORE(NCP81610)

Size: | Document Number: LA-K741P | Rev: 0.1

Date: Thursday, December 03, 2020 | Sheet 102 of 1

Input Current (Total) :
GN20-E7 (150W)/19.5V=7.69A

20200622 follow PGM-09939-001_v01 design

+NVVDD(GN20-E3/E5)	+NVVDD (GN20-E7)
TGP=115W	TGP=150W
TDC 112 A	TDC 123 A
Peak Current 286A	Peak Current 297A
OCP 450A	OCP 540A
Fsw=561kHz	Fsw=561kHz
Delta IL = 9.66A	Delta IL = 9.66A
DRMOS	DRMOS
H/S Rds(on) : 4.44mohm	H/S Rds(on) : 4.44mohm
L/S Rds(on) : 1.44mohm	L/S Rds(on) : 1.44mohm
Choke	Choke
Idc = 37A	Idc = 36A
Isat = 45A	Isat = 60A
Rdc = 0.9mohm +-5%	Rdc = 0.67mohm +-5%

Rboot for AOS	Rboot for VISHAY
AOS@ PRV298 2.2_0603_1%	VIS@ PRV298 4.7_0603_1%
AOS@ PRV303 2.2_0603_1%	VIS@ PRV303 4.7_0603_1%

ZCD disable
AOS@ PRV381 1K_0402_5%
AOS@ PRV383 1K_0402_5%

ON NCP302052	AOS Dr.MOS	VISHAY Dr.MOS
ON52@ PUV202 NCP303152MNTWG	AOS@ PUV202 AOZ5279QI	VIS@ PUV202 SIC830AED
ON52@ PUV203 NCP303152MNTWG	AOS@ PUV203 AOZ5279QI	VIS@ PUV203 SIC830AED

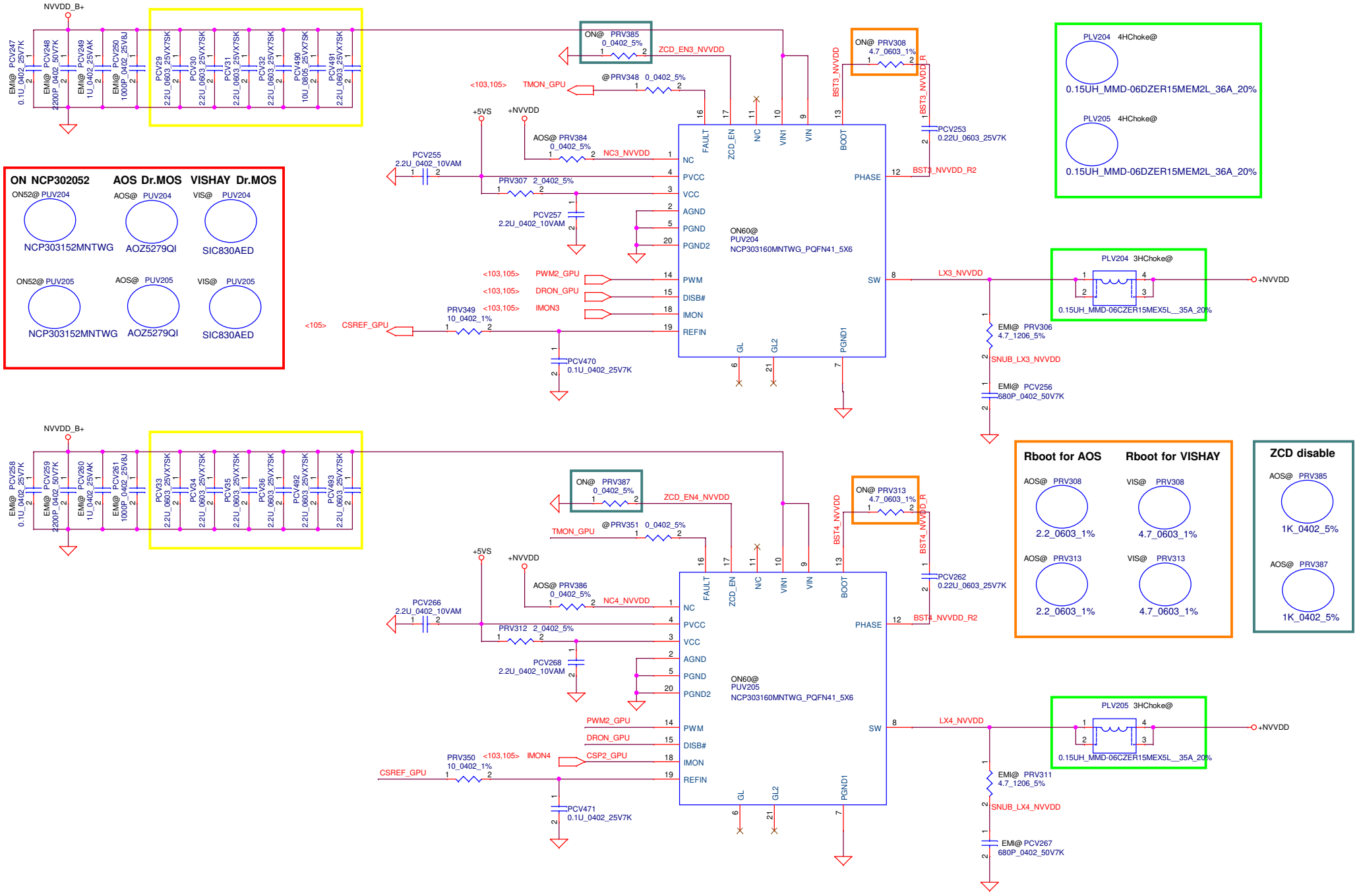
Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: PWR_+NVVDD_Phase1&2

Size: | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 103 of 114



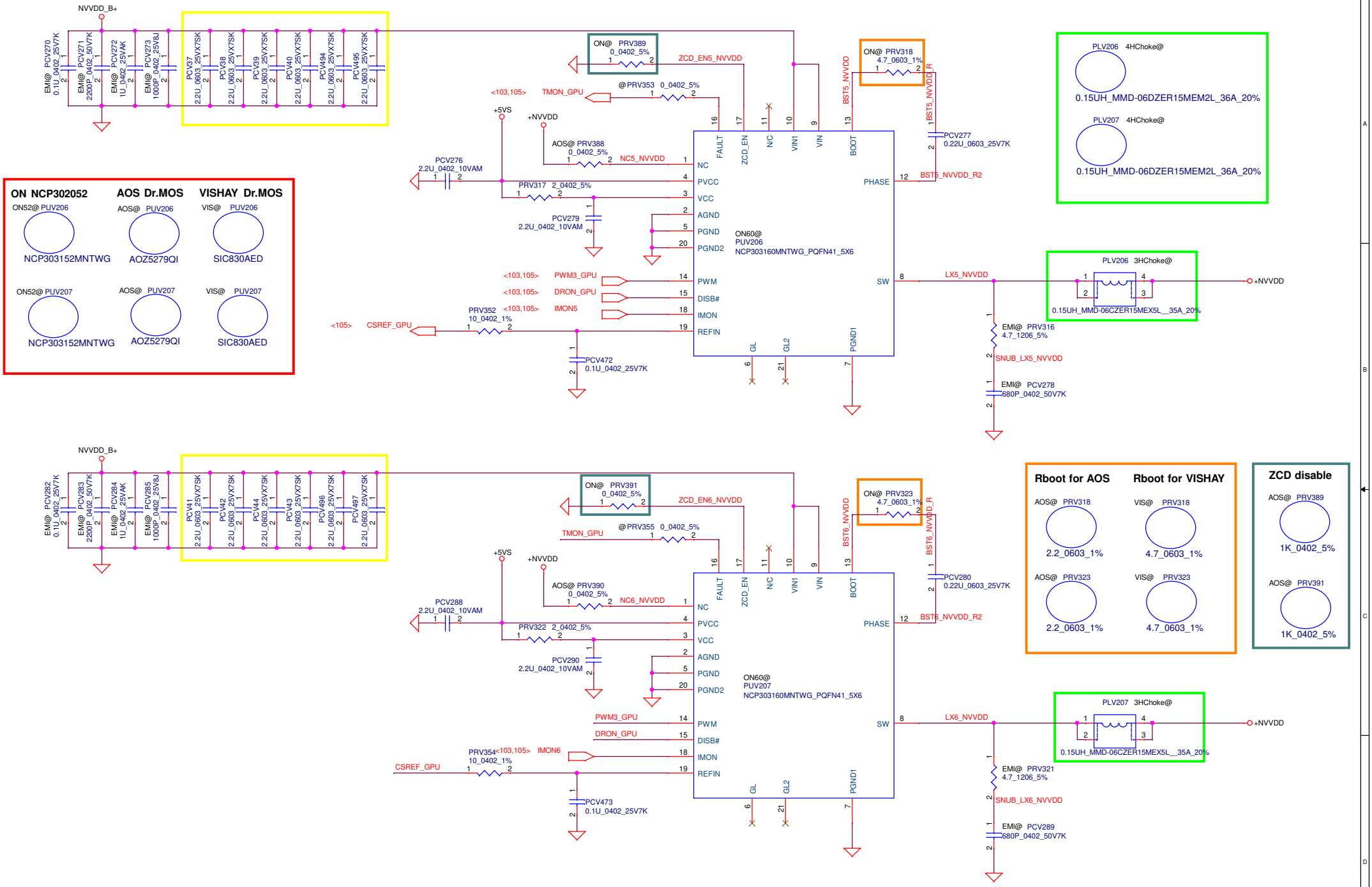
Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: **PWR_+NVVDD_Phase3&4**

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 104 of 114



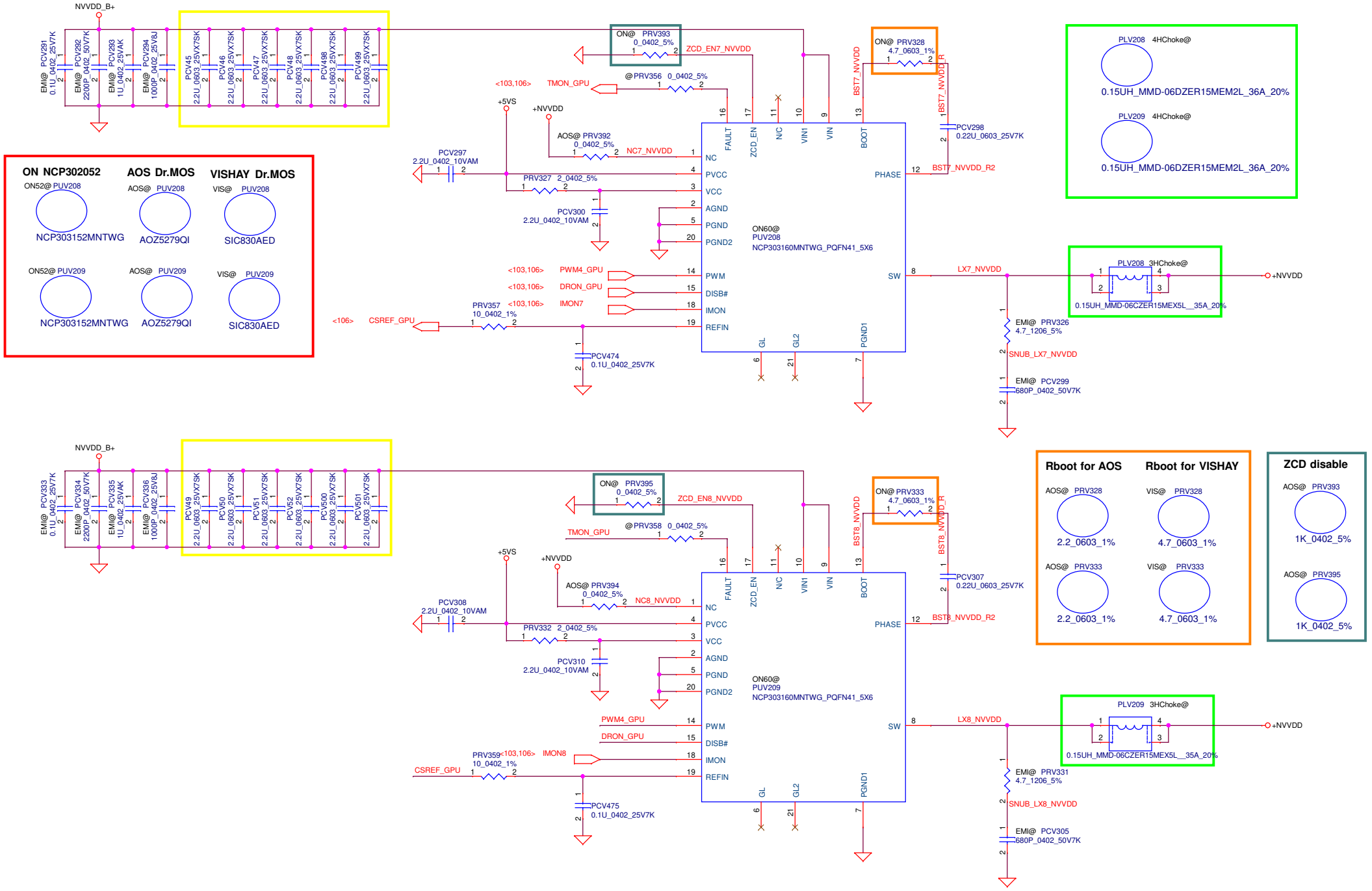
Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: **PWR_+NVVDD_Phase5&6**

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 105 of 114



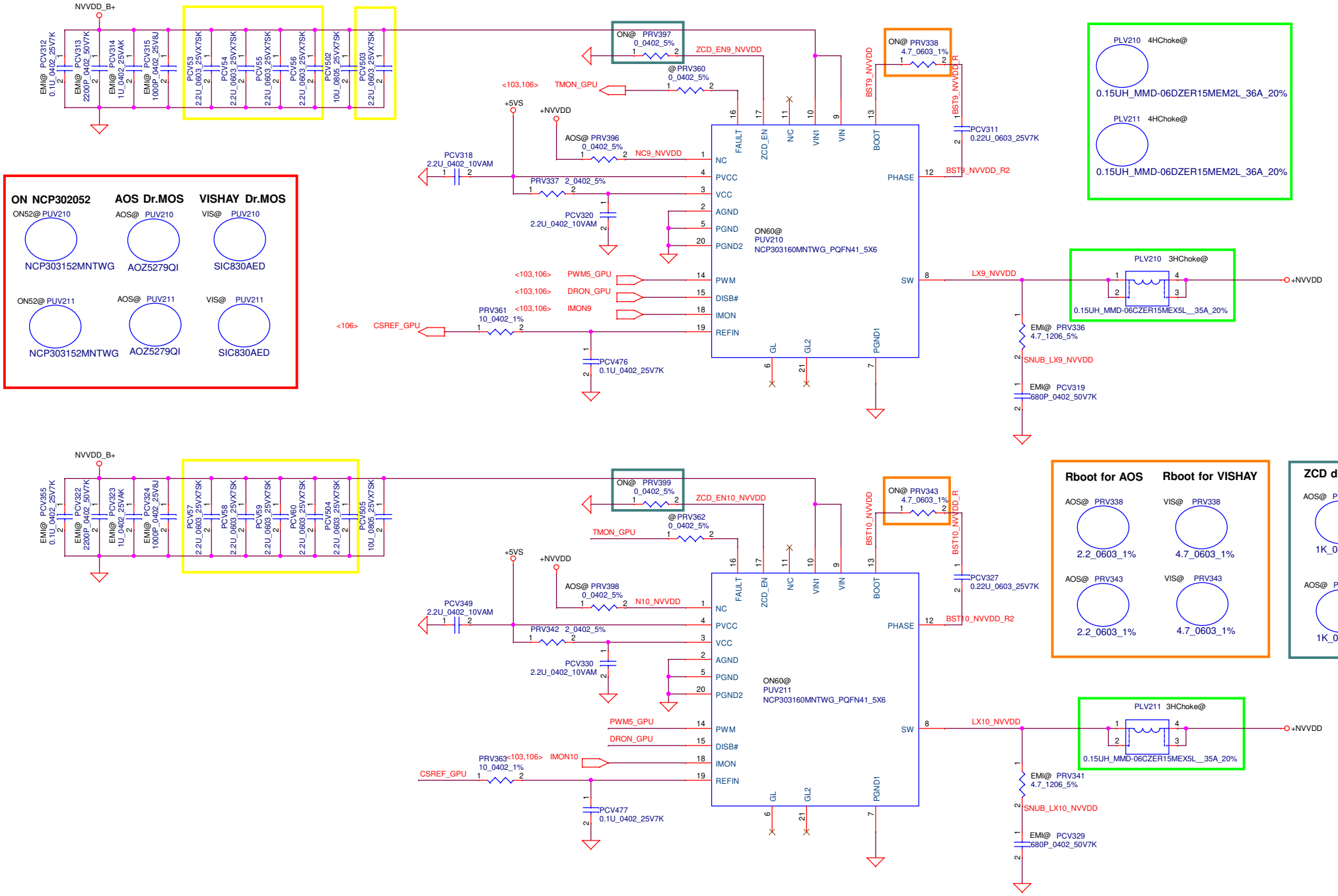
Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: **PWR_+NVVDD_Phase7&8**

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 106 of 114



Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: **PWR_+NVVDD_Phase9&10**

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 | Sheet 107 of 114

Input Current (Total) :
1.35V*40A/0.85/9V=7.06A
1.35V*26A/0.85/9V=6.88A
1.35V*20A/0.85/9V=3.53A

OCP setting for 4H Choke
4HChoke@ PRW24
48.7K_0402_1%
4HChoke@ PRW28
75K_0402_1%

NVDIA DVS BOM Table			
		PRW30	PRW31
V	1.35V~1.25V	21kΩ	82.5kΩ
	1.35V~1.2V	21kΩ	52.3kΩ

1.25V@ PRW31
82.5K_0402_1%
1.2V@ PRW31
52.3K_0402_1%

20200716
Add&reserve for NV request

Current sense tunning for 3H Choke

Current sense tunning for 4H Choke
4HChoke@ PRW2
3.6K_0402_1%
4HChoke@ PRW14
3.6K_0402_1%

20200903 Follow SP-09948-001_v04
GN20-E7
Edp-c 36A -> 39A
Edp-p 41A -> 50A

+1.35VS_VGA (GN20-E7)
Vout = 1.35V
TDC 39A
Peak Current 50A
OCP current 81.58A
FSW=300KHz
Delta IL=27.9A

DRMOS
MAX

H/S Rds(on):4.8mohm
L/S Rds(on):1.3mohm

Choke
Idc = 36A
Isat = 60A
Rdc = 0.67mohm +-5%

20200903 Follow SP-09948-001_v04
GN20-E5
Edp-c 26A -> 40A
Edp-p 30A -> 59A

+1.35VS_VGA (GN20-E5)
Vout = 1.35V
TDC 40A
Peak Current 59A
OCP current 88.32A
FSW=300KHz
Delta IL=27.9A

Choke
Idc = 35A
Isat = 50A
Rdc = 0.85mohm +-5%

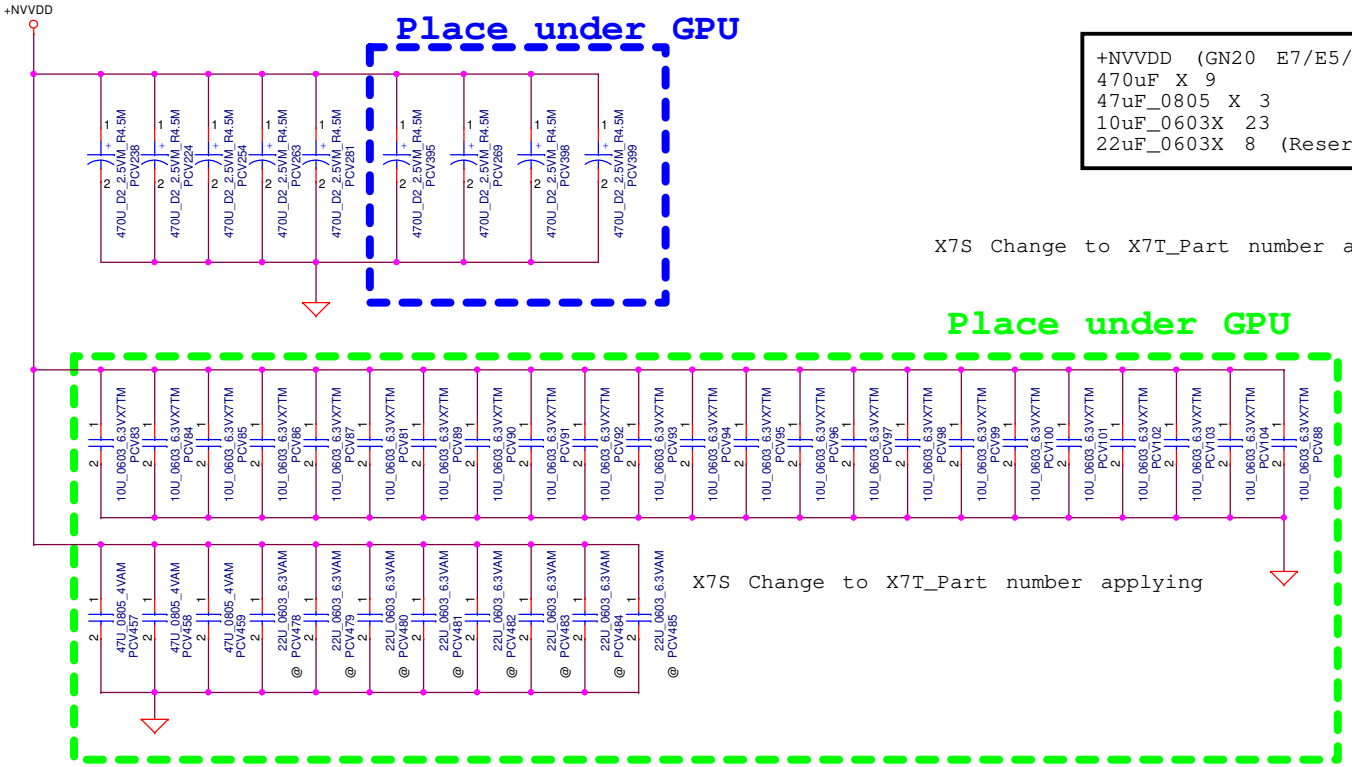
+1.35VS_VGA (GN20-E3)
Vout = 1.35V
TDC 20A
Peak Current 23A
OCP current 88.32A
FSW=300KHz
Delta IL=27.9A

Choke
Idc = 35A
Isat = 50A
Rdc = 0.85mohm +-5%

PLW2 4HChoke@
0.15UH_MMD-06DZER15MEM2L_36A_20%
PLW3 4HChoke@
0.15UH_MMD-06DZER15MEM2L_36A_20%

Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.
Title: PWR +1.35VS_VGA
Size: | Document Number: LA-K741P | Rev: 0.3
Date: Thursday, December 03, 2020 | Sheet 108 of 114



Security Classification	Compal Secret Data		
Issued Date	2019/04/19	Deciphered Date	2020/04/19

Compal Electronics, Inc.

Title: PWR_GPU DECOUPLING

Size | Document Number: LA-K741P | Rev: 0.3

Date: Thursday, December 03, 2020 | Sheet 109 of 114

+12VP
Vout = 12.09V
TDC = 0.6A
Peak current = 0.86A
Fsw = 1.24MHz
Delta IL = 0.717A

MOS

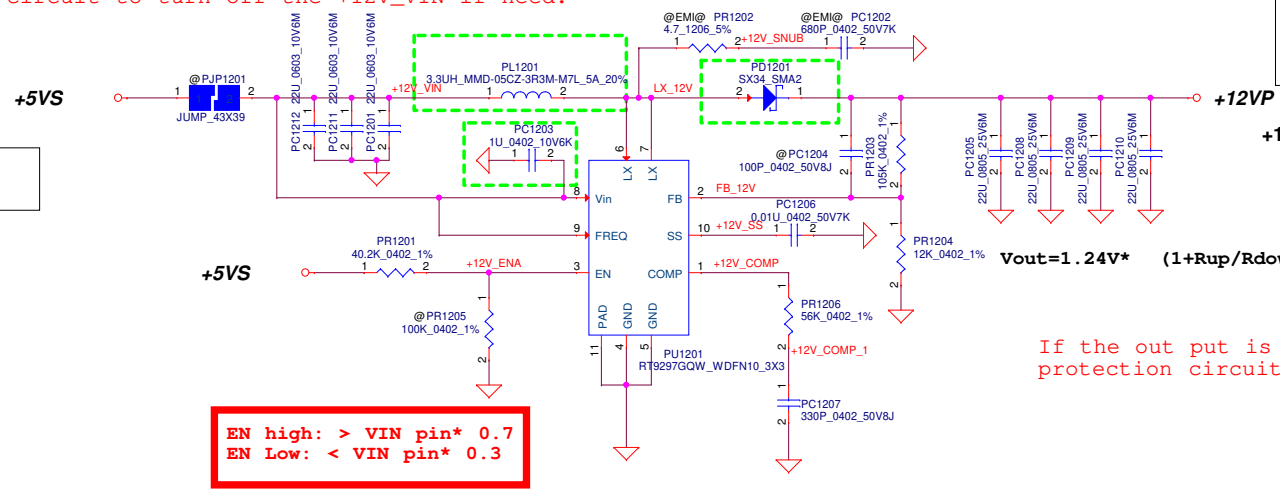
	TYP	MAX
Rds(on) :	125mohm	250mohm

Choke
Idc = 5A
Isat = 7A
Rdc = 32m ohm (Typ), 38m ohm(Max)

Add a switch circuit to turn off the +12V_VIN if need.

Must check PL1201 and PD1201 rating for your application.

Input Current: 2.26A
12V*0.8A/0.85/5V=2.43A



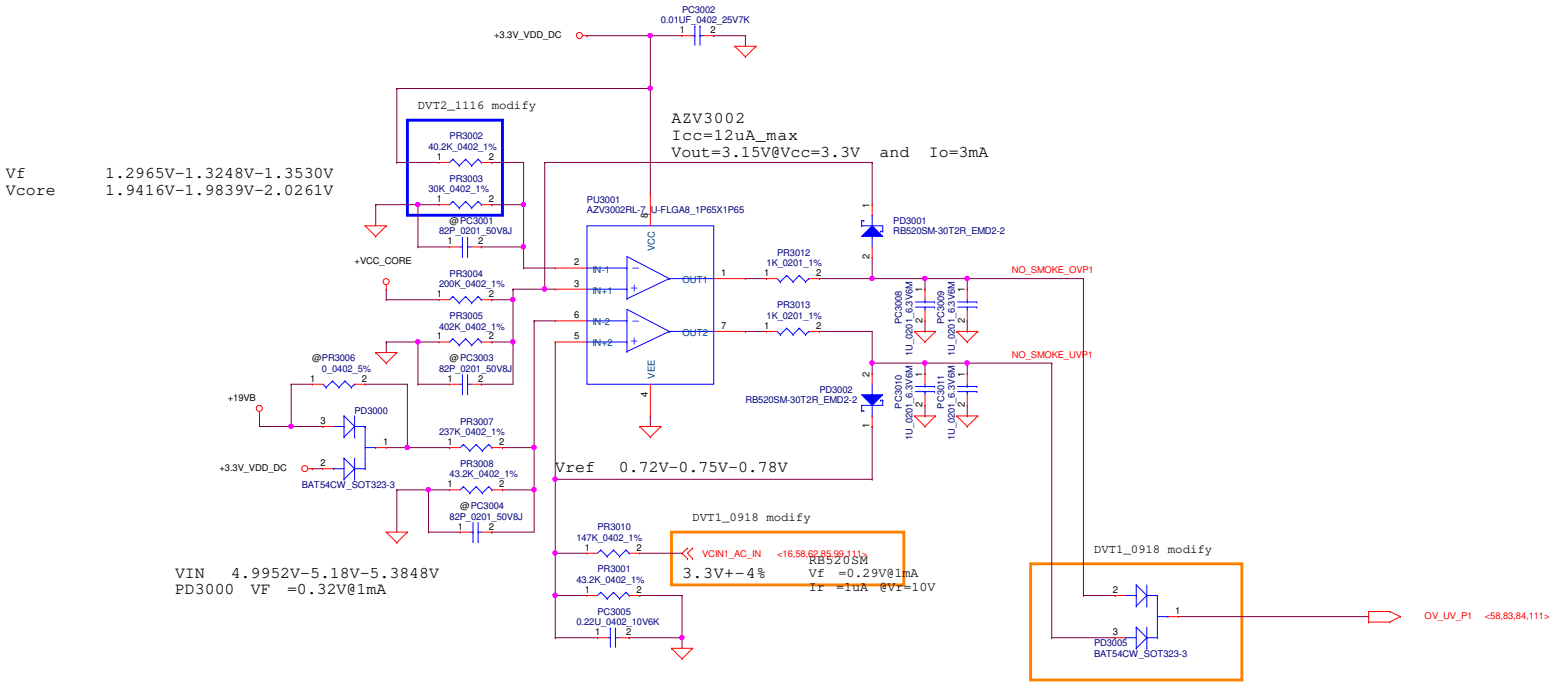
Vout=1.24V* (1+Rup/Rdown)

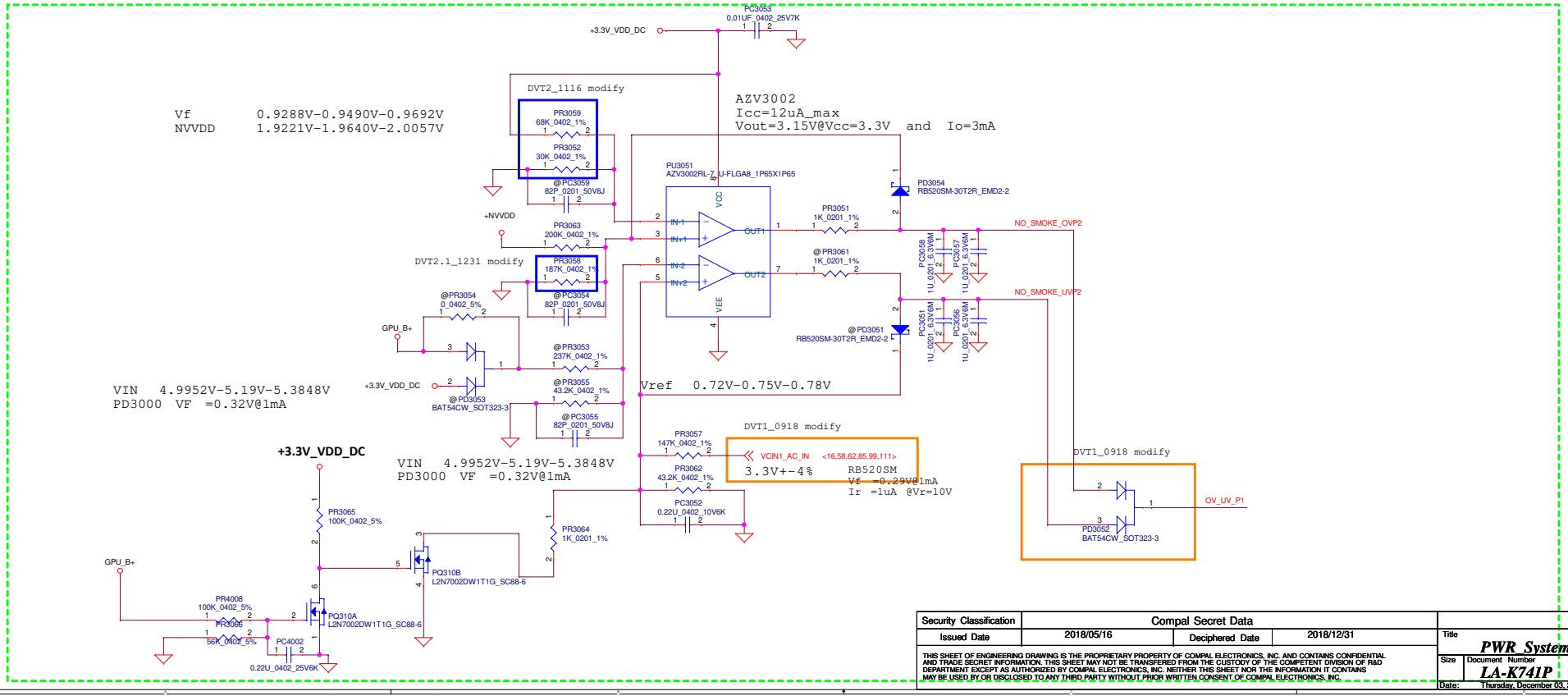
EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3

FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add protection circuit for I/O short protection.

Title		
+12VP		
Size	Document Number	Rev
	LA-K741P	0.3
Date: Thursday, December 03, 2020	Sheet 110 of 114	





Security Classification	Compal Secret Data		
Issued Date	2018/05/16	Deciphered Date	2018/12/31

Title: PWR_System UVP/OVP

Size	Document Number	Rev
	LA-K741P	0.3

Date: Thursday, December 03, 2020 Sheet 111 of 114

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.102	P102-PWR_GPU_CORE(NCP81610)	2020/08/07	Compal_PWR	1.Modify OCL from 75A/phase to 37.5A/phase for NVVDD. (Main source Dr.MOS with 3H Choke) 2.Modify OCL from 75A/phase to 45A/phase for NVVDD. (Main source Dr.MOS with 4H Choke)	1.PRV228 change from SD034226380(226k) to SD034113380(113kΩ). 2.PRV228 change from SD034226380(226k) to SD034137380(137kΩ).	0.1
2	P.103 P.104 P.105 P.106 P.107	P103-PWR_+NVVDD_Phase1&2 P104-PWR_+NVVDD_Phase3&4 P105-PWR_+NVVDD_Phase5&6 P106-PWR_+NVVDD_Phase7&8 P107-PWR_+NVVDD_Phase9&10	2020/08/10	Compal_PWR	1.Change resistance and capacitance of snubber circuit for each phase of NVVDD Dr.MOS to meet PD derating.	1.PRV296,PRV301,PRV306,PRV311,PRV316,PRV321,PRV326,PRV331,PRV336, PRV341change from SD012220B80(2.2Ω)to SD001470B80(4.7Ω). PCV232,PCV245,PCV256,PCV267,PCV278,PCV289,PCV299,PCV305,PCV319, PCV329 change from SE025102K80(1000pF)to SE025681K80(680pF).	0.1
3	P.103 P.104 P.105 P.106 P.107	P103-PWR_+NVVDD_Phase1&2 P104-PWR_+NVVDD_Phase3&4 P105-PWR_+NVVDD_Phase5&6 P106-PWR_+NVVDD_Phase7&8 P107-PWR_+NVVDD_Phase9&10	2020/08/17	Compal_PWR	1.Change main source Dr.MOS NCP303150D to NCP303152 for DVT1 SMT	1.PUV202,PUV203,PUV204,PUV205,PUV206,PUV207,PUV208,PUV209, PUV210,PUV211 change from SA0000CUO00 to SA0000DIL00.	0.1
4	P.102	P102-PWR_GPU_CORE(NCP81610)	2020/08/26	Compal_PWR	1.Modify OCL from 75A/phase to 37.5A/phase for NVVDD. (2nd source Dr.MOS with 3H Choke) 2.Modify OCL from 75A/phase to 45A/phase for NVVDD. (2nd source Dr.MOS with 4H Choke)	1.PRV228 change from SD034169380(169k) to SD034113380(113kΩ). 2.PRV228 change from SD034169380(169k) to SD034137380(137kΩ).	0.1
5	P.108	P108-PWR_+1.35VS_VGA	2020/09/01	Compal_PWR	1.Modify FBVDD DVS function.(1.2-1.35)change to(1.25-1.35)	1.PRW31 change from SD034523280(52.3kΩ) to SD034649280(82.5kΩ)	0.1
6	P.108	P108-PWR_+1.35VS_VGA	2020/09/03	Compal_PWR	Because NV change specification for edpp and edpc of FBVDD. 1.Modify FBVDD OCP from 56.46A to 88.32A.(with 3H Choke) 2.Modify FBVDD OCP from 58.16A to 81.58A.(with 4H Choke)	1.PRW28 change from SD034768280(76.8kΩ) to SD034649280(64.9kΩ) 2.PRW24 change from SD034475280(47.5kΩ) to SD03448728048.7kΩ) PRW28 change from SD00000DM00(82kΩ) to SD034750280(75kΩ)	0.1
7	P.108	P097-PWR_+1.8VSP	2020/09/11	Compal_PWR	1.Because NV change specification for edpp of 1.8V. Modify +1.8V OCP from fixed 12A to adjustable and pull high for PU1801 pin 10 to set OCP=12A.	1.PU1801 pin10 net name "VCC_+1.8VGS" change to "ILIMT_+1.8VGS"	0.1
8	P.103 P.104 P.105 P.106 P.107	P103-PWR_+NVVDD_Phase1&2 P104-PWR_+NVVDD_Phase3&4 P105-PWR_+NVVDD_Phase5&6 P106-PWR_+NVVDD_Phase7&8 P107-PWR_+NVVDD_Phase9&10	2020/09/15	Compal_PWR	1.To prevent material shortage for 0603 X7S 680pF. Downsize capacitor of NVVDD subber circuit from 0603 X7S 680pF to 0402 X7S 680pF	1.PCV232,PCV245,PCV256,PCV267,PCV278,PCV289,PCV299,PCV305,PCV319, PCV329 MLCC 0603 680pF(SE025681K80) change 0402 680pF(SE074681K80).	0.1
9	P.103 P.104 P.105 P.106 P.107	P103-PWR_+NVVDD_Phase1&2 P104-PWR_+NVVDD_Phase3&4 P105-PWR_+NVVDD_Phase5&6 P106-PWR_+NVVDD_Phase7&8 P107-PWR_+NVVDD_Phase9&10	2020/09/25	Compal_PWR	1.Due to delivery of NCP303160 can't catch up DVT1 SMT build. Change Dr.MOS of +NVVDD to NCP303160.	1.PUV202,PUV203,PUV204,PUV205,PUV206,PUV207,PUV208,PUV209,PUV210, PUV211 change from NCP303152(SA0000DIL00) to NCP303160(SA0000DC900)	0.1
10	P.102	P102-PWR_GPU_CORE(NCP81610)	2020/09/25	Compal_PWR	1.Improve IMON accuracy for NVVDD main source and 2nd source solution.	1.Pop PCV201 MLCC 0402 1000pF(SE074102K80)	0.1
11	P.98	P098-PWR_+1.0VS_VGAP	2020/11/17	Compal_PWR	1.Delete current sense and change to short at MP phase.	1.Delete PR1114 0805 0.005ohm(SD00001UY20)	0.2
12	P.92 P.93 P.94 P.95	P092-PWR_+VCC_CORE_Phase1&2 P093-PWR_+VCC_CORE_Phase3&4 P094-PWR_+VCC_CORE_Phase5&6 P095-PWR_+VCC_GT/+VCC_SA	2020/11/30	Compal_PWR	1.Due to AOZ5239 shortage,exchange main source(AOZ5239) and 2nd source(NCP302045) for Dr.MOS of NVVDD power solution.	1.PUZ01,PUG1,PUZ02,PUZ03,PUZ04,PUZ05,PUZ06 change from AOZ5239(SA0000AZQ00) to NCP302045(SA0000AOI30)	0.2

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