Cyborg-N/V/L 14/15_TGL-U & Watchmen 14N TGL-U Schematic

2021-01-07
REV : A00

DY : None Installed
UMA: Unified Memory Architecture
OPS: Optimal Playable Settings

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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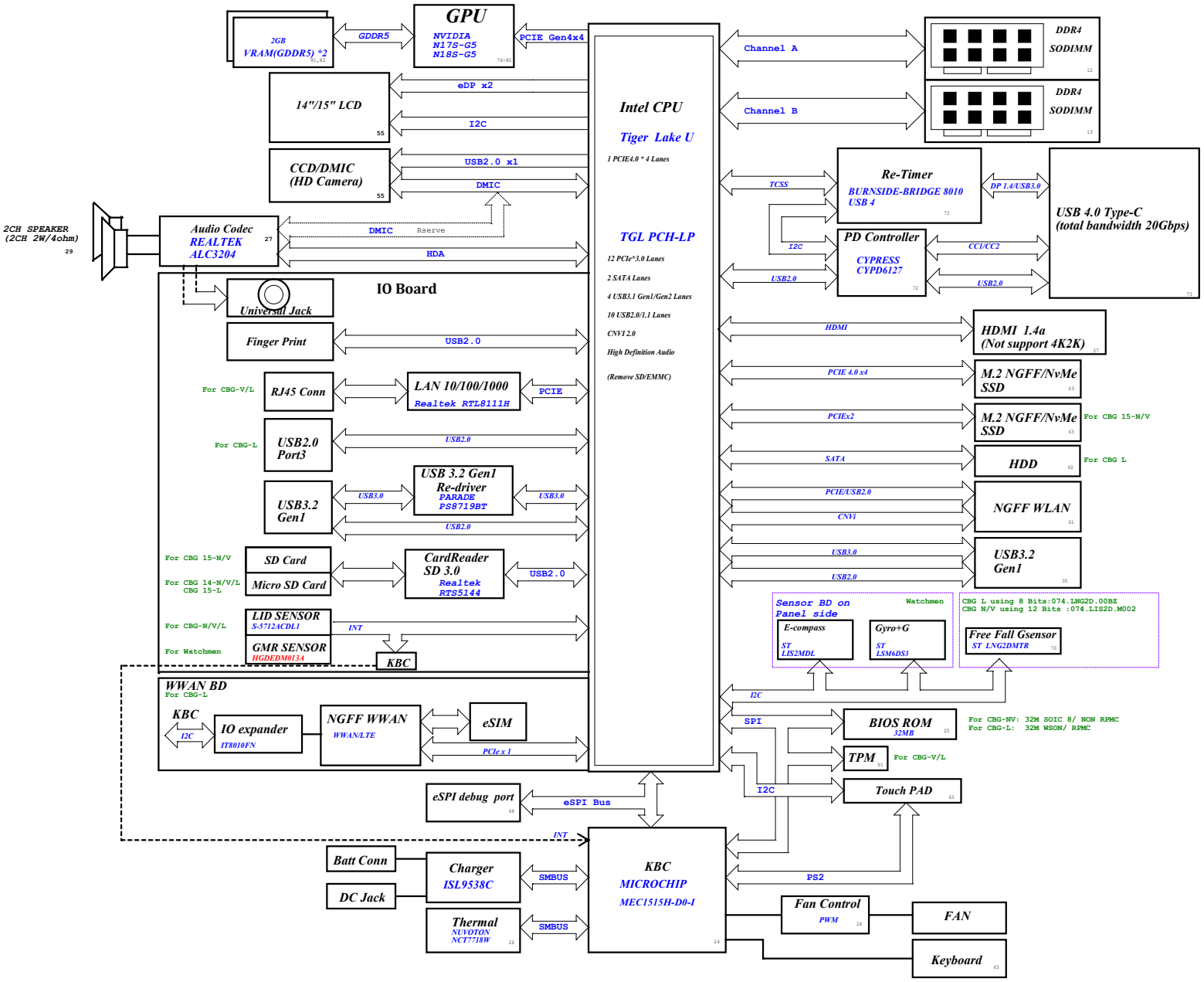
Cyborg N/V/L & Watchmen 14 TGL Block Diagram



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
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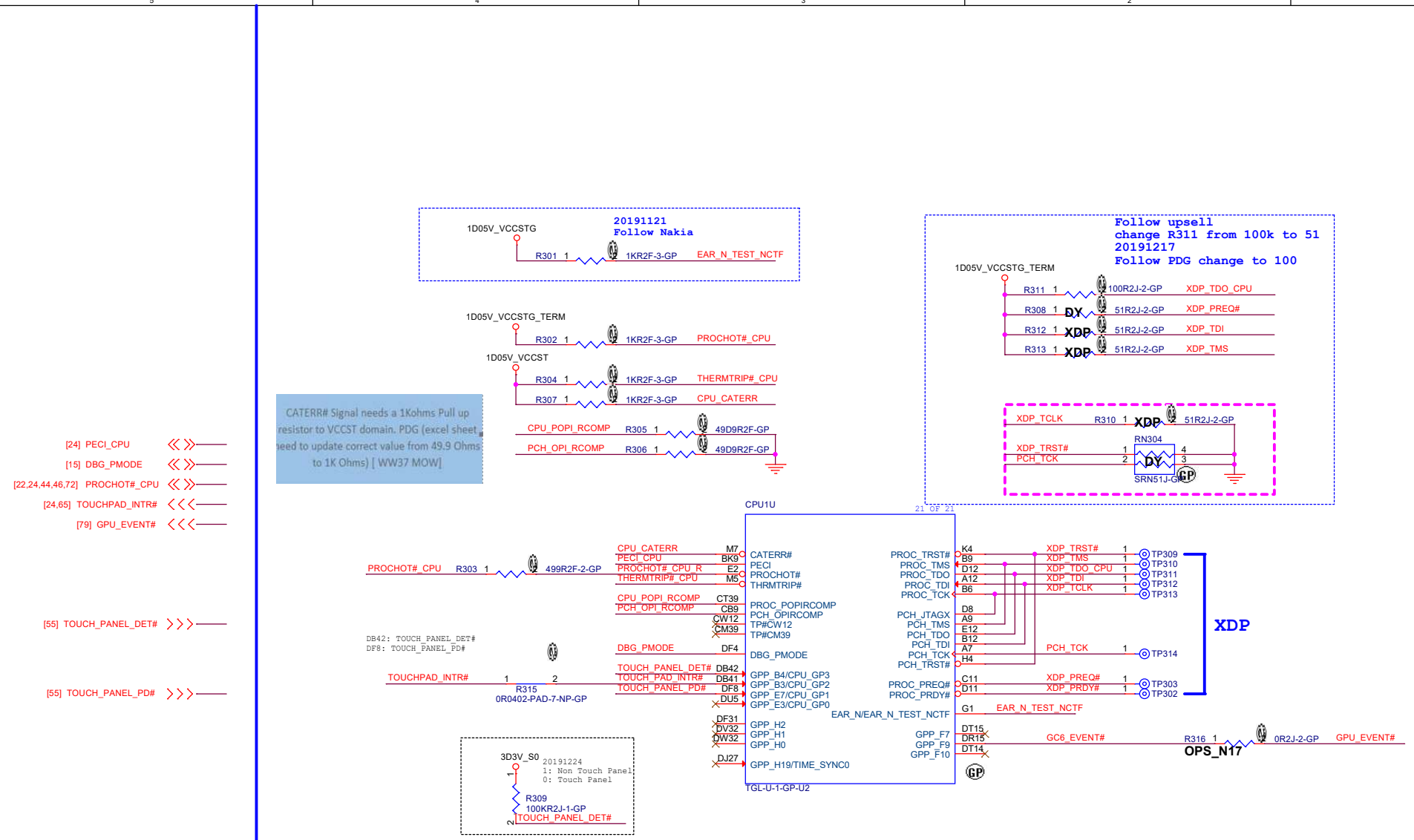

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THML/JTAG)

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eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_N
[55] eDP_AUX_CPU_P
[55] EDP_HPD
[24] L_BKLT_EN
[55] eDP_VDD_EN
[55] L_BKLT_CTRL

HDMI

[57] HDMI_DDI_TX_P3
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N2

[57] HDMI_SCL_CPU
[57] HDMI_SDA_CPU

[57] CPU_DISP_HPDB

TBT

[71] USB1_TCSS_TX_N0
[71] USB1_TCSS_TX_P0
[71] USB1_TCSS_TX_N1
[71] USB1_TCSS_TX_P1
[71] USB1_TCSS_RX_N0
[71] USB1_TCSS_RX_P0
[71] USB1_TCSS_RX_N1
[71] USB1_TCSS_RX_P1

[71] USB1_TCSS_TXD
[15,71] USB1_TCSS_RXD

[71] USB1_TCSS_AUX_P
[71] USB1_TCSS_AUX_N

[72] USB_OC2#

Other

[15] GPP_E21
[15] GPP_D12
[15] GPP_D10
[65] KB_DET#

USB3.2 Type-A Port2 (IO)

[66] USB_OC1#

[62] WWAN_GPIO_PERST#
[62] WWAN_FULL_PWR_EN_R

CPU1A

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eDP
AC2 DDIA_TXP3
AC1 DDIA_TXN3
AD2 DDIA_TXP2
AD1 DDIA_TXN2
AF1 DDIA_TXP1
AF2 DDIA_TXN1
AG2 DDIA_TXP0
AG1 DDIA_TXN0
AJ2 DDIA_AUX_P
AJ1 DDIA_AUX_N

eDP_TX_CPU_P1
eDP_TX_CPU_N1
eDP_TX_CPU_P0
eDP_TX_CPU_N0
eDP_AUX_CPU_P
eDP_AUX_CPU_N

WWAN_FULL_PWR_EN_R
R408 1 2 0R0402-PAD-7-NP-GP
WWAN
WWAN_GPIO_PERST# DN4
WWAN_FULL_PWR_EN DT6
GPP_E22/DDPA_CTRLCLK/DNX_FORCE_RELOAD
GPP_E23/DDPA_CTRLDATA

eDP
EDP_HPD DR5
GPP_E14/DDSP_HPDA/DISP_MISCA

HDMI
HDMI_DDI_TX_P3 T12 DDIB_TXP3
HDMI_DDI_TX_N3 T11 DDIB_TXN3
HDMI_DDI_TX_P0 Y11 DDIB_TXP2
HDMI_DDI_TX_N0 Y9 DDIB_TXN2
HDMI_DDI_TX_P1 T9 DDIB_TXP1
HDMI_DDI_TX_N1 P9 DDIB_TXN1
HDMI_DDI_TX_P2 V11 DDIB_TXP0
HDMI_DDI_TX_N2 V9 DDIB_TXN0
AB9 DDIB_AUX_P
AD9 DDIB_AUX_N

HDMI_SCL_CPU DM29 GPP_H16/DDPB_CTRLCLK/PCIE_LNK_DOWN
HDMI_SDA_CPU DK27 GPP_H17/DDPB_CTRLDATA

CPU_DISP_HPDB DG43 GPP_A18/DDSP_HPDB/DISP_MISCB/I2S4_RXD

DN4: WWAN_GPO_PERST#
DT6: WWAN_CARD_PWR_OFF#
DG47: 3.3V_CAM_EN
DF6: TBT_LSX1_TXD
DN23: SENSOR_DB_DET#
DD6: TBT_LSX1_RXD
DK23: CPU_DDP4_CTRL_CLK
DN21: CPU_DDP4_CTRL_DATA
DF47: CPU_DISP_HPD2
DH52: USB_OC1#
DK45: CPU_DISP_HPD4

DG47 GPP_A21/DDPC_CTRLCLK/I2S5_TXD
KB_DET# DJ47 GPP_A22/DDPC_CTRLDATA/I2S5_RXD

TBT
20191211 for TBT
USB1_TCSS_TXD DU8 GPP_E18/DDP1_CTRLCLK/TBT_LSX0_TXD
USB1_TCSS_RXD DV8 GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD

DF6 GPP_E20/DDP2_CTRLCLK/TBT_LSX1_TXD
GPP_E21 DD6 GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD

DN23 GPP_D9/ISH_SPI_CS#/DDP3_CTRLCLK/TBT_LSX2_TXD/GSPI2_CS0#
GPP_D10 DM23 GPP_D10/ISH_SPI_CLK/DDP3_CTRLDATA/TBT_LSX2_RXD/GSPI2_CLK

DK23 GPP_D11/ISH_SPI_MISO/DDP4_CTRLCLK/TBT_LSX3_TXD/GSPI2_MISO
GPP_D12 DN21 GPP_D12/ISH_SPI_MOSI/DDP4_CTRLDATA/TBT_LSX3_RXD/GSPI2_MOSI

DF43 GPP_A17/DISP_MISCC/I2S4_TXD
CPU_DISP_HPD1 DF45 GPP_A19/DDSP_HPD1/DISP_MISC1/I2S5_SCLK
DF47 GPP_A20/DDSP_HPD2/DISP_MISC2/I2S5_SFRM

USB_OC1# DH52 GPP_A14/USB_OC1#/DDSP_HPD3/I2S3_RXD/DISP_MISC3/DMIC_CLK_B1
USB_OC2# DK45 GPP_A15/USB_OC2#/DDSP_HPD4/DISP_MISC4/I2S4_SCLK

eDP
eDP_VDD_EN DM8 EDP_VDDEN
L_BKLT_EN DN8 EDP_BKLTEN
L_BKLT_CTRL DG10 EDP_BKLTCTL

CPU_DISP_HPD1
R403 1 DY 2 100KR2J-1-GP

TGL-U-1-GP-U2

TBT
20191211 for TBT
TCP0_TXRX_P1 AY2 USB1_TCSS_RX_P1
TCP0_TXRX_N1 AY1 USB1_TCSS_RX_N1
TCP0_TXRX_P0 BB1 USB1_TCSS_RX_P0
TCP0_TXRX_N0 BB2 USB1_TCSS_RX_N0
TCP0_TX_P1 AM5 USB1_TCSS_TX_P1
TCP0_TX_N1 AM7 USB1_TCSS_TX_N1
TCP0_TX_P0 AT7 USB1_TCSS_TX_P0
TCP0_TX_N0 AT5 USB1_TCSS_TX_N0
TCP0_AUX_P AP7 USB1_TCSS_AUX_P
TCP0_AUX_N AP5 USB1_TCSS_AUX_N

TCP1_TXRX_P1 AT2
TCP1_TXRX_N1 AT1
TCP1_TXRX_P0 AU1
TCP1_TXRX_N0 AU2
TCP1_TX_P1 AD5
TCP1_TX_N1 AD7
TCP1_TX_P0 AH7
TCP1_TX_N0 AH5
TCP1_AUX_P AF7
TCP1_AUX_N AF5

TCP2_TXRX_P1 BF1
TCP2_TXRX_N1 BF2
TCP2_TXRX_P0 BE2
TCP2_TXRX_N0 BE1
TCP2_TX_P1 BD7
TCP2_TX_N1 BD5
TCP2_TX_P0 AY5
TCP2_TX_N0 AY7
TCP2_AUX_P BB5
TCP2_AUX_N BB7

TCP3_TXRX_P1 BK1
TCP3_TXRX_N1 BK2
TCP3_TXRX_P0 BJ2
TCP3_TXRX_N0 BJ1
TCP3_TX_P1 BM7
TCP3_TX_N1 BM5
TCP3_TX_P0 BH5
TCP3_TX_N0 BH7
TCP3_AUX_P BK5
TCP3_AUX_N BK7

TC_RCOMP_P AN2 TCSS_RCOMP_P
TC_RCOMP_N AN1 TCSS_RCOMP_N
R402 1 2 150R2F-1-GP

DSI_DE_TE_2 M8

DDI_RCOMP AB1 DISP_RCOMP
R401 1 2 150R2F-1-GP

DISP_UTILS/DSI_DE_TE_1 CE4

GP

3D3V_S0
20191129 layout Request
RN402 2 1 4 SRN2K2J-1-GP
HDMI_SCL_CPU
HDMI_SDA_CPU
R419 1 2 10KR2J-3-GP KB_DET#

3D3V_S5_VCCPRIM 20191211 Remove R422
R421 1 2 10KR2J-3-GP USB_OC1#
20191224 Follow Internal review

Add RTC Gen 9 reset circuit_20170814
leakage issue 20191224 Follow Internal review

3D3V_S5_VCCPRIM
R406 10KR2J-3-GP DY_RTC_RST
3D3V_S5_VCCPRIM
R405 10KR2J-3-GP DY_RTC_RST
Q401
CPU_DISP_HPD1
CPU_DISP_HPD1_P
2N7002KDW-1-GP DY_RTC_RST
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.07002.0A7C

<Core Design>

Wistron Corporation
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Title: CPU (DDI/EDP/TBT/TPC/)
Size: A3
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DDR4 ball type: Non-Interleaved Type

Channel A

M_A_A0 [12] … M_A_A16 [12]

M_A_DQS_DP0 … M_A_DQS_DP7 [12]

M_A_DQS_DN0 … M_A_DQS_DN7 [12]

M_A_DQ0 [12] … M_A_DQ63 [12]

[12] M_A_CLK#0 · [12] M_A_CLK0 · [12] M_A_CKE0 · [12] M_A_CKE1 · [12] M_A_CS#0 · [12] M_A_BA0 · [12] M_A_BA1 · [12] M_A_BG0 · [12] M_A_BG1

[12] M_A_ODT0 · [12] M_A_ODT1 · [12] M_A_ACT_N · [12] M_A_PARITY · [12] M_A_ALERT_N · M_A_CLK1 [12] · M_A_CLK#1 [12] · M_A_CS#1 [12]

Channel B

M_B_A0 [13] … M_B_A16 [13]

M_B_DQS_DN0 … M_B_DQS_DN7 [13]

M_B_DQS_DP0 … M_B_DQS_DP7 [13]

M_B_DQ0 [13] … M_B_DQ63 [13]

[13] M_B_CLK#0 · [13] M_B_CLK0 · [13] M_B_CKE1 · [13] M_B_CKE0 · [13] M_B_CS#0 · [13] M_B_BA0 · [13] M_B_BA1 · [13] M_B_BG0 · [13] M_B_BG1

[13] M_B_ODT0 · [13] M_B_ODT1 · [13] M_B_ACT_N · [13] M_B_PARITY · [13] M_B_ALERT_N · M_B_CLK1 [13] · M_B_CLK#1 [13] · M_B_CS#1 [13]

[12] V_SM_VREF_CNTA · [13] V_SM_VREF_CNTB · [51] VTT_CNTL · [12,13] SM_DRAMRST_N

CPU1B

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LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR0_DQ0_7/DDR0_DQ0_7/DDR0_DQ0_7 … DDR0_DQ0_6/DDR0_DQ0_6/DDR0_DQ0_6

DDR0_DQ0_5/DDR0_DQ0_5/DDR0_DQ0_5 … DDR0_DQ0_4/DDR0_DQ0_4/DDR0_DQ0_4

DDR0_DQ0_3/DDR0_DQ0_3/DDR0_DQ0_3 … DDR0_DQ0_2/DDR0_DQ0_2/DDR0_DQ0_2

DDR0_DQ0_1/DDR0_DQ0_1/DDR0_DQ0_1 … DDR0_DQ0_0/DDR0_DQ0_0/DDR0_DQ0_0

DDR0_DQ1_7/DDR0_DQ1_7/DDR0_DQ1_7 … DDR0_DQ1_6/DDR0_DQ1_6/DDR0_DQ1_6

DDR0_DQ1_5/DDR0_DQ1_5/DDR0_DQ1_5 … DDR0_DQ1_4/DDR0_DQ1_4/DDR0_DQ1_4

DDR0_DQ1_3/DDR0_DQ1_3/DDR0_DQ1_3 … DDR0_DQ1_2/DDR0_DQ1_2/DDR0_DQ1_2

DDR0_DQ1_1/DDR0_DQ1_1/DDR0_DQ1_1 … DDR0_DQ1_0/DDR0_DQ1_0/DDR0_DQ1_0

DDR0_DQ2_7/DDR0_DQ2_7/DDR0_DQ2_7 … DDR0_DQ2_6/DDR0_DQ2_6/DDR0_DQ2_6

DDR0_DQ2_5/DDR0_DQ2_5/DDR0_DQ2_5 … DDR0_DQ2_4/DDR0_DQ2_4/DDR0_DQ2_4

DDR0_DQ2_3/DDR0_DQ2_3/DDR0_DQ2_3 … DDR0_DQ2_2/DDR0_DQ2_2/DDR0_DQ2_2

DDR0_DQ2_1/DDR0_DQ2_1/DDR0_DQ2_1 … DDR0_DQ2_0/DDR0_DQ2_0/DDR0_DQ2_0

DDR1_DQ0_7/DDR1_DQ0_7/DDR1_DQ0_7 … DDR1_DQ0_6/DDR1_DQ0_6/DDR1_DQ0_6

DDR1_DQ0_5/DDR1_DQ0_5/DDR1_DQ0_5 … DDR1_DQ0_4/DDR1_DQ0_4/DDR1_DQ0_4

DDR1_DQ0_3/DDR1_DQ0_3/DDR1_DQ0_3 … DDR1_DQ0_2/DDR1_DQ0_2/DDR1_DQ0_2

DDR1_DQ0_1/DDR1_DQ0_1/DDR1_DQ0_1 … DDR1_DQ0_0/DDR1_DQ0_0/DDR1_DQ0_0

DDR1_DQ1_7/DDR1_DQ1_7/DDR1_DQ1_7 … DDR1_DQ1_6/DDR1_DQ1_6/DDR1_DQ1_6

DDR1_DQ1_5/DDR1_DQ1_5/DDR1_DQ1_5 … DDR1_DQ1_4/DDR1_DQ1_4/DDR1_DQ1_4

DDR1_DQ1_3/DDR1_DQ1_3/DDR1_DQ1_3 … DDR1_DQ1_2/DDR1_DQ1_2/DDR1_DQ1_2

DDR1_DQ1_1/DDR1_DQ1_1/DDR1_DQ1_1 … DDR1_DQ1_0/DDR1_DQ1_0/DDR1_DQ1_0

DDR2_DQ0_7/DDR2_DQ0_7/DDR2_DQ0_7 … DDR2_DQ0_6/DDR2_DQ0_6/DDR2_DQ0_6

DDR2_DQ0_5/DDR2_DQ0_5/DDR2_DQ0_5 … DDR2_DQ0_4/DDR2_DQ0_4/DDR2_DQ0_4

DDR2_DQ0_3/DDR2_DQ0_3/DDR2_DQ0_3 … DDR2_DQ0_2/DDR2_DQ0_2/DDR2_DQ0_2

DDR2_DQ0_1/DDR2_DQ0_1/DDR2_DQ0_1 … DDR2_DQ0_0/DDR2_DQ0_0/DDR2_DQ0_0

DDR2_DQ1_7/DDR2_DQ1_7/DDR2_DQ1_7 … DDR2_DQ1_6/DDR2_DQ1_6/DDR2_DQ1_6

DDR2_DQ1_5/DDR2_DQ1_5/DDR2_DQ1_5 … DDR2_DQ1_4/DDR2_DQ1_4/DDR2_DQ1_4

DDR2_DQ1_3/DDR2_DQ1_3/DDR2_DQ1_3 … DDR2_DQ1_2/DDR2_DQ1_2/DDR2_DQ1_2

DDR2_DQ1_1/DDR2_DQ1_1/DDR2_DQ1_1 … DDR2_DQ1_0/DDR2_DQ1_0/DDR2_DQ1_0

DDR3_DQ0_7/DDR3_DQ0_7/DDR3_DQ0_7 … DDR3_DQ0_6/DDR3_DQ0_6/DDR3_DQ0_6

DDR3_DQ0_5/DDR3_DQ0_5/DDR3_DQ0_5 … DDR3_DQ0_4/DDR3_DQ0_4/DDR3_DQ0_4

DDR3_DQ0_3/DDR3_DQ0_3/DDR3_DQ0_3 … DDR3_DQ0_2/DDR3_DQ0_2/DDR3_DQ0_2

DDR3_DQ0_1/DDR3_DQ0_1/DDR3_DQ0_1 … DDR3_DQ0_0/DDR3_DQ0_0/DDR3_DQ0_0

DDR3_DQ1_7/DDR3_DQ1_7/DDR3_DQ1_7 … DDR3_DQ1_6/DDR3_DQ1_6/DDR3_DQ1_6

DDR3_DQ1_5/DDR3_DQ1_5/DDR3_DQ1_5 … DDR3_DQ1_4/DDR3_DQ1_4/DDR3_DQ1_4

DDR3_DQ1_3/DDR3_DQ1_3/DDR3_DQ1_3 … DDR3_DQ1_2/DDR3_DQ1_2/DDR3_DQ1_2

DDR3_DQ1_1/DDR3_DQ1_1/DDR3_DQ1_1 … DDR3_DQ1_0/DDR3_DQ1_0/DDR3_DQ1_0

DDR4_CPU_PWRGD

DDR4/LP4/LP5/LP5 CMD Flip

DDR0_CLK_P1/DDR3_CLK_P/DDR3_CLK_P/DDR3_CLK_P5 · DDR0_CLK_N1/DDR3_CLK_N/DDR3_CLK_N/DDR3_CLK_N5

NC/DDR2_CLK_P/DDR2_CLK_P/DDR2_CLK_P5 · NC/DDR2_CLK_N/DDR2_CLK_N/DDR2_CLK_N5

NC/DDR1_CLK_P/DDR1_CLK_P/DDR1_CLK_P5 · NC/DDR1_CLK_N/DDR1_CLK_N/DDR1_CLK_N5

DDR0_CLK_P0/DDR0_CLK_P/DDR0_CLK_P/DDR0_CLK_P5 · DDR0_CLK_N0/DDR0_CLK_N/DDR0_CLK_N/DDR0_CLK_N5

NC/DDR3_CKE0/DDR3_WCK_P/DDR3_WCK_P5 · NC/DDR3_CKE1/DDR3_WCK_N/DDR3_WCK_N5

NC/DDR2_CKE0/DDR2_WCK_P/DDR2_WCK_P5 · NC/DDR2_CKE1/DDR2_WCK_N/DDR2_WCK_N5

NC/DDR1_CKE0/DDR1_WCK_P/DDR1_WCK_P5 · NC/DDR1_CKE1/DDR1_WCK_N/DDR1_WCK_N5

NC/DDR0_CKE0/DDR0_WCK_P/DDR0_WCK_P5 · NC/DDR0_CKE1/DDR0_WCK_N/DDR0_WCK_N5

DDR0_CKE1/DDR2_CA4/DDR2_CA5/DDR2_CA1 · DDR0_CKE0/DDR2_CA5/DDR2_CA6/DDR2_CA0

DDR0_CS1/DDR1_CA1/DDR1_CA1/DDR1_CA5 · DDR0_CS0/NC/DDR1_CS1/DDR1_CA4

NC/DDR0_CA0/DDR0_CA0/DDR0_CA6 · NC/DDR0_CA1/DDR0_CA1/DDR0_CA5 · NC/DDR2_CS0/DDR2_CA2/DDR2_CA2 · NC/DDR3_CA5/DDR3_CA5/DDR3_CA0 · NC/DDR3_CA4/DDR3_CA5/DDR3_CA1 · NC/DDR3_CA3/DDR3_CA4/DDR3_CS1 · NC/DDR3_CA2/DDR3_CA3/DDR3_CS0

DDR3_DQSP_1/DDR0_DQSP_7/DDR1_DQSP_3 … DDR3_DQSN_1/DDR0_DQSN_7/DDR1_DQSN_3

DDR3_DQSP_0/DDR0_DQSP_6/DDR1_DQSP_2 … DDR3_DQSN_0/DDR0_DQSN_6/DDR1_DQSN_2

DDR2_DQSP_1/DDR0_DQSP_5/DDR0_DQSP_3 … DDR2_DQSN_1/DDR0_DQSN_5/DDR0_DQSN_3

DDR2_DQSP_0/DDR0_DQSP_4/DDR0_DQSP_2 … DDR2_DQSN_0/DDR0_DQSN_4/DDR0_DQSN_2

DDR1_DQSP_1/DDR0_DQSP_3/DDR1_DQSP_1 … DDR1_DQSN_1/DDR0_DQSN_3/DDR1_DQSN_1

DDR1_DQSP_0/DDR0_DQSP_2/DDR1_DQSP_0 … DDR1_DQSN_0/DDR0_DQSN_2/DDR1_DQSN_0

DDR0_ODT1/DDR1_CA0/DDR1_CA0/DDR1_CA6 · DDR1_ODT0/DDR1_CS0/DDR1_CA2/DDR1_CA2

DDR0_MA16/DDR1_CA4/DDR1_CA5/DDR1_CA1 · DDR0_MA15/DDR1_CA3/DDR1_CA4/DDR1_CS1 · DDR0_MA14/DDR1_CA2/DDR1_CA3/DDR1_CS0 · DDR0_MA13/DDR1_CS1/DDR1_CS0/DDR1_CA3 · DDR0_MA12/DDR2_CA1/DDR2_CA1/DDR2_CA5

DDR0_MA11/NC/DDR2_CS1/DDR2_CA4 · DDR0_MA10/DDR3_CA1/DDR3_CA1/DDR3_CA5 · DDR0_MA9/DDR2_CA0/DDR2_CA0/DDR2_CA6 · DDR0_MA8/DDR2_CA2/DDR2_CA2/DDR2_CA3 · DDR0_MA7/DDR0_CA4/DDR0_CA5/DDR0_CA1 · DDR0_MA6/DDR0_CA3/DDR0_CA4/DDR0_CS1 · DDR0_MA5/DDR0_CA5/DDR0_CA6/DDR0_CA0 · DDR0_MA4/DDR0_CS0/DDR0_CA2/DDR0_CA2 · DDR0_MA3/DDR0_CS1/DDR0_CS0/DDR0_CA3 · DDR0_MA2/DDR3_CS0/DDR3_CA2/DDR3_CA2

DDR0_MA1/NC/DDR0_CS1/DDR0_CA4 · DDR0_MA0/NC/DDR3_CS1/DDR3_CA4

DDR0_BG1/DDR2_CA2/DDR2_CA3/DDR2_CS0 · DDR0_BG0/DDR2_CA3/DDR2_CA4/DDR2_CS1

DDR0_BA1/DDR1_CA5/DDR1_CA6/DDR1_CA0 · DDR0_BA0/DDR3_CA0/DDR3_CA0/DDR3_CA6

DDR0_ACT#/DDR2_CS1/DDR2_CS0/DDR2_CA3

DDR0_PAR/DDR3_CS1/DDR3_CS0/DDR3_CA3

DDR0_ALERT# / DDR0_VREF_CA · V_SM_VREF_CNTA

DDR_VTT_CTL / DRAM_RESET# / DDR_RCOMP · VTT_CNTL_CPU · SM_DRAMRST#_CPU · SM_RCOMP · R502 100R2F-L1-GP-U

CPU1C

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LP4-LP5(NIL)/DDR4 (NIL)/DDR4 (IL)

DDR4/LP4/LP5/LP5 CMD Flip

DDR4_DQ0_7/DDR1_DQ0_7/DDR0_DQ4_7 … DDR4_DQ0_6/DDR1_DQ0_6/DDR0_DQ4_6

DDR4_DQ0_5/DDR1_DQ0_5/DDR0_DQ4_5 … DDR4_DQ0_4/DDR1_DQ0_4/DDR0_DQ4_4

DDR4_DQ0_3/DDR1_DQ0_3/DDR0_DQ4_3 … DDR4_DQ0_2/DDR1_DQ0_2/DDR0_DQ4_2

DDR4_DQ0_1/DDR1_DQ0_1/DDR0_DQ4_1 … DDR4_DQ0_0/DDR1_DQ0_0/DDR0_DQ4_0

DDR4_DQ1_7/DDR1_DQ1_7/DDR0_DQ5_7 … DDR4_DQ1_6/DDR1_DQ1_6/DDR0_DQ5_6

DDR4_DQ1_5/DDR1_DQ1_5/DDR0_DQ5_5 … DDR4_DQ1_4/DDR1_DQ1_4/DDR0_DQ5_4

DDR4_DQ1_3/DDR1_DQ1_3/DDR0_DQ5_3 … DDR4_DQ1_2/DDR1_DQ1_2/DDR0_DQ5_2

DDR4_DQ1_1/DDR1_DQ1_1/DDR0_DQ5_1 … DDR4_DQ1_0/DDR1_DQ1_0/DDR0_DQ5_0

DDR4_DQ2_7/DDR1_DQ2_7/DDR0_DQ6_7 … DDR4_DQ2_6/DDR1_DQ2_6/DDR0_DQ6_6

DDR4_DQ2_5/DDR1_DQ2_5/DDR0_DQ6_5 … DDR4_DQ2_4/DDR1_DQ2_4/DDR0_DQ6_4

DDR4_DQ2_3/DDR1_DQ2_3/DDR0_DQ6_3 … DDR4_DQ2_2/DDR1_DQ2_2/DDR0_DQ6_2

DDR4_DQ2_1/DDR1_DQ2_1/DDR0_DQ6_1 … DDR4_DQ2_0/DDR1_DQ2_0/DDR0_DQ6_0

DDR4_DQ3_7/DDR1_DQ3_7/DDR0_DQ7_7 … DDR4_DQ3_6/DDR1_DQ3_6/DDR0_DQ7_6

DDR4_DQ3_5/DDR1_DQ3_5/DDR0_DQ7_5 … DDR4_DQ3_4/DDR1_DQ3_4/DDR0_DQ7_4

DDR4_DQ3_3/DDR1_DQ3_3/DDR0_DQ7_3 … DDR4_DQ3_2/DDR1_DQ3_2/DDR0_DQ7_2

DDR4_DQ3_1/DDR1_DQ3_1/DDR0_DQ7_1 … DDR4_DQ3_0/DDR1_DQ3_0/DDR0_DQ7_0

DDR1_CLK_P1/DDR7_CLK_P/DDR7_CLK_P … DDR1_CLK_N1/DDR7_CLK_N/DDR7_CLK_N

NC/DDR6_CLK_P/DDR6_CLK_P/DDR6_CLK_P · NC/DDR6_CLK_N/DDR6_CLK_N/DDR6_CLK_N

NC/DDR5_CLK_P/DDR5_CLK_P/DDR5_CLK_P · NC/DDR5_CLK_N/DDR5_CLK_N/DDR5_CLK_N

DDR1_CLK_P0/DDR4_CLK_P/DDR4_CLKP/DDR4_CLK_P · DDR1_CLK_N0/DDR4_CLK_N/DDR4_CLK_N/DDR4_CLK_N

NC/DDR7_CKE0/DDR7_WCK_P/DDR7_WCK_P · NC/DDR7_CKE1/DDR7_WCK_N/DDR7_WCK_N

NC/DDR6_CKE0/DDR6_WCK_P/DDR6_WCK_P · NC/DDR6_CKE1/DDR6_WCK_N/DDR6_WCK_N

NC/DDR5_CKE0/DDR5_WCK_P/DDR5_WCK_P · NC/DDR5_CKE1/DDR5_WCK_N/DDR5_WCK_N

NC/DDR4_CKE0/DDR4_WCK_P/DDR4_WCK_P · NC/DDR4_CKE1/DDR4_WCK_N/DDR4_WCK_N

DDR1_CKE1/DDR6_CA4/DDR6_CA5/DDR6_CA1 · DDR1_CKE0/DDR6_CA5/DDR6_CA6/DDR6_CA0

DDR1_CS1/DDR5_CA1/DDR5_CA1/DDR5_CA5 · DDR1_CS0/NC/DDR5_CS1/DDR5_CA4

NC/DDR7_CA5/DDR7_CA6/DDR7_CA0 · NC/DDR7_CA4/DDR7_CA5/DDR7_CA1 · NC/DDR7_CA3/DDR7_CA4/DDR7_CS1 · NC/DDR7_CA2/DDR7_CA3/DDR7_CS0 · NC/DDR6_CS0/DDR6_CA2/DDR6_CA2 · NC/DDR6_CA1/DDR6_CA1/DDR6_CA5 · NC/DDR4_CA0/DDR4_CA0/DDR4_CA6

DDR7_DQSP_1/DDR1_DQSP_7/DDR1_DQSP_7 … DDR7_DQSN_1/DDR1_DQSN_7/DDR1_DQSN_7

DDR7_DQSP_0/DDR1_DQSP_6/DDR1_DQSP_6 … DDR7_DQSN_0/DDR1_DQSN_6/DDR1_DQSN_6

DDR6_DQSP_1/DDR1_DQSP_5/DDR0_DQSP_7 … DDR6_DQSN_1/DDR1_DQSN_5/DDR0_DQSN_7

DDR6_DQSP_0/DDR1_DQSP_4/DDR0_DQSP_6 … DDR6_DQSN_0/DDR1_DQSN_4/DDR0_DQSN_6

DDR5_DQSP_1/DDR1_DQSP_3/DDR1_DQSP_5 … DDR5_DQSN_1/DDR1_DQSN_3/DDR1_DQSN_5

DDR5_DQSP_0/DDR1_DQSP_2/DDR1_DQSP_4 … DDR5_DQSN_0/DDR1_DQSN_2/DDR1_DQSN_4

DDR4_DQSP_1/DDR1_DQSP_1/DDR0_DQSP_5 … DDR4_DQSN_1/DDR1_DQSN_1/DDR0_DQSN_5

DDR4_DQSP_0/DDR1_DQSP_0/DDR0_DQSP_4 … DDR4_DQSN_0/DDR1_DQSN_0/DDR0_DQSN_4

DDR1_ODT1/DDR5_CA0/DDR5_CA0/DDR5_CA6 · DDR1_ODT0/DDR5_CS0/DDR5_CA2/DDR5_CA2

DDR1_MA16/DDR5_CA4/DDR5_CA5/DDR5_CA1 · DDR1_MA15/DDR5_CA3/DDR5_CA4/DDR5_CS1 · DDR1_MA14/DDR5_CA2/DDR5_CA3/DDR5_CS0 · DDR1_MA13/DDR5_CS1/DDR5_CS0/DDR5_CA3 · DDR1_MA12/DDR6_CA1/DDR6_CA1/DDR6_CA5

DDR1_MA11/NC/DDR6_CS1/DDR6_CA4 · DDR1_MA10/DDR7_CA1/DDR7_CA1/DDR7_CA5 · DDR1_MA9/DDR6_CA0/DDR6_CA0/DDR6_CA6 · DDR1_MA8/DDR4_CA2/DDR4_CA3/DDR4_CS0 · DDR1_MA7/DDR4_CA4/DDR4_CA5/DDR4_CA1 · DDR1_MA6/DDR4_CA3/DDR4_CA4/DDR4_CS1 · DDR1_MA5/DDR4_CA5/DDR4_CA6/DDR4_CA0 · DDR1_MA4/DDR4_CS0/DDR4_CA2/DDR4_CA2 · DDR1_MA3/DDR4_CS1/DDR4_CS0/DDR4_CA3 · DDR1_MA2/DDR7_CS0/DDR7_CA2/DDR7_CA2

DDR1_MA1/NC/DDR4_CS1/DDR4_CA4 · DDR1_MA0/NC/DDR7_CS1/DDR7_CA4

DDR1_BG1/DDR6_CA2/DDR6_CA3/DDR6_CS0 · DDR1_BG0/DDR6_CA3/DDR6_CA4/DDR6_CS1

DDR1_BA1/DDR5_CA5/DDR5_CA6/DDR5_CA0 · DDR1_BA0/DDR7_CA0/DDR7_CA0/DDR7_CA6

DDR1_ACT#/DDR6_CS1/DDR6_CS0/DDR6_CA3

DDR1_PAR/DDR7_CS1/DDR7_CS0/DDR7_CA3

DDR1_ALERT# / DDR1_VREF_CA

Power / Clock

3D3V_S0 · R520 220KR2F-GP · 1D2V_S3 · Q501 PJA138KA-GP · VTT_CNTL_CPU · VTT_CNTL

084.00138.0A31

2nd = 84.05067.031

1D2V_S3 · R510 470R2F-GP · SM_DRAMRST#_CPU · R511 0R0402-PAD-7-NP-GP · SM_DRAMRST_N · C501 10UF/6.3V/20X-3DLGP · DY

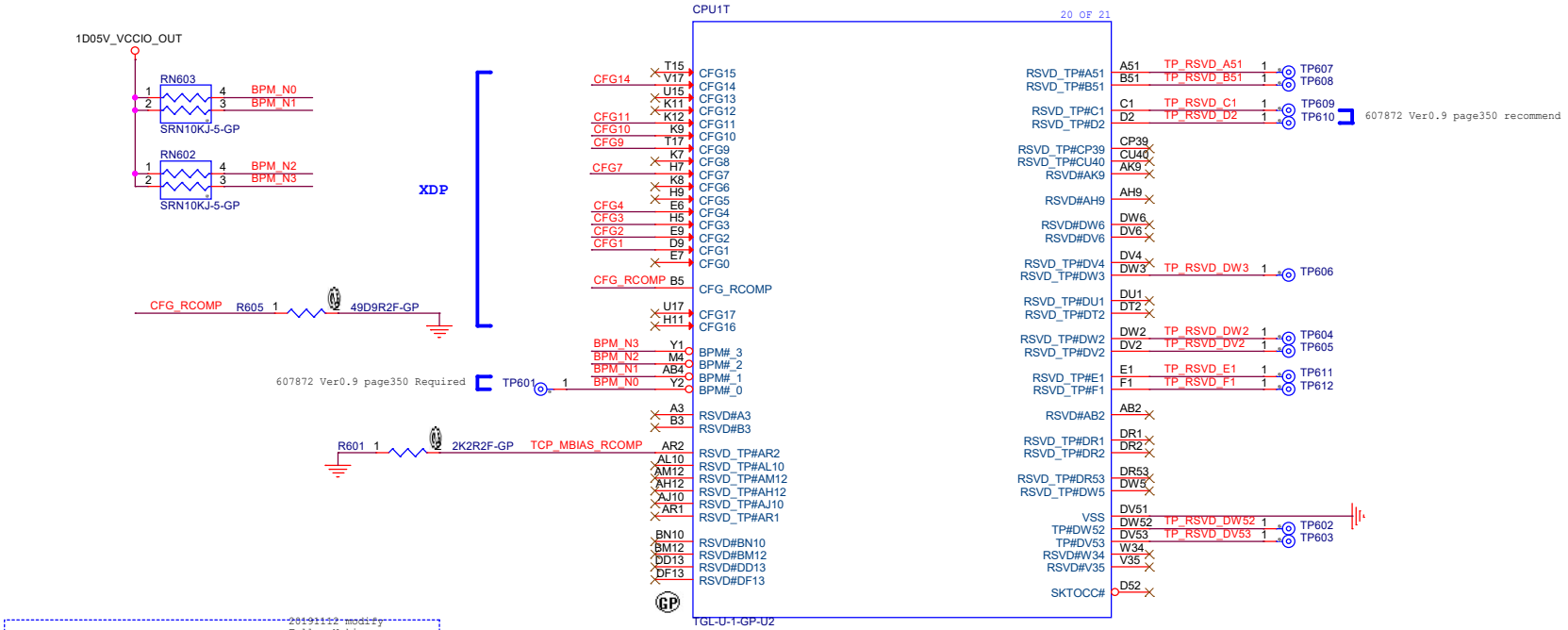
<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

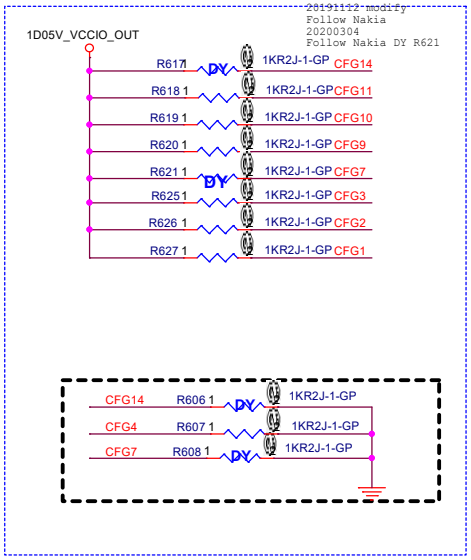
Title: CPU (DDR)

Size: A2 · Document Number: Cyborg TGL · Rev: SC

Date: Thursday, January 14, 2021 · Sheet 5 of 105



607872 Ver0.9 page350 Required



CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-up to VCCSTG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

Bifurcation	Link Width	CFG Signals	Lanes			
	0:6:0	CFG [14]	0	1	2	3
1x4	x4	0	0	1	2	3
1x4 **Reversed**	x4	1	3	2	1	0

Notes:
1. PCIe* Port60 is a single x4 port without bifurcation capabilities, thus bifurcation pin straps are not applicable.

<Core Design>

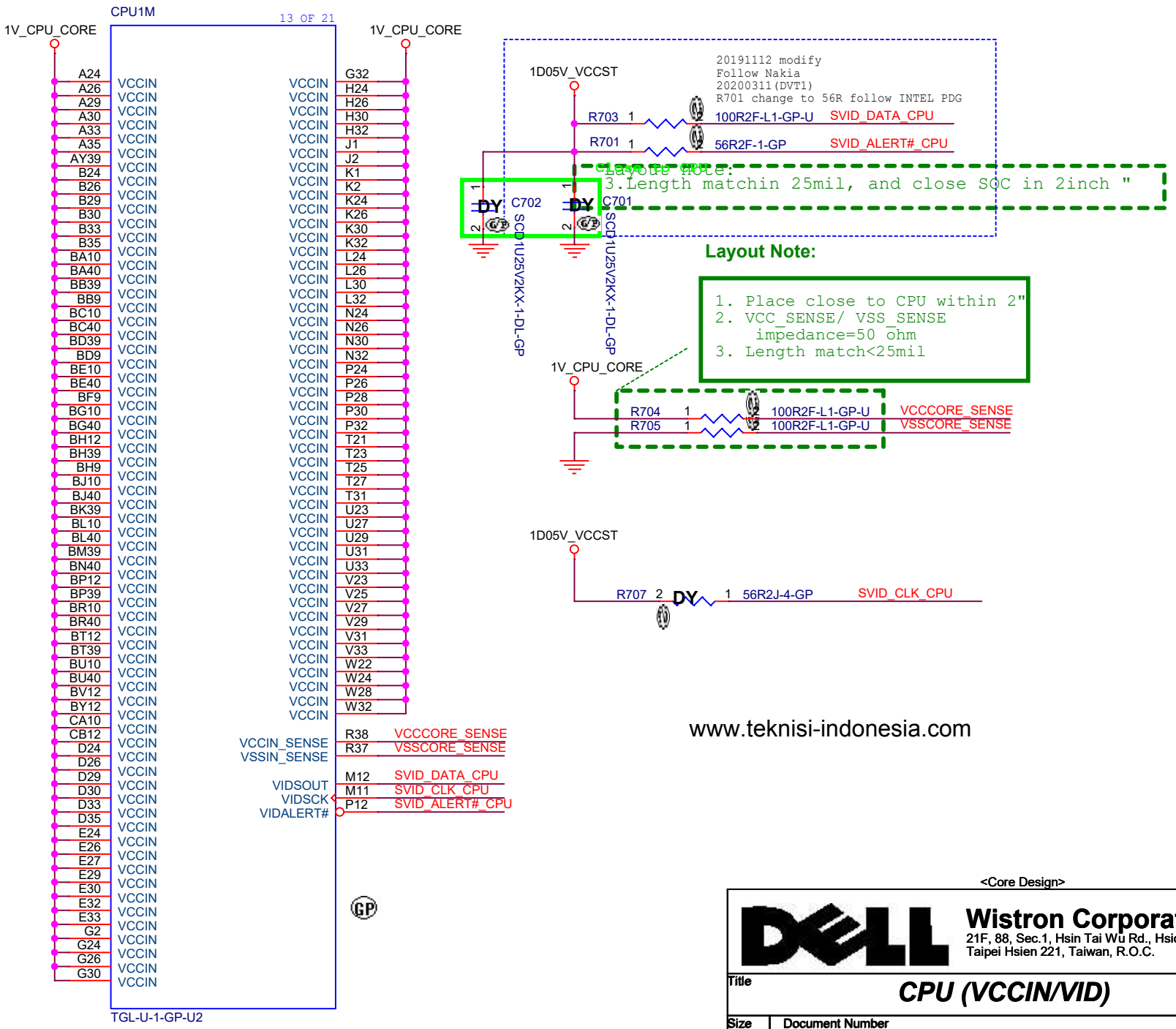
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (CFG/IST)***

Size	Document Number	Rev
A3	***Cyborg TGL***	SC

Date: Thursday, January 14, 2021 Sheet 6 of 105

[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] SVID_ALERT#_CPU
[46] SVID_CLK_CPU
[46] SVID_DATA_CPU



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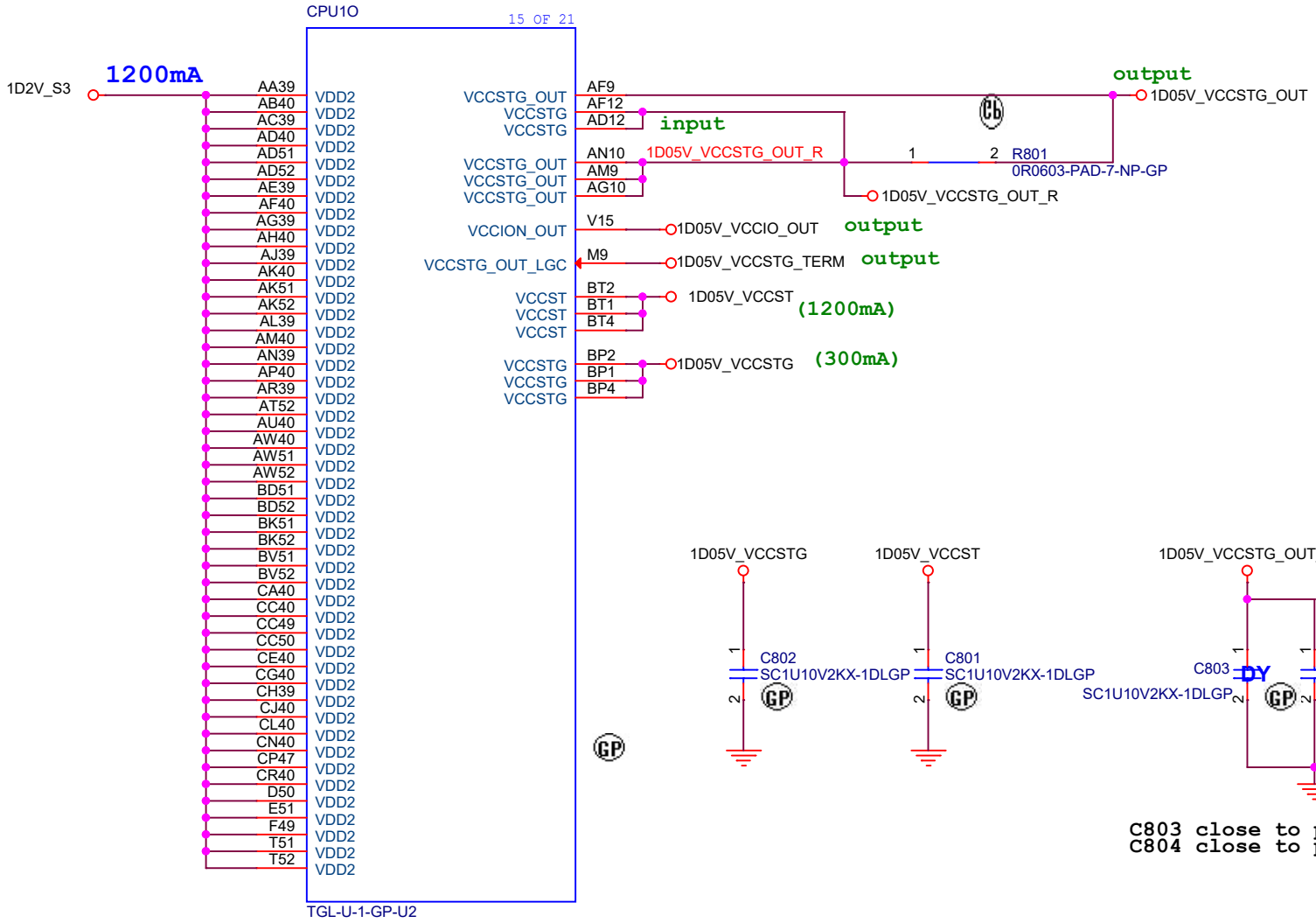
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN/VID)

Size	Document Number	Rev
A4	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 7 of 105

Main Func = CPU



Lack of VCCPLL_OC / VCC1P8A / VCCPLL

<Core Design>

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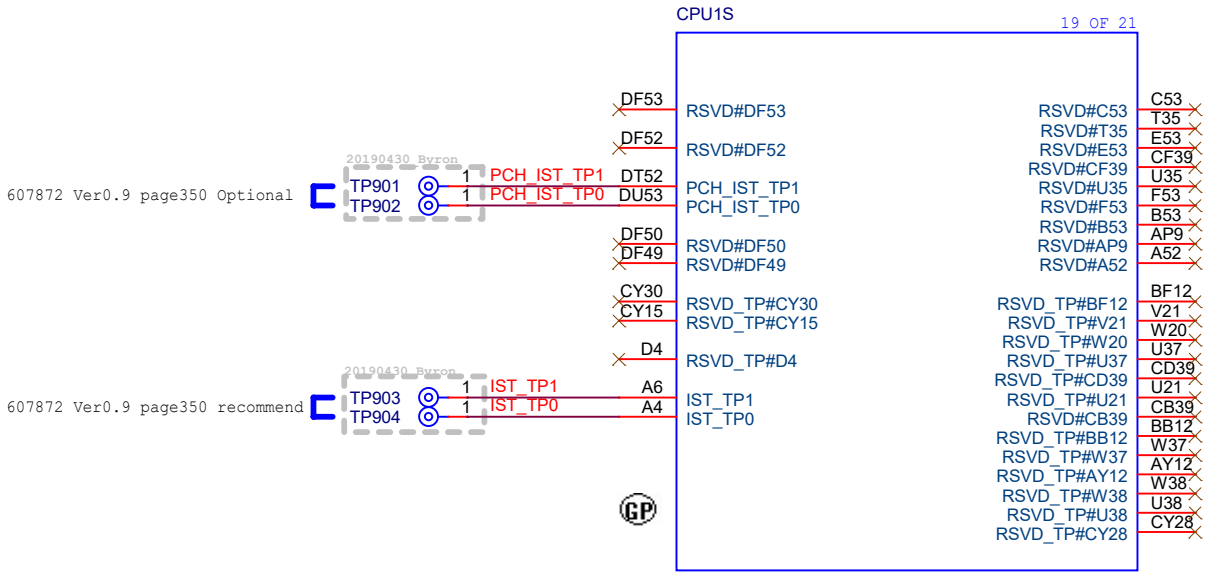
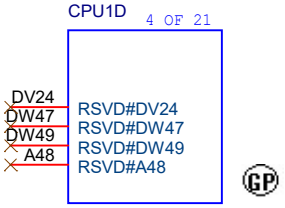
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VDDQ/VCC/VCCST/VCCSTG)	
Size A4	Document Number Cyborg TGL	Rev SC
Date: Thursday, January 14, 2021	Sheet 8 of 105	





<Core Design>

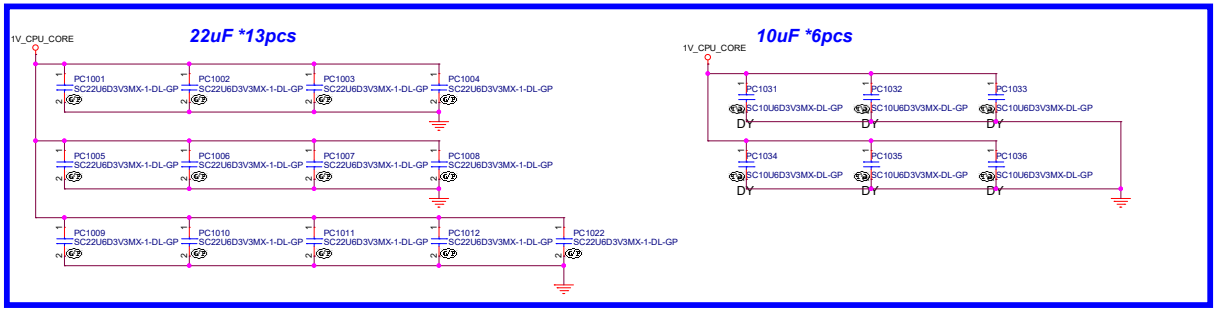
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

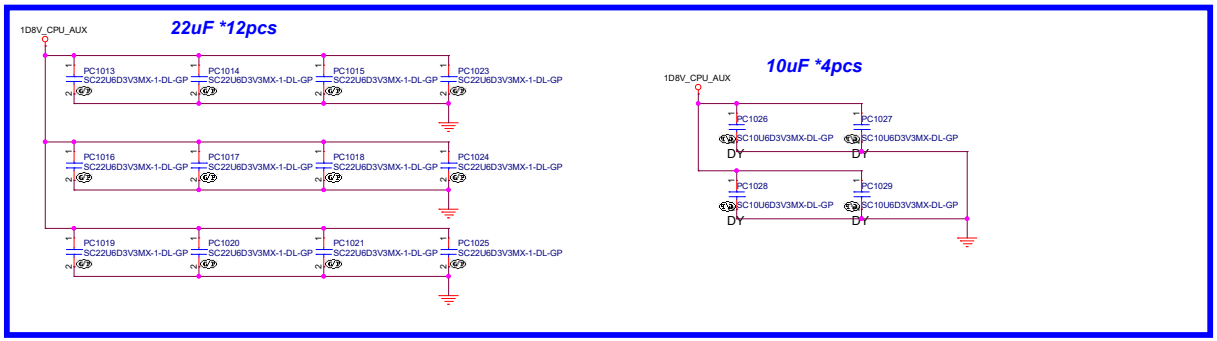
Title: CPU (RSVD)

Size	Document Number	Rev
A4	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 9 of 105

Main Func = CPU





<Core Design>

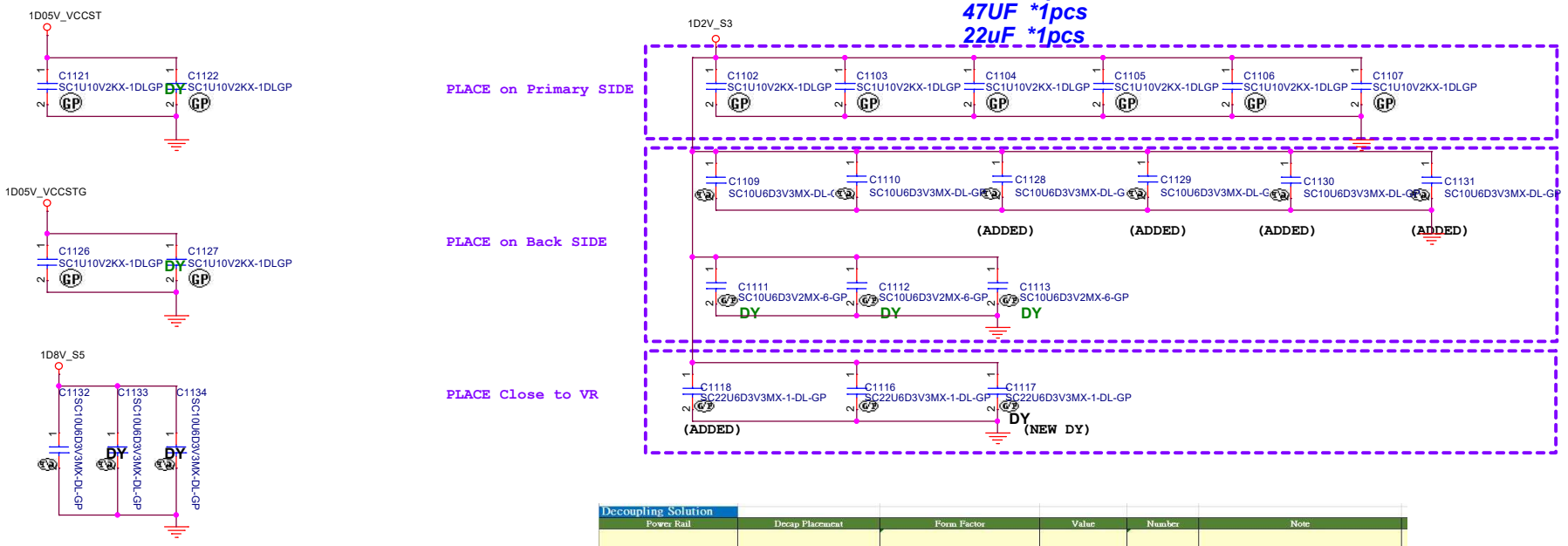
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet: 10 of 105

Main Func = CPU



11/5 Tery Don
add 1D8V_S5 decoupling cap. follow Shuri

Decoupling Solution

Power Rail	Decap Placement	Form Factor	Value	Number	Note
VCCDD2	Secondary Side	0402	10uF	8	Place on the back side of the SOC, as close as possible to the vias that connect to the outer row of BGA pins. Locate the capacitor such that the trace length from the GND via to the pad is minimized, and maximize the width of this trace.
	Primary Side	0603	47uF	2	Place them as close to the VR as possible. 2 caps should be stuffed.
		0402	1uF	8	Place on the primary side, as close as possible to the vias that connect to the outer row of SoC pins, use wide traces to connect the capacitor pins to the vias. Make sure to put atleast 1 via down near the outer Vdd2 BGA and 1 via down near the cap pad.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power Cap2)

Size: A3 | Document Number: Cyborg TGL | Rev: SC

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Main Func = MEMORY

10/15 Modify DIM1 DQ/DQS tuning. follow CRB

DM1A 1 OF 4

DDR4-260P-78-GP-U

062.10011.M001
2nd = 062.10011.M021
3rd = 062.10011.M003
4th = 062.10011.M013

M_A_DQ[56:63]
M_A_DQ[48:55]
M_A_DQ[40:47]
M_A_DQ[32:39]
M_A_DQ[8:15]
M_A_DQ[0:7]
M_A_DQ[24:31]
M_A_DQ[16:23]

DM1B 2 OF 4

DDR4-260P-78-GP-U

062.10011.M001

DM1C 3 OF 4

DDR4-260P-78-GP-U

062.10011.M001

DM1D 4 OF 4

DDR4-260P-78-GP-U

062.10011.M001

10uF *8pcs (DY *3)
1uF *8pcs (DY *3)
2.2uF *1pcs (DY *1)
0.1uF *1pcs (DY *1)

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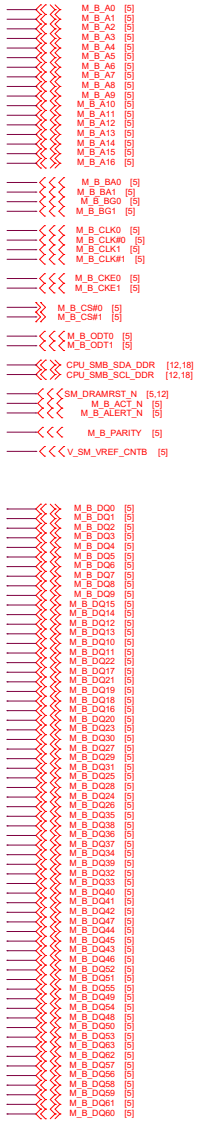
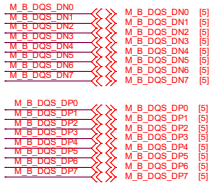
<Core Design>

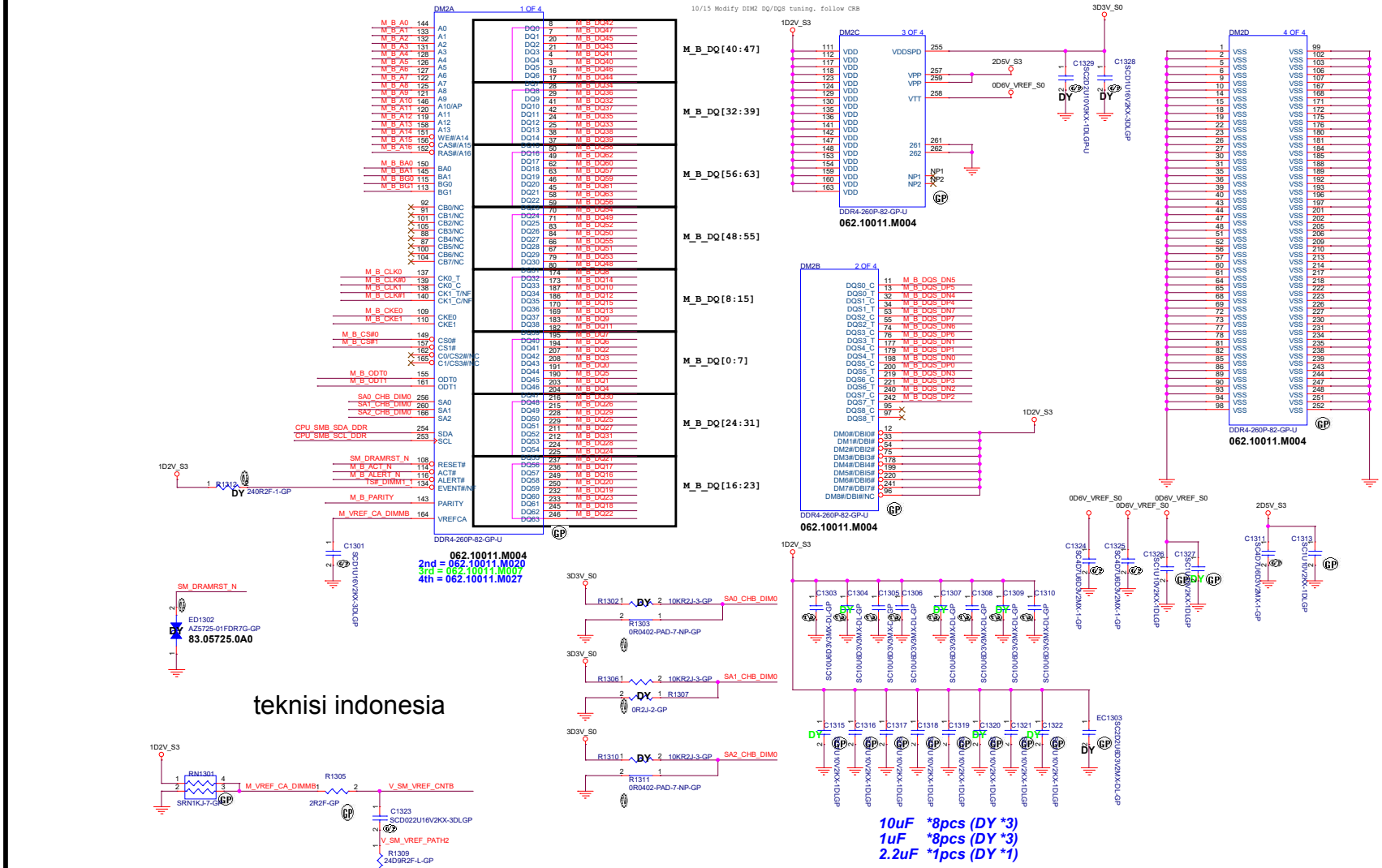
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 12 of 105

Main Func = MEMORY







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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 13 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

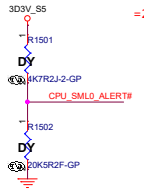
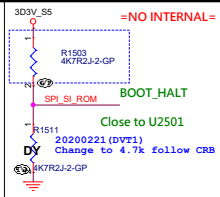
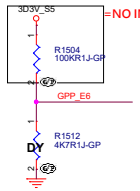
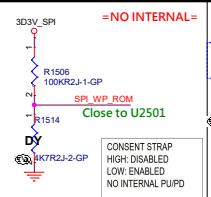
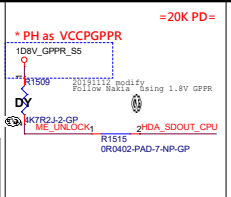
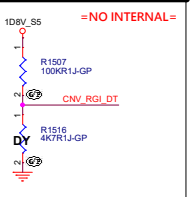
Title: ***DDR (RSVD) (DDR4-CHA1)***

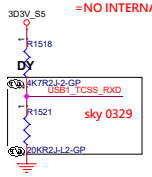
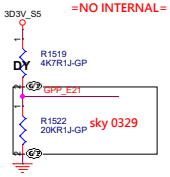
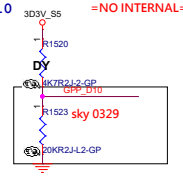
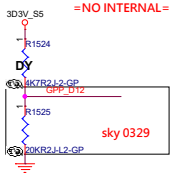
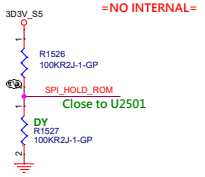
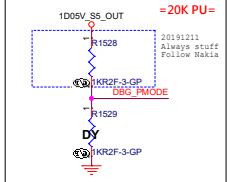
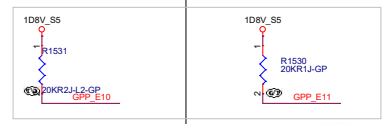
Size	Document Number	Rev
A4	***Cyborg TGL***	***SC***

Date: Thursday, January 14, 2021 Sheet 14 of 105

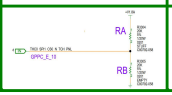
[18,24,25,91] SPI_SI_ROM
[18,24,25] SPI_WP_ROM
[18,24,25] SPI_HOLD_ROM

[21] CNV_RGI_DT
[18] CPU_SML0_ALERT#
[18] GPP_E6
[19] HDA_SDOUT_CPU
[4,71] USB1_TCSS_RXD
[4] GPP_D10
[3] DBG_PMODE
[4] GPP_D12
[4] GPP_E21
[18] GPP_E10
[18] GPP_E11

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic				=20K PD=			
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	A0		GPP_E10	GPP_E11
Schematic								
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

Original Ref.

GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH - DISABLED LOW- ENABLED NO INTERNAL PU/PD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PU/PD	CPUNSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESCRIPTOR SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PU/PD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD
TBT LSX #1	**TBT LSX #2**	**TBT LSX #3**	**A0**	**GPP_E10**	**GPP_E11**		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PU/PD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD				

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
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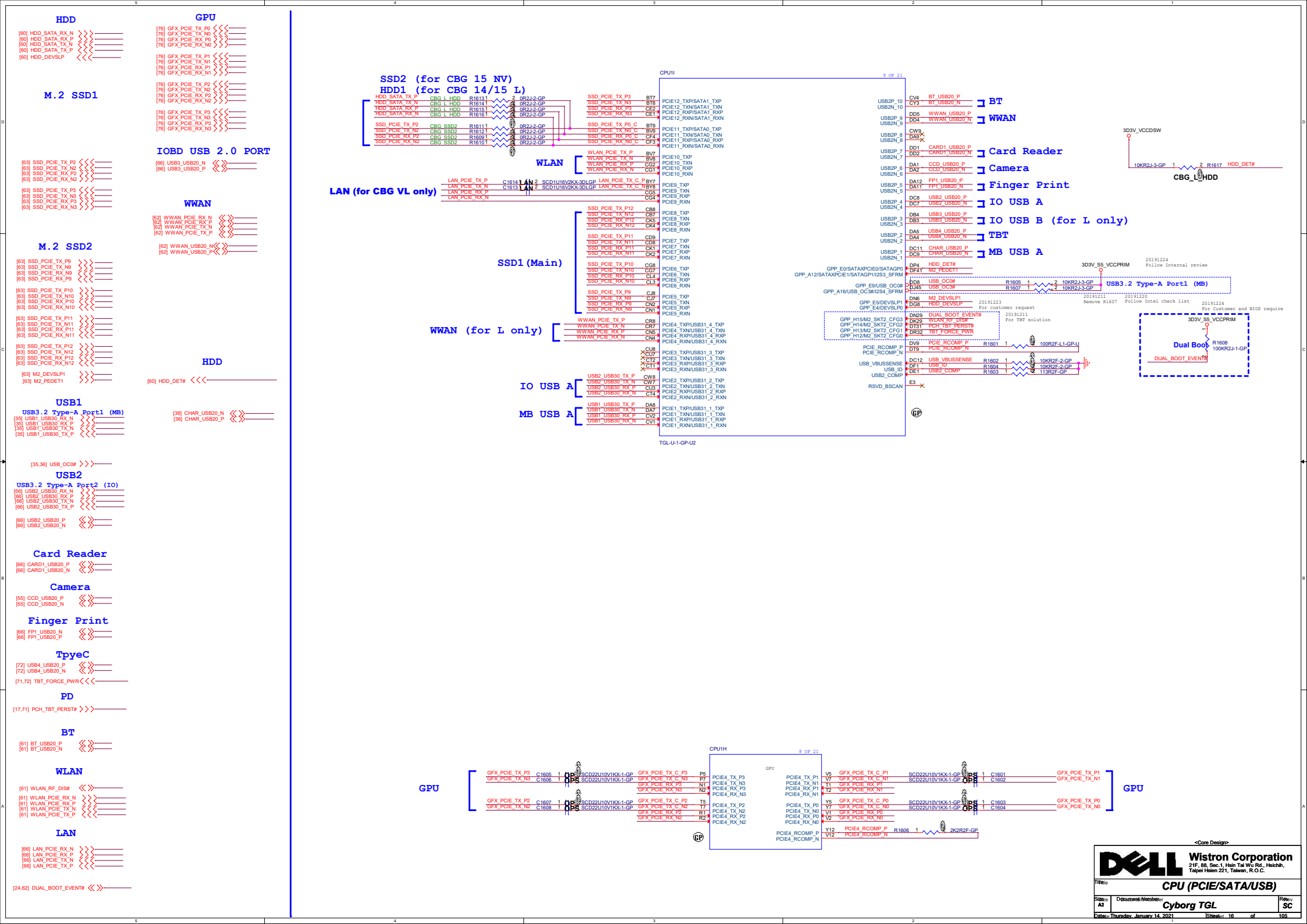
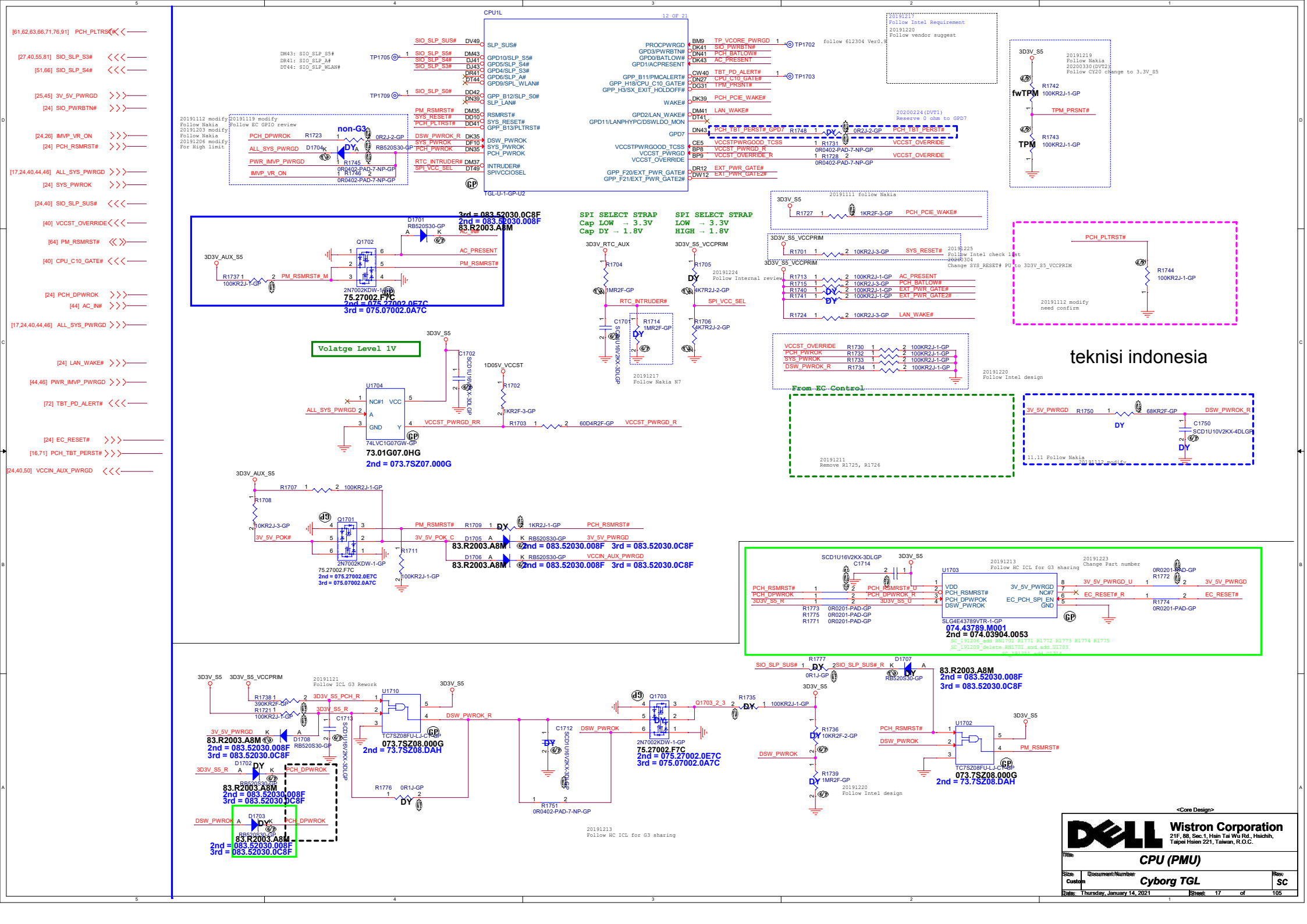


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 16 of 105



SPI ROM

[24,25,91] SPI_CLK_ROM
[15,24,25] SPI_HOLD_ROM
[15,24,25] SPI_WP_ROM
[24,25,91] SPI_SO_ROM
[15,24,25,91] SPI_SI_ROM
[24,25] SPI_CS_ROM_N0
[24,25] SPI_CS_ROM_N1
[91] SPI_CS_ROM_N2

[17,64] PM_RSMRST#

BIOS ROM_16

EC

[24,68] ESPI_IO0
[24,68] ESPI_IO1
[24,68] ESPI_IO2
[24,68] ESPI_IO3

[24,68] ESPI_CS#
[24,68] ESPI_RESET#
[24,68] ESPI_CLK

Audio

[29] SPK_ID

M.2 SSD

[63] SSD_CLK_CPU_N
[63] SSD_CLK_CPU_P
[63] SSD_CLKREQ_CPU_N
[64] SATA_LED#

[63] SSD2_CLK_CPU_P
[63] SSD2_CLK_CPU_N
[63] SSD2_CLKREQ_CPU_N

GPU

[76] GFX_CLK_CPU_N
[76] GFX_CLK_CPU_P
[76] CLK_PCIE_PEG_REQ#

[76] DGPU_HOLD_RST#
[79,86] GC6_FB_EN

SMBUS

[12,13] CPU_SMB_SCL_DDR
[12,13] CPU_SMB_SDA_DDR

[72] CPU_SML_SCL1_PD
[72] CPU_SML_SDA1_PD
[24,71] CPU_SML_SCL0
[24,71] CPU_SML_SDA0

[24] EC_I2C_SCL_THM
[24] EC_I2C_SDA_THM

OTHER

[24,61] SUSCLK

HW STRAP

[15] CPU_SML0_ALERT#
[15] GPP_E6
[15] GPP_E10
[15] GPP_E11

LAN

[66] LAN_CLK_CPU_N
[66] LAN_CLK_CPU_P
[66] CLK_PCIE_LAN_REQ#

WLAN

[61] WLAN_CLK_CPU_P
[61] WLAN_CLK_CPU_N
[61] CLK_PCIE_WLAN_REQ#

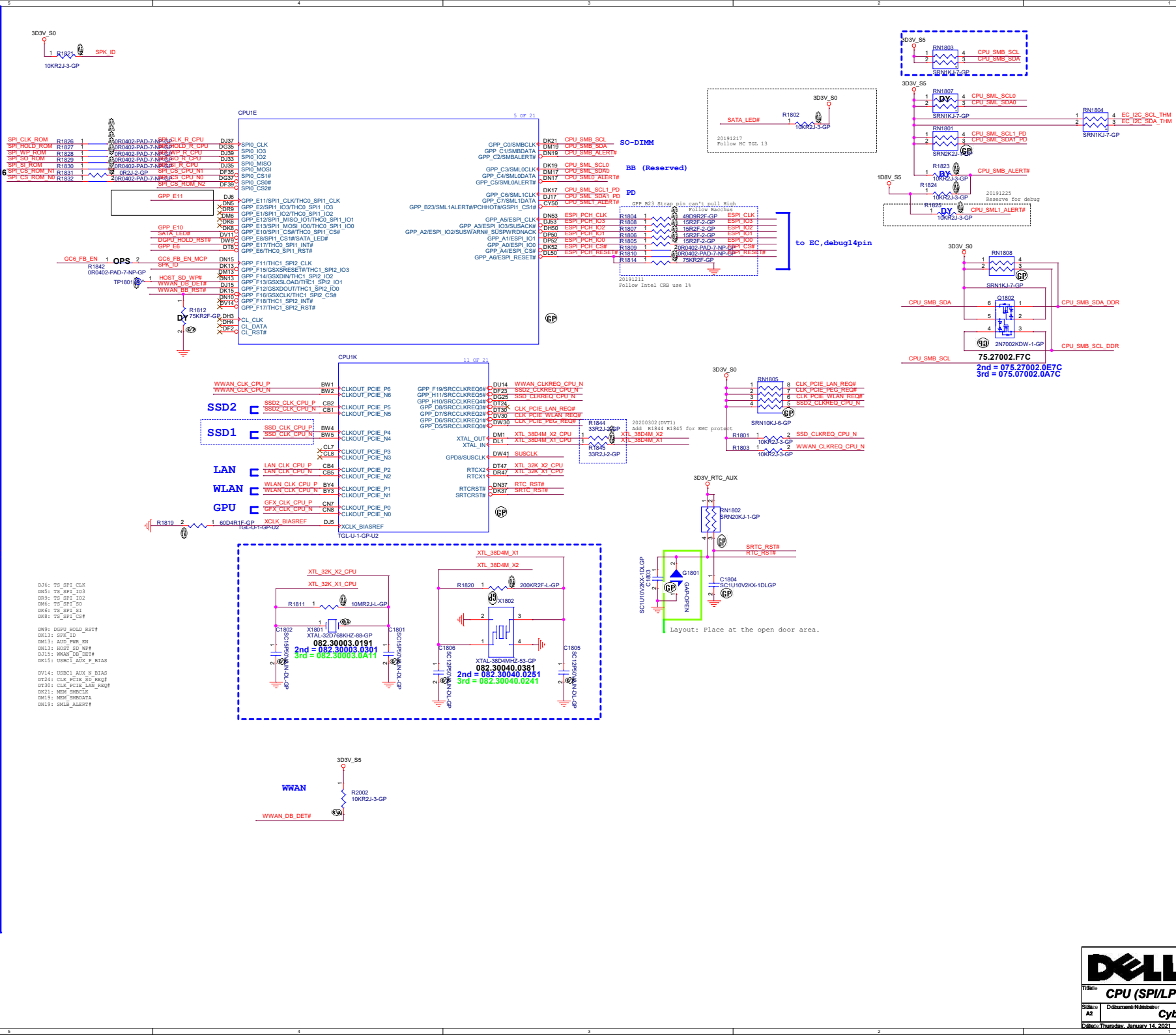
WWAN 0508

[62] WWAN_CLKREQ_CPU_N
[62] WWAN_CLK_CPU_N
[62] WWAN_CLK_CPU_P

[62] WWAN_BB_RST#

SITP

[62] WWAN_DB_DET#



<core_design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SPI/LPC/SMBS/XTAL/CLK)

Size: A2 | Document Number: Cyborg TGL | Rev: SC

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Audio

[27] HDA_SYNC_CODEC
[27] HDA_BITCLK_CODEC
[27] HDA_SDOUT_CODEC
[27] HDA_SDIN0_CPU
[15] HDA_SDOUT_CPU
[55] DMIC_PCH_CLK_Q
[55] DMIC_PCH_DATA_Q

GPU

[24,85] DGPU_PWROK
[86] DGPU_PWR_EN

G SENSOR

[70] FFS_INT2

RTC

[25] RTC_DET#

BT

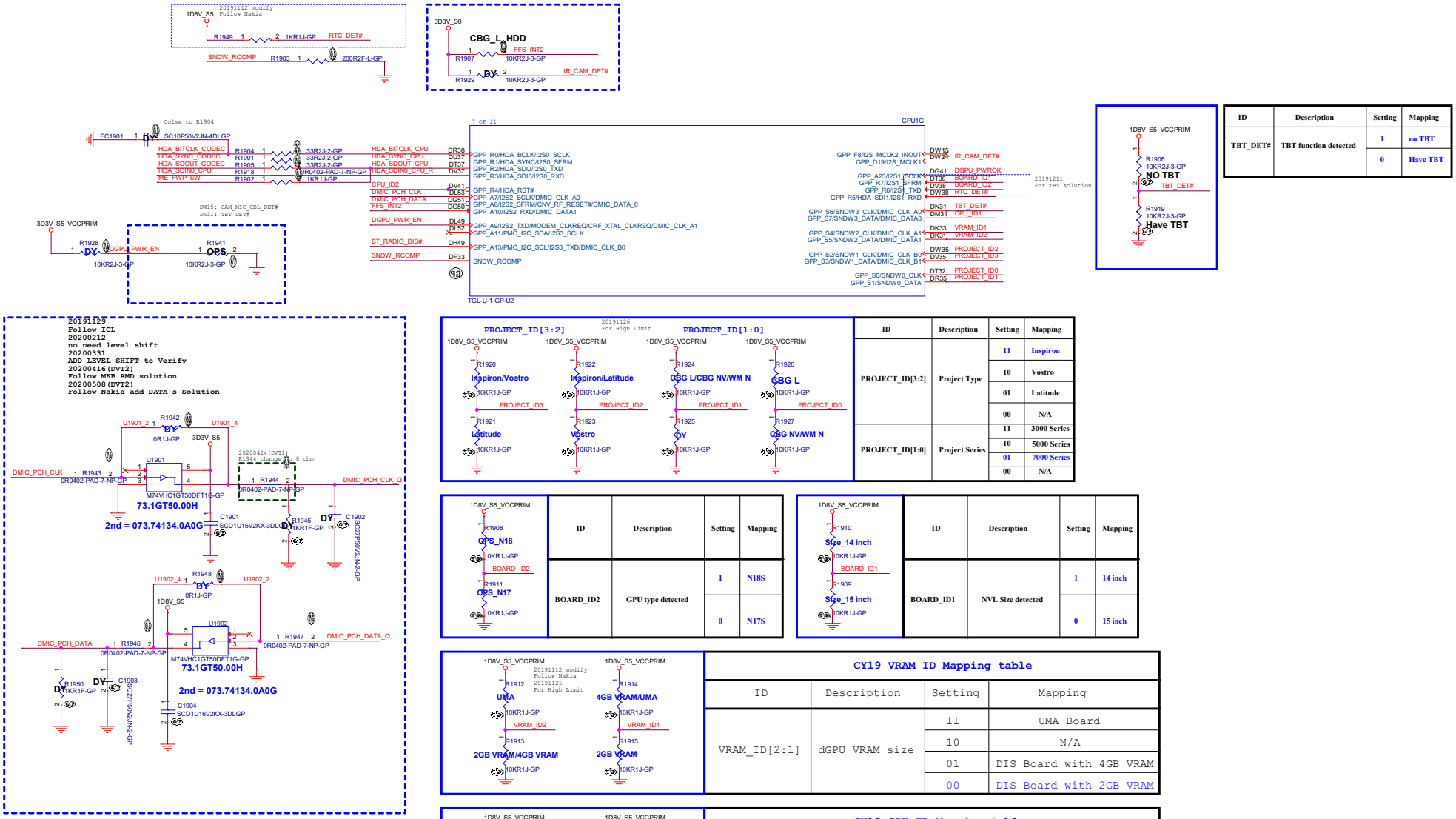
[61] BT_RADIO_DIS#

ME

[98] ME_FWP_SW

For SITP

[55] IR_CAM_DET#



ID	Description	Setting	Mapping
TBT_DET#	TBT function detected	1	no TBT
		0	Have TBT

20191129
Follow ICL
20200212
no need level shift
20200331
ADD LEVEL SHIFT to Verify
20200416(DVT2)
Follow MKB AMD solution
20200508(DVT2)
Follow Nakia add DATA's Solution

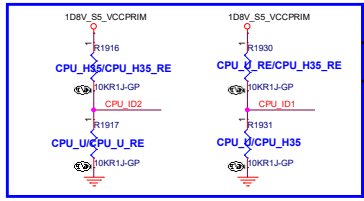
ID	Description	Setting	Mapping
PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Series
		10	5000 Series
		01	7000 Series
		00	N/A

ID	Description	Setting	Mapping
BOARD_ID2	GPU type detected	1	N18S
		0	N17S

ID	Description	Setting	Mapping
BOARD_ID1	NVL Size detected	1	14 inch
		0	15 inch

CY19 VRAM ID Mapping table

ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UMA Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



CY19 CPU ID Mapping table

ID	Description	Setting	Mapping
CPU_ID[2:1]	CPU type Select	11	TGL-H35 Re-flash
		10	TGL-H35
		01	TGL-UP3 Re-flash
		00	TGL-UP3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
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TOUCH PAD/E3

[65,66] CPU_I2C_SCL_P0
[65,66] CPU_I2C_SDA_P0

G SENSOR

[70] FFS_INT1

[55,70] SENSOR_I2C_SDA
[55,70] SENSOR_I2C_SCL

[70] GSEN2_INT1_C
[55] GSEN_INT1_C

AUDIO

[24,27] SPKR

KEYBOARD

[65] KB_LED_BL_DET

OTHER

[24] TABLE_MODE#
[24] NB_MODE#
[91] TPM_SPI_IRQ#

PD

[71] PCH_I2C_SCL_TBT
[71] PCH_I2C_SDA_TBT

eDP

[55] DBC_PANEL_EN

LID

[24,66] LID_CL_SIO#
[24,66] LID_CL_SIO_TAB#

[68] CPU_UART2_TXD
[68] CPU_UART2_RXD

TOUCH

[55] PCH_I2C0_SDA_TS
[55] PCH_I2C0_SCL_TS

[55] TOUCH_PANEL_INTR#

[24,64] MASK_SATA_LED#
[64] SATA_LED#_D
[24,64] BATT_WHITE_LED#

WWAN

[66] IO_DB_DET#_GPPG5
[66] LOM_CABLE_DETECT#

[55] LCD_CBL_DET#

20200304
KB_LED_BL_DET , GPP_C10 -> GPP_D16
Internal review , follow Nakia
Follow GPIO table

20191129
layout design

3D3V_S0

RN2005
CPU_I2C_SCL_ISH0
CPU_I2C_SDA_ISH0
SRN2K2J-1-GP 20191125
Follow Upsell

3D3V_VCCDSW

10KR2J-3-GP R2001 LCD_CBL_DET#

PAID_L

CPU1F
6 OF 21

SPKR
TPM_SPI_IRQ#
GC6_THM_DIS#_PCH
FFS_INT1
LCD_CBL_DET#
CPU_UART2_TXD
CPU_UART2_RXD
TOUCH_PANEL_INTR#
PCH_I2C0_SCL_TS
PCH_I2C0_SDA_TS
CPU_I2C_SCL_P0
CPU_I2C_SDA_P0
DBC_PANEL_EN
LOM_CABLE_DETECT#

GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

TGL-U-1-GP-U2

TP2010

GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/IMGCLKOUT1
KB_LED_BL_DET
IO_DB_DET#_GPPG5
GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7
GPP_E15/ISH_GP6
GPP_D18/ISH_GP5
GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCOMP
GPP_T3/I2C7_SCL
GPP_T2/I2C7_SDA
GPP_U5/GSPI3_CLK
GPP_U4/GSPI3_CS0#

celerometer sensor
SENSOR_I2C_SCL
SENSOR_I2C_SDA
ISH

20200113 DVT1
Follow Customer CY20 change from I2C2 to I2C5

PCH_I2C_SCL_TBT
PCH_I2C_SDA_TBT
PCH to BB
SDA/SCL Pull UP on BB side(page71)

20191125
Follow CY20

LID_CL_SIO_TAB#
ISH_LID_CLS_NB
ISH_NB_MODE
ISH_TABLE_MODE#
ISH_ACC2_INT#
ISH_ACC1_INT#
GPP_RCOMP

20191210
Follow CY20

LID_CL_SIO#
100KR2J-1-GP
TABLE_MODE#
GSEN2_INT1_C
GSEN_INT1_C
FFS
G Sensor
200R2F-L-GP

PCH to Touch Screen
SDA/SCL/INT Pull UP on PD side(page72)

PCH to Touch Pad/E3
SDA/SCL/INT Pull UP on TP side(page65)

3D3V_S0
20200420(DVT2)
Follow ICL reserved 3.3V PH
R2058
FFS_INT1
10KR2J-3-GP

Q2001
ISH_NB_MODE
BATT_WHITE_LED#
NB_MODE#
MASK_SATA_LED#
SATA_LED#_D
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.07002.0A7C

3D3V_S5
R2050
10KR2J-3-GP
NB_MODE#

	NB_MODE	LID_CL_SIO_TAB#	
NB Mode	1	1	KB可以動
Tablet Mode	don´t care	0	KB鎖住
Clam Shell Mode	0	1	KB鎖住

DA51: NRB_BIT
DC49: VGA_DB_DET#
CY49: TPM_PIRQ#
CY53: GC6_THM_DIS#_PCH
CY52: PCH_3.3V_TS_EN
DA50: HDD_FALL_INT
DV21: SBIOS_TX
DR21: USBC0_AUX_N_BIAS
DW21: USBC0_AUX_P_BIAS
DV19: DGPU_MACO_EN
DT19: SIO_EXT_WAKE#
DR18: PCH_HDD_EN
DU19: LCD_CBL_DET#
DG23: cTPM_PRSNT#
DJ19: TOUCH_PANEL_INTR#
DF21: TOUCH_I2C_DET#
DV18: I2C0_SCL_TS
DW18: I2C0_SDA_TS
DF29: DBC_PANEL_EN
DG29: LOM_CABLE_DETECT#
DF25: CNV_COEX1
DF27: CNV_COEX2
DR27: STYLUS_PWR_OCP#
DW27: CAM_SHUTTER#
DY25: IO_DB_DET#
CY39: ISH_I2C1_ALS_SCL
DB47: ISH_I2C1_ALS_SDA
DD47: ISH_I2C2_SCL
DD44: ISH_I2C2_SDA
DJ8: ISH_P_SENSOR_INT#
DV31: ISH_ALS_INT#
DG17: ZPODD_PWR_EN#
DG19: ZPODD_DA#

<Core Design>

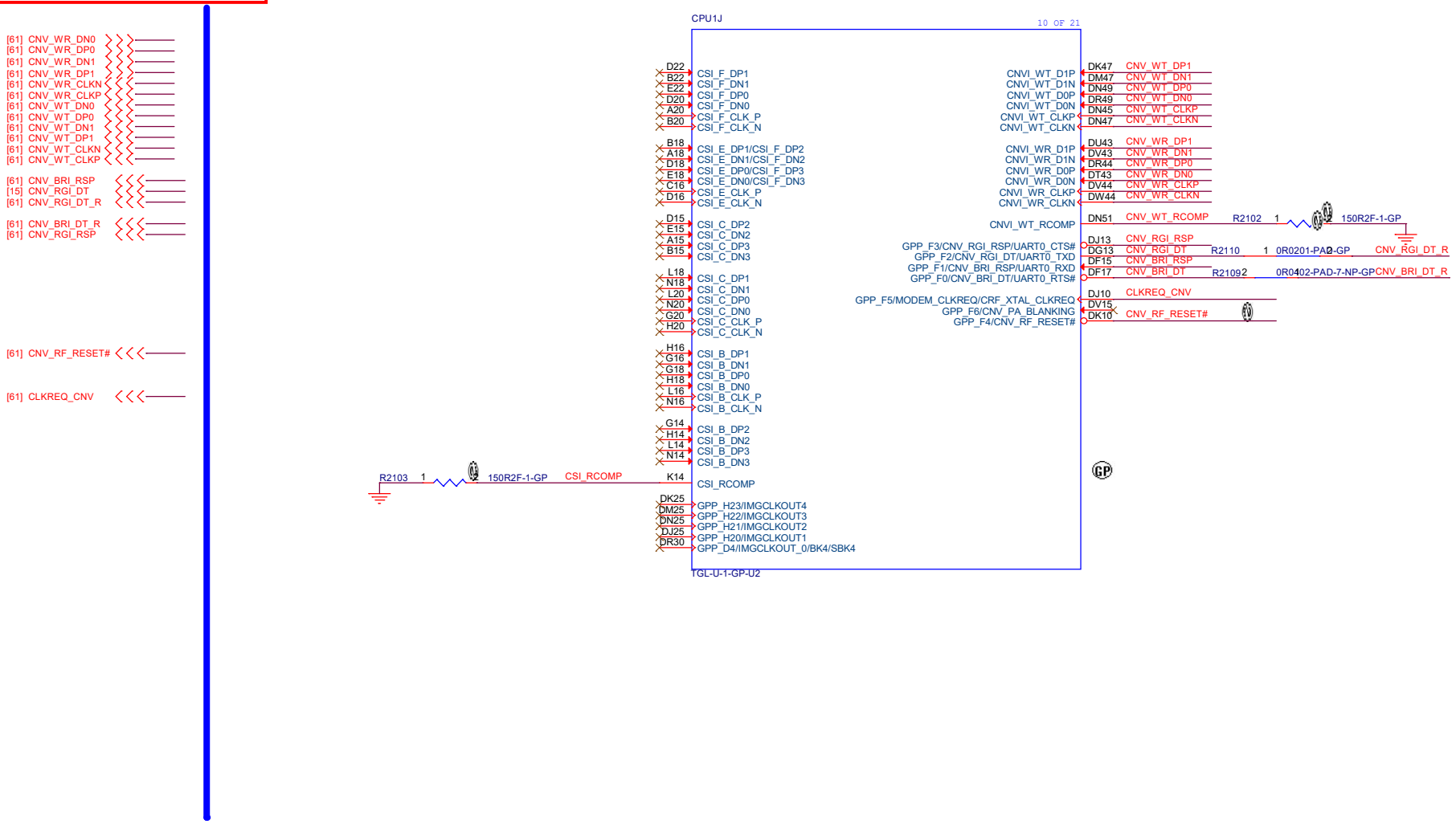
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 20 of 105

Main Func = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVi)

Size: A3 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 21 of 105

[50] VCCAUX_SENSE
[50] VSSAUX_SENSE
[40,50] CORE_VID0
[40,50] CORE_VID1
[3,24,44,46,72] PROCHOT#_CPU
[40] V1P05_CTRL_R
[40] VNN_CTRL_R

CPU1N
14 OF 21
1D8V_CPU_AUX

AB12 VCCIN_AUX
AC10 VCCIN_AUX
AE10 VCCIN_AUX
AK2 VCCIN_AUX
AR10 VCCIN_AUX
AT12 VCCIN_AUX
AU10 VCCIN_AUX
AW10 VCCIN_AUX
BV1 VCCIN_AUX
BV39 VCCIN_AUX
BW40 VCCIN_AUX
BY39 VCCIN_AUX
CC1 VCCIN_AUX
CD12 VCCIN_AUX
CF10 VCCIN_AUX
CG12 VCCIN_AUX
CH10 VCCIN_AUX
CJ1 VCCIN_AUX
CJ12 VCCIN_AUX
CK10 VCCIN_AUX
CL12 VCCIN_AUX
CM10 VCCIN_AUX
CP1 VCCIN_AUX
CP10 VCCIN_AUX
CR12 VCCIN_AUX
CT10 VCCIN_AUX
CU12 VCCIN_AUX
CY1 VCCIN_AUX
AK1 VCCIN_AUX

PH/PL 100R at VR side.

VSSAUX_SENSE AV9 VCCIN_AUX_VSSSENSE
VCCAUX_SENSE AT9 VCCIN_AUX_VCCSENSE

20191224
Follow Internal review
(200mA) 1D05V_VNN_BYPASS
DD17 VCC_VNNEXT_1P05
DD18 VCC_VNNEXT_1P05

3D3V_S5_VCCPRIM
(200mA) 1D05V_S5_BYPASS
DA15 VCC_V1P05EXT_1P05
DA17 VCC_V1P05EXT_1P05

R2215 1 1 10KR2J-3-GP VRALERT# DB39 GPP_B2/VRALERT#
VNN_CTRL_R
R2212 1 1 DY 2 0R2J-2-GP VNN_CTRL DV12 GPP_F22/VNN_CTRL
V1P05_CTRL_R R2213 1 2 V1P05_CTRL DT12 GPP_F23/V1P05_CTRL
0R0402-PAD-7-NP-GP
20191112 modify
Follow Nakia
CORE_VID0 DB37 GPP_B0/CORE_VID0
CORE_VID1 DB38 GPP_B1/CORE_VID1

D2201
RB520S30-GP
PROCHOT#_CPU A K VRALERT#
20191210
Follow Nakia N7
Intel CRB and Intel review
83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

TGL-U-1-GP-U2

(1.3A)
1D8V_S5_VCCPRIM
R2203 1 2 1D8V_S5
0R0805-PAD-NP-GP

CY18 VCCPRIM_1P8
CY20 VCCPRIM_1P8
CY24 VCCPRIM_1P8
CY26 VCCPRIM_1P8
DA18 VCCPRIM_1P8
DA20 VCCPRIM_1P8
DA22 VCCPRIM_1P8
DA24 VCCPRIM_1P8
DA26 VCCPRIM_1P8
DC18 VCCPRIM_1P8
DC20 VCCPRIM_1P8
DC22 VCCPRIM_1P8
DC24 VCCPRIM_1P8
DC26 VCCPRIM_1P8
DD20 VCCPRIM_1P8
DD22 VCCPRIM_1P8
DV22 VCCPRIM_1P8

(200mA) 3D3V_S5_VCCPRIM
20191112 modify

DA35 VCCPRIM_3P3
DC28 VCCPRIM_3P3
DC30 VCCPRIM_3P3
DD30 VCCPRIM_3P3

DV34 DCPRTC 3D3V_RTC_EXT
DV46 VCCLDOSTD_0P85 0D85V_S5_VCCLDOSTD_OUT
DV16 VCCA_CLKLDO_1P8 1D8V_S5_CLKLDO (165mA)
DC15 VCCA_CLKLDO_1P8
DV28 VCCDPHY_1P24 1D24V_S5_VCCDPHY_OUT
DD38 VCCDSW_1P05 1D05V_S5_VCCDSW_OUT
BR3 VCC1P05 1D05V_S5_OUT (1.5A)
BR4 VCC1P05
BT5 VCC1P05

Supply to VCCST & VCCSTG

DA31 VCCPRIM1P05_OUT_PCH 1D05V_S5_VCCPRIM_OUT (Output)
DC33 VCCPRIM1P05_OUT_PCH
DC31 VCCPRIM1P05_OUT_PCH

DC35 VCCRTC 3D3V_RTC_AUX
DD37 VCCDSW_3P3 3D3V_VCCDSW
DA28 VCCPGPPR 1D8V_GPPR_S5

VCCGPPR
3.3V or 1.8V

CY31 VCCPRIM_3P3 3D3V_S5_VCCPRIM
CY33 VCCPRIM_3P3
CV39 VCCPRIM_3P3 1D8V_S5_VCCPRIM
VCCPRIM_1P8

AP12 RSVD#AP12 TP_VCCANA_EHV 1 TP2201

3D3V_VCCDSW
20191112 modify
20191211
Follow Nakia
(1.3A)
R2202 1 2 DY 0R2J-2-GP 3D3V_S5
1D8V_S5
R2207 0R0402-PAD-7-NP-GP
Follow Nakia using 1.8V GPPR

Trace width > 40mil
1D05V_S5_VCCDSW_OUT
C2204 SC1U10V2KX-1DLGP

Place cap within 3mm from SOC edge
1D24V_S5_VCCDPHY_OUT
20191126
For High Limit
For CNVi C2205 SC4D7U6D3V2MX-1-GP

Place cap within 3mm from SOC edge
0D85V_S5_VCCLDOSTD_OUT
20191126
For High Limit
C2213 SC2D2U6D3V2MX-DL-GP
20200504(DVT2)
C2213 change to common

Must take care this power layout and add shield GND.
1D8V_S5
1D8V_S5_CLKLDO
(165mA)
R2204 0R0402-PAD-7-NP-GP
C2215 SC22U6D3V2MX-1-DLGP
C2216 SC22U6D3V2MX-1-DLGP

PH Same as SPI Programming Guide for details
1D8V_S5
RN2201
1 2 4 3 CORE_VID0 CORE_VID1
SRN10KJ-5-GP
10/09,RN2201 Pin3 ->CORE_VID1,charon
20191112 modify
Follow Nakia

(1.3A)
1D8V_S5_VCCPRIM
C2210 DY C2211 DY
SC1U10V2KX-1DLGP SC1U10V2KX-1DLGP

3D3V_S5_VCCPRIM
C2201 DY C2202
SC1U10V2KX-1DLGP SCD1U16V2KX-3DLGP

3D3V_RTC_AUX
C2206 C2207
SC1U10V2KX-1DLGP SCD1U16V2KX-3DLGP

3D3V_RTC_EXT
C2248
SCD1U16V2KX-3DLGP

1D05V_S5_VCCPRIM_OUT
C2203 DY
SC1U10V2KX-1DLGP

(200mA)
1D05V_S5_BYPASS
C2246 DY
SC1U10V2KX-1DLGP

(200mA)
1D05V_VNN_BYPASS
C2247 DY
SC1U10V2KX-1DLGP

(SR#1406479253)
20191112 modify
Follow Nakia

1D05V_S5_OUT
C2208 DY
SC1U10V2KX-1DLGP

3D3V_VCCDSW
C2209
SC1U10V2KX-1DLGP

20191112 modify
Follow Nakia using 1.8V GPPR
1D8V_GPPR_S5
DY C2214
SCD1U16V2KX-L-GP

Close to pin DD37

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)
Size: A3
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 22 of 105

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VSS)**

Size	Document Number	Rev
A4	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 23 of 105

Main Func = KBC

VTR Signal

For USB Charge Level shift

For USB TypeC

Board ID and Model ID

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	000	100.0K	10.0K	3
2	001	100.0K	17.8K	2.901
3	002	100.0K	27.0K	2.598
4	003(connect)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.806
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

#	MODEL ID (GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR (R2442)	VOLTAGE	
1	CBG-N-14&15 UMA	100k	100k	3	64.10025.6DL
2	CBG-V-14&15 UMA	100k	17.8k	2.801	64.17825.6DL
3	CBG-L-14&15 UMA	100k	27.0k	2.598	64.27025.6DL
4	WMN-N-14 UMA	100k	37.4k	2.402	64.37425.6DL
5		100k	49.9k	2.201	
6	CBG-N-14&15 DIS	100k	64.9k	2.001	64.64925.6DL
7	CBG-V-14&15 DIS	100k	82.5k	1.808	64.82525.6DL
8	CBG-L-14&15 DIS	100k	107k	1.594	64.10735.6DL
9	WMN-N-14 DIS	100k	154k	1.299	64.15435.6DL
10		100k	200k	1.1	

LED

Key Matrix

SMBUS Option

JTAG DEBUG CONN

Power Switch Logic(PSL)

G3 Sharing

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot Note 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM3/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT_P_IN1/SHD_IO3/CT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.

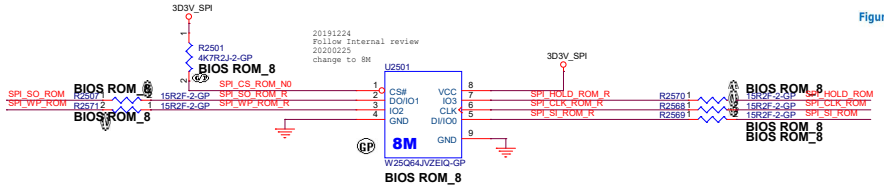
Wistron Corporation	DELL
KBC Nuvoton NPCE285PA0DX	
Cyborg TGL	sc

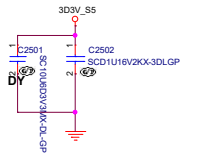
Main Func = SPI Flash

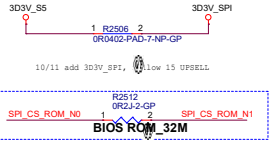
[18,24] SPI_CS_ROM_N1
[18,24] SPI_CS_ROM_N0
[18,24,91] SPI_SO_ROM
[18,24,91] SPI_CLK_ROM
[15,18,24,91] SPI_SI_ROM
[15,18,24] SPI_HOLD_ROM
[15,18,24] SPI_WP_ROM

Socket for 32M (WSON)

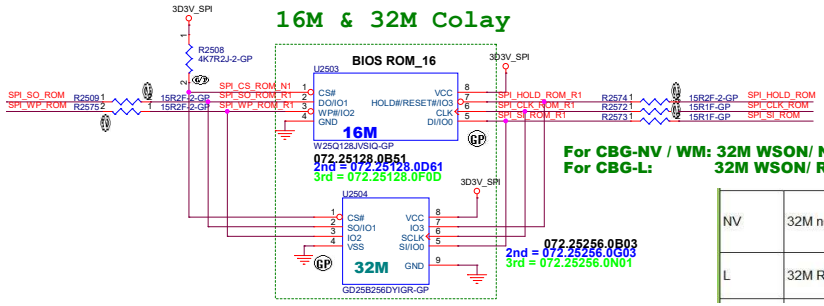
20200923 Remove







16M & 32M Colay

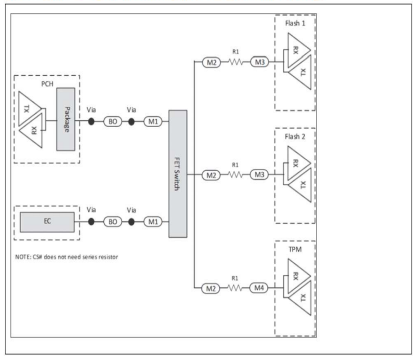


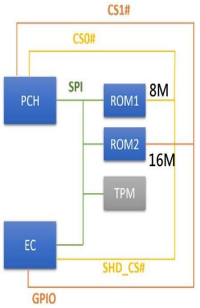
072.25128.0B51
2nd = 072.25128.0D61
3rd = 072.25128.0F0D

072.25256.0B03
2nd = 072.25256.0G03
3rd = 072.25256.0N01

For CBG-NV / WM: 32M WSON/ NON RPMC
For CBG-L: 32M WSON/ RPMC

Figure 217. SPI0 3-Load EC G3 Flash Sharing with FET Isolation Topology

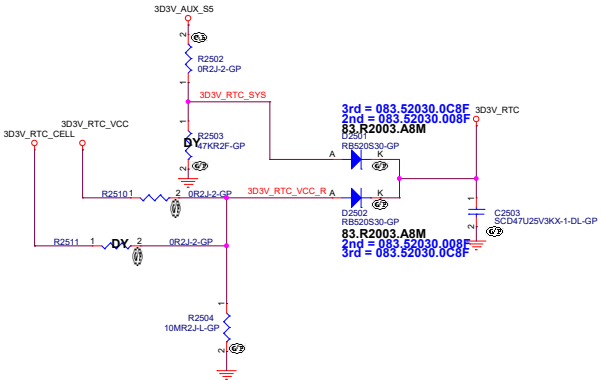




NV	32M non RPMC (WSON)	072.25256.0B03	GD		for I7+TBT	1st
		072.25256.0G03	XMC		for I7+TBT	2nd
		072.25673.0003	MXIC			1st
		072.25256.0N01	WINBOND			2nd
L	32M RPMC (WSON)	072.25256.0H03	GD			
		072.25256.0A91	XMC		remove	
		072.25256.0AA1	Winbond			

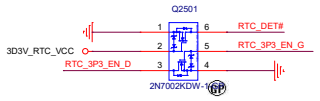
Main Func = RTC

[19] RTC_DET#
[24] VCCDSW_EN
[24] RTCRST_ON
[17,45] 3V_5V_PWRGD



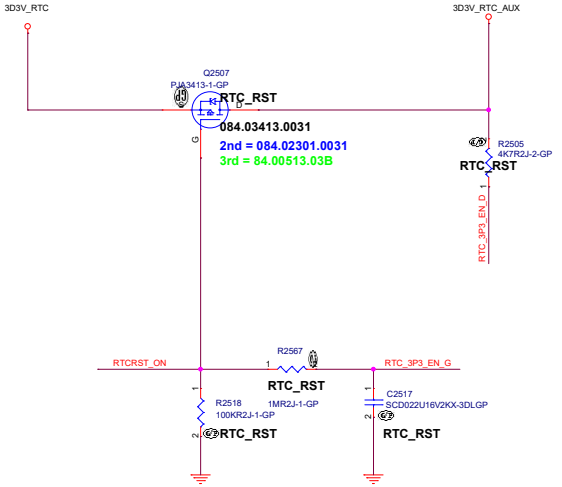
3rd = 083.52030.0C8F
2nd = 083.52030.008F
83.R2003.A8M

83.R2003.A8M
2nd = 083.52030.008F
3rd = 083.52030.0C8F

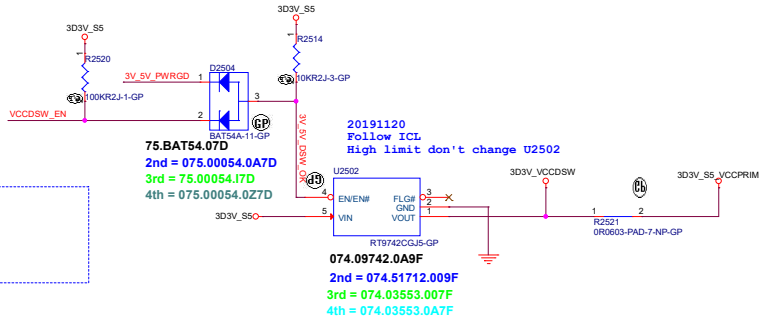


75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.07002.0A7C

20191120 follow Nakia



084.03413.0031
2nd = 084.02301.0031
3rd = 84.00513.03B



75.BAT54.07D
2nd = 075.00054.0A7D
3rd = 75.00054.I7D
4th = 075.00054.0Z7D

20191120
Follow ICL
High limit don't change U2502

074.09742.0A9F
2nd = 074.51712.009F
3rd = 074.03553.007F
4th = 074.03553.0A7F

20191224
Follow Internal review

20191111 follow Nakia

20191112 modify
Follow Nakia

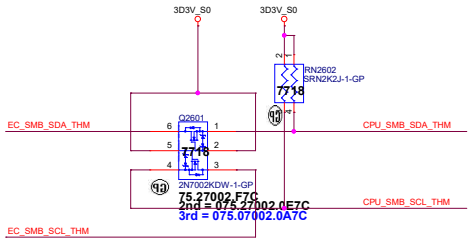
<Core Design>

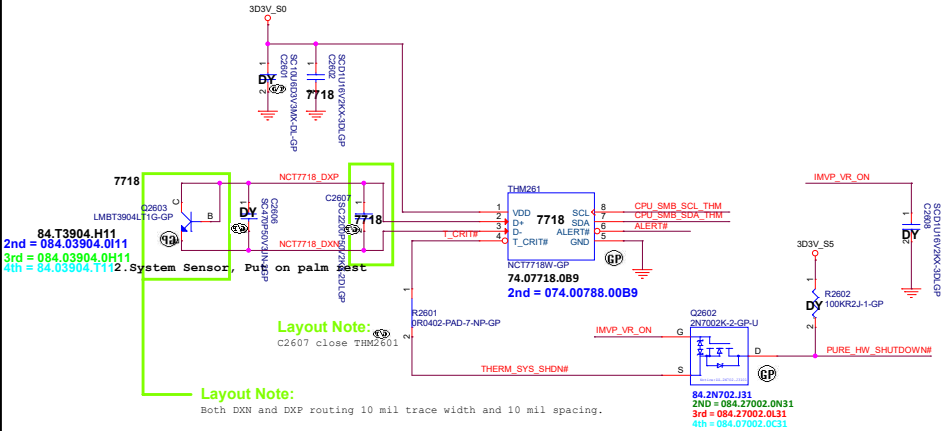
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

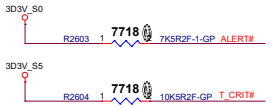
Title: Flash
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 25 of 105

Main Func = Thermal Sensor

[24,79] EC_SMB_SDA_THM
[24,79] EC_SMB_SCL_THM
[17,24] IMVP_VR_ON
[40] PURE_HW_SHUTDOWN#
[24] PWM_FAN1
[24] FAN_TACH1



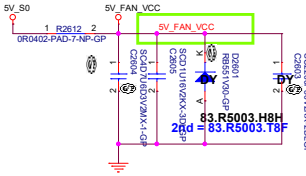


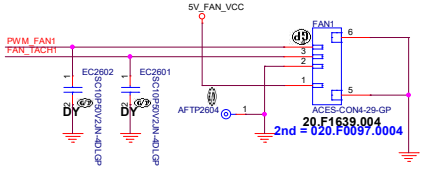


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1

Layout Note:
Signal Routing Guideline:
Trace width = 15mil





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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 26 of 105

Main Func = Audio

Audio Codec Chip ALC3204

[19] HDA_SDIN0_CPU
[19] HDA_SDOUT_CODEC
[19] HDA_SYNC_CODEC
[19] HDA_BITCLK_CODEC

[29] AUD_SPK_R+
[29] AUD_SPK_R-
[29] AUD_SPK_L+
[29] AUD_SPK_L-

[24] NB_Mute#
[20,24] SPKR
[24] BEEP
[66] AUD_SENSE
[29] LINE1_VREFO
[29] MIC2_VREFO
[29] AUD_HP1_JACK_L
[29] AUD_HP1_JACK_R
[29] LINE1_L
[29] LINE1_R
[29,66] AUD_SLEEVE
[29,66] AUD_RING
[55] DMIC_SCL_CODEC
[55] DMIC_SDA_CODEC
[17,40,55,81] SIO_SLP_S3#
[81] 1D8V_EN#

Analog
Digital
>2A
moat

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is unavailable, please make sure that switch frequency operates at out-band(over 20KHz)

ALC3204
QFN40 (5x5)
071.03204.0003

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Layout Note:
Place close to Pin 20

Layout Note:
Tied at point only under Codec or near the Codec

DVDD must >= DVDD_IO

place close to pin8

20191112 modify Follow Nakia

20191204
For Vendor request
20200302
Stuff R2717

20191128
Follow Nakia

For RTC Gen9 reset circuit change power rail.
20170921

Open drain output. pull up to DVDD or max. 5V

20191204
For Vendor request

Azalia I/F EMI

20191119
Follow ICL
High limit

150mA
Q2701 PJA3415AE-GP
084.03415.0C31
2nd = 84.03327.031

Q2702 PJE8408-R1-00001-GP
084.08408.0031
2nd = 084.00138.0E31

75.00054.A7D
2nd = 75.00054.T7D

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 27 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Cyborg TGL*	*SC*

Date: Thursday, January 14, 2021 Sheet 28 of 105

Main Func = Audio

[27] AUD_SPK_R+
[27] AUD_SPK_R-
[27] AUD_SPK_L-
[27] AUD_SPK_L+

[18] SPK_ID

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

AUD_SPK_L+ R2902 1 — 2 0R0603-PAD-7-NP-GP
AUD_SPK_L- R2901 1 — 2 0R0603-PAD-7-NP-GP
AUD_SPK_R- R2903 1 — 2 0R0603-PAD-7-NP-GP
AUD_SPK_R+ R2904 1 — 2 0R0603-PAD-7-NP-GP

AUD_SPK_R+_C
AUD_SPK_R-_C
AUD_SPK_L-_C
AUD_SPK_L+_C
SPK_ID

ED2901 AZ5725-01FDR7G-GP
ED2902 AZ5725-01FDR7G-GP
ED2903 AZ5725-01FDR7G-GP
ED2904 AZ5725-01FDR7G-GP
ED2905 AZ5725-01FDR7G-GP

EC2902 SC1KP50V2KX-1DLGP
EC2901 SC1KP50V2KX-1DLGP
EC2903 SC1KP50V2KX-1DLGP
EC2904 SC1KP50V2KX-1DLGP

83.05725.0A0 83.05725.0A0 83.05725.0A0
83.05725.0A0 83.05725.0A0

SPK1
AUD_SPK_L+_C 1
AUD_SPK_L-_C 2
AUD_SPK_R-_C 3
AUD_SPK_R+_C 4
SPK_ID 5
6
7
8
SPK6P
ACES-CON6-20-GP-U
20.F1639.006
2nd = 020.F1263.0006

SPK2
1
2
3
4
5
6
ACES-CON4-114-GP
020.F1796.M002
2nd = 020.F1794.M001
SPK4P

For CBG L only

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: VECO
0: ZY

AUD_SPK_L-_C 1 — AFTP2901
AUD_SPK_L+_C 1 — AFTP2902
AUD_SPK_R-_C 1 — AFTP2903
AUD_SPK_R+_C 1 — AFTP2904
SPK_ID 1 — AFTP2911

From Codec

[27] MIC2_VREFO
[27,29,66] AUD_RING
[27] AUD_HP1_JACK_L
[27] LINE1_L
[27] LINE1_R
[27] AUD_HP1_JACK_R
[27,29,66] AUD_SLEEVE
[27] LINE1_VREFO

To IO Board

[27,29,66] AUD_RING
[66] AUD_HP1_JACK_L1
[66] AUD_HP1_JACK_R1
[27,29,66] AUD_SLEEVE

Universal Jack (Moved to I/O Board)

MIC2_VREFO 2 — 1 RN2901 4 SRN2K2J-1-GP

AUD_HP1_JACK_L
LINE1_L C2907 1 — LINE1-L_C R2922 1 — 2 1KR2J-1-GP
SC10U6D3V3MX-DL-GP
LINE1_R C2908 1 — LINE1-L_R R2921 1 — 1KR2J-1-GP
AUD_HP1_JACK_R
SC10U6D3V3MX-DL-GP

R2908 1 — 2 10R2F-L-GP — AUD_RING / AUD_HP1_JACK_L1
R2910 1 — 2 10R2F-L-GP — AUD_HP1_JACK_R1 / AUD_SLEEVE

LINE1_VREFO
D2901 A — RB520S30-GP
LINE1_VREFO_D1 R2912 1 — 2 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

D2902 A — RB520S30-GP
LINE1_VREFO_D2 R2913 1 — 2 4K7R2J-2-GP
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F

<Core Design>

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Title: Audio IO
Size: A3 | Document Number: Cyborg TGL | Rev: SC
Date: Thursday, January 14, 2021 | Sheet 29 of 105

(Blanking)

<Core Design>

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***(Reserved)***		
Size: A4	Document Number: **Cyborg TGL**	Rev: **SC**
Date: Thursday, January 14, 2021	Sheet 30 of 105	

Main Func = LAN

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8106

Size: Custom | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 31 of 105

Main Func = LAN

<Core Design>

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Title: *XFOM&RJ45*

Size	Document Number	Rev
A3	*Cyborg TGL*	*SC*

Date: Thursday, January 14, 2021 Sheet 32 of 105

Main Func = Card Reader

<Core Design>

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Title

Card Reader-RTS5170

Size	Document Number	Rev
A4	*Cyborg TGL*	*SC*

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Main Func = USB2.0

<Core Design>

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Title: USB2.0 CONN

Size | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 34 of 105

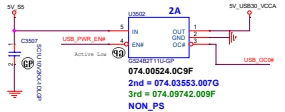
Main Func = USB3.0 Port1

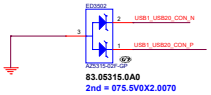
[24,66] USB_PWR_EN#

[16,36] USB_OC0#

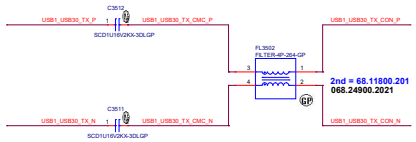
[36] USB1_USB20_N
[36] USB1_USB20_P

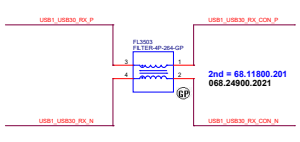
[16] USB1_USB30_TX_N
[16] USB1_USB30_TX_P
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P

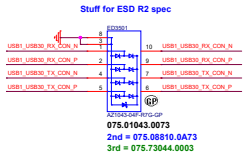




2020/02/29:swap EL3501

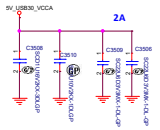




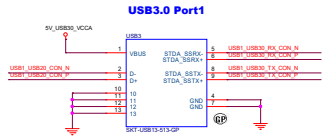


USB3.0 Port 1

Layout Note: Close USB3



USB3.0 Port1



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Title: USB3.0 CONN

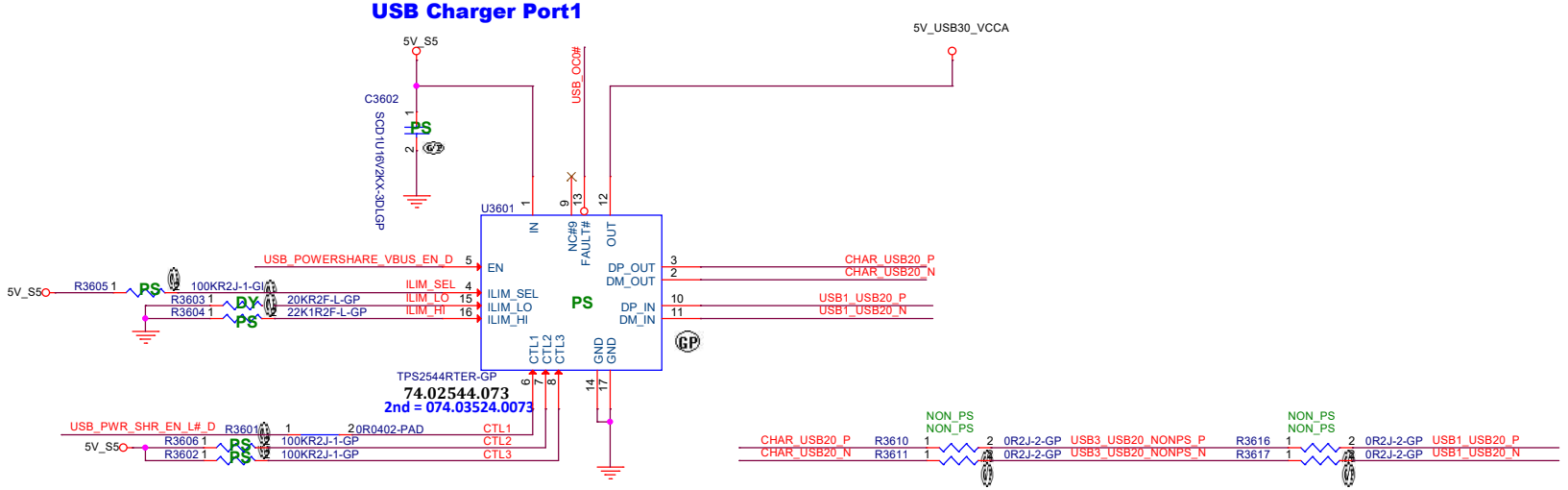
Size: A1 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 16, 2020 | Sheet 35 of 100

Main Func = USB Charger

For CBG L

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}\,(mA) = \frac{50{,}500}{(R_{ILIM\_XX}\,(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

[16] CHAR_USB20_P
[16] CHAR_USB20_N

[35] USB1_USB20_N
[35] USB1_USB20_P

[24] USB_POWERSHARE_VBUS_EN_D
[24] USB_PWR_SHR_EN_L#_D

[16,35] USB_OC0#

<Core Design>

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Title: USB Charger

Size: Custom | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 36 of 106

(Blanking)

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Title: USB3.0 PORT

Size	Document Number	Rev
A4	Cyborg TGL	SC

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(Blanking)

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Title

Reserved

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A4	*Cyborg TGL*	*SC*

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Title

(RSVD)

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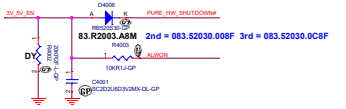
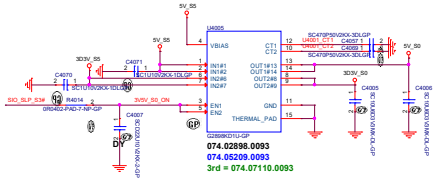
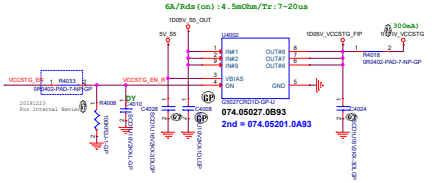
RUN Power

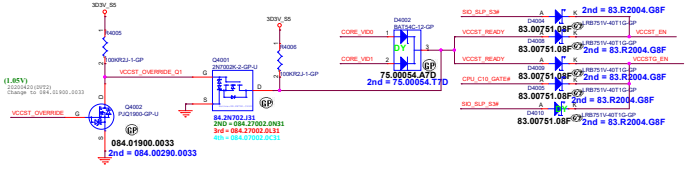
20200815
Remove

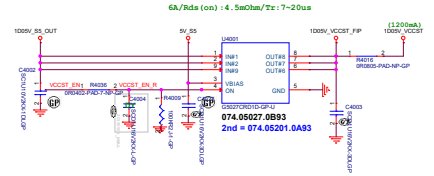
HW SHUTDOWN



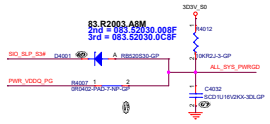


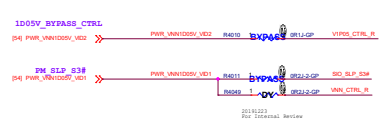


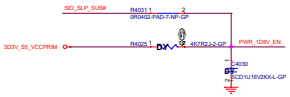


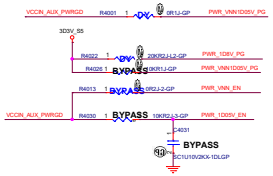


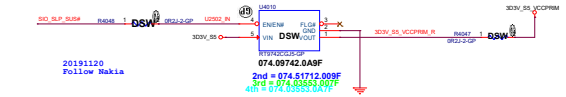
Power Sequence / Pull High PWRGD



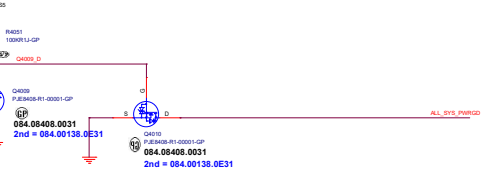








V-tree



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20200807
Remove

CPU (THML/JTAG)

Cyborg TGL

SC

Thursday, January 14, 2021

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Title

Connected_Standby(1/2)+DS3

Size	Document Number	Rev
A4	*Cyborg TGL*	*SC*

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(Blanking)

<Core Design>

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
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[24,44] AC_DIS

[24] PS_ID

[24,44] HW_ACAVIN_NB

[44,69] 19V_AD_JK_C

Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

84.T3904.H11
2nd = 084.03904.0H11
3rd = 084.03904.0H11
4th = 84.03904.T11

84.00138.0A31
2nd = 84.05067.031

83.05725.0A0
2nd = 083.00051.00AF

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

20.F2120.002
2nd = 20.F1295.008

083.00624.00AM
2nd = 083.FJ24A.00AM

84.05212.B11
2nd = 84.00124.H1K
3rd = 084.00024.0B1K

084.05112.001K
2nd = 84.00124.K1K
3rd = 084.00024.0A1K

S1

084.21321.0037
2nd = 084.20P03.0033
3rd = 084.03307.0037

75.00099.O7D
2nd = 75.00099.E7D
3rd = 75.00099.B7D
4th = 075.00099.0E7D

Barrel Adapter Piug-in Detect

74.00331.H2F
2nd = 74.00391.02F

Main Func = M-BAT Input

Batt Connecter

External_RTC

Internal_RTC
084.27002.0031
2nd = 084.27002.0C31

020.F1198.0010
2nd = 020.F1196.0010

Placement: Close to Batt Connector

2nd = 75.00099.E7D	2nd = 75.00099.E7D	2nd = 75.00099.E7D
3rd = 75.00099.B7D	3rd = 75.00099.B7D	3rd = 75.00099.B7D
4th = 075.00099.0E7D	4th = 075.00099.0E7D	4th = 075.00099.0E7D

[24,44] PBAT_CHG_SMBCLK
[24,44] PBAT_CHG_SMBDAT
[24,44] PBAT_PRES#

«Core Design»
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Title: DCIN
Size: A1 | Document Number: Cyborg TGL | Rev: SC
Date: Thursday, January 14, 2021 | Sheet 43 of 105

ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

I2C form EC

To EC

ISL9538 AMON/BMON to EC

External_RTC

From NXP ACK

E3

S2

+3D3V_VDD_DCIN

Vcore_OVP

For CBG L

CHECK EE follow custormer circuits.

TypeC Prochot Follow custormer circuits.

PU +VCCSTG = 1.0 V on CPU side

PU 3V3_AON_S0 on GPU side

OPS

Internal_RTC

External_RTC

Location	Gen11	Gen12
PC44A1	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PQ4425	Stuff	DY
PR4447	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4446	Stuff	DY
PR44A2	Stuff	DY
PR44A3	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU44A1	Stuff	DY
PD44A1	Stuff	DY
PD44A2	DY	Stuff
PD44A3	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm&L Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

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Power (Charger_ISL9538)

Cyborg TGL

Thursday, January 14, 2021

SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal

OFFPAGE-GAP

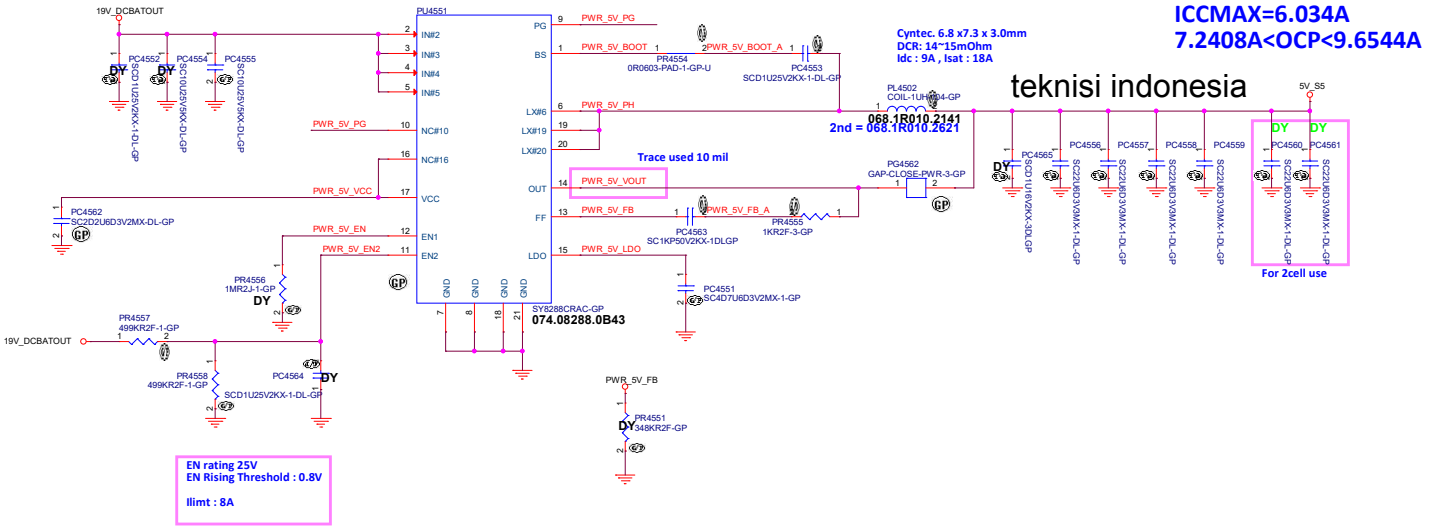
[40,45] 3V_5V_EN — PR4559 0R0402-PAD-7-NP-GP — PWR_5V_EN

PH on EE Side

[17,25,45] 3V_5V_PWRGD — PR4561 0R0402-PAD-7-NP-GP — PWR_5V_PG

SY8288C For 5V

19V_DCBATOUT — PD4501 AZ4024-01L-R7G-GP DY



TDC=8.62A
ICCMAX=6.034A
7.2408A<OCP<9.6544A

SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP

[40,45] 3V_5V_EN — PR4560 0R0402-PAD-7-NP-GP — PWR_3D3V_EN

PH on EE Side

[17,25,45] 3V_5V_PWRGD — PR4562 0R0402-PAD-7-NP-GP — PWR_3D3V_PG

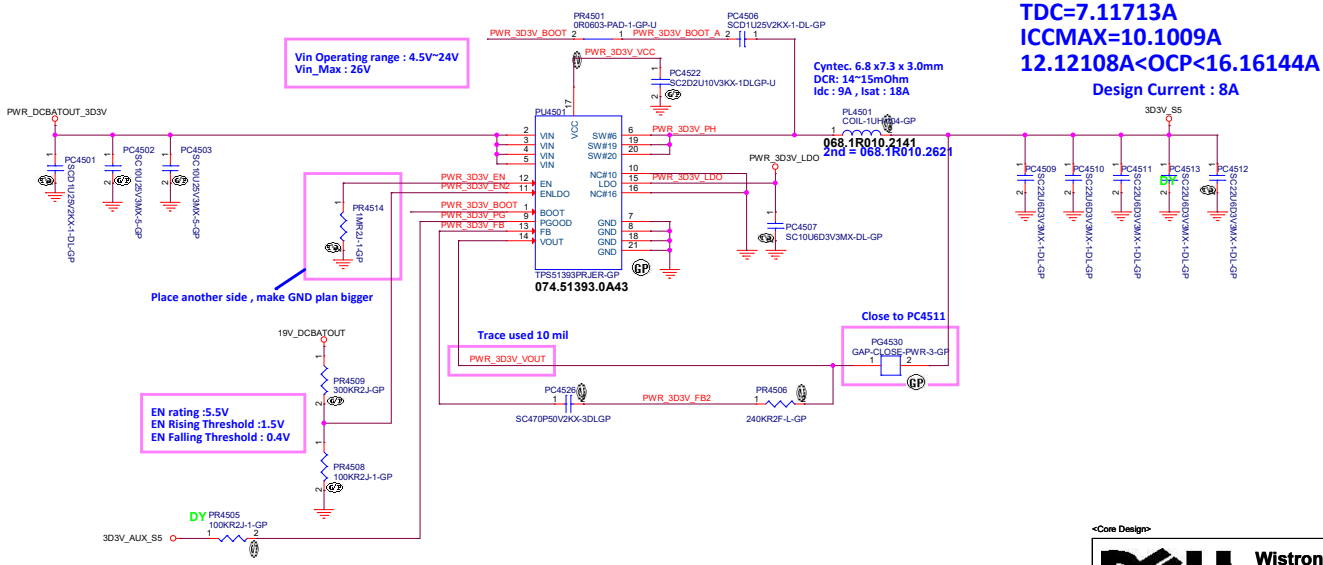
19V_DCBATOUT — PWR_DCBATOUT_3D3V

PG4515 GAP-CLOSE-PWR-3-GP
PG4516 GAP-CLOSE-PWR-3-GP
PG4517 GAP-CLOSE-PWR-3-GP
PG4518 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PG4532 GAP-CLOSE-PWR-3-GP — PWR_3D3V_LDO

TPS51393 For 3D3V

PWR_DCBATOUT_3D3V — PD4502 AZ4024-01L-R7G-GP DY



TDC=7.11713A
ICCMAX=10.1009A
12.12108A<OCP<16.16144A
Design Current : 8A

<Core Design>

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Title: POWER (SY8288_5V/3D3V)
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
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Main Func = CPU_CORE

OFFPAGE

SVID

- [7] SVID_CLK_CPU
- [7] SVID_DATA_CPU
- [7] SVID_ALERT#_CPU

[3,22,24,44,72] PROCHOT#_CPU — PR4631 0R0402-PAD-1-GP — PWR_VCORE_VRHOT_R

[44] CHGR_PSYS_IMVP — CHGR_PSYS_IMVP

20191119
check with Nakia need change
netname to PWR_VCORE_VR_READY or
not

[17,44] PWR_IMVP_PWRGD — PR4636 0R0402-PAD-1-GP — PWR_VCORE_VR_READY

[17,24,40,44] ALL_SYS_PWRGD — PR4635 0R0402-PAD-1-GP — PWR_VCORE_VR_EN

VCORE_SENSE

- [7] VSSCORE_SENSE — VSSCORE_SENSE
- [7] VCCCORE_SENSE — VCCCORE_SENSE

- [47] PWR_VCORE_UGATE1 — PWR_VCORE_UGATE1
- [47] PWR_VCORE_PHASE1 — PWR_VCORE_PHASE1
- [47] PWR_VCORE_LGATE1 — PWR_VCORE_LGATE1

- [47] PWR_VCORE_UGATE2 — PWR_VCORE_UGATE2
- [47] PWR_VCORE_PHASE2 — PWR_VCORE_PHASE2
- [47] PWR_VCORE_LGATE2 — PWR_VCORE_LGATE2

- [47] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
- [47] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
- [47] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
- [47] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

1D05V_VCCST — Close to VR_IC — PR4605 DY — PC4626 SCD1U25V2KX-1-DL-GP

1D05V_VCCSTG_TERM — PR4603 1KR2F-3-GP DY

SVID_CLK_CPU
SVID_ALERT#_CPU
SVID_DATA_CPU

PWR_VCORE_VRHOT_R — PR4607 100R2F-L1-GP-U

5V_S5 — PR4617 0R0402-PAD-7-NP-GP

3D3V_S0 — PR4609 10KR2J-3-GP

19V_DCBATOUT — PD4601 AZ4024-01L-R7G-GP — 083.04024.0A01 — 2nd = 83.PJSD2.0AF

PR4601 0R0603-PAD-7-NP-GP — PC4601 SCD22U25V2KX-4-GP — PC4613 SC1U10V2KX-1DLGP

PWR_VCORE_VR_READY
PWR_VCORE_VR_EN

PC4612 SC4700P50V2KX-1DLGP — PR4602 12K1R2F-L1-GP DY

PC4609 SC330P50V2KX-2-GP — PR4608 90K9R2F-GP

20200302 (DVT1)
Change PC4609 to 0201
20200313 (DVT1)
Change to 25V

20200221 (DVT1)
changes to 90.9K

PU4601 ISL95869HRTZ-T-GP

1st = 074.95869.M001

PROG1
VBOOT: 0V
F=750kHz

PR4619 78K7R2F-GP — PR4620 9K31R2F-GP

PC4610 SCD22U25V2KX-4-GP — PR4621 0R0603-PAD-7-NP-GP — PWR_VCORE_BOOT1_N

PR4625 0R0402-PAD-7-NP-GP — O5V_S5 — PC4605 SC1U10V2KX-1DLGP

PR4616 10KR2F-2-GP

PWR_VCORE_NTC_N

B=4500

PR4655 27K4R2F-GP — PR4618 2nd = 069.60012.0001 NTC-40K-41-GP

20200221 (DVT1)
changes to 2K
20200227 (DVT1)
change back to1.3K

PR4615 1K5R2F-2-GP

PC4608 SC82P50V2KN-3-DL-GP

PR4611 0R0603-PAD-7-NP-GP — PWR_VCORE_BOOT2_N — PC4611 SCD22U25V2KX-4-GP

PR4668 0R2J-2-GP DY — O5V_S5

PR4614 2KR2F-3-GP — PR4613 24K9R2F-GP — PR4612 392R2F-GP

PC4607 SCD01U25V2KX-3DLGP

PWR_VCORE_FB1 — PC4606 SC220P50V2KX-3DLGP

PWR_VCORE_FB4 — PWR_VCORE_FB2 — PC4604 SC820P50V2KX-1-DL-GP

VCCCORE_SENSE — PR4667 0R0402-PAD-1-GP

PR4640 100R2F-L1-GP-U — O1V_CPU_CORE

PWR_VCORE_FB3 — PC4615 SCD01U25V2KX-3DLGP DY

PR4665 0R0402-PAD-7-NP-GP

PC4605 SC330P50V2KX-3-DL-GP — PC4638 SC330P50V2KX-3-DL-GP

PC4623 SC2200P50V2KX-2DLGP — PWR_VCORE_ISUMN_N — PR4628 3K48R2F-GP

PR4627 511R2F-2-GP

PR4666 0R0402-PAD-1-GP — VSSCORE_SENSE — PR4626 100R2F-L1-GP-U

PWR_VCORE_ISEN2
PWR_VCORE_ISEN1

PC4614 SCD22U16V2KX-3DLGP — PC4618 SCD22U16V2KX-3DLGP

PWR_VCORE_ISUMP — PR4629 0R0402-PAD-7-NP-GP — PWR_VCORE_ISUMP_N

PC4602 SCD22U16V2KX-3DLGP — PC4616 SCD22U16V2KX-3DLGP

PR4630 11KR2F-L-GP — PR4653 2K61R2F-1-GP — PWR_VCORE_ISUMNP_2

PR4650 NTC-10K-29-GP-U 69.60011.201 2nd = 69.60013.131 — B=3370

PWR_VCORE_ISUMN

PC4603 SCD01U25V2KX-3DLGP 20200212 Change to 0.1u 25V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95869_CPUCORE(1/3))

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 46 of 105

Main Func = VCCIN

OFFPAGE

[46] PWR_VCORE_UGATE — PWR_VCORE_UGATE1
[46] PWR_VCORE_PHASE — PWR_VCORE_PHASE1
[46] PWR_VCORE_LGATE — PWR_VCORE_LGATE1

[46] PWR_VCORE_UGATE — PWR_VCORE_UGATE2
[46] PWR_VCORE_PHASE — PWR_VCORE_PHASE2
[46] PWR_VCORE_LGATE — PWR_VCORE_LGATE2

[46] PWR_VCORE_ISEN2 — PWR_VCORE_ISEN2
[46] PWR_VCORE_ISEN1 — PWR_VCORE_ISEN1
[46] PWR_VCORE_ISUMP — PWR_VCORE_ISUMP
[46] PWR_VCORE_ISUMN — PWR_VCORE_ISUMN

19V_DCBATOUT
PC4702 SC10U25V3MX-6-GP
PC4703 SC10U25V3MX-6-GP
PC4704 SC10U25V5KX-DL-GP
PC4705 SC10U25V3MX-6-GP
PC4706 SCD1U25V2KX-1DL-GP

20200414
For acoustic low noice

19V_DCBATOUT
TC4701 ST100U25VDM-1-GP
077.C1071.0071
077.C1071.0101

For acoustic noice

20200414
For spacing using TC4701 only

TGL_U42 28W
Performance
TDC=43A
ICCMAX=65A

PWR_VCORE_LGATE1
PWR_VCORE_UGATE1
PWR_VCORE_PHASE1
19V_DCBATOUT
PU4701
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
4ZA_CPU CORE

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A
PL4701 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141

1V_CPU_CORE
PT4701 ST330U2D5VBM-1-GP
80.3371V.A2L
2nd = 77.23371.34L

PR4705 2D2R6J-3-GP
PWR_VCORE_SNB1
PC4710 SC1KP50V2KX-1DLGP
PG4711 GAP-CLOSE-PWR-3-GP
PG4712 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISUMP_GA
PWR_VCORE_ISUMN_GA
PWR_VCORE_ISEN1
PR4721 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4708 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN2
PR4709 10R2F-L-GP
PR4722 100KR2F-L1-GP

19V_DCBATOUT
PD4701 AZ4024-01L-R7G-GP
DY

19V_DCBATOUT
PD4702 AZ4024-01L-R7G-GP
DY

20200414
For acoustic low noice

19V_DCBATOUT
PC4714 SC10U25V3MX-5-GP
PC4715 SC10U25V3MX-5-GP
PC4716 SC10U25V3MX-5-GP
PC4717 SC10U25V3MX-5-GP
PC4718 SCD1U25V2KX-1DL-GP

PWR_VCORE_LGATE2
PWR_VCORE_UGATE2
PWR_VCORE_PHASE2
19V_DCBATOUT
PU4702
AOE6932-GP
075.06932.0A73
2nd = 075.16038.0073
4ZA_CPU CORE

teknisi indonesia

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 38A , Isat : 45A
PL4702 IND-D15UH-33-GP
068.R1510.1171
2nd = 068.R1510.1141

1V_CPU_CORE

PR4714 2D2R6J-3-GP
PWR_VCORE_SNB2
PC4713 SC1KP50V2KX-1DLGP
PG4713 GAP-CLOSE-PWR-3-GP
PG4714 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISUMP_GB
PWR_VCORE_ISUMN_GB
PWR_VCORE_ISEN2
PR4723 100KR2F-L1-GP
PWR_VCORE_ISUMP
PR4716 3K65R2F-1-GP
PWR_VCORE_ISUMN
PWR_VCORE_ISEN1
PR4715 10R2F-L-GP
PR4724 100KR2F-L1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (95829_CPUCORE(2/3))
Size: A2
Document Number: Cyborg TGL
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Date: Thursday, January 14, 2021
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Main Func = CPU_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A3		SC

Date: Thursday, January 14, 2021 Sheet 48 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RSVD)*

Size	Document Number	Rev
A	*Cyborg TGL*	*SC*

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Main Func = VCCIN_AUX

OFFPAGE

VID

[22,40] CORE_VID0 — PR5014 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID0

[22,40] CORE_VID1 — PR5015 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_VID1

[40,53] PWR_1D8V_PG

[17,24,40] VCCIN_AUX_PWRGD

VCCIN_AUX SENSE

PWR_VCCIN_AUX_FB_O — PR5012 0R2J-2-GP — 1D8V_CPU_AUX

[22] VCCAUX_SENSE — PR5017 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_FB_O

[22] VSSAUX_SENSE — PR5018 0R0402-PAD-7-NP-GP — PWR_VCCIN_AUX_RGND

20200414
For acoustic low noice

19V_DCBATOUT — FC5001 DY 10U25V1UN-GP; PC5006 SC10U25V3MX-5-GP; PC5007 SC10U25V3MX-5-GP; PC5012 SC10U25V3MX-5-GP; PC5013 SC10U25V3MX-5-GP

19V_DCBATOUT — PD5001 AZ4024-01L-R7G-GP
083.04024.0AA1
2nd = 83.PJSD2.0AF

19V_DCBATOUT — TC5001 ST100U25VDM-1-GP
077.C1071.0071
2nd = 077.C1071.0101

For acoustic noice

20200414
For spacing using TC4701 only

TGL_U42 28W
Performance
TDC=14A
ICCMAX=27A
32.4A<OCP<37.8A

PWR_VCCIN_AUX_BOOT — PC5009 SC1U10V2KX-1DLGP

19V_DCBATOUT — PR5024 2D2R3-1-U-GP — PC5005 SCD1U25V2KX-1-DL-GP

3D3V_S5 — PR5004 10KR2J-3-GP

5V_S5 — PR5001 2D2R2J-GP — PR5002 118KR2F-1-GP

PWR_1D8V_PG — PR5005 2D2R2J-GP

PR5003 DY 10KR2J-3-GP

PU5001 RT6543AGQW-GP
074.06543.0073

Pin	Name	Net
1	CS_DIS	PWR_VCCIN_AUX_CS
2	ISENSEP	PWR_VCCIN_AUX_ISENP
3	ISENSEN	PWR_VCCIN_AUX_ISENN
4	PG	VCCIN_AUX_PWRGD
5	COMP	PWR_VCCIN_AUX_COMP
6	FB	PWR_VCCIN_AUX_FB
7	RGND	PWR_VCCIN_AUX_RGND
8	VOUT	PWR_VCCIN_AUX_FB_O
9	FSWSEL	PWR_VCCIN_AUX_FSW
10	BOOT	PWR_VCCIN_AUX_BOOT
11	UG	PWR_VCCIN_AUX_UG
12	PH	PWR_VCCIN_AUX_LX
13	LG	PWR_VCCIN_AUX_LG
14	PGND	
15	PVCC	PWR_VCCIN_AUX_VCC
16	VCC	
17	VID1	PWR_VCCIN_AUX_VID1
18	VID0	PWR_VCCIN_AUX_VID0
19	EN	PWR_VCCIN_AUX_EN
20	VSYS	PWR_VCCIN_AUX_VSYS
21	AGND	

PC5008 SC1U10V2KX-1DLGP — PC5010 SC1U10V2KX-1DLGP

19V_DCBATOUT

PU5002 / PU5003 FDMS3600-02-RJK0215-COLAY-GP
075.07321.0073
2nd = 075.36304.0073 4ZA_AUX

PG5005 GAP-CLOSE-PWR-3-GP

PR5021 5K36R2F-GP — PWR_VCCIN_AUX_ISENP_A

PC5011 SCD1U25V2KX-1-DL-GP

PR5008 267R2F-GP — PR5022 866R1F-GP — PWR_VCCIN_AUX_RC

PR5023 NTC-10K-29-GP-U
B=3370K
69.60011.261
2nd = 69.60013.131

Cyntec. 6.8 x 7.3 x 3mm
DCR: 2.5~2.8 mOhm
Idc : 23A , Isat : 40A

PL5001 IND-D22UH-37-GP
68.R2210.10V
2nd = 068.R2210.1141

PG5006 GAP-CLOSE-PWR-3-GP — PR5007 10KR2F-1-GP-U

1D8V_CPU_AUX — PT5001 ST330U2D5VBM-1-GP
80.3371V.A2L
2nd = 77.23371.34L

PC5003 SC2200P50V2KX-2DLGP — PWR_VCCIN_AUX_COMP_R — PR5011 10KR2F-2-GP

PC5002 SC470P50V2KX-3DLGP — PWR_VCCIN_AUX_FB_R — PR5009 1K6R2F-GP DY

PC5004 SC22P50V2JN-4DLGP

PR5010 5K62R2F-GP

PWR_VCCIN_AUX_FB_O

DY PC5020 SCD1U25V2KX-1-DL-GP

PR5006 100R2F-L1-GP-U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT6543A_VCCIN_AUX

Size: A2 | Document Number | Rev: SC

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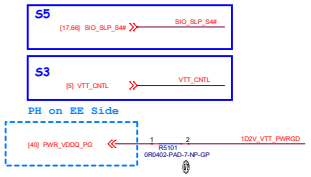
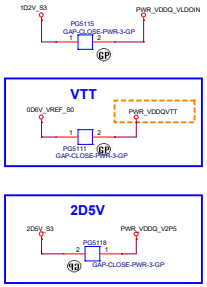
OFFPAGE



OFFPAGE_GAP



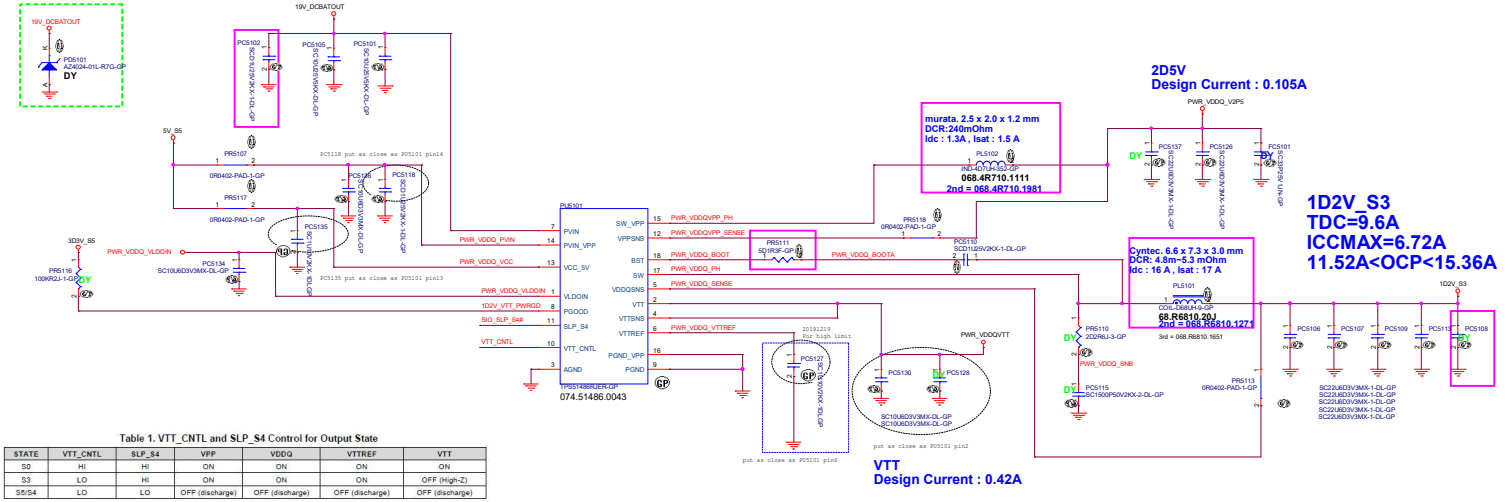


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 051_POWER (TPS51486R_VDDQ/VTT)

Size: C | Document Number: | Rev: SC

Custom: Cyborg TGL

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SSID = PWR.Plane.Regulator_1D0V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ2262Q_1D0V)

Size: A3 | Document Number: Cyborg TGL | Rev: SC

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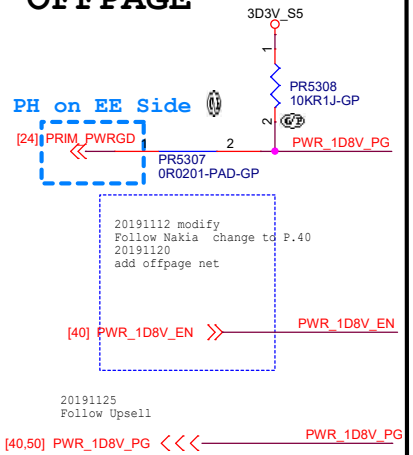
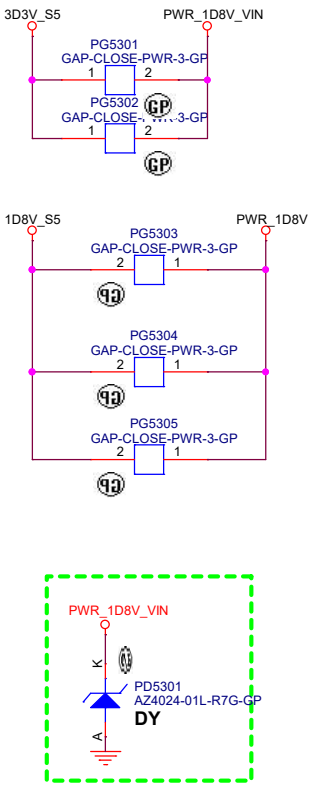
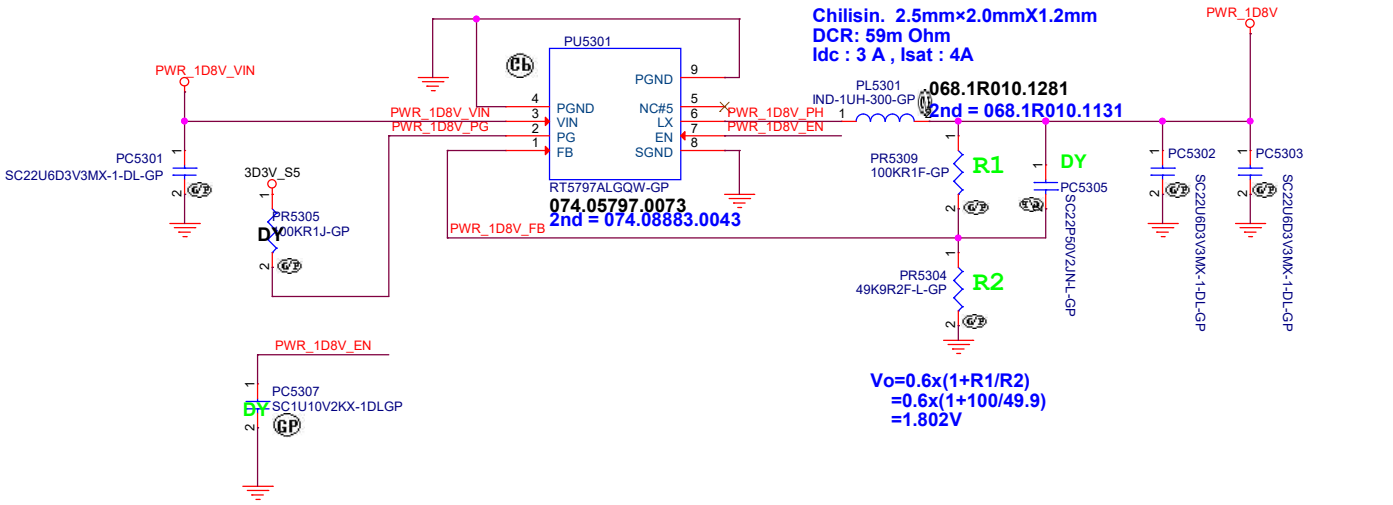
Main Func = 1D8V/1D2V

OFFPAGE



OFFPAGE_GAP





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: B | Document Number: Cyborg TGL | Rev: SC

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Main Func = 1D05V

OFFPAGE

PH on EE Side

20191119
Check with UPSELL and Nakia follow which one

VCCIN_AUX_PWRGD
[40] PWR_VNN_EN

PWR_VNN_EN

1D05V_BP_PWRGD
[24,40] PWR_VNN1D05V_PG

PWR_VNN1D05V_PG

[40] PWR_1D05V_EN

PWR_1D05V_EN

PH on EE Side

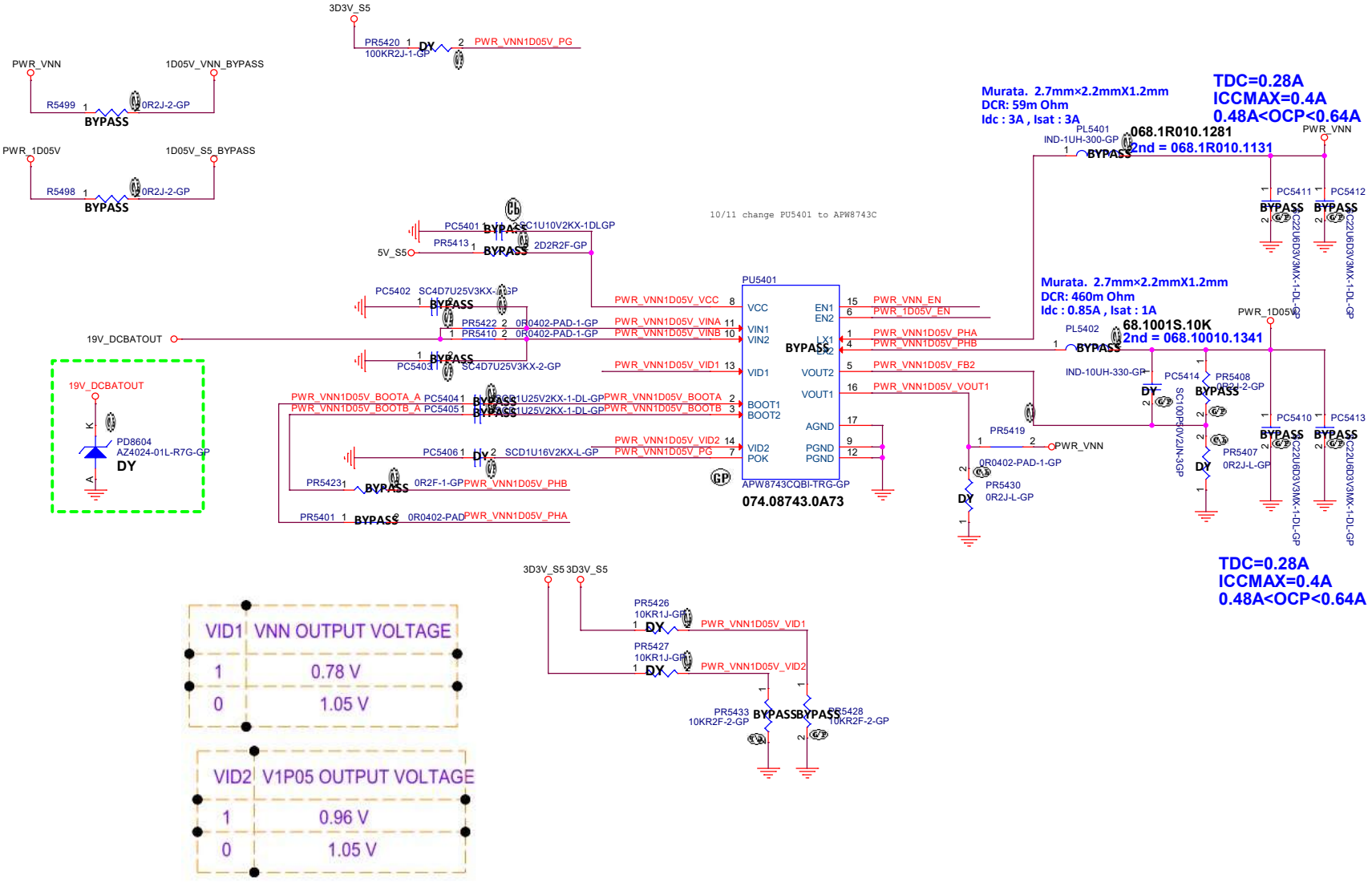
1D05V_BYPASS_CTRL
[40] PWR_VNN1D05V_VID2

PWR_VNN1D05V_VID2

PM_SLP_S3#
[40] PWR_VNN1D05V_VID1

PWR_VNN1D05V_VID1

OFFPAGE-GAP



VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER(APW8738A_VNN1D05)

Size: A3 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 54 of 105

Main Func = LCD

From CPU

[4] eDP_TX_CPU_N0
[4] eDP_TX_CPU_P0
[4] eDP_TX_CPU_N1
[4] eDP_TX_CPU_P1
[4] eDP_AUX_CPU_P
[4] eDP_AUX_CPU_N
[4] EDP_HPD
[4] eDP_VDD_EN
[4] L_BKLT_CTRL

From EC

[24] PANEL_BKEN
[17,27,40,81] SIO_SLP_S3#
[20] LCD_CBL_DET#

FOR TESTING

[20] DBC_PANEL_EN
[24] LCD_VCC_TEST_EN
[24] LCD_TST
[24] CABLE2_OCP#
[24] PANEL_MONITOR
[20,70] SENSOR_I2C_SDA
[20,70] SENSOR_I2C_SCL
[20] GSEN_INT1_C

INVERTER POWER

19V_DCBATOUT
19V_DCBATOUT_LCD_R
FS503
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 69.50007.G71
19V_DCBATOUT_LCD
3D3V_S0
PCH_I2C0_SCL_TS
PCH_I2C0_SDA_TS
AFTP5504 AFTE14P-GP
AFTP5505 AFTE14P-GP
DMIC_SDA_EDP
DMIC_SCL_EDP
AFTP5509 AFTE14P-GP
AFTP5510 AFTE14P-GP
3D3V_HINGE_S0
AFTP5511 AFTE14P-GP
EDP_HPD_CONN
AFTP5521 AFTE14P-GP
AFTP5522 AFTE14P-GP
AFTP5523 AFTE14P-GP
AFTP5525 AFTE14P-GP

Camera & DMIC

Camera
DMIC
5V_IRLED
3D3V_HINGE_S0
IR_CAM_DET#
DMIC_SDA_EDP
DMIC_SCL_EDP
SENSOR_I2C_SDA_R
SENSOR_I2C_SCL_R
GSEN_INT1_C_R
LCD_USB20_CON_N
LCD_USB20_CON_P

Sensor Board

SENSOR_I2C_SDA
SENSOR_I2C_SCL
GSEN_INT1_C
DBC_PANEL_EN
DBC_EN_R
LCD_CBL_DET#

eDP

eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_AUX_CPU_P
eDP_AUX_CPU_N
eDP_TX_CON_N1
eDP_TX_CON_P1
eDP_TX_CON_N0
eDP_TX_CON_P0
eDP_AUX_CON_P
eDP_AUX_CON_N

Display

3D3V_LCDVDD_S0
trace width = 80mil
LCD_TST_C
EDP_HPD_CONN
BLON_OUT_C
LCD_BRIGHTNESS
TOUCH_PANEL_DET#_R
TOUCH_REPORT_SW_R
TOUCH_I2C0_SCL_TS_R
TOUCH_I2C0_SDA_TS_R
TOUCH_PANEL_INTR#
TOUCH_PANEL_PD#_R
19V_DCBATOUT_LCD
LCD1
STAR-CON40-6-GP
020.F0847.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040

Touch

5V_3D3V_TOUCH_S0
TOUCH_PANEL_DET#
TOUCH_REPORT_SW
TOUCH_I2C0_SCL_TS
TOUCH_I2C0_SDA_TS
TOUCH_PANEL_PD#

Hinge up cable protection

20191023(EVT1)
Follow Dell CY20 change net name
20200420(DVT2)
Change C5542 to 0402 for layout limit
20200508(DVT2)
Change U5501 to 074.02895.0A73

3D3V_S5
5V_S5
LCDVDD_EN
SIO_SLP_S3#
CABLE1_OCP#
CABLE2_OCP#
3D3V_HINGE_R
U5501
G2899BLK21U-GP
074.02895.0A73
2nd = 074.05206.0093
3D3V_LCDVDD_S0
eDP_VDD_EN
LCDVDD_EN
D5502
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
LCD_VCC_TEST_EN
D5506
CABLE3_OCP#
CABLE4_OCP#
20210114
Remove shortpad
3D3V_HINGE_S0
R5564
0R1206-DB-GP

Brightness

EC (BIST MODE)
L_BKLT_CTRL
LCD_TST
EDP_HPD
LCDVDD_EN
D5503
BAT54C-12-GP
2nd = 79.00054.7TD
RN5501
SRN10KJ-3-GP
PANEL_BKEN
BLON_OUT_C
LCD_BRIGHTNESS
LCD_TST_C
EDP_HPD_CONN
RN5502
SRN100KJ-5-GP

TOUCH_WM / TOUCH_CBG

5V_3D3V_TOUCH_S0
5V_TPAN_VDD
TOUCH_WM
TOUCH_CBG
5V_IRLED
C5504
330R CAP
TP_PWR_EN
SIO_SLP_S3#
U5502
G2899BLK21U-GP
074.02895.0A73
2nd = 074.05206.0093
TOUCH_CBG

PANEL_PWRGD CIRCUIT

19V_DCBATOUT
19V_DCBATOUT_LCD
Q5503_E
Q5503_B
Q5503_C
LMBT3906LT1G-1-GP
DCBATOUT_LCD_PWRGD
DCBATOUT_LCD_PG
Q5505
LMBT3904LT1G-GP
84.T3906.E11
2nd = 84.T3906.I11
3rd = 084.03906.0B11
4th = 084.03906.0C11
84.T3904.H11
2nd = 084.03904.0I11
3rd = 084.03904.0H11
4th = 84.03904.T11
3D3V_S5
PANEL_PWRGD_R
PANEL_MONITOR
3D3V_S0
Q5505_E
Q5504_B
Q5504_C
3D3V_LCDVDD_S0
LCDVDD_PWRGD
LCDVDD_PG
Q5504
Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.

MIC POWER / CAMERA POWER / SENSOR POWER / TOUCH PANEL POWER

3D3V_HINGE_S0
5V_3D3V_TOUCH_S0

Main Func = Touch panel

[20] PCH_I2C0_SDA_TS
[20] PCH_I2C0_SCL_TS
[20] TOUCH_PANEL_INTR#
[24] TOUCH_REPORT_SW
[3] TOUCH_PANEL_DET#
[3] TOUCH_PANEL_PD#

Main Func = CAMERA

[19] IR_CAM_DET#
[16] CCD_USB20_N
[16] CCD_USB20_P
[27] DMIC_SCL_CODEC
[27] DMIC_SDA_CODEC
[19] DMIC_PCH_CLK_Q
[19] DMIC_PCH_DATA_Q

2020/02/29:swap EL5501

CCD_USB20_N
CCD_USB20_P
EL5501
TLVR05R5V2D-GP
068.09002.2001
2nd = 68.02002.061
CCD_USB20_CON_N
CCD_USB20_CON_P
ED5502
AZ5315-02F-GP
DY

2020/02/29:swap RN5505

BLM15AG121SN-1GP
EL5502
EL5503
DMIC_PCH_CLK_Q
DMIC_PCH_DATA_Q
DMIC_SCL_EDP
DMIC_SDA_EDP
DMIC_SCL_CODEC
DMIC_SDA_CODEC
RN5504
SRN33J-5-GP-U
DY_DMICtoCODEC

<Core Design>
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Title: LCD&CAM&DMC&Touch
Size: Custom
Document Number: Cyborg TGL
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Main Func = CRT

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Title: *CRT(Reserved)*

Size: A3 | Document Number: *Cyborg TGL* | Rev: *SC*

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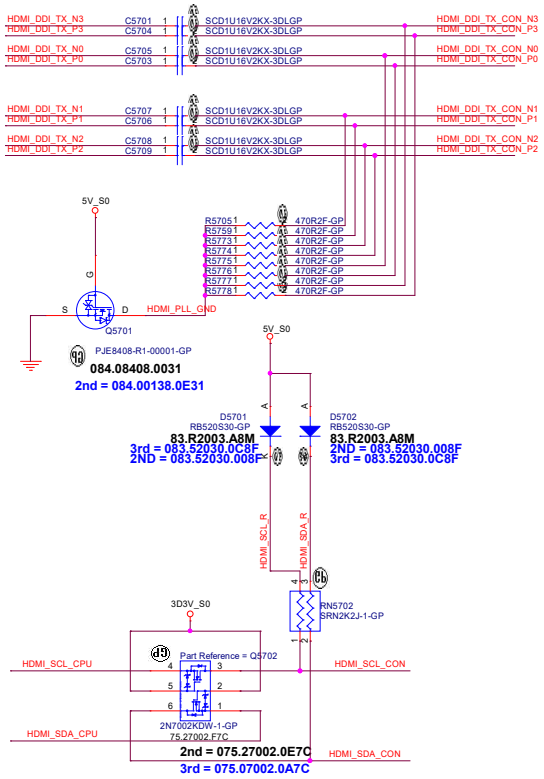
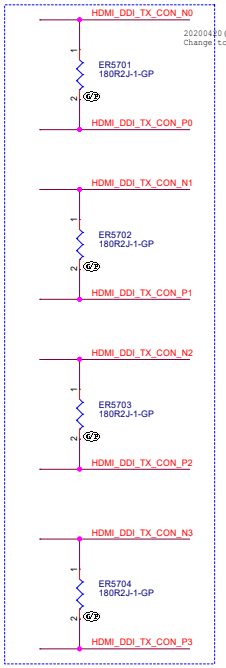
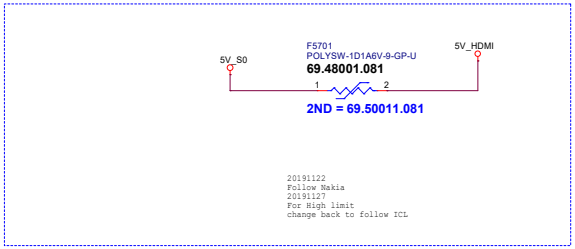
SSID = HDMI Level Shifter/Connector

[4] HDMI_DDI_TX_N0
[4] HDMI_DDI_TX_P0
[4] HDMI_DDI_TX_N1
[4] HDMI_DDI_TX_P1
[4] HDMI_DDI_TX_N2
[4] HDMI_DDI_TX_P2
[4] HDMI_DDI_TX_N3
[4] HDMI_DDI_TX_P3

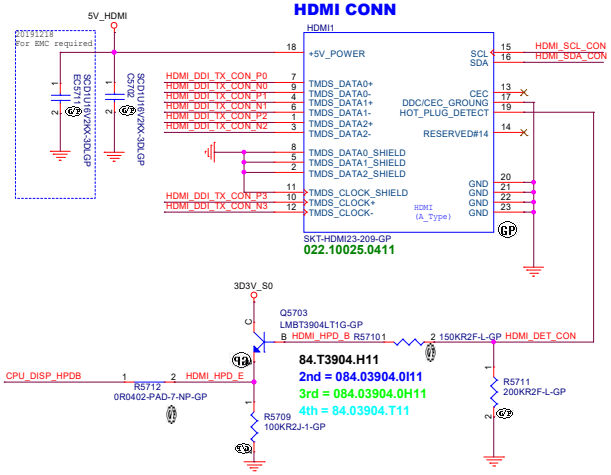
[4] HDMI_SCL_CPU
[4] HDMI_SDA_CPU
[4] CPU_DISP_HPDB



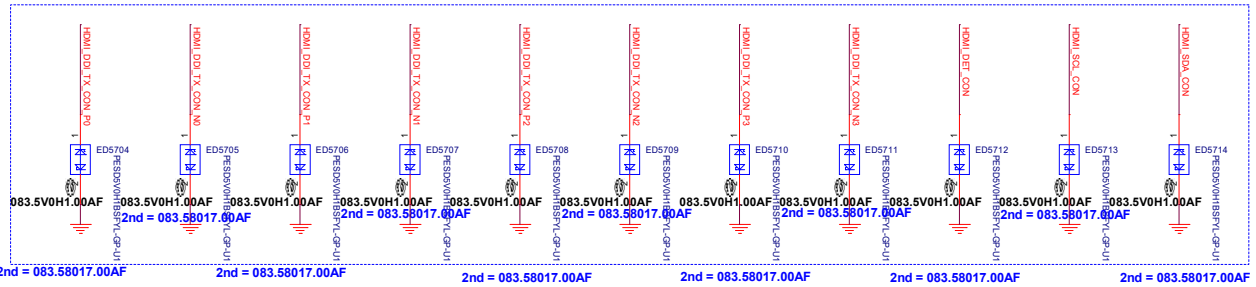




HDMI CONN



EMI Request:



<Core Design>

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Title: Title
HDMI

Size: Custom | Document Number: Document Number: **Cyborg TGL** | Rev: Rev: **SC**

Date: Thursday, January 14, 2021 | Sheet: Sheet 57 of 105

(Blanking)

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Title
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Size	Document Number	Rev
A4	*Cyborg TGL*	*SC*

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Title: *(Reserved)*		
Size: A4	Document Number: *Cyborg TGL*	Rev: *SC*
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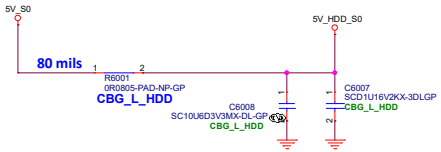
Main Func = HDD

HDD

[70] FFS_INT2_Q
[16,60] HDD_DEVSLP
[16] HDD_SATA_TX_P
[16] HDD_SATA_TX_N
[16] HDD_SATA_RX_P
[16] HDD_SATA_RX_N
[16,60] HDD_DEVSLP
[16] HDD_DET#

HDD POWER

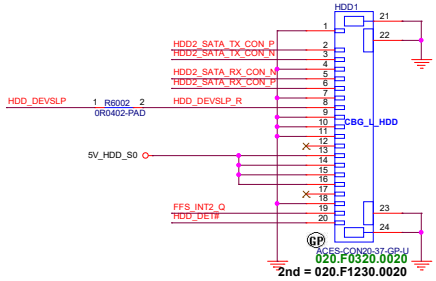
For CBG L

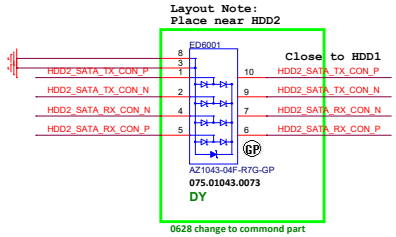


SATA RE-DRIVER

20201013
Remove

SATA HDD Connector





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Title: SATA IF HDD/ODD

Size: A2 | Document Number: Cyborg TGL | Rev: SC

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Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18] CLK_PCIE_WLAN_REQ#

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[19] BT_RADIO_DIS#
[16] WLAN_RF_DIS#
[17,62,63,66,71,76,91] PCH_PLTRST#
[18,24] SUSCLK

Debug

Power EN (Madesimo)

[21] CNV_BRI_DT_R
[21] CNV_RGI_DT_R
[21] CLKREQ_CNV
[21] CNV_RF_RESET#
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLKN
[21] CNV_WT_CLKP
[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLKN
[21] CNV_WR_CLKP
[21] CNV_BRI_RSP
[21] CNV_RGI_RSP
[24] JIO3_PCIE_WAKE#

3D3V_S5 → R6140 0R0805-PAD-NP-GP → 3D3V_WLAN

1.1A

C6110 SCD1U16V2KX-3DLGP
C6106 SC10U6D3V3MX-DLGP
C6109 SCD1U16V2KX-3DLGP

AFTE14P-GP AFTP6101 — 1 3D3V_WLAN
AFTE14P-GP AFTP6105 — 1 CLK_PCIE_WLAN_REQ#
AFTE14P-GP AFTP6106 — 1 WIFI_RF_EN_R
AFTE14P-GP AFTP6107 — 1 BLUETOOTH_EN_R
AFTE14P-GP AFTP6108 — 1 PCH_PLTRST#
AFTE14P-GP AFTP6109 — 1 BT_USB20_CON_N
AFTE14P-GP AFTP6110 — 1 BT_USB20_CON_P
AFTE14P-GP AFTP6111 — 1 JIO3_PCIE_WAKE#

3D3V_WLAN → R6145 10KR2J-3-GP → WLAN_RF_DIS# — R6144 0R0402-PAD-7-NP-GP — WIFI_RF_EN_R

3D3V_WLAN → R6146 10KR2J-3-GP → BT_RADIO_DIS# — R6143 0R0402-PAD-7-NP-GP — BLUETOOTH_EN_R

3D3V_WLAN → R6106 DY 10KR2J-3-GP → CLKIN_XLAL_LCP_R

WIFI_RF_EN_R
BLUETOOTH_EN_R
PCH_PLTRST#
SUSCLK → R6135 33R2J-2-GP → SUSCLK_WLAN

CNV_RGI_RSP → R6109 49D9R1F-GP → CNV_BRI_DT_R / CNV_RGI_RSP_R / CNV_RGI_DT_R

CNV_BRI_RSP → R6118 49D9R1F-GP → CNV_BRI_RSP_R

CLKREQ_CNV → R6141 33R1F-GP → BT_PCMOUT_CLKREQ0_R
CNV_RF_RESET# → R6142 33R1F-GP → BT_PCMFRM_CRF_RST_N

3D3V_WLAN → R6134 75KR1F-GP / DY R6133 71K5R1F-GP

WLAN1 — NGFF_KEY_E_75P — SKT-NGFF75P-164-GP

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	RESERVED#73 → CNV_WT_CLKP
70	RESERVED#70	71	RESERVED#71 → CNV_WT_CLKN
68	RESERVED#68	69	GND
66	RESERVED#66	67	RESERVED#67/2ND_LANE_PERN1 → CNV_WT_DP0
64	GPIO0_NFC_RESET#/MGPIO7	65	RESERVED#65/2ND_LANE_PERP1 → CNV_WT_DN0
62	NFC_I2C_IRQ/MGPIO5	63	GND
60	NFC_I2C_SM_CLK	61	RESERVED#61/2ND_LANE_PETN1 → CNV_WT_DP1
58	NFC_I2C_SM_DATA	59	RESERVED#59/2ND_LANE_PETP1 → CNV_WT_DN1
56	W_DISABLE#1	57	GND
54	RESERVED#54/W_DISABLE#2	55	PEWAKE0# → JIO3_PCIE_WAKE#
52	PERST0#	53	CLKREQ0# → CLK_PCIE_WLAN_REQ#
50	SUSCLK_32KHZ	51	GND
48	COEX1	49	REFCLKN0 → WLAN_CLK_CPU_N
46	COEX2	47	REFCLKP0 → WLAN_CLK_CPU_P
44	COEX3	45	GND
42	CLINK_CLK	43	PERN0 → WLAN_PCIE_RX_N
40	CLINK_DATA	41	PERP0 → WLAN_PCIE_RX_P
38	CLINK_RESET	39	GND
36	UART_CTS	37	PETN0 → WLAN_PCIE_TX_CON_N
34	UART_RTS	35	PETP0 → WLAN_PCIE_TX_CON_P
32	UART_TX	33	GND
22	UART_RX	23	SDIO_RESET → CNV_WR_CLKP
20	UART_WAKE	21	SDIO_WAKE → CNV_WR_CLKN
18	GND	19	SDIO_DAT3
16	LED#2	17	SDIO_DAT2 → CNV_WR_DP0
14	PCM_OUT	15	SDIO_DAT1 → CNV_WR_DN0
12	PCM_IN	13	SDIO_DAT0 → CNV_WR_DP1
10	PCM_SYNC	11	SDIO_CMD → CNV_WR_DN1
8	PCM_CLK	9	SDIO_CLK
6	LED#1	7	GND
4	3_3VAUX	5	USB_D- → BT_USB20_CON_N
2	3_3VAUX	3	USB_D+ → BT_USB20_CON_P
		1	GND
NP2	NP2	NP1	NP1

062.10003.0B11
2nd = 062.10007.0371

C6107 SCD1U25V1MX-1-GP — WLAN_PCIE_TX_N
C6108 SCD1U25V1MX-1-GP — WLAN_PCIE_TX_P

BT_USB20_CON_P — R6111 0R0402-PAD-7-NP-GP — BT_USB20_P

BT_USB20_CON_N — R6110 0R0402-PAD-7-NP-GP — BT_USB20_N

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Title: NGFF_WLAN CONN
Size: A3 | Document Number: Cyborg TGL | Rev: SC
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Main Func = WWAN

For CBG L

[24] EC_I2C_SCL_ITE8010
[24] EC_I2C_SDA_ITE8010

WWAN

[16] WWAN_PCIE_RX_N
[16] WWAN_PCIE_RX_P
[16] WWAN_PCIE_TX_N
[16] WWAN_PCIE_TX_P

[18] WWAN_CLK_CPU_P
[18] WWAN_CLK_CPU_N
[18] WWAN_CLKREQ_CPU_N

[4] WWAN_FULL_PWR_EN_R

[18] WWAN_BB_RST#
[4] WWAN_GPIO_PERST#
[17,61,63,66,71,76,91] PCH_PLTRST#

[18] WWAN_DB_DET#

[16] WWAN_USB20_N
[16] WWAN_USB20_P

[16,24] DUAL_BOOT_EVENT#

close to CONN,<8mils

WWAN_PCIE_TX_P — C6202 1 — 2 SCD1U16V2KX-3DLGP WWAN — WWAN_PCIE_TX_P_C
WWAN_PCIE_TX_N — C6201 1 — 2 SCD1U16V2KX-3DLGP WWAN — WWAN_PCIE_TX_N_C
WWAN_PCIE_RX_P — R6210 1 — 2 0R0402-PAD-7-NP-GP WWAN — WWAN_PCIE_RX_P_R
WWAN_PCIE_RX_N — R6211 1 — 2 0R0402-PAD-7-NP-GP WWAN — WWAN_PCIE_RX_N_R

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WWAN_CLK_CPU_P
WWAN_CLK_CPU_N

WWAN_USB20_P — R6202 1 — 2 0R0402-PAD-7-NP-GP WWAN — WWAN_USB20_P_R
WWAN_USB20_N — R6203 1 — 2 0R0402-PAD-7-NP-GP WWAN — WWAN_USB20_N_R

TPAD14-OP-GP TP6201 1 — WWAN_PCIE_WAKE_N
WWAN_CLKREQ_CPU_N
PCH_PLTRST#

WWAN_DB_DET# — R6201 1 — 2 WWAN — WWAN_DB_DET#_R
WWAN_BB_RST# — 0R0402-PAD-7-NP-GP
WWAN_GPIO_PERST# — R6204 1 — 2 — WWAN_GPIO_PERST#_R
0R0201-PAD-GP

EC_I2C_SCL_ITE8010
EC_I2C_SDA_ITE8010
WWAN_INT#_ITE8010

DUAL_BOOT_EVENT# — R6205 1 — DY — 2
0R1J-GP

TPAD14-OP-GP TP6202 1

WWAN_FULL_PWR_EN_R

3D3V_S5

FC6201 1 — 2 SC33P25V1JN-GP DY
FC6202 1 — 2 SC33P25V1JN-GP DY

WWAN1 — KYO-CON34-GP

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	36

WWAN

020.K0346.0034
2nd = 020.K0270.0034

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Title: **WWAN**

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Main Func = M.2 SSD

[18] SSD_CLKREQ_CPU_N
[17,61,62,66,71,76,91] PCH_PLTRST#

[18] SSD_CLK_CPU_P
[18] SSD_CLK_CPU_N

[16] SSD_PCIE_TX_P9
[16] SSD_PCIE_TX_N9
[16] SSD_PCIE_RX_N9
[16] SSD_PCIE_RX_P9

[16] SSD_PCIE_TX_P10
[16] SSD_PCIE_TX_N10
[16] SSD_PCIE_RX_P10
[16] SSD_PCIE_RX_N10

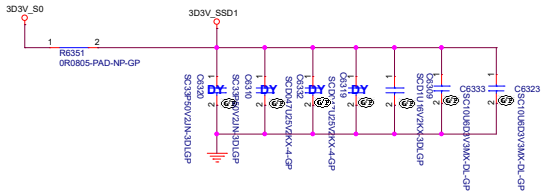
[16] SSD_PCIE_TX_P11
[16] SSD_PCIE_TX_N11
[16] SSD_PCIE_RX_P11
[16] SSD_PCIE_RX_N11

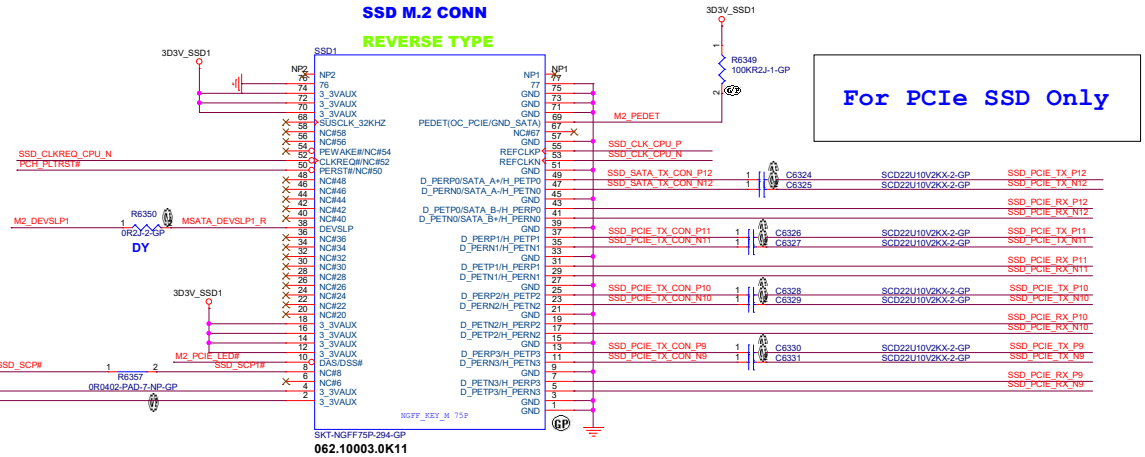
[16] SSD_PCIE_TX_P12
[16] SSD_PCIE_TX_N12
[16] SSD_PCIE_RX_P12
[16] SSD_PCIE_RX_N12

[64] M2_PCIE_LED#

[24] SSD_SCP#

[16] M2_DEVSLP1





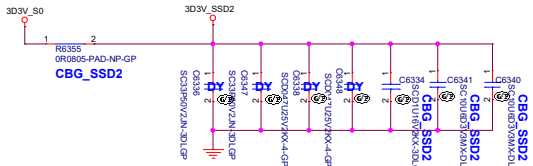
For PCIe SSD Only

M.2 SSD2

[16] SSD_PCIE_TX_P3
[16] SSD_PCIE_TX_N3
[16] SSD_PCIE_RX_P3
[16] SSD_PCIE_RX_N3
[16] SSD_PCIE_TX_P2
[16] SSD_PCIE_TX_N2
[16] SSD_PCIE_RX_P2
[16] SSD_PCIE_RX_N2

[18] SSD2_CLK_CPU_P
[18] SSD2_CLK_CPU_N
[16] SSD2_CLKREQ_CPU_N

[16] M2_PEDET1



For CBG 15" N/V

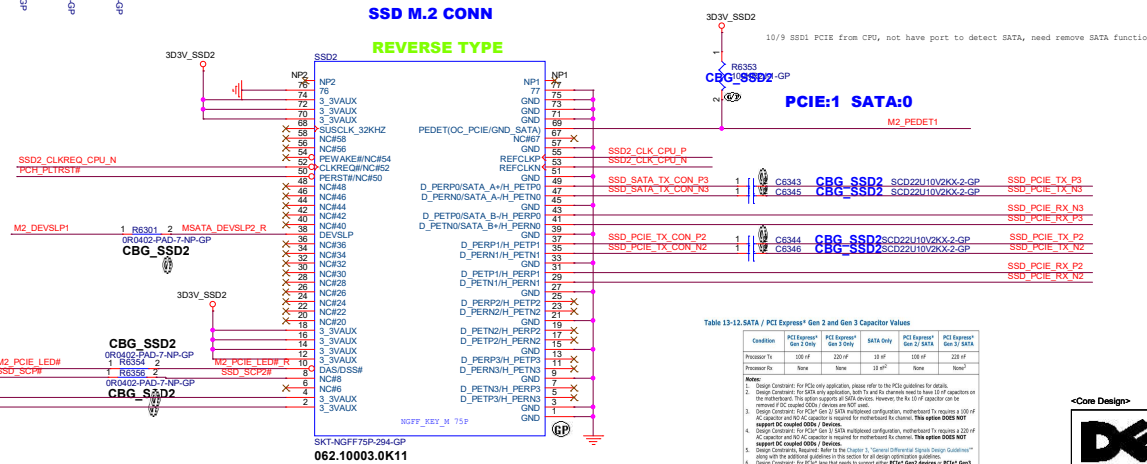


Table 13-12.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[2]

Notes:
1. Design Constraint: For PCIe only applications, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only applications, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT desired.
3. Design Constraint: For PCIe* Gen 3 SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3 SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints. Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimizations guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	+3.3V	GND	75
72	+3.3V	GND	73
70	+3.3V	PEDET(OC_PCIE/GND_SATA)	71
68	SUSCLK(32kHz) (OD)(3.3V)	N/C	69
66	Connector Key	Connector Key	67
64	Connector Key	Connector Key	65
62	Connector Key	Connector Key	63
60	Connector Key	Connector Key	61
58	N/C	GND	59
56	N/C	REFCLKp	57
54	PEWAKE# (OD)(3.3V) or N/C	REFCLKn	55
52	CLKREQ# (OD)(3.3V) or N/C	GND	53
50	PERST# (OD)(3.3V) or N/C	PETn0/SATA-A+	51
48	N/C	PETp0/SATA-A-	49
46	N/C	GND	47
44	N/C	PERn0/SATA-B-	45
42	N/C	PERp0/SATA-B+	43
40	N/C	GND	41
38	DEVSLP (OD)	PETn1	39
36	N/C	PETp1	37
34	N/C	GND	35
32	N/C	PERn1	33
30	N/C	PERp1	31
28	N/C	GND	29
26	N/C	PETn2	27
24	N/C	PETp2	25
22	N/C	GND	23
20	N/C	PERn2	21
18	N/C	PERp2	19
16	3.3V	GND	17
14	3.3V	PETn3	15
12	3.3V	PETp3	13
10	DAS/DSS# (I/O)(3.3V)(OD)	GND	11
8	N/C	PERn3	9
6	N/C	PERp3	7
4	3.3V	GND	5
2	3.3V	GND	3

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
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Main Func = Power BTN

NONE FINGER PRINT 才會上件

Power button

[24] KBC_PWRBTN#

[66] KBC_PWRBTN#_R

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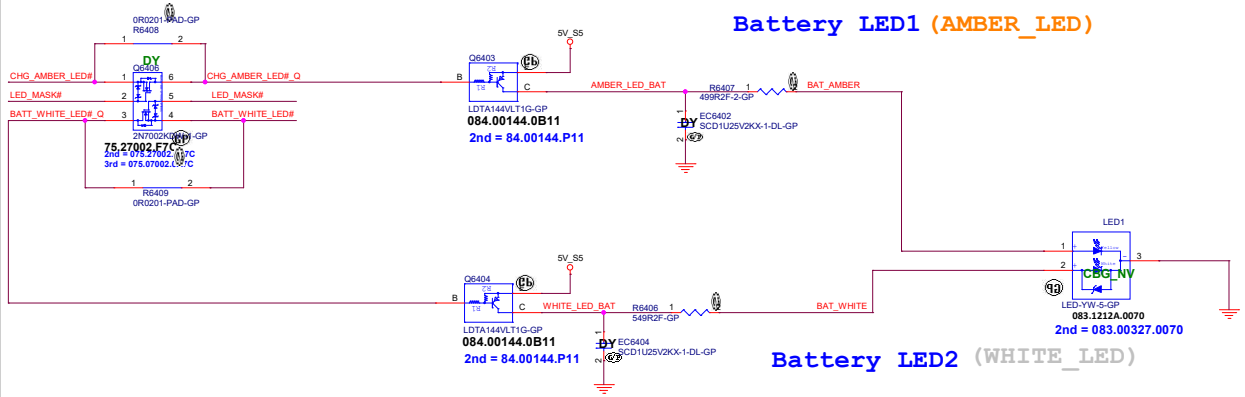
Main Func = Battery LED

Low actived from KBC GPIO

[24] LED_MASK#

[24] CHG_AMBER_LED#

[20,24] BATT_WHITE_LED#



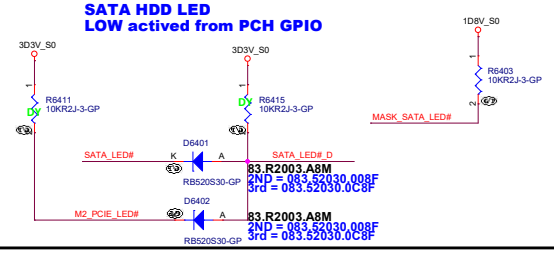
Main Func = HDD LED

[20,24] MASK_SATA_LED#

[18] SATA_LED#

[63] M2_PCIE_LED#

[20] SATA_LED#_D

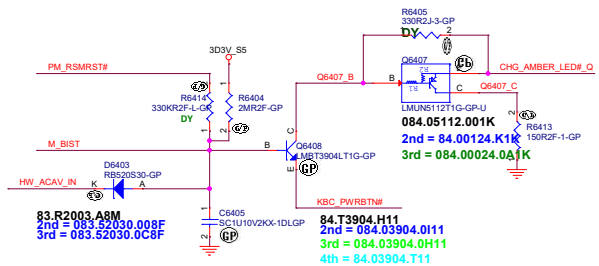


Main Func = M-BIST

[17] PM_RSMRST#

[24] M_BIST

[24,44] HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

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Title: LED Board&Power Button

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 64 of 105

Main Func = KB

[24] CAP_LED#_R

[4] KB_DET#

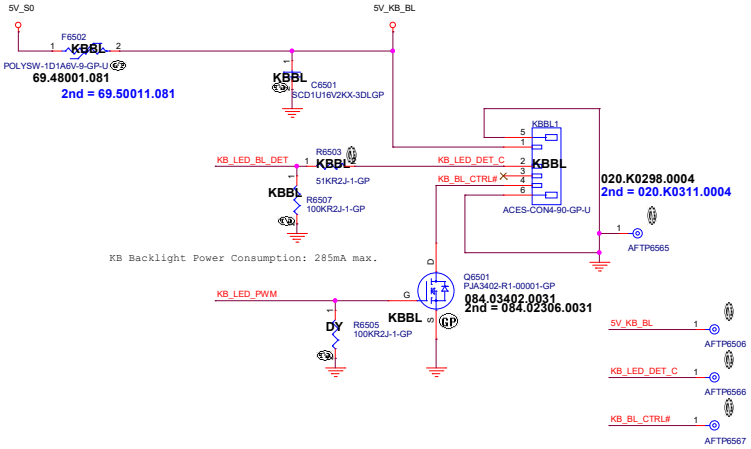
[20] KB_LED_BL_DET

[24] KB_LED_PWM

[24] KSO00
[24] KSO01
[24] KSO02
[24] KSO03
[24] KSO04
[24] KSO05
[24] KSO06
[24] KSO07
[24] KSO08
[24] KSO09
[24] KSO10
[24] KSO11
[24] KSO12
[24] KSO13
[24] KSO14
[24] KSO15
[24] KSO16

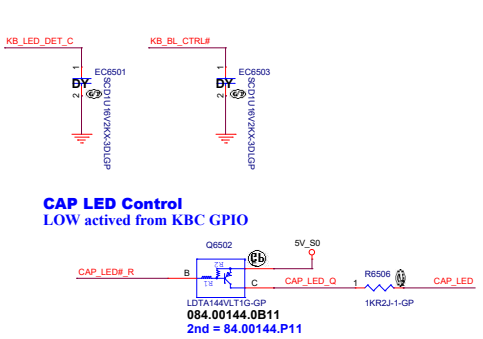
[24] KSI[0..7] — KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

Keyboard Backlight (Reserved)

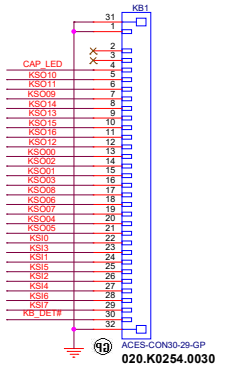


CAP LED Control

LOW actived from KBC GPIO



Internal Keyboard Connector

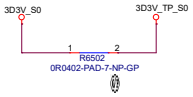


Main Func = TPAD

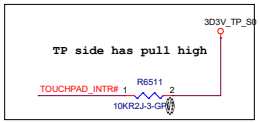
[24] EC_I2C_SDA_TP
[24] EC_I2C_SCL_TP

[20,66] CPU_I2C_SCL_P0
[20,66] CPU_I2C_SDA_P0

[3,24] TOUCHPAD_INTR#
[24] PTP_DIS#



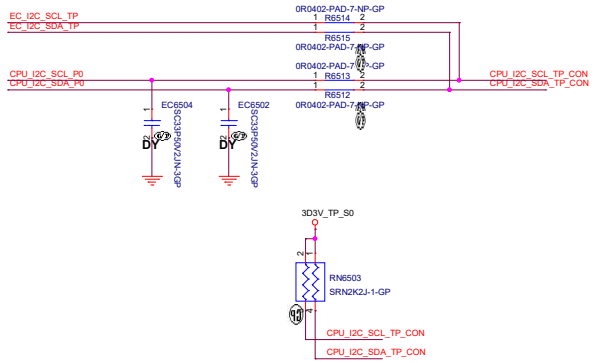
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



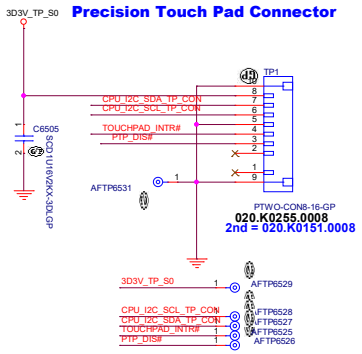
Support PTP

PS2

I2C



Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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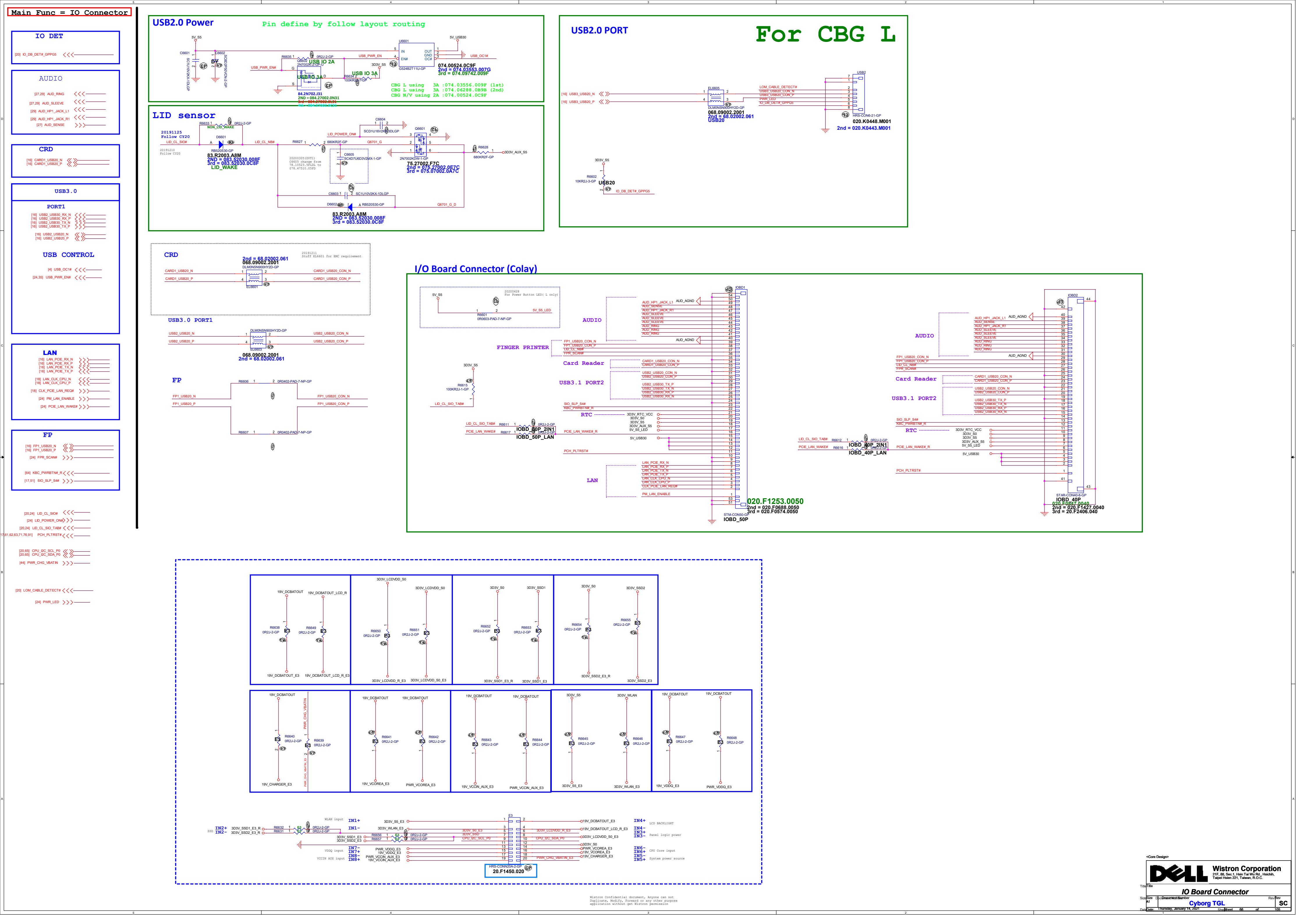
Title: Key Board&Touch Pad

Size: A2 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 65 of 105



Main Func = IO Connector
IO DET
AUDIO
CRD
USB3.0
PORT1
USB CONTROL
LAN
FP
USB2.0 Power
Pin define by follow layout routing
USB IO 2A
USB IO 3A
074.00524.0C9F
2nd = 074.03553.007G
3rd = 074.09742.009F
CBG L using 3A :074.03556.009F (1st)
CBG L using 3A :074.06288.0B9B (2nd)
CBG N/V using 2A :074.00524.0C9F
LID sensor
83.R2003.A8M
2ND = 083.52030.008F
3rd = 083.52030.0C8F
LID_WAKE
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.07002.0A7C
USB2.0 PORT
For CBG L
068.09002.2001
2nd = 68.02002.061
USB20
020.K0448.M001
2nd = 020.K0443.M001
CRD
USB3.0 PORT1
FP
I/O Board Connector (Colay)
AUDIO
FINGER PRINTER
Card Reader
USB3.1 PORT2
RTC
LAN
IOBD_50P_2IN1
IOBD_50P_LAN
020.F1253.0050
2nd = 020.F0688.0050
3rd = 020.F0574.0050
IOBD_50P
IOBD_40P_2IN1
IOBD_40P_LAN
IOBD_40P
020.F0547.0040
2nd = 020.F1427.0040
3rd = 20.F2406.040
20.F1450.020
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IO Board Connector
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Main Func = HALL SENSOR

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Title: Reserved

Size: A3 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 67 of 105

Main Func = Debug

ESPI

[18,24] ESPI_CLK
[18,24] ESPI_RESET#
[18,24] ESPI_CS#

[18,24] ESPI_IO0
[18,24] ESPI_IO1
[18,24] ESPI_IO2
[18,24] ESPI_IO3

UART

[24] HOST_DEBUG_TX
[20] CPU_UART2_TXD
[20] CPU_UART2_RXD

Follow upsell remove 3D3V_DB1

3D3V_S5
3D3V_S0
20191119
add net name

R6820 1 — 2 0R2J-2-GP — DY
R6821 1 — 2 0R2J-2-GP — DEBUG

HOST_DEBUG_TX — R6801 1 — 2 0R2J-2-GP — HOST_DEBUG_TX_CON — DEBUG
CPU_UART2_TXD — R6802 1 — 2 0R2J-2-GP — CPU_UART2_TXD_CON — DEBUG
CPU_UART2_RXD — R6803 1 — 2 0R2J-2-GP — CPU_UART2_RXD_CON — DEBUG

20191212
Follow CY20

3D3V_S0
R6804 1 — 2 51KR2J-1-GP — CPU_UART2_TXD — DEBUG
R6805 1 — 2 51KR2J-1-GP — CPU_UART2_RXD — DEBUG

ESPI Debug Connector

DBG1
ESPI_CLK
ESPI_RESET#
ESPI_CS#
ESPI_IO3
ESPI_IO2
ESPI_IO1
ESPI_IO0
3D3V_DB1
DEBUG
20.F0765.014
DM-ACES-CON14-5-GP-01
ZZ.F0765.01401

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Title: Dubug connector

Size	Document Number	Rev
A4	Cyborg TGL	SC

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Title: Reserved

Size	Document Number	Rev
A4	Cyborg TGL	SC

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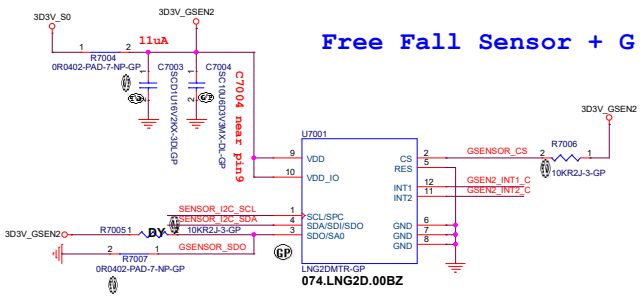
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

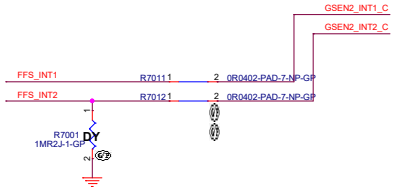
[20] GSEN2_INT1_C
[20,55] SENSOR_I2C_SCL
[20,55] SENSOR_I2C_SDA
[20] FFS_INT1
[19] FFS_INT2
[60] FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor

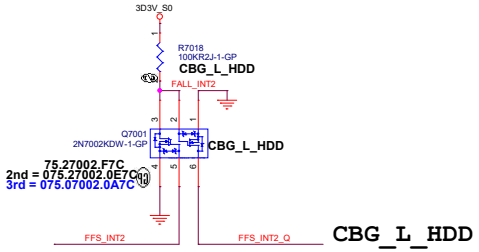


CBG L/WM using 8 Bits :074.LNG2D.00BZ
CBG N/V using 12 Bits :074.LIS2D.M002



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: Free Fall Sensor
Size: A2
Document Number: Cyborg TGL
Rev: SC
Date: Thursday, January 14, 2021
Sheet 70 of 105

Main Func = TBT

USB1

Type-C PD

HP team on applying, only murata have sample can meet Intel request
220nF AC cap must be placed on RX lines close to SOC side

TBT PORTS

Port A - Host Side

Port B - TypeC Side

BB

ZZ.000IC.002

HP team on applying ,only murata have sample can meet Intel request

MISC & DEBUG

BB TO PCH(TBT)

BB TO PCH(NON-TBT)

20200221 (DVT1)
Follow reference circuits NC _a12

Follow Hellcat15 Upsell TGL

	WPN	DPN
TBT	071.00TBT.0F0U	M11GX
NON_TBT	071.00TBT.0D0U	7DYVG

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Power

GND

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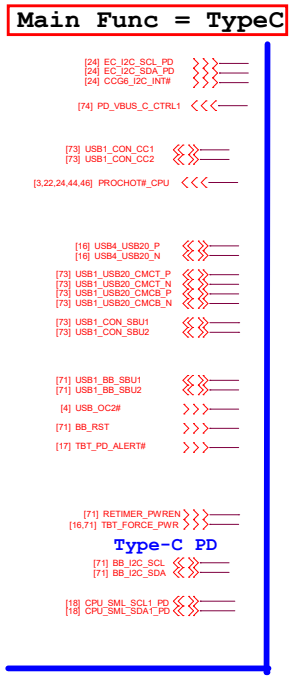
EXT IO (Thunderbolt(1/3)/Type C Re-driver)

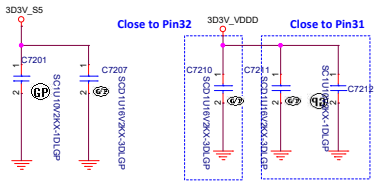
Cyborg TGL

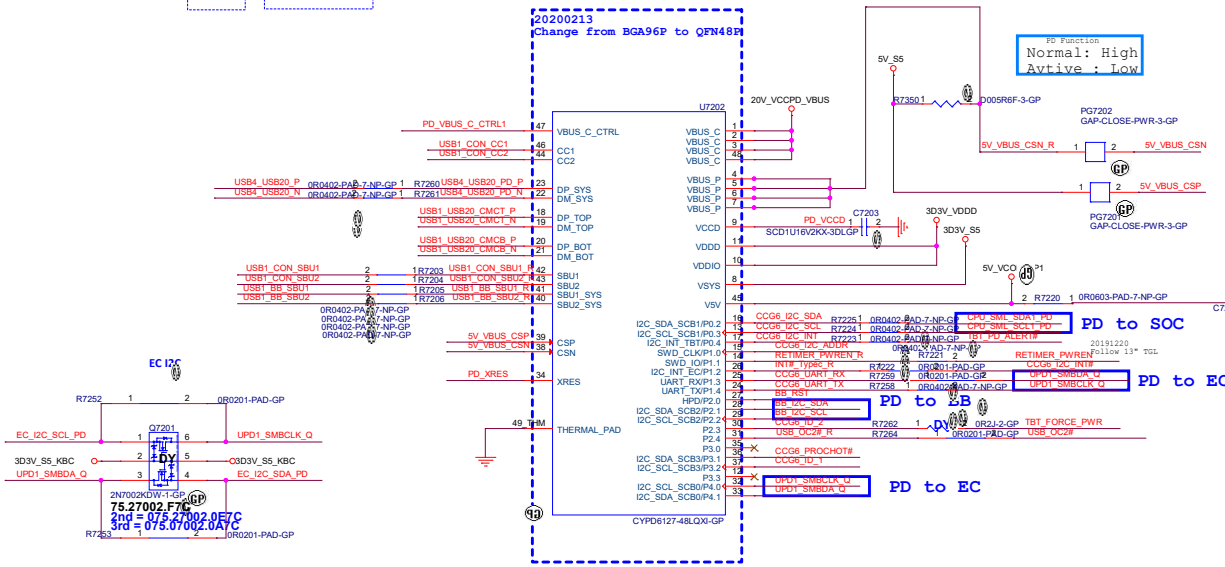
Thursday, January 14, 2021

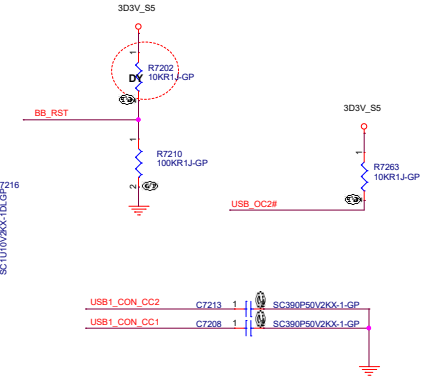
Follow Hellcat15 Upsell TGL

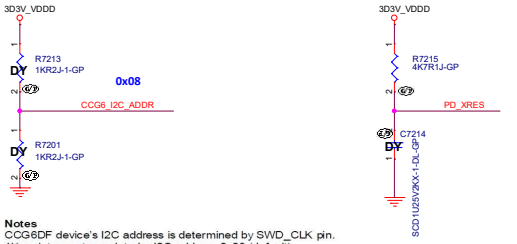
Main Func = TypeC



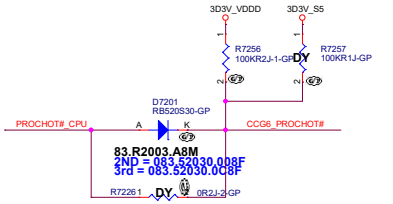




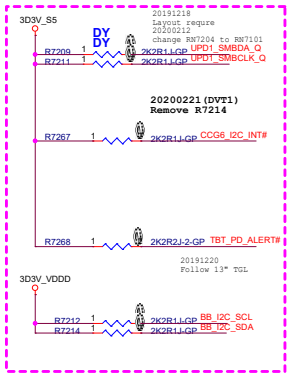




Notes
CCG6DF device's I2C address is determined by SWD_CLK pin.
1K resistors not populated = I2C address 0x08 (default)
1K resistor connected to GND = I2C address 0x40
1K resistor connected to VDDD = I2C address 0x42

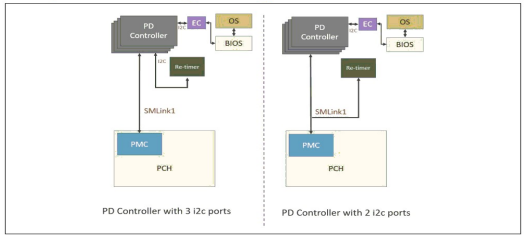


Dell TGL Platform MOD_ID Options NEW			
Project	**MOD_ID1**	**MOD_ID2**	**Description**
Hellcat 8040	L0	N/A	BB8040(Special for Hellcat)
Hellcat 8010	L2	N/A	BB8010(Special for Hellcat)
Moonknight N/V	L1	L0	TGL-U/BB8040/CCG6DF/SOC address 0x21 for P2
Cyborg TGL-U-8040	L1	L2	TGL-U/BB8040/CCG6SF
Moonknight L Cyborg TGL-U-8010 Watchman	L1	L1	TGL-U/BB8010/CCG6XF
	L3	L0	TGL-H/BB8040/CCG6DF
Stradale MLK	L3	L1	TGL-H/Cascade-BB8040/CCG6DF
Cyborg-TGL-H	L3	L2	TGL-H/BB8040/CCG6SF
	L3	L3	TGL-H/No RT application/CCG6SF
	L4	L0 - L2	PS8802(MFDP)

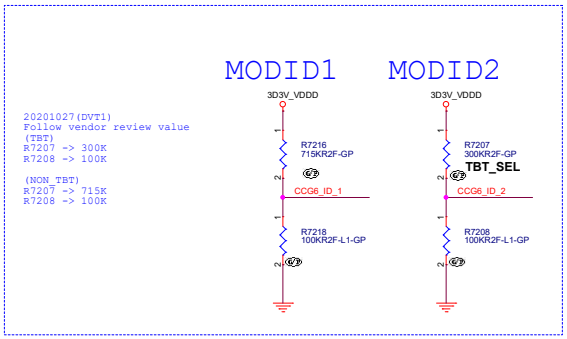


	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

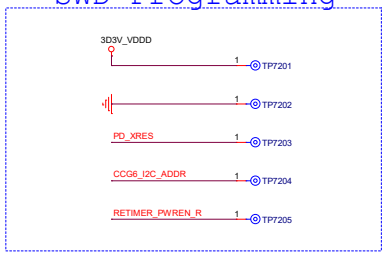
Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



MODID Setting



SWD Programming



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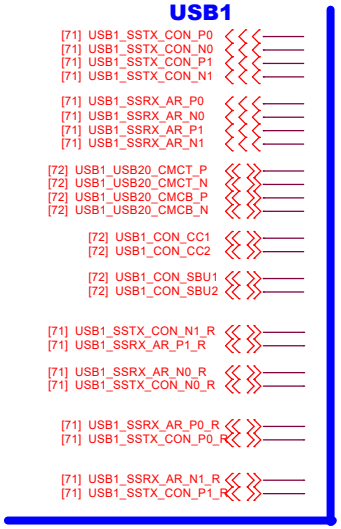
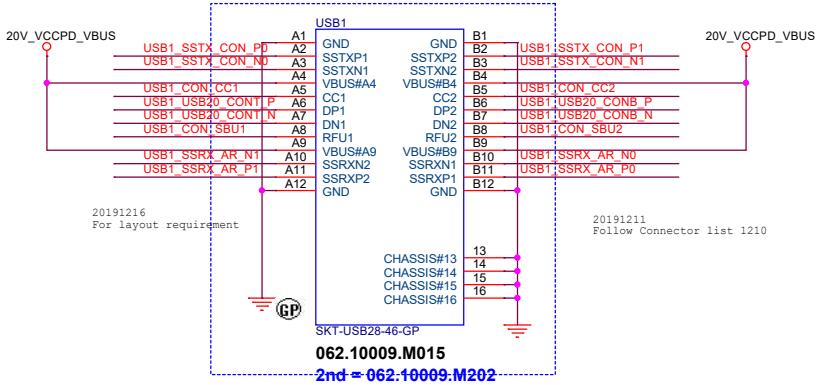
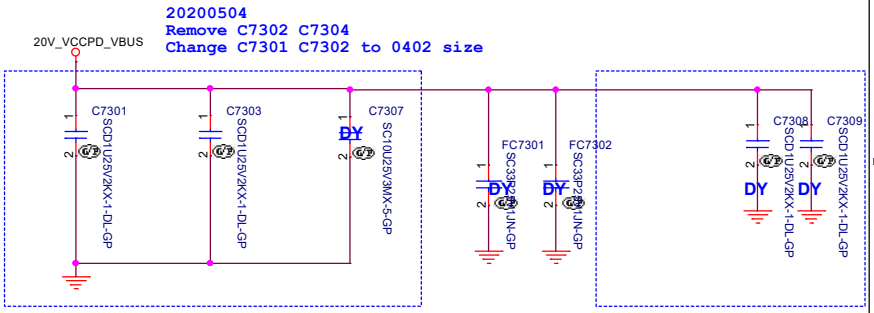
Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)
Size: A2 | Document Number: Cyborg TGL | Rev: SC
Date: Thursday, January 14, 2021 | Sheet 72 of 105

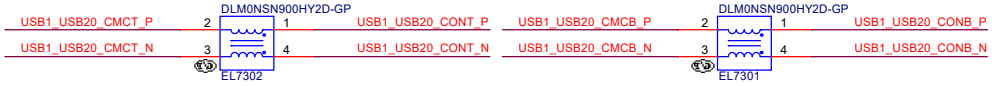
Main Func = TypeC







2020/02/29:swap EL7302/EL7301



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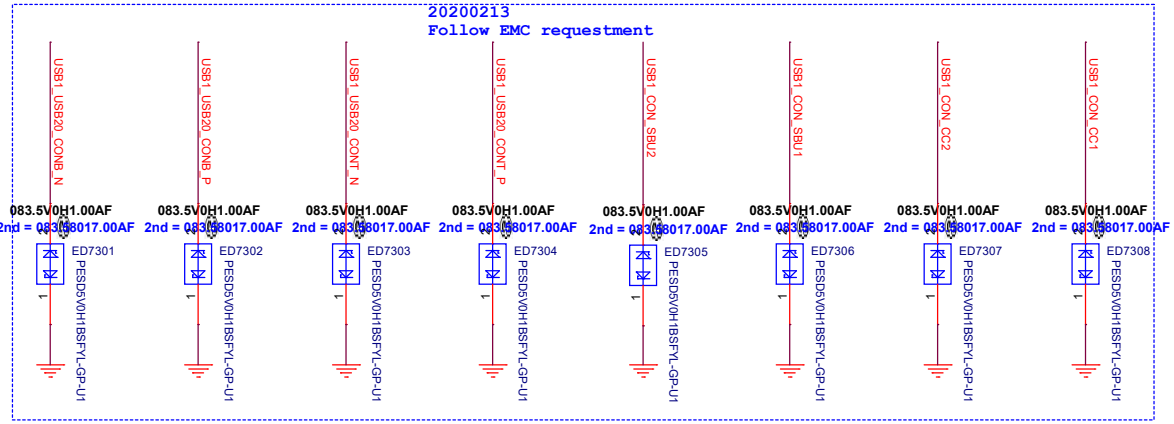

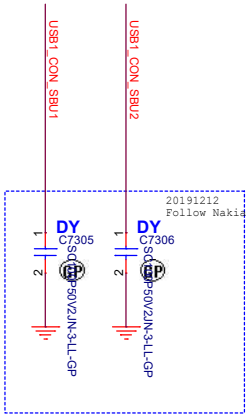

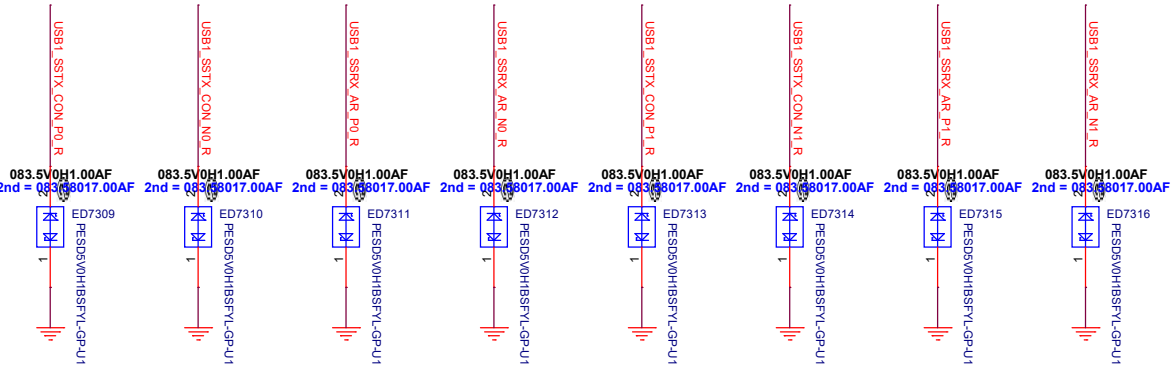

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Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

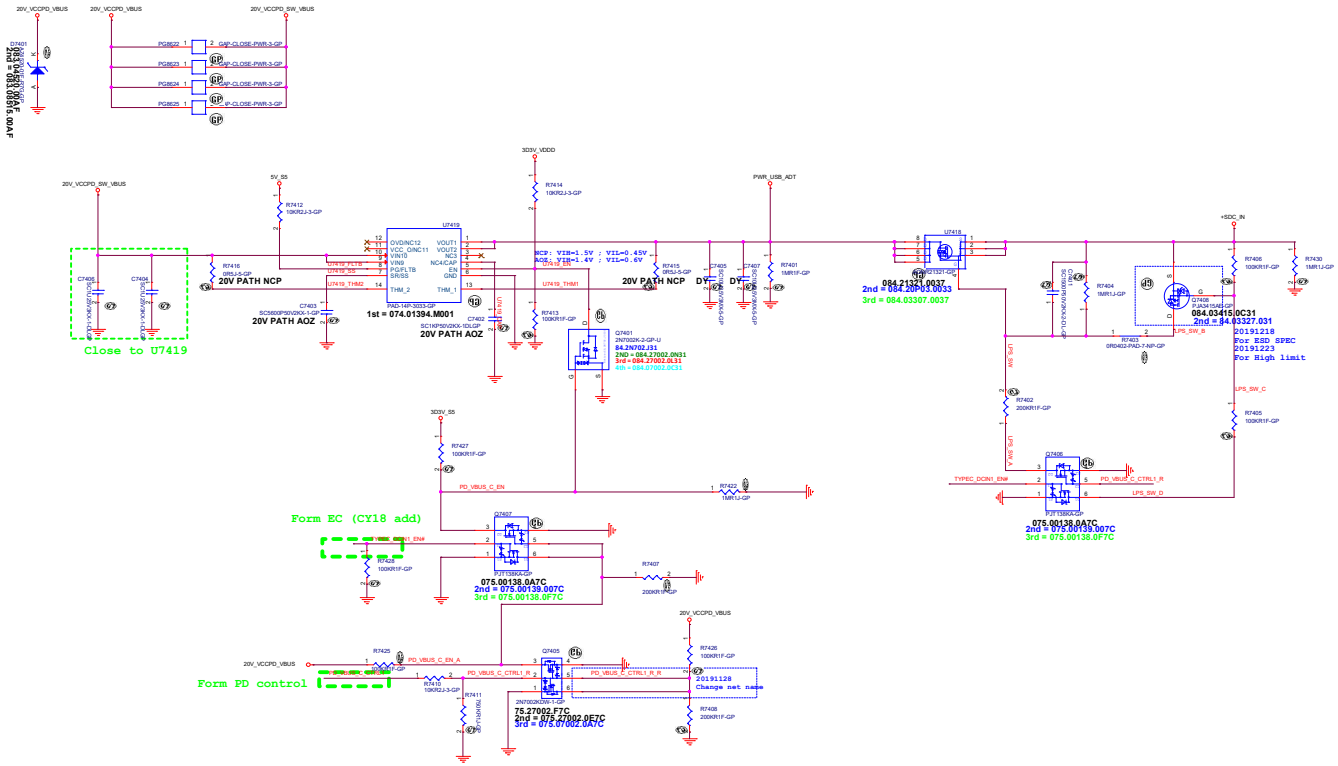
Size: A3 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 73 of 105

[72] PD_VBUS_C_CTRL1

[24] TYPEC_DCIN1_EN#

[44] U7419_FLTB



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Title: GPU(2/5)DIGITALOUT

Size: A1 | Document Number: Cyborg TGL | Rev: SC

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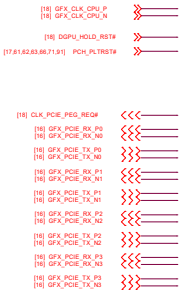
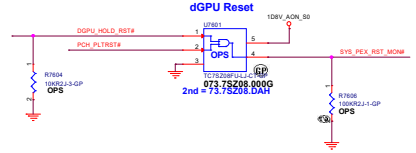
Title: *Reserved*

Size: A3 | Document Number: *Cyborg TGL* | Rev: *SC*

Date: Thursday, January 14, 2021 | Sheet 75 of 105

Main Func = dGPU





▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.

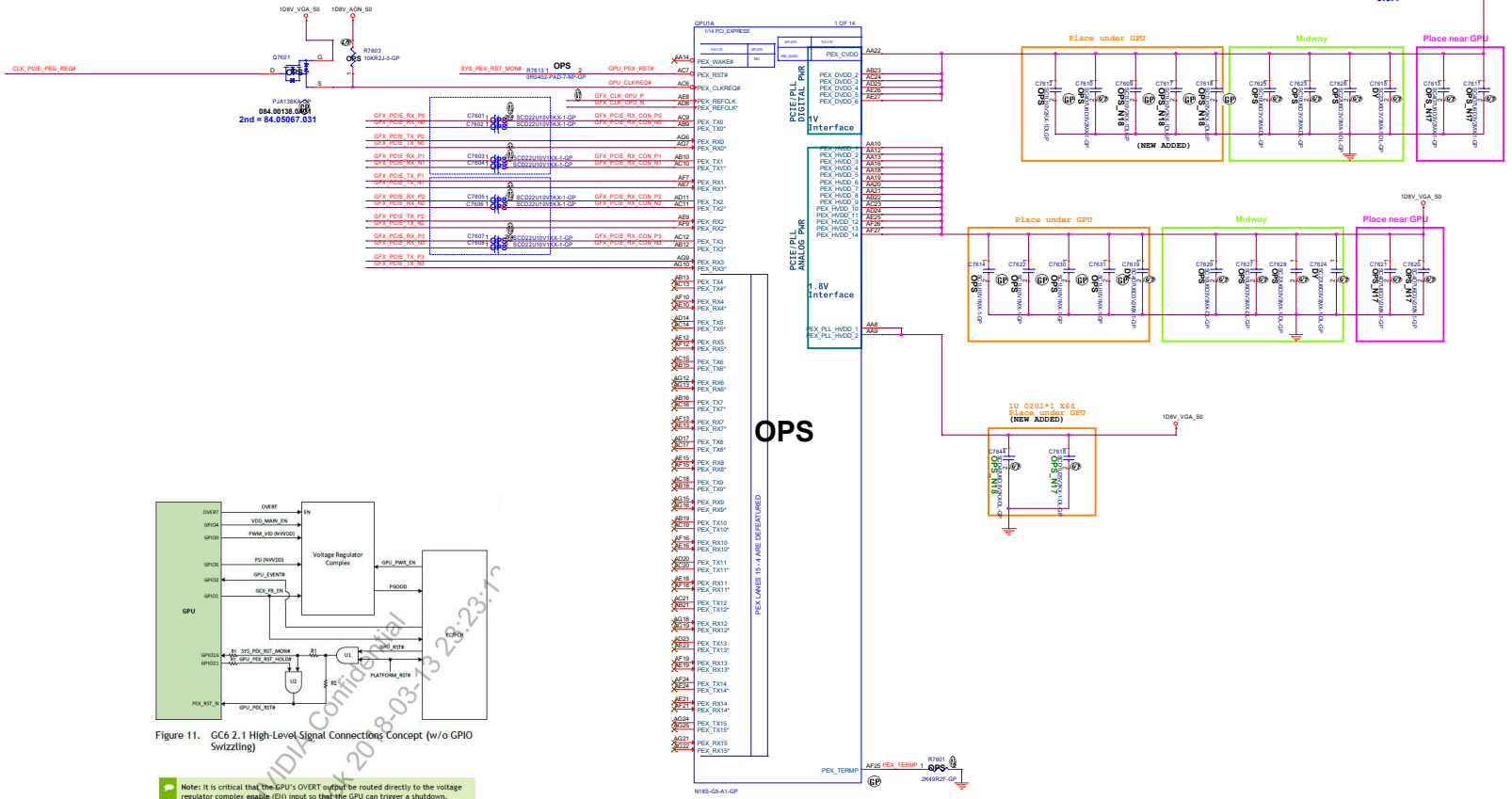
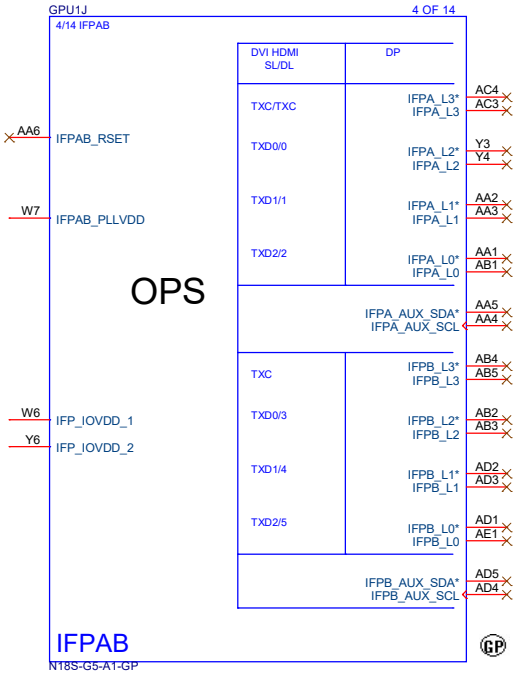
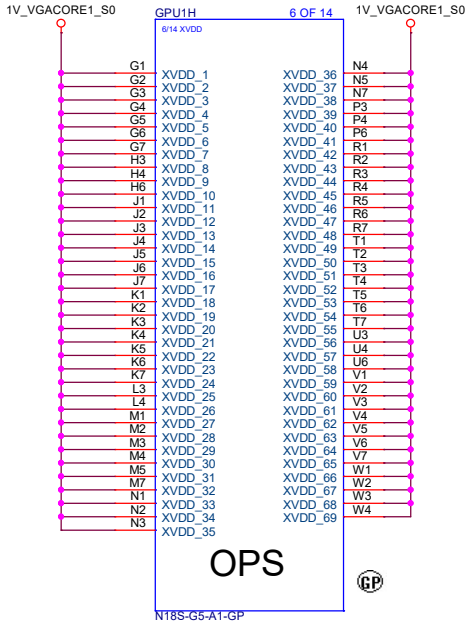


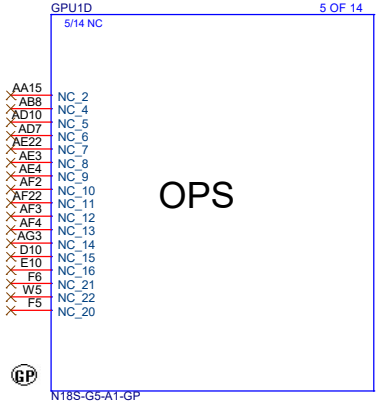
Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Main Func = dGPU







<Core Design>

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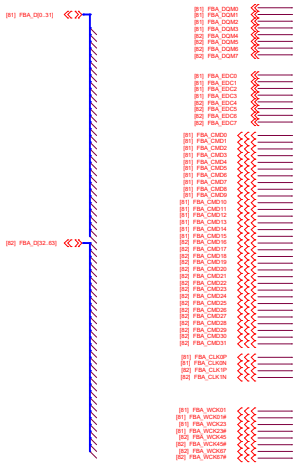
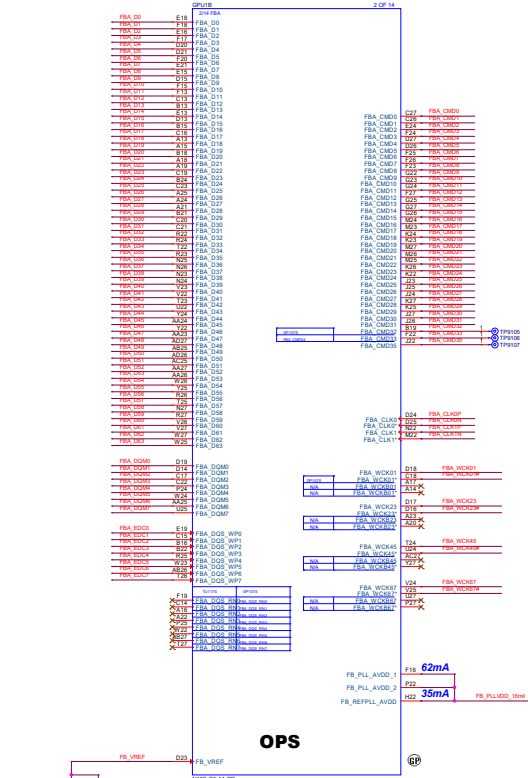
Title: GPU(2/5)DIGITALOUT

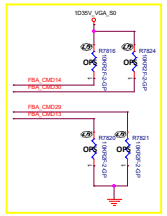
Size	Document Number	Rev
A3	Cyborg TGL	SC

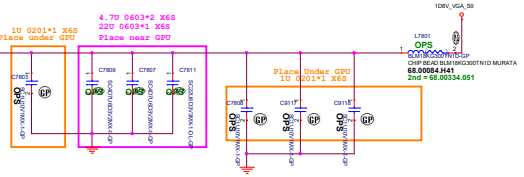
Date: Thursday, January 14, 2021 Sheet 77 of 105

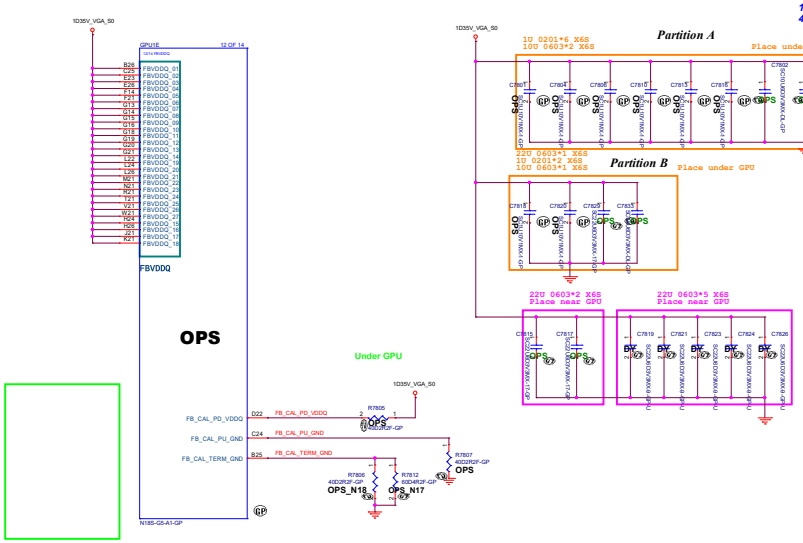
Main Func = dGPU











1.35V +/- 3%
4.88A

Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

Main Func = dGPU

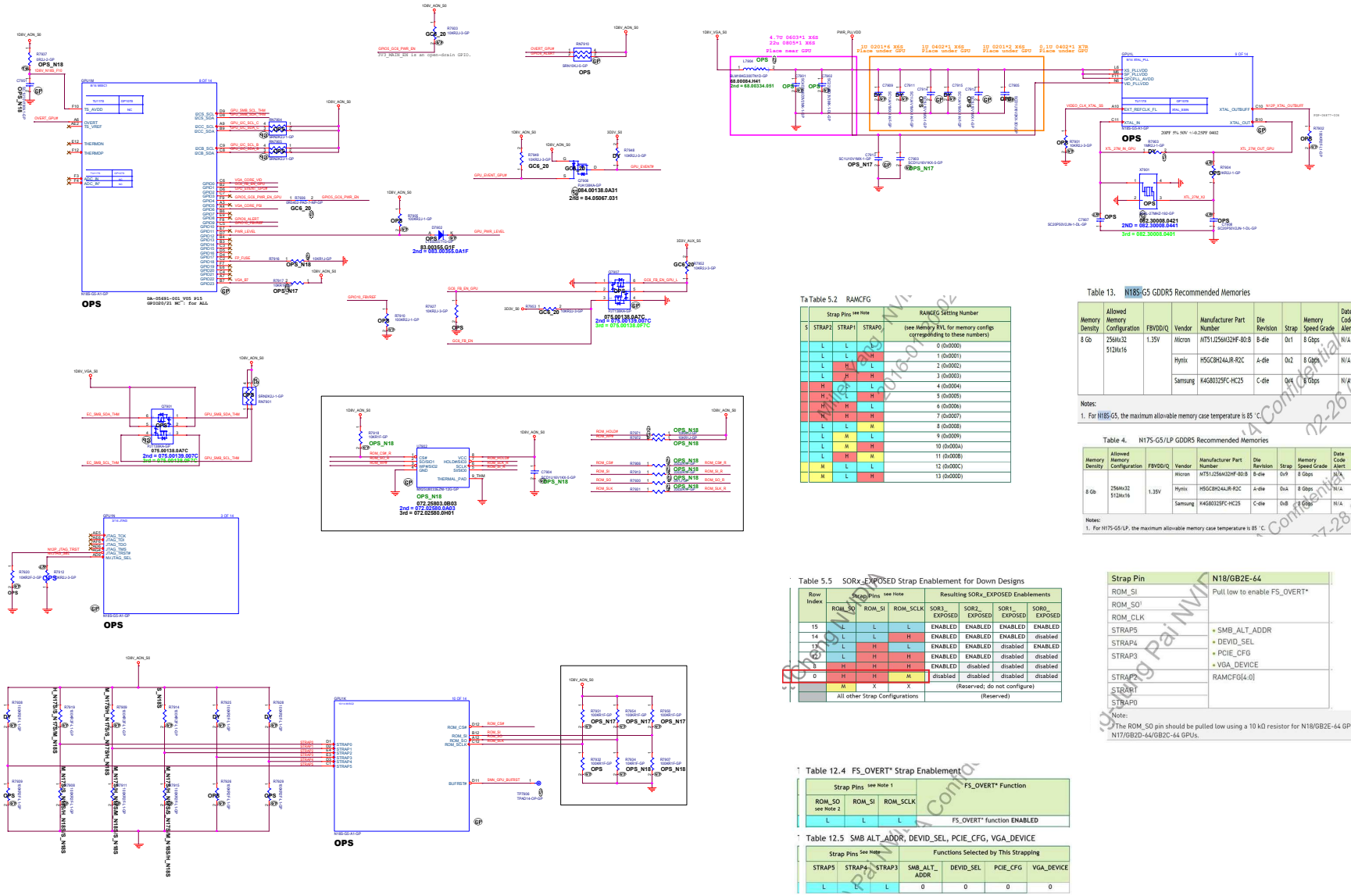


Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 13. N18S-G5 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x4	8 Gbps	N/A	Full	Production candidate

Notes:
1. For N18S-G5, the maximum allowable memory case temperature is 85 °C.

Table 4. N17S-G5/LP GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0xB	8 Gbps	N/A	Full	Production candidate

Notes:
1. For N17S-G5/LP, the maximum allowable memory case temperature is 85 °C.

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Strap Pin	N18/GB2E-64
ROM_SI	Pull low to enable FS_OVERT*
ROM_SO	
ROM_CLK	
STRAP5	• SMB_ALT_ADDR
STRAP4	• DEVID_SEL
STRAP3	• PCIE_CFG
	• VGA_DEVICE
STRAP2	RAMCFG[4:0]
STRAP1	
STRAP0	

Note:
The ROM_SO pin should be pulled low using a 10 kΩ resistor for N18/GB2E-64 GPUs and using a 100 kΩ resistor for N17/GB2D-64/GB2C-64 GPUs.

Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

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Cyborg TGL
GPU(4/5)GPIO/STRAP
SC

Main Func = dGPU

[79] FP_FUSE

[85] PWR_VGA_NVDDS_VSEN1_P_R

[85] PWR_VGA_NVDDS_VSEN1_N_R

1V_VGACORE1_S0

RF RESERVED

22U 0603*10 X6S
Place under GPU

10U 0603*14 X6S
Place under GPU

1U 0201*5 X6S
Place under GPU

GPU1C 11 OF 14

GPU1G 7 OF 14

GPU1U 13 OF 14

VDD_SENSE
GND_SENSE

PWR_VGA_NVDDS_VSEN1_P_R
PWR_VGA_NVDDS_VSEN1_N_R

N18S-GS-A1-GP

OPS

OPTIONAL GND:

XVDD AREA

PCB ADRCMD

PWR REFERENCE

3.3V +/- 5%
85mA

1DBV_VGA_S0

Under GPU

Near GPU

OPS_N17
(NEW ADDED)

1U 0201*2 X6S
Place under GPU

GPU1F 14 OF 14

1DBV_AON_S0

FP_FUSE_SRC

OPS_N18

R8004
2K21R2D-GP

U8001
SSQ7B11G-GP

074.05017.009Z
2nd = 074.04622.009Z

Place near GPU
1U 0201*3 X6S
4.7U 0603*3 X6S

<Core Design>

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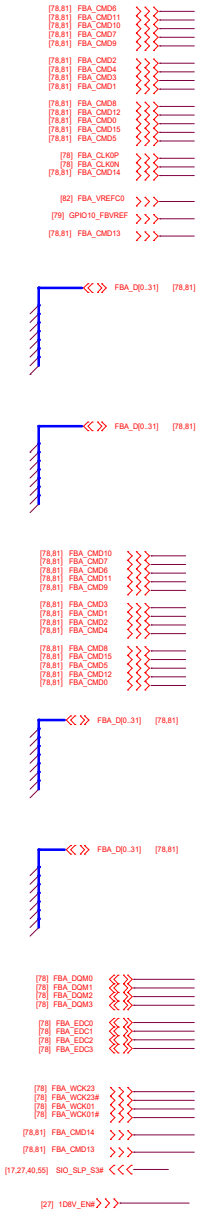
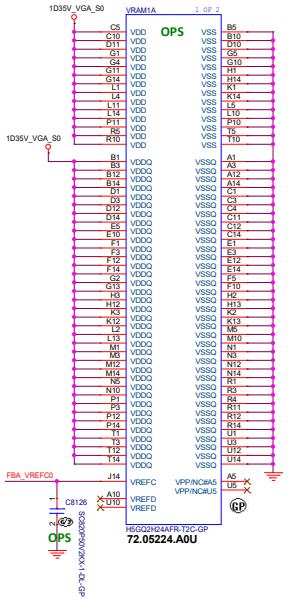
Title: GPU(5/5)PWR/GND

Size: A3 | Document Number: Cyborg TGL | Rev: SC

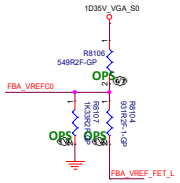
Date: Thursday, January 14, 2021 | Sheet 80 of 105

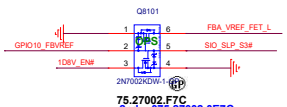
SSID = VRAM





Frame Buffer Patition A-Lower Half

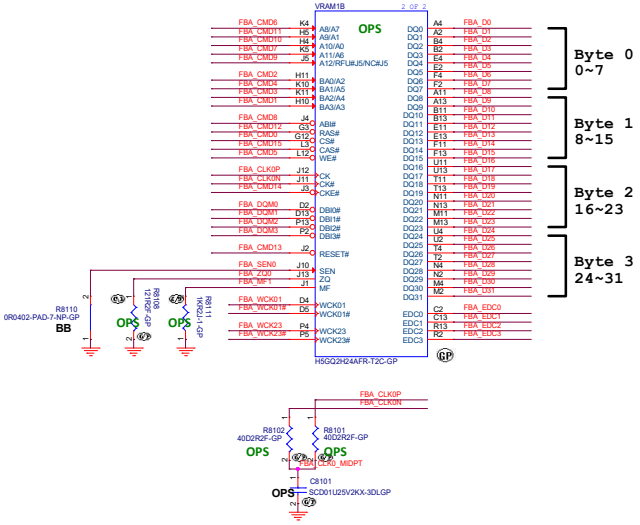




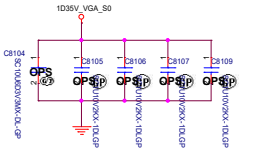
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

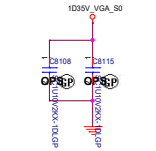
Normal(MF=0)



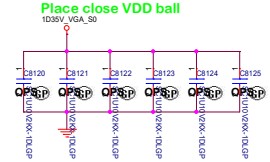
Place close VDD ball

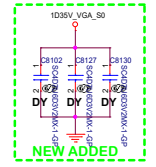


Place close VDD ball

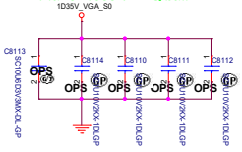


Place close VDD ball

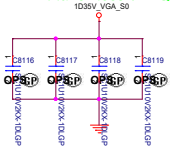




Place close VDDQ ball



Place close VDDQ ball



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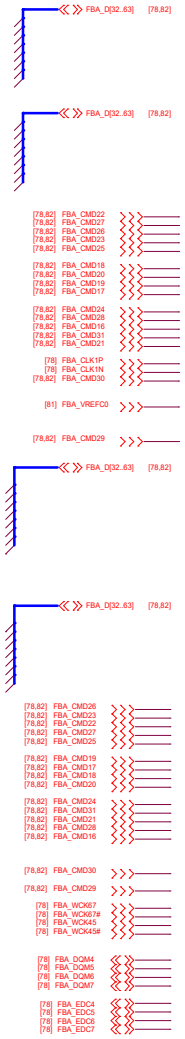
Title: **GPU-VRAM1,2 (1/4)**

Size	Document Number	Rev
Custom	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 81 of 105

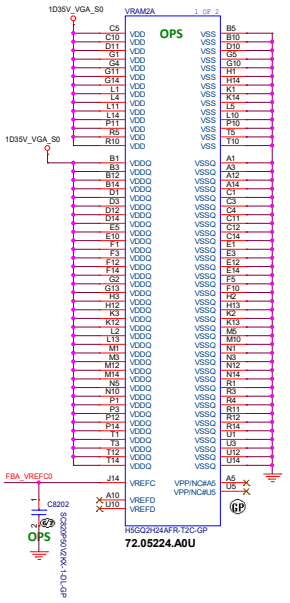
SSID = VRAM

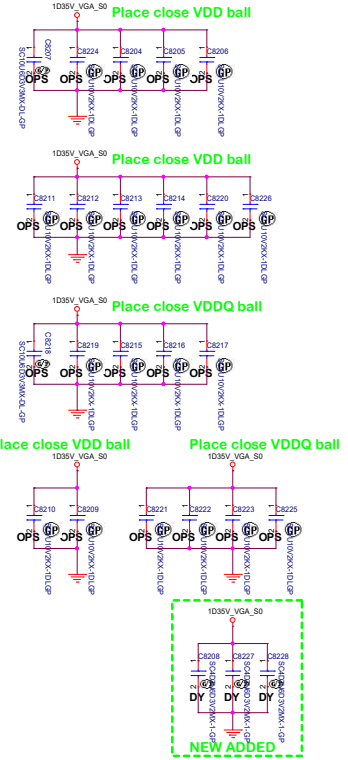
Frame Buffer Patition A-Upper Half

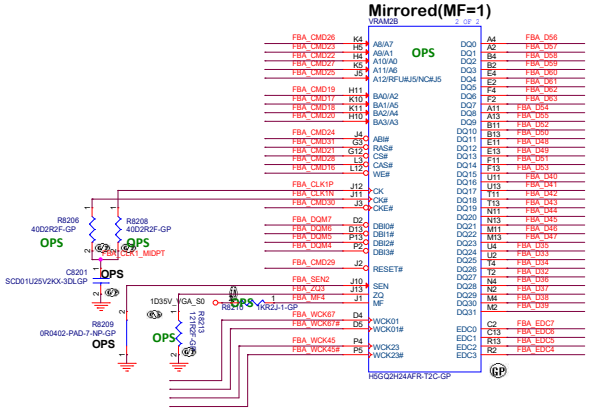


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low







<Core Design>

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Title: *GPU-VRAM3,4 (2/4)*

Size: Custom | Document Number: *Cyborg TGL* | Rev: *SC*

Date: Thursday, January 14, 2021 | Sheet 82 of 105

<Core Design>

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Title

GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 83 of 105

<Core Design>

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Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
A4	Cyborg TGL	SC

Date: Thursday, January 14, 2021 Sheet 84 of 105

OFFPAGE-Signal

OFFPAGE-GAP

RT8816B For NVVDDS

VGA : N17S-G3/G5
EDP-Peak : 69.9A

PH on EE side

1. Check EE side
2. Modify DAT

PH on EE side

EE need check

Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

For VGA_CORE sequence
EE need check

Table 1	
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

VGA : N17S-G5/N18S-G5
EDP:32.6A
EDP-Peak : 78A
93.6A<OCP<109.2A

PU8552 PU8554
For G5: 075.07362.0073

Rdson: 8.5~11.1m/2~2.6m (Q1/Q2)

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Iout : 41A

OPS_4ZA_GPU CORE

OCP setting

SS setting

Place Near GPU (NVVDDS)
1X330uF (Poscap) - PT8511 (Page85)

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (RT8816A_VGA)

Size: A1 | Document Number: Cyborg TGL | Rev: SC

Date: Thursday, January 14, 2021 | Sheet 85 of 105

Main Func = dGPU

Main Func = dGPU

[DG-07158-001 Rev03]Power up sequence:
3.3V ==> NVVDD (VGA_CORE) ==> PEX_VDD (1.05V) ==> PEXVDD/Q (1.35V)

3D3V_S0 to 3V3_AON_S0 and 3D3V_VGA_S0

1D8V_AON_S0 to 1D8V_VGA_S0

dGPU Power Discharge Circuit

1V_VGA_S0

VGA_CORE

1D35V_VGA_S0

1D8V_AON_S0

1D8V_VGA_S0

RT5797 for 1V_VGA_S0

For tuning VGA_CORE sequence.

TDC=0.2A
ICCMAX=0.3A
0.36A<OCP<0.48A

1D35V_VGA_S0

SY8288RAC for 1D35V

TDC=5.8A
ICCMAX=7.4A
8.88A<OCP<11.84A

OCP setting	
High	16A
Float	12A
Low	8A

Wistron Corporation	
DISCRETE VGA POWER	
Cyborg 7GL	8C

Main Func = dGPU

<Core Design>

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Title: ***Reserved***		
Size: A3	Document Number: ***Cyborg TGL***	Rev: ***SC***
Date: Thursday, January 14, 2021	Sheet 87 of 105	

(Blanking)

<Core Design>

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Title	***Reserved***	
Size: A4	Document Number: ***Cyborg TGL***	Rev: ***SC***
Date: Thursday, January 14, 2021	Sheet 88 of 105	

Main Func = UnusedParts

LAN PORT

H8
HOLE335R178-GP
ZZ.00PAD.7F1

Fix PCB BD

H12
HOLE256R142-1-GP
ZZ.PAD01.V91

For WLAN

HS1
STF237R113H91-GP
434.0HH0K.0001

For Cable ARRANGEMENT

CLIP1
SPRING-39-GP-U
34.49U01.001
CHIP1_N14_V14

For ME

H13
HOLE
ZZ.0HOLE.XXX
PCB Footprint = HT12X12B10X10R45

CPU SKREW HOLE

H1 HOLE233R150-GP — ZZ.00PAD.WN1
H2 HOLE233R150-GP — ZZ.00PAD.WN1
H3 HOLE233R150-GP — ZZ.00PAD.WN1
H4 HOLE233R150-GP — ZZ.00PAD.WN1

GPU SKREW HOLE

H5 HOLE276R154-GP — ZZ.00PAD.2T1
H6 HOLE276R154-GP — ZZ.00PAD.2T1
H7 HOLE276R154-GP — ZZ.00PAD.2T1

TYPEC SKREW HOLE

H10
HOLE256R142-1-GP
ZZ.PAD01.V91

For Factory requirement

TP8901 TP8902 TP8903 TP8904 TP8905 TP8906 TP8907 TP8908

Main Func = EMI Capacitors

Mind the voltage rating of the caps.

[43,44] 19V_AD_JK_C

19V_DCBATOUT

EC8917 SC1U25V2KX-1DLGP
EC8916 SC1U25V2KX-1DLGP
EC8883 SC1U25V2KX-1DLGP
EC8925 SC1U25V2KX-1DLGP
EC8915 SC1KF50V2KX-1DLGP
EC8928 SC1KF50V2KX-1DLGP
EC8929 SC1KF50V2KX-1DLGP
EC8911 SC1KF50V2KX-1DLGP

20191218
For EMC required

20200324(DVT2)
change .1u 50V to common .1u 25V

EC8958 SCD1U25V2KX-1DLGP

1D2V_S3

EC8901 SC1KF50V2KX-1DLGP
EC8902 SC1KF50V2KX-1DLGP
EC8903 SC1KF50V2KX-1DLGP
EC8904 SC1KF50V2KX-1DLGP
EC8905 SC1KF50V2KX-1DLGP
EC8906 SC1KF50V2KX-1DLGP
EC8907 SC1KF50V2KX-1DLGP
EC8908 SC1KF50V2KX-1DLGP

19V_DCBATOUT

EC8918 SCD1U25V2KX-1DLGP
EC8920 SCD1U25V2KX-1DLGP
EC8921 SCD1U25V2KX-1DLGP
EC8922 SCD1U25V2KX-1DLGP
EC8923 SCD1U25V2KX-1DLGP
EC8924 SC1KF50V2KX-1DLGP
EC8926 SC1KF50V2KX-1DLGP
EC8927 SC1KF50V2KX-1DLGP
EC8930 SC1KF50V2KX-1DLGP

20191224
For EMC required

20191204
For EMC request
放在 R4701 R4702旁

19V_DCBATOUT

EC8957 SCD1U25V2KX-1DLGP
EC8962 SCD1U25V2KX-1DLGP
EC8963 SCD1U25V2KX-1DLGP

+SDC_IN

EC8969 SCD1U25V2KX-1DLGP
EC8970 SCD1U25V2KX-1DLGP
EC8971 SCD1U25V2KX-1DLGP
EC8972 SC1KF50V2KX-1DLGP
EC8973 SC1KF50V2KX-1DLGP
EC8974 SCD1U25V2KX-1DLGP

20191213
for High limit

EC8913 SCD1U25V2KX-1DLGP
EC8932 SCD1U25V2KX-1DLGP

1V_CPU_CORE

EC8975 SCD1U16V2KX-3DLGP
EC8976 SCD1U16V2KX-3DLGP
EC8977 SCD1U16V2KX-3DLGP

3D3V_S0

EC8951 SC1U10V2KX-1DLGP
EC8953 SC1U10V2KX-1DLGP
EC8954 SCD1U16V2KX-3DLGP
EC8956 SCD1U16V2KX-3DLGP
EC8958 SCD1U16V2KX-3DLGP
EC8964 SCD1U16V2KX-3DLGP

19V_DCBATOUT

EC8909 SC1KF50V2KX-1DLGP
EC8910 SC1KF50V2KX-1DLGP
EC8912 SC1KF50V2KX-1DLGP

20191224
For EMC required

5V_S0

EC8933 SC1U10V2KX-1DLGP
EC8934 SC1U10V2KX-1DLGP
EC8935 SC1U10V2KX-1DLGP
EC8936 SC1U10V2KX-1DLGP
EC8937 SC1U10V2KX-1DLGP
EC8938 SC1U10V2KX-1DLGP
EC8939 SC1U10V2KX-1DLGP

5V_S5

EC8947 SC1U10V2KX-1DLGP
EC8948 SC1KF50V2KX-1DLGP
EC8949 SC1KF50V2KX-1DLGP

1V_VGACORE1_S0

EC8961 SCD1U16V2KX-3DLGP
EC8965 SCD1U16V2KX-3DLGP
EC8966 SCD1U16V2KX-3DLGP
EC8967 SCD1U16V2KX-3DLGP
EC8968 SCD1U16V2KX-3DLGP

19V_DCBATOUT

EC8982 SCD1U25V2KX-1DLGP
EC8983 SCD1U25V2KX-1DLGP

優先放在PC4705旁邊
或相對PC4705的Top層

優先放在PC4717旁邊
或相對PC4717的Top層

1D8V_CPU_AUX

EC8989 SC1U10V2KX-1DLGP
EC8990 SC1U10V2KX-1DLGP
EC8991 SC1U10V2KX-1DLGP

19V_DCBATOUT

EC8985 SCD1U25V2KX-1DLGP

20V_DCBATOUT

EC8986 SC47U1MX-1GP

PWR_DCBATOUT_1D35V

EC8987 SCD1U25V2KX-1DLGP

Main Func = RF Capacitors

Mind the voltage rating of the caps.

3D3V_S5

FC8901 SC10U6D3V2AN-4DLGP
FC8903 SC10U6D3V2AN-4DLGP
FC8904 SCD1U16V2KX-3DLGP
FC8905 SC4D7P50V2BN-2GP
FC8936 SCD1U16V2KX-3DLGP
FC8937 SC6P50V2CN-1NLGP
FC8938 SC6P50V2CN-1NLGP
FC8939 SC4D7P50V2BN-2GP

5V_S5

FC8906 SC10U6D3V2AN-4DLGP
FC8907 SC10U6D3V2AN-4DLGP
FC8941 SC4D7P50V2BN-2GP
FC8909 SCD1U16V2KX-3DLGP
FC8940 SCD1U16V2KX-3DLGP
FC8908 SCD1U16V2KX-3DLGP
FC8942 SCD1U16V2KX-3DLGP
FC8943 SCD1U16V2KX-3DLGP

19V_DCBATOUT

FC8916 SC10U6D3V2KX-1DLGP
FC8917 SC10U6D3V2KX-1DLGP
FC8918 SC4D7P50V2BN-2GP
FC8922 SC4D7P50V2BN-2GP
FC8921 SC4D7P50V2BN-2GP
FC8920 SCD1U25V2KX-1DLGP
FC8923 SCD1U25V2KX-1DLGP
FC8924 SCD1U25V2KX-1DLGP
FC8957 SC4D7P50V2BN-2GP
FC8959 SC4D7P50V2BN-2GP
FC8960 SC6P50V2JN-4DLGP
FC8961 SC6P50V2JN-4DLGP
FC8962 SC6P50V2JN-4DLGP
FC8963 SC6P50V2JN-4DLGP
FC8964 SCD1U25V2KX-1DLGP

3D3V_S0

FC8948 SC4D7P50V2BN-2GP
FC8949 SC4D7P50V2BN-2GP
FC8950 SCD1U16V2KX-3DLGP
FC8951 SC6P50V2JN-4DLGP
FC8952 SCD1U16V2KX-3DLGP
FC8954 SC6P50V2JN-4DLGP

1D2V_S3

FC8955 SC1P50V2JN-1DLGP
FC8956 SC1P50V2JN-1DLGP
FC8958 SC1P50V2JN-1DLGP
FC8902 SC1P50V2JN-1DLGP

1V_CPU_CORE

FC8925 SC1P50V2JN-1DLGP
FC8926 SC1P50V2JN-1DLGP
FC8927 SC1P50V2JN-1DLGP
FC8928 SC1P50V2JN-1DLGP
FC8929 SC1P50V2JN-1DLGP
FC8930 SC1P50V2JN-1DLGP

1D8V_CPU_AUX

FC8931 SC1P50V2JN-1DLGP
FC8932 SC1P50V2JN-1DLGP
FC8933 SC1P50V2JN-1DLGP
FC8934 SC1P50V2JN-1DLGP
FC8935 SC1P50V2JN-1DLGP
FC8953 SC1P50V2JN-1DLGP

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Title: UNUSED PARTS/EMI Capacitors
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Title	***Reserved***	
Size: A4	Document Number: ***Cyborg TGL***	Rev: ***SC***
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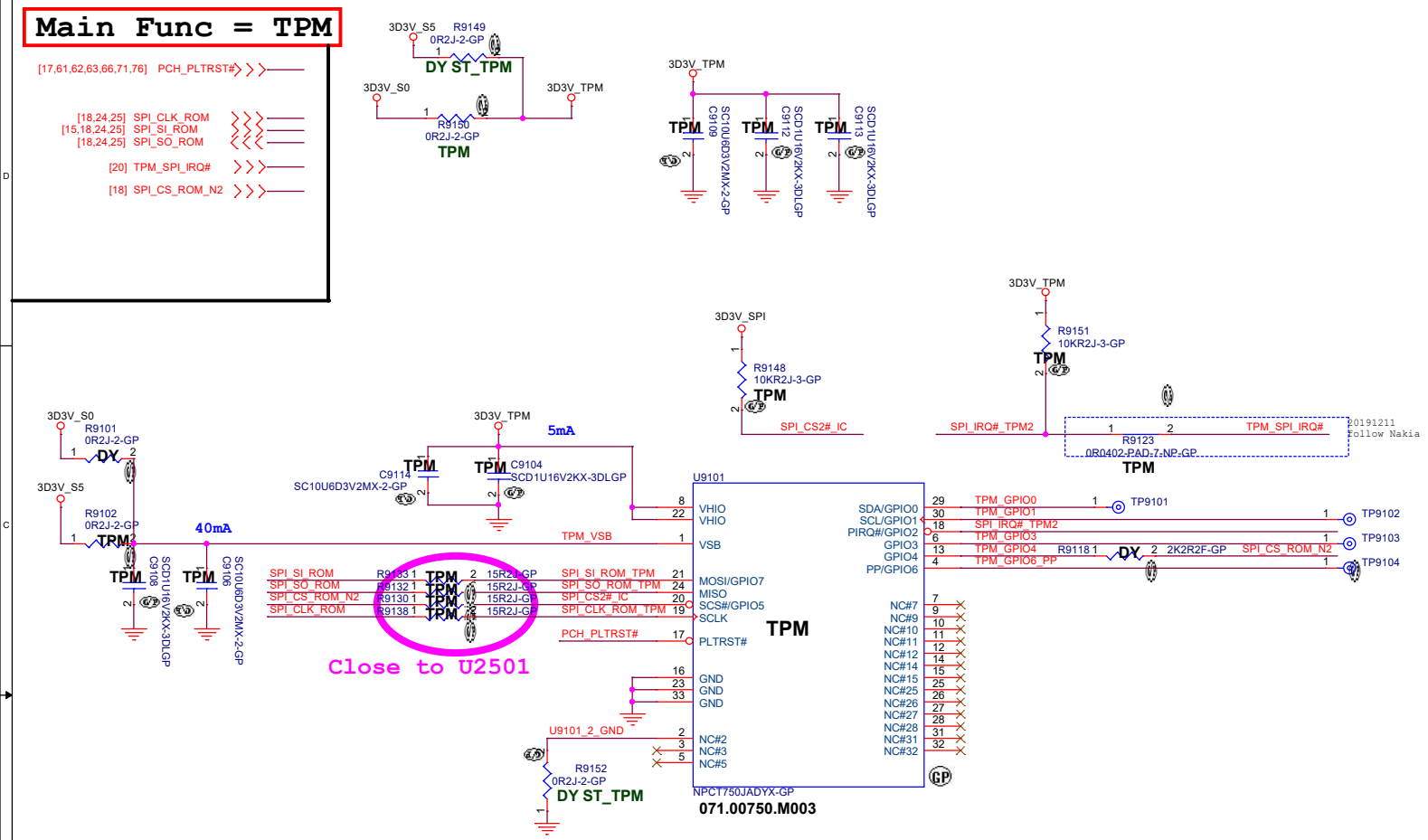
Main Func = TPM

For CBG V/L



<Core Design>

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Title: INT IO (TPM)

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SSID = Finger Print

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Title: Finger Print

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20200915
Remove

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Title: SITP

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Title
LVDS_Switch

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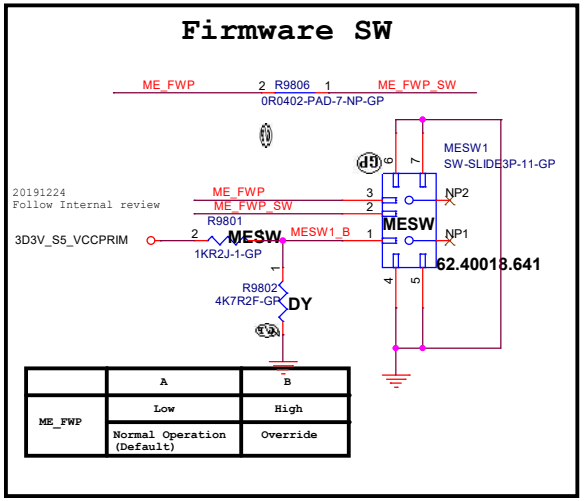
Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

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Title: CRT_Switch

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Title

Debug (XDP debug)

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CLK Block Diagram

TBD

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Title: CLK Block Diagram

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

Size	Document Number	Rev
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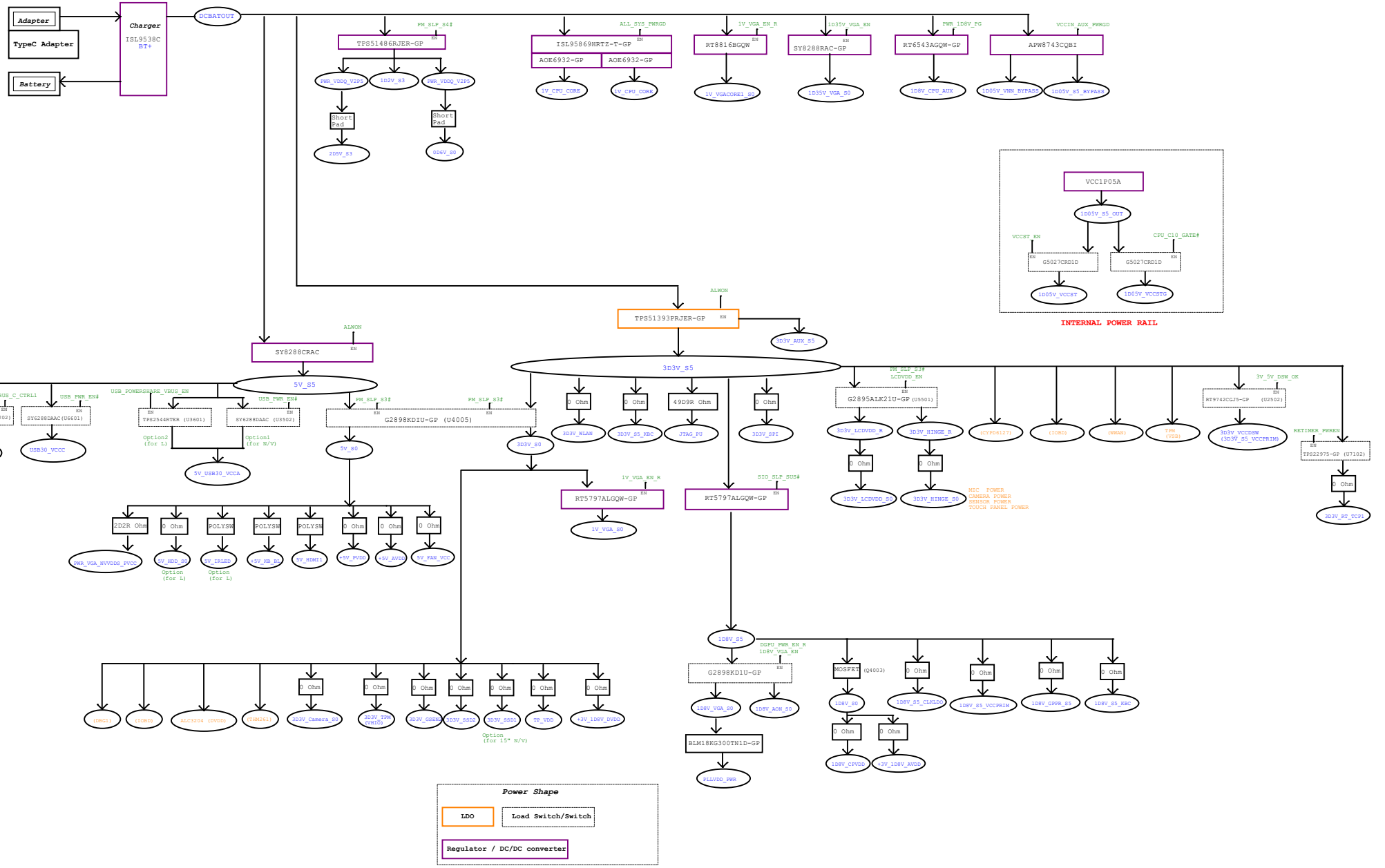
TBD



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Title: Power Block Diagram

Size	Document Number	Rev
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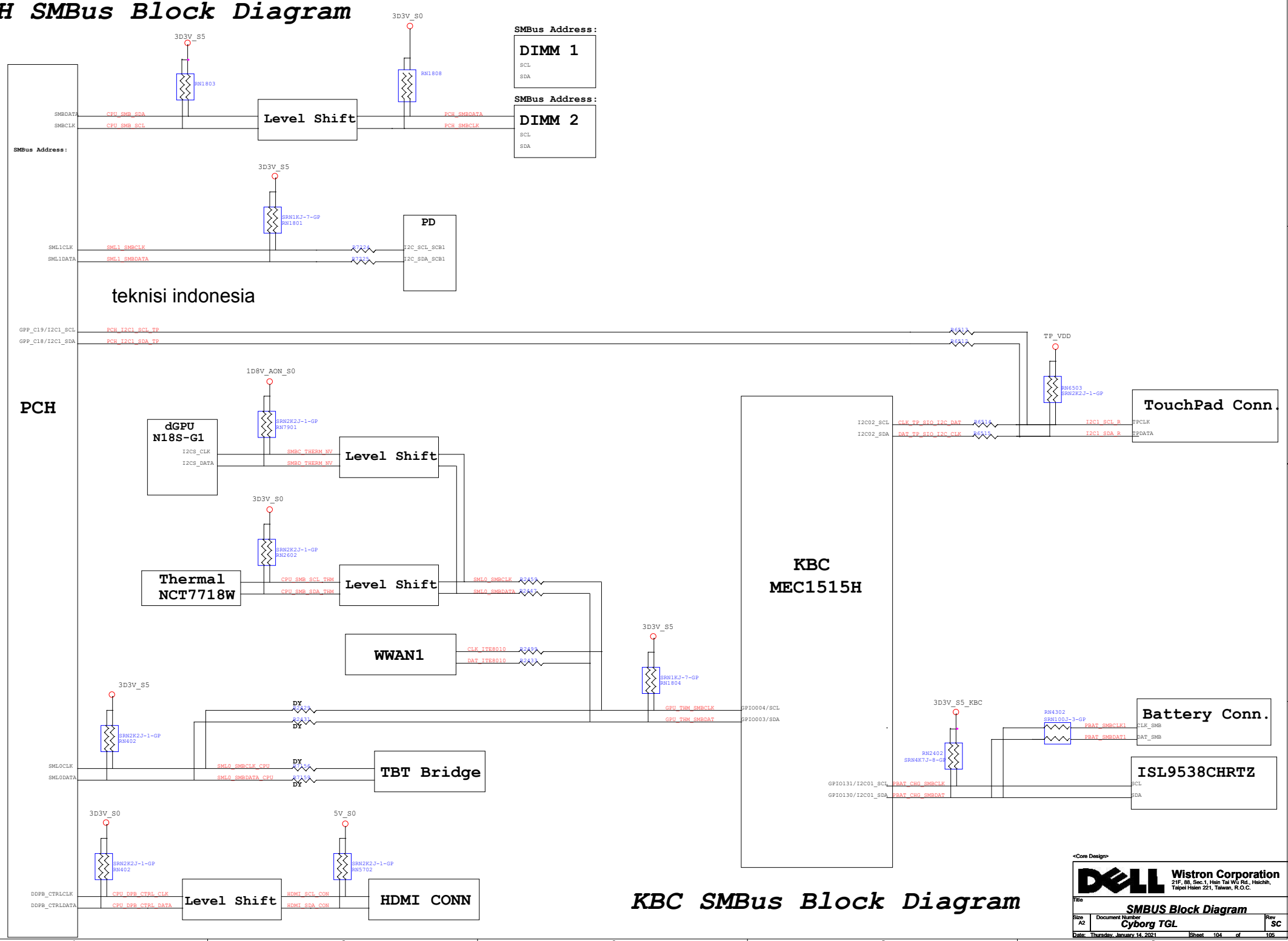
PCH SMBus Block Diagram



KBC SMBus Block Diagram

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Title: SMBUS Block Diagram

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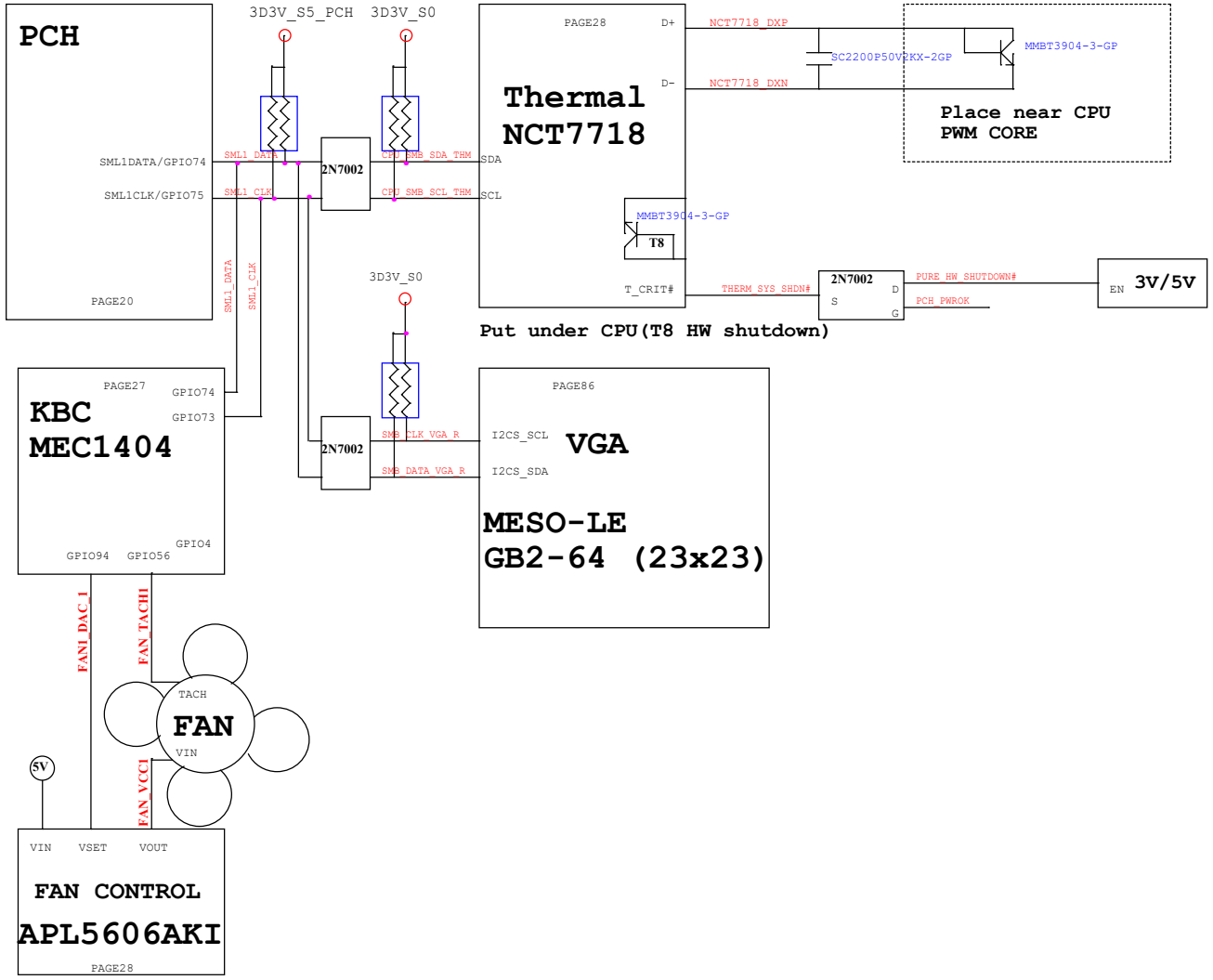
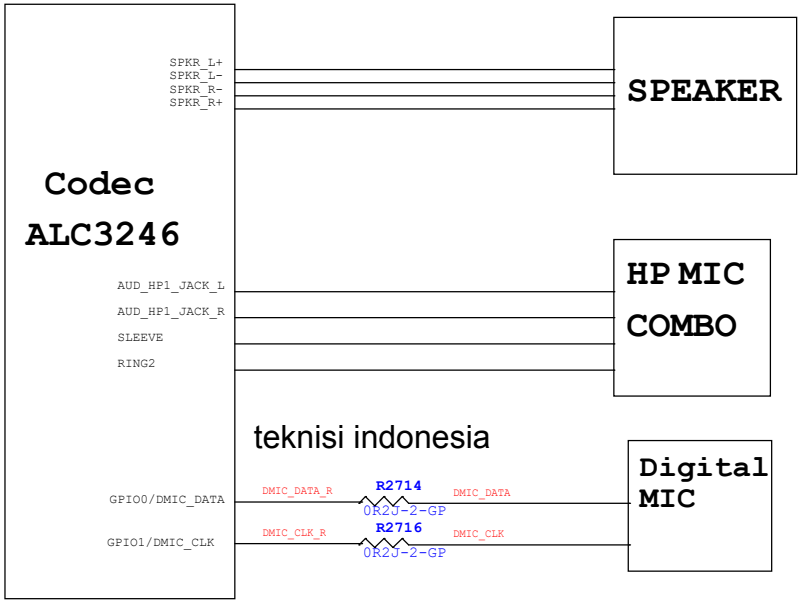
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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