DW30 Winery CALPELLA DIS N11M-GE1 Schematics

uFCPGA Mobile Arrandale

Intel Ibex Peak-M

2009-09-01

REV : SA

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

1st Samsung

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Title: Cover Page

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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Winery CALPELLA Block Diagram

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Project code : 91.4EX01.001
Part Number : 48.4EX11.0SA
PCB P/N : 09288
Revision : SA

Clock Generator SLG8SP585 7

VRAM(gDDR3) 64Mbx16x4 (512MB) 84,85
VRAM
Nvidia N11M-GE1(40nm) 80,81,82,83
100MHz/ 2.5Gbps
PCIe x 16
Bandwidth :8GB
Intel CPU Arrandale 8,9,10,11,12,13,14

DDRIII 1066 Channel A 800/1066MHz
DDRIII 1066 Slot 0 18
DDR III 1066 Channel B 800/1066MHz
DDRIII 1066 Slot 1 19

Power SW TPS2231R 34
New Card (FPC Cable to Connect) 34
PCIE x 1 & USB 2.0 x 1

LVDS
RGB CRT
CRT 55
LCD (Single Chanel) 54
Switchable 74

DMIx4 2.5 GT/s
FDI (UMA) 2.7 GT/s
100MHz 2.5Gbps PCIE

PCIE x 1
10/100/1000LOM RTL8111DL 35
RJ45 CONN
USB 2.0 x 2
PCIE x 1
Mini-Card WWAN/ WiMAX?
USB 2.0 x 1
Left Side: USB x 1
(On daughter board)

Intel PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

USB 2.0 480Mbps
USB 2.0 x 1 PCIE x 1
Mini-Card WLAN 802.11a/b/g/n 64

(3 in 1) SD/MMC/MMC+ 33
CardReader REALTEK RTS5138 32
USB 2.0 480Mbps
USB 2.0 x 1
Right Side: USB x 1 63

SM Bus 400KHz
Free fall sensor 40
USB 2.0 x 1
Bluetooth 73

LPC Bus 33MHz
TPM 36
USB 2.0 x 1
Biometric 78

73 CAMERA
USB2.0 x 1
Digital Mic Array
AZALIA 24MHz
Azalia CODEC OP AMP IDT 92HD81UA 30
MIC IN
HP OUT
1CH SPEAKER 60

SATA,USB
SATA 3Gbps
SPI

KBC NUVOTON NPCE781BA0DX 37
SPI
SM Bus
Thermal & Fan EMC2102 39,58
Capacity Board 78

Flash ROM 256kB 62
Touch PAD 68
Int. KB 68

USB,ESATA Multi-Port x1 63
ODD HDD 59
Flash ROM 4MB 62

CPU DC/DC ISL62883 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC TPS51218 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

LDO APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO RT9025 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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Title: Block Diagram
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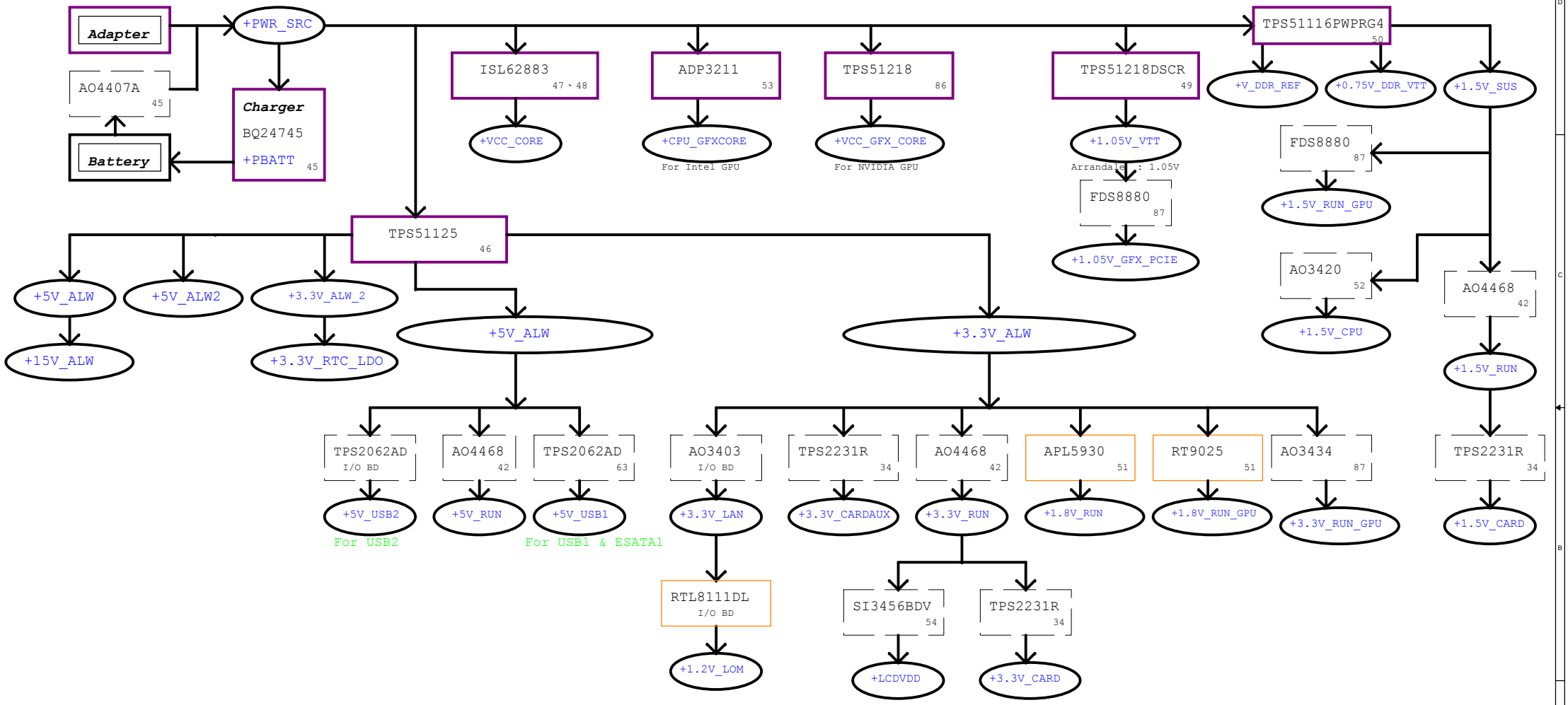

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Title: Power Block Diagram

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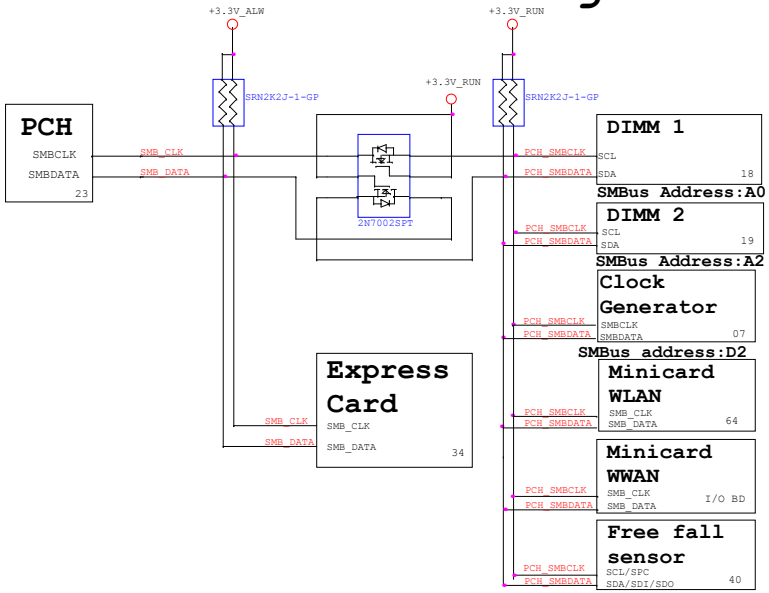
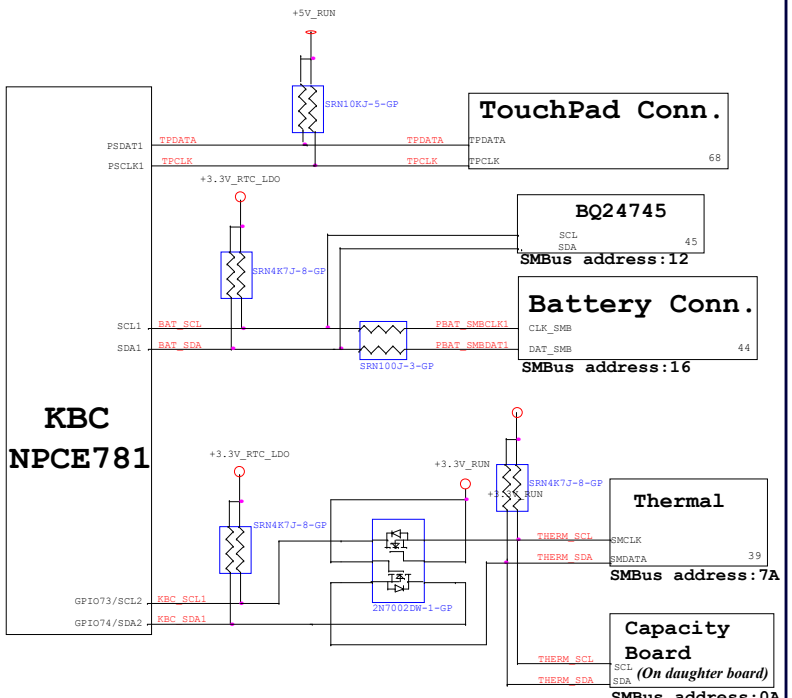
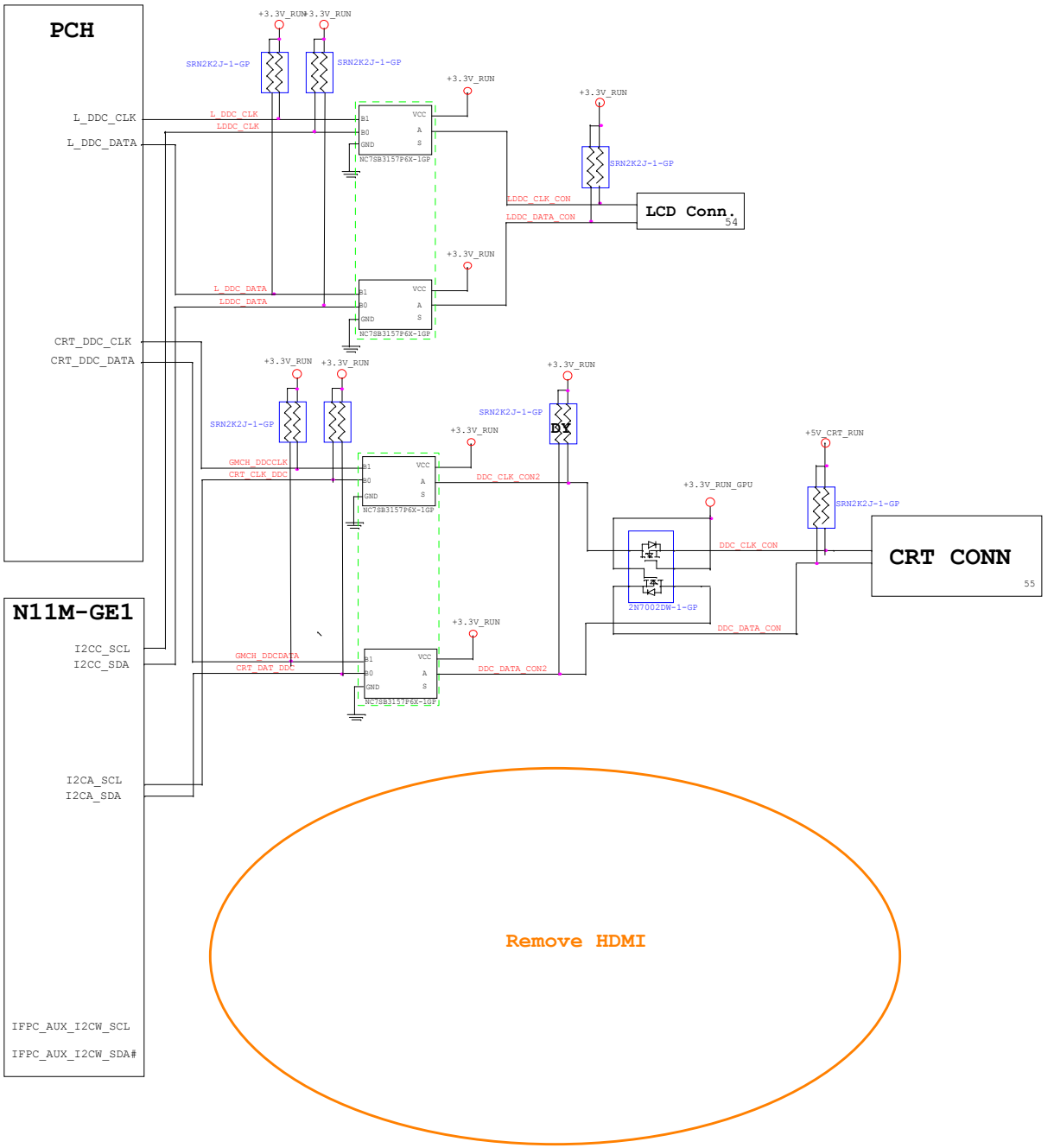
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Switchable Graphic SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
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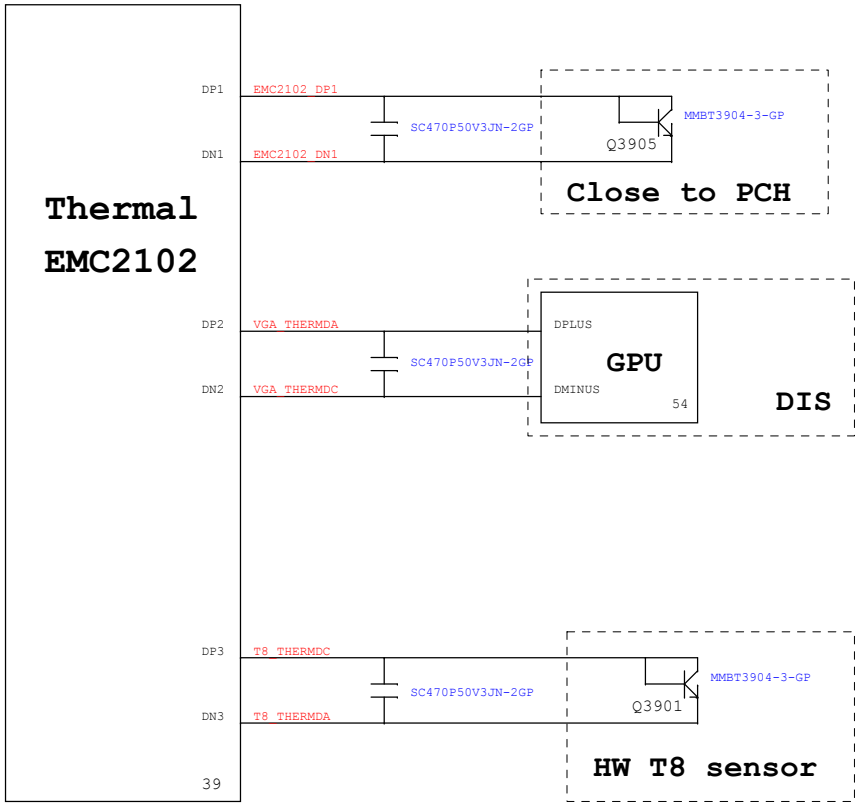
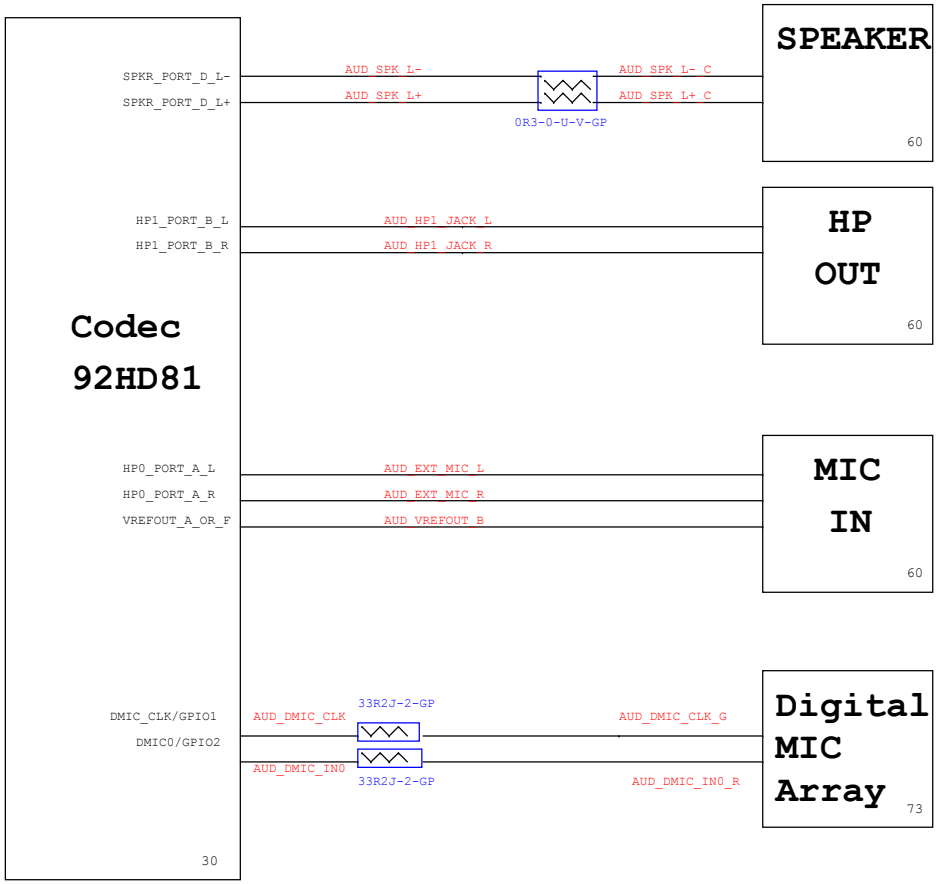
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
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PCH Strapping Calpella Schematic Checklist Rev1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:**Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:**Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)-:**Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:**CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)-:**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella Schematic Checklist Rev1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BlUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

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Title: Table of Content

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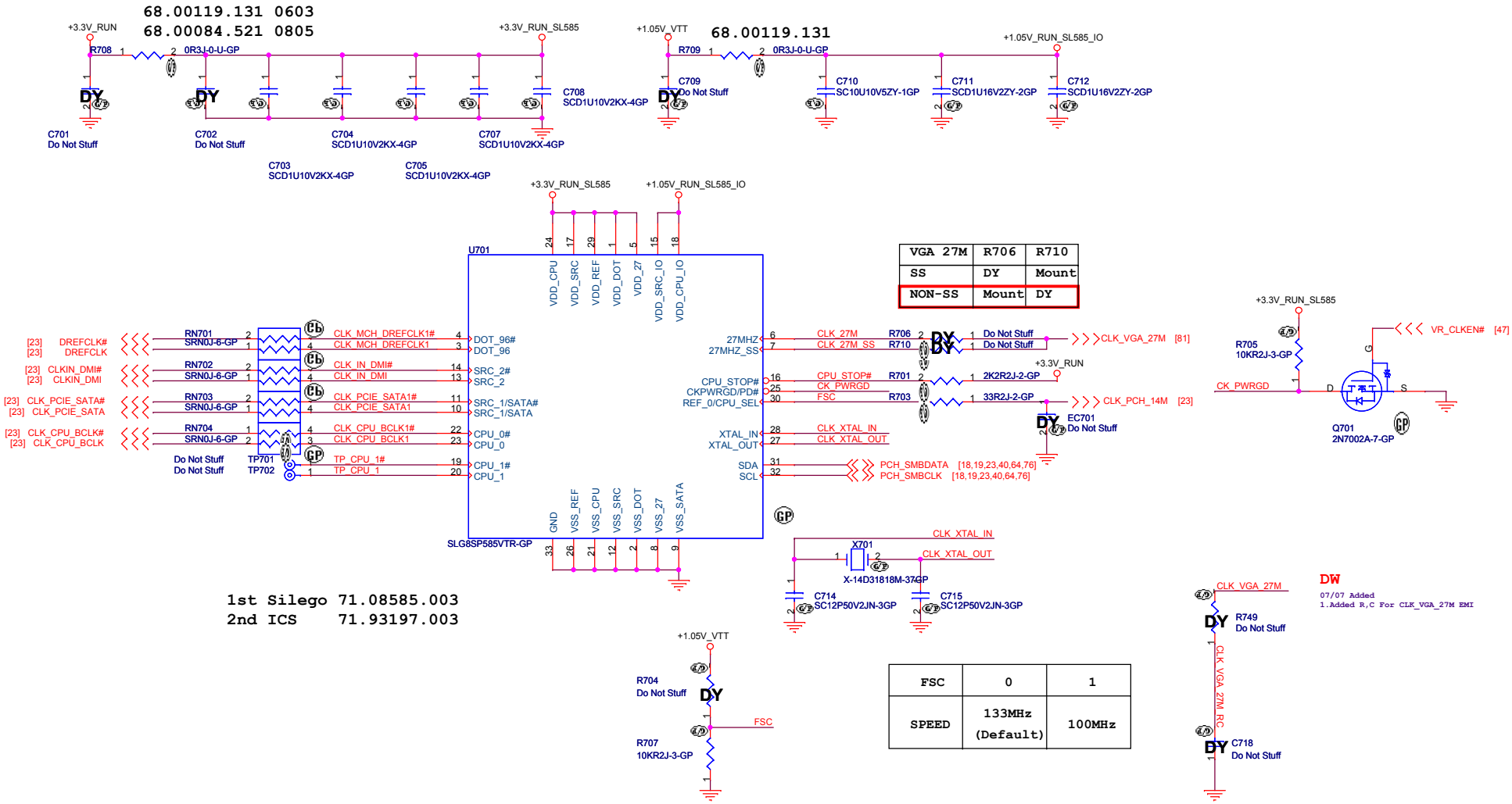

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Title: Clock Generator SLG8SP585

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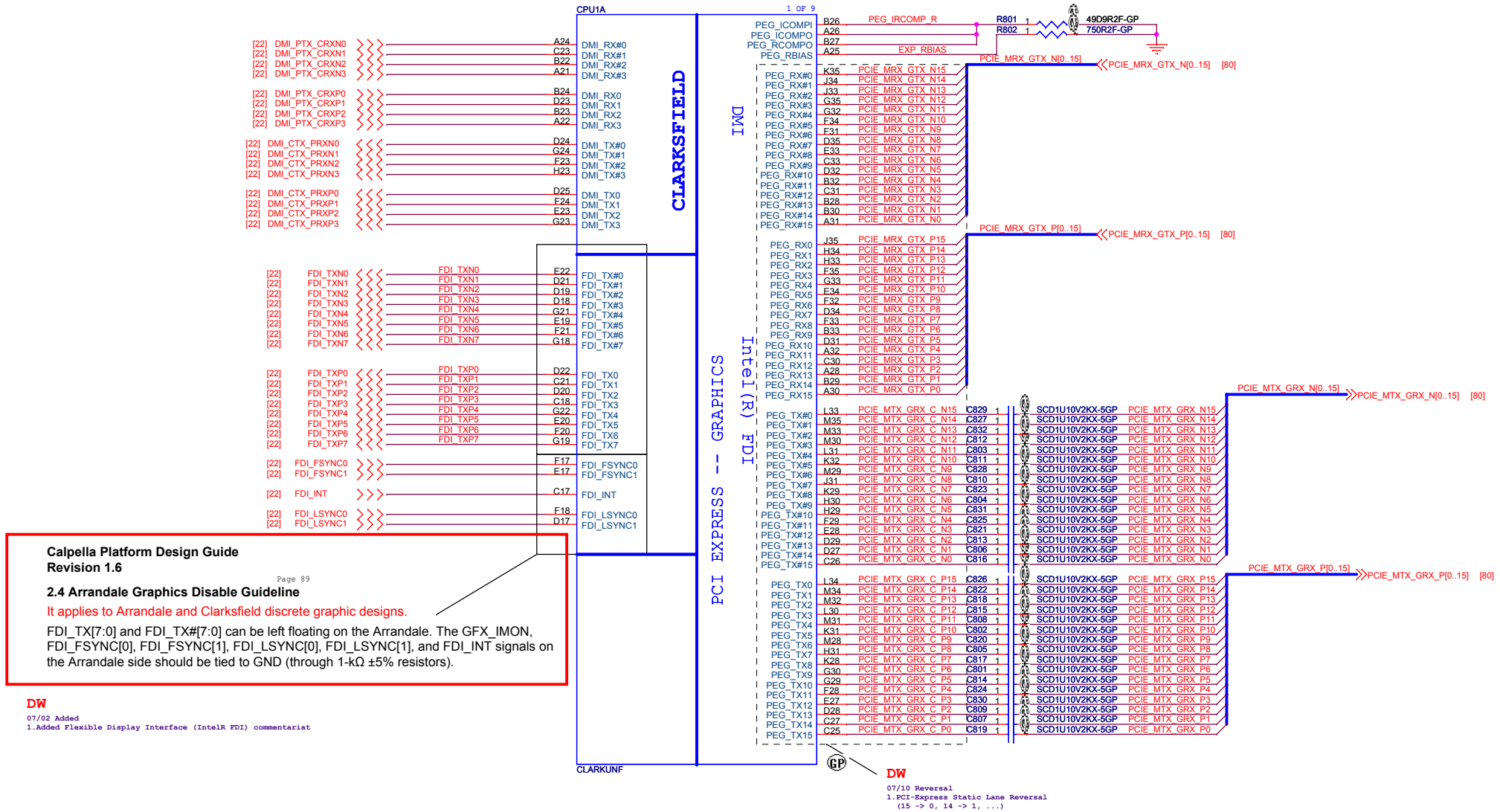

Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

DW

07/02 Added
1.Added Flexible Display Interface (IntelR FDI) commentariat

DW

07/10 Reversal
1.PCI-Express Static Lane Reversal
(15 -> 0, 14 -> 1, ...)

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Title: **CPU (PCIE/DMI/FDI)**

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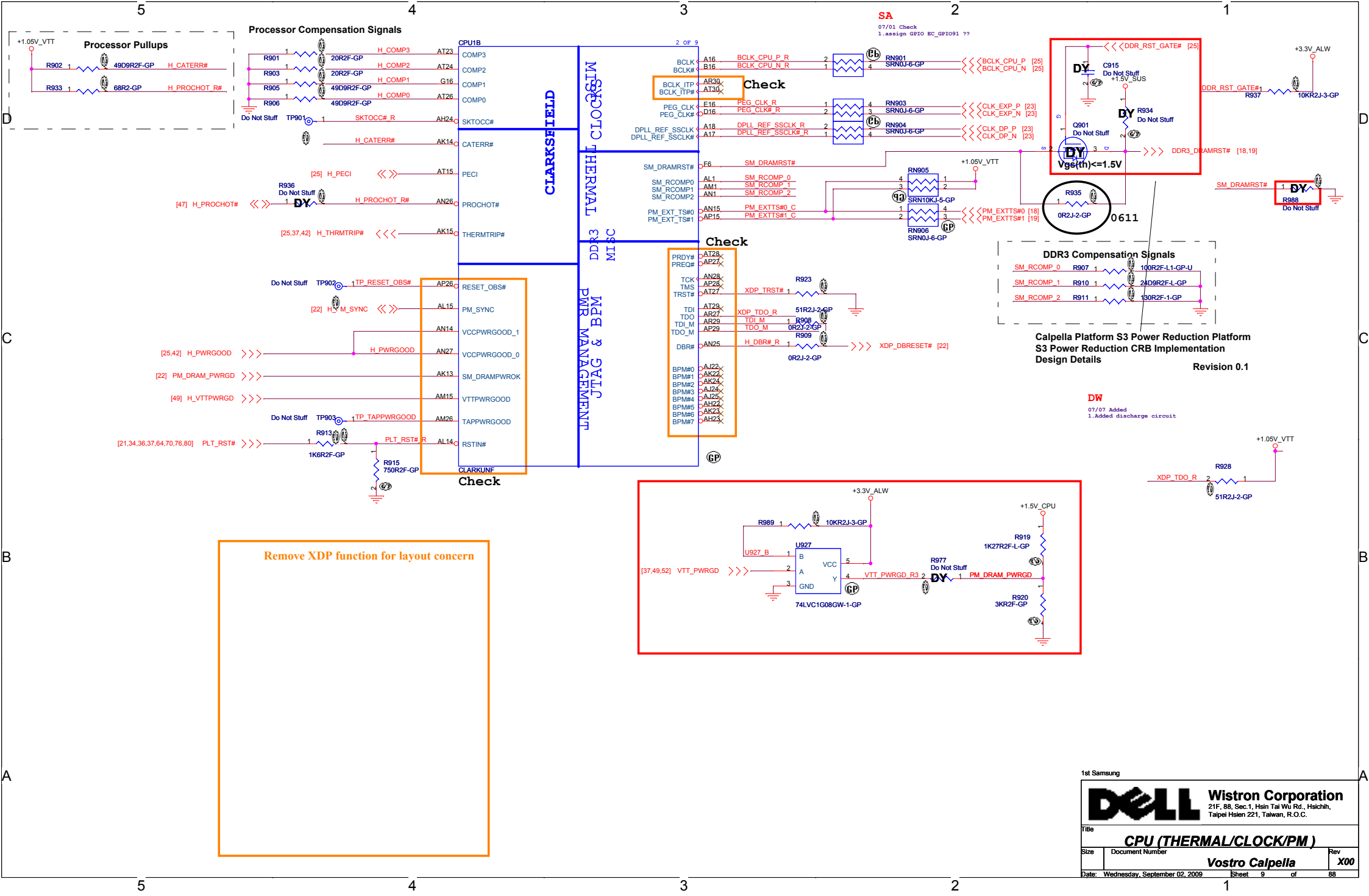
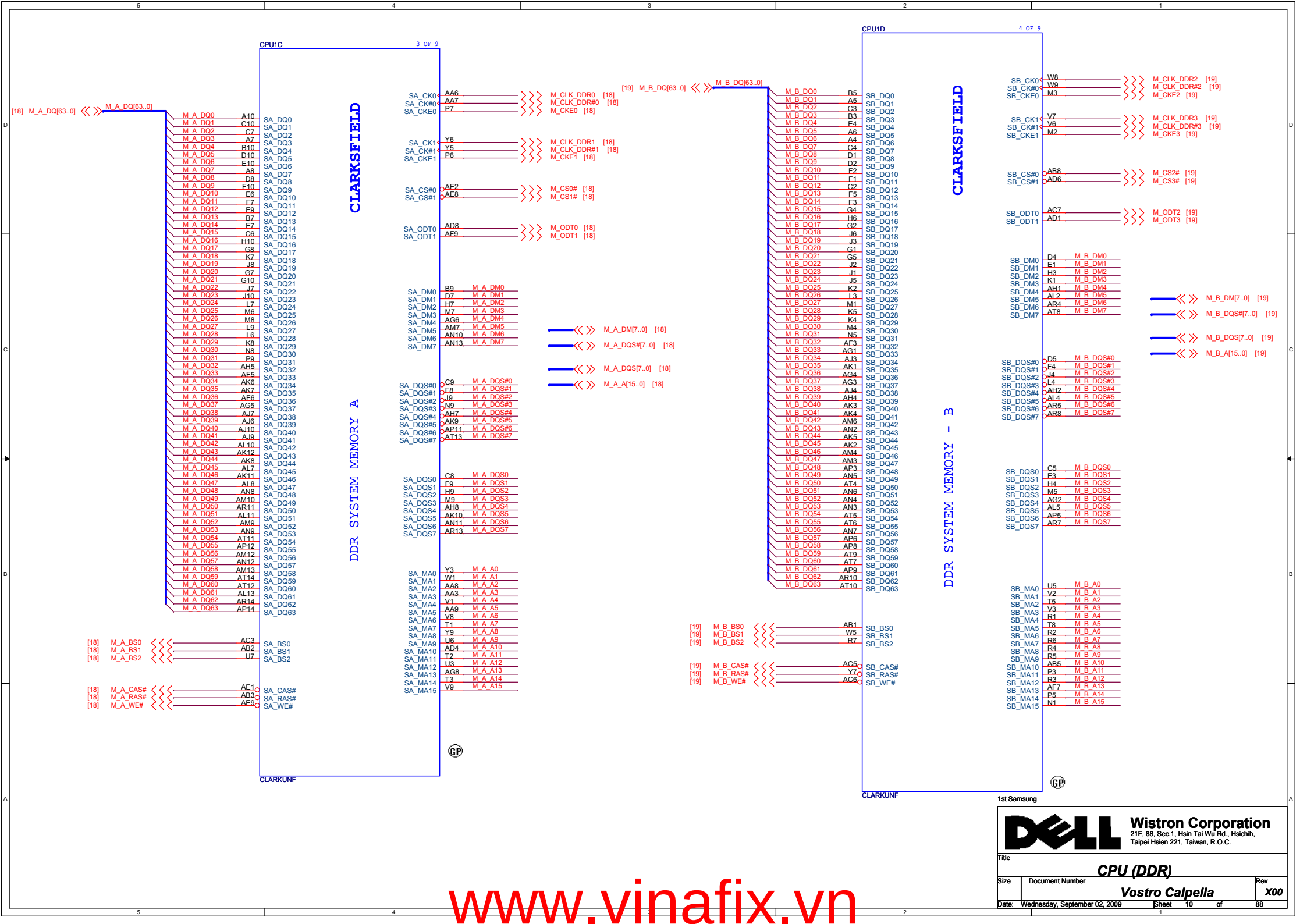
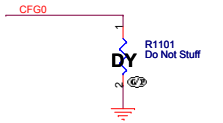
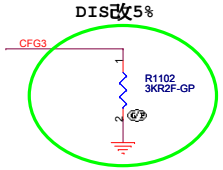






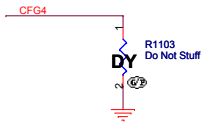
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



DW

07/10 Reversal
1.PCI-Express Static Lane Reversal

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

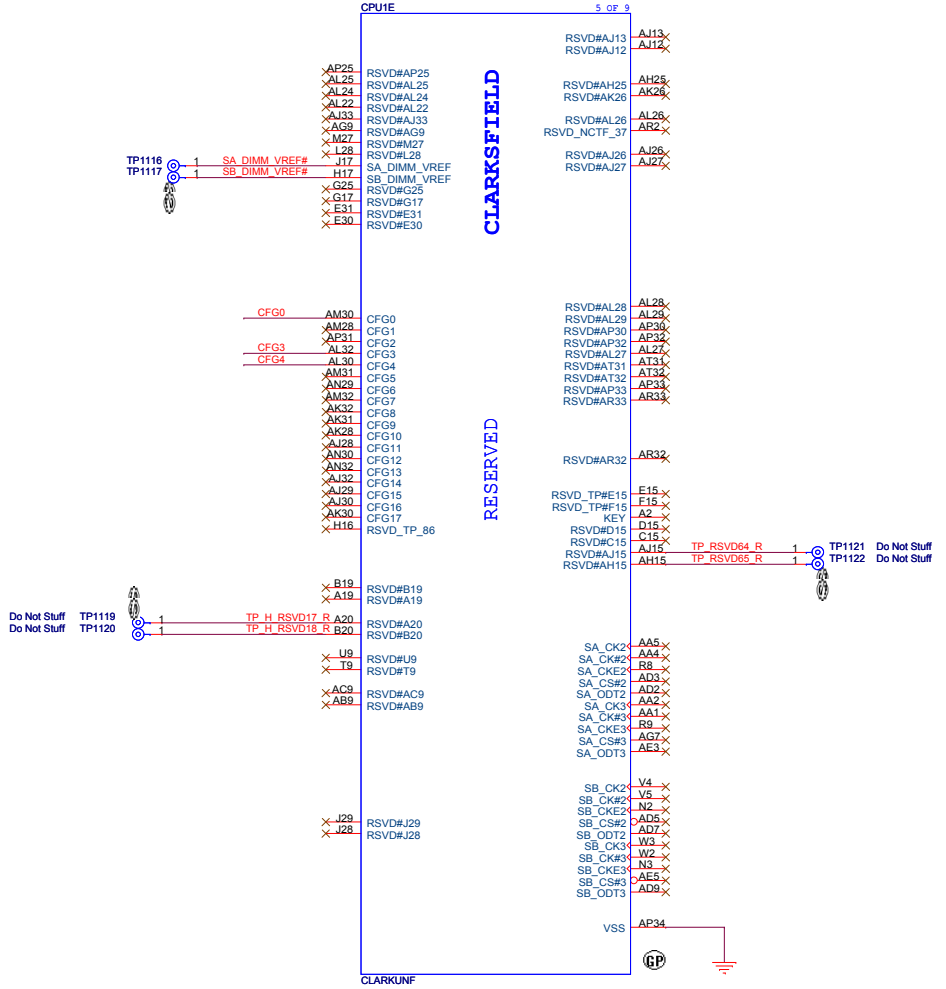
Page 482,486

DW

07/02 Added
1.Added display Switchable strap commentariat

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

DW30 Only support Arrandale, CFG7 no need pull down



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Title: CPU (RESERVED)

Size	Document Number	Rev
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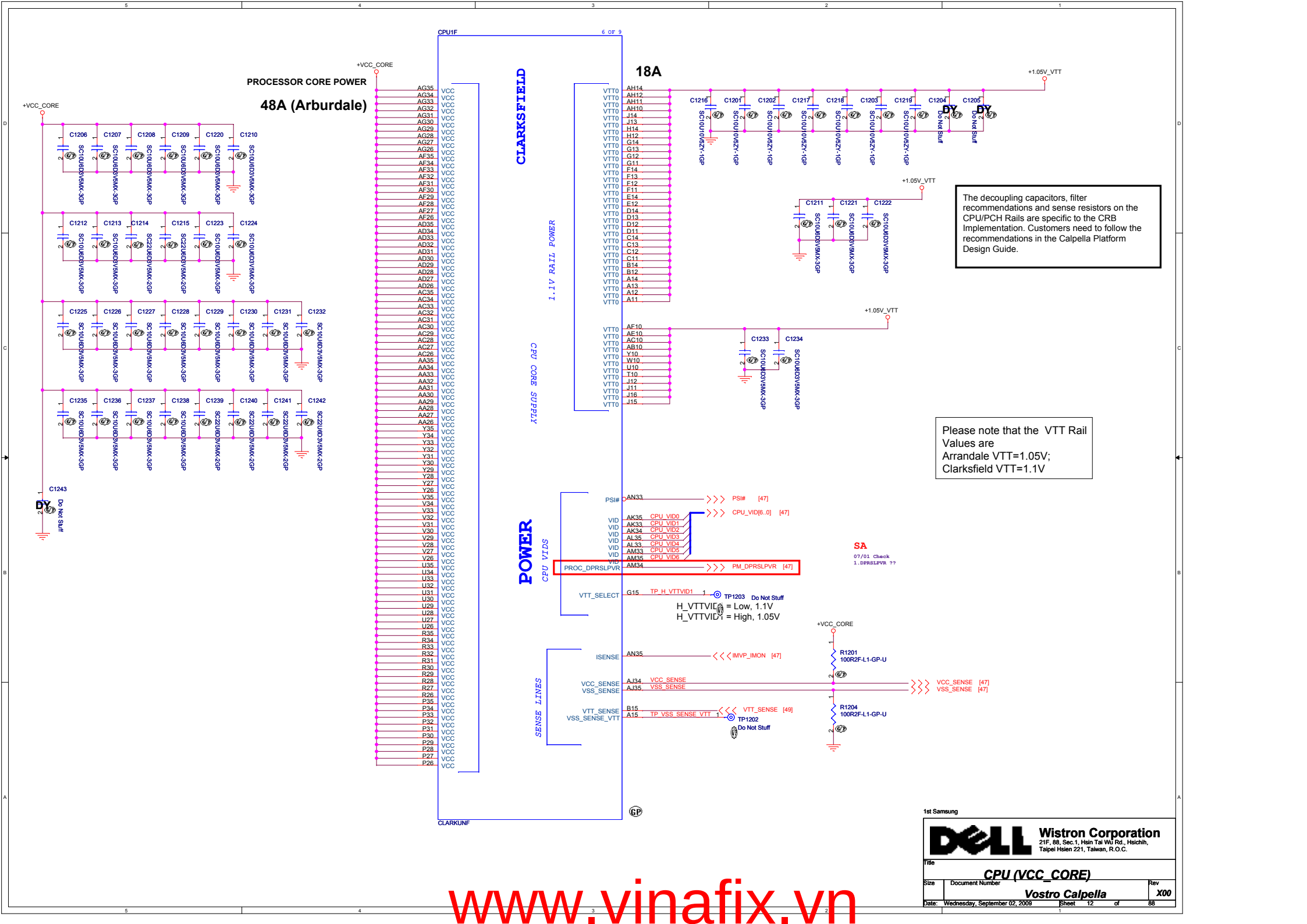

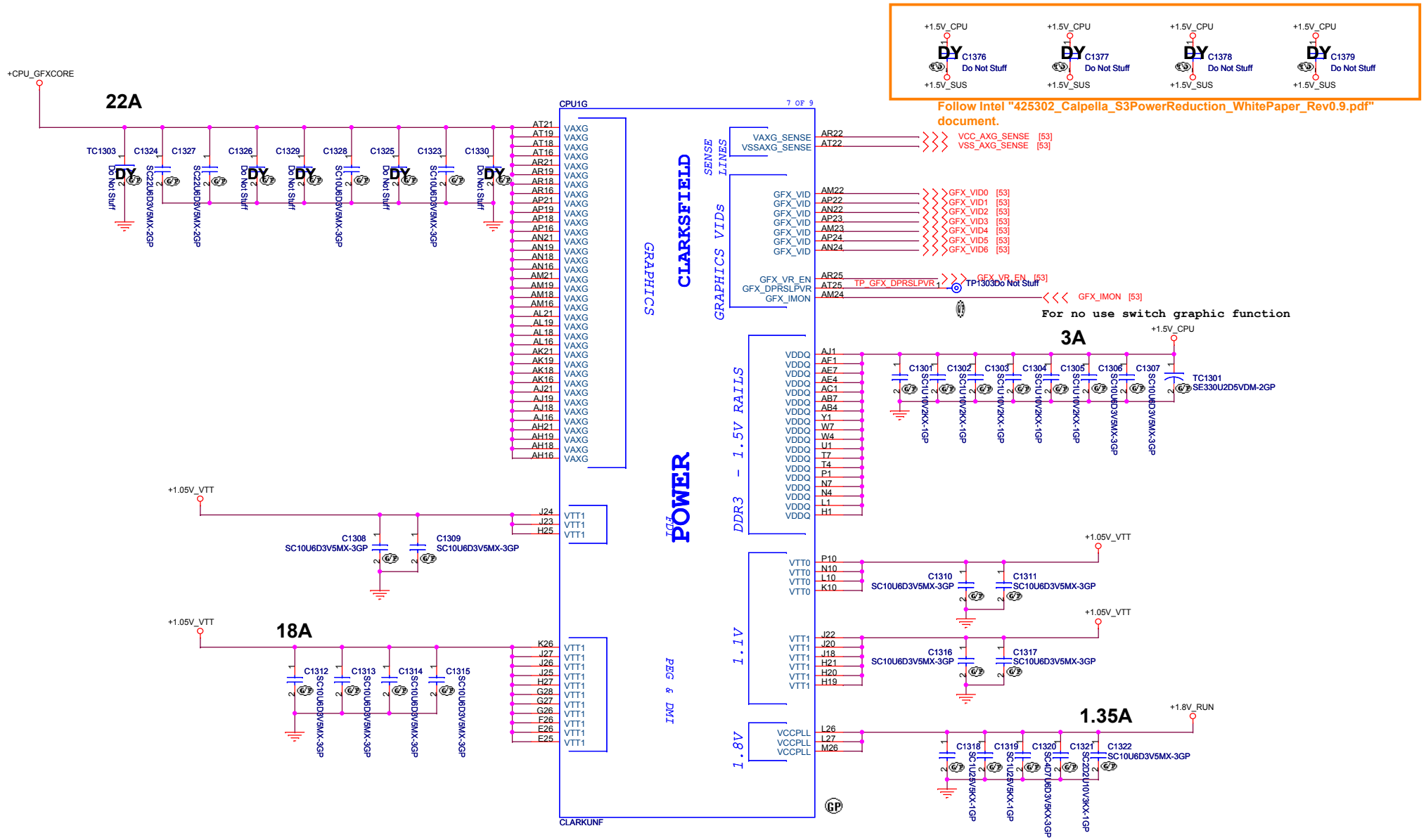

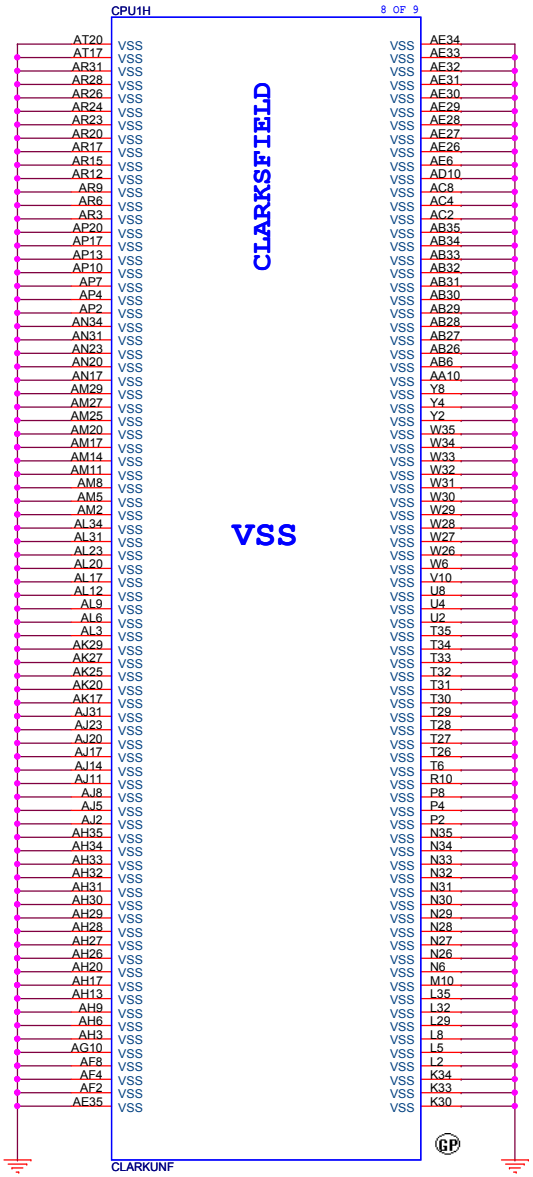

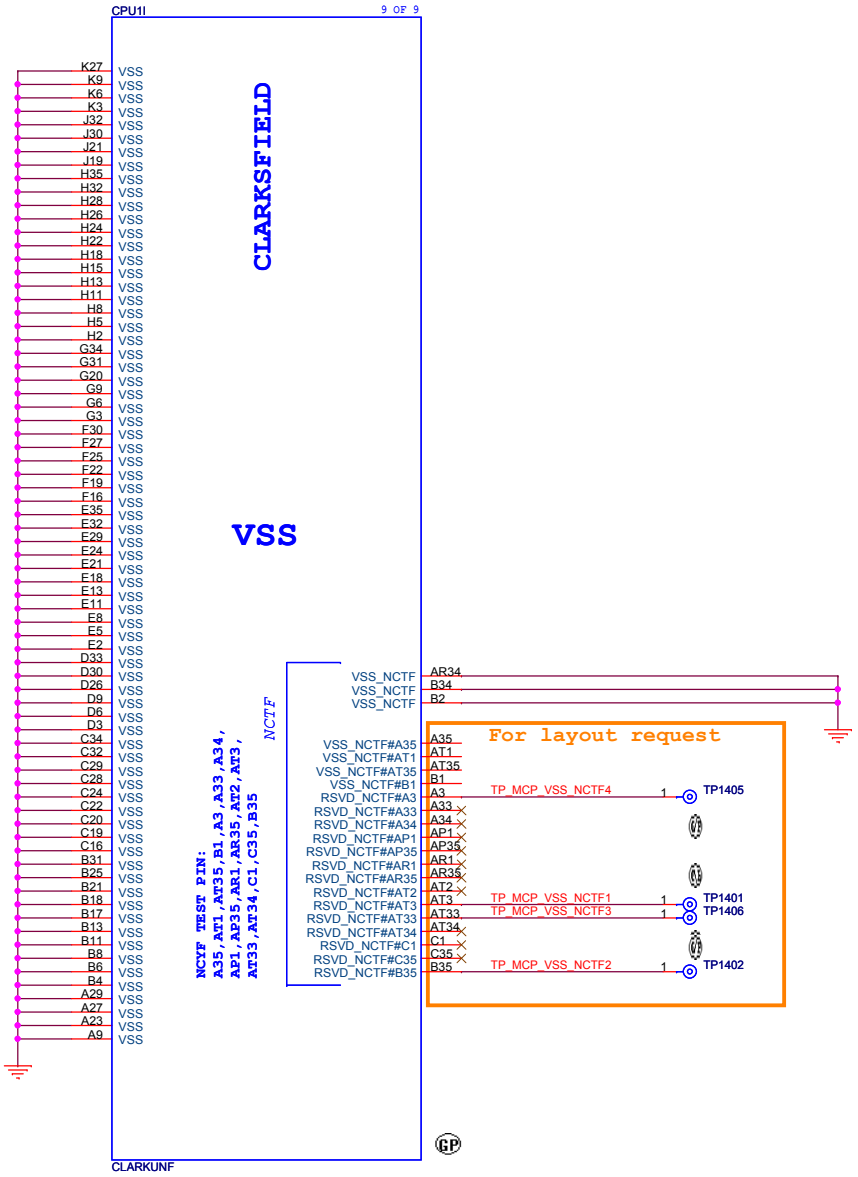

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SSID = MEMORY

DM1

DDR3-204P-47-GP

62.10017.P31

Height 5.2mm

[10] M_A_DQS#[7..0]
[10] M_A_DQ[63..0]
[10] M_A_DM[7..0]
[10] M_A_DQS[7..0]
[10] M_A_A[15..0]

[10] M_A_BS2
[10] M_A_BS0
[10] M_A_BS1

M_A_RAS# [10]
M_A_WE# [10]
M_A_CAS# [10]
M_CS0# [10]
M_CS1# [10]
M_CKE0 [10]
M_CKE1 [10]
M_CLK_DDR0 [10]
M_CLK_DDR#0 [10]
M_CLK_DDR1 [10]
M_CLK_DDR#1 [10]

PCH_SMBDATA [7,19,23,40,64,76]
PCH_SMBCLK [7,19,23,40,64,76]
PM_EXTTS#0 [9]

SMBUS address:A0

R1802 10KR2J-3-GP
R1801 10KR2J-3-GP

DW
07/02 Reserve
1.Added SA0_DM1 pull-up resistor
07/07
2.Reserve pull-hi,lo resistor

+3.3V_RUN
+1.5V_SUS

C1806 SCD1U16V2KX-3GP
C1807 Do Not Stuff

Layout Note:
Place near DM1

+1.5V_SUS

C1803 SC10U6D3V5MX-3GP
C1804 SC10U6D3V5MX-3GP
C1812 SC10U6D3V5MX-3GP
C1802 SC10U6D3V5MX-3GP
C1811 SC10U6D3V5MX-3GP
C1816 SC10U6D3V5MX-3GP
TC1803 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

Layout Note:
Put between two SO-DIMM

+0.75V_DDR_VTT

C1814 SC1U10V2KX-1GP
C1813 SC1U10V2KX-1GP
C1815 SC1U10V2KX-1GP
C1801 SC1U10V2KX-1GP
C1823 SC10U6D3V5MX-3GP

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS

C1872 SCD1U16V2KX-4GP
C1873 SCD1U16V2KX-4GP
C1874 SCD1U16V2KX-4GP
C1875 SCD1U16V2KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1

C1821 Do Not Stuff
C1819 Do Not Stuff
C1820 Do Not Stuff
C1818 Do Not Stuff

+V_DDR_REF

[10] M_ODT0
[10] M_ODT1

+0.75V_DDR_VTT
[9,19] DDR3_DRAMRST#

C1810 SCD1U16V2KX-3GP
C1817 SCD1U16V2KX-3GP
C1809 Do Not Stuff DY

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Title: DDRIII-SODIMM SLOT1
Size: Custom
Document Number: Vostro Calpella
Rev: SA
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SSID = MEMORY

Change CONN
2009/06/01

[10] M_B_DQS#[7..0]
[10] M_B_DQ[63..0]
[10] M_B_DM[7..0]
[10] M_B_DQS[7..0]
[10] M_B_A[15..0]

DM2

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15
[10] M_B_BS2 79 A16/BA2
[10] M_B_BS0 109 BA0
[10] M_B_BS1 108 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
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M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
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M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 10 DQS0#
M_B_DQS#1 27 DQS1#
M_B_DQS#2 45 DQS2#
M_B_DQS#3 62 DQS3#
M_B_DQS#4 135 DQS4#
M_B_DQS#5 152 DQS5#
M_B_DQS#6 169 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

[10] M_ODT2 116 ODT0
[10] M_ODT3 120 ODT1

126 VREF_CA
1 VREF_DQ

[9,18] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP1
NP2 NP2

RAS# 110 M_B_RAS# [10]
WE# 113 M_B_WE# [10]
CAS# 115 M_B_CAS# [10]

CS0# 114 M_CS2# [10]
CS1# 121 M_CS3# [10]

CKE0 73 M_CKE2 [10]
CKE1 74 M_CKE3 [10]

CK0 101 M_CLK_DDR2 M_CLK_DDR2 [10]
CK0# 103 M_CLK_DDR#2 M_CLK_DDR#2 [10]
CK1 102 M_CLK_DDR3 M_CLK_DDR3 [10]
CK1# 104 M_CLK_DDR#3 M_CLK_DDR#3 [10]

DM0 11 M_B_DM0
DM1 28 M_B_DM1
DM2 46 M_B_DM2
DM3 63 M_B_DM3
DM4 136 M_B_DM4
DM5 153 M_B_DM5
DM6 170 M_B_DM6
DM7 187 M_B_DM7

SDA 200 PCH_SMBDATA PCH_SMBDATA [7,18,23,40,64,76]
SCL 202 PCH_SMBCLK PCH_SMBCLK [7,18,23,40,64,76]

EVENT# 198 PM_EXTTS#1 [9]

VDDSPD 199

SA0 197 SA0_DM2
SA1 201 SA1_DM2

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2,3,8,9,13,14,19,20,25,26,31,32,37,38,43,44,48,49,54,55,60,61,65,66,71,72,127,128,133,134,138,139,144,145,150,151,155,156,161,162,167,168,172,173,178,179,184,185,189,190,195,196,205,206

Height 9.2mm

DDR3-204P-55-GP
62.10017.Q31

+1.5V_SUS
+0.75V_DDR_VTT
+V_DDR_REF

Layout Note:
Place near DM2

+1.5V_SUS
C1919 SC10U6D3V5MX-3GP
C1905 SC10U6D3V5MX-3GP
C1911 SC10U6D3V5MX-3GP
C1916 SC10U6D3V5MX-3GP
C1913 SC10U6D3V5MX-3GP
C1920 SC10U6D3V5MX-3GP
TC1903 ST330U2D5YBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT
C1908 SC1U10V2KX-1GP
C1917 SC1U10V2KX-1GP
C1918 SC1U10V2KX-1GP
C1909 SC1U10V2KX-1GP

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS
C1976 SC1U10V2KX-4GP
C1977 SC1U10V2KX-4GP
C1978 SC1U10V2KX-4GP
C1979 SCD1U10V6KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

+V_DDR_REF
C1907 SCD1U16V2KX-3GP
C1910 SCD1U16V2KX-3GP
C1914 Do Not Stuff

+0.75V_DDR_VTT

+3.3V_RUN
R1903 Do Not Stuff
R1904 10KR2J-3-GP
EC1901 Do Not Stuff
SA1_DM2
SA0_DM2
R1901 10KR2J-3-GP
R1902 Do Not Stuff

SMBUS address:A2

+3.3V_RUN
C1906 SCD1U16V2KX-3GP
C1921 Do Not Stuff

DW
07/02 Reserve
1.Added SA1_DM2 pull-down resistor
07/07
2.Reserve pull-hi,lo resistor

put near connector
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C1901 Do Not Stuff
C1904 Do Not Stuff
C1902 Do Not Stuff
C1903 Do Not Stuff

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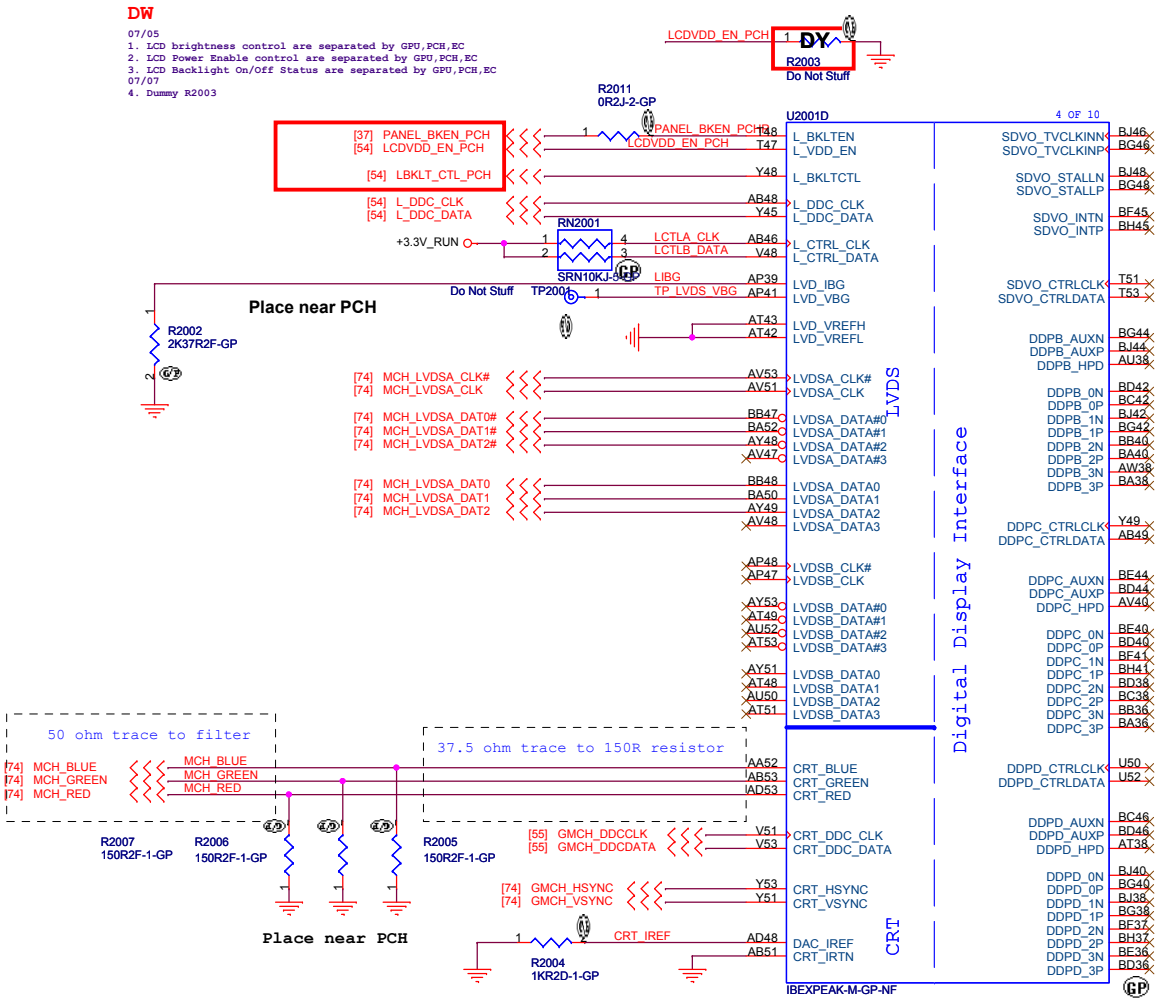
Title: DDRIII-SODIMM SLOT2
Size: Custom
Document Number: Vostro Calpella
Rev: SA
Date: Wednesday, September 02, 2009
Sheet 19 of 88



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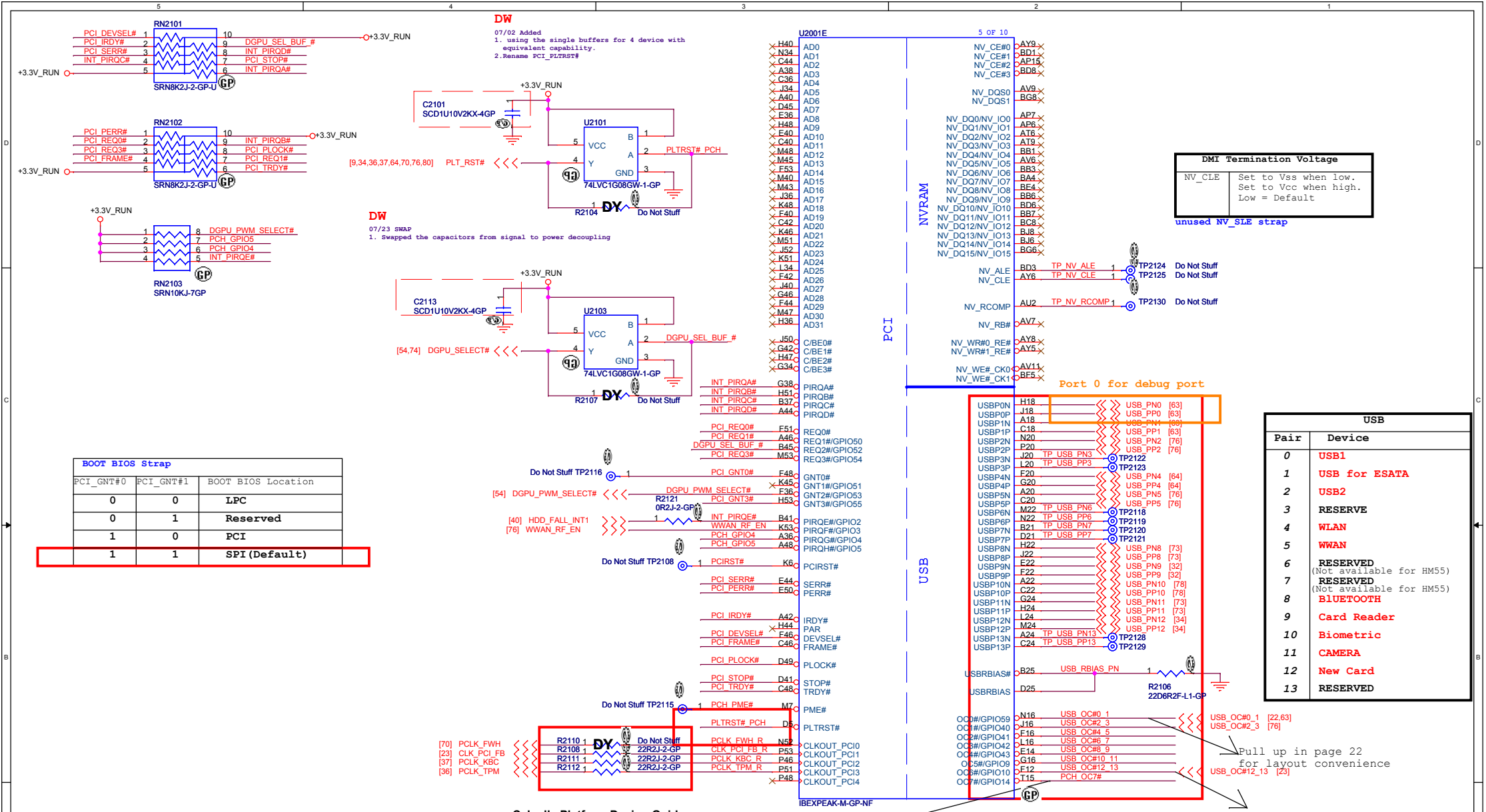
Title		
PCH (LVDS/CRT/DDI)		
Size	Document Number	Rev
	Vostro Calpella	X00
Date: Wednesday, September 02, 2009	Sheet 20 of 88	



Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

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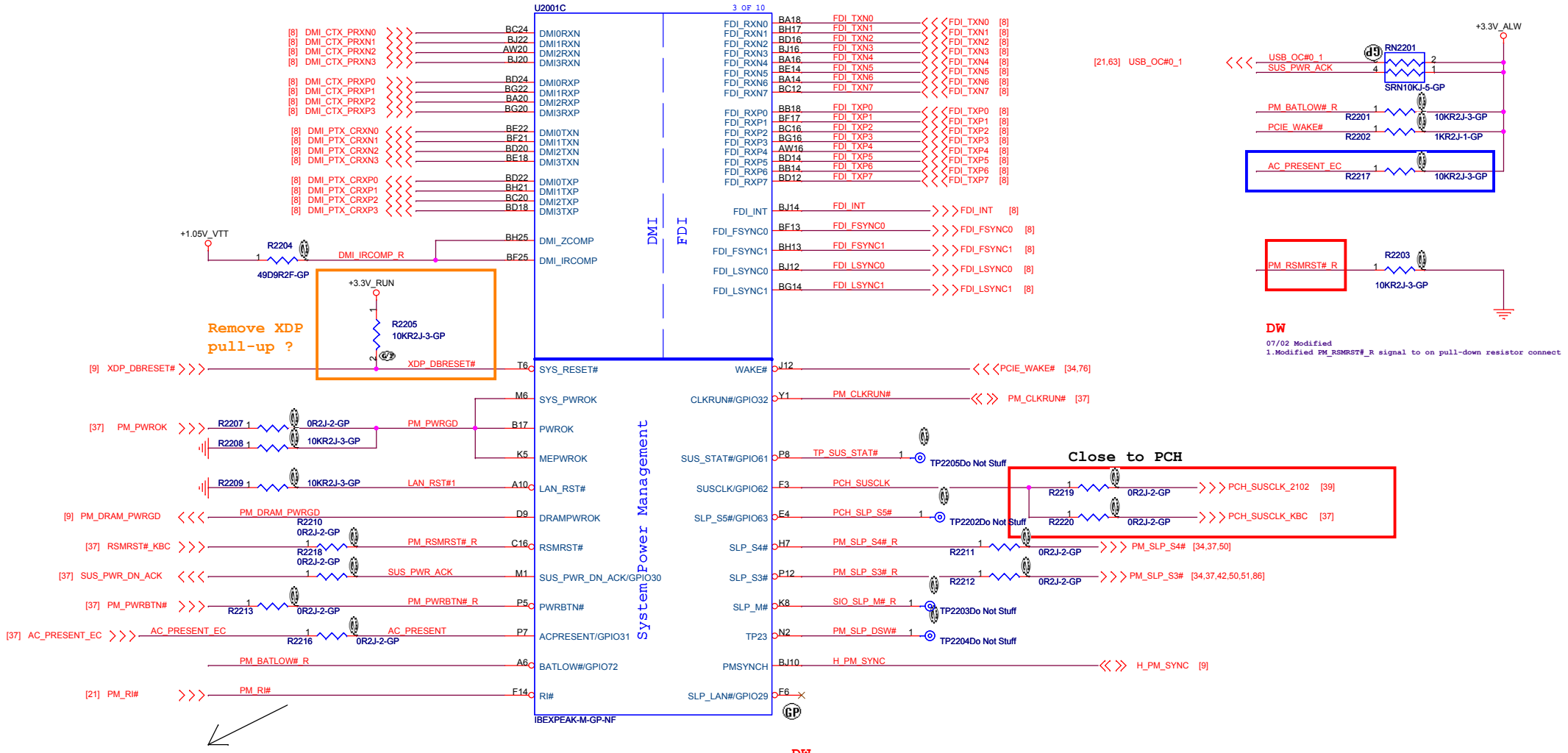
Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Vostro Calpella Rev: X00
Date: Wednesday, September 02, 2009 Sheet 21 of 88



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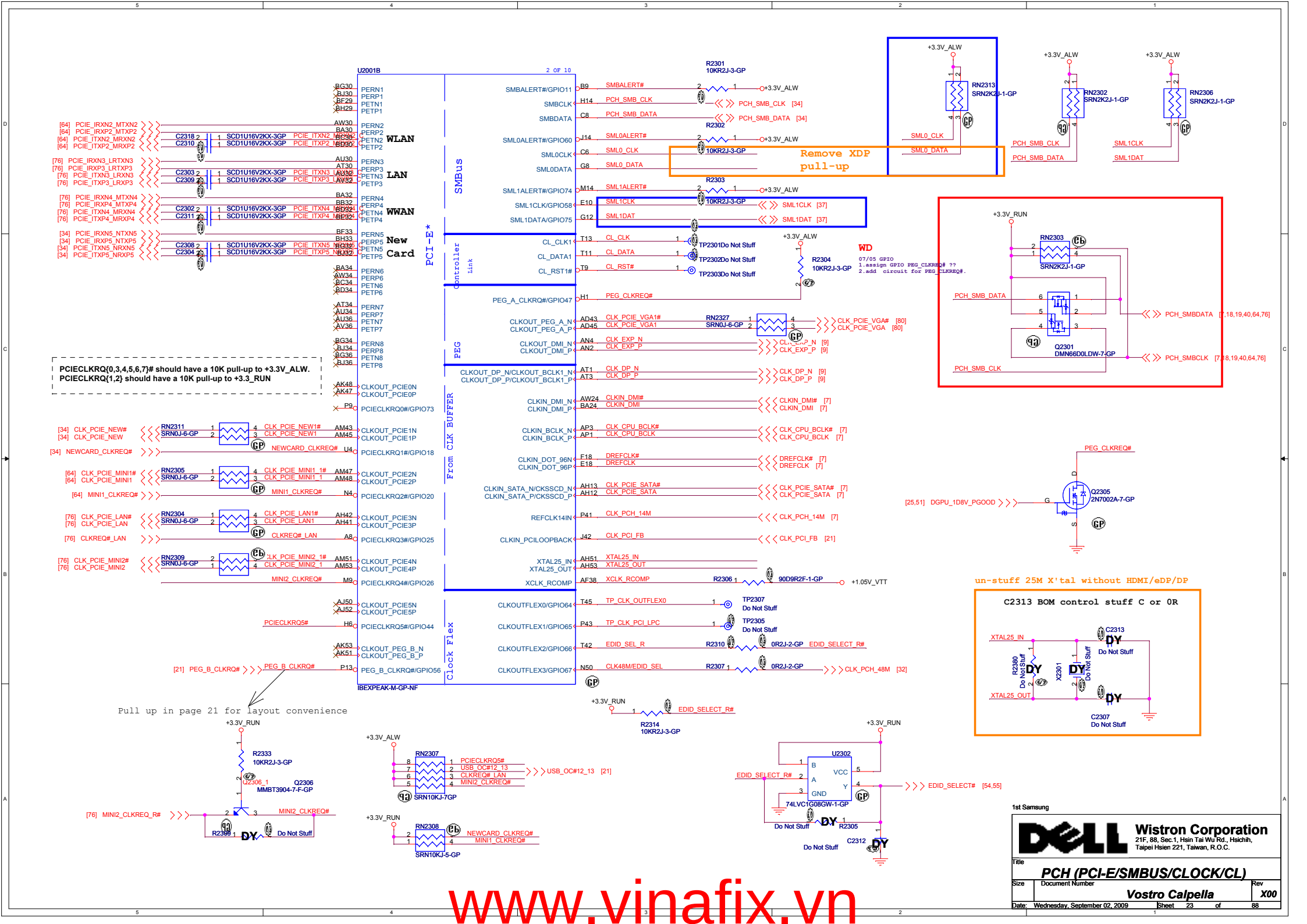
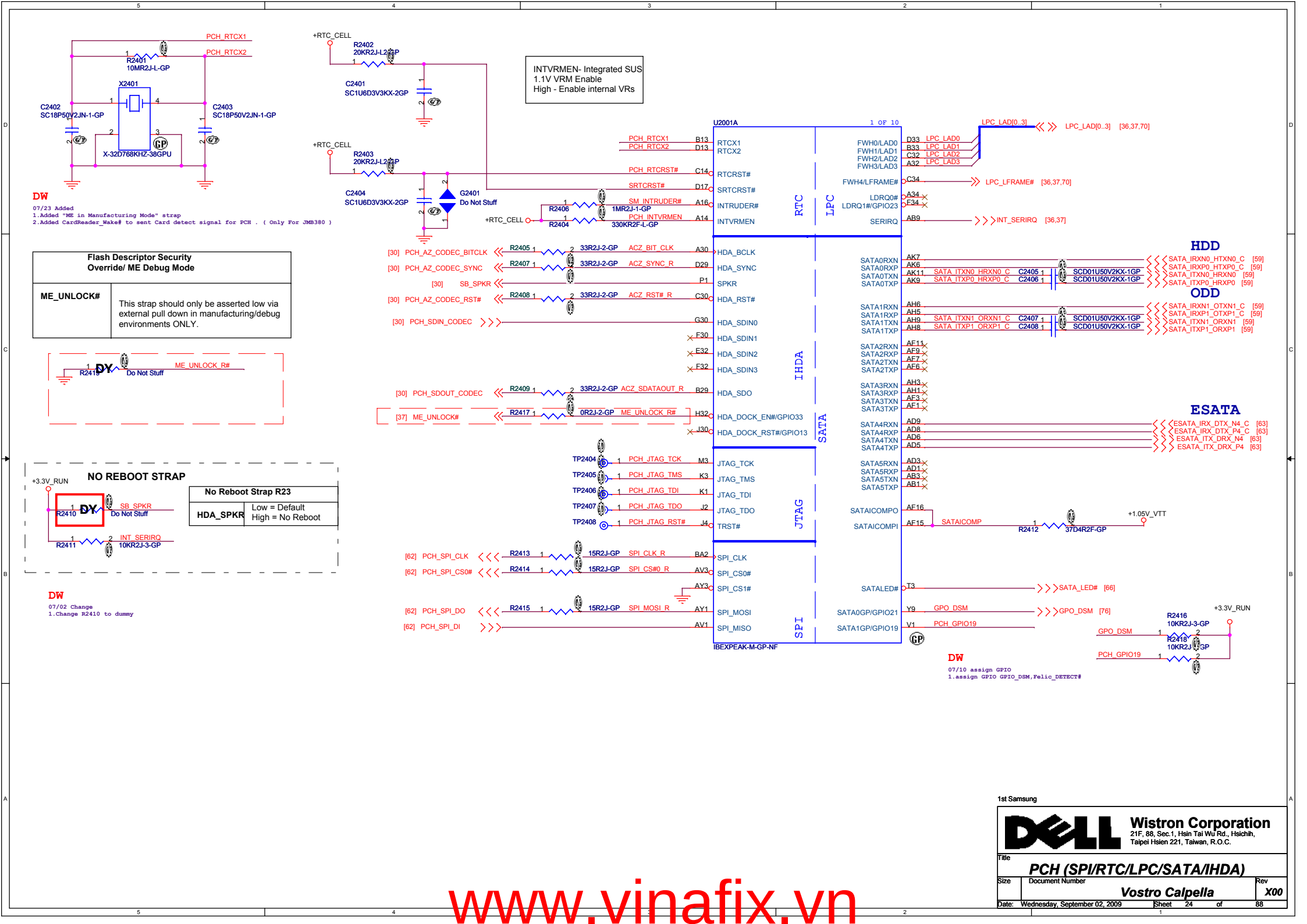
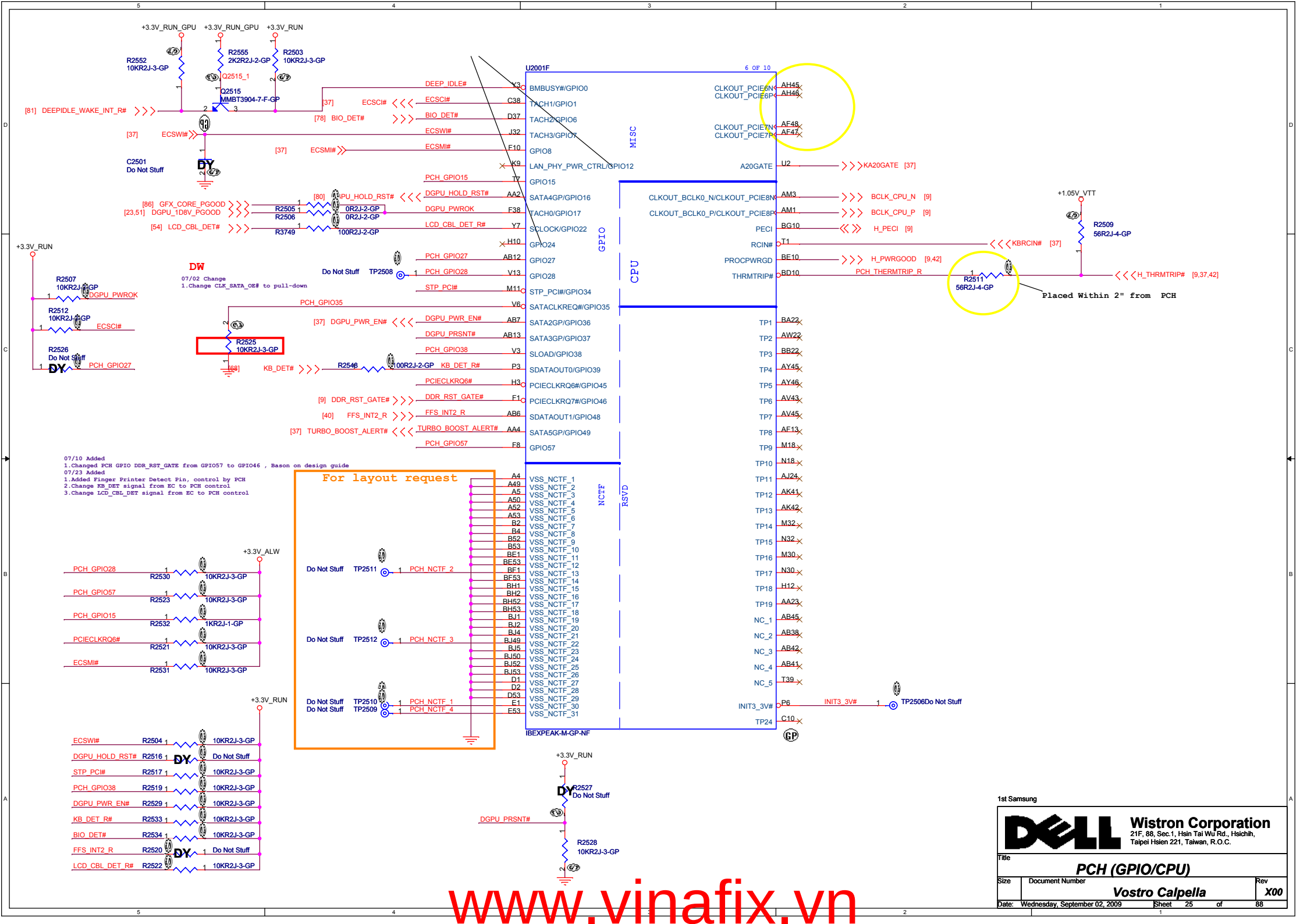
Title: PCH (DM I/FDI/PM)

Size | Document Number: Vostro Calpella | Rev: X00

Date: Wednesday, September 02, 2009 | Sheet 22 of 88







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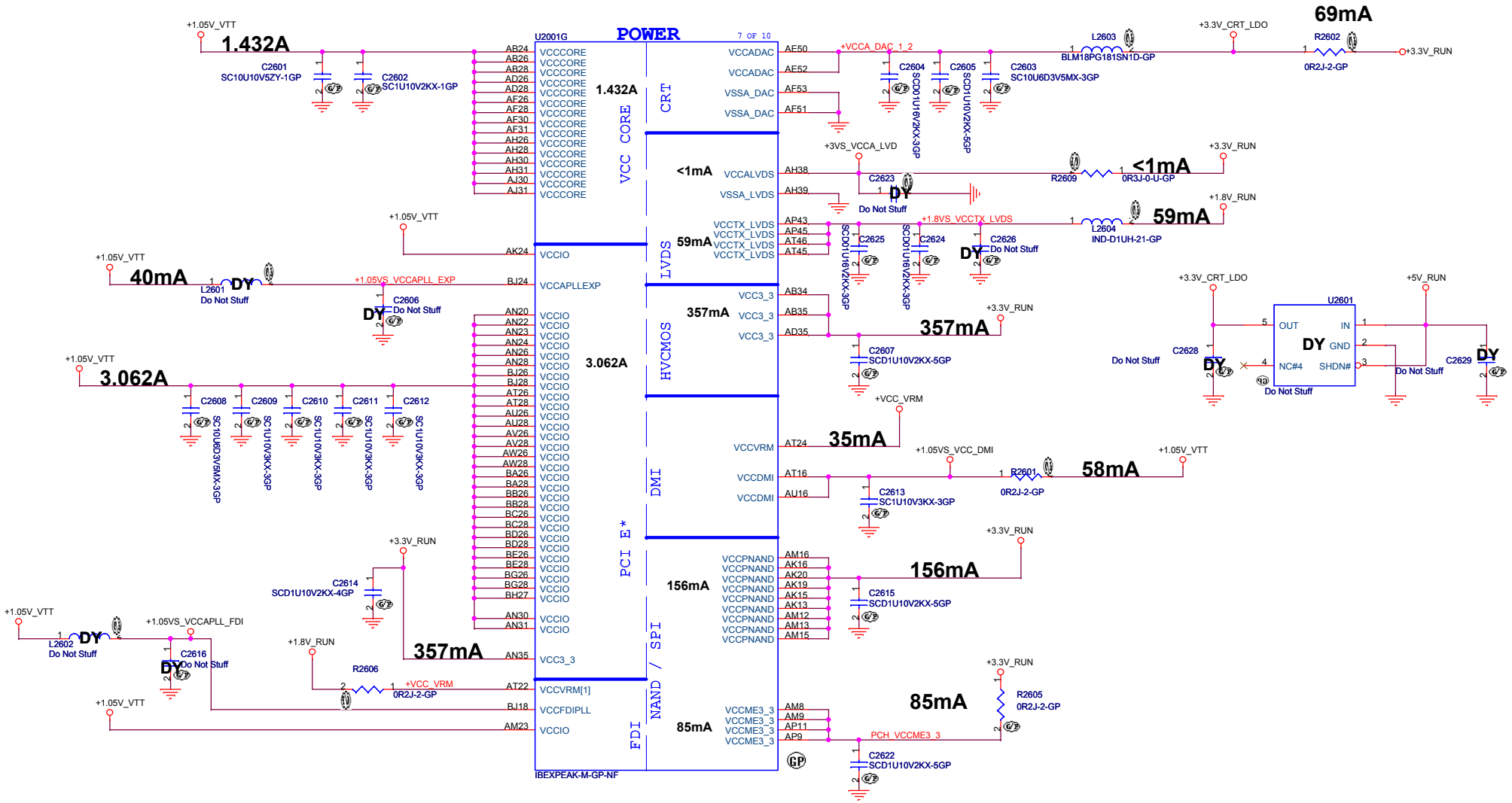
Title: PCH (GPIO/CPU)

Size	Document Number	Rev
	Vostro Calpella	X00

Date: Wednesday, September 02, 2009 Sheet 25 of 88



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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size	Document Number	Rev
	Vostro Calpella	X00

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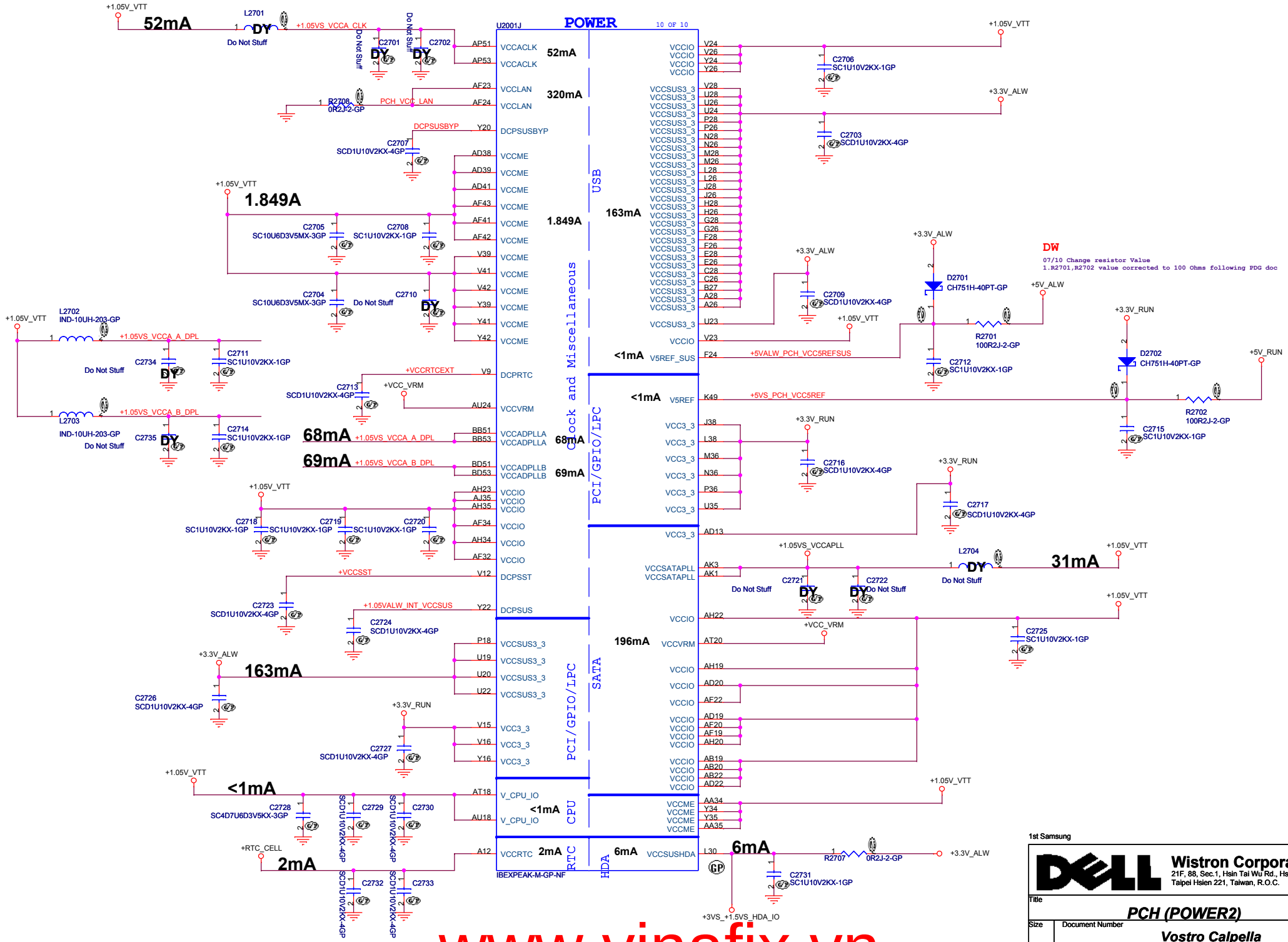

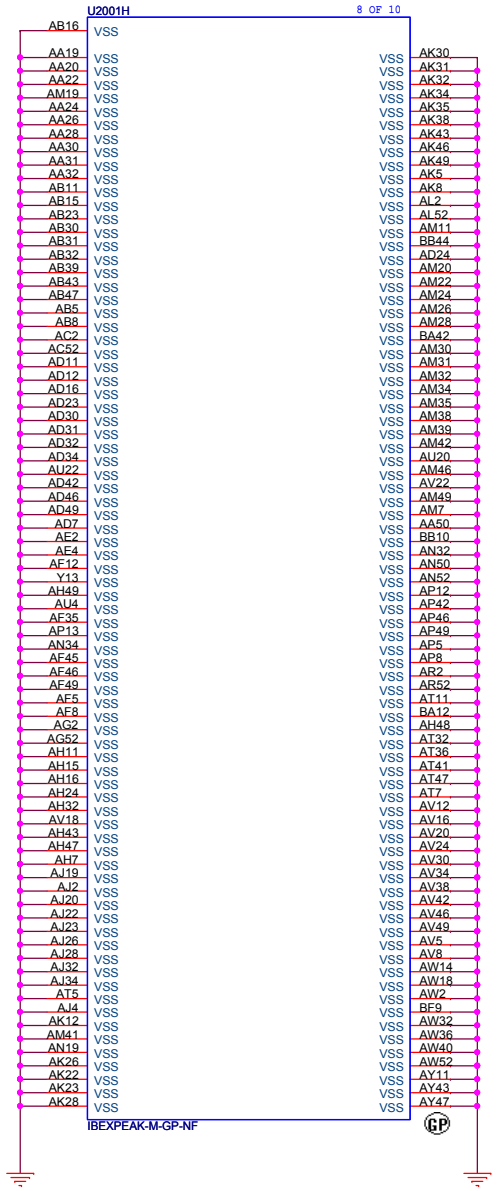

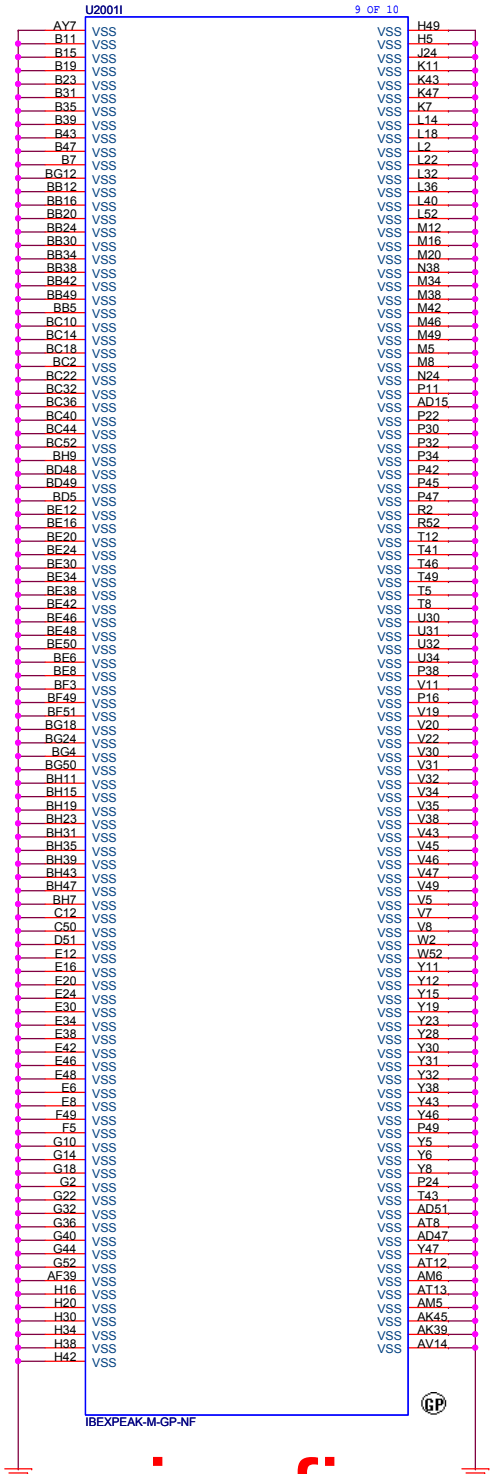

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Title: **PCH (VSS)**

Size	Document Number	Rev
	Vostro Calpella	X00

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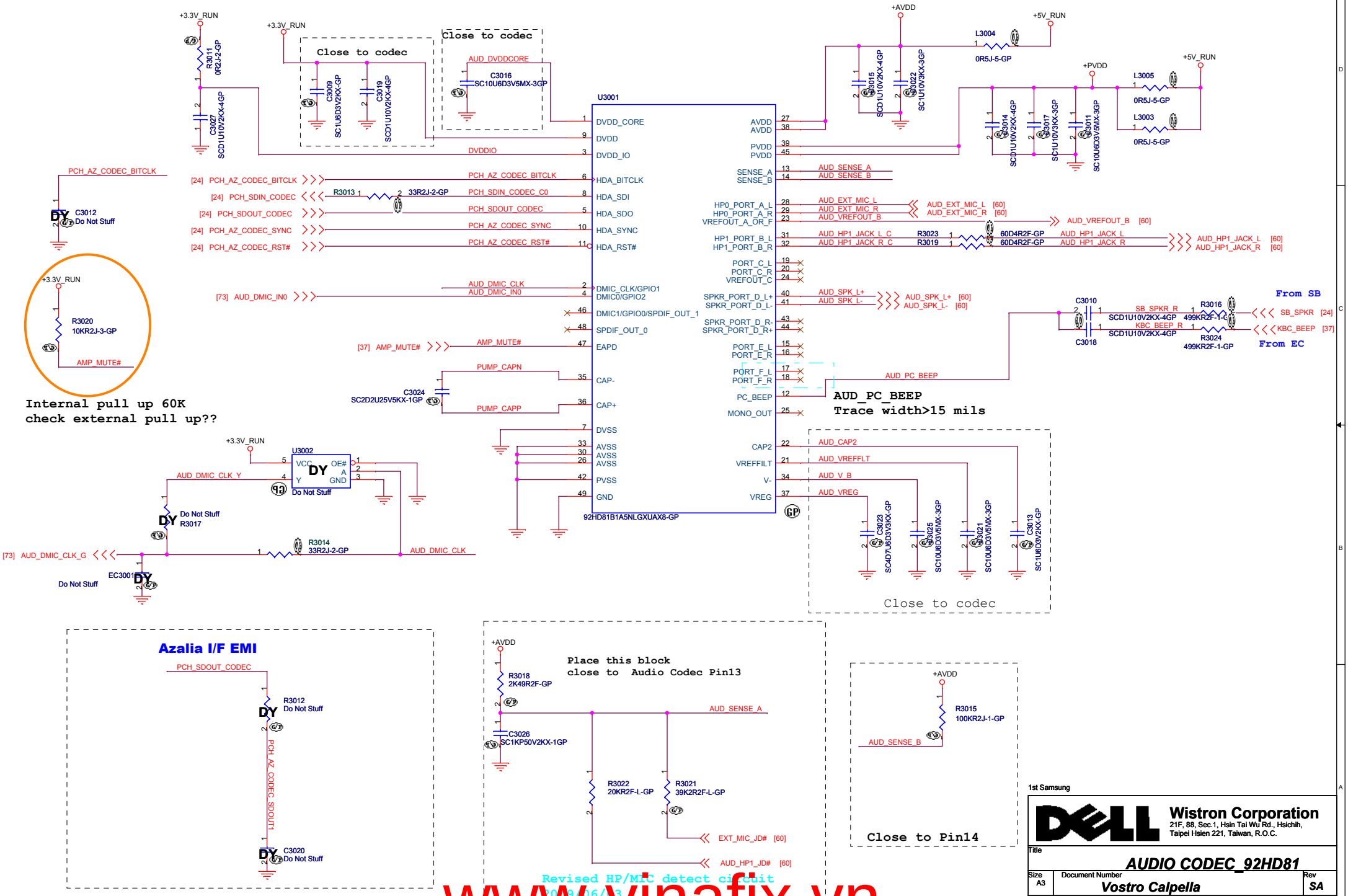
Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 29 of 88

SSID = AUDIO



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Title: AUDIO CODEC_92HD81

Size: A3 | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 30 of 88

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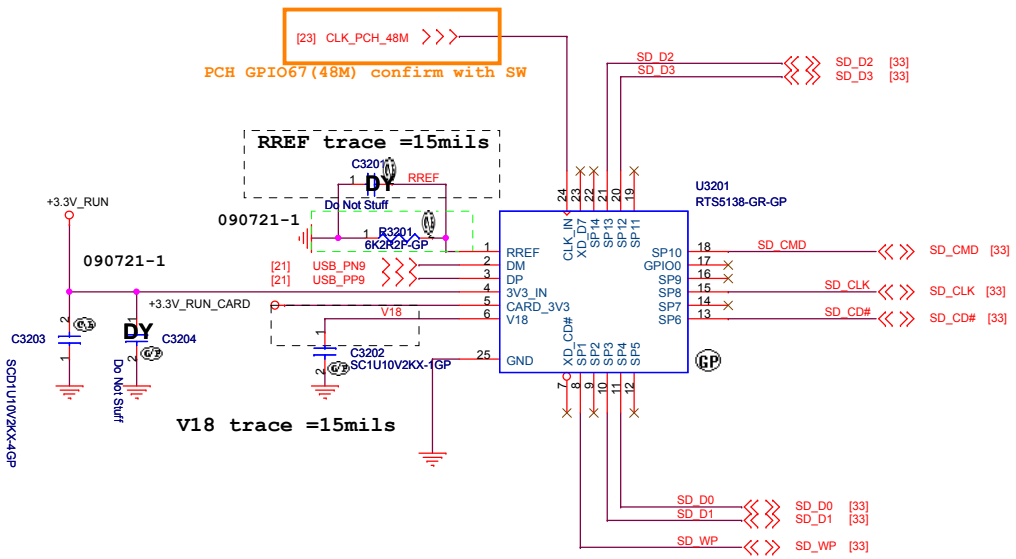
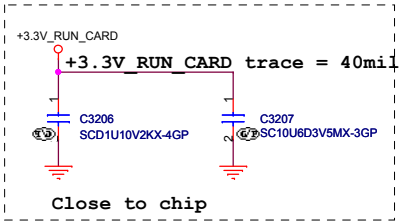
Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 31 of 88





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Title	CardReader/RTS5138	
Size: Custom	Document Number: Vostro Calpella	Rev: SA
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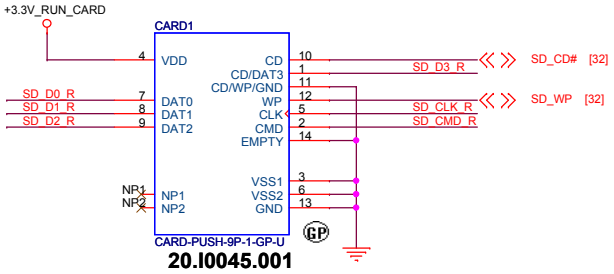
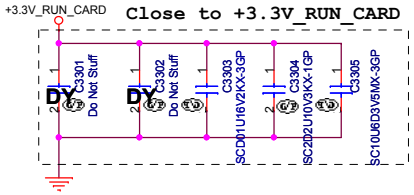
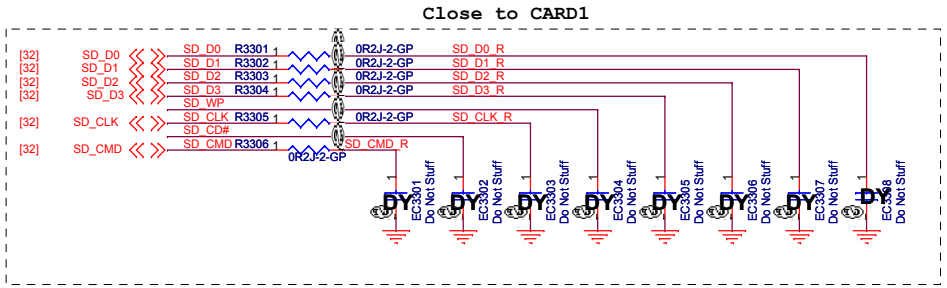
SSID = SDIO

SD/MMC/MMC+ Card Reader







SSID = 1394

Remove 1394

1st Samsung

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Title: CARD READER CONN

Size	Document Number	Rev
A3	Vostro Calpella	SA

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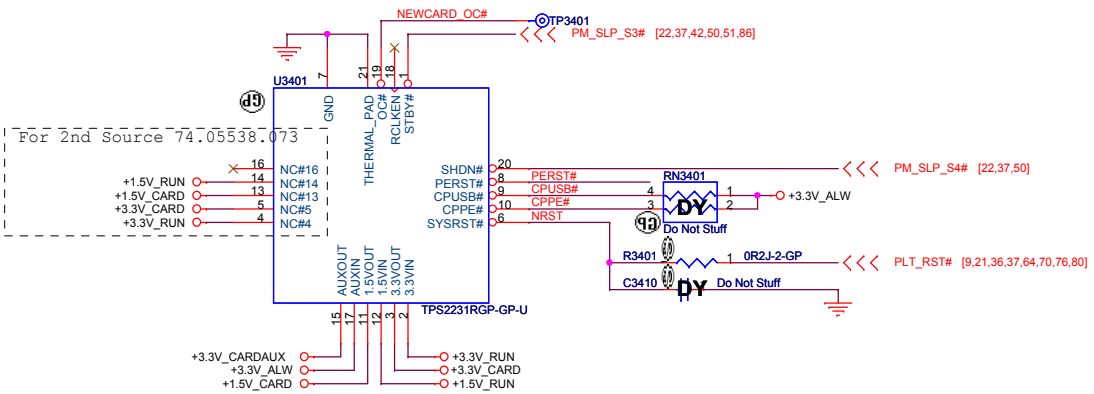
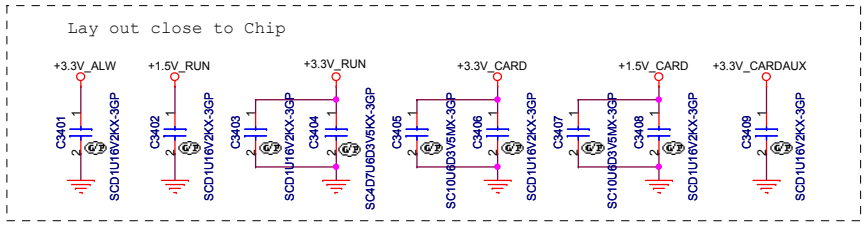
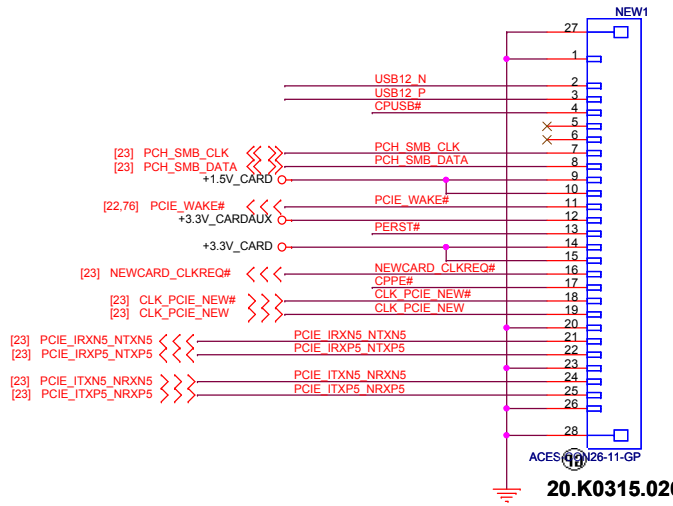
SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

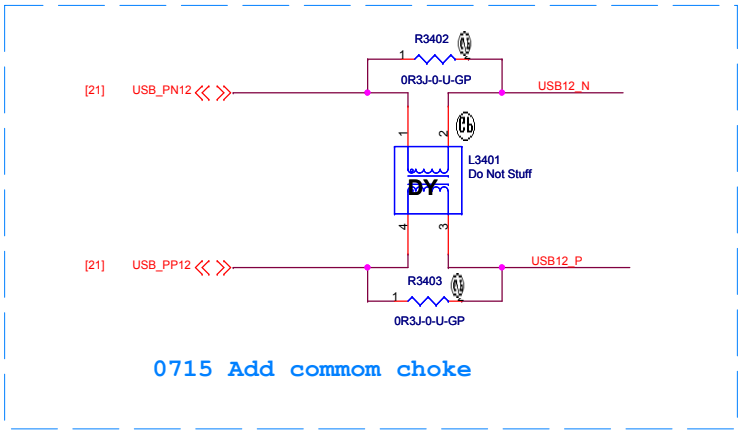


+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA





20.K0315.026



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Title	ExpressCard	
Size A3	Document Number Vostro Calpella	Rev SA
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Title: *(Reserve)*

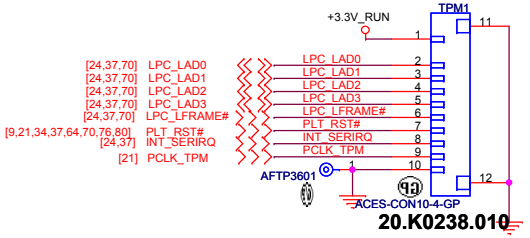
Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

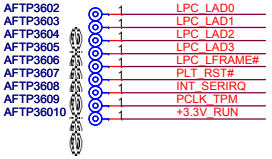
Date: Wednesday, September 02, 2009 | Sheet 35 of 88

SSID = User.Interface

Remove TPM EEPROM

TPM board CONN





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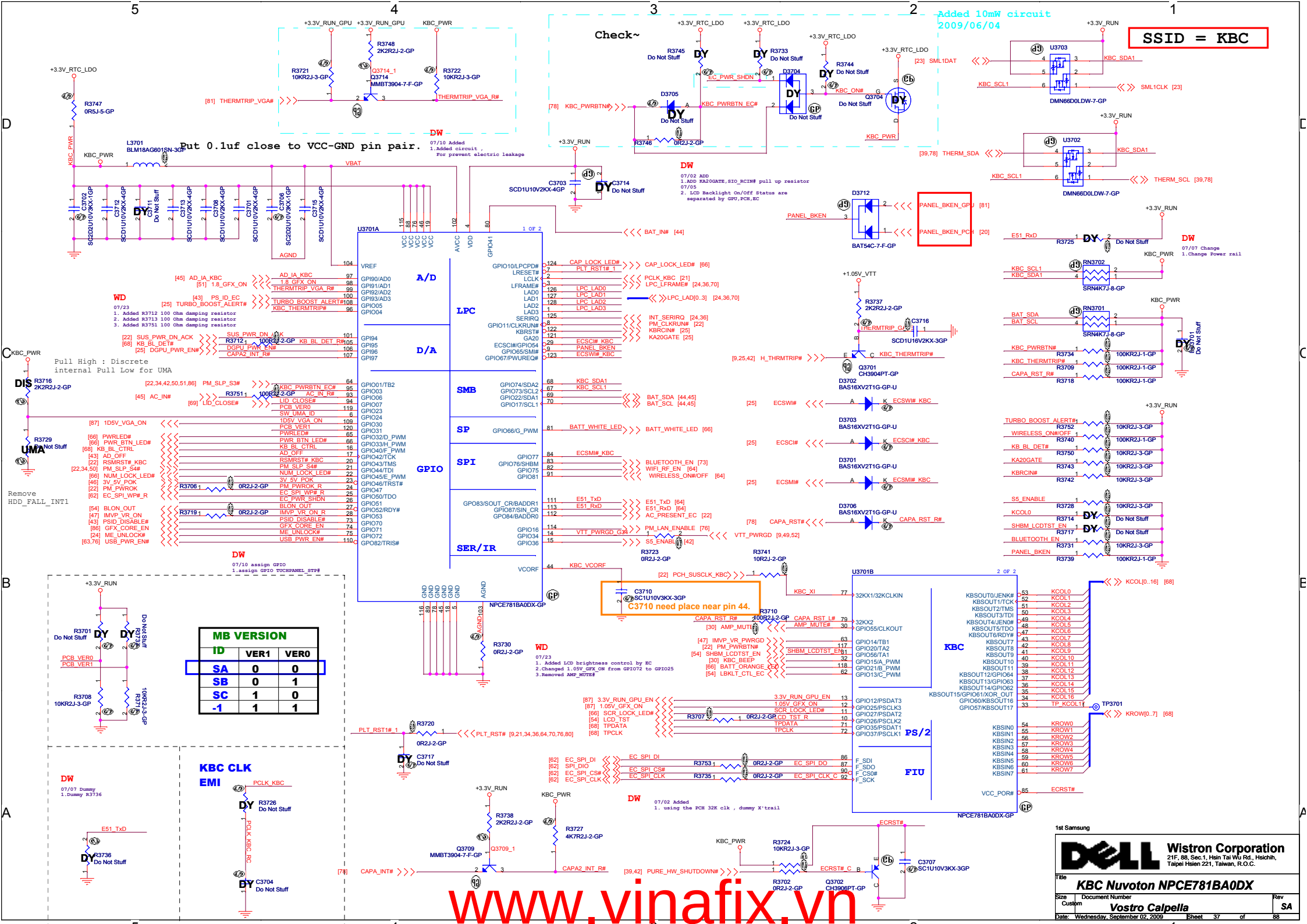
Title: TPM

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 36 of 88


SSID = KBC
Added 10mW circuit
2009/06/04
Check~
Put 0.1uf close to VCC-GND pin pair.
Pull High : Discrete
internal Pull Low for UMA
Remove
HDD_FALL_INT1
C3710 need place near pin 44.
MB VERSION
ID | VER1 | VER0
SA | 0 | 0
SB | 0 | 1
SC | 1 | 0
-1 | 1 | 1
KBC CLK
EMI
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
Vostro Calpella
Wednesday, September 02, 2009
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Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

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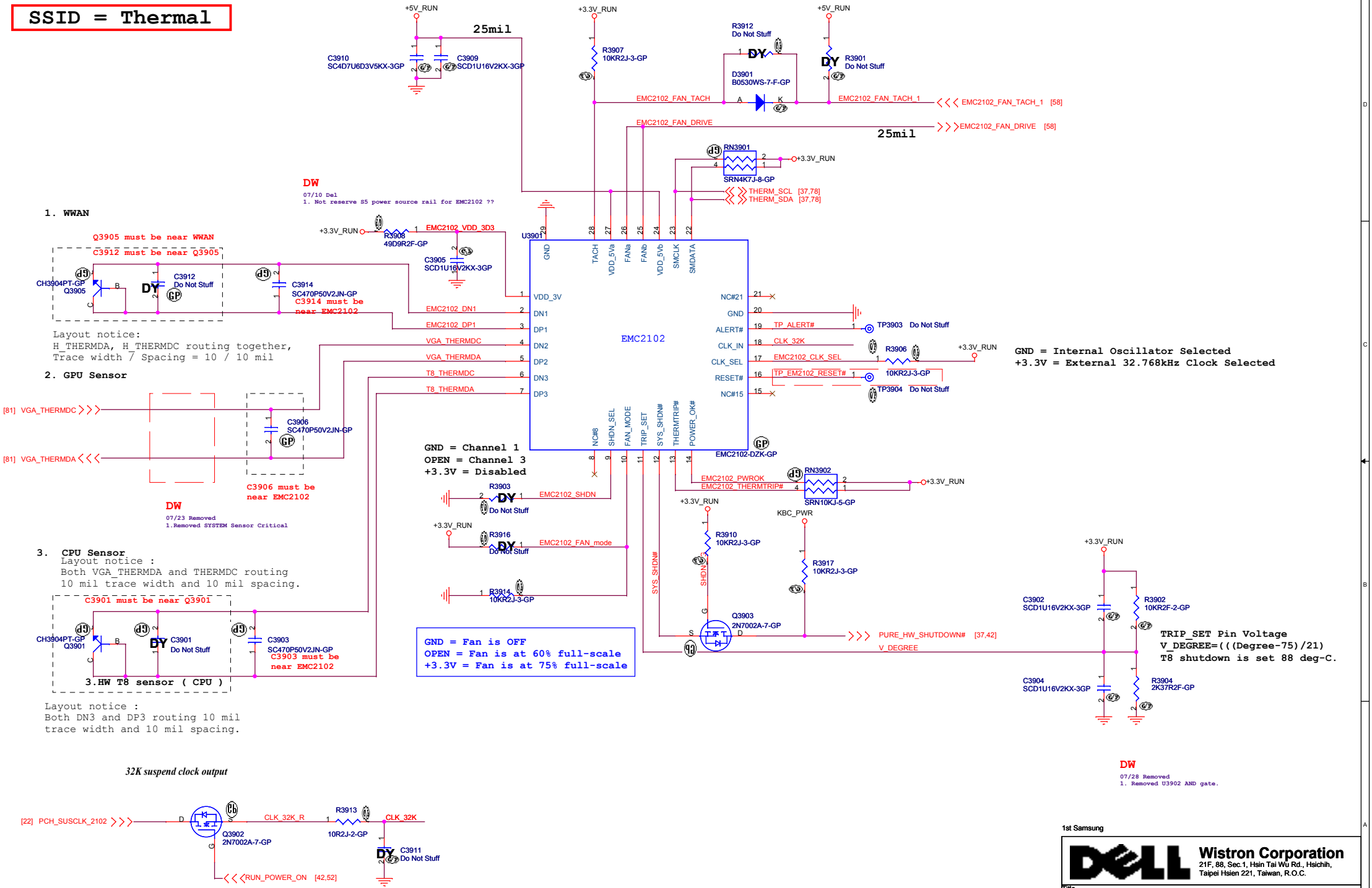
SSID = Thermal



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Title: Thermal/Fan Controllor EMC2102

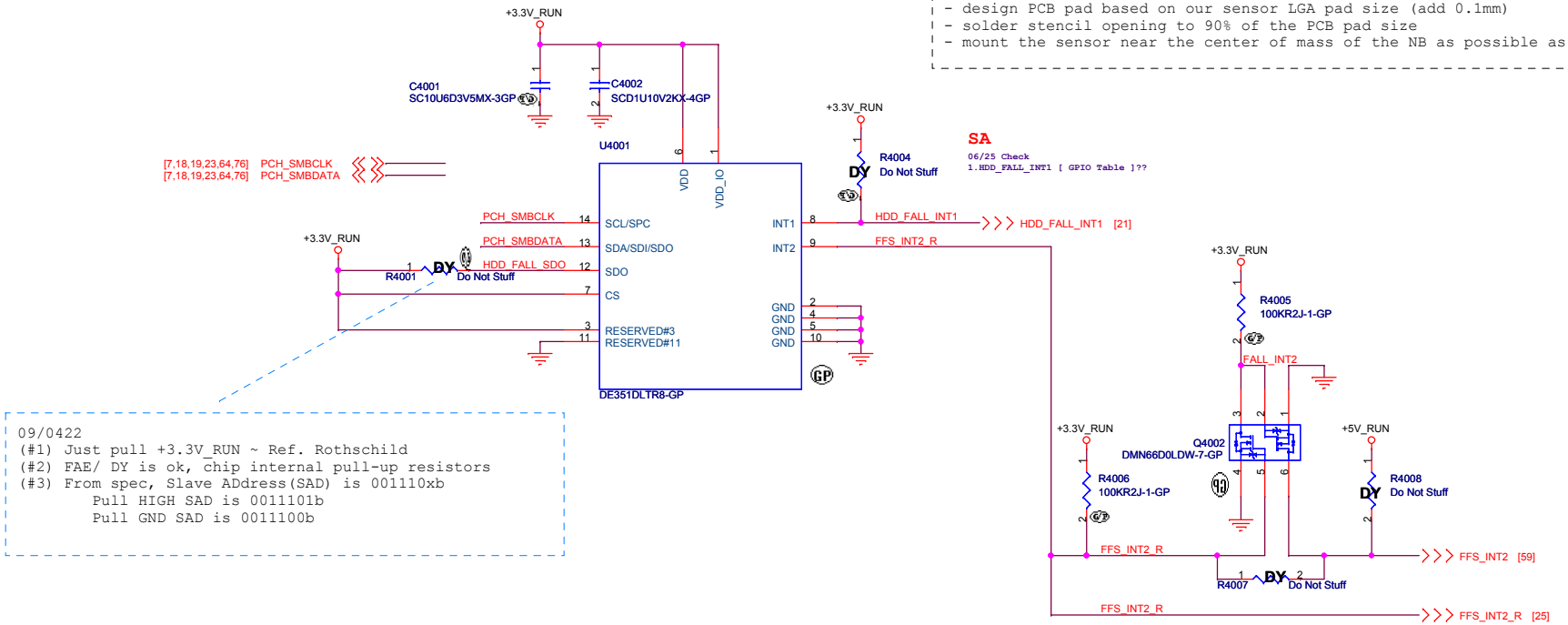
Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 39 of 88

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 40 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

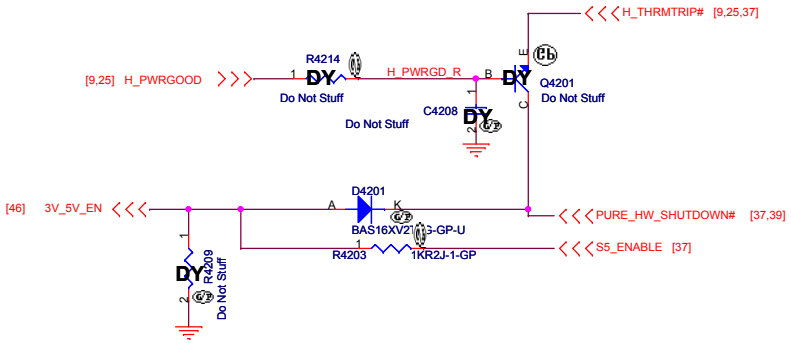
Title: *(Reserve)*

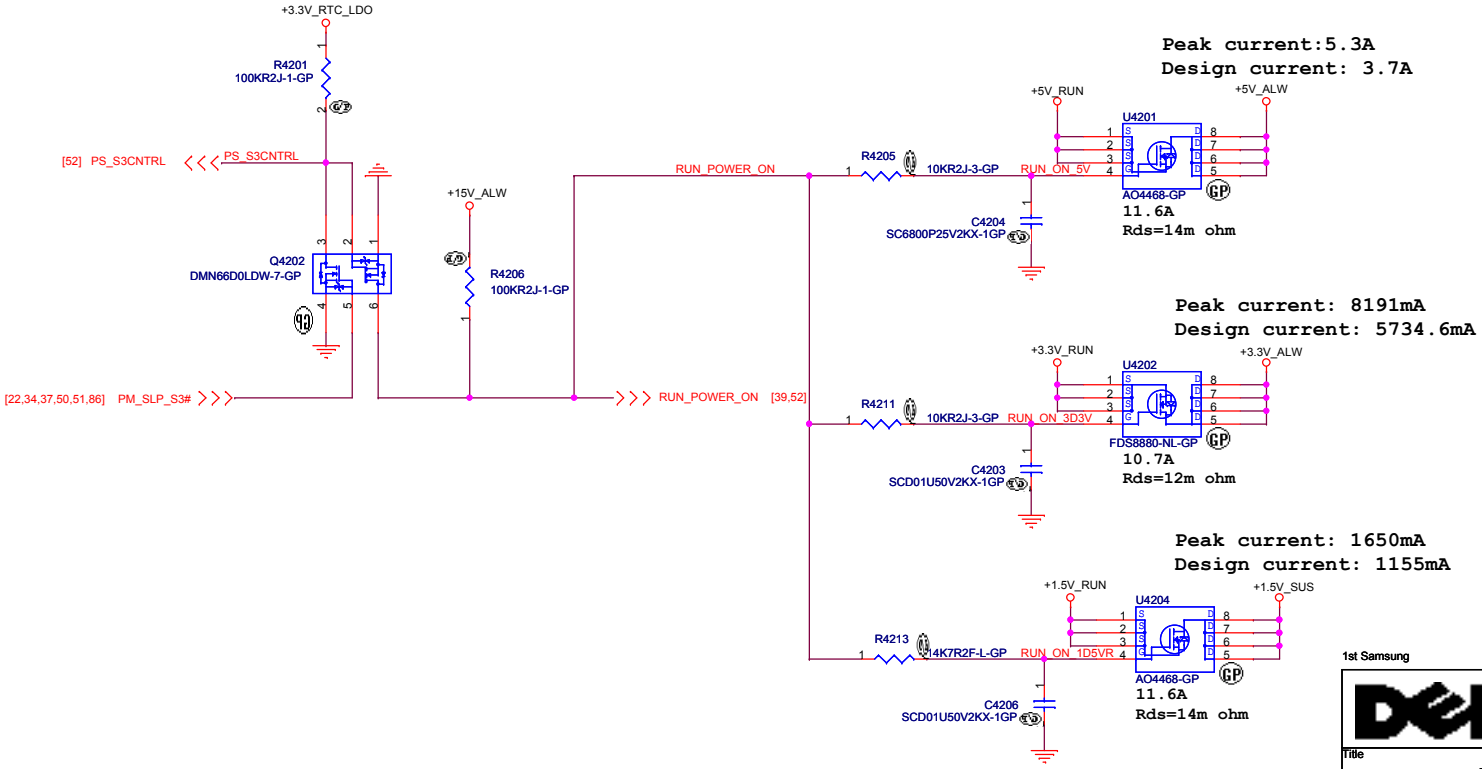
Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 41 of 88

SSID = Reset.Suspend

Remove +3.3V_DELAY power rail 2009/05/25





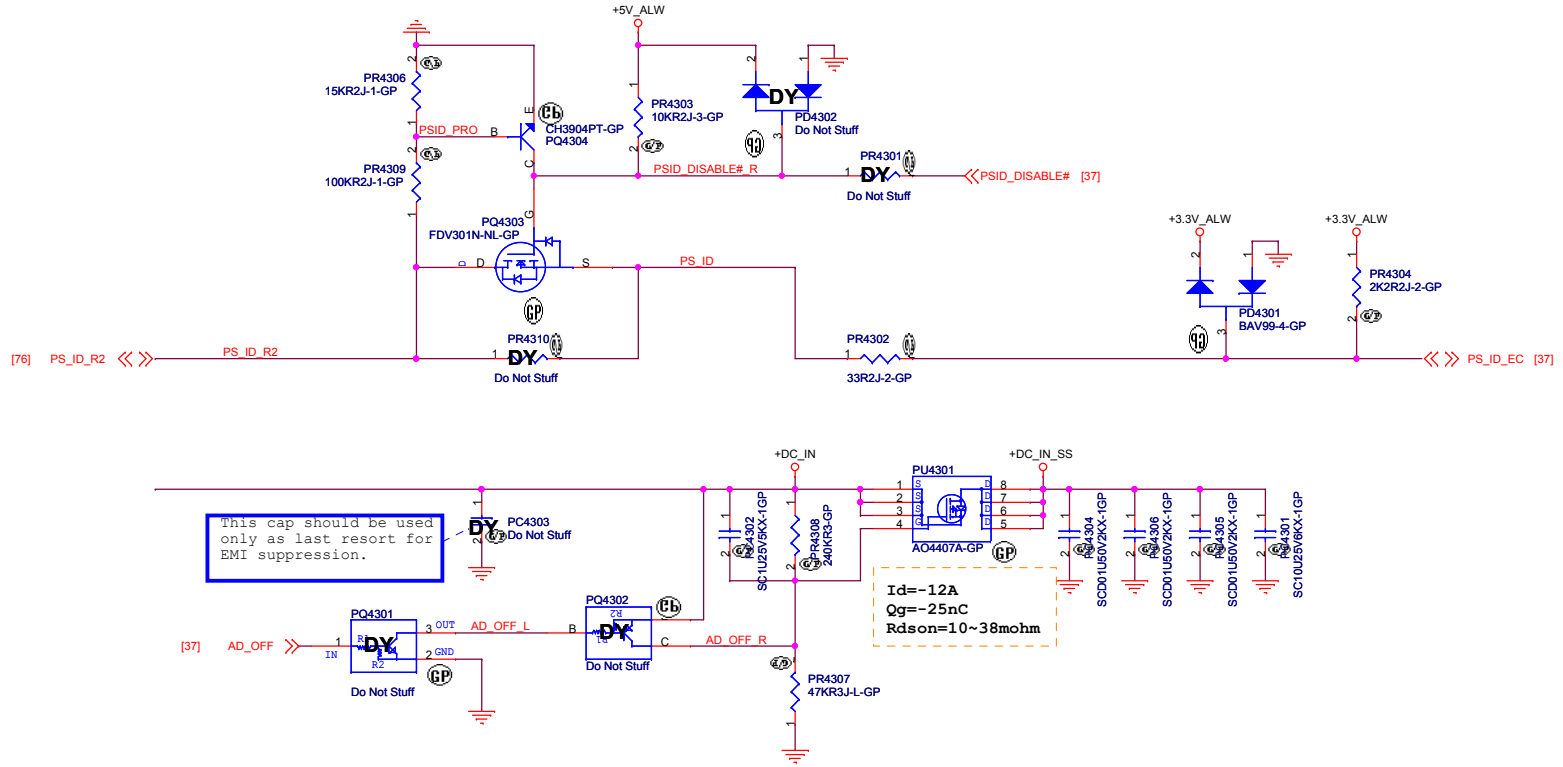
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size	Document Number	Rev
Custom	***Vostro Calpella***	*SA*

Date: Wednesday, September 02, 2009 Sheet 42 of 88



1st Samsung

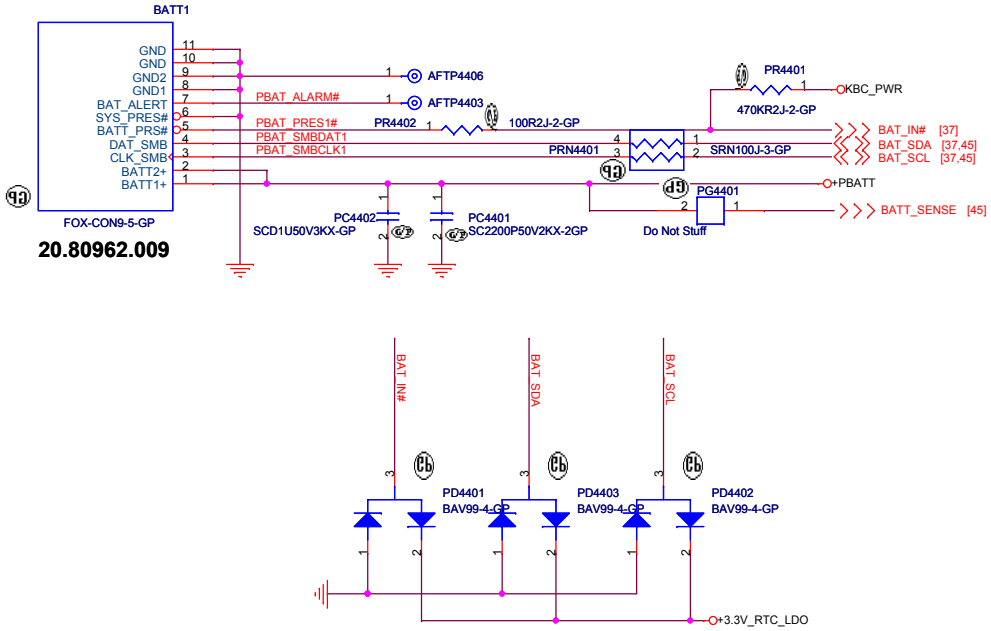
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 43 of 88

Batt Connecter

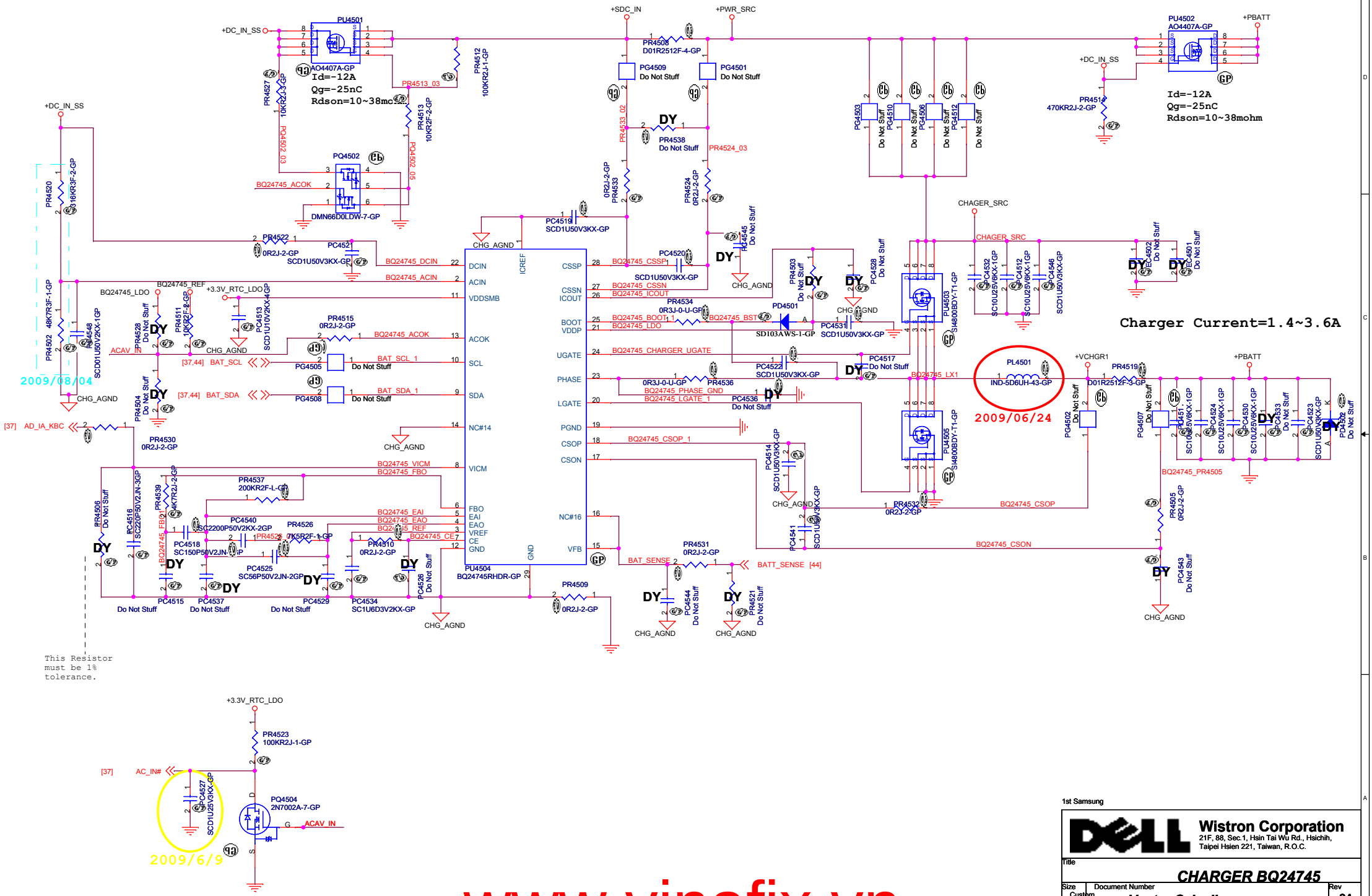


1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Batt Connecter***	
Size: A3	Document Number: ***Vostro Calpella***	Rev: ***SA***
Date: Wednesday, September 02, 2009	Sheet 44 of 88	

SSID = Charger



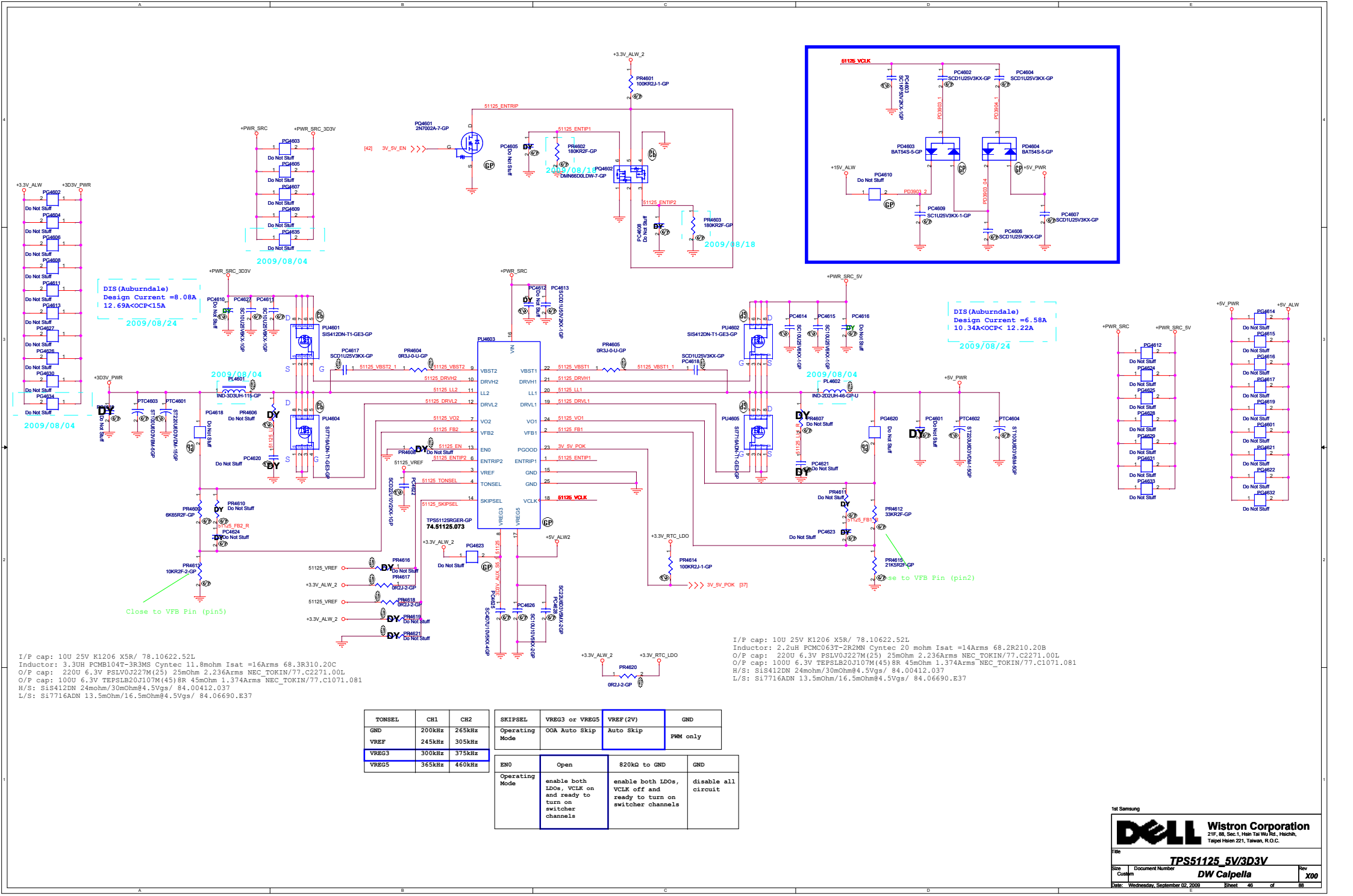
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 45 of 88



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

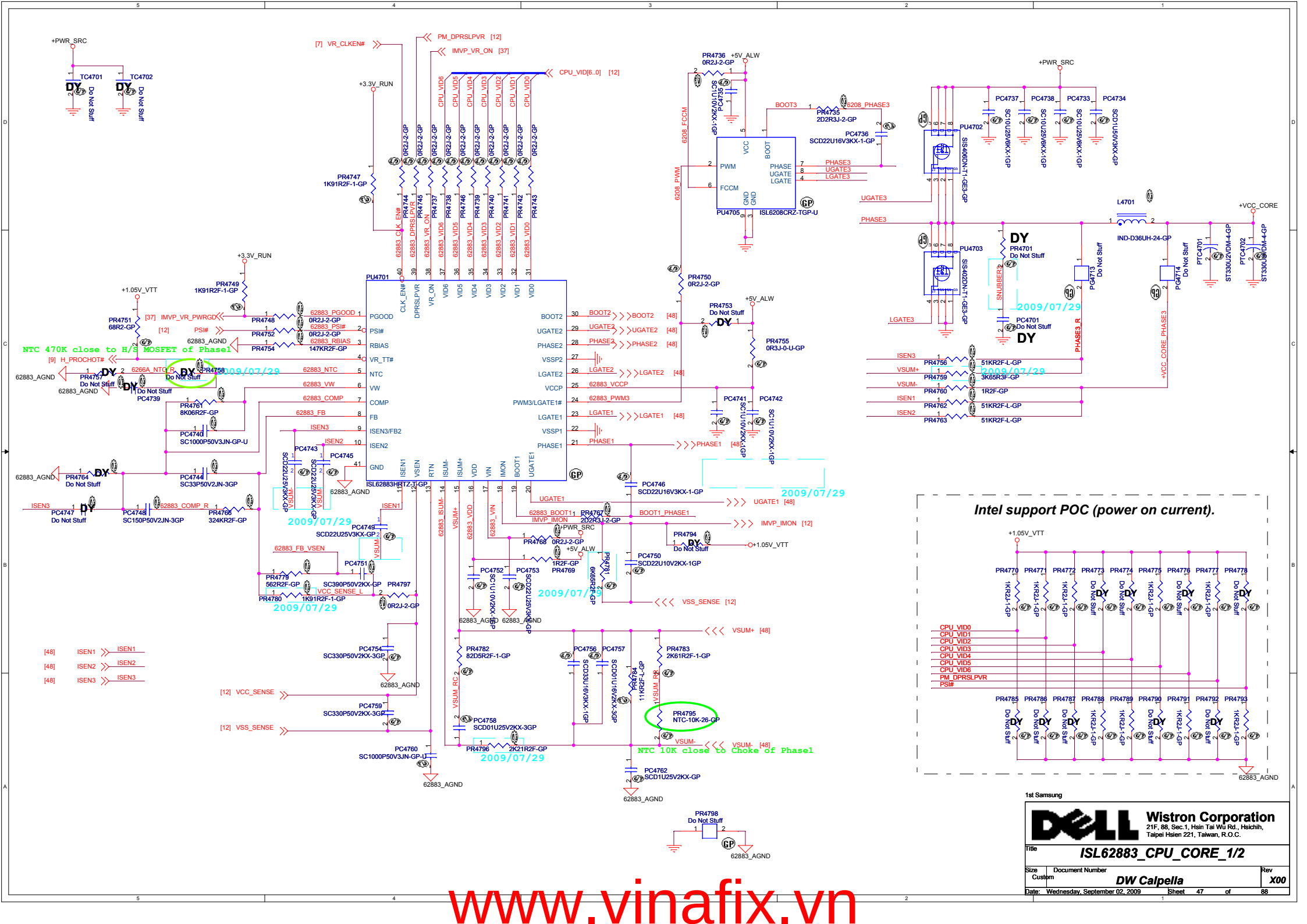
1st Samsung

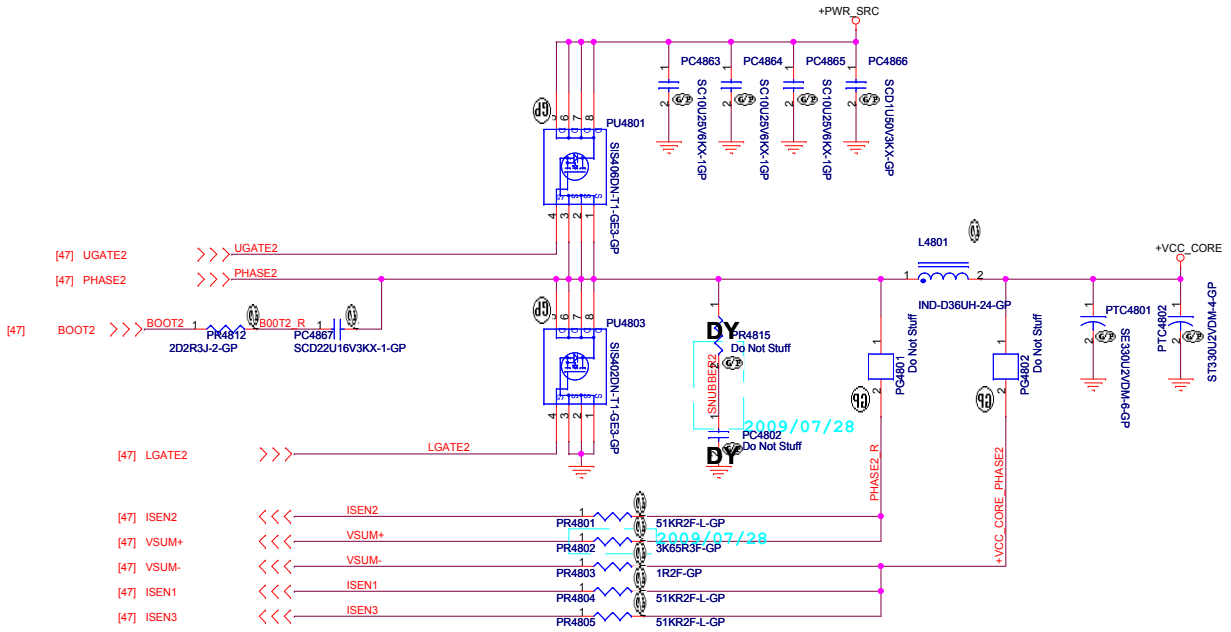
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

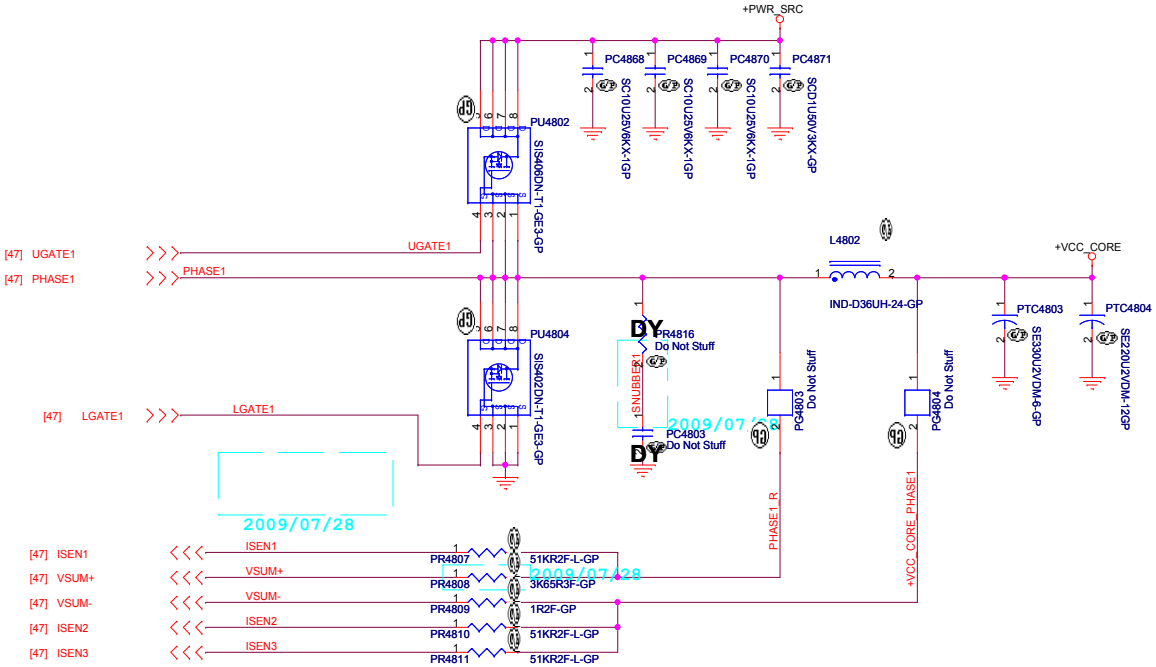
Size: Custom | Document Number: DW Calpella | Rev: X00

Date: Wednesday, September 02, 2009 | Sheet 46 of 88





DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiR474DP/ POWERPAK-8/ 10mOhm/12mOhm @4.5Vgs/ 84.00474.037
L/S: Si7170DP/ POWERPAK-8/ 3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037
Freq=300KHz@PER PHASE

1st Samsung

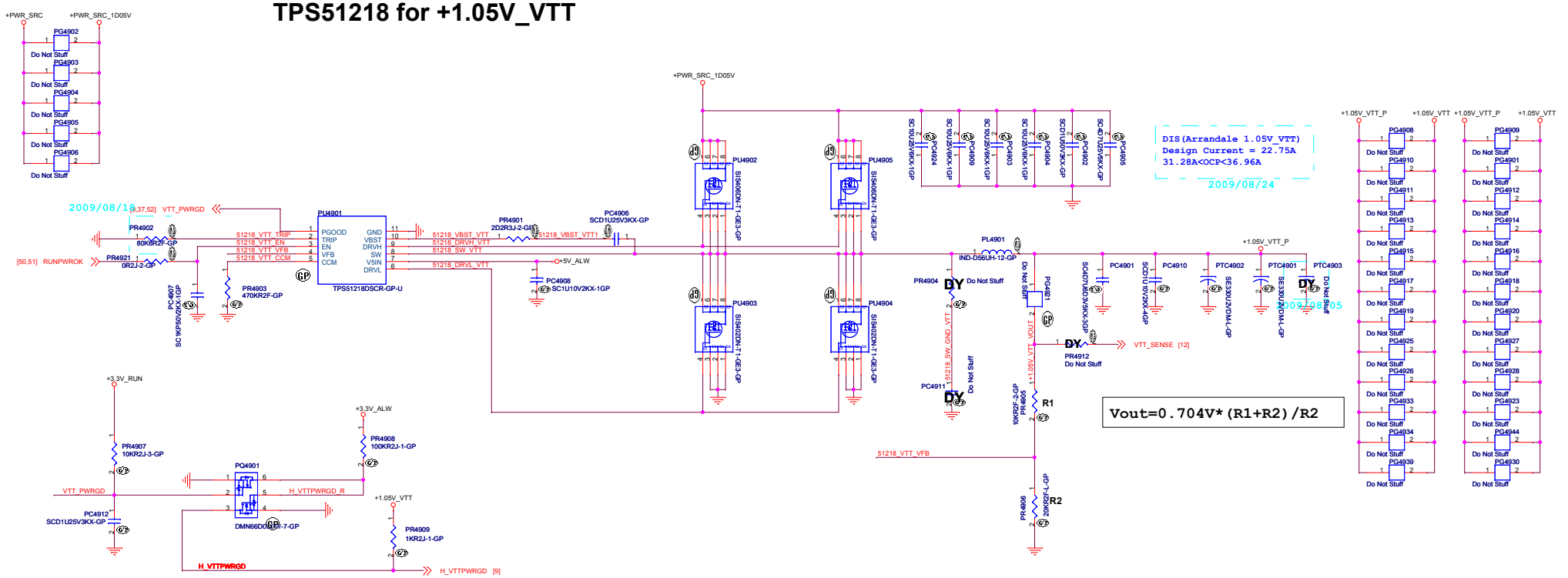
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE_2/2

Size: Custom | Document Number: DW Calpella | Rev: X00

Date: Wednesday, September 02, 2009 | Sheet 48 of 88

TPS51218 for +1.05V_VTT



Frequency setting
470K --> 290KHz
200K --> 340KHz
100K --> 380KHz
39K --> 430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

1st Samsung

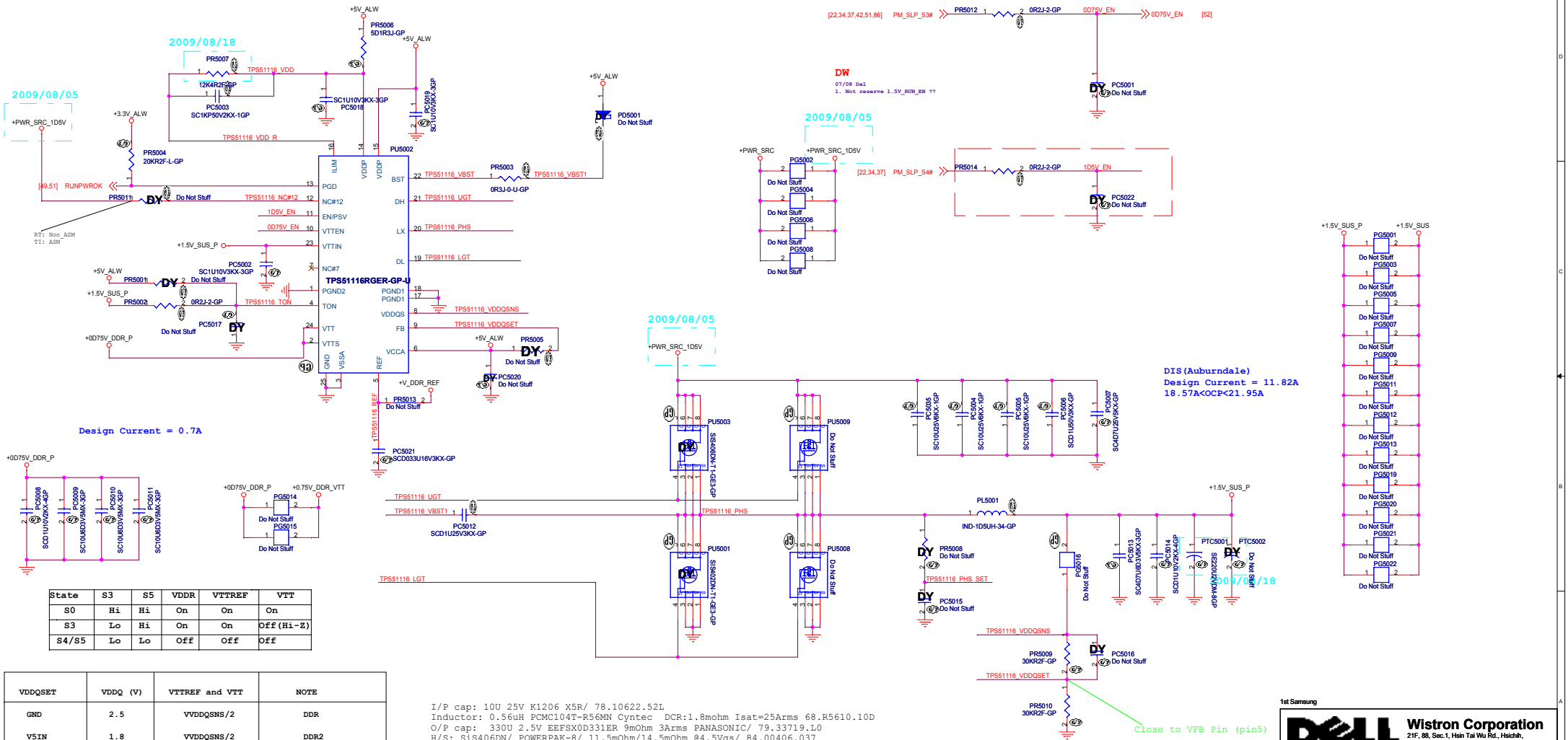
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VTT

Size	Document Number	Rev
Custom	DW Calpella	X00

Date: Wednesday, September 02, 2009 Sheet 49 of 88

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Switching freq-->400KHz

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

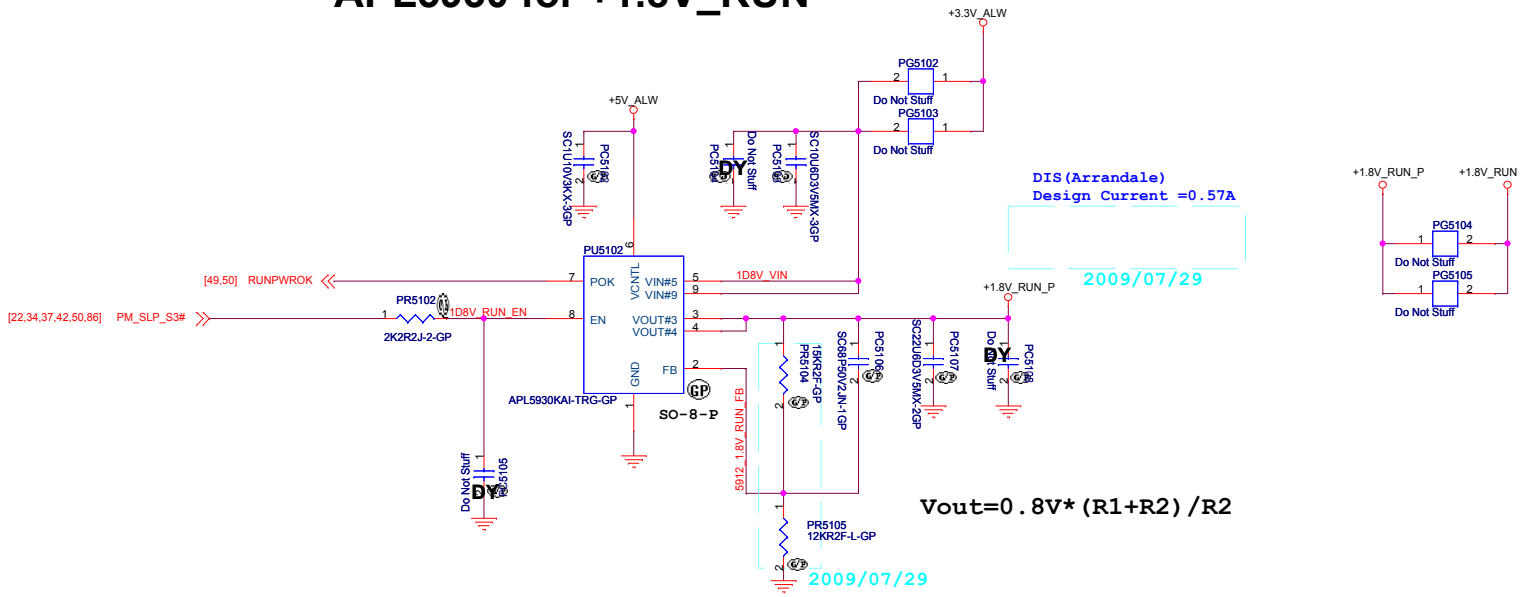
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: DW Calpella | Rev: X00

Date: Thursday, September 03, 2009 | Sheet 50 of 88

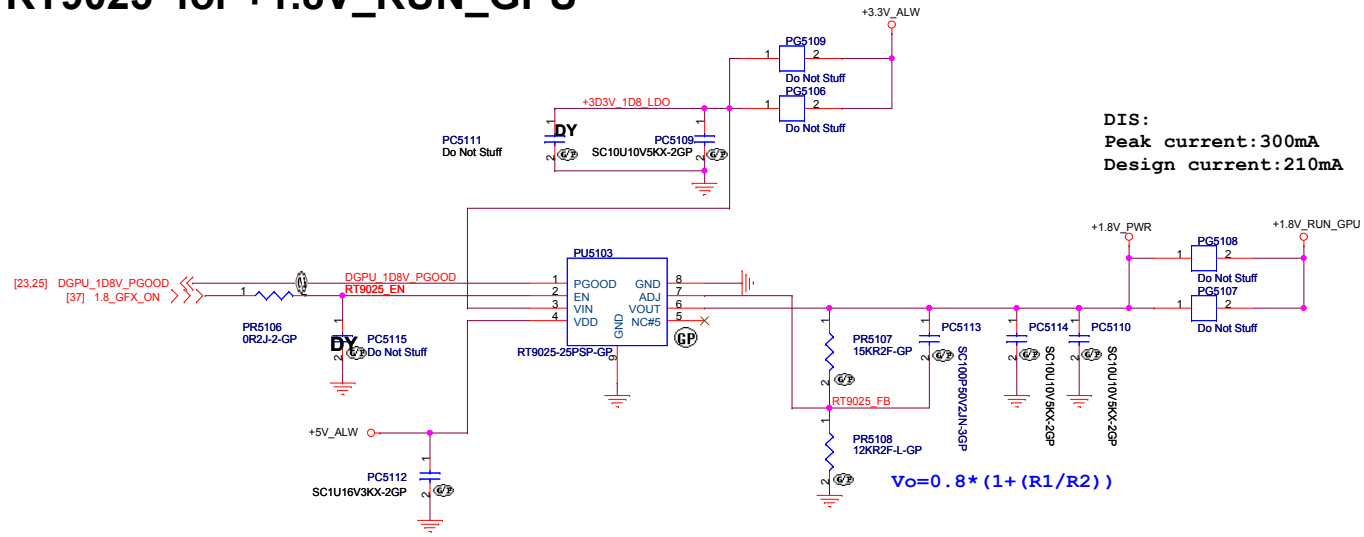
SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



Vout=0.8V*(R1+R2)/R2

RT9025 for +1.8V_RUN_GPU



Vo=0.8*(1+(R1/R2))

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5930/RT9205

Size	Document Number	Rev
Custom	DW Calpella	X00

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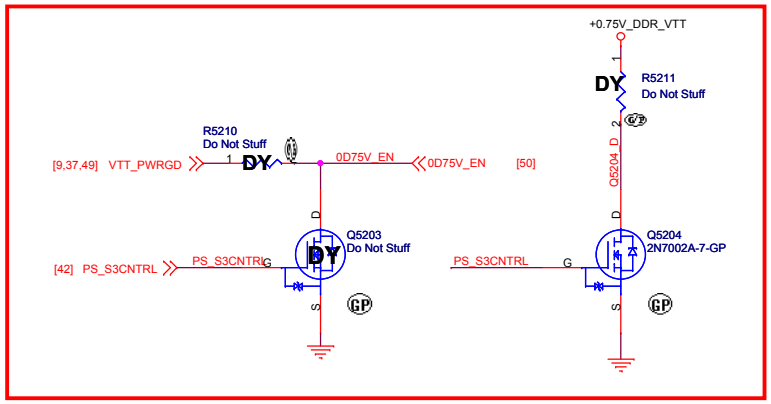
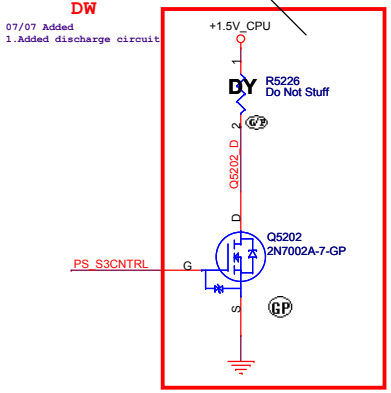


Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

Revision 0.1

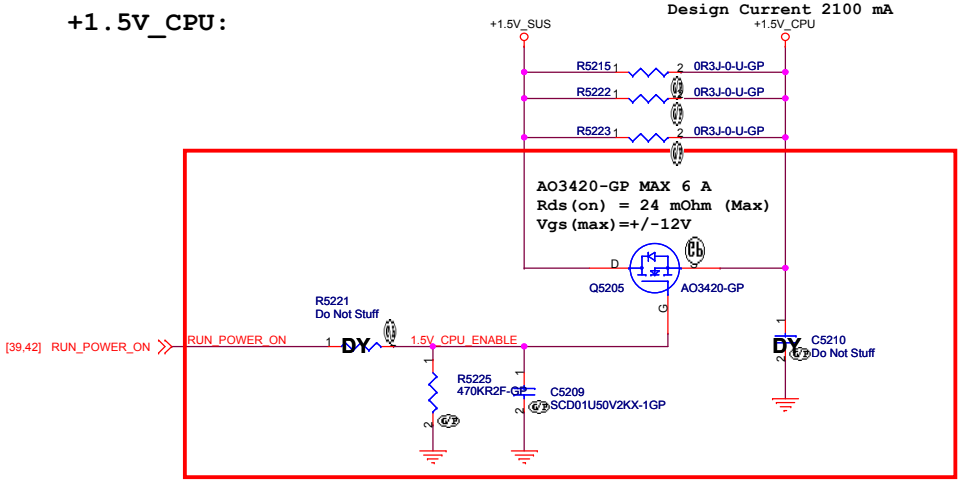
DW

07/07 Added
1.Added discharge circuit



+1.5V_CPU:

MAX Current 3000 mA
Design Current 2100 mA



DW

07/20 corrected
1. Removed C5288
2. RemovedQ5207,R5225,R5220 to save more part counts

1st Samsung

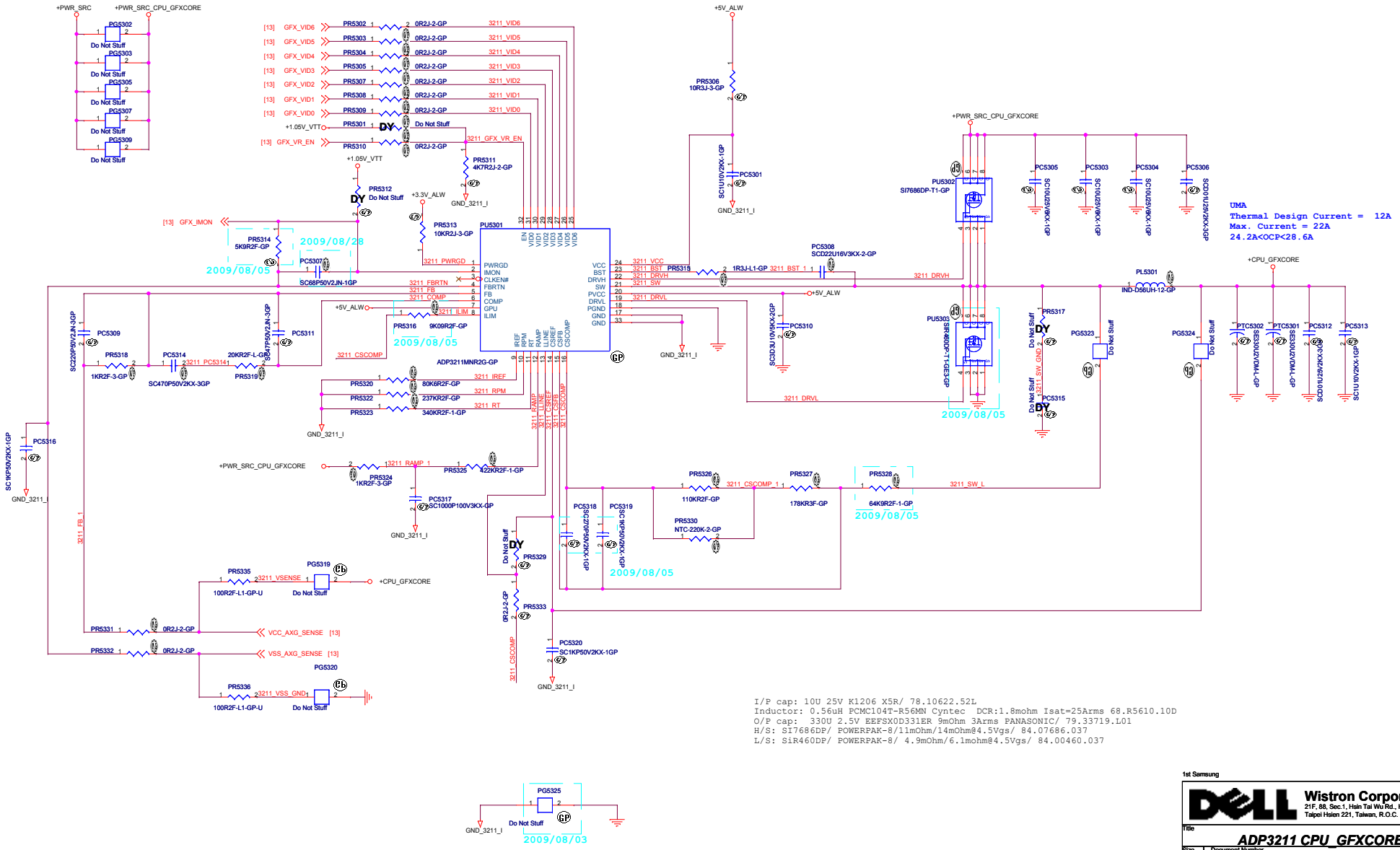
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D5V

Size: Custom | Document Number: Vostro Calpella | Rev: SA

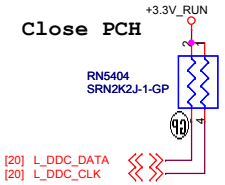
Date: Wednesday, September 02, 2009 | Sheet 52 of 88

SSID = CPU.GFX.Regulator

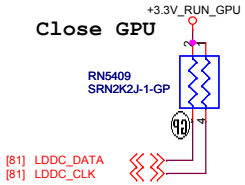


SSID = VIDEO

Close PCH



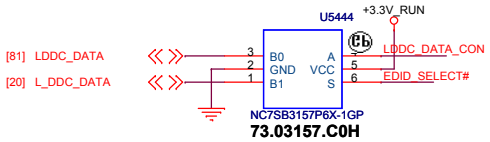
Close GPU



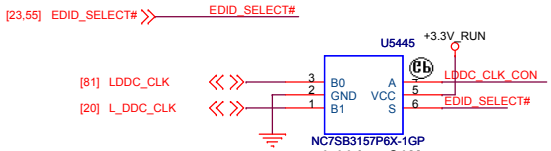
DW

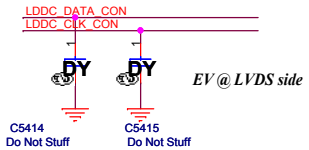
07/07 Added
1.Added LVDS DDC CLK/DAT Pull Hi

UMA/DIS LVDS DDC CLK/DAT select circuit

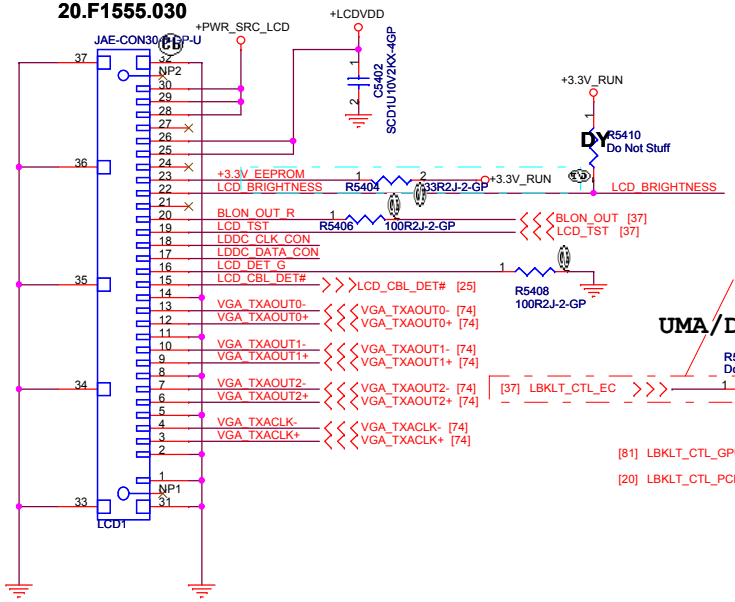


H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)





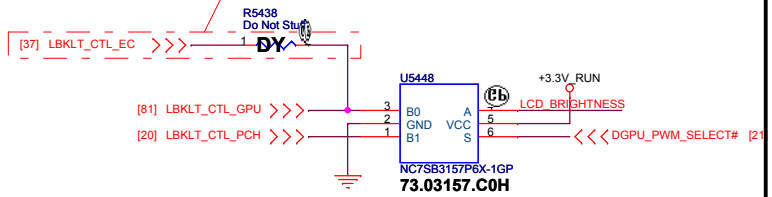
LVDS CONNECTOR
20.F1555.030



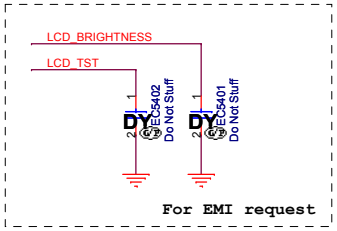
WD

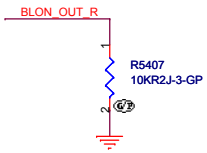
07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
07/23
1. Added LCD brightness control by EC
07/28
1. Removed LCD brightness control with EC and GPU

UMA/DIS LVDS PWM select circuit



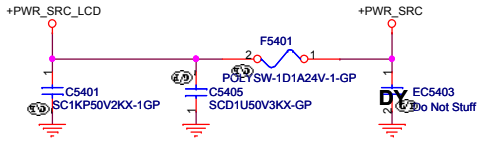
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)





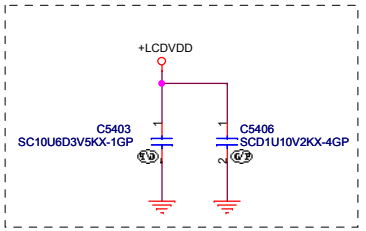
SSID = Inverter

INVERTER POWER

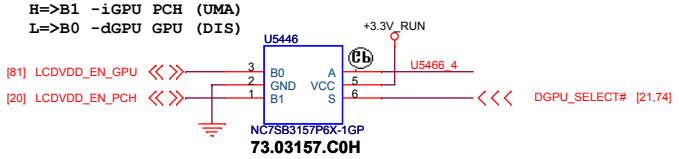


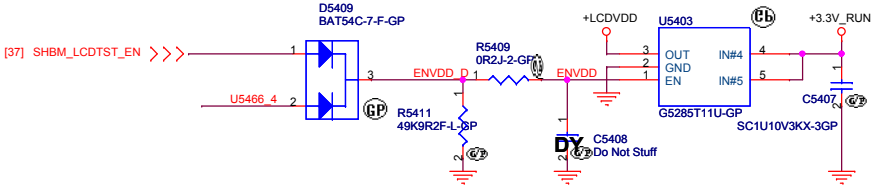
SSID = VIDEO

LCD POWER



DGPU_SELECT# :
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)





1st Samsung

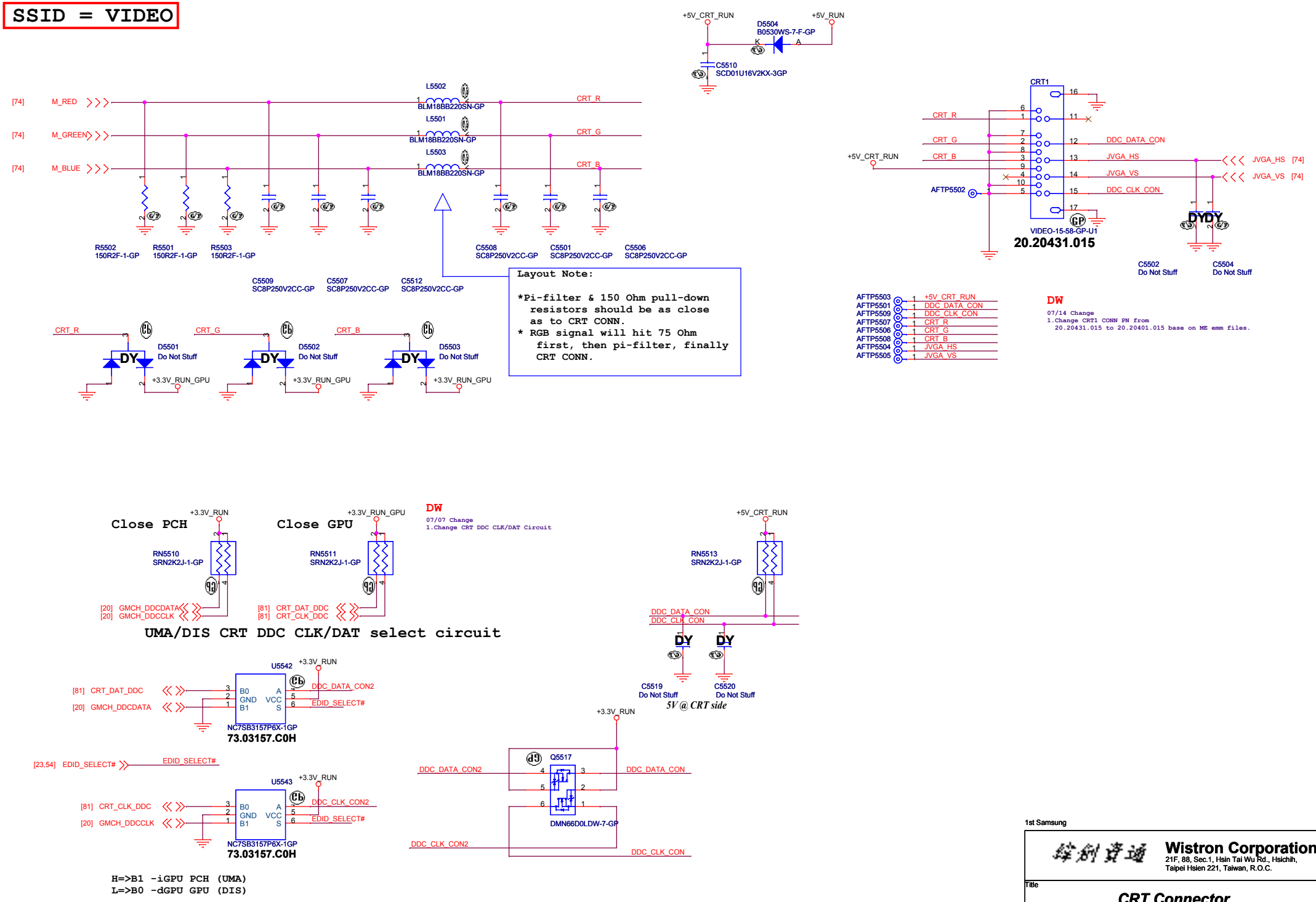
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

Size: Custom | Document Number: **Vostro Calpella** | Rev: **SA**

Date: Wednesday, September 02, 2009 | Sheet 54 of 88

SSID = VIDEO



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 55 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 56 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

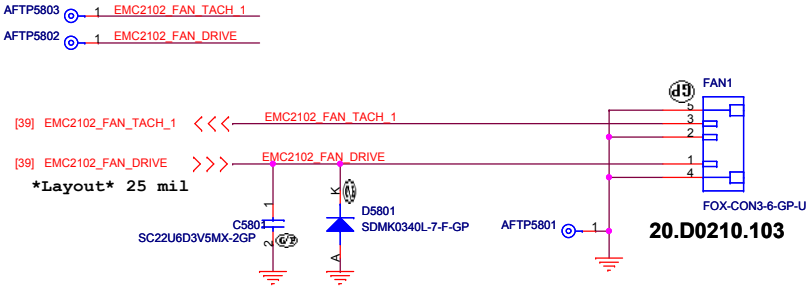
Title: HDMI Connector

Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 57 of 88

SSID = Thermal

Fan Connector



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

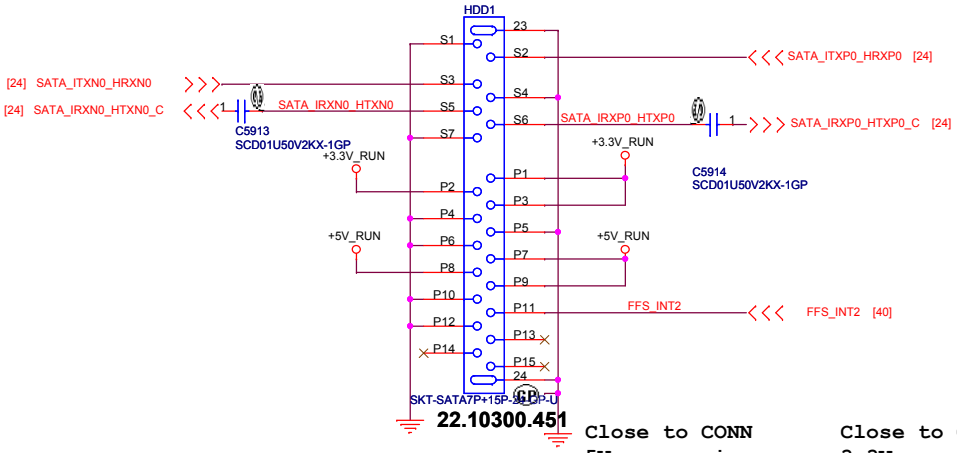
Title: FAN

Size: A3 | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 58 of 88

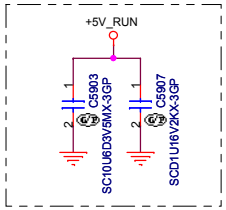
SSID = SATA

SATA HDD Connector

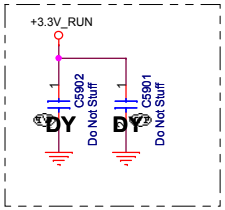



```
SATA HDD Interface comment
*****************************
S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND
*****************************
P1------------ 3.3V
P2------------ 3.3V
P3------------ 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7------------ 5V
P8------------ 5V
P9------------ 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13------------ 12V
P14------------ 12V
P15------------ 12V
*****************************
```

Close to CONN
5V power pin

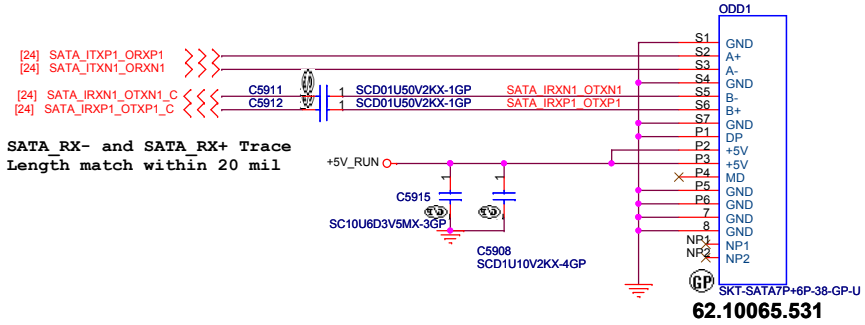


Close to CONN
3.3V power pin



SSID = SATA

ODD Connector



1st Samsung

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD Connector

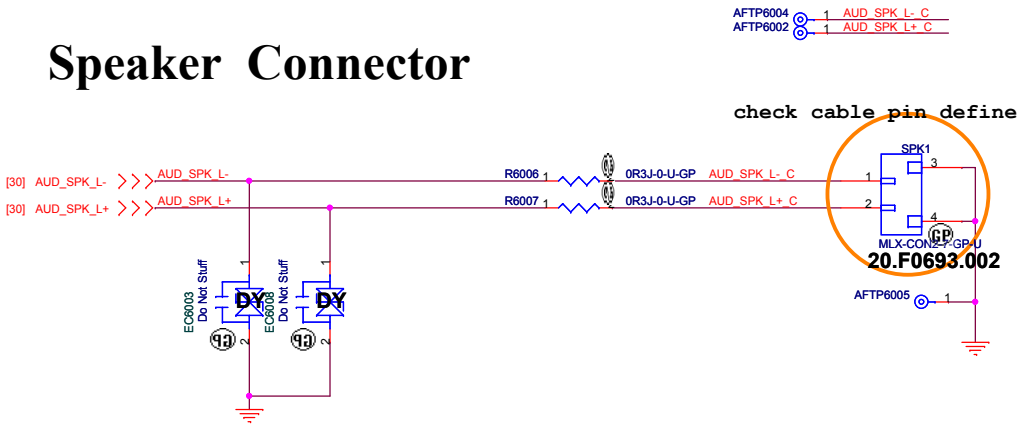
Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 59 of 88

SSID = AUDIO

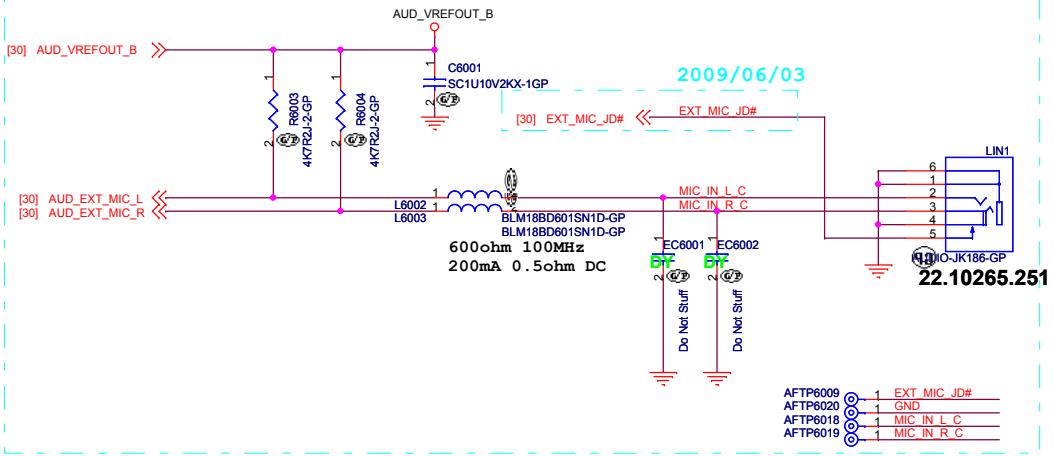
Speaker Connector

check cable pin define



SSID = AUDIO

MIC IN

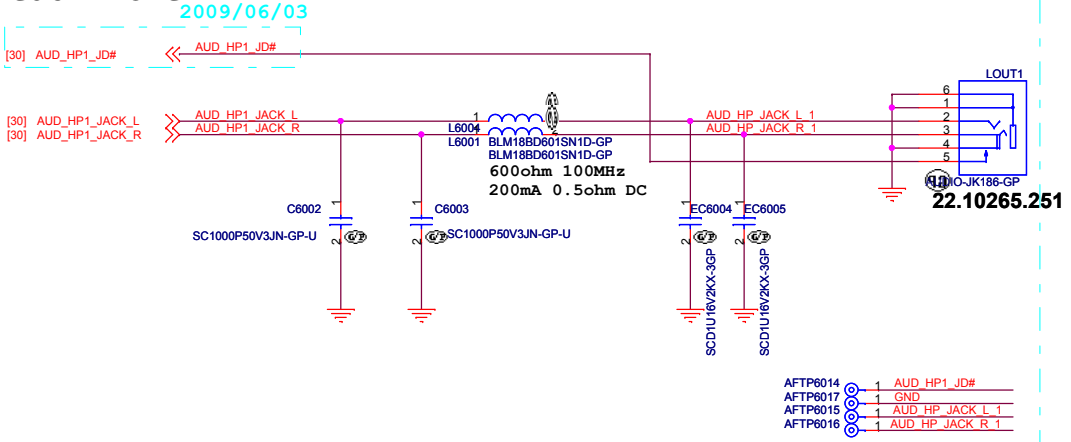


Added MIC circuit 2009/05/26

Delete Audio De-pop Circuit
2009/07/24

SSID = AUDIO

Head Phone



Added HP circuit 2009/05/26

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER/MIC/AUDIO JACK

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 60 of 88

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Taipei Hsien 221, Taiwan, R.O.C.

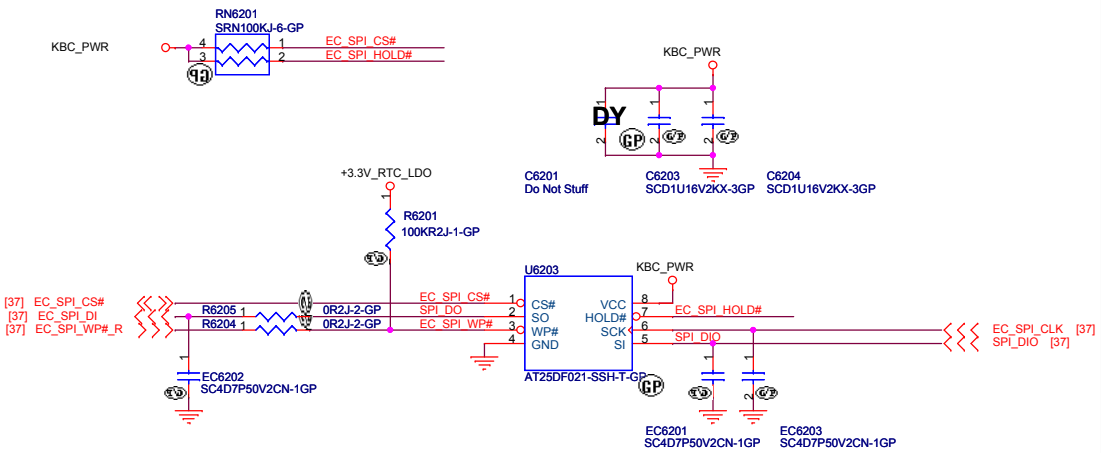
Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

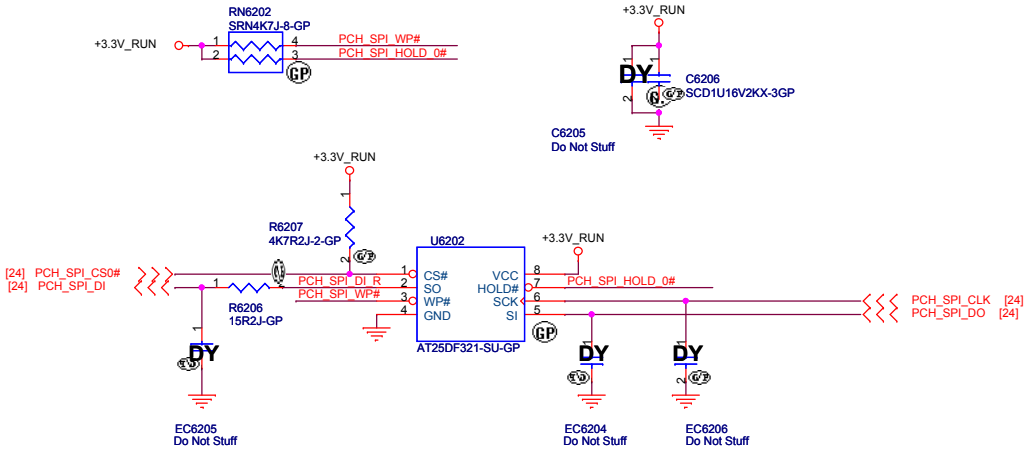
Date: Wednesday, September 02, 2009 | Sheet 61 of 88

SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

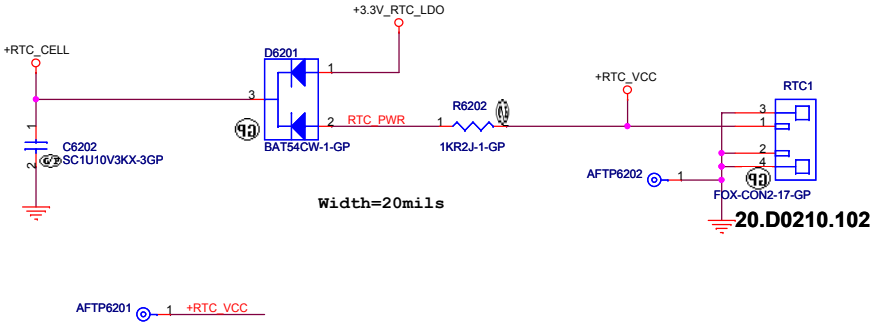


SPI FLASH ROM (32M bits) for PCH



SSID = RBATT

RTC Connector



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

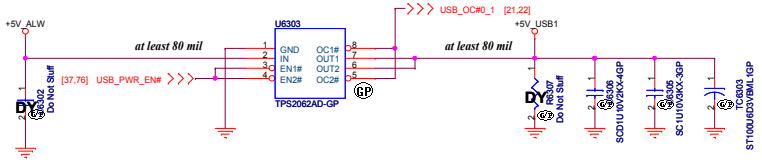
Title: EEPROM/RTC Connector

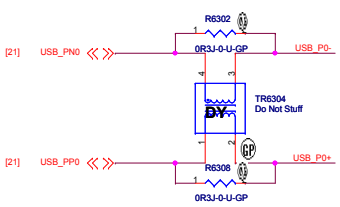
Size	Document Number	Rev
A3	Vostro Calpella	SA

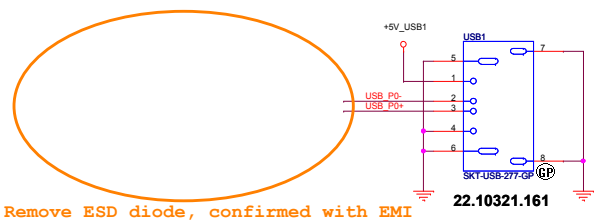
Date: Wednesday, September 02, 2009 Sheet 62 of 88

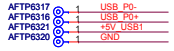
SSID = USB

USB & ESATA Power SW



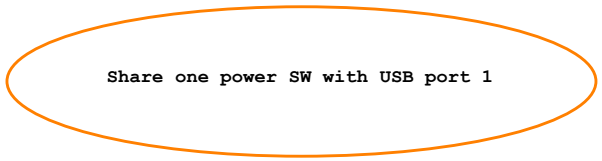


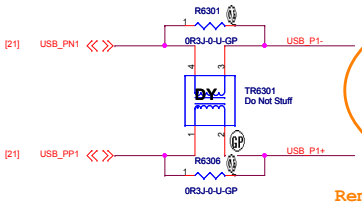


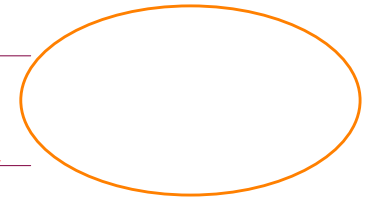


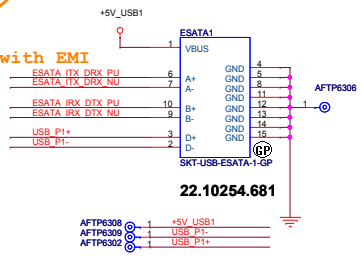
SSID = ESATA

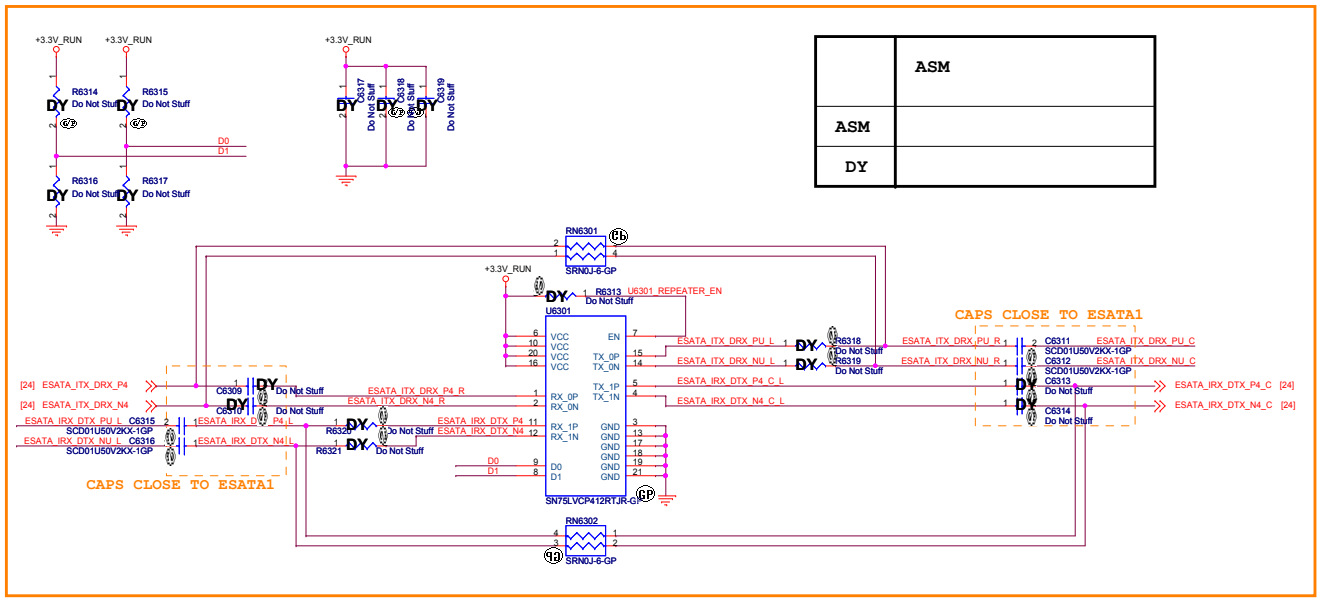
ESATA Power



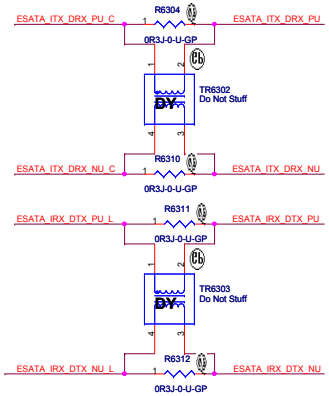








	ASM
ASM	
DY	



1st Samsung

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

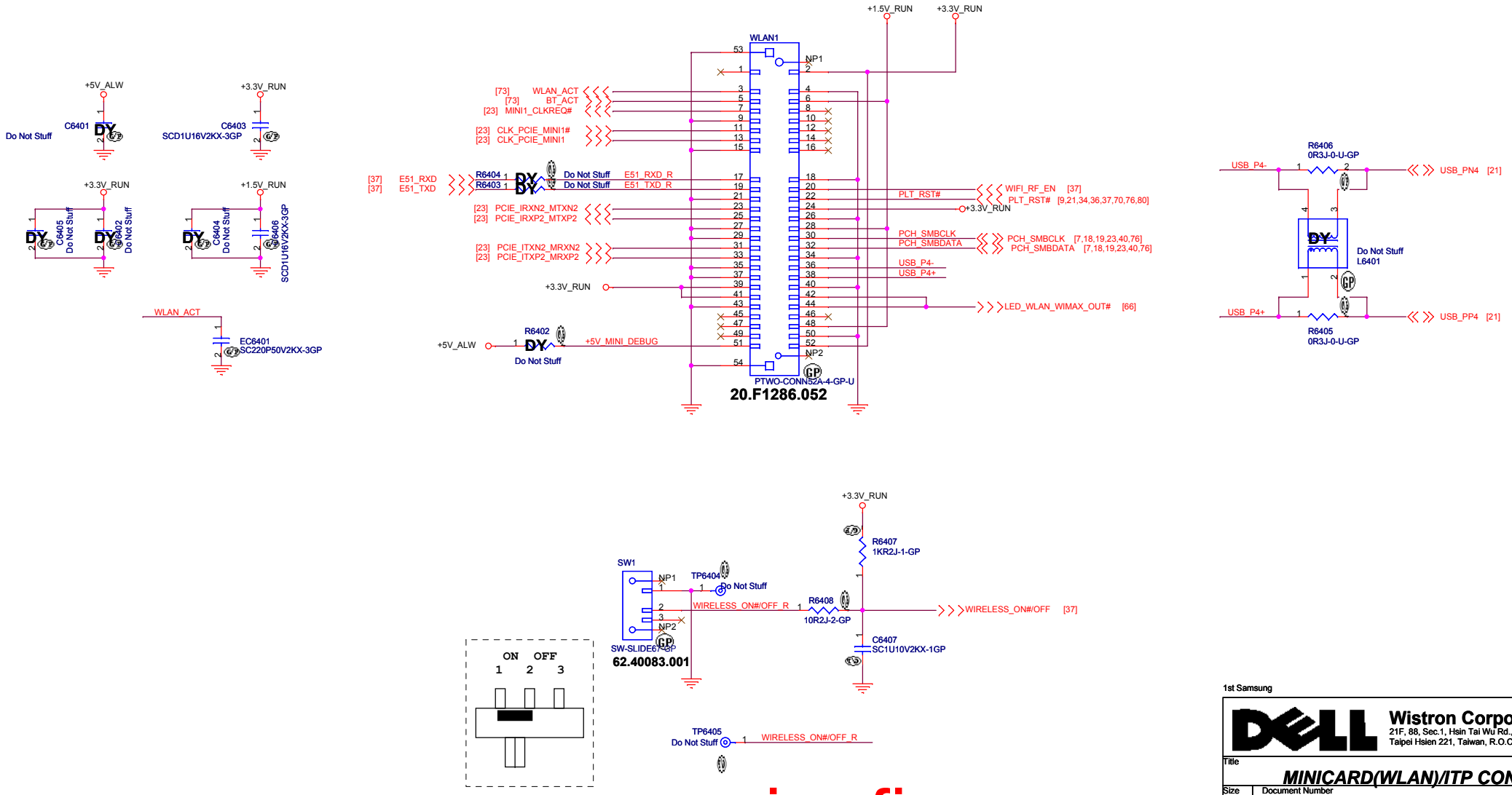
Title: **USB/ESATA Port**

Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 63 of 88

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/ITP CONN***

Size	Document Number	Rev
A3	*Vostro Calpella*	SA

Date: Wednesday, September 02, 2009 Sheet 64 of 88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

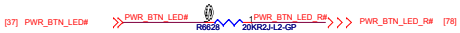
Size: A3 | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 65 of 88

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED



SCRLK LED

CAPS LED

NUM LED

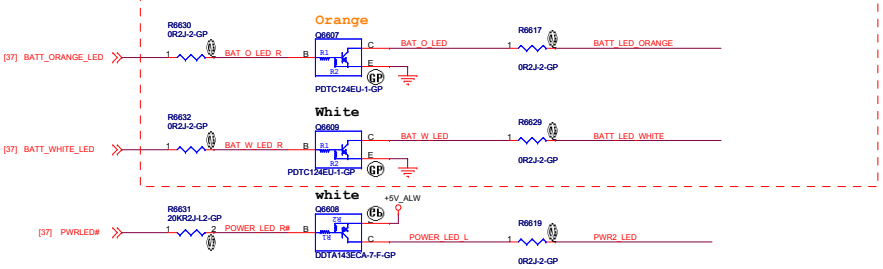
Bluetooth LED

WWAN LED

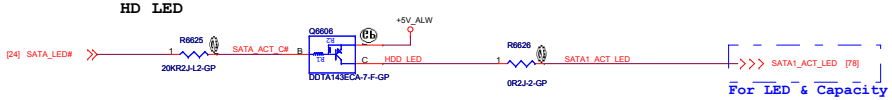
For LED&Capacity board:

WLAN WIMAX_LED

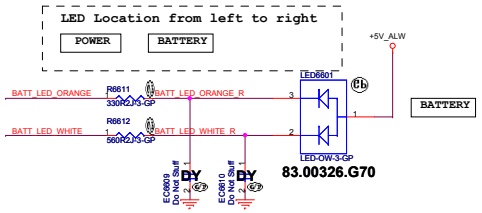
For LED&Capacity board:



HD LED



For LED & Capacity board



Remove HDD LED

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED

Size: Custom | Document Number: Calpella | Rev: SA

Date: Wednesday, November 02, 2011 | Sheet 66 of 88

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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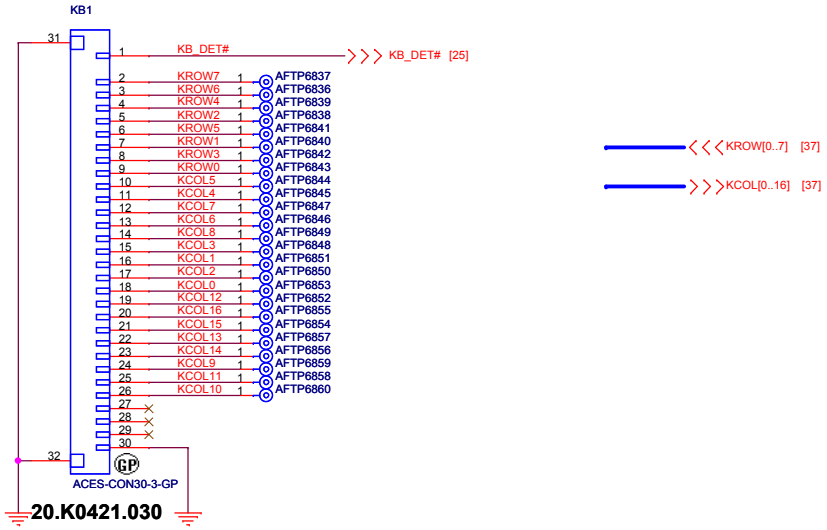
Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 67 of 88

SSID = KBC

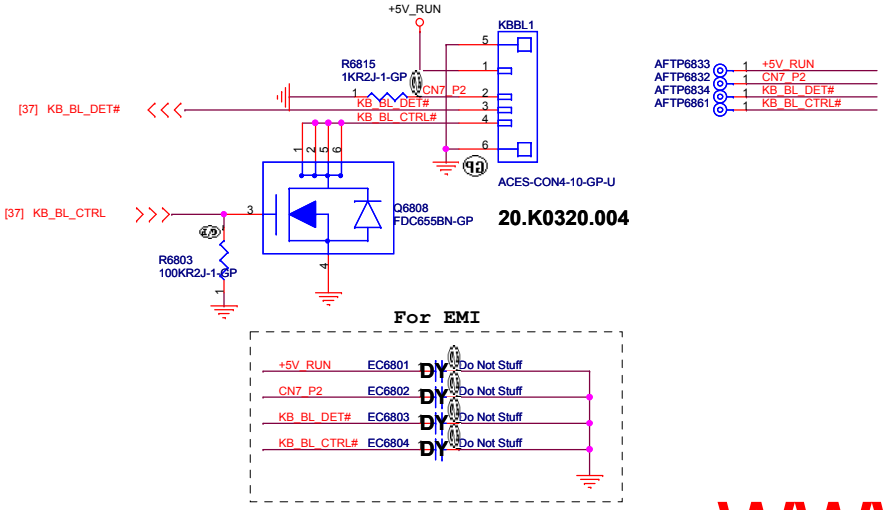
Internal KeyBoard Connector



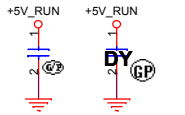
KROW[0..7] [37]

KCOL[0..16] [37]

KB Backlight CONN



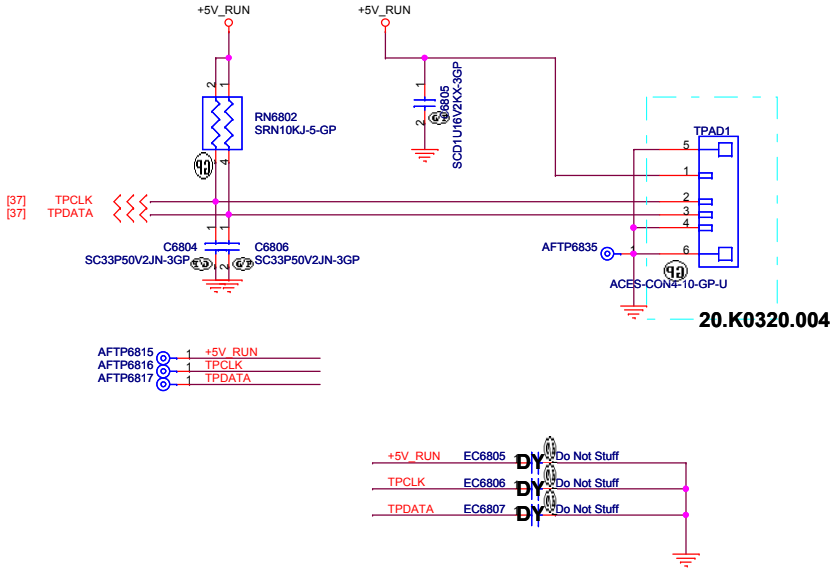
AFTP6833 +5V_RUN
AFTP6832 CN7_P2
AFTP6834 KB_BL_DET#
AFTP6861 KB_BL_CTRL#



Place near CON5

SSID = Touch.Pad

TouchPad Connector



AFTP6815 +5V_RUN
AFTP6816 TPCLK
AFTP6817 TPDATA

+5V_RUN EC6805 Do Not Stuff
TPCLK EC6806 Do Not Stuff
TPDATA EC6807 Do Not Stuff

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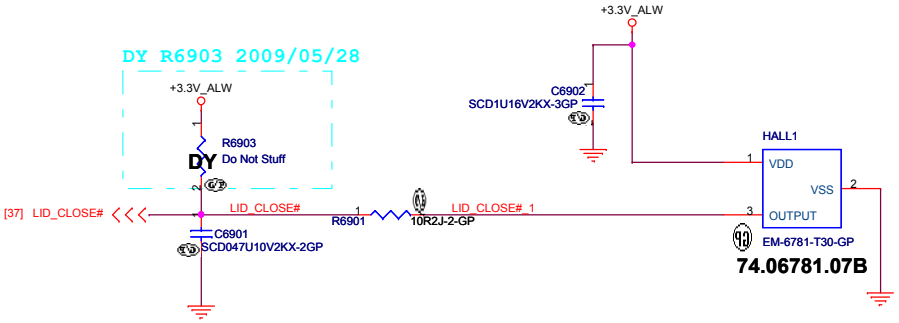
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard/Touch Pad

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 68 of 88

Hall Sensor Connector



1st Samsung

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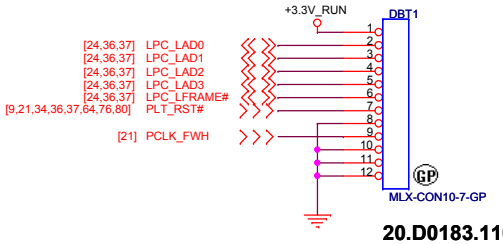
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall sensor***

Size	Document Number	Rev
Custom	***Vostro Calpella***	***SA***

Date: Wednesday, September 02, 2009 Sheet 69 of 88

GOLDEN FINGER FOR DEBUG BOARD



20.D0183.110

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Debug port***		
Size: Custom	Document Number: ***Vostro Calpella***	Rev: ***SA***
Date: Wednesday, September 02, 2009	Sheet 70 of 88	

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *(Reserve)*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 71 of 88

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1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

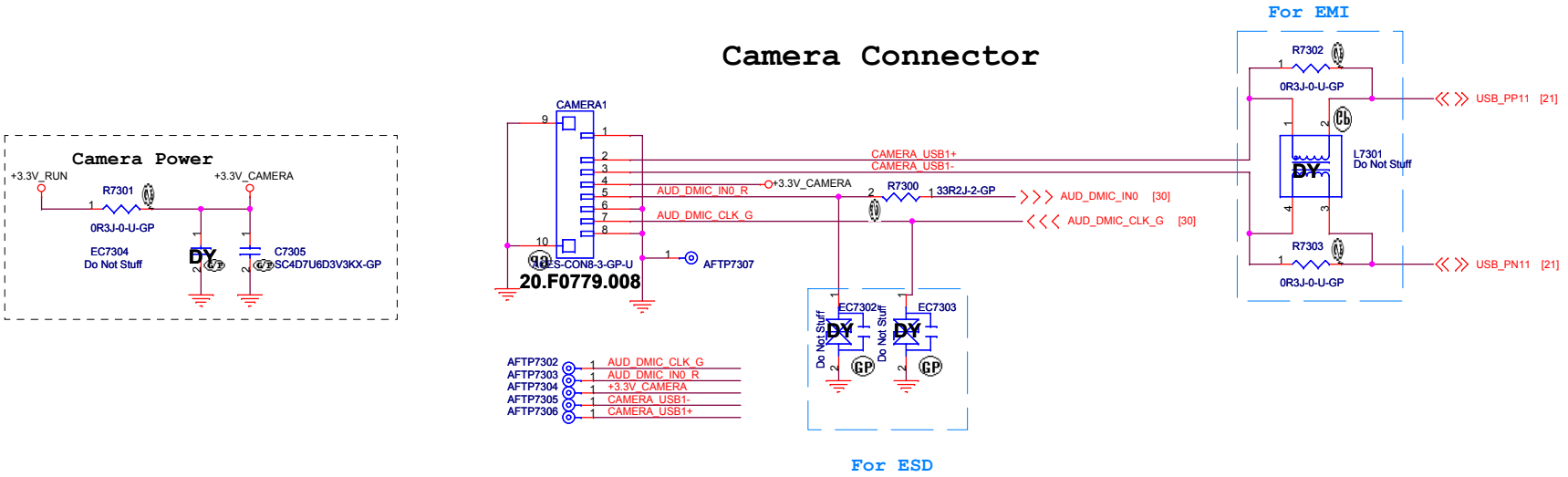
Title: Braidwood

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 72 of 88

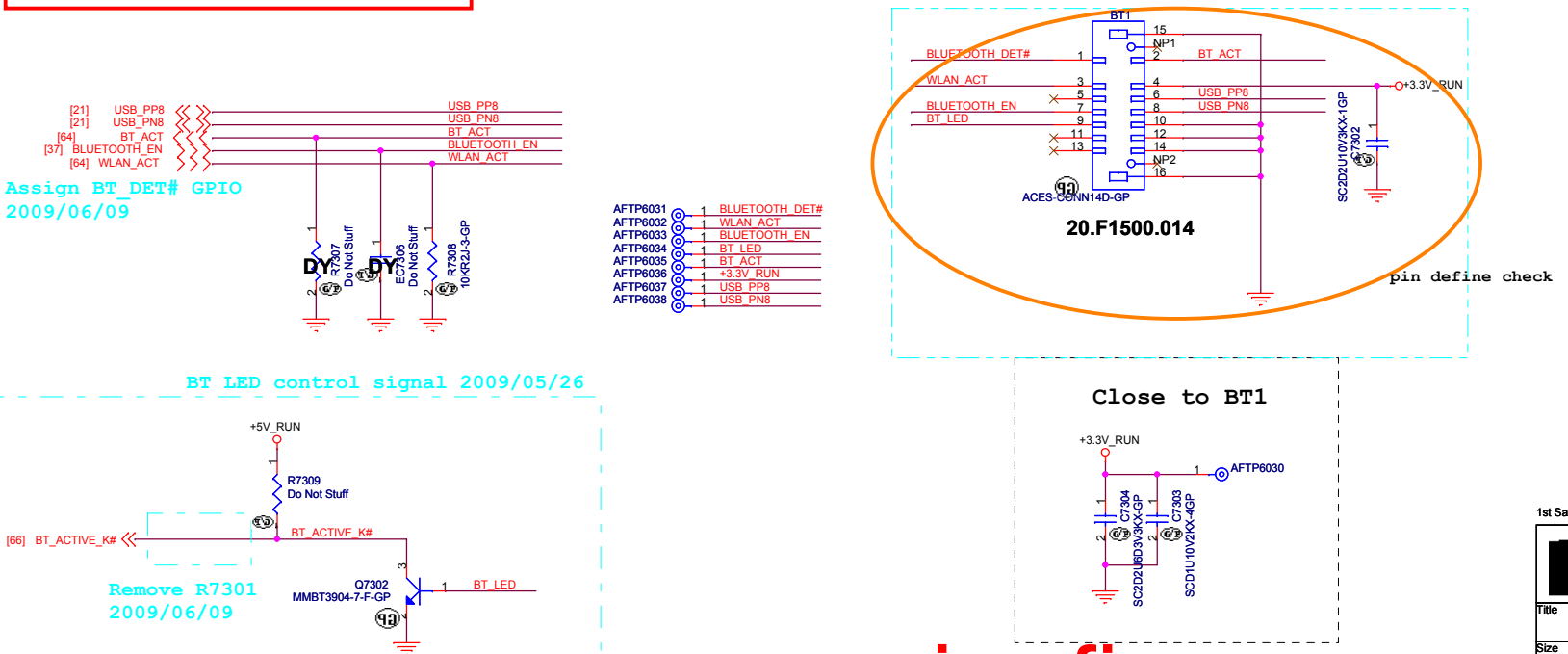
SSID = User.Interface

Camera Connector



SSID = User.Interface

Bluetooth cable conn.



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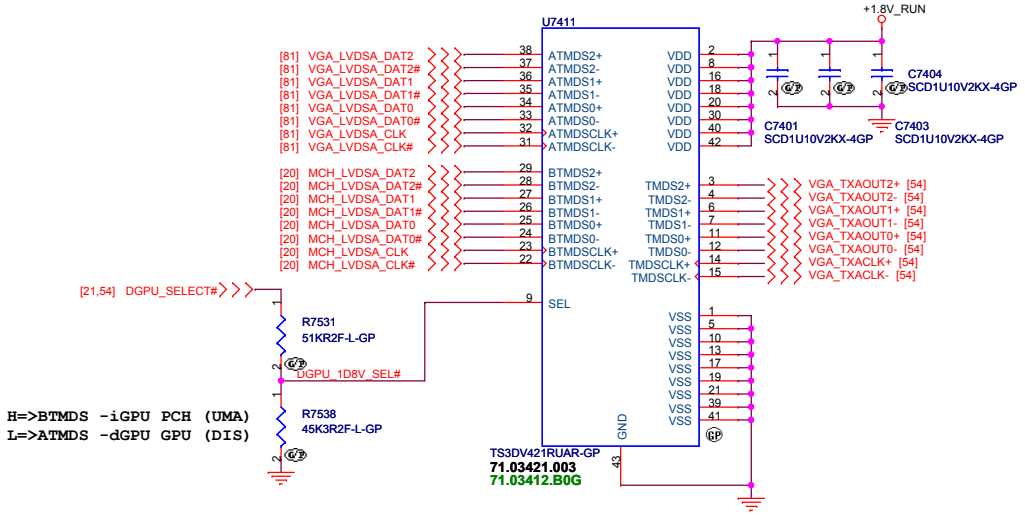
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Camera CONN

Size: A3 | Document Number: Vostro Montevina Discrete | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 73 of 88

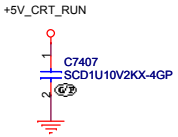
UMA/DIS LVDS signal select circuit



H=>BTMDS -iGPU PCH (UMA)
L=>ATMDS -dGPU GPU (DIS)

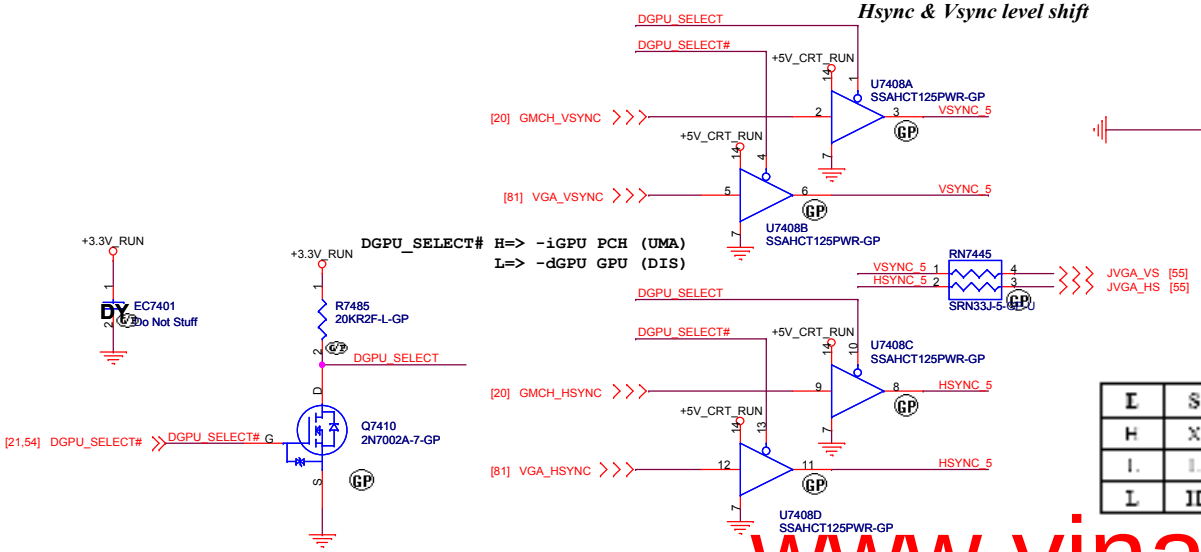
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
	IMDSn = AIMDSn+ TMDSn- = ATMDSn-	
L	IMDSCLK+ = AIMDSCLK+ IMDSCLK- = AIMDSCLK RTMDSn+ = High Impedance BIMDSn- = High Impedance BIMDSCLK+ = High Impedance RTMDSCLK- = High Impedance	IMDSn+ IMDSn- TMDSCLK+ IMDSCLK-
H	TMDSn+ = RTMDSn+ IMDSn- = BIMDSn- IMDSCLK+ = BIMDSCLK+ TMDSCLK- = RTMDSCLK- AIMDSn+ = High Impedance AIMDSn- = High Impedance ATMDSCLK+ = High Impedance AIMDSCLK- = High Impedance	IMDSn+ TMDSn- TMDSCLK+ IMDSCLK-



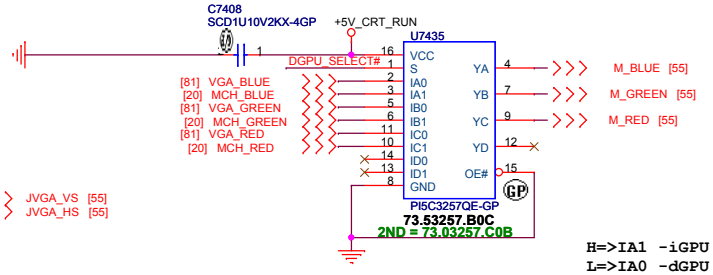
UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



DGPU_SELECT# H=> -iGPU PCH (UMA)
L=> -dGPU GPU (DIS)

UMA/DIS CRT signal select circuit



H=>IA1 -iGPU PCH (UMA)
L=>IA0 -dGPU GPU (DIS)

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PX Swith-1

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 74 of 88

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *(Reserve)*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

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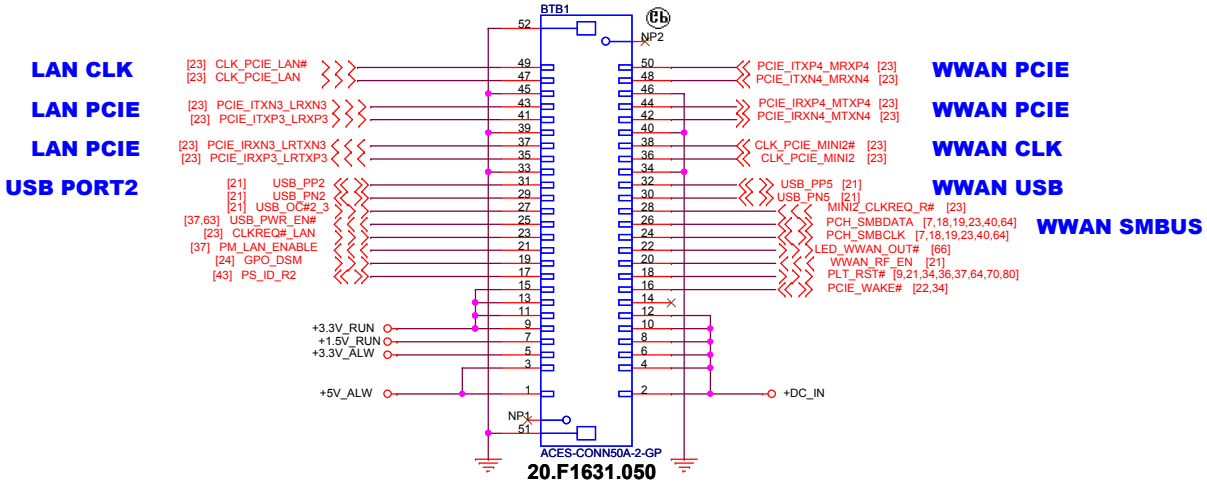
DC_IN baord CON

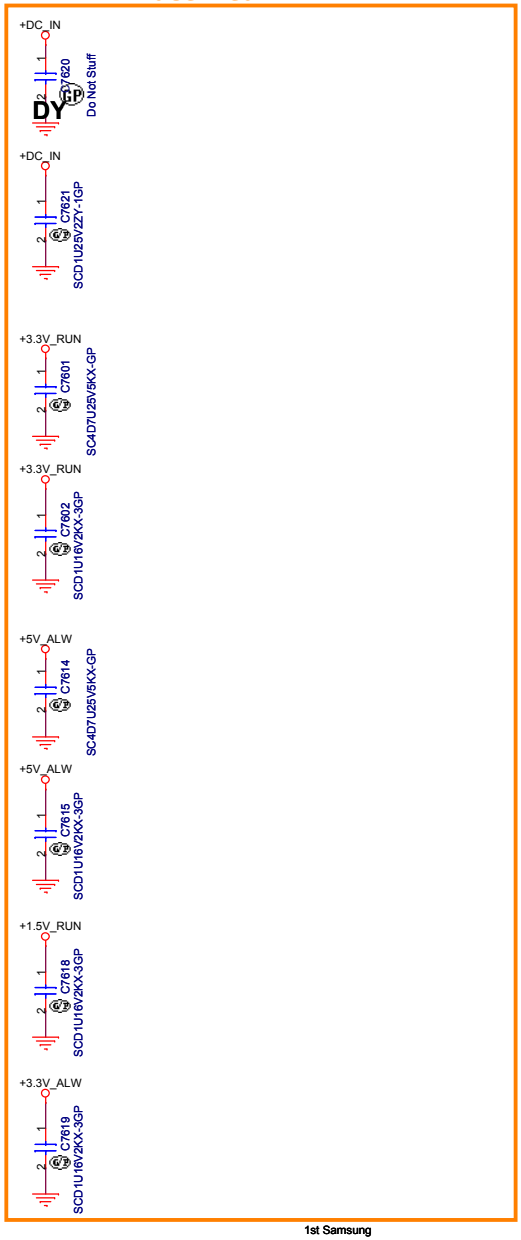
+DC_IN	:	19.5V/85W
+3.3V_RUN	:	3300mA
+5V_ALW	:	1000mA
+1.5V_RUN	:	500mA
+3.3V_ALW	:	58mA

Please reoute 300 mil at least.



Remove AFTP test point
Confirmed with AFTE.

Place near BTB1



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC_IN Board BTB Connector

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 76 of 88

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1st Samsung

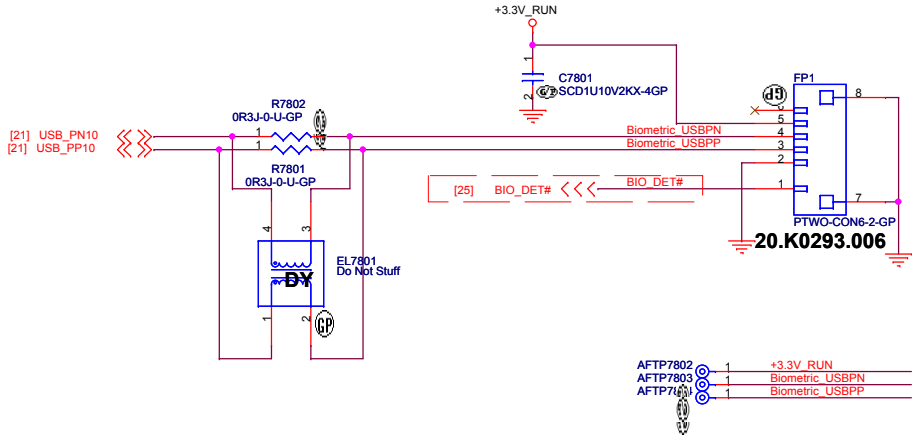
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio BD/IO BD CONN

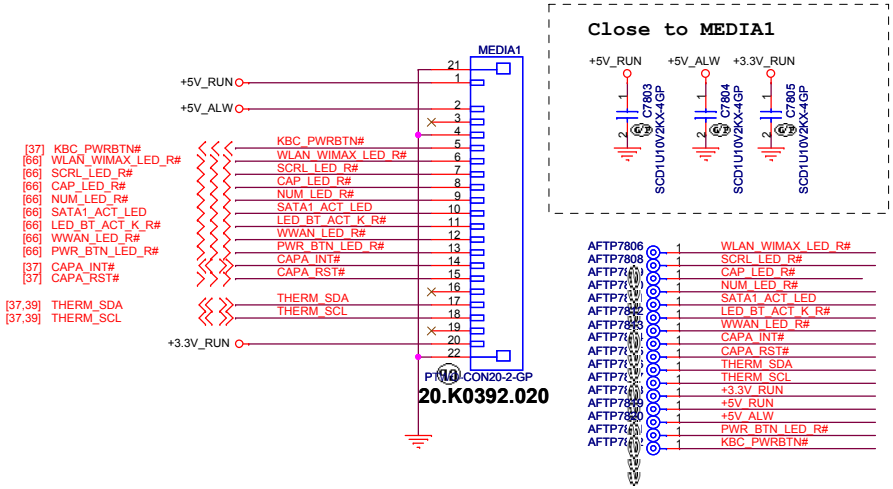
Size: Custom | Document Number: Vostro Montevina Discrete | Rev: SA

Date: Wednesday, September 02, 2009 | Sheet 77 of 88

Finger Printer Connector



LED&Capacity board CONN



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

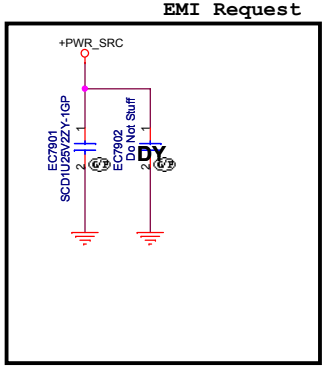
Title: *Finger Printer/Felica/Capacity*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Wednesday, September 02, 2009 | Sheet 78 of 88

SSID = Mechanical

EMI Request



HOLE:

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H6 Do Not Stuff — Do Not Stuff
H7 Do Not Stuff — Do Not Stuff
H8 Do Not Stuff — Do Not Stuff
H10 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff
H14 Do Not Stuff — Do Not Stuff
H5 Do Not Stuff — Do Not Stuff

FOR CPU HOLE

H11 Do Not Stuff DY — Do Not Stuff
H12 Do Not Stuff DY — Do Not Stuff
H13 Do Not Stuff DY — Do Not Stuff

FOR FAN BOSS

H4 STF296R138H83-GP — 34.4A908.001

FOR BT BOSS

H9 STF237R115H123-GP — 34.4A902.001

SPR1 SPRING-24-GP — 34.45T31.001
SPR2 SPRING-24-GP — 34.45T31.001
SPR3 SPRING-24-GP — 34.45T31.001
SPR4 SPRING-31-GP — 34.49U24.001
SPR5 SPRING-6-GP — 34.13B01.001

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Miscellaneous Components
Size: Custom | Document Number: Vostro Calpella | Rev: SA
Date: Wednesday, September 02, 2009 | Sheet 79 of 88

SSID = VIDEO

PCIE_MTX_GRX_P[0..15] → PCIE_MTX_GRX_P[0..15] [8]
PCIE_MTX_GRX_N[0..15] → PCIE_MTX_GRX_N[0..15] [8]
PCIE_MRX_GTX_P[0..15] → PCIE_MRX_GTX_P[0..15] [8]
PCIE_MRX_GTX_N[0..15] → PCIE_MRX_GTX_N[0..15] [8]

U8001B 2 OF 7

PCIE_MTX_GRX_P0	AE12	PEX_RX0	PEX_TX0	AD10	PCIE_MRX_GTX_C_P0	C8033
PCIE_MTX_GRX_N0	AF12	PEX_RX0#	PEX_TX0#	AD11	PCIE_MRX_GTX_C_N0	C8034
PCIE_MTX_GRX_P1	AG12	PEX_RX1	PEX_TX1	AD12	PCIE_MRX_GTX_C_P1	C8035
PCIE_MTX_GRX_N1	AG13	PEX_RX1#	PEX_TX1#	AC12	PCIE_MRX_GTX_C_N1	C8036
PCIE_MTX_GRX_P2	AF13	PEX_RX2	PEX_TX2	AB11	PCIE_MRX_GTX_C_P2	C8037
PCIE_MTX_GRX_N2	AE13	PEX_RX2#	PEX_TX2#	AB12	PCIE_MRX_GTX_C_N2	C8038
PCIE_MTX_GRX_P3	AE15	PEX_RX3	PEX_TX3	AD13	PCIE_MRX_GTX_C_P3	C8039
PCIE_MTX_GRX_N3	AF15	PEX_RX3#	PEX_TX3#	AD14	PCIE_MRX_GTX_C_N3	C8040
PCIE_MTX_GRX_P4	AG15	PEX_RX4	PEX_TX4	AD15	PCIE_MRX_GTX_C_P4	C8042
PCIE_MTX_GRX_N4	AG16	PEX_RX4#	PEX_TX4#	AC15	PCIE_MRX_GTX_C_N4	C8043
PCIE_MTX_GRX_P5	AF16	PEX_RX5	PEX_TX5	AB14	PCIE_MRX_GTX_C_P5	C8044
PCIE_MTX_GRX_N5	AE16	PEX_RX5#	PEX_TX5#	AB15	PCIE_MRX_GTX_C_N5	C8045
PCIE_MTX_GRX_P6	AE18	PEX_RX6	PEX_TX6	AC16	PCIE_MRX_GTX_C_P6	C8047
PCIE_MTX_GRX_N6	AF18	PEX_RX6#	PEX_TX6#	AD16	PCIE_MRX_GTX_C_N6	C8048
PCIE_MTX_GRX_P7	AG18	PEX_RX7	PEX_TX7	AD17	PCIE_MRX_GTX_C_P7	C8050
PCIE_MTX_GRX_N7	AG19	PEX_RX7#	PEX_TX7#	AD18	PCIE_MRX_GTX_C_N7	C8051
PCIE_MTX_GRX_P8	AF19	PEX_RX8	PEX_TX8	AC18	PCIE_MRX_GTX_C_P8	C8052
PCIE_MTX_GRX_N8	AE19	PEX_RX8#	PEX_TX8#	AB18	PCIE_MRX_GTX_C_N8	C8053
PCIE_MTX_GRX_P9	AE21	PEX_RX9	PEX_TX9	AB19	PCIE_MRX_GTX_C_P9	C8054
PCIE_MTX_GRX_N9	AF21	PEX_RX9#	PEX_TX9#	AB20	PCIE_MRX_GTX_C_N9	C8055
PCIE_MTX_GRX_P10	AG21	PEX_RX10	PEX_TX10	AD19	PCIE_MRX_GTX_C_P10	C8056
PCIE_MTX_GRX_N10	AG22	PEX_RX10#	PEX_TX10#	AD20	PCIE_MRX_GTX_C_N10	C8057
PCIE_MTX_GRX_P11	AF22	PEX_RX11	PEX_TX11	AD21	PCIE_MRX_GTX_C_P11	C8058
PCIE_MTX_GRX_N11	AE22	PEX_RX11#	PEX_TX11#	AC21	PCIE_MRX_GTX_C_N11	C8077
PCIE_MTX_GRX_P12	AE24	PEX_RX12	PEX_TX12	AB21	PCIE_MRX_GTX_C_P12	C8078
PCIE_MTX_GRX_N12	AF24	PEX_RX12#	PEX_TX12#	AB22	PCIE_MRX_GTX_C_N12	C8079
PCIE_MTX_GRX_P13	AG24	PEX_RX13	PEX_TX13	AC22	PCIE_MRX_GTX_C_P13	C8080
PCIE_MTX_GRX_N13	AF25	PEX_RX13#	PEX_TX13#	AD22	PCIE_MRX_GTX_C_N13	C8081
PCIE_MTX_GRX_P14	AG25	PEX_RX14	PEX_TX14	AD23	PCIE_MRX_GTX_C_P14	C8082
PCIE_MTX_GRX_N14	AG26	PEX_RX14#	PEX_TX14#	AD24	PCIE_MRX_GTX_C_N14	C8083
PCIE_MTX_GRX_P15	AF27	PEX_RX15	PEX_TX15	AE25	PCIE_MRX_GTX_C_P15	C8084
PCIE_MTX_GRX_N15	AE27	PEX_RX15#	PEX_TX15#	AE26	PCIE_MRX_GTX_C_N15	C8085

All C8033–C8085 → SCD1U16V2KX-3GP → PCIE_MRX_GTX_P0 … PCIE_MRX_GTX_N15

PEX_IOVDDQ: AB13, AB16, AB17, AB7, AB8, AB9, AC13, AC7, AD6, AE6, AF6, AG6

PEX_IOVDD: AC9, AD7, AD8, AE7, AG7

PEX_REFCLK / PEX_REFCLK# ← CLK_PCIE_VGA / CLK_PCIE_VGA# [23]

PEX_TSTCLK_OUT / PEX_TSTCLK_OUT# ← PEX_TEST_PLL_CLK_OUT / PEX_TEST_PLL_CLK_OUT# — Do Not Stuff — DY — R8002

PEX_CLKREQ# ← PEX_CLKREQ#
PEX_RST# ← PEX_RST#

PEX_SVDD_3V3 ← +3.3V_RUN_GPU

PEX_TERMP ← PEX_TERMP — R8001 2K49R2F-GP

PEX_PLLVDD ← +PEX_PLLVDD

PLLVDD ← +GPU_PLLVDD

N11M-GE1-S-A2-GP

+1.05V_GFX_PCIE

SC22U6D3V5MX-2GP C8069 | SC10U6D3V5MX-3GP C8074 | SC4D7U6D3V3KX-GP C8064 | SC1U6D3V2KX-GP C8067 | SC1U6D3V2KX-GP C8068 — Place near GPU

SCD1U10V2KX-4GP C8066 | SCD1U10V2KX-4GP C8065 — Place under GPU

Revised decoupling C 2009/05/28

Revised decoupling C 2009/05/28

Place under GPU: SCD1U10V2KX-4GP C8059 | SCD1U10V2KX-4GP C8060

Place near GPU: SC1U6D3V2KX-GP C8063 | SC1U6D3V2KX-GP C8062 | SC4D7U6D3V3KX-GP C8061 | SC10U6D3V5MX-3GP C8073 | SC22U6D3V5MX-2GP C8041

+3.3V_RUN_GPU → R8004 10KR2J-3-GP

Change R8004 resistor value 2009/06/05

DY — R8002 — Do Not Stuff

DW
07/10 NO STUFF
1. R8002 made NO STUFF

Remove 0.01u capacity C8039 2009/05/28

Place under GPU: SCD1U10V2KX-4GP C8049

Change power rail 2009/05/26

[25] DGPU_HOLD_RST# → R8039 0R2J-2-GP → PLT_RST# → PLT_RST_RC

[9,21,34,36,37,64,70,76] PLT_RST# → R8017 100KR2J-1-GP

U8028 74LVC1G08GW-1-GP: B, A, GND, VCC, Y

+3.3V_RUN → PEX_RST# → R8016 100KR2J-1-GP

DY — C8086 — Do Not Stuff

DW
07/10 Change
1. Change U8028 from Operating voltage Range 5 to 3 V . Add
2.Added Pull-down resistors on GPU Reset [PEX_REST#] Pin

+PEX_PLLVDD — PEX_PLLVDD = 120mA — L8011 IND-D1UH-20-GP 100NH 0603 DCR= 0.13 ohm → +1.05V_GFX_PCIE

C8087 SCD1U10V2KX-4GP | C8070 SC1U6D3V2KX-GP | C8046 SC4D7U6D3V3KX-GP

NV suggestion. Place near GPU

Revised decoupling C 2009/05/28

Place under GPU (Pre pin): +GPU_PLLVDD — C8071 SCD1U10V2KX-4GP | C8072 SCD1U10V2KX-4GP

Place near GPU: L8005 IND-100NH-7-GP → +1.05V_GFX_PCIE — C8076 SC1U6D3V2KX-GP | C8075 SC4D7U6D3V3KX-GP

I SP_PLLVDD=45mA

Revised decoupling C 2009/05/28

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)
Size: A3 | Document Number: Vostro Calpella | Rev: SA
Date: Wednesday, September 02, 2009 | Sheet 80 of 88

SSID = VIDEO

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/10 Not Reserve
1. Shorted LBKLT_CTL_GPU,LCDVDD_EN_GPU,PANEL_BKEN_GPU Not Reserve R8134,R8135,R8136.

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[54] LBKLT_CTL_GPU
[54] LCDVDD_EN_GPU
[37] PANEL_BKEN_GPU
[86] PWRCNTL_0
[86] PWRCNTL_1
[37] THERMTRIP_VGA#
[25] DEEPIDLE_WAKE_INT_R#

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19

I2CA_SCL I2CA_SDA → CRT_CLK_DDC [55], CRT_DAT_DDC [55]
I2CB_SCL I2CB_SDA → I2CB_SCL, I2CB_SDA
I2CC_SCL I2CC_SDA → LDDC_CLK [54], LDDC_DATA [54]
I2CH_SCL I2CH_SDA
I2CS_SCL I2CS_SDA

JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST# JTAG_TCK → TP_JTAG_TDI_GPU, TP_JTAG_TDO_GPU, TP_JTAG_TMS_GPU, JTAG_RST# GPU, TP_JTAG_TCK_GPU 1KR2J-1-GP; TP8102, TP8104, TP8101, TP8103 R8120

ROM_SO ROM_SI ROM_SCLK ROM_CS# → ROM_SO_GPU [83], ROM_SI_GPU [83], ROM_SCLK_GPU [83]

XTAL_IN XTAL_OUT XTALBUFF XTAL_SSIN → GPU_XTAL_IN, GPU_XTALOUT, R8114 0R2J-2-GP, R8113 0R2J-2-GP, R8124 10KR2J-3-GP

STRAP_CAL_PU_GND0 STRAP_CAL_PU_GND1 → R8133, R8126 40K2R2F-GP → VGA_THERMDC [39]
THERMDN THERMDP → C8102 Do Not Stuff, R8107 10KR2J-3-GP → VGA_THERMDA [39]
TESTMODE CEC SP_PLLVDD SPDIF BUFRST# → R8127 10KR2J-3-GP → +3.3V_RUN_GPU; +SP_PLLVDD

[74] VGA_BLUE
[74] VGA_GREEN
[74] VGA_RED
[74] VGA_VSYNC
[74] VGA_HSYNC

DACA_BLUE DACA_GREEN DACA_RED DACA_VSYNC DACA_HSYNC DACA_RSET DACA_VDD DACA_VREF

R8116 150R2F-1-GP, R8117 150R2F-1-GP, R8118 150R2F-1-GP, R8119 150R2F-1-GP
R8106 124R2F-U-GP, C8103 SCD1U10V2KX-GP

DACB_BLUE DACB_GREEN DACB_RED DACB_VSYNC DACB_HSYNC DACB_RSET DACB_VDD DACB_VREF

MULTI_STRAP_REF0_GND MULTI_STRAP_REF1_GND

[83] STRAP0
[83] STRAP1
[83] STRAP2

R8111 10KR2F-2-GP

+DACA_VDD = 120mA

Place near GPU
+3.3V_RUN_GPU → L8106 BLM18SG331TN1D-GP → SC470U6D3V2KX-GP, C8153, C8154 SC1U6D3V2KX-GP

Place under GPU
16mil
+DACA_VDD → C8144 SCD1U10V2KX-4GP, C8143 SCD1U10V2KX-4GP, C8118 SCD1U10V2KX-4GP, C8106 SC470P50V2KX-1GP, C8107 SC470P50V2KX-3GP

Spec 300 ohm,
ESR<0.25 ohm

Revised decoupling C 2009/05/28

Added CLK GEN 27M select circuit 2009/06/15
Added R8132 (DY) 2009/06/17

2009/06/03
2009/05/28
2009/06/03

CLK GEN 27M select:

XTAL_IN R8123 DY Do Not Stuff
XTAL_SSIN R8131 DY Do Not Stuff
→ CLK_VGA_27M [7]
R8132 Do Not Stuff DY
R8125 10KR2J-3-GP

Remove R8112,
R8114 2009/06/09

VGA 27M	R8123	R8131	R8125	R8132
SS	DY	POP	DY	POP
NON-SS	POP	DY	POP	DY

Default X'tal

Main 82.30034.651
Second ?

X8101 XTAL-27MHZ-84-GP
GPU_XTAL_IN, GPU_XTALOUT
R8115 1MR2J-1-GP
C8135 SC10P50V2JN-4GP, C8138 SC10P50V2JN-4GP

+3.3V_RUN_GPU → RN8112 SRN2K2J-1-GP → I2CB_SCL, I2CB_SDA

Place near GPU
+SP_PLLVDD → L8110 IND-100NH-7-GP → +1.05V_GFX_PCIE
SC1U6D3V2KX-GP, C8120 SC470U6D3V9MX-GP
I SP_PLLVDD=45mA

Revised decoupling C 2009/05/28

U8001C 3 OF 7

[74] VGA_LVDSA_CLK
[74] VGA_LVDSA_CLK#
[74] VGA_LVDSA_DAT0
[74] VGA_LVDSA_DAT0#
[74] VGA_LVDSA_DAT1
[74] VGA_LVDSA_DAT1#
[74] VGA_LVDSA_DAT2
[74] VGA_LVDSA_DAT2#

IFPA_TXC IFPA_TXC# IFPA_TXD0 IFPA_TXD0# IFPA_TXD1 IFPA_TXD1# IFPA_TXD2 IFPA_TXD2# IFPA_TXD3 IFPA_TXD3# IFPA_IOVDD IFPA_PLLVDD IFPA_RSET

R8121 DY Do Not Stuff 2009/05/28

IFPB_TXC IFPB_TXC# IFPB_TXD4 IFPB_TXD4# IFPB_TXD5 IFPB_TXD5# IFPB_TXD6 IFPB_TXD6# IFPB_TXD7 IFPB_TXD7# IFPB_IOVDD

IFPD_L0 IFPD_L0# IFPD_L1 IFPD_L1# IFPD_L2 IFPD_L2# IFPD_L3 IFPD_L3# IFPD_PLLVDD IFPD_RSET IFPD_AUX_I2CX_SCL IFPD_AUX_I2CX_SDA# IFPDE_IOVDD

R8128 10KR2J-3-GP
R8129 10KR2J-3-GP

IFPE_L0 IFPE_L0# IFPE_L1 IFPE_L1# IFPE_L2 IFPE_L2# IFPE_L3 IFPE_L3# IFPE_PLLVDD IFPE_RSET IFPE_AUX_I2CY_SCL IFPE_AUX_I2CY_SDA#

R8130 10KR2J-3-GP

DW30 LVDS only 1 chanel
Vendor confirm tie to +1.8V powe rail

DW30 not support HDMI
NV DG: pull-down 10K

IFPC_L0 IFPC_L0# IFPC_L1 IFPC_L1# IFPC_L2 IFPC_L2# IFPC_L3 IFPC_L3# IFPC_IOVDD IFPC_PLLVDD IFPC_RSET IFPC_AUX_I2CW_SCL IFPC_AUX_I2CW_SDA#

R8135 10KR2J-3-GP
R8134 10KR2J-3-GP

N11M-GE1-S-A2-GP

Unused IFP
Interfaces setting
2009/06/03

+IFPAB_IOVDD

+1.8V_RUN_GPU → L8107 BLM18PG181SN1D-GP
IFPAB_IOVDD = 300mA
C8126 SC470U6D3V9MX-GP, C8149 SC1U6D3V2KX-GP
Place near GPU

+IFPAB_IOVDD → C8150 SCD1U10V2KX-4GP
Place under GPU
near IFPA_IOVDD

+IFPAB_IOVDD → C8151 SCD1U10V2KX-4GP
Place under GPU
near IFPB_IOVDD

Revised decoupling C 2009/05/28

+IFPAB_PLLVDD

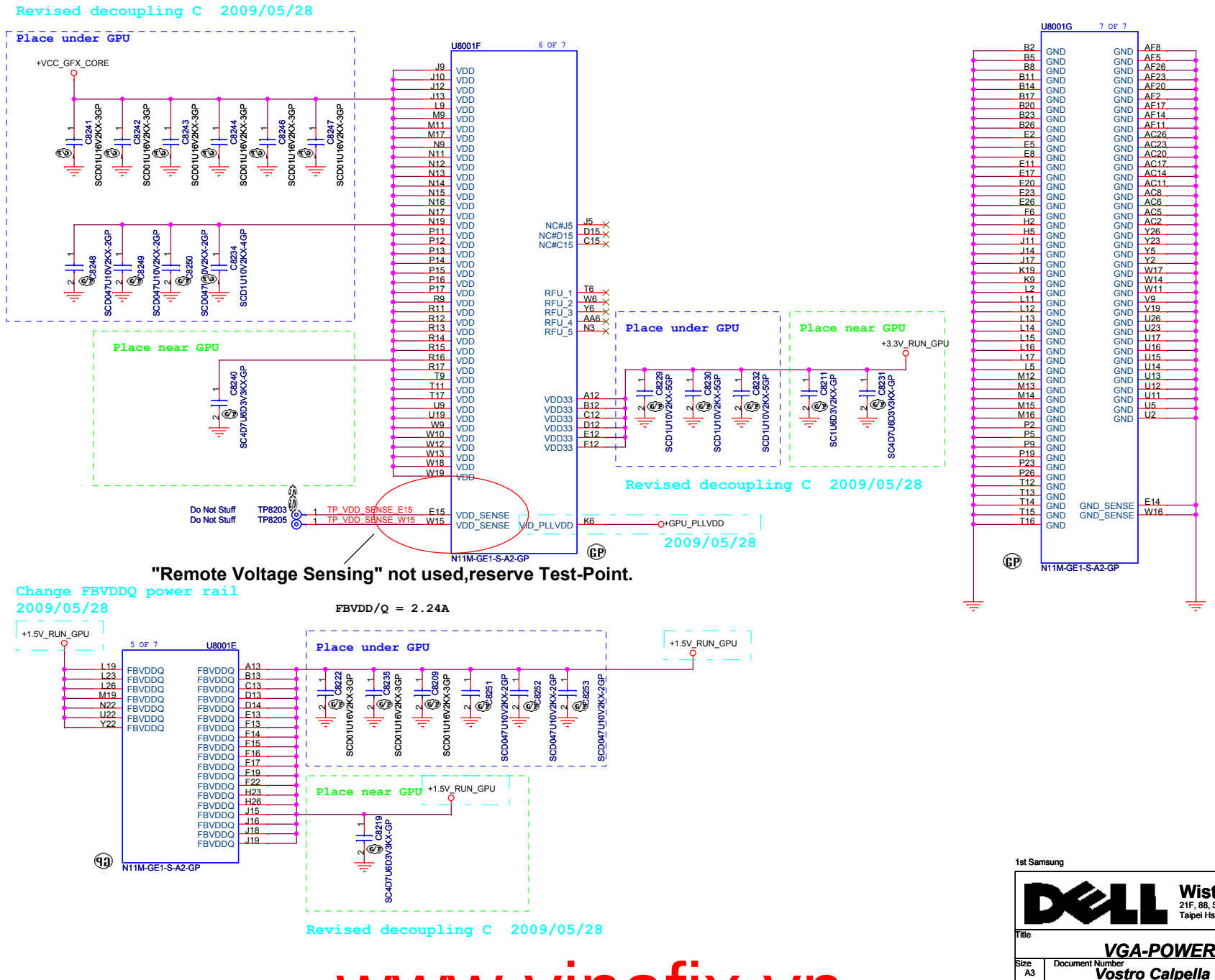
Revised decoupling C 2009/05/28
Change power rail 2009/05/28
+1.05V_GFX_PCIE → L8108 BLM18PG181SN1D-GP
IFPAB_PLLVDD = 220mA
C8128 SC470U6D3V9MX-GP, C8152 SC1U6D3V2KX-GP
Place near GPU
→ +IFPAB_PLLVDD

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-LVDS/CRT/DP PORT
Size: A2 | Document Number: Vostro Calpella | Rev: SA
Date: Wednesday, September 02, 2009 | Sheet 81 of 88

SSID = VIDEO



1st Samsung

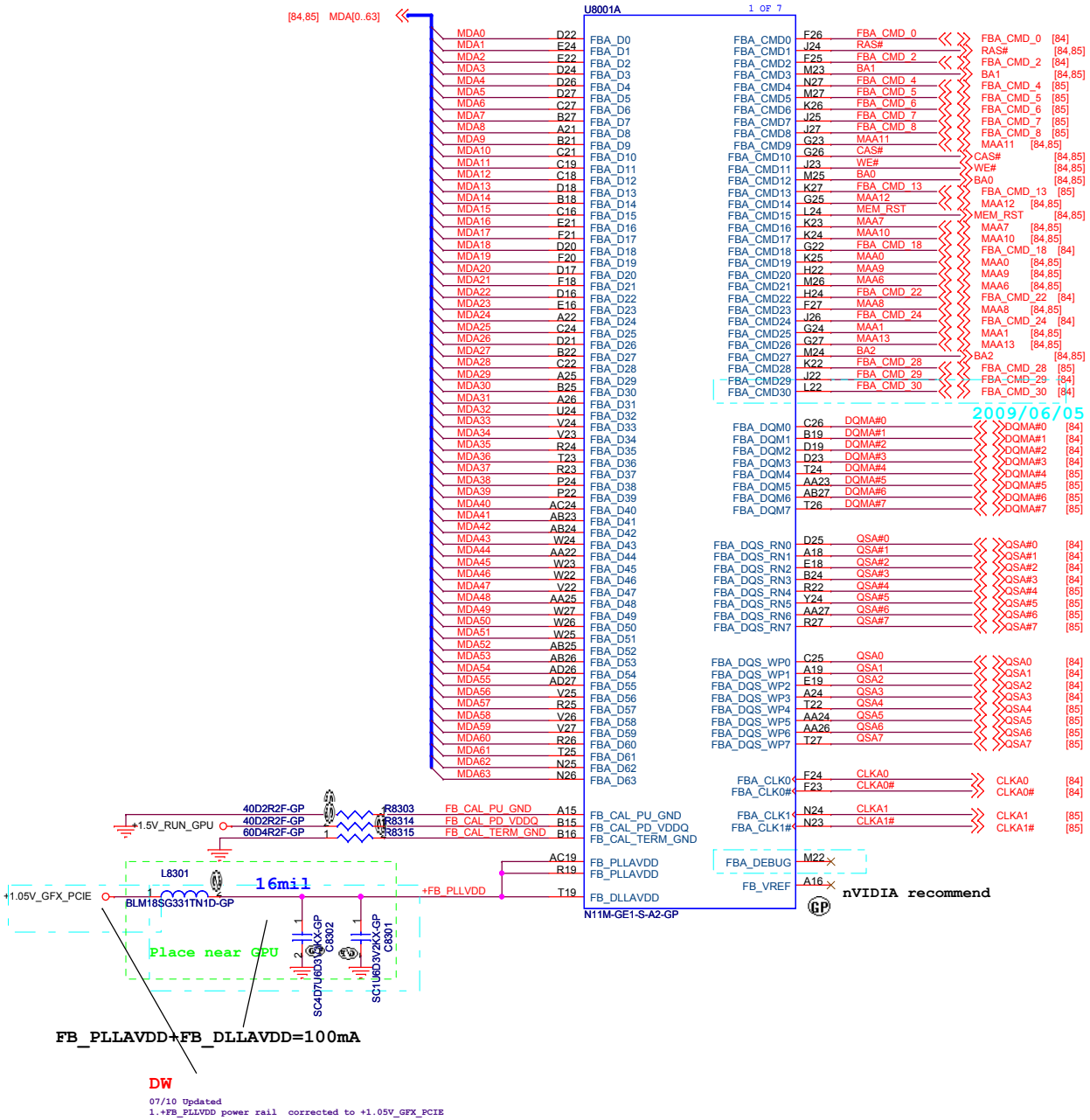
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Wednesday, September 02, 2009 Sheet 82 of 88

SSID = VIDEO

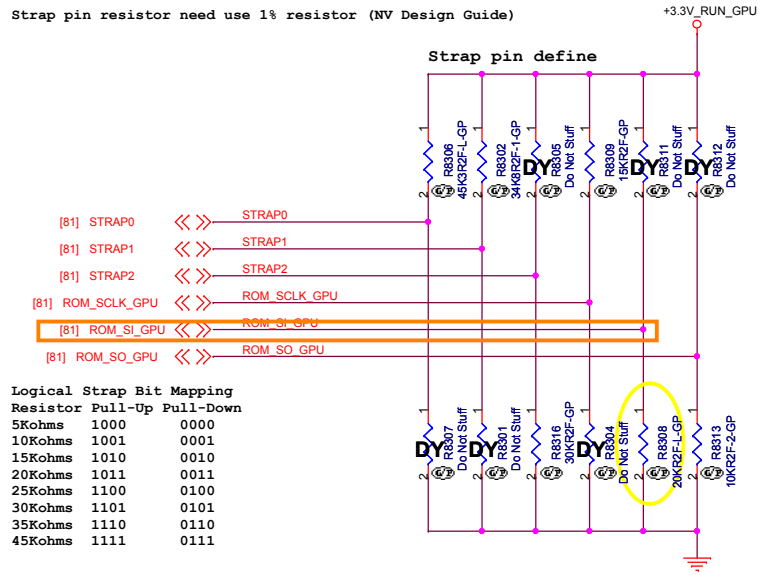


FB_PLLAVDD+FB_DLLAVDD=100mA

DW

07/10 Updated
1.+FB_PLLVDD power rail corrected to +1.05V_GFX_PCIE

Strap pin resistor need use 1% resistor (NV Design Guide)



Logical Strap Bit Mapping

Resistor	Pull-Up	Pull-Down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Strap0		Strap1		Strap2	
USER_BIT0	1	3GIO_PADCFG_LUT_ADR0	0	PCI_DEVID_0	1
USER_BIT1	1	3GIO_PADCFG_LUT_ADR1	1	PCI_DEVID_1	0
USER_BIT2	1	3GIO_PADCFG_LUT_ADR2	1	PCI_DEVID_2	1
USER_BIT3	1	3GIO_PADCFG_LUT_ADR3	1	PCI_DEVID_3	0
EDID is used		Reserved		N11M-GE1 GPU Device ID=0x0A75	
ROM_SI_GPU		**ROM_SO_GPU**		**ROM_SCLK_GPU**	
RAM_CFG0		VGA_DEVICE	1	PEX_PLL_EN_TERM	0
RAM_CFG1		SMB_ALT_ADDR	0	SLOT_CLK_CONFIG	1
RAM_CFG2		FB_0_BAR_SIZE	0	SUB_VENDOR	0
RAM_CFG3		XCLK_417	0	PCI_DEVID_4	1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)
If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K.

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000			
0001			
0010	64MX16	DDR3 64Bit	Hynix
0011	64MX16	DDR3 64Bit	Samsung
0100			Default
0101			
0110			
0111			

SUB_VENDOR	XCLK_417	PEX_PLL_EN_TERM
0 No VBIOS ROM	0 277MHz(POR)	0 Disable (POR)
1 BIOS ROM present	1 Reserved	1 Enable

3GIO_PADCFG USER[3:0]
0000 Desktop 1111 Use EDID to detect panel settings
1110 Notebook (POR)

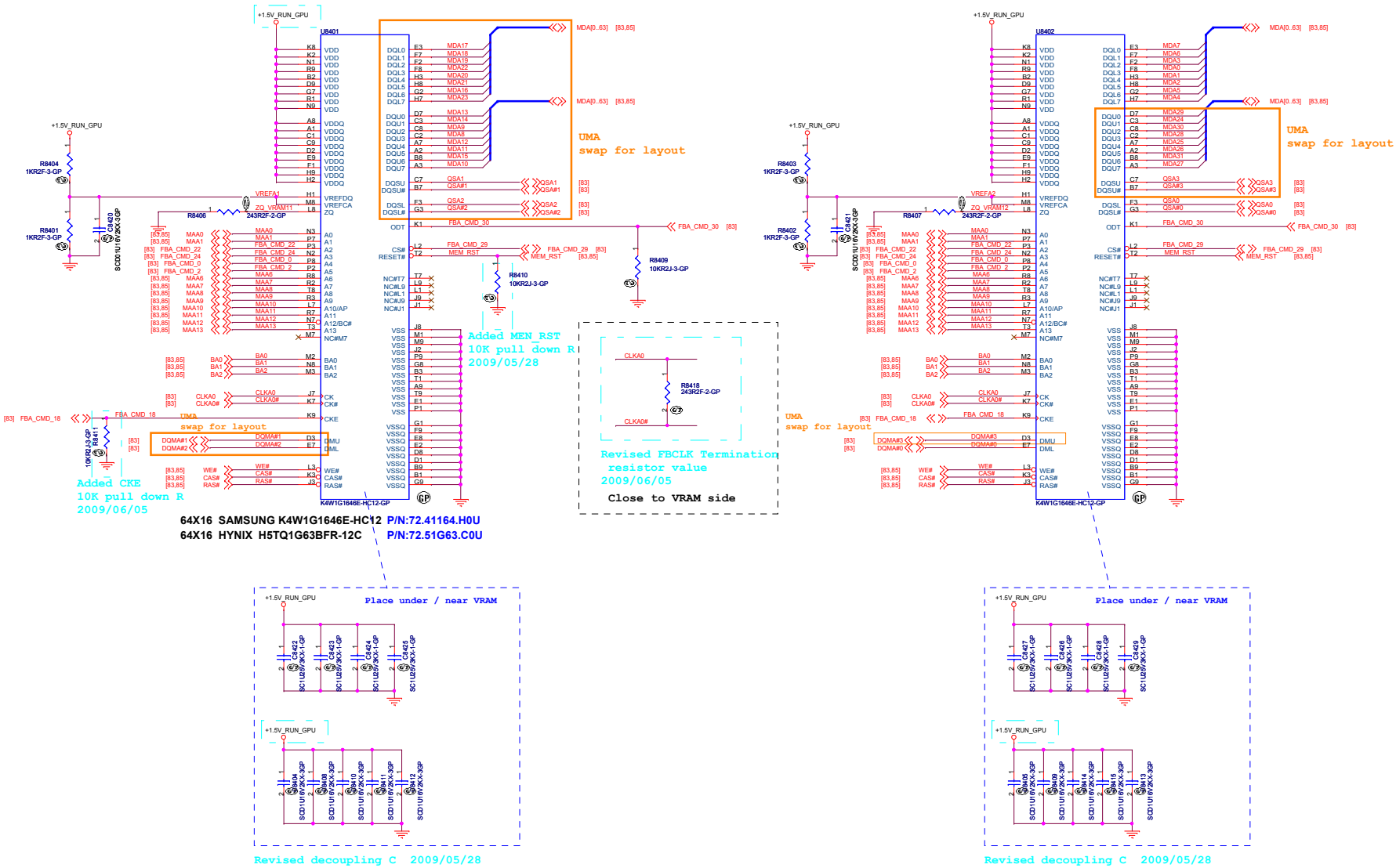
SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-MEMORY/STRAPS(4/4)
Size: A3 | Document Number: Vostro Calpella | Rev: SA
Date: Wednesday, September 02, 2009 | Sheet 83 of 88

SSID = VIDEO



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Title: VRAM(1/2)

Size	Document Number	Rev
A2	Vostro Calpella	SA

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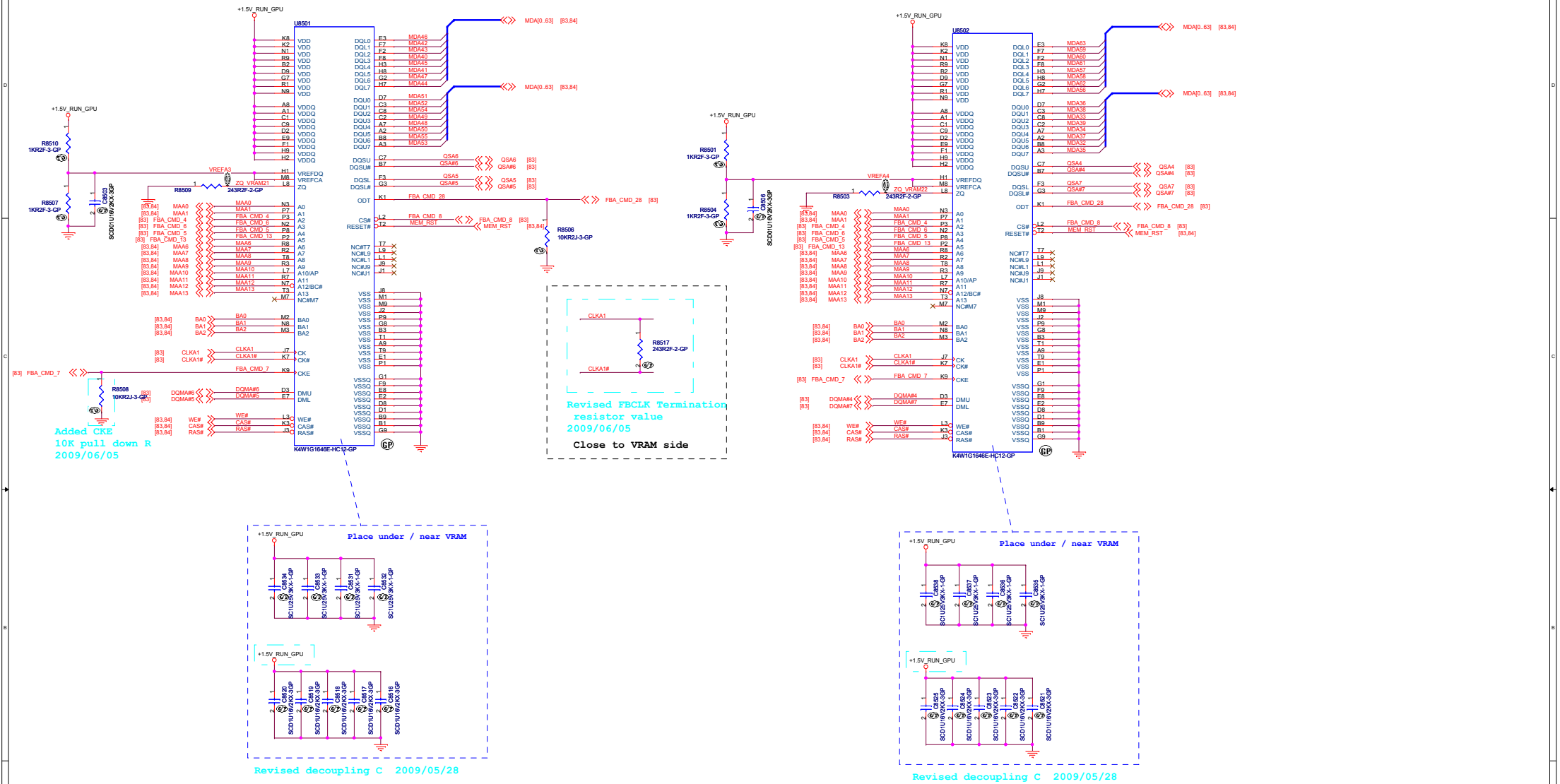
SSID = VIDEO



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Title: VRAM

Size	Document Number	Rev
A2	Vostro Calpella	SA

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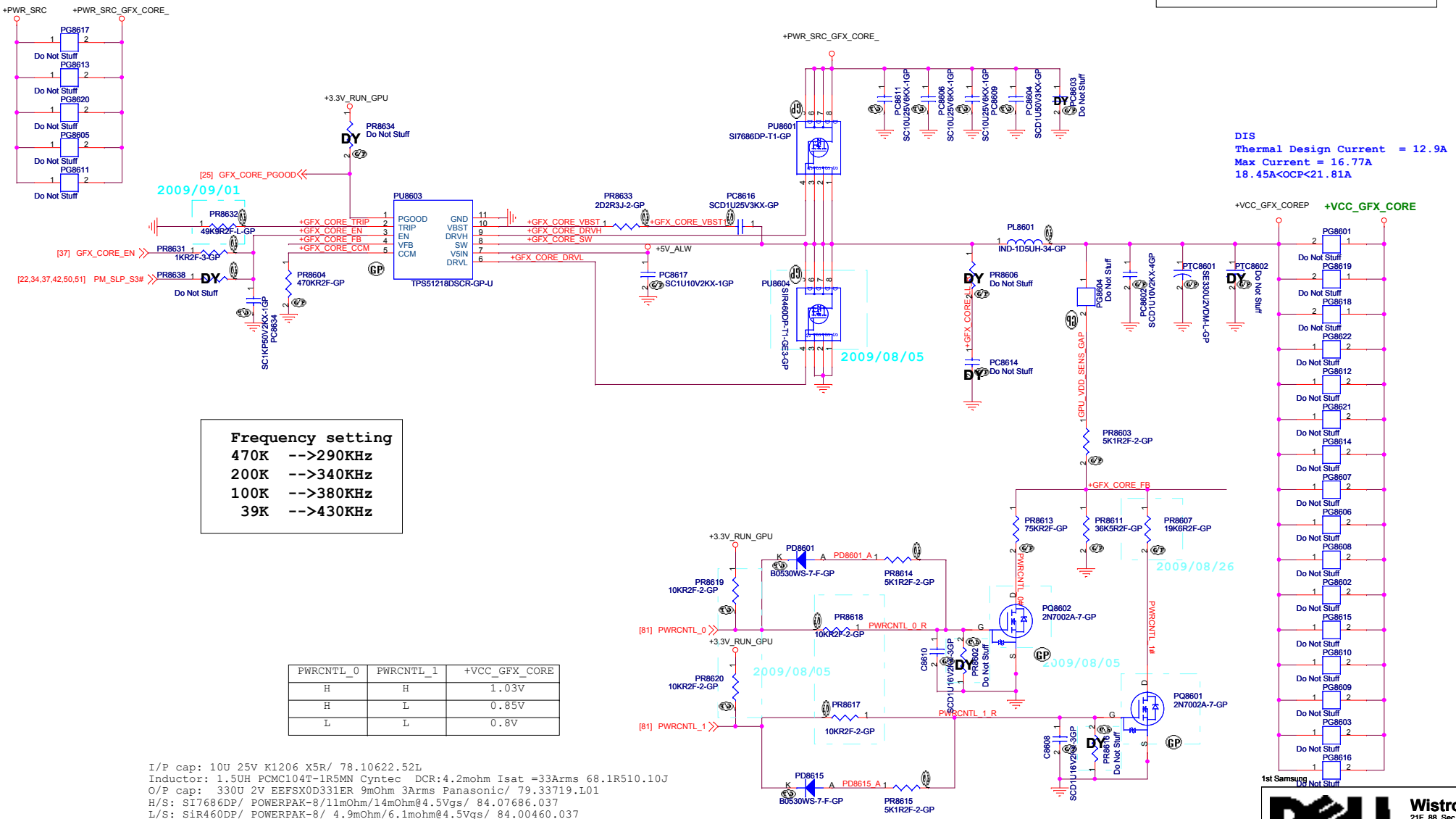
SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



Frequency setting

470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V
L	L	0.8V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

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Title: TPS51218 +VCC_GFX_CORE

Size	Document Number	Rev
Custom	DW Calpella (Discrete)	X00

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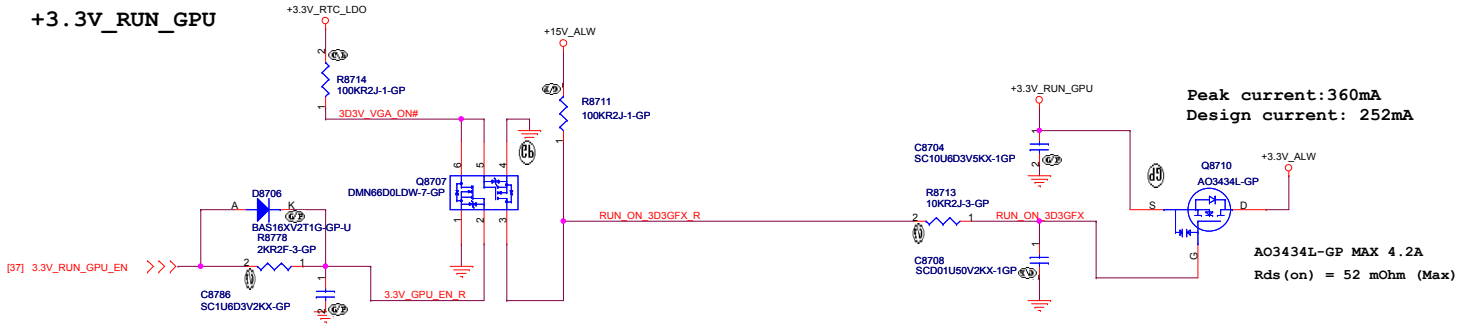
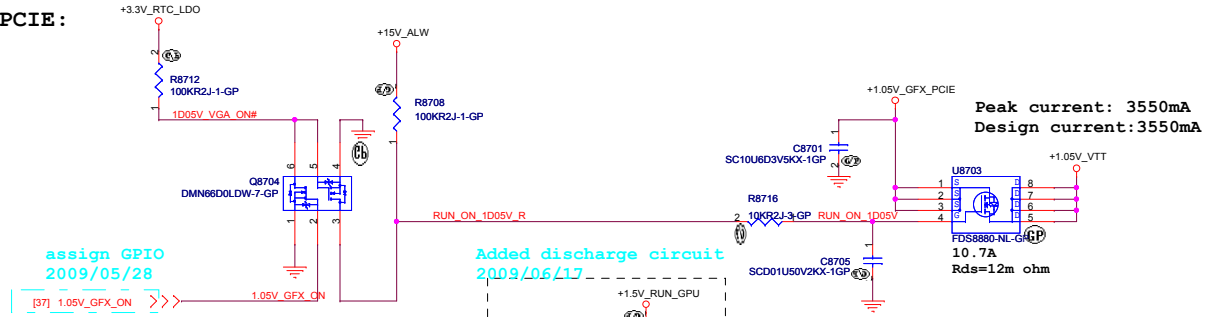
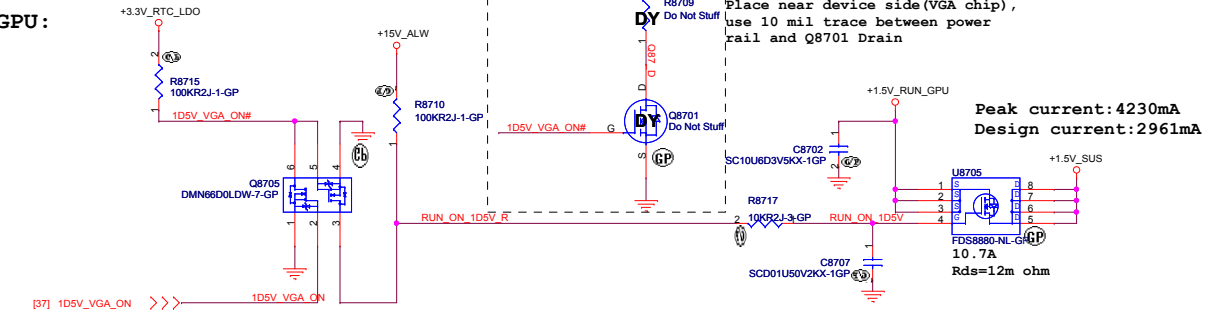
+3.3V_RUN_GPU



+1.05V_GFX_PCIE:



+1.5V_RUN_GPU:



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Title: LDO 1.8V

Size	Document Number	Rev
Custom	Vostro Calpella	SA

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.

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Title: ***Change List(1/3)***

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

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