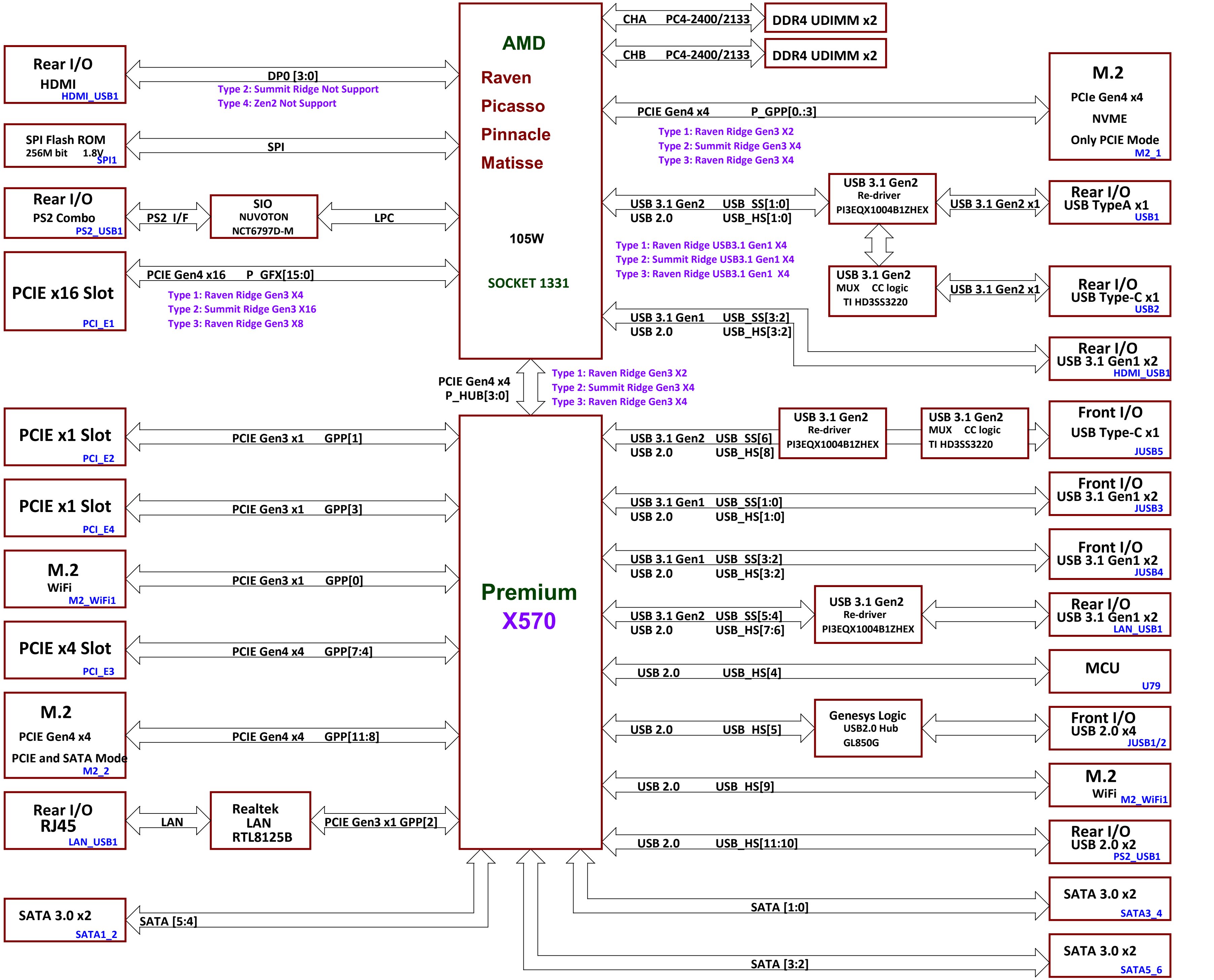
AMD AM4

GAMING EDGE AC

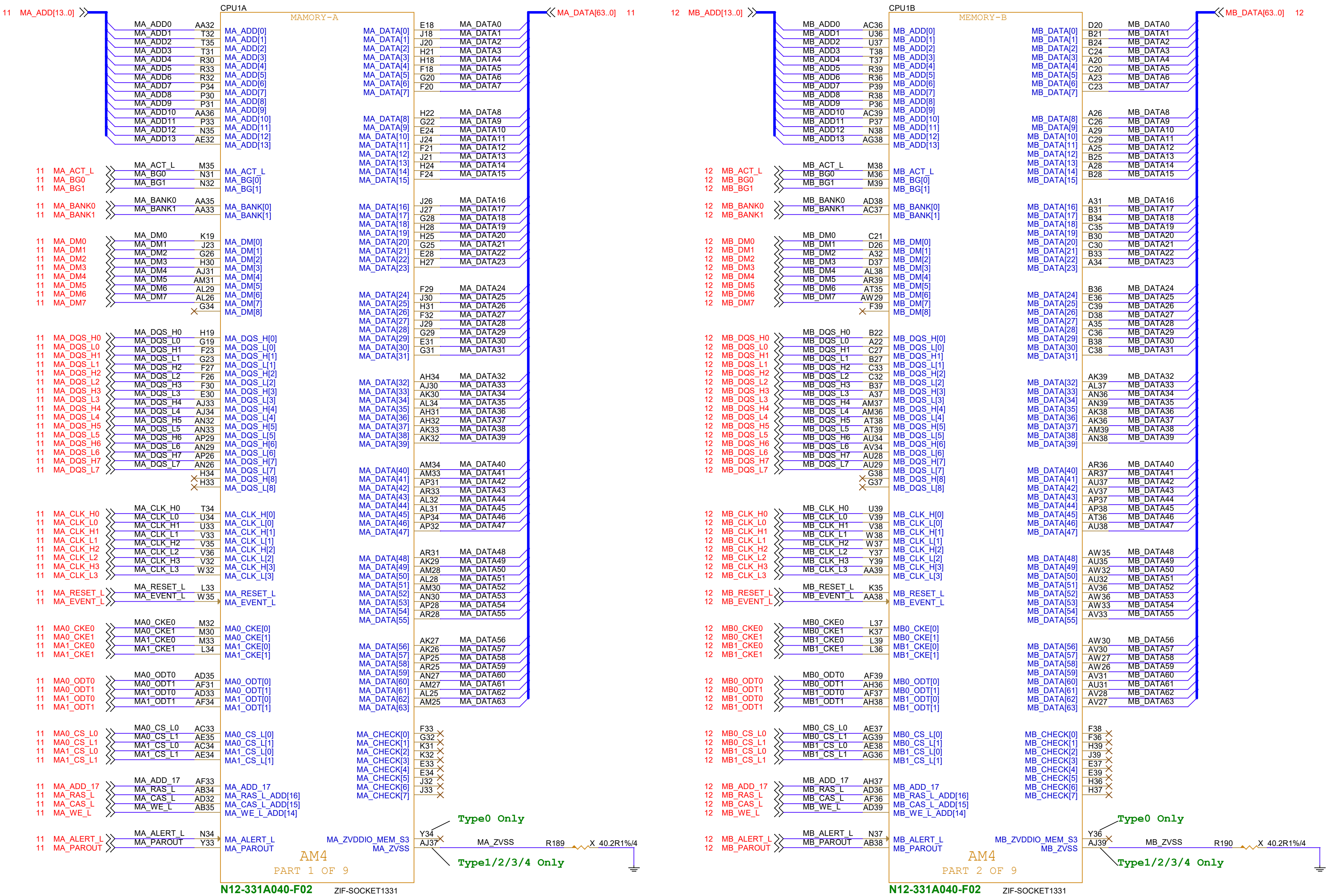


MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	Block Diagram	11

Date: Friday, June 04, 2021 Sheet 2 of 73

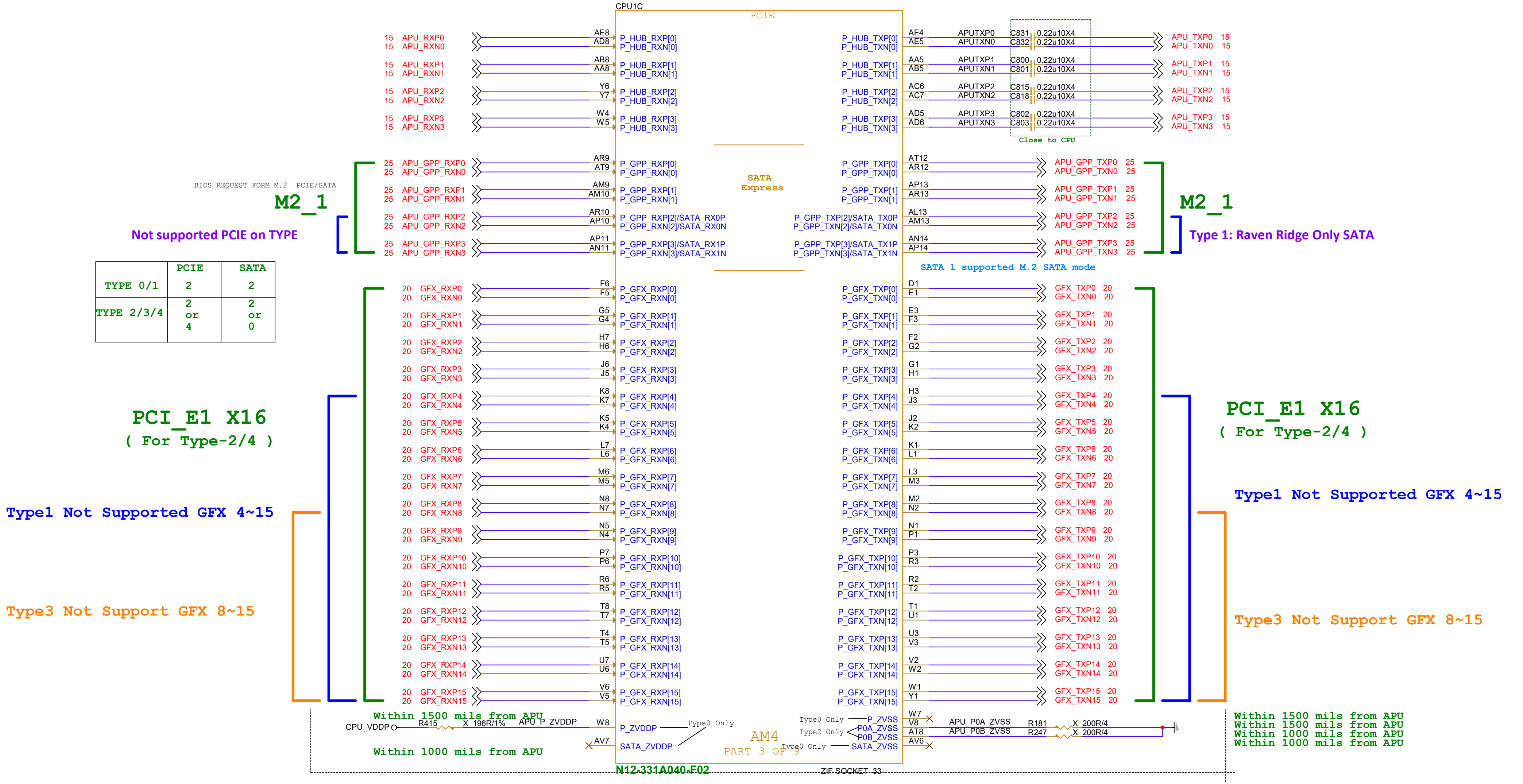


MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	AM4 DDR4 I/F	11

Date Friday June 04 2021 Sheet 3 of 73



	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

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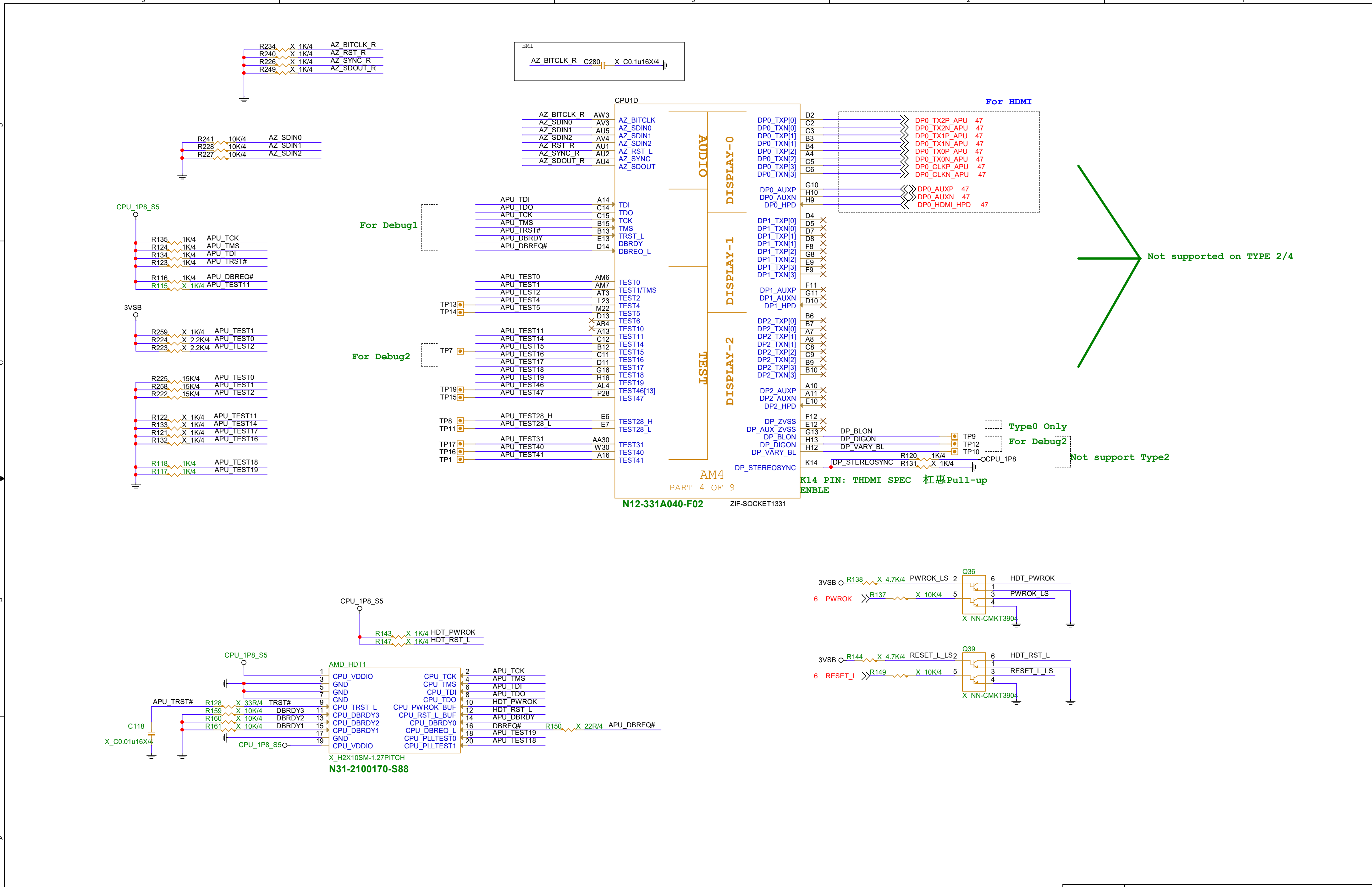
MS-7D54

Size: Custom

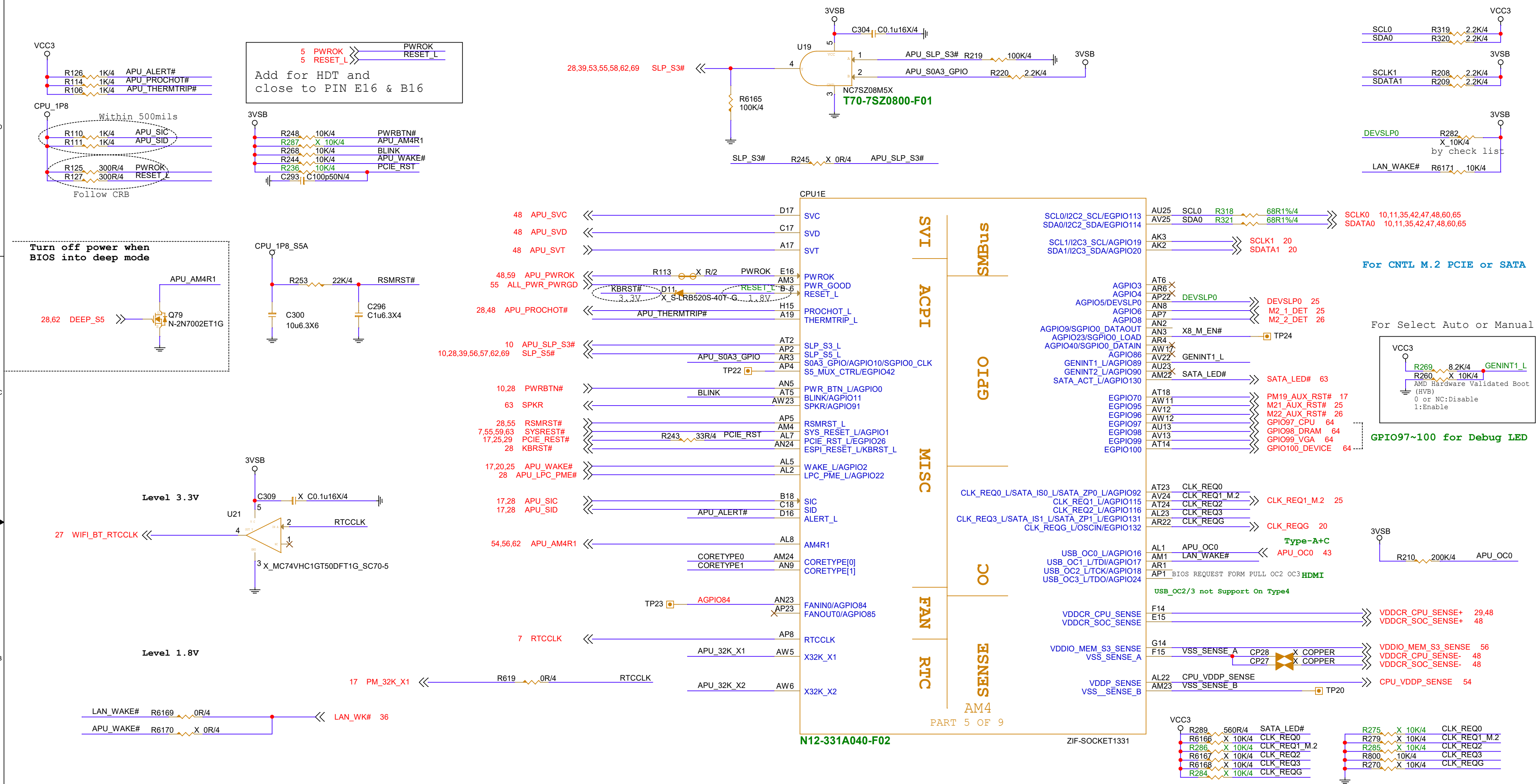
Document Description: AM4 PCIE / SATAE

Rev: 11

Date: Friday, June 04, 2021



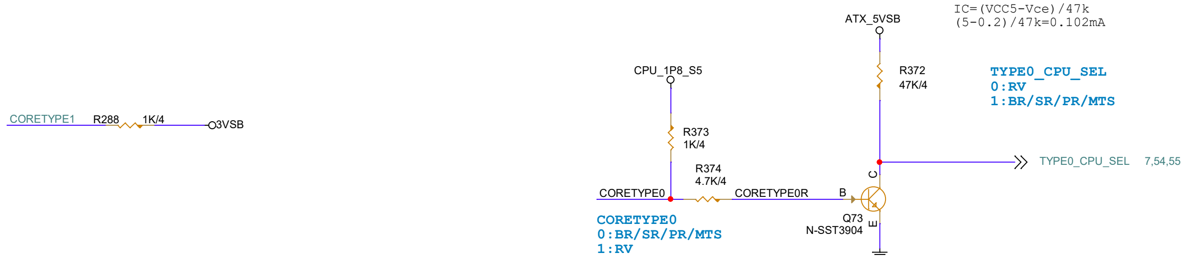
MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: AM4 Display / Audio	Rev: 11
Date: Friday, June 04, 2021	Sheet 5 of 73	



AM4 CPU TYPE Circuit

IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA

IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA



TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS

CORETYPE0
0:BR/SR/PR/MTS
1:RV

SPEC no Support

CPU	TYPE	CORETYPE 1	CORETYPE 0
~~BR~~	~~0~~	~~0~~	~~0~~
NA		0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1

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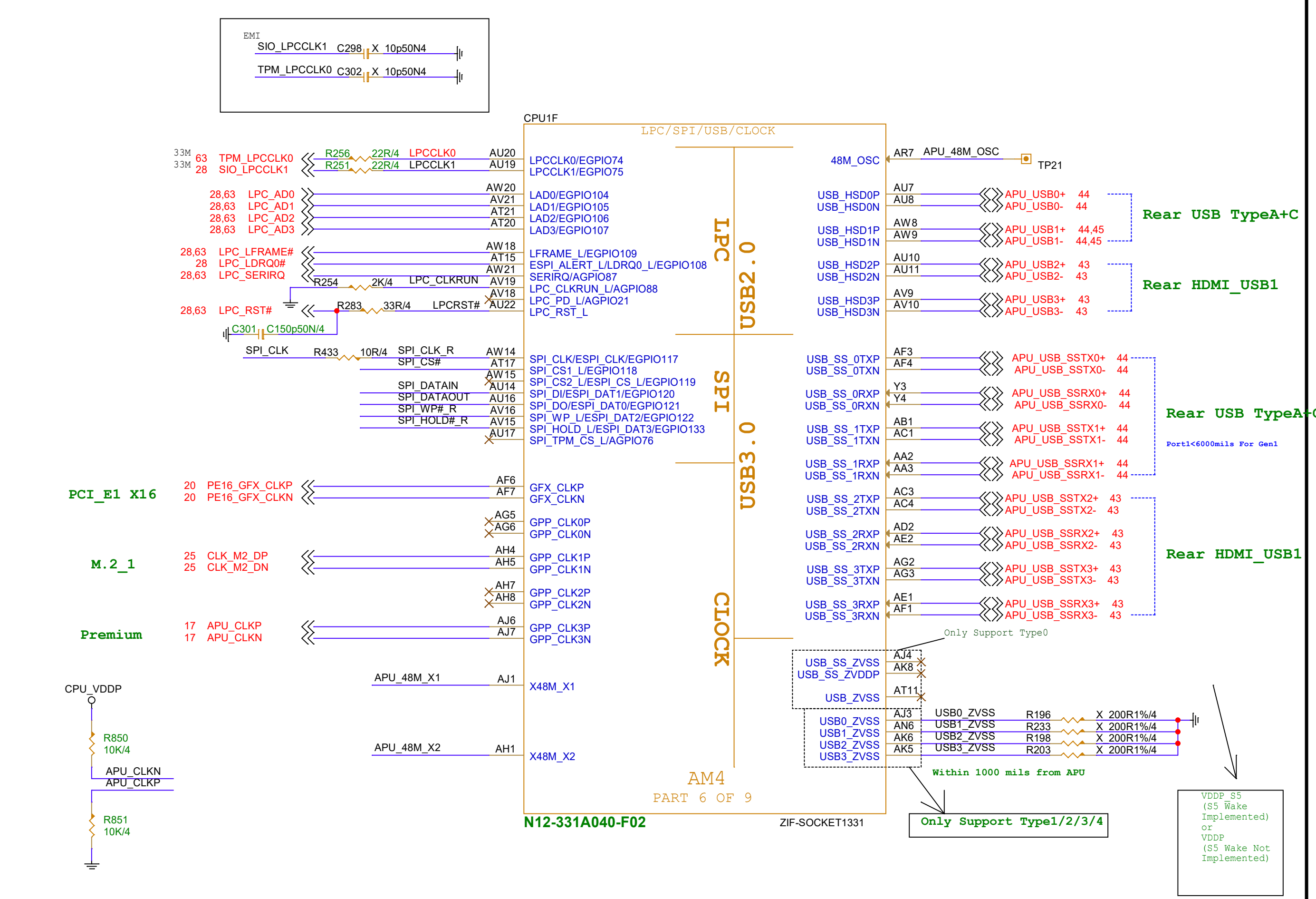
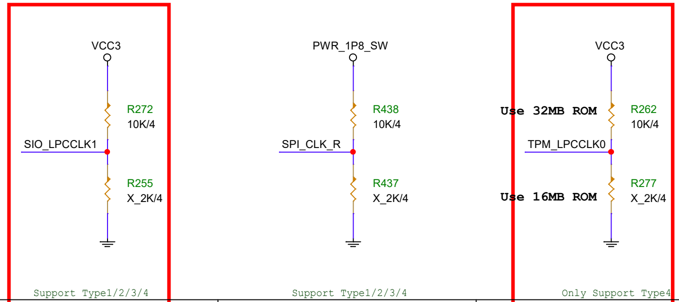
MS-7D54

Size: Custom | Document Description: AM4 SVI / ACPI / GPIO | Rev: 11

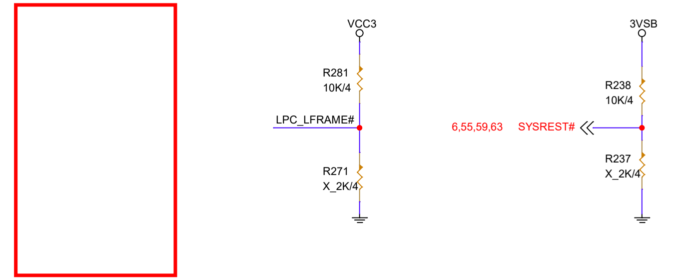
Date: Friday, June 04, 2021 | Sheet 6 of 73



Strapping Options



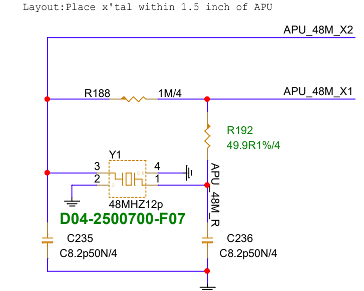
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]



VDDP_S5 (S5 Wake Implemented) or VDDP (S5 Wake Not Implemented)

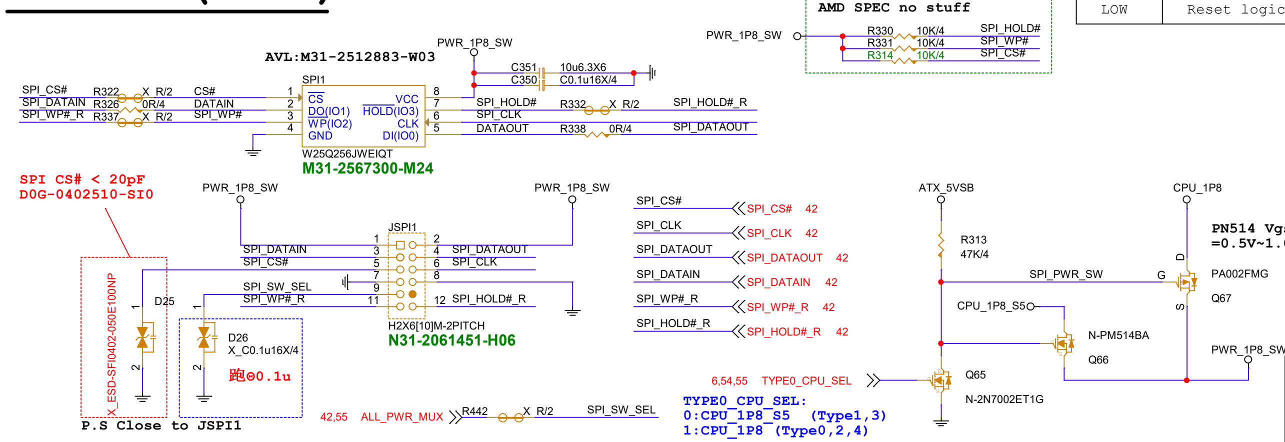
	AGPIO3 (Only Support Type0)	LFRAME (Support Type1/2/3/4)	SYSREST# (Support Type1/2/3/4)
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

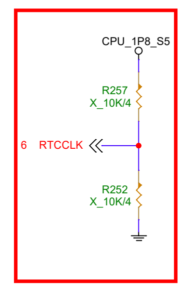
Layout:Place x'tal within 1.5 inch of APU



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

SPI ROM(1.8V)





	RTCCLK (Only Support Type4)
PULL HIGH	RTCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

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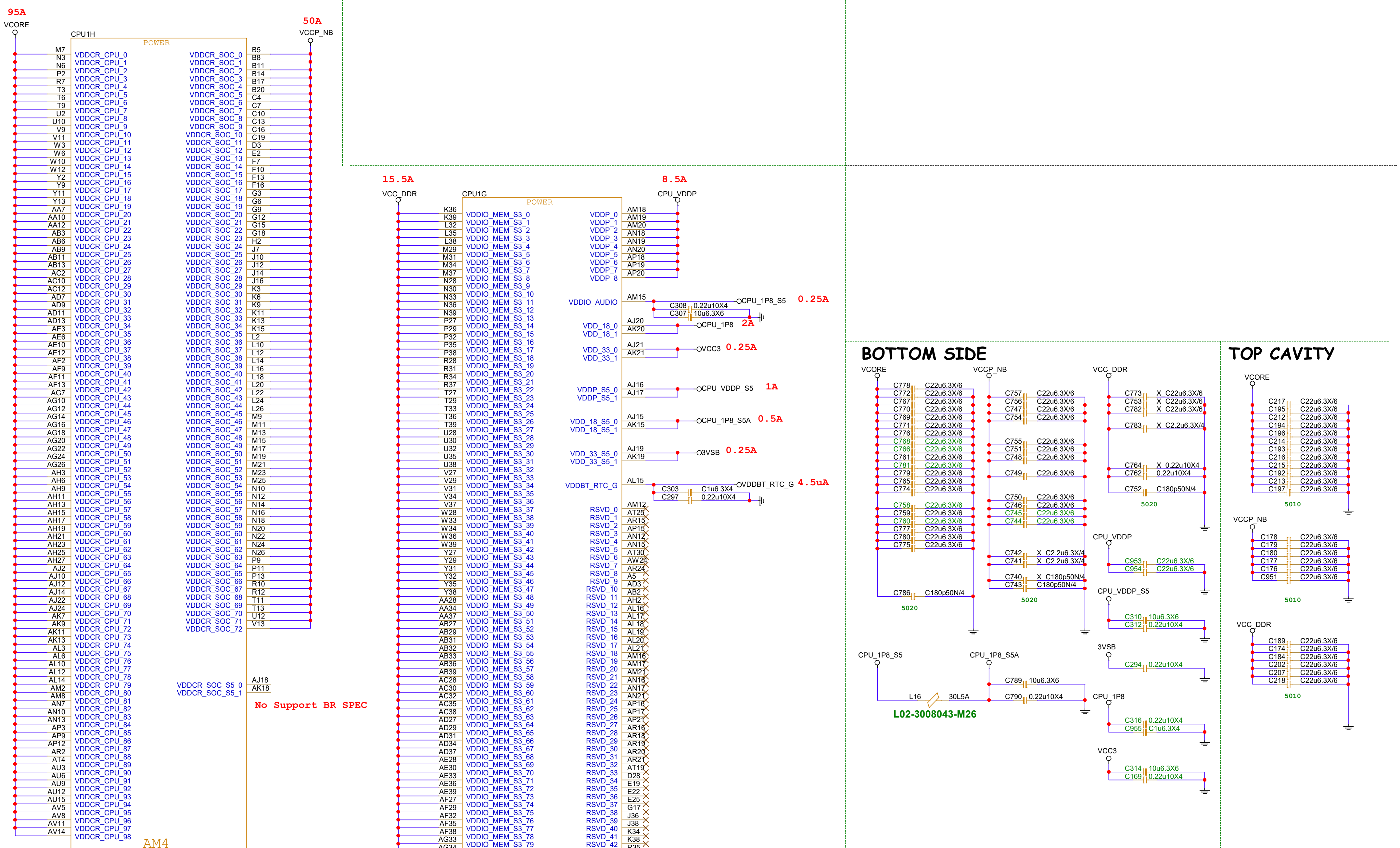
MS-7D54

Size	Document Description	Rev
Custom	AM4 LPC / SPI / USB / CLK / STRAP	11

Date Friday June 04 2021 Sheet 7 of 73

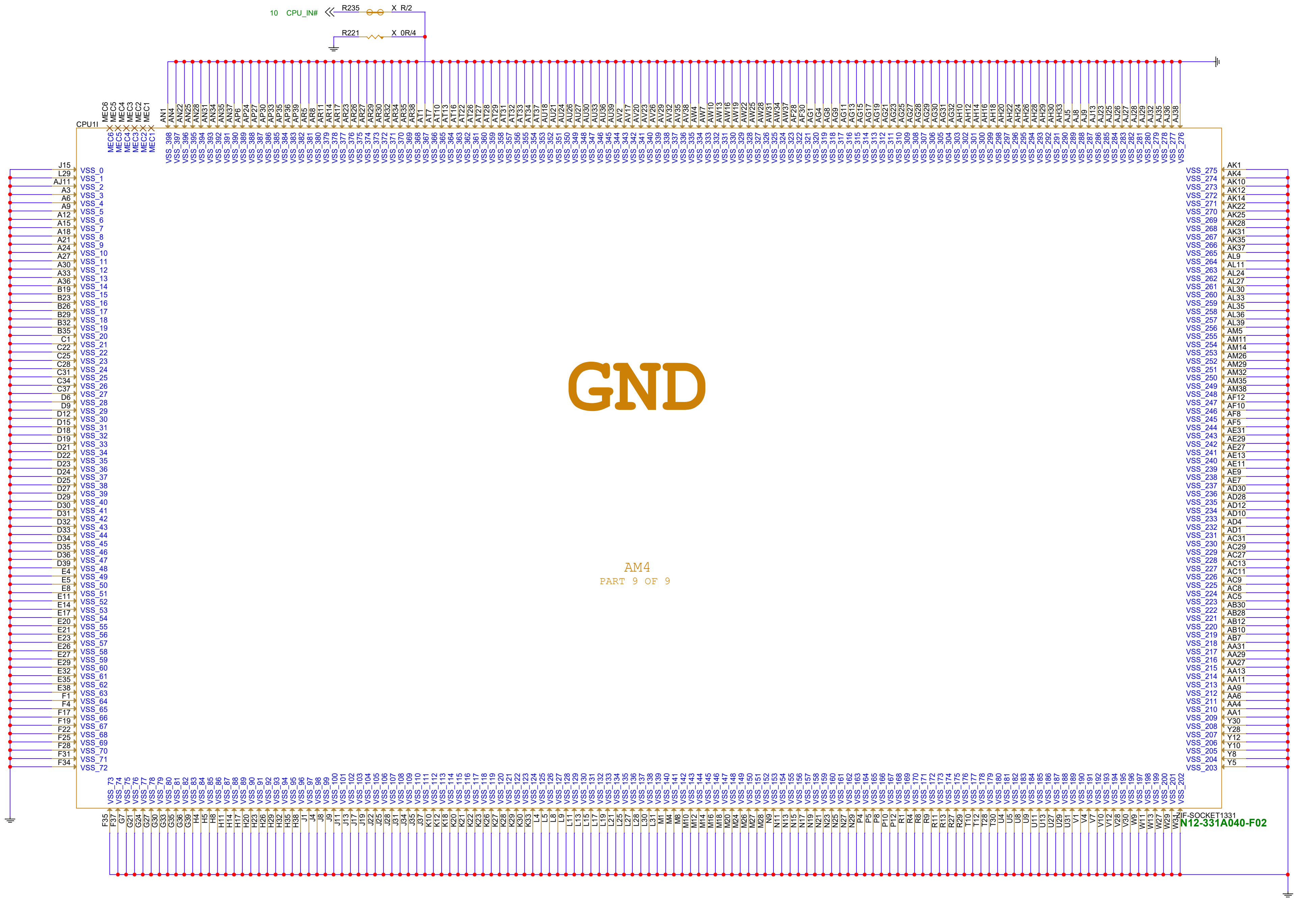


MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	AM4 Power / VDDIO_AUDIO	11

Date: Friday, June 04, 2021 — Sheet 8 of 73

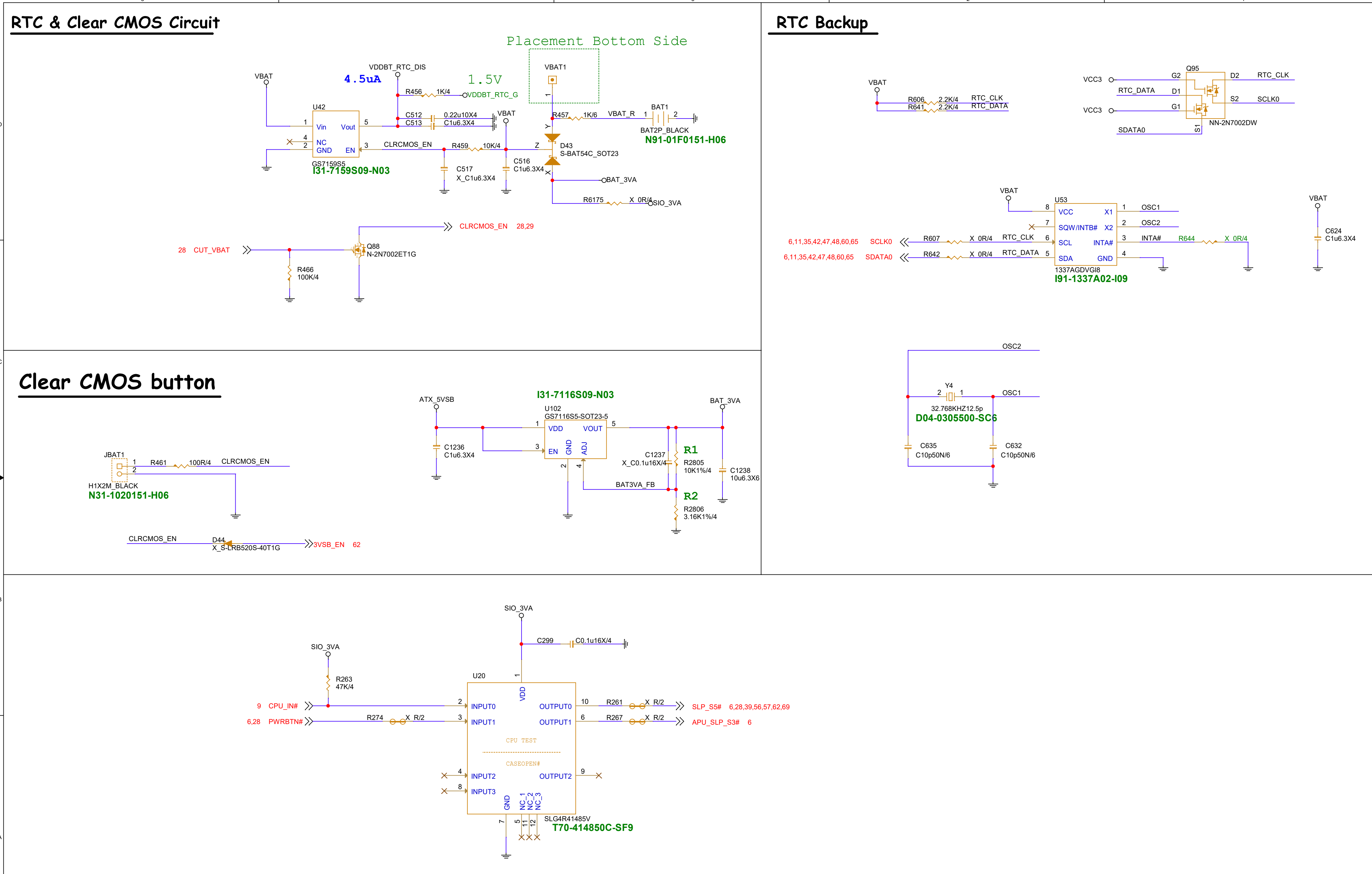


MICRO-STAR INT'L CO.,LTD

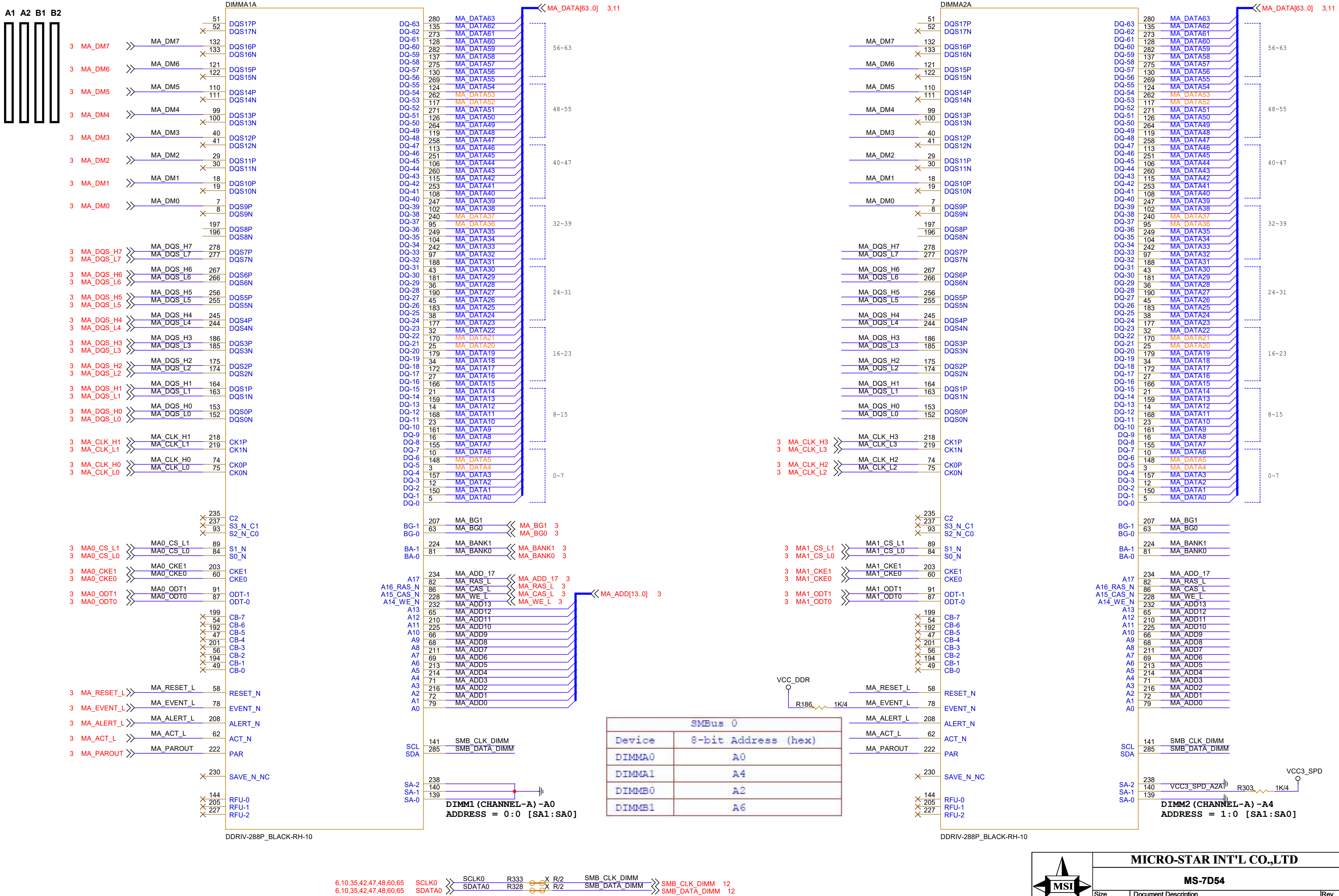
MS-7D54

Size	Document Description	Rev
Custom	AM4 GND	11

Date Friday, June 04, 2021 Sheet 9 of 73



MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: RTC / CMOS	Rev: 11
Date: Friday, June 04, 2021	Sheet 10 of 73	



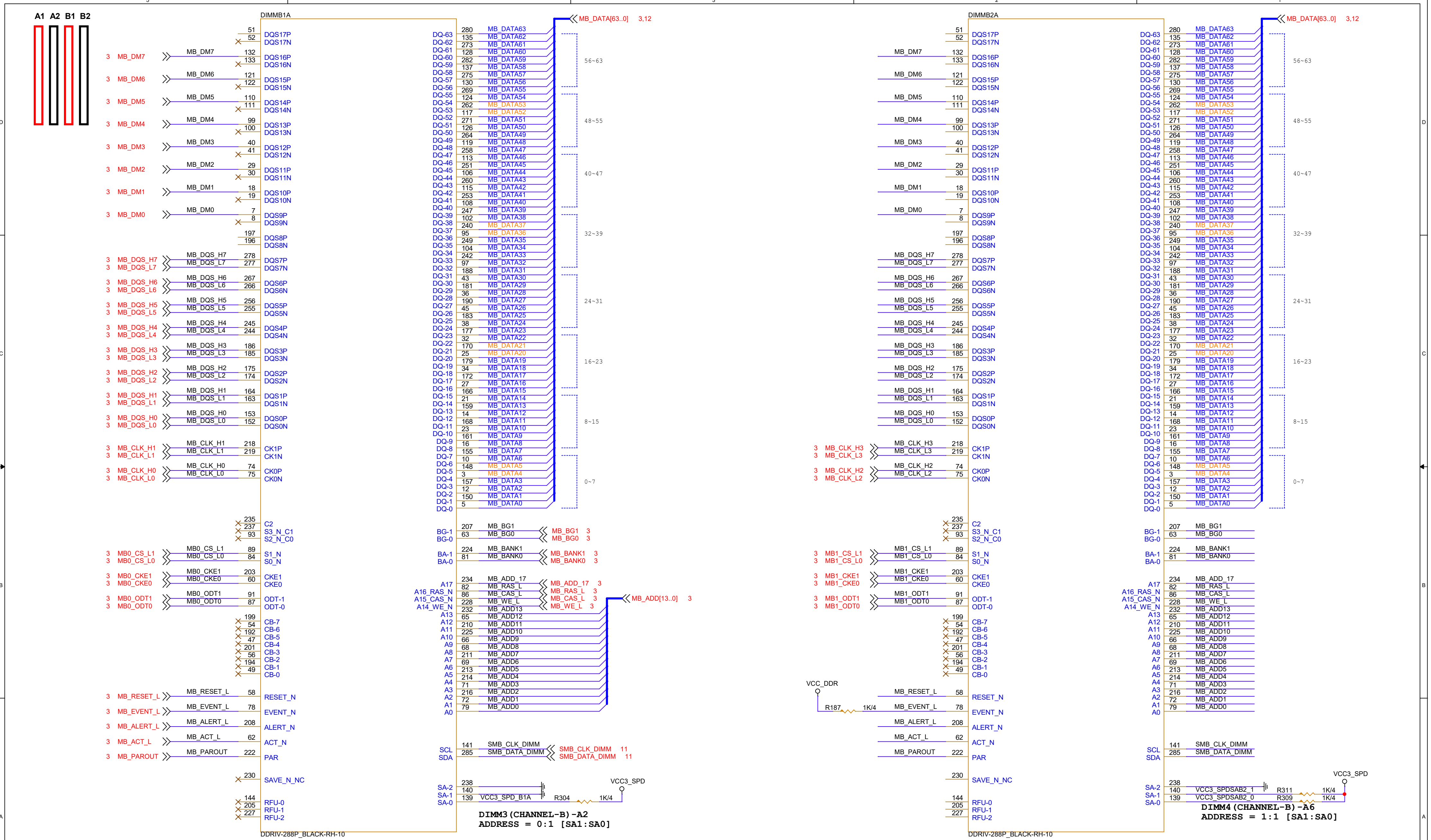
SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

MICRO-STAR INT'L CO.,LTD

MS-7D54

Size: Custom
Document Description: DDR4 - DIMM CH-A
Rev: 11

Date: Friday, June 04, 2021 Sheet 11 of 73

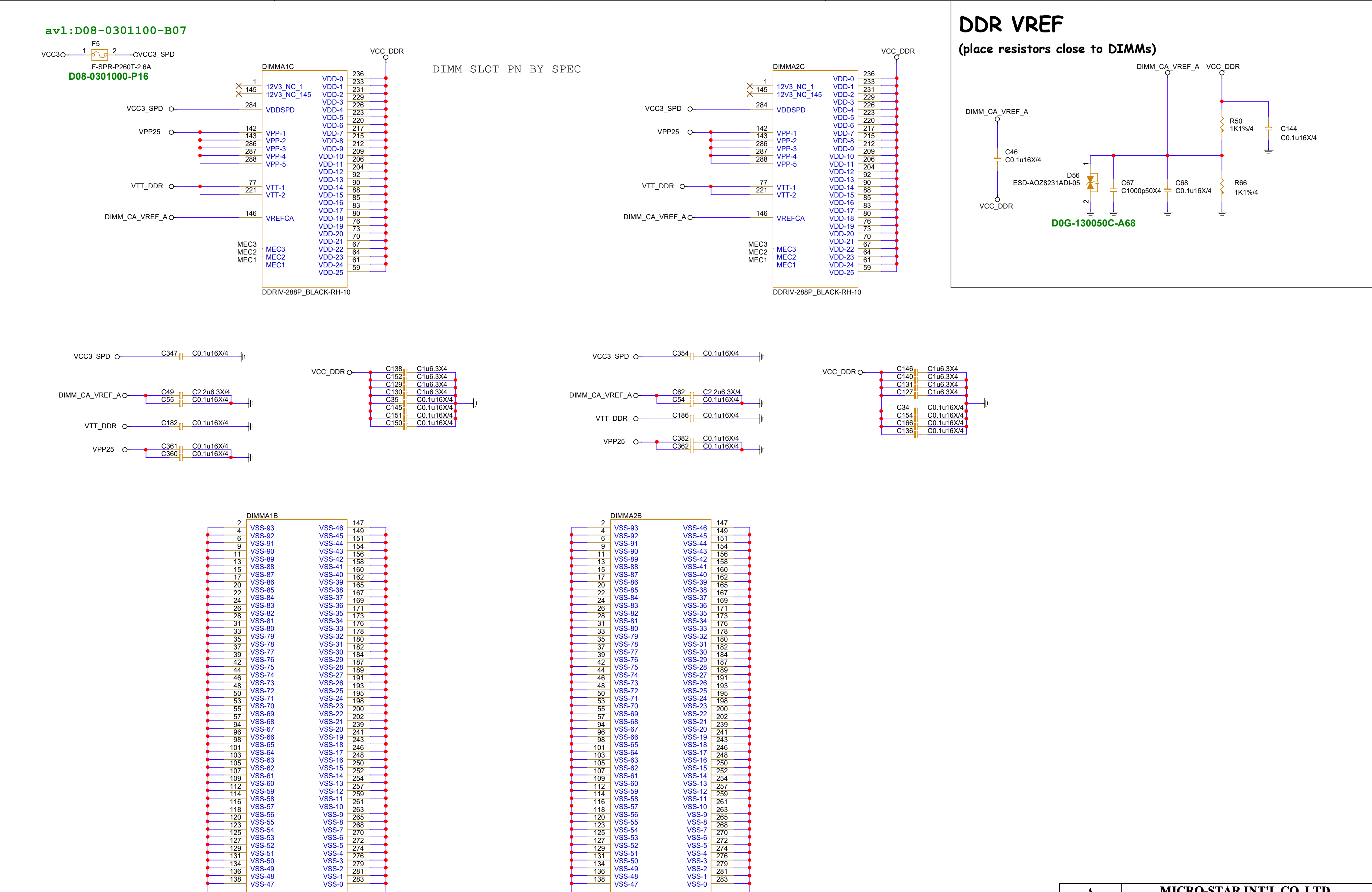


MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	11

Date: Friday, June 04, 2021 | Sheet 12 of 73



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MS-7D54

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	11

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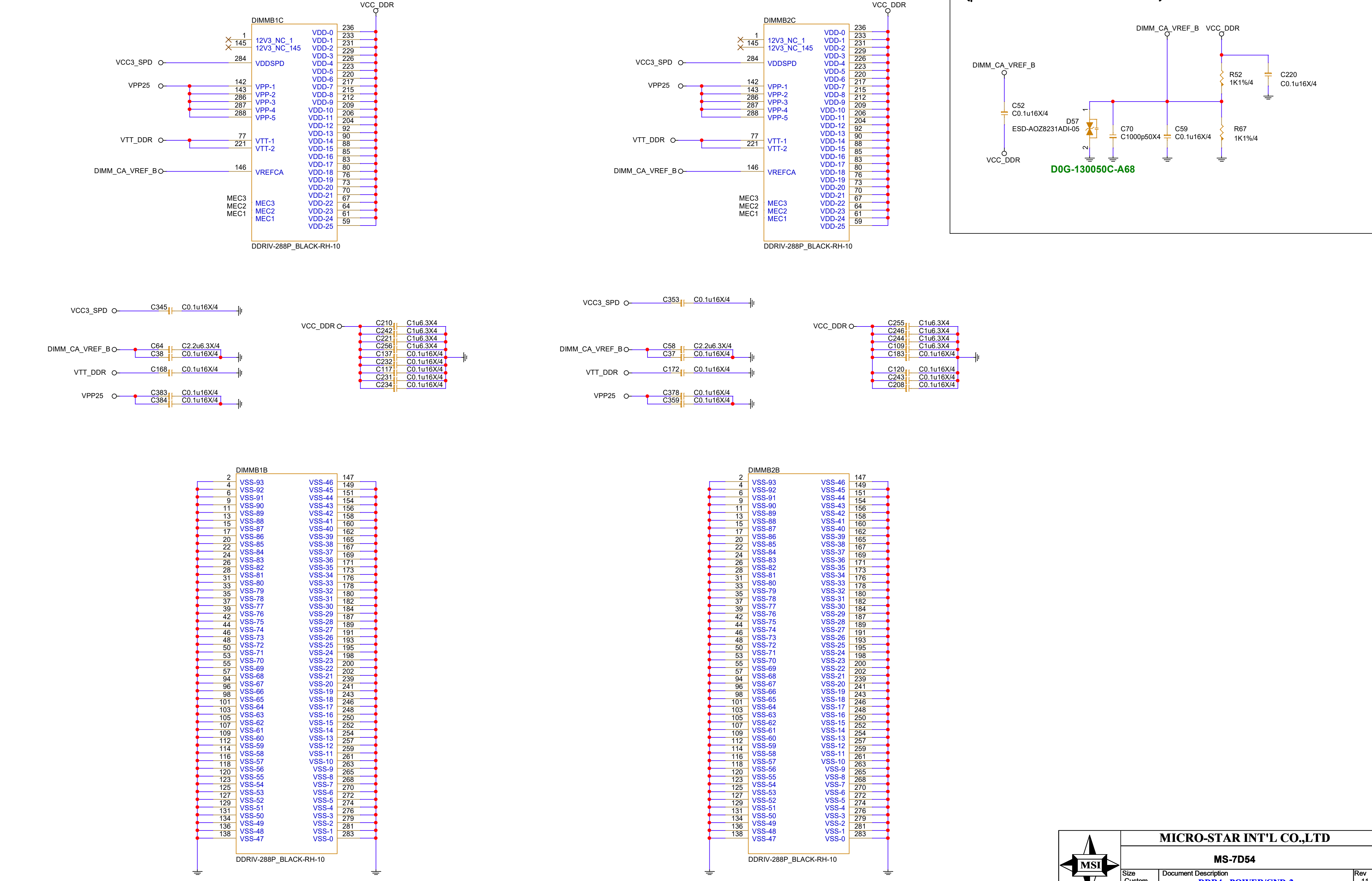
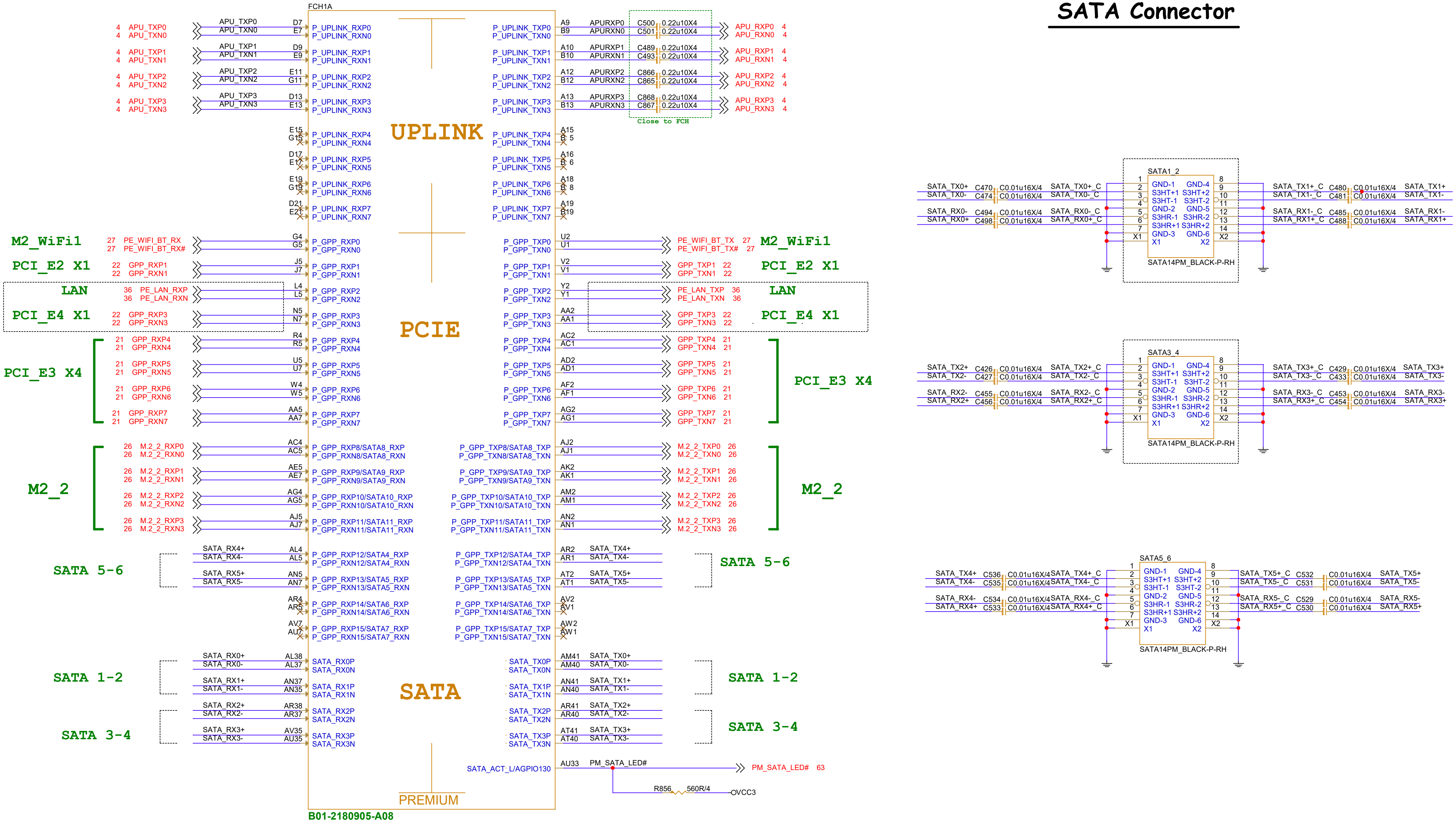
DDR VREF

(place resistors close to DIMMs)

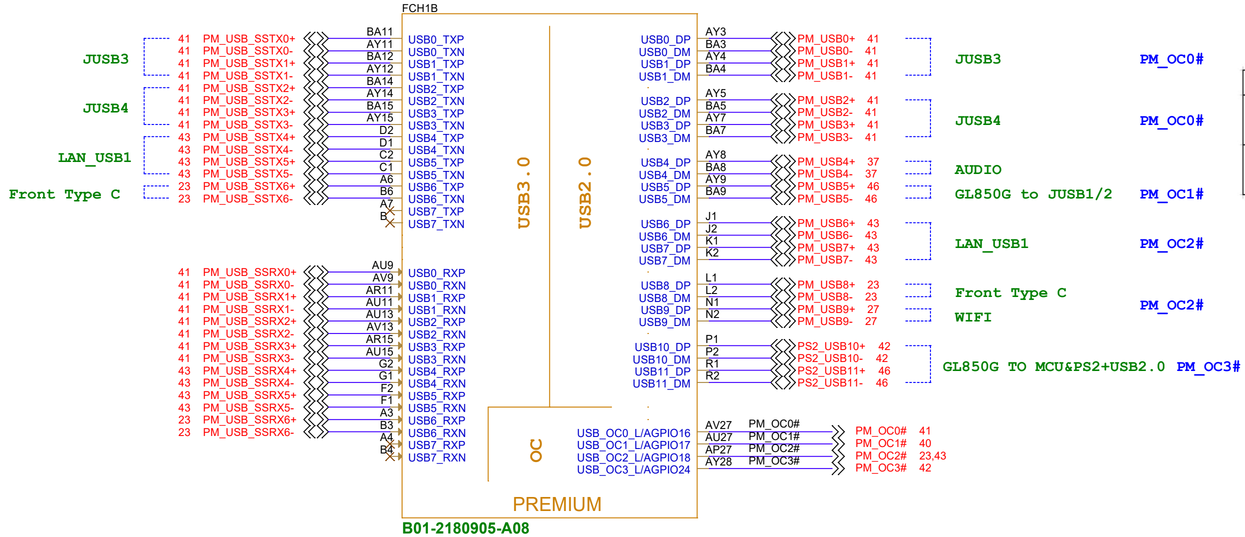


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D54	
Size: Custom	Document Description: DDR4 - POWER/GND-2	Rev: 11
Date: Friday, June 04, 2021	Sheet 14 of 73	

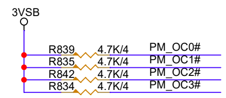
SATA Connector



MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: Premium - PCIE/SATA	Rev: 11
Date: Friday, June 04, 2021	Sheet 15 of 73	



Ports	Host Controller	OC Pins Mapped
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0_L/AGPIO16
		USB_OC1_L/AGPIO17
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC2_L/AGPIO18
		USB_OC3_L/AGPIO24



21ci203T

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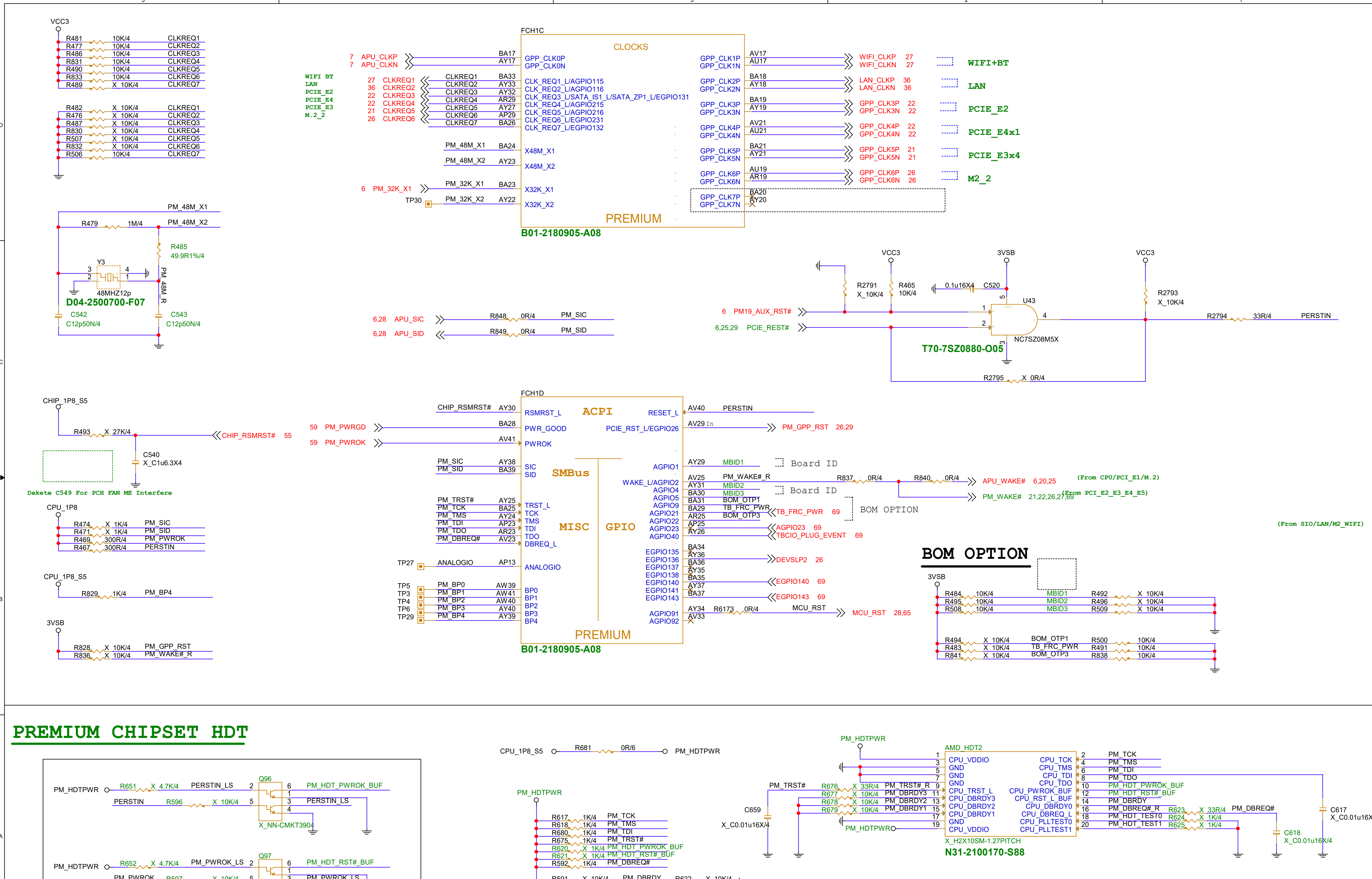
MS-7D54

Size: Custom | Document Description: Premium - USB/OC | Rev: 11

Date: Friday, June 04, 2021 | Sheet 16 of 73

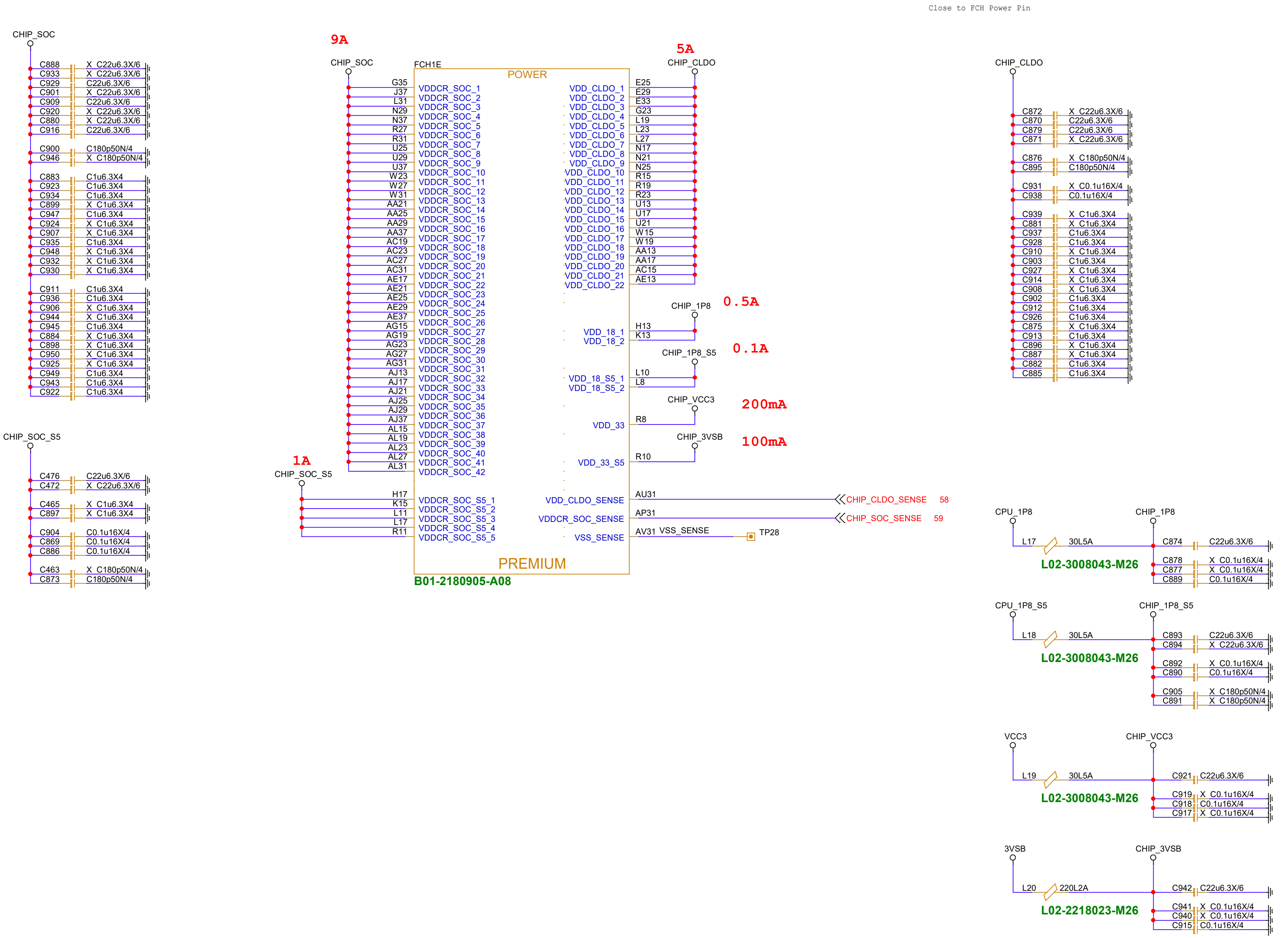


MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	Premium - CLK/ACPI/GPIO	11

Date Friday June 04 2021 Sheet 17 of 73

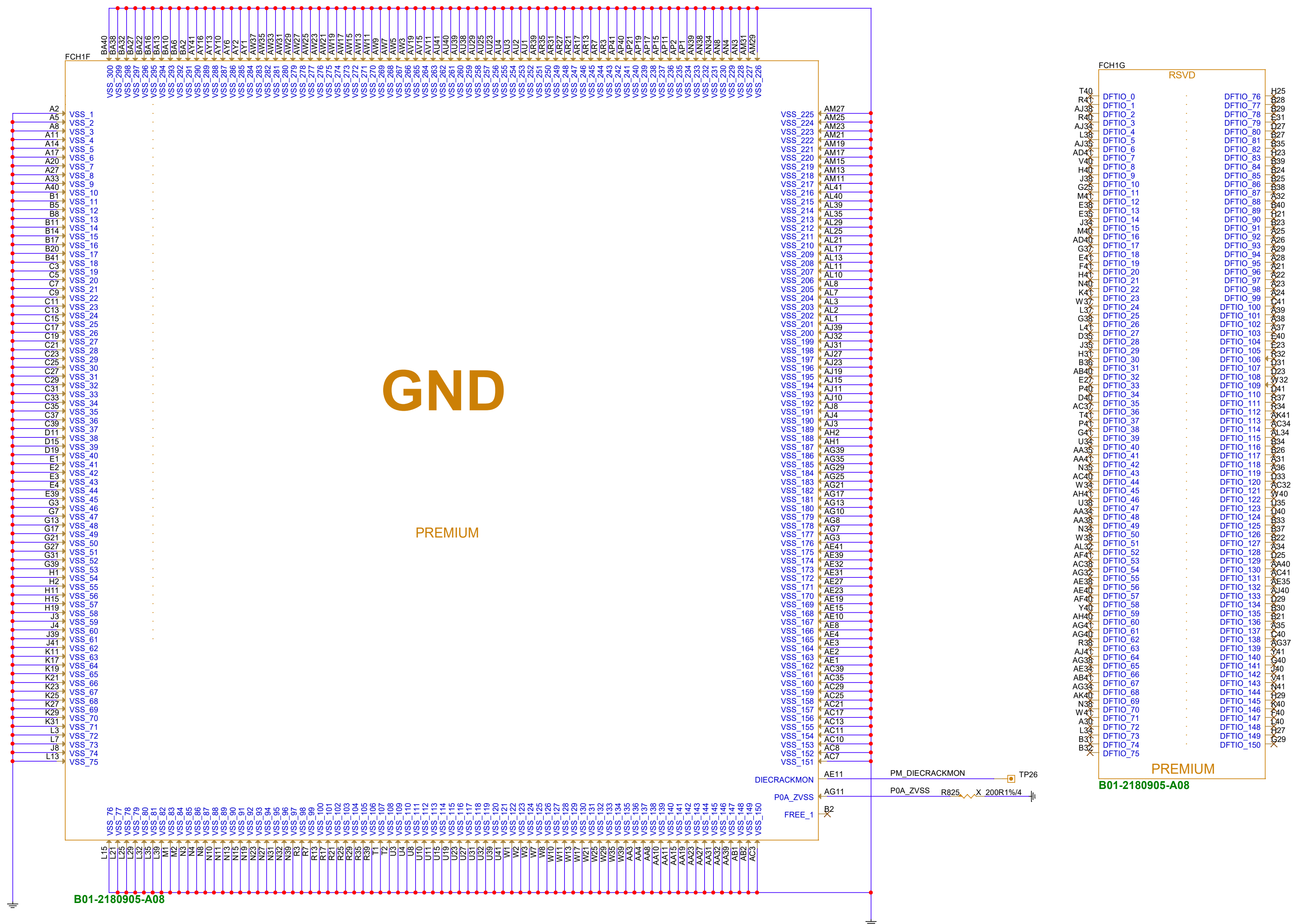


MICRO-STAR INT'L CO.,LTD

MS-7D54

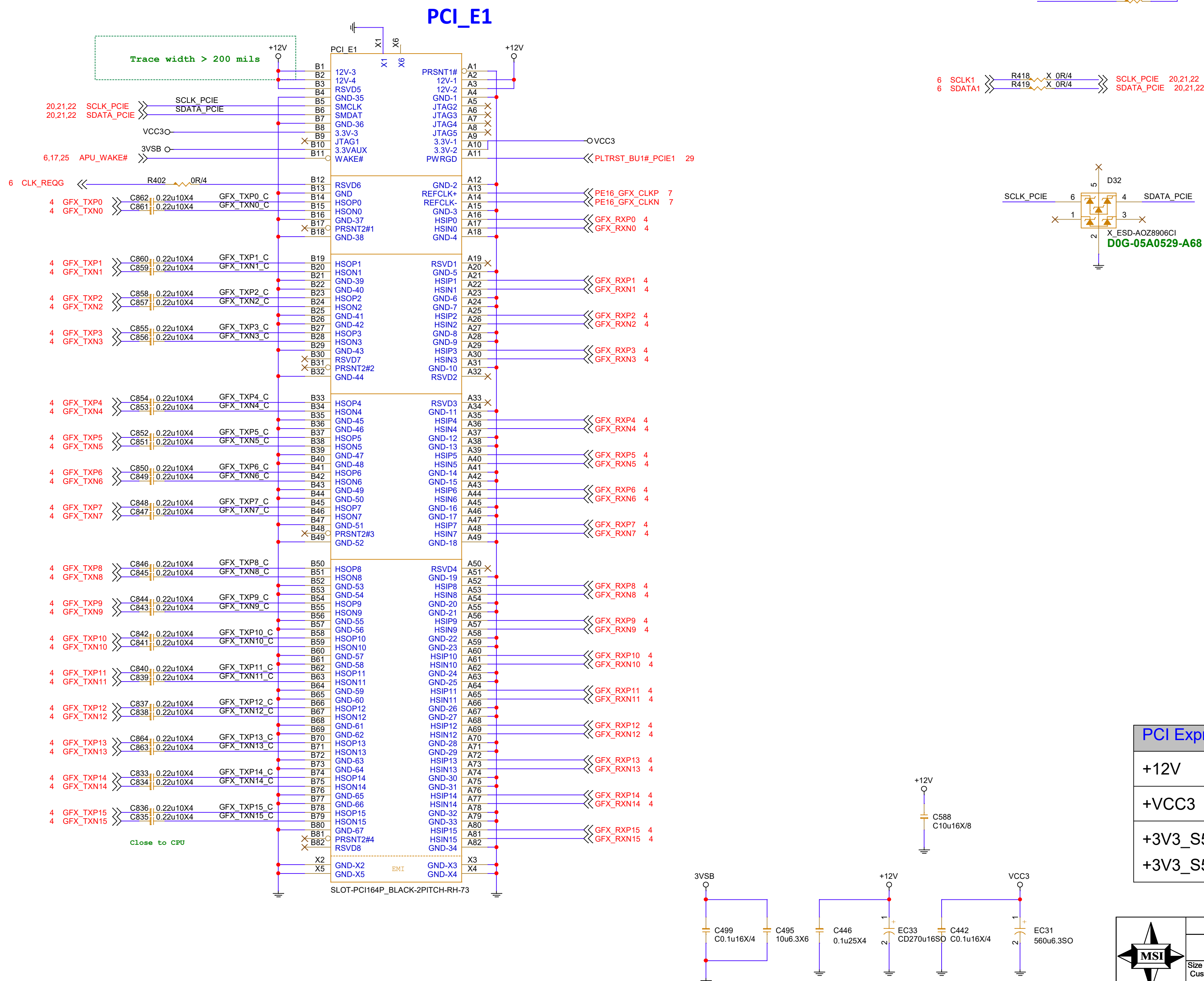
Size	Document Description	Rev
Custom	Premium - Power	11

Date: Friday, June 04, 2021 — Sheet 18 of 73



MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: **Premium - GND**	Rev: 11
Date: Friday, June 04, 2021	Sheet 19 of 73	

PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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MS-7D54

Size	Document Description	Rev
Custom	PCI_E1 (X16)	11

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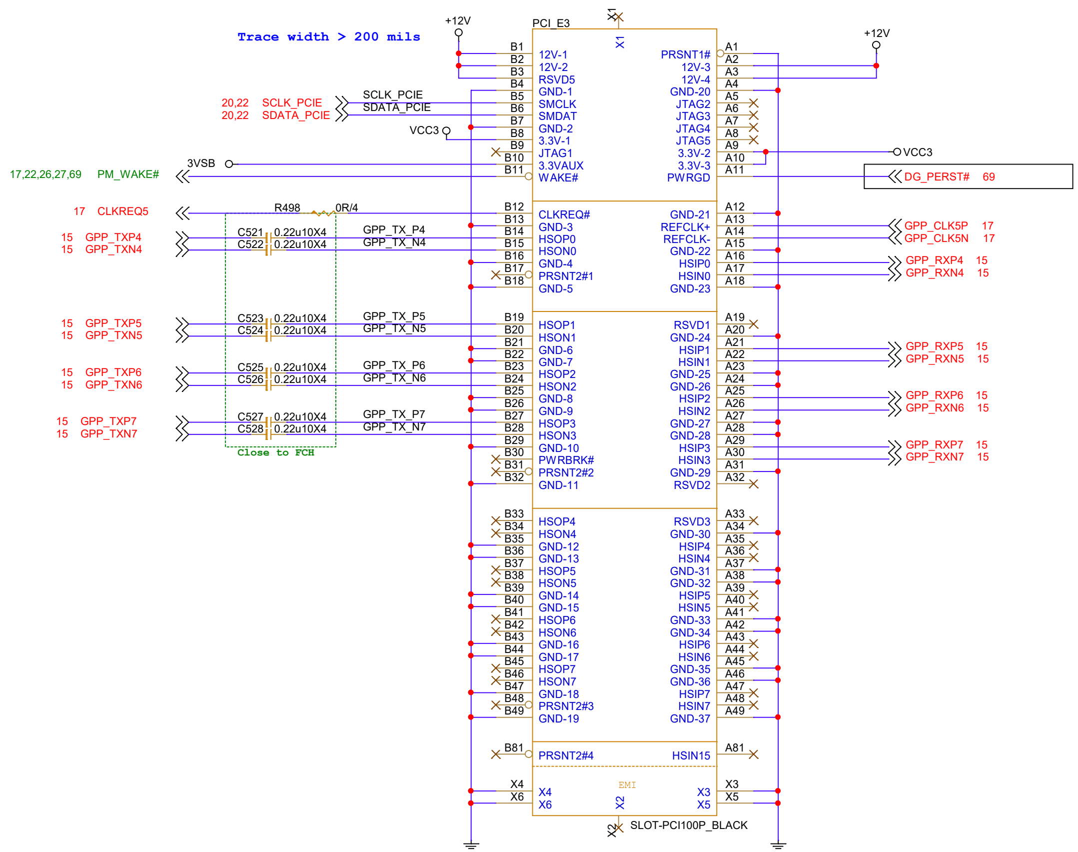
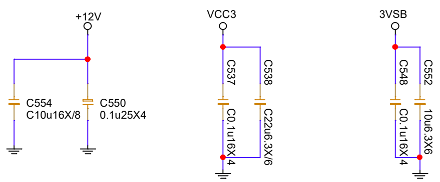
PCI_E3 X4





PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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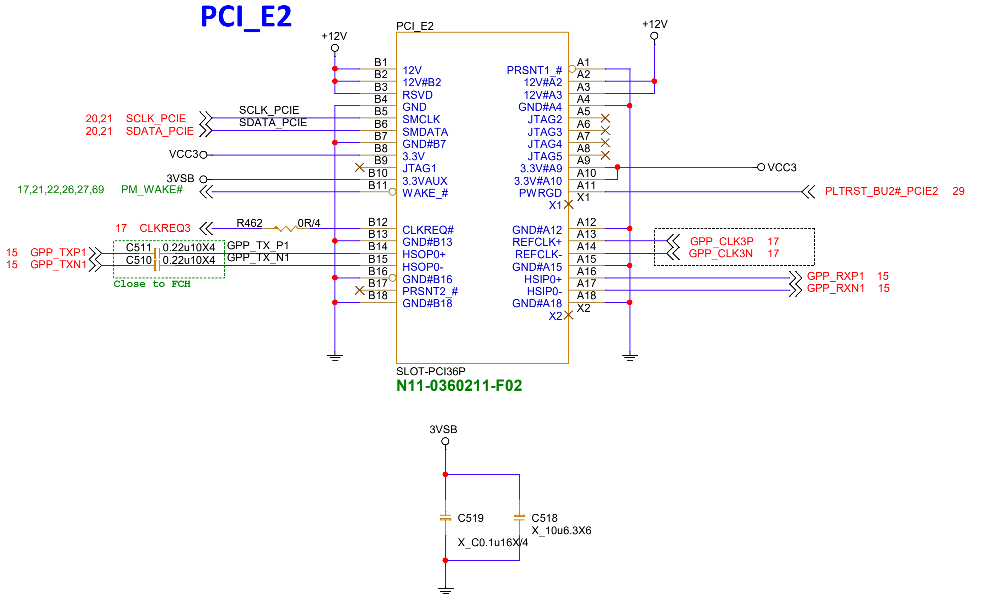
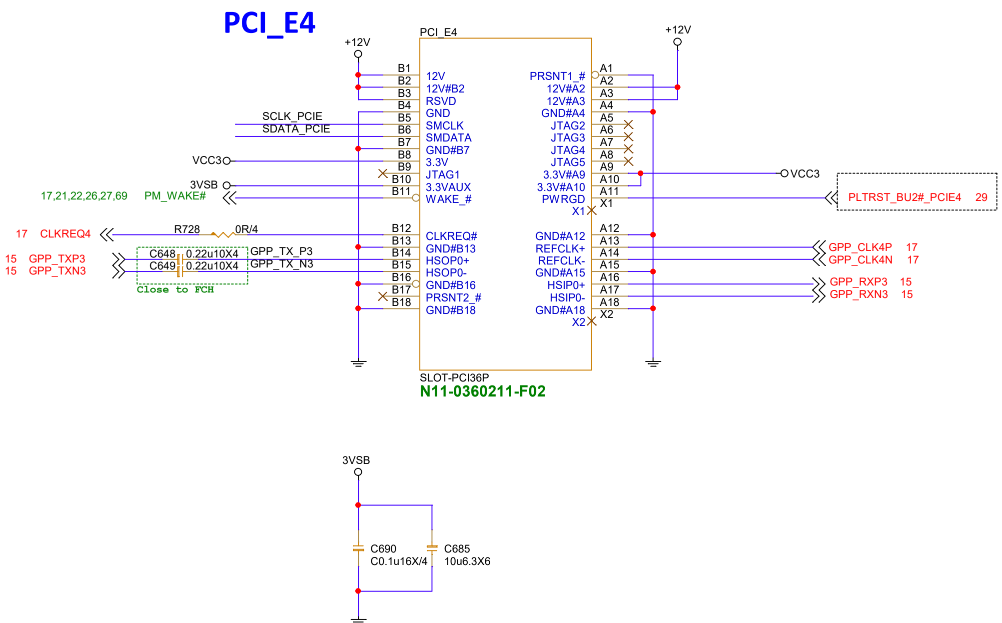
Size	Document Description	Rev
Custom	PCI_E3 (X4)	11
Date: Friday, June 04, 2021	Sheet 21 of 73	

PCI_E2



PCIE_E2 & PCIE_E4がち， PCIE_E2 & PCIE_E4 TPCIE device PCIE_E4 綫

PCI_E4



PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

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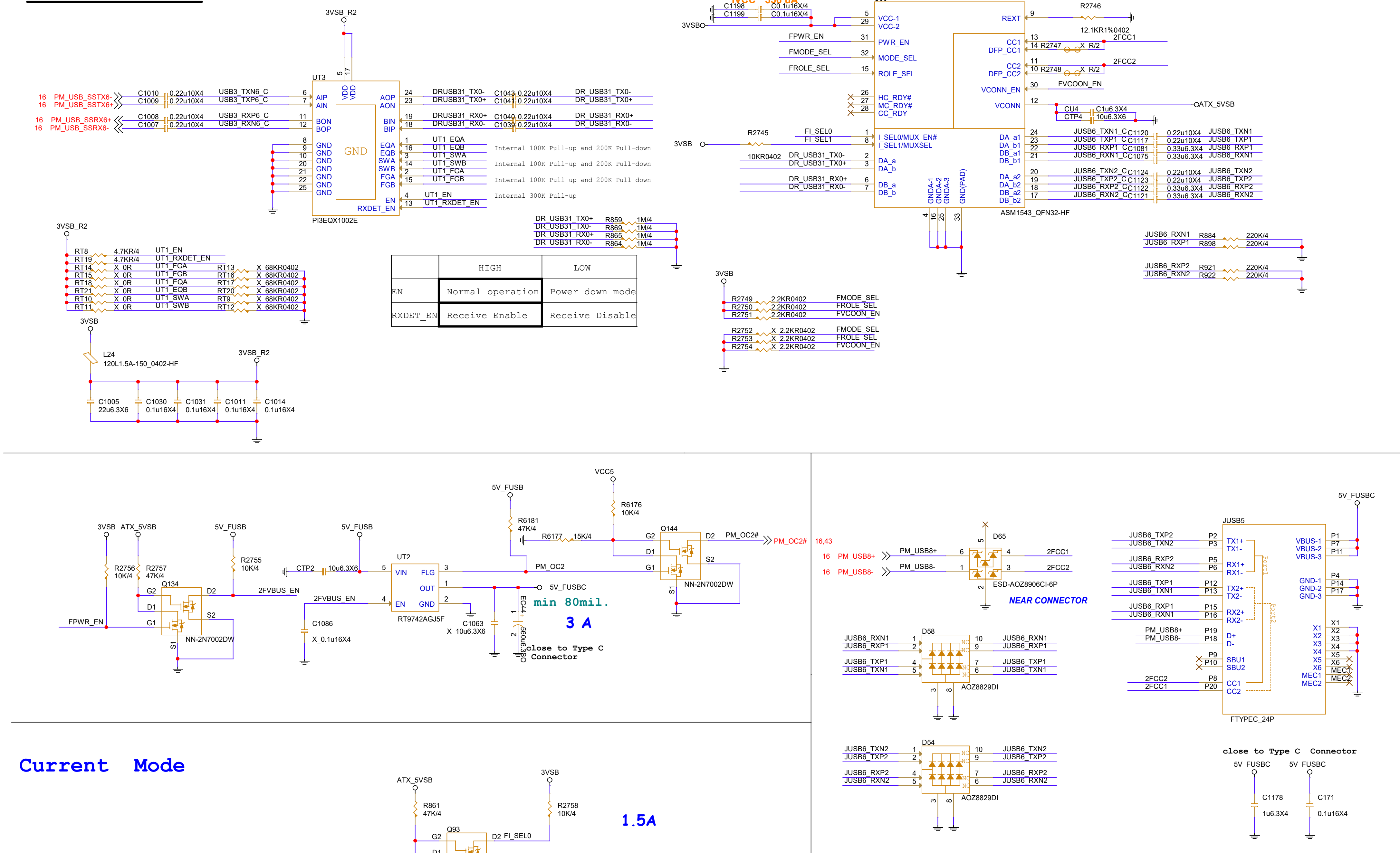
Size	Document Description	Rev
Custom	PCIE Switch PCI_E2 / E4 / E5 (X1)	11
Date: Friday June 04 2021	Sheet 22 of 73	

USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)



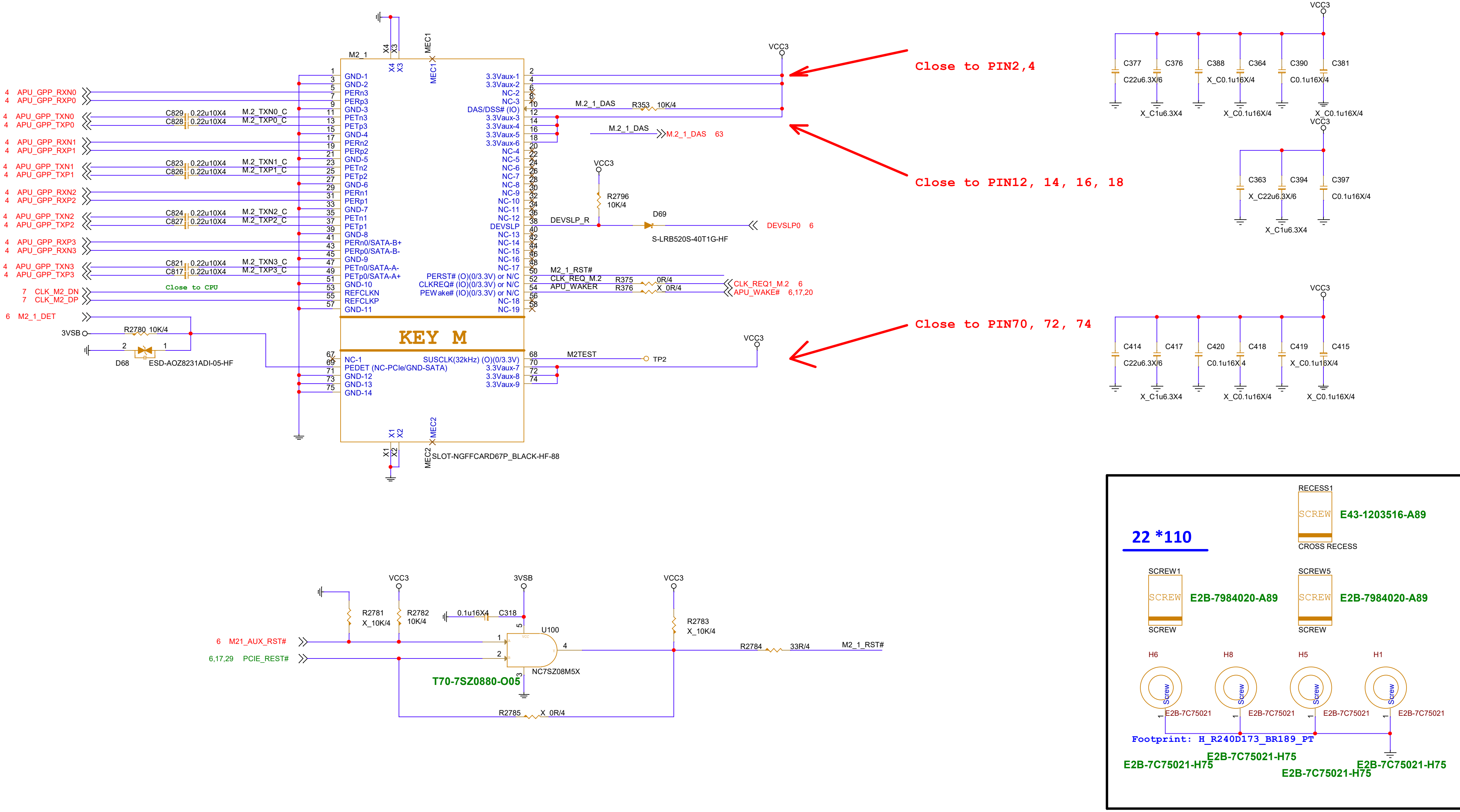
	HIGH	LOW
EN	Normal operation	Power down mode
RXDET_EN	Receive Enable	Receive Disable

Current Mode

MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: Front USB Type-C Gen2	Rev: 11
Date: Friday June 04 2021	Sheet 23 of 73	

M.2 1 Connector

VCC3 4.25A
Max: 14W



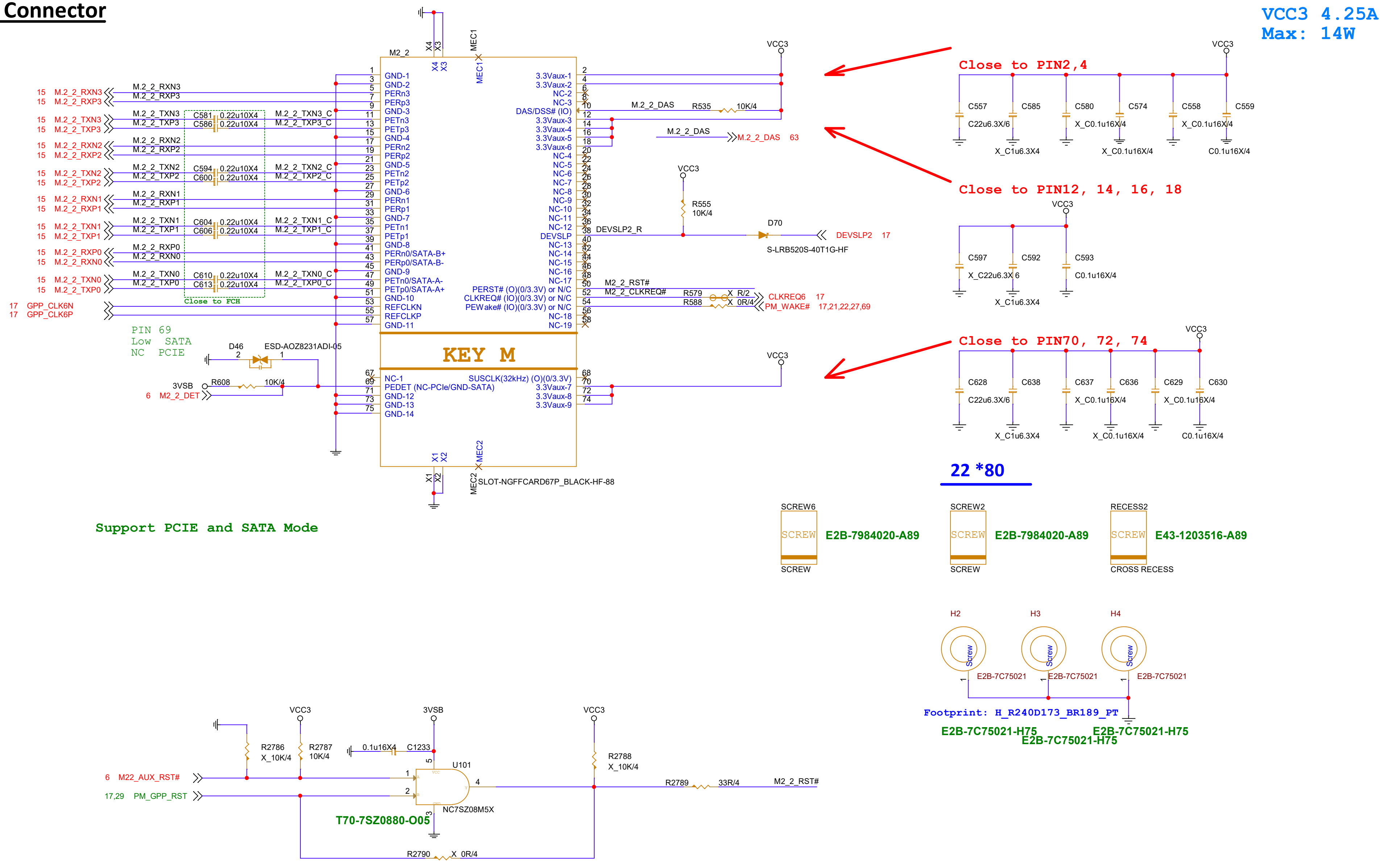
MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	M2_1	11

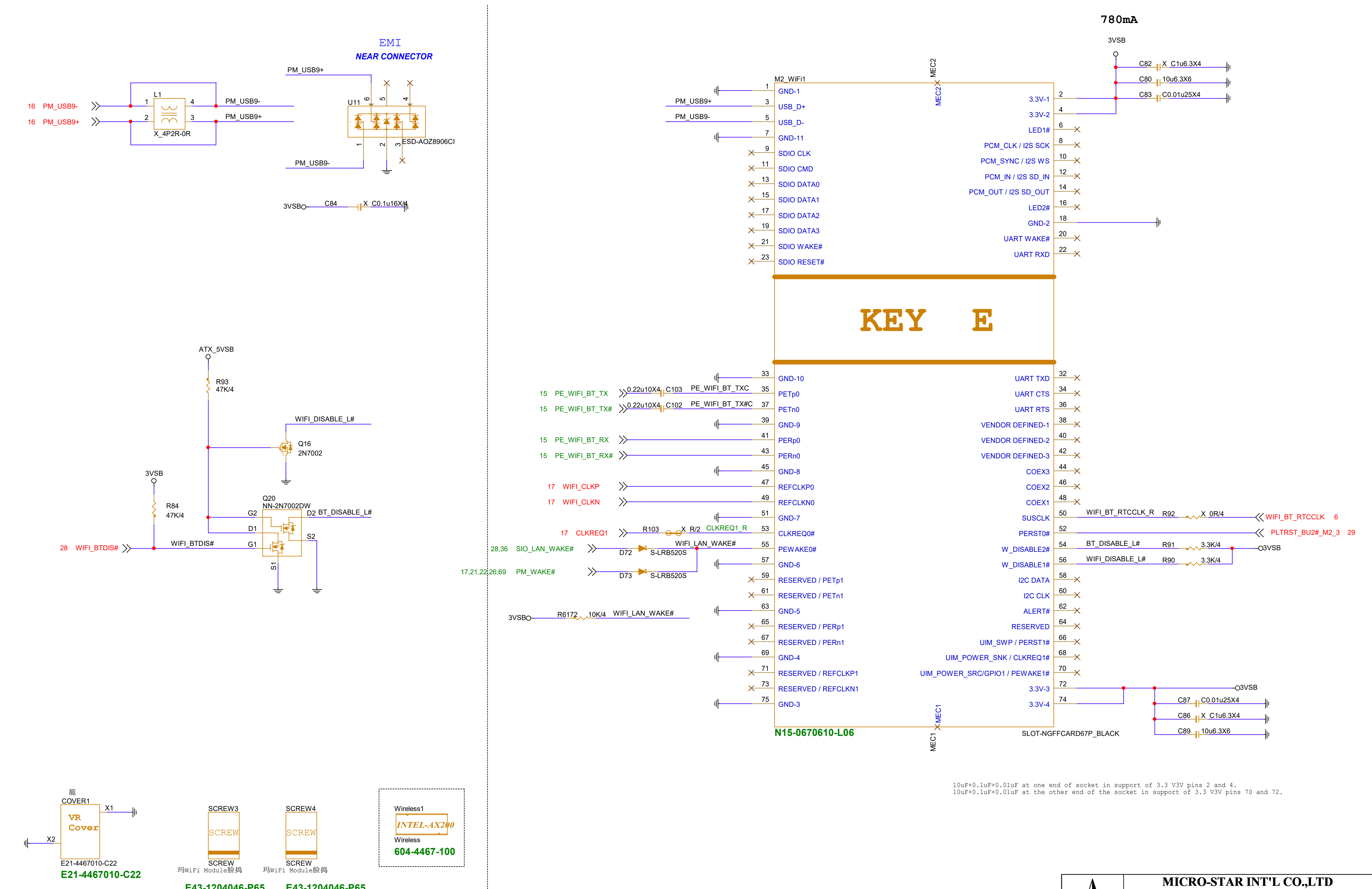
Date Friday, June 04, 2021 Sheet 24 of 73

M.2 2 Connector



Support PCIE and SATA Mode

MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: M2_2	Rev: 11
Date: Friday, June 04, 2021	Sheet 25 of 73	



MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	M2_WIFI+BT	11

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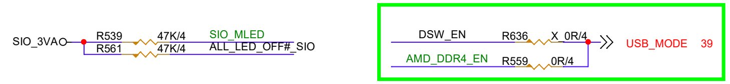
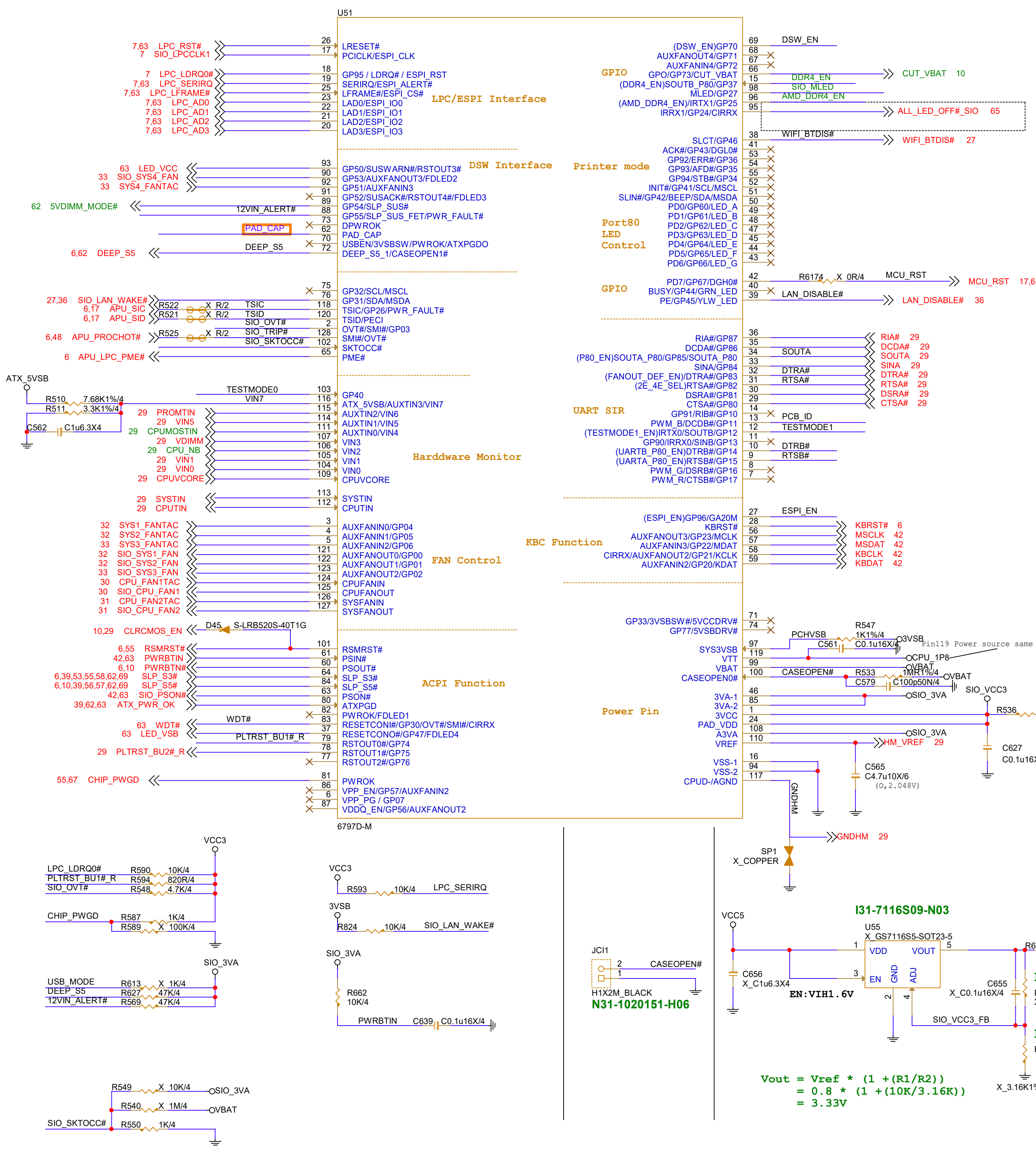
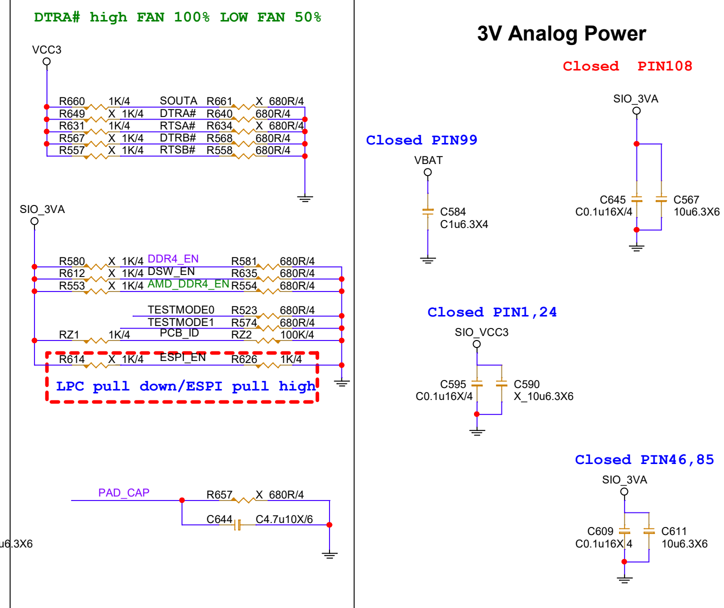


POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO





MICRO-STAR INT'L CO.,LTD

MS-7D54

Size	Document Description	Rev
Custom	SIO - NCT6797D-M	11

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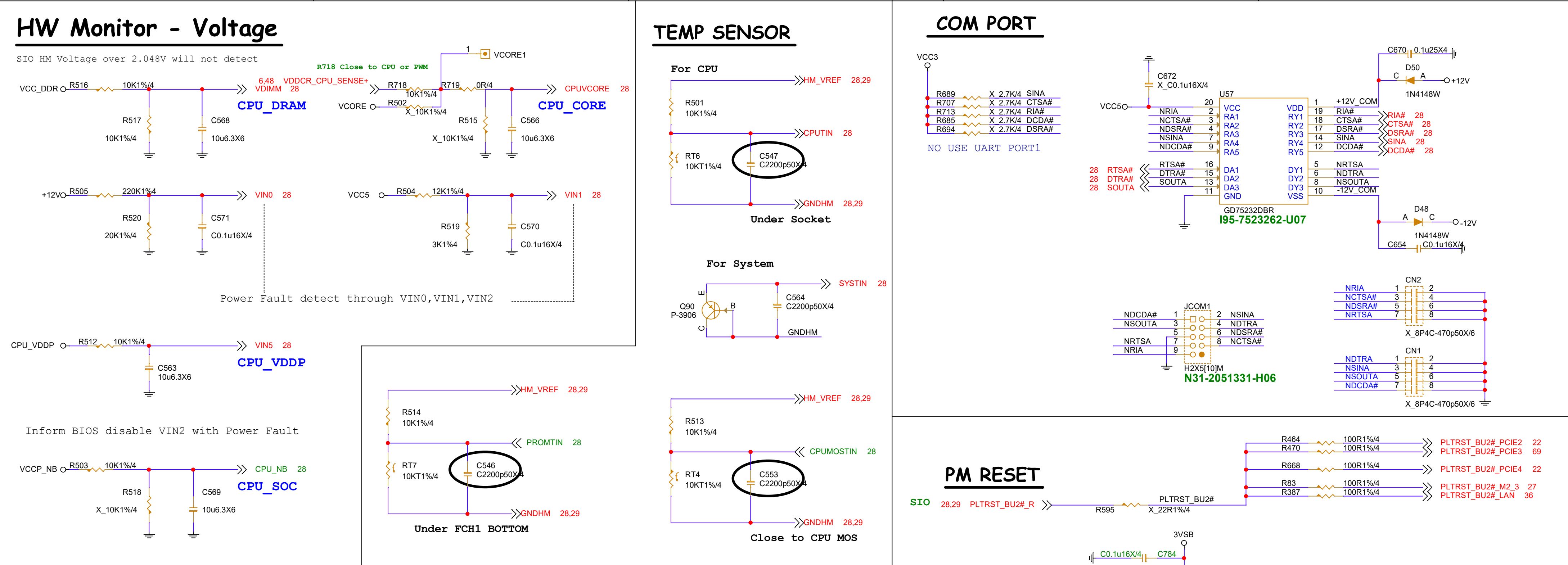
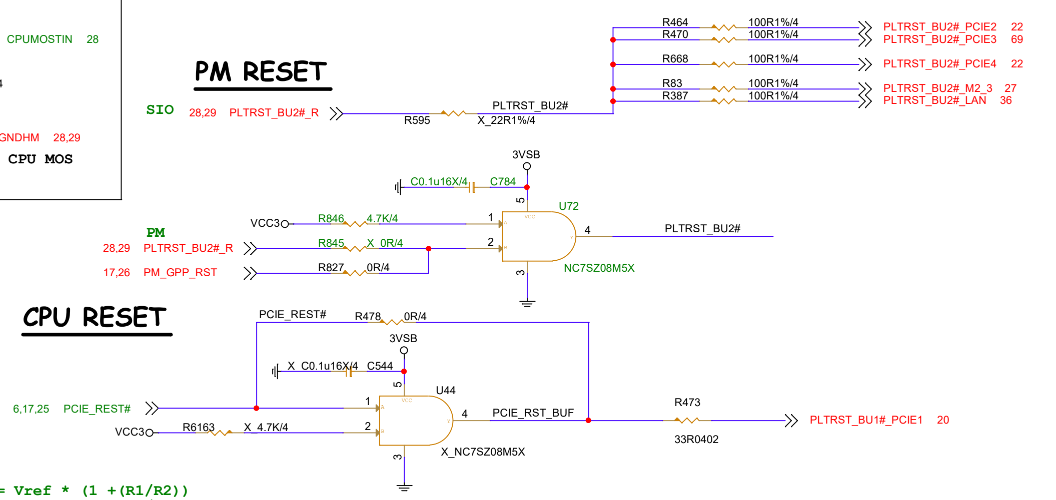




NCT7718W delete 20210315

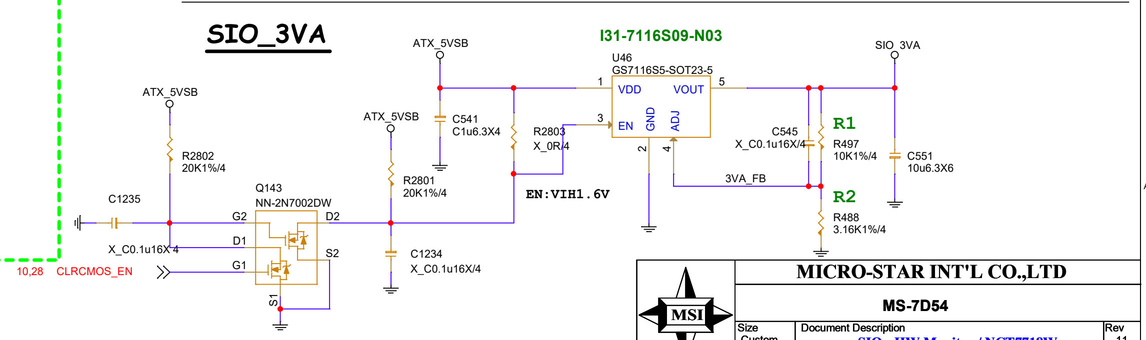
Layout notice:
1. Put the C1 2200pF to close the NCT7718W.
2. Add Ground Shielding For D and D- Traces.
3. D /D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

NCT7718W SM Bus address is 98h (1001100xb)

Default: ALERT# Output Comparator Mode

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

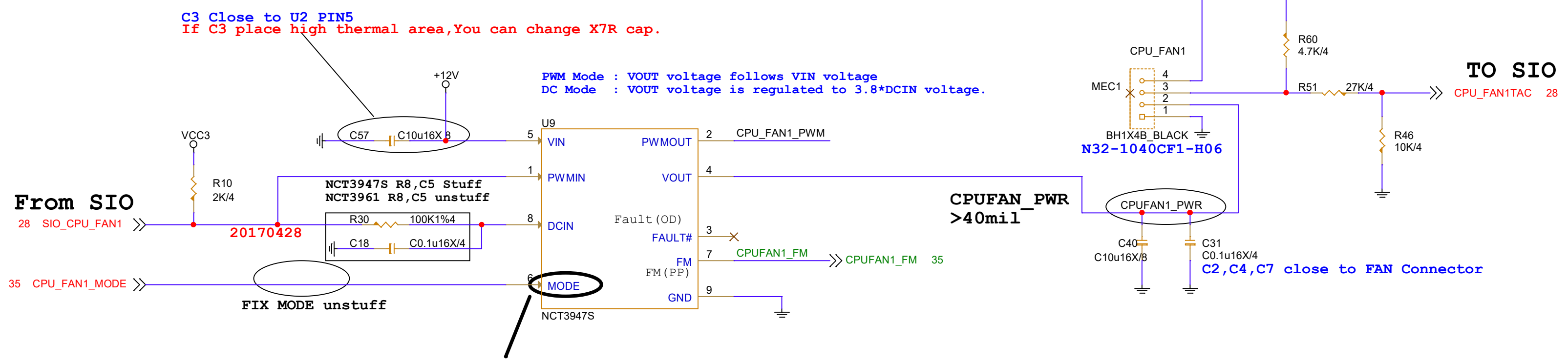


TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



GPIO Control

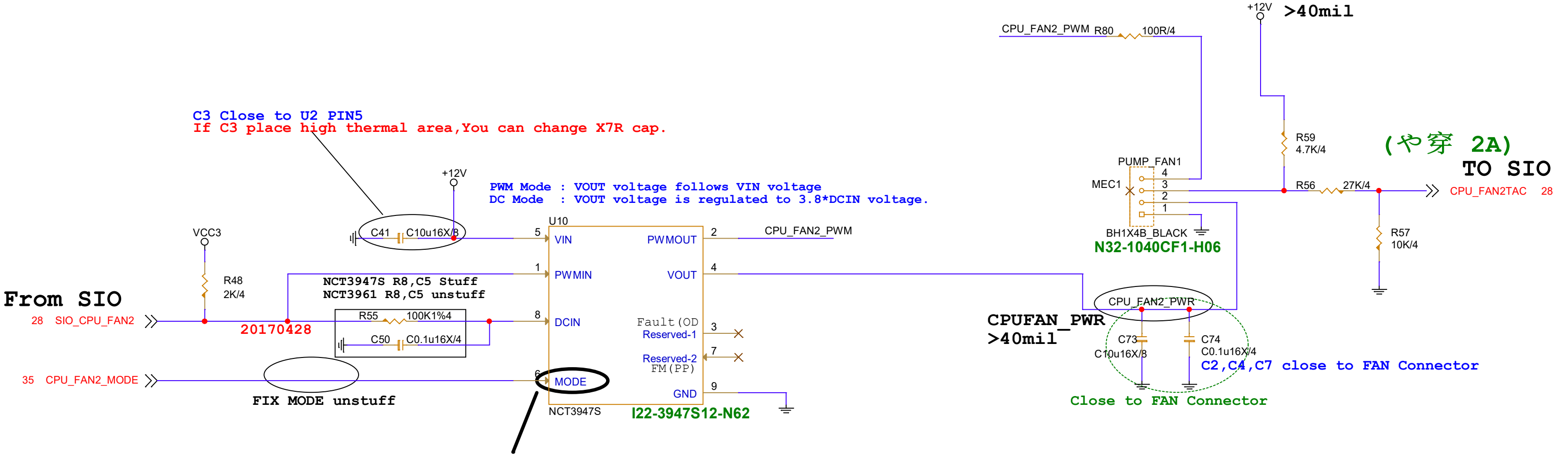
	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

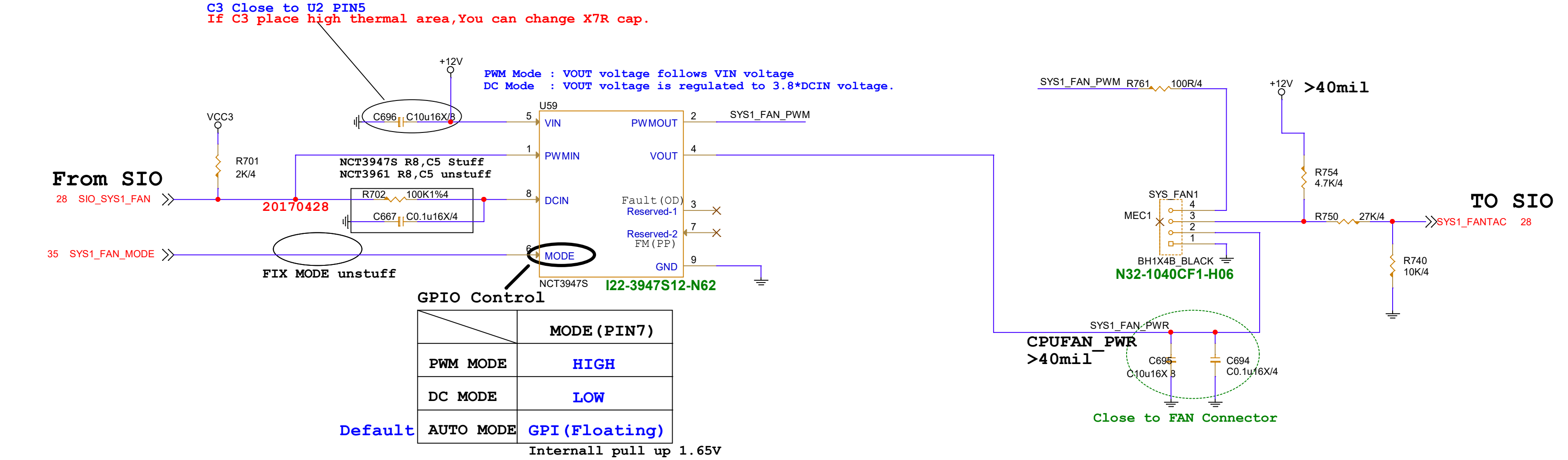
	PCH GPIO	
PWM MODE	HIGH	
DC MODE	LOW	
AUTO MODE	GPI(Floating)	Default

NCT3947S Internall pull up 1.65V

SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

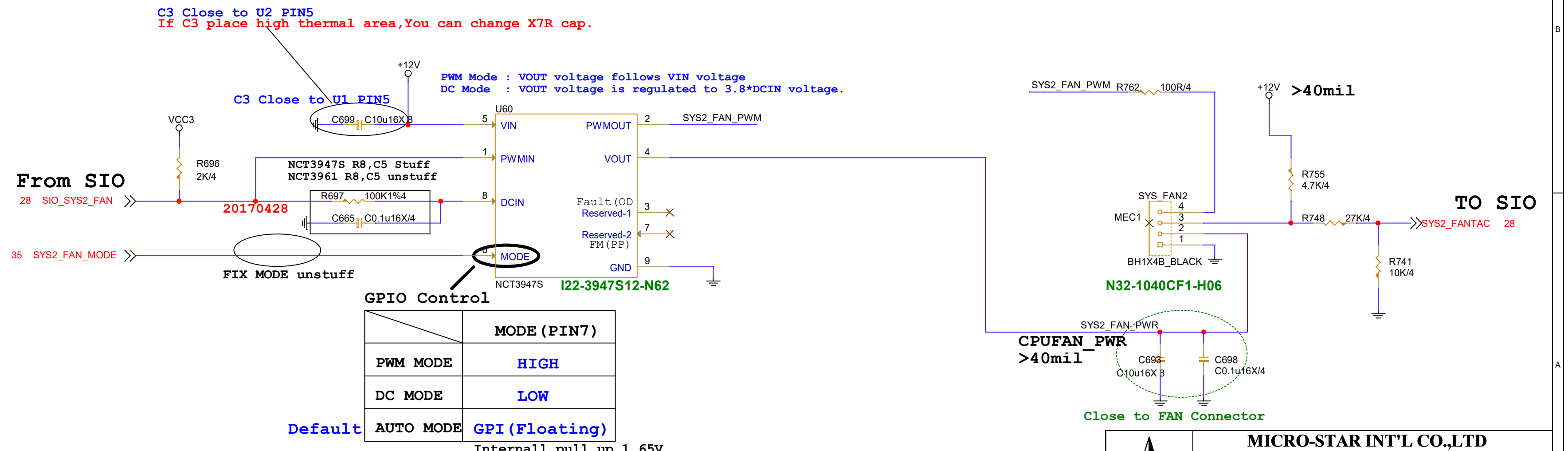
Default

Internall pull up 1.65V

SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V

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Size: Custom	Document Description: FAN TYPE-K SYSFAN1/2	Rev: 11
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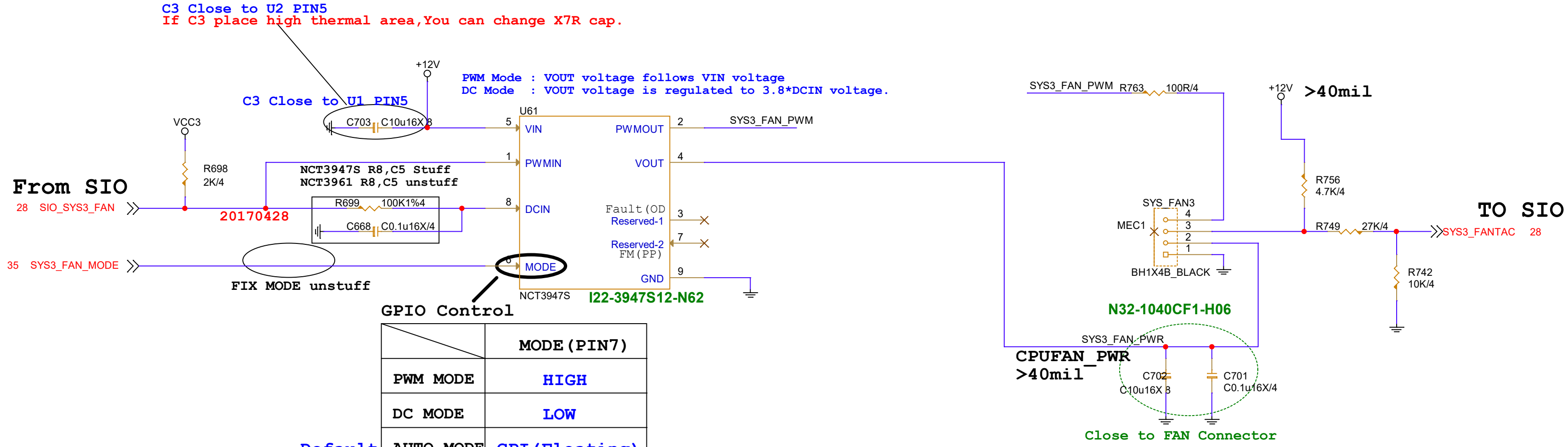
SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



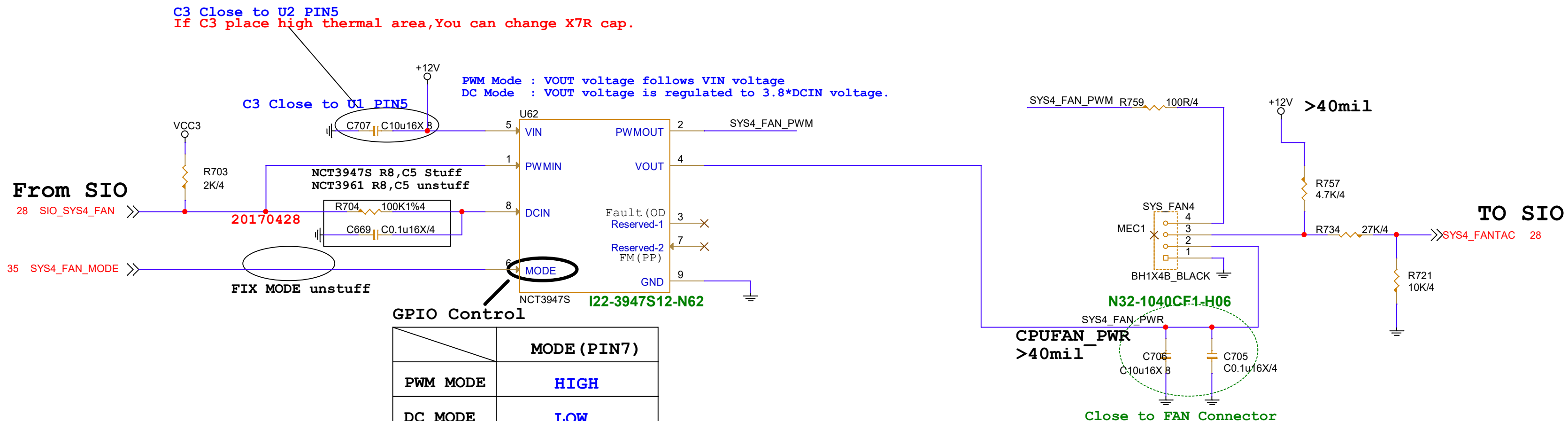
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



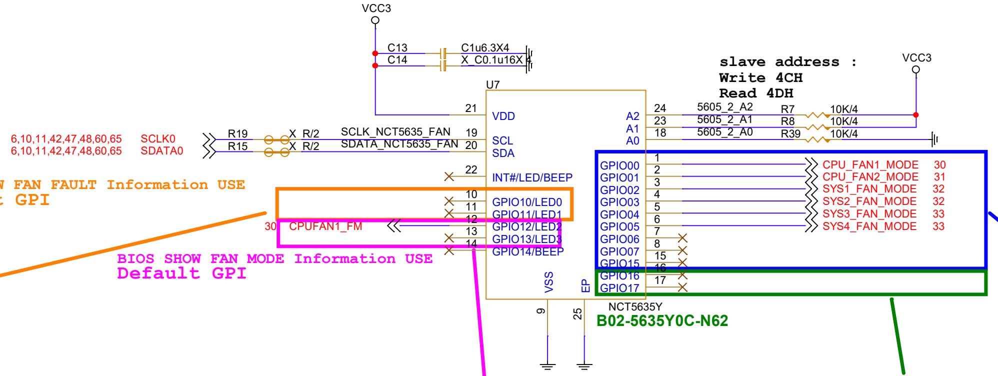
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

BIOS SHOW FAN FAULT Information USE
Default GPI

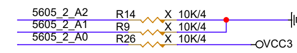
By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN



slave address :
Write 4CH
Read 4DH

BIOS SHOW FAN MODE Information USE
Default GPI



By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2

By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI
USE LED OFF & LED BLINK

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

use avoid S5 leakage

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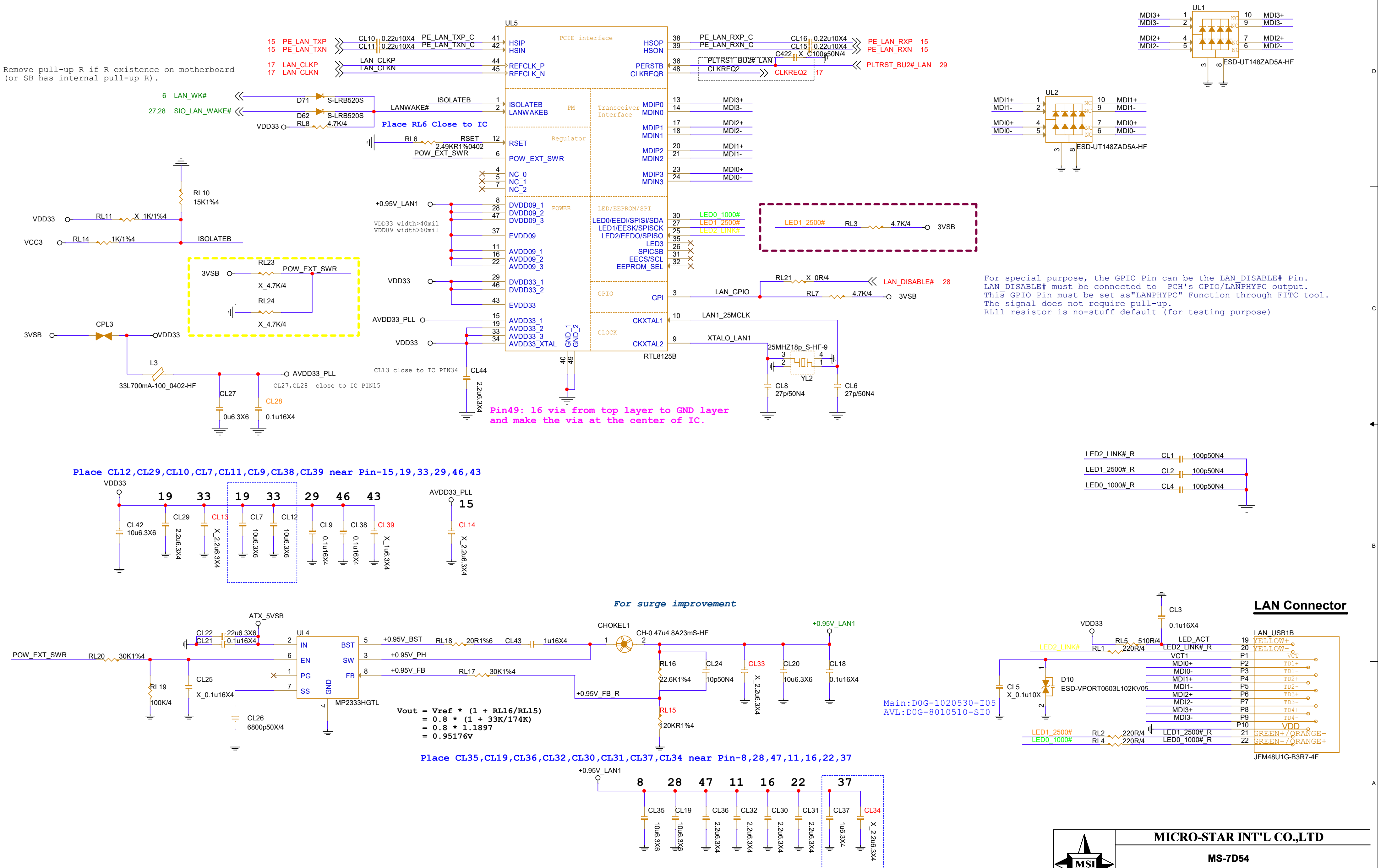
RTL8125B 10/100/1000/2.5G LAN Controller

ESD Protect
UL1&UL2 close to connector



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Size: Custom	Document Description: LAN - I211AT		Rev: 11
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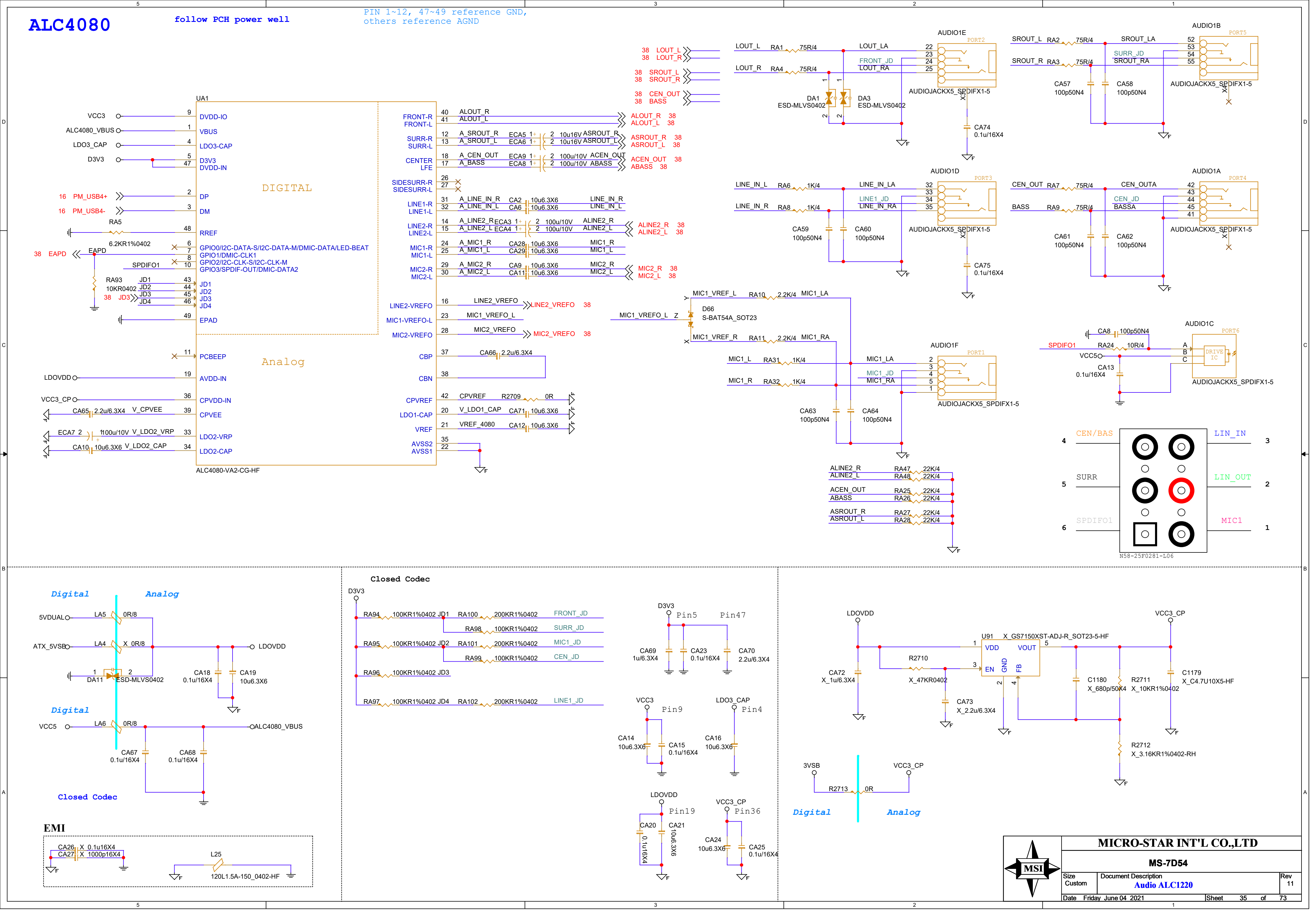

ALC4080
follow PCH power well
PIN 1~12, 47~49 reference GND,
others reference AGND
UA1
DIGITAL
Analog
ALC4080-VA2-CG-HF
VCC3
ALC4080_VBUS
LDO3_CAP
D3V3
DVDD-IO
VBUS
LDO3-CAP
D3V3
DVDD-IN
16 PM_USB4+
16 PM_USB4-
DP
DM
RA5
6.2KR1%0402
RREF
38 EAPD
EAPD
SPDIFO1
GPIO0/I2C-DATA-S/I2C-CLK-M/DMIC-DATA/LED-BEAT
GPIO1/DMIC-CLK1
GPIO2/I2C-CLK-S/I2C-CLK-M
GPIO3/SPDIF-OUT/DMIC-DATA2
RA93
10KR0402
38 JD3
JD1
JD2
JD3
JD4
EPAD
PCBEEP
LDOVDD
AVDD-IN
VCC3_CP
CPVDD-IN
CA65 2.2u/6.3X4 V_CPVEE
CPVEE
ECA7 2 100u/10V V_LDO2_VRP
LDO2-VRP
CA10 10u6.3X6 V_LDO2_CAP
LDO2-CAP
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDESURR-R
SIDESURR-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
LINE2-VREFO
MIC1-VREFO-L
MIC2-VREFO
CBP
CBN
CPVREF
LDO1-CAP
VREF
AVSS2
AVSS1
ALOUT_R
ALOUT_L
A_SROUT_R
A_SROUT_L
ECA5
ECA6
10u16V
ASROUT_R
ASROUT_L
A_CEN_OUT
A_BASS
ECA9
ECA8
100u/10V
ACEN_OUT
ABASS
A_LINE_IN_R
A_LINE_IN_L
CA2
CA6
10u6.3X6
LINE_IN_R
LINE_IN_L
A_LINE2_R
A_LINE2_L
ECA3
ECA4
ALINE2_R
ALINE2_L
A_MIC1_R
A_MIC1_L
CA28
CA29
MIC1_R
MIC1_L
A_MIC2_R
A_MIC2_L
CA9
CA11
MIC2_R
MIC2_L
LINE2_VREFO
MIC1_VREFO_L
MIC2_VREFO
CA66 2.2u/6.3X4
CPVREF R2709 0R
V_LDO1_CAP CA71 10u6.3X6
VREF_4080 CA12 10u6.3X6
38 LOUT_L
38 LOUT_R
38 SROUT_L
38 SROUT_R
38 CEN_OUT
38 BASS
LOUT_L RA1 75R/4 LOUT_LA
LOUT_R RA4 75R/4 LOUT_RA
FRONT_JD
DA1 ESD-MLVS0402
DA3 ESD-MLVS0402
AUDIO1E
PORT2
AUDIOJACKX5_SPDIFX1-5
CA74 0.1u/16X4
SROUT_L RA2 75R/4 SROUT_LA
SROUT_R RA3 75R/4 SROUT_RA
SURR_JD
CA57 100p50N4
CA58 100p50N4
AUDIO1B
PORT5
LINE_IN_L RA6 1K/4 LINE_IN_LA
LINE_IN_R RA8 1K/4 LINE_IN_RA
LINE1_JD
CA59 100p50N4
CA60 100p50N4
AUDIO1D
PORT3
CA75 0.1u/16X4
CEN_OUT RA7 75R/4 CEN_OUTA
BASS RA9 75R/4 BASSA
CEN_JD
CA61 100p50N4
CA62 100p50N4
AUDIO1A
PORT4
MIC1_VREF_L RA10 2.2K/4 MIC1_LA
MIC1_VREFO_L
D66 S-BAT54A_SOT23
MIC1_VREF_R RA11 2.2K/4 MIC1_RA
MIC1_L RA31 1K/4
MIC1_R RA32 1K/4
MIC1_JD
AUDIO1F
PORT1
CA63 100p50N4
CA64 100p50N4
SPDIFO1 RA24 10R/4
CA8 100p50N4
VCC5
CA13 0.1u/16X4
AUDIO1C
PORT6
DRIVE IC
ALINE2_R RA47 22K/4
ALINE2_L RA48 22K/4
ACEN_OUT RA25 22K/4
ABASS RA26 22K/4
ASROUT_R RA27 22K/4
ASROUT_L RA28 22K/4
CEN/BAS
LIN_IN
SURR
LIN_OUT
SPDIFO1
MIC1
N58-25F0281-L06
Digital
Analog
5VDUAL LA5 0R/8
ATX_5VSB LA4 X_0R/8
LDOVDD
DA11 ESD-MLVS0402
CA18 0.1u/16X4
CA19 10u6.3X6
VCC5 LA6 0R/8
ALC4080_VBUS
CA67 0.1u/16X4
CA68 0.1u/16X4
Closed Codec
EMI
CA26 X_0.1u16X4
CA27 X_1000p16X4
L25
120L1.5A-150_0402-HF
D3V3
RA94 100KR1%0402 JD1 RA100 200KR1%0402 FRONT_JD
RA98 100KR1%0402 SURR_JD
RA95 100KR1%0402 JD2 RA101 200KR1%0402 MIC1_JD
RA99 100KR1%0402 CEN_JD
RA96 100KR1%0402 JD3
RA97 100KR1%0402 JD4 RA102 200KR1%0402 LINE1_JD
Pin5 Pin47
CA69 1u/6.3X4
CA23 0.1u/16X4
CA70 2.2u/6.3X4
VCC3 Pin9
CA14 10u6.3X6
CA15 0.1u/16X4
LDO3_CAP Pin4
CA16 10u6.3X6
LDOVDD Pin19
CA20 0.1u/16X4
CA21 10u6.3X6
VCC3_CP Pin36
CA24 10u6.3X6
CA25 0.1u/16X4
U91 X_GS7150XST-ADJ-R_SOT23-5-HF
VDD VOUT EN GND FB
CA72 X_1u/6.3X4
R2710 X_47KR0402
CA73 X_2.2u/6.3X4
C1180 X_680p/50X4
R2711 X_10KR1%0402
C1179 X_C4.7U10X5-HF
R2712 X_3.16KR1%0402-RH
3VSB R2713 0R VCC3_CP
MSI
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MS-7D54
Size Custom
Document Description
Audio ALC1220
Rev 11
Date Friday June 04 2021
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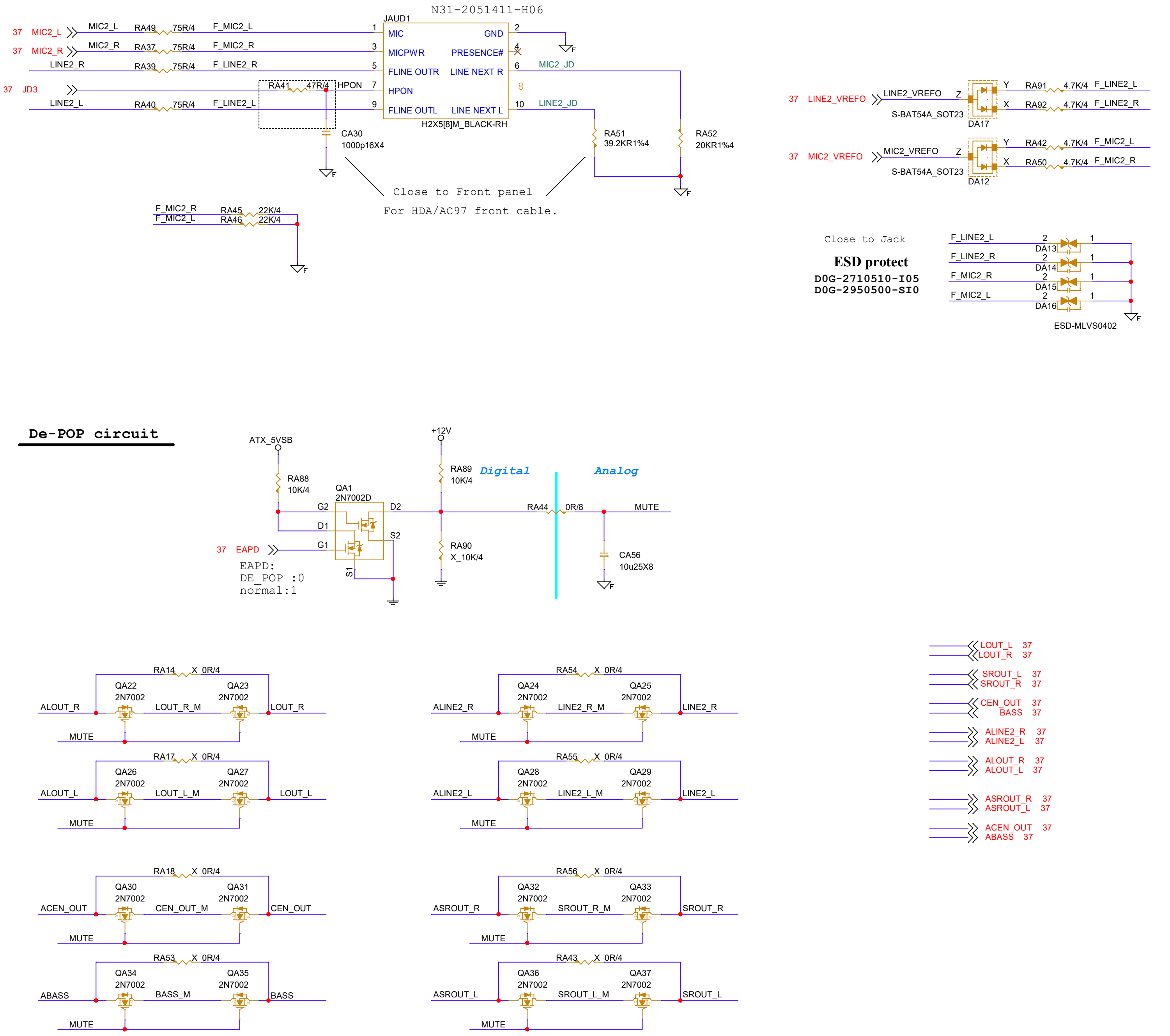

MSI	MICRO-STAR INT'L CO.,LTD
	MS-7D54
Size: Custom	Document Description: Audio DePop — Rev 11
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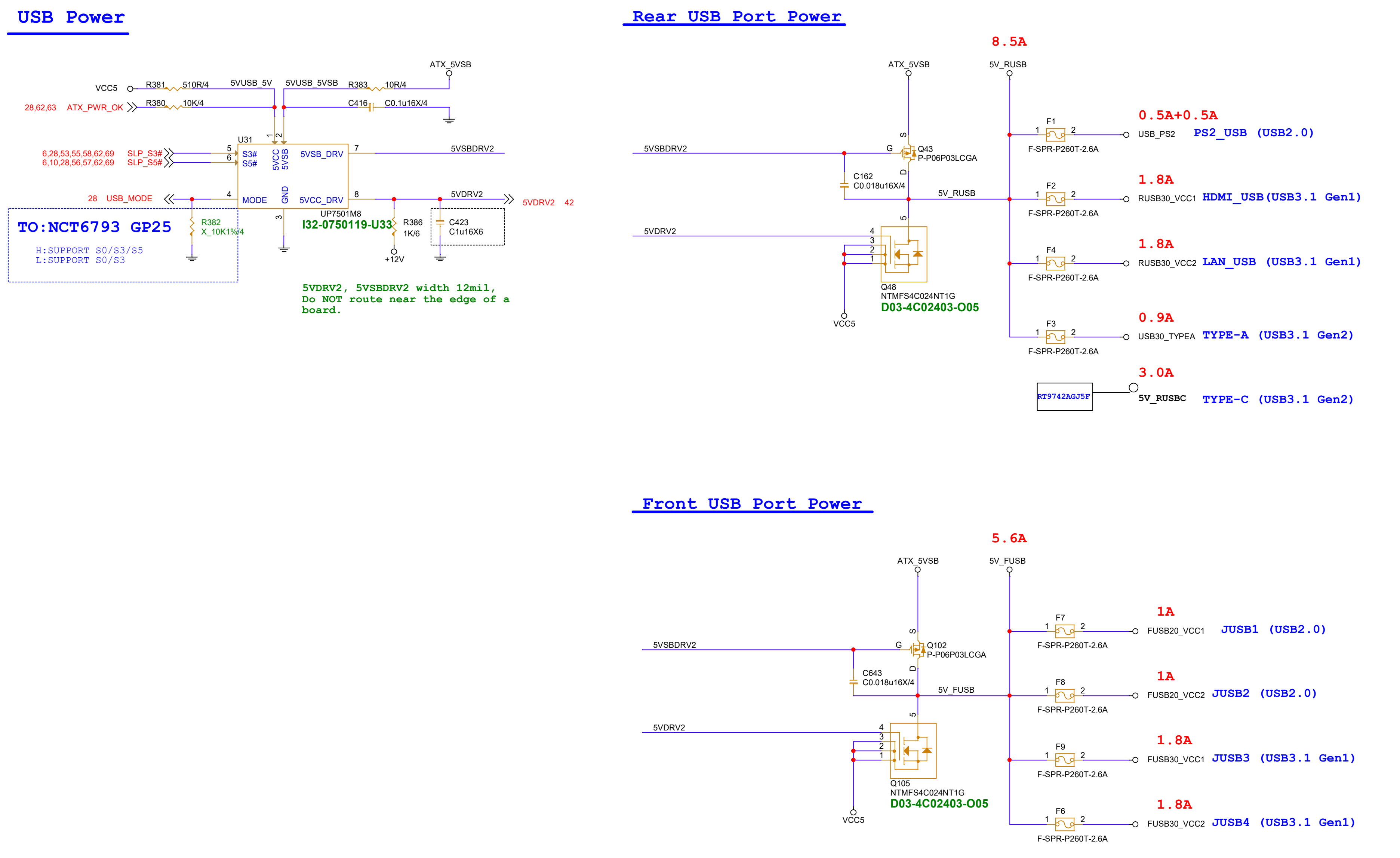

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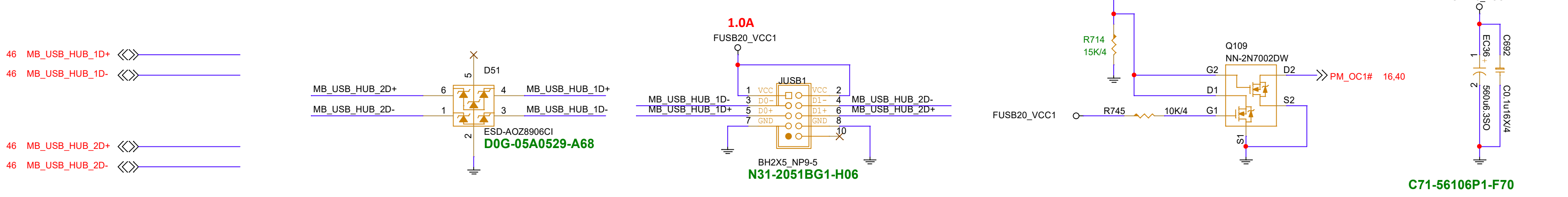
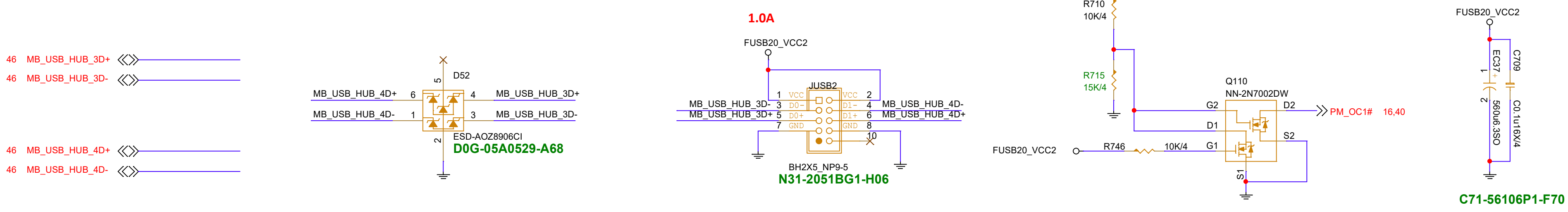
Front USB2.0(JUSB1)



Front USB2.0(JUSB2)



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Size	Document Description	Rev
Custom	Front USB2.0 Header	11

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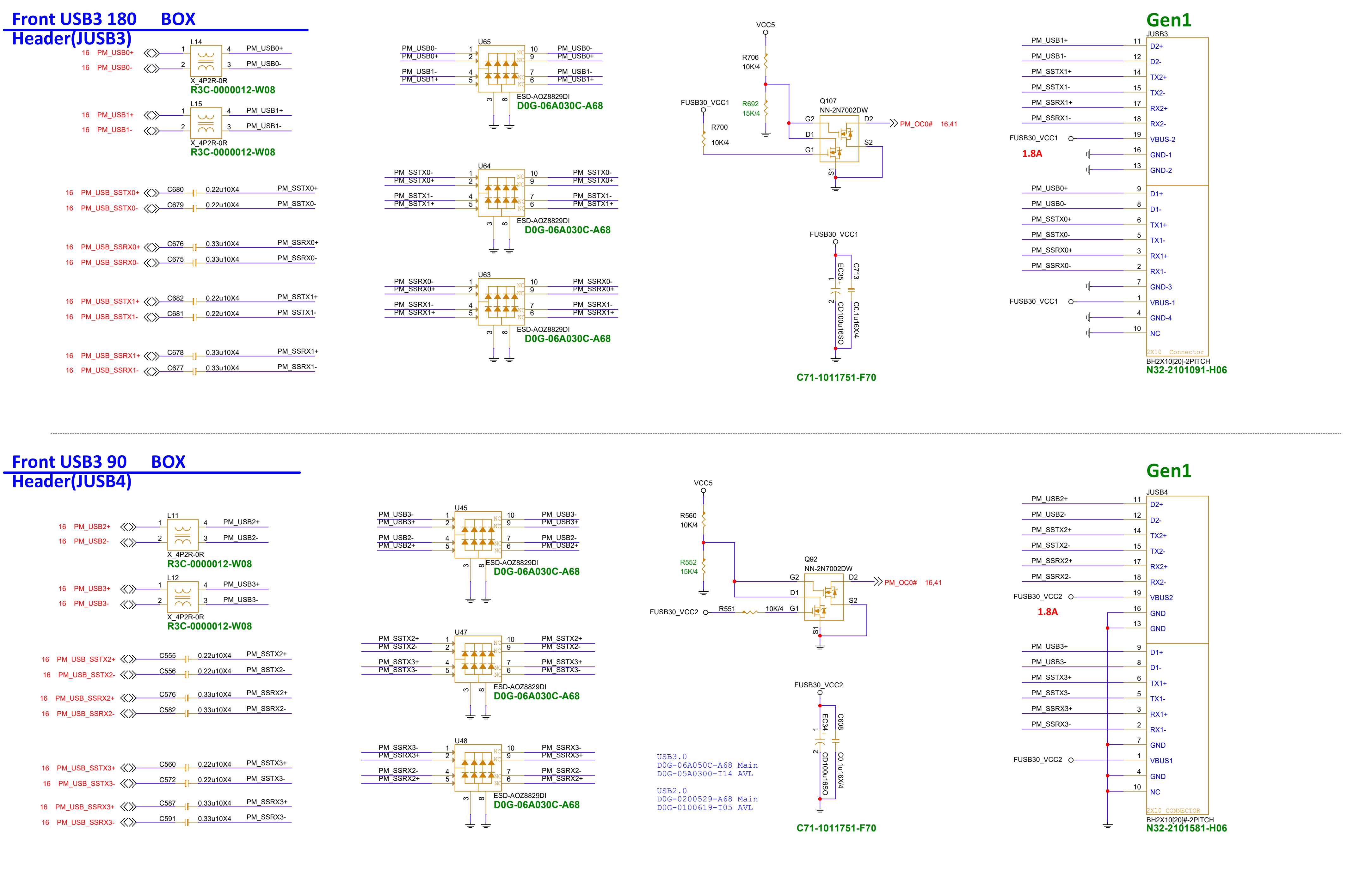

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Size: Custom	Document Description: Front USB3.0 Header	Rev: 11
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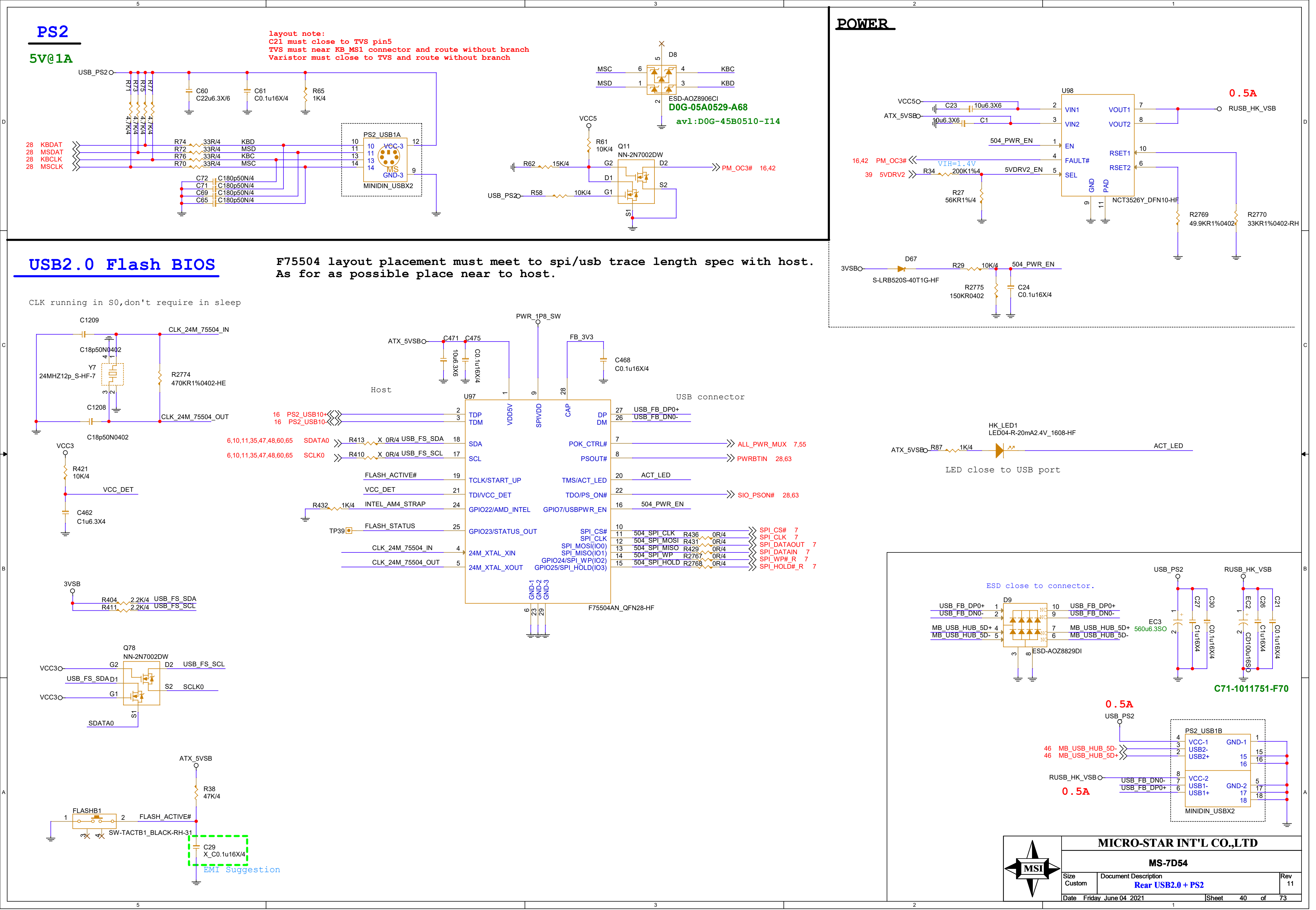

PS2
5V@1A
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch
USB_PS2
C60 C22u6.3X6
C61 C0.1u16X/4
R65 1K/4
R71 R73 R75 R77 4.7K/4
28 KBDAT
28 MSDAT
28 KBCLK
28 MSCLK
R74 33R/4 KBD
R72 33R/4 MSD
R76 33R/4 KBC
R70 33R/4 MSC
C72 C180p50N/4
C71 C180p50N/4
C69 C180p50N/4
C65 C180p50N/4
PS2_USB1A
MINIDIN_USBX2
VCC-3
GND-3
MS
D8
ESD-AOZ8906CI
D0G-05A0529-A68
avl:D0G-45B0510-I14
VCC5
R61 10K/4
Q11 NN-2N7002DW
R62 15K/4
R58 10K/4
PM_OC3# 16,42
POWER
U98
NCT3526Y_DFN10-HF
VCC5
ATX_5VSB
C23 10u6.3X6
C1 10u6.3X6
VIN1 VIN2 EN FAULT# SEL VOUT1 VOUT2 RSET1 RSET2 GND PAD
504_PWR_EN
16,42 PM_OC3#
39 5VDRV2
VIH=1.4V
R34 200K1%/4
5VDRV2_EN
R27 56KR1%/4
0.5A
RUSB_HK_VSB
R2769 49.9KR1%0402
R2770 33KR1%0402-RH
3VSB
D67 S-LRB520S-40T1G-HF
R29 10K/4
R2775 150KR0402
C24 C0.1u16X/4
USB2.0 Flash BIOS
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.
CLK running in S0,don't require in sleep
C1209 C18p50N0402
Y7 24MHZ12p_S-HF-7
R2774 470KR1%0402-HE
C1208 C18p50N0402
CLK_24M_75504_IN
CLK_24M_75504_OUT
VCC3
R421 10K/4
VCC_DET
C462 C1u6.3X4
PWR_1P8_SW
ATX_5VSB
C471 10u6.3X6
C475 C0.1u16X/4
FB_3V3
C468 C0.1u16X/4
Host
USB connector
U97
F75504AN_QFN28-HF
16 PS2_USB10+
16 PS2_USB10-
TDP TDM VDD5V SPIVDD CAP DP DM
USB_FB_DP0+
USB_FB_DN0-
6,10,11,35,47,48,60,65 SDATA0
6,10,11,35,47,48,60,65 SCLK0
R413 X_0R/4 USB_FS_SDA
R410 X_0R/4 USB_FS_SCL
SDA SCL POK_CTRL# PSOUT#
ALL_PWR_MUX 7,55
PWRBTIN 28,63
FLASH_ACTIVE#
TCLK/START_UP
TMS/ACT_LED
ACT_LED
TDI/VCC_DET
TDO/PS_ON#
SIO_PSON# 28,63
R432 1K/4
INTEL_AM4_STRAP
GPIO22/AMD_INTEL
GPIO7/USBPWR_EN
504_PWR_EN
TP39
FLASH_STATUS
GPIO23/STATUS_OUT
SPI_CS# SPI_CLK SPI_MOSI(IO0) SPI_MISO(IO1) GPIO24/SPI_WP(IO2) GPIO25/SPI_HOLD(IO3)
24M_XTAL_XIN
24M_XTAL_XOUT
504_SPI_CLK R436 0R/4 SPI_CS# 7
504_SPI_MOSI R431 0R/4 SPI_CLK 7
504_SPI_MISO R429 0R/4 SPI_DATAOUT 7
504_SPI_WP R2767 0R/4 SPI_DATAIN 7
504_SPI_HOLD R2768 0R/4 SPI_WP#_R 7
SPI_HOLD#_R 7
GND-1 GND-2 GND-3
HK_LED1
LED04-R-20mA2.4V_1608-HF
ATX_5VSB R87 1K/4
ACT_LED
LED close to USB port
3VSB
R404 2.2K/4 USB_FS_SDA
R411 2.2K/4 USB_FS_SCL
Q78 NN-2N7002DW
VCC3
USB_FS_SDA
USB_FS_SCL
SCLK0
SDATA0
ATX_5VSB
R38 47K/4
FLASHB1
SW-TACTB1_BLACK-RH-31
FLASH_ACTIVE#
C29 X_C0.1u16X/4
EMI Suggestion
ESD close to connector.
USB_PS2
RUSB_HK_VSB
D9
ESD-AOZ8829DI
USB_FB_DP0+
USB_FB_DN0-
MB_USB_HUB_5D+
MB_USB_HUB_5D-
EC3 560u6.3SO
C27 C1u16X4
C30 C0.1u16X4
EC2 CD100u16SO
C26 C1u16X4
C21 C0.1u16X4
C71-1011751-F70
0.5A
USB_PS2
PS2_USB1B
MINIDIN_USBX2
46 MB_USB_HUB_5D-
46 MB_USB_HUB_5D+
VCC-1 USB2- USB2+ GND-1
VCC-2 USB1- USB1+ GND-2
RUSB_HK_VSB
0.5A
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MS-7D54
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Rear USB2.0 + PS2
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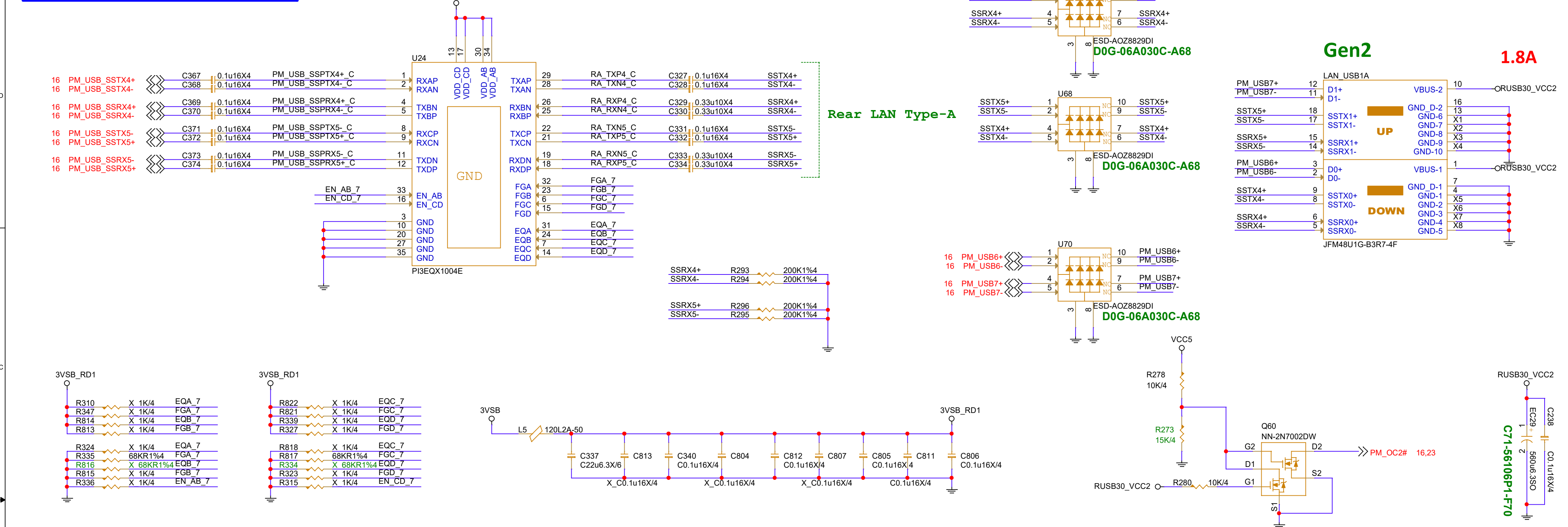
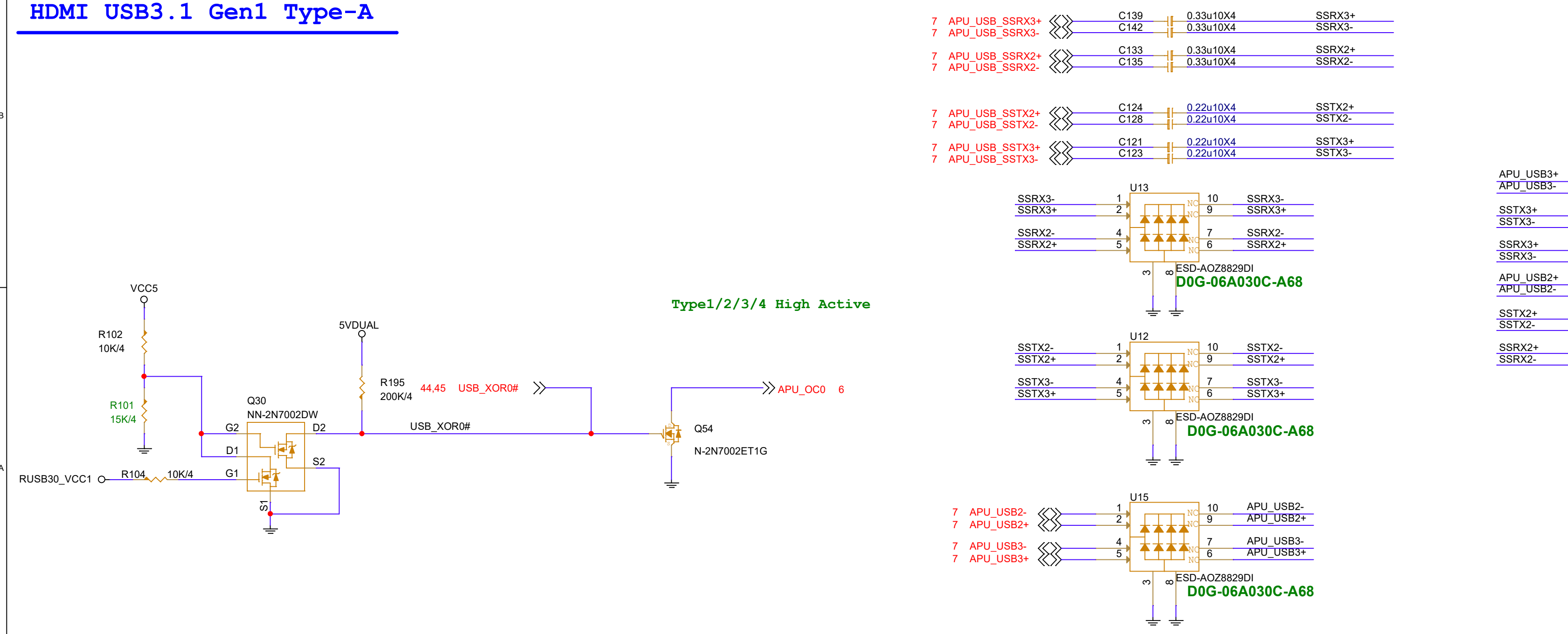
LAN USB3.1 Gen2 Type-A



HDMI USB3.1 Gen1 Type-A



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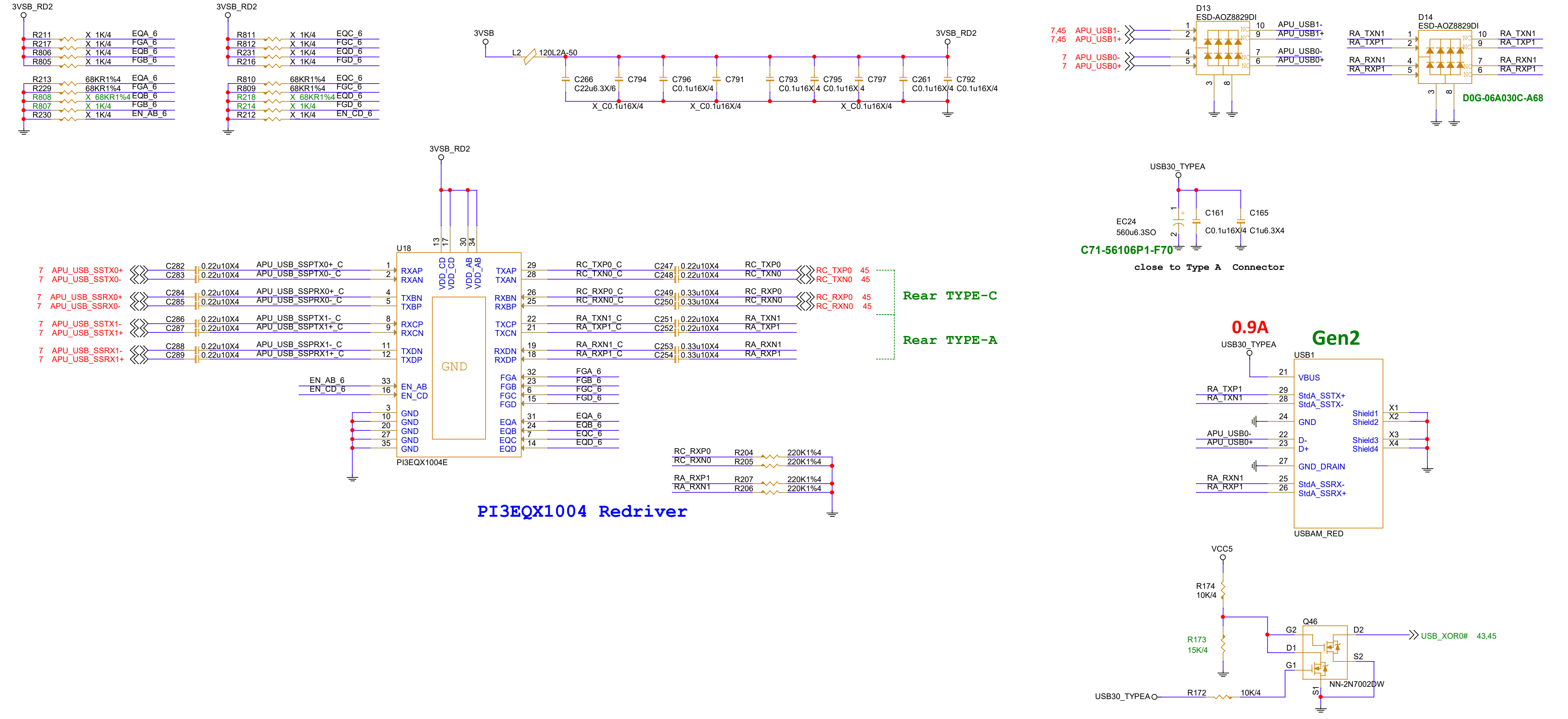
USB3.1 Gen2 Redriver + Type-A



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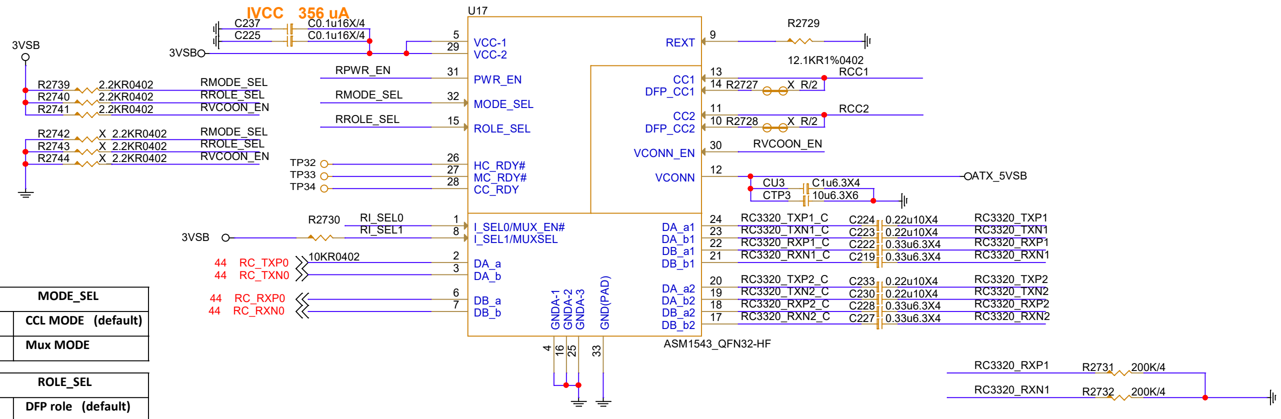
MS-7D54			
Size: Custom	Document Description: Rear USB3.1 Type A / redrive		Rev: 11
Date: Friday June 04 2021	Sheet 42 of 73		

USB3.1 Gen2 Type-C

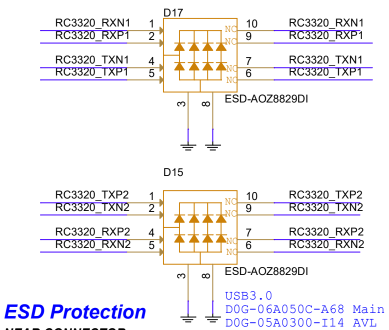
USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

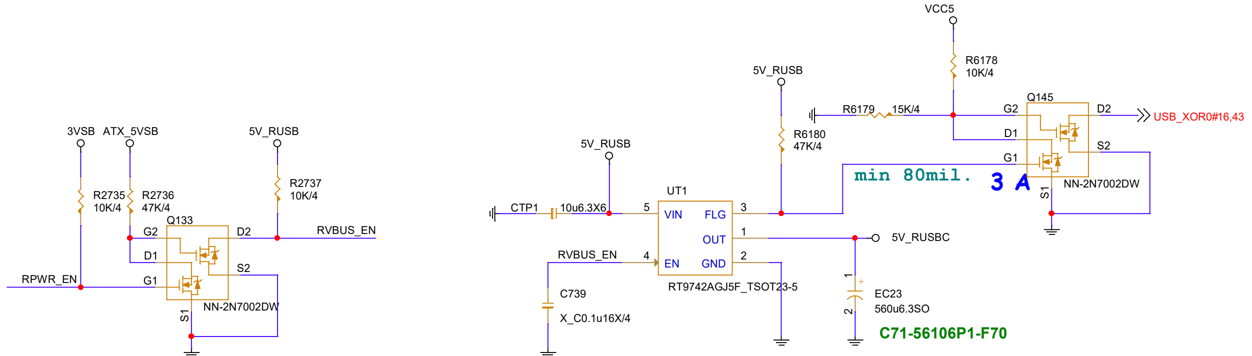
VCONN_EN	
1	enable
0	disable

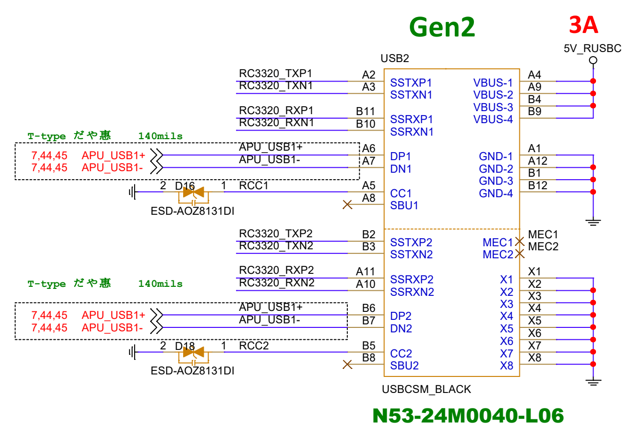


ESD Protection

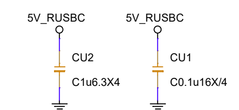
NEAR CONNECTOR

VBUS EN



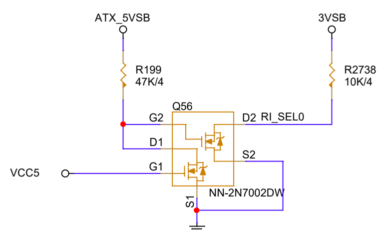


close to Type C Connector



Current Mode

I_SEL0	I_SEL1	
X	0	900mA
0	1	1.5A,5V
1	1	3A,5V



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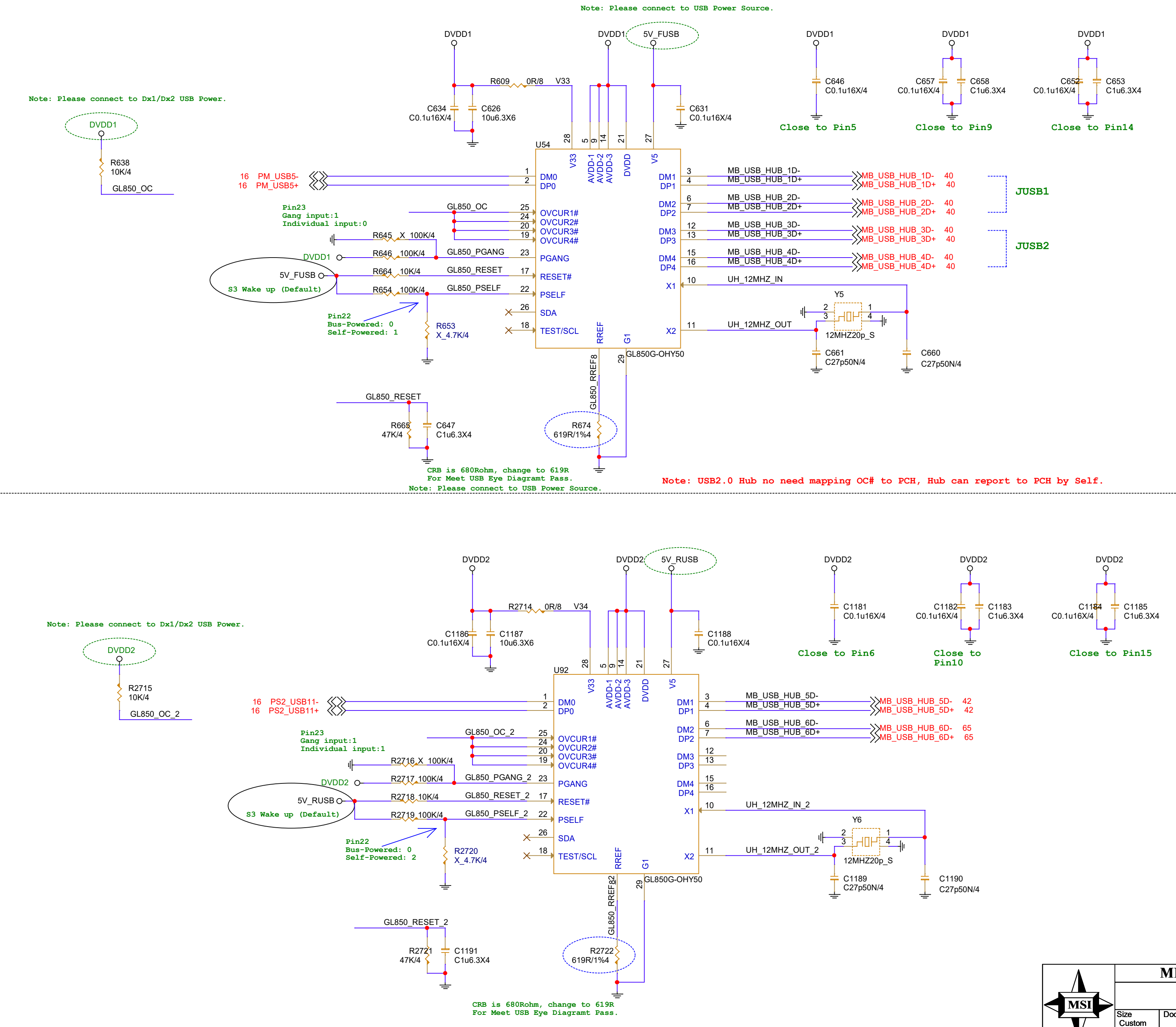
GL850G USB2.0 HUB

5V_FUSB



MICRO-STAR INT'L CO.,LTD	
MS-7D54	
Size Custom	Document Description GL850G — Rev 11
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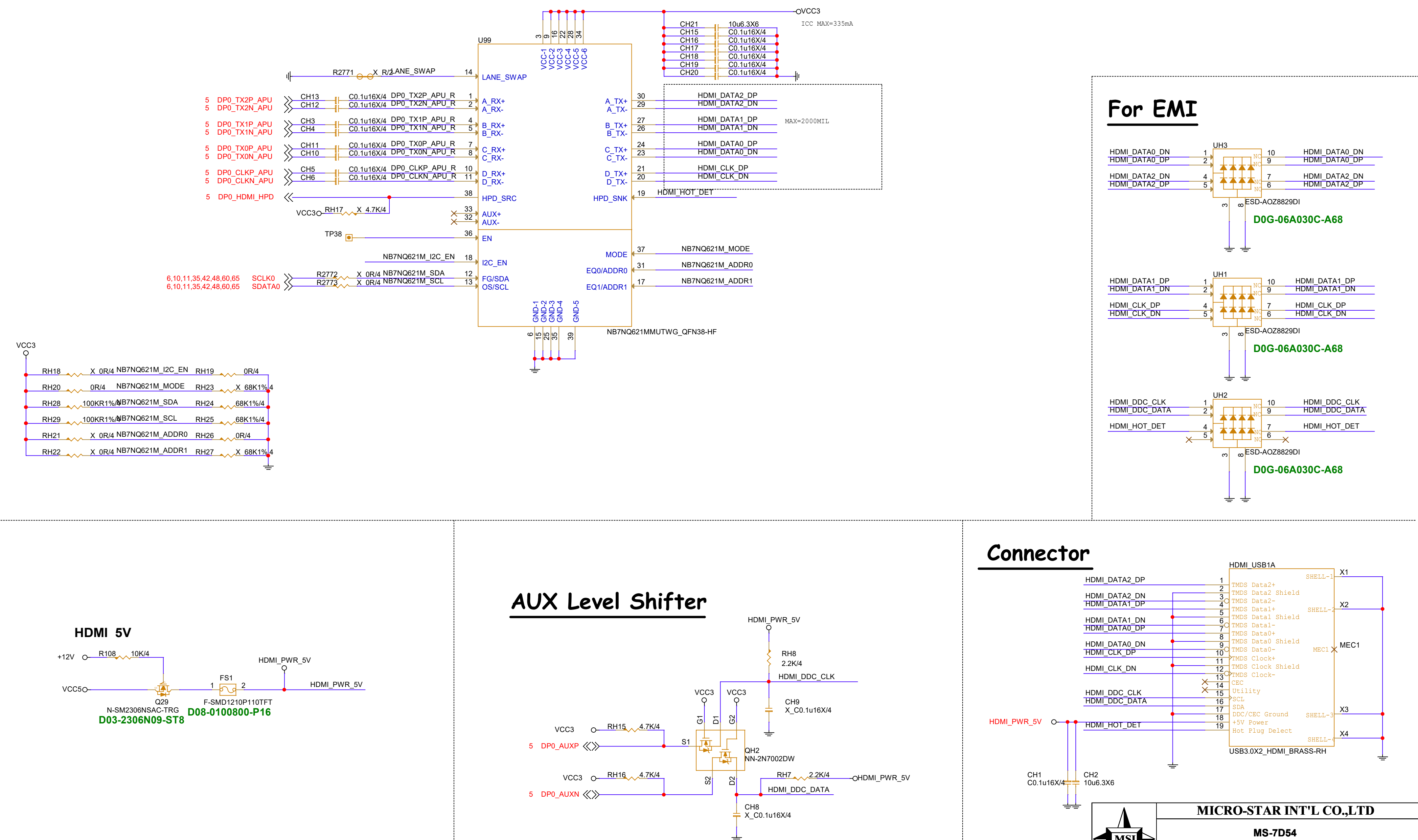
HDMI CONNECTOR

For HDMI 2.1



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	HDMI	11

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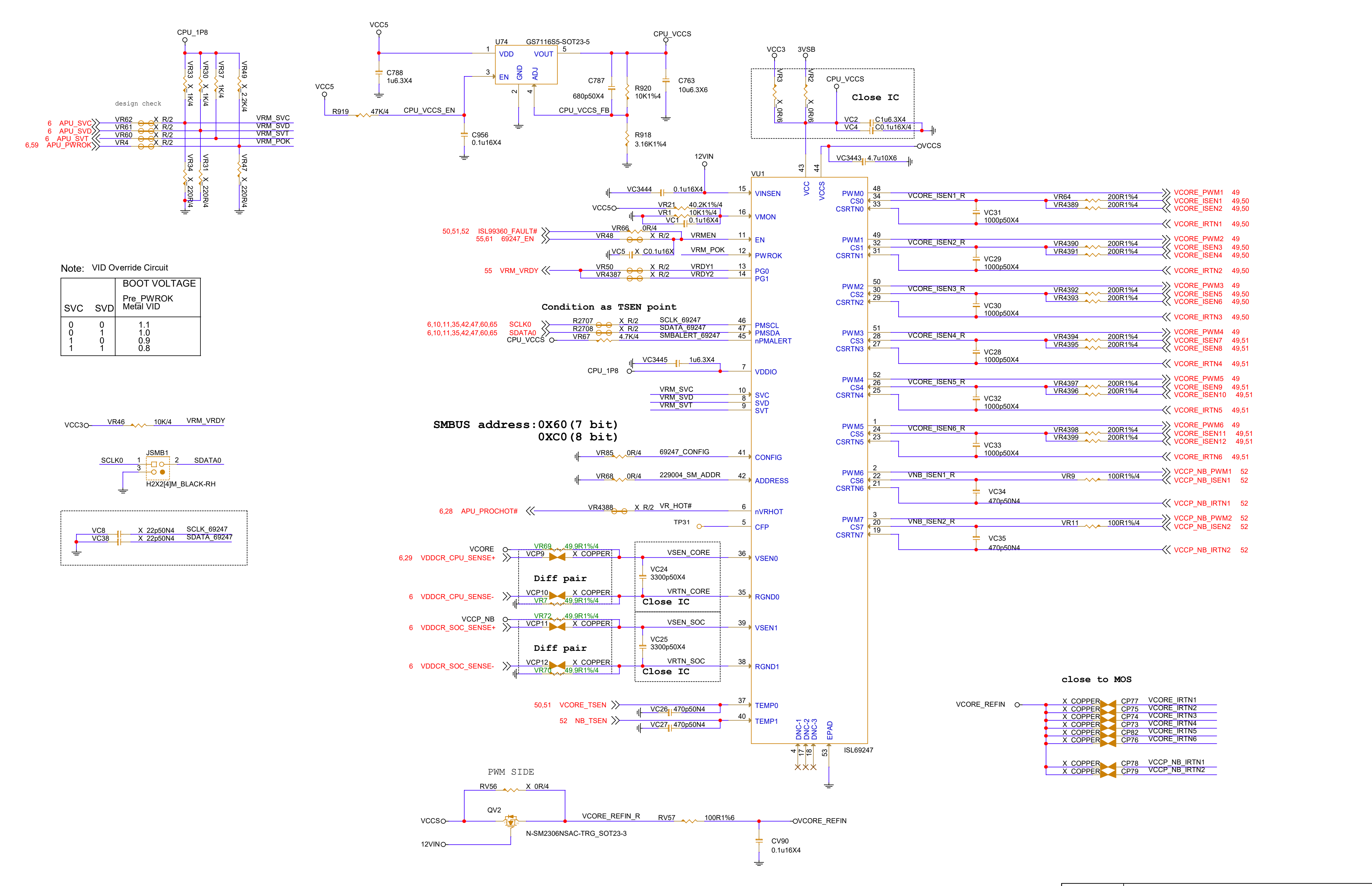

Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

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CPU_CORE Driver IC

VCORE Double 12-PHASE

MICRO-STAR INT'L CO.,LTD		
MS-7D54		
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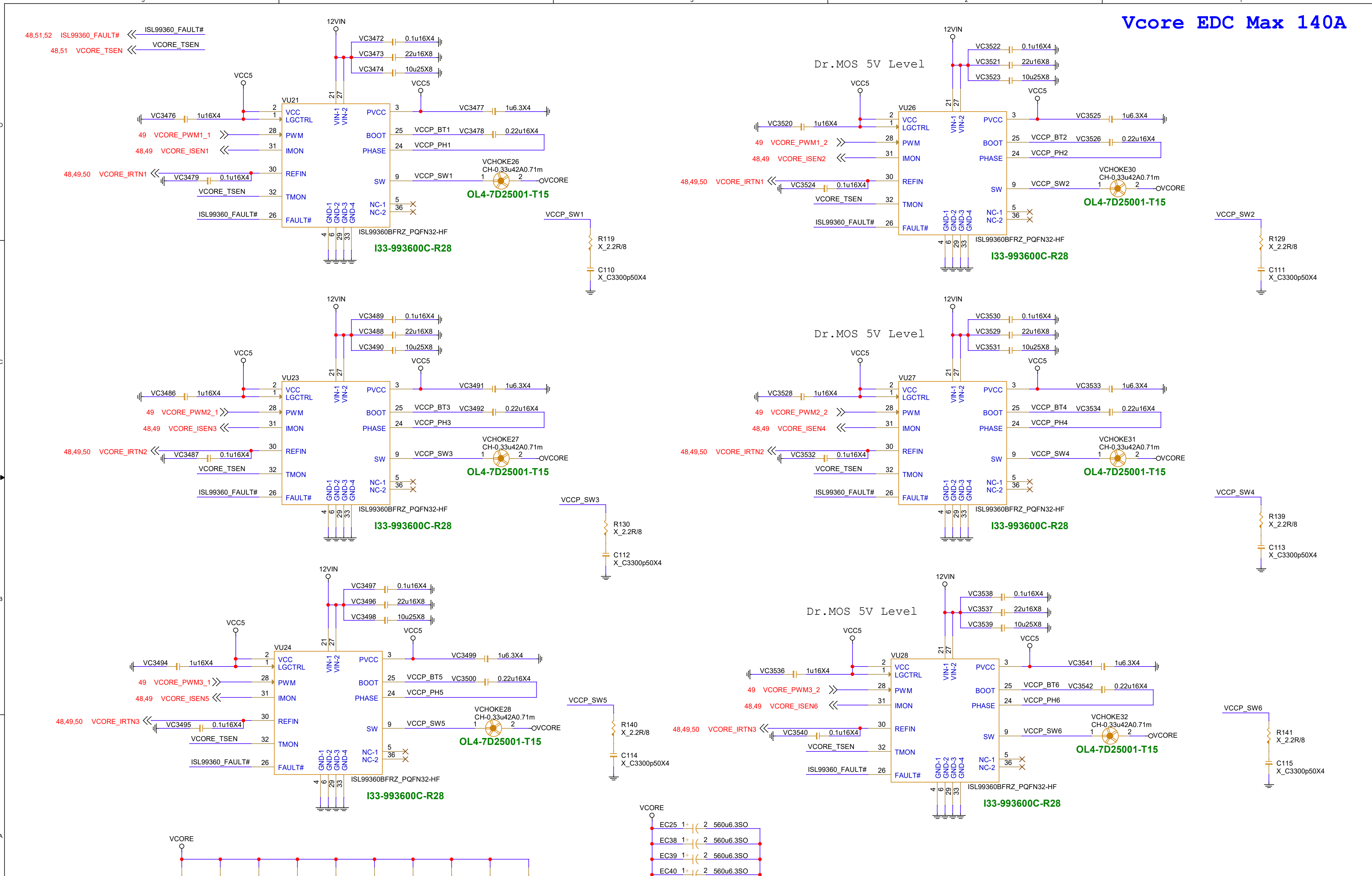
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power Vocre Phase 1-6	11

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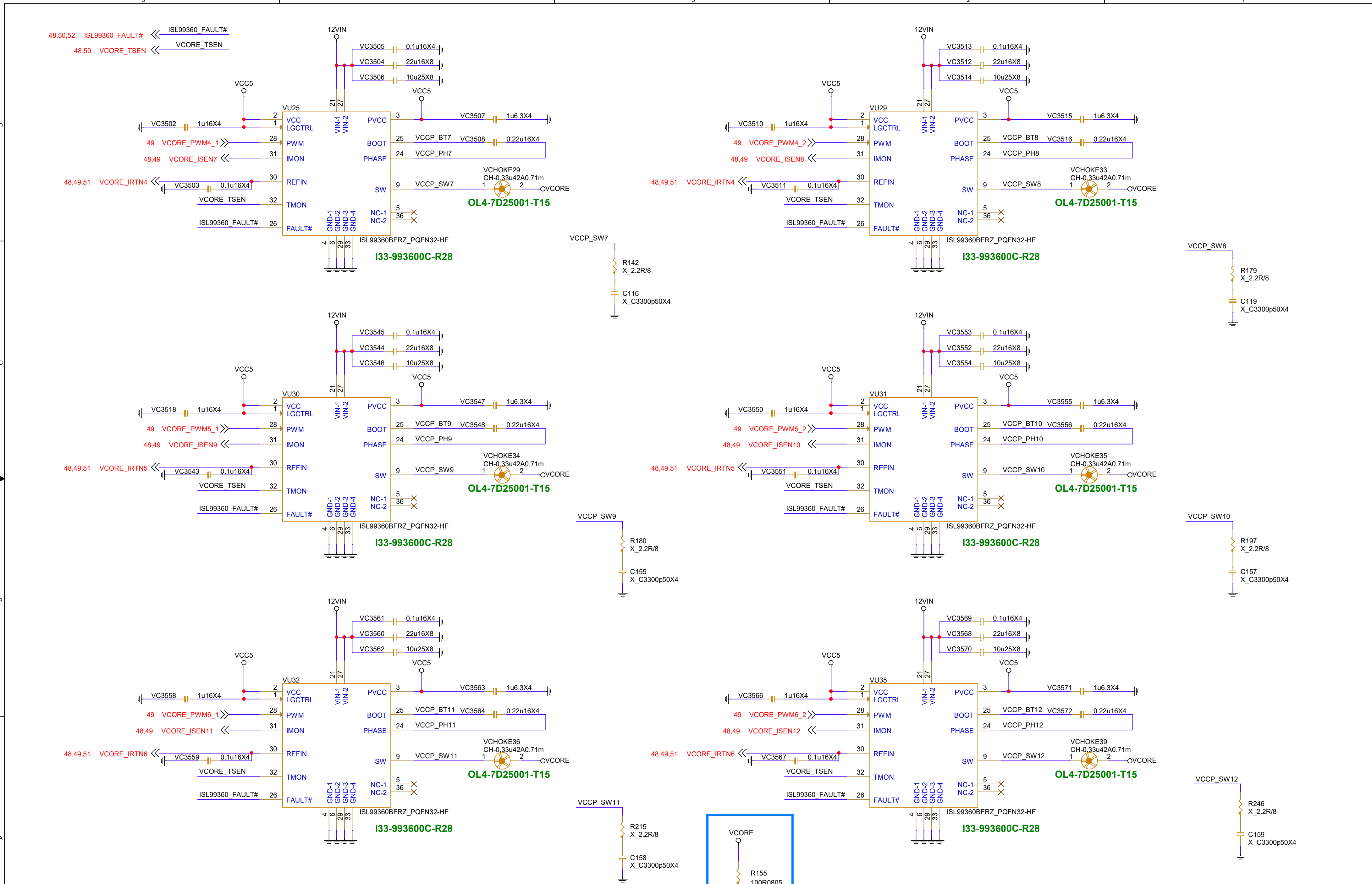

MICRO-STAR INT'L CO.,LTD		
MS-7D54		
Size: Custom	Document Description: CPU Power Vocre Phase 7 - 10	Rev: 11
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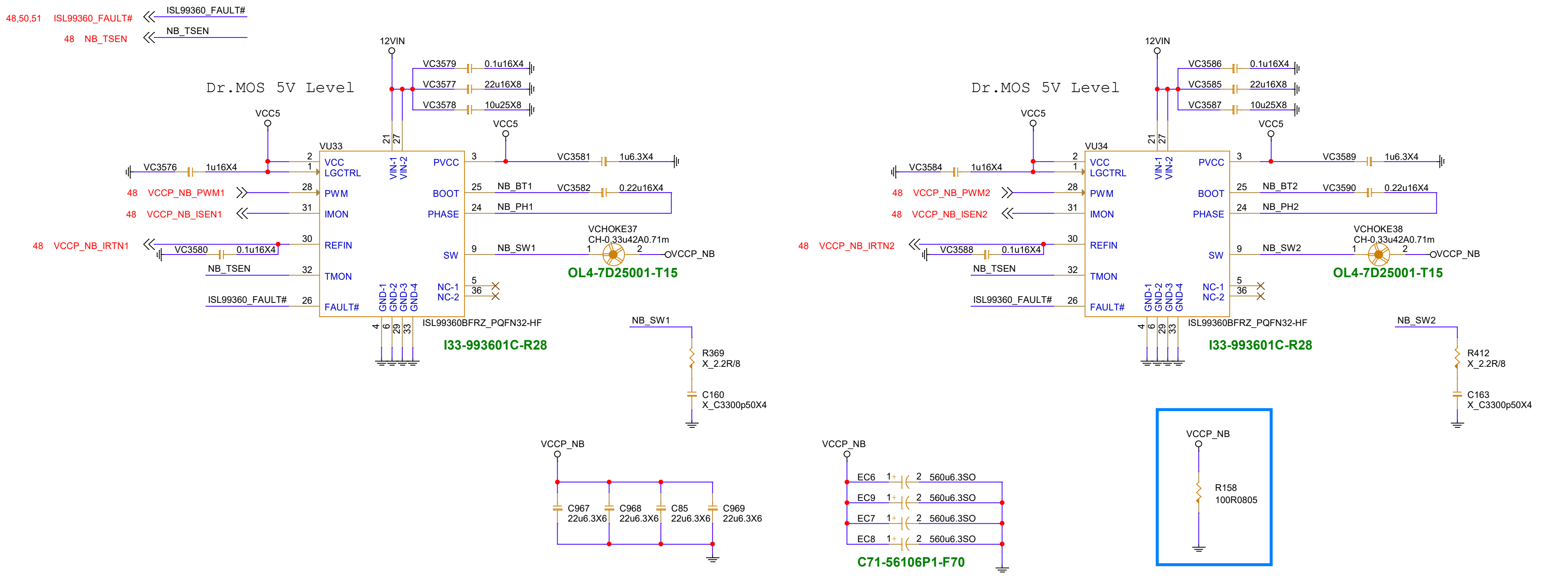

MICRO-STAR INT'L CO.,LTD

MS-7D54

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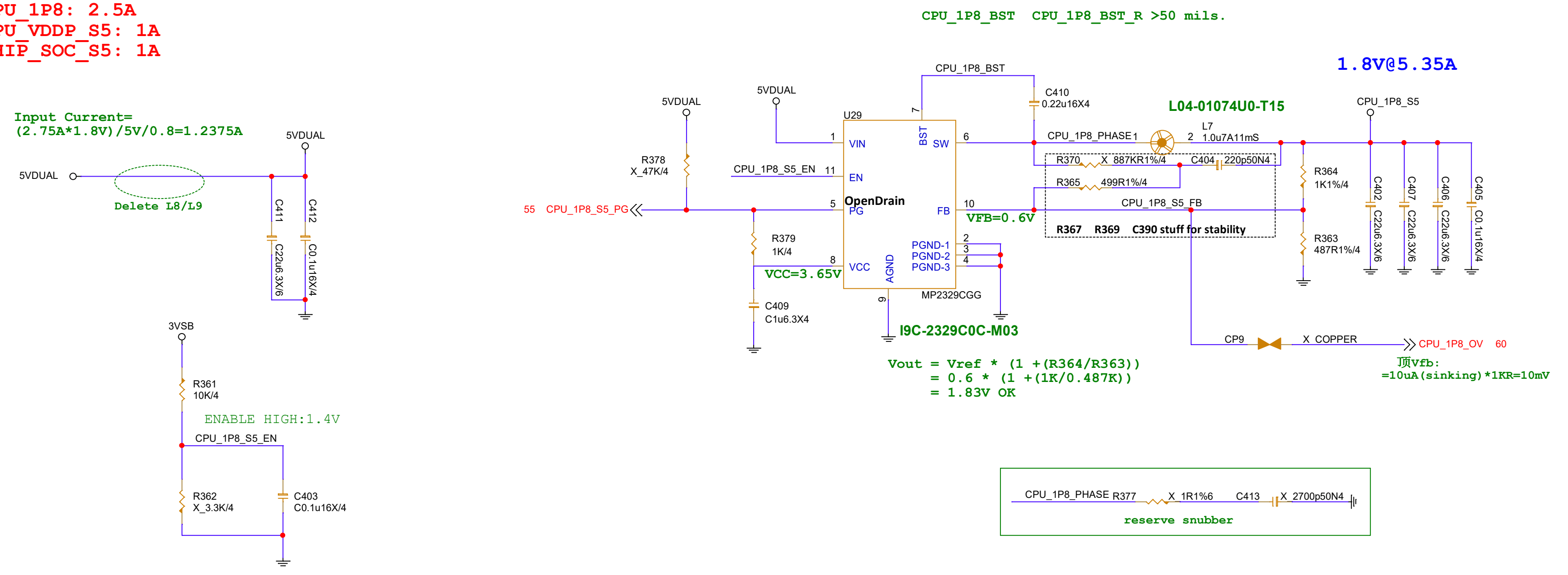
CPU 1P8V S5

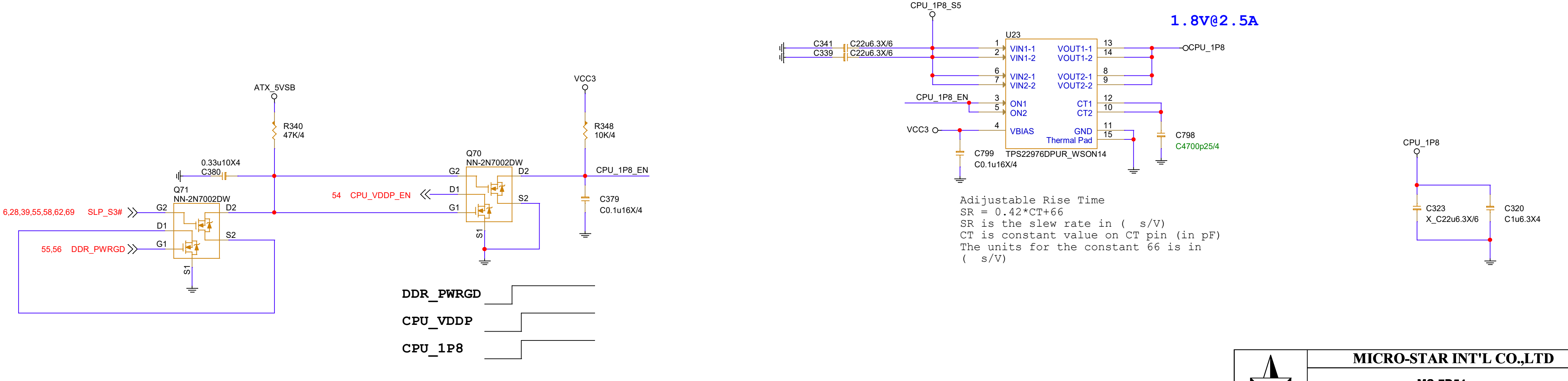
CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A

CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A



CPU 1P8V

CPU: VDD_18@2A
CHIP: VDD_18@0.5A



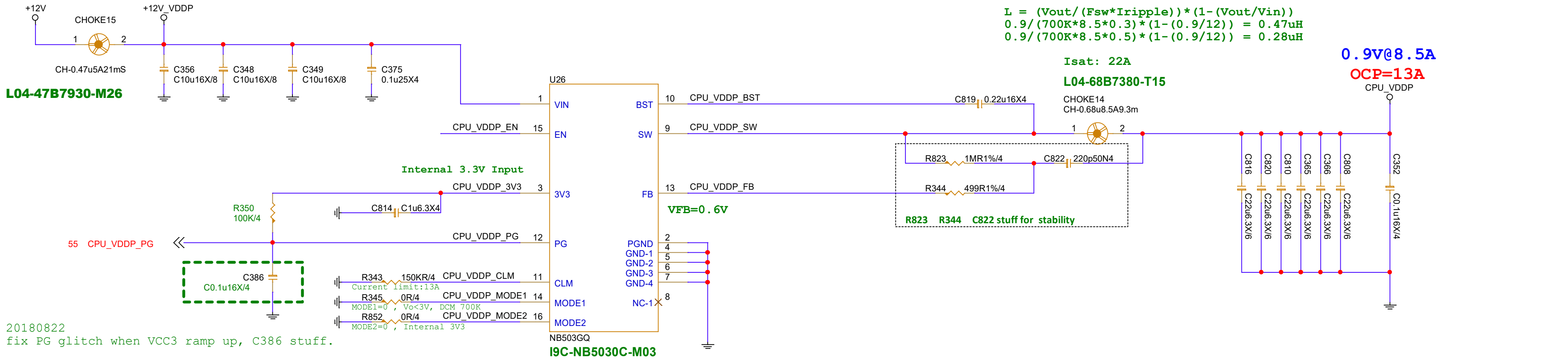
Adjustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (s/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in
(s/V)

CPU_VDDP

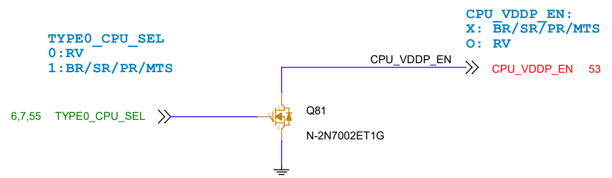
CPU: VDDP@8.5A

Input Current = (8.5A*0.9V)/12V/0.8 = 0.8A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A

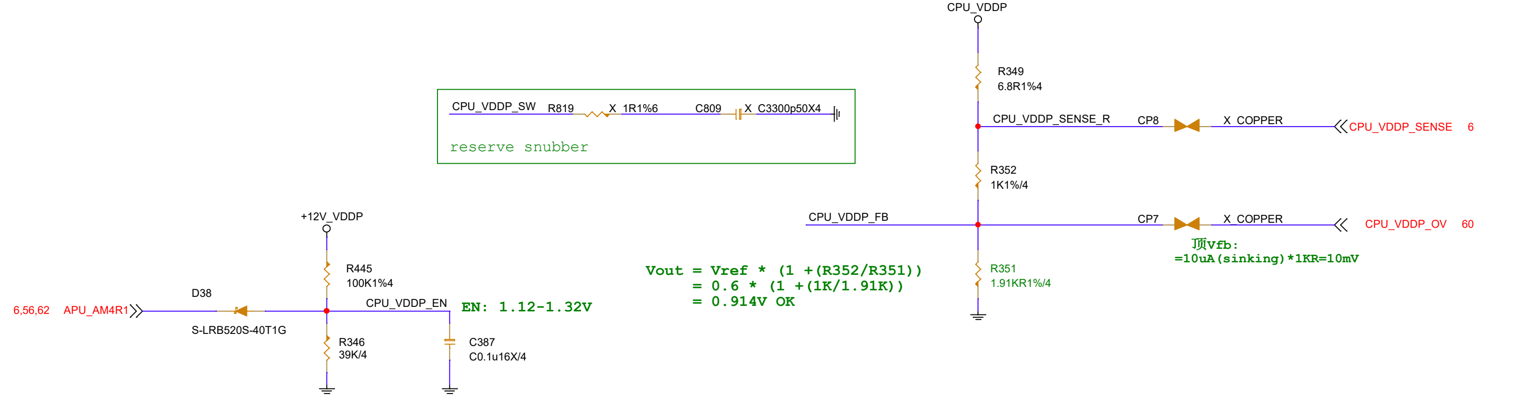
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH



No support BR SPEC



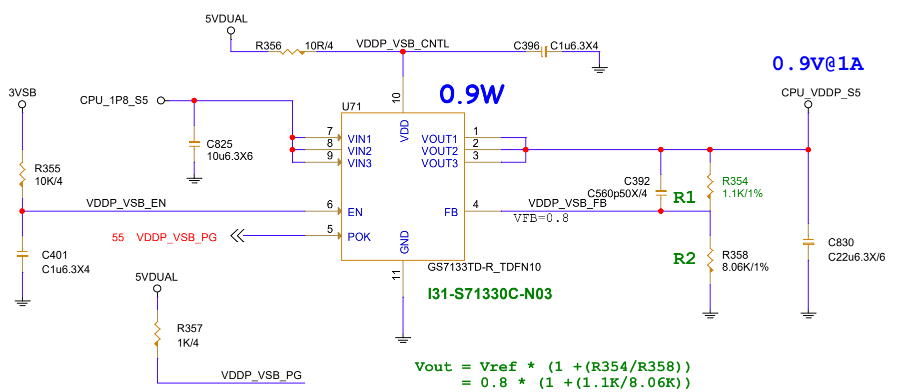
CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
~~BR~~	~~0~~	~~1~~	~~1~~	SPEC no Support
NA	X	0		0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	
RV/ZP	3	0	1	1
MTS	4	1	CPU VDDP NOT SUPPORT TYPE4	0



Vout = Vref * (1 +(R352/R351))
= 0.6 * (1 +(1K/1.91K))
= 0.914V OK

CPU_VDDP_S5

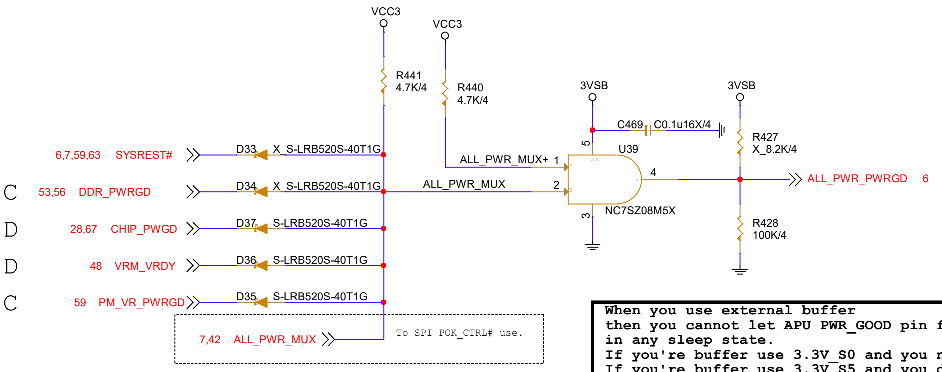
CPU: VDDP_S5@1A



Vout = Vref * (1 +(R354/R358))
= 0.8 * (1 +(1.1K/8.06K))
= 0.909V OK

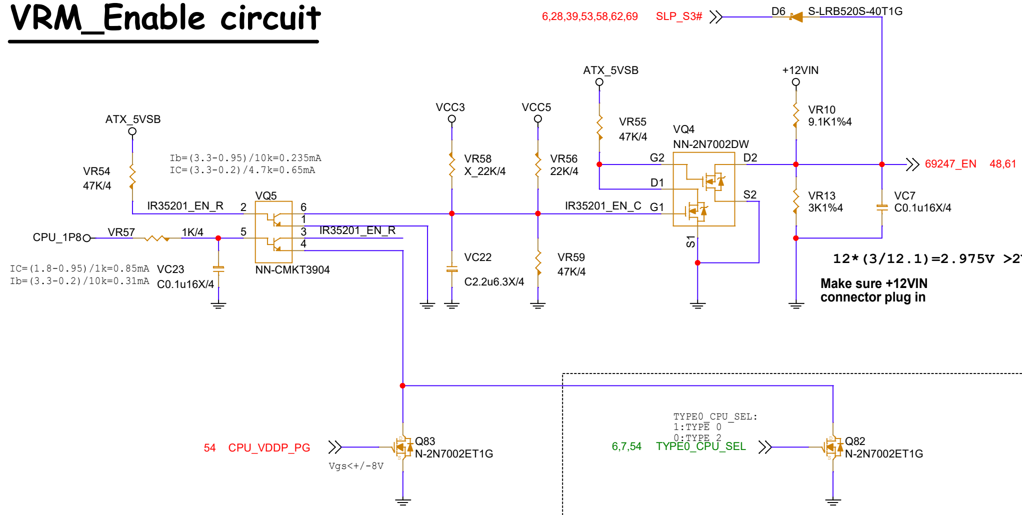
ALL POWER GOOD MUX

S0 PG



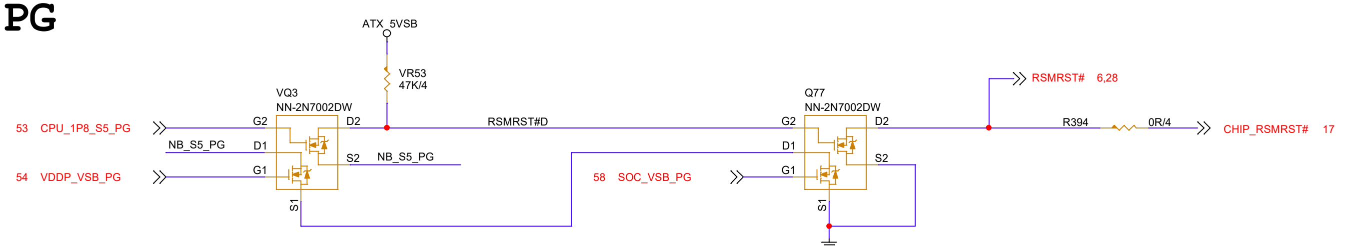

```
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.
```

VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~BR~~	~~0~~	~~0~~ SPEC no Support	~~1~~
NA	X	0	0
SR	2	1 CPU VDDP NOT SUPPORT TYPE2	1
RV/ZP	3	1	0
MTS	4	1 CPU VDDP NOT SUPPORT TYPE4	1

S5 PG



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VCC DDR

15.5A For CPU
9.5A For 4DIMM
1.2A For DDR VTT

OCP = 39.3A; Choke Isat=42A

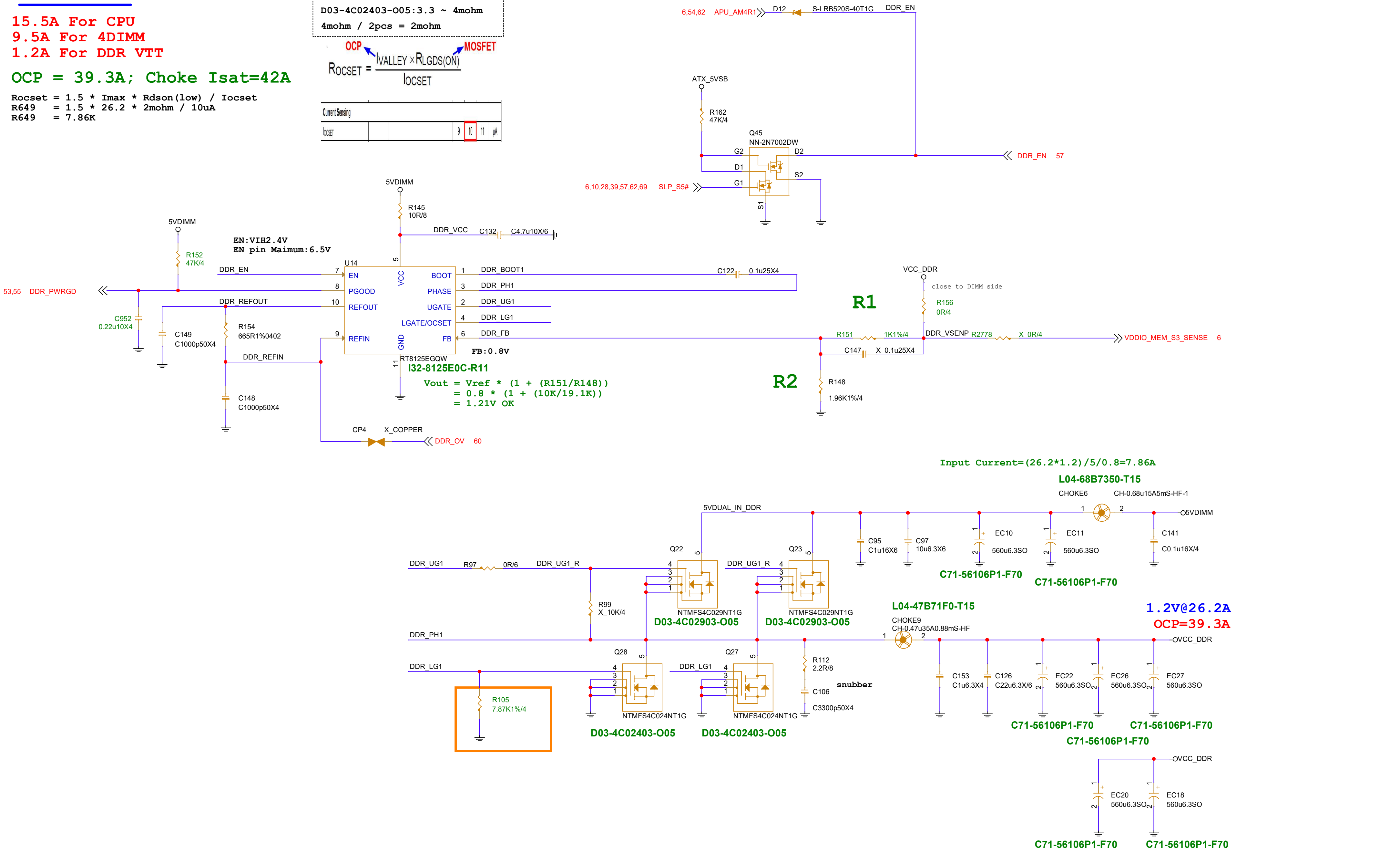
Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649 = 1.5 * 26.2 * 2mohm / 10uA
R649 = 7.86K

Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~ 4mohm
4mohm / 2pcs = 2mohm

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

OCP MOSFET

Current Sensing						
IOCSET			9	10	11	μA



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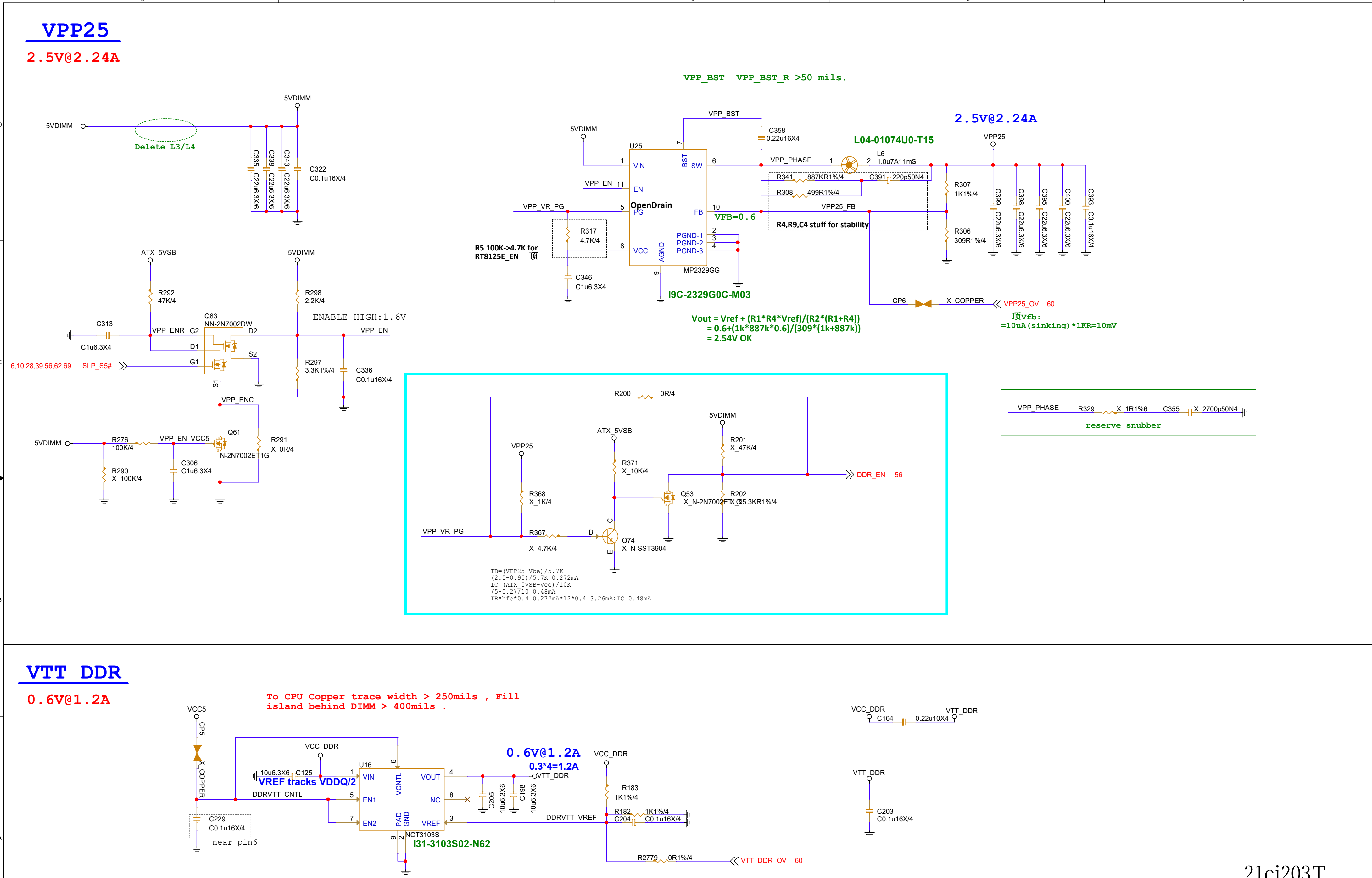

21ci203T

MICRO-STAR INT'L CO.,LTD

MS-7D54

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Custom	DDR VPP25 / VTT	11

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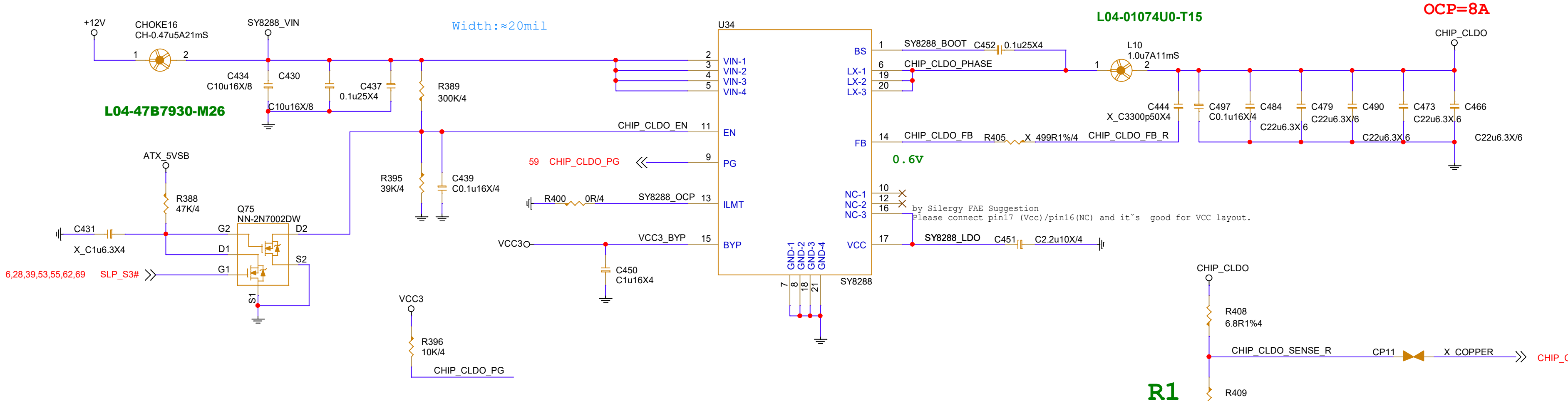
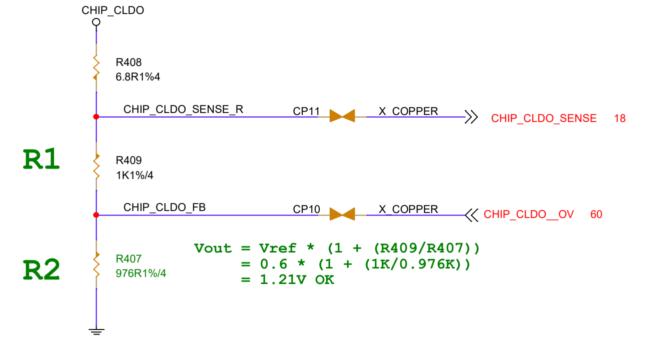
CHIP_CLDO

CHIP: VDD_CLDO@5A

Input Current= (5.5A*1.05V)/12V/0.8=0.625A



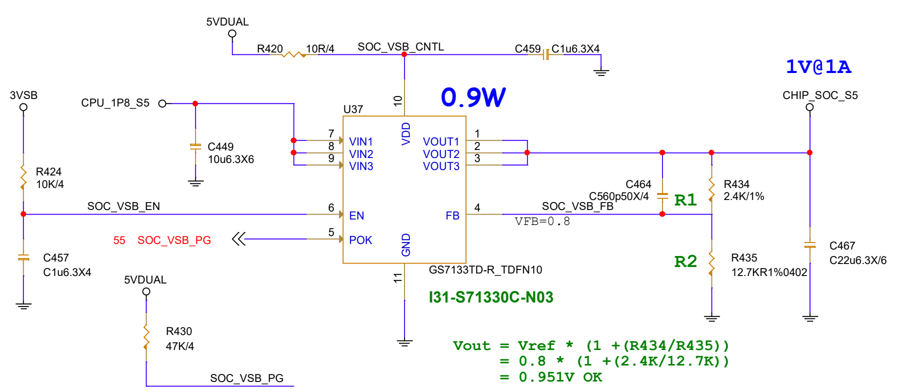


$$Vout = Vref * (1 + (R409/R407)) = 0.6 * (1 + (1K/0.976K)) = 1.21V \text{ OK}$$

SY8288_OCP	OCP
0	8A
floating	12A
1	16A

CHIP_SOC_S5

CHIP: VDDCR_SOC_S5@1A



$$Vout = Vref * (1 + (R434/R435)) = 0.8 * (1 + (2.4K/12.7K)) = 0.951V \text{ OK}$$

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Size: Custom	Document Description: PROM - SY8288RAC / 1.05V	Rev: 11
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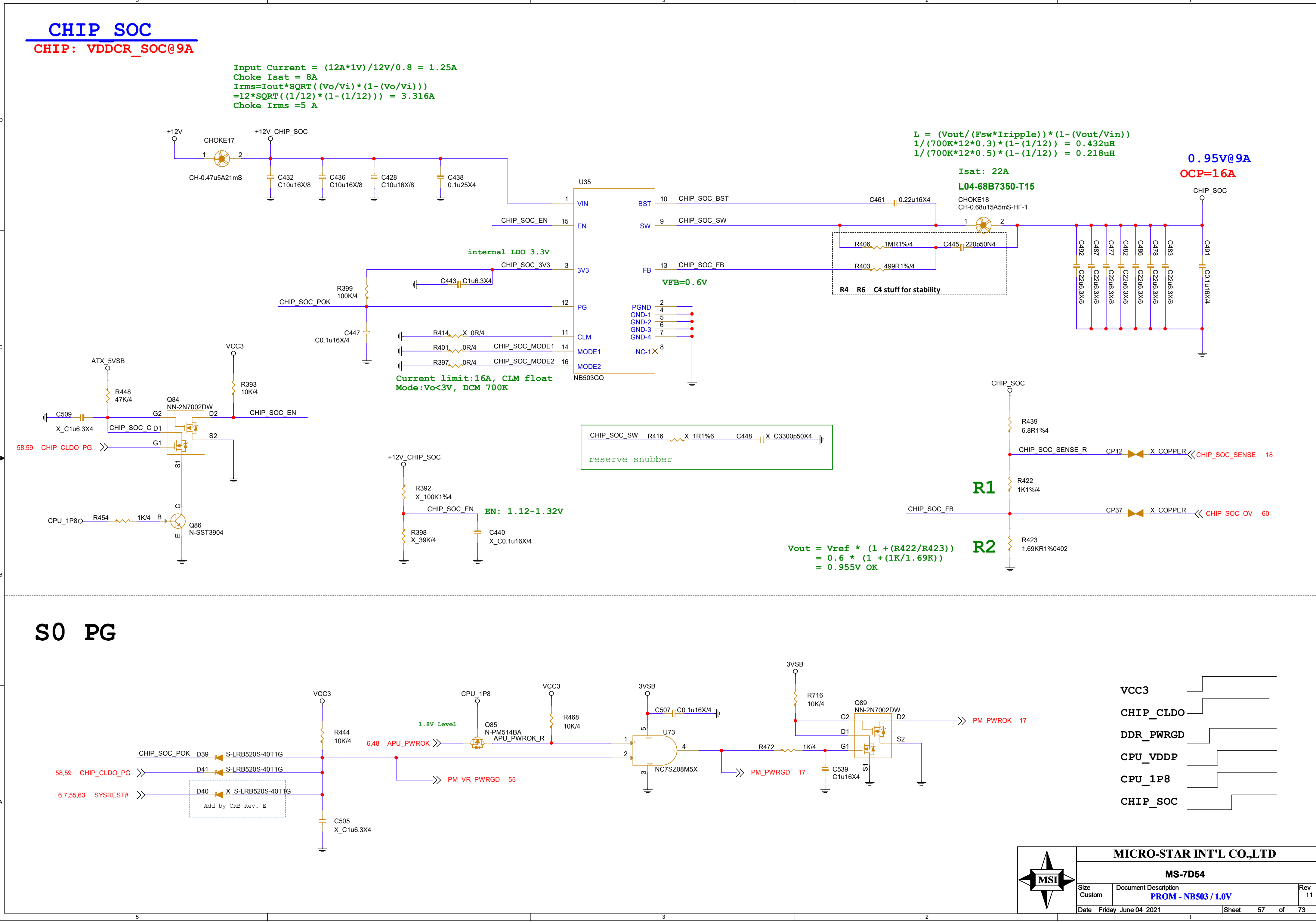

CHIP_SOC
CHIP: VDDCR_SOC@9A
Input Current = (12A*1V)/12V/0.8 = 1.25A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=12*SQRT((1/12)*(1-(1/12))) = 3.316A
Choke Irms =5 A
+12V
CHOKE17
CH-0.47u5A21mS
+12V_CHIP_SOC
C432 C10u16X/8
C436 C10u16X/8
C428 C10u16X/8
C438 0.1u25X4
U35
VIN
EN
3V3
PG
CLM
MODE1
MODE2
BST
SW
FB
PGND
GND-1
GND-2
GND-3
GND-4
NC-1
NB503GQ
CHIP_SOC_EN
CHIP_SOC_3V3
CHIP_SOC_POK
CHIP_SOC_BST
CHIP_SOC_SW
CHIP_SOC_FB
internal LDO 3.3V
C443 C1u6.3X4
R399 100K/4
C447 C0.1u16X/4
R414 X_0R/4
R401 0R/4 CHIP_SOC_MODE1
R397 0R/4 CHIP_SOC_MODE2
Current limit:16A, CLM float
Mode:Vo<3V, DCM 700K
VFB=0.6V
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
1/(700K*12*0.3)*(1-(1/12)) = 0.432uH
1/(700K*12*0.5)*(1-(1/12)) = 0.218uH
Isat: 22A
L04-68B7350-T15
CHOKE18
CH-0.68u15A5mS-HF-1
C461 0.22u16X4
R406 1MR1%/4
C445 220p50N4
R403 499R1%/4
R4 R6 C4 stuff for stability
0.95V@9A
OCP=16A
CHIP_SOC
C492 C487 C477 C482 C486 C478 C483 C22u6.3X/6
C491 C0.1u16X/4
ATX_5VSB
VCC3
R448 47K/4
R393 10K/4
Q84 NN-2N7002DW
C509 X_C1u6.3X4
CHIP_SOC_C
58,59 CHIP_CLDO_PG
CPU_1P8 R454 1K/4
Q86 N-SST3904
+12V_CHIP_SOC
R392 X_100K1%4
R398 X_39K/4
C440 X_C0.1u16X/4
EN: 1.12-1.32V
CHIP_SOC_SW R416 X_1R1%6 C448 X_C3300p50X4
reserve snubber
R439 6.8R1%4
CHIP_SOC_SENSE_R CP12 X_COPPER CHIP_SOC_SENSE 18
R1
R422 1K1%/4
CP37 X_COPPER CHIP_SOC_OV 60
R2
R423 1.69KR1%0402
Vout = Vref * (1 +(R422/R423))
= 0.6 * (1 +(1K/1.69K))
= 0.955V OK
S0 PG
VCC3
R444 10K/4
CHIP_SOC_POK D39 S-LRB520S-40T1G
58,59 CHIP_CLDO_PG D41 S-LRB520S-40T1G
6,7,55,63 SYSREST# D40 X_S-LRB520S-40T1G
Add by CRB Rev. E
C505 X_C1u6.3X4
CPU_1P8
1.8V Level
Q85 N-PM514BA
6,48 APU_PWROK
APU_PWROK_R
PM_VR_PWRGD 55
R468 10K/4
3VSB
C507 C0.1u16X/4
U73 NC7SZ08M5X
PM_PWRGD 17
R472 1K/4
C539 C1u16X4
R716 10K/4
Q89 NN-2N7002DW
PM_PWROK 17
VCC3
CHIP_CLDO
DDR_PWRGD
CPU_VDDP
CPU_1P8
CHIP_SOC
MICRO-STAR INT'L CO.,LTD
MSI
MS-7D54
Size Custom
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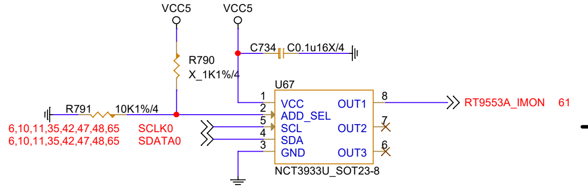
Over Voltage Control IC

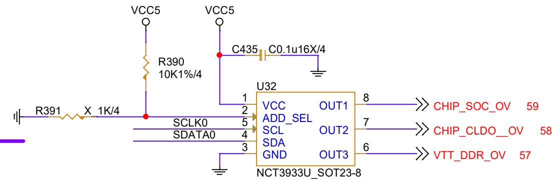
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS SEL	0%	25%	40%	60%	75%	100%

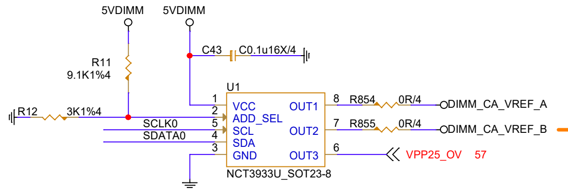
0x2A:RH=OPEN,RL=10K



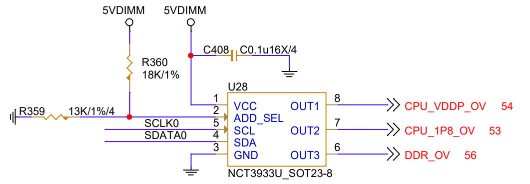
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



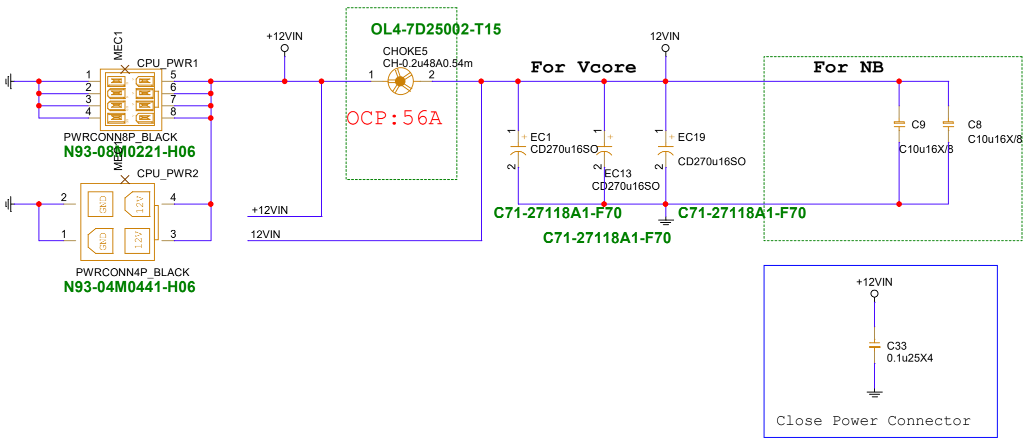
0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE

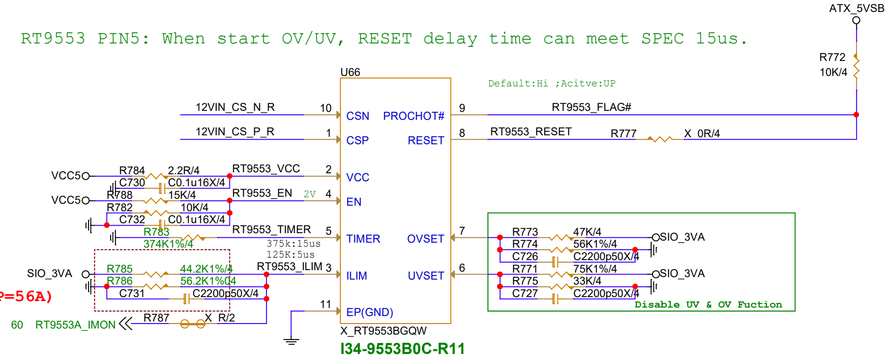
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS SEL	0%	25%	40%	60%	75%	100%

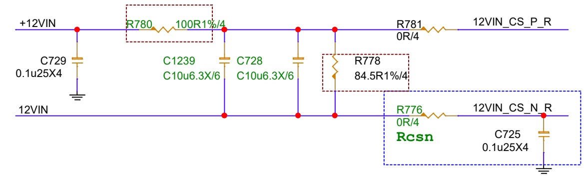
CPU POWER CONNECTOR



RT9553B CURRENT SENSE

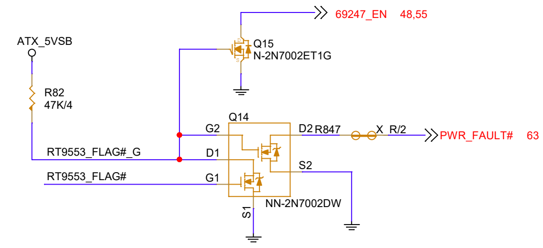
RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.





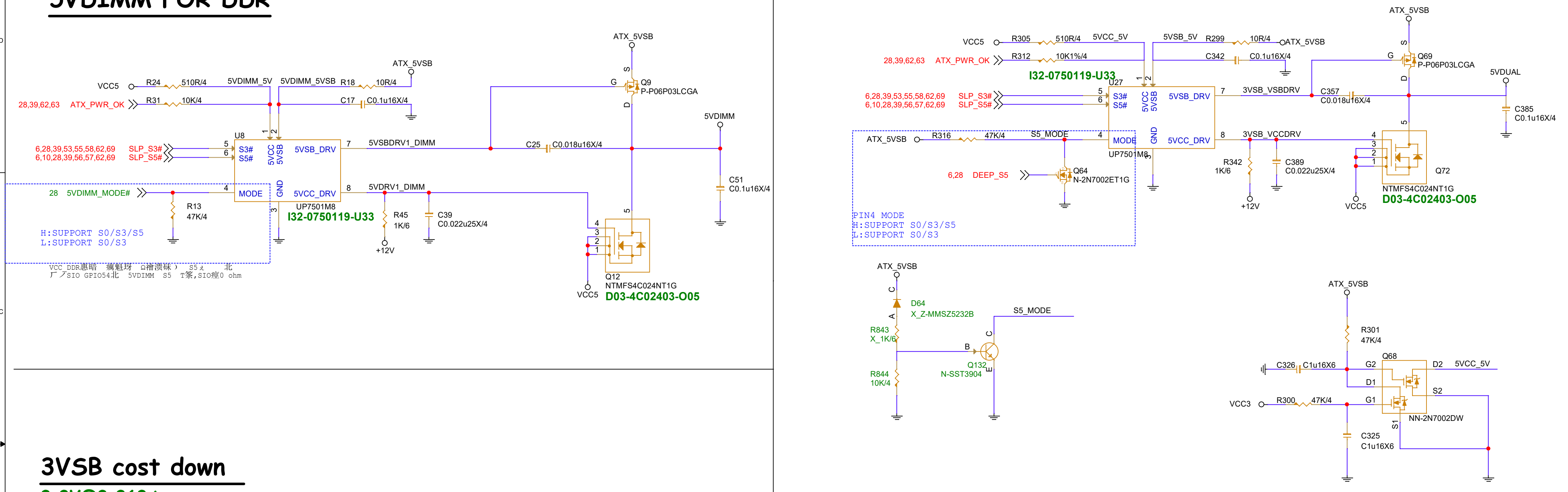
Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.



5VDIMM FOR DDR

5VDUAL For 3VSB CPU 1.8V VDDP

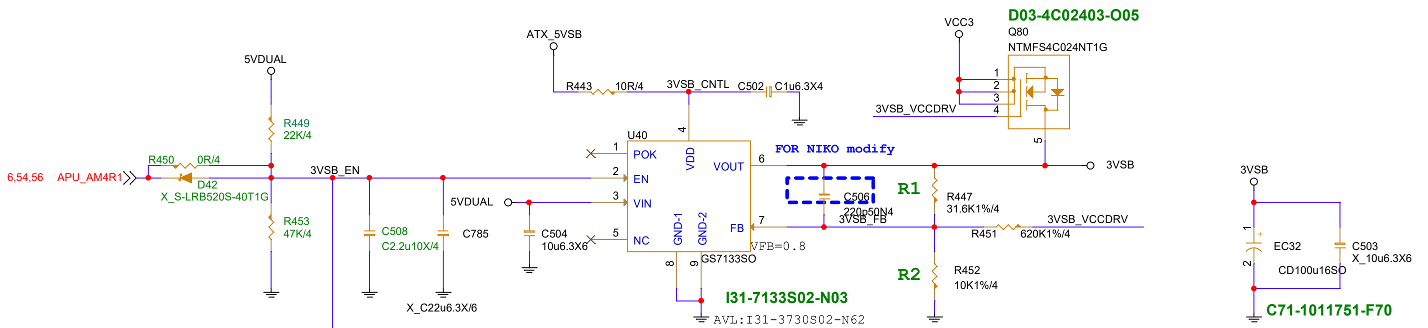


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@3.363A

CPU: VDD_33_S5@0.25A
CHIP: VDD_33_S5@0.1A
PCIE*4@1.5A
M.2_WIFI@0.78A
LAN@0.065A
Redriver*2@0.668A
USB TYPE-C@0.9mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10K))
= 3.328V OK

21ci203T

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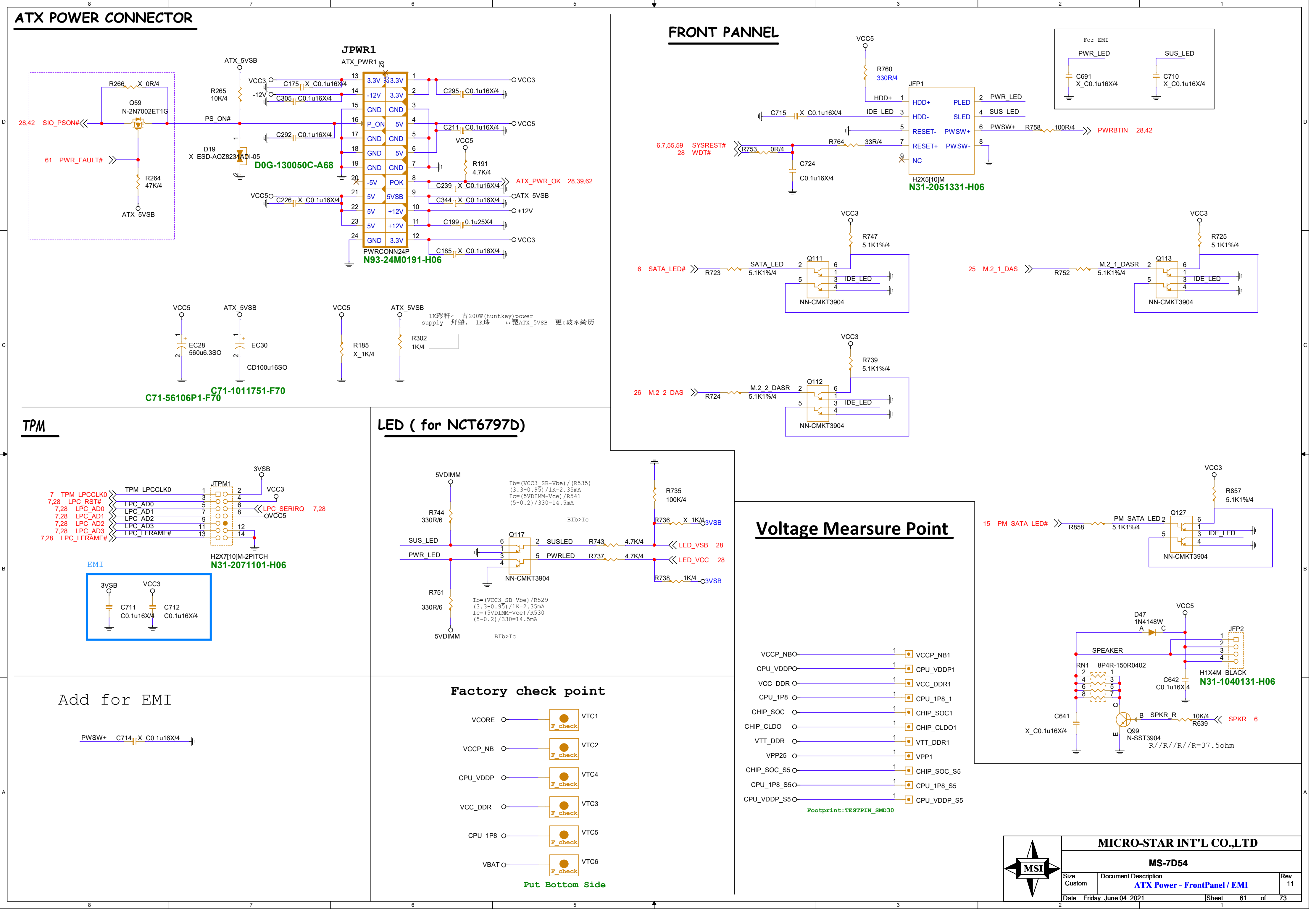

ATX POWER CONNECTOR
JPWR1
ATX_PWR1
PWRCONN24P
N93-24M0191-H06
D0G-130050C-A68
C71-56106P1-F70
C71-1011751-F70
FRONT PANNEL
JFP1
H2X5[10]M
N31-2051331-H06
For EMI
TPM
JTPM1
H2X7[10]M-2PITCH
N31-2071101-H06
EMI
LED (for NCT6797D)
Voltage Mearsure Point
Footprint:TESTPIN_SMD30
JFP2
H1X4M_BLACK
N31-1040131-H06
Add for EMI
Factory check point
Put Bottom Side
MICRO-STAR INT'L CO.,LTD
MS-7D54
Size
Custom
Document Description
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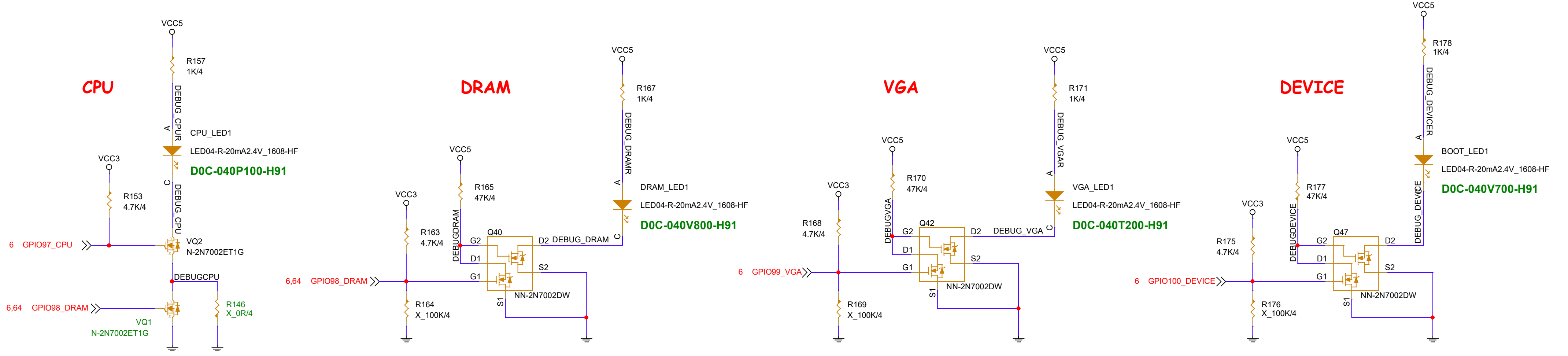
EZ Debug LED



LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獯	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防臧	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED獯繕 豔CPU LED闰奔

AMD AMP Detect LED

MICRO-STAR INT'L CO.,LTD

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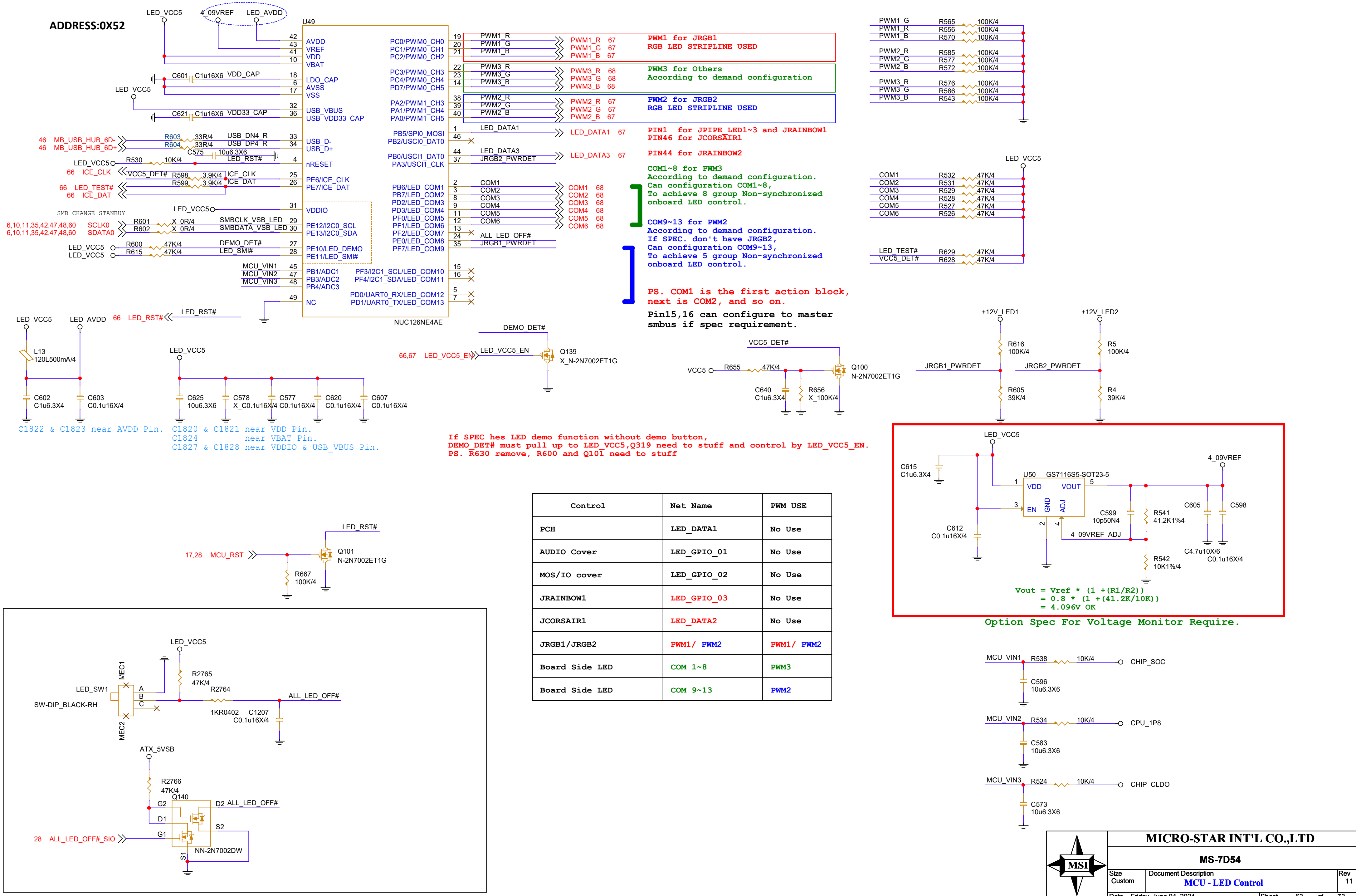
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

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Size: Custom | Document Description: MCU - LED Control | Rev: 11

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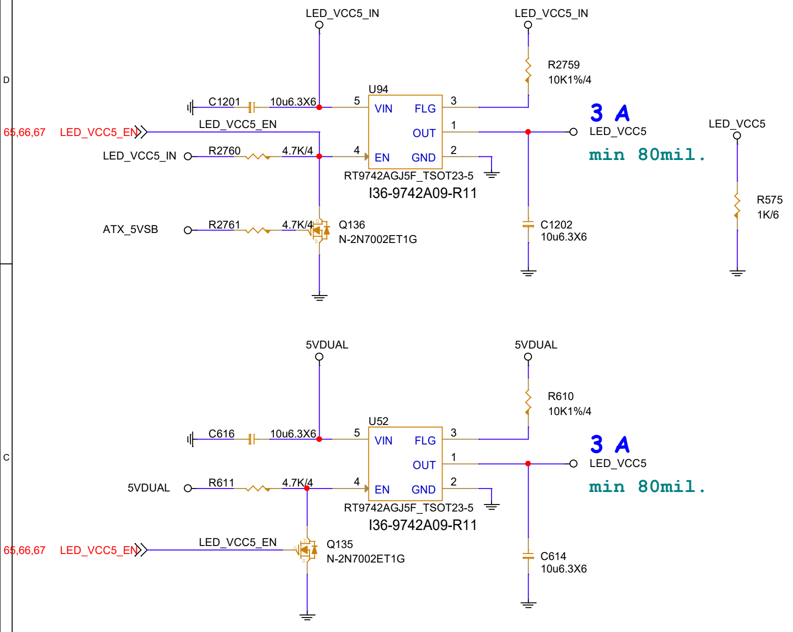
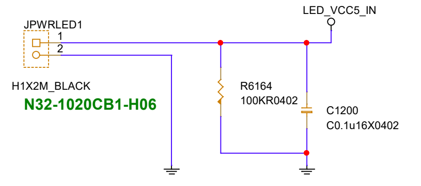
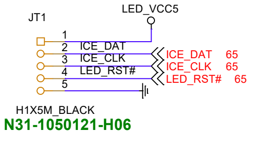
EXTERNAL POWER INPUT



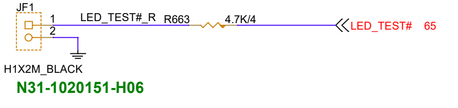
External Power



JT1 for FW update



JF1 For Factory Test



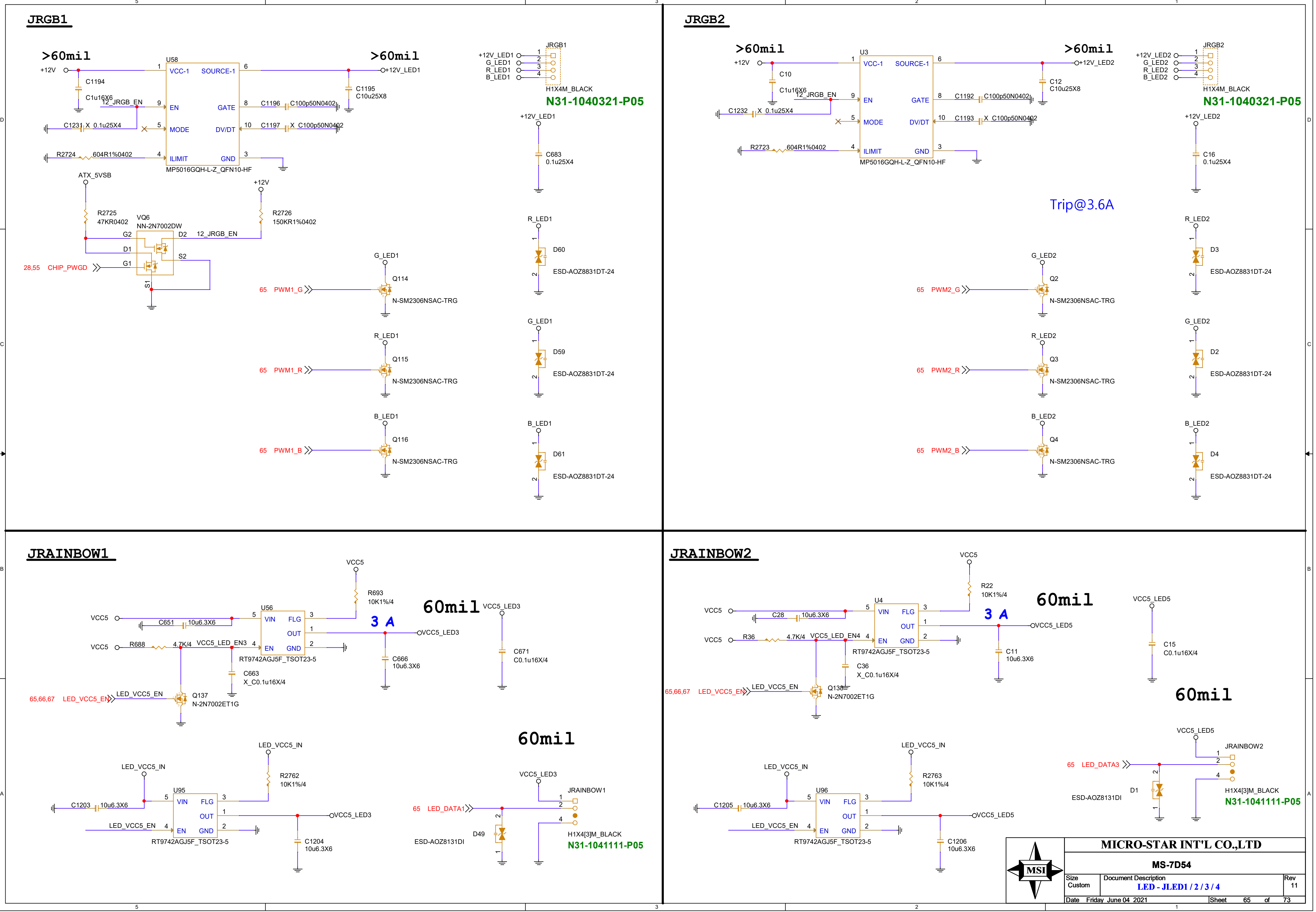
1 PCH HEATSINK LED

2 AUDIO/IO Cover LED

3 MOS HEATSINK LED

JPIPE:PIN1:output ,PIN2:input

PIN2:MCU IN
PIN1:HEATSINK OUT



JRGB1
>60mil
>60mil
+12V
C1194
C1u16X6
12_JRGB_EN
C1231 X 0.1u25X4
R2724 604R1%0402
U58
VCC-1
SOURCE-1
EN
GATE
MODE
DV/DT
ILIMIT
GND
MP5016GQH-L-Z_QFN10-HF
C1196 C100p50N0402
C1197 X C100p50N0402
+12V_LED1
C1195
C10u25X8
JRGB1
+12V_LED1
G_LED1
R_LED1
B_LED1
H1X4M_BLACK
N31-1040321-P05
C683
0.1u25X4
ATX_5VSB
R2725
47KR0402
VQ6
NN-2N7002DW
R2726
150KR1%0402
28,55 CHIP_PWGD
65 PWM1_G
Q114
N-SM2306NSAC-TRG
65 PWM1_R
Q115
65 PWM1_B
Q116
D60
ESD-AOZ8831DT-24
D59
D61
JRGB2
+12V_LED2
U3
C10
C1232 X 0.1u25X4
R2723 604R1%0402
C1192 C100p50N0402
C1193 X C100p50N0402
C12
C10u25X8
G_LED2
R_LED2
B_LED2
C16
Trip@3.6A
65 PWM2_G
Q2
65 PWM2_R
Q3
65 PWM2_B
Q4
D3
D2
D4
JRAINBOW1
VCC5
R693
10K1%/4
60mil
3 A
VCC5_LED3
C651 10u6.3X6
R688 4.7K/4
VCC5_LED_EN3
U56
VIN
FLG
OUT
RT9742AGJ5F_TSOT23-5
C663
X_C0.1u16X/4
C666
10u6.3X6
C671
C0.1u16X/4
65,66,67 LED_VCC5_EN
Q137
N-2N7002ET1G
LED_VCC5_IN
U95
C1203 10u6.3X6
R2762
10K1%/4
C1204
10u6.3X6
65 LED_DATA1
D49
ESD-AOZ8131DI
JRAINBOW1
H1X4[3]M_BLACK
N31-1041111-P05
JRAINBOW2
R22
VCC5_LED5
C28 10u6.3X6
R36 4.7K/4
VCC5_LED_EN4
U4
C36
C11
C15
Q138
U96
C1205 10u6.3X6
R2763
C1206
65 LED_DATA3
D1
JRAINBOW2
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MSI
MS-7D54
Size Custom
Document Description
LED - JLED1 / 2 / 3 / 4
Rev 11
Date Friday June 04 2021
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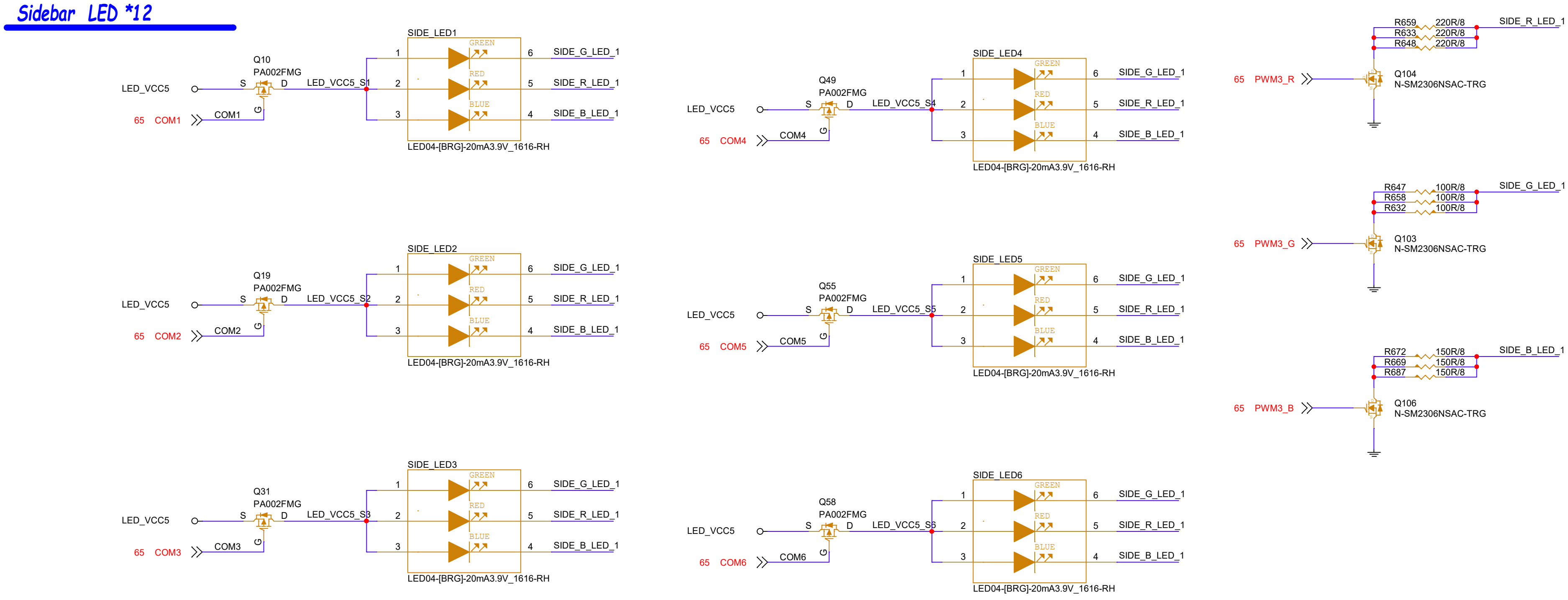

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Custom	LED - Sidebar LED	11
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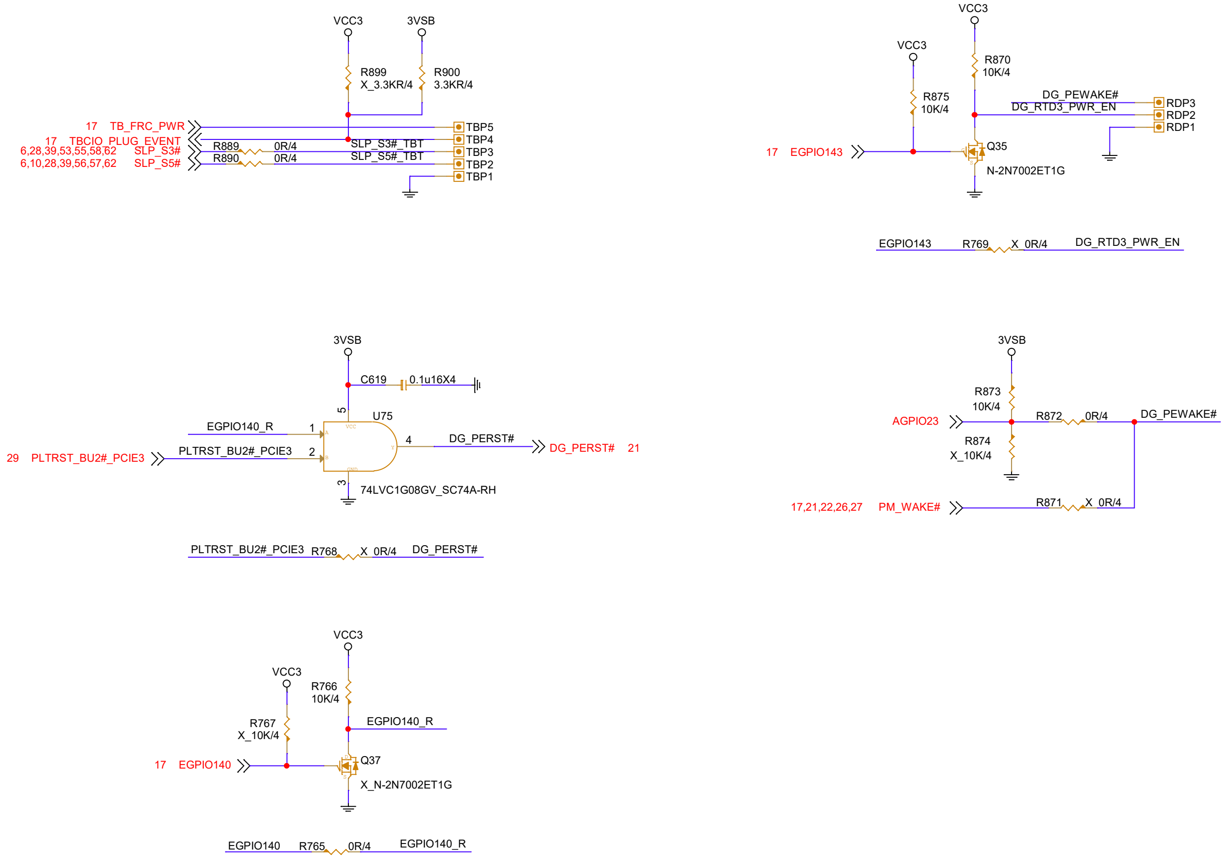
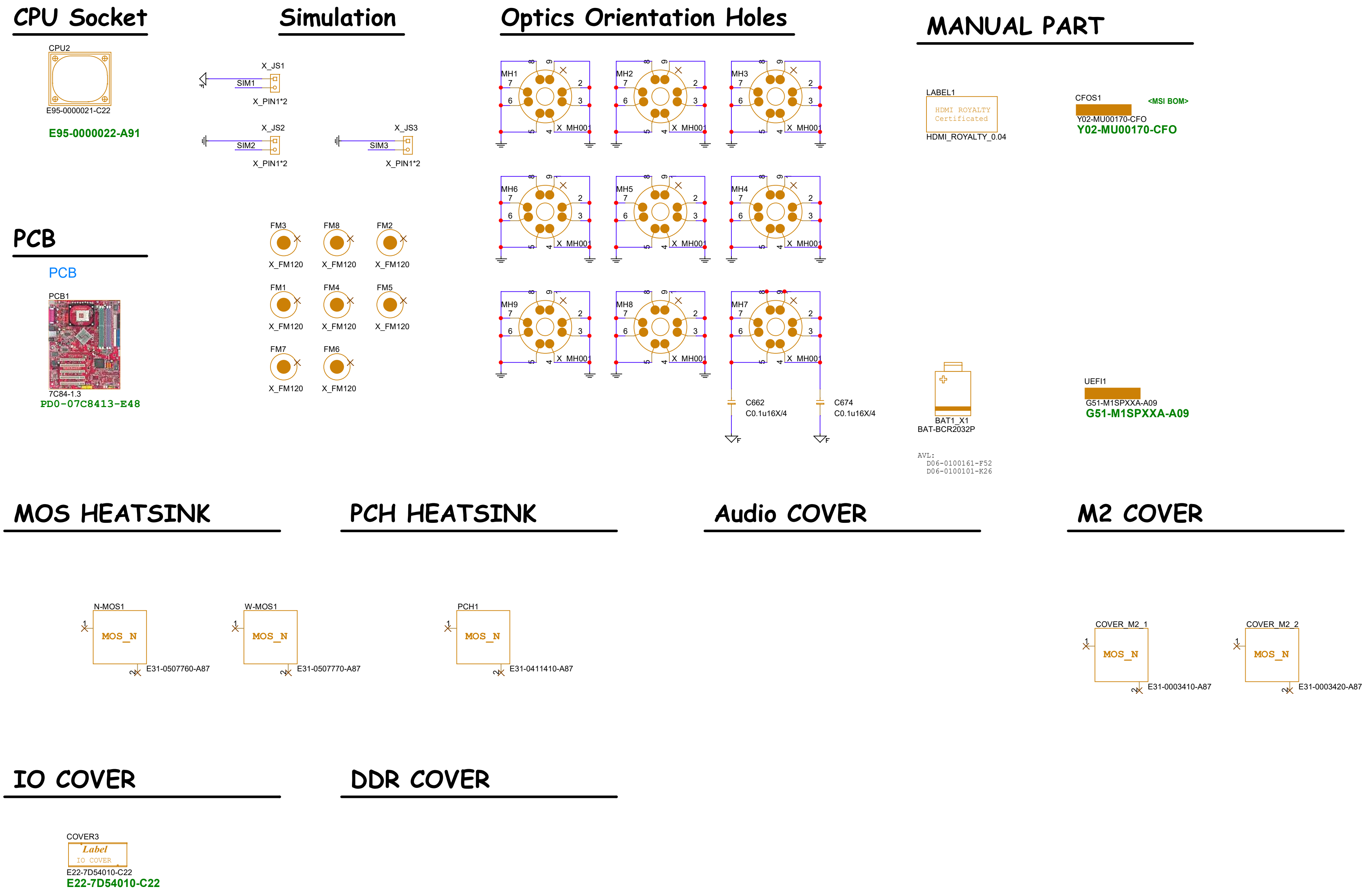

VCC3
3VSB
R899
X_3.3KR/4
R900
3.3KR/4
17 TB_FRC_PWR
17 TBCIO_PLUG_EVENT
6,28,39,53,55,58,62 SLP_S3#
6,10,28,39,56,57,62 SLP_S5#
R889 0R/4
R890 0R/4
SLP_S3#_TBT
SLP_S5#_TBT
TBP5
TBP4
TBP3
TBP2
TBP1
VCC3
VCC3
R870
10K/4
R875
10K/4
DG_PEWAKE#
DG_RTD3_PWR_EN
RDP3
RDP2
RDP1
17 EGPIO143
Q35
N-2N7002ET1G
EGPIO143 R769 X_0R/4 DG_RTD3_PWR_EN
3VSB
C619 0.1u16X4
U75
EGPIO140_R
29 PLTRST_BU2#_PCIE3
PLTRST_BU2#_PCIE3
DG_PERST#
DG_PERST# 21
74LVC1G08GV_SC74A-RH
PLTRST_BU2#_PCIE3 R768 X_0R/4 DG_PERST#
3VSB
R873
10K/4
AGPIO23
R872 0R/4
DG_PEWAKE#
R874
X_10K/4
17,21,22,26,27 PM_WAKE#
R871 X_0R/4
VCC3
VCC3
R766
10K/4
EGPIO140_R
R767
X_10K/4
17 EGPIO140
Q37
X_N-2N7002ET1G
EGPIO140 R765 0R/4 EGPIO140_R



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Size	Document Description	Rev
Custom	**Manual Parts**	11

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