SYSTEM PAGE REF.

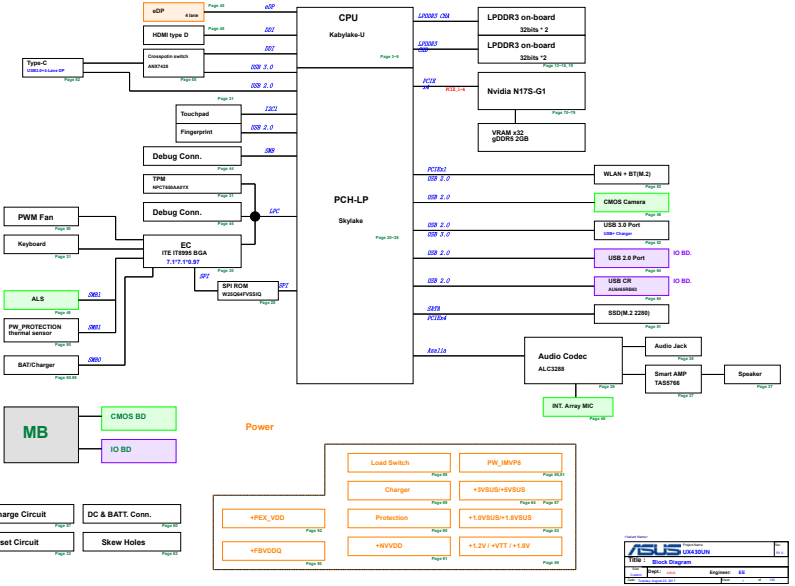
PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DISPLAY
4	CPU_DDR3L
5	CPU_LPC,SPI,SMB,CLINK
6	CPU_PCIEWS
7	CPU_XDP
8	CPU_MISC,JTAG,CLK
9	CPU_CFG,RSVD
13	LPDDR3_TERMINATION
14	LPDDR3_ON-BOARD_A
15	LPDDR3_ON-BOARD_B
19	LPDDR3_CA_DQ VOLTAGE
20	CPU_PCH_CFG,DISPLAY
21	CPU_PCH_CSPIO, LPIO, MISC
22	CPU_PCH_SATA,JTAG,AUDIO,RTC
23	CPU_PCH_PCIE,USB
24	CPU_PCH_CLOCK SIGNALS
25	CPU_PCH_SYS_POWER
26	CPU_PCH_PWEMS,GND
27	CPU_PCH_PWEMS,GND
28	PCH_SPI ROM,OTW, TPM
30	EXC_IT8995
31	EC_KB_TP
32	RST_Reset Circuit
44	EDG_Debug
45	CRT_LCD Panel_CMOS_IMIC
48	HDMI type-D
51	M2_SSD
52	USB Port
56	LED_Indicator
57	DSG_Discharge
58	PRO_PROTECT
60	DC_DC & BAT Conn.
62	ME_Conn & Skew Hole
64	B TO B CONN
70	VGA_NV_N16S-GTR_PCIE
71	VGA_NV_N16S-GTR_FB-IF
72	VGA_NV_N16S-GTR_FB-GDDR5
73	VGA_NV_N16S-GTR_VDD
74	VGA_NV_N16S-GTR_DISPLAY
75	VGA_NV_N16S-GTR_ROM,XTAL
76	VGA_NV_N16S-GTR_GPIO
77	VGA_NV_N16S-GTR_POWER
78	VGA_NV_N16S-GTR_Protection
80	PW_KBL - U (1) [NCP81216A]
81	PW_KBL - U (2) [NCP81216A]
83	PW_+1.0VSUS / +1.8VSUS
86	PW_1.2V/+VTT/+1.8V
87	PW_+3VADSW/+5VSUS
88	PW_LOAD SWITCH
89	PW_CHARGER
90	PW_PROTECTION_KBL
91	PW_+NVVDD (1)
93	+FBVDDQ
99	PW_FLOW CHART
100	AC Power On Timing
101	POWER-ON SEQUENCE
102	Revision History

BLOCK DIAGRAM

UX430UN/UNR/UAR SCHEMATIC Revision 1.0

Marketing name:
UN: NVIDIA GeForce 1040 (C.S N17S-G1-A1 FCBGA595 QS), GDDR5 2G (256 x 32 x 2)
UNR: NVIDIA GeForce 1040 (C.S N17S-G1-A1 FCBGA595 QS), GDDR5 2G (256 x 32 x 2)
UAR : INTEL HD GRAPHIC

Modern standby



Title :	Block Diagram
Engineer:	EE

KBL-U PCH GPIO Table

PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power
GPP_A0	Native	RC_IN#		EXT PU 10K	+3VS
GPP_A1	Native	LPC_AD0			
GPP_A2	Native	LPC_AD1			
GPP_A3	Native	LPC_AD2			
GPP_A4	Native	LPC_AD3			
GPP_A5	Native	LPC_FRAME#			
GPP_A6	Native	INT_SERIRQ		EXT PU 10K	+3VS
GPP_A7	GPO	N/A			
GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS
GPP_A9	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	Native	CLK_TPMPCI_PCH_X1			
GPP_A11	GPO	PME#		EXT PU 10K	+3VA_DSW
GPP_A12	GPO	N/A			
GPP_A13	Native	SUSWARN#		EXT PU 10K	+3VSUS
GPP_A14	Native	PCH_SUS_STAT#			
GPP_A15	Native	PCH_SUSACK#			
GPP_A16	GPO	N/A			
GPP_A17	GPO	N/A			
GPP_A18	GPO	N/A			
GPP_A19	GPO	N/A			
GPP_A20	GPO	N/A			
GPP_A21	GPO	N/A			
GPP_A22	GPO	N/A			
GPP_A23	GPO	N/A			
GPP_B0	GPO	N/A			
GPP_B1	GPO	N/A			
GPP_B2	GPO	VRALERT#		EXT PU 10K	+3VA_DSW
GPP_B3	GPO	N/A			
GPP_B4	GPO	N/A			
GPP_B5	Native	CK_REQ_P0#		EXT PU 10K	+3VS
GPP_B6	Native	CK_REQ_P1#		EXT PU 10K	+3VS
GPP_B7	GPO	N/A			
GPP_B8	GPO	N/A			
GPP_B9	GPO	N/A			
GPP_B10	Native	CK_REQ_P5#		EXT PU 10K	+3VS
GPP_B11	Native	MPHY_PWREN		EXT PU 20K	+3VSUS
GPP_B12	GPO	PCH_SLP_S0#			
GPP_B13	GPO	PLT_RST#			
GPP_B14	GPO	N/A			
GPP_B15	GPO	N/A			
GPP_B16	GPO	N/A			
GPP_B17	GPO	N/A			
GPP_B18	GPO	N/A			
GPP_B19	GPO	N/A			
GPP_B20	GPI	GPU_EVENT#		EXT PU 10K	+3VSG
GPP_B21	GPI	GC6_FB_EN		EXT PD 10K	
GPP_B22	GPO	N/A			
GPP_B23	Native	SML1ALERT#		EXT PU 150K	+3VSUS
GPP_C0	Native	SMB_CLK		EXT PU 2.2K	+3VSUS
GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS
GPP_C2	GPO	N/A			
GPP_C3	Native	SML0_CK		EXT PU 2.2K	+3VSUS
GPP_C4	Native	SML0_DATA		EXT PU 2.2K	+3VSUS
GPP_C5	GPO	N/A			
GPP_C6	Native	SML1_CK		EXT PU 2.2K	+3VSUS
GPP_C7	Native	SML1_DATA		EXT PU 2.2K	+3VSUS
GPP_C8	GPO	N/A			
GPP_C9	GPO	N/A			
GPP_C10	GPO	N/A			
GPP_C11	GPO	N/A			
GPP_C12	GPI	DIMM_SEL0			+3VSUS
GPP_C13	GPI	DIMM_SEL1			+3VSUS
GPP_C14	GPI	DIMM_SEL2			+3VSUS
GPP_C15	GPO	N/A			
GPP_C16	GPO	N/A			
GPP_C17	GPO	ALS_INT#_X1		EXT PU 10K	+3VSUS
GPP_C18	Native	I2C1_SDA		EXT PU 4.7K	+3VS
GPP_C19	Native	I2C1_SCL		EXT PU 4.7K	+3VS
GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VSG
GPP_C21	GPO	GPU_RST#		EXT PD 10K	
GPP_C22	GPO	DGPU_PWR_EN#			+3VSUS
GPP_C23	GPO	N/A			
GPP_D0	Native	SPI_CS#0_FP		EXT PU 10K	+3VS
GPP_D1	Native	SPI_CLK_FP		EXT PU 10K	+3VS
GPP_D2	Native	SPI_MISO_FP		EXT PU 56K	+3VS
GPP_D3	Native	SPI_MOSI_FP		EXT PU 10K	+3VS
GPP_D4	GPO	N/A			
GPP_D5	GPO	N/A			
GPP_D6	GPO	N/A			
GPP_D7	GPO	N/A			
GPP_D8	GPO	N/A			
GPP_D9	GPI	PCB_ID0		EXT PD 10K	+3VS
GPP_D10	GPI	PCB_ID1		EXT PD 10K	+3VS
GPP_D11	GPI	Touchpad_id_X1			+3VS
GPP_D12	GPO	N/A			
GPP_D13	GPI	TOUCHPAD_INTR#_R		EXT PU 10K	+3VS
GPP_D14	GPO	N/A			
GPP_D15	GPO	WLAN_BT_LED		EXT PU 10K	+3VSUS
GPP_D16	GPI	SPI_INT#_FP		EXT PU 10K	+3VS
GPP_D17	GPO	N/A			
GPP_D18	GPO	N/A			
GPP_D19	GPO	DMIC_CLK_PCH			
GPP_D20	GPO	DMIC_DATA_PCH			
GPP_D21	GPO	N/A			
GPP_D22	GPO	N/A			

PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power
GPP_D23	GPO	N/A			
GPP_E0	NATIVE	PE_DET		EXT PU 10K	+3VS
GPP_E1	GPO	N/A			
GPP_E2	GPO	N/A			
GPP_E3	GPO	N/A			
GPP_E4	NATIVE	SATA0_DEVSLP		EXT PD 10K	
GPP_E5	GPO	N/A			
GPP_E6	GPO	N/A			
GPP_E7	GPO	N/A			
GPP_E8	GPO	N/A			
GPP_E9	NATIVE	USB_OC_1_2#		EXT PU 10K	+3VSUS
GPP_E10	NATIVE	USB_OC_3_4#		EXT PU 10K	+3VSUS
GPP_E11	NATIVE	USB_OC_5_6#		EXT PU 10K	+3VSUS
GPP_E12	NATIVE	USB_OC_7_8#		EXT PU 10K	+3VSUS
GPP_E13	GPO	N/A			
GPP_E14	NATIVE	HDMI_HP		EXT PU 1M	+3VS
GPP_E15	GPI	EXT_SMI#		EXT PU 10K	+3VS
GPP_E16	GPI	EXT_SCI#		EXT PU 10K	+3VS
GPP_E17	NATIVE	EDP_HPD_CON		EXT PD 100K	
GPP_E18	GPO	N/A			
GPP_E19	GPO	N/A			
GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS
GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS
GPP_E22	GPO	N/A			
GPP_E23	GPO	N/A			
GPP_F0	GPO	N/A			
GPP_F1	GPO	N/A			
GPP_F2	GPO	N/A			
GPP_F3	GPO	N/A			
GPP_F4	GPO	N/A			
GPP_F5	GPO	N/A			
GPP_F6	GPO	N/A			
GPP_F7	GPO	N/A			
GPP_F8	GPO	N/A			
GPP_F9	GPO	N/A			
GPP_F10	GPO	N/A			
GPP_F11	GPO	N/A			
GPP_F12	GPO	N/A			
GPP_F13	GPO	N/A			
GPP_F14	GPO	N/A			
GPP_F15	GPO	N/A			
GPP_F16	GPO	N/A			
GPP_F17	GPO	N/A			
GPP_F18	GPO	N/A			
GPP_F19	GPO	N/A			
GPP_F20	GPO	N/A			
GPP_F21	GPO	N/A			
GPP_F22	GPO	N/A			
GPP_F23	GPO	N/A			
GPP_G0	GPO	N/A			
GPP_G1	GPO	N/A			
GPP_G2	GPO	N/A			
GPP_G3	GPO	N/A			
GPP_G4	GPO	N/A			
GPP_G5	GPO	N/A			
GPP_G6	GPO	N/A			
GPP_G7	GPO	N/A			
GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW
GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW
GPD2	GPO	PCH_GPD2#			
GPD3	Native	PM_PWRBTN#		EXT PU 10K	+3VSUS
GPD4	Native	PM_SUSB#		EXT PD 100K	
GPD5	Native	PM_SUSC#		EXT PD 100K	
GPD6	GPO	N/A			
GPD7	GPO	N/A			
GPD8	GPO	SUS_CK		EXT PD 1K	
GPD9	GPO	N/A			
GPD10	GPO	SLP_S5#			
GPD11	GPO	LAN_PWREN			

EC IT8995 - DX GPIO Table

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K	+3VA_EC
GPA3	Alt	GPO			
GPA4	O	GPO	ANX7428_PWR_EN		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	ANX7428_RESET#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 10K	+3VA
GPB2	OD	GPO			
GPB3	Alt	GPO	PWR_SW#	PU 10K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	I	GPI	ANX7428_CABLE_DET		
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	I	GPI	ANX7428_INT#		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K	+3VSUS
GPC4	I	GPO	GC6_FB_EN		
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 10K	
GPC7	O	GPO			

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	OP_SD#		
GPD6	Alt	GPI	FAN0_TACH		
GPD7	Alt	GPO			

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 10K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 10K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO			
GPE4	O	GPO			
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#	PU 10K	+3VS
GPE7	OD	GPO	THRO_CPU#	PU 1K	+VCCSTG

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 10K & PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K & PD 1M @	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	GPO			
GPF5	Alt	GPO			
GPF6	Alt	PECI	PECI_EC_R/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH	PD 10K (@)	
GPG4	GPI		EC_SI/EC_SI_PCH	PD 10K (@)	
GPG5	GPI		EC_SO/EC_SO_PCH	PD 10K (@)	
GPG6	O	GPO			
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	SMB3_CLK		
GPH2	Alt	SMBus	SMB3_DAT		
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 100K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 10K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#	PU 10K	+3VSUS
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 93.1K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPO			
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	GPO			
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	GPO			
GPJ5	O	GPO			
GPJ6	I	GPO			
GPJ7	O	GPO			

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

Design IP Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	SM-Bus Address

EC Master (SMB1)	SM-Bus Address
SM-Bus Device	
DIMM TEMP.(U1410)	9Ah
CPU & GPU TEMP.(U7801)	0x74
Power TEMP.(PU9001)	0x7E

PCI Express

PCIE 1	VGA
PCIE 2	VGA
PCIE 3	VGA
PCIE 4	VGA
PCIE 5	
PCIE 6	WLAN
PCIE 7	
PCIE 8	
PCIE 9	SSD
PCIE 10	SSD
PCIE 11	SSD
PCIE 12	SSD

SATA Port

SATA 0	
SATA 1	
SATA 2	
SATA 3	SSD

USB 3.0 Port

USB 1	USB 3.0 (MB)
USB 2	USB 3.0 (IO)
USB 3	USB 3.0 (Type-C)
USB 4	USB 3.0 (Type-C)

USB 2.0 Port

USB 1	USB 3.0(MB)
USB 2	USB 3.0 (IO BD)
USB 3	
USB 4	Card Reader
USB 5	CMOS Camera
USB 6	MB Type C
USB 7	MB Type C
USB 8	BT
USB 9	Finger Printer
USB 10	

Device Identification

Memory Thermal Sensor		
1st	06G023040020	G781-1P8F
2nd		

CPU & GPU Thermal Sensor		
1st	06023-00020000	UP1905AMA8
2nd		

Power Thermal Sensor		
1st	06023-00020000	UP1905AMA8
2nd		

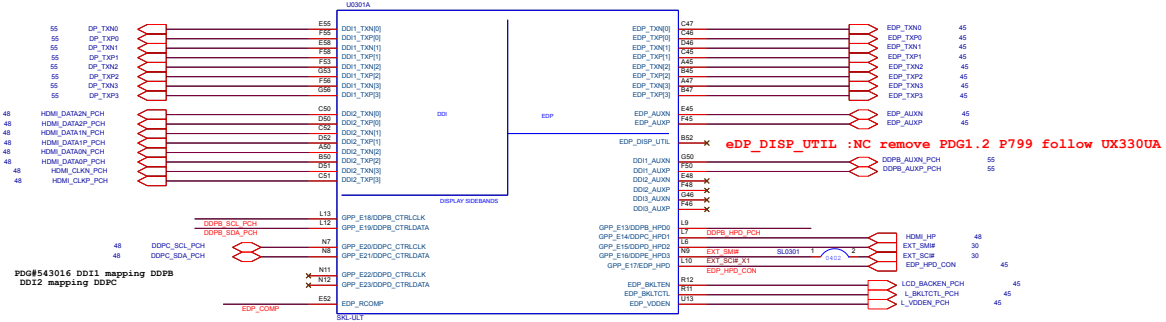
<Variant Name>

ASUS	Project Name UX430UN	Rev R1.0
Title : System Setting		
Size Custom	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 2 of 102	

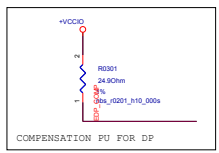
Display Port

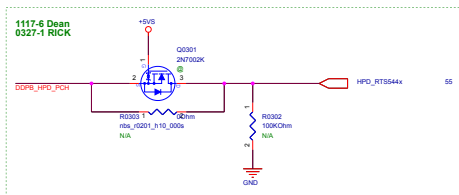
	EDP
1	DP
2	HDMI

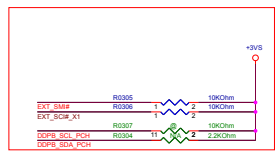
Intel Version	ASUS P/N
KBL-U QS Sample	01001-01280100



	HDMI
DDI2_0	Lane2
DDI2_1	Lane1
DDI2_2	Lane0
DDI2_3	CLK



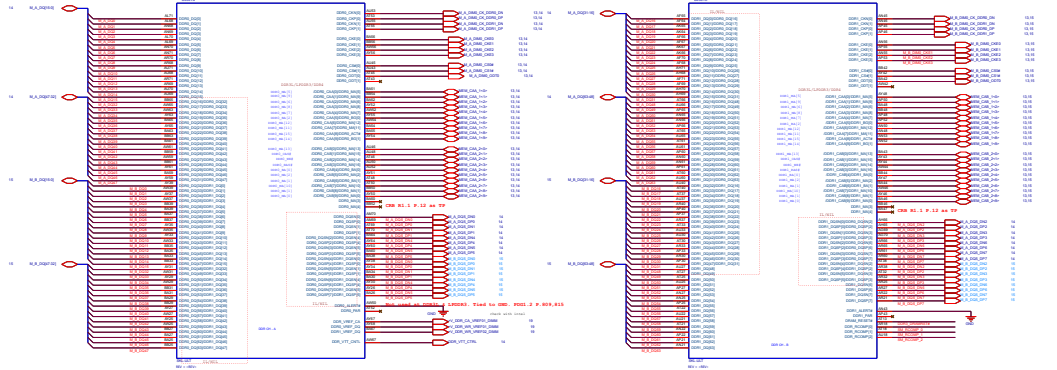




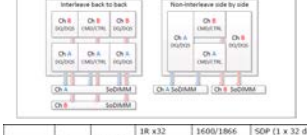
<Variant Name>

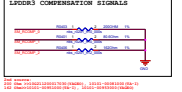
Project Name: UX430UN		Rev: R1.0
Title: CPU_DISPLAY		
Size: B	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 3 of 102	

LPDDR3 Non-Interleaved



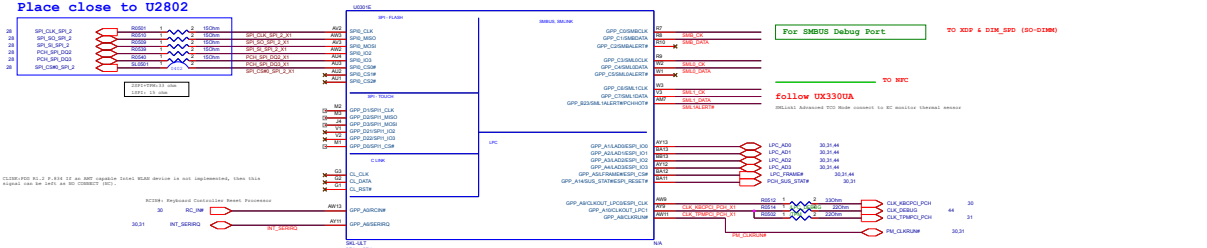
IL		NIL	
Channel	Byte	Channel	Byte
DDR0	Byte0	DDR0	Byte0
DDR0	Byte1	DDR0	Byte1
DDR0	Byte2	DDR0	Byte4
DDR0	Byte3	DDR0	Byte5
DDR0	Byte4	DDR1	Byte0
DDR0	Byte5	DDR1	Byte1
DDR0	Byte6	DDR1	Byte4
DDR0	Byte7	DDR1	Byte5
DDR1	Byte0	DDR0	Byte2
DDR1	Byte1	DDR0	Byte3
DDR1	Byte2	DDR0	Byte6
DDR1	Byte3	DDR0	Byte7
DDR1	Byte4	DDR1	Byte2
DDR1	Byte5	DDR1	Byte3
DDR1	Byte6	DDR1	Byte6



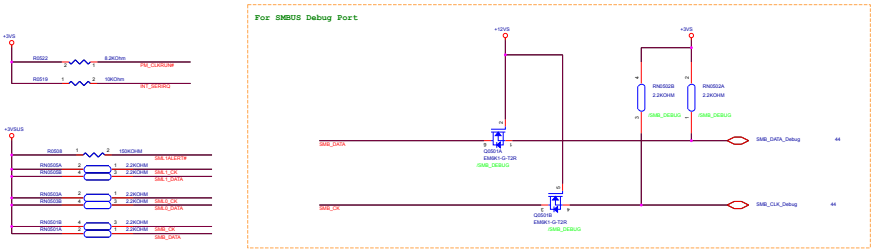


KBL-U LPDDR3	4.3	LPDDR3	1R x32	1600/1866	SDP (1 x 32 die)		
			2R x32	1600/1866	DDP (2 x 32 dies)	178	Type3 - 10L	NIL
			2R x32	1600/1866	QDP (4 x 16 dies)			
	4.4	LPDDR3	1R x32	1600/1866	SDP (1 x 32 die)			
			2R x32	1600/1866	DDP (2 x 32 dies)	178	HDI 10L (2-x-2+) (1-x-1+)	NIL
			2R x32	1600/1866	QDP (4 x 16 dies)			
	4.5	LPDDR3	1R x64	1600/1866	DDP (2 x 32 dies)	253	HDI 10L	NIL
			2R x64	1600/1866	QDP (4 x 32 dies)			

Variant Name:			
ASUS	Project Name: UX430UQ		Rev: 0.1
Title :	CPU_LPDDR3		
File:	Dept: MB/SB/EC	Engineer:	Mario_Jhu
Note: Tuesday, August 04, 2015		Sheet 4 of 100	



1216-1 ECN Remove Debug IO/RF CLIP/TYPE-C CONN 12013-00117500 Foxconn陪料
UA:EN-0248068-R UQ:EN-0248045-R



follow UX330UA

GPP_C5: weak internal pull down	
PU	SPI BIOS
PD	LPC is selected for EC (Default)

Transport Layer Security (TLS) Confidentiality

follow UX330UA

GPP_C2: weak internal pull down	
PU	Enable
PD	Disable Intel ME TLS cipher suite (no confidentiality)(Default)

TP for Boundary Scan Test

<Variant Name>

Project Name	UX430UN	Rev 0.2
Title :	CPU_LPC,SPI,SMB,CLINK	
Size: Custom	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 5 of 102	

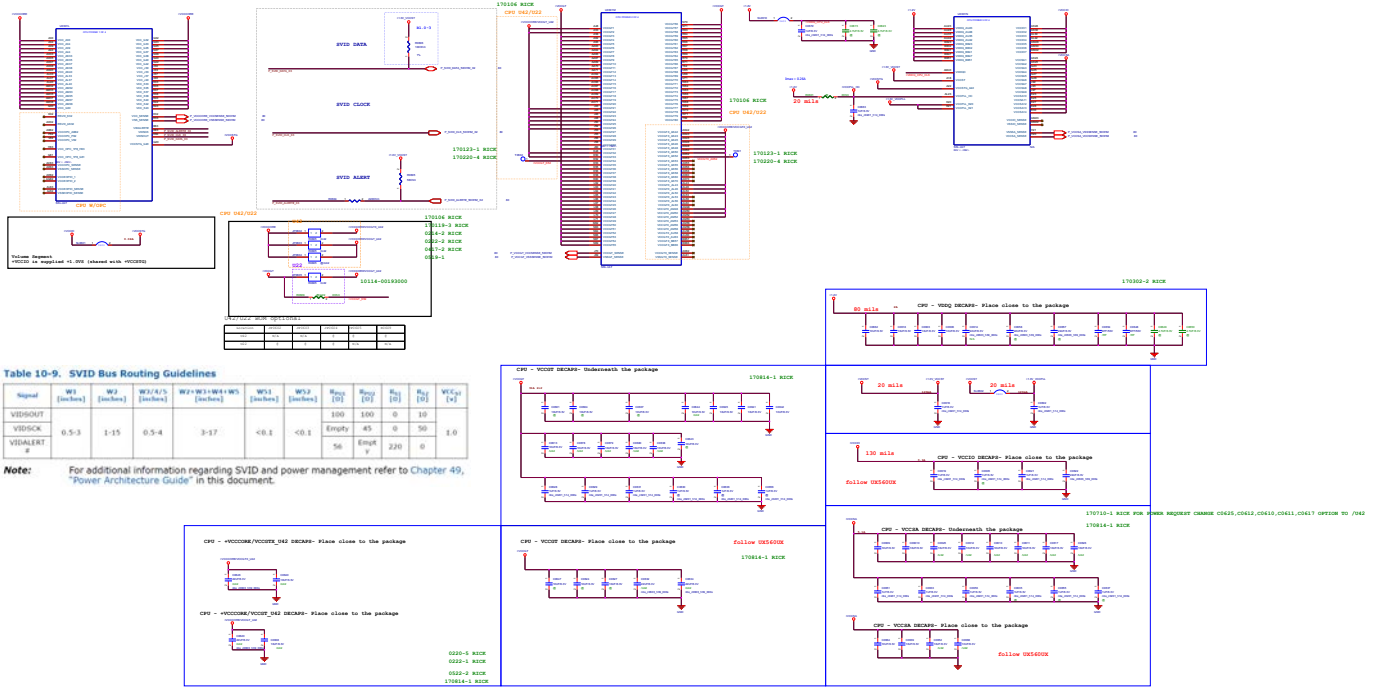
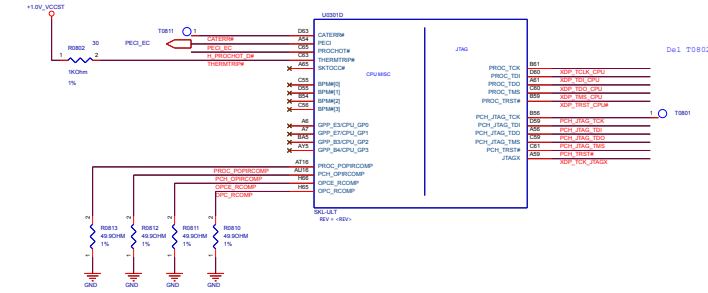


Table 10-9. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{S1} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to Chapter 49, "Power Architecture Guide" in this document.

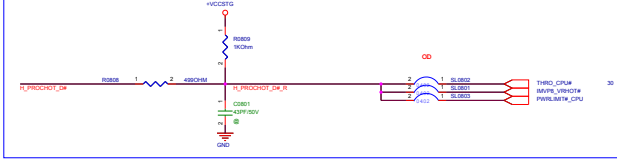
CATERR:This signal indicates that the system has experienced a catastrophic error and cannot continue to operate.



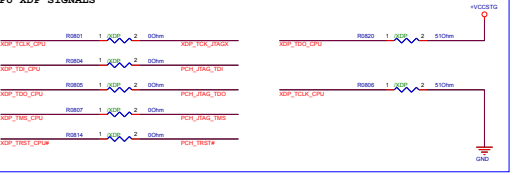
B0#:Skylake processor bi-directional signal that indicate the status of breakpoints and programmable counters used for monitoring Skylake processor performance

1216-1 ECN Remove Debug IO/RF CLIP/TYPE-C CONN 12013-00117500 Foxconn用料
UA:EN-0248068-R UQ:EN-0248045-R

CPU SIDEBAND SIGNALS

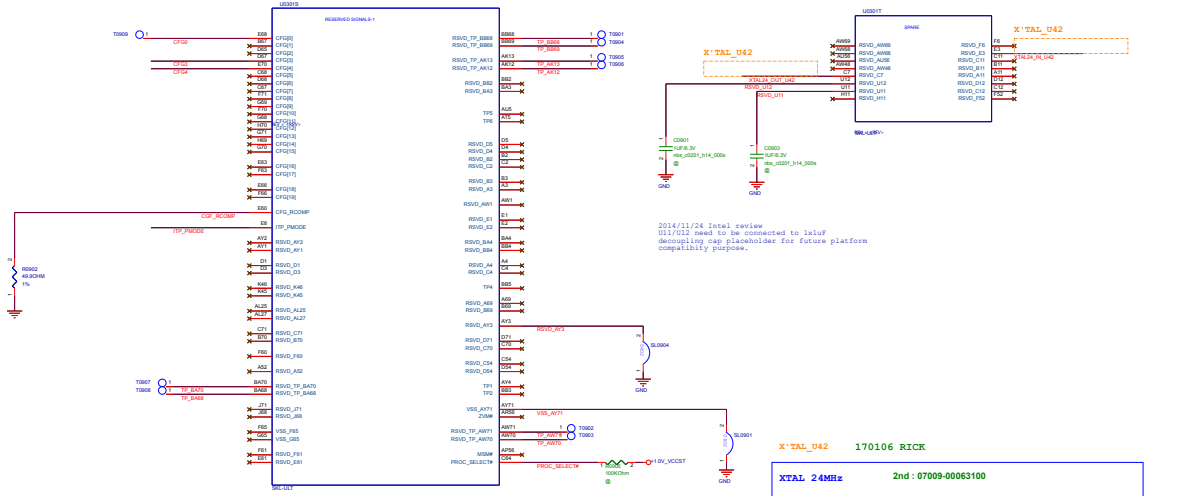


CPU XDP SIGNALS



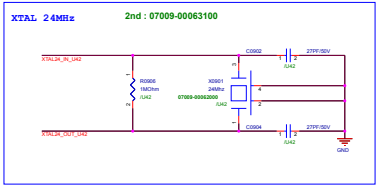
<Variant Name>

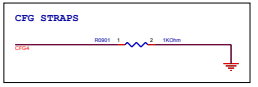
ASUS	Project Name: UX430UN	Rev: R1.0
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet: 8 of 102	



2014/11/24 Intel review
U11/U12 need to be connected to 1x1uF
decoupling cap placeholder for future platform
compatibity purpose.

X'TAL U42 170106 RICK

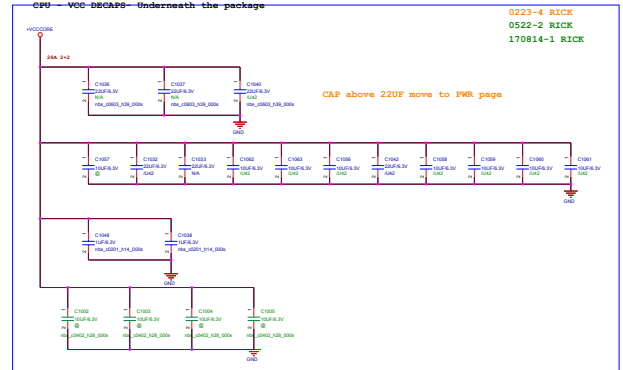


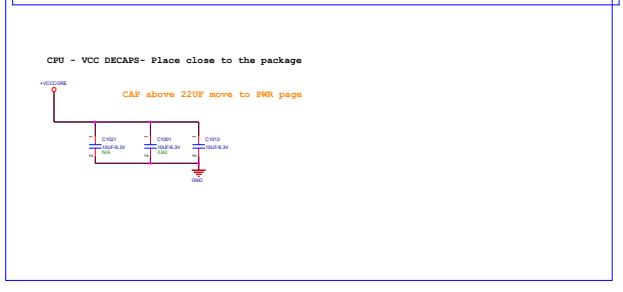


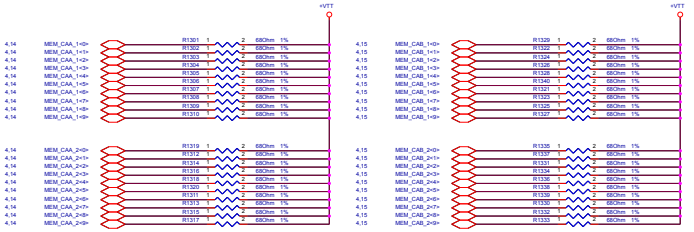
	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

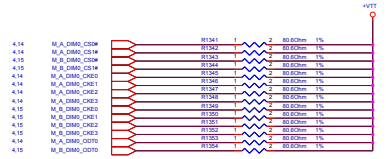
<Variant Name>

ASUS	Project Name: UX430UN		Rev: R1.0
Title : CPU_CFG,RSVD			
Size: Custom	Dept.: ASUS	Engineer: EE	
Date: Tuesday, August 22, 2017	Sheet 9 of 102		

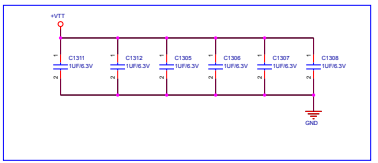

CPU - VCC DECAPS- Underneath the package
0223-4 RICK
0522-2 RICK
170814-1 RICK
+VCCCORE
28A 2+2
C1036 22UF-6.3V N/A nbs_c0603_h39_000s
C1037 22UF-6.3V N/A nbs_c0603_h39_000s
C1040 22UF-6.3V /U42 nbs_c0603_h39_000s
CAP above 22UF move to PWR page
GND
C1057 10UF-6.3V /U42
C1032 10UF-6.3V /U42
C1033 22UF-6.3V N/A
C1062 10UF-6.3V /U42
C1063 10UF-6.3V /U42
C1056 10UF-6.3V /U42
C1042 10UF-6.3V /U42
C1058 10UF-6.3V /U42
C1059 10UF-6.3V /U42
C1060 10UF-6.3V /U42
C1061 10UF-6.3V /U42
GND
C1048 1UF-6.3V nbs_c0201_h14_000s
C1038 1UF-6.3V nbs_c0201_h14_000s
GND
C1002 10UF-6.3V nbs_c0402_h28_000s
C1003 10UF-6.3V nbs_c0402_h28_000s
C1004 10UF-6.3V nbs_c0402_h28_000s
C1005 10UF-6.3V nbs_c0402_h28_000s
GND


CPU - VCC DECAPS- Place close to the package
+VCCCORE
CAP above 22UF move to PWR page
C1021 10UF-6.3V N/A
C1001 10UF-6.3V /U42
C1013 10UF-6.3V /U42
GND

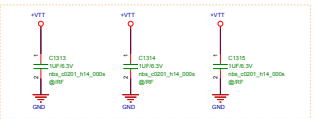


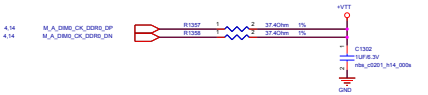


Close to LPDDR3 termination resistance (0201 size)



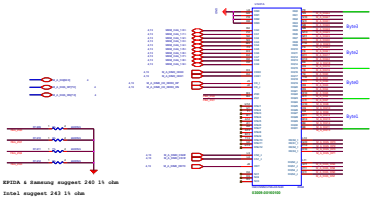
RF

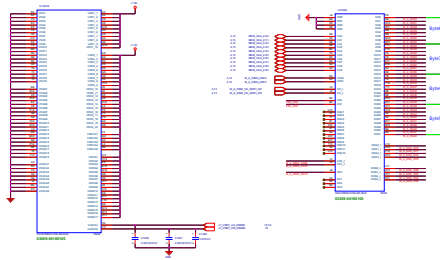


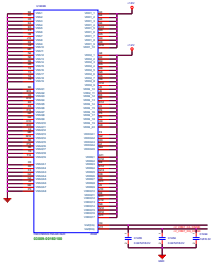


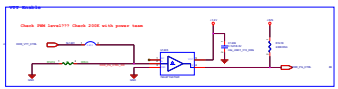
<Variant Name>

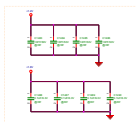
ASUS	Project Name: UX430UQ		Rev: R1.0
Title :	LPDDR3_TERMINATION		
Size: B	Dept.: NB1RD2EE2	Engineer: Mario_Jhu	
Date: Tuesday, August 22, 2017		Sheet 13 of 102	

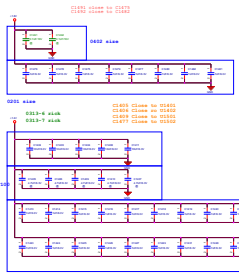








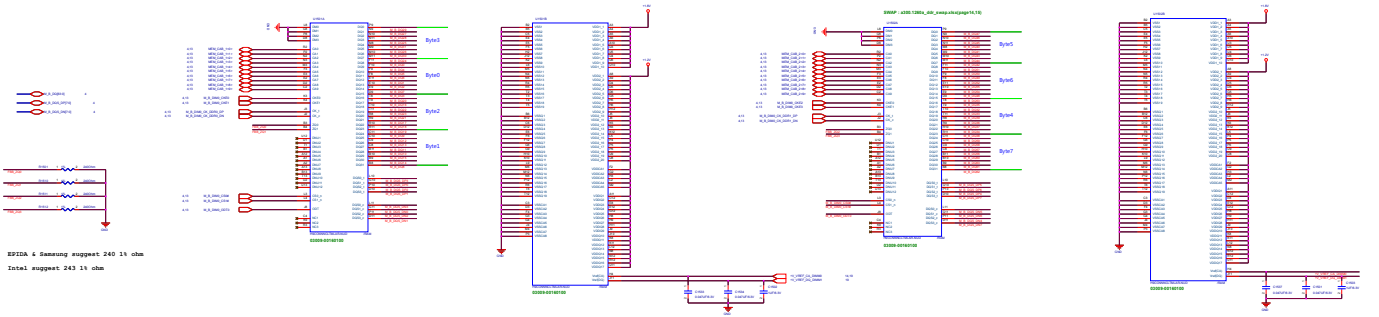




LPDDR3 x32 Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x pF [size]	Note
LPDDR3 Memory Down x32 - 2 Devices per Channel	VDDQ	1 near each device, Figure 4-55, VDDQ red circles	8x 0.1µF [0201]	2
		4 near each device, Figure 4-55 VDDQ red circles	16x 1µF [0402]	2
		2 near each device, Figure 4-55 VDDCA yellow circles	8x 1µF [0402]	2
		3 near each device, Figure 4-55 VDD2 blue circles	12x 1µF [0402]	2
		7 near each device, Figure 4-55 VDD1 pink circles	8x 1µF [0402]	2
		5 Distributed, VDDQ red circles Figure 4-56	5x 10µF [0603]	2
		3 Distributed, VDDCA yellow circles Figure 4-56	3x 10µF [0603]	2
		4 Distributed, VDD2 blue circles Figure 4-56	5x 10µF [0603]	2
		5 Distributed, VDD1 pink circles Figure 4-56	5x 10µF [0603]	2
	VTT	Distributed along terminations, Caps shown in blue Figure 4-57	8x 1µF [0402]	
		Edge of VR island. Caps shown in green Figure 4-57	2x 22µF [0603]	

Notes:
1. Total quantity is referring to 2 channels.
2. Distributed among the 4 LPDDR3 Devices

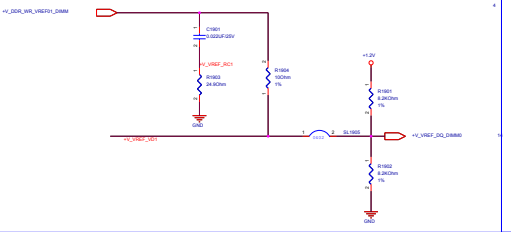


U58 LPDDR3 - 1866 MT/s DRAM 256Mb x 32 (1024MB) 1st: P/N: 03009-00058500 SAMSUNG/K4E8E324XB-EGCF 2nd: P/N: 03009-00096900 MICRON/MT52L256M32D1PF-107WT:B	**U59 LPDDR3 - 1866 MT/s DRAM 512Mb x 32 (2048MB)** 1st: P/N: 03009-00052300 SAMSUNG/K4E8E324XB-EGCF 2nd: P/N: 03009-00033900 MICRON/MT52L512M32D2PF-107WT:B	**U56 LPDDR3 - 1866 MT/s DRAM 1024Mb x 32 (4096MB)** 1st: P/N: 03009-00158100 HYNIX/H9CCNNNCLTMLAR-NUD 2nd: P/N: 03009-00160300 MICRON/MT52L1G32D4PG-107WT:B

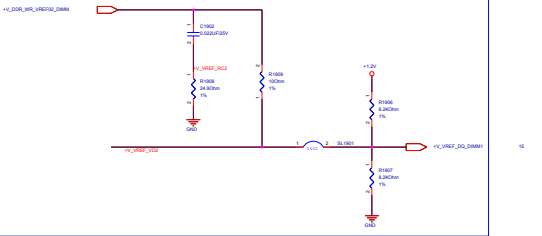
Custom Name:			
ASUS Computer Inc.	Project Name: UX430UQ		Rev: 0.1
Title:	LPDDR3_CH-B/4GB_S		
Size:	Dept: MB/NBQ	Engineer:	Mario_zhu
Date: Monday, December 28, 2015		Sheet 16 of 49	

Power plan:1.2V

CHA - VREF_DQ (All close to memory)



CHB - VREF_DQ (All close to memory)



VREF_CA (All close to memory)

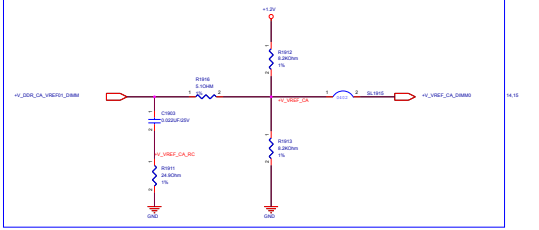
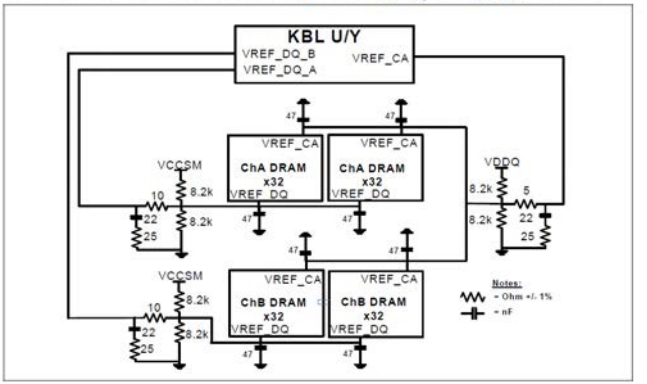
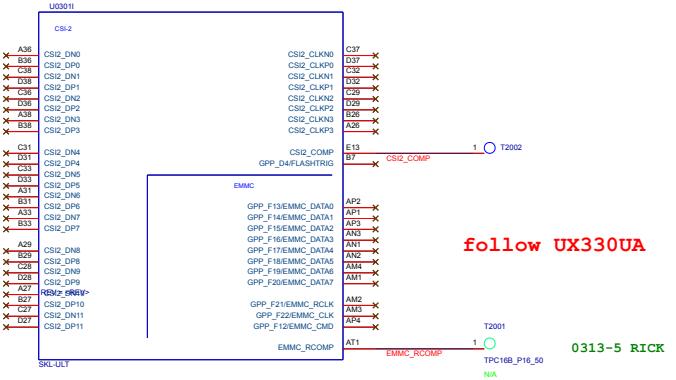


Figure 4-52. KBL U and KBL Y LPDDR3 x32 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



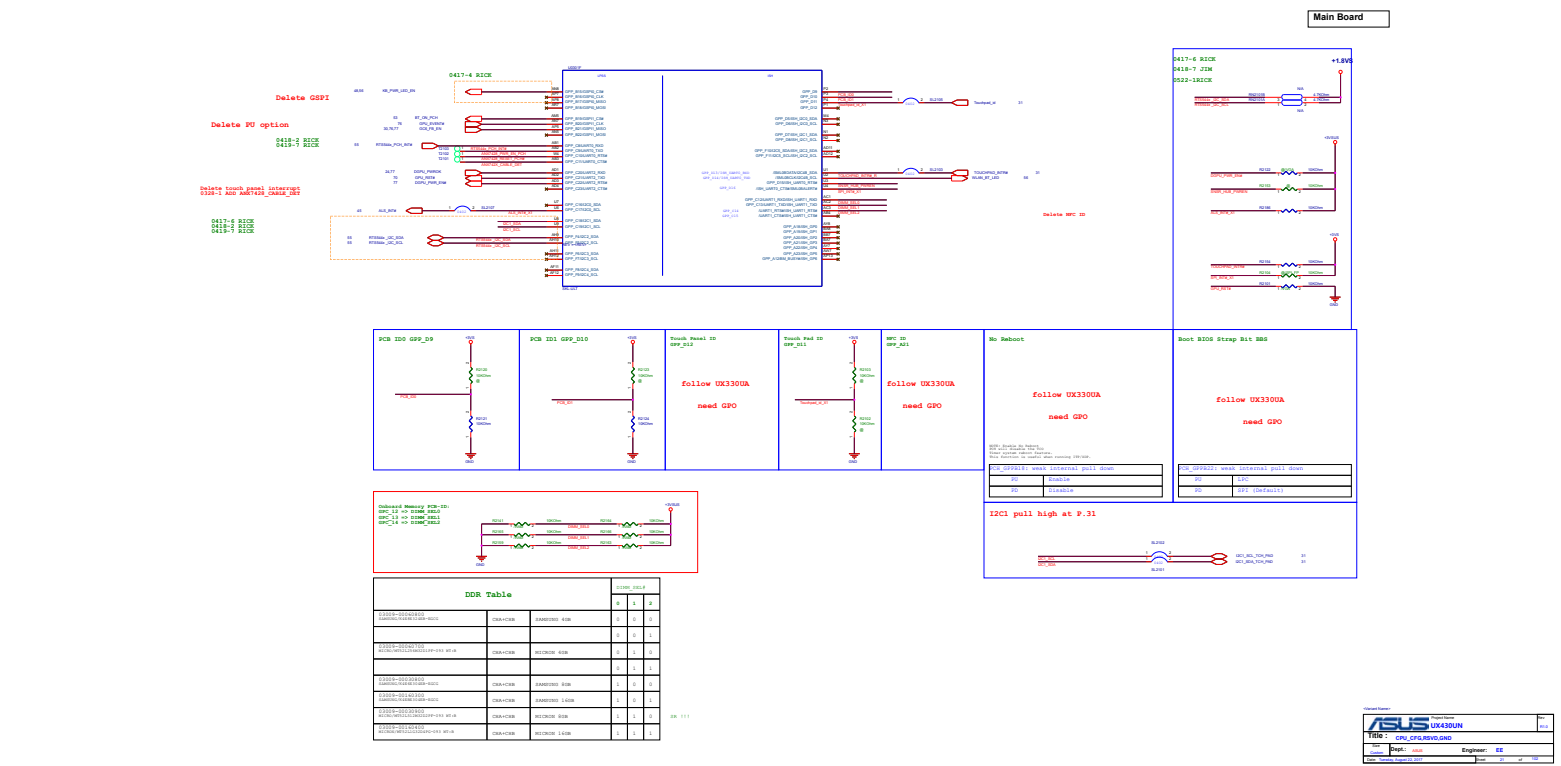
Project Name: UX430UQ			Rev: 0.1.0
Title : LPDDR3 CA_DQ VOLTAGE			
Size: Custom	Dept.:	Engineer: Mario_Jhu	
Date: Tuesday, August 22, 2017	Sheet 16 of 102		



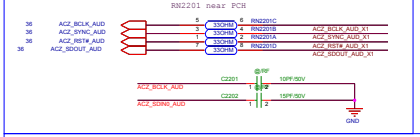
<Variant Name>

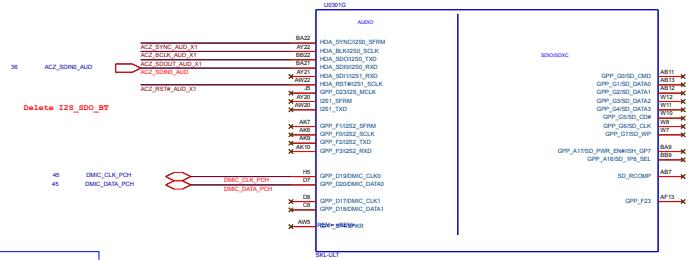
ASUS	Project Name: UX430UN	Rev: R1.0
Title : CPU_PCH_CSI2,EMMC		
Size: B	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 20 of 102	

Main Board


Delete GSPI
Delete PU option
Delete touch panel interrupt
0328-1 ADD A4E7528_CABLE_DET
0417-4 RICK
0417-6 RICK
0418-2 RICK
0419-7 RICK
0418-2 RICK
0419-7 RICK
Delete MFC ID
0417-6 RICK
0418-7 JIM
0522-1RICK
+1.8VS
PCB ID0 GPP_D9
PCB ID1 GPP_D10
Touch Panel ID
GPP_D12
follow UX330UA
need GPO
Touch Pad ID
GPP_D11
follow UX330UA
need GPO
MFC ID
GPP_A21
follow UX330UA
need GPO
No Reboot
follow UX330UA
need GPO
Boot BIOS Strap Bit BBS
follow UX330UA
need GPO
PCH_GPP921: weak internal pull down
PU Enable
PD Disable
PCH_GPP922: weak internal pull down
PU LPC
PD SPI (Default)
I2C1 pull high at P.31
Onboard Memory PCB-ID:
SPC_13 => DIMM_SEL0
SPC_14 => DIMM_SEL1
DDR Table
DIMM SELE
0
1
2
ER !!!
UX430UN
CPU_CFG,RSVD,GND
Engineer: EE

HD Audio



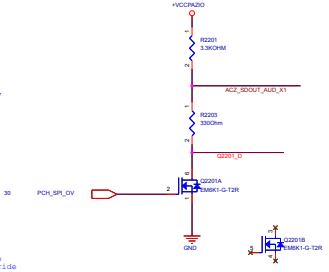


FLASH DESCRIPTOR STRAP

EDS 31.7.1.3

HDA_SDO
0=Enable
1=Disable Override

ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V (2) ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V



ACZ_SDOUT is a signal used for Flash DesCriptor security Override/ME debug mode
HIGH : get overridden, LOW : disable override

Intel: To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 KΩ to 2.2 KΩ ±5% resistor.

Top-Block Swap Override

follow UX330UA

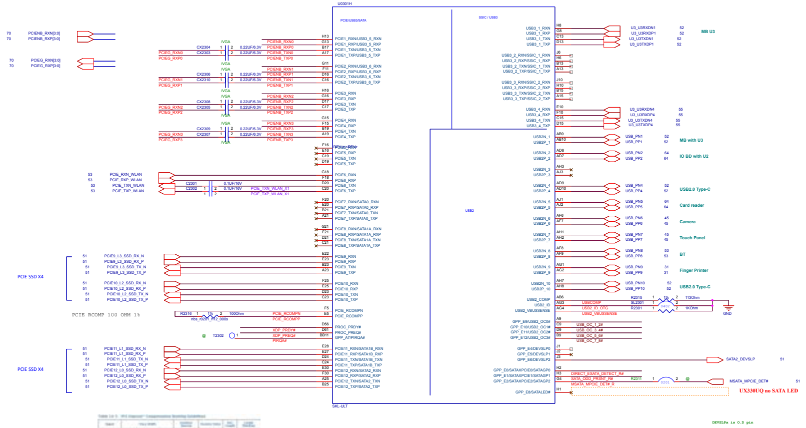
need GPO

PCH_GPPB14: weak internal pull down

PU	Enable
PD	Disable (default)

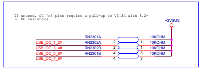
<Variant Name>

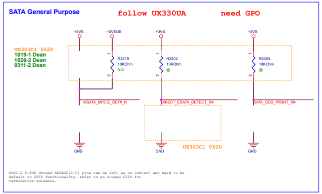
ASUS	Project Name: UX430UN	Rev: R1.0
Title : CPU_PCH_AUDIO,SDIO,SDXC		
Size: C	Dept.: ASUS	Engineer: EE
Date: Wednesday, May 31, 2017	Sheet 22 of 102	



	USB 2.0
1	MB U3 port
2	IO BD U2 port
3	
4	TYPE-C
5	Card reader
6	Camera
7	Touch Panel
8	BT
9	Finger Printer
10	TYPE-C

	USB 3.0
USB3_1	USB 3.0 Port (MB)
USB3_2	
USB3_3	
USB3_4	USB 3.0 Port (Type C)





SATA PORT	SATA USAGE DEFAULT/OPTION
PORT #0	N/A
PORT #1A	N/A
PORT #1B	N/A
PORT# 2	SSD

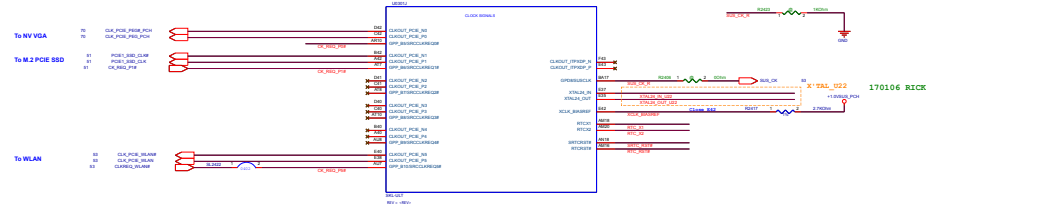
OPTION PCIE

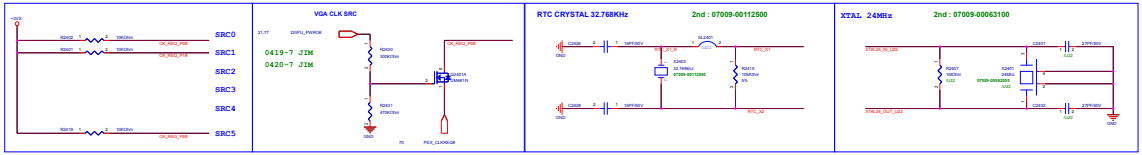
PCIE-Lane Reversal Enable/Disable !!!

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
Reversal Disable! PCIE #1	DGPU -> Lane 0		Port0
PCIE #2	DGPU -> Lane 1		
PCIE #3	DGPU -> Lane 2		
PCIE #4	DGPU -> Lane 3		
Reversal Disable! PCIE #5	N/A		
PCIE #6	WLAN		
PCIE #7/SATA #0	N/A		
PCIE #8/SATA #1A	N/A		Port5
Reversal Enable! PCIE #9	M2.SSD -> Lane 3		Port1
PCIE #10	M2.SSD -> Lane 2		
PCIE #11/SATA #1B	M2.SSD -> Lane 1		
PCIE #12/SATA #2	M2.SSD -> Lane 0	M2.SSD(SATA #2)	

<Variant Name>

Project Name: UX430UN		Rev: R1.0
Title : CPU_PCH_PCIE,USB,SATA		
Size: Custom	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 23 of 102	

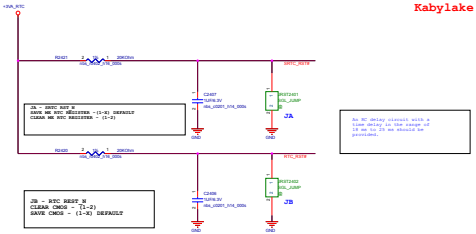




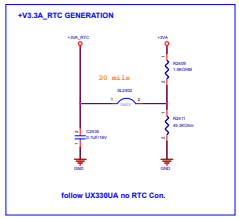
Note: Any no-used CK410BQR signal not mapped to a Down Device or Connector/ASD-to Card Device should be disabled in BIOS to save power. They must be left as no connects at the SOC side on the platform. (ERS1202 2.0)?

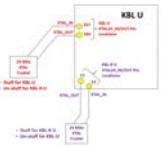
Note: The CK410BQR signals can be configured to map to any of the DOS ICS Expander Root Ports while using any of the CLK600_DOS_F/H differential clock pairs (ERS1202 2.0)?

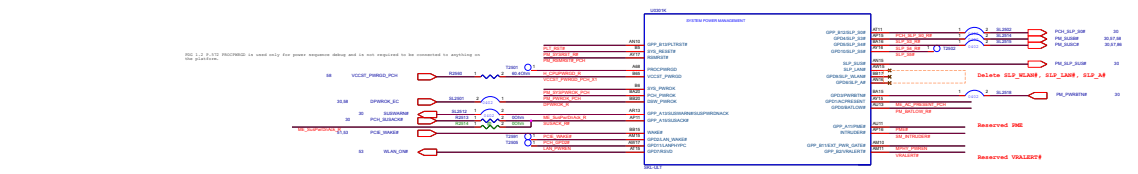
Kabylake +3VA_RTC MAX:3.2V min:3.0V 0512



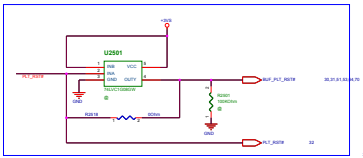
An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided.



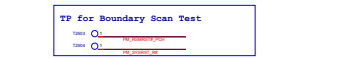




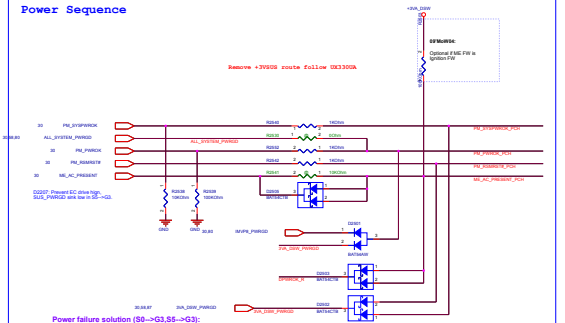
follow UX330UA use short land

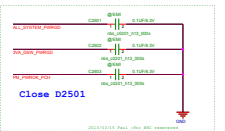


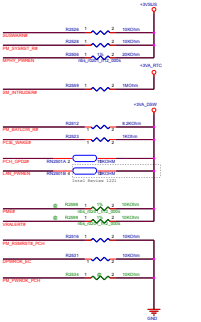
TP for Boundary Scan Test



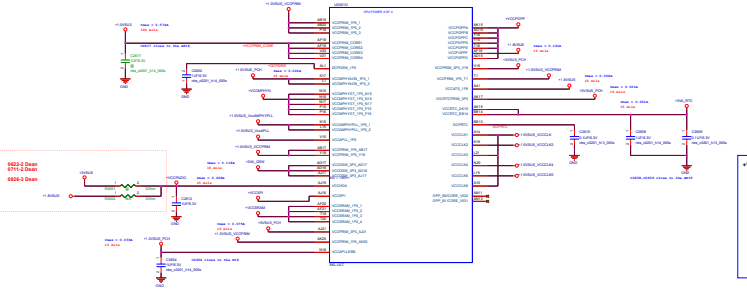
Power Sequence



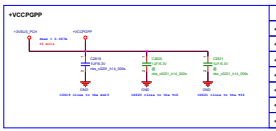




<Variant Name>	Project Name: UX430UN		Rev: 01.2
Title :	CPU_PCH_SYS_POWER		
Size: Custom	Dept.: FAE/S	Engineer: EE	
Date: Tuesday, August 22, 2017	Sheet 20 of 100		

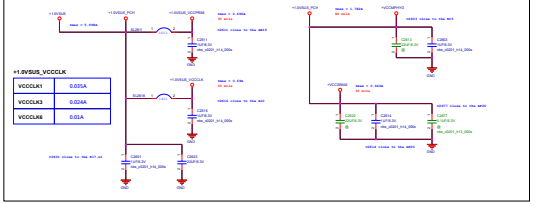


5622-2 Dean
5711-2 Dean
5826-3 Dean



	3.3V	1.8V
+VCCPGPA	0.002A	0.009A
+VCCPGPB	0.004A	0.002A
+VCCPGPC	0.006A	0.003A
+VCCPGPD	0.008A	0.003A
+VCCPGPE	0.006A	0.002A
+VCCPGPF	1.8V only	0.161A
+VCCPGPG	0.041A	0.056A

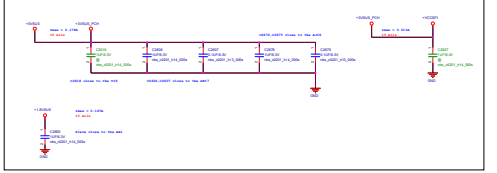
+1.0VSUS



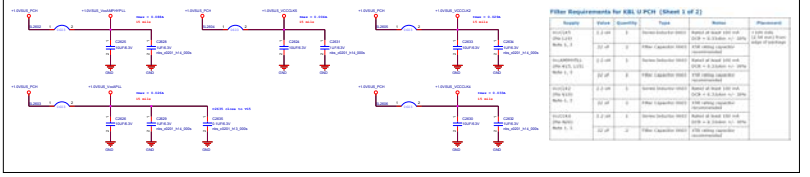
+1.0VSUS_VCCCLK

VCCCLK1	0.035A
VCCCLK3	0.026A
VCCCLK6	0.01A

+3VSUS / +1.8VSUS



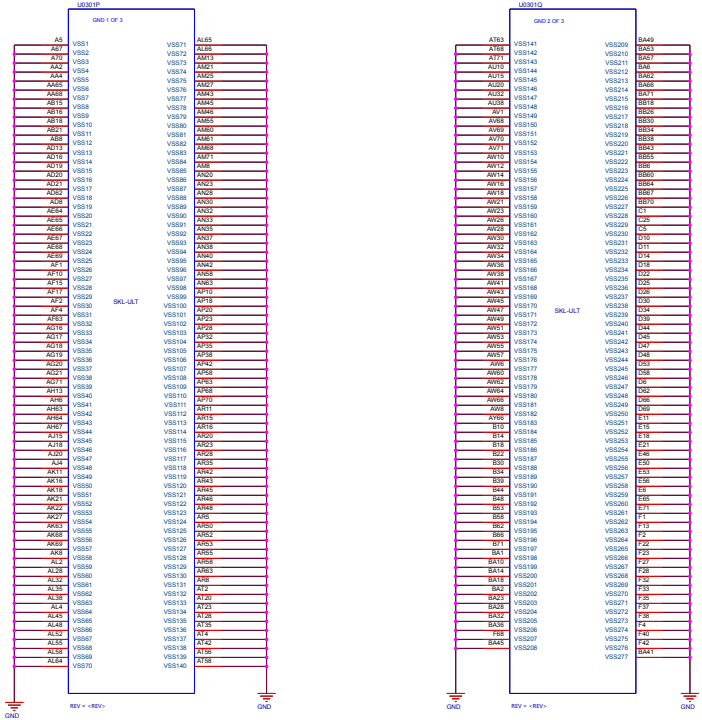
Filter requirement for +1.0VSUS

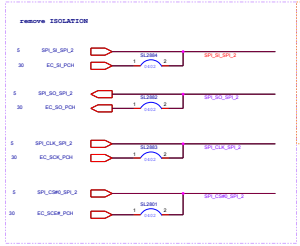


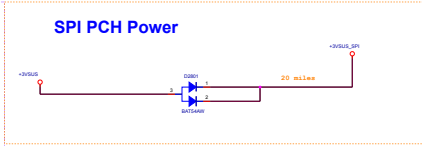
Filter Requirements for KBL U PCH (Sheet 1 of 2)

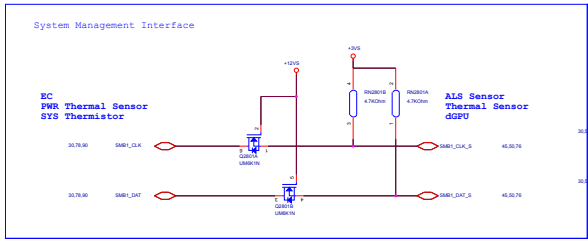
Supply	Value	Quantity	Type	Notes	Placement
VccCLK1 (Pin L27) Note 1, 3	2.2 uH	1	Ferrite Inductor SMD	Rated at least 400 mA DCR = 0.3 ohm +/- 20%	< 500 mils (1.54 mm) from edge of package
	22 uF	1	Filter Capacitor SMD	ESR rating capacitor recommended	
VccMPHYPLL (Pin K1), L(2) Note 1, 3	2.2 uH	1	Ferrite Inductor SMD	Rated at least 100 mA DCR = 0.3 ohm +/- 20%	
	22 uF	2	Filter Capacitor SMD	ESR rating capacitor recommended	
VccCLK3 (Pin K23) Note 1, 3	2.2 uH	1	Ferrite Inductor SMD	Rated at least 100 mA DCR = 0.3 ohm +/- 20%	
	22 uF	1	Filter Capacitor SMD	ESR rating capacitor recommended	
VccCLK6 (Pin N23) Note 1, 3	2.2 uH	1	Ferrite Inductor SMD	Rated at least 100 mA DCR = 0.3 ohm +/- 20%	
	22 uF	2	Filter Capacitor SMD	ESR rating capacitor recommended	

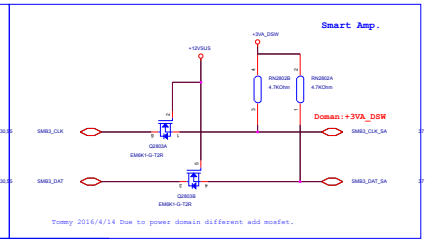
Title :	CPU_PCH_POWERLOAD
Project Name	UX430UN
Rev	2.0
Custom	Dept.: AMUS
Engineer:	EE
Date: Tuesday, August 04, 2015	Sheet 38 of 100

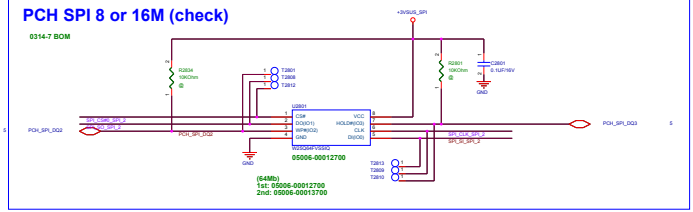

U0301P
GND 1 OF 3
SKL-ULT
REV = <REV>
GND
U0301Q
GND 2 OF 3
SKL-ULT
REV = <REV>
GND
U0301R
GND 3 OF 3
SKL-ULT
GND











<variant_name>

Project Name: UX430UN		Rev: R1.0
Title : PCH-SPI ROM.OTH		
Size: A3	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet: 28	of: 102

EC 8995

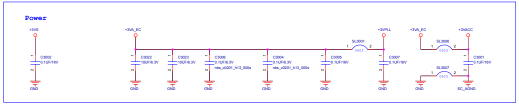
Only 3V Torlence

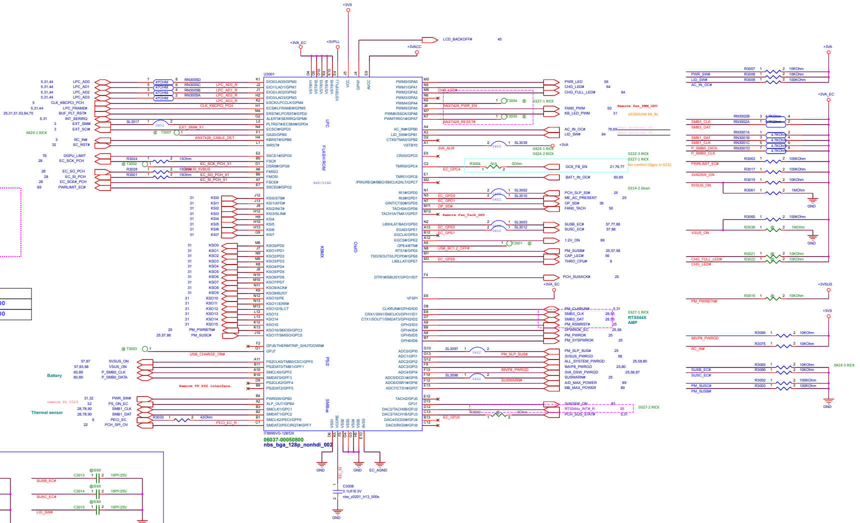
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

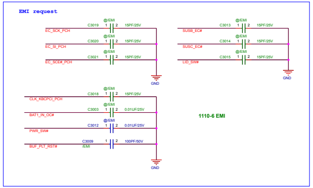




0327-1 RICK

ANX7428 CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

ITE Version	ASUS P/N
IT8995E-128/DX	06037-00050700
IT8995VG-128/DX	06037-00050800



<Variant Name>

Project Name	UX430UN		Rev R1.0
Title :	CR_KBC_IT8521		
Size C	Dept.: ASUS	Engineer: EE	
Date: Tuesday, August 22, 2017		Sheet 30	of 102

Reserved for EMI

1102-1 Dean
1104-2 Dean
1117-3 Dean

Keyboard_CON.

0826-2 Dean

12015-00260000

BL_CON.

1105-1 Dean

12015-00602900

0220-1 RICK

KB BL組裝方式.

Touch Pad & FP

Finger Printer (USB)

87034-60200200

同面cable !!

3D Mils

12015-00214300

1105-1 Dean

Del SPI to Finger print.

TPM

/BIOS Disable is only for NPCT.gen to disable TPM under BIOS setting

1116-4 Dean

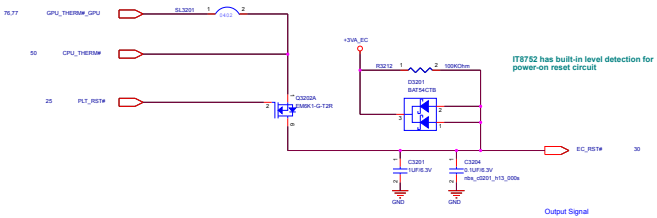
09120-00010800

BA100	SELECT CODE
0	BEN → KYS
1	TBEL → TPS

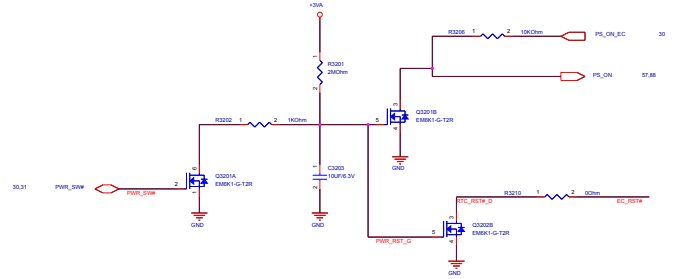
1202-3 Dean
1207-2 Dean

Project Name	UX430UN
Title :	EC_KB_TP
Dept:	MSD
Engineer:	EE
Date:	Tuesday, August 29, 2017

Thermal Policy



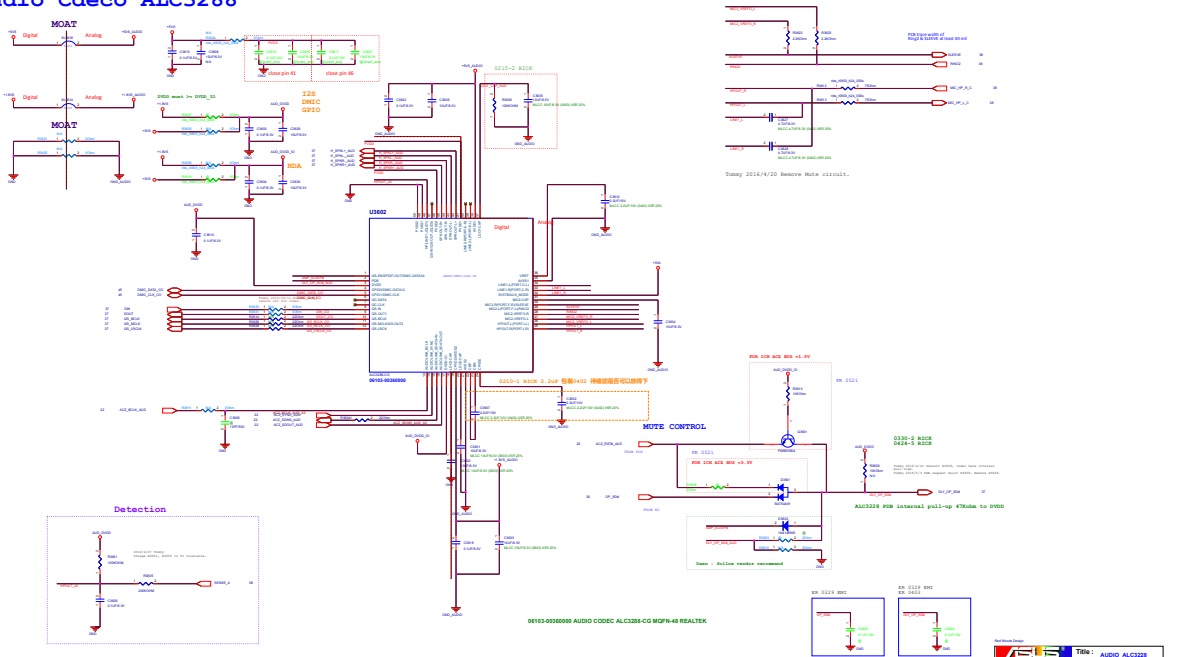
battery embedded (press pwr_sw 10sec, then reset ec)

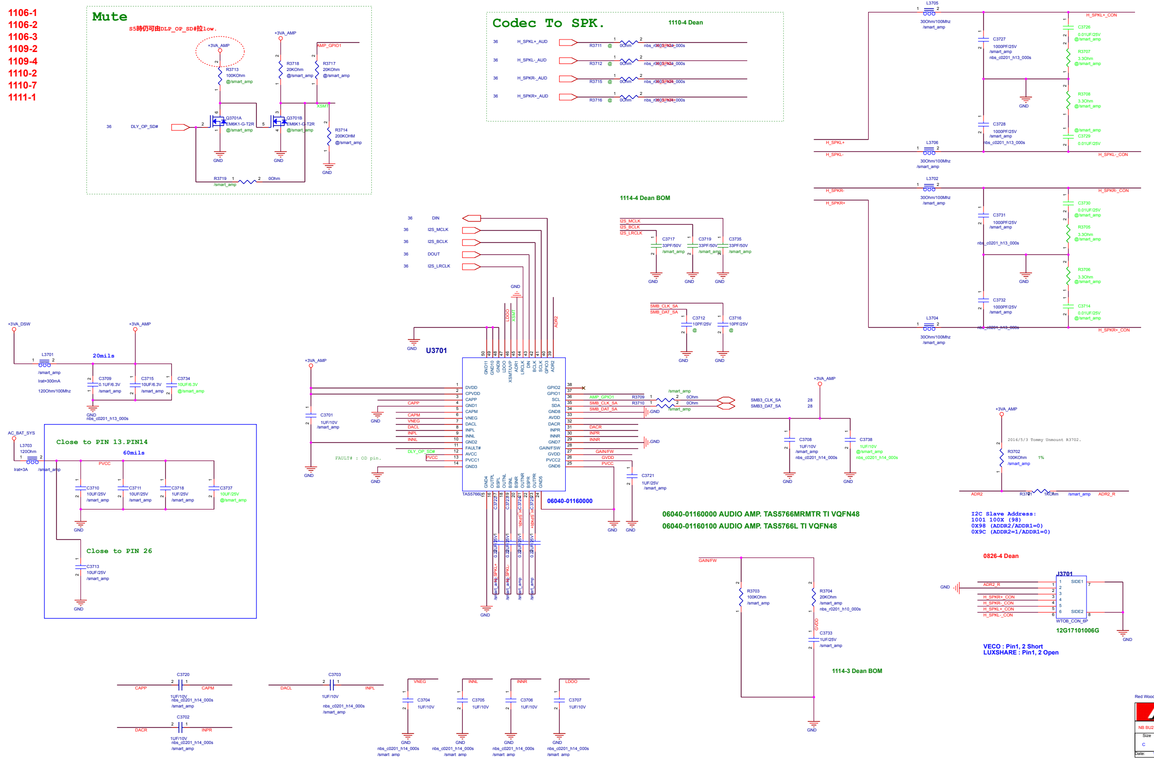


<Variant Name>

ASUS	Project Name: UX430UN	Rev: R1.0
Title : RST_Reset Circuit		
Size: B	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 32 of 102	

Audio Cdeco ALC3288





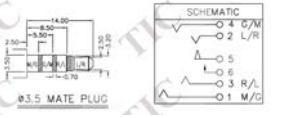
Red Woods Design			
NB BU2	Title :		
	Engineer:	Div3.Dep2.Sec1	
Size C	Project Name UX430UN		Rev R1.0
Date: Tuesday, August 22, 2017	Sheet 37 of 102		

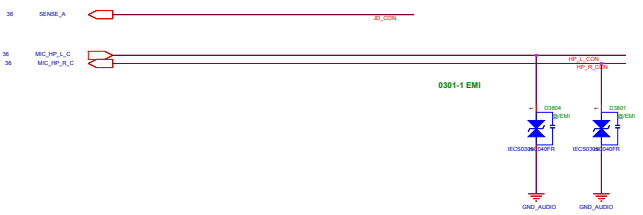
Audio Jack

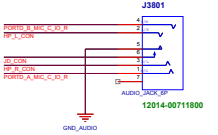
Replaced L6404-L6407 to 00hm (6/3)
C6431-C6434 changed to 22pF and mounted (8/19)
R6645, R6644, R6643, R6642 changed to 22 Ohm (8/18)

1116-1 Dean
1207-4 EMI
0106-7 Dean

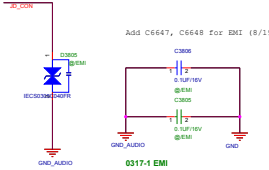
JD pin = Normal open.







Diode's GND changed 4/21



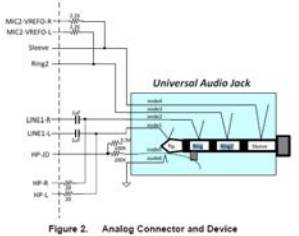


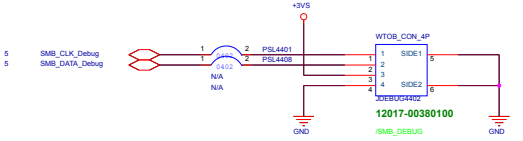
Figure 2. Analog Connector and Device

<Variant Name>

ASUS	Title : ****	
	Engineer: EE	
Size: B	Project Name: UX430UN	Rev: R1.0
Date: Tuesday, August 22, 2017	Sheet 38 of 102	

1216-1 ECN Remove Debug IO/RF CLIP/TYPE-C CONN 12013-00117500 Foxconn用料
UA:EN-0248068-R UQ:EN-0248045-R

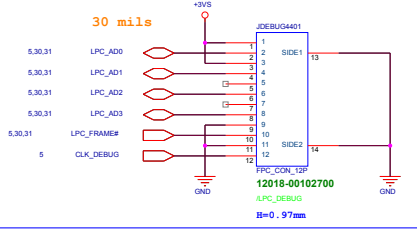
New Design Debug Port



Old Design Debug Port

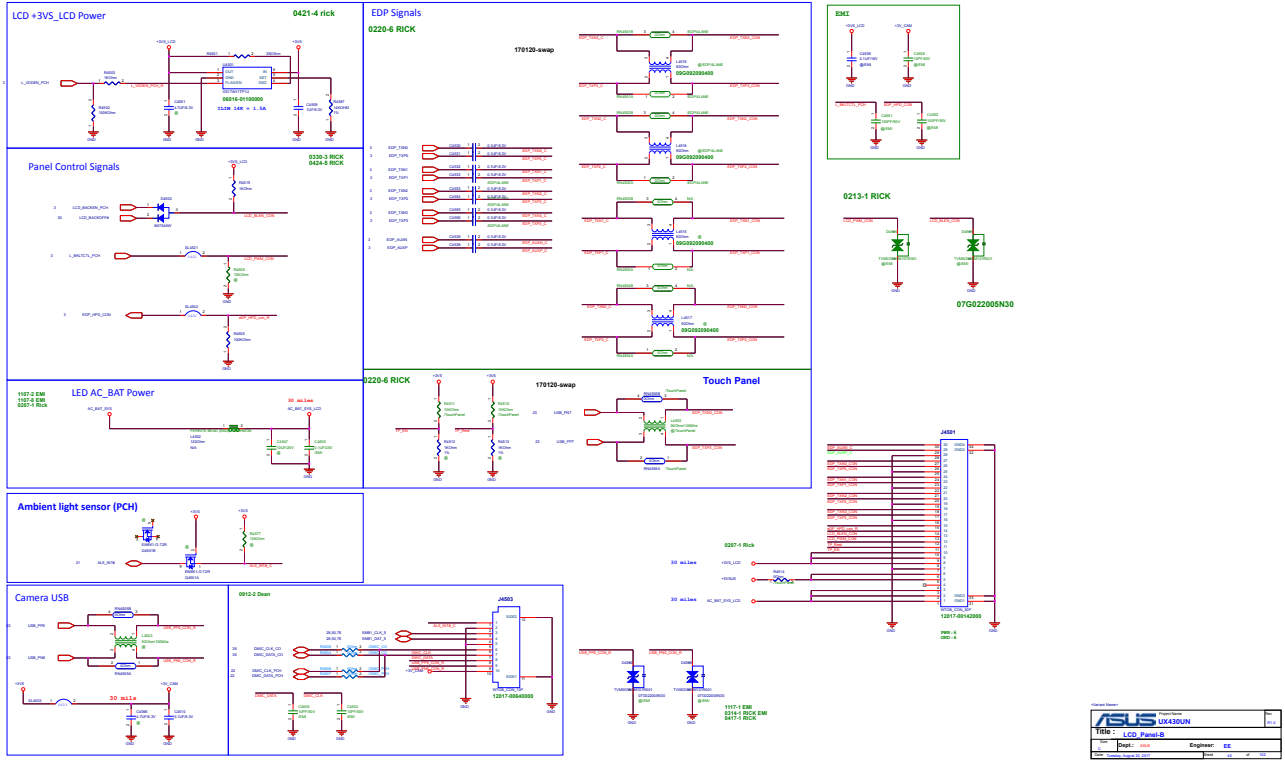
NPI Use

LPC Debug Port 同面cable.

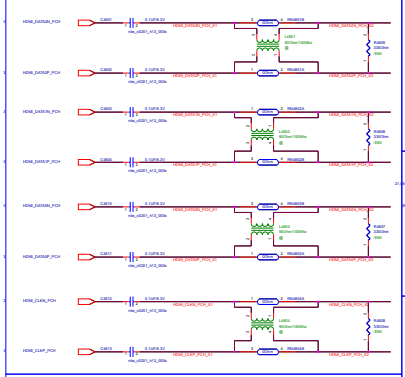


<Variant Name>

Project Name: UX430UN		Rev: R1.0
Title : BUG_Debug		
Size: A4	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 44 of 102	

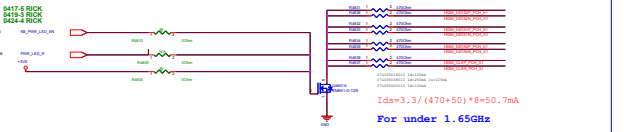

LCD +3VS_LCD Power
0421-4 rick
Panel Control Signals
0330-3 RICK
0424-5 RICK
LED AC_BAT Power
1107-2 EMI
1107-2 EMI
0207-1 Rick
Ambient light sensor (PCH)
Camera USB
0912-2 Dean
EDP Signals
0220-6 RICK
170120-swap
Touch Panel
EMI
0213-1 RICK
07G022005N30
J4501
12017-00142000
J4503
12017-00640000
1107-1 EMI
0314-1 RICK EMI
0417-1 RICK
Project Name
UX430UN
Title
LCD_Panel-B
Engineer:
EE

HDMI Signals

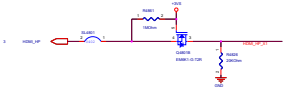


HDMI Power

HDMI Cost-reduced Level shiter

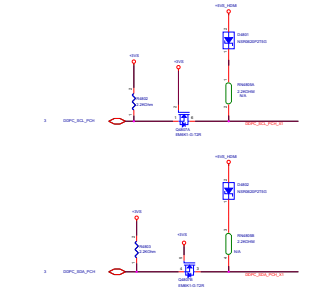


HDMI HPD

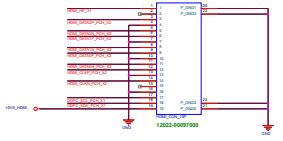


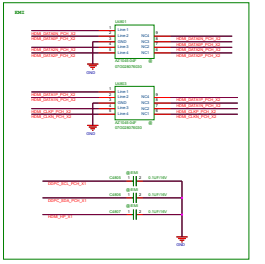
HDMI DDC Level-shifter

0301-3 RICK



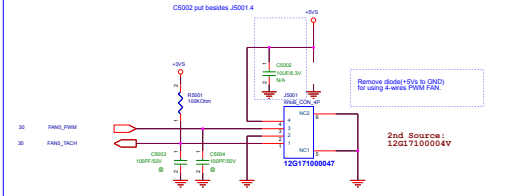
HDMI CON.





PWM Fan

1106-2 Dean
0425-2 Rick

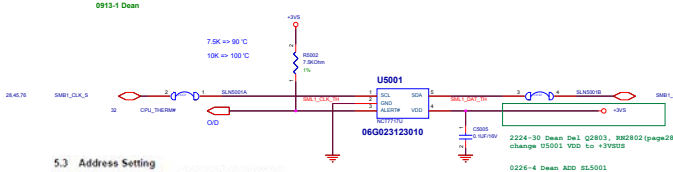


GPU Thermal Sensor

Tung, 0302-6 Add GPU Thermal Sensor (PS0)

CPU Thermal Sensor

0913-1 Dean



2224-30 Dean Del Q2803, RM2802(page28)
change U5001 VDD to +3VSUS

0226-4 Dean ADD SL5001

0304-1 Dean modify SMBus(EC_PD & Thermal sensor都接+3VS)

0307-3 Dean change SLN6102A to SLN5001A

5.3 Address Setting

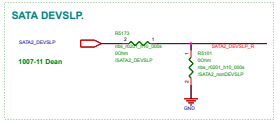
NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

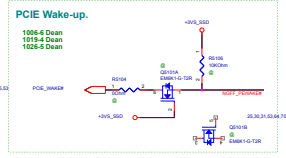
5.6 ALERT# point hardware power-on setting (TBD)

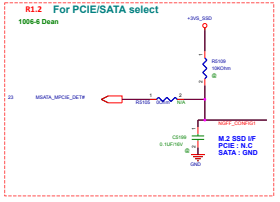
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

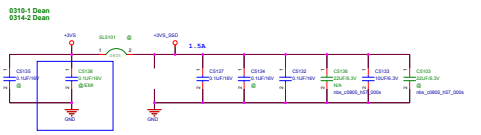
PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.6KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

SSD CONN.

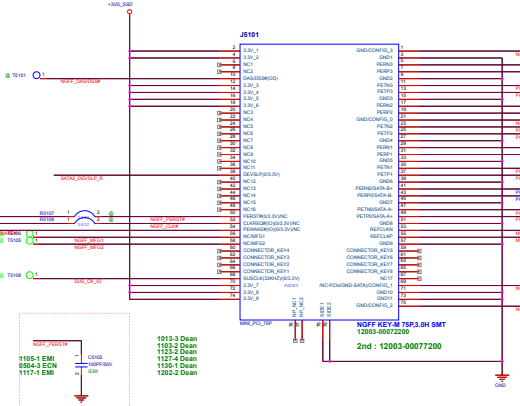








6/8 Jacky add 0.1UF for ESD



36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

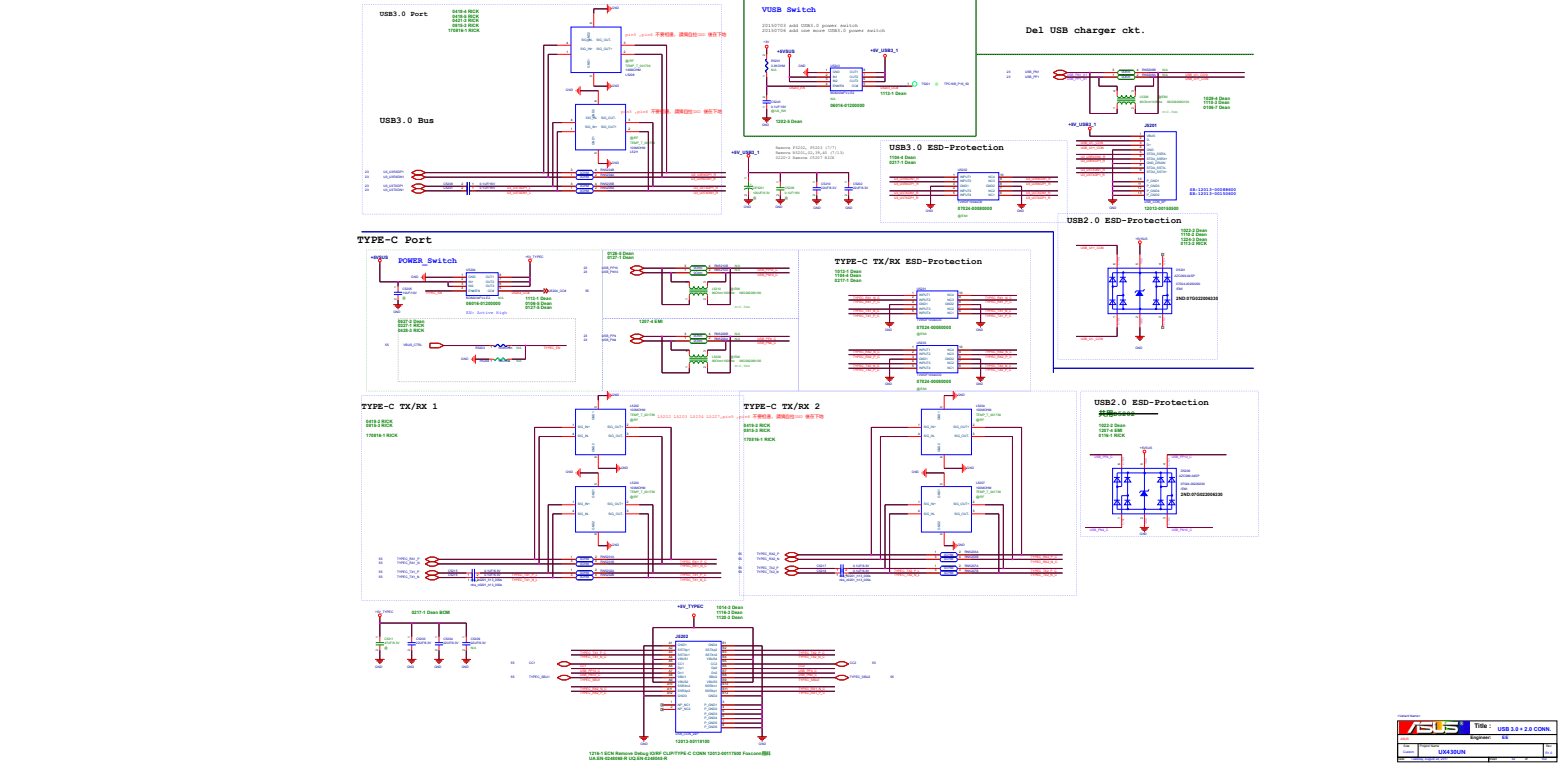
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

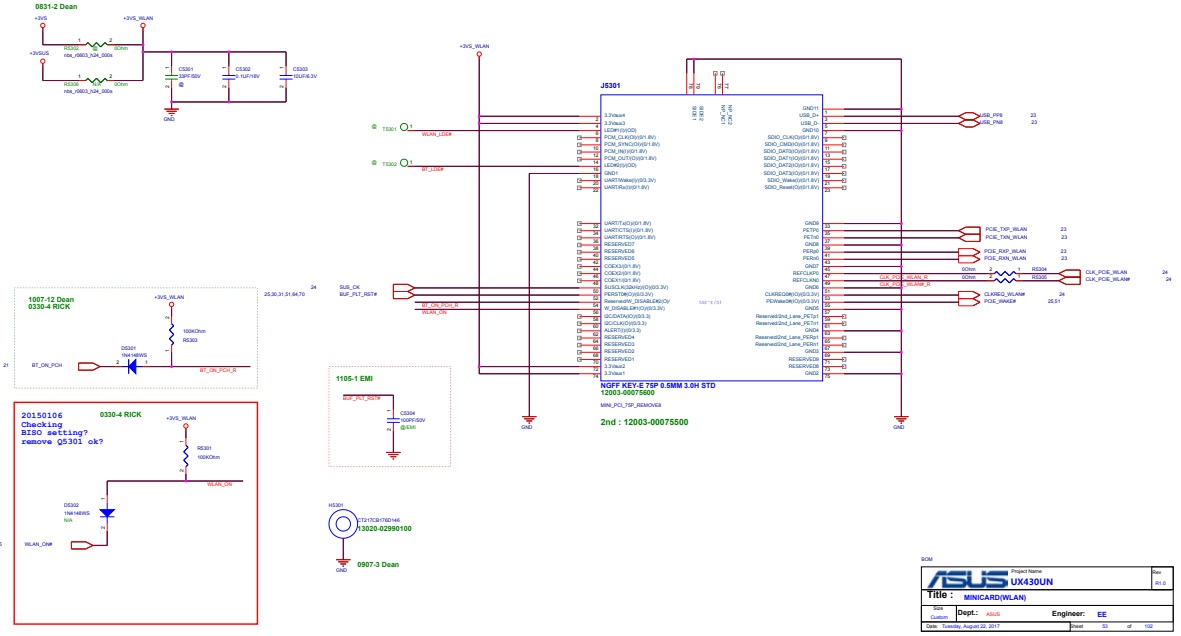
Table 36-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None	None[2]

BOM			
ASUS	Project Name: UX430UN		Rev: R1.0
Title :	SATA HDD & ODD		
Size: Custom	Dept.:	Engineer: EE	
Date: Tuesday, August 22, 2017		Sheet 51 of 102	

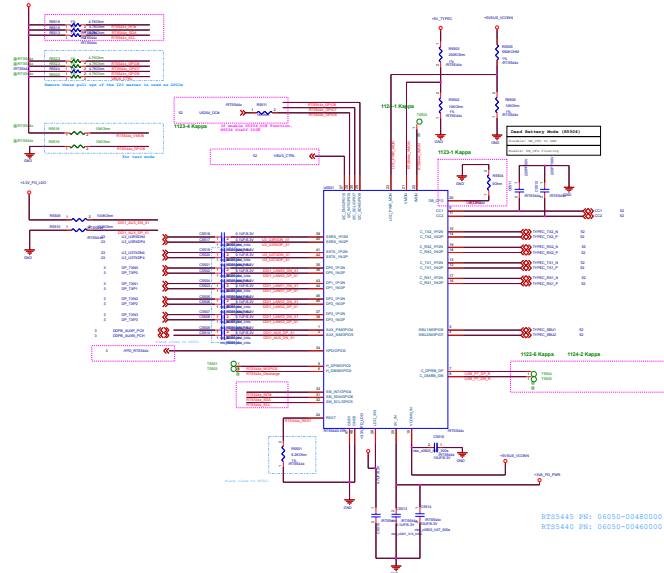

USB3.0 Port
USB3.0 Bus
VUSS Switch
20150703 add USB3.0 power switch
20150706 add one more USB3.0 power switch
Del USB charger ckt.
USB3.0 ESD-Protection
USB2.0 ESD-Protection
TYPE-C Port
POWER_Switch
TYPE-C TX/RX ESD-Protection
TYPE-C TX/RX 1
TYPE-C TX/RX 2
USB2.0 ESD-Protection
Title : USB 3.0 + 2.0 CONN.
Engineer: SS
LIX43GUN

WLAN con.


0831-2 Dean
+3VS
+3VS_WLAN
+3VSUS
RS302
nbk_r0603_h24_000x
0Ohm
RS306
CS301
10PF/50V
CS302
0.1UF/16V
CS303
10UF/6.3V
GND
+3VS_WLAN
TS301
WLAN_LOE#
TS302
BT_LOE#
J5301
3.3Vdual4
3.3Vdual3
LED#1(o)(OD)
PCM_CLK/O(I)(SI1.8V)
PCM_SYNC/O(I)(SI1.8V)
PCM_IN(I)(SI1.8V)
PCM_OUT(O)(SI1.8V)
LED#0(o)(OD)
GND1
UART:Wake(o)(SI3.3V)
UART:Rx(I)(SI1.8V)
UART:Tx(O)(SI1.8V)
UART:CTS(I)(SI1.8V)
UART:RTS(O)(SI1.8V)
RESERVED7
RESERVED6
RESERVED5
CODEX(I)(SI1.8V)
CODEX(O)(SI1.8V)
SUSCLK(32kHz)(O)(SI3.3V)
PERST0#(O)(SI3.3V)
Reserved/W_DISABLE#2(O)(SI3.3V)
W_DISABLE#1(O)(SI3.3V)
GCOATA/CS(O)(SI3.3)
GCCLK(O)(SI3.3)
ALERT(I)(SI3.3)
RESERVED4
RESERVED3
RESERVED2
RESERVED1
3.3Vdual2
3.3Vdual1
GND11
USB_D+
USB_D-
GND10
SDIO_CLK(O)(SI1.8V)
SDIO_CMD(I/O)(SI1.8V)
SDIO_DAT3(I/O)(SI1.8V)
SDIO_DAT2(I/O)(SI1.8V)
SDIO_DAT1(I/O)(SI1.8V)
SDIO_DAT0(I/O)(SI1.8V)
SDIO_Wake(I)(SI1.8V)
SDIO_Reset(O)(SI1.8V)
GND9
PETP0
PETN0
GND8
PERP0
PERN0
GND7
REFCLKP
REFCLKN
GND6
CLKREQ0#(O)(SI3.3V)
PEWake0#(O)(SI3.3V)
GND5
Reserved/2nd_Lane_PETp1
Reserved/2nd_Lane_PETn1
GND4
Reserved/2nd_Lane_PERp1
Reserved/2nd_Lane_PERn1
GND3
RESERVED0
GND2
NGFF KEY-E 75P 0.5MM 3.0H STD
12003-00075600
MINI_PCI_75P_REMOVE#
2nd : 12003-00075500
USB_PP8
USB_PN8
PCIE_TXP_WLAN
PCIE_TXN_WLAN
PCIE_RXP_WLAN
PCIE_RXN_WLAN
0Ohm
RS304
RS305
CLK_PCIE_WLAN
CLK_PCIE_WLAN#
CLK_PCIE_WLAN_R
CLK_PCIE_WLAN#_R
CLKREQ_WLAN#
PCIE_WAKE#
SUS_CK
BUF_PLT_RST#
BT_ON_PCH_R
WLAN_ON
1007-12 Dean
0330-4 RICK
+3VS_WLAN
100KOhm
RS303
DS301
1N4148WS
BT_ON_PCH
1105-1 EMI
CS304
150PF/50V
@EMI
20150106
Checking
BISO setting?
remove Q5301 ok?
0330-4 RICK
DS302
1N4148WS
N/A
WLAN_ON#
HS301
13020-02990100
0907-3 Dean
GND
BOM
Project Name
UX430UN
Rev
R1.0
Title :
MINICARD(WLAN)
Size
Custom
Dept.:
ASUS
Engineer:
EE
Date:
Tuesday, August 22, 2017
Sheet
83
of
102

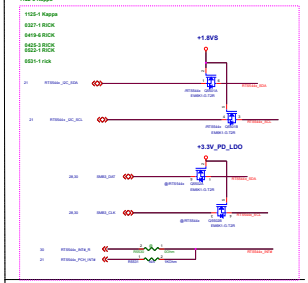
Type-C Controller

1122-1 Kappa

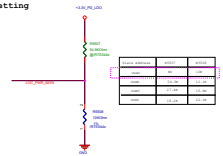


I2C To EC:

1122-6 Kappa



Slave Addr. Setting

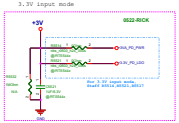


Slave_Address	ADDR1	ADDR0
0x4E	Vss	Vss
0x4F	Vss	Float
0x4C	Float	Vss
0x4D	Float	Float

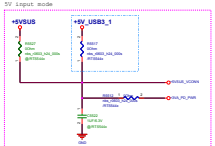
Power

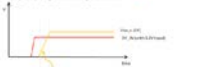
1122-6 Kappa 1124-4 Kappa

3.3V input mode



5V input mode



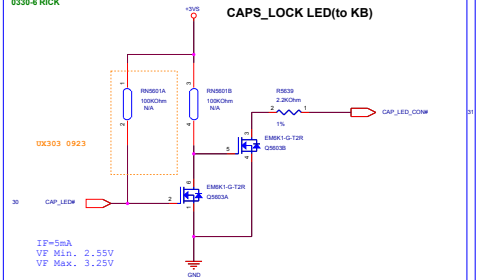


1123-2 Kappa

ASUS	Project Name: UX310		Rev: 0.1
Title : RTS544x			
Size:	Dept: Customer Experience Engineer: EE		
Date: Wednesday, May 31, 2017	Sheet 01 of 13		

0330-6 RICK

CAPS_LOCK LED(to KB)

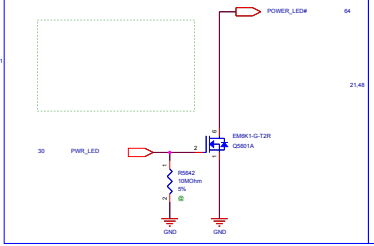


PWR LED(to IO BD)

ER-017

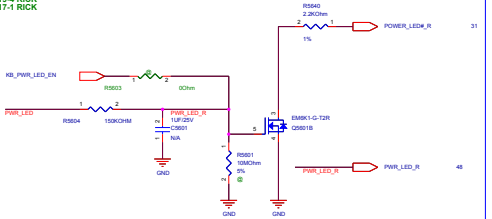
UX31EP 024 01/18

1119-6 Dean
0920-2 Dean



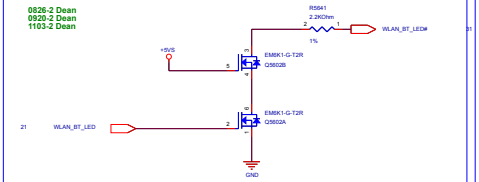
PWR LED(to KB)

1103-1 Dean
0417-4 RICK
0419-1 RICK
0419-4 RICK
0517-1 RICK



WireLess/BT LED(to KB)

0826-2 Dean
0920-2 Dean
1103-2 Dean



WirelessLAN & Bluetooth Status LED

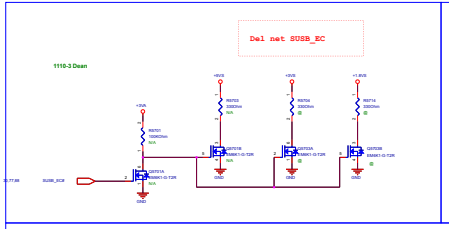
Charger LED

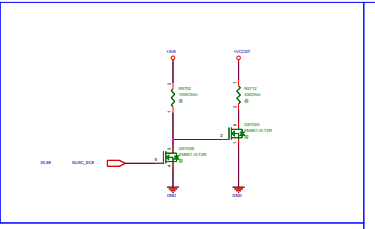
Change Charger LED 07014-00190300 (1015)

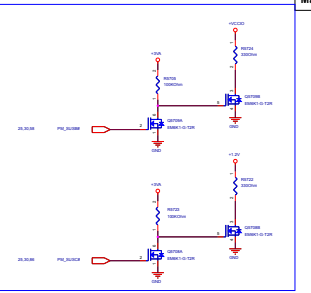
WHITE	ORANGE
IF = 5.6~6.5mA	IF = 7.88~9.1mA
VF Typ. = 2.85V	VF Typ. = 2.0V
VF Max. = 3.15V	VF Max. = 2.4V

<Variant Name>

ASUS	Title : HALL_SW	
	Engineer: EE	
Size: Custom	Project Name: UX430UN	Rev: R1.0
Date: Tuesday, August 22, 2017	Sheet 56 of 102	

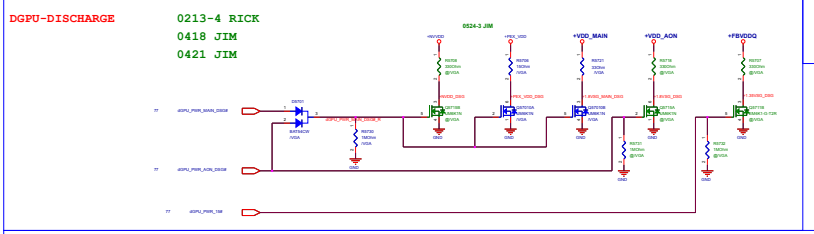


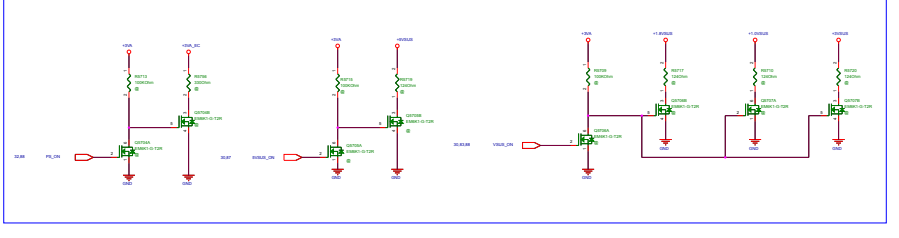




DGPU-DISCHARGE

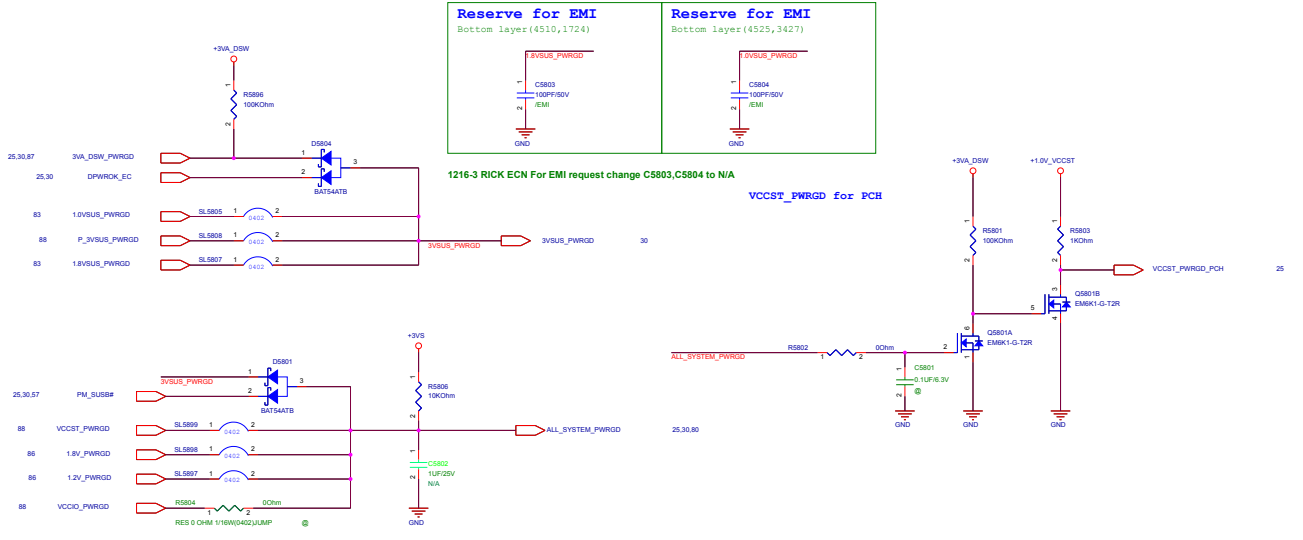
0213-4 RICK
0418 JIM
0421 JIM





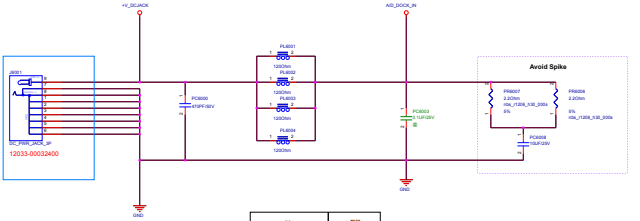
<Variant Name>

ASUS	Project Name: UX430UN		Rev: R1.0
Title : DSG_Discharge			
Size: Custom	Dept.: ASUS	Engineer: EE	
Date: Tuesday, August 02, 2011	Sheet 97 of 102		



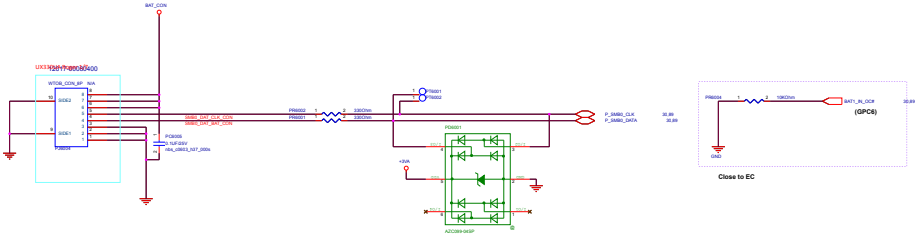
<Variant Name>

ASUS	Project Name: UX430UN	Rev: R1.0
Title : PRO_Protect		
Size: Custom	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 58 of 102	



瓦數	Boot 跳線
45W & 65W	3
90W	4

Battery Connector



Main Board

NUT

A

B

C TOP面件!!

E 0421-6 RICK

GND PAD

0220-3 RICK
0304-1 RICK

Screw Hole

D

E 0418-2 RICK
0418-6 RICK

F

G

H

I

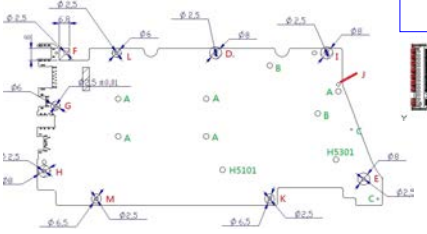
J

K

L 0220-3 RICK

M 1114-2 Dean

N



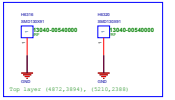
Project Name	UX430UN
Title :	
Engineer:	

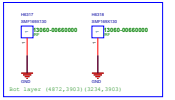
Spring

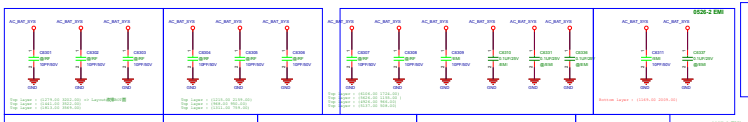
Clip

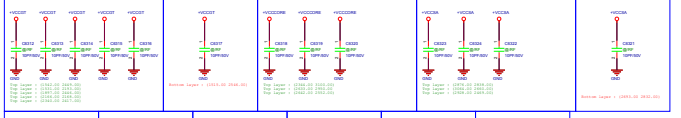
170815 RICK REMOVE SHIELDING CLIP H6305,H6306,H6307,H6308,H6309,H6311

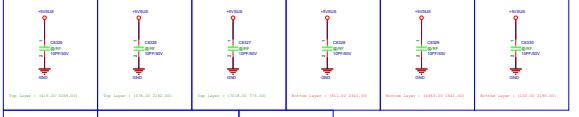
Gasket

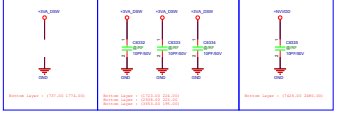












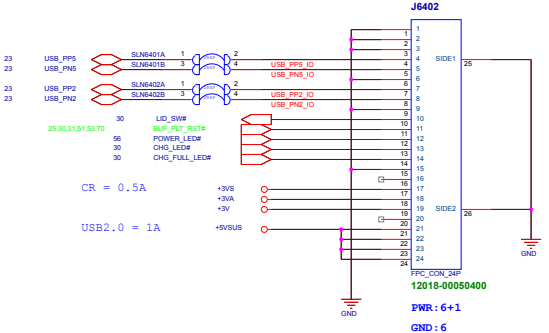
MB TO IO BD

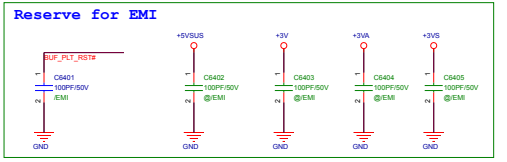
USB2.0 Port * 1, USB CR, Hall sensor, LEDs

1022-3 Dean
1104-1 Dean
1111-2 Dean
1119-6 Dean
0922-1 Dean
0221-4 RICK

R1.1 pin define有異動

異面cable !!





1110-6 EMI

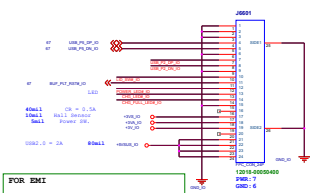
pin define 待確認...

<Variant Name>

ASUS	Title : IO_SATA HDD	
	Engineer: EE	
Size: Custom	Project Name: UX430UN	Rev: R1.0
Date: Tuesday, August 22, 2017	Sheet 64 of 102	

MB to IO CONN

1016-5 Dean
1028-1 Dean
1109-1 Kappa
1126-1 Kappa
0126-1 Kappa
0711-3 RICK
0922-1 Dean **Rt.1 pin define有異動**

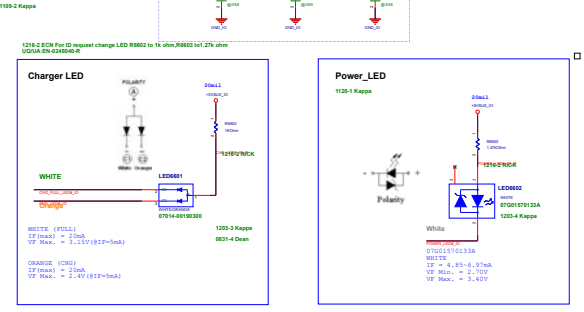


LEDs

1109-2 Kappa

FOR EMI 1207-1 Kappa

1216-2 ECN For ID request change LED R6602 to 1k ohm,R6603 to1.27k ohm
UQ/UA:EN-0248040-R

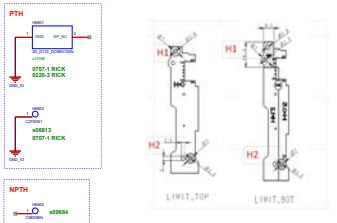


SCREW HOLE

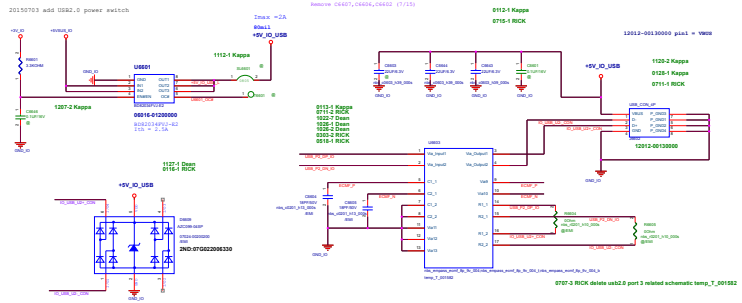
0907-2
0922-2

DXF - ux41_io_daf_outline_0620

0707-1 RICK

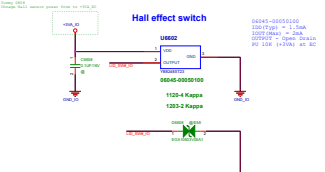


USB 2.0 Port



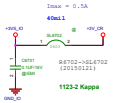
0707-3 RICK delete usb2.0 port 3 related schematic temp_T_001582

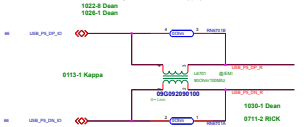
Hall Sensor

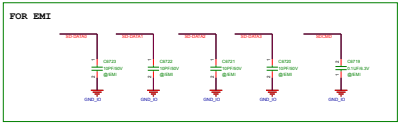


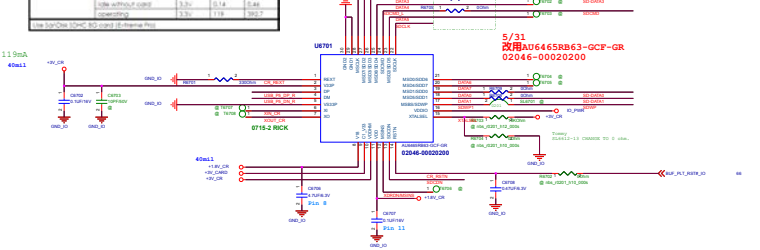
Title :	ID_BD-1		
Engineer:	EE		
Size	Project Name		Rev
Custom	UX430UN		R2.0
Date: Tuesday, August 02, 2016	Sheet 66 of 72		

USB
Card Reader





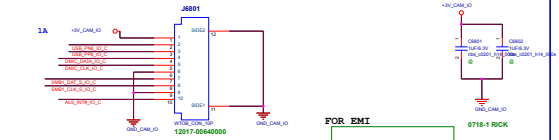




<Variant Name>
ASUSTeK COMPUTER INC.
Title : IO_BD-2(AU6465RB63)
Engineer: EE
Size: Custom
Project Name: UX430UN
Rev: R1.0
Date: Tuesday, August 22, 2017
Sheet: 37 of 52

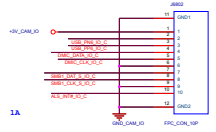
MB TO CAM BD

WtoB CON 10P Conn MB side. =12017-00640000
WtoB CON 10P Conn CAM BD side. = 12017-00640000



SCREW HOLE

CAM CONN



<Variant Name>

ASUSTeK COMPUTER INC	Title :	HDD_BD
	Engineer:	EE
Size: Custom	Project Name: UX430UN	Rev: R0.0
Date: Tuesday, August 22, 2017	Sheet 69 of 102	

0113-1 RICK

0419-7 JTM

0524-1 JTM

Place under GPU

170112-RICK
170123-RICK
170124-2 RICK

Place Near BALLS

Place Near GPU

3300 uA

0113-1 RICK

0216-1 RICK

Control Signal form PCH

需再確認

0125-1-RICK
0216-1 RICK
0216-6 RICK

Reserve for EMI

close to GPU

0905-1 Dean

1216-3 RICK ECN For EMI request
change C7004 to N/A

0206-2 RICK
0216-1 RICK

Table 7.6 PCI Express and Other Power Rails Specification

Power Rails	Voltage	Transient Noise
PEX_DVDD / IFPx_IOVDD	1.0 V ± 3%	100mV p-p, within 20 MHz
1V8_MAIN / IFPx_PLLVDD / PEX_HVDD / PEX_PLL_HVDD / VID_PLLVDD / FBx_PLL_AVDD / SP_PLLVDD / GPC_PLLVDD / CORE_PLLVDD / 1V8_AON	1.8 V ± 3%	N/A

Note:

- The transient noise tolerance requirement applies to all shared 1V power rails.
- ASPM must remain ON when measuring PCI Express transient noise

ASUS	Project Name: UX430UN		Rev: 0.2
Title :	VGA_NV_N16S-GTR_PCIE		
Size:	Dept.: MB/B	Engineer: BE	
Date: Tuesday, August 22, 2017		Sheet 15 of 53	

0216-2 RICK
0223-3 RICK

Place Near GPU
Place Near Balls
+FBVDDQ
2.5A
待確認

Default GPU Drive Calibration for Frame Buffer Interface

FBVDDQ	1.35V or 1.50V
FBCAL_PD_VDDQ	40.2 Ohm
FBCAL_PU_GND	40.2 Ohm
FBCAL_TERM_GND	60.4 Ohm

gDDR5

0112-2 RICK

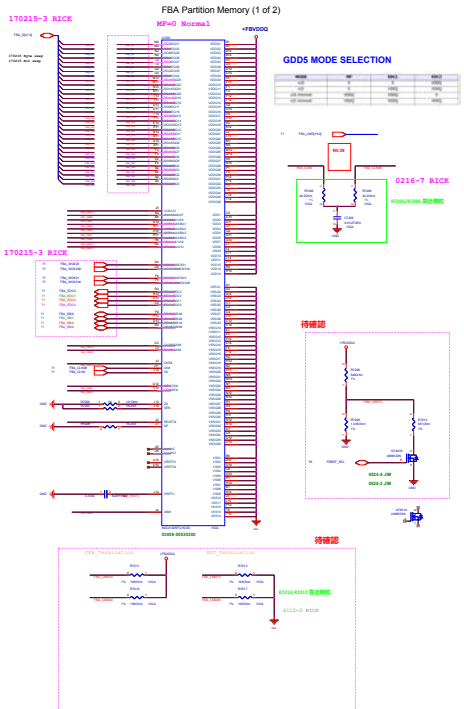
0113-1 RICK 待確認
待確認
+PEX_VVDD
200mA
Place Near Balls
Place Near GPU

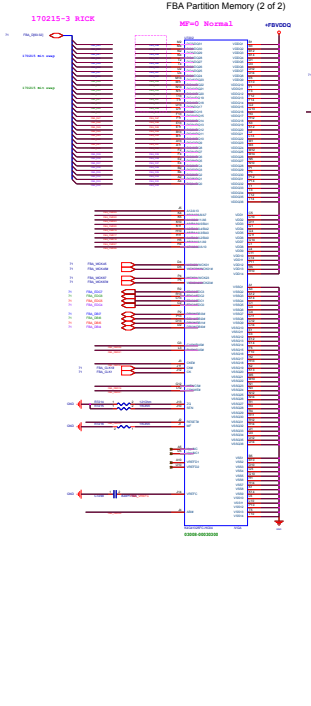
Table 9.5 GDDR5 Command Mapping (GB2C-64 package):

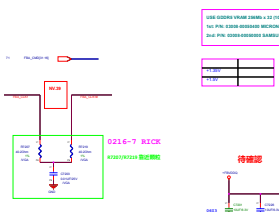
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to BG[1:0]	For DRAM(s) tied to BG[A3:32]	
FBA_CA00	FBA_CA0016	CS0
FBA_CA01	FBA_CA0017	CA40
FBA_CA02	FBA_CA0018	CA41
FBA_CA03	FBA_CA0019	CA42
FBA_CA04	FBA_CA0020	CA43
FBA_CA05	FBA_CA0021	WE*
FBA_CA06	FBA_CA0022	CAS*
FBA_CA07	FBA_CA0023	RAS*
FBA_CA08	FBA_CA0024	CS1
FBA_CA09	FBA_CA0025	BA0
FBA_CA10	FBA_CA0026	BA1
FBA_CA11	FBA_CA0027	A0_A9
FBA_CA12	FBA_CA0028	BA2
FBA_CA13	FBA_CA0029	BG*
FBA_CA14	FBA_CA0030	CA0*
FBA_CA15	FBA_CA0031	CA1*

ASUS	Project Name: UX430UN		Rev: R1.0
Title :	VGA_NV_N16S-GTR_FB-IF		
Size:	Dept.: MIUI	Engineer: EE	
Date: Tuesday, August 22, 2017	Sheet 15 of 102		

02004-00441700







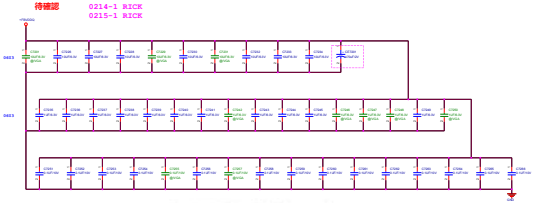


Table 9.8 GDDR5 x32 vs. x16 Quad Bus Connectivity

GPU Signal (for FBA Partition n)	x32 Mode (Non-Clamshell) GDDR5 SDRAM Device	Data Lines	x16 Mode (Clamshell) GDDR5 SDRAM Device	Data Lines
FBn_D<31:24>, FBn_D<56>	High Device (typically a non-mirrored pinout, top of PCB)	DQ[7:0]/24	Hi-CH mem Device 1 (mirrored pinout, bottom of PCB)	DQ[7:0]/24
FBn_D<55>, FBn_D<48>		DQ[15:8]/24	Hi-CH mem Device1 (non-mirrored pinout, top of PCB)	DQ[15:8]/24
FBn_D<47>, FBn_D<40>		DQ[7:0]/28	Hi-CH mem Device 0 (mirrored pinout, bottom of PCB	DQ[7:0]/28
FBn_D<39>, FBn_D<32>		INT DQ8	Hi-CH mem Device 0 (non-mirrored pinout, top of PCB	DQ7 DQ8

Table 9.8 GDDR5 x32 vs. x16 Data Bus Connectivity (Continued)

GPU Signal (for FB Partition n)	x32 Mode (Non-Clamshell) GDDR5 SDRAM Device	Data Lines	x16 Mode (Clamshell) GDDR5 SDRAM Device	Data Lines
FBn_D<31>, FBn_D<24>	Low Device (typically a non-mirrored pinout, top of PCB)	DQ[31:24]/24	Lo-CHmem Device1 (mirrored pinout, bottom of PCB)	DQ[31:24]/24
FBn_D<23>, FBn_D<16>		DQ[23:16]/24	Lo-CHmem Device1 (non-mirrored pinout, top of PCB)	DQ[23:16]/24
FBn_D<15>, FBn_D<8>		DQ[15:8]/28	Lo-CHmem Device0 (mirrored pinout, bottom of PCB)	DQ[15:8]/28
FBn_D<7>, FBn_D<0>		DQ7 DQ0	Lo-CHmem Device0 (non-mirrored pinout, top of PCB)	DQ7 DQ0

Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: GB2C-64 (preliminary)			
1.0 uF	X6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	X6S [0603]	1	Near GPU device
10 uF	X6S [0603]	1	Near GPU device
22 uF	X6S [0603]	3	

Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM/Package/Face-Mode)
Combined FBVDD-FBVDDQ Rail			Note
1.0 uF	X6S [0402]	10	For x32 DRAM, Under the DRAM FBVDD or FBVDDQ ball. For x16 DRAM in a "clamshell" PCB configuration, as close to DRAM periphery as possible. Ensure at least 1 GND via and 2 power vias for each decoupling capacitor.
1.0 uF	X6S [0402]	6 additional	For x32 DRAM: Choose x32 interface to achieve max PCB DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD-Q ball, should there existing FBVDD-Q ball. via if possible. See Figure 9.23 for an example.
10 uF	X6S [0603]	1	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	1	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 3 GND vias and 2 power vias for each capacitor.

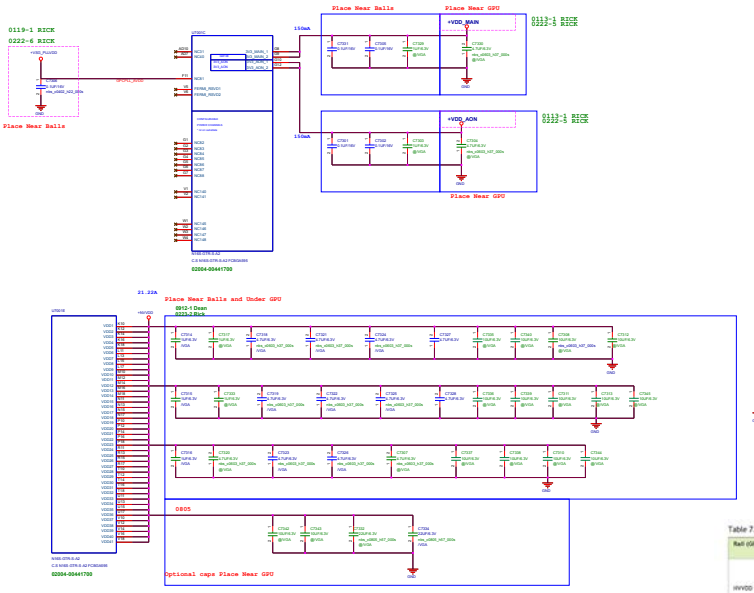
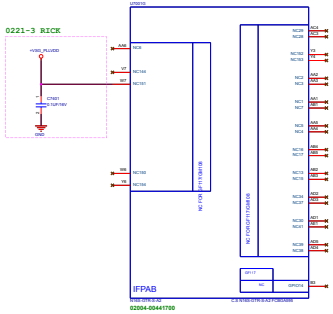


Table 7.18 GB2C-64 Package: Power Rail Filtering

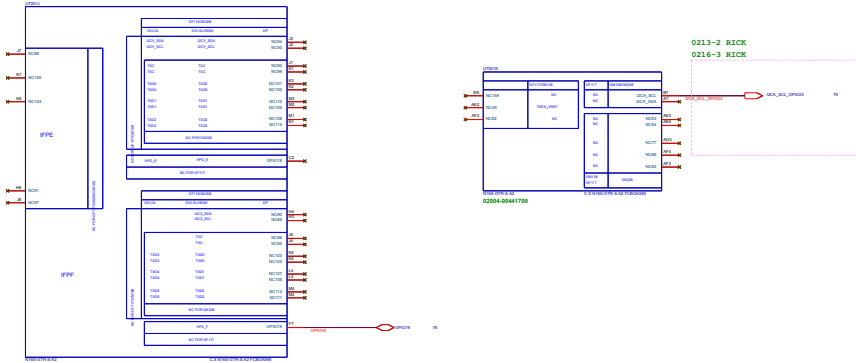
Rail (GPU Ball) Name	Balls	Voltage, Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies:	4 x 4.7uF (0805) 2 x 10uF (0805) 1 x 22uF (0805) 4.7 4.7uF (0402) 2.2 4.7uF (0603)	1 X 330uF (Poscap) Near VR: 2 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)
NVVDDS	10	Varies:	2 X 1uF (0402) 4 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)

ASUS	Project Name: UX430UN		Rev: 0.2
Title:	VGA_NV_N16S-GTR_VDD		
Size:	Dept.: AMUI	Engineer: EE	
Date: Tuesday, August 30, 2017		Sheet 73 of 100	

LVDS



CRT



ASUS	Project Name: UX430UN		Rev: R1.0
Title :	VGA_NV_N16S-GTR_DISPLAY		
Size:	Dept.: MB/B	Engineer: EE	
Date: Tuesday, August 29, 2017	Sheet 75 of 102		

Strap Pin	N17S-G1, GDDR5			N16S-GTR, GDDR5
	SAMSUNG(256Mx32) K4G80325FB-HC28 03008-00050000	MICRON(256Mx32) MT51J256M32HF-70:A 03008-00050400	HYMX(256Mx32) H5GC8H24MJR-R0C	
STRAP0	L: R7S04 = 100Kohm	H: R7S01 = 100Kohm	L: R7S04 = 100Kohm	R7S01 = 49.9Kohm, R7S04=NC
STRAP1	L: R7S05 = 100Kohm	H: R7S02 = 100Kohm	H: R7S02 = 100Kohm	Do not stuff
STRAP2	L: R7S06 = 100Kohm	L: R7S06 = 100Kohm	L: R7S06 = 100Kohm	Do not stuff
STRAP3		L: R7S10 = 100Kohm		Do not stuff
STRAP4		L: R7S11 = 100Kohm		Do not stuff
STRAP5		L: R7S12 = 100Kohm		Do not stuff
ROM_SCLK		H: R7S17 = 100Kohm		R7S18 = 4.99Kohm, R7S19=NC
ROM_SI		H: R7S16 = 100Kohm		see N16 VRAM table
ROM_SO		M: R7S13,R7S18 = 100Kohm		R7S20 = 4.99Kohm, R7S17=NC

VGA_DEVICE = 0
PCIE_CFG = 0
DEVID_CFG = 0
SMB_ALT_ADDR = 0

設定 ROM_SCLK,ROM_SI,ROM_SO PULL DOWN， 與sv確認是否可以使用 SW override， FAE：建議DISABLE

0208-2 RICK

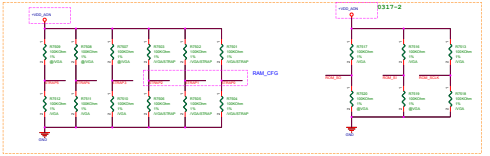
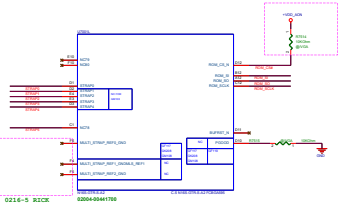


Table 5.5 SOR1 EXPOVD Strap Explanation for Down Design

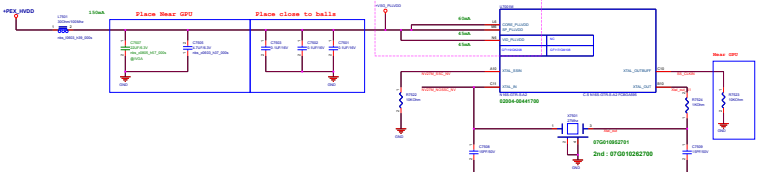
Bus Index	Resulting SOR1_EXPOVD Explanation			
	SOR1_EXPOVD[3]	SOR1_EXPOVD[2]	SOR1_EXPOVD[1]	SOR1_EXPOVD[0]
0	Strap_En	Strap_En	Strap_En	Strap_En
1	Strap_En	Strap_En	Strap_En	Strap_En
2	Strap_En	Strap_En	Strap_En	Strap_En
3	Strap_En	Strap_En	Strap_En	Strap_En
4	Strap_En	Strap_En	Strap_En	Strap_En
5	Strap_En	Strap_En	Strap_En	Strap_En
6	Strap_En	Strap_En	Strap_En	Strap_En
7	Strap_En	Strap_En	Strap_En	Strap_En

0116-2 RICK 待確認



Xtal

0222-4 RICK



GPIO, TEMP SENSOR, JTAG

Table 14.1 GPIO Descriptions for G82C-64 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	VGAS0_PWM	O	PWM Output to control dV/dt	0 to10 PWM output
GPIO1	VGAS_GCX_FB_EN	O	FB Enable for GCX 2.1	Open Source 10 kΩ pull-down

Table 14.1 GPIO Descriptions for G82C-64 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO2	GCMA_GPU_EVENT(*) VGATE*	I	GPU wake signal for GCX 2.1	10 kΩ pull-up to 1VB_AON, unless drives actively.
GPIO3	HYVDD_PWM	I/O	PWM output to control the HYVDD power supply	0 to 1VB output
GPIO4	GCMA_FB_WAKE_EN	O	GPU power sequencing for GCX 2.1	Open Drain, 10 kΩ pull-up to 1VB_AON.
GPIO5	PBA_LCD*	I	Active low Push Button	Open Drain 10 kΩ pull-up to 1VB_AON
GPIO6	HYVDD_PG(*) HYVDD_PG*	O	Power Switching (see Section 14.1.3)	10 kΩ pull-up to 1VB_AON to monitor HYVDD physic.
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VSD_CTL	O	Memory voltage control	Pull up/pull down to set the FBVDDQ power on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1VB_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD_EN	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LIMIT(*)	I	AC power detect or power supply overdrive input	10K kΩ pull-up to 1VB_AON
GPIO13	LCD_PWM_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_PEX(*)	I	Hot Plug Detect for PEX	Inverted input. See Figure 14.5
GPIO15	HPD_PEX*	I	Hot Plug Detect for PEX	Inverted input. See Figure 14.5
GPIO16	SCAN_CTL_PEX_ROT_MOD*	I	System side PCIe reset monitor	10 kΩ pull-up to 1VB_AON unless actively driven
GPIO17	UNUSED	I/O		
GPIO18	UNUSED	I/O		

Table 14.1 GPIO Descriptions for G82C-64 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO19	SI Scan	I	SI Scan – 0 Open	100 kΩ pull-down
GPIO20	eDx_HB_CTL	O	Trans Buffer EB select	Open Drain, 10 kΩ pull-down(Default for N16S/G), driven as output of both sides
GPIO21	UNUSED	I/O		
GPIO22	SCAN_CTL_PEX_ROT_MOD*	I	SCAN clock PCIe reset control	100 kΩ pull-up to 1VB_AON

170116-3 RICK

0526-2 JTM

0221-2 RICK
0317_3 RICK

0221-1 RICK

170116-3 RICK
0207-2 RICK
0209-1 RICK
0216-3 RICK

02004-00441700

GPIO N17

170207-2 RICK
0213-2 RICK
0216-3 RICK

FOR N17

Q7705A 調整到PAGE.77

170123-3 RICK remove U7601 R7616 for no demand(N16_0062.0).

170216-3 RICK modify N16/N17 colay ckt. (GPIO_PART)
to N17 ckt. only.

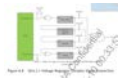
170206-1 RICK
170314-4 RICK
170323-1 RICK
170327-2 RICK
170328-2 RICK

un-used:

GPIO-3
GPIO-5
GPIO-7
GPIO-10
GPIO-11
GPIO-13
GPIO-14
GPIO-15
GPIO-17
GPIO-18
GPIO-19
GPIO-20
GPIO-21
GPIO-22

ASUS	Project Name: UX430UN			Rev: R0.0
Title :	VGA_NV_N16S-GTR_GPIO			
Size:	Custom	Dept.: ASUS	Engineer: EE	
Date:	Tuesday, August 22, 2017	Sheet 76 of 102		

dGPU Power Sequence



170112-RICK
0302-0 Dean

Reserve for EMI

Trip point 2.5V/1.25V

+VDD_AON

0330-7

+FBVDDQ Enable

0210-2 Rick

For GC6 2.1

0719-2 Rick
0226-1 Rick

0226-2 Rick

0421-7 JSM

Power GD

0302-7 Dean
0226-1 Rick
0226-7 Rick
0410-7 JSM

PWR那邊的pull-up是可不上件
R7740, R7703是可改short land

+VDD_MAIN / NVVDD Enable

0410-7 JSM

0113-2 Rick
0719-2 Rick
0719-7 Rick
0213-2 Rick

0424-4 JSM

N17 power source :

0216-4 Rick

+1.8V3
+VDD_MAIN
+3V3
+PEX_NVDD

+PEX_VDD

0328-7 Dean
0719-2 Rick
0719-7 Rick
0213-2 Rick
0220-1 Rick

0424-1 JSM
0424-6 JSM

0424-2 JSM
0320-1 JSM

NVVDD POWER GOOD LOOPBACK

ref.G753VI

0302-1 rick
0303-1 rick

PCB Layout Placement

ASUS	Project Name: UX430UN		Rev: 0.1
Title :	VGA_NV_N16S-GTR_POWER		
Size:	Project:	Engineer:	EE
Date: Tuesday, August 22, 2017		Sheet 11 of 100	

dGPU Protection

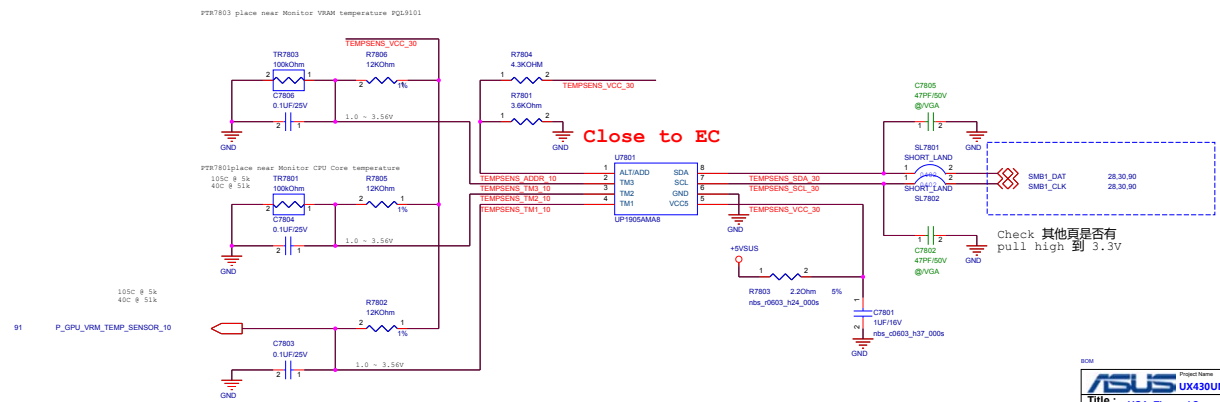
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7804	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7801	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threahold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

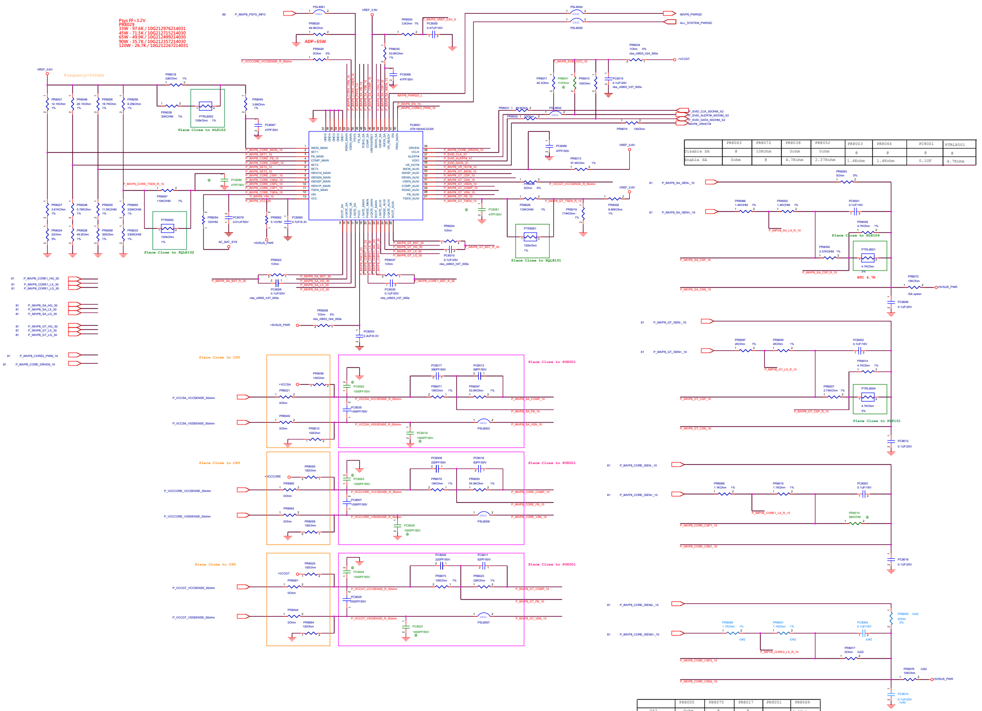
ALERT# pull low if sensed temp.
is higher than setting



BOM

ASUS	Project Name: UX430UN	Rev: R1.0
Title : VGA_Thermal Sensor		
Size: B	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 78 of 102	

Skylake IMVP8 Power [For CPU]



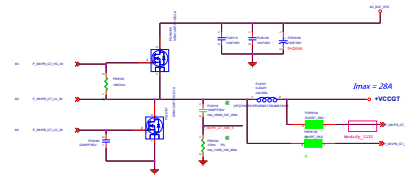
	PR8063	PR8072	PR8038	PR8052	PR8003	PR8066	PC8001	PTRL8001
Disable SA	@	10Kohm	0ohm	0ohm	@	@	@	@
Enable SA	0ohm	@	4.7Kohm	2.37Kohm	1.4Kohm	1.4Kohm	0.1UF	4.7Kohm

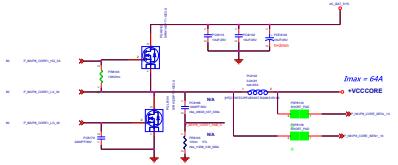
	PR8005	PR8075	PR8017	PR8051	PR8069
U42	0ohm	@	@	1.1Kohm	1.1Kohm
U22	@	10Kohm	0ohm	@	@

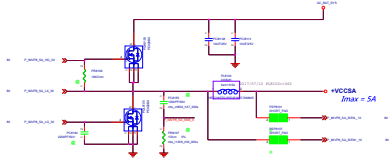
<Variant Name>

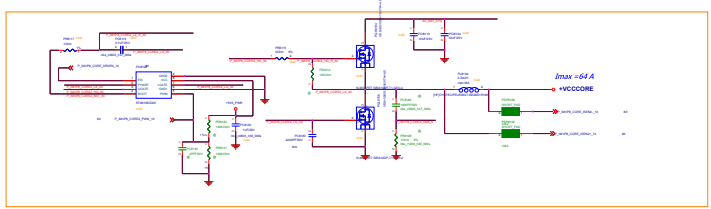
ASUS	Project Name: UX303UB	Rev: 1.0
Title : Skylake IMVP8		
Size: Custom	Dept.: Power team	Engineer: Rock
Date: Tuesday, August 22, 2017	Sheet 80 of 102	

Kaby Lake-U IMVP8 Power (2) [For CPU]

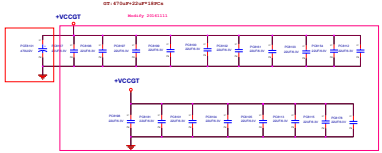


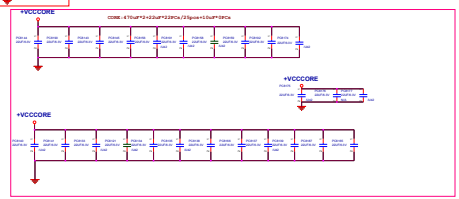






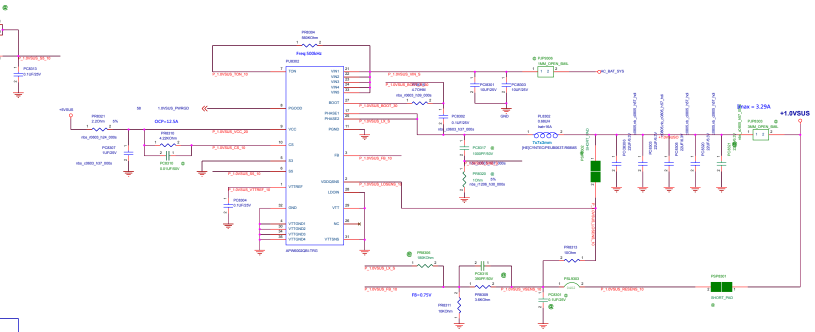
Page81 BOM rule
U22=> N/A全上
U42=> N/A + /U42 全上
# => U22與U42皆不上





Size	Project Name				Rev
	ASUS	UX430UN			1.0
Date	Title : PM_KabyLAKE-U(2/2)				
2014-11-18	Sheet	of	Engineer:	Power	

+1.0VSUS (APW6001QBI-TRG)

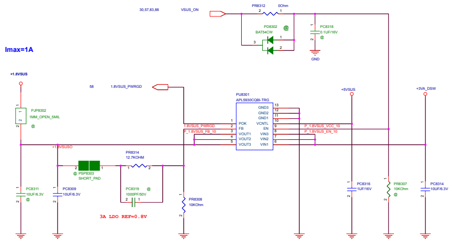


PR8315	Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

PT830* 請放置 PU8302旁;並請放置Trace 上!

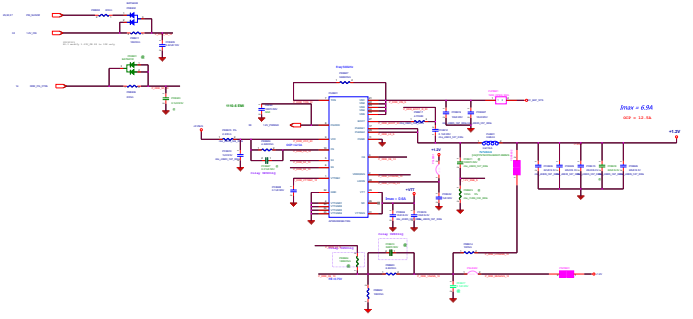
P_1.0VSUS_LX_S — PT8301 NB_TPC20T

+1.8VSUS [For PCH]



Project Name: UX430UN		Rev: R1.0
Title: PW_+1.0VSUS / +1.8VSUS		
Size: Custom	Dept.: ASUS	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 83 of 102	

+1.2V / +VTT / +2.5V[For Memory]

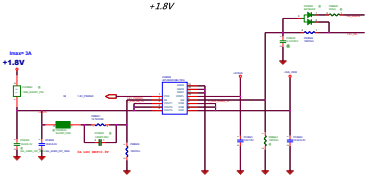


S5 And S3 Truth Table

State	Pin12(G)	Pin4(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF	OFF	OFF
			(Discharge)	(Discharge)	(Discharge)

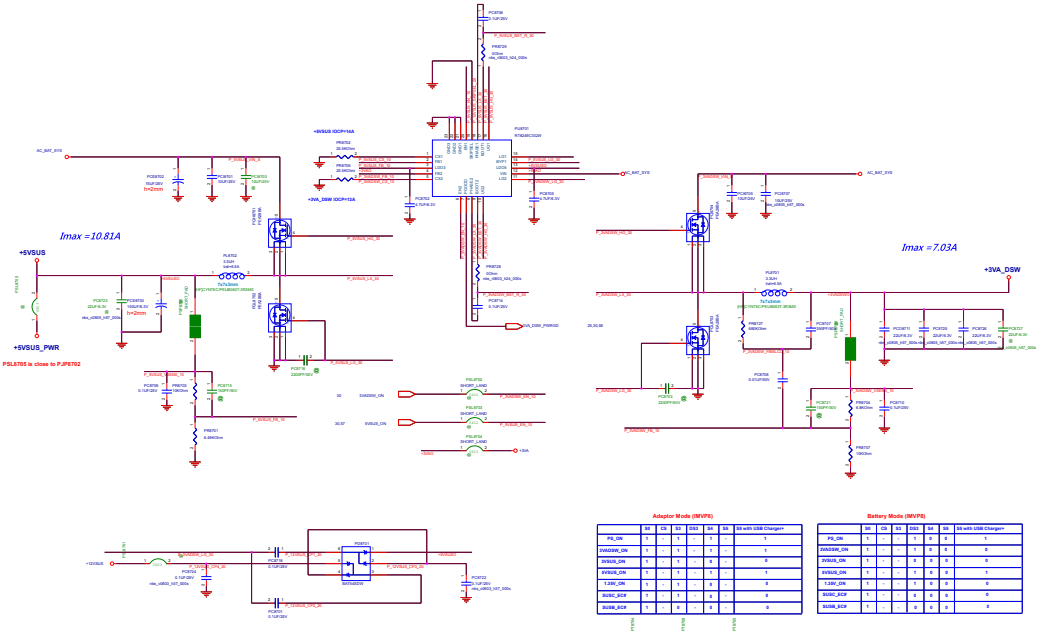
Inductor	MPN(Delta_Side)
1.2V	1.2uH
1.8V	1.2uH
0.9V	1.2uH
0.45V	1.2uH
0.9V	1.2uH

+1.8V



ASUSTeK COMPUTER INC.	Size	Rev
Title: PM_+1.2V+VTT+2.5V		
Engineer: Ryuan		

+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (5V/PS)

	S0	S3	S4/S5	DSO	S4	S5	S5 with USB Charger=
PS_ON	1	1	-	-	1	-	1
3VA3SW_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	0	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_SCF	1	-	1	-	0	-	0
SUSB_SCF	1	-	0	-	0	-	0

Battery Mode (5V/PS)

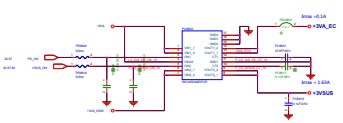
	S0	S3	S4/S5	DSO	S4	S5	S5 with USB Charger=
PS_ON	1	-	-	1	0	0	1
3VA3SW_ON	1	-	-	1	0	0	0
5VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_SCF	1	-	-	0	0	0	0
SUSB_SCF	1	-	-	0	0	0	0

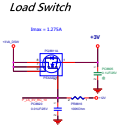
插 check 整台線圈 +12VSUS total 短期狀態電阻不得小於10kOhm

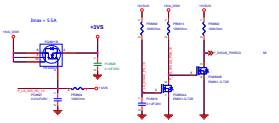
BOM

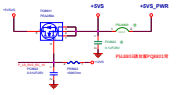
ASUS	Project Name: UX430UN	Rev: 0.2
Title : PWR_+3VA_DSW/+5VSUS		
Size: Custom	Dept.: MB/B	Engineer: EE
Date: Tuesday, August 22, 2017	Sheet 67 of 102	

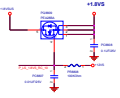
Load Switch

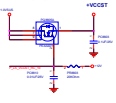


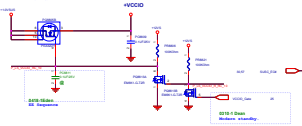


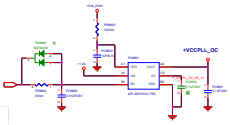


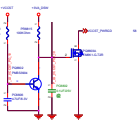


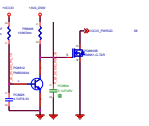


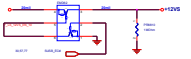












Size

ASUS	Compal Electronics		Rev
	LV41SUN		1.0
Title : PW_LOAD_SWITCH			
Size	Project : LV41	Engineer:	EE
Date: Tuesday, August 06, 2013		Sheet 50 of 59	

Main Board

PR89901	<=45W	<=120W	>=120W
	20m	10m	5m
	150475-0004N003	150475-0004N003	150475N0004S1A1

AD : 17.8V

AC_BAT_SYS

BAT

I limit : Charge 6A
DisCharge 14.5A

Adaptor select
total power = 90% ADP

Adaptor select		N Series	
PR8921		10m	5m
968936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
83.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle

dGPU_PD# ---> GPIO12(EE page 75 or 78)

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

PD9901 請放置 PU8900在旁邊靠近pin 27

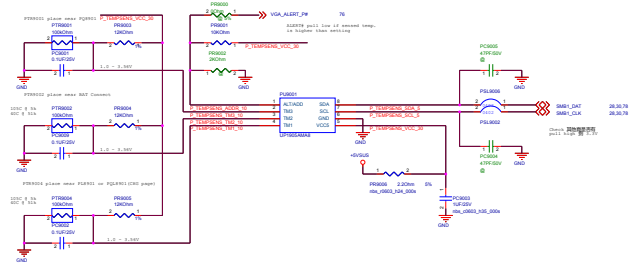
ASUS	Project Name: UX433UN	Rev: 1.0
Title: PM_CHARGER		
Size: Custom	Engineer: EE	
Date: Monday, January 08, 2018	Sheet of	

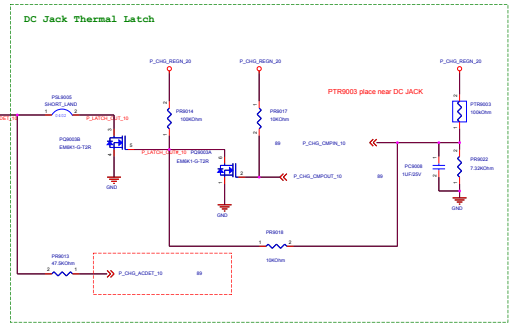
Address Selection Table

Address	0x78	0x7C	0x7A	0x7E	0x76	0x74	0x72	0x70
R9002	10k	1.5k	2k	3.4k	4.9k	6.5k	9.1k	6k
R9002	Open	8.2k	6.2k	6.8k	8.7k	9.4k	2.7k	2k

Register Address

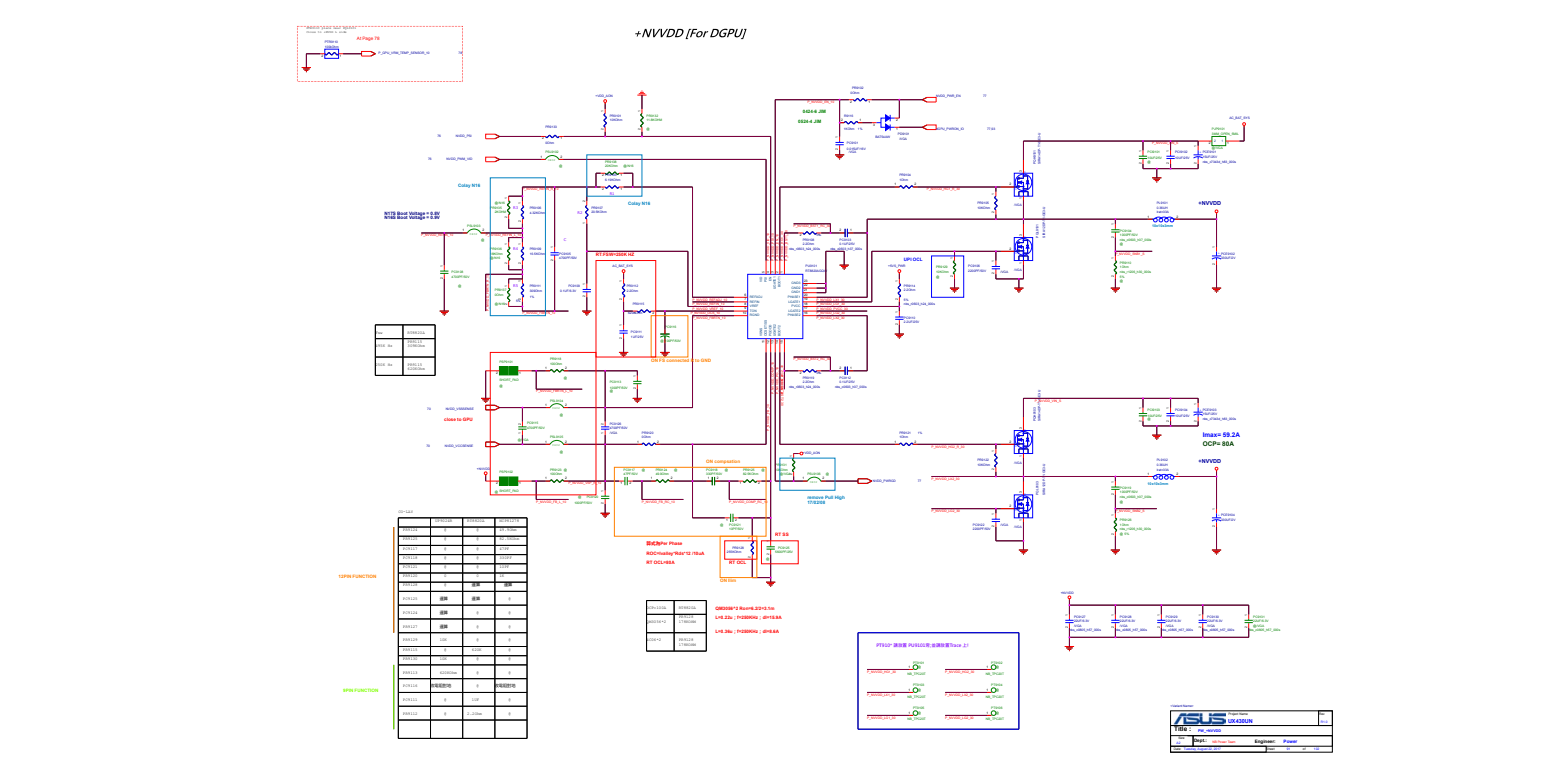
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 6 = 0 bit 5 = 0 bit 4 = 0 When ALERT# assert

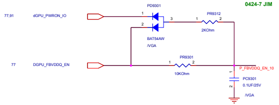




<Variant Name>

Project Name: UX430UN			Rev: R1.0
Title : PW_PROTECTION			
Size: A3	Dept.: ASUS	Engineer: EE	
Date: Tuesday, August 22, 2017	Sheet 90 of 102		

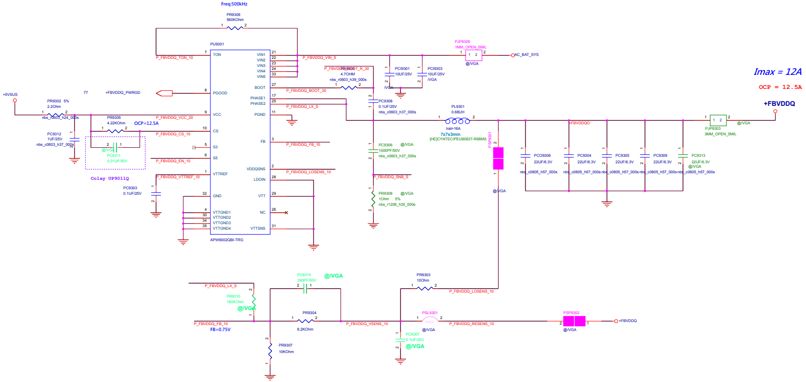

+NVVDD [For DGPU]
At Page 76
PJ_GPU_VRM_TEMP_SENSOR_10
5424-4 JIM
5524-4 JIM
Colay NT6
NT6 Boot Voltage = 0.8V
NT6S Boot Voltage = 0.8V
RT FSW=350K HZ
ON compensation
Remove Pull High 17.02.09
RT SS
RT OCL
Iimax= 59.2A
OCP= 80A
+NVVDD
UPI OCL
close to iGPU
Per Phase
ROCP=Iload*Rds*12 =70uA
RT OCL=60A
GM3038*2 Rcs=6.22+2.1m
L=0.22u ; f=320KHz ; dI=10.6A
L=0.36u ; f=320KHz ; dI=8.6A
12PIN FUNCTION
9PIN FUNCTION
PT512* 請測量 PJ512U1用 做測量Trace 上!
ASUS
UX430UN
Title : PWR_NVVDD
Engineer: Power



S3 And S5 Truth Table

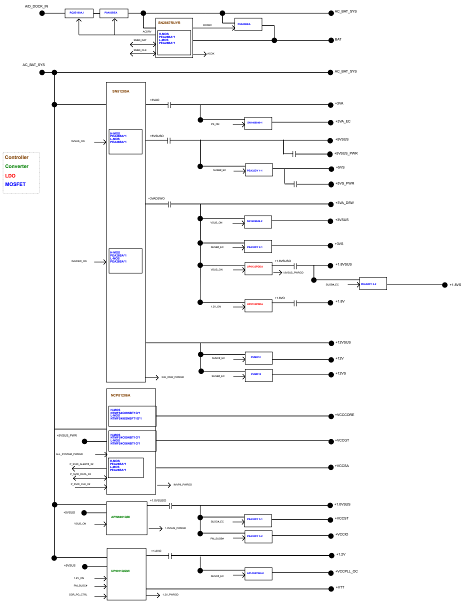
State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+FBVDDQ [For VRAM]

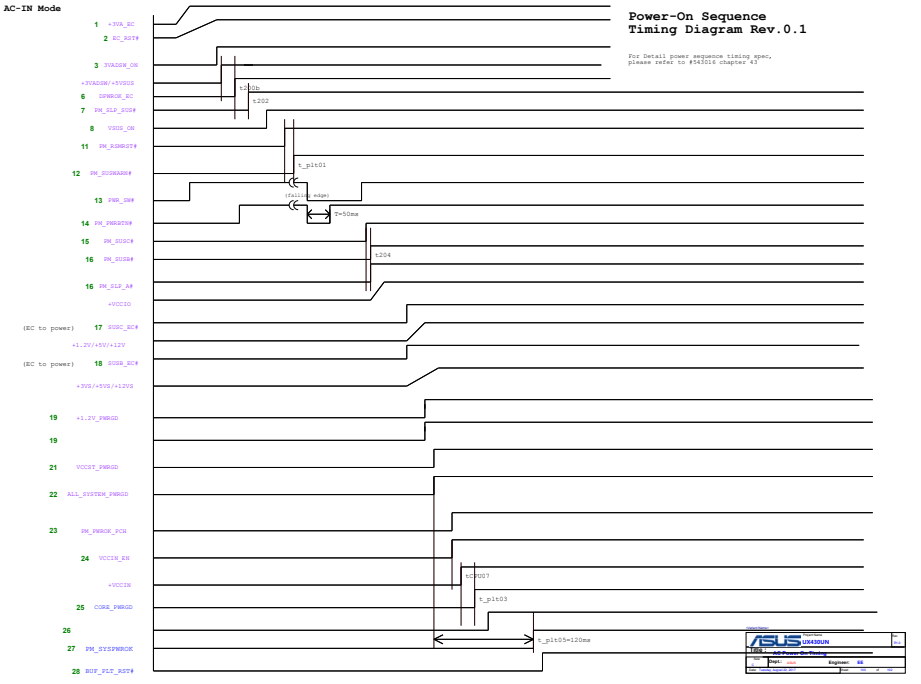


<Variant Name>

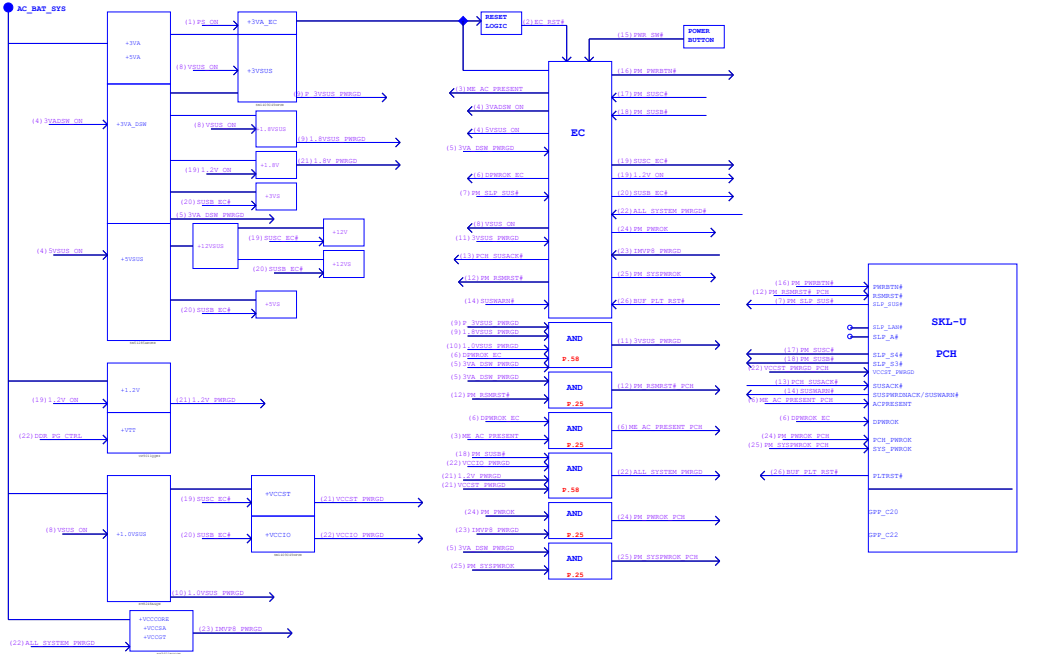
ASUS	Project Name: UX430UN	Rev: R1.0
Title : PW_+FBVDDQ		
Size: Custom	Dept.: ASUS	Engineer:
Date: Tuesday, August 22, 2017	Sheet 93 of 102	



ASUS
Project Name: UX430UN
Title : PW_FLOWCHART
Dept.: ASUS
Engineer: EE


AC-IN Mode
Power-On Sequence
Timing Diagram Rev.0.1
For Detail power sequence timing spec, please refer to #543016 chapter 43
1 +3VA_EC
2 EC_RST#
3 3VADSW_ON
+3VADSW/+5VSUS
6 DPWROK_EC
7 PM_SLP_SUS#
8 VSUS_ON
11 PM_RSMRST#
12 PM_SUSWARN#
13 PWR_SW#
14 PM_PWRBTN#
15 PM_SUSC#
16 PM_SUSS#
16 PM_SLP_A#
+VCCIO
(EC to power) 17 SUSC_EC#
+1.2V/+5V/+12V
(EC to power) 18 SUSB_EC#
+3VS/+5VS/+12VS
19 +1.2V_PWRGD
19
21 VCCST_PWRGD
22 ALL_SYSTEM_PWRGD
23 PM_PWROK_PCH
24 VCCIN_EN
+VCCIN
25 CORE_PWRGD
26
27 PM_SYSPWROK
28 BUF_PLT_RST#
t210b
t202
t_plt01
(Falling edge)
T=50ms
t204
t_plt03
t_plt05=120ms
ASUS
UX430UN
Power On Timing
Engineer:

Power On Sequence Diagram Rev.2.0



Project Name	UX430UN
Title :	POWER-ON SEQUENCE
Engineer:	SS