DELL/COMPAL

MODEL NAME : FDV50/FDV51

PCB NO : LA-J282P

BOM P/N :

GPIO MAP: X11_CMLH_GPIO map Rev0.4_20190927

PWR Circuit : BHMLK_CMLH_15DIS_A00_PWR_20200302B

Brook Hollow MLK 15 DSC (TBT)

Comet Lake H

2020-03-02

REV : 1.0 (A00)

X76@ :
SATAPERIX76@ :
SATAPARAX76@ :
2GSAMX76@
2GMICRX76@
2GHYNX76@
4GMICRX76@
4GHYNX76@

@ : Nopop Component
N17@ : N17S-G1-B Component
N19@ : N19M-Q3 GPU Component
EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESD Component
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
VPRO@ : VPRO support
NVPRO@ : non VPRO support
JUMP@ : Jump solder and short
@JUMP@ : Jump no solder
XDP@ : XDP Component
@XDP@ : XDP Nopop Component
CONN@ : Connector Component
WWAN@ : WWAN Component
WWANRF@ : WWAN RF Component

ESPI@ : eSPI interface
DS3@ : Deep sleep support
NDS3@ : non Deep sleep support
@NDS3@ : non Deep sleep Nopop Component
RTD3@ : RTD3 support
NRTD3@ : non RTD3 support
5107ES@ :
5107NES@ :
SATAPERI@ : Pericom SATA repeater support
SATAPARA@ : Parade SATA repeater support
2GSAM@
2GMICR@
2GHYN@
4GMICR@
4GHYN@

MB PCB

Part Number	Description
DAZ2VX00201	PCB FDV50 LA-J282P LS-G901P TRIPOD A31 !

Layout Dell logo

REV: X00
PWB:

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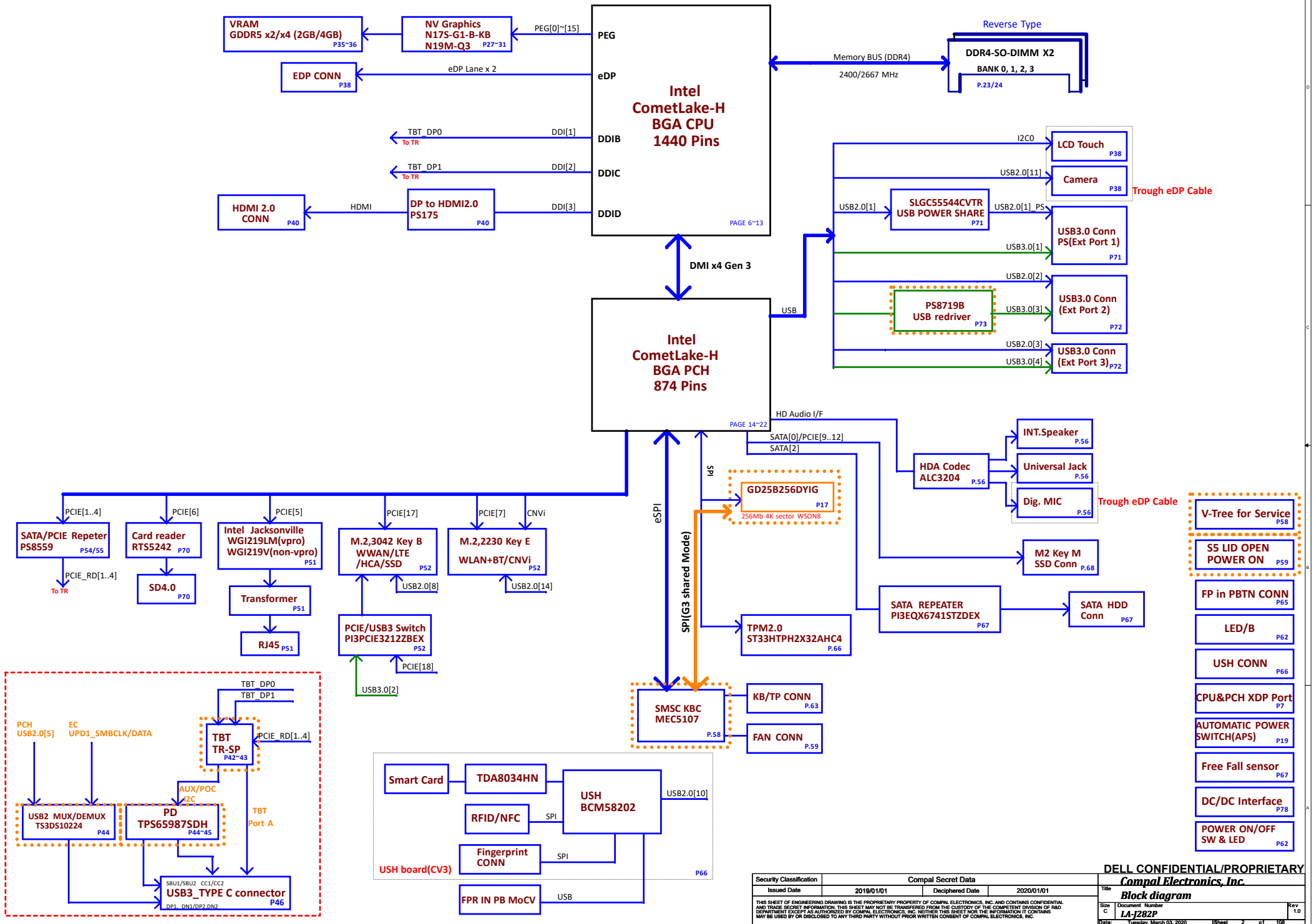
Title: Cover Sheet

Size: A | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 1 of 108

Brook Hollow MLK 15 DSC TBT Block Diagram



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Title: Block diagram

Size	Document Number	Rev
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane \ State			
	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB2-->LEFT
USB3.0-4				JUSB3-->RIGHT
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		Titan Ridge - SP
USB3.0-8		PCIE-2		
USB3.0-9		PCIE-3		
USB3.0-10		PCIE-4		
		PCIE-5		LOM
		PCIE-6		Card Reader
		PCIE-7		JNGFF1-->M.2 2230(WLAN)
		PCIE-8		NA
		PCIE-9		M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10		
		PCIE-11	SATA-0A	
		PCIE-12	SATA-1A	
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	
		PCIE-19	SATA-6	NA
		PCIE-20	SATA-7	NA

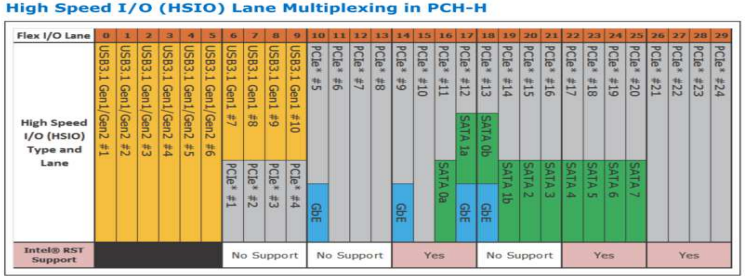
USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2 ->LEFT
3	JUSB3-->RIGHT
4	FP IN PB
5	TI PD
6	test point
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	NA
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA
13	NA
14	JNGFF1--> M.2 2230(CNVi_BT)

USH	H	BIO

VIDEO	DESTINATION
eDP	LCD
DDI-B	Titan Ridge - SP (Port 0)
DDI-C	Titan Ridge - SP (Port 1)
DDI-D	PS175 --> JHDMI1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		3.7	SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1086 or 1080	2.70
2	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Core	3mil	3.00
3	Sig1		Copper foil	0.5oz	0.65
		3.8	Prepreg	2116	4.20
4	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Core	3mil	3.00
5	Sig2		Copper foil	0.5oz	0.65
		3.8	Prepreg	2116	4.20
6	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Core	3mil	3.00
7	Sig3		Copper foil	0.5oz	0.65
		3.8	Prepreg	2116	4.20
8	Sig4		Copper foil	0.5oz	0.65
		3.7	Core	3mil	3.00
9	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Prepreg	2116	4.20
10	Sig5		Copper foil	0.5oz	0.65
		3.7	Core	3mil	3.00
11	GND/PWR		Copper foil	0.5oz	0.65
		3.7	Prepreg	1086 or 1080	2.70
12	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
		3.7	SolderMask		0.50
Overall Thickness (1.7mm ± 10%)					47.90000
					1.21666

Figure 110. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



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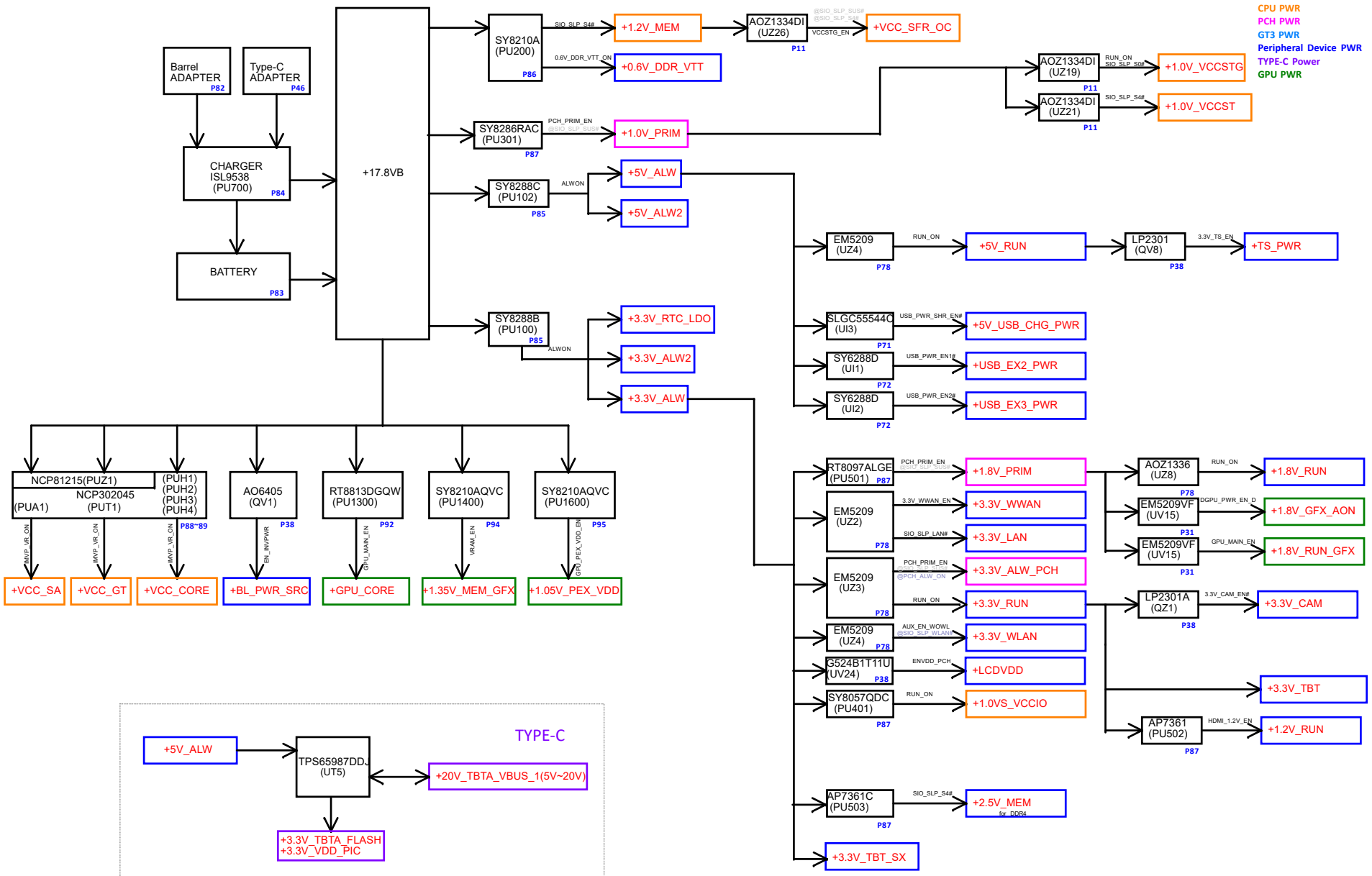
Title: Port Assignment			
Size: A	Document Number: LA-J282P		Rev: 1.0
Date: Tuesday, March 03, 2020	Sheet 3 of 108		



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Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: Power Rails

Size	Document Number	Rev
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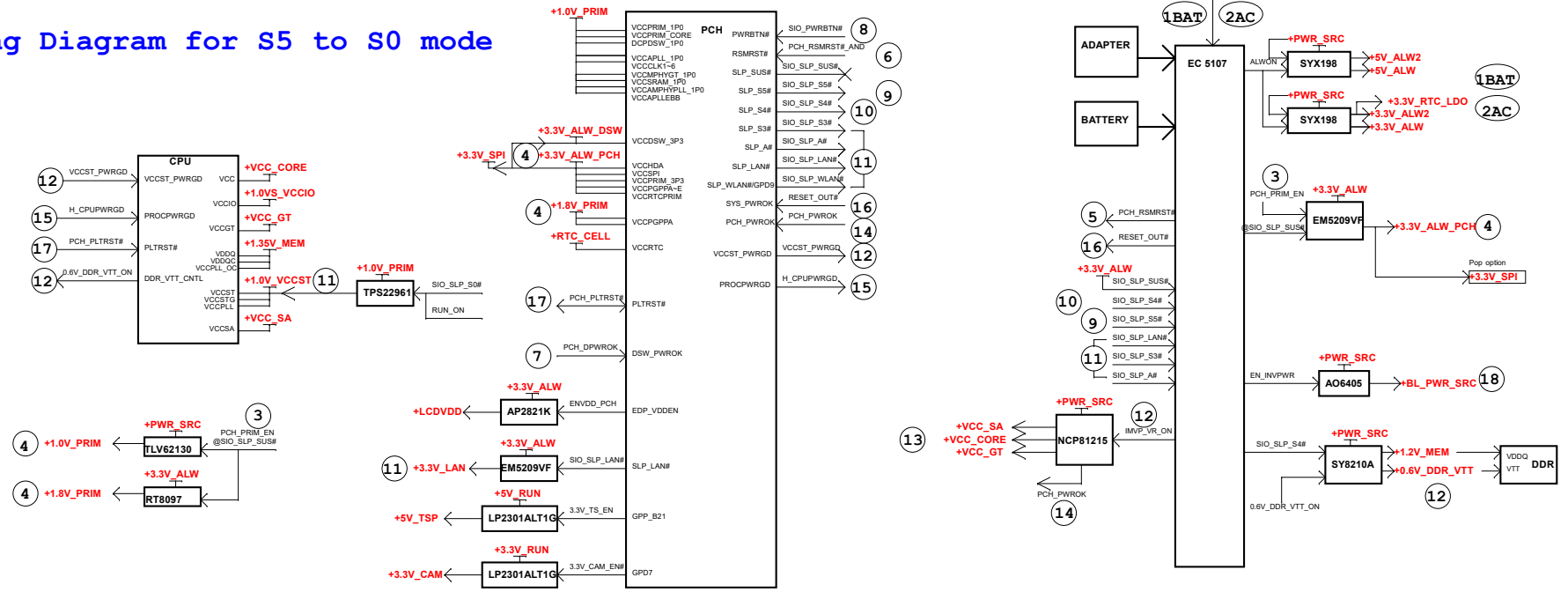
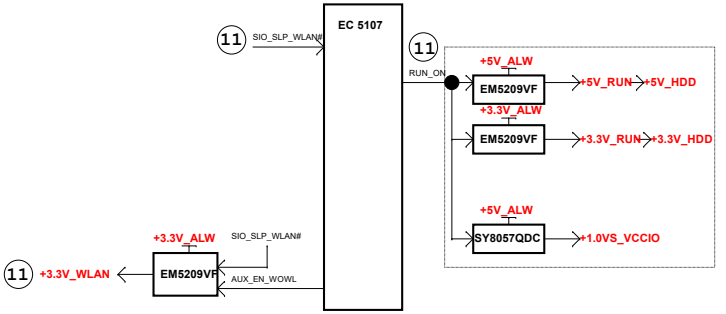
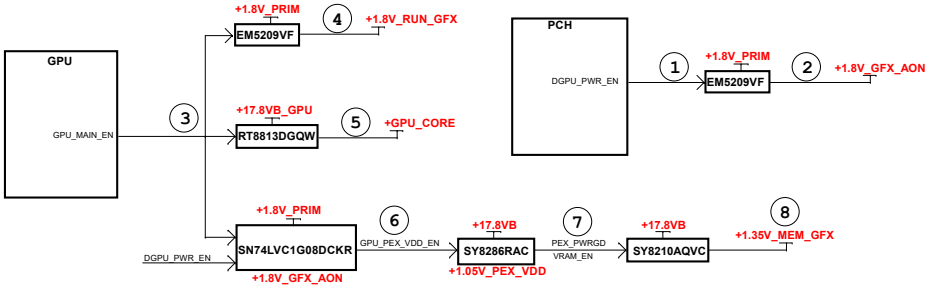
Timing Diagram for S5 to S0 mode





GPU power-on Timing Diagram during win10



Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.			
Title	Power Sequence		
Size	Document Number		Rev
Custom	LA-J282P		1.0
Date:	Tuesday, March 03, 2020	Sheet 5 of 108	

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UC1C

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PEG_CRX_GTX_P14	E24	PEG_RXP_1	PEG_TXP_1	B24	PEG_CTX_GRX_P14	CC36 1	2 0.22U_0402_16V7K	PEG_CTX_C_GRX_P14
PEG_CRX_GTX_N14	F24	PEG_RXN_1	PEG_TXN_1	C24	PEG_CTX_GRX_N14	CC37 1	2 0.22U_0402_16V7K	PEG_CTX_C_GRX_N14
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CML-H_BGA1440
3 OF 13

+1.0VS_VCCIO
RC2 1 2 PEG_COMP 24.9_0402_1%

Trace width=5 mils
,Spacing=15mil
Max length= 600 mils.

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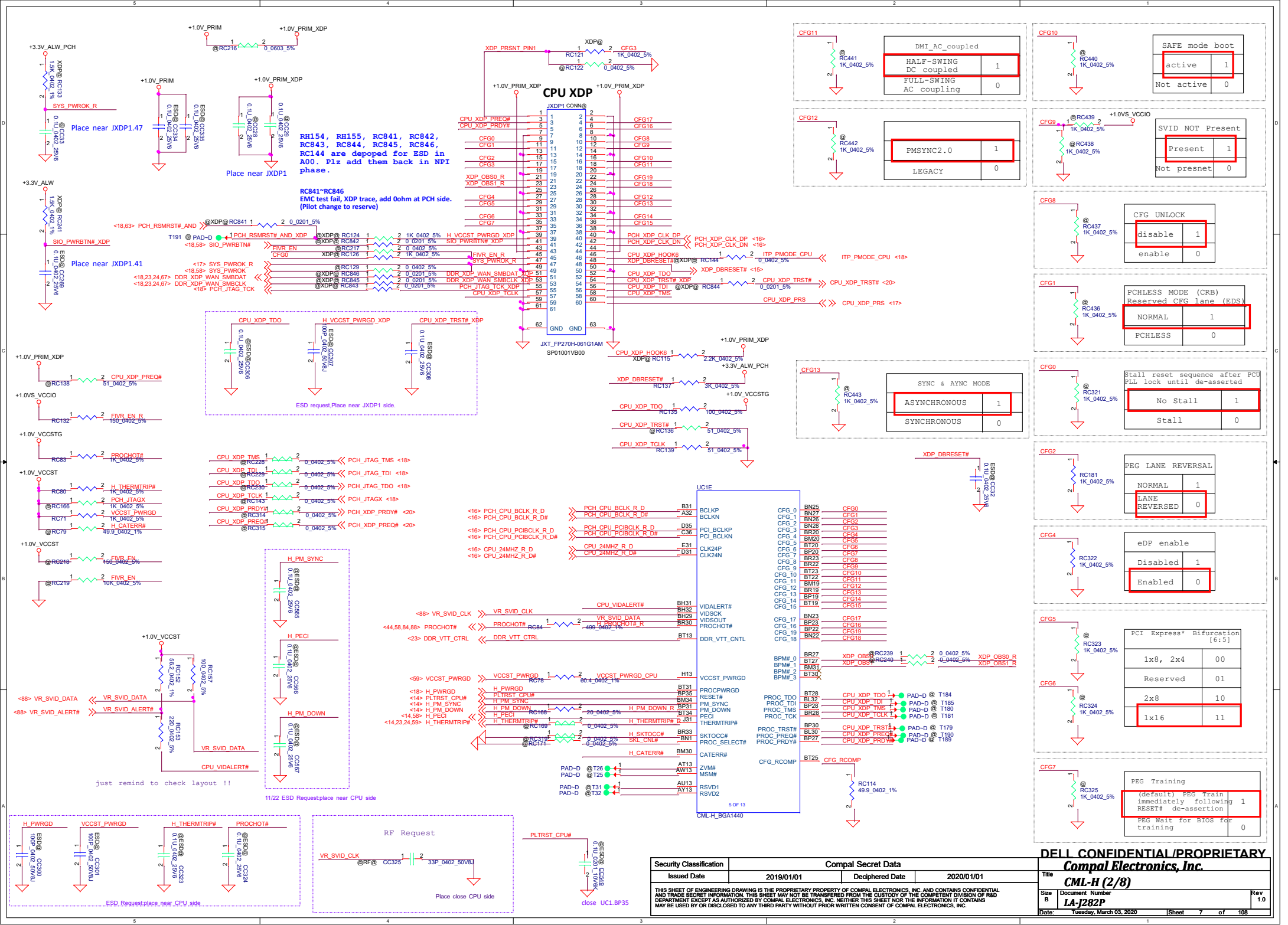

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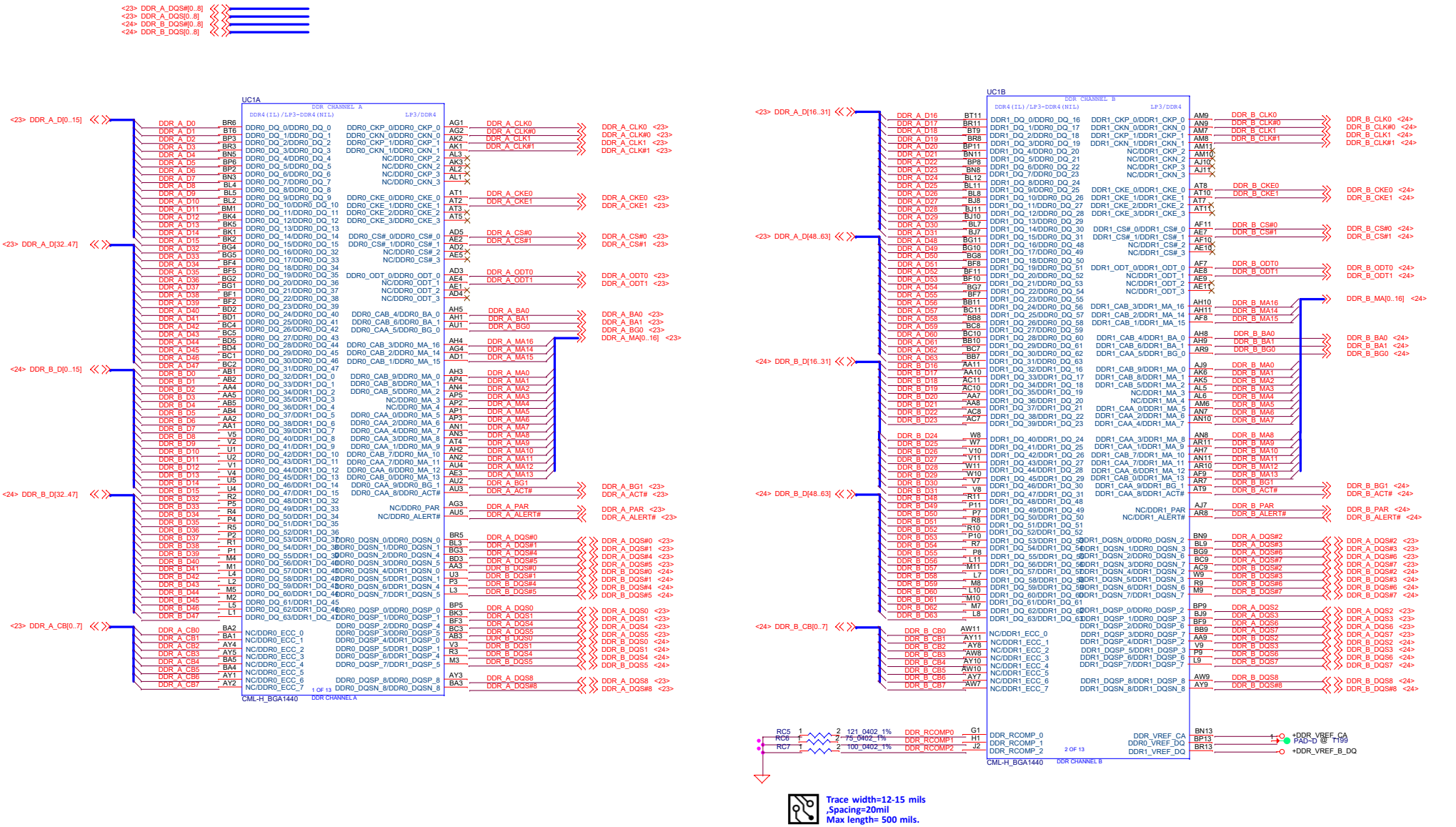

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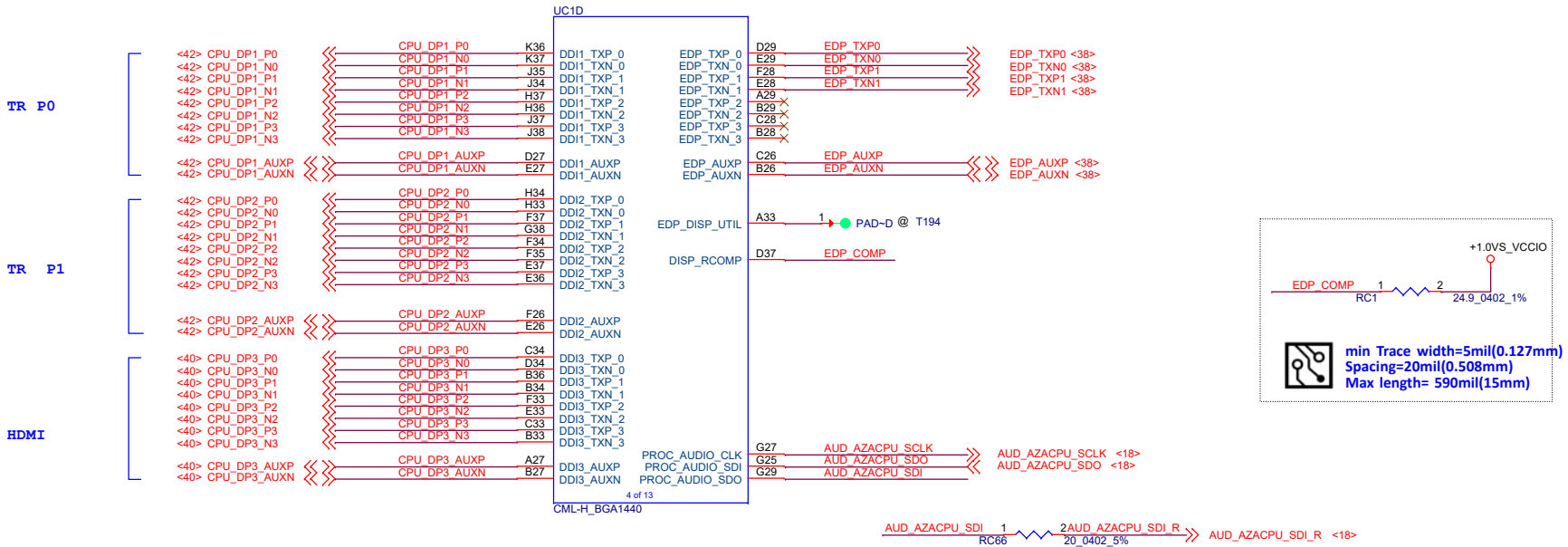
Size: B	Document Number: LA-J282P	Rev: 1.0
Date: Tuesday, March 03, 2020	Sheet 8 of 108	



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Size	Document Number	Rev
A	LA-J282P	1.0

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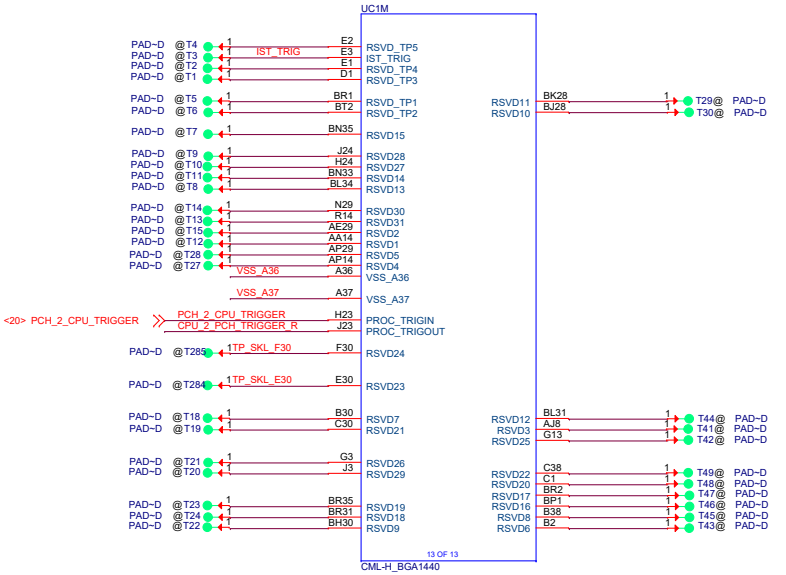

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

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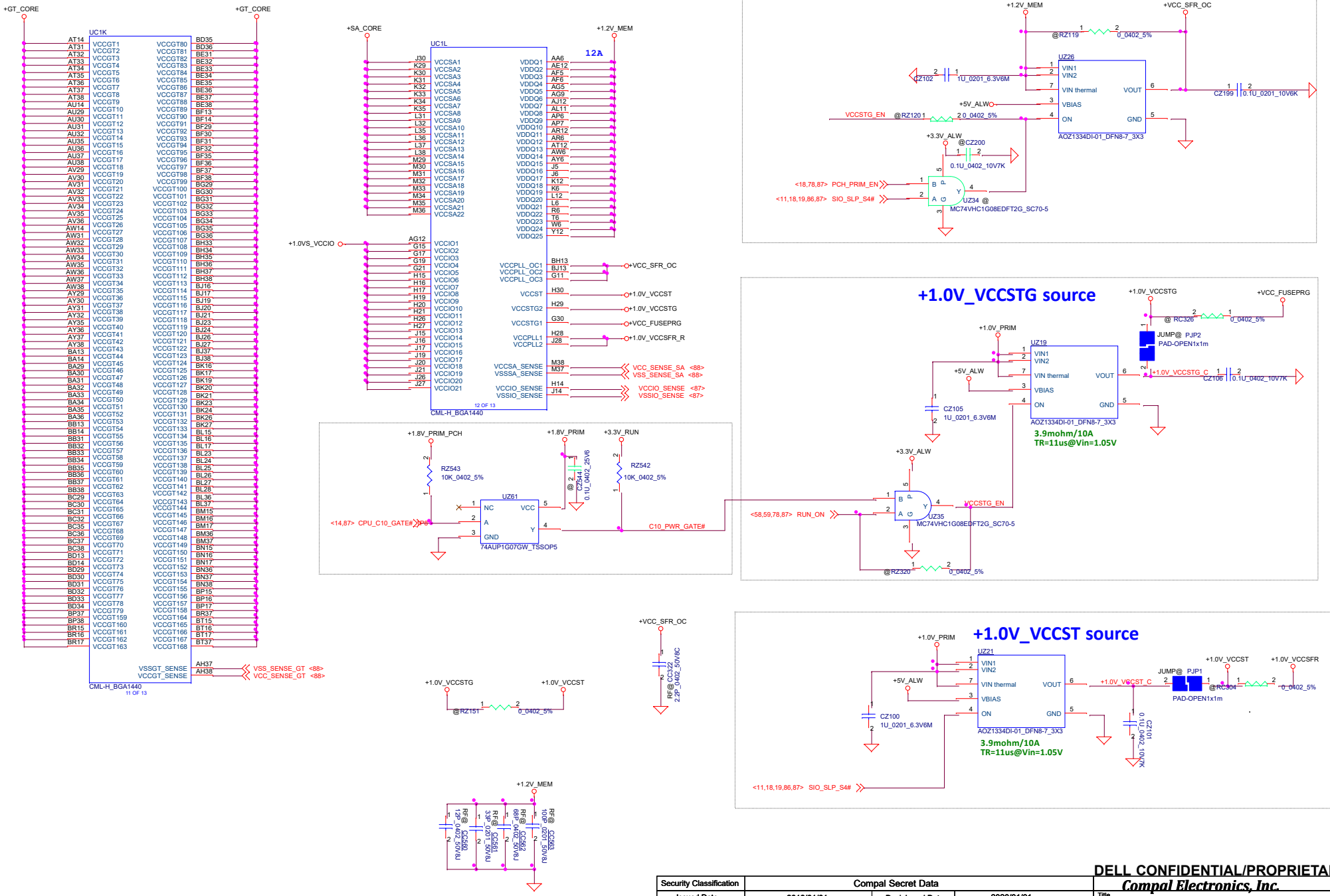
Title	*Compal Electronics, Inc.* / *CML-H (5/8)*
Size	B
Document Number	*LA-J282P*
Rev	1.0
Date:	Tuesday, March 03, 2020
Sheet	10 of 108



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Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Compal Electronics, Inc.

Title: CML-H (6/8)

Size	Document Number	Rev
B	LA-J282P	1.0

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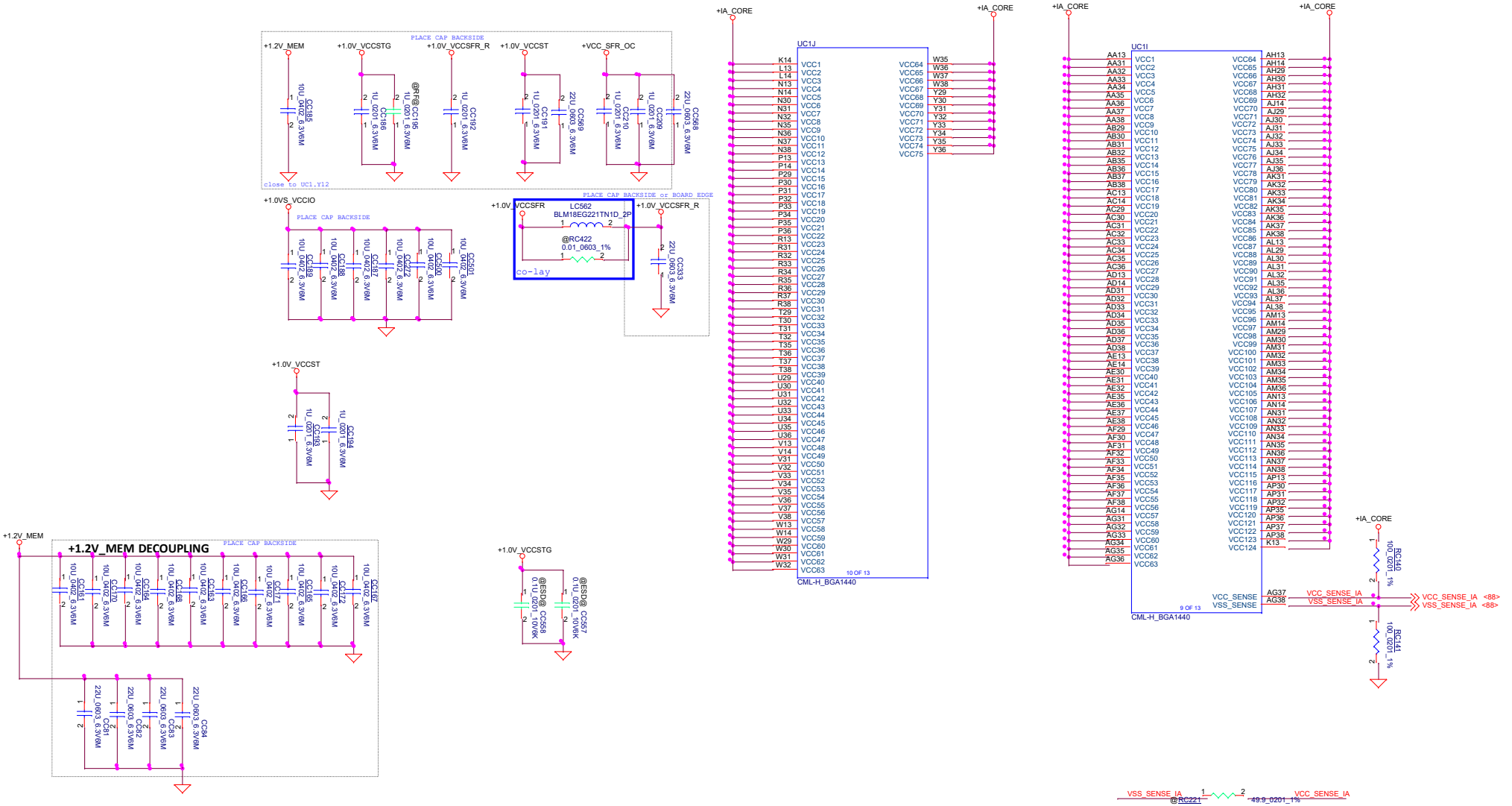
CPU Decoupling CAP Follow 611586_CML_H_PDG_Rev0p7
page. 592 ,593 Table 326. CML H 8+2 Processor Decoupling Requirements



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Title	CML-H (7/8)	
Size	Document Number	Rev
B	LA-J282P	1.0
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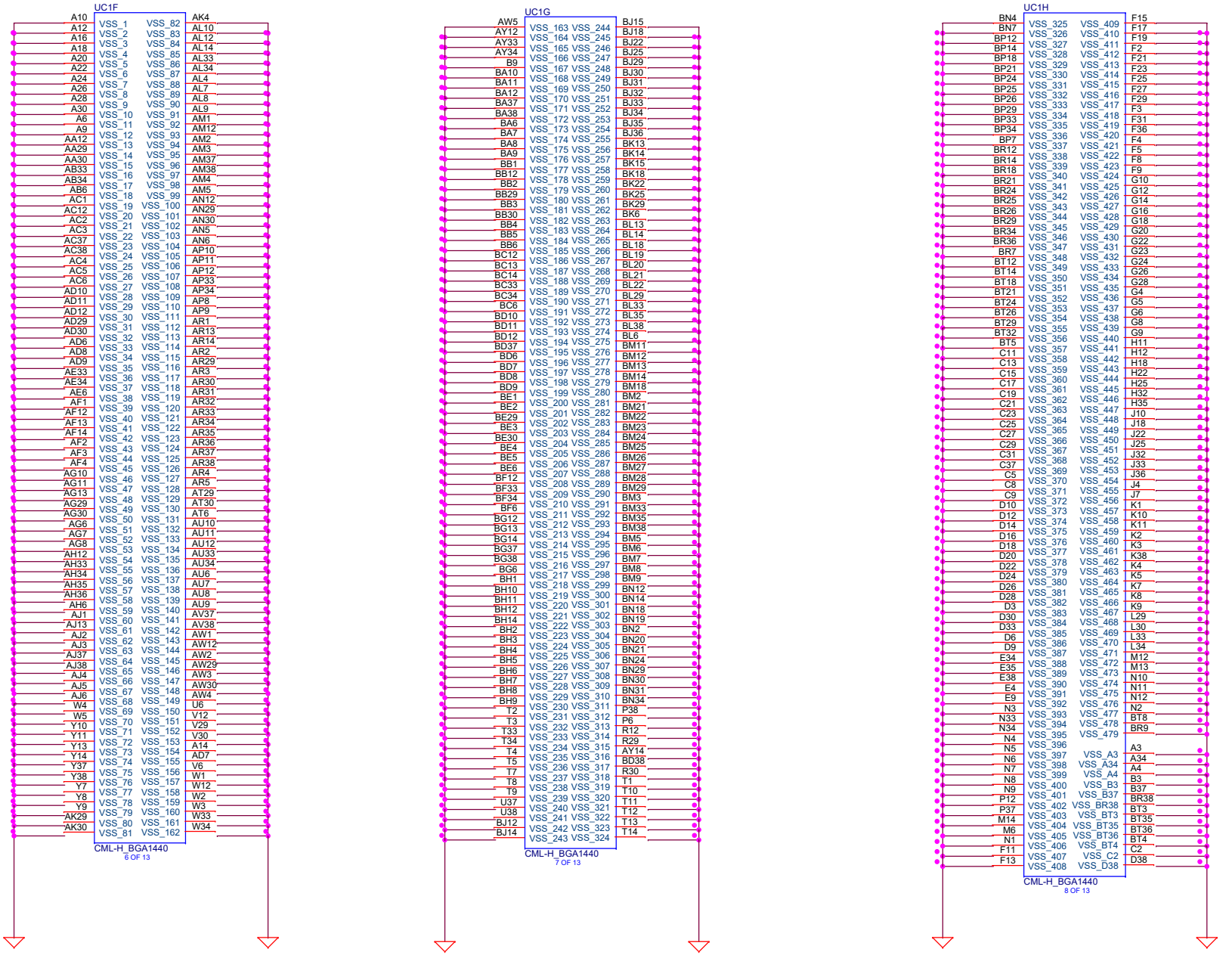

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Title: CML-H (8/8)

Size	Document Number	Rev
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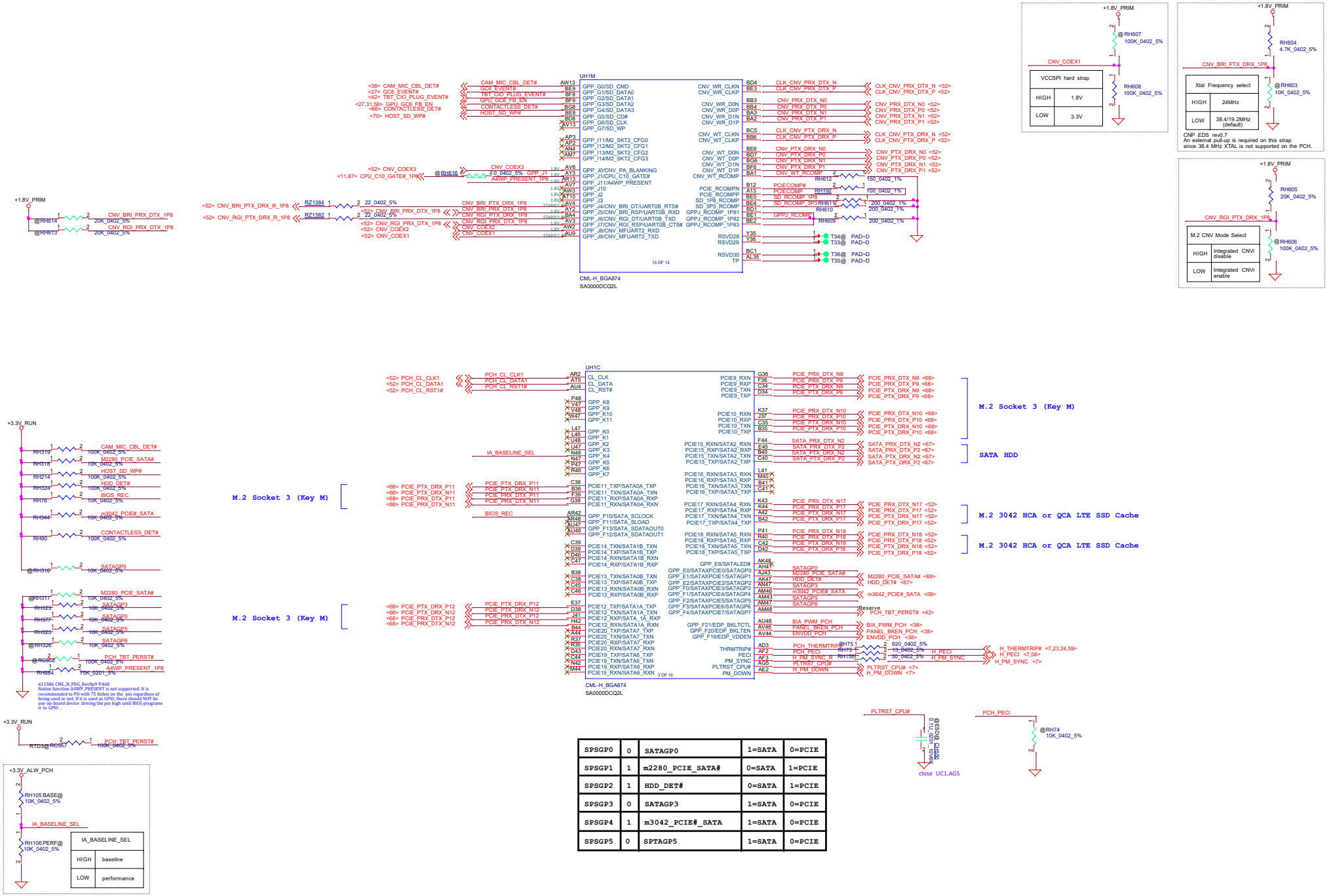

SPSGP0	0	SATAGP0	1=SATA	0=PCIE
SPSGP1	1	m2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	m3042_PCIE#_SATA	1=SATA	0=PCIE
SPSGP5	0	SPTAGP5	1=SATA	0=PCIE

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Title: CometLake PCH-H (1/9)			
Size: C	Document Number: LA-J282P		Rev: 1.0
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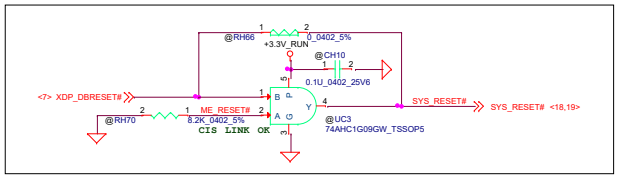

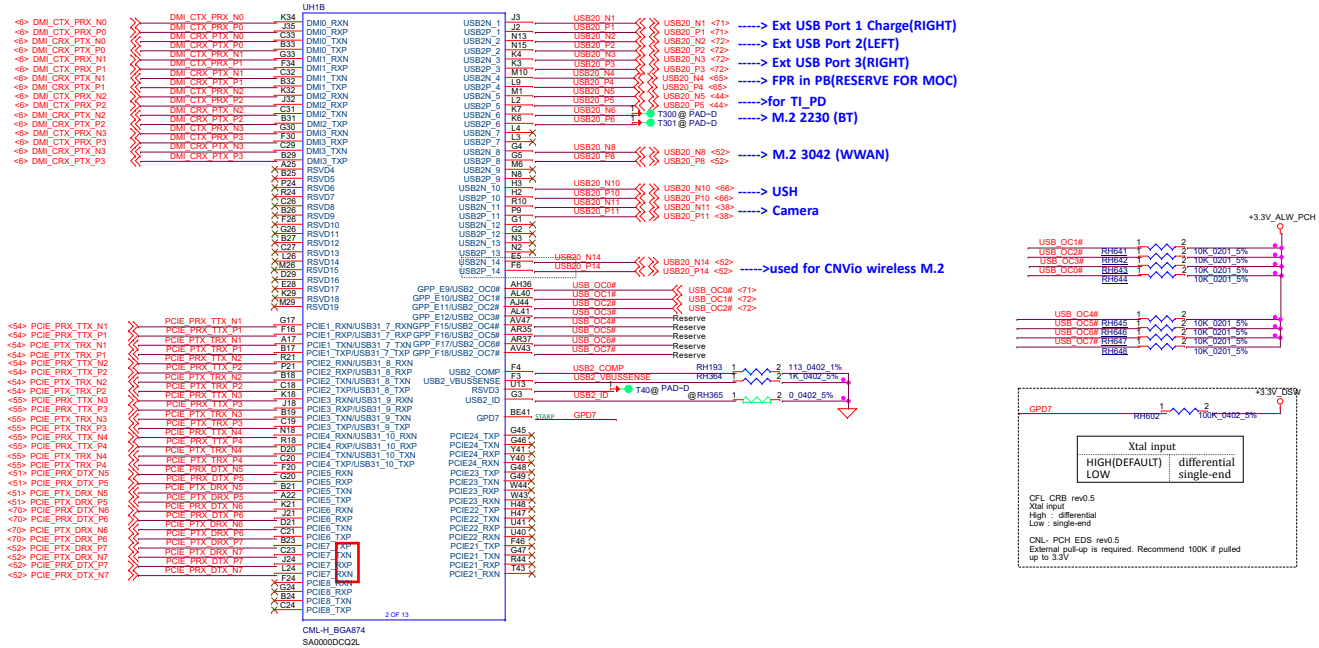

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Title: CometLake PCH-H (2/9)

Size	Document Number	Rev
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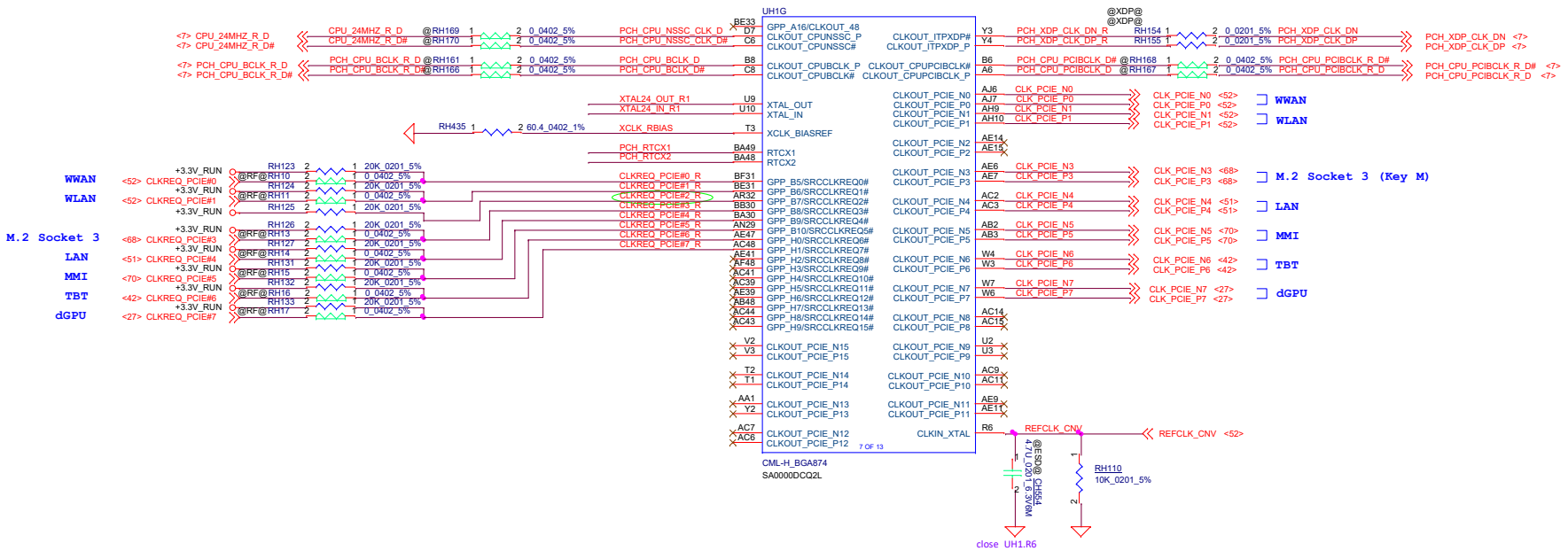

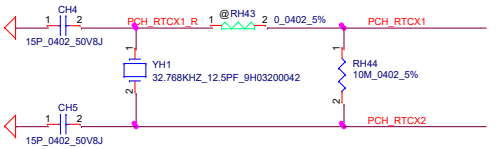

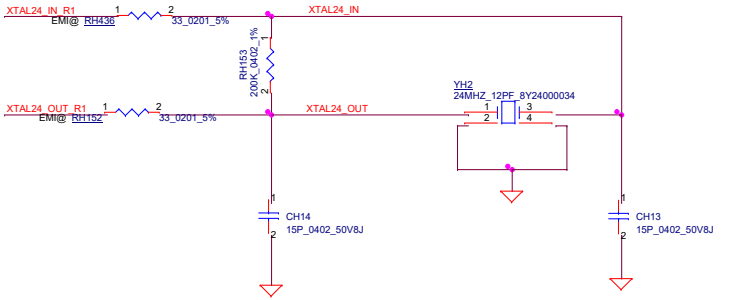

Security Classification	Compal Secret Data		
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support EC G3 flash

+3.3V_ALW_PCH

RH898 1 2 100K_0402_5% PCH_BT_RADIO_DIS#
@RH310 1 2 10K_0402_5% SIO_EXT_SMI#
@RH559 1 2 10K_0402_5% RTD3_CIO_PWR_EN
RH834 1 2 100K_0402_5% 3.3V_CAM_EN#
RH840 1 2 10K_0402_5% WWAN_GPIO_WAKE#
RH866 1 2 100K_0402_5% RTC_DET#

+3.3V_RUN

@RH348 1 2 10K_0402_5% TOUCH_SCREEN_PD#
TOUCH_SCREEN_PD# don't move to RPC,

@RH756 2 1 10K_0201_5% WWAN_GPIO_PERST#

+3.3V_ALW_PCH

PCH_PLTRST# → U UH7 MC74VHC1G08EDFT2G_SC70-5 → PCH_PLTRST#_AND
@RH65 100K_0402_5%
@RH187 2 1 0_0402_5% PCH_PLTRST#_AND <38,42,52,68,70>
PLTRST_TPM# <66>

UH1A CML-H_BGA874 SA0000DCQ2L 1 OF 13

<52> WWAN_BB_RST# WWAN_BB_RST# BE36 GPP_A11/PME#/SD_VDD2_PWR_EN#
PAD~D @T60 R15 RSVD2
PAD~D @T61 R13 RSVD1
PAD~D @T63 AL37 VSS247
PAD~D @T62 AN35 TP
<7> SYS_PWROK_R XDP@ RC128 1K_0201_1% PCH_SPI_D0_PCH AU41 SPI0_MOSI
PCH_SPI_D1_PCH BA45 SPI0_MISO
PCH_SPI_CS#0 AY47 SPI0_CS0#
PCH_SPI_CLK_PCH AW47 SPI0_CLK
AW48 SPI0_CS1#
<7> CPU_XDP_PRS CPU_XDP_PRS XDP@ RH180 1K_0402_5% PCH_SPI_D2_PCH AY48 SPI0_IO2
PCH_SPI_D3_PCH BA46 SPI0_IO3
<66> PCH_SPI_CS#2 PCH_SPI_CS#2 AT40 SPI0_CS2#
VPRO_DET# BE19 GPP_D1/SPI1_CLK/SBK1/BK1
BF19 GPP_D0/SPI1_CS#/SBK0/BK0
<52> WWAN_FULL_PWR_EN BF18 GPP_D3/SPI1_MOSI/SBK3/BK3
<83> RTC_DET# RTC_DET# BE18 GPP_D2/SPI1_MISO/SBK2/BK2
<38> 3.3V_CAM_EN# BC17 GPP_D22/SPI1_IO3
<52> WWAN_GPIO_PERST# WWAN_GPIO_PERST# BD17 GPP_D21/SPI1_IO2
<52> WWAN_GPIO_WAKE# WWAN_GPIO_WAKE#
GPP_B13/PLTRST# AV29 PCH_PLTRST#
GPP_K16/GSXCLK Y47
GPP_K12/GSXDOUT Y46
GPP_K13/GSXSLOAD Y48
GPP_K14/GSXDIN W46
GPP_K15/GSXSRESET# AA45
GPP_E3/CPU_GP0 AL47 SIO_EXT_SMI#
GPP_E7/CPU_GP1 AM45 TOUCH_SCREEN_PD#
GPP_B3/CPU_GP2 BF32 PCH_BT_RADIO_DIS# <52>
GPP_B4/CPU_GP3 BC33 TOUCH_SCREEN_DET# <38>
GPP_H18/SML4ALERT# AE44
GPP_H17/SML4DATA AJ46
GPP_H16/SML4CLK AE43
GPP_H15/SML3ALERT# AC47 GPP_H15
GPP_H14/SML3DATA AD48
GPP_H13/SML3CLK AE47
GPP_H12/SML2ALERT# AB47 GPP_H12
GPP_H11/SML2DATA AD47
GPP_H10/SML2CLK AE48
INTRUDER# BB44 PCH_INTRUDER_HDR#

@RH62 2 1 0_0402_5% PLTRST_LAN# <51>
@RH195 2 1 0_0402_5% PLTRST_GPU# <27>
@RH566 0_0402_5% TOUCH_SCREEN_PD#_R <38>
RTD3_CIO_PWR_EN <42,54>
+RTC_CELL_PCH RH198 1M_0402_5%

PCH_PLTRST# @ESD@ CH552 0.1U_0201_10V6K
ESD request 7/25 Close UH1.AE3

PCH Signal Glitch Free Implementation Requirements
PCH_PLTRST# @RH635 100K_0201_5%
PCH_SPI_CLK_PCH RH634 100K_0201_5%
CML-H PDG0.91 P171 required.

eSPI Flash sharing mode (GPP_H12)
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

+3.3V_SPI

@RH615 GPP_H12 2.2K_0402_5%
RH601 GPP_H15 100K_0402_5%
RH600 PCH_SPI_D0_PCH 100K_0402_5%
RH269 PCH_SPI_D1_PCH 100K_0402_5%
RH30 PCH_SPI_D2_PCH 20K_0402_5%
RH335 PCH_SPI_D3_PCH 20K_0402_5%
RH206 PCH_SPI_CS#0 4.7K_0402_5%
@RH334 PCH_SPI_D3_PCH 1K_0402_5%

Follow CML-H PDG V0.9 P367 SPI0 Wire-OR topology
RH877~RH881 0 ohm

Topology R1 loaction

From PCH --->
PCH_SPI_CLK_PCH @RH877 0_0201_5% PCH_SPI_CLK → PCH_SPI_CLK <66>
PCH_SPI_D0_PCH @RH878 0_0201_5% PCH_SPI_D0 → PCH_SPI_D0 <66>
PCH_SPI_D1_PCH @RH879 0_0201_5% PCH_SPI_D1 → PCH_SPI_D1 <66>
PCH_SPI_D2_PCH @RH880 0_0201_5% PCH_SPI_D2
PCH_SPI_D3_PCH @RH881 0_0201_5% PCH_SPI_D3
--->To TPM

Follow CML-H PDG V0.9 P367 SPI0 Wire-OR topology
RH656,RH351 need to be 22ohm for 3.3V, others 33ohm

Topology R3 loaction

From EC --->
<58> SHD_CLK 33_0201_1% RH871
<58> SHD_IO0 33_0201_1% RH872
<58> SHD_IO1 33_0201_1% RH873
<58> SHD_IO2 75_0201_1% RH874
<58> SHD_IO3 75_0201_1% RH875
PCH_SPI_CLK_0_R RH653 PCH_SPI_CLK_0_R
PCH_SPI_D0_0_R RH654 PCH_SPI_D0_0_R
PCH_SPI_D1_0_R RH655 PCH_SPI_D1_0_R
PCH_SPI_D2_0_R RH656 PCH_SPI_D2_0_R
PCH_SPI_D3_0_R RH351 PCH_SPI_D3_0_R
--->To UC5 ROM

Topology R2 loaction

<58> SHD_CS#0 @RH876 0_0201_5% PCH_SPI_CS#0

Follow CML-H PDG V0.9 P367 SPI0 Wire-OR topology
RH874,RH875 need to be 75 ohm for 3.3V, others 33ohm

PCH_SPI_CLK 1 PCH_SPI_D0 1 PCH_SPI_D1 1 PCH_SPI_D2 1 PCH_SPI_D3 1 → VIA–D @VIA1 @VIA2 @VIA3 @VIA4 @VIA5
VIA for Auto TLCT Footprint:TP_18D8

G3 sharing WDT circuit

QZ9 @ 2N7002KW_SOT323-3
<18> VCCDSW_EN_Q
RZ663 @ 200K_0402_1%
CZ622 @ 0.33U_0402_10V6K
PCH_RSMRST# <58,62,63>

For vPro & Non-vPro
32MB WSON8 Flash ROM

+3.3V_SPI
CH9 0.1U_0201_10V6K
PCH_SPI_CS#0 @RH437 0_0201_5% SPI_CS#0_R
PCH_SPI_D1_0_R
PCH_SPI_D2_0_R
UC5 GD25B256DYIG_WSON8_8X6
CS# SO(IO1) IO2 VSS VCC IO3 SCLK SI(IO0) ThermalPad
PCH_SPI_D3_0_R
PCH_SPI_CLK_0_R
PCH_SPI_D0_0_R

FOLLOW BHMLK ARD Rev2.0
BIOS ROM(16MB/32MB)
Dell Approved P/N's (See Dell EMG 013005 for updates)
Single flash footprint Configs: 32MB (W25Q256JWEIQ, Winbond W25Q256JWEIQ, Gigadevice GD25B256D, MXIC MX25L25673GZ4I)

JXT FP243A-020G1BM
GND_2 GND_1
PCH_SPI_D0 PCH_SPI_D1 PCH_SPI_CLK PCH_SPI_CS#0 PCH_SPI_D2 PCH_SPI_D3
JSPI1 CONN@ SP01001W100
use ACES_50696-0200M-P01_20P footprint

+3.3V_SPI
+3.3V_ALW_PCH
<63> PROM_BIOS_R
DH3 RB751S40_SOD523-2
@RH185 0_0402_5%
DH3 use fp RB520SM-30T2R_EMD2-2

+3.3V_ALW_PCH
NVPRO@ RH885 10K_0201_5%
VPRO_DET#
VPRO@ RH886 10K_0201_5%

VPRO_DET#	
HIGH	NON VPRO
LOW	VPRO

PCH_SPI_CLK_0_R
@EMI@ RH29 33_0402_5%
@EMI@ CH622 33P_0402_50V8J

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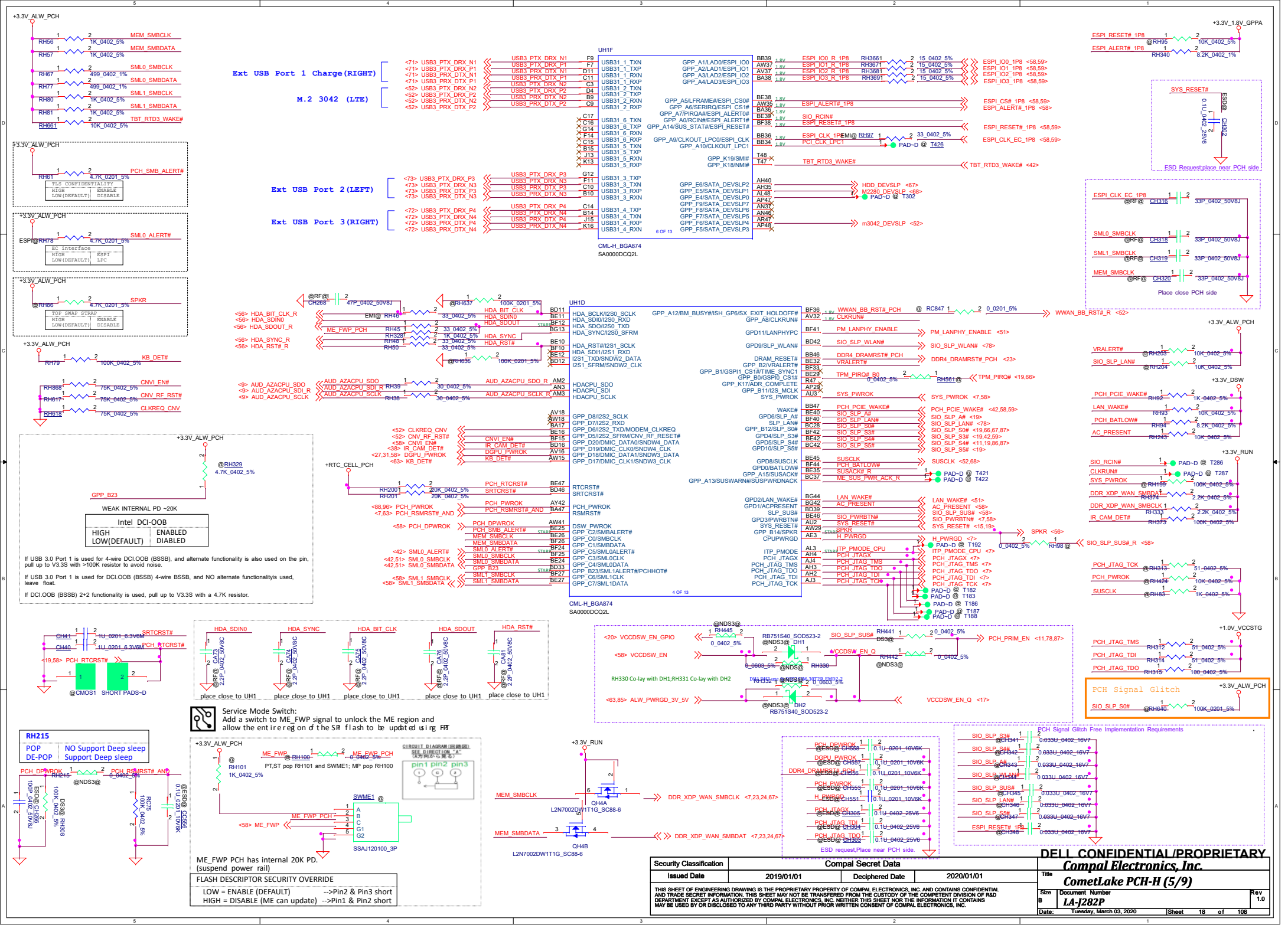
Ext USB Port 1 Charge(RIGHT)
M.2 3042 (LTE)
Ext USB Port 2(LEFT)
Ext USB Port 3(RIGHT)
UH1F
CML-H_BGA874
SA0000DCQ2L
UH1D
CML-H_BGA874
SA0000DCQ2L
Intel DCI-OOB
HIGH ENABLED
LOW(DEFAULT) DIABLED
If USB 3.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
If USB 3.0 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionalityis used, leave float.
If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT
RH215
POP NO Support Deep sleep
DE-POP Support Deep sleep
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin2 & Pin3 short
HIGH = DISABLE (ME can update) -->Pin1 & Pin2 short
ME_FWP PCH has internal 20K PD. (suspend power rail)
PT,ST pop RH101 and SWME1; MP pop RH100
PCH Signal Glitch Free Implementation Requirements
PCH Signal Glitch
Security Classification Compal Secret Data
Issued Date 2019/01/01 Deciphered Date 2020/01/01
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Size B Document Number LA-J282P Rev 1.0
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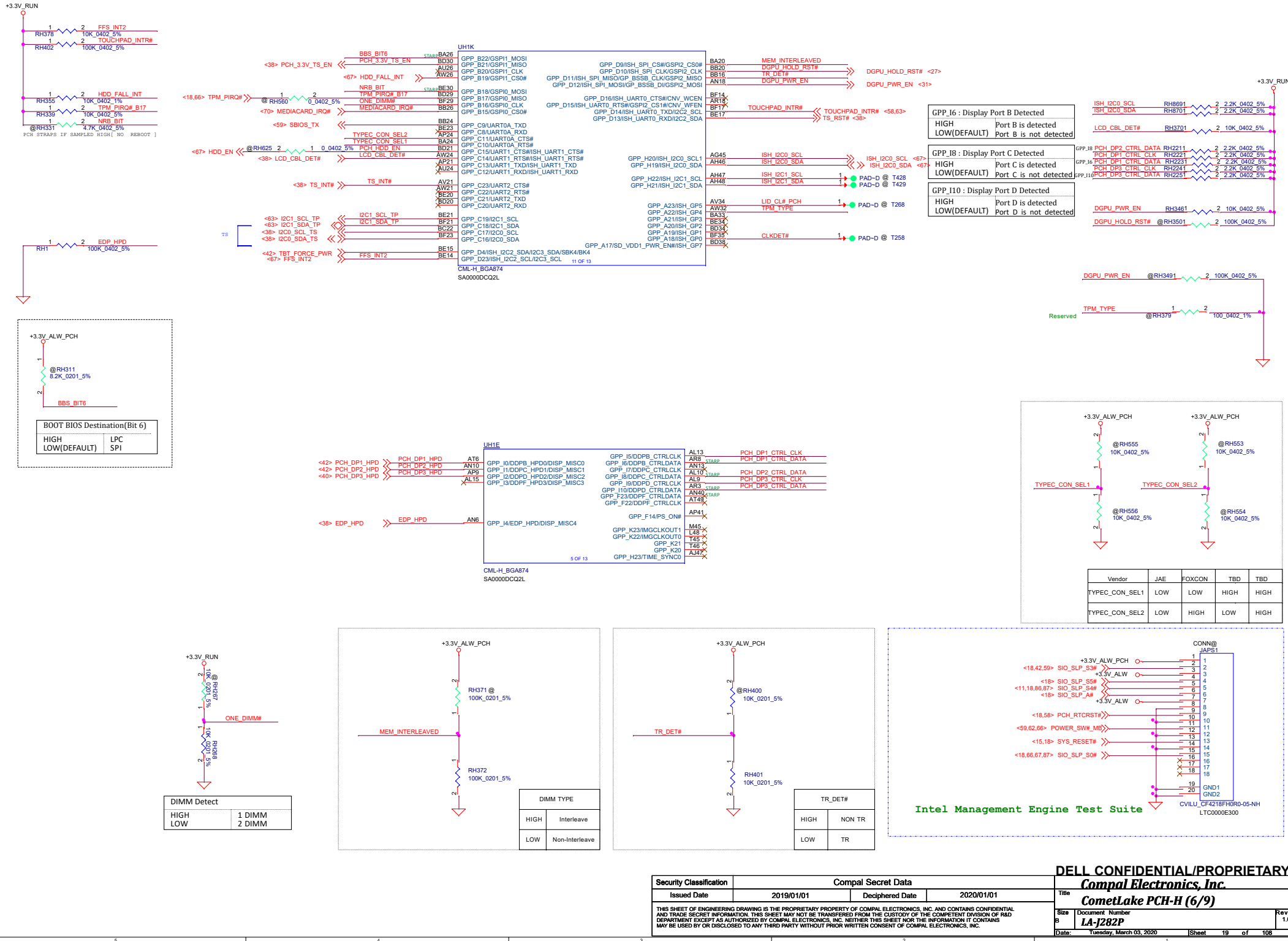

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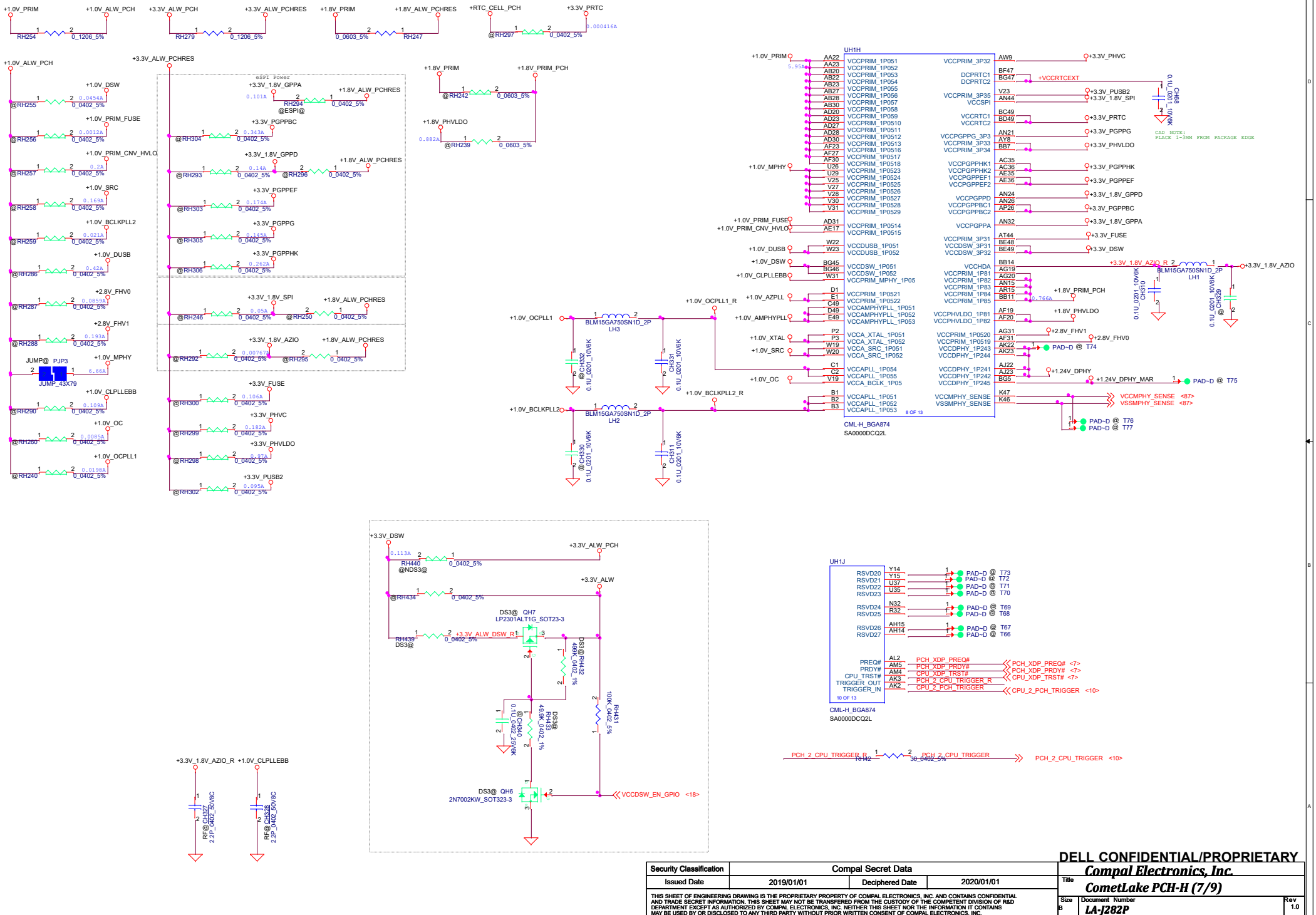

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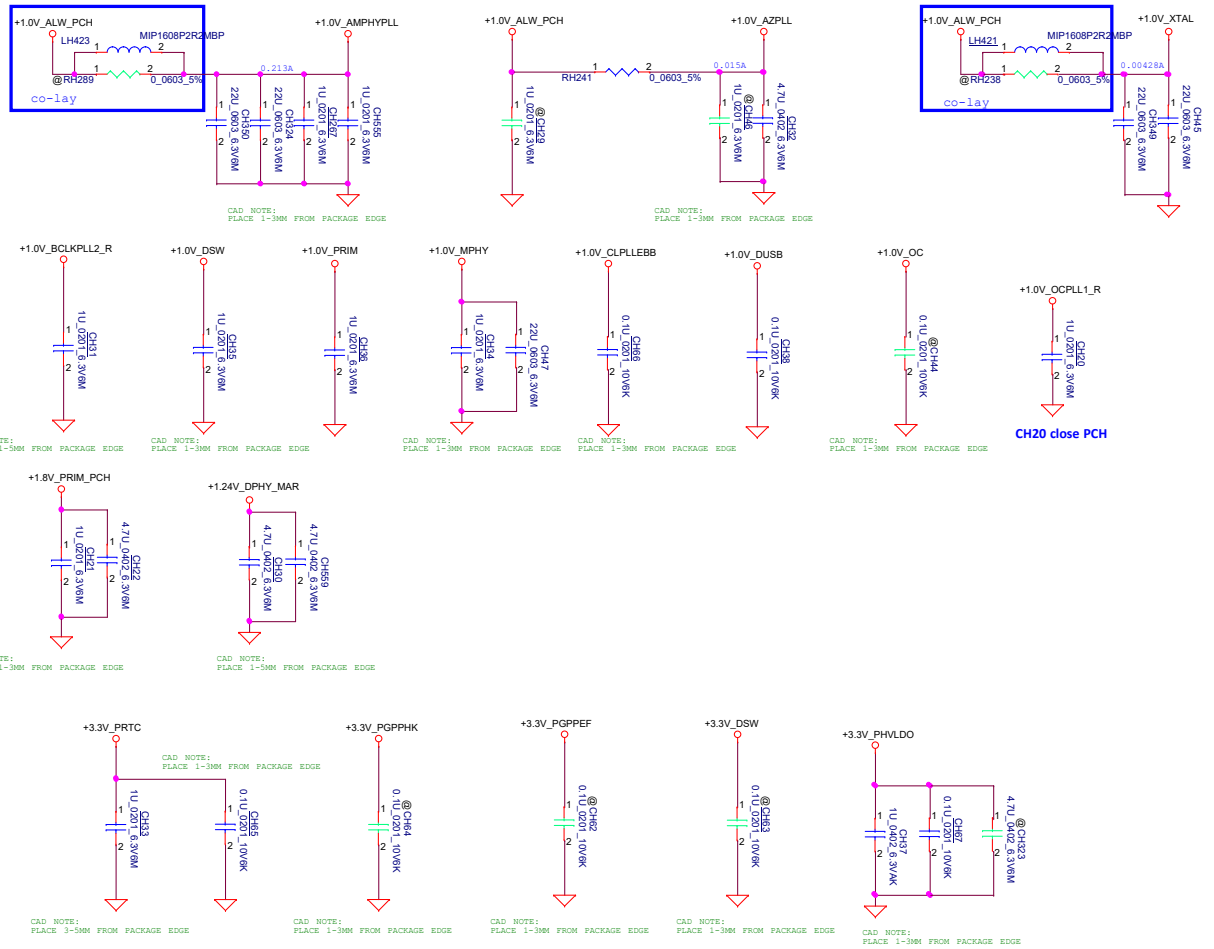
PCH Decoupling cap Follow 611586_CML_H_PDG_Rev0p7
page. 598 Table 329. Decoupling and Power Connection Requirements for PCH-H



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Title: CometLake PCH-H (8/9)

Size: B | Document Number: LA-J282P | Rev: 1.0

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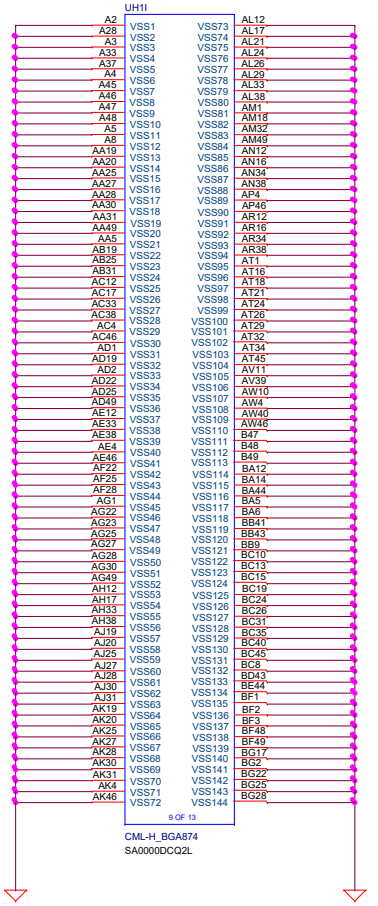

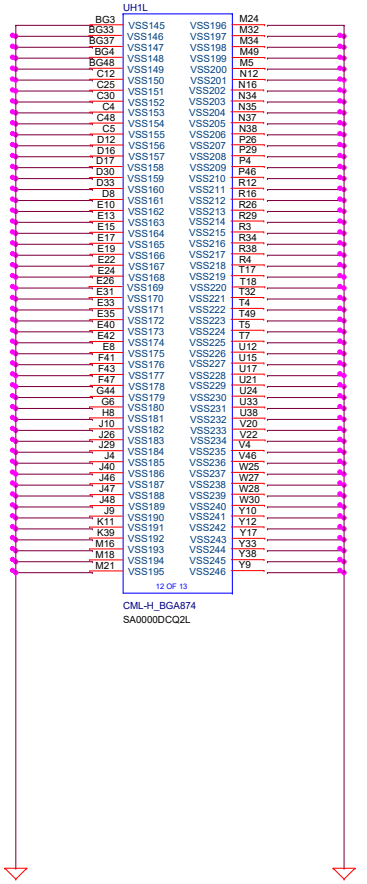

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Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Title: CometLake PCH-H (1/9)

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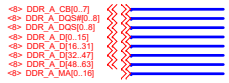
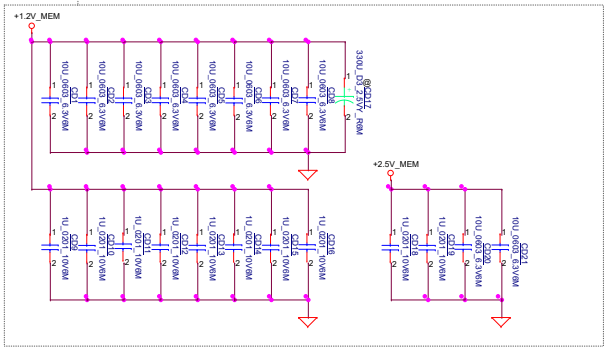
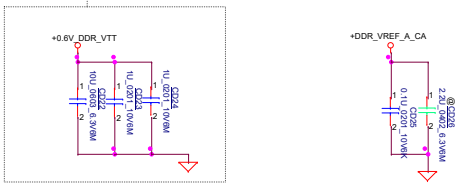


Layout Note:
Place near JDIMM1

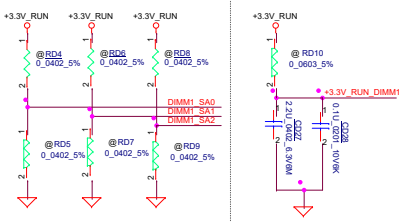
SODIMM Decoupling cap Follow 611586_CML_H_PDG_Rev0p7 page. 126 Table 28. DDR4 SODIMM Power Plane Decoupling



Layout Note:
Place near
JDIMM1.258

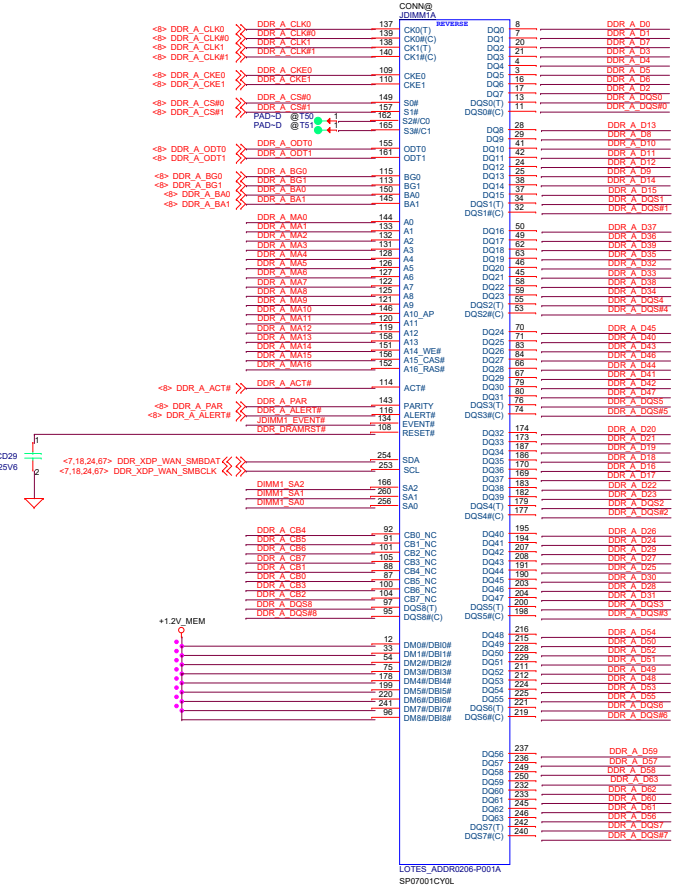


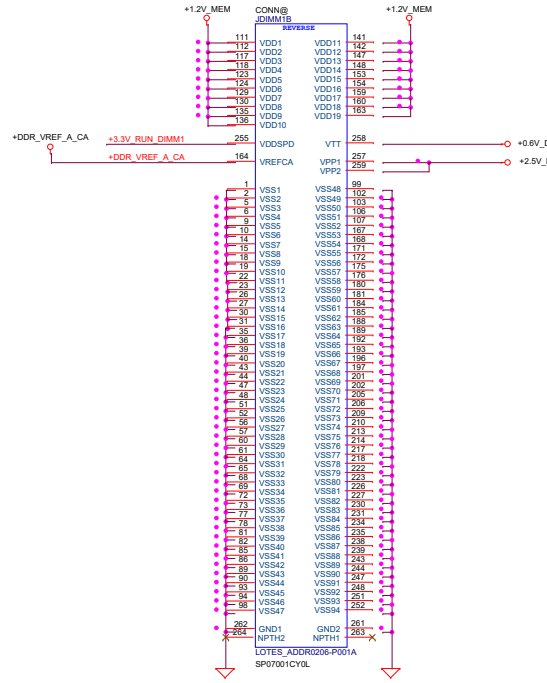
DIMM Select

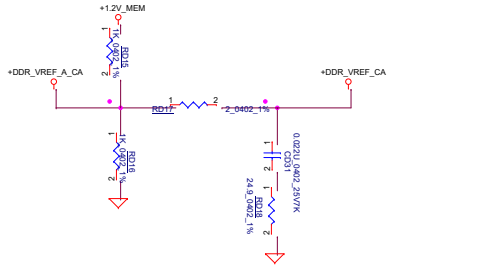


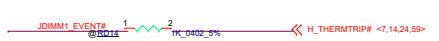
	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

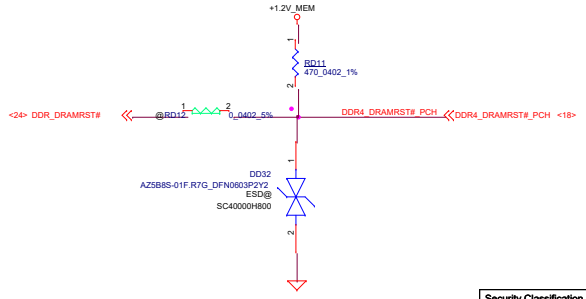
Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

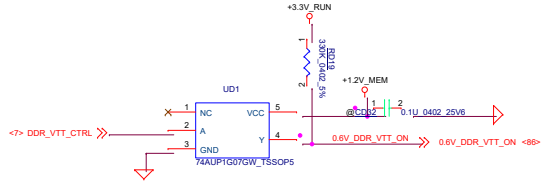












Compal Electronics, Inc.	
Title	DDR4-SODIMM SLOT1
Size	C
Document Number	LA-J282P
Rev	1.0
Date	Tuesday, March 03, 2020
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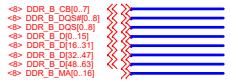
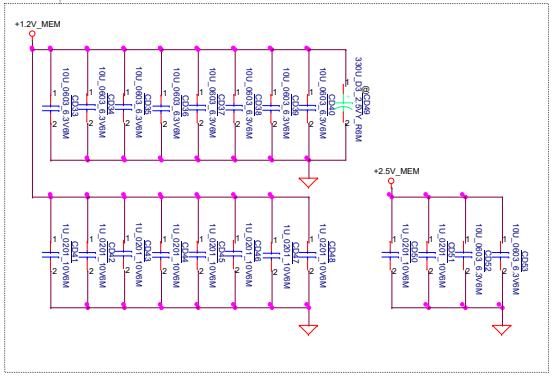
Issued Date	2019/01/01	Deciphered Date 2020/01/01

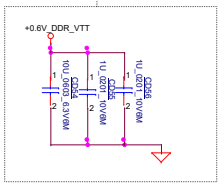


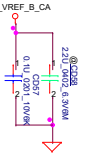
Layout Note:
Place near JDIMM2

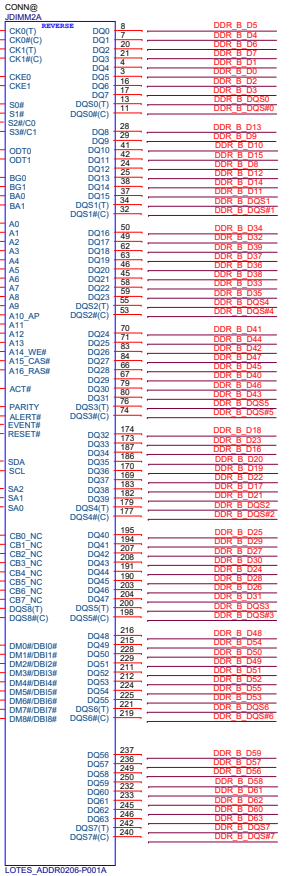
SODIMM Decoupling cap Follow 611586_CML_H_PDG_Rev0p7
page. 126 Table 28. DDR4 SODIMM Power Plane Decoupling

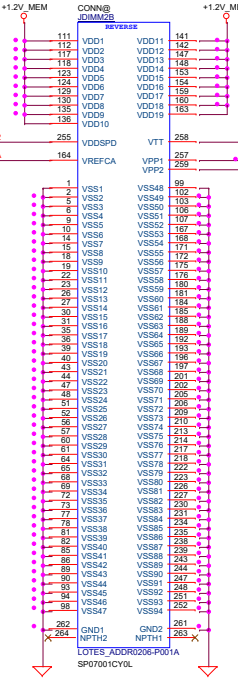


Layout Note:
Place near
JDIMM2.258

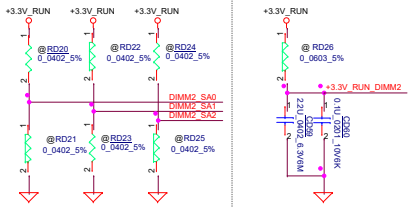




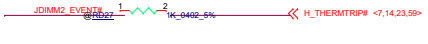


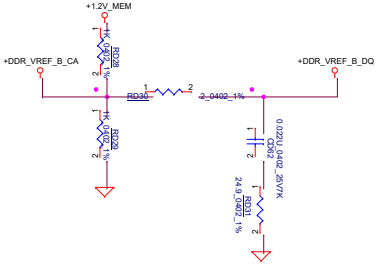


DIMM Select



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0





Byte[0]	DQ[7:0]	DQS/DQS#[0]
Byte[1]	DQ[15:8]	DQS/DQS#[1]
Byte[2]	DQ[23:16]	DQS/DQS#[2]
* Byte[3]	DQ[31:24]	DQS/DQS#[3]
Byte[4]	DQ[39:32]	DQS/DQS#[4]
* Byte[5]	DQ[47:40]	DQS/DQS#[5]
Byte[6]	DQ[55:48]	DQS/DQS#[6]
Byte[7]	DQ[63:56]	DQS/DQS#[7]

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: DDR4-SODIMM SLOT2

Size	Document Number	Rev
C	LA-J282P	1.0

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Reserve

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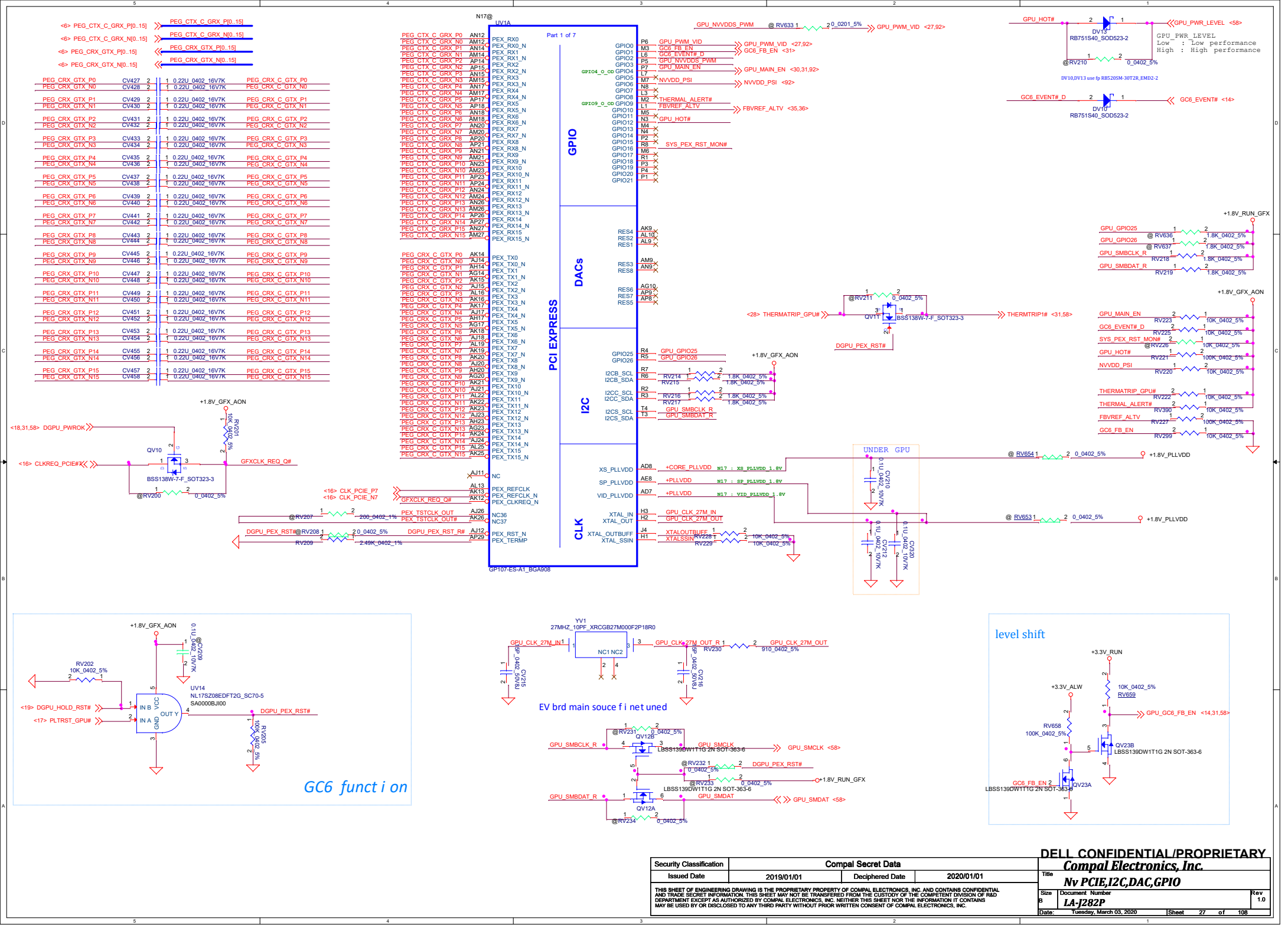
Compal Electronics, Inc.

Title: DDR_3

Size | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 26 of 108



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Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Compal Electronics, Inc.

Title: Nv PCIE,I2C,DAC,GPIO

Size	Document Number	Rev
B	LA-J282P	1.0

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I2CS Slave Address

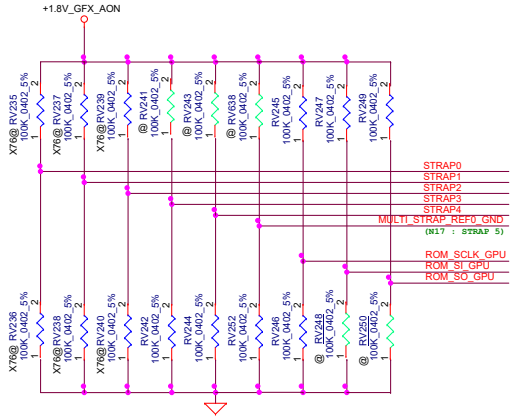
SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

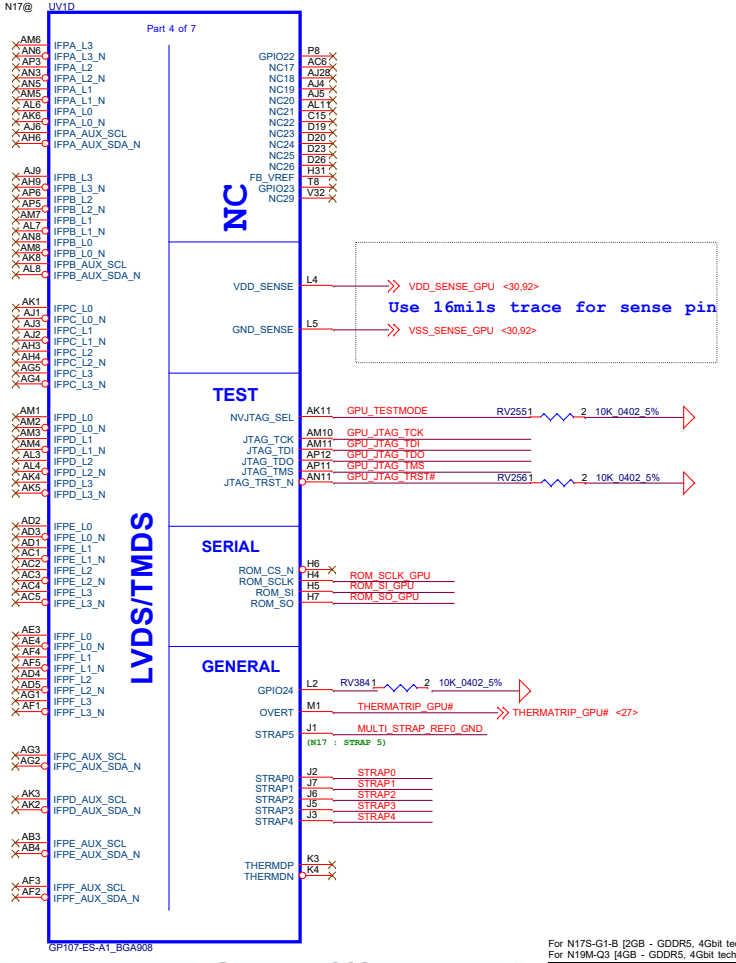
VGA_DEVICE Setting

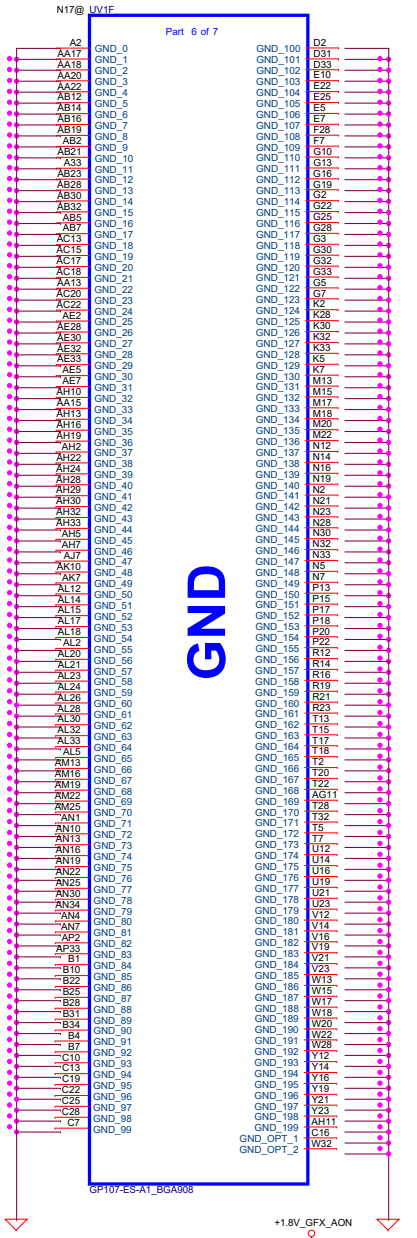
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

N17S-G1-B Decive ID 0x1C90

N19M-Q3 Decive ID 0x1CBD







Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

For N17S-G1-B [2GB - GDDR5, 4Gbit technology, 2pcs x 32]
For N19M-Q3 [4GB - GDDR5, 4Gbit technology, 4pcs x 32]

VENDER	STRAP	Part Number	Note (Strap2,Strap1,Strap0)
Micron	0x4	MT51J256M32HF-80:B SA00009TI3L	(H, L, L)
Hynix	0x5	H5GC8H24AJR-R2C SA0000C171L	(H, L, H)
Samsung	0x3	K4G80325FC-HC25 SA00009TA3L	(L, H, H)

SAMSUNG ONLY FOR N17S-G1-B

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Title: Nv DP, STRAP, GND

Size	Document Number	Rev
B	LA-J282P	1.0

Date: Tuesday, March 03, 2020 Sheet 28 of 108

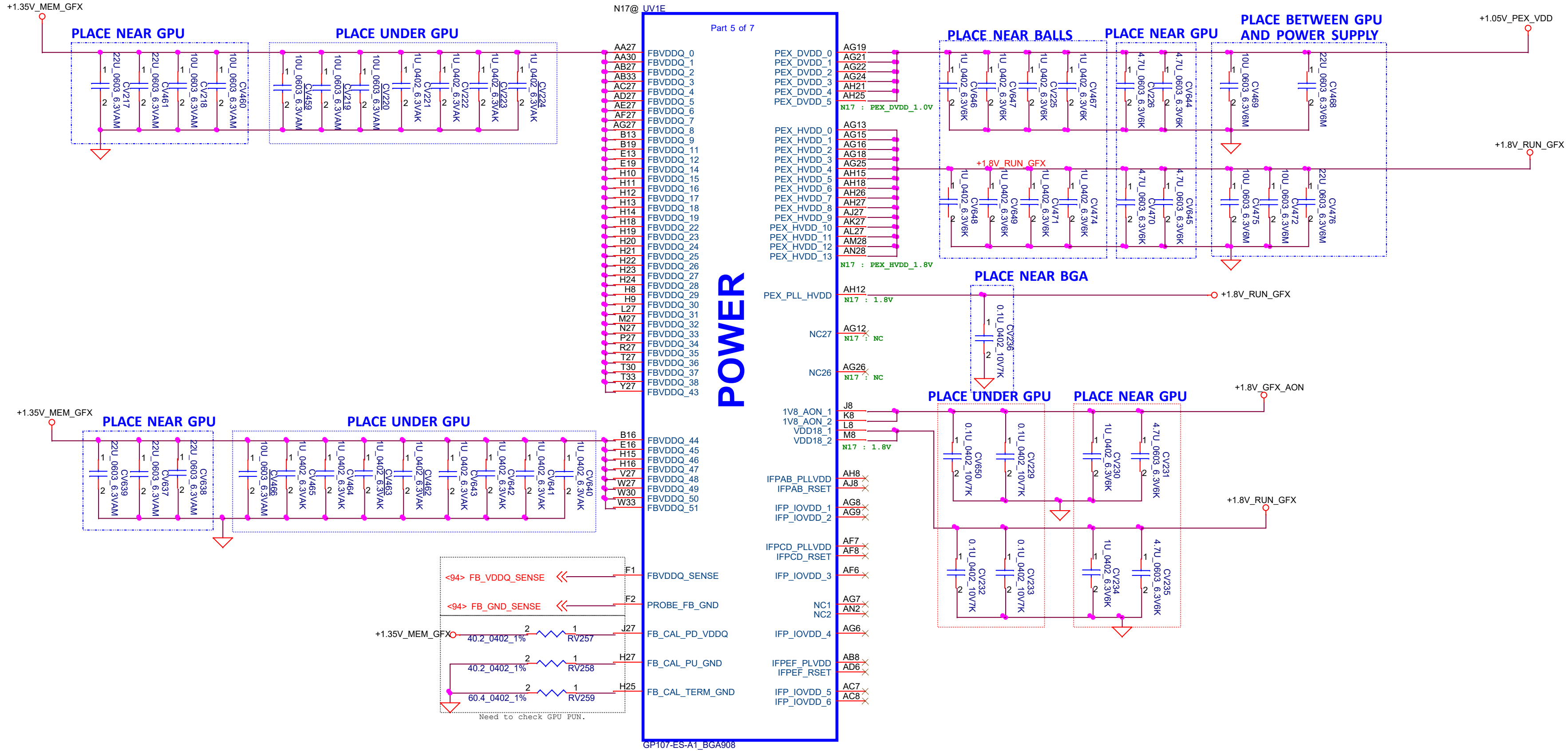


Table 3. PCB Power Nets and GPU Power Rails for N16/GB4B-128 and N17/GB4C-128 GPUs Co-Design

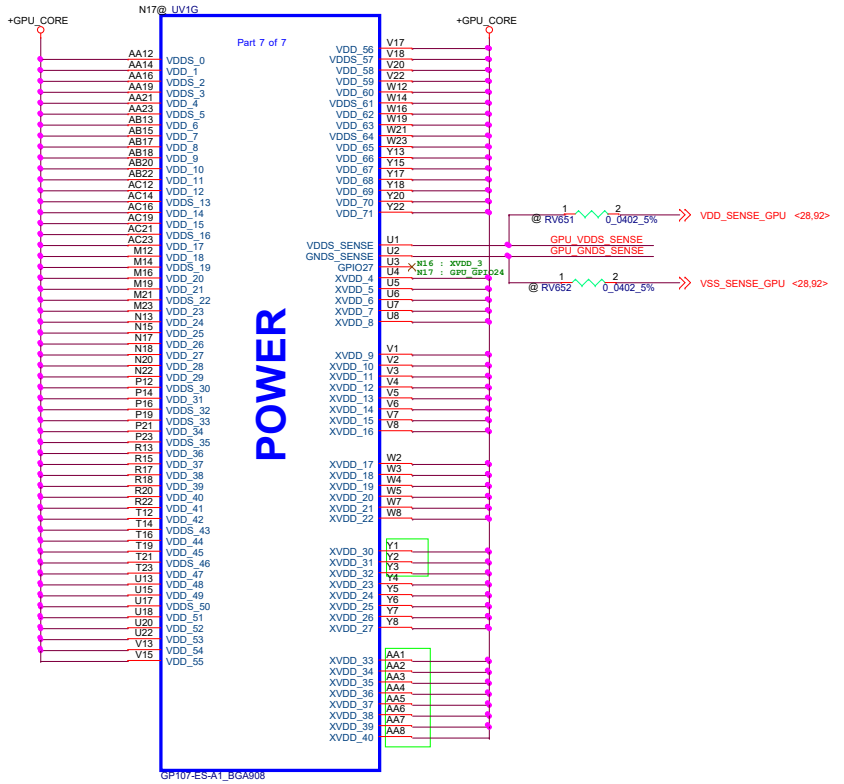
PCB Net	N16 Power Rail/Pins	N16 Nominal Value	N17 Power Rail/Pins	N17 Nominal Value
NVVDD	VDD	Variable	VDD	Variable
NVVDDS	-	N/A	VDDS	Variable
FBVDD	FBVDDQ, FBVDDQ_AON	{1.35, 1.5} V	FBVDDQ	{1.35, 1.5, 1.55} V
PEX_VDD or VDD_MAIN	FBx_PLL_AVDD (x=A, B)	N16P: 1.05 V N16E: 3.3 V	FBx_PLL_AVDD (x=A, B)	1.8 V
PEX_VDD or VDD_MAIN	FB_DLL_AVDD	1.05 V	FB_REFPLL_AVDD	1.8 V
PEX_VDD	PEX_IOVDD	1.05 V	PEX_DVDD	1.0 V
PEX_VDD or VDD_MAIN	PEX_IOVDDQ	1.05 V	PEX_HVDD	1.8 V
PEX_VDD	PEX_PLLVDD	1.05 V	-	NC
VDD_AON	PEX_SVDD_3V3	3.3 V	-	NC
VDD_AON or VDD_MAIN	PEX_PLL_HVDD	3.3 V	PEX_PLL_HVDD	1.8 V
PEX_VDD or VDD_MAIN	PLLVDD	1.05 V	XS_PLLVDD	1.8 V
PEX_VDD or VDD_MAIN	VID_PLLVDD	1.05 V	VID_PLLVDD[2]	1.8 V
PEX_VDD or VDD_MAIN	SP_PLLVDD	1.05 V	SP_PLLVDD	1.8 V
VDD_MAIN	FB_VREF	NC	GPCPLL_AVDD	1.8 V
VDD_MAIN	DACA_VDD[1]	RES	-	NC
VDD_MAIN	3V3_MAIN	3.3 V	VDD18	1.8 V
VDD_AON	3V3_AON	3.3 V	1V8_AON	1.8 V

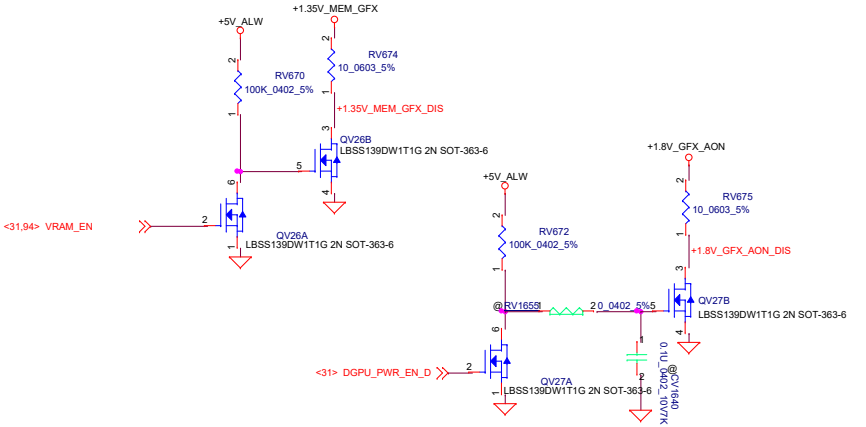
Compal Electronics, Inc.

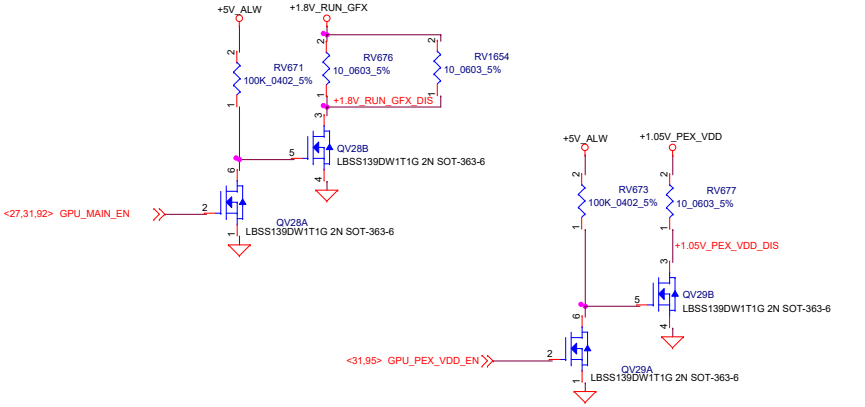
Title: Nv Power

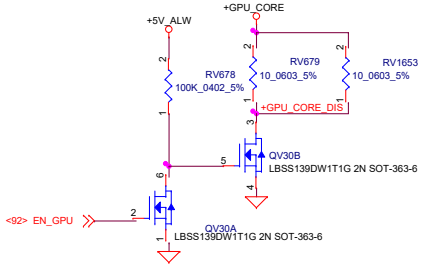
Size: B | Document Number: LA-J282P | Rev: 1.0

Caps on Power Side
1UX8 4.7UX15 under GPU
4.7UX5 22UX7 330UX1 near GPU









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Compal Electronics, Inc.

Title: *Nv Power GFX Core*

Size	Document Number	Rev
B	*LA-J282P*	1.0

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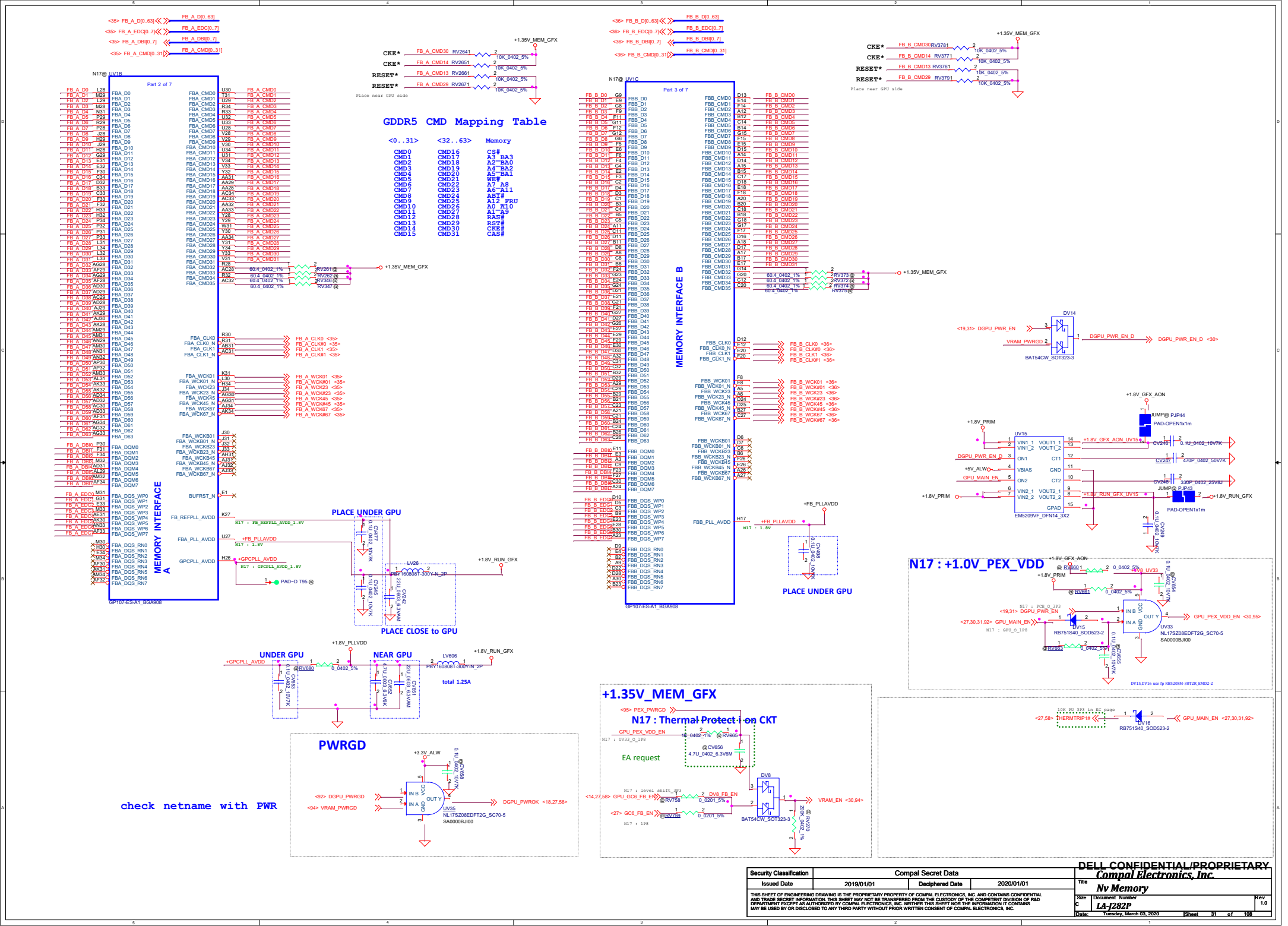
GDDR5 CMD Mapping Table
<0..31> <32..63> Memory
CMD0 CMD16 CS#
CMD1 CMD17 A3_BA3
CMD2 CMD18 A2_BA0
CMD3 CMD19 A4_BA2
CMD4 CMD20 A5_BA1
CMD5 CMD21 WE#
CMD6 CMD22 A7_A8
CMD7 CMD23 A6_A11
CMD8 CMD24 ABI#
CMD9 CMD25 A12_FBU
CMD10 CMD26 A0_A10
CMD11 CMD27 A1_A9
CMD12 CMD28 RAS#
CMD13 CMD29 RST#
CMD14 CMD30 CKE#
CMD15 CMD31 CAS#
N17@ U1V1B
Part 2 of 7
MEMORY INTERFACE A
GP107-ES-A1_BGA908
N17@ U1V1C
Part 3 of 7
MEMORY INTERFACE B
GP107-ES-A1_BGA908
PLACE UNDER GPU
PLACE CLOSE to GPU
PLACE UNDER GPU
UNDER GPU
NEAR GPU
total 1.25A
N17 : +1.0V_PEX_VDD
PWRGD
check netname with PWR
+1.35V_MEM_GFX
N17 : Thermal Protect : on CKT
EA request
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Nv Memory
LA-J282P
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Reserve

Reserve

Reserve

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

NORMAL

MIRROR

BYTE0 BYTE1 BYTE2 BYTE3 BYTE4 BYTE5 BYTE6 BYTE7

170-BALL SGRAM GDDR5

MT51J256M32HF-70:B

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Title	Compal Electronics, Inc.		
	GDDR5 VRAM A		
Size	Document Number		Rev
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GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

NORMAL

MIRROR

BYTE0 BYTE1 BYTE2 BYTE3 BYTE4 BYTE5 BYTE6 BYTE7

170-BALL SGRAM GDDR5

MT51J256M32HF-70:B

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.			
Title: GDDR5 VRAM B			
Size: C	Document Number: LA-J282P		Rev: 1.0
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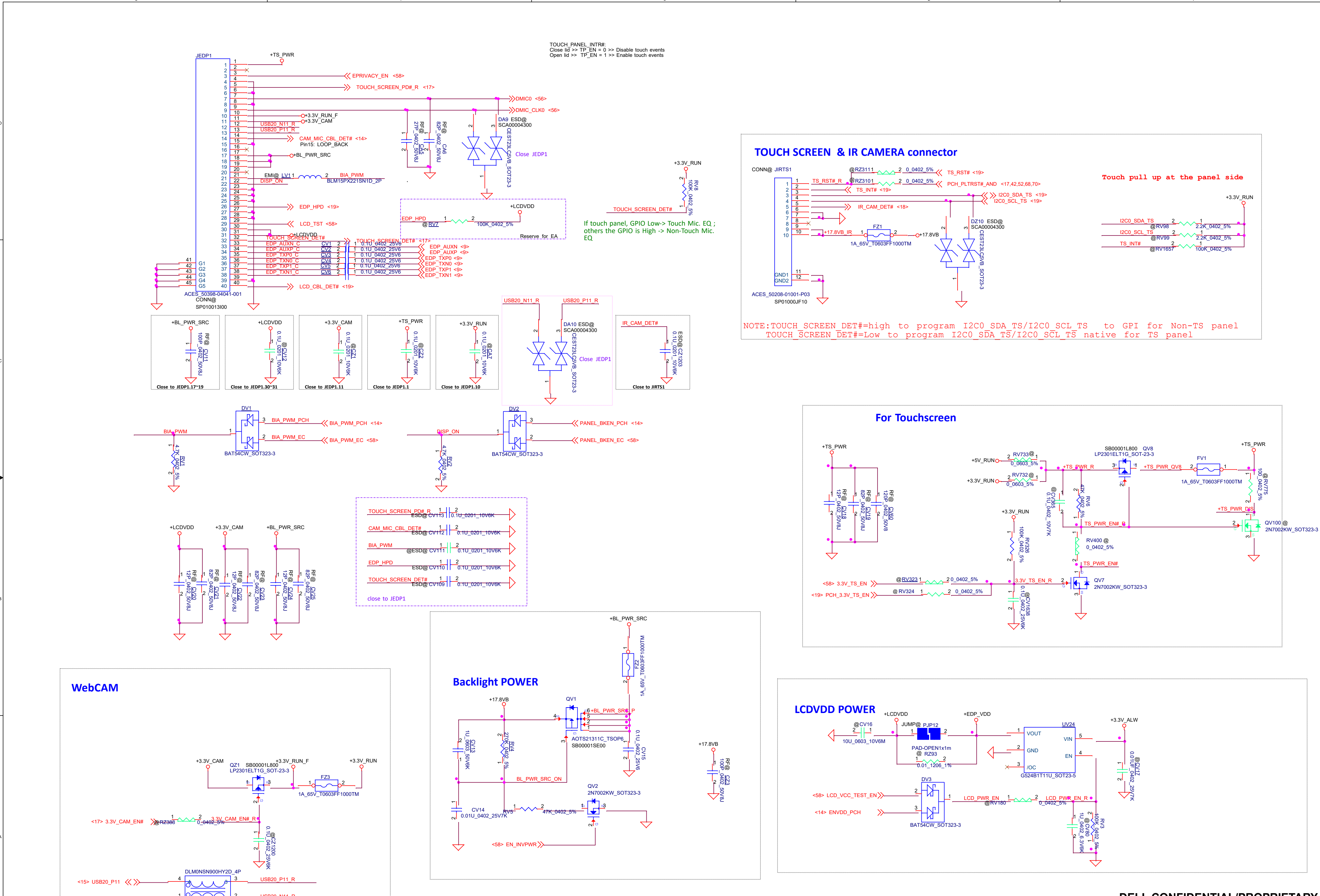
Reserve

Compal Electronics, Inc.

Title: DGPU_DC/DC Interface

Size | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 37 of 108


TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events
JEDP1
+TS_PWR
EPRIVACY_EN <58>
TOUCH_SCREEN_PD#_R <17>
DMIC0 <56>
DMIC_CLK0 <56>
+3.3V_RUN_F
+3.3V_CAM
USB20_N11_R
USB20_P11_R
CAM_MIC_CBL_DET# <14>
Pin15: LOOP_BACK
+BL_PWR_SRC
BIA_PWM
DISP_ON
BLM15PX221SN1D_2P
EDP_HPD <19>
LCD_TST <58>
+LCDVDD
TOUCH_SCREEN_DET#
EDP_AUXN <9>
EDP_AUXP <9>
EDP_TXP0 <9>
EDP_TXN0 <9>
EDP_TXP1 <9>
EDP_TXN1 <9>
LCD_CBL_DET# <19>
ACES_50398-04041-001
CONN@
SP010013I00
DA9 ESD@
SCA00004300
CESD23LC5VB_SOT23-3
Close JEDP1
Reserve for EA
If touch panel, GPIO Low-> Touch Mic. EQ ; others the GPIO is High -> Non-Touch Mic. EQ
TOUCH SCREEN & IR CAMERA connector
CONN@ JIRTS1
TS_RST#_R
TS_RST# <19>
PCH_PLTRST#_AND <17,42,52,68,70>
TS_INT# <19>
I2C0_SDA_TS <19>
I2C0_SCL_TS <19>
IR_CAM_DET# <18>
+17.8VB_IR
FZ1
1A_65V_T0603FF1000TM
+17.8VB
DZ10 ESD@
SCA00004300
ACES_50208-01001-P03
SP01000JF10
Touch pull up at the panel side
+3.3V_RUN
NOTE:TOUCH_SCREEN_DET#=high to program I2C0_SDA_TS/I2C0_SCL_TS to GPI for Non-TS panel
TOUCH_SCREEN_DET#=Low to program I2C0_SDA_TS/I2C0_SCL_TS native for TS panel
Close to JEDP1.17~19
Close to JEDP1.30~31
Close to JEDP1.11
Close to JEDP1.1
Close to JEDP1.10
Close to JIRTS1
DA10 ESD@
SCA00004300
DV1
BIA_PWM_PCH <14>
BIA_PWM_EC <58>
BAT54CW_SOT323-3
DV2
PANEL_BKEN_PCH <14>
PANEL_BKEN_EC <58>
close to JEDP1
For Touchscreen
+5V_RUN
+3.3V_RUN
SB00001L800 QV8
LP2301ELT1G_SOT-23-3
+TS_PWR_R
+TS_PWR_QV8
FV1
1A_65V_T0603FF1000TM
+TS_PWR_DIS
QV100@
2N7002KW_SOT323-3
TS_PWR_EN#_R
TS_PWR_EN#
<58> 3.3V_TS_EN
<19> PCH_3.3V_TS_EN
3.3V_TS_EN_R
QV7
2N7002KW_SOT323-3
WebCAM
+3.3V_CAM
QZ1 SB00001L800
LP2301ELT1G_SOT-23-3
FZ3
1A_65V_T0603FF1000TM
<17> 3.3V_CAM_EN#
3.3V_CAM_EN#_R
DLM0NSN900HY2D_4P
<15> USB20_P11
<15> USB20_N11
Backlight POWER
+BL_PWR_SRC
FZ2
1A_65V_T0603FF1000TM
+17.8VB
QV1
AOTS21311C_TSOP6
SB00001SE00
BL_PWR_SRC_ON
QV2
2N7002KW_SOT323-3
<58> EN_INVPWR
LCDVDD POWER
+LCDVDD
JUMP@ PJP12
PAD-OPEN1x1m
+EDP_VDD
UV24
G524B1T11U_SOT23-5
+3.3V_ALW
DV3
BAT54CW_SOT323-3
<58> LCD_VCC_TEST_EN
<14> ENVDD_PCH
LCD_PWR_EN
LCD_PWR_EN_R

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Title: eDP CONN & Touch screen

Size: C | Document Number: LA-J282P | Rev: 1.0

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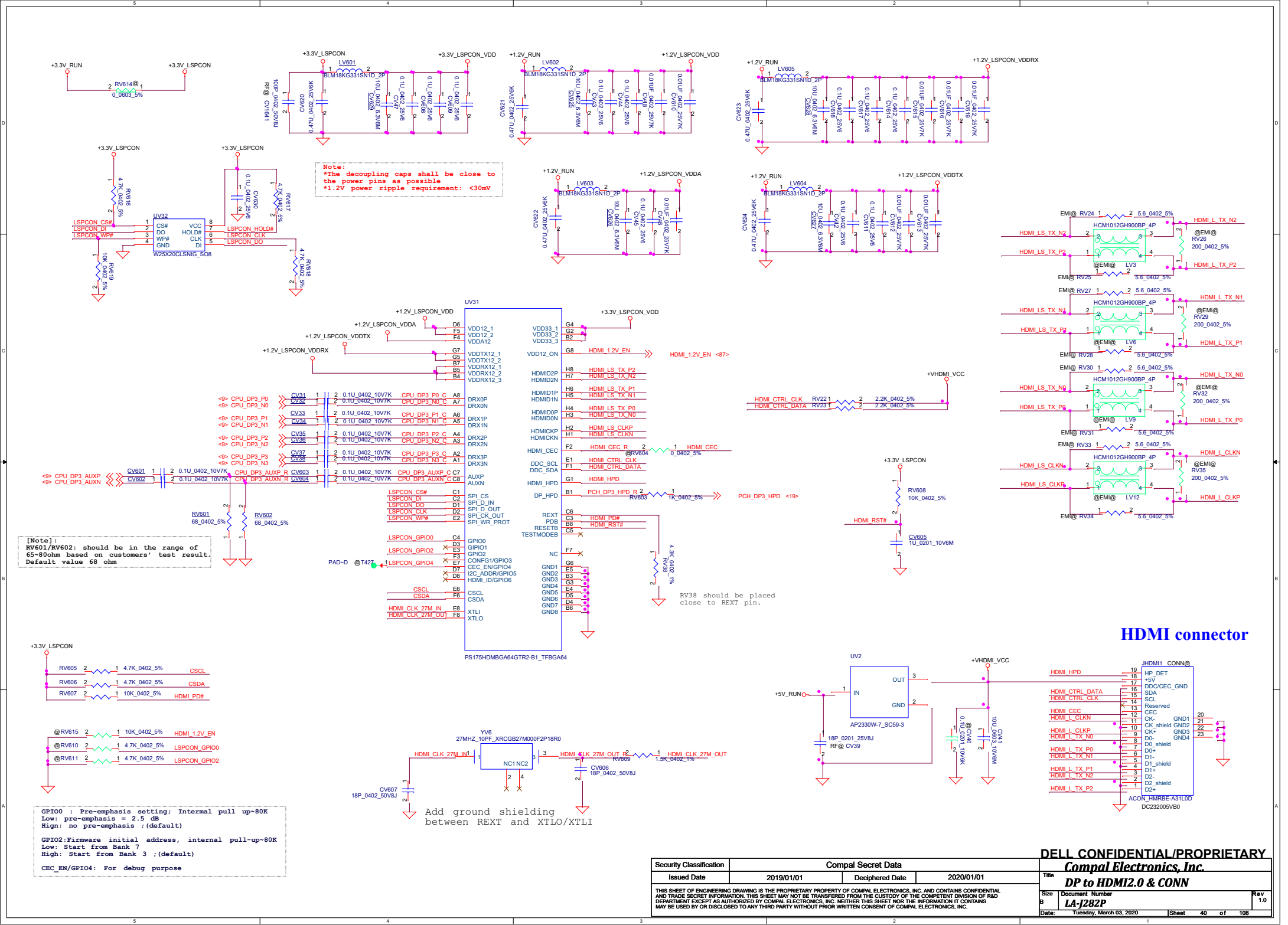
Reserve


+3.3V_RUN
+3.3V_LSPCON
RV614@ 0_0603_5%
+3.3V_LSPCON_VDD
LV601 BLM18KG331SN1D_2P
+1.2V_RUN
+1.2V_LSPCON_VDD
LV602 BLM18KG331SN1D_2P
+1.2V_LSPCON_VDDRX
LV605 BLM18KG331SN1D_2P
Note:
*The decoupling caps shall be close to the power pins as possible
*1.2V power ripple requirement: <30mV
+1.2V_LSPCON_VDDA
LV603 BLM18KG331SN1D_2P
+1.2V_LSPCON_VDDTX
LV604 BLM18KG331SN1D_2P
UV32
W25X20CLSNIG_SO8
LSPCON_CS#
LSPCON_DI
LSPCON_WP#
LSPCON_HOLD#
LSPCON_CLK
LSPCON_DO
UV31
PS175HDMBGA64GTR2-B1_TFBGA64
HDMI_1.2V_EN
HDMI_1.2V_EN <87>
PCH_DP3_HPD <19>
+VHDMI_VCC
HDMI_CTRL_CLK
HDMI_CTRL_DATA
HDMI_CEC
HDMI_PD#
HDMI_RST#
[Note]:
RV601/RV602: should be in the range of 65~80ohm based on customers' test result.
Default value 68 ohm
RV38 should be placed close to REXT pin.
HDMI connector
UV2
AP2330W-7_SC59-3
JHDMI1 CONN@
ACON_HMRBE-A31L0D
DC232005VB0
YV6
27MHZ_10PF_XRCGB27M000F2P18R0
Add ground shielding between REXT and XTLO/XTLI
GPIO0 : Pre-emphasis setting; Intermal pull up~80K
Low: pre-emphasis = 2.5 dB
High: no pre-emphasis ;(default)
GPIO2:Firmware initial address, internal pull-up~80K
Low: Start from Bank 7
High: Start from Bank 3 ;(default)
CEC_EN/GPIO4: For debug purpose
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
DP to HDMI2.0 & CONN
Security Classification
Compal Secret Data
Issued Date
2019/01/01
Deciphered Date
2020/01/01
Size
B
Document Number
LA-J282P
Rev
1.0
Date:
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Reserve

FOLLOW X11 NB MLK(0508) AR change to TR

Reference Titan Ridge SP 1.41 Datasheet

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6

connect to repeater PS8559

connect to repeater PS8559

For backdrive issue

CPU DDI1

CPU DDI2

Type-C

Place as close as possible to pins

NC for TR SP

Titan Redge SP

For vPRO docking support vHPD , should be used on PD & TR

Reference TR_DP_TI8I8_HOST_REF_DESIGN_R1V2

TBT RTD3 Support

TBT XTAL

EV brd main souce f i net uned

TBT Reset AND gate

reserve for shared ROM
Titan Ridge is held in reset till PD controller fetches code/boots first from ROM

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NC TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

IN	NC	NO
L	COM	X
H	X	COM

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2018/01/01

Compal Electronics, Inc.

Title: TBT-TR-SP(1/2)

Size: Custom | Document Number: LA-J282P | Rev: 1.0

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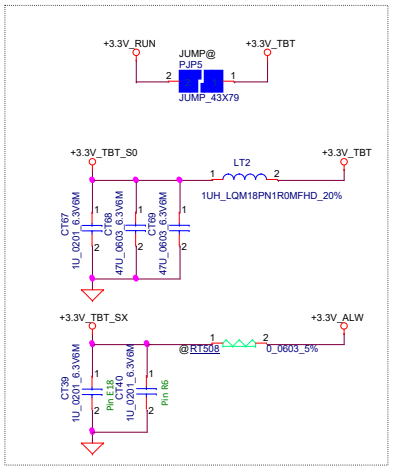
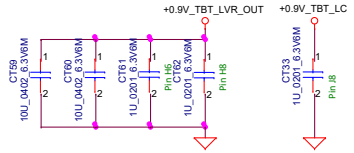
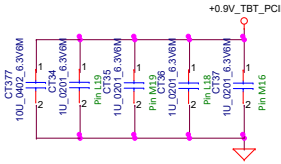
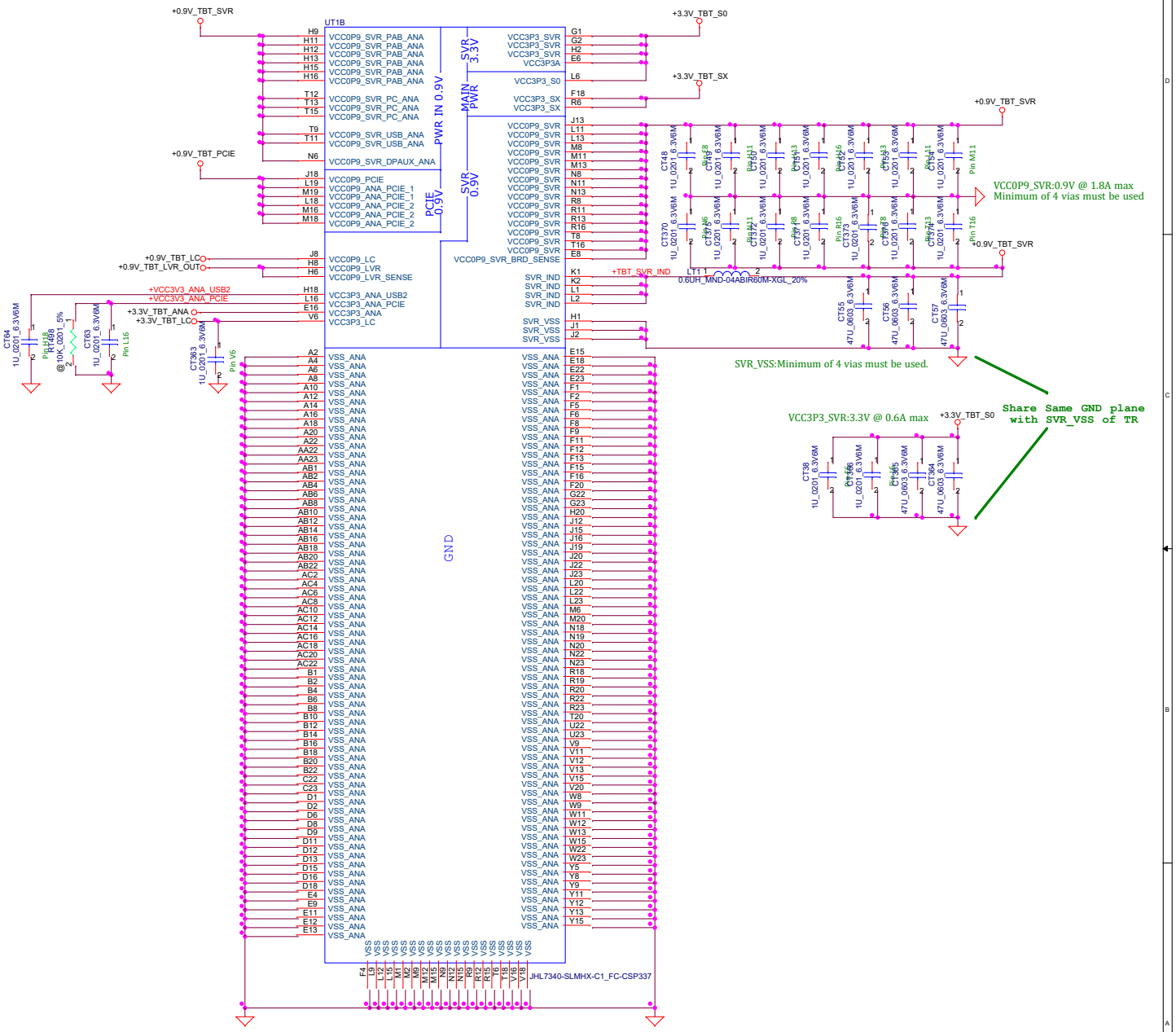
TBT Power circuit









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Issued Date	2017/01/01	Deciphered Date	2018/01/01

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Compal Electronics, Inc.

Title: *TBT-TR-SP(2/2)PWR,VSS*

Size: B | Document Number: *LA-J282P* | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 43 of 108

FOLLOW X11_NB_MLK(0508)_PD_65982DD_change_to_65987DD

For TR Config

PD GPIO define

GPIO	Pin #	Package Pin Name	TPS6598 (Dual Port)	TPS659875 (Single Port)	NOTES
			CML-TR	CML-TR	
0	16	GPIO0 (RESET2)	TR_RESET2	TR_RESET2	
1	17	GPIO1	DDM_MUX1_FLIP	DDM_MUX1_FLIP	GPIO for I2C/USB2.0 Mux control
2	18	GPIO2	DDM_MUX1_EN	DDM_MUX1_EN	
3	30	GPIO3 (HPD1)	TR_PA_HPD	TR_PA_HPD	HPD/SMBus_vPro
4	31	GPIO4 (HPD2)	TR_PB_HPD	-	
5	21	GPIO5	-	-	Raw I2C3/GPIO for external DP-USB3 Mux control
6	22	GPIO6	-	-	
7	23	GPIO7	-	-	
8	36	SPI_MISO (Boot Mode)	SPI_MISO	SPI_MISO	Backup SPI Flash
9	37	SPI_MOSI (GPIO9)	SPI_MOSI	SPI_MOSI	
10	38	SPI_CLK (GPIO10)	SPI_CLK	SPI_CLK	
11	39	SPI_SS (GPIO11)	SPI_SS	SPI_SS	
12	40	GPIO12 (SWD)	PROCHOT#	PROCHOT#	PD configs as OD for shared use
13	41	GPIO13 (SWD)	-	-	Reso for DDM_MUX2_USB_EN
14	42	GPIO 14 (PWM)	DDM_MUX2_FLIP	DDM_MUX2_FLIP	GPIO for I2C/USB2.0 Mux control
15	43	GPIO 15 (PWM)	DDM_MUX2_EN	DDM_MUX2_EN	
16	48	GPIO16 (PP_EXT1)	PP3_HVE_EN	PP3_HVE_EN	
17	49	GPIO17 (PP_EXT2)	PP4_HVE_EN	-	
18	50	GPIO18 (C1_USB_P)	-	-	Raw I2C3/GPIO for external DP-USB3 Mux control
19	53	GPIO19 (C1_USB_N)	-	-	
20	54	GPIO20 (C2_USB_P)	-	-	
21	55	GPIO21 (C2_USB_N)	-	-	Reso for DDM_MUX1_USB_EN
	24	C1_CC1	Port1 CC	Port1 CC	Port 1 CC
	26	C1_CC2	Port1 CC	Port1 CC	
	45	C2_CC1	Port2 CC	-	Port 2 CC
	47	C2_CC2	Port2 CC	-	
-	6	ADCIN1	Buspower Config	Buspower Config	
-	10	ADCIN2 (I2C Add)	Pull Dn (0x20, 0x24)	Pull Dn (0x20, 0x24)	I2C Address config:
-	27	I2C1_SCL (Master/Slave)	I2C1 for EC	I2C1 for EC	
-	28	I2C1_SDA (M/S)			
-	29	I2C1_IRQ (M/S)			
-	32	I2C2_SCL (Slave Only)	I2C2 for TR	I2C2 for TR	
-	33	I2C2_SDA (Slave)			
-	34	I2C2_IRQ (Slave)			

BUSPOWER Config

BP_NoWait value 0.7~0.78

R1 RT86 100K_0402_1%

PD_ADCIN1

R2 RT87 300K_0402_1%

Table 5. Boot Mode Pin Strapping

SPI_MISO	ADCIN1 DIV = R2/(R1+R2) (1) DIV MIN	DIV MAX	Dead Battery Mode	Device Configuration
1	0.00	0.10	BP_NoResponse	Safe Configuration
1	0.20	0.29	BP_WaitForSYS_Internal	Safe Configuration
1	0.30	0.39	BP_ICVInit_Internal	Infinite Wait
1	0.40	0.49	BP_WaitForSYS_External	Safe Configuration
1	0.50	0.59	BP_ICVInit_External	Infinite Wait
1	0.60	1.00	BP_NoWait	Safe Configuration
0	0.10	0.19	BP_NoResponse	Configuration 1
0	0.20	0.29	BP_NoWait	Configuration 2
0	0.30	0.39	BP_ICVInit_Internal	Infinite Wait
0	0.40	0.49	BP_NoWait	Configuration 3
0	0.50	0.59	BP_ICVInit_External	Infinite Wait
0	0.60	0.69	BP_NoWait	Configuration 4
0	0.70	0.79	BP_NoWait	Reserved
0	0.80	0.89	BP_NoResponse	Reserved
0	0.90	1.00	BP_NoWait	Configuration 5

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Need CHECK

I2C Address Divider:010b

R1 RT88 100K_0402_1%

PD_ADCIN2

R2 RT89 100K_0402_1%

Table 4. I2C Address Selection

DIV = R2/(R1+R2) (1) DIV_min	DIV_max	I2C UNIQUE ADDRESS [3:1] I2C ADDR_DECODE
Short ADCIN2 to GND		000b
0.20	0.39	001b
0.40	0.59	010b
Short ADCIN2 to LDO_3V3		011b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

X10 +3.3V_VDD_PIC_PDA change connect to +3.3V_ALW

Table 3. Design Parameters (continued)

PARAMETER			VALUE
DC Boost	22 kΩ - 47 kΩ	Do Not Install (DNI)	40 mV Low DC Boost
	DNI	DNI	60 mV Mid DC Boost
	DNI	22 kΩ - 47 kΩ	80 mV High DC Boost

DC_BOOST

RDC2 47K_0402_5%

PDC_BOOST

RDC1 47K_0402_5%

*If pop UT10, RT14 need to pop.

UT10 layout placement

RSTN internal 500K ohm PU.

AC_BOOST

Table 1. Enable and Disable Function Table

ENA	ENB	INA	INB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Enabled	Hi-Z	Hi-Z	Enabled	Hi-Z	Enabled
1	0	Enabled	Hi-Z	Enabled	Hi-Z	Enabled	Hi-Z
1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

Table 6. Complete Function Table

SAI	SBI	SA0	SB0	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE	
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux	
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux	USB only on SW_TBT_A_USB20_P1/N1
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux	USB on SW_TBT_A_USB20_P1/N1
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux	DDM on SW_TBT_A_USB20_P2/N2
0	1	0	0	INB	—	—	INA		
0	1	0	1	INB	—	—	INA		
0	1	1	0	—	INB	INB	—		
0	1	1	1	—	INB	—	INB		
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration	
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration	
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration	
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration	
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux	
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux, 1-channel 1:4 mux	USB only on SW_TBT_A_USB20_P2/N2
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux, 1-channel 1:4 mux	USB on SW_TBT_A_USB20_P2/N2
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux, 1-channel 1:4 mux	DDM on SW_TBT_A_USB20_P1/N1

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2018/01/01

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Compal Electronics, Inc.

[Type C]PD Controller TI

Size C | Document Number LA-J282P | Rev 1.0

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2018/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.		
Title: Reserve Type-C_D Power		
Size: B	Document Number: LA-J282P	Rev: 1.0
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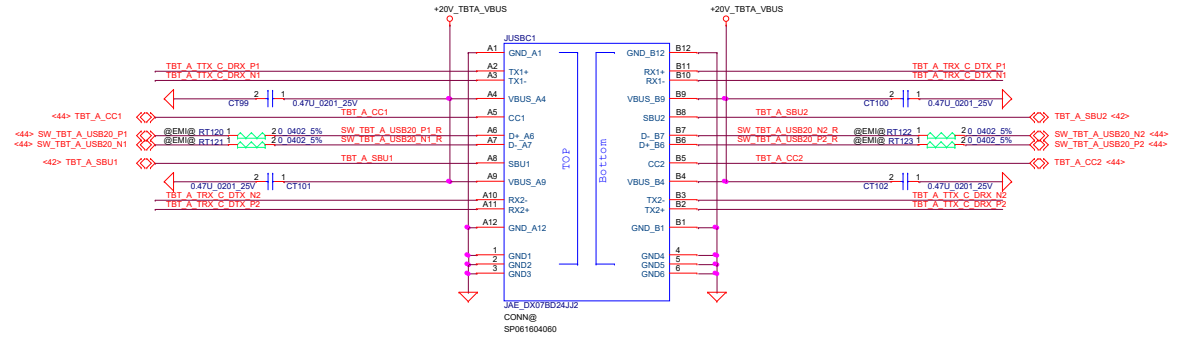
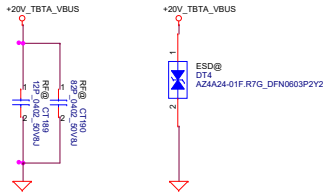
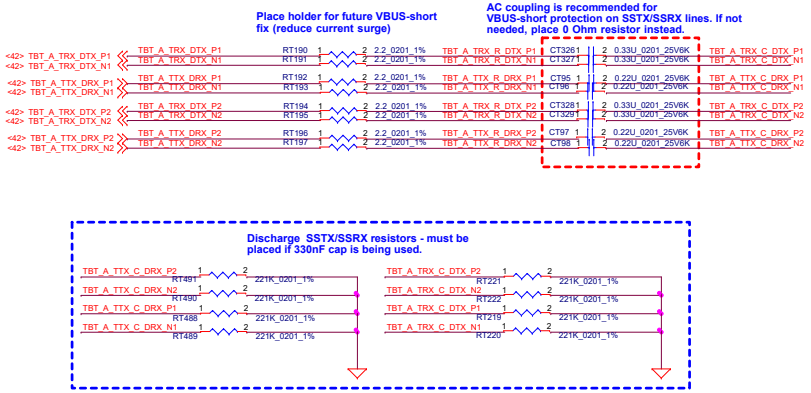
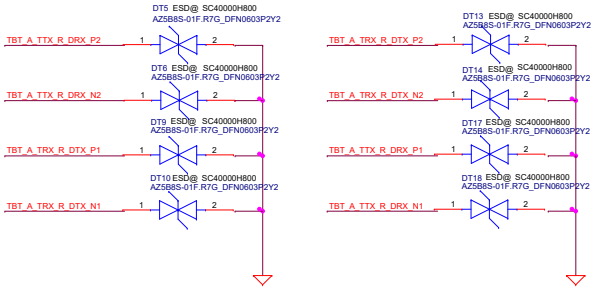
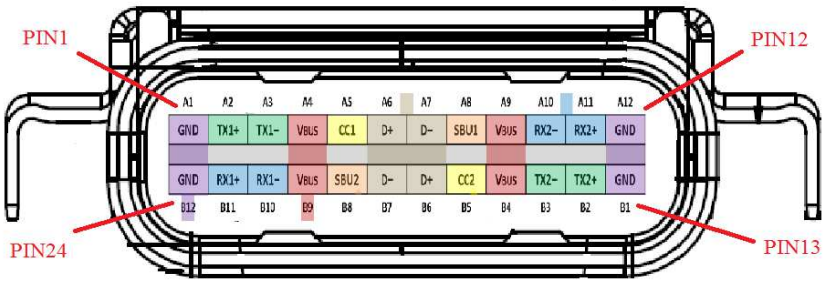


to be change to LTCX0097NBL
DX07BD24JJ3R1100









Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size: C | Document Number: LA-J282P | Rev: 1.0

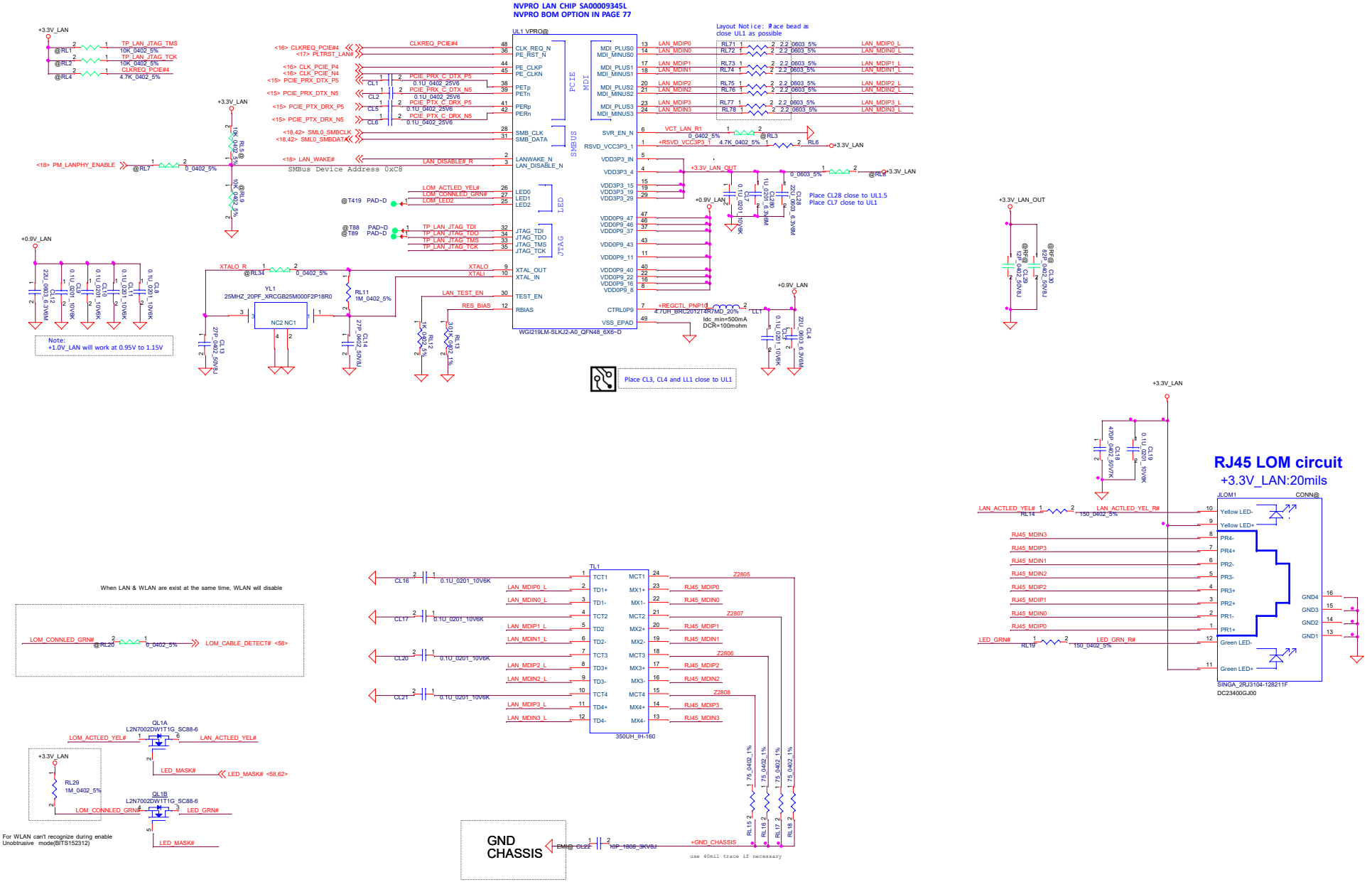
Date: Tuesday, March 03, 2020 | Sheet 46 of 108

Reserve

Reserve

Reserve

Reserve



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Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Compal Electronics, Inc.	
Title	LAN Jacksonville & RJ45
Size	C
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STATE #	CONFIG_0 (PIN21)	CONFIG_1 (PIN69)	CONFIG_2 (PIN75)	CONFIG_3 (PIN1)	Module Type	m3042_PCIE#_SATA
0	GND	GND (PEDET_PD)	GND	GND (device_PD)	SSD-SATA	High
1	GND	HIGH (PEDET_NC)	GND	GND	SSD-PCIE(2 lane)	Low
8	GND (device_PD)	GND (device_PD)	HIGH (device_NC)	HIGH (device_NC)	WWAN	Low
	GND (device_PD)	GND (device_PD)	GND (device_PD)	HIGH (device_NC)	WWAN	Low
15	EC (MB_PU)	EC (MB_PU)	EC (MB_PU)	EC (MB_PU)	NA	Low

NGFF slot B Key B

NGFF slot E Key E

SUPPORT WWAN 7360 CARD

SUPPORT WWAN 7360 CARD

Reserve eSIM (7560 card Intel)

SIM Card Push-Push

S	SW
1	B2 to A
0	B1 to A

C	B	A	Y
0	0	0	0
0	1	0	1
1	0	0	0
1	1	0	0

Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

main PERICOM SA00006EJ00
S IC P13PCIE32122BEX TQFN 20P MUX SW
2nd TI SA00009A100
S IC HD3SS32120RKSR VQFN 20P MUX/DEMUX SW

WLAN

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Issued Date	2019/01/01	Deciphered Date 2020/01/01

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Compal Electronics, Inc.

Title: NGFF Card

Size: D | Document Number: LA-I282P | Rev: 1.0

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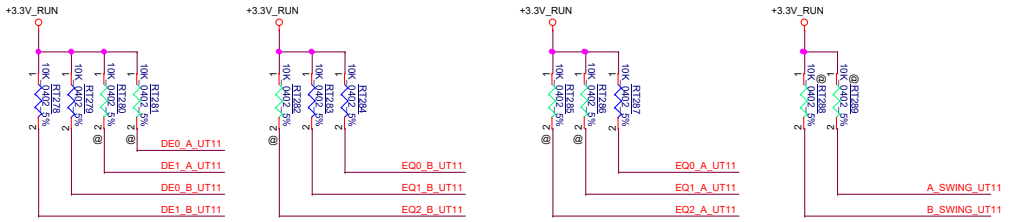
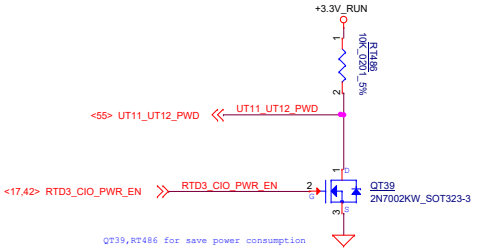
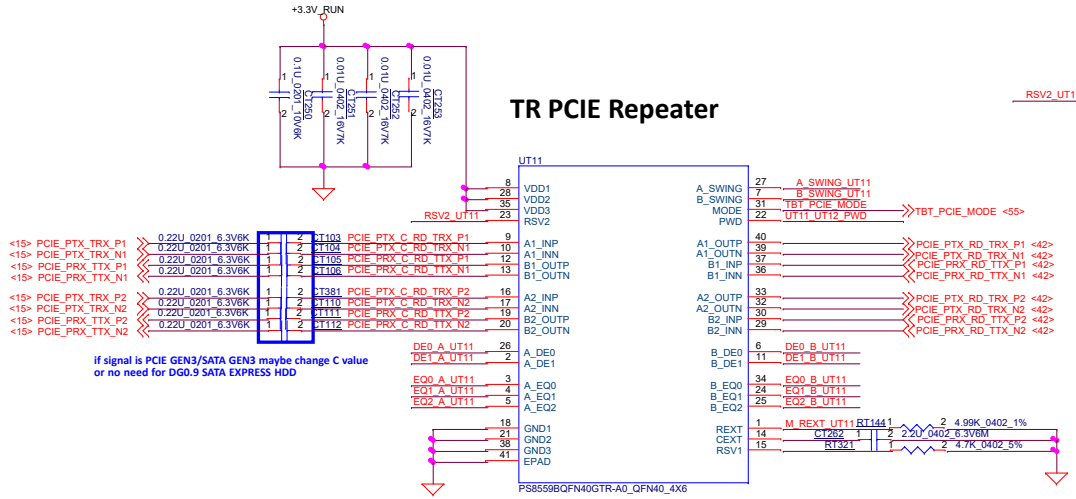
Reserve





MODE	I	SATA mode or PCIe mode selection. Internally pulled down at ~150KΩ. Mode= L: SATA Mode H: PCIe Mode
A_DE1, A_DE0 B_DE1, B_DE0	I	Programmable output de-emphasis level setting for channel Ax/Bx. Internally pulled down at ~150KΩ.
A_SWING, B_SWING	I	Adjust Ax/Bx channel output swing. Internally pulled down at ~150KΩ. A_SWING/B_SWING= L: default swing H: Increase 10%

DE<1:0>	DE level
00 (default)	-3.5dB
01	-2dB
10	-6dB
11	-7.5dB



Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

A_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

B_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

PWD	Funtion
0	Normal mode(Default)
1	Chip power down

M2_SLOT4_PEDET	DEVICE interface
0	SATA
1 (3.3V)	PCIE

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.	
Title	SATA/PCIE REPEATER for TR
Size	B
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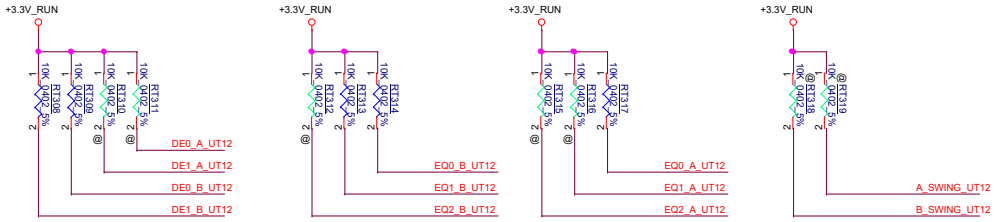


Programmable output de-emphasis level setting for channel A .
A_DE0 and A_DE1: internally pulled down at ~150K

A_DE<1:0>	DE Level
00(defult)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Internally pulled down at ~150KΩ

A_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%

B_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%

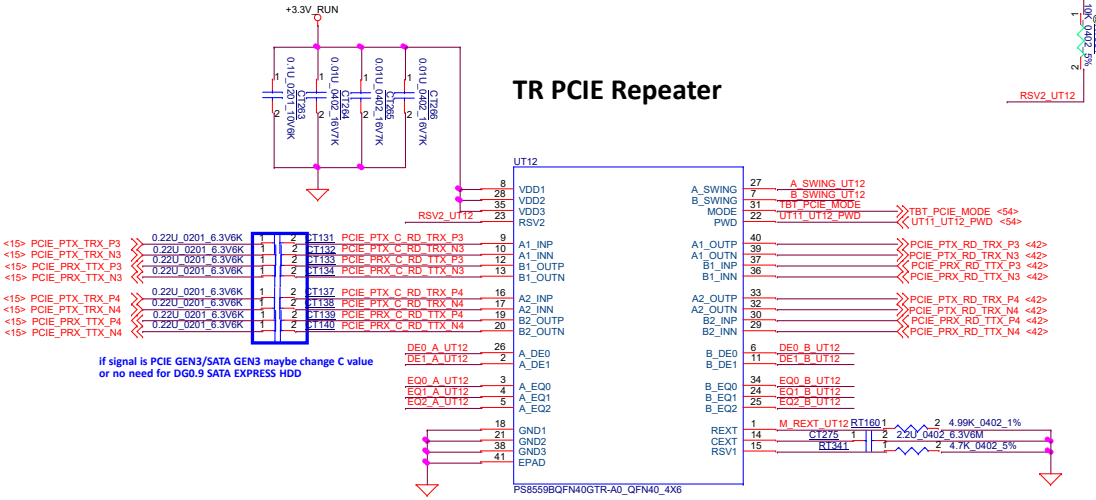
Programmable output de-emphasis level setting for channel B .
B_DE0 and B_DE1: internally pulled down at ~150K

B_DE<1:0>	DE Level
00(defult)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB

Internally pulled down at ~150KΩ

MODE	Operation Mode
0(defult)	SATA
1	PCIe

TR PCIE Repeater



if signal is PCIE GEN3/SATA GEN3 maybe change C value
or no need for DG0.9 SATA EXPRESS HDD

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

A_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

B_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

PWD	Funtion
0	Normal mode(Default)
1	Chip power down

M2_SLOT4_PEDET	DEVICE interface
0	SATA
1 (3.3V)	PCIE

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: SATA/PCIE REPEATER for TR

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

SM01000PL00

JSPK1

CVILU_CI4204M2HRJ-NH

CONN@

SP020012X10

Close to UA1

Close to UA1 pin5

place close to UA1 pin3

Place closely to Pin 12.

Add for solve pop noise and detect issue

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

place at AGND and DGND plane

PAD-OPEN1x2m

2.5A

PAD-OPEN1x1m

500mA

CA29,CA79,CA49,CA80 downsize,Vendor suggest 1u_0603x1 to 1u_0201x2
only use SE00000YB00 (CL03A105KQ3CSNC_JDK063ABJ105KP-F) (0201 size 1uF 6.3V X5R)

Place CA29,CA79 close to Codec

CA77, CA78 close to Codec

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Add this Filter to avoid other components/chips be influenced

Universal Jack

SINGA_2SJ3095-190111F

DC230001600

NORMAL OPEN

If EMI changes value, need to inform vendor first .

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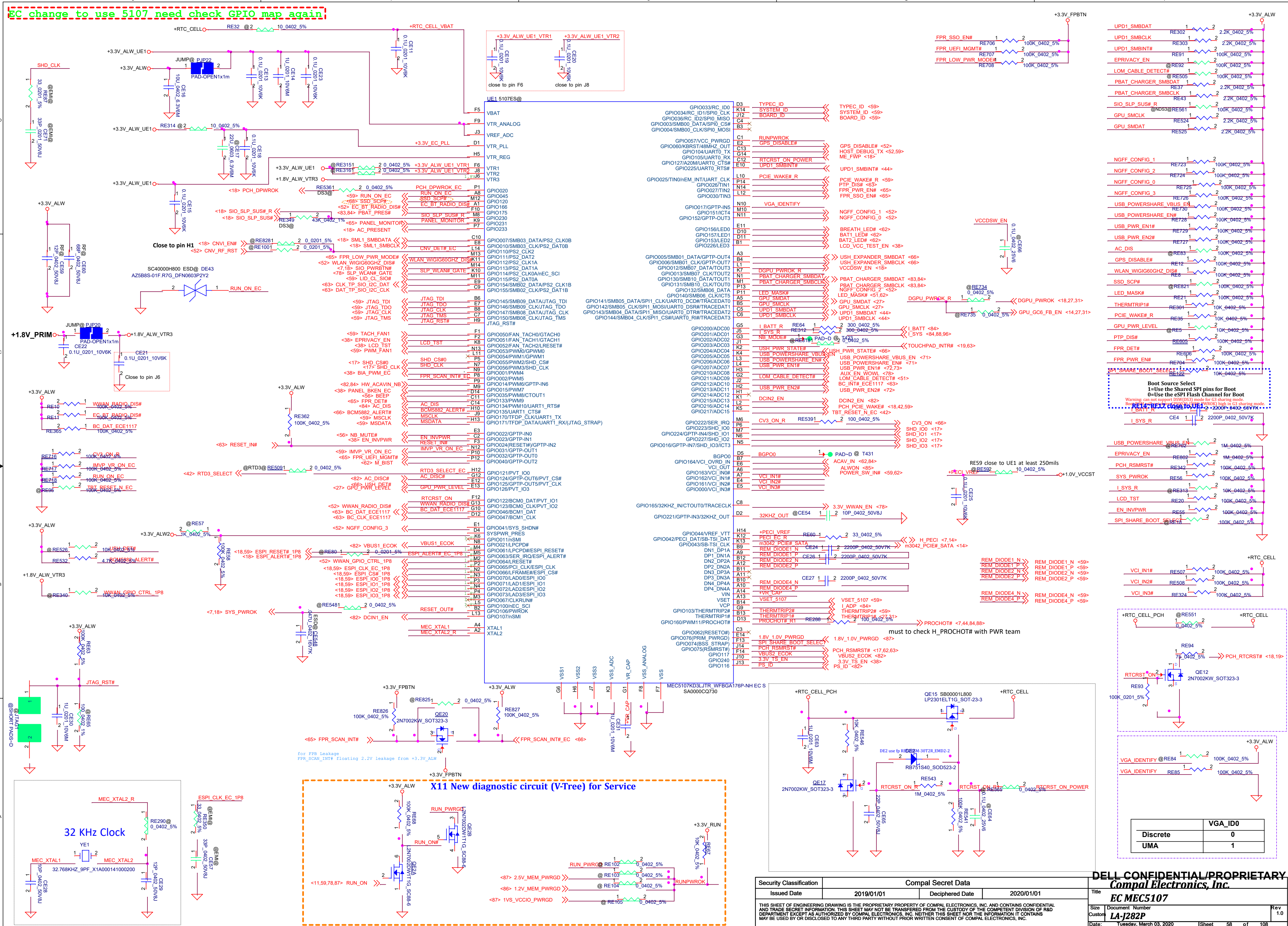
Compal Electronics, Inc.	
Title: Codec ALC3204	
Size:	Document Number: LA-J282P
Rev: 1.0	
Date: Tuesday, March 03, 2020	Sheet 56 of 106

Reserve



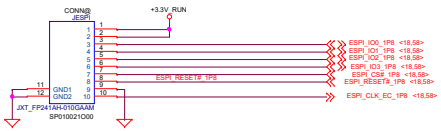
Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

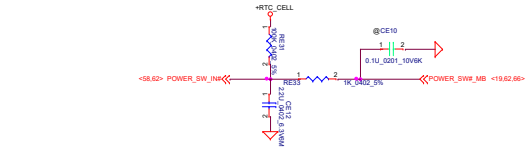
Compal Electronics, Inc.

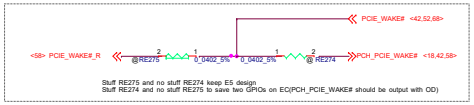
Title: EC MEC5107

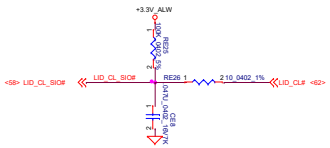
Size: Custom | Document Number: LA-J282P | Rev: 1.0

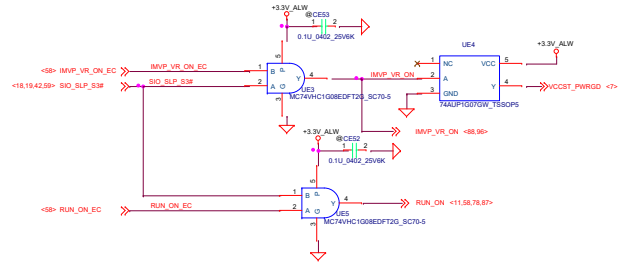
For BH_MLK DSC

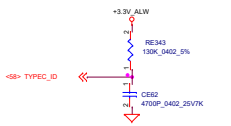






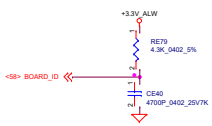






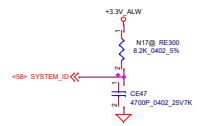
RE343	CE62	REV
240K	4700p	Single Port ACE w/o TR
* 130K	4700p	Single Port ACE w/TR
62K	4700p	Dual Port ACE w/o TR
33K	4700p	Dual Port ACE w/TR
8.2K	4700p	Dual Port ACE (w/TR +w/o TR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise ti meis measuredfro m5 %~68 %



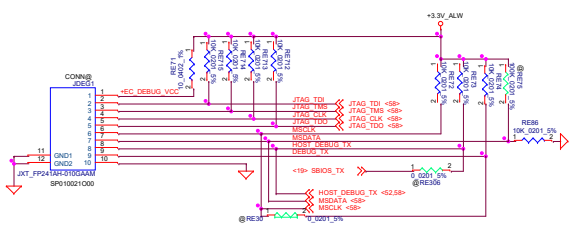
RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

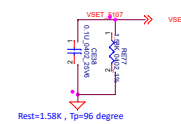
BOARD_ID rise ti meis measuredfro m5 %~68 %

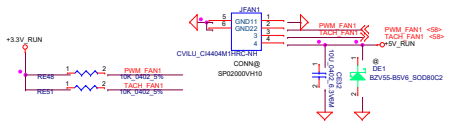


RE300	CE47	PANEL SIZE
240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
33K	4700p	14"
* 8.2K	4700p	BR15 H
4.3K	4700p	17"
* 2K	4700p	BR15 P
1K	4700p	

PANEL_ID rise ti meis measuredfro m5 %~68 %

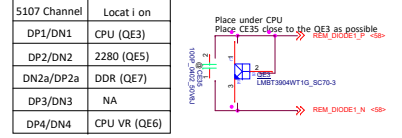


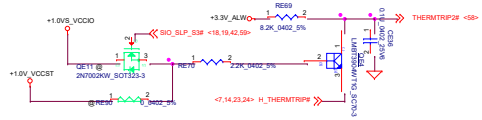


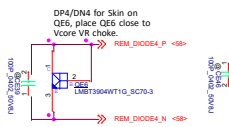


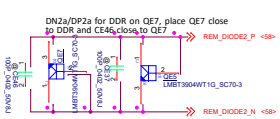
Thermal diode mapping

5107 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	2280 (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)









DP2/DN2 for 2280 on QE5, place QE5 close to JNGFF3 and CE37 close to QE5

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Title: MEC5107 SUPPORT

Size: Custom | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 59 of 108

Reserve

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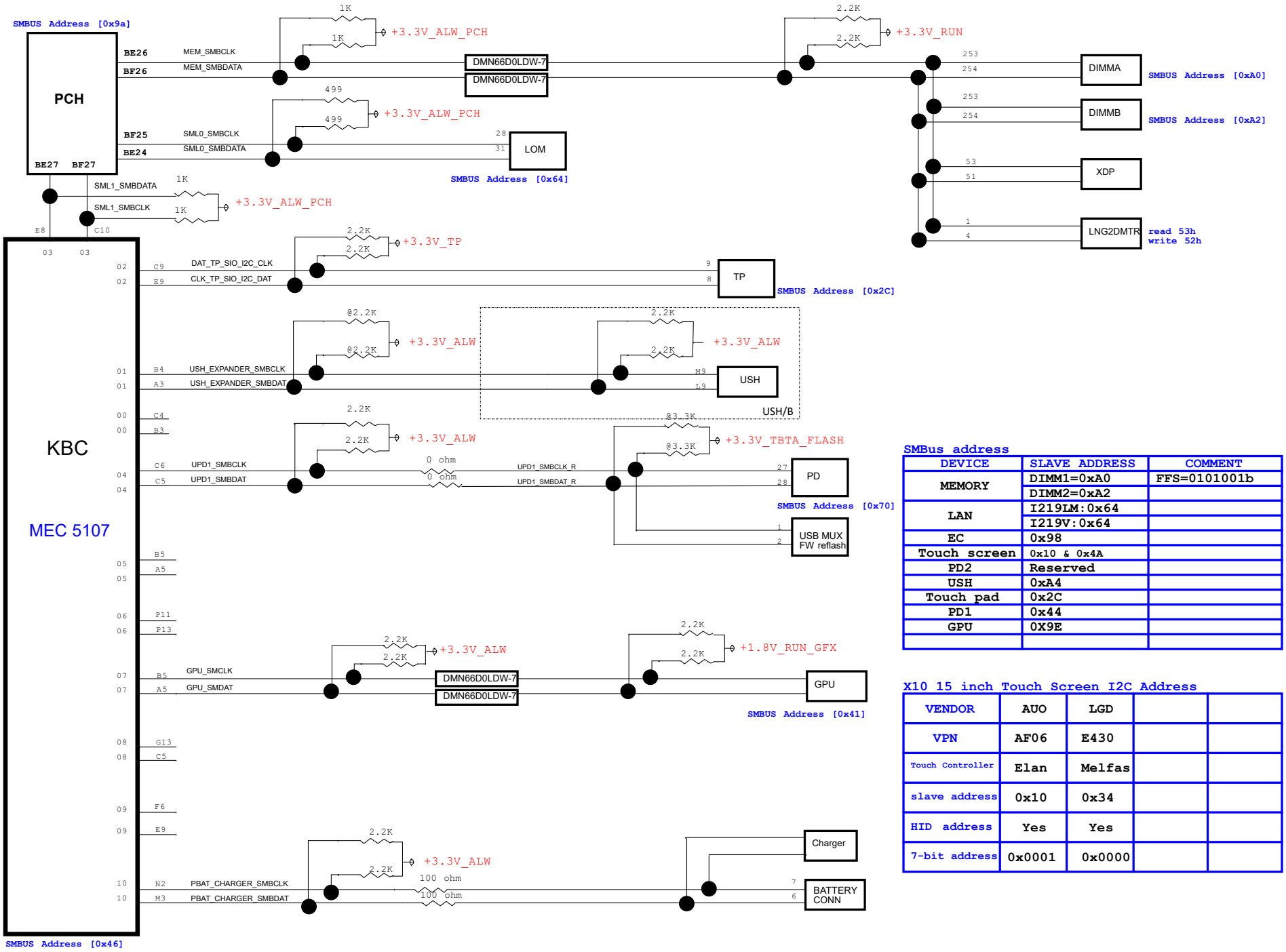
Title: Secure & Reset IC

Size | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 60 of 108



SMBus address

DEVICE	SLAVE ADDRESS	COMMENT
MEMORY	DIMM1=0xA0	FFS=0101001b
	DIMM2=0xA2	
LAN	I219LM:0x64	
	I219V:0x64	
EC	0x98	
Touch screen	0x10 & 0x4A	
PD2	Reserved	
USH	0xA4	
Touch pad	0x2C	
PD1	0x44	
GPU	0X9E	

X10 15 inch Touch Screen I2C Address

VENDOR	AUO	LGD		
VPN	AF06	E430		
Touch Controller	Elan	Melfas		
slave address	0x10	0x34		
HID address	Yes	Yes		
7-bit address	0x0001	0x0000		

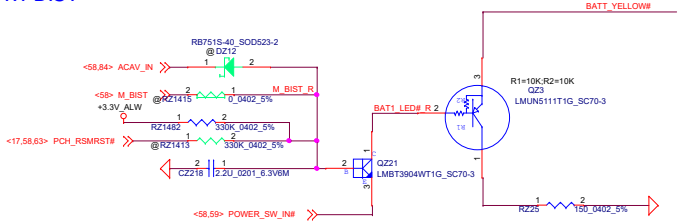
Compal Electronics, Inc.

Title: SMbus Block Diagram

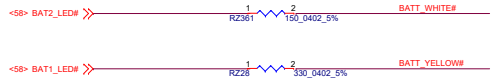
Size: B | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 61 of 108

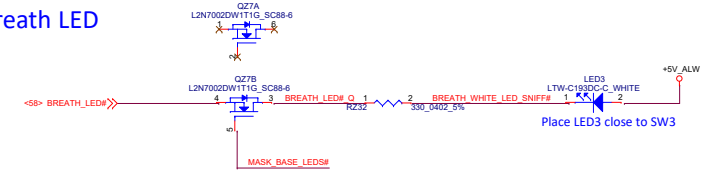
M BIST

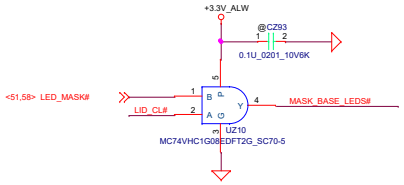


Bat t ery LED

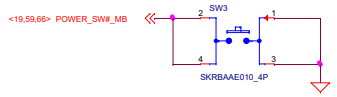


Breath LED



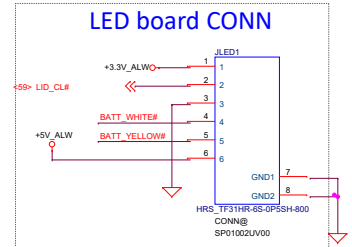


POWER & INSTANT ON SWITCH



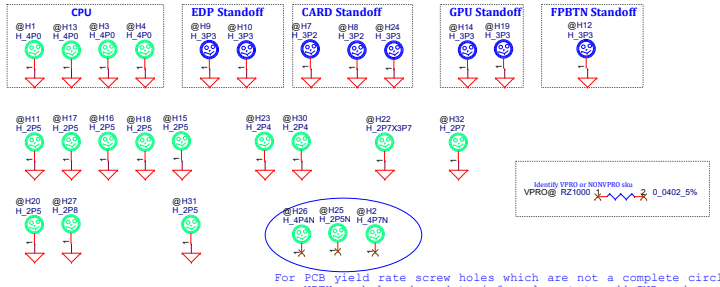
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

LED board CONN

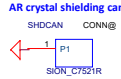


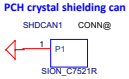
Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D
@FD5 FIDUCIAL MARK~D
@FD6 FIDUCIAL MARK~D
@FD7 FIDUCIAL MARK~D
@FD8 FIDUCIAL MARK~D



For PCB yield rate screw holes which are not a complete circle located at PCB edge use NPTH symbol and need to inform layout to add GND pad





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Compal Electronics, Inc.			
Title: PAD, LED			
Size: C	Document Number: LA-J282P		Rev: 1.0
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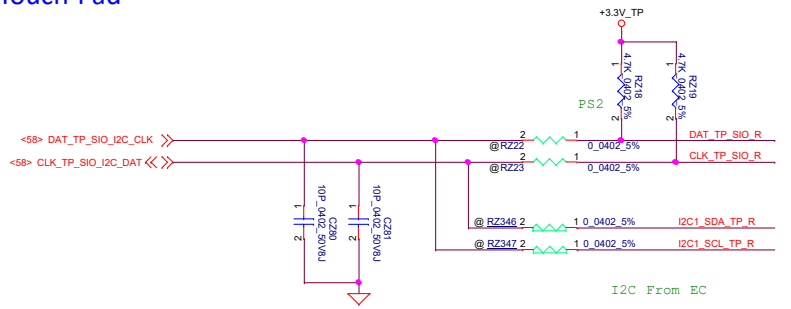
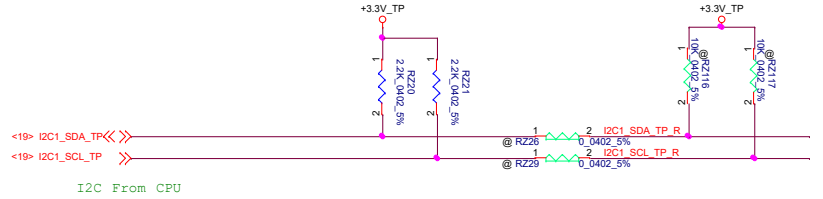
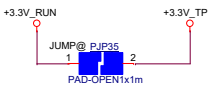
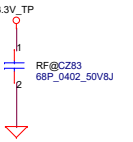
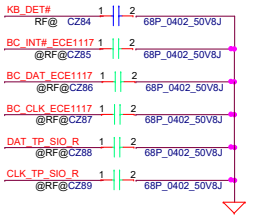
Touch Pad



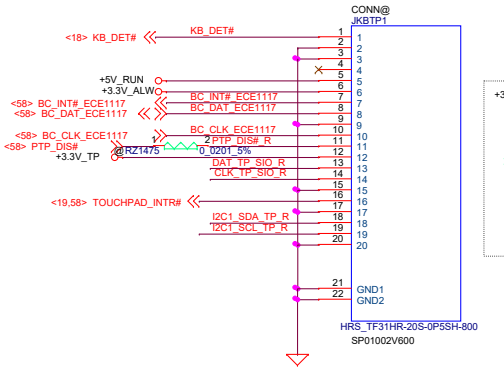


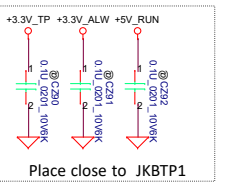




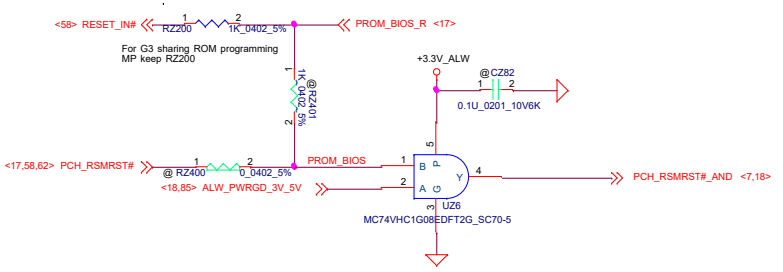


Keyboard





RSMRST circuit



Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Compal Electronics, Inc.

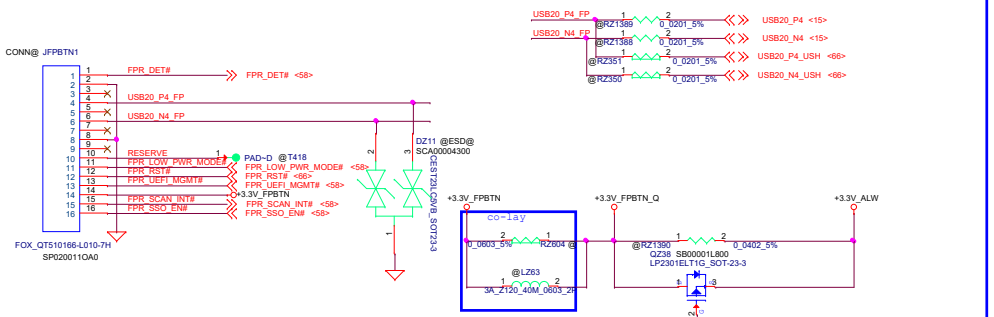
Title: ***Keyboard***

Size	Document Number	Rev
B	*LA-J282P*	1.0

Date: Tuesday, March 03, 2020 | Sheet 63 of 108

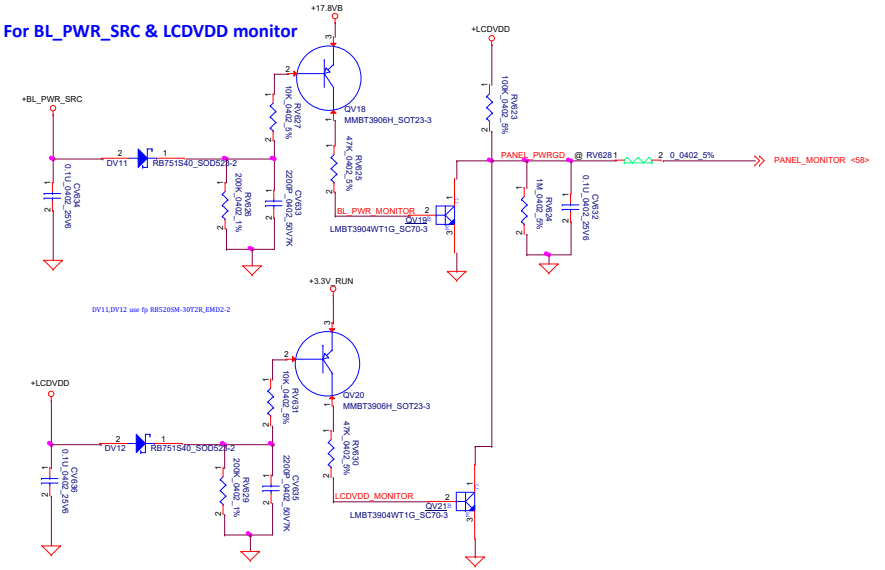
Reserve

FP in PWR BUTTON connector



Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_SSO_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR DET(GND)	16

For BL_PWR_SRC & LCDVDD monitor

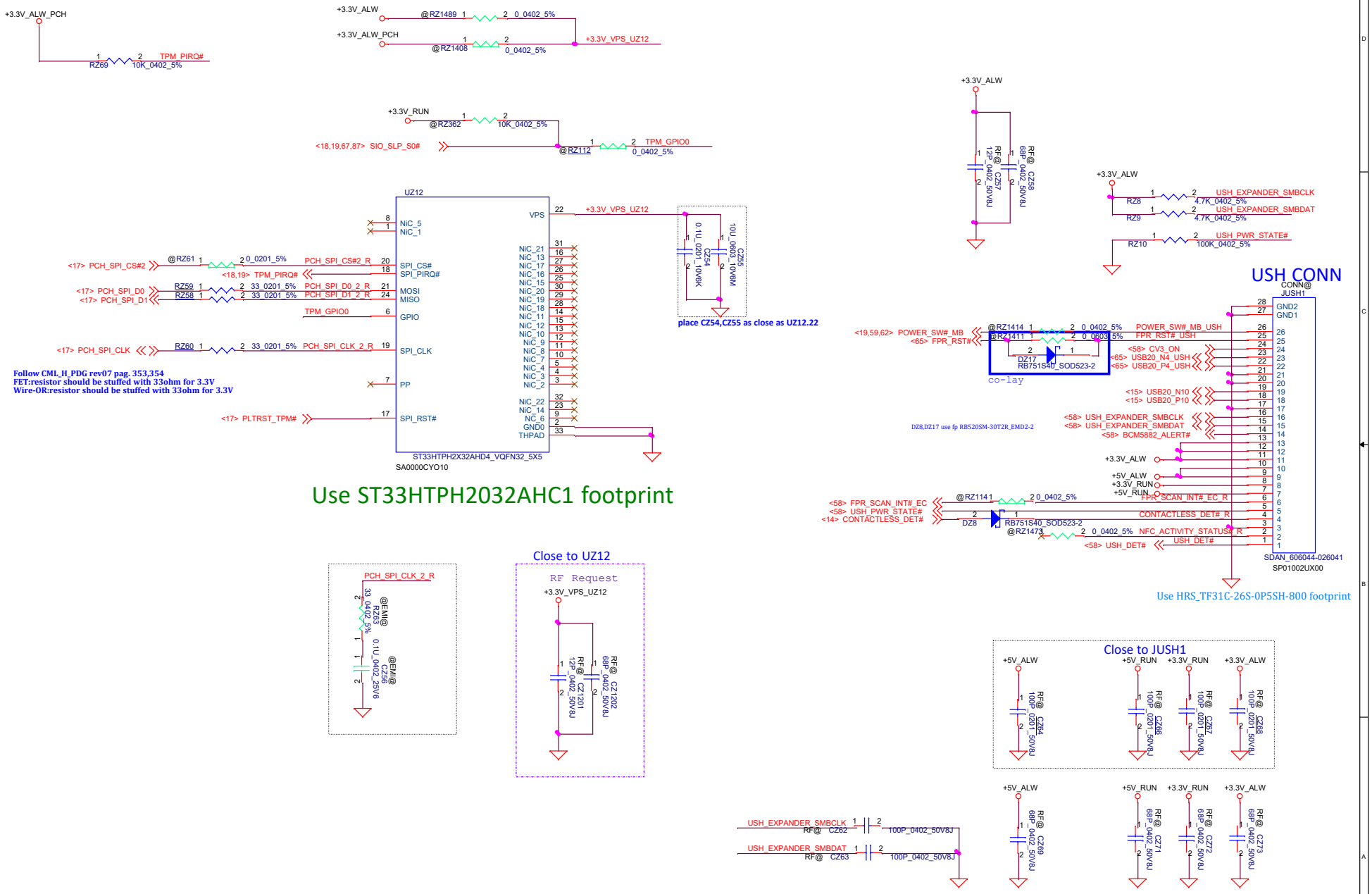


Compal Electronics, Inc.

Title: FP in PWRBTN

Size: | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 65 of 108



Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

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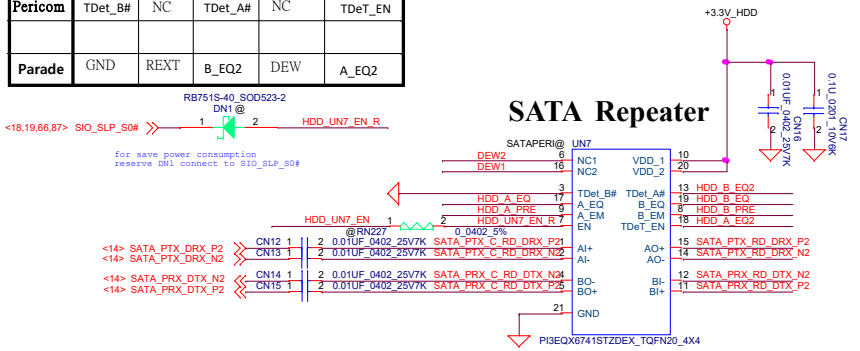
Compal Electronics, Inc.

Title	USH & TPM		
Size: Custom	Document Number: LA-J282P		Rev: 1.0
Date: Tuesday, March 03, 2020	Sheet 66 of 108		

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater

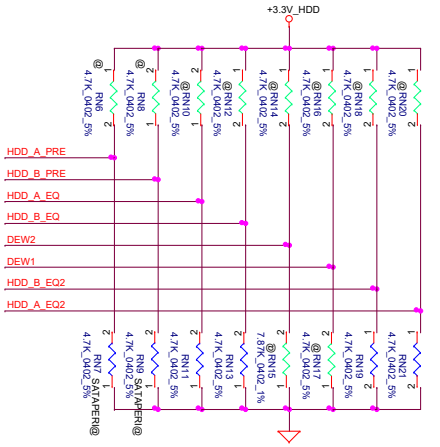


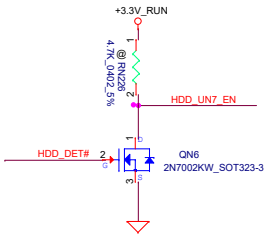
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8	
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)	*main
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)	*2nd

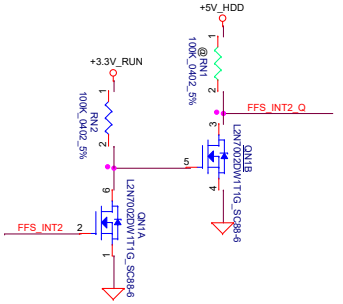
			A_EQ	B_EQ		A_EM	B_EM
2nd	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB

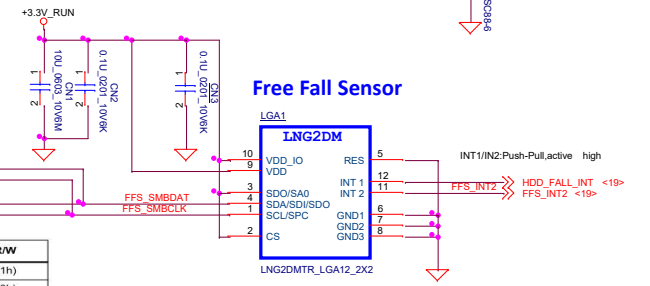
		EQ2	EQ1	A_EQ	B_EQ		A_EM	B_EM
Main	Parade	(M = VDD/2)						
		0	M	2.4dB	2.4dB			
		0	0	7.4dB	7.4dB			
		0	1	14.4dB	14.4dB	0	0dB	0dB
		M	M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M	0	9.4dB	9.4dB	1	-6dB	-6dB
		M	1	13.3dB	13.3dB			
		1	M	6.2dB	6.2dB			
		1	0	11.2dB	11.2dB			
		1	1	5dB	5dB			

* red color is current setting

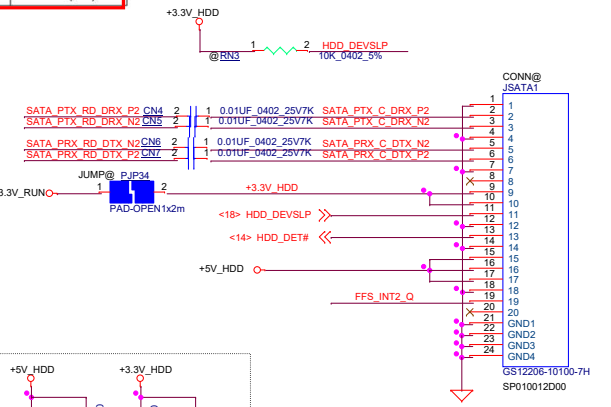


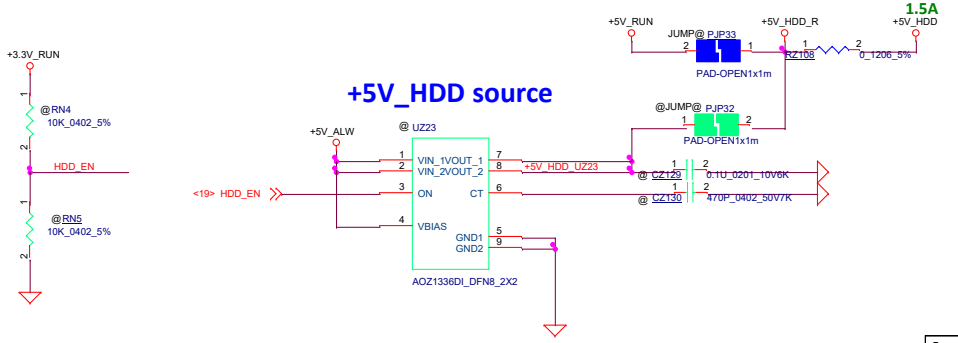


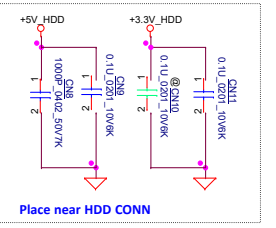




Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)







Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: HDD CONN

Size	Document Number	Rev
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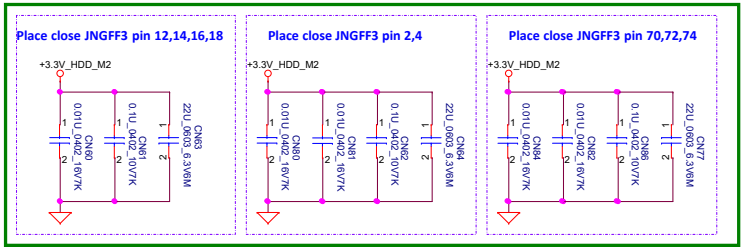
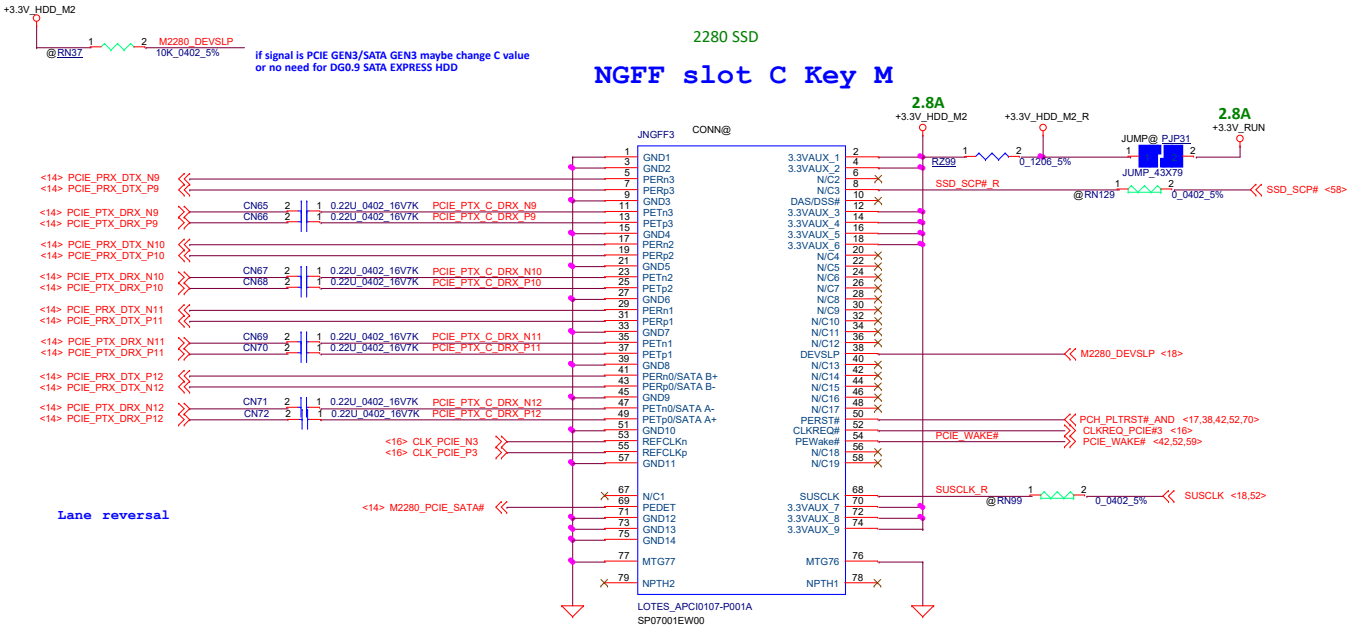
Add Power Decoupling for support Intel Teton Glacier





Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.			
Title: M2 2280 Socket			
Size: B	Document Number: LA-J282P		Rev: 1.0
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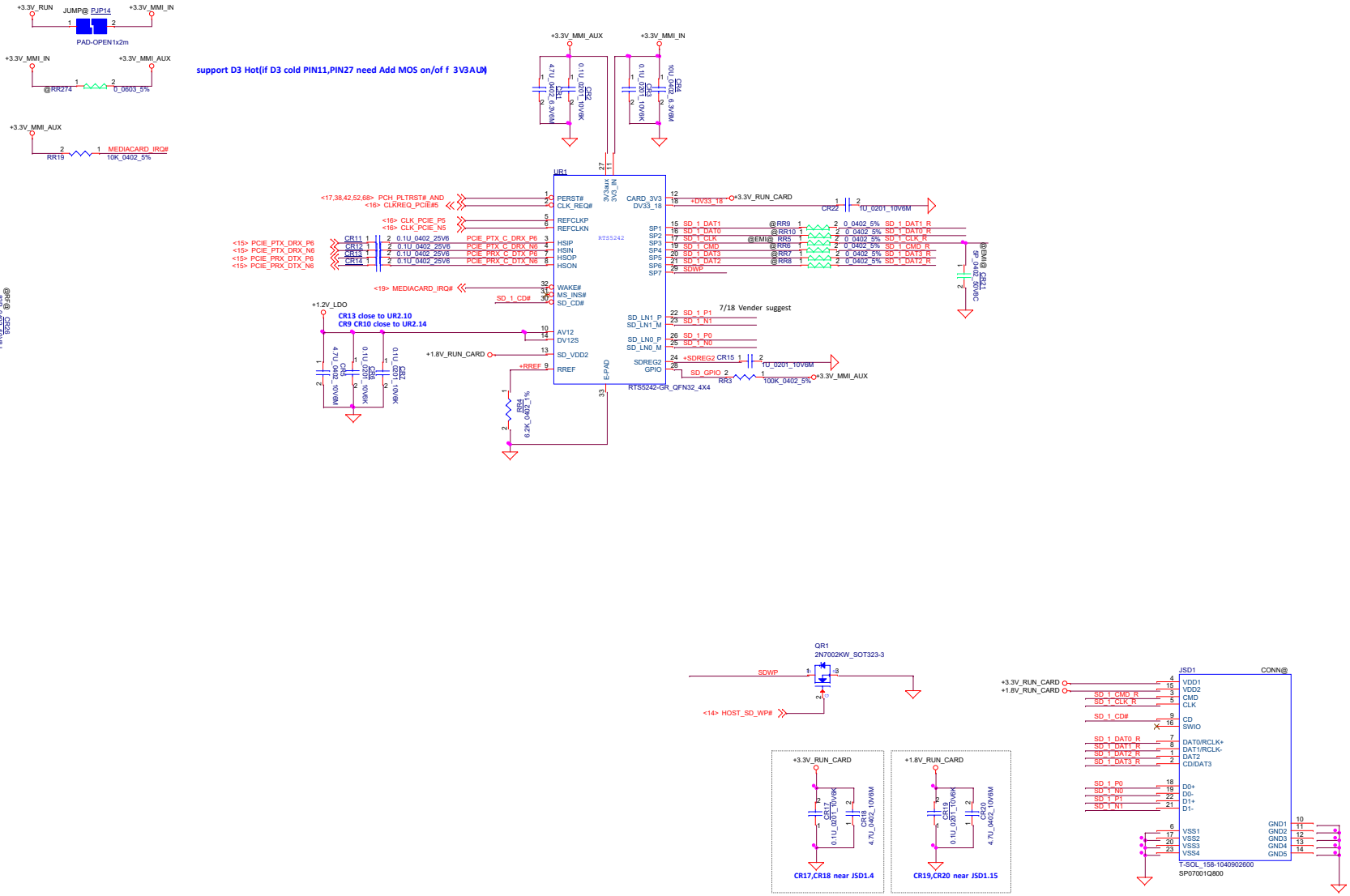
Reserve

For PCIE Interface



Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: Card Reader

Size	Document Number	Rev
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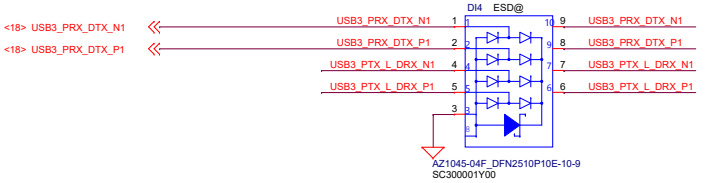
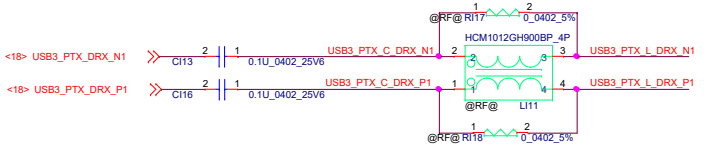
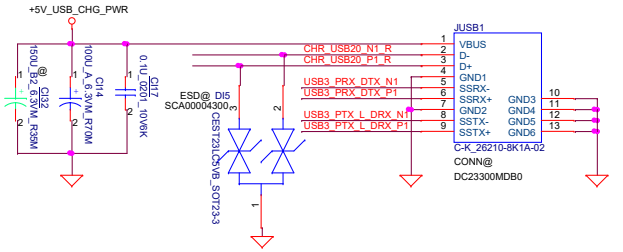
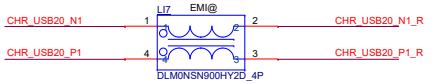
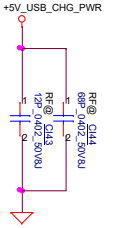
For PWR SW + Charger combine IC

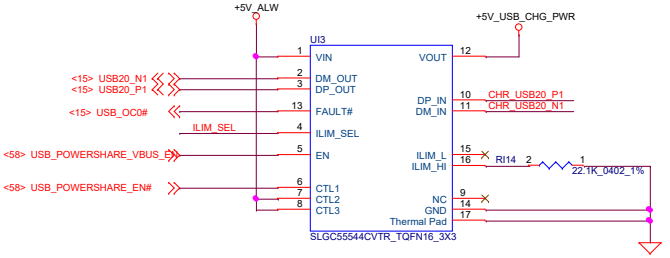


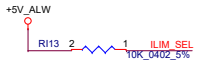


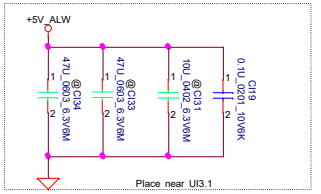












Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

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Compal Electronics, Inc.

Title	USB SW	
Size B	Document Number LA-J282P	Rev 1.0
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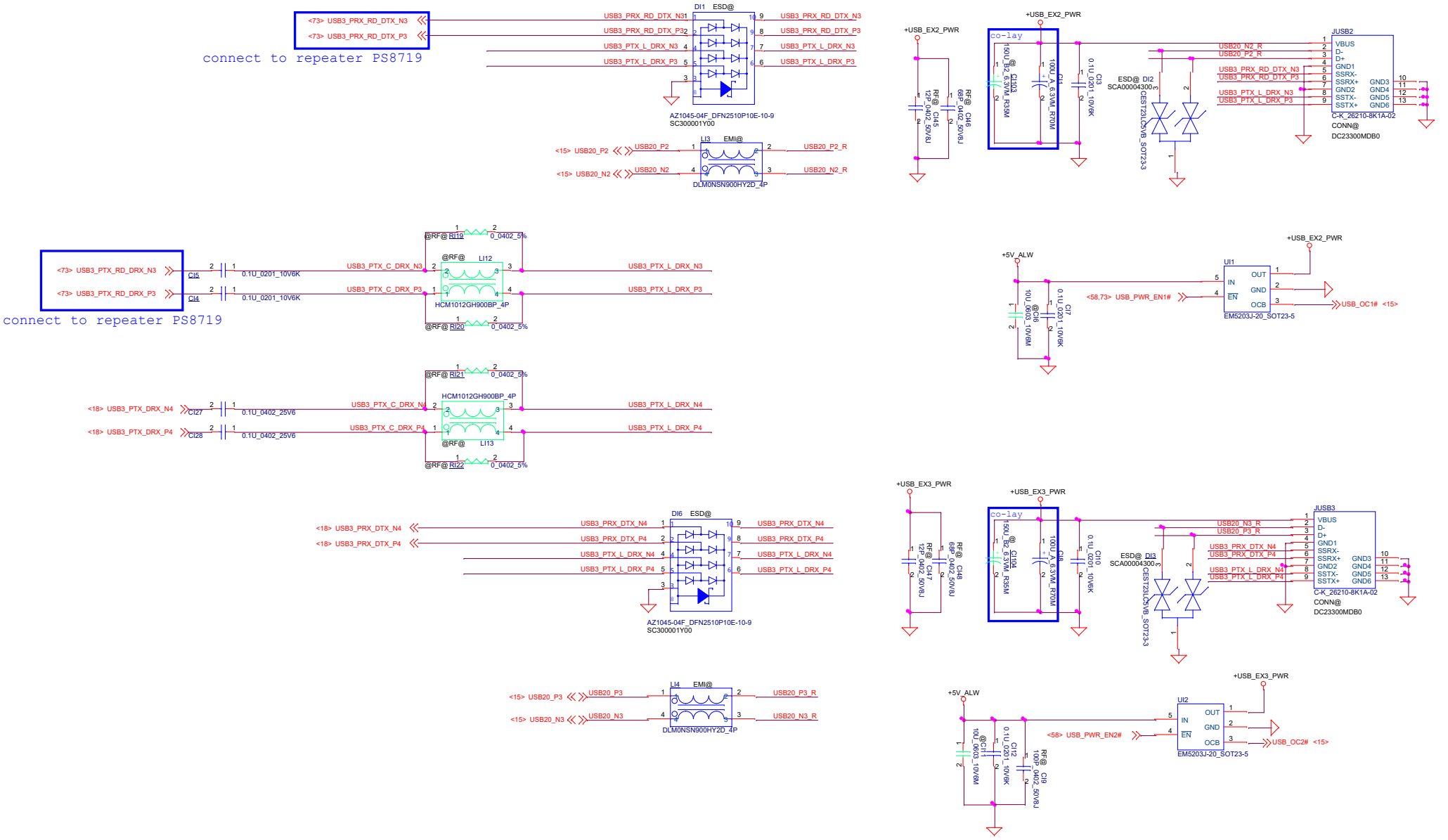


Compal Electronics, Inc.

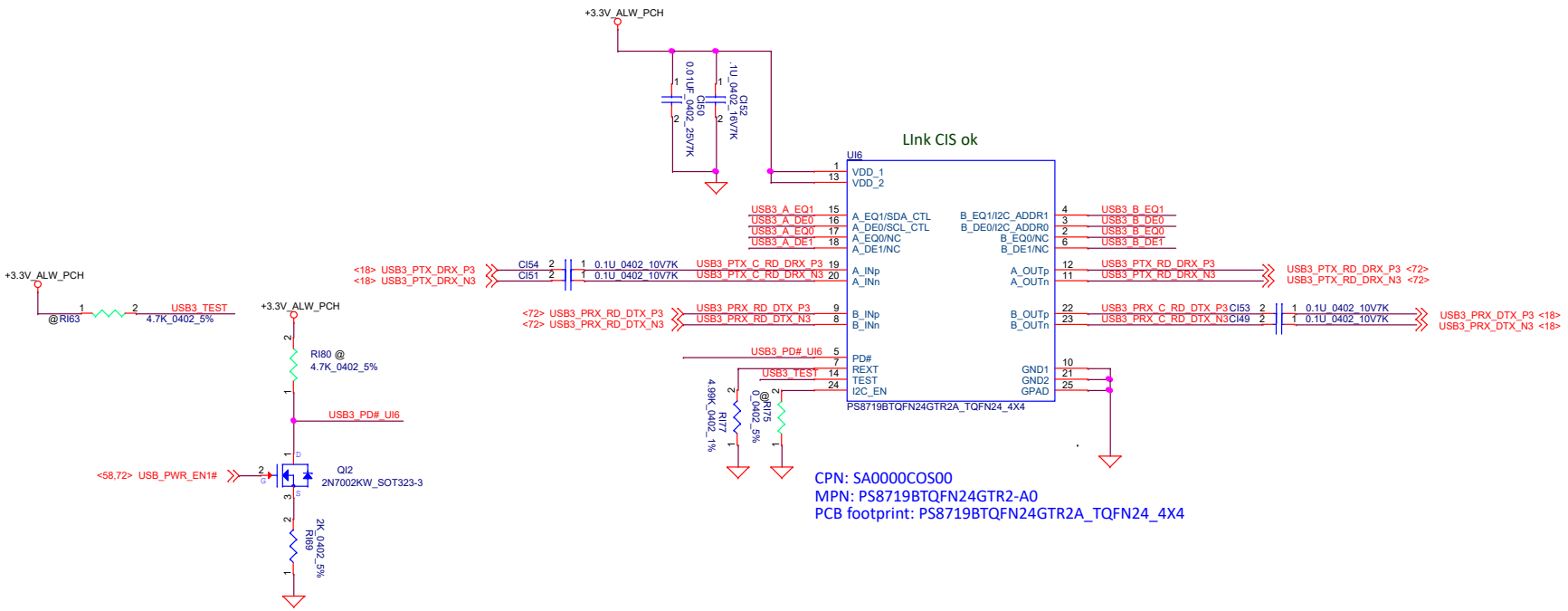
Title: JUSB2&JUSB3

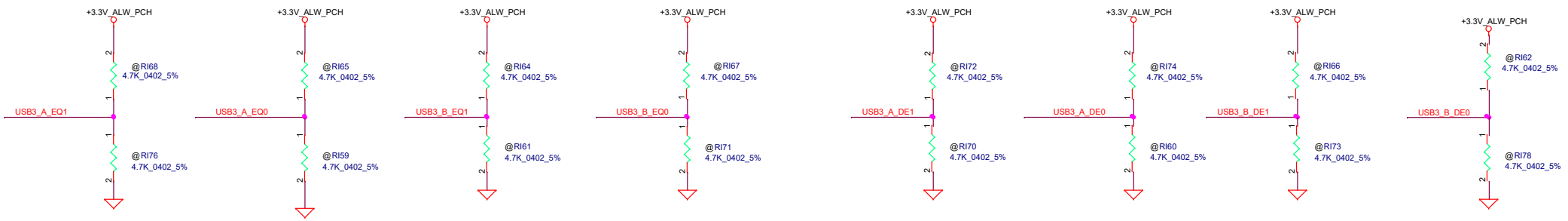
Size	Document Number	Rev
B	LA-J282P	1.0

Date: Tuesday, March 03, 2020 Sheet 72 of 108

USB3_repeater_from_PS8713B_change_to_PS8719B

FOR LEFT JUSB2 USE





Parade_PS8719B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_DE&B_DE have internal pull-down 150k

Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: USB3.0 Repeater for JUSB3

Size: Custom | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 73 of 108

Reserve

Reserve

Reserve

FOR NVPRO LAN chip BOM OPTION

NVPRO@ UL1

WGI219V SLKJ4 A0 QFN

FOR SATA repeater BOM OPTION

SATAPARA@ UN7

PS8527CTQFN20GTR2-A2

SATAPARA@ RN15

7.87K +-1% 0402

EC Chip

5107NES@ UE1

MEC5107KD4LJTR_WFBGA176P-NH

SA0000CQ740

FOR Precision sku SSID

N19@ RE300

2K_0402_5%

FOR Precision GPU CPN

N19@ UV1

S IC N19M-Q3-A1 FCBGA 908P GPU

FOR SATA repeater X76

SATAPERIX76@ ZZZ

ALT. GROUP PARTS SATA PERICOM CDP80

X7670231LC5

SATAPARAX76@ ZZZ

ALT. GROUP PARTS SATA PARADE CDP80

X7670231LC4

FOR 15HD VRAM BOM OPTION

X76 PN to change in DVT

VENDER	STRAP	Part Number	Strap2,Strap1,Strap0)	H:RV239 L:RV240	H:RV237 L:RV238	H:RV235 L:RV236
Samsung	0x3	K4G80325FC-HC25 SA00009TA3L 2GSAM@ UV17 K4G80325FC-HC25 2GSAM@ UV18 K4G80325FC-HC25	(L, H, H)	2GSAM@ RV240 100K_0402_5%	2GSAM@ RV237 100K_0402_5%	2GSAM@ RV235 100K_0402_5%
Micron	0x4	MT51J256M32HF-80:B SA00009TI3L 2GMICR@ UV17 MT51J256M32HF-80:B 2GMICR@ UV18 MT51J256M32HF-80:B	(H, L, L)	2GMICR@ RV239 100K_0402_5%	2GMICR@ RV238 100K_0402_5%	2GMICR@ RV236 100K_0402_5%
Hynix	0x5	H5GC8H24AJR-R2C SA0000C171L 2GHYN@ UV17 H5GC8H24AJR-R2C 2GHYN@ UV18 H5GC8H24AJR-R2C	(H, L, H)	2GHYN@ RV239 100K_0402_5%	2GHYN@ RV238 100K_0402_5%	2GHYN@ RV235 100K_0402_5%

FOR 15HD VRAM X76

2GSAMX76@ ZZZ

ALT. GROUP PARTS VRAM SAM EDC42

X7670231LC3

2GMICRX76@ ZZZ

ALT. GROUP PARTS VRAM MICRON EDC42

X7670231LC1

2GHYNX76@ ZZZ

ALT. GROUP PARTS VRAM HYNIX EDC42

X7670231LC2

FOR 15P VRAM BOM OPTION

VENDER	STRAP	Part Number	Strap2,Strap1,Strap0)	H:RV239 L:RV240	H:RV237 L:RV238	H:RV235 L:RV236
Micron	0x4	MT51J256M32HF-80:B SA00009TI3L 4GMICR@ UV17 MT51J256M32HF-70:B 4GMICR@ UV18 MT51J256M32HF-70:B 4GMICR@ UV19 MT51J256M32HF-70:B 4GMICR@ UV20 MT51J256M32HF-70:B	(H, L, L)	4GMICR@ RV239 100K_0402_5%	4GMICR@ RV238 100K_0402_5%	4GMICR@ RV236 100K_0402_5%
Hynix	0x5	H5GC8H24AJR-R2C SA0000C171L 4GHYN@ UV17 H5GC8H24AJR-R0C 4GHYN@ UV18 H5GC8H24AJR-R0C 4GHYN@ UV19 H5GC8H24AJR-R0C 4GHYN@ UV20 H5GC8H24AJR-R0C	(H, L, H)	4GHYN@ RV239 100K_0402_5%	4GHYN@ RV238 100K_0402_5%	4GHYN@ RV235 100K_0402_5%

FOR 15P VRAM X76

4GMICRX76@ ZZZ

ALT. GROUP PARTS VRAM MICRON EDA51

X7670231LD1

4GHYNX76@ ZZZ

ALT. GROUP PARTS VRAM HYNIX EDA51

X7670231LD2

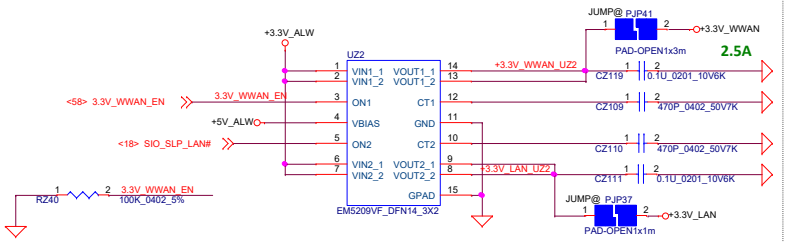
Compal Electronics, Inc.

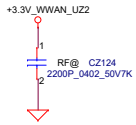
Title: Bom option

Size | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 77 of 108

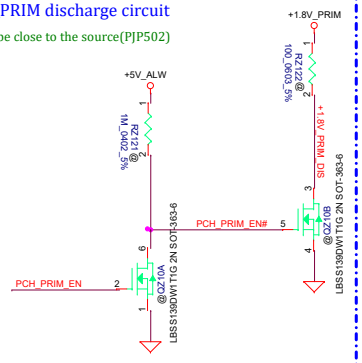
+3.3V_WWAN/+3.3V_LAN source



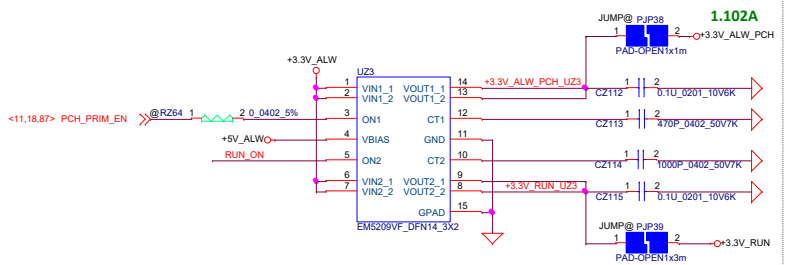


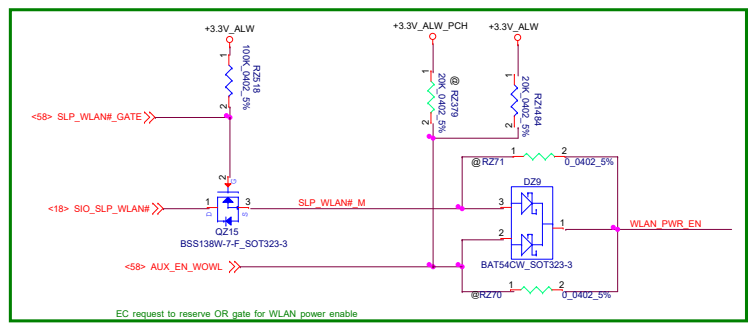
+1.8V_PRIM discharge circuit

Need to be close to the source(PJP502)

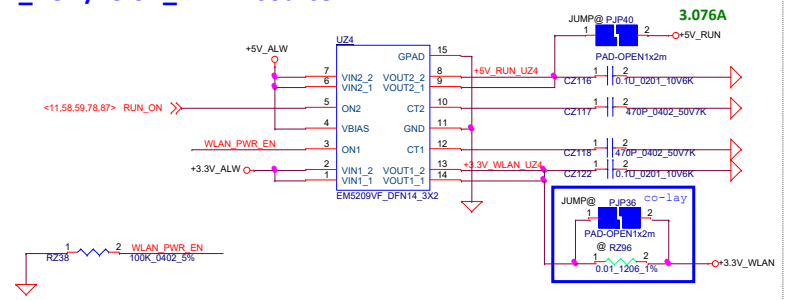


+3.3V_ALW_PCH/+3.3V_RUN source

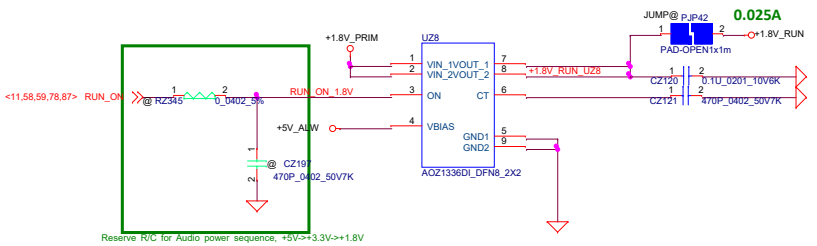




+5V_RUN/+3.3V_WLAN source



+1.8V_RUN source



Security Classification	Compal Secret Data		
Issued Date	2019/01/01	Deciphered Date	2020/01/01

Compal Electronics, Inc.

Title: Power control

Size	Document Number	Rev
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Reserve

Reserve

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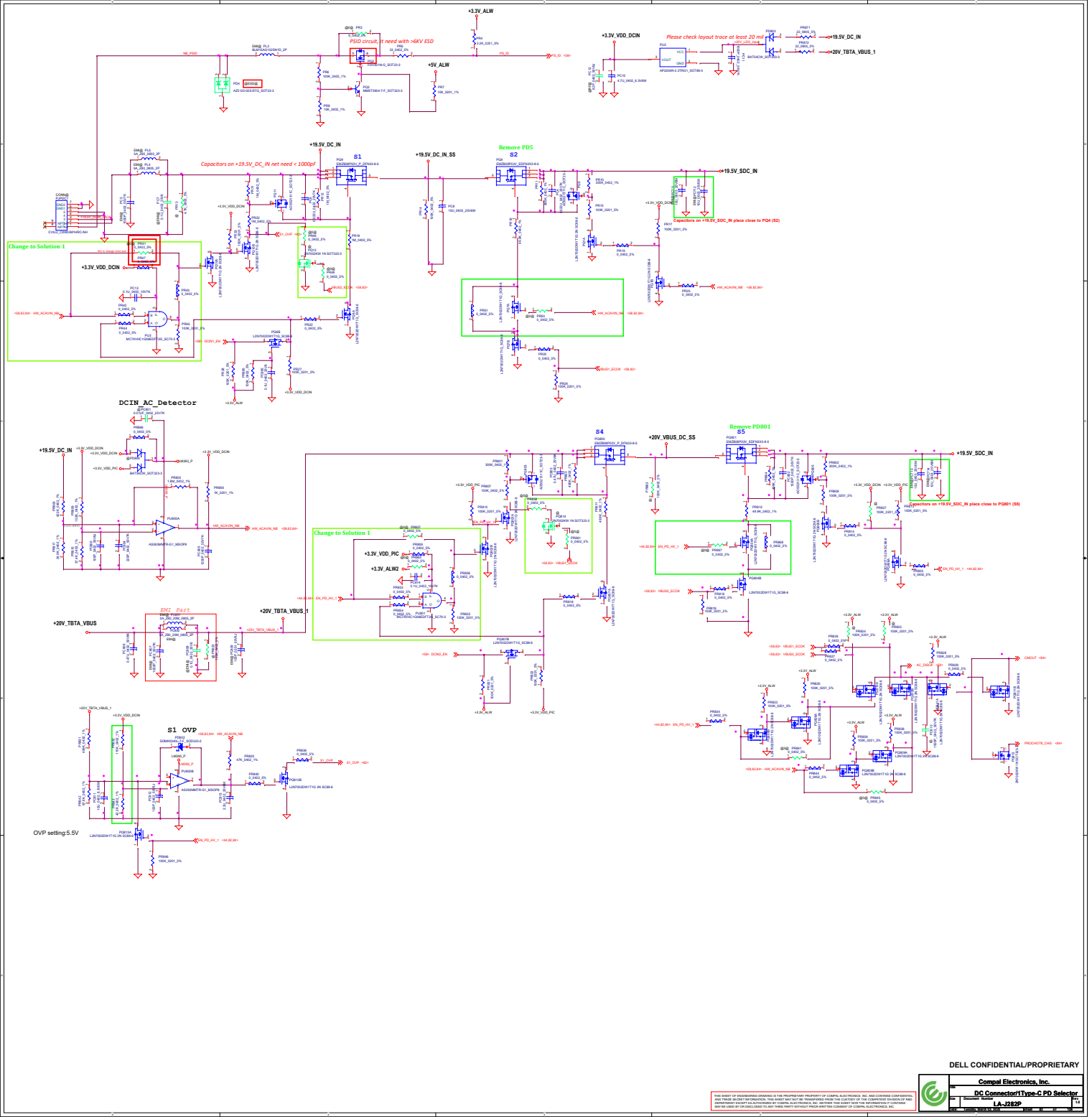
Compal Electronics, Inc.

Title: PWR-Block Diagram

Size | Document Number: LA-J282P | Rev: 1.0

Date: Tuesday, March 03, 2020 | Sheet 81 of 108



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Compal Electronics, Inc.		
DC Connector/1Type-C PD Selector		
Document Number		Rev
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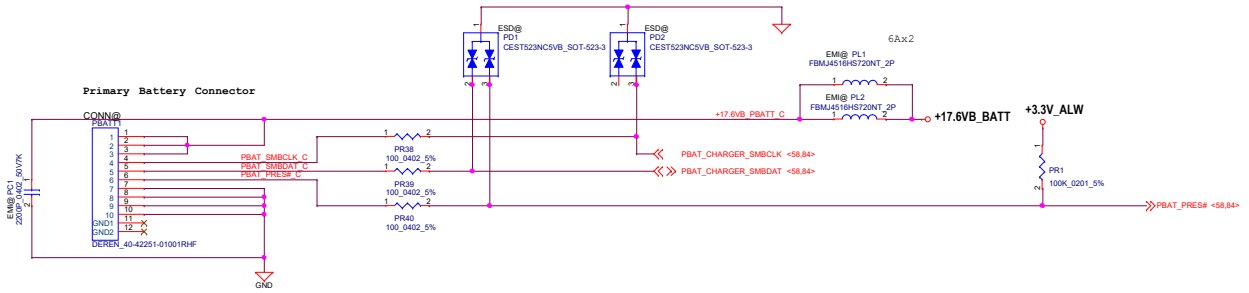
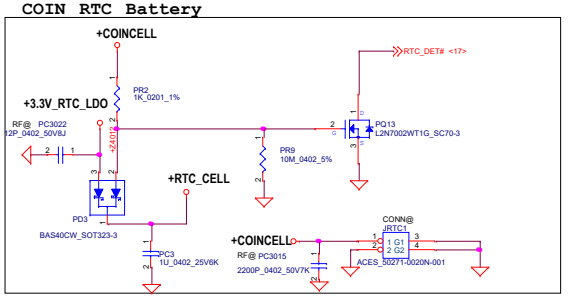
Date: Tuesday, March 06, 2018	Sheet 38 of 103	



COIN RTC Battery



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Compal Electronics, Inc.

Title: Battery Connector/ RTC

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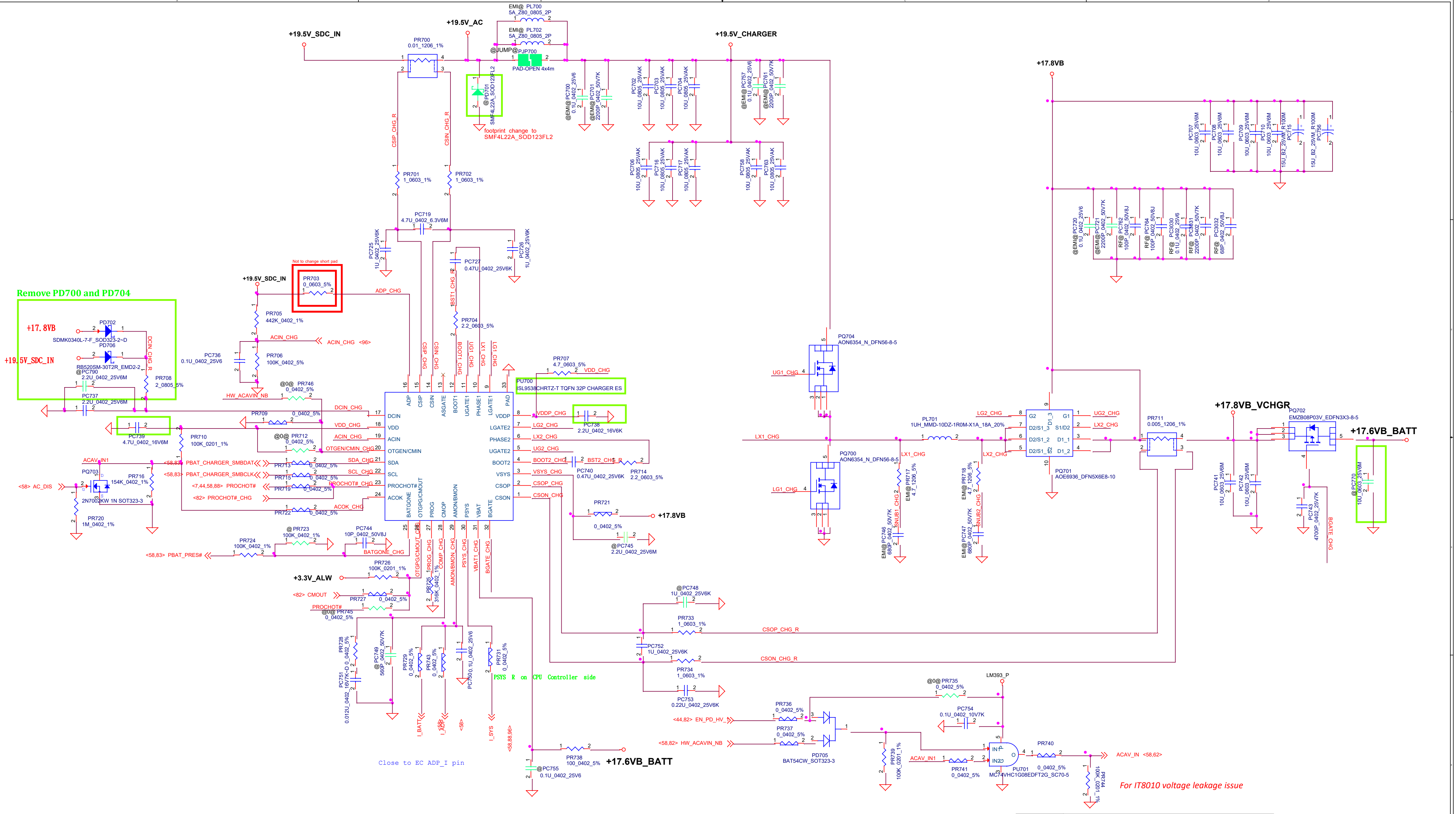

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Compal Electronics, Inc.

Title: Charger

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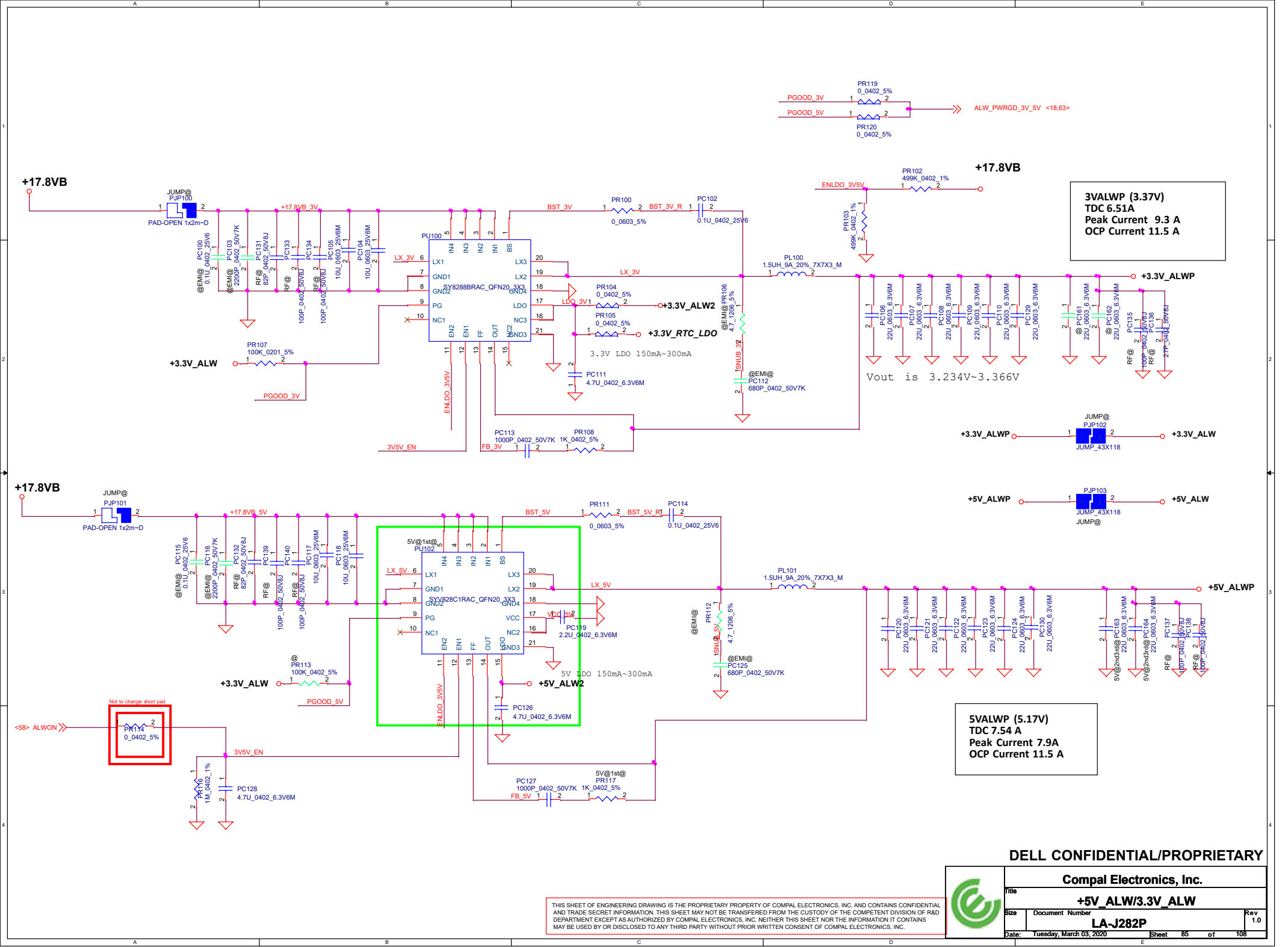

Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
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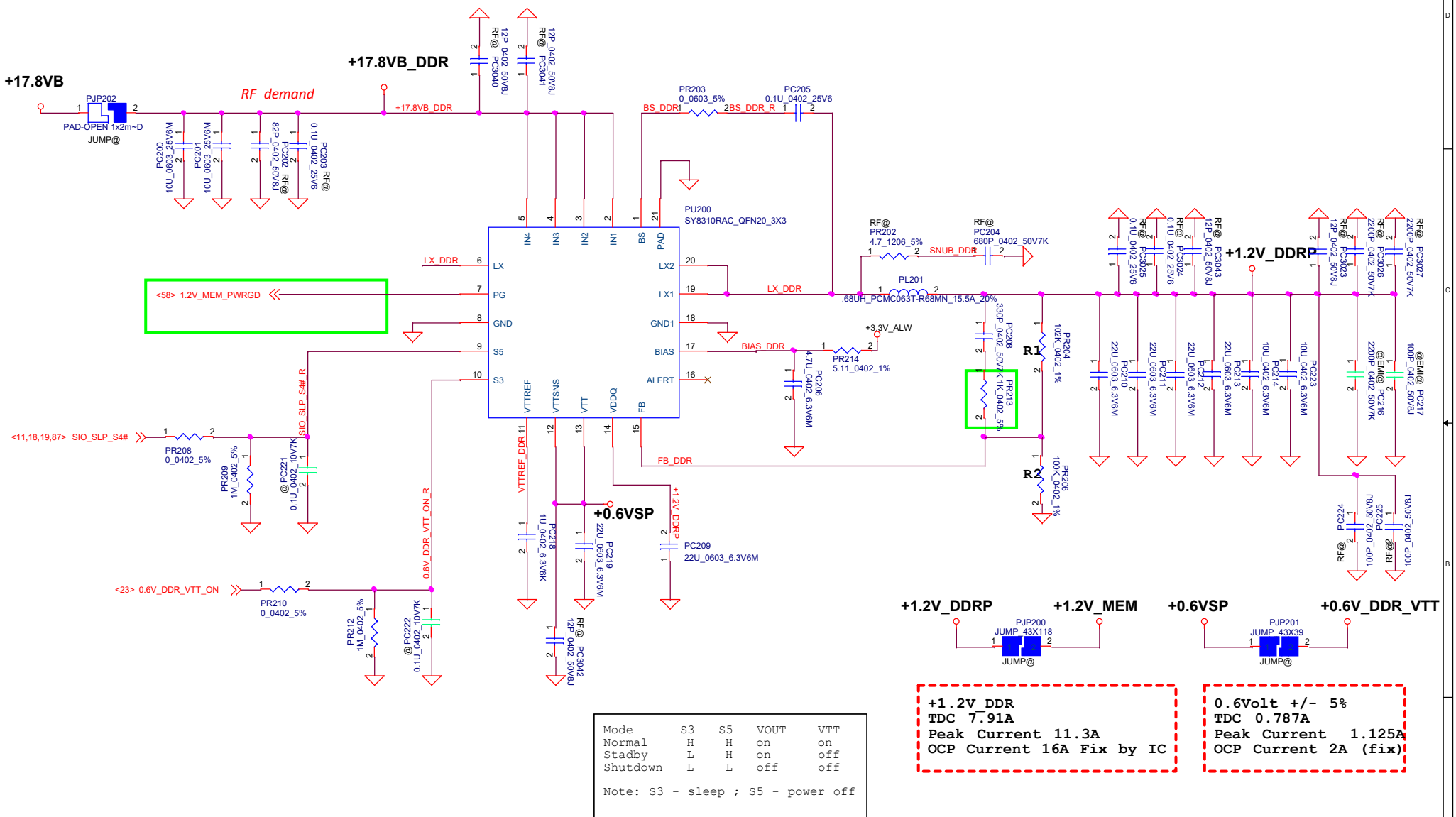

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 7.91A
Peak Current 11.3A
OCP Current 16A Fix by IC

0.6Volt +/- 5%
TDC 0.787A
Peak Current 1.125A
OCP Current 2A (fix)

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Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

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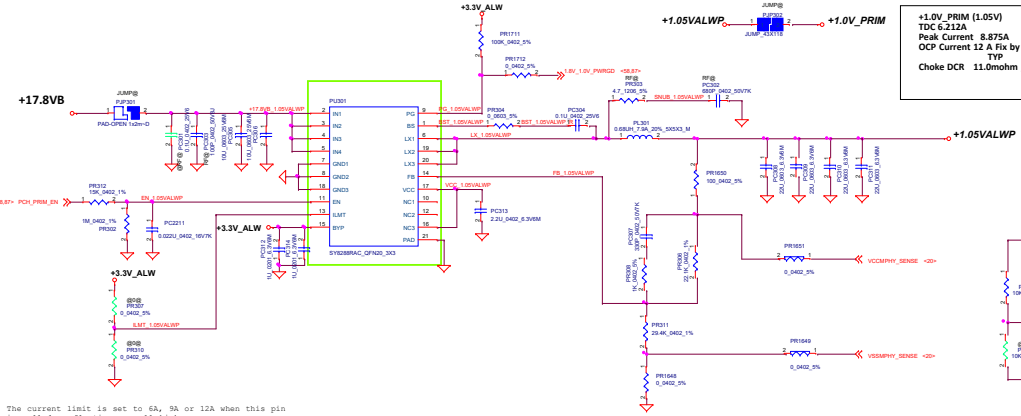
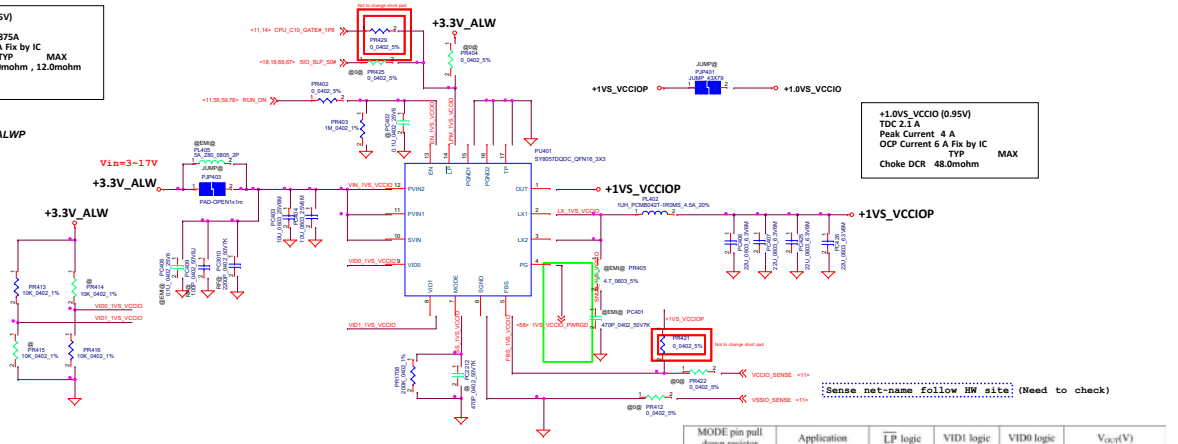
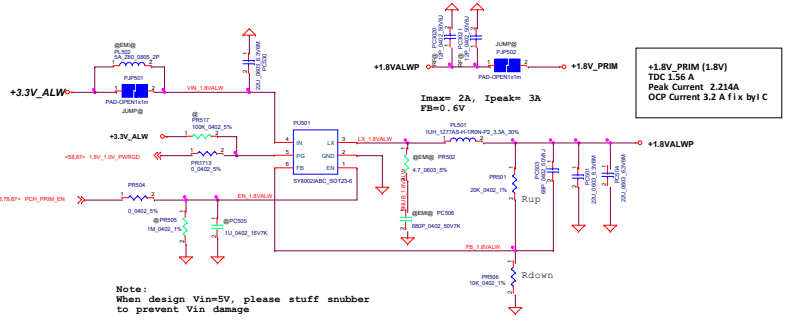
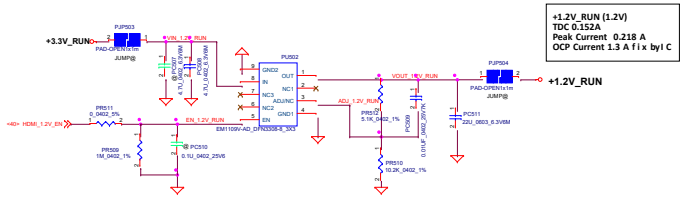
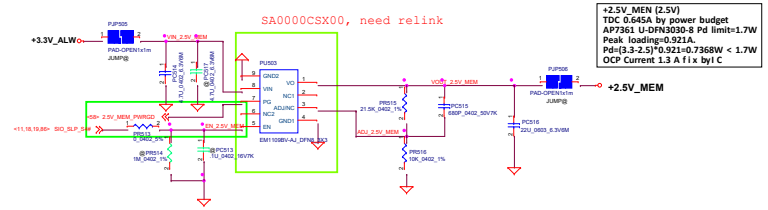




MODE pin pull down resistor	Application	$\overline{LP}$ logic	VID1 logic	VID0 logic	V_{OUT}(V)
200k	Vcc_IO	0	x	x	0.000(LPM)
		1	0	0	0.850
		1	0	1	0.875
		1	1	0	0.950
		1	1	1	0.975
>500k or floating	Vcc_PRIM_CORE	0	x	x	0.700(LPM)
		1	0	0	0.850
		1	0	1	0.900
		1	1	0	0.950
		1	1	1	1.000
0	Vcc_EDRAM	0	x	x	0.000(LPM)
		1	0	0	0.800(MSM)
		1	0	1	0.950
		1	1	0	1.000
		1		1	1.050







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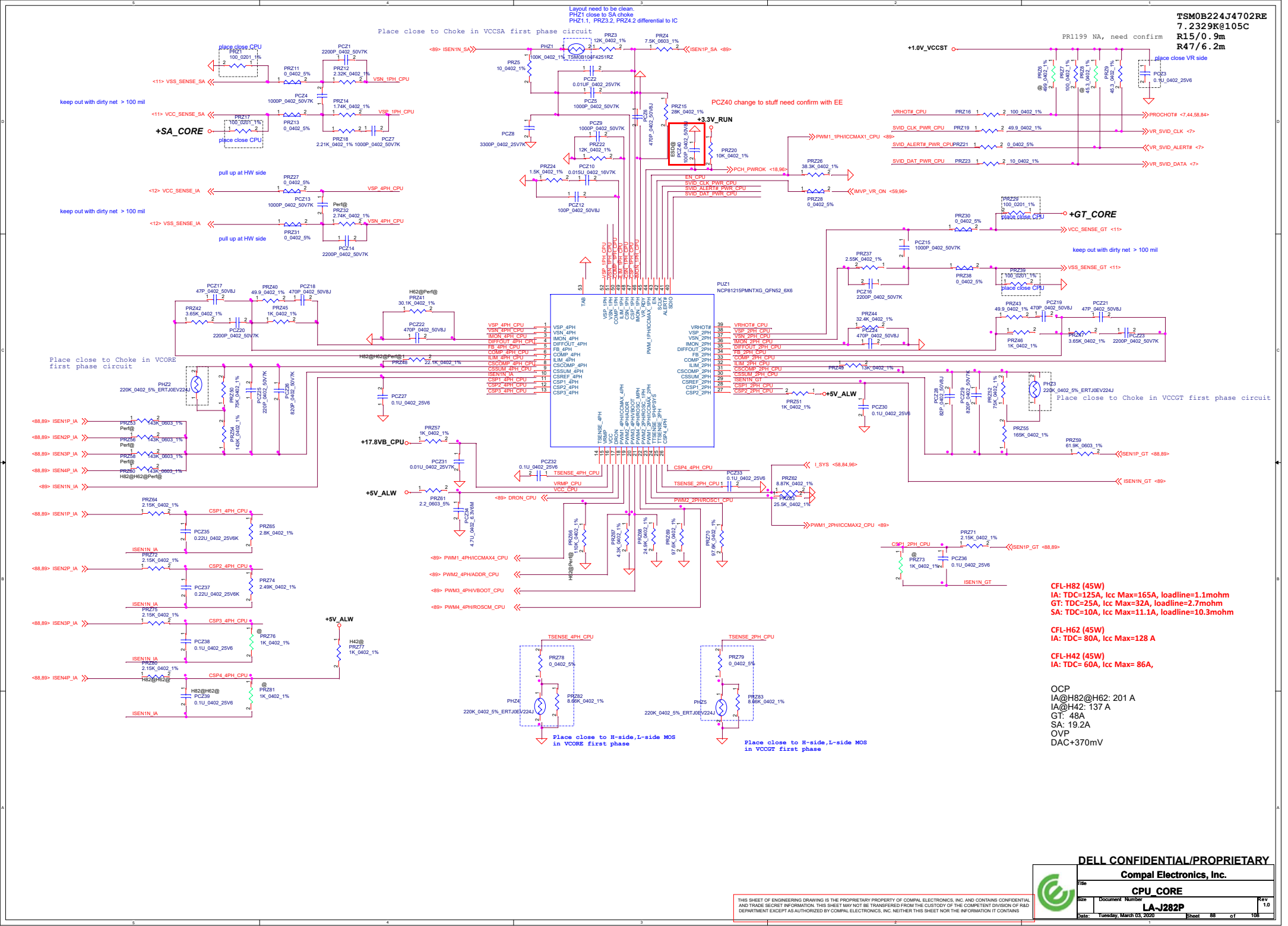
+1VALWP/VCCIO/PRIM_CORE/1.8V/2.5V/1.2V

LA-J282P

1.0

Tuesday, March 05, 2013



Compal Electronics, Inc.
Title: CPU_CORE
Size: Document Number: LA-J282P
Rev: 1.0
Date: Tuesday, March 03, 2020
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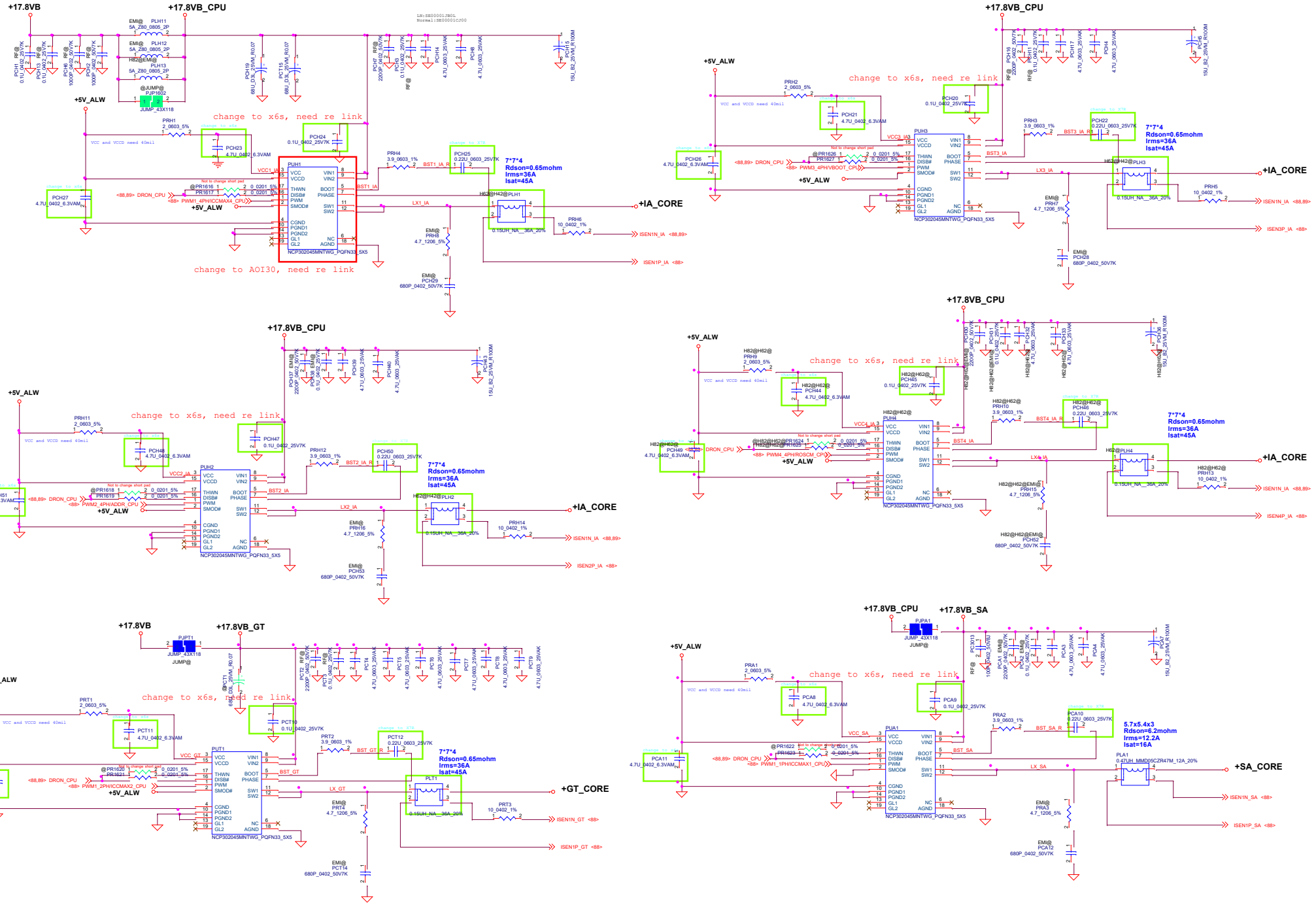

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Compal Electronics, Inc.	
Title	CPU_CORE
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Date:	Tuesday, March 03, 2020
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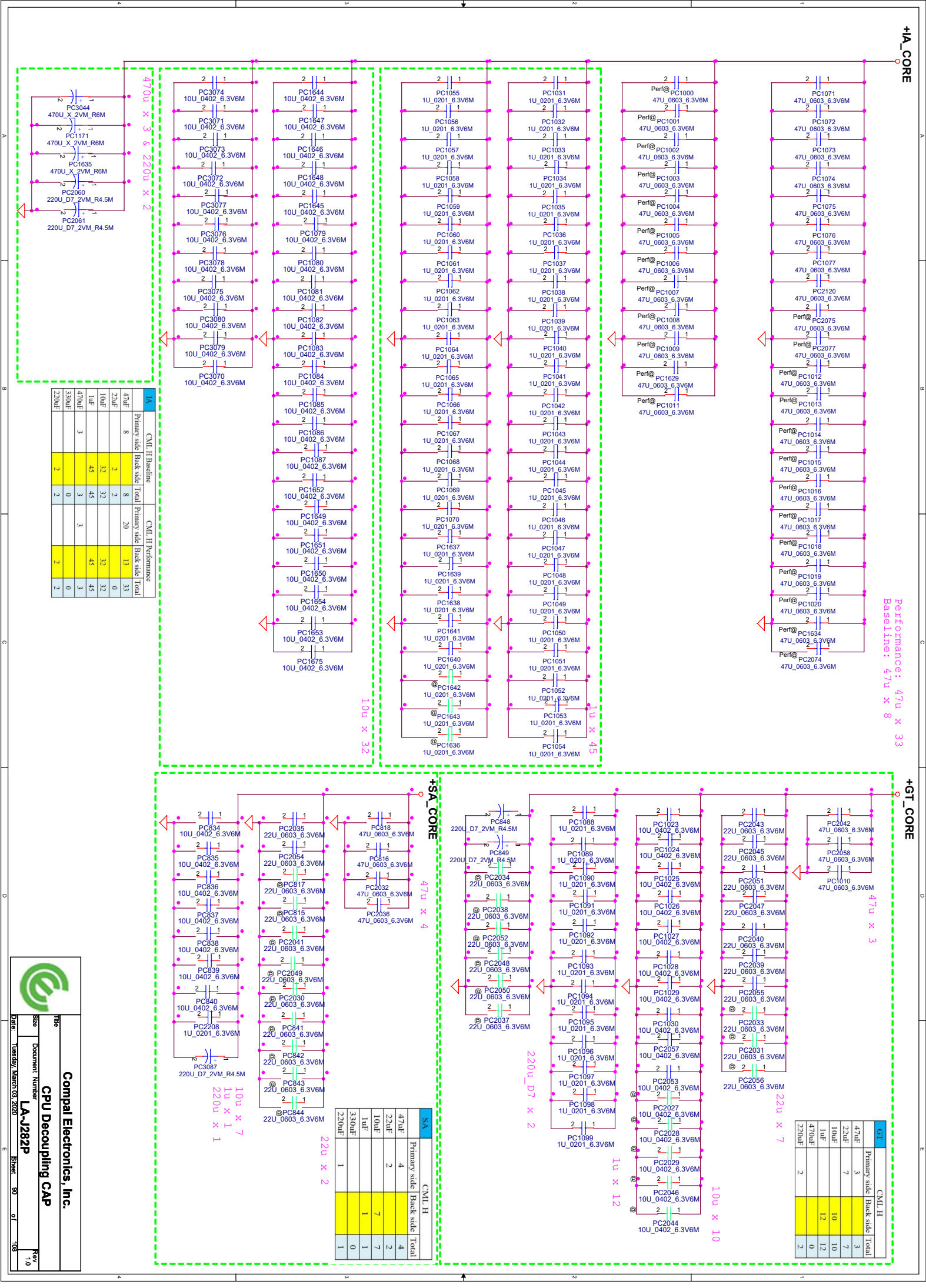

IA	CML H Baseline				CML H Performance			
	Primary side	Back side	Total		Primary side	Back side	Total	
47uF	8		8		20			
22uF		2	2			13	33	
10uF		32	32			32	32	
1uF		45	45			45	45	
470uF	3		3		3		3	
330uF								
220uF		2	2			2	2	

SA	CML H			
	Primary side	Back side	Total	
47uF	4		4	
22uF	2		2	
10uF		7	7	
1uF		1	1	
330uF				
220uF	1		1	

GT	CML H			
	Primary side	Back side	Total	
47uF	3		3	
22uF	7		7	
10uF		10	10	
1uF		12	12	
470uF				
220uF	2		2	

Compal Electronics, Inc.			
Title: CPU Decoupling CAP			
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Reserve

		N165-GTR				N17x
		Config A	Config B	Config C	Config D	N18M-Q3
Vmin	V	0.6	0.6	0.65	0.9	0.3
Vmax	V	1.2	1.2	1.15	1.15	1.3
Vboot	V	0.875	0.9	0.9	1.028	0.8
Voltage Step Vstep	mV	6.25	6.25	25	12.5	6.25
Number of Voltage Levels N	Level	96	96	20	20	160
PWM Frequency Fpwm	MHz	1.125	1.125	0.676	0.676	0.675
PWM Minimum Pulse Width Tdmin	ns	9.26	9.26	74	74	9.26
VID Transient Time T	us	<100	<100	<100	<100	<100
EDP-Continue			26.5A			30A
EDP-Peak			53A			64A
Component Value						
R1(1%)	KΩ	39	20	39	27	6.19
R2(1%)	KΩ	39	20	30	7.5	20.5
R3(1%)	KΩ	1.5	2	3	0	4.32
R4(1%)	KΩ	30	18	24	6.2	16.5
R5(1%)	KΩ	1.5	0	3	1.74	0.309
C	nF	1.5	2.7	1.8	5.6	4.7

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.8V to 1V
Active phase with CCM	1.4V to 5.5V

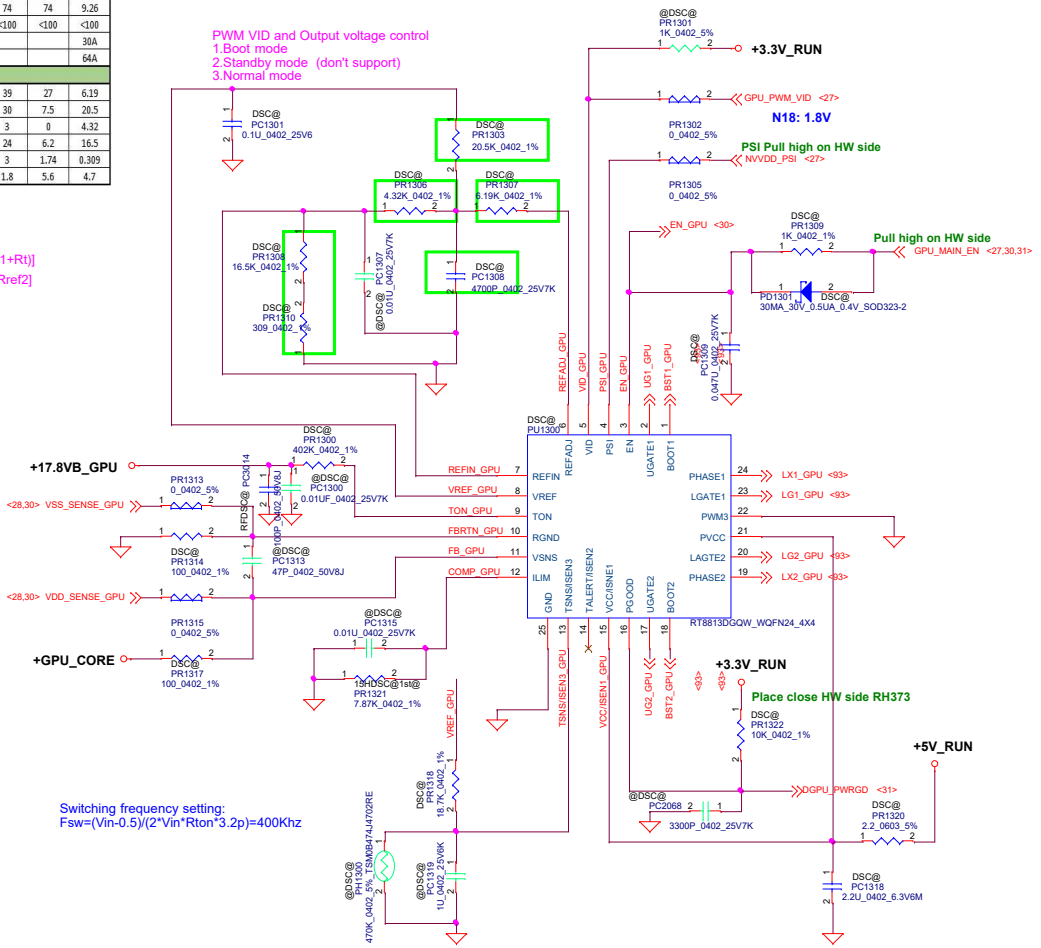
PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

14HD: N17S-G1 (GB2C-64)
15HD: N17S-G1-B (GB4C-128)
15HP:N19M-Q3

Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=400Khz



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Title: GPU_CORE

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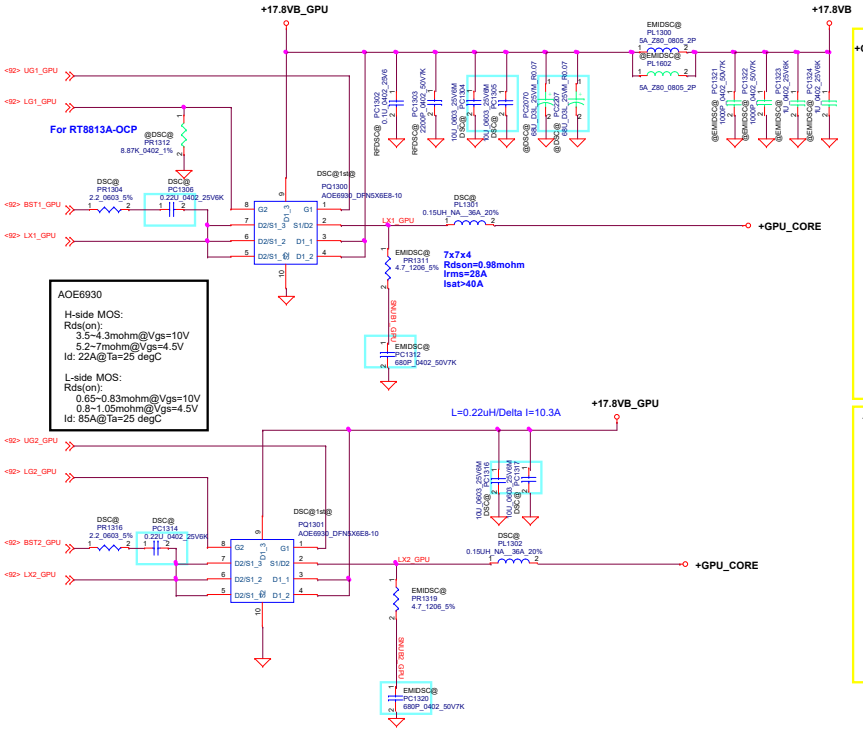
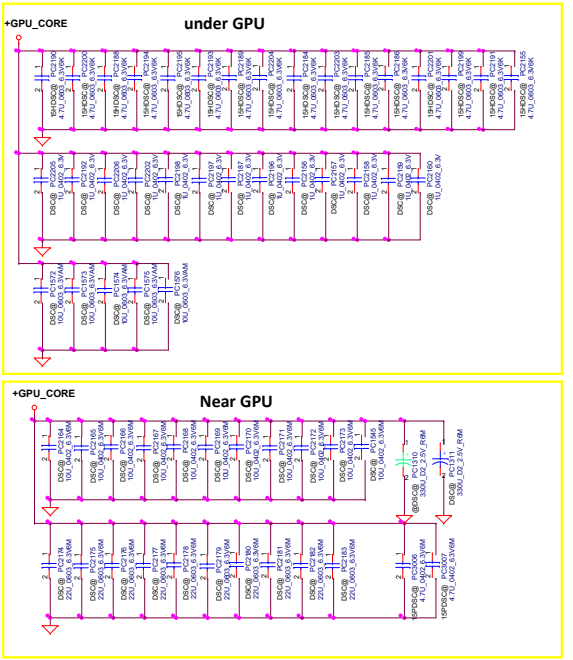
+VGA_CORE(N18M-Q3)
TDC=30 A
Peak 64 A (NVDD=54A, NVDDS=10A)
OCP=78.8 A

C=1*330uF (6mohm)=330uF
Vripple=Iripple*ESR(min)=12.78A*6mohm=76.69mV





BH X10		15PD		15HD	
		N19M-Q3		N17S-G1-B	
power rail	cap(uF)	Under	Near	Under(x6s)	Near(x6s)
NVVDD+ NVDDS	1	13		13	
	4.7		2	16	
	10	21	11	5	11
	22		10		10
	330		1		1
Total		892.4		798.2	

		N17	N19
Location	PQ1300,PQ1301	PR1321	
Main	AOE6930	7.87K	8.87K
2nd	FDPC5018SG	9.53K	13.7K
3rd	AOE6932	10.7K	12.4K

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Title: GPU_decoupling

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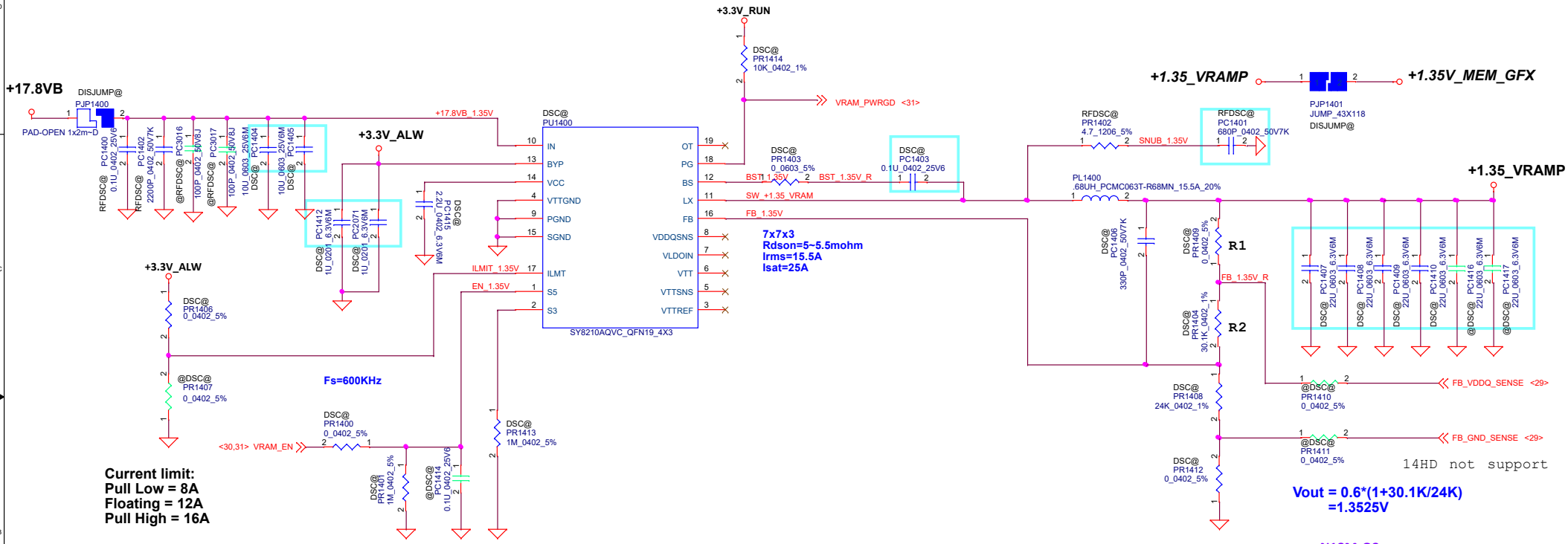
+1.35_VRAM (1.3525V)
TDC=7.7A
Peak Current=11A
OCP=16A



Compal Electronics, Inc.

Title: GPU_VRAM

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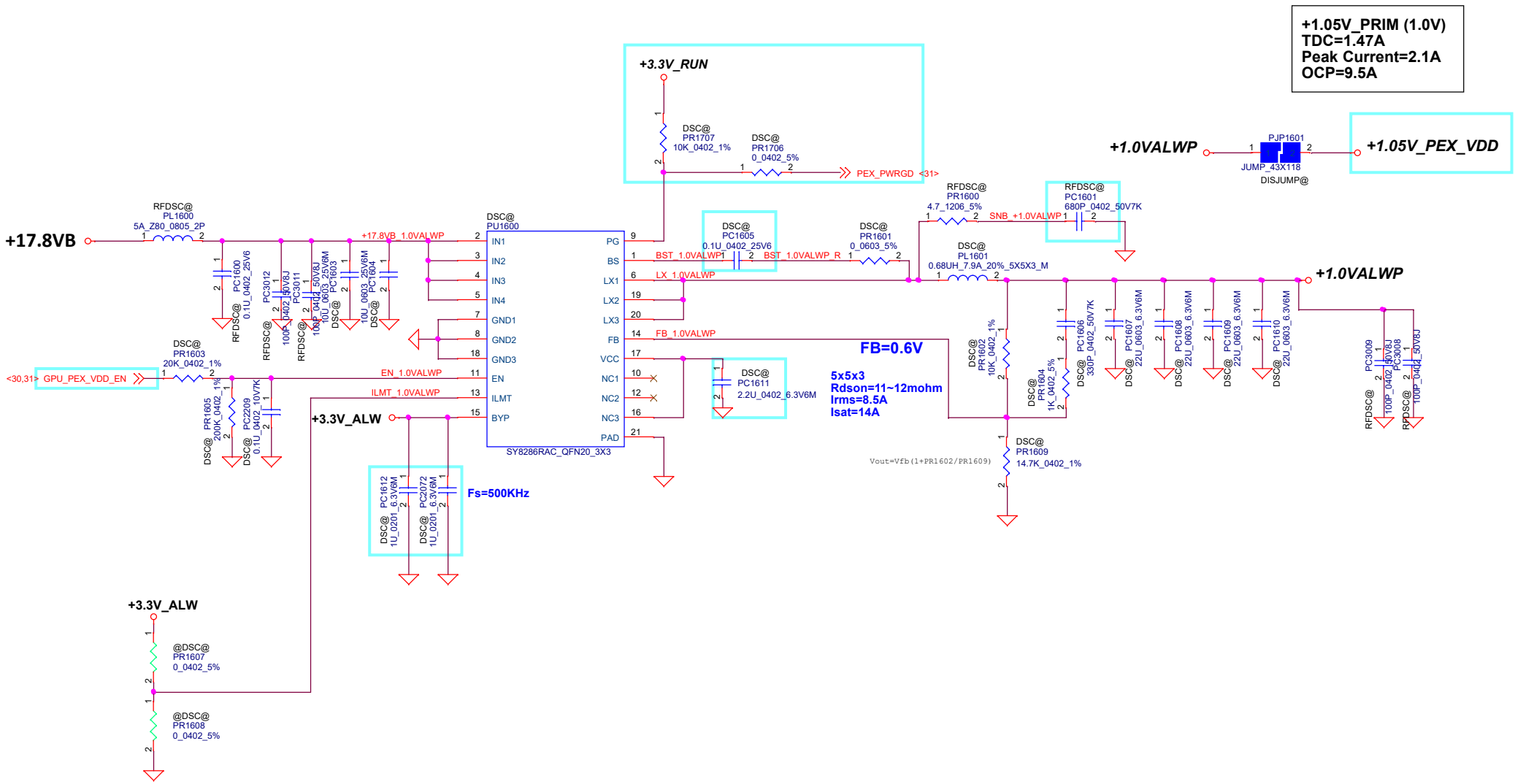

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Compal Electronics, Inc.	
Title	+1.05V_PEX_VDD
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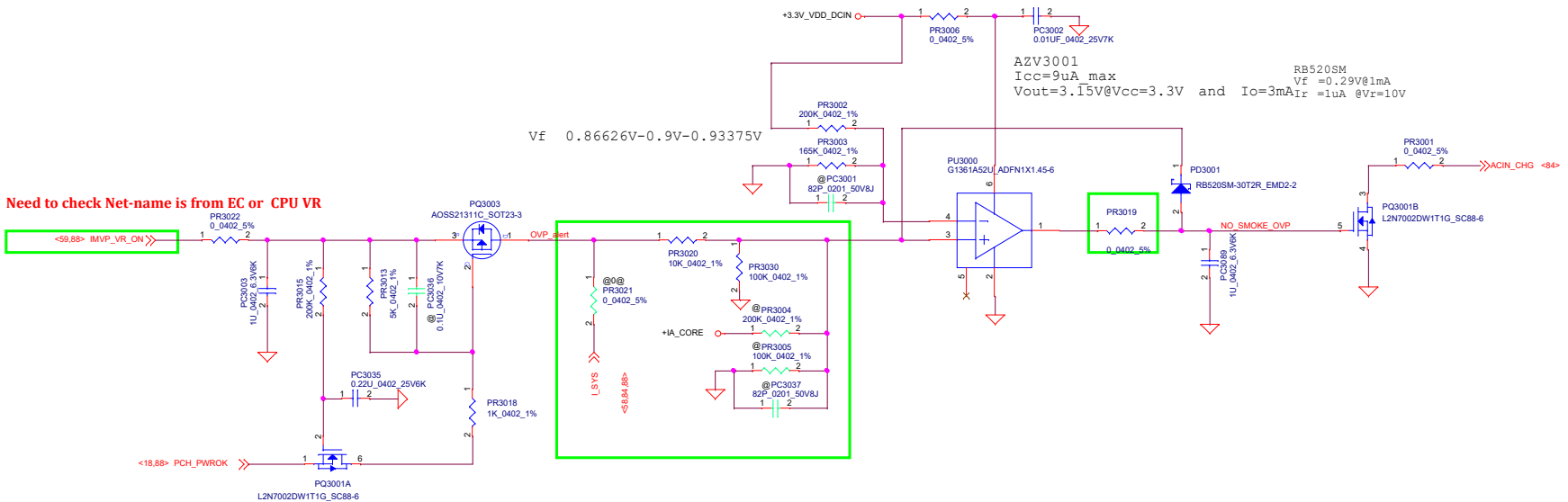

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Compal Electronics, Inc.	
Title	VCORE OVP
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Reserve

Reserve

CPU IC

H42@Base@ PRZ4T 29.4K_0402_1%
H42@Perf@ PRZ4T 26.1K_0402_1%
H62@Base@ PRZ4T 25.5K_0402_1%
H82@ PRZ4T 25.5K_0402_1%
H42@Base@ PRZ48 20.5K_0402_1%
H42@Perf@ PRZ48 14.3K_0402_1%
H62@Base@ PRZ48 26.1K_0402_1%

H42@Base@ PRZ6R 68.1K_0402_1%
H42@Perf@ PRZ6R 82.5K_0402_1%
H62@Base@ PRZ6R 100K_0402_1%
H82@ PRZ6R 130K_0402_1%
Base@ PRZ32 2.05K_0402_1%
Base@ PRZ53 90.9K_0402_1%
Base@ PRZ56 90.9K_0402_1%

Base@ PRZ58 90.9K_0402_1%
H82@H62@Base@ PRZ60 90.9K_0402_1%

		H82	H62		H42	
Function	Location	Perf@	Perf@	Base@	Perf@	Base@
Loadline	PRZ53,PRZ56 PRZ58,PRZ60	143K	143K	90.9K	143K PRZ60 Unstuff	90.9K
Iccmax	PRZ66	130K	110K	100K	82.5K	68.1K
Imon	PRZ41	25.5K	30.1K	25.5K	26.1K	29.4K
Ilim	PRZ48	22.1K	22.1K	26.1K	14.3K	20.5K
	PRZ32	2.74K	2.74K	2.05K	2.74K	2.05K

CPU Choke

H82@1st@ PLH1 0.15UH_MMD06DZER15MEM2L_36A_20%
H82@1st@ PLH2 0.15UH_MMD06DZER15MEM2L_36A_20%
H82@1st@ PLH3 0.15UH_MMD06DZER15MEM2L_36A_20%

H82@1st@ PLH4 0.15UH_MMD06DZER15MEM2L_36A_20%
H82@2nd3rd@ PLH1 0.15UH_BMKM00060640R15M2L_36A_20%
H82@2nd3rd@ PLH2 0.15UH_BMKM00060640R15M2L_36A_20%

H82@2nd3rd@ PLH3 0.15UH_BMKM00060640R15M2L_36A_20%
H82@2nd3rd@ PLH4 0.15UH_BMKM00060640R15M2L_36A_20%

OUTPUT CAPS

Base@ PC1000 22U_0603_6.3V6M
Base@ PC1001 22U_0603_6.3V6M

+5V_ALWP

5V@2nd3rd@ PU102 TPS51395P-1 VQFN 20P PWM
5V@2nd3rd@ PR117 71.5K_0402_1%

GPU IC

15PDSC@1st@ PR1321 8.87K_0402_1%
15HDSC@2nd@ PR1321 9.53K_0402_1%
15PDSC@2nd@ PR1321 13.7K_0402_1%
DSC@2nd@ PQ1300 FDPC5018SG_POWER-CLIP56-8-10
DSC@2nd@ PQ1301 FDPC5018SG_POWER-CLIP56-8-10

15HDSC@3rd@ PR1321 10.7K_0402_1%
15PDSC@3rd@ PR1321 12.4K_0402_1%
DSC@3rd@ PQ1300 AOE6932_DFN5X6E8-10
DSC@3rd@ PQ1301 AOE6932_DFN5X6E8-10

		N17	N19
Location	PQ1300,PQ1301	PR1321	
Main	AOE6930	7.87K	8.87K
2nd	FDPC5018SG	9.53K	13.7K
3rd	AOE6932	10.7K	12.4K

OUTPUT CAPS

15PDSC@ PC2190 10U_0603_6.3VAM
15PDSC@ PC2200 10U_0603_6.3VAM
15PDSC@ PC2188 10U_0603_6.3VAM
15PDSC@ PC2194 10U_0603_6.3VAM
15PDSC@ PC2195 10U_0603_6.3VAM

15PDSC@ PC2193 10U_0603_6.3VAM
15PDSC@ PC2189 10U_0603_6.3VAM
15PDSC@ PC2204 10U_0603_6.3VAM
15PDSC@ PC2184 10U_0603_6.3VAM
15PDSC@ PC2203 10U_0603_6.3VAM

15PDSC@ PC2185 10U_0603_6.3VAM
15PDSC@ PC2186 10U_0603_6.3VAM
15PDSC@ PC2201 10U_0603_6.3VAM
15PDSC@ PC2199 10U_0603_6.3VAM
15PDSC@ PC2191 10U_0603_6.3VAM

15PDSC@ PC2155 10U_0603_6.3VAM

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Compal Electronics, Inc.
Title: Reserve for PWR
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Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.

Category	Sub-category	BHMLK_EVvsBH(15HD)	
		Change	Remark
Power	Power Path_Barrel	Schematic	Follow X11 POV
	Power Path_Type C (1,2...)	Schematic	Follow X11 POV
	LCD_Backligtht_Driver	NA	
	3VALW	No	
	5VALW	No	
	1.2V_DDR	Schematic	IC solution change from SY8210 to SY8310
	0.6VS	No	
	1.8VA	No	
	VCC_CORE	BOM	CPU parameter change to CML-H (Iccmax, LL,OCP) CPU decoupling cap change to CML-H
	VCC_GT	No	
	VCC_SA	BOM	CPU decoupling cap change to CML-H
	1.8VU	No	
	1.0VA	BOM	IC solution change from SY8286RAC to SY8288RAC
	1.0VS_VCCIO	No	
	2.5V_MEM	BOM	IC solution change from EM1109V to EM1109BV Add power good function for V-tree
	Charger	Schematic	Change ISN choke to bead+MLCC
	Wireless Charging	No	
	GPU_CORE	No	
	charger UVP and Vcore OVP	Schematic	Follow X11 POV

Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.

Category	Sub-category	BH MLK vs NB MLK	BHMLK_EV vs BH(15HD)	
			Change	Remark
Power	Power Path_Barrel	Same	BOM	Change back to X10 solution
	Power Path_Type C (1,2...)	Same	BOM	Change back to X10 solution
	VCC_CORE	Different (Different CPU)	BOM	1.CPU parameter change to CML-H (Iccmax, LL,OCP) 2.CPU decoupling cap add performance and baseline option
			Schematic	CPU decoupling cap add 3 pcs 1uF 0201 for baseline option& layout placement same as X10
	Charger	Same	Schematic	1. Add PC790 same as PC737 2.2U_0402_25V(SE000013H00)
	Charger UVP and Vcore OVP	Same	Schematic	1.Add PR3006 0_0402_5%(SD028000080) on PU3000 Vcc pin 2.Change PR3003 from 120K_0402_1% to 165K_0402_1%(SD034165380)
	Common (Source change)	Same	BOM	1.Change PR202,PR303 from S RES 1/2W 4.7 +-5% 1206(SD000010280) to S RES 1/4W 4.7 +-5% 1206(SD001470B80) 2.Change DSC parts PR1311,PR1319,PR1402 and PR1600 from S RES 1/2W 4.7 +-5% 1206(SD000010280) to S RES 1/4W 4.7 +-5% 1206(SD001470B80)

Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.

Category	Sub-category	BH MLK vs NB MLK	BHMLK_EV vs BH(15HD)	
			Change	Remark
Power	Common (Source change)	Same	BOM	1. BOM change to modify DIDT for ESD protect solution. PQ5, PQ11, PQ803, PQ805, PQ3003 change from S TR AOSS21319C 1P SOT23-3(SB00001ST00) to S TR AOSS21311C 1P SOT23-3(SB00001SS00)
	Charger	Same	BOM	1. Follow vender suggest (RENESAS) to un-pop PC790 (2.2U_0402_25V(SE000013H00)
	Common	NA	Schematic/BOM	0 ohm change to short-pad

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay Time (ps/inch)	DK	DF(1GHz)	35 ± 3.5 ohm single-end	40 ± 4 ohm single-end	42 ± 4.2 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm single-end	80 ± 8 ohm Diff	85 ± 8.5 ohm Diff	88 ± 8.8 ohm Diff	90 ± 9 ohm Diff	100 ± 10 ohm Diff	REF	90 ± 9 ohm Diff	85 ±8.5 ohm Diff	REF	100 ± 10 ohm Diff	REF
		3.7	SolderMask	GA-150LL	0.50		3.70	0.03	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
			Add Plating		0.95																			
1	Top		Copper foil	0.5oz	0.65				8.5	6.6	6	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L2	7.1/4	8.5/4	L3	10.5/4.5	No REF
		3.7	Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195	34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84		90.66	85.15		99.63	
2	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		3.70	0.0187																
3	Sig1		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L2/L4				9/5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
4	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		3.70	0.0187																
5	Sig2		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L4/L6				9/5.5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					10.16	
6	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Core	3mil	3.00		3.70	0.0187																
7	Sig3		Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176	34.48	40.3	41.55	45.29	50.47	80.59	85.13	88.67	90.14	100.62					99.68	
8	Sig4		Copper foil	0.5oz	0.65				7.5	5.8	5.5	4.7	3.8	4.5/3.5	4.2/4	4/4.5	4/5	3.5/7.5	L6/L9				9/5.5	No REF
		3.7	Core	3mil	3.00		3.70	0.0187																
9	GND/PWR		Copper foil	0.5oz	0.65																			
		3.8	Prepreg	2116	4.20	163.60	3.80	0.0176																
10	Sig5		Copper foil	0.5oz	0.65				6	4.7	4.5	3.8	3.1	4/3.5	3.7/4	3.5/4.5	3.5/5.5	3/7.5	L9/L11				9/5	No REF
		3.7	Core	3mil	3.00		3.70	0.0187	34.78	40.33	41.35	45.37	50.27	80.24	85.03	88.78	90.8	100.14					99.19	
11	GND/PWR		Copper foil	0.5oz	0.65																			
		3.7	Prepreg	1086 or 1080	2.70	152.90	3.70	0.0195																
12	Bottom		Copper foil	0.5oz	0.65				8.5	6.6	6	5.3	4.3	5/4.5	4.2/4	3.9/4.1	4/5	3.5/7	L11	7.1/4	8.5/4	L10	10.5/4.5	No REF
			Add Plating		0.95				34.7	40.3	42.48	45.36	50.26	80.67	85.22	88.24	90.62	100.84		90.66	85.15		99.63	
		3.7	SolderMask		0.50		3.70	0.03																
Overall Thickness (1.2mm ± 10%)					47.90000																			
					1.21666																			
Reference GCE RD data																								

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Title: Stack Up

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PROCHOT# Topology

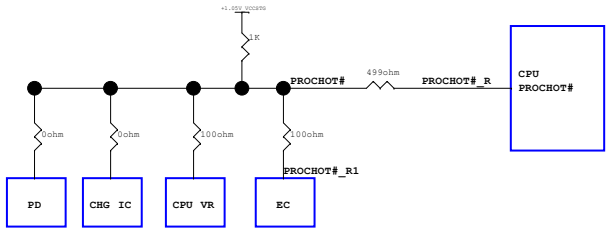


Figure 248. SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology

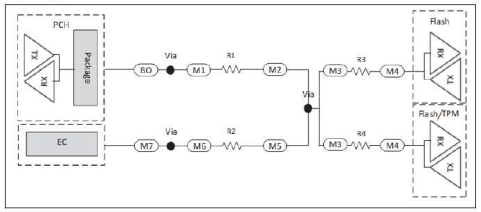
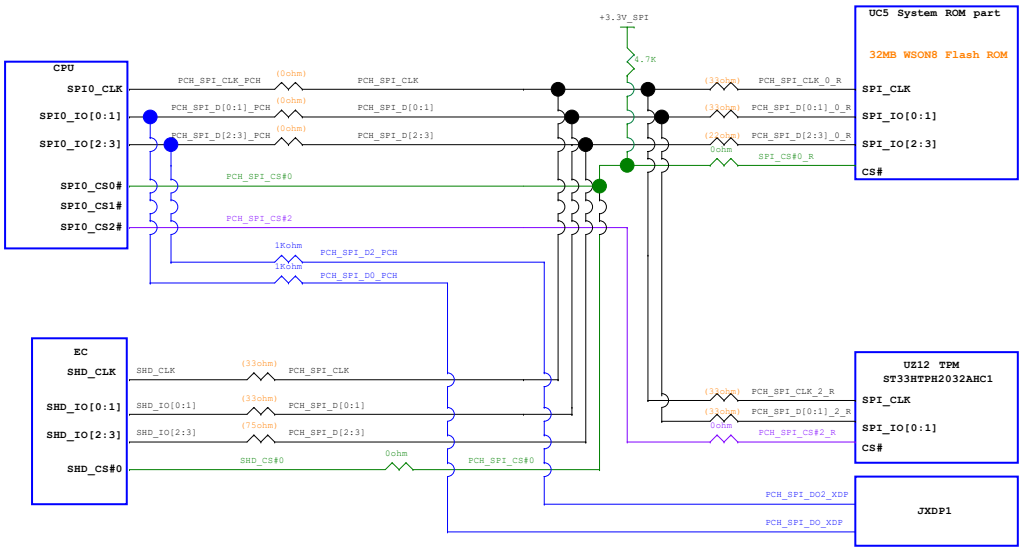


Table 229. SPI0 2 Load EC G3 Flash Sharing with Wire-OR Topology Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
BO/M7	MS/SL	VSS	1	12.7	152.4
M1/M6	MS/SL/DSL	VSS	1	76.2	
M2/M5	MS	VSS	0	25.4	
M3	MS	VSS	0	12.7	
M4	MS	VSS	0	25.4	

Notes:
1. 5 number of vias can be allowed.
2. Continuous ground referencing plane
3. Design guideline support 20MHz, 33MHz, 50MHz
4. EC and PCH branch requirement: Delta between M1+M2 and M5+M6 shall not exceed 50.8mm (2inch)
5. R1 resistor should be stuffed with 0 ohm placeholder for 3.3V and 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3.
6. R2 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses two Flash.
7. R2 resistor should be stuffed with 75 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses 1Flash and 1TPM. If TPM use this signal, R2 value shall follow MISO and MOSI recommendation.
8. R3 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses two Flash.
9. R3 resistor should be stuffed with 22 ohm for 3.3V and 50 ohm for 1.8V. To be placed on SPI0_IO_2 and SPI0_IO_3. Applicable if topology uses 1Flash and 1TPM. If TPM use this signal, R3 value shall follow MISO and MOSI recommendation
10. R4 resistor should be stuffed with 33 ohm for 3.3V and 22 ohm for 1.8V. To be placed on SPI0_CLK, SPI0_MISO and SPI0_MOSI. If TPM use SPI0_IO_2 and SPI0_IO_3, R4 value shall follow MISO and MOSI recommendation
11. Minimum length for M1, M2, M4, M5 and M6: 12.7mm
12. Minimum length for M3: 2.54mm
13. SPI branches of segment M3+M4 need to have length matching of 2.54mm
14. Length matching between CLK and DATA/CS# signals: 12.7mm
15. Trace spacing between DATA and DATA signals: 0.250mm
16. Trace spacing between CLK and DATA/Other signals: 0.375mm

EC G3 SPI Flash Sharing with Wire-OR Topology



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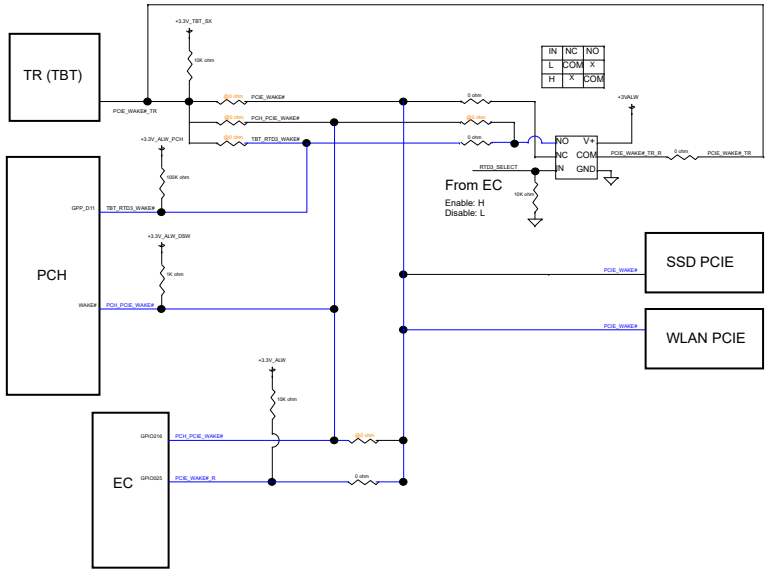
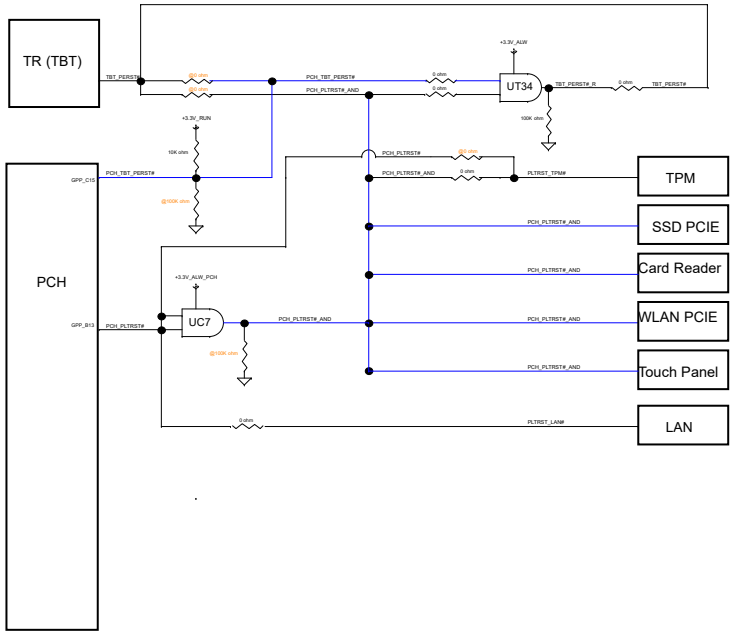
PCH_PCIE_WAKE# Topology



PCH_PLTRST# Topology



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Version Change List (P. I. R. List)

Item	Page#	Date	Issue Description	Solution Description	Rev.
1	38	2019/9/20	Reserve RC delay on +LCDVDD enable for LCD sequence adjustment flexibility(X11 platform)	add RV180 SD028000080(S RES 1/16W 0 +-5% 0402) and CV80(non-pop) SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on DV3.1	0.2(X01)
2	19 38	2019/9/20	Spyglass lesson learn, reserve PCH GPIO for TS_RST# control(X11 platform)	P19 add net TS_RST# on UH1.BE17(GPP_D13) with offpage P38 add two control path RZ311(SD028000080(S RES 1/16W 0 +-5% 0402, pop) & RZ310(SD028000080(S RES 1/16W 0 +-5% 0402, no-pop)on JIRTS1.1(TS_RST#_R) by PCH & EC(PCH_PLTRST#_AND) respectively,	0.2(X01)
3	52	2019/10/9	CML-H not light up LCD with AX201 installed, implement new push-pull and-gate as level shift for CNVi RF_RESET & CLKREQ_CNV(Aligned with Rialto and Fiorano, X11 platform)	add UZ1,UZ63 SA00003R000(S IC NL17SZ08DFT2G SC70 5P AND GATE) between PCH & WLAN NGFF	0.2(X01)
4	52 58	2019/10/9	Dell request BT_RADIO_DIS# controlled by both EC & PCH(X11 platform)	P52 add two control path DZ16,DZ2 SCS00003700(S SCH DIO RB751S40 SOD523) on JNGFF1.54 BT_RADIO_DIS# by both PCH & WLAN NGFF P58 change RE11 SD028100380(S RES 1/16W 100K +-5% 0402) form no-pop to pop	0.2(X01)
5	59	2019/10/9	DVT1.0 PCB revision, Board_ID change to X01 (X11 platform)	change RE79 from SD000001B80(S RES 1/16W 240K +-1% 0402) to SD034130380(S RES 1/16W 130K +-1% 0402)	0.2(X01)
6	17	2019/10/15	MEC5107 D4 ver has fixed load code issue, depop WDT circuit(X11 platform)	change QZ9,RZ663,CZ622 from pop to no-pop	0.2(X01)
7	44	2019/10/15	1) Dell PW SA request to disconnect PD PROHOT# control (X11 platform) 2) TI request, for TypeC disable feature(X11 platform)	1) change RT85 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from pop to no-pop(X11 platform) 2) change RT79 (SD028000080(S RES 1/16W 0 +-5% 0402, pop) from no-pop to pop(X11 platform)	0.2(X01)
8	14	2019/10/15	MLCC reduction for baseline sku	add net IA_BASELINE_SEL# on UH1.N48(GPP_K4), and PU/PD RES R105,R106 SD028100280(S RES 1/16W 10K +-5% 0402), PU stands for baseline sku	0.2(X01)
9	58	2019/11/21	Reduce power consumption by changing PCH_RSMRST#, SYS_PWROK EC side PD RES	change RE342, RE56 from 10k_0402 to 100k_0402	0.3(X02)
10	52	2019/11/22	QS CPU doesn't need REFCLK from WLAN module	depop RZ81	0.3(X02)
11	59	2019/11/22	DVT2.0 PCB revision, Board_ID change to X02 (X11 platform)	change RE79 from 130K_0402_1% to 62K_0402_1%	0.3(X02)
12	all	2019/11/25	replace 0ohm by short pad	refer to other document	0.3(X02)
14	17 58	2019/12/9	overall GPIO check for simultaneous external PU & internal PD	P17 1. depop RH310(SIO_EXT_SMI#) P58 1. depop RE561(SIO_SLP_SUS#_R)	0.3(X02)
15	59	2020/2/5	PVT PCB revision, Board_ID change to A00 (X11 platform)	change RE79 from 130K_0402_1% to 4.3K_0402_1%	1.0(A00)
16	18	2020/2/5	depop service mode switch	1. depop SWME1, RH101 2. change RH100 from 0ohm placeholder to short pad	1.0(A00)

Version Change List (P. I. R. List)

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Version Change List (P. I. R. List)

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