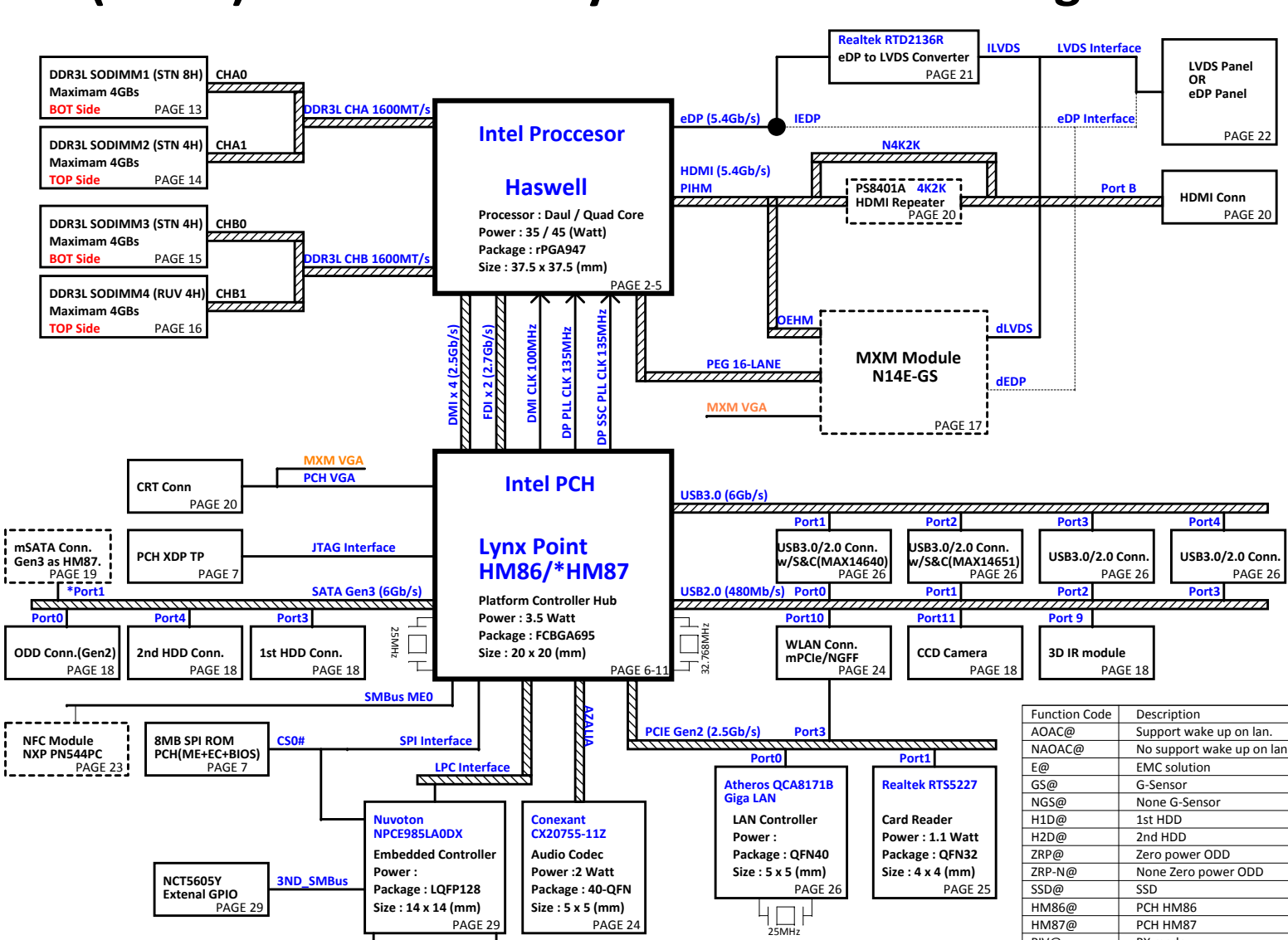
(17.3") Intel Shark Bay Platform Block Diagram

01



PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : SVCC
LAYER 5 : IN2(Low)
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT

Power Source

Intersil ISL88732HRTZ-T
System Charger Power
PAGE 30

Richtek RT8223P
System 5V/3V Power
PAGE 31

TI TPS51216RUKR
+1.35V DDR3L Power
PAGE 32

TI TPS51211DSCR
+1.05V PCH Power
PAGE 33

Intersil ISL95812HRZ-T
+VCCIN CPU Power
PAGE 34

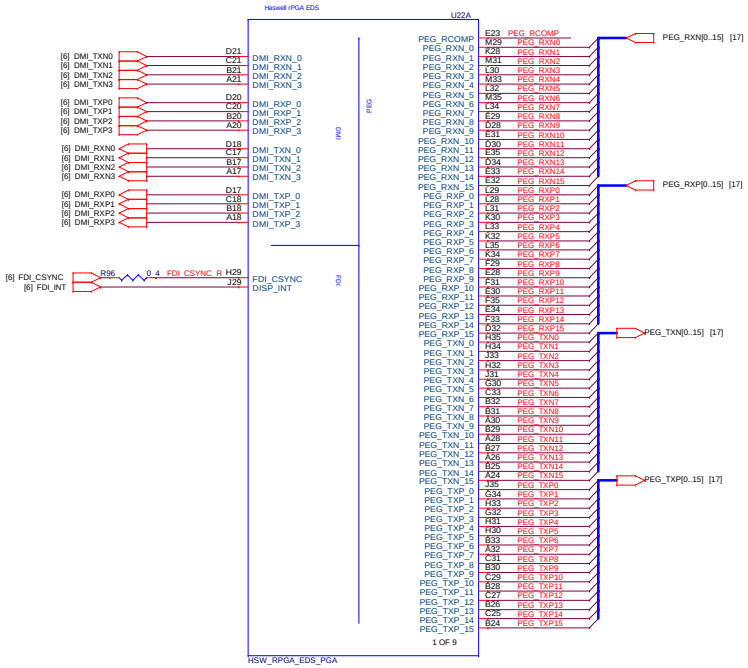
AOS AON7406
Power Switch IC
PAGE 31

Function Code	Description
IEDP@	Internal EDP mode
dEDP@	external EDP mode
ILVDS@	Internal LVDS mode
dLVDS@	external LVDS mode
EDPLVDS@	EDP / LVDS optional
OLVDS@	Only LVDS mode
OEDP@	Only EDP mode

Function Code	Description	Function Code	Description
AOAC@	Support wake up on lan.	47W@	Haswell CPU 47W
NAOAC@	No support wake up on lan.	37W@	Haswell CPU 37W
E@	EMC solution	NGFF@	Intel NGFF WLAN CARD
GS@	G-Sensor	WLAN@	WLAN mini card
NGS@	None G-Sensor	NMP@	Debug Mode
H1D@	1st HDD	WIN8@	Support WIN8
H2D@	2nd HDD	WIN7@	Support WIN7
ZRP@	Zero power ODD	CRT@	CRT function
ZRP-N@	None Zero power ODD	ICRT@	Internal CRT function
SSD@	SSD	ECRT@	External CRT function
HM86@	PCH HM86	ECO@	ECO Mode
HM87@	PCH HM87	3D@	3D Mode
PIV@	PX mode	HM@	HDMI function
OEV@	Only discrete mode	NHM@	None HDMI function
KBP@	Keyboard power	4K@	4K2K support
NKBP@	None keyboard power	N4K@	None 4K2K support
Logo_LED@	Logo LED function	8401@	Use HDMI Repeater IC 8401.
S&C@	Sleep and charge	PIHM@	PX mode internal HDMI
NS&C@	None sleep and charge	OEHM@	Only external HDMI
S3@	Power S3 mode	N4KPIHM@	None 4K2K PX mode internal HDMI
NS3@	None power S3 mode	N4KOEHM@	None 4K2K Only external HDMI
NFC@	NFC support		

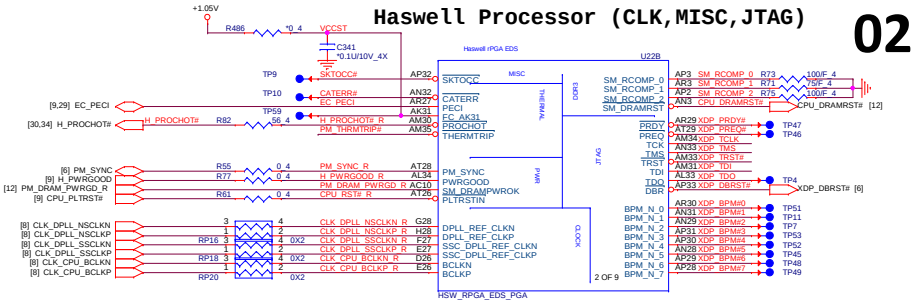
Quanta Computer Inc.
PROJECT : BDD
Size | Document Number: Block Diagram | Rev A1A
Date: Tuesday, February 05, 2013 | Sheet 1 of 37

Haswell Processor (DMI,PEG,FDI)

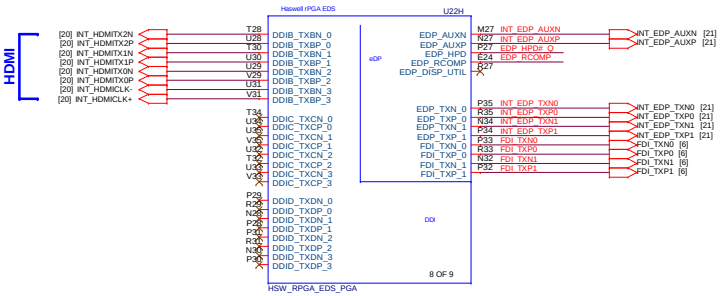


Haswell Processor (CLK,MISC,JTAG)

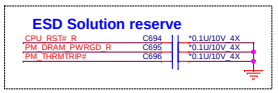
02



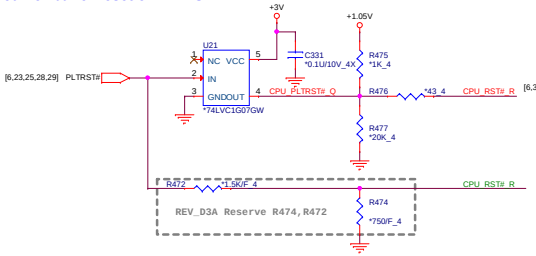
Haswell Processor (DDI,eDP,FDI)



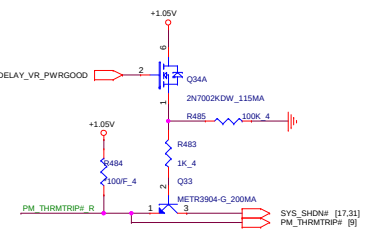
ESD Solution reserve



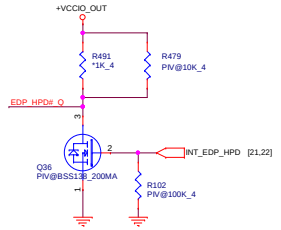
Reserved For buffer reset of PLTRSRIN# CPU



Thermal Trip & Process HOT CPU

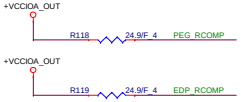


eDP Hot Plug Detect CPU

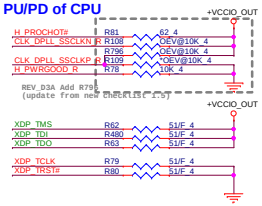


FDI Disabling (Discrete Only) <CPU>

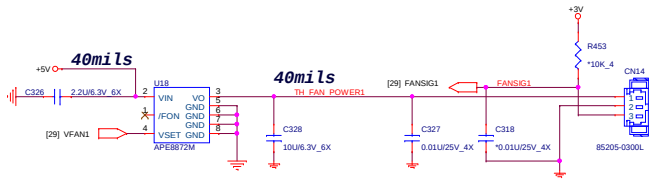
DP & PEG Compensation <CPU>



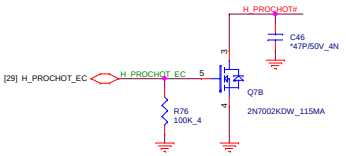
PU/PD of CPU



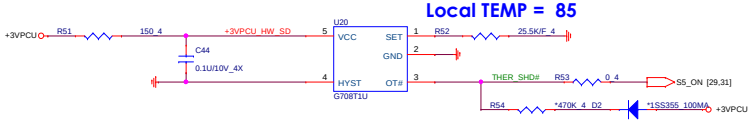
FAN Control-->For one FAN solution <THC>



Intel Turbo mode only CPU



CPU Thermal sensor / MB Local TEMP <THC>

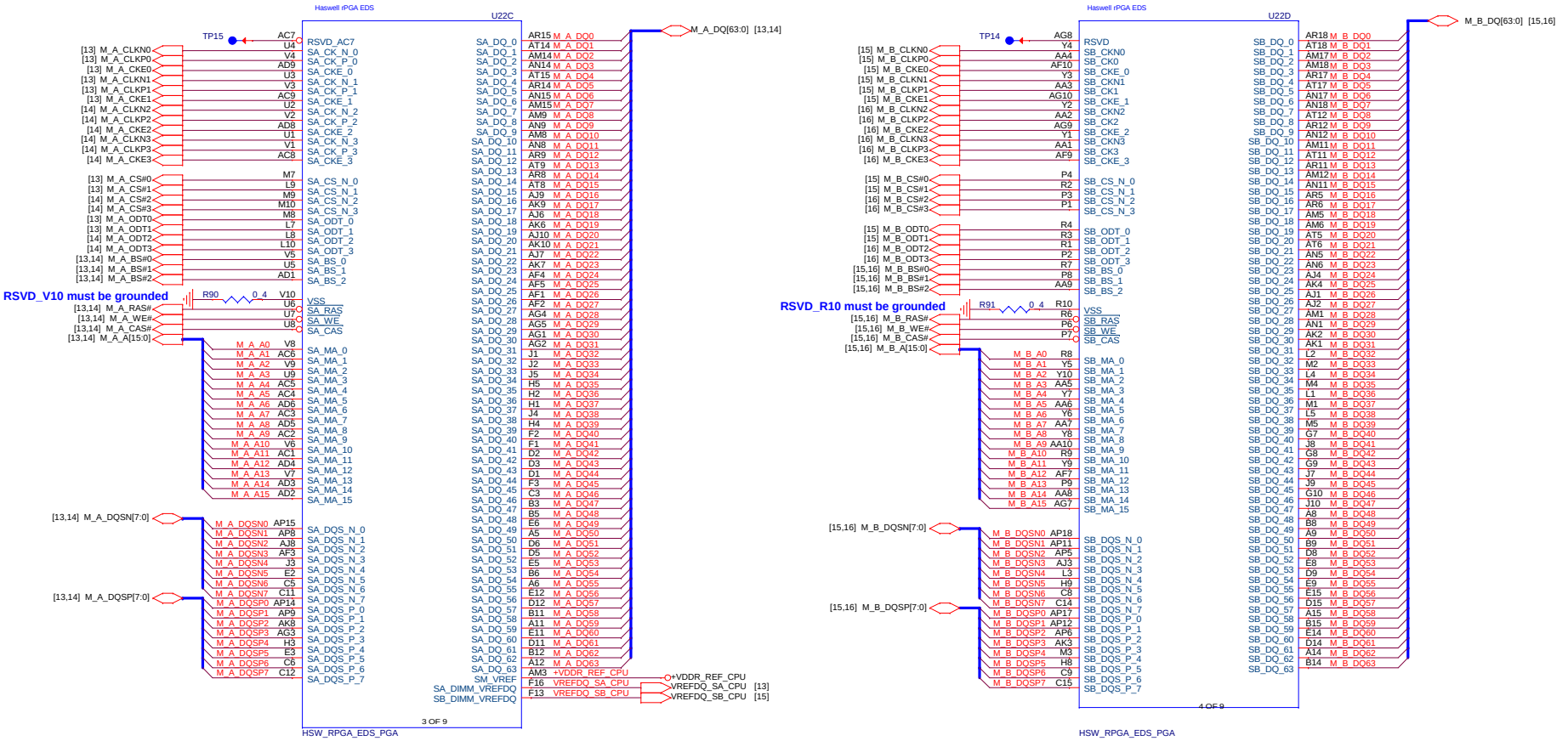


Local TEMP = 85

Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 85dgree
Hysteresis is 30C

Quanta Computer Inc.		
PROJECT : BDD		
Size	Document Number: Haswell 1/4 (PEG/DMI/FDI)	Rev: A1A
Date: Tuesday, February 05, 2013	Sheet 2 of 37	

Haswell Processor (DDR3)



Quanta Computer Inc.			
PROJECT : BDD			
Size	Document Number		Rev
	Haswell 2/4 (DDR3 I/F)		A1A
Date: Tuesday, February 05, 2013	Sheet 3 of 37		

Haswell Processor (POWER)

04

+1.35V_CPU 4.2A

+1.35V_CPU

C377 22U/6.3V_8X, C360 22U/6.3V_8X, C403 *22U/6.3V_8X, C53 *22U/6.3V_8X, C414 *22U/6.3V_8X, C359 *22U/6.3V_8X

C54 *22U/6.3V_8X, C395 *22U/6.3V_8X, C65 *22U/6.3V_8X, C48 *22U/6.3V_8X, C59 *22U/6.3V_8X

C74 10U/6.3V_6X, C376 10U/6.3V_6X, C394 *10U/6.3V_6X, C58 *10U/6.3V_6X, C73 *10U/6.3V_6X

C409 *10U/6.3V_6X, C404 *10U/6.3V_6X, C64 *10U/6.3V_6X, C410 *10U/6.3V_6X, C47 *10U/6.3V_6X

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

Haswell rPGA EDS

U22E

TP2 TP2 TP2 TP19 → K27 L27 T27 V27 RSVD

AB11 AB2 AB5 AB8 AE11 AE2 AE5 AE8 AH11 K11 N11 N8 T11 T2 T5 T8 W11 W2 W5 W8 VDDQ

TP22 TP3 TP8 → N26 K26 AL27 AK27 RSVD

+VCC_CORE

[34] VCC_SENSE → R85 0_4 → VCC_SENSE_R → AL35 VCC_SENSE; E17 RSVD

+VCC_CORE → R86 100_4

300mA +VCCIO_OUT → R72 *0_1206 → +VCCIO_OUT_R → AN35 VCCIO_OUT

+VCCIO_PCH → R120 *0_1206 → +VCCIO_PCH_R → A23 FC_A23

300mA +VCCIOA_OUT → R121 *0_1206 → +VCCIOA_OUT_R → F22 VCOMP_OUT

REV 1.0 change, depop R724

TP16 TP13 TP25 TP12 → W32 AL16 J27 AL13 RSVD

H_CPU_SVIDART# → AM28 VIDALERT

H_CPU_SVIDCLK → AM29 VIDSCLK

H_CPU_SVIDDAT → AL28 VIDSOUT

R74 0_4 → TP21 PWR_DEBUG_R → AP35 VSS; H27 PWR_DEBUG

AP34 AT35 VSS

TP57 TP58 TP56 TP5 → AR35 AR32 AL26 AT34 RSVD_TP

AL22 AT33 AM21 AM25 AM22 AM20 AM24 AL19 AM23 AT32 VSS

+VCC_CORE → Y25 Y26 Y27 Y28 Y29 Y30 Y31 Y32 Y33 Y34 Y35 VCC

5 OF 9

HSW_RPGA_EDS_PGA

+VCCIN 95A

+VCC_CORE

C413 22U/6.3V_8X, C411 22U/6.3V_8X, C397 22U/6.3V_8X, C407 22U/6.3V_8X, C396 22U/6.3V_8X, C378 22U/6.3V_8X

C363 22U/6.3V_8X, C67 22U/6.3V_8X, C362 22U/6.3V_8X, C361 22U/6.3V_8X, C406 22U/6.3V_8X, C412 22U/6.3V_8X

C398 22U/6.3V_8X, C68 22U/6.3V_8X, C51 22U/6.3V_8X, C50 22U/6.3V_8X, C49 22U/6.3V_8X, C66 22U/6.3V_8X

C76 22U/6.3V_8X, C55 10U/6.3V_6X, C60 10U/6.3V_6X, C75 10U/6.3V_6X, C57 10U/6.3V_6X, C56 10U/6.3V_6X

C61 10U/6.3V_6X, C62 10U/6.3V_6X, C77 10U/6.3V_6X, C405 10U/6.3V_6X, C379 10U/6.3V_6X, C380 10U/6.3V_6X

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

Power Test Propose

+1.05V → R92 150_4 → PWR_DEBUG_R → R93 *10K_4

REV 1.0 change Pop R741

+1.05V → R69 *0_8 → +VCCIO_OUT → C45 *4.7U/6.3V_6X

MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

+1.05V → R126 0_6 → +VCCIO_PCH → C95 *4.7U/6.3V_6X

REV 1.0 change Pop R16059

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

+VCCIO_OUT → R65 130/F_4

Place PU resistor close to CPU

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

H_CPU_SVIDDAT → R64 0_4 → VR_SVIDDAT [34]

+VCCIO_OUT → R66 75/F_4

Place PU resistor close to CPU

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

H_CPU_SVIDART# → R67 43_4 → VR_SVIDART# [34]

H_CPU_SVIDCLK → R68 0_4 → VR_SVIDCLK [34]

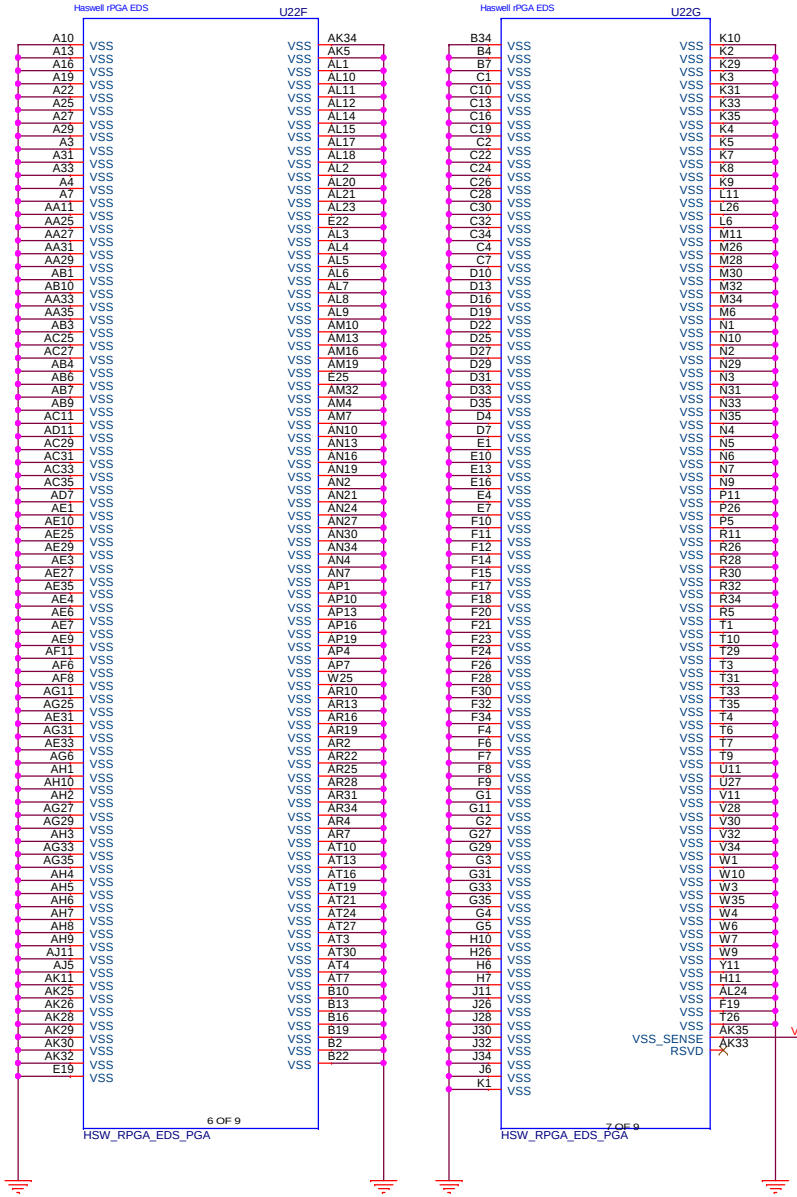
Quanta Computer Inc.

PROJECT : BDD

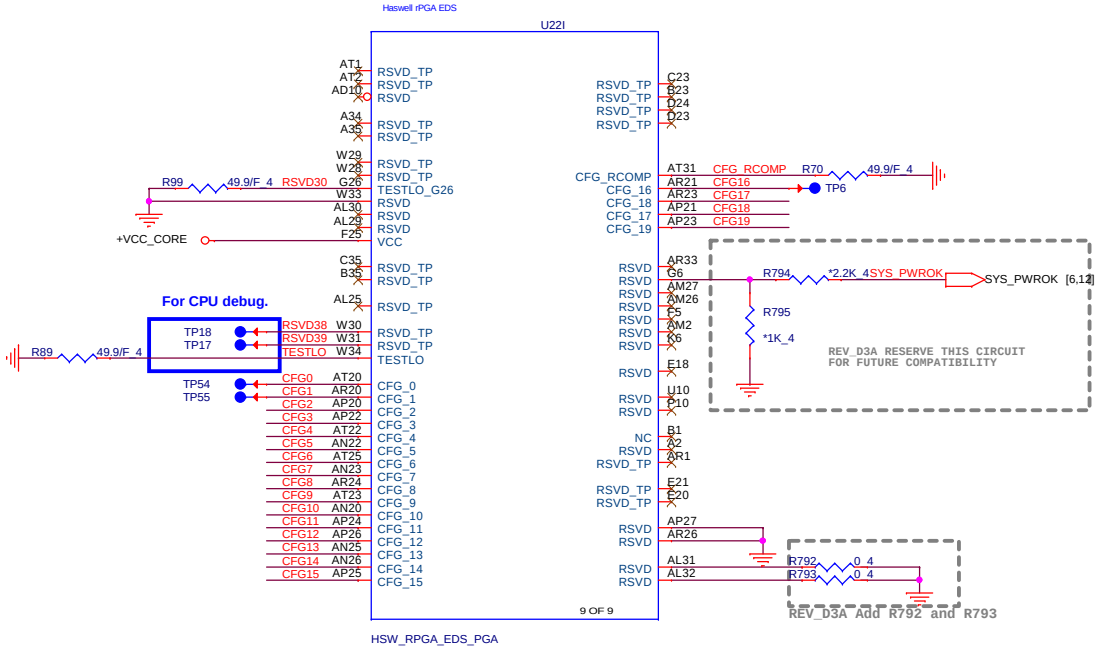
Size	Document Number	Rev
	Haswell 3/4 (POWER)	A1A

Date: Tuesday, February 05, 2013 Sheet 4 of 37

Haswell Processor (GND)



Haswell Processor (CFG,RSVD)



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R56 *1K_4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R57 PIV@1K_4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R60 *1K_4 CFG5 R58 *1K_4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	CFG7 R59 *1K_4

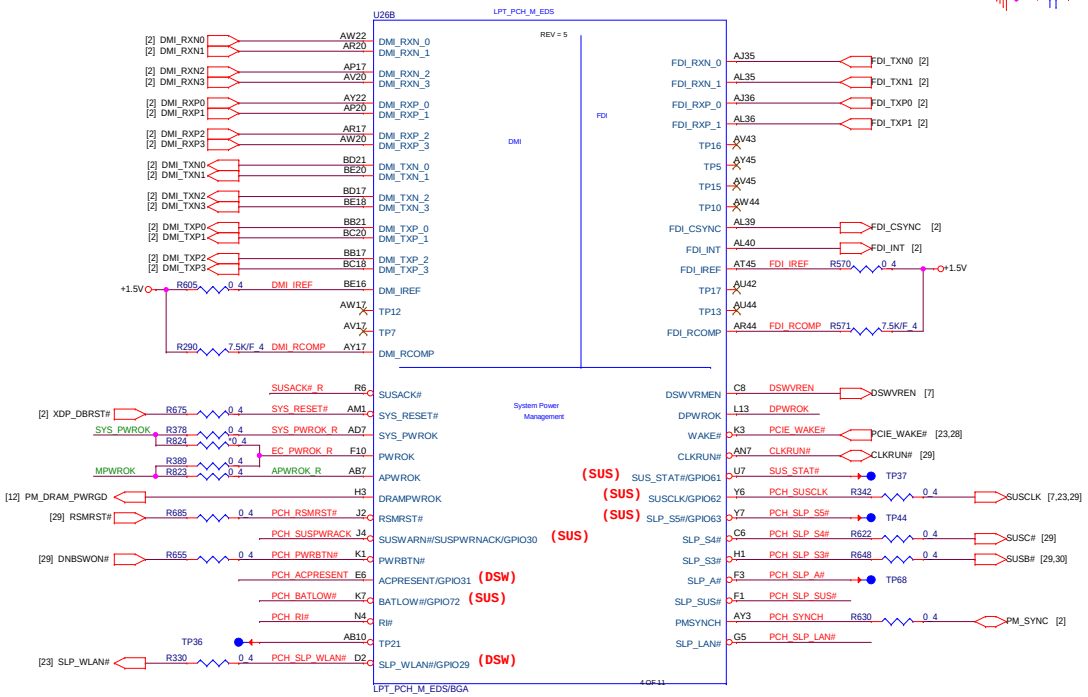
Quanta Computer Inc.

PROJECT : BDD

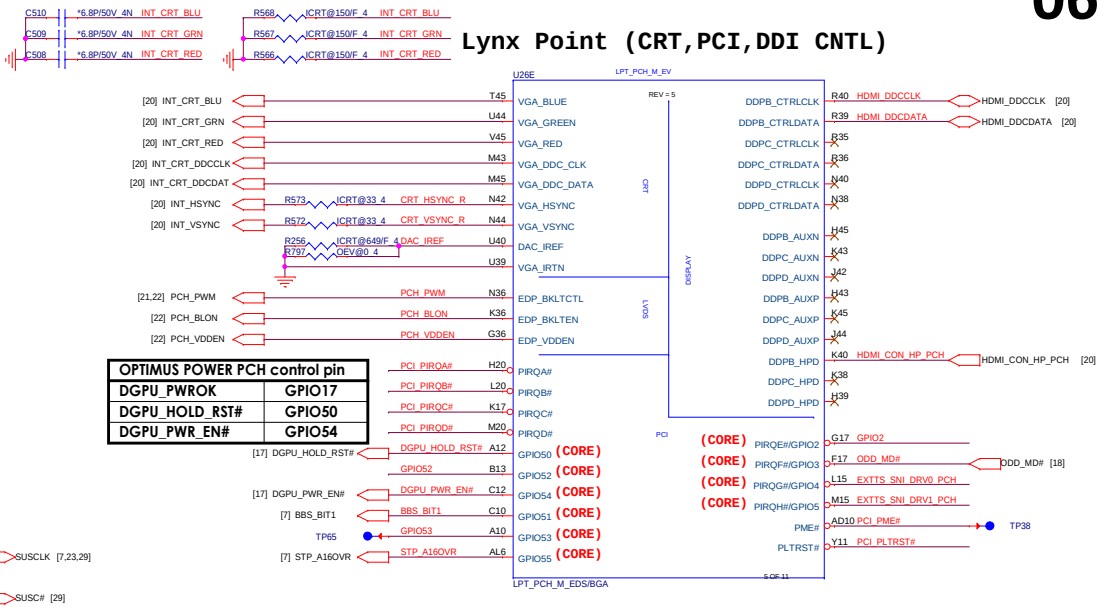
Size	Document Number	Rev
	Haswell 4/4 (CFG/GND)	A1A
Date: Tuesday, February 05, 2013	Sheet 5 of 37	

06

Lynx Point (DMI,FDI,PM)

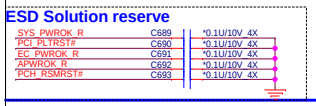


Lynx Point (CRT,PCI,DDI CNTL)

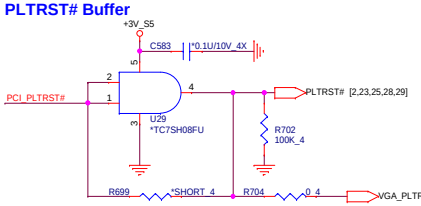


OPTIMUS POWER PCH control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

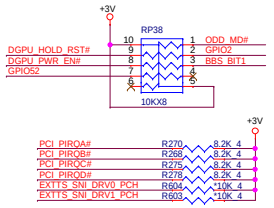
ESD Solution reserve



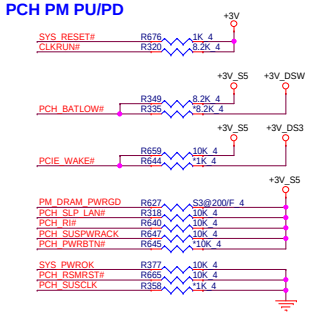
PLTRST# Buffer



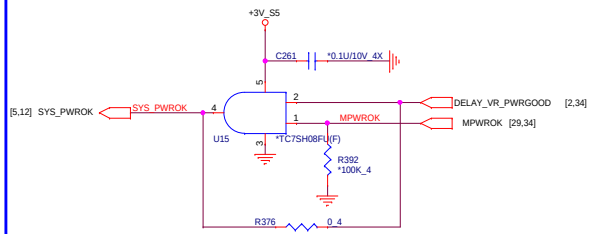
PCI PU



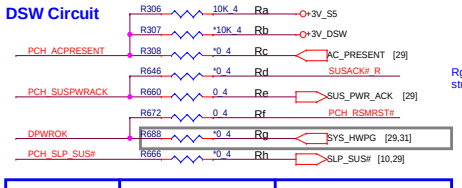
PCH PM PU/PD



SYSPWOK

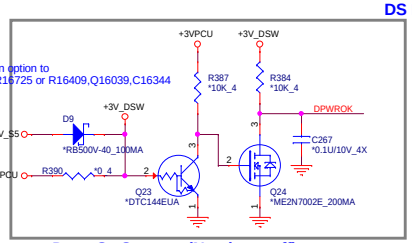


DSW Circuit

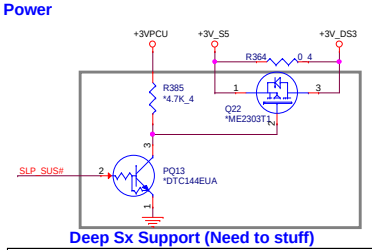


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

DS Power



Deep Sx Support (Need to stuff)



Deep Sx Support (Need to stuff)

Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	A1A

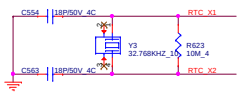
Date: Tuesday, February 05, 2013 Sheet 6 of 37

Lynx Point (RTC,IHDA,SATA,JTAG)

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

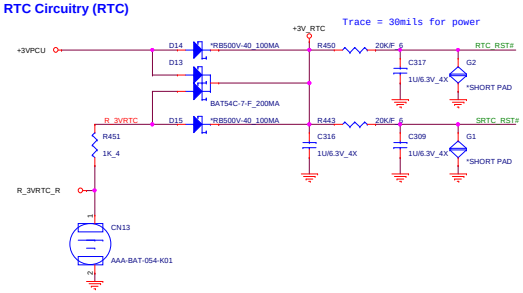
07

RTC Clock 32.768KHz (RTC)

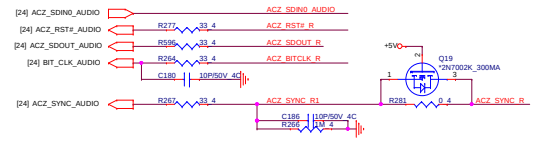


RTC Circuitry (RTC)

Trace = 30mils for power

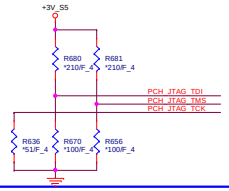


HDA



PCH JTAG

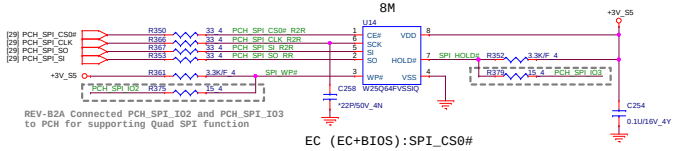
JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



PCH SPI

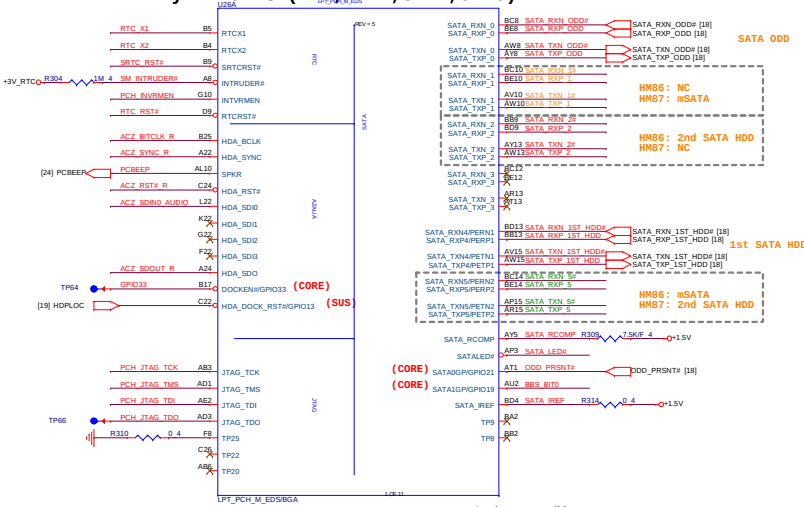
CLG

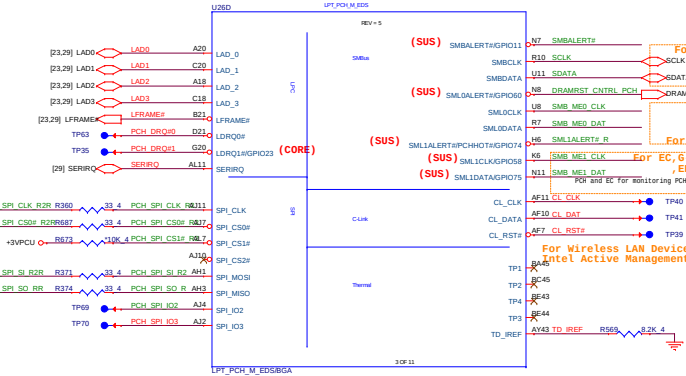
Change to single 8M SPI.20121017

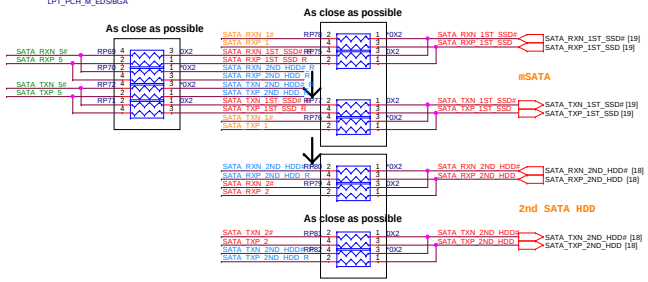


REV-B2A Connected PCH_SPI_IO2 and PCH_SPI_IO3 to PCH for supporting Quad SPI function

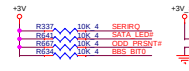
EC (EC+BIOS):SPI_CS0#



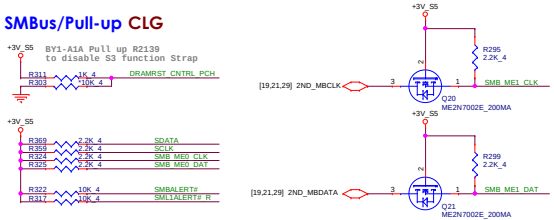




CLG



SMBus/Pull-up CLG



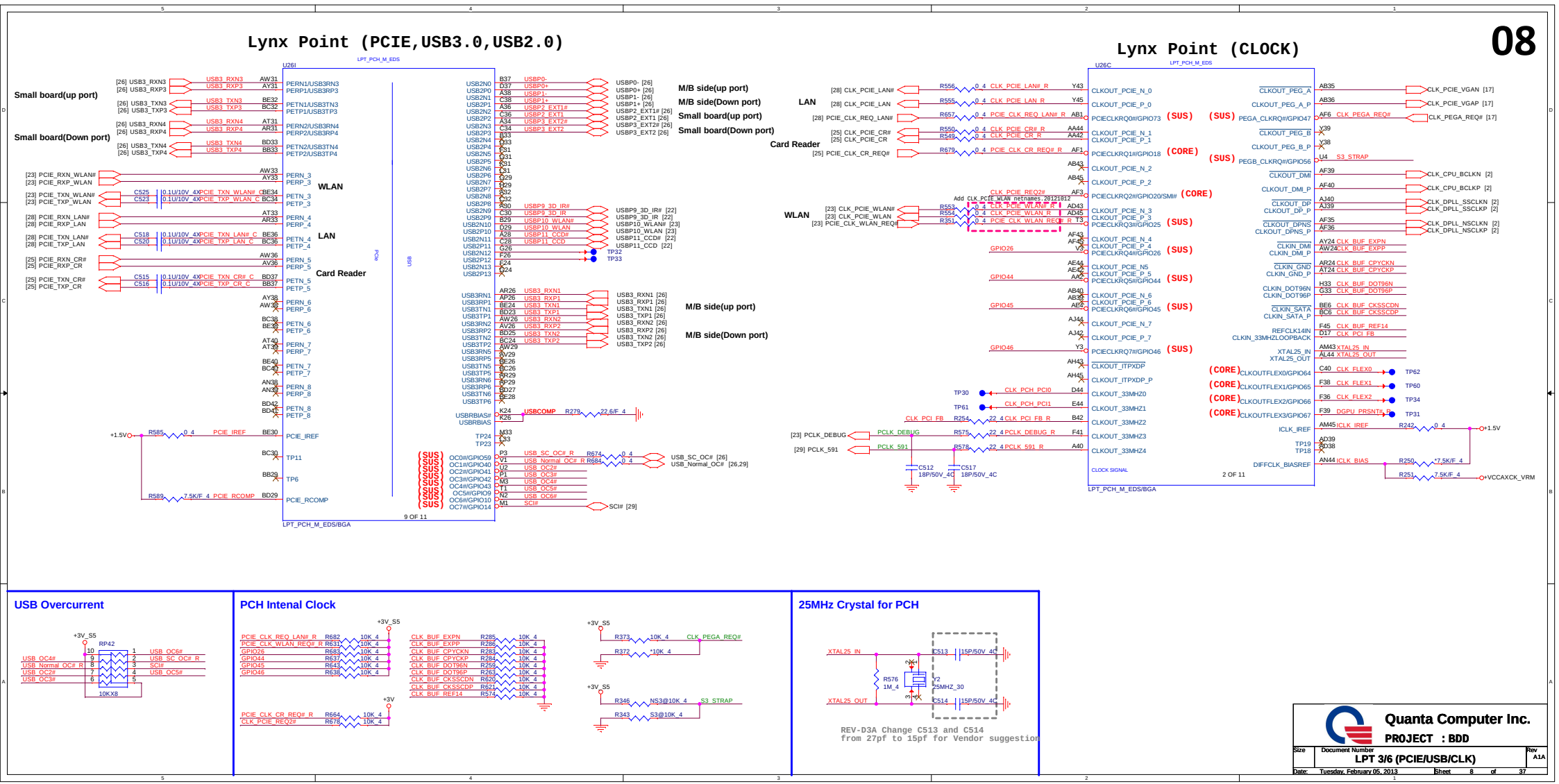
PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R363 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	[6,23,29] SUSCLK R357 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	[6] STP_A16OVR R315 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R319 330K_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	[6] BBS_BIT1 R294 *1K_4 BBS_BIT0 R635 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	[29] ACZ_SDOUT R590 *1K_4 +VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	[9] GPIO36 R669 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	[9] FDI_OVRVLTG R672 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	[9] GPIO8 R658 10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	[9] PLL_ODVR_EN R309 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	[6] DSWVREN R614 330K_4 R615 330K_4 +3V_RTC

Check list V1.0 Removed the GPIO28 signal information of PLL VR enable signal

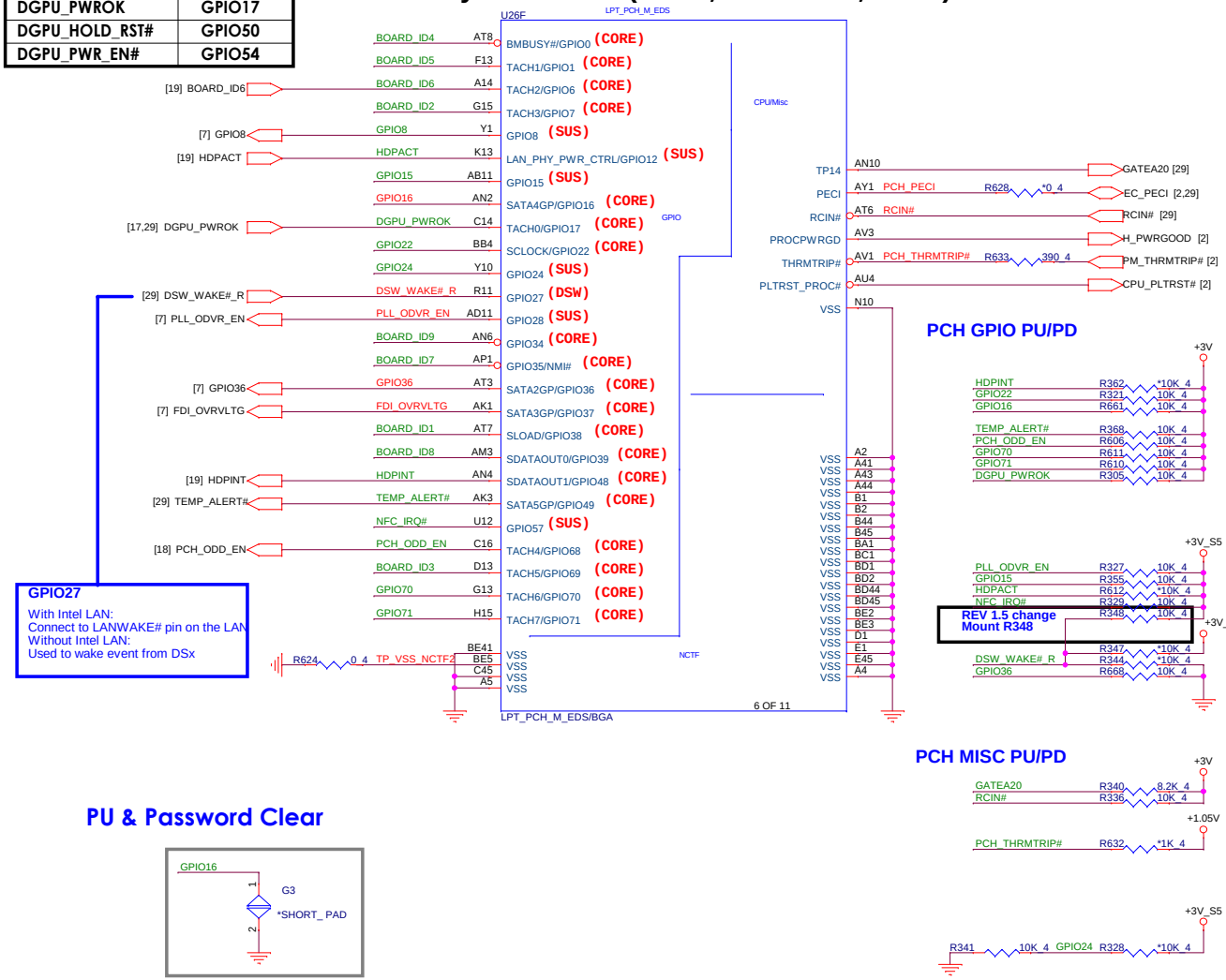
Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	A1A
Date: Tuesday, February 05, 2013	Sheet 7 of 37	



OPTIMUS POWER PCH control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

Lynx Point (GPIO,CPU/MISC,NCTF)



GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

PCH GPIO PU/PD

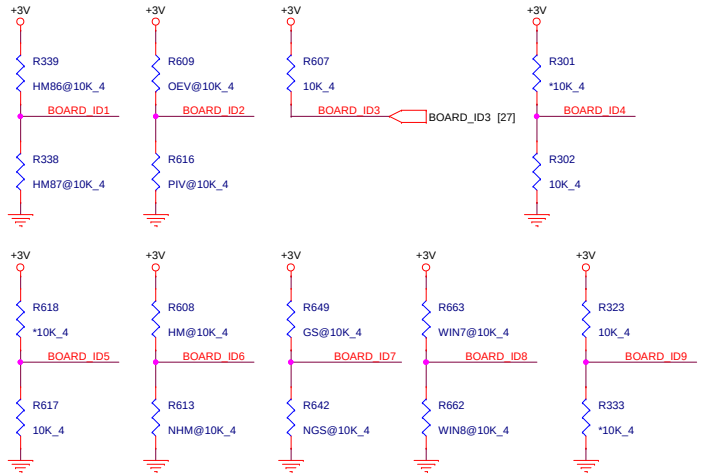
PCH MISC PU/PD

PU & Password Clear

Change G3 for Clear CMOS password from GPIO21 to GPIO16

BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
ChiefRiver Shark Bay				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
ECO Mode 3D Mode									H L			
										H L		
											H L	
												H L

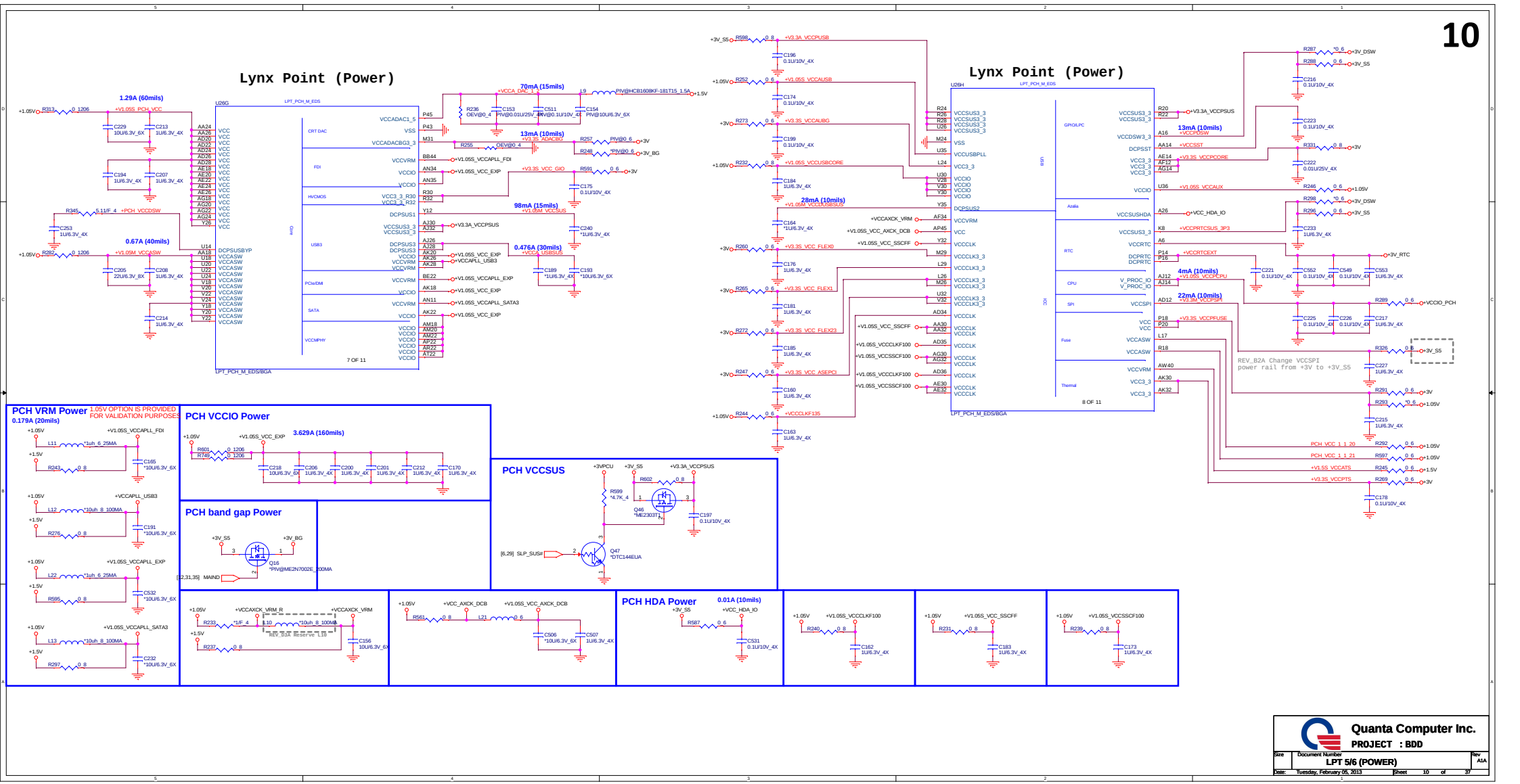


09

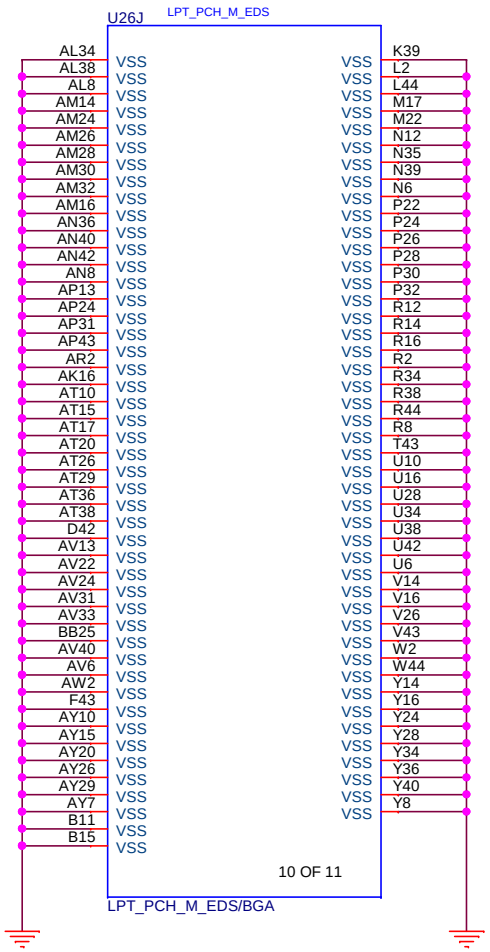
Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	A1A

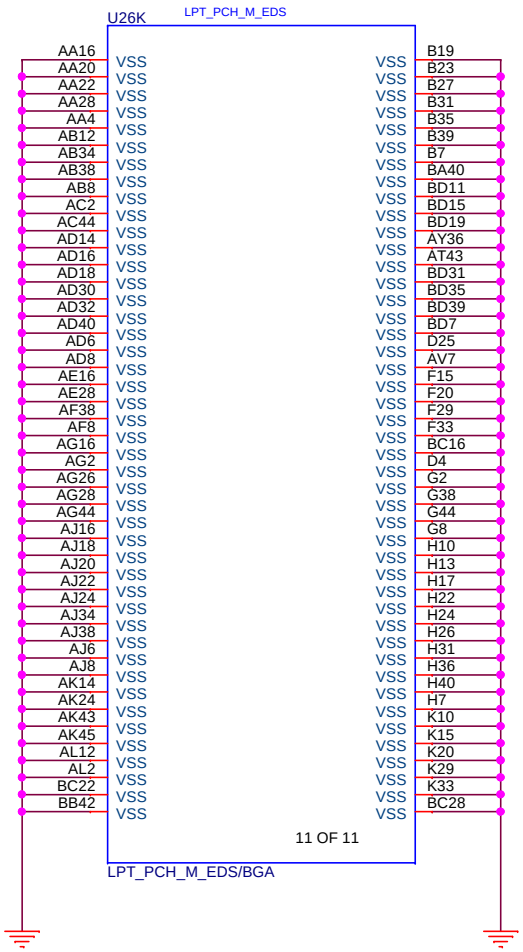
Date: Tuesday, February 05, 2013 Sheet 9 of 37



Lynx Point (GND)

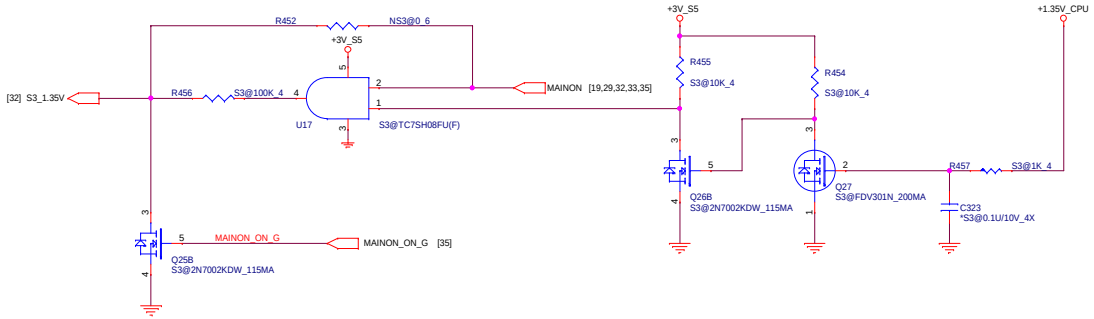


Lynx Point (GND)

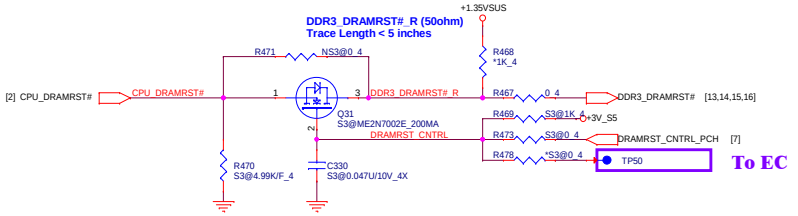


Quanta Computer Inc.		
PROJECT : BDD		
Size	Document Number: LPT 6/6 (GND)	Rev: A1A
Date: Tuesday, February 05, 2013	Sheet 11 of 37	

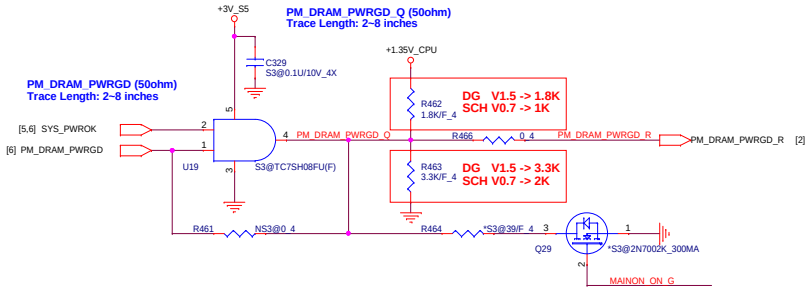
For S3 power Reduction Sequence S3P/NS3P/CPU



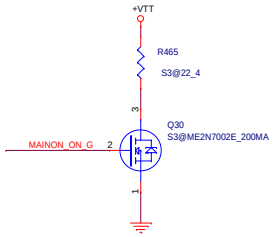
SM_DRAMRST# Topology S3P/NS3P/CPU



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

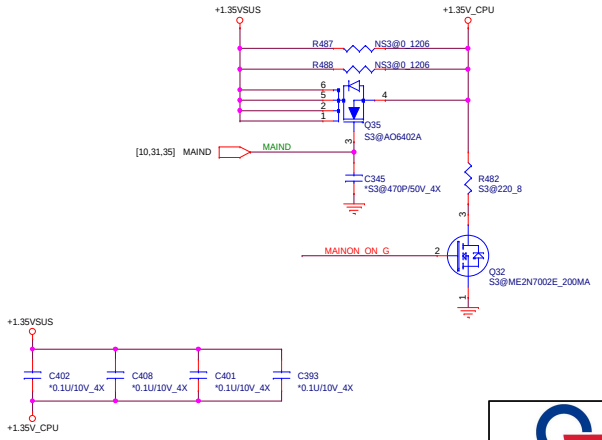


For S3 power Reduction VTT discharge S3P/NS3P/CPU



CPU SM_VREF S3P/NS3P/CPU

S3 power Reduction (CPU Power) S3P/NS3P/CPU

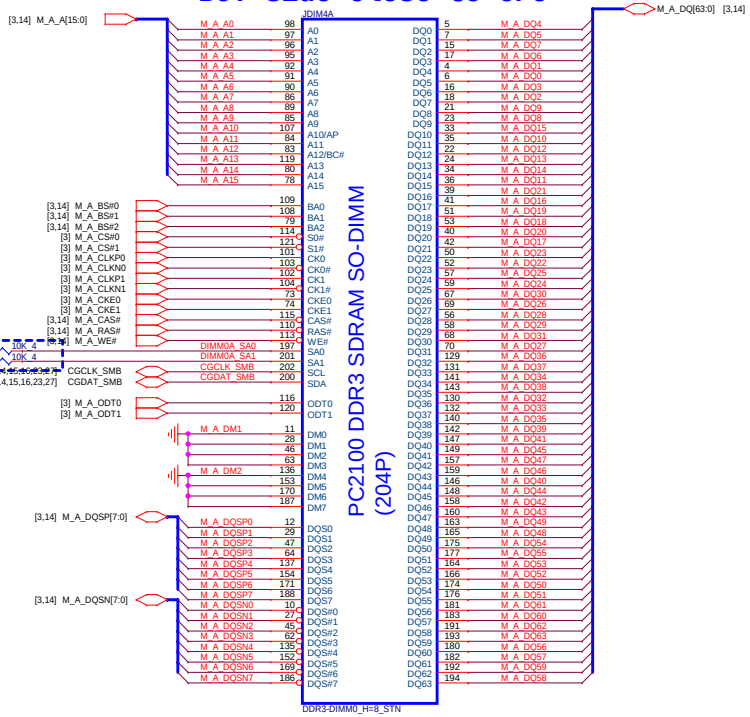


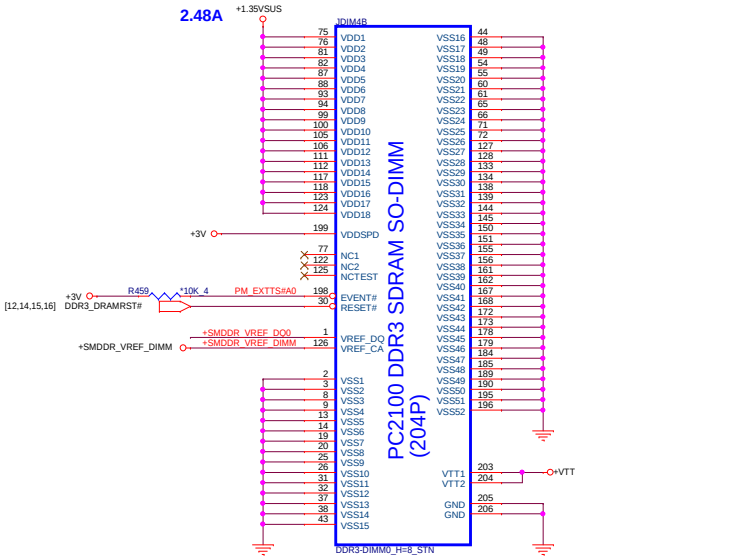
Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	S3 Power Reduction	A1A
Date: Tuesday, February 05, 2013	Sheet 12 of 37	

BOT Side Close to CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

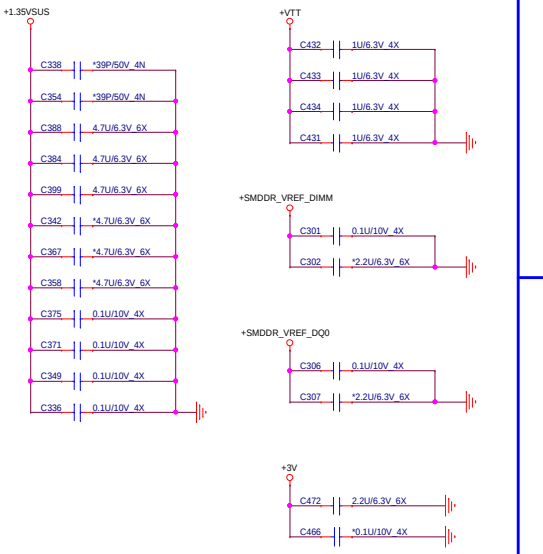




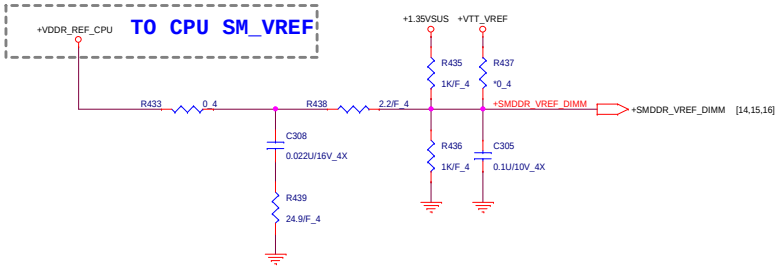
[2,6,7,8,9,10,14,15,16,17,18,19,20,21,22,23,25,27,29,31,35] +3V

[12,14,15,16,32] +VTT

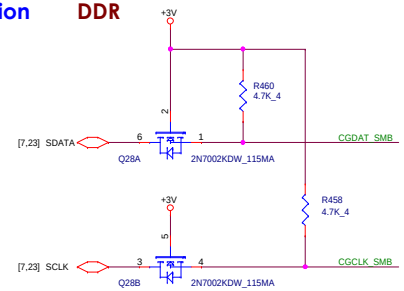
Place these Caps near So-Dimm0.



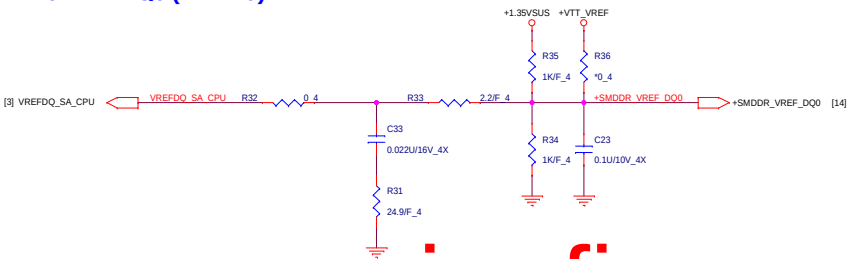
DDR3 VREF CA DDR



SMBus Isolation DDR



DDR3 VREF DQ0 (M1+M3) DDR

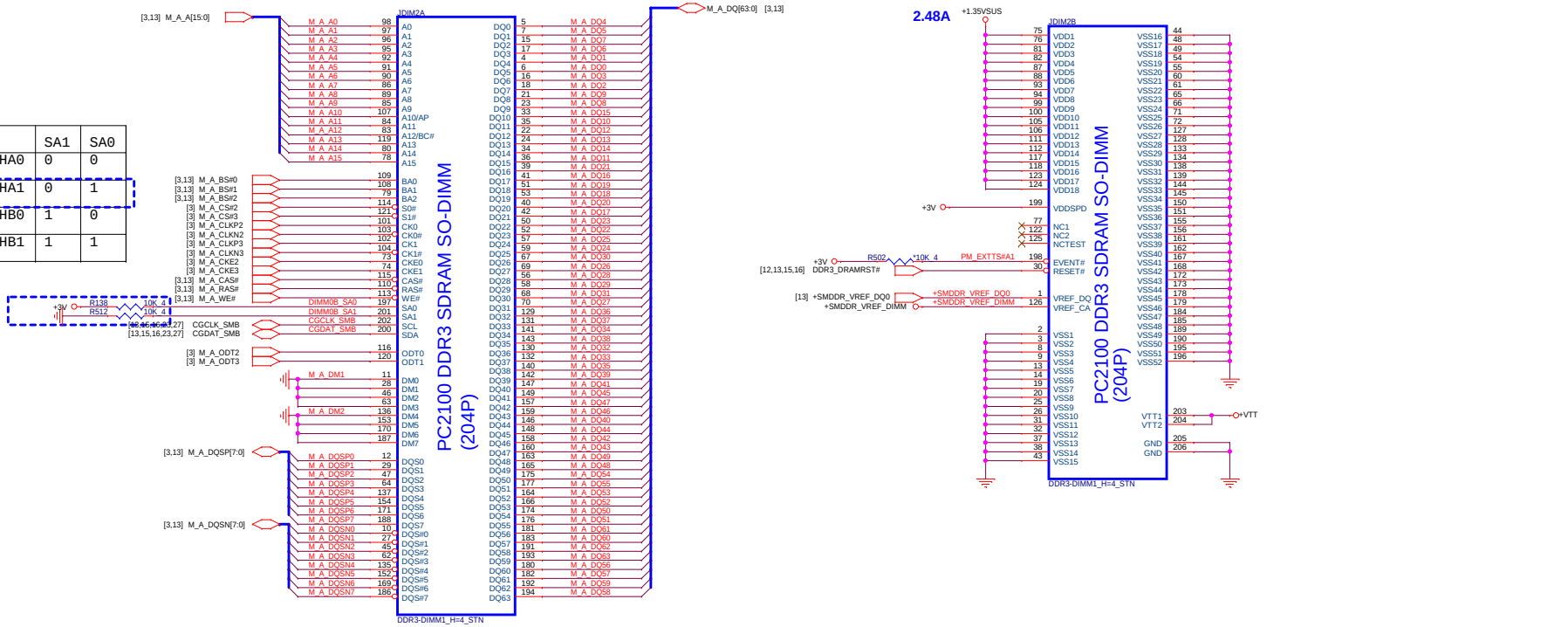


Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	System Memory A0 STD (8H)	A1A
Date: Tuesday, February 05, 2013	Sheet 13 of 37	

TOP Side Close to CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

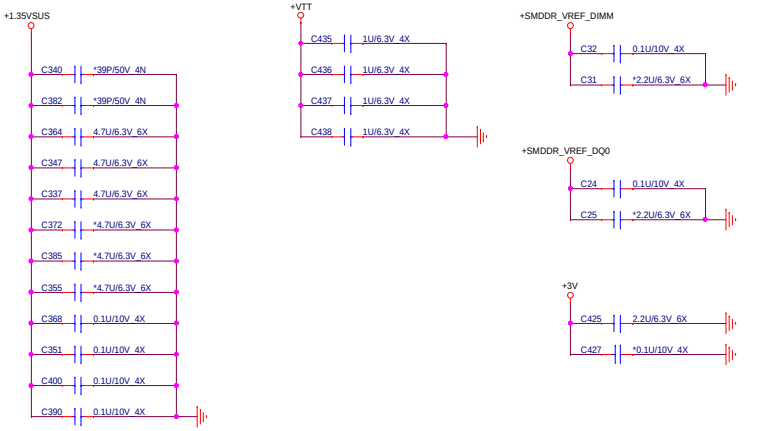


[2,6,7,8,9,10,13,15,16,17,18,19,20,21,22,23,25,27,29,31,35] +3V

[12,13,15,16,32] +VTT

[13,15,16] +SMDDR_VREF_DIMM

Place these Caps near So-Dimm0.



Quanta Computer Inc.

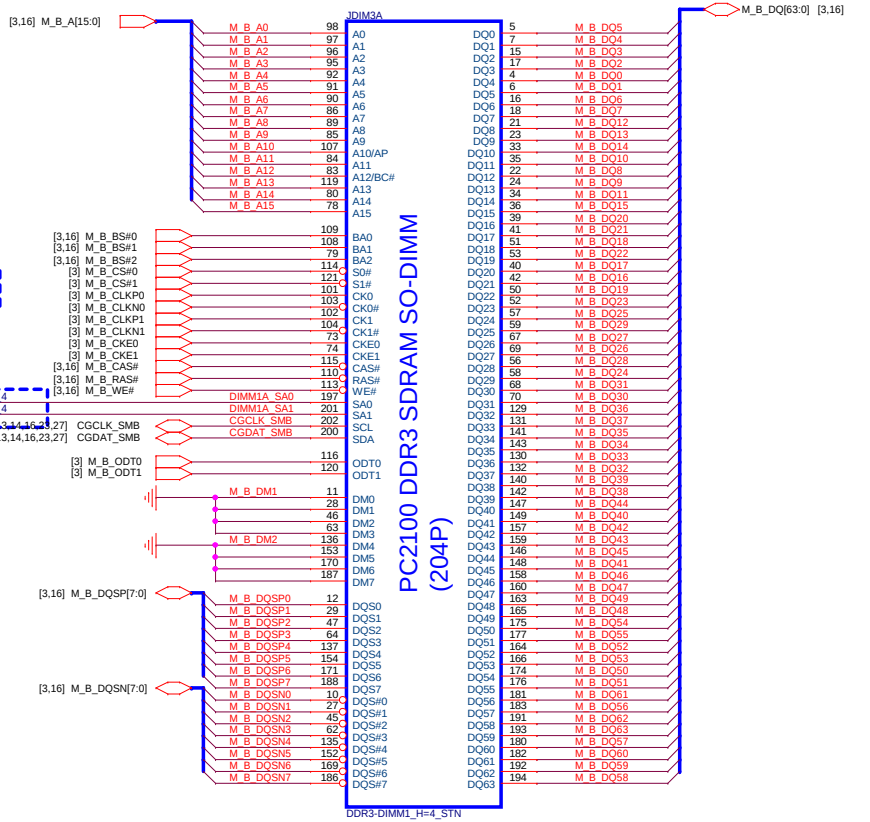
PROJECT : BDD

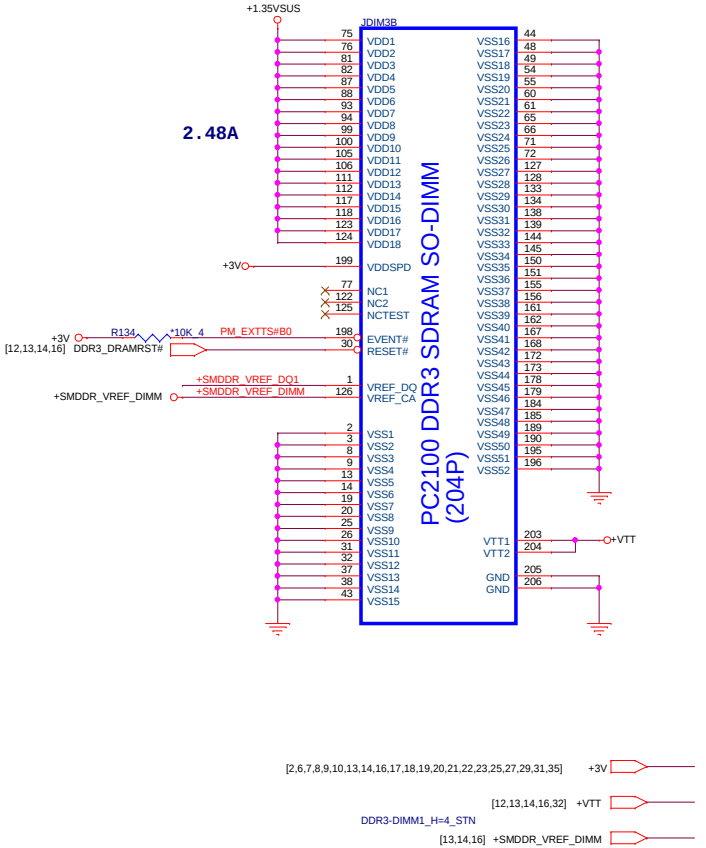
Size	Document Number	Rev
	System Memory A1 STD (4H)	A1A

Date: Tuesday, February 05, 2013 Sheet 14 of 37

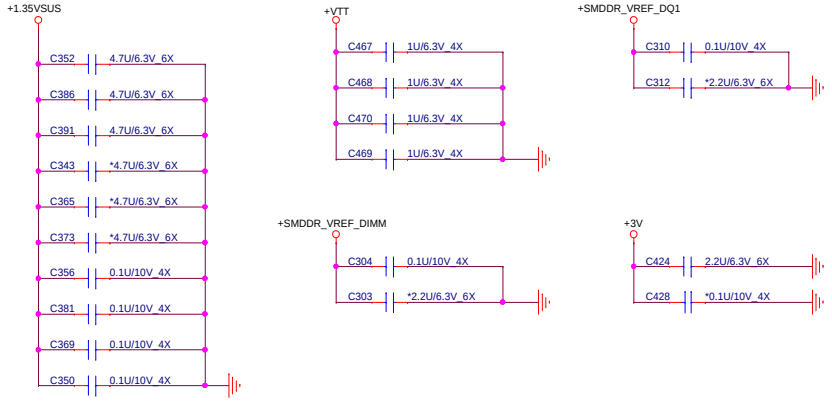
BOT Side Far away CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

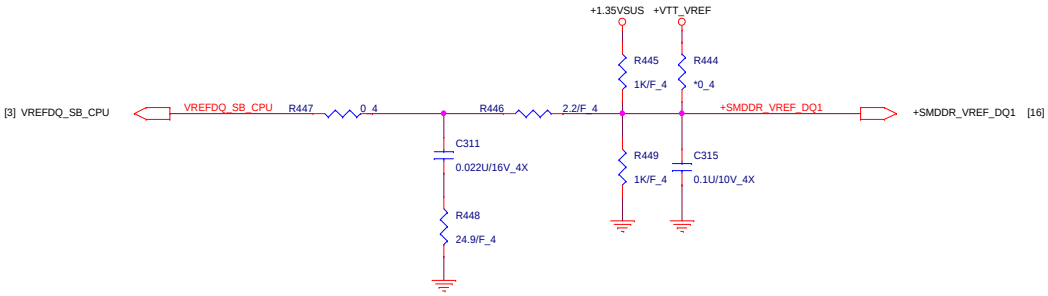




Place these Caps near So-Dimm1.



DDR3 VREF DQ1 (M1+M3) DDR

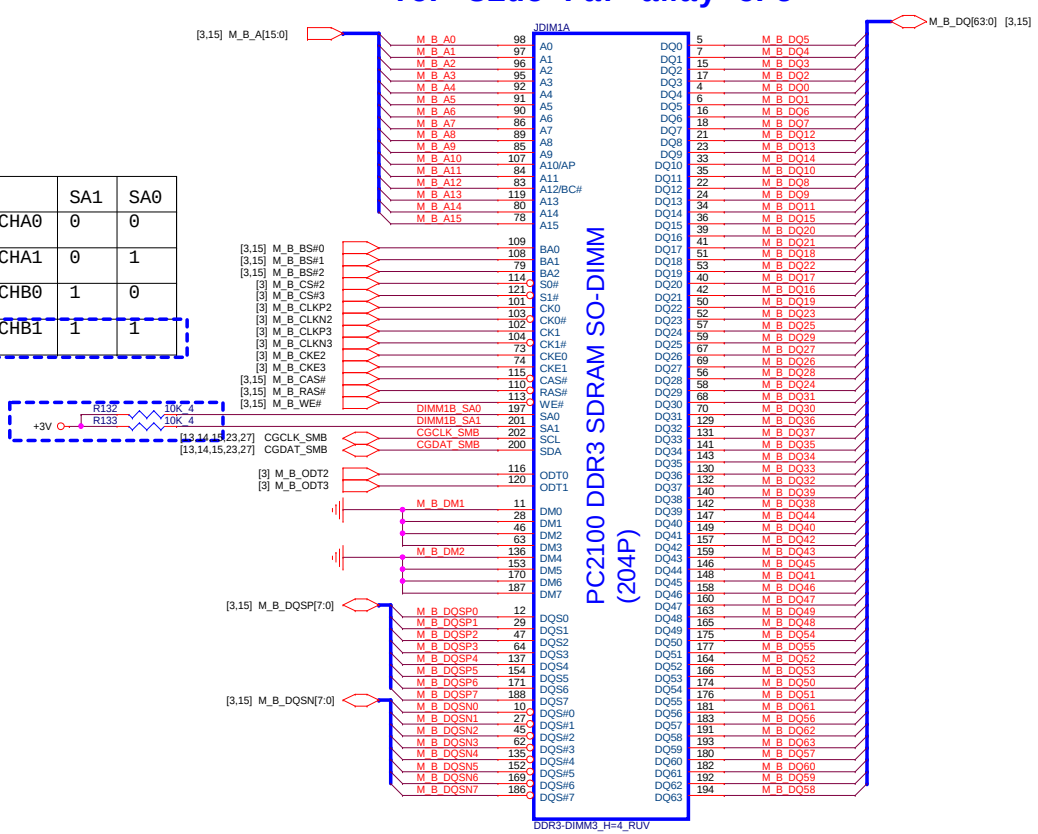


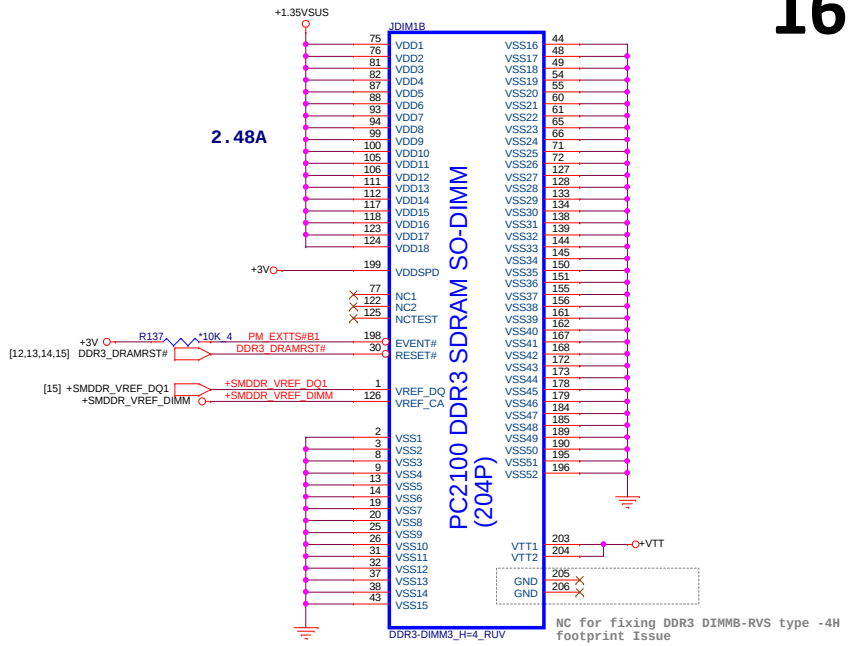
Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	System Memory B0 STD (4H)	A1A
Date: Tuesday, February 05, 2013	Sheet 15 of 37	

TOP Side Far away CPU

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



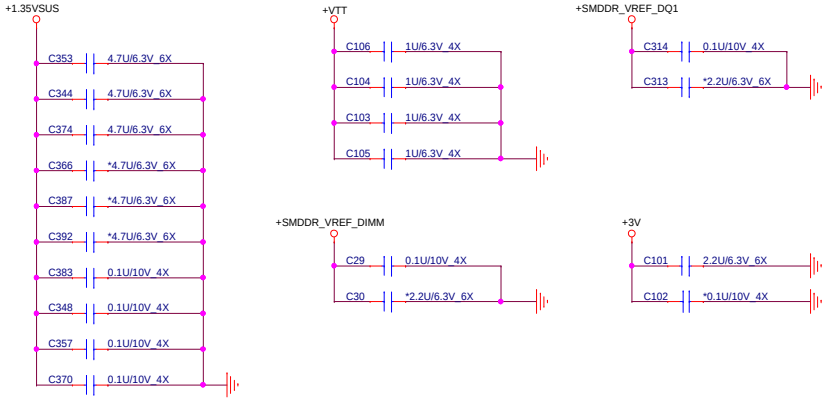


[2,6,7,8,9,10,13,14,15,17,18,19,20,21,22,23,25,27,29,31,35] +3V

[12,13,14,15,32] +VTT

[13,14,15] +SMDDR_VREF_DIMM

Place these Caps near So-Dimm1.



Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	System Memory B1 RVS (4H)	A1A

Date: Tuesday, February 05, 2013 Sheet 16 of 37

MXM 3.0

REV-B2A Change Footprint to mxm-106322be75c-314p

PWR_SRC(10A)--7-20V
5VS(2.5A)--5V
3VS(2A)--3V

N14E-GS GPU +VIN power (5A)

GPU +5V power (2.5A)

PEX_STD_SW=	Low swing	Unstuff
	High swing	Stuff

GPU +3V power (2A)

DisplayPort	DVI/HDMI
DP_x_L0	TX_x_D2
DP_x_L0#	TX_x_D2#
DP_x_L1	TX_x_D1
DP_x_L1#	TX_x_D1#
DP_x_L2	TX_x_D0
DP_x_L2#	TX_x_D0#
DP_x_L3	TX_x_CLK
DP_x_L3#	TX_x_CLK#
DP_x_AUX	DDC_x_CLK
DP_x_AUX#	DDC_x_DATA

OPTIMUS POWER PCH control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN#	GPIO54

SMBUS power plane isolate

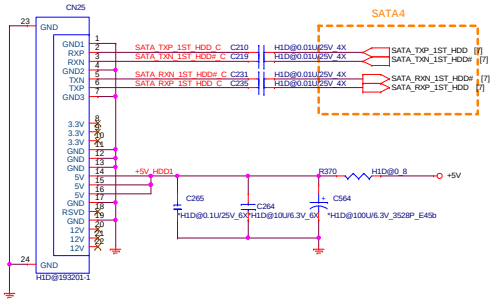
VGA Power Enable Reverse (Intel --> Low Active)

Platform Reset

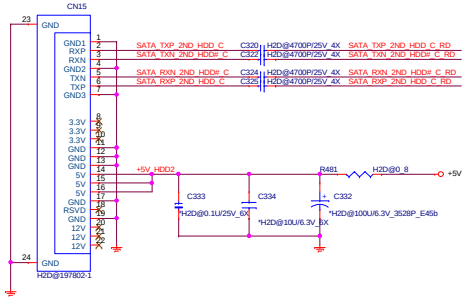
PEG (CLK_REQ)

Quanta Computer Inc.
PROJECT : BDD
Size | Document Number: MXM CONN | Rev: A1A
Date: Tuesday, February 05, 2013 | Sheet 17 of 37

HDD Interface <H1D> <H2D> [Connector Checked]



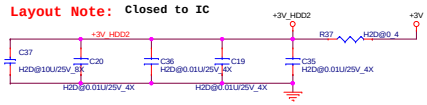
Primary HDD(H3.2)

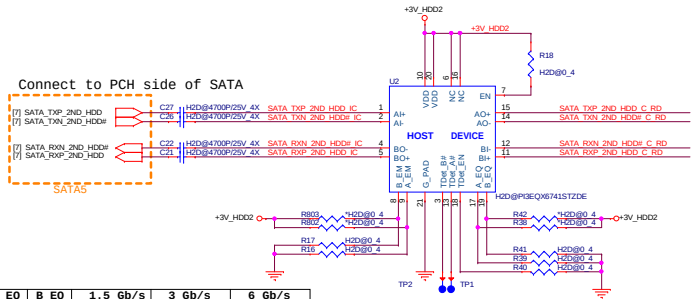


Secondary HDD(H7.8)

2nd HDD SATA Re-driver

Layout Note: Closed to IC



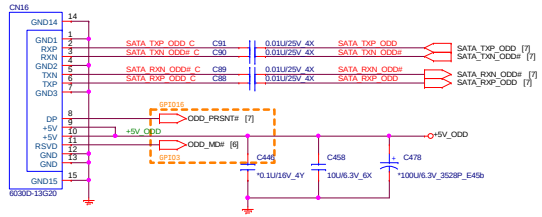


A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

ODD Interface <ODD>

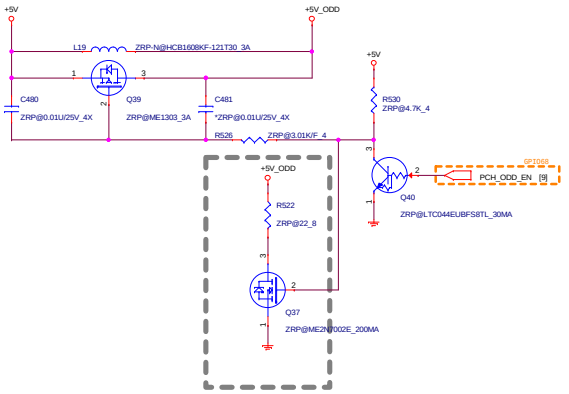
[Connector Checked]



REV_C Change footprint to sata-c185n1-11309-l-13p-r

ODD (H2.4)

ODD Zero Power <OZP>

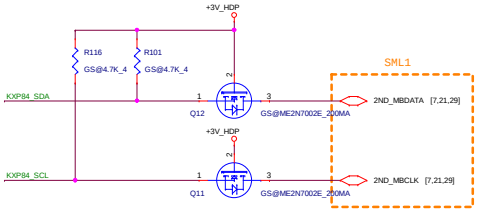


REV-B2A Fix ODD power discharge timing issue

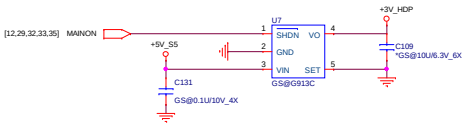
Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	HDD/ODD/G-sensor	A1A
Date: Tuesday, February 05, 2013	Sheet 18 of 37	

3D-SMBus <GSR>



3D-LDO Power <GSR>



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

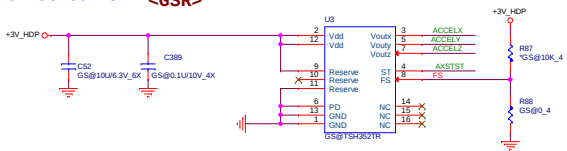
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

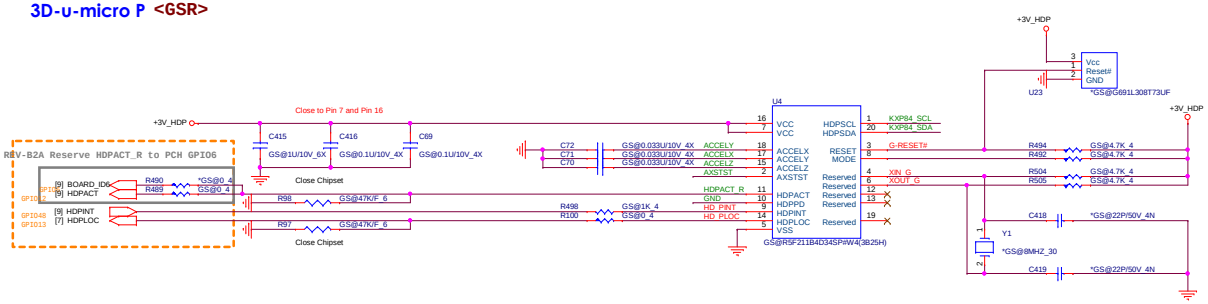
HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

3D-Sensor IC <GSR>



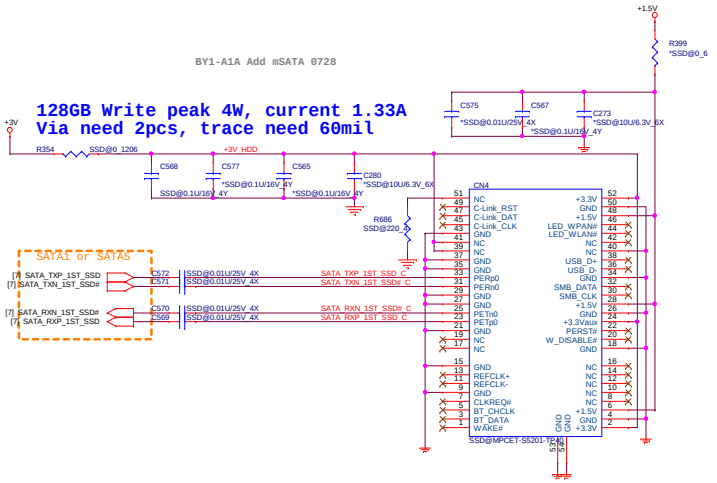
3D-u-micro P <GSR>



mSATA <SSD> [Connector Checked]

BY1-A1A Add mSATA 0728

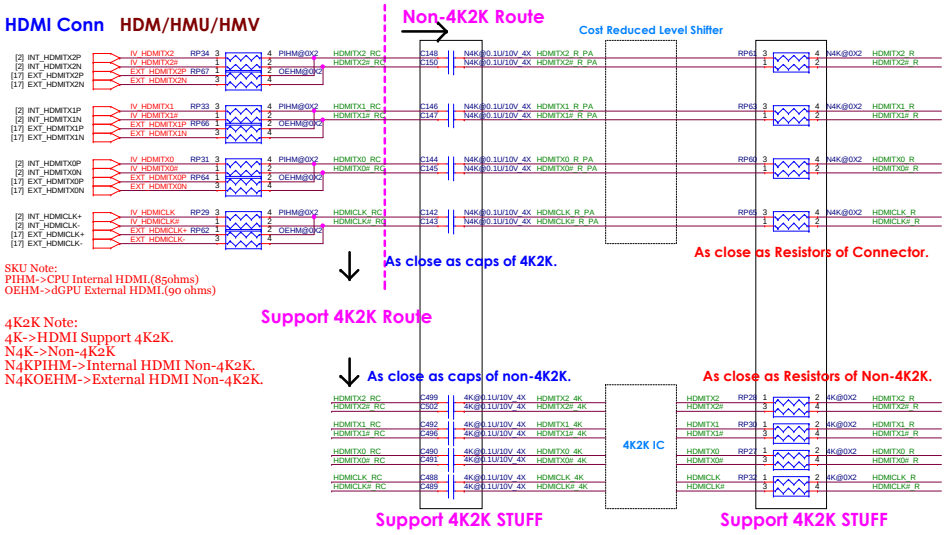
128GB Write peak 4W, current 1.33A
Via need 2pcs, trace need 60mil



Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	MINI PCIE CONN/LED	A1A
Date: Tuesday, February 05, 2013	Sheet 19 of 37	

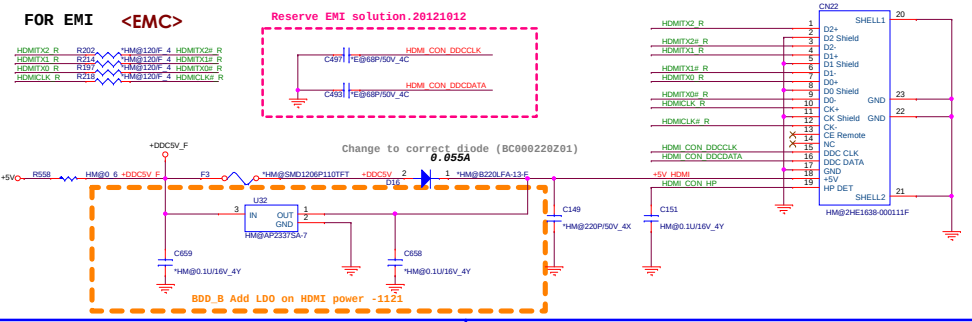
HDMI Conn HDM/HMU/HMV



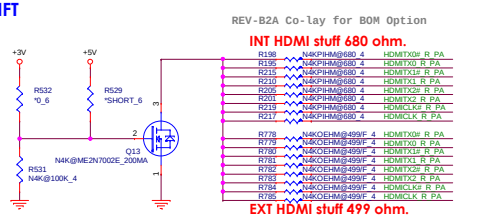
SKU Note:
PIHM->CPU Internal HDMI.(85ohms)
OEHM->dGPU External HDMI.(90 ohms)

4K2K Note:
4K->HDMI Support 4K2K.
N4K->Non-4K2K
N4KPIHM->Internal HDMI Non-4K2K.
N4KOEHM->External HDMI Non-4K2K.

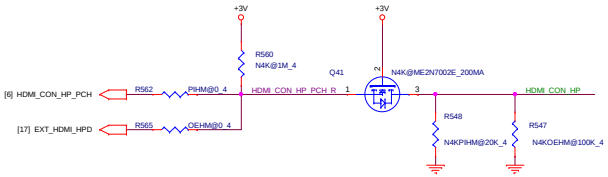
FOR EMI <EMC>



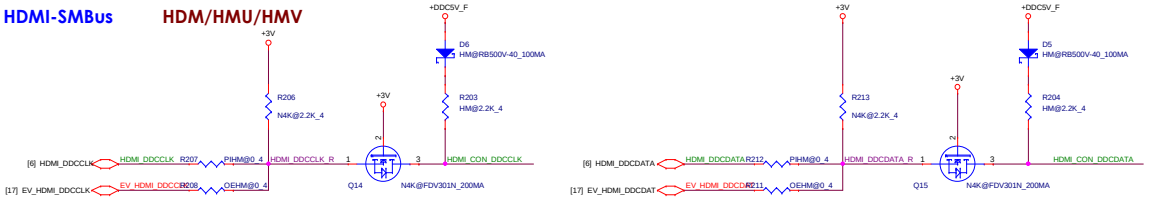
HDMI LEVEL SHIFT HDM/HMU/HMV Non-4K2K STUFF



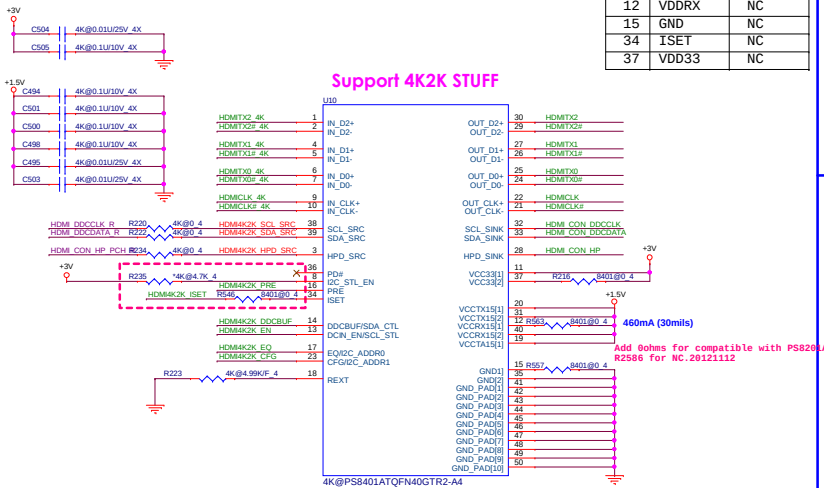
HDMI-HPD HDM/HMU/HMV



HDMI-SMBus HDM/HMU/HMV

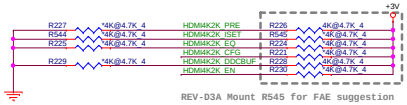


HDMI RPT



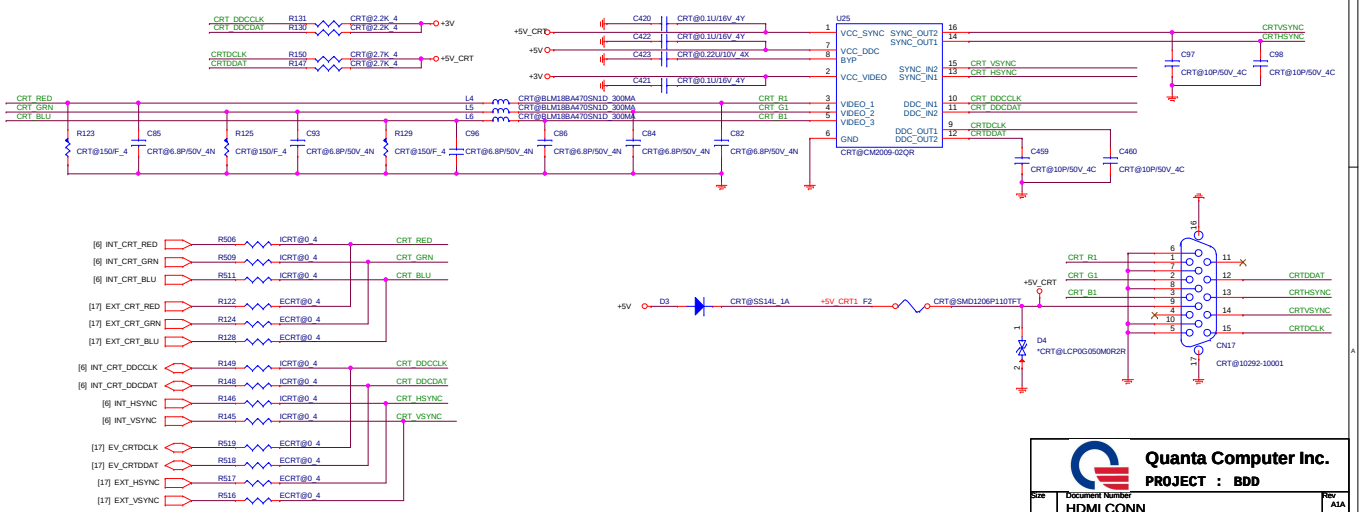
Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A



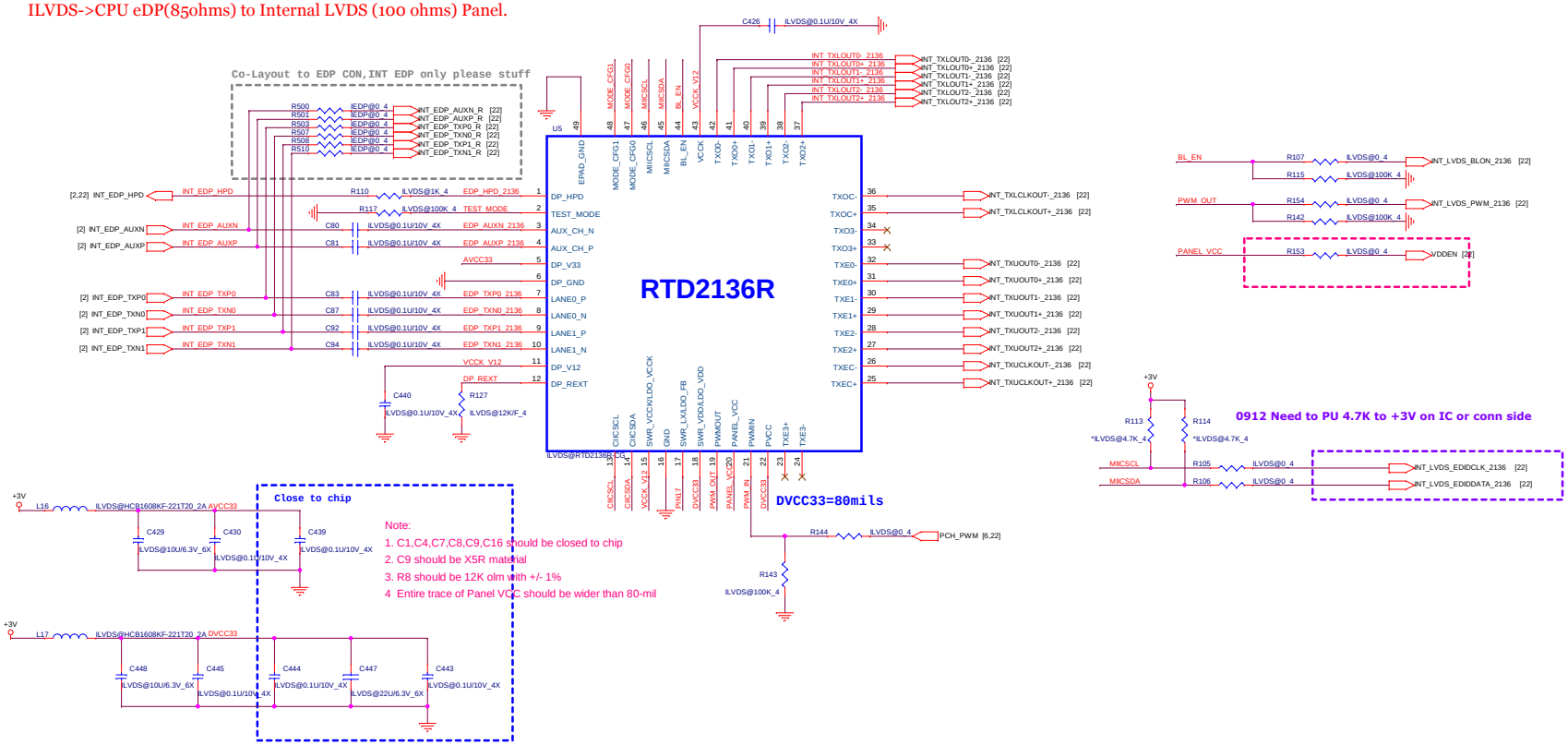
Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

CRT CRT/CRU/CRV



Quanta Computer Inc.
PROJECT : BDD
Size: Document Number: HDMI CONN Rev: A1A
Date: Tuesday, February 05, 2013 Sheet 20 of 37

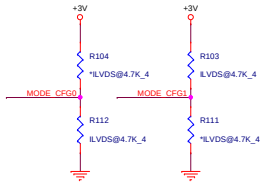
SKU Note:
ILVDS->CPU eDP(85ohms) to Internal LVDS (100 ohms) Panel.



Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

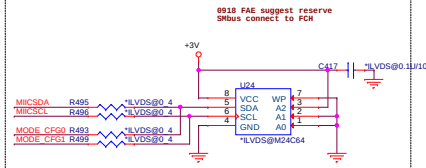
ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

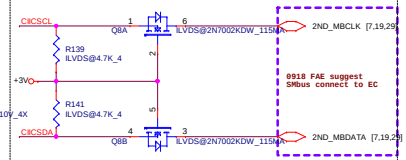
1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8



I2C address=0xA8

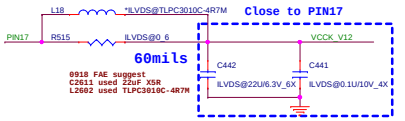
EP Mode

External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used



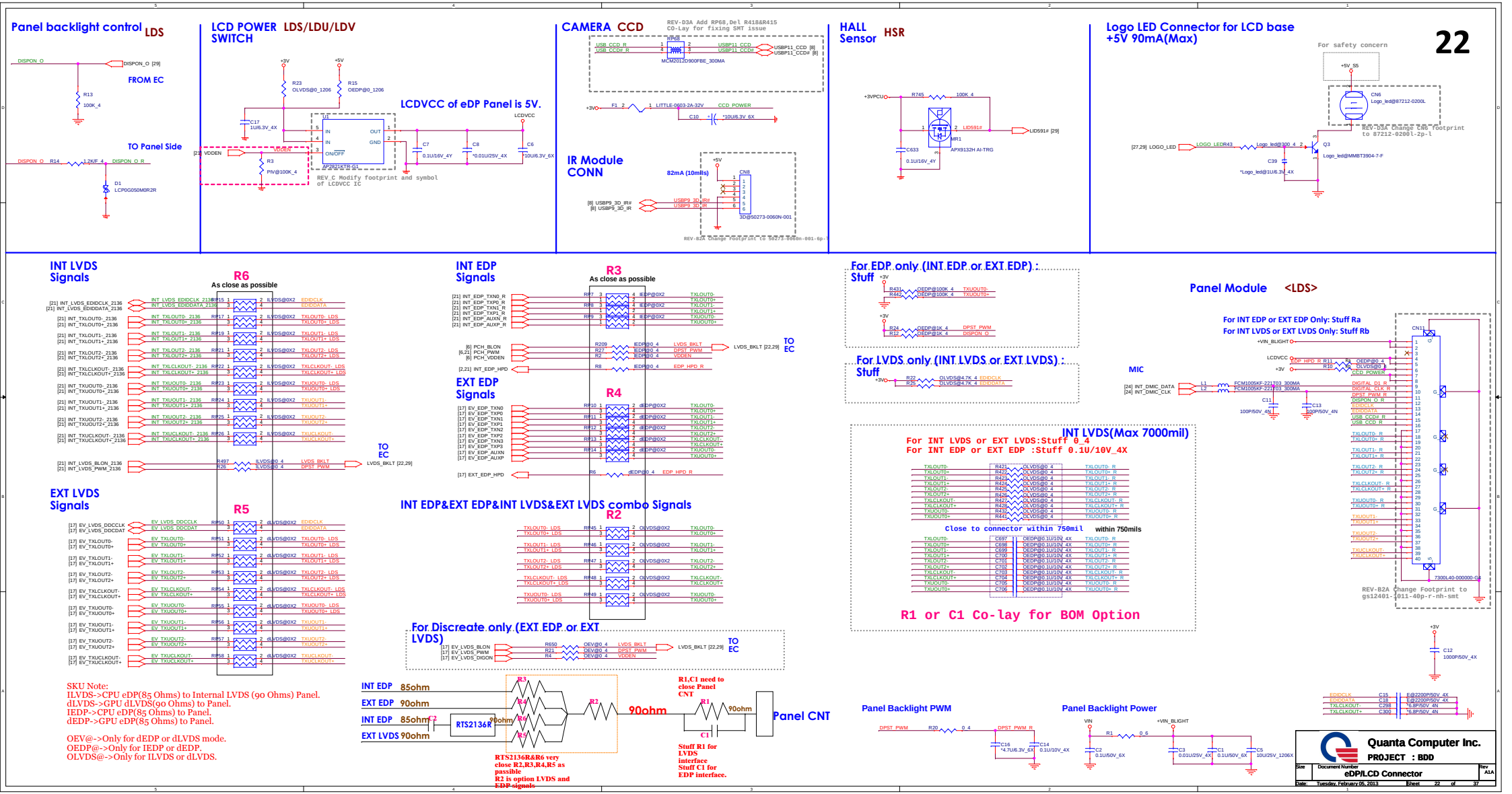
Dual Mode Regulator Configuration

	4.7-uH(L2602)	0 Olm(R2632)
SWR	Connect	NC
LDO	NC	Connect

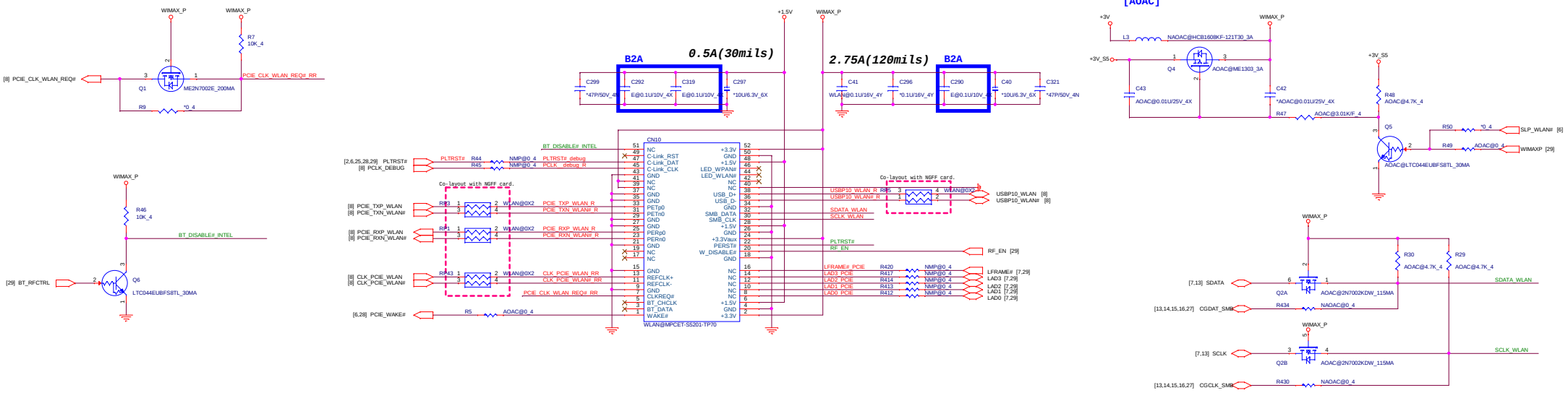


1. C2602 22-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN17

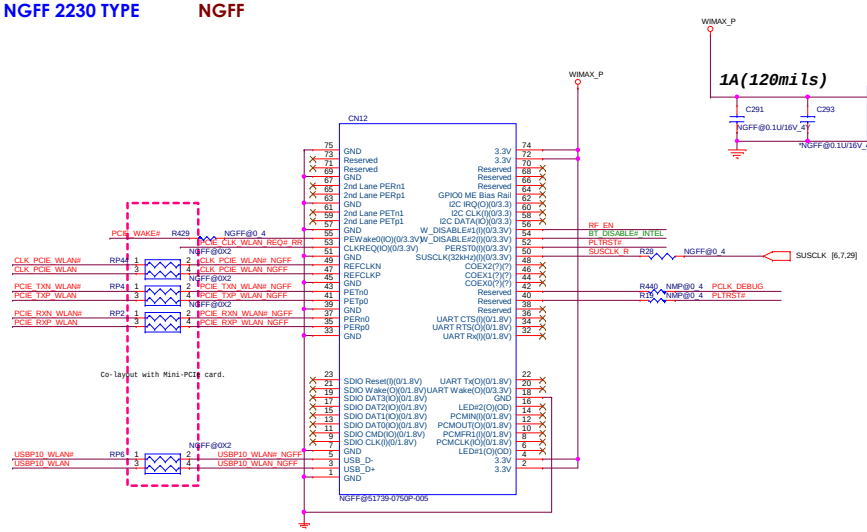
Quanta Computer Inc.
PROJECT : BDD
Size | Document Number: eDP to LVDS (PS8625) | Rev A1A
Date: Tuesday, February 05, 2013 | Sheet 21 of 37



MINI Card Slot#1(WiFi / Wimax MNW/DEG / Combo)



NGFF 2230 TYPE NGFF

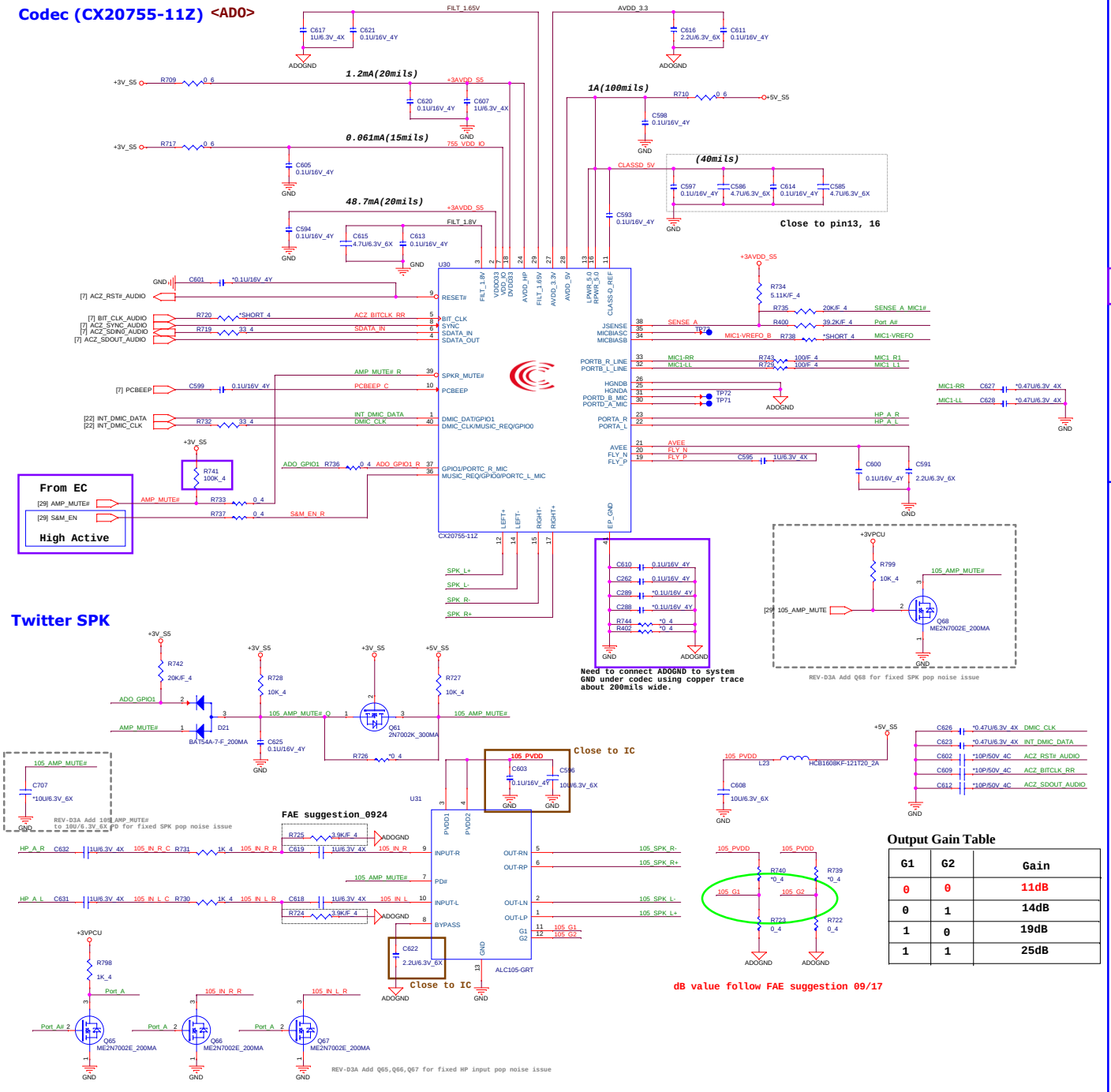


NFC Connector

REV-C2A Del NFC circuit

Quanta Computer Inc.		
PROJECT : BDD		
Size	Document Number: MINI-PCIE(WLAN/NGFF)	Rev: A1A
Date: Tuesday, February 05, 2013	Sheet 23 of 37	

Codec (CX20755-11Z) <ADO>

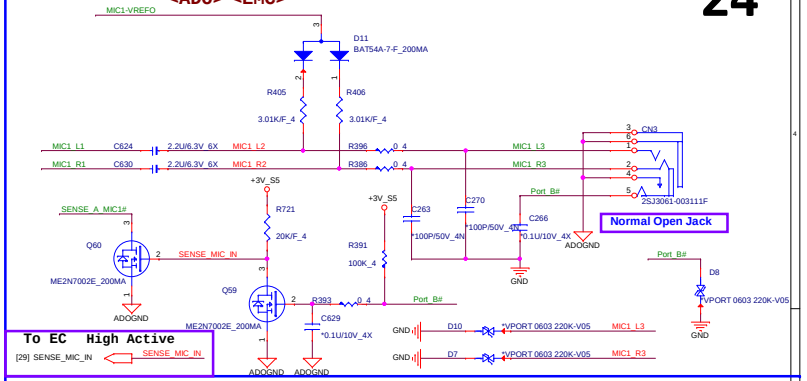


Twitter SPK

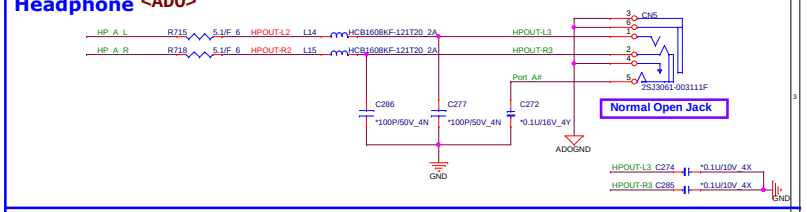
Output Gain Table

G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

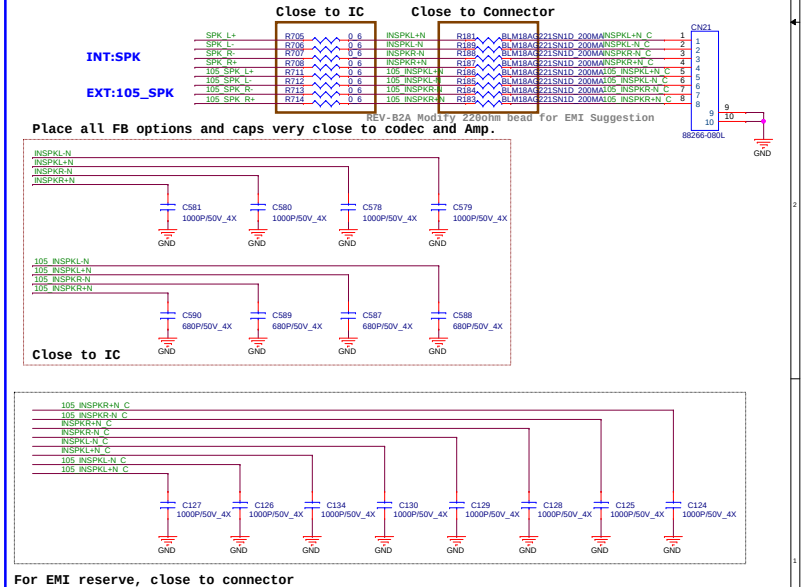
External MIC <ADO> <EMC>



Headphone <ADO>



4 Speakers <ADO>

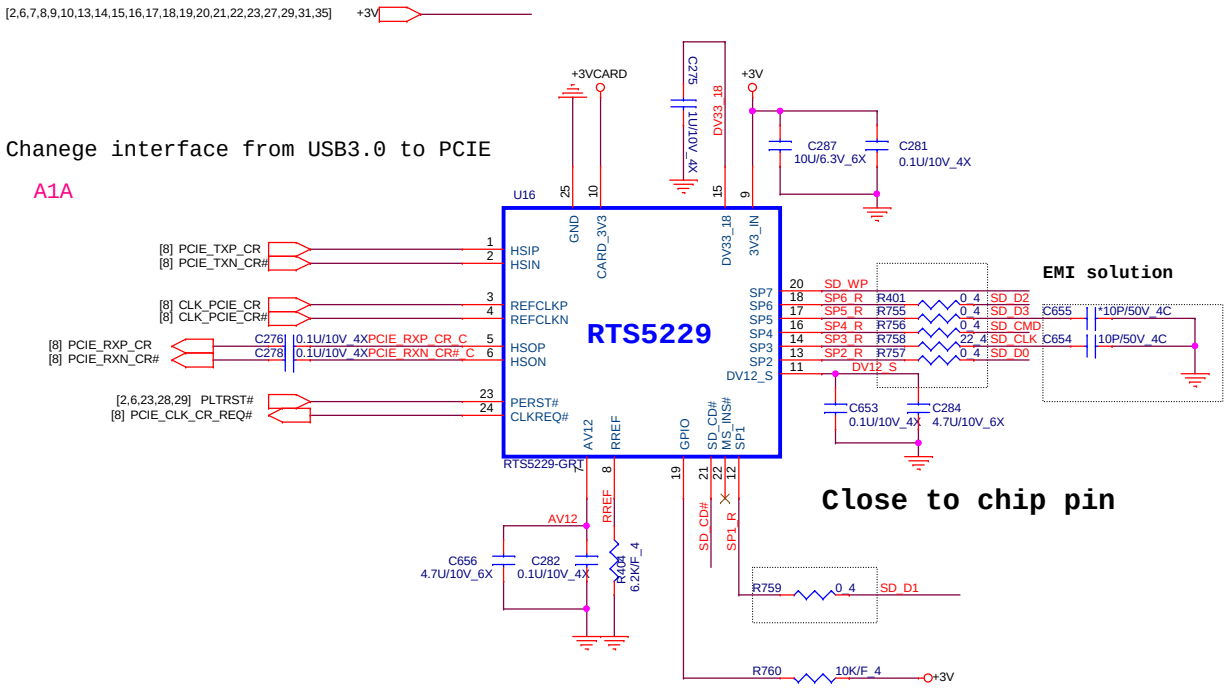


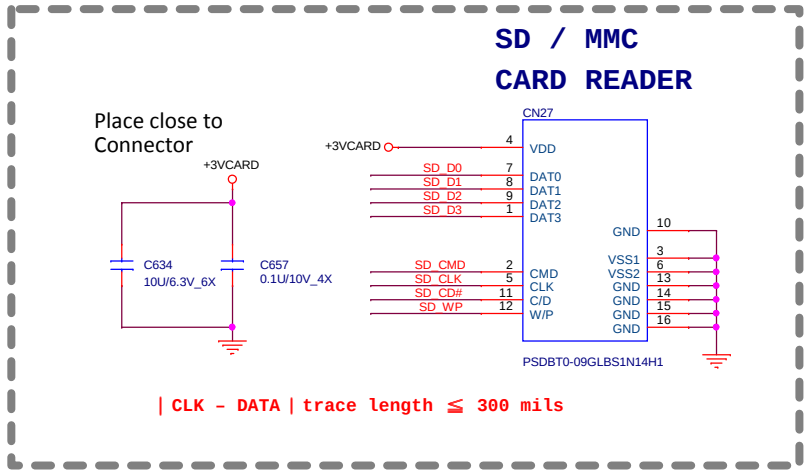
Quanta Computer Inc.	PROJECT : BDD
Size	Document Number: Codec(CX20755 S&M+4SPKS) — Rev: A1A
Date: Tuesday, February 05, 2013	Sheet 24 of 37

2 IN 1 CARD READER (Type: MS/SD) <MMC>

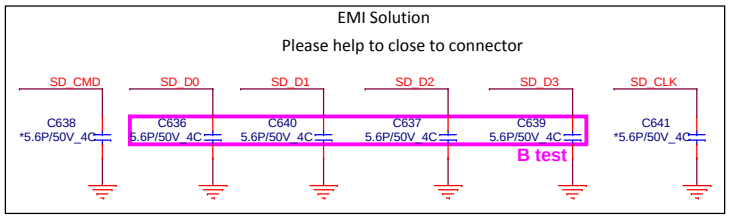
Card Reader (RTS5227-GRT PCI-E)

SP1 => SD_D1
SP2 => MS_D1 /SD_D0
SP3 => MS_D0 /SD_CLK
SP4 => MS_D2 /SD_CMD
SP5 => MS_D3 /SD_D3
SP6 => MS_CLK/SD_D2
SP7 => MS_BS /SD_WP





Share Pin



Quanta Computer Inc.
PROJECT : BDD

Size	Document Number	Rev
	Card Reader (RTS5229) & CR SOCKET	A1A
Date: Tuesday, February 05, 2013	Sheet 25 of 37	

USB w S&C MAXIM solution <SLC>

14566/14600/14617

	R1	R2	R3	R4	R5	R6	R7	
14566	V	V				V		
14600		V		V				
14617(no CB2)		V		V			V	
14641/14642/14644		V		V				
14640/14651			V		V			

REV-C2A Add pull-up to +3V_S5 for fixing leakage

SW2	SW3	14600	
CB0	CB1	Status	
0	0	Auto mode	Charger , AM
0	1	Force dedicated charger mode	Charger , FM
1	0	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14641	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force 1A for Apple device	Charger , AP1
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14644	
CB0	CB1	Status	
0	0	2A Auto mode for Apple device	Charger , AM2
1	**0**	Force dedicated charger mode	Charger , FM
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

SW2	SW3	14642	
CB0	CB1	Status	
X	0	2A Auto mode for Apple device	Charger , AM2
0	**1**	Pass-Through(USB) mode	USB , PM
1	1	pass-through(USB) with CDP Emulation	USB , CM

<SLC>

<EMI> <U3B> <USB>

USB 3.0 CONN

USB 3.0 Power switch <U2B><USB><U3B>

Change power CAP to 220U. 20121017

150 mils (Iout=3.5A)

80 mils (Iout=2A)

REV-D3A Del co-lay EMI common chock for fixing SMT solder open risk.

USB3.0: DFHS09FR355

M/B side(up port)

M/B side(Down port)

Support Sleep & Charge

REV-B2A Del LAN PCIE signals and Add LAN signals to Daughter board

USB2.0 & Lan (Daughter/B)

Small board(up port)

Small board(Down port)

Small board(up port)

Small board(Down port)

REV-D3A Add for wake on USB

ESD Protect

Quanta Computer Inc.

PROJECT : BDD

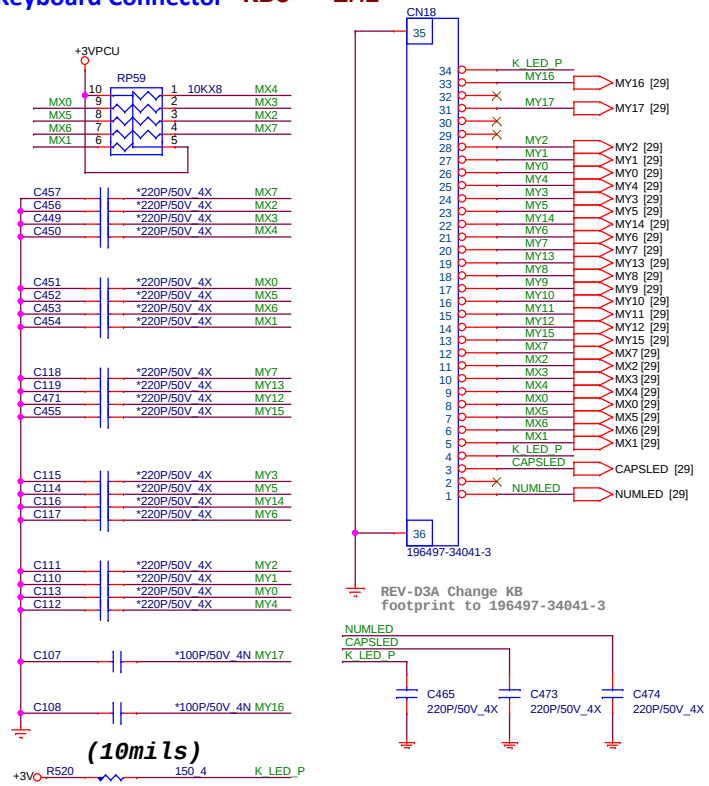
USB 3.0/IO Board

Size: Document Number: Rev: A1A

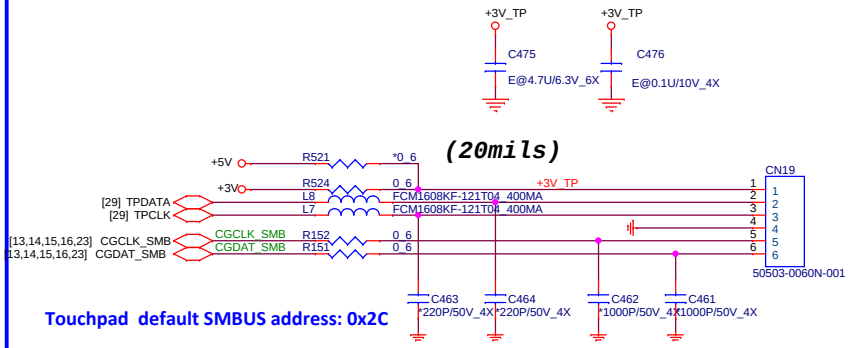
Date: Tuesday, February 05, 2013 Sheet 26 of 37

27

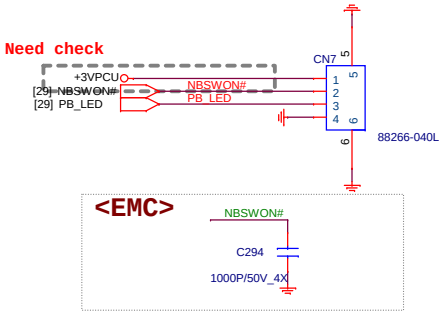
Keyboard Connector <KBC> <EMI>



Touch Pad Connector <TPD> <EMI>



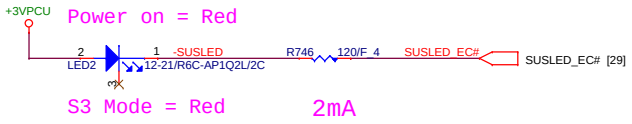
Power Botton Connector <PSW>



LED <LED>

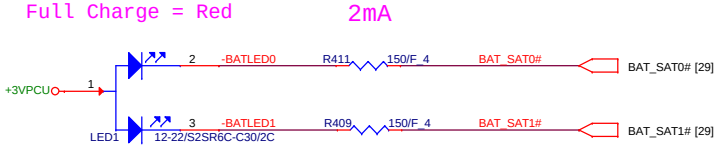
LED-Power

POWER

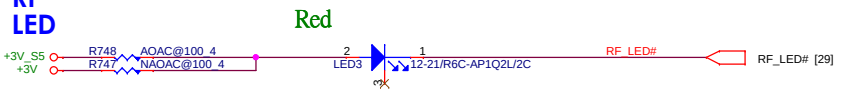


BATERRY

BATT LED (DC-IN)

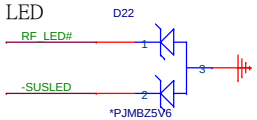


RF LED

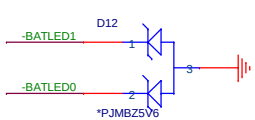


ESD Protect <EMC>

FOR POWER LED and W-LAN LED



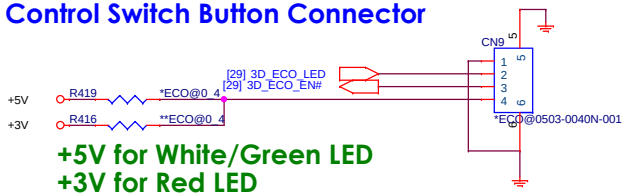
FOR BATTERY LED



	DC IN/BAT charge	Power	Wireless
10F/10FG/10S/10SG	White/Amber(+5VPCU)	White/Amber(+5VPCU)	Amber
10FH/10SH	Red/Amber(+3VPCU)	Red/Amber(+3VPCU)	Red

	DC IN/BAT charge		Power		Wireless
Control I/O net name	BAT_SAT0#	BAT_SAT1#	PWRLED#	SUSLED_EC#	RF_LED#
Active Status	Low	Low	Low	Low	Low

Control Switch Button Connector



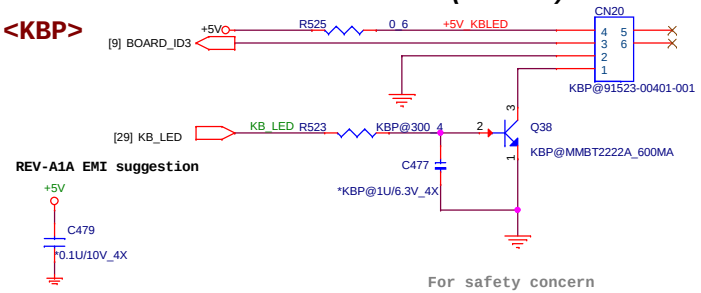
+5V for White/Green LED
+3V for Red LED

K/B LED power

REV-C2A Modify CN20 footprint

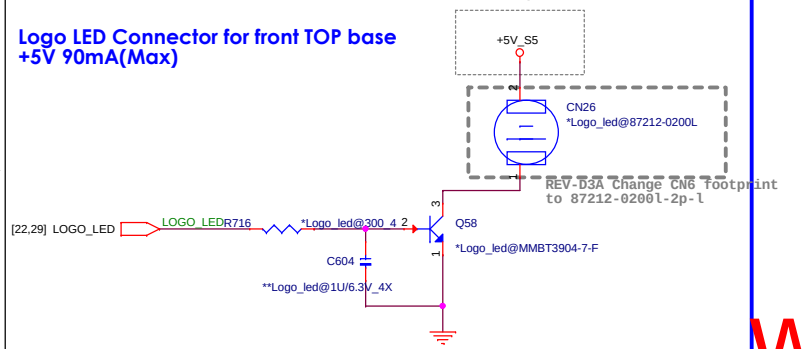
0.35A(20mils)

<KBP>



For safety concern

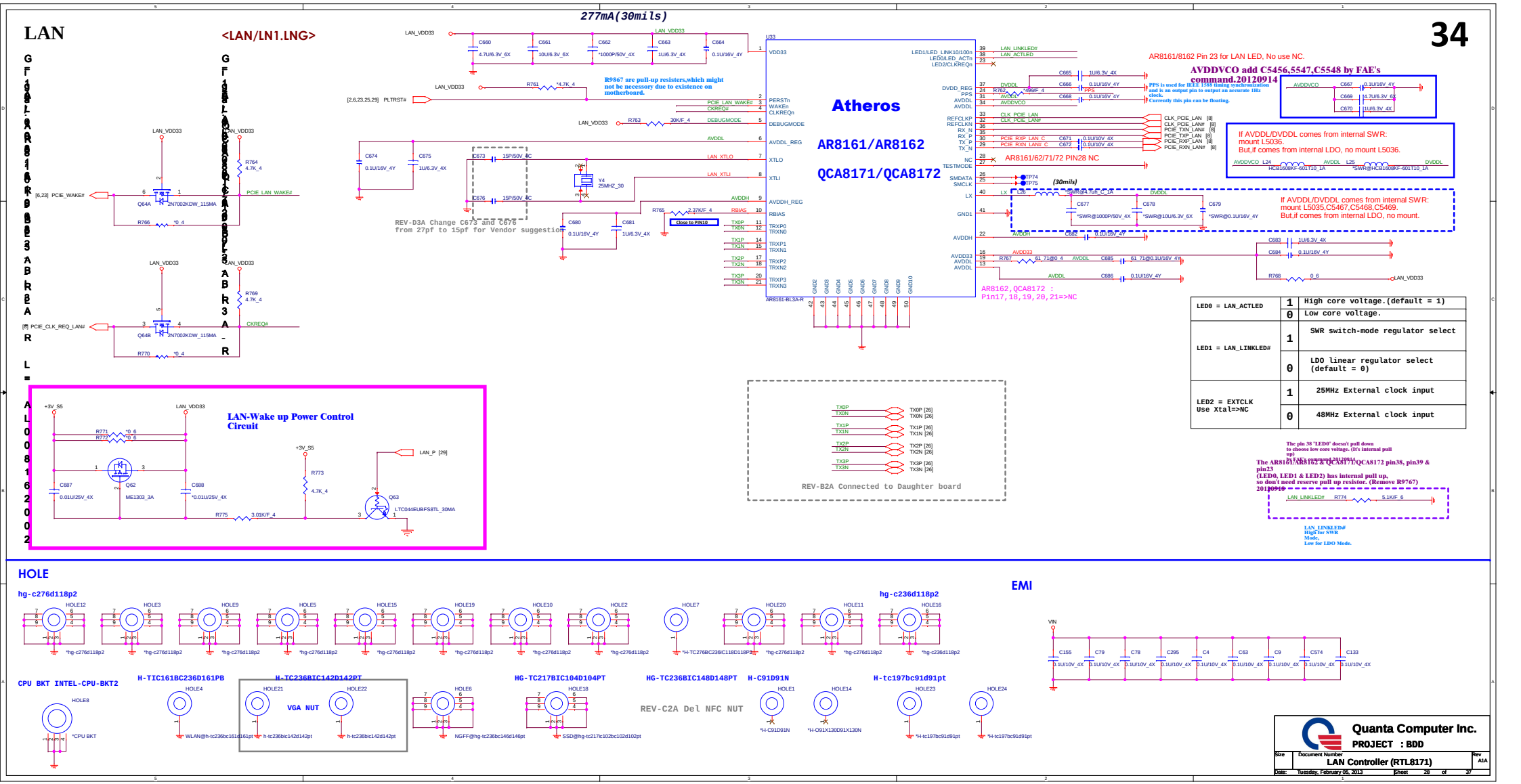
Logo LED Connector for front TOP base
+5V 90mA(Max)

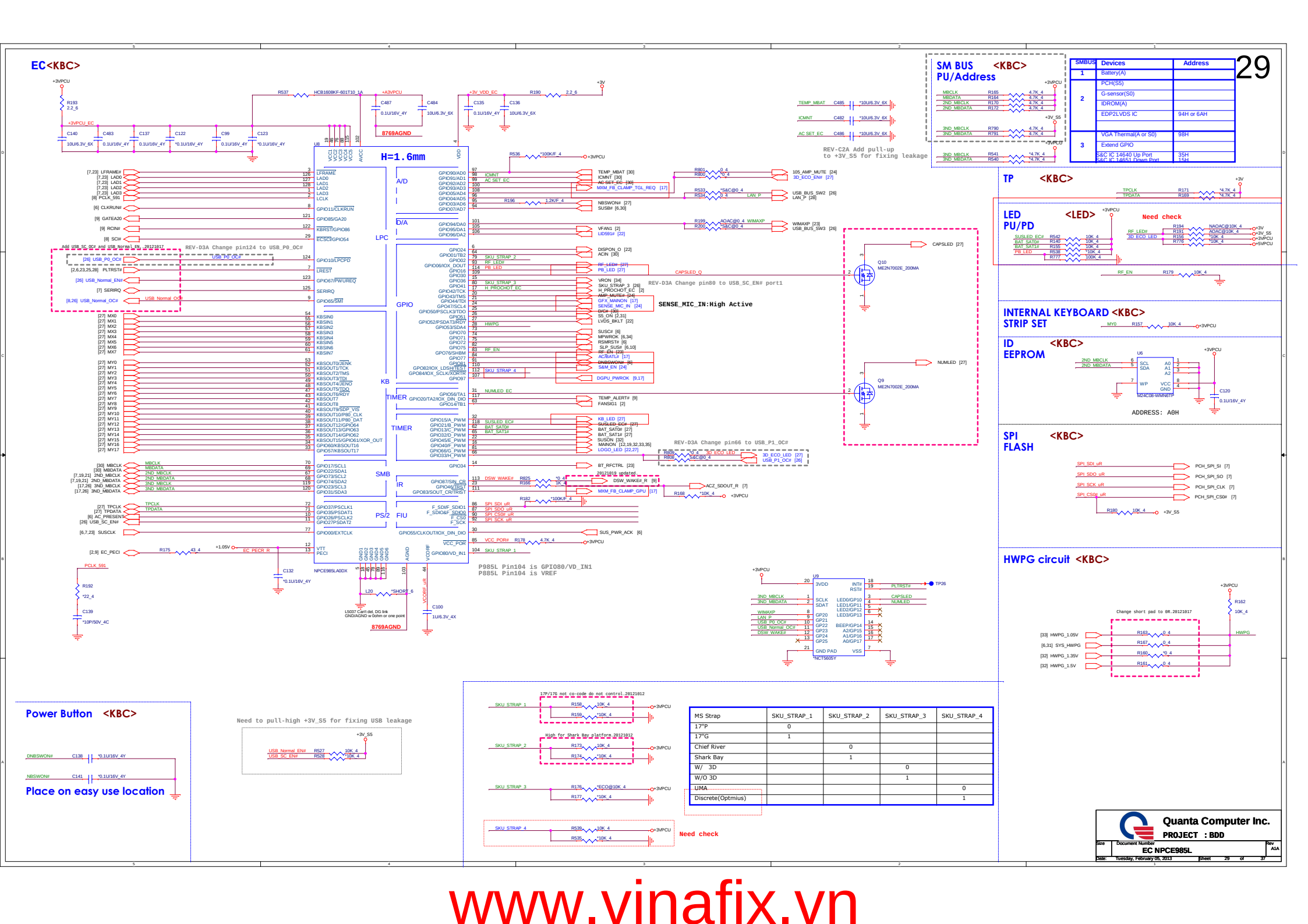


Quanta Computer Inc.
PROJECT : BDD

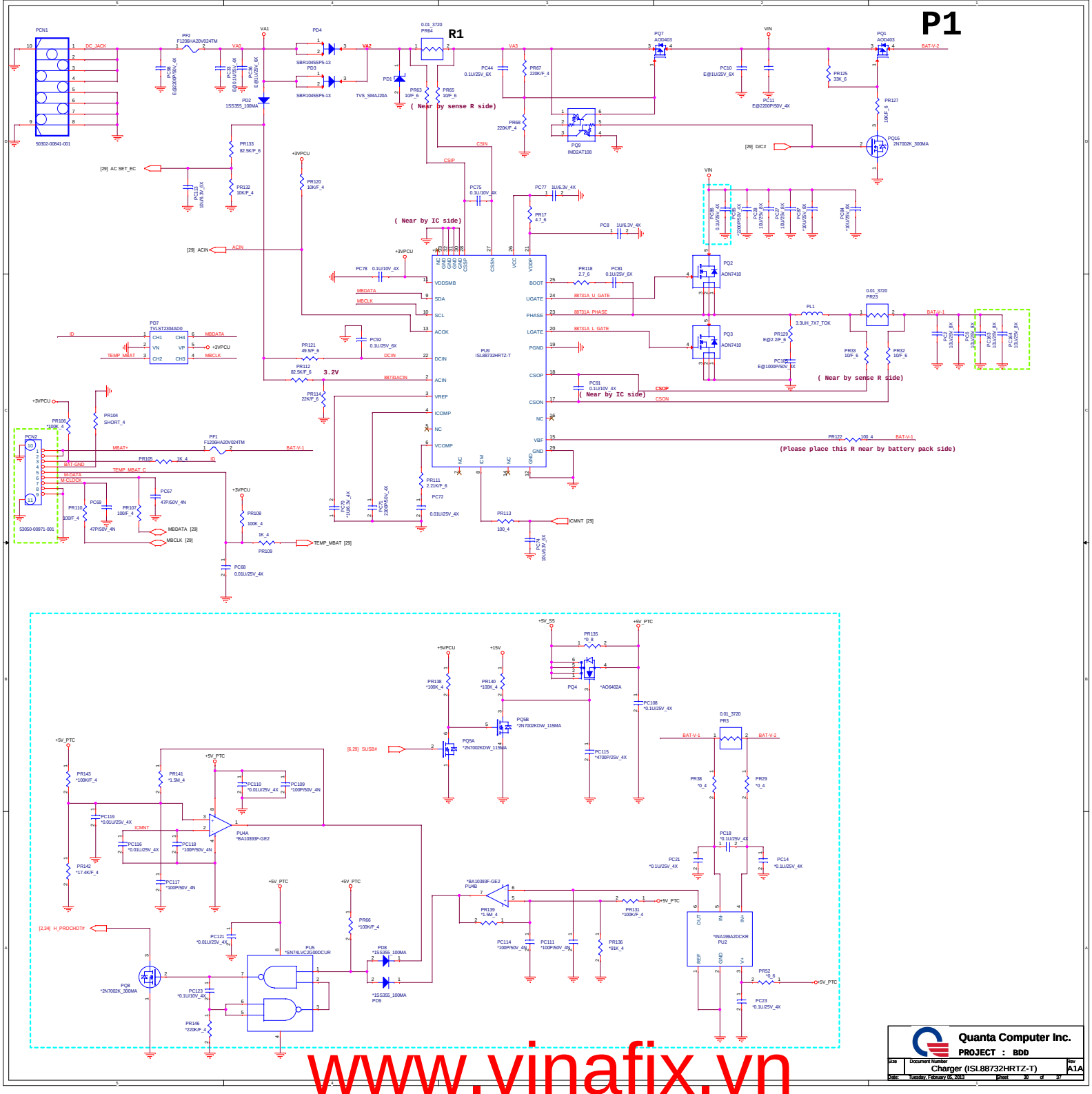
Size	Document Number	Rev
	HDD/ODD/FAN/KEY CONN	A1A

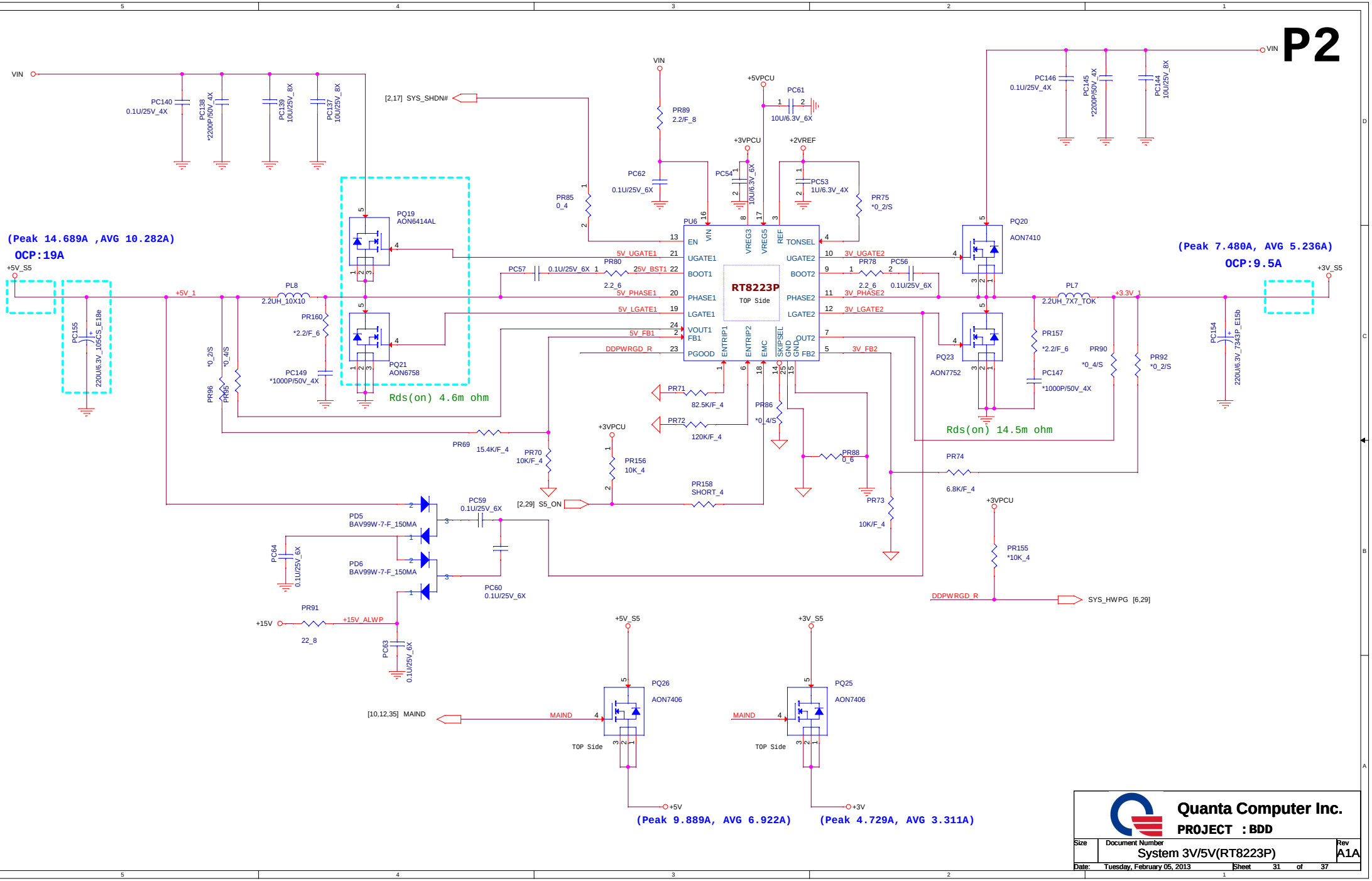
Date: Tuesday, February 05, 2013 Sheet 27 of 37

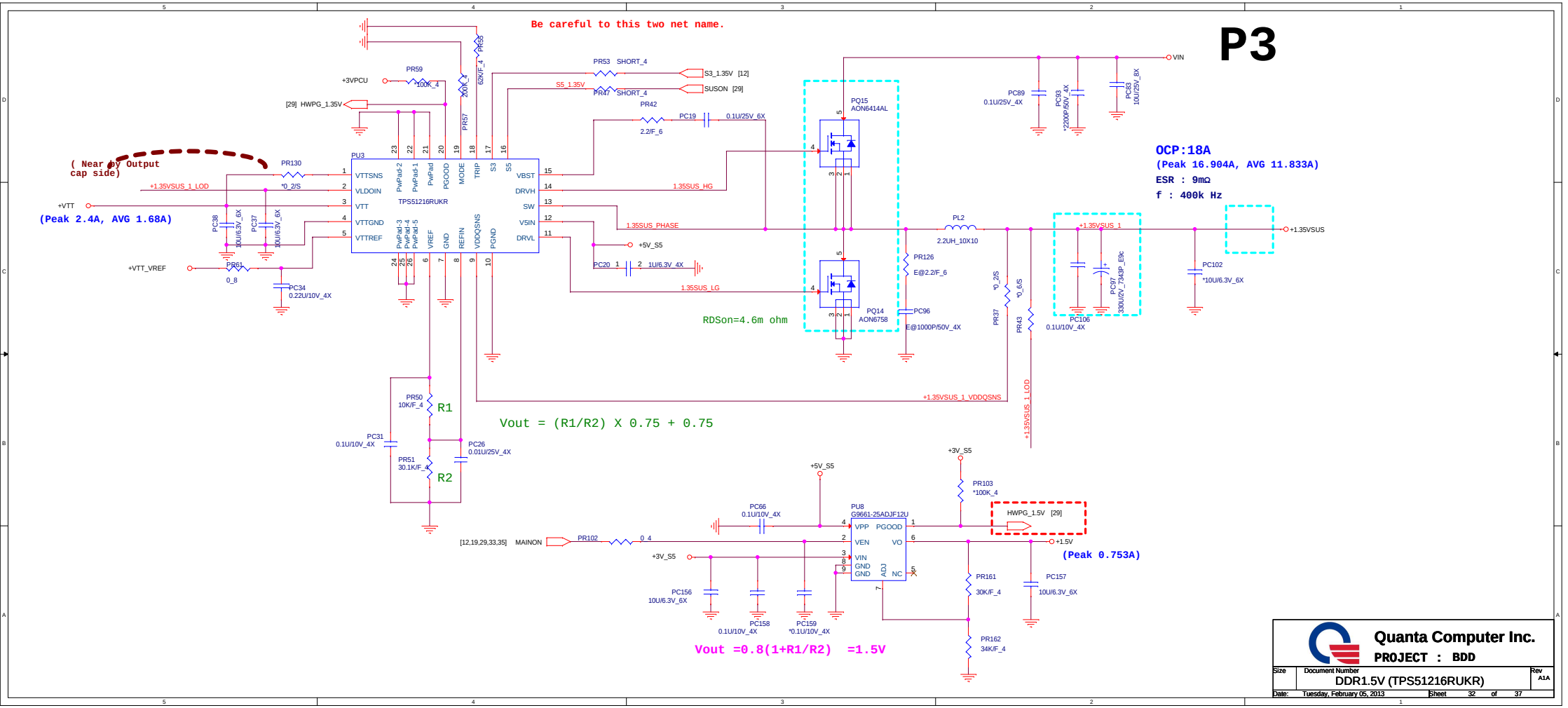


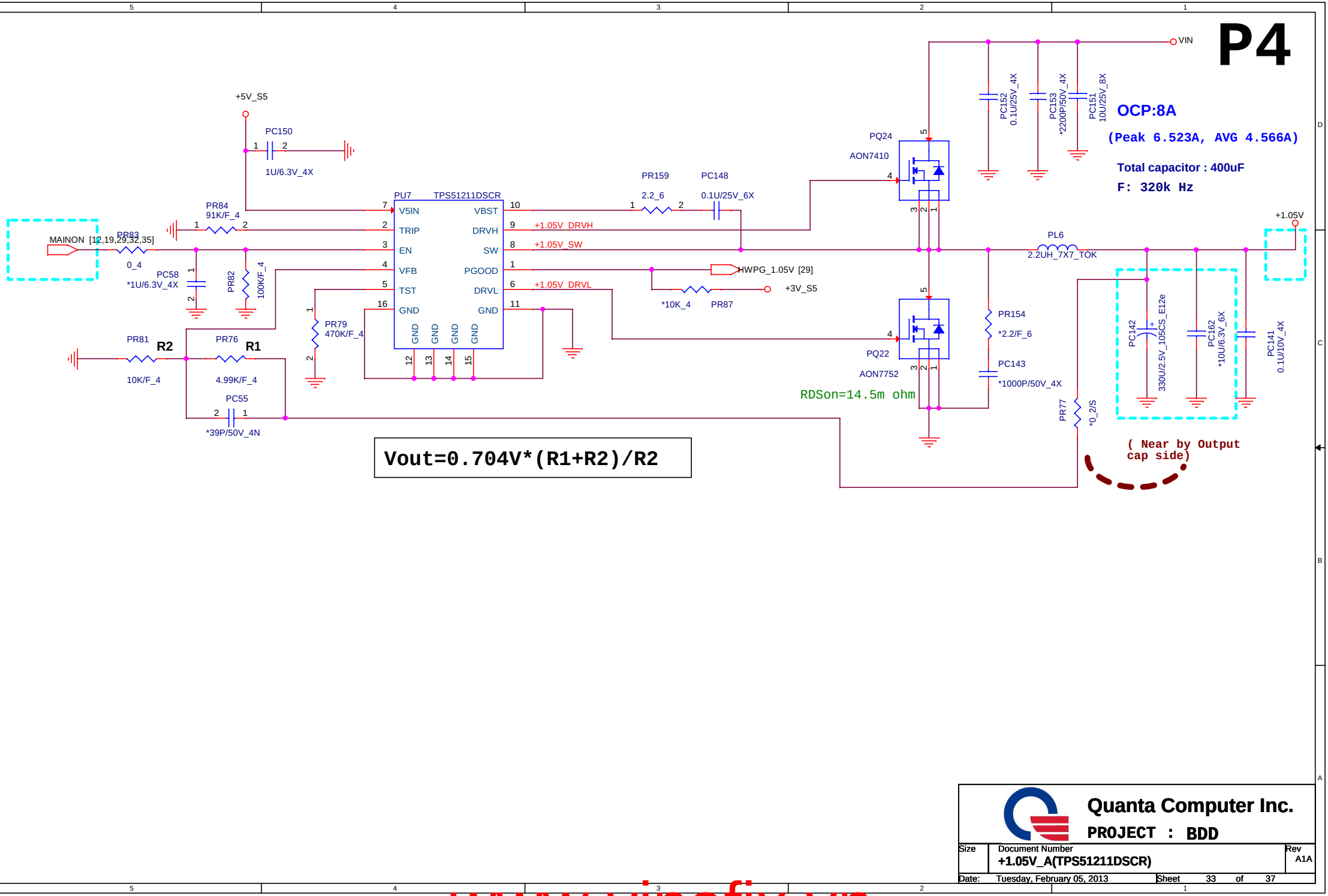


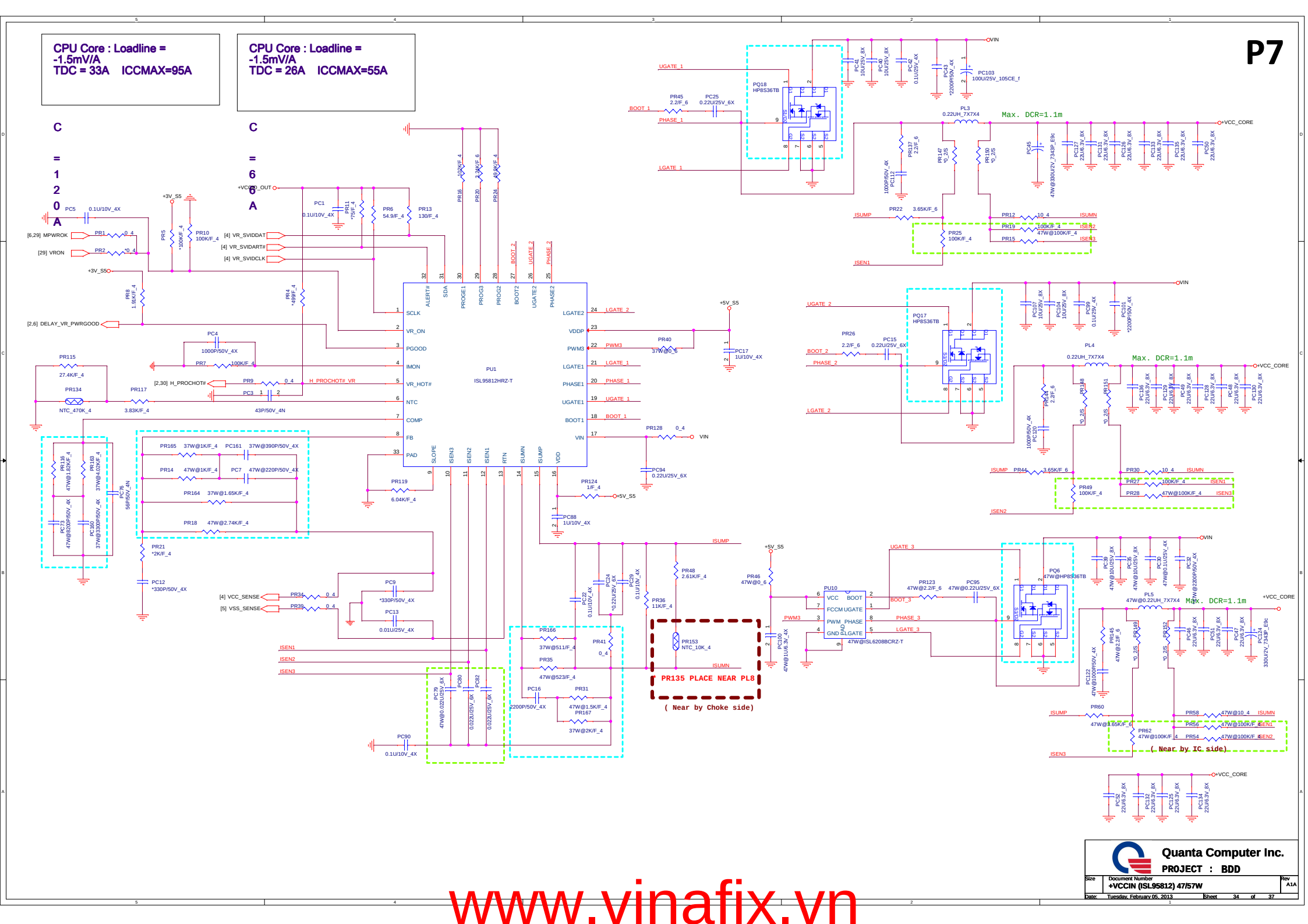
MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17"P	0			
17"G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optmius)				1

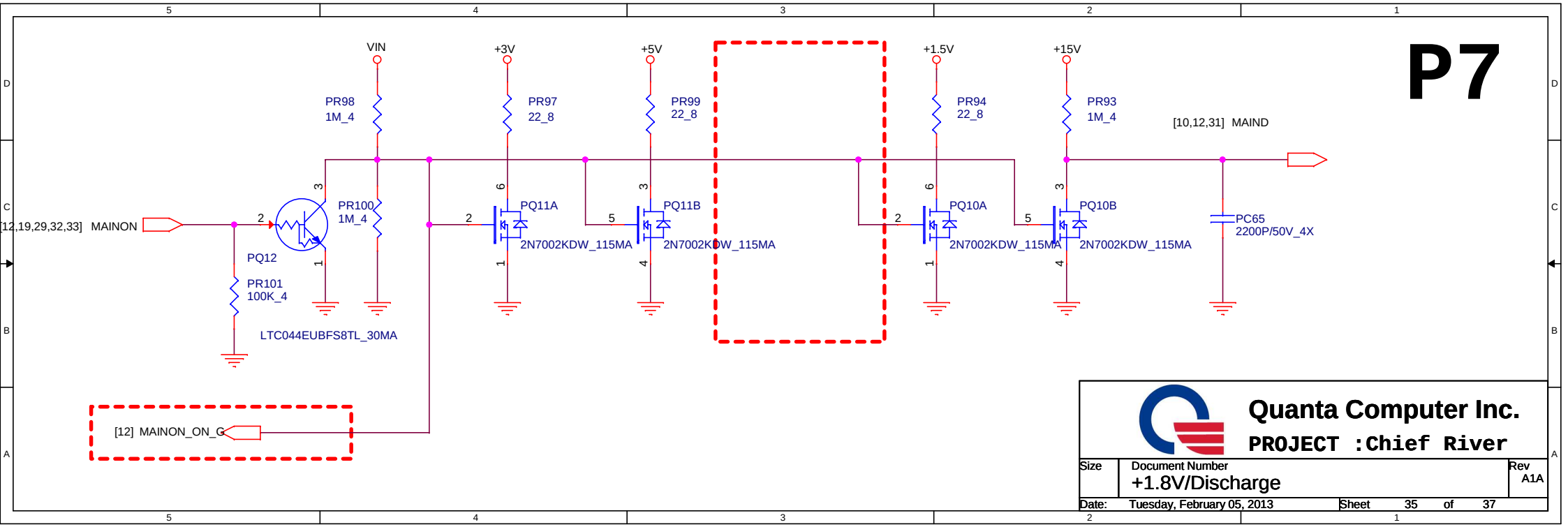


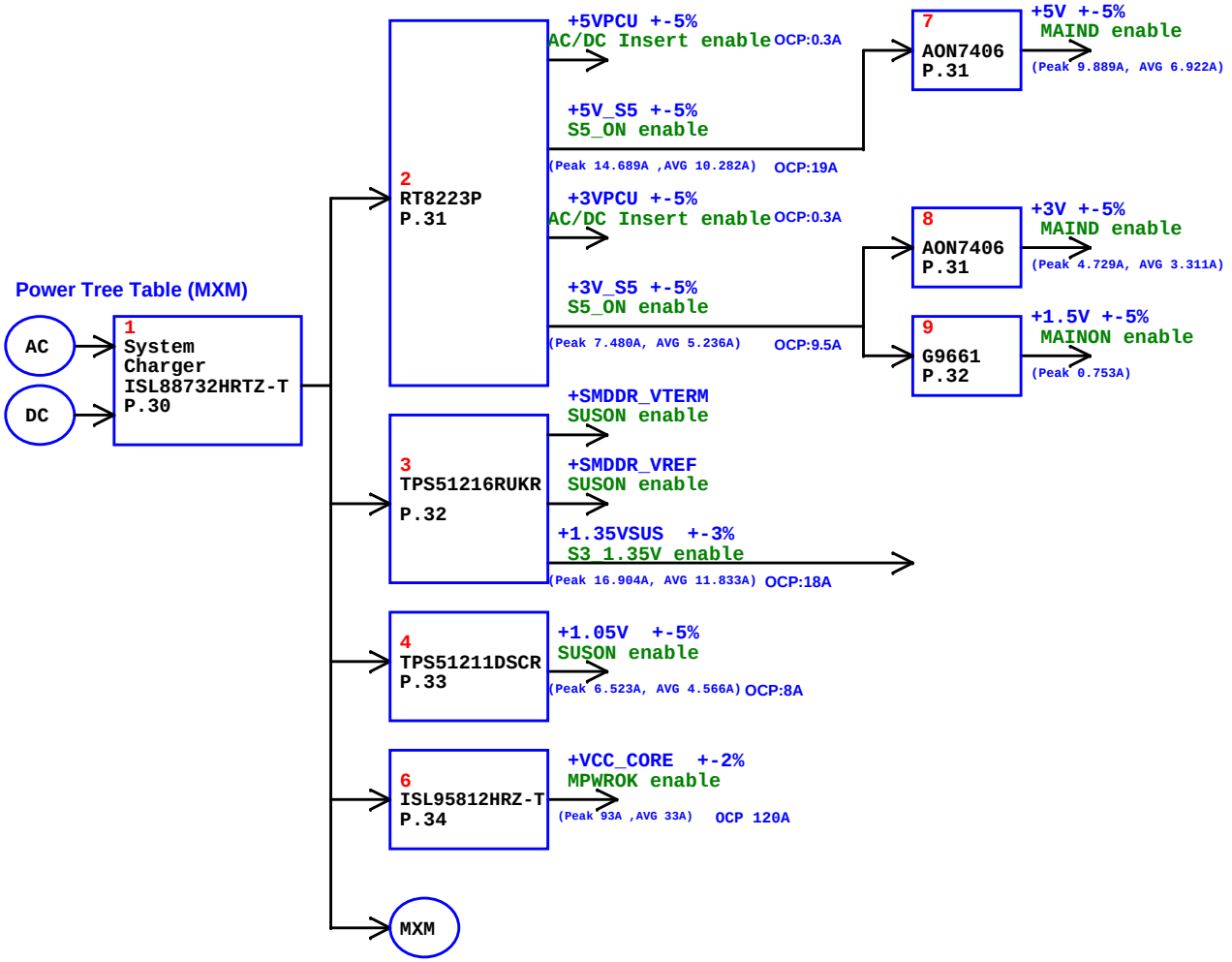












Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BDD
Size | Document Number: POWER TREE TABLE | Rev: 1A
Date: Tuesday, February 05, 2013 | Sheet 36 of 37

Model	REV
BDD MB	1A

CHANGE LIST

MODEL	TE5	
PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
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25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 204					
PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01
PART NUMBER:		DRAWING BY:	Andy Wang	REVISON:	1A

Quanta Computer Inc.
PROJECT : BDD
Size | Document Number: Power change list | Rev: 1A
Date: Tuesday, February 05, 2013 | Sheet 37 of 37