Dell/Compal LA-L613P

HDS70 Schematic Document

Horizon MLK 17

(Alder Lake P with nVIDIA GN20-E)

EngR

2021-11-25

Rev: 1.0 (A00)

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.		
Title: Cover Page		
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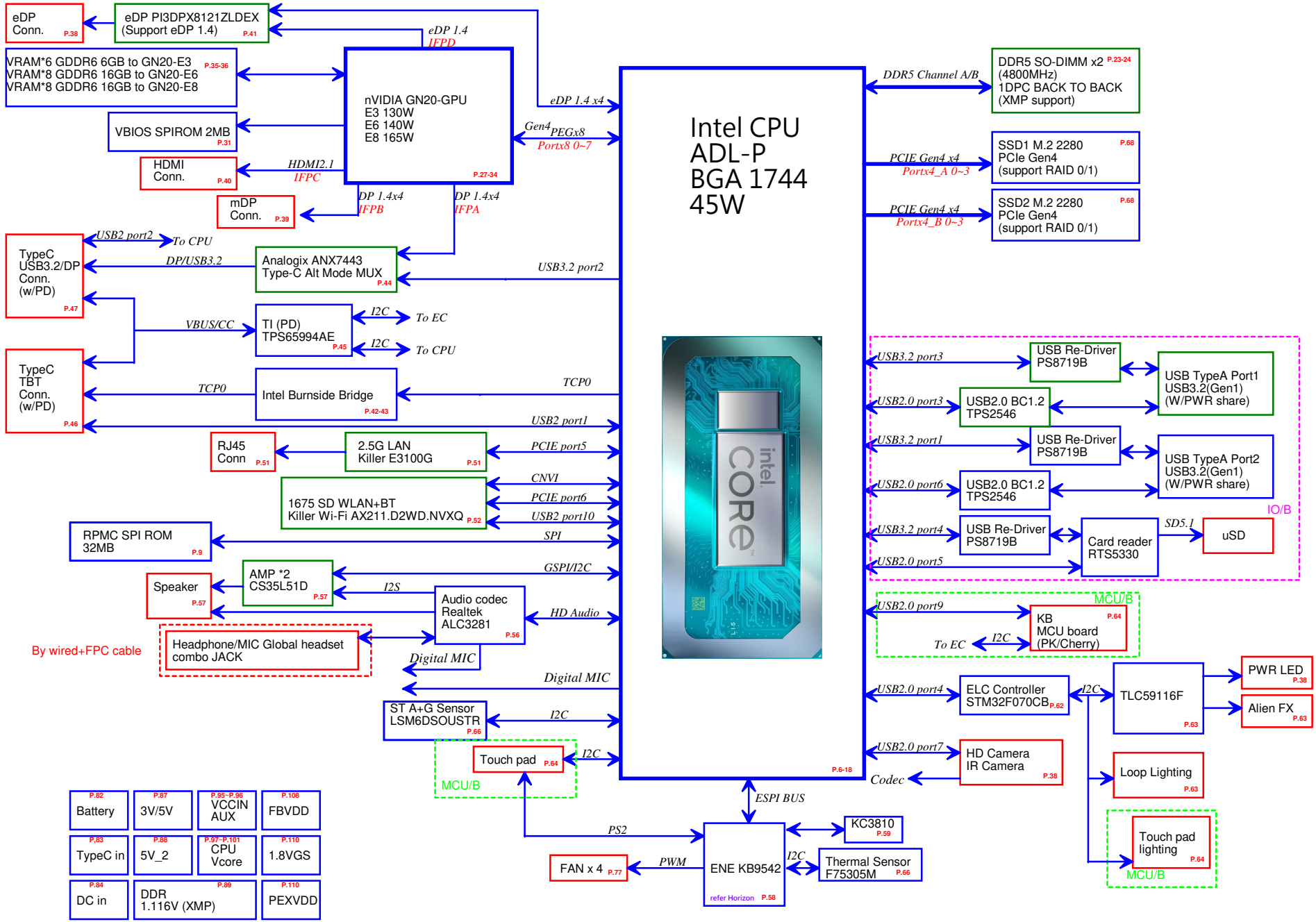

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Block Diagram			
Size	Document Number: LA-L613P		Rev: 0.3
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Board ID Table for AD channel

Vcc	3.1V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.000V	0x00 – 0x17
1	12K +/- 1%	0.323V	0.332V	0.342V	0x18 – 0x1E
2	15K +/- 1%	0.393V	0.404V	0.416V	0x1F – 0x25
3	20K +/- 1%	0.503V	0.517V	0.531V	0x26 – 0x30
4	27K +/- 1%	0.642V	0.659V	0.676V	0x31 – 0x3A
5	33K +/- 1%	0.750V	0.769V	0.789V	0x3B – 0x45
6	43K +/- 1%	0.910V	0.932V	0.955V	0x46 – 0x53
7	56K +/- 1%	1.088V	1.112V	1.138V	0x54 – 0x64
8	75K +/- 1%	1.300V	1.329V	1.357V	0x65 – 0x76
9	100K +/- 1%	1.519V	1.550V	1.581V	0x77 – 0x88
10	130K +/- 1%	1.720V	1.752V	1.785V	0x89 – 0x96
11	160K +/- 1%	1.874V	1.908V	1.941V	0x97 – 0xA3
12	200K +/- 1%	2.032V	2.067V	2.101V	0xA4 – 0xAF
13	240K +/- 1%	2.153V	2.188V	2.223V	0xB0 – 0xB7
14	270K +/- 1%	2.227V	2.262V	2.297V	0xB8 – 0xBF
15	330K +/- 1%	2.344V	2.37V	2.413V	0xC0 – 0xC9
16	430K +/- 1%	2.480V	2.515V	2.550V	0xCA – 0xD4
17	560K +/- 1%	2.596V	2.630V	2.665V	0xD5 – 0xDD
18	750K +/- 1%	2.701V	2.735V	2.769V	0xDE – 0xE6
19	1.2M +/- 1%	2.829V	2.862V	2.895V	0xE7 – 0xFF

PCIE CLK table

PCIE CLK	PCB Revision
0	GPU
1	
2	
3	SSD1
4	SSD2
5	LAN
6	WLAN
7	

Board ID table

NV GN20	PCB Revision (HDS70)
2	EVT-1
6	DVT-1
10	DVT-2
14	Pilot

Voltage Rails

Power Plane	Description	S0	S0ix	S4 / S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+12.6VB_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Processor Core power rail	ON	OFF	OFF
+VCC_GT	Processor graphics power rail	ON	OFF	OFF
+VCCIN_AUX	Processor AUX power rail	ON	ON/OFF	OFF
+1.116V_MEM	System memory power	ON	ON	OFF
+5V_BULK_DRAM	DDR5 bulk power rail	ON	ON	OFF
+1.8V_PROC	1.8V Input Power rail to Processor	ON	ON/OFF	OFF
+1.8V_PRIM	PCH Primary (I/O)	ON	ON	OFF
+3V_PRIM	PCH Primary (I/O)	ON	ON	OFF
+1.05VO_VNNBYPASS	PCH Bypass Rails	ON	ON	OFF
+1.05VO_EXTBYPASS	PCH Bypass Rails	ON	ON	OFF
+1.05V_PROC	1.05V Input rail to Processor	ON	ON	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	OFF
+3V_WLAN	+3VALW power for WLAN power rails	ON	ON	OFF
+3VS	System +3VS power rail	ON	ON	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	ON	OFF
+3VGS	+3VS power rail for GPU	ON	ON	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF
+3VL_RTC	RTC power	ON	ON	ON
+3VALW_LAN	+3VALW power for LAN power rails	ON	ON	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

HSIO	USB3.2	PCIe	SATA3	Function
1	1	1		Type-A(IO/B)
2	2	2		Type-C(M/B)
3	3	3		Type-A(IO/B)
4	4	4		Card reader(IO/B)
5		5		LAN
6		6		WLAN
7		7		N/A
8		8		N/A
9		9		N/A
10		10		N/A
11		11	0	N/A
12		12	1	N/A

USB2	Function
1	TBT Type-C
2	Type-C
3	Type-A(IO/B)
4	ELC
5	Card reader(IO/B)
6	Type-A(IO/B)
7	Camera
8	N/A
9	Per Key(MCU/B)
10	WLAN+BT

PCIex4	PEG	Function
A_0	60	SSD - JSSD1
A_1		
A_2		
A_3		
B_0	62	SSD - JSSD2
B_1		
B_2		
B_3		

PCIex8	PEG	Function
0	10	GPU
1		
2		
3		
4		
5		
6		
7		

Symbol Note :

Digital Ground

Analog Ground

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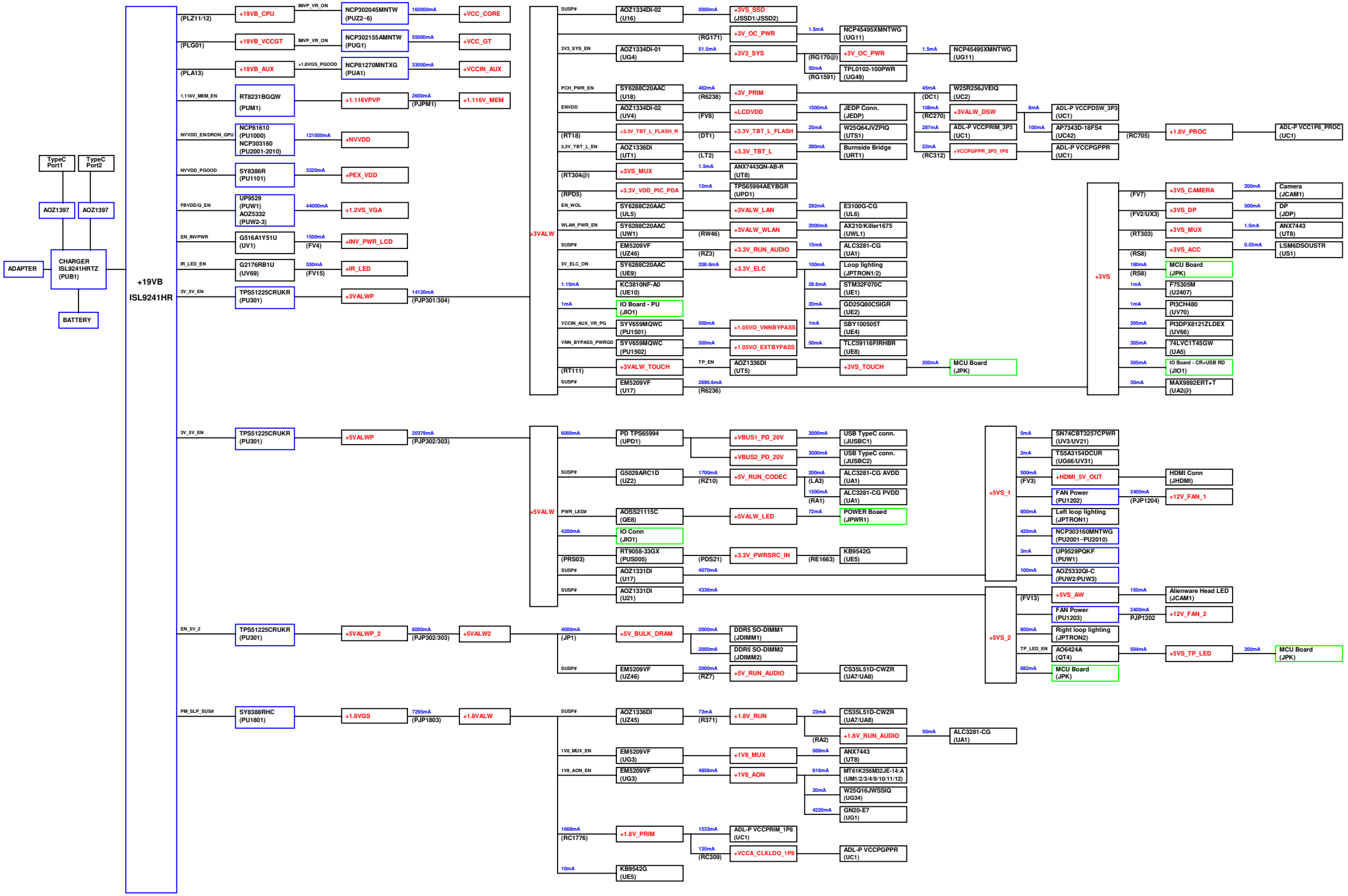
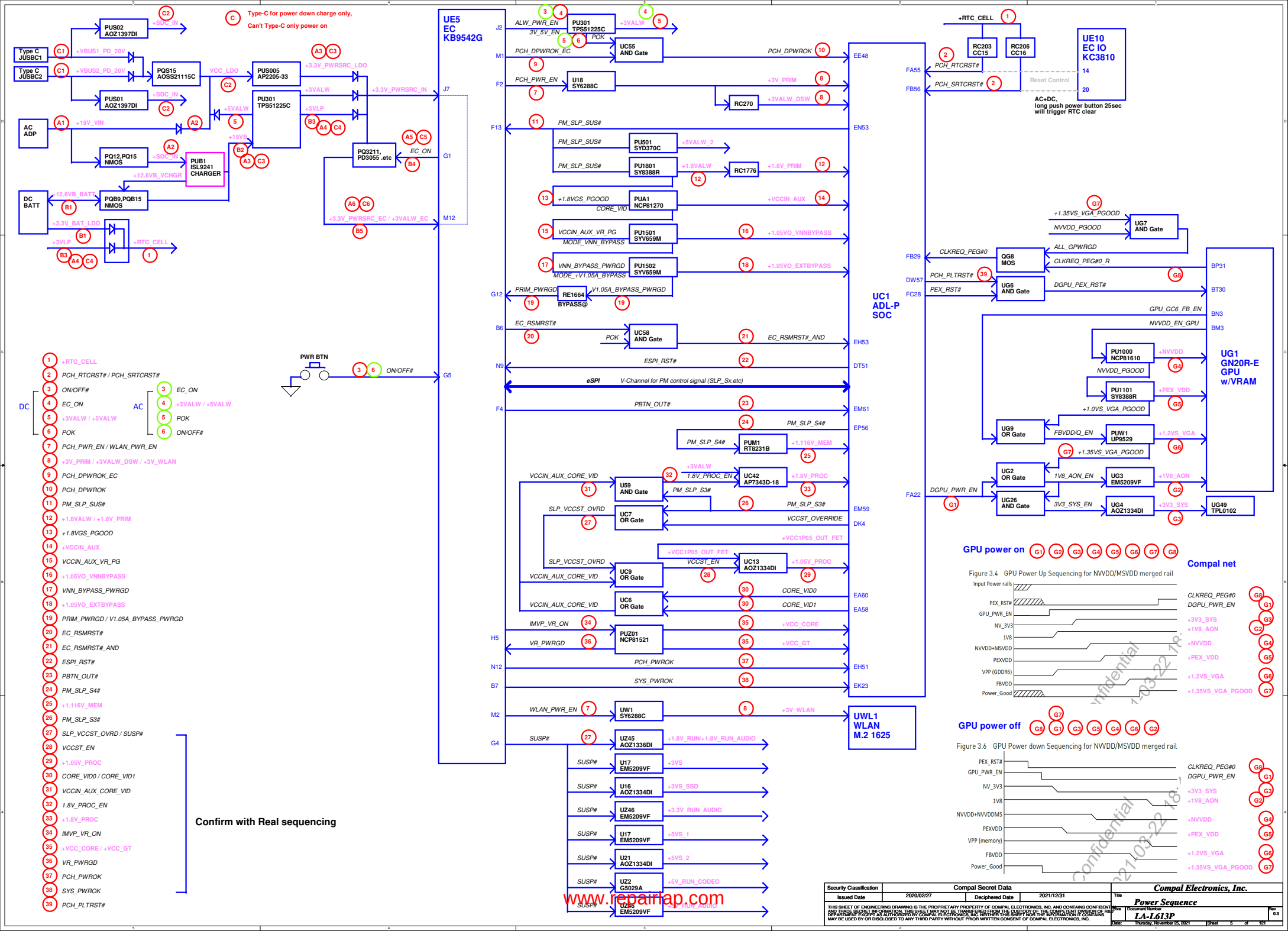
Title: Notes List			
Size:	Document Number: LA-L613P		Rev: 0.3
Date: Thursday, November 25, 2021	Sheet 3 of 121		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Title	Power Map		
Size	Document Number		Rev
	LA-L613P		0.3
Date: Tuesday, November 29, 2022	Sheet 4 of 58		



1 +RTC_CELL
2 PCH_RTCRST# / PCH_SRTCRST#
3 ON/OFF#
4 EC_ON
5 +3VALW / +5VALW
6 POK
7 PCH_PWR_EN / WLAN_PWR_EN
8 +3V_PRIM / +3VALW_DSW / +3V_WLAN
9 PCH_DPWROK_EC
10 PCH_DPWROK
11 PM_SLP_SUS#
12 +1.8VALW / +1.8V_PRIM
13 +1.8VGS_PGOOD
14 +VCCIN_AUX
15 VCCIN_AUX_VR_PG
16 +1.05VO_VNNBYPASS
17 VNN_BYPASS_PWRGD
18 +1.05VO_EXTBYPASS
19 PRIM_PWRGD / V1.05A_BYPASS_PWRGD
20 EC_RSMRST#
21 EC_RSMRST#_AND
22 ESPI_RST#
23 PBTN_OUT#
24 PM_SLP_S4#
25 +1.116V_MEM
26 PM_SLP_S3#
27 SLP_VCCST_OVRD / SUSP#
28 VCCST_EN
29 +1.05V_PROC
30 CORE_VID0 / CORE_VID1
31 VCCIN_AUX_CORE_VID
32 1.8V_PROC_EN
33 +1.8V_PROC
34 IMVP_VR_ON
35 +VCC_CORE / +VCC_GT
36 VR_PWRGD
37 PCH_PWROK
38 SYS_PWROK
39 PCH_PLTRST#

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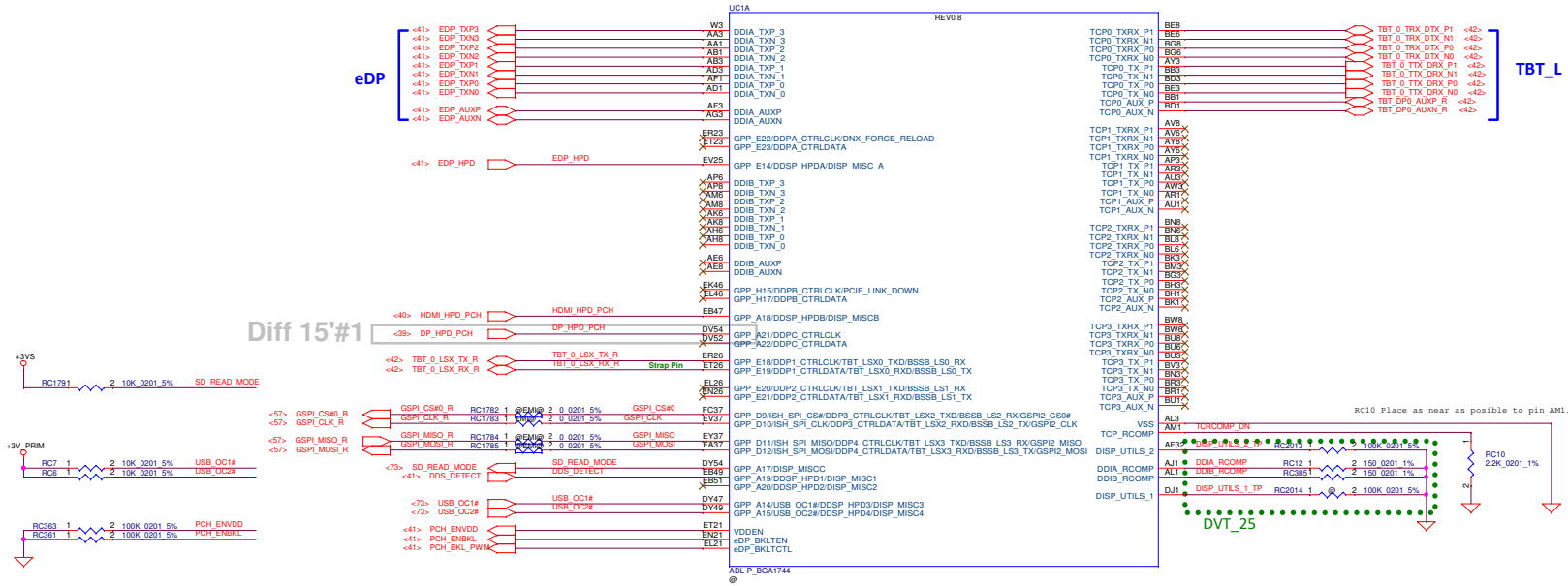
Issued Date	2020/02/27	Deciphered Date 2021/12/31	Title: Power Sequence
			Size: Document Number: LA-L613P Rev: 0.3
			Date: Thursday, November 25, 2021 Sheet 5 of 121



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Compal Electronics, Inc.			
Title: ADL-P(1/13)TCSS,EDP			
Size	Document Number: LA-L613P		Rev: 0.3
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TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

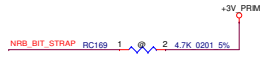
1 = Enable "Top Swap" mode.

NO REBOOT

GPP_B18/GSPI0_MOS (Internal 20 K Pull Down)

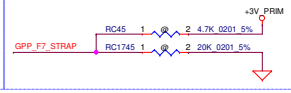
0 = Disable "No Reboot" mode

1 = Enable "No Reboot" mode (This function is useful when running ITP/XDP).



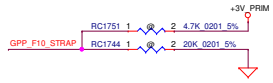
Reserved

GPP_F7 (Weak internal PD 20K)



Reserved

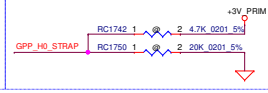
GPP_F10 (Weak internal PD 20K)



BOOT STRAP 1

GPP_H0 (Weak internal PD 20K)

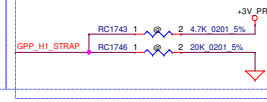
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 2

GPP_H1 (Weak internal PD 20K)

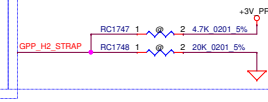
This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.

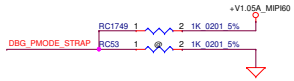


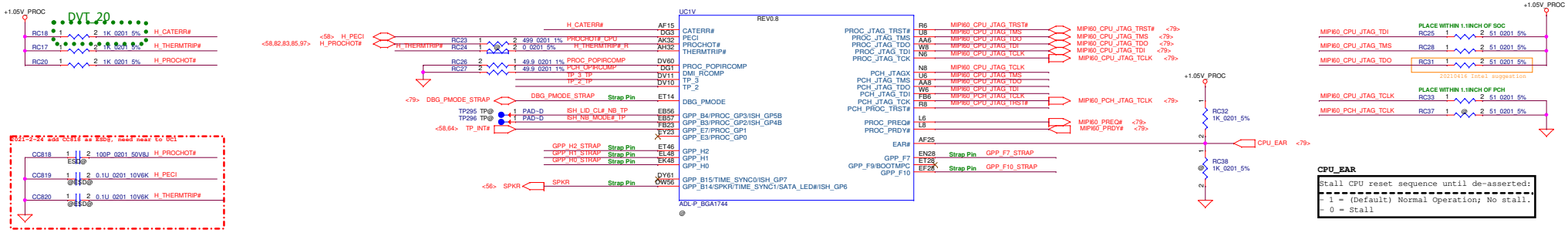
DFXTESTMODE(ITP_PMODE)

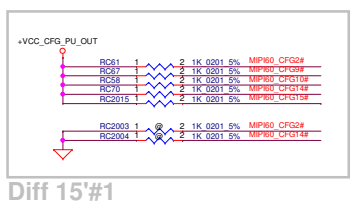
DBG_PMODE (Internal 20 K Pull UP)

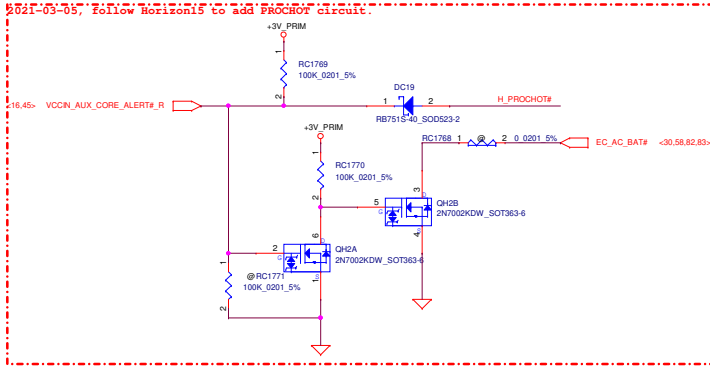
0 = DFXTESTMODE ENABLED

1 = DFXTESTMODE DISABLED(DEFAULT)









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Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	ADL-P(2/13)MISC,MIPI60
Size	Document Number: LA-L613P
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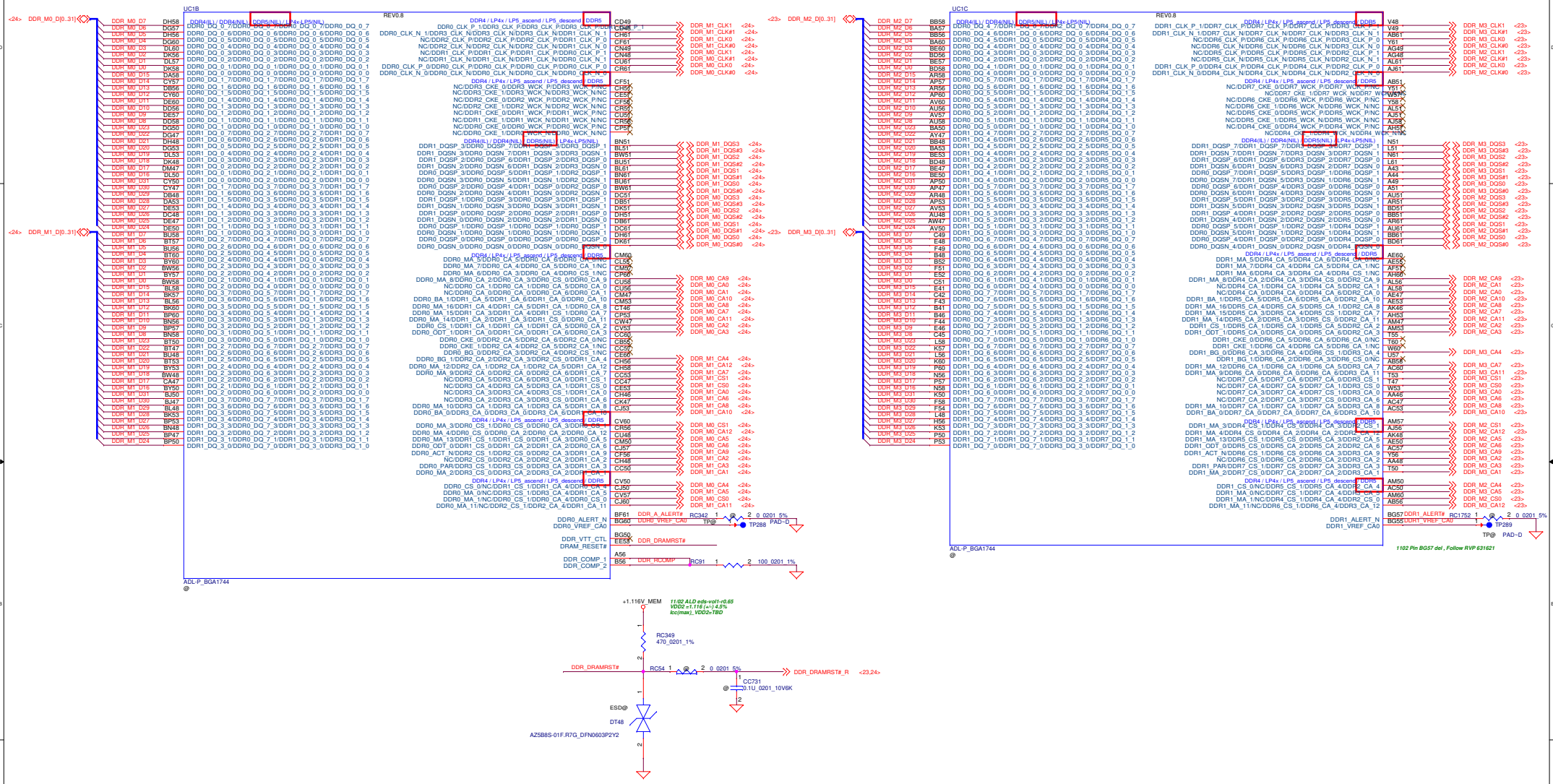

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Compal Electronics, Inc.

Title: **ADL-P(3/13)LPDDR4/x**

Size: — Document Number: **LA-L613P** Rev: 0.3

Date: Thursday, November 25, 2021 Sheet 8 of 121

JTAG ODT disable

GPP_E6 (External pull-up is required)

0: JTAG ODT disable

1: JTAG ODT enable

This strap does not have an internal pull-up or pull-down. External pull-up is recommended

BOOT HALT

SPI0_MOSI(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

CPUNSSC CLOCK FREQ

GPP_B23 (Weak internal PD 20K)

0 = 38.4 MHz clock direct from crystal (default)

1 = 19.2 MHz clock from divider (Device from 38.4MHz crystal)

TLS CONFIDENTIALITY

GPP_C2 (Internal PD 20K)

0 = TLS CONFIDENTIALITY DISABLE

1 = TLS CONFIDENTIALITY ENABLE

CONSENT STRAP

SPI0_IO2(NO INTERNAL PU/PD)

0 = Enable

1 = Disable

PLACE RC115 AND RC122 CLOSE TO THE SPI SIGNAL TO AVOID STUB

A0 PERSONALITY STRAP

SPI0_IO3

0 = Enable

1 = Disable

PLACE RC116 AND RC123 CLOSE TO THE SPI SIGNAL TO AVOID STUB

Boot Strap 0

GPP_C5 (Weak internal PD 20K)

0 = Enable eSPI. (Default)

1 = Disable eSPI.

This strap is used in conjunction with Boot Strap 1,2,3, (on GPP_H0, GPP_H1, GPP_H2 respectively).

0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI enable<--use this

0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.
Others: Reserved.

Diff 15'#1

SPI ROM (32MByte)
ROM is Quad SPI 75%

UC2 W25R256JVEIN WSON 8P_8X6 SA0000DUA00

DC1 @ RB751S-40_SOD523-2

Diff 15'#2

SODIMM1&SODIMM2

BB (For support Vpro)

PD

ESPI 1.8V

DVT_23

UC1E ADL-P_BGA1744 REV0.8

Didn't support C-Link

eSPI Alert 0 (Server Only):Alert signal from eSPI slave to the PCH.
Note: If only a single Slave is connected, the eSPI Compatibility Specification requires that the Slave must operate with in-band Alert# signaling in order to free up the GPIO pin required for the discrete Alert# pin.

*****Need confirm***
PCH EDS P.72 rev0p7

2021-3-3 modify to G2R, follow intel PDG

To SPI ROM

From MIPI60

SPI Topology

PCH — 62-ohm — SPI ROM

JSPI

DVT_02

GPU ID	ID2	ID1	ID0
GN20-E8	H	H	L
GN20-E6	H	L	H
GN20-E7	H	L	L
GN20-E5	L	H	H
GN20-E3	L	H	L
GN20-P1	L	L	H
Intel DG2	L	L	L

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	ADL-P(4/13)SPI,SMB,ESPI
Size	Document Number: LA-L381P
Rev	0.3
Date:	Thursday, November 25, 2021
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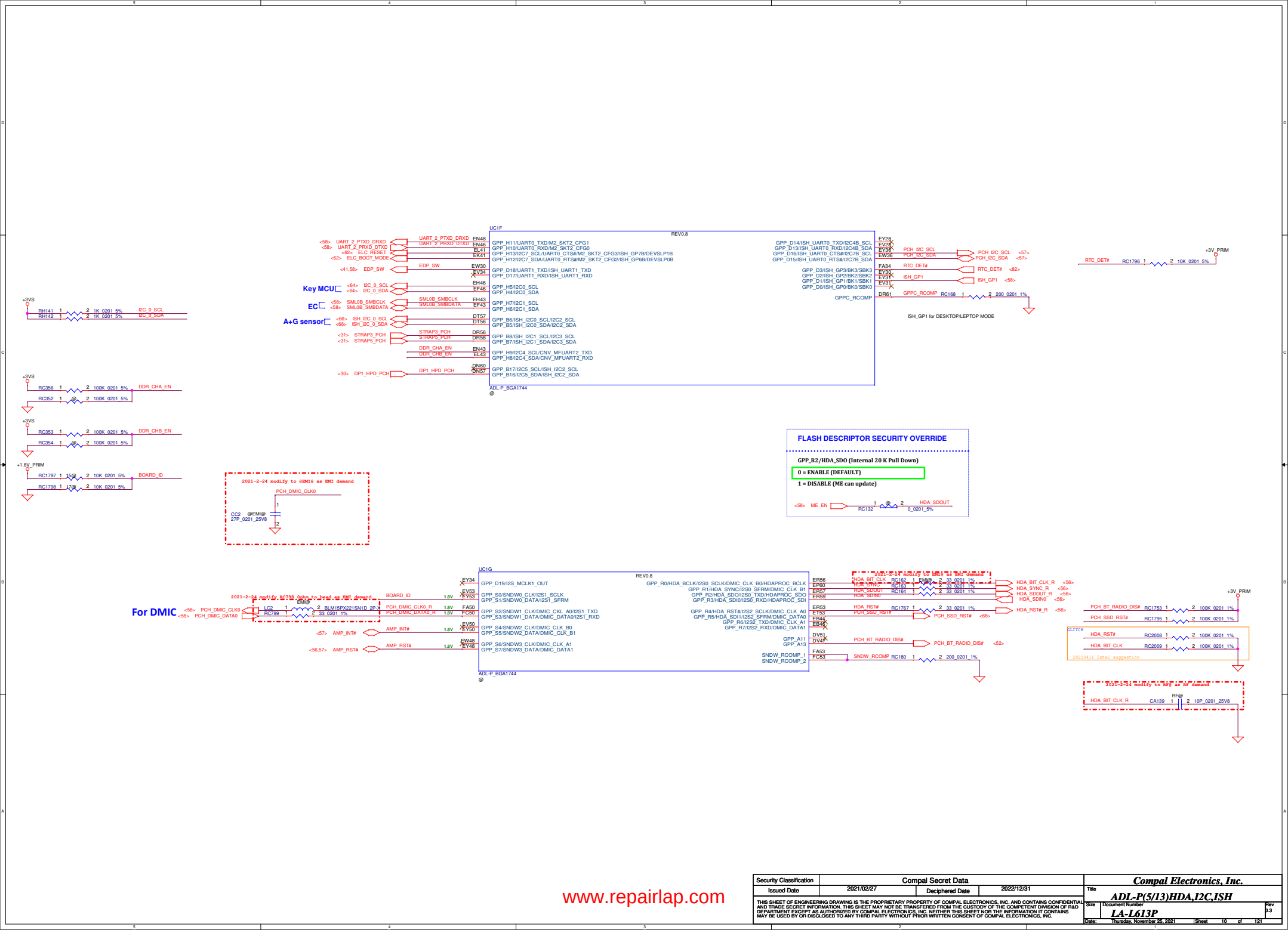

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Compal Electronics, Inc.	
Title	ADL-P(5/13)HDA,I2C,ISH
Size	Document Number: LA-L613P
Rev	0.3
Date:	Thursday, November 25, 2021
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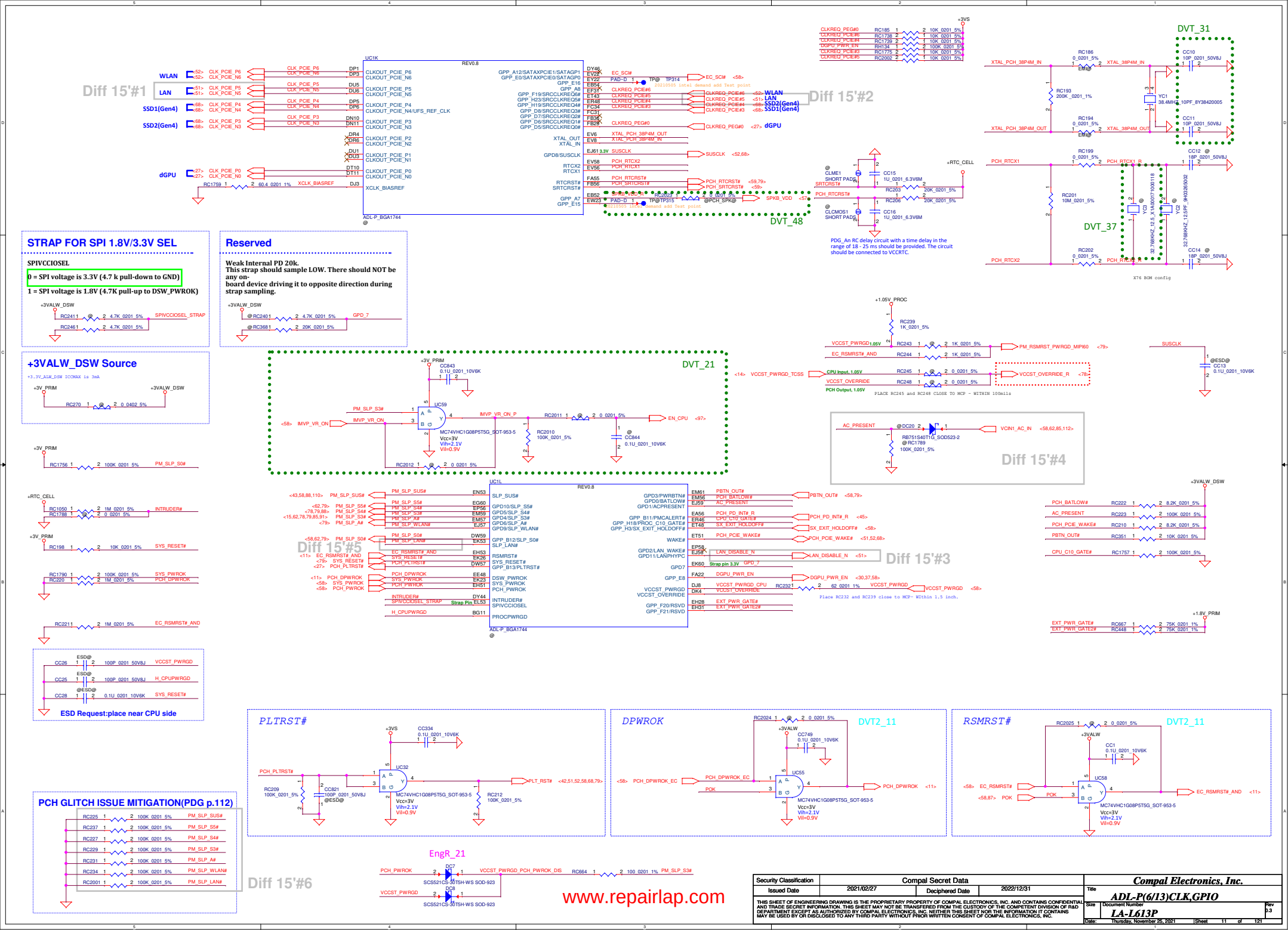
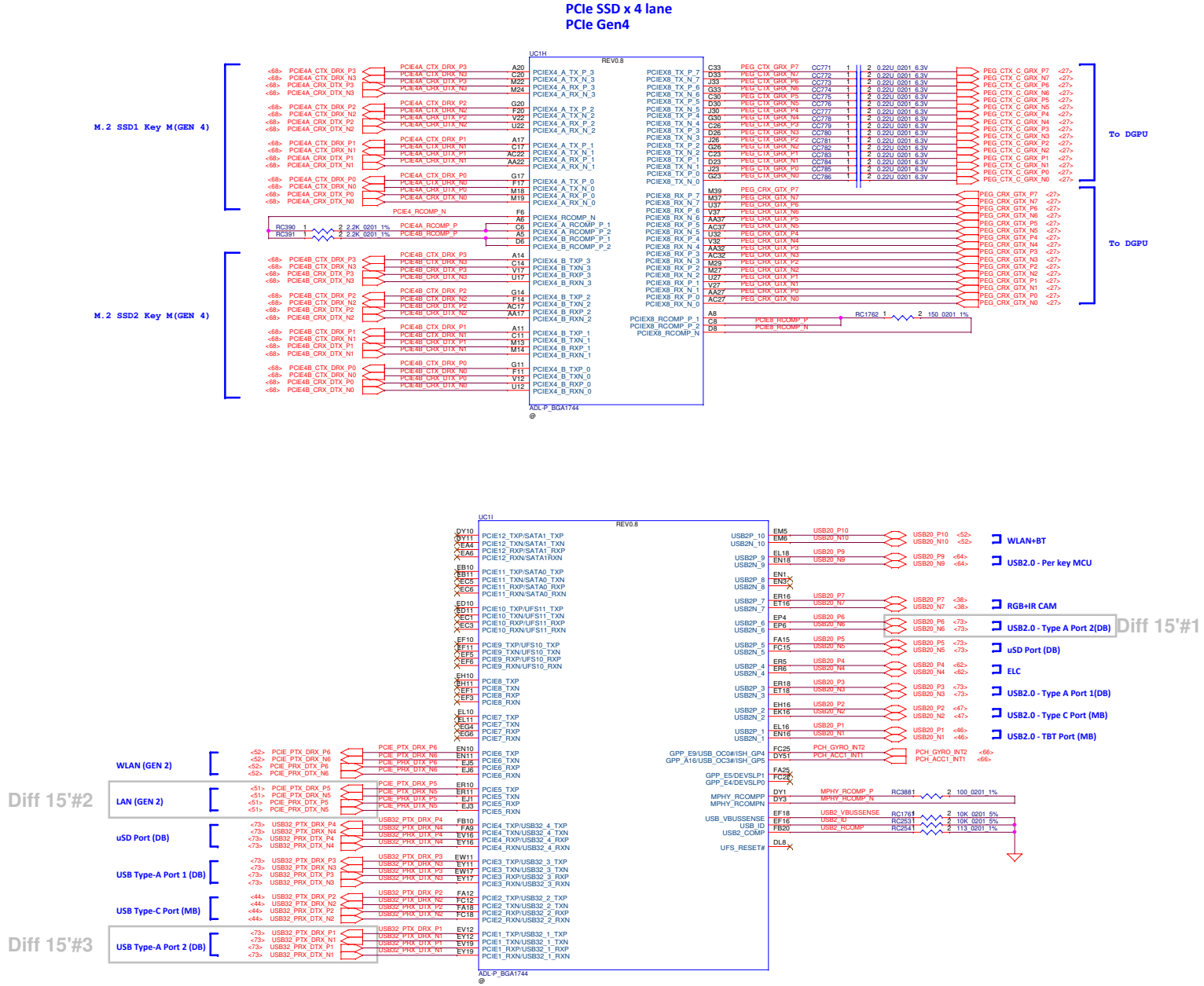
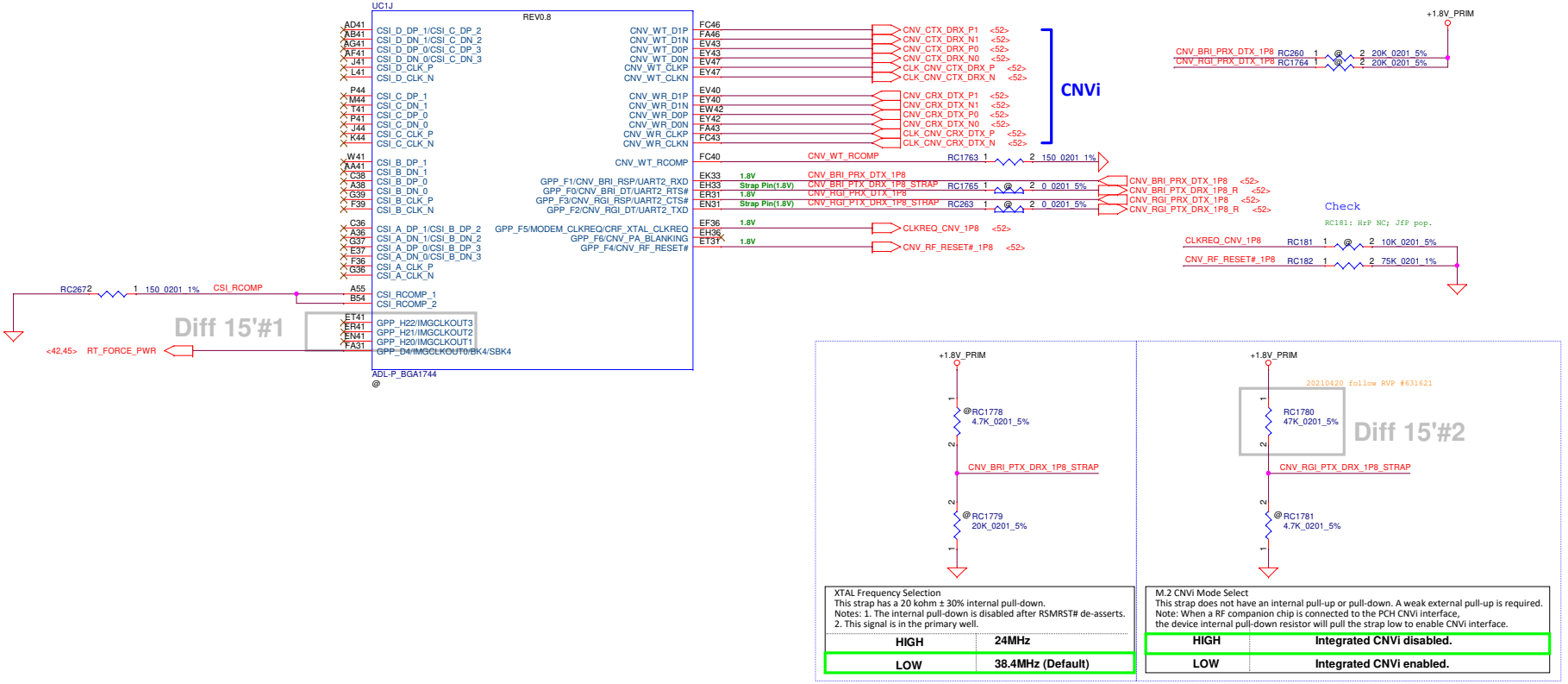

STRAP FOR SPI 1.8V/3.3V SEL
SPIVCCIOSEL
0 = SPI voltage is 3.3V (4.7 k pull-down to GND)
1 = SPI voltage is 1.8V (4.7K pull-up to DSW_PWROK)
Reserved
Weak Internal PD 20k.
This strap should sample LOW. There should NOT be any on-
board device driving it to opposite direction during strap sampling.
+3VALW_DSW Source
ESD Request:place near CPU side
PCH GLITCH ISSUE MITIGATION(PDG p.112)
Diff 15'#1
Diff 15'#2
Diff 15'#3
Diff 15'#4
Diff 15'#5
Diff 15'#6
DVT_21
DVT_31
DVT_48
DVT_37
PDG_An RC delay circuit with a time delay in the range of 18 - 25 ms should be provided. The circuit should be connected to VCCRTC.
PLTRST#
DPWROK
RSMRST#
EngR_21
www.repairlap.com
Compal Electronics, Inc.
ADL-P(6/13)CLK,GPIO
LA-L613P
Thursday, November 25, 2021



Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	ADL-P(7/13)PCIE,USB		
Size	Document Number		Rev
	LA-L613P		0.3
Date:	Thursday, November 25, 2021	Sheet	12 of 121



Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: **ADL-P(8/13)CSI,CNVi**

Size	Document Number	Rev
	LA-L613P	0.3

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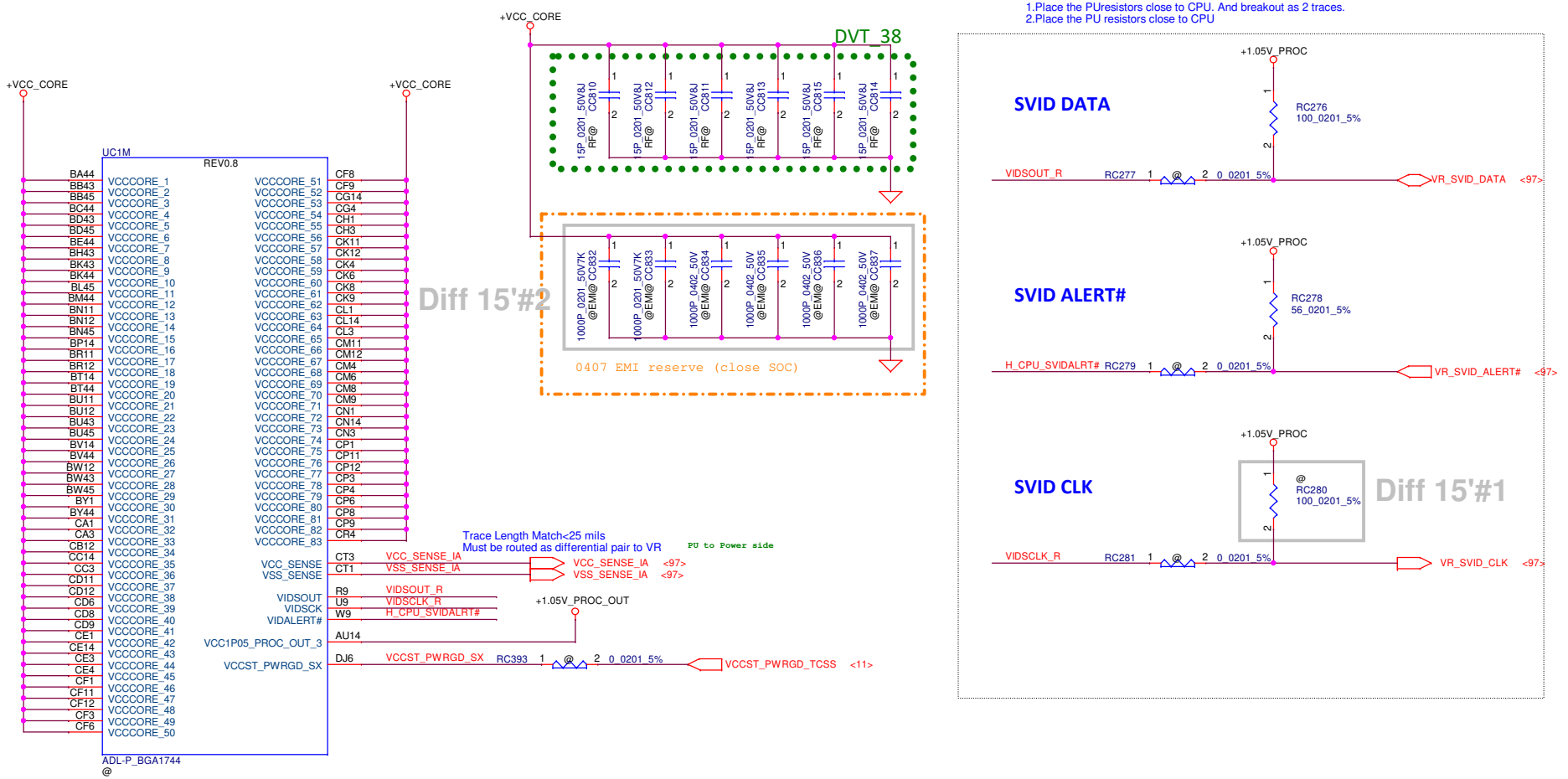

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	ADL-P(9/13)CPU PWR,SVID		
Size	Document Number		Rev
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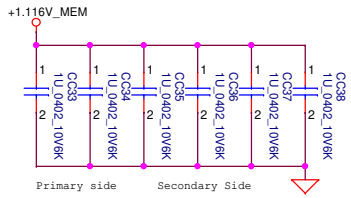
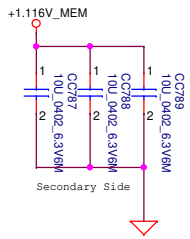
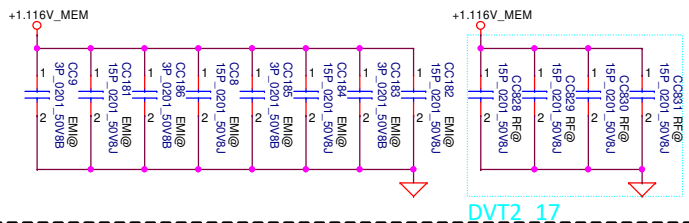
Primary side Cap
2x 1uF 0402
Secondary Side Cap
4x 1uF 0402
3x 10uF 0402

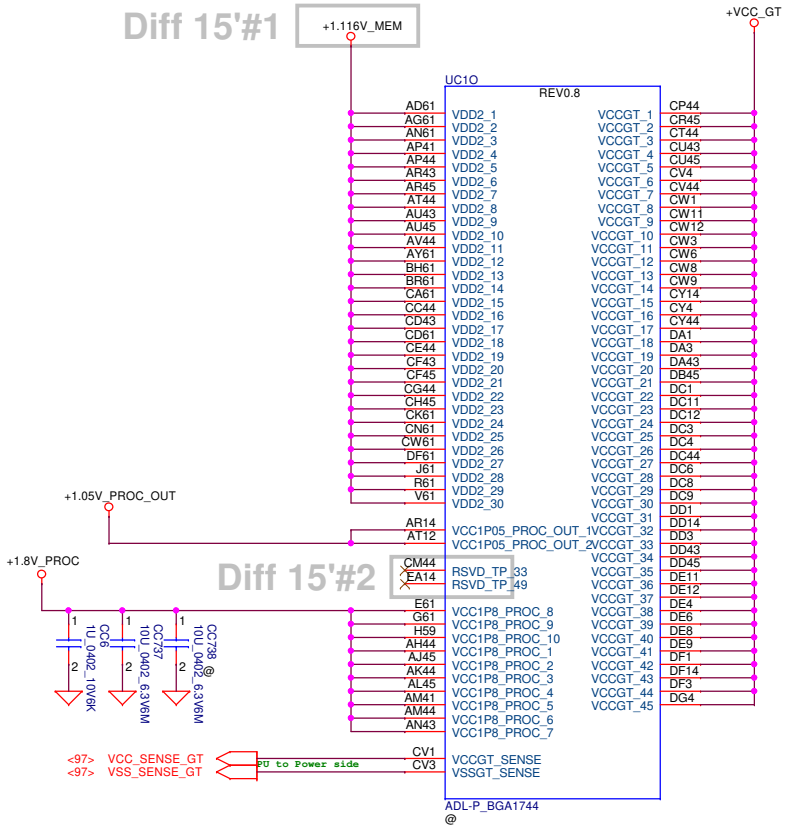




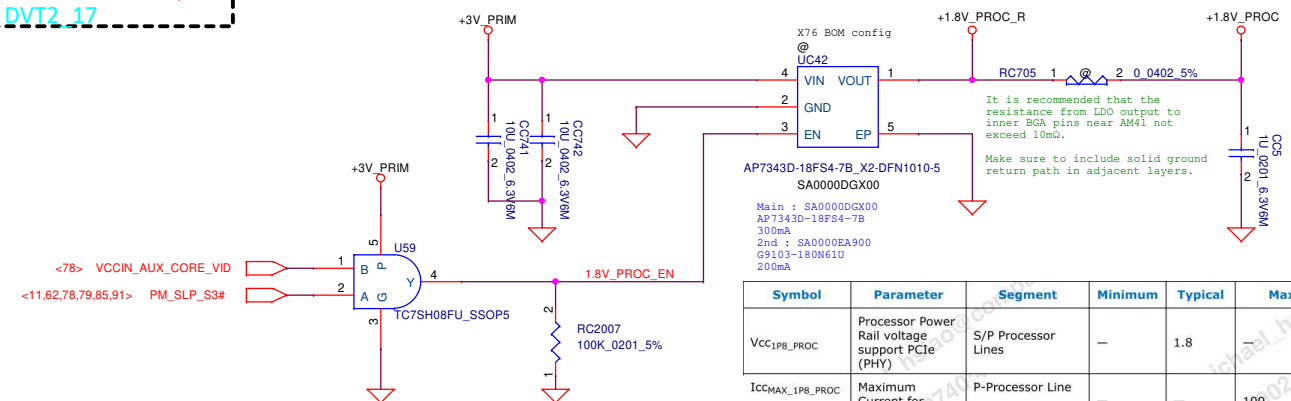
EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART



Diff 15'#1



Need to check PDG Output Current



Symbol	Parameter	Segment	Minimum	Typical	Maximum	Units	Notes [1,2,5]
Vcc_{1P8_PROC}	Processor Power Rail voltage support PCIe (PHY)	S/P Processor Lines	—	1.8	—	V	3
$Icc_{MAX\_1P8\_PROC}$	Maximum Current for Vcc_{1P8_PROC}	P-Processor Line	—	—	100	mA	4

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Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: ADL-P(10/13)CPU PWR

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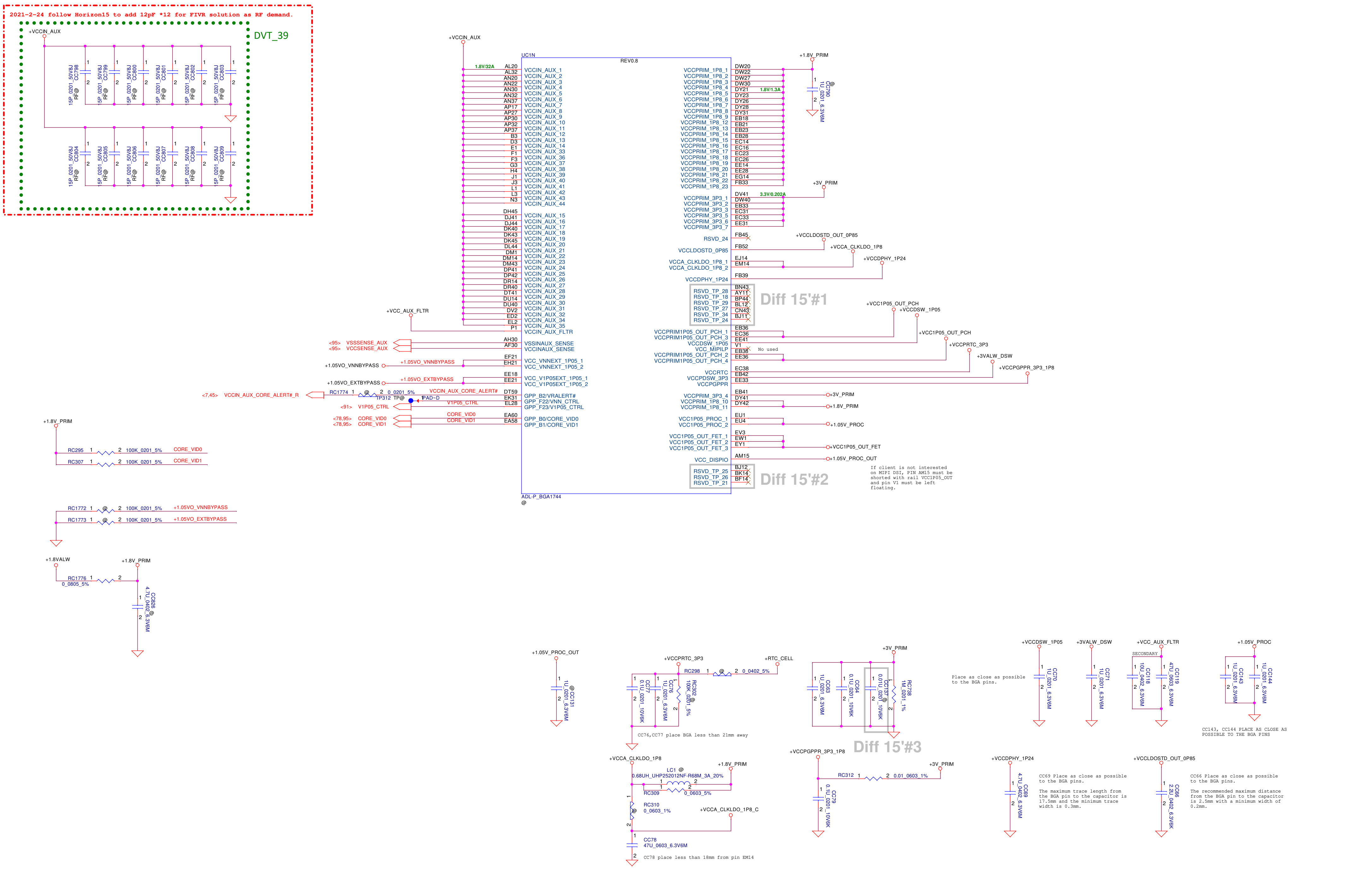
2021-2-24 follow Horizon15 to add 12pF *12 for FIVR solution as RF demand.
DVT_39
+VCCIN_AUX
CC798 CC799 CC800 CC801 CC802 CC803
CC804 CC805 CC806 CC807 CC808 CC809
15P_0201_50V8J
RF@
UC1N
REV0.8
1.8V/32A
VCCIN_AUX_1
VCCIN_AUX_FLTR
VSSINAUX_SENSE
VCCINAUX_SENSE
VCC_VNNEXT_1P05_1
VCC_VNNEXT_1P05_2
VCC_V1P05EXT_1P05_1
VCC_V1P05EXT_1P05_2
GPP_B2/VRALERT#
GPP_F22/VNN_CTRL
GPP_F23/V1P05_CTRL
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1
ADL-P_BGA1744
+1.8V_PRIM
1.8V/1.3A
CC790
1U_0201_6.3V6M
+3V_PRIM
3.3V/0.202A
VCCPRIM_1P8_1
VCCPRIM_3P3_1
RSVD_24
VCCLDOSTD_0P85
VCCA_CLKLDO_1P8_1
VCCA_CLKLDO_1P8_2
VCCDPHY_1P24
Diff 15'#1
VCCPRIM1P05_OUT_PCH_1
VCCDSW_1P05
VCC_MIPILP
No used
VCCRTC
VCCPDSW_3P3
VCCPGPPR
VCC1P05_PROC_1
VCC1P05_OUT_FET_1
VCC_DISPIO
Diff 15'#2
If client is not interested on MIPI DSI, PIN AM15 must be shorted with rail VCC1P05_OUT and pin V1 must be left floating.
<95> VSSSENSE_AUX
<95> VCCSENSE_AUX
+1.05VO_VNNBYPASS
+1.05VO_EXTBYPASS
<7,45> VCCIN_AUX_CORE_ALERT#_R
RC1774
0_0201_5%
TP312 TP@
PAD~D
<91> V1P05_CTRL
<78,95> CORE_VID0
<78,95> CORE_VID1
RC295 100K_0201_5%
RC307 100K_0201_5%
RC1772 100K_0201_5%
RC1773 100K_0201_5%
+1.8VALW
RC1776 0_0805_5%
CC826 4.7U_0402_6.3V6M
+1.05V_PROC_OUT
CC131 1U_0201_6.3V6M
+VCCPRTC_3P3
+RTC_CELL
RC298 0_0402_5%
RC302 100K_0201_5%
CC76 1U_0201_6.3V6M
CC77 0.1U_0201_10V6K
CC76,CC77 place BGA less than 21mm away
CC63 1U_0201_6.3V6M
CC64 0.1U_0201_10V6K
CC137 0.01U_0201_10V6K
RC738 1M_0201_1%
Diff 15'#3
Place as close as possible to the BGA pins.
+VCCDSW_1P05
CC70 1U_0201_6.3V6M
+3VALW_DSW
CC71 1U_0201_6.3V6M
+VCC_AUX_FLTR
SECONDARY
CC118 10U_0402_6.3V6M
CC119 47U_0603_6.3V6M
+1.05V_PROC
CC143 1U_0201_6.3V6M
CC144 1U_0201_6.3V6M
CC143, CC144 PLACE AS CLOSE AS POSSIBLE TO THE BGA PINS
+VCCA_CLKLDO_1P8
LC1 0.68UH_UHP252012NF-R68M_3A_20%
RC309 0_0603_5%
RC310 0_0603_1%
+VCCA_CLKLDO_1P8_C
CC78 47U_0603_6.3V6M
CC78 place less than 18mm from pin EM14
+VCCPGPPR_3P3_1P8
RC312 0.01_0603_1%
CC79 0.1U_0201_10V6K
+VCCDPHY_1P24
CC69 4.7U_0402_6.3V6M
CC69 Place as close as possible to the BGA pins.
The maximum trace length from the BGA pin to the capacitor is 17.5mm and the minimum trace width is 0.3mm.
+VCCLDOSTD_OUT_0P85
CC66 2.2U_0402_6.3V6K
CC66 Place as close as possible to the BGA pins.
The recommended maximum distance from the BGA pin to the capacitor is 2.5mm with a minimum width of 0.2mm.

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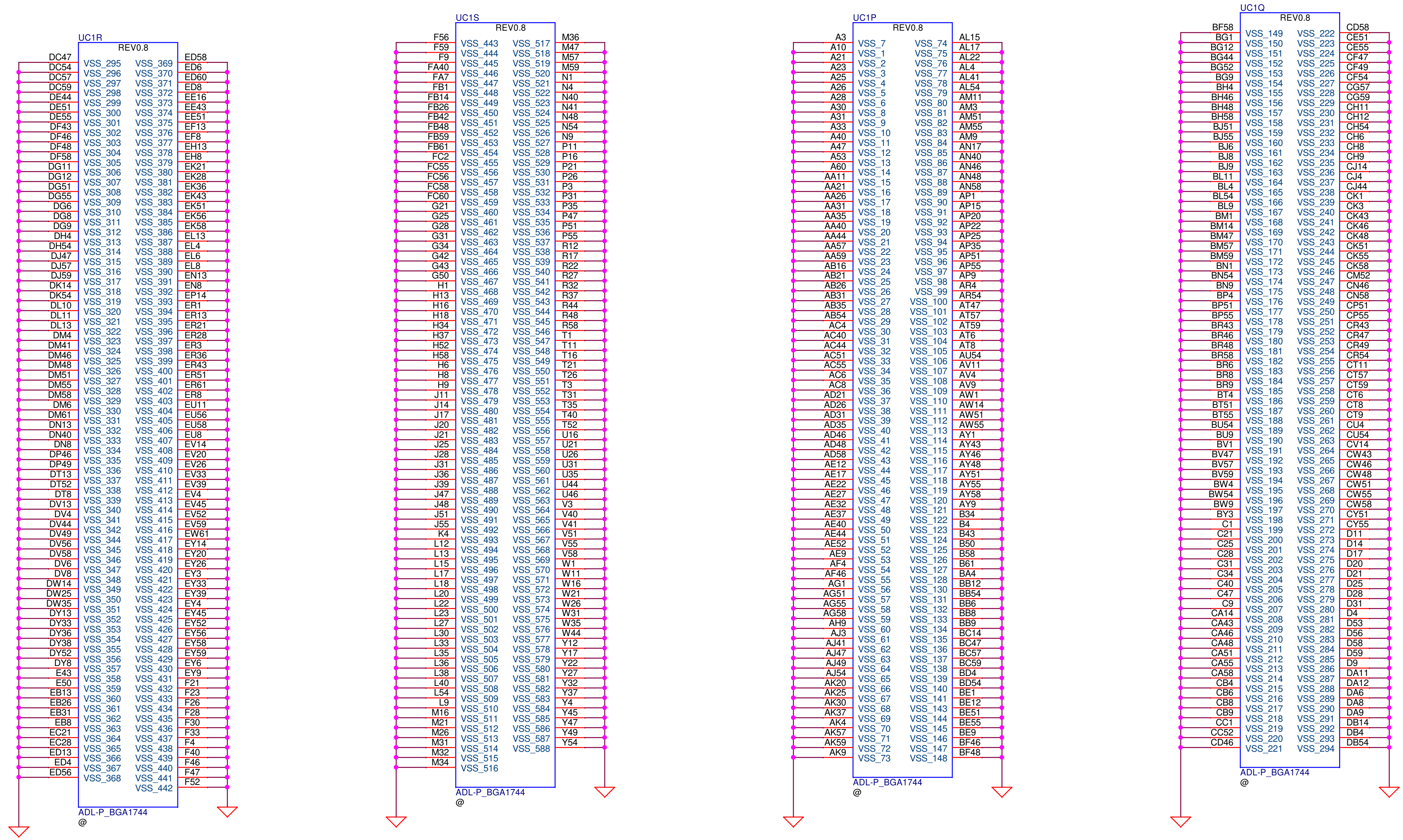
			Date: Thursday, November 25, 2021 / Sheet 16 of 121



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Issued Date	2021/02/27	Deciphered Date	2022/12/31

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Compal Electronics, Inc.

Title: *ADL-P(12/13)GND*

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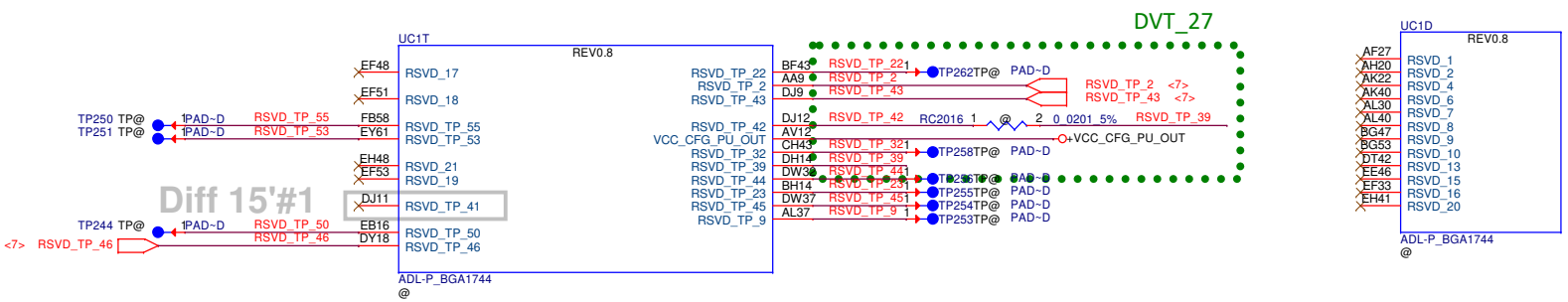

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	ADL-P(13/13)RSVD		
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Reserve

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Compal Electronics, Inc.

Title	*Reserve*	
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Reserve

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: *Reserve*

Size | Document Number: *LA-L613P* | Rev 0.3

Date: Thursday, November 25, 2021 |

Reserve

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title	*Reserve*	
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VRAM X76 BOM

ZZZ2 X76VS6G@ — **Samsung 6GB**
ALT. GROUP PARTS VRAM 6G SAM HDS70 X76891311B1

ZZZ3 X76VM6G@ — **Micron 6GB**
ALT. GROUP PARTS VRAM 6G MIC HDS70 X76891311B2

ZZZ4 X76VH6G@ — **Hynix 6GB**
ALT. GROUP PARTS VRAM 6G HYN HDS70 X76891311B3

ZZZ5 X76VS8G@ — **Samsung 8GB**
ALT. GROUP PARTS VRAM 8G SAM HDS70 X76891311B4

ZZZ6 X76VM8G@ — **Micron 8GB**
ALT. GROUP PARTS VRAM 8G MIC HDS70 X76891311B5

ZZZ7 X76VH8G@ — **Hynix 8GB**
ALT. GROUP PARTS VRAM 8G HYN HDS70 X76891311B6

ZZZ14 X76VS16G_16G@ — **Samsung 16GB** **16Gbps**
ALT. GROUP PARTS VRAM 16G SAM E6E8 HDS70 X76891311B8

ZZZ8 X76VS16G@ — **Samsung 16GB**
ALT. GROUP PARTS VRAM 16G SAM HDS70 X76891311B7

8G bit GDDR6 GN20-E3

Micron 6G Byte

R1 SA0000BND6L

UM11 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UM3 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UM12 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UM4 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UM9 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L
UM10 VM6GR1@ MT61K256M32JE-14:A SA0000BND6L

R3 SA0000BND7L

UM11 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UM3 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UM12 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UM4 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UM9 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L
UM10 VM6GR3@ MT61K256M32JE-14:A SA0000BND7L

Samsung 6G Byte

R1 SA0000C625L

UM11 VS6GR1@ K4Z80325BC-HC14 SA0000C625L
UM3 VS6GR1@ K4Z80325BC-HC14 SA0000C625L
UM12 VS6GR1@ K4Z80325BC-HC14 SA0000C625L
UM4 VS6GR1@ K4Z80325BC-HC14 SA0000C625L
UM9 VS6GR1@ K4Z80325BC-HC14 SA0000C625L
UM10 VS6GR1@ K4Z80325BC-HC14 SA0000C625L

R3 SA0000C626L

UM11 VS6GR3@ K4Z80325BC-HC14 SA0000C626L
UM3 VS6GR3@ K4Z80325BC-HC14 SA0000C626L
UM12 VS6GR3@ K4Z80325BC-HC14 SA0000C626L
UM4 VS6GR3@ K4Z80325BC-HC14 SA0000C626L
UM9 VS6GR3@ K4Z80325BC-HC14 SA0000C626L
UM10 VS6GR3@ K4Z80325BC-HC14 SA0000C626L

Hynix 6G Byte

R1 SA0000DUW0L

UM11 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM3 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM12 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM4 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM9 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM10 VH6GR1@ H56C8H24AIR-S2C SA0000DUW0L

R3 SA0000DUW1L

UM11 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM3 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM12 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM4 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM9 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM10 VH6GR3@ H56C8H24AIR-S2C SA0000DUW1L

8G bit GDDR6 GN20-E6

Micron 8G Byte

R1 SA0000BND6L

UM11 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM3 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM12 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM4 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM9 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM1 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM10 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L
UM2 VM8GR1@ MT61K256M32JE-14:A SA0000BND6L

R3 SA0000BND7L

UM11 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM3 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM12 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM4 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM9 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM1 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM10 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L
UM2 VM8GR3@ MT61K256M32JE-14:A SA0000BND7L

Samsung 8G Byte

R1 SA0000C625L

UM11 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM3 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM12 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM4 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM9 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM1 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM10 VS8GR1@ K4Z80325BC-HC14 SA0000C625L
UM2 VS8GR1@ K4Z80325BC-HC14 SA0000C625L

R3 SA0000C626L

UM11 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM3 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM12 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM4 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM9 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM1 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM10 VS8GR3@ K4Z80325BC-HC14 SA0000C626L
UM2 VS8GR3@ K4Z80325BC-HC14 SA0000C626L

Hynix 8G Byte

R1 SA0000DUW0L

UM11 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM3 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM12 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM4 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM9 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM1 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM10 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L
UM2 VH8GR1@ H56C8H24AIR-S2C SA0000DUW0L

R3 SA0000DUW1L

UM11 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM3 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM12 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM4 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM9 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM1 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM10 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L
UM2 VH8GR3@ H56C8H24AIR-S2C SA0000DUW1L

16G bit GDDR6 GN20-E8

Samsung 16G Byte (16Gbps)

R1 SA0000DYL2L

UM11 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM3 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM12 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM4 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM9 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM1 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM10 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L
UM2 VNS16GR1@ K4ZAF325BM-HC16 SA0000DYL2L

R3 SA0000DYL3L

UM11 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM3 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM12 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM4 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM9 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM1 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM10 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L
UM2 VNS16GR3@ K4ZAF325BM-HC16 SA0000DYL3L

16G bit GDDR6 GN20-E7

Samsung 16G Byte

R1 SA0000CBG0L

UM11 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM3 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM12 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM4 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM9 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM1 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM10 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L
UM2 VS16GR1@ K4ZAF325BM-HC14 SA0000CBG0L

R3 SA0000CBG2L

UM11 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM3 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM12 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM4 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM9 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM1 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM10 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L
UM2 VS16GR3@ K4ZAF325BM-HC14 SA0000CBG2L

Crystal 3215

ZZZ19 X76_3215@ ALT. GROUP PARTS CRYSTAL 3215 EE HDS50 X76891311LBF
YC2 3215@ S CRYSTAL 32.768KHZ 12.5PF 9H03265002 SJ1000171V00
CC12 3215@ S CER CAP 15P 50V J NPO 0201 SE000007D00
CC14 3215@ S CER CAP 15P 50V J NPO 0201 SE000007D00

Crystal 2012

ZZZ20 X76_2012@ ALT. GROUP PARTS CRYSTAL 2012 EE HDS50 X76891311LBJ
YC3 2012@ S CRYSTAL 32.768KHZ X1A000171000118 SJ1000151U00
CC12 2012@ S CER CAP 18P 25V J NPO 0201 SE000004H00
CC14 2012@ S CER CAP 18P 25V J NPO 0201 SE000004H00

LDO

Main DII

ZZZ17 X76DII@ ALT. GROUP PARTS DII LDO 15E EE HDS50 X76891311LBH
UC42 1V8_DII@ S IC D5 32G MT62F1G32D4DR-031 WT:B S SA0000DGX00

2nd GMT

ZZZ18 X76GMT@ AP7343D-18FS4-7B_X2-DFN1010-5 X76891311LBI
UC42 1V8_GMT@ S IC G9103-180N61U UDFN 4P LDO SA0000EA900

OVR-M

ZZZ22 X76ONOVRM@ ONSEMIGEN2OVRM HDS70 X76891311LBJ
UG11 **On-Semi Gen2** NCP454954XMNTWG_QFN32_4X4 SA0000DUX00 ONOVRM@

ZZZ23 X76UPIOVRM@ UPI GEN2 OVRM HDS70 X76891311LBT
UG11 **uPI Gen2** US5651AQKI WQFN 32P POWER MONITOR SA0000DY100 UPIOVRM@

Analog Switch

Main 5V

ZZZ24 X76TI5V@ ALT. GROUP PARTS TI 5V HDS70 X76891311LBV
TI_5V@ RV1010 0_0201_5%
UV31 TI_5V@ TPS63154DCUR SA0000962B00
UG66 TI_5V@ TPS63154DCUR SA0000962B00

2nd 3V

ZZZ25 X76TI3V@ ALT. GROUP PARTS TI 3V HDS70 X76891311LBW
TI_3V@ RV1009 0_0201_5%
UV31 TI_3V@ TPS62053DCUR SA0000FC300
UG66 TI_3V@ TPS62053DCUR SA0000FC300

WLAN

UWL1 **GFP4** AX411.E2WGNVXE2 PX29500CR0L GFP4@
UWL1 **GFP2** INTEL AX211.D2WD.NVX W/BT PX29500CM7L GFP2@

HDMI LOGO

ZZZ21 HDMI45@ HDMI W/LOGO + HDCP PO0000003HM

BB

URT1 **R1** JHL8040R QURW A1 SA0000CAH10 TBT@
URT1 **R3** JHL8040R SLMN7 A1 SA0000CAH3L TBTR3@

EC

UE5 KB9542G-F_VFBGA124 SA0000BPU30 EC@

PCB

ZZZ LA-L613P DAB0005J011 PCB@

DAB0009J011PCB 3g3 LA-L613P REV1 MB GN20-E GOLD A31 !
DAB0009J012PCB 3g3 LA-L613P REV1 MB GN20-E TRIPOD A31 !
DAB0009J013PCB 3g3 LA-L613P REV1 MB GN20-E UNITECH A31 !

CPU

UC1 **MP R3 - 6+8 I7-12700H** S IC FJ8071504786106 SRLD1 L0 2.3G A31 ! SA000F70L SRLD1@
UC1 **MP R3 - 6+8 I9-12900H** S IC FJ8071504786411 SRLD4 L0 2.5G A31 ! SA000F8F2L SRLD4@
UC1 **MP R3 - 6+8 I9-12900HK** S IC FJ8071504786312 SRLD3 L0 2.5G A31 ! SA000F8G2L SRLD3@

GPU

UG1 **GN20-E3 MP** S IC GN20-E3-A1 FCBGA 2714 GPU A31 ! SA0000E194L GN20_E3@
UG1 **GN20-E6 MP R3** S IC GN20-E6-A1 FCBGA 2714 GPU A31 ! SA0000E03SL GN20_E6@
UG1 **GN20-E8 MP R3** S IC GN20-E8-A1 FCBGA 2714 GPU A31 ! SA0000E04SL GN20_E8@
UG1 **GN20-E7 MP** S IC GN20-E7-A1 BGA 2714 GPU A31 ! SA000UDUM1L GN20_E7@

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Issued Date	2021/02/27	Deciphered Date 2022/12/31	Title

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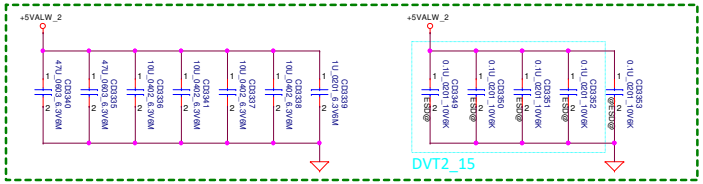
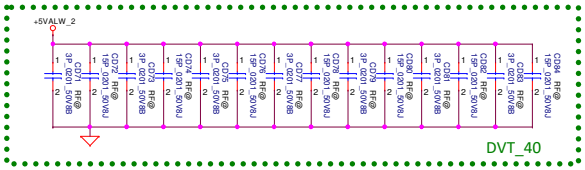
Diff 15'#1

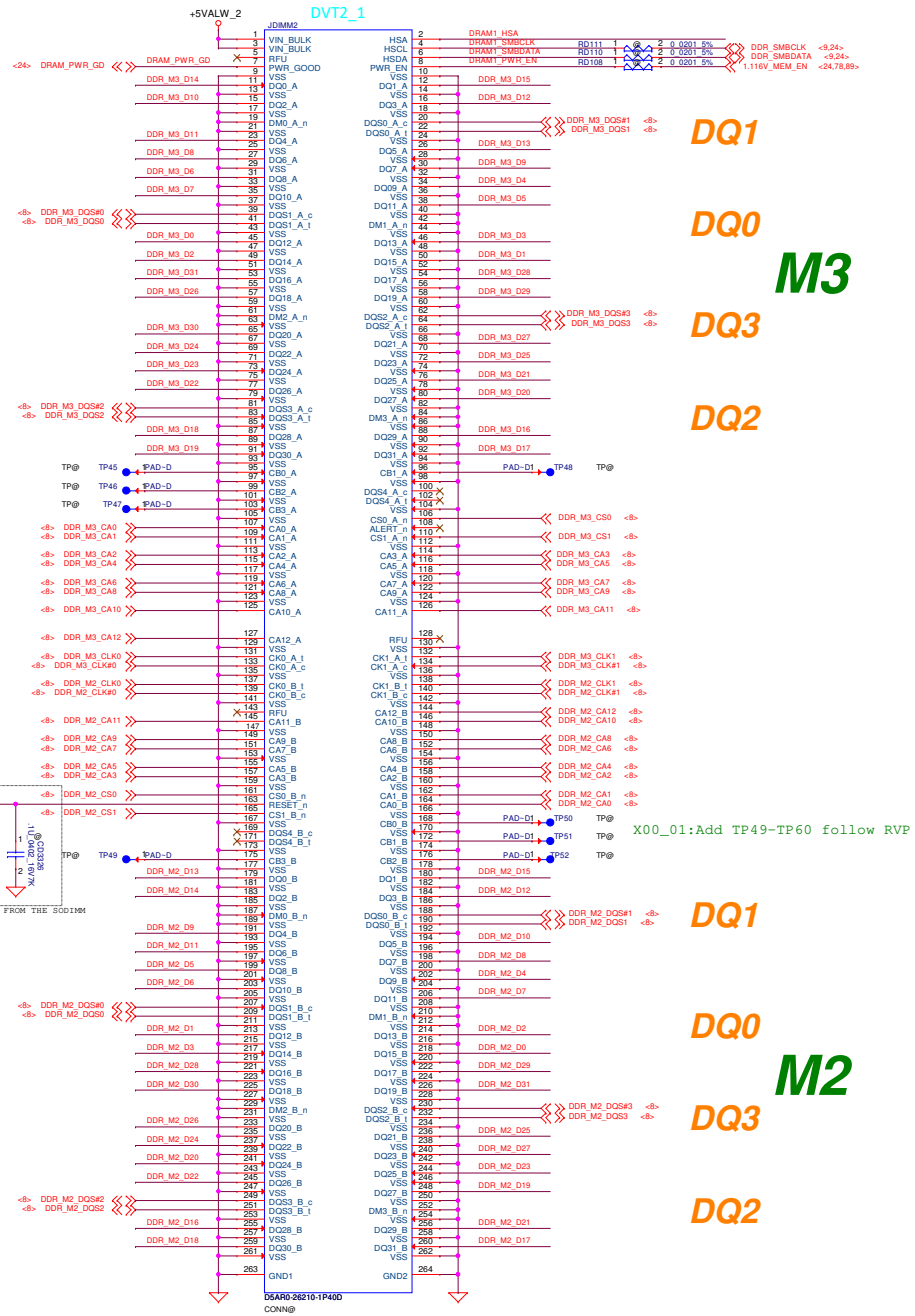
Reverse type connector



1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.

11/02 ALD RVP document 631621
HID address for 2nd DIMM is 010 and resistor value is 23.2K





X00_01:Add TP49-TP60 follow RVP

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Compal Electronics, Inc.	
Title	DDR5 DIMMA
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Diff 15'#1

Standard type connector

Layout Note:
Place near JDIMM2.257,259

1104 DDR5 SODIMM request ,+5V_BULK_DRAM cap.

DVT2_1

DVT_41

DVT2_18

DVT2_16

03/29 ALD RVP document 631621 R0P72
HID address for 1st DIMM is 000 and resistor value is 10K

PLACE THE CAP WITHIN 200 MILS FROM THE SODIMM

X00_01:Add TP49-TP60 follow RVP

DQ3 M1 DQ2 DQ1 DQ0

DQ1 M0 DQ0 DQ3 DQ2

www.repairlap.com

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Compal Electronics, Inc.

Title: DDR5 DIMMB

Size: | Document Number: LA-L613P | Rev: 0.3

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Compal Electronics, Inc.

Title: **Reserve**

Size	Document Number	Rev
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Diff 15'#1

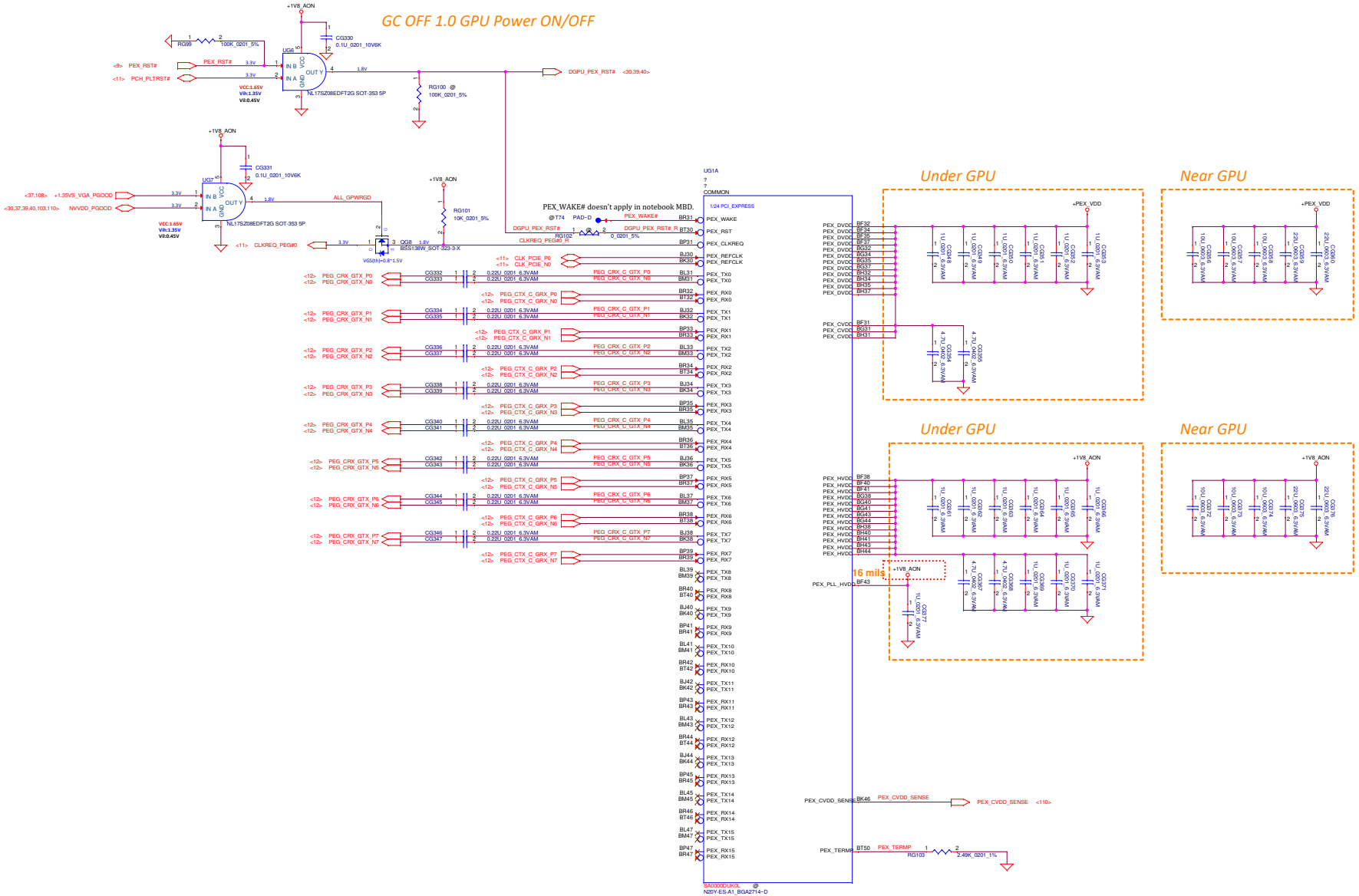
Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: **Reserve**

Size | Document Number: **LA-L613P** | Rev: 0.3

Date: Thursday, November 25, 2021 | Sheet 26 of 121



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date 2022/12/31	Title: NV(1/8) PCI EXPRESS
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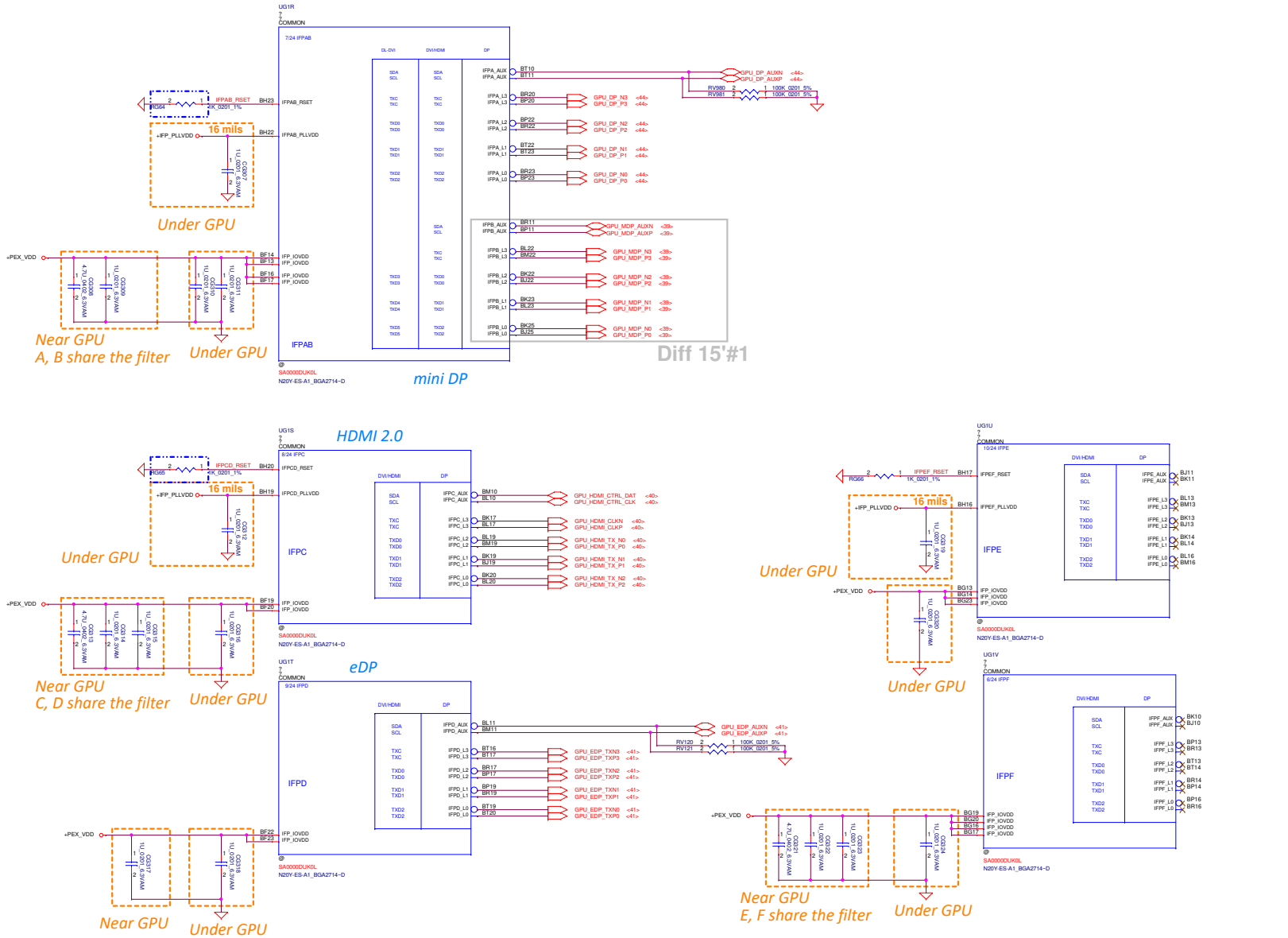
			Date: Thursday, November 25, 2021 Sheet 27 of 121



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date	2022/12/31
Title	NV(2/8) IFP_ABCDEF		
Size	Document Number		Rev
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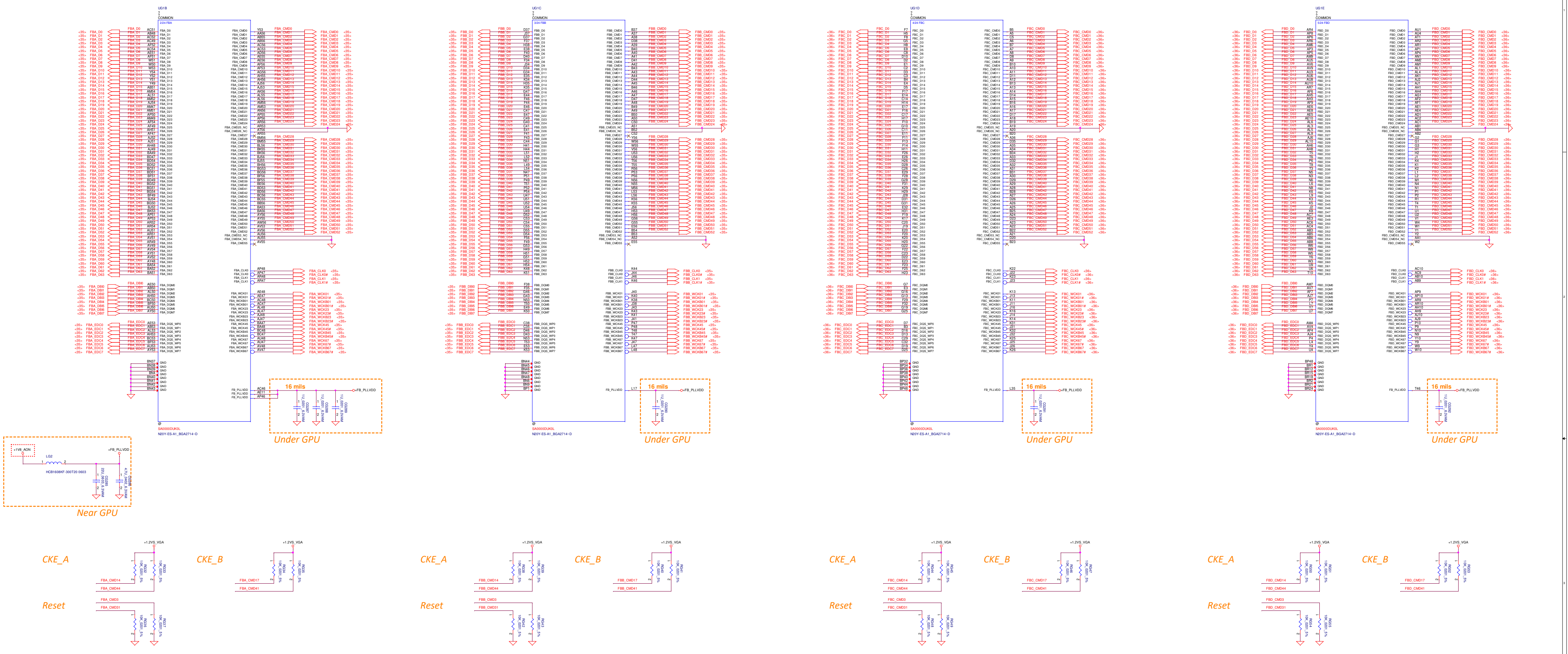


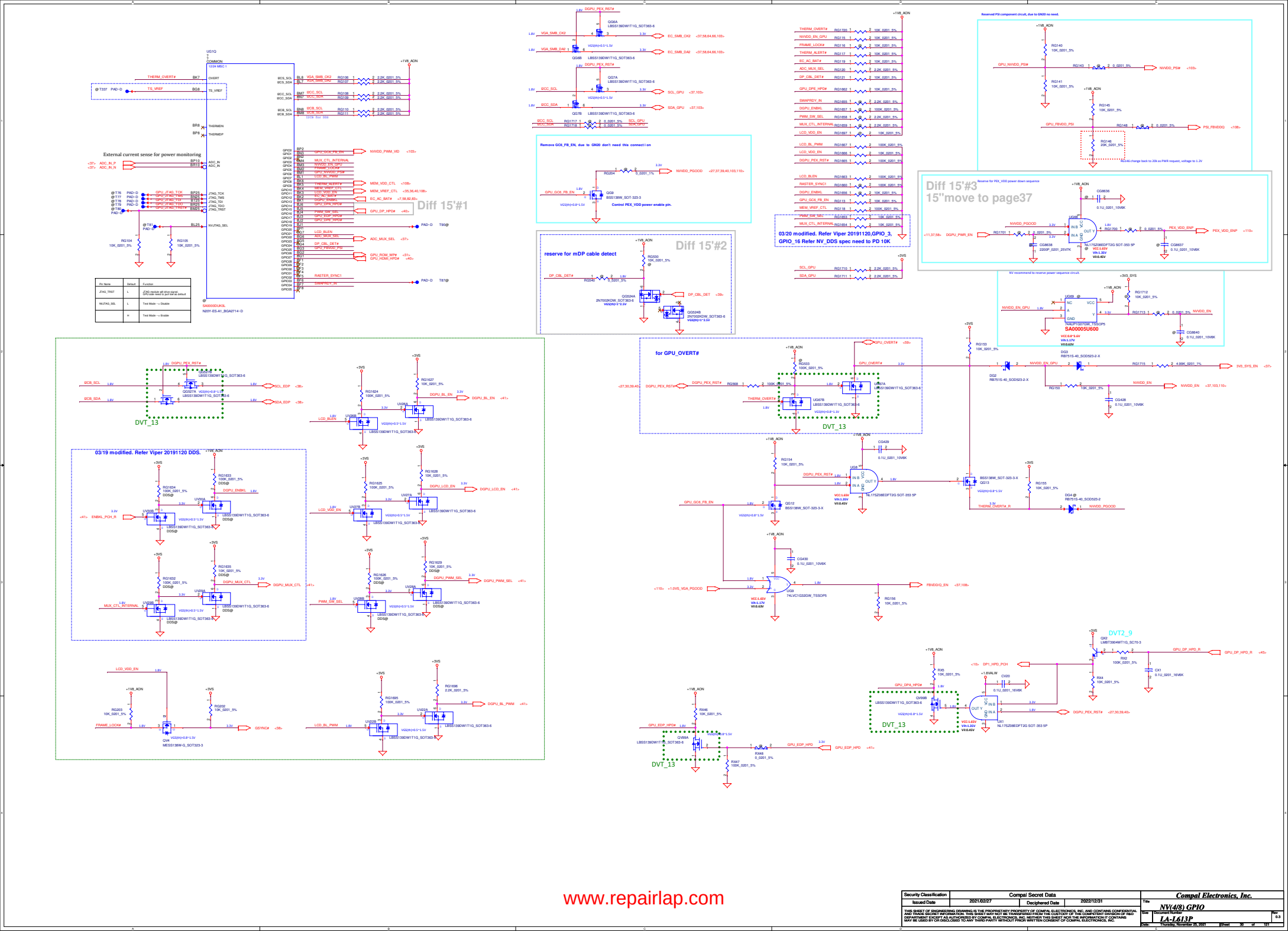
Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: **NV(3/8) MEMORY_FB_ABCD**

Size | Document Number: **LA-L613P** | Rev 0.3

Date: Thursday, November 25, 2021 |



Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

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Compal Electronics, Inc.

Title: **NV(4/8) GPIO**

Size: | Document Number: **LA-L613P** | Rev: 0.3

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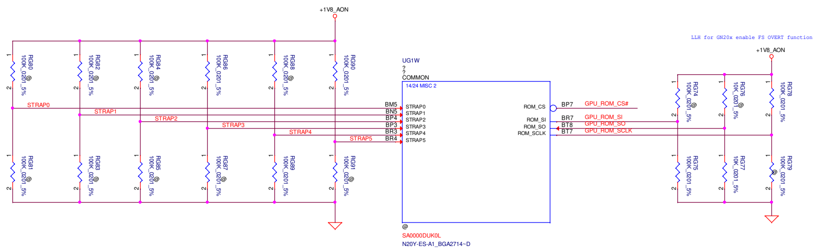
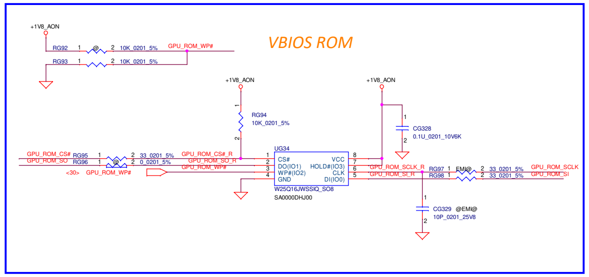
For Horizon15/17 MLK use DVT2_36

GN20-E3/E6	Samsung 8Gb 0x0(LLL) 14Gbps	VRAM_S8@ RG81 100K_0201_5%	VRAM_S8@ RG83 100K_0201_5%	VRAM_S8@ RG85 100K_0201_5%	
GN20-E3/E6	Micron 8Gb 0x1(HLL) 14Gbps	VRAM_M8@ RG80 100K_0201_5%	VRAM_M8@ RG83 100K_0201_5%	VRAM_M8@ RG85 100K_0201_5%	
GN20-E3/E6	Hynix 8Gb 0x2(LHL) 14Gbps	VRAM_H8@ RG81 100K_0201_5%	VRAM_H8@ RG82 100K_0201_5%	VRAM_H8@ RG85 100K_0201_5%	
GN20-E8	Samsung 16Gb 0x6(LHH) 16Gbps	VRAM_NS16@ RG81 100K_0201_5%	VRAM_NS16@ RG82 100K_0201_5%	VRAM_NS16@ RG84 100K_0201_5%	
GN20-E7	Samsung 16Gb 0x9(LML) 14Gbps	VRAM_S16@ RG81 100K_0201_5%	VRAM_S16@ RG82 100K_0201_5%	VRAM_S16@ RG83 100K_0201_5%	VRAM_S16@ RG85 100K_0201_5%





RVL-09964-001_v10

Table 1. GN20-E8 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V [1]	Samsung	K4ZAF325BM-HC16	M-die	0x6	16 Gbps	2137 [2]	Full	Production candidate	QS or later
				K4ZAF325BC-SC16	C-die	0xA	16 Gbps	N/A	Full	Post-production candidate	TBD

Notes:

[1] Refer to the *GN20-E8/E6 Refresh GeForce Product Specification* for memory voltages and clocks.

[2] Before the date code is available, the Samsung memory is screened for 12 Gbps @ 1.2V support. The Samsung memory is identified by the letters "SPL", which are inserted before the seven digits in its lot ID.

- GN20-E8 will be single sourced for the foreseeable future until further notice from NVIDIA.
- For GN20-E8, the maximum allowable memory case temperature is 95 °C.

Table 2. GN20-E7 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V [1]	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028 [2]	Full	Production ready	QS or later
				K4ZAF325BM-HC16	M-die	0x9	16 Gbps	N/A	N/A	Substitution allowed with waiver [3]	September 2021
				K4ZAF325BC-SC16	C-die	TBD	16 Gbps	N/A	Full	Post-production candidate	TBD
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V [1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 [2]	Full	Production ready	ES or later

Notes:

[1] Refer to the *GN20-E GeForce Product Specification* for memory voltages and clocks.

[2] Before the date code is available, the Samsung memory is screened for 11 Gbps @ 1.2V support. The Samsung memory is identified by the letters "SPL", which are inserted before the seven digits in its lot ID.

[3] Higher-speed grade memory devices can be used on GN20-E7 GPU designs in accordance with written waivers from the memory vendors. An acceptable waiver should indicate that the higher speed grade memory can be used as a substitute for lower-speed grade memory without any changes to spec parameters, including but not limited to timing, BIOS, and voltage.

- GN20-E7 will be single sourced for the foreseeable future until further notice from NVIDIA.
- For GN20-E7, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E6 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V [1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 [2]	Full	Production candidate	QS or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later
				H56G32CS4DX005	C-die	0x5	16 Gbps	2125	Full	Post-production candidate	TBD
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940	Full	Production candidate	QS or later

Notes:

[1] Refer to the *GN20-E8/E6 Refresh GeForce Product Specification* for memory voltages and clocks.

[2] Before the date code is available, the Samsung memory is screened for 12 Gbps @ 1.2V support. The Samsung memory is identified by the letters "SPL", which are inserted before the seven digits in its lot ID.

- For GN20-E6, the maximum allowable memory case temperature is 95 °C.

Table 5. GN20-E3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V [1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 [2]	Full	Production ready	QS or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production ready	QS or later
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 [3]	Full	Post-production ready	December 2020

Notes:

[1] Refer to the *GN20-E GeForce Product Specification* for memory voltages and clocks.

[2] Before the date code is available, the Samsung memory is screened for 11 Gbps @ 1.2V support. The Samsung memory is identified by the letters "SPL", which are inserted before the seven digits in its lot ID.

[3] Before the date code is available, the Micron memory is screened for 11 Gbps @ 1.2V support. The Micron memory will include the words "GDDR6 1.2V @ 11 Gbps" in the label.

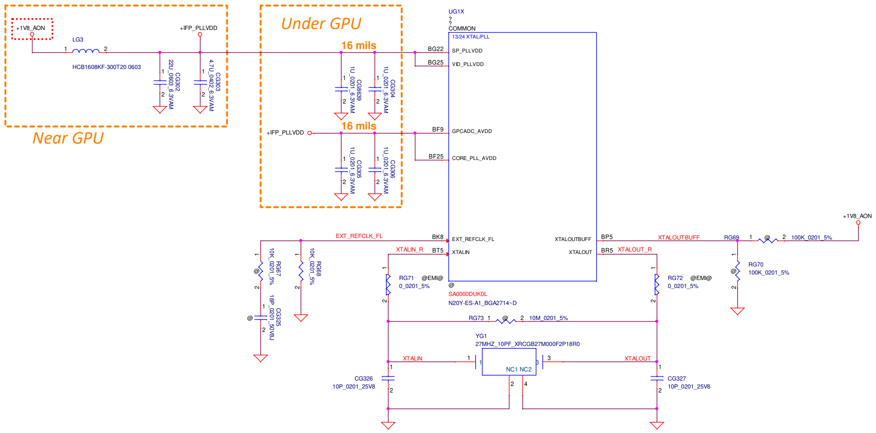
For GN20-E3, the maximum allowable memory case temperature is 95 °C.

Table 9.3 RAMCFG

Strap Pins (see Note) STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)

Table 9.3 RAMCFG

Strap Pins (see Note) STRAP2	STRAP1	STRAP0	RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

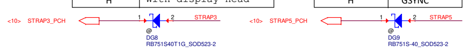


GPIO TABLE

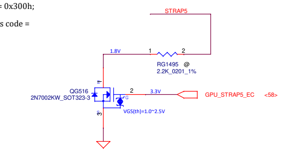
Strap to PCH

STRAP3_PCH	Discrete/MSHybrid
L	Without display head
H	With display head

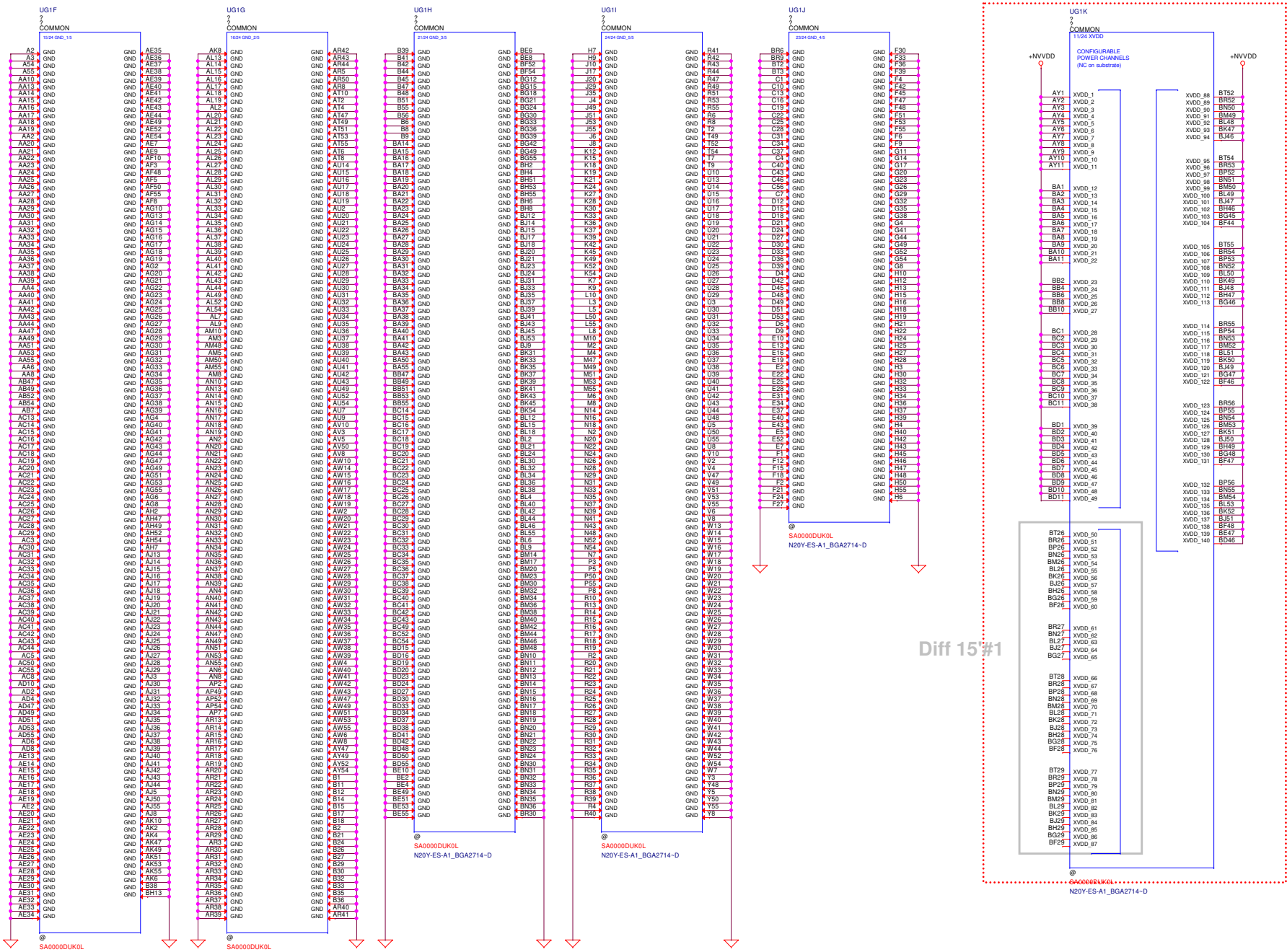
STRAP5_PCH	GPU DID
L	NON-GSYNC
H	GSYNC



GPU have display out then set to PCI class code = 0x300h; Discrete/MSHybrid with display head.
GPU didn't have any display out then set PCI class code = 0x302h. Pure Optimus W/O display head.



Follow NV reference SCH



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Title	NV(6/8) GND, RFUs		
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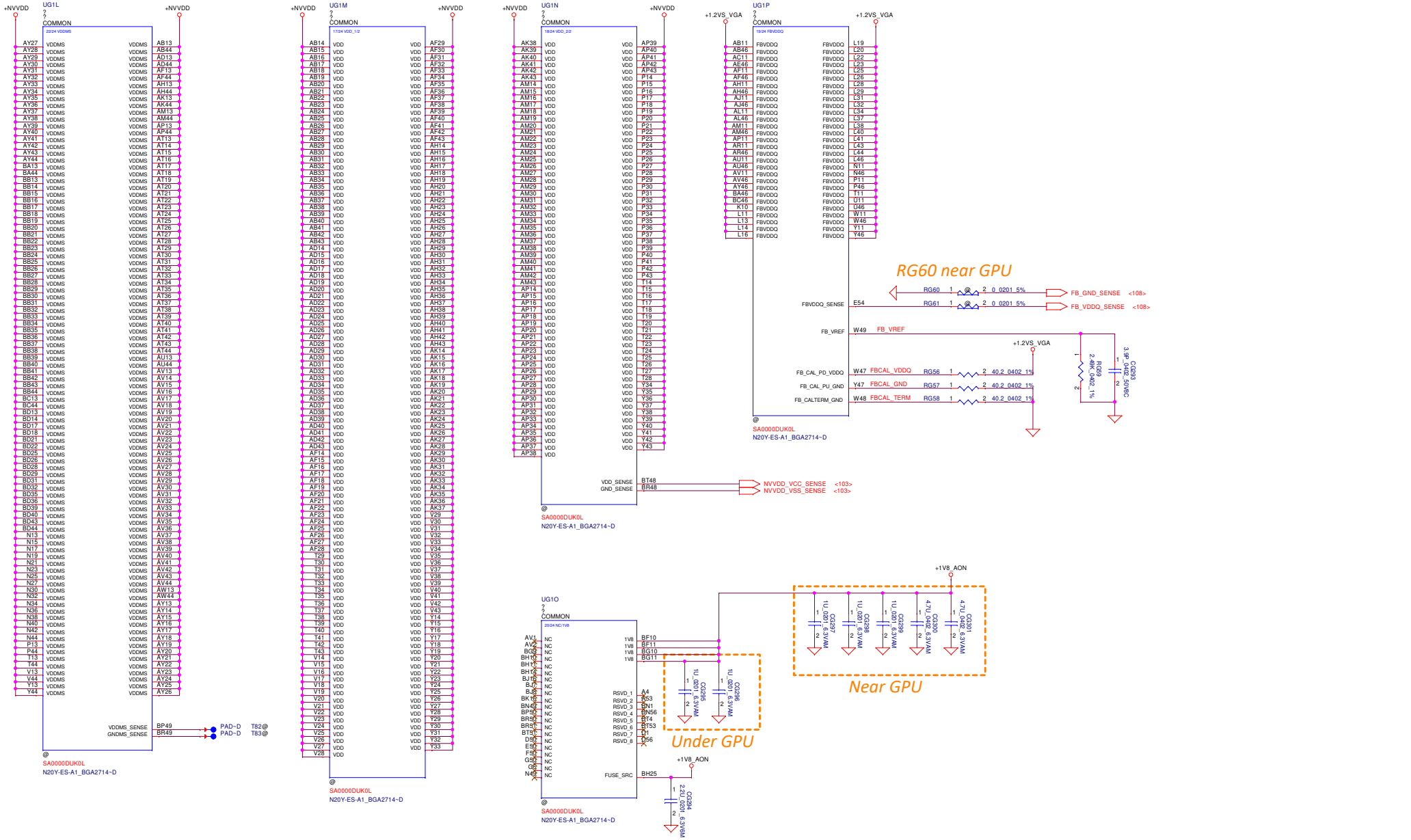

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	NV(7/8) POWERS
Size	Document Number: LA-L613P
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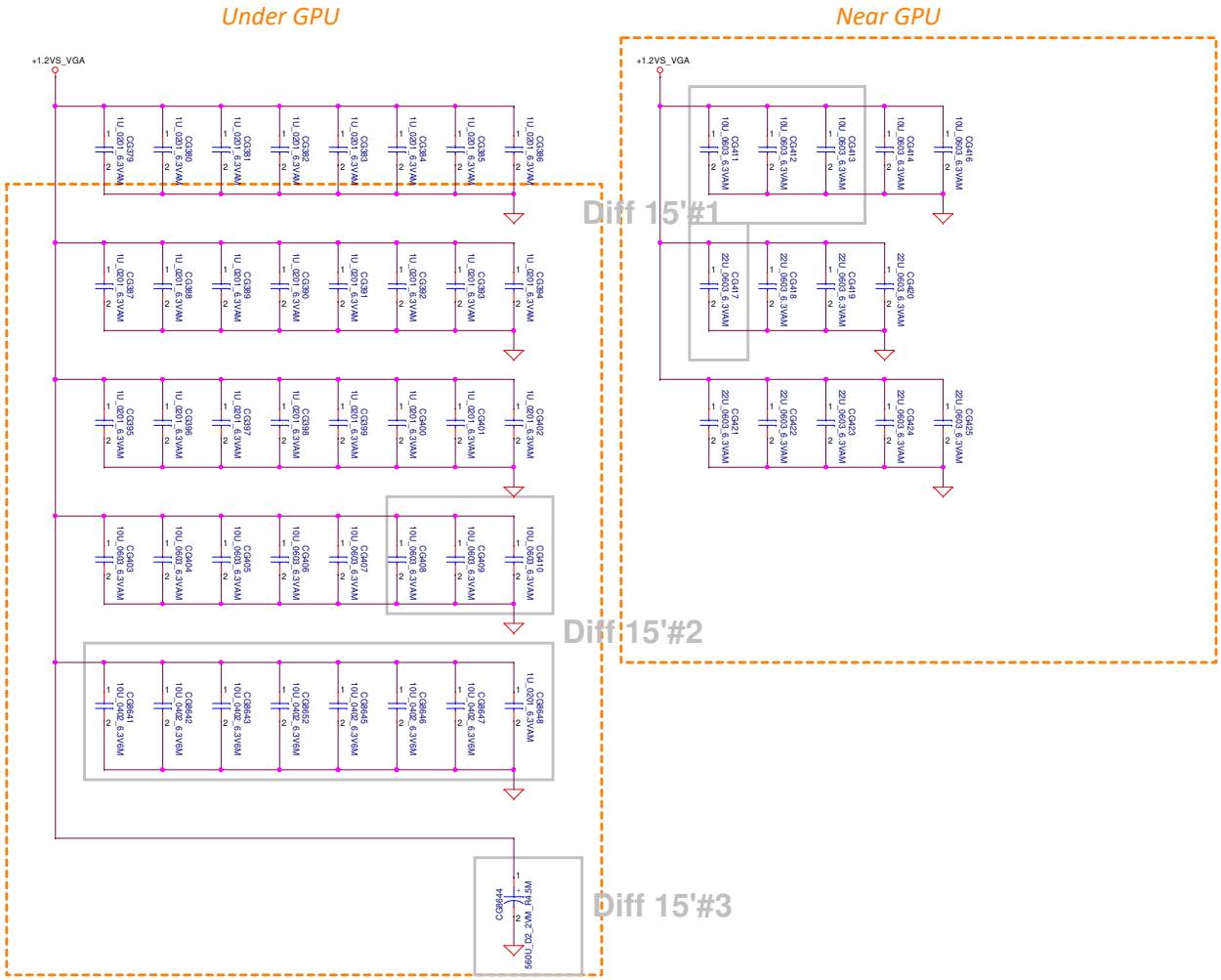
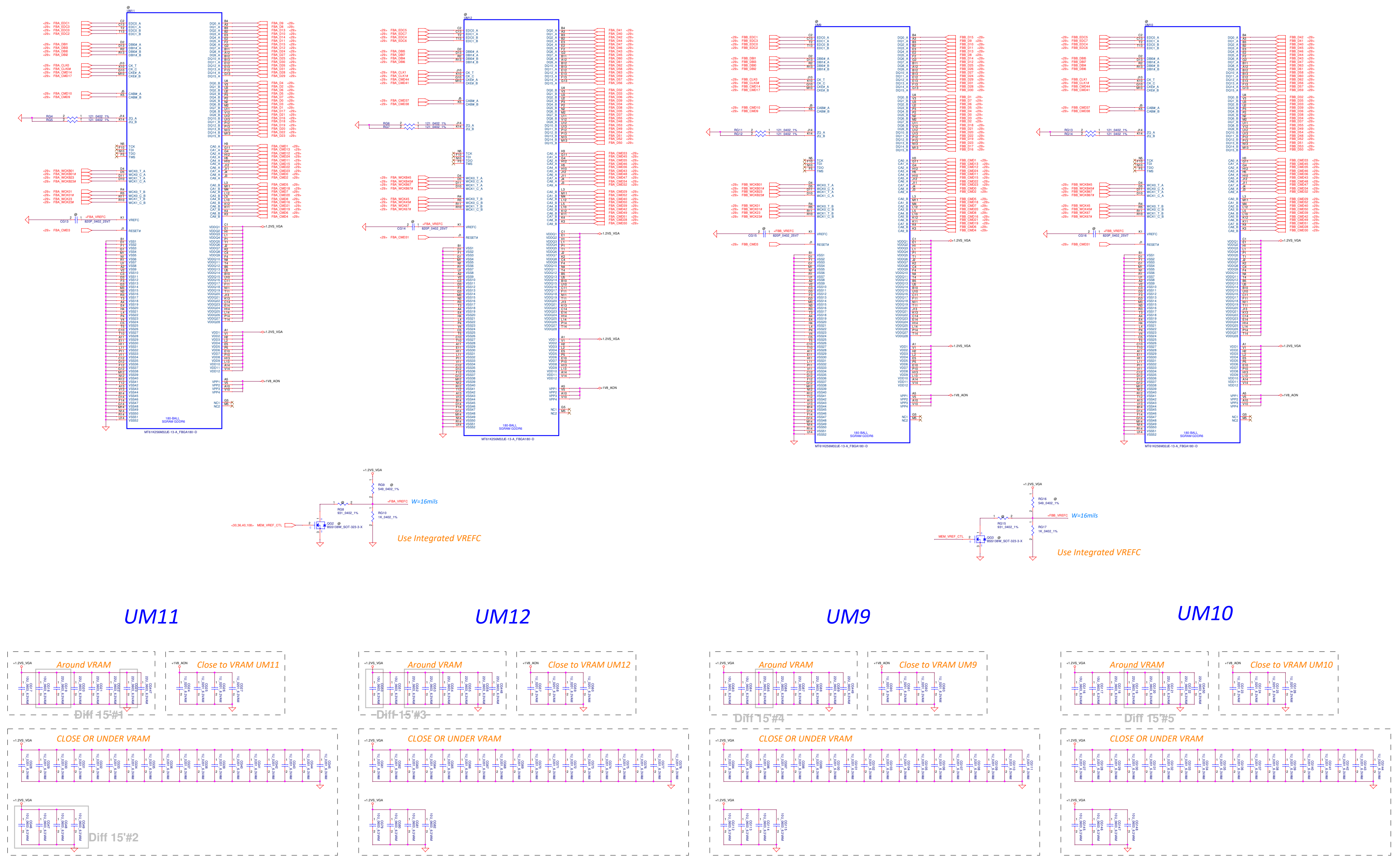
FBVDDQ_GPU

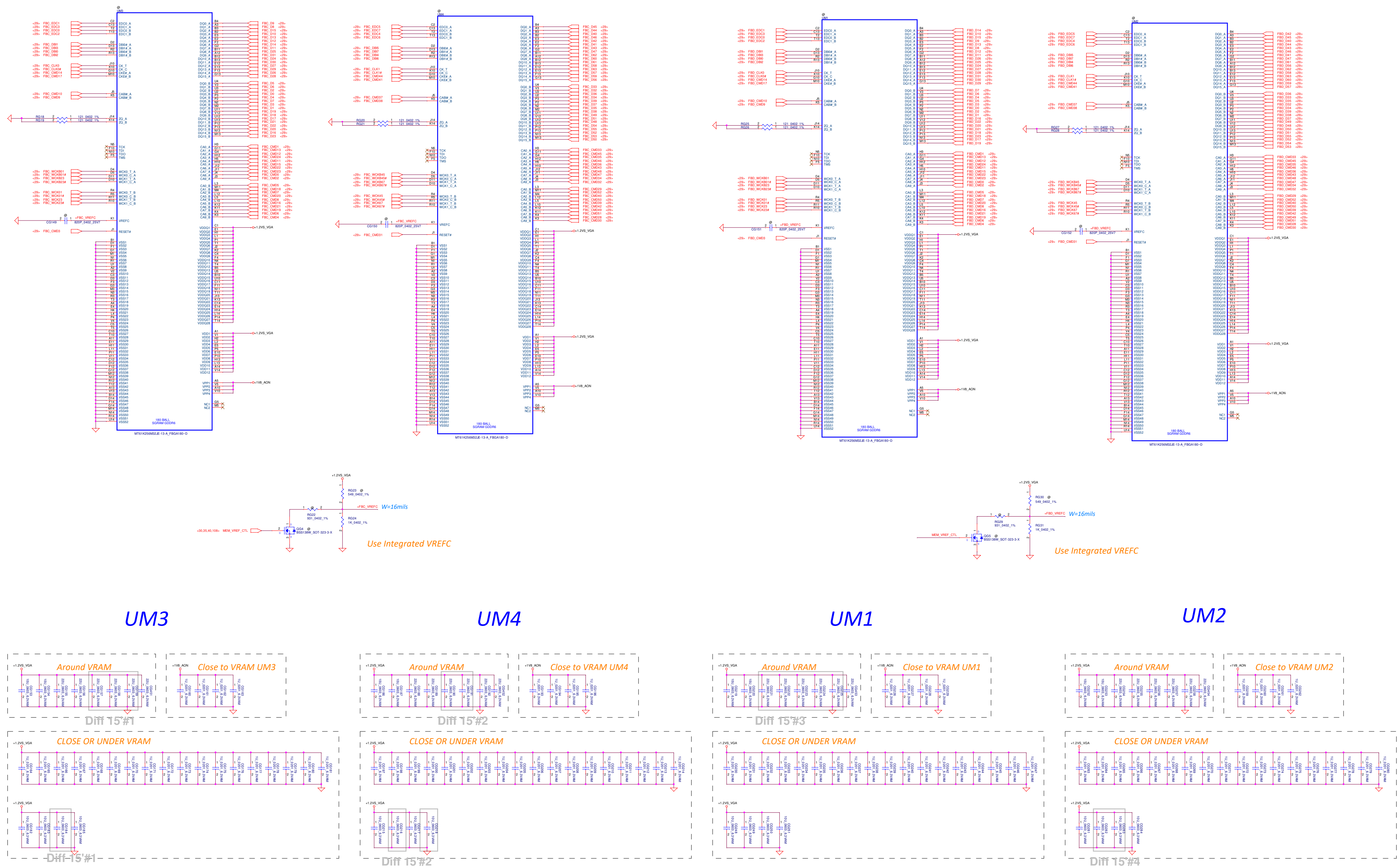


Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	NV(8/8) GPU DECOUPLING
Size	Document Number: LA-L613P
Rev	0.3
Date: Thursday, November 25, 2021	Sheet 34 of 121



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date	2022/12/31	Title: VRAM_GDDR6_AB
				Size / Document Number: LA-L613P / Rev 0.3
				Date: Thursday, November 25, 2021 / Sheet 35 of 121



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date	2022/12/31	Title: VRAM_GDDR6_CD
				Size / Document Number: LA-L613P / Rev 0.3
				Date: Thursday, November 25, 2021 / Sheet 36 of 121

ON-Semi	ONOVRM@ RG173 0_0402_1%	ONOVRM@ RG172 0_0402_1%	ONOVRM@ RG174 49.9_0402_1%	ONOVRM@ RG175 49.9_0402_1%	ONOVRM@ RG205 0_0402_1%	ONOVRM@ RG189 0_0402_1%	ONOVRM@ RG190 0_0402_1%	
	ONOVRM@ CG443 680P_0402_50V7K	ONOVRM@ CG444 0.47U_0402_50V6K						
uPI	UPIOVRM@ RG173 49.9_0402_1%	UPIOVRM@ RG172 49.9_0402_1%	UPIOVRM@ RG174 49.9_0402_1%	UPIOVRM@ RG175 49.9_0402_1%	UPIOVRM@ RG205 0_0402_1%	UPIOVRM@ RG189 49.9_0402_1%	UPIOVRM@ RG190 49.9_0402_1%	
	UPIOVRM@ CG443 0.1U_0402_50V7K	UPIOVRM@ CG444 0.1U_0402_50V7K	UPIOVRM@ CG436 0.1U_0402_50V7K	UPIOVRM@ CG437 0.1U_0402_50V7K				

EngR_13 X76 BOM config

8 mils

EngR_6

Unused SH_Ox Connect to SH_P2(PinS) or VCC(3V3)

follow NV& ON-semi)

Unused BSIN3/4 Connect to BS_IN1 or VCC (3V3) (default)

R value		Control	Address	Data
Raw1	5.9K ohm	0010	0000	01101001
	2.35K ohm	0010	0000	11000100
	1.85K ohm	0010	0000	11010001
Raw2	5.9K ohm	0010	0001	01101001
	2.35K ohm	0010	0001	11000100
	1.85K ohm	0010	0001	11010001

DVT_13

DVT_28

+1V8_AON / +1V8_MAIN(PLL)

NV_3V3(For Sequence)

1V8-->NV3V3-->NVVDD-->PEXVDD-->VPP-->FBVDD

Diff 15'#1

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	OC, Discharging		
Size	Document Number		Rev
	LA-L613P		0.3
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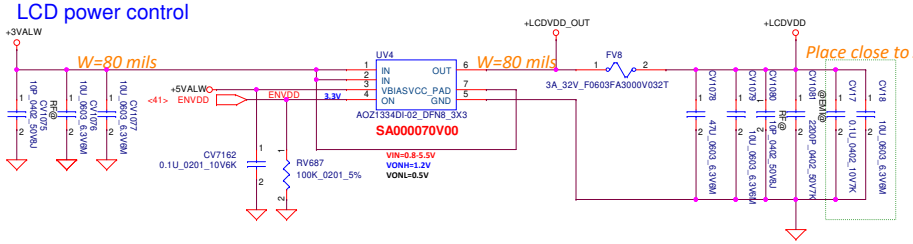
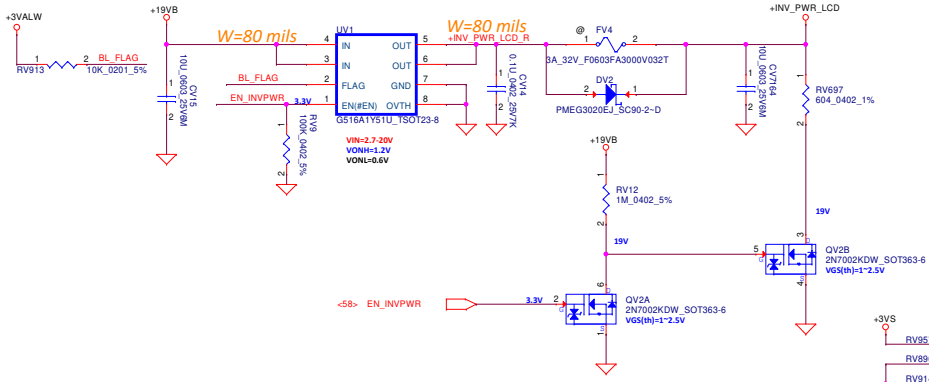
Main Func = LCD/CAM

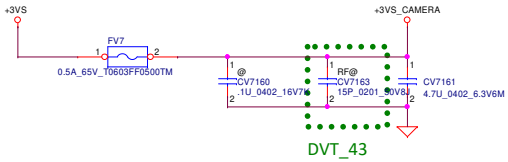
LCD power control



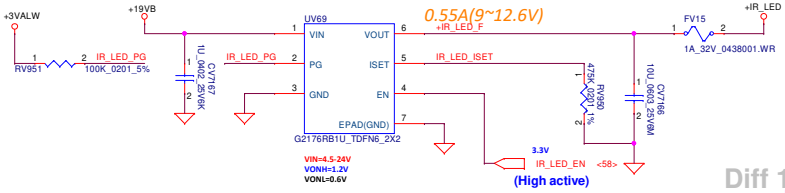
LCD backlight power control

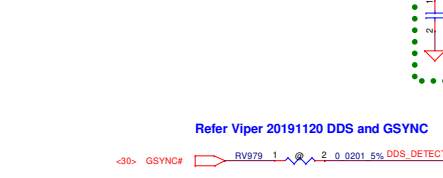


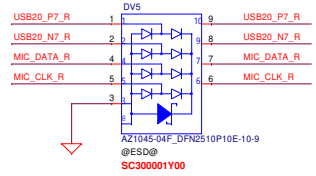
CAMERA POWER

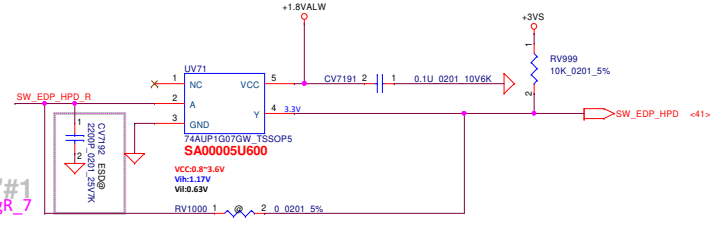


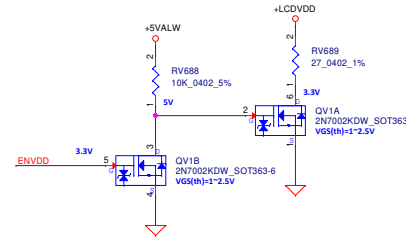
DVT_43

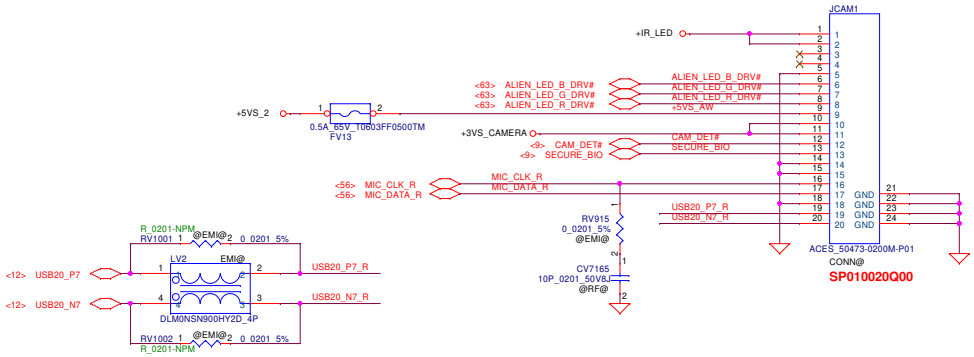


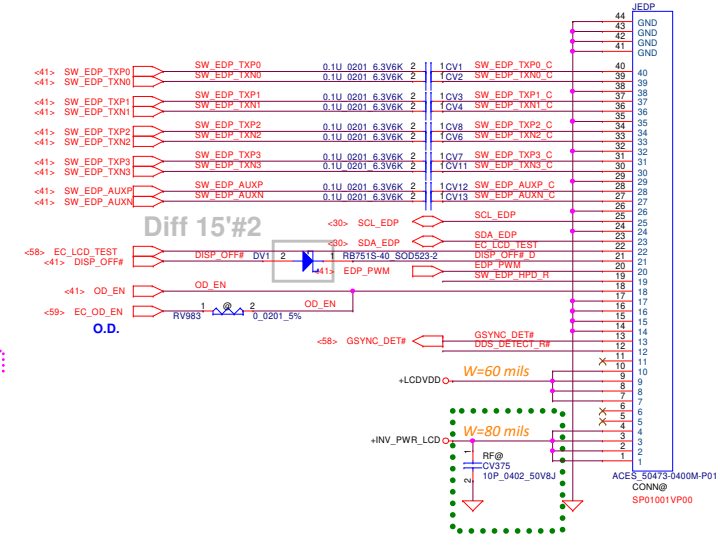












DVT_42

Refer Viper 20191120 DDS and GSYNC

<30> GSYNC#
RV979
0_0201_5%
DDS_DETECT_R#
DDS_DETECT_R#
<58>

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	eDP/Camera
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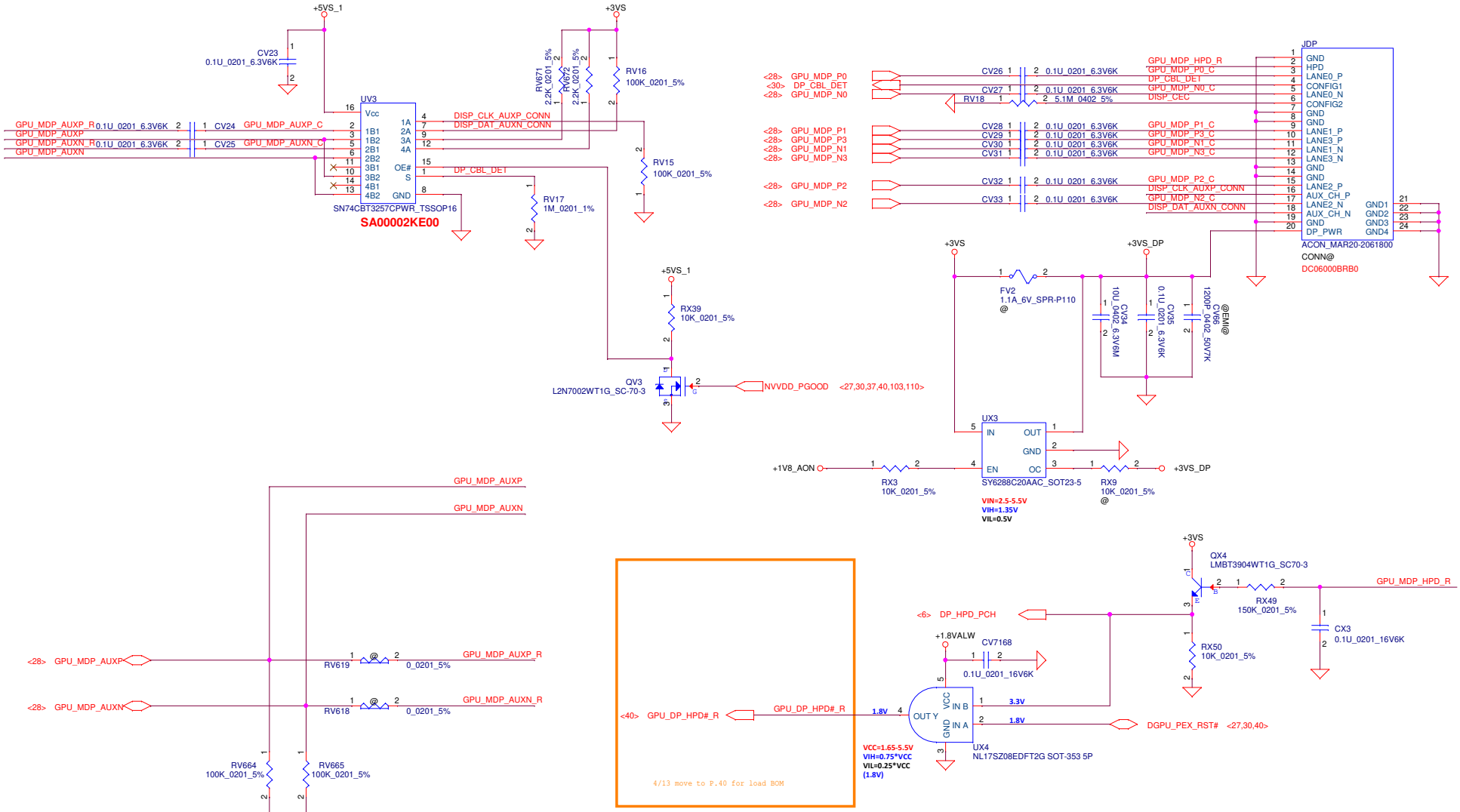
"17 ONLY"

Diff 15'#1



Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	Mini DP		
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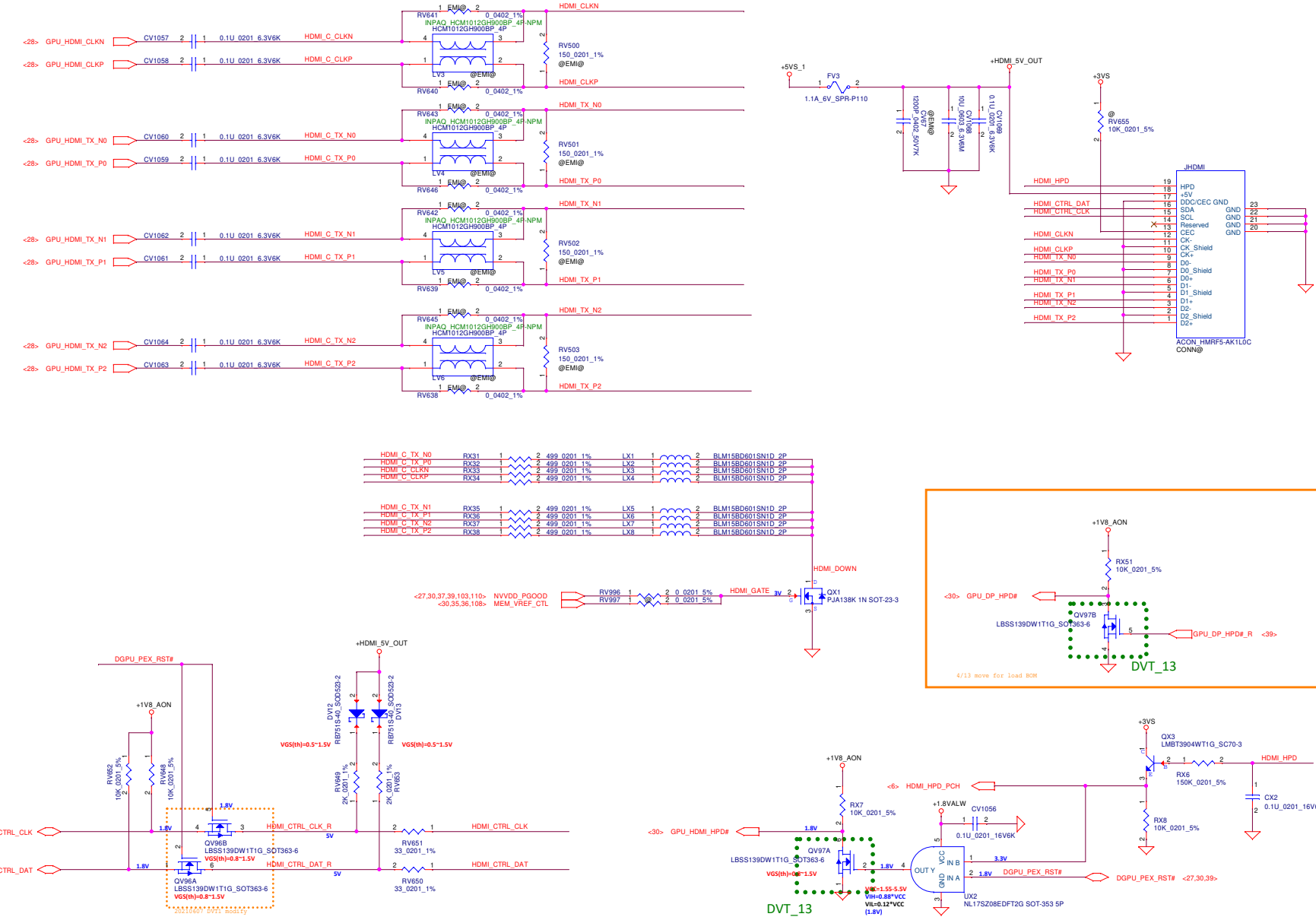

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	HDMI
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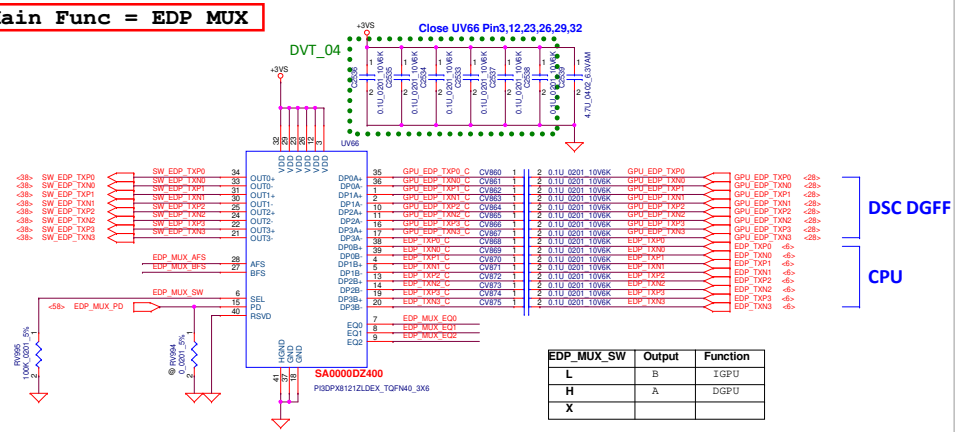
Main Func = EDP MUX

DVT_04

Close UV66 Pin3,12,23,26,29,32



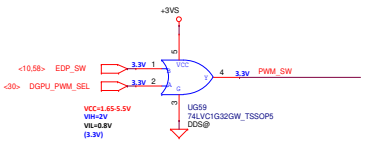
DSC DGFF

CPU

EDP_MUX_SW	Output	Function
L	B	IGPU
H	A	DGPU
X		

Diff 15'#1

SW	EDP_SW
0 (Default)	CPU
1	DGFF

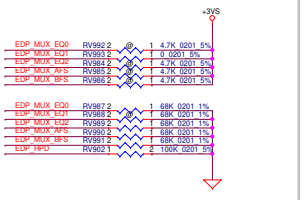


Input Equalization EQ at 10Gbps

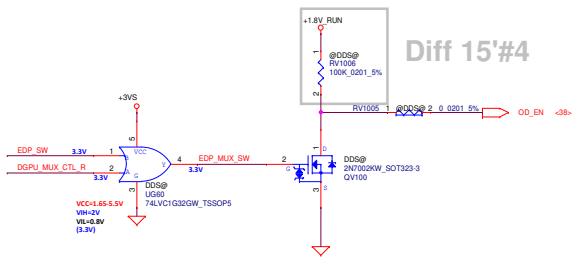
Port A Value	EQ0	EQ1	Port B Value	EQ2	EQ1
3.2dB	0	0/R	3.2dB	0	0/F
3.8dB	0	F/1	3.8dB	0	R/1
4.7dB	R	0/R	4.7dB	R	0/F
5.9dB	R	F/1	5.9dB	R	R/1
7.0dB	F	0/R	7.0dB	F	0/F
7.8dB	F	F/1	7.8dB	F	R/1
9.0dB	1	0/R	9.0dB	1	0/F
10.3dB	1	F/1	10.3dB	1	R/1

Flat Gain and Output Swing Linearity Selections:

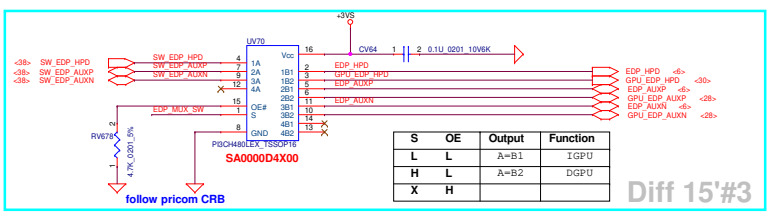
AFS or BFS	Flat Gain (dB)	Output Swing Linearity Range Selection (mVp-p)
0	-3.5	1000
R	-6.5	1000
F	-3.5	1200
1	-6.5	1200



Diff 15'#2



Diff 15'#4



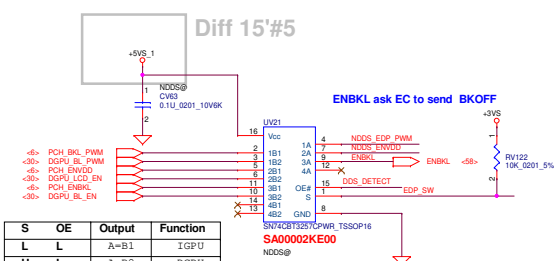
S	OE	Output	Function
L	L	A=B1	IGPU
H	L	A=B2	DGPU
X	H		

Diff 15'#3

NDDS : Mshybrid mode

DDS_Detect Control close UV21

Diff 15'#5



S	OE	Output	Function
L	L	A=B1	IGPU
H	L	A=B2	DGPU
X	H		

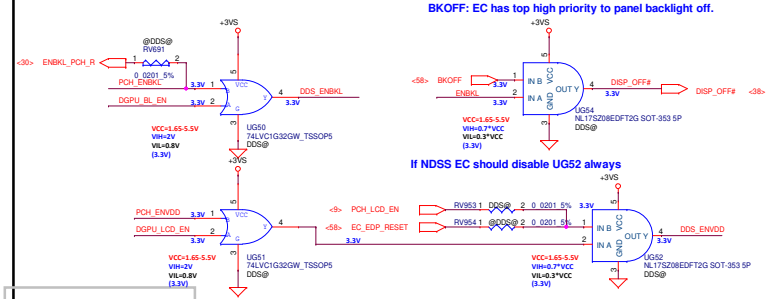
NDDS : Mshybrid mode

DDS_Detect Control close UV21

Main Func = DDS

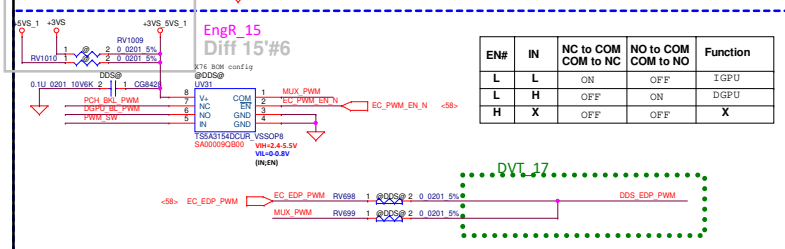
BKOFF: EC has top high priority to panel backlight off.

If NDSS EC should disable UG52 always



EngR_15

Diff 15'#6



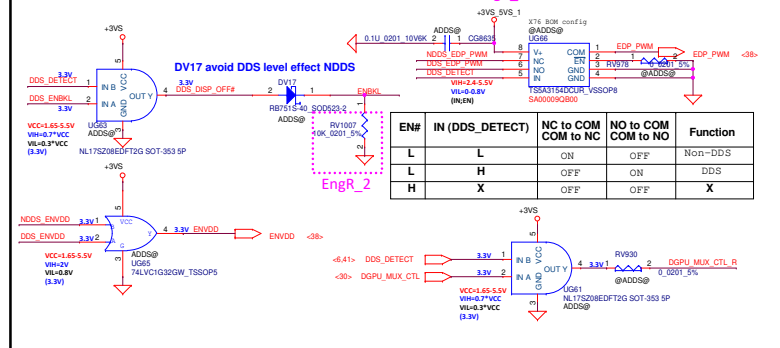
EN#	IN	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	IGPU
L	H	OFF	ON	DGPU
H	X	OFF	OFF	X

Main Func = DDS Auto Detect

EngR_15

DV17 avoid DDS level effect NDDS

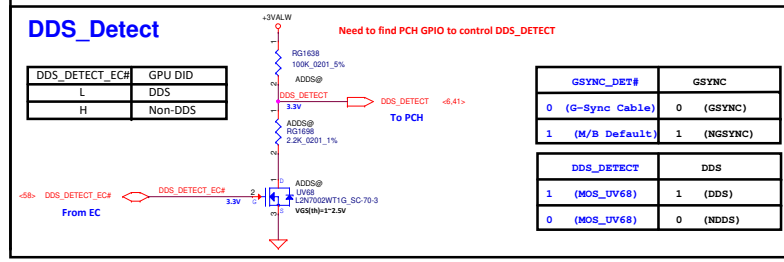
EngR_2



EN#	IN (DDS_DETECT)	NC to COM COM to NC	NO to COM COM to NO	Function
L	L	ON	OFF	Non-DDS
L	H	OFF	ON	DDS
H	X	OFF	OFF	X

DDS_Detect

Need to find PCH GPIO to control DDS_DETECT



DDS_DETECT_EC#	GPU DID
L	DDS
H	Non-DDS

GSYNC_DET#	GSYNC
0 (G-Sync Cable)	0 (GSYNC)
1 (M/B Default)	1 (NGSYNC)

DDS_DETECT	DDS
1 (MOS_UV68)	1 (DDS)
0 (MOS_UV68)	0 (NDDS)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDS/NDDS

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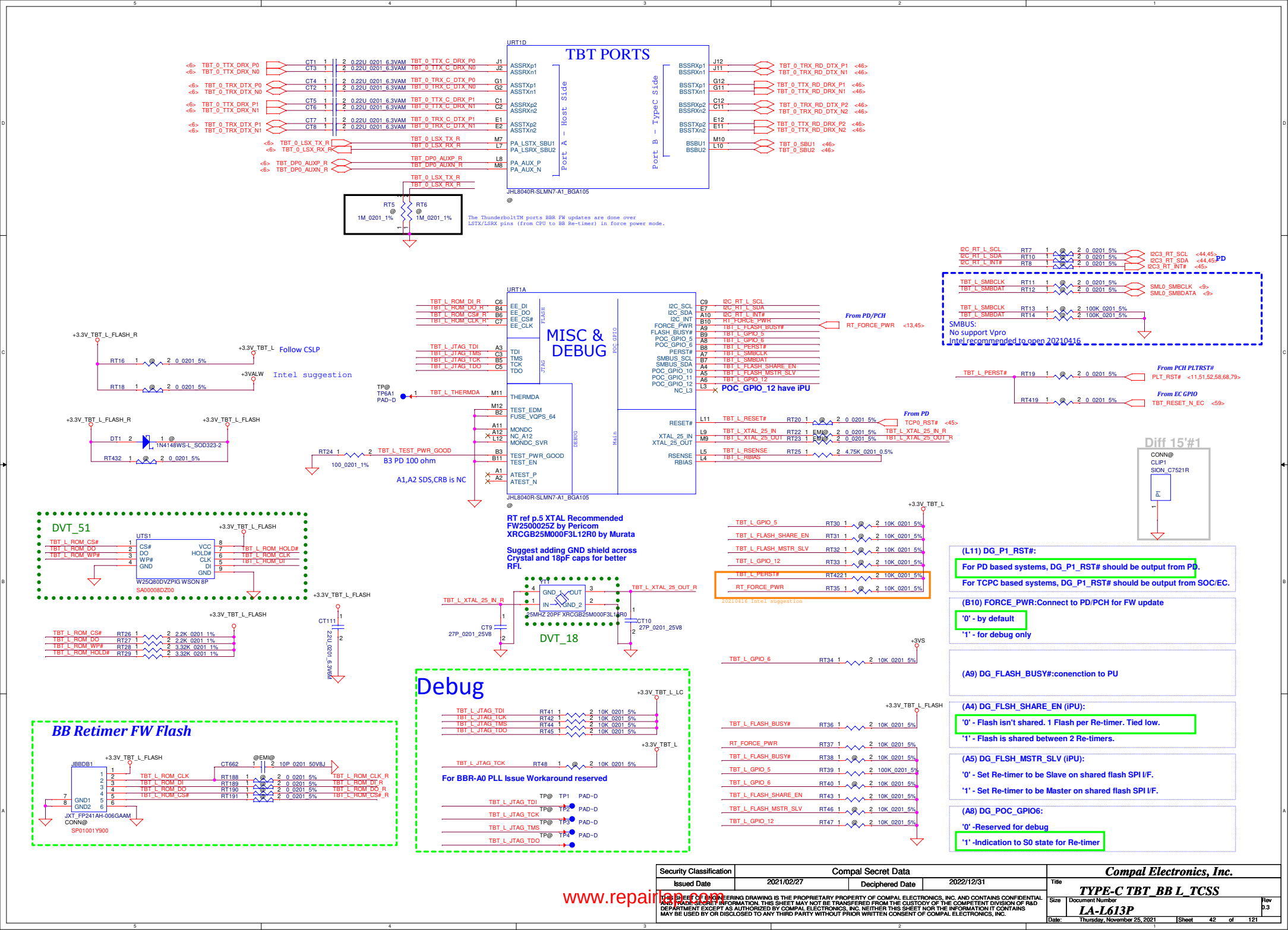

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	TYPE-C TBT_BB L_TCSS
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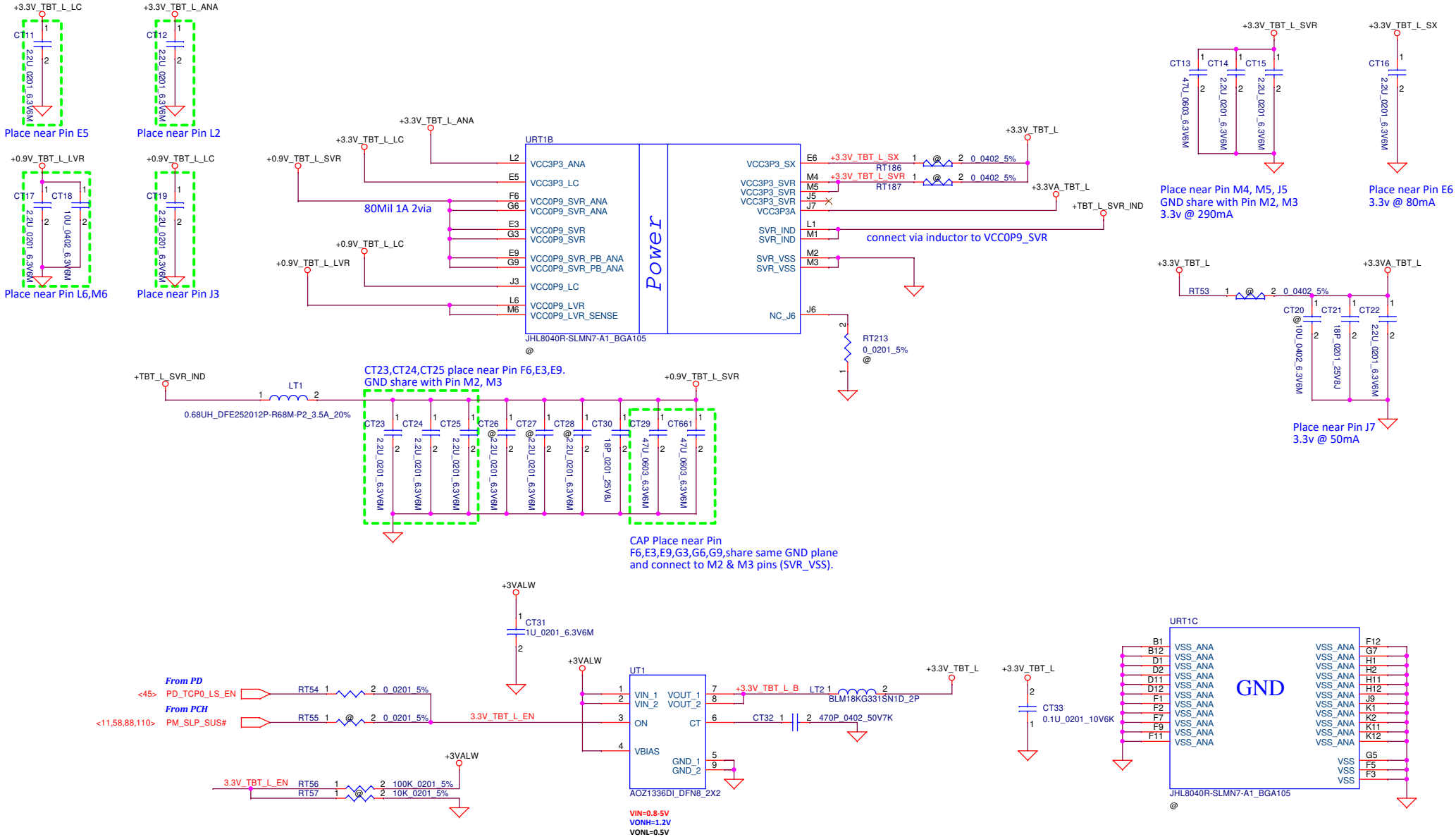

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	TYPE-C TBT_BB L_PWR,GND		
Size	Document Number		Rev
	LA-L613P		0.3
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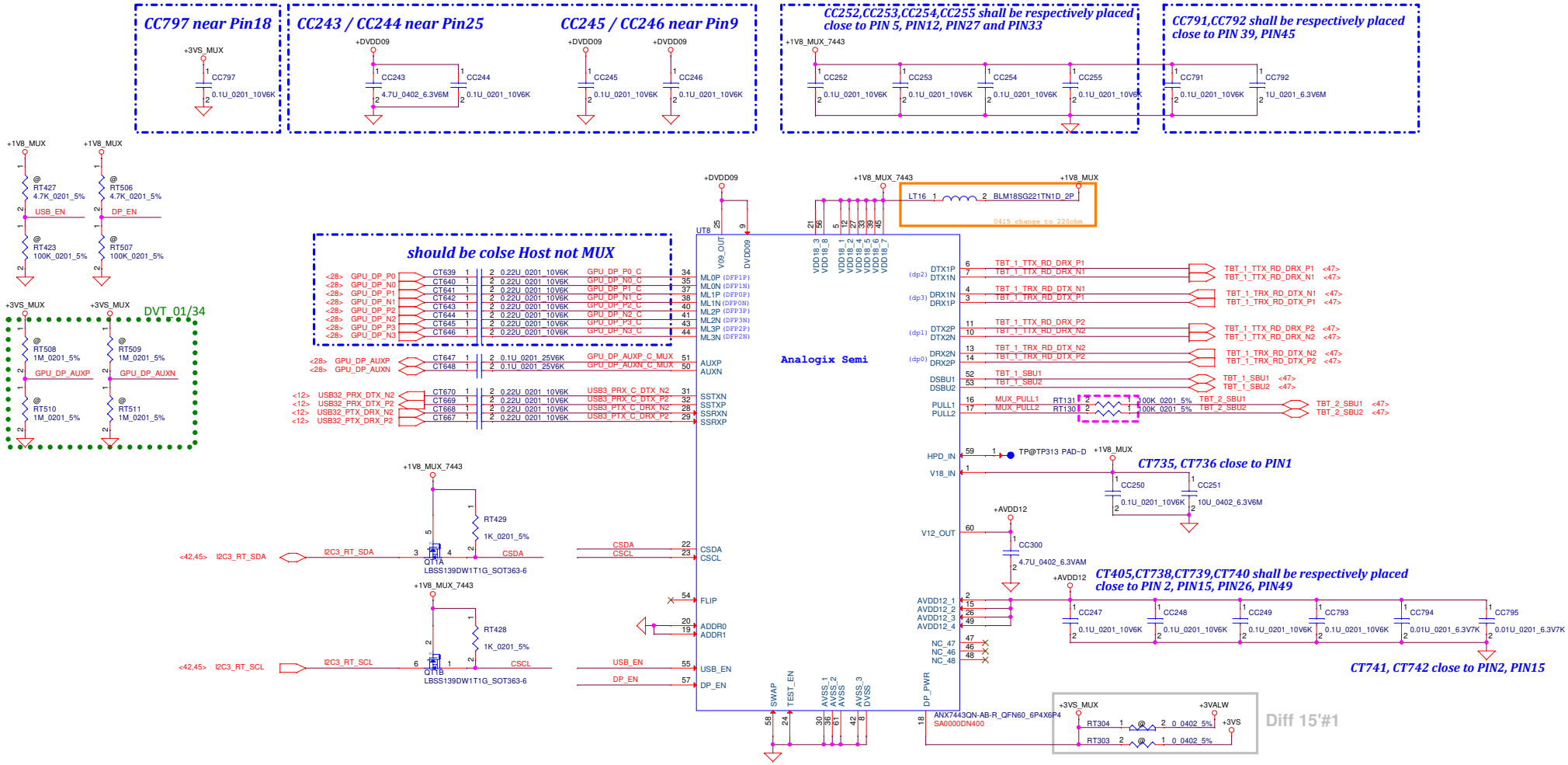

Table 6. Complete Function Table

SAI	SBI	SA0	SBO	OUTA0	OUTA1	OUTB0	OUTB1	FUNCTIONAL MODE	
0	0	0	0	INB	—	INA	—	Crosspoint, 1-channel 1:4 mux	
0	0	0	1	INB	—	—	INA	1-channel 1:4 mux	USB only on TBT_A_TOP_P/N
0	0	1	0	—	INB	INA	—	1-channel 1:4 mux	
0	0	1	1	—	INB	—	INA	1-channel 1:4 mux	USB on TBT_A_TOP_P/N; DDM on TBT_A_BOT_P/N
0	1	0	0	INB	—	INA	—		
0	1	0	1	INB	—	—	INA		
0	1	1	0	—	INB	INB	—		
0	1	1	1	—	INB	—	INB		
1	0	0	0	INA	—	INA	—	Fan-out 1:2 configuration	
1	0	0	1	INA	—	—	INA	Fan-out 1:2 configuration	
1	0	1	0	—	INA	INA	—	Fan-out 1:2 configuration	
1	0	1	1	—	INA	—	INA	Fan-out 1:2 configuration	
1	1	0	0	INA	—	INB	—	Crosspoint, 2-channel 1:2 mux, 1-channel 1:4 mux	
1	1	0	1	INA	—	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB only on TBT_A_BOT_P/N
1	1	1	0	—	INA	INB	—	2-channel 1:2 mux,1-channel 1:4 mux	
1	1	1	1	—	INA	—	INB	2-channel 1:2 mux,1-channel 1:4 mux	USB on TBT_A_BOT_P/N; DDM on TBT_A_TOP_P/N

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	DP/USB3 Re-timer PS8802		
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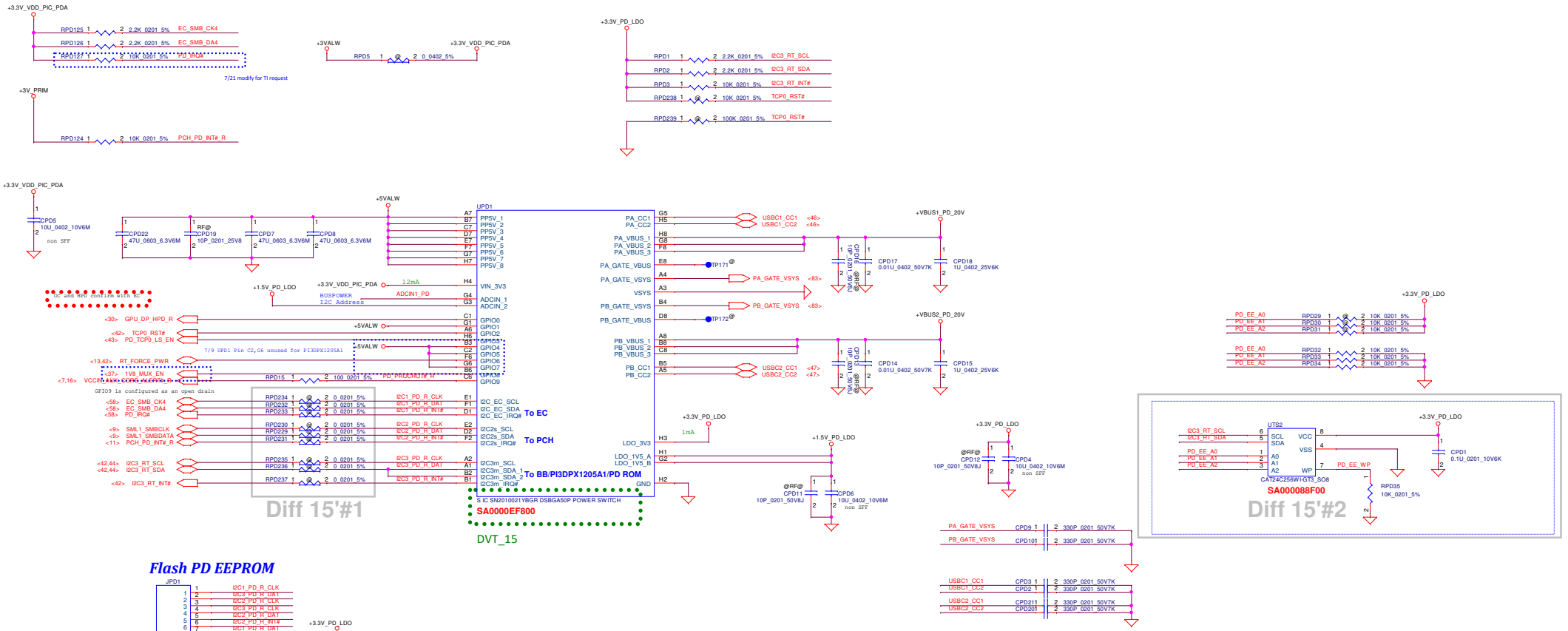

Table 2. Decoding of ADCIN1 and ADCIN2 Pins (continued)

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

Table 6. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	Port	Slave Address Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Available During BOOT
#1	A	0	1	0	0	0	0	0	R/W	Yes
#1	B	0	1	0	0	0	0	0	R/W	No
#2	A	0	1	0	0	0	0	1	R/W	Yes
#2	B	0	1	0	0	0	0	1	R/W	No
#3	A	0	1	0	0	0	1	0	R/W	Yes
#3	B	0	1	0	0	0	1	0	R/W	No
#4	A	0	1	0	0	0	1	1	R/W	Yes
#4	B	0	1	0	0	0	1	1	R/W	No

Table 7. Device Configuration using ADCIN1 and ADCIN2 .

ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address Index(2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A(3): The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A(3): The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	0	#1	SafeMode: The device does not enable he sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.
0	0	#2	
6	0	#3	
5	7	#4	

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Compal Electronics, Inc.			
Title	TYPE-C_PD_TPS65994		
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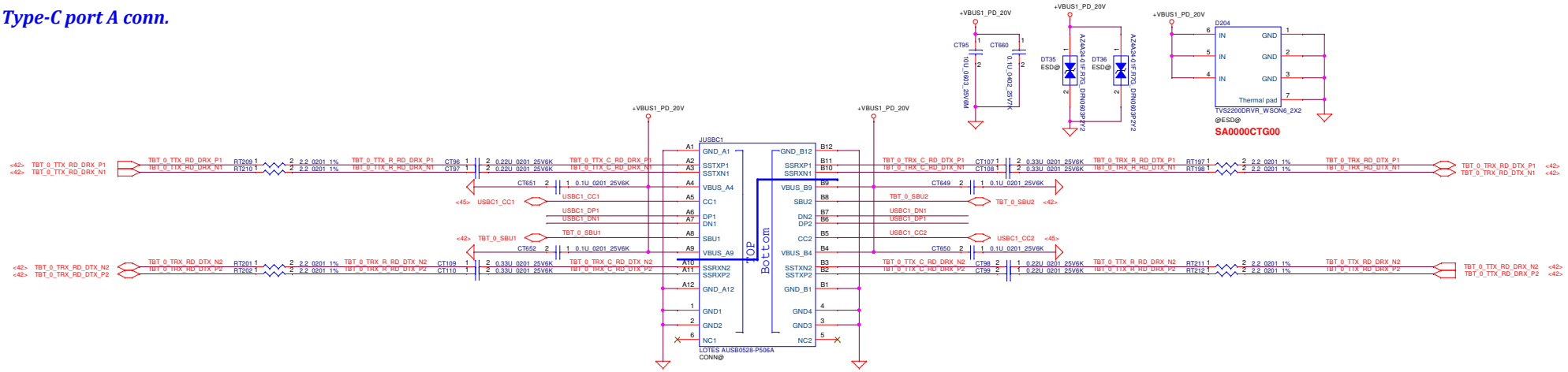
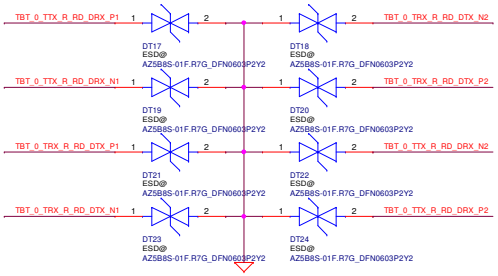
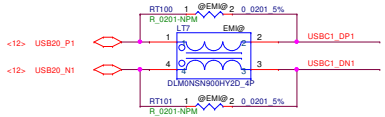
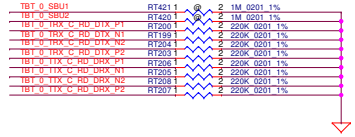
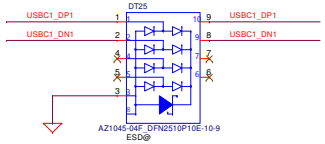
Type-C port A conn.

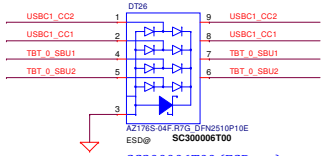




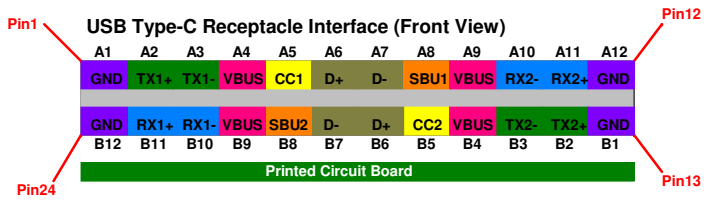








SC300006T00 (ESD use)
SC300002800 (symbol)



Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title: TYPE-C_PortA_CONN			
Size: Custom	Document Number: LA-L613P		Rev: 0.3
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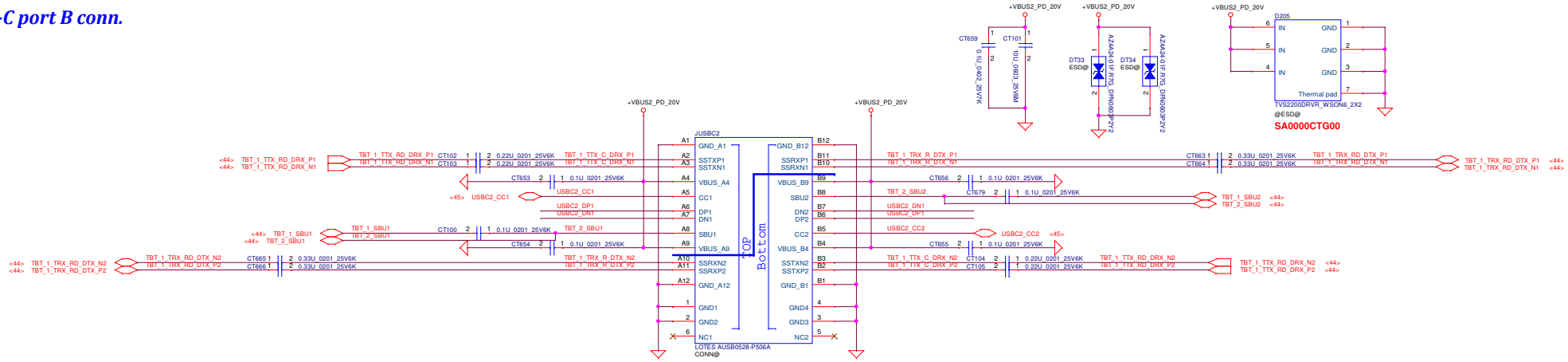
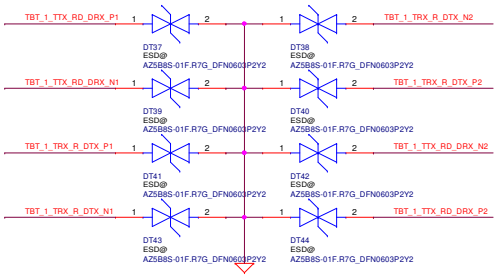
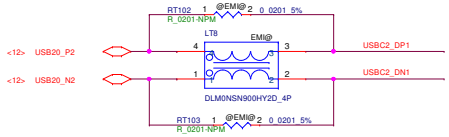
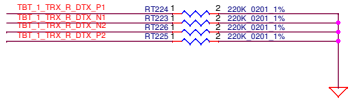
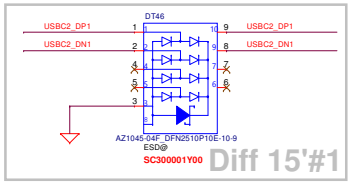
Type-C port B conn.

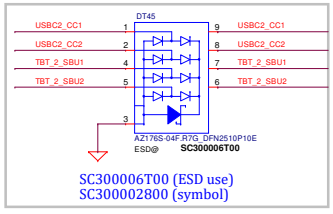


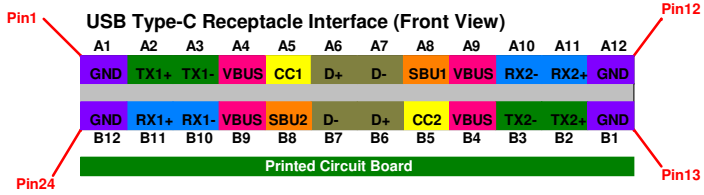












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Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	TYPE-C_PortB_CONN		
Size: Custom	Document Number: LA-L613P		Rev: 0.3
Date: Thursday, November 25, 2021	Sheet 47 of 121		

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: **Reserve**

Size	Document Number	Rev
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Date: Thursday, November 25, 2021 | Sheet 48 of 121

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: **Reserve**

Size | Document Number: **LA-L613P** | Rev: 0.3

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Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: ***Reserve***

Size | Document Number: ***LA-L613P*** | Rev: 0.3

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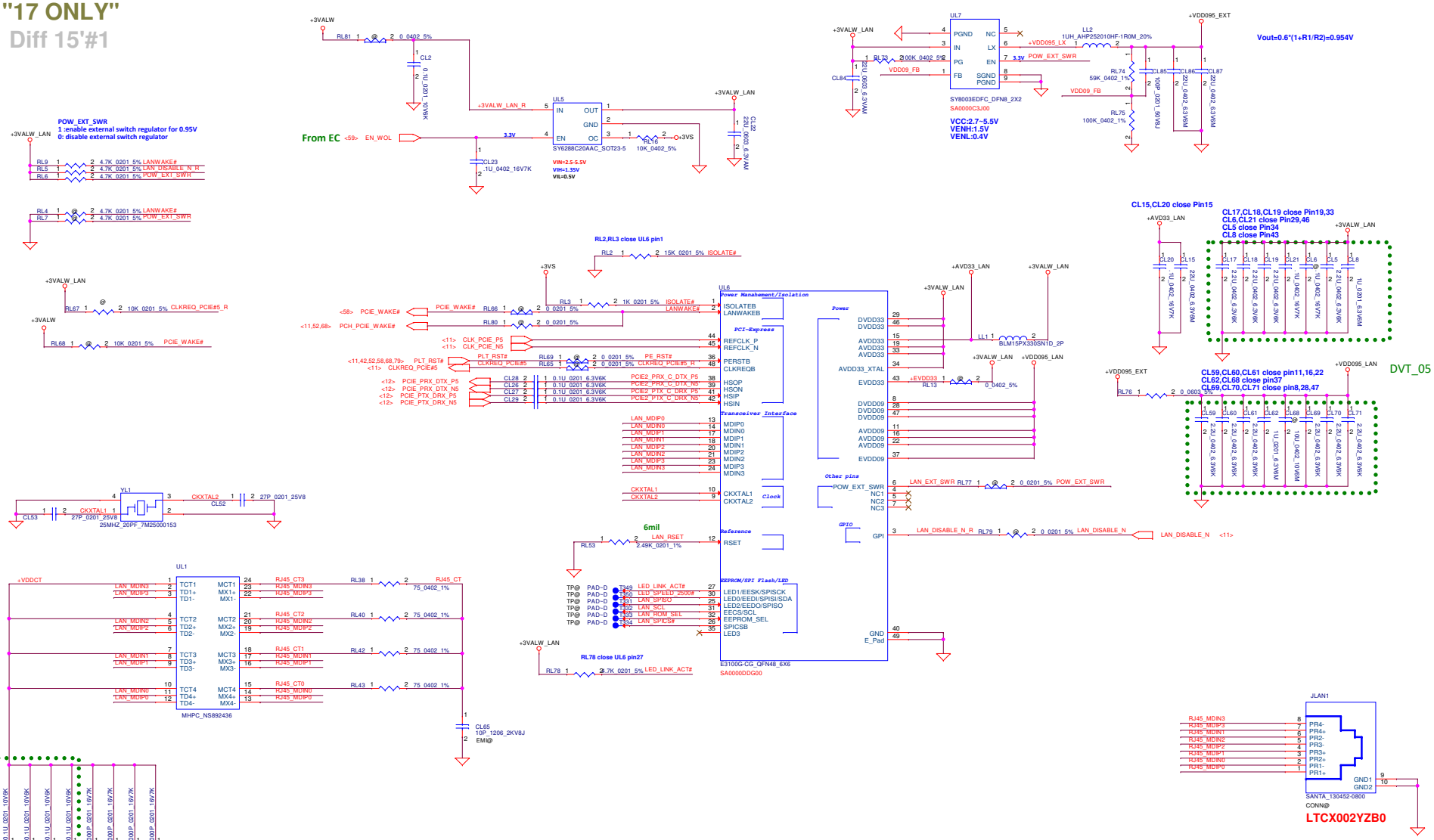
"17 ONLY"
Diff 15'#1

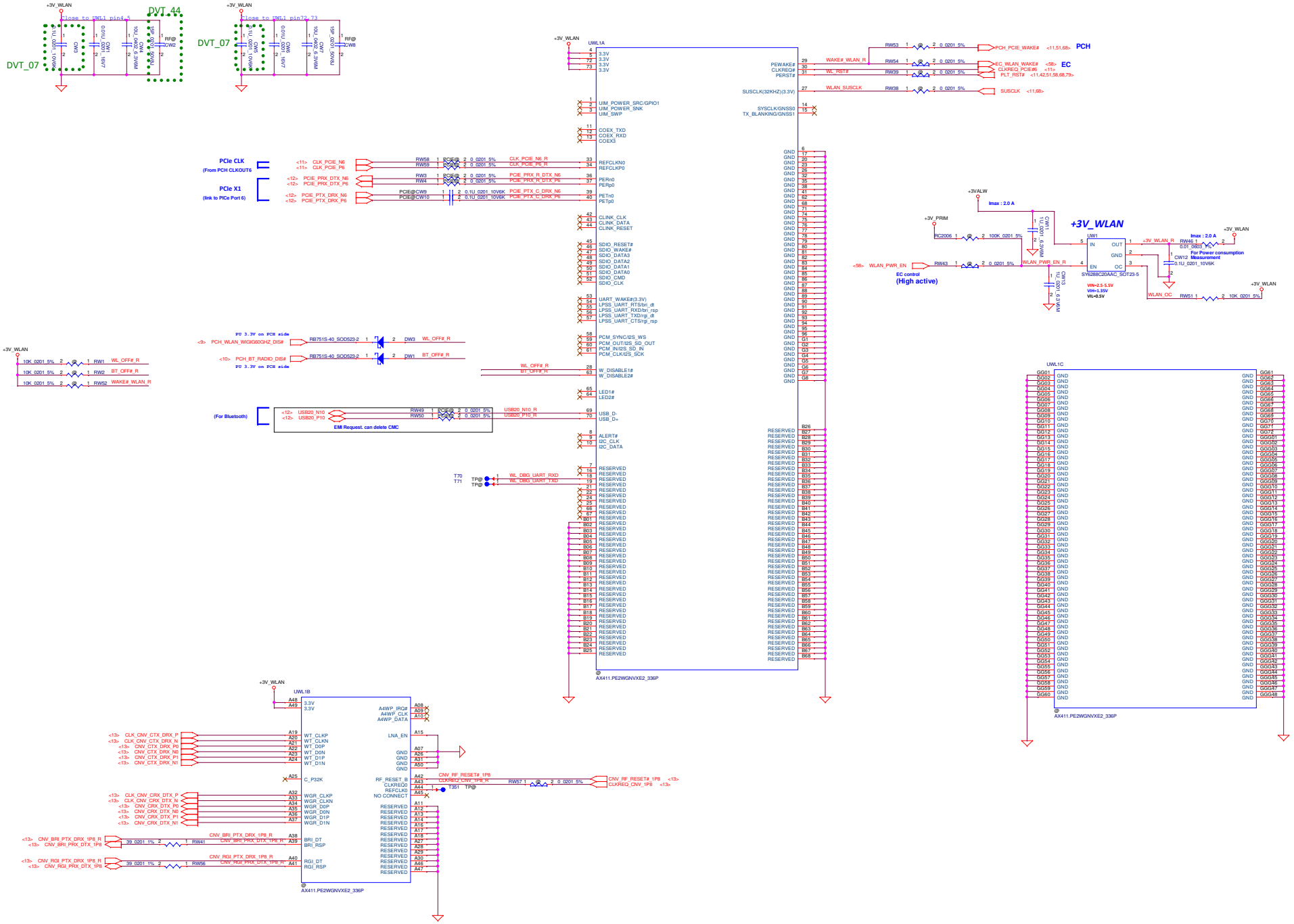


Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title: LAN E3100			
Size	Document Number: LA-L613P		Rev: 0.3
Date: Thursday, November 25, 2021	Sheet 51 of 121		

M.2 1625 SIP Module(PCIE+USB)

Diff 15'#1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2021/02/27	Deciphered Date 2022/12/31	Title: WLAN (non/ CNVi)(KEY E)
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			Date: Thursday, November 25, 2021 Sheet 82 of 121

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Compal Electronics, Inc.

Title		
Size	Document Number: LA-L613P	Rev: 0.3
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Compal Electronics, Inc.

Title

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Compal Electronics, Inc.

Title			
Size	Document Number		Rev
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Verb table configures as 1 JD mode with
internal 47K pull high to save external rBOM.

500mA

10mA

DVT2_37

Diff 15'#1

DVT_08

Diff 15'#2

Diff 15'#4

Diff 15'#3

EC Beep

MCU Beep

MODIFY BY COMPAL FOLLOW FC11 AMD solution.

DMIC 1.8V POWER

DMIC 3.3V POWER

To PCH

From Module

DATA OUTPUT

DATA INPUT

SA0000ANI00

SA00001NQ00

DVT_45

RF Request

moat

place at AGND and DGND plane

RA23 near codec IC
RA24 near JHP1

DVT2_26

0401 Change power source

Diff 15'#5

www.repairlap.com

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Codec ALC3281

LA-L613P

Rev 0.3

Thursday, November 25, 2021

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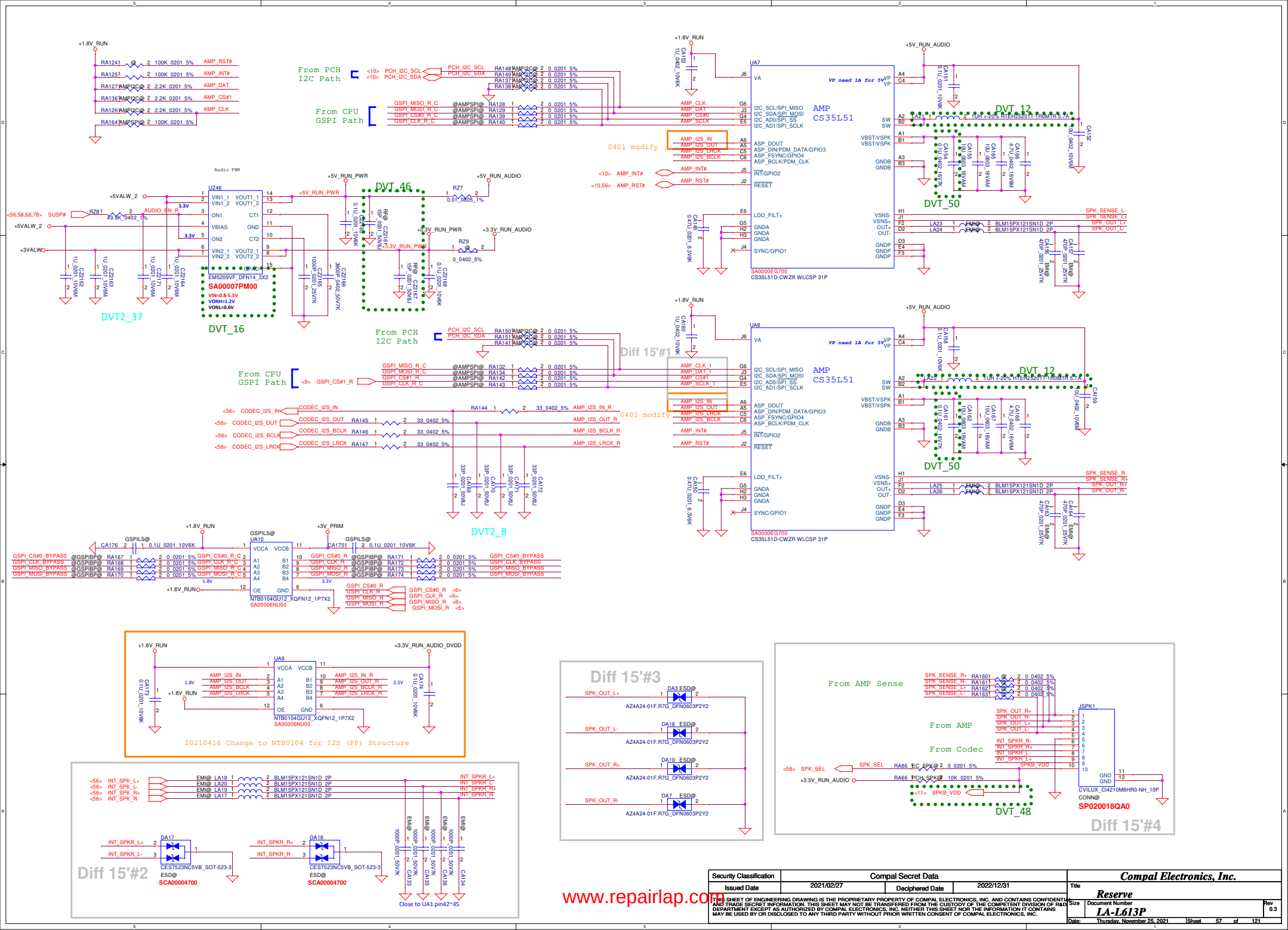

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	Reserve
Size	Document Number: LA-L613P
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DVT_53

DVT_14

+3.3V_PWRSRC_EC

CE171 Close to UE5

Ra

Rb

```
00.SD028000080 0_0402_5%
01.SD034120280 12K_0402_1%
02.SD034150280 15K_0402_1%
03.SD028200280 20K_0402_5%
04.SD034270280 27K_0402_1%
05.SD034330280 33K_0402_1%
H17 DVT1 06.SD034430280 43K_0402_1%
07.SD034560280 56K_0402_1%
08.SD034750280 75K_0402_1%
H17 DVT2 09.SD034100380 100K_0402_1%
10.SD034130380 130K_0402_1%
11.SD034160380 160K_0402_1%
-----------------------------------------
12.SD034200380 200K_0402_1%
13.SD000001B80 240K_0402_1%
H17 PLOT 14.SD00000G280 270K_0402_1%
15.SD034330380 330K_0402_1%
16.SD028430380 430K_0402_5%
17.SD034560380 560K_0402_1%
18.SD000000AL80 750K_0402_1%
19.SD000010U00 1.2M_0402_1%
```

Board ID table

NV GN20	PCB Revision
2	EVT-1
6	DVT-1
10	DVT-2
14	Pilot
16	Reserve

close EC k13 PIN

Diff 15'#1

EngR_12

DVT2_11

Reserve for abnormal shutdown

Diff 15'#2

DVT_21

Test point only

close EC G4 PIN

should PD in power. need check

Power ON circuit
Place on BOT

W=20 mils

Use SHI0000N600 footprint (MURAT_LQM18PN180MFHD_2P)

EC debug

BIOS debug

(KSO3)

flash EC code

(KSI4 KSI5 KSI6 KSI7)

SP010026E00

Security Classification	Compal Secret Data	
Issued Date	2021/02/27	Deciphered Date 2022/12/31

Compal Electronics, Inc.

Title: EC ENE-KB9542 QFN

Size: | Document Number: LA-L613P | Rev: 0.3

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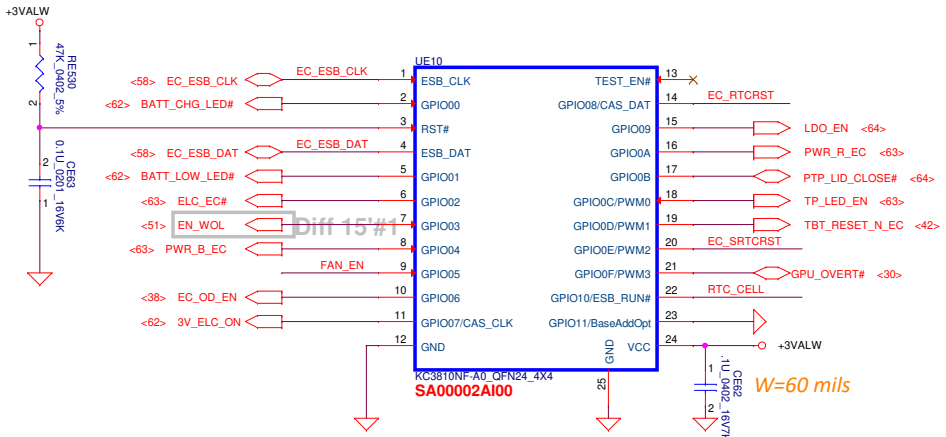
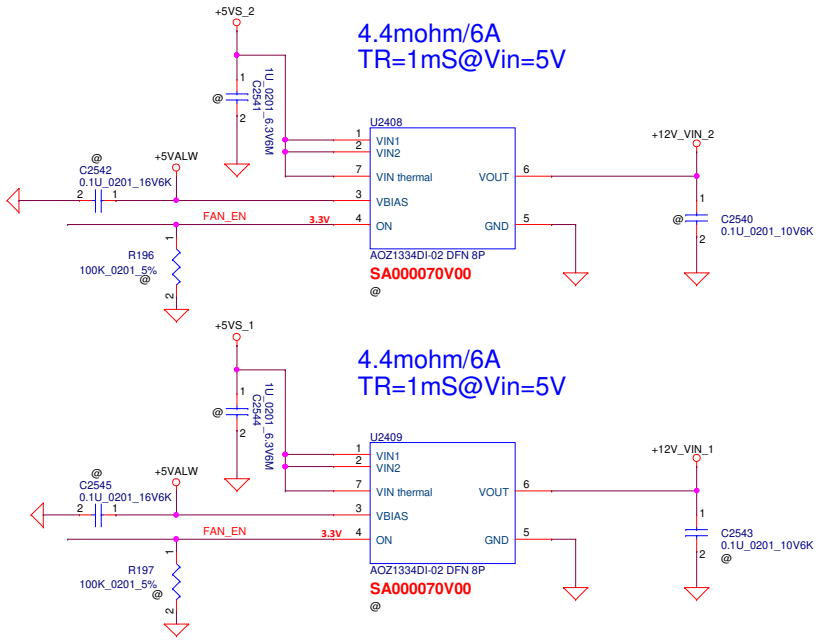
Main Func = EC ENE-KC3810

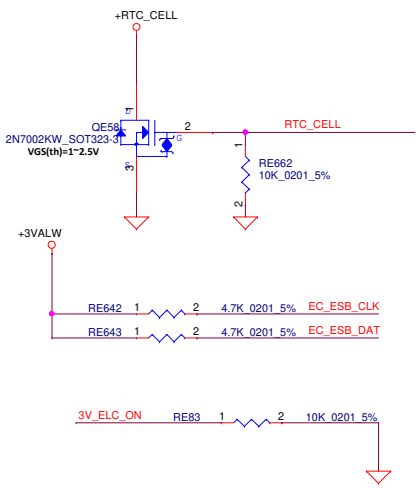


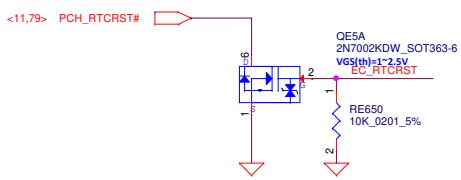
Main Func = FAN_EN(Reserve only)

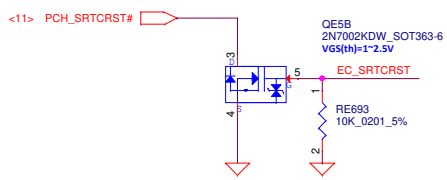
"17 ONLY"

Diff 15'#2









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Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: EC ENE-KB9022/S5 LID

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Compal Electronics, Inc.

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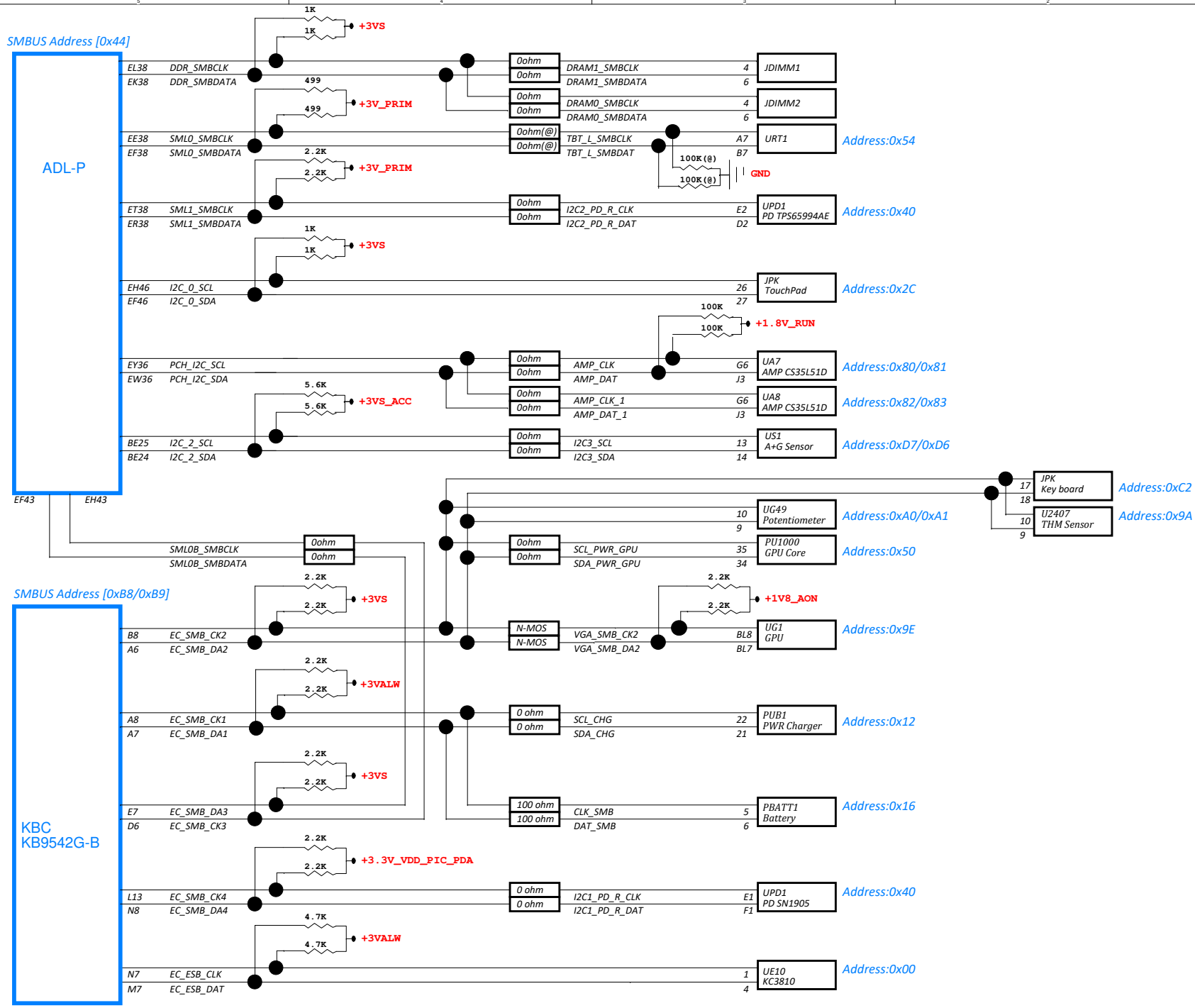

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
	LA-L613P	0.3

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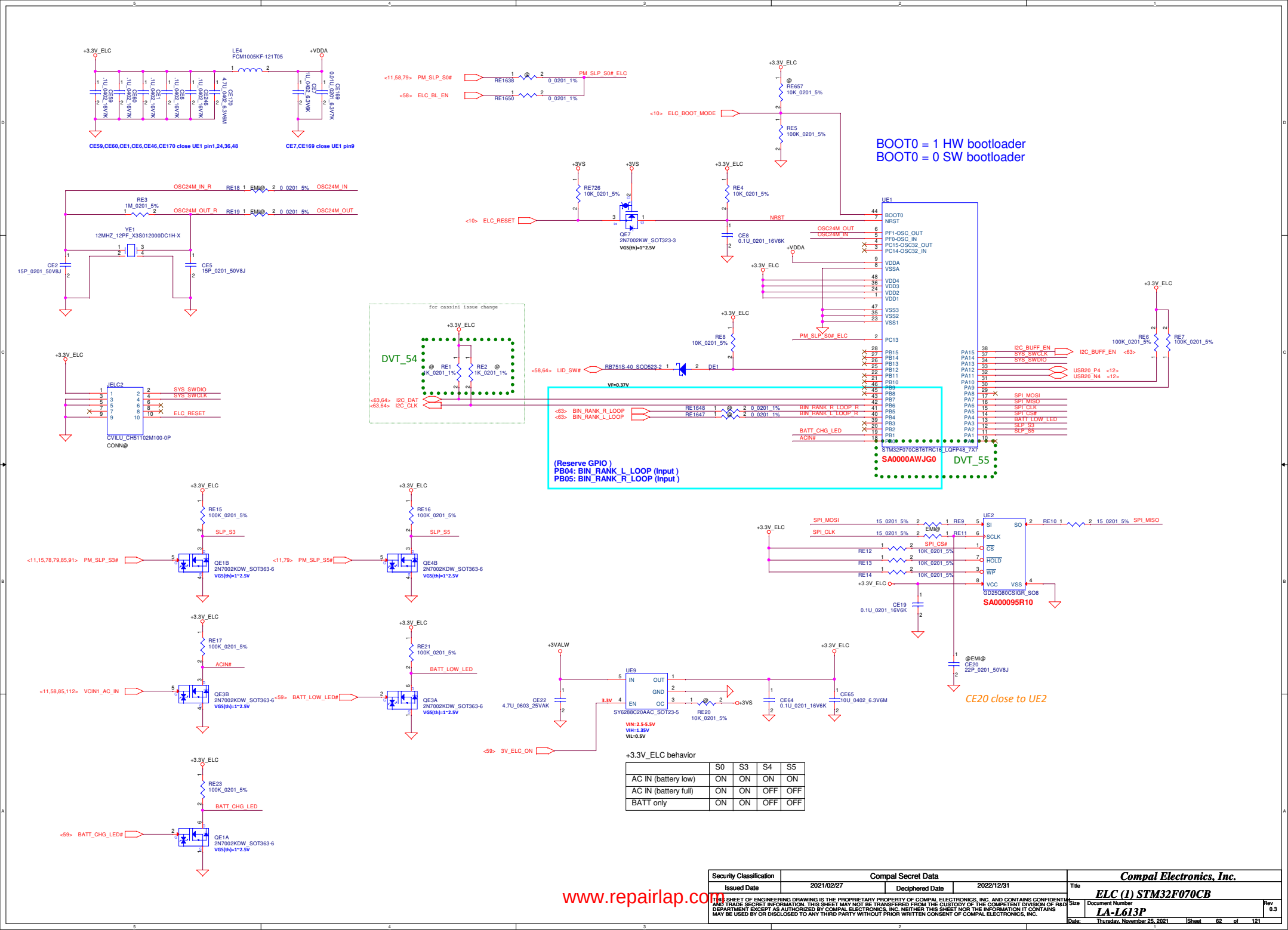

+3.3V_ELC behavior

	S0	S3	S4	S5
AC IN (battery low)	ON	ON	ON	ON
AC IN (battery full)	ON	ON	OFF	OFF
BATT only	ON	ON	OFF	OFF

Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.			
Title	ELC (1) STM32F070CB		
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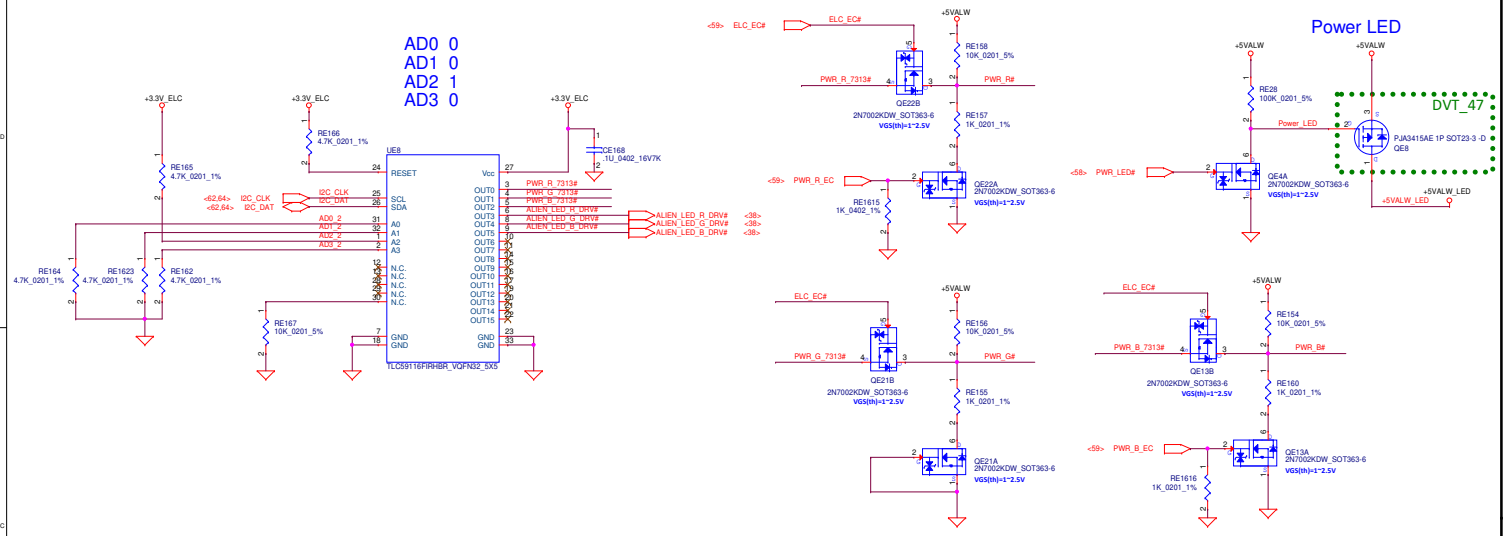
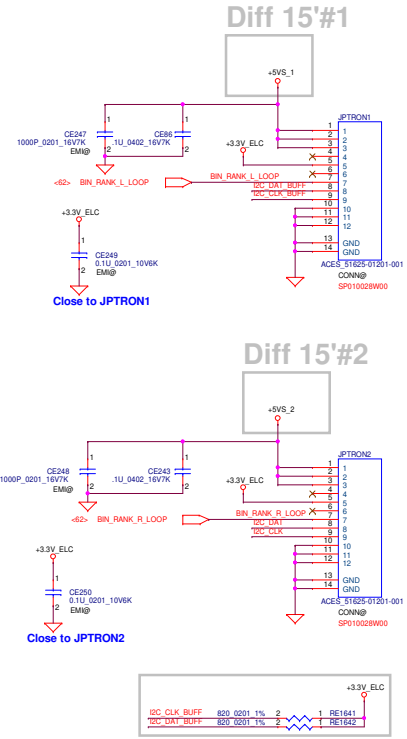
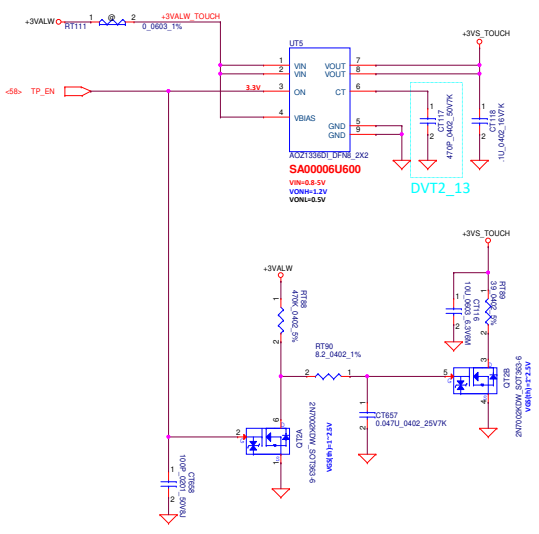
Main Func = ELC



Main Func = ON/OFF LOOP

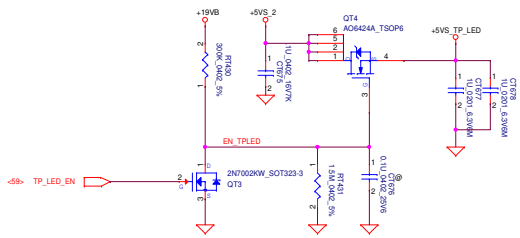


Main Func = Touch pad

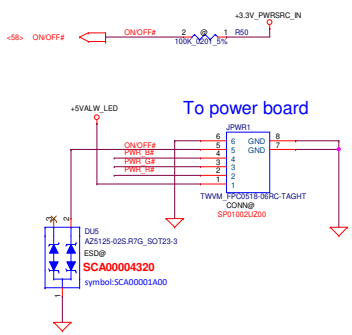


Main Func = TP LED

Touchpad LED circuit



Main Func = ON/OFF



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Issued Date	2021/02/27	Deciphered Date 2022/12/31	Title: ELC (2) TP/PW/LOOP/AW
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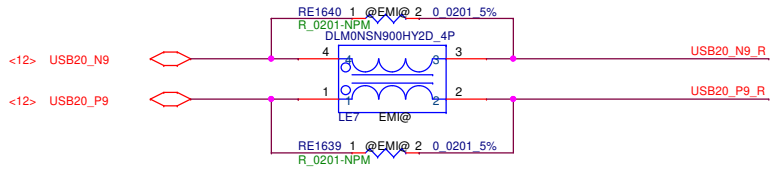
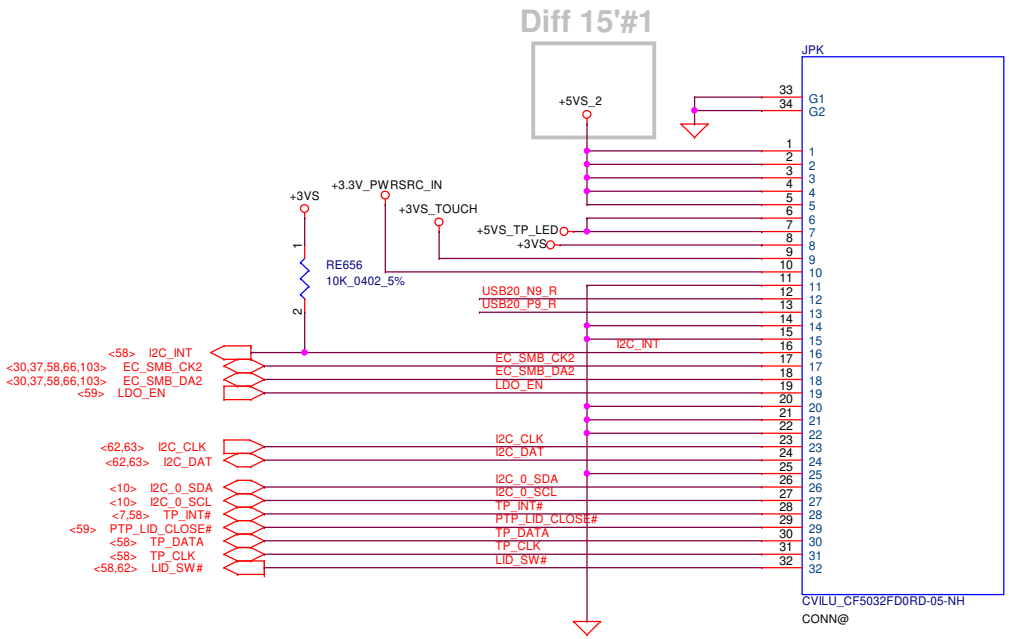
			Date: Thursday, November 25, 2021 Sheet 63 of 121





Per Key MCU board pin define

Pin1~5	+5VS_2
Pin6~7	+5VS_TP_LED
Pin8	+3VS
Pin9	+3S_TOUCH
Pin10	+3.3V_PWRSRC_IN
Pin11	GND
Pin12	D-
Pin13	D+
Pin14~15	GND
Pin16	I2C_INT
Pin17	I2C_CLK(EC)
Pin18	I2C_DAT(EC)
Pin19	LDO_EN
Pin20~22	GND
Pin23	I2C_CLK
Pin24	I2C_DAT
Pin25	GND
Pin26	I2C_0_SDA
Pin27	I2C_0_SCL
Pin28	TP_INT#
Pin29	PTP_LED_CLOSE#
Pin30	TP_DATA
Pin31	TP_CLK
Pin32	LID_SW#

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ELC (3) KBBL/Per Key

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Compal Electronics, Inc.

Title

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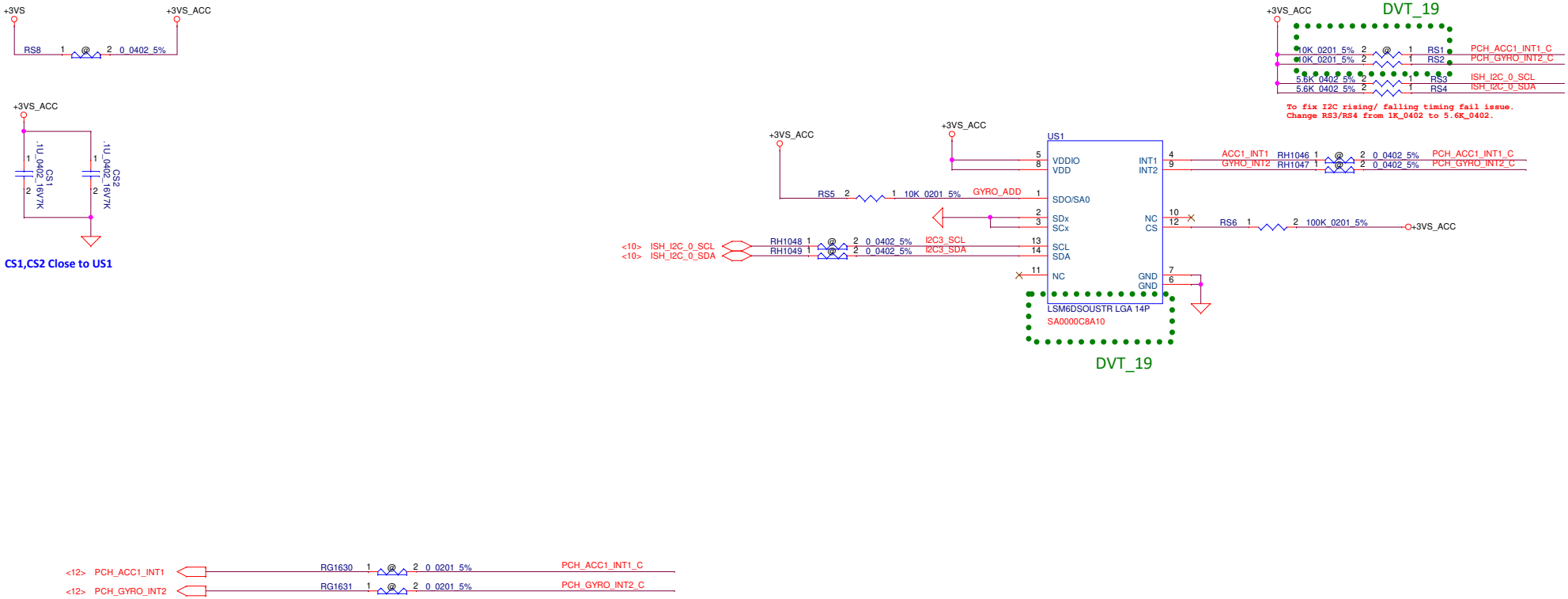
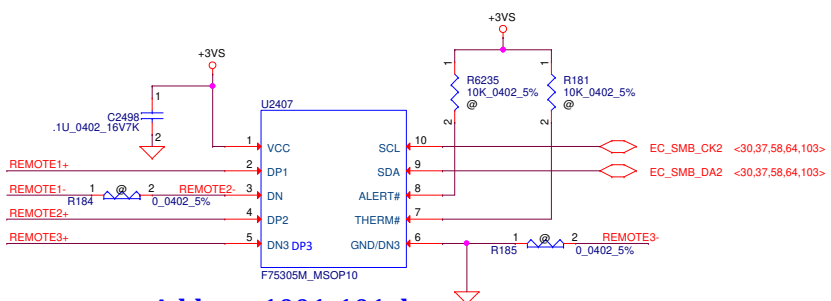


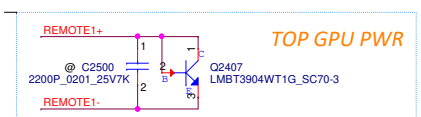
Fintek thermal sensor---> CPU core, DIMM

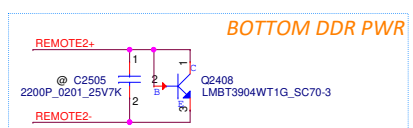


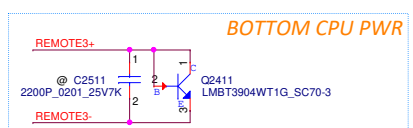
Address 1001_101xb

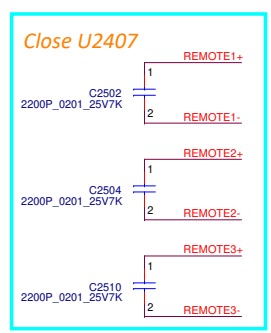
2nd source
SA000029210-->EMC1403-2-AIZL-TR

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"









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Compal Electronics, Inc.

Title

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Title			
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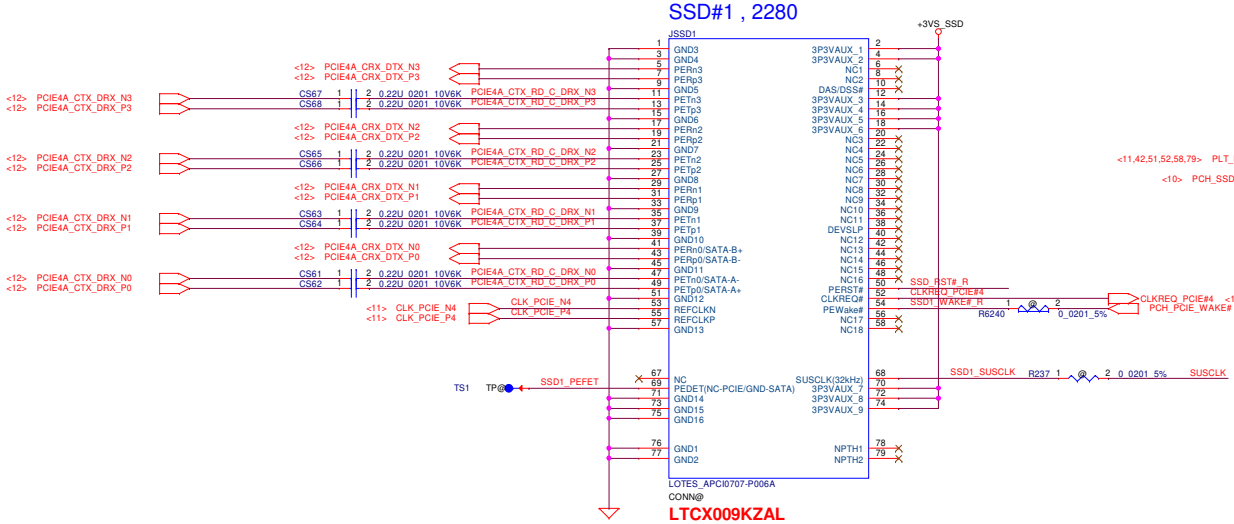
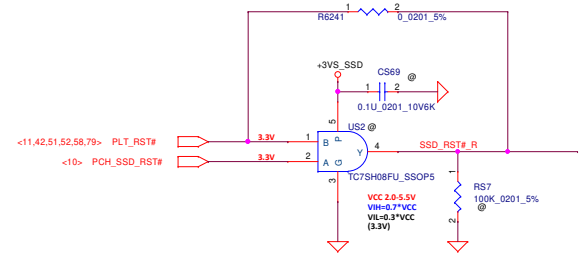
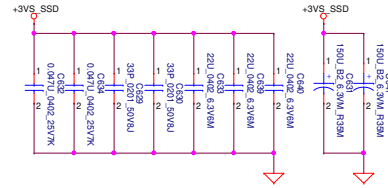
PCIe Gen4
SSD#1 , 2280

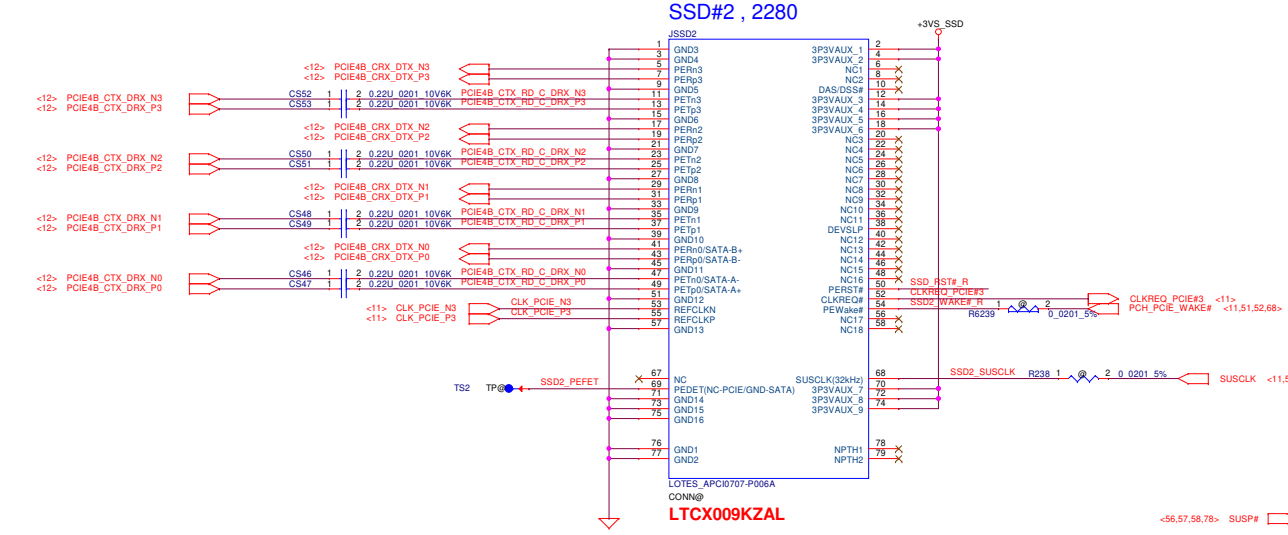




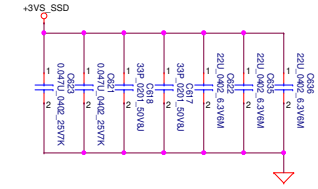
JSSD1

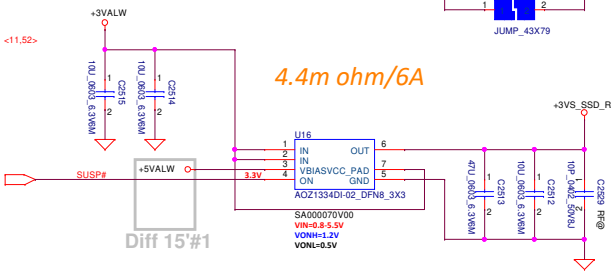


PCIe Gen4
SSD#2 , 2280



JSSD2





Security Classification	Compal Secret Data		
Issued Date	2021/02/27	Deciphered Date	2022/12/31

Compal Electronics, Inc.	
Title	NGFF SSD
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Compal Electronics, Inc.

Title			
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Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title

Size	Document Number	Rev
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Compal Electronics, Inc.

Title

Size | Document Number: **LA-L613P** | Rev 0.3

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Compal Electronics, Inc.		
Title		
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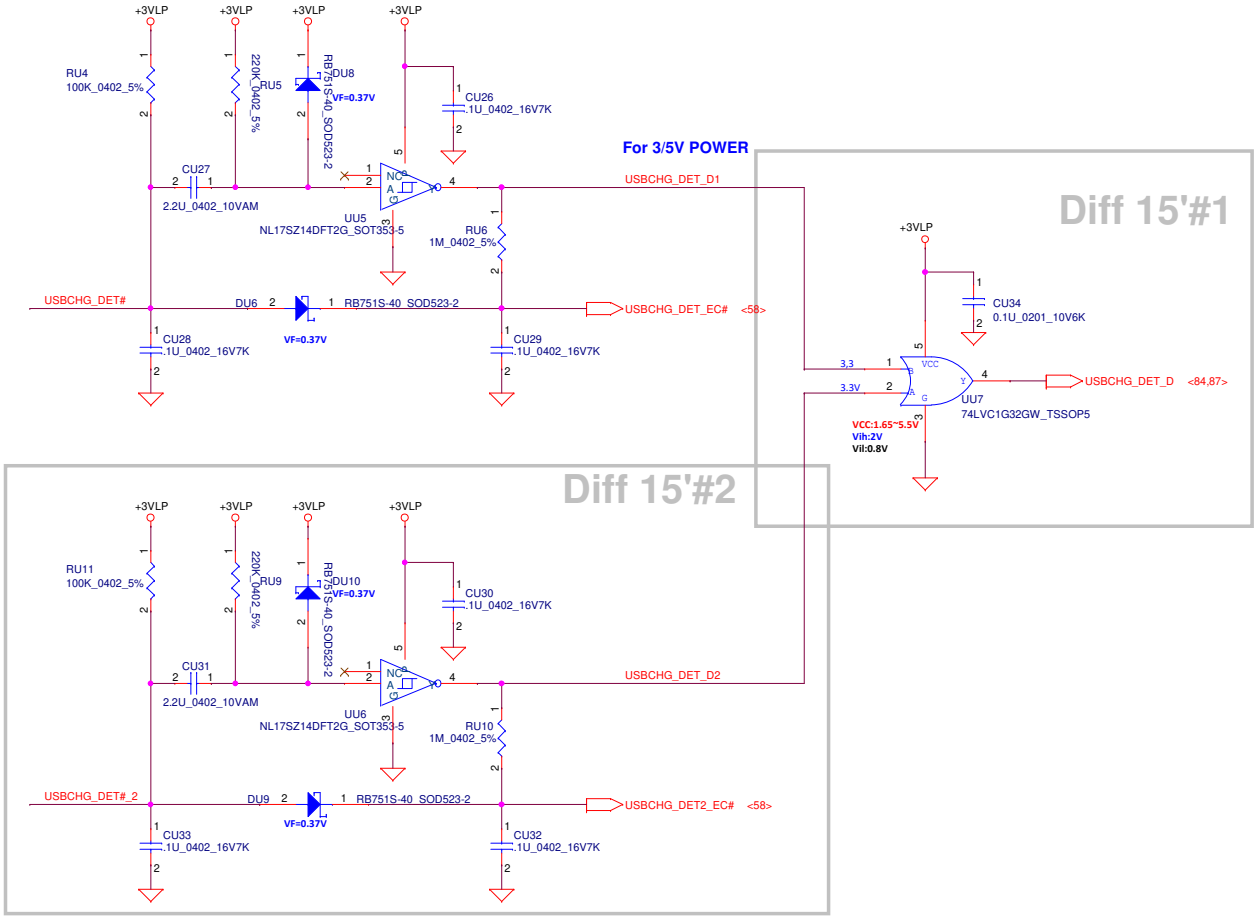
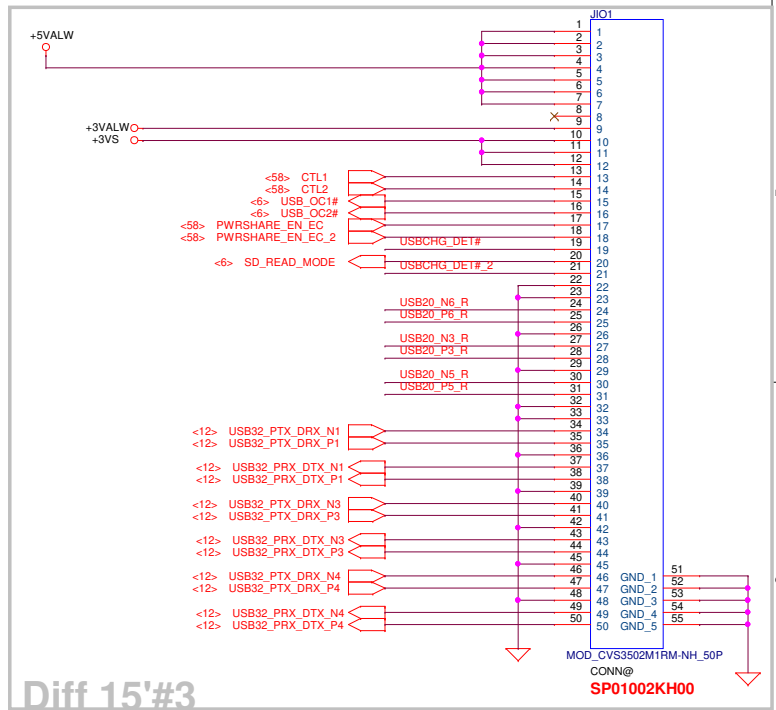
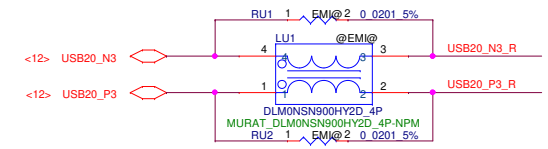
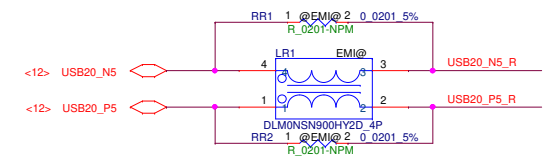
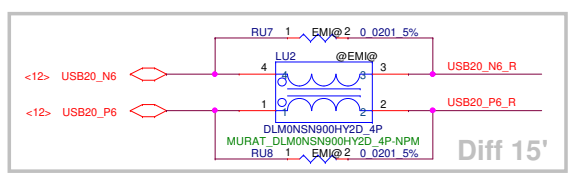
USB charge for DC S5











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Compal Electronics, Inc.

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Title

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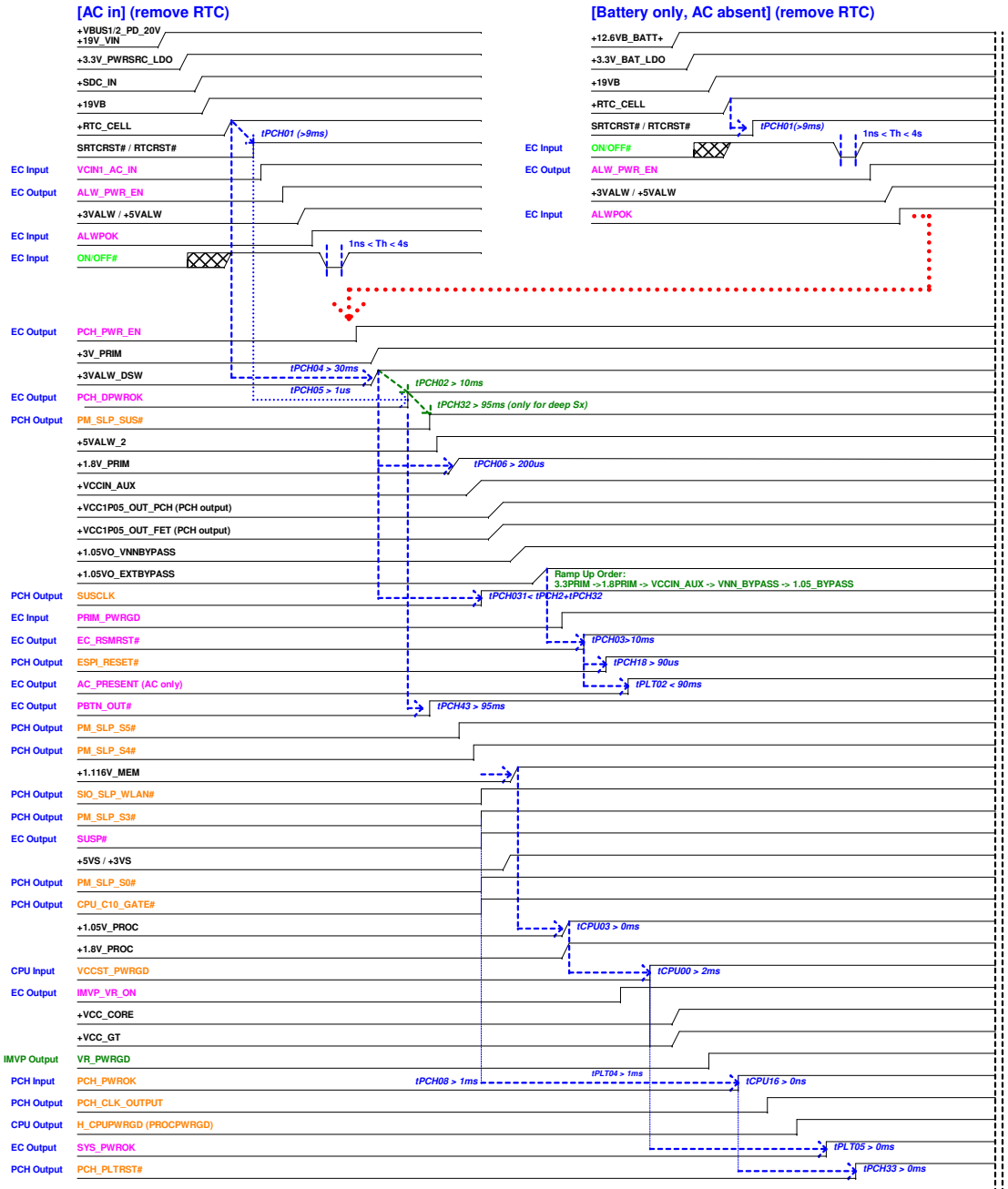
Power Sequence
G3 -> S0



GPU Sequence
GN20-E

Figure 3.4 GPU Power Up Sequencing for NVVDD/MSVDD merged rail

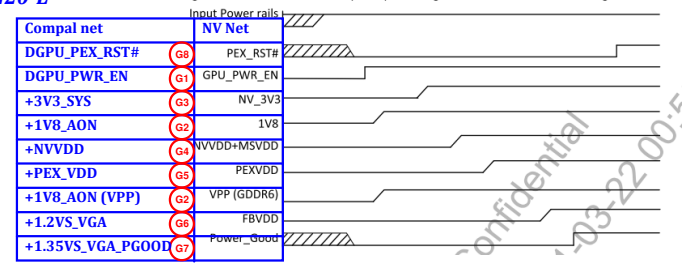
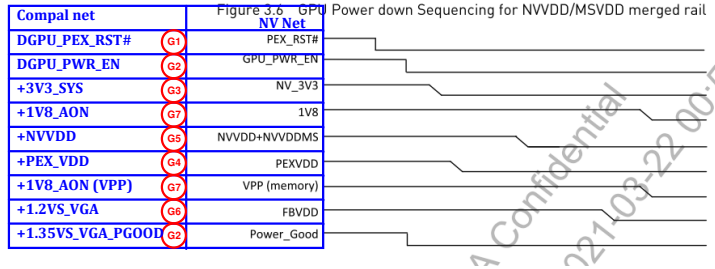


Figure 3.6 GPU Power down Sequencing for NVVDD/MSVDD merged rail



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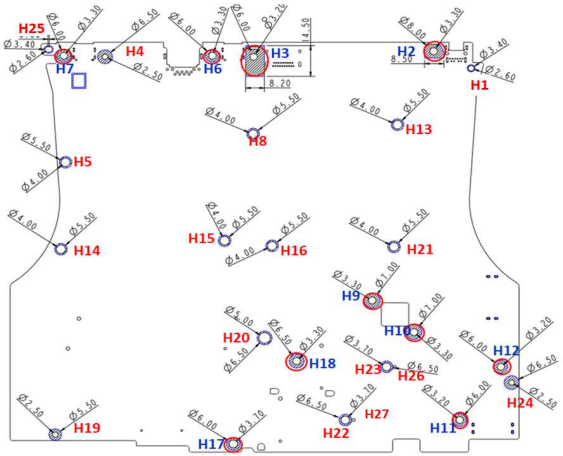
Main Func = Screw



PTH

H1 H_2P6-G @	H2 H_3P3-G @	H3 H_3P2 @	H4 H_2P5-G @	H5 H_4P0-G @	H8 H_4P0-G @	
H13 H_3P3-G @	H14 H_4P0-G @	H15 H_4P0-G @	H16 H_4P0-G @	H19 H_2P5-G @	H20 H_3P5-G @	
H21 H_4P0-G @	H22 H_3P7-G @	H23 H_3P7-G @	H24 H_2P5-G @	H25 H_2P6X3P2-G @		

Stand-off

H6 H_3P3 @	H7 H_3P3 @	H9 H_3P3 @	H10 H_3P3 @
H11 H_3P2 @	H12 H_3P2 @	H18 H_3P3 @	

NPTH

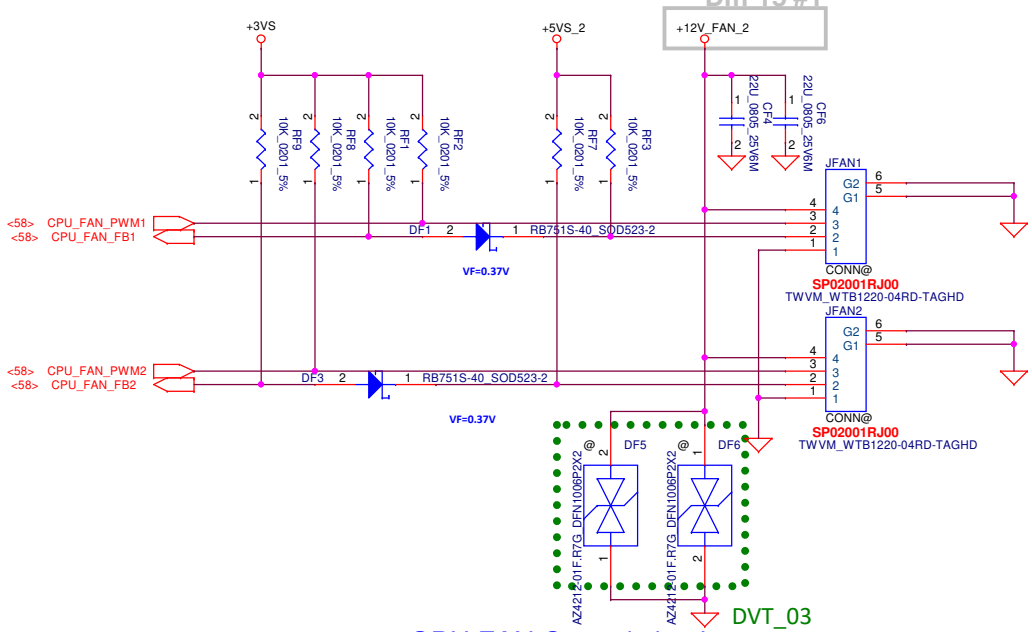
H26 H_1P3N @	H27 H_1P3N @

Fiducial Mark

FD1 @FIDUCIAL	FD2 @FIDUCIAL	FD3 @FIDUCIAL	
FD4 @FIDUCIAL	FD5 @FIDUCIAL	FD6 @FIDUCIAL	
FD7 @FIDUCIAL	FD8 @FIDUCIAL	FD9 @FIDUCIAL	FD10 @FIDUCIAL

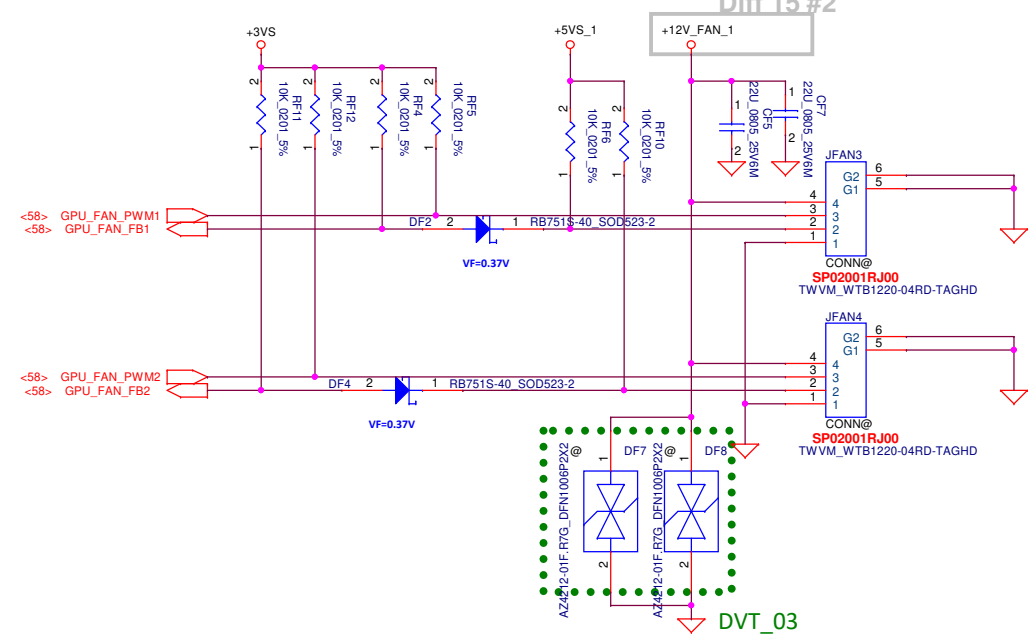
CPU FAN Control circuit

Diff 15'#1



GPU FAN Control circuit

Diff 15'#2



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Compal Electronics, Inc.	
Title	FAN/Screw Hole
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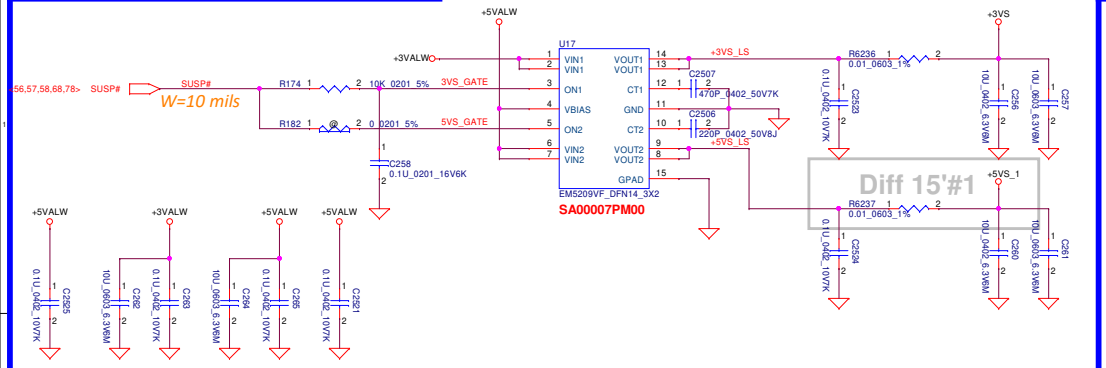
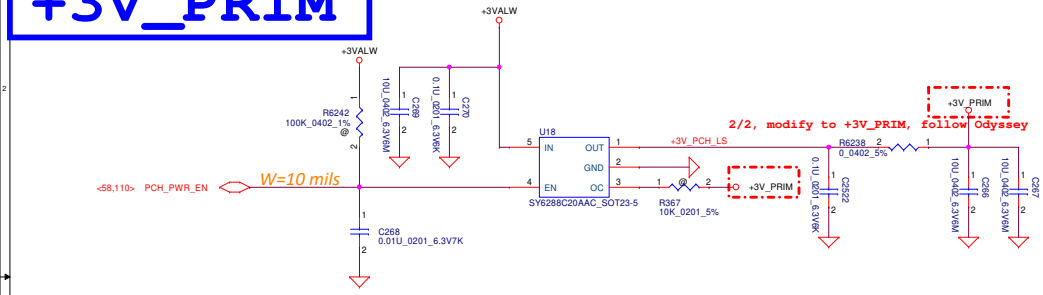
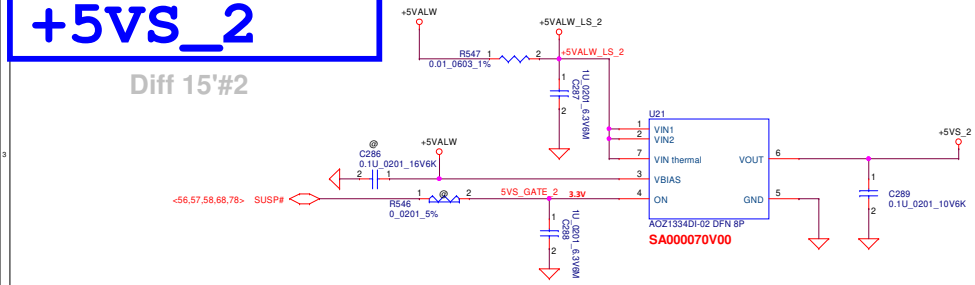
+3VS/+5VS_1



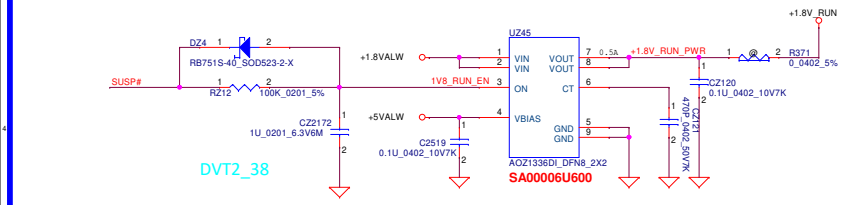
+3V_PRIM



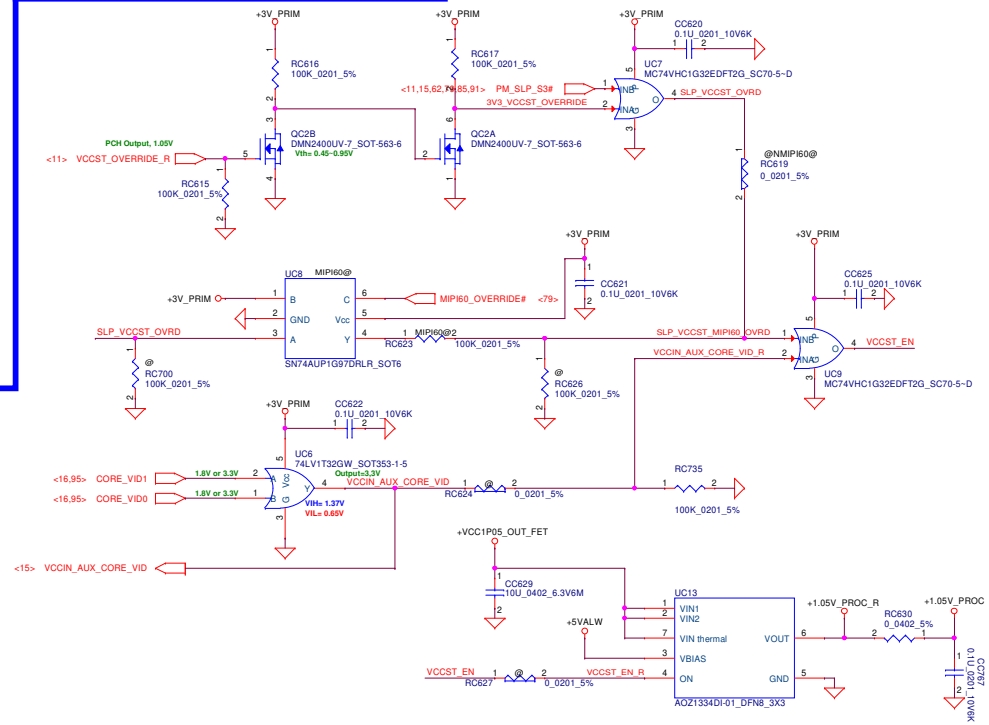
+5VS_2



+1V8_RUN

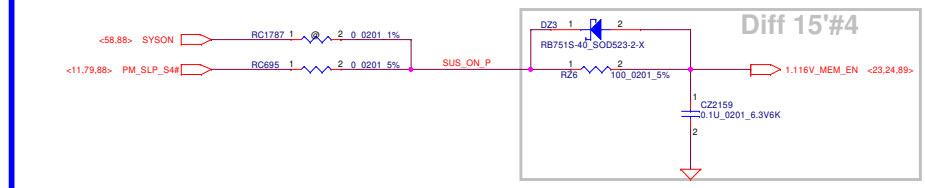


+1.05V_PROC



+1V8_RUN

SUS_ON(DDR EN)



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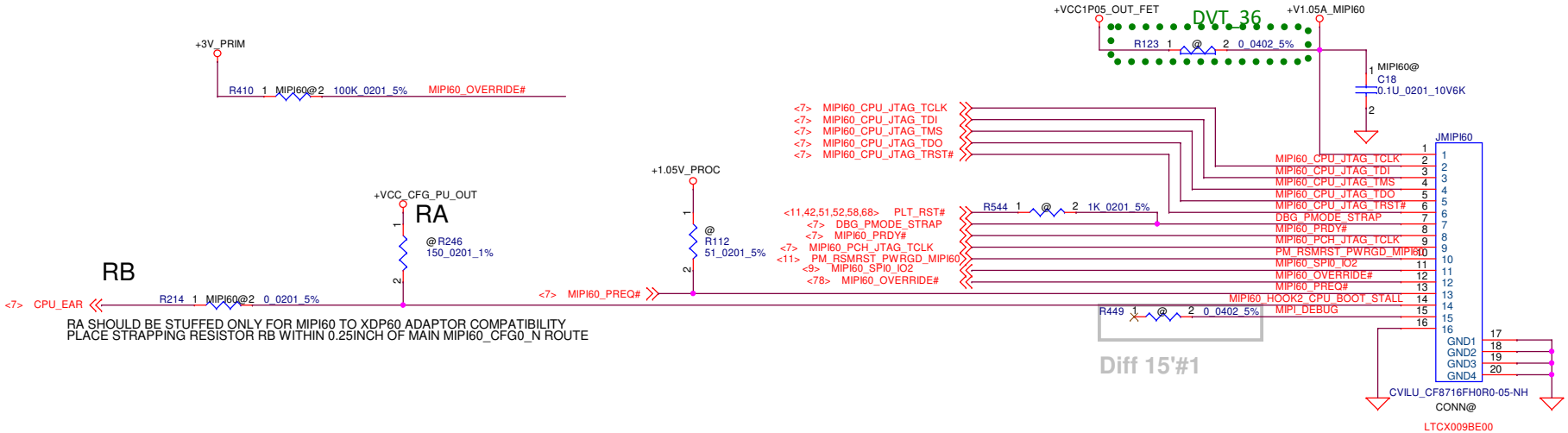
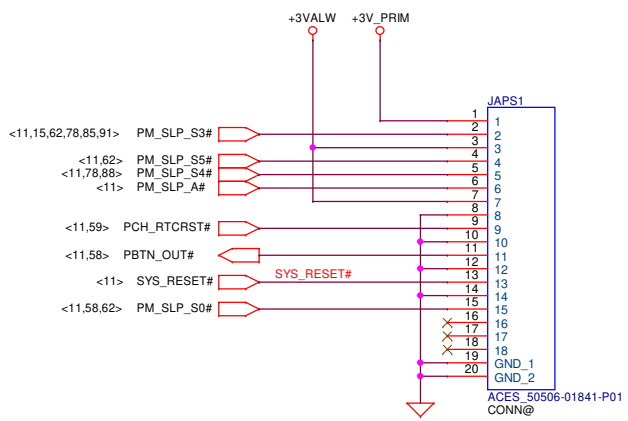
MIPI60



APS



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Compal Electronics, Inc.			
Title: Debug APS,MIPI60			
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Compal Electronics, Inc.

Title: ***Reserve***

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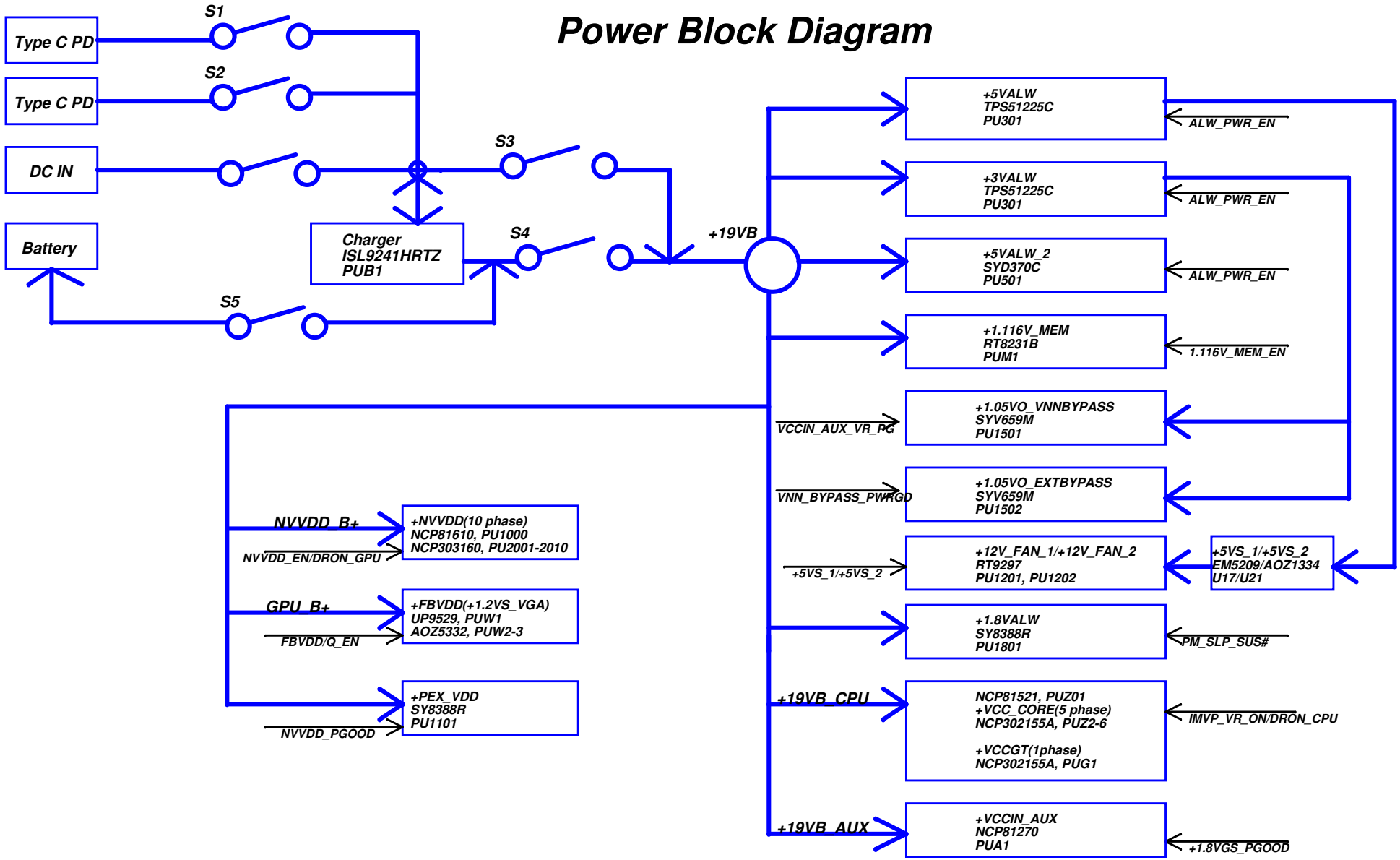
Power Block Diagram



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Title: PWR_POWER BLOCK DIAGRAM

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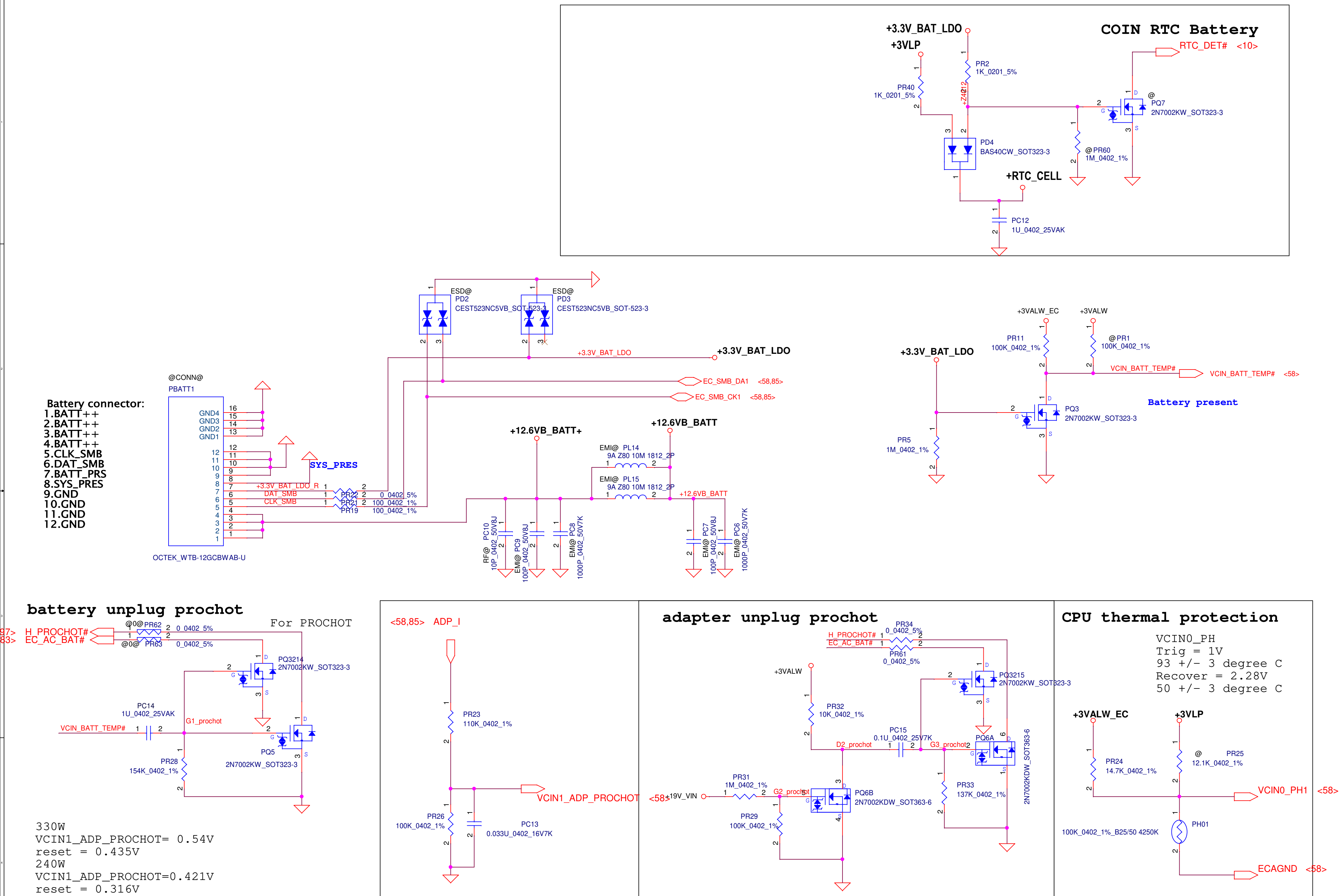

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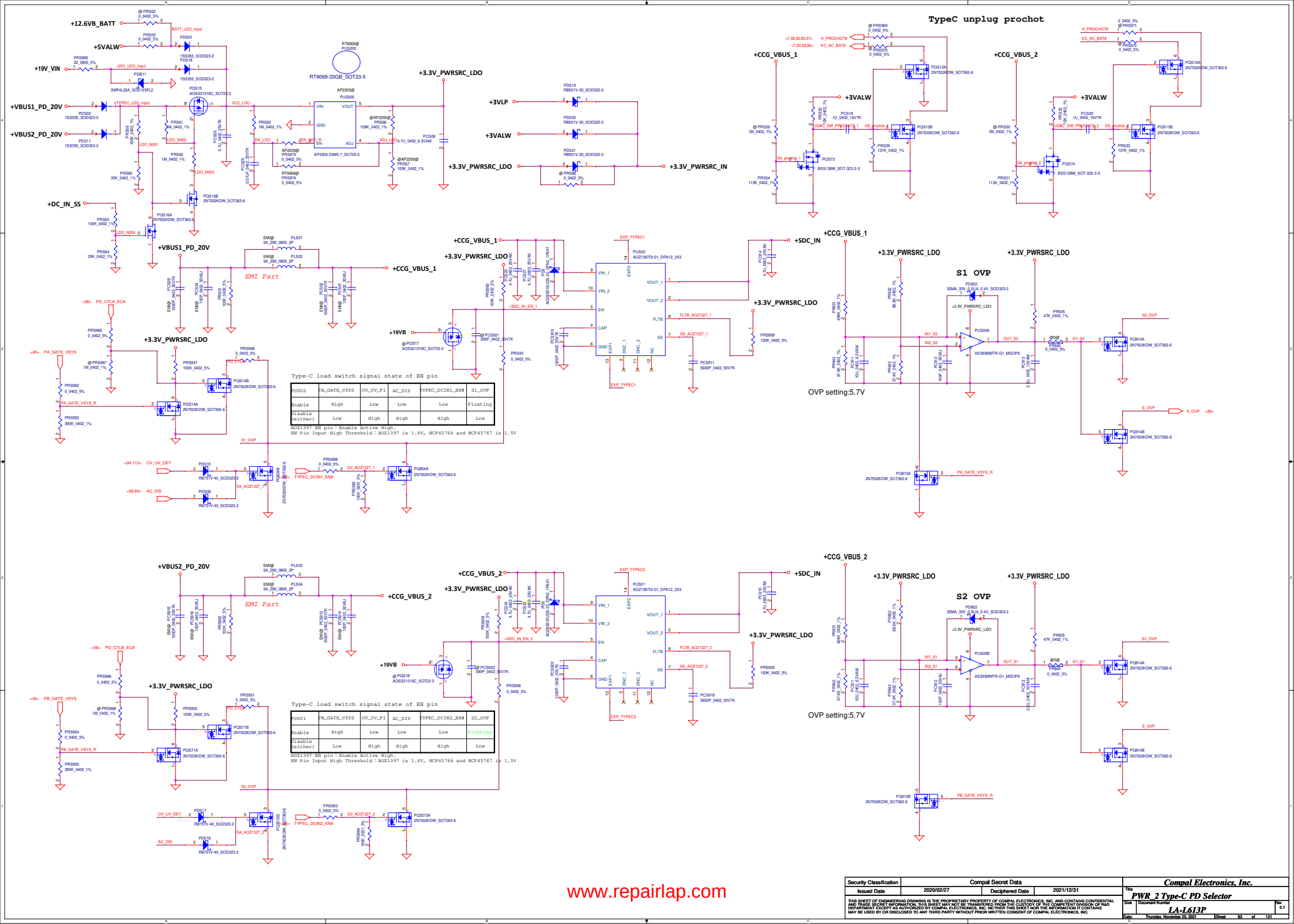

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Title: PWR_2 Type-C PD Selector

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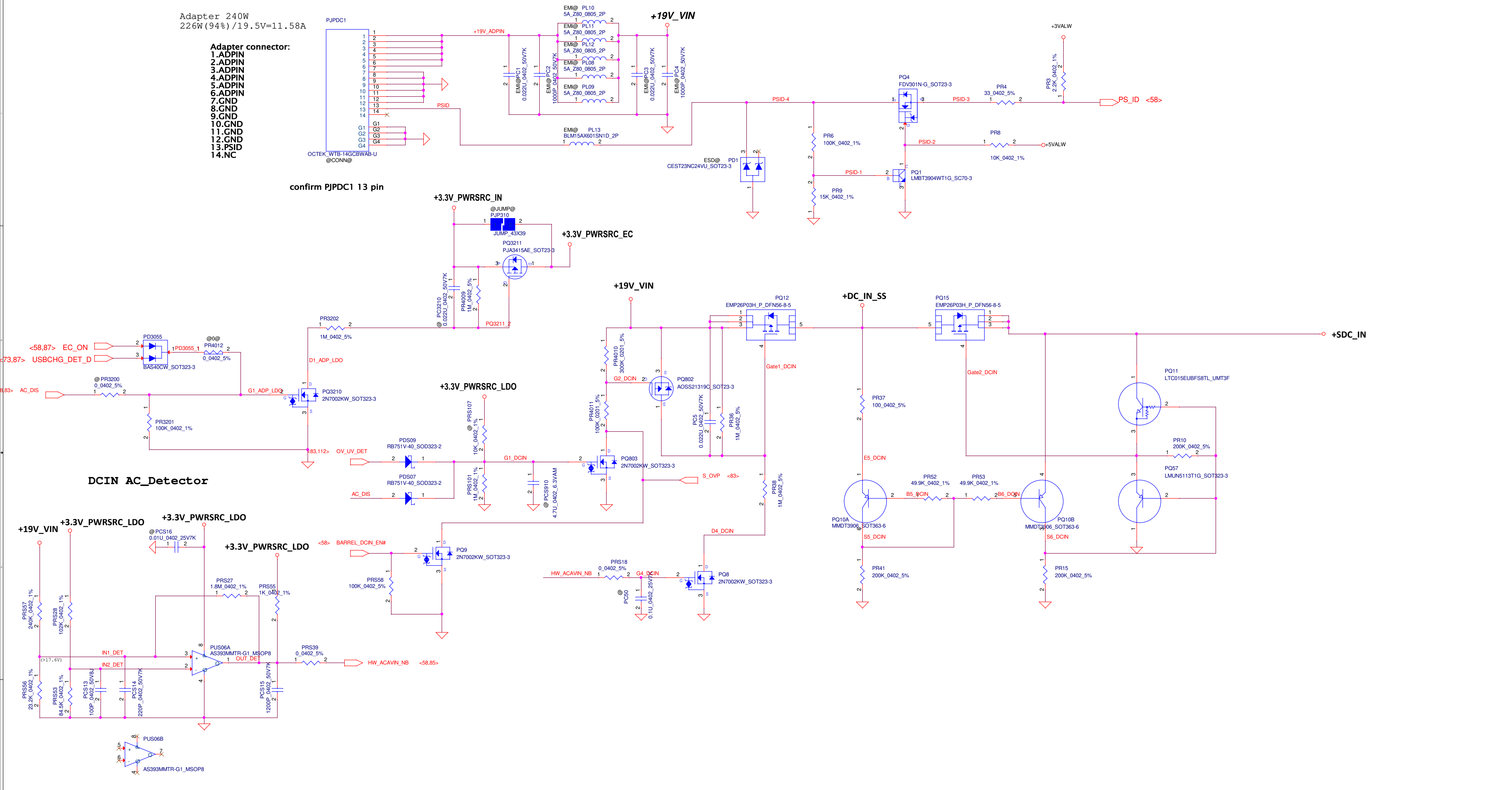

Adapter 240W
226W(94%)/19.5V=11.58A
Adapter connector:
1.ADPIN
2.ADPIN
3.ADPIN
4.ADPIN
5.ADPIN
6.ADPIN
7.GND
8.GND
9.GND
10.GND
11.GND
12.GND
13.PSID
14.NC
confirm PJPDC1 13 pin
PJPDC1
OCTEK_WTB-14GCBWAB-U
@CONN@
+19V_ADPIN
PSID
+19V_VIN
EMI@ PL10 5A_Z80_0805_2P
EMI@ PL11 5A_Z80_0805_2P
EMI@ PL12 5A_Z80_0805_2P
EMI@ PL08 5A_Z80_0805_2P
EMI@ PL09 5A_Z80_0805_2P
EMI@ PL13 BLM15AX601SN1D_2P
EMI@PC1 0.022U_0402_50V7K
EMI@PC2 1000P_0402_50V7K
EMI@PC3 0.022U_0402_50V7K
EMI@PC4 1000P_0402_50V7K
+3VALW
PR3 2.2K_0402_1%
PQ4 FDV301N-G_SOT23-3
PR4 33_0402_5%
PSID-4
PSID-3
PS_ID <58>
PR8 10K_0402_1%
PSID-2
+5VALW
PR6 100K_0402_1%
PR9 15K_0402_1%
PSID-1
PQ1 LMBT3904WT1G_SC70-3
ESD@ PD1 CEST23NC24VU_SOT23-3
+3.3V_PWRSRC_IN
@JUMP@ PJP310 JUMP_43X39
+3.3V_PWRSRC_EC
PQ3211 PJA3415AE_SOT23-3
@ PC3210 0.022U_0402_50V7K
PR4009 1M_0402_5%
PQ3211_2
PR3202 1M_0402_5%
D1_ADP_LDO
<58,87> EC_ON
<73,87> USBCHG_DET_D
PD3055 BAS40CW_SOT323-3
PD3055_1
@0@ PR4012 0_0402_5%
AC_DIS
@ PR3200 0_0402_5%
G1_ADP_LDO
PQ3210 2N7002KW_SOT323-3
PR3201 100K_0402_1%
<83,112> OV_UV_DET
DCIN AC_Detector
+3.3V_PWRSRC_LDO
PDS09 RB751V-40_SOD323-2
PDS07 RB751V-40_SOD323-2
@ PRS107 10K_0402_1%
PRS101 1M_0402_1%
G1_DCIN
@ PCS910 4.7U_0402_6.3VAM
+19V_VIN
PR4010 300K_0201_5%
G2_DCIN
PQ802 AOSS21319C_SOT23-3
PR4011 100K_0201_5%
PC5 0.022U_0402_50V7K
PR36 1M_0402_5%
PQ803 2N7002KW_SOT323-3
S_OVP <83>
PQ12 EMP26P03H_P_DFN56-8-5
Gate1_DCIN
PR38 1M_0402_5%
D4_DCIN
+DC_IN_SS
PR37 100_0402_5%
E5_DCIN
PQ15 EMP26P03H_P_DFN56-8-5
Gate2_DCIN
+SDC_IN
PQ11 LTC015EUBFS8TL_UMT3F
PR10 200K_0402_5%
PQ57 LMUN5113T1G_SOT323-3
PR52 49.9K_0402_1%
PR53 49.9K_0402_1%
B5_DCIN
B6_DCIN
PQ10A MMDT3906_SOT363-6
PQ10B MMDT3906_SOT363-6
S5_DCIN
S6_DCIN
PR41 200K_0402_5%
PR15 200K_0402_5%
+19V_VIN
+3.3V_PWRSRC_LDO
@PCS16 0.01U_0402_25V7K
PRS27 1.8M_0402_1%
PRS55 1K_0402_1%
PRS57 240K_0402_1%
PRS28 102K_0402_1%
IN1_DET
IN2_DET
(>17.6V)
PUS06A AS393MMTR-G1_MSOP8
OUT_DET
PRS39 0_0402_5%
HW_ACAVIN_NB <58,85>
PRS56 23.2K_0402_1%
PRS53 84.5K_0402_1%
PCS13 100P_0402_50V8J
PCS14 220P_0402_50V7K
PCS15 1200P_0402_50V7K
PUS06B AS393MMTR-G1_MSOP8
<58> BARREL_DCIN_EN#
PQ9 2N7002KW_SOT323-3
PRS58 100K_0402_5%
HW_ACAVIN_NB
PRS18 0_0402_5%
G4_DCIN
@ PC50 0.1U_0402_25V7K
PQ8 2N7002KW_SOT323-3

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Title: *PWR_DCIN/Back to back*

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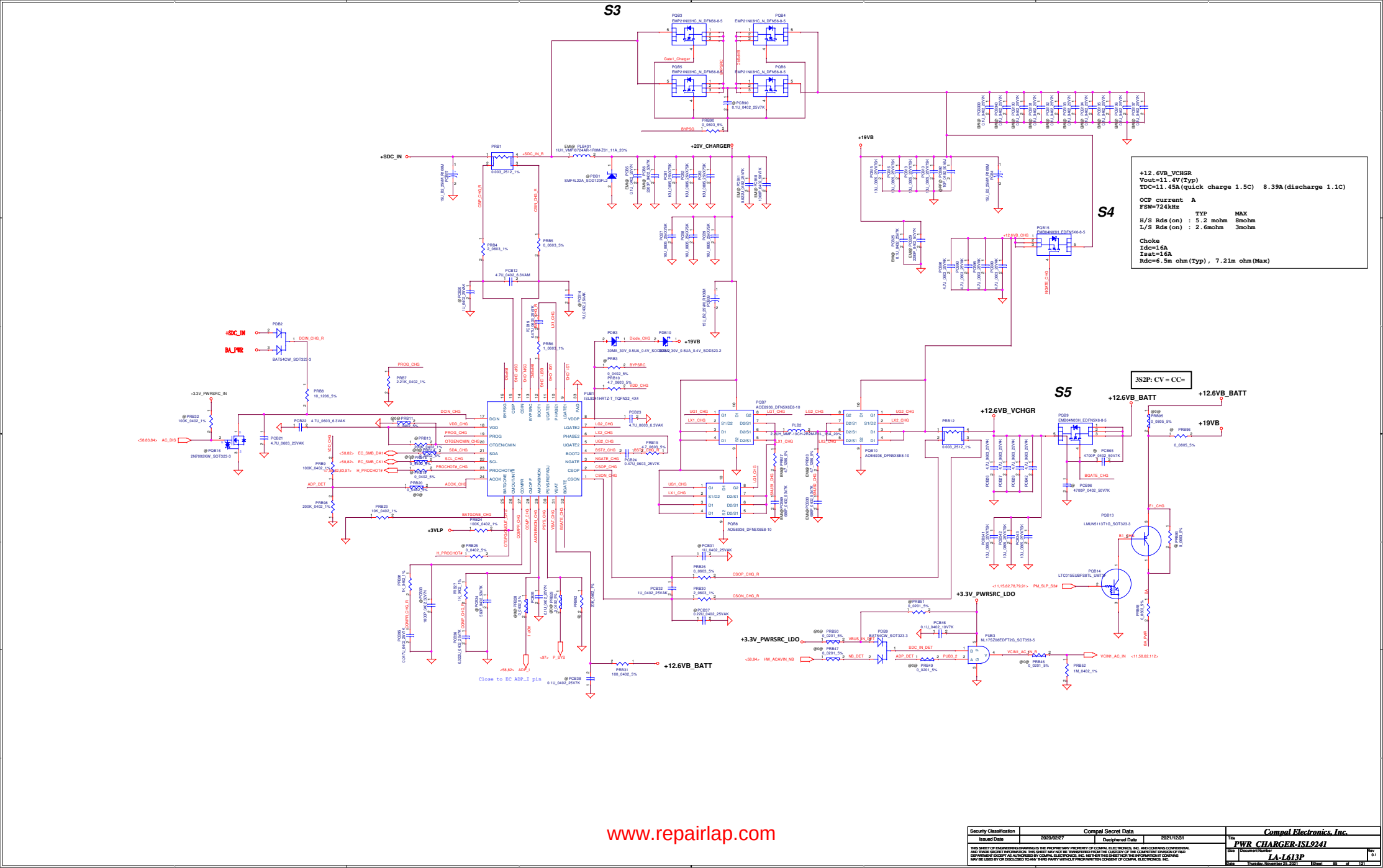

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Compal Electronics, Inc.

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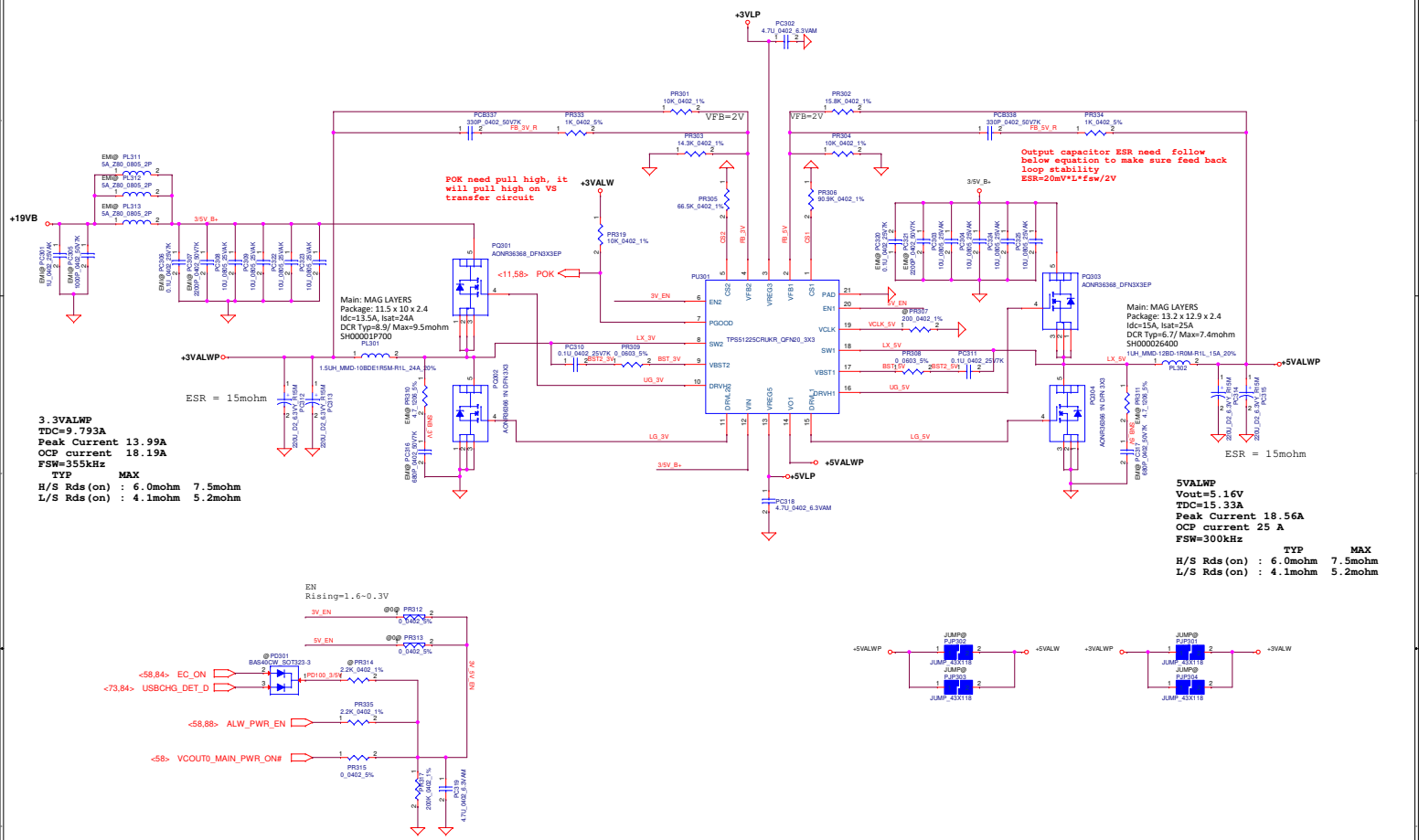

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Issued Date	2020/02/27	Deciphered Date	2021/12/31

Title	PWR +3.3VALWP/+5VALWP		
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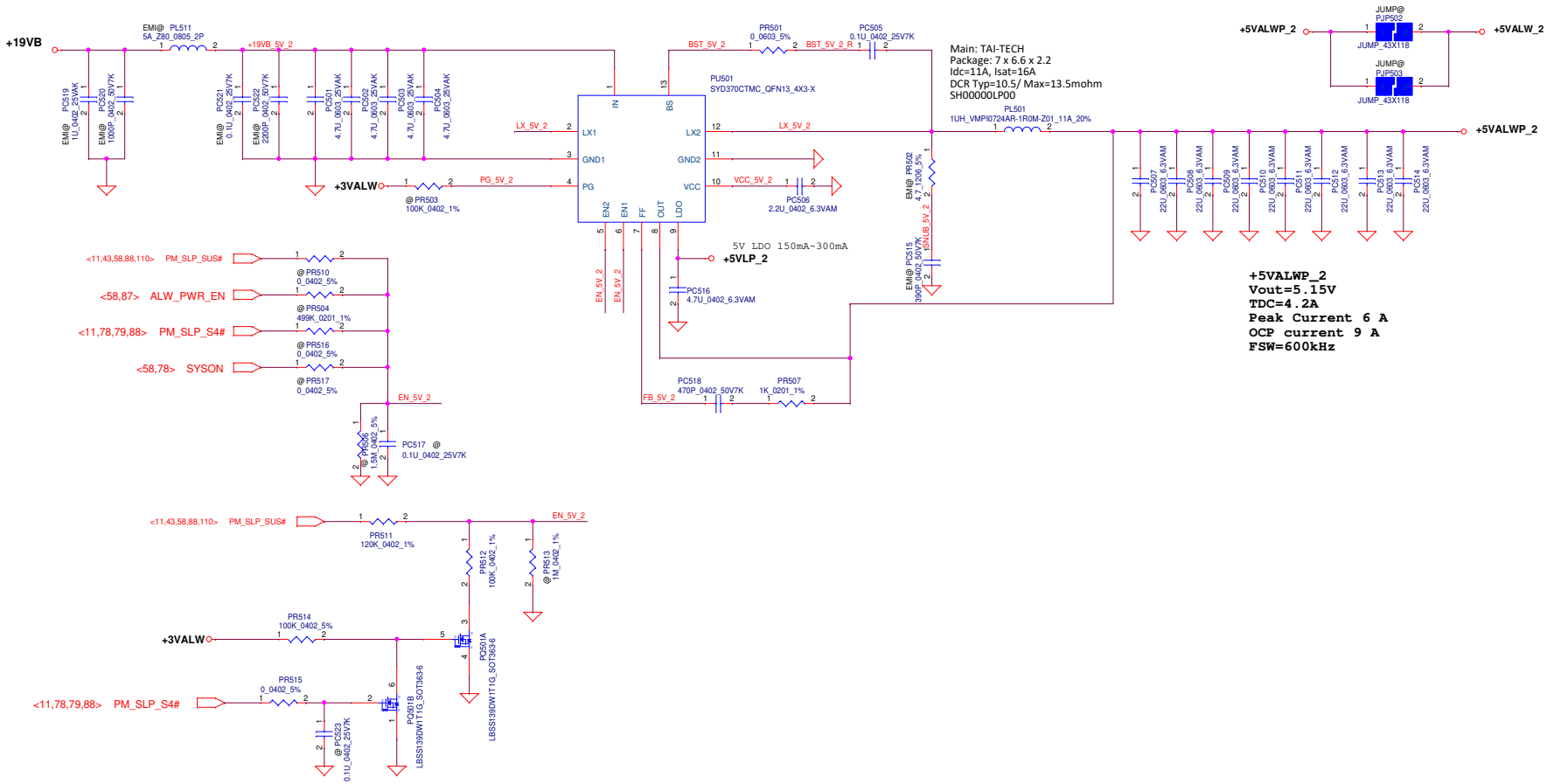

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Title	PWR_+5VALWP_2
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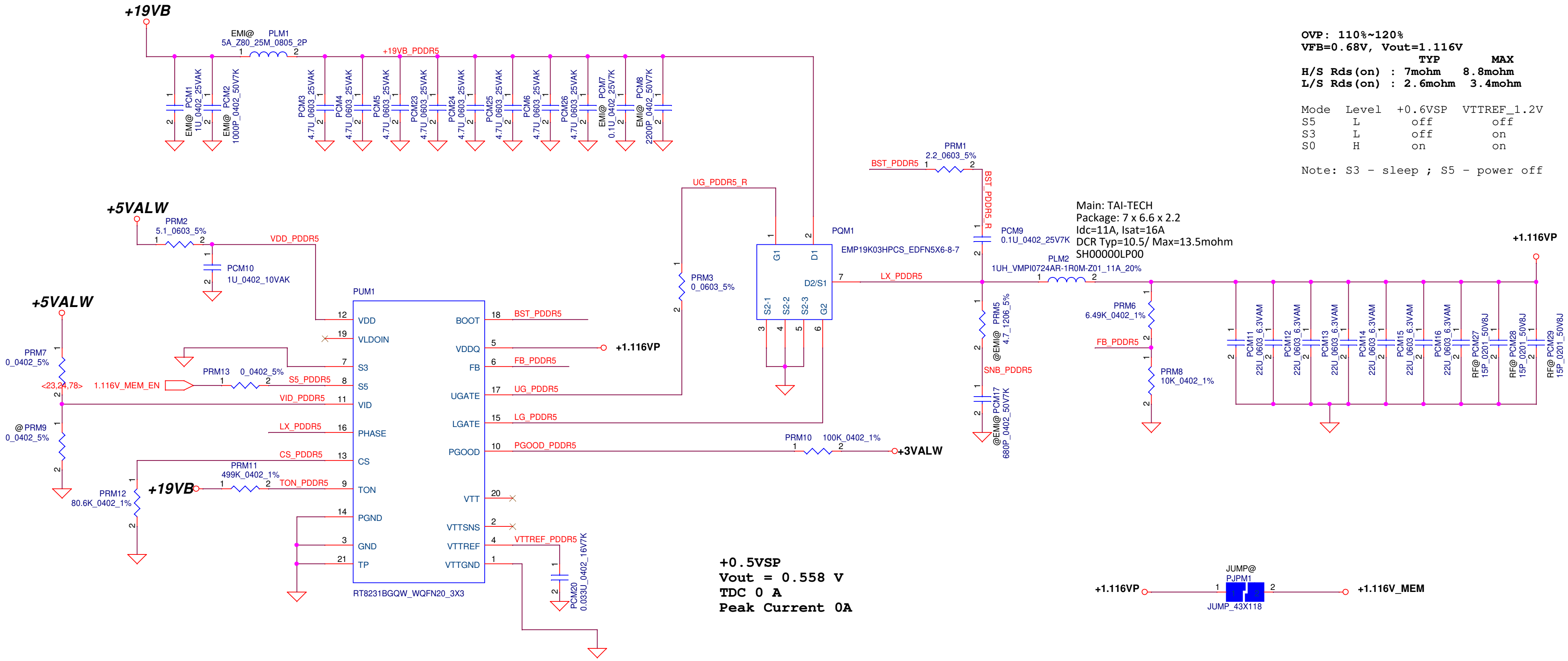
+1.116VP
Vout = 1.116 V
TDC 3.01A
Peak Current 4.3A
OCP 12A
Fsw 520kHz

OVP: 110%~120%
VFB=0.68V, Vout=1.116V

	TYP	MAX
H/S Rds(on) :	7mohm	8.8mohm
L/S Rds(on) :	2.6mohm	3.4mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



+0.5VSP
Vout = 0.558 V
TDC 0 A
Peak Current 0A

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Issued Date	2020/02/27	Deciphered Date	2021/12/31

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Compal Electronics, Inc.

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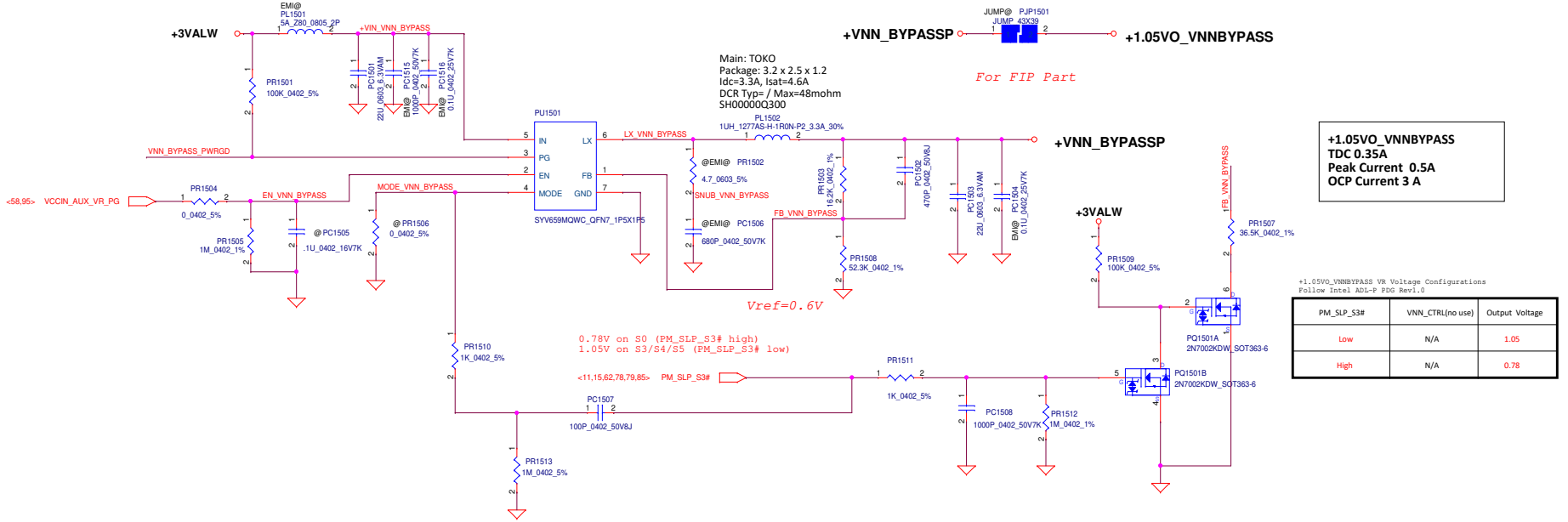

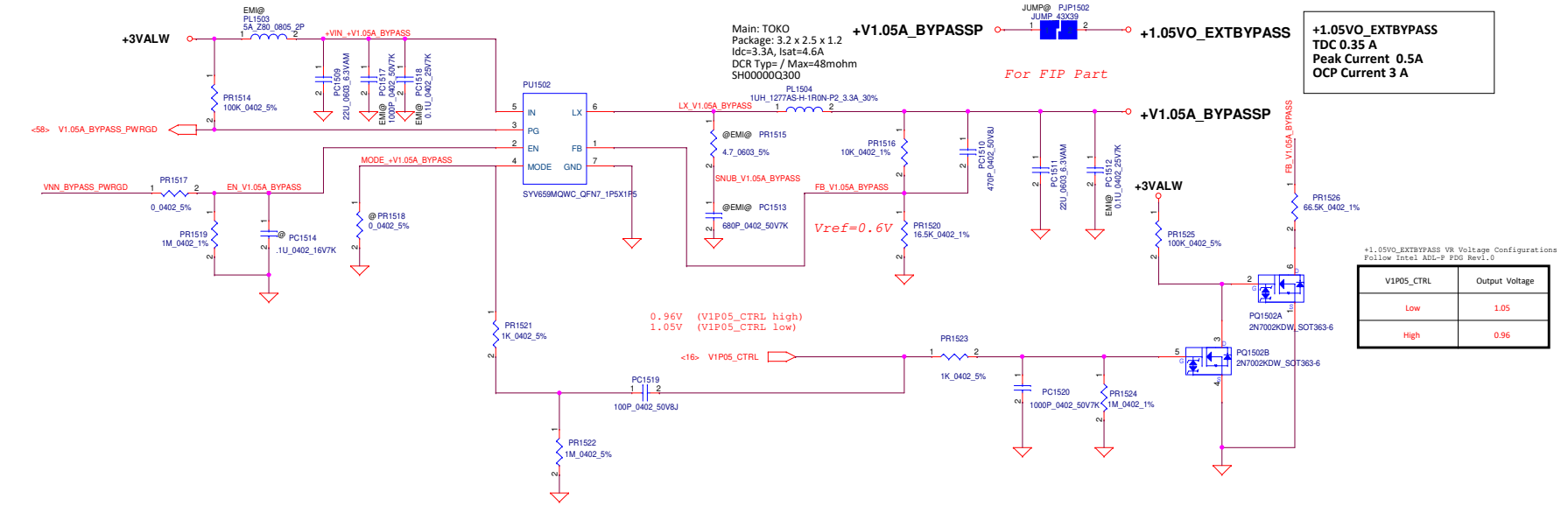

VCC_VNNEXT_1P05 (VNN_BYP) and VCC_V1P05EXT_1P05 (V1P05_BYP) are two dedicated voltage regulators that save platform power during low power states (Sx/S0ix).
Both VCC_V1P05EXT_1P05 and VCC_VNNEXT_1P05 are VIDed rails that operate at two voltage levels each. The VID control for this VR is the SLP_S3#,V1P05_CTRL, VNN_CTRL (optional) signals.

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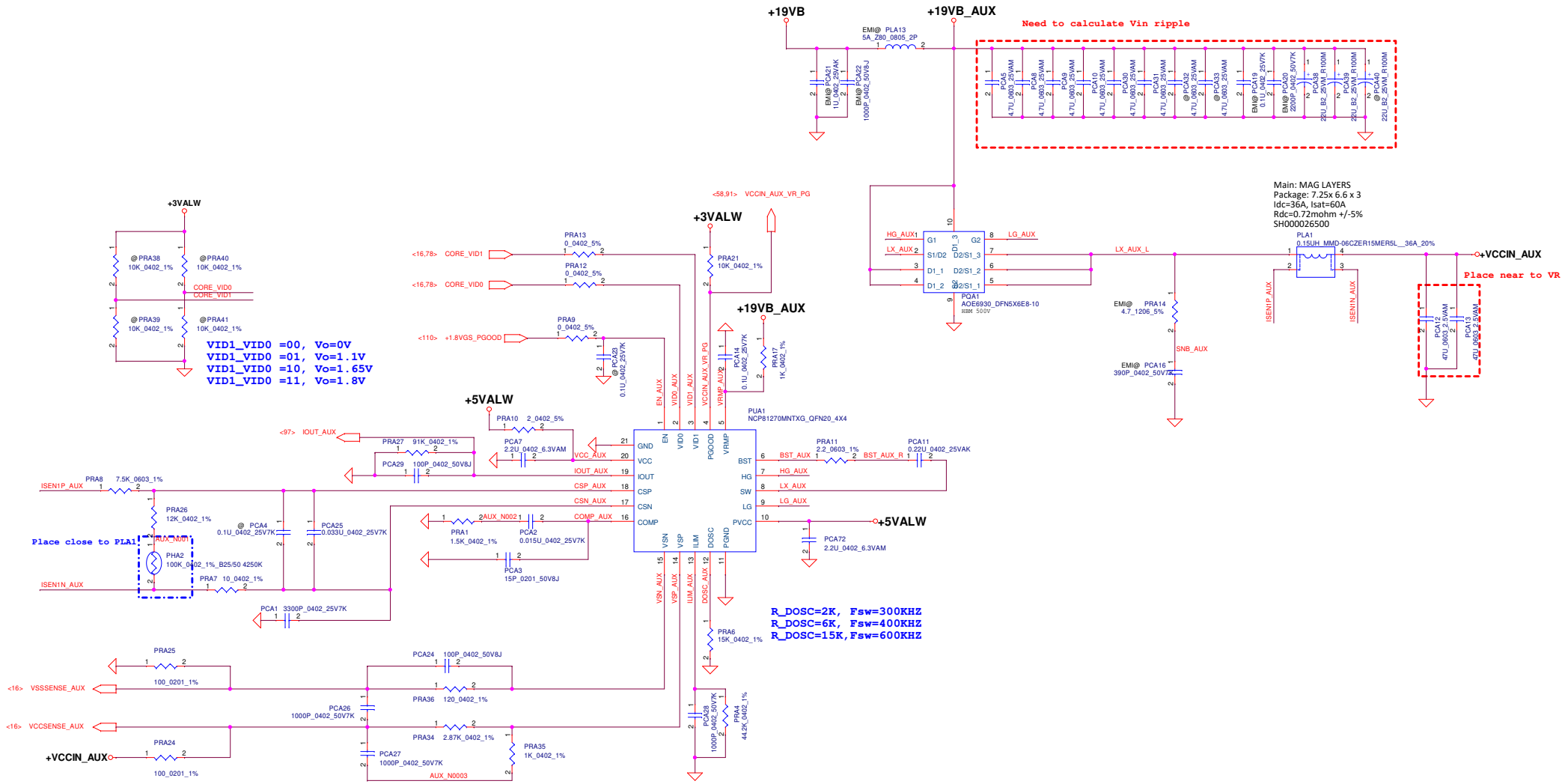
Main Func = +VCCIN_AUX

+VCCIN_AUX
Vout 1.8V
IPL2(TDC) = 17A
Peak Current = 34.2A(ICCmax)
OCP 44.46 A
FSW= 600KHz



Security Classification	Compal Secret Data		
Issued Date	2021/01/07	Deciphered Date	2021/01/07

Compal Electronics, Inc.

Title

Size	Document Number	Rev
	LA-L613P	0.2

Date: Thursday, November 25, 2021 | Sheet 95 of 120

Main Func = +VCCIN_AUX DECOUPLING

Follow Intel ADL-P PDG Rev1.0
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF *1pcs
47uF_0603 *4 pcs

CPU Secondary side:
10uF_0402 *10pcs
47uF_0603 *4pcs

Compal
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF_B2 *4pcs
22uF_0603_low-noise *8 pcs

CPU Secondary side:
22uF_0603_low-noise *19 pcs

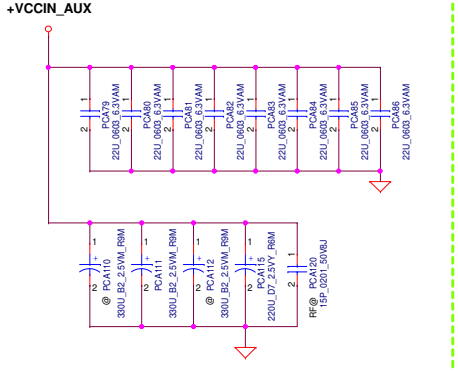
Compal(follow PDG)
+VCCIN_AUX Output CAP :

CPU Primary Side:
330uF_B2 *5pcs
47uF_0603_low-noise *4 pcs

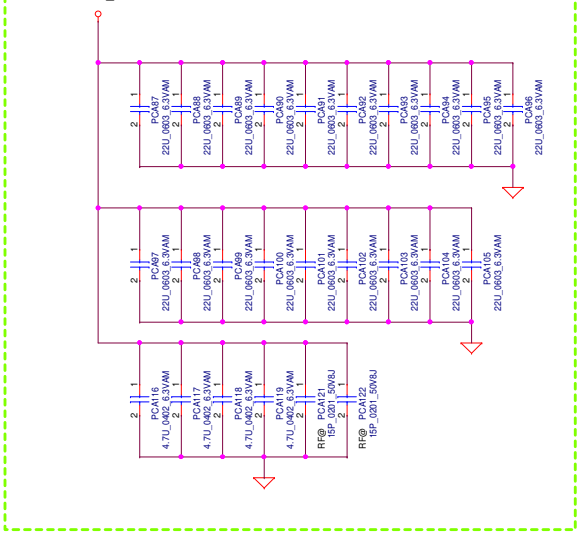
CPU Secondary side:
10uF_0603_low-noise *10 pcs
47uF_0603_low-noise *4 pcs

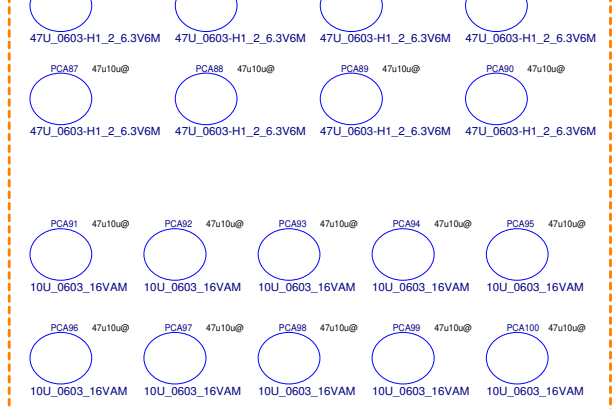
For FIVR solution
15pF_0201 *6
12pF_0402 *6
on EE side (20200214)

CPU Primary Side



CPU Secondary side





Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_VCCIN_AUX DECOUPLING

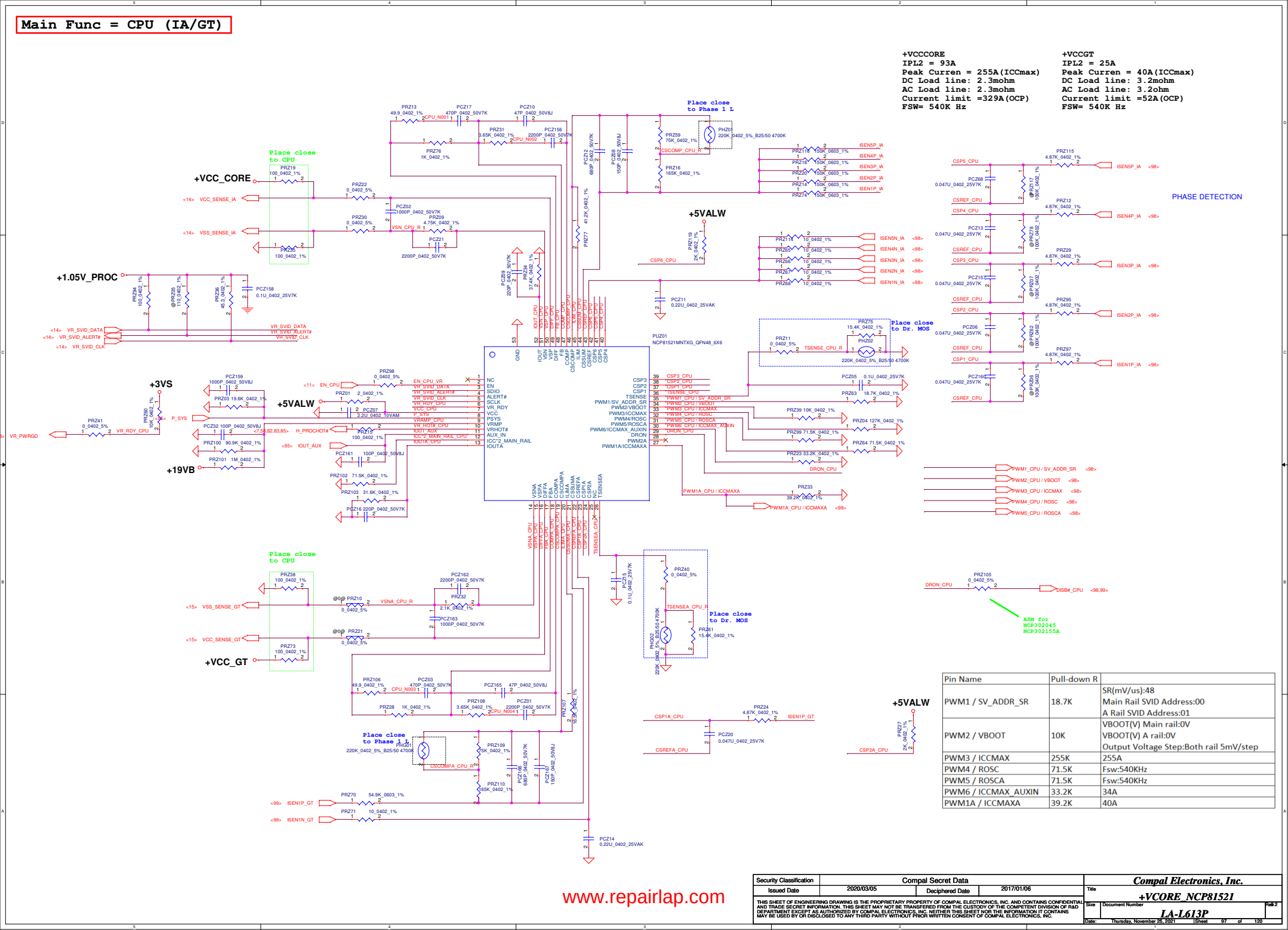
Size	Document Number	Rev
	LA-L613P	0.1

Date: Thursday, November 25, 2021 Sheet 96 of 121

Main Func = CPU (IA/GT)

+VCCCORE
IPL2 = 93A
Peak Curren = 255A(ICCmax)
DC Load line: 2.3mohm
AC Load line: 2.3mohm
Current limit =329A(OCP)
FSW= 540K Hz

+VCCGT
IPL2 = 25A
Peak Curren = 40A(ICCmax)
DC Load line: 3.2mohm
AC Load line: 3.2ohm
Current limit =52A(OCP)
FSW= 540K Hz



Pin Name	Pull-down R	
PWM1 / SV_ADDR_SR	18.7K	SR(mV/us):48 Main Rail SVID Address:00 A Rail SVID Address:01
PWM2 / VBOOT	10K	VBOOT(V) Main rail:0V VBOOT(V) A rail:0V Output Voltage Step:Both rail 5mV/step
PWM3 / ICCMAX	255K	255A
PWM4 / ROSC	71.5K	Fsw:540KHz
PWM5 / ROSCA	71.5K	Fsw:540KHz
PWM6 / ICCMAX_AUXIN	33.2K	34A
PWM1A / ICCMAXA	39.2K	40A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/03/05	Deciphered Date 2017/01/06	Title: +VCORE_NCP81521
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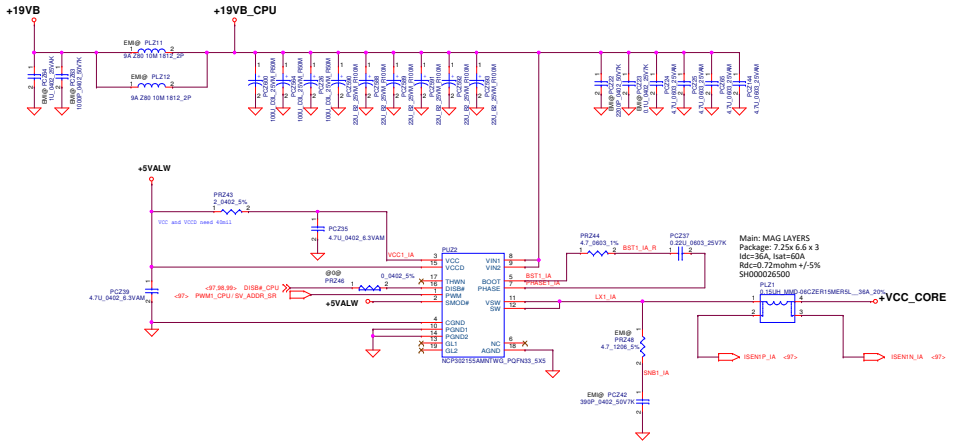
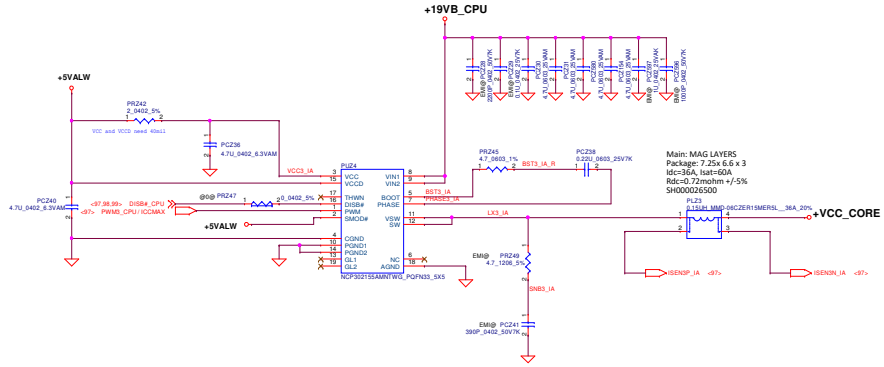
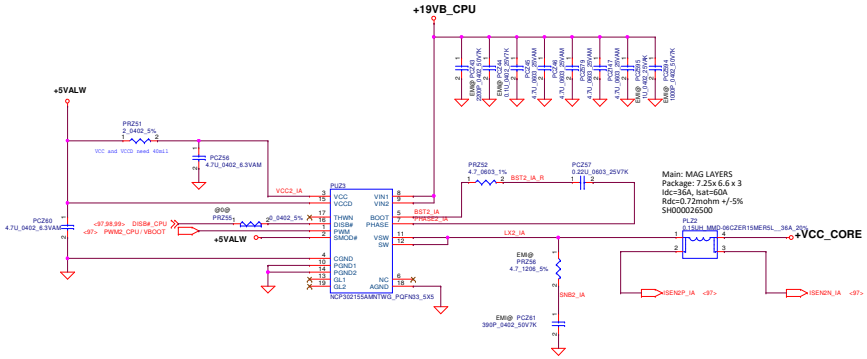
			Date: Thursday, November 25, 2021 Sheet 97 of 120

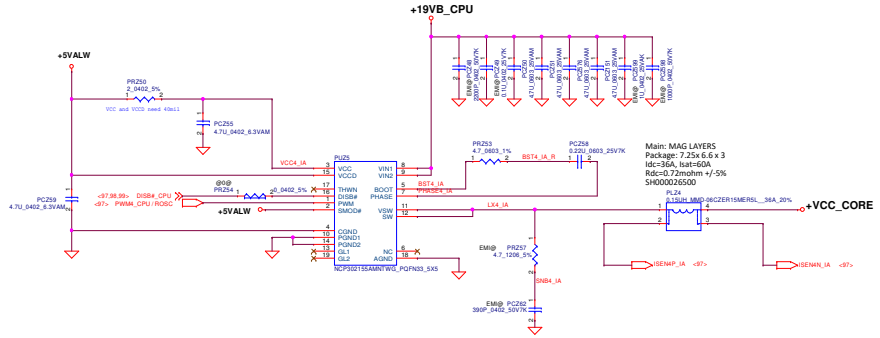
Main Func = +VCCCORE

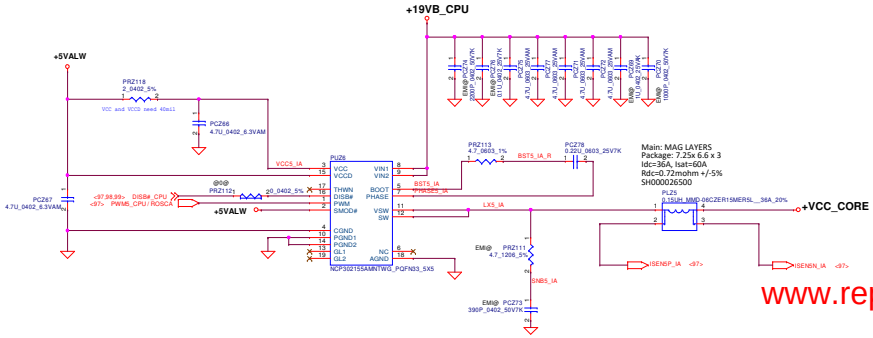
+VCCCORE
IPL2 = 93A
Peak Curren = 255A(ICCmax)
DC Load line: 2.3mohm
AC Load line: 2.3mohm
Current limit =329A(OCP)
FSW= 540K Hz











Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.			
Title	PWR +VCC_CORE		
Size	Document Number		Rev
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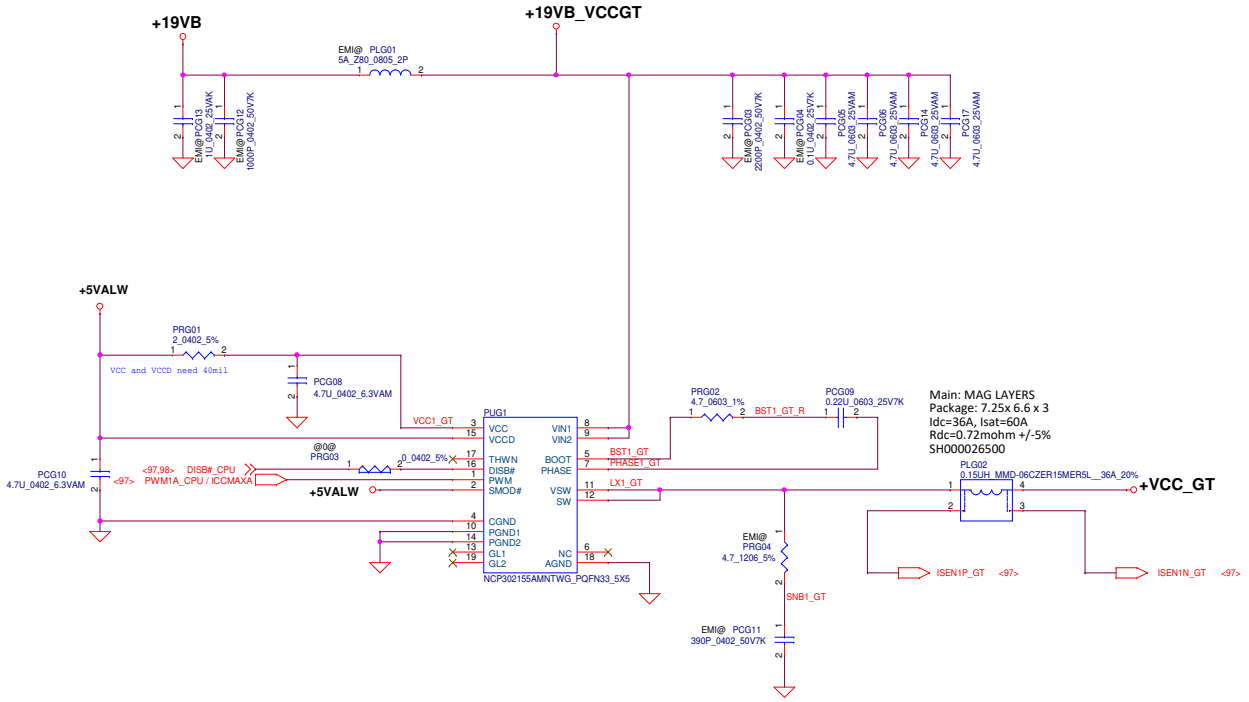
Date: Thursday, November 25, 2021	Sheet 98 of 120		

Main Func = +VCCGT

+VCCGT
IPL2 = 25A
Peak Curren = 40A(ICCmax)
DC Load line: 3.2mohm
AC Load line: 3.2ohm
Current limit =52A(OCP)
FSW= 540K Hz



Security Classification	Compal Secret Data		
Issued Date	2020/03/05	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR_+VCC_CORE

Size	Document Number	Rev
	LA-L613P	0.2

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_ Reserve for PWR

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Main Func = +VCCIN DECOUPLING

Intel ADL-P PDG Rev1.0
+VCC_CORE Output CAP :

CPU Primary Side:
330uF_D2 *3pcs
47uF_0603 *8 pcs

CPU Secondary side:
2.2uF_0402 *8pcs

Compal
+VCCCORE Output CAP :

CPU Primary Side:
330uF_D2 *2pcs
220uF_D7 *1pcs
22uF_0603_low-noise *18pcs

CPU Secondary side:
2.2uF_0402 *8pcs

Intel ADL-P PDG Rev1.0
+VCC_GT Output CAP :

CPU Primary Side:
330uF_D2 *2pcs
47uF_0603 *7 pcs
22uF_0402 *2 pcs

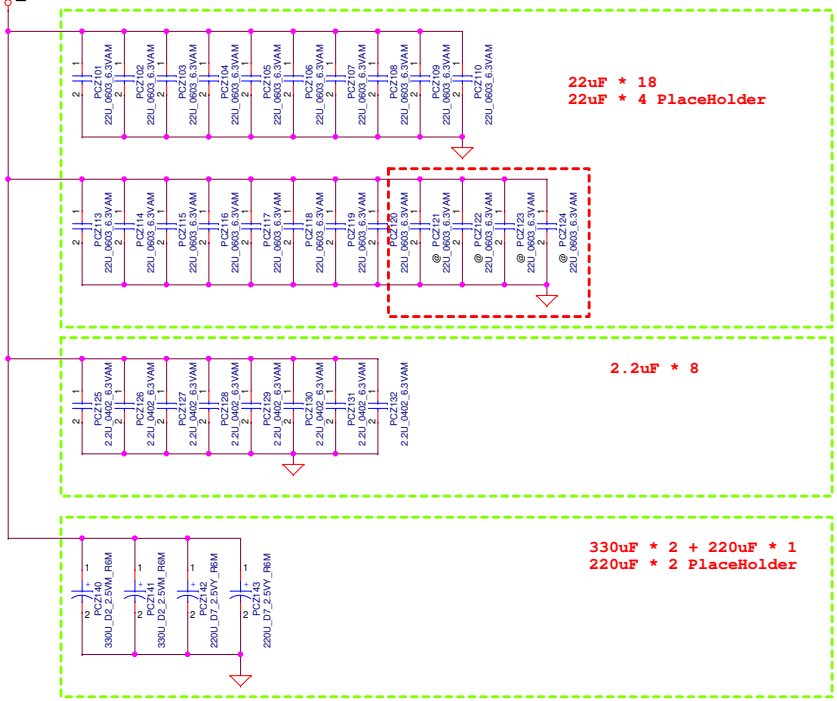
CPU Secondary side:
22uF_0402 *6pcs
10uF_0402 *2pcs

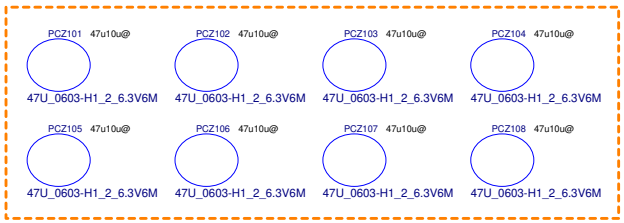
Compal
+VCCGT Output CAP :

CPU primary side:
330uF_B2 *3pcs
22uF_0603_low-noise *16pcs

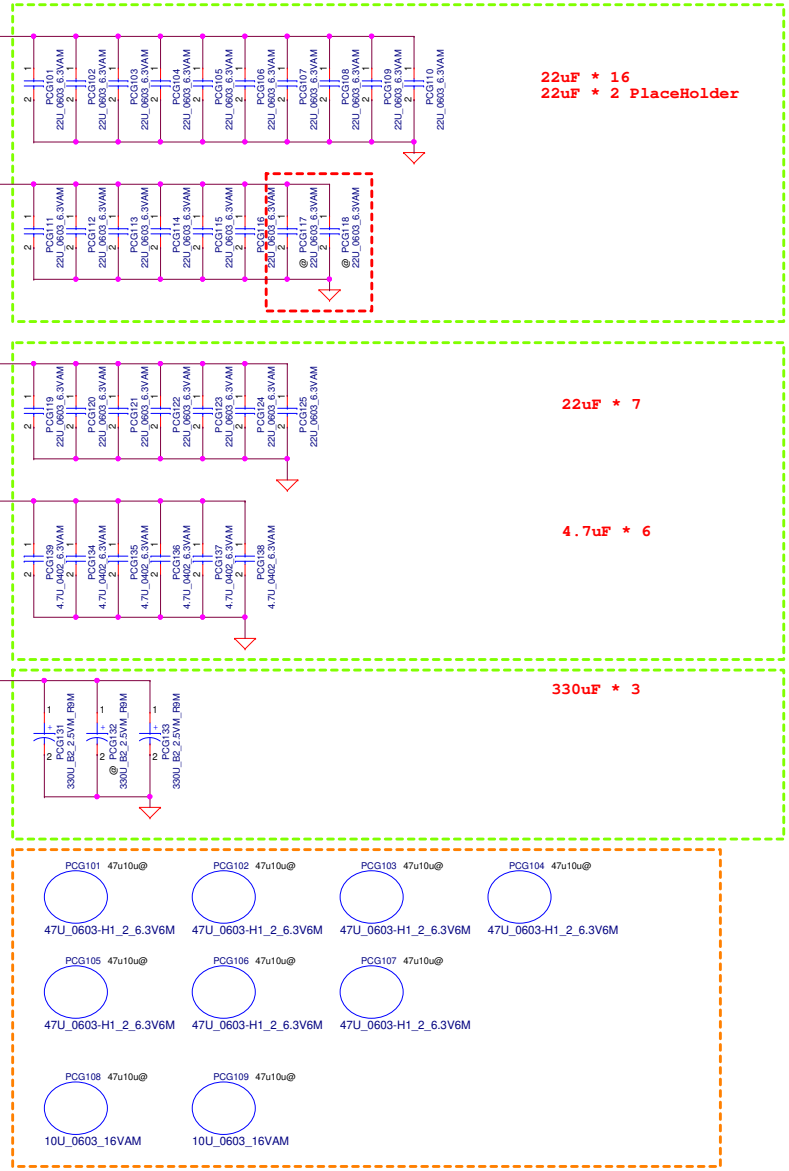
CPU Secondary side:
22uF_0603_low-noise *7pcs

+VCC_CORE





+VCC_GT



Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_CPU Decoupling CAP

Size | Document Number: LA-L613P | Rev: 0.1

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.		
Title: PWR_ Reserve for PWR		
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+NVVDD(GN20E3)
TDC 115A
Peak Current 300A
OCP 390A
Fsw 561k Hz

+NVVDD(GN20E6)
TDC 128A
Peak Current 277A
OCP 397.8A
Fsw 561k Hz

+NVVDD(GN20E8)
TDC 151A
Peak Current 336A
OCP 474.5A
Fsw 561k Hz

GPU	E3 MAX-P	E6 MAX-P	E8 MAX-P
EDP-P	300A	277A	336A
BOM sturcture	GN20E3@	GN20E6@	GN20E8@
PR1028	25.5K	25.5K	25.5K
PR1029	45.3K	46.4K	54.9K
PR1029(OCL)	30A	30.6A	36.5A
PR1037	316K	309K	261K
PR1037(OCP)	390A	397.8A	474.5A

Config	
Vmin	0.3
Vmax	1.3
Vboot	0.75
R1	6.19K
R2	20.5K
R3	2.8K
R4	13.7K
R5	0.274
C	4.7n

	Pull down R	
PWM1/PHTH4	NA	Function Disabled
PWM2/PHTH3	NA	Function Disabled
PWM3/PHTH2	NA	Function Disabled
PWM4/PHTH1	NA	Function Disabled
PWM5/LPC2	10K	CCM Mode
PWM6/LPC1	10K	CCM Mode
PWM7/I2C	26.1K	Address: 0x50
PWM8/SS	26.1K	0.6s

Place close to GPU pins

PU1000 NCP81610MNTXG_QFN40_5X5

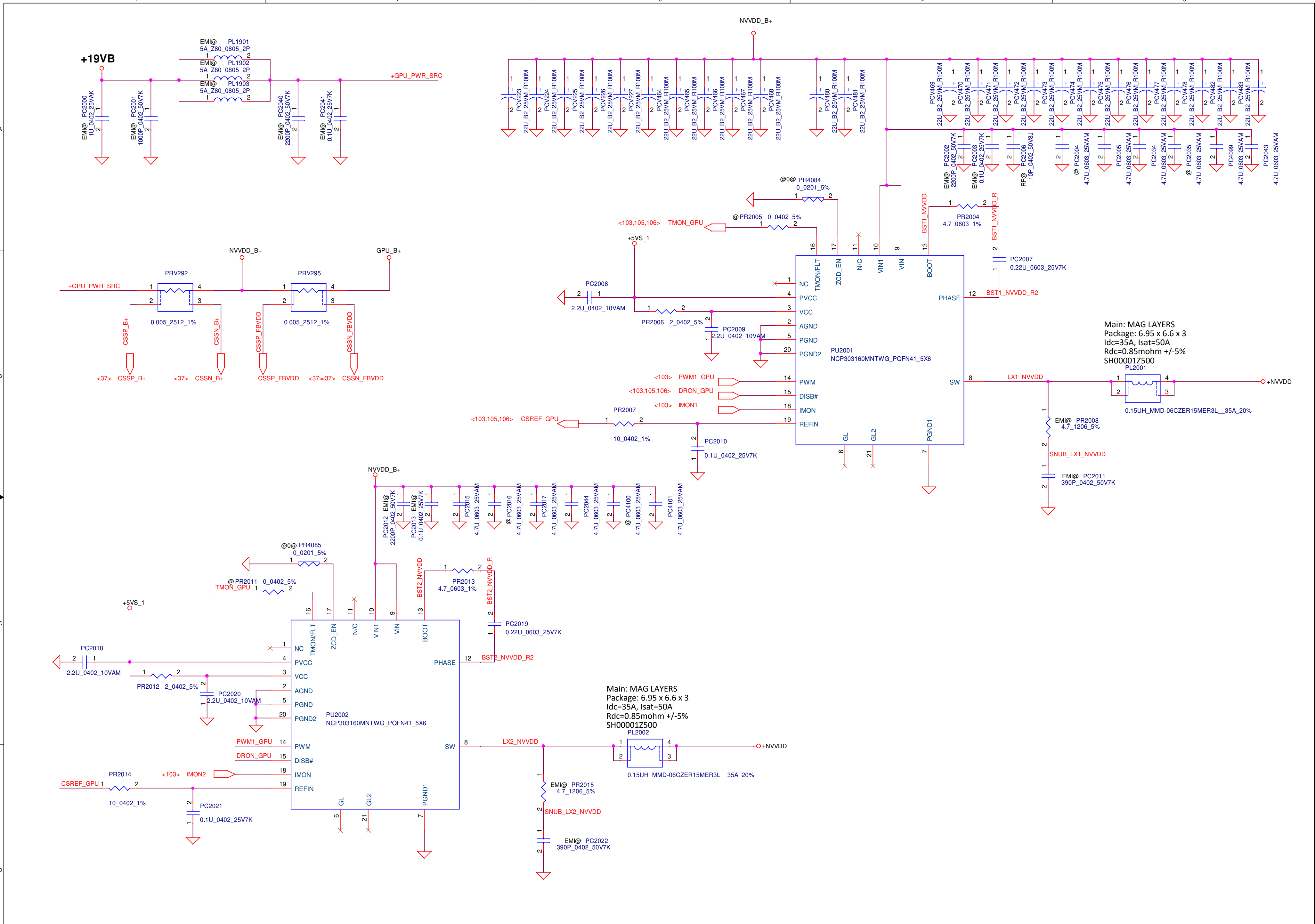
Security Classification	Compal Secret Data	
Issued Date	2020/02/27	Deciphered Date 2021/12/31

Compal Electronics, Inc.

Title: PWR_GPU_CORE IC-NCP81610

Size: | Document Number: LA-L613P | Rev: 0.1

Date: Thursday, November 25, 2021 | Sheet 103 of 121



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/02/27	Deciphered Date 2021/12/31	Title: PWR_GPU_CORE_SW1&2
			Size / Document Number: LA-L613P / Rev 0.1
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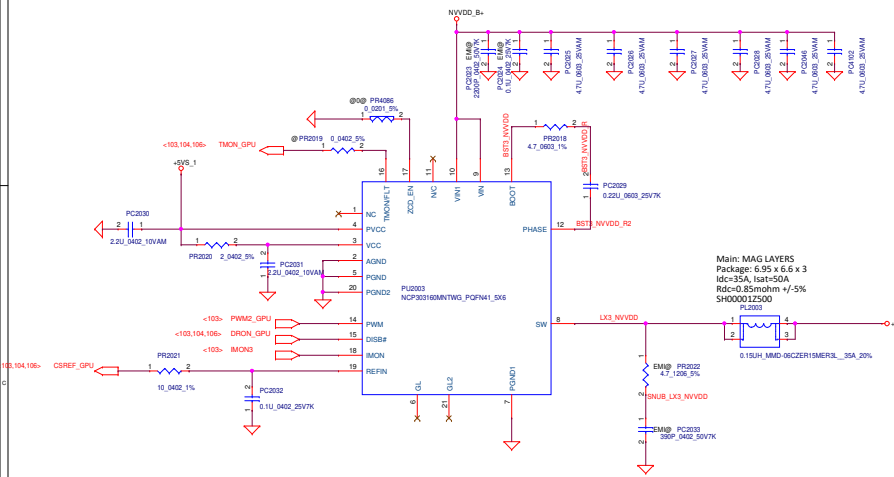
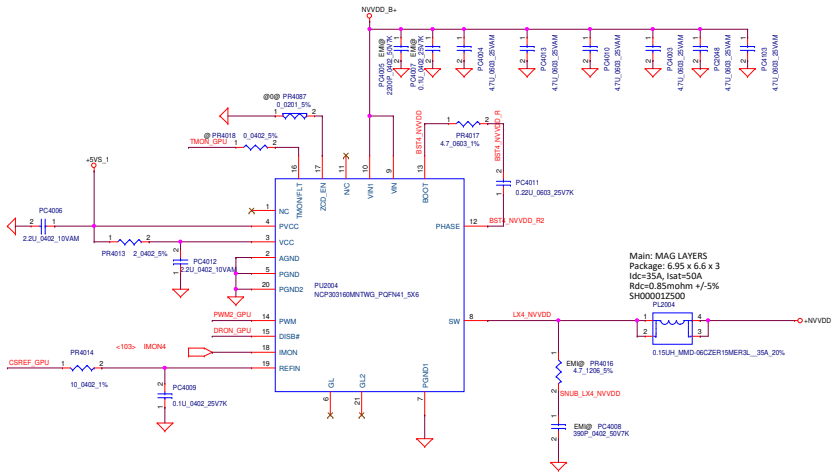
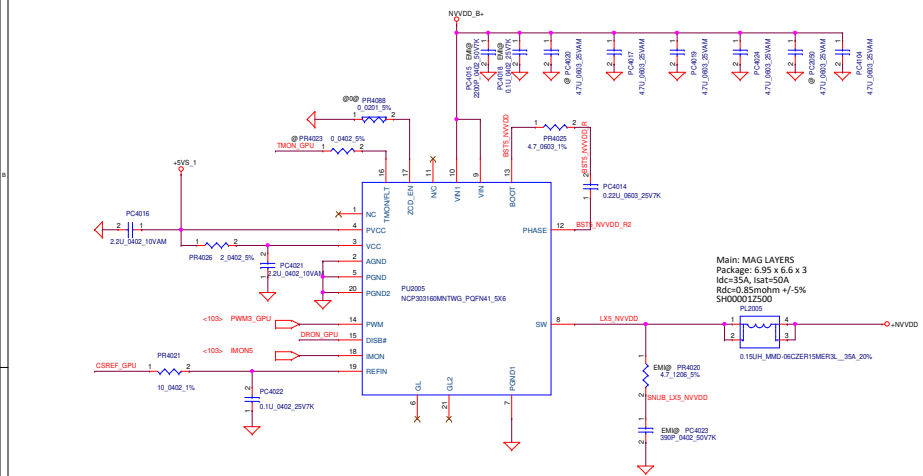
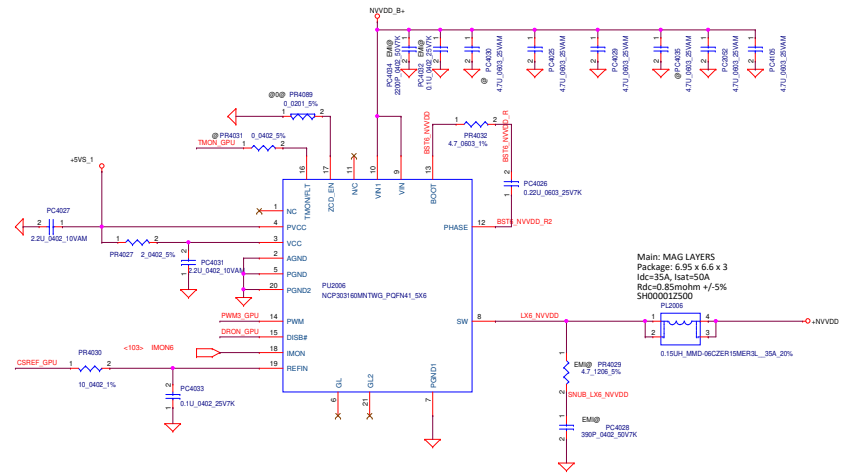


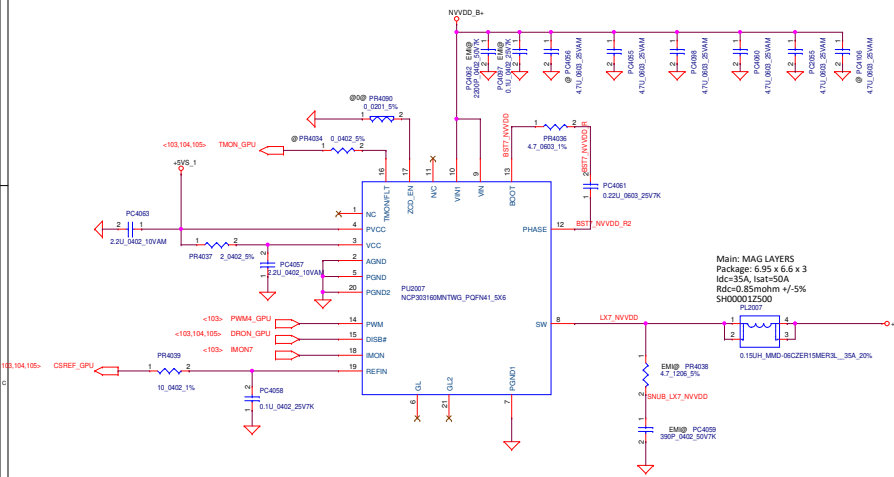


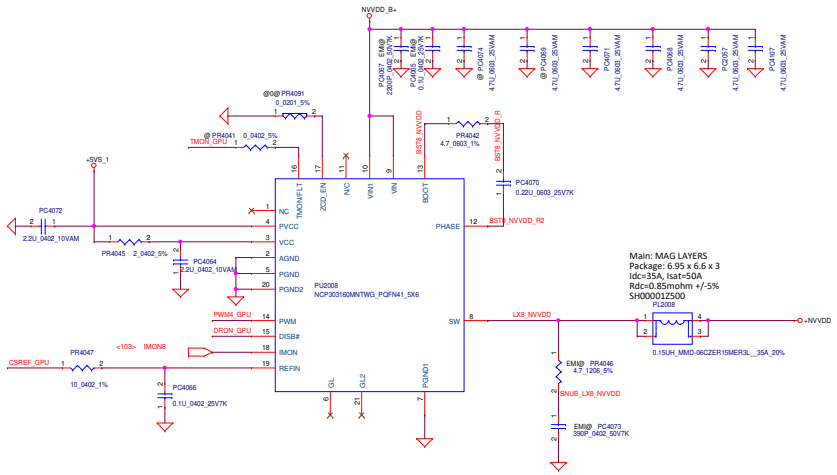


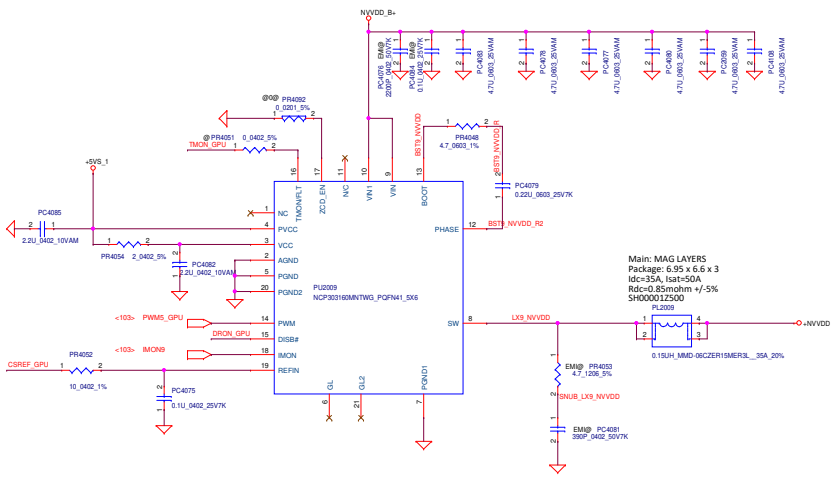


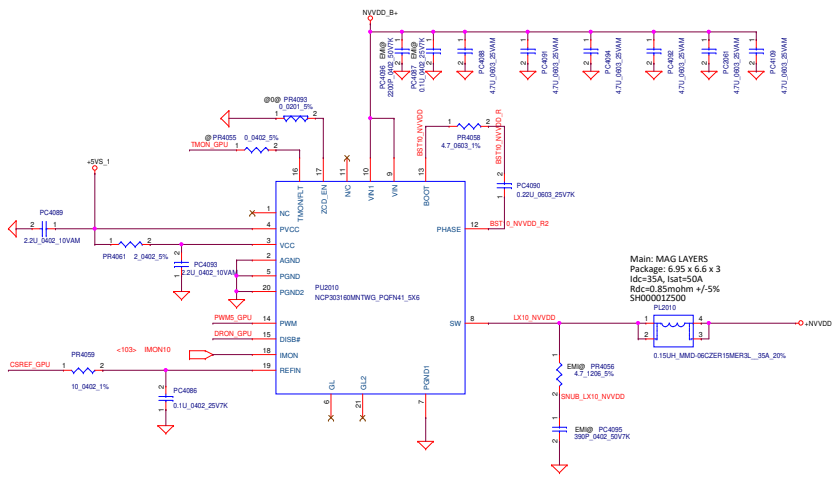
Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.			
Title	PWR_GPU_CORE_SW3-6		
Size	Document Number	LA-L613P	Rev 0.1
Date: Thursday, November 25, 2021	Sheet 105 of 121		









Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.			
Title	PWR_GPU_CORE_SW7-10		
Size	Document Number	LA-L613P	Rev 0.1
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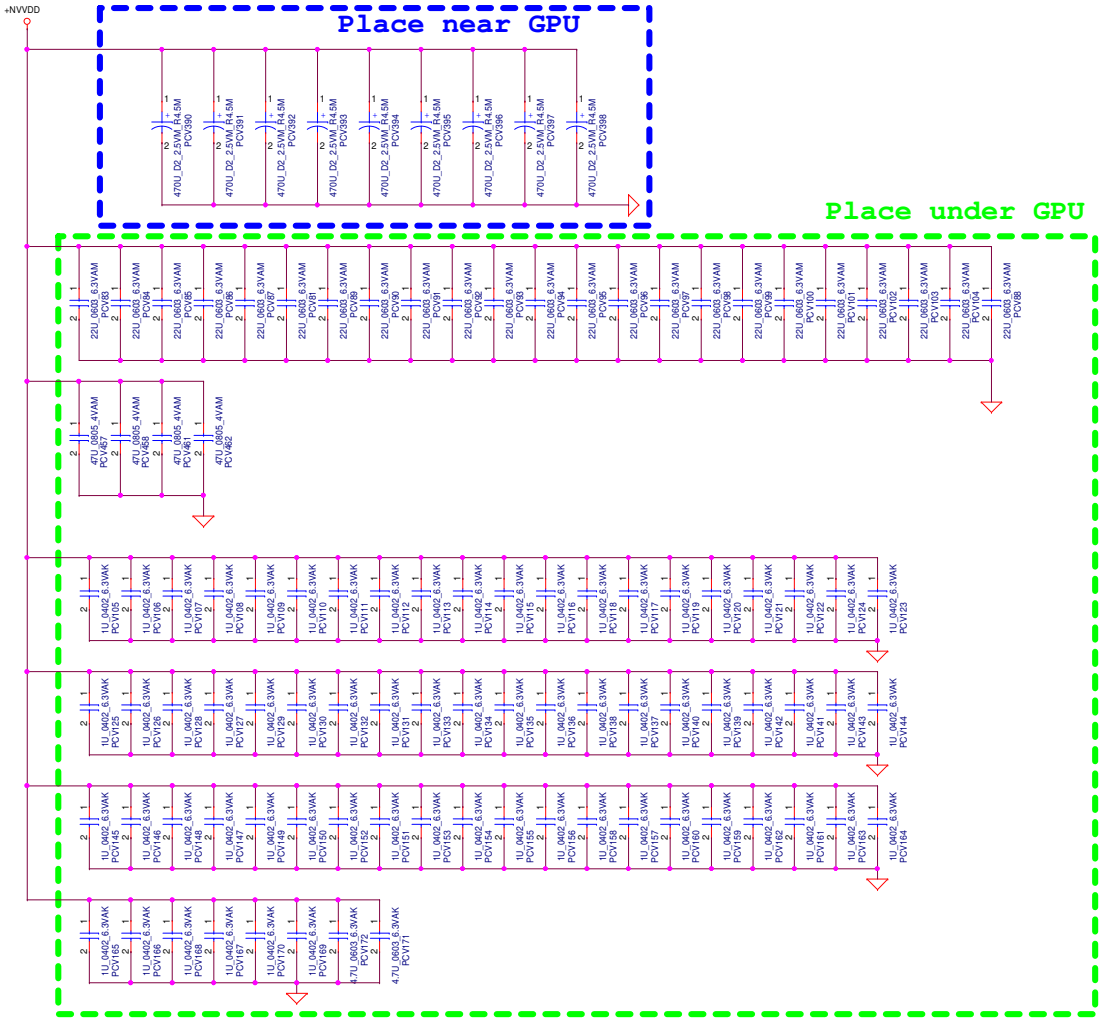

NV DG-09845-001_v07
NVVDD Output CAP :

Under GPU Side:
330uF *4pcs
47uF *7pcs
10uF *23pcs
4.7uF *2pcs
1uF *66pcs

Near GPU side:
Follow regulator vendor

Compal
NVVDD Output CAP :

Under GPU Side:
47uF *4pcs
22uF *23pcs
4.7uF *2pcs
1uF *66pcs

Near GPU side:
470uF*9pcs

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_GPU_DECOUPLING

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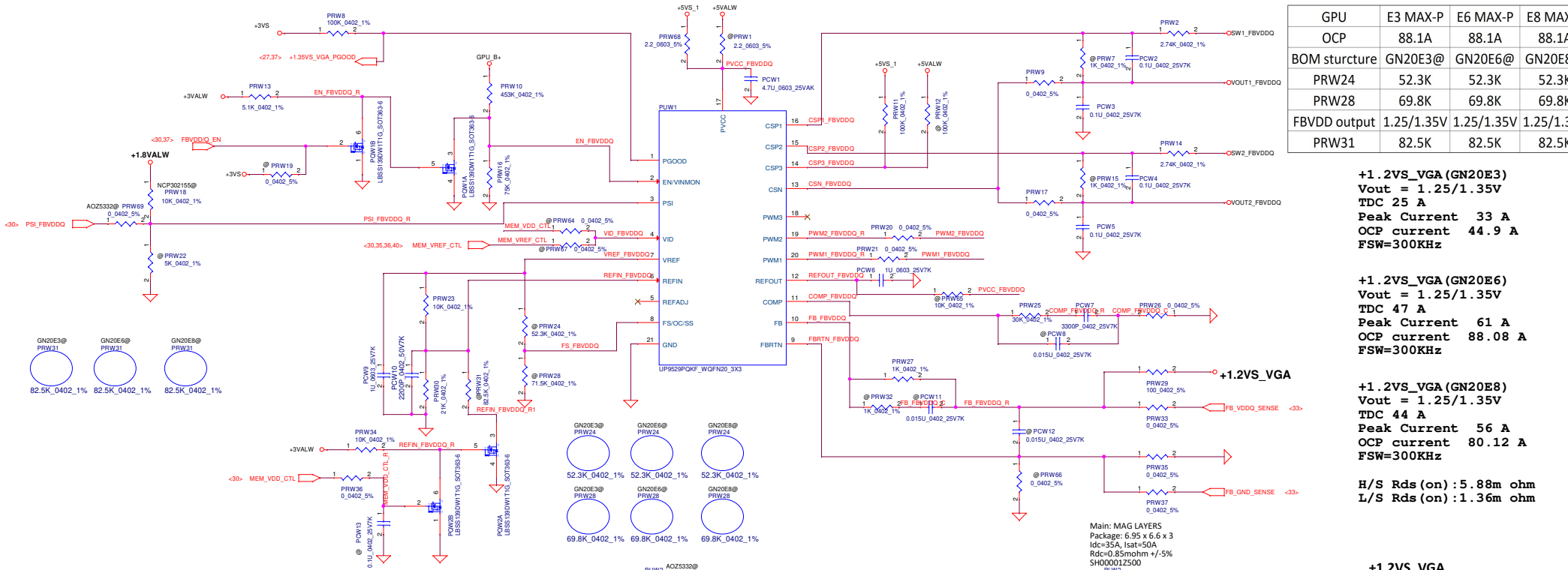
GPU	E3 MAX-P	E6 MAX-P	E8 MAX-P
OCP	88.1A	88.1A	88.1A
BOM sturcture	GN20E3@	GN20E6@	GN20E8@
PRW24	52.3K	52.3K	52.3K
PRW28	69.8K	69.8K	69.8K
FBVDD output	1.25/1.35V	1.25/1.35V	1.25/1.35V
PRW31	82.5K	82.5K	82.5K

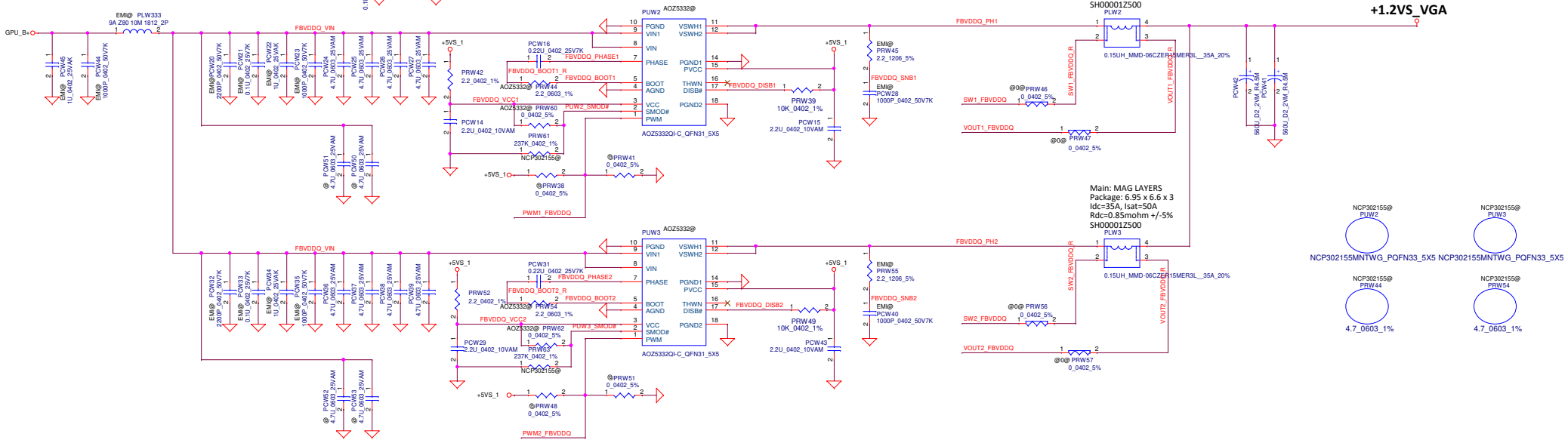
+1.2VS_VGA(GN20E3)
Vout = 1.25/1.35V
TDC 25 A
Peak Current 33 A
OCP current 44.9 A
FSW=300KHz

+1.2VS_VGA(GN20E6)
Vout = 1.25/1.35V
TDC 47 A
Peak Current 61 A
OCP current 88.08 A
FSW=300KHz

+1.2VS_VGA(GN20E8)
Vout = 1.25/1.35V
TDC 44 A
Peak Current 56 A
OCP current 80.12 A
FSW=300KHz

H/S Rds(on):5.88m ohm
L/S Rds(on):1.36m ohm





Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.

Title: PWR_GPU_VRAM

Size | Document Number: LA-L613P | Rev: 0.1

Date: Thursday, November 25, 2021 | Sheet 108 of 121

Reserve

Security Classification	Compal Secret Data		
Issued Date	2020/02/27	Deciphered Date	2021/12/31

Compal Electronics, Inc.		
Title: PWR_ Reserve for PWR		
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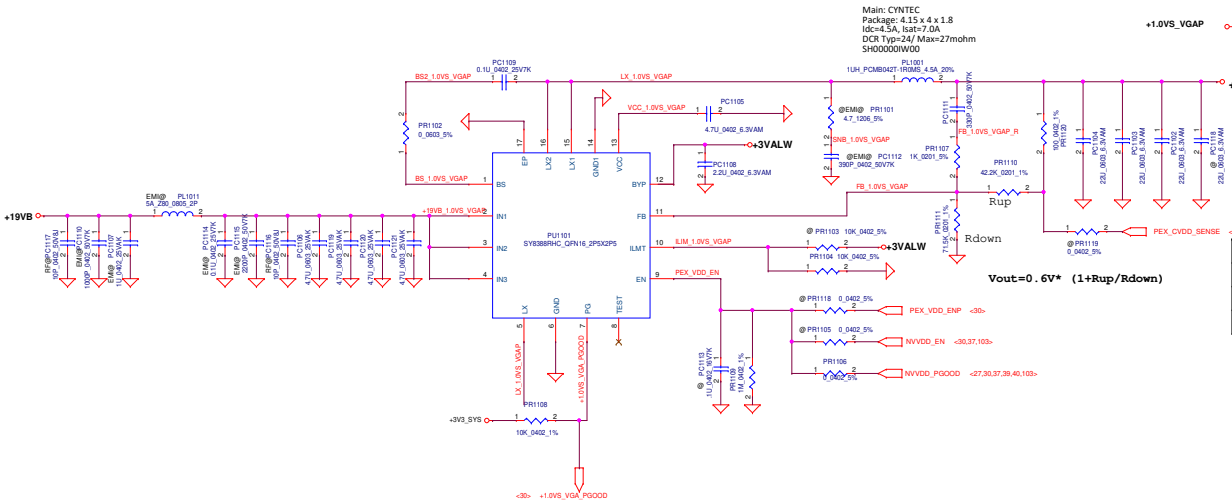
Date: Thursday, November 25, 2021	Sheet 109 of 121	

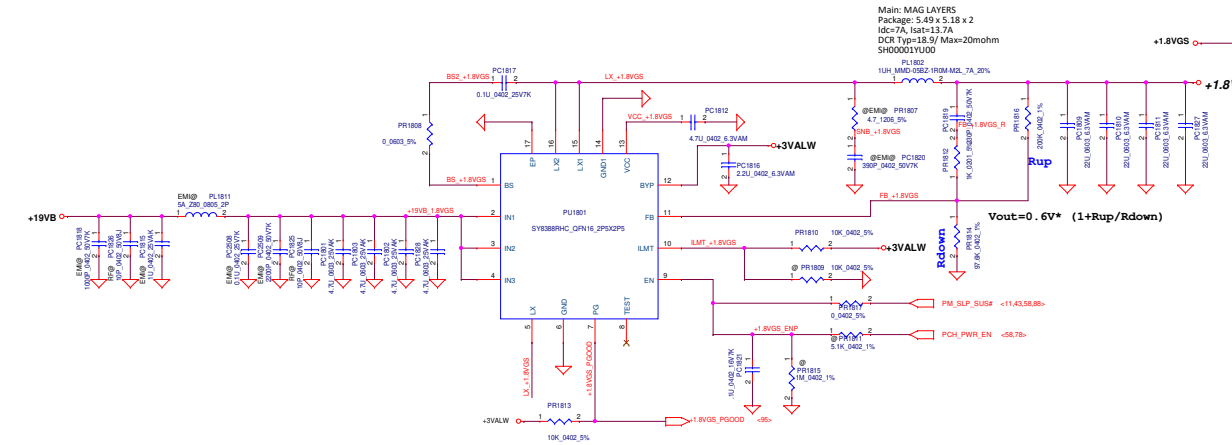


+1.0VS_VGAP

Vout=0.95V
TDC=3.32A (2.1+0.305*4=3.32)
Peak Current 5.32A (4.1+0.305*4=5.32)
OCP current 8A
FSW=500KHz

	TYP	MAX
Choke DCR	24mohm ,	27mohm

Output current limit threshold selection		
Low	8A	V
Floating	10A	
High	12A	



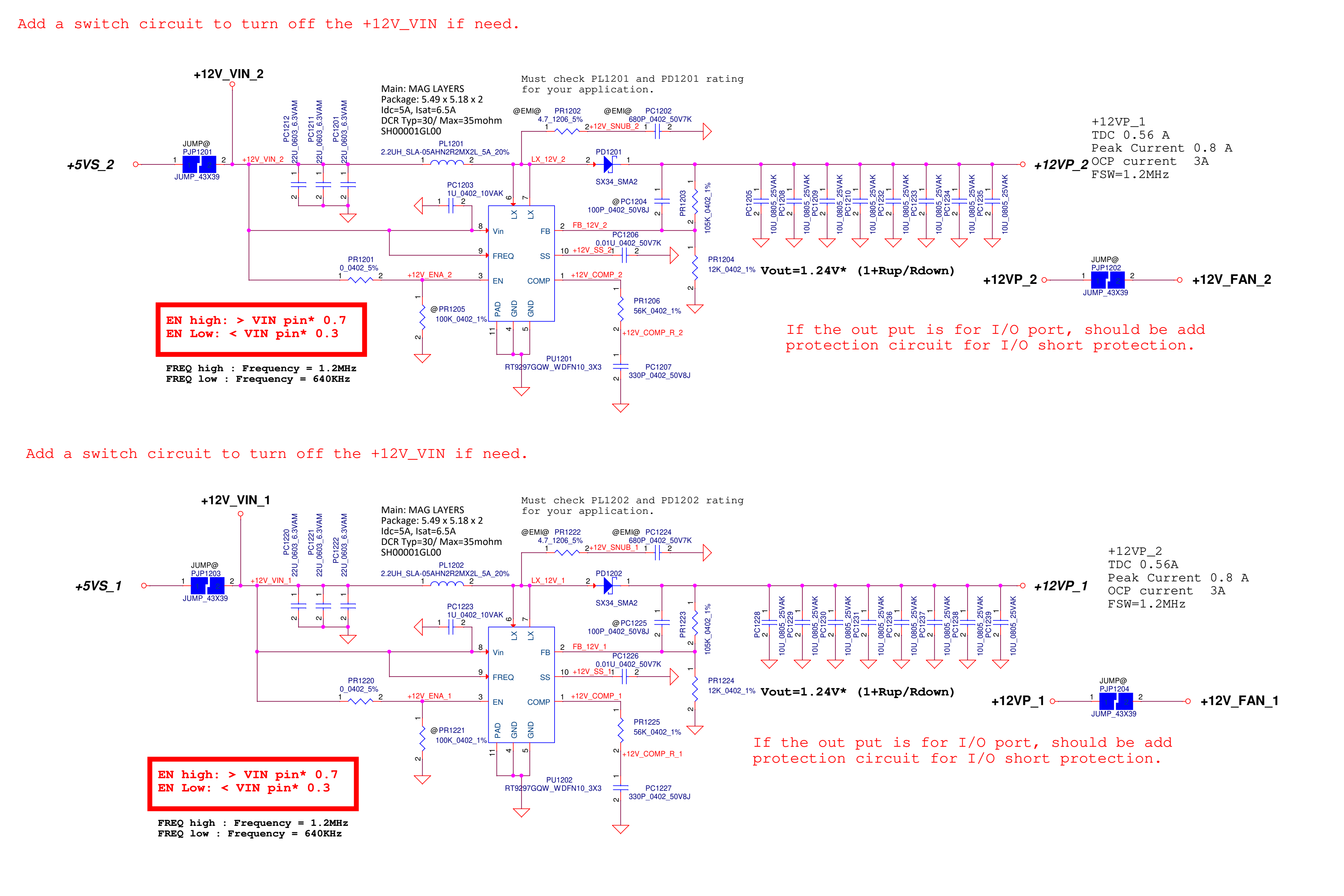
+1.8VGS

+1.8VGS
TDC 5.92 A (3.145*0.7+2.4+0.33*4)
Peak Current 9.37 A (3.145+4.9+0.33*4)
OCP current 12A
FSW=500kHz

	TYP	MAX
Choke DCR	18.9mohm ,	20mohm

Output current limit threshold selection		
Low	8A	
Floating	10A	
High	12A	V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2020/02/27	Deciphered Date 2021/12/31	Title: PWR_GPU_PEXVDD/1.8VGS
			Size: Document Number: LA-L613P Rev: 0.1
			Date: Thursday, November 25, 2021 Sheet 110 of 121



Add a switch circuit to turn off the +12V_VIN if need.
+12V_VIN_2
Main: MAG LAYERS
Package: 5.49 x 5.18 x 2
Idc=5A, Isat=6.5A
DCR Typ=30/ Max=35mohm
SH00001GL00
Must check PL1201 and PD1201 rating for your application.
+5VS_2
JUMP@ PJP1201 JUMP_43X39
+12V_VIN_2
PC1212 22U_0603_6.3VAM
PC1211 22U_0603_6.3VAM
PC1201 22U_0603_6.3VAM
PL1201 2.2UH_SLA-05AHN2R2MX2L_5A_20%
@EMI@ PR1202 4.7_1206_5%
+12V_SNUB_2
@EMI@ PC1202 680P_0402_50V7K
LX_12V_2
PD1201 SX34_SMA2
+12VP_2
PC1203 1U_0402_10VAK
@PC1204 100P_0402_50V8J
PR1203 105K_0402_1%
PC1205 10U_0805_25VAK
PC1208 10U_0805_25VAK
PC1209 10U_0805_25VAK
PC1210 10U_0805_25VAK
PC1232 10U_0805_25VAK
PC1233 10U_0805_25VAK
PC1234 10U_0805_25VAK
PC1235 10U_0805_25VAK
Vin FB FREQ SS EN COMP LX LX PAD GND GND
FB_12V_2
PC1206 0.01U_0402_50V7K
+12V_SS_2
PR1201 0_0402_5%
+12V_ENA_2
+12V_COMP_2
PR1204 12K_0402_1%
Vout=1.24V* (1+Rup/Rdown)
@PR1205 100K_0402_1%
PR1206 56K_0402_1%
+12V_COMP_R_2
PU1201 RT9297GQW_WDFN10_3X3
PC1207 330P_0402_50V8J
EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3
FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz
+12VP_1
TDC 0.56 A
Peak Current 0.8 A
OCP current 3A
FSW=1.2MHz
+12VP_2
JUMP@ PJP1202 JUMP_43X39
+12V_FAN_2
If the out put is for I/O port, should be add protection circuit for I/O short protection.
Add a switch circuit to turn off the +12V_VIN if need.
+12V_VIN_1
Main: MAG LAYERS
Package: 5.49 x 5.18 x 2
Idc=5A, Isat=6.5A
DCR Typ=30/ Max=35mohm
SH00001GL00
Must check PL1202 and PD1202 rating for your application.
+5VS_1
JUMP@ PJP1203 JUMP_43X39
+12V_VIN_1
PC1220 22U_0603_6.3VAM
PC1221 22U_0603_6.3VAM
PC1222 22U_0603_6.3VAM
PL1202 2.2UH_SLA-05AHN2R2MX2L_5A_20%
@EMI@ PR1222 4.7_1206_5%
+12V_SNUB_1
@EMI@ PC1224 680P_0402_50V7K
LX_12V_1
PD1202 SX34_SMA2
+12VP_1
PC1223 1U_0402_10VAK
@PC1225 100P_0402_50V8J
PR1223 105K_0402_1%
PC1228 10U_0805_25VAK
PC1229 10U_0805_25VAK
PC1230 10U_0805_25VAK
PC1231 10U_0805_25VAK
PC1236 10U_0805_25VAK
PC1237 10U_0805_25VAK
PC1238 10U_0805_25VAK
PC1239 10U_0805_25VAK
FB_12V_1
PC1226 0.01U_0402_50V7K
+12V_SS_1
PR1220 0_0402_5%
+12V_ENA_1
+12V_COMP_1
PR1224 12K_0402_1%
Vout=1.24V* (1+Rup/Rdown)
@PR1221 100K_0402_1%
PR1225 56K_0402_1%
+12V_COMP_R_1
PU1202 RT9297GQW_WDFN10_3X3
PC1227 330P_0402_50V8J
EN high: > VIN pin* 0.7
EN Low: < VIN pin* 0.3
FREQ high : Frequency = 1.2MHz
FREQ low : Frequency = 640KHz
+12VP_2
TDC 0.56A
Peak Current 0.8 A
OCP current 3A
FSW=1.2MHz
+12VP_1
JUMP@ PJP1204 JUMP_43X39
+12V_FAN_1
If the out put is for I/O port, should be add protection circuit for I/O short protection.

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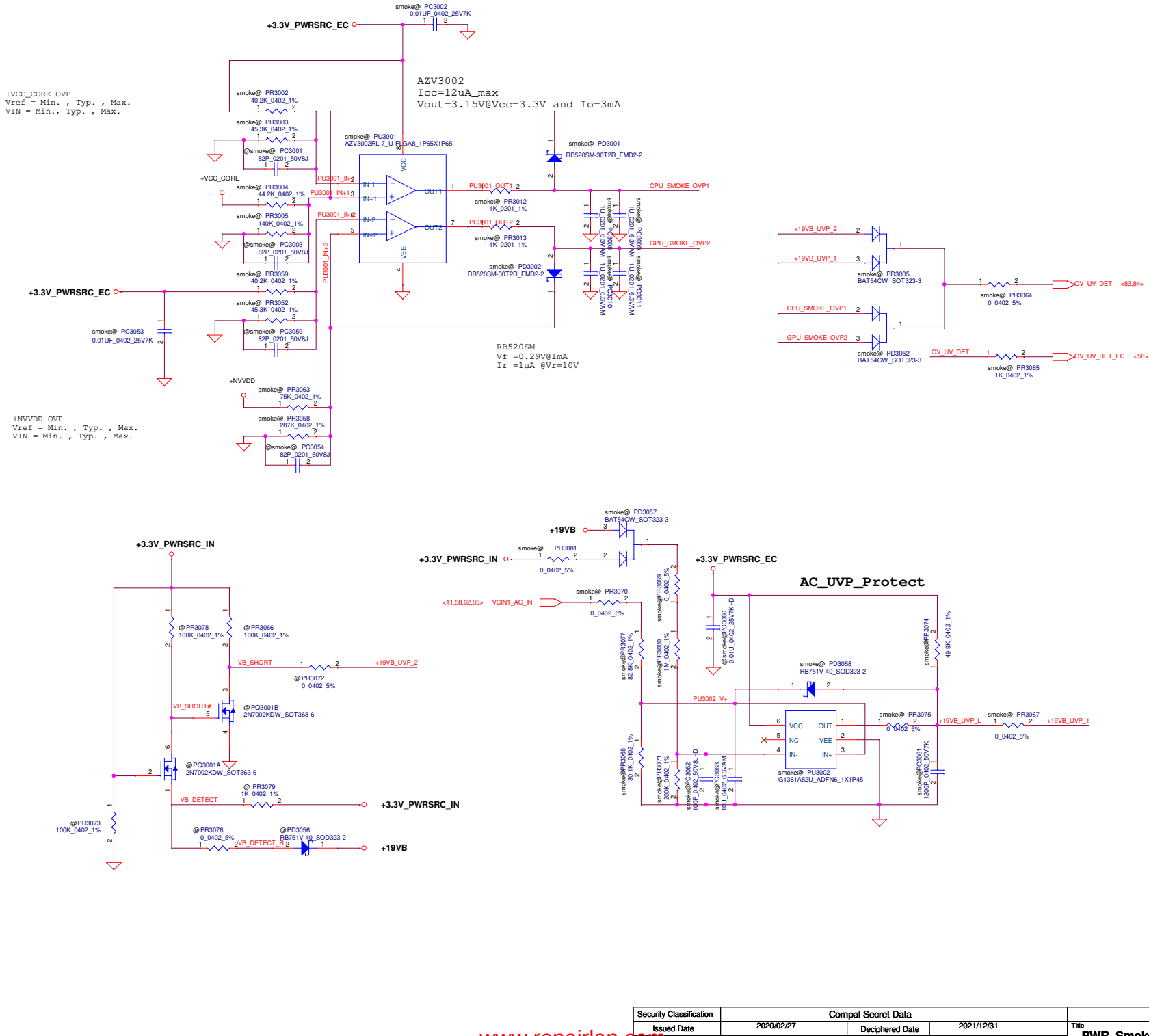

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Reserve

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Compal Electronics, Inc.

Title: *PWR_ Reserve for PWR*

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	108	GPU_VRAM_PW	2021/06/17	PWR	UP9529 change pull high net of CSP3_FBVDDQ from +5VALW to +5VS_1	Pop PRW11, unpop PRW12	0.1
2	95	+VCCIN_AUX (NCP81270)_PW	2021/06/17	PWR	MLCC downsize	Change PCA3 from SE071150J80(0402) to SE00000TD00(0201)	0.1
3	97	P097_+VCORE IC(NCP81521)_PW	2021/06/17	PWR	Setting PSYS resistor meet system request	Change PRZ03 from SD034205280(20.5k) to SD000003580(19.6k)	0.1
4	83	2 Type-C PD Selector_PW	2021/06/17	PWR	Random cannot power on,UE5 VCC0 voltage cannot meet spec.	Change PDS19,PDS20,PDS21 from SCS00000Z00 to SCS00005800. Pop PDS20.	0.1
5	111	+12VP_PW	2021/06/17	PWR	Enable setting no timing contronl change to 0 ohm	Change PR1220,PR1201 from SD034402280(40.2K) to SD028000080(0 ohm)	0.1
6	84	DCIN/Back to back_PW	2021/06/17	PWR	Avoid mis trigger smokeless when BARREL_DCIN_EN# high on DC mode Swap AC_DIS and BARREL_DCIN_EN# net	Change net of BARREL_DCIN_EN# from PDS07.2 to PQ9.2 Change net of AC_DIS from PQ9.2 to PDS07.2	0.1
7	98	+VCCCORE_SW_PW	2021/06/17	PWR	0603 resistor used common parts	Change PRZ52,PRZ53,PRZ44,PRZ45,PRZ113 from SD00001RD00(1/5W) to SD000006T80(1/10W)	0.1
8	99	+VCCGT_SW_PW	2021/06/17	PWR	0603 resistor used common parts	Change PRG02 from SD00001RD00(1/5W) to SD000006T80(1/10W)	0.1
9	108	GPU_VRAM_PW	2021/06/23	PWR	Reserve for thermal derating	Add unpop PCW50,PCW51,PCW52,PCW53 (SE00001JB00)	0.1
10	108	GPU_VRAM_PW	2021/06/23	PWR	Down downgrade plane change from X7R to X6S	PCW1 change form SE00001PGM0(2.2uF/25V/0603/X7S) to SE00001CJ00(4.7uF/25V/0603/X6S)	0.1
11	108	GPU_VRAM_PW	2021/06/24	PWR	Jitter is too much during testing	PCW3,PCW5 change form SE075153K80(0.015uF) to SE00000W210(0.1uF) PRW2,PRW14 change form SD00000JB80(1.69k) to SD034274180(2.74k)	0.1
12	103	GPU_CORE IC-NCP81610_PW	2021/06/25	PWR	NV request GPU I2C net	Add PRV497,PRV498 0ohm for EC_SMB_DA2/EC_SMB_CK2. Change PRV495,PRV496 uppop for reserved SDA_GPU/ SCL_GPU.	0.1
13	97	+VCORE IC(NCP81521)_PW	2021/06/25	PWR	Solve step drop issue	Change IMVP_VR_ON net name to EN_CPU. Change EN_CPU net name to EN_CPU_VR.	0.1
14	95	+VCCIN_AUX (NCP81270)_PW	2021/06/28	PWR	NCP81270 real test adjust by VRTT	Change PRA27 form SD034113380(113k) to SD034910280(91k) for AUX Iout gain setting.	0.1
15	97	+VCORE IC(NCP81521)_PW	2021/06/28	PWR	NCP81521 real test adjust by VRTT	PRZ102 changed to 71.5k for ICC*2_MAIN_RAIL turn on PRZ103 changed to 31.6k for GT Iout gain setting PCZ167 changed to 150p for GT CSCOMPA/CSSUMA compensate adjust PRZ04 changed to 127k for Iccmax resistance setting PCZ08 changed to 150p for IA CSS/SR compensate adjust PRZ16 changed to 178k for GT CSS/SR compensate adjust PRZ34 changed to 29.4k for IA Iout gain setting PRZ09 changed to 4.75k for IA VCC/SS compensate adjust	0.1
16	83	2 Type-C PD Selector_PW	2021/06/28	PWR	Reserve LDO co-lay circuit	Reserve co-lay circuit for 2nd RT9069 LDO PRS973,PRS974 add 0 ohm 0402 SA0000ES010(AP2205@),SA00008AU00(RT9069@) BOM change	0.1

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	97	+VCORE IC(NCP81521)_PW	2021/06/17	PWR	Down downgrade plane change from X7R to X6S	Change PCZ11,PCZ14 form SE00001MT00(X7R) to SE000013J00(X6S)	0.1
18	83	2 Type-C PD Selector_PW	2021/06/17	PWR	Unify material	Change PDS08,PDS16,PDS17,PDS10 SCS00002G00 to SCS00000Z00.	0.1
19	84	DCIN/Back to back_PW	2021/06/17	PWR	Unify material	Change PDS09,PDS07 SCS00002G00 to SCS00000Z00.	0.1
20	101	CPU Decoupling CAP_PW	2021/07/06	PWR	Follow vender modification for +VCCGT power solution	Unpop PCG132.	0.1
21	88	+5VALWP_2_PW	2021/07/02	PWR	DDR5 PMIC leakage issue	Change PR515 form SD028300380(300k) to SD028000080(0ohm) pop Uppop PR510 Pop PR511,PR512,PR514	0.1
22	84	DCIN/Back to back_PW	2021/07/08	PWR	The manufacturer does not provide	Change PQ3211 form SB00001SM00 to SB00001SN00	0.1
23	96	+VCCIN_AUX DECOUPLING_PW	2021/07/08	PWR	PI simulation VCC_AUX fail on 2.5MHz~5MHz	Add PCA117,PCA116,PCA118,PCA119 (SE00001BY00)	0.1
24	101	CPU Decoupling CAP_PW	2021/07/08	PWR	PI simulation VCC_GT fail on 1.5MHz~4MHz	Add PCG139,PCG134,PCG135,PCG136,PCG137,PCG138 (SE00001BY00)	0.1
25	88	+5VALWP_2_PW	2021/07/12	PWR	Reserved 0ohm for PM_SLP_S4#	Uppop PR516(0ohm) SD028000080	0.1
26	97	+VCORE IC(NCP81521)_PW	2021/08/16	PWR	VCORE H_PROCHOT#	Pop PRZ15 for H_PROCHOT#	0.2
27	103	GPU_CORE IC-NCP81610_PW	2021/08/16	PWR	For GN20-E5 change GN20-E6, GN20-E7 change GN20-E8 OCL/OCP design	Bom Structure (GN20E5@) PR1028,PR1029,PR1037 change (GN20E6@) PR1028,PR1029,PR1037 Bom Structure (GN20E7@) PR1028,PR1029,PR1037 change (GN20E8@) PR1028,PR1029,PR1037 (GN20E6@) PR1029 change SD000009K00 to SD000009R00 (GN20E6@) PR1037 change SD00000WW00 to SD034309380 (GN20E8@) PR1029 change SD034432280 to SD00000H880 (GN20E8@) PR1037 change SD034332380 to SD034261380	0.2
28	108	GPU_VRAM_PW	2021/08/16	PWR	For GN20-E5 change GN20-E6, GN20-E7 change GN20-E8 OCL/OCP design	Bom Structure (GN20E5@) PRW24,PRW28 change (GN20E6@) PRW24,PRW28 Bom Structure (GN20E7@) PRW24,PRW28 change (GN20E8@) PRW24,PRW28 (GN20E6@) PRW24 change SD034511280 to SD034523280 (GN20E6@) PRW28 change SD034715280 to SD034698280 (GN20E8@) PRW24 change SD034499280 to SD034523280 (GN20E8@) PRW28 change SD034750280 to SD00000B180 PRW31 unpop by BOM control Add (GN20E3@) PRW31(SD000002780) Add (GN20E6@) PRW31,(GN20E8@) PRW31 (SD00000H880)	0.2
29	85	CHARGER-ISL9241_PW	2021/08/17	PWR	DVT1.1 change, incomplete substitute with EE, main and 3rd swap	PUB3 Change from SA00001DG90 to SA0000BJI00.	0.2
30	97	+VCORE IC(NCP81521)_PW	2021/08/17	PWR	Follow vender modification for NCP815221 PD0 power solution	PRZ74,PRZ14,PRZ20,PRZ18,PRZ116 change from 80.6K(SD014806280) to 150K(SD014150380) PRZ34 change from 29.4K(SD034294280) to 35.7K(SD000007D00) PRZ77 change from 64.9K(SD034649280) to 41.2K(SD000009K00) PUZ01 NCP81521 change from PC0(SA0000ELJ10) to PD0(SA0000ELJ20)	0.2
31	112	Smokeless UVP/OVP_PW	2021/08/24	PWR	OCP/UVP design change	PR3071 change 464K(SD034464380) to 200K(SD034200380) PR3068 change 93.1K(SD034931280) to 30.1K(SD034301280) PR3005 change 196K(SD034196380) to 140K(SD034140380)	0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
32	88	+5VALWP_2_PW	2021/08/31	PWR	Reserved 0ohm for SYSON	Uppop PR517(0ohm) SD028000080	0.3
33	97	+VCORE IC(NCP81521)_PW	2021/09/02	PWR	Net mane different, Unify net mane	PUZ01.27 net mane change from PWM1A / ICCMAXA to PWM1A_CPU / ICCMAXA PUG01.1 net mane change from PWM1A / ICCMAXA to PWM1A_CPU / ICCMAXA	0.3
34	89	DDR(RT8231B)_PW	2021/09/11	PWR	For RF Layout Modify	Add PCM27,PCM28,PCM29 (SE00000TD00)	0.3
35	96	+VCCIN_AUX DECOUPLING_PW	2021/09/11	PWR	For RF Layout Modify	Add PCA120,PCA121,PCA122 (SE00000TD00)	0.3
36	108	GPU_VRAM_PW	2021/09/14	PWR	AOZ5332 footprint modify	Delete PUW2,PUW3 pin2 pin13	0.3
37	108	GPU_VRAM_PW	2021/09/27	PWR	Lack of material, change to 2nd source parts	PCW16,PCW31 change SE00001MT00 to SE00001MTM0	0.3
38	108	GPU_VRAM_PW	2021/09/27	PWR	For GN20-E6, GN20-E8 Memory specifications	E6, Vout=1.25/1.35V, PRW31 change 54.9Kohm(SD00000H880) to 82.5Kohm(SD000002780) E8, Vout=1.25/1.35V, PRW31 change 54.9Kohm(SD00000H880) to 82.5Kohm(SD000002780)	0.3
39	108	GPU_VRAM_PW	2021/11/15	PWR	VRAM GN20-E3, GN20-E8 OCL setting follow GN20-E6 specifications	(GN20E3@)PRW24 change 47.5Kohm(SD034475280) to 52.3Kohm(SD034523280) (GN20E3@)PRW28 change 82.5Kohm(SD000002780) to 69.8Kohm(SD034698280) (GN20E8@)PRW28 change 82.5Kohm(SD000002780) to 69.8Kohm(SD034698280)	0.4
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