COMPAL CONFIDENTIAL

MODEL NAME :CDM80

PCB NO : LA-E092P

BOM P/N :

BR15 KBL-U DSC

Kabylake U

2016-11-07

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DA80018J000	PCB 1S4 LA-E092P REV0 MB DSC 1

Layout Dell logo

REV:X00
PWB: 93K47

Compal Electronics, Inc.

Title: Cover Sheet

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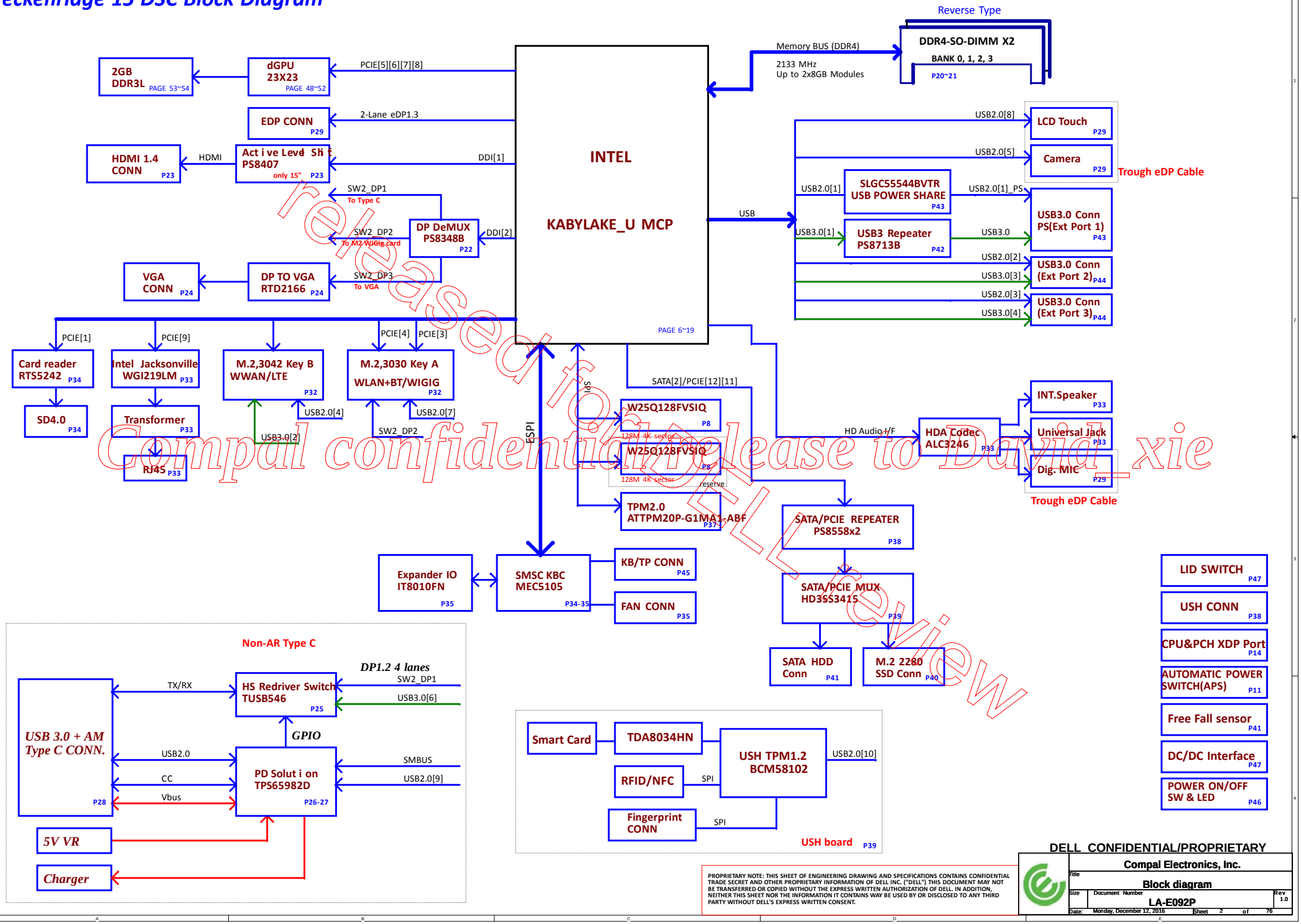
Breckenridge 15 DSC Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane \ State			
	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

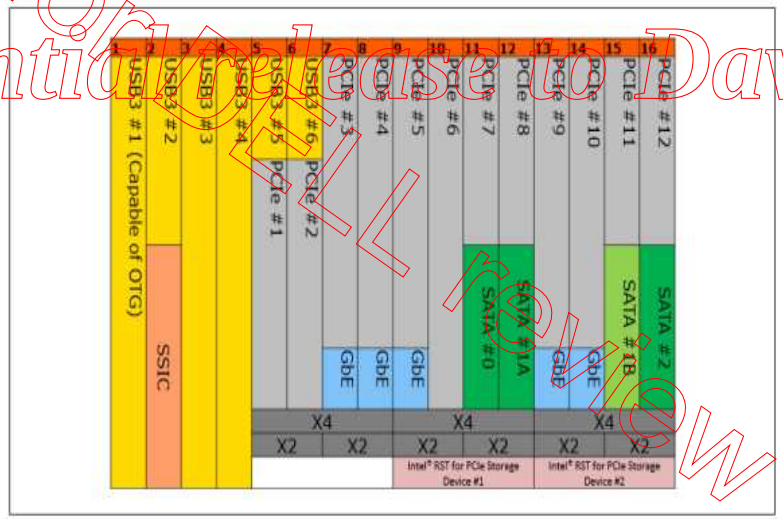
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1086	2.65
2	GND1		Copper foil	1oz	1.25
		3.8	Core	3mil	3.00
3	Sig 1		Copper foil	1oz	1.25
		3.7	Prepreg	7628+1080	10.95
4	GND/PWR		Copper foil	1oz	1.25
		3.8	Core	3mil	3.00
5	Sig2		Copper foil	1oz	1.25
		3.8	Prepreg	7628+1080	10.28
6	Sig3		Copper foil	1oz	1.25
		3.8	Core	3mil	3.00
7	GND2		Copper foil	1oz	1.25
		3.7	Prepreg	1086	2.65
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.2mm ± 10%)			47.2		47.23000

1.199642

USB3.0	SSIC	PCIE	SATA	DESTINATION	
USB3.0-1				JUSB1-->Right	
USB3.0-2	SSIC			M.2 3042(LTE)	
USB3.0-3				JUSB2-->Lef t	
USB3.0-4				JUSB3-->Rear Lef t	
USB3.0-5		PCIE-1		Card Reader	
USB3.0-6		PCIE-2		Type-C Port	
		PCIE-3		M.2 3030(WLAN)	
		PCIE-4		M.2 3030(WIGIG)	
		PCIE-5		Discrete Graphics x4	
		PCIE-6			
		PCIE-7	SATA-0		
		PCIE-8	SATA-1		
		PCIE-9		LOM	
		PCIE-10		NA	
		PCIE-11	SATA-1*	NA	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	SATA HDD	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	JUSB3-->Rear Lef t
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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Title: Port assignment

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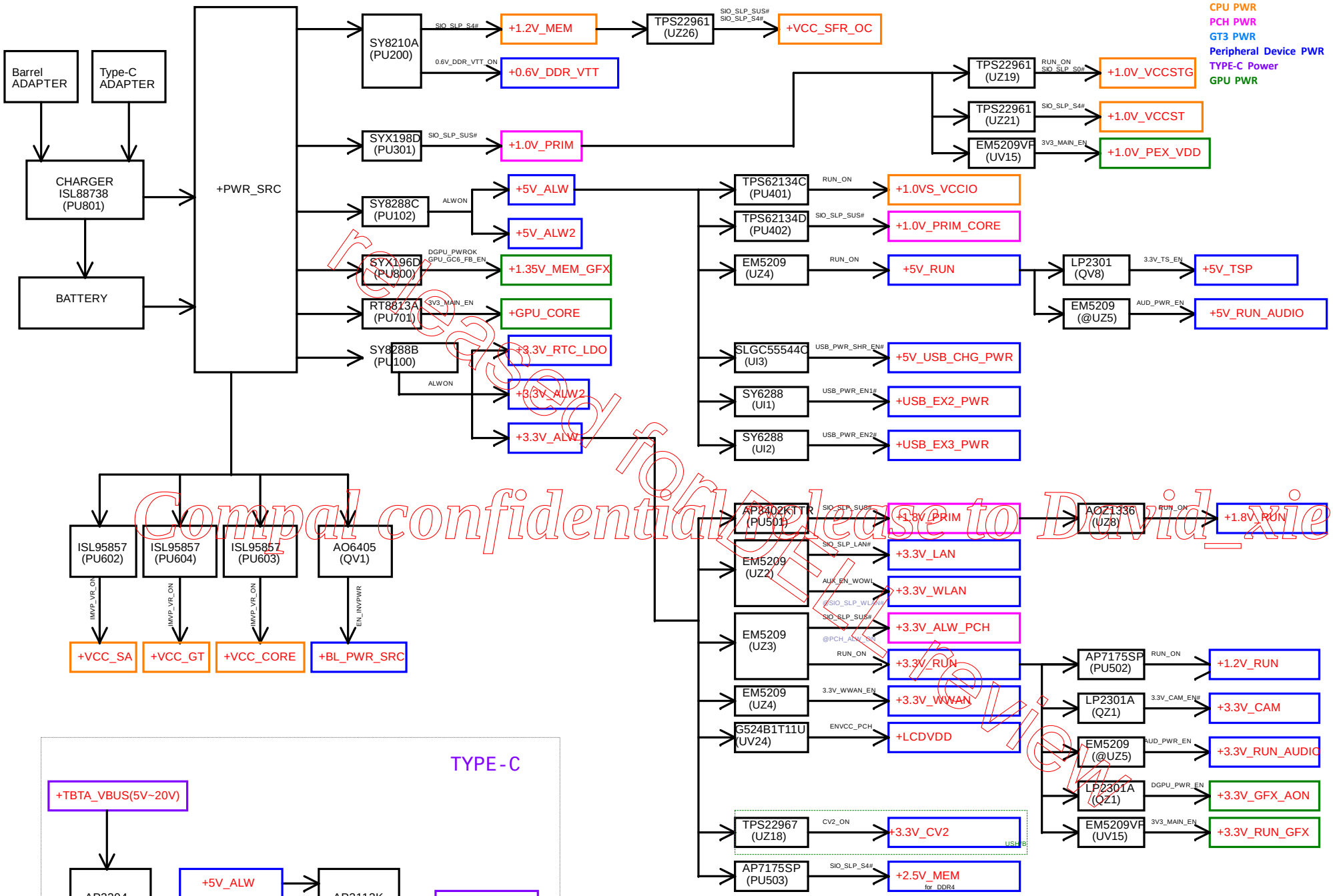
Date: Monday, December 12, 2016 | Sheet 3 of 76



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Title: Power rails

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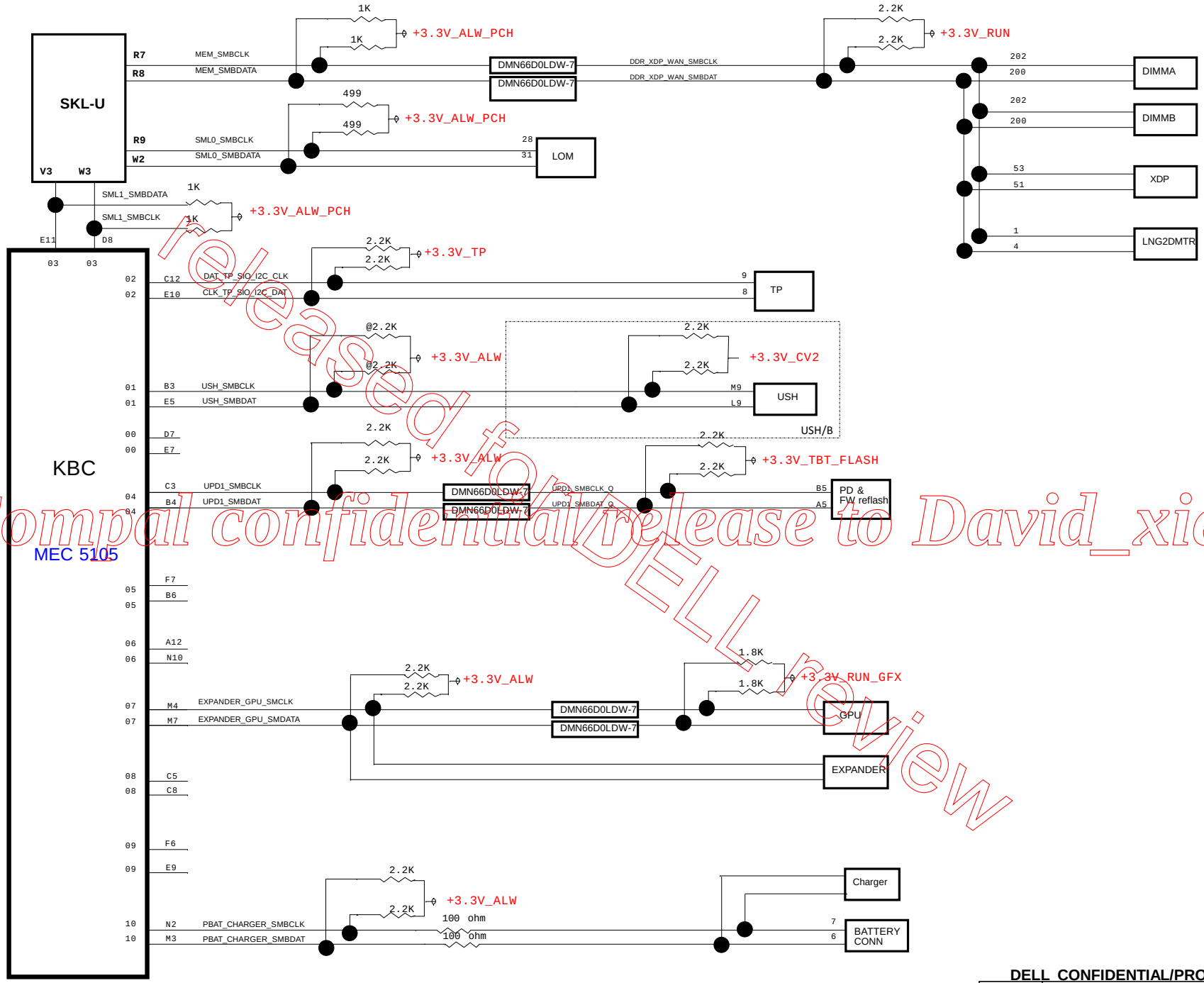

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Title: Port assignment

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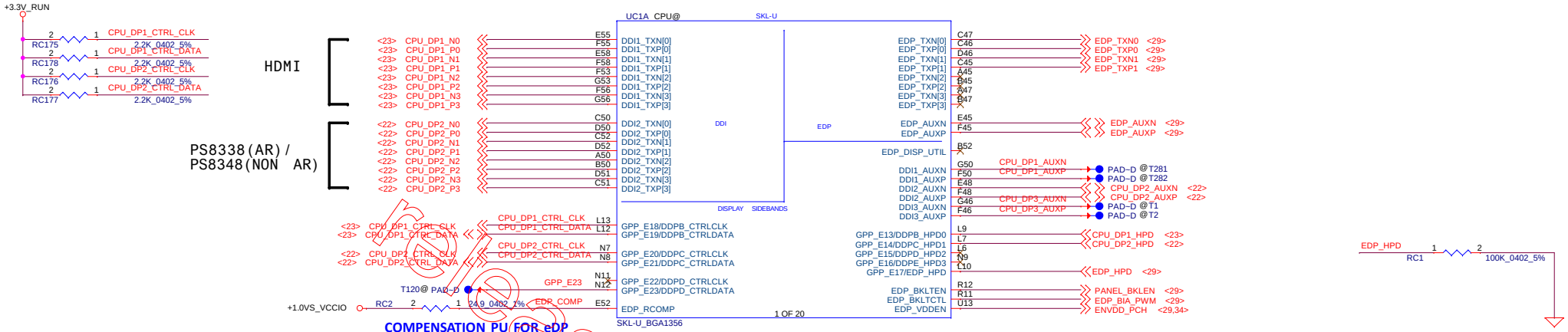
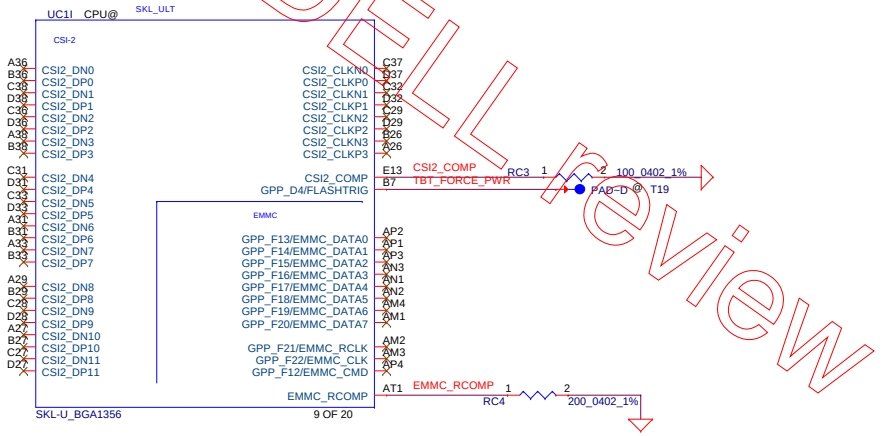
For 2LANE EDP,BR/SB12



COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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Title: CPU (1/14)

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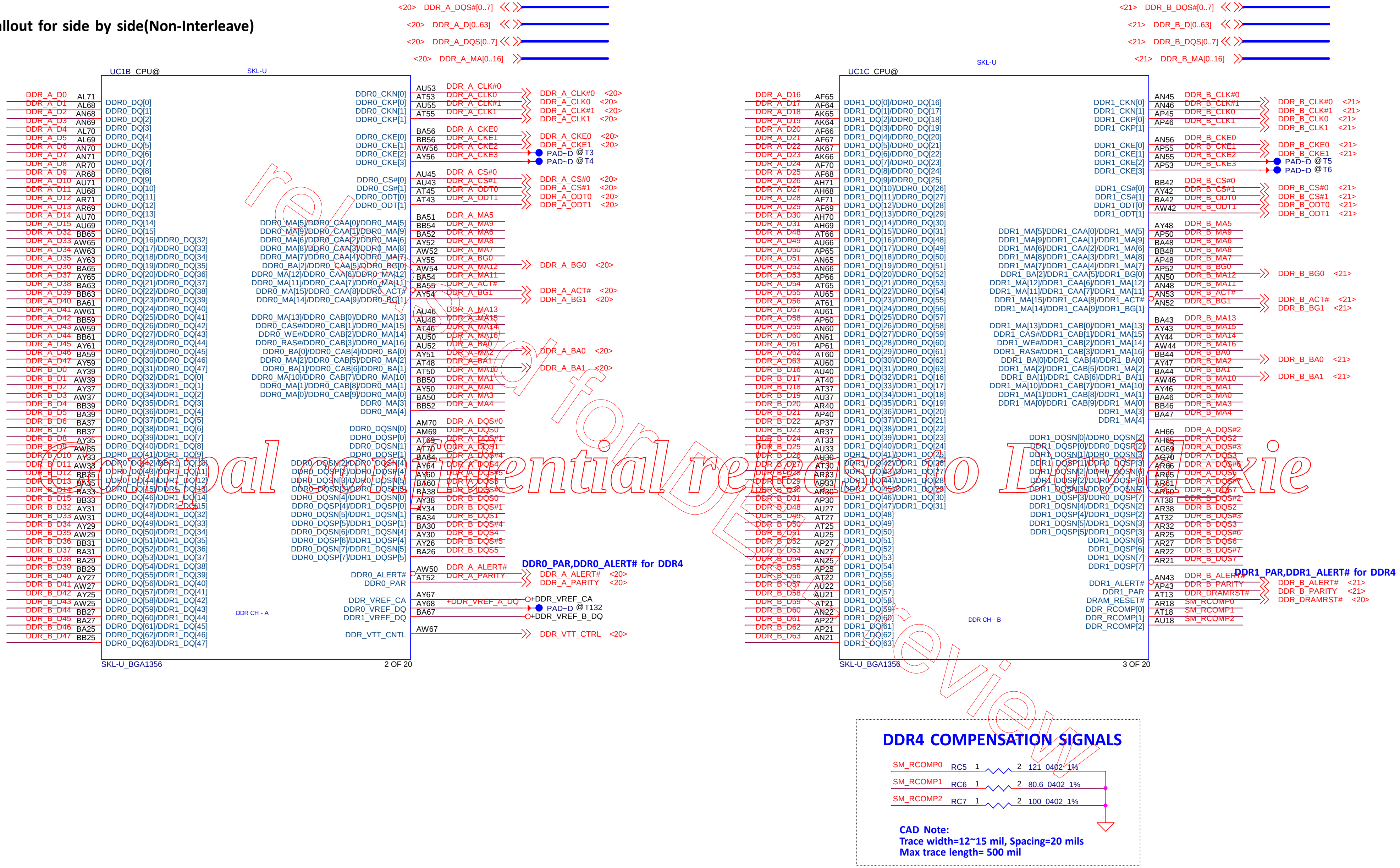
For DDR4

DDR4, Ballout for side by side(Non-Interleave)



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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ SKL-U

SPI - FLASH

PCH_SPI_CLK AV2
PCH_SPI_D1 AW3
PCH_SPI_D0 AV3
PCH_SPI_D2 AW2
PCH_SPI_D3 AU4
PCH_SPI_CS#0 AU3
PCH_SPI_CS#1 AU2
PCH_SPI_CS#2 AU1

SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

<14> PCH_SPI_DO_XDP
<14> PCH_SPI_DO2_XDP
CXDP@ RC10 1 2 1K_0402_1%
CXDP@ RC11 1 2 1K_0402_1%
<36> PCH_SPI_CS#2

SPI - TOUCH

M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

C LINK

<32> PCH_CL_CLK1 G3 CL_CLK
<32> PCH_CL_DATA1 G2 CL_DATA
<32> PCH_CL_RST1# G1 CL_RST#

+3.3V_RUN LPC@ RC13 2 1 10K_0402_5%
<34> SIO_RCIN# AW13 GPP_A0/RCIN#
<34> ESPI_ALERT# AY11 GPP_A6/SERIRQ
+3.3V_1.8V_ESPI RC21 2 1 8.2K_0402_1%

SKL-U_BGA1356

SMBUS, SMLINK

GPP_C0/SMBCLK R7 MEM_SMBCLK
GPP_C1/SMBDATA R8 MEM_SMBDATA
GPP_C2/SMBALERT# R10 PCH_SMB_ALERT#

GPP_C3/SML0CLK R9 SML0_SMBCLK
GPP_C4/SML0DATA W2 SML0_SMBDATA
GPP_C5/SML0ALERT# W1 GPP_C5
SML0_SMBCLK <30>
SML0_SMBDATA <30>

GPP_C6/SML1CLK W3 SML1_SMBCLK
GPP_C7/SML1DATA V3 SML1_SMBDATA
GPP_B23/SML1ALERT#/PCHHOT# AM7 GPP_B23
SML1_SMBCLK <34>
SML1_SMBDATA <34>

LPC

GPP_A1/LAD0/ESPI_IO0 AY13 ESPI_IO0_R
GPP_A2/LAD1/ESPI_IO1 BA13 ESPI_IO1_R
GPP_A3/LAD2/ESPI_IO2 BB13 ESPI_IO2_R
GPP_A4/LAD3/ESPI_IO3 AY12 ESPI_IO3_R
RC3661 RC3671 RC3681 RC3691 2 15_0402_5%
ESPI_IO0 <34,35>
ESPI_IO1 <34,35>
ESPI_IO2 <34,35>
ESPI_IO3 <34,35>

GPP_A5/LFRAME#/ESPI_CS# BA12 ESPI_CS# <34,35>
GPP_A14/SUS_STAT#/ESPI_RESET# BA11 ESPI_RESET# <34>

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 ESPI_CLK
GPP_A10/CLKOUT_LPC1 AY9 PCI_CLK_LPC1
GPP_A8/CLKRUN# AW11 CLKRUN# <34>
EMI@ RC16 1 2 15_0402_5%
@ RC22 1 2 22_0402_5%
ESPI_CLK_5105 <34,35>

5 OF 20

+3.3V_RUN
MEM_SMBCLK 6 1 DDR_XDP_WAN_SMBCLK <14,20,21,41>
QC2A DMN65D8LDW-7_SOT363-6
MEM_SMBDATA 3 4 DDR_XDP_WAN_SMBDAT <14,20,21,41>
QC2B DMN65D8LDW-7_SOT363-6

+3.3V_RUN
DDR_XDP_WAN_SMBDAT RC318 2.2K_0402_5%
DDR_XDP_WAN_SMBCLK RC319 2.2K_0402_5%

+3.3V_ALW_PCH
MEM_SMBCLK RC12 1K_0402_5%
MEM_SMBDATA RC14 1K_0402_5%
SML1_SMBCLK RC15 1K_0402_5%
SML1_SMBDATA RC17 1K_0402_5%
SML0_SMBCLK RC347 499_0402_1%
SML0_SMBDATA RC348 499_0402_1%

+3.3V_LAN
SML0_SMBCLK @RC19 499_0402_1%
SML0_SMBDATA @RC20 499_0402_1%

+3.3V_RUN
CLKRUN# LPC@ RC27 8.2K_0402_5%

+3.3V_ALW_PCH
PCH_SMB_ALERT# RC23 2.2K_0402_5%

TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE
WEAK INTERNAL 20K PD

+3.3V_ALW_PCH
GPP_C5 ESPI@RC25 4.7K_0402_5%

EC interface
HIGH ESPI
LOW(DEFAULT) LPC
WEAK INTERNAL 20k PD

+3.3V_ALW_PCH
GPP_B23 RC317 150K_0402_5%

EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD

PCH_SPI_CLK_1_R
PCH_SPI_CLK_0_R
@EMI@ RC28 33_0402_5%
@EMI@ RC29 33_0402_5%
@EMI@ CC7 33P_0402_50V8J
@EMI@ CC8 33P_0402_50V8J

SOFTWARE TAA

+3.3V_SPI
@RC30 PCH_SPI_D2_R1 1K_0402_5%
@RC31 PCH_SPI_D3_R1 1K_0402_5%
@RC316 PCH_SPI_D1_R1 1K_0402_5%
03/02:follow Intel MOW_2015WW06

<36> PCH_SPI_D1_R1
<36> PCH_SPI_D0_R1
<36> PCH_SPI_CLK_R1
RPC1 33_0804_8P4R_5%
PCH_SPI_D1_R1 PCH_SPI_D1_0_R
PCH_SPI_D0_R1 PCH_SPI_D0_0_R
PCH_SPI_CLK_R1 PCH_SPI_CLK_0_R
PCH_SPI_D3_R1 PCH_SPI_D3_0_R

PCH_SPI_D3_R1 @RC407 33_0402_5% PCH_SPI_D3_1_R
PCH_SPI_CLK_R1 @RC408 33_0402_5% PCH_SPI_CLK_1_R
PCH_SPI_D0_R1 @RC409 33_0402_5% PCH_SPI_D0_1_R
PCH_SPI_D1_R1 @RC410 33_0402_5% PCH_SPI_D1_1_R

RF Request
ESPI_CLK_5105 @RF@ CC316 33P_0402_50V8J
SML0_SMBCLK @RF@ CC318 33P_0402_50V8J
SML1_SMBCLK @RF@ CC319 33P_0402_50V8J
MEM_SMBCLK @RF@ CC320 33P_0402_50V8J
Place close CPU side

128Mb Flash ROM
UC5
+3.3V_SPI
CC9 0.1U_0201_10V6K
PCH_SPI_CS#0_R1 @RC37 0_0402_5% PCH_SPI_CS#0_R2
PCH_SPI_D2_R1 RC39 33_0402_5% PCH_SPI_D2_0_R
PCH_SPI_D1_0_R
PCH_SPI_D3_0_R
PCH_SPI_CLK_0_R
PCH_SPI_D0_0_R
/CS VCC
IO1 IO3
IO2 CLK
GND IO0
W25Q128FVSIQ_SO8

128Mb Flash ROM
@UC6
+3.3V_SPI
@CC10 0.1U_0201_10V6K
PCH_SPI_CS#1_R1 @RC42 0_0402_5% PCH_SPI_CS#1_R2
PCH_SPI_D2_R1 @RC43 33_0402_5% PCH_SPI_D2_1_R
PCH_SPI_D1_1_R
PCH_SPI_D3_1_R
PCH_SPI_CLK_1_R
PCH_SPI_D0_1_R
/CS VCC
IO1 IO3
IO2 CLK
GND IO0
W25Q128FVSIQ_SO8

JSPI1
+3.3V_SPI
@RC32 PCH_SPI_CS#1_R1 PCH_SPI_CS#1
PCH_SPI_D0_R1 RC33 @ PCH_SPI_D0
PCH_SPI_D1_R1 RC34 @ PCH_SPI_D1
PCH_SPI_CLK_R1 RC35 @ PCH_SPI_CLK
PCH_SPI_CS#0_R1 RC36 @ PCH_SPI_CS#0
PCH_SPI_D2_R1 RC38 @ PCH_SPI_D2
PCH_SPI_D3_R1 RC40 @ PCH_SPI_D3
+3.3V_ALW_PCH RC41 @
GND2 GND1
E-T_6705K-Y20N-00L
CONN@

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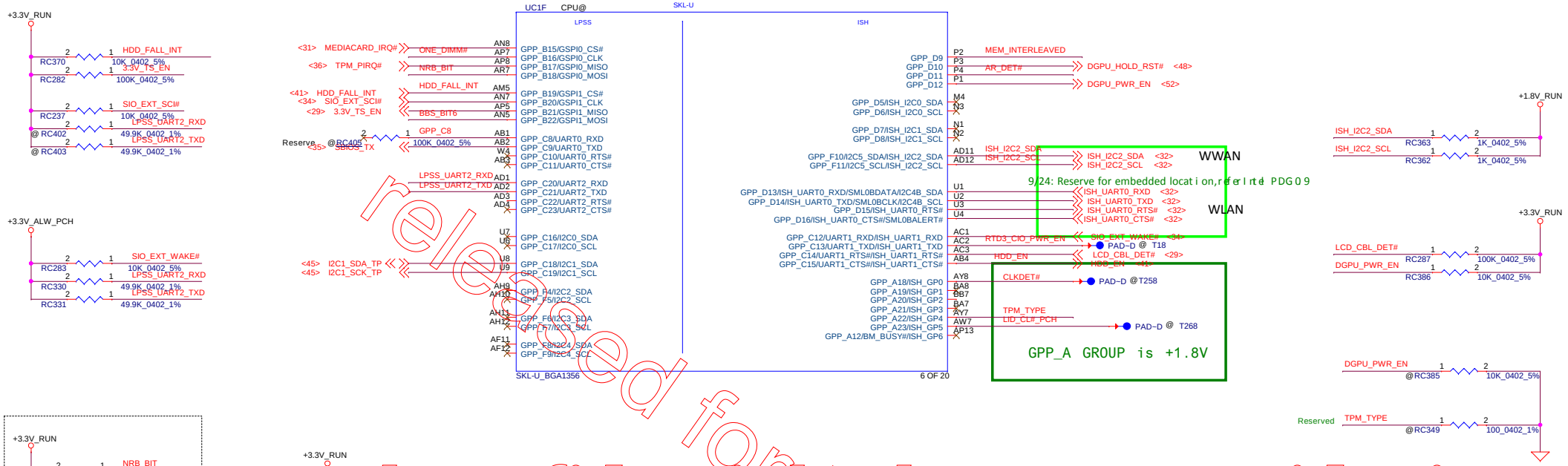
For BR DSC



NO REBOOT STRAP	
HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

Internal 20k PD

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

BOOT BIOS Destination(Bit 5)	
HIGH	LPC
LOW(DEFAULT)	SPI

Internal 20k PD

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

AR_DET#	
HIGH	NON AR
LOW	AR

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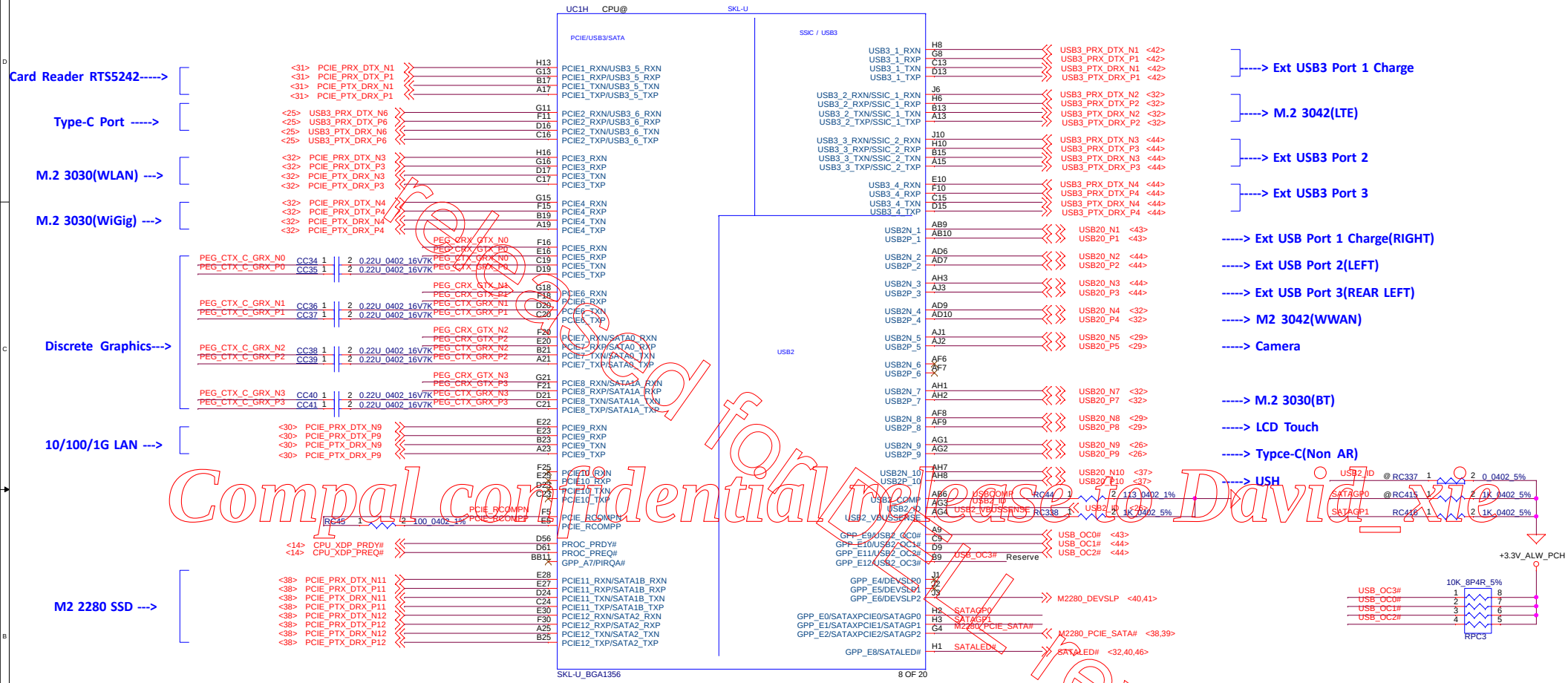
For Non AR,Breckenridge 14/15 DSC



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Title: CPU (5/14)

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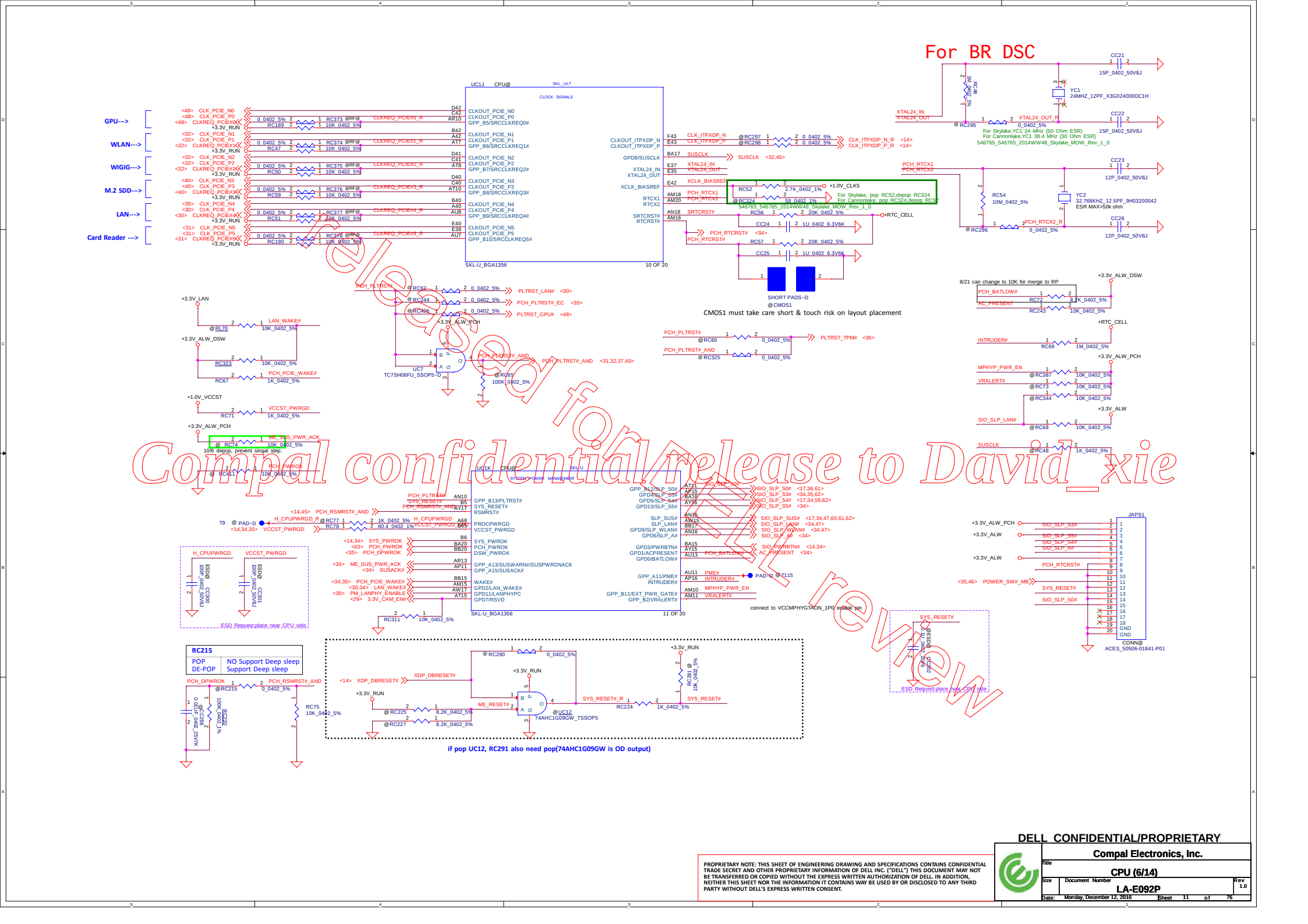
For BR DSC
GPU--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->
Card Reader --->
UC1J CPU@ SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
10 OF 20
CMOS1 must take care short & touch risk on layout placement
SHORT PADS~D
@CMOS1
UC7
TC7SH08FU_SSOP5~D
UC1K CPU@ SKL-U
SYSTEM POWER MANAGEMENT
SKL-U_BGA1356
11 OF 20
connect to VCCMPHYGTAON_1P0 enable pin
ESD Request place near CPU side
RC215
POP NO Support Deep sleep
DE-POP Support Deep sleep
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)
JAPS1
CONN@
ACES_50506-01841-P01
Confidential release to David_xie for review
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
CPU (6/14)
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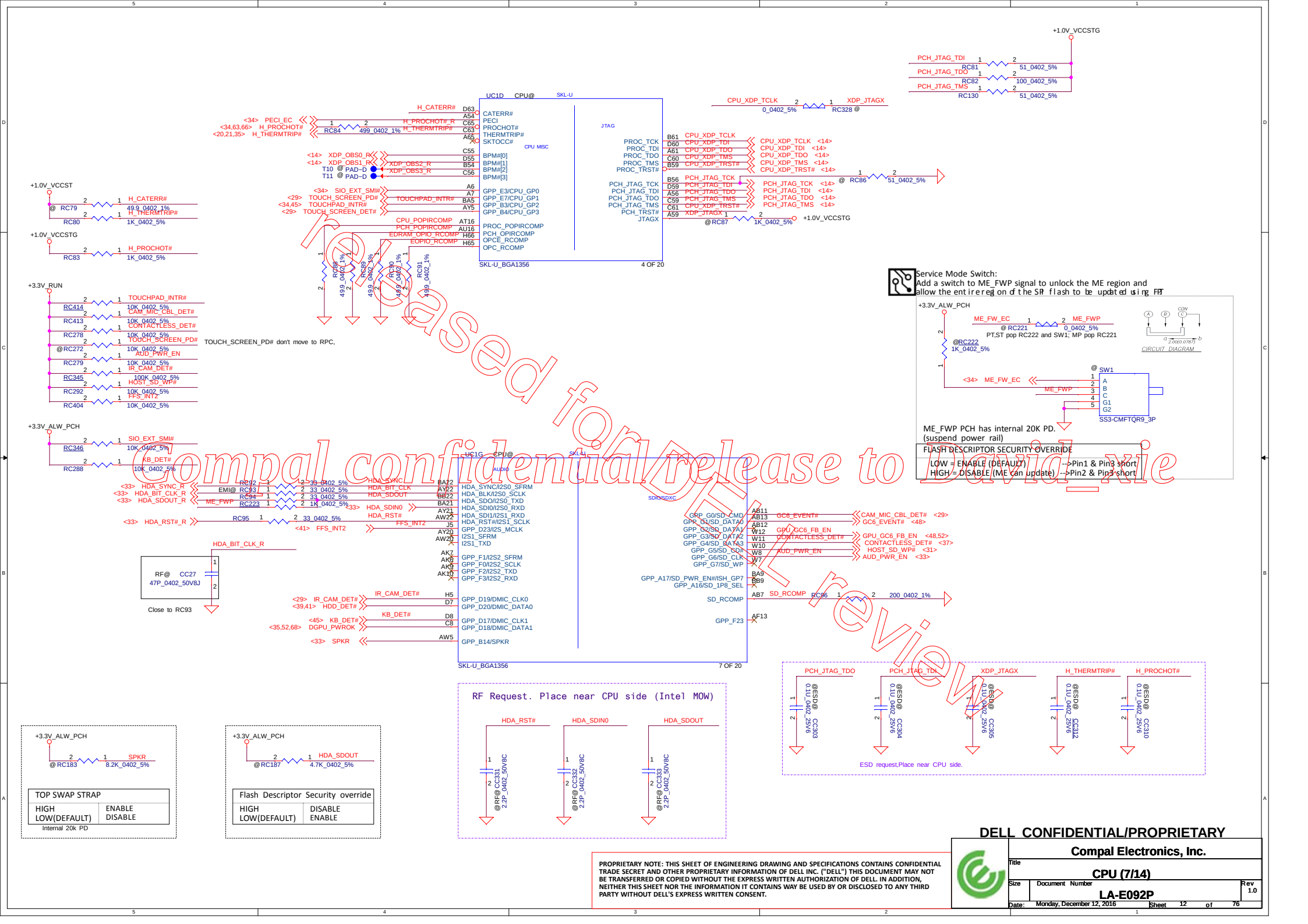

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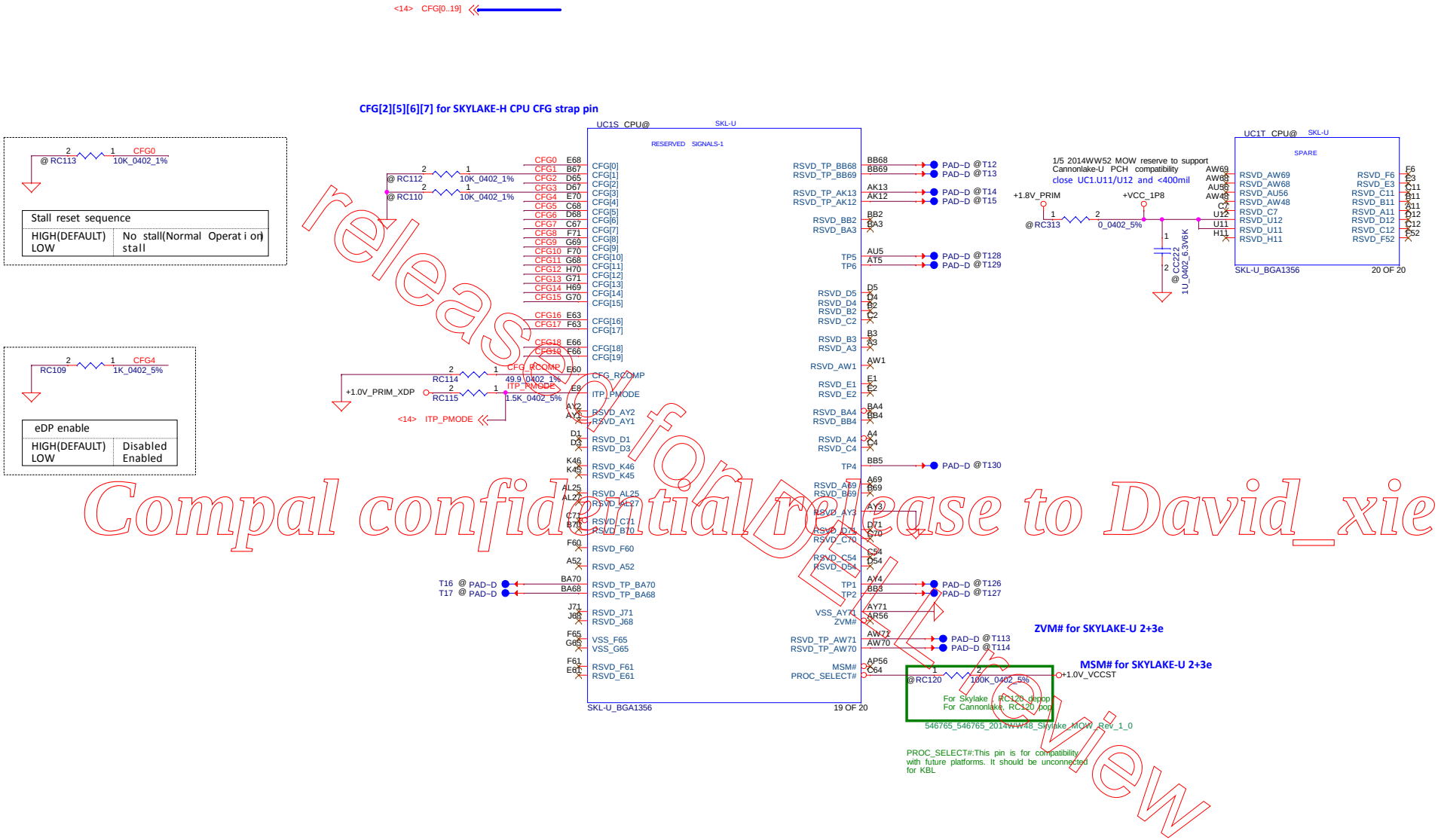

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Title: CPU (8/14)

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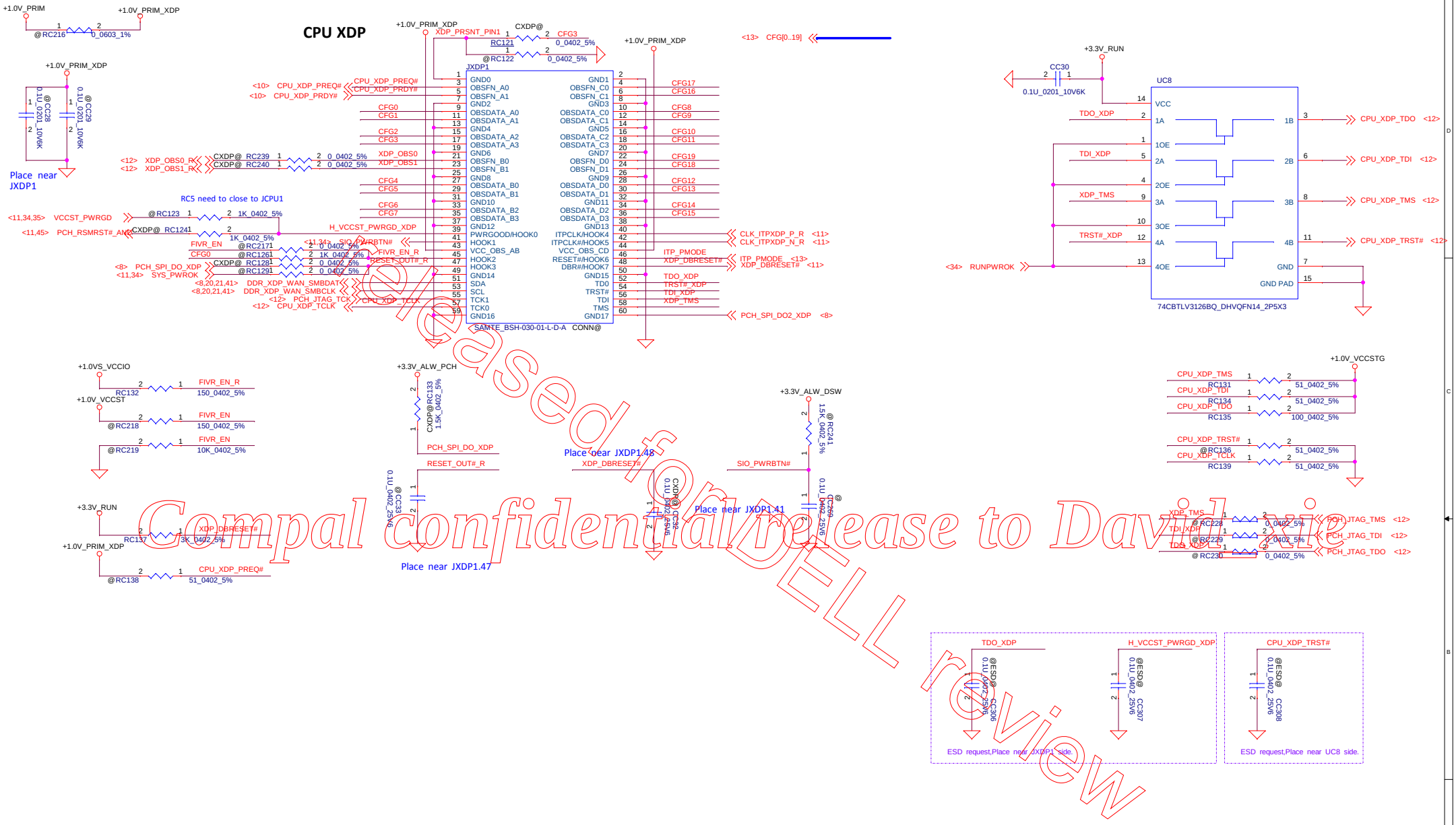
CPU XDP



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Title: CPU (9/14)

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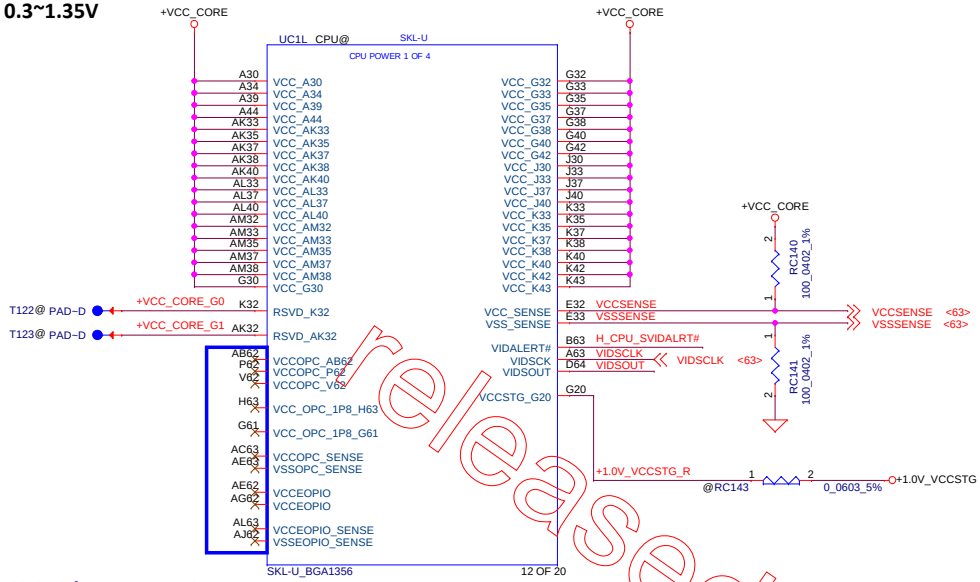
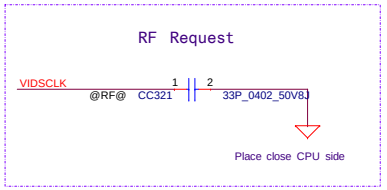
+VCC_CORE: 0.3~1.35V

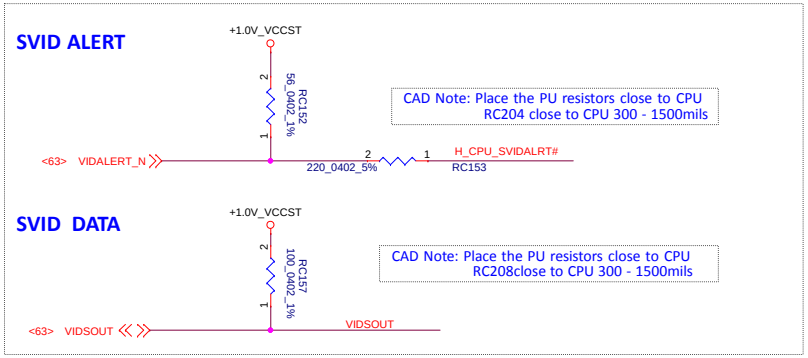


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source





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Title: CPU (10/14)

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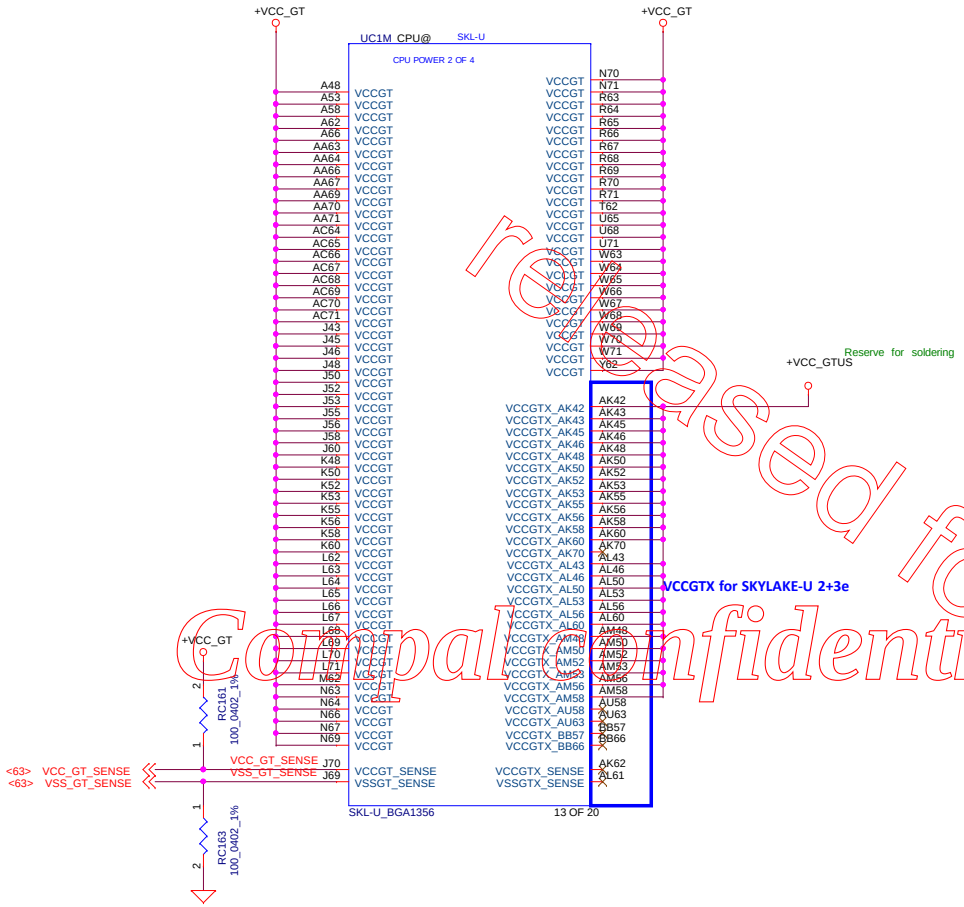
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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Title: CPU (11/14)

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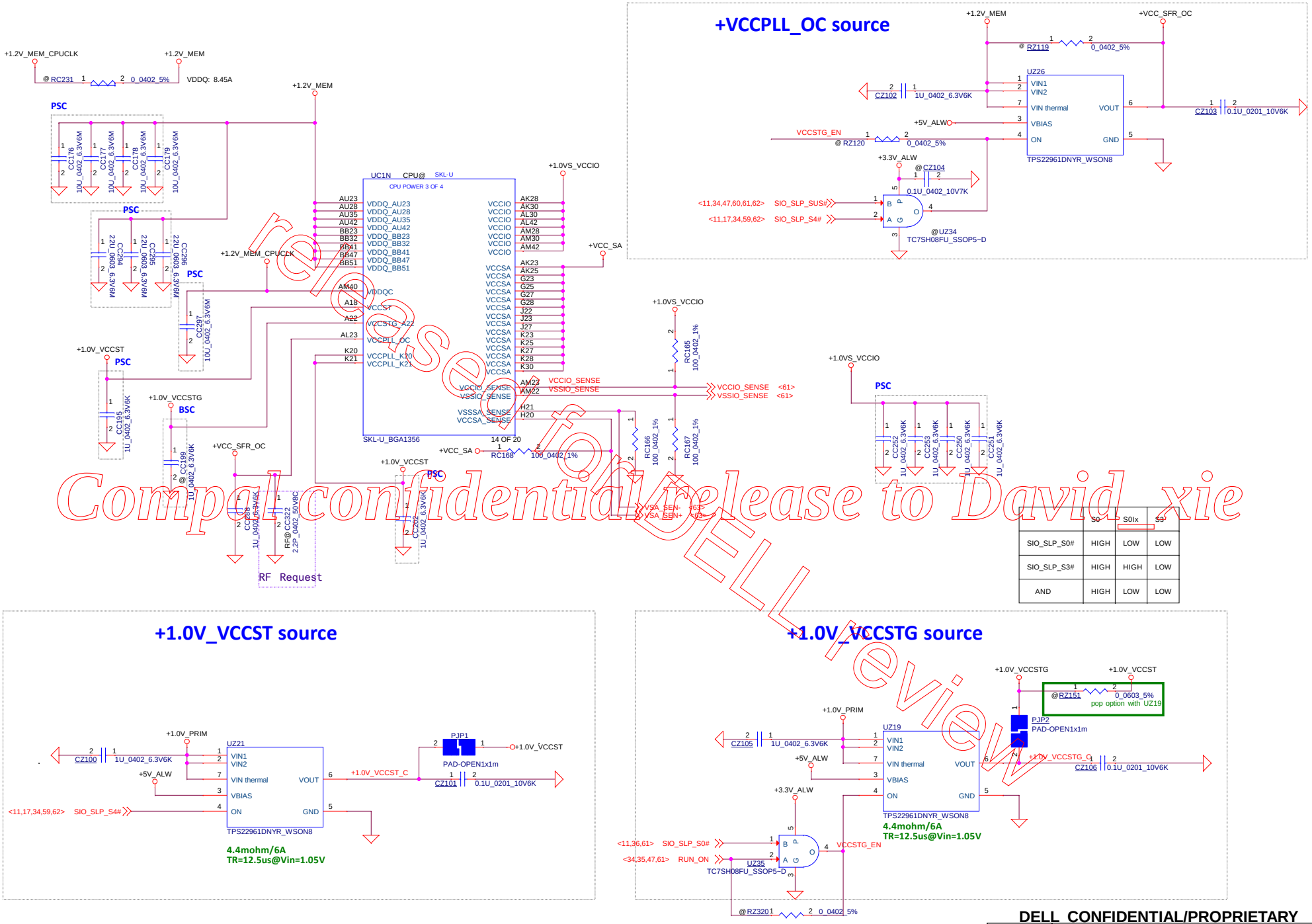

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

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Compal Electronics, Inc.

Title: CPU (12/14)

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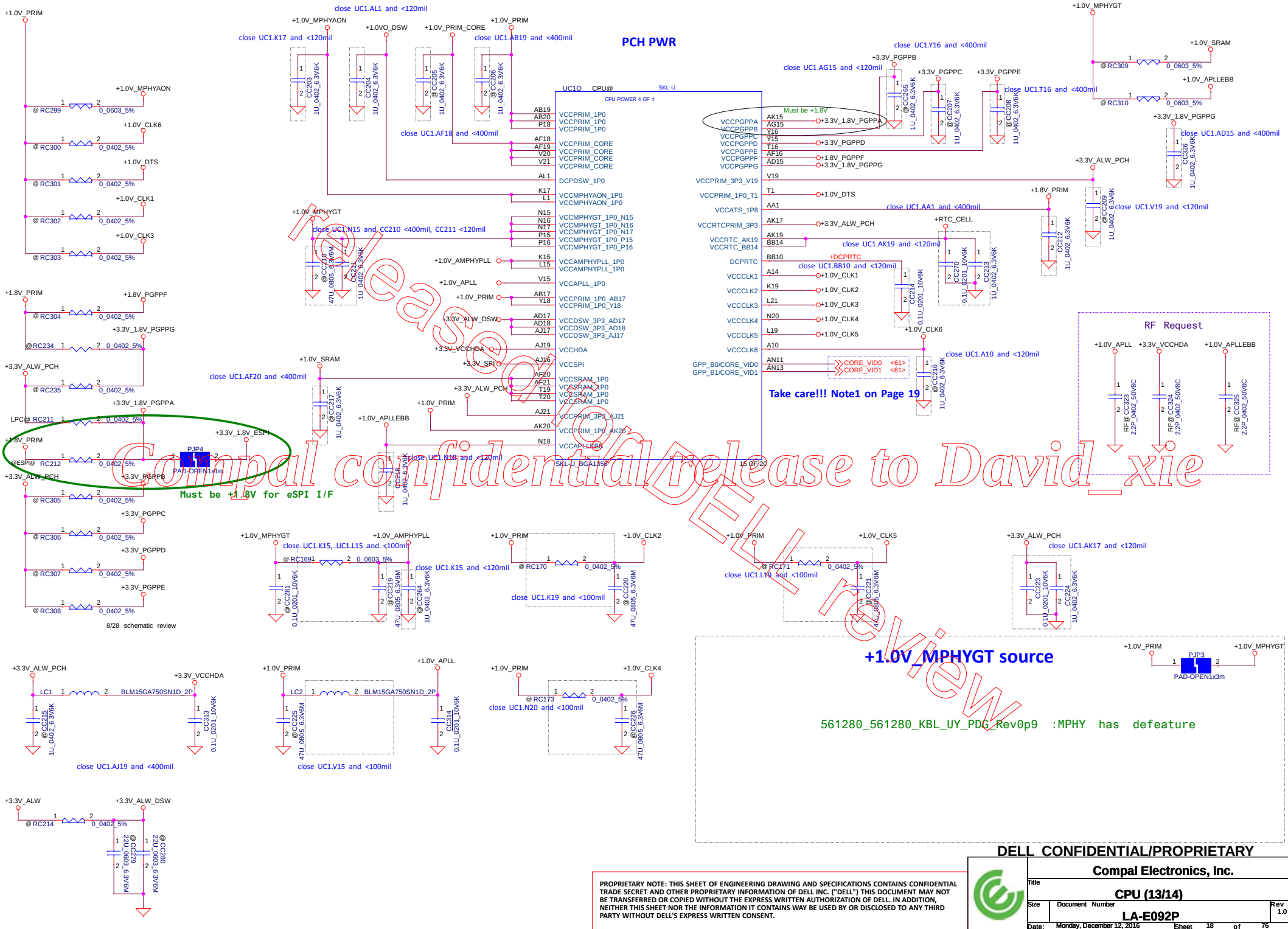
PCH PWR
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.N15 and CC210 <400mil, CC211 <120mil
close UC1.AF20 and <400mil
close UC1.K18 and <120mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.AD15 and <400mil
close UC1.AA1 and <400mil
close UC1.V19 and <120mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.AK17 and <120mil
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.K19 and <100mil
close UC1.L19 and <100mil
close UC1.N20 and <100mil
close UC1.AJ19 and <400mil
close UC1.V15 and <100mil
Must be +1.8V
Take care!!! Note1 on Page 19
Must be +1.8V for eSPI I/F
RF Request
+1.0V_MPHYGT source
561280_561280_KBL_UY_PDG_Rev0p9 :MPHY has defeature
8/28 schematic review
Compal confidential Release to David_xie
Compal Electronics, Inc.
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CPU@
UC1P SKL-U

GND 1 OF 3

SKL-U_BGA1356 16 OF 20

CPU@
UC1Q SKL-U

GND 2 OF 3

SKL-U_BGA1356 17 OF 20

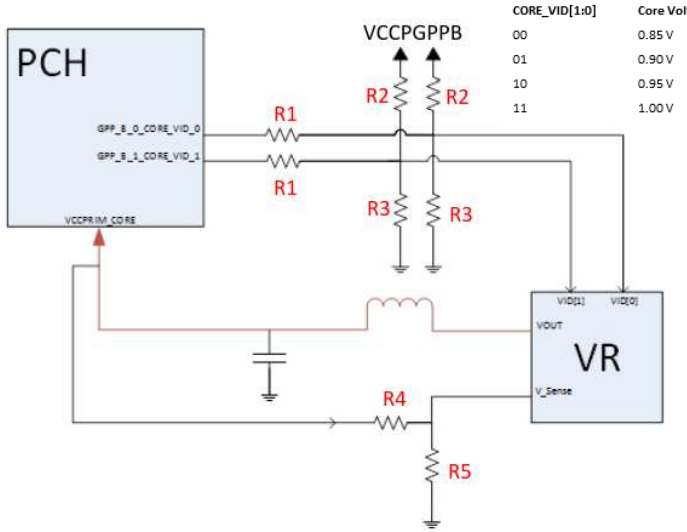
CPU@
UC1R SKL-U

GND 3 OF 3

SKL-U_BGA1356 18 OF 20

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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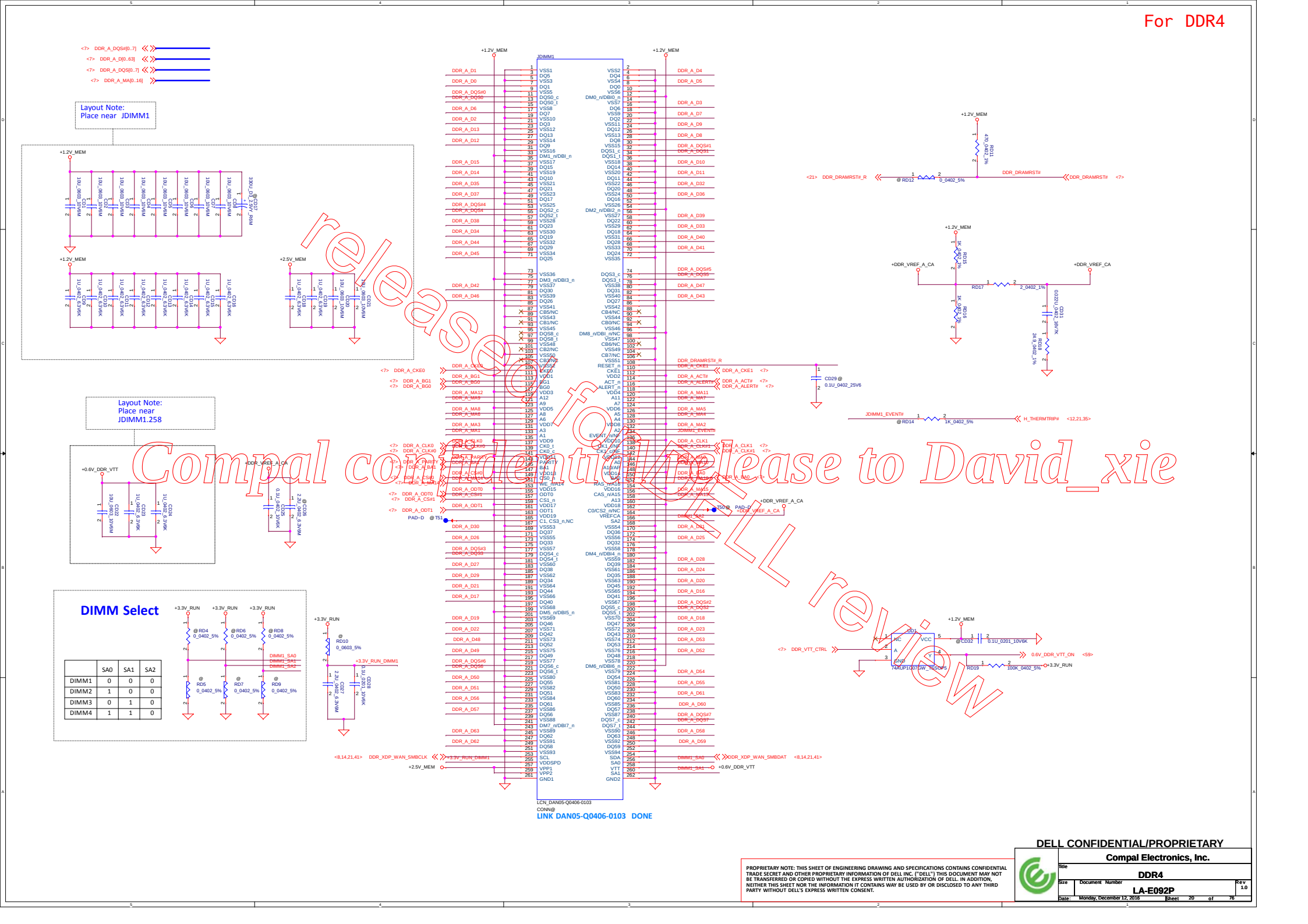
For DDR4



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

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Title: DDR4

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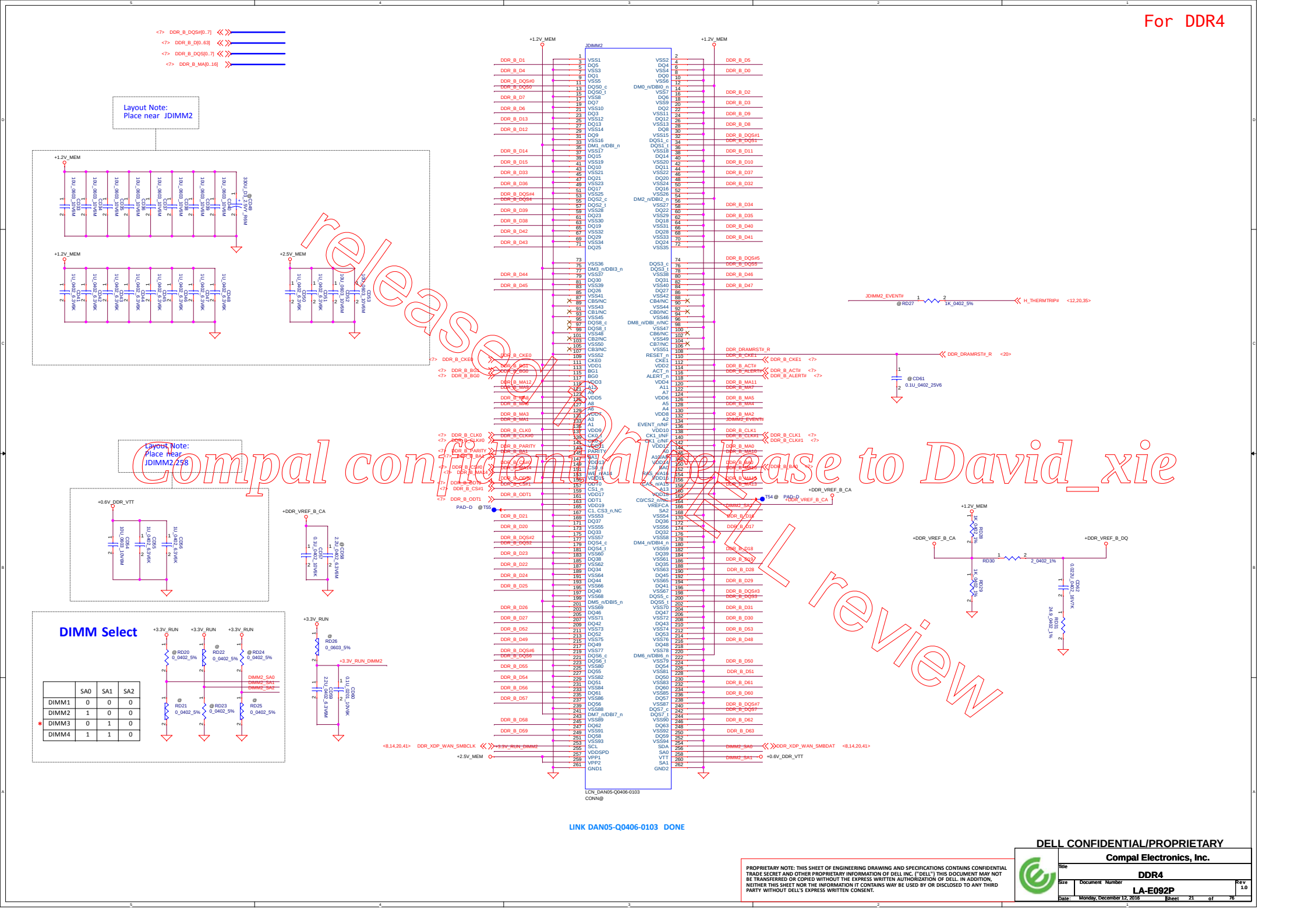
For DDR4



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Title: DDR4

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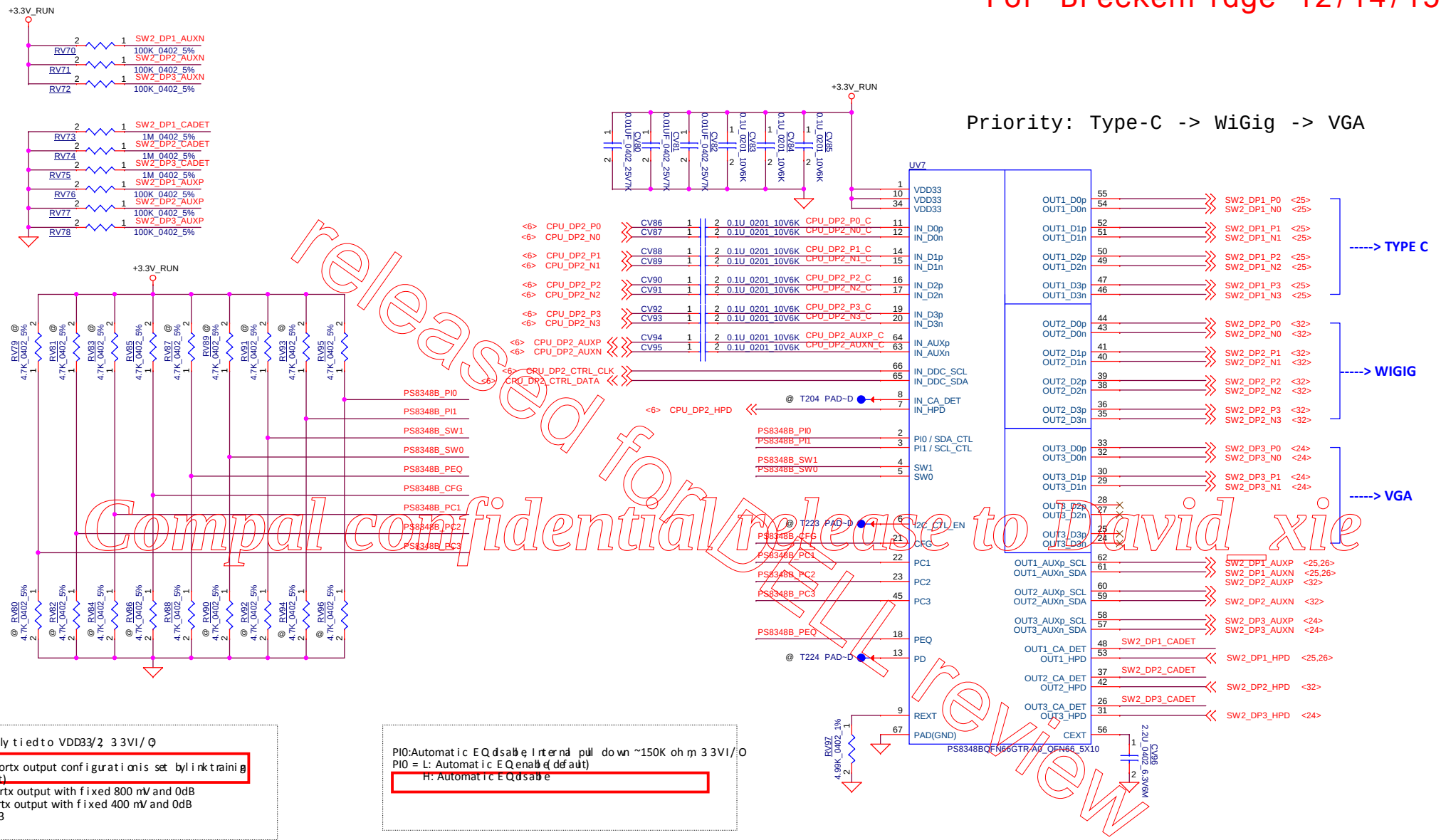
For Breckenridge 12/14/15



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Title: DP SW2 PS8348B

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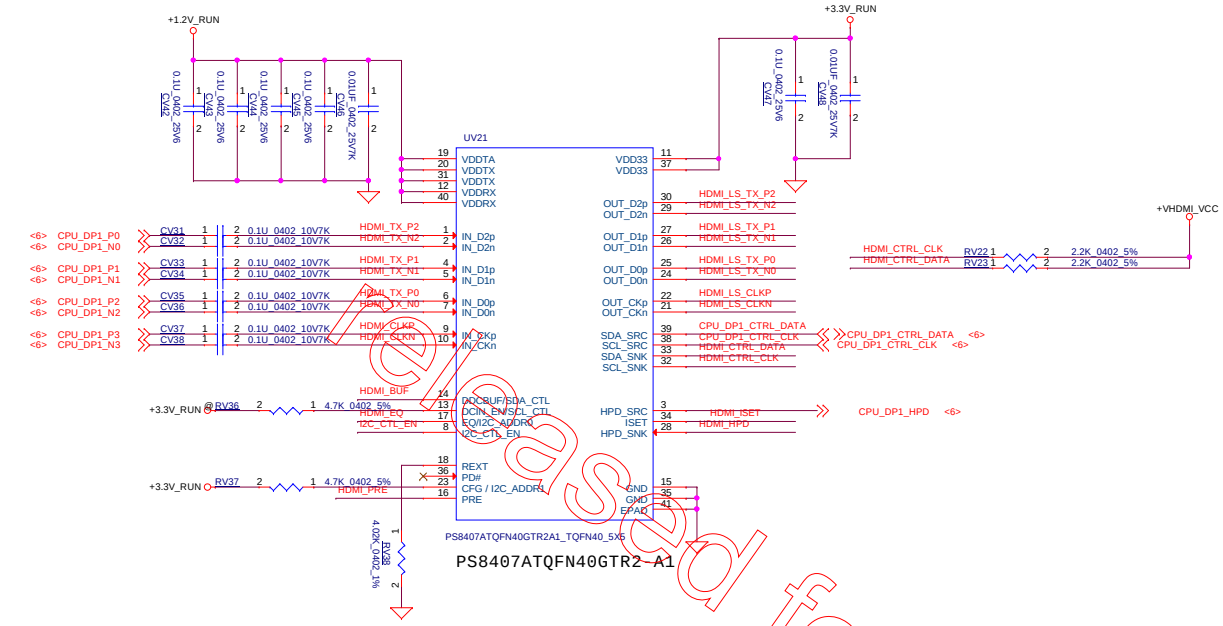
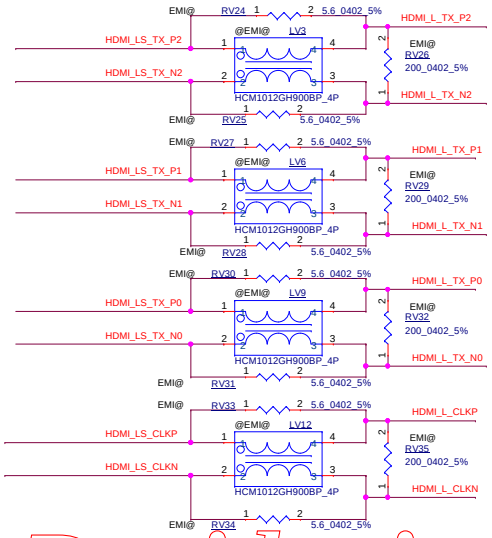
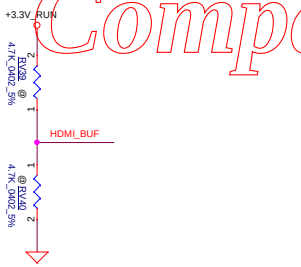
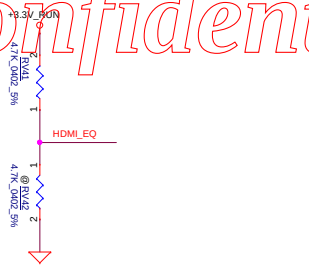
For Breckenridge 15 DSC



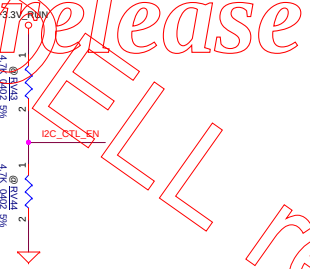




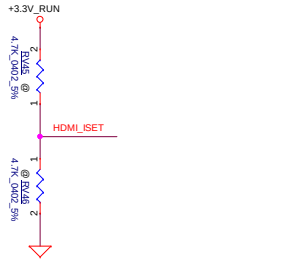
Enable active DDC buffer, Internal pull down at ~150kΩ, 3.3V I/O
L: passive DDC pass-through(default)
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor



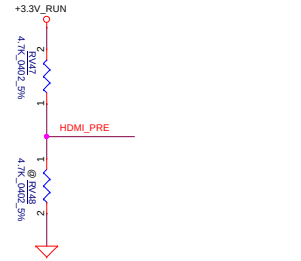
Receiver equalization setting Internal pull down at ~150kΩ, 3.3V I/O
L: programmable EQ for channel loss up to 12.4dB(default)
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB



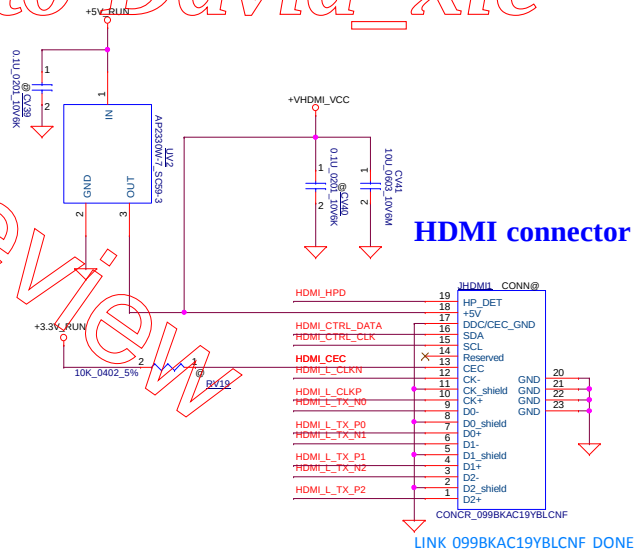
I2C Control enable,Internal pull down at 150k,3.3V I/O
L: Pin control is selected with auto jitter cleaning(default)
H: I2C control is selected with default I2C address
M: Pin control is selected with full jitter cleaning



TMDS output swing adjustment, Internal pull down at ~150kΩ, 3.3V I/O
L: default,1000mV
H: increase +13%
M: reduce -13%



Output pre-emphasis setting Internal pull down at ~150kΩ, 3.3V I/O
L: no pre-emphasis(default)
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis



HDMI connector

LINK 099BKAC19YBLCNF DONE

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Title: HDMI CONN		
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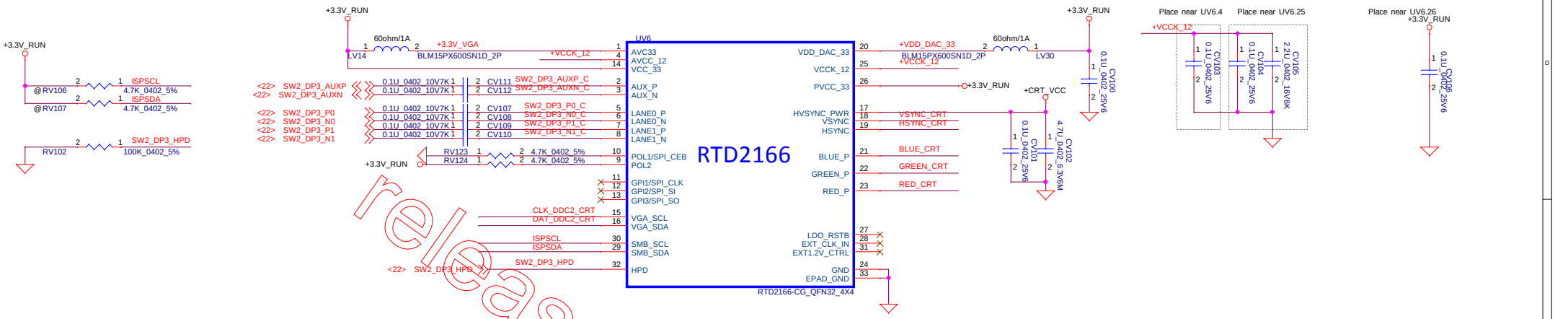
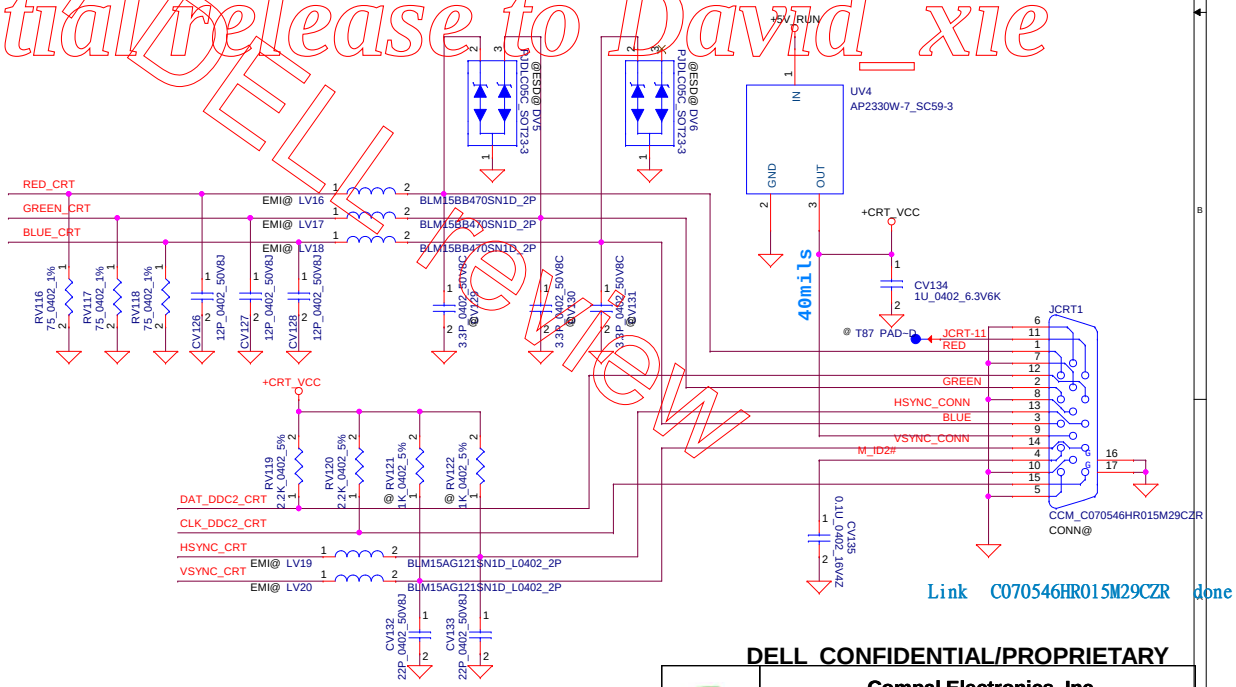
For Breckenridge 12/14/15
For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



Link C070546HR015M29CZR done

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Title: DP to VGA & VGA Conn

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For NON-AR port1

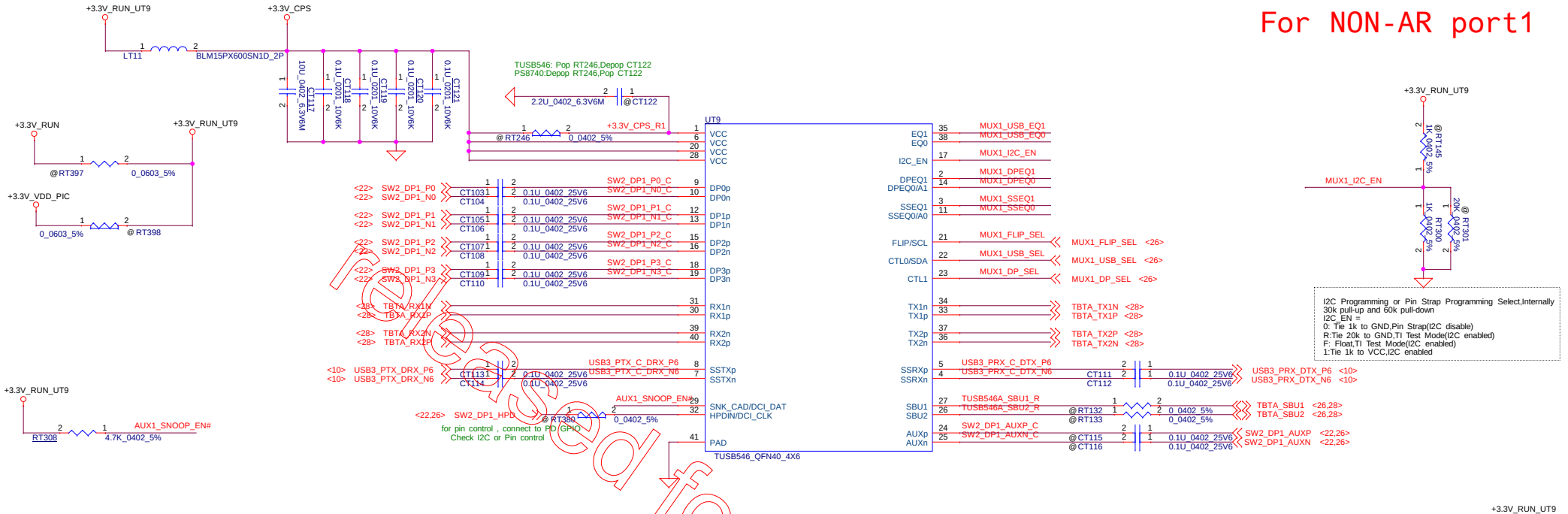

Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

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Title: DP/USB3 Repeater SW TUSB546

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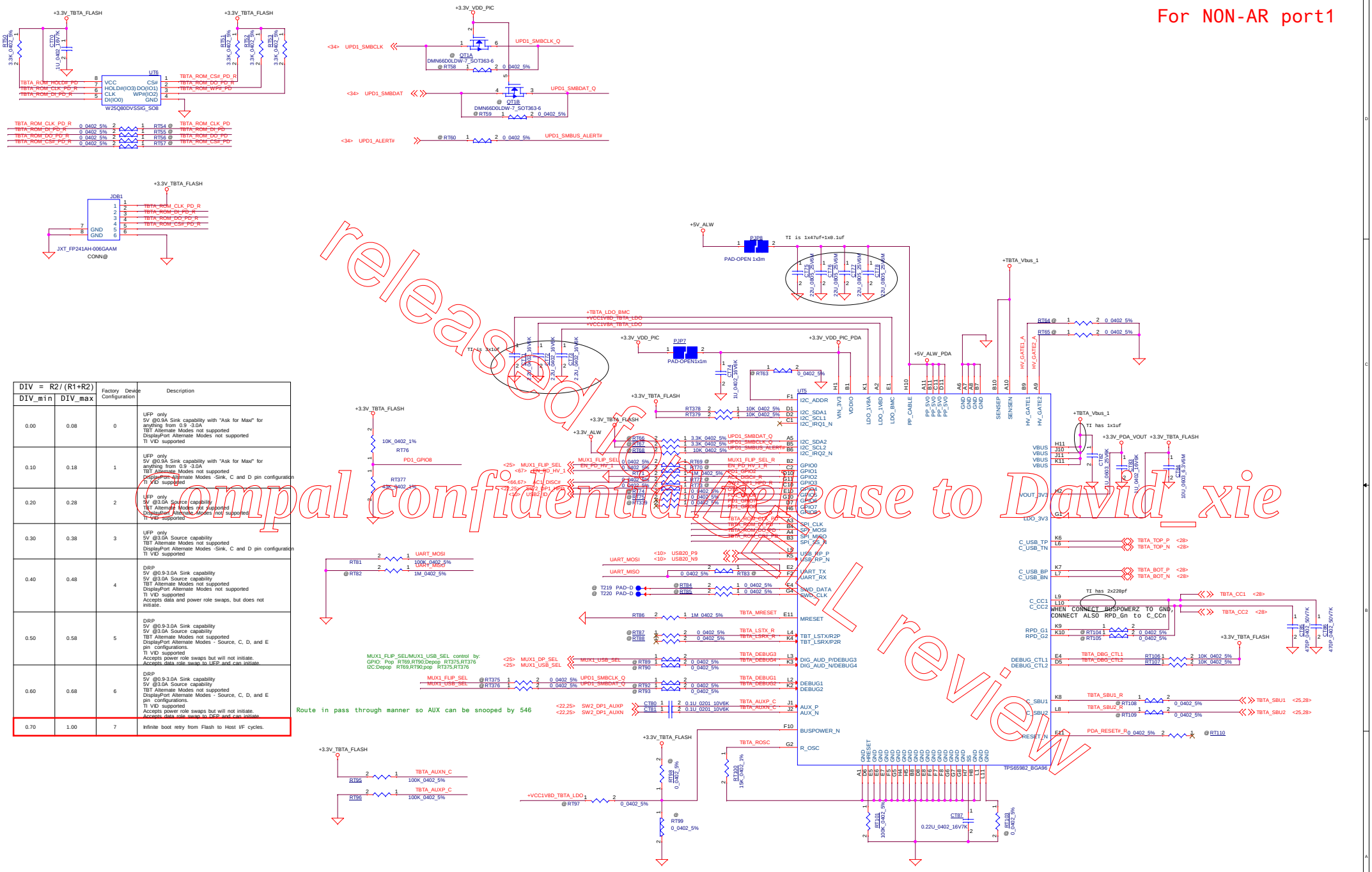
For NON-AR port1



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

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Title: [Type C]PD Controller TI

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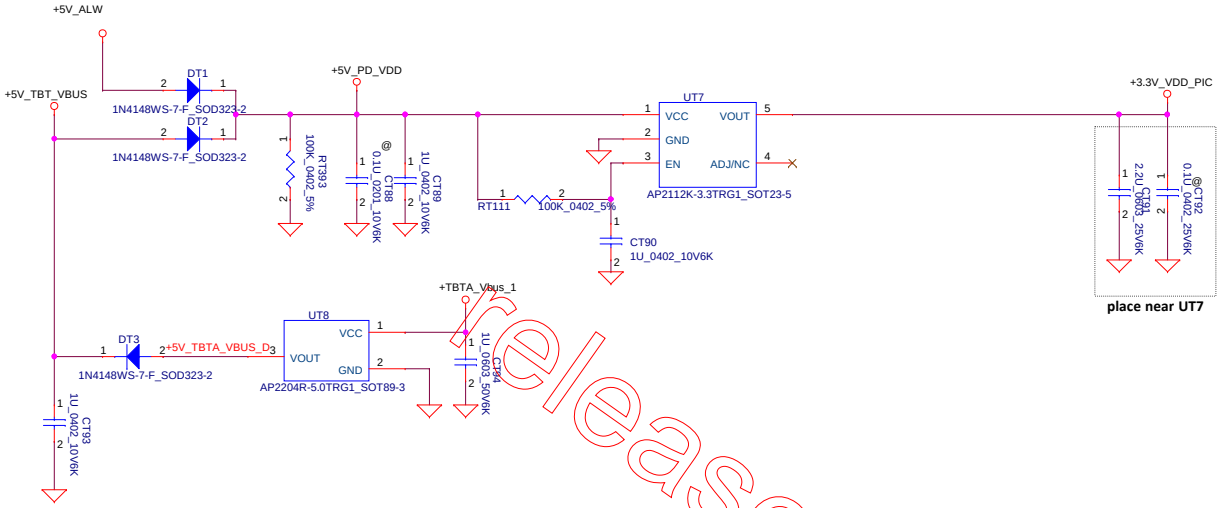

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Title: [Type C]PD Power

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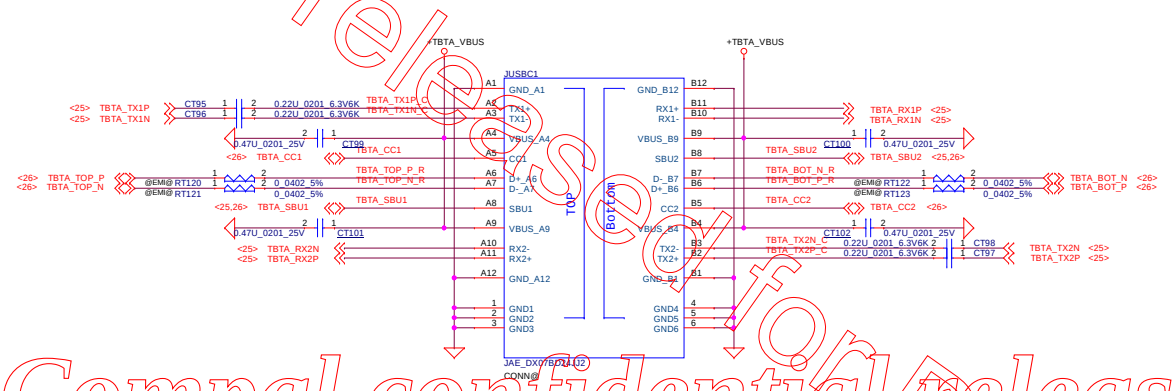
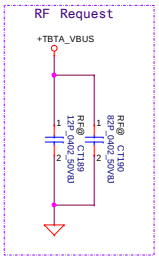
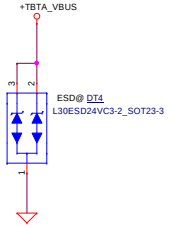
For NON AR Config

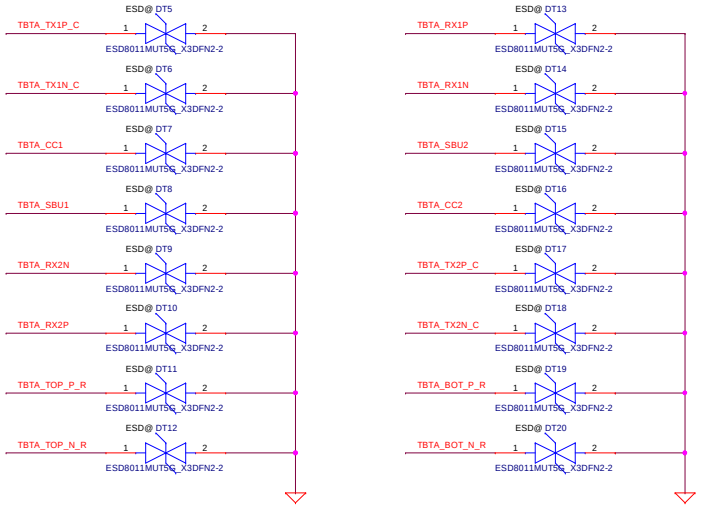


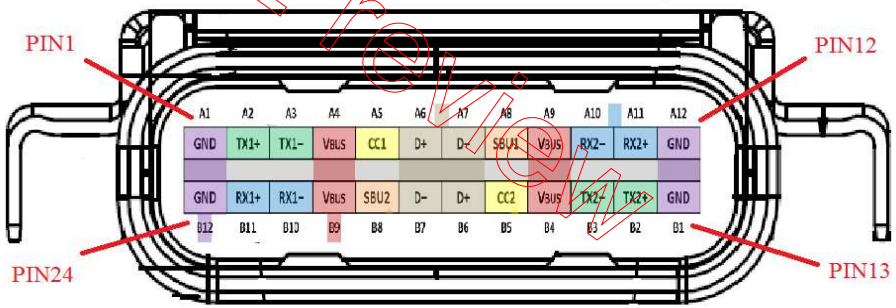




DX07BD24J2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B





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Title: USB 3.0 CONN TYPE C

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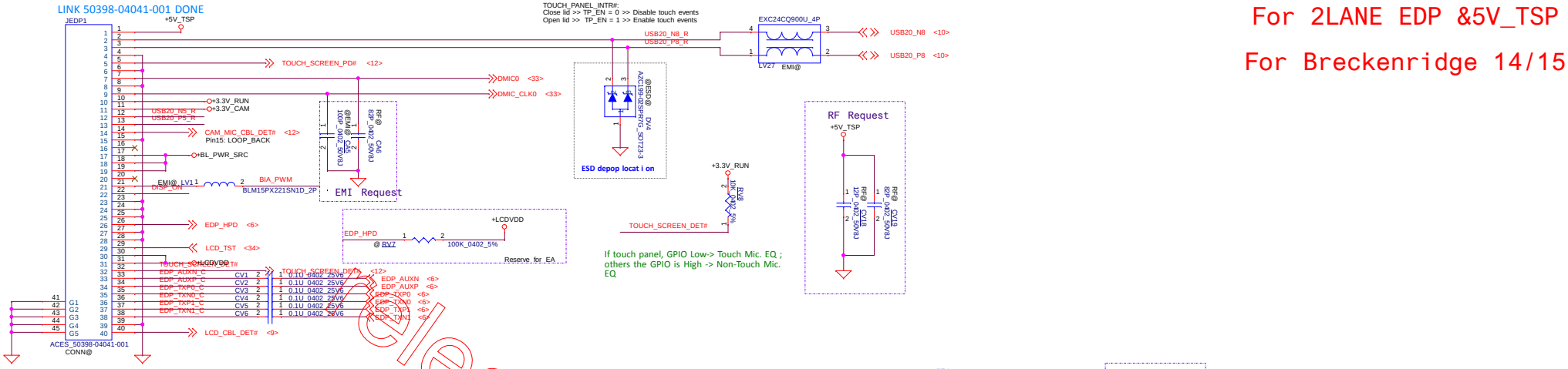
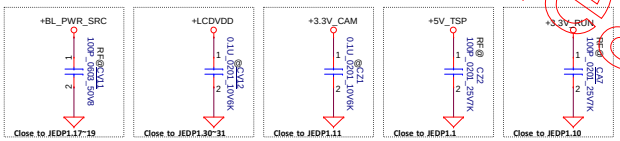
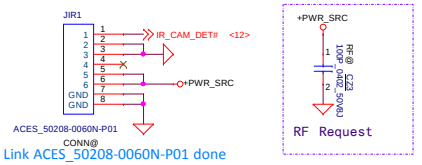
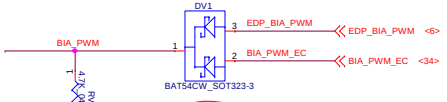
For 2LANE EDP &5V_TSP

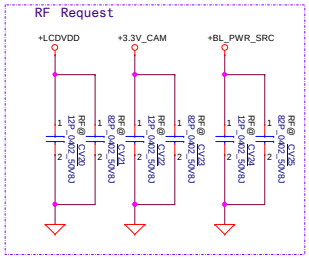
For Breckenridge 14/15

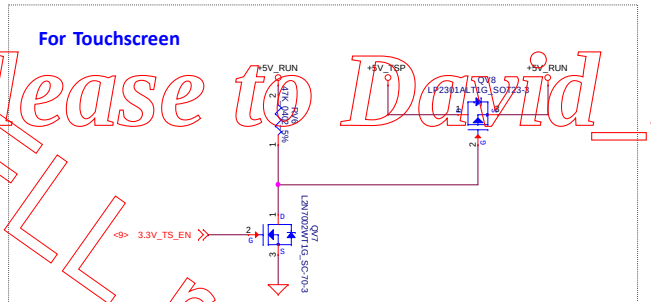


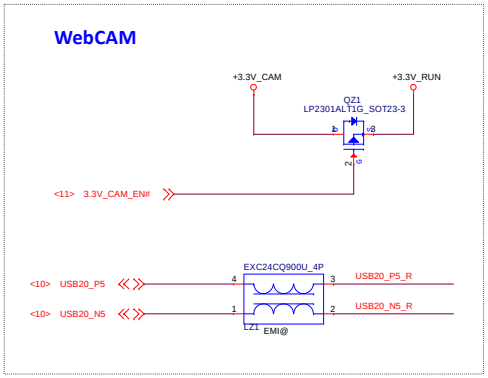


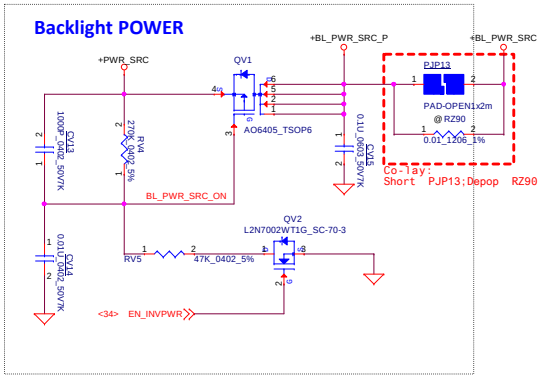


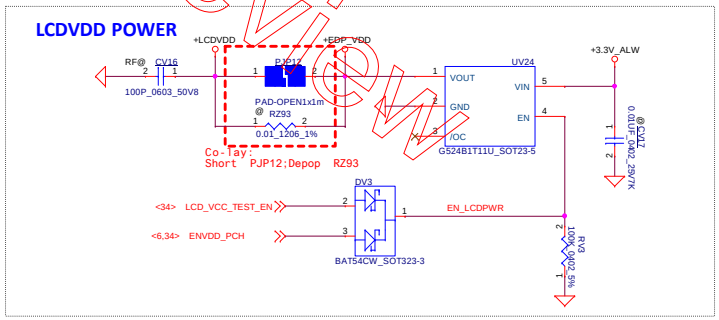












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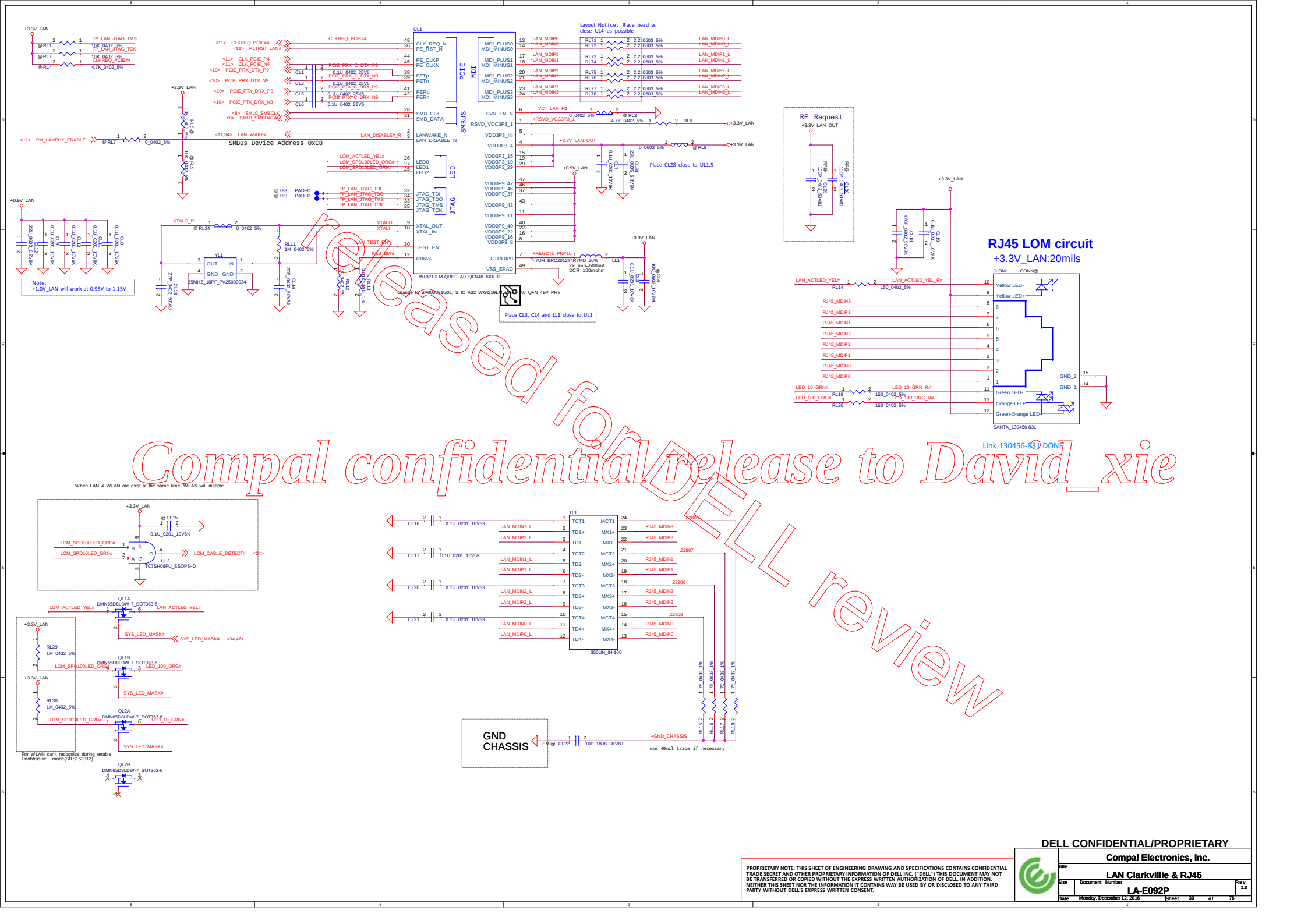
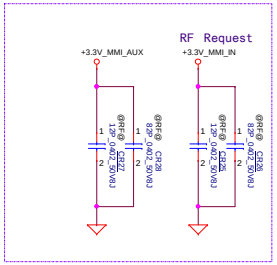
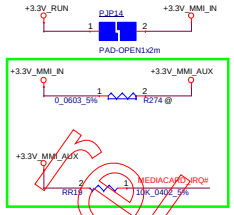


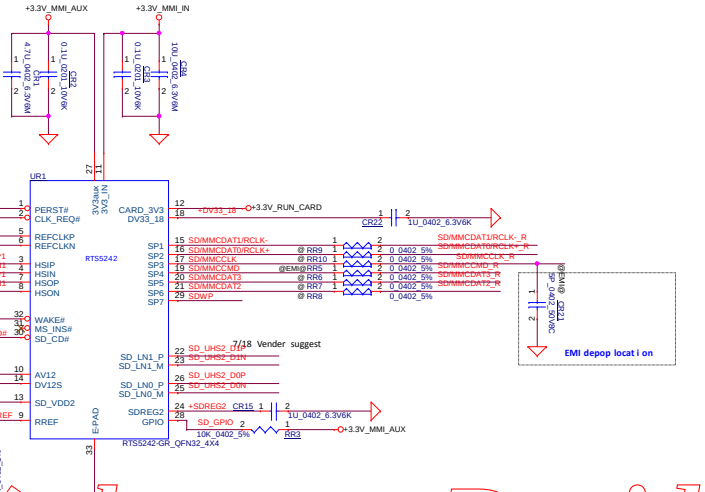
For PCIE Interface



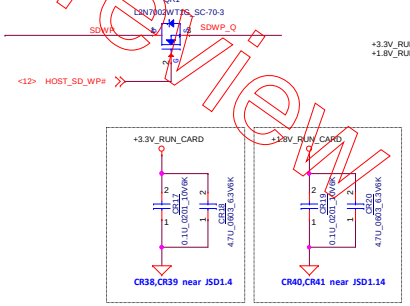


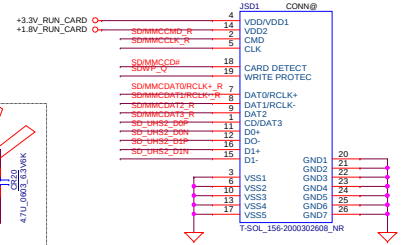
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/of f 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)





LINK SP070011U00 DONE

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Compal Electronics, Inc.

Title: Card Reader RTS5242

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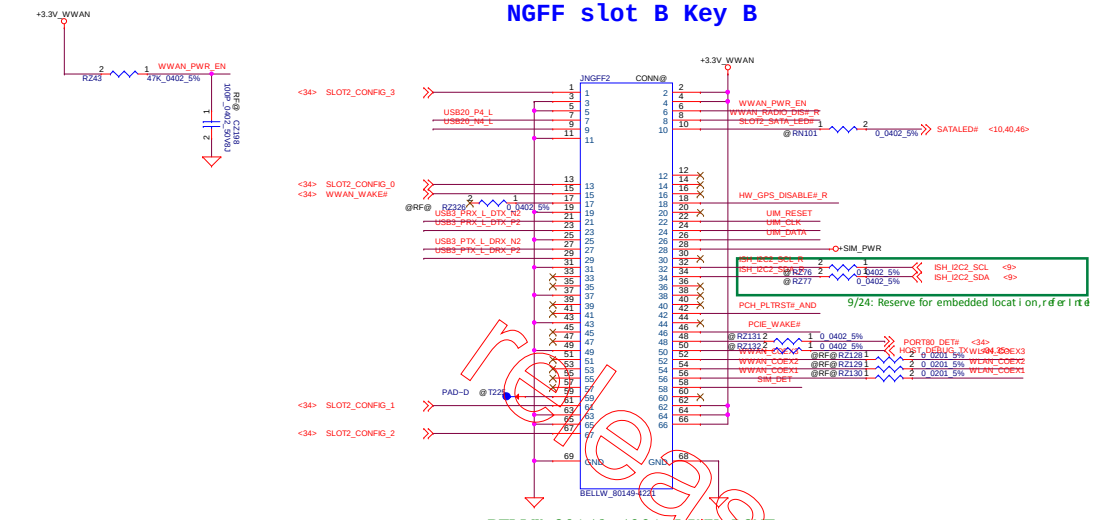
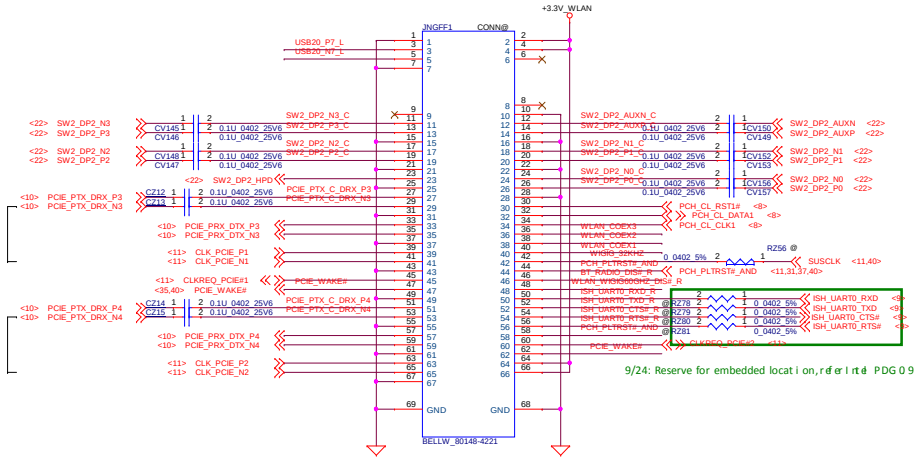
NGFF slot B Key B

for Brekenridge 14/15 DSC

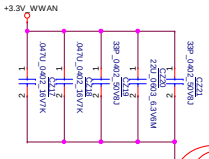


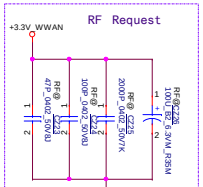
BELLW_80149-4221 LINK DONE

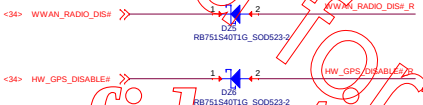
NGFF slot A Key A

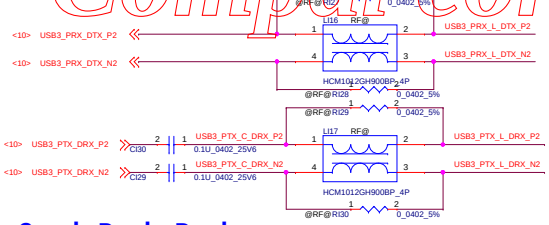


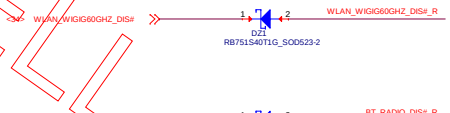
BELLW_80148-4221 LINK DONE

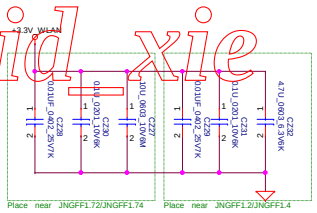


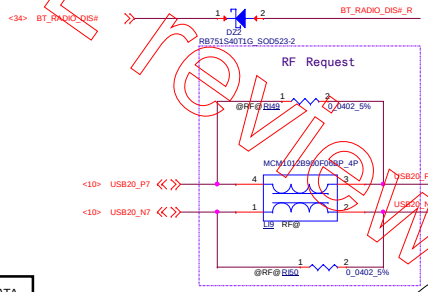


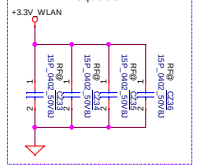




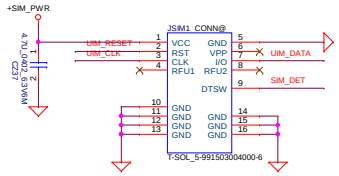




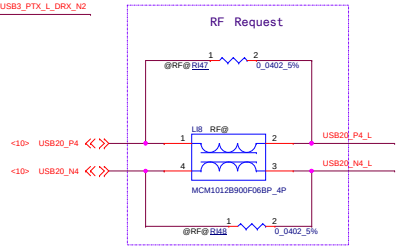


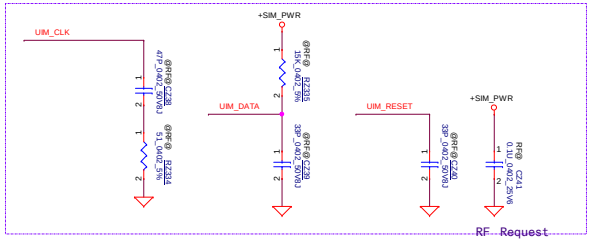


SIM Card Push-Push



T-SOL_5-991503004000-6 LINK DONE





STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

Compal Electronics, Inc.

Title: NGFF Card

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Link 50278-00401-001 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 14.

Add for solve pop noise and detect issue

place close to pin41

place close to pin46

place close to pin26

place close to pin40

place close to pin9

place close to pin1

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

Normal Open

Link SINGA_2SJ3095-059111F DONE

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	<Deciphered_Date>

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Compal Electronics, Inc.

Title: Codec ALC3246

Size: C | Document Number: LA-E092P | Rev: 1.0

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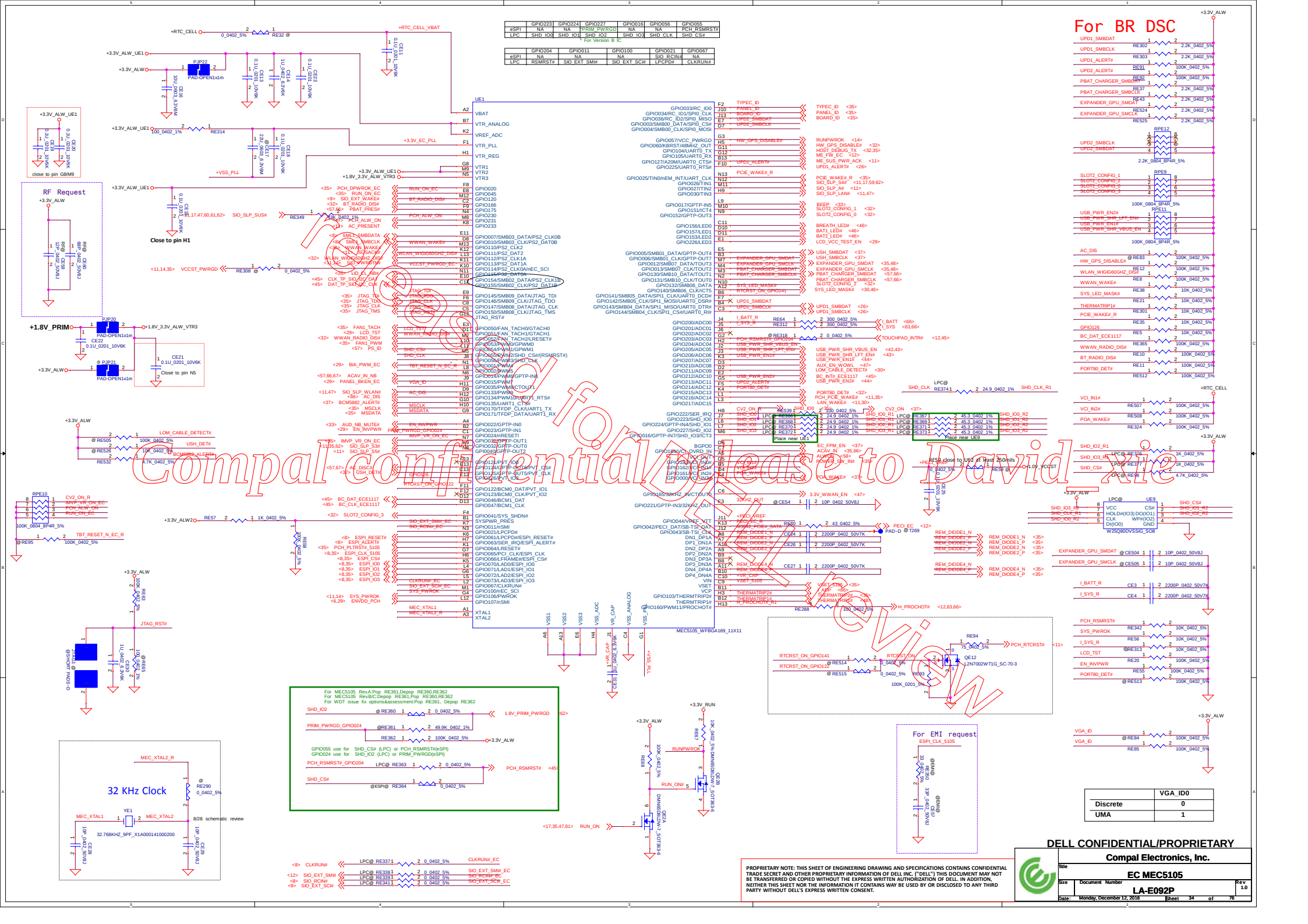

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

	VGA_ID0
Discrete	0
UMA	1

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Compal Electronics, Inc.

Title: EC MEC5105

Size: Document Number: LA-E092P Rev: 1.0

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For BR DSC

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

JXT_FP241AH-010GAAM LINK DONE

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

WDT option
MEC5105 rev.B: Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C: Pop RE362, RE536, Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537

CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

GPIO223 is OD. When EC fetches the code, set GPIO223 to Low.

To prevent backdrive to PCH_DPWROK_EC when AC is plugged before +3.3V_ALW ramps up.

In DC mode, ACAV_IN is LOW. This circuit doesn't affect PCH_DP WROK.
In AC mode, 1. ACAV_IN is high. GPIO223 is tri-state. QE13B is ON. QE13A can prevent backdrive to PCH_DPWROK.
2. EC fetches code and the drives GPIO223 to LOW to turn off QE13B. When QE13B is off, un-plug/plug AC will not affect DSW_DPWRO
3. When WDT occurs, GPIO223 is tri-state (EC reset). ACAV_IN charges CE503. When AC is removed, ACAV_IN goes LOW immediately.
QE13B still keeps on according to RC discharging rate to PCH_DP WROK is LOW because ACAV_IN is LOW

JXT_FP241AH-010GAAM LINK DONE

Link 50271-0040N-001 DONE

RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	TBD
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time measured from 5%~68%

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

BOARD_ID rise time measured from 5%~68%

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
* 33K	4700p	15"
4.3K	4700p	17"

PANEL_ID rise time measured from 5%~68%

Thermal diode mapping	
5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Write
R/W = 1 = Read

SMBus address 0x40

Stuff RE275 and no stuff RE274 keep ES design
Stuff RE274 and no stuff RE275 to save two GPIOs on EC(PCH_PCIE_WAKE# should be output with OD)

RF Request

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

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Title: MEC5105 Support
Size: Document Number: LA-E092P
Rev: 1.0
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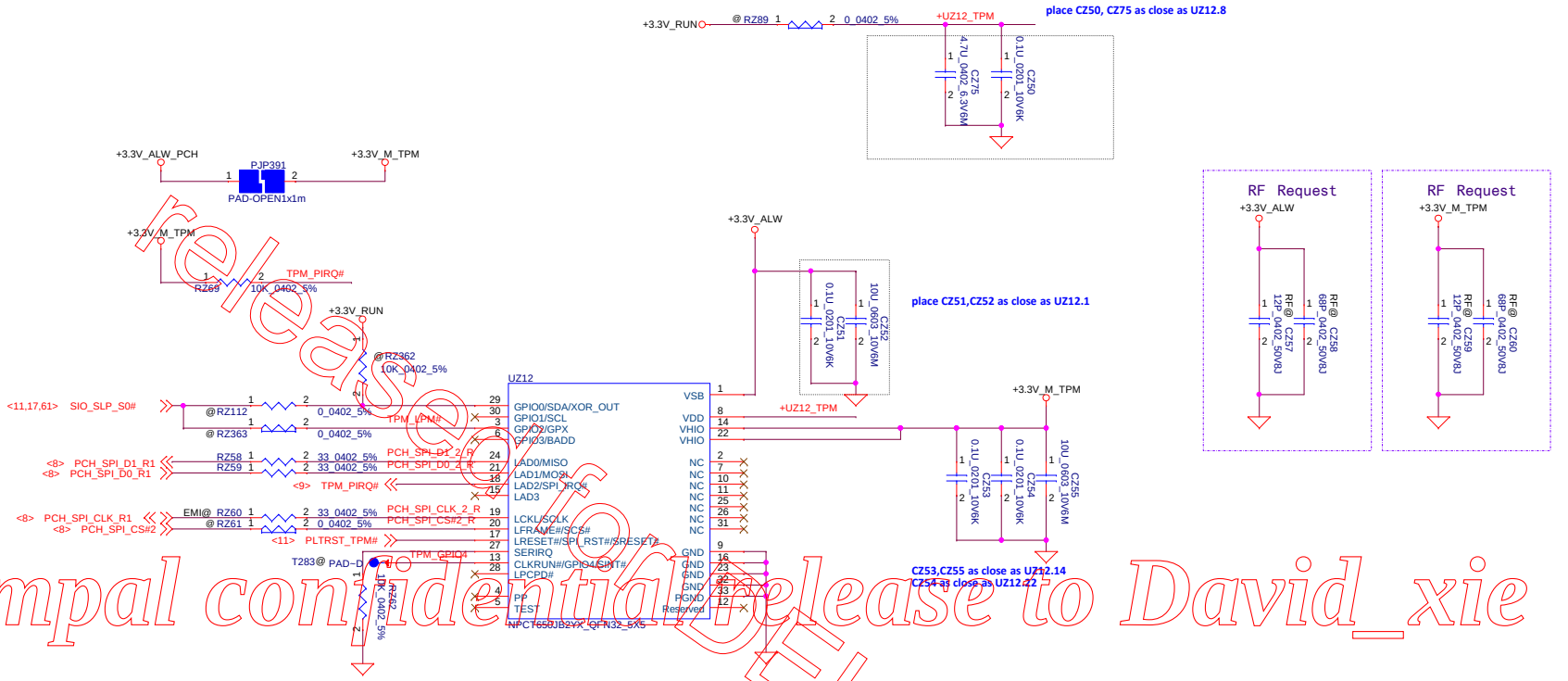
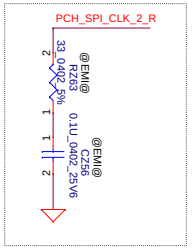
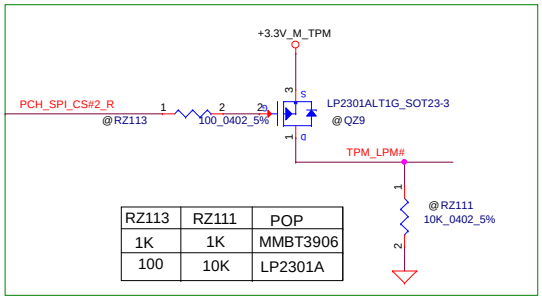
For NUVOTON TPM



JB2YX change to VB2YX 09/08





RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

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Title: USH & TPM

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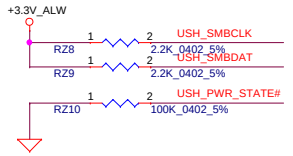
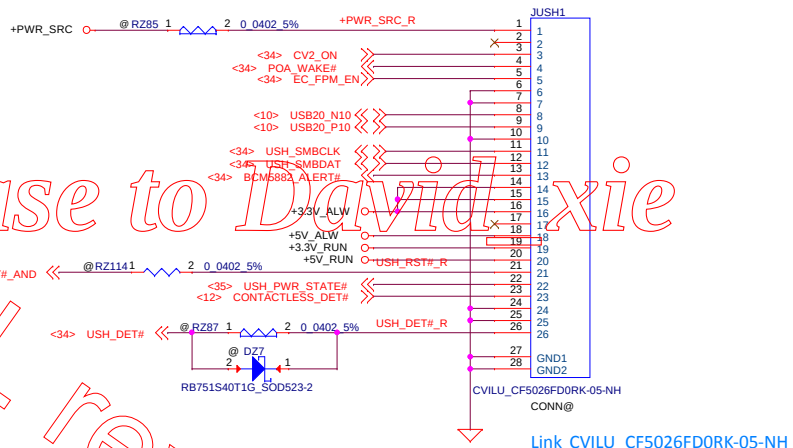
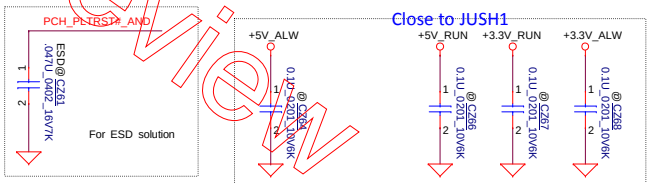
For ATMEL TPM

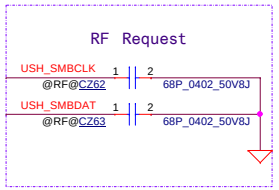


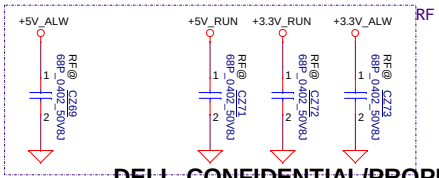
USH CONN



Link CVILU_CF5026FD0RK-05-NH







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Compal Electronics, Inc.	
Title	USH & TPM
Size	Document Number: LA-E092P
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For Parade 2 Lane solution

	PCIE/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check

Programmable output de-emphasis level setting for channel A
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Programmable output de-emphasis level setting for channel B
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
LL: -2dB
HL: -7.5dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

[A_EQ2,A_EQ1,A_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
LLL: For channel loss up to 17dB (default)
LHL: For channel loss up to 14dB
HLL: For channel loss up to 19dB
HHL: For channel loss up to 21dB
LLH: For channel loss up to 18dB
LHH: For channel loss up to 10dB
HLH: For channel loss up to 16dB
HHH: For channel loss up to 20dB

PCIE/SATA Repeater

PWD	Funtion
0	Normal mode(default)
1	power down mode

M2280_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIE

PCIE/SATA Repeater

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

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Compal Electronics, Inc.

Title: SATA/PCIE REPEATER for M.2 2280

Size: | Document Number: LA-E092P | Rev: 1.0

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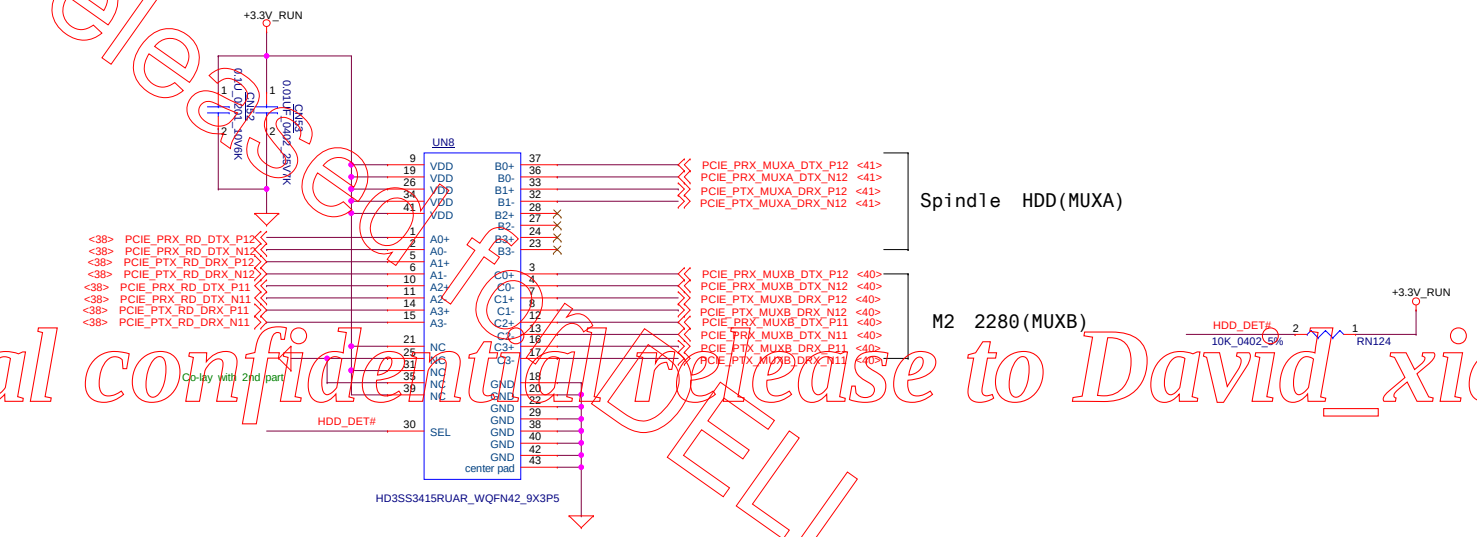
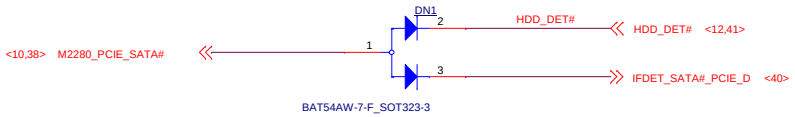
For Breckenridge 14/15 DSC

NEED LINK TI hd3ss3415 as main



IFDET_SATA#_PCIE	
L	SATA
H	PCIE

HDD_SEL(HDD_DET#)	
L	Spindle HDD(MUXA)
H	M.2 2280(MUXB)



Compal Electronics, Inc.

Title: SATA/PCIE DEMUX

Size | Document Number: LA-E092P | Rev: 1.0

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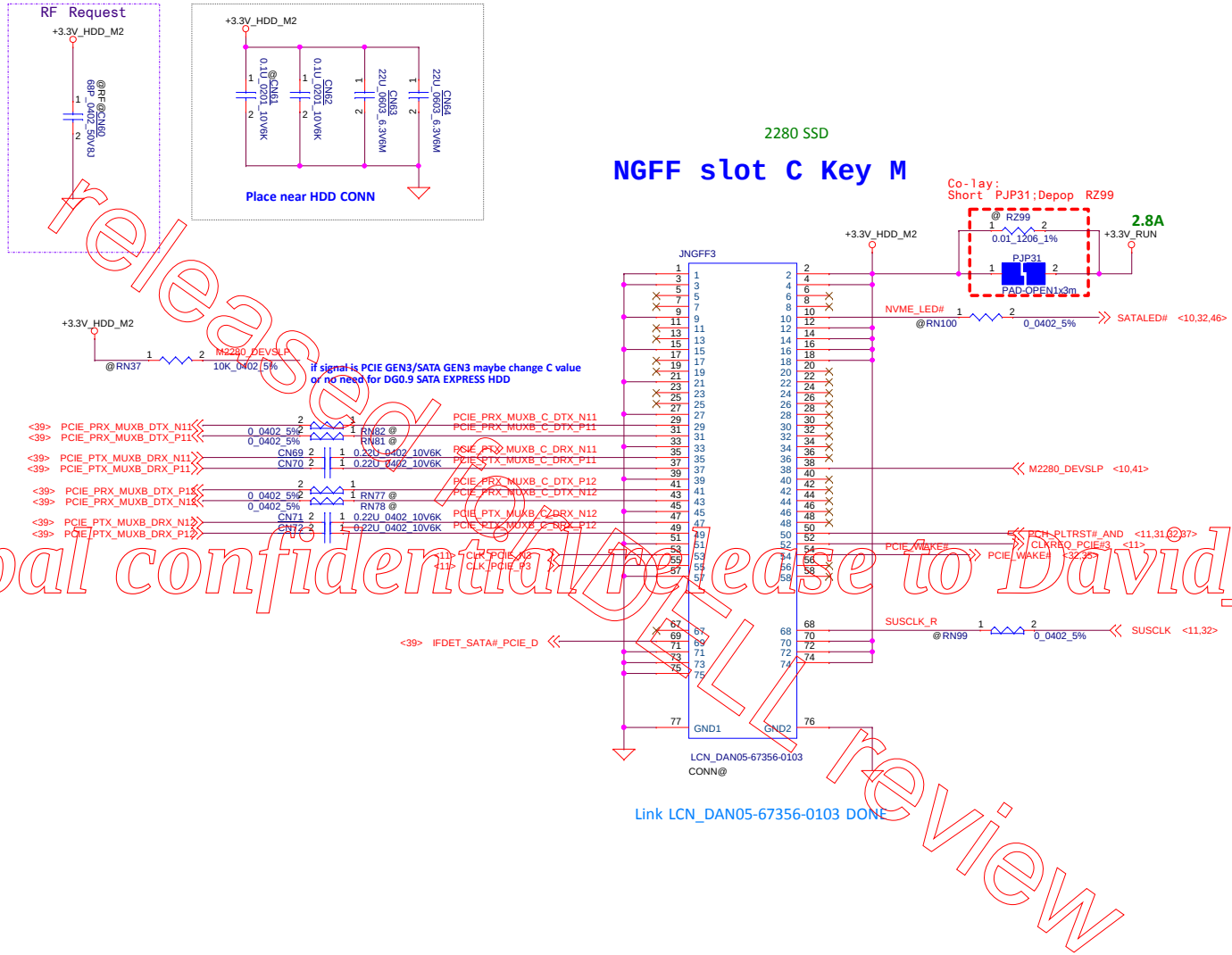

Compal Electronics, Inc.

Title: M2 2280 Socket

Size | Document Number: LA-E092P | Rev: 1.0

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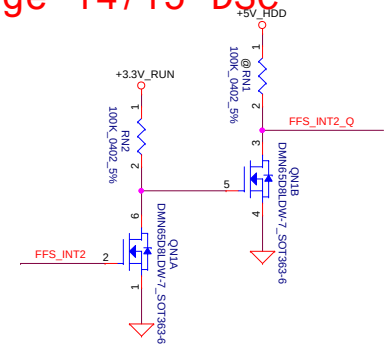
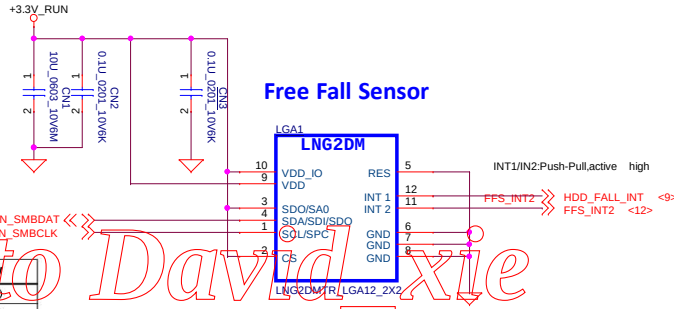
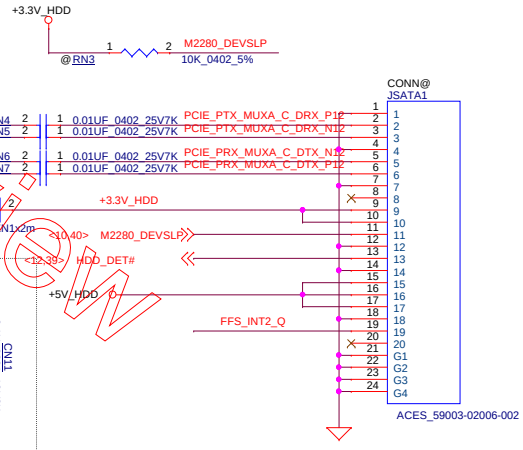
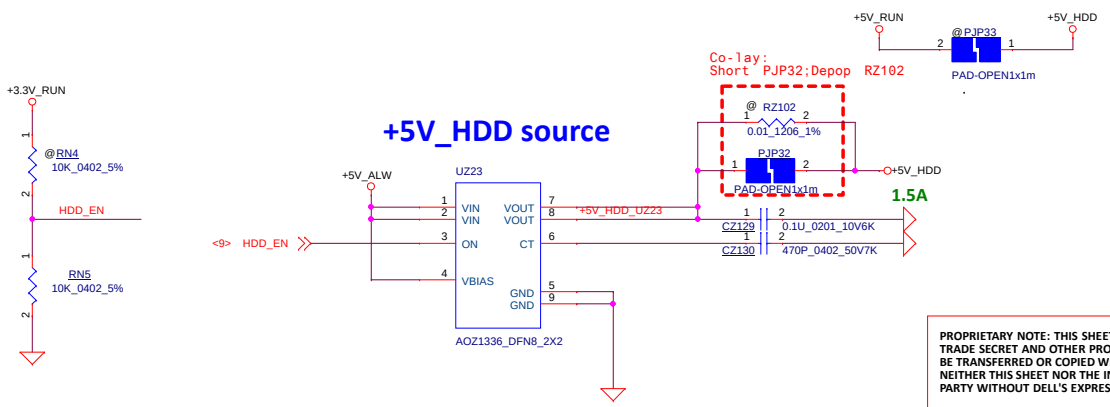
For Breckenridge 14/15 DSC





Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)





Compal Electronics, Inc.

Title: HDD CONN

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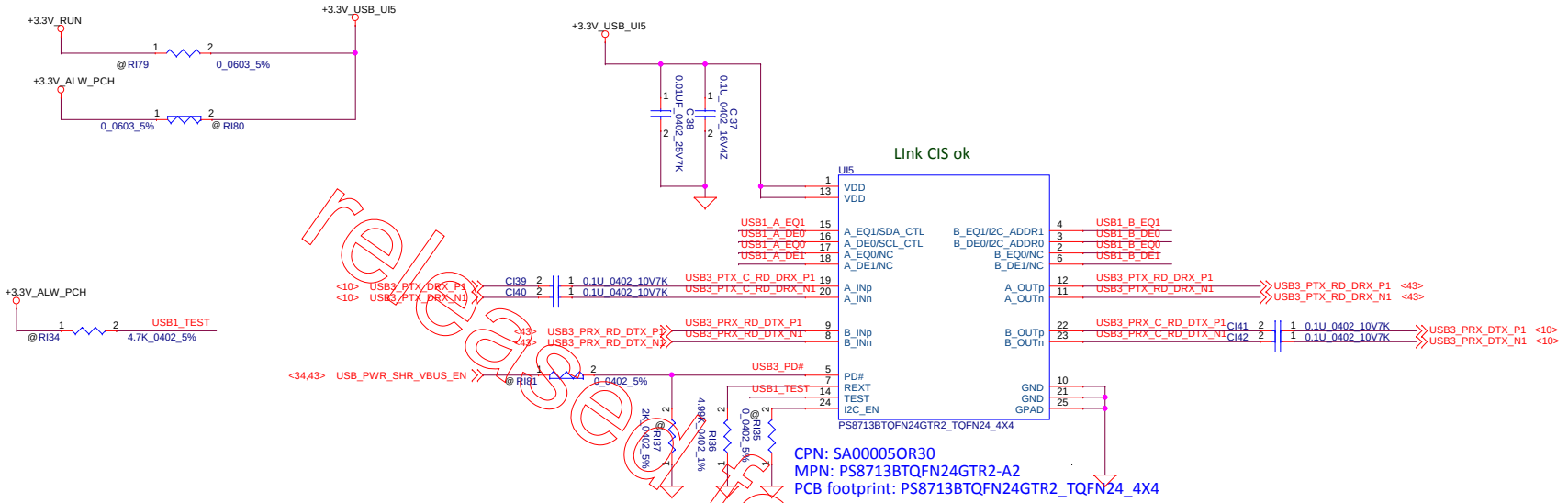
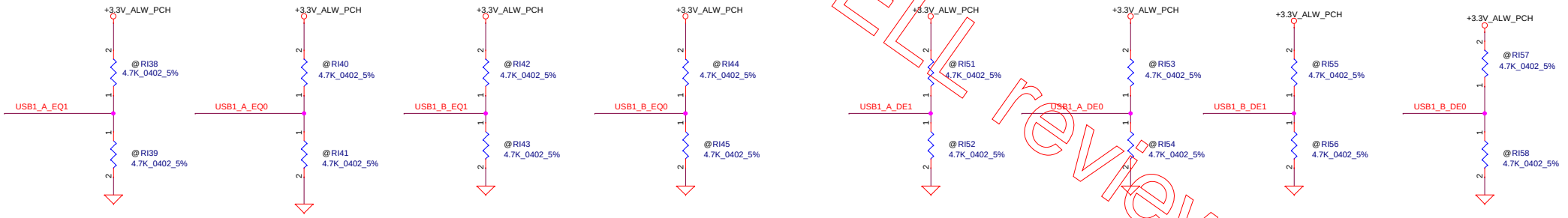
Date: Monday, December 12, 2016 | Sheet 41 of 76



CPN: SA00005OR30
MPN: PS8713BTQFN24GTR2-A2
PCB footprint: PS8713BTQFN24GTR2_TQFN24_4X4



Parade_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A_EQ&B_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A_DE&B_DE have internal pull-down 150k

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Compal Electronics, Inc.

Title: USB3.0 Repeater

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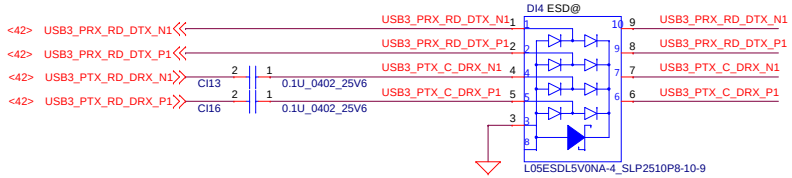
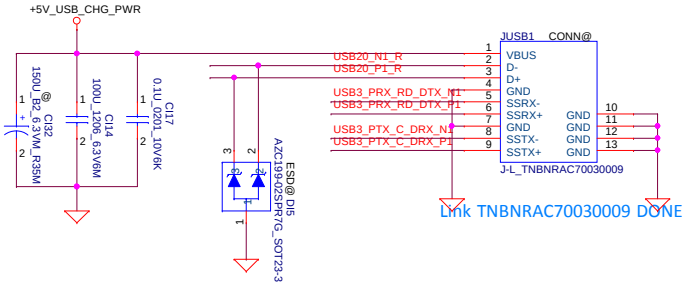
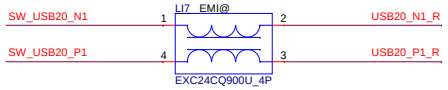
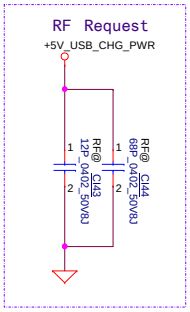
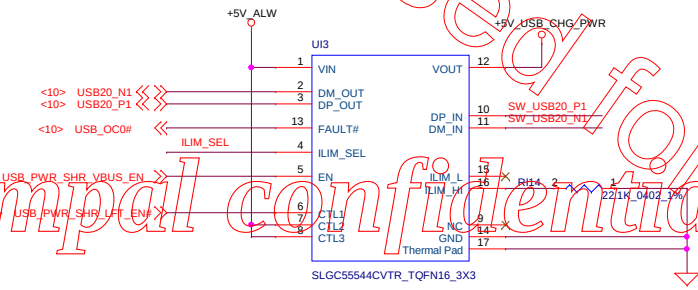
For w/ Repeater



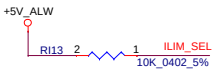


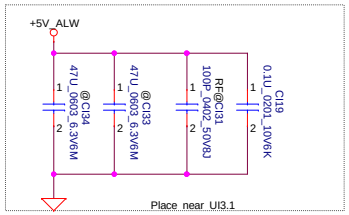






Link Seligro SA000097E10 Done
MAIN:SLGC55544CVTR





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Compal Electronics, Inc.

Title: JUSB1+PS

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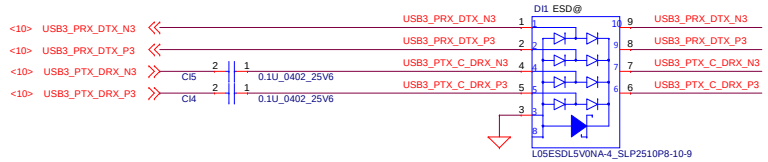
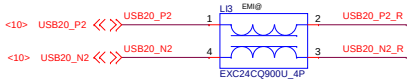
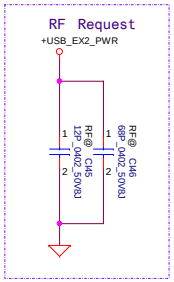
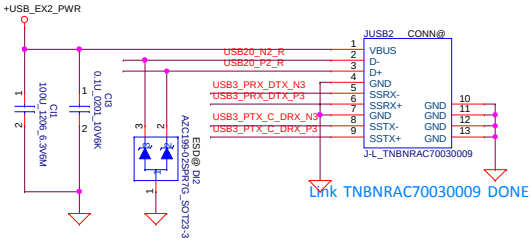
For Breckenridge 14&15/Steamboat 14



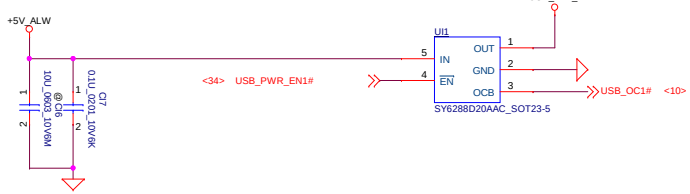


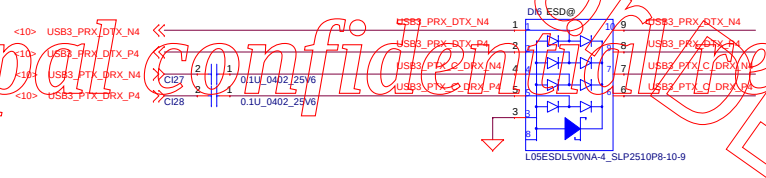


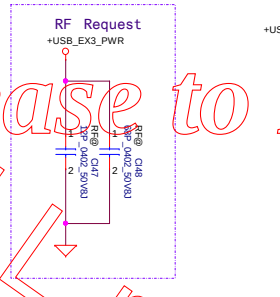


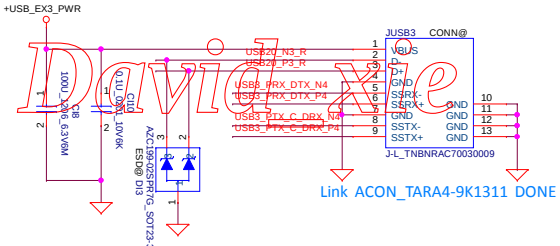
Link TNBNRAC70030009 DONE

DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

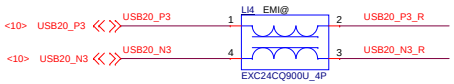


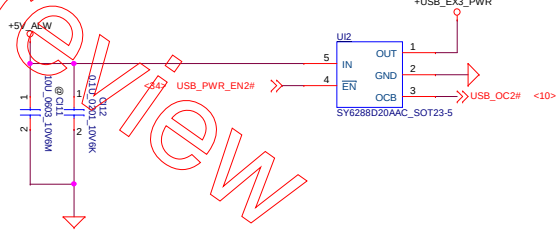






Link ACON_TARA4-9K1311 DONE





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Compal Electronics, Inc.

Title: JUSB2&JUSB3

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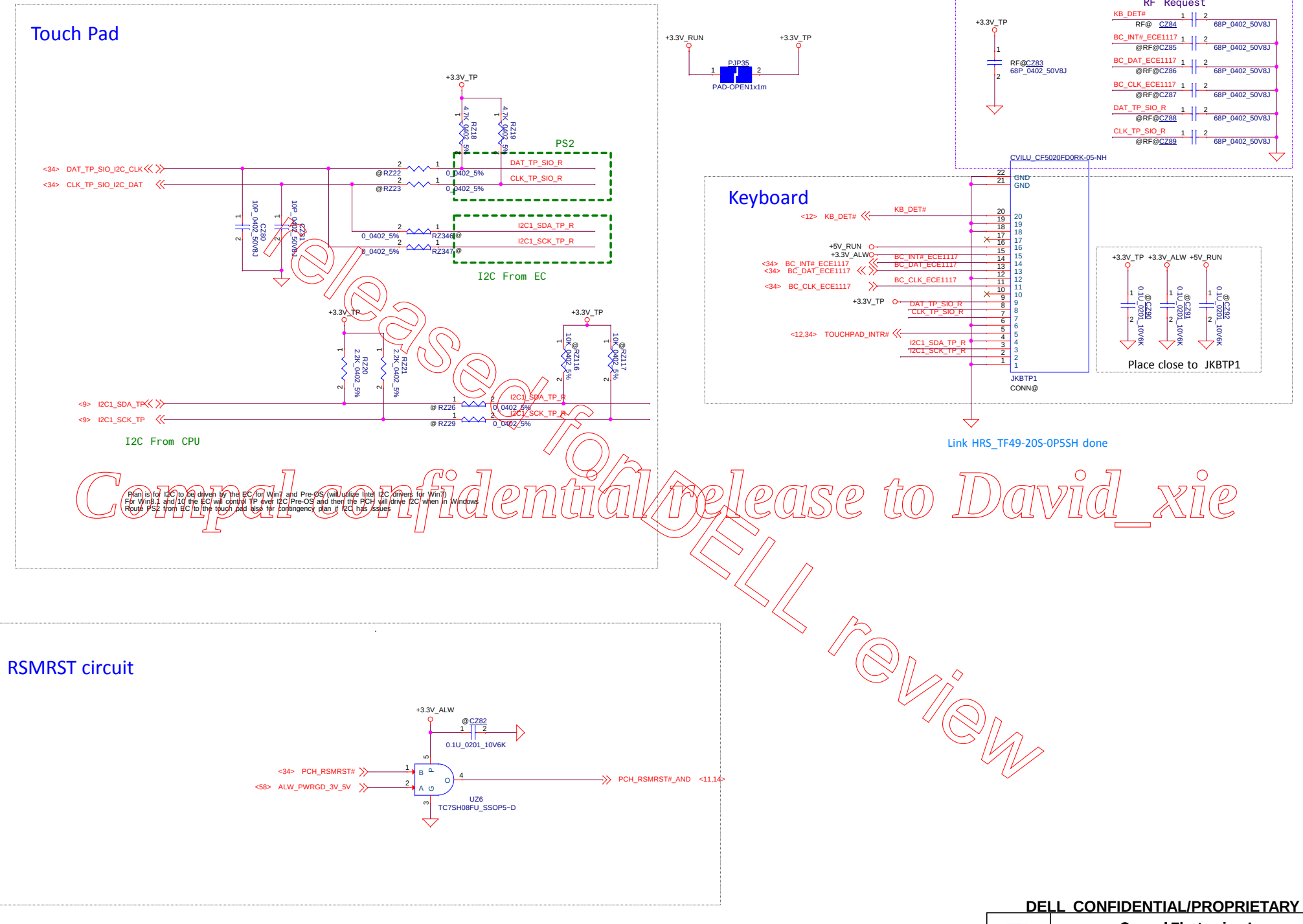

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Compal Electronics, Inc.	
Title	Keyboard
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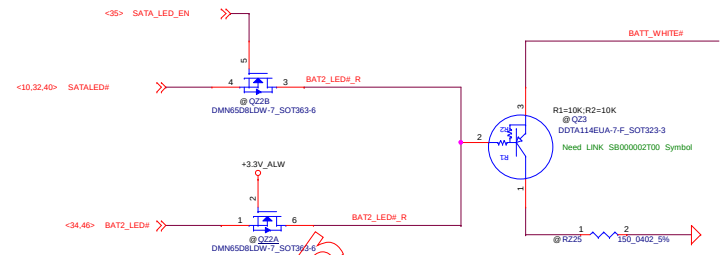
Bat t ery LE D

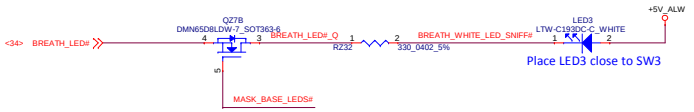
HDD LED MUX

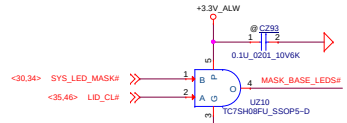
means EC can switch battery white led and HDD LED by hot key " Fn+F



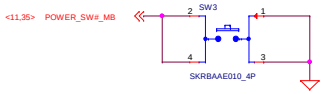
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

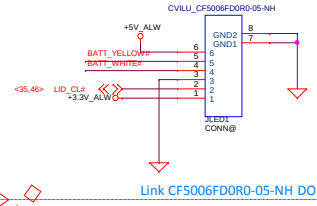




POWER & INSTANT ON SWITCH



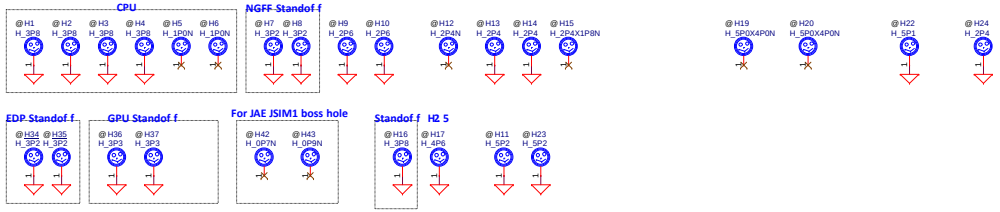
LED board CONN



Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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Compal Electronics, Inc.

Title: PAD, LED

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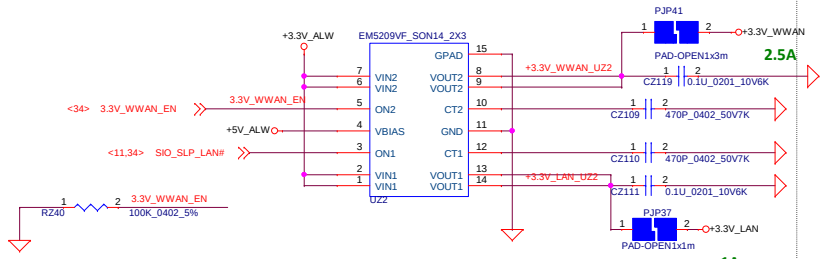
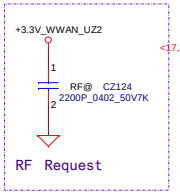
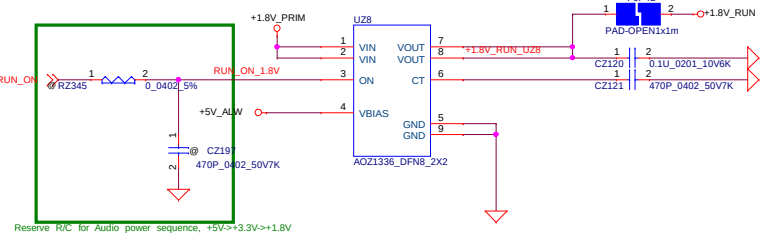
+3.3V_WWAN/+3.3V_LAN source

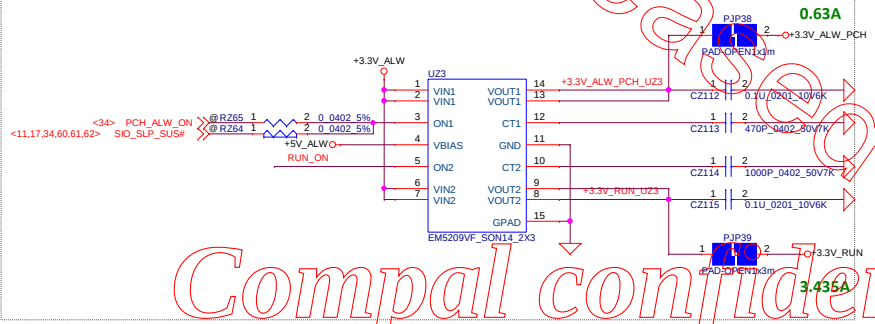




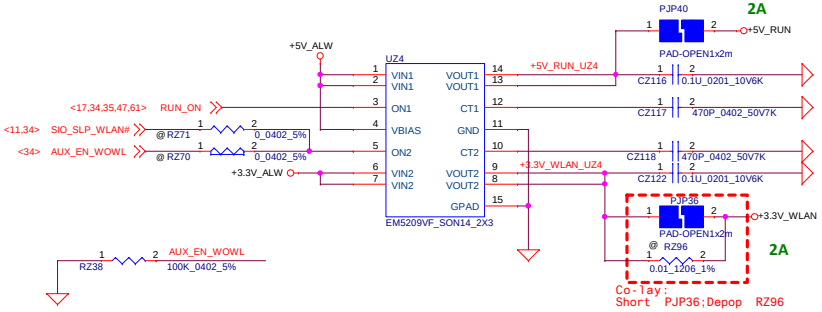
+1.8V_RUN source



+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WLAN source



Compal Electronics, Inc.	
Title	Power control
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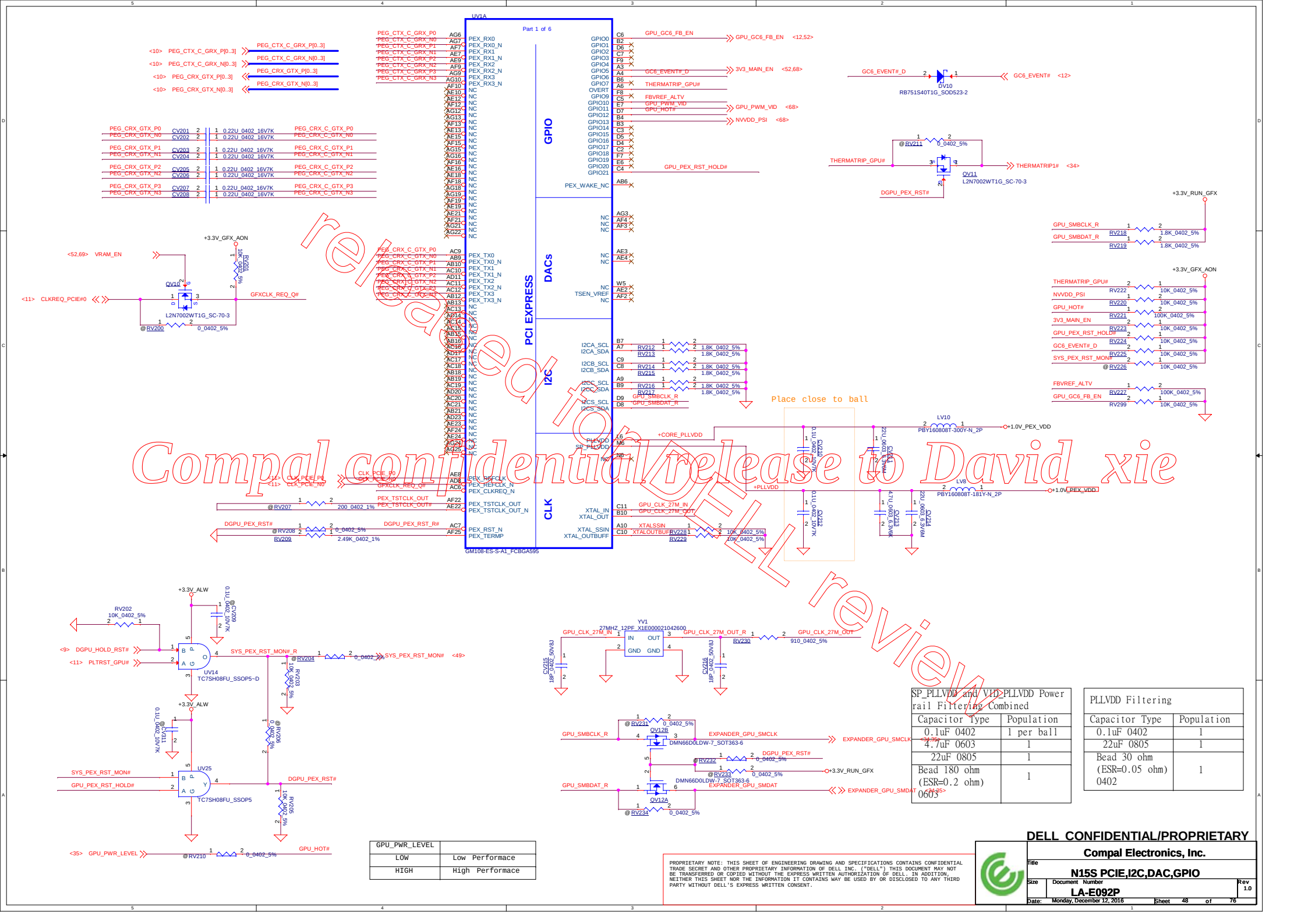


I2CS Slave Address

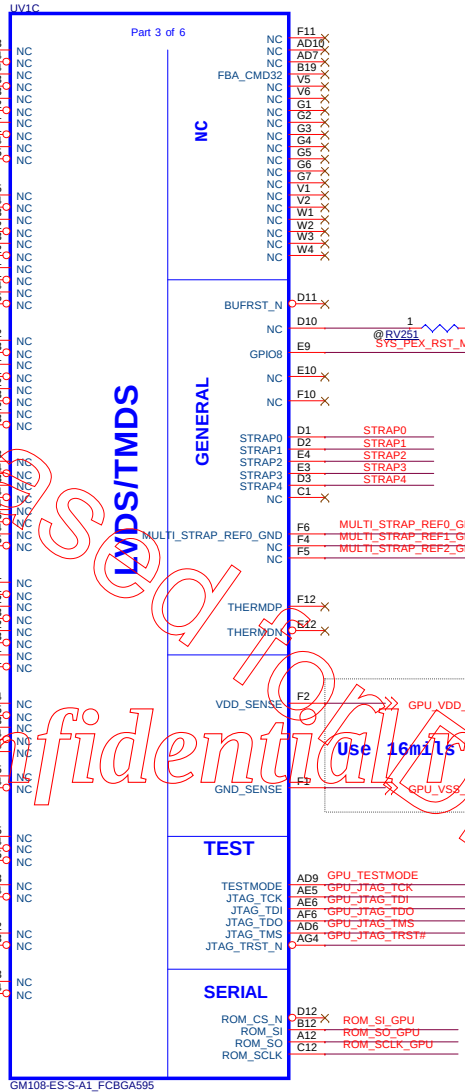
SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

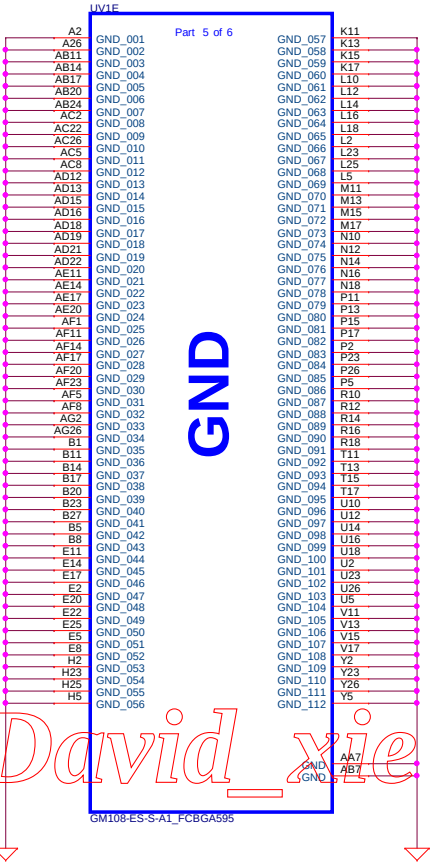
VGA_DEVICE Setting

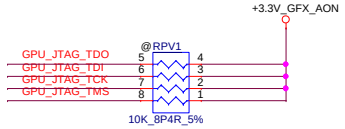
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

Resistance Mapping to Hex Values

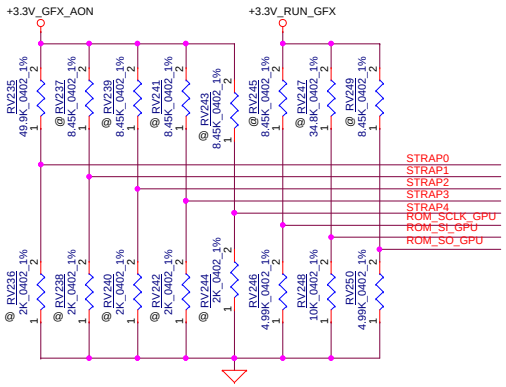
Resistor Value	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111







Decive ID change to 0x1056



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down RV246 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down RV248 24.9k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(defual)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down RV250 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up RV235 50k to +3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG defaul set 0, need refer Platform Update Notification for the latest configuration

VENDER	STRAP	Part Number	Note(ROM_SI)
Hynix	0x7	H5TC4G63CFR-N0C	RV248 45.3k PD
Micron	0x6	MT41J256M16LY-091G:N	RV248 34.8k PD
Samsung	0x1	K4W4G1646E-BC1A	RV248 10k PD

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Compal Electronics, Inc.

Title: N15S DP, STRAP, GND

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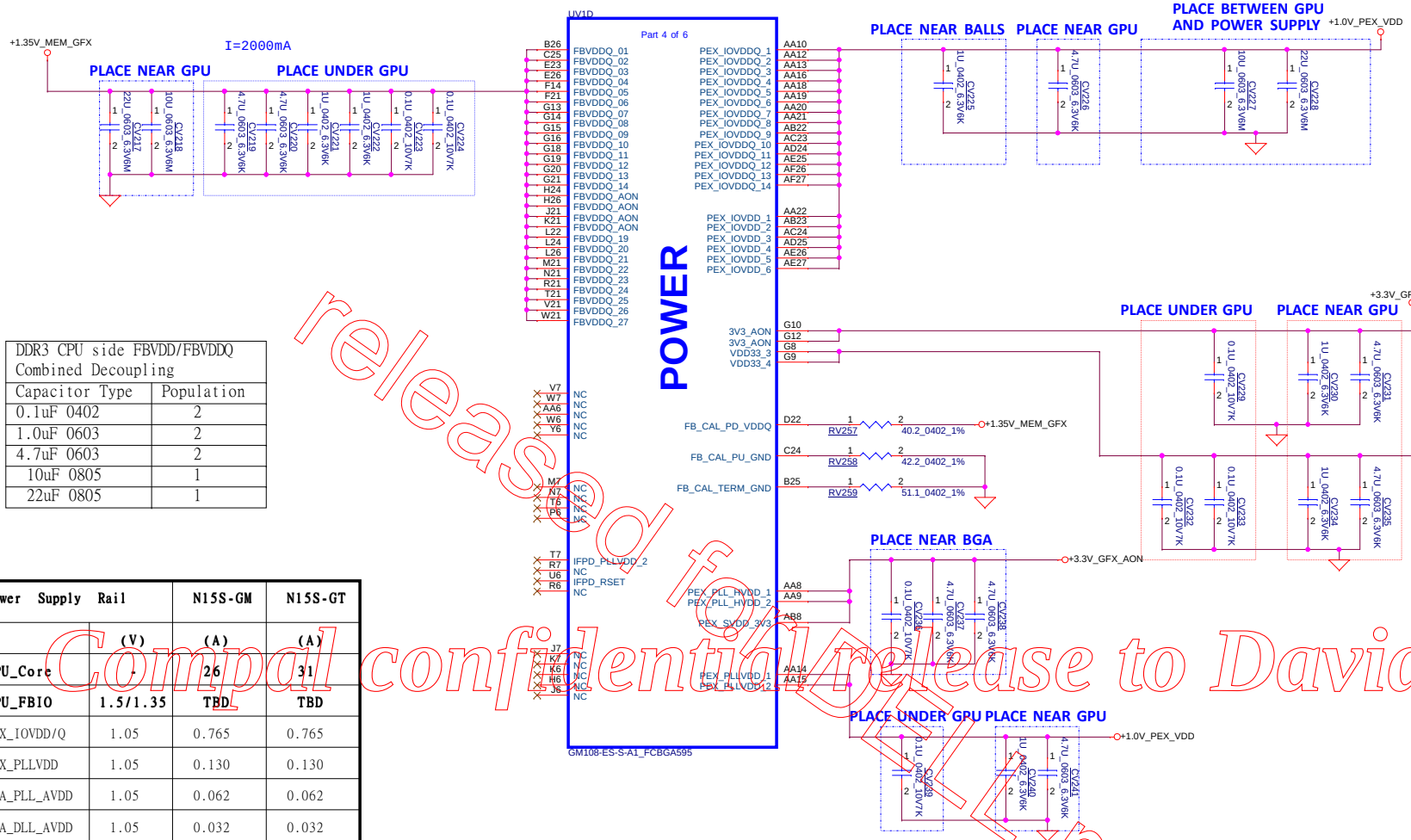

PEX_IOVDD/Q Power Rail Combined	
Capacitor Type	Population
1uF 0402	1
4.7uF 0603	1
10uF 0805	1
22uF 0805	1

DDR3 CPU side FBVDD/FBVDDQ Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	2
10uF 0805	1
22uF 0805	1

Power Supply Rail		N15S-GM	N15S-GT
	(V)	(A)	(A)
GPU_Core	-	26	31
GPU_FBIO	1.5/1.35	TBD	TBD
PEX_IOVDD/Q	1.05	0.765	0.765
PEX_PLLVDD	1.05	0.130	0.130
FBA_PLL_AVDD	1.05	0.062	0.062
FBA_DLL_AVDD	1.05	0.032	0.032
PLL_VDD	1.05	0.058	0.058
SP_PLLVDD	1.05	0.030	0.030
1.05V Total	1.05	1.060	1.060
VDD33+3V3AON	3.3	0.036	0.036
PEX_SVDD_3V3	3.3	0.167	0.167
PEX_PLL_HVDD	3.3	0.022	0.022
3.3V Total	3.3	0.225	0.025

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

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Compal Electronics, Inc.

Title: N15S Power

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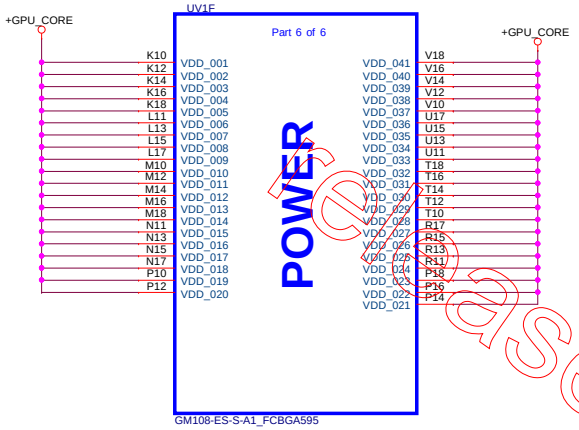
Caps on Power Side
1UX4 4.7UX10 under GPU
4.7UX5 22UX1 47UX2 330UX2 near GPU



Compal Electronics, Inc.

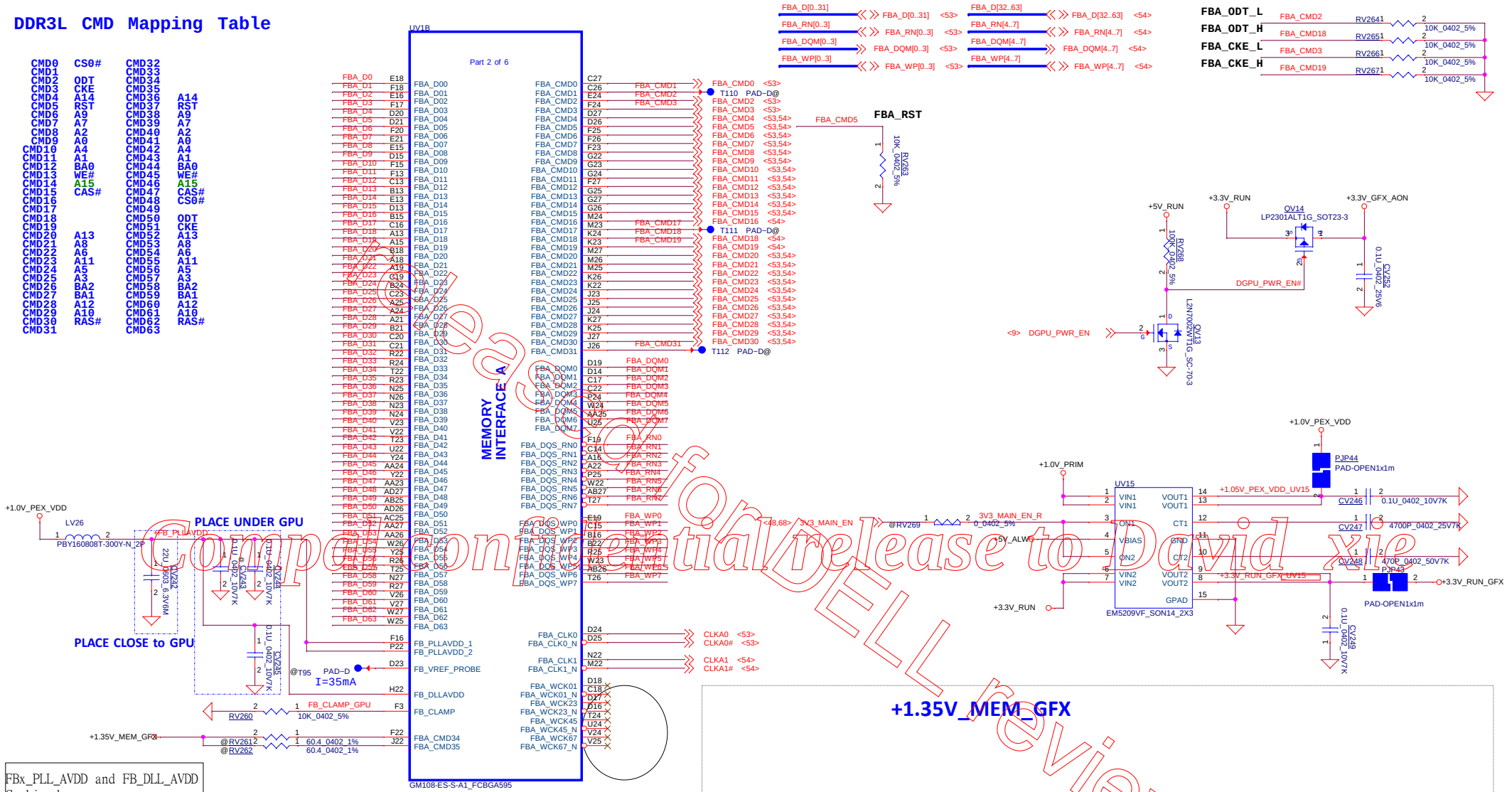
Title: N15S Power GFX Core

Size | Document Number: LA-E092P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 51 of 76

DDR3L CMD Mapping Table

CMD0	CS0#	CMD32		
CMD1		CMD33		
CMD2	ODT	CMD34		
CMD3	CKE	CMD35		
CMD4	A14	CMD36	A14	
CMD5	RST	CMD37	RST	
CMD6	A9	CMD38	A9	
CMD7	A7	CMD39	A7	
CMD8	A2	CMD40	A2	
CMD9	A0	CMD41	A0	
CMD10	A4	CMD42	A4	
CMD11	A1	CMD43	A1	
CMD12	BA0	CMD44	BA0	
CMD13	WE#	CMD45	WE#	
CMD14	A15	CMD46	A15	
CMD15	CAS#	CMD47	CAS#	
CMD16		CMD48	CS0#	
CMD17		CMD49		
CMD18		CMD50	ODT	
CMD19		CMD51	CKE	
CMD20	A13	CMD52	A13	
CMD21	A8	CMD53	A8	
CMD22	A6	CMD54	A6	
CMD23	A11	CMD55	A11	
CMD24	A5	CMD56	A5	
CMD25	A3	CMD57	A3	
CMD26	BA2	CMD58	BA2	
CMD27	BA1	CMD59	BA1	
CMD28	A12	CMD60	A12	
CMD29	A10	CMD61	A10	
CMD30	RAS#	CMD62	RAS#	
CMD31		CMD63		



FBx_PLL_AVDD and FB_DLL_AVDD Combined	
Capacitor Type	Population
0.1uF 0402	2
22uF 0805	1
Bead 30 ohm (ESR=0.01 ohm) 0603	1

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Compal Electronics, Inc.

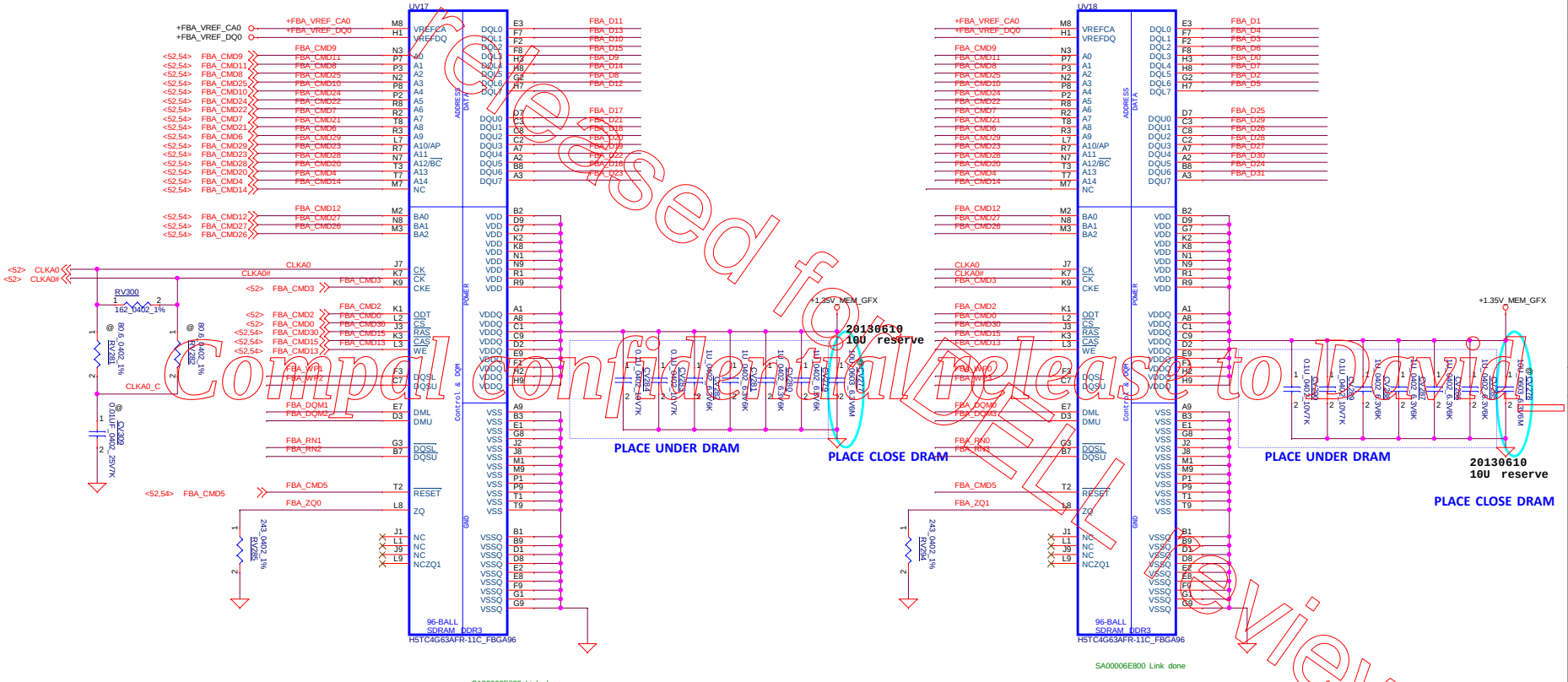
Title: N15S Memory

Size | Document Number: LA-E092P | Rev: 1.0

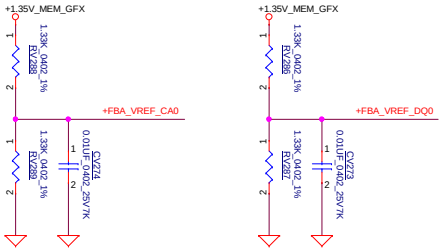
Date: Monday, December 12, 2016 | Sheet 52 of 76

Memory Partition A - Upper 16 bits

256x16 DDR3L



DDR3 per Memory FBVDD/Q Decoupling	
FBVDD/Q Combined	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	4
10uF 0805	0



Compal Electronics, Inc.

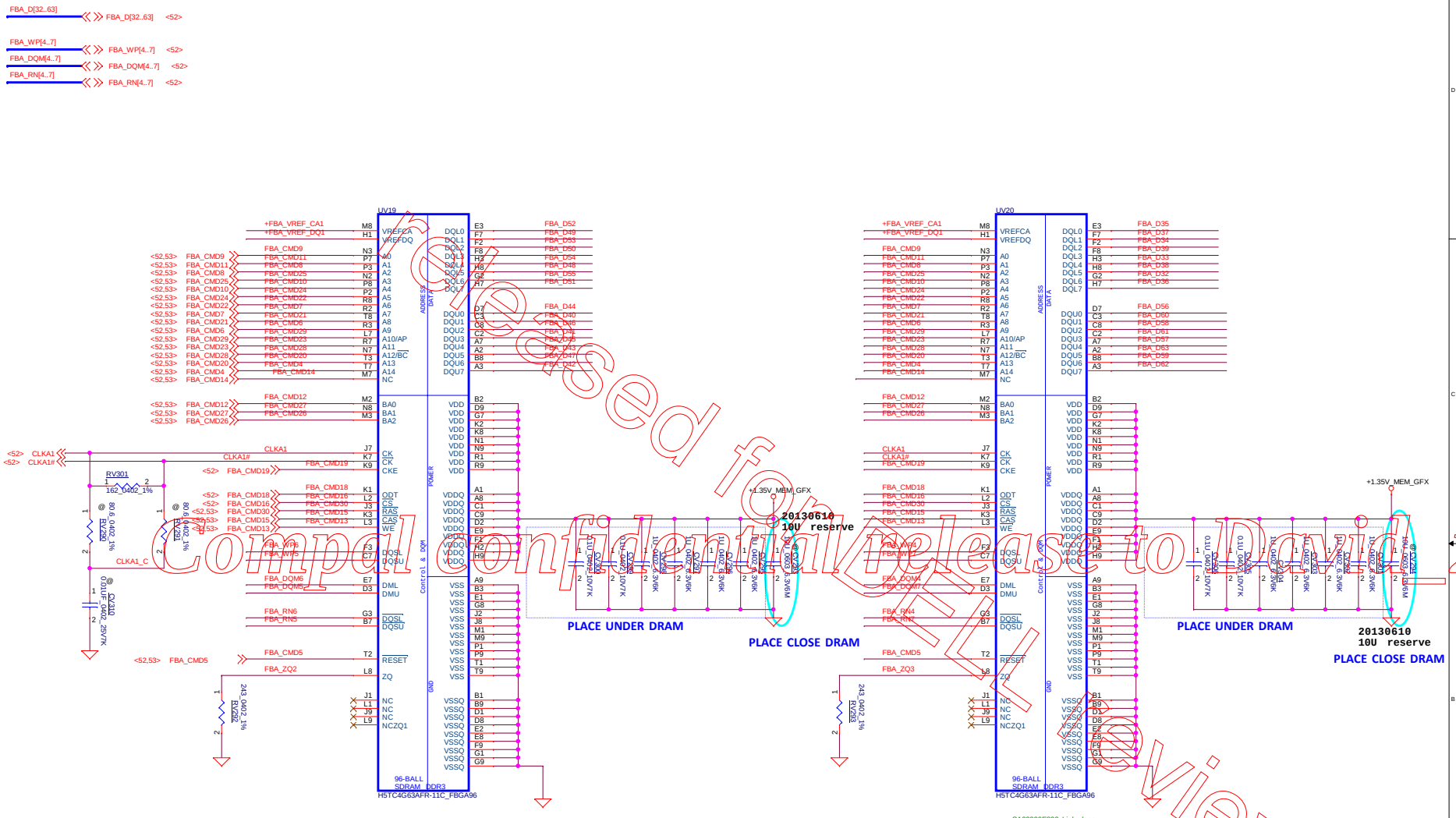
Title: MARX-VRAM_A Lower

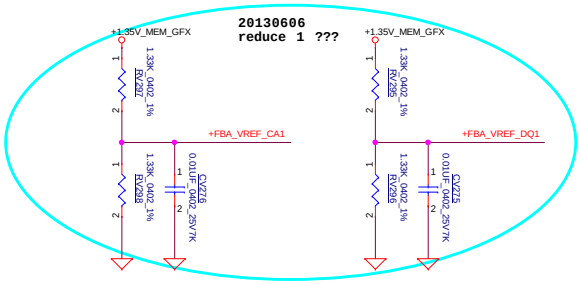
Size: | Document Number: LA-E092P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 53 of 76

Memory Partition A - Lower 16 bits

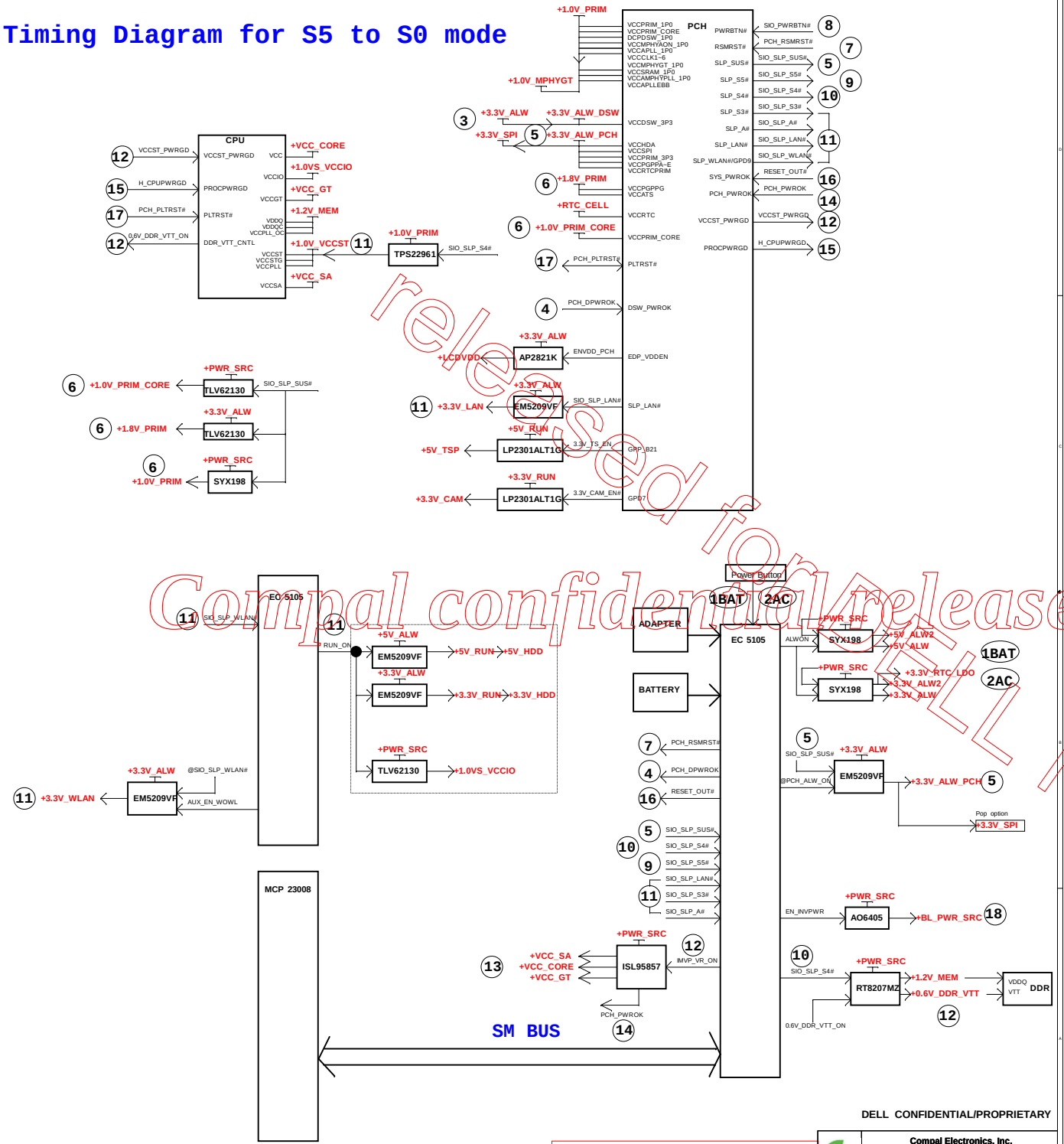
256x16 DDR3L





Compal Electronics, Inc.		
Title: MARX-VRAM_A Lower		
Size	Document Number: LA-E092P	Rev: 1.0
Date: Monday, December 12, 2016	Sheet 54 of 76	

Timing Diagram for S5 to S0 mode



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Compal Electronics, Inc.

Title: Power Sequence

Size: Document Number: LA-E071P — Rev: 1.0

Date: Monday, December 12, 2016 — Sheet 55 of 76

1

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	40 ± 4 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm Single-end	52 ± 5.2 ohm Single-end	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref
			SolderMask	GA-150LL	0.50	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	
			Add Plating		0.95								SE 50				
1	Top		Copper foil	0.5oz	0.65	6.6	5.3	4.2	3.9	4.4/3.5	4/3.5	3.8/3.5	4.2/4.2	3.5/3..6	3.5/3.9	3.5/7.1	L2
		3.7	Prepreg	1086	2.65	39.94	44.57	50.16	51.84	80.13	83.26	84.93	84.93	88.19	89.84	99.93	
2	GND1		Copper foil	1oz	1.25												
		3.8	Core	3mil	3.00								SE 50				
3	Sig 1		Copper foil	1oz	1.25	6	4.8	3.9	3.5	4/3.5	3.7/3.5	3.5/3.6	3.9/4.4	3.5/4.2	3.5/4.7	3.5/9.6	L2/L4
		3.7	Prepreg	7628+1080	10.95	40.13	45.06	49.72	52.16	80.22	85.65	85.01	85.09	87.98	90.04	99.97	
4	GND/PWR		Copper foil	1oz	1.25												
		3.8	Core	3mil	3.00								SE 50				
5	Sig2		Copper foil	1oz	1.25	6.3	5	4	3.6	4/3.5	3.7/3.5	3.5/3.6	4/4.6	3.5/4.2	3.5/4.7	3.5/9.2	L4/L7
		3.8	Prepreg	7628+1080	10.28	39.87	44.94	49.94	52.3	80.16	82.61	84.91	84.99	87.93	90.03	99.97	
6	Sig3		Copper foil	1oz	1.25	6.3	5	4	3.6	4/3.5	3.7/3.5	3.5/3.6	4/4.6	3.5/4.2	3.5/4.7	3.5/9.2	L4/L7
		3.8	Core	3mil	3.00												
7	GND2		Copper foil	1oz	1.25												
		3.7	Prepreg	1086	2.65								SE 50				
8	Bottom		Copper foil	0.5oz	0.65	6.6	5.3	4.2	3.9	4.4/3.5	4/3.5	3.8/3.5	4.2/4.2	3.5/3..6	3.5/3.9	3.5/7.1	L7
			Add Plating		0.95	39.94	44.57	50.16	51.84	80.13	83.26	84.93	84.93	88.19	89.84	99.93	
			SolderMask		0.50												
Overall Thickness (1.2mm ± 10%)			47.2		47.23000												
					1.199642												

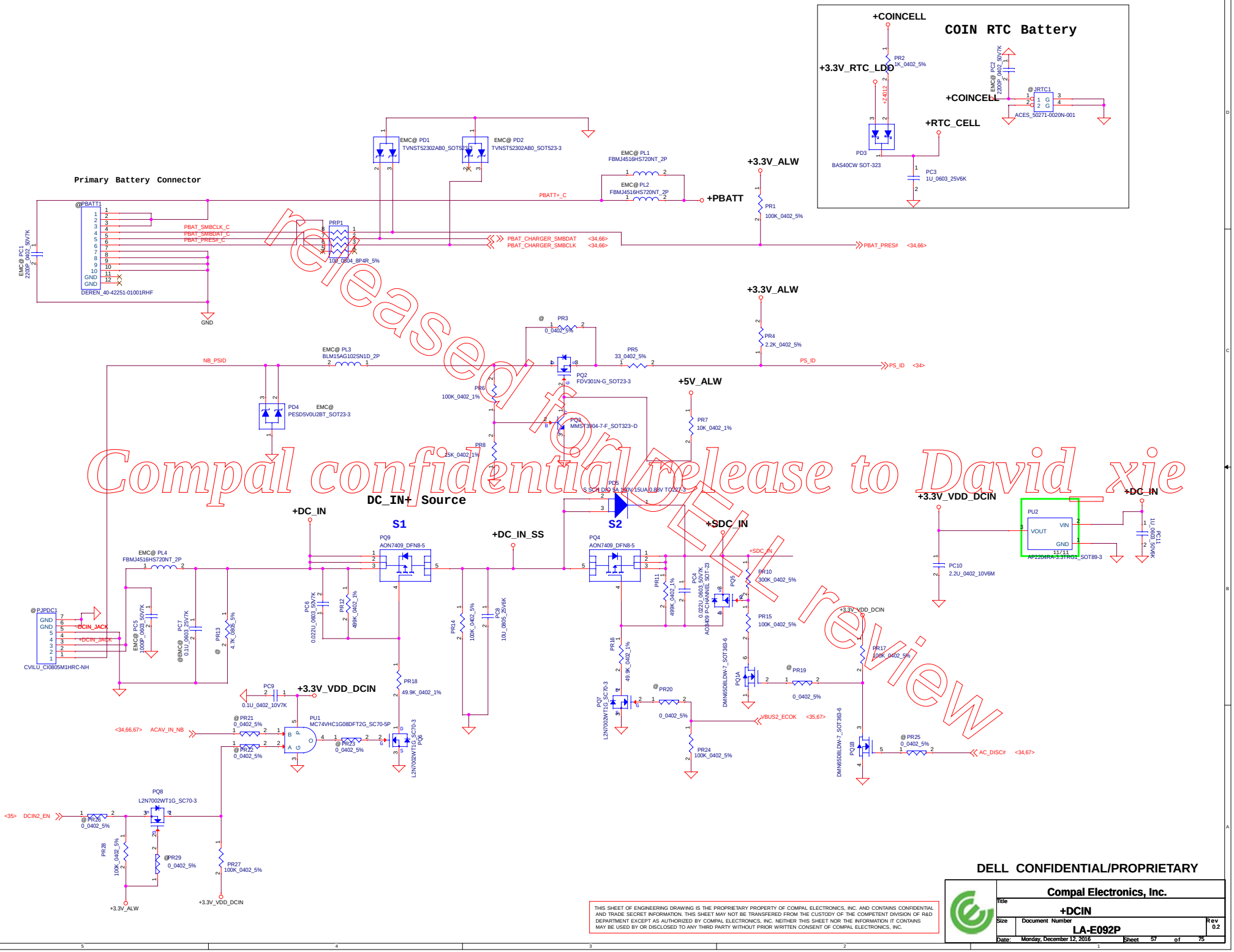
40 ± 4 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm single-end	52 ± 5.2 ohm single-end	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	88 ± 8.8 ohm Diff.	88 ± 8.8 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref
trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
									12/5	no Ref
									100.75	
									11/6.5	no Ref
									99.63	
6	4.8	3.8	3.5	4/3.5	3.7/3.5	3.5/3.6	3.5/4.2	L4/L6	10/6.5	no Ref
39.87	44.8	50.03	51.88	80.1	82.59	84.91	87.85		99.46	
6	4.8	3.8	3.5	4/3.5	3.7/3.5	3.5/3.6	3.5/4.2	L5/L7	10/6.5	no Ref
									12/5	no Ref
									100.75	

Compal Electronics, Inc.

Title: Stack-up

Size | Document Number: LA-E092P | Rev: 1.0

Date: Monday, December 12, 2016 | Sheet 56 of 76



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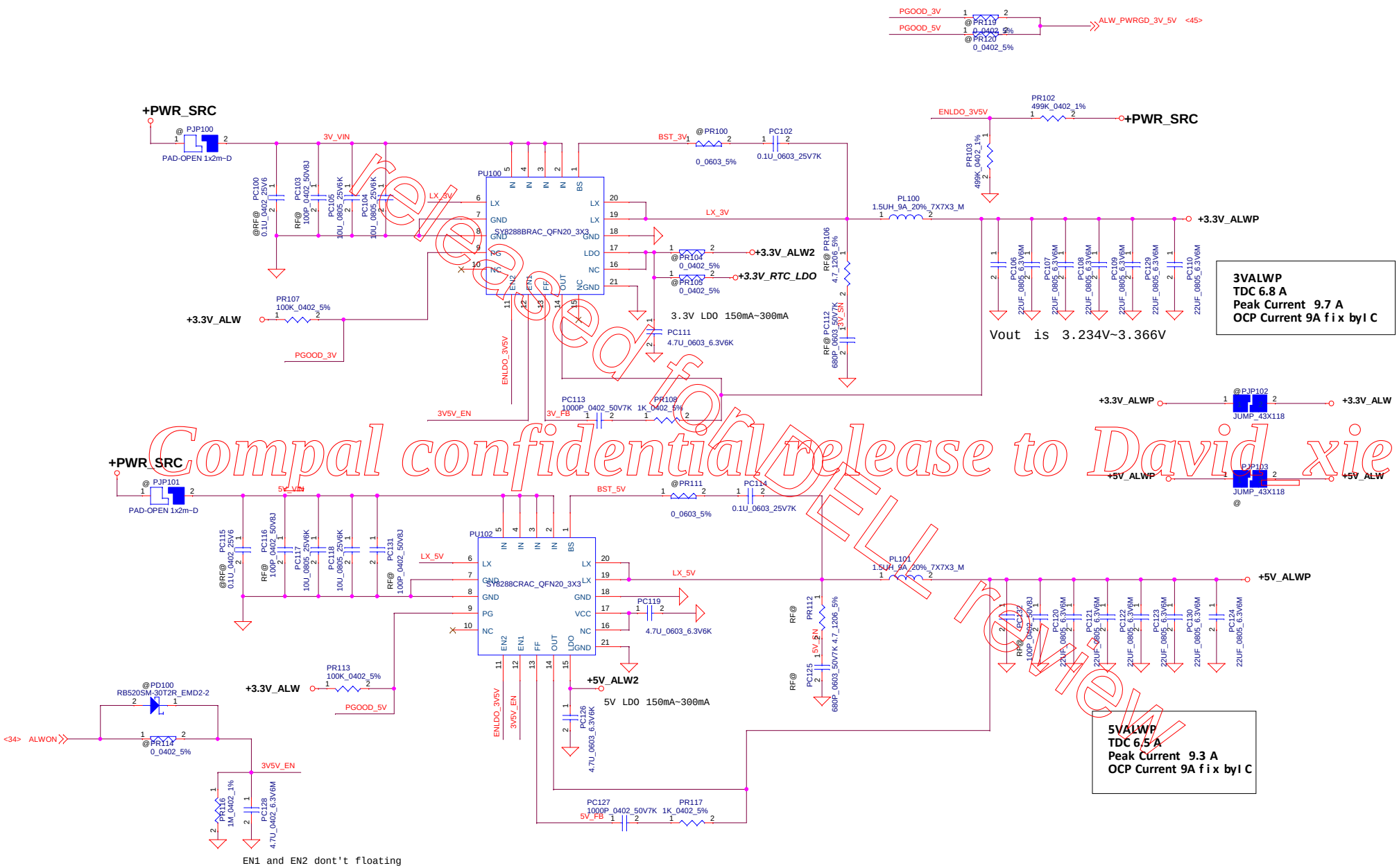
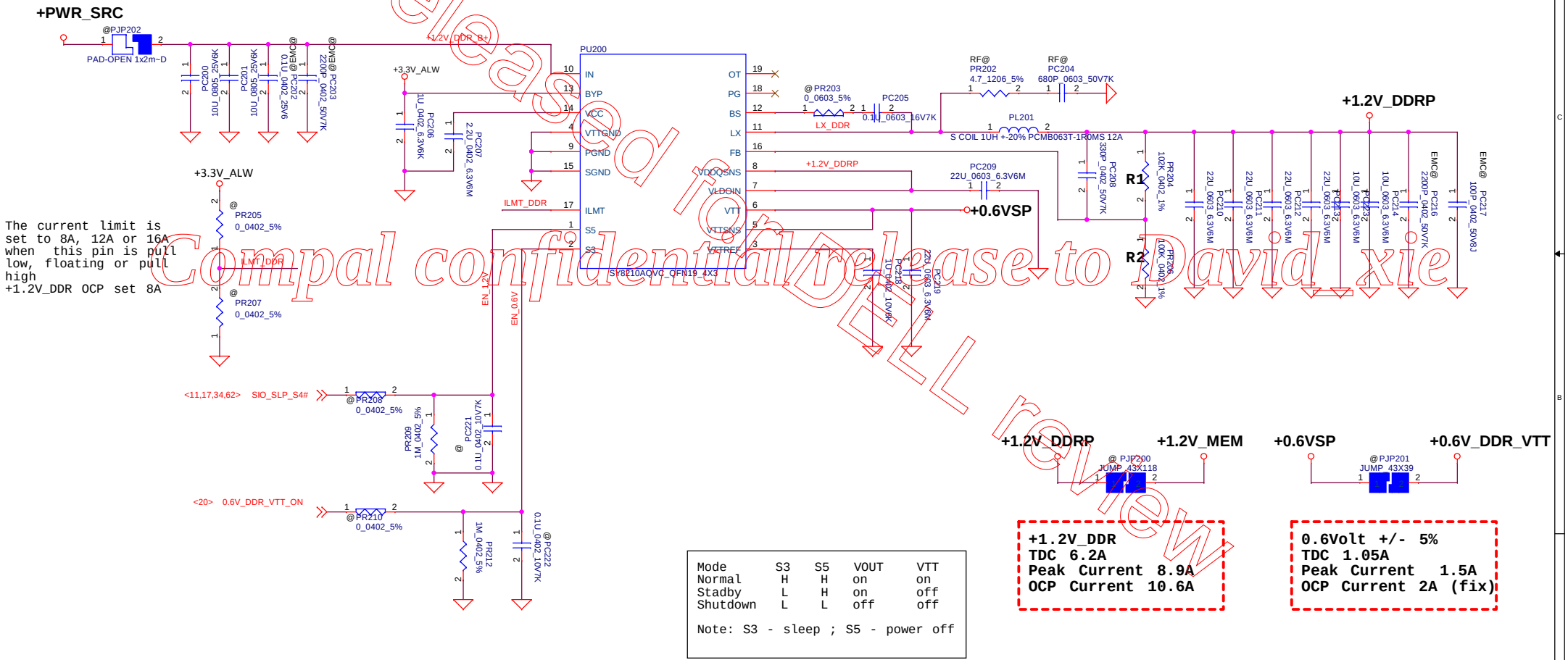
Compal Electronics, Inc.			
Title: +DCIN			
Size	Document Number: LA-E092P		Rev: 0.2
Date: Monday, December 12, 2016	Sheet 57 of 75		



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-E092P
Rev	0.2
Date:	Monday, December 12, 2016
Sheet	58 of 75



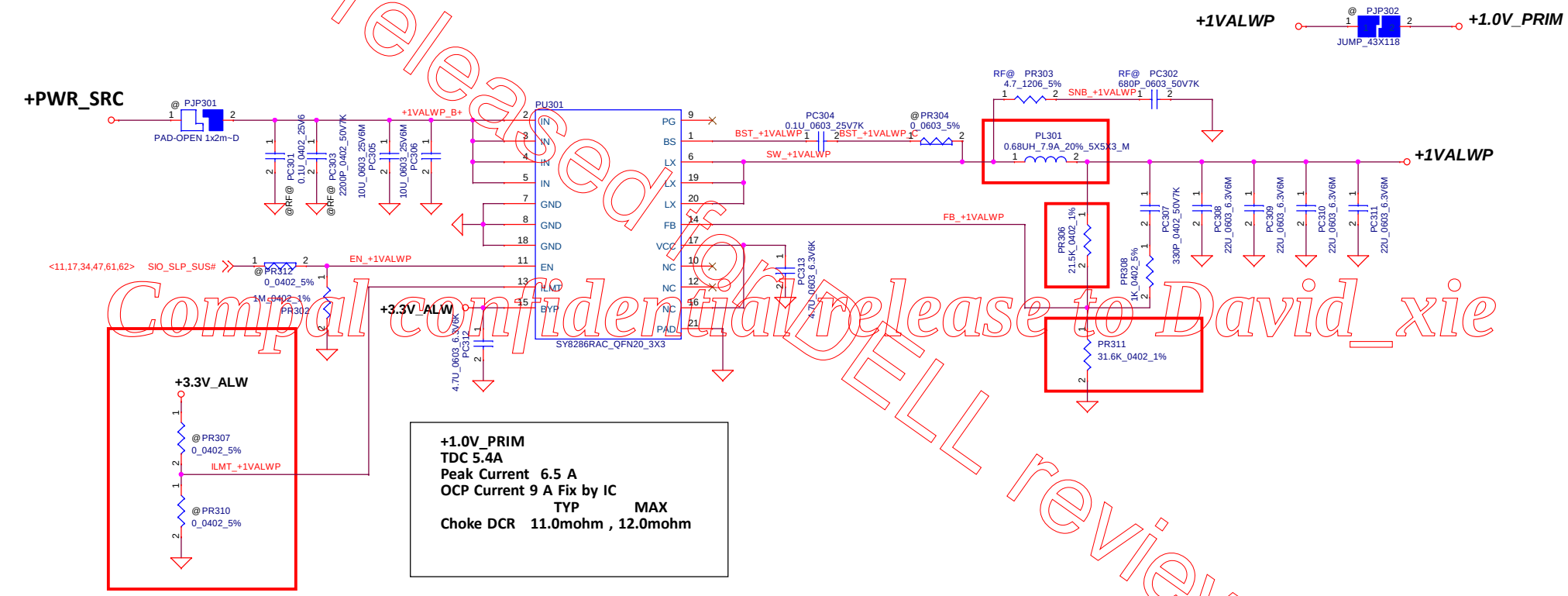
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size | Document Number: LA-E092P | Rev: 0.2

Date: Monday, December 12, 2016 | Sheet 59 of 75



+1.0V_PRIM
TDC 5.4A
Peak Current 6.5 A
OCP Current 9 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm , 12.0mohm	

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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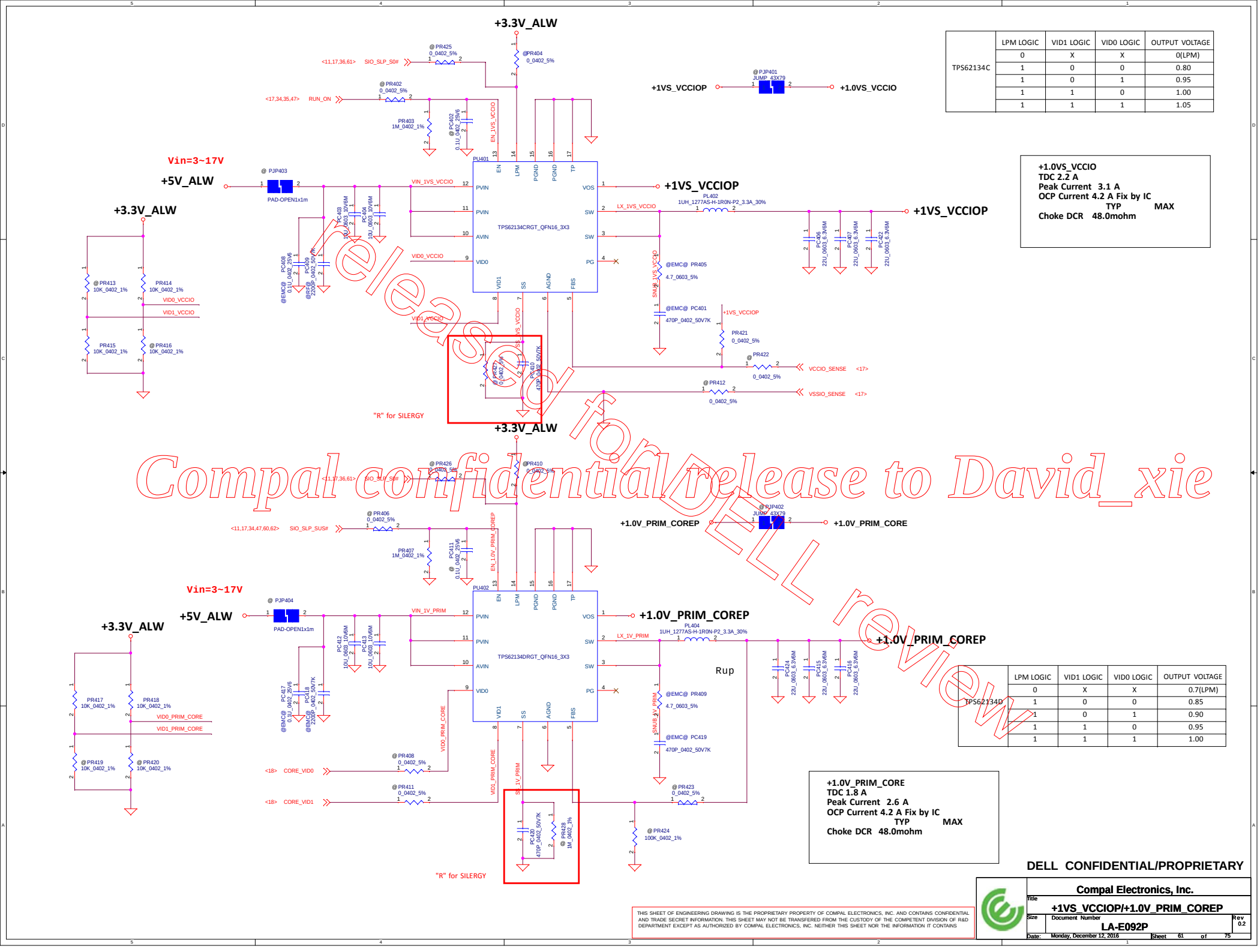
Compal Electronics, Inc.

Title	+1VALWP	
Size	Document Number LA-E082P	Rev 0.1
Date: Monday, December 12, 2016	Sheet 60 of 75	



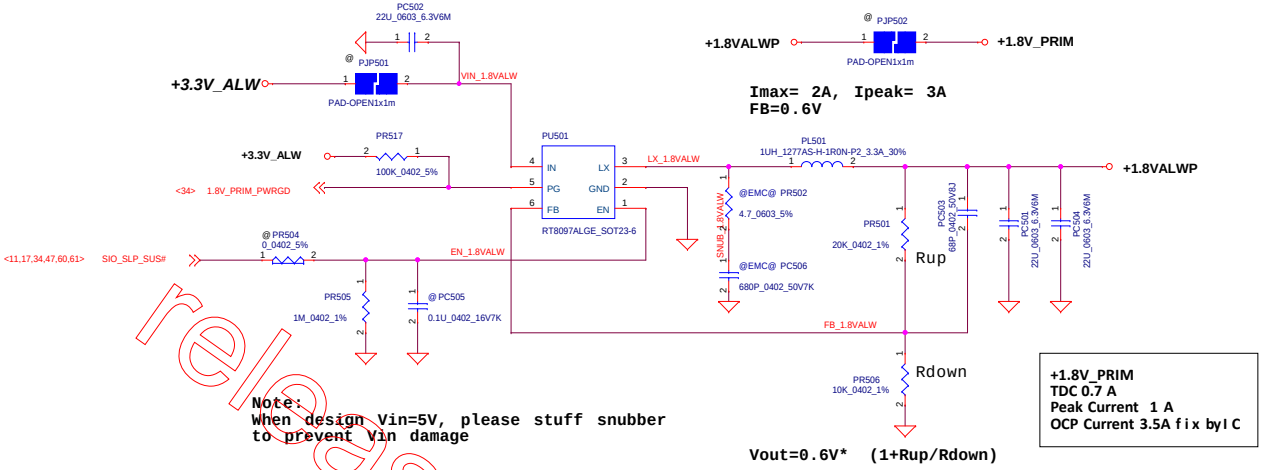
TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

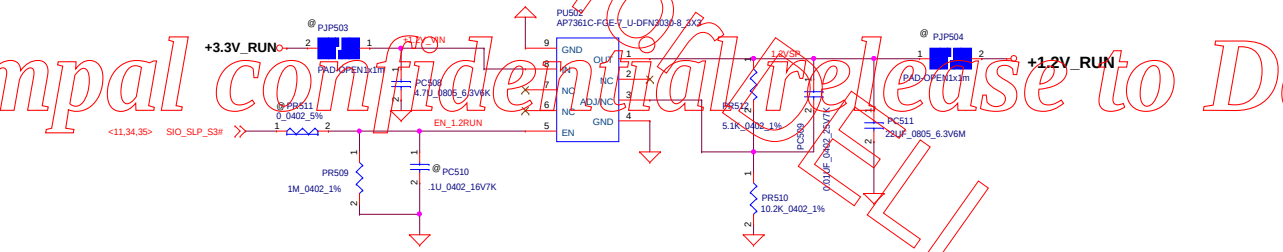
+1.0VS_VCCIO
TDC 2.2 A
Peak Current 3.1 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

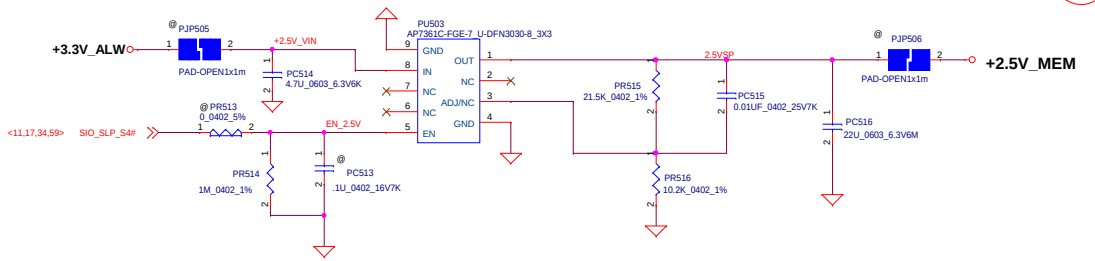
TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

Compal Electronics, Inc.
Title: +1VS_VCCIOP/+1.0V_PRIM_COREP
Size: Document Number: LA-E092P
Rev: 0.2
Date: Monday, December 12, 2016 Sheet 61 of 75





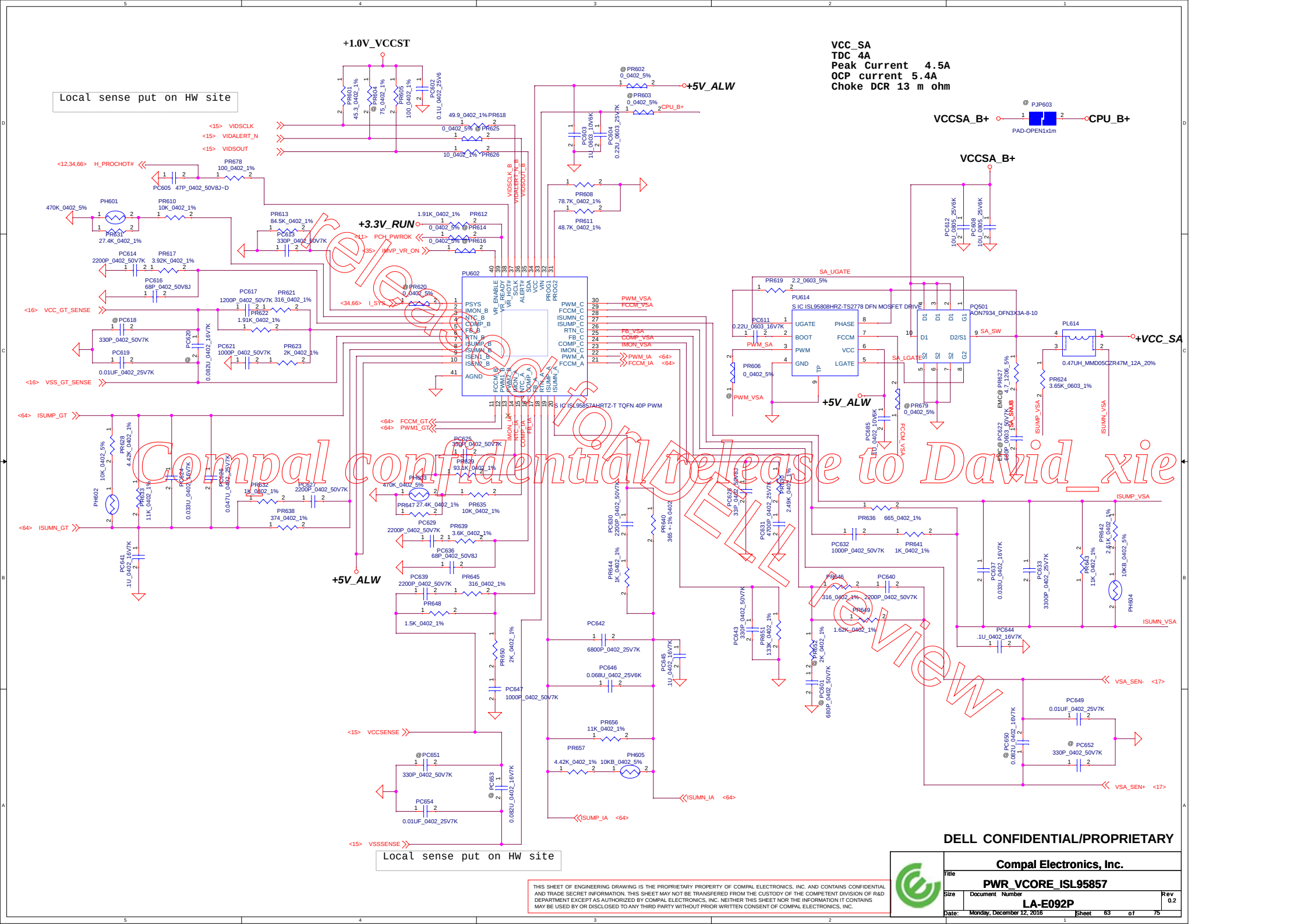


Compal Electronics, Inc.

Title: +1.8VALWP/+1.2V_RUN/2.5V_MEM

Size | Document Number: LA-E092P | Rev: 0.2

Date: Monday, December 12, 2016 | Sheet 62 of 75


+1.0V_VCCST
Local sense put on HW site
VCC_SA
TDC 4A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
VCCSA_B+
CPU_B+
PAD-OPEN1x1m
+5V_ALW
+3.3V_RUN
PU602
S IC ISL95857AHRTZ-T TQFN 40P PWM
PU614
S IC ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ501
AON7934_DFN3X3A-8-10
+VCC_SA
Local sense put on HW site
Compal confidential release to David_xie
Review
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
PWR_VCORE_ISL95857
LA-E092P
Rev 0.2
Monday, December 12, 2016
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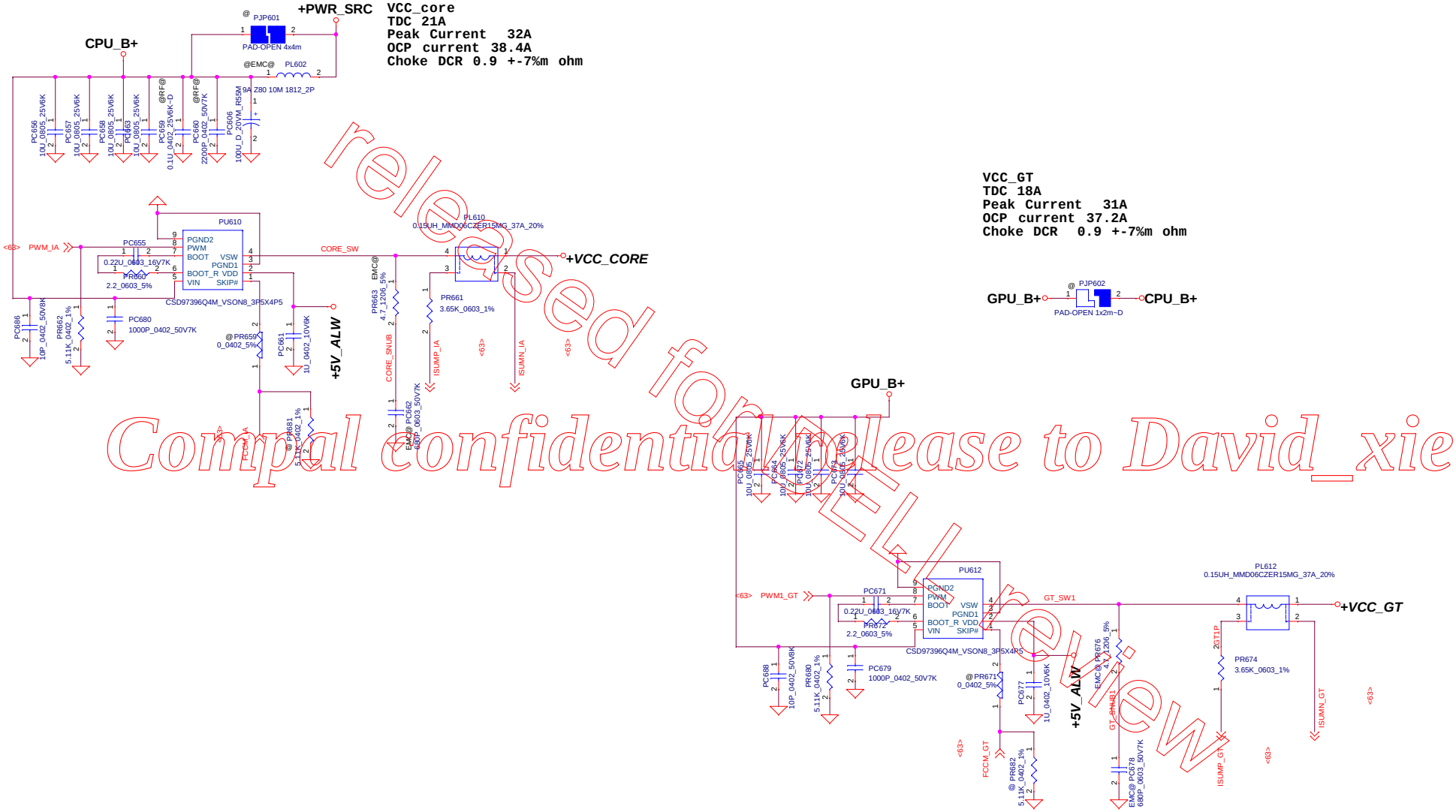

Compal Electronics, Inc.

Title: PWR_VCORE_ISL95857

Size | Document Number: LA-E092P | Rev: 0.2

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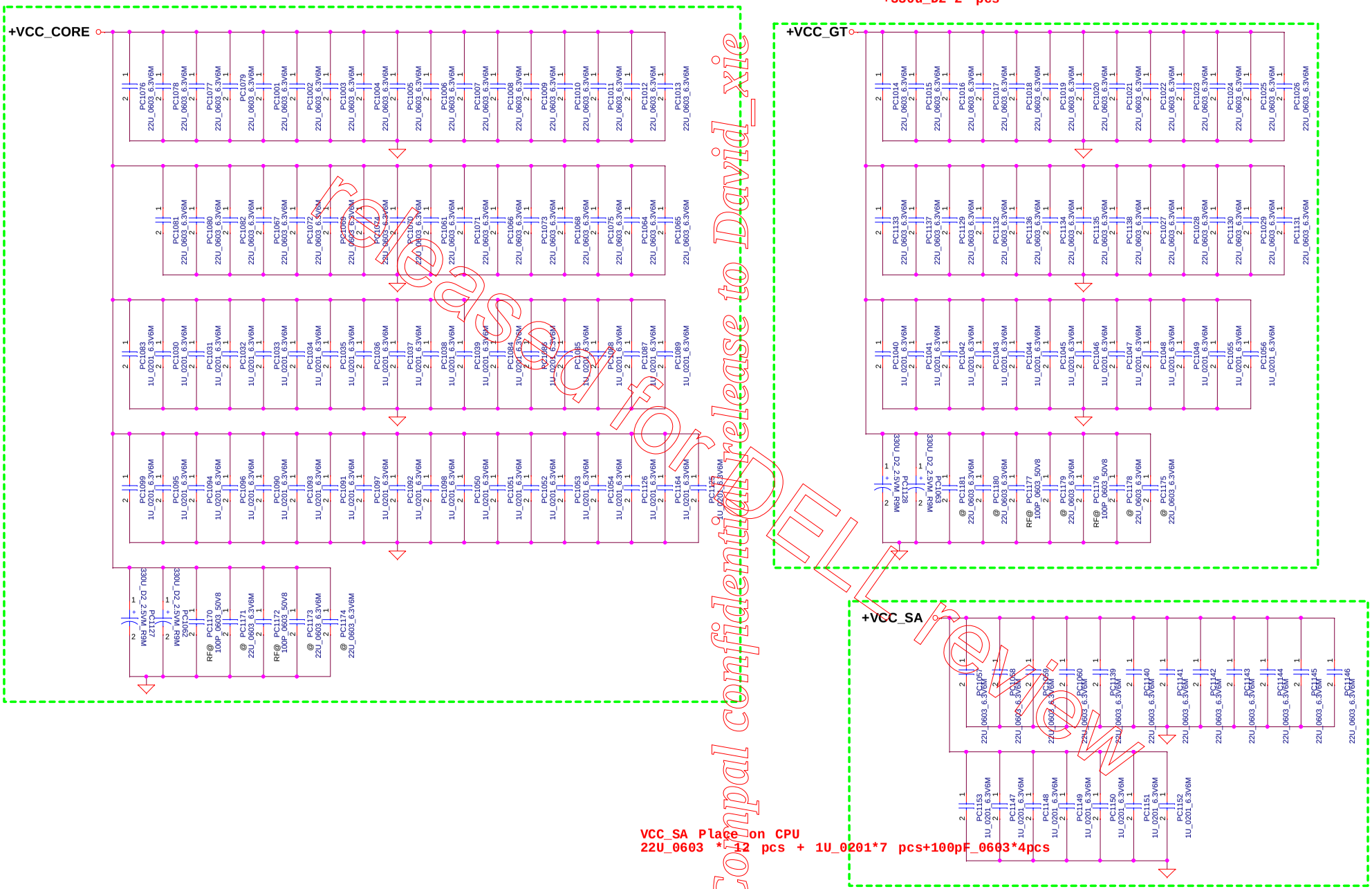
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs



VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs+100pF_0603*4pcs

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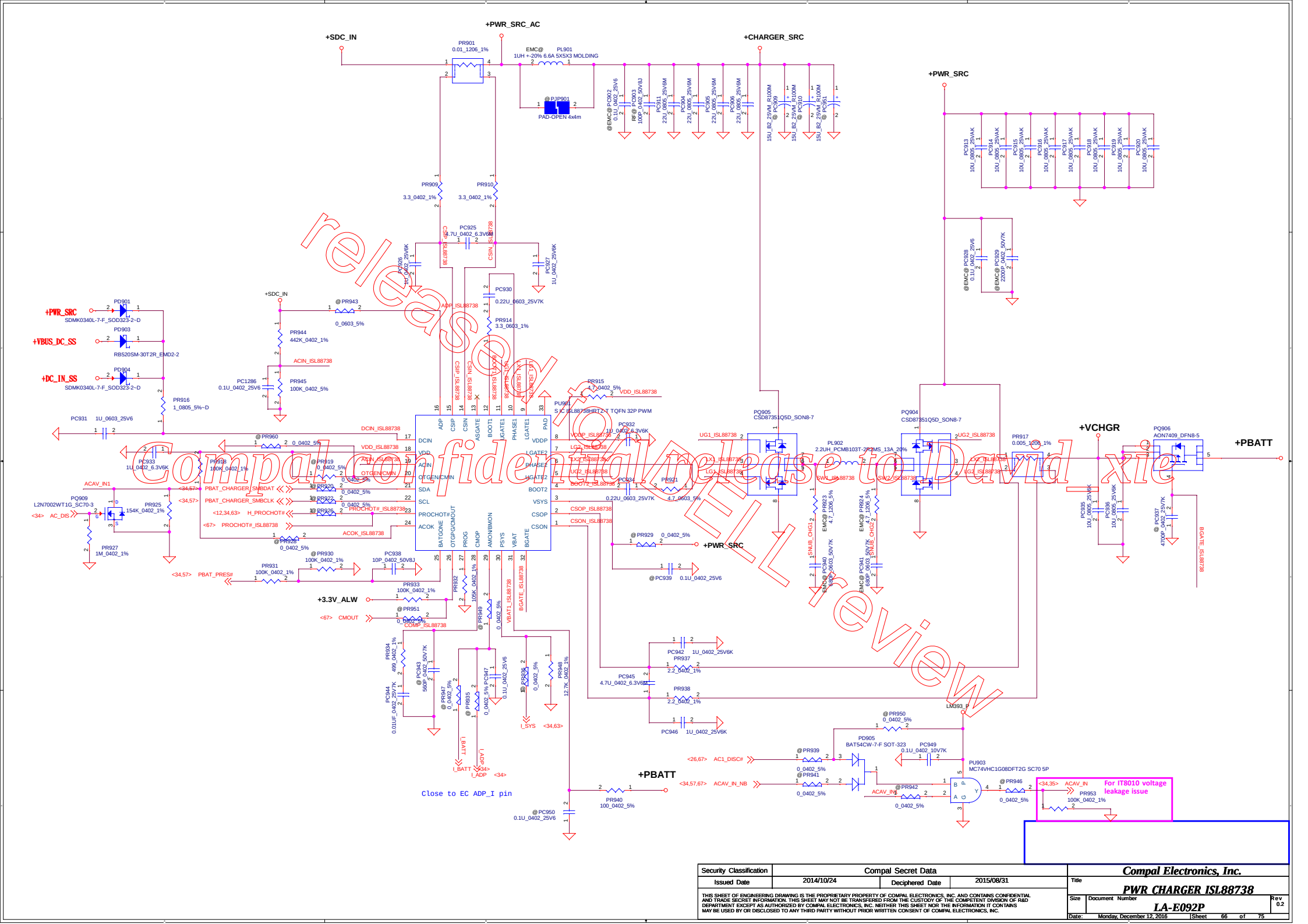
Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

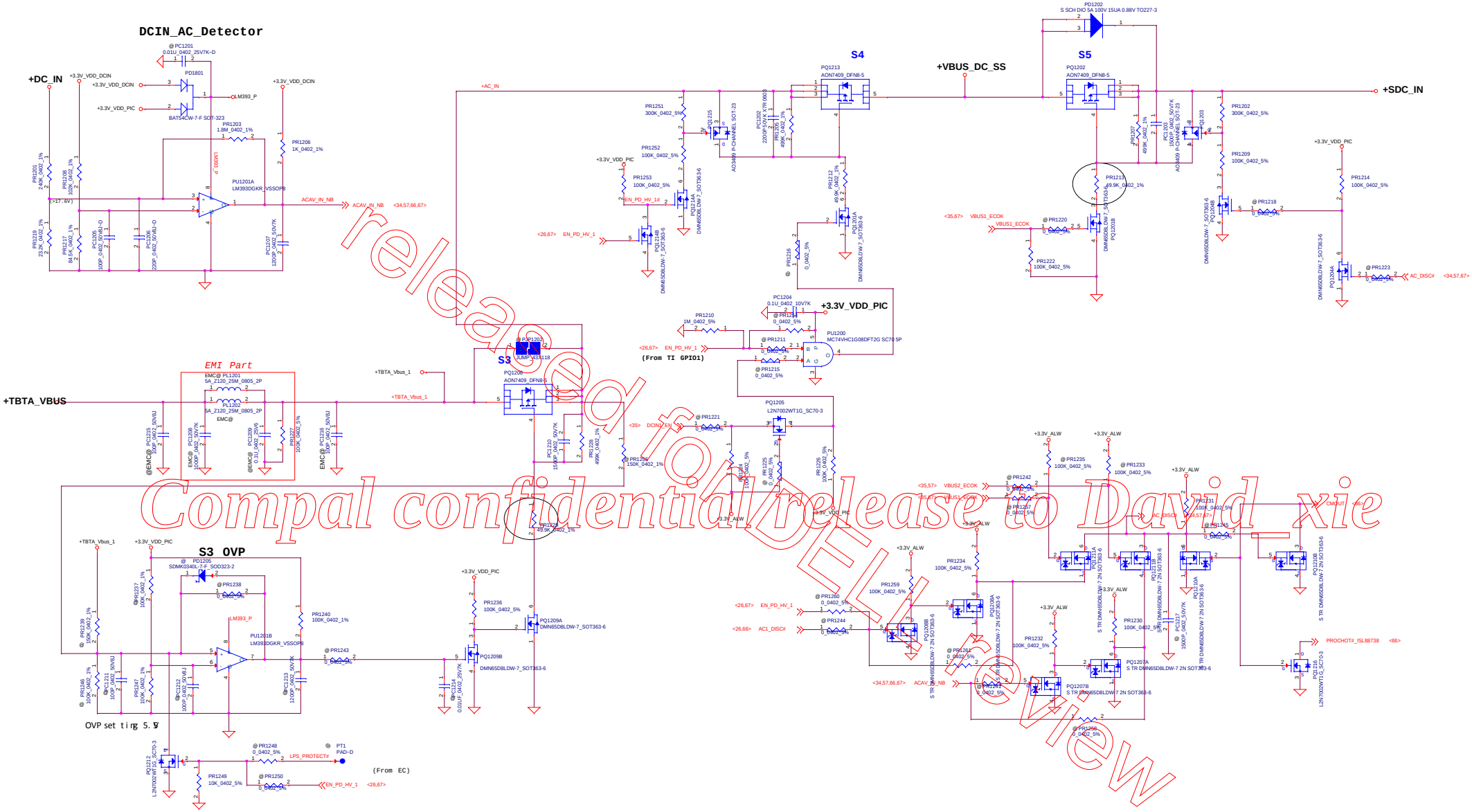
Size: | Document Number: LA-E092P | Rev: 0.2

Date: Monday, December 12, 2016 | Sheet 65 of 75



Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/08/31

Compal Electronics, Inc.	
Title	PWR CHARGER ISL88738
Size	Document Number: LA-E092P
Rev	0.2
Date:	Monday, December 12, 2016
Sheet	66 of 75



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Compal Electronics, Inc.		
Title: Breckenridge_TypeC_PD		
Size	Document Number: LA-E092P	Rev: 0.2
Date: Monday, December 12, 2016	Sheet 67 of 75	

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR9	39K	20K	39K
Rref1	PR5	39K	20K	30K
Rboot	PR8	1.5K	2K	3K
Rref2=PR10+PR12	PR10	30K	18K	24K
	PR12	1.5K	0	3K
C	PC8	1.5nf	2.7nf	1.8nf

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA
Rocset=9.53k ohm , Ivalley=17.84A Rds(on)=3.1m ohm
I_ripple1=(13.5-0.9)*0.9/(301.53Khz*0.22u*13.5)=12.67A
I_ripple2=(6-0.9)*0.9/(287Khz*0.22u*6)=12.10A
OCP=(Ivalley+1/2I_ripple)=(17.84+6.05)x2=47.4A
OCP=86W/1.35=64A (two phase)
OCP= 32A per phase
Ivalley=32A-12.67A/2=19.202A

H-side MOS:TPCA8065
Rds(on):
11.7mohm@Vgs=10V
9.4mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

Choke: 0.22uH (Size:6.8*7.6*4.0)
Rdc=1.1mohm +-20%
Heat Rating Current=28A
Saturation Current=28A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=12,798A*3mohm=38.39mV

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Power at Boost GPU	25W	32W	25W	20W	23W	N/A	30W	40W
Total at Tj=102C								
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

Operation phase Number	PSI Voltage setting
1 phase with DEM	0.8V to 1.8V
1 phase with CCM	1.8V to 2.4V
Active phase with CCM	2.4V to 5.5V

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PSI Pull high on HW side

Pull high on HW side

Reserve Location

1. VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC616 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=301.53Khz

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR620=VTSNS/Rth

	T_min	T_typical	T_max
PR620=18.7K	96.73C	100C	103.1C
PR620=13K	106.38C	110C	113.4C

+VGA_CORE
EDP-Continuous 21 A
EDP-Peak 39.5 A
OCP 47.4A

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Title: +GPU_CORE
Size: Document Number: LA-E092P
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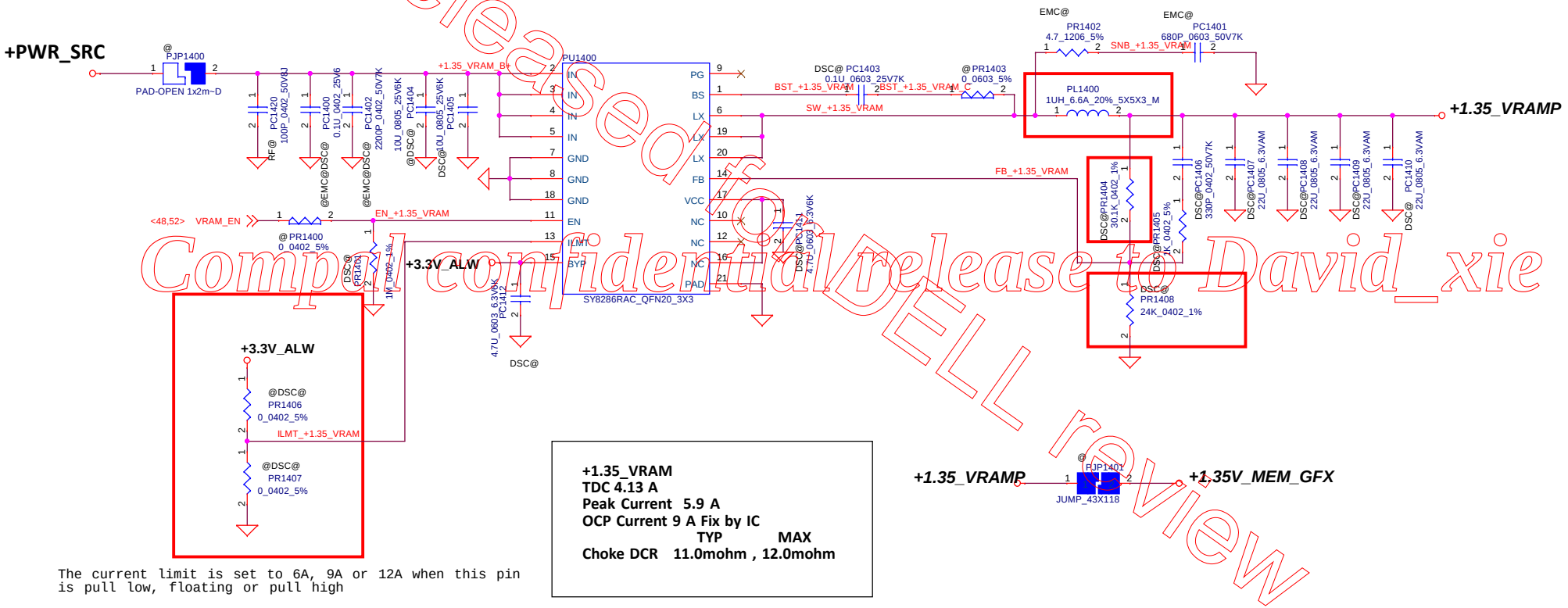

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

+1.35_VRAM
TDC 4.13 A
Peak Current 5.9 A
OCP Current 9 A Fix by IC

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

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Title	GPU_VRAM(SY8286RAC)	
Size	Document Number LA-E082P	Rev 0.1
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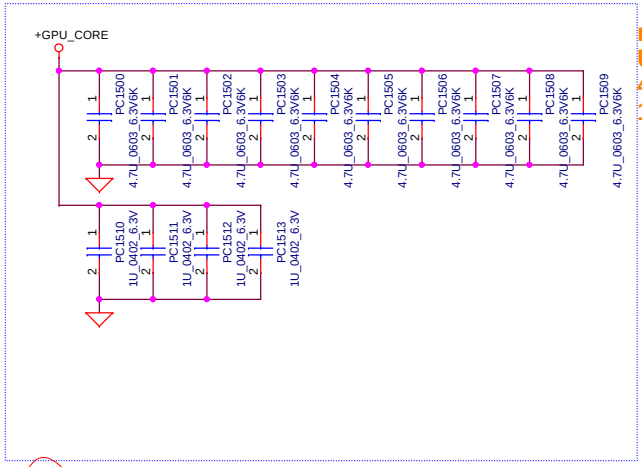
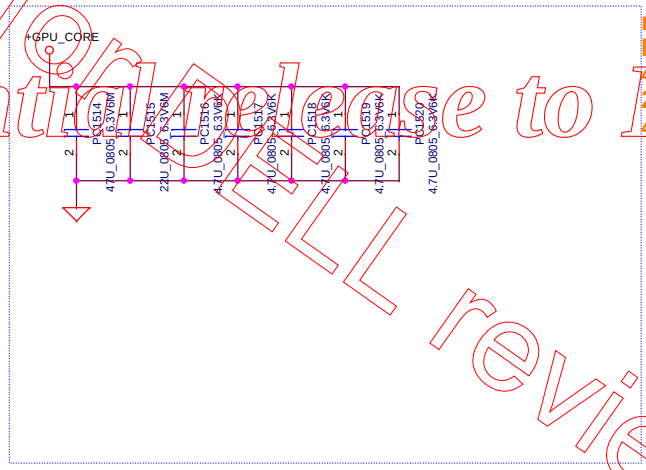


nVidia GB4-64 package
Under GPU
4.7uF 0603 * 10
1uF 0402 * 4



nVidia GB4-64 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5

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Title: PROCESSOR DECOUPLING

Size | Document Number: LA-E092P | Rev: 0.2

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	PU501 PG connect to +1.8V_RPIM_PWRGD & Pull high to 3.3V	modify power rail PU501, pull high to 3.3V and connect netname +1.8V_PRIM_PWRGD	X00
2	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	New add 1.2V_RUN (From 3.3V_RUN) by use power regulator SW ,only for HDMI PS8407 EE request	modify power rail PU502, change PR508 from 8.87K to 5.1K	X00
3	52	+1.2V_MEM/ +0.6V_DDR	2016 03/07	Compal	remove 1.2V_DDR_PG	remove 1.2V_DDR_PG,remove PR201	X00
4	60	1Type-C PD Selector	2016 03/14	Compal	ESD part repeat with PD1204 and DT4	remove PD1204	X00
5	60	1Type-C PD Selector	2016 03/17	Compal	to add S4 quick turn off 3/14 by chris	add PQ1214 and PD1801	X00
6	60	1Type-C PD Selector	2016 05/12	Compal	change solution version to fix PS4 funciton issue by MichaelCC Chen	modify PU602 ,change from P/N: SA00008602L (S IC ISL95857HRTZ-TS2778 TQFN 40P PWM)To P/N: SA0000A4A00 (S IC ISL95857AHRTZ-T TQFN 40P PWM)	X00
7	61	PWR_GPU_COREP (RT8813A)	2016 06/03	Compal	change GPU resistance PR1312 to fix OCP of RT8813A by MichaelCC Chen	Change PR1312 from 8.87K_0402_1%(SD034887180) to 9.53k _0402_1%(SD034953180) and change 9.53k[SD034976180] _0402_1% to 9.76k_0402_1%[SD034976180] on 6/20	X01
8	59	PWR_CHARGER (ISL88738)	2016 06/29	Compal	Change charger version by MichaelCC Chen	Charger: Change the charger version to B version from A version.	X01
9	60	1Type-C PD Selector	2016 06/29	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT# by MichaelCC Chen	Add PQ1216 DMN65D8LW-7_SOT323-3(SB00000UO00) Reserve PC1217 1500P_0402_50V7K(SE074152K80)	X01
10	56	P56-PWR_VCCSA	2016 06/29	Compal	change VCC_CORE capacitance PR640 ,PC642 and PC646 to tune the VCORE by MichaelCC Chen	Change PR640 change from 383_0402_1%(SD034383080) to 365_0402_1%(SD034365080) PC642 change from 0.033uF[SE076333K80] to 6800pF[SE075682K80] PC646 change from[SE00000MJ00] 0.047uF to 0.068uF [SE00000WX00] PC647 from 680pF[SE074681K80]to 1000pF[SE074102K80] PC621 from 680pF[SE074681K80] to 1000pF[SE074102K80]	X01
11	57	P53-PWR_1VALWP (SY8286RAC)	2016 06/29	Compal	Change the SY8286 for cost down plan by MichaelCC Chen	+1V_ALW: Change the power solution to SY8286R from SYX196D VRAM: Change the power solution to SY8286R from SYX196D	X01
12	59	1Type-C PD Selector	2016 06/29	Compal	Change the S4 fast turn off circuit to avoid the leakage. by MichaelCC Chen	TypeC: Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN.	X01
13	59,60	PWR_CHARGER (ISL88738) 1Type-C PD Selector	2016 06/29	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT# by MichaelCC Chen	Charger: Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND. Add 1 net PROCHOT#_ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01
14		1Type-C PD Selector	2016 06/29	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V by MichaelCC Chen	TypeC: PR1219 change from 22.6K to 23.2K. SD034232280	X01

Version Change List (P. I. R. List)

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15	57	P57-PWR_+VCC _CORE	2016 06/29	Compal	Location Alignment by MichaelCC Chen	VCORE: U-Line VCCSA change the PU606 to PU614 and PL601 to PL614 IA change the PU603 to PU610 and PL603 to PL610 GT change the PU604 to PU612 and PL604 to PL612	X01
16	59	P59-PWR_Charger	2016 06/29	Compal	To decrease the charger input leakage voltage for TypeC AC. by MichaelCC Chen	Change the PD903 from SCS0340L010 to SCS00006C00.	X01
17	52	1Type-C PD Selector	2016 06/29	Compal	Reserve the OVP function to protect the typeC device. by MichaelCC Chen	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205, PC1213, PC1214 a Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm Re-modify the S11 OVP description to S3 OVP.	X01
18	50,60	P50-PWR_DC_IN & P60-TypeC PD selector	2016 06/29	Compal	To solve the MOS leakage problem to avoid the error active. by MichaelCC Chen	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X01
19	51,52, 53,56, 56,59	PWR_DC_IN 3V/5V CPU Charger TypeC PD selector	2016 06/29	Compal	RF require and tune on snubber R,C by MichaelCC Chen	POP PC903,PC103,PC1302,PC1303,PC116 [SE071101J80] PC1320,PC1312,PC1401,PC125,PC622,PC662,PC678,PC940,PC941,PC204,PC112,PC302 [SE025681K80] PR1319,PR1311,PR1402,PR112,PR627,PR663,PR676,PR923,PR924,PR202,PR106,PR303 [SD000010280]	X01
20	57	PWR_+VCCSA _ISL95857	2016 06/29	Compal	Tune value for (IMON SA), (OCP of IA),(GT DVID) by MichaelCC Chen	Change the PR651 from 130kOhm to 124kOhm. (IMON SA) Change the PR640 from 383 Ohm to 365 Ohm. (OCP of IA) Change the PC621 from 680pF to 1000pF. (GT DVID)	X01
21	59	P59-PWR_Charger	2016 06/29	Compal	For EMI require.	Change PR914 from 4.7_0603_5%(SD013470B80) to 3.3_0603_1%(SD014330B80)	X01
22	61	PWR_GPU_COREP (RT8813A)	2016 06/22	Compal	DGPU_PWROK PU resistor	Add PR1321 10K_0402_1%(SD034100280)	
23	58	P58-PWR-CPU BACK SIDE MLCC	2016 06/29	Compal	For EMI require.	POP PC1170,PC1172 PC1176,PC1177 100pF [SE024101J80]	
24							
25							

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	HW	2016/05/24	COMPAL	For Schematic align	Remove RA2	0.2(X01)
2	35	HW	2016/05/24	COMPAL	Symbol pin name change	UE1.C1 pin name change to GPIO024/nRESETI	0.2(X01)
3	9	HW	2016/05/24	COMPAL	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
4	25	HW	2016/05/24	COMPAL	Symbol pin name change	UT9.20 pin name change to SNK_CAD/DCI_DAT, UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
5	6	HW	2016/05/24	COMPAL	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
6	25	HW	2016/05/24	COMPAL	Disable AUX snoop feature	Pop RT308	0.2(X01)
7	33,40	HW	2016/05/24	COMPAL	Remove HDD LED MUX feature	Depop RN100/RN101	0.2(X01)
8	35	HW	2016/05/24	COMPAL	PORT80_DET#	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
9	6	HW	2016/05/24	COMPAL	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
10	17	HW	2016/05/24	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
11	46	HW	2016/05/24	COMPAL	For DFX request	H1/H2/H3/H4/H7/H8/H34/H35/H16/H17/H11/H23 footprint remove "-G"	0.2(X01)
12	25	HW	2016/06/01	COMPAL	Follow ME drawing	Delete H21	0.2(X01)
13	40	HW	2016/06/01	COMPAL	Base on LED FFC cable routing	SWAP JLED1 pin define	0.2(X01)
14	30	HW	2016/06/01	INTEL	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
15	37,38	HW	2016/06/07	DELL	change to Nuvoton TPM form ATMEL TPM	Delete ATMEL TPM circuit, Add Nuvoton TPM circuit	0.2(X01)
16	12	HW	2016/06/07	INTEL	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
17	33	HW	2016/06/07	INTEL	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
18	33	HW	2016/06/07	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
19	35	HW	2016/06/07	COMPAL	For MEC5105K-D1-TN sample	1.UE1 change to SA00009GL00(S IC MEC5105K-D1-TN WFBGA 169P EC) 2.Depop RE361,Pop RE360,RE362	0.2(X01)
20	23	HW	2016/06/17	COMPAL	Base on HDMI EA result, change pre-emphasis to 1.6dB	Pop RV47	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	46	HW	2016/06/17	COMPAL	Base on ME drawing	Remove H18	0.2(X01)
22	42	HW	2016/06/17	COMPAL	Base on USB3 EA result,B_EQ change to 9.5dB	Depop RI42	0.2(X01)
23	11	HW	2016/06/17	COMPAL	Base on Crystal EA result	CC23 change form 15pF to 12pF	0.2(X01)
24	41	HW	2016/06/17	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	Depop RN5	0.2(X01)
25	38,45	HW	2016/06/20	COMPAL	ME request	1.JKBTP1 change from HRS_TF49-20S-0P5SH_20P-T to CVILU_CF5020FD0RK-05-NH_20P-T 2.JUSH1 change from HRS_TF49-26S-0P5SH_26P-T to CVILU_CF5026FD0RK-05-NH_26P-T	0.2(X01)
26	34	HW	2016/06/20	COMPAL	Base on Audio EA result	RA7,RA8 change from 24.9 to 16.2 ohm(SD00001U900)	0.2(X01)
27	30	HW	2016/06/22	COMPAL	EMI request	CL22 change from 1500pF to 10pF (SE167100J80 S CER CAP 10P 3KV J NPO 1808 AC250V X2Y3)	0.2(X01)
28	29	HW	2016/06/22	COMPAL	EMI request	Change LV1 from SM01000BV00 to SM01000NY00	0.2(X01)
29	46	HW	2016/06/22	COMPAL	Intel request	H5,H6 change from H_1P1N to H_1P0N	0.2(X01)
30	46	HW	2016/06/22	COMPAL	ME request	JIR1 change from SP010023D00 to SP010013W20	0.2(X01)
31	35	HW	2016/06/22	DELL	The posibility of GPIO map update,RTCRST_ON change from GPIO141 to GPIO122	Add RE514(@),RE515 for RTCRST_ON	0.2(X01)
32	36	HW	2016/06/22	COMPAL	For pre-config TPM	POP RZ363, De-POP RZ112,RZ113,RZ111,QZ9	0.2(X01)
33	12	HW	2016/06/22	COMPAL	BIOS need detect Storage type and dynamic change the name	UE1.D7 add HDD_DET#	0.2(X01)
34	29,30,43	HW	2016/06/22	COMPAL	RF request	1.CL30,CL29,CI31 change to 100pF(0402) SE071101J80 2.CA7,CZ2 change to 100pF(0201)SE174101J80 3.CV11,CV16 change to 100pF(0603)SE024101J80	0.2(X01)
33	24	HW	2016/06/28	COMPAL	For VGA test result	Pop RV121/RV122/CV132/CV133	0.2(X01)
34	38	HW	2016/06/29	COMPAL	X8 have no difference JUSH1 pin define concern	Depop DZ7,Pop RZ87	0.2(X01)
35	38	HW	2016/06/29	COMPAL	Let USH_PWR_STATE# keep low at S5	RZ10 change from 1M to 100k ohm	0.2(X01)
36	36	HW	2016/06/29	COMPAL	Foe X01 Board ID	RE79 change from 240k to 130k ohm	0.2(X01)
37	41	HW	2016/06/29	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
38	29	HW	2016/08/04	COMPAL	RF request	POP CC27 & change value from 22p to 47p	0.3(X02)
39	18	HW	2016/08/04	COMPAL	DSC BOM change	Pop RC385, Depop RC386	0.3(X02)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40	34, 35	HW	2016/08/04	COMPAL	Vendor schematic review	1. Add net WRST# to UE2.4 and CE500 1uf (SE000000K80) 2. Add RE523 0 ohm for UE2 power pin soft start 3. Change RE14,RE15,RE18 from 100k ohm to 10k ohm 4. Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT 5. Change RPE12.2 to RE525 (10Kohm) for EXPANDER_GPU_SMCLK 6. Reserve CE504~CE505 for EXPANDER_GPU_SMDAT/CLK to GND.	0.3(X02)
41	14	HW	2016/08/04	COMPAL	Intel suggestion	RC137 change from 1K to 3K	0.3(X02)
42	27	HW	2016/08/04	COMPAL	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
43	45	HW	2016/08/04	COMPAL	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
44	26	HW	2016/08/04	COMPAL	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
45	42	HW	2016/08/05	COMPAL	BITS290368-System can't be waked from S3 when connect to right USB port via USB3.0 to LAN Dongle.	USB3 repeater power rail Add RI79 0ohm to +3.3V_RUN and De-pop it. Add RI80 0ohm to +3.3V_ALW_PCH and pop it.	0.3(X02)
46	42	HW	2016/08/08	COMPAL	schematic modify	1. pop RI37 2. RI79, RI80 footprint change form 0402 to 0603 3. add QI1 controlling USB3 repeater PD#	0.3(X02)
47	32, 37	HW	2016/08/09	COMPAL	DFB request	SMT concern DZ1, DZ2, DZ5, DZ6 PCB pad is too small, suggest use the symbol "RB520SM-30T2R_EMD2-2" follow PD903	0.3(X02)
48	48	HW	2016/08/09	COMPAL	schematic modify	pop RV299 for NV GC6	0.3(X02)
49	35	HW	2016/08/10	COMPAL	Layout limit	SWAP RPE7	0.3(X02)
50	33, 35, 48	HW	2016/08/10	COMPAL	Footprint align	DA8,DE1,DV10 follow symbol "RB520SM-30T2R_EMD2-2"	0.3(X02)
51	46	HW	2016/08/11	COMPAL	ME request	H11/H23 change form 4.2mm to 5.2mm	0.3(X02)
52	42	HW	2016/08/11	COMPAL	schematic modify	change USB repeater PD# enable pin to "USB_PWR_SHR_VBUS_EN"	0.3(X02)
53	35	HW	2016/08/11	COMPAL	schematic align	add power rail +3.3V_ALW_UE2 for UE2	0.3(X02)
54	42	HW	2016/08/12	COMPAL	schematic modify	delete QI1, depop RI37, add RI81 connecting "USB_PWR_SHR_VBUS_EN" & "USB3_PD#'	0.3(X02)
55	29	HW	2016/08/15	COMPAL	RF request	pop CA6 & change value from 100p to 82p	0.3(X02)
56	42	HW	2016/08/24	COMPAL	EA request	depop RI38, RI53, RI57 for USB3 repeater	0.3(X02)
57	9	HW	2016/09/08	COMPAL	DGPU_PWR_EN need to use BIOS solution	depop RC385,pop RC386	0.4(X03)
58	38	HW	2016/09/08	COMPAL	TPM change to NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
59	35	HW	2016/09/08	COMPAL	Expander I/O change from ITE8010 to MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
60	34	HW	2016/09/08	COMPAL	Board ID	Change RE79 to 33kohm (SD028330280)	0.4(X03)
61	34	HW	2016/09/08	COMPAL	schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
62	34	HW	2016/09/08	COMPAL	EC request for power consumption	Add RE505 PU to +3.3V_ALW for LOM_CABLE_DETECT# (Reserve) Add RE532 PU to +3.3V_ALW for BCM5882_ALERT#	0.4(X03)
63	37	HW	2016/09/08	COMPAL	USH/B de-pop, pop on MB side	POP RZ8,RZ9 for USH SMBus	0.4(X03)
64	35	HW	2016/09/20	COMPAL	DELL request	Add RE536/RE537 for resistors for PCH_DPWROK circuit	0.4(X03)
65	34	HW	2016/09/20	COMPAL	WDT schematic option 2	use Option2: pop RE361 / depop RE362	0.4(X03)
66	33	HW	2016/09/20	COMPAL	EMI request	1. L6~L9 change to 80ohm bead (BLM15PD800SN1D, SM01000N000) for BR14/15 2. depop CA2, CA3 3. RA55,RA56 change location toLA15, LA16 with 33ohm bead (BLM15PX330SN1D,SM01000NA00)	0.4(X03)
67	39	HW	2016/09/20	COMPAL	NV GPU seqest	CV247 change from 3900pf t0 4700pf (SE075472K80) CV248 change form 220pf to 470pf (SE074471K80)	0.4(X03)
68	52	HW	2016/09/20	COMPAL	ME request	H17 change form 4P2 to 4P6	

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Title: EE P.I.R (2/6)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
69	35	HW	2016/10/04	COMPAL	BITS294007 - Sometimes need to press power button twice to power on system.	CE12 change to 2.2u (SE000008880) RE33 change to 1K (SD028100180)	0.4(X03)
70	24	HW	2016/10/04	COMPAL	U-line VGA EA PASS	depop RV121/RV122	0.4(X03)
71	26	HW	2016/10/04	COMPAL	TI CC pin for ESD request	CT85,CT86 change to 470p.(SE074471k80)	0.4(X03)
72	26	HW	2016/10/31	COMPAL	EC watchdog reserve	add QE13,RE530,CE503	1.0(A00)
73	26	HW	2016/10/31	COMPAL	UE1.H8 to prevent EOS issue on MEC5105	Add RE539(100ohm) to CV2_ON	1.0(A00)
74	36	HW	2016/10/31	COMPAL	BOARD ID	Change RE79 to 4.3k ohm(SD028430180)	1.0(A00)
75	36	HW	2016/10/31	COMPAL	Change R1 to R3 for MP part	Change UL1 CP/N to SA000081G1L Change UE1 CP/N to SA00009GL30 change UV1 CP/N to SA00009S01L	1.0(A00)
76	36	HW	2016/10/31	COMPAL	For DFB request.	Close solder mask CMOS1 (-NPM) and other co-lay part	1.0(A00)
77	36	HW	2016/10/31	COMPAL	Service Mode Switch remove	Depop SW1 and RC222 and RC221 change to short pad	1.0(A00)
78	36	HW	2016/10/31	COMPAL	RE374 change BS to LPC@	RE374 change BS to LPC@	1.0(A00)
79	36	HW	2016/10/31	COMPAL	For MEC5105 rev. C	Pop RE362,RE536; Depop RE361,QE13,CE503,RE530,UE7,CE5,CE6,RE348,RE537	1.0(A00)
80	36	HW	2016/12/12	COMPAL	For IE no display with FW 3.09	pop RT139, depop RT140	1.0(A00)