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MS-7613 Ver: 11 uATX(244mm X 244mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:SLI SL28748ELC-T
HD Audio Codec:ALC888S
LAN:RTL8111DL 10/100/1000
IO: Fintek F71858D
Flash ROM: 32 Mb SPI (CHIP) Fire wire: VIA VT6315N

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 3
Mini PCI Express (X1) Slot * 1
ONFI Slot *1

PWM:

Controller:Intersil ISL6333 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *6
USB2.0 *14 (Rear*6 / Front*8)
on BOARD BUZZER

D-SUB *1
DVI PORT*1

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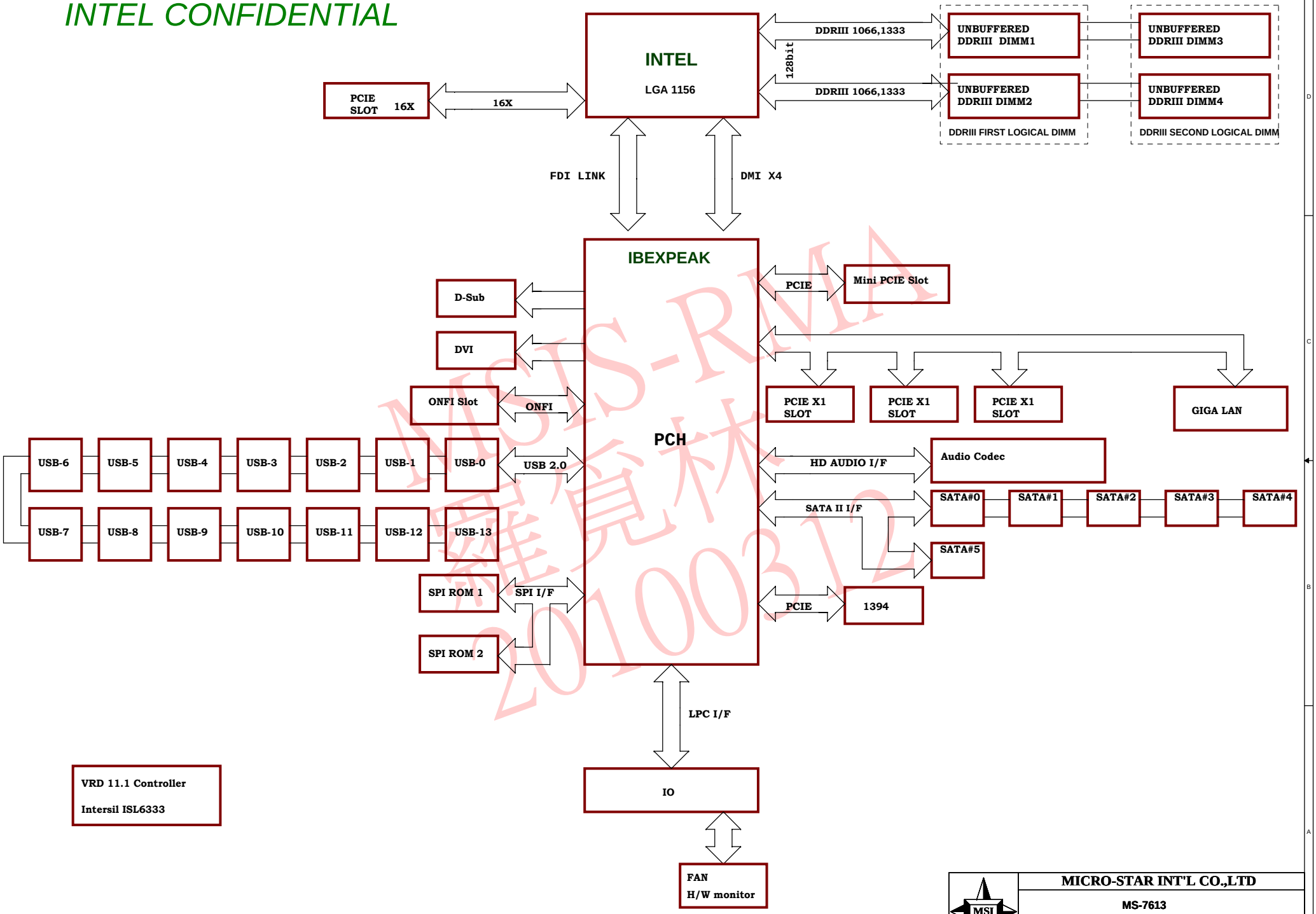

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

				LEBLKPBAK GPIO DEFINITION	
GPIO	POWER	I/O	Function	Implementation	Mother board Function
GPIO0	MAIN	I	SMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	I	TACH1	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	I	PCI_IRQE#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	I	PCI_IRQF#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	I	PCI_IRQG#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	I	PCI_IRQH#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	I	TACH2	**Pull-up to +3.3V and connect to PS2 pin 12. The COMM Bassembly connects pin 12 directly to GND**	COMM_B_DET#/ MXM_TH_ALRT#
GPIO7	MAIN	I	TACH3	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RSUSMB	O	ICC_EN#		Reserved
GPIO9	RSUSMB	I	OC5	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO10	RSUSMB	I	OC6	**10K Pull-up to +3_3V and connect to P126-pin 16**	PRNTR_DET#
GPIO11	RSUSMB	I	SMBALERT#	20K Pull-up to +3_3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RSUSMB	I	LAN_DISABLEB	Follow implementation in Intel Pickton Design Guide	LAN_DISABLE#
GPIO13	RSUSMB	I	IO_PME	10K Pull-up to +3_3V and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET# or DASH SMI
GPIO14	RSUSMB	I	OC7	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RSUSMB	I	PCIE_GP15		Reserved
GPIO16	RSUSMB	O	SATA4GP	10 M pull- up to VBAT and connect to CPU SKTOCC# , SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	I	TACH0	connect through a 0 Ω series resistor, and refer the PCA spec for Fans mapping. if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	I	PCICLKRQ1#	Through a 1KΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	I	SATA1GP	connect to a test point	unused
GPIO20	MAIN	I	PCICLKRQ2#	Through a 0 Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKRQ2#
GPIO21	MAIN	I	SATA0GP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	I	SCLOCK	10K Pull-up to +3_3V and connect to P150-pin 10	INT_USB_DET#
GPIO23	MAIN	I	LDRQ1#	connect to a test point.	PEG_MXM_DET#
GPIO24	RSUSMB	O	MEMLED	Through a 1k Ω series resistor, 8.2K pull-up to +3_3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RSUSMB	I	PCICLKRQ3#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ3#
GPIO26	RSUSMB	I	PCICLKRQ4#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ4#
GPIO27	RSUSMB	O	OD_PLL_VR_EN	10k pull-up to +3.3VAUX	Reserved
GPIO28	RSUSMB	O	PCIE_GP28	connect to a test point	unused
GPIO29	RSUSMB	O	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RSUSMB	I	SUS_PWR_ACK	100K Pull-up to 3.3V_AUX	unused
GPIO31	MAIN	I	ACPRESENT	10K Pull-up to +3_3V and connect to P25-pin 10	FRONT_USB_DET 1#
GPIO32	MAIN	O	PCIE_GP32	Through a 1k Ω series resistor, 10K pull-up to +3_3V and connect to P2-pin 6.	NON-EPA_PS_DET#
GPIO33	MAIN	O	PCIE_GP33	Through a 1k Ω series resistor, 8.2K pull-up to +3_3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	O	SP_PCI#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-pu to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	O	SATACLKREQ#	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	I	SATA2GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	I	SATA3GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	I	SLOAD	Through a series 1K resistor, 10K Pull-up to +3_3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	I	SDATAOUT0	Pull-up to +3_3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RSUSMB	I	OC1	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for XDP implementation. 8.2k Ω pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RSUSMB	I	OC2	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO42	RSUSMB	I	OC3	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO43	RSUSMB	I	OC4	connect through a 0 Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO44	RSUSMB	I	PCICLKRQ5#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKRQ5#
GPIO45	RSUSMB	I	PCICLKRQ6#	Through a 0 Ω series resistor. 10K pull-up to +3.3V and connect to J31-pinB17	PRSNT#_J31
GPIO46	RSUSMB	I	PCICLKRQ7#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ7#
GPIO47	RSUSMB	I	PEG_A_CLKRQ#	Through a 0 Ω series resistor. 10K pull-up to +3.3V and connect to J41-pinB48 and B81	PRSNT#_J41
GPIO48	MAIN	I	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3_3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	O	SATA5GP	10K Pull-up to +3_3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	I	PCI_REQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	O	PCI_GNT#1	connect to a test point	GNT1#
GPIO52	MAIN	I	PCI_REQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	O	PCI_GNT#2	connect to a test point	GNT2#
GPIO54	MAIN	I	PCI_REQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14 -pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	O	PCI_GNT#3	connect to a test point	GNT3#
GPIO56	RSUSMB	I	PEG_B_CLKRQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	I	PCIE_GP57	10K Pull-up to +3_3VME installed and 10K pull-down to GND not installed.	TPM_PP
GPIO58	RSUSMB	O	SML1CLK	10K pull-up to 3V_AUX	SML1CLK
GPIO59	RSUSMB	I	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer theXDP design guide for xdp implementation.	USB_OC#
GPIO60	RSUSMB	O	SMLDALERT#	10K pull-up to 3V_AUX	SMLDALARM
GPIO61	RSUSMB	O	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RSUSMB	O	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RSUSMB	O	SLP_S5#	Connect to the SIO-pin37	SLP_S5#
GPIO64	MAIN	O	CLKOUTFLEX0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX0
GPIO65	MAIN	O	CLKOUTFLEX1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX1
GPIO66	MAIN	O	CLKOUTFLEX2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLEX2
GPIO67	MAIN	O	CLKOUTFLEX3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RSUSMB	I	PCIE_GP72	Pull-up to +3_3V and connect to P24-pin 10	FRONT_USB_DET 0#
GPIO73	RSUSMB	I	PCIECLKRQ0#	10K pull-up to +3.3VAUx and through a 0 Ω series resistor. connect to J42-pinB17. B31, B48, and B81	PRSNT#_J42
GPIO74	RSUSMB	O	SML1ALERT#	10K pull-up to 3V_AUX	SML1ALERT#
GPIO75	RSUSMB	O	SML1DATA	10K pull-up to 3V_AUX	SML1DATA

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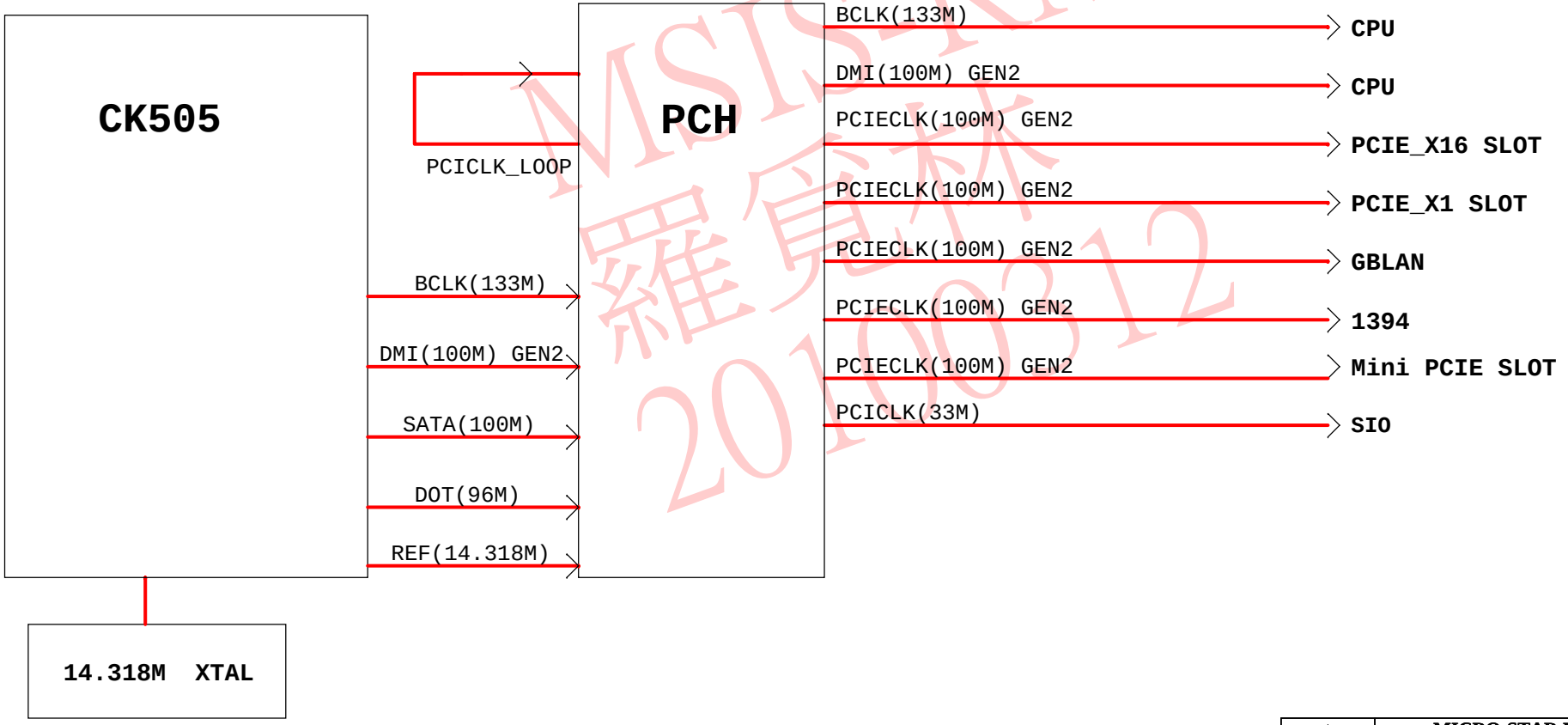

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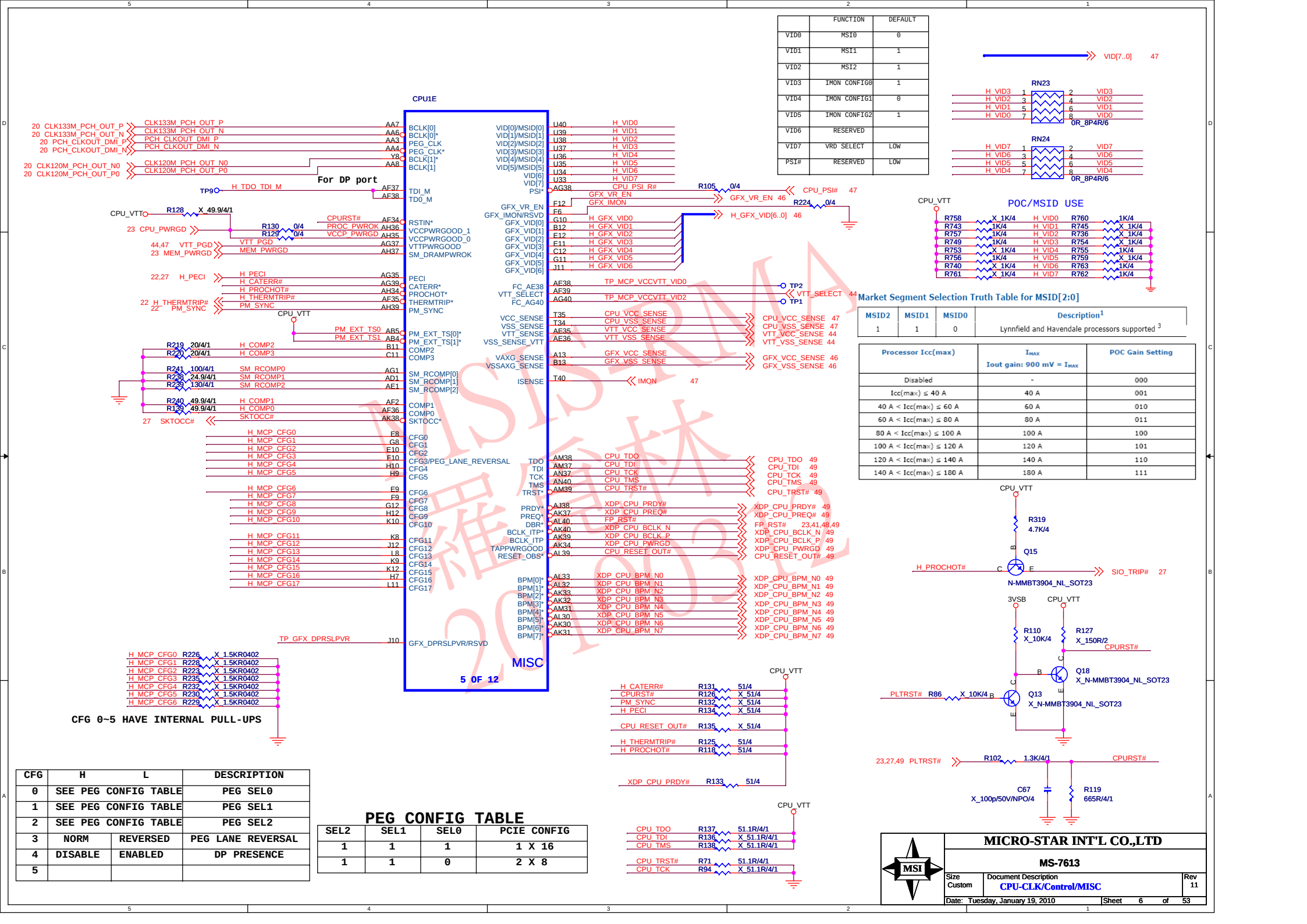

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG2	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

MSID2	MSID1	MSID0	Description[1]
1	1	0	Lynnfield and Havendale processors supported [3]

Processor Icc(max)	I_{MAX} Iout gain: 900 mV = I_{MAX}	POC Gain Setting
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111

CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	SEE PEG CONFIG TABLE		PEG SEL1
2	SEE PEG CONFIG TABLE		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLED	DP PRESENCE
5			

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

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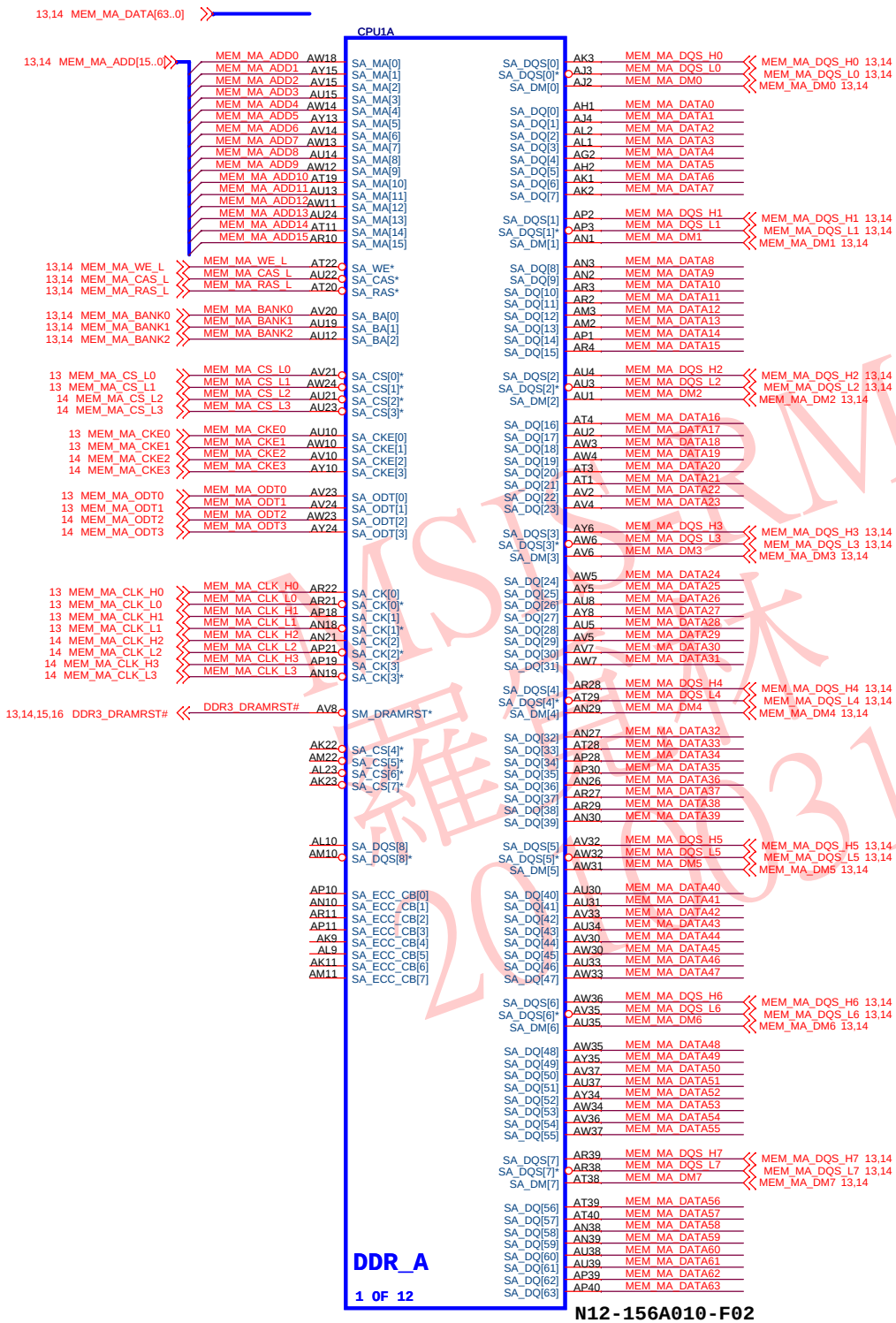

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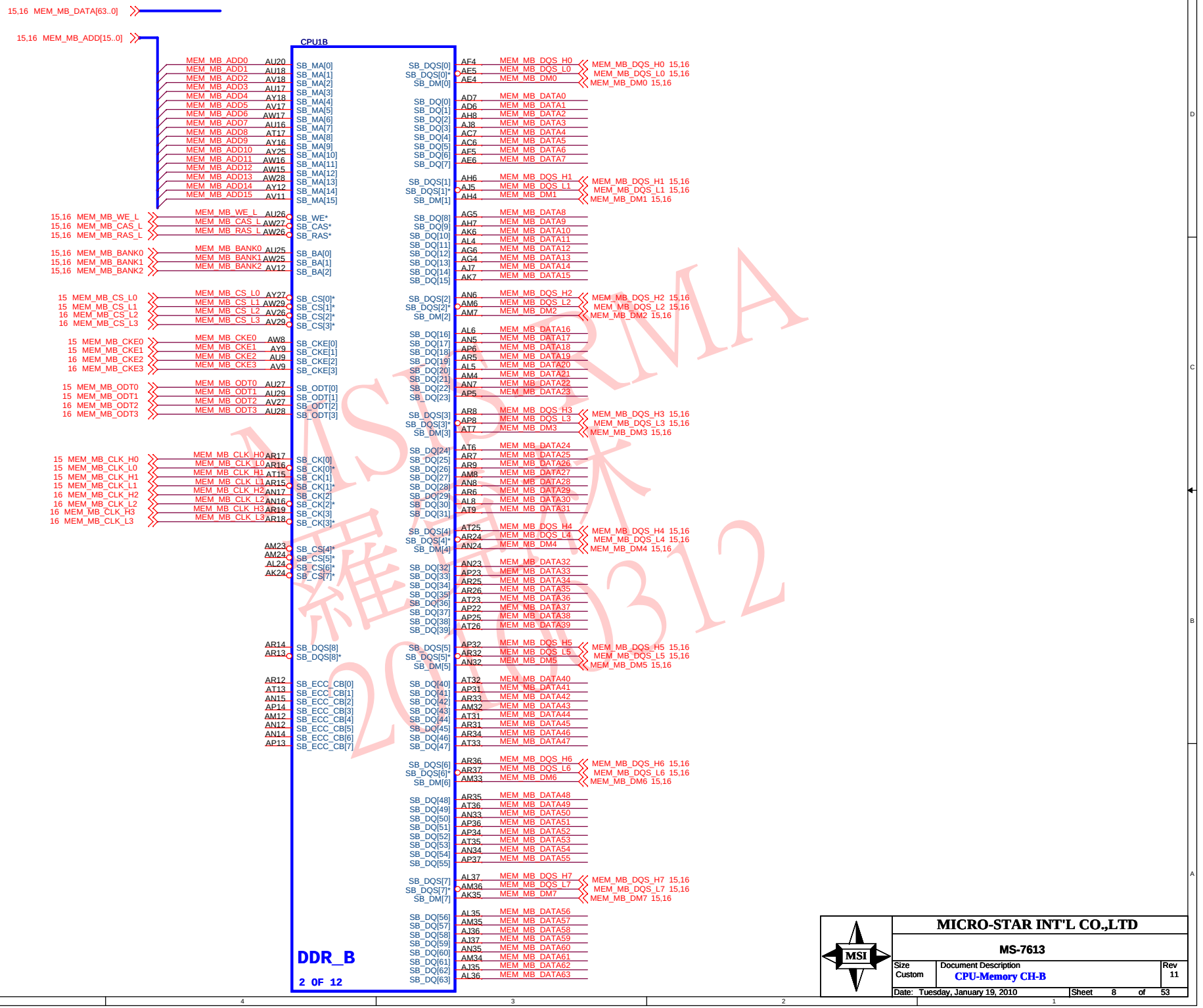
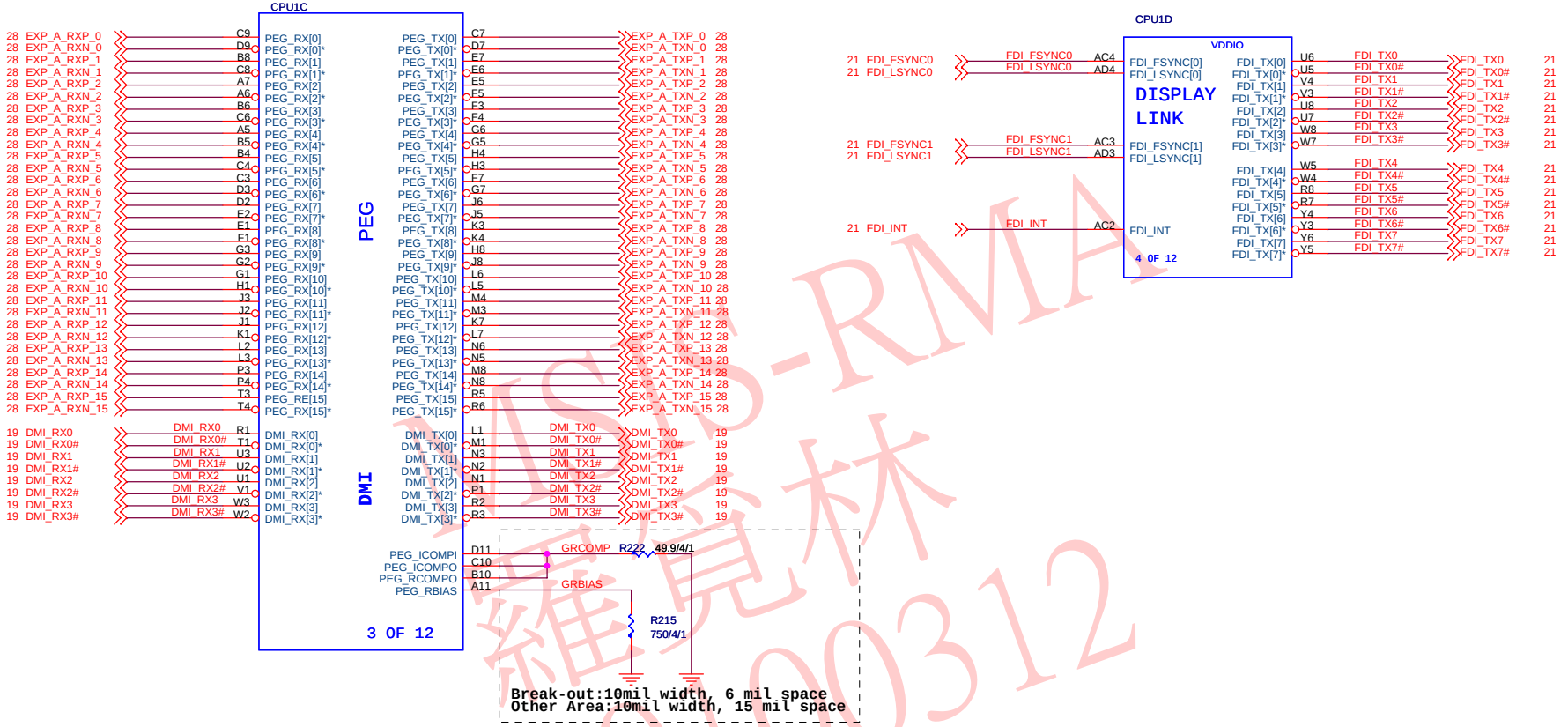
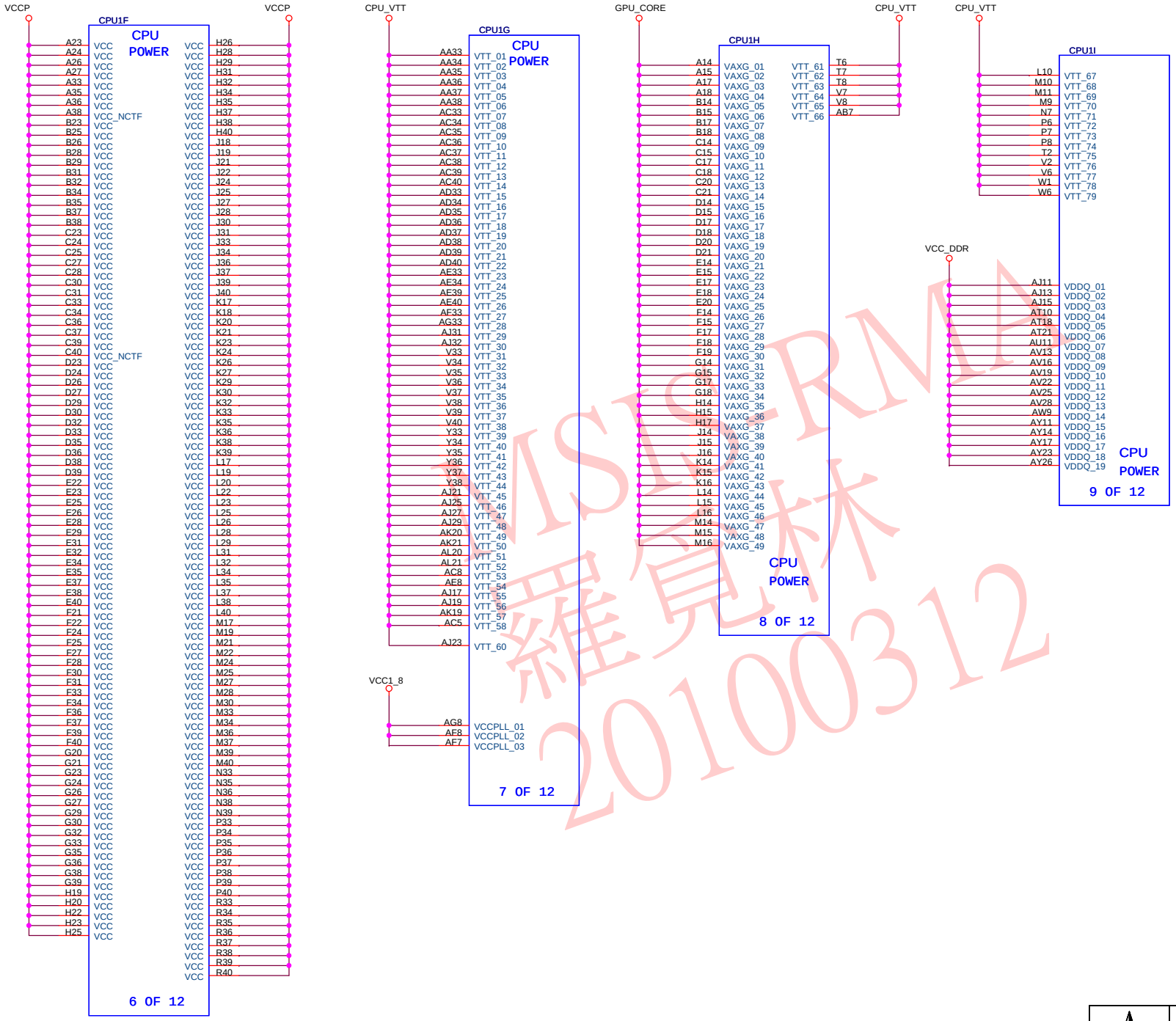

15,16 MEM_MB_DATA[63..0]
15,16 MEM_MB_ADD[15..0]
CPU1B
MEM_MB_ADD0 AU20 SB_MA[0]
MEM_MB_ADD1 AU18 SB_MA[1]
MEM_MB_ADD2 AV18 SB_MA[2]
MEM_MB_ADD3 AU17 SB_MA[3]
MEM_MB_ADD4 AY18 SB_MA[4]
MEM_MB_ADD5 AV17 SB_MA[5]
MEM_MB_ADD6 AW17 SB_MA[6]
MEM_MB_ADD7 AU16 SB_MA[7]
MEM_MB_ADD8 AT17 SB_MA[8]
MEM_MB_ADD9 AY16 SB_MA[9]
MEM_MB_ADD10 AY25 SB_MA[10]
MEM_MB_ADD11 AW16 SB_MA[11]
MEM_MB_ADD12 AW15 SB_MA[12]
MEM_MB_ADD13 AW28 SB_MA[13]
MEM_MB_ADD14 AY12 SB_MA[14]
MEM_MB_ADD15 AV11 SB_MA[15]
15,16 MEM_MB_WE_L MEM_MB_WE_L AU26 SB_WE*
15,16 MEM_MB_CAS_L MEM_MB_CAS_L AW27 SB_CAS*
15,16 MEM_MB_RAS_L MEM_MB_RAS_L AW26 SB_RAS*
15,16 MEM_MB_BANK0 MEM_MB_BANK0 AU25 SB_BA[0]
15,16 MEM_MB_BANK1 MEM_MB_BANK1 AW25 SB_BA[1]
15,16 MEM_MB_BANK2 MEM_MB_BANK2 AV12 SB_BA[2]
15 MEM_MB_CS_L0 MEM_MB_CS_L0 AY27 SB_CS[0]*
15 MEM_MB_CS_L1 MEM_MB_CS_L1 AW29 SB_CS[1]*
16 MEM_MB_CS_L2 MEM_MB_CS_L2 AV26 SB_CS[2]*
16 MEM_MB_CS_L3 MEM_MB_CS_L3 AV29 SB_CS[3]*
15 MEM_MB_CKE0 MEM_MB_CKE0 AW8 SB_CKE[0]
15 MEM_MB_CKE1 MEM_MB_CKE1 AY9 SB_CKE[1]
16 MEM_MB_CKE2 MEM_MB_CKE2 AU9 SB_CKE[2]
16 MEM_MB_CKE3 MEM_MB_CKE3 AV9 SB_CKE[3]
15 MEM_MB_ODT0 MEM_MB_ODT0 AU27 SB_ODT[0]
15 MEM_MB_ODT1 MEM_MB_ODT1 AU29 SB_ODT[1]
16 MEM_MB_ODT2 MEM_MB_ODT2 AV27 SB_ODT[2]
16 MEM_MB_ODT3 MEM_MB_ODT3 AU28 SB_ODT[3]
15 MEM_MB_CLK_H0 MEM_MB_CLK_H0 AR17 SB_CK[0]
15 MEM_MB_CLK_L0 MEM_MB_CLK_L0 AR16 SB_CK[0]*
15 MEM_MB_CLK_H1 MEM_MB_CLK_H1 AT15 SB_CK[1]
15 MEM_MB_CLK_L1 MEM_MB_CLK_L1 AR15 SB_CK[1]*
16 MEM_MB_CLK_H2 MEM_MB_CLK_H2 AN17 SB_CK[2]
16 MEM_MB_CLK_L2 MEM_MB_CLK_L2 AN16 SB_CK[2]*
16 MEM_MB_CLK_H3 MEM_MB_CLK_H3 AR19 SB_CK[3]
16 MEM_MB_CLK_L3 MEM_MB_CLK_L3 AR18 SB_CK[3]*
AM23 SB_CS[4]*
AM24 SB_CS[5]*
AL24 SB_CS[6]*
AK24 SB_CS[7]*
AR14 SB_DQS[8]
AR13 SB_DQS[8]*
AR12 SB_ECC_CB[0]
AT13 SB_ECC_CB[1]
AN15 SB_ECC_CB[2]
AP14 SB_ECC_CB[3]
AM12 SB_ECC_CB[4]
AN12 SB_ECC_CB[5]
AN14 SB_ECC_CB[6]
AP13 SB_ECC_CB[7]
SB_DQS[0] AF4 MEM_MB_DQS_H0 MEM_MB_DQS_H0 15,16
SB_DQS[0]* AE5 MEM_MB_DQS_L0 MEM_MB_DQS_L0 15,16
SB_DM[0] AE4 MEM_MB_DM0 MEM_MB_DM0 15,16
SB_DQ[0] AD7 MEM_MB_DATA0
SB_DQ[1] AD6 MEM_MB_DATA1
SB_DQ[2] AH8 MEM_MB_DATA2
SB_DQ[3] AJ8 MEM_MB_DATA3
SB_DQ[4] AC7 MEM_MB_DATA4
SB_DQ[5] AC6 MEM_MB_DATA5
SB_DQ[6] AE5 MEM_MB_DATA6
SB_DQ[7] AE6 MEM_MB_DATA7
SB_DQS[1] AH6 MEM_MB_DQS_H1 MEM_MB_DQS_H1 15,16
SB_DQS[1]* AJ5 MEM_MB_DQS_L1 MEM_MB_DQS_L1 15,16
SB_DM[1] AH4 MEM_MB_DM1 MEM_MB_DM1 15,16
SB_DQ[8] AG5 MEM_MB_DATA8
SB_DQ[9] AH7 MEM_MB_DATA9
SB_DQ[10] AK6 MEM_MB_DATA10
SB_DQ[11] AL4 MEM_MB_DATA11
SB_DQ[12] AG6 MEM_MB_DATA12
SB_DQ[13] AG4 MEM_MB_DATA13
SB_DQ[14] AJ7 MEM_MB_DATA14
SB_DQ[15] AK7 MEM_MB_DATA15
SB_DQS[2] AN6 MEM_MB_DQS_H2 MEM_MB_DQS_H2 15,16
SB_DQS[2]* AM6 MEM_MB_DQS_L2 MEM_MB_DQS_L2 15,16
SB_DM[2] AM7 MEM_MB_DM2 MEM_MB_DM2 15,16
SB_DQ[16] AL6 MEM_MB_DATA16
SB_DQ[17] AN5 MEM_MB_DATA17
SB_DQ[18] AP6 MEM_MB_DATA18
SB_DQ[19] AR5 MEM_MB_DATA19
SB_DQ[20] AL5 MEM_MB_DATA20
SB_DQ[21] AM4 MEM_MB_DATA21
SB_DQ[22] AN7 MEM_MB_DATA22
SB_DQ[23] AP5 MEM_MB_DATA23
SB_DQS[3] AR8 MEM_MB_DQS_H3 MEM_MB_DQS_H3 15,16
SB_DQS[3]* AP8 MEM_MB_DQS_L3 MEM_MB_DQS_L3 15,16
SB_DM[3] AT7 MEM_MB_DM3 MEM_MB_DM3 15,16
SB_DQ[24] AT6 MEM_MB_DATA24
SB_DQ[25] AR7 MEM_MB_DATA25
SB_DQ[26] AR9 MEM_MB_DATA26
SB_DQ[27] AM8 MEM_MB_DATA27
SB_DQ[28] AN8 MEM_MB_DATA28
SB_DQ[29] AR6 MEM_MB_DATA29
SB_DQ[30] AL8 MEM_MB_DATA30
SB_DQ[31] AT9 MEM_MB_DATA31
SB_DQS[4] AT25 MEM_MB_DQS_H4 MEM_MB_DQS_H4 15,16
SB_DQS[4]* AR24 MEM_MB_DQS_L4 MEM_MB_DQS_L4 15,16
SB_DM[4] AN24 MEM_MB_DM4 MEM_MB_DM4 15,16
SB_DQ[32] AN23 MEM_MB_DATA32
SB_DQ[33] AP23 MEM_MB_DATA33
SB_DQ[34] AR25 MEM_MB_DATA34
SB_DQ[35] AR26 MEM_MB_DATA35
SB_DQ[36] AT23 MEM_MB_DATA36
SB_DQ[37] AP22 MEM_MB_DATA37
SB_DQ[38] AP25 MEM_MB_DATA38
SB_DQ[39] AT26 MEM_MB_DATA39
SB_DQS[5] AP32 MEM_MB_DQS_H5 MEM_MB_DQS_H5 15,16
SB_DQS[5]* AR32 MEM_MB_DQS_L5 MEM_MB_DQS_L5 15,16
SB_DM[5] AN32 MEM_MB_DM5 MEM_MB_DM5 15,16
SB_DQ[40] AT32 MEM_MB_DATA40
SB_DQ[41] AP31 MEM_MB_DATA41
SB_DQ[42] AR33 MEM_MB_DATA42
SB_DQ[43] AM32 MEM_MB_DATA43
SB_DQ[44] AT31 MEM_MB_DATA44
SB_DQ[45] AR31 MEM_MB_DATA45
SB_DQ[46] AR34 MEM_MB_DATA46
SB_DQ[47] AT33 MEM_MB_DATA47
SB_DQS[6] AR36 MEM_MB_DQS_H6 MEM_MB_DQS_H6 15,16
SB_DQS[6]* AR37 MEM_MB_DQS_L6 MEM_MB_DQS_L6 15,16
SB_DM[6] AM33 MEM_MB_DM6 MEM_MB_DM6 15,16
SB_DQ[48] AR35 MEM_MB_DATA48
SB_DQ[49] AT36 MEM_MB_DATA49
SB_DQ[50] AN33 MEM_MB_DATA50
SB_DQ[51] AP36 MEM_MB_DATA51
SB_DQ[52] AP34 MEM_MB_DATA52
SB_DQ[53] AT35 MEM_MB_DATA53
SB_DQ[54] AN34 MEM_MB_DATA54
SB_DQ[55] AP37 MEM_MB_DATA55
SB_DQS[7] AL37 MEM_MB_DQS_H7 MEM_MB_DQS_H7 15,16
SB_DQS[7]* AM36 MEM_MB_DQS_L7 MEM_MB_DQS_L7 15,16
SB_DM[7] AK35 MEM_MB_DM7 MEM_MB_DM7 15,16
SB_DQ[56] AL35 MEM_MB_DATA56
SB_DQ[57] AM35 MEM_MB_DATA57
SB_DQ[58] AJ36 MEM_MB_DATA58
SB_DQ[59] AJ37 MEM_MB_DATA59
SB_DQ[60] AN35 MEM_MB_DATA60
SB_DQ[61] AM34 MEM_MB_DATA61
SB_DQ[62] AJ35 MEM_MB_DATA62
SB_DQ[63] AL36 MEM_MB_DATA63
DDR_B
2 OF 12
MICRO-STAR INT'L CO.,LTD
MS-7613
Size Custom
Document Description CPU-Memory CH-B
Rev 11
Date: Tuesday, January 19, 2010
Sheet 8 of 53



MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size: Custom	Document Description: CPU-PEG/DMI		Rev: 11
Date: Tuesday, January 19, 2010		Sheet 9 of 53	

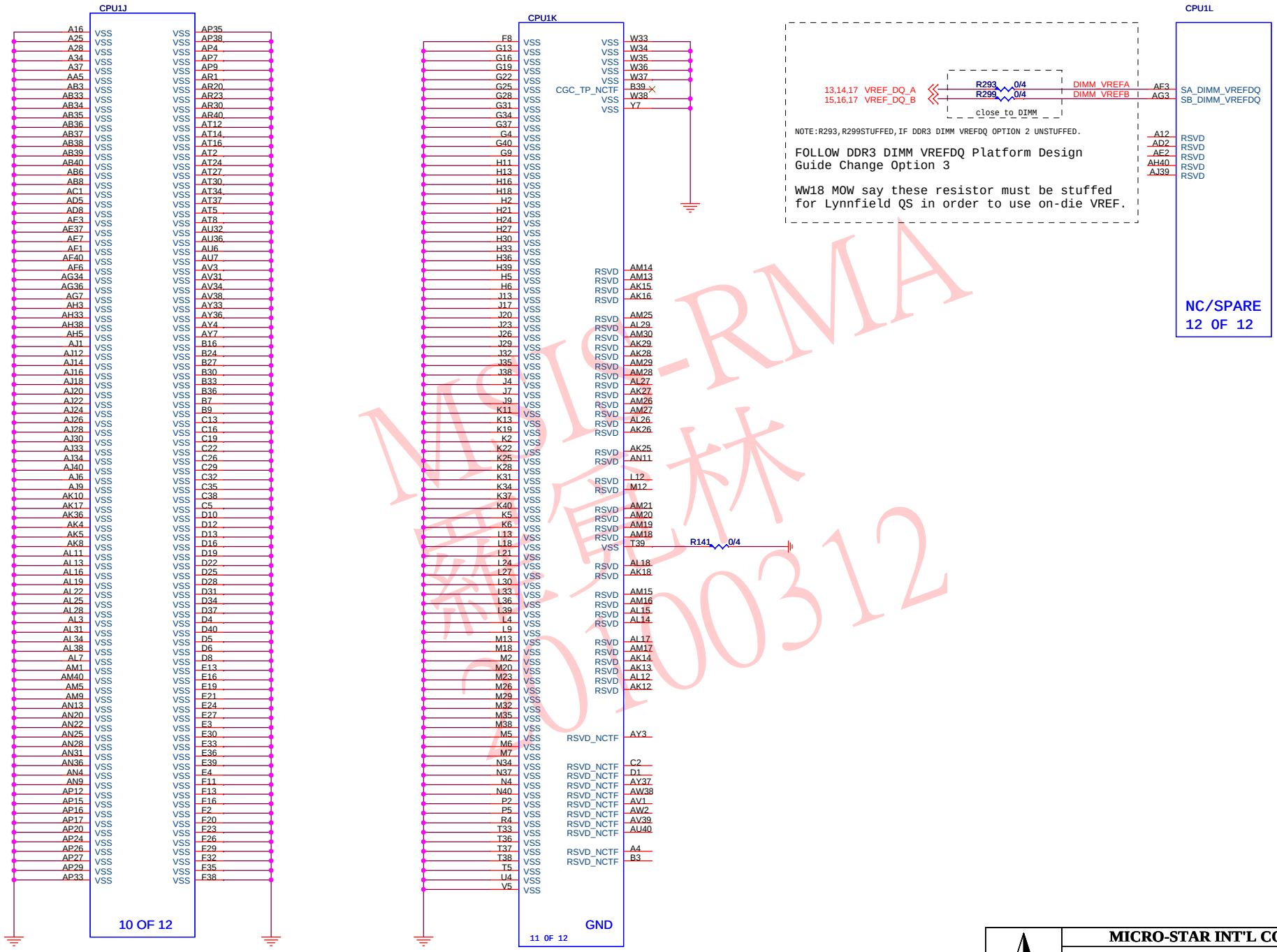


MICRO-STAR INT'L CO.,LTD

MS-7613

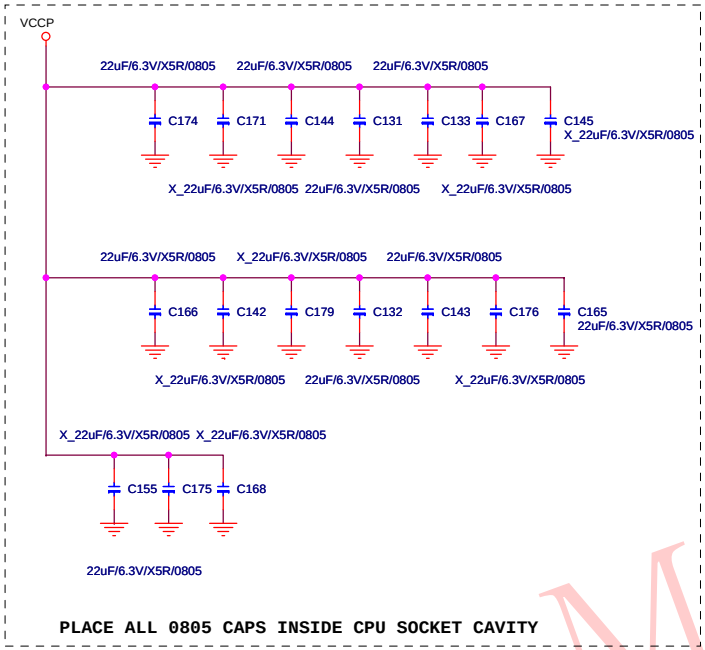
Size	Document Description	Rev
Custom	CPU-Power	11

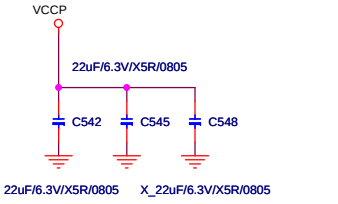
Date: Tuesday, January 19, 2010 | Sheet 10 of 53

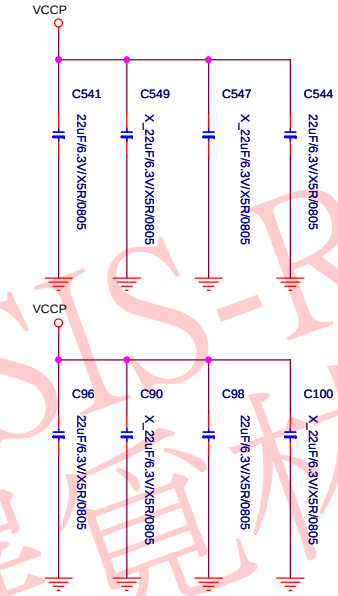


MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size: Custom	Document Description: CPU-GND		Rev: 11
Date: Tuesday, January 19, 2010		Sheet 11 of 53	

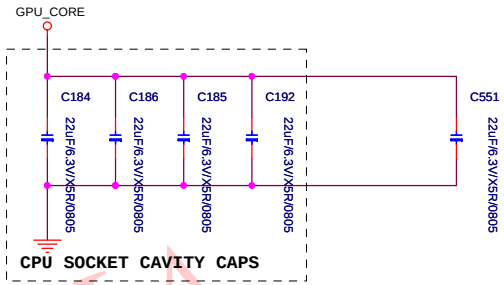
+CPU_VCCP-Decoupling



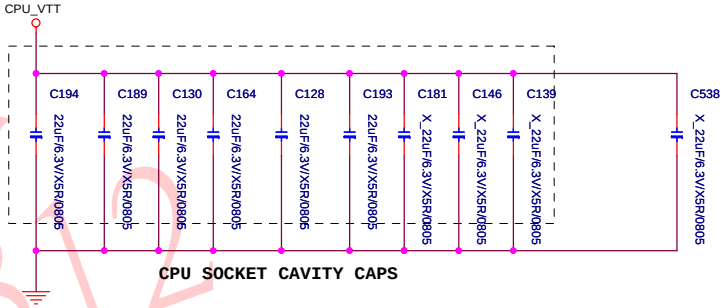


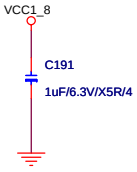


+CPU_GFX Decoupling

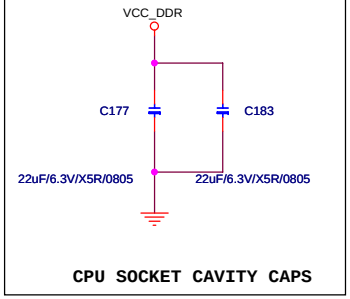


+CPU_VTT Decoupling





+1.5V_DDR3-Decoupling



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: CPU-Decoupling	Rev: 11
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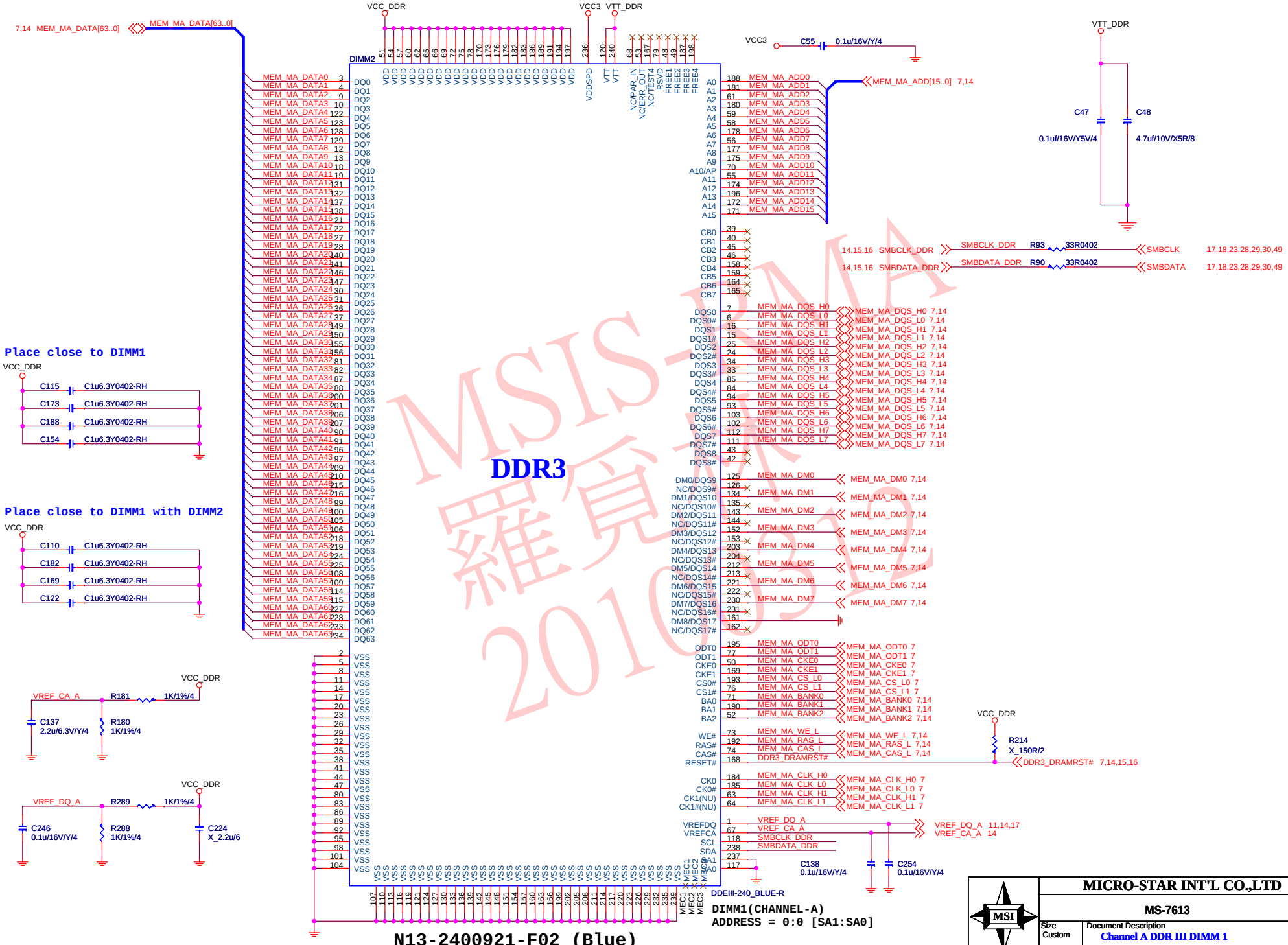
DDRIII DIMM_A1



MICRO-STAR INT'L CO.,LTD	
MS-7613	
Size: Custom	Document Description: Channel A DDR III DIMM 1
Rev: 11	
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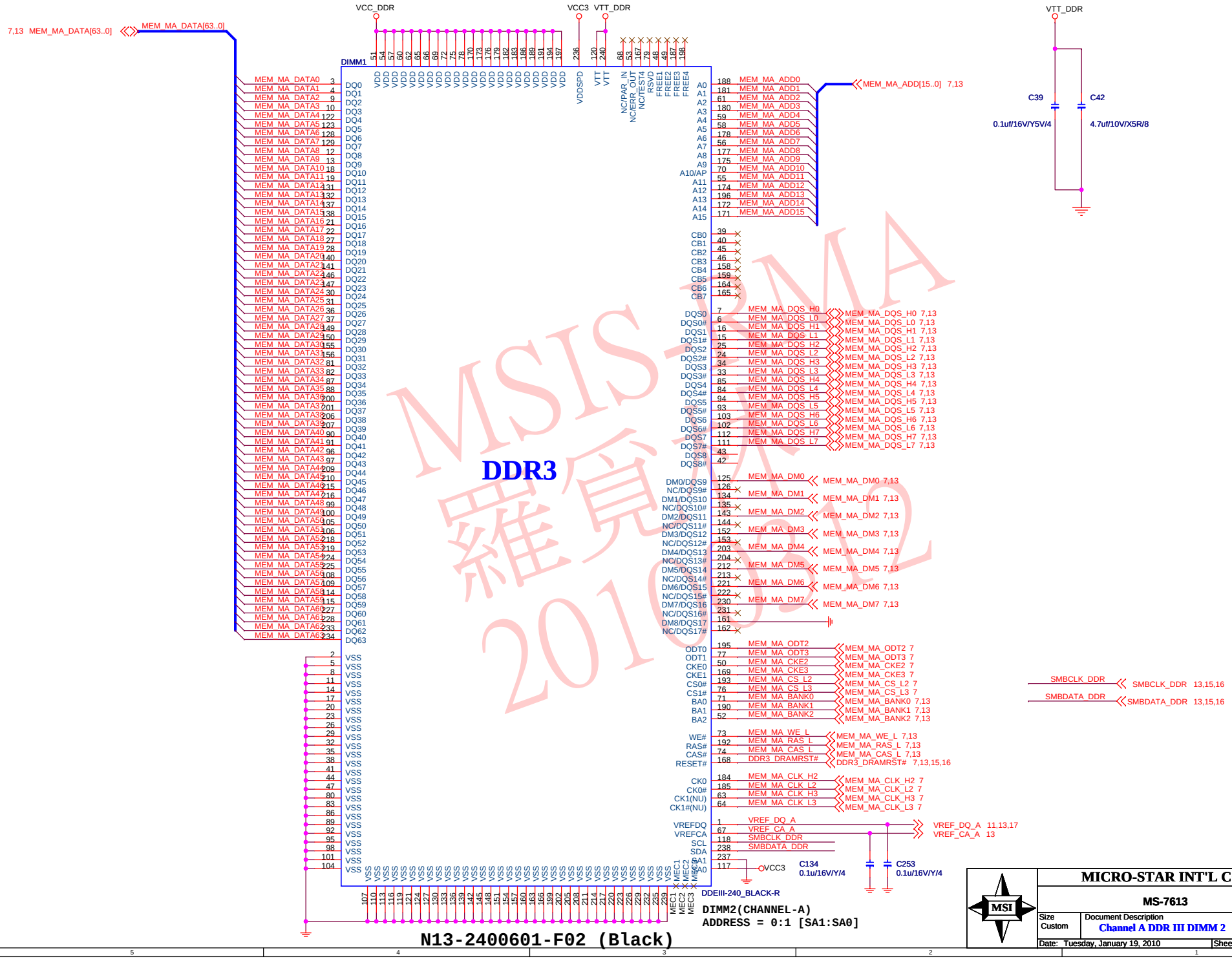
DDRIII DIMM_A2



MICRO-STAR INT'L CO.,LTD	
MS-7613	
Size: Custom	Document Description: Channel A DDR III DIMM 2
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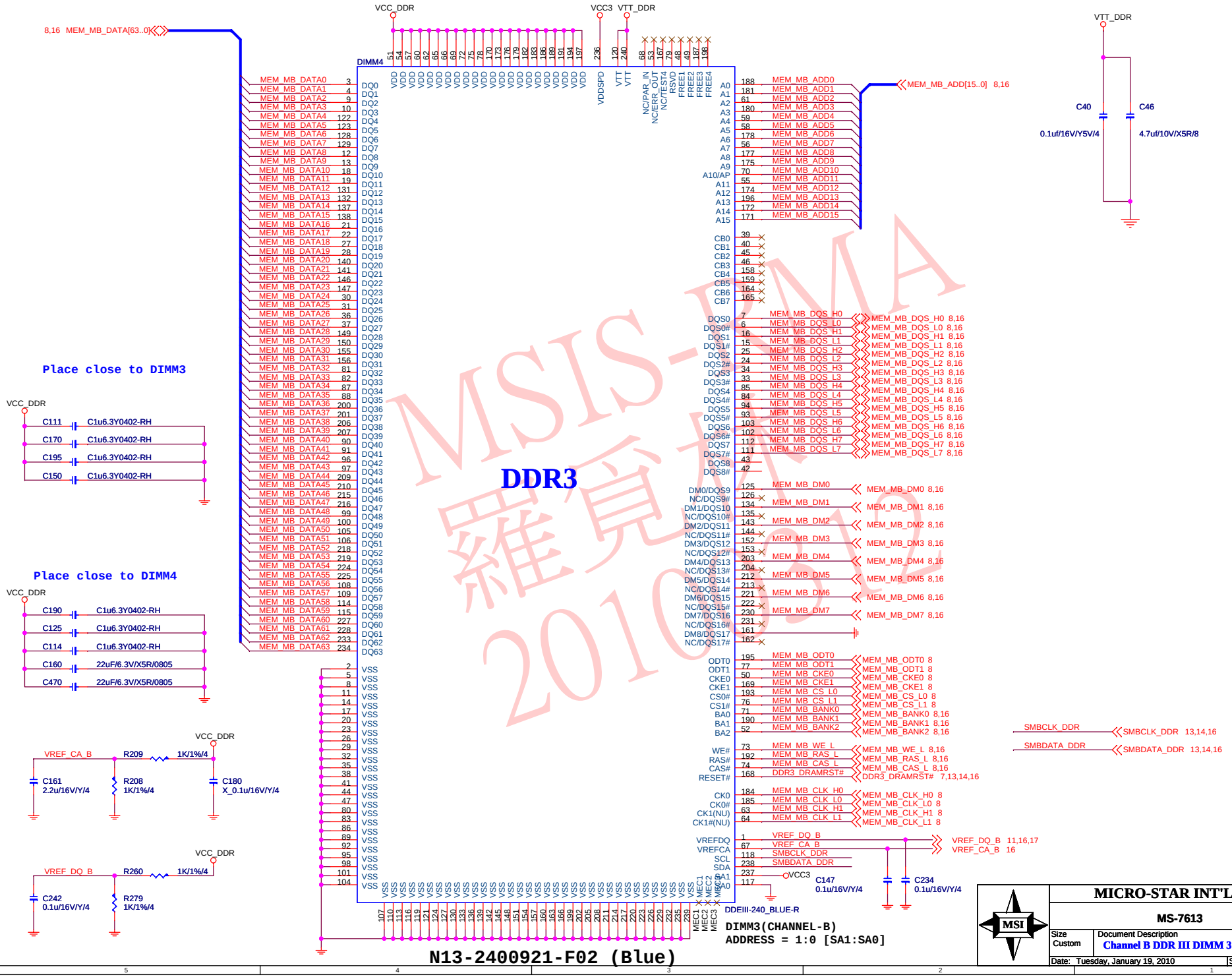
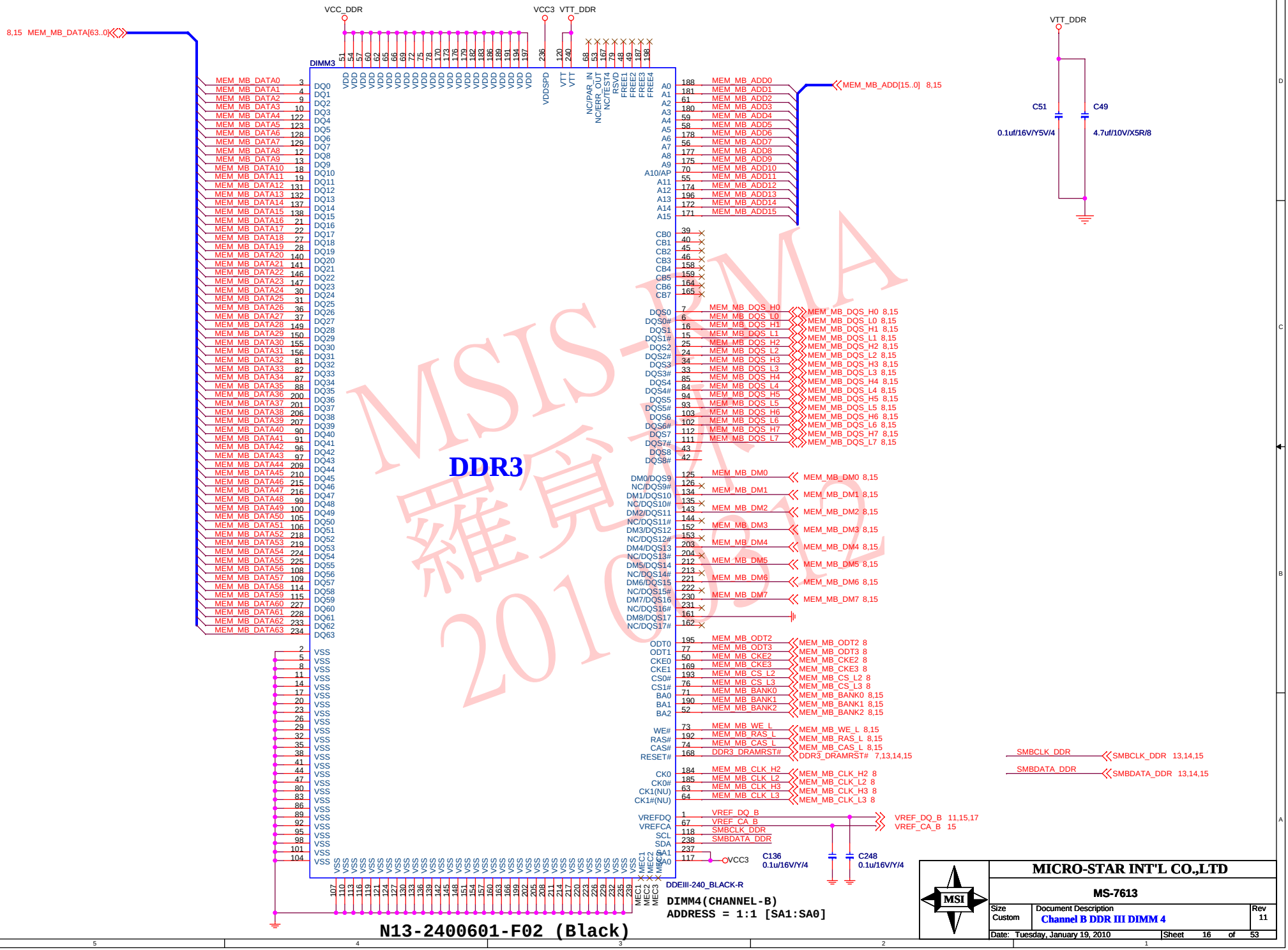
DDRIII DIMM_B1

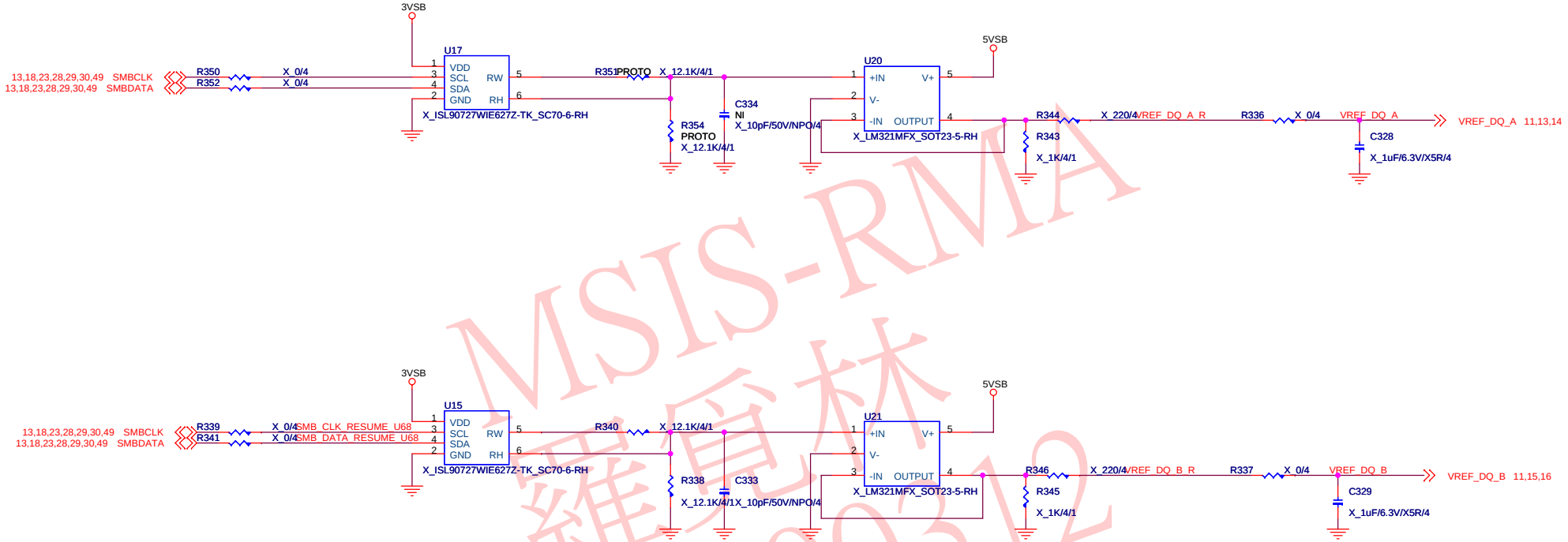


MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: Channel B DDR III DIMM 3	Rev: 11
Date: Tuesday, January 19, 2010	Sheet 15 of 53	

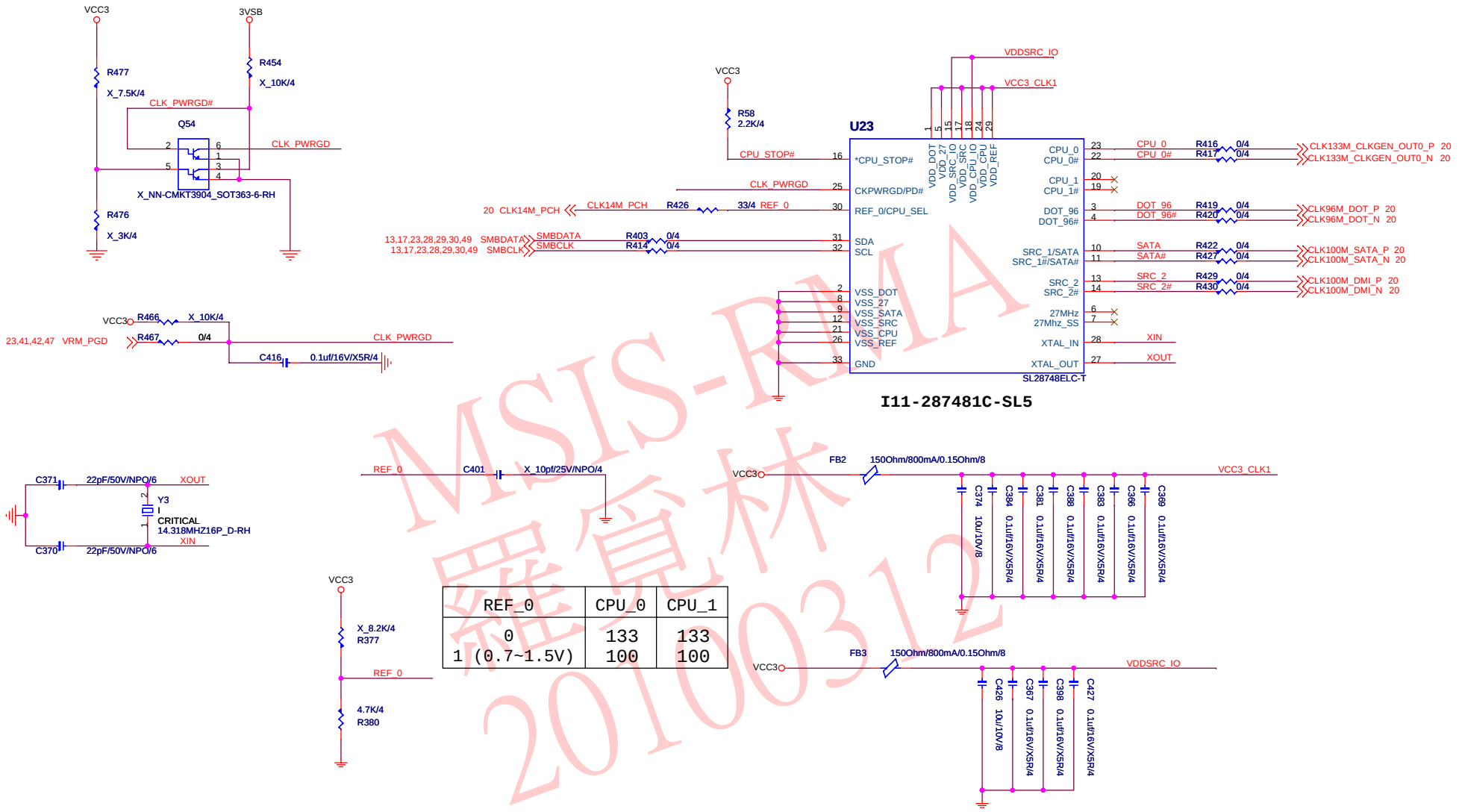
DDRIII DIMM_B2



MICRO-STAR INT'L CO.,LTD	
MS-7613	
Size: Custom	Document Description: Channel B DDR III DIMM 4
Rev: 11	
Date: Tuesday, January 19, 2010	Sheet 16 of 53



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: DIMM VREF (Option)	Rev: 11
Date: Tuesday, January 19, 2010	Sheet 17 of 53	



REF_0	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100

MICRO-STAR INT'L CO.,LTD	
MS-7613	
Size: Custom	Document Description: Clock Gen SLI SL28748ELC-T
Rev: 11	
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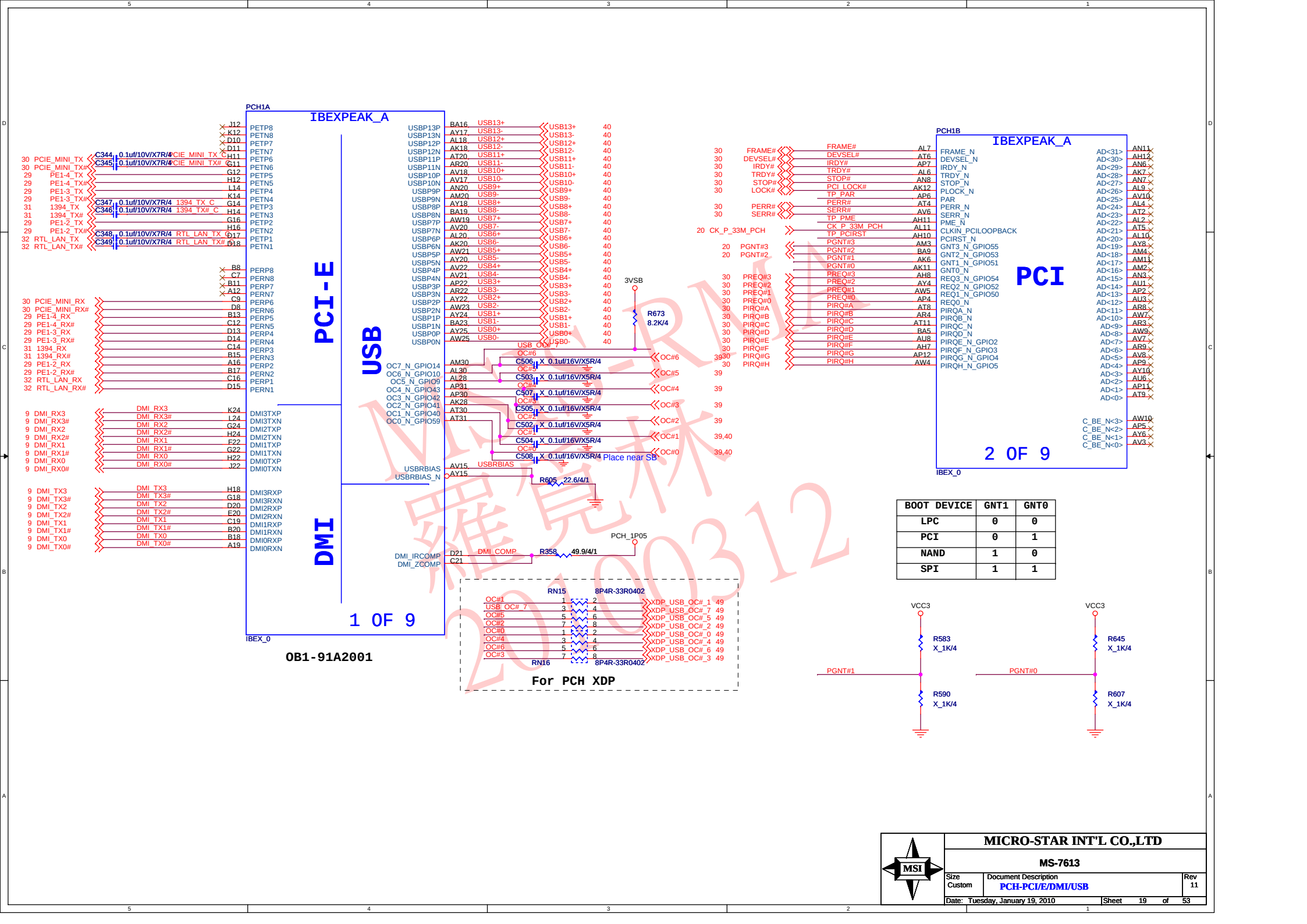

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	PCH-PCI/E/DMI/USB	11

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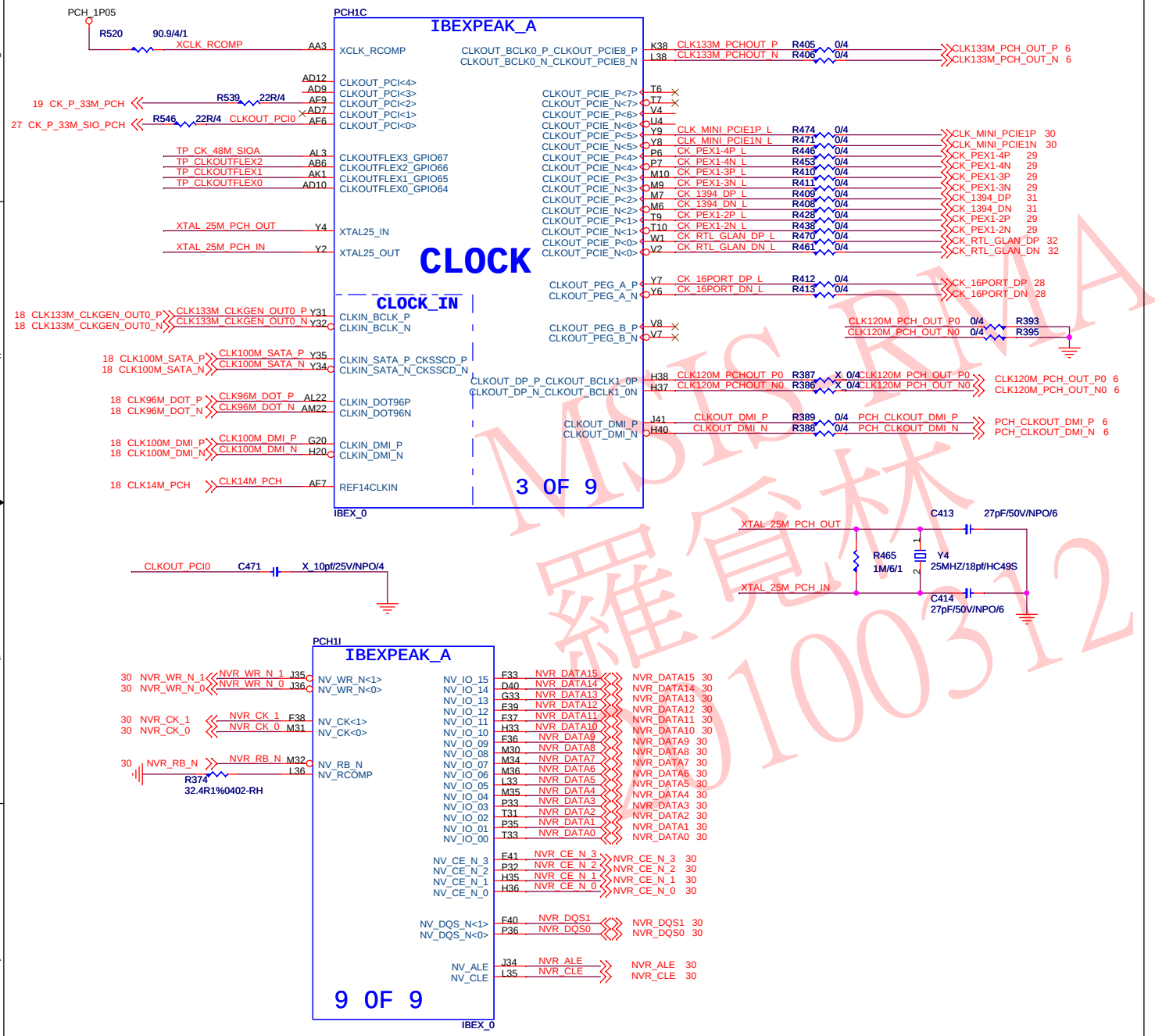

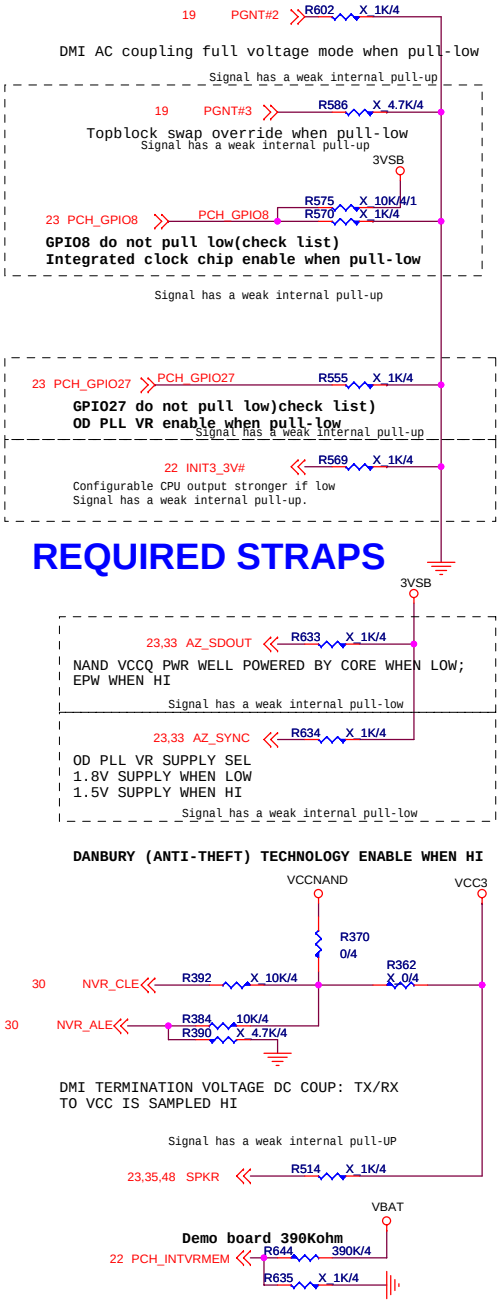

MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCH-CLOCK	Rev: 11
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PCH1F

IBEXPEAK_A

DISPLAY

6 OF 9

IBEX_0

R176 X_1K/4

37 DVI_DDPB_HPD → DVI_DDPB_HPD → H2 DDPD_HPD

R407 1K/4 → J3 DDPC_HPD

R418 1K/4 → J1 DDPB_HPD

TP_DDPD_AUXP → K4 DDPD_AUXP

TP_DDPD_AUXN → L4 DDPD_AUXN

L9 DDPC_AUXP

L10 DDPC_AUXN

TP_DDPB_AUXP → M1 DDPB_AUXP

TP_DDPB_AUXN → L2 DDPB_AUXN

37 DVI_DDPB_CLK_P	DVI_DDPB_CLK_P	F9	DDPD_TXP<3>
37 DVI_DDPB_CLK_N	DVI_DDPB_CLK_N	G9	DDPD_TXN<3>
37 DVI_DDPB_TXP2	DVI_DDPB_TXP2	F8	DDPD_TXP<2>
37 DVI_DDPB_TXN2	DVI_DDPB_TXN2	G8	DDPD_TXN<2>
37 DVI_DDPB_TXP1	DVI_DDPB_TXP1	D6	DDPD_TXP<1>
37 DVI_DDPB_TXN1	DVI_DDPB_TXN1	D7	DDPD_TXN<1>
37 DVI_DDPB_TXP0	DVI_DDPB_TXP0	C5	DDPD_TXP<0>
37 DVI_DDPB_TXN0	DVI_DDPB_TXN0	B6	DDPD_TXN<0>
		D3	DDPC_TXP<3>
		D2	DDPC_TXN<3>
		B4	DDPC_TXP<2>
		C4	DDPC_TXN<2>
		F2	DDPC_TXP<1>
		G3	DDPC_TXN<1>
		E3	DDPC_TXP<0>
		F4	DDPC_TXN<0>
TP_DDPB_TXP3		G4	DDPB_TXP<3>
TP_DDPB_TXN3		H4	DDPB_TXN<3>
TP_DDPB_TXP2		H6	DDPB_TXP<2>
TP_DDPB_TXN2		F6	DDPB_TXN<2>
TP_DDPB_TXP1		K11	DDPB_TXP<1>
TP_DDPB_TXN1		J11	DDPB_TXN<1>
TP_DDPB_TXP0		K10	DDPB_TXP<0>
TP_DDPB_TXN0		J8	DDPB_TXN<0>

M3 SDVO_INTP

N4 SDVO_ININ

N2 SDVO_STALLP

P3 SDVO_STALLN

L6 SDVO_TVCLKINP

L7 SDVO_TVCLKINN

FDI_RXP<7>	B34	FDI_TX7	FDI_TX7 9
FDI_RXN<7>	C33	FDI_TX7#	FDI_TX7# 9
FDI_RXP<6>	B32	FDI_TX6	FDI_TX6 9
FDI_RXN<6>	A33	FDI_TX6#	FDI_TX6# 9
FDI_RXP<5>	B31	FDI_TX5	FDI_TX5 9
FDI_RXN<5>	C30	FDI_TX5#	FDI_TX5# 9
FDI_RXP<4>	J31	FDI_TX4	FDI_TX4 9
FDI_RXN<4>	K31	FDI_TX4#	FDI_TX4# 9
FDI_RXP<3>	G31	FDI_TX3	FDI_TX3 9
FDI_RXN<3>	E31	FDI_TX3#	FDI_TX3# 9
FDI_RXP<2>	D32	FDI_TX2	FDI_TX2 9
FDI_RXN<2>	D31	FDI_TX2#	FDI_TX2# 9
FDI_RXP<1>	G30	FDI_TX1	FDI_TX1 9
FDI_RXN<1>	H30	FDI_TX1#	FDI_TX1# 9
FDI_RXP<0>	J30	FDI_TX0	FDI_TX0 9
FDI_RXN<0>	K30	FDI_TX0#	FDI_TX0# 9

FDI_LSYNC<1>	D35	FDI_LSYNC1	FDI_LSYNC1 9
FDI_LSYNC<0>	C35	FDI_LSYNC0	FDI_LSYNC0 9
FDI_FSYNC<1>	E36	FDI_FSYNC1	FDI_FSYNC1 9
FDI_FSYNC<0>	E34	FDI_FSYNC0	FDI_FSYNC0 9
FDI_INT	B36	FDI_INT	FDI_INT 9

DDPC_CTRLCLK	AB10		
DDPC_CTRLDATA	AB11		
DDPD_CTRLCLK	AB7	DVI_DDPB_CTRLCLK	DVI_DDPB_CTRLCLK 37
DDPD_CTRLDATA	AB9	DVI_DDPB_CTRLDATA	DVI_DDPB_CTRLDATA 37
SDVO_CTRLCLK	AB13	TP_SDVO_CTRLCLK	
SDVO_CTRLDATA	AB12	TP_SDVO_CTRLDATA	
CRT_HSYNC	AD4	VGA_HSYNC R507 33R0402	HSYNC 36
CRT_VSYNC	AD3	VGA_VSYNC R496 33R0402	VSYNC 36
CRT_RED	AC1		VGA_R 36
CRT_GREEN	AC3		VGA_G 36
CRT_BLUE	AB2		VGA_B 36
CRT_IRTN	AB4		
CRT_DDC_CLK	AG2	RGB_DDC_CLK	RGB_DDC_CLK 36
CRT_DDC_DATA	AG4	RGB_DDC_DATA	RGB_DDC_DATA 36
CRT_IREF	AE2	VGA_DACSET R521 1.02K/4/1	

Demoboard 1.02K
EDS 255ohm

VGA DACSET
RESISTORS CLOSE
TO MCH(500 MILS
TO MCH BALLS)

SPI DEBUG PROT

Close to SPI ROM

VCC3 VCC3

JSPI1

SPI_MISO_F 3 4 SPI_MOSI_F

SPI_CS0_F# 5 6 SPI_CLK_F

7 8

SPI_HOLD# 9

R375 0/4

SPI_CS1_F# R376 X_0/4

H2X5[1]_BLACK-RH

Part Number:N31-2051451-H06

SPI FLASH ROM

VCC3 C434 0.1uf/16V/X5R/4

C338 C10u10Y0805

VCC3 R356 2.2KR/2

23 SPI_CS0_F#
23 SPI_MISO
23 SPI_WP#

SPI_CS0_F#
SPI_MISO R329 15R/2 SPI_MISO_F
SPI_WP#

From South-Bridge GPIO32

VCC3 R342 2.2KR/2

U19

1	CS	VCC	8
2	DO	HOLD	7
3	WP	CLK	6
4	GND	DIO	5

W25Q64BVSSIG

SPI_HOLD#
SPI_CLK_F
SPI_MOSI_F

R355 X_0/4 SPI_HOLD_GPO# SPI_HOLD_GPO# 23

From South-Bridge GPIO33

SPI_CLK_F 23
SPI_MOSI_F 23

M31-25Q6403-W03

VCC3

R549 2.2KR/2 R550 2.2KR/2

DVI_DDPB_CTRLCLK

DVI_DDPB_CTRLDATA

23 SPI_CS1_F#

SPI_CS1_F#
SPI_MISO_F
SPI_WP#

U18

1	CS	VCC	8
2	DO	HOLD	7
3	WP	CLK	6
4	GND	DIO	5

X_W25X32VSSIG-RH

SPI_HOLD#
SPI_CLK_F
SPI_MOSI_F

M31-25X3203-W03

R360 is TEST POINT closer Chipset

DVI_DDPB_CLK_P

R360 X_10M/4

DVI_DDPB_CLK_N

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MS-7613	
Size: Custom	Document Description: PCH-DISPLAY/ SPI ROM
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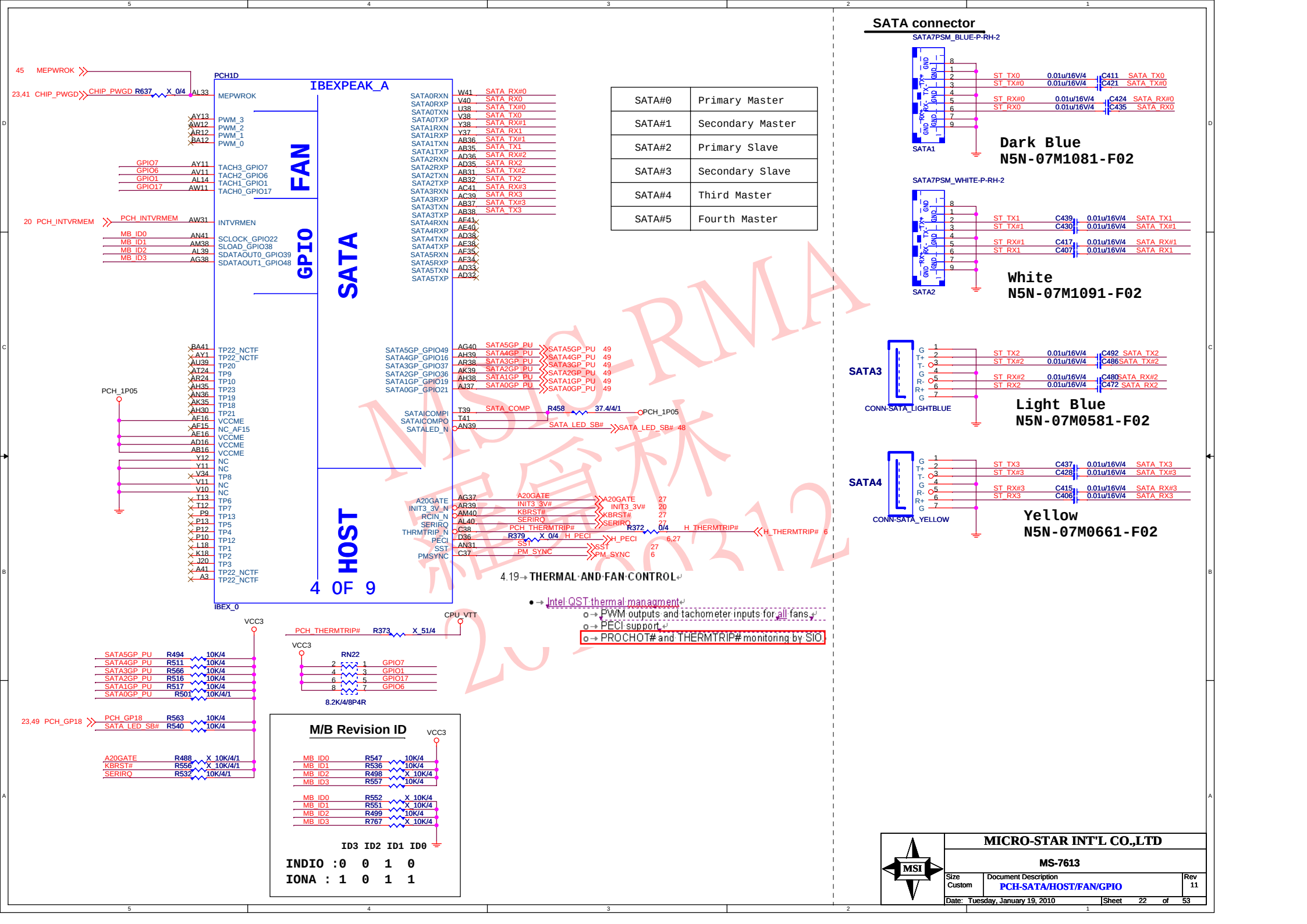
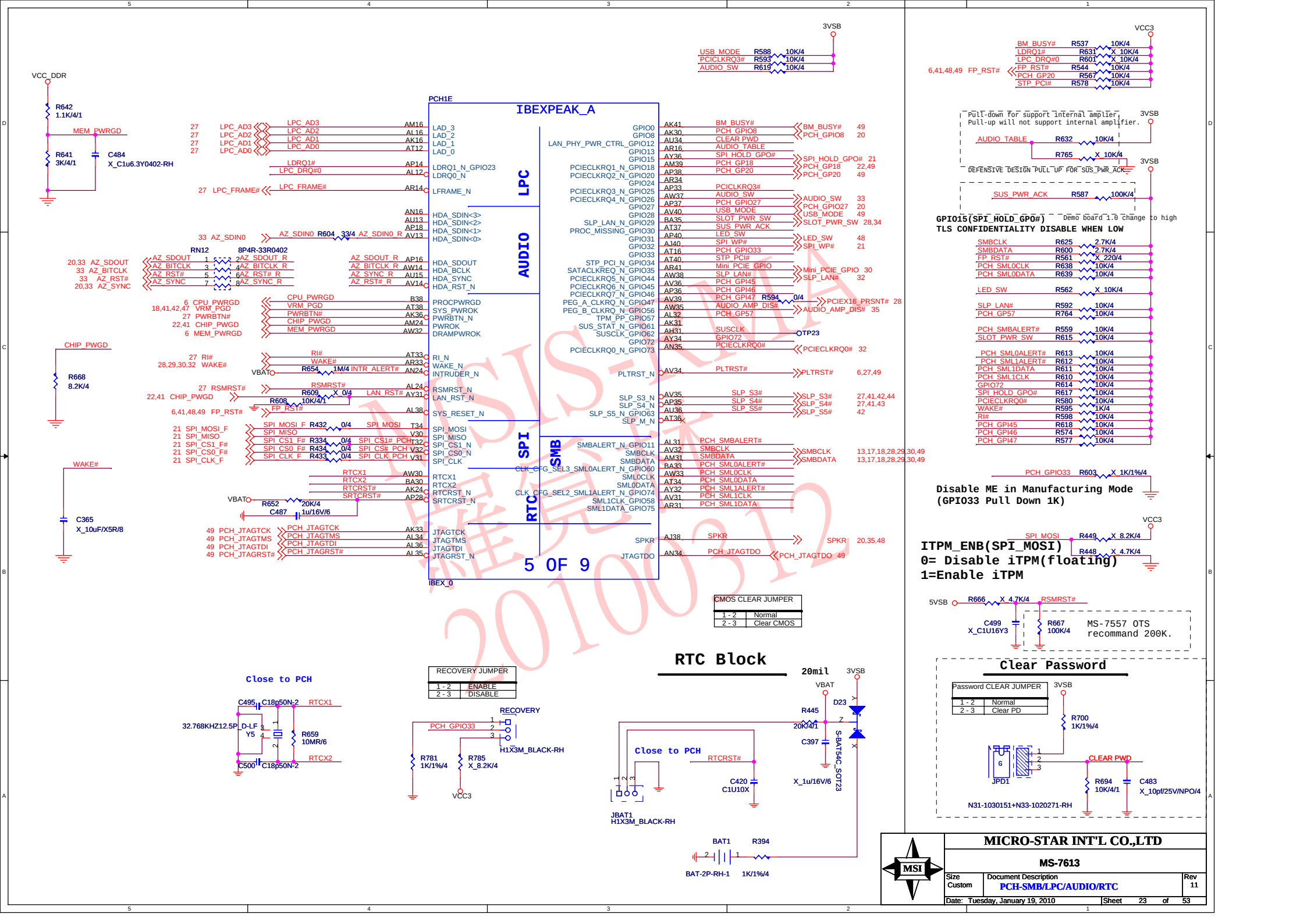
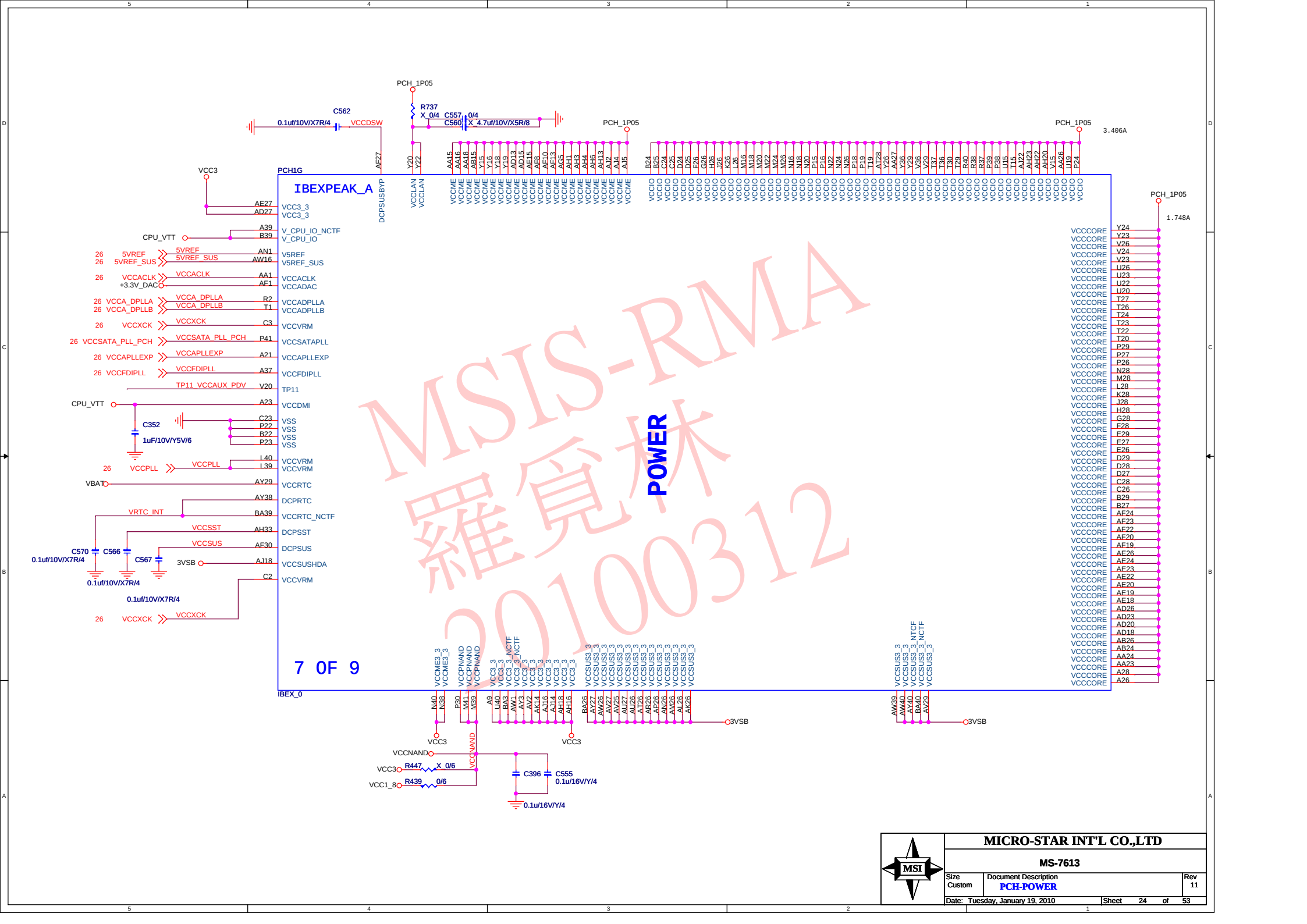


SATA#0	Primary Master
SATA#1	Secondary Master
SATA#2	Primary Slave
SATA#3	Secondary Slave
SATA#4	Third Master
SATA#5	Fourth Master

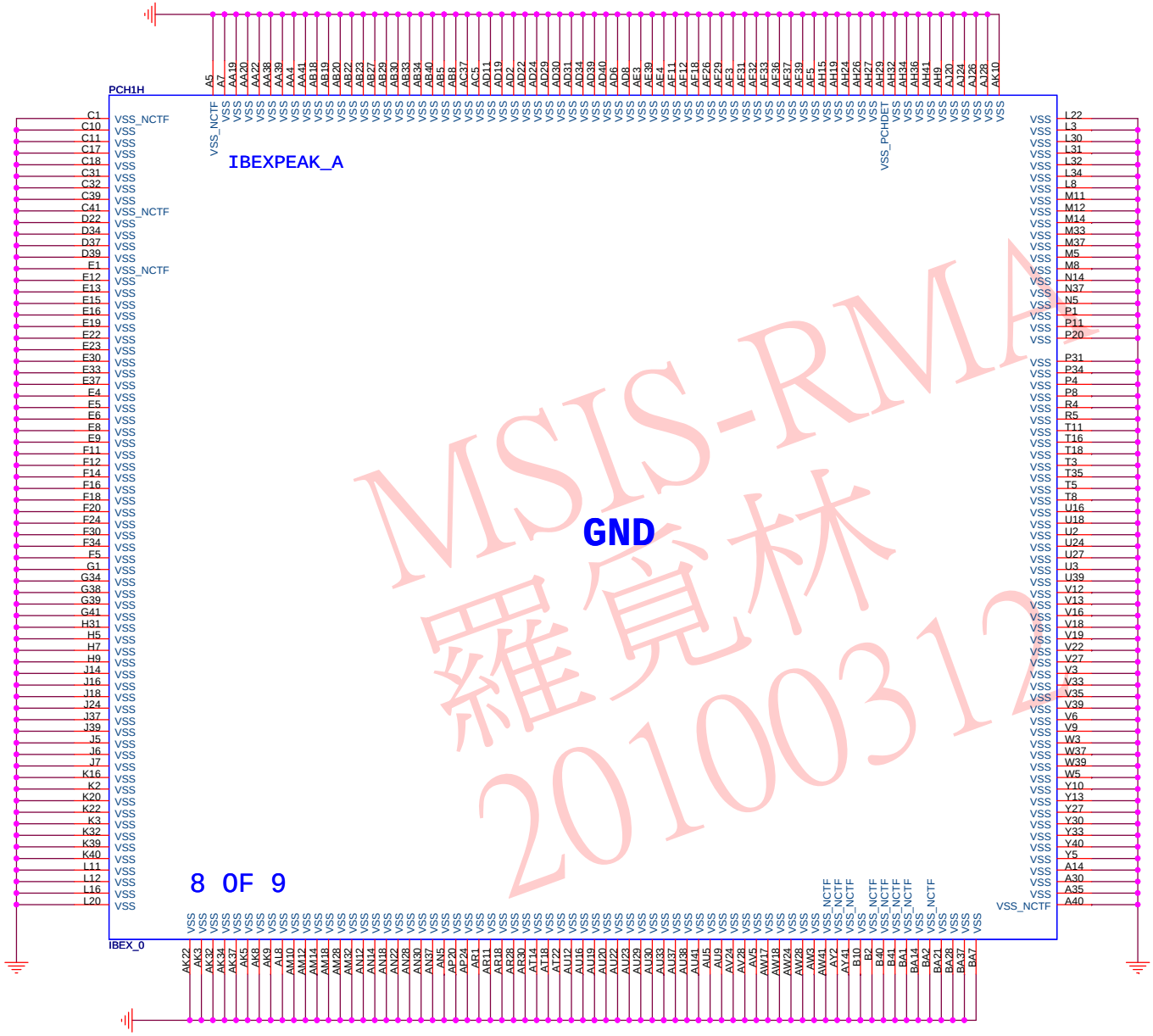
SATA connector

MICRO-STAR INT'L CO.,LTD	
MS-7613	
Size: Custom	Document Description: PCH-SATA/HOST/FAN/GPIO
Rev: 11	
Date: Tuesday, January 19, 2010	Sheet 22 of 53


PCH1E
IBEXPEAK_A
LPC
AUDIO
SPI
SMB
RTC
5 0F 9
IBEX_0
RTC Block
Close to PCH
Clear Password
MS-7557 OTS recommand 200K.
ITPM_ENB(SPI_MOSI)
0= Disable iTPM(floating)
1=Enable iTPM
Disable ME in Manufacturing Mode (GPIO33 Pull Down 1K)
GPIO15(SPI_HOLD_GPO#)
TLS CONFIDENTIALITY DISABLE WHEN LOW
CMOS CLEAR JUMPER
RECOVERY JUMPER
Password CLEAR JUMPER
MICRO-STAR INT'L CO.,LTD
MS-7613
PCH-SMB/LPC/AUDIO/RTC
Tuesday, January 19, 2010



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCH-POWER	Rev: 11
Date: Tuesday, January 19, 2010	Sheet 24 of 53	



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCH-GND	Rev: 11
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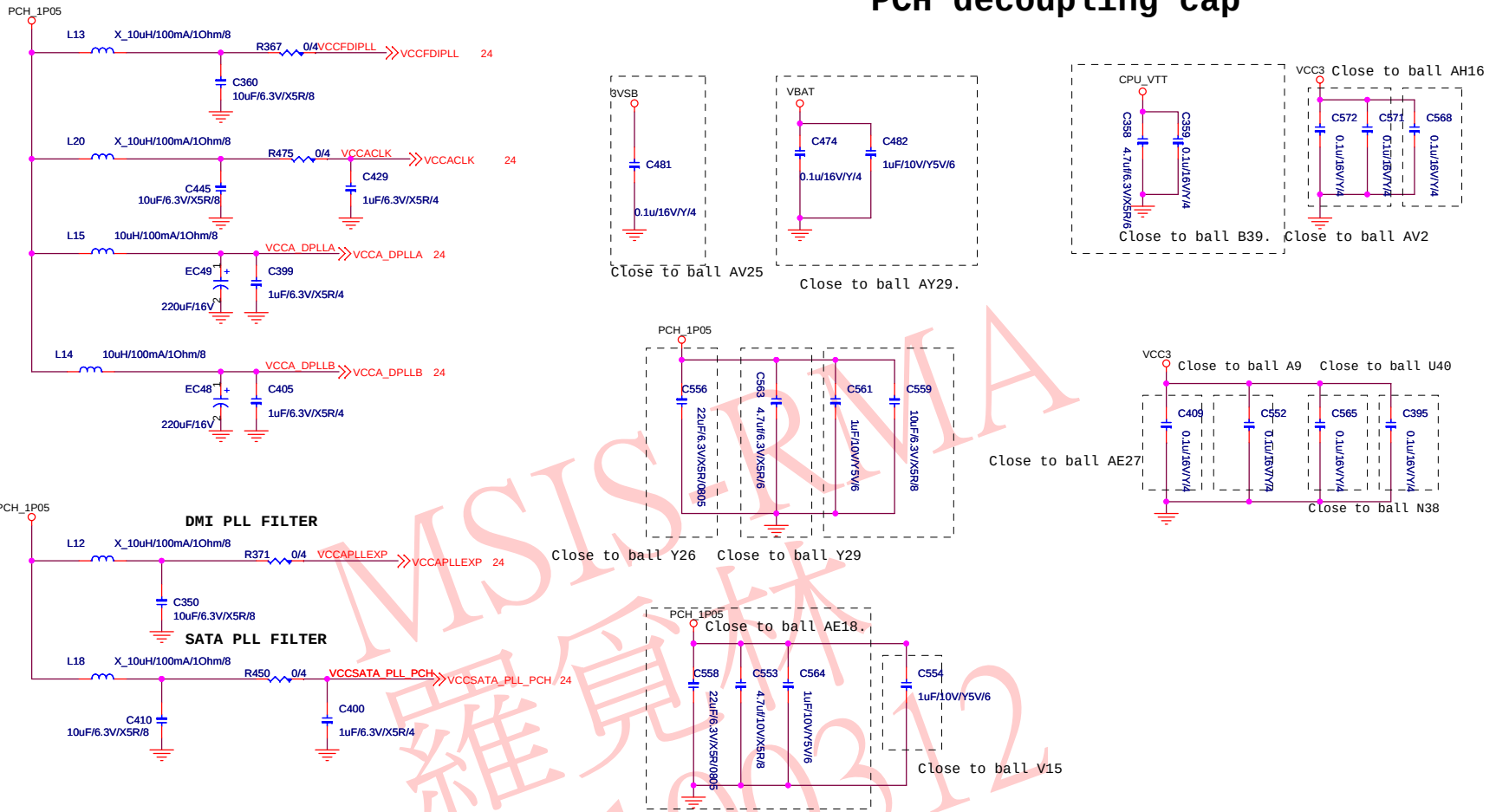
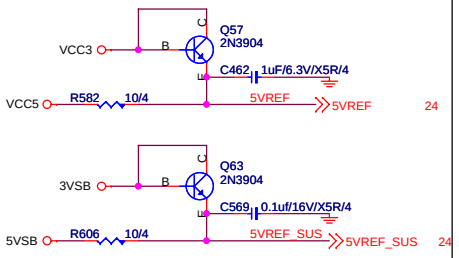
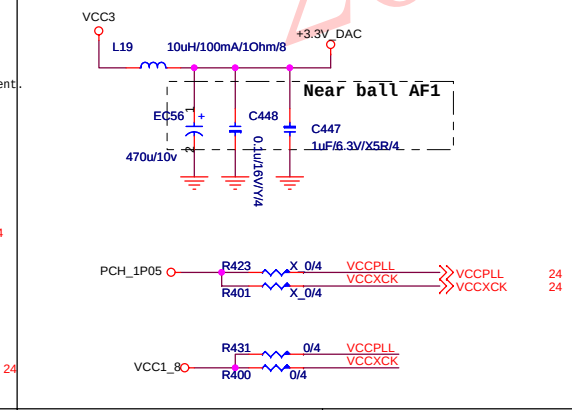
PCH decoupling cap



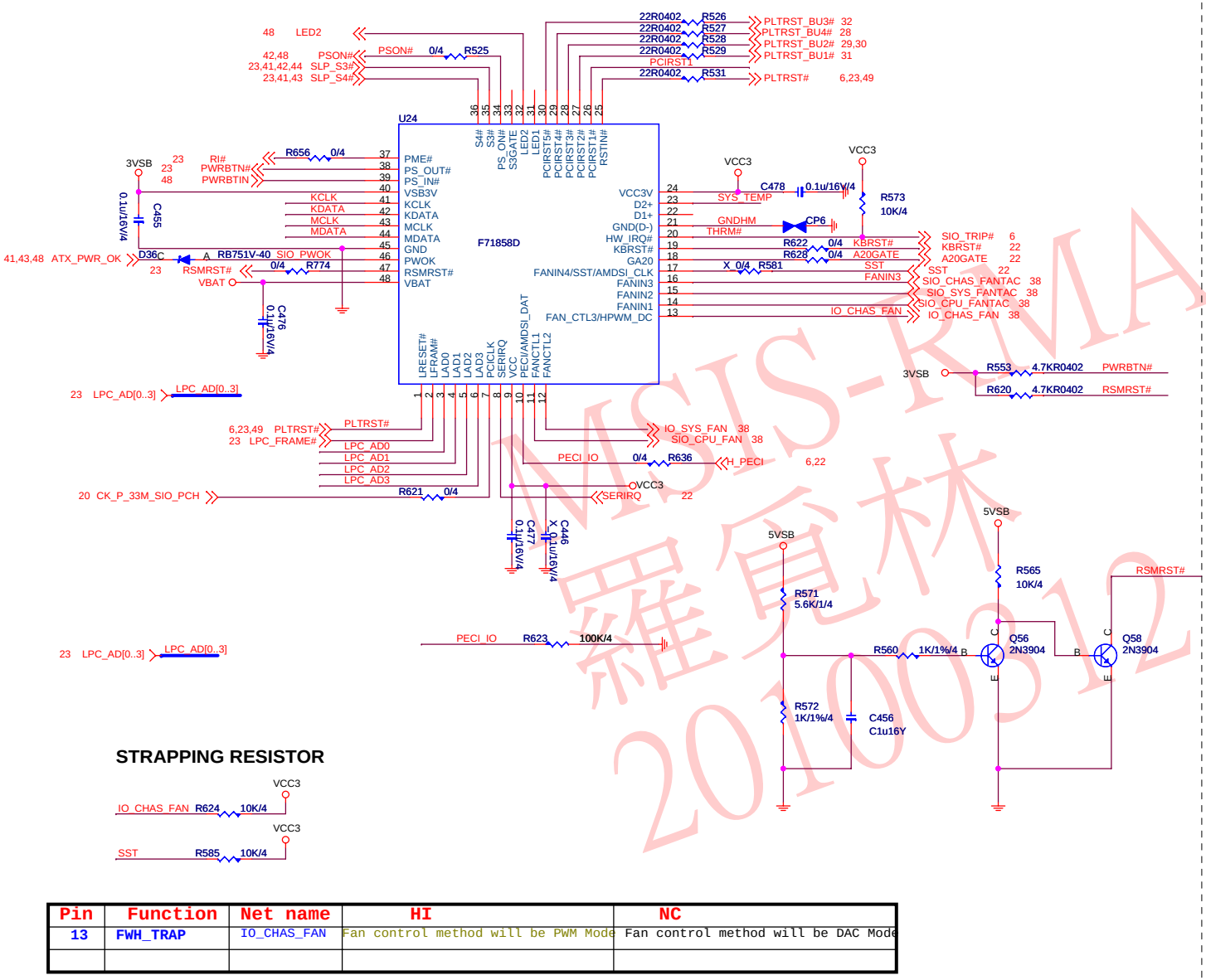
5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.





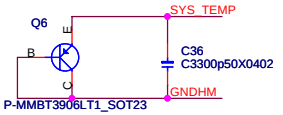
MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCH-DECOPLING	Rev: 11
Date: Tuesday, January 19, 2010	Sheet 26 of 53	



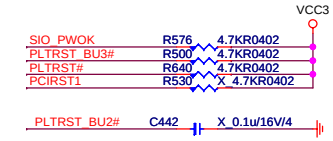
STRAPPING RESISTOR

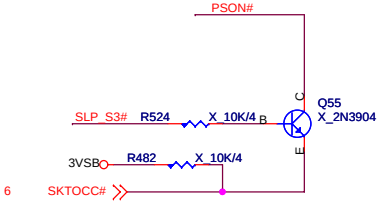
Pin	Function	Net name	HI	NC
13	FWH_TRAP	IO_CHAS_FAN	Fan control method will be PWM Mode	Fan control method will be DAC Mode

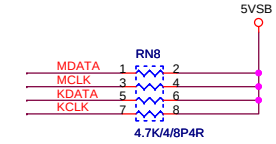
SYSTEM TEMP

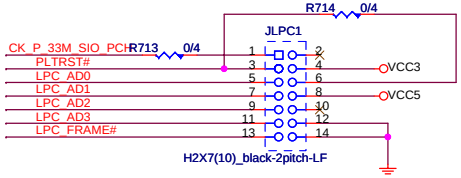


near the PWM MOS









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Size: Custom	Document Description: IO-Fintek F71858D	Rev: 11
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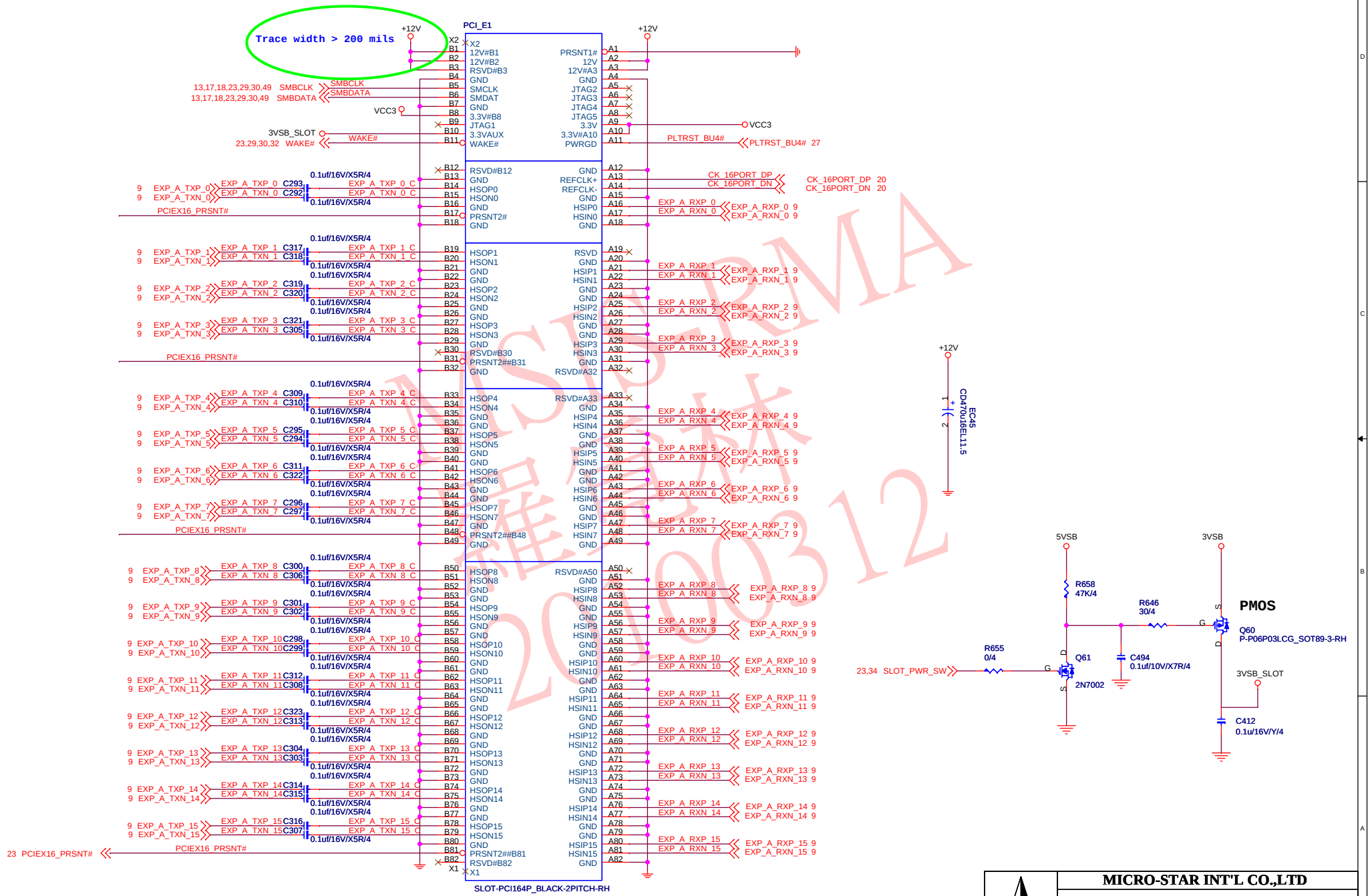
PCI_Express X16 Slot



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCIE X16 SLOT	Rev: 11
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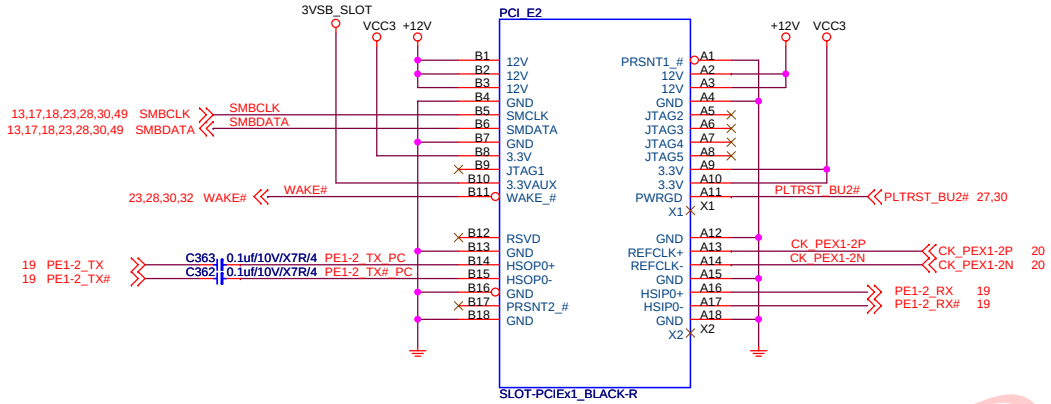
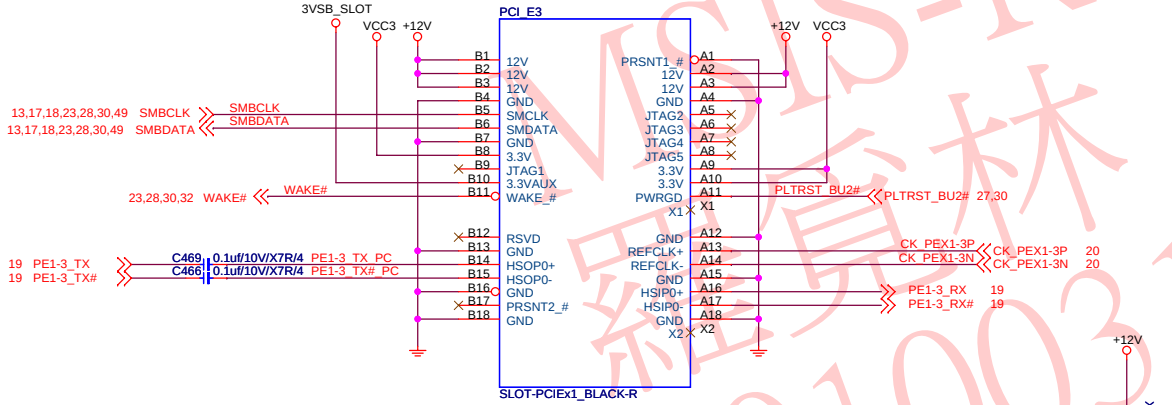
PCI EXPRESS x1-PORT1



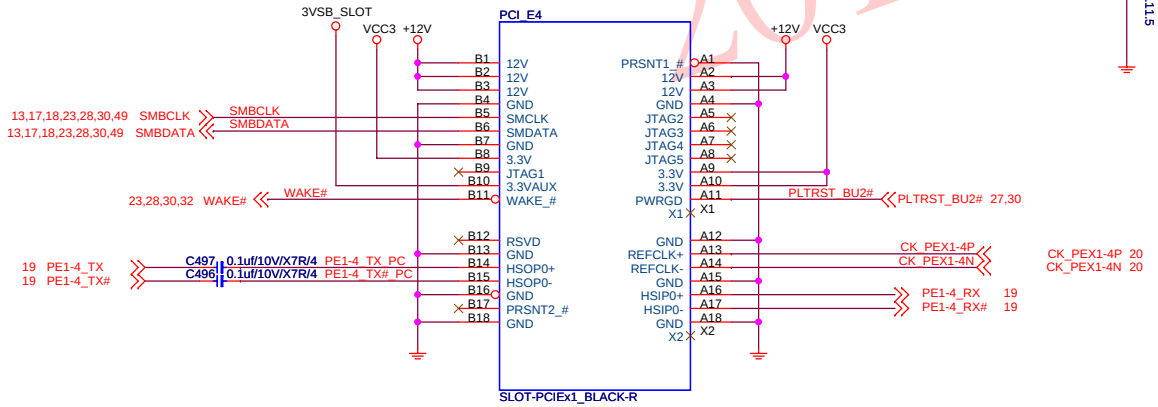
N11-0360281-K06

PCI EXPRESS x1-PORT2



N11-0360281-K06

PCI EXPRESS x1-PORT3



N11-0360281-K06

MICRO-STAR INT'L CO.,LTD		
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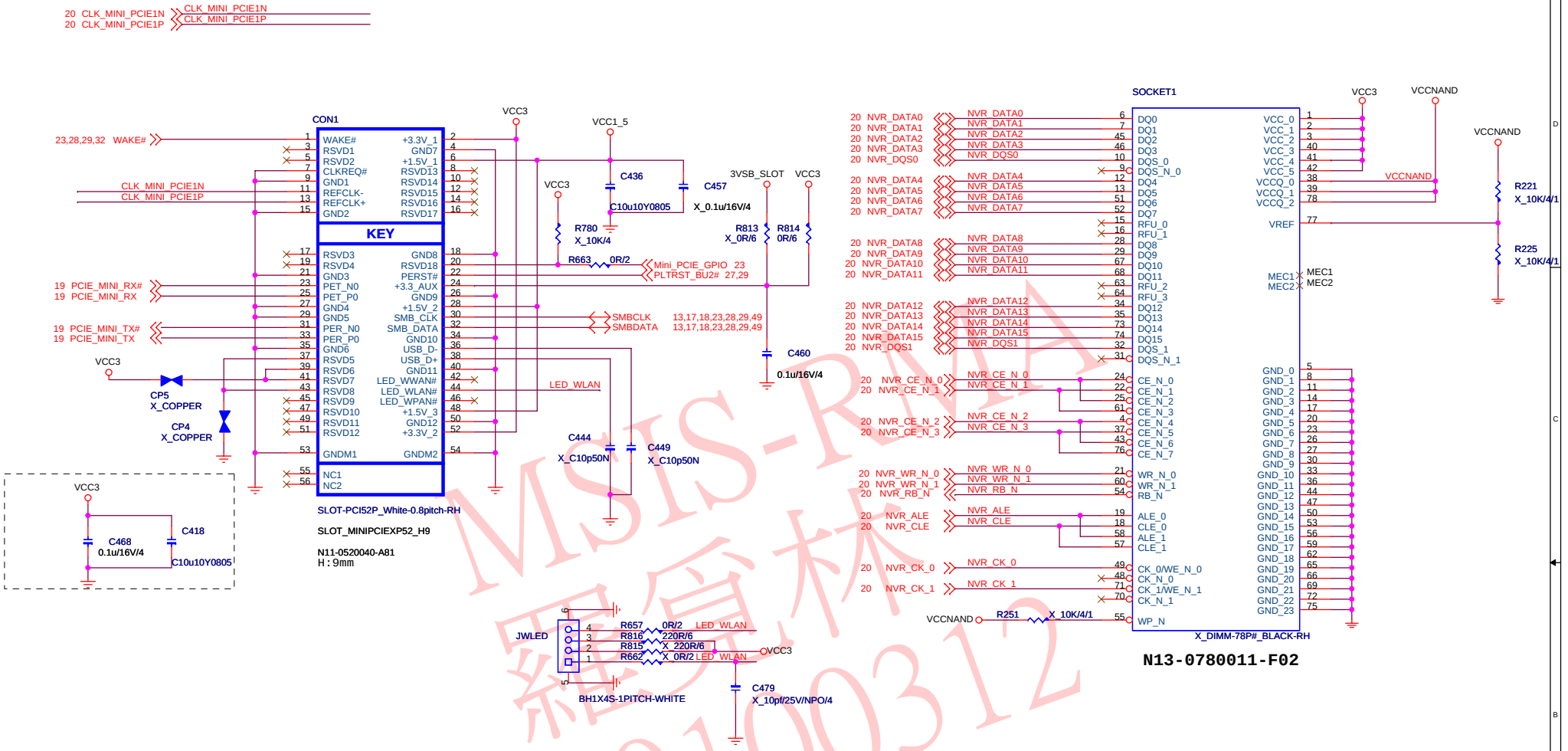
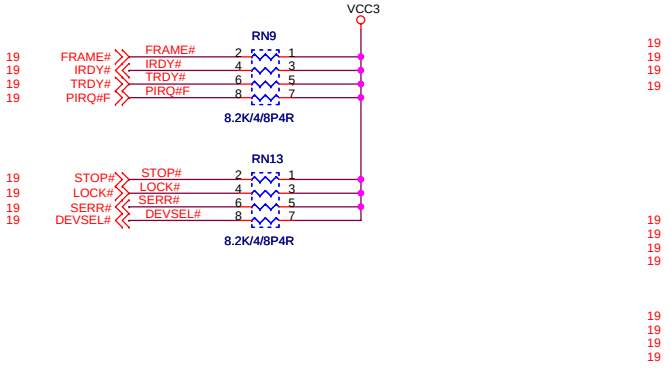
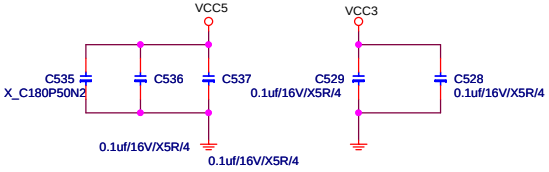


PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: Mini PCI_E Slot & ONFI Slot	Rev: 11
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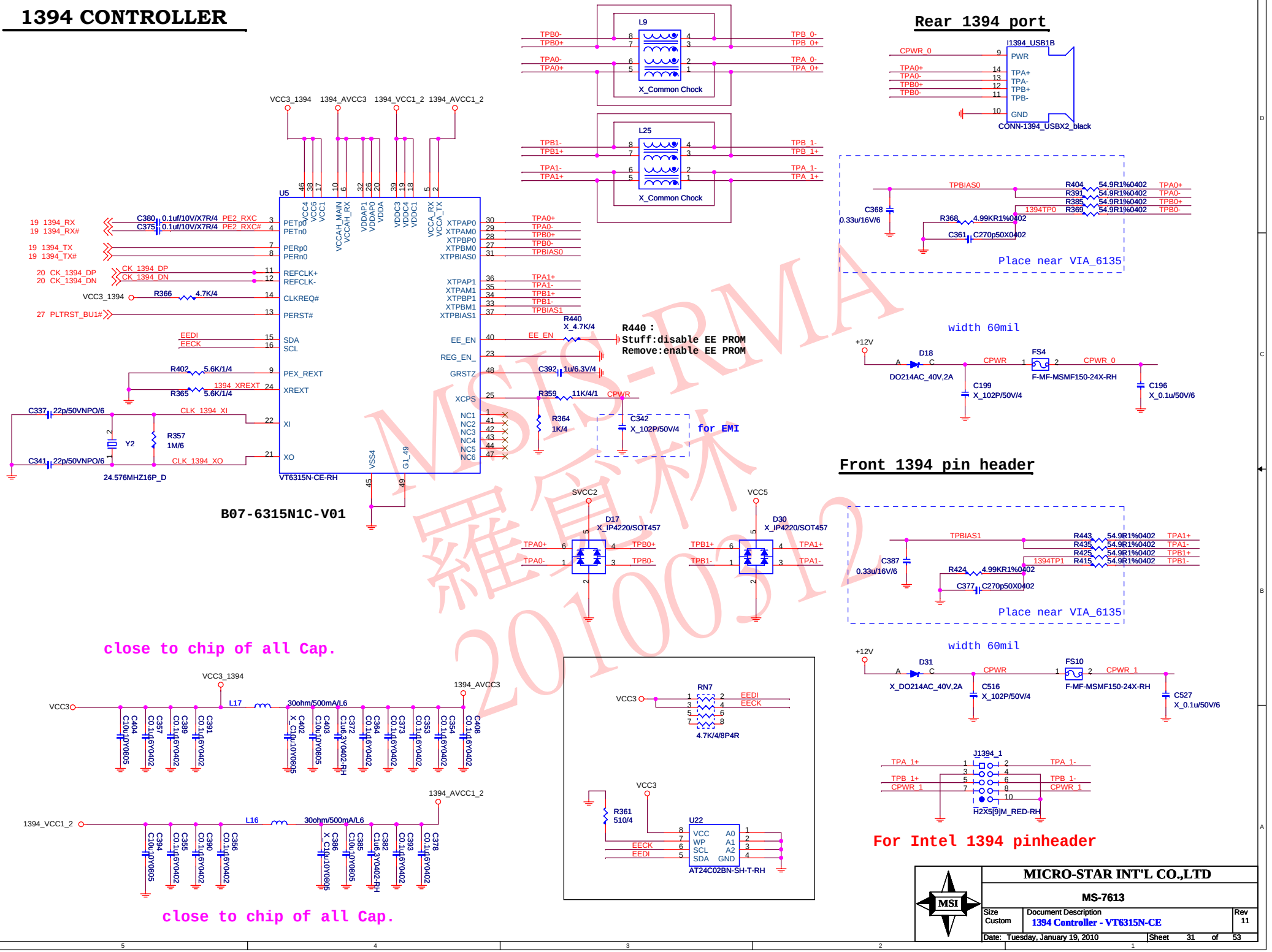
1394 CONTROLLER



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: 1394 Controller - VT6315N-CE	Rev: 11
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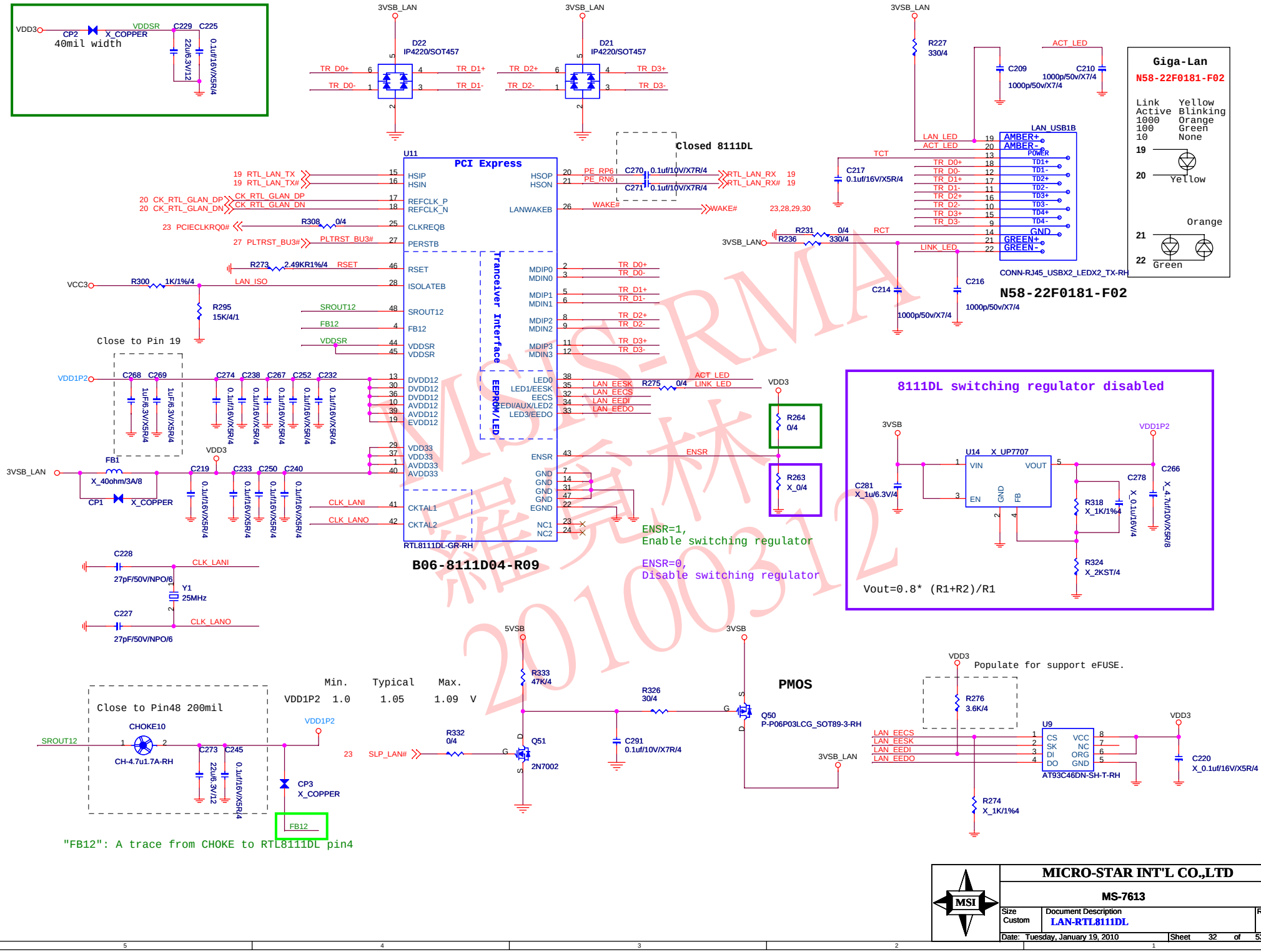

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7613	
Size: Custom	Document Description: LAN-RTL8111DL	Rev: 11
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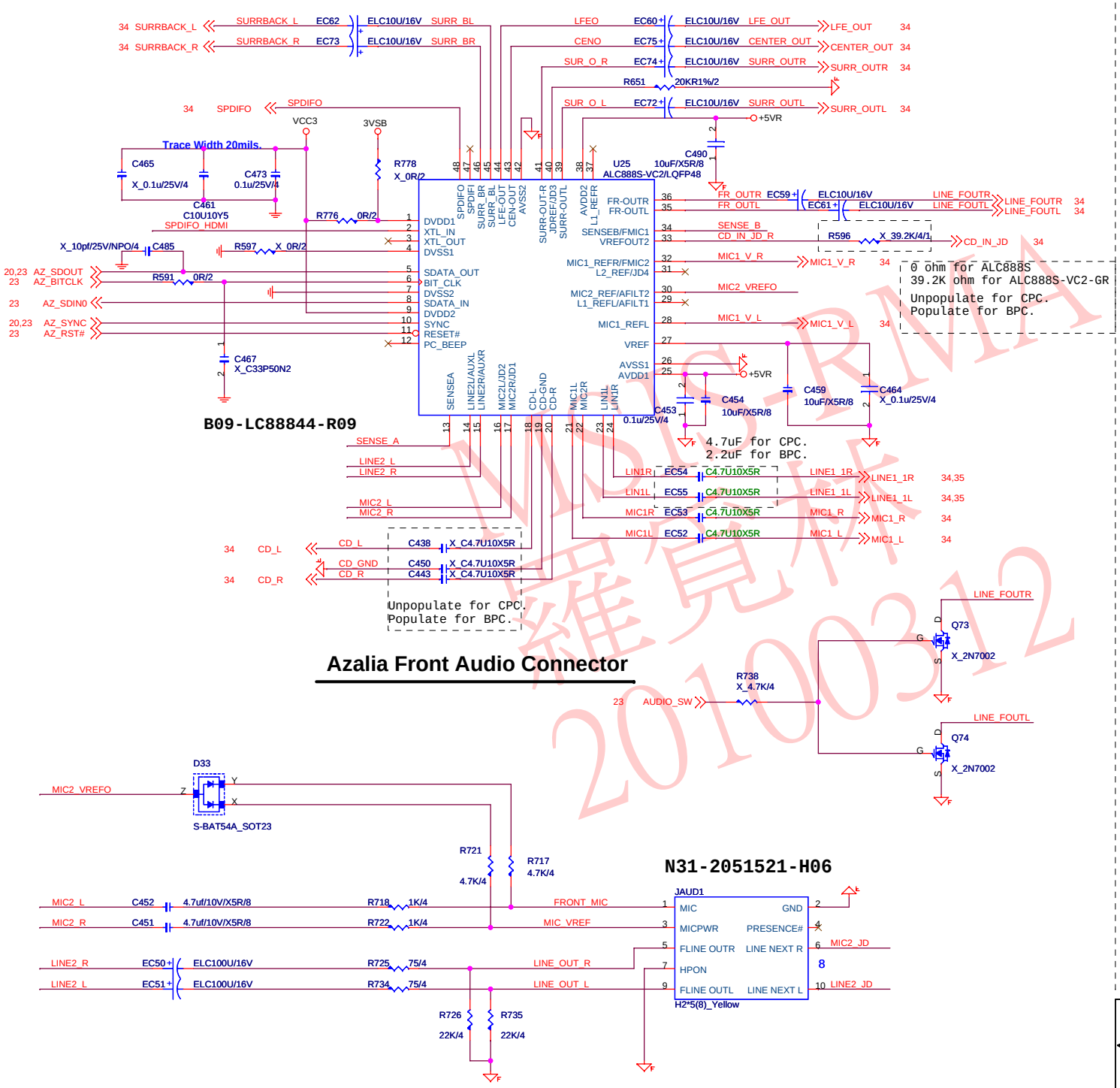
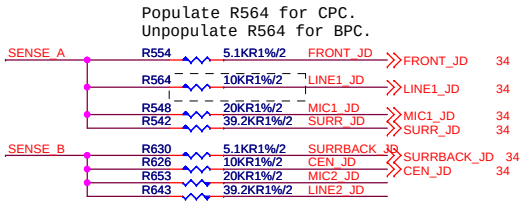
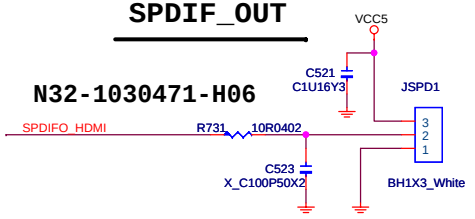
ALC888S CODEC

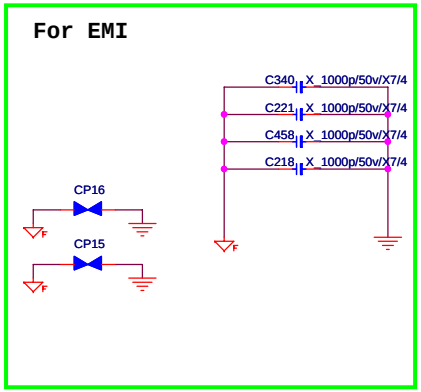


ALC888S JACK DETECT



SPDIF_OUT





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MS-7613		
Size: Custom	Document Description: Audio Codec ALC888S-VC2	Rev: 11
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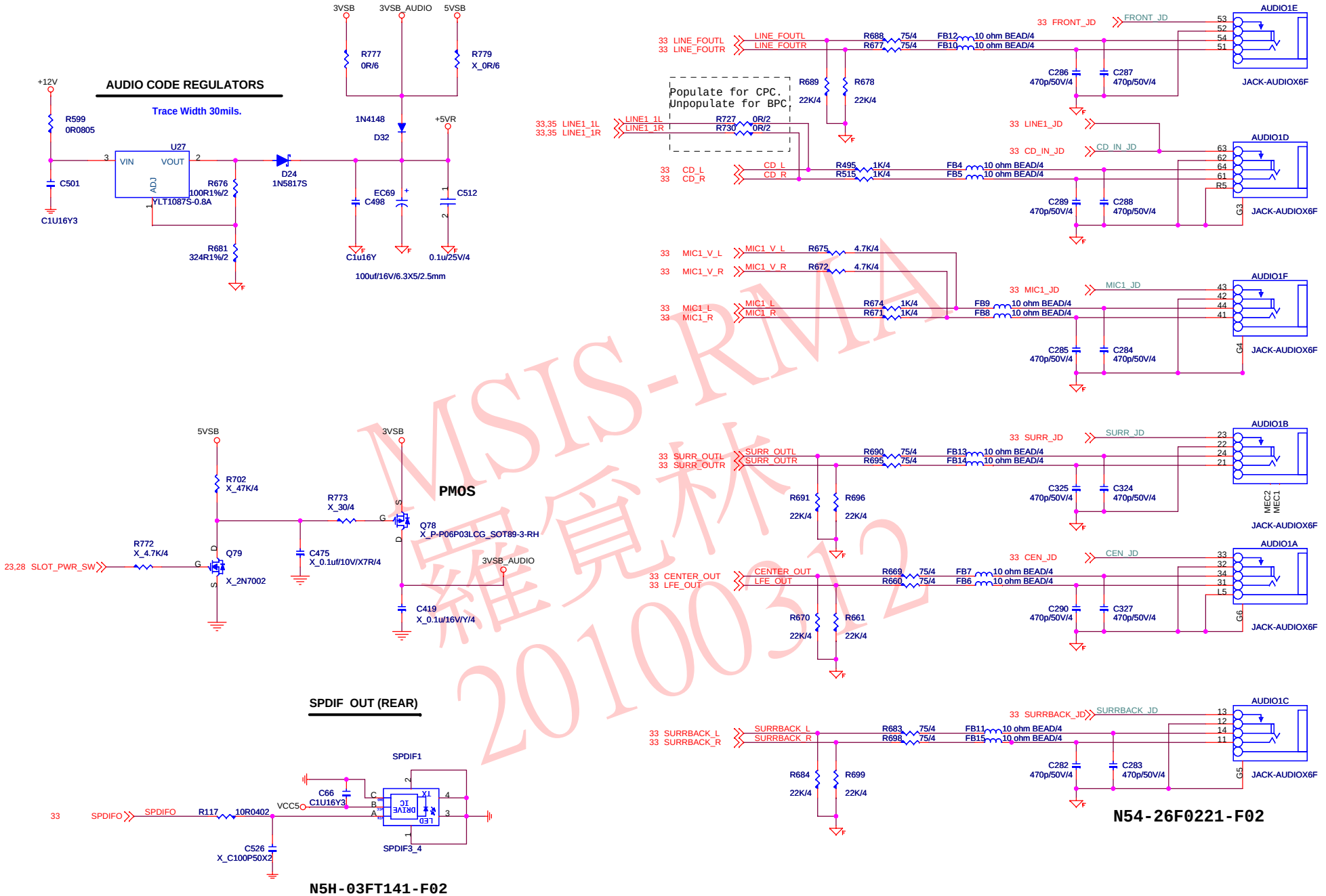
AUDIO CODE REGULATORS
Trace Width 30mils.
+12V
R599
0R0805
C501
C1U16Y3
U27
VIN
VOUT
ADJ
YLT10875-0.8A
R676
100R1%/2
R681
324R1%/2
D24
1N5817S
3VSB
3VSB_AUDIO
5VSB
R777
0R/6
R779
X_0R/6
1N4148
D32
+5VR
EC69
C498
C1u16Y
C512
0.1u/25V/4
100uf/16V/6.3X5/2.5mm
Populate for CPC.
Unpopulate for BPC
33,35 LINE1_1L
33,35 LINE1_1R
LINE1_1L
LINE1_1R
R727
R730
0R/2
33 CD_L
33 CD_R
CD_L
CD_R
R495
R515
1K/4
33 LINE_FOUTL
33 LINE_FOUTR
LINE_FOUTL
LINE_FOUTR
R688
R677
75/4
FB12
FB10
10 ohm BEAD/4
R689
R678
22K/4
33 FRONT_JD
FRONT_JD
C286
C287
470p/50V/4
AUDIO1E
JACK-AUDIOX6F
33 LINE1_JD
33 CD_IN_JD
CD_IN_JD
AUDIO1D
FB4
FB5
C289
C288
33 MIC1_V_L
33 MIC1_V_R
MIC1_V_L
MIC1_V_R
R675
R672
4.7K/4
33 MIC1_L
33 MIC1_R
MIC1_L
MIC1_R
R674
R671
1K/4
FB9
FB8
33 MIC1_JD
MIC1_JD
AUDIO1F
C285
C284
5VSB
3VSB
R702
X_47K/4
R773
X_30/4
PMOS
Q78
X_P-P06P03LCG_SOT89-3-RH
R772
X_4.7K/4
23,28 SLOT_PWR_SW
Q79
X_2N7002
C475
X_0.1uf/10V/X7R/4
3VSB_AUDIO
C419
X_0.1u/16V/Y/4
33 SURR_OUTL
33 SURR_OUTR
SURR_OUTL
SURR_OUTR
R690
R695
FB13
FB14
33 SURR_JD
SURR_JD
AUDIO1B
R691
R696
C325
C324
MEC2
MEC1
33 CENTER_OUT
33 LFE_OUT
CENTER_OUT
LFE_OUT
R669
R660
FB7
FB6
33 CEN_JD
CEN_JD
AUDIO1A
R670
R661
C290
C327
SPDIF OUT (REAR)
SPDIF1
33
SPDIFO
R117
10R0402
VCC5
C66
C1U16Y3
C526
X_C100P50X2
SPDIF3_4
N5H-03FT141-F02
33 SURRBACK_L
33 SURRBACK_R
SURRBACK_L
SURRBACK_R
R683
R698
FB11
FB15
33 SURRBACK_JD
SURRBACK_JD
AUDIO1C
R684
R699
C282
C283
N54-26F0221-F02
MSIS-RMA
羅覓林
20100312
MICRO-STAR INT'L CO.,LTD
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Custom
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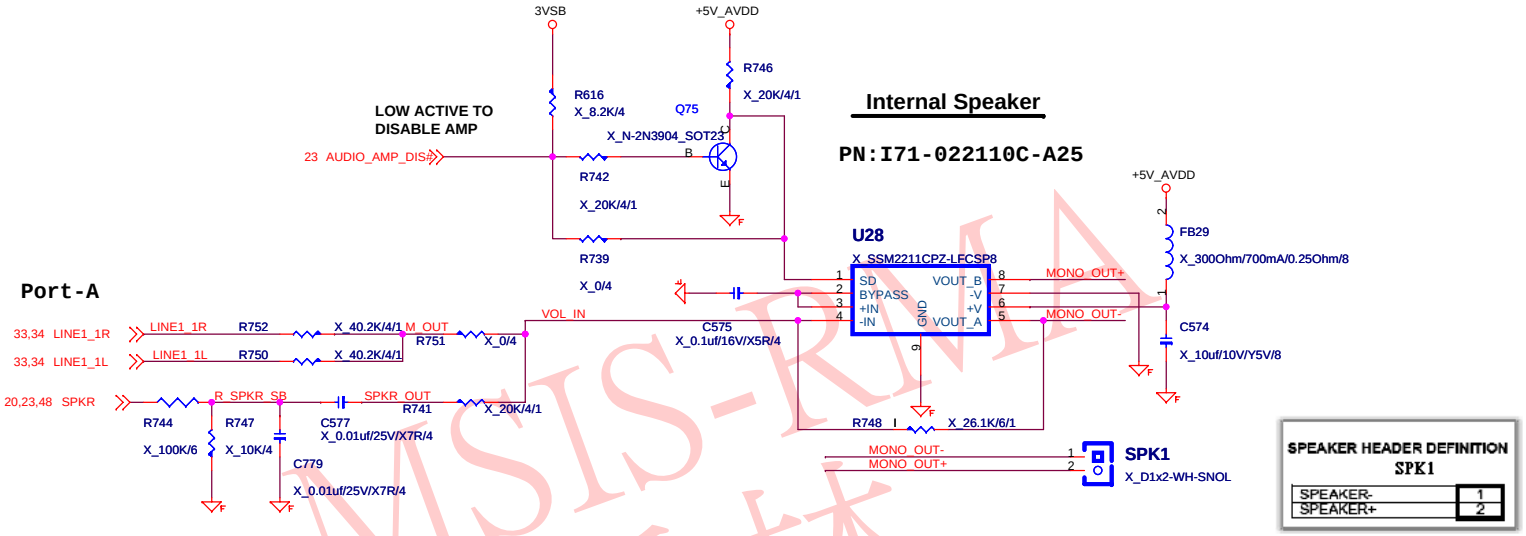
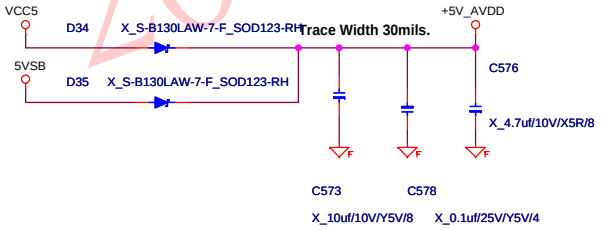


AUDIO AMPLIFIER POWER REGULATORS



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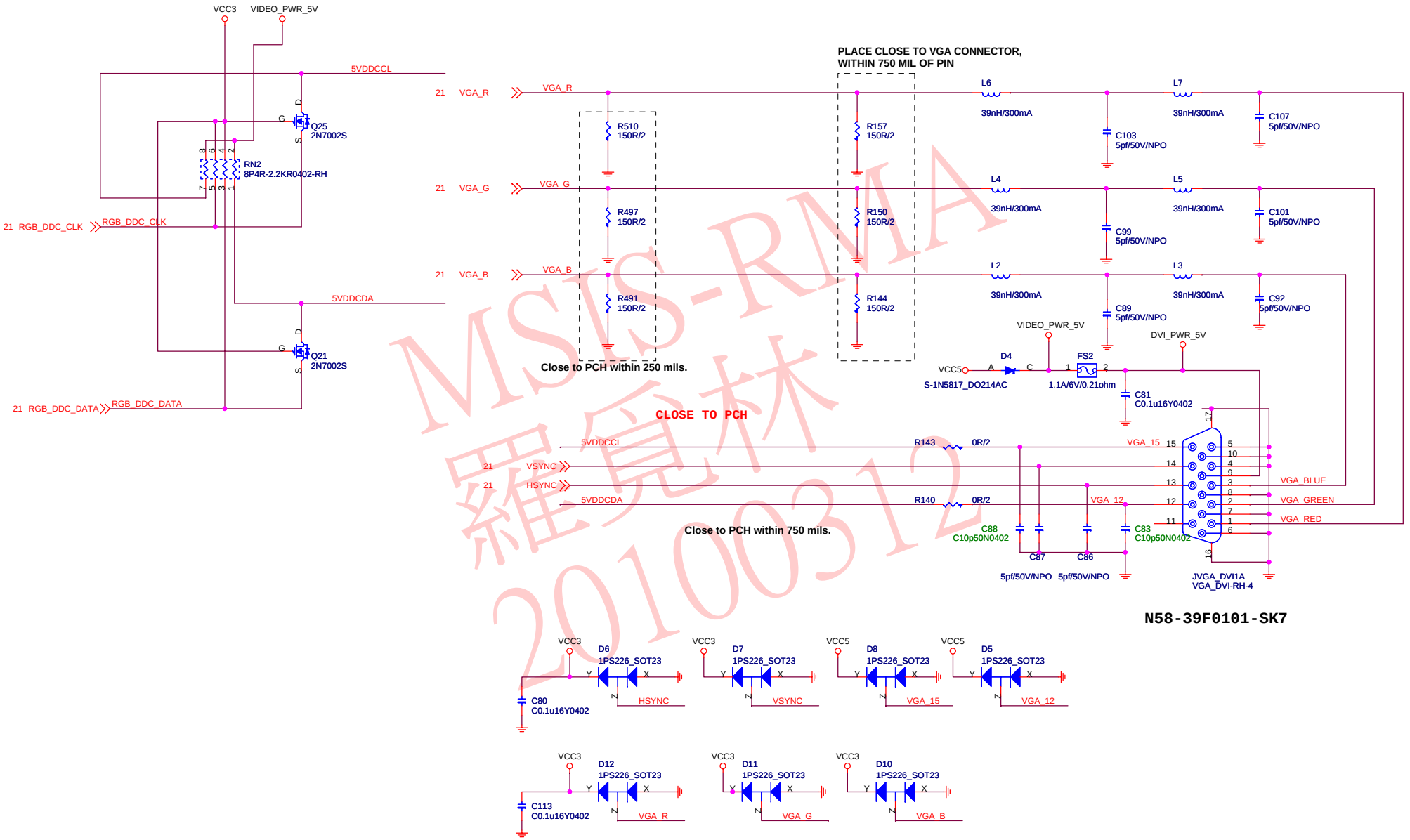
Video Connector



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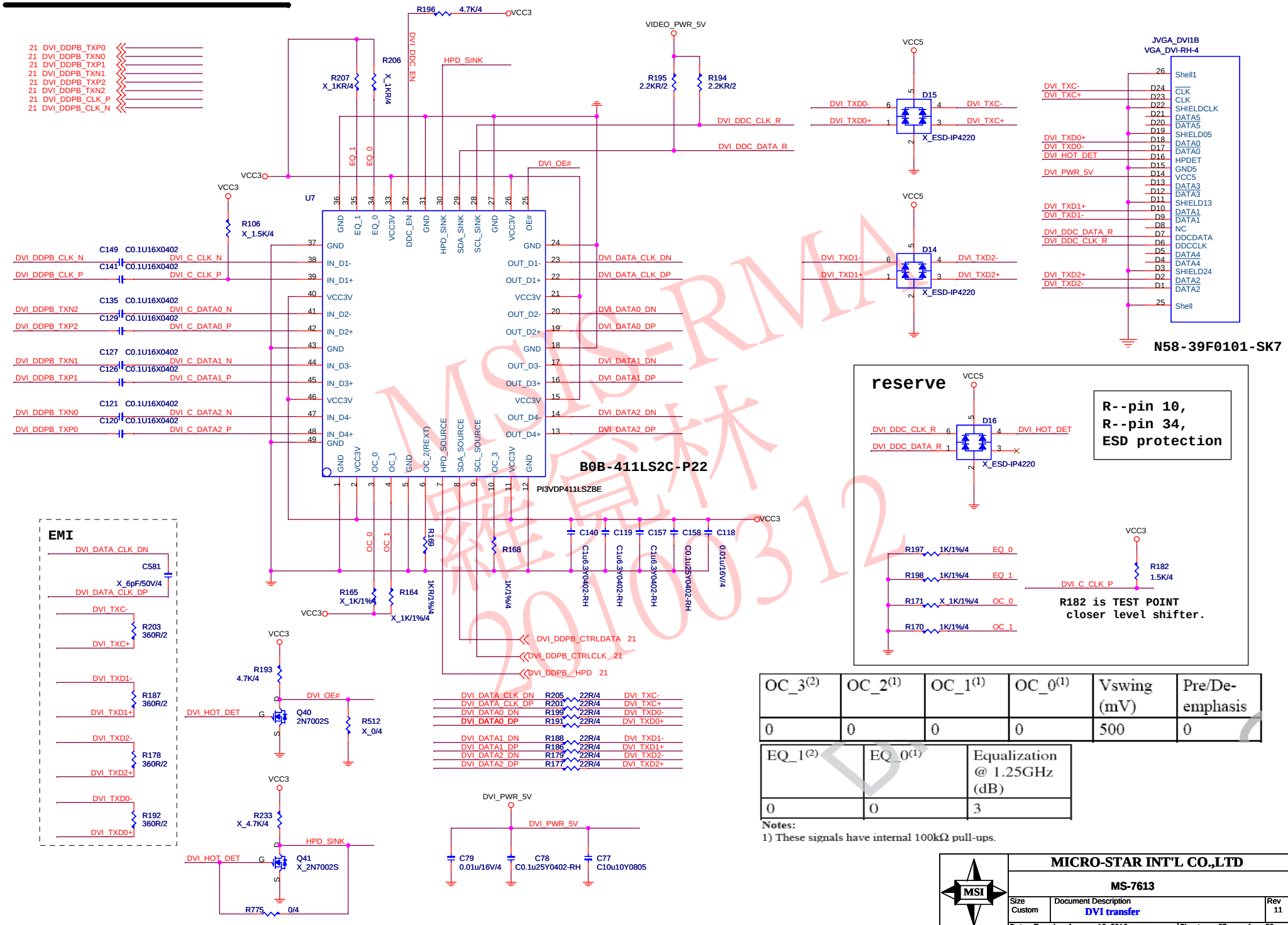
DVI level shifter



OC_3(2)	OC_2(1)	OC_1(1)	OC_0(1)	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0

EQ_1(2)	EQ_0(1)	Equalization @ 1.25GHz (dB)
0	0	3

Notes:

1) These signals have internal 100kΩ pull-ups.

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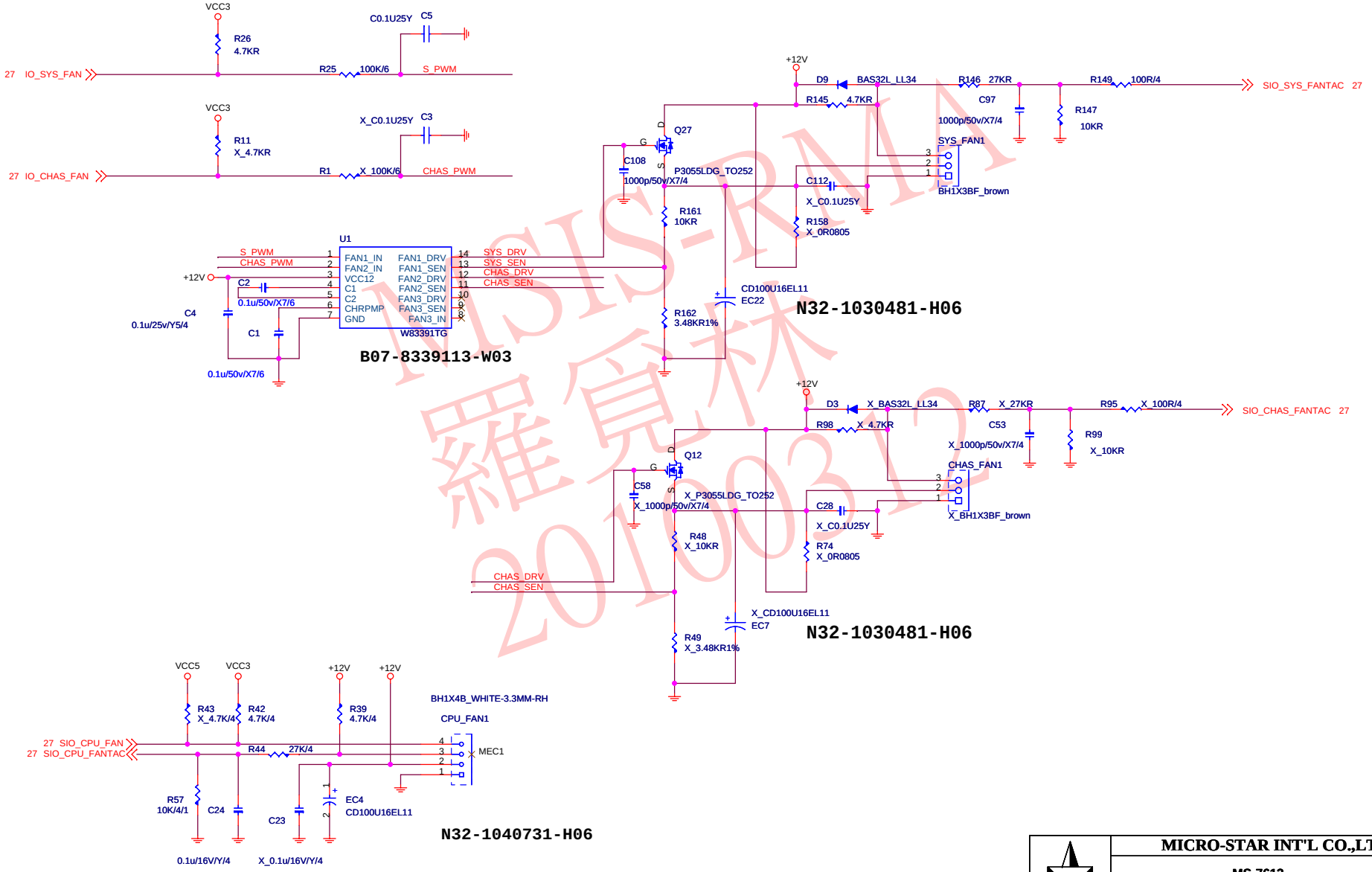
FAN-COUNTROL CIRCUIT



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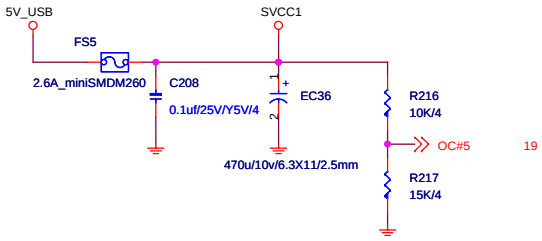
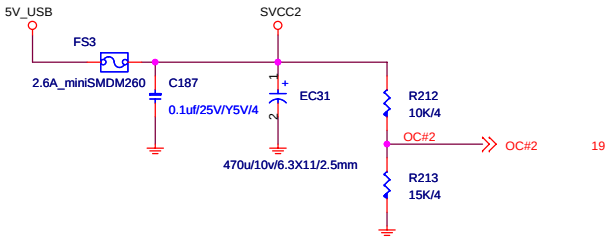
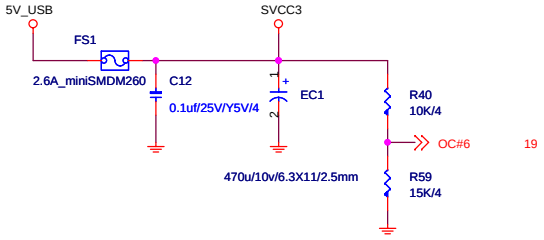
POWER CIRCUIT FOR USB PORT 10, 11



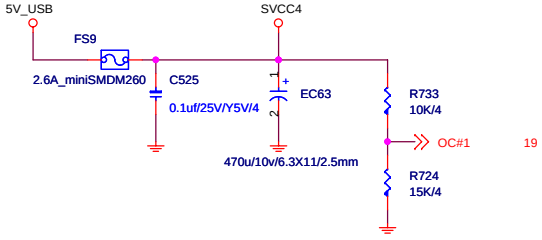
POWER CIRCUIT FOR USB PORT 4, 5



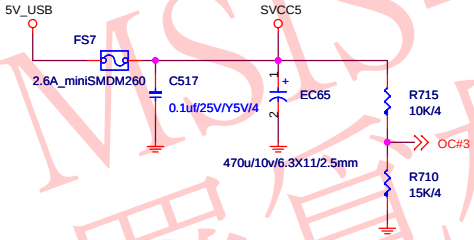
POWER CIRCUIT FOR USB PORT 12, 13



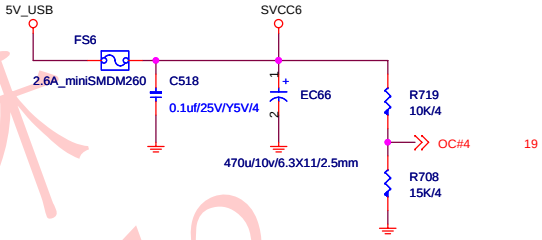
POWER CIRCUIT FOR USB PORT 2, 3



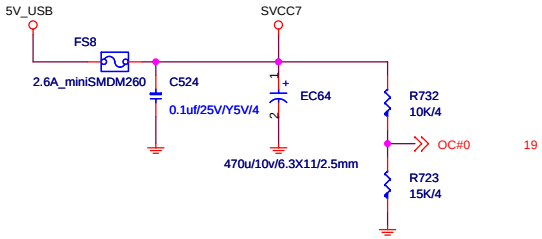
POWER CIRCUIT FOR USB PORT 6, 7



POWER CIRCUIT FOR USB PORT 8, 9



POWER CIRCUIT FOR USB PORT 0, 1



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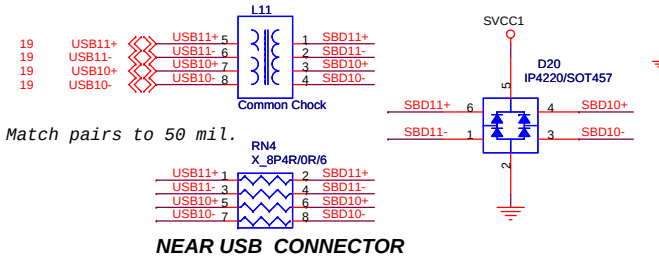
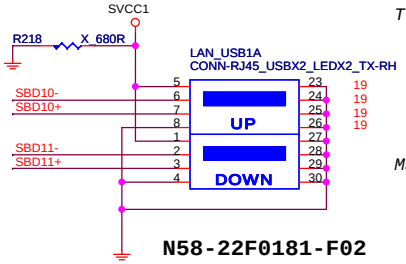
REAR PANEL USB CONNECTOR FOR USB PORT 10,11

Trace lengths must be less 12 inches



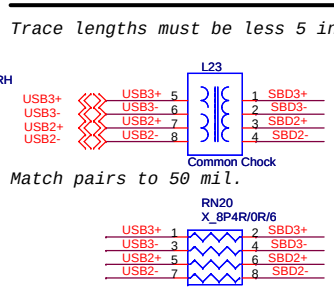
NEAR USB CONNECTOR



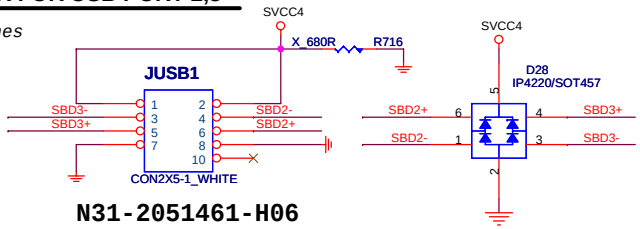
N58-22F0181-F02

FRONT PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 5 inches



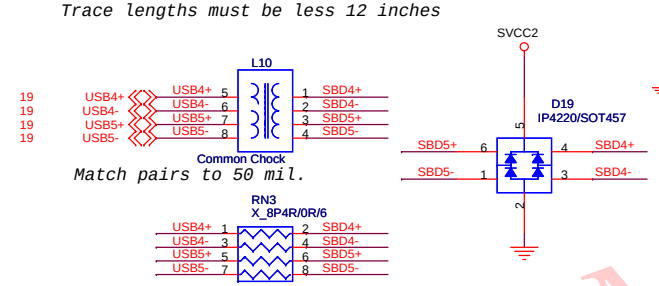
NEAR USB CONNECTOR



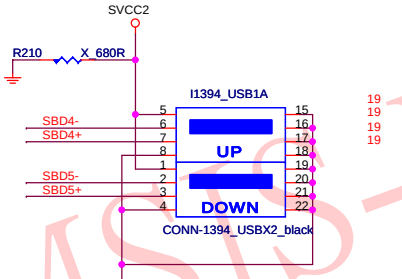
N31-2051461-H06

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



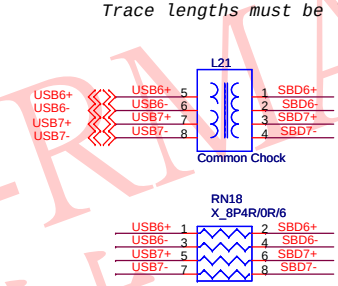
NEAR USB CONNECTOR



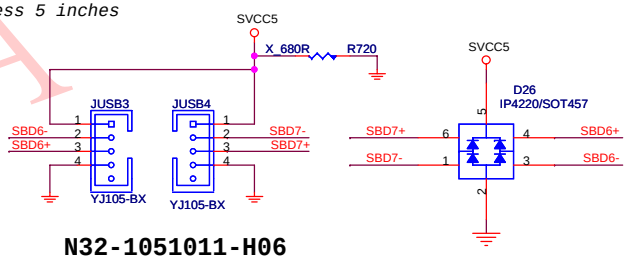
N58-14M0051-L06

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



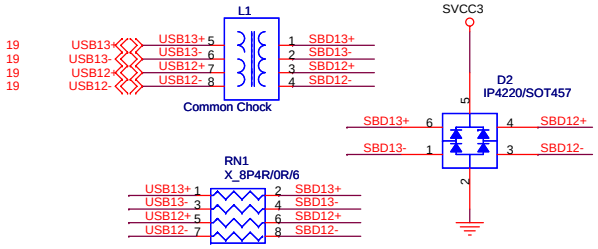
NEAR USB CONNECTOR

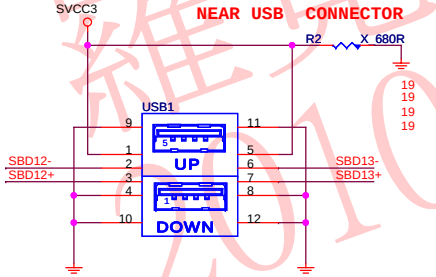


N32-1051011-H06

FRONT USB CONNECTOR FOR USB PORT 12,13

Trace lengths must be less 5 inches

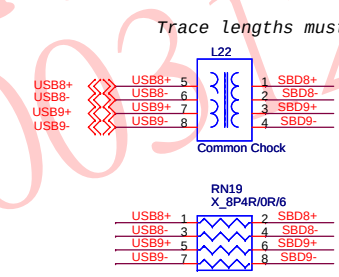




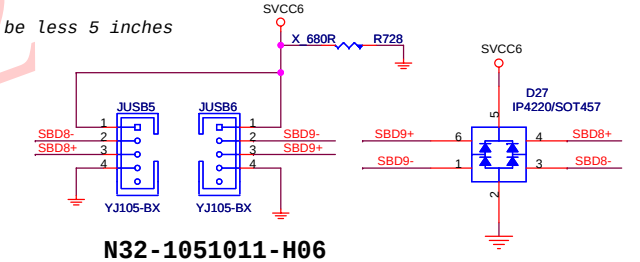
N53-08M0421-F02

FRONT PANEL USB CONNECTOR FOR USB PORT 8, 9

Trace lengths must be less 5 inches



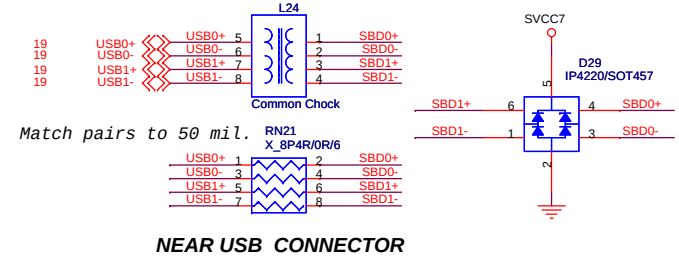
NEAR USB CONNECTOR



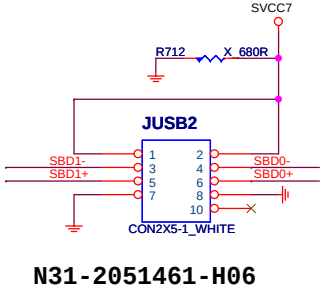
N32-1051011-H06

FRONT USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 5 inches



NEAR USB CONNECTOR



N31-2051461-H06

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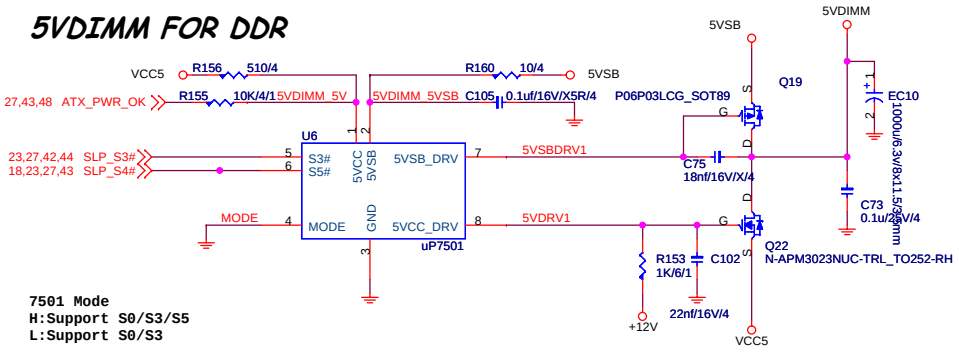

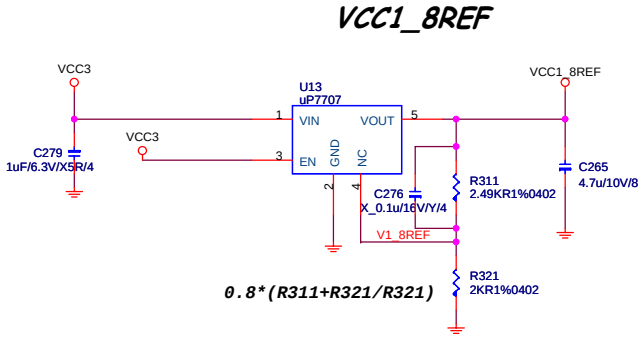

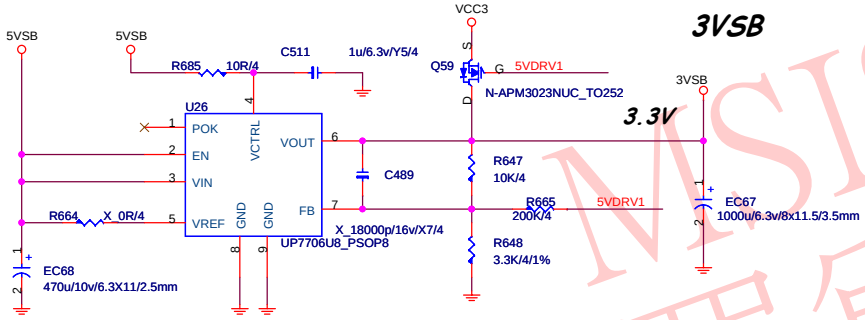

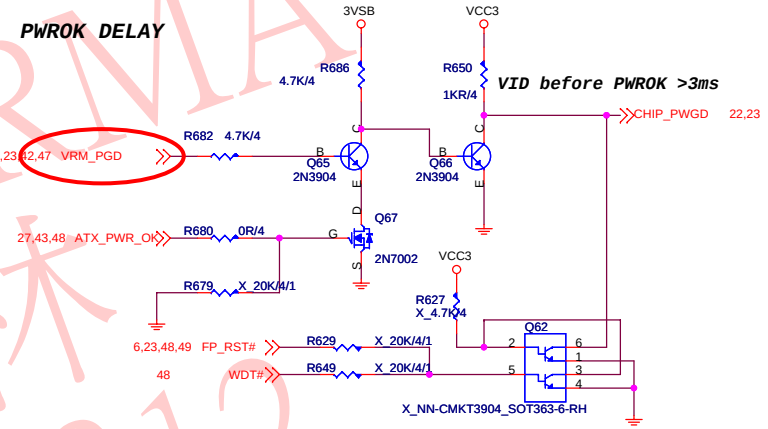

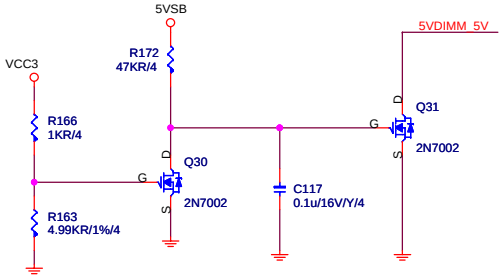

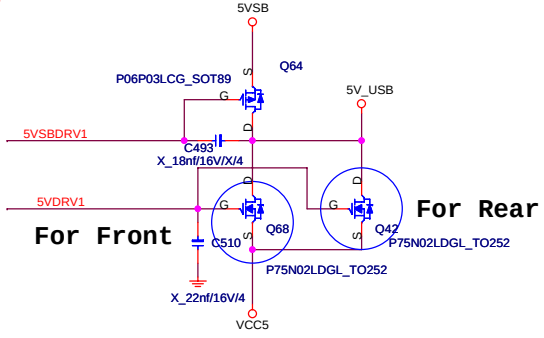

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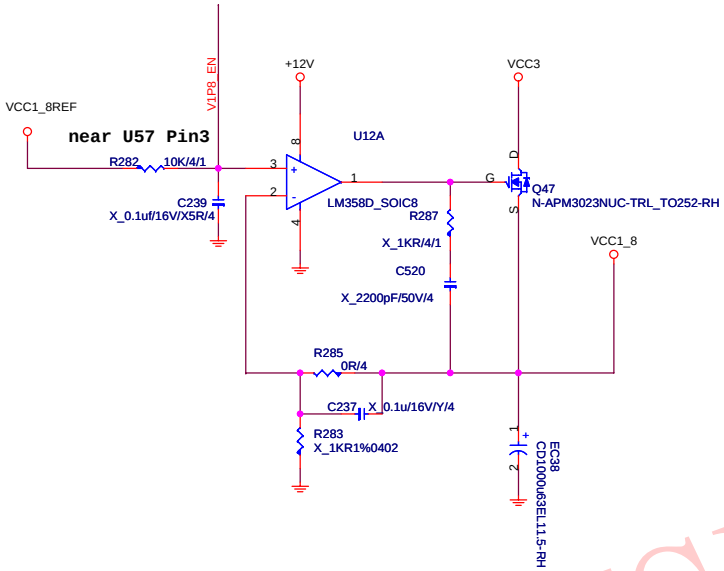
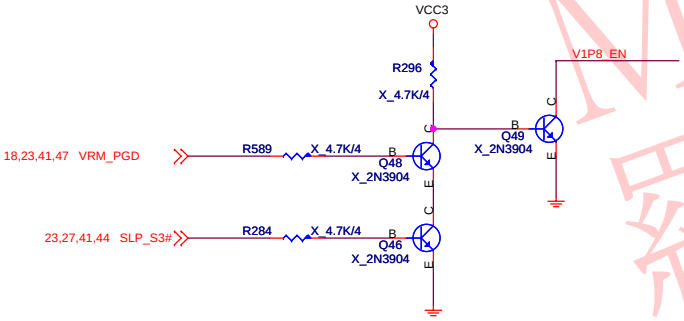
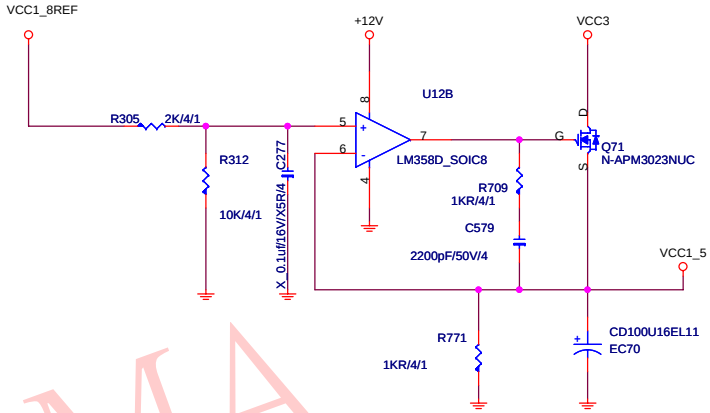
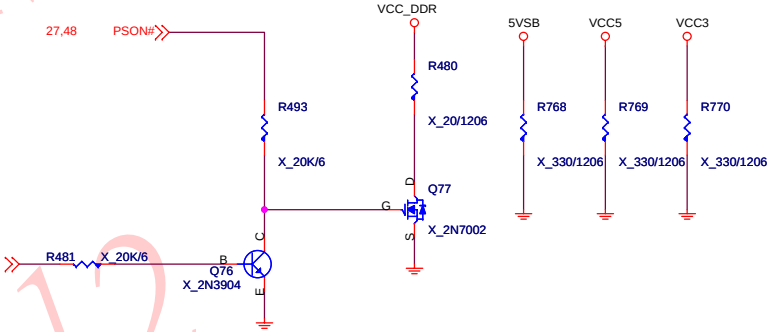


cpuvtt & pch vore wait 1.8v

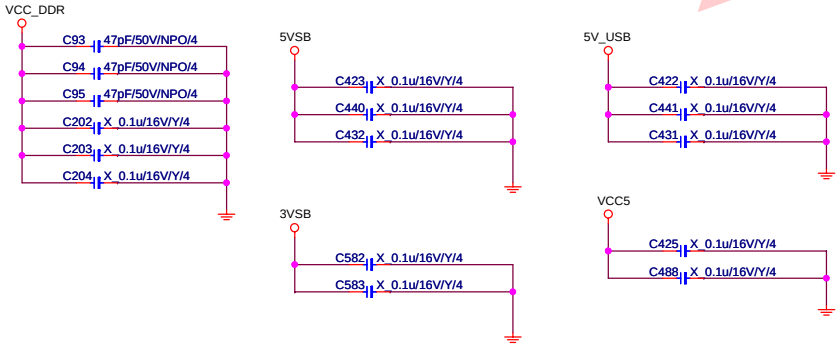


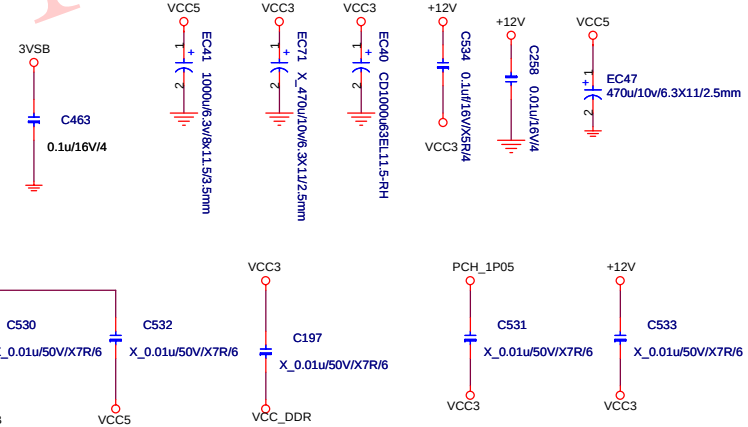


Discharge Circuit



For EMI





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Custom	ACPI Controller 2	11

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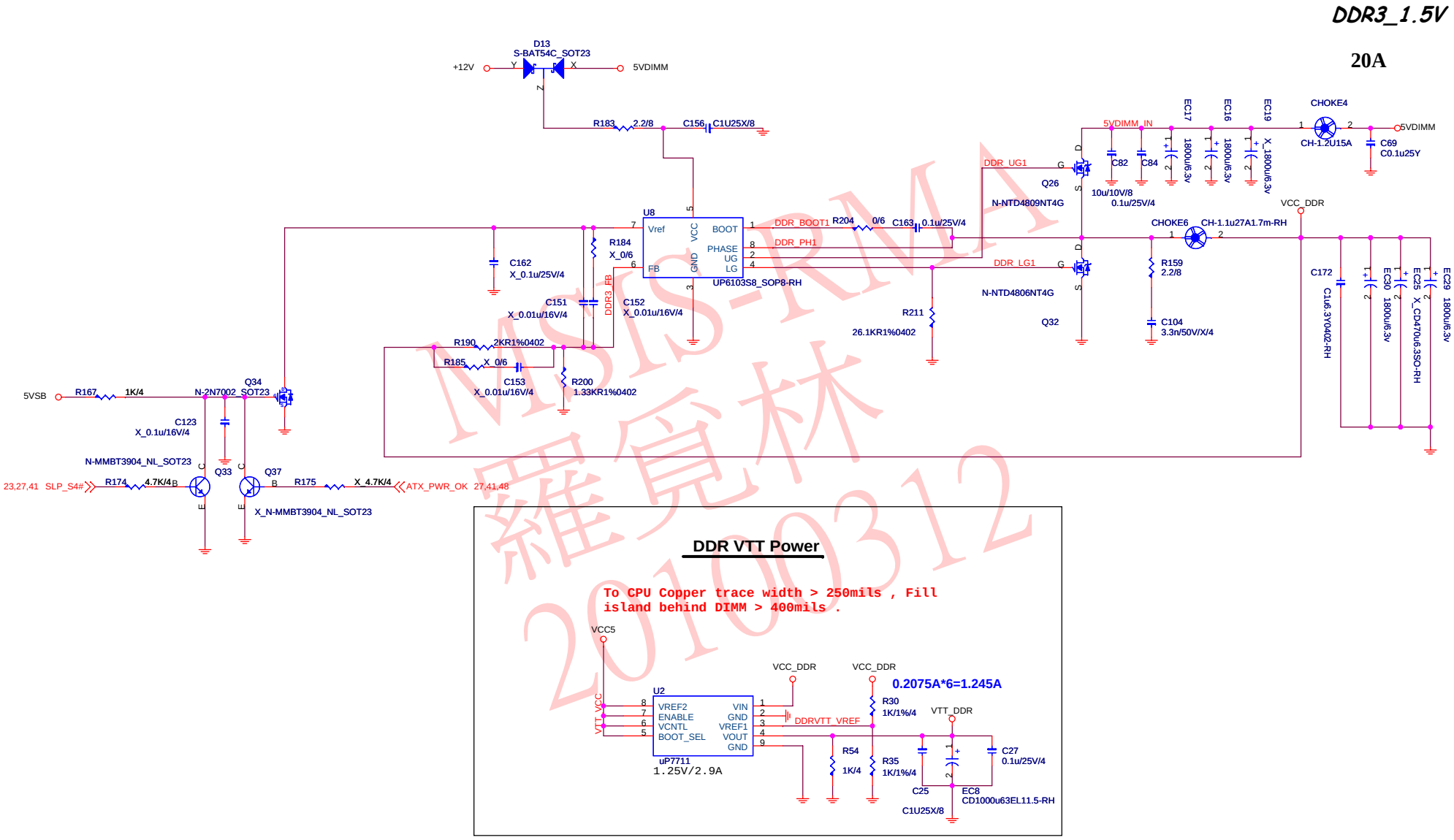

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MS-7613		
Size: Custom	Document Description: DDR POWER - UPI6103_1-Phase	Rev: 11
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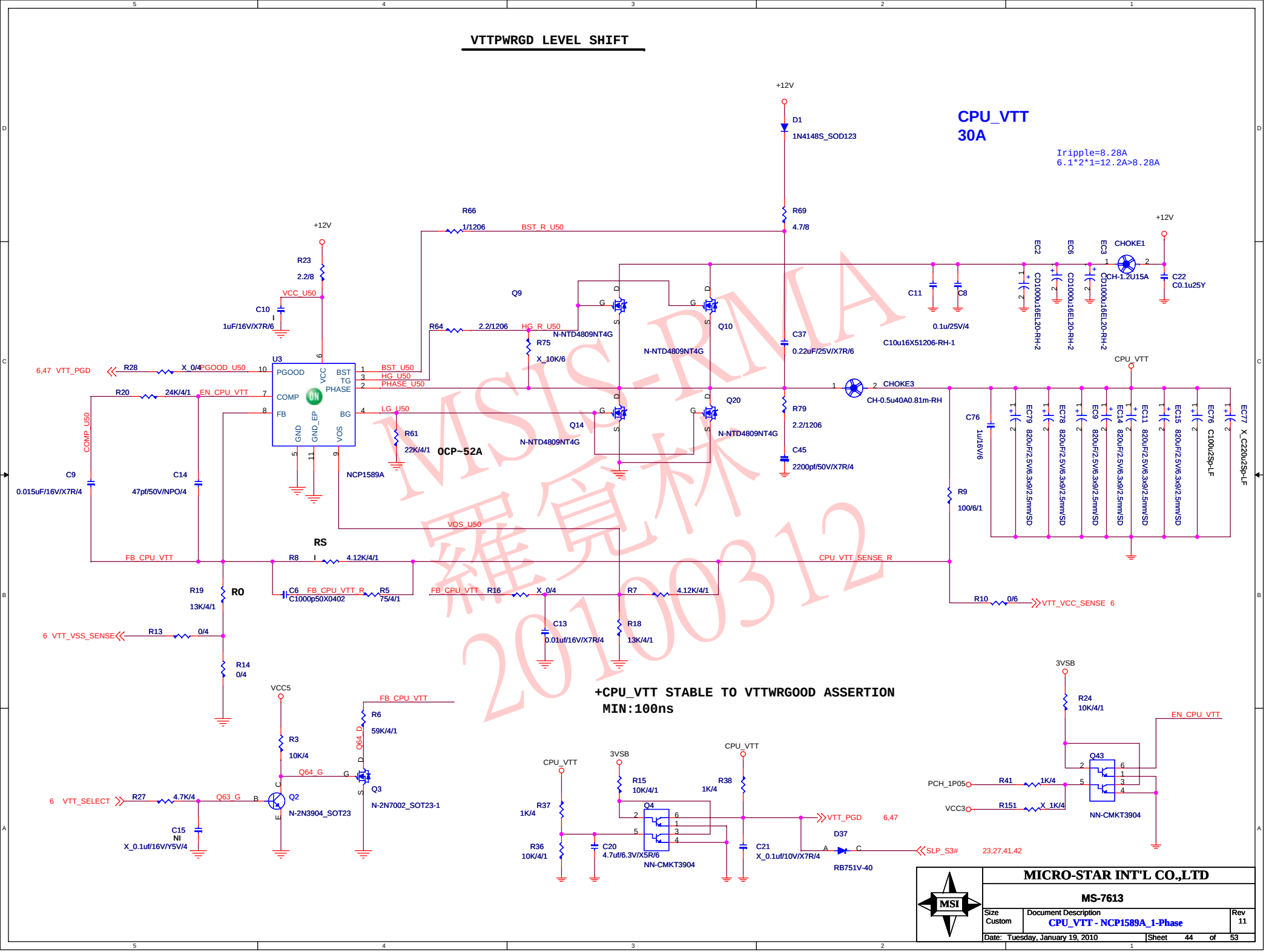
VTTPWRGD LEVEL SHIFT



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MS-7613	
Size: Custom	Document Description: CPU_VTT - NCP1589A_1-Phase
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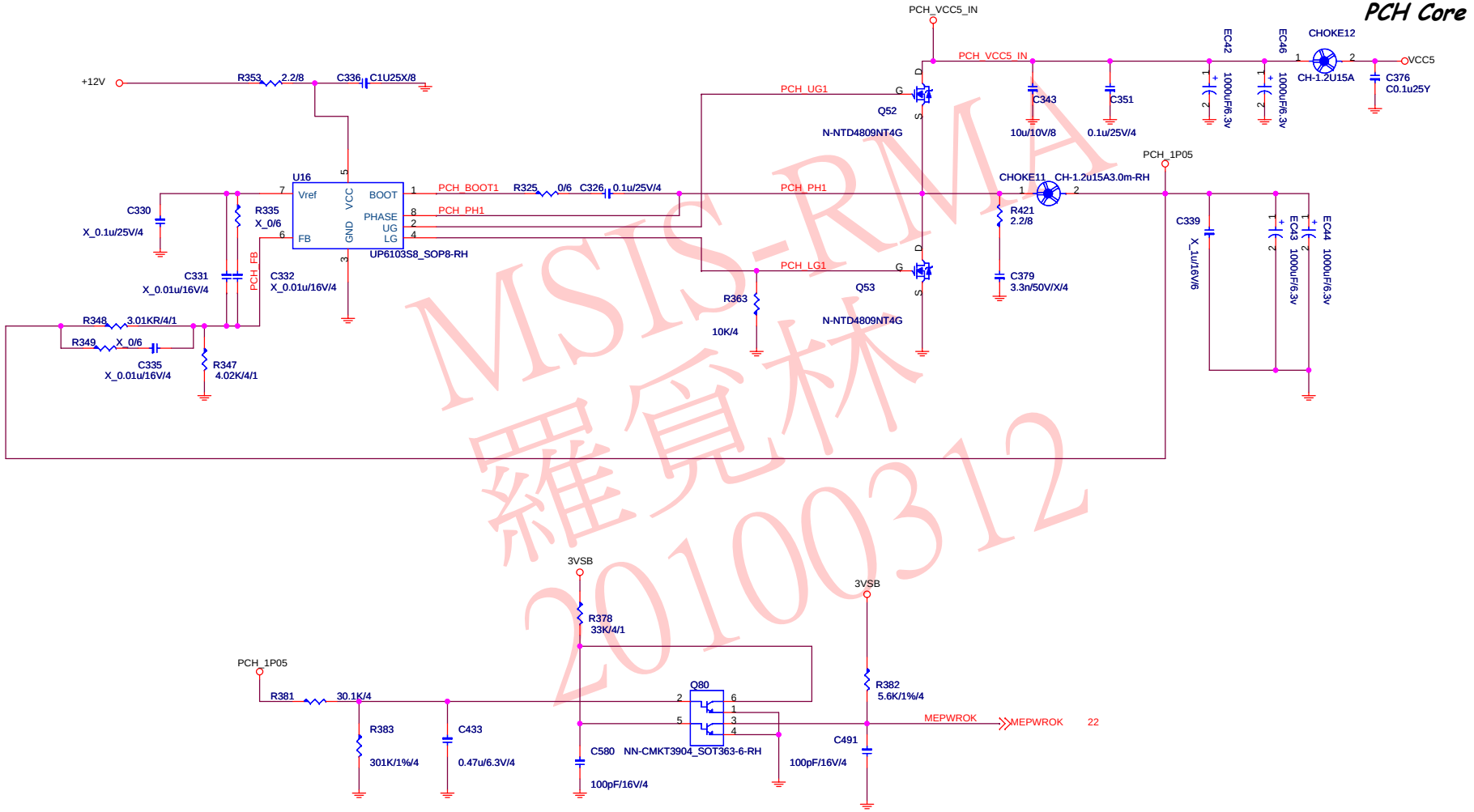
5.5A+2.5A(VCCME)=8A

PCH Core



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size: Custom	Document Description: PCH POWER - UPI6103_1-Phase	Rev: 11
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TABLE 2. VR11 VID 8 BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000

GPU_CORE 20A

20A

U10 ISL6314CRZ_QFN32-RH

6X6 QFN

BOTTOM PAD CONNECT TO GND Through 8 VIAs

Following CRB REV 1.1

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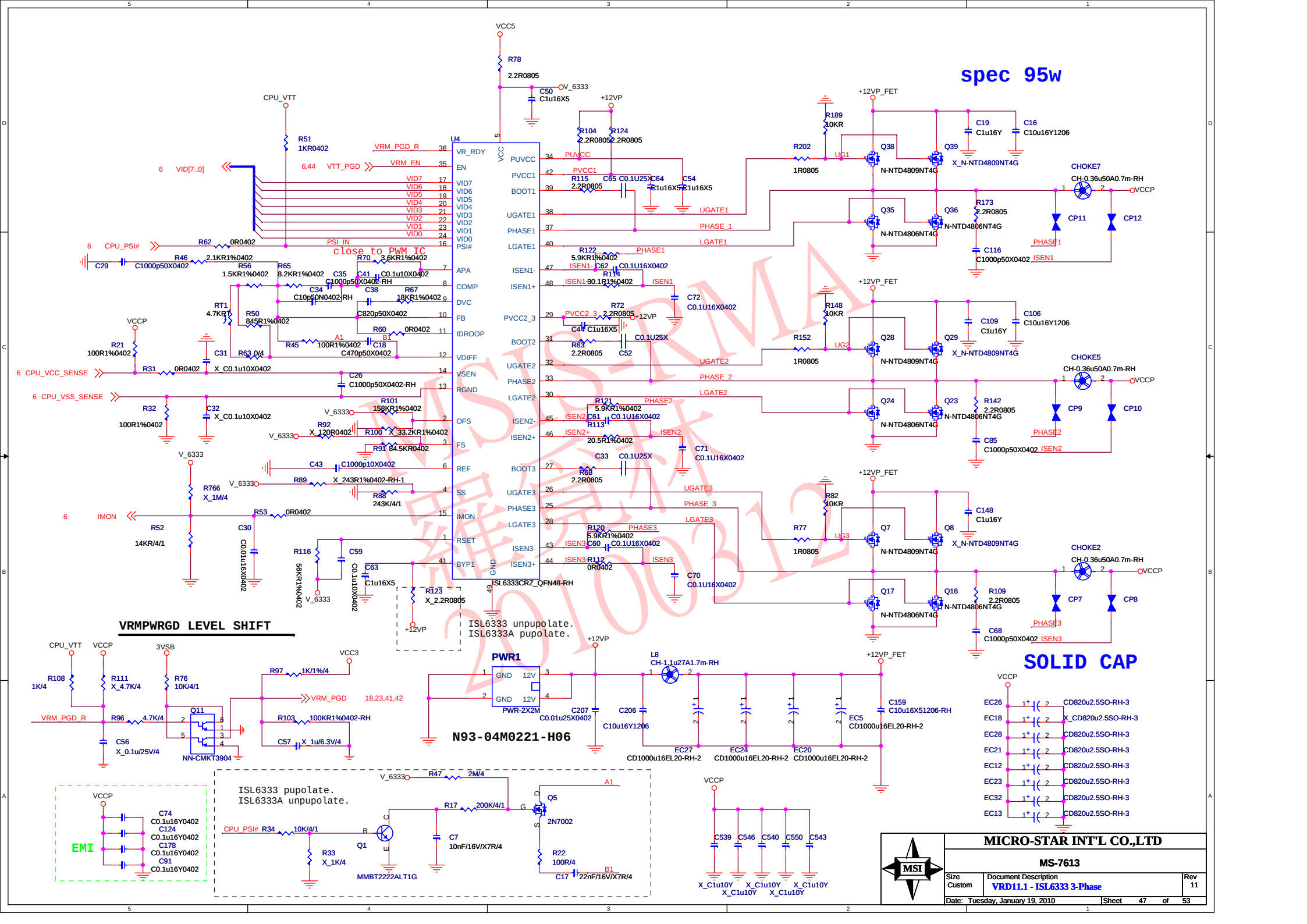
spec 95w
U4
ISL6333CRZ_QFN48-RH
close to PWM IC
VRMPWRGD LEVEL SHIFT
ISL6333 unpupolate.
ISL6333A pupolate.
ISL6333 pupolate.
ISL6333A unpupolate.
PWR1
PWR-2X2M
N93-04M0221-H06
SOLID CAP
EMI
MICRO-STAR INT'L CO.,LTD
MS-7613
VRD11.1 - ISL6333 3-Phase
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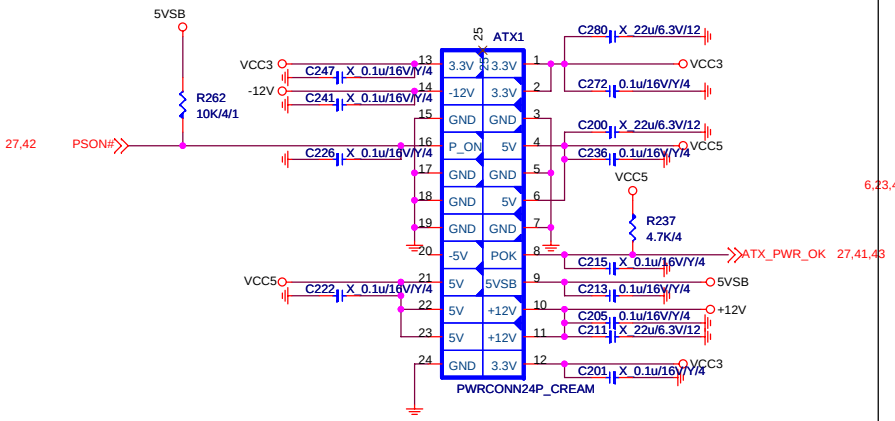
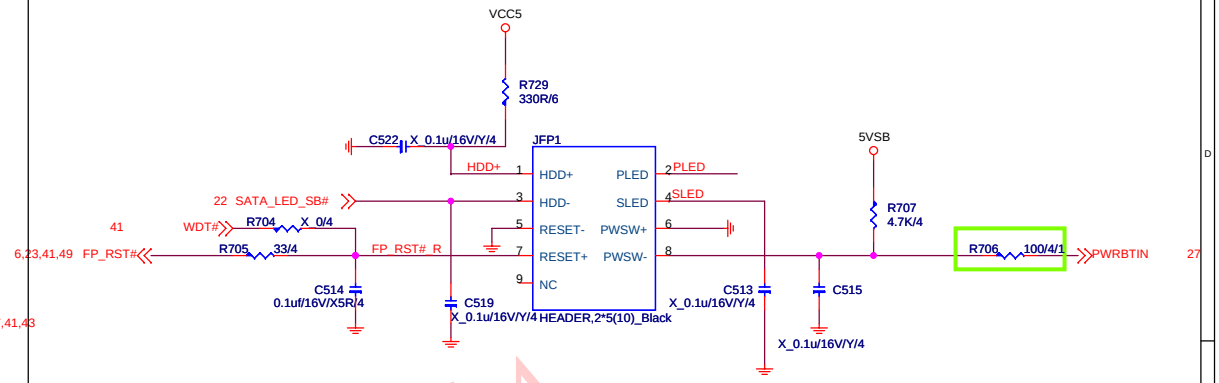
MSI-RMA
20100312

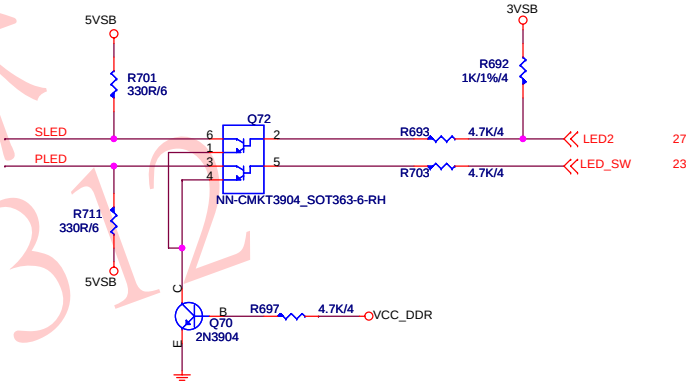
ATX POWER CONNECTOR

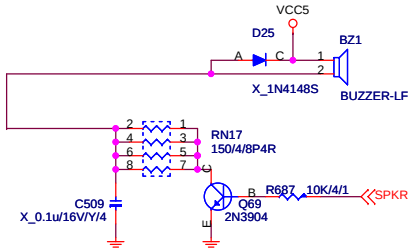


FRONT PANNEL



LED





	Single color LED		Dual color LED	
	LED2	LED_SW	LED2	LED_SW
S0	H	L	H	L
S1/S3	Blinking	L	L	H
S4/S5	L	L	L	L

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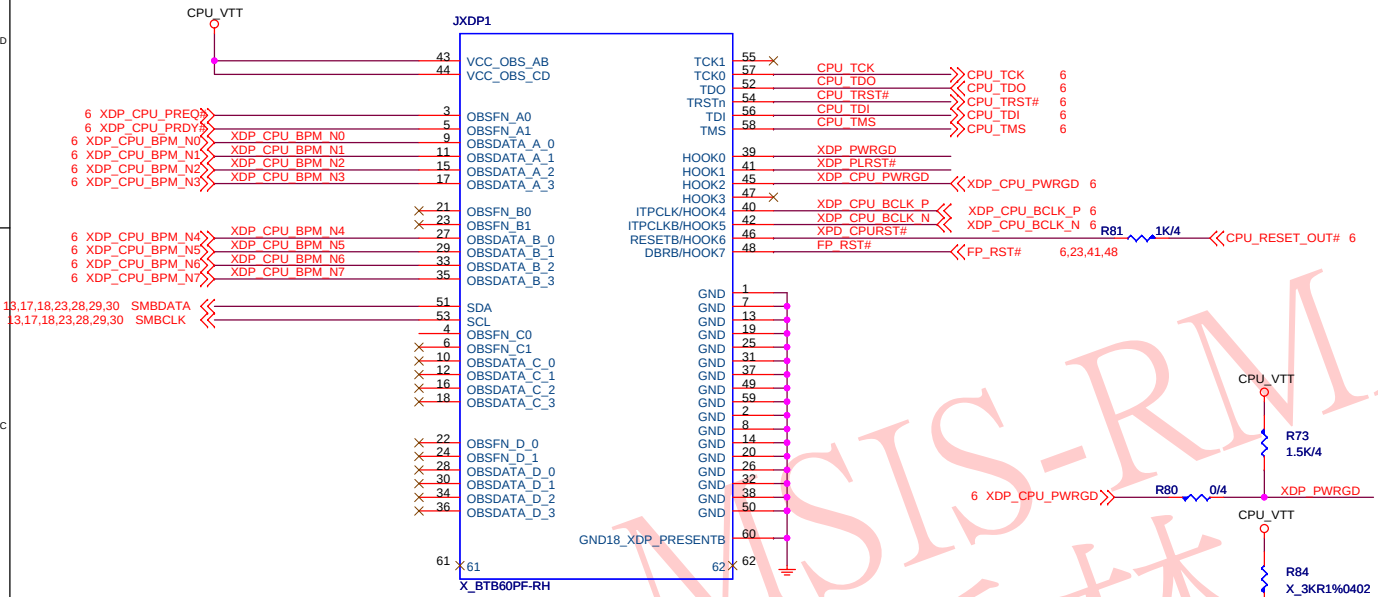
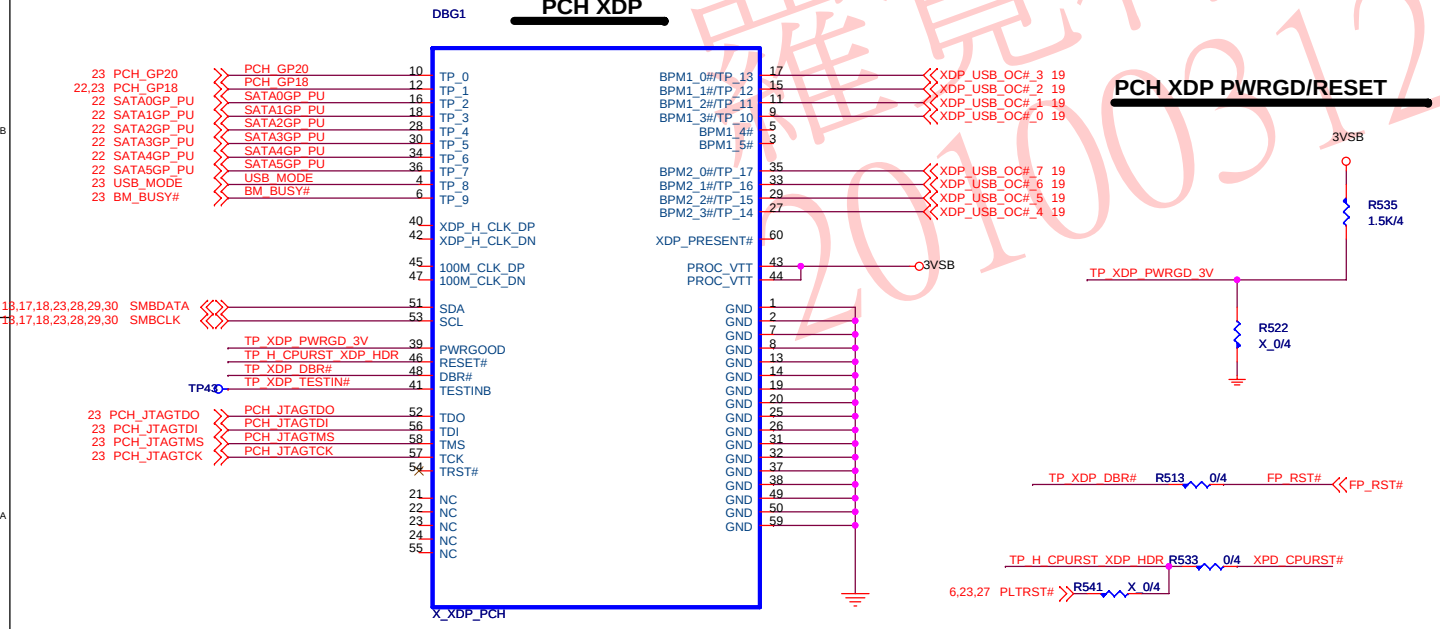
Reserve debug port



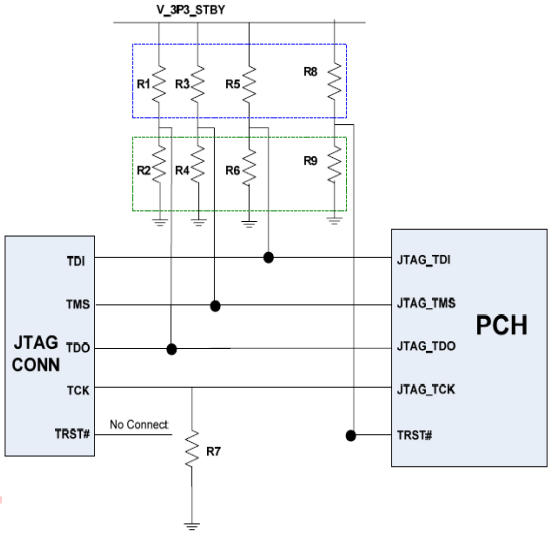
N5C-60F0040-S88

PCH XDP



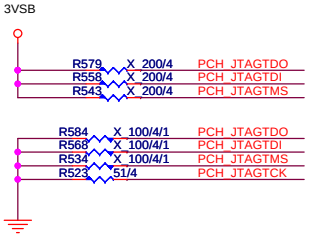
N5C-60F0040-S88

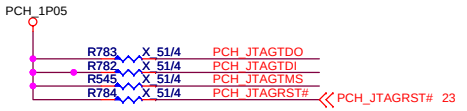
PCH XDP PWRGD/RESET



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
TDI	R5	200 Ohms	200 Ohms	No Stuff
	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable[1]	Not Applicable[1]
	R9	10K Ohms	Not Applicable[1]	Not Applicable[1]

Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes.





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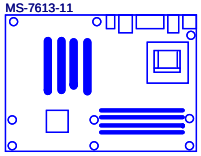
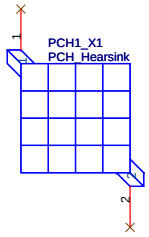
PCB

PCB1
MS-7613-11



P30-0761311-G37

PCH1_X1
PCH_Hearsink

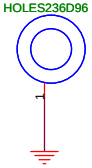


E31-0401634-K08

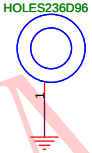
BAT1_X1

BAT-BCR2032P-RH

H1
HOLES236D96

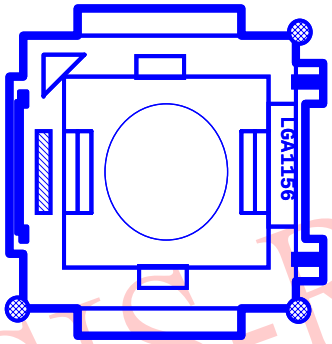


H2
HOLES236D96



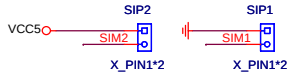
CPU SOCKET

CPU1_X1
CPU SOCKET

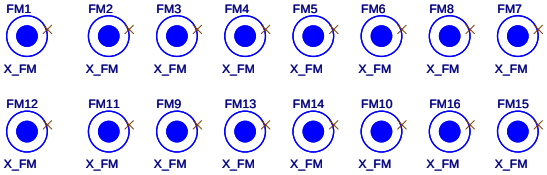


E21-7557010-F02

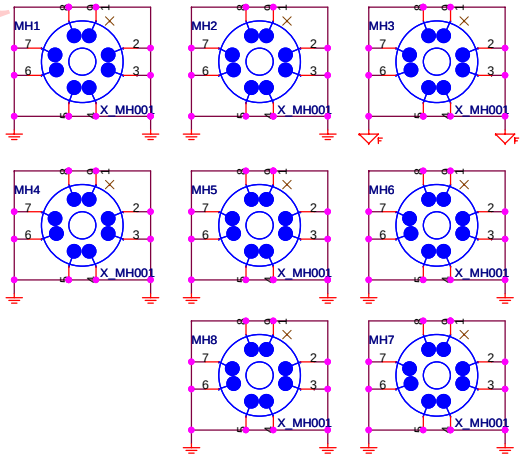
Simulation



Optical Fiducial Marks-120



Mounting Holes



MSI	MICRO-STAR INT'L CO.,LTD	
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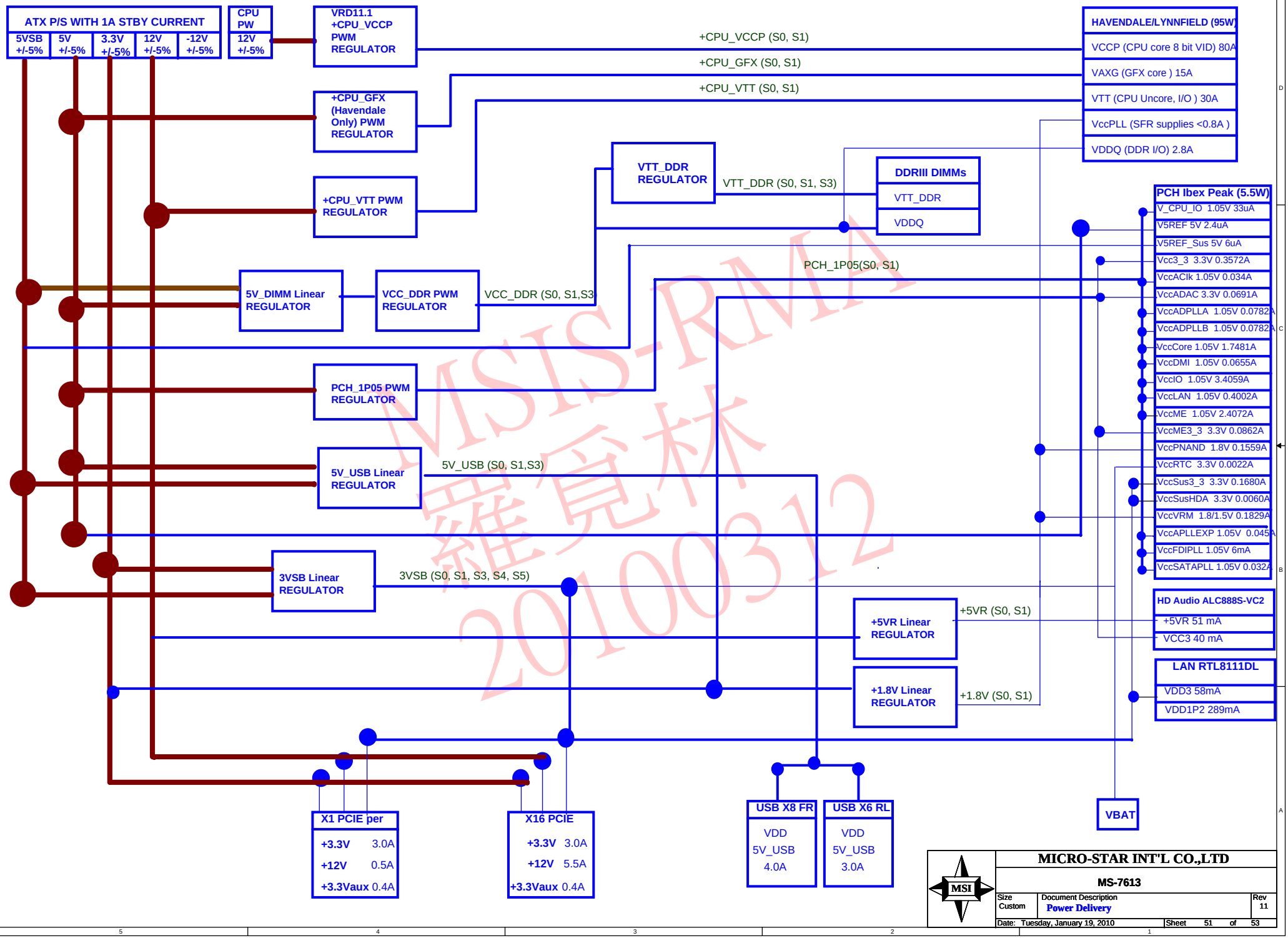

Version 0A:

2009/03/16
Page 23: Populate R668 by Intel suggestion.
Page 23: Populate 100k ohm in R668 by Intel suggestion.
Page 23: Unpopulate R214 by Intel suggestion.

Version 0B:

2009/03/17
Page 35: Add internal amplifier circuit by HP requestion.
Page 34: Remove internal line-in circuit by HP requestion.
Page 6: Add CPU POC circuit following Design guide..
Page 47: Change R123 to 2.2ohm/0805 reserve for ISL6333A.
Page 39: Change USB port 0, 1 OC from OC#5 to OC#0 following Design guide.
Page 36: Change R143 and R140 from 100 ohm to 0 ohm by Intel suggestion.
Page 23: Pull-up GPIO57 to 3VSB by Intel suggestion.
Page 23: Unpopulate R603 by Intel suggestion.
Page 23: Pull-up SML0CLK and SML0DATA to 3VSB by Intel recommend.
Page 23: Pull-up SMBCLK and SMBDATA to 3VSB by Intel recommend.
Page 23: Swap HAD_SYNC and HAD_RST to match ball name.
Page 23: Connect PCH_JTAGRST# to a test point by Intel recommend.
Page 49: Connect SATA4GP to Pin 34 of the JTAG connector by Intel recommend.
Page 49: Connect Pin 41 of the JTAG connector to a test point by Intel recommend.
Page 49: Connect VCC of the JTAG connector to 3VSB by Intel recommend.
Page 23: Connect GIOP26 to control audio de-pop circuit.
Page 23: Use GIOP13 to switch audio Verb Table with internal amplifier or not.
Page 37: Reserve R512 for DVI level shifter eable control.
2009/03/19
Page 20: Change R539 and R546 from 39 ohm to 22 ohm by Intel recommend.
Page 27: Reserve R766 for RSMRST# timing control.
Page 23: Change GPIO45, GPIO46, GPIO47 pull-up well from VCC3 to 3VBS following schematic checklist.
Page 22: Connect SATA port4 to SATA5 connector by HP recommend.
Page 22: Connect SATA port2 to SATA3 connector by HP recommend.
Page 22: Use GPIO22, GPIO38, GPIO39, GPIO48 for MB_ID.
Page 32: Unpopulate C216 for EEPROM can not be programed issue.
2009/03/20
Page 42: Reserve discharge circuit.
Page 47: Connect IMON pin of VRD to ISENSE of CPU.
2009/03/23
Page 32: Unpopulate C209, C210, C214 to fix LAN LED wrong.
Page 42: Add R771 approve VCC1_5 whithout load.
2009/03/24
Page 22: Delete SATA5, SATA6 connector.
Page 22: Change SATA1 and SATA2 to right angle connector.
Page 15: Change C160 to 22uF/0805 and add a 22uF/0805 in C470.

2009/03/25
Page 23: Change R595 from 10k ohm to 1k ohm.
Page 23: Reserve R561 to pull-up FP_RST# to 3VSB.
Page 30: Add R813 and R814 to switch Mini-card support wake function or not.
Page 41: Change R650 from 4.7k ohm to 1k ohm for approving CHIP_PWGD signal level.
2009/03/26
Page 34: Move D24 to pin2 of U27.
Page 34: Change R681 from 309 ohm to 324 ohm.
Page 34: Connect D32 to 3VSB.
Page 30: Add Wireless LED (JWLED) by HP requirement.
2009/03/27
Power solution:
Page 47: Change R50 from 681 ohm to 931 ohm.
Page 47: Change R56 from 1.24k ohm to 1.33k ohm.
Page 47: Change R101 from 162k ohm to 255k ohm.
Page 47: Change C34 from 33 pF to 10 pF.
Page 47: Change C35 from 470 pF to 1000 pF.
Page 47: Change R65 from 16.5k ohm to 21k ohm.
Page 47: Change R70 from 5.1k ohm to 3k ohm.
Page 12: Populate C96 and C98.
Page 47: Populate 4700pF cap in C29 and 2.49k ohm resistor in R46.
Page 47: Change R52 from 13.3k ohm to 14.3k ohm.
Page 47: Change CHOKE2, CHOKE5 and CHOKE from 0.5uH to 0.36uH
Page 47: Populate EC32.
Page 47: Change R120, 121 and R122 from 6.19k ohm to 5.11k ohm.
Page 44: Change C6 from 0.015uF to 4700pF.
Page 44: Change R8 from 4.32k ohm to 4.12k ohm.
Page 44: Populate 820uF cap in EC78.
Page 44: Change EC76 from 100uF to 220uF and non-stuff EC77.
Page 44: Add a 820uF cap in EC79.

2009/03/30
Page 23: Change R642 from 4.75k ohm to 1.1k ohm.
and R641 from 12.1k ohm to 3k ohm following Intel MOW WW13 2009.
Page 27: Change R571 from 5.6k ohm to 5.9k ohm to meet RSMRST# falling spec.
and unpopulate C456 to meet RSMRST# falling spec.
2009/03/31
Page 20: Reserve C471, C479 and C483 for EMI.
2009/04/02
Page 26: Un-stuff R431 and R400.
Stuff R423, R401, R367, R475, R371 and R450 for using external LC filter.
Page 38: Connect Pin 1 of U1 to fix system fan always full on.
Page 48:Use GPIO31 to control power LED for LED turn red then green with dual color LED.
2009/04/06
Page 33: Reserve C485 for AZ_SDOUT.
2009/04/07
Page 34: Reserve Q78, Q79, R773, C475, R702, R773 for power saving in S5.
Page 43: Change R200 from 1.3k ohm to 1.33k ohm for DDR power quality.
Page 27: Add D36 and connect to ATX_PWR_OK for AC power lost last state function adnormal.
2009/04/09
Page 18: Change Clock gen from realtek RTM875N-606 to realtek RTM885N-932.
Page 44: Add D37 to fix CPU_VTT leakage in S3 state.

Version 0C:

2009/04/21
Page 23: Add C365 to fix sometime the system auto wake when insert PCIE device.
Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.
Page 23: Use GPIO44 to control onboard LAN power.
2009/04/27
Page 28: Reserve C412 for PCIE slot power.
Page 34: Reserve C419 for audio power.

Version 0C:

2009/04/21

Page 23: Reserve C365 to fix sometime the system auto wake when insert PCIE device.

Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.

Page 23: Use GPIO44 to control onboard LAN power.

2009/04/27

Page 28: Add C412 for PCIE slot power.

Page 34: Reserve C419 for audio power.

2009/05/06

Page 40: Leave pin10 of JUSB1 and JUSB2 NC for some card reader work abnormal.

Page 41: Change EC67 to 1000uF for 3VSB power quality.

Page 37: Swap DVI_TXD2+ and DVI_TXD2-.

2009/05/07

Power Solution:

Page 12: Unpopulate C146, C139, C181

Page 12: Unpopulate C142, C155, C168, C171, C179, C176, C167, C145

Page 44: Change EC76 from 220uF to 100uF.

Page 44: Change C6 from 4700pF to 1000pF.

Page 47: Change R101 from 255k ohm to 158k ohm.

Page 47: Change C18 from 680 pF to 470pF.

Page 47: Change R70 from 3k ohm to 2.74k ohm.

Page 47: Change R120, R121 and R122 from 5.1k ohm to 5.9k ohm.

Page 47: Change C29 from 4700 pF to 1000pF.

Page 47: Change R46 from 2.49k ohm to 2.1k ohm.

Page 47: Change R45 from 750 ohm to 100 ohm.

Page 47: Change R65 from 2.1k ohm to 8.2k ohm.

Page 47: Change C35 from 1000 pF to 3300pF.

Page 47: Change R52 from 14.3k ohm to 14k ohm.

Page 47: Change R56 from 1.33k ohm to 1.4k ohm.

Page 46: Change R290 from 9.1k ohm to 15.4k ohm.

Page 46: Change R309 from 19.6k ohm to 23.7k ohm.

Page 46: Change R286 from 100k ohm to 82k ohm.

2009/05/11

Page 18: Change clock gen from RTM885N-932 to Seligo SLG8SP585

Page 27: Change R571 from 5.9K ohm to 5.6K ohm for meet RSMRST# falling time.

Page 12: Populate 0 ohm in C186 following WW16 MoW
(Discrete graphic only support, VAXG tie to GND)

Page 11: Populate R293, R299 following WW18 MoW

Page 30: Connect LED_WLED to pin4 of JWLED for meet LED cable define.

Page 22: Change SATA1 and SATA2 connector type to DIP.

2009/05/18

Page 23: Change C495 and C500 from 10pF to 18pF.

Page 13, 15: Change C137 and C161 from 0.1uF to 2.2uF to improve Vref_CA power.

Page 30: Reserve R780 for mini card.

Page 30: Connect R813 to 3VSB_SLOT.

Page 21: Add R375 and R376 for support two TL-399.

2009/05/26

Page 23: Populate R619 to fix TV tuner card can't be detected when system restart.

2009/06/16

Power Solution:

Page 46: Un-stuff R33.

Page 46: Change R50 from 931 ohm to 845 ohm.

Page 46: Change R56 from 1.4K ohm to 1.5K ohm.

Page 46: Change R70 from 2.74K ohm to 3.6K ohm.

Page 46: Change C35 from 3300 pF to 1000 pF.

Page 46: Stuff 1000 pF in C26.

Page 44: Change R6 from 69.8K ohm to 59K ohm.

2009/06/22

Page 24: Un-stuff C560

Page 24: Change C557 to 0 ohm.

2009/06/25

Page 39: Change R216,R212,R40,R733,R715,R719,R732 from 220 ohm to 10K ohm.

Page 39: Change R217,R213,R59,R723,R710,R708,R723 from 330 ohm to 15K ohm.

Version 0D:

2009/06/22

Page 45: Add MEPWRGD circuit.

2009/06/25

Page 23: Add JME1 header.

2009/06/26

Page 37: Reserve C581 for EMI.

2009/06/30

Page 20: Add R393 and R395.

2009/07/02

Page 42: Reserver C582 and C583 for EMI.

Page 49: Reserve R545,R782,R783 and R784.

2009/07/09

Page 49: Un-stuff R579,R558,R543,R584,R568,R534.

2009/07/14

Power Solution:

Page 44: Un-stuff R16.

Page 44: Stuff 4.12k ohm in R7.

Page 44: Stuff 13k ohm in R18.

Page 44: Stuff 0.01uF in C13.

Page 46: Change C244 from 10nf to 1nf.

Page 46: Un-stuff R290.

Page 46: Change R301 from 15k ohm to 9.1k ohm

2009/07/21

Page 32: stuff 1000pf cap in C209,C210,C214,C216,C244 for EMI.

Page 42: stuff 47pf cap in C93,C94,C95 for EMI.

2009/07/29

Page 22: Change MB ID to 1010.

Page 27: Change R565 from 4.7K to 10K ohm.

Version 10:

2009/10/05

Page 30: Un-stuff ONFI slot.

Page 37: Un-stuff R171 to change DVI Vswing to 600mV.

Page 46: Stuff 22K ohm in R171 for power solution.

Page 20: Change PCH PN to B01-BD82H45-IX6

Version 11:

2010/01/11

Page 30: Connect Pin 5 of RN10 to VCC3 for PCI_E2 slot download files slowly from PXE server with LAN card.

Page 37: Connect DVI connector power pin to DVI_PWR_5V for safety.