PG411 A01

GP104 - 8GB GDDR5, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

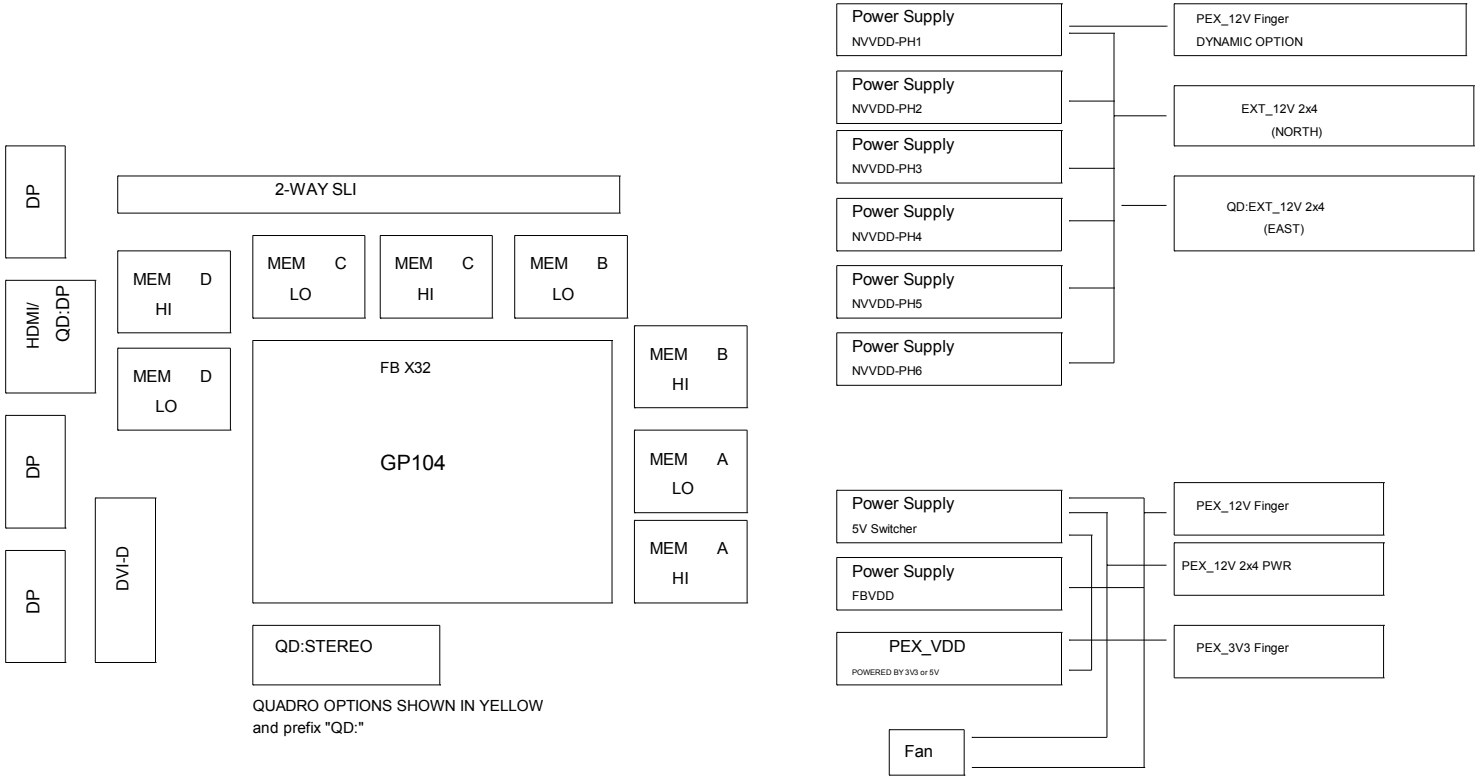
TABLE OF CONTENTS

ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
Table of Contents

GIGABYTE

Title: Table of Contents		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 1 of 42	

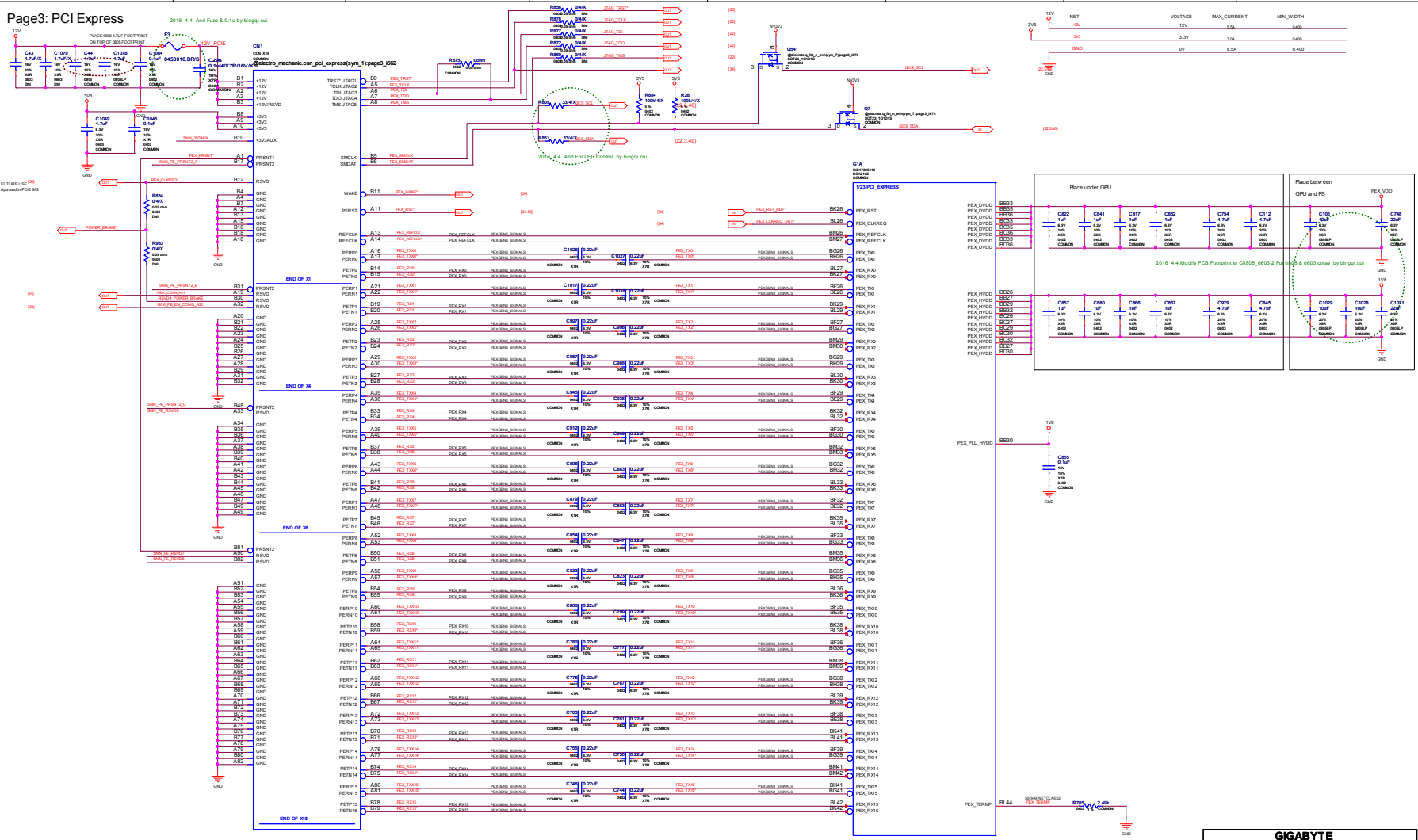


ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
Block Diagram

GIGABYTE		
Title: Block Diagram		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 2 of 42	

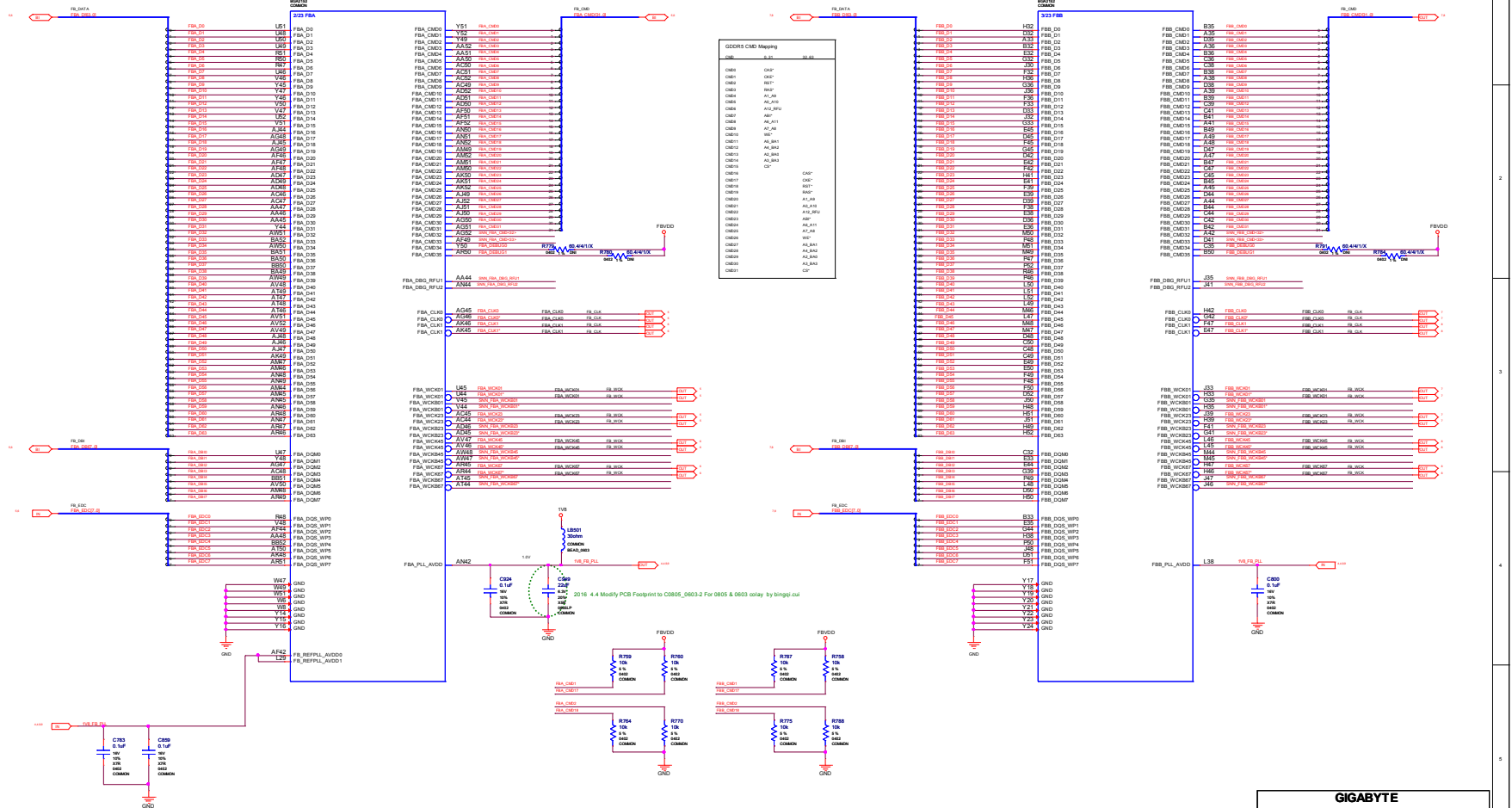
Page3: PCI Express



ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
PCI Express

Page4: MEMORY: GPU Partition A/B



ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
MEMORY: GPU Partition A/B

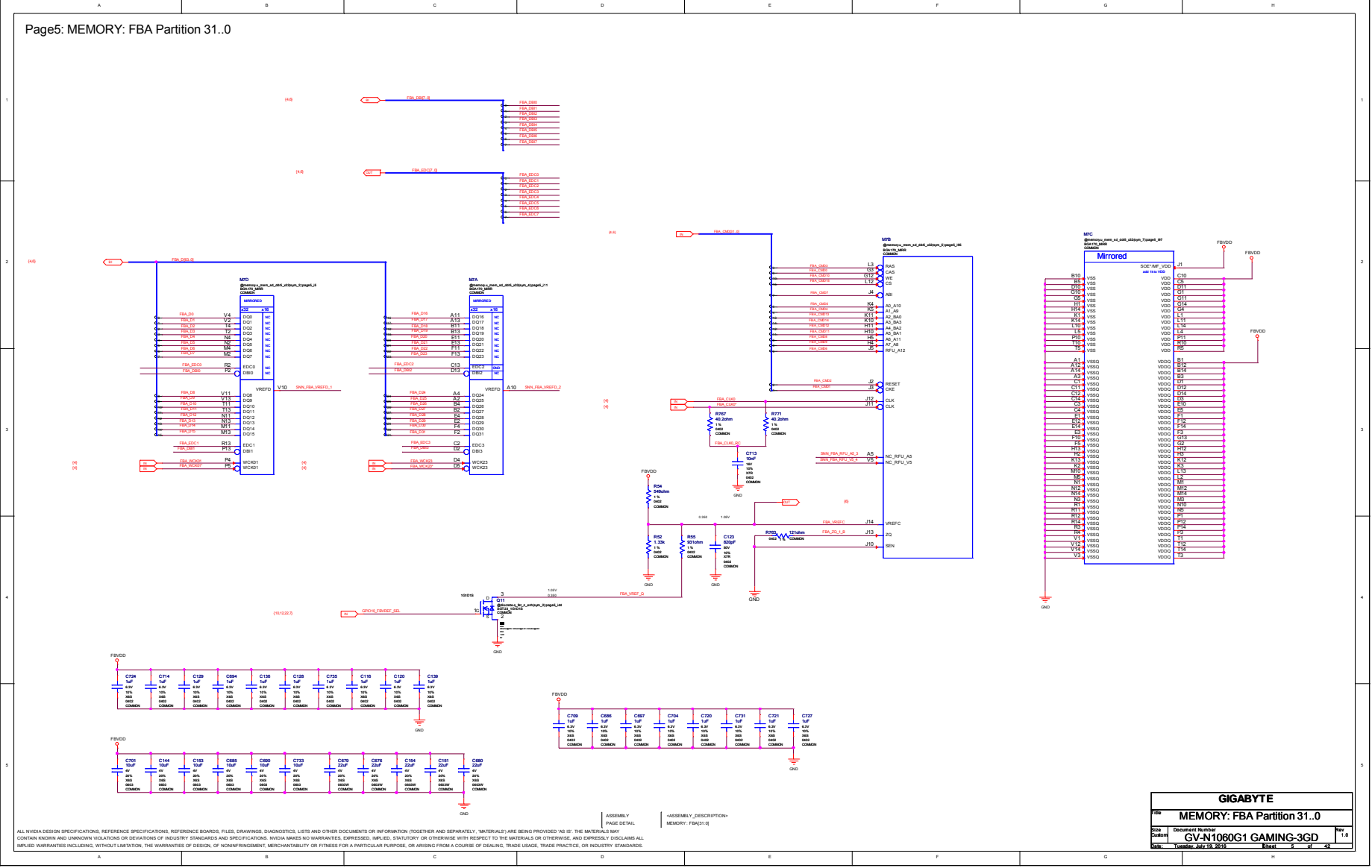
GIGABYTE

Title: GPU Partition A/B

Size: Custom | Document Number: GV-N1060G1 GAMING-3GD | Rev: 1.0

Date: Tuesday, July 19, 2016 | Sheet 4 of 42

Page5: MEMORY: FBA Partition 31..0



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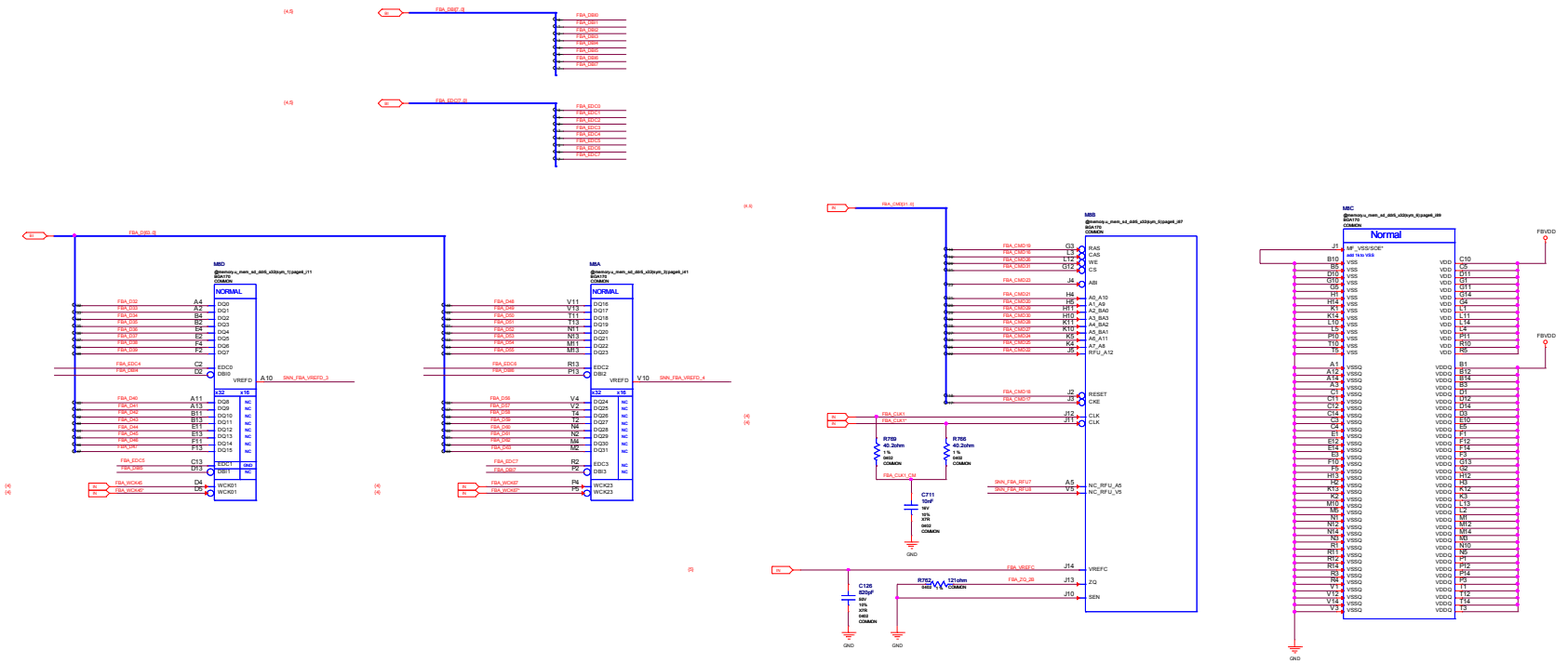
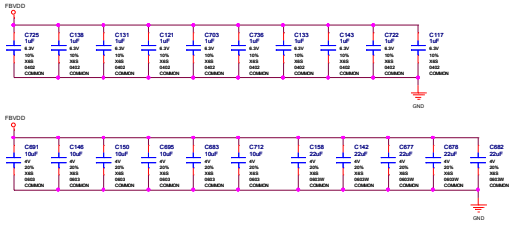
ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MEMORY: FBA[31:0]

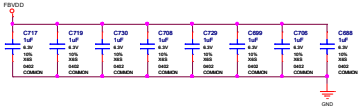
GIGABYTE

Title	MEMORY: FBA Partition 31..0	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 5 of 42	

Page6: MEMORY: FBA Partition 63..32

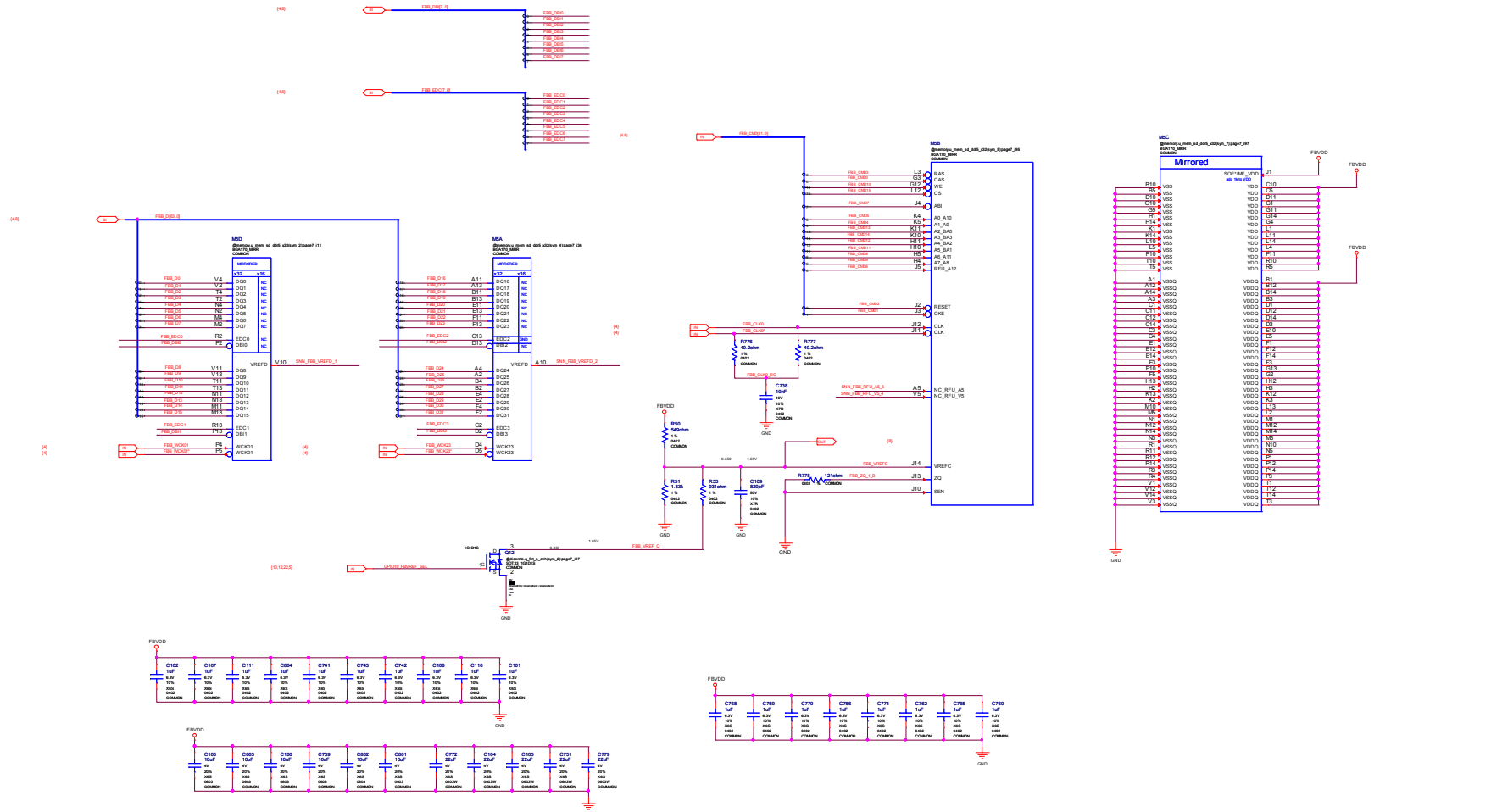






ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	MEMORY: FBA[63:32]

GIGABYTE		
Title: MEMORY: FBA Partition 63..32		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 6 of 42	



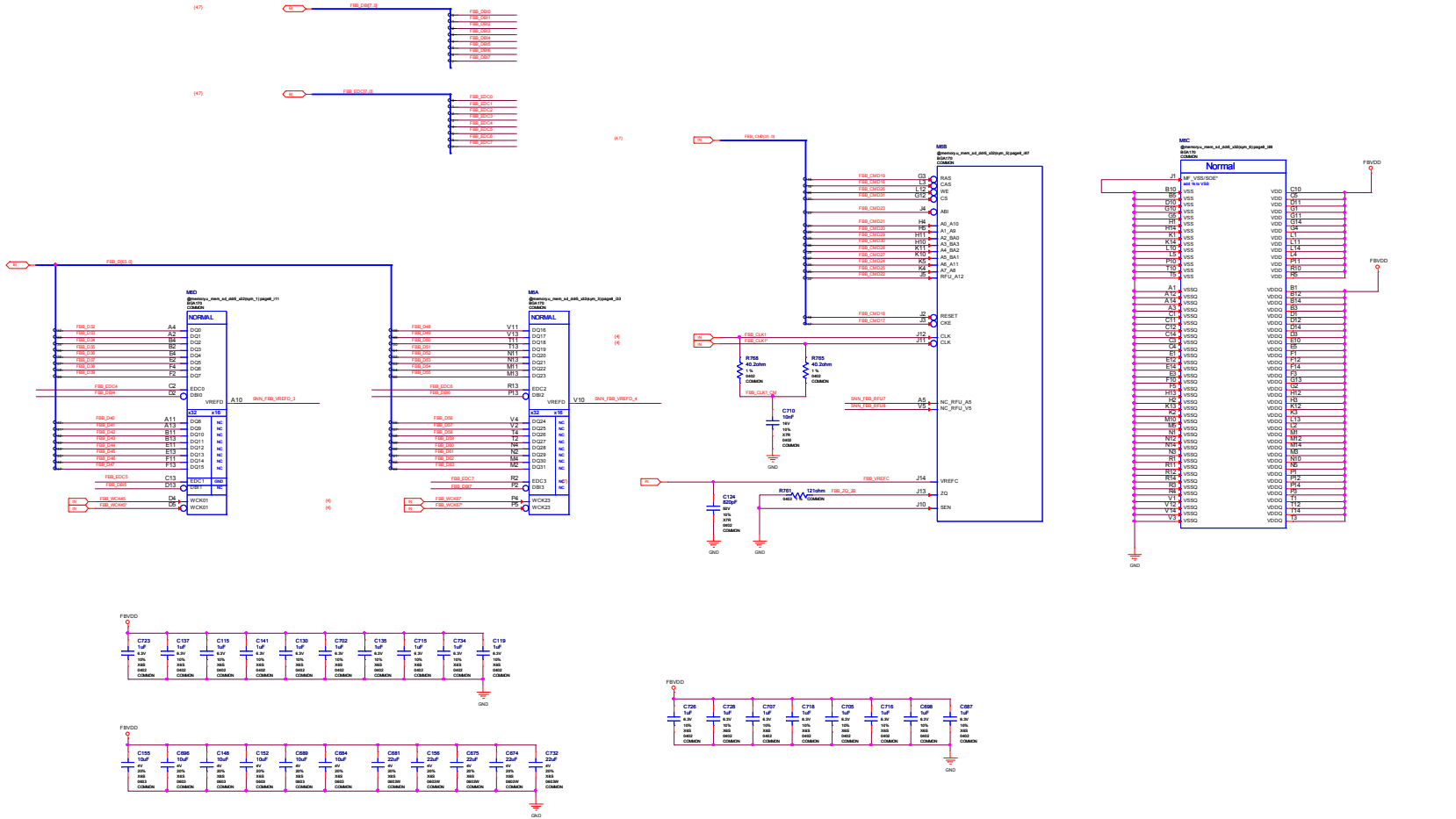
ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
MEMORY: FBB[31:0]

Title	MEMORY: FBB Partition 31..0
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD
Rev	1.0
Date: Tuesday, July 19, 2016	Sheet 7 of 42

GIGABYTE

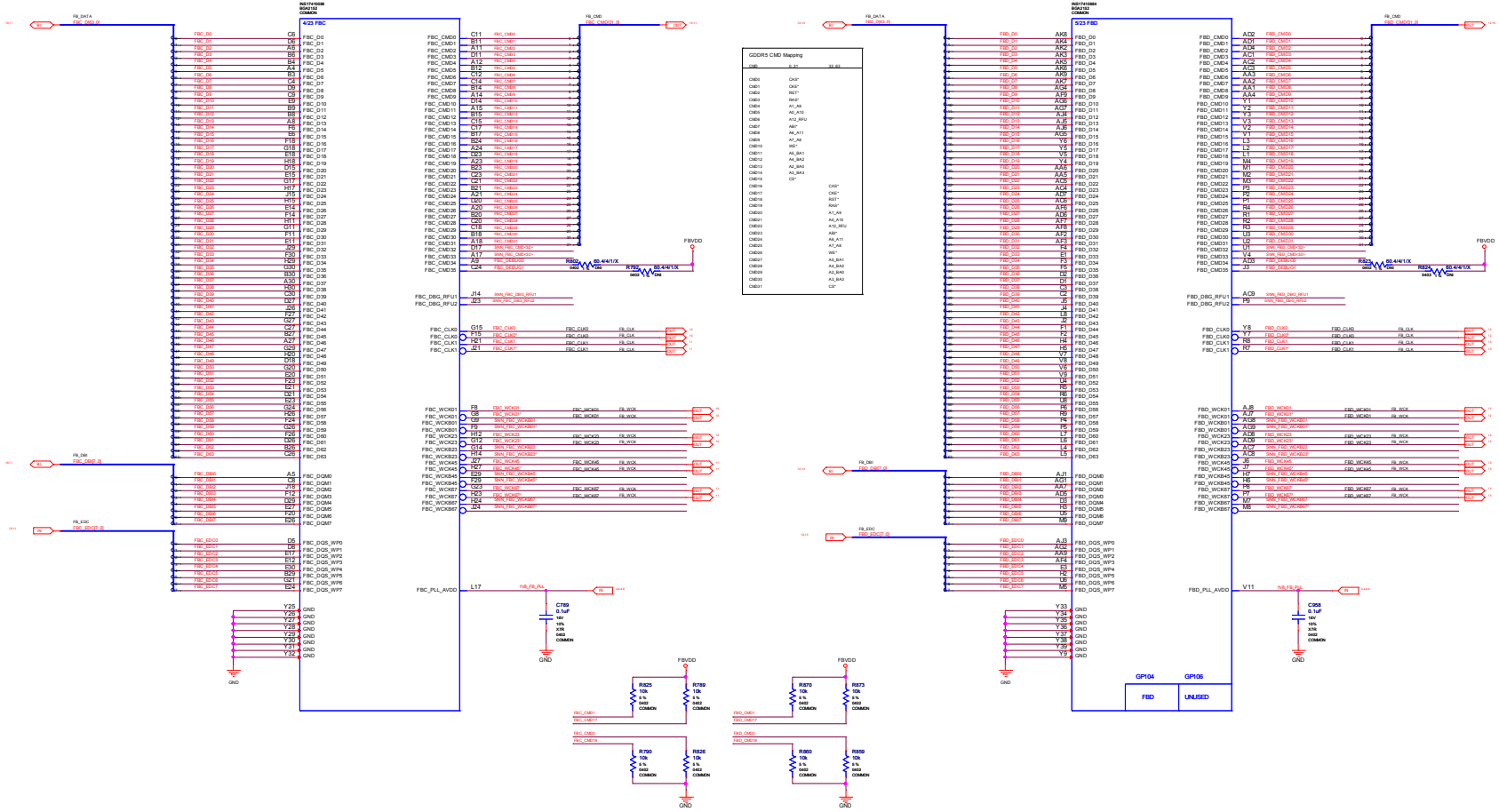
Page8: MEMORY: FBB Partition 63..32



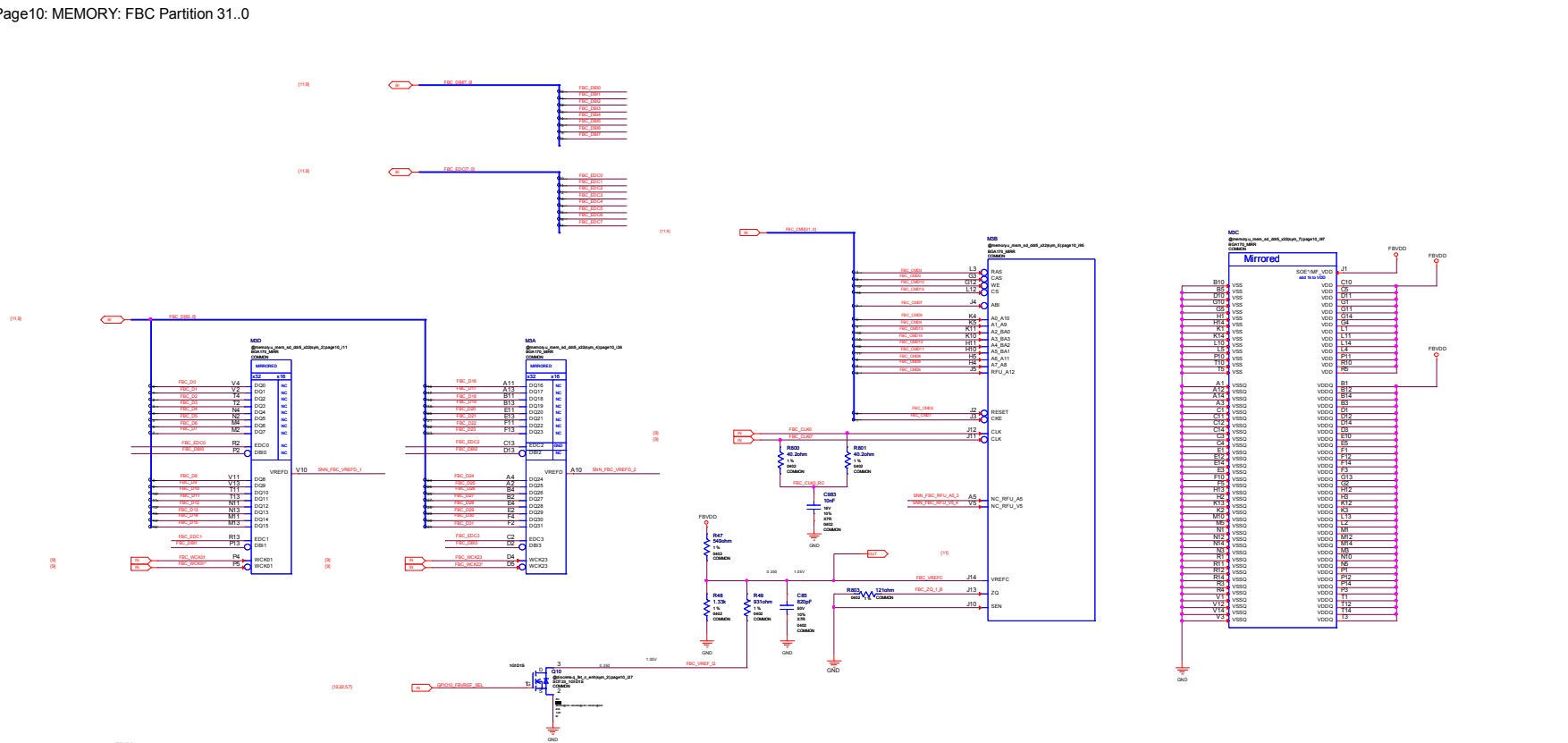
ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL MEMORY: FBB[63:32]

GIGABYTE		
Title: MEMORY: FBB Partition 63..32		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 8 of 42	

Page9: MEMORY: GPU Partition C/D



Page10: MEMORY: FBC Partition 31..0



ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL MEMORY: FBC[31:0]

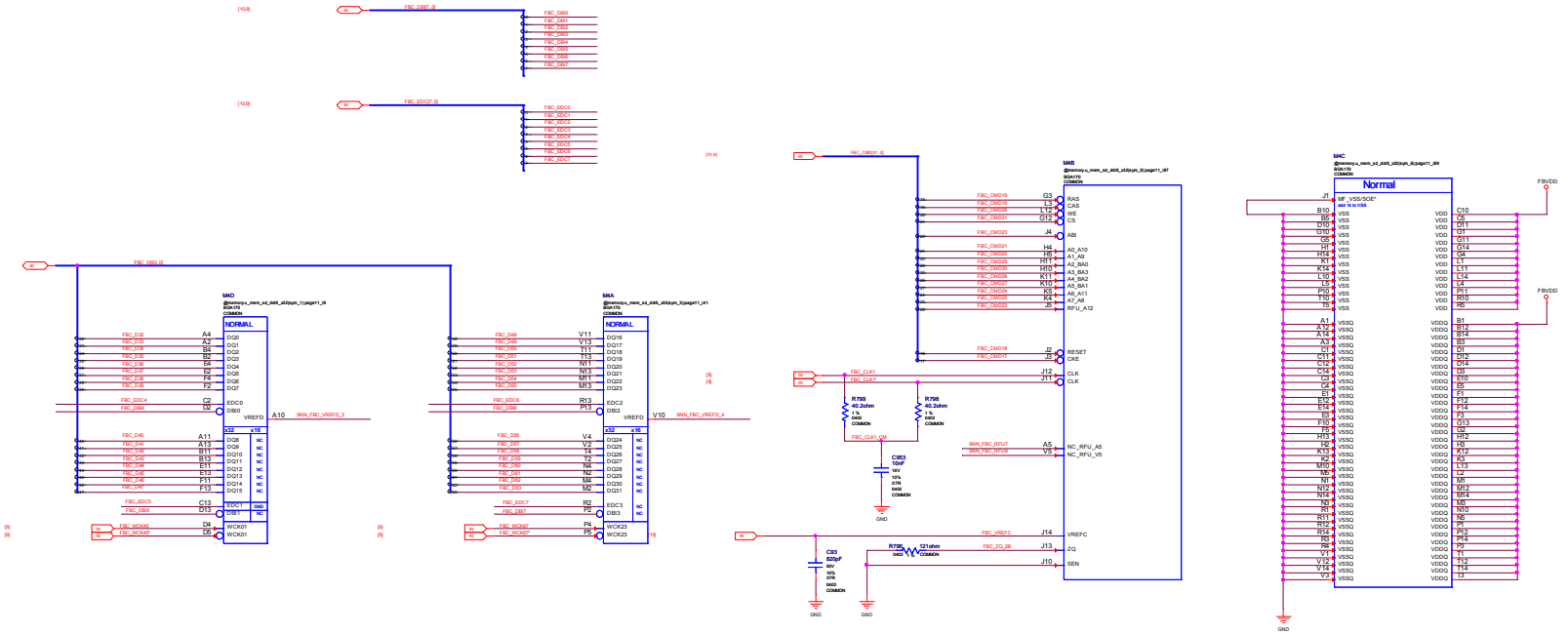
GIGABYTE

Title: MEMORY: FBC Partition 31..0

Size	Document Number	Rev
Custom	GV-N1060G1 GAMING-3GD	1.0

Date: Tuesday, July 19, 2016 Sheet 10 of 42

Page11: MEMORY: FBC Partition 63..32



ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL MEMORY: FBC[63:32]

GIGABYTE

Title	MEMORY: FBC Partition 63..32	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 11 of 42	

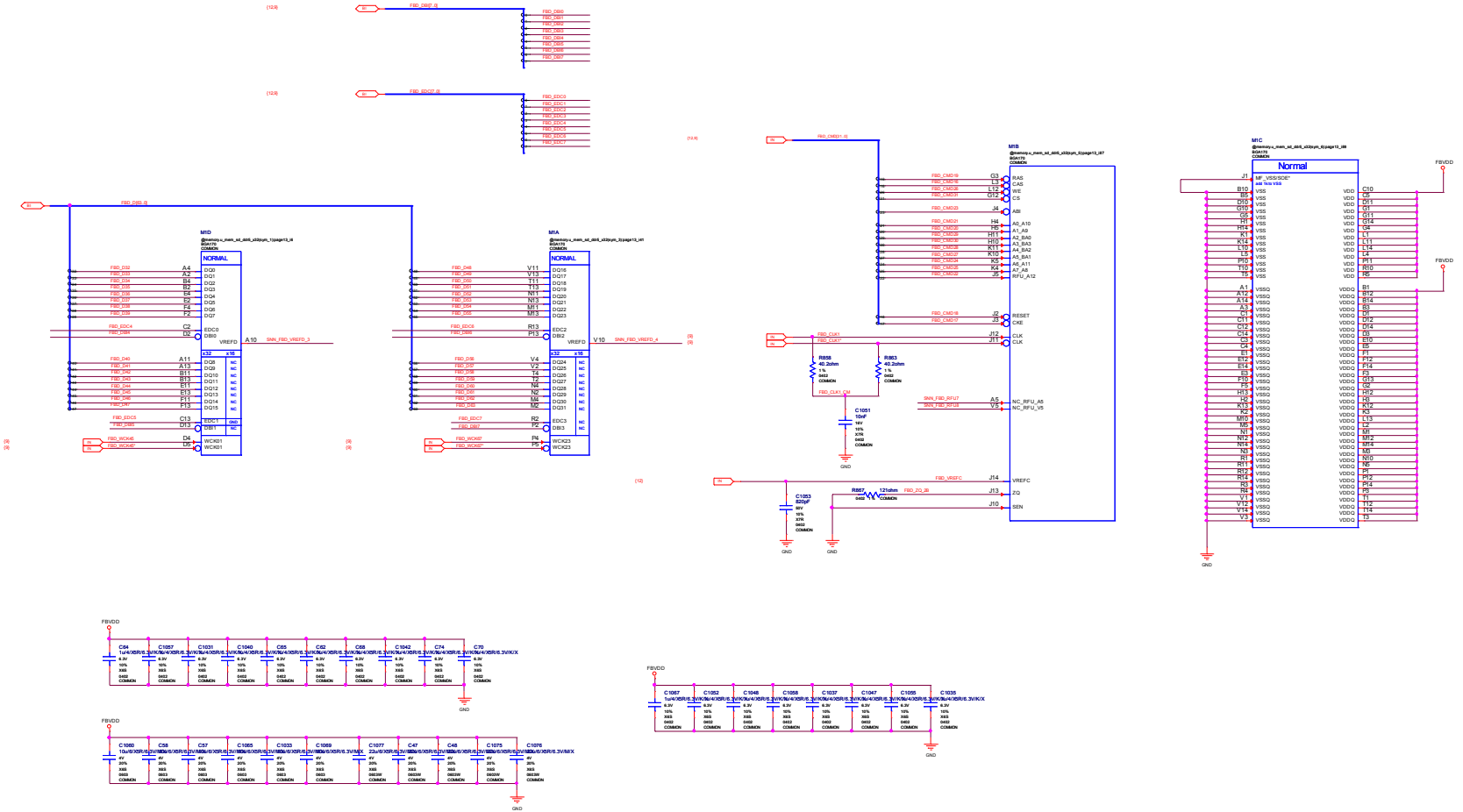
Page12: MEMORY: FBD Partition 31..0

ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL MEMORY: FBD[31:0]

GIGABYTE

Title	MEMORY: FBD Partition 31..0		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD		Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 12 of 42		

Page13: MEMORY: FBD Partition 63..32

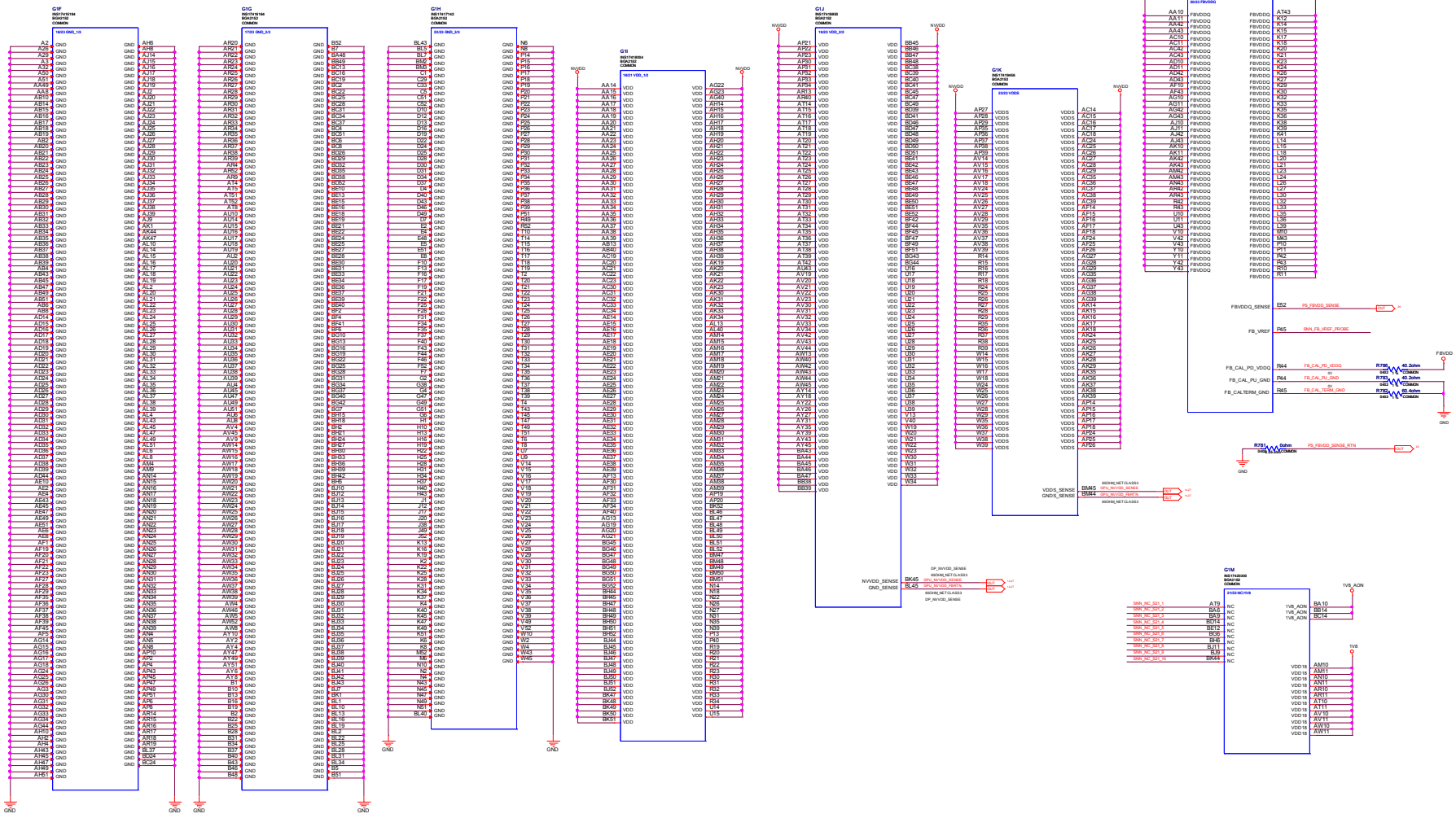


ASSEMBLY: «ASSEMBLY_DESCRIPTION»
PAGE DETAIL: MEMORY: FBD[63:32]

GIGABYTE

Title	MEMORY: FBD Partition 63..32	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 13 of 42	

Page14: GPU PWR and GND



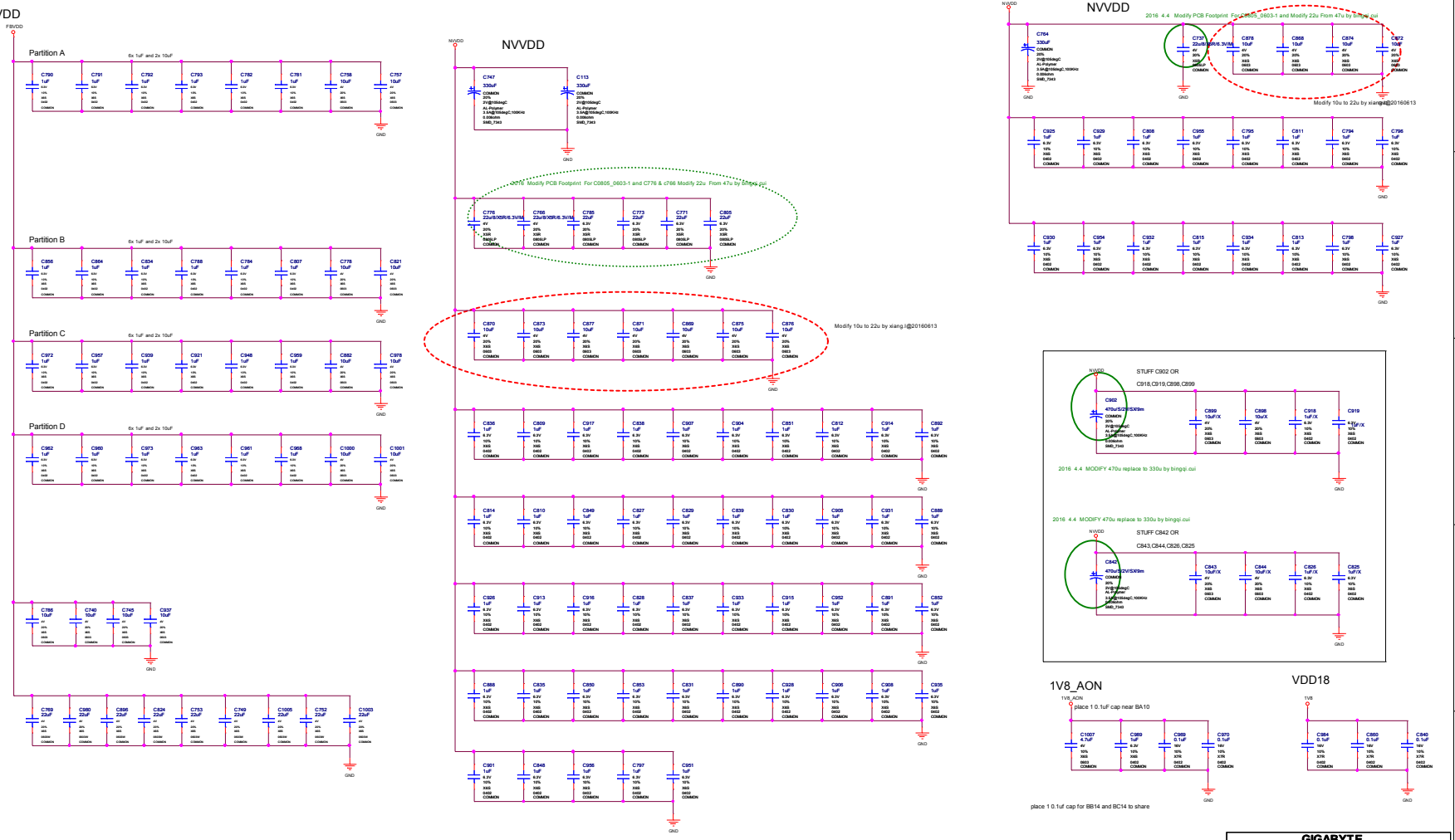
ASSEMBLY
PAGE DETAIL

<ASSEMBLY_DESCRIPTION>
GPU PWR and GND

GIGABYTE

Title	GPU PWR and GND	
Size	Document Number	Rev
Custom	GV-N1060G1 GAMING-3GD	1.0
Date:	Tuesday, July 19, 2016	Sheet 14 of 42

Page15: GPU Decoupling

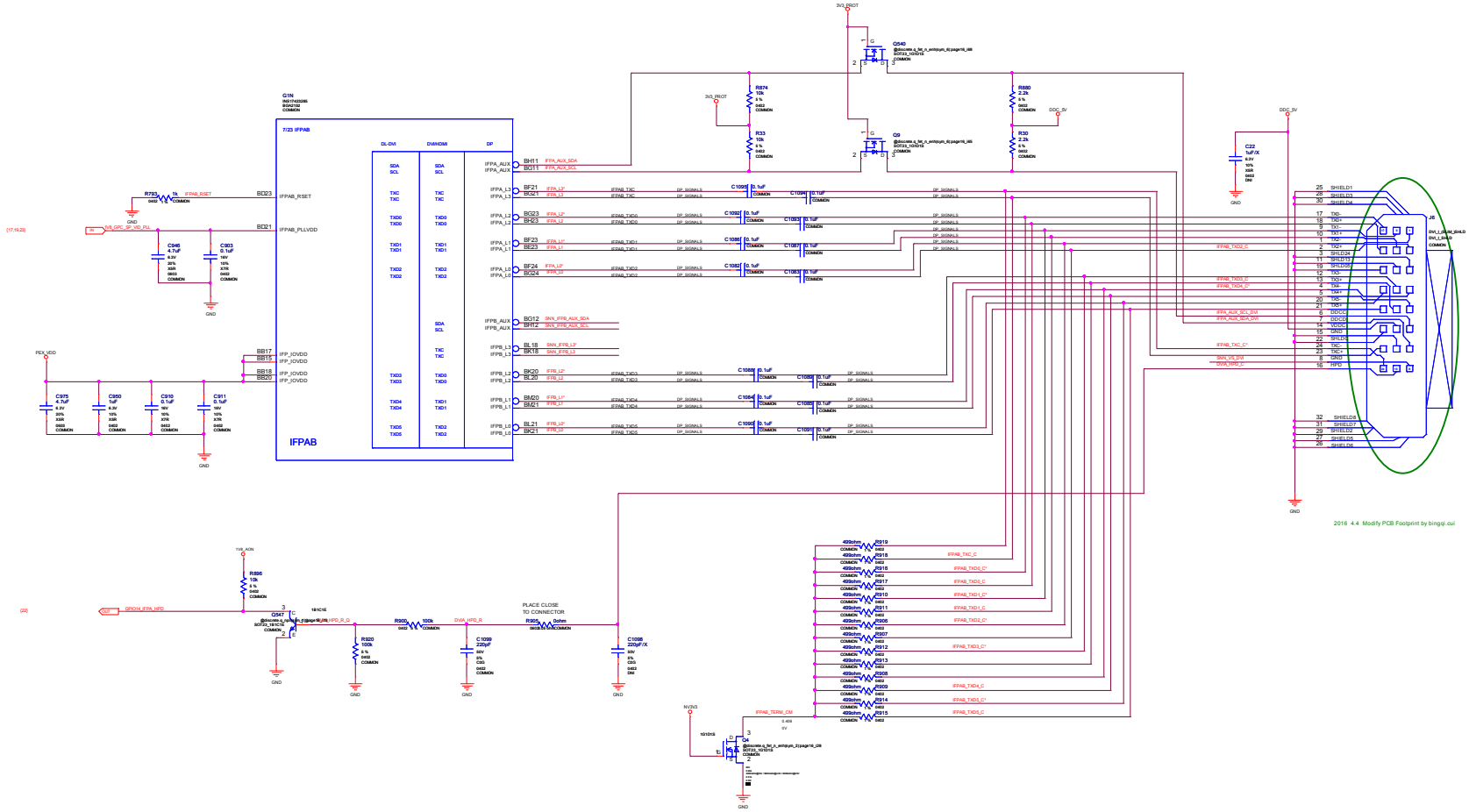


ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	GPU Decoupling

GIGABYTE

Title	GPU Decoupling	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 15 of 42	

Page16: IFPAB DVI-D-DL

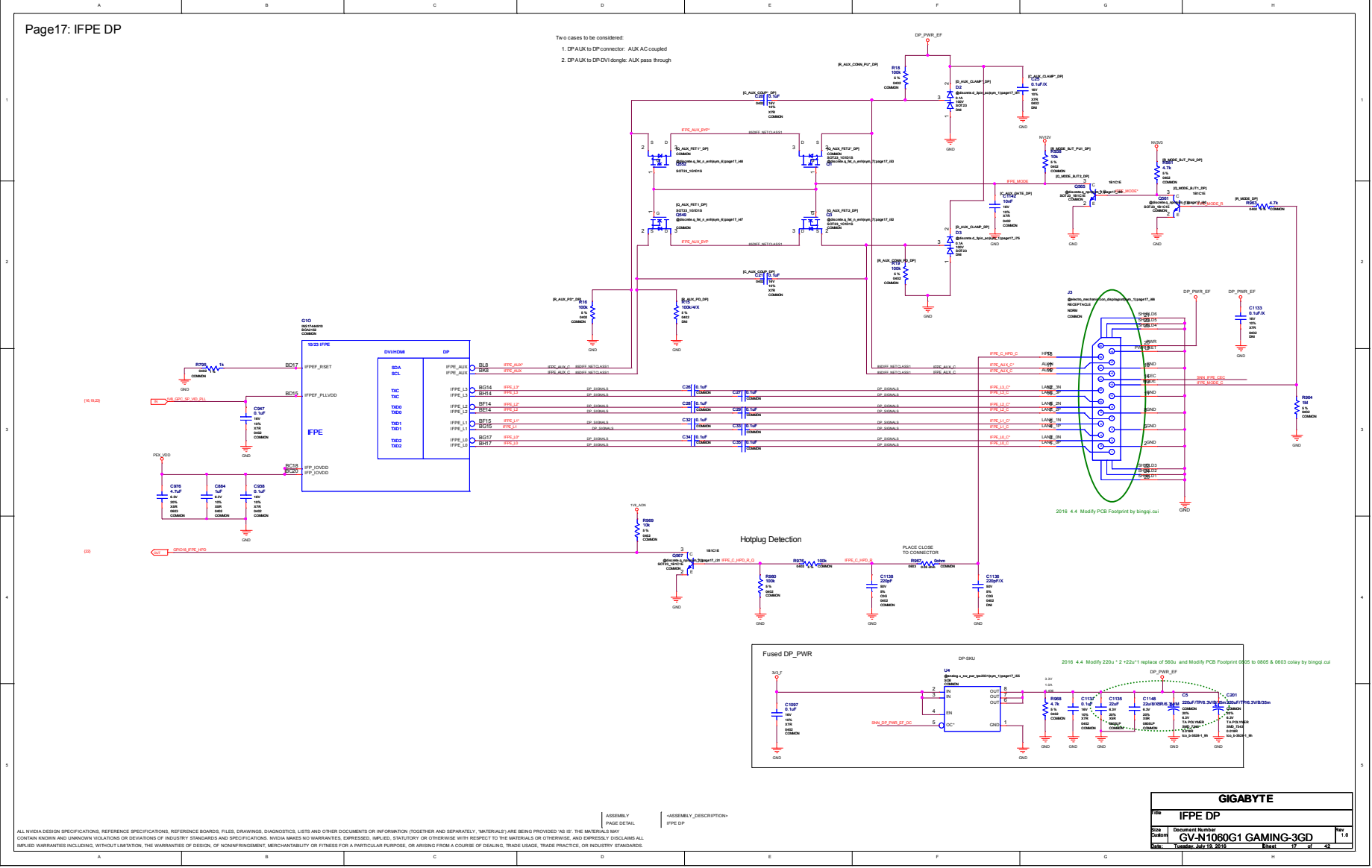


ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
IFPAB DVI-D-DL

GIGABYTE		
Title: IFPAB DVI-D-DL		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 16 of 42	

Page17: IFPE DP



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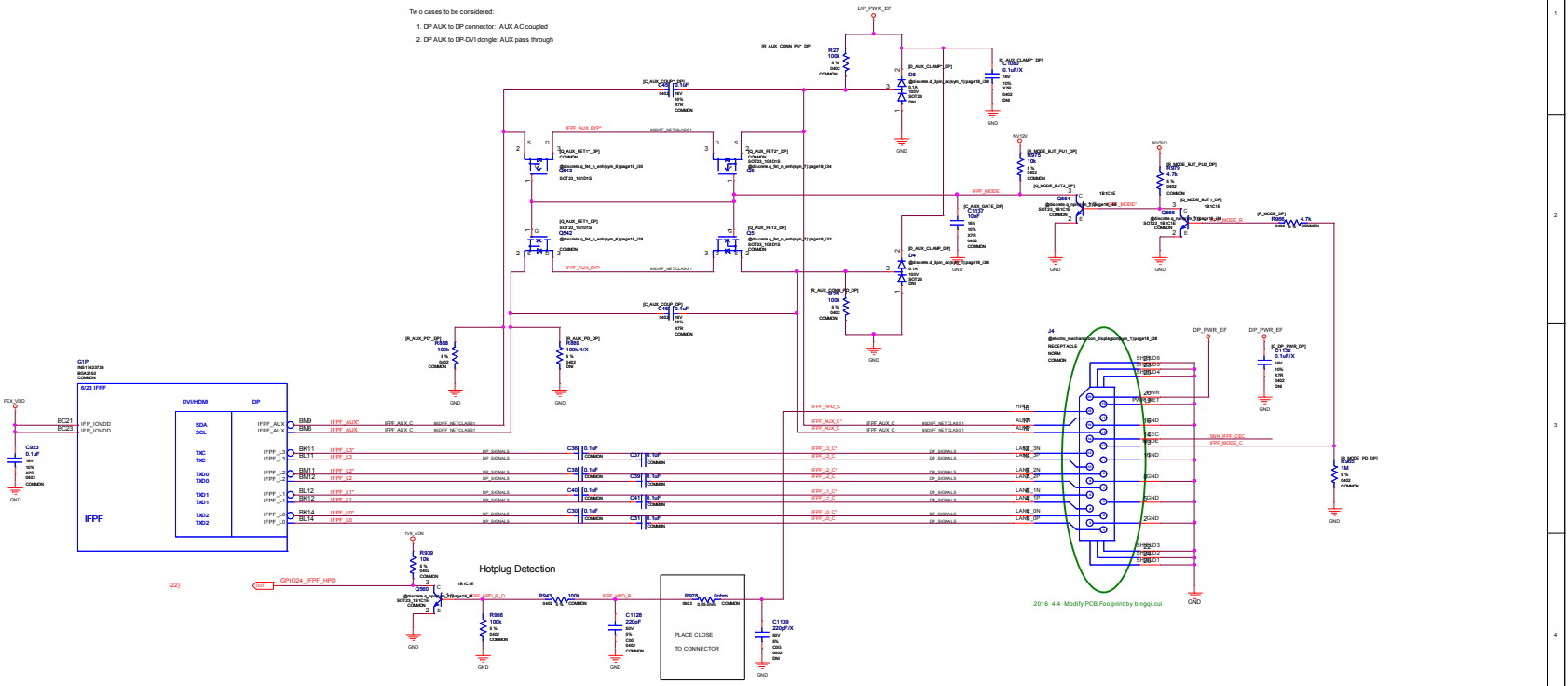
ASSEMBLY | «ASSEMBLY_DESCRIPTION»
PAGE DETAIL | IFPE DP

GIGABYTE

Title	IFPE DP	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 17 of 42	

Page18: IFPF DP

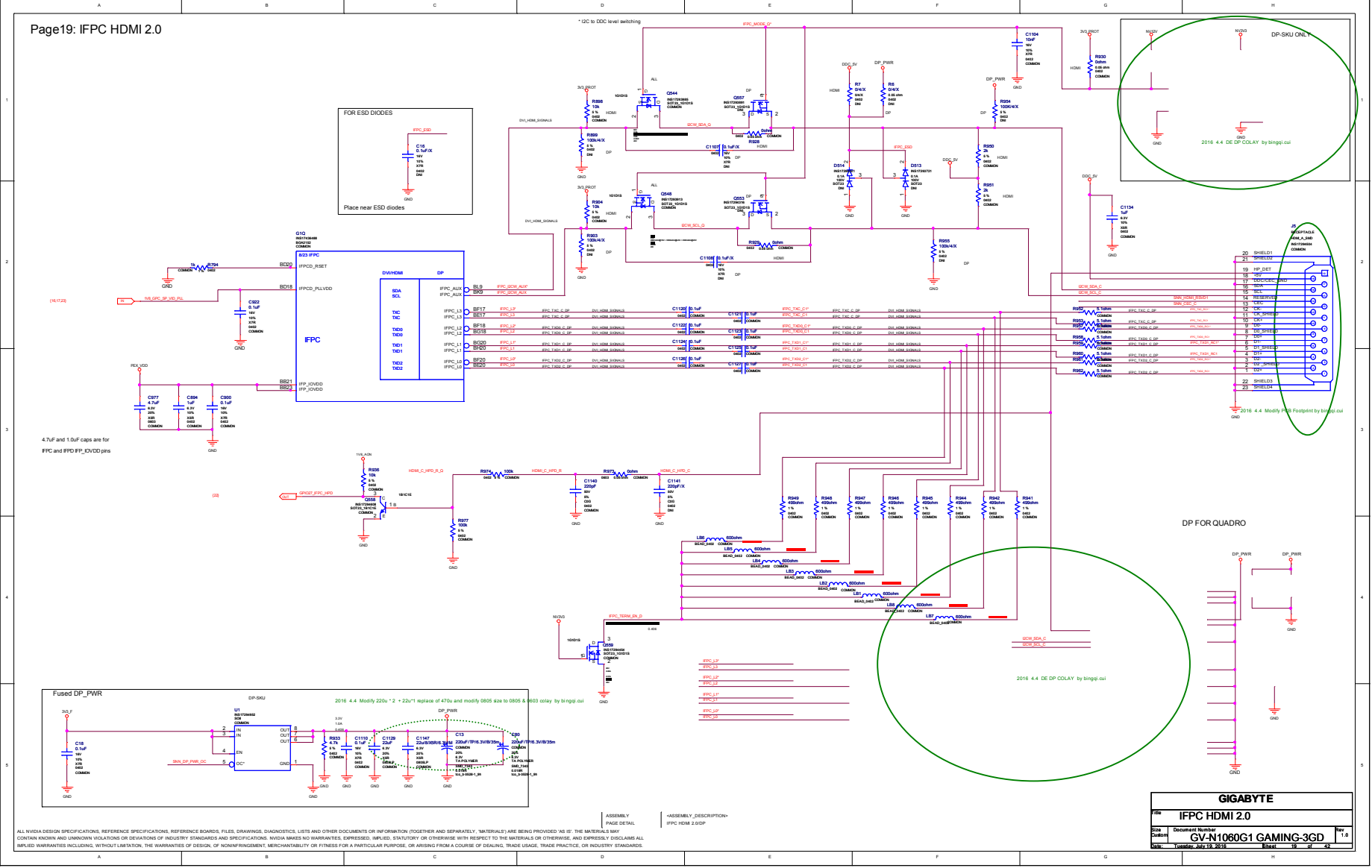


GIGABYTE

Title	IFPF DP	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 18 of 42	

ASSEMBLY
PAGE DETAIL
«ASSEMBLY_DESCRIPTION»
IFPEF DP

Page19: IFPC HDMI 2.0

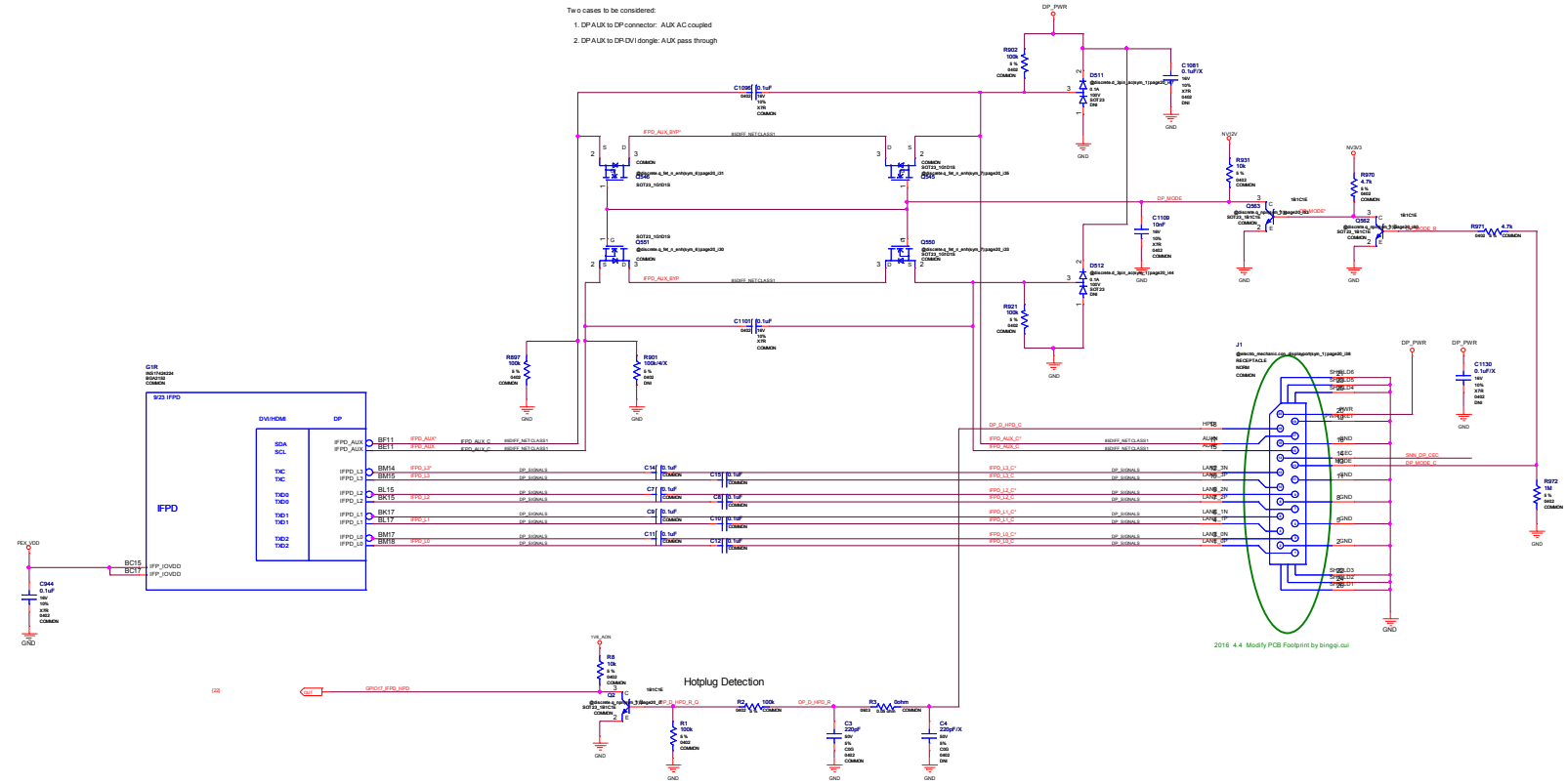


ASSEMBLY	«ASSEMBLY_DESCRIPTION»
PAGE DETAIL	IFPC HDMI 2.0/DP

GIGABYTE

Title	IFPC HDMI 2.0	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 19 of 42	

Page20: IFPD DP



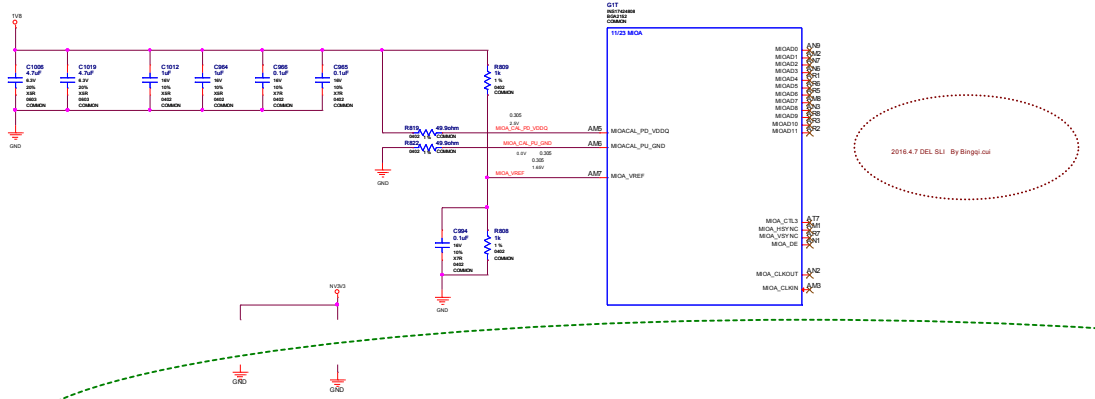
ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
IFPD DP

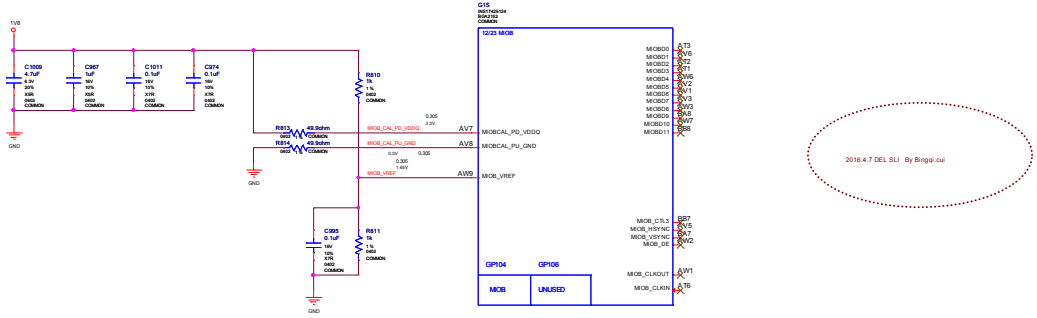
GIGABYTE

Title	IFPD DP	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 20 of 42	

Page21: MIOA/B Interface and FRAME LOCK



2016.4.7 Del Co-Lay By Bingqi.cui



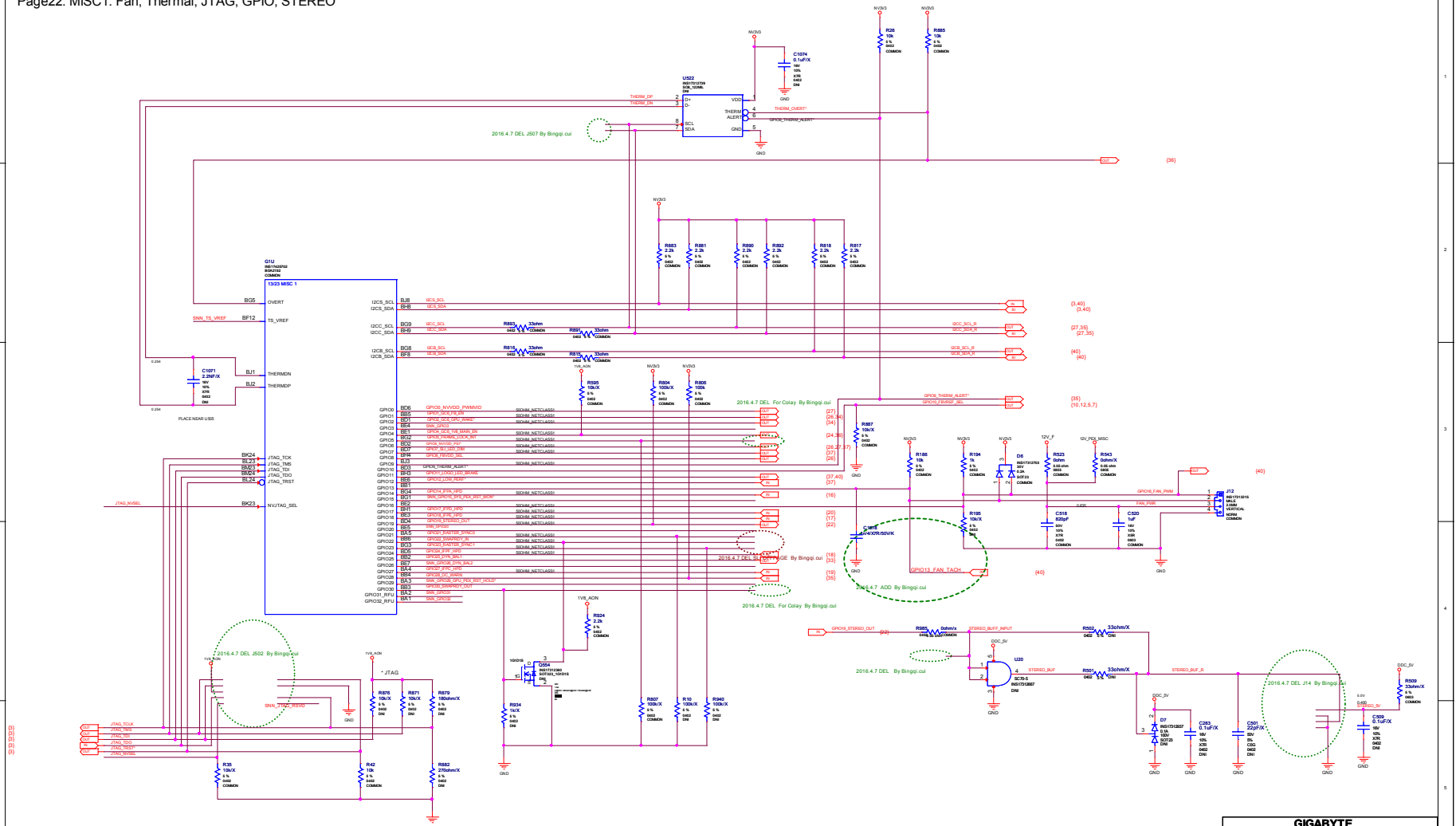
ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
MIOA/B Interface and Frame Lock

GIGABYTE

Title	MIOA/B Interface and FRAME LOCK	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 21 of 42	

Page22: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
MISC1: Fan, Thermal, JTAG, GPIO, Stereo

GIGABYTE

File: MISC1: Fan, Thermal, JTAG, GPIO, STEREO

Size: Custom | Document Number: GV-N1060G1 GAMING-3GD | Rev: 1.0

Date: Tuesday, July 19, 2016 | Sheet 22 of 42

Page23: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

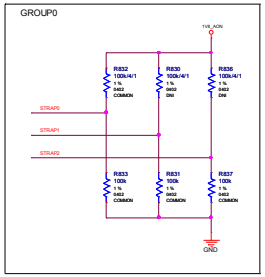
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

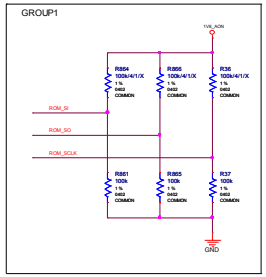
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

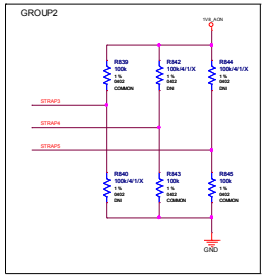
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

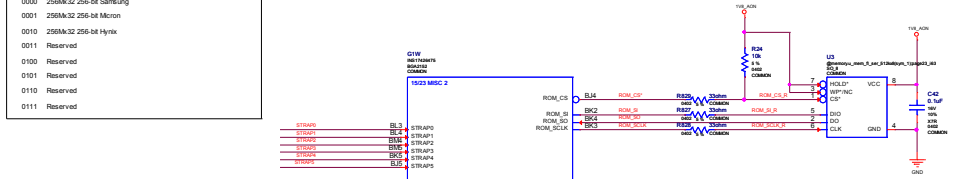
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

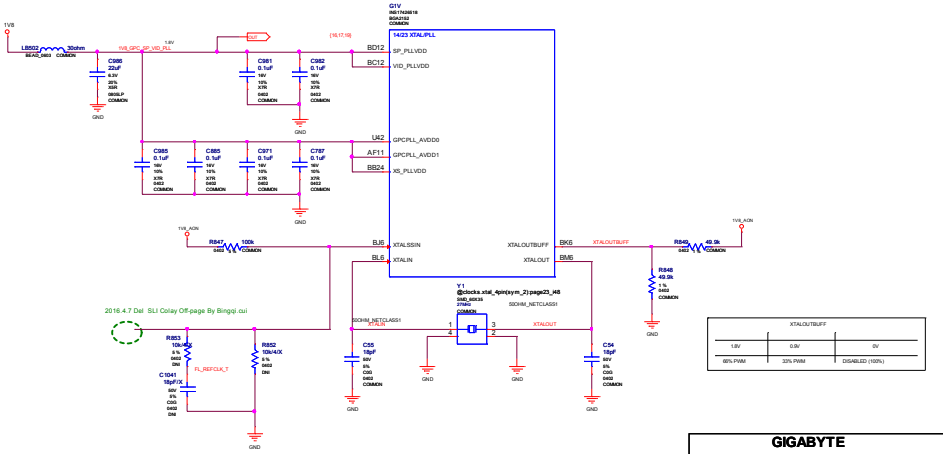






CFG[3:0]	Config Width	Vendor
0000	256Mx32 256-bit	Samsung
0001	256Mx32 256-bit	Micron
0010	256Mx32 256-bit	Hynix
0011	Reserved	
0100	Reserved	
0101	Reserved	
0110	Reserved	
0111	Reserved	



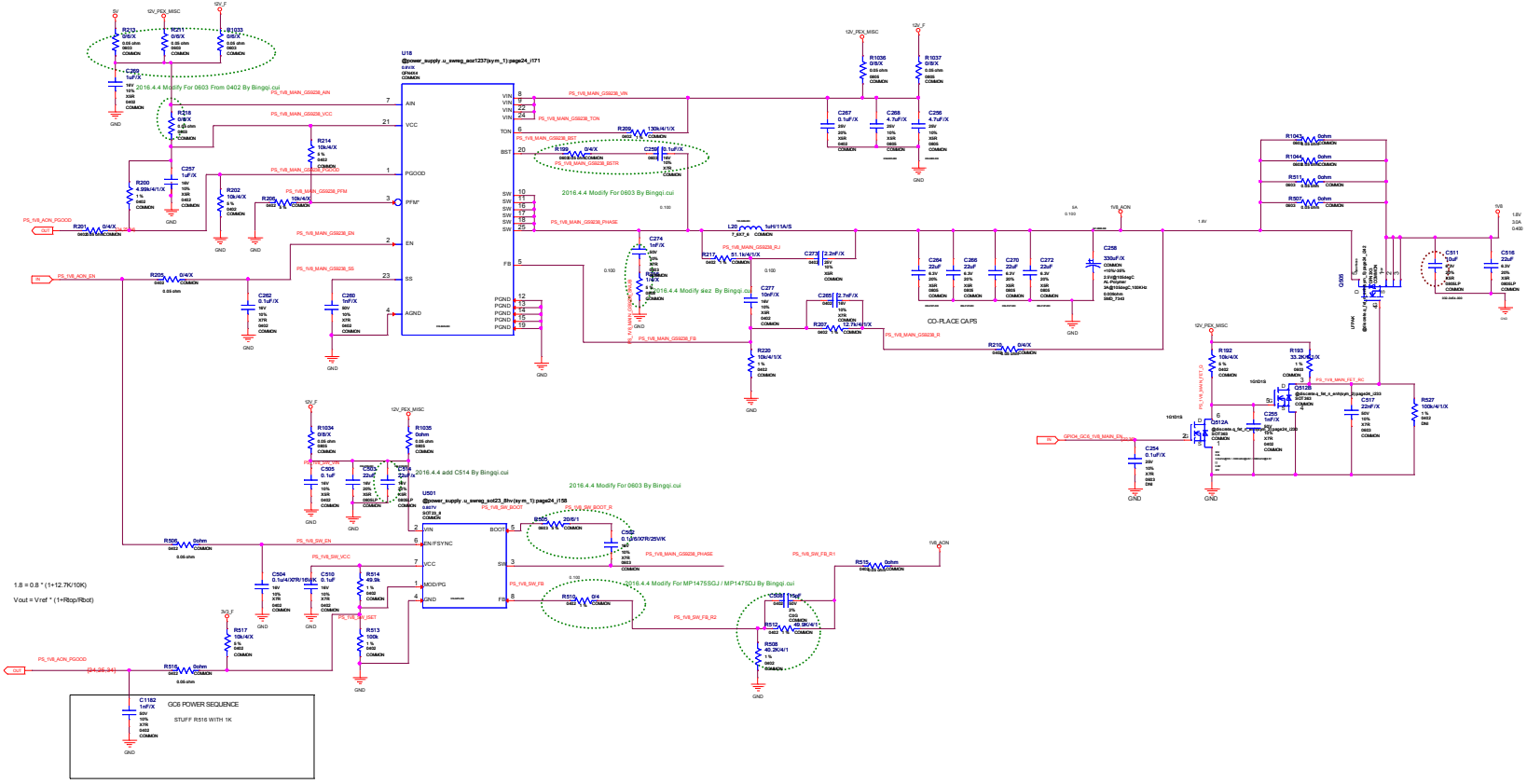


ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL MISC2: ROM, XTAL, Straps

GIGABYTE

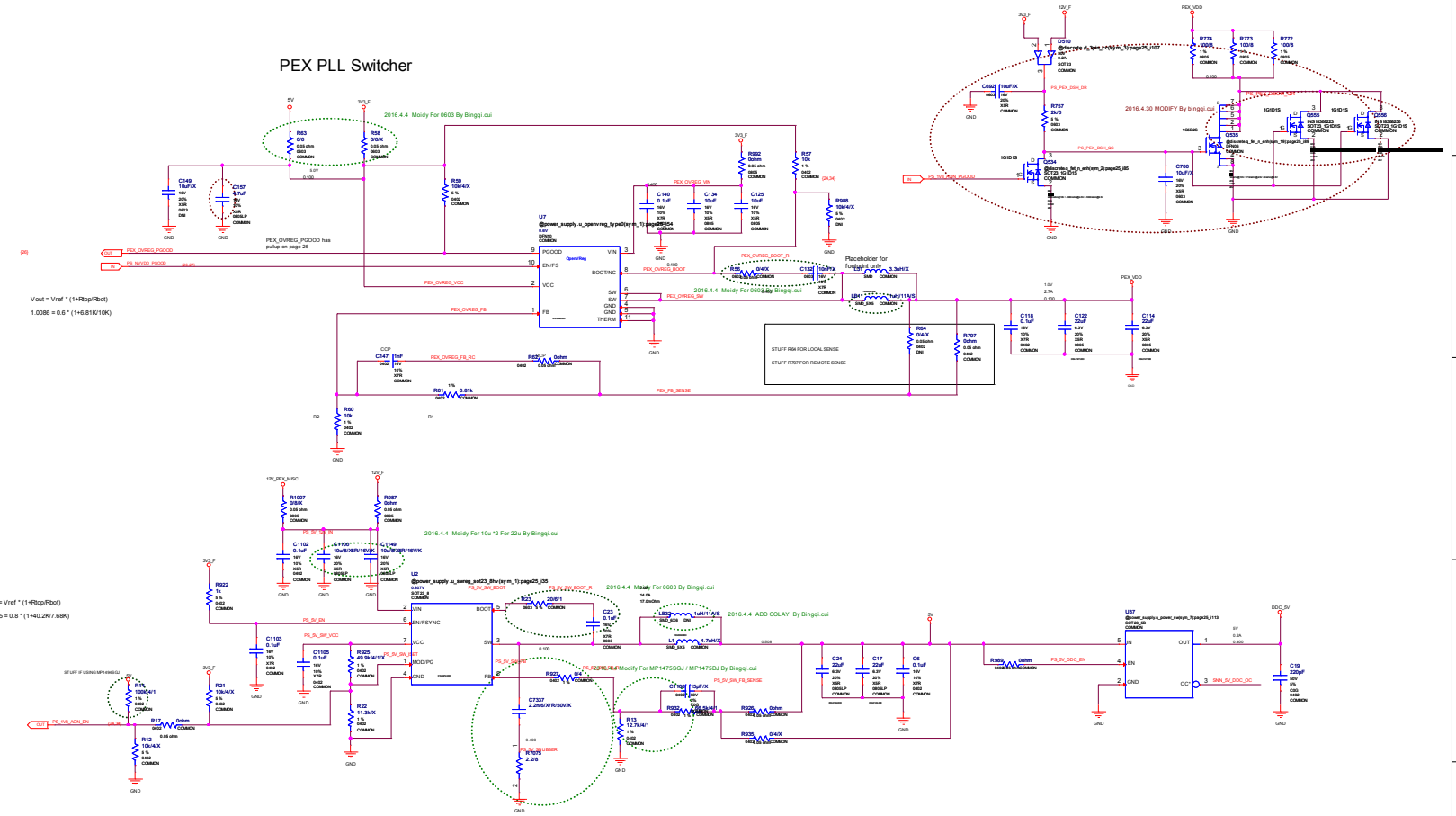
Title	MISC2: ROM, XTAL, Straps		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD		Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 23 of 42		

Page24: PS: 1V8, 1V8_AON

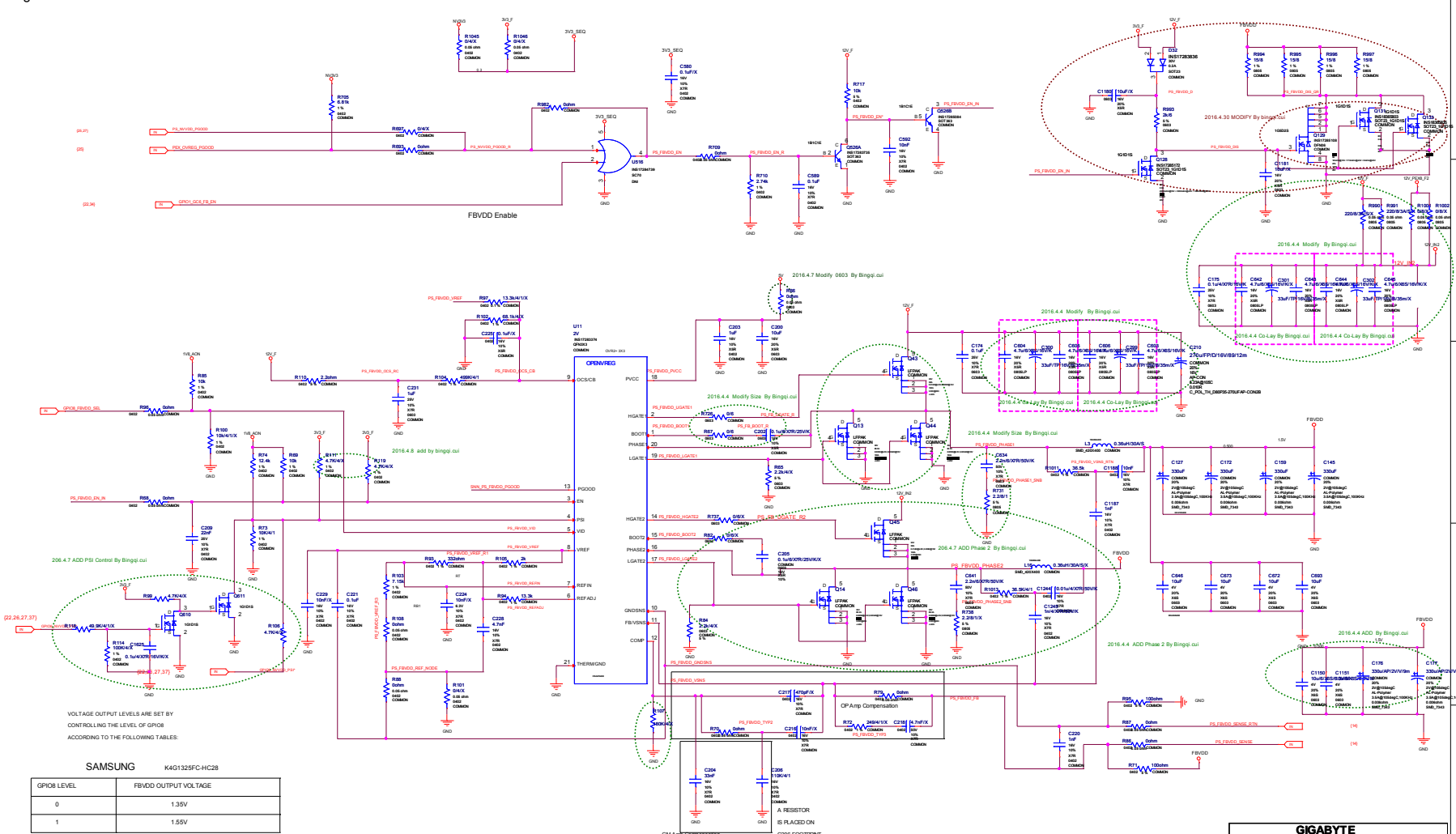


ASSEMBLY	«ASSEMBLY_DESCRIPTION»	
PAGE DETAIL	PS: 1V8, 1V8_AON	

GIGABYTE			
Title	1V8, 1V8_AON		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD		Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 24 of 42		



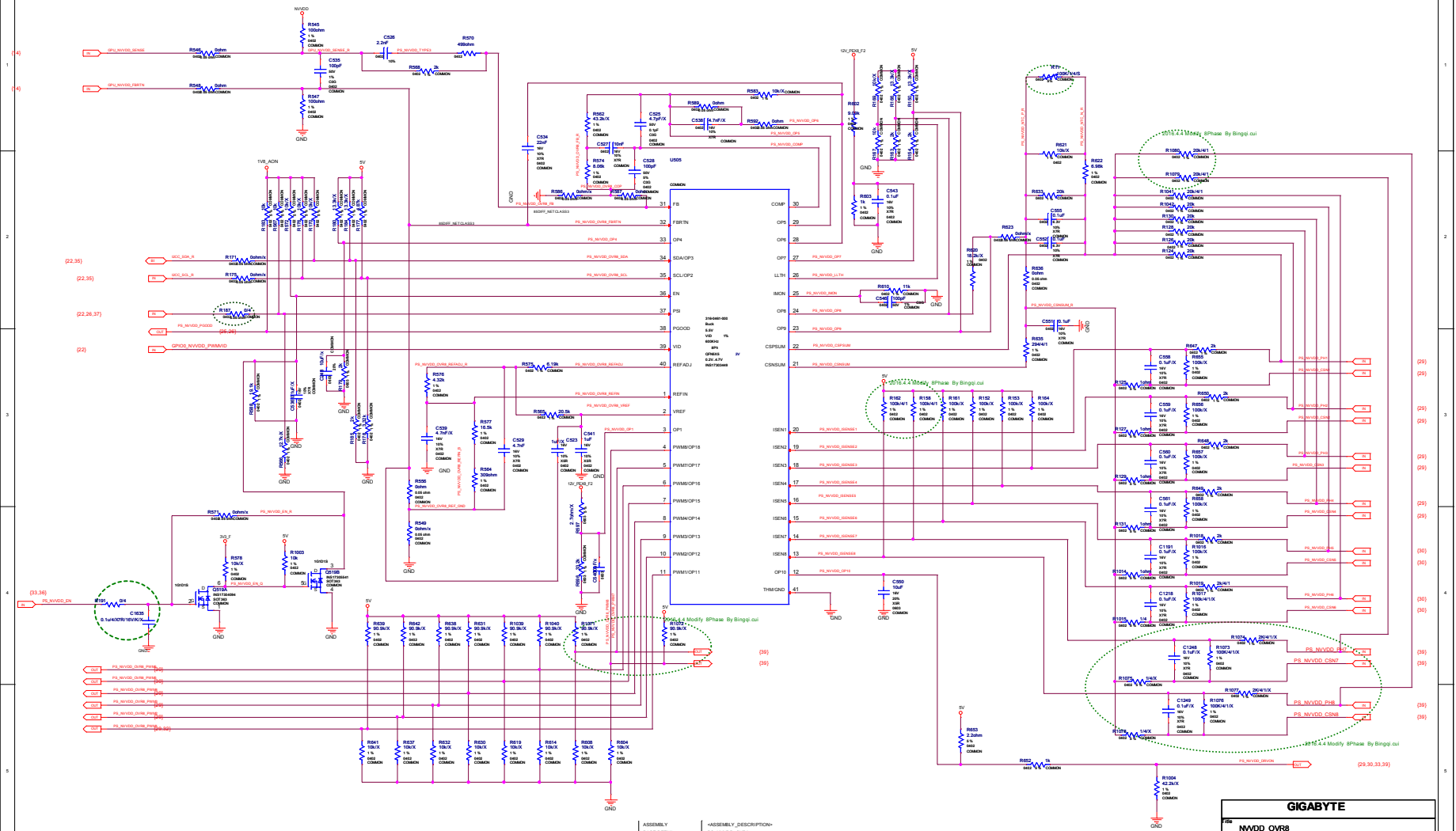
Page26: PS: FBVDD



GIGABYTE

Title	FBVDD	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 26 of 42	

Page27: PS: NVVDD_OVR8



ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL PS: NVVDD_OVR8

GIGABYTE

Title	NVVDD_OVR8	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 27 of 42	

Page28: PS: Blank Page

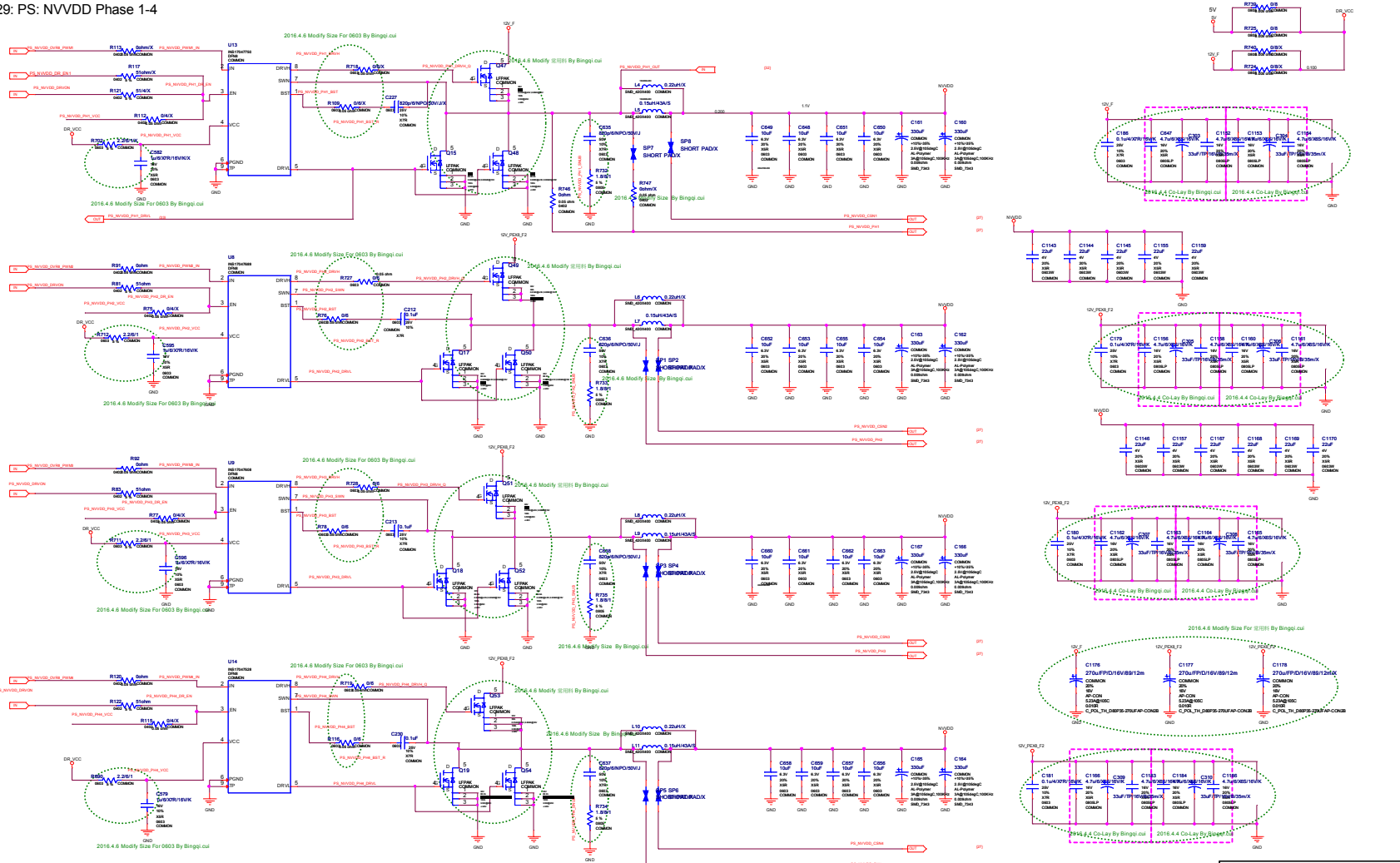
ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
PS: Blank Page

GIGABYTE

Title: Blank Page		
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 28 of 42	

Page29: PS: NVVDD Phase 1-4



ASSEMBLY
PAGE DETAIL

«ASSEMBLY_DESCRIPTION»
PS: NVVDD Phase 1-4

GIGABYTE

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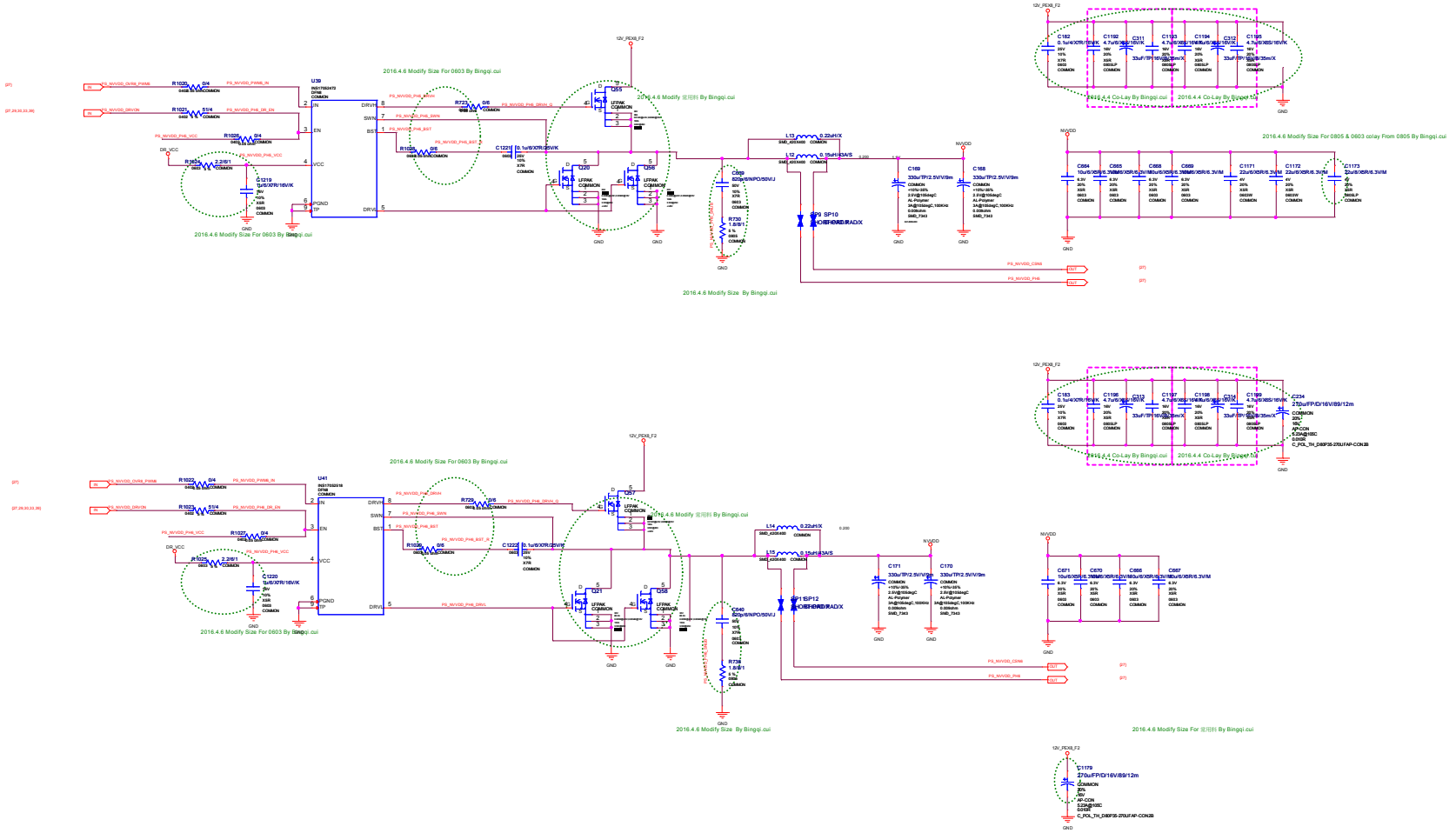
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 29 of 42	



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PAGE DETAIL | PS: NVVDD Phase 5 & 6

GIGABYTE

Title	NVDD Phase 5 & 6	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 30 of 42	

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PAGE DETAIL

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GIGABYTE

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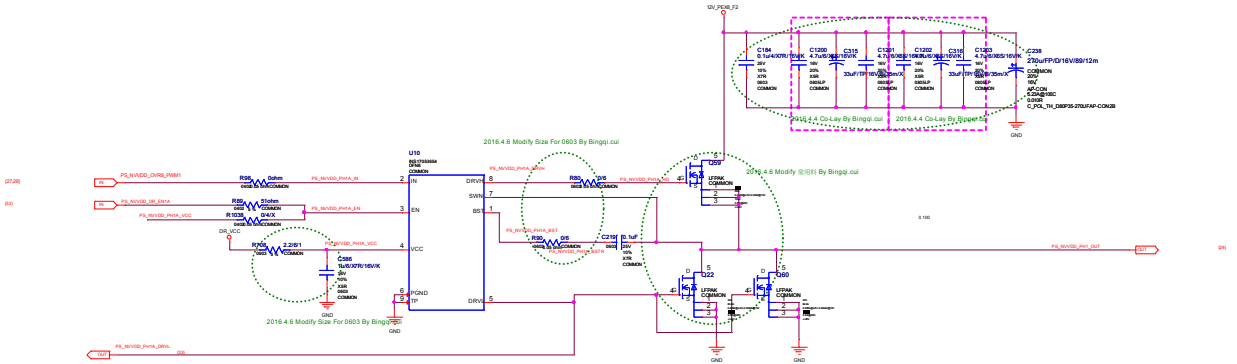
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 31 of 42	

Page32: PS: Dynamic Power Balance Phases



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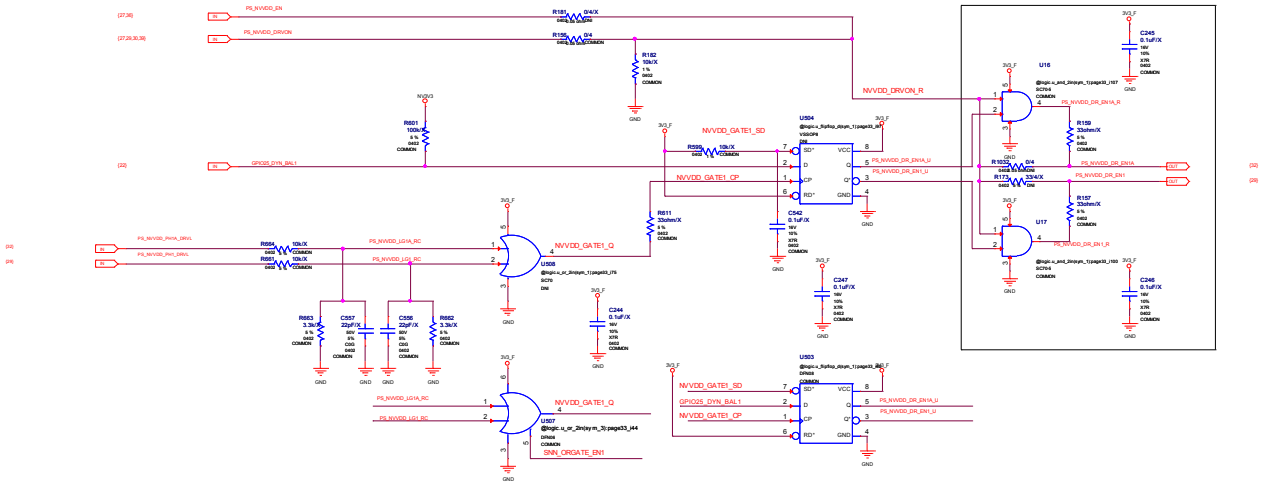
Size	Custom
Document Number	GV-N1060G1 GAMING-3GD
Rev	1.0
Date	Tuesday, July 19, 2016
Sheet	32 of 42

GIGABYTE

Page33: PS: Dynamic Power Balance Logic



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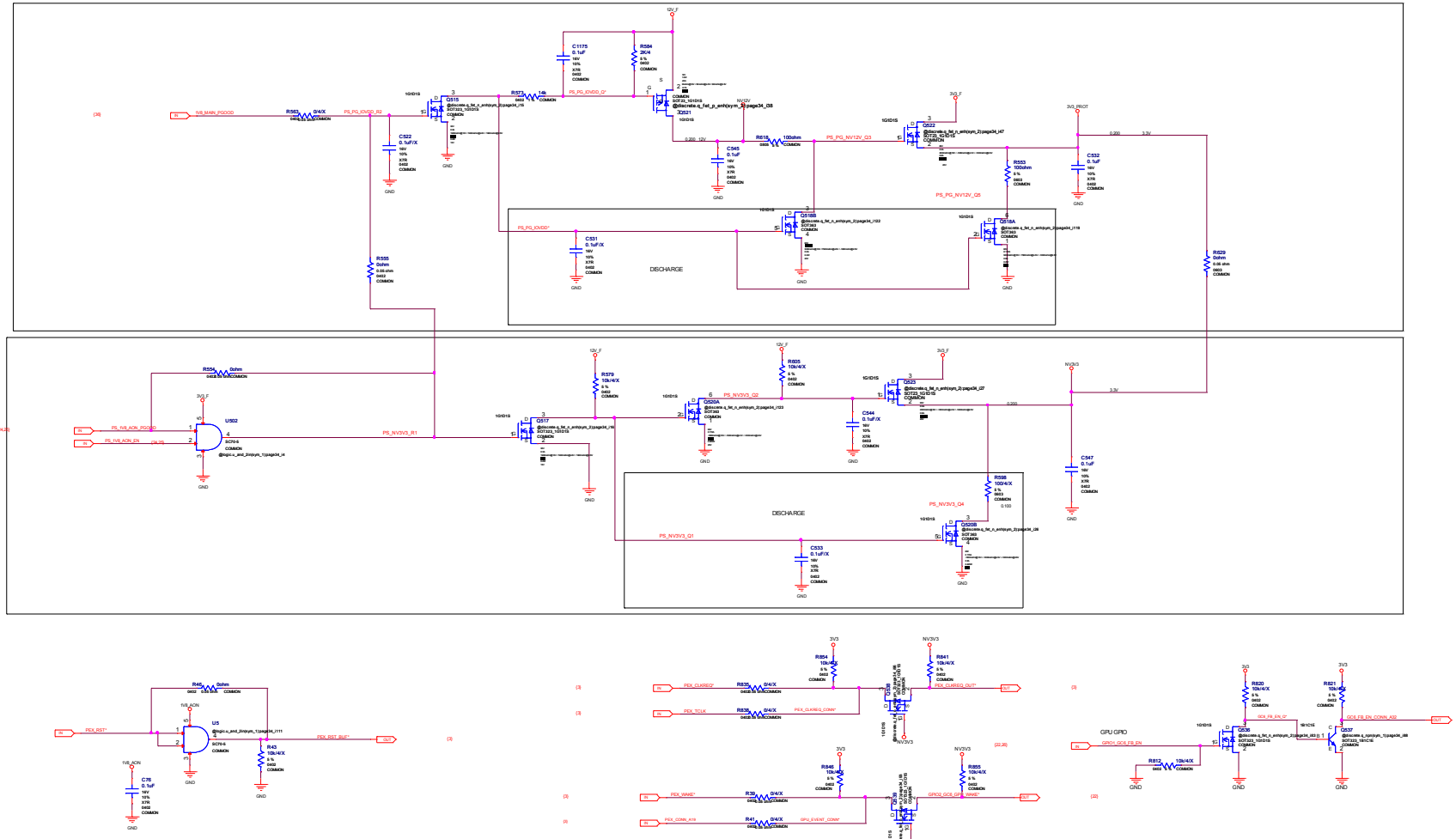
GIGABYTE

Title	Dynamic Power Balance Logic	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 33 of 42	

Page34:PS: NV3V3, NV12V



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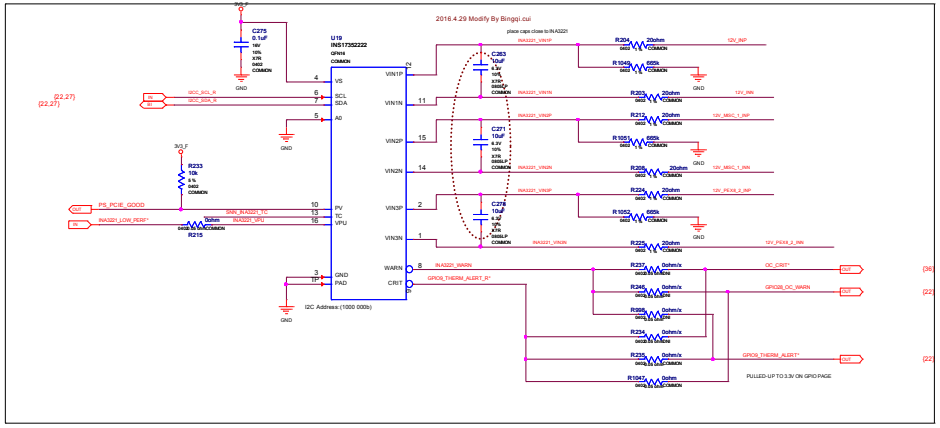
PAGE DETAIL PS: NV3V3, NV12V

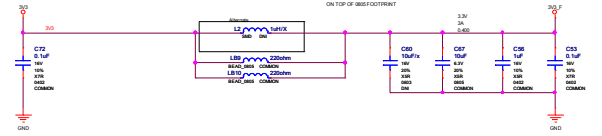
GIGABYTE

Title	NV3V3, NV12V	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 34 of 42	

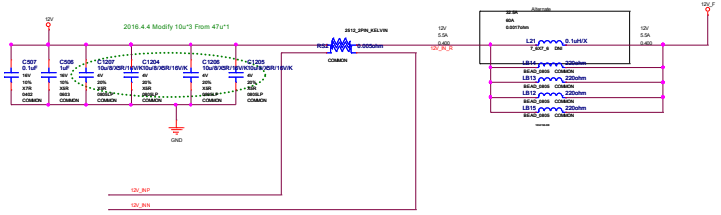
Page35: PS: Inputs, Filtering, and Monitoring

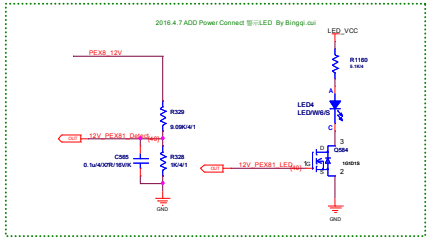


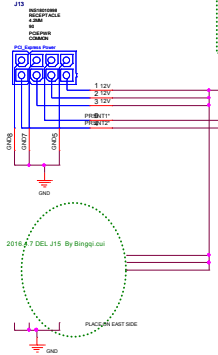
PEX 3V3 INPUT - 10W

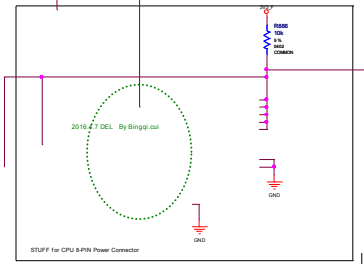


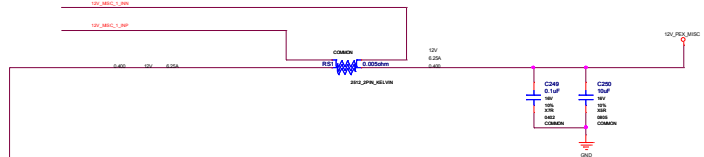
PEX_12V INPUT - 66W



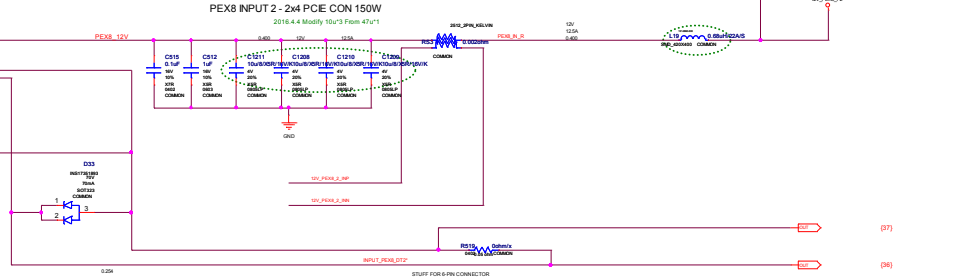








PEX8 INPUT 2 - 2x4 PCIE CON 150W



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PS: Inputs, Filtering, and Monitoring

GIGABYTE

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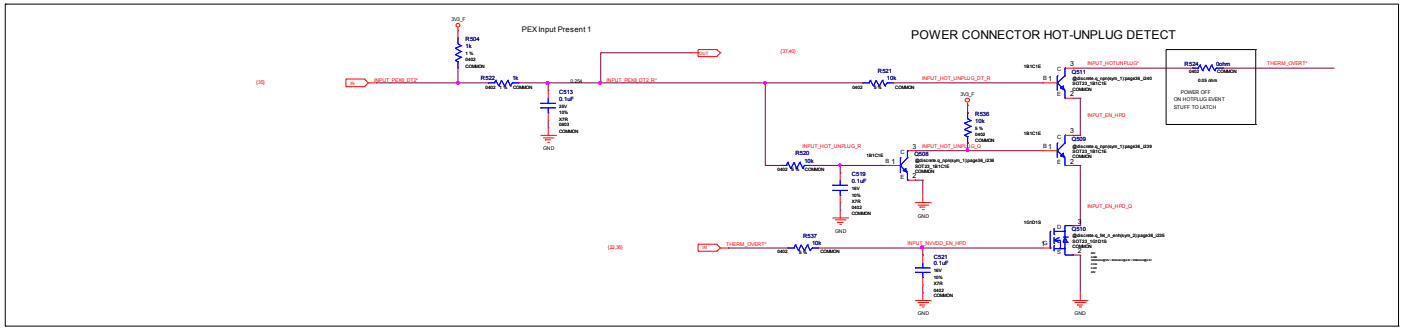
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 35 of 42	



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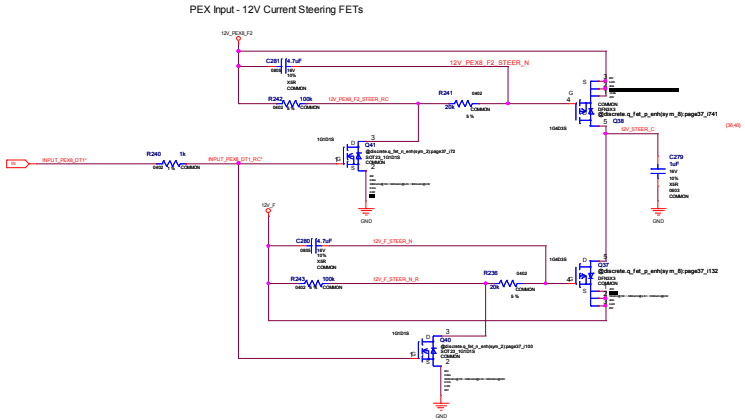
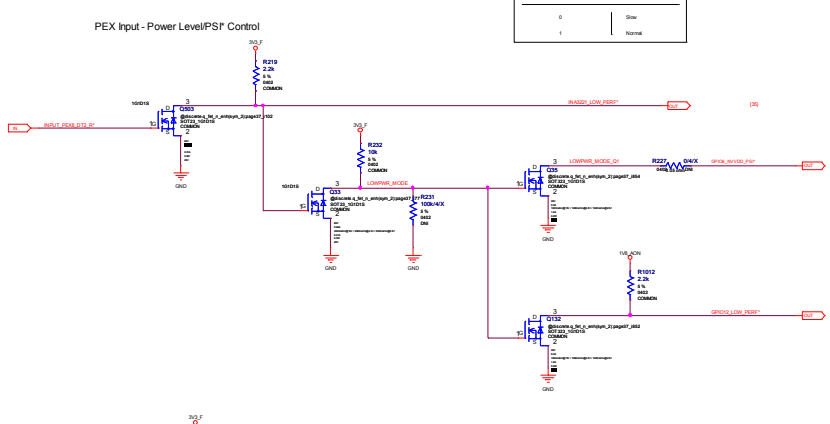
PS: Shutdown and Sequencing

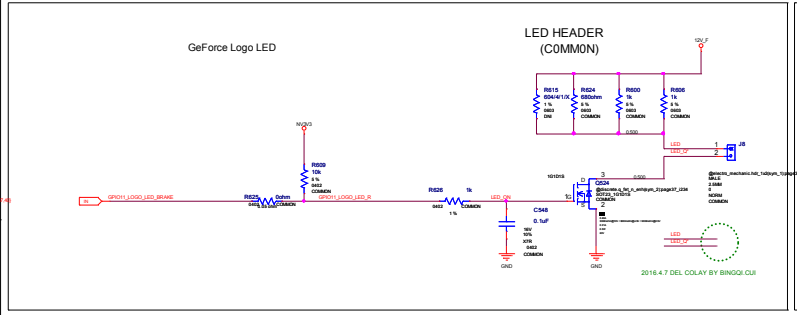
GIGABYTE

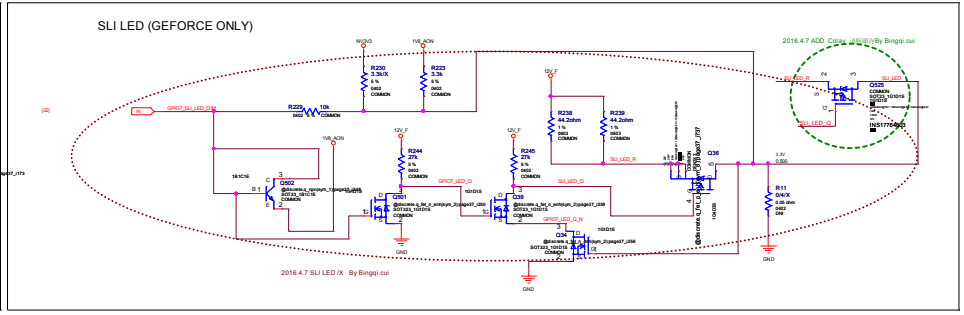
Title	Shutdown and Sequencing	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 36 of 42	

Page37: PS: 12V Current Steering, PSI Control, and LED









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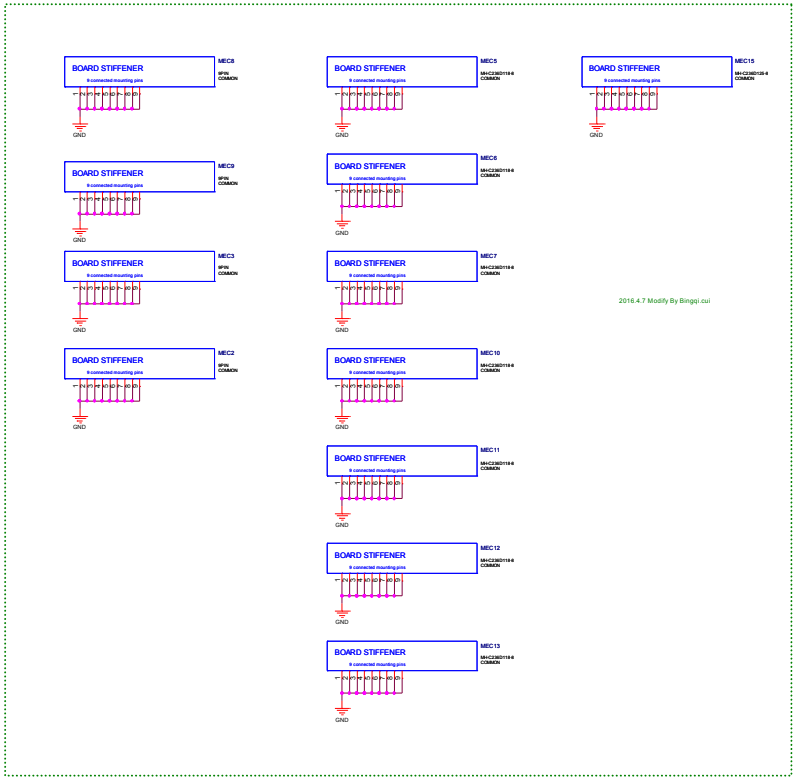
ASSEMBLY «ASSEMBLY_DESCRIPTION»
PAGE DETAIL PS: 12V Current Steering PSI Control and LED

GIGABYTE

Title	12V Current Steering, PSI Control, and LED	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 37 of 42	

Page38: Mechanical: Bracket/Thermal Solution



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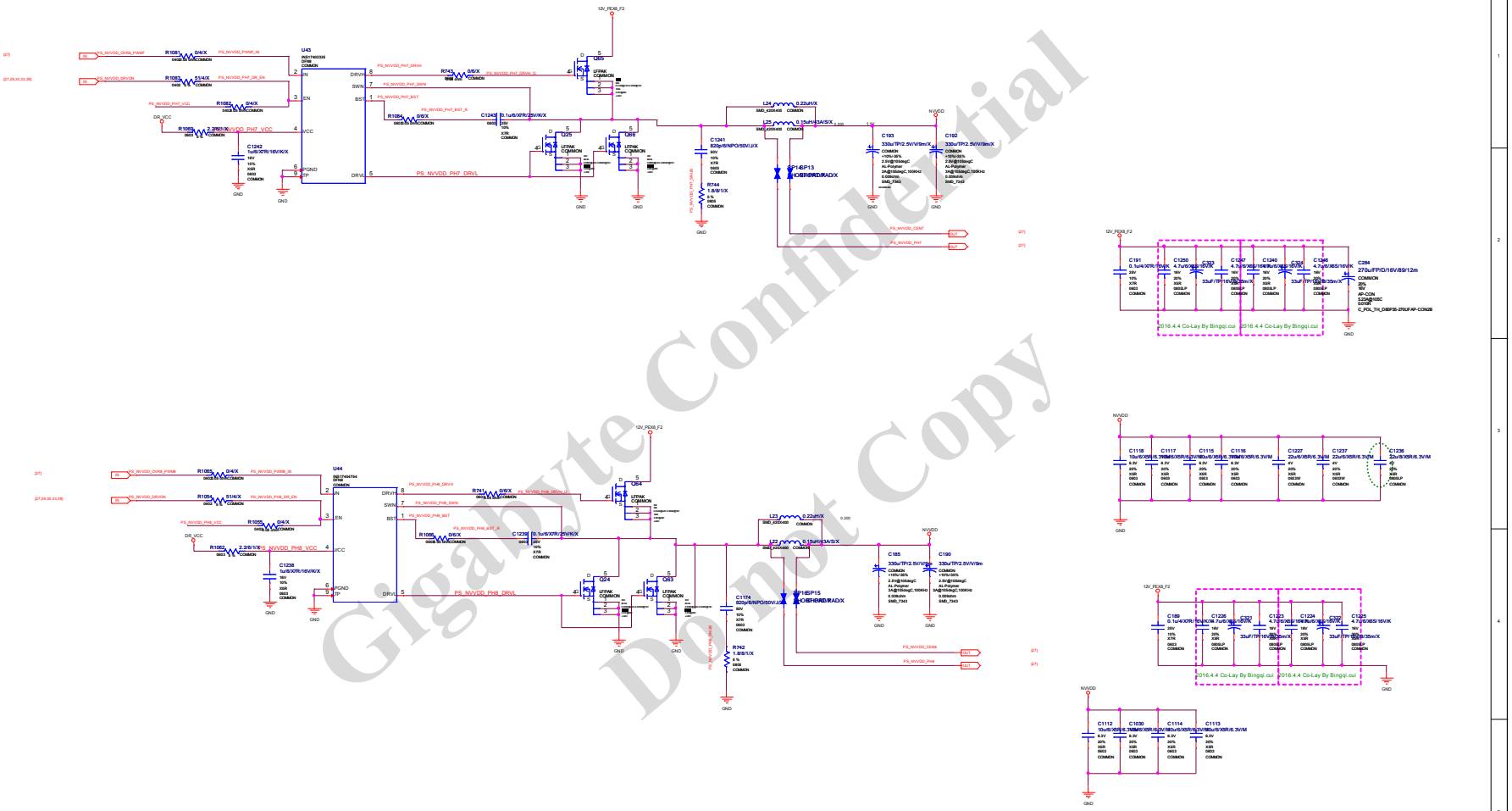
GIGABYTE

Title	Bracket/Thermal Solution	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 38 of 42	

Page30: PS: NVVDD Phase 7 & 8



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GIGABYTE

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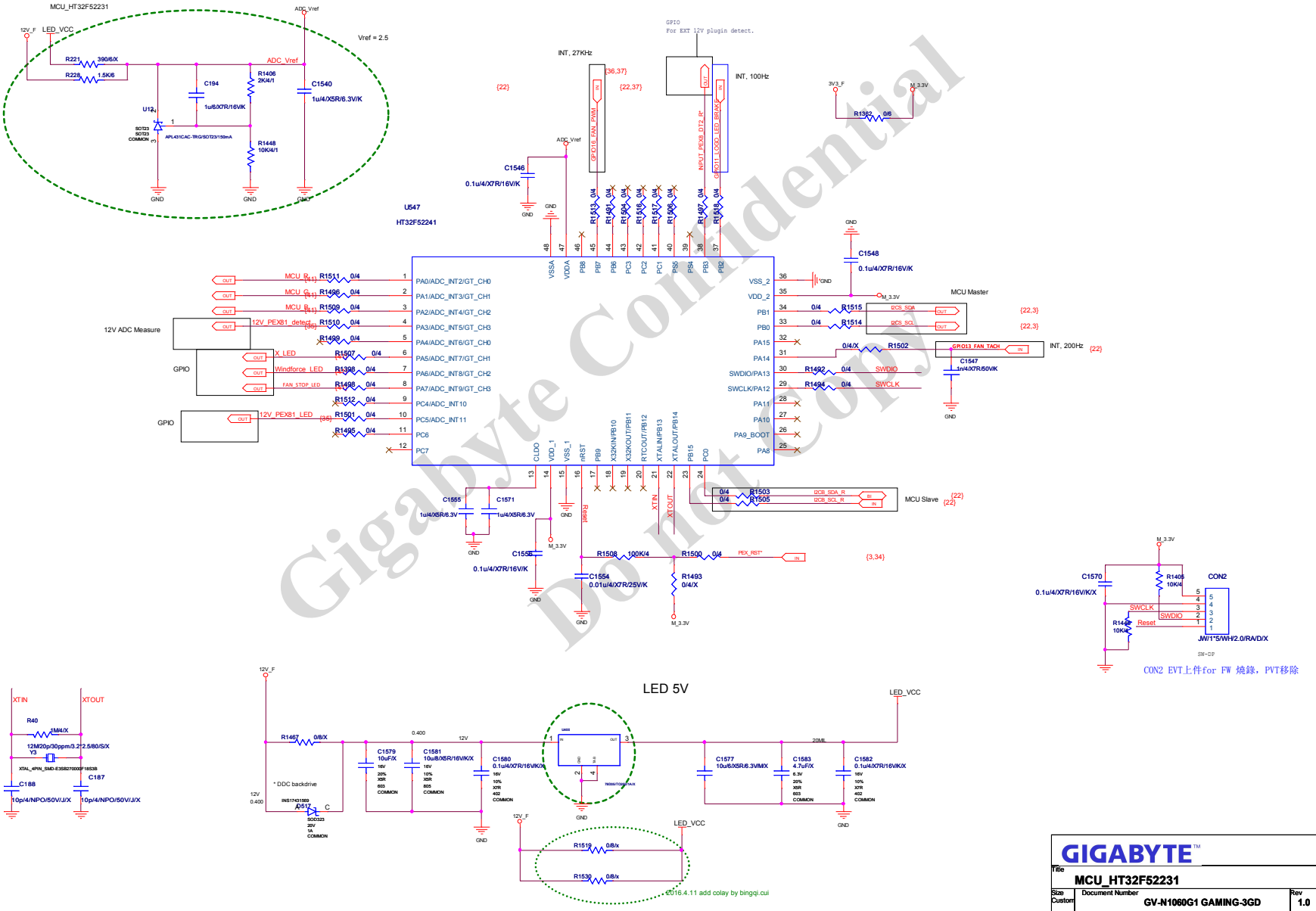
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 39 of 42	



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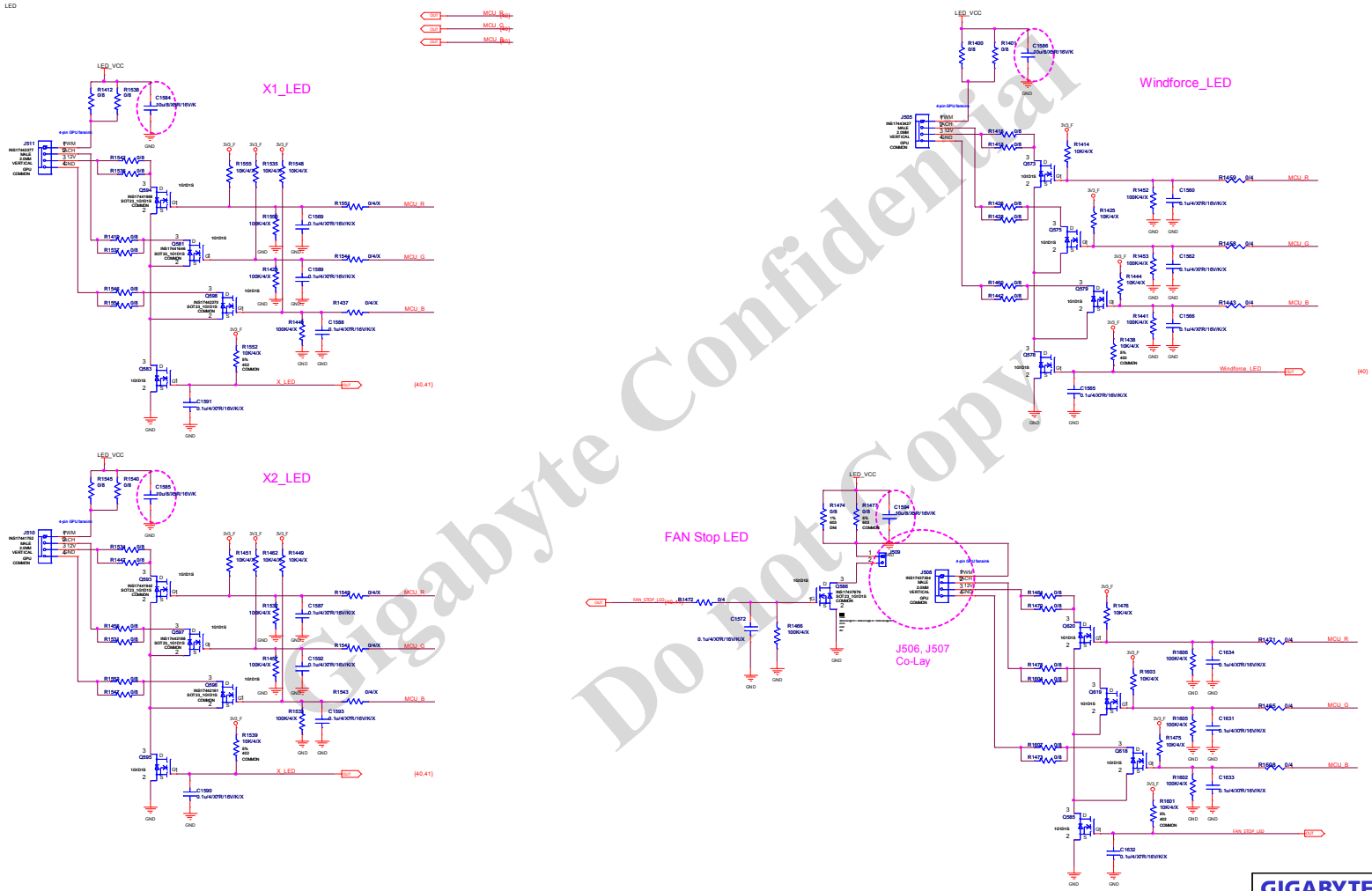
Title	MCU_HT32F52231	
Size: Custom	Document Number: GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 40 of 42	



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BASE LEVEL GENERIC SCHEMATIC ONLY
MECH

History

Data	Modify
2016.04.04	First version

Title		
Size: A	Document Number: history GV-N1060G1 GAMING-3GD	Rev: 1.0
Date: Tuesday, July 19, 2016	Sheet 42 of 42	