Agassi

DTX **FAB-B**

CPU:

Intel Lynnfield/Havendale processors in LGA1156 Package

System Chipset:

PCH(Ibex Peak)

Main Memory:

Dual Channel / DDR-III * 4 (Max 16GB)

On Board Device:

Clock Generator ICS9LRS4105
Super I/O:IT8721F-CX
LAN:RTL8111E
HDA Codec:ALC662
BIOS:SPI Flash ROM(32MX2)

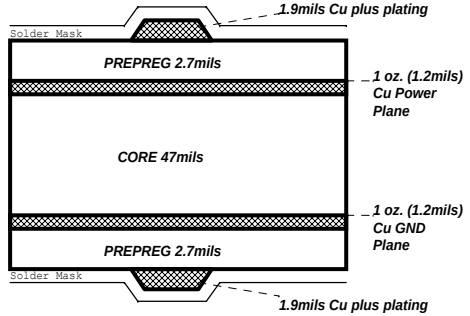
Expansion Slots:

PCI EXPRESS 16X SLOT * 1

PCI EXPRESS 1X SLOT * 1

Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4-mil trace target, ±15%
USB2.0 - 90 ohm : 17.5%
SATA - 90 ohm : 17.5%
PCIE1.1 - 80 ohm : 17.5%
DMI - 80 ohm : 17.5%
PCIE2.0 - 80 ohm : 17.5%
HDMI - 95 ohm : 17.5%

Version	Function	SKU	BOM
Fab.A			
Fab.B			

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Title: **Cover Sheet**

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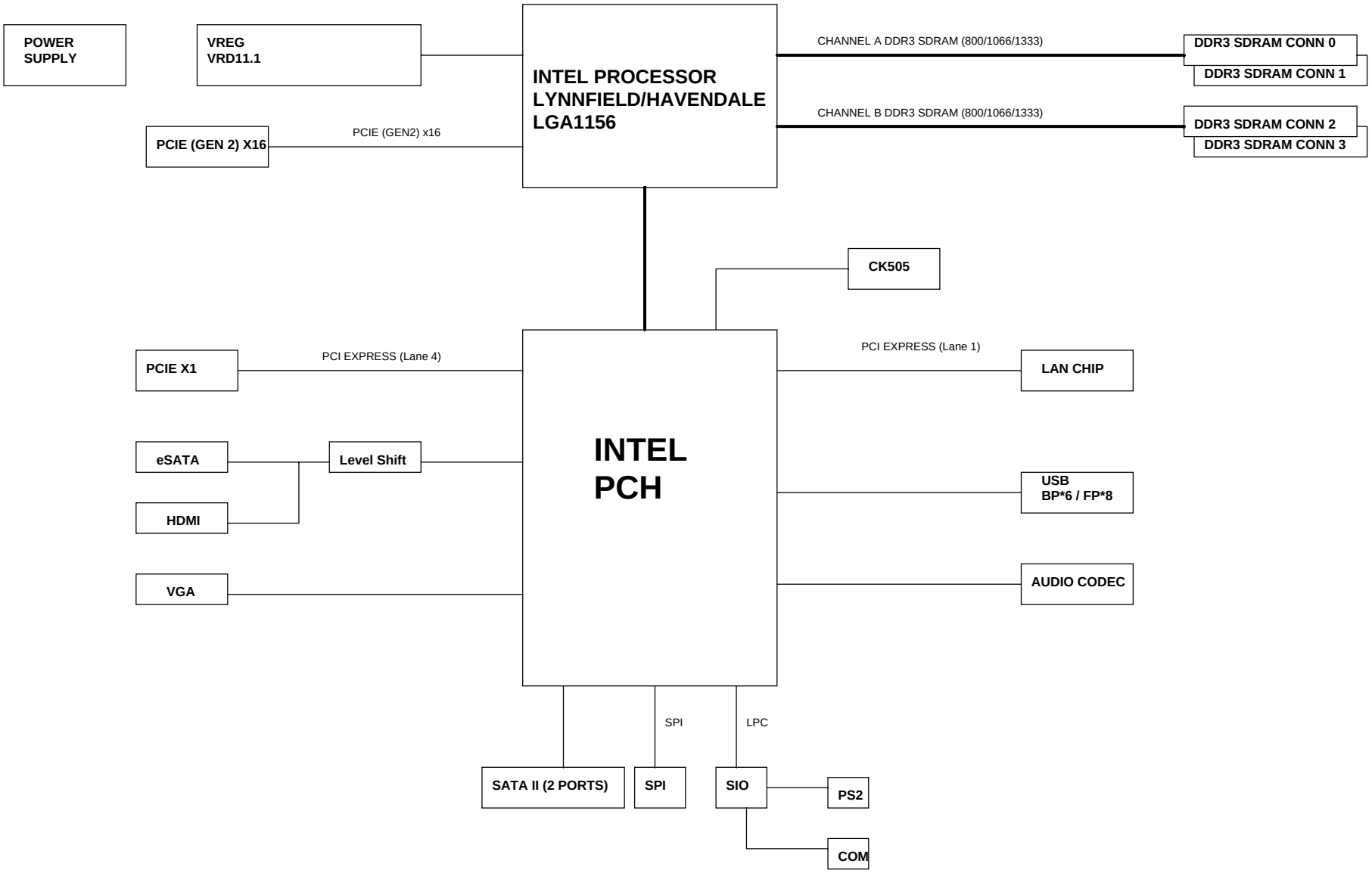
BLOCK DIAGRAM



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Title: Block Diagram		
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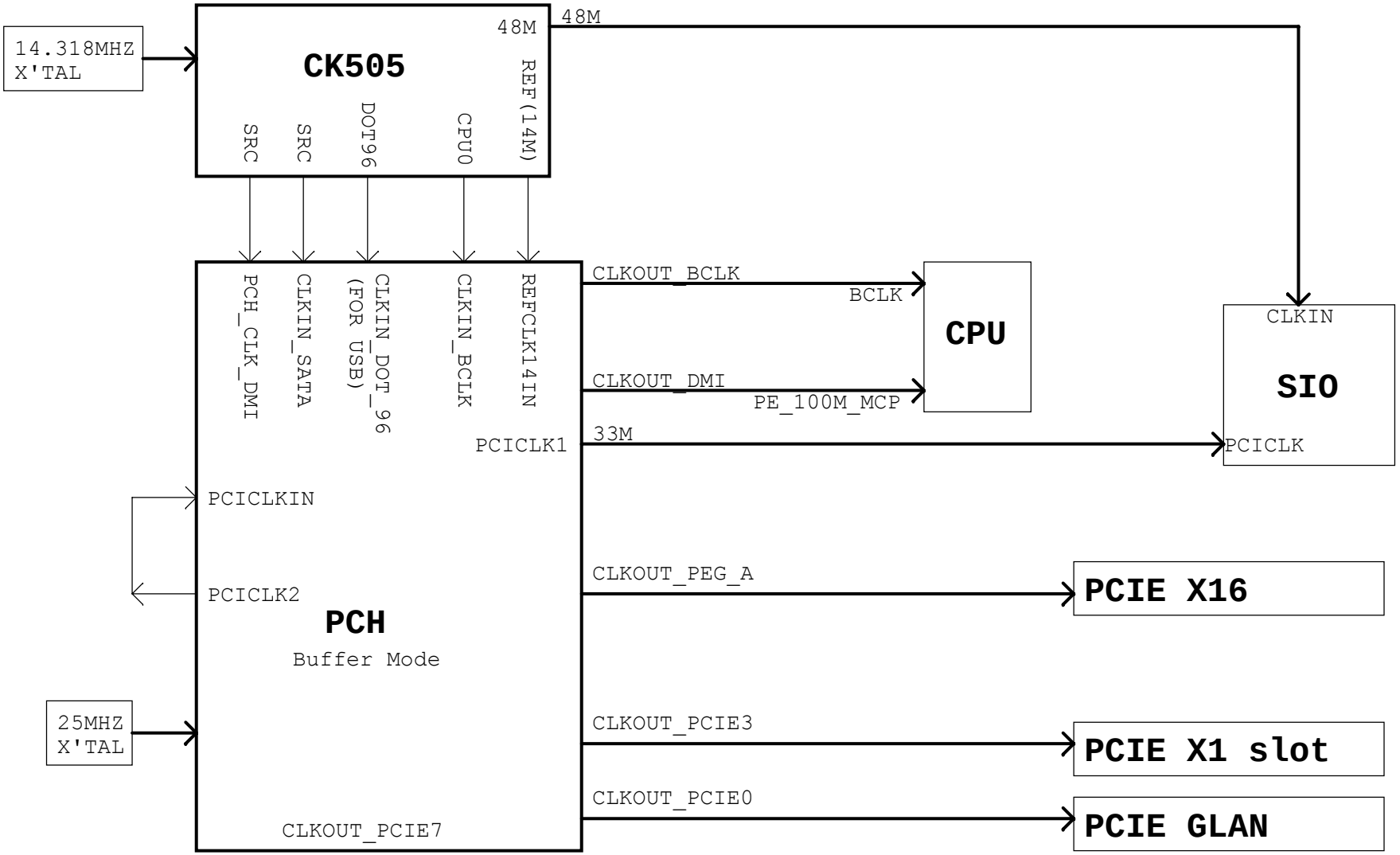
CLOCK DISTRIBUTION



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Title: Clock Distribution		
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POWER DELIVERY MAP

DDR3(4 DIMM)
V_SM=1.5V

V_SM_VTT=0.75V

SWITCHING
Icc=20A
Max=30A

V_SM(1.5V) TO
V_SM_VTT(0.75V)
Icc=1A Max=1A

12V(4PIN)

SWITCHING
Icc=90A
Max=100A

SWITCHING
Icc=16A
Max=20A

SWITCHING
Icc=30A
Max=35A

LYN/HVN(79W & 95W)
VCCP (CPU Vcore)
Voltage=1.1V
Icc=90A Max=100A
3-Phases Swithing

V_AXG(Havendale only)
Voltage=1.1V
Icc=16A Max=20A

V_SM(DDR III)
Voltage=1.5V

VTT(1.1/1.05V)

VCCPLL(1.8V)
Icc<0.8A

5VSB

5V_SB to
3.3VSB
Icc=2.874A

3.3V

PCI Express X16
+12V=4.4A

3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)

+3.3V=3A

12V

PCI Express X1
+12V=0.5A

3.3VSB
Icc(Max)=0.375A(wake)
Icc(Max)=0.02A(no wake)

+3.3V=3A

RTL8111E
3.3V_LAN
18mA

1.8V ANALOG 181mA

1.2VR 284mA

3.3V

LAN DUAL

BJT

12V

HDA Codec
+5VA
Voltage=5V
Icc=200mA

VCC
Voltage=3.3V
Icc=40mA

12V TO +5VA
Icc=200mA

3.3V

IBEX PEAK(5.5W)
VCCCORE(V_1P05_PCH)
Voltage=1.05V
Icc(Max)=7.5A

V_SM(1.5V)
to 1.05V
Icc=5A
Max=7.A

5VSB(5V)
to 1.05V
Icc=2.5A
Max=2.5A

5VSB

3.3V

3.3V TO
V_IP8V_SFR
Icc=1.5A
Imax=1.5A

VCCME(V_1P05_ME)
Voltage=1.05V
Icc(Max)=2.5A

VCCDMI 0.065A

V_CPU_IO <1mA

VCCPNAND=1.8V 0.156A

3.3V_AUX 0.168A

3.3V 0.357A

VCCME(V_3P3_EPW)
0.086A

RTC
Battery

VCCRTC 0.002A

Super I/O
5V
Icc=50mA

5VSB
Icc=50mA(S0)

5VSB
Icc=38mA(S3)

PS2
+5V DUAL=345mA(S0, S1)
+5V DUAL=2mA(S3)

USB2.0 14 Ports
+5V DUAL=7A(S0, S1)
+5V DUAL=?A(S3)

5V_DUAL

5V

5VSB

3.3V

CK505
Vdd (Core)
Voltage=3.3V
Ivdd=200mA

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Title: Power Delivery Map

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Figure 8-1. G3 w/RTC Loss to S4/S5 Timing Diagram

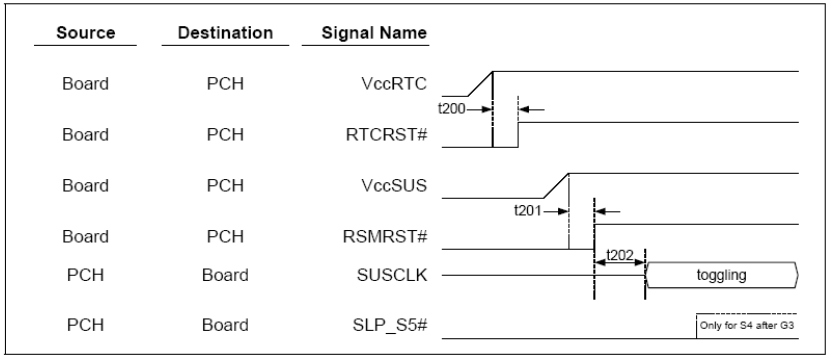


Figure 8-2. S5 to S0 Timing Diagram

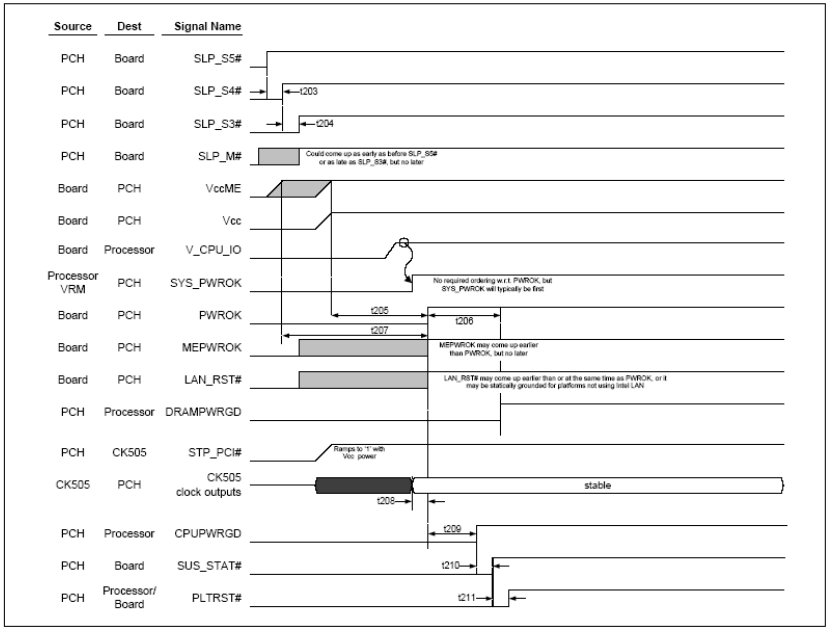


Figure 8-3. S3/M3 to S0 Timing Diagram

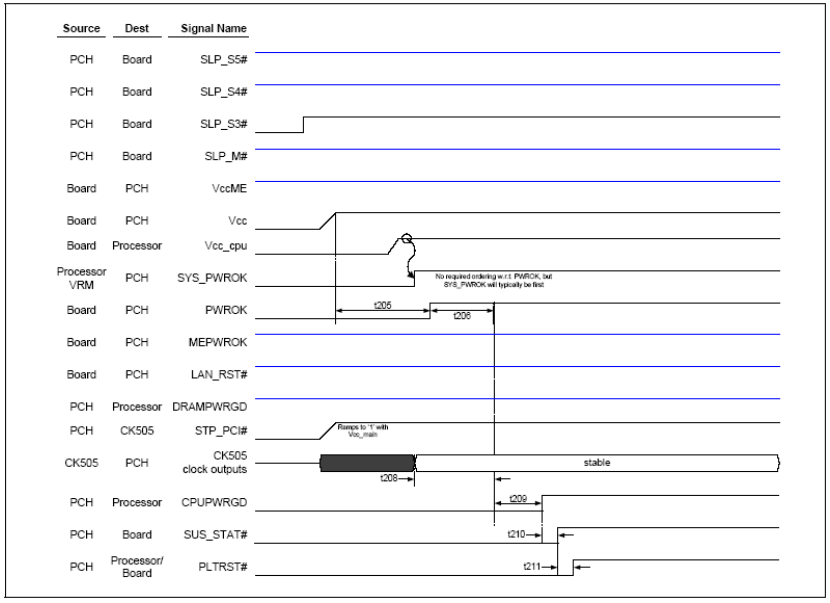


Figure 8-4. S5/Moff - S5/M3 Timing Diagram

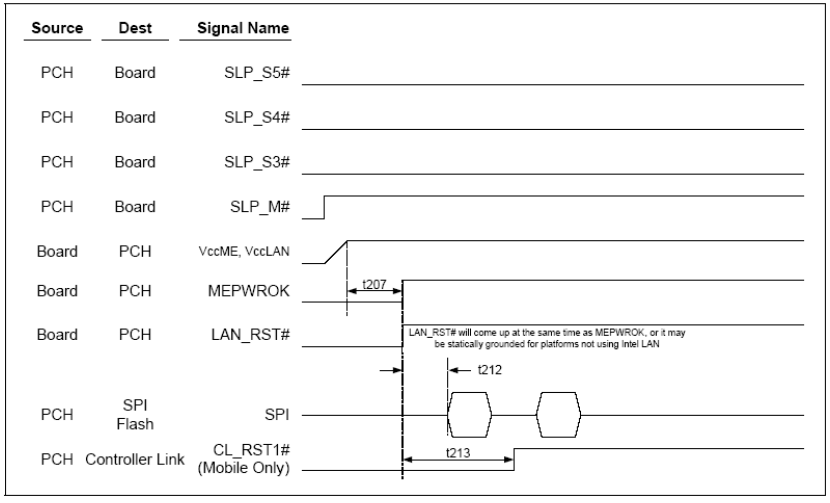
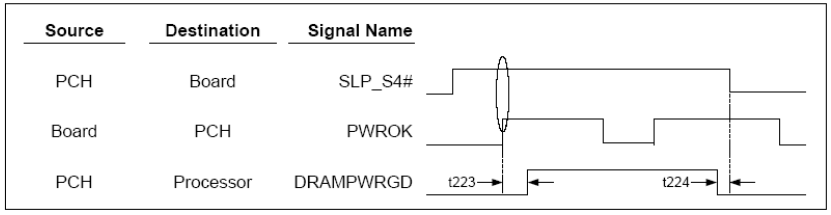


Figure 8-6. DRAMPWRGD Timing Diagram



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Title: Power On Sequence		
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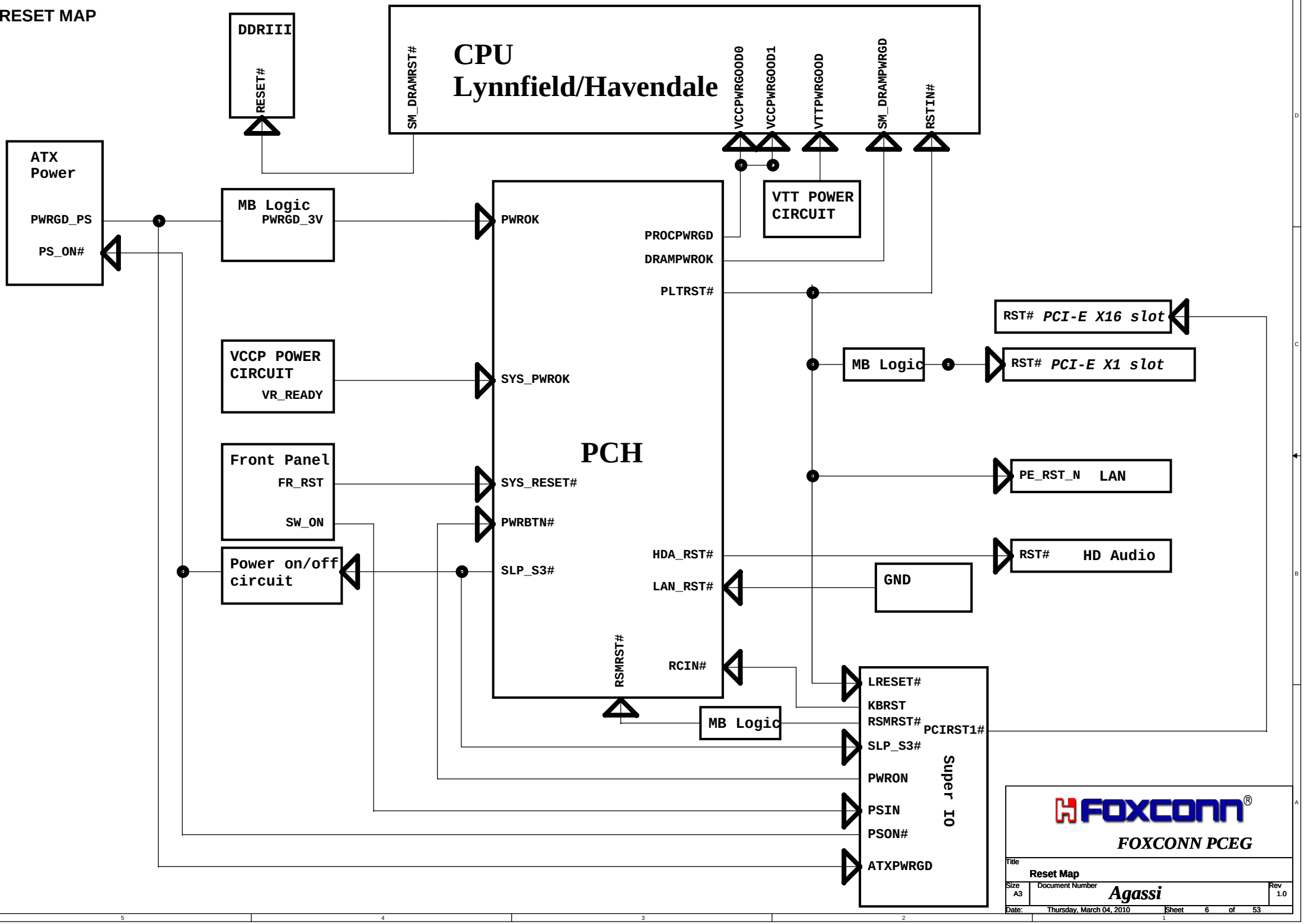
RESET MAP



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Title: Reset Map		
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PCH GPIO TABLE

PIN NAME	FUNCTION
REQ1#/GPIO50	K_PCI_REQ#1(not used) Pull up to 3.3V
GNT1#/GPIO51	Not connect
REQ2#/GPIO52	K_PCI_REQ#2(not used) Pull up to 3.3V
GNT2#/GPIO53	Not connect
REQ3#/GPIO54	K_PCI_REQ#3(not used) Pull up to 3.3V
GNT3#/GPIO55	Not connect
PIRQE#/GPIO2	K_PCI_INT_E# (not used) Pull up to 3.3V
PIRQF#/GPIO3	K_PCI_INT_F# (not used) Pull up to 3.3V
PIRQG#/GPIO4	K_PCI_INT_G# (not used) Pull up to 3.3V
PIRQH#/GPIO5	THERMAL_SHUTDOWN, Pull up to 3.3V
OC0#/GPIO59	U_USB_OC_R_#0
OC1#/GPIO40	U_USB_OC_R_#1
OC2#/GPIO41	U_USB_OC_R_#2
OC3#/GPIO42	U_USB_OC_R_#3
OC4#/GPIO43	U_USB_OC_R_#4
OC5#/GPIO9	U_USB_OC_R_#5
OC6#/GPIO10	U_USB_OC_R_#6
OC7#/GPIO14	U_USB_OC_R_#7
TACH0/GPIO17	S_PCH_CPU_FAN_TACH
TACH1/GPIO1	S_PCH_SYS_FAN_TACH1
TACH2/GPIO6	Pull up to 3.3V
TACH3/GPIO7	Pull up to 3.3V
SCLOCK/GPIO22	S_PCH_CONFIG_JUMPER(no used)PULL UP TO 1P05_PCH
SDATAOUT0/GPIO39	S_CRB_DETECT_GP39(no used) PULL UP TO 1P05_PCH
SDATAOUT1/GPIO48	S_SV_ADVANCE_GP48(no used) PULL UP TO 1P05_PCH
SLOAD/GPIO38	S_GP38_MFG_MODE#(no used) PULL UP TO 1P05_PCH
SATA0GP/GPIO21	S_SATA0GP PULL UP TO 3.3V
SATA1GP/GPIO19	S_SATA1GP PULL UP TO 3.3V
SATA2GP/GPIO36	S_CDC_DWN_DISABLE(no used)PULL UP TO 3.3V
SATA3GP/GPIO37	MCR (not used) Pull up to 3.3V
SATA4GP/GPIO16	H_SKTOCC_R_#
SATA5GP/GPIO49	S_PCH_GP49_PU PULL UP TO 3.3V
LDRQ1#/GPIO23	Not connect
SMBALERT#/GPIO11	S_SMBALERT# PULL UP TO 3.3V_AUX
SML0ALERT#/GPIO60	S_SML0ALERT PULL UP TO 3.3V_AUX
SML1ALERT#/GPIO74	S_SML1ALERT PULL UP TO 3.3V_AUX
SML1CLK/GPIO58	PULL UP TO 3.3V_AUX
SML1DATA/GP75	PULL UP TO 3.3V_AUX
BMBUSY#/GPIO0	A_FP_AUDIO_PRESENCE#
GPIO8	S_IGC_EN#
SLP_LAN#/GPIO29	SLP_LAN#
SUS_PWR_ACK/GPIO30	S_SUS_PWR_ACK PULL UP TO 3.3V_AUX
LAN_PHY_PWR_CTRL/GPIO12	LAN_DISABLE#
GPIO13	O_IO_PME#
GPIO15	S_PCH_GP15 PULL UP TO 3.3V_AUX
PCIECLKRQ1#/GPIO18	S_PCH_GP18_PU PULL UP TO 3.3V
PCIECLKRQ2#/GPIO20	S_PCH_GP20_PU PULL UP TO 3.3V
MEM_LED/GPIO24	GPIO_YLW_HDR, Pull up to 3.3V_AUX
PCIECLKRQ3#/GPIO25	S_1_WATT_CTRL_1, Pull up to 3.3V_AUX
PCIECLKRQ4#/GPIO26	S_GP26_44_45_56_PD (no used), Pull up to 3.3V_AUX
GPIO27	S_PCH_GP27 Pull up to 3.3V_AUX
GPIO28	S_PCH_GP28_PU(for XDP) PULL UP TO 3.3V_AUX
ACPRESENT/GPIO31	S_GP31_PU PULL UP TO 3.3V_AUX
GPIO32	not used (TP162)
GPIO33	S_ME_ENABLE
STP_PCI#/GPIO34	S_GP34_PU PULL UP TO 3.3V
SATACLKREQ#/GPIO35	Not used (TP78)
PCIECLKRQ5#/GPIO44	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
PCIECLKRQ6#/GPIO45	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
PCIECLKRQ7#/GPIO46	S_GP46_47_PD PULL UP TO 3.3V_AUX
PEG_A_CLKRQ#/GPIO47	S_GP46_47_PD PULL UP TO 3.3V_AUX
PEG_B_CLKRQ#/GPIO56	S_GP26_44_45_56_PD (no used) Pull up to 3.3V_AUX
GPIO57	TPM_PHY_PRESENT(no used) Pull Low
PCIECLKRQ0#/GPIO73	SPI_WP_GPIO73 PULL UP TO 3.3_AUX
SUS_ATAT#/GPIO61	RF_KILLJ, Pull up to 3.3V_AUX
SUSCLK/GPIO62	TP66
SLP_S5#/GPIO63	S_SLP_S5#
GPIO72	S_1_WATT_CTRL_2, Pull up to 3.3V_AUX
CLKOUTFLEX0/GPIO64	TP125
CLKOUTFLEX1/GPIO65	TP8
CLKOUTFLEX2/GPIO66	TP7
CLKOUTFLEX3/GPIO67	TP5

SIO GPIO TABLE

PIN NAME	FUNCTION
PSON#/GP42	PS_ON#
PANSWH#/GP43	PWRBTN#_SIO
PWRON#/GP44	S_PWRBTN#
RSMRST#/CIRRX/GP55	SIO_RSMRST#
PWROK1/GP13	SIO_PWRGD
PWROK2/GP41	R_GPIO1 Pull up to 3.3VAUX
IRRX/GP46	R_GPIO2 Pull up to 3.3VAUX
VIDO6/GP17/RI2#	SIO_BEEP
KRST#/GP62	KBRST# Pull up to 3.3V
KDAT/GP61	KBDATA
KCLK/GP60	KBCLK
MDAT/GP57	MSDATA
MCLK/GP56	MSCLK
VIN3/ATXPG	ATX_PWRGD
VID5/GP35	THERMAL_SHUTDOWN

SIO HW MONITOR

PIN NAME	FUNCTION
VIN0	VIN0_VCCP
VIN1	VIN1_1P1_VTT
VIN2	VIN2_3D3V_SYS
VIN4	VIN4_+12V_SYS
VIN5	VIN5_5V_SYS
VIN6	VIN6_5VSB_SYS
TMPIN1	TMPIN1

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Title: **GPIO/IRQ/IDSEL Table**

Size	Document Number	Rev
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HC1: Defensive min RC delay site
HR2: Divide to VTT

Follow MOW WW04,2009. Close to processor. 03/03/09

Follow Intel review result. Follow WW04 MOW. Close to processor. 02/13/09

Follow 0.8 SCH

HU1E

MISC

HVN/LYN

5/10

CFG[0..5] HAVE INTERNAL PULL-UP

CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	RSVD		PEG SEL1
2	RSVD		PEG SEL2
3	NORM		
4	DISABLE	REVERSAL	PEG LANE REVERSAL
5	RSVD	ENABLE	DP PRESENCE
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		

PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1X16
1	1	0	2X8

PLACE NEAR POWER CONTROLLER

DEFENSIVE PULL UP SITES follow CRB 1.1 FAB B

NEAR CPU

NEAR XDP_CONN

	FUNCTION	DEFAULT
VID0	MSI0	
VID1	MSI1	
VID2	MSI2	
VID3	IMON_CONFIG0	
VID4	IMON_CONFIG1	
VID5	IMON_CONFIG2	
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

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Title: CPU-1:MISC

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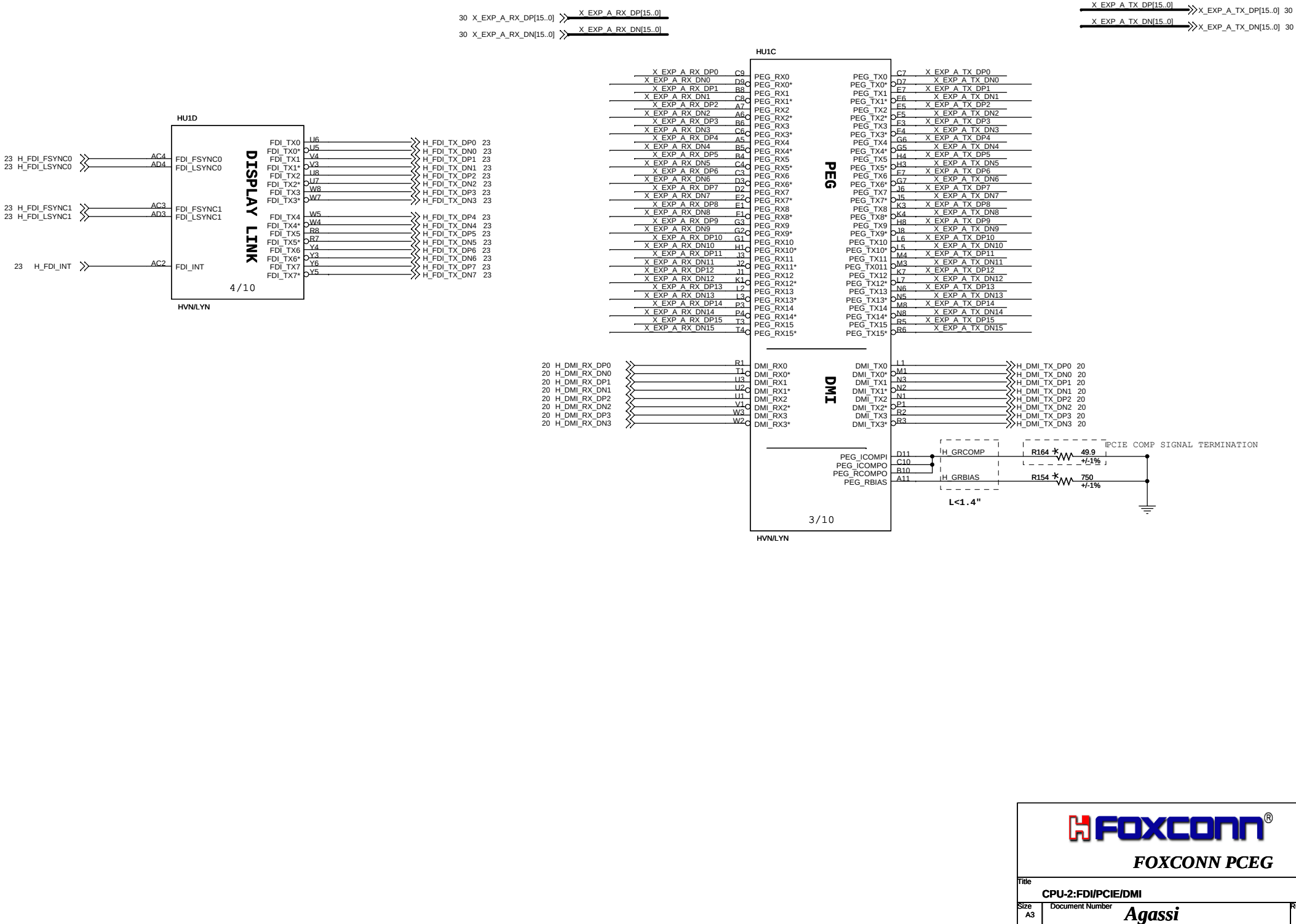

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Title: CPU-2:FDI/PCIE/DMI		
Size: A3	Document Number: Agassi	Rev: 1.0
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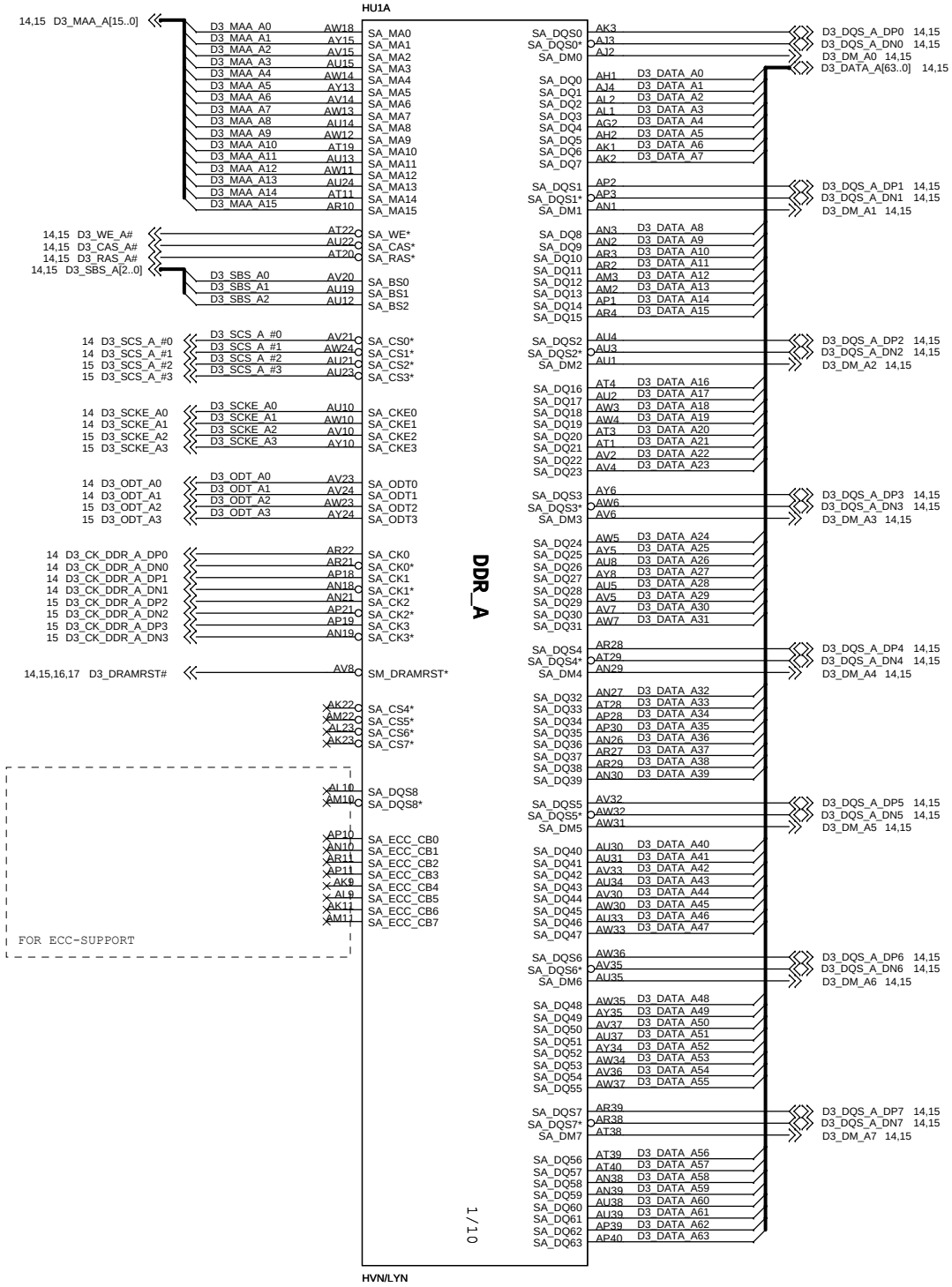

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Size: A3	Document Number: *Agassi*	Rev: 1.0
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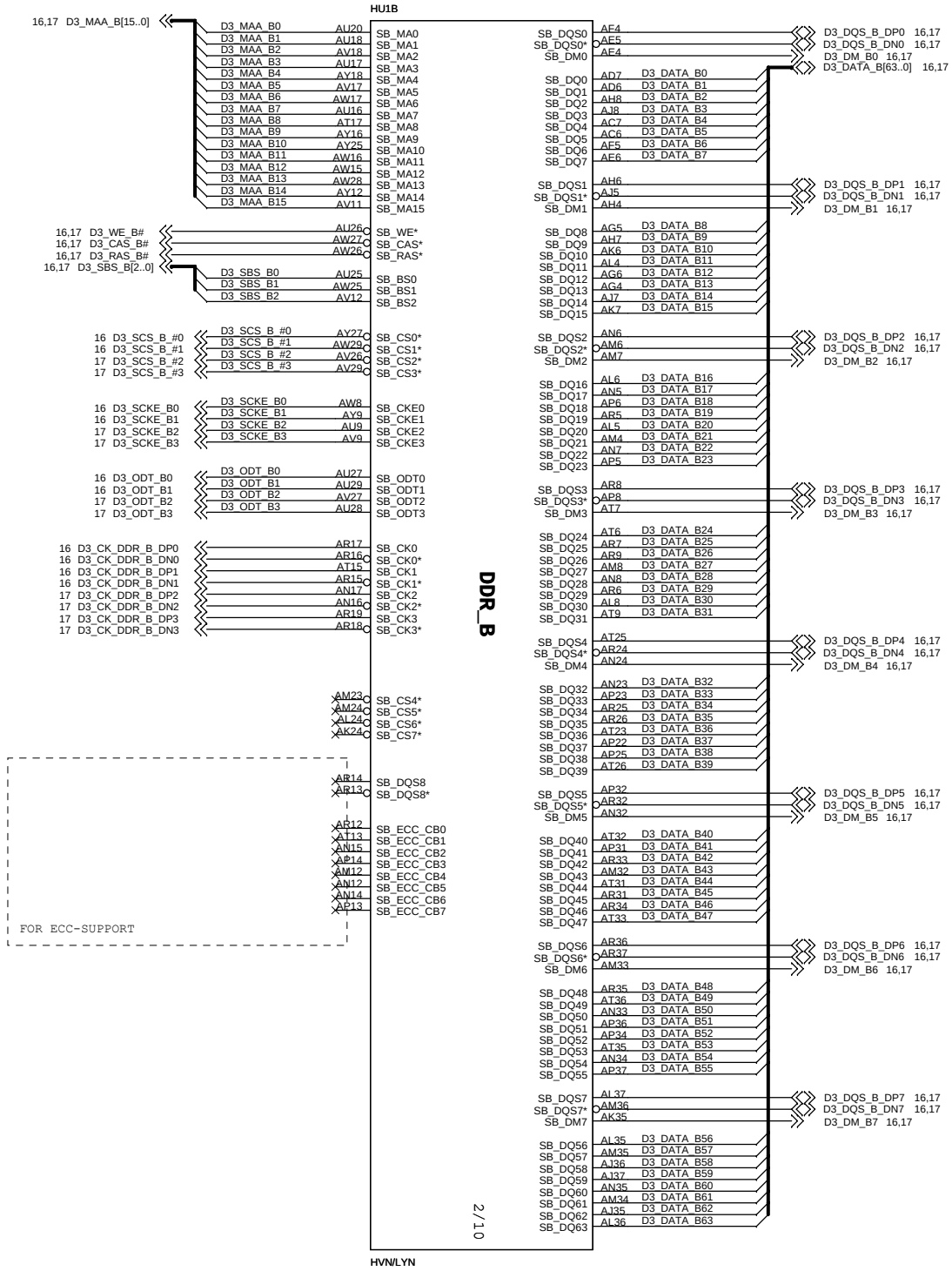

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Size: A3	Document Number: Agassi	Rev: 1.0
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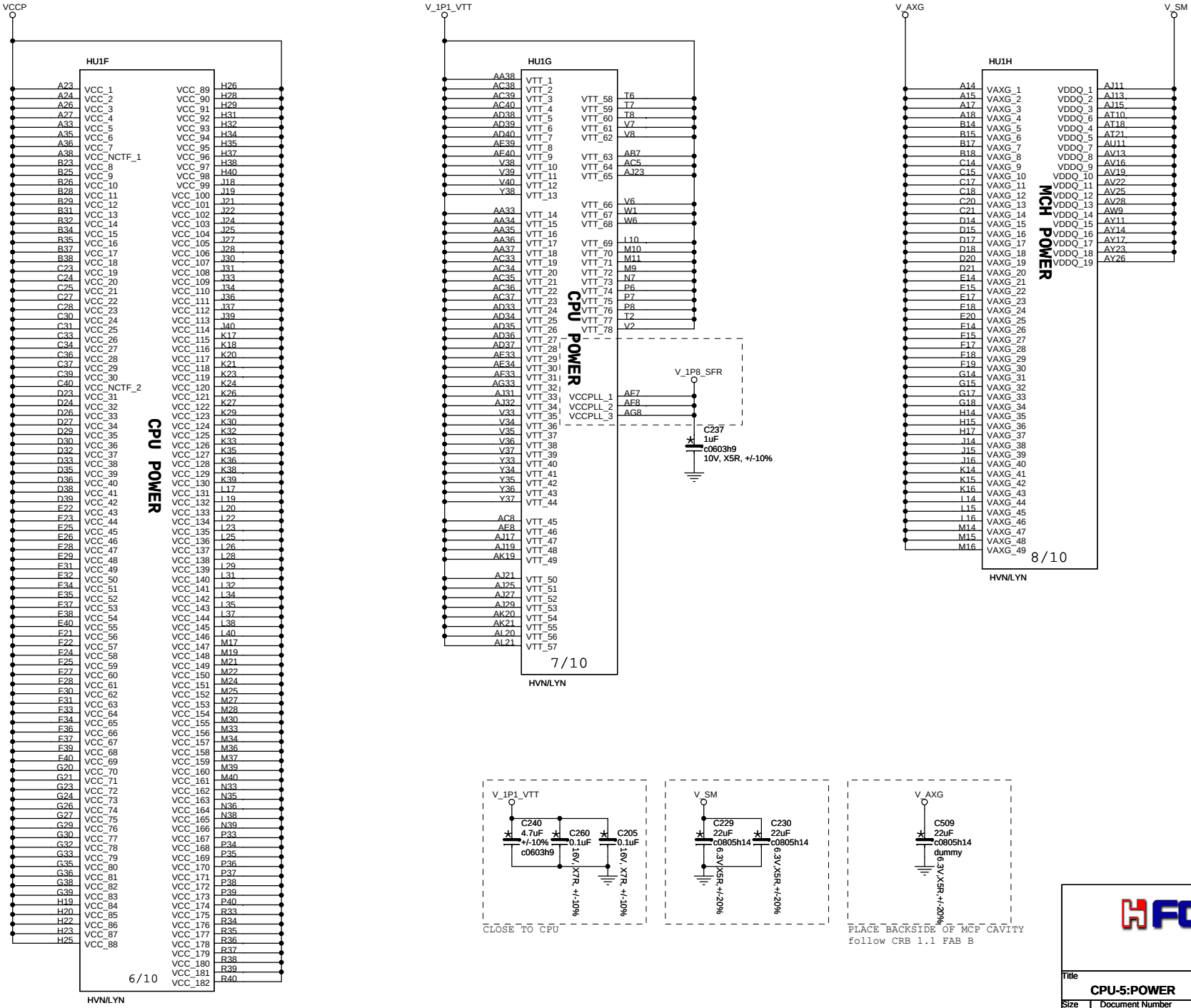

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Title: CPU-5:POWER		
Size: A3	Document Number: *Agassi*	Rev: 1.0
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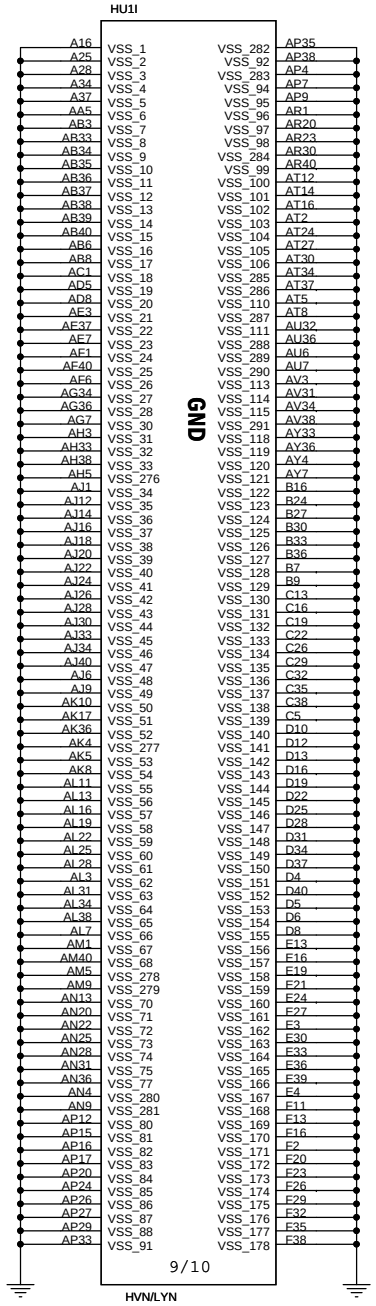

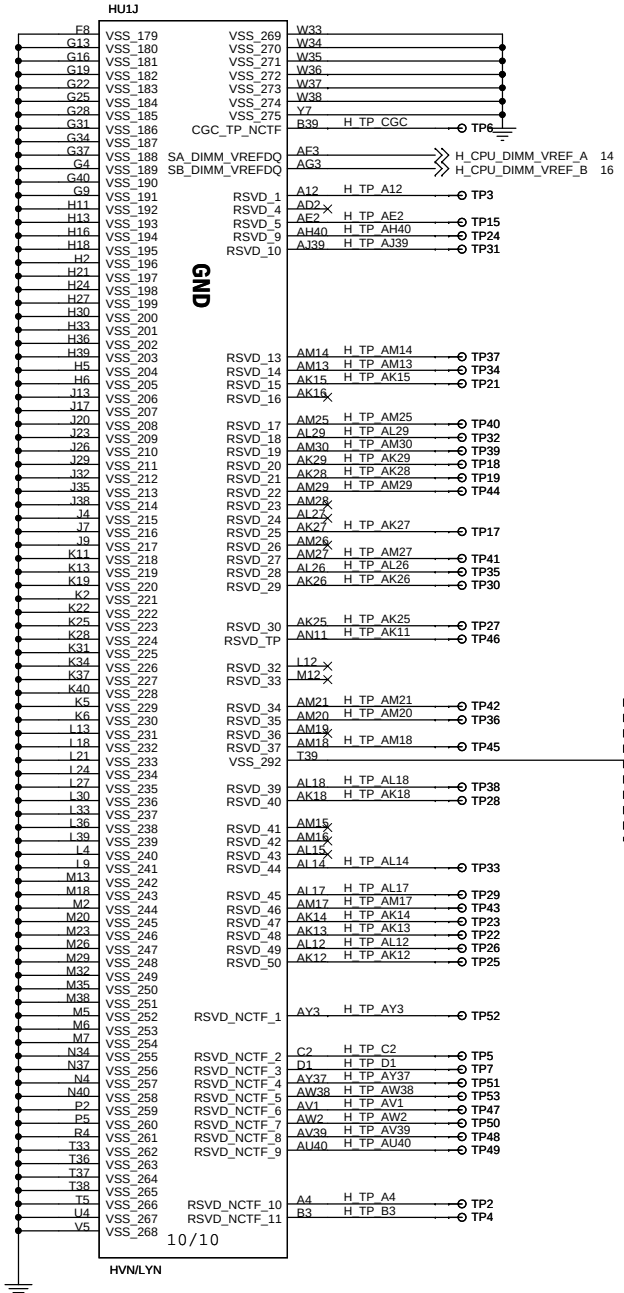

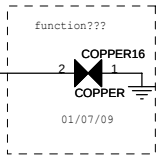

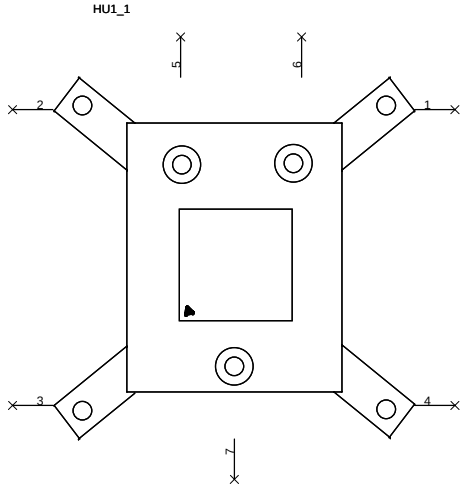

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Title

CPU-6:GND

Size	Document Number	Rev
A3	*Agassi*	1.0

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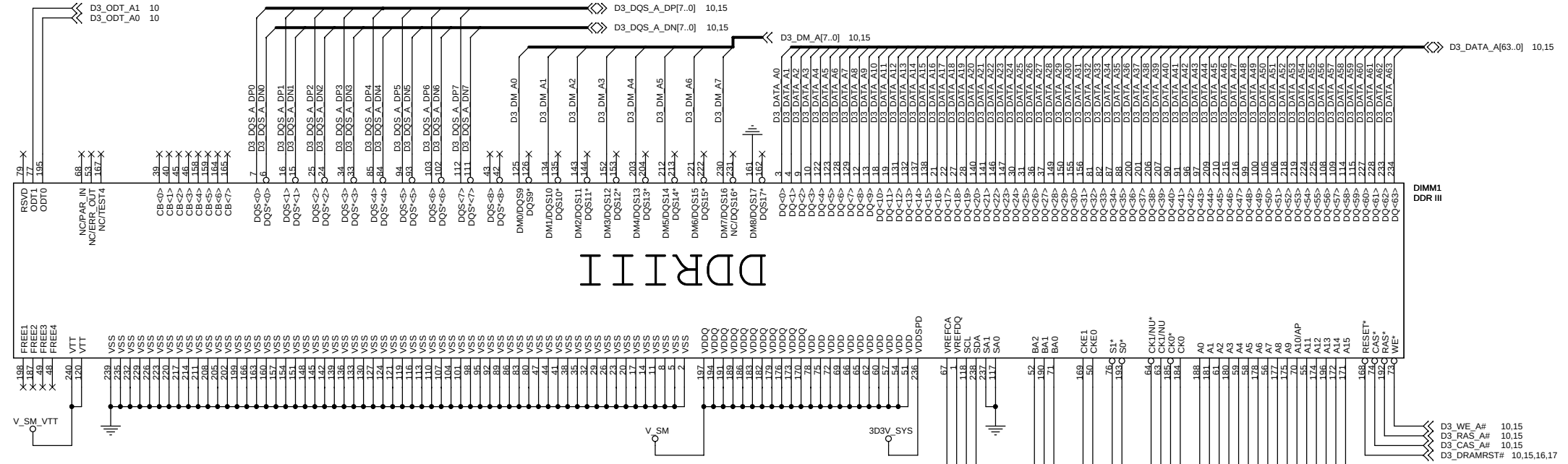
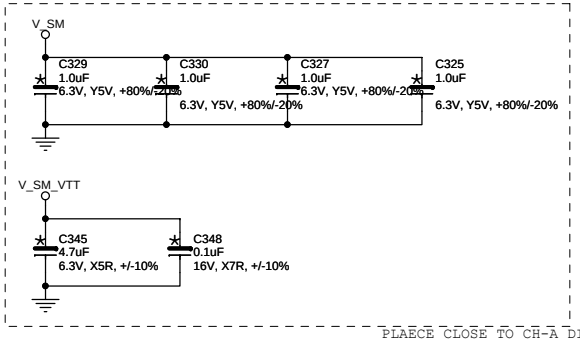
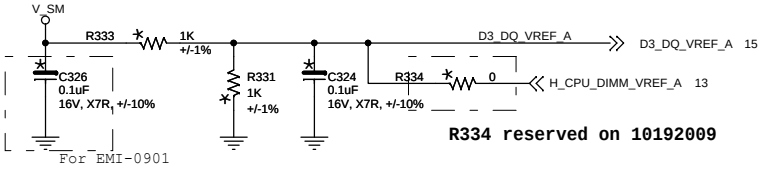
CHANNEL A BANK 1
SMB ADDRESS:000



CLOSE TO DIMM POWER PIN



PLAECE CLOSE TO CH-A DIMM



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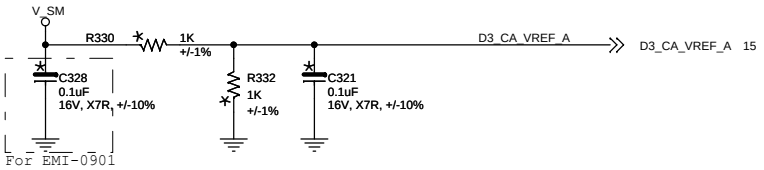

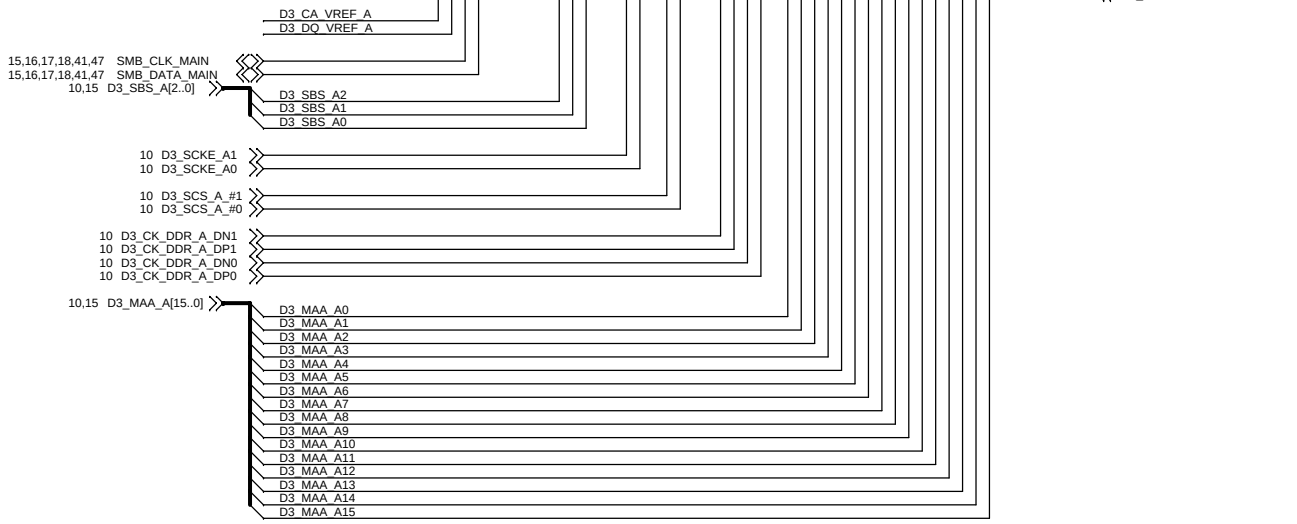

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Title
DDR3-1:CHA_1

Size	Document Number	Rev
A3	*Agassi*	1.0

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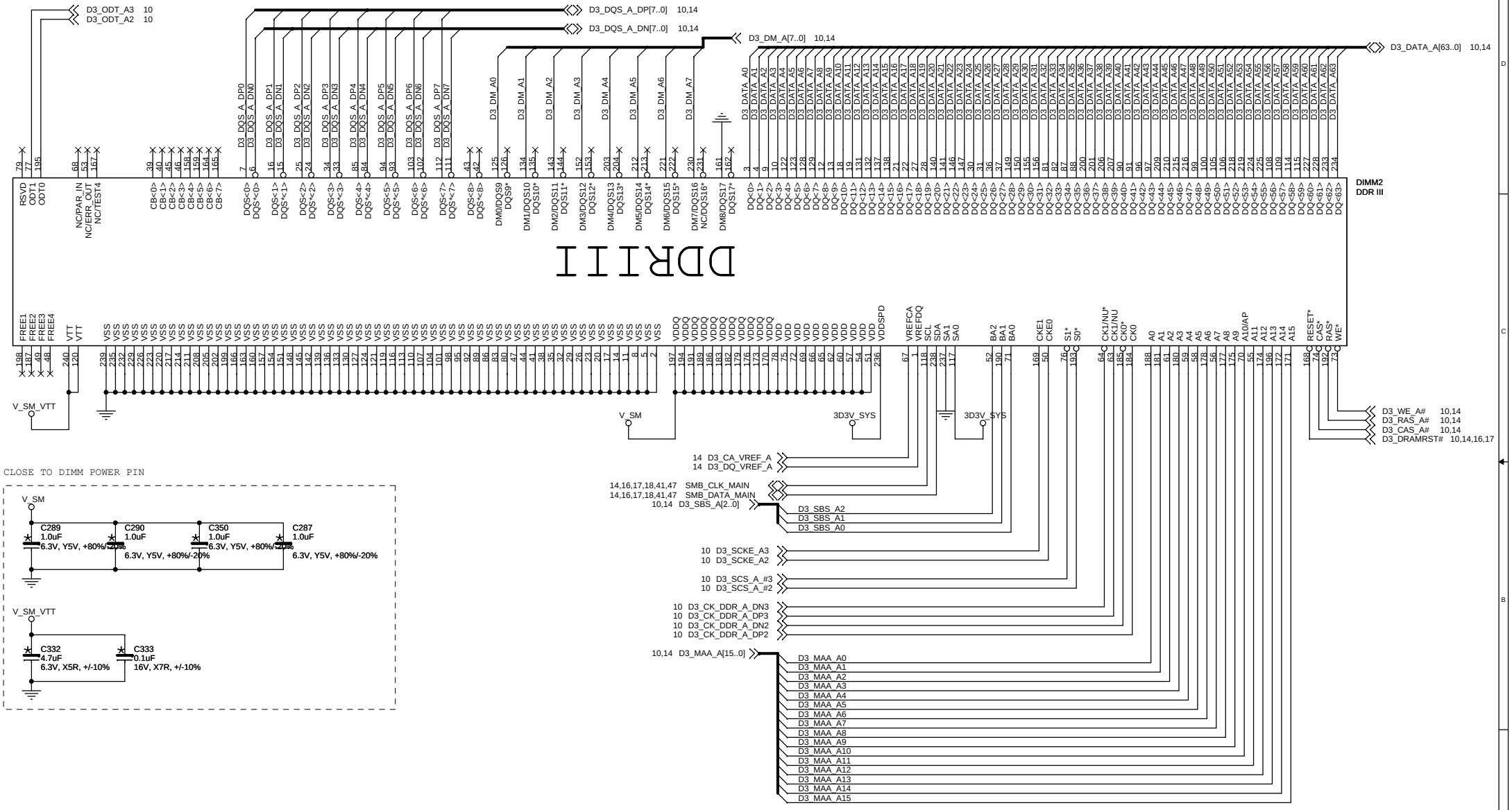
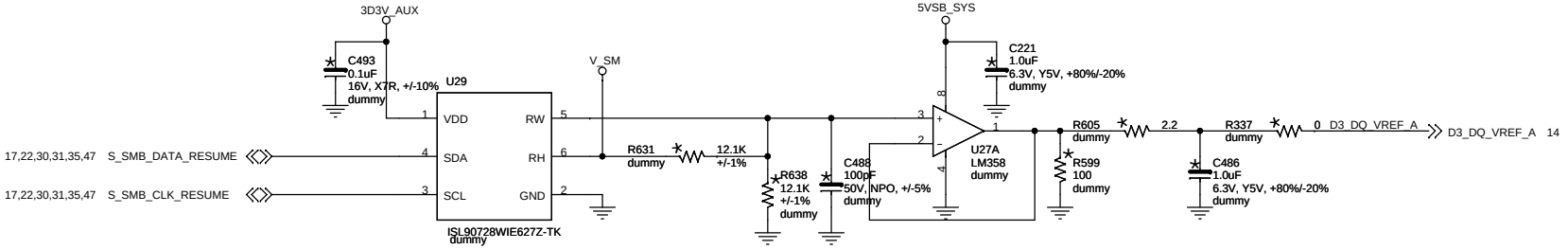
CHANNEL A BANK 2
SMB ADDRESS:001



CLOSE TO DIMM POWER PIN



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Title	DDR3-2:CHA_2	
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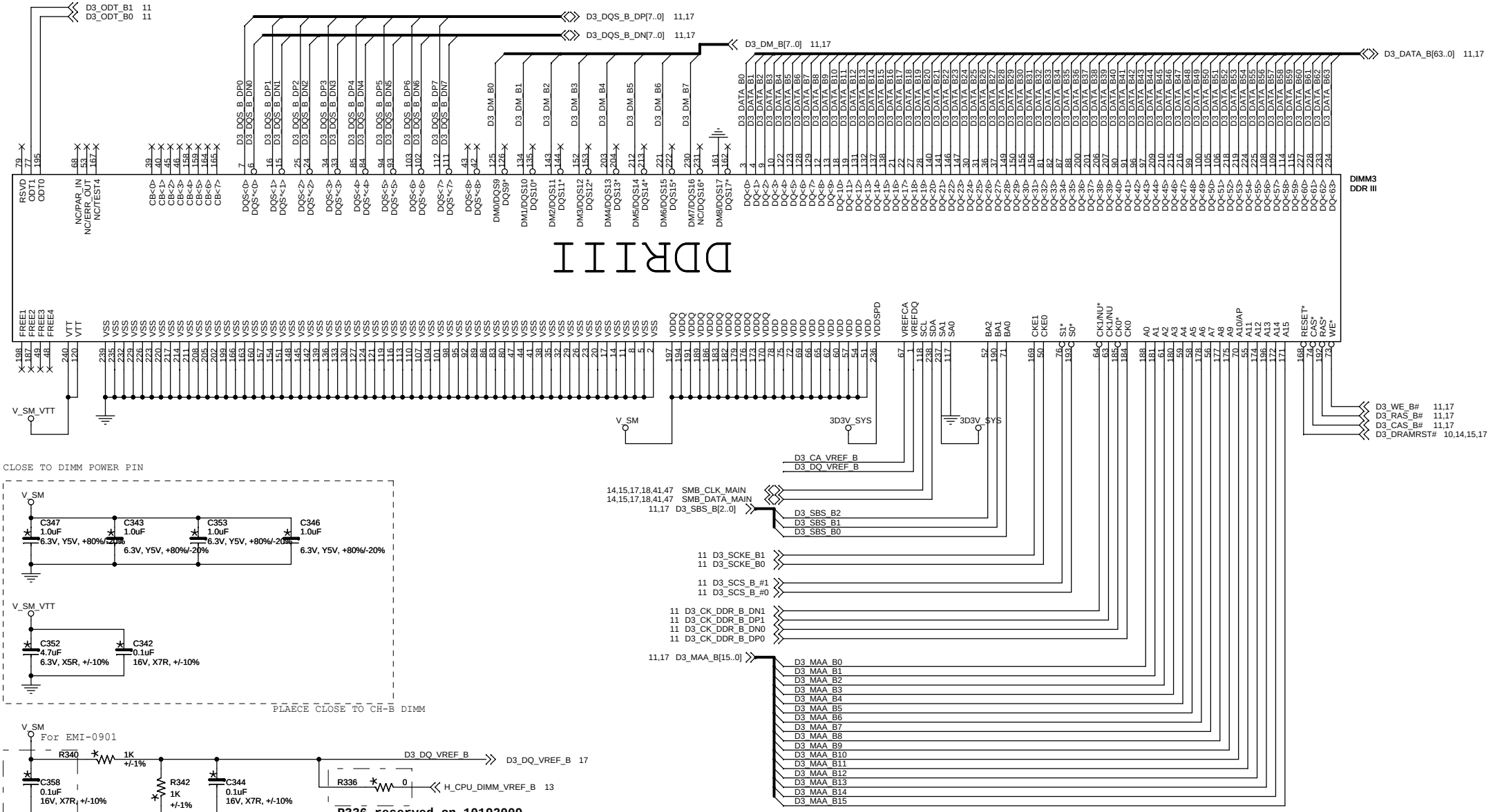
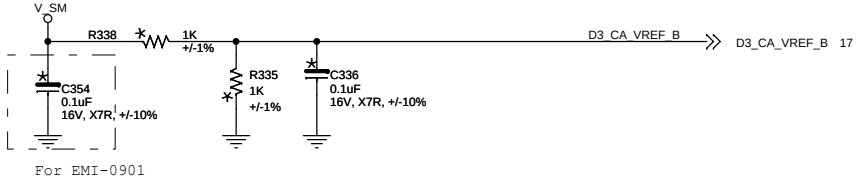
CHANNEL B BANK 1
SMB ADDRESS:010



CLOSE TO DIMM POWER PIN

PLAECE CLOSE TO CH-B DIMM



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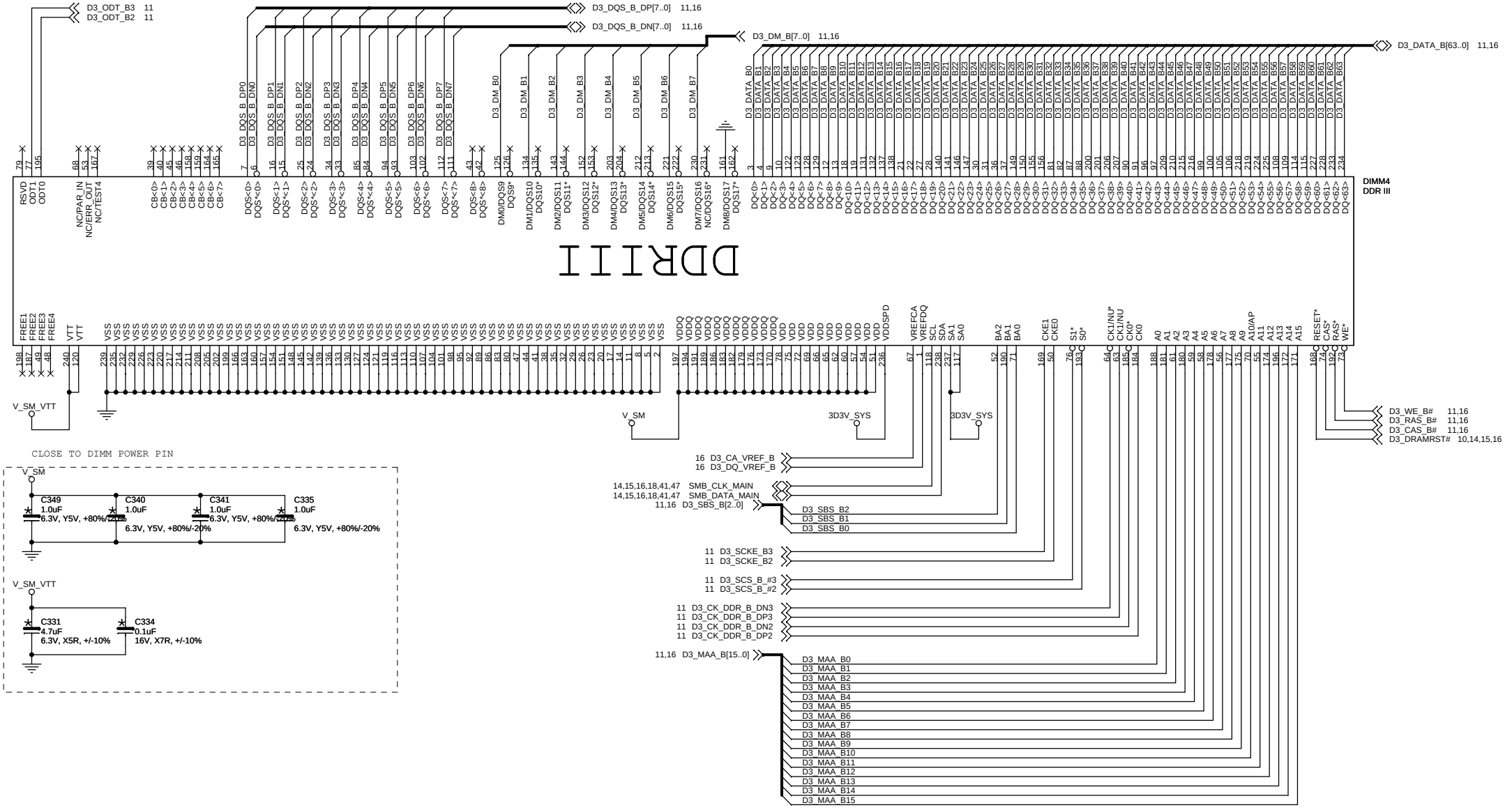
Title: DDR3-3:CHB_1		
Size: A3	Document Number: Agassi	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 16 of 53	

CHANNEL B BANK 2
SMB ADDRESS:011



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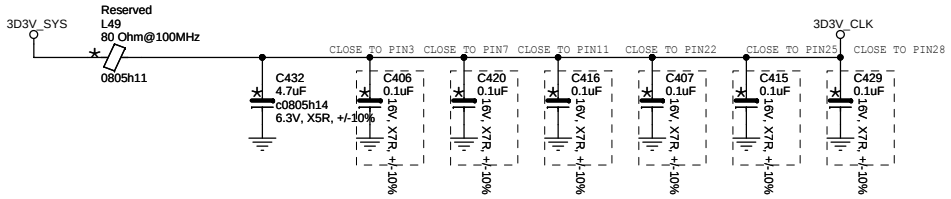
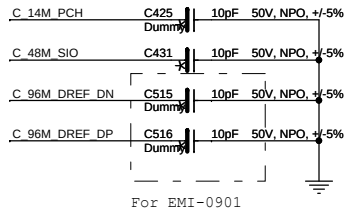
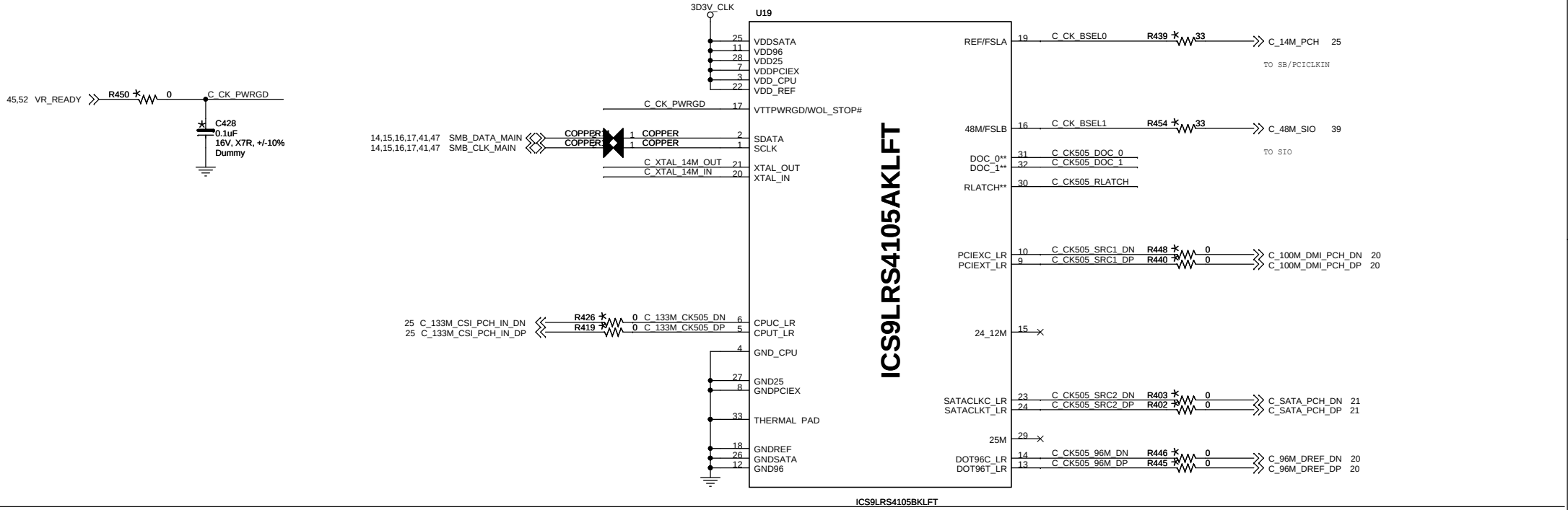
Title	DDR3-4:CHB_2	
Size A3	Document Number *Agassi*	Rev 1.0
Date: Thursday, March 04, 2010	Sheet 17 of 53	



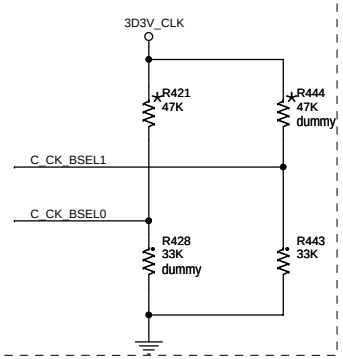
for EMI

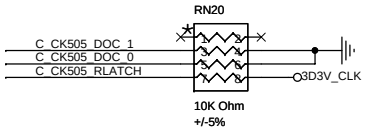


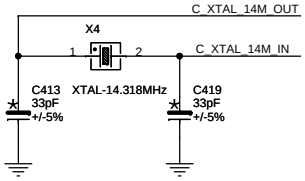


ICS9LRS4105BKLFT

FREQ	BSEL0	BSEL1
100	1	1
133	1	0







Ce = 2 * 20 pF - 7 pF = 40 pF - 7 pf = 33 pF

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Title: **CLOCK GEN**

Size	Document Number	Rev
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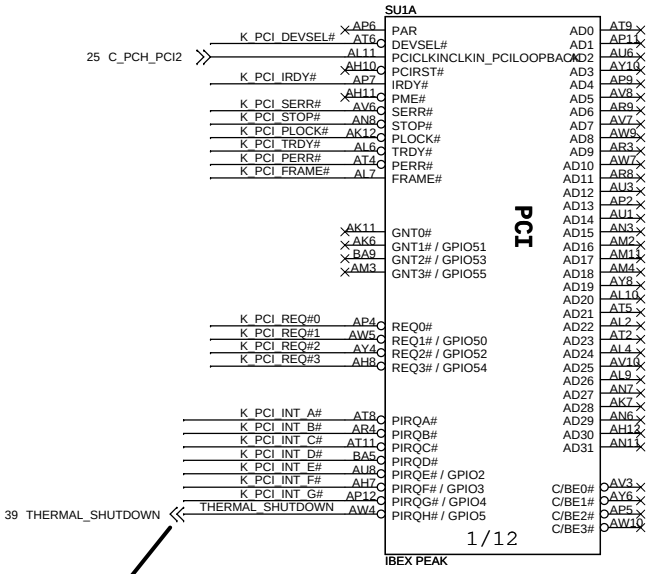
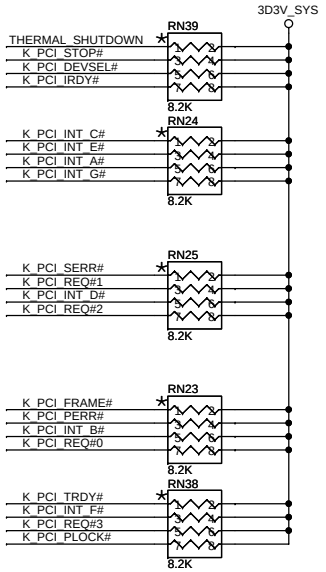
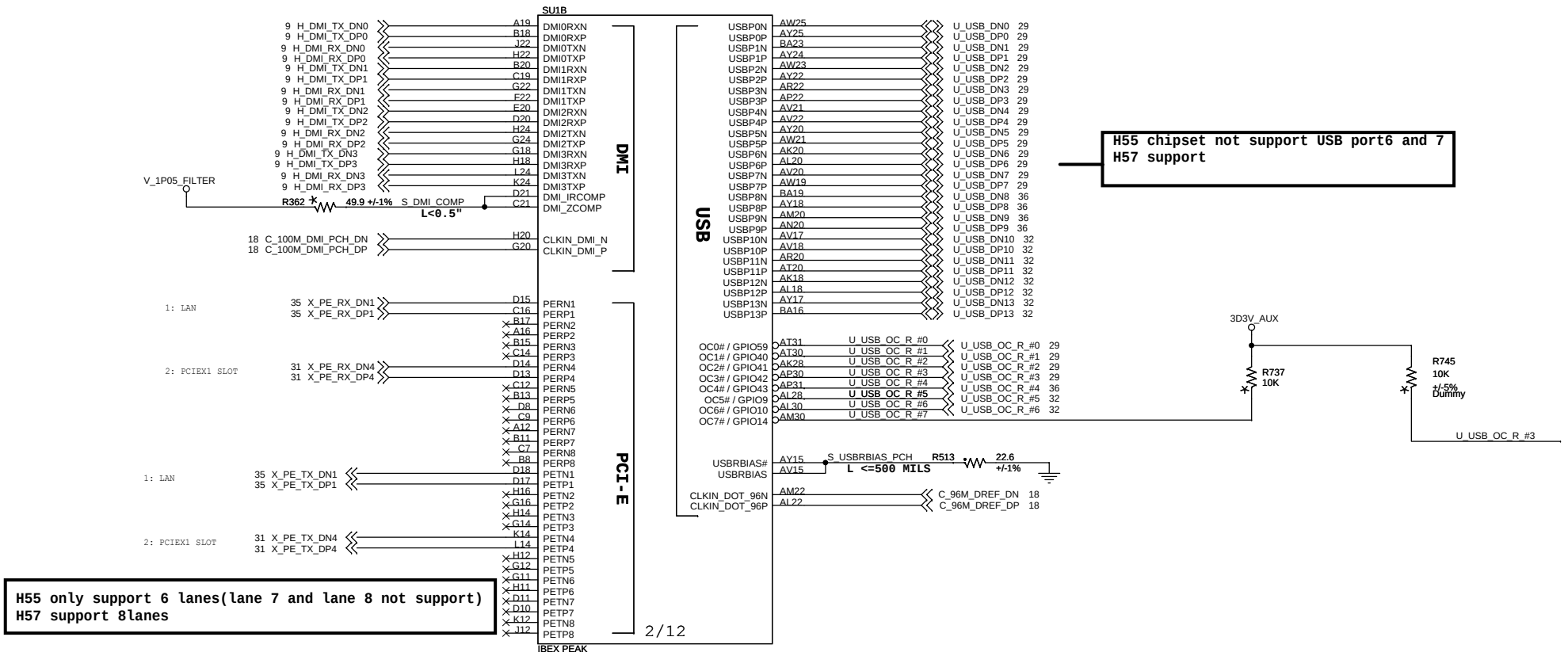


THERMAL_SHUTDOWN need to be GPIO0~15 of IBEX PEAK



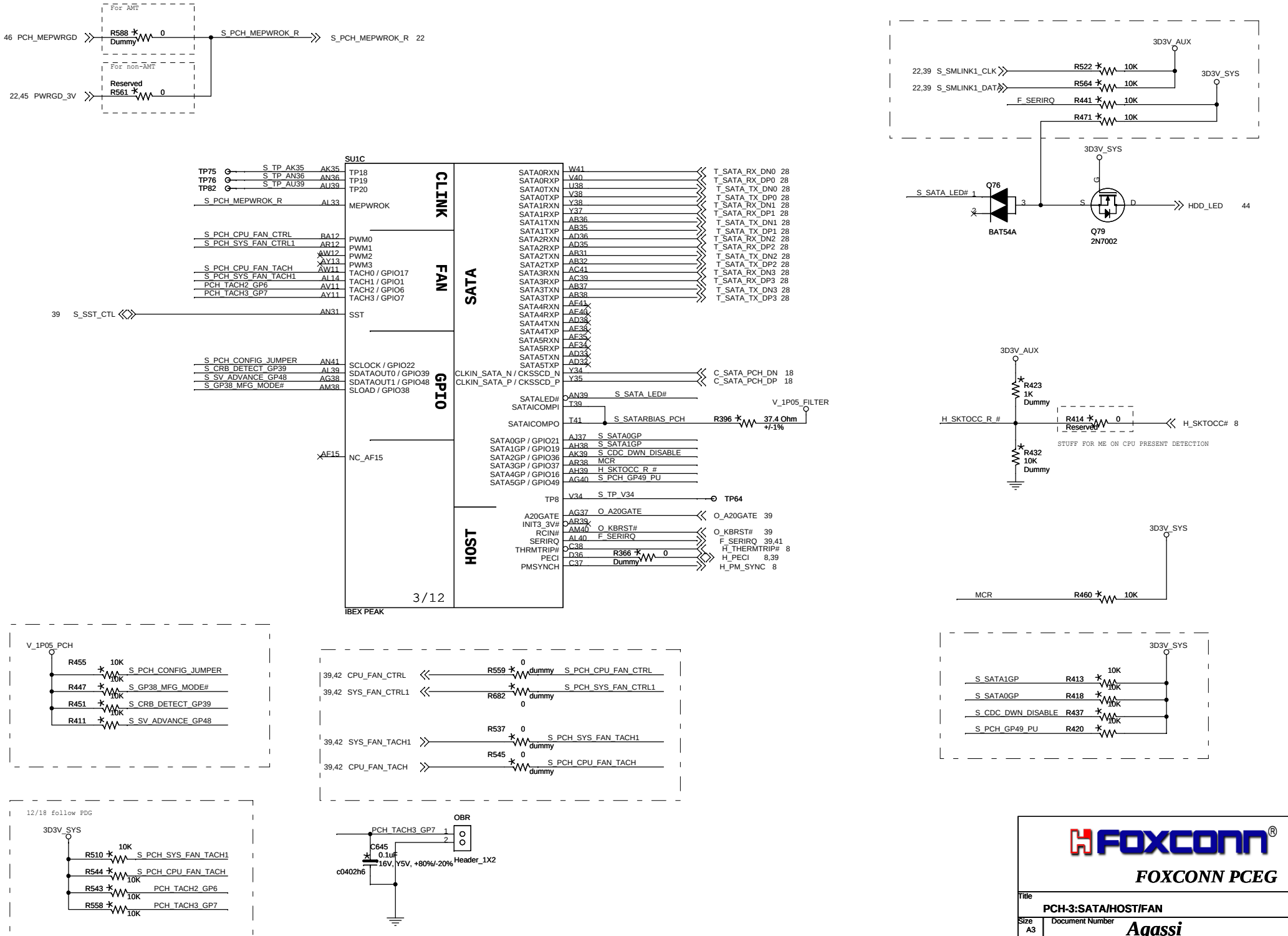
FOXCONN PCEG

Title: PCH-1:PCI		
Size: A3	Document Number: Agassi	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 19 of 53	



FOXCONN PCEG

Title: PCH-2:DMI/PCIE/USB		
Size: A3	Document Number: Agassi	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 20 of 53	



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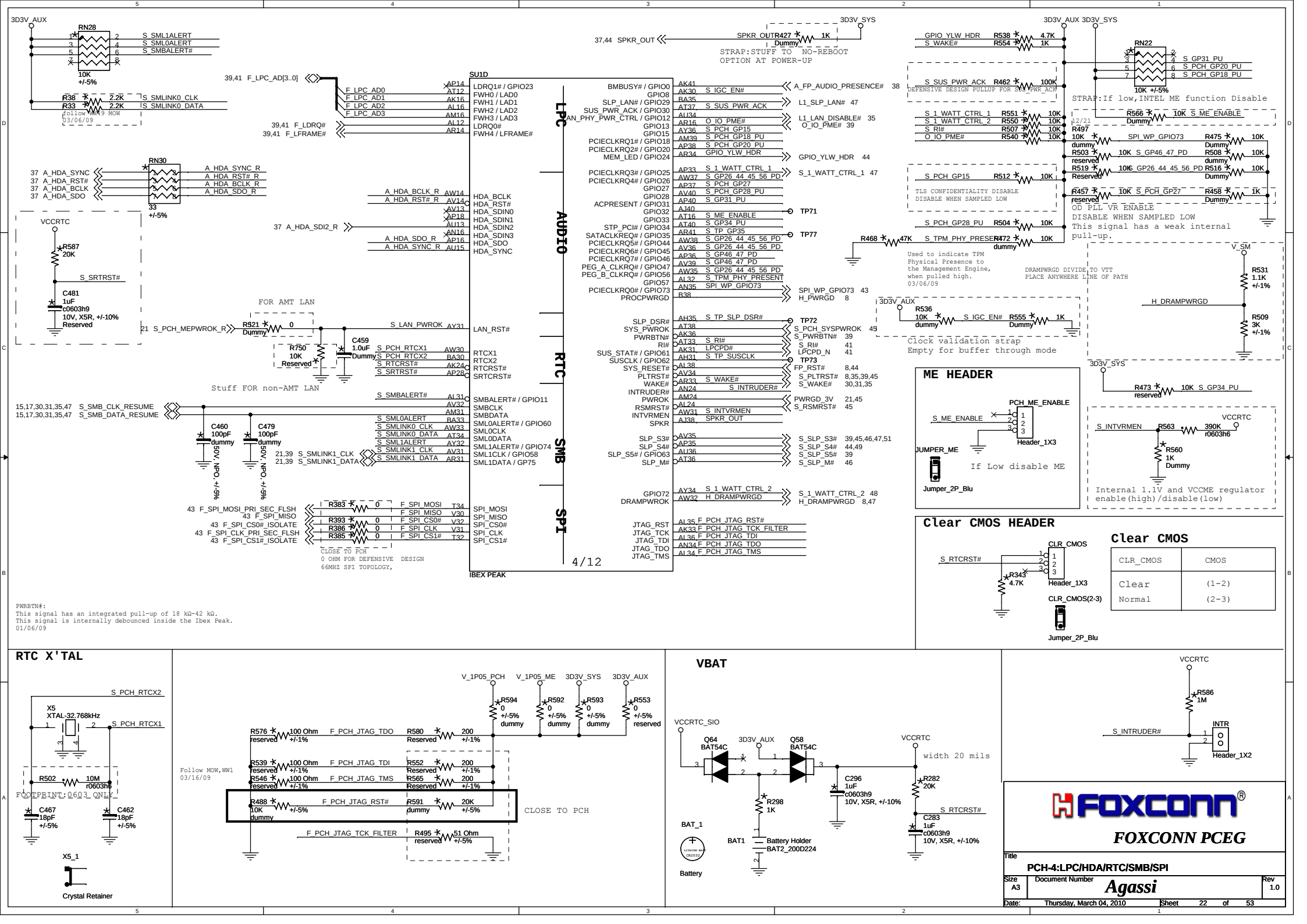
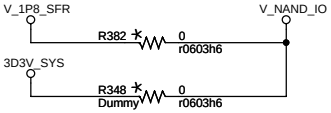
FOXCONN PCEG

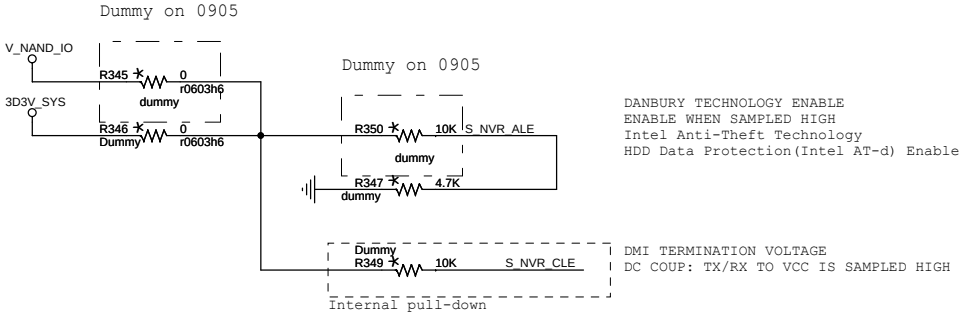
Title: PCH-3:SATA/HOST/FAN

Size	Document Number	Rev
A3	Agassi	1.0

Date: Thursday, March 04, 2010 Sheet 21 of 53

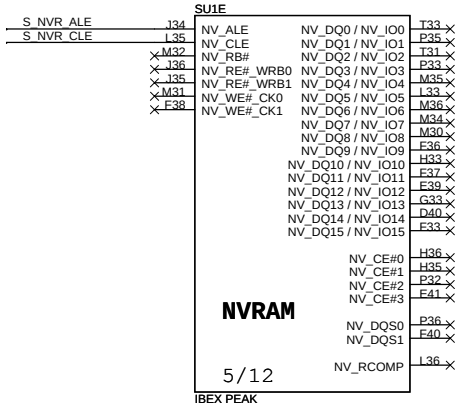

3D3V_AUX
RN28
S_SML1ALERT
S_SML0ALERT
S_SMBALERT#
10K +/-5%
R38 2.2K S_SMLINK0_CLK
R33 2.2K S_SMLINK0_DATA
Follow MOW 9 MOW 03/06/09
39,41 F_LPC_AD[3..0]
F_LPC_AD0
F_LPC_AD1
F_LPC_AD2
F_LPC_AD3
39,41 F_LDRQ#
39,41 F_LFRAME#
SU1D
LDRQ1# / GPIO23
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
LDRQ0#
FWH4 / LFRAME#
LPC
RN30
37 A_HDA_SYNC
37 A_HDA_RST#
37 A_HDA_BCLK
37 A_HDA_SDO
A_HDA_SYNC_R
A_HDA_RST#_R
A_HDA_BCLK_R
A_HDA_SDO_R
33 +/-5%
A_HDA_BCLK_R
A_HDA_RST#_R
37 A_HDA_SDI2_R
A_HDA_SDO_R
A_HDA_SYNC_R
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC
AUDIO
VCCRTC
R587 20K
S_SRTRST#
C481 1uF c0603h9 10V, X5R, +/-10% Reserved
FOR AMT LAN
21 S_PCH_MEPWROK_R
R321 0 Dummy
S_LAN_PWROK
LAN_RST#
R750 10K Reserved
C459 1.0uF Dummy
S_PCH_RTCX1
S_PCH_RTCX2
S_RTCRST#
S_SRTRST#
RTCX1
RTCX2
RTCRST#
SRTCRST#
RTC
Stuff FOR non-AMT LAN
S_SMBALERT#
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GP75
15,17,30,31,35,47 S_SMB_CLK_RESUME
15,17,30,31,35,47 S_SMB_DATA_RESUME
S_SML0ALERT
S_SMLINK0_CLK
S_SMLINK0_DATA
S_SML1ALERT
S_SMLINK1_CLK
S_SMLINK1_DATA
C460 100pF dummy 50V, NPO, +/-5%
C479 100pF dummy 50V, NPO, +/-5%
21,39 S_SMLINK1_CLK
21,39 S_SMLINK1_DATA
SMB
43 F_SPI_MOSI_PRI_SEC_FLSH
43 F_SPI_MISO
43 F_SPI_CS0#_ISOLATE
43 F_SPI_CLK_PRI_SEC_FLSH
43 F_SPI_CS1#_ISOLATE
R383 0 F_SPI_MOSI
F_SPI_MISO
R393 0 F_SPI_CS0#
R386 0 F_SPI_CLK
R385 0 F_SPI_CS1#
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1#
SPI
CLOSE TO PCH
0 OHM FOR DEFENSIVE DESIGN
66MHZ SPI TOPOLOGY,
4/12
IBEX PEAK
BMBUSY# / GPIO0
GPIO8
SLP_LAN# / GPIO29
SUS_PWR_ACK / GPIO30
LAN_PHY_PWR_CTRL / GPIO12
GPIO13
GPIO15
PCIECLKRQ1# / GPIO18
PCIECLKRQ2# / GPIO20
MEM_LED / GPIO24
PCIECLKRQ3# / GPIO25
PCIECLKRQ4# / GPIO26
GPIO27
GPIO28
ACPRESENT / GPIO31
GPIO32
GPIO33
STP_PCI# / GPIO34
SATACLKREQ# / GPIO35
PCIECLKRQ5# / GPIO44
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
PEG_A_CLKRQ# / GPIO47
PEG_B_CLKRQ# / GPIO56
GPIO57
PCIECLKRQ0# / GPIO73
PROCPWRGD
SLP_DSR#
SYS_PWROK
PWRBTN#
RI#
SUS_STAT# / GPIO61
SUSCLK / GPIO62
SYS_RESET#
PLTRST#
WAKE#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
SPKR
SLP_S3#
SLP_S4#
SLP_S5# / GPIO63
SLP_M#
GPIO72
DRAMPWROK
JTAG_RST
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
A_FP_AUDIO_PRESENCE# 38
L1_SLP_LAN# 47
L1_LAN_DISABLE# 35
O_IO_PME# 39
GPIO_YLW_HDR 44
S_1_WATT_CTRL_1 47
TP71
TP77
SPI_WP_GPIO73 43
H_PWRGD 8
TP72
S_PCH_SYSPWROK 45
S_PWRBTN# 39
S_RI# 41
LPCPD_N 41
TP73
FP_RST# 8,44
S_PLTRST# 8,35,39,45
S_WAKE# 30,31,35
PWRGD_3V 21,45
S_RSMRST# 45
S_SLP_S3# 39,45,46,47,51
S_SLP_S4# 44,49
S_SLP_S5# 39
S_SLP_M# 46
S_1_WATT_CTRL_2 48
H_DRAMPWRGD 8,47
F_PCH_JTAG_RST#
F_PCH_JTAG_TCK_FILTER
F_PCH_JTAG_TDI
F_PCH_JTAG_TDO
F_PCH_JTAG_TMS
37,44 SPKR_OUT
SPKR_OUT
R427 1K Dummy
3D3V_SYS
STRAP:STUFF TO NO-REBOOT OPTION AT POWER-UP
GPIO_YLW_HDR R538 4.7K
S_WAKE# R554 1K
S_SUS_PWR_ACK R462 100K
DEFENSIVE DESIGN PULLUP FOR SUS_PWR_ACK
S_1_WATT_CTRL_1 R551 10K
S_1_WATT_CTRL_2 R550 10K
S_RI# R507 10K
O_IO_PME# R540 10K
S_PCH_GP15 R512 10K
TLS CONFIDENTIALITY DISABLE
DISABLE WHEN SAMPLED LOW
S_PCH_GP28_PU R504 10K
R468 47K S_TPM_PHY_PRESENT R472 10K dummy
Used to indicate TPM Physical Presence to the Management Engine, when pulled high.
03/06/09
3D3V_AUX 3D3V_SYS
RN22
S_GP31_PU
S_PCH_GP20_PU
S_PCH_GP18_PU
10K +/-5%
STRAP:If low,INTEL ME function Disable
R566 10K S_ME_ENABLE Dummy
12/21
R497 10K dummy
SPI_WP_GPIO73 R475 10K Dummy
R503 10K reserved
S_GP46_47_PD R508 10K dummy
R519 10K Reserved
S_GP26_44_45_56_PD R516 10K Dummy
R457 10K reserved
S_PCH_GP27 R458 1K Dummy
OD PLL VR ENABLE
DISABLE WHEN SAMPLED LOW
This signal has a weak internal pull-up.
DRAMPWRGD DIVIDE TO VTT
PLACE ANYWHERE LINE OF PATH
V_SM
R531 1.1K +/-1%
H_DRAMPWRGD
R509 3K +/-1%
3D3V_AUX
R536 10K dummy
S_IGC_EN#
R555 Dummy 1K
Clock validation strap
Empty for buffer through mode
3D3V_SYS
R473 10K S_GP34_PU reserved
ME HEADER
PCH_ME_ENABLE
S_ME_ENABLE
JUMPER_ME
Header_1X3
If Low disable ME
Jumper_2P_Blu
VCCRTC
S_INTVRMEN
R563 390K r0603h6
R560 1K Dummy
Internal 1.1V and VCCME regulator enable(high)/disable(low)
Clear CMOS HEADER
CLR_CMOS
S_RTCRST#
R343 4.7K
Header_1X3
CLR_CMOS(2-3)
Jumper_2P_Blu
Clear CMOS
CLR_CMOS | CMOS
Clear (1-2)
Normal (2-3)
PWRBTN#:
This signal has an integrated pull-up of 18 kΩ-42 kΩ.
This signal is internally debounced inside the Ibex Peak.
01/06/09
RTC X'TAL
S_PCH_RTCX2
X5
XTAL-32.768kHz
S_PCH_RTCX1
R502 10M r0603h6
FOOTPRINT:0603 ONLY
C467 18pF +/-5%
C462 18pF +/-5%
X5_1
Crystal Retainer
V_1P05_PCH
V_1P05_ME
3D3V_SYS
3D3V_AUX
R594 0 +/-5% dummy
R592 0 +/-5% dummy
R593 0 +/-5% dummy
R553 0 +/-5% reserved
R576 100 Ohm +/-1% reserved
F_PCH_JTAG_TDO
R580 200 Reserved +/-1%
R539 100 Ohm +/-1% reserved
F_PCH_JTAG_TDI
R552 200 Reserved +/-1%
R546 100 Ohm +/-1% reserved
F_PCH_JTAG_TMS
R565 200 Reserved +/-1%
Follow MOW,WW1 03/16/09
R488 10K +/-5% dummy
F_PCH_JTAG_RST#
R591 20K dummy +/-5%
CLOSE TO PCH
F_PCH_JTAG_TCK_FILTER
R495 51 Ohm reserved +/-5%
VBAT
VCCRTC_SIO
Q64 BAT54C
3D3V_AUX
Q58 BAT54C
VCCRTC
width 20 mils
C296 1uF c0603h9 10V, X5R, +/-10%
R282 20K
R298 1K
S_RTCRST#
C283 1uF c0603h9 10V, X5R, +/-10%
BAT_1
BAT1
Battery Holder
BAT2_200D224
Battery
VCCRTC
R586 1M
S_INTRUDER#
INTR
Header_1X2
FOXCONN®
FOXCONN PCEG
Title
PCH-4:LPC/HDA/RTC/SMB/SPI
Size A3
Document Number
Agassi
Rev 1.0
Date: Thursday, March 04, 2010
Sheet 22 of 53

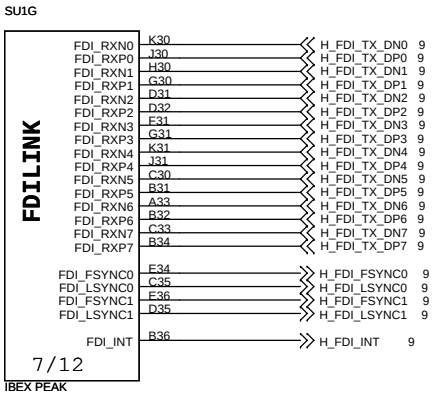




DANBURY TECHNOLOGY ENABLE
ENABLE WHEN SAMPLED HIGH
Intel Anti-Theft Technology
HDD Data Protection(Intel AT-d) Enable

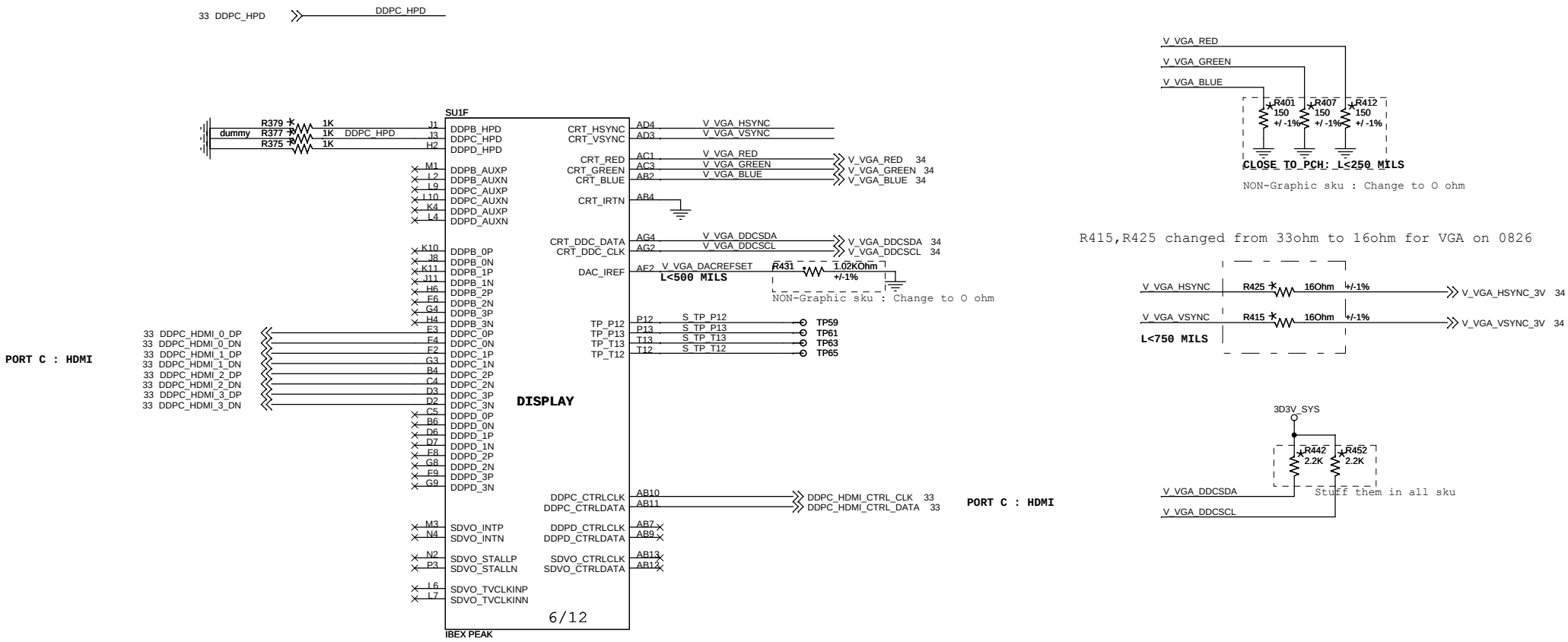
DMI TERMINATION VOLTAGE
DC COUP: TX/RX TO VCC IS SAMPLED HIGH





FOXCONN PCEG

Title: PCH-5:NVRAM/FDI		
Size: A3	Document Number: Agassi	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 23 of 53	



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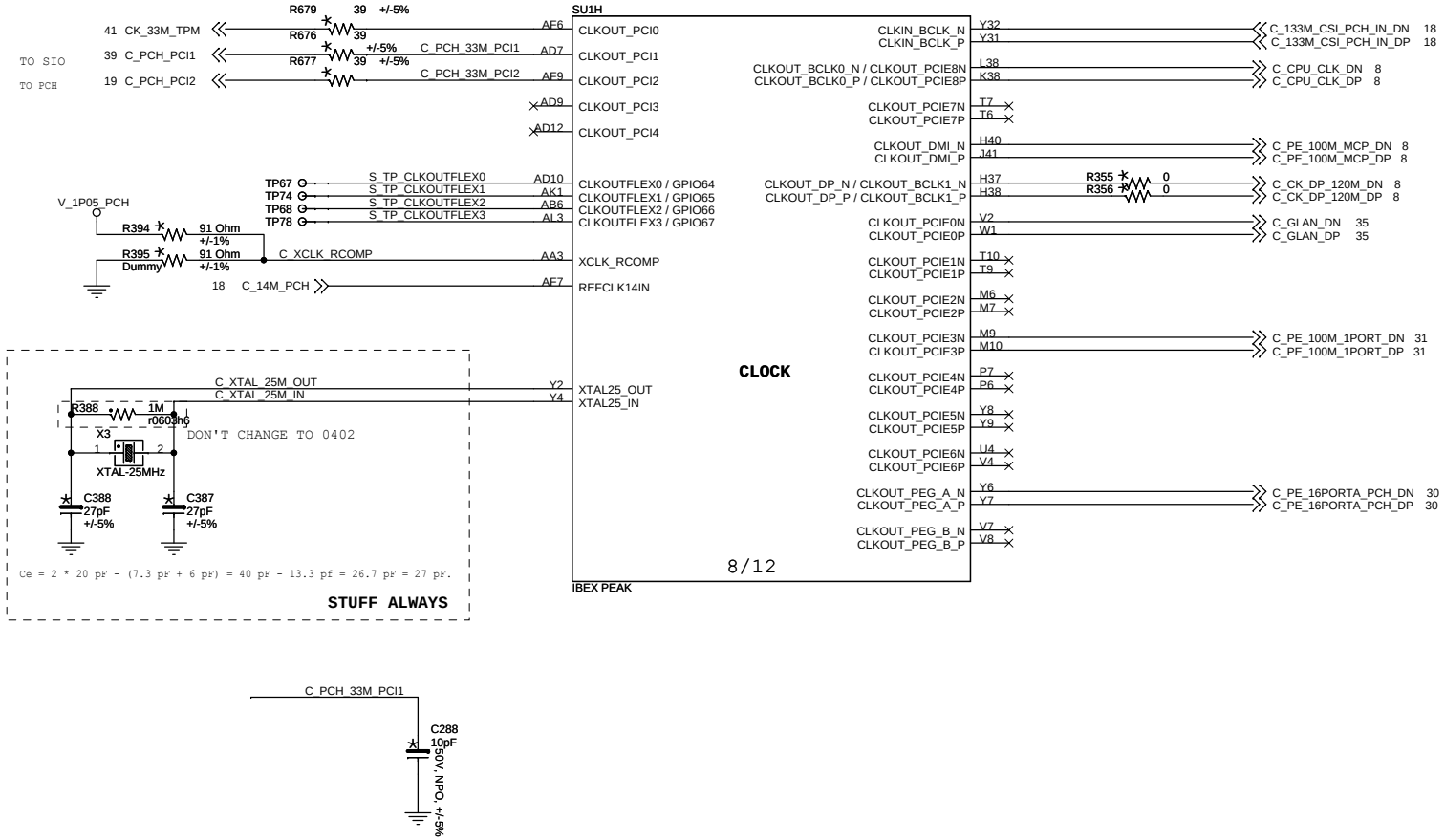
FOXCONN PCEG

Title: PCH-6:DISPLAY

Size	Document Number	Rev
A3	Agassi	1.0

Date: Thursday, March 04, 2010 Sheet 24 of 53



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FOXCONN PCEG

Title: PCH-7:CLOCK

Size	Document Number	Rev
A3	*Agassi*	1.0

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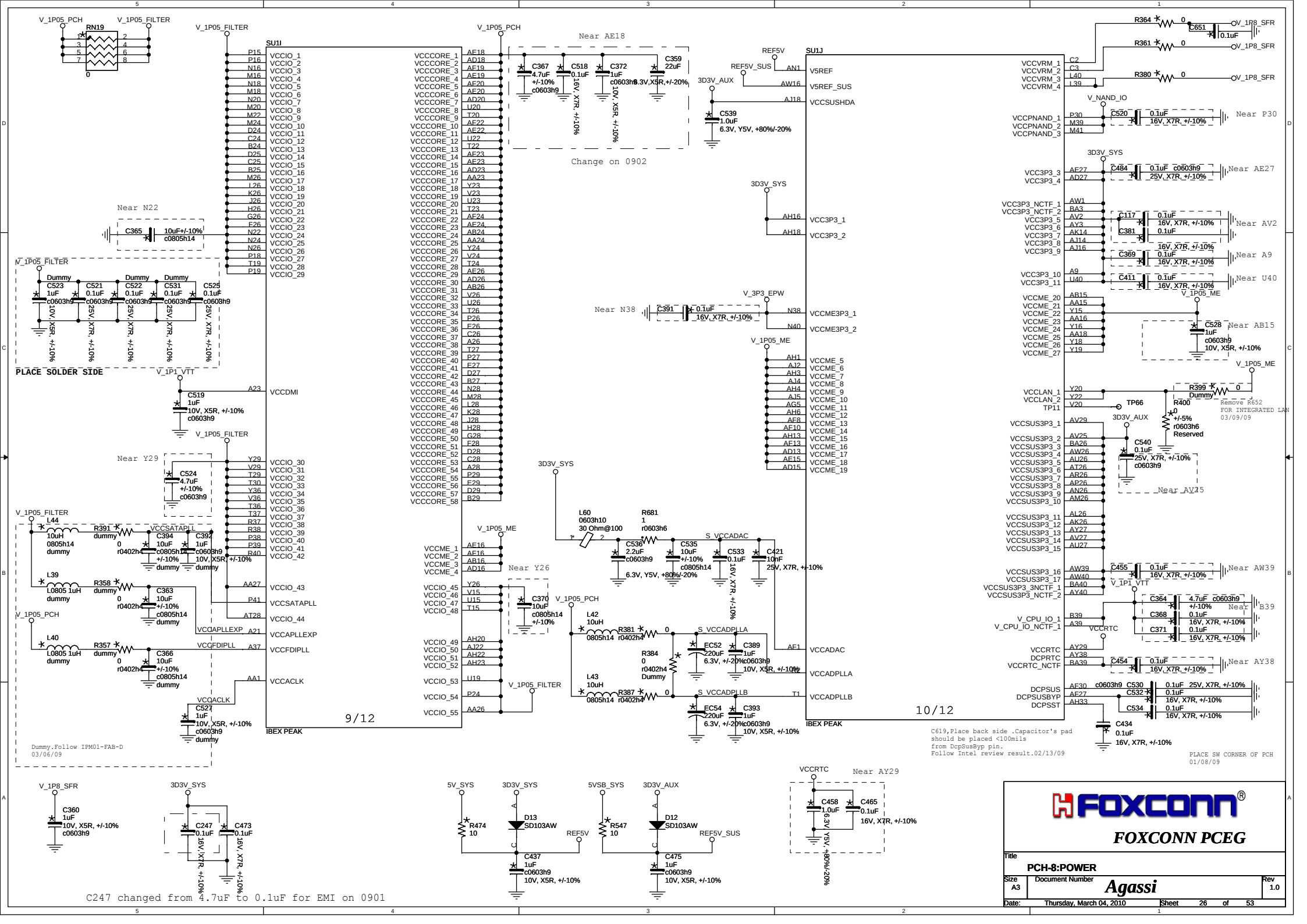
SU1I
SU1J
IBEX PEAK
9/12
10/12
PLACE SOLDER SIDE
Near N22
Near Y29
Near Y26
Near AE18
Change on 0902
Near N38
Near AB15
Near AV2
Near A9
Near U40
Near AW39
Near B39
Near AV15
Near AY38
Near AY29
Near P30
Near AE27
Dummy.Follow IPM01-FAB-D
03/06/09
C247 changed from 4.7uF to 0.1uF for EMI on 0901
C619,Place back side .Capacitor's pad should be placed <100mils from DcpSusByp pin. Follow Intel review result.02/13/09
PLACE SW CORNER OF PCH
01/08/09
Remove R652 FOR INTEGRATED LAN
03/09/09
FOXCONN PCEG
PCH-8:POWER
Agassi
Size A3
Rev 1.0
Date: Thursday, March 04, 2010
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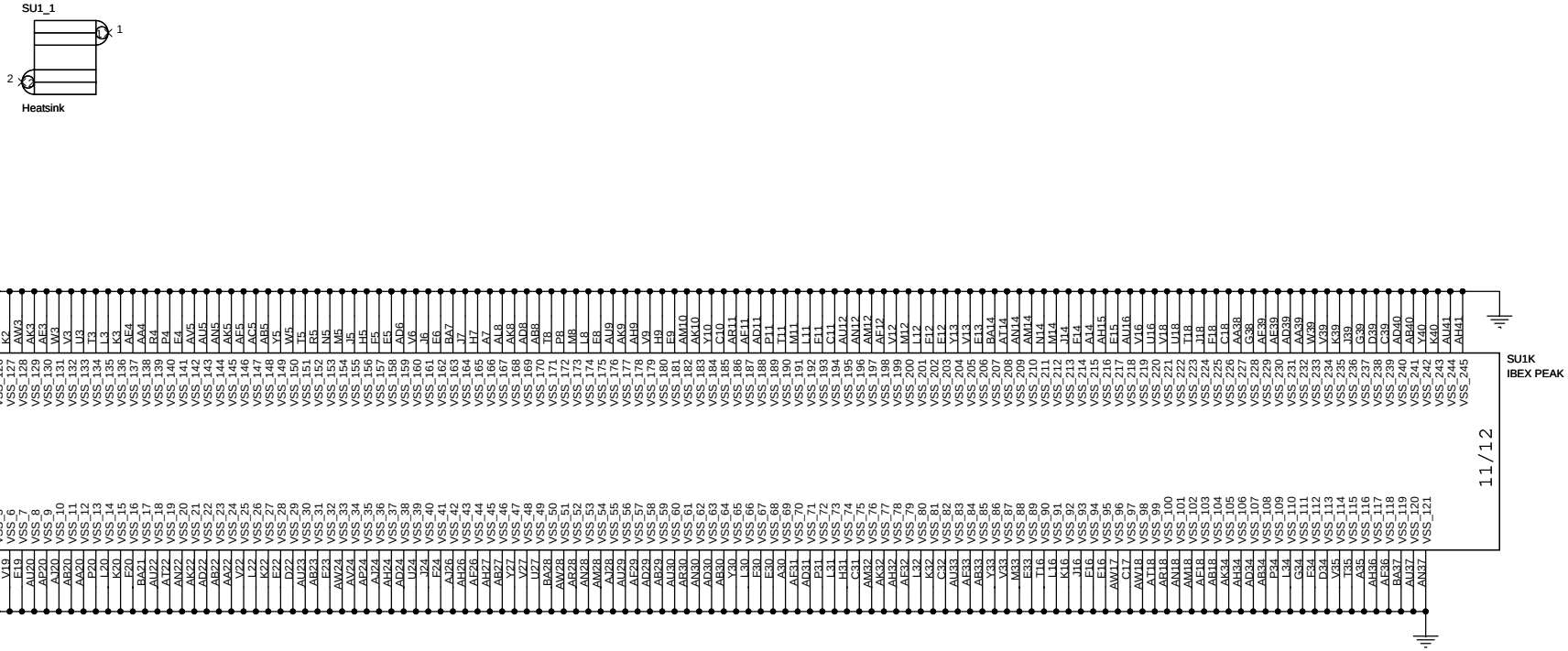

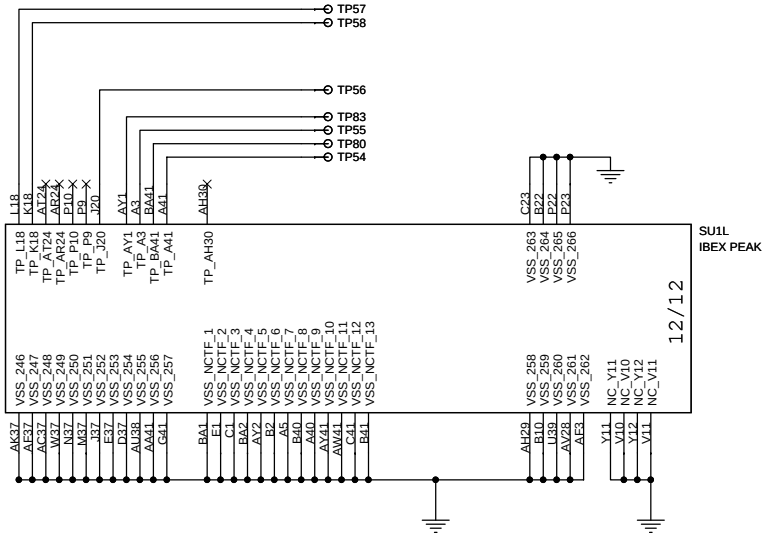

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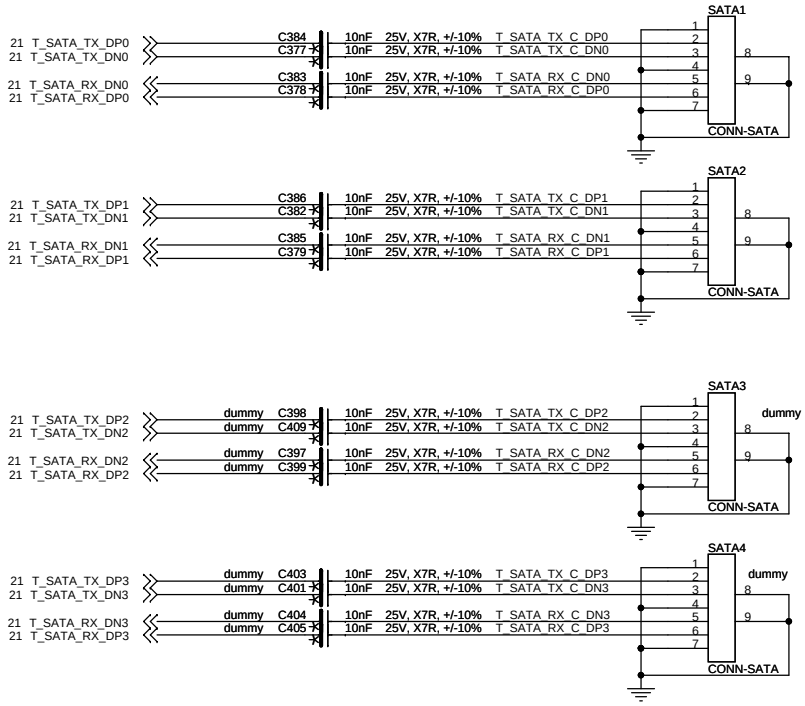
FOXCONN PCEG

Title: PCH-9:GND		
Size: A3	Document Number: *Agassi*	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 27 of 53	

BLUE



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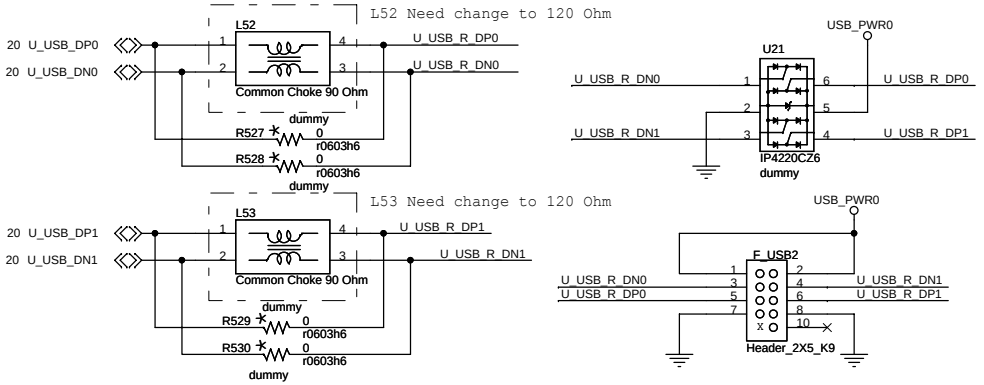
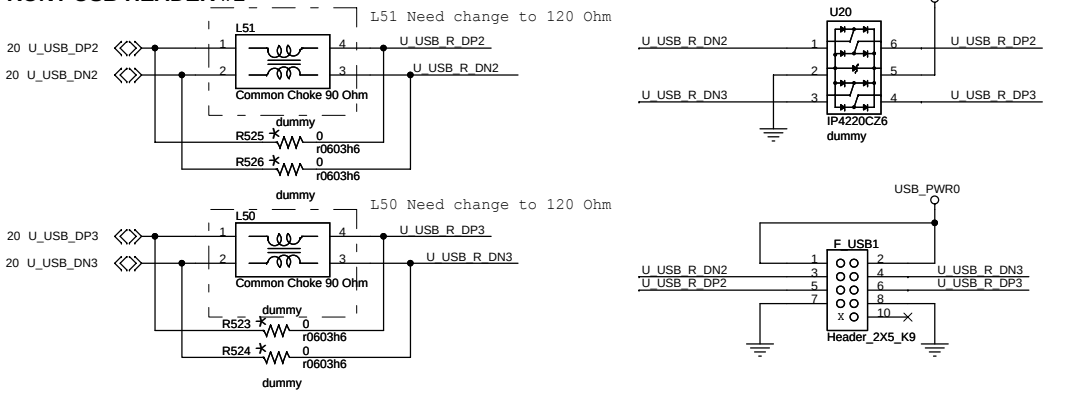
FOXCONN PCEG

Title: SATA CONNECTOR		
Size: A3	Document Number: *Agassi*	Rev: 1.0
Date: Thursday, March 04, 2010	Sheet 28 of 53	

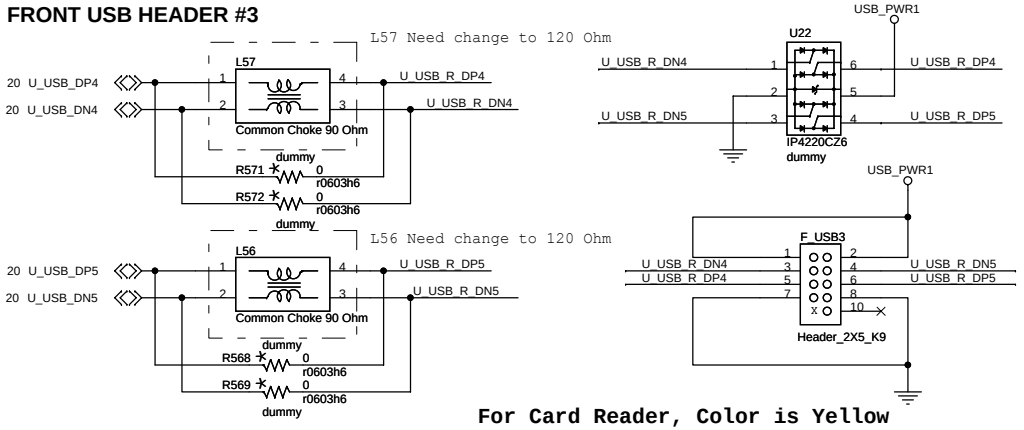
FRONT USB HEADER #2



FRONT USB HEADER #1

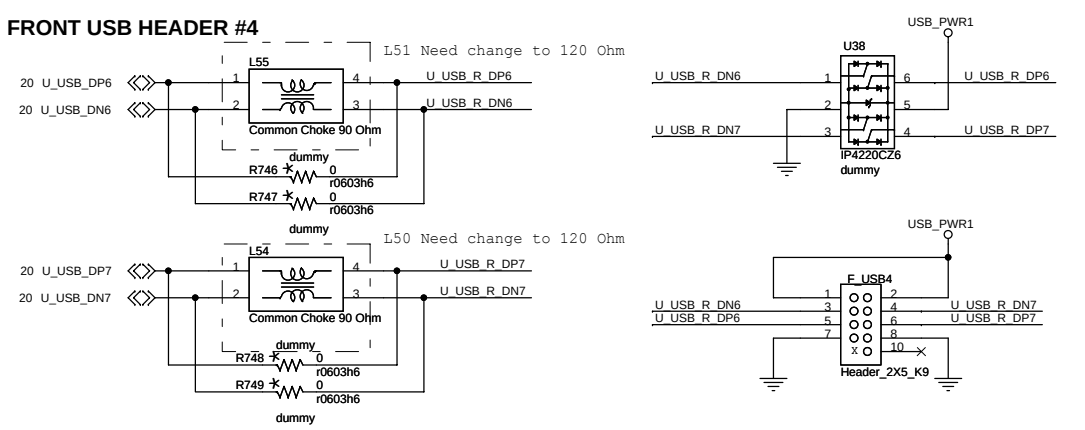


FRONT USB HEADER #3

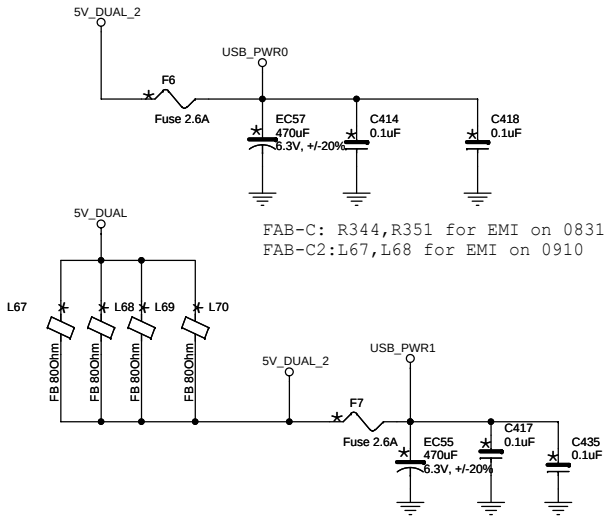


For Card Reader, Color is Yellow

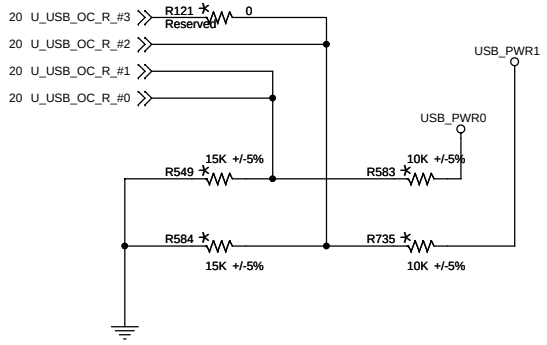
FRONT USB HEADER #4

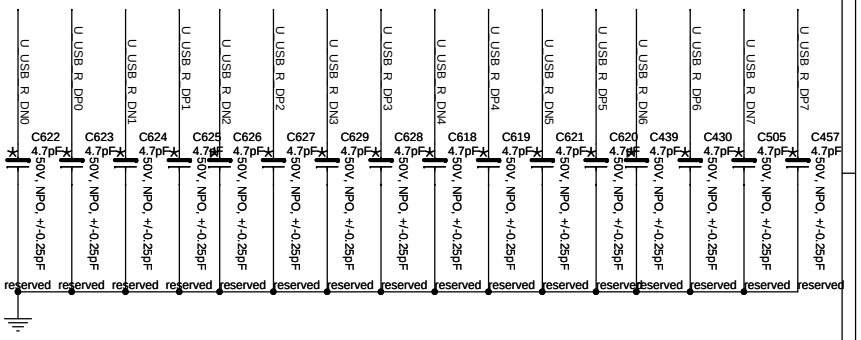


FRONT USB POWER



F-USB OC





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FOXCONN PCEG

Title: **USB:FRONT USB HEADER 1/2/3/4**

Size	Document Number	Rev
A3	*Agassi*	1.0

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9 X_EXP_A_TX_DP[15..0]

9 X_EXP_A_TX_DN[15..0]

X_EXP_A_RX_DP[15..0] 9

X_EXP_A_RX_DN[15..0] 9

V_3P3_PCIVAUX 3D3V_SYS +12V_SYS

+12V_SYS 3D3V_SYS

PCI-E1_16X

15,17,22,31,35,47 S_SMB_CLK_RESUME

15,17,22,31,35,47 S_SMB_DATA_RESUME

22,31,35 S_WAKE#

R174 0 X_PLTRST_PCIE_SLOTA# 39

C147 22pF 50V, NPO, +/-5%

C_PE_16PORTA_PCH_DP 25

C_PE_16PORTA_PCH_DN 25

X_EXP_A_TX_DP0	C161	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP0	X_EXP_A_TX_DN0	C159	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN0
X_EXP_A_TX_DP1	C167	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP1	X_EXP_A_TX_DN1	C168	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN1
X_EXP_A_TX_DP2	C169	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP2	X_EXP_A_TX_DN2	C176	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN2
X_EXP_A_TX_DP3	C183	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP3	X_EXP_A_TX_DN3	C182	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN3
X_EXP_A_TX_DP4	C210	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP4	X_EXP_A_TX_DN4	C211	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN4
X_EXP_A_TX_DP5	C223	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP5	X_EXP_A_TX_DN5	C234	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN5
X_EXP_A_TX_DP6	C242	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP6	X_EXP_A_TX_DN6	C241	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN6
X_EXP_A_TX_DP7	C244	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP7	X_EXP_A_TX_DN7	C248	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN7
X_EXP_A_TX_DP8	C250	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP8	X_EXP_A_TX_DN8	C253	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN8
X_EXP_A_TX_DP9	C257	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP9	X_EXP_A_TX_DN9	C258	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN9
X_EXP_A_TX_DP10	C262	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP10	X_EXP_A_TX_DN10	C265	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN10
X_EXP_A_TX_DP11	C270	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP11	X_EXP_A_TX_DN11	C271	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN11
X_EXP_A_TX_DP12	C274	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP12	X_EXP_A_TX_DN12	C275	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN12
X_EXP_A_TX_DP13	C276	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP13	X_EXP_A_TX_DN13	C278	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN13
X_EXP_A_TX_DP14	C279	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP14	X_EXP_A_TX_DN14	C280	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN14
X_EXP_A_TX_DP15	C281	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DP15	X_EXP_A_TX_DN15	C282	0.1uF 16V, X7R, +/-10%	X_EXP_A_TX_C_DN15

A1	PRSNT1#	12V1	B1
A2	12V3	12V2	B2
A3	12V4	RSVD8	B3
A4	GND68	GND1	B4
A5	JTAG2	SMCLK	B5
A6	JTAG3	SMDAT	B6
A7	JTAG4	GND2	B7
A8	JTAG5	3.3V3	B8
A9	3.3V1	JTAG1	B9
A10	3.3V2	3.3VAUX	B10
A11	PWRGD	WAKE#	B11
	KEY		
A12	GND67	RSVD1	B12
A13	REFCLK+	GND3	B13
A14	REFCLK-	HSOP0	B14
A15	GND66	HSON0	B15
A16	HSIP0	GND4	B16
A17	HSIN0	PRSNT2_B17#	B17
A18	GND65	GND5	B18
A19	RSVD7	HSOP1	B19
A20	GND64	HSON1	B20
A21	HSIP1	GND6	B21
A22	HSIN1	GND7	B22
A23	GND63	HSOP2	B23
A24	GND62	HSON2	B24
A25	HSIP2	GND8	B25
A26	HSIN2	GND9	B26
A27	GND61	HSOP3	B27
A28	GND60	HSON3	B28
A29	HSIP3	GND10	B29
A30	HSIN3	RSVD2	B30
A31	GND59	PRSNT2_B31#	B31
A32	RSVD6	GND11	B32
A33	RSVD5	HSOP4	B33
A34	GND58	HSON4	B34
A35	HSIP4	GND12	B35
A36	HSIN4	GND13	B36
A37	GND57	HSOP5	B37
A38	GND56	HSON5	B38
A39	HSIP5	GND14	B39
A40	HSIN5	GND15	B40
A41	GND55	HSOP6	B41
A42	GND54	HSON6	B42
A43	HSIP6	GND16	B43
A44	HSIN6	GND17	B44
A45	GND53	HSOP7	B45
A46	GND52	HSON7	B46
A47	HSIP7	GND18	B47
A48	HSIN7	PRSNT2_B48#	B48
A49	GND51	GND19	B49
A50	RSVD4	HSOP8	B50
A51	GND50	HSON8	B51
A52	HSIP8	GND20	B52
A53	HSIN8	GND21	B53
A54	GND49	HSOP9	B54
A55	GND48	HSON9	B55
A56	HSIP9	GND22	B56
A57	HSIN9	GND23	B57
A58	GND47	HSOP10	B58
A59	GND46	HSON10	B59
A60	HSIP10	GND24	B60
A61	HSIN10	GND25	B61
A62	GND45	HSOP11	B62
A63	GND44	HSON11	B63
A64	HSIP11	GND26	B64
A65	HSIN11	GND27	B65
A66	GND43	HSOP12	B66
A67	GND42	HSON12	B67
A68	HSIP12	GND28	B68
A69	HSIN12	GND29	B69
A70	GND41	HSOP13	B70
A71	GND40	HSON13	B71
A72	HSIP13	GND30	B72
A73	HSIN13	GND31	B73
A74	GND39	HSOP14	B74
A75	GND38	HSON14	B75
A76	HSIP14	GND32	B76
A77	HSIN14	GND33	B77
A78	GND37	HSOP15	B78
A79	GND36	HSON15	B79
A80	HSIP15	GND34	B80
A81	HSIN15	PRSNT2_B81#	B81
A82	GND35	RSVD3	B82

Slot-PCIE-16X

X_EXP_A_RX_DP0	X_EXP_A_RX_DN0	A16	A17
X_EXP_A_RX_DP1	X_EXP_A_RX_DN1	A21	A22
X_EXP_A_RX_DP2	X_EXP_A_RX_DN2	A25	A26
X_EXP_A_RX_DP3	X_EXP_A_RX_DN3	A29	A30
X_EXP_A_RX_DP4	X_EXP_A_RX_DN4	A35	A36
X_EXP_A_RX_DP5	X_EXP_A_RX_DN5	A39	A40
X_EXP_A_RX_DP6	X_EXP_A_RX_DN6	A43	A44
X_EXP_A_RX_DP7	X_EXP_A_RX_DN7	A47	A48
X_EXP_A_RX_DP8	X_EXP_A_RX_DN8	A52	A53
X_EXP_A_RX_DP9	X_EXP_A_RX_DN9	A56	A57
X_EXP_A_RX_DP10	X_EXP_A_RX_DN10	A60	A61
X_EXP_A_RX_DP11	X_EXP_A_RX_DN11	A64	A65
X_EXP_A_RX_DP12	X_EXP_A_RX_DN12	A68	A69
X_EXP_A_RX_DP13	X_EXP_A_RX_DN13	A72	A73
X_EXP_A_RX_DP14	X_EXP_A_RX_DN14	A76	A77
X_EXP_A_RX_DP15	X_EXP_A_RX_DN15	A80	A81

+12V_SYS 3D3V_SYS V_3P3_PCIVAUX

For EMI-0909

EC25 470uF 16V, +/-20% ce35d80h125 Reserved

C126 0.1uF reserved

EC31 1000uF +/-20% ce35d80h130 dummy

C130 0.1uF dummy

C131 0.1uF dummy

C134 0.1uF reserved

16V, Y5V, +80%/-20%

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Title: PCIE X16 SLOT

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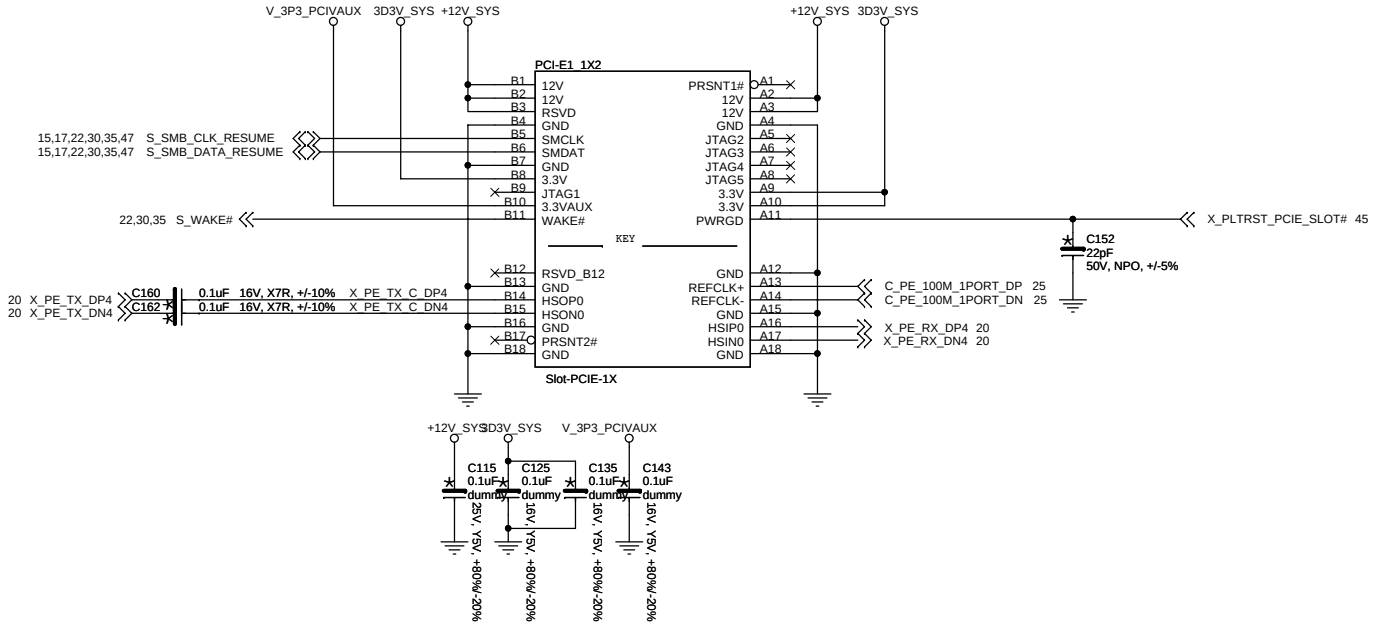
PCIEX1_SLOT



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Title: PCIE X1 SLOT 1/2		
Size: A3	Document Number: *Agassi*	Rev: 1.0
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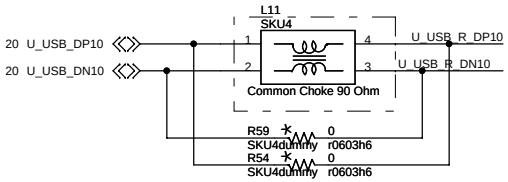
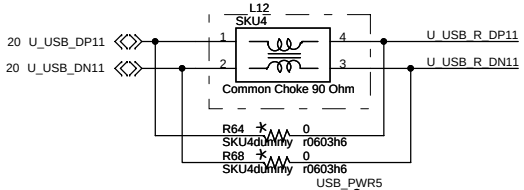
Rear USB connector X2

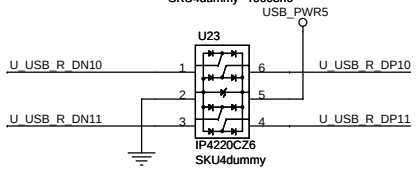
Change U18 and U17 from 90 to 120 for EMI-060926

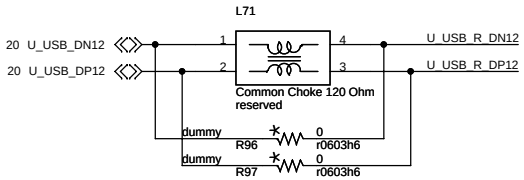
L11 Changed from 90ohm to 120ohm for EMI-0909

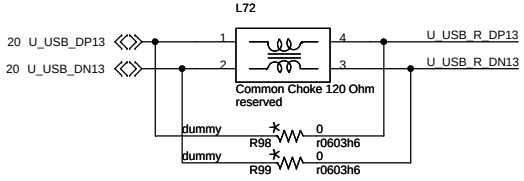


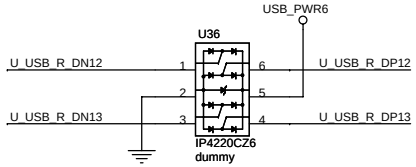
L12 Changed from 90ohm to 120ohm for EMI-0909

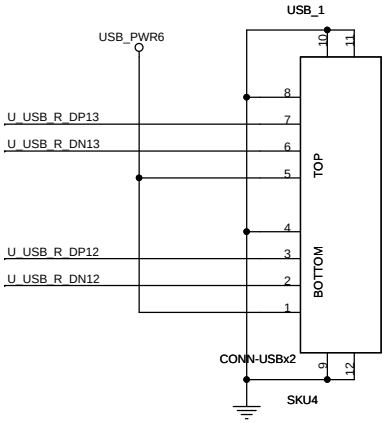


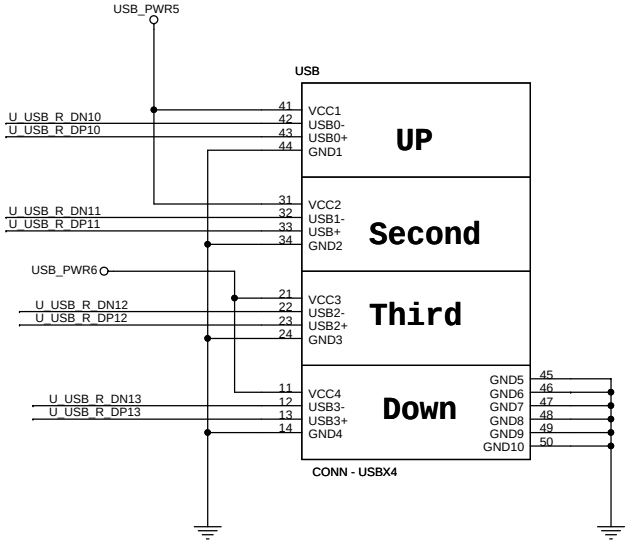


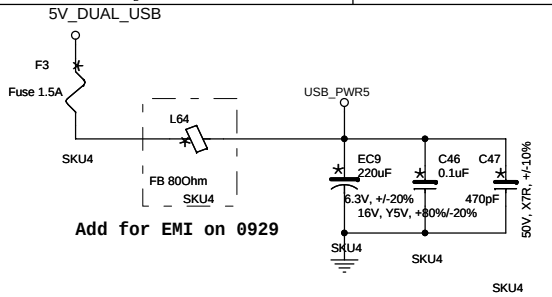




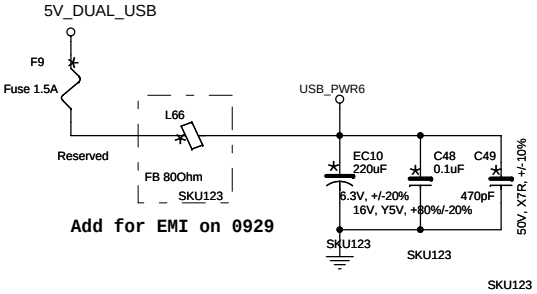






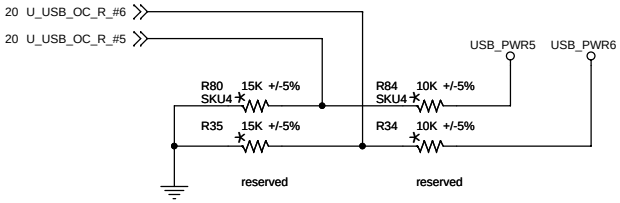


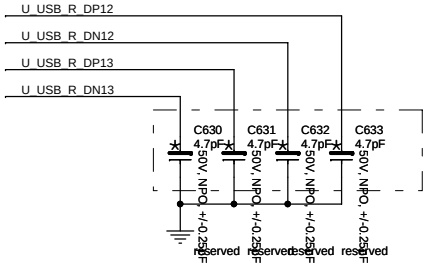
Add for EMI on 0929

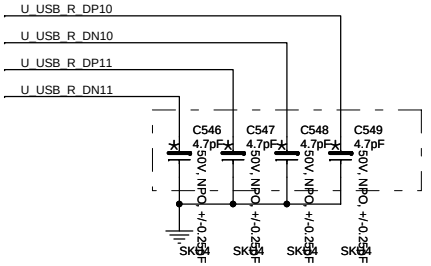


Add for EMI on 0929

Rear USB OC







ADD for SI -0901

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Title: eSATA_USB CONN		
Size: A3	Document Number: Agassi	Rev: 1.0
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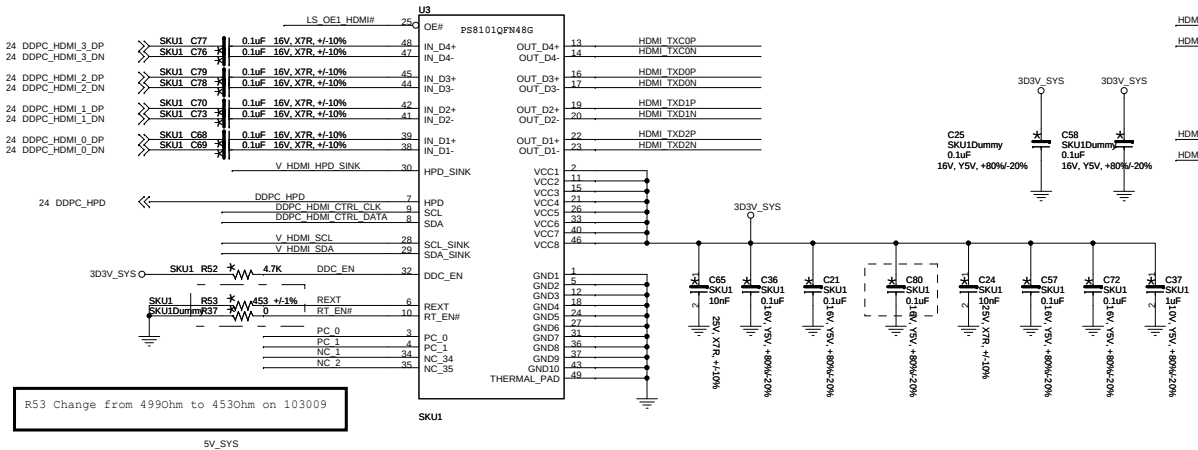
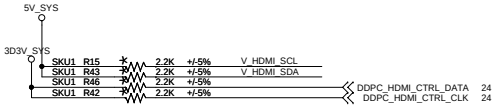
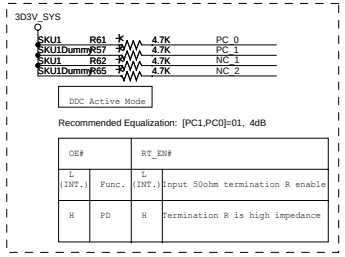
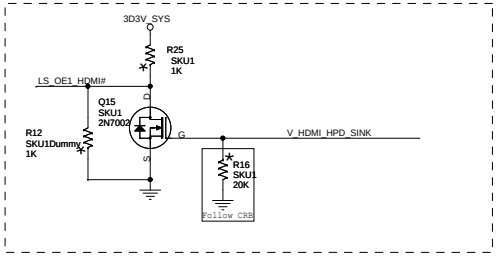
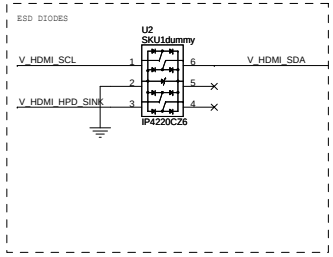
HDMI Level shift

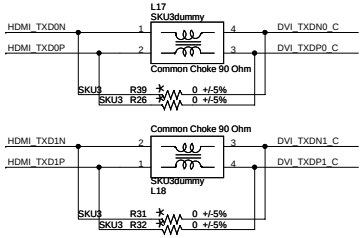


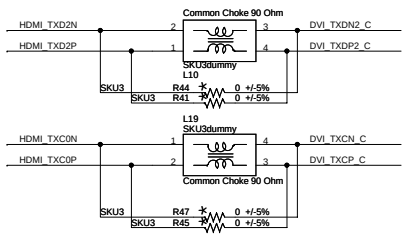


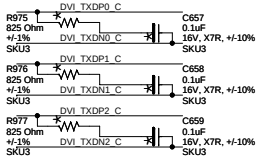


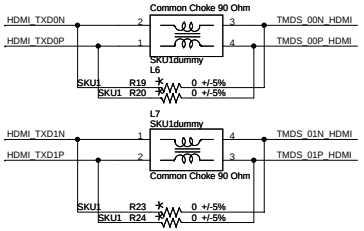


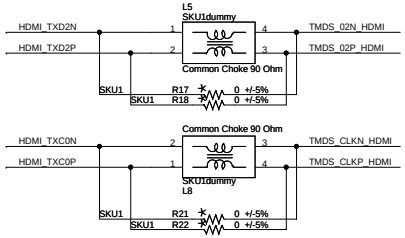




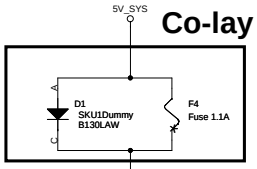




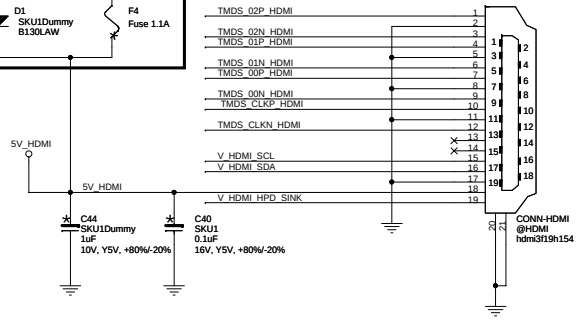




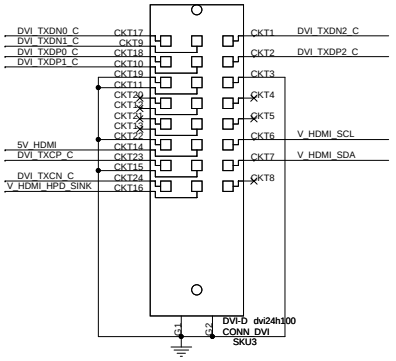
Co-lay



HDMI Connector



DVI_D



FOXCONN PCEG			
Title: HDMI connector			
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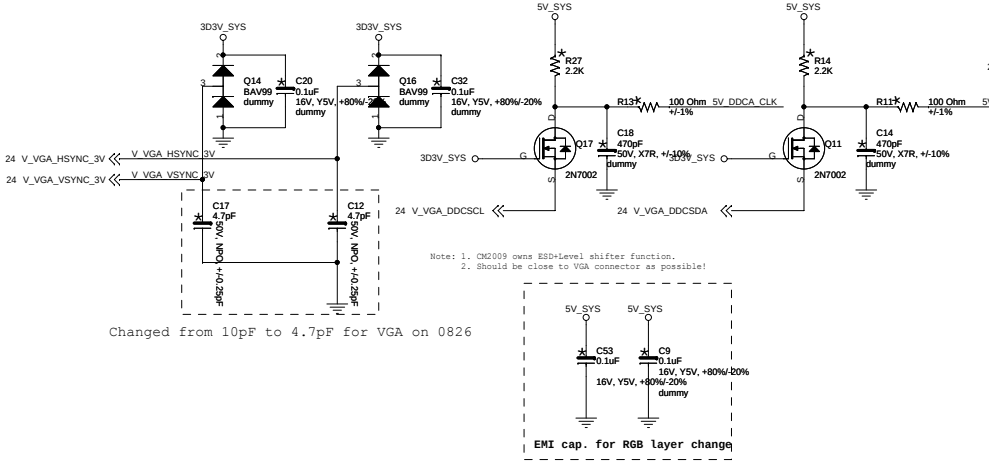
RGB routing
1.Match the trace lengths within CRT_RED, CRT_GREEN and CRT_BLUE to 200 mils (0.508 cm).
2.Match the trace lengths of CRT SYNC signals with CRT DAC signals to 200 mils (0.508 cm).
3.All length matching is based on Ibex Peak die-pad to CRT connector routing length and thus includes package length compensation.

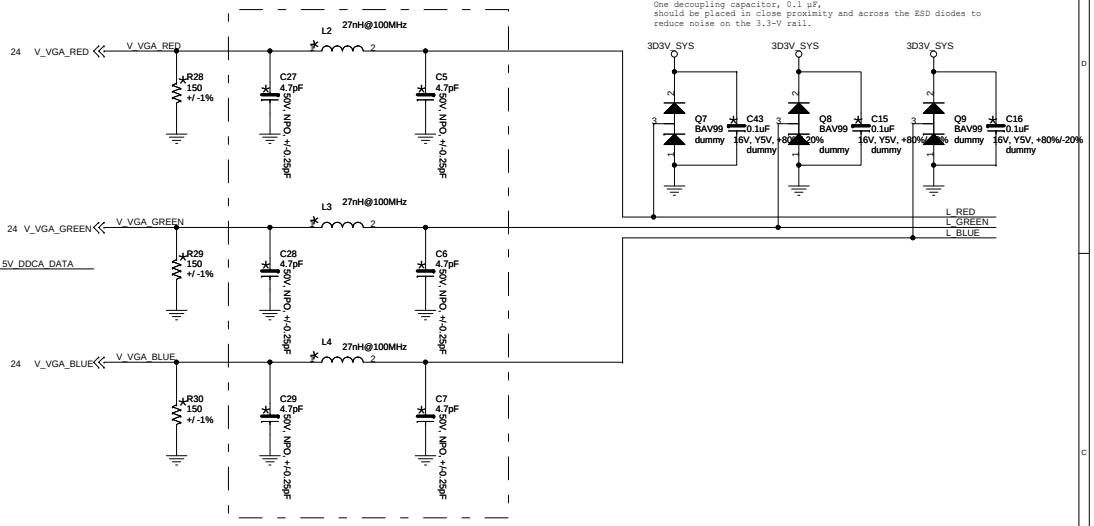
ESD diodes are required for each CRT DAC output. The diodes should connect between the 3.3-V power plane (from the regulator) and ground. These diodes should have a low C rating (~5 pF max) and a small leakage current (~10 µA at 120°C). The diodes should be placed to keep the inductance of the 3.3-V power rail connection as low as possible. These diodes should be placed between the analog switch and the VGA connector, preferably near the respective VGA connector. In addition, one decoupling capacitor, C1 = 0.1 µF, should be placed in close proximity and across the ESD diodes to reduce noise on the 3.3-V rail.



Changed from 10pF to 4.7pF for VGA on 0826

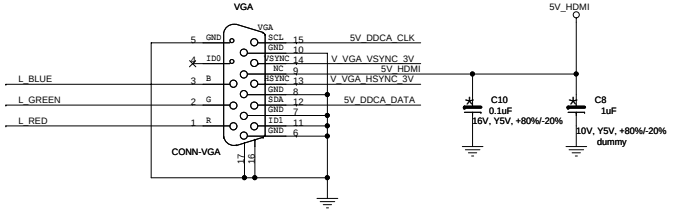
Note: 1. CM2009 owns ESD+Level shifter function.
2. Should be close to VGA connector as possible!

Changed for VGA on 0826



One decoupling capacitor, 0.1 µF, should be placed in close proximity and across the ESD diodes to reduce noise on the 3.3-V rail.

VGA Connector



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FOXCONN PCEG

Title: VGA connector			
Size: C	Document Number: Agassi		Rev: 1.0
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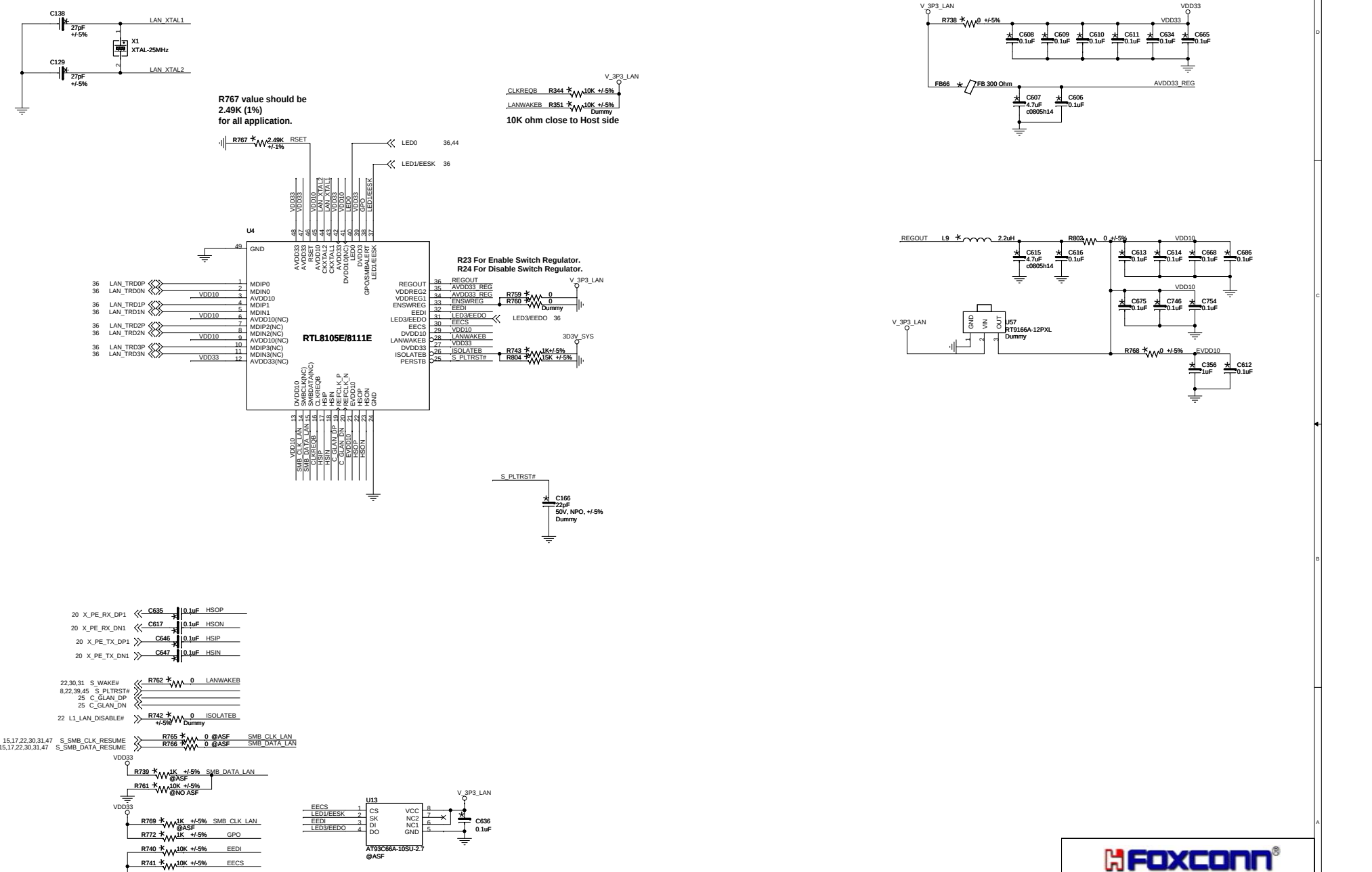
C138
27pF
+/-5%
LAN_XTAL1
X1
XTAL-25MHz
C129
27pF
+/-5%
LAN_XTAL2
R767 value should be
2.49K (1%)
for all application.
R767 2.49K +/-1% RSET
LED0 36,44
LED1/EESK 36
U4
RTL8105E/8111E
CLKREQB R344 10K +/-5%
LANWAKEB R351 10K +/-5% Dummy
V_3P3_LAN
10K ohm close to Host side
R23 For Enable Switch Regulator.
R24 For Disable Switch Regulator.
R759 0 Dummy
R760 0
R743 1K+/-5%
R804 15K +/-5%
3D3V_SYS
LED3/EEDO 36
S_PLTRST#
C166
22pF
50V, NPO, +/-5%
Dummy
V_3P3_LAN
R738 0 +/-5%
VDD33
C608 0.1uF
C609 0.1uF
C610 0.1uF
C611 0.1uF
C634 0.1uF
C665 0.1uF
FB66 FB 300 Ohm
AVDD33_REG
C607 4.7uF c0805h14
C606 0.1uF
REGOUT
L9 2.2uH
R802 0 +/-5%
VDD10
C615 4.7uF c0805h14
C616 0.1uF
C613 0.1uF
C614 0.1uF
C668 0.1uF
C686 0.1uF
C675 0.1uF
C746 0.1uF
C754 0.1uF
U57
RT9166A-12PXL
Dummy
GND
VIN
OUT
R768 0 +/-5%
EVDD10
C356 1uF
C612 0.1uF
20 X_PE_RX_DP1 C635 0.1uF HSOP
20 X_PE_RX_DN1 C617 0.1uF HSON
20 X_PE_TX_DP1 C646 0.1uF HSIP
20 X_PE_TX_DN1 C647 0.1uF HSIN
22,30,31 S_WAKE#
8,22,39,45 S_PLTRST#
25 C_GLAN_DP
25 C_GLAN_DN
R762 0 LANWAKEB
22 L1_LAN_DISABLE#
R742 0 +/-5% Dummy ISOLATEB
15,17,22,30,31,47 S_SMB_CLK_RESUME
15,17,22,30,31,47 S_SMB_DATA_RESUME
R765 0 @ASF SMB_CLK_LAN
R766 0 @ASF SMB_DATA_LAN
VDD33
R739 1K +/-5% @ASF SMB_DATA_LAN
R761 10K +/-5% @NO ASF
R769 1K +/-5% @ASF SMB_CLK_LAN
R772 1K +/-5% GPO
R740 10K +/-5% EEDI
R741 10K +/-5% EECS
U13
EECS
LED1/EESK
EEDI
LED3/EEDO
CS
SK
DI
DO
VCC
NC2
NC1
GND
C636 0.1uF
AT93C66A-10SU-2.7
@ASF
FOXCONN
FOXCONN PCEG
Title
LAN-1:INTEL HANKSVILLE
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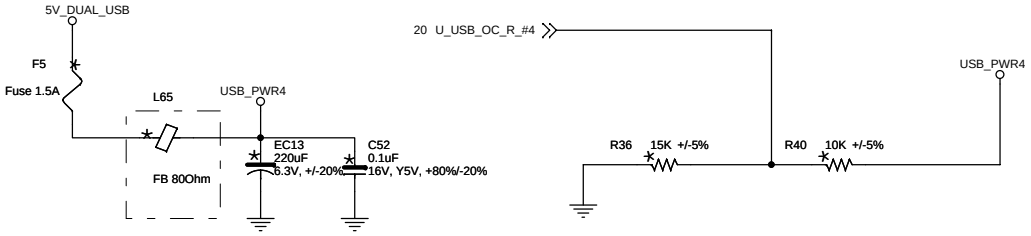
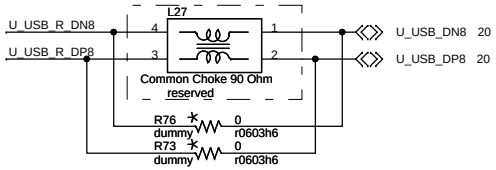
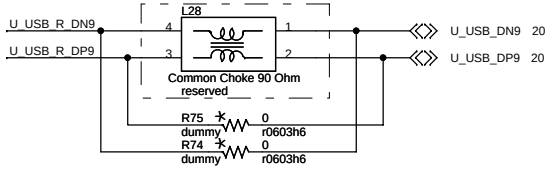
LAN + 2USB CONNECTOR

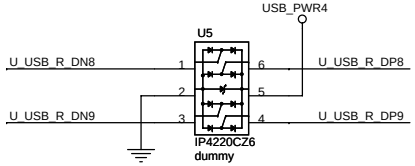


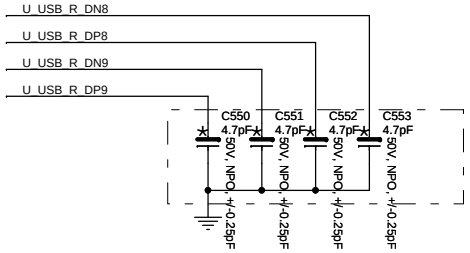
L27 changed from 90ohm to 120ohm for EMI-0909



L28 changed from 90ohm to 120ohm for EMI-0909



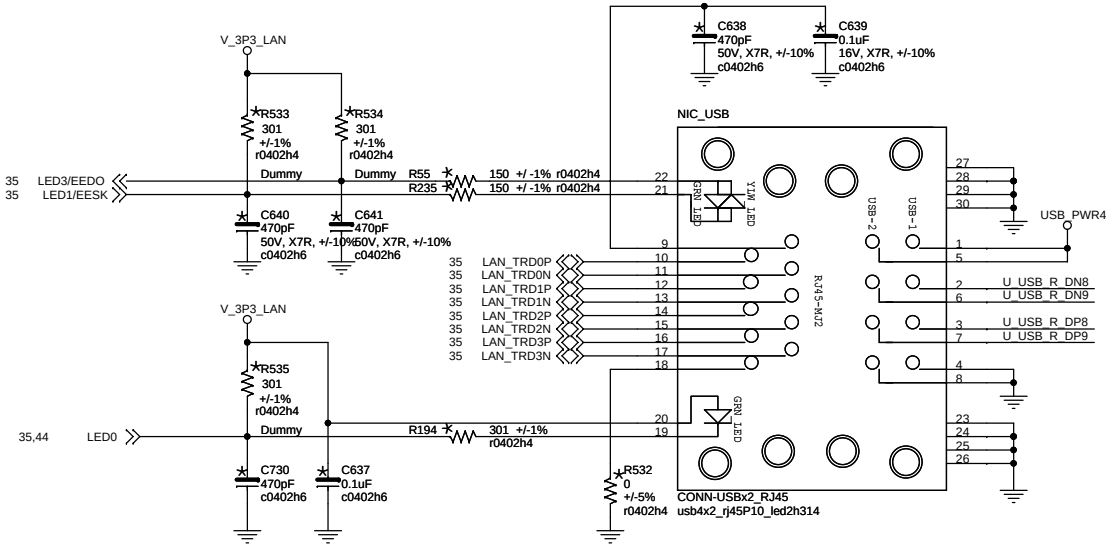




ADD for SI -0901

LAN CONN

OFF = LINK 10 Mbps
GREEN = LINK 100 Mbps
YELLOW = LINK 1000 Mbps



ACTIVE LED
GREEN = LINK UP
BLINKING = TX/RX ACTIVITY

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Title: LAN-2:CONNECTOR WITH USB		
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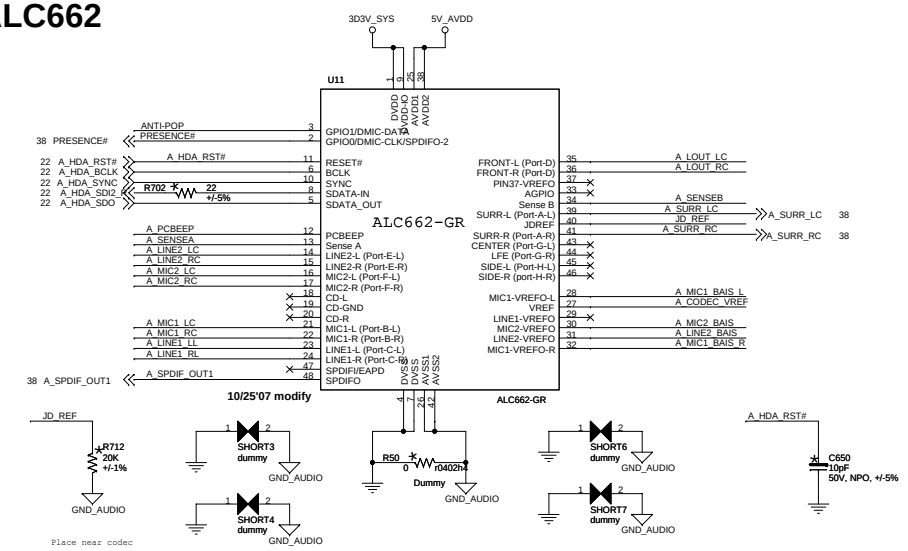
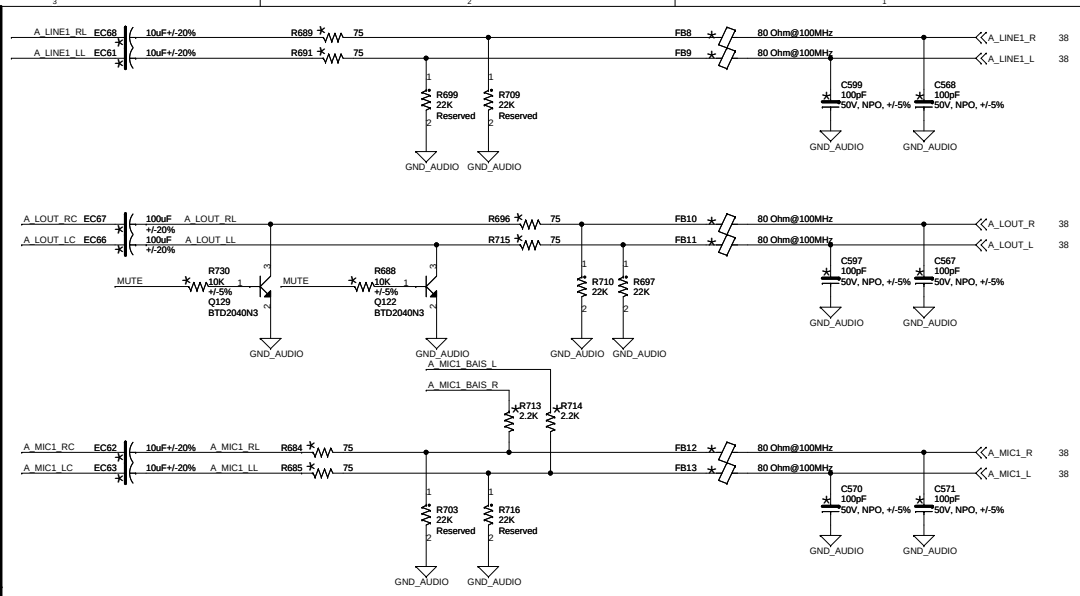
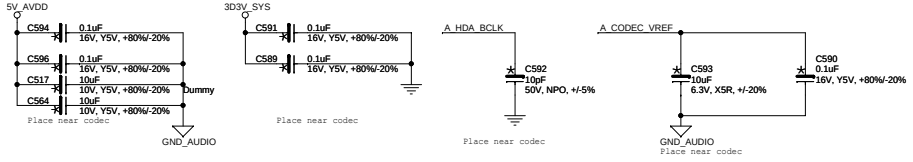
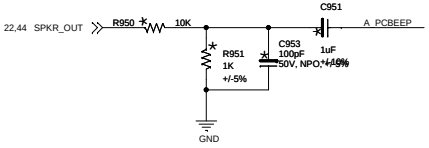
ALC662



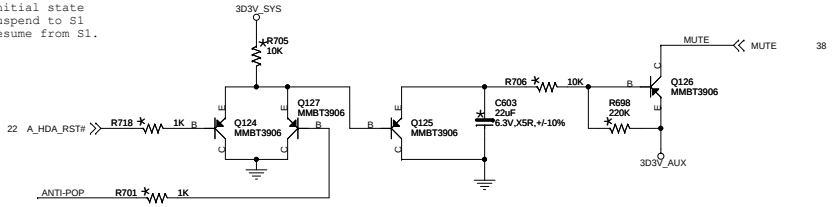




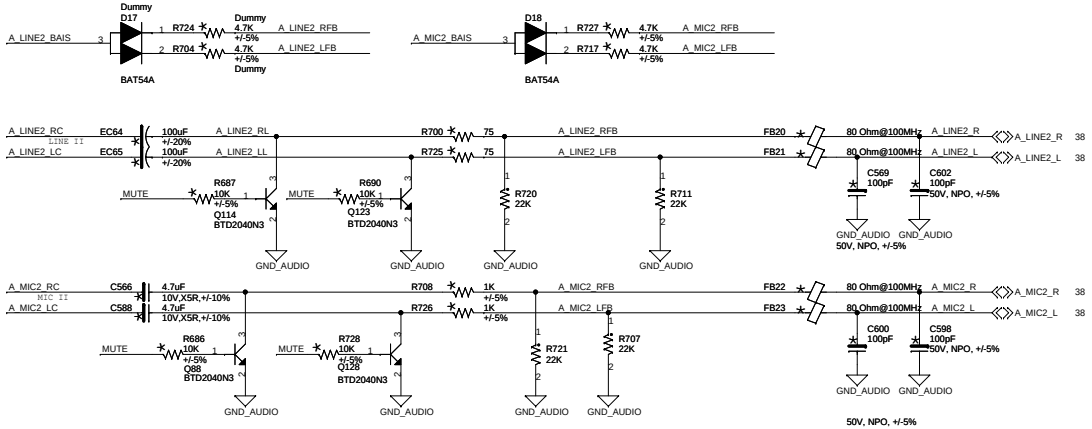


Control by software driver and
S/B GPIO.
GPIO#0 driver low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.

DIGITAL AREA

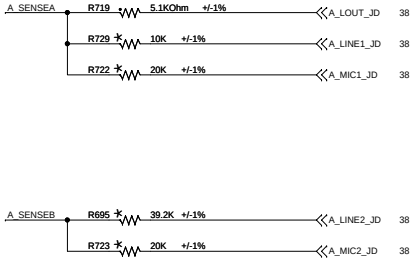


FRONT PANEL



JACK SENSE

All of JD resistors should be placed as close to the codec sense pin.



FOXCONN PCEG

Title	AUDIO-1:ALC888S	
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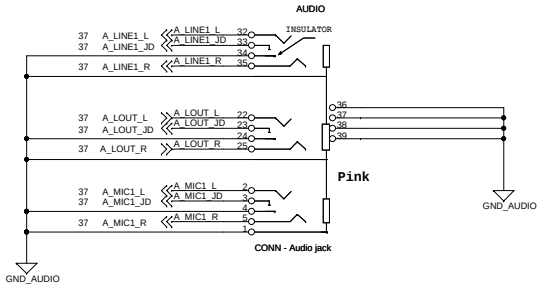
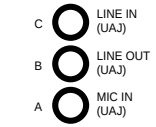
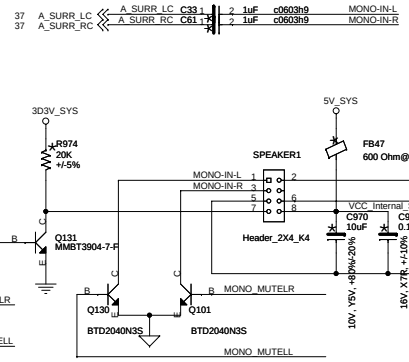
Audio CONN (3 Port)

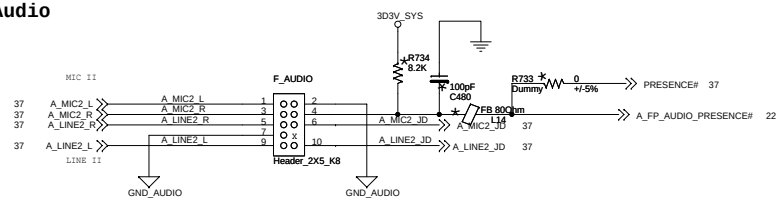


Audio Jack

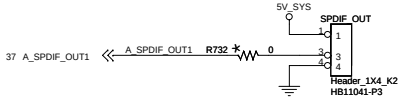




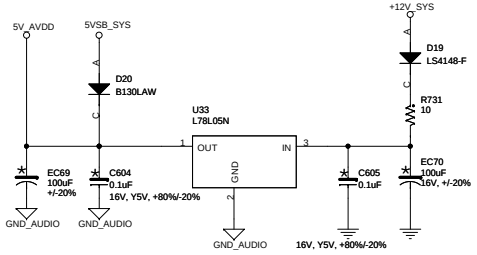
Front_Audio



SPDIF_OUT



12V to 5V Power Regulator



FOXCONN PCEG			
Title: AUDIO-2:CONNECTOR			
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IT8720 Power On Strapping Options

Symbol		value	Description
JP1 (pin 38)	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment1 is enable
JP3 Pin 124	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP2/JP6 Pin122/Pin29	SVID_EN	11	Disable VID/SVID out pins
		01	For Intel Platform Enable VIDO0-VIDO7 output pins.
		10	For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins
		00	For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out It is selected by CPU

Follow ITE:
R683 changed from 2.2K to 4.7K
Pull changed from 3D3V_SYS to 3D3V_AUX on 0929

Follow ITE:
R633 changed from 10K to 4.7K
Pull changed from 5V_SYS to 3D3V_SYS on 0929

Follow ITE:
R648 Pull up changed from 3D3V_AUX to 3D3V_SYS on 0929

If without use these pins, Please pull-up to VCC.
Don't let it floating
1.Pin 30:RESETCON#
2.Pin 95:VIN3/ATXPG
3.Pin 71:SUSB#
4..Power On Strapping Options pin

R632 changed from 1K to 10K for EUP on 0929

ITE suggest :
change C606 to 4.7uF for 8721
2009-07-08

IT8721F/CX

ITE8720 Colay ITE8721

FOXCONN PCEG

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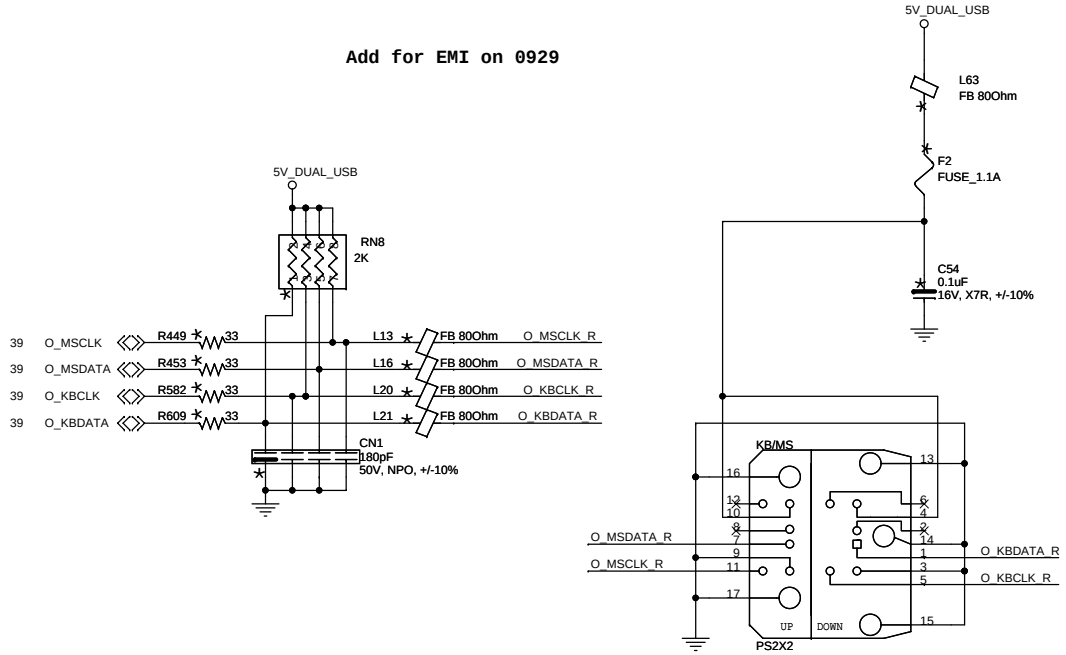
PS2

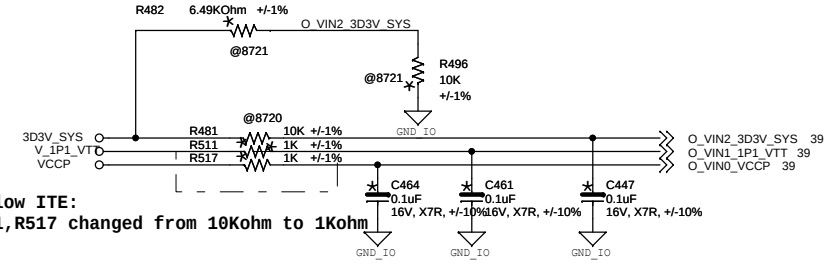
L13,L14,L15.L16 change from 80ohm to 120ohm on 1105200

Add for EMI on 0929

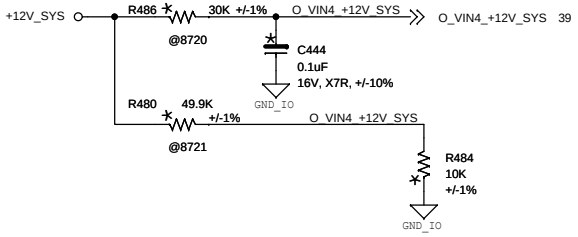


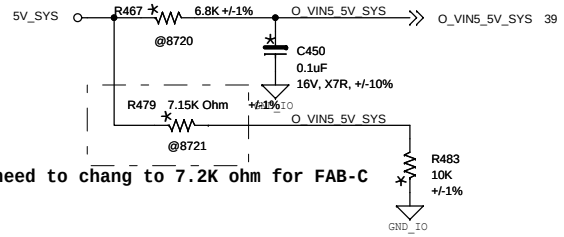
Voltage Monitor Detect:Vcore/+12V/+5V_SYS/+3.3V_SYS/1P1_VTT/5VSB

All parts close to SIO



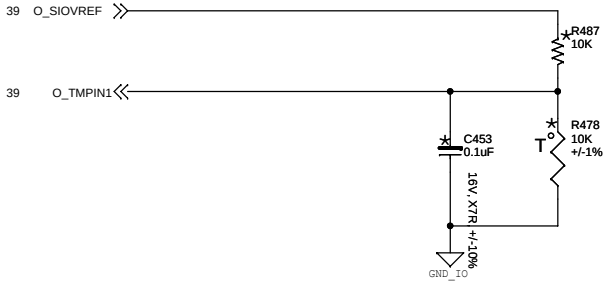
Follow ITE:
R511,R517 changed from 10Kohm to 1Kohm

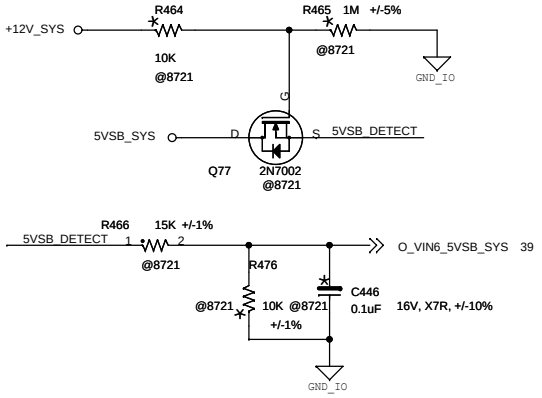




R479 need to chang to 7.2K ohm for FAB-C

Temperature Monitor: Detect system temperature





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Title: SIO-2:PS2/HW Monitor		
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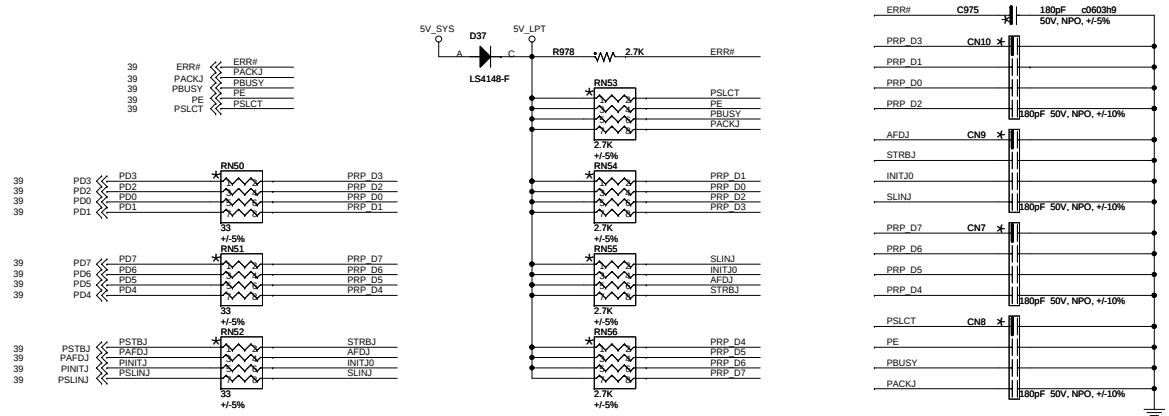
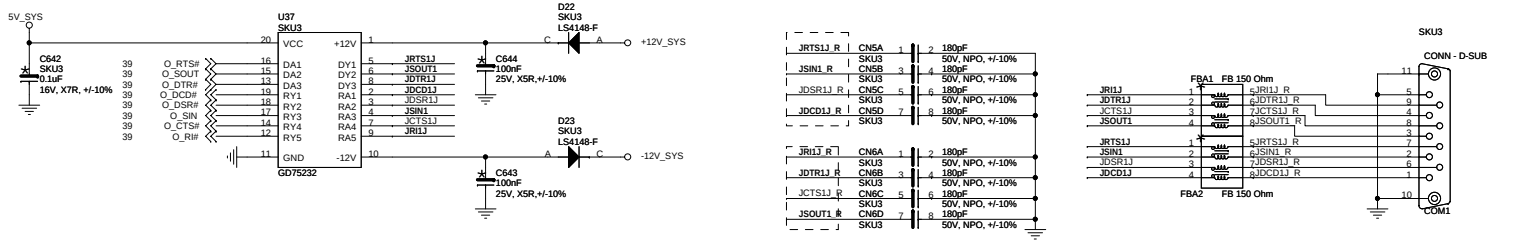
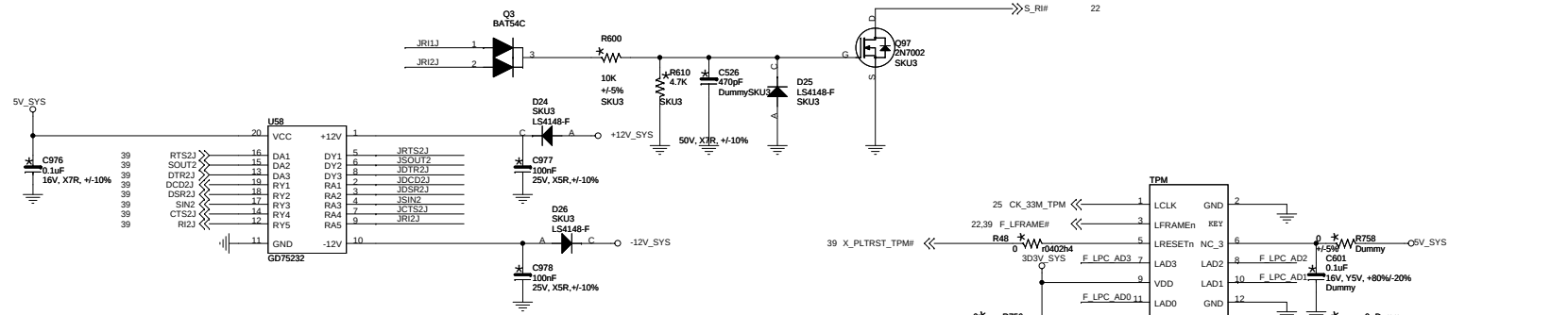


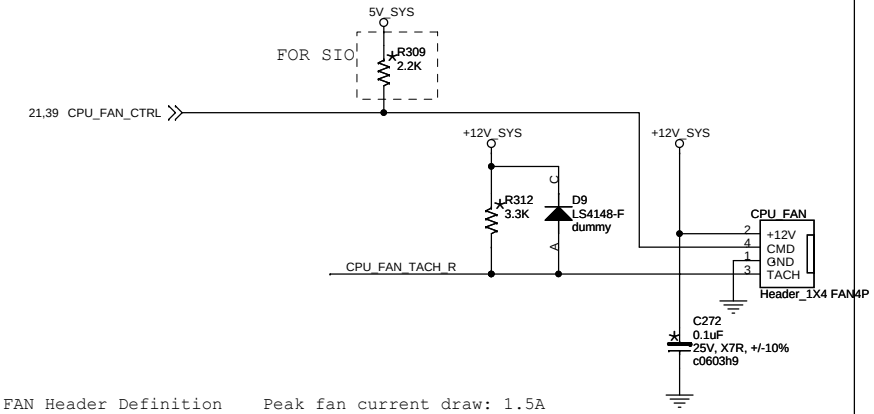
Serial Port



Serial Port



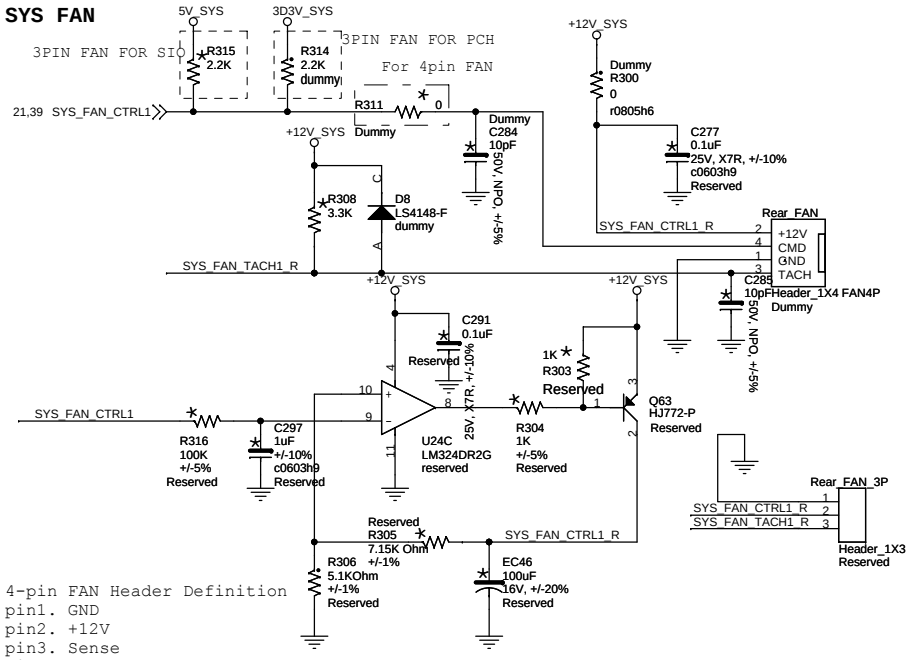
CPU FAN



4-pin FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

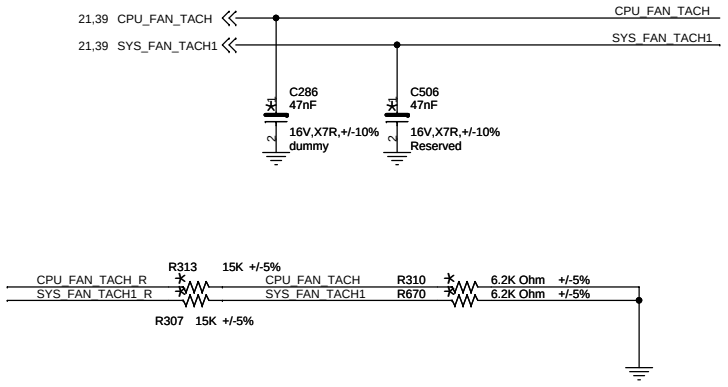
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

SYS FAN



4-pin FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

FAN TACH



FOXCONN PCEG

Title: FAN

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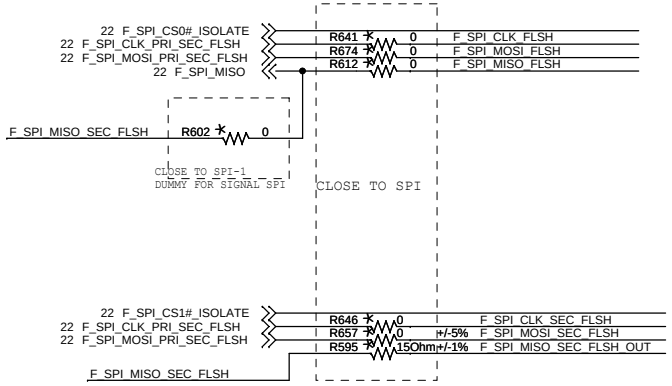
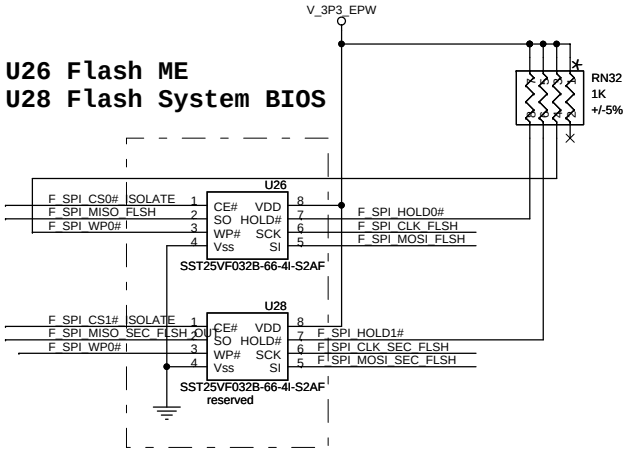
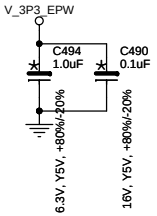
H55,H57 and Q57 SPI ROM size need 8MB for ME6.0 FW

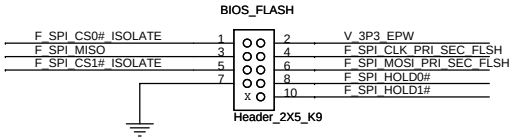


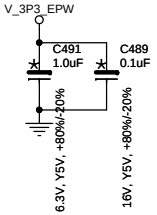
U26 Flash ME
U28 Flash System BIOS

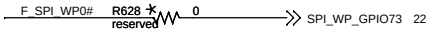


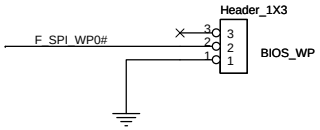
need to change to 64M SPI ROM











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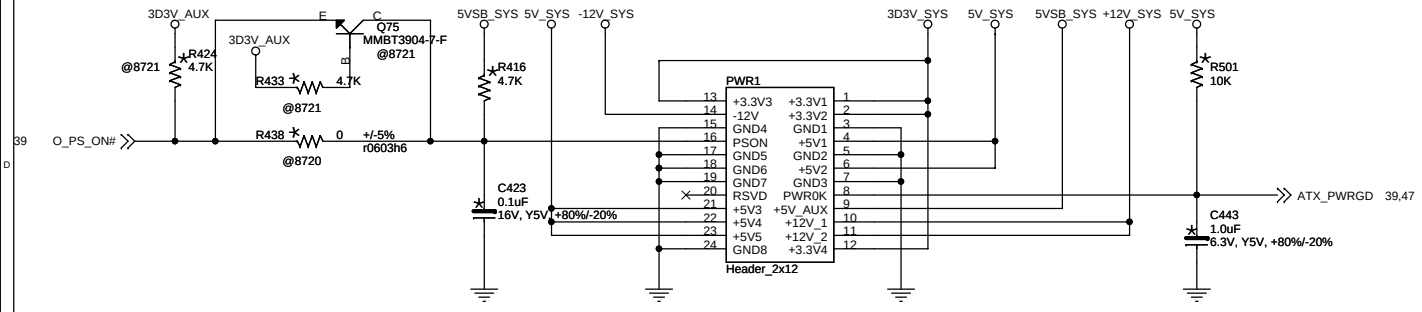
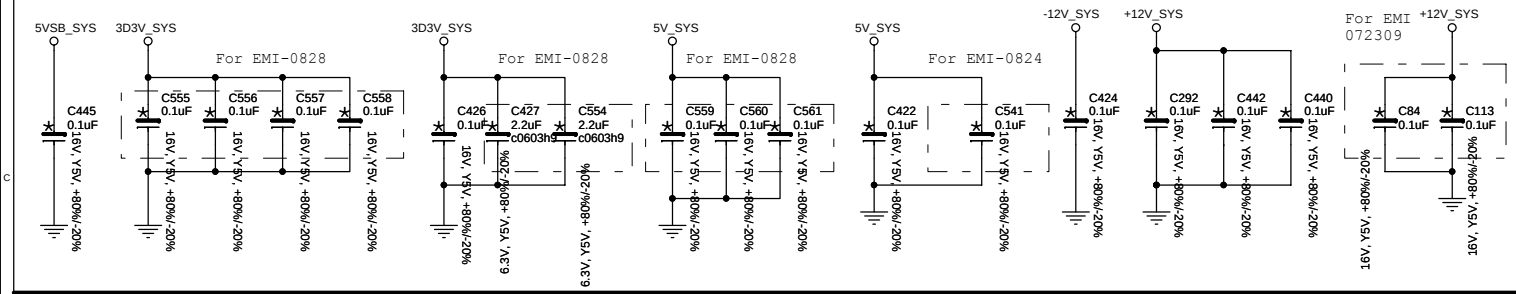
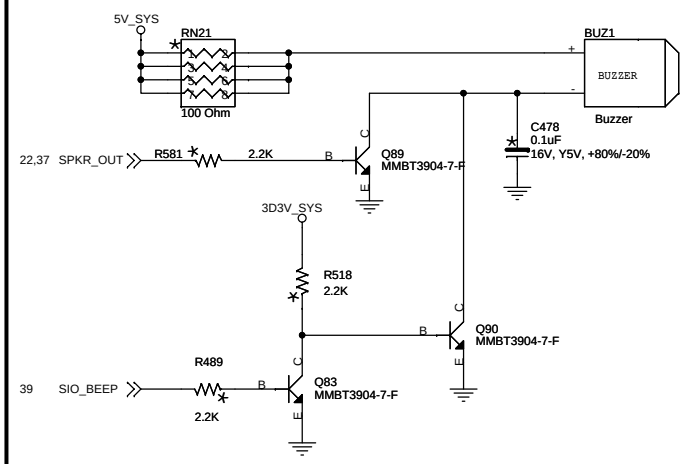
ATX POWER CONNECTOR

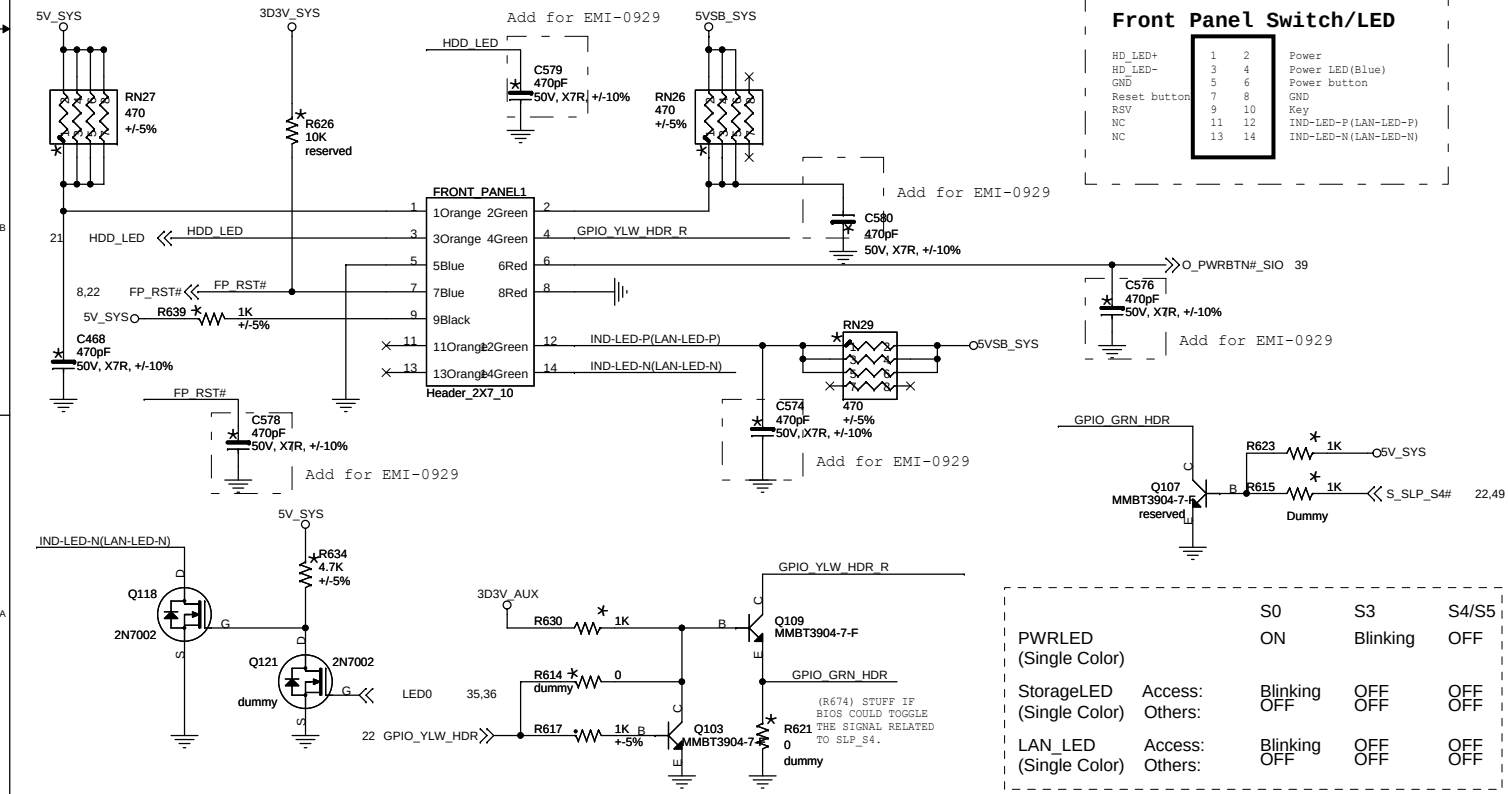




BUZZER



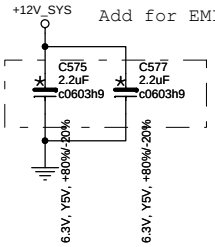
FRONT PANNEL



Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Blue)
GND	5	6	Power button
Reset button	7	8	GND
RSV	9	10	Key
NC	11	12	IND-LED-P(LAN-LED-P)
NC	13	14	IND-LED-N(LAN-LED-N)

		S0	S3	S4/S5
PWRLED (Single Color)		ON	Blinking	OFF
StorageLED (Single Color)	Access:	Blinking	OFF	OFF
	Others:	OFF	OFF	OFF
LAN_LED (Single Color)	Access:	Blinking	OFF	OFF
	Others:	OFF	OFF	OFF



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Title: **ATX/FrontPanel/BUZ**

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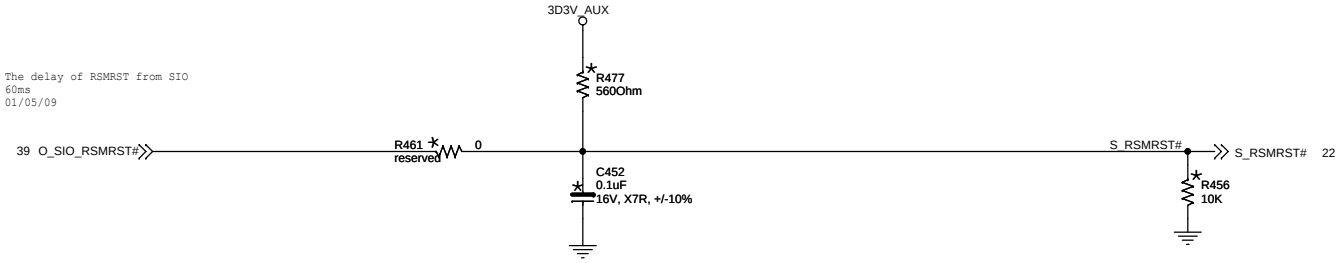
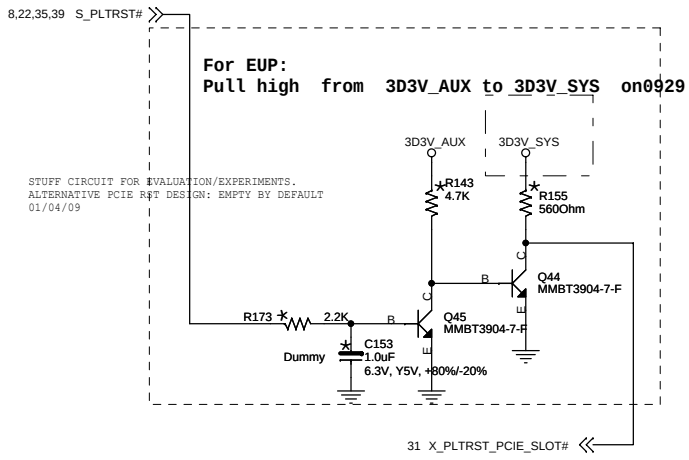
RSMRST

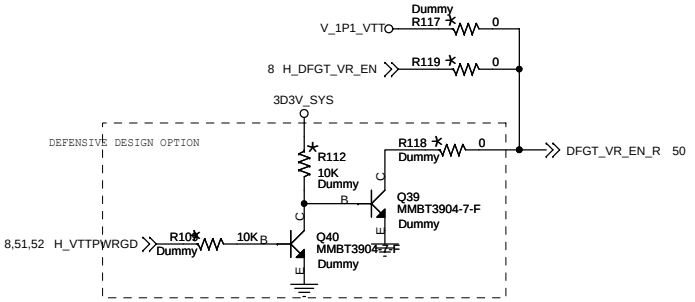
Ibex Peak SPEC:
VccSUS active to RSMRST# inactive.
T201>10ms.
RSMRST# falling edge must transition to 0.8 V or less before VccSus3_3 drops to 2.85V.
01/05/09



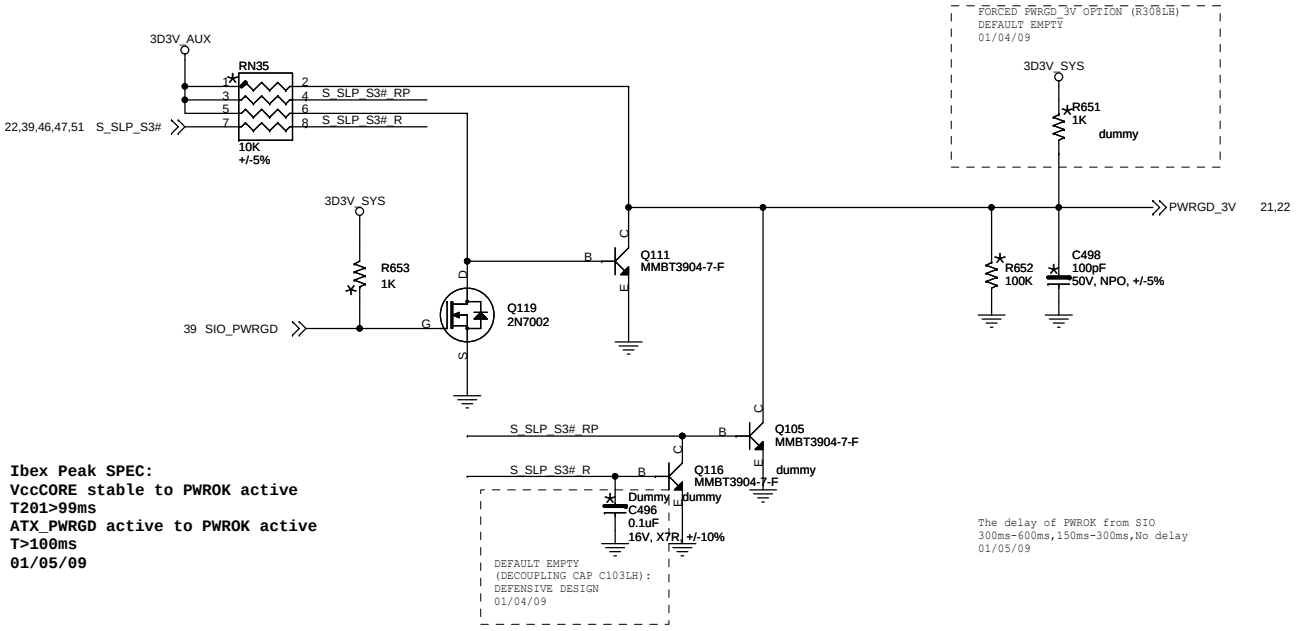
PCI_E1_1X2 RESET



GFX VR ENABLE DEFENSIVE



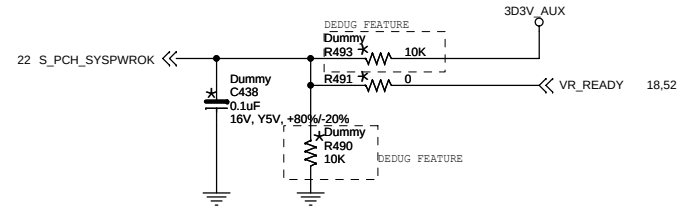
POWER-GOOD 3V



Ibex Peak SPEC:
VccCORE stable to PWROK active
T201>99ms
ATX_PWRGD active to PWROK active
T>100ms
01/05/09

The delay of PWROK from SIO
300ms-600ms,150ms-300ms,No delay
01/05/09

VR_READY DEFENSIVE (PCH POWEROK)



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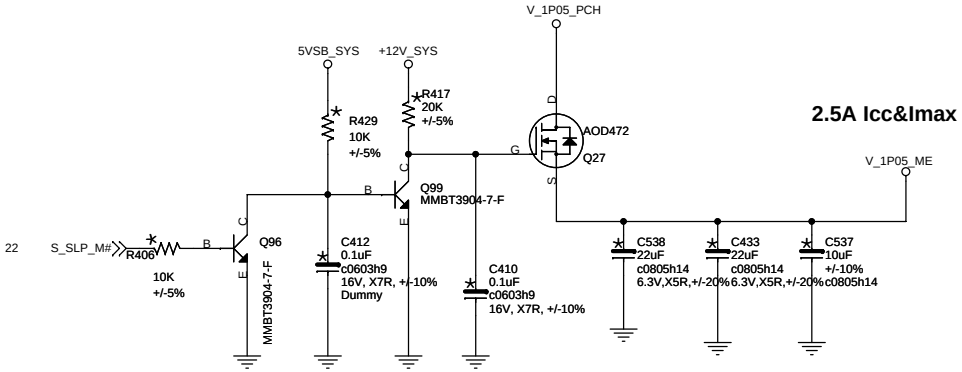
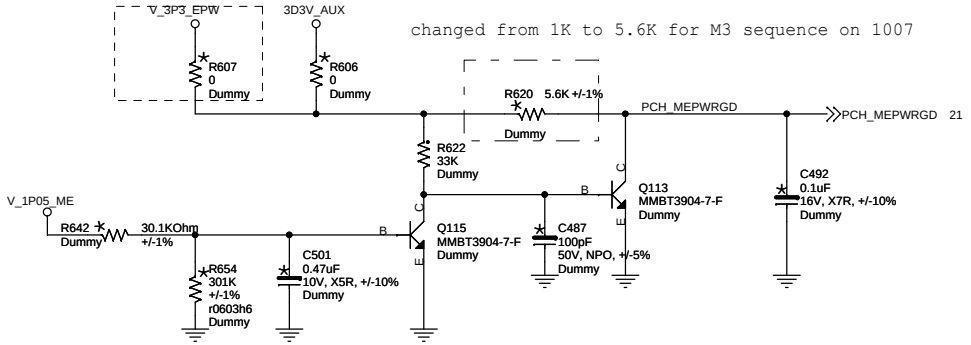
V_1P05_ME

For Non-M3 support directly unstuff



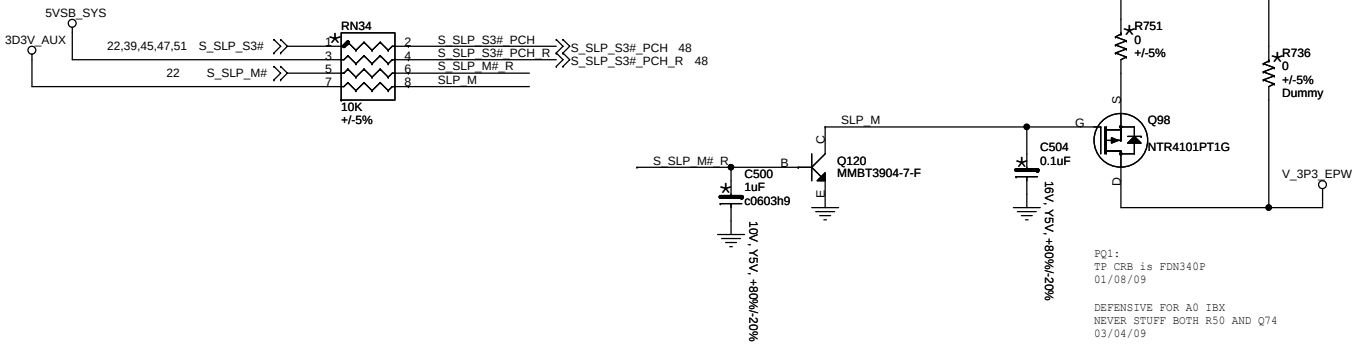
3P3EPW RACE CONDITION DEFENSIVE



For Non-M3 support with third-party LAN:
1.delete V_1P05_ME power,directly connect it to V_1P05_PCH
2.directly connect 3D3V_SYS to V_3P3_EPW
3.VCCLAN directly connect to GND
4.LAN_RST# connect to GND through restor
5.MEPWRGD connect to PWRGD_3V

V_3P3_EPW(FOR PCH ME)

For Non-M3 support, directly connect 3D3V_SYS to V_3P3_EPW
DEFENSIVE DESIGN: 3.3VEPW SUPPLY CONTROL
03/04/09



PQ1:
TP CRB is FDN340P
01/08/09

DEFENSIVE FOR A0 IBX
NEVER STUFF BOTH R50 AND Q74
03/04/09

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Title: ME POWER		
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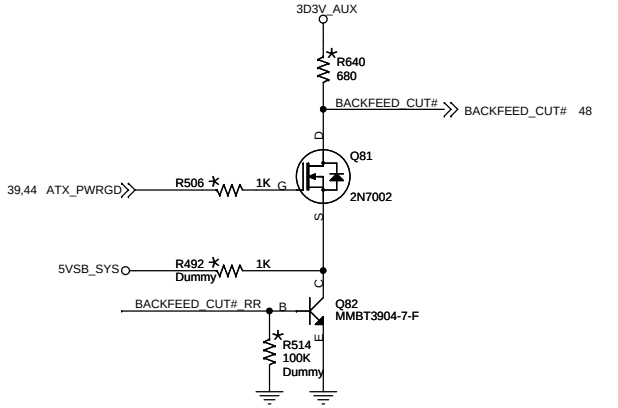
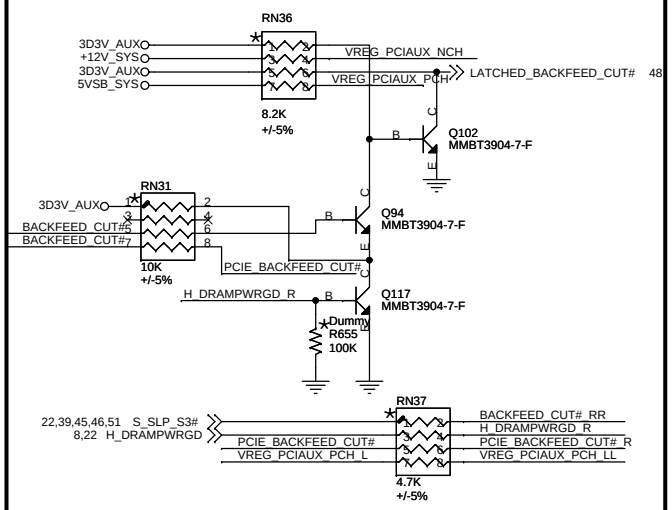
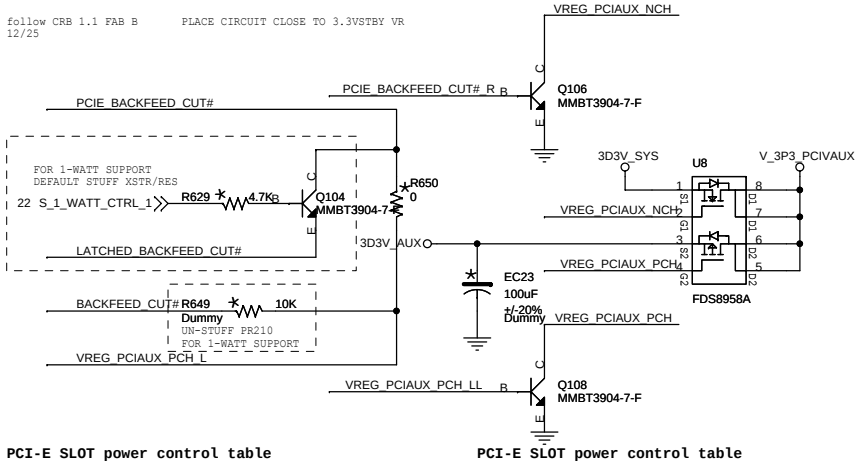
BACKFEED CUT



LATCHED BACKFEED CUT



V_3P3_PCIVAUX(FOR PCI/PCIE SLOT)



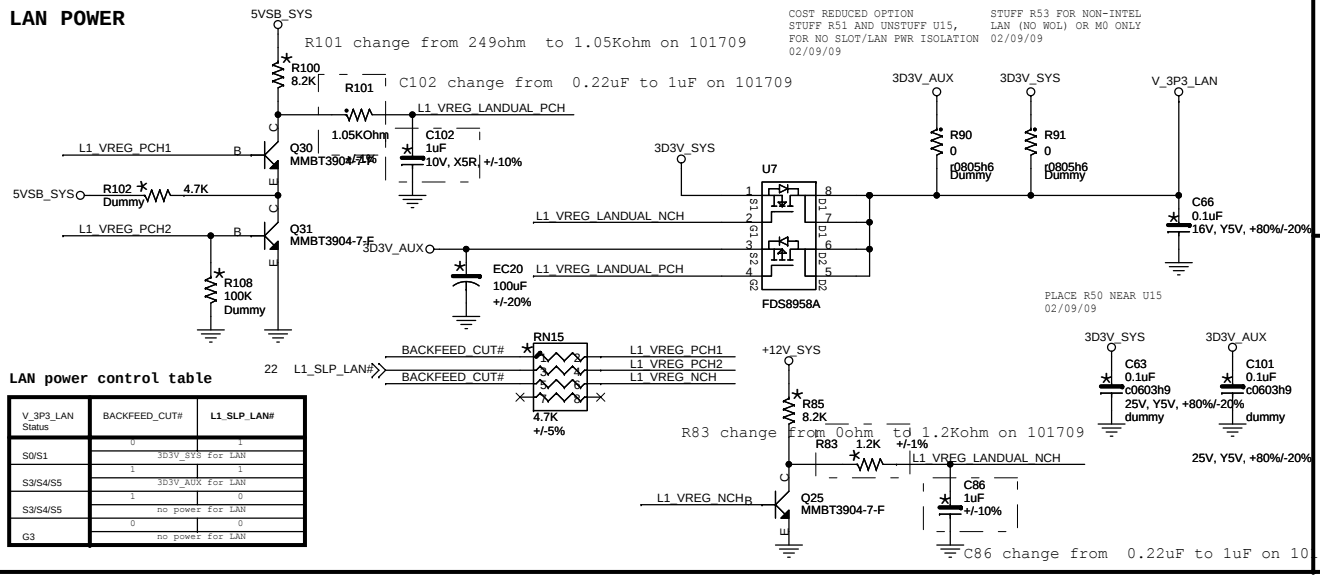
PCI-E SLOT power control table for 1-WATT support

V_3P3_PCIVAUX Status	BACKFEED_CUT#	LATCHED_BACKFEED_CUT#	S_1_WATT_CTRL_1
	0	0	0
S0/S1	3D3V_SYS for PCI-E SLOT		
	1	1	1/0
S3	3D3V_AUX for PCI-E SLOT		
	1	0	0
S4	3D3V_AUX for PCI-E SLOT		
	0	0	1
S4	no power for PCI-E SLOT		
	1	0	0
S5	3D3V_AUX for PCI-E SLOT		
	0	0	1
S5	no power for PCI-E SLOT		
	0	0	0
G3	no power for PCI-E SLOT		

PCI-E SLOT power control table for none 1-WATT support

V_3P3_PCIVAUX Status	BACKFEED_CUT#	LATCHED_BACKFEED_CUT#
	0	0
S0/S1	3D3V_SYS for PCI-E SLOT	
	1	1
S3	3D3V_AUX for PCI-E SLOT	
	1	0
S4	3D3V_AUX for PCI-E SLOT	
	1	0
S5	3D3V_AUX for PCI-E SLOT	
	0	0
G3	no power for PCI-E SLOT	

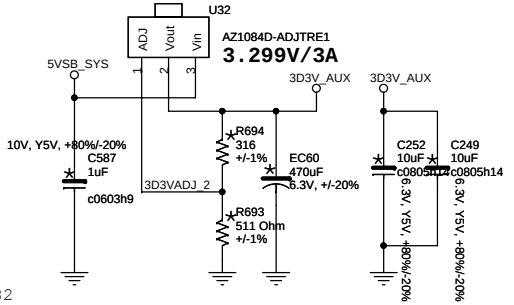
LAN POWER



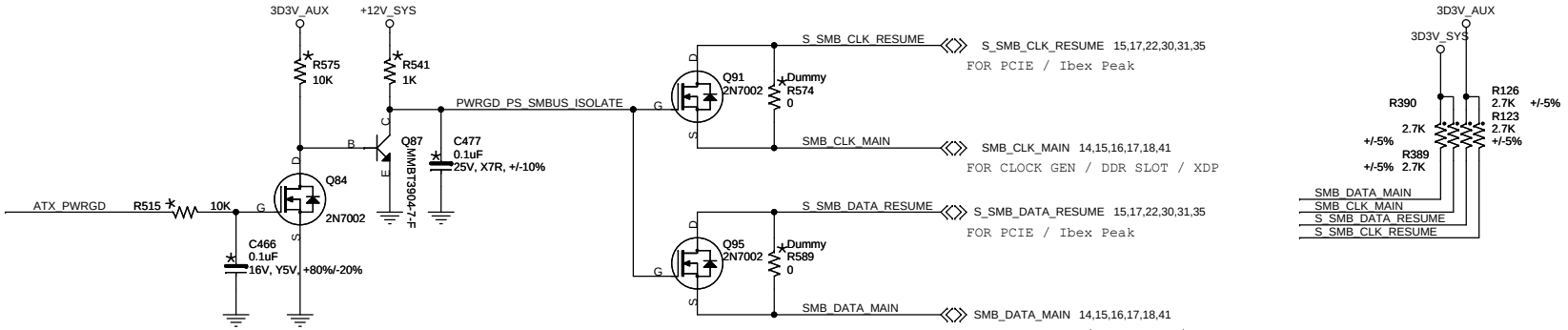
LAN power control table

V_3P3_LAN Status	BACKFEED_CUT#	L1_SLP_LAN#
	0	1
S0/S1	3D3V_SYS for LAN	
	1	1
S3/S4/S5	3D3V_AUX for LAN	
	1	0
S3/S4/S5	no power for LAN	
	0	0
G3	no power for LAN	

3D3V_AUX



SMB ISOLATE



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Title: **POWER-1:LINEAR POWER-1**

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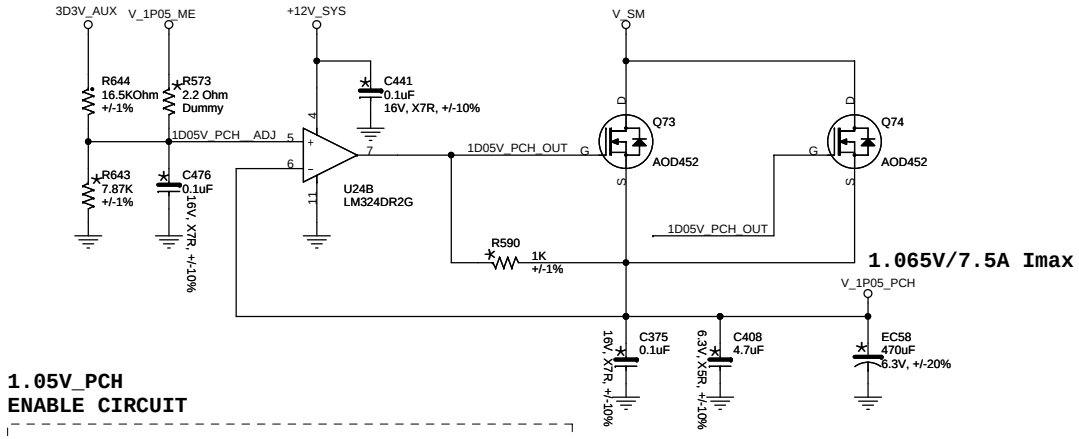
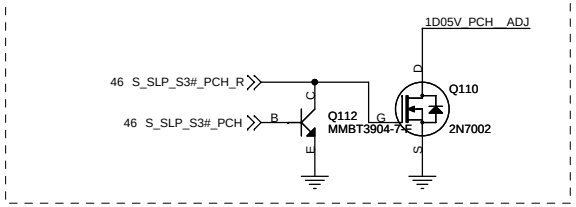
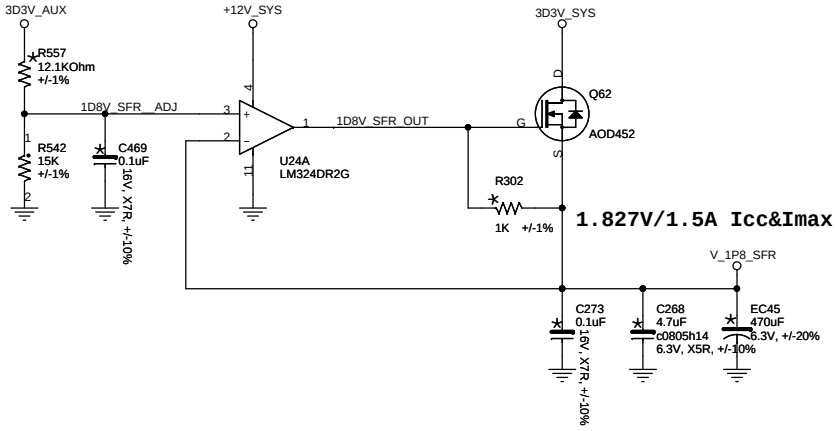
V_1P05_PCH



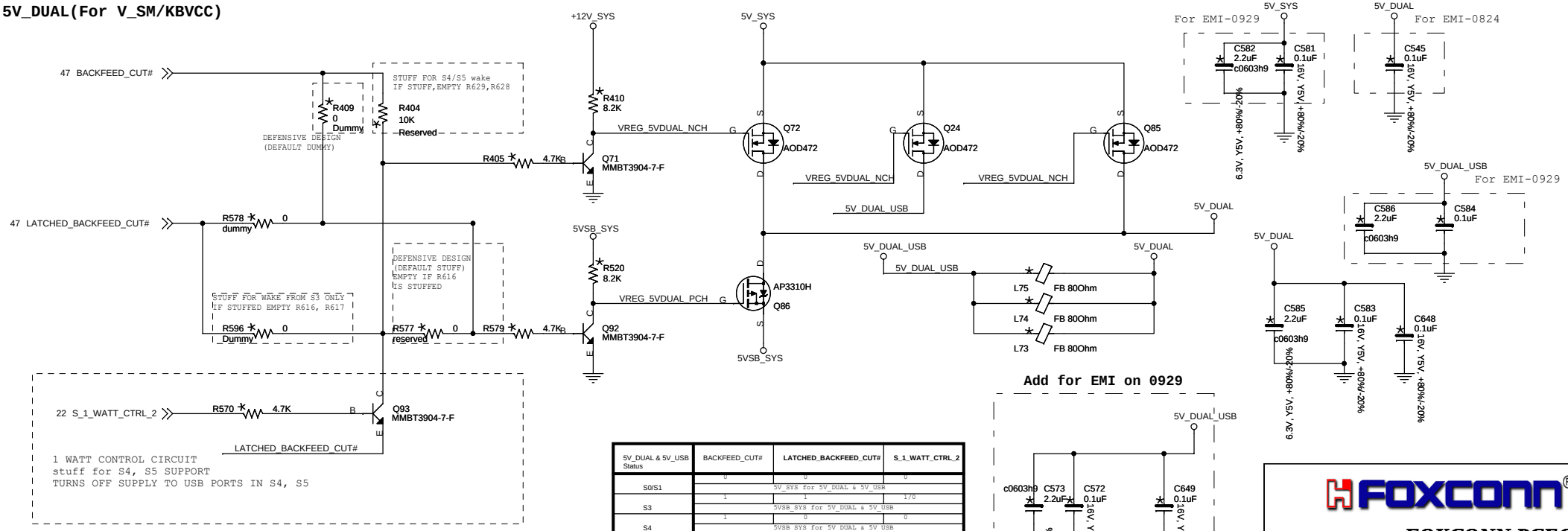
1.05V_PCH ENABLE CIRCUIT



V_1P8_SFR



5V_DUAL(For V_SM/KBVCC)



5V_DUAL & 5V_USB Status	BACKFEED_CUT#	LATCHED_BACKFEED_CUT#	S_1_WATT_CTRL_2
S0/S1	0	0	0
	5V_SYS for 5V_DUAL & 5V_USB		
S3	1	1	1/0
	5VSB_SYS for 5V_DUAL & 5V_USB		
S4	1	0	0
	5VSB_SYS for 5V_DUAL & 5V_USB		
S4	0	0	1
	no power for 5V_DUAL & 5V_USB		
S5	1	0	0
	5VSB_SYS for 5V_DUAL & 5V_USB		
S5	0	0	1
	no power for 5V_DUAL & 5V_USB		
G3	0	0	0
	no power for 5V_DUAL & 5V_USB		

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Title: POWER-2:LINEAR POWER-2

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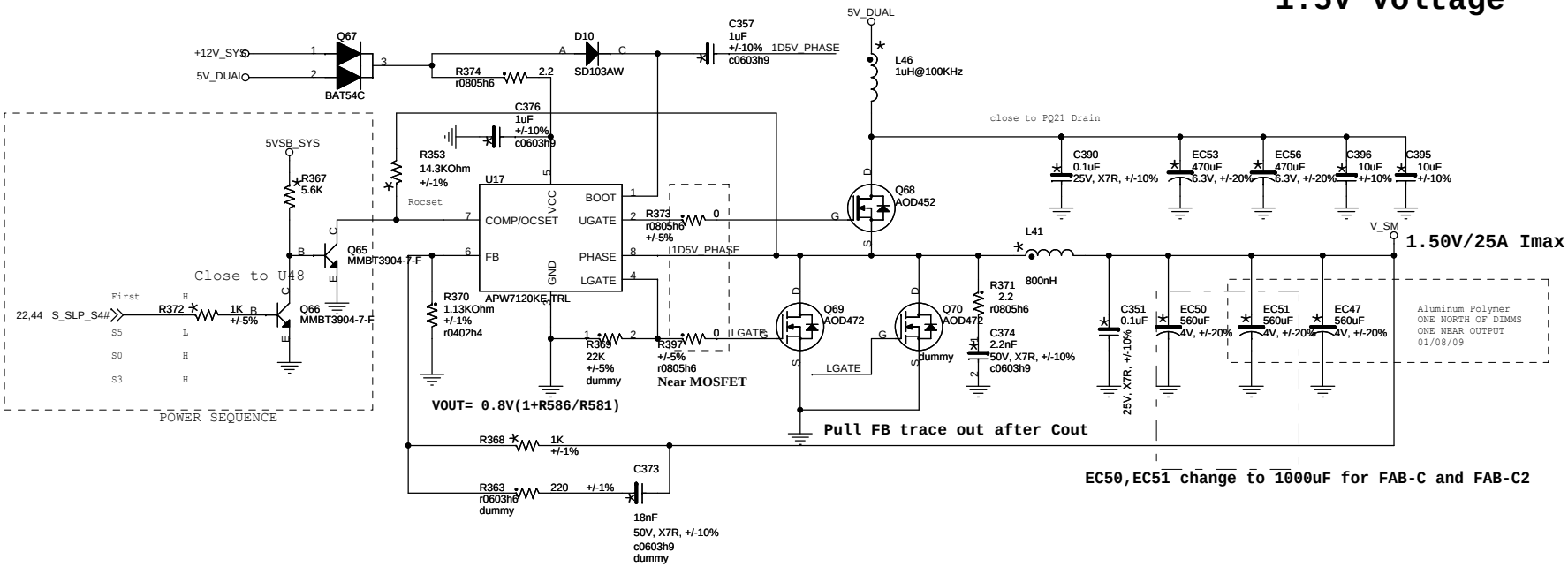
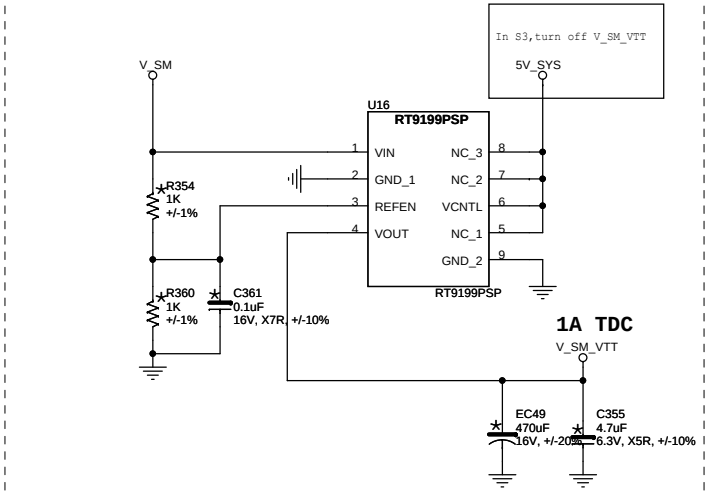
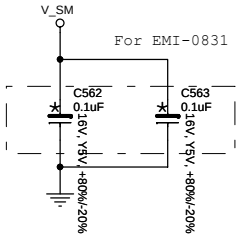
V_SM FOR DDRIII(1.5V)



V_SM_VTT FOR DDRIII(0.75V)





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Title: POWER-3:V_SM		
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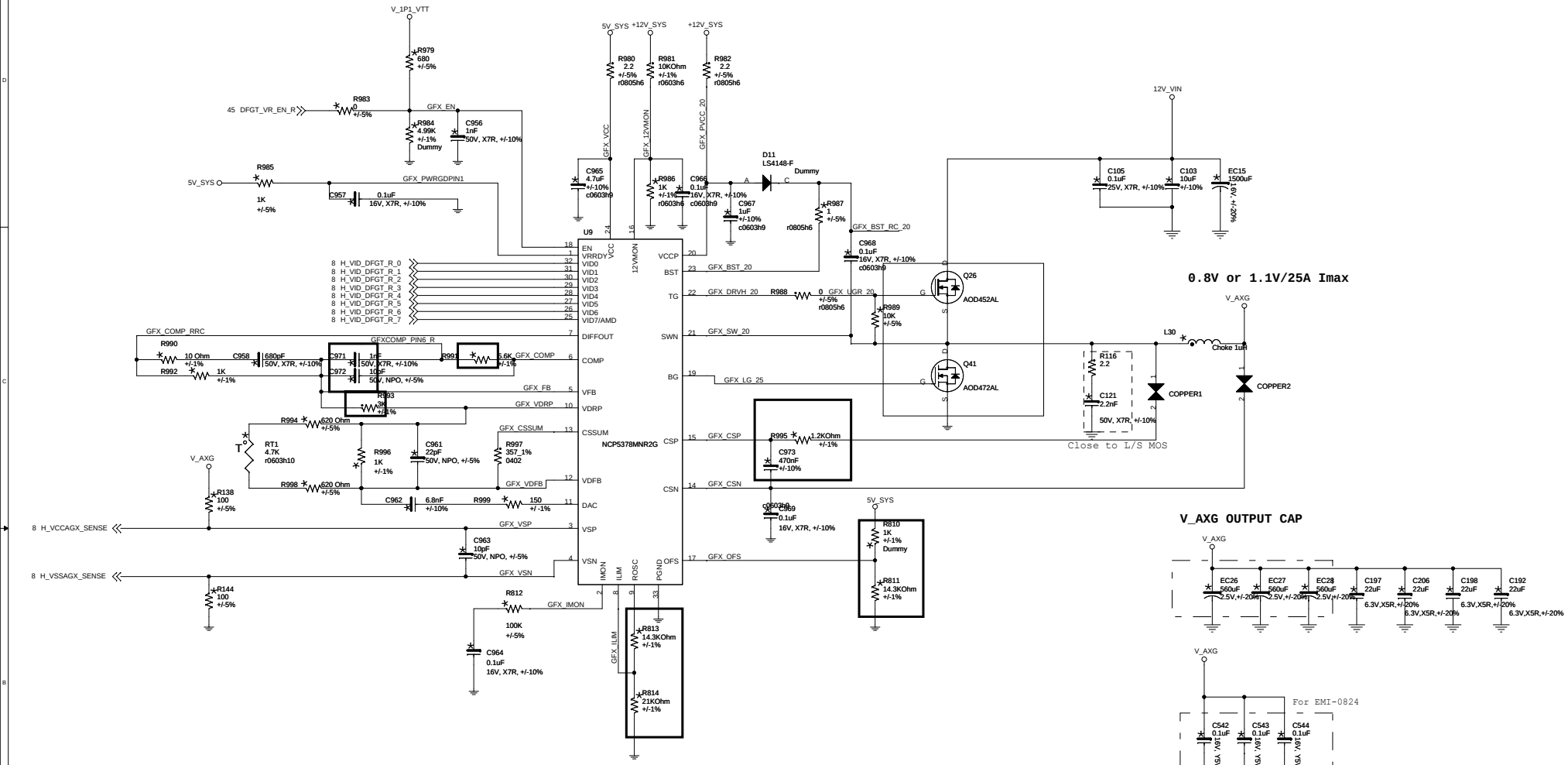
VAXG(1.1V)



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Title	POWER-4:VAXG	
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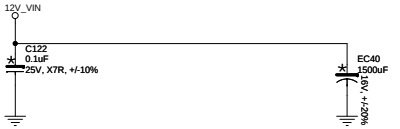
V_1P1_VTT(1.1V)

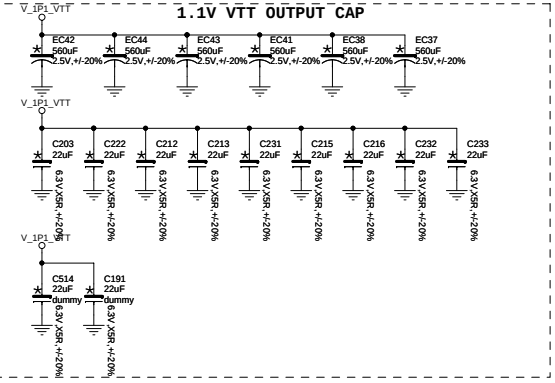
MLCC 22uF x 20%
5pcs in the southeast corner of the socket cavity,
4pcs in the west side of socket
01/08/09
Aluminum Polymer
5pcs East side by the output of the VR
1pcs West side of the socket
01/08/09

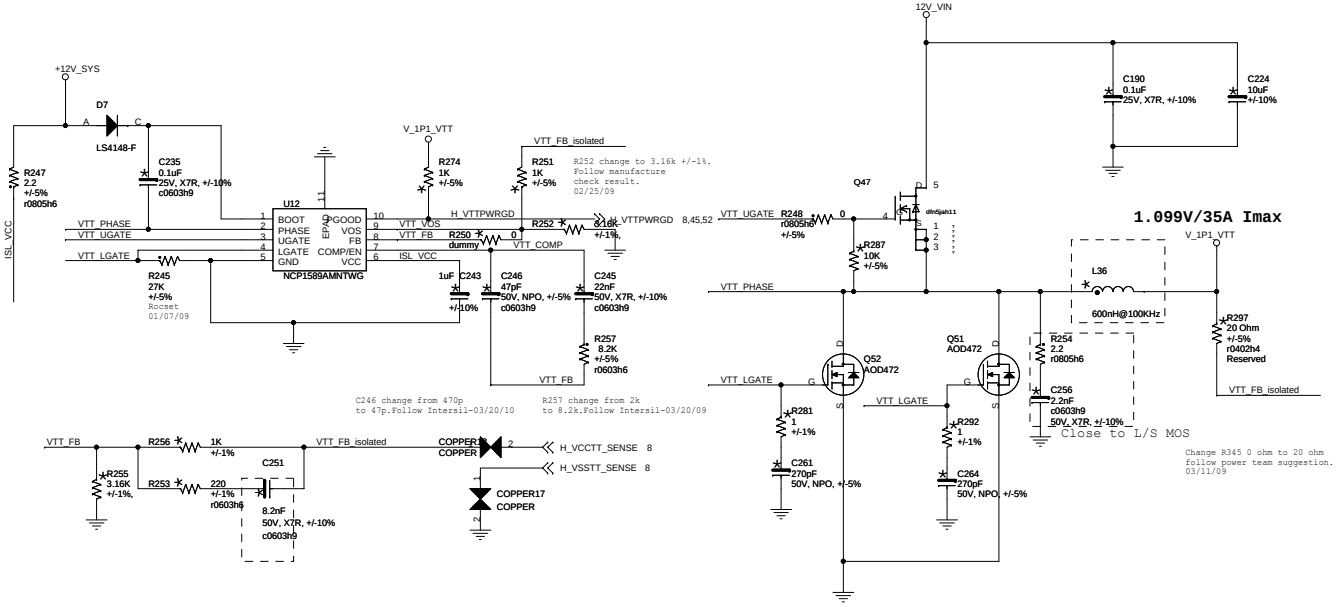
1pcs MLCC(dummy)C11VR PLACED ON BACKSIDE OF THE BOARD
01/08/09

Input LC circuit

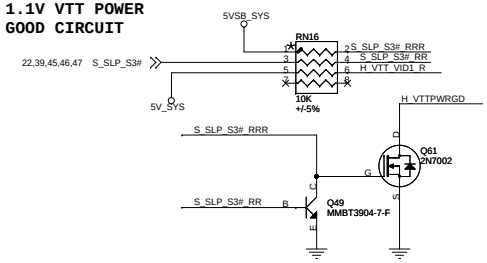


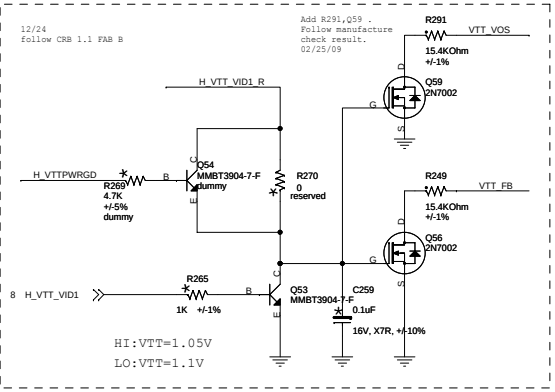
1.1V VTT OUTPUT CAP





1.1V VTT POWER GOOD CIRCUIT





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Title	POWER-5:VTT		
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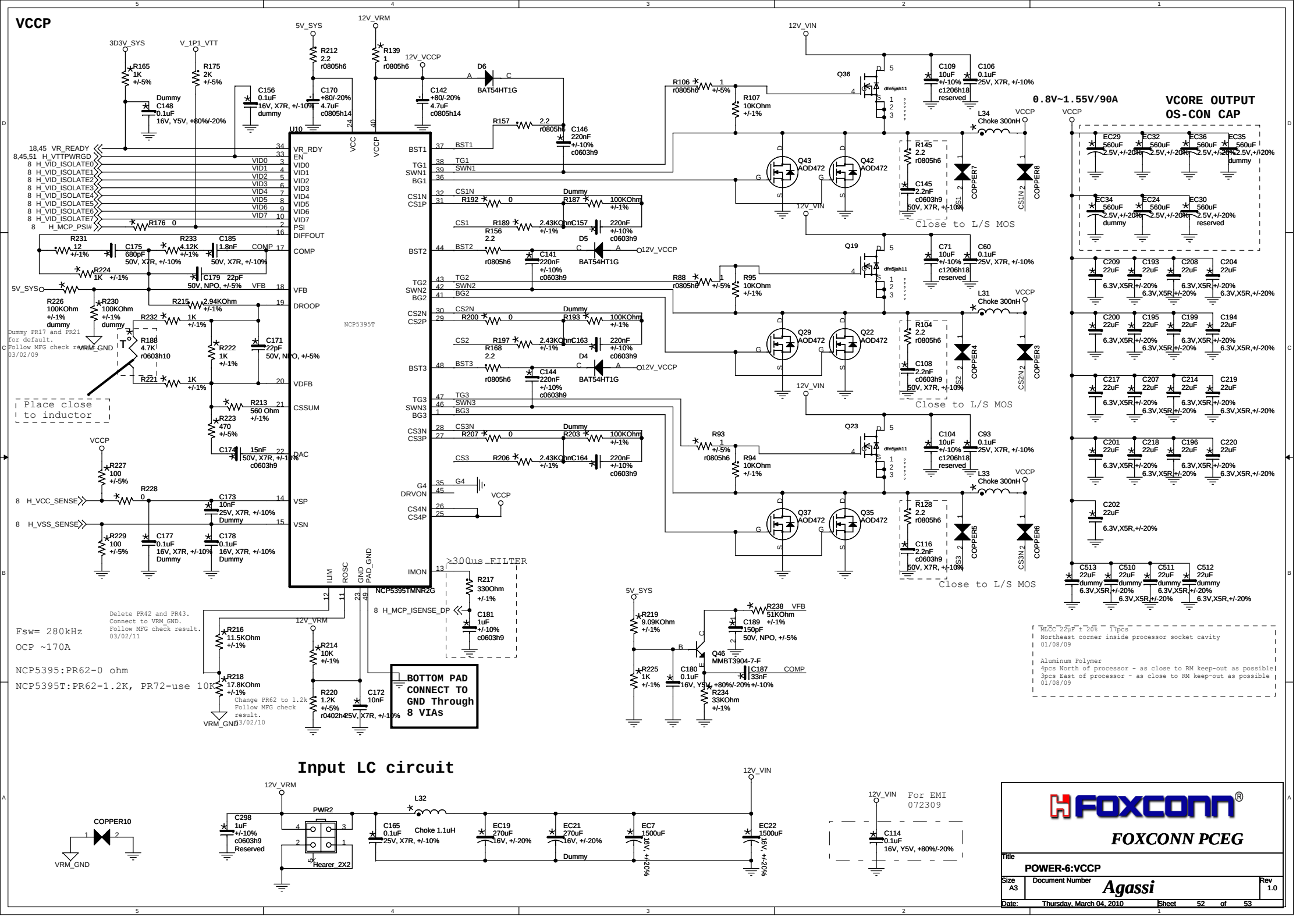
VCCP



Input LC circuit

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FOXCONN PCEG

Title: POWER-6:VCCP		
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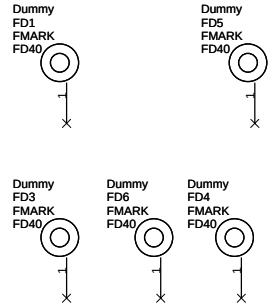
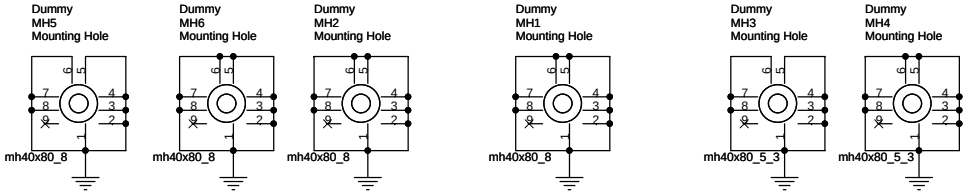
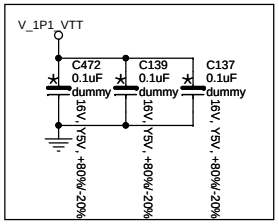
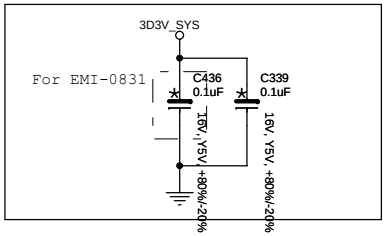




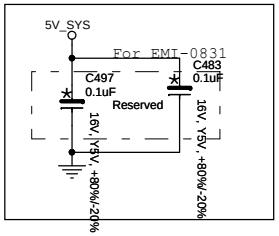
Stitch for DMI reference plane



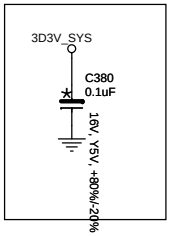
Stitch for 96M clock reference plane

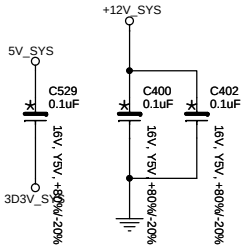


Stitch for LAN PCIE/Clock difference reference plane



Stitch for PCICLK





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