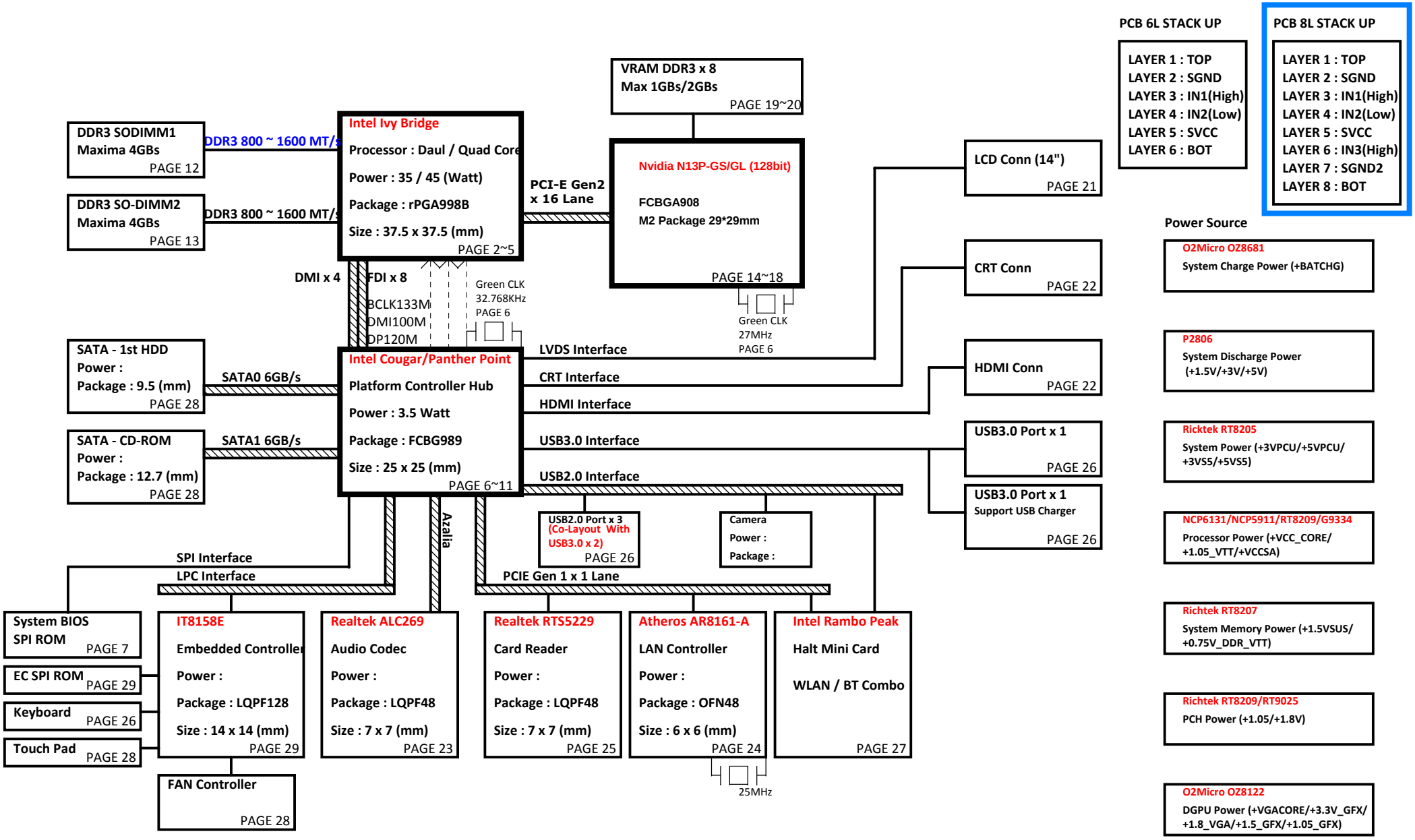
# JW2 DIS (14") Intel Chief River Platform Block Diagram 01




| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size A3 | Document Number<br>Block Diagram | Rev D A |
| Date: Wednesday, November 02, 2011 | Sheet 1 of 40 | |

# Ivy Bridge Processor (DMI,PEG,FDI)

# Ivy Bridge Processor (CLK,MISC,JTAG)

**02**

U15A

DMI_TXN0 [6] B27 DMI_RX#[0]
DMI_TXN1 [6] B25 DMI_RX#[1]
DMI_TXN2 [6] A25 DMI_RX#[2]
DMI_TXN3 [6] B24 DMI_RX#[3]
DMI_TXP0 [6] B28 DMI_RX[0]
DMI_TXP1 [6] B26 DMI_RX[1]
DMI_TXP2 [6] A24 DMI_RX[2]
DMI_TXP3 [6] B23 DMI_RX[3]
DMI_RXN0 [6] G21 DMI_TX#[0]
DMI_RXN1 [6] E22 DMI_TX#[1]
DMI_RXN2 [6] F21 DMI_TX#[2]
DMI_RXN3 [6] D21 DMI_TX#[3]
DMI_RXP0 [6] G22 DMI_TX[0]
DMI_RXP1 [6] D22 DMI_TX[1]
DMI_RXP2 [6] F20 DMI_TX[2]
DMI_RXP3 [6] C21 DMI_TX[3]

DMI

FDI_TXN0 [6] A21 FDI0_TX#[0]
FDI_TXN1 [6] H19 FDI0_TX#[1]
FDI_TXN2 [6] E19 FDI0_TX#[2]
FDI_TXN3 [6] F18 FDI0_TX#[3]
FDI_TXN4 [6] B21 FDI1_TX#[0]
FDI_TXN5 [6] C20 FDI1_TX#[1]
FDI_TXN6 [6] D18 FDI1_TX#[2]
FDI_TXN7 [6] E17 FDI1_TX#[3]
FDI_TXP0 [6] A22 FDI0_TX[0]
FDI_TXP1 [6] G19 FDI0_TX[1]
FDI_TXP2 [6] E20 FDI0_TX[2]
FDI_TXP3 [6] G18 FDI0_TX[3]
FDI_TXP4 [6] B20 FDI1_TX[0]
FDI_TXP5 [6] C19 FDI1_TX[1]
FDI_TXP6 [6] D19 FDI1_TX[2]
FDI_TXP7 [6] F17 FDI1_TX[3]
FDI_FSYNC0 [6] J18 FDI0_FSYNC
FDI_FSYNC1 [6] J17 FDI1_FSYNC
FDI_INT [6] H20 FDI_INT
FDI_LSYNC0 [6] J19 FDI0_LSYNC
FDI_LSYNC1 [6] H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP A18 eDP_COMPIO
INT_eDP_HPD_Q A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

eDP

Ivy Bridge_rPGA_2DPC_Rev0p61

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_COMP

PEG_RX#[0] K33
PEG_RX#[1] M35
PEG_RX#[2] L34
PEG_RX#[3] J35
PEG_RX#[4] J32
PEG_RX#[5] H34
PEG_RX#[6] H31
PEG_RX#[7] G33
PEG_RX#[8] G30
PEG_RX#[9] F35
PEG_RX#[10] E34
PEG_RX#[11] E32
PEG_RX#[12] D33
PEG_RX#[13] D31
PEG_RX#[14] B33
PEG_RX#[15] C32

PEG_RX[0] J33
PEG_RX[1] L35
PEG_RX[2] K34
PEG_RX[3] H35
PEG_RX[4] H32
PEG_RX[5] G34
PEG_RX[6] G31
PEG_RX[7] E33
PEG_RX[8] E30
PEG_RX[9] E35
PEG_RX[10] E33
PEG_RX[11] F32
PEG_RX[12] D34
PEG_RX[13] E31
PEG_RX[14] C33
PEG_RX[15] B32

PEG_TX#[0] M29
PEG_TX#[1] M32
PEG_TX#[2] M31
PEG_TX#[3] L32
PEG_TX#[4] L29
PEG_TX#[5] K31
PEG_TX#[6] K28
PEG_TX#[7] J30
PEG_TX#[8] J28
PEG_TX#[9] H29
PEG_TX#[10] G27
PEG_TX#[11] E29
PEG_TX#[12] F27
PEG_TX#[13] D28
PEG_TX#[14] F26
PEG_TX#[15] E25

PEG_TX[0] M28
PEG_TX[1] M33
PEG_TX[2] M30
PEG_TX[3] L31
PEG_TX[4] L28
PEG_TX[5] K30
PEG_TX[6] K27
PEG_TX[7] J29
PEG_TX[8] J27
PEG_TX[9] H28
PEG_TX[10] G28
PEG_TX[11] E28
PEG_TX[12] F28
PEG_TX[13] D27
PEG_TX[14] E26
PEG_TX[15] D25

PCI EXPRESS* - GRAPHICS

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0..15] [14]
PEG_RX[0..15] [14]

[7] H_SNB_IVB# → C26 PROC_SELECT#
SNB_IVB# N.A at SNB EDS #27637 0.7v1
TP24 SKTOCC# AN34
TP25 TP_CATERR# AL33 CATERR#
Placement close to EC.
[29] H_PECI H_PECI AN33 PECI
[29,38] H_PROCHOT# R161 56_4 H_PROCHOT#_R AL32 PROCHOT#
C493 43P/50V_4 close to VR side
AN32 THERMTRIP#
[9,29] PM_THRMTRIP# PM_THRMTRIP#

MISC
THERMAL

[6] PM_SYNC R469 0_4 PM_SYNC_R AM34 PM_SYNC
8/31 reserved for "boot hang 47" issue
C614 *0.1U/10V_4
[9] H_PWRGOOD H_PWRGOOD AP33 UNCOREPWRGOOD
R473 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
Intel DG request

CPU RESET#

[8,14,24,25,27,29] PLTRST# R480 1.5K/F_4 AR33 RESET#
20110816 modify:
REGULATOR DEL FOR SHORT
R476 750/F_4

SM_DRAMPWROK
Processor Input.

PWR MANAGEMENT

Ivy Bridge_rPGA_2DPC_Rev0p61

CLOCKS

BCLK A28 CLK_CPU_BCLKP [8]
BCLK# A27 CLK_CPU_BCLKN [8]
DPLL_REF_CLK A16 CLK_DPLL_SSCLKP_R
DPLL_REF_CLK# A15 CLK_DPLL_SSCLKN_R

DDR3 MISC

SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R136 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R411 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R410 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM

PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI_R
TDO AP26 XDP_TDO
DBR# AL35 XDP_DBRST#
BPM#[0] AT28 XDP_BPM0
BPM#[1] AR29 XDP_BPM1
BPM#[2] AR30 XDP_BPM2
BPM#[3] AT30 XDP_BPM3
BPM#[4] AP32 XDP_BPM4
BPM#[5] AR31 XDP_BPM5
BPM#[6] AT31 XDP_BPM6
BPM#[7] AR32 XDP_BPM7

CPU XDP
TP66 TP29 TP64 TP60 TP65 TP28 TP61 TP30 TP31 TP59 TP62 TP26 TP58 TP63 TP57
R468 *1K_4 +3V
XDP_DBRST# [6]

## DDR3 DRAM RESET

+1.5VSUS R75 1K_4
[12,13] DDR3_DRAMRST# R68 1K_4
CPU_DRAMRST#_R
Q21 2N7002
CPU_DRAMRST#
[8,12,13] DRAMRST_CNTRL_PCH
R77 4.99K/F_4
C115 0.047U/10V_4

+1.5V_CPU
R516 200/F_4
[6] PM_DRAM_PWRGD
PM_DRAM_PWRGD R146 *39_4 R141 130/F_4 PM_DRAM_PWRGD_R
20110816 modify:
REGULATOR DEL FOR SHORT
R139 *3K/F_4
Q26 *2N7002
MAIN_ONG [4,40]

[6,7,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,34,36,38,40] +3V
[6,7,8,9,10,29,31,34,35,37,40] +3VS5
[4,10,27] +1.5V_CPU
[4,6,7,8,10,29,34,37,38] +1.05V

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

## FDI disable (DIS only stuff)

20110816 modify:
FDI DEL FOR SG

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

## PEG x16 disable (UMA only remove)

[14] PEG_TX[0..15]

| | | | | | |
|---|---|---|---|---|---|
| C_PEG_TX0 | C631 | 0.22U/10V_4 | PEG_TX0 | C_PEG_TX#0 | C634 | 0.22U/10V_4 | PEG_TX#0 |
| C_PEG_TX1 | C626 | 0.22U/10V_4 | PEG_TX1 | C_PEG_TX#1 | C628 | 0.22U/10V_4 | PEG_TX#1 |
| C_PEG_TX2 | C625 | 0.22U/10V_4 | PEG_TX2 | C_PEG_TX#2 | C627 | 0.22U/10V_4 | PEG_TX#2 |
| C_PEG_TX3 | C623 | 0.22U/10V_4 | PEG_TX3 | C_PEG_TX#3 | C624 | 0.22U/10V_4 | PEG_TX#3 |
| C_PEG_TX4 | C619 | 0.22U/10V_4 | PEG_TX4 | C_PEG_TX#4 | C620 | 0.22U/10V_4 | PEG_TX#4 |
| C_PEG_TX5 | C621 | 0.22U/10V_4 | PEG_TX5 | C_PEG_TX#5 | C622 | 0.22U/10V_4 | PEG_TX#5 |
| C_PEG_TX6 | C612 | 0.22U/10V_4 | PEG_TX6 | C_PEG_TX#6 | C616 | 0.22U/10V_4 | PEG_TX#6 |
| C_PEG_TX7 | C615 | 0.22U/10V_4 | PEG_TX7 | C_PEG_TX#7 | C618 | 0.22U/10V_4 | PEG_TX#7 |
| C_PEG_TX8 | C607 | 0.22U/10V_4 | PEG_TX8 | C_PEG_TX#8 | C610 | 0.22U/10V_4 | PEG_TX#8 |
| C_PEG_TX9 | C609 | 0.22U/10V_4 | PEG_TX9 | C_PEG_TX#9 | C611 | 0.22U/10V_4 | PEG_TX#9 |
| C_PEG_TX10 | C601 | 0.22U/10V_4 | PEG_TX10 | C_PEG_TX#10 | C604 | 0.22U/10V_4 | PEG_TX#10 |
| C_PEG_TX11 | C603 | 0.22U/10V_4 | PEG_TX11 | C_PEG_TX#11 | C606 | 0.22U/10V_4 | PEG_TX#11 |
| C_PEG_TX12 | C594 | 0.22U/10V_4 | PEG_TX12 | C_PEG_TX#12 | C602 | 0.22U/10V_4 | PEG_TX#12 |
| C_PEG_TX13 | C593 | 0.22U/10V_4 | PEG_TX13 | C_PEG_TX#13 | C597 | 0.22U/10V_4 | PEG_TX#13 |
| C_PEG_TX14 | C583 | 0.22U/10V_4 | PEG_TX14 | C_PEG_TX#14 | C592 | 0.22U/10V_4 | PEG_TX#14 |
| C_PEG_TX15 | C580 | 0.22U/10V_4 | PEG_TX15 | C_PEG_TX#15 | C590 | 0.22U/10V_4 | PEG_TX#15 |

0.22uF AC coupling Caps for PCIE GEN3

0.22uF AC coupling Caps for PCIE GEN3

## Embedded Display PLL Clock

CLK_DPLL_SSCLKP_R R413 1K_4
CLK_DPLL_SSCLKN_R R402 1K_4 +1.05V
Intel DG.

20110816 CLK DPLL_SSCLK DEL

## DP & PEG Compensation

+1.05V R404 *10K_4 INT_eDP_HPD_Q
+1.05V R405 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V R88 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up (CPU)

Ver B Modify

+1.05V

| | | |
|---|---|---|
| H_PROCHOT# | R163 | 62_4 |
| XDP_TDO | R489 | 51_4 |
| XDP_TMS | R490 | 51_4 |
| XDP_TDI_R | R155 | 51_4 |
| XDP_PREQ# | R157 | *51_4 |
| XDP_TCLK | R158 | 51_4 |
| XDP_TRST# | R491 | 51_4 |

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | Processor 1/4 (Host/GPU) | A |

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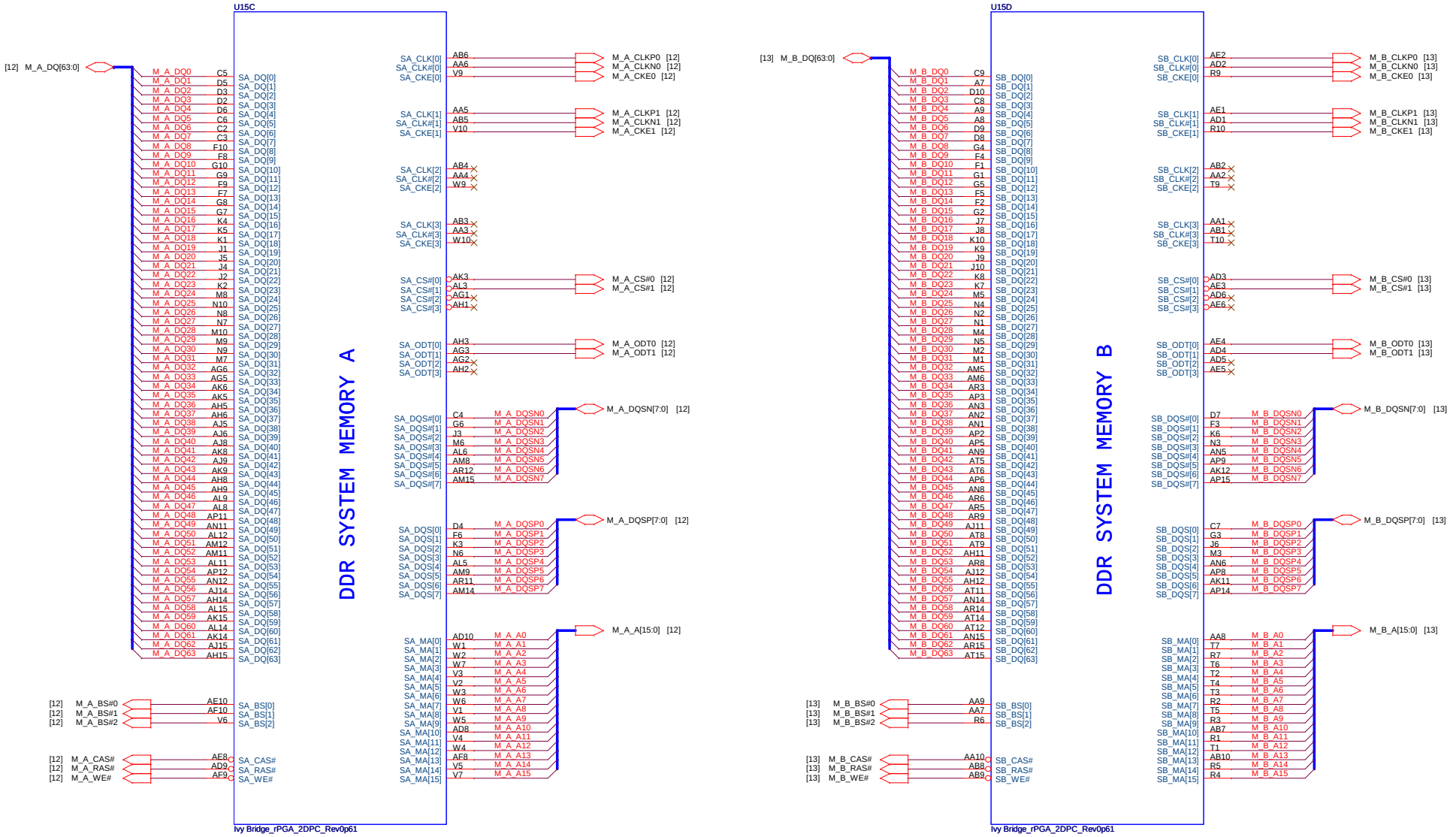
# Ivy Bridge Processor (DDR3)






NB5

**PROJECT : JW2**

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 2/4 (Memory) | D A |

Date: Wednesday, November 02, 2011 | Sheet 3 of 40

# Ivy Bridge Processor

04

## POWER

U15F

### CORE SUPPLY

SNB: 55A
IVY: 55A

+VCC_CORE

C211 22U/6.3VS_8, C100 22U/6.3VS_8, C124 22U/6.3VS_8
C569 22U/6.3VS_8, C570 22U/6.3VS_8, C182 22U/6.3VS_8
C116 22U/6.3VS_8, C510 22U/6.3VS_8, C141 22U/6.3VS_8
C212 22U/6.3VS_8, C165 22U/6.3VS_8, C145 22U/6.3VS_8
C179 22U/6.3VS_8, C50 *22U/6.3VS_8, C98 22U/6.3VS_8
C135 22U/6.3VS_8, C119 22U/6.3VS_8, C158 22U/6.3VS_8
C130 22U/6.3VS_8, C133 22U/6.3VS_8, C147 22U/6.3VS_8
C560 *22U/6.3VS_8, C81 *22U/6.3VS_8, C577 22U/6.3VS_8
C503 22U/6.3VS_8, C506 22U/6.3VS_8, C160 22U/6.3VS_8
C587 22U/6.3VS_8, C578 22U/6.3VS_8, C567 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

[7,10,35] +1.8V
[33] +VCCSA
[2,12,13,32,37] +1.5VSUS
[39] +VCC_GFX
[2,10,27] +1.5V_CPU
[39] +VCC_CORE

Ivy Bridge_rPGA_2DPC_Rev0p61

### PEG AND DDR

SNB: 8.5A
IVY: 8.5A

+1.05V

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C507 22U/6.3VS_8, C204 22U/6.3VS_8, C551 22U/6.3VS_8
C157 22U/6.3VS_8, C512 22U/6.3VS_8, C99 22U/6.3VS_8
C504 *22U/6.3VS_8, C131 22U/6.3VS_8, C579 22U/6.3VS_8
C586 *22U/6.3VS_8, C120 22U/6.3VS_8, C111 *22U/6.3VS_8
C546 22U/6.3VS_8, C97 *10U/6.3V_6 (5/14 modify), C181 *22U/6.3VS_8
C545 *22U/6.3VS_8, C555 22U/6.3VS_8, C142 *22U/6.3VS_8
C571 *22U/6.3VS_8, C561 22U/6.3VS_8, C109 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V

### SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VR_SVID_CLK
VIDSOUT AJ28 VR_SVID_DATA

### SENSE LINES

VCC_SENSE AJ35 — R131 100_4 — +VCC_CORE
VSS_SENSE AJ34 — VCC_SENSE [38], VSS_SENSE [38]
R135 100_4
VCCIO_SENSE B10 — VCCP_SENSE — VCCP_SENSE [34]
VSS_SENSE_VCCIO A10 — VSSP_SENSE — VSSP_SENSE [34]

Trace Route to Power IC area.

+1.05V
VCCP_SENSE R55 10/F_4
VSSP_SENSE R56 10/F_4

U15G

### GRAPHICS

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX

SNB: 21.5A
IVY: 38A

C582 22U/6.3VS_8, C294 22U/6.3VS_8
C213 22U/6.3VS_8, C214 22U/6.3VS_8
C633 22U/6.3VS_8, C630 22U/6.3VS_8
C217 22U/6.3VS_8, C291 22U/6.3VS_8
C632 22U/6.3VS_8, C293 22U/6.3VS_8
C292 22U/6.3VS_8, C581 22U/6.3VS_8

0809 DEL FOR SG

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

### 1.8V RAIL

SNB: 1.5A
IVY: 1.5A

+1.8V

C511 10U/6.3V_8, C509 1U/6.3V_4, C514 1U/6.3V_4, C505 *330U/2V_7343

VCCPLL1 VCCPLL2 VCCPLL3

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

Ivy Bridge_rPGA_2DPC_Rev0p61

## POWER

### SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R140 100_4 +VCC_GFX
VCC_AXG_SENSE [38]
VSS_AXG_SENSE [38]
R137 100_4

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

### VREF

+VDDR_REF_CPU
SM_VREF AL1
R162 100K_4
Q25 2N7002
DDR_VTTREF [12,13,32]
MAIND
MAIND [40]

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1
SMDDR_VREF_DQ0_M3 [12]
SMDDR_VREF_DQ1_M3 [13]
R401 *1K_4
R409 *1K_4

### DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A
IVY: 5A

+1.5V_CPU

C126 10U/6.3VS_6, C148 10U/6.3V_8, C215 10U/6.3VS_6, C151 10U/6.3VS_6

330uF x1, 10uF_8 x6 Socket BOT edge.

C168 10U/6.3VS_6, C225 10U/6.3VS_6, C642 *220U/6.3V_6X4.5ESR18

### SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

SNB: 6A
IVY: 6A

+VCCSA

C544 10U/6.3V_8, C508 10U/6.3V_8, C84 10U/6.3V_8, C513 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

### MISC

VCCSA_SENSE H23 — VCCUSA_SENSE_R — R403 0_4 — VCCUSA_SENSE [33]
VCCSA_SEL0 [33]
VCCSA_VID[0] C22 — R407 10/F_4
VCCSA_VID[1] C24 — R408 10/F_4 — VCCSA_SEL [33]
VCCIO_SEL A19 — R406 0_4 — H_VTTVID1 [34]

Layout note: need routing together and ALERT need between CLK and DATA.

### SVID CLK

Place PU resistor close to VR
R399 *54.9/F_4 +1.05V
Intel DG request
VR_SVID_CLK — VR_SVID_CLK [38]

### SVID DATA

+1.05V +1.05V
Place PU resistor close to CPU — R125 130/F_4
R398 *130/F_4 — Place PU resistor close to VR
VR_SVID_DATA — VR_SVID_DATA [38]
Intel DG request

### SVID ALERT

Place PU resistor close to CPU
+1.05V R154 75_4
H_CPU_SVIDALRT# R142 43_4 — VR_SVID_ALERT# [38]

+1.5VSUS +1.5V_CPU +1.5VSUS
Q44 AON7410
R166 220_8
C650 0.1U/10V_4
C651 0.1U/10V_4
C652 0.1U/10V_4
C648 0.1U/10V_4
Placement close to CPU.
MAIND
C295 *470P/50V_4
Q27 2N7002
MAIN_ONG [2,40]

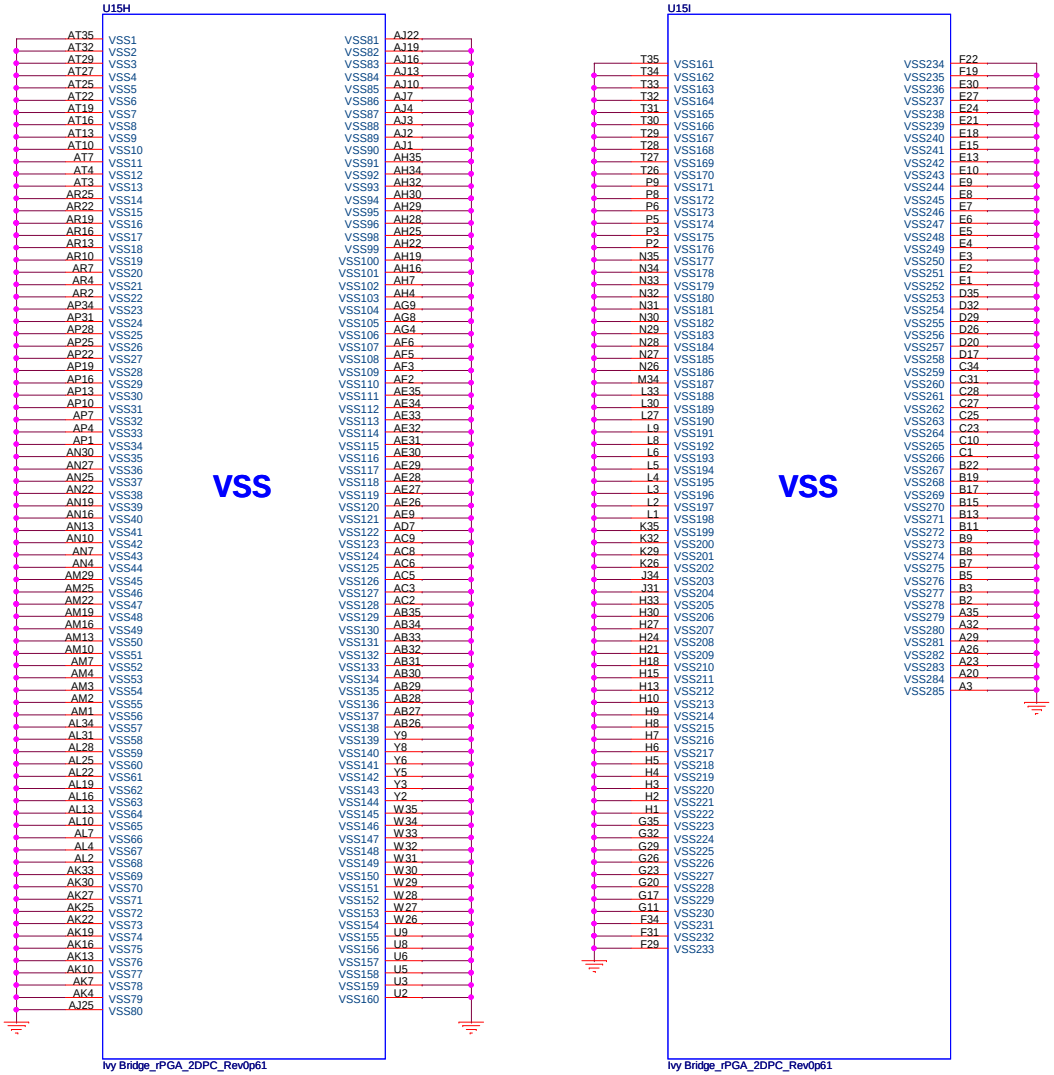
### CPU VDDQ

PROJECT : JW2
Quanta Computer Inc.
NB5

| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 3/4 (Power) | D A |

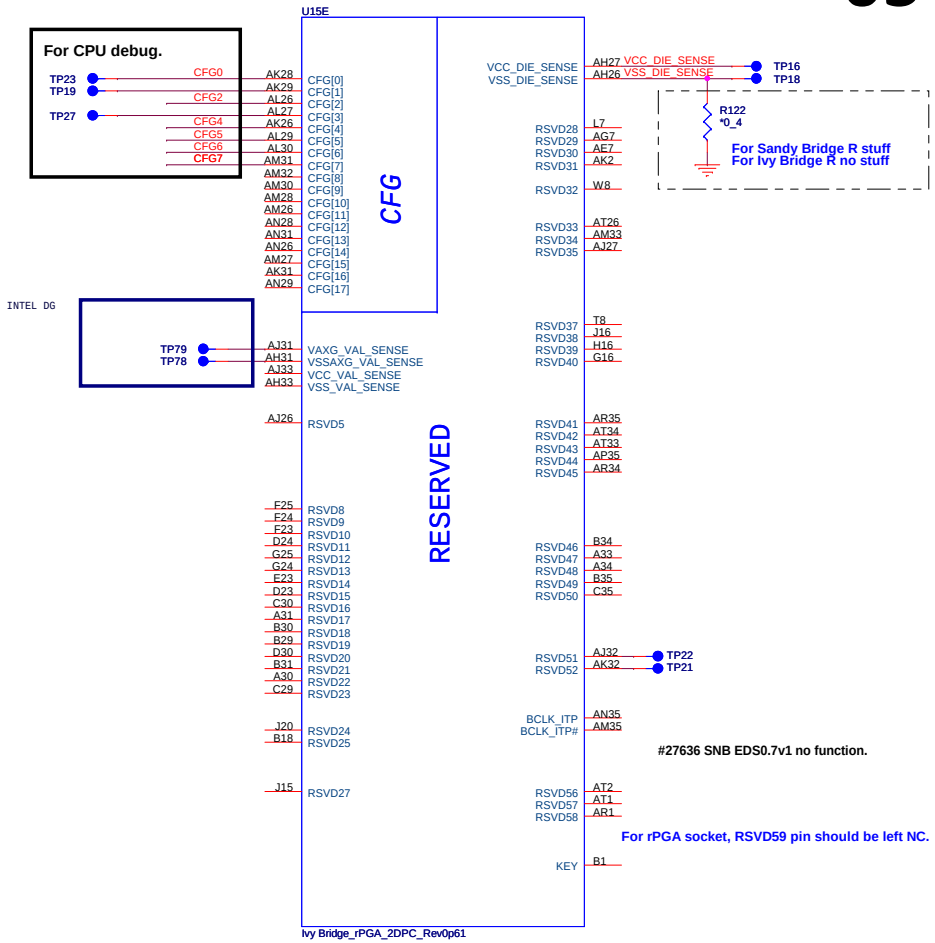
Date: Wednesday, November 02, 2011 | Sheet 4 of 40

# Ivy Bridge Processor (GND)




# Ivy Bridge Processor (RESERVED, CFG)

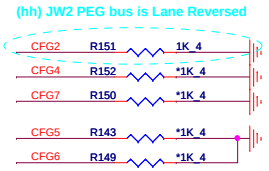





## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |




**CFG[6:5] (PCIE Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

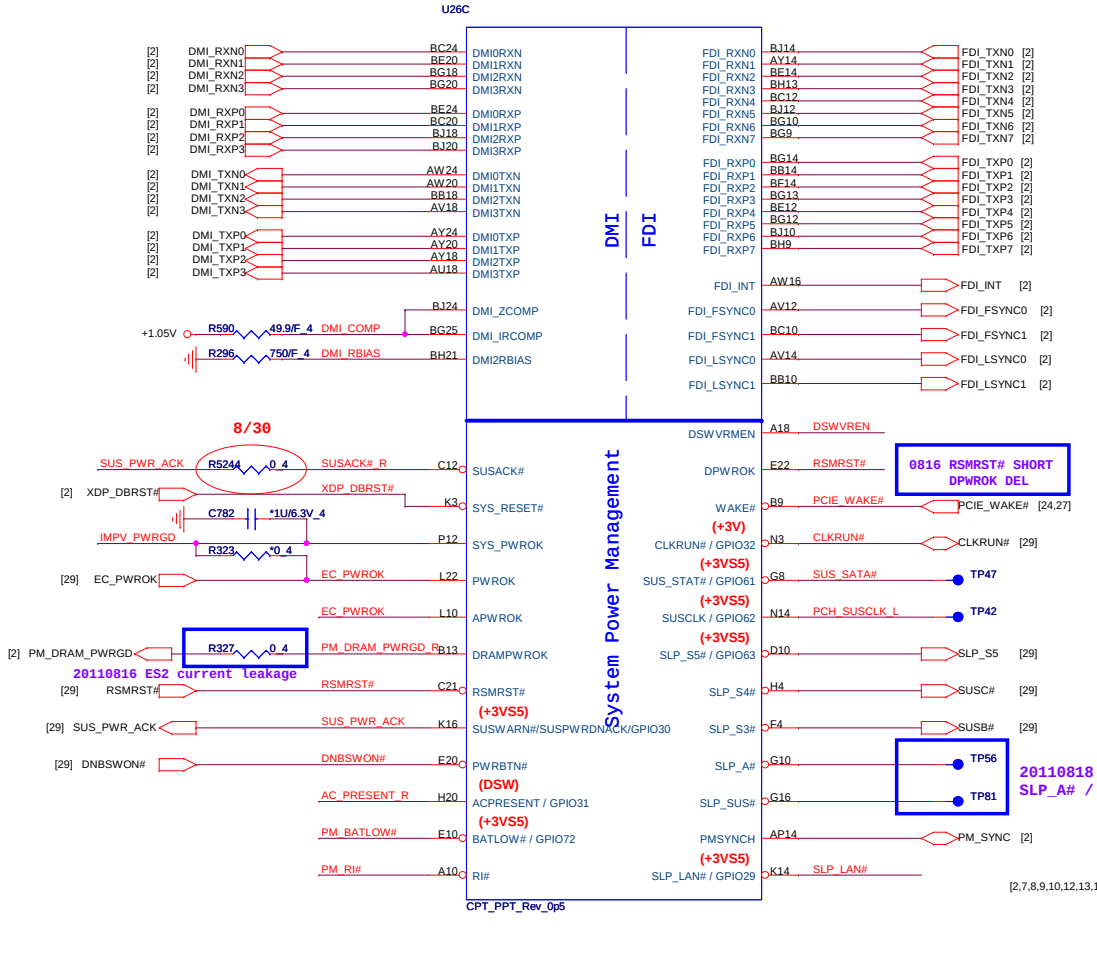
NB5

**PROJECT : JW2**
Quanta Computer Inc.

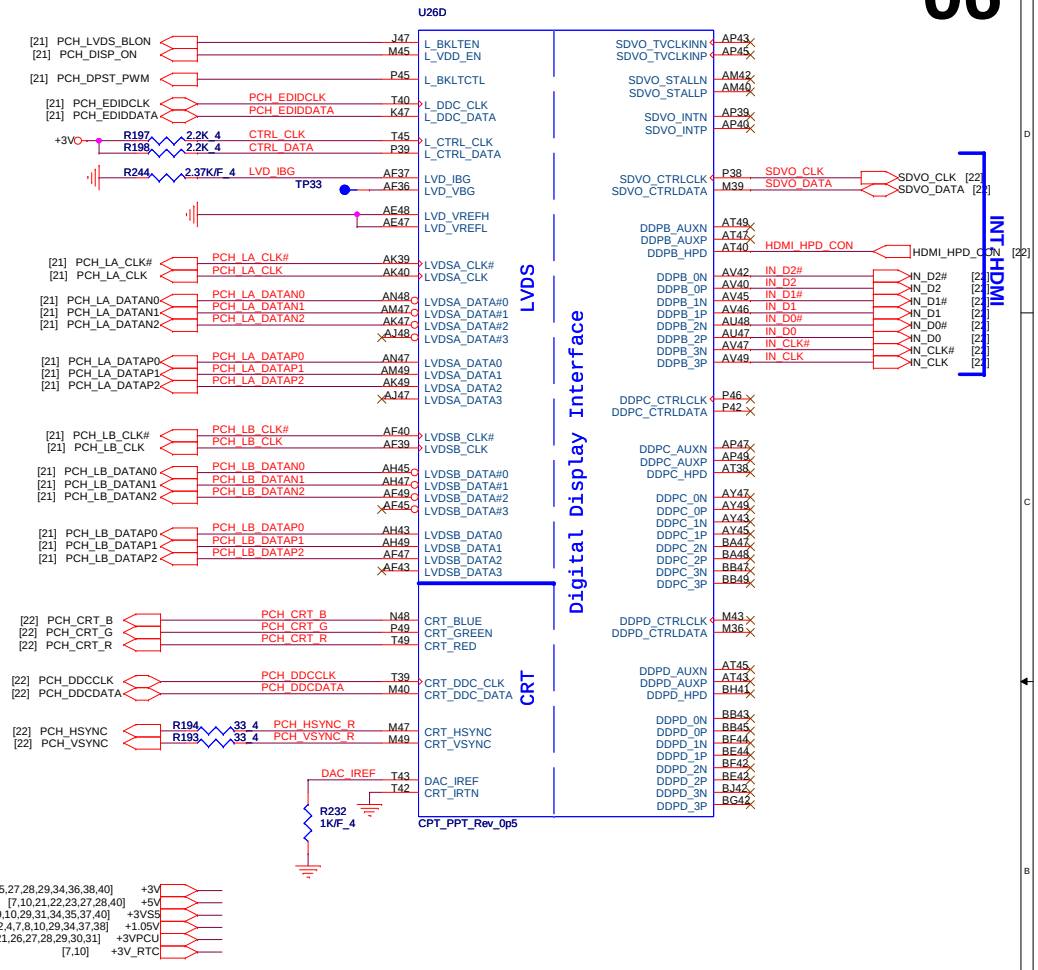
| Size | Document Number | Rev/D |
|---|---|---|
| Custom | Processor 4/4 (Ground) | A |

Date: Wednesday, November 02, 2011 | Sheet 5 of 40

# Cougar Point/Panther Point (DMI,FDI,PM)

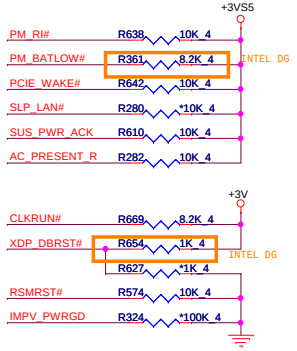



# Cougar Point/Panther Point (LVDS,DDI)

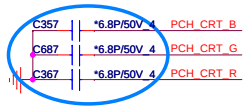



06

## PCH Pull-high/low(CLG)



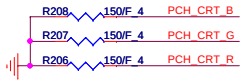

## INT LVDS & CRT disable (DIS only remove)




EMI(near PCH)

PD Res place close to PCH

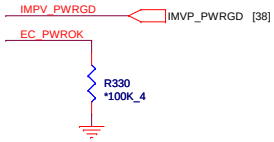
PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.

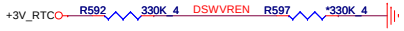



## INT HDMI disable (DIS only remove)

20110818 DEL
INT HDMI Detect Function

## System PWR_OK(CLG)




| On Die DSW VR Enable |
|---|
| High = Enable (Default)<br>Low = Disable |

## DPWROK FOR DSW

0816 DSW circuit DEL

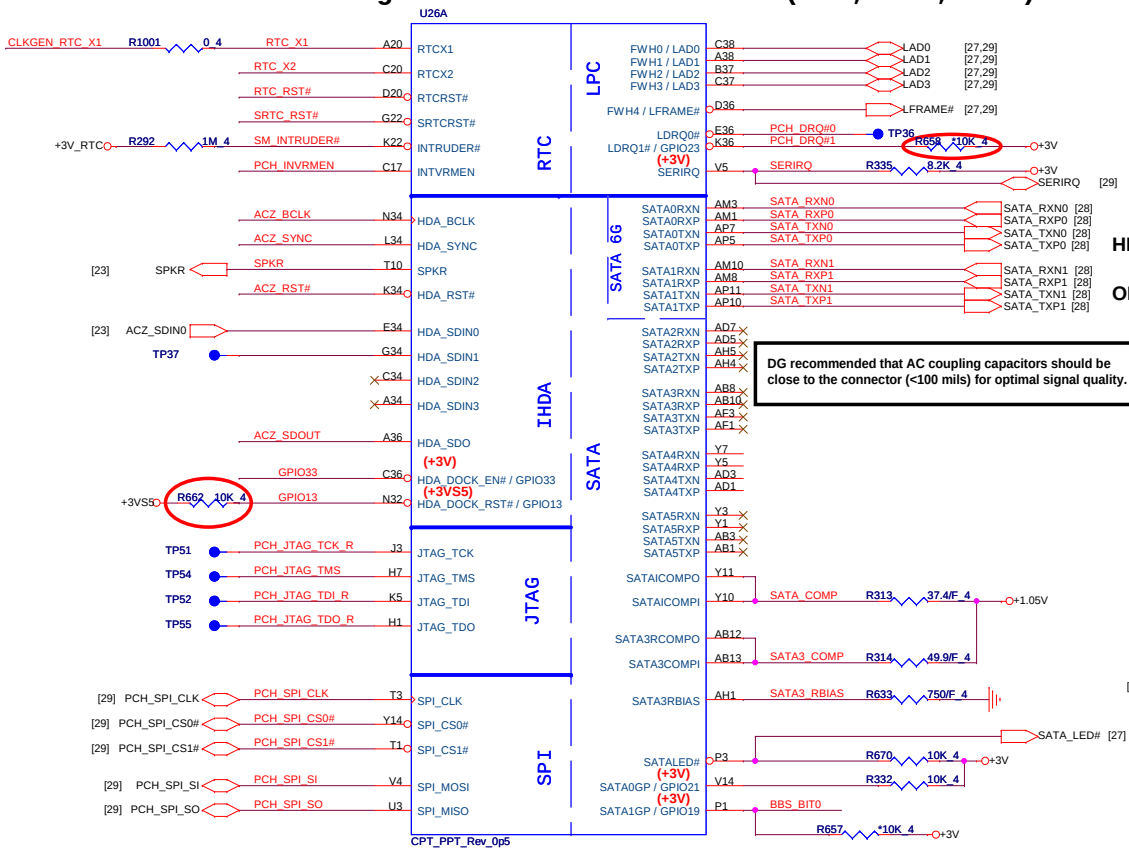
NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 1/6 (Host/Display) | D<br>A |

Date: Wednesday, November 02, 2011 | Sheet 6 of 40

# Cougar Point/Panther Point (HDA,JTAG,SATA)




HDD0 (SATA3 6.0Gb/s)

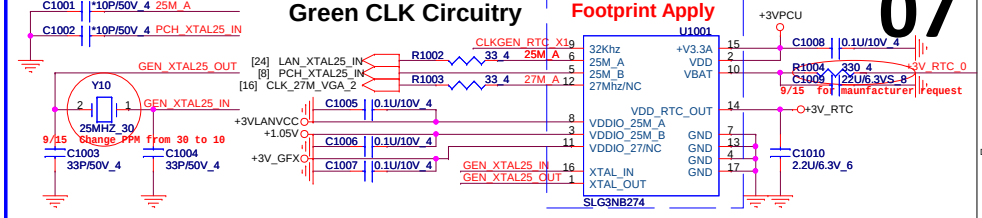
ODD (SATA1 6Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

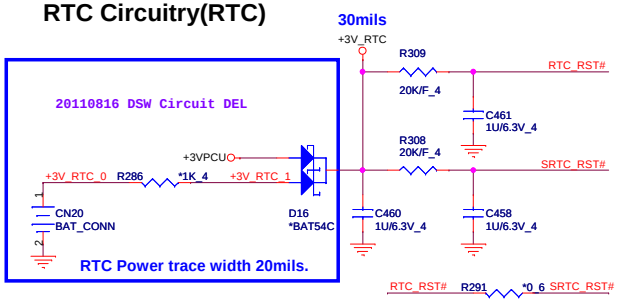
## Green CLK Circuitry

For UMA : SLG3NB244
For DIS : SLG3NB274
Footprint Apply

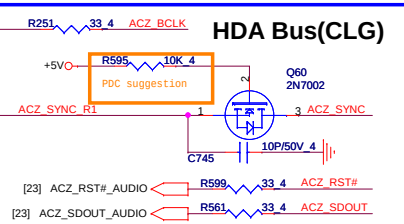
07



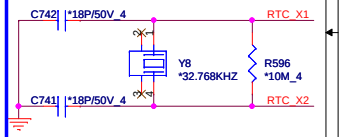

## RTC Circuitry(RTC)




## HDA Bus(CLG)

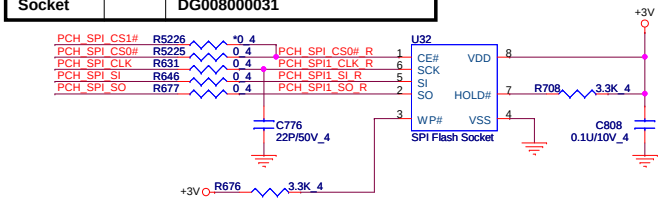



## RTC Clock 32.768KHz




## PCH SPI ROM(CLG)

| Vender | Size | P/N |
|---|---|---|
| EON | 4MB | AKE39FN0Q00 (EN25F32-100HIP) |
| Winbond | 4MB | AKE391P0N00 (W25Q32BVSSIG) |
| Socket | | DG008000031 |




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | Circuit |
|---|---|---|---|---|
| SPKR Different from Calpella | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | SPKR R666 *1K_4 +3V |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | +3V R548 *1K_4 R546 10K_4 PCI_GNT3# [8] |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | PCH_INVRMEN R593 330K_4 +3V_RTC |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | GPIO33 R566 *1K_4 ACZ_SDOUT ACZ_SDOUT [29] |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1# |
| GPIO19 Different from Calpella | Boot BIOS Selection 0 [bit-0] | PWROK | | R630 *1K_4 BBS_BIT0<br>R547 *1K_4 BBS_BIT1 [8] |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | +1.8V R635 *1K_4 NV_ALE [8] |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 20kohm | +1.8V R644 2.2K_4 R634 1K_4 NV_CLE [9] H_SNB_IVB# [2] sandy/Ivy bridge |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V | +3VS5 R594 1K_4 ACZ_SYNC |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | ACZ_SDOUT R571 *1K_4 +3VS5 |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down (weak pull-up 20K) | R639 *1K_4 ICC_EN# [9] |
| GPIO28 Different from Calpella | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | R648 *1K_4 PLL_ODVR_EN [9] |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | PCH_SPI_SI R622 *1K_4 +3V |

+3V [2,6,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,34,36,38,40]
+5V [10,21,22,23,27,28,40]
+1.8V [4,10,35]
+1.05V [2,4,6,8,10,29,34,37,38]
+3VS5 [6,8,9,10,29,31,34,35,37,40]
+3VPCU [21,26,27,28,29,30,31]
+3V_RTC [6,10]

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | PCH 2/6 (HDA/RTC/SATA/SPI) | A |

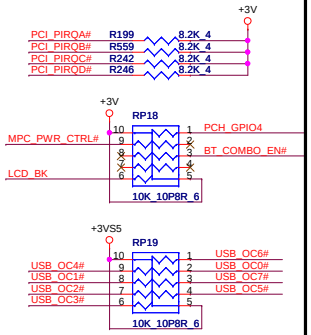
Date: Wednesday, November 02, 2011 | Sheet 7 of 40

# Cougar Point-M/Panther Point (PCI,USB,NVRAM)

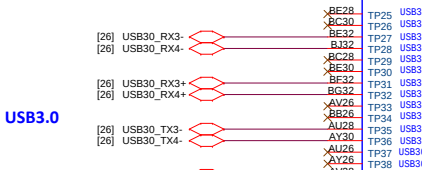
# Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

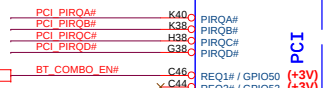
## PCI/USBOC# Pull-up(CLG)



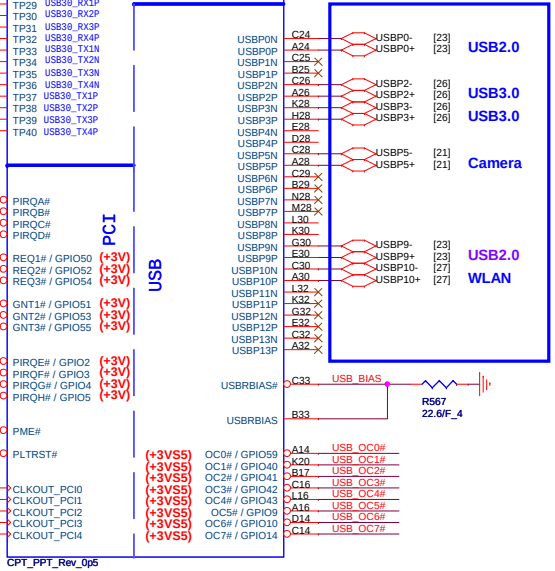

## USB3.0



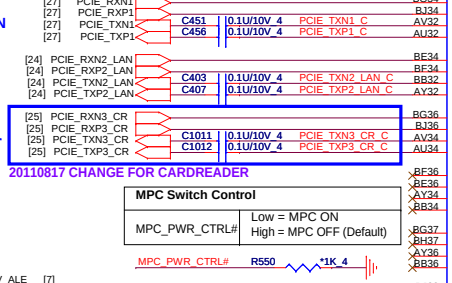

## PCI



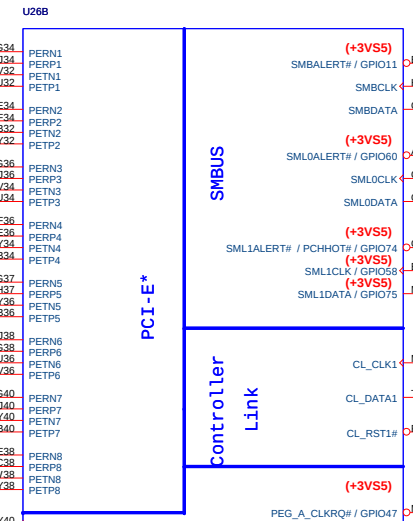

## USB



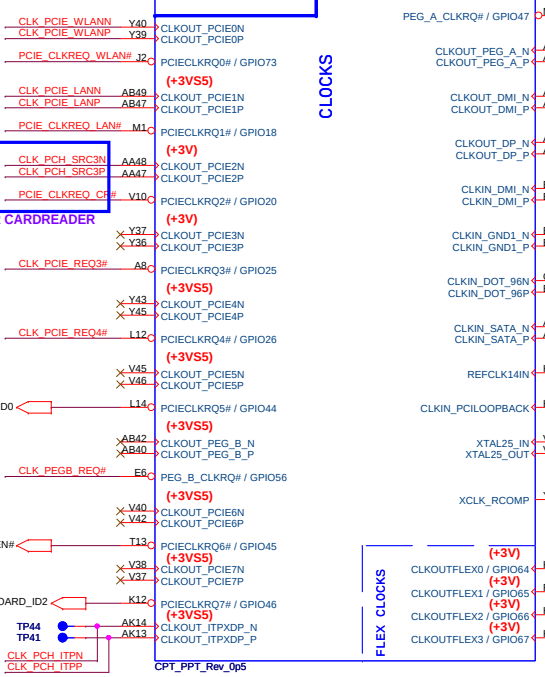

## WLAN / LAN / Cardreader



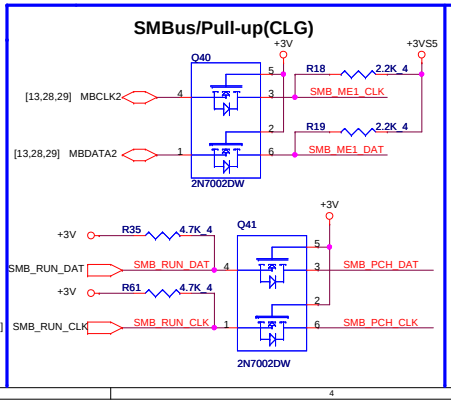

## PCI-E* / SMBUS / Controller Link



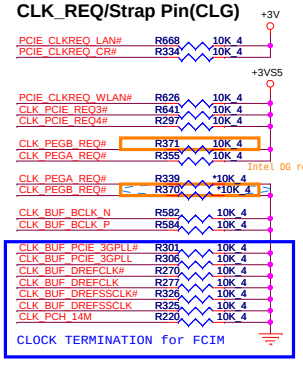

## CLOCKS



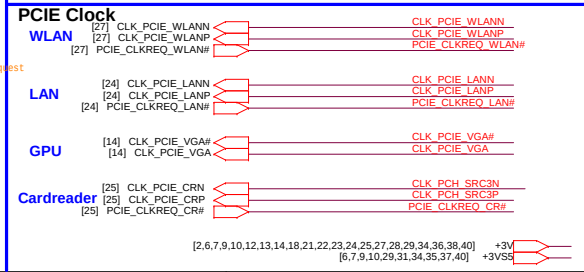

## SMBus/Pull-up(CLG)



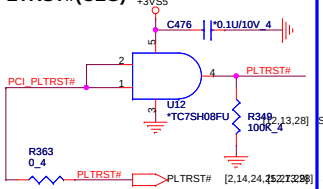

## CLK_REQ/Strap Pin(CLG)



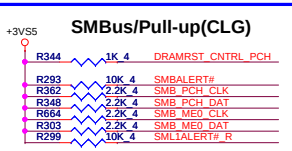

## PCIE Clock




## PLTRST#(CLG)




## SMBus/Pull-up(CLG)




NB5

**PROJECT : JW2**

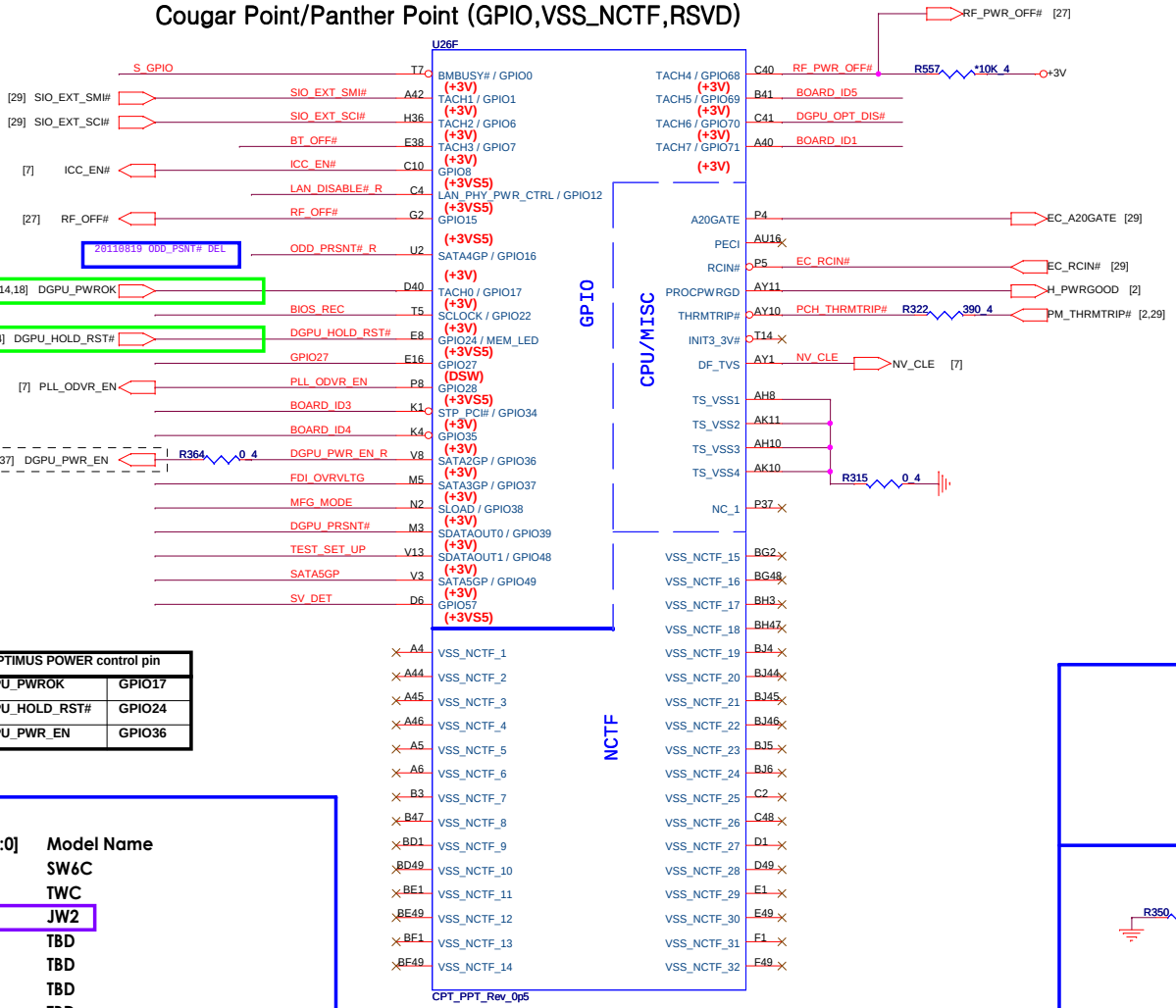
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | PCH 3/6 (Clock/PCI/PCIE/USB) | A |

Date: Wednesday, November 02, 2011 | Sheet 8 of 40

# Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)





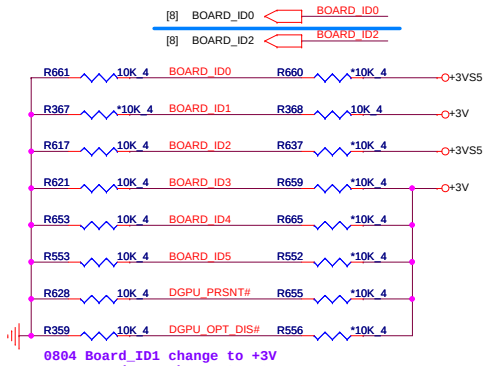

| OPTIMUS POWER control pin | |
|---|---|
| DGPU_PWROK | GPIO17 |
| DGPU_HOLD_RST# | GPIO24 |
| DGPU_PWR_EN | GPIO36 |

| BOARD_ID[3:0] | Model Name |
|---|---|
| 0000 | SW6C |
| 0001 | TWC |
| 0010 | JW2 |
| 0011 | TBD |
| 0100 | TBD |
| 0101 | TBD |
| 0110 | TBD |
| 0111 | TBD |
| 1000 | TBD |

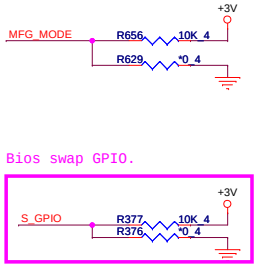
## Chief River BOARD ID SETTING

| | | |
|---|---|---|
| BOARD_ID0 | GPIO44 | MODEL BIT0 |
| BOARD_ID1 | GPIO71 | MODEL BIT1 |
| BOARD_ID2 | GPIO46 | MODEL BIT2 |
| BOARD_ID3 | GPIO34 | MODEL BIT3 |
| BOARD_ID4 | GPIO35 | No Dolby=0, Dolby=1 |
| BOARD_ID5 | GPIO69 | Reserve and pull low |
| DGPU_PRSNT# | GPIO39 | Reserve and pull low |
| DGPU_OPT_DIS# | GPIO70 | Optimus=0, Dis only=1 |

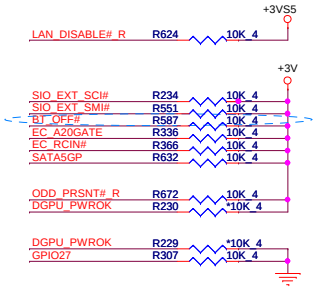
20110816 Define BRD_ID[3:0]

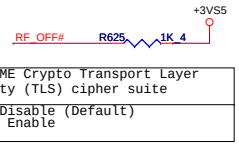


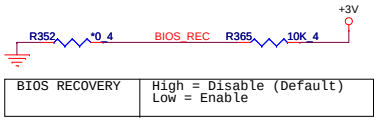

### MFG-TEST

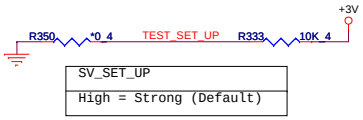


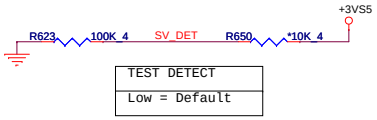

### GPIO Pull-up/Pull-down(CLG)

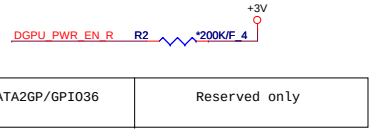


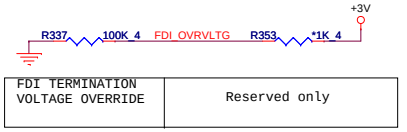




[2,6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,34,36,38,40] +3V
[6,7,8,10,29,31,34,35,37,40] +3VS5

NB5

**PROJECT : JW2**

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 4/6 (GPIO) | D A |

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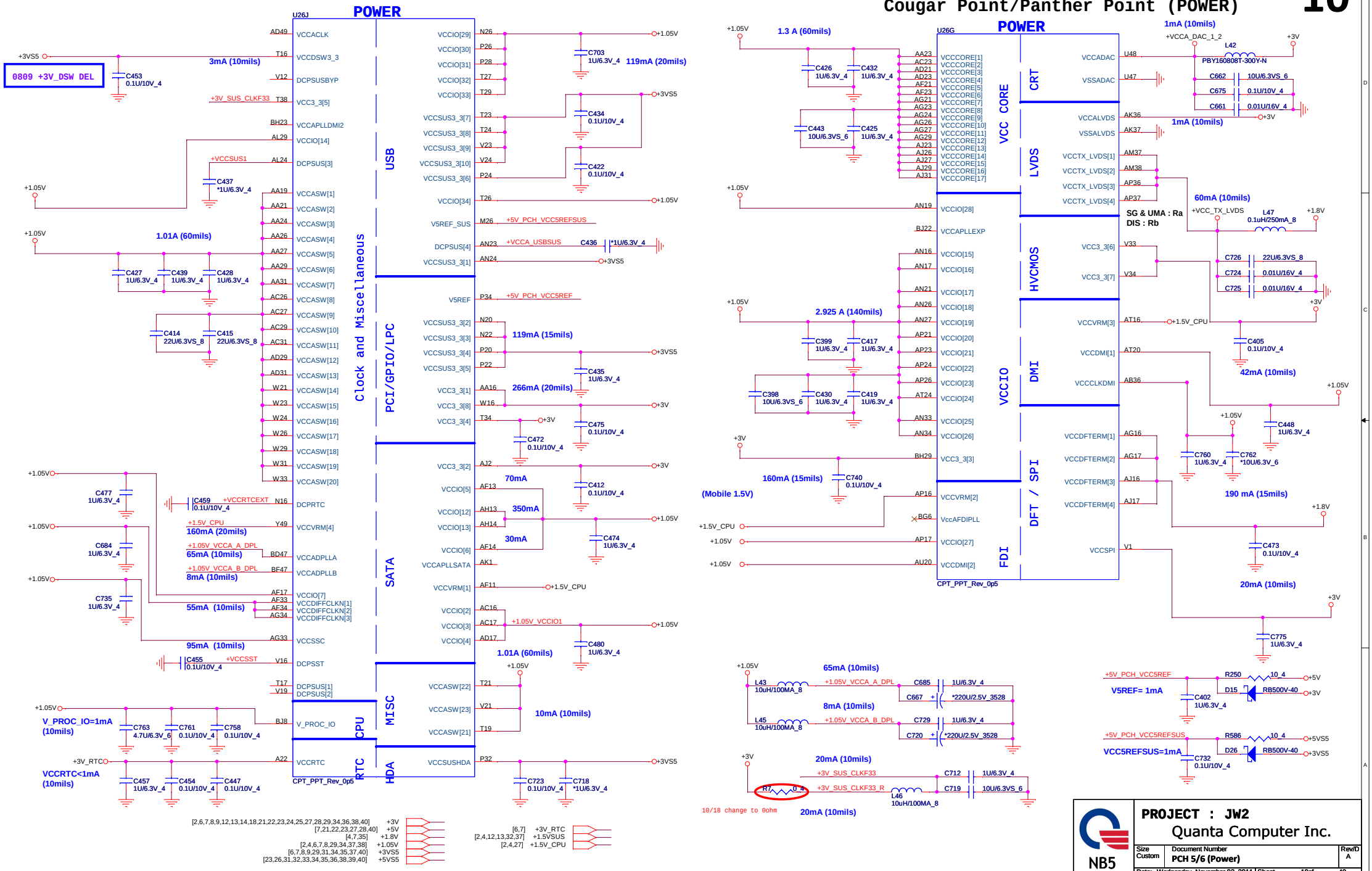
# Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)






| | |
|---|---|
| [2,6,7,8,9,12,13,14,18,21,22,23,24,25,27,28,29,34,36,38,40] | +3V |
| [7,21,22,23,27,28,40] | +5V |
| [4,7,35] | +1.8V |
| [2,4,6,7,8,29,34,37,38] | +1.05V |
| [6,7,8,9,29,31,34,35,37,40] | +3VS5 |
| [23,26,31,32,33,34,35,36,38,39,40] | +5VS5 |
| [6,7] | +3V_RTC |
| [2,4,12,13,32,37] | +1.5VSUS |
| [2,4,27] | +1.5V_CPU |

PROJECT : JW2

Quanta Computer Inc.

NB5

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | PCH 5/6 (Power) | A |

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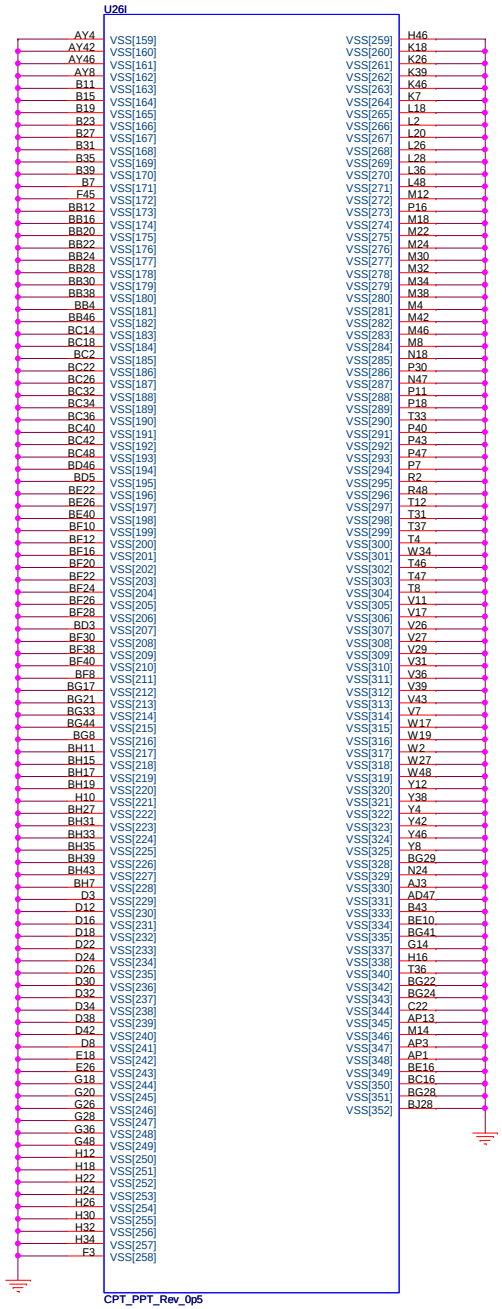
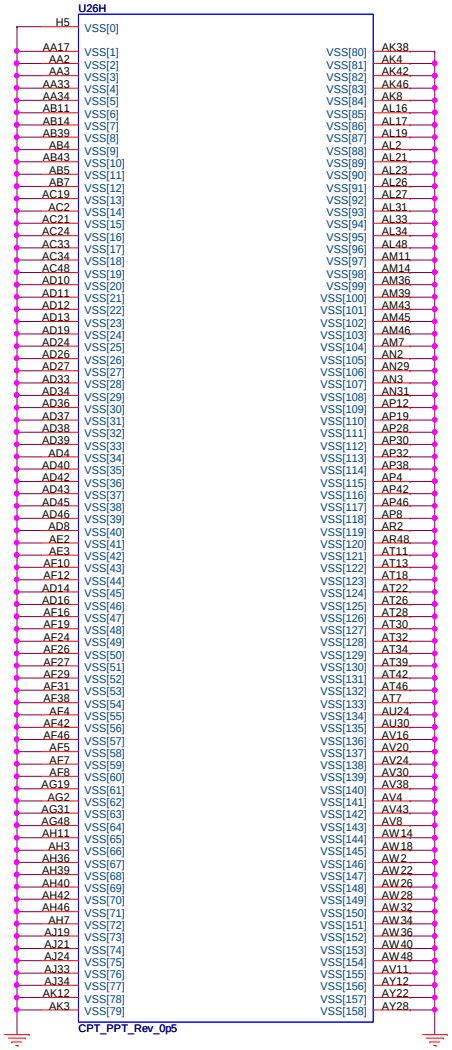
## Cougar Point/Panther Point (GND)




## Cougar Point/Panther Point (GND)




**PROJECT : JW2**

Quanta Computer Inc.

NB5

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | PCH 6/6 (Ground) | A |

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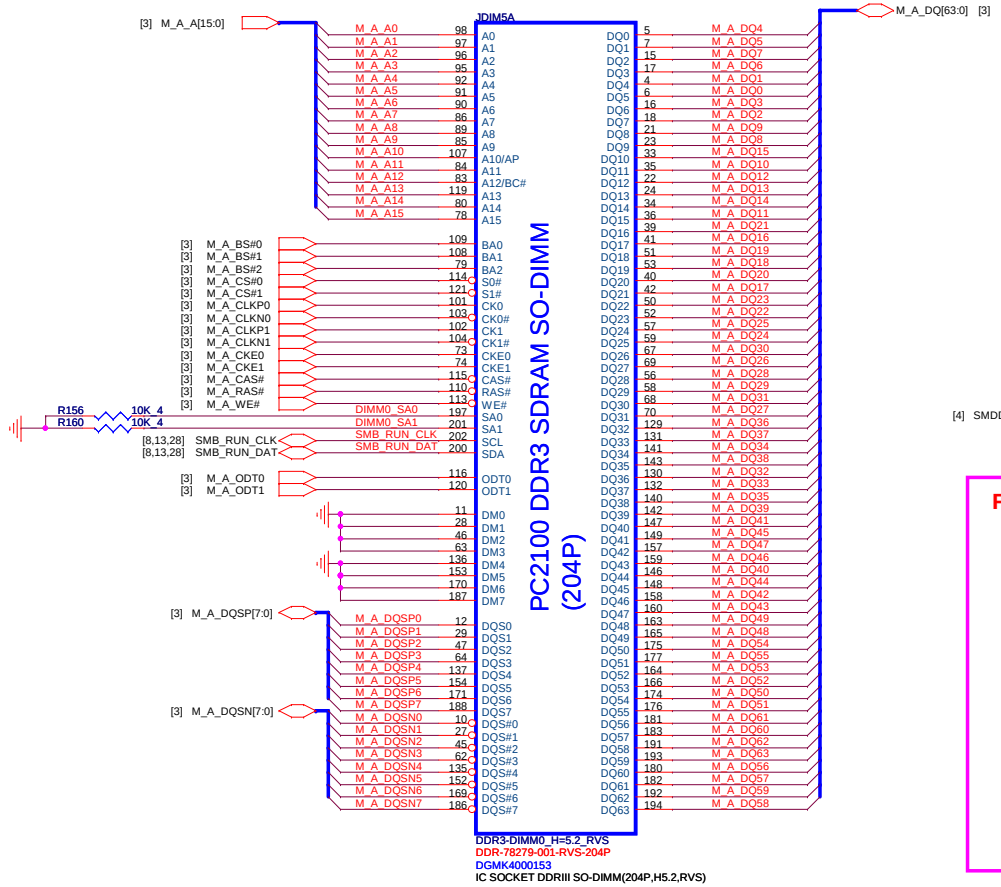
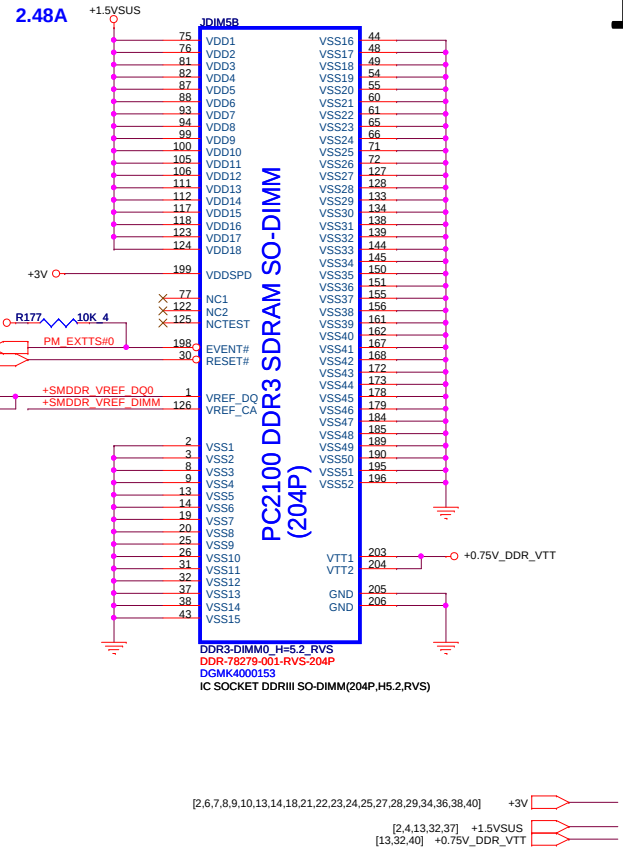
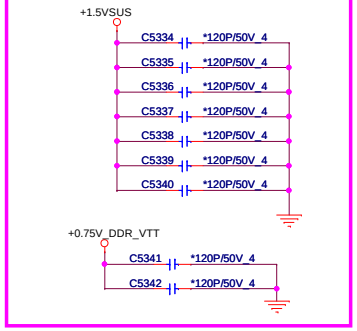


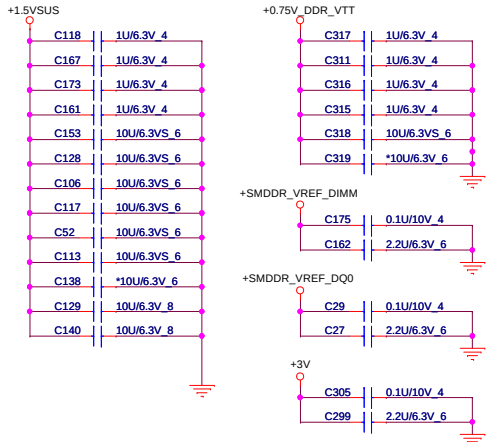




## For EMI RESERVE 8/30

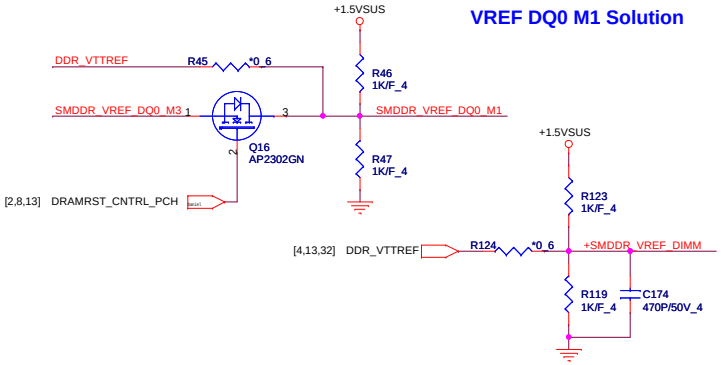




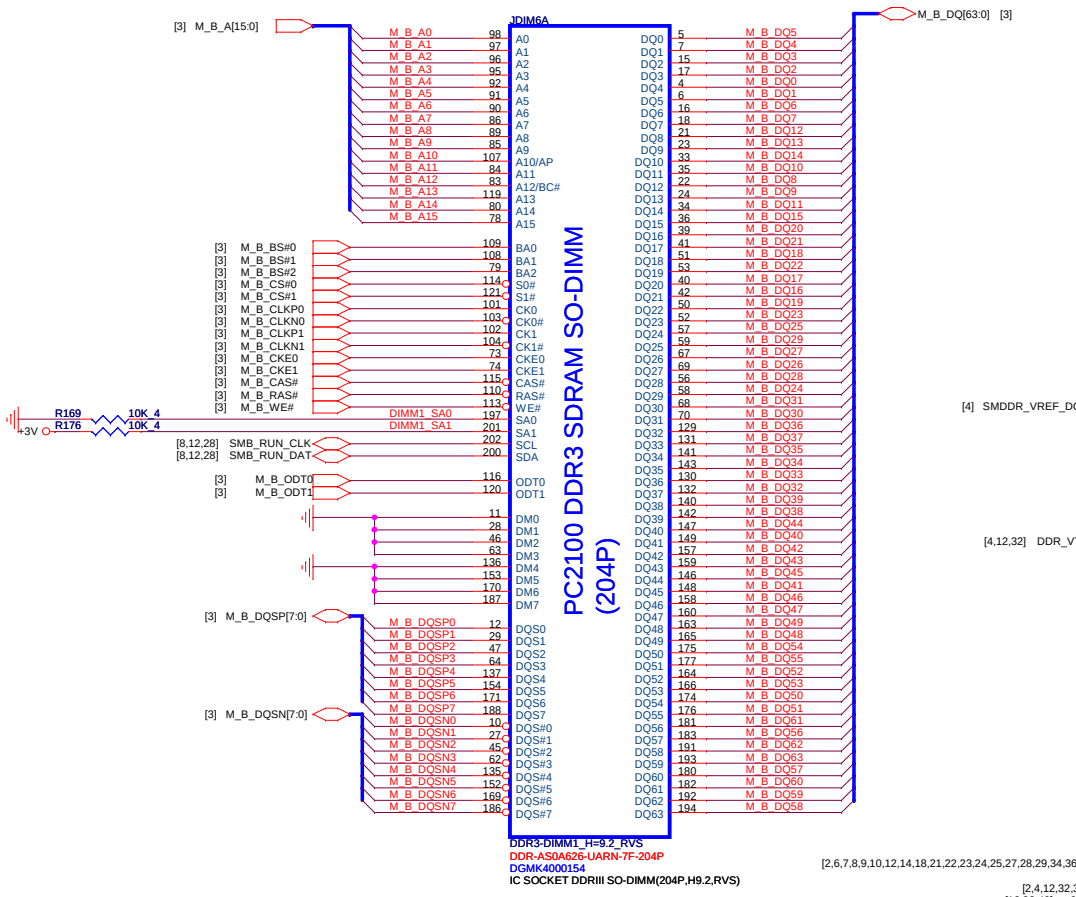
## Place these Caps near So-Dimm0.

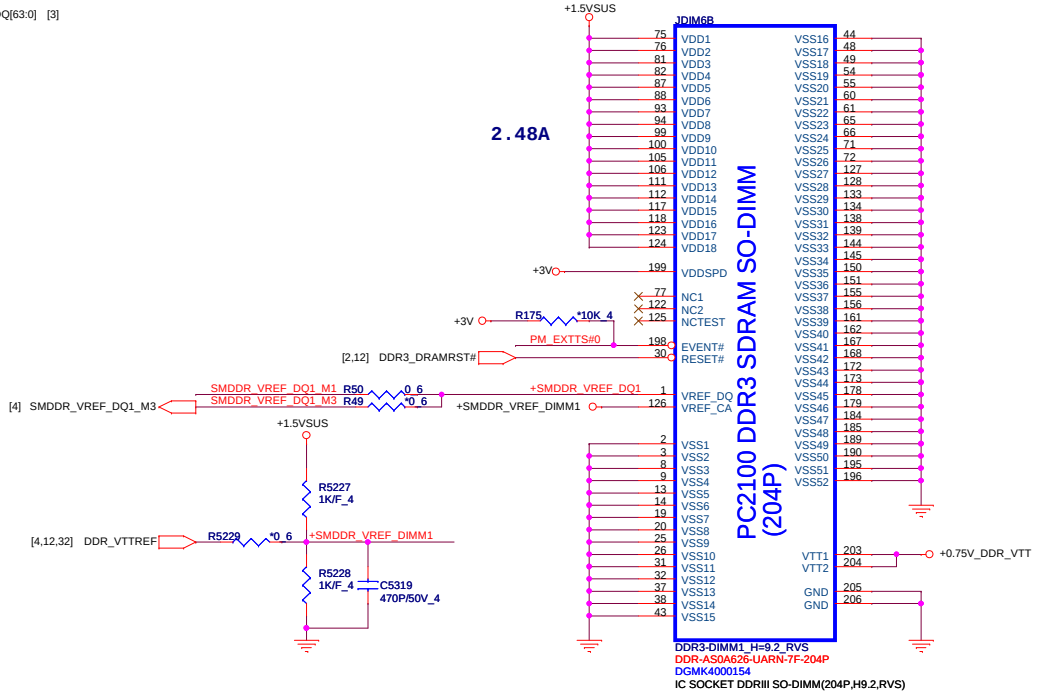


## VREF DQ0 M1 Solution

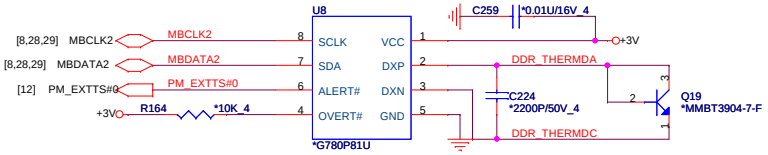


| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: System Memory 1/2 (5.2H) | Rev: D A |
| Date: Wednesday, November 02, 2011 | Sheet 12 of 40 | |

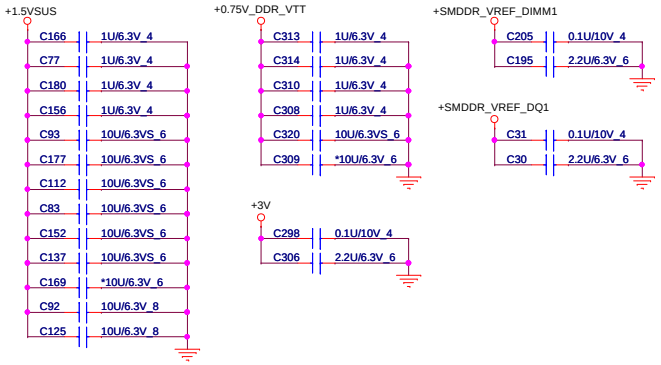


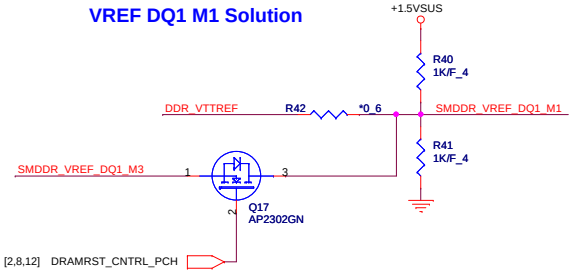

## DDR3 Thermal Sensor




## Place these Caps near So-Dimm1.



## VREF DQ1 M1 Solution




| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: System Memory 2/2 (9.2H) | Rev/D: A |
| Date: Wednesday, November 02, 2011 | Sheet 13of 40 | |

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C5187 22U/6.3VS_8
C5002 22U/6.3VS_8
C5003 10U/6.3VS_6
C5004 10U/6.3VS_6
PLACE UNDER BGA C5013 4.7U/6.3V_6
C5005 1U/6.3V_4
PLACE NEAR BALLS C5006 1U/6.3V_4

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C5007 22U/6.3VS_8
C5008 22U/6.3VS_8
C5009 10U/6.3VS_6
C5014 10U/6.3VS_6
PLACE UNDER BGA C5010 4.7U/6.3V_6
C5011 1U/6.3V_4
PLACE NEAR BALLS C5012 1U/6.3V_4

**0727 PEX_IOVDD/Q**
**TOTAL 3500mA**

U17A

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6

AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

[PEG Interface]

| | | | |
|---|---|---|---|
| PEX_RX0 | AN12 | PEG_TX15 | PEG_TX15 [2] |
| PEX_RX0_N | AM12 | PEG_TX#15 | PEG_TX#15 [2] |
| PEX_RX1 | AN14 | PEG_TX14 | PEG_TX14 [2] |
| PEX_RX1_N | AM14 | PEG_TX#14 | PEG_TX#14 [2] |
| PEX_RX2 | AP14 | PEG_TX13 | PEG_TX13 [2] |
| PEX_RX2_N | AP15 | PEG_TX#13 | PEG_TX#13 [2] |
| PEX_RX3 | AN15 | PEG_TX12 | PEG_TX12 [2] |
| PEX_RX3_N | AM15 | PEG_TX#12 | PEG_TX#12 [2] |
| PEX_RX4 | AN17 | PEG_TX11 | PEG_TX11 [2] |
| PEX_RX4_N | AM17 | PEG_TX#11 | PEG_TX#11 [2] |
| PEX_RX5 | AP17 | PEG_TX10 | PEG_TX10 [2] |
| PEX_RX5_N | AP18 | PEG_TX#10 | PEG_TX#10 [2] |
| PEX_RX6 | AN18 | PEG_TX9 | PEG_TX9 [2] |
| PEX_RX6_N | AM18 | PEG_TX#9 | PEG_TX#9 [2] |
| PEX_RX7 | AN20 | PEG_TX8 | PEG_TX8 [2] |
| PEX_RX7_N | AM20 | PEG_TX#8 | PEG_TX#8 [2] |
| PEX_RX8 | AP20 | PEG_TX7 | PEG_TX7 [2] |
| PEX_RX8_N | AP21 | PEG_TX#7 | PEG_TX#7 [2] |
| PEX_RX9 | AN21 | PEG_TX6 | PEG_TX6 [2] |
| PEX_RX9_N | AM21 | PEG_TX#6 | PEG_TX#6 [2] |
| PEX_RX10 | AN23 | PEG_TX5 | PEG_TX5 [2] |
| PEX_RX10_N | AM23 | PEG_TX#5 | PEG_TX#5 [2] |
| PEX_RX11 | AP23 | PEG_TX4 | PEG_TX4 [2] |
| PEX_RX11_N | AP24 | PEG_TX#4 | PEG_TX#4 [2] |
| PEX_RX12 | AN24 | PEG_TX3 | PEG_TX3 [2] |
| PEX_RX12_N | AM24 | PEG_TX#3 | PEG_TX#3 [2] |
| PEX_RX13 | AN26 | PEG_TX2 | PEG_TX2 [2] |
| PEX_RX13_N | AM26 | PEG_TX#2 | PEG_TX#2 [2] |
| PEX_RX14 | AP26 | PEG_TX1 | PEG_TX1 [2] |
| PEX_RX14_N | AP27 | PEG_TX#1 | PEG_TX#1 [2] |
| PEX_RX15 | AN27 | PEG_TX0 | PEG_TX0 [2] |
| PEX_RX15_N | AM27 | PEG_TX#0 | PEG_TX#0 [2] |

| | | | | |
|---|---|---|---|---|
| PEX_TX0 | AK14 | C_PEG_RX15 | C5016 | 0.22U/10V_4 |
| PEX_TX0_N | AJ14 | C_PEG_RX#15 | C5017 | 0.22U/10V_4 |
| PEX_TX1 | AH14 | C_PEG_RX14 | C5018 | 0.22U/10V_4 |
| PEX_TX1_N | AG14 | C_PEG_RX#14 | C5019 | 0.22U/10V_4 |
| PEX_TX2 | AK15 | C_PEG_RX13 | C5020 | 0.22U/10V_4 |
| PEX_TX2_N | AJ15 | C_PEG_RX#13 | C5021 | 0.22U/10V_4 |
| PEX_TX3 | AL16 | C_PEG_RX12 | C5022 | 0.22U/10V_4 |
| PEX_TX3_N | AK16 | C_PEG_RX#12 | C5023 | 0.22U/10V_4 |
| PEX_TX4 | AK17 | C_PEG_RX11 | C5024 | 0.22U/10V_4 |
| PEX_TX4_N | AJ17 | C_PEG_RX#11 | C5025 | 0.22U/10V_4 |
| PEX_TX5 | AH17 | C_PEG_RX10 | C5026 | 0.22U/10V_4 |
| PEX_TX5_N | AG17 | C_PEG_RX#10 | C5027 | 0.22U/10V_4 |
| PEX_TX6 | AK18 | C_PEG_RX9 | C5028 | 0.22U/10V_4 |
| PEX_TX6_N | AJ18 | C_PEG_RX#9 | C5029 | 0.22U/10V_4 |
| PEX_TX7 | AL19 | C_PEG_RX8 | C5030 | 0.22U/10V_4 |
| PEX_TX7_N | AK19 | C_PEG_RX#8 | C5031 | 0.22U/10V_4 |
| PEX_TX8 | AK20 | C_PEG_RX7 | C5032 | 0.22U/10V_4 |
| PEX_TX8_N | AJ20 | C_PEG_RX#7 | C5033 | 0.22U/10V_4 |
| PEX_TX9 | AH20 | C_PEG_RX6 | C5034 | 0.22U/10V_4 |
| PEX_TX9_N | AG20 | C_PEG_RX#6 | C5035 | 0.22U/10V_4 |
| PEX_TX10 | AK21 | C_PEG_RX5 | C5036 | 0.22U/10V_4 |
| PEX_TX10_N | AJ21 | C_PEG_RX#5 | C5037 | 0.22U/10V_4 |
| PEX_TX11 | AL22 | C_PEG_RX4 | C5038 | 0.22U/10V_4 |
| PEX_TX11_N | AK22 | C_PEG_RX#4 | C5039 | 0.22U/10V_4 |
| PEX_TX12 | AK23 | C_PEG_RX3 | C5040 | 0.22U/10V_4 |
| PEX_TX12_N | AJ23 | C_PEG_RX#3 | C5041 | 0.22U/10V_4 |
| PEX_TX13 | AH23 | C_PEG_RX2 | C5042 | 0.22U/10V_4 |
| PEX_TX13_N | AG23 | C_PEG_RX#2 | C5043 | 0.22U/10V_4 |
| PEX_TX14 | AK24 | C_PEG_RX1 | C5044 | 0.22U/10V_4 |
| PEX_TX14_N | AJ24 | C_PEG_RX#1 | C5045 | 0.22U/10V_4 |
| PEX_TX15 | AL25 | C_PEG_RX0 | C5046 | 0.22U/10V_4 |
| PEX_TX15_N | AK25 | C_PEG_RX#0 | C5047 | 0.22U/10V_4 |

PEG_RX15 [2] … PEG_RX#0 [2]

AC6 NC_1
AJ28 NC_2
AJ4 NC_3
AJ5 NC_4
AL11 NC_5
C15 NC_6
D19 NC_7
D20 NC_8
D23 NC_9
D26 NC_10
H31 NC_11
T8 NC_12
V32 NC_13

0824 DGPU SMB ISOLATION

R5123 *0_4
Q5013
ME3424D
+3V_GFX
+3V_GFX_VDD33

[36,37] DGPU_PWR_EN — DGPU_PWR_EN

J8 VDD33_1
K8 VDD33_2
L8 VDD33_3
M8 VDD33_4
+3V_GFX

| | | | |
|---|---|---|---|
| PEX_REFCLK | AL13 | CLK_PCIE_VGA | CLK_PCIE_VGA [8] |
| PEX_REFCLK_N | AK13 | CLK_PCIE_VGA# | CLK_PCIE_VGA# [8] |
| PEX_TSTCLK_OUT | AJ26 | PEX_TSTCLK | R5008 *200_4 |
| PEX_TSTCLK_OUT_N | AK26 | PEX_TSTCLK# | |
| PEX_WAKE | AJ11 | | |
| PEX_RST_N | AJ12 | VGA_RST# | R5009 0_4 PEGX_RST# |
| PEX_CLKREQ_N | AK12 | PEX_CLKREQ# | R5010 10K_4 +3V_GFX |
| PEX_TERMP | AP29 | PEX_TERMP | R5011 2.49K/F_4 |
| TESTMODE | AK11 | TESTMODE | R5012 10K_4 |
| PEX_PLLVDD | AG26 | PEX_PLLVDD | R5013 *0_6 +1.05V_GFX |
| PEX_PLL_HVDD | AH12 | | R5047 *0_4 |
| PEX_SVDD_3V3 | AG12 | | |
| 3.3V_AUX_NC | P8 | | |
| VDD_SENSE | L4 | | |
| GND_SENSE | L5 | | |

Ra La L5001 PBY160808T-300Y-N

C5049 4.7U/6.3V_6 PLACE NEAR BGA CLOSE TO CAPS
C5051 1U/6.3V_4
C5054 0.1U/10V_4 PLACE UNDER BGA
PLACE NEAR BALLS

PLACE NEAR BGA
0.1U/10V_4 C5057
4.7U/6.3V_6 C5058
4.7U/6.3V_6 C5059
+3V_GFX

**12~16 mils width**

VGPU_CORE_SENSE [36]
VSS_GPU_SENSE [36]

+3V_GFX
PLACE CLOSE TO BGA
C5048 4.7U/6.3V_6
C5050 1U/10V_6
C5052 0.1U/10V_4
C5053 0.1U/10V_4
C5055 0.1U/10V_4
C5056 0.1U/10V_4
PLACE CLOSE TO GPU BALLS

N13x
**N13P**

+3V_GFX
R5122 4.7K_4
[9,18] DGPU_PWROK — R5124 *0_4/S
PEX_CLKREQ# — Q5002 DTC144EUA
Q5008 DTC144EUA
CLK_PEGA_REQ# [8]

+3V
U5000 MC74VHC1G08DFT2G
C5015 0.1U/10V_4
[2,8,24,25,27,29] PLTRST#
[9] DGPU_HOLD_RST#
DGPU_HOLD_RST#
PEGX_RST#
R5125 100K_4
R5006 *330_4

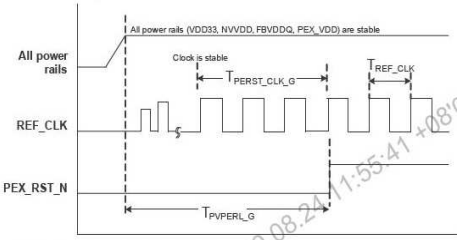
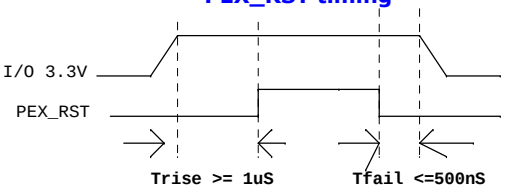



Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

| Constraint Parameter | Requirement | Notes |
|---|---|---|
| $T_{PVPERL\_G}$ | $T_{PVPERL\_G} \geq 1us$ | |
| $T_{PERST\_CLK\_G}$ | $T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$ | |

**PEX_RST timing**




[15,16,18,37] +1.05V_GFX
[7,16,17,18,36,37] +3V_GFX

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| A3 | DGPU 1/5 (PEG) | A |

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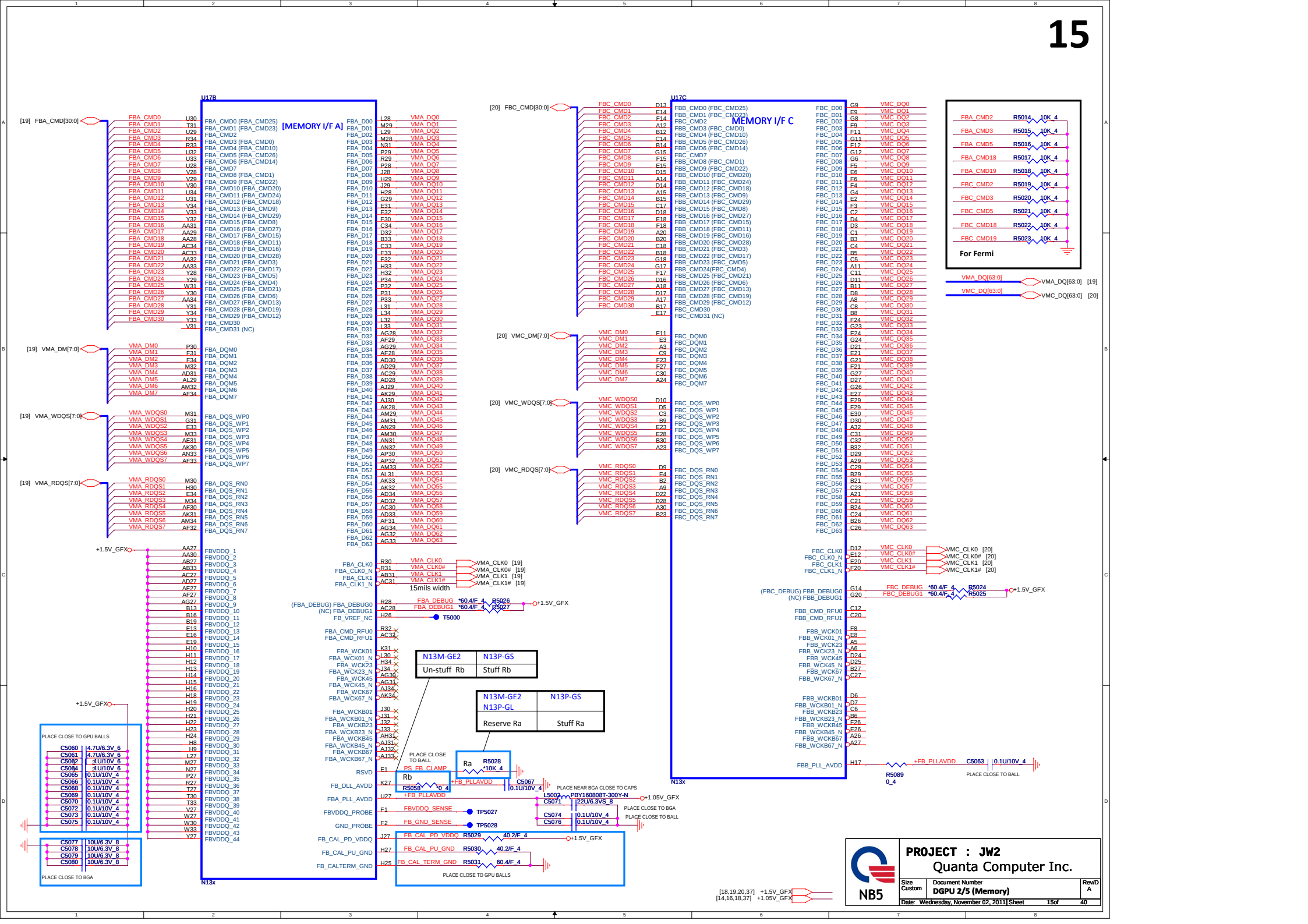
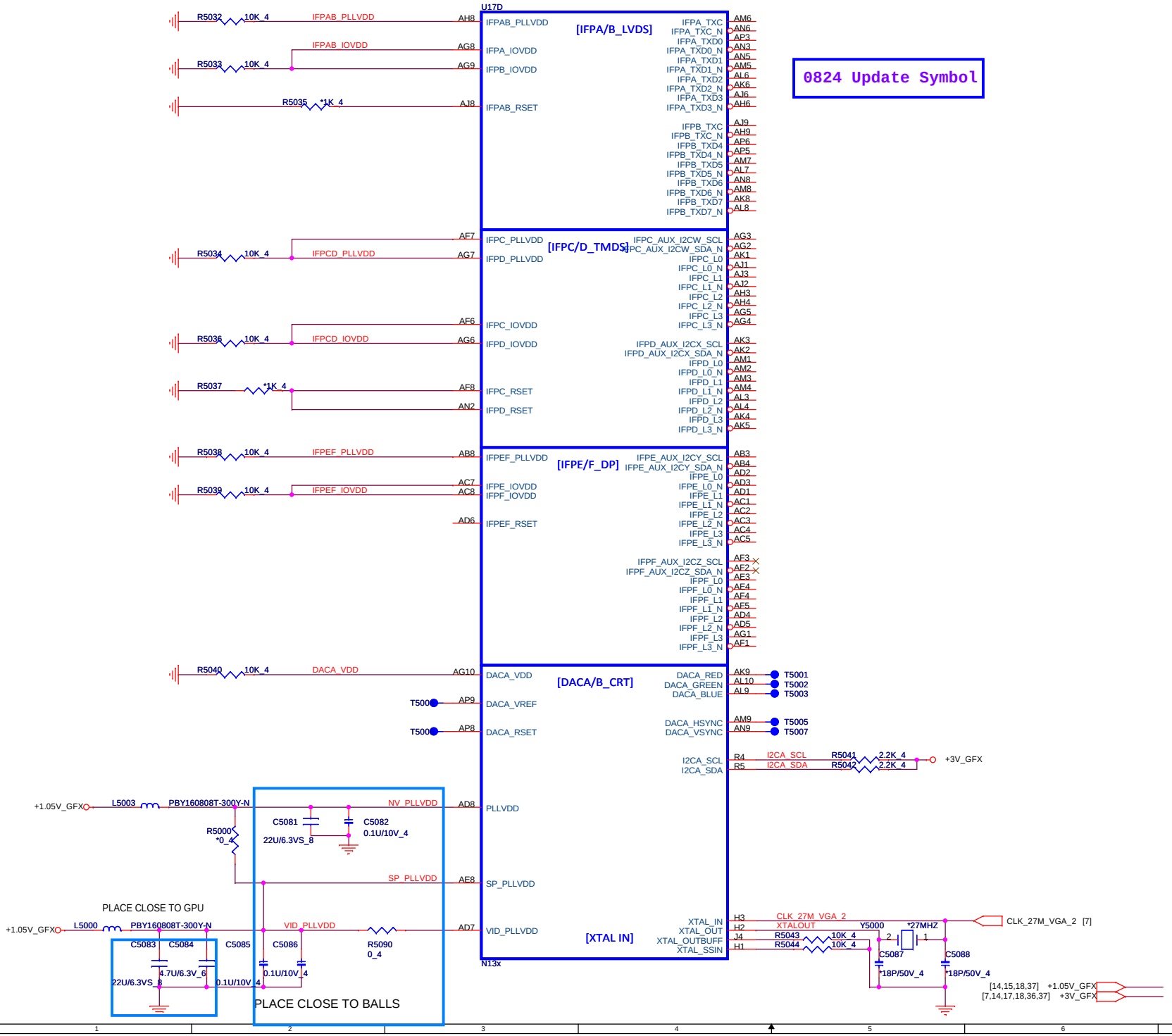

U17B
[MEMORY I/F A]
U17C
MEMORY I/F C
N13x
N13M-GE2 N13P-GS
Un-stuff Rb Stuff Rb
N13M-GE2 N13P-GS
N13P-GL
Reserve Ra Stuff Ra
15mils width
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
PLACE NEAR BGA CLOSE TO CAPS
PLACE CLOSE TO BGA
For Fermi
PROJECT : JW2
Quanta Computer Inc.
NB5
Document Number
DGPU 2/5 (Memory)
Size Custom
Rev D A
Date: Wednesday, November 02, 2011 Sheet 15 of 40




| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size A3 | Document Number<br>DGPU 3/5 (Display) | Rev/D A |
| Date: Wednesday, November 02, 2011 | Sheet 16of 40 | |

| Net name | N13M-GE2 | N13P-GS(QS) |
|---|---|---|
| ROM_SI | | |
| ROM_SO | PD 10K | PU 5K |
| ROM_SCLK | PD 15K | PD 10K |
| STRAP0 | PU 45K | PU 45K |
| STRAP1 | PD 35K | PD 35K |
| STRAP2 | PU 15K | PD 15K |
| STRAP3 | UN-STUFF | PD 5K |
| STRAP4 | UN-STUFF | PD 10K |

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

For N13M-GS (QS)
STRAP3 PD 5K
STRAP4 PD 10K
ROM_SCLK PD 10K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2

## Logical Strap Bit Mapping

| | PU-VDD | PD |
|---|---|---|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

Default: Hynix VRAM

| | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 | |
|---|---|---|---|---|---|
| ROM_SO | XCLK_417 | FB_0_BAR_SIZE | SMB_ALT_ADDR | VGA_DEVICE | 1001 |
| ROM_SCLK | PCI_DEVIDE[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM | 0011 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] | XXXX |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | 1111 |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | 0110 |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | 0111 |
| STRAP3 | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED | XXXX |
| STRAP4 | RESERVED | PCI SPEED CHANGE GEN3 | PCI_MAX SPEED | DP_PLL_VDD33 | XXXX |

VID 0 0 0 0 1 1 0 ---> 0.9V

| | N13M-GE2 | N13P-GS |
|---|---|---|
| Ra | Un-Stuff | Stuff |
| Qa | Stuff | Un-Stuff |

For N13M-GE2, N13M-GS (QS)
Defult : 2G Samsung

**VRAM Configuration Table**
ROM_SI
1G Hynix 64Mx16 -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD

## GPIO ASSIGNMENTS

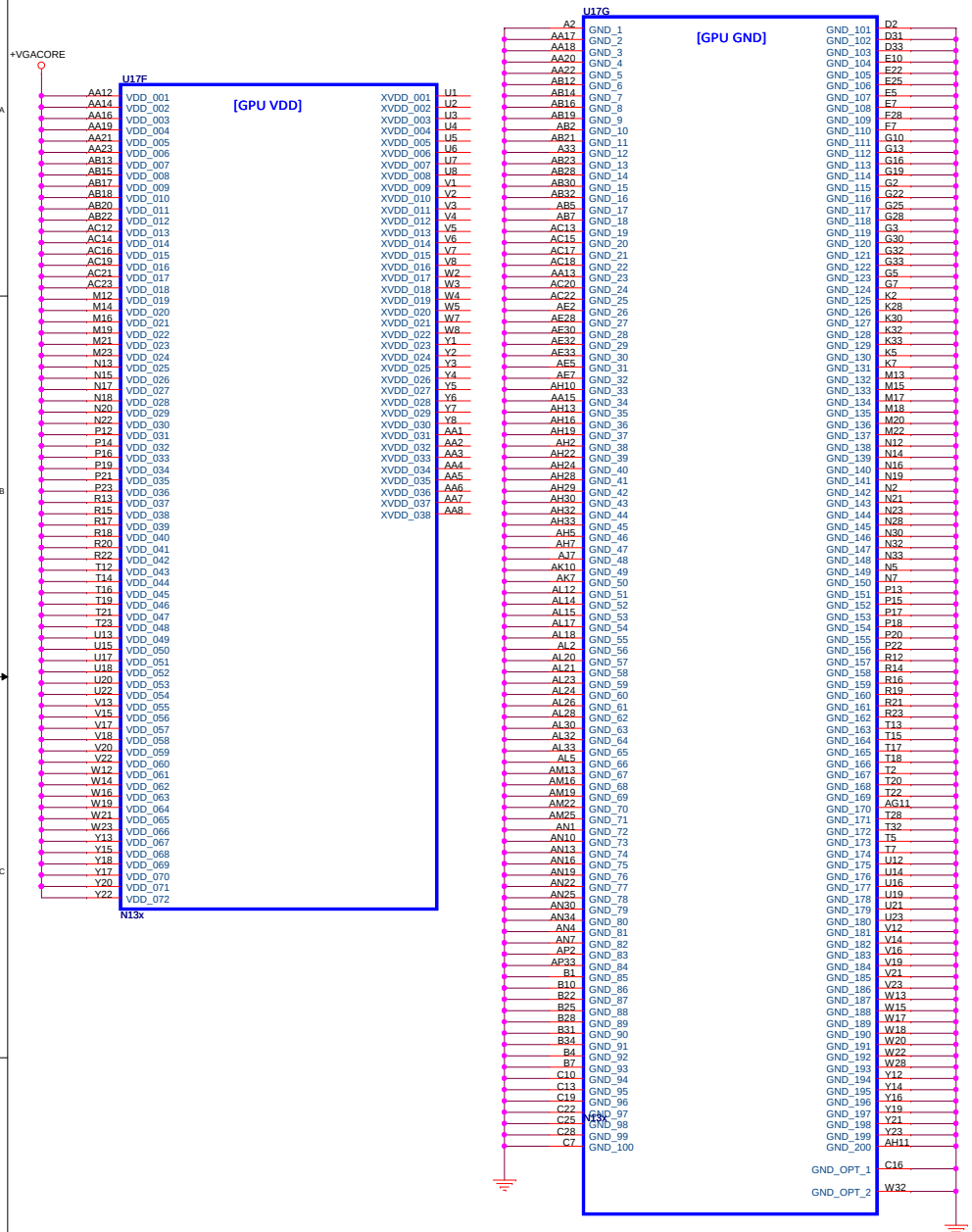
| GPIO | I/O | PIN | USAGE |
|---|---|---|---|
| 0 | OUT | GPU_VID4 | GPU CORE_VDD VID4 |
| 1 | OUT | GPU_VID3 | GPU CORE_VDD VID3 |
| 2 | OUT | LCD_BL_PWM | LCD BACKLIGHT PWM |
| 3 | OUT | LCD_VCC | PANEL POWER ENABLE |
| 4 | OUT | LCD_BLEN | PANEL BACKLIGHT ENABLE |
| 5 | OUT | GPU_VID1 | GPU CORE_VDD VID1 |
| 6 | OUT | GPU_VID2 | GPU CORE_VDD VID2 |
| 7 | OUT | 3D VISION | 3D VISION LEFT/RIGHT VISION |
| 8 | I/O | OVERT | ACTIVE LOW THERMAL OVER TEMP |
| 9 | I/O | ALERT | ACTIVE LOW THERMAL ALERT |
| 10 | OUT | MEM VREF | MEMMORY VREF CONTROL |
| 11 | OUT | GPU_VID0 | GPU CORE_VDD VID0 |
| 12 | IN | PWR_LEVEL | Power Detect ,HIGH=AC, LOW=DC |
| 13 | OUT | GPU_VID5 | GPU CORE_VDD VID5 |
| 14 | IN | HPD_AB | HOT PLUG DETECT FOR IFPAB |
| 15 | IN | HPD_C | HOT PLUG DETECT FOR IFPC |
| 16 | OUT | MEM VDD | MEMMORY VDD CONTROL |
| 17 | IN | HPD_D | HOT PLUG DETECT FOR IFPD |
| 18 | IN | HPD_E | HOT PLUG DETECT FOR IFPE |
| 19 | IN | HPD_F | HOT PLUG DETECT FOR IFPF |
| 20/21 | | RESERVE | |

| N13M-GE2 N13P-GL | N13P-GS |
|---|---|
| Stuff Rc | Un-stuff Rc |

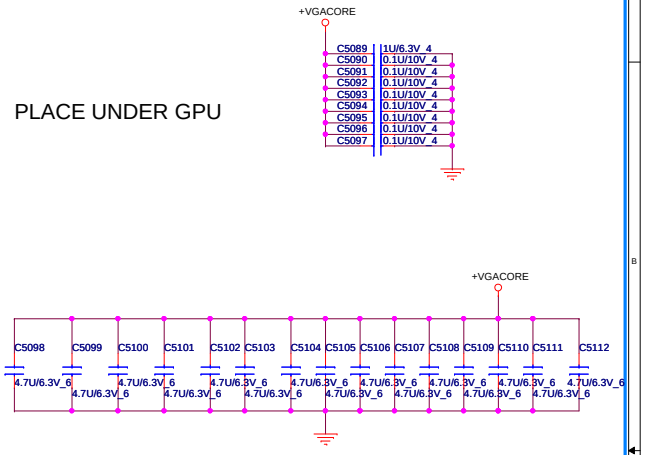
GFx SMBus Isolation

11/8 change for GPU temp detect

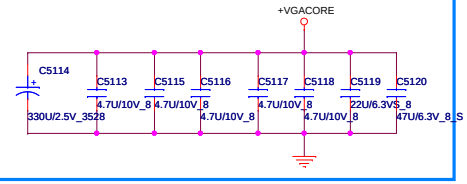
PROJECT : JW2
Quanta Computer Inc.
NB5
Size Custom | Document Number DGPU 4/5 (MIO/GPIO) | Rev/D A
Date: Wednesday, November 02, 2011 | Sheet 17of 40

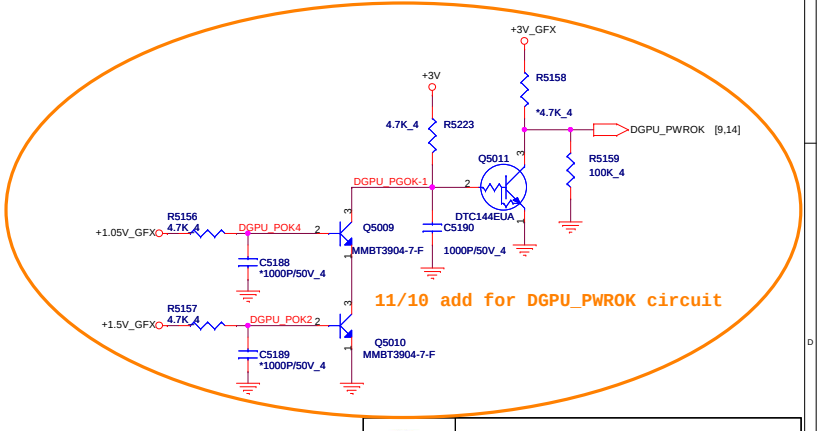



PLACE UNDER GPU

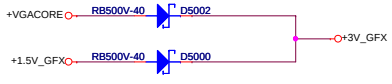



PLACE NEAR GPU




for meet Power down sequence for +3V_GFX




[36] +VGACORE
[14,15,16,37] +1.05V_GFX
[15,19,20,37] +1.5V_GFX
[7,14,16,17,36,37] +3V_GFX
[2,6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,34,36,38,40] +3V

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DGPU 5/5 (Power/Ground) | A |

Date: Wednesday, November 02, 2011 | Sheet 18 of 40

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

# CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

VRAM3 / VRAM8 / VRAM4 / VRAM7
96-BALL SDRAM DDR3
VRAM _DDR3_SAMSUNG_128MX16

Should be 240 Ohms +-1%
R5224 243/F_4
R5163 243/F_4
R5164 243/F_4
R5165 243/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R5170 162/F_4 VMA_CLK0 VMA_CLK0#
R5171 162/F_4 VMA_CLK1 VMA_CLK1#

R5166 1.33K/F_4 VREFC_VMA1 R5172 1.33K/F_4 C5191 0.1U/10V_4
R5167 1.33K/F_4 VREFD_VMA1 R5173 1.33K/F_4 C5192 0.1U/10V_4
R5168 1.33K/F_4 VREFC_VMA3 R5174 1.33K/F_4 C5193 0.1U/10V_4
R5169 1.33K/F_4 VREFD_VMA3 R5175 1.33K/F_4 C5194 0.1U/10V_4

[15] FBA_CMD17 FBA_CMD17 TP2021
[15] FBA_CMD1 FBA_CMD1 TP2022

+1.5V_GFX

C5207 1U/6.3V_4
C5211 1U/6.3V_4
C5215 1U/6.3V_4
C5220 1U/6.3V_4

C5201 10U/6.3V_8
C5205 1U/6.3V_4
C5208 1U/6.3V_4
C5212 1U/6.3V_4
C5216 1U/6.3V_4
C5221 1U/6.3V_4

C5195 10U/6.3V_8
C5197 1U/6.3V_4
C5200 1U/6.3V_4
C5202 1U/6.3V_4
C5209 1U/6.3V_4
C5213 1U/6.3V_4
C5217 1U/6.3V_4
C5222 1U/6.3V_4

C5196 10U/6.3V_8
C5198 10U/6.3V_8
C5203 0.1U/10V_4
C5206 0.1U/10V_4
C5210 0.1U/10V_4
C5218 0.1U/10V_4
C5223 0.1U/10V_4

C5199 10U/6.3V_8
C5204 10U/6.3V_8
C5214 0.1U/10V_4
C5219 0.1U/10V_4
C5224 0.1U/10V_4

[15,18,20,37] +1.5V_GFX

NB5

PROJECT : JW2
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | DGPU Memory 1/2 (DDR3) | 1A |

Date: Wednesday, November 02, 2011 Sheet 19 of 40

# CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

VRAM5 / VRAM1 / VRAM2 / VRAM6

96-BALL SDRAM DDR3
VRAM _DDR3_SAMSUNG_128MX16

Should be 240 Ohms +-1%

R5176 243/F_4
R5177 243/F_4
R5178 243/F_4
R5179 243/F_4

+1.5V_GFX

R5180 1.33K/F_4
R5181 1.33K/F_4
R5182 1.33K/F_4
R5183 1.33K/F_4
R5184 162/F_4
R5185 162/F_4
R5186 1.33K/F_4
R5187 1.33K/F_4
R5188 1.33K/F_4
R5189 1.33K/F_4
C5225 0.1U/10V_4
C5226 0.1U/10V_4
C5227 0.1U/10V_4
C5228 0.1U/10V_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

C5229 10U/6.3V_8
C5230 10U/6.3V_8
C5235 1U/6.3V_4
C5240 1U/6.3V_4
C5241 1U/6.3V_4
C5244 1U/6.3V_4
C5245 1U/6.3V_4
C5248 1U/6.3V_4
C5249 1U/6.3V_4
C5252 1U/6.3V_4
C5231 0.1U/10V_4
C5233 0.1U/10V_4
C5236 0.1U/10V_4
C5238 0.1U/10V_4
C5242 0.1U/10V_4
C5246 0.1U/10V_4
C5250 0.1U/10V_4
C5253 0.1U/10V_4
C5232 1U/6.3V_4
C5234 1U/6.3V_4
C5237 1U/6.3V_4
C5239 1U/6.3V_4
C5243 1U/6.3V_4
C5247 1U/6.3V_4
C5251 1U/6.3V_4
C5254 1U/6.3V_4

[15] FBC_CMD17 — FBC_CMD17 — TP2023
[15] FBC_CMD1 — FBC_CMD1 — TP2024

[15,18,19,37] +1.5V_GFX

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

NB5

PROJECT : JW2
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | DGPU Memory 2/2 (DDR3) | 1A |

Date: Wednesday, November 02, 2011 Sheet 20 of 40

## USB Camera Connector

MIC

[23] DIGITAL_D1
[23] DIGITAL_CLK
L32 SBK160808T-301Y-N DIGITAL_D1_R
L31 SBK160808T-301Y-N DIGITAL_CLK_R

[8] USBP5-
[8] USBP5+
CAMERA
L30 *WCM2012-90
USBP5-
USBP5+

C495 100P/50V_4
C494 100P/50V_4
EMI request

Change to USB port 11
for BIOS request0218

+5V
C16 0.01U/16V_4
C18 *4.7U/6.3V_6

C492 *10P/50V_4 USBP5-
C491 *10P/50V_4 USBP5+
C497 33P/50V_4 DIGITAL_D1
C496 33P/50V_4 DIGITAL_CLK

20110817 CAMERA REGULATOR DEL

EMI request

+3V
C41 0.1U/10V_4
C6 0.1U/10V_4
C4 0.1U/10V_4
C2 0.1U/10V_4
C20 0.1U/10V_4
C5 0.1U/10V_4
C3 0.1U/10V_4

+5V
C49 0.1U/10V_4
C47 0.1U/10V_4
C45 0.1U/10V_4
C43 0.1U/10V_4
C48 0.1U/10V_4
C46 0.1U/10V_4
C44 0.1U/10V_4
C42 0.1U/10V_4

+3V
R17 2.2K_4
R16 2.2K_4
[6] PCH_EDIDCLK
[6] PCH_EDIDDATA
PCH_EDIDCLK
PCH_EDIDDATA

+3V
C5318 1U/6.3V_4
U5001
IN
IN
ON/OFF
OUT
GND
IC(5P) G5243AT11U
[6] PCH_DISP_ON
PCH_DISP_ON
R5190 100K_4

+LCDVCC
L5 FBM2125 HM330-T
+3VLCD_CON
C11 *0.01U/16V_4
C13 0.1U/10V_4
C7 *10U/6.3V_8

20110817 Change to G5243AT11U

[6] PCH_DPST_PWM
PCH_DPST_PWM

[29] LID_CONTROL
LID_CONTROL
D5 RB500V-40
R8 100K_4
C10 22P/50V_4
BLON_CON
R9 47K/F_4
+3VPCU
[6] PCH_LVDS_BLON
PCH_LVDS_BLON
R15 1K_4
D6 *RB500V-40
LID_EC# [28,29]
R20 100K_4
[8] LCD_BK
Q9 *DTC144EUA

+3VLCD_CON
C14 1000P/50V_4
+3V
PCH_EDIDCLK
PCH_EDIDDATA
[6] PCH_LA_DATAN0
[6] PCH_LA_DATAP0
PCH_LA_DATAN0
PCH_LA_DATAP0
[6] PCH_LA_DATAN1
[6] PCH_LA_DATAP1
PCH_LA_DATAN1
PCH_LA_DATAP1
[6] PCH_LA_DATAN2
[6] PCH_LA_DATAP2
PCH_LA_DATAN2
PCH_LA_DATAP2
[6] PCH_LA_CLK#
[6] PCH_LA_CLK
PCH_LA_CLK#
PCH_LA_CLK
[6] PCH_LB_DATAN0
[6] PCH_LB_DATAP0
PCH_LB_DATAN0
PCH_LB_DATAP0
[6] PCH_LB_DATAN1
[6] PCH_LB_DATAP1
PCH_LB_DATAN1
PCH_LB_DATAP1
[6] PCH_LB_DATAN2
[6] PCH_LB_DATAP2
PCH_LB_DATAN2
PCH_LB_DATAP2
[6] PCH_LB_CLK#
[6] PCH_LB_CLK
PCH_LB_CLK#
PCH_LB_CLK
DIGITAL_D1_R
DIGITAL_CLK_R
+5V
USBP5-
USBP5+
C15 *4.7U/6.3V_6
C17 *0.1U/10V_4
PCH_DPST_PWM
BLON_CON
+VIN_BLIGHT
CN11
GS12401-1011-9F

+VIN_BLIGHT
+VIN
L6 FBM2125 HM330-T +VIN_BLIGHT
C12 0.1U/50V_6
C490 *10U/25V_12
C8 0.1U/50V_6
C9 0.01U/25V_4

[2,6,7,8,9,10,12,13,14,18,22,23,24,25,27,28,29,34,36,38,40] +3V
[7,26,27,28,29,30,31] +3VPCU
[7,10,22,23,27,28,40] +5V
[30,31,32,34,36,37,39,40] +VIN
[37,40] +12VALW
[10,23,26,31,32,33,34,35,36,38,39,40] +5VS5

| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: LCD Connector (LVDS) | Rev: D A |
| Date: Wednesday, November 02, 2011 | Sheet: 21 of 40 | |

# CRT PORT

40 MIL

40 mils F5 FUSE1A6V_POLY +5V 2 1 +5VCRT +5VCRT
C24 0.1U/10V_4
SSM14 spec is 40V 1A

D8 RB500V-40 +5VCRT 2 1 +5V_CRT2

[6] PCH_CRT_R L8 BLM18BA470SN1D CRT_R_CON
[6] PCH_CRT_G L9 BLM18BA470SN1D CRT_G_CON
[6] PCH_CRT_B L7 BLM18BA470SN1D CRT_B_CON
+5VCRT
R51 R52 R53 150/F_4
C40 C39 C38 6.8P/50V_4
C34 C36 C37 6.8P/50V_4
EMI
CRT CONN CN13
CRT_DDCDATA_CON C33 *470P/50V_4
CRT_HSYNC_CON C32 *47P/50V_6
CRT_VSYNC_CON C28 *47P/50V_6
CRT_DDCCLK_CON C26 *470P/50V_4

U7 IP4772
+5V_CRT2
+5V C35 0.22U/25V_6 CRT_BYP
+3V
VCC_SYNC SYNC_OUT2 SYNC_OUT1
VCC_DDC BYP
VCC_VIDEO SYNC_IN2 SYNC_IN1
VIDEO_1 VIDEO_2 VIDEO_3 DDC_IN1 DDC_IN2 DDC_OUT1 DDC_OUT2
GND
CRT_VSYNC1 R54 22_4 CRT_VSYNC_CON
CRT_HSYNC1 R66 22_4 CRT_HSYNC_CON
PCH_VSYNC PCH_HSYNC
PCH_VSYNC [6] PCH_HSYNC [6]
R58 2.2K_4 R64 2.2K_4
CRT_R_CON CRT_G_CON CRT_B_CON
PCH_DDCCLK PCH_DDCDATA
PCH_DDCCLK [6] PCH_DDCDATA [6]
CRT_DDCCLK_CON CRT_DDCDATA_CON
PCH_DDCCLK R59 2.7K_4
PCH_DDCDATA R60 2.7K_4

# HDMI PORT

## HDMI SMBus Isolation

+3V R486 2.2K_4 Q46 2N7002DW
[6] SDVO_CLK HDMI_SCL_R HDMI_SCLK
[6] SDVO_DATA HDMI_SDA_R HDMI_SDATA
R492 2.2K_4

for EMI request
+5VCRT C238 *0.01U/16V_4

## EMI Solution

C_TX2_HDMI+ R165 *0_4 C_TX2_HDMI-
C_TX1_HDMI+ R159 *0_4 C_TX1_HDMI-
C_TX0_HDMI+ R153 *0_4 C_TX0_HDMI-
C_IN_CLK R147 *0_4 C_IN_CLK#
R475 0_4
C_IN_CLK C_IN_CLK# RP17 *WCM2012-90 C_TXC_HDMI+ C_TXC_HDMI-
R472 0_4

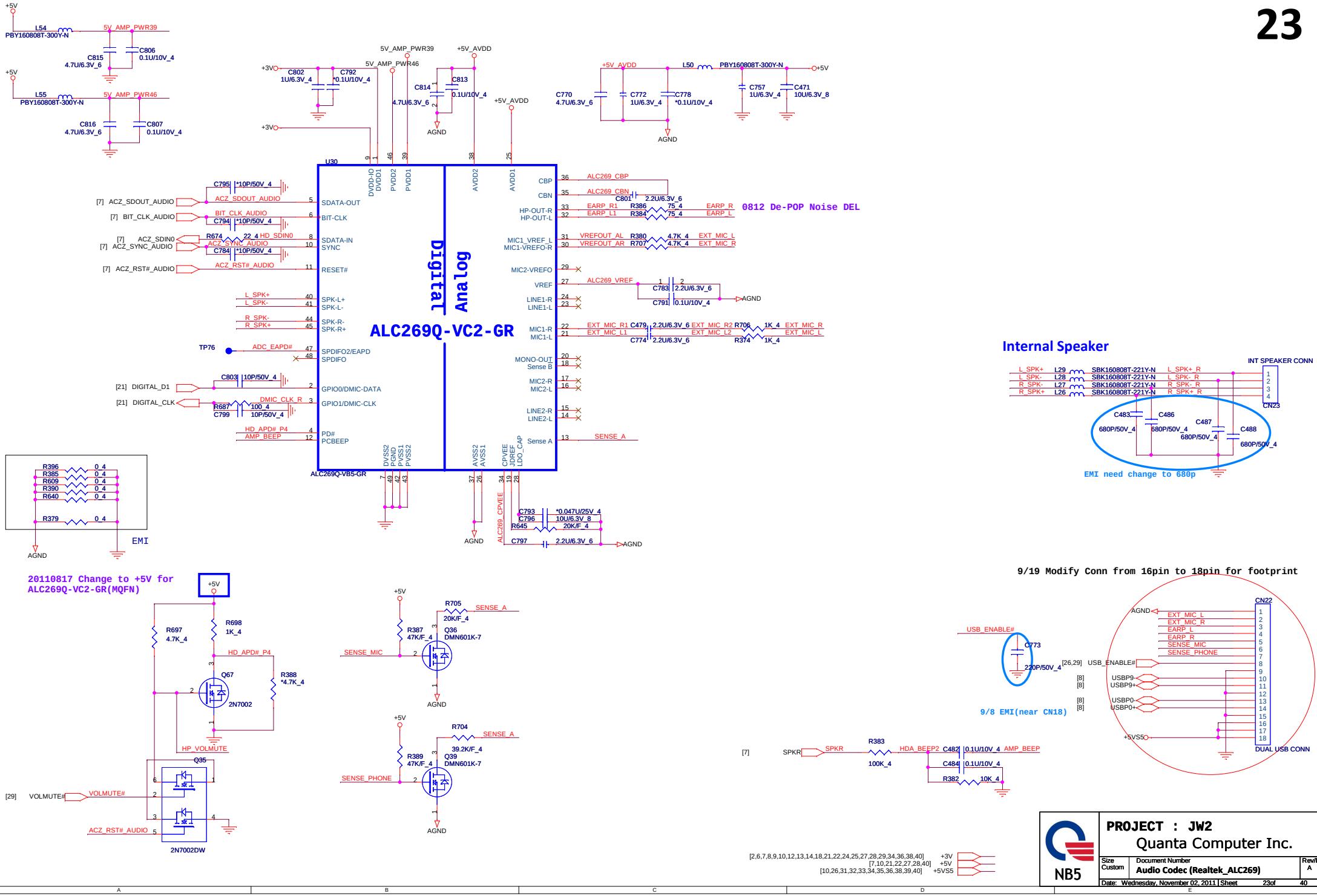
CN17 HDMI CONN_4 pin GND
[6] IN_D2 C300 0.1U/10V_4 C_TX2_HDMI+
[6] IN_D2# C297 0.1U/10V_4 C_TX2_HDMI-
[6] IN_D1 C290 0.1U/10V_4 C_TX1_HDMI+
[6] IN_D1# C287 0.1U/10V_4 C_TX1_HDMI-
[6] IN_D0 C284 0.1U/10V_4 C_TX0_HDMI+
[6] IN_D0# C281 0.1U/10V_4 C_TX0_HDMI-
[6] IN_CLK C280 0.1U/10V_4 C_IN_CLK C_TXC_HDMI+
[6] IN_CLK# C273 0.1U/10V_4 C_IN_CLK# C_TXC_HDMI-
RB500V-40
+5V D22 D21 RB500V-40 5V_HSMBCK 5V_HSMBDT R484 2.2K_4 R483 2.2K_4 HDMI_SCLK HDMI_SDATA
C249 C258 *10P/50V_4
+5VCRT
HDMI_HPD R121 0_4 HDMI_DET_C
C227 220P/50V_4
add for EMI
D9 BAV99W R129 110K/F_4
B-stage change

Q43 MMBT3904-7-F R460 150K/F_4 R458 10K_4
[6] HDMI_HPD_CON HDMI_HPD_CON HDMI_DET_P HDMI_HPD

Q24 2N7002
DGPU_CL_HDMIP R488 680/F_4 C_TX2_HDMI+ R487 680/F_4 C_TX2_HDMI-
R485 680/F_4 C_TX1_HDMI+ R482 680/F_4 C_TX1_HDMI-
R481 680/F_4 C_TX0_HDMI+ R478 680/F_4 C_TX0_HDMI-
R148 680/F_4 C_IN_CLK R144 680/F_4 C_IN_CLK#

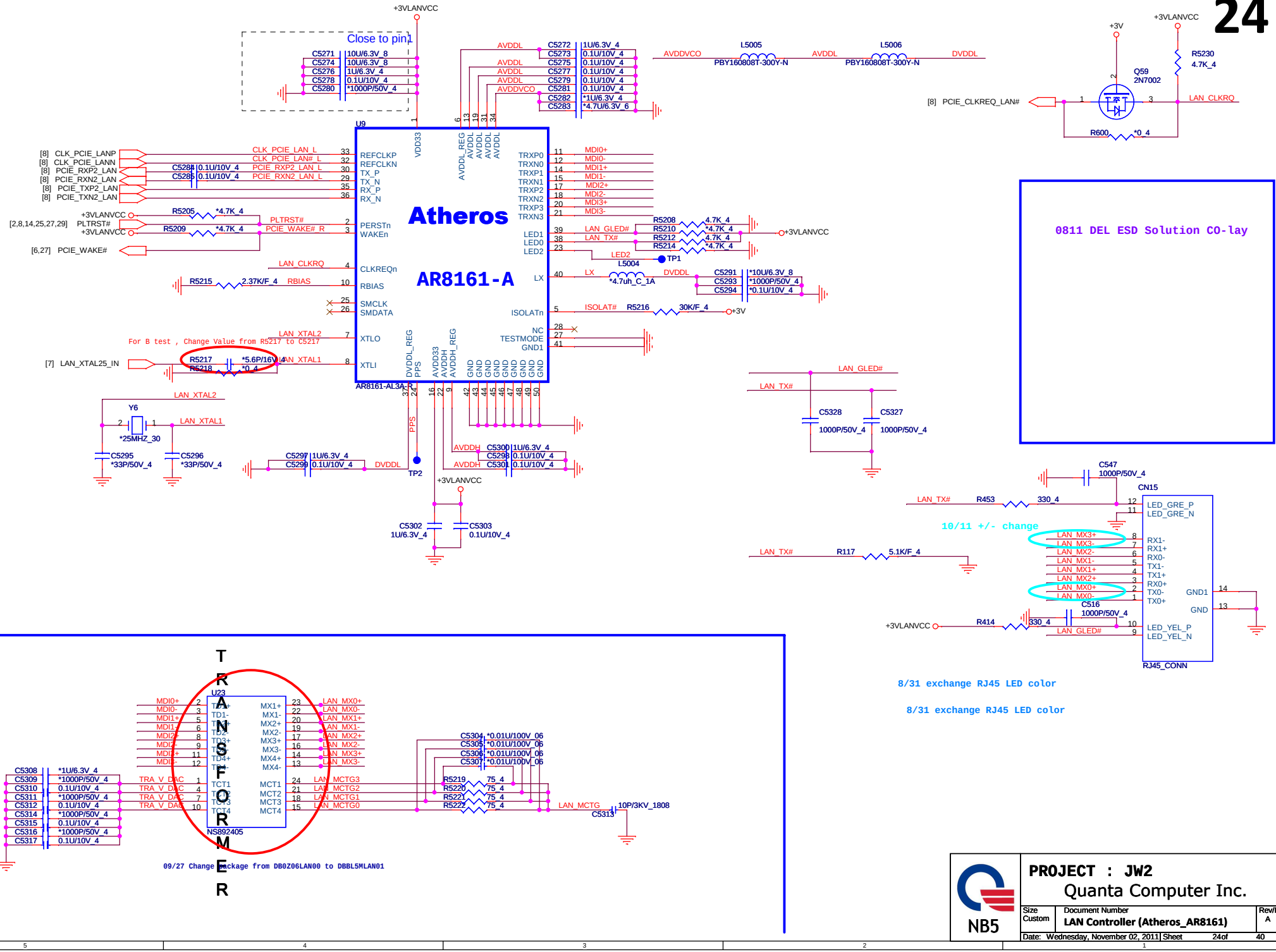
9/1 change to 680ohm
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm

NB5
PROJECT : JW2
Quanta Computer Inc.
Size Custom | Document Number CRT/HDMI Connector | Rev/D A
Date: Wednesday, November 02, 2011 | Sheet 22of 40


ALC269Q-VC2-GR
Digital
Analog
U30
ALC269Q-VB5-GR
0812 De-POP Noise DEL
EMI need change to 680p
Internal Speaker
INT SPEAKER CONN
DUAL USB CONN
20110817 Change to +5V for ALC269Q-VC2-GR(MQFN)
9/19 Modify Conn from 16pin to 18pin for footprint
9/8 EMI(near CN18)
2N7002
2N7002DW
PROJECT : JW2
Quanta Computer Inc.
NB5
Audio Codec (Realtek_ALC269)

# Atheros Lan





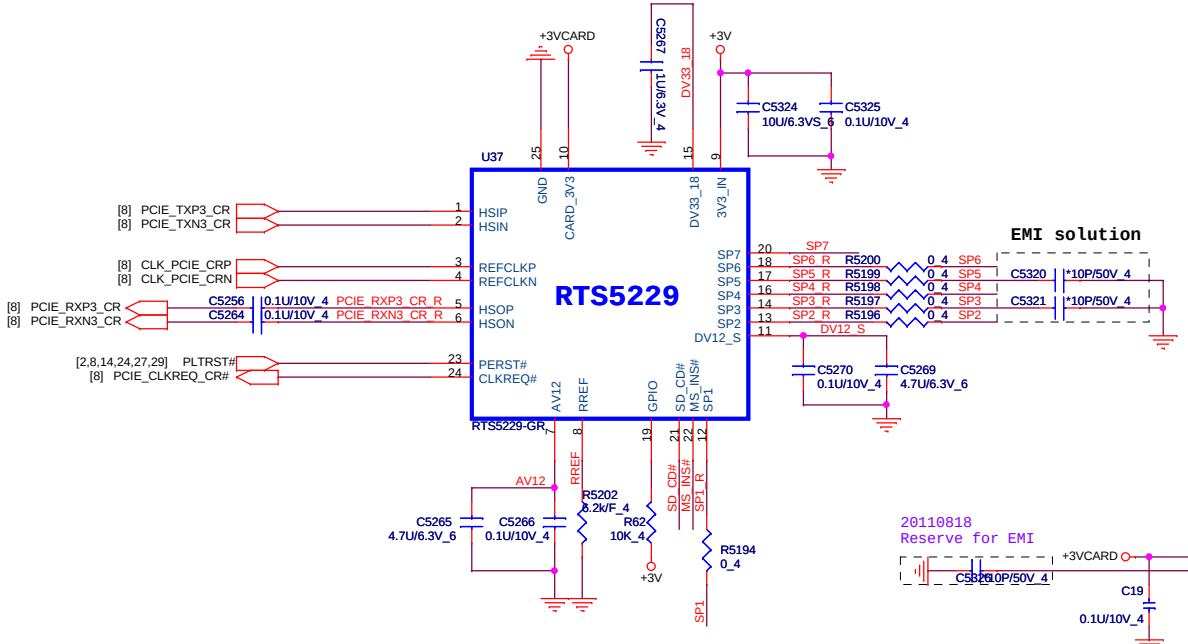

**PROJECT : JW2**

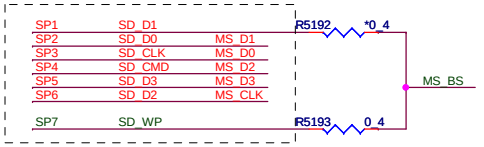
Quanta Computer Inc.

NB5

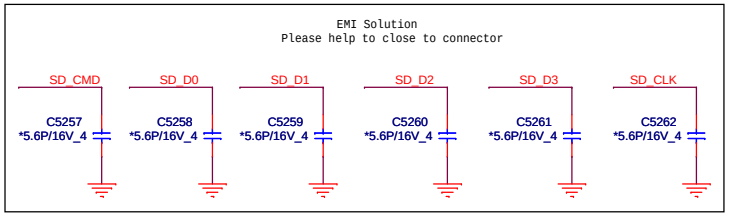
| Size | Document Number | Rev/D |
|---|---|---|
| Custom | LAN Controller (Atheros_AR8161) | A |

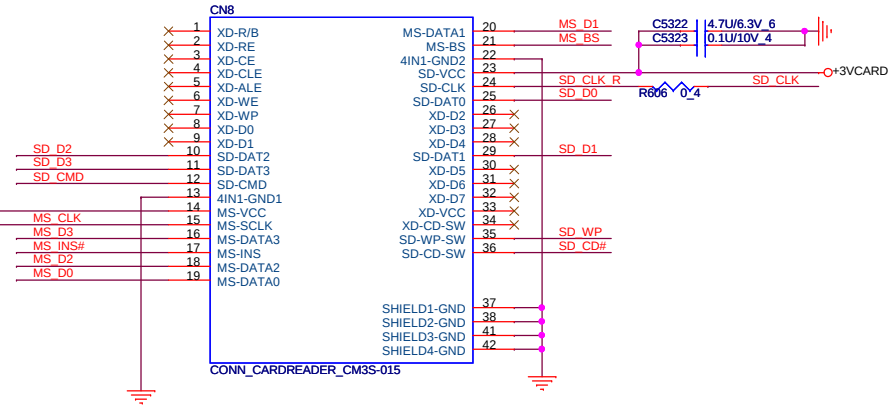
Date: Wednesday, November 02, 2011 | Sheet 24of 40




## Share Pin

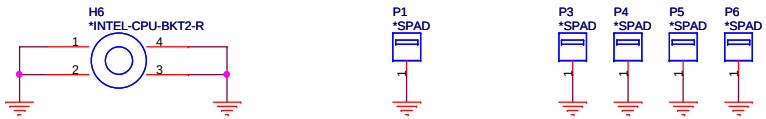


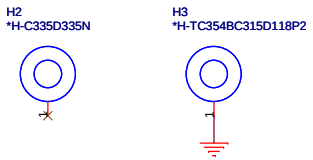



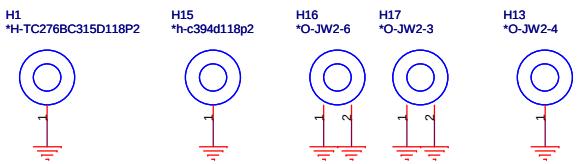

**Note:**

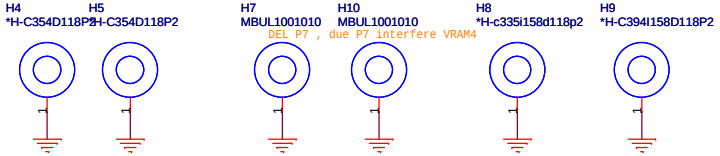
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

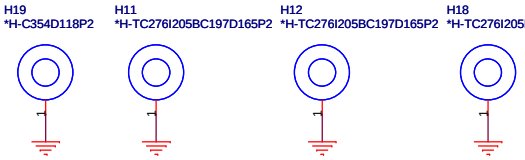
## CPU Bracket




NB5

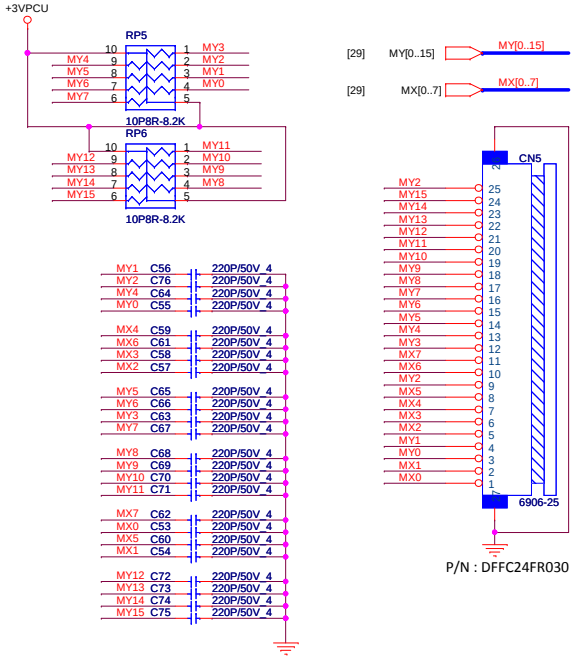
**PROJECT : JW2**

Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | Card Reader control (RT5229) | A |

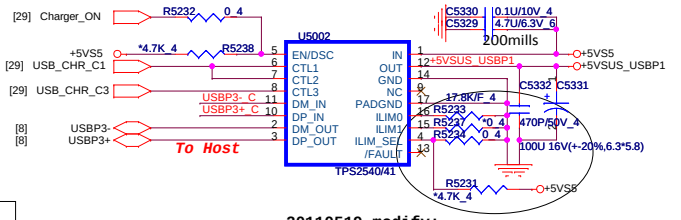
Date: Wednesday, November 02, 2011 | Sheet 25of 40

# Keyboard Connector




P/N : DFFC24FR030

# Charger USB

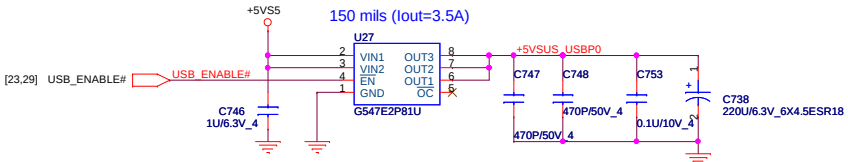



**20110519 modify:**
**Add R338, R776, R353 for reserve TPS2543.**

| CTL1 | CTL2 | CTL3 | TPS2540 Control Truth Table |
|---|---|---|---|
| 0 | 0 | 0 | Out Discharge ,Power switch OFF |
| 0 | X | 1 | Dedicated charging port, auto-detect (DCP) |
| X | 1 | 0 | Standard downstream port, USB 2.0 Mode (SDP) |
| 1 | 1 | 1 | Charging downstream port, BC1.2 (draft).(CDP) |

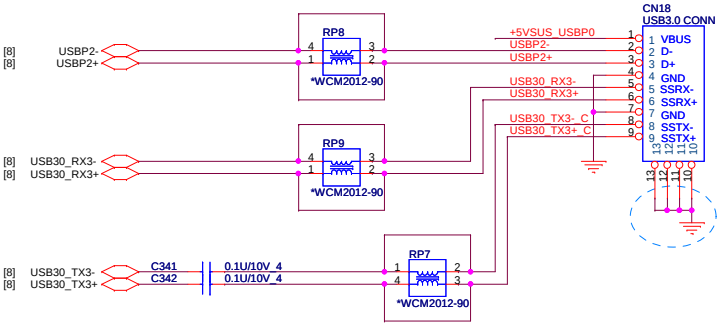
| LGE SPEC | S0/S3 | | S4/S5 | |
|---|---|---|---|---|
| | AC Mode | DC Mode | AC Mode | DC Mode |
| change mode | CDP | CDP | DCP | DCP |
| user define and wake up | | SDP | | OFF |

[2,6,7,8,9,10,12,13,14,18,21,22,23,24,25,27,28,29,34,36,38,40] +3V
[10,23,31,32,33,34,35,36,38,39,40] +5VS5
[7,21,27,28,29,30,31] +3VPCU



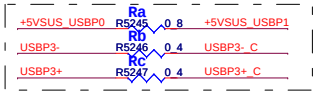

# USB3.0 X 2/USB2.0 COMBO

USB 3.0

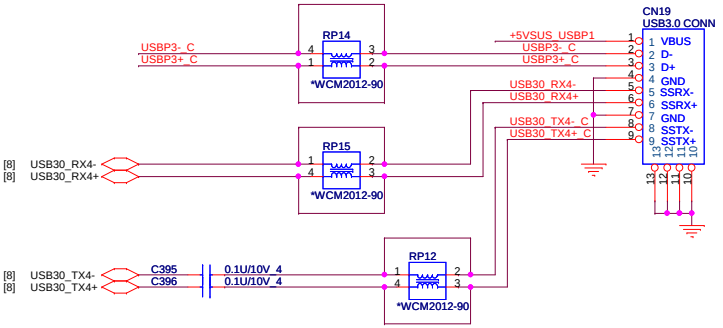



**USB CHARGER OPTION**

| U5002 | Ra | Rb | Rc |
|---|---|---|---|
| STUFF | UNSTUFF | UNSTUFF | UNSTUFF |
| UNSTUFF | STUFF | STUFF | STUFF |




USB 3.0



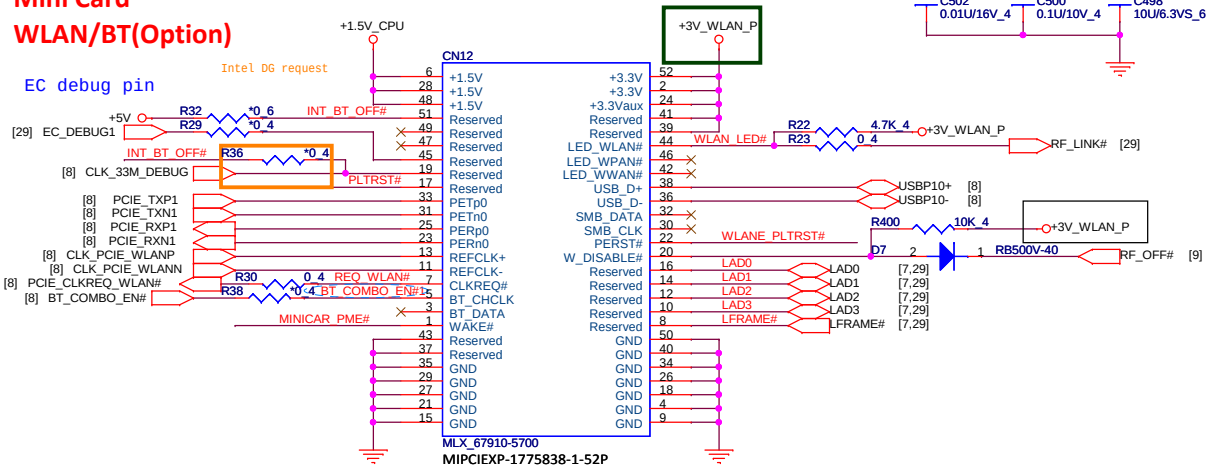

NB5

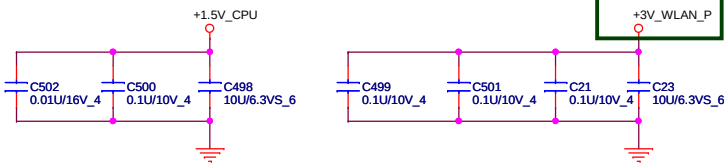
**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | USB 3.0/KEY Connector | A |

Date: Wednesday, November 02, 2011 | Sheet 26of 40

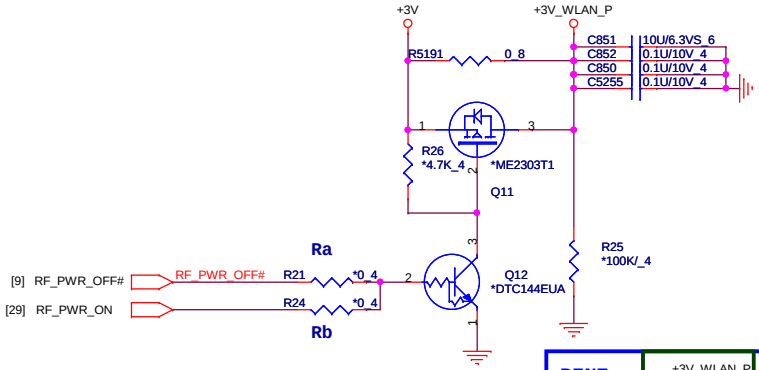
# Mini Card WLAN/BT(Option)



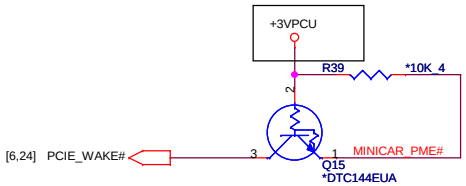





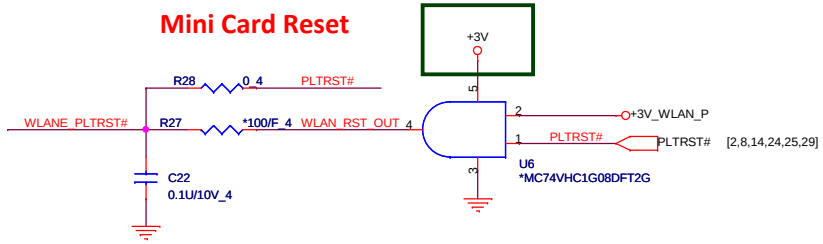




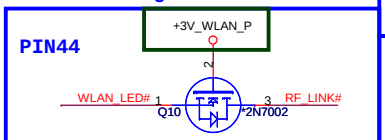

## Support Wake Function(Reserve)

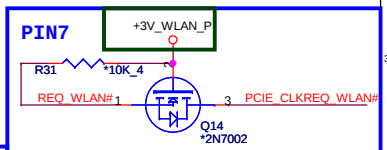


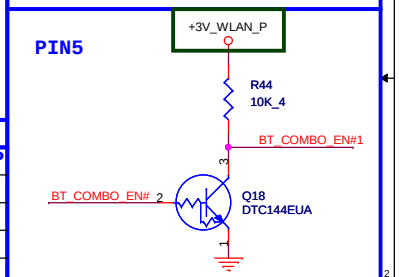

## Mini Card Reset




## Avoid leakage issue

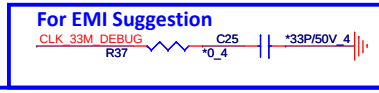


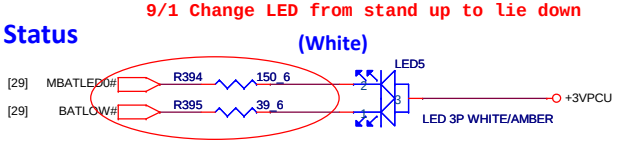

**LGE mini-pcie power status**

| WLAN | Bluetooth | +3V_WLAN_P |
|---|---|---|
| Radio-ON | Radio-ON | Power-ON |
| Radio-ON | Radio-OFF | Power-ON |
| Radio-OFF | Radio-ON | Power-ON |
| Radio-OFF | Radio-OFF | Power-OFF |



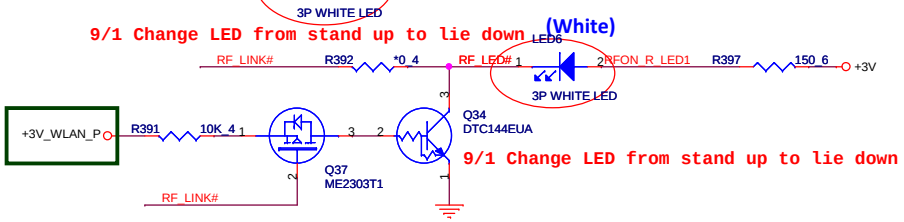

## LED Status

9/1 Change LED from stand up to lie down



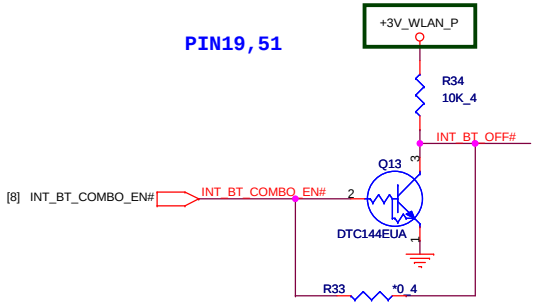


9/1 Change LED from stand up to lie down




9/1 Change LED from stand up to lie down

## PIN19,51




9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

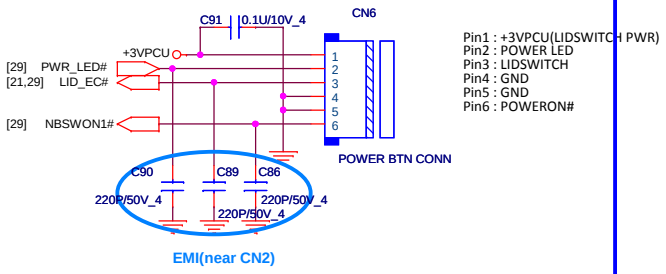
[2,6,7,8,9,10,12,13,14,18,21,22,23,24,25,28,29,34,36,38,40] +3V
[7,10,21,22,23,28,40] +5V
[7,21,26,28,29,30,31] +3VPCU
[2,4,10] +1.5V_CPU

NB5

**PROJECT : JW2**
Quanta Computer Inc.

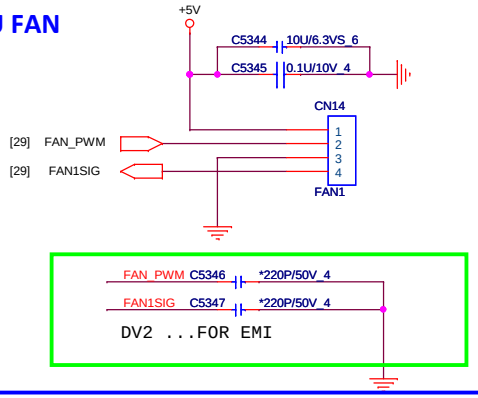
| Size | Document Number | Rev/D |
|---|---|---|
| Custom | Audio Codec (Realtek_ALC269) | A |
| Date: Wednesday, November 02, 2011 | Sheet 27of 40 | |

## Power Botton Connector



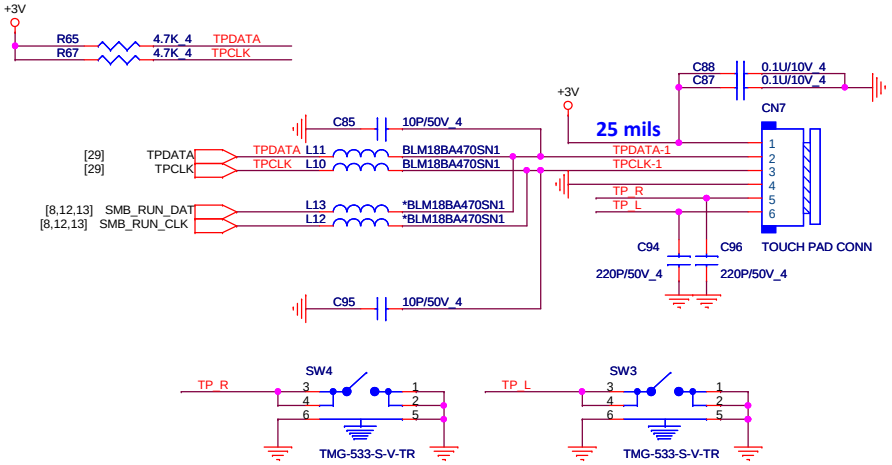

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

## CPU FAN

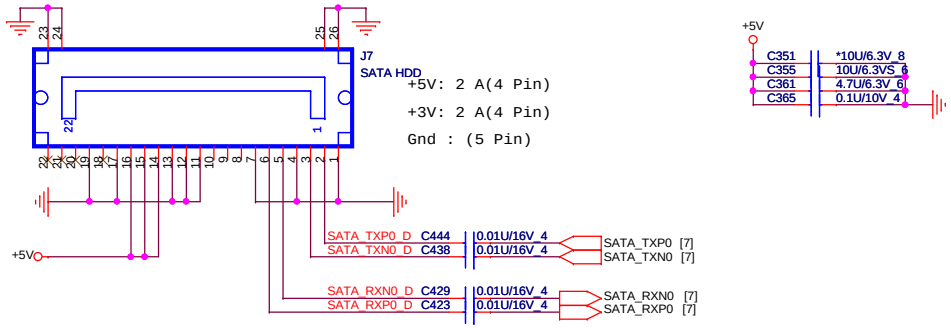



## Touch Pad Connector

B-stage change footprint to BL121-12R-TAND-12P-L




## SATA HDD Connector

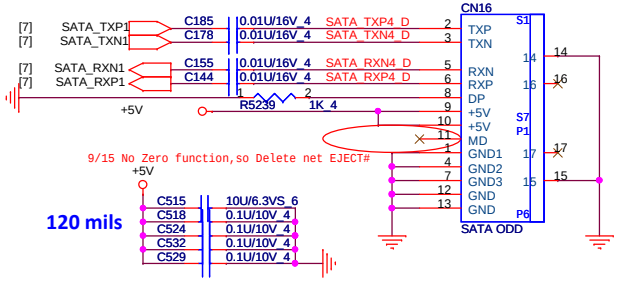



## Finger Print Connector

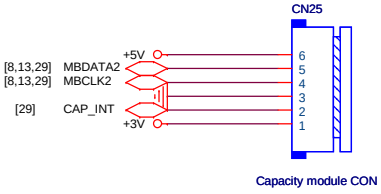
## SATA ODD Connector

0812 ODD ZERO PWR DEL

20110818 ODD_PRSNT DEL




## Capacity module Connector




[2,6,7,8,9,10,12,13,14,18,21,22,23,24,25,27,29,34,36,38,40] +3V
[7,10,21,22,23,27,40] +5V
[7,21,26,27,29,30,31] +3VPCU
[2,4,10,27] +1.5V_CPU
[37,40] +12VALW

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev/D |
|---|---|---|
| Custom | SATA HDD/ODD/MSATA CONN | A |
| Date: Wednesday, November 02, 2011 | Sheet 28of 40 | |

Select Pin

Rb R228 10K_4 CB/LG Ra R214 *10K_4 +3VPCU

| CB/LG Select | |
|---|---|
| LG | Ra |
| CB | Rb |

20110818
RTC XTAL DEL

+3V_ECACC L23 PBY160808T-300Y-N +3VPCU
C387 1U/6.3V_4 C384 1000P/50V_4
IT8502_AGND IT8502_AGND
+3v_STBY L25 BK1608HS121-T +3VPCU
C450 0.1U/10V_4
C465 0.1U/10V_4
+3V +3VPCU

U10

IT8518/BX

LPC
LAD0 LAD1 LAD2 LAD3 LPCRST#/WUI4/GPD2 LPCCLK LFRAME#
LPCPD#/WUI6/GPE6

GPIO
GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/BBO/GPC7
GPC0 TMA0/GPB2

PS/2
PS2DAT0/TMB1/GPF1 PS2CLK0/TMB0/GPF0
PS2DAT2/WUI21/GPF5 PS2CLK2/WUI20/GPF4

SM_BUS
SMCLK2/WUI22/GPF6/PECI SMDAT2/WUI23/GPF7 SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2

UART
DAC4/DCD0#/GPJ4 DSR0#/GPG6 GINT/CTS0#/GPD5 PS2DAT1/RTS0#/GPF3 DAC5/RIG0#/GPJ5 PS2CLK1/DTR0#/GPF2 RXD/SIN0/GPB0 TXD/SOUT0/GPB1

FLASH
GPG0 FSCK FMISO FMOSI FSCE# SSCE0#/GPG2

PWM
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/GPA7
TACH0/GPD6 TACH1/TMA1/GPD7
TMR0/WUI2/GPC4 TMR1/WUI3/GPC6

KBMX
KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7

WAKE UP
PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1
WUI5/GPE5
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7

A/D D/A
ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/WUI29/GPI5 ADC6/WUI30/GPI6 ADC7/WUI31/GPI7
DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3

CLOCK
CK32K CK32KE

IT8518E/HX

[7,27] LAD0 [7,27] LAD1 [7,27] LAD2 [7,27] LAD3 [2,8,14,24,25,27] PLTRST# [8] CLK_33M_KBC [7,27] LFRAME#
[6] SLP_S5
[9] EC_A20GATE [7] SERIRQ [9] SIO_EXT_SMI# [9] SIO_EXT_SC# [9] EC_RCIN#
D17 D19 D20 D18 RB500V-40 EC_WRST TP45
[30] D/C# [6] RSMRST#
H_PROCHOT# EC Charger_ON [26] Charger_ON
[28] TPDATA [28] TPCLK
CB/LG
[26] USB_CHR_C3 [31,32,33,34,35] HWPG [21] LID_CONTROL [27] RF_PWR_ON
[7] ACZ_SDOUT D23 RB500V-40
[27] EC_DEBUG1 [23,26] USB_ENABLE#
EC_SCK EC_SO EC_SI EC_CE#
[26] MY[0..15] MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7
[26] MX[0..7]

+3VPCU R321 470K_4 EC_WRST C467 0.1U/10V_4

BATLOW VRON [38]
PM_SLP_A# TP5021 EC_PWROK [6]
PM_SLP_LAN# TP5022 SUSON [32]
MBATLED0 R1 0_4 R2 0_4 R3 0_4 R4 0_4 PCH_SPI_SI [7] PCH_SPI_SO [7] PCH_SPI_CLK [7]
R5 0_4 R6 0_4 PCH_SPI_CS1# [7] PCH_SPI_CS0# [7]
MAINON [30,32,34,35,40] RF_LINK# [27] CLKRUN# [6]
EC_PECI_R R273 43_4 H_PECI [2]
CAP_INT [28] MBCLK [30] MBDATA [30] MBCLK2 [8,13,28] MBDATA2 [8,13,28]
For Battery charge
For PCH SMB/DDR Thermal IC/VGA and Cap board

LAN_POWER [40]
Num LK TP48 AC_PRESENT TP5023 SATA5GP_EC TP5024 FAN_PWM [28] SUS_PWR_ACK [6] VOLMUTE# [23]
D815 DEL PC_BEEP_EC
R5243 10K_4 R328 0_4 +3V FAN1SIG [28] 3VS5_ON [31]
SUSC# [6] 5VS5_ON [31]
LAN_S5_WAKE#
NBSWON1# NBSWON1# [28] LID_EC# [21,28] ACIN [30] SUSB# [6] PWR_LED

GPI0 GFX_HWPG_EC TP5026 SYS_I [30] AD_AIR [30] TEMP_MBAT [30]
SETVPRO TP72
9/15 Modify for EC
USB_CHR_C1 USB_CHR_C1 [26]
VFAN D13 RB500V-40 TP73 DNBSWON# [6]
R200 10K_4 +3VS5

R235 10K_4 GPI0 R233 *10K_4 +3VPCU

| Platfrom | ADC |
|---|---|
| JW2 | 0V |
| TWC | 0.75V |
| SW6C | 1.5V |
| CB3 | 2.25V |
| CB4 | 3V |

Select Pin

Rb R227 10K_4 SETVPRO R211 *10K_4 +3VPCU

| Vpro Select | |
|---|---|
| Vpro | Ra |
| Non-Vpro | Rb |

+3VPCU R287 10K_4 NBSWON1# C445 0.1U/10V_4

MBCLK MBDATA R255 10K_4 R258 10K_4 +3VPCU
TPCLK R225 *10K_4 TPDATA R224 *10K_4 MBCLK2 R265 10K_4 MBDATA2 R274 10K_4 +3V

Layout Note:
Place all capacitors close to IT8502N.

+3VPCU 12 MILS
C469 0.1U/10V_4 C418 0.1U/10V_4 C468 0.1U/10V_4 C431 0.1U/10V_4 C416 0.1U/10V_4 C386 0.1U/10V_4

R261 100K_4 H_PROCHOT#_EC Q38
[2,38] H_PROCHOT# 0_4 R253 H_PROCHOT#_Q
BATLOW
[27] BATLOW#
2N7002DW

Q47
PWR_LED [28] PWR_LED#
MBATLED0 [27] MBATLED0#
2N7002DW

thermal shutdown circuit
EC_WRST R195 10K_4 +3V
Q30 OVT_DETC EC_PWROK D12 *RB500V-40
*MMBT3904-7-F
SYS_SHDN-1# D10 DGPU_OVT# *RB500V-40 DGPU_OVT# [47]
EC_CT_UP R186 *4.7K_4 +1.05V
C359 220P/50V_4
PV Change
PM_THRMTRIP# [2,9]
Q29 *MMBT3904-7-F

SPI FLASH
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031

| NON-iAMT | 1MB |
|---|---|
| iAMT | 8MB |

U22
EC_CE# EC_SCK R563 47_4 EC_SCK_R EC_SI R562 47_4 EC_SI_R EC_SO R530 15_4 EC_SO_R
CE# SCK SI SO HOLD# WP# VDD VSS
+3VPCU R529 10K_4 R560 10K_4 C696 0.1U/10V_4
SPI Flash Socket

Delete it after B test
D11 *RB500V-40
DGPU_HOLD_RST# OVT_DETC
Mount for Optimus

L22 BK1608HS121-T IT8502_AGND
C466 0.1U/10V_4

NB5

PROJECT : JW2
Quanta Computer Inc.
Size Custom | Document Number Embedded Controller (ITE_IT8518) | Rev/D A
Date: Wednesday, November 02, 2011 | Sheet 29of 40

TOP DC_JACK
90W/4.75A

CN2
HS3404F

Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

Kelvin Connections for the Current-Sense Resistors

Parallel routing

New Battery Pack
3S2P (2200mAH)

CN9
BP07061-BA015

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

include charger boost function

PU5
OZ8682

Using Kevin connection for layout

Place this cap close to EC

Place this cap close to IC

Place this cap close to EC

EMI Suggestion

PROJECT : JW2
Quanta Computer Inc.
NB5
Size Custom
Document Number <Doc>
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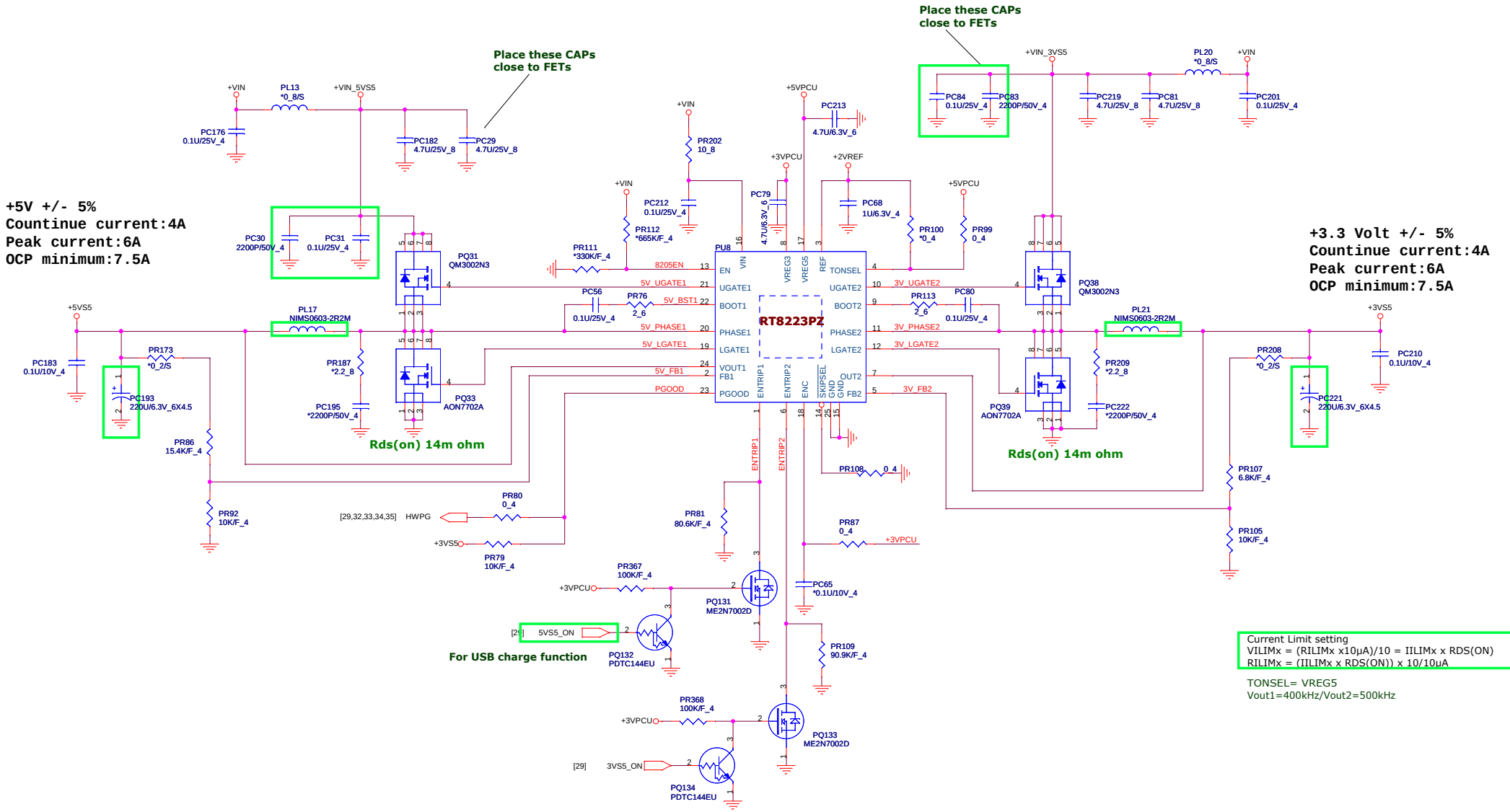
# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW






[21,30,32,34,36,37,39,40] +VIN
[6,7,8,9,10,29,34,35,37,40] +3VS5
[10,23,26,32,33,34,35,36,38,39,40] +5VS5
[7,21,26,27,28,29,30] +3VPCU

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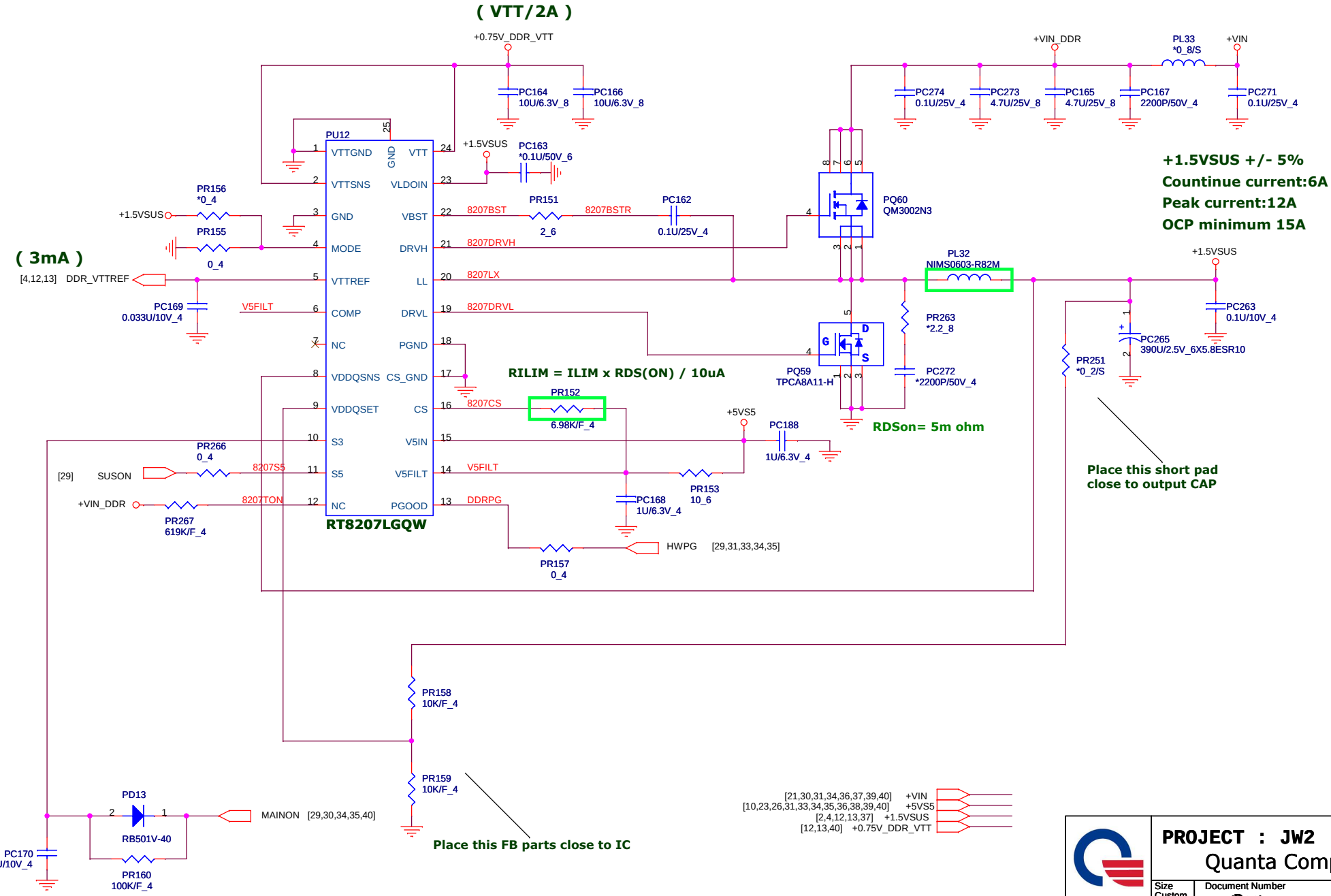


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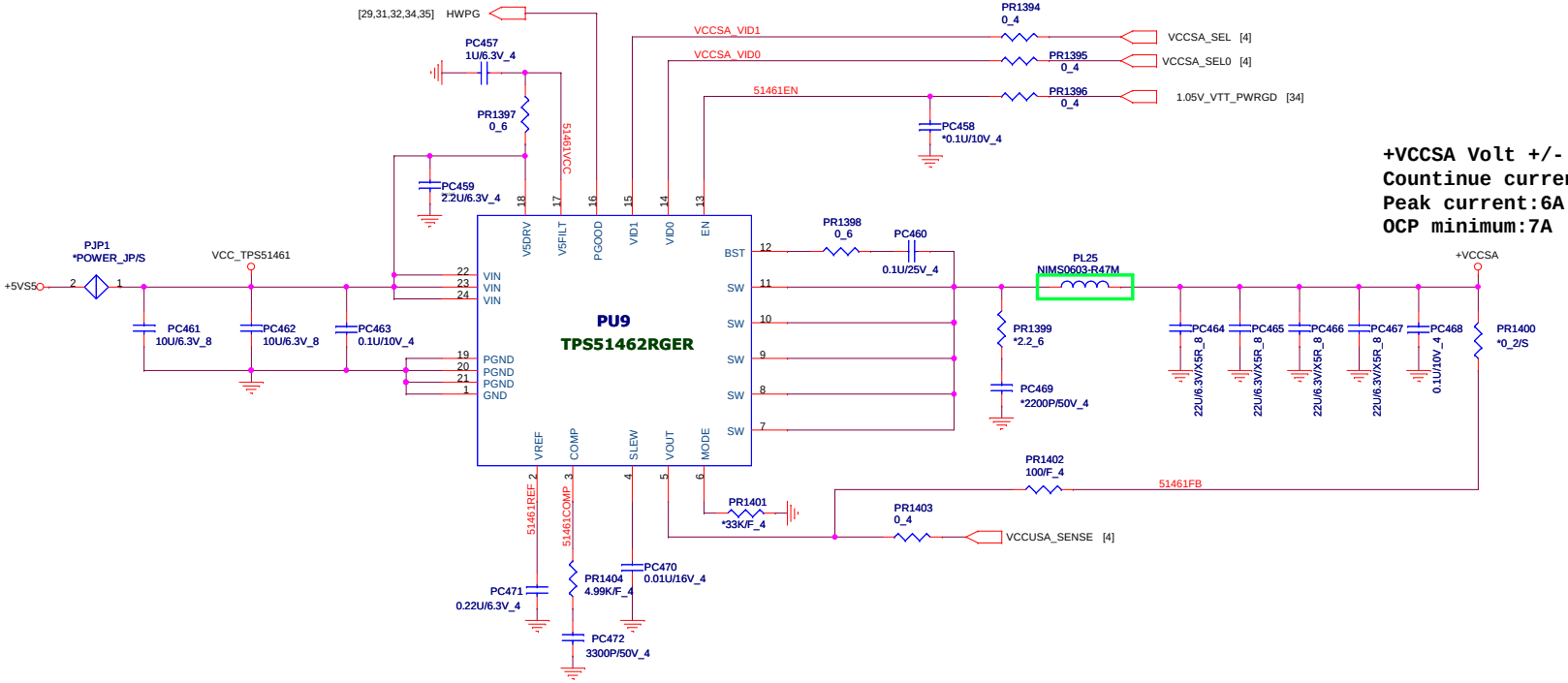
**CPU system agent**
**voltage slew rate of 0.5 -10 mV/μs**

| SEL0 | SEL1 | +VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

**+VCCSA Volt +/- 5%**
**Countinue current:4A**
**Peak current:6A**
**OCP minimum:7A**

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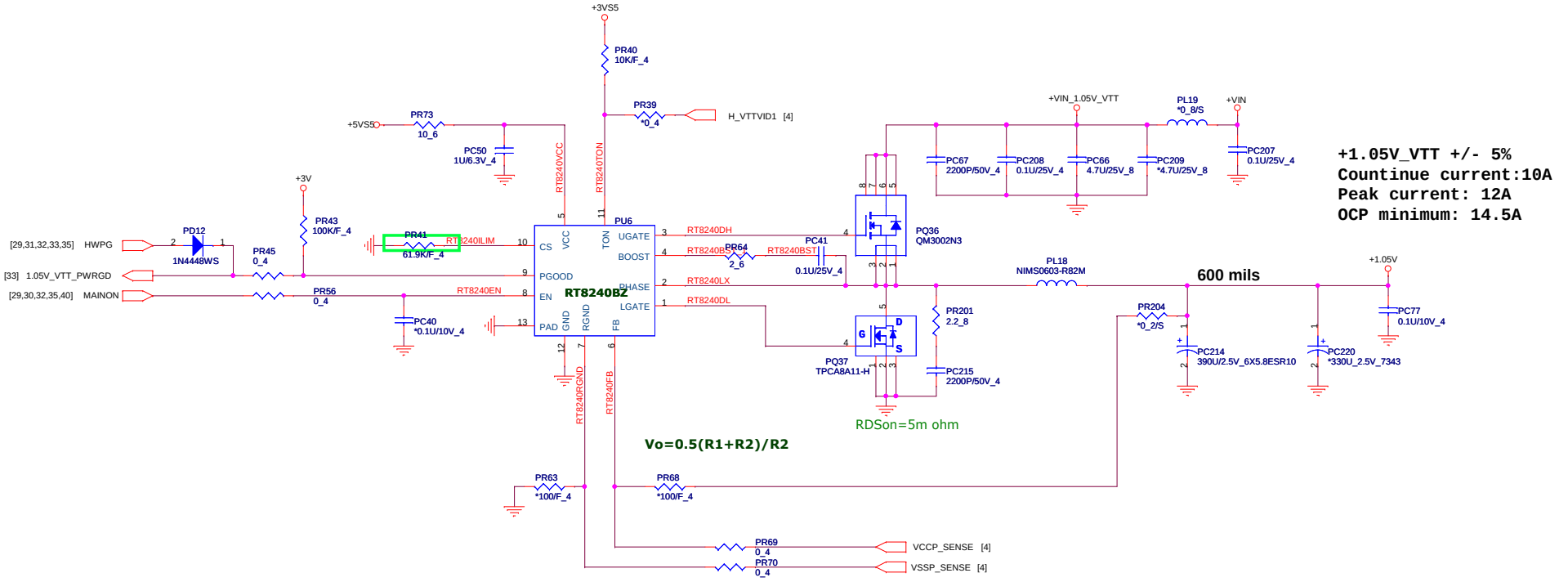


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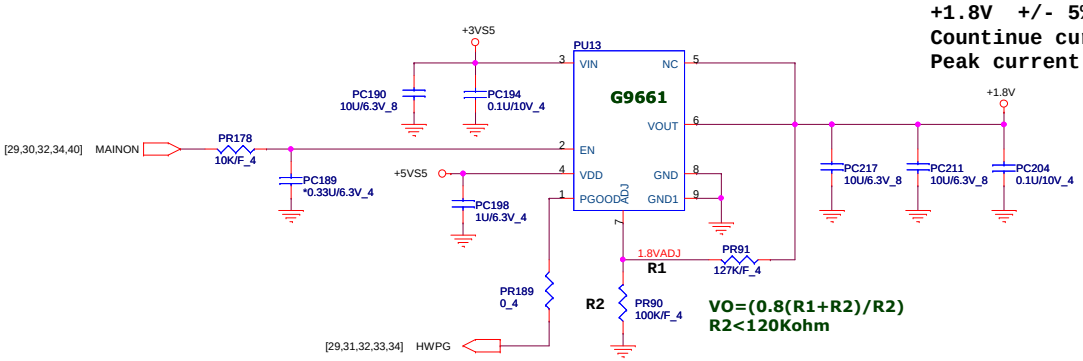


**+1.8V +/- 5%**
**Countinue current:1.2A**
**Peak current:2A**

**VO=(0.8(R1+R2)/R2)**
**R2<120Kohm**

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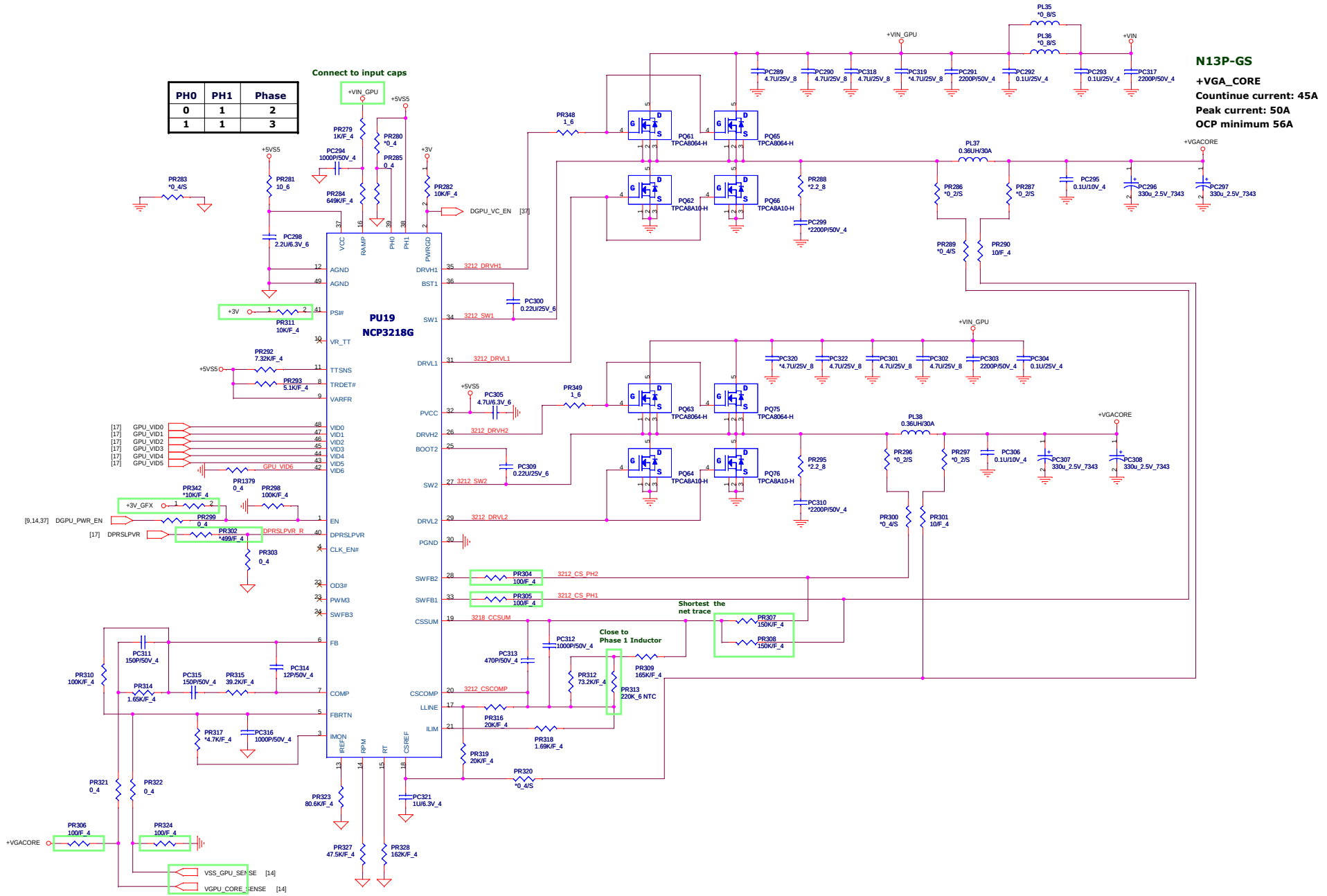
Connect to input caps
PH0 PH1 Phase
0 1 2
1 1 3
PU19
NCP3218G
N13P-GS
+VGA_CORE
Countinue current: 45A
Peak current: 50A
OCP minimum 56A
Shortest the net trace
Close to Phase 1 Inductor
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+VGA_CORE ( NCP3218G)
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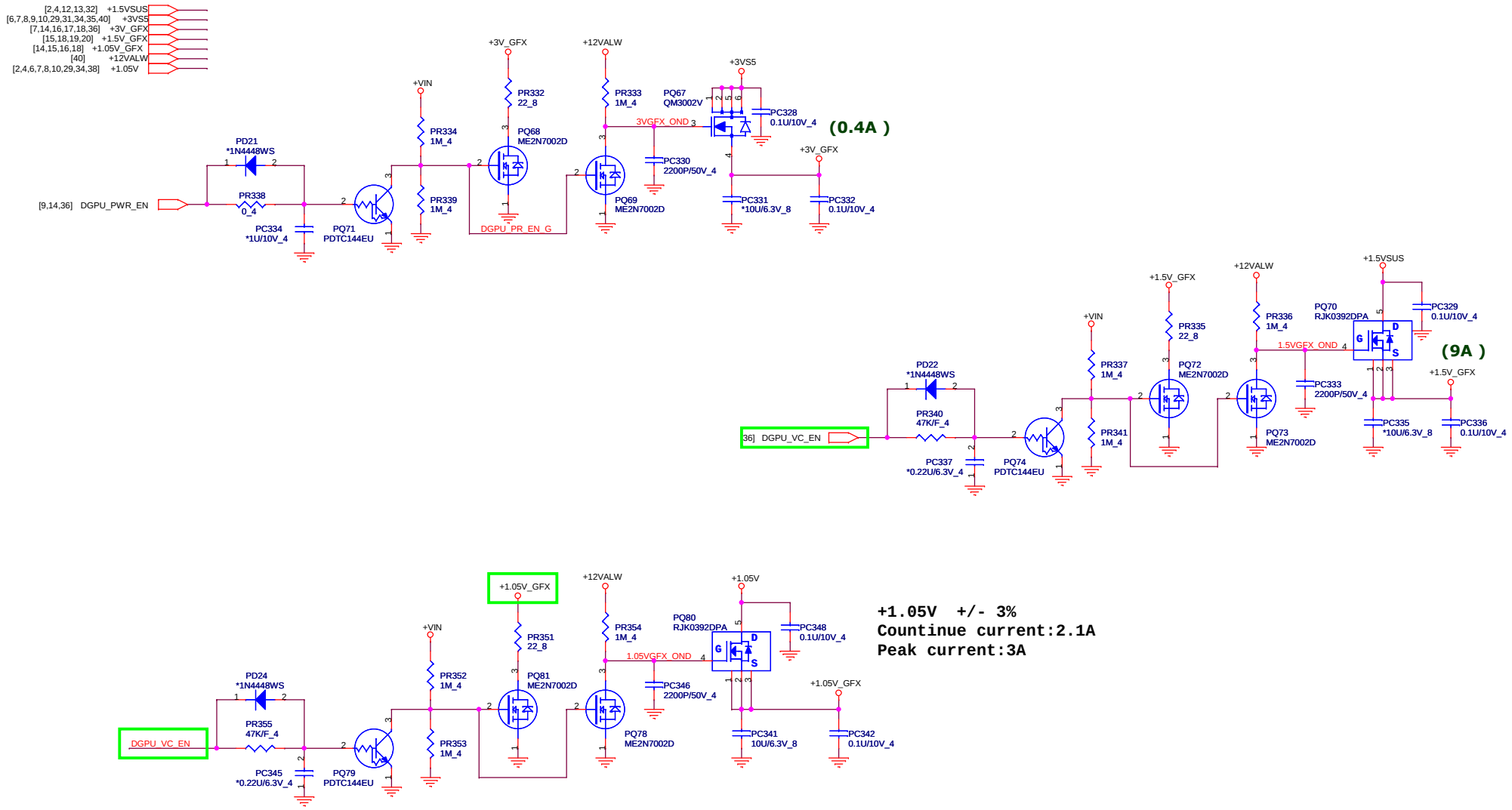
# VGA






**+1.05V +/- 3%**
**Countinue current:2.1A**
**Peak current:3A**

NB5

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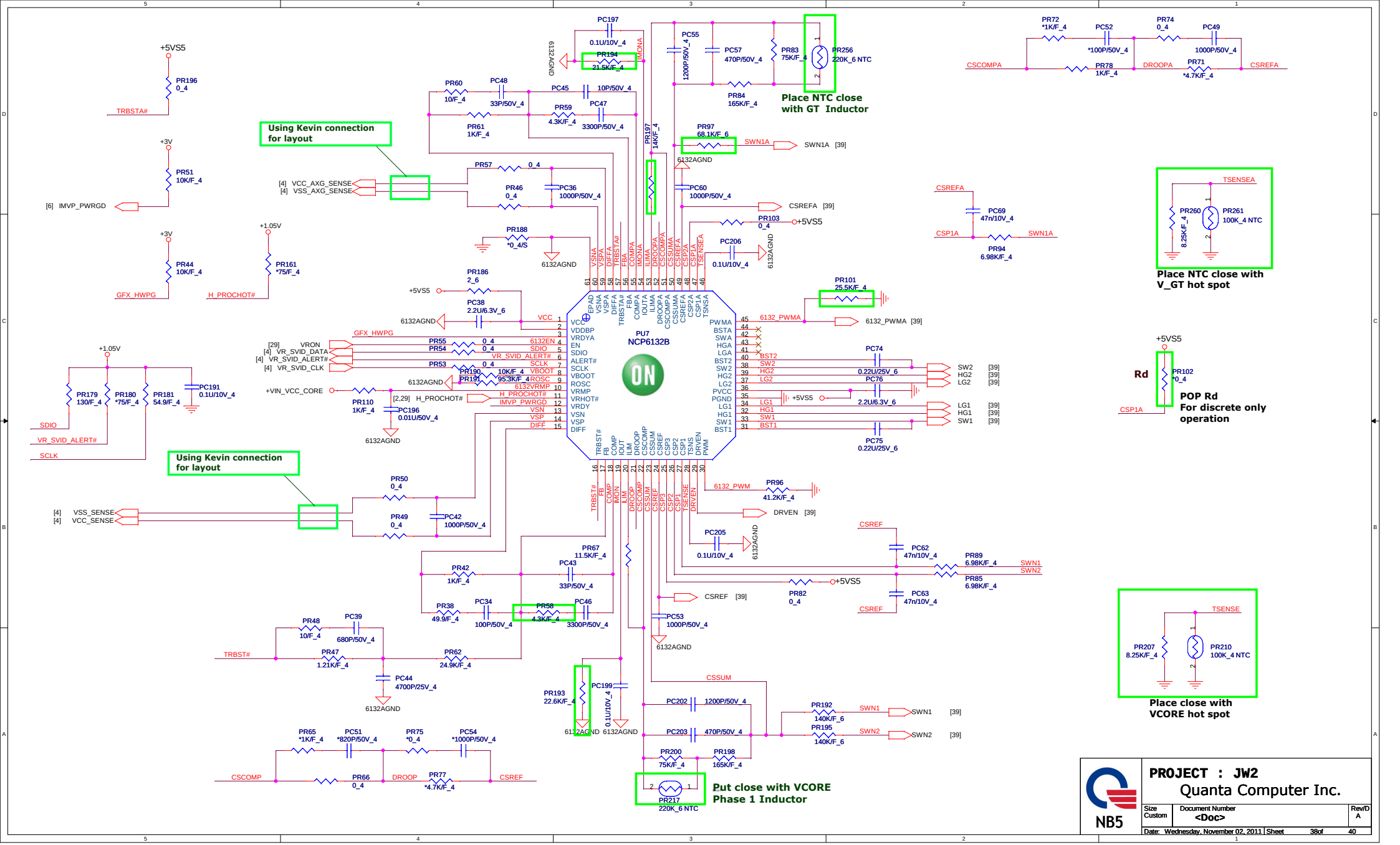
PU7
NCP6132B
Using Kevin connection for layout
Using Kevin connection for layout
Place NTC close with GT Inductor
Place NTC close with V_GT hot spot
POP Rd For discrete only operation
Place close with VCORE hot spot
Put close with VCORE Phase 1 Inductor
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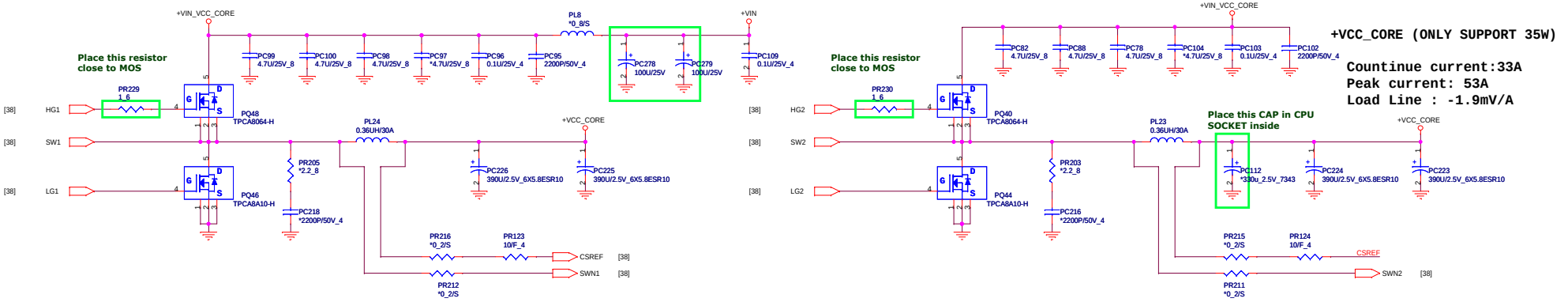
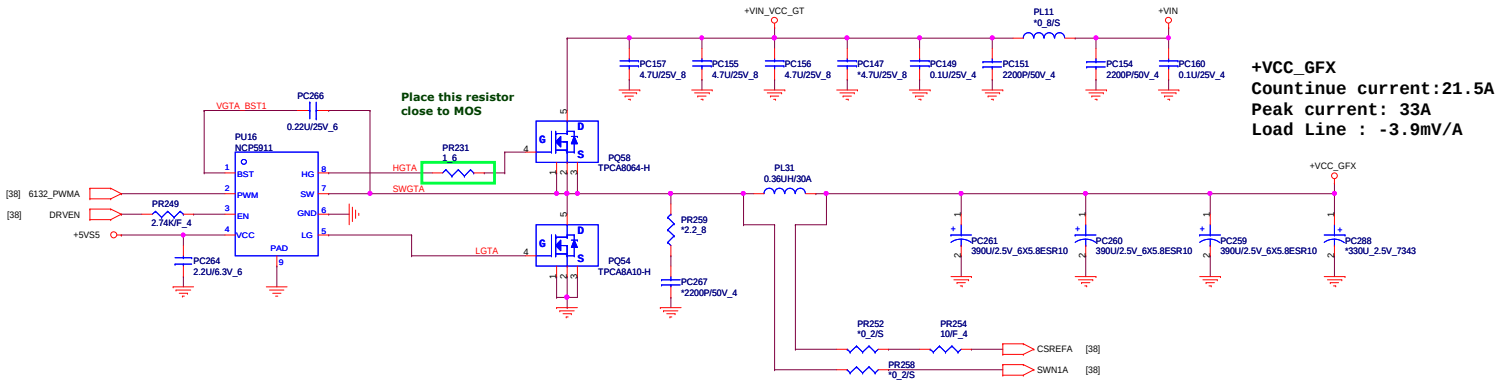



**+VCC_CORE (ONLY SUPPORT 35W)**

**Countinue current:33A**
**Peak current: 53A**
**Load Line : -1.9mV/A**




**+VCC_GFX**
**Countinue current:21.5A**
**Peak current: 33A**
**Load Line : -3.9mV/A**

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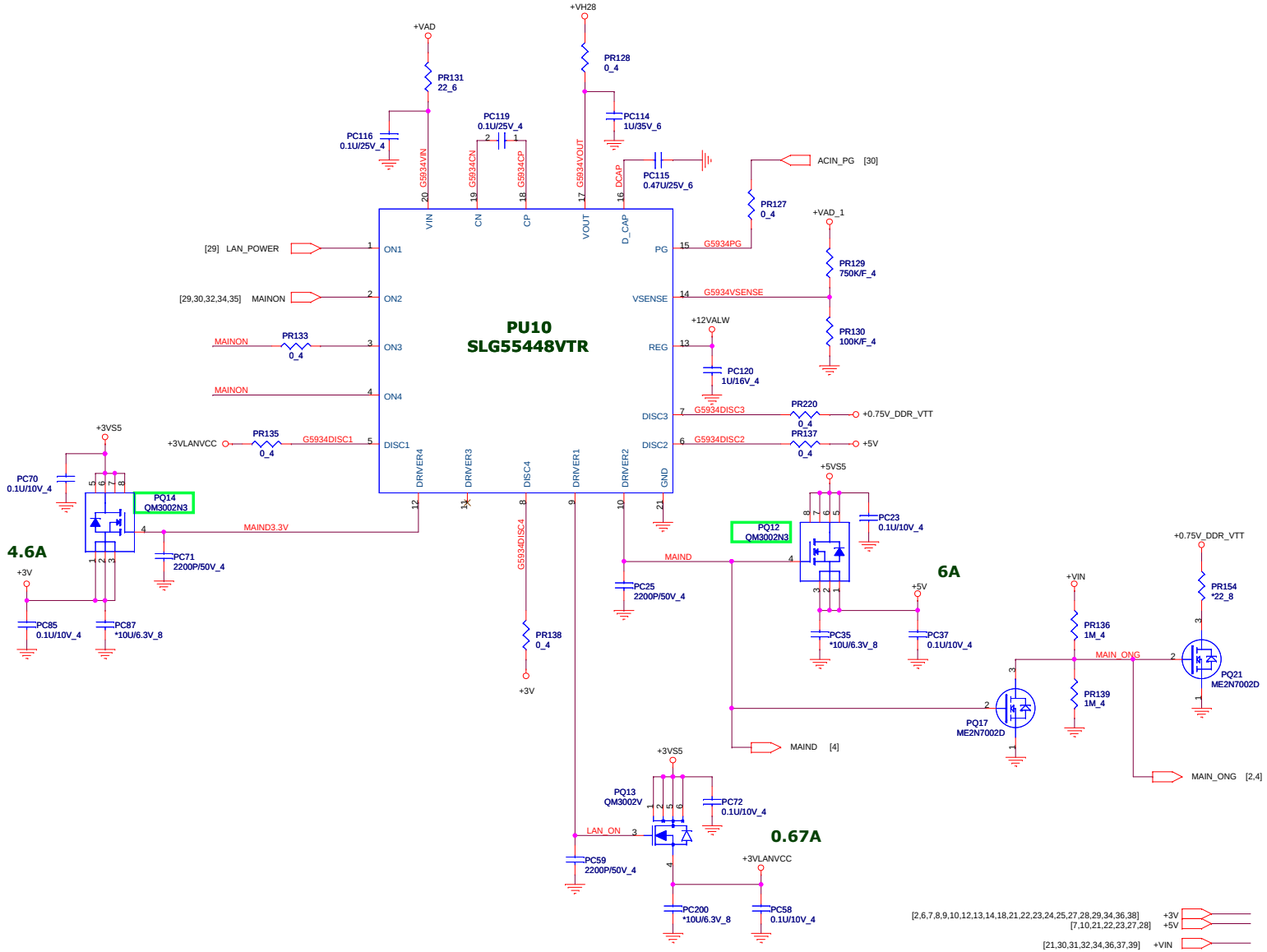


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