Compal Confidential

C5MMH MB Schematic Document

LA-E911P

Rev:1A

2017.04.11

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.		
Title: Cover Sheet		
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eDP

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eDP

Nvidia N17P-GX with gDDR5 x4
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Processor page 06~13

Memory BUS
Dual Channel
1.2V DDR4 1333/1600

Interleaved Memory

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260pin DDR4-SO-DIMM X1
BANK 4, 5, 6, 7 page 15

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Flexible IO

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5GT/s
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USB 3.0 Type-C x2
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on Sub/B
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Realtek 8411H

Card Reader

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Compal Electronics, Inc.

Title: Block Diagrams

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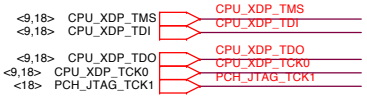
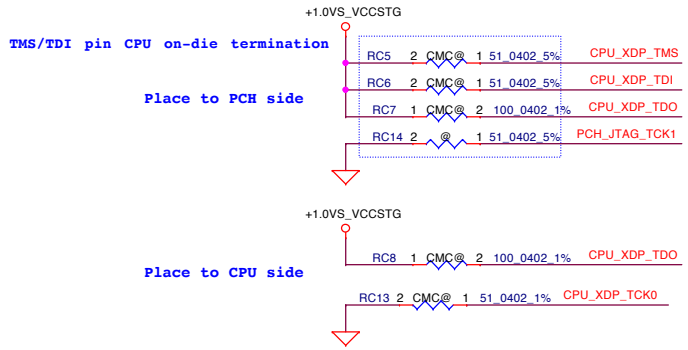


If need debug from usb port. this cmc@ need pop



1.0 Modify

UC1 SR32S@
S IC CL8067702870309 SR32S B0 2.5G ABO!
SA0000AD850

UC1 SR32Q@
S IC CL8067702870109 SR32Q B0 2.8G ABO!
SA0000AD750

UH1 SR30W@
S IC GL82HM175 SR30W D1 FCBGA PCH-H ABO!
SA0000ADB30

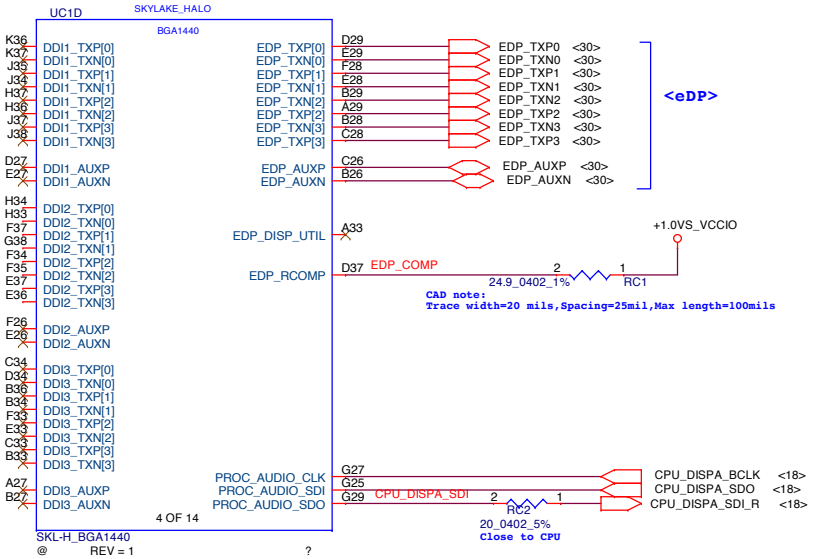
UV1 G0@
S IC N17P-G0-A1 FCBGA 908P GPU 1706
SA0000A0540

UV1 G1@
S IC N17P-G1-A1 FCBGA 908P GPU 1707
SA0000A0660

1.A Modify

ZZZ DAZ@
PCB C5MMH LA-E911P LS-E911P/E912P
DAZ20Z00102

1A Modify



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Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: SKL-H(1/9)DDI,EDP

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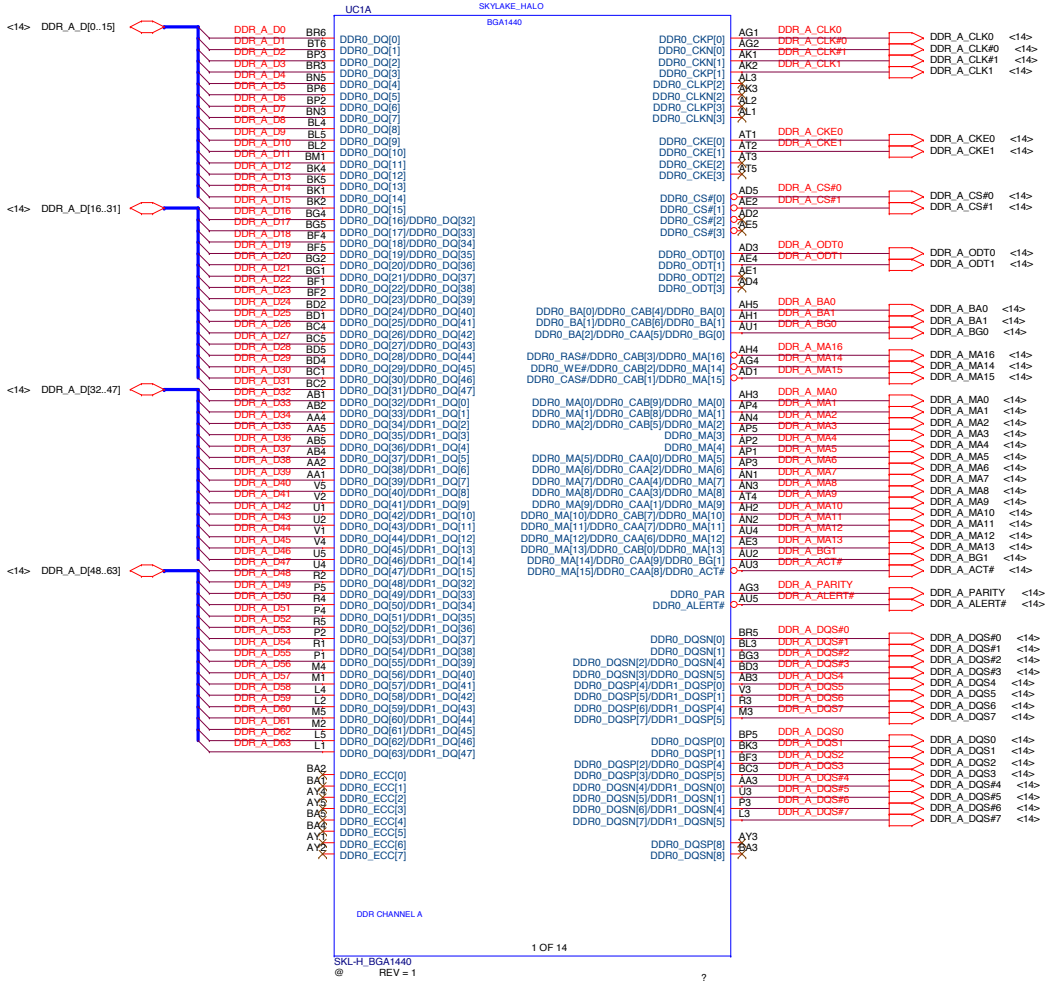
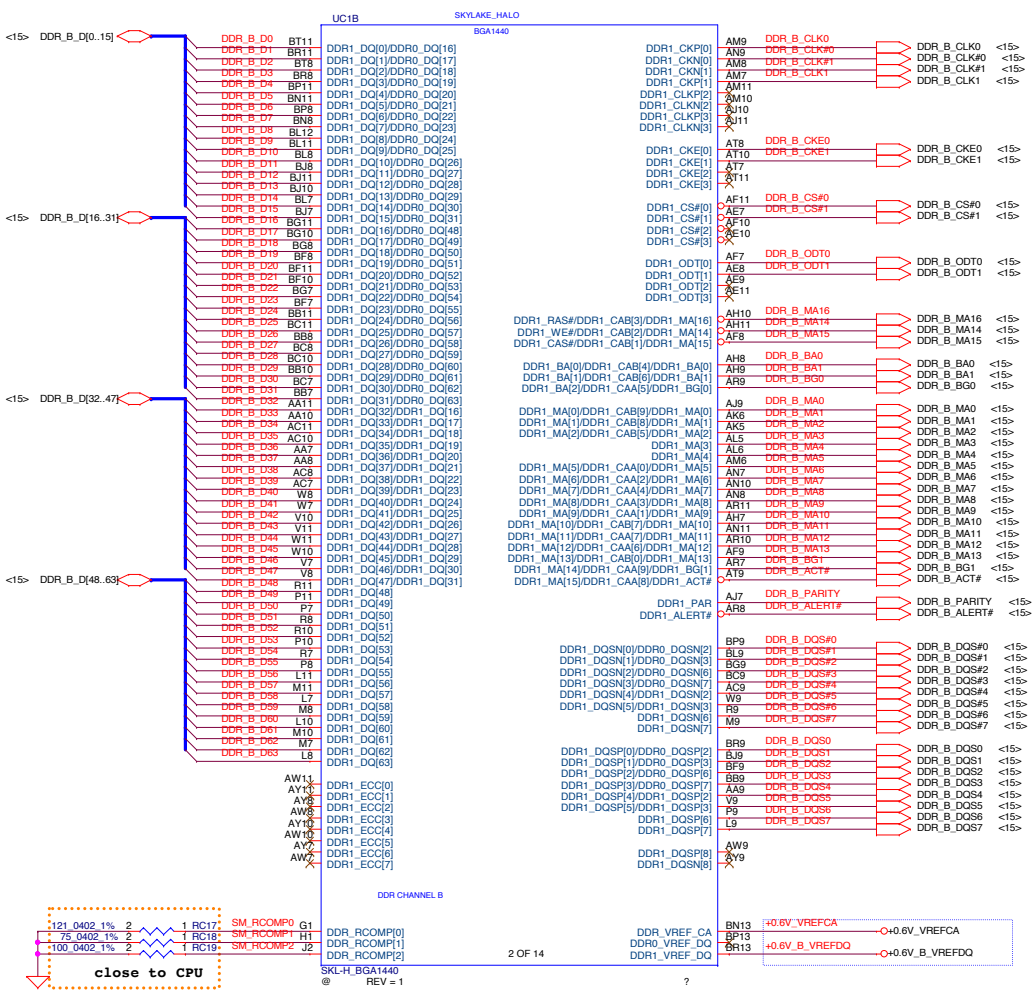
Interleaved Memory





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: SKL-H(2/9)DDRIII

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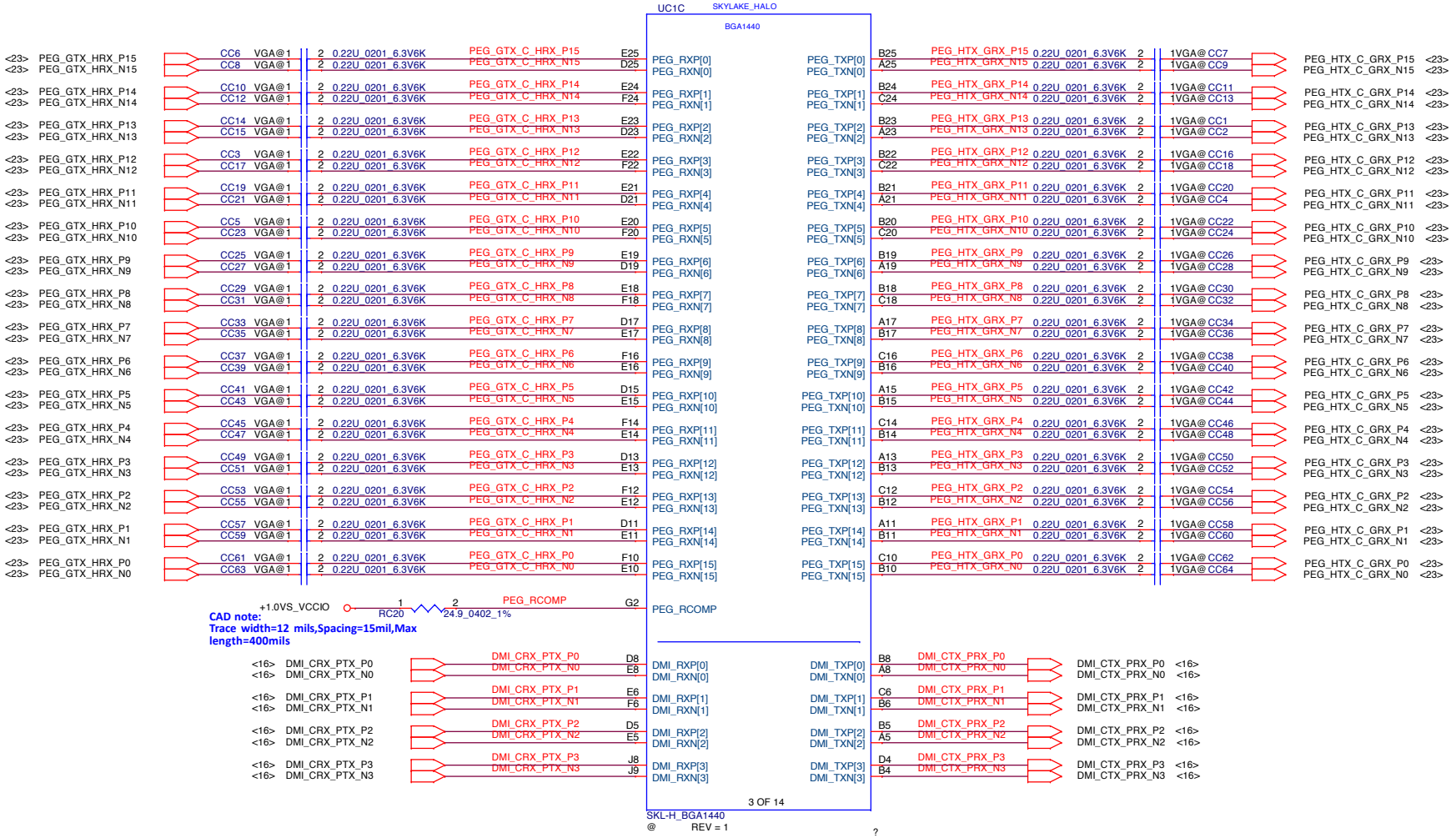

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: SKL-H(3/9) PEG,DMI

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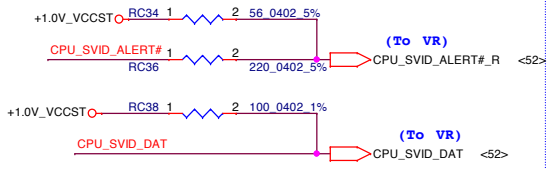
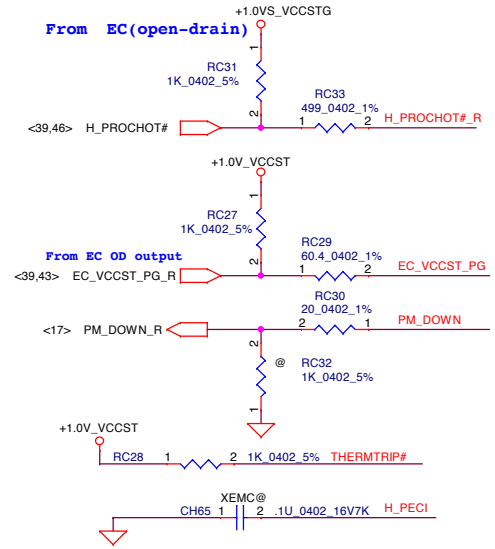
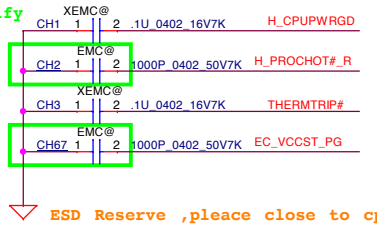
SVID Alert / Data

Place the PU resistors close to CPU

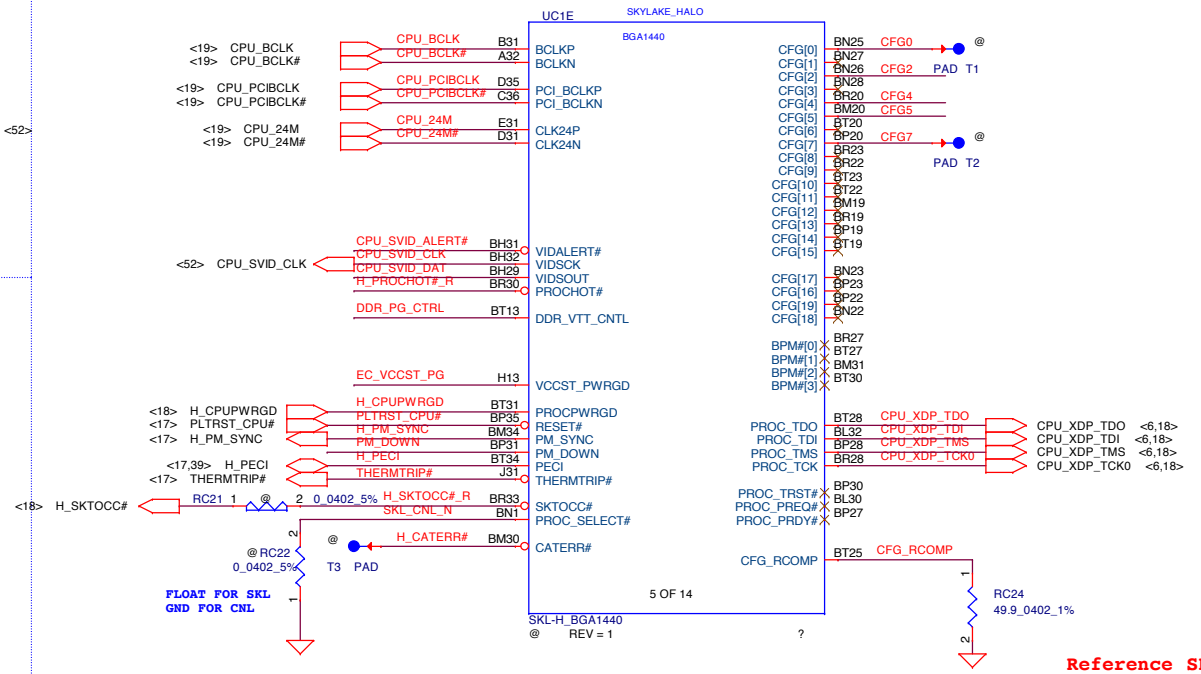


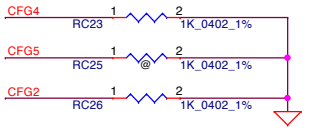


1.0 Modify

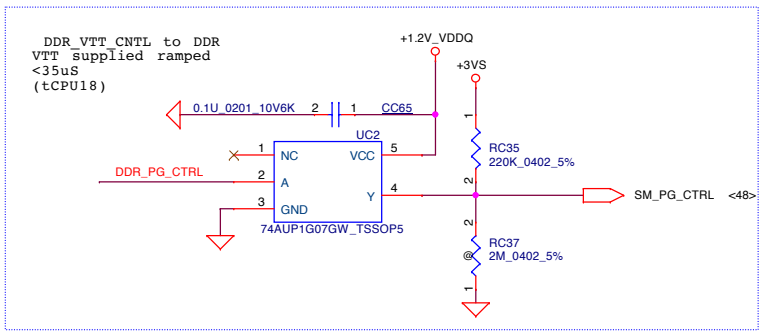


ESD Reserve ,pleace close to cpu





PCIE port assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 * reverse	1	1	0
2 x 8	1	0	1
2 x 8 reverse	1	0	0
1 x 8 + 2 x 4	0	0	1
1x8+2x4 reverse	0	0	0



Reference SKL EDS 0.85 Table 6-8
CFG signals internal PH default value = 1

		Description
CFG[0]	*	Stall reset sequence after PCU PLL lock until de-asserted – 1 = (Default) Normal Operation; No stall. – 0 = Stall.
CFG[4]	*	Enable eDP – 1 = Disabled. – 0 = Enabled.
CFG[7]	*	PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]		Reserved configuration lane.

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Title: SKL-H(4/9)CLK,GPIO

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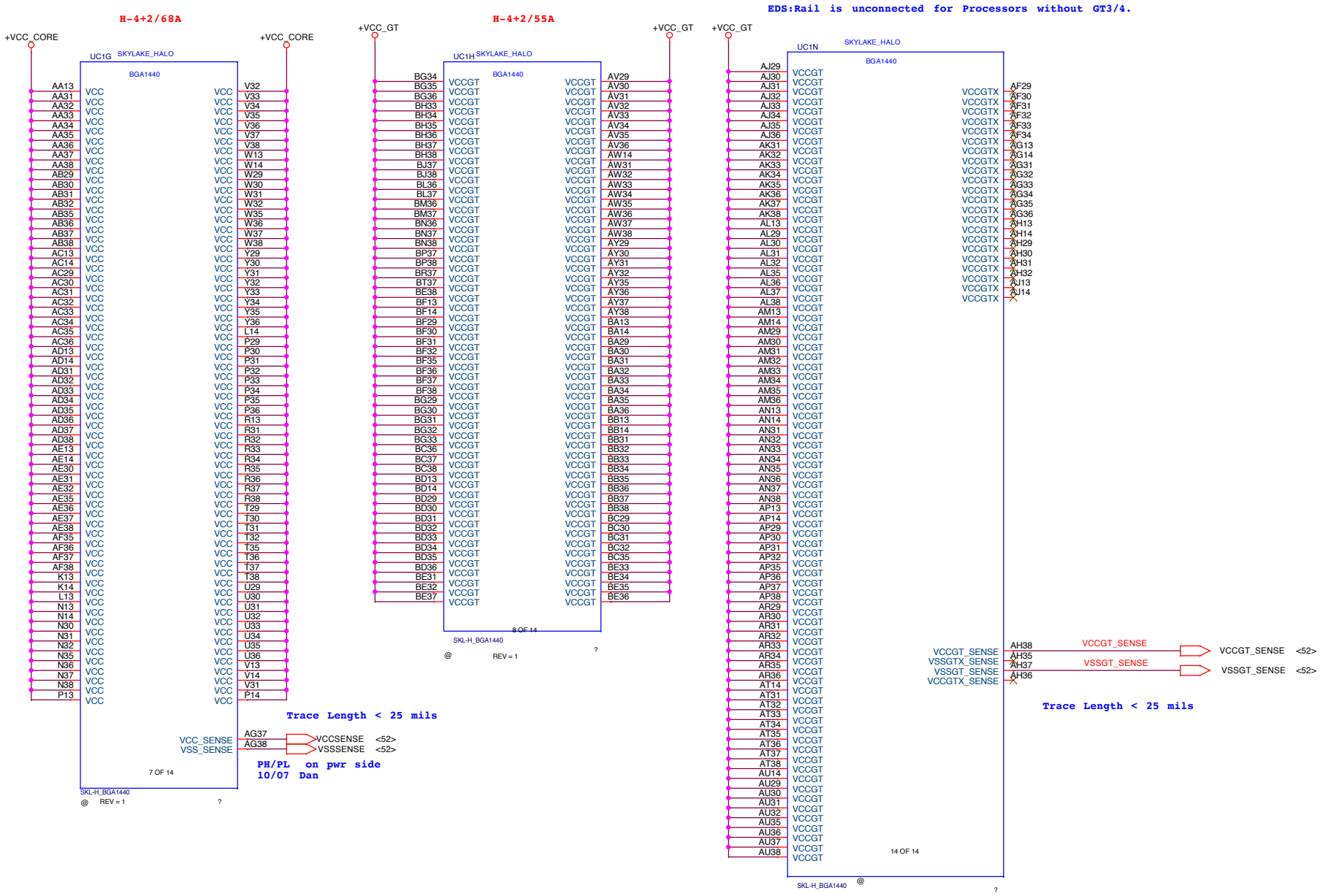

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Compal Electronics, Inc.

Title: SKL-H(5/9)Power,SVID

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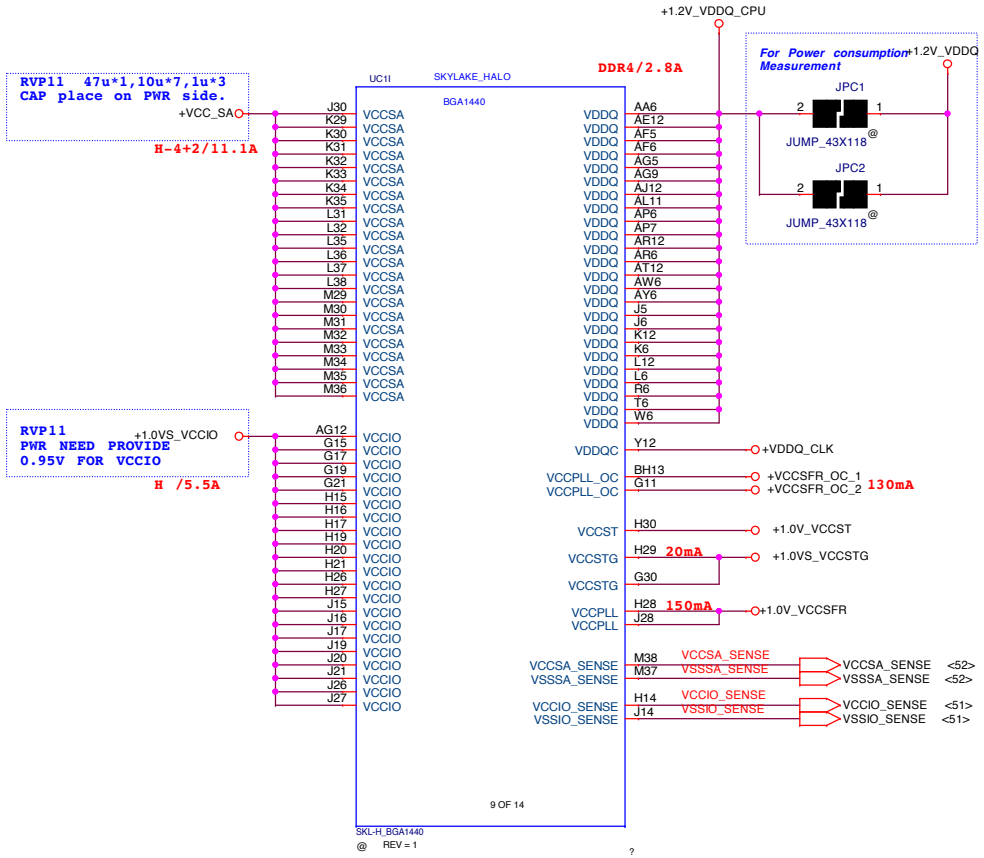

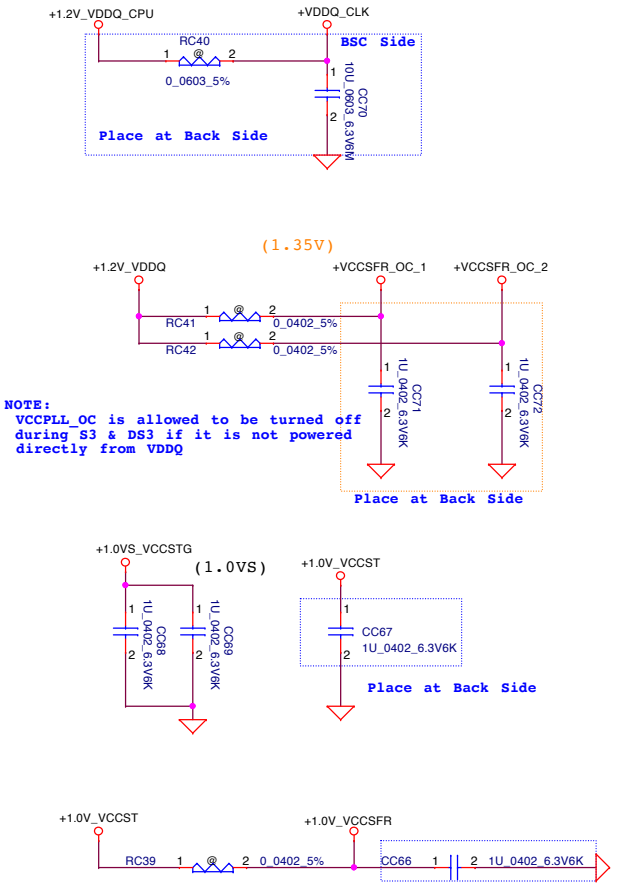

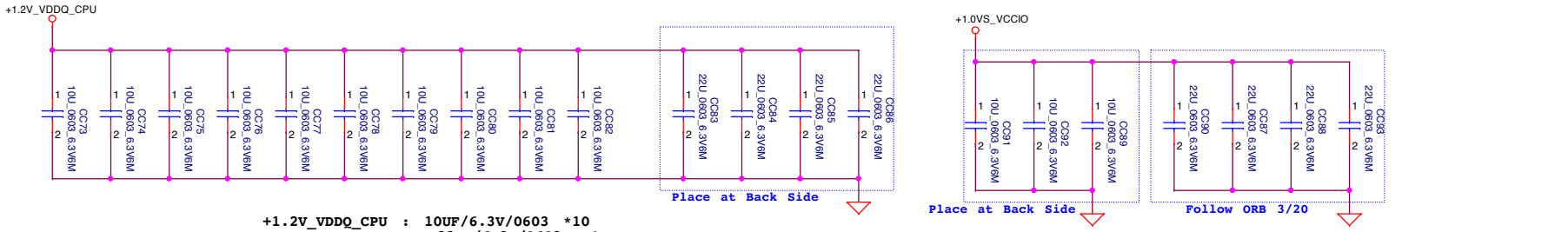

+1.2V_VDDQ_CPU : 10UF/6.3V/0603 *10
22UF/6.3V/0603 * 4
update CRB cap QTY

CPU_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: SKL-H(6/9)POWER			
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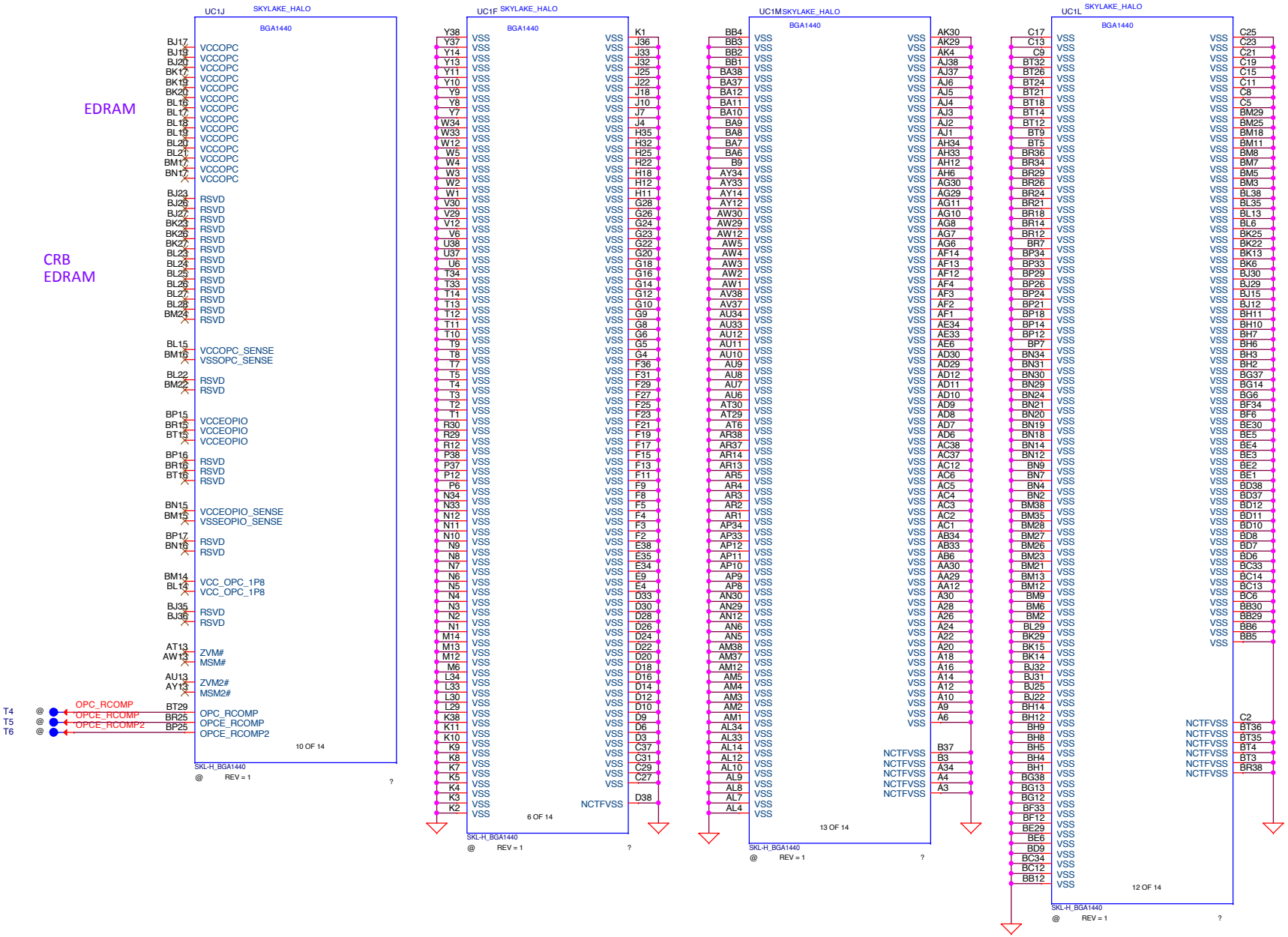

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SKL-H(8/9)GND

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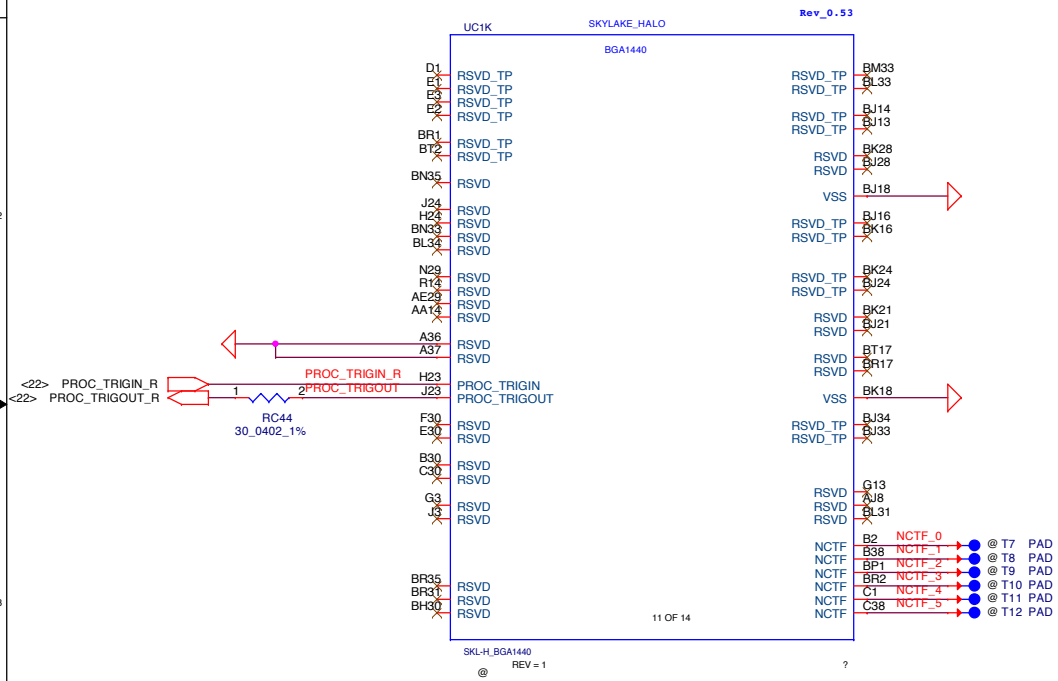
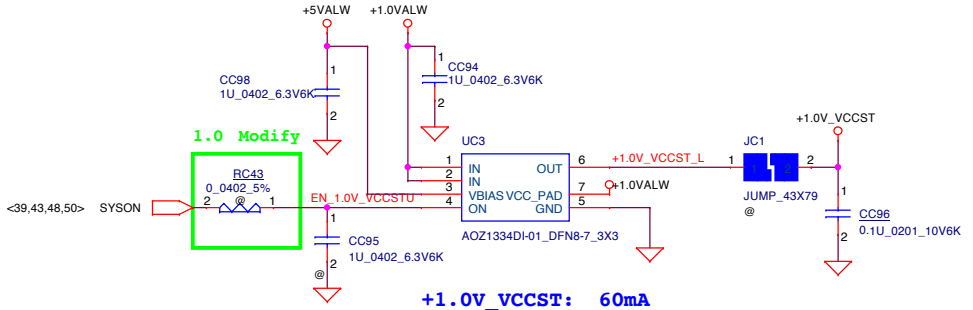


+1.0VALW TO +1.0V_VCCST

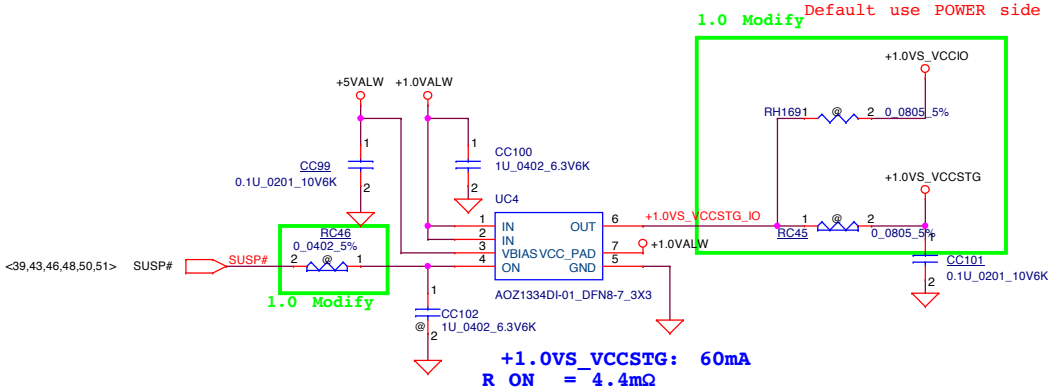


+1.0V_VCCST: 60mA
R ON = 4.5mΩ
VDROP= 1.32mV
Delay time: 270us

+1.0VALW TO +1.0VS_VCCSTG

VCCSTG and VCCIO SLEW RATE <=65us

UNPOP
Default use POWER side



+1.0VS_VCCSTG: 60mA
R ON = 4.4mΩ
VDROP= 11mV
Delay time: 9.3us

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: **SKL-H(9/9)RSVD**

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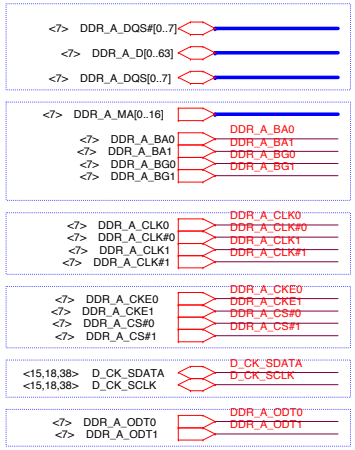
Reverse Type-4H

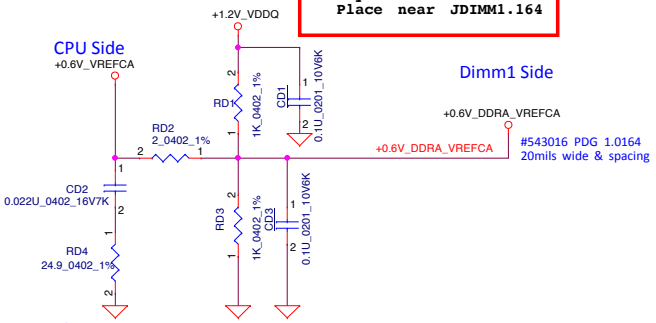
2-3A to 1 DIMMs/channel



Layout Note:
Place near JDIMM1.164

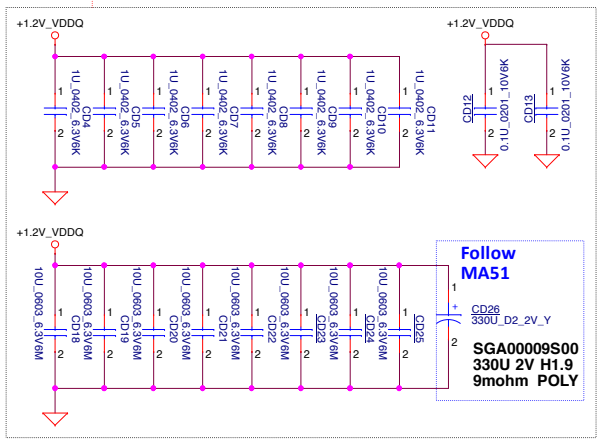
CPU Side

Dimm1 Side

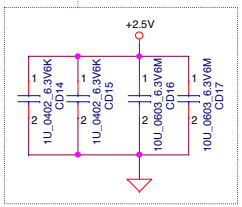


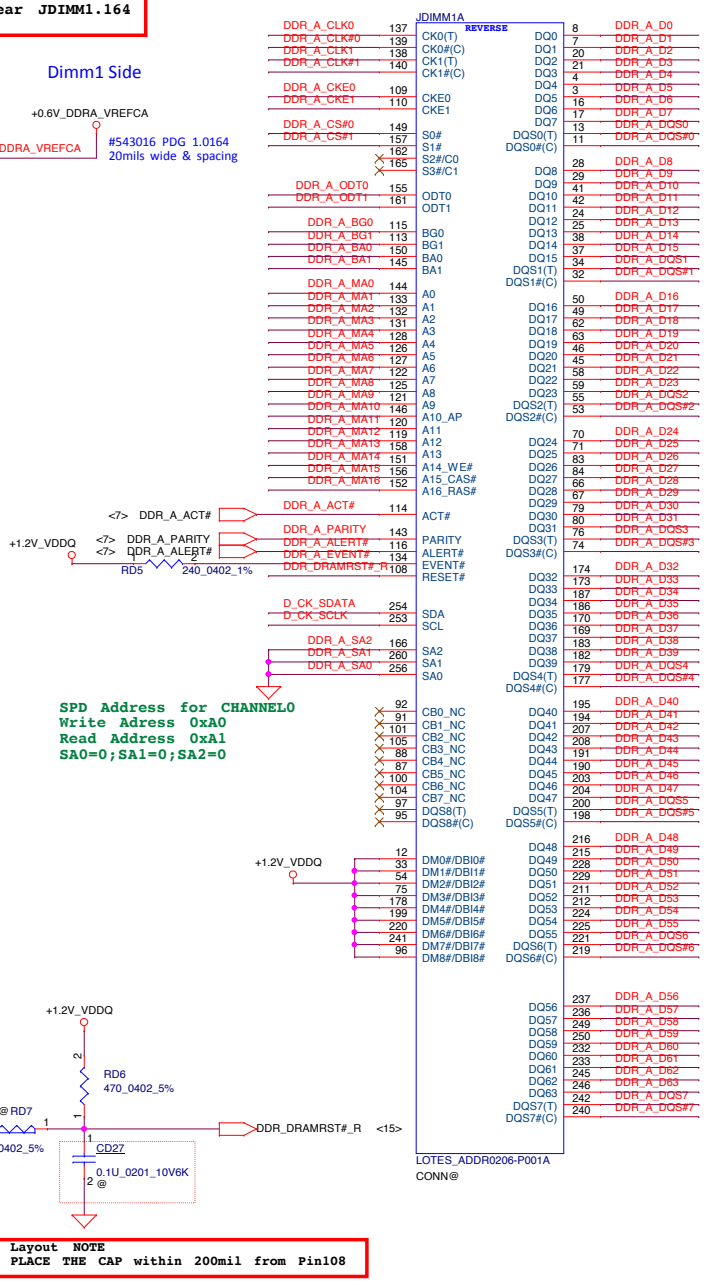
Layout Note:
Place near JDIMM1

Note:
place caps close to DIMM
4 on each side of DIMM

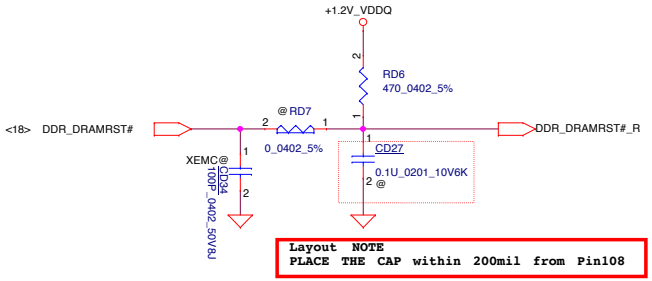


Layout Note:
Place near JDIMM1.257/259





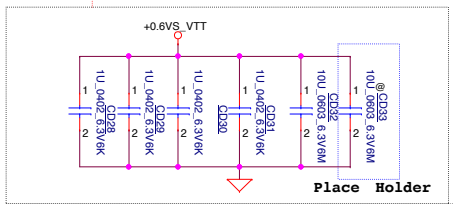
SPD Address for CHANNEL0
Write Adress 0xA0
Read Address 0xA1
SA0=0;SA1=0;SA2=0

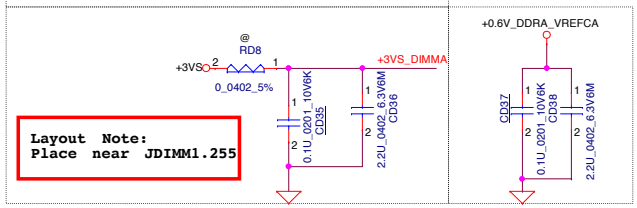


Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

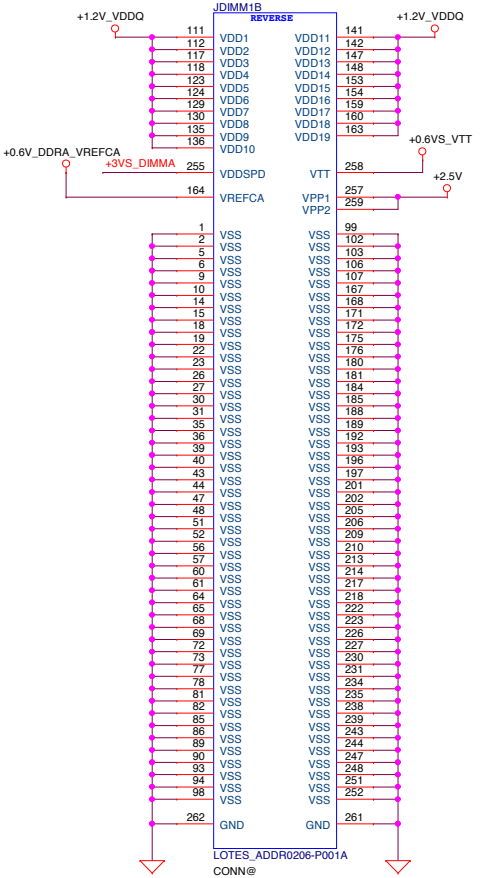
Layout Note:
Place near JDIMM1.258





Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164
within 200mils



Interleaved Memory

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: DDR4 DIMMA

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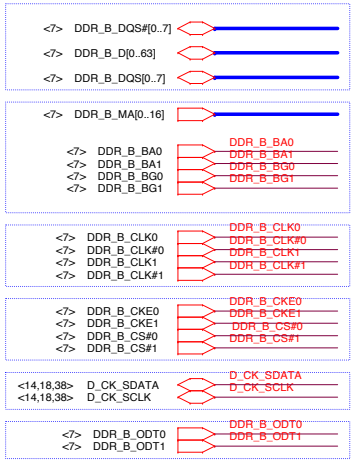
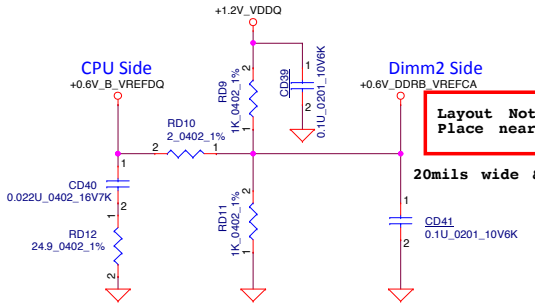
Reverse Type-8H

2-3A to 1 DIMMs/channel





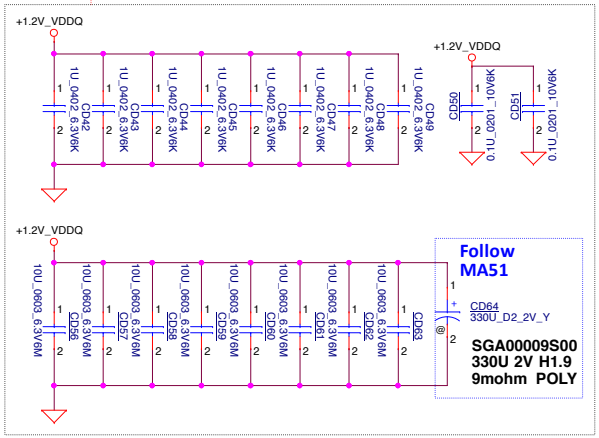
Layout Note:
Place near JDIMM2.164

20mils wide & spacing

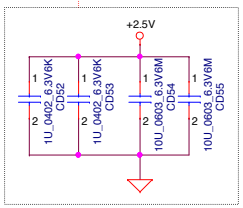
Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM2

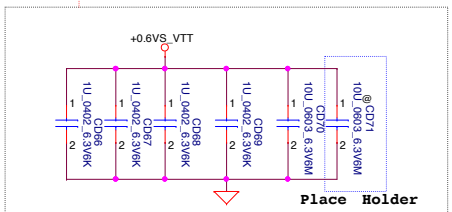
Note:
place caps close to DIMM
4 on each side of DIMM

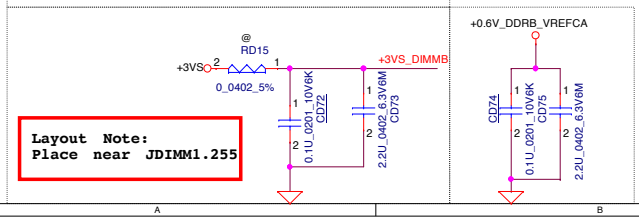


Layout Note:
Place near JDIMM2.257/259



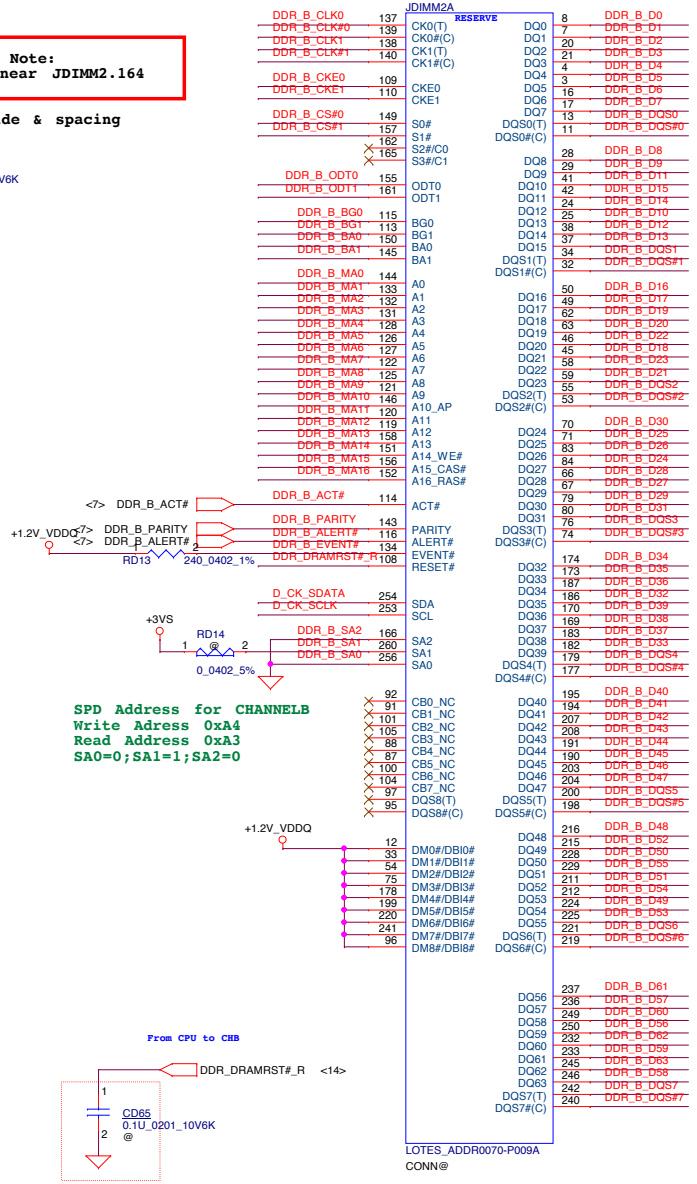
Layout Note:
Place near JDIMM2.258

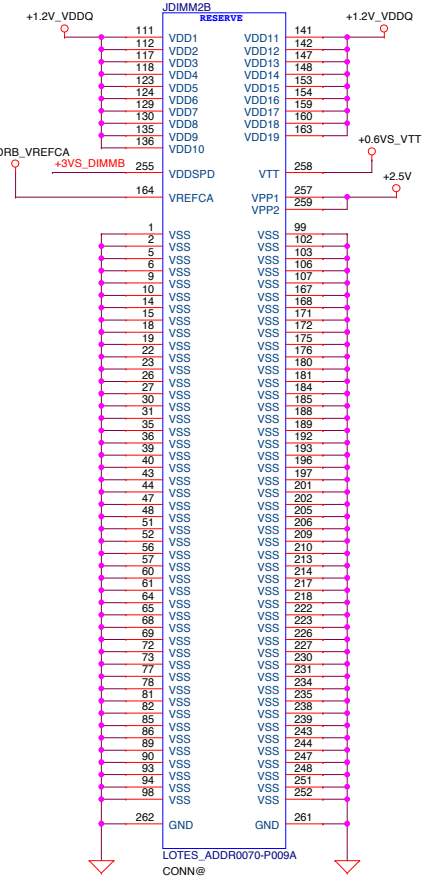




Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1.164
within 200mils





SPD Address for CHANNELB
Write Adress 0xA4
Read Address 0xA3
SA0=0;SA1=1;SA2=0

Layout NOTE
PLACE THE CAP within 200mil from Pin108

*2015MOW02, Can't install Cap on DRAMRST

Interleaved Memory

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Compal Electronics, Inc.

Title: DDR4 DIMMB

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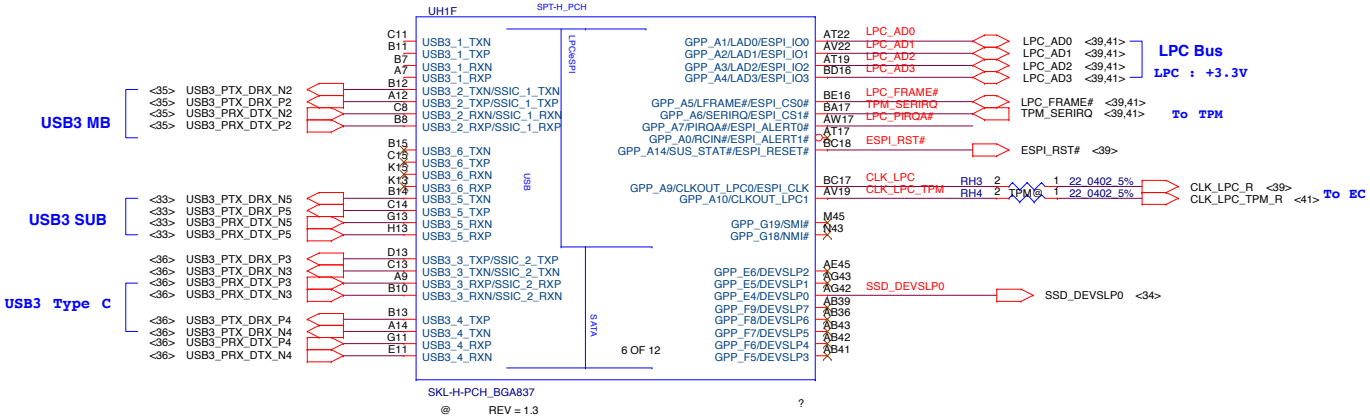

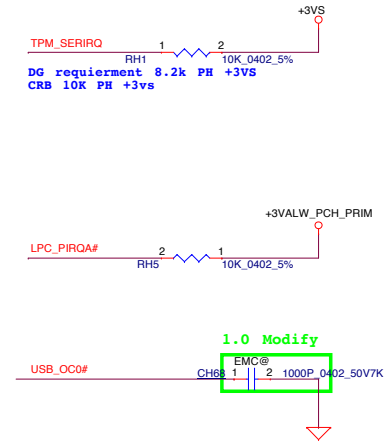

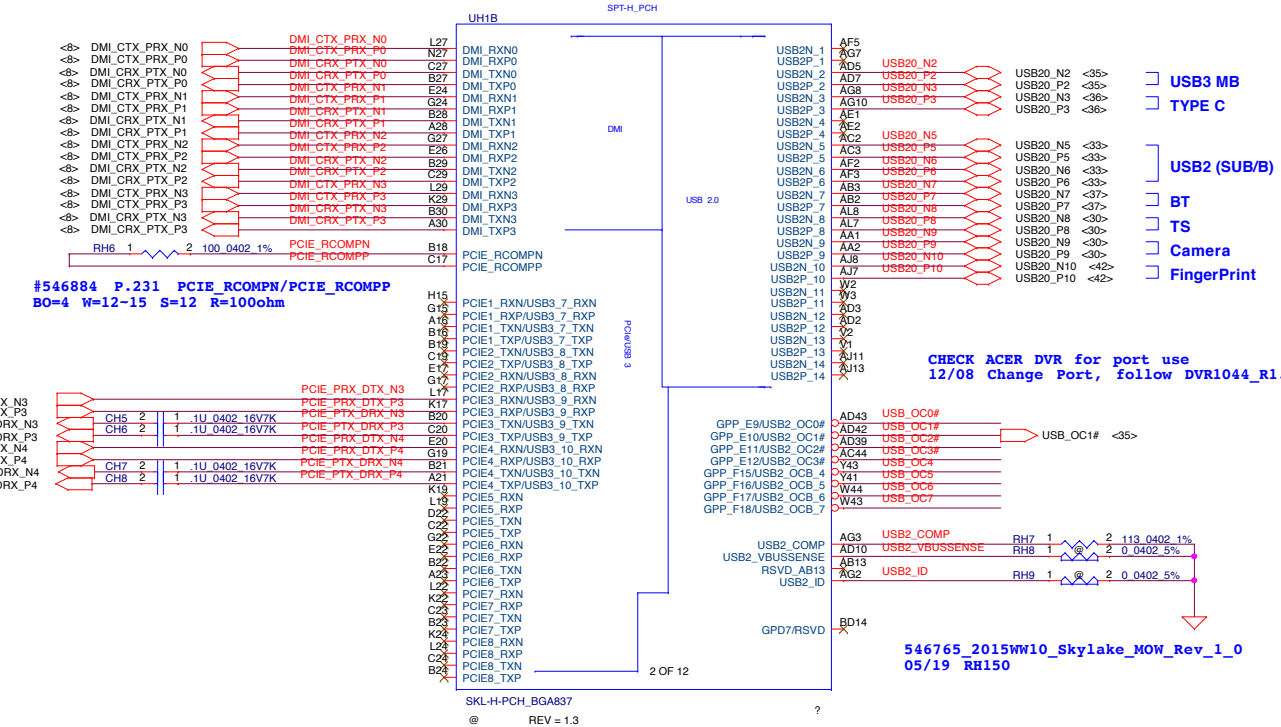

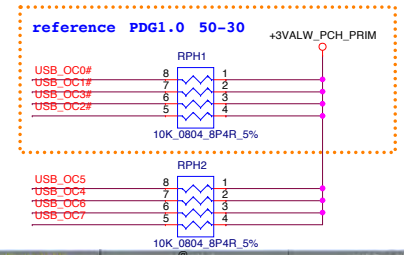

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(1/7)DMI,PCIE,USB

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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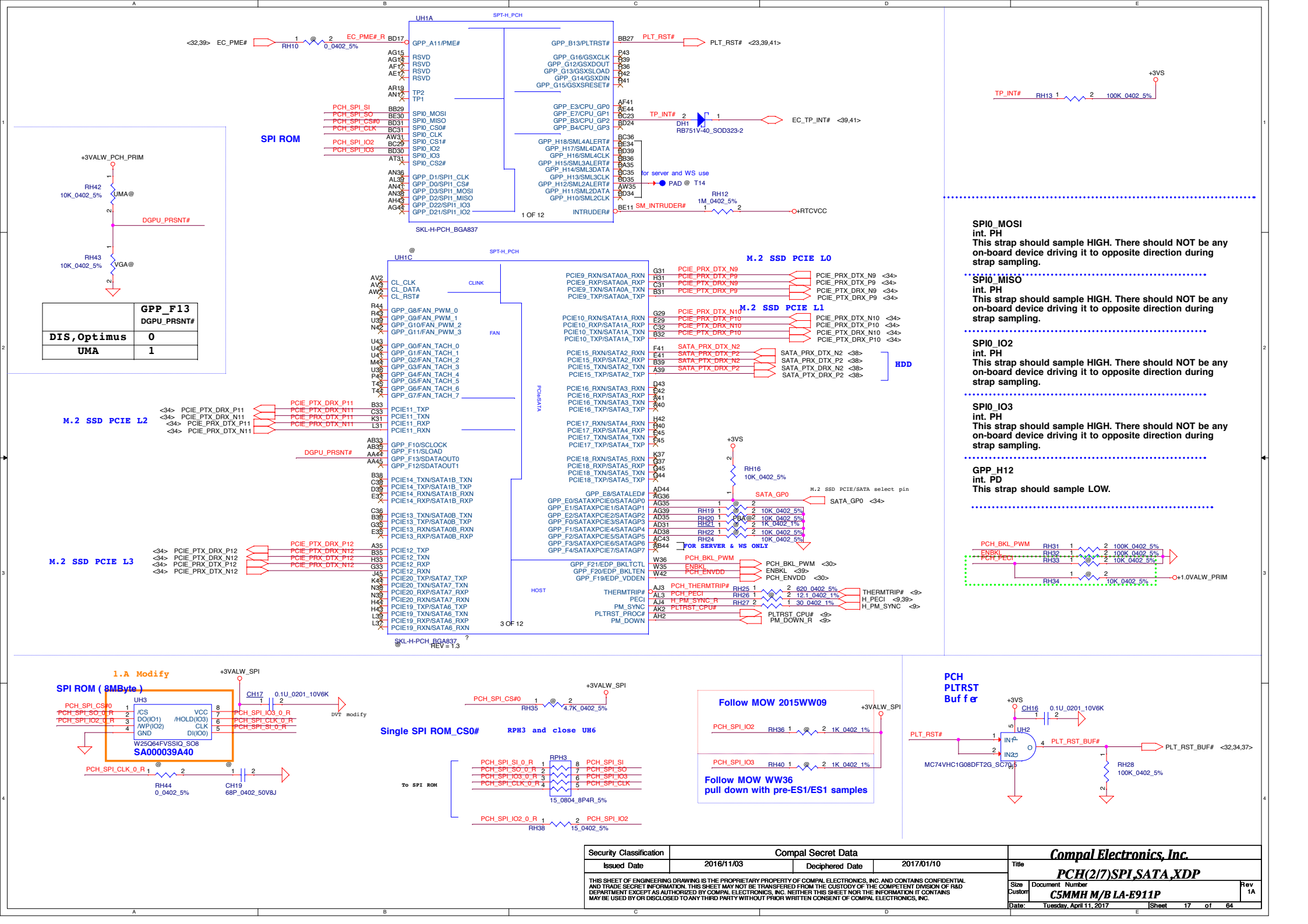

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(2/7)SPI,SATA,XDP

Size	Document Number	Rev
Custom	C5MMH M/B LA-E911P	1A

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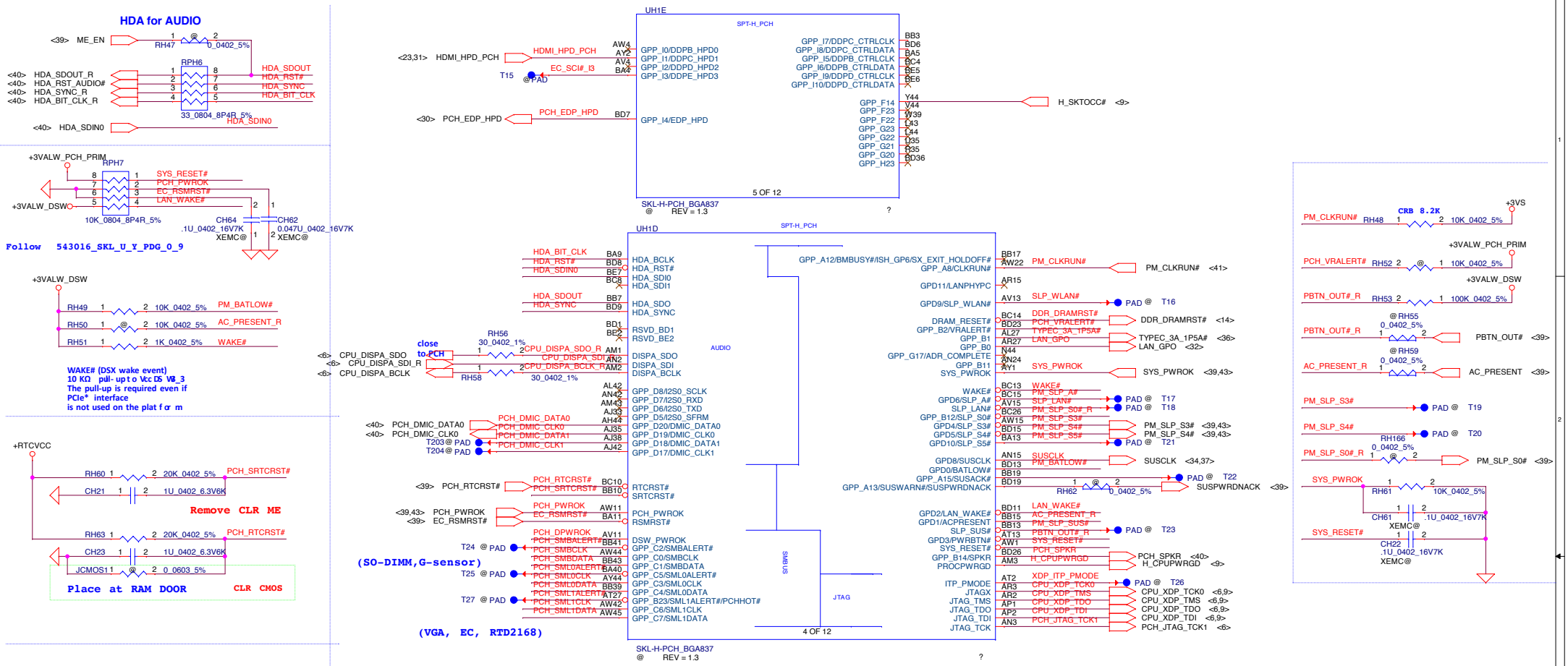

Functional Strap Definitions

SMBALERT# / GPP_C2
int. PD
0 = Disable Intel ME (TLS) (Default)
1 = Enable Intel ME (TLS)

SML0ALERT# / GPP_C5
int. PD
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT# / GPP_B23
int. PD

SPKR / GPP_B14
int. PD
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode.

HDA_SDO
int. PD
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).

DDPB_CTRLDATA / GPP_I6
int. PD
0 = Port B is not detected.
1 = Port B is detected. (Default)

DDPC_CTRLDATA / GPP_I8
int. PD
0 = Port C is not detected.
1 = Port C is detected. (Default)

DDPD_CTRLDATA / GPP_I10
int. PD
0 = Port D is not detected. (Default)
1 = Port D is detected.

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(3/7)GPIO,SMBUS

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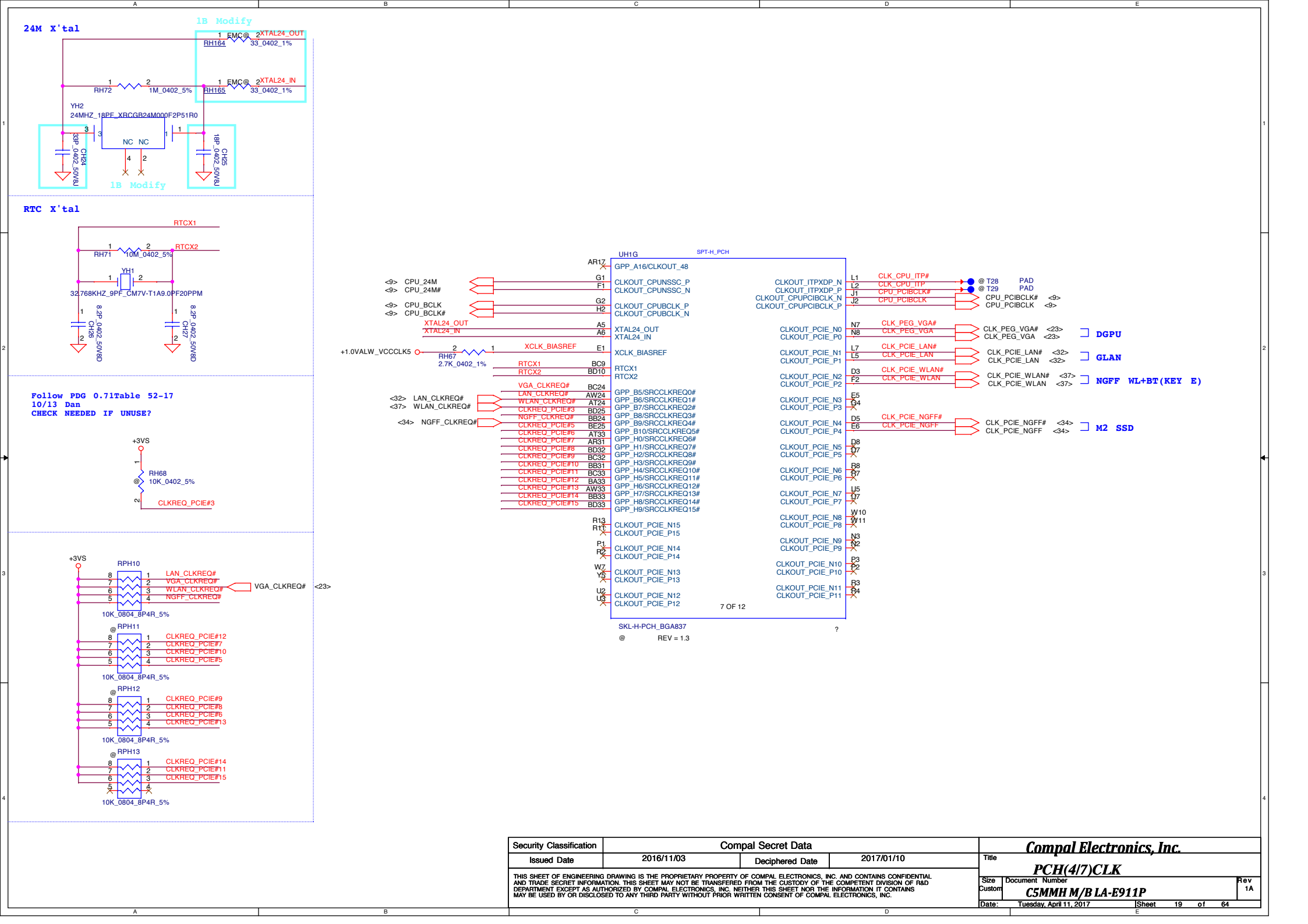

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(4/7)CLK

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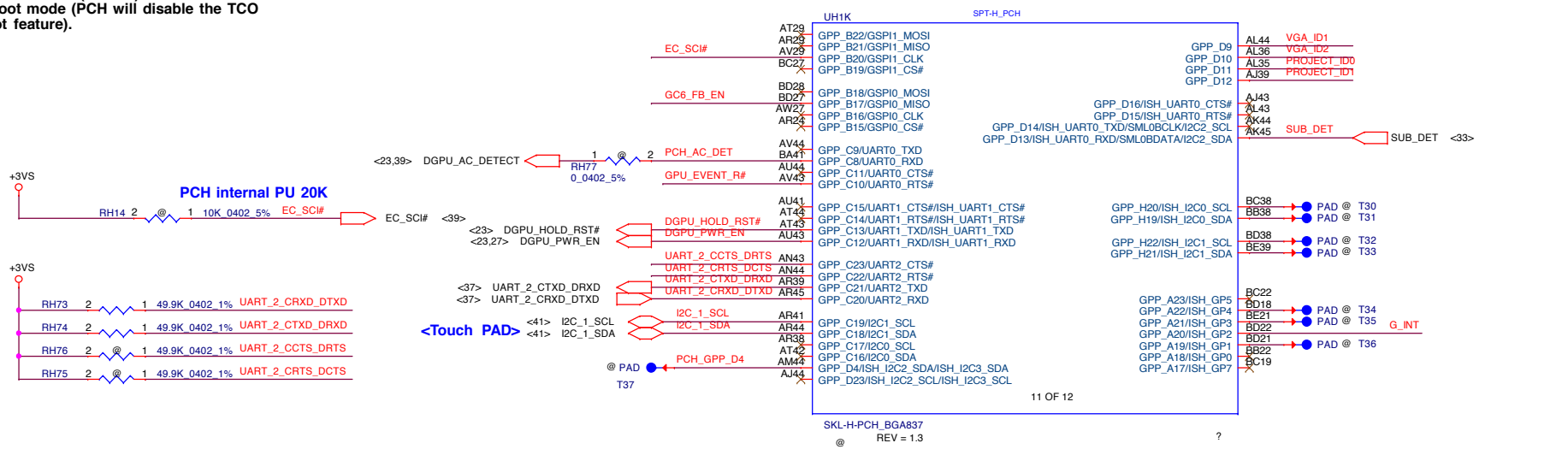
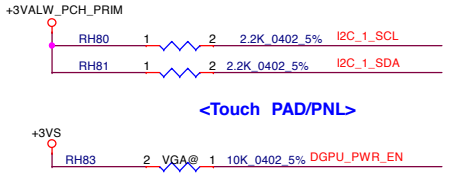
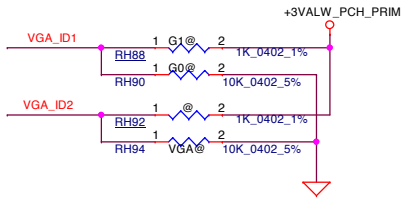
Functional Strap Definitions

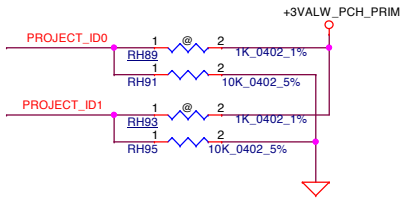
GSPI1_MOSI / GPP_B22
int. PD
Boot BIOS Destination
0 = SPI (Default)
1 = LPC

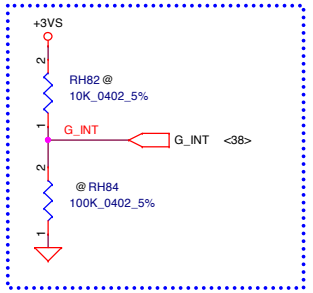
GSPI0_MOSI / GPP_B18
int. PD
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature).

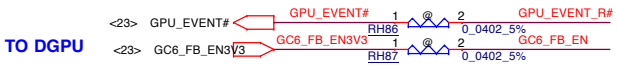












VGA ID	VGA_ID2 GPP_D10	VGA_ID1 GPP_D9
N17P-G0	0	0
N17P-G1	0	1
N17E-G1	1	0
Reserved	1	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*C5MMH	0	0
C5PRH	0	1
Reserved	1	0
Reserved	1	1

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(5/7)UART,I2C,GPIO

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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1.0 Modify

JC2
JUMP_43X118
+1.0VALW
+1.0VALW_PRIM
+1.0VALW_PCH
RH98 0_0805_5%

RH101 for Deep SX

+1.0VALW_PCH
+1.0VALW_DCPDSW
RH101 0_0402_5%
Near PIN BA29
CH28 1U_0402_6.3V6K

+1.0VALW_VCCCLK
RH103 0_0603_5%

LH1 FBMA-L11-160808-800LMT_0603
+1.0VALW_VCCCLK5
Near PIN K2,K3
CH30 22U_0603_6.3V6M
CH31 22U_0603_6.3V6M
CH32 1U_0402_6.3V6K

+1.0VALW_MPHY
RH104 0_0603_5%
modify follow PDG 05/18
CH39 22U_0603_6.3V6M
CH40 1U_0402_6.3V6K
CH41 1U_0402_6.3V6K
CH42 1U_0402_6.3V6K
NO USE MPHYGT ON H CHANGE TO +1.0VALW_MPHY
Near PIN U21,U23,U25,U26,V26
Near PIN V28
Near PIN AC17

+1.0VALW_AMPHYPLL
LH2 FBMA-L11-160808-800LMT_0603
Near PIN A42,A43,B43
CH47 22U_0603_6.3V6M
CH48 22U_0603_6.3V6M
CH49 1U_0402_6.3V6K

+1.0VALW_AUSB_AZPLL
LH3 FBMA-L11-160808-800LMT_0603
Near PIN AJ5,AL5
CH53 22U_0603_6.3V6M
CH54 22U_0603_6.3V6M

+1.0VALW_PRIMAL22
RH106 0_0402_5%

+1.0VALW_PRIMAD15
1.0 Modify
RH107 0_0402_5%
EMC@ CH71 1000P_0402_50V7K
Sensitive net cap for AD15

PCH_EDS Table10-4 12/30 J

UH1H SPT-H_PCH

+1.0VALW_PRIM	2.899A	AA23	VCCPRIM_1P0	CORE VCC	
		AA26	VCCPRIM_1P0		
		AA28	VCCPRIM_1P0		
		AC23	VCCPRIM_1P0		
		AC26	VCCPRIM_1P0		
		AC28	VCCPRIM_1P0		
		AE23	VCCPRIM_1P0		
		AE26	VCCPRIM_1P0		
		Y23	VCCPRIM_1P0		
		Y25	VCCPRIM_1P0		
+1.0VALW_DCPDSW	0.0454A	BA29	DCPDSW_1P0		
+1.0VALW_VCCCLK	0.021A	N17	VCCCLK1		
	0.050A	R19	VCCCLK3		
	0.024A	U20	VCCCLK4		
	0.137A	V17	VCCCLK2		
		R17	VCCCLK2		
	0.006A	K2	VCCCLK5		
+1.0VALW_VCCCLK5		K3	VCCCLK5		
+1.0VALW_MPHY	1.307A	U21	VCCMPHY_1P0	MPHY	
		U23	VCCMPHY_1P0		
		U25	VCCMPHY_1P0		
		U26	VCCMPHY_1P0		
		V26	VCCMPHY_1P0		
+1.0VALW_AMPHYPLL	0.110A	A43	VCCMPHYPLL_1P0		
		B43	VCCMPHYPLL_1P0		
modify follow PDG 05/18		C44	VCCPCIE3PLL_1P0		
		C45	VCCPCIE3PLL_1P0		
+1.0VALW_MPHY	0.030A	V28	VCCAPLLEBB_1P0		
	0.533A	AC17	VCCPRIM_1P0		
+1.0VALW_AUSB_AZPLL	0.012A	AJ5	VCCUSB2PLL_1P0	USB	
	0.033A	AL5	VCCUSB2PLL_1P0		
		AN19	VCCHDAPLL_1P0		
+3VALW_HDA	0.075A	BA15	VCCHDA		
+3VALW_DSW		W15	VCCDSW_3P3		

VCCPRIM_1P0	AL22	0.0908A	+1.0VALW_PRIMAL22		
VCCDSW_3P3	BA24	0.195A	+3VALW_DSW		
VCCPGPPA	BA31	0.082A	+3VALW_PCH_PRIM		
VCCPGPPBCH	BC42	0.2726A			
VCCPGPPBCH	BD40				
VCCPGPPEF	AJ41	0.1410A			
VCCPGPPEF	AL41				
VCCPGPPG	AD41	0.1318A			
VCCPRIM_3P3	AN5	0.2875A			
VCCPRIM_1P0	AD15	0.0061A	+1.0VALW_PRIMAD15		
VCCATS	AD13	0.007A	+3VS_VCCATS		
VCCRTCPRIM_3P3	BA20	0.0002A	+3VALW_PCH_PRIM		
VCCRTC	BA22		+RTCVCC		
DCPRTC	BA26		Near PIN BA26		
	CH34 0.1U_0201_10V6K				
VCCPRIM_1P0	AJ20		+1.0VALW_PRIM		
	AJ21				
	AJ23				
	AJ25				
VCCSPI	BE41	0.029A	+3VALW_SPI		
VCCSPI	BE43				
VCCSPI	BE42				
VCCSPI	BC44	0.078A	+3VALW_PCH_PRIM		
VCCPGPPD	BA45				
VCCPGPPD	BC45				
VCCPGPPD	BB45				
VCCPGPPD					
VCCPRIM_3P3	BD3	0.117A	+3VALW_PCH_PRIM		
VCCPRIM_3P3	BE3				
VCCPRIM_3P3	BE4				

8 OF 12

SKL-H-PCH_BGA837
@ REV = 1.3

+3VALW_HDA
+3VALW_DSW
CH44 1U_0402_6.3V6K
Near PIN W15 Add 05/18

Table 10-6. PCH-H VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (mA)	Details
700	All HSIO disabled. Assumes DMI x4 Running 100%...
132	Each USB 3.0 Port
154	Each PCIe Gen3 Lane
54	First SATA Gen3 Port
132	Each Additional SATA Gen3 Port
102	Each PCIe Gen2 Lane
44	GbE Port

VCCMPHY power defined by HSIO lane qty.

1.0 Modify
+1.0VALW_MPHY
EMC@ CH69 1000P_0402_50V7K
+1.0VALW_MPHY
EMC@ CH70 1000P_0402_50V7K
Sensitive net cap for V28,AC17

+3VALW
+3VALW_DSW
RH97 0_0603_5%
1.0 Modify
+3VALW_PCH_PRIM
RH99 0_0805_5%
+3VALW_HDA
RH100 0_0603_5%

+3VALW_PCH_PRIM
+3VALW_SPI
RH102 0_0603_5%
CH66 0.1U_0201_10V6K

+3VALW_PCH_PRIM
CH51 1U_0402_6.3V6K
+1.0VALW_PRIM
CH52 1U_0402_6.3V6K
+3VALW_PCH_PRIM
CH55 22U_0603_6.3V6M
CH57 22U_0603_6.3V6M
+1.0VALW_PRIM
CH56 22U_0603_6.3V6M
CH58 22U_0603_6.3V6M

+3VALW_PCH_PRIM
CH29 Near PIN BD3,BE3,BE4
CH33 Near PIN BA20
CH35 Near PIN AN5
CH36 No requirment Near PIN BC44
CH37 Near PIN BC42,BD40
CH38 Near PIN AJ41 , AL41
CH43 Near PIN AD41
CH45
CH46 Near PIN BA20
1U_0402_6.3V6K / 0.1U_0201_10V6K / 0.1U_0402_6.3V6K

+3VS
+3VS_VCCATS
RH105 0_0402_5%
CH50 Near PIN AD13

RTC Battery

+RTCVCC
BAV70W_SOT323-3
DH3
+CHGRTC
+RTCBATT
RH163 10K_0402_5% W=20mils
CH60 0.1U_0201_10V6K
CH59 1U_0402_6.3V6K

PN : SC600000B00
Near PIN BA22
09/26 dan

+RTCBATT
JRTC1
GND GND
ACES_50271-0020N-001
CONN@
SP02000RO00

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	

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Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(6/7)POWER

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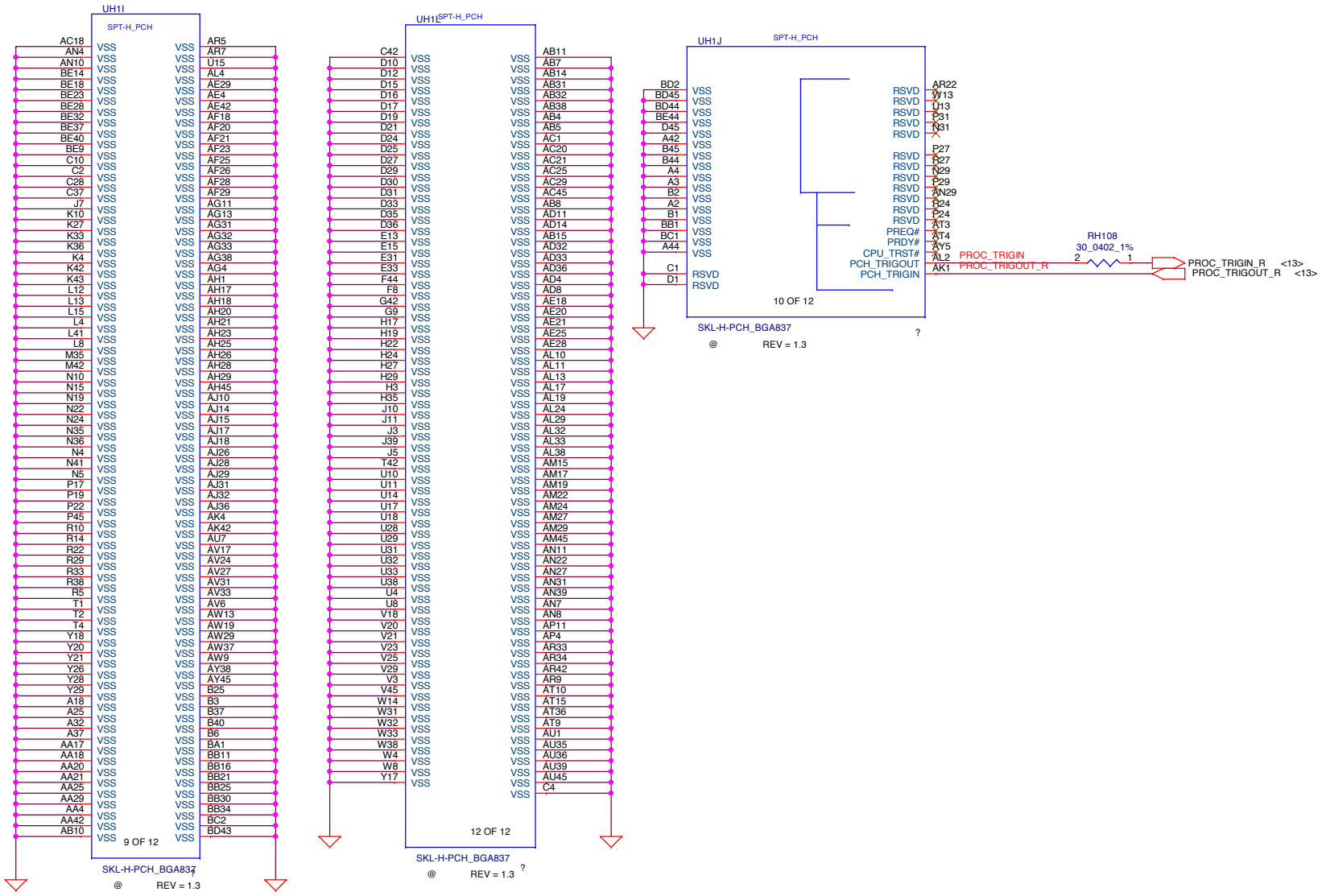

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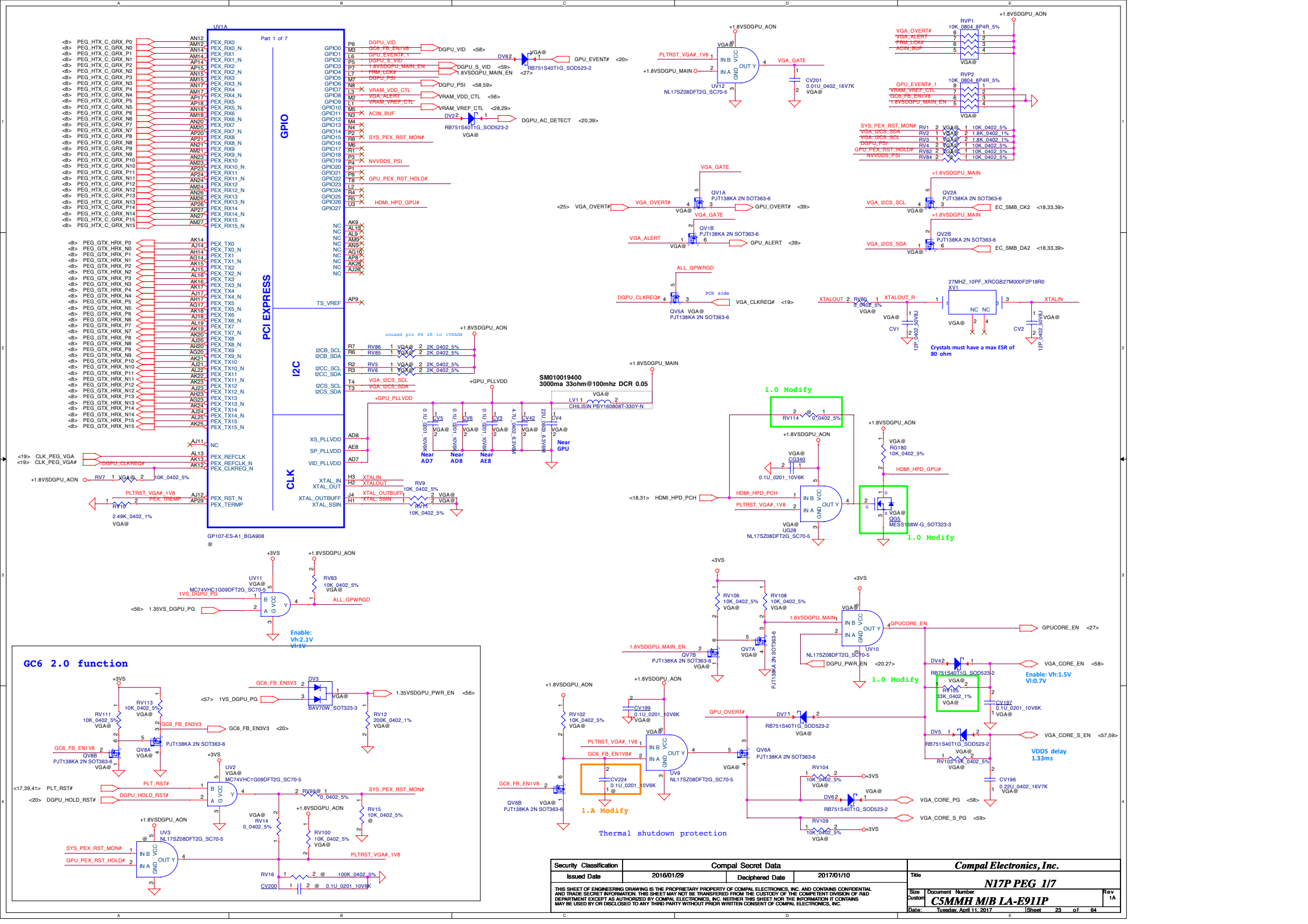
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: PCH(7/7)GND

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

Date: Tuesday, April 11, 2017 | Sheet 22 of 64



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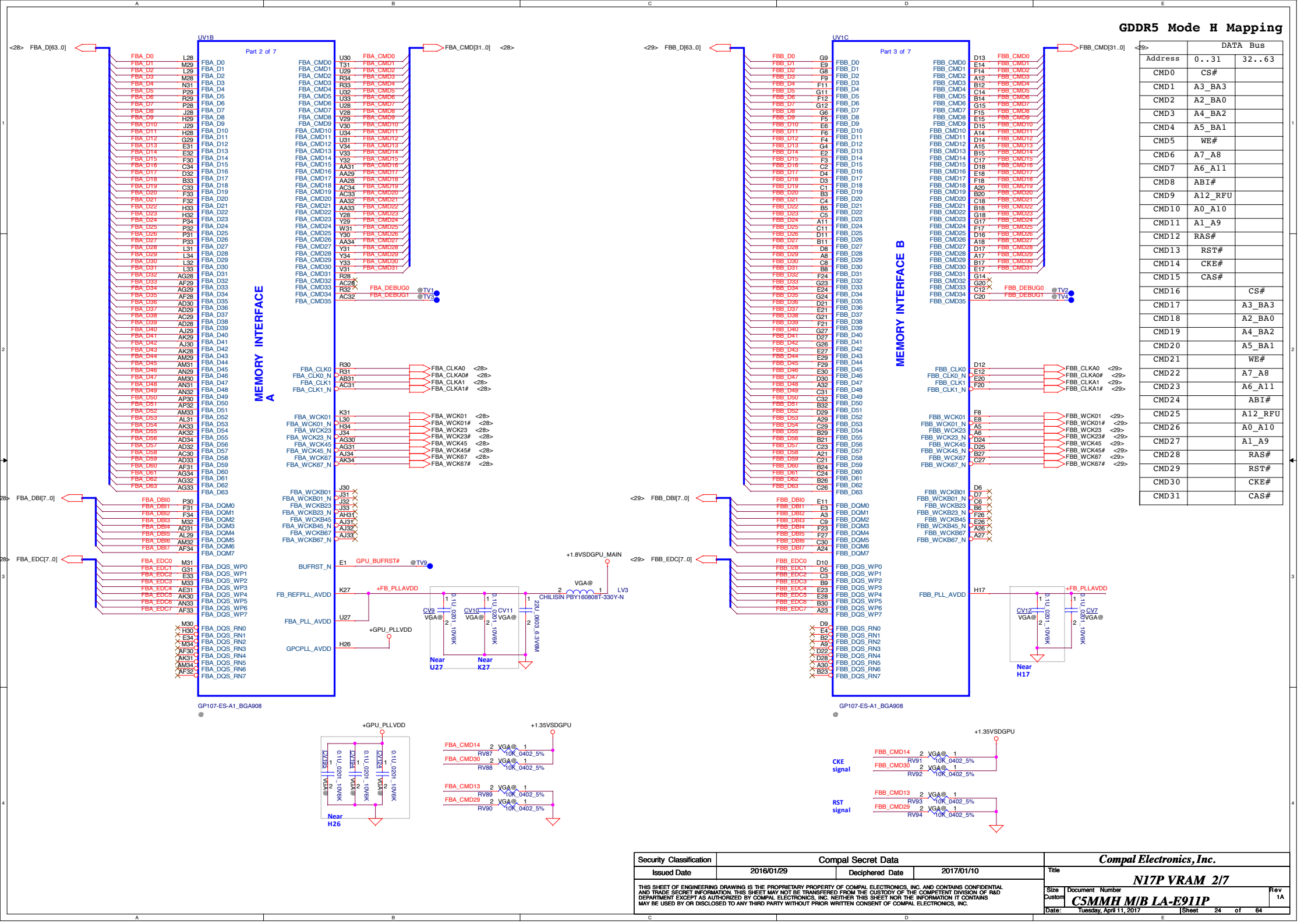
GDDR5 Mode H Mapping
DATA Bus
Address
0..31
32..63
CMD0 CS#
CMD1 A3_BA3
CMD2 A2_BA0
CMD3 A4_BA2
CMD4 A5_BA1
CMD5 WE#
CMD6 A7_A8
CMD7 A6_A11
CMD8 ABI#
CMD9 A12_RFU
CMD10 A0_A10
CMD11 A1_A9
CMD12 RAS#
CMD13 RST#
CMD14 CKE#
CMD15 CAS#
CMD16 CS#
CMD17 A3_BA3
CMD18 A2_BA0
CMD19 A4_BA2
CMD20 A5_BA1
CMD21 WE#
CMD22 A7_A8
CMD23 A6_A11
CMD24 ABI#
CMD25 A12_RFU
CMD26 A0_A10
CMD27 A1_A9
CMD28 RAS#
CMD29 RST#
CMD30 CKE#
CMD31 CAS#
UV1B
Part 2 of 7
MEMORY INTERFACE A
GP107-ES-A1_BGA908
UV1C
Part 3 of 7
MEMORY INTERFACE B
GP107-ES-A1_BGA908
FBA_D[63..0]
FBB_D[63..0]
FBA_CMD[31..0]
FBB_CMD[31..0]
FBA_DBI[7..0]
FBB_DBI[7..0]
FBA_EDC[7..0]
FBB_EDC[7..0]
FBA_DEBUG0
FBA_DEBUG1
FBB_DEBUG0
FBB_DEBUG1
FBA_CLK0
FBA_CLK0_N
FBA_CLK1
FBA_CLK1_N
FBA_CLKA0
FBA_CLKA0#
FBA_CLKA1
FBA_CLKA1#
FBA_WCK01
FBA_WCK01_N
FBA_WCK23
FBA_WCK23_N
FBA_WCK45
FBA_WCK45_N
FBA_WCK67
FBA_WCK67_N
FBA_WCK23#
FBA_WCK45#
FBA_WCK67#
FBA_WCKB01
FBA_WCKB01_N
FBA_WCKB23
FBA_WCKB23_N
FBA_WCKB45
FBA_WCKB45_N
FBA_WCKB67
FBA_WCKB67_N
BUFRST_N
GPU_BUFRST#
FB_REFPLL_AVDD
FBA_PLL_AVDD
GPCPLL_AVDD
+FB_PLLAVDD
+GPU_PLLVDD
+1.8VSDGPU_MAIN
VGA@
CHILISIN PBY160808T-330Y-N
0.1U_0201_10V6K
2200P_0603_6.3V6M
Near U27
Near K27
Near H26
Near H17
+1.35VSDGPU
RV87 10K_0402_5%
RV88 10K_0402_5%
RV89 10K_0402_5%
RV90 10K_0402_5%
RV91 10K_0402_5%
RV92 10K_0402_5%
RV93 10K_0402_5%
RV94 10K_0402_5%
CKE signal
RST signal
Security Classification
Compal Secret Data
Issued Date
2016/01/29
Deciphered Date
2017/01/10
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1A
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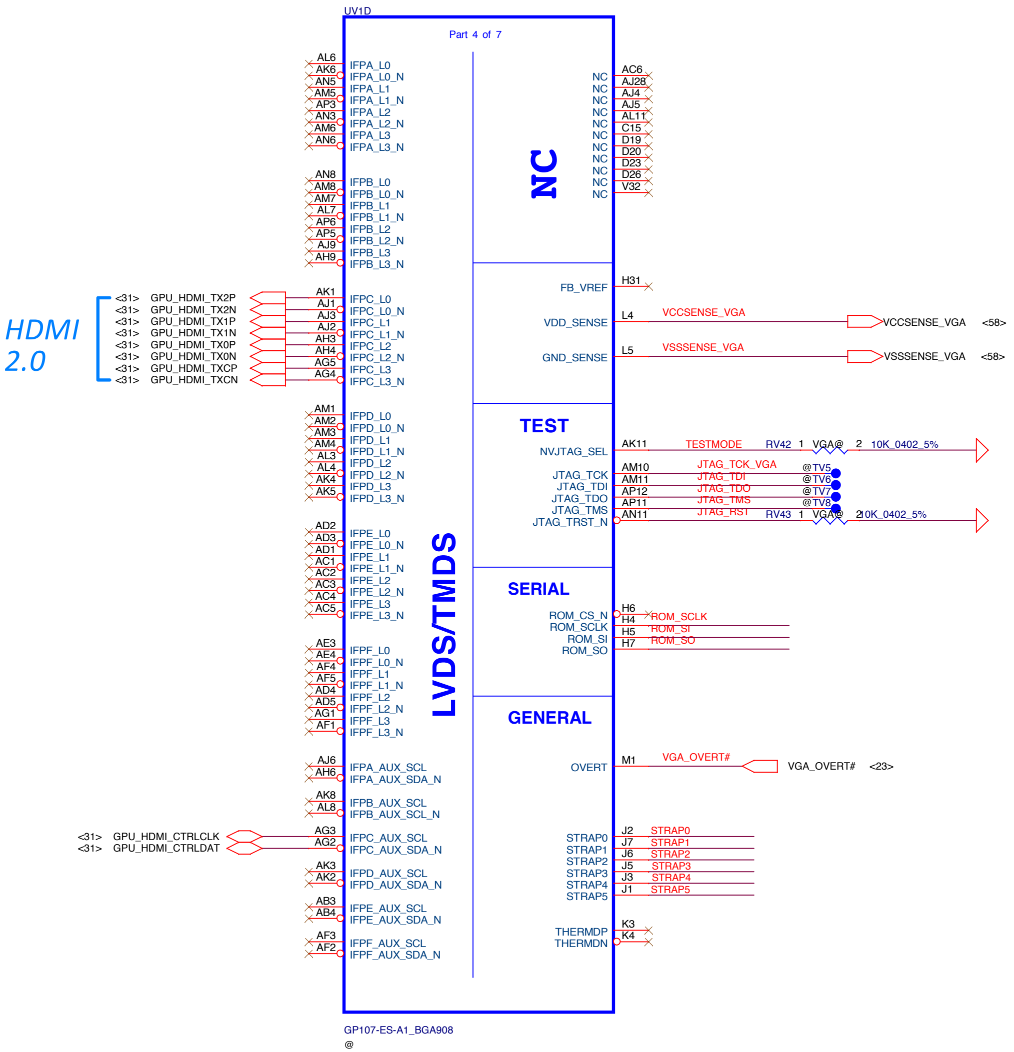

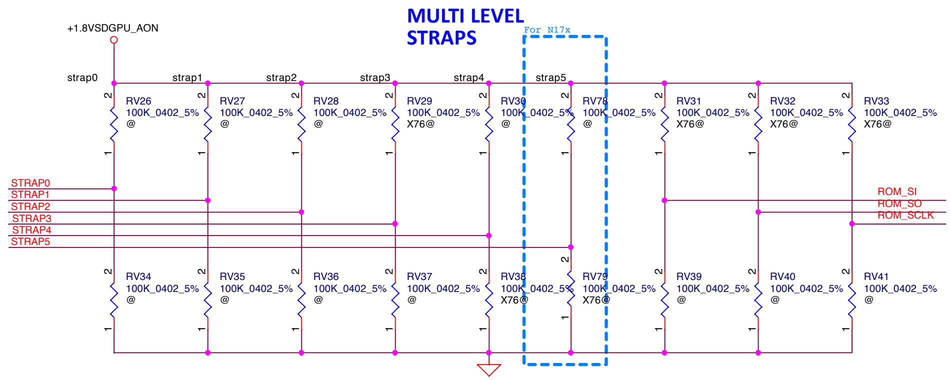

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V²	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V²	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V²	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V²	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

HDMI audio output

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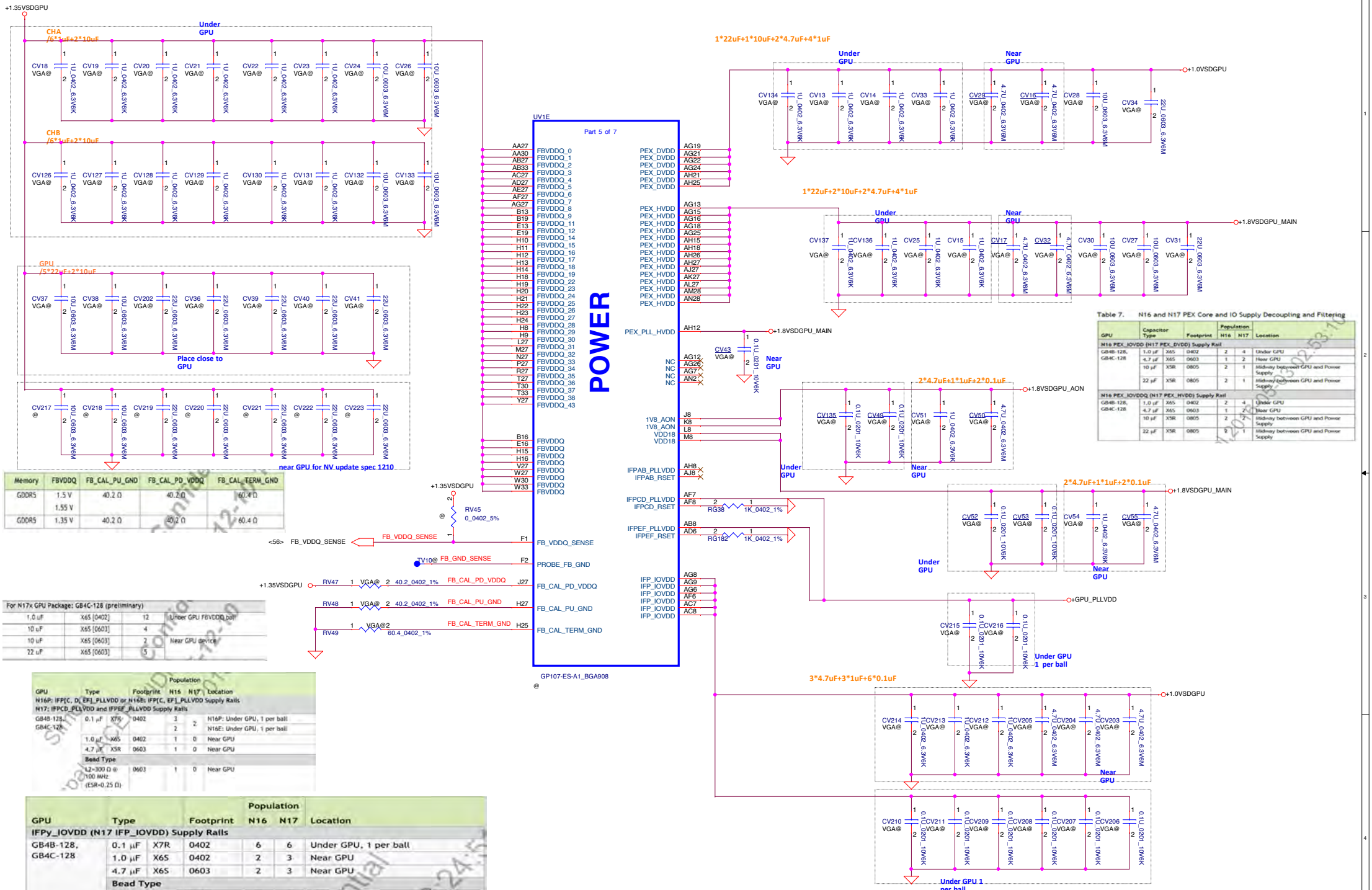
				Date: Tuesday, April 11, 2017; Sheet 25 of 64



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Issued Date	2016/01/29	Deciphered Date	2017/01/10

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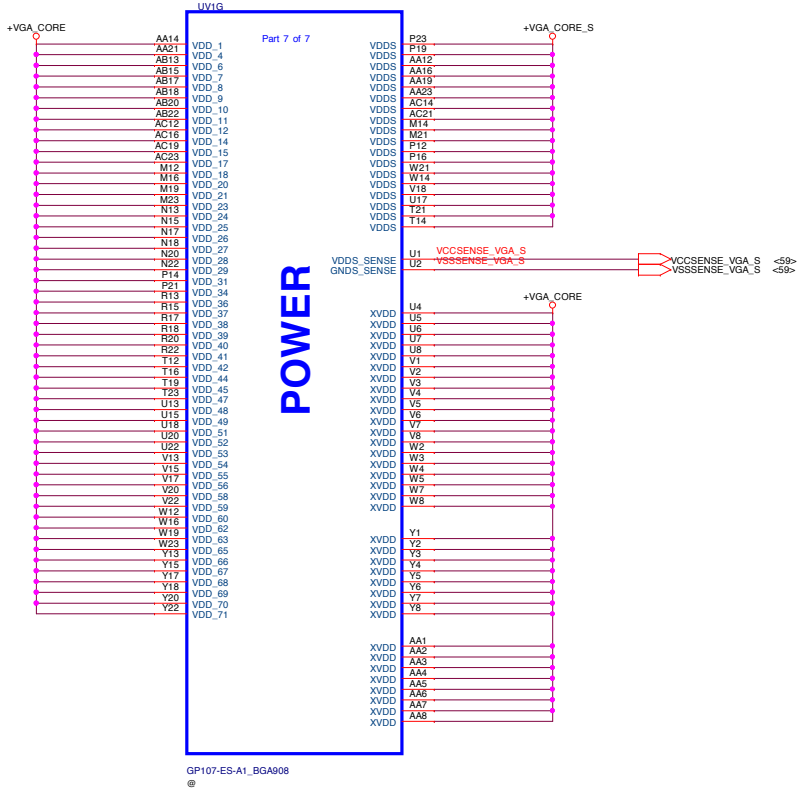
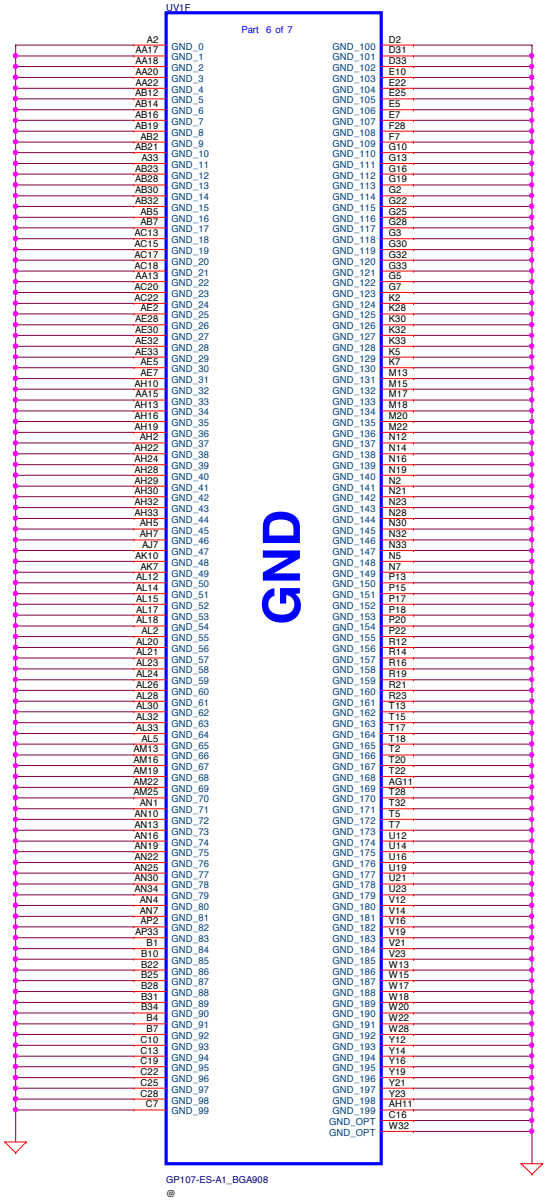
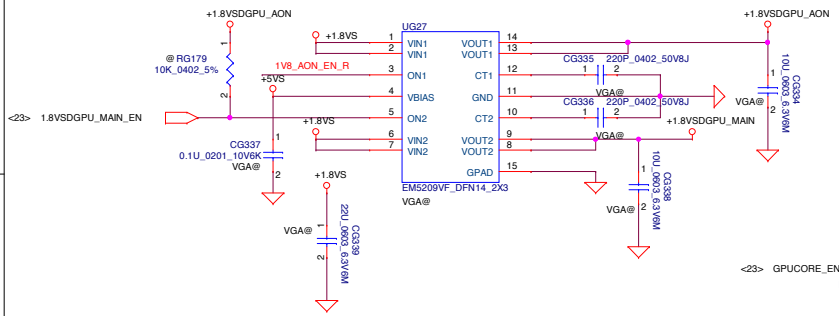
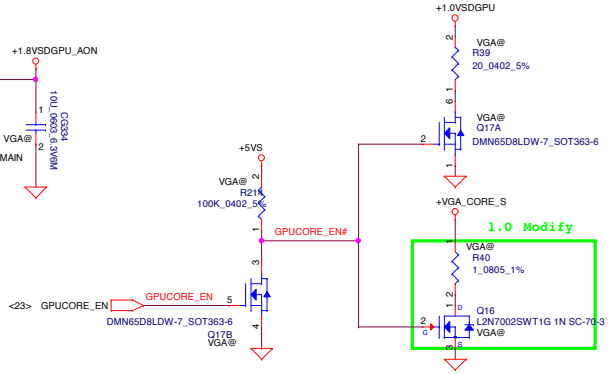
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



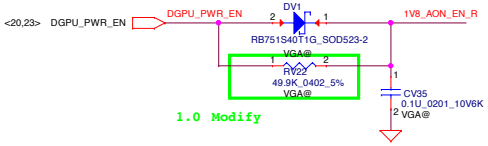


+1.8V_AON/+1.8V_MAIN





For Power down sequence



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MF=0

MF=1

<24> FBA_D[63:0]

UV4B 2 OF 2

<24> FBA_CMD6
<24> FBA_CMD11
<24> FBA_CMD10
<24> FBA_CMD7
<24> FBA_CMD9
<24> FBA_CMD2
<24> FBA_CMD4
<24> FBA_CMD3
<24> FBA_CMD1
<24> FBA_CMD8
<24> FBA_CMD12
<24> FBA_CMD0
<24> FBA_CMD15
<24> FBA_CMD5
<24> FBA_CLKA0
<24> FBA_CLKA0#
<24> FBA_CMD14
<24> FBA_DBI0
<24> FBA_DBI1
<24> FBA_DBI2
<24> FBA_DBI3
<24> FBA_CMD13
FBA0_ZQ1
<24> FBA_WCK01
<24> FBA_WCK01#
<24> FBA_WCK23
<24> FBA_WCK23#

A8/A7 A9/A1 A10/A0 A11/A6 A12/RFU#J5/NC#J5
BA0/A2 BA1/A5 BA2/A4 BA3/A3
ABI# RAS# CS# CAS# WE#
CK CK# CKE#
DBI0# DBI1# DBI2# DBI3#
RESET#
SEN ZQ MF
WCK01 WCK01#
WCK23 WCK23#

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31

EDC0 EDC1 EDC2 EDC3
FBA_EDC0 <24>
FBA_EDC1 <24>
FBA_EDC2 <24>
FBA_EDC3 <24>

VGA@ RV57 1K_0402_5%
VGA@ RV58 121_0402_1%
VGA@ RV59 1K_0402_5%

X76@

+1.35VSDGPU

RV50 549_0402_1% VGA@
RV51 931_0402_1% VGA@
FBA0_VREFC
RV52 1.33K_0402_1% VGA@

FBA_VREFC_R

RV53 549_0402_1% VGA@
RV54 931_0402_1% VGA@
FBA1_VREFC
RV56 1.33K_0402_1% VGA@

<23,29> VRAM_VREF_CTL
QV3 MESS138W-G_SOT323-3
1.0 Modify

UV5B 2 OF 2

<24> FBA_CMD26
<24> FBA_CMD23
<24> FBA_CMD22
<24> FBA_CMD27
<24> FBA_CMD25
<24> FBA_CMD19
<24> FBA_CMD17
<24> FBA_CMD18
<24> FBA_CMD20
<24> FBA_CMD24
<24> FBA_CMD31
<24> FBA_CMD21
<24> FBA_CMD28
<24> FBA_CMD16
<24> FBA_CLKA1
<24> FBA_CLKA1#
<24> FBA_CMD30
<24> FBA_DBI7
<24> FBA_DBI6
<24> FBA_DBI5
<24> FBA_DBI4
<24> FBA_CMD29
<24> FBA_WCK67
<24> FBA_WCK67#
<24> FBA_WCK45
<24> FBA_WCK45#

RV55 VGA@ 1K_0402_5%
FBA1_ZQ3
RV60 VGA@ 1K_0402_5%
RV61 VGA@ 121_0402_1%

FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39

FBA_EDC7 <24>
FBA_EDC6 <24>
FBA_EDC5 <24>
FBA_EDC4 <24>

UV4A 1 OF 2

VDD VDDQ VSS VSSQ VREFC VREFD VPP/NC#A5 VPP/NC#U5

FBA_CLKA0 FBA_CLKA0#
RV63 40.2_0402_1%
RV95 40.2_0402_1%
CV190 0.01U_0402_16V7K

FBA_CLKA1 FBA_CLKA1#
RV96 40.2_0402_1%
RV62 40.2_0402_1%
CV191 0.01U_0402_16V7K

(3GHz and up)

CV58 CV59 CV67 CV56 CV57 CV60 CV68 1U_0402_6.3V6K
Close to VRAM
CV143 CV142 CV140 1U_0402_6.3V6K
CV73 CV74 CV75 CV76 10U_0402_6.3V6M
Close to VRAM
CV84 CV85 10U_0402_6.3V6M
CV70 CV71 CV72 CV138 CV139 22U_0603_6.3V6M
Around VRAM
CV161 CV160 CV158 CV162 CV163 CV164 CV159 CV165 1U_0402_6.3V6K
x32 only

FBA0_VREFC
CV89 820P_0402_50V7K

CV61 CV62 CV63 CV64 CV65 CV66 CV69 1U_0402_6.3V6K
Close to VRAM
CV77 CV78 CV79 CV80 CV81 CV82 CV83 10U_0402_6.3V6M
Close to VRAM
CV86 CV87 CV143 CV144 CV145 CV147 CV148 22U_0603_6.3V6M
Around VRAM
CV166 CV168 CV167 CV170 CV169 CV172 CV171 CV173 1U_0402_6.3V6K
x32 only

FBA1_VREFC
CV88 820P_0402_50V7K

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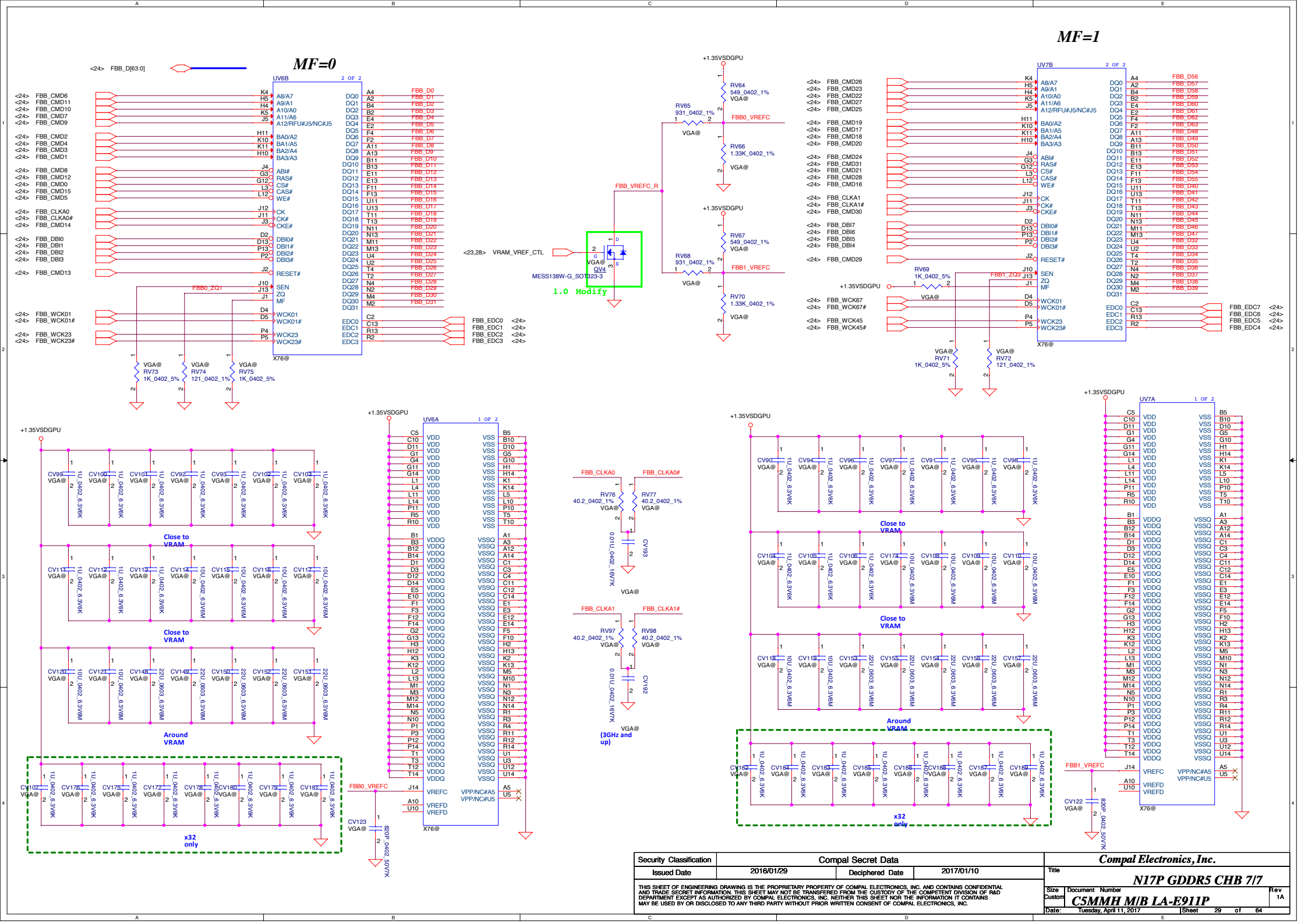

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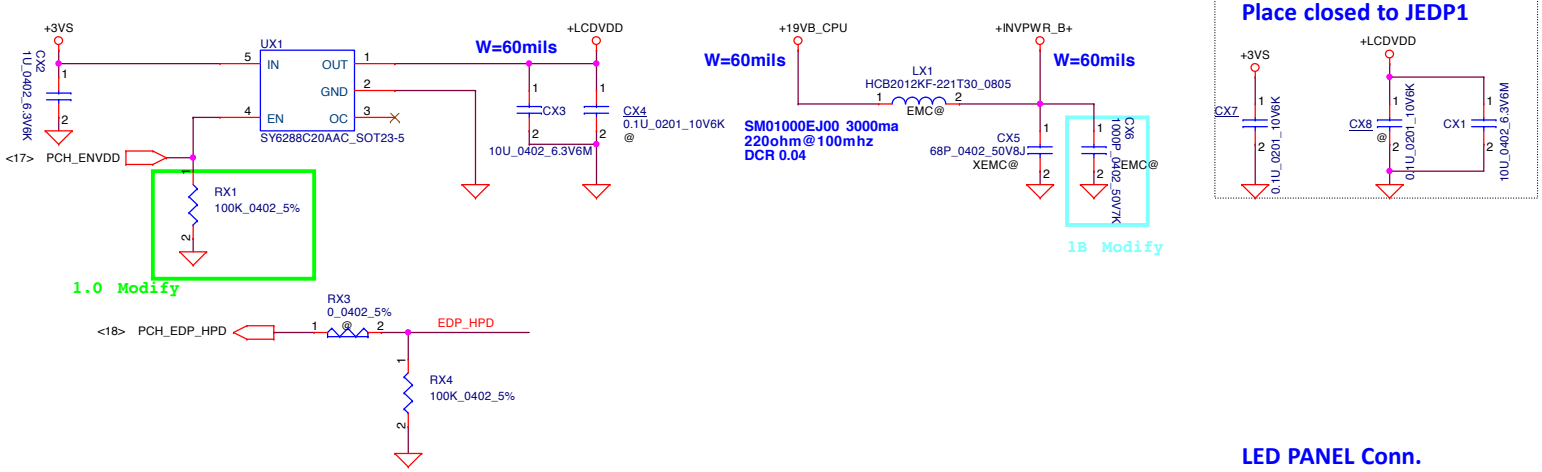
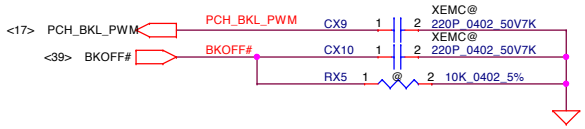
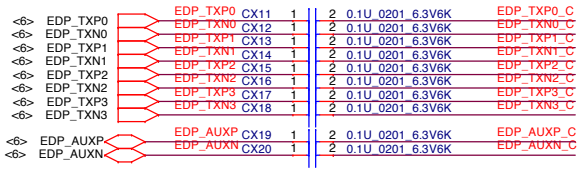
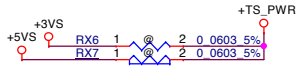
LCD POWER CIRCUIT





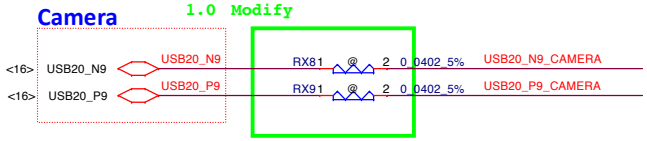


Touch Screen

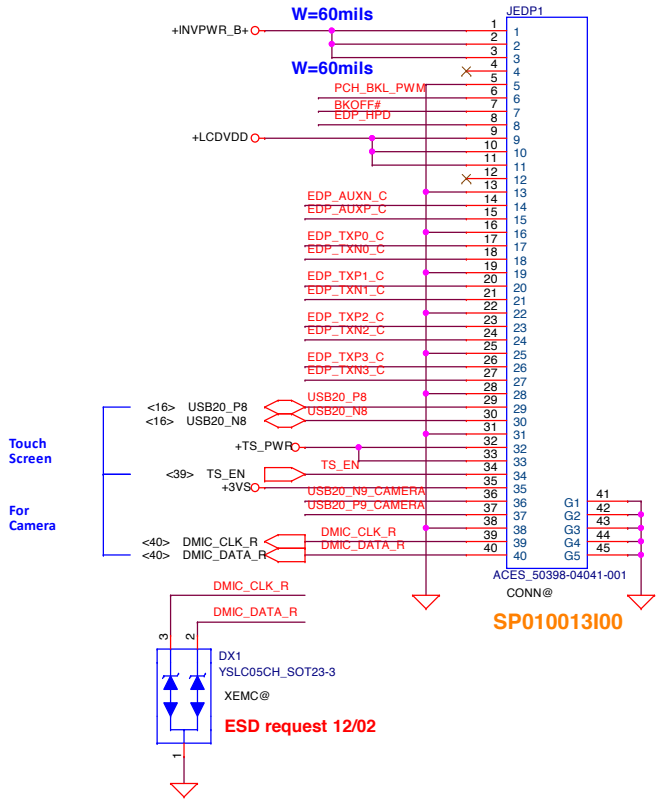


Camera

1.0 Modify



LED PANEL Conn.



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Title: eDP CONN.

Size	Document Number	Rev
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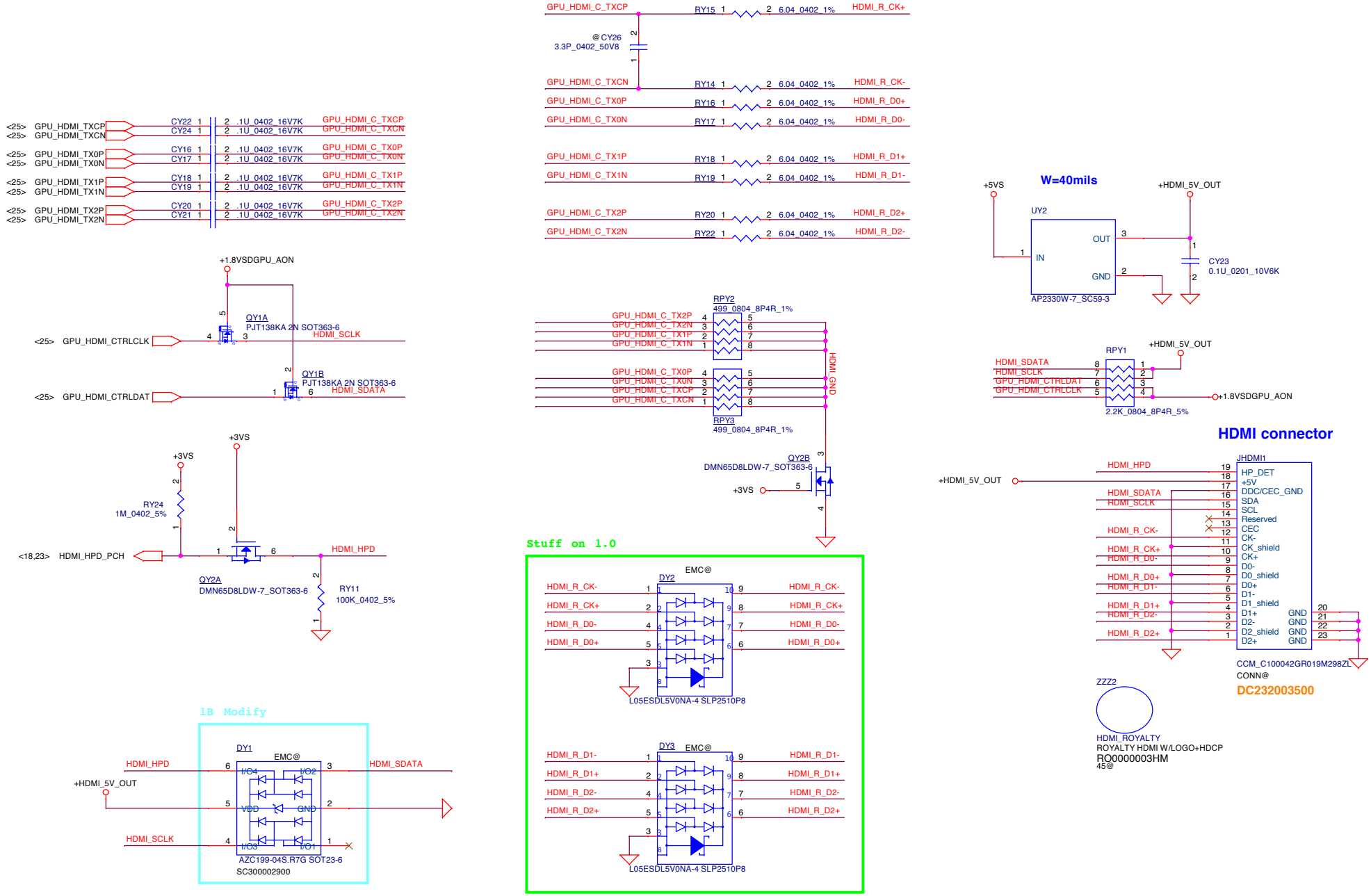

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: **HDMI CONN.**

Size	Document Number	Rev
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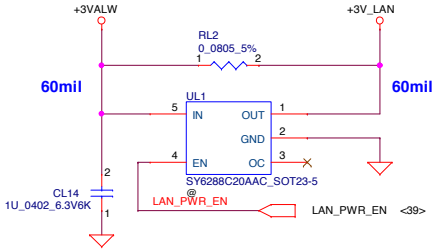
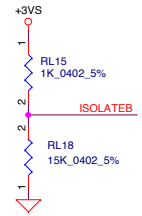
LAN-RTL8411B

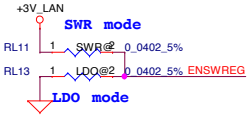


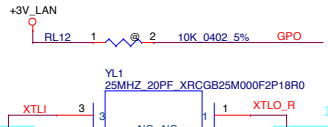
From EC

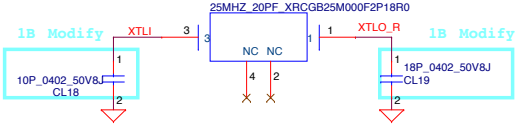
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

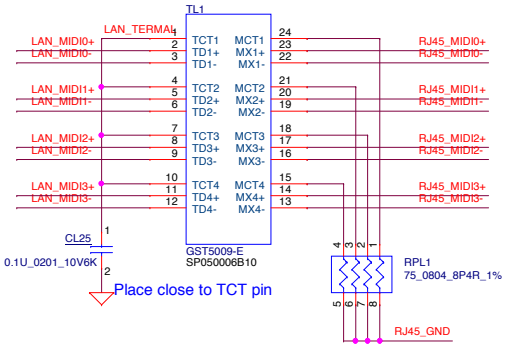
+3V_LAN Rising time must >0.5ms and <100ms

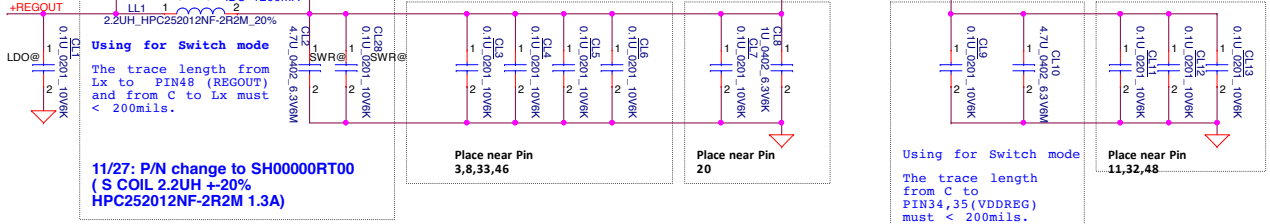


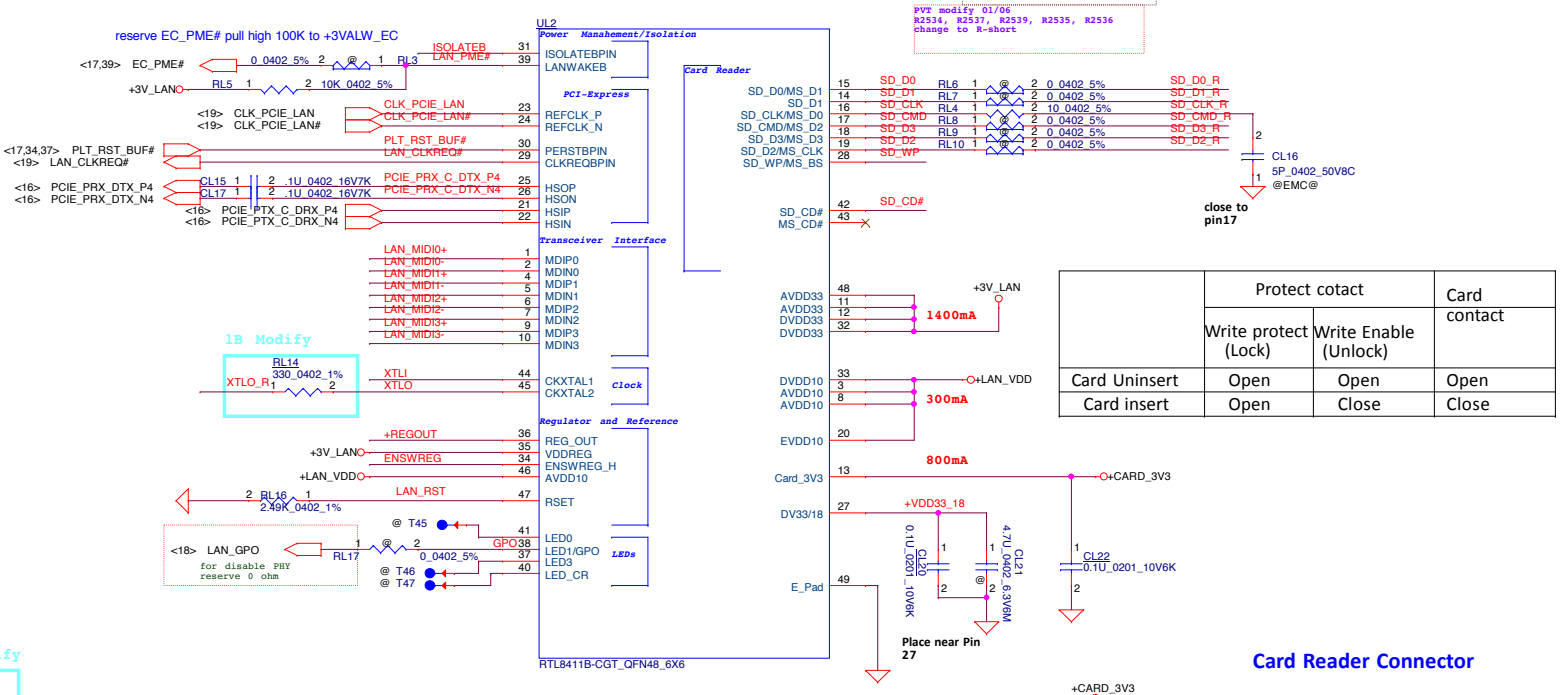








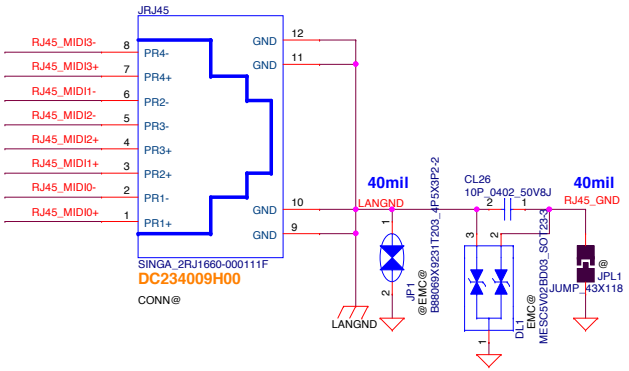




PVT modify 01/06
R2534, R2537, R2539, R2535, R2536 change to R-short

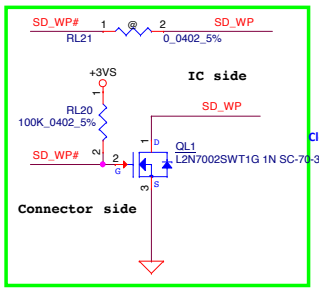
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

LAN Connector



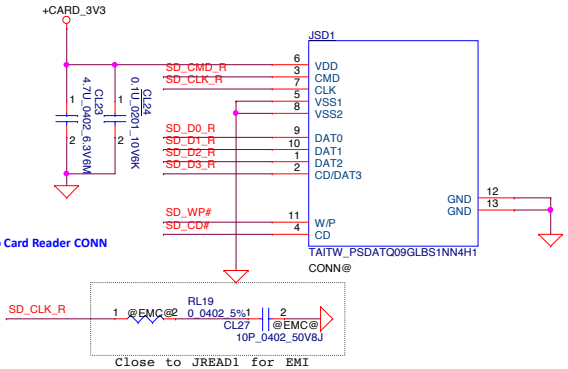
1.0 Modify

SD Write protect inverter circuit



Close to Card Reader CONN

Card Reader Connector



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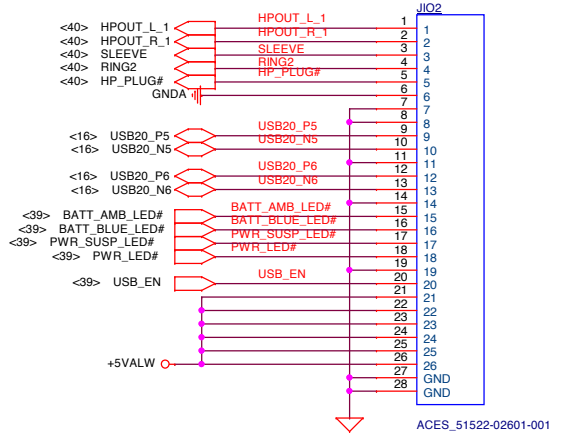
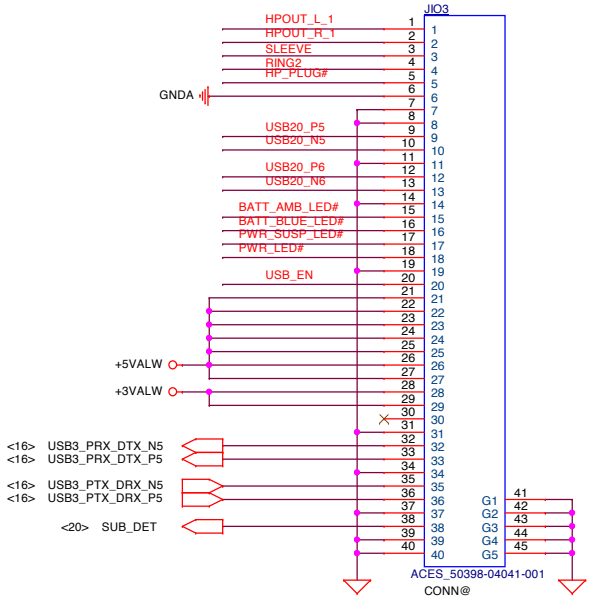
To USB/B Co lay CONN

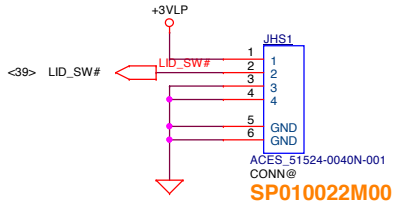


SP01001AO00



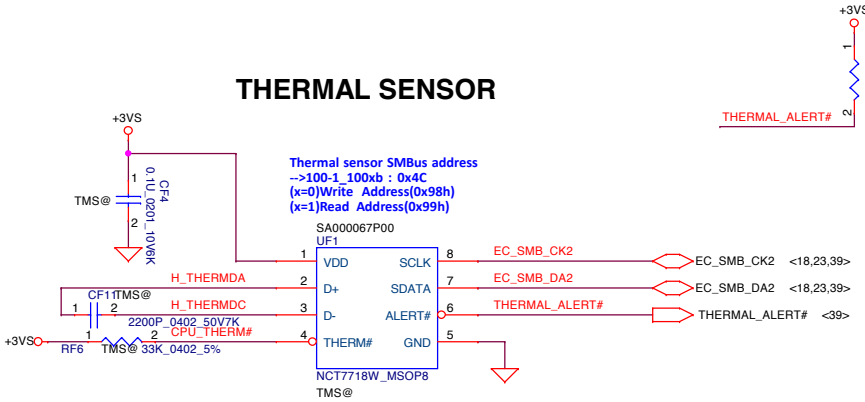
SP010013I00

To Hall sensor/B



SP010022M00

THERMAL SENSOR



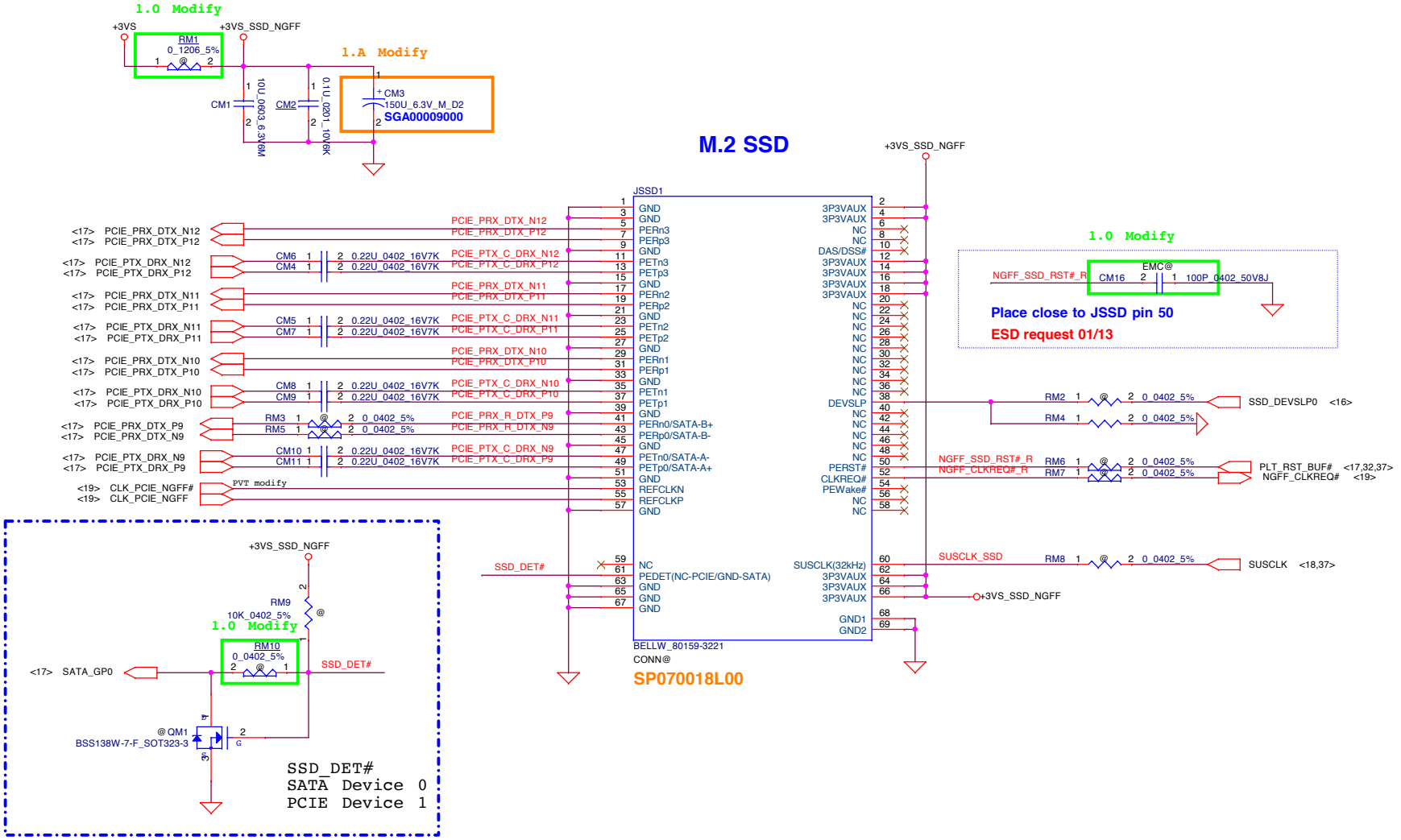
Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: FUN/B & LED/B

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

Date: Tuesday, April 11, 2017 | Sheet 33 of 64



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

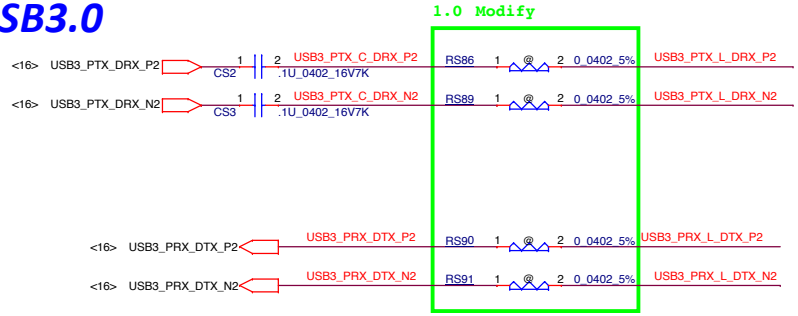
Compal Electronics, Inc.

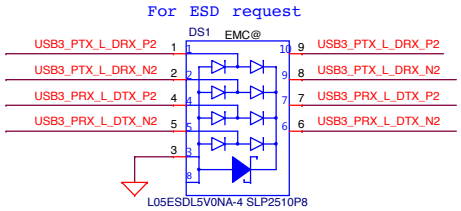
Title: mSATA-SSD

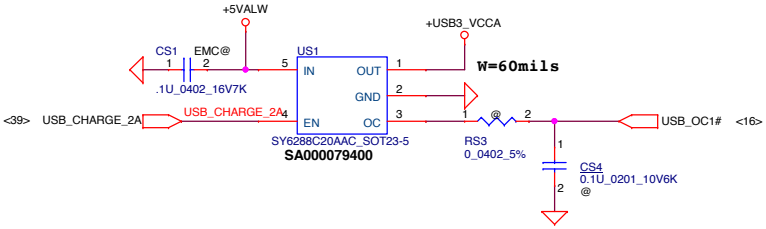
Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

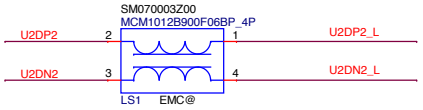
Date: Tuesday, April 11, 2017 | Sheet 34 of 64

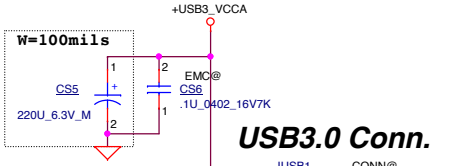
USB3.0



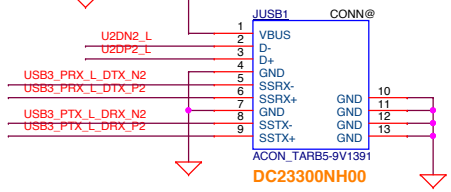






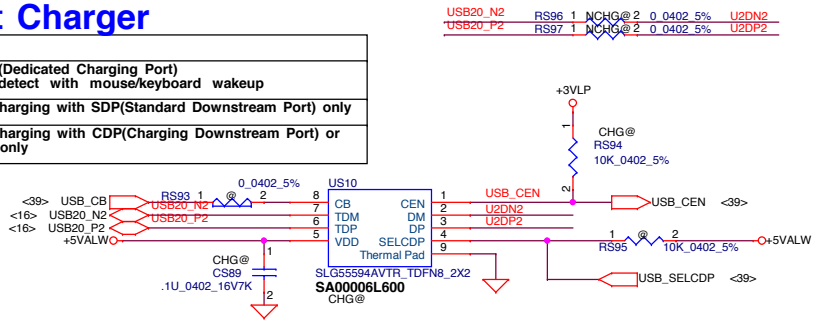


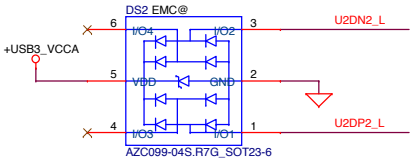
USB3.0 Conn.



USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only





Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: USB3.0 Conn/USB Charger

Size	Document Number	Rev
Custom	C5MMH M/B LA-E911P	1A

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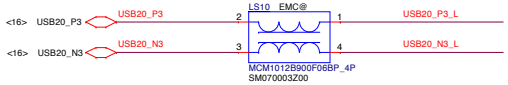
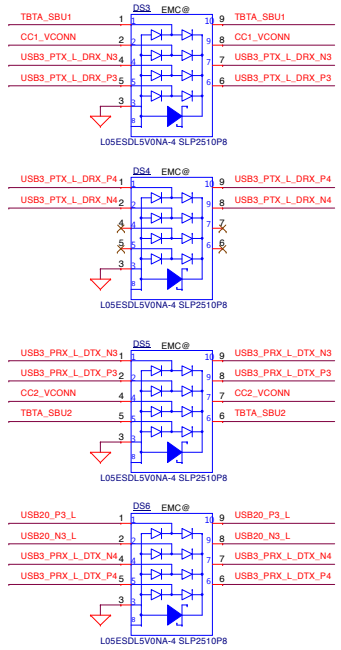
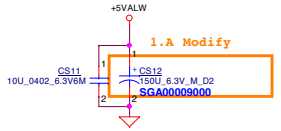
USB3.0 (Port 3)

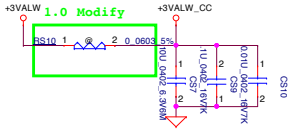


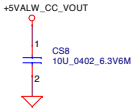
For ESD request

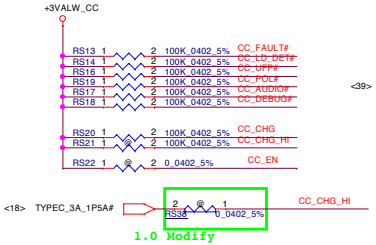


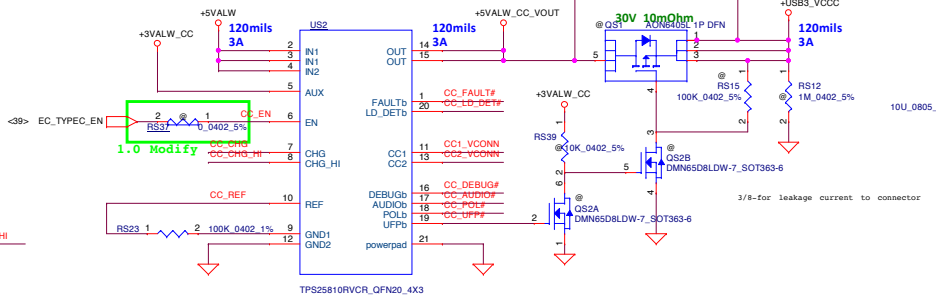
USB3.0 (Port 4)











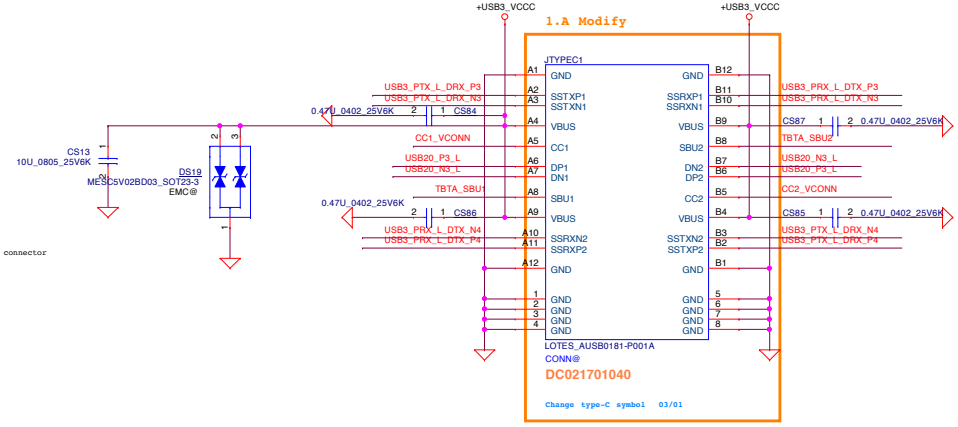


Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On[1]	Off

Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: CC+USB TYPE C

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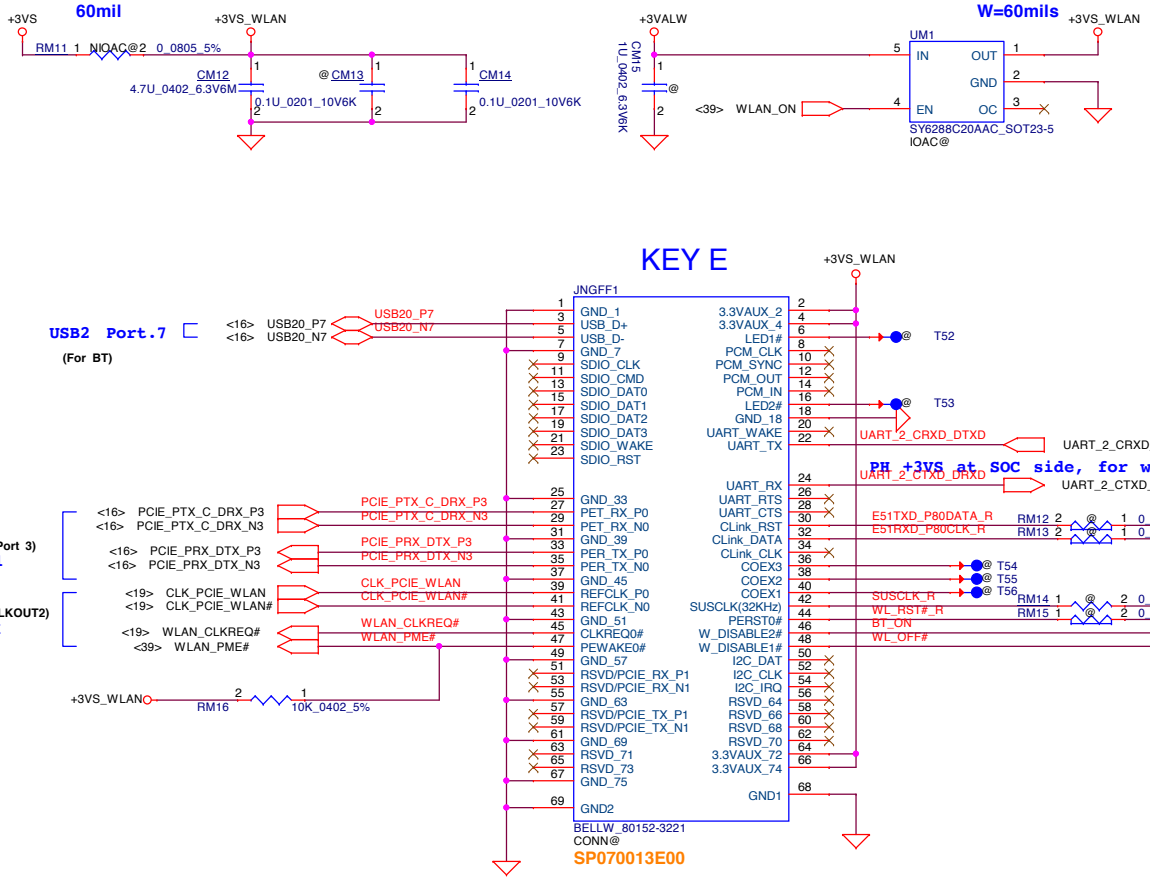
Wireless LAN



NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I)(O/3.3)	GND	63
60	I2C CLK (O)(O/3.3)	Reserved/PETn1	61
58	I2C DATA (IO)(O/3.3)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(O/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(O/3.3V)	PEWake0# (IO)(O/3.3V)	55
52	PERST0# (O)(O/3.3V)	CLKREQ0# (IO)(O/3.3V)	53
50	SUSCLK(32kHz) (O)(O/3.3V)	GND	51
48	COEX1 (I/O)(O/1.8V)	REFCLKN0	49
46	COEX2(I/O)(O/1.8V)	REFCLKP0	47
44	COEX3(I/O)(O/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(O/1.8V)	PETn0	37
34	UART CTS (I)(O/1.8V)	PETp0	35
32	UART Tx (O)(O/1.8V)	GND	33
	[redacted]	[redacted]	
22	UART Rx (I)(O/1.8V)	SDIO Reset# (O)(O/1.8V)	23
20	UART Wake# (I)(O/3.3V)	SDIO Wake# (I)(O/1.8V)	21
18	GND	SDIO DAT3(IO)(O/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(O/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(O/1.8V)	SDIO DAT1(IO)(O/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(O/1.8V)	SDIO DAT0(IO)(O/1.8V)	13
10	PCM_SYNC/I2S WS (OI)(O/1.8V)	SDIO CMD(IO)(O/1.8V)	11
8	PCM_CLK/I2S SCK (OI)(O/1.8V)	SDIO CLK(IO)(O/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: M.2 Key E (WLAN)

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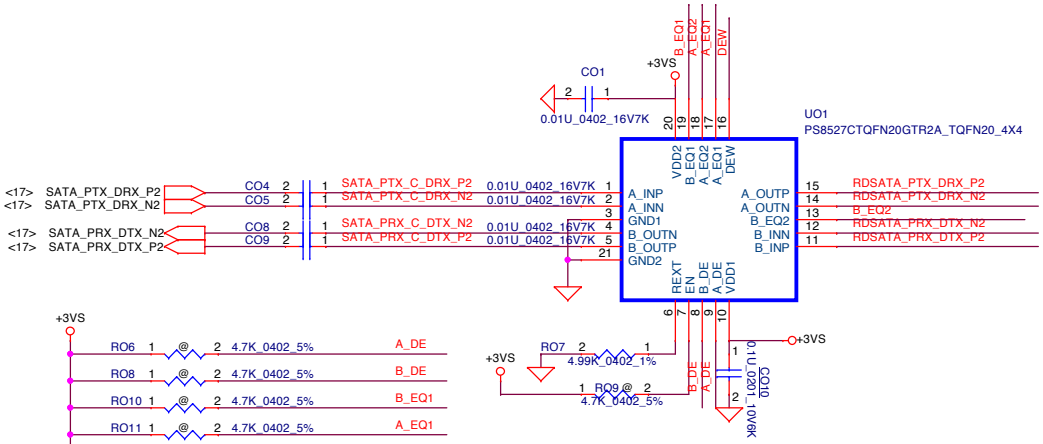
SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10

Chip Enable. Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)

Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

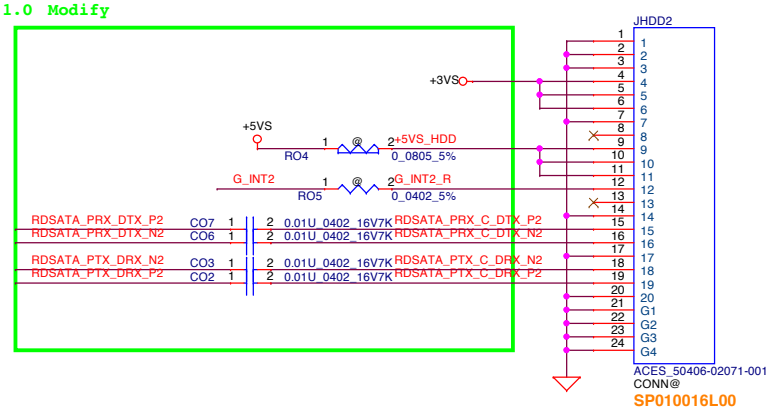
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

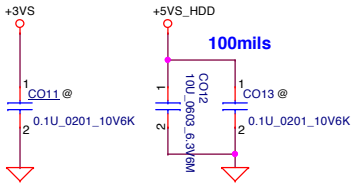
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

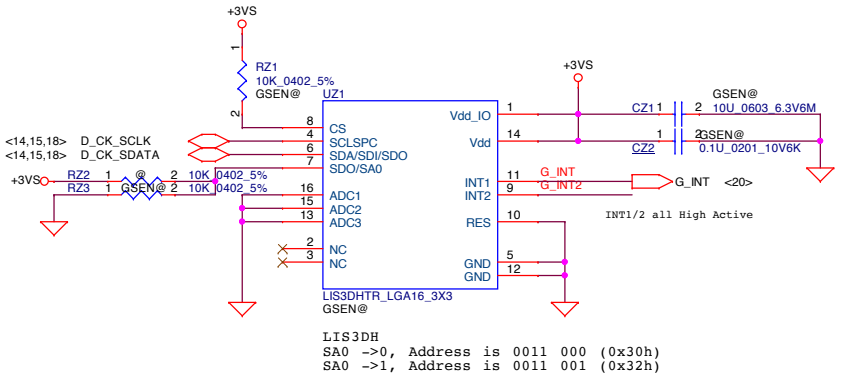
B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

1.0 Modify





G-Sensor reserved



LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: HDD/ Re-Driver/ G-sensor

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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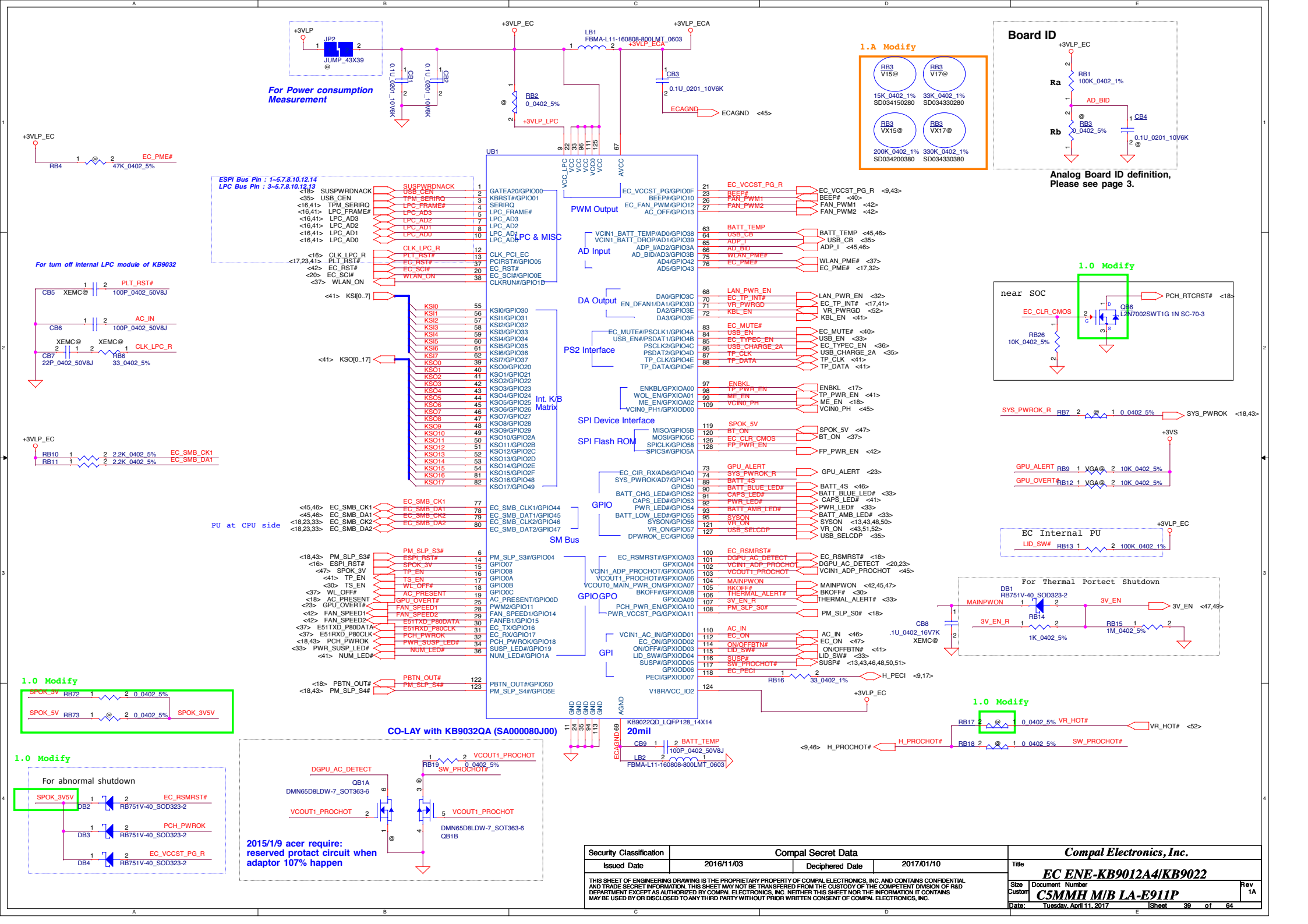

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.			
Title: EC ENE-KB9012A4/KB9022			
Size: Custom	Document Number: C5MMH M/B LA-E911P		Rev: 1A
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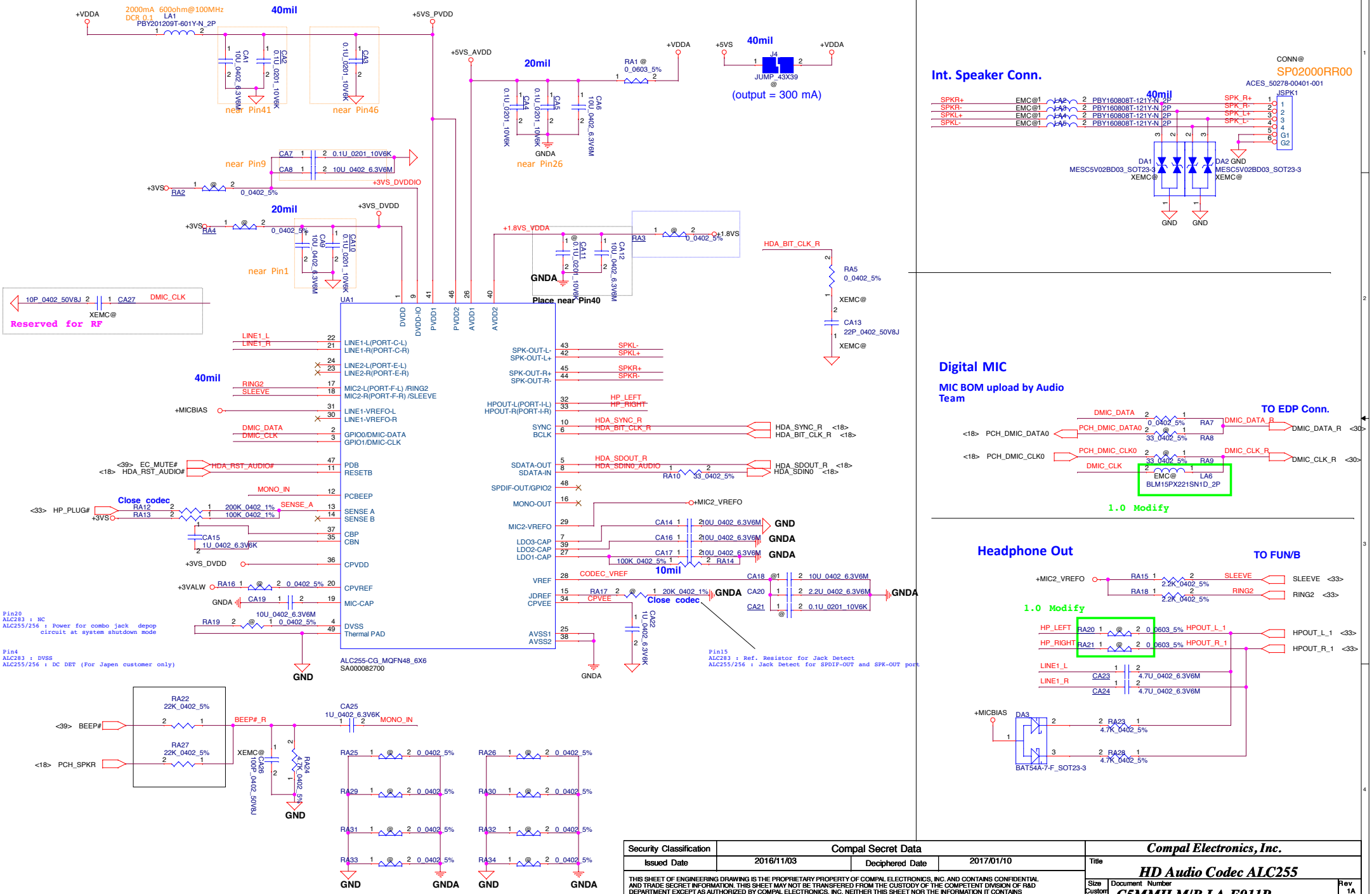
HD Audio Codec



Int. Speaker Conn.

Digital MIC

MIC BOM upload by Audio Team

Headphone Out

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.	
Title	HD Audio Codec ALC255
Size: Custom	Document Number: C5MMH M/B LA-E911P
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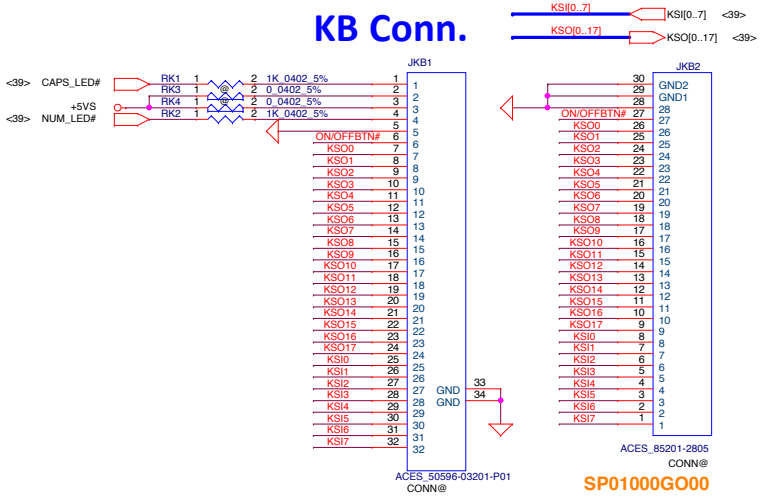
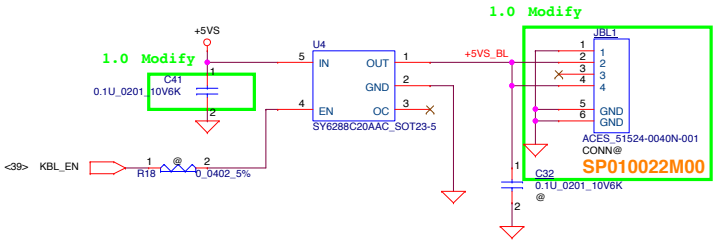
Date: Tuesday, April 11, 2017	Sheet 40 of 64

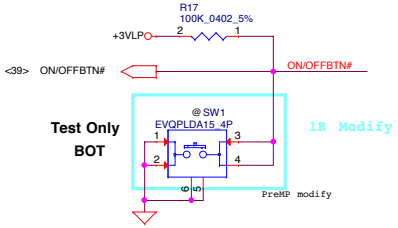
KB Conn.



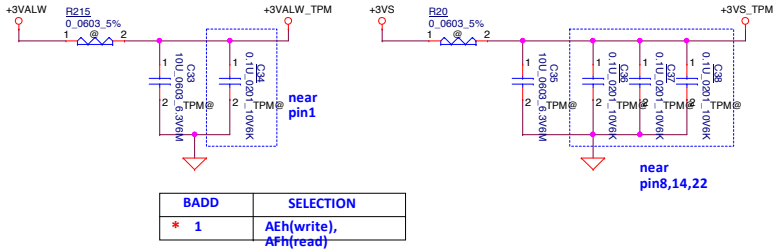
KB BackLight



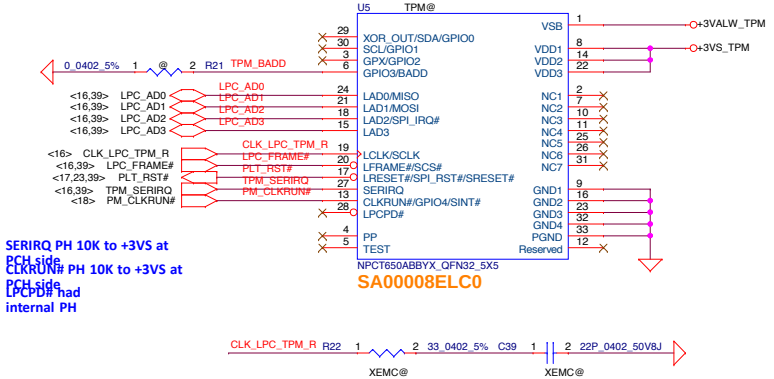
ON/OFF BTN



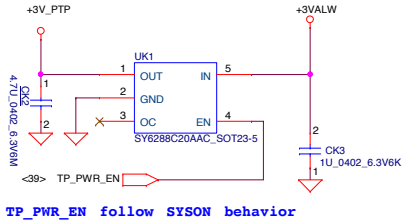
TPM

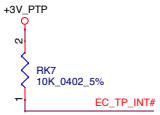


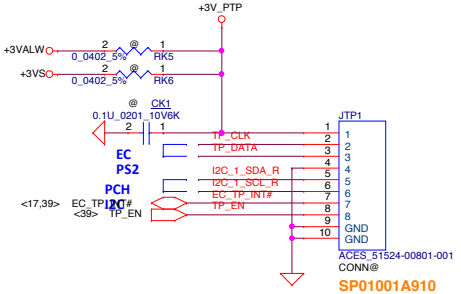
BADD	SELECTION
* 1	AEh(write), AFh(read)

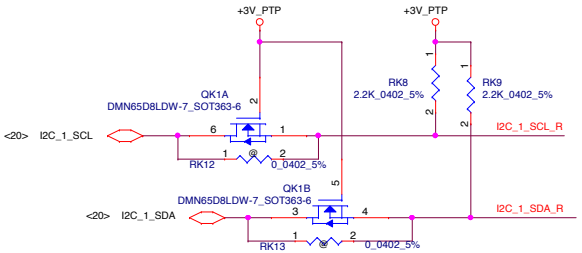


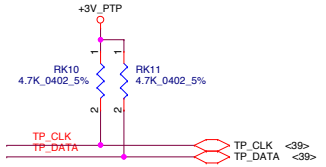
Touch Pad











Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.			
Title: KB & TP & TPM Connector			
Size: Custom	Document Number: C5MMH M/B LA-E911P		Rev: 1A
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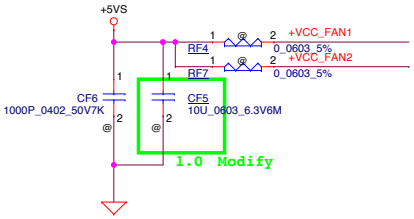
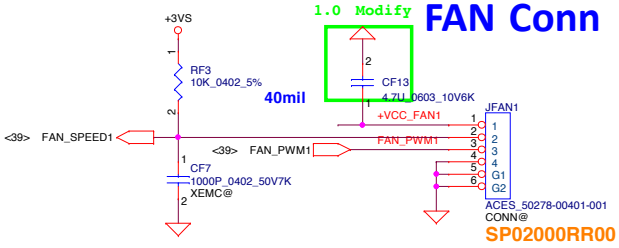
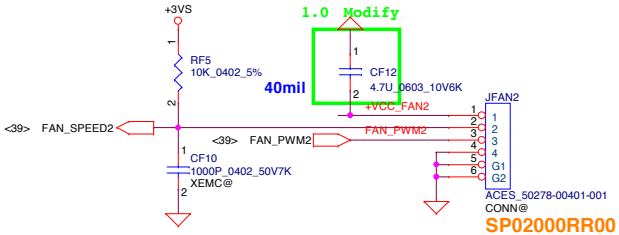


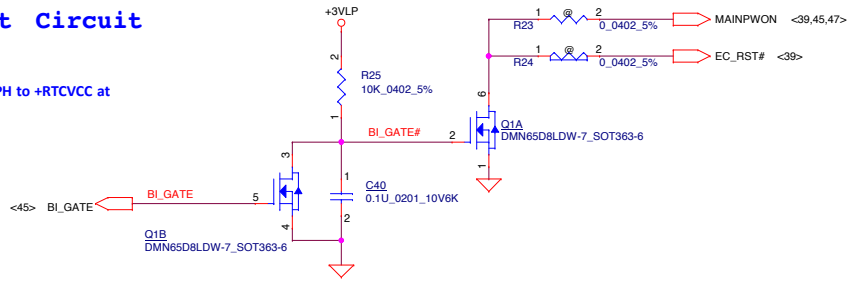
FAN Conn





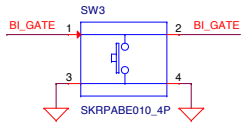
Reset Circuit

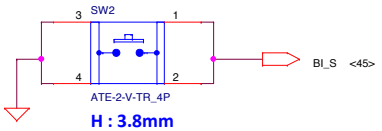
BI_GATE PH to +RTCVCC at PWR side



BI SW

Reset Button



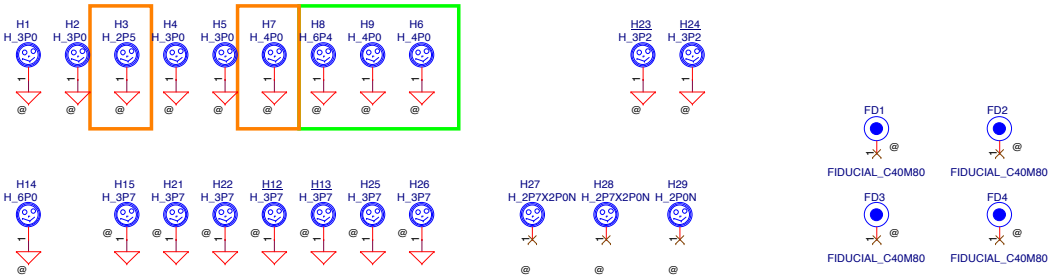


H : 3.8mm

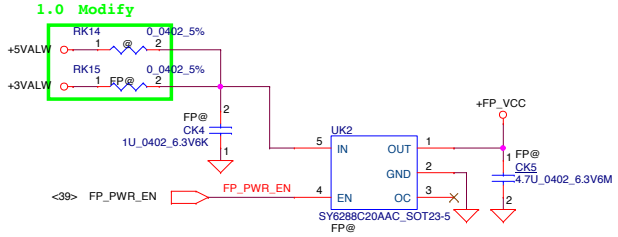
Release : Battery Of
Push : Battery ON

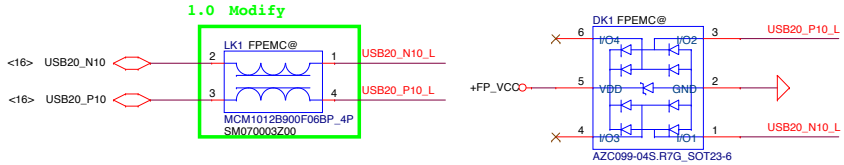
Screw Hole

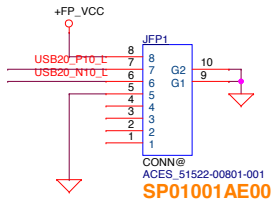
1.A Modify 1.0 Modify



Finger Print







PIN	ETU801	FA577E-1200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: FAN & FP & Screw Hole

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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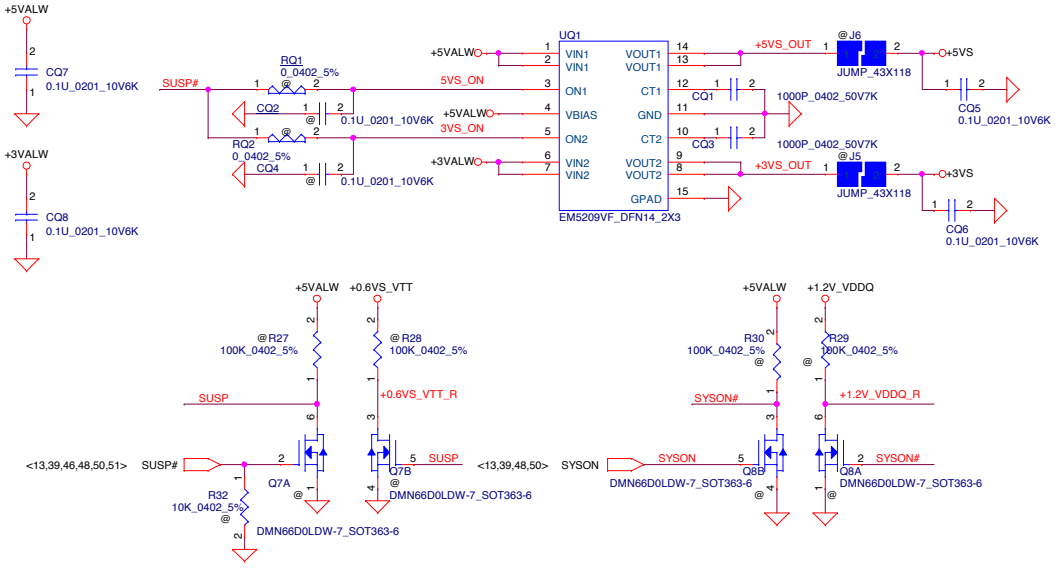
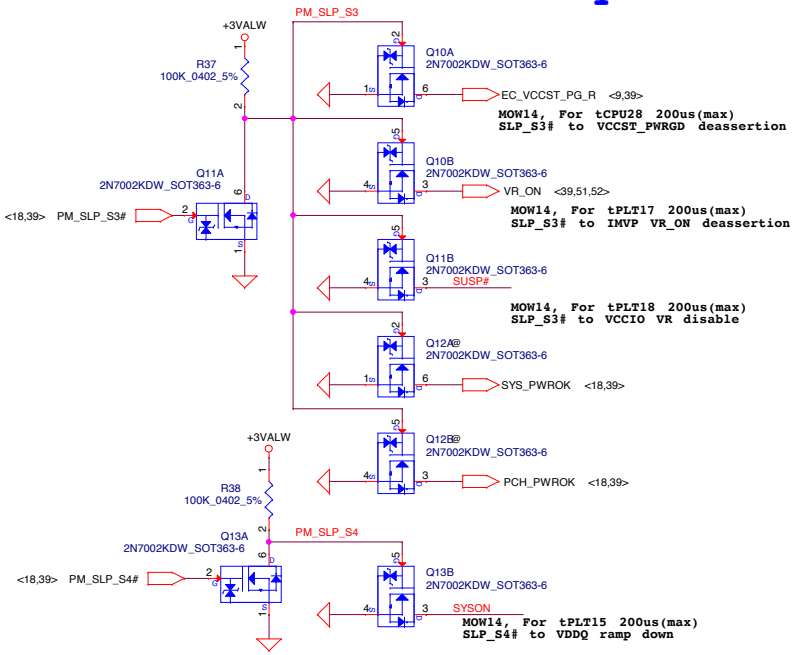
System DC inferface



For Power ON/Off Sequence



Security Classification	Compal Secret Data		
Issued Date	2016/11/03	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: DC Interface

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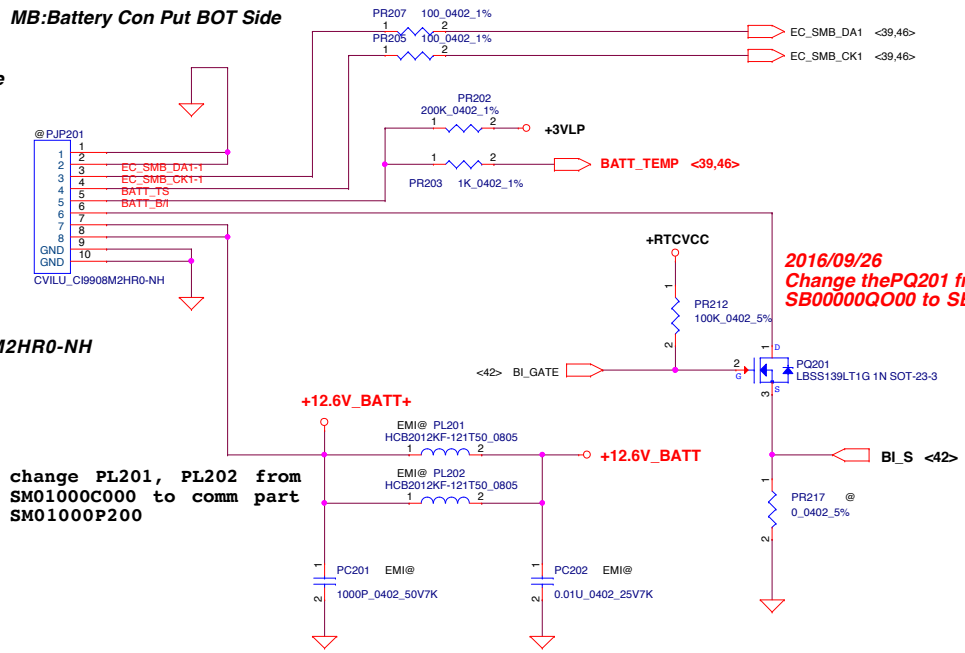
MB:Battery Con Put BOT Side

Battery Bot Side

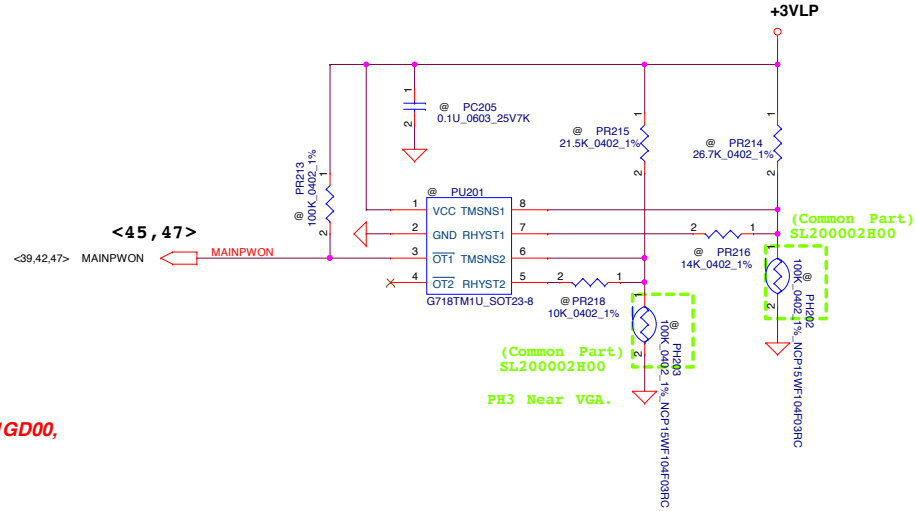
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+
PIN9 GND
PIN10 GND
SP020017H00

CVILU_CI9908M2HR0-NH



2016/09/26
Change thePQ201 from
SB00000QO00 to SB00001GD00,

change PL201, PL202 from SM01000C000 to comm part SM01000P200

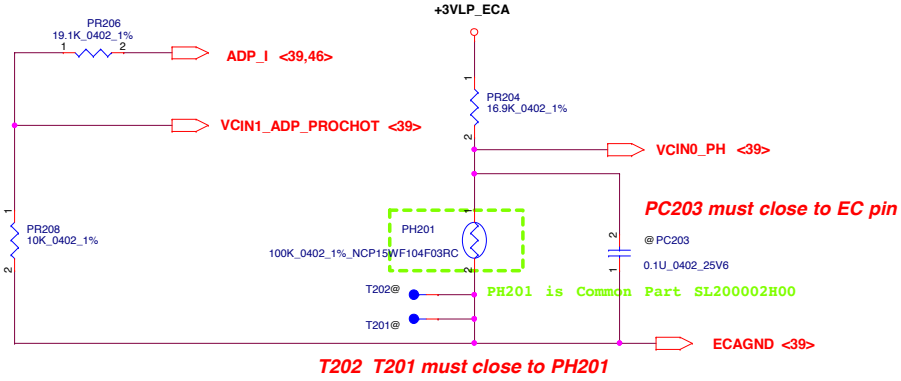


2016/08/16 update

For KB9022 sense 20mΩ	Active	Recovery
135W PR206 19.1K ohm SD034191280	175W,0.63V	175W,0.63V
135W PR206 19.1K ohm SD034191280	175W,0.63V	175W,0.63V

When PR204=16.9K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92'C, 1V	56'C, 2V
PH202(ohm)	7.3092K	26.11K




```
ADP_I=20*I(adapter)*0.01
I(adapter)=adapter(W)*95%/19
```

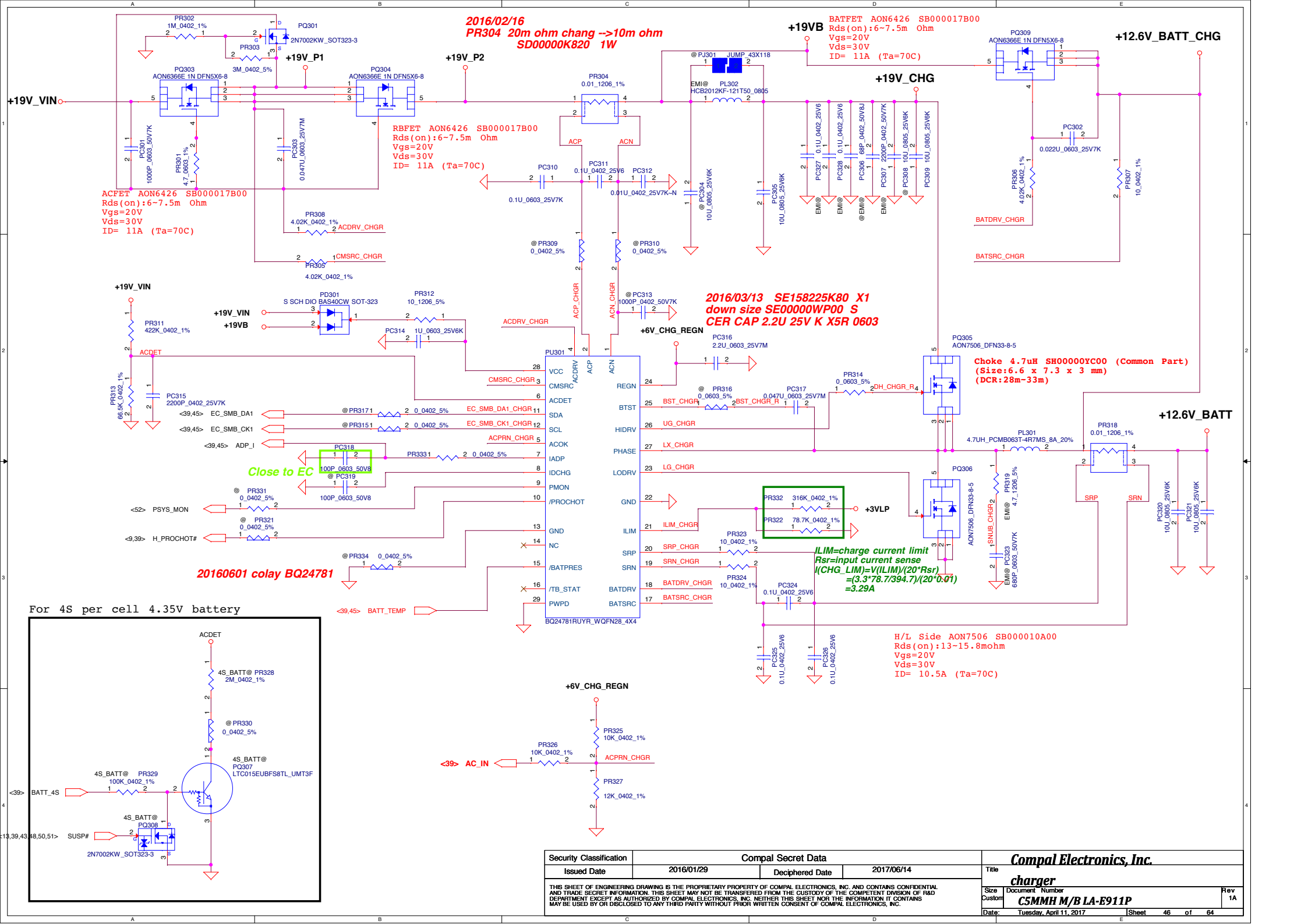
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

Date: Tuesday, April 11, 2017 | Sheet 45 of 64



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.			
Title	charger		
Size	Document Number		Rev
Custom	C5MMH M/B LA-E911P		1A
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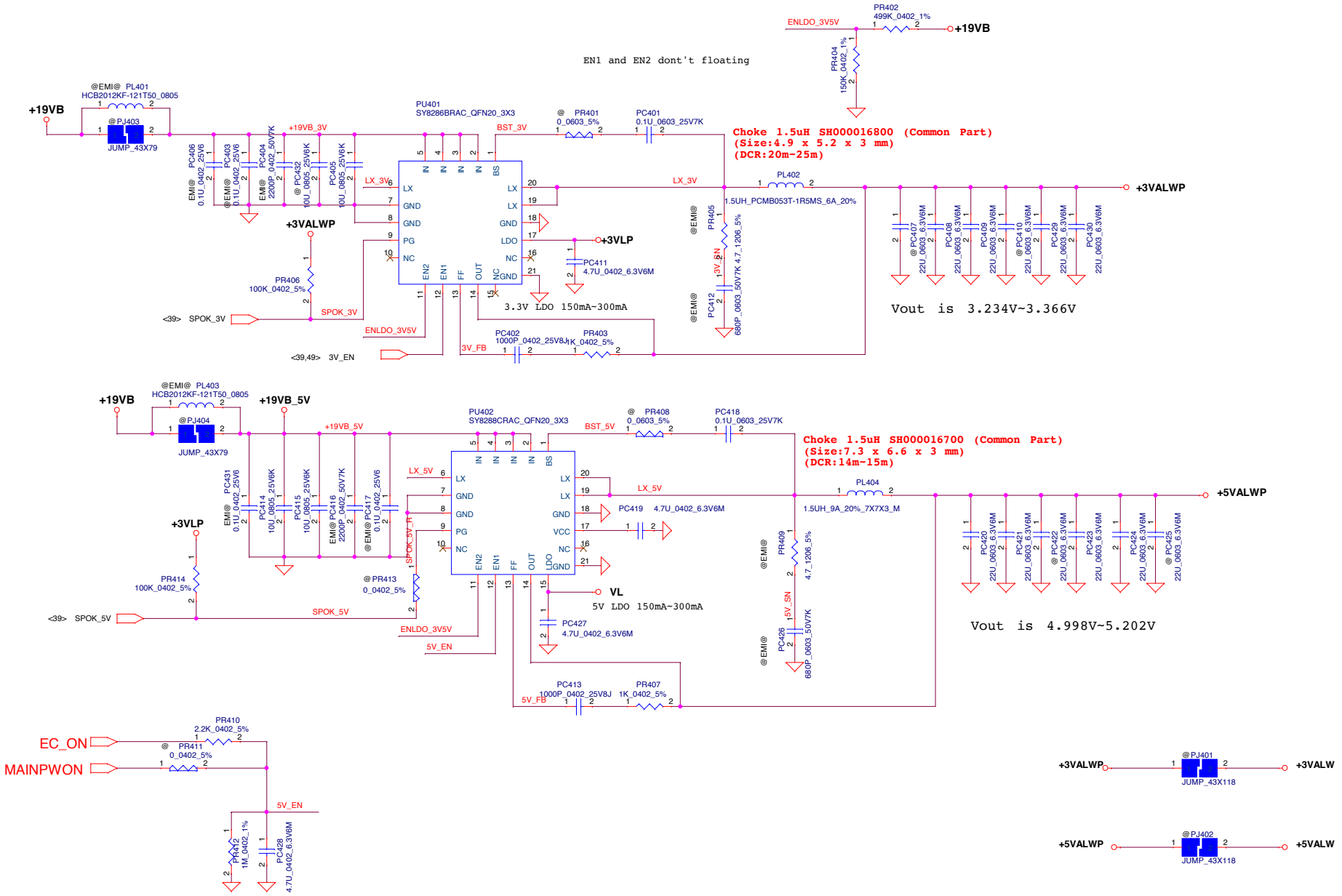


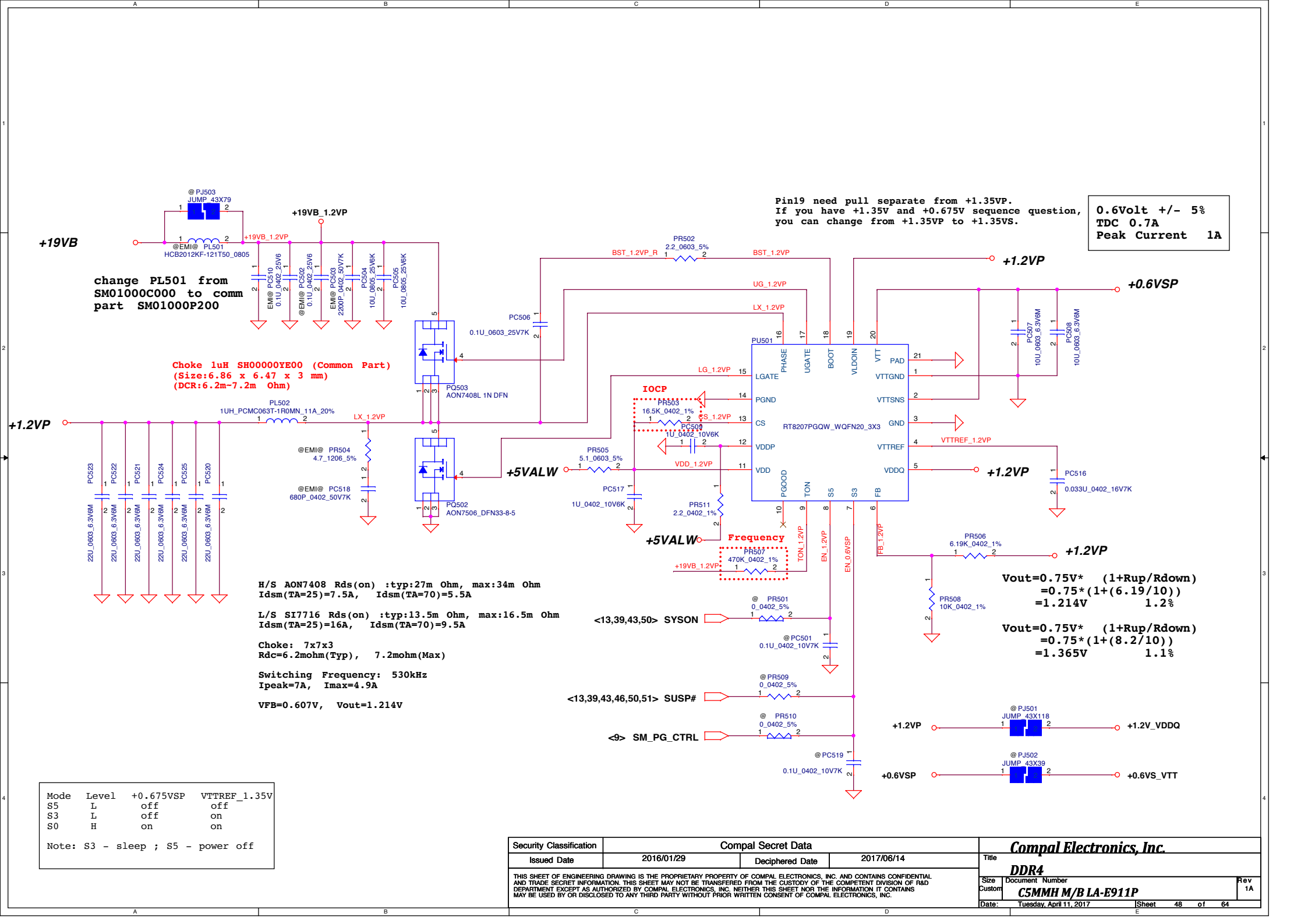
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 3.3VALWP/5VALWP

Size	Document Number	Rev
Custom	C5MMH M/B LA-E911P	1A

Date: Tuesday, April 11, 2017 Sheet 47 of 64



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

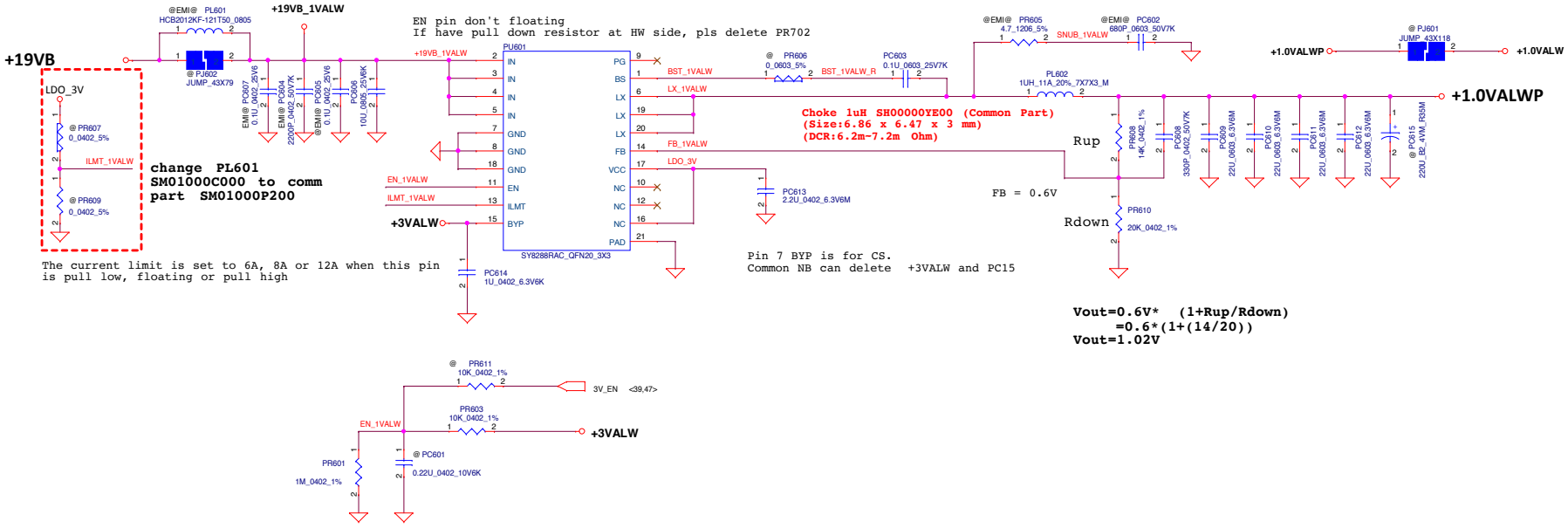
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: DDR4

Size: Custom | Document Number: C5MMH M/B LA-E911P | Rev: 1A

Date: Tuesday, April 11, 2017 | Sheet 48 of 64



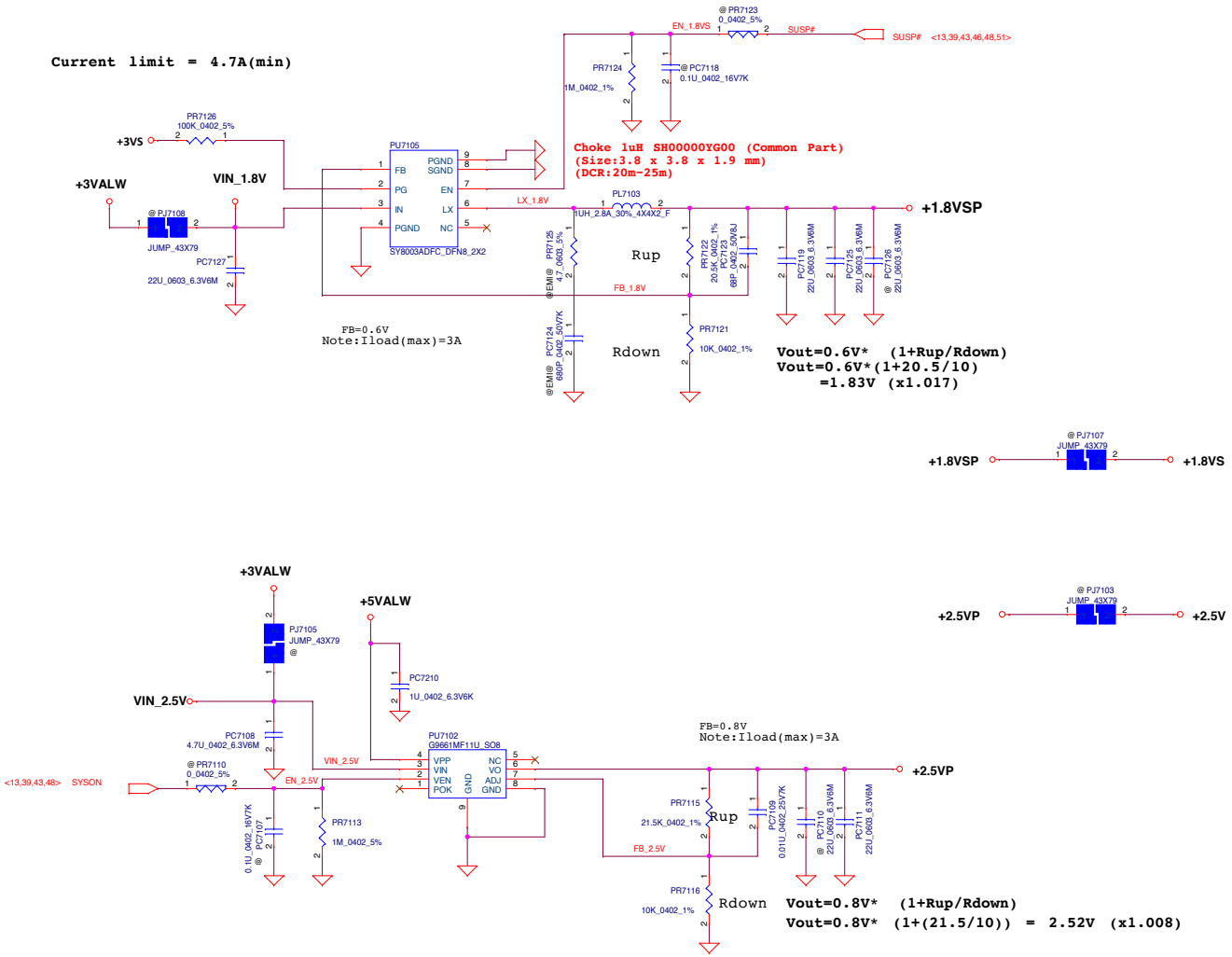
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 1V

Size	Document Number	Rev
C	C5MMH M/B LA-E911P	1A

Date: Tuesday, April 11, 2017 Sheet 49 of 64



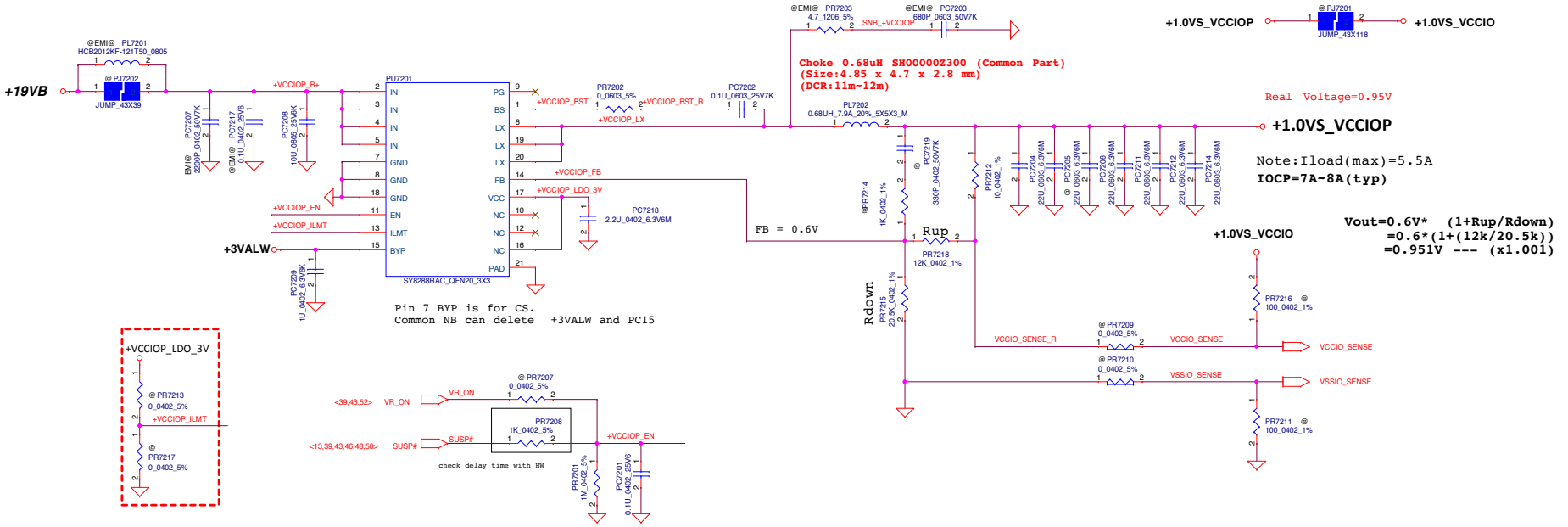
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: 1.5VS/2.5V

Size	Document Number	Rev
C	C5MMH M/B LA-E911P	1A

Date: Tuesday, April 11, 2017 Sheet 50 of 64



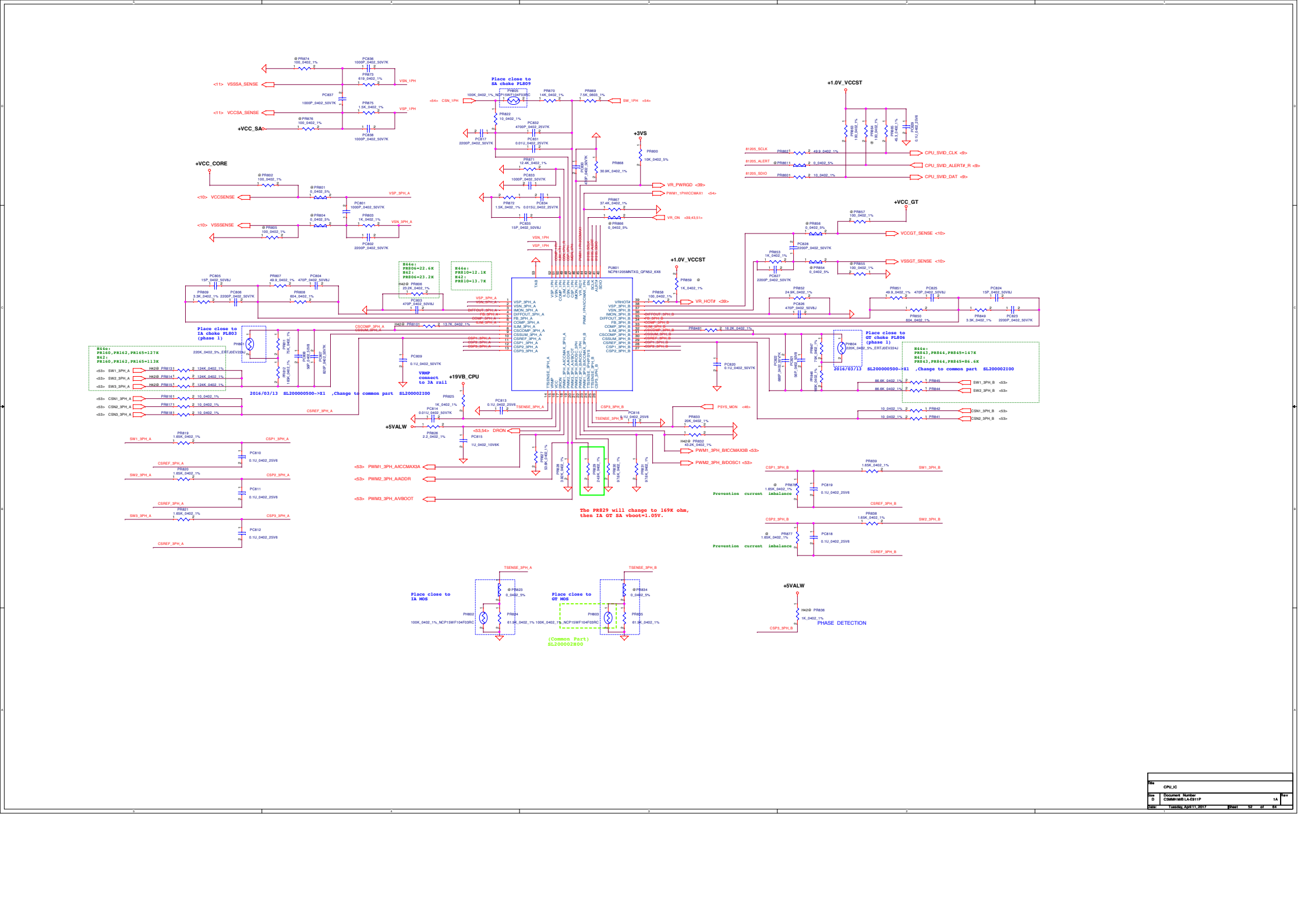
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5MMH M/B LA-E911P

Size: C | Document Number: 1.0VS_VCCIO | Rev: 1A

Date: Tuesday, April 11, 2017 | Sheet 51 of 64


+VCC_SA
+VCC_CORE
+3VS
+1.0V_VCCST
+VCC_GT
+19VB_CPU
+5VALW
PU801
NCP81205MNTXG_QFN52_6X6
Place close to SA choke PL809
Place close to IA choke PL803 (phase 1)
Place close to GT choke PL806 (phase 1)
Place close to IA MOS
Place close to GT MOS
VRHOT# <39>
VR_PWRGD <39>
VR_ON <39,43,51>
PWM1_1PH/ICCMAX1 <54>
PWM1_3PH_B/ICCMAX3B <53>
PWM2_3PH_B/DOSC1 <53>
PWM1_3PH_A/ICCMAX3A <53>
PWM2_3PH_A/ADDR
PWM3_3PH_A/VBOOT
DRON <53,54>
PSYS_MON <46>
CPU_SVID_CLK <9>
CPU_SVID_ALERT#_R <9>
CPU_SVID_DAT <9>
VCCGT_SENSE <10>
VSSGT_SENSE <10>
PHASE DETECTION
The PR829 will change to 169K ohm, then IA GT SA vboot=1.05V.
Prevention current imbalance
Prevention current imbalance
2016/03/13 SL200000500->X1 ,Change to common part SL200002100
2016/03/13 SL200000500->X1 ,Change to common part SL200002100
(Common Part) SL200002H00
VRMP connect to 3A rail
H44e: PR806=22.6K H42: PR806=23.2K
H44e: PR810=12.1K H42: PR810=13.7K
H44e: PR160,PR162,PR165=127K H42: PR160,PR162,PR165=113K
H44e: PR843,PR844,PR845=147K H42: PR843,PR844,PR845=86.6K
CPU_IC
Document Number CSMMIMB LA-E911P
Rev 1A
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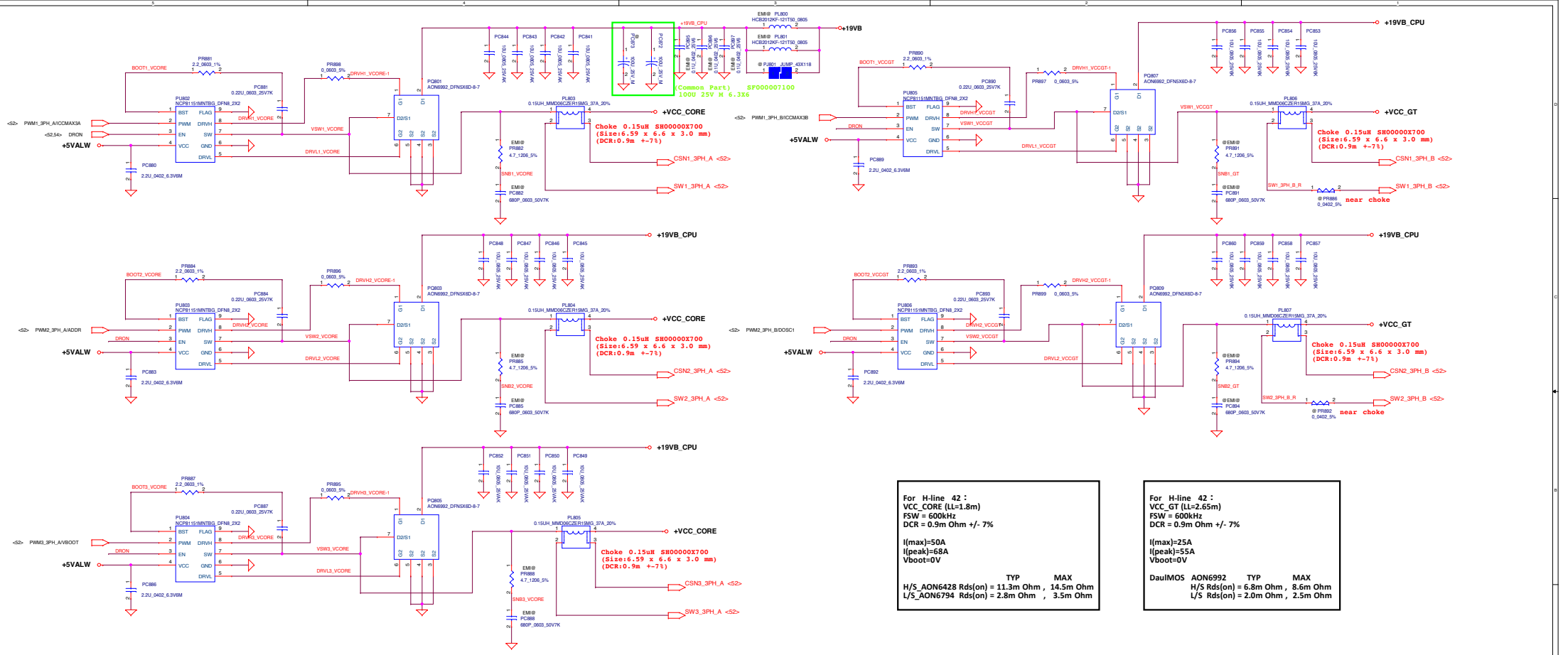
+19VB
+19VB_CPU
+VCC_CORE
+VCC_GT
+5VALW
Choke 0.15uH SH00000X700 (Size:6.59 x 6.6 x 3.0 mm) (DCR:0.9m +-7%)
near choke
(Common Part) SP000007100 100u 25V M 6.3X6
PWM1_3PH_A/CCMAX3A
PWM1_3PH_B/CCMAX3B
PWM2_3PH_A/ADDR
PWM2_3PH_B/DOSC1
PWM3_3PH_A/VBOOT
DRON
CSN1_3PH_A
SW1_3PH_A
CSN1_3PH_B
SW1_3PH_B
CSN2_3PH_A
SW2_3PH_A
CSN2_3PH_B
SW2_3PH_B
CSN3_3PH_A
SW3_3PH_A
VCC_CORE (LL=1.8m)
FSW = 600kHz
DCR = 0.9m Ohm +/- 7%
I(max)=50A
I(peak)=68A
Vboot=0V
TYP MAX
H/S_AON6428 Rds(on) = 11.3m Ohm , 14.5m Ohm
L/S_AON6794 Rds(on) = 2.8m Ohm , 3.5m Ohm
VCC_GT (LL=2.65m)
FSW = 600kHz
DCR = 0.9m Ohm +/- 7%
I(max)=25A
I(peak)=55A
Vboot=0V
DaulMOS AON6992 TYP MAX
H/S Rds(on) = 6.8m Ohm , 8.6m Ohm
L/S Rds(on) = 2.0m Ohm , 2.5m Ohm
Function Field :
Drivers - 36.2
Rest of support elements - 36.3
Acoustic Noise B+ Bulk CAP - 37.2
Security Classification
Compal Secret Data
Issued Date
2016/01/29
Deciphered Date
2017/06/14
Compal Electronics, Inc.
C5MMH M/B LA-E911P
VCC/VCCGT
Rev 1A
Tuesday, April 11, 2017
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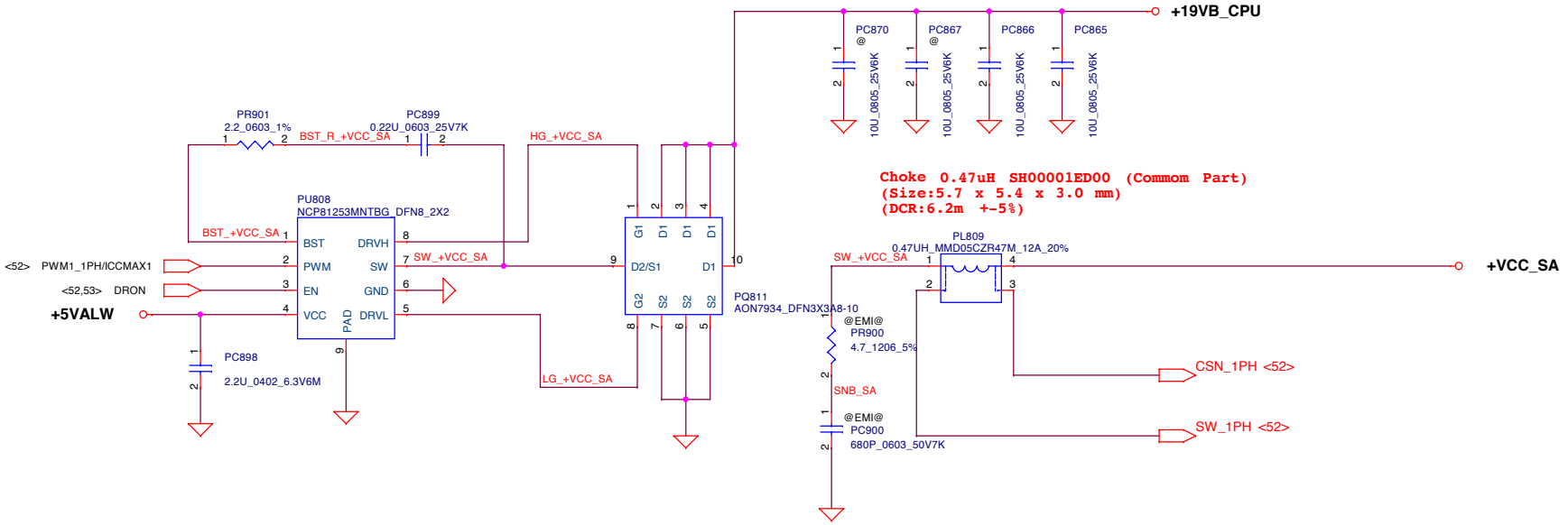

For H-line 42 :
VCC_SA (LL=10m)
FSW = 600kHz
DCR = 6.2m Ohm +/- 5%

I(max)=10A
I(peak)=12A
Vboot=1.05V

DaulMOS	AON7934	TYP	MAX
	H/S Rds(on) =	12.4m Ohm ,	15.8m Ohm
	L/S Rds(on) =	9.1m Ohm ,	11.6m Ohm

Function Field :
Drivers - 36.2
Rest of support elements - 36.3

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5MMH M/B LA-E911P

Size: Custom | Document Number: VCCSA | Rev: 1A

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Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: C5MMH M/B LA-E911P

Size: Custom | Document Number: CPU CAP | Rev: 1A

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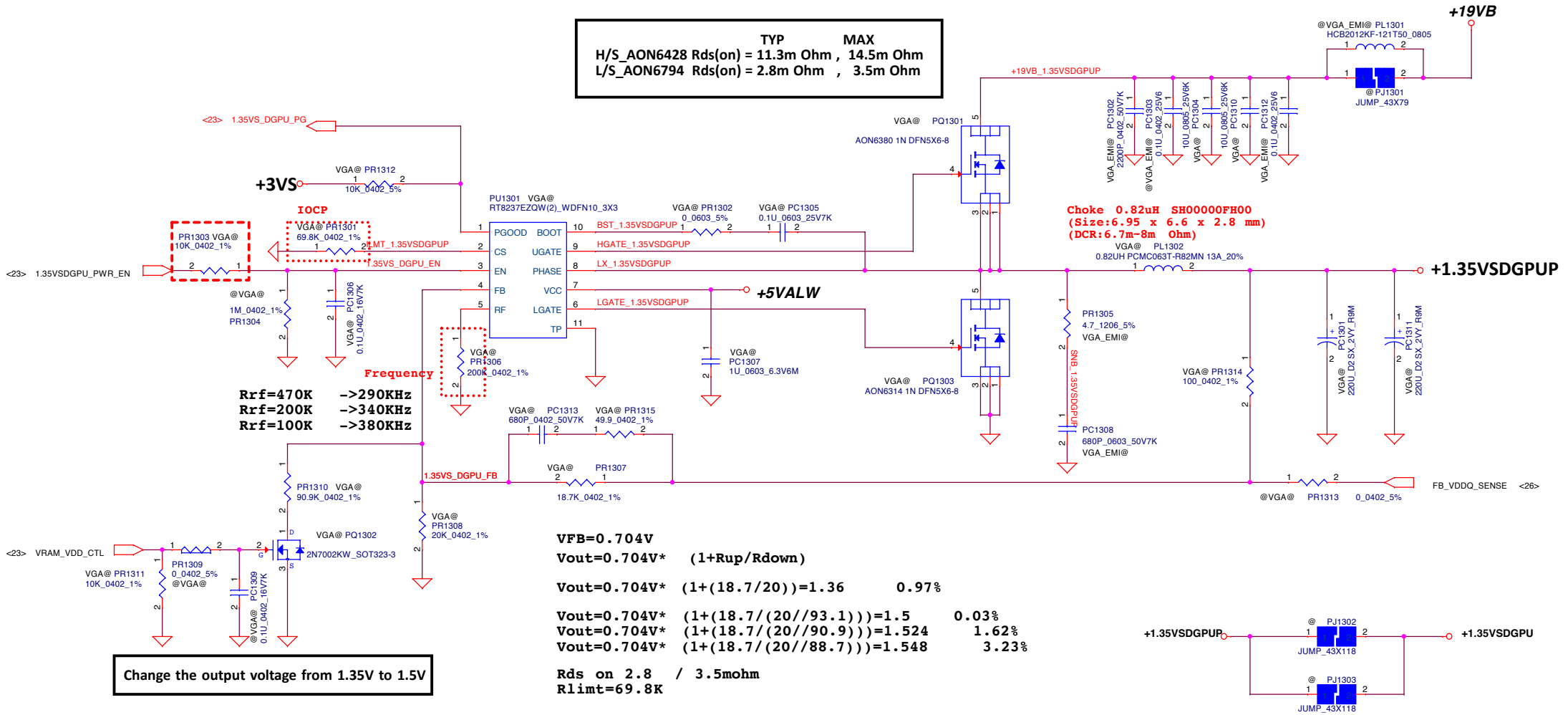

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VRAM

Size: A3 | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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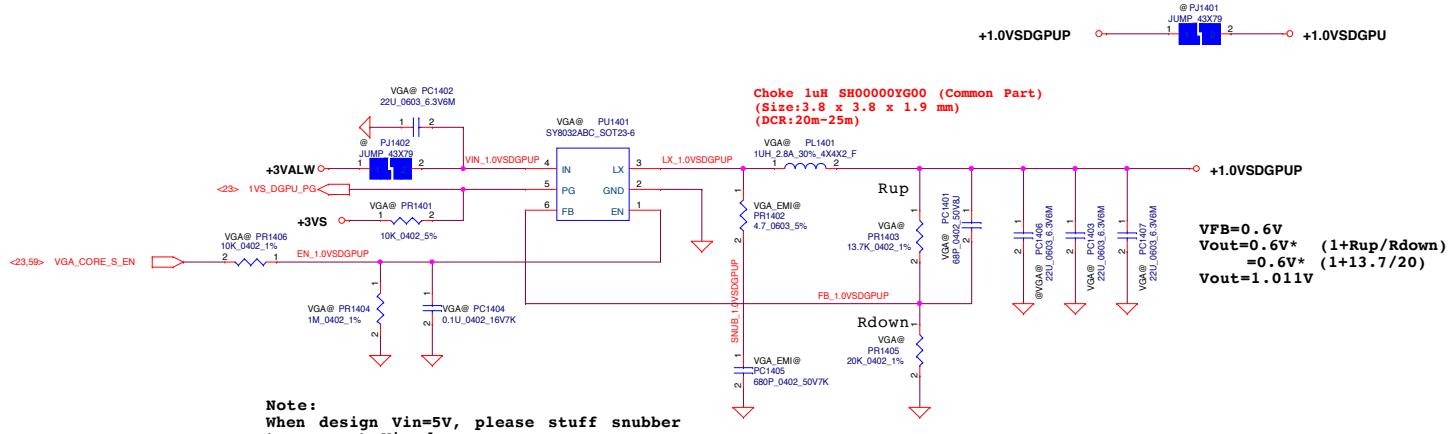

Compal Electronics, Inc.

Title: 1.05VSDGPU

Size	Document Number	Rev
C	C5MMH M/B LA-E911P	1A

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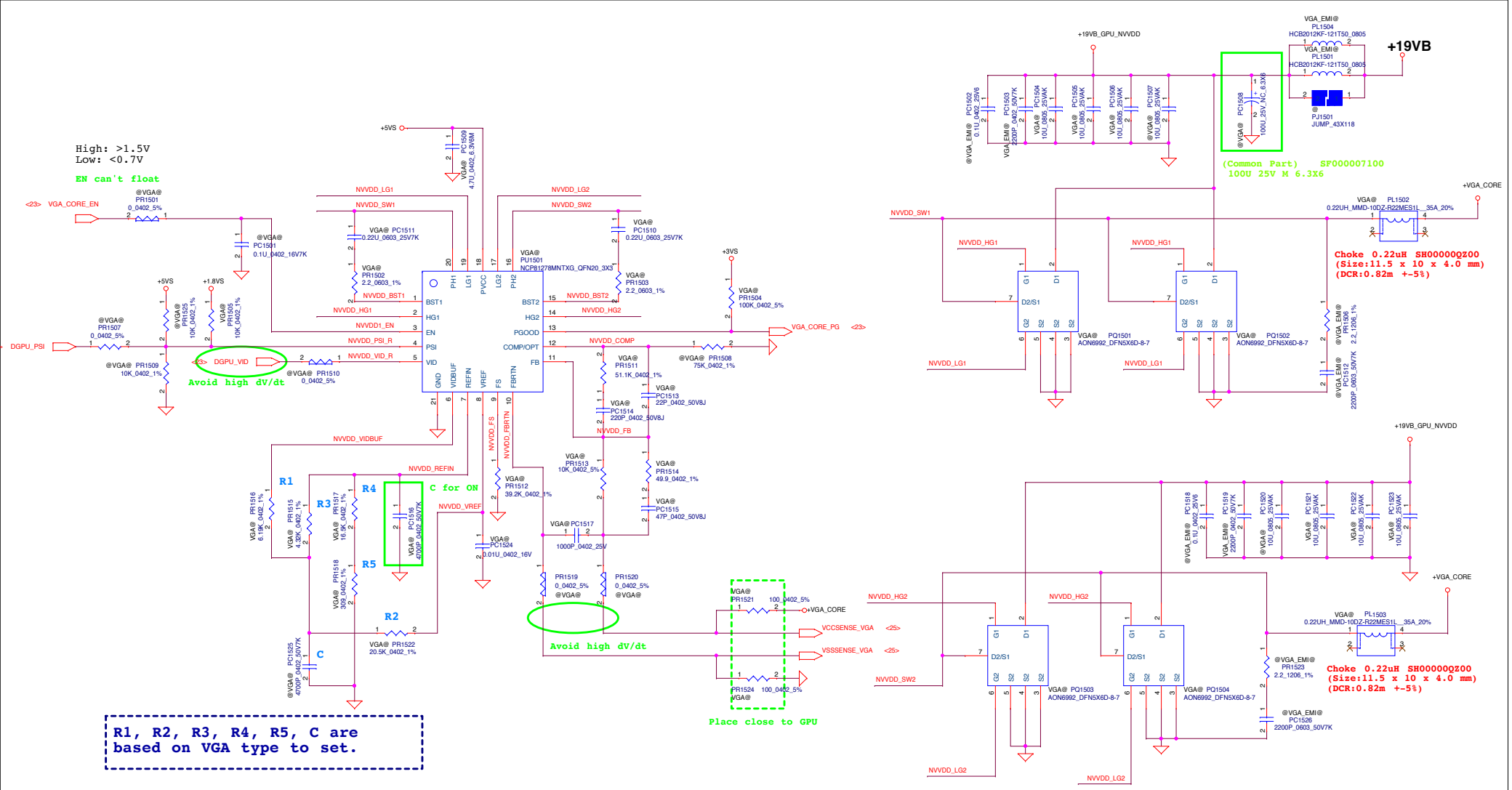

For N17P-G1 -30 W [N17P-GC-4-0M]
VGA_CORE (NVVDD)
FSW = 450kHz
DCR = 0.82m Ohm +/- 5%

TDC=45A
I(max)=106A
Vboot=0.8V

DaulMOS AON6992	TYP	MAX
H/S Rds(on) =	6.8m Ohm ,	8.6m Ohm
L/S Rds(on) =	2.0m Ohm ,	2.5m Ohm

Please base on GPU spec to calculate.

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VGA_CORE

Size | Document Number: C5MMH M/B LA-E911P | Rev: 1A

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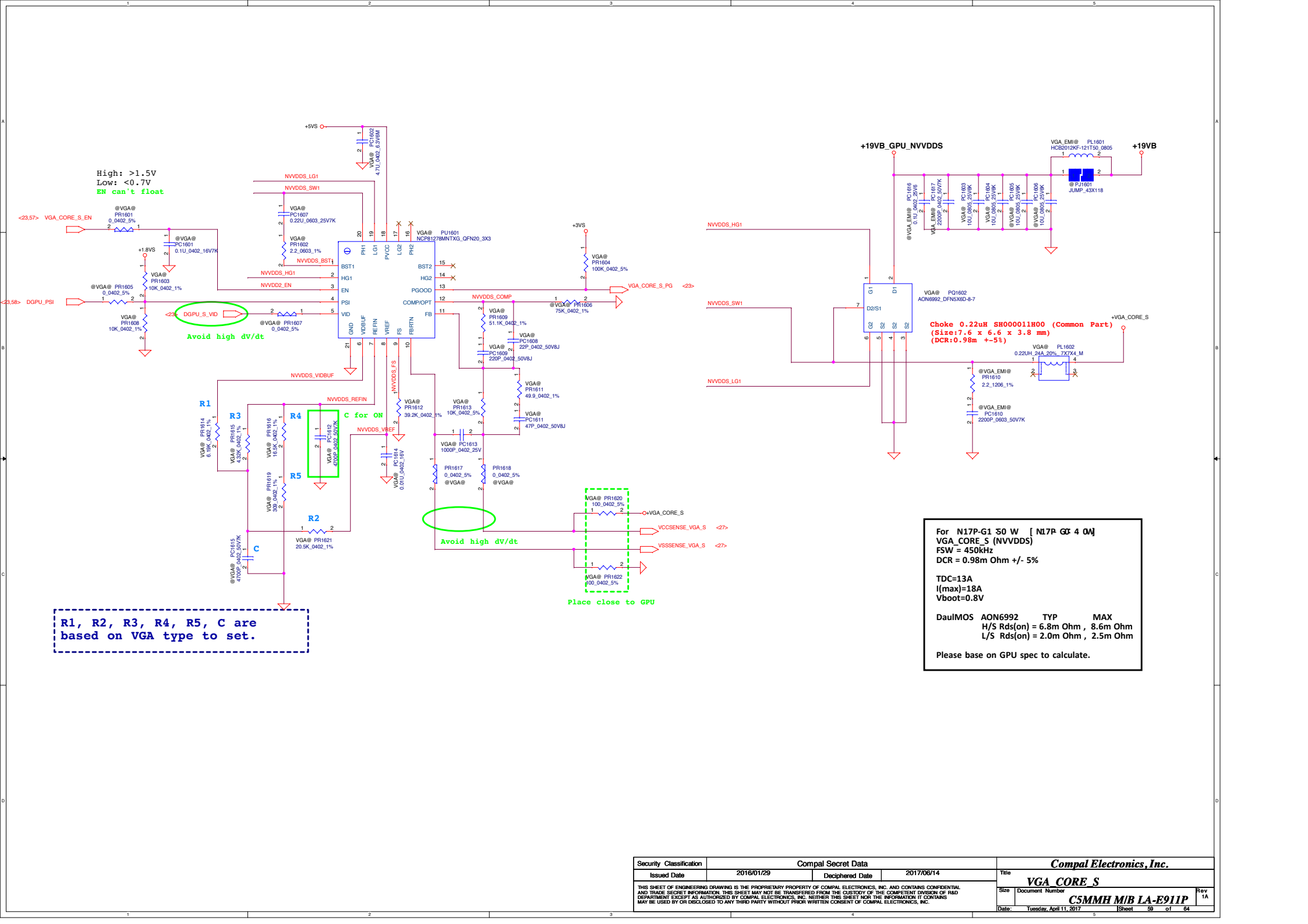

For N17P-G1 :50 W [N17P-G0: 4 0W]
VGA_CORE_S (NVVDDS)
FSW = 450kHz
DCR = 0.98m Ohm +/- 5%

TDC=13A
I(max)=18A
Vboot=0.8V

DaulMOS	AON6992	TYP	MAX
	H/S Rds(on) =	6.8m Ohm ,	8.6m Ohm
	L/S Rds(on) =	2.0m Ohm ,	2.5m Ohm

Please base on GPU spec to calculate.

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/06/14

Compal Electronics, Inc.

Title: VGA_CORE_S

Size	Document Number	Rev
	C5MMH M/B LA-E911P	1A

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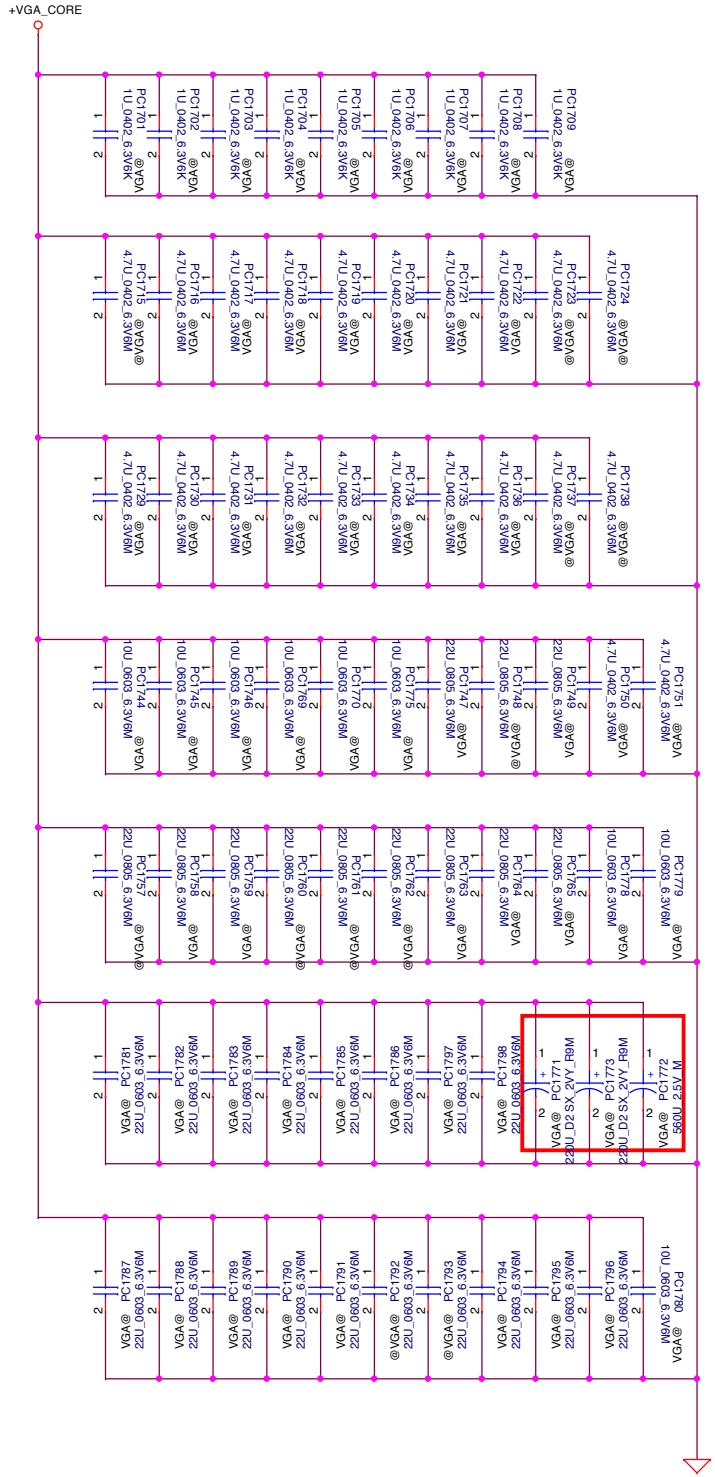
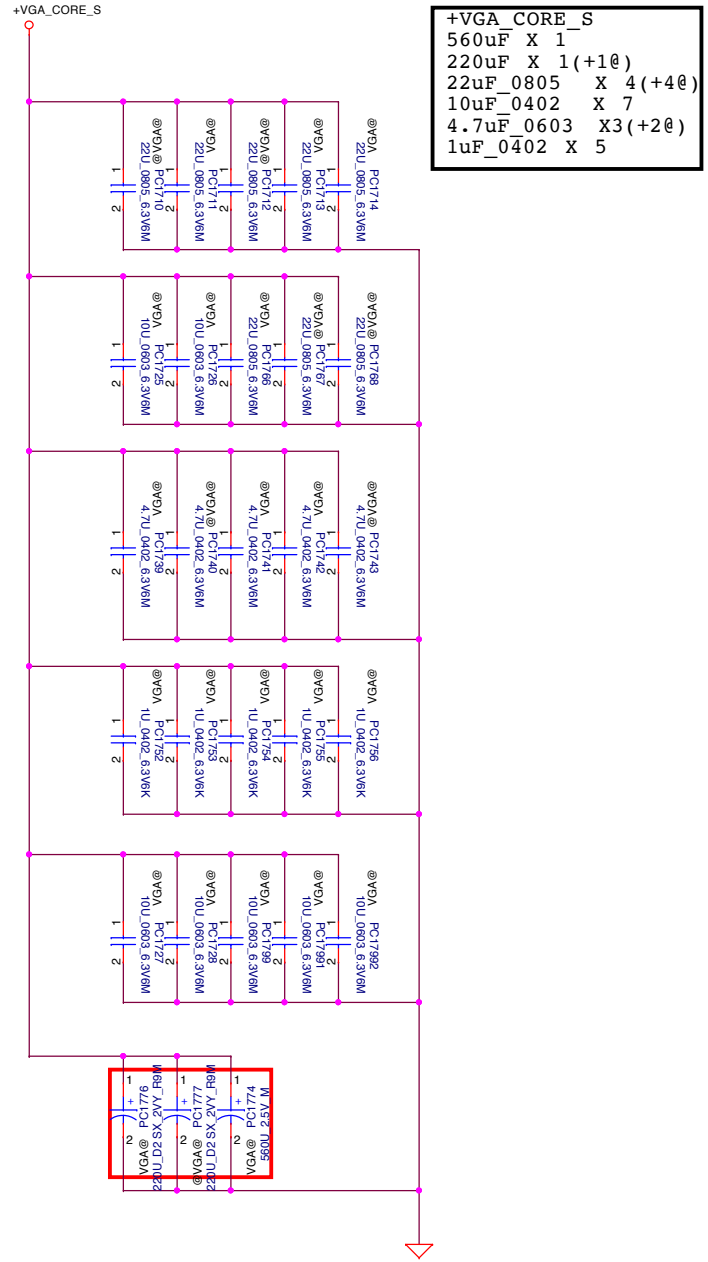



```
+VGA_CORE
560uF X 1
220uF X 2
22uF_0805 X 7(+5@)
22uF_0603 X 16(+2@)
10uF_0603X 9
4.7uF_0402 X 17(+5@)
1uF_0402 X 9
```




```
+VGA_CORE_S
560uF X 1
220uF X 1(+1@)
22uF_0805 X 4(+4@)
10uF_0402 X 7
4.7uF_0603 X3(+2@)
1uF_0402 X 5
```


Compal Electronics, Inc.

Title: VGA DECOUPLING

Size | Document Number | Rev: C5MMH M/B LA-E911P | 1A

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