Keystone 13.3" Schematics
Skylake-U / Kabylake-U

2016-11-22
REV : A00

DY : None Installed
WWAN: WWAN only Installed
NON WWAN: NON WWAN Installed
DS3: Support DS3 Installed
NON DS3: NON DS3 only Installed

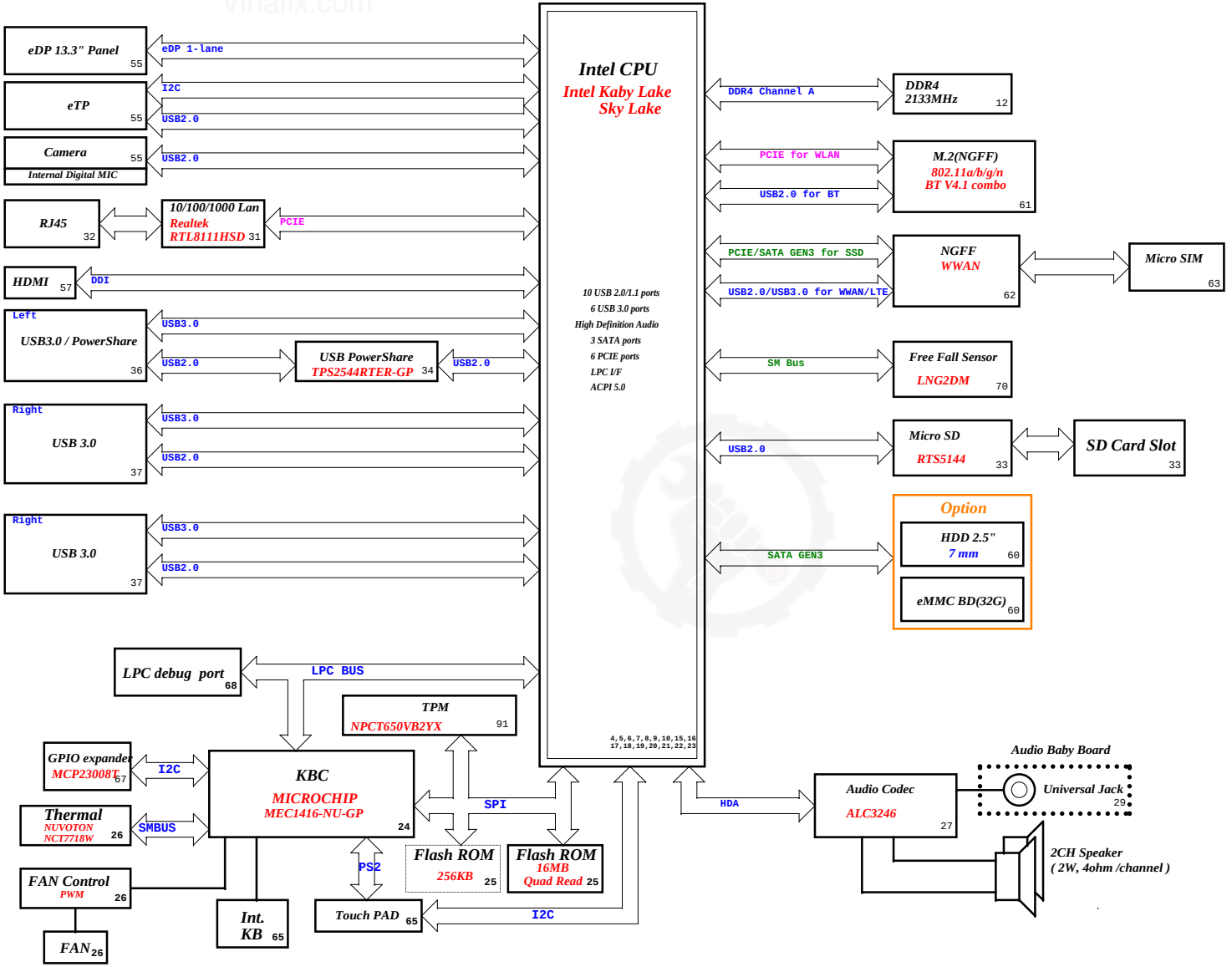
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A4	Document Number: Keystone 13.3"	Rev: X00
Date: Wednesday, November 23, 2016	Sheet 1 of 106	

Project code: 4PD0AW010001 (KBL)
Project code: 4PD0BH010001 (SKL)
PCB P/N: 16824
Revision: A00

Keystone 13.3" Block Diagram



CHARGER
BQ24786RUYR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC
RT6575DGQW 45

INPUTS	OUTPUTS
DCBATOUT	PWR_5V 5V_S5 5V_AUX_S5

CPU Core Power
NCP81218MNTXG
NCP81381MNTXG
NCP81381MNTXG
NCP81253MNTBG 46~50

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCSA

DDR4
RT8231AGQW 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0

CPU DCDC-V1D00A
AOZ2261QI-10 52

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V
RT9025-25ZSP-2-GP 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

LDO-V2D5V
RT9025-25ZSP-2-GP 54

INPUTS	OUTPUTS
3D3V_S5	2D5V_S3

5V/3V S0
G5016KD1U 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG
APE8939GN3-GP 40

INPUTS	OUTPUTS
1D0V_S5	+VCCSTG

VCCST
APE8939GN3-GP 40

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU

SYSTEM DC/DC
RT6575DGQW 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A2 | Document Number: Keystone 13.3" | Rev: X00
Date: Wednesday, November 23, 2016 | Sheet 2 of 106

Main Func = CPU

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 3 of 106

Main Func = CPU

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

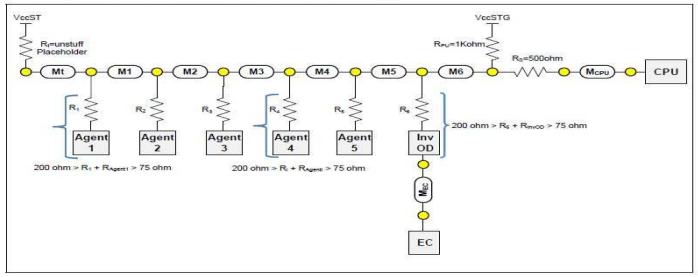
Add resistor by NON DS3 function

Merge R414,R415 to RN402 20160623(DVT1)

modify 20160628(DVT1)

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

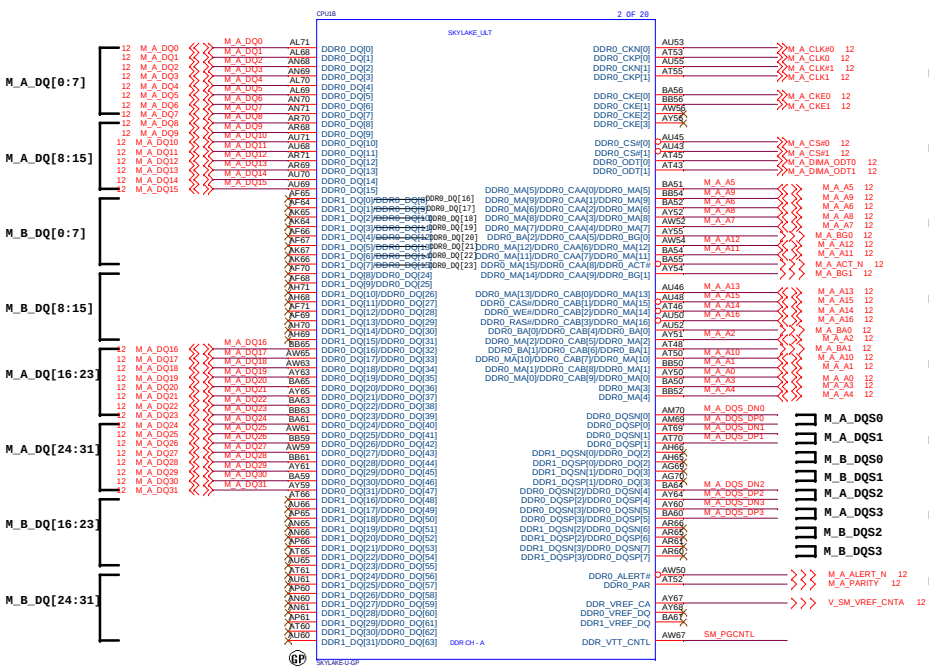
Title: CPU_(JTAG/CPU SIDE BAND)

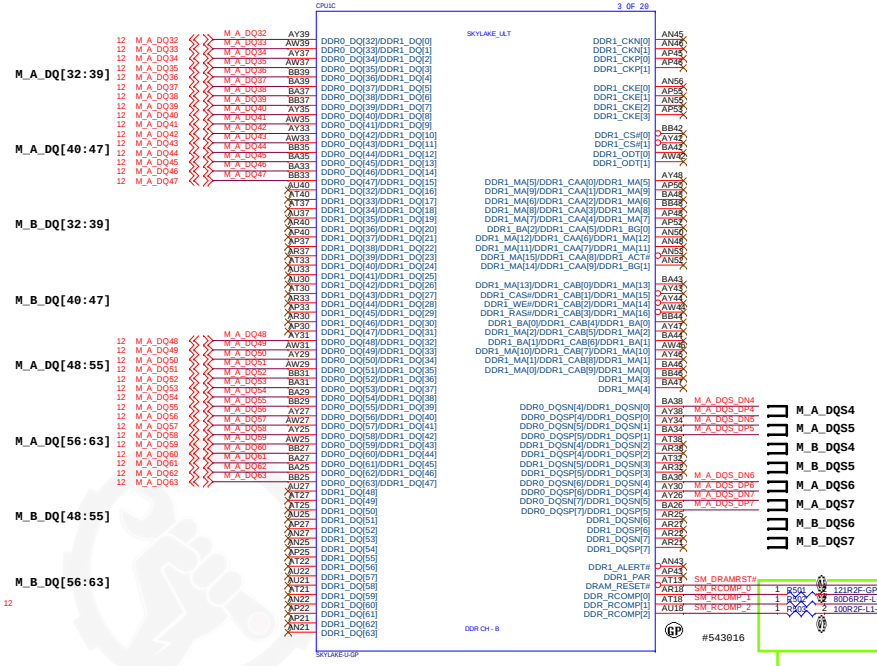
Size: A3 | Document Number: Keystone 13.3" | Rev: X00

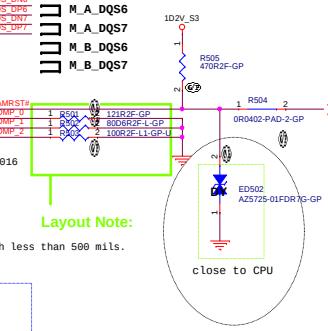
Date: Wednesday, November 23, 2016 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type: Interleaved Type







Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

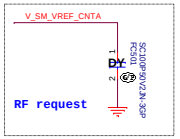
PDG: DDR/ODT

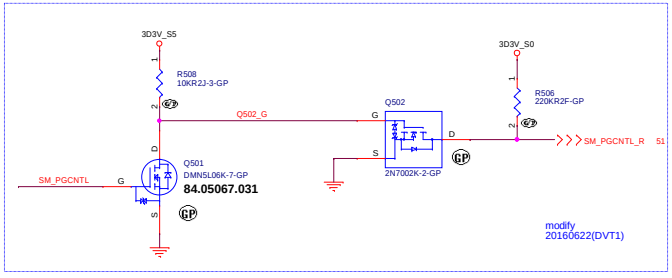
4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

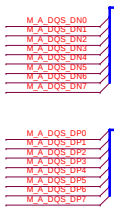
Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.







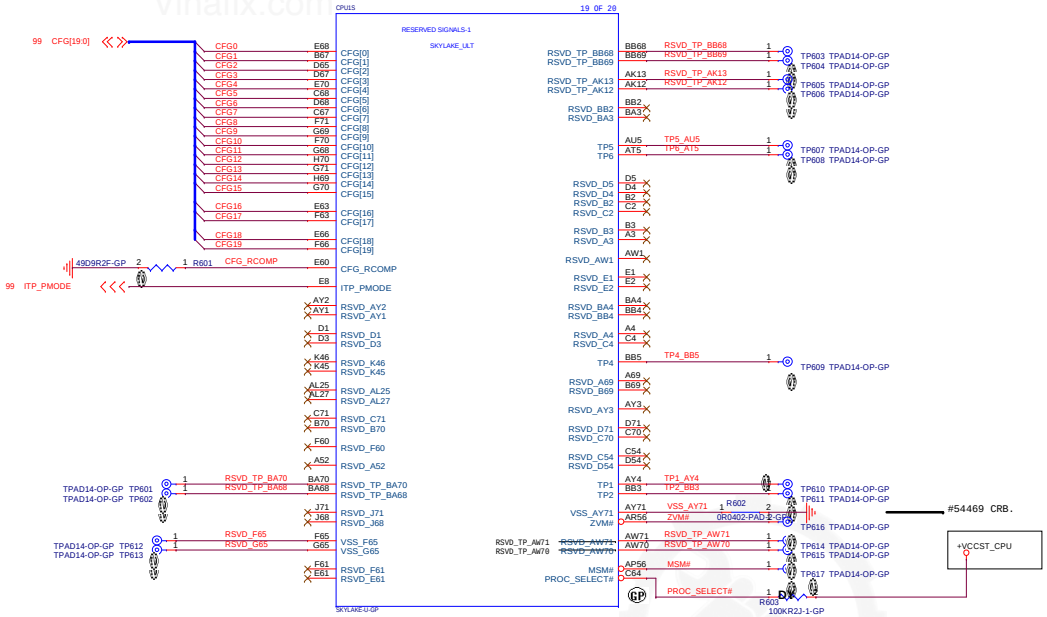
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

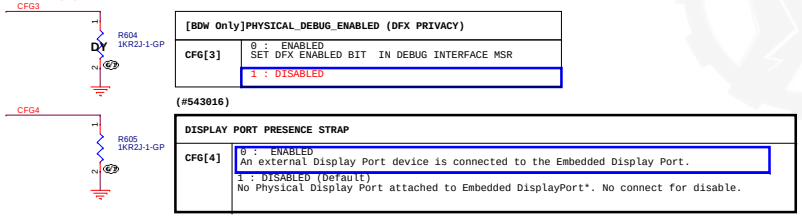
Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 5 of 106

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

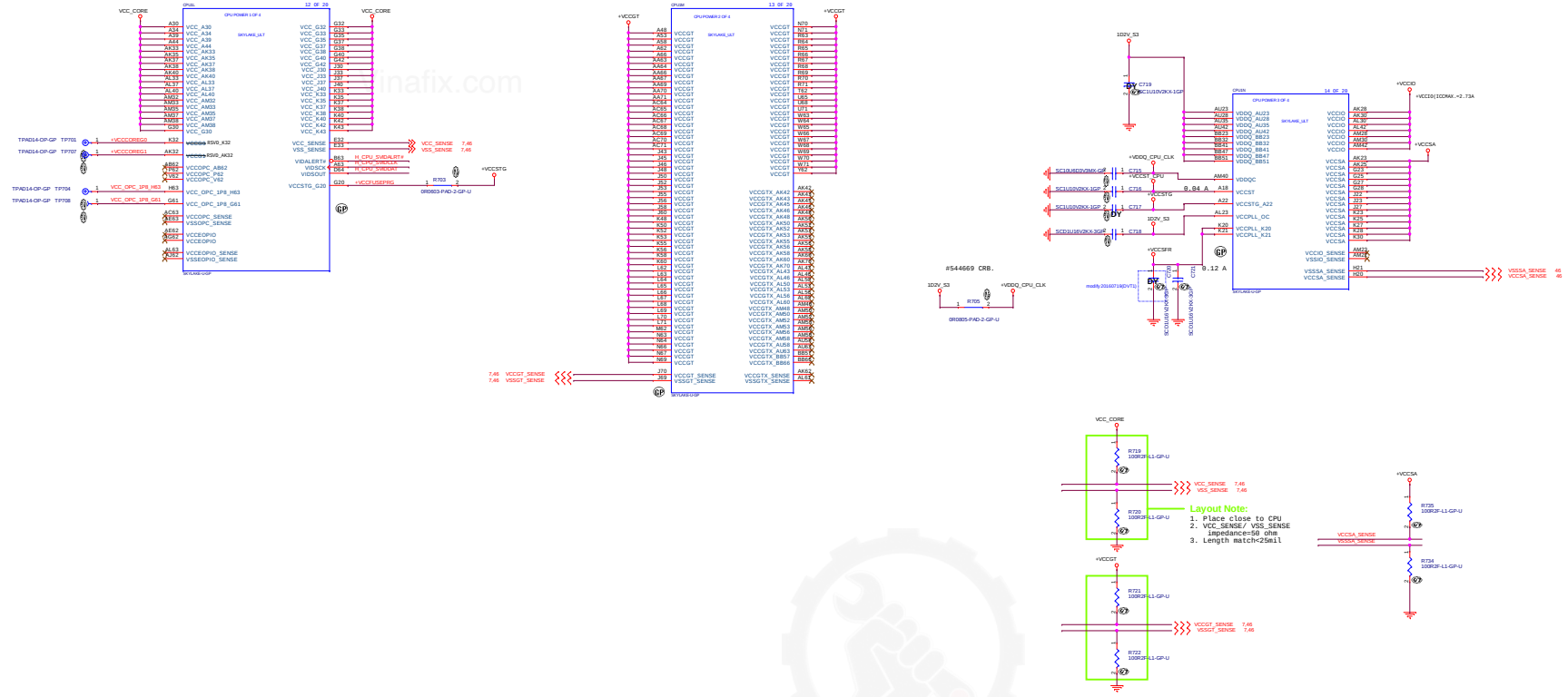
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RESERVED)

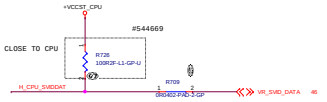
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 6 of 106

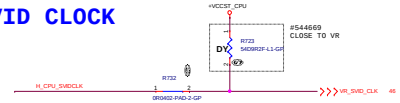


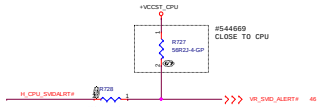
SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK





SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

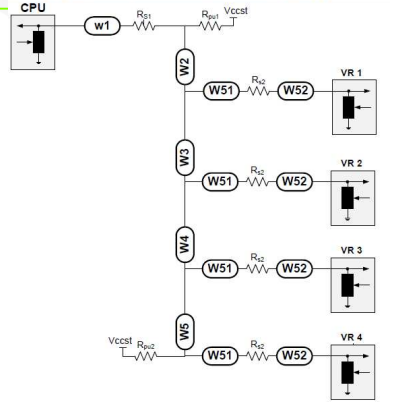
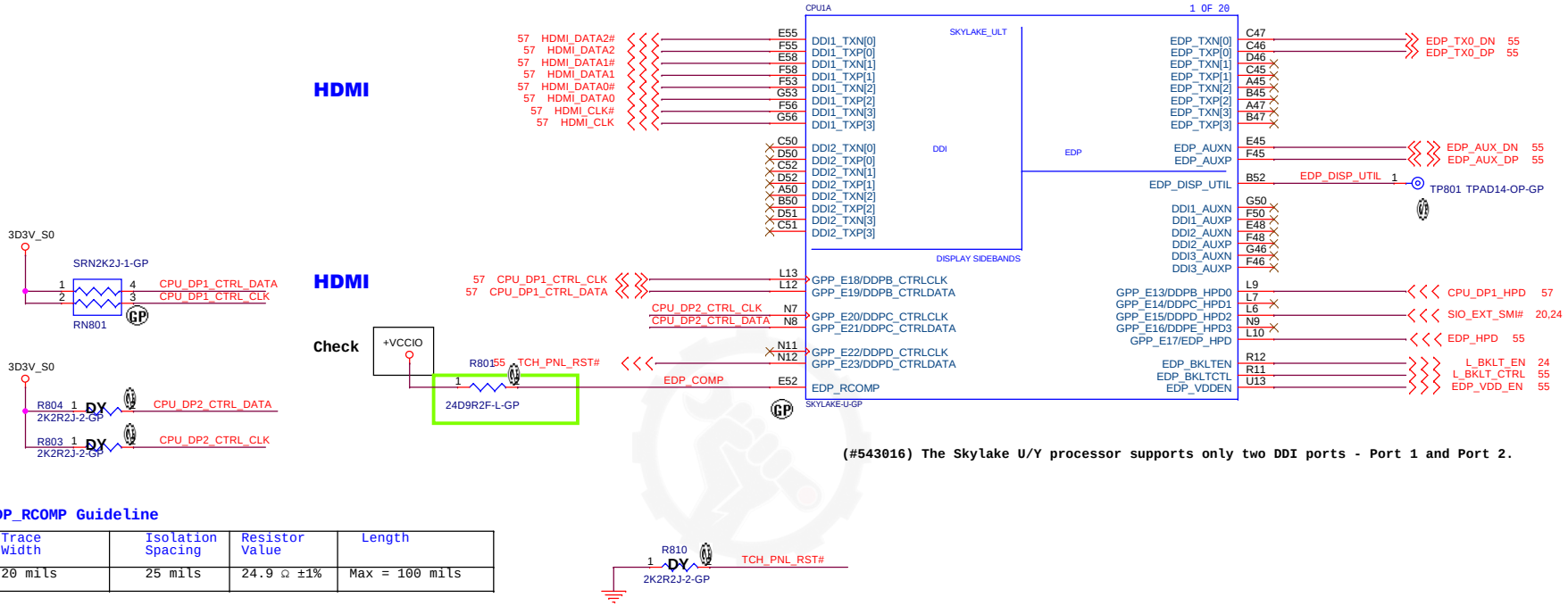


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCCpr [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Main Func = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

SIO_EXT_SM# PU move to RN2013
20160628(DVT1)

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DISPLAY)
Size: A3
Document Number: Keystone 13.3"
Rev: X00
Date: Wednesday, November 23, 2016
Sheet 8 of 106

Main Func = CPU

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Keystone 13.3"* | Rev: *X00*

Date: Wednesday, November 23, 2016 | Sheet 9 of 106

Main Func = CPU

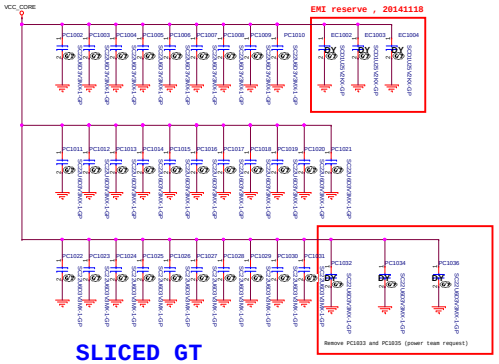
(#543016 PDG)

20140814 DAVID

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

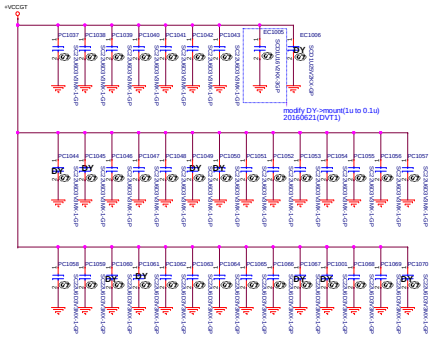
22U 0603 x 35(5 DY)



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

22U 0603 x35 (5 DY)



VCCSA

22U 0603 x13 (4 DY)

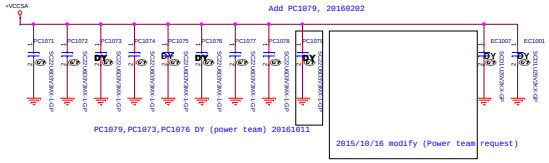


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

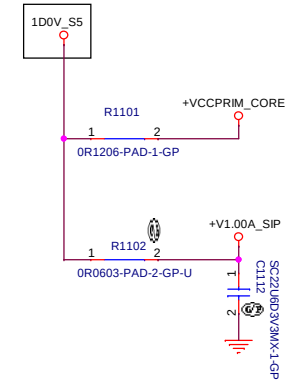
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

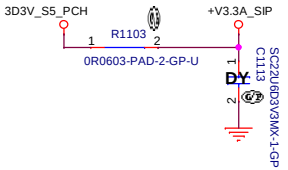
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

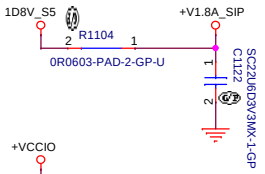
Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

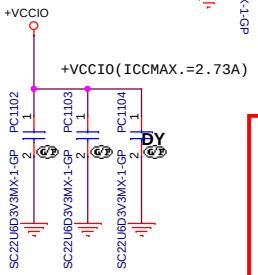
Main Func = CPU

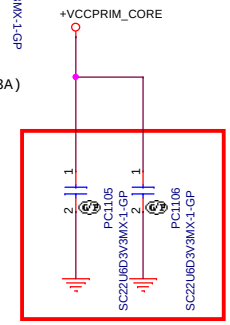
PCH DERIVED RAILS



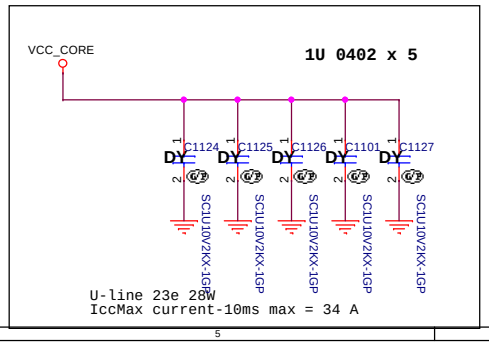


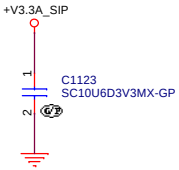




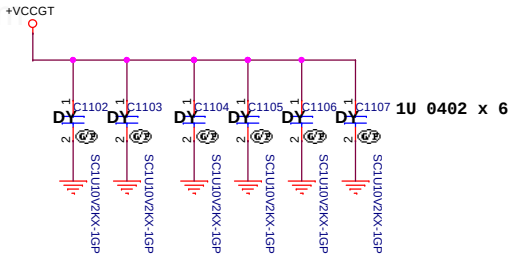


Size:0805 change to 0603
20141117

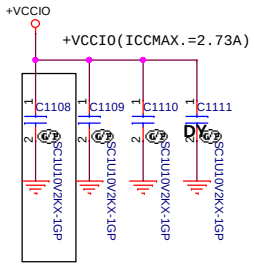




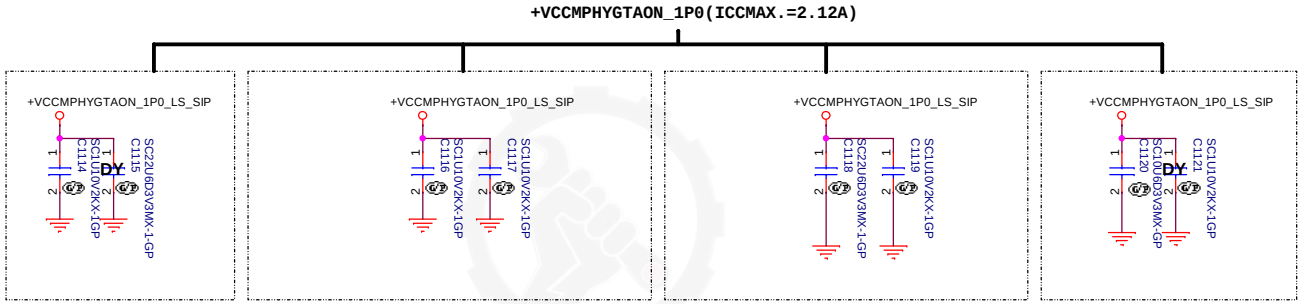
UNSLICED GT



VCCIO



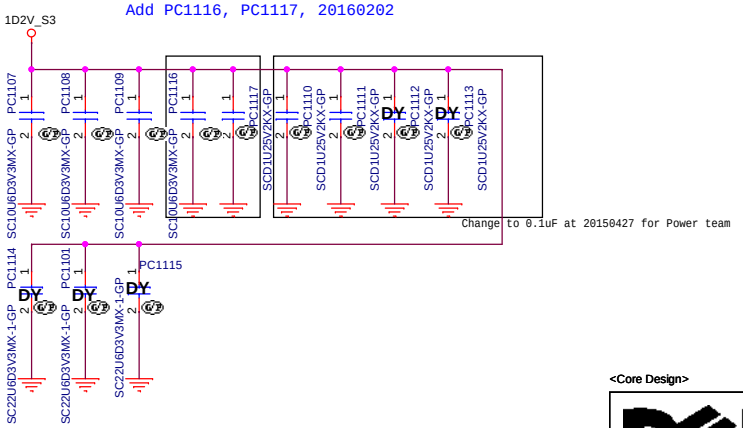
C1108 remove DY, 20160202



Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

Add PC1116, PC1117, 20160202



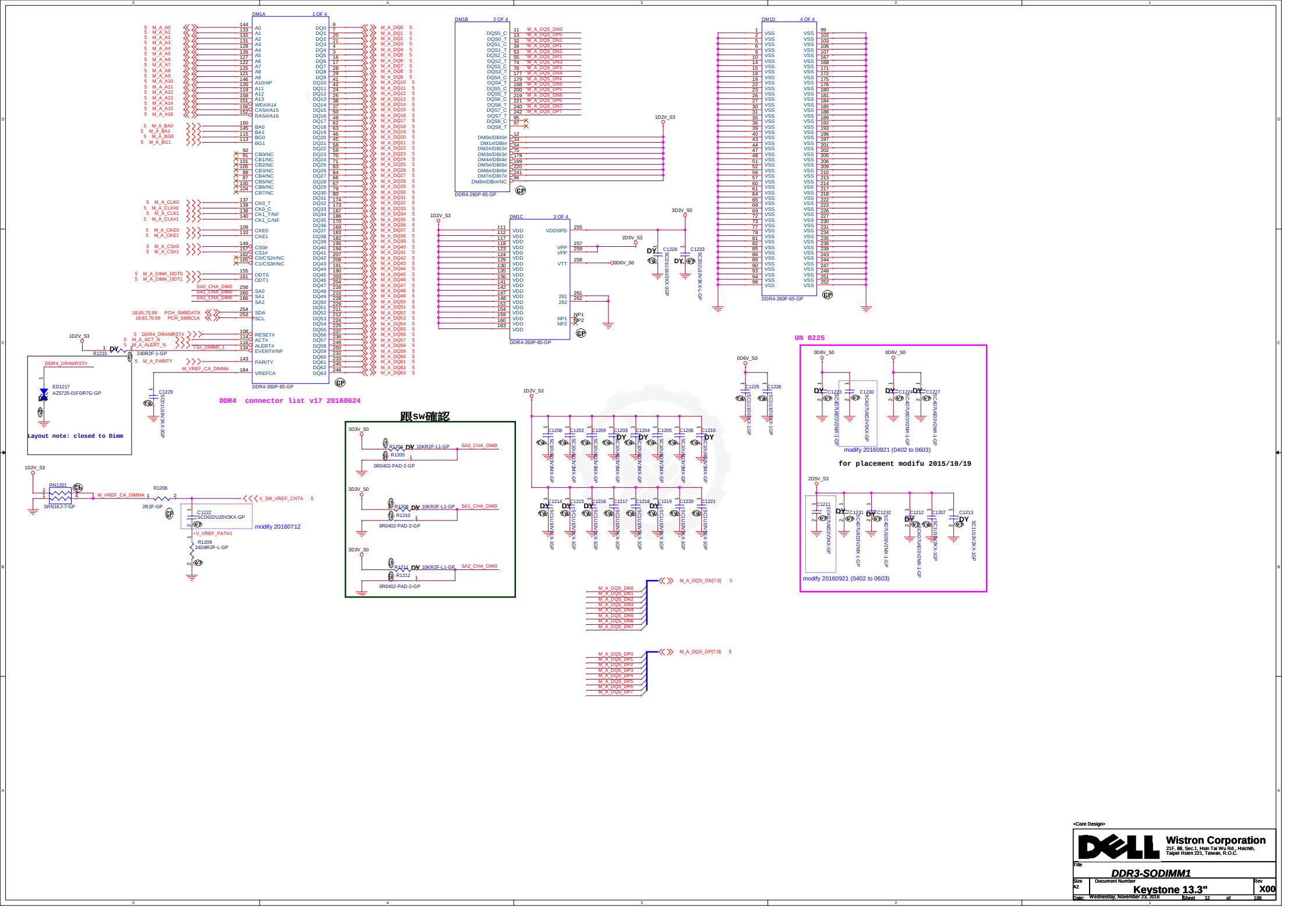
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP2)

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 11 of 106


DM1A
1 OF 4
DDR4-260P-65-GP
DM1B
2 OF 4
DDR4-260P-65-GP
DM1C
3 OF 4
DDR4-260P-65-GP
DM1D
4 OF 4
DDR4-260P-65-GP
DDR4 connector list v17 20160624
Layout note: closed to Dimm
跟Sw確認
UN 0225
for placement modifu 2015/10/19
modify 20160921 (0402 to 0603)
modify 20160712
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3-SODIMM1
Keystone 13.3"
X00
Wednesday, November 23, 2016

(Blanking)

(Blanking)

<Core Design>

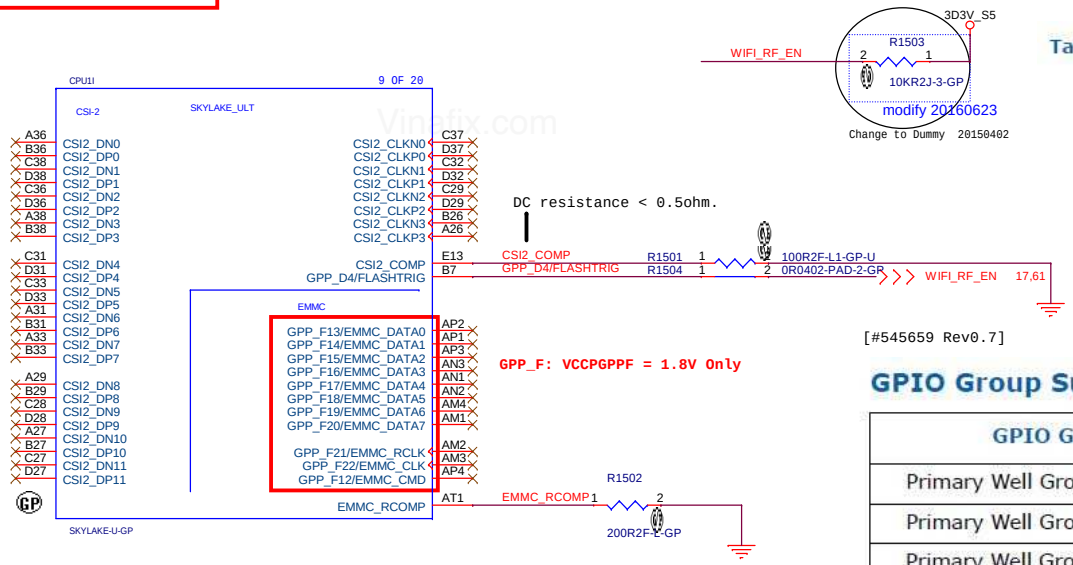
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	*Keystone 13.3"*	*X00*

Date: Wednesday, November 23, 2016 Sheet 14 of 106

Main Func = PCH



[#545659 Rev0.7]

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

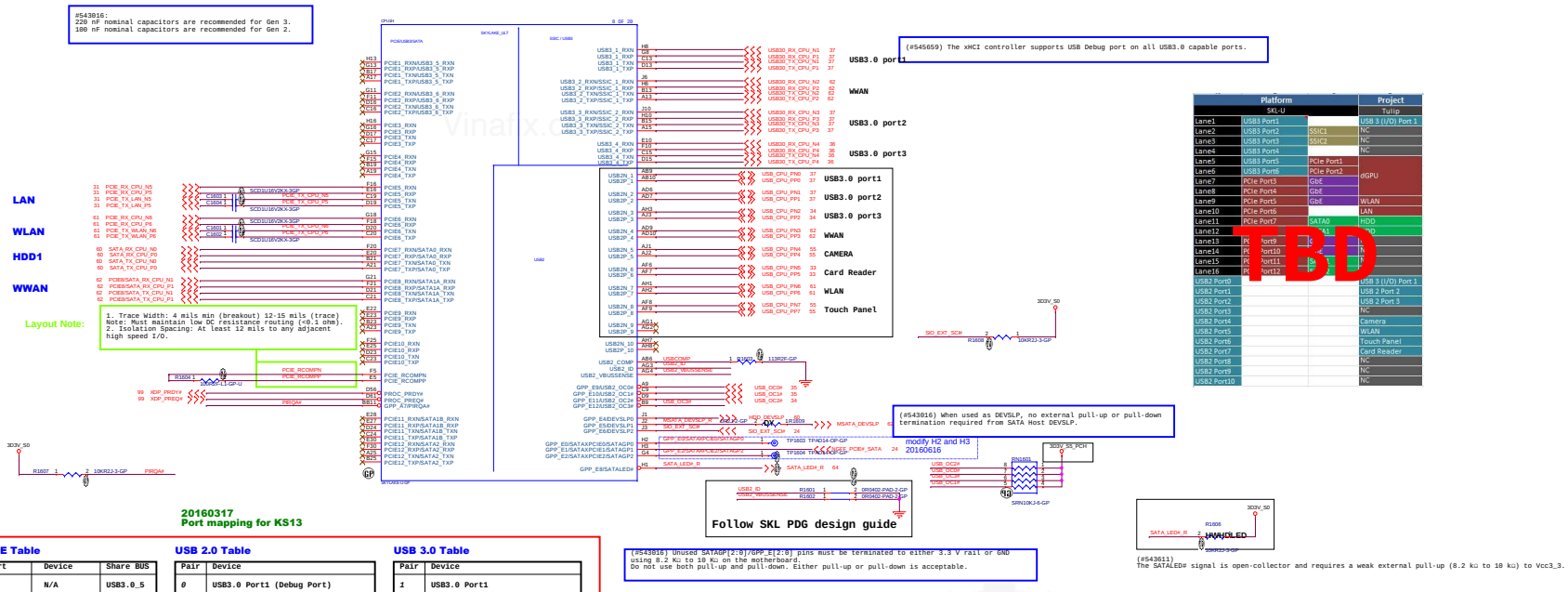
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 15 of 106

Main Func = PCH



Platform			Project
SKL-U			Tulip
Lane1	USB3 Port1		USB 3 (I/O) Port 1
Lane2	USB3 Port2	SSIC1	NC
Lane3	USB3 Port3	SSIC2	NC
Lane4	USB3 Port4		NC
Lane5	USB3 Port5	PCIe Port1	dGPU
Lane6	USB3 Port6	PCIe Port2	
Lane7	PCIe Port3	GbE	
Lane8	PCIe Port4	GbE	
Lane9	PCIe Port5	GbE	WLAN
Lane10	PCIe Port6		LAN
Lane11	PCIe Port7	SATA0	HDD
Lane12	[illegible]	[illegible]	[illegible]
Lane13	PCIe Port9	[illegible]	[illegible]
Lane14	PCIe Port10	[illegible]	[illegible]
Lane15	PCIe Port11	[illegible]	[illegible]
Lane16	PCIe Port12	[illegible]	[illegible]
USB2 Port0			USB 3 (I/O) Port 1
USB2 Port1			USB 2 Port 2
USB2 Port2			USB 2 Port 3
USB2 Port3			NC
USB2 Port4			Camera
USB2 Port5			WLAN
USB2 Port6			Touch Panel
USB2 Port7			Card Reader
USB2 Port8			NC
USB2 Port9			NC
USB2 Port10			NC

20160317
Port mapping for KS13

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_5
2	N/A	USB3.0_6
3	N/A	
4	N/A	
5	LAN	
6	WLAN	
7	HDD	SATA0
8	WWAN	

USB 2.0 Table

Pair	Device
0	USB3.0 Port1 (Debug Port)
1	USB3.0 Port2
2	USB3.0 port3
3	WWAN
4	CAMERA
5	Card Reader
6	WLAN (BT)
7	Touch Panel

USB 3.0 Table

Pair	Device
1	USB3.0 Port1
2	WWAN
3	USB3.0 Port2
4	USB3.0 port3

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

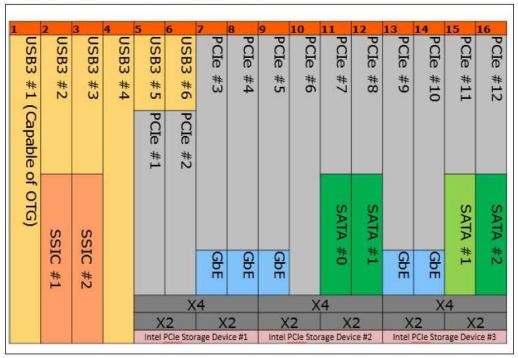


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH

R1709,R1723,R1703,R1724 merge to RN1704

GPD11 pull high by Intel PDG1.3 request

modify mount to DY 20160628

Layout note: 3 PAD SHARING

#561280 (PDG): 1M.
#544669 (CRB): 330k.

[543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

NON DS3

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

BATLOW#:
Pull-up required even if not implemented.

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

HSIO power switch IC and relate schematic

For sequence fine tune 2016/01/04

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

+VCCMPHYGTAON_1P0
SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

Reserve R1724, R1725 follow Iris SKL, 20160201

modify 20160923(DVT2)

DS3 BOM Option

Change dummy property from DS3 to DY

Change location to net PCH_DPWROK

modify 20160628(DVT1)

Dummy C1710 by it's useless

EC1711 modify to 100k and 0.01uF at DVT1 20150203

Reserve by NON DS3 function 20150413

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Keystone 13.3" | Rev: X00
Date: Wednesday, November 23, 2016 | Sheet 17 of 106

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

R1835 and R1834 merge to RN1802
2015/10/06 modify

PLACE WITHIN 1.1 INCH OF PCH

(#543016)Optional, can be left as OPEN/No-Connect.

Modify for layout, 20160427

modify RN1803 PN 20161122(X1)

66.10036.08L

SERIRQ PH:
PDG: 8.2k
CRB: 10k

RCIN#:
Frequency to Avoid: 33 MHz

20140820 DAIVD

RF 20160627
FC1802 LPC 20160701
FC1801 120p->100p 20160706

modify mount->DY
20160623

EE for DVT1 0212

DVT1 0212 for Vendor suggest (change 3p)

DVT1 0212 for Vendor suggest

separated, 20160425 modify

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

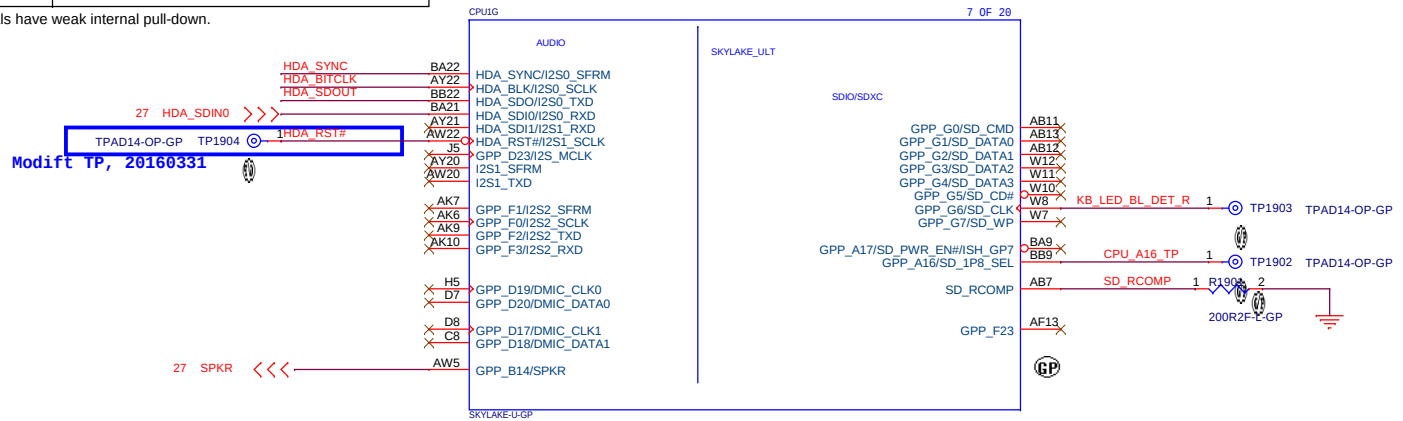
Date: Wednesday, November 23, 2016 | Sheet 18 of 106

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

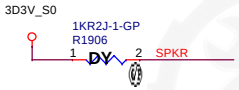
Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

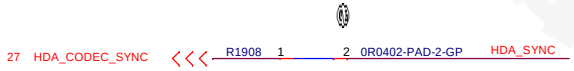
The internal pull-down is disabled after PLTRST# deasserts

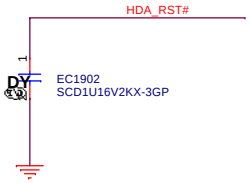
PCH strap pin:

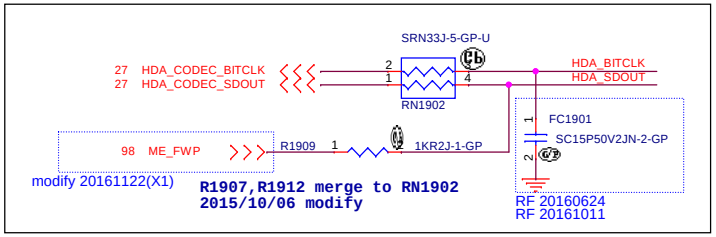
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts









<Core Design>

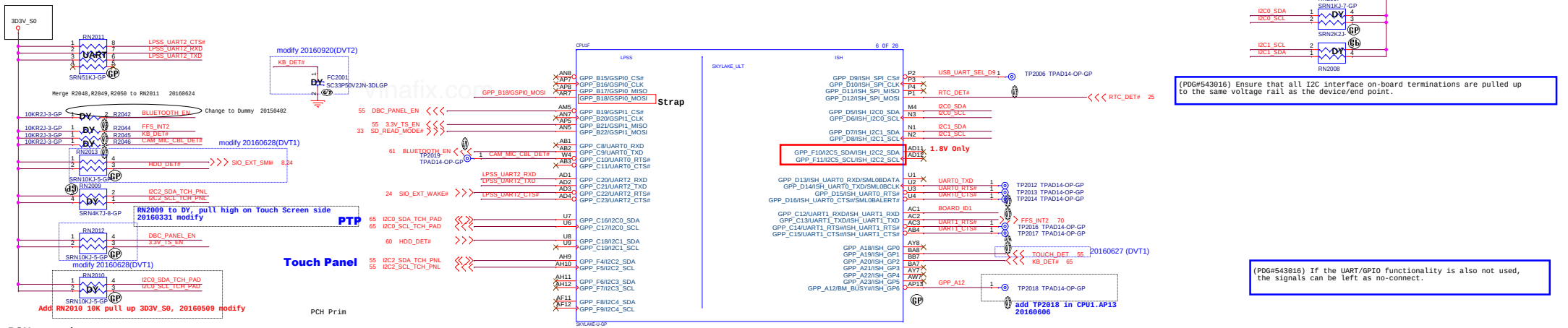
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 19 of 106

Main Func = PCH



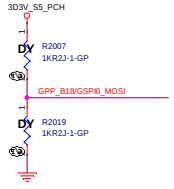
(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

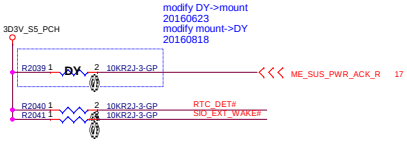
(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

PCH strap pin:

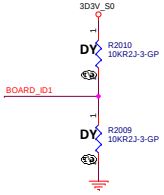
No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

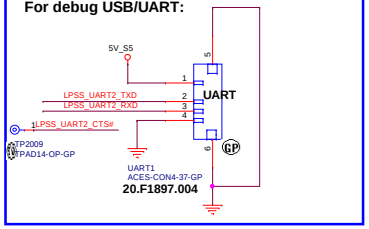




remove R2012(DY) and R2011(DY).
20160606



For debug USB/UART:



Intel has removed EHCI controller from BDW and proposed to use UART interface for Win7 debug.

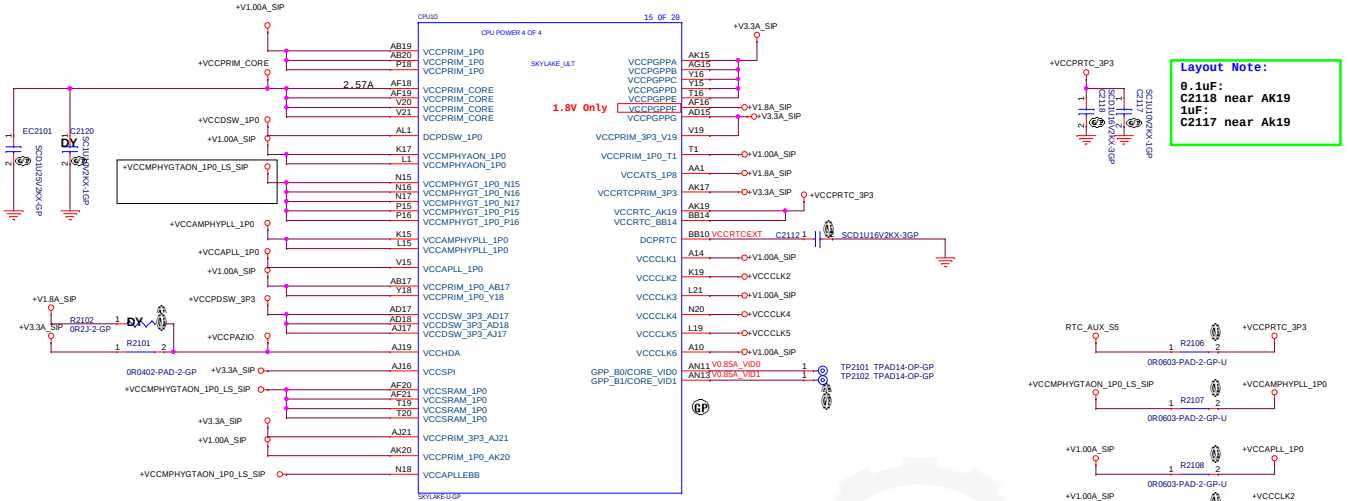
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPSS/ISH)

Size	Document Number	Rev
A2	Keystone 13.3"	X00

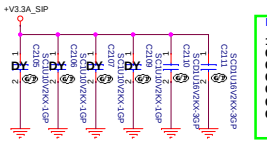
Date: Wednesday, November 23, 2016 Sheet 20 of 106

Main Func = PCH



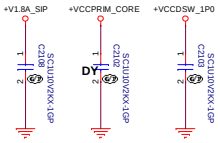
Layout Note:

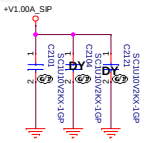
0.1uF:
C2118 near AK19
1uF:
C2117 near Ak19



Layout Note:

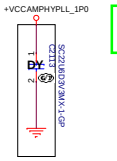
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19





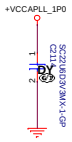
Layout Note:

1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1



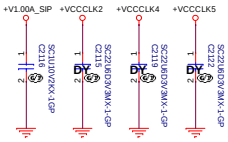
Layout Note:

22uF:
C2113 near K15



Layout Note:

22uF:
C2113 near K15



Layout Note:

1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

C2113 remove DY, 20160202

<Core Design>

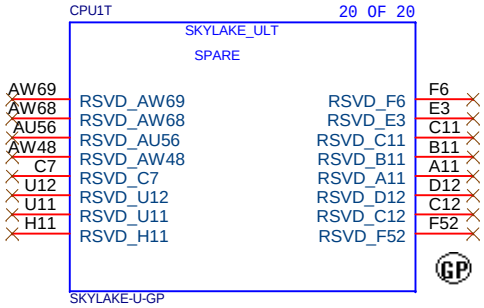
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 21 of 106

Main Func = PCH



<Core Design>

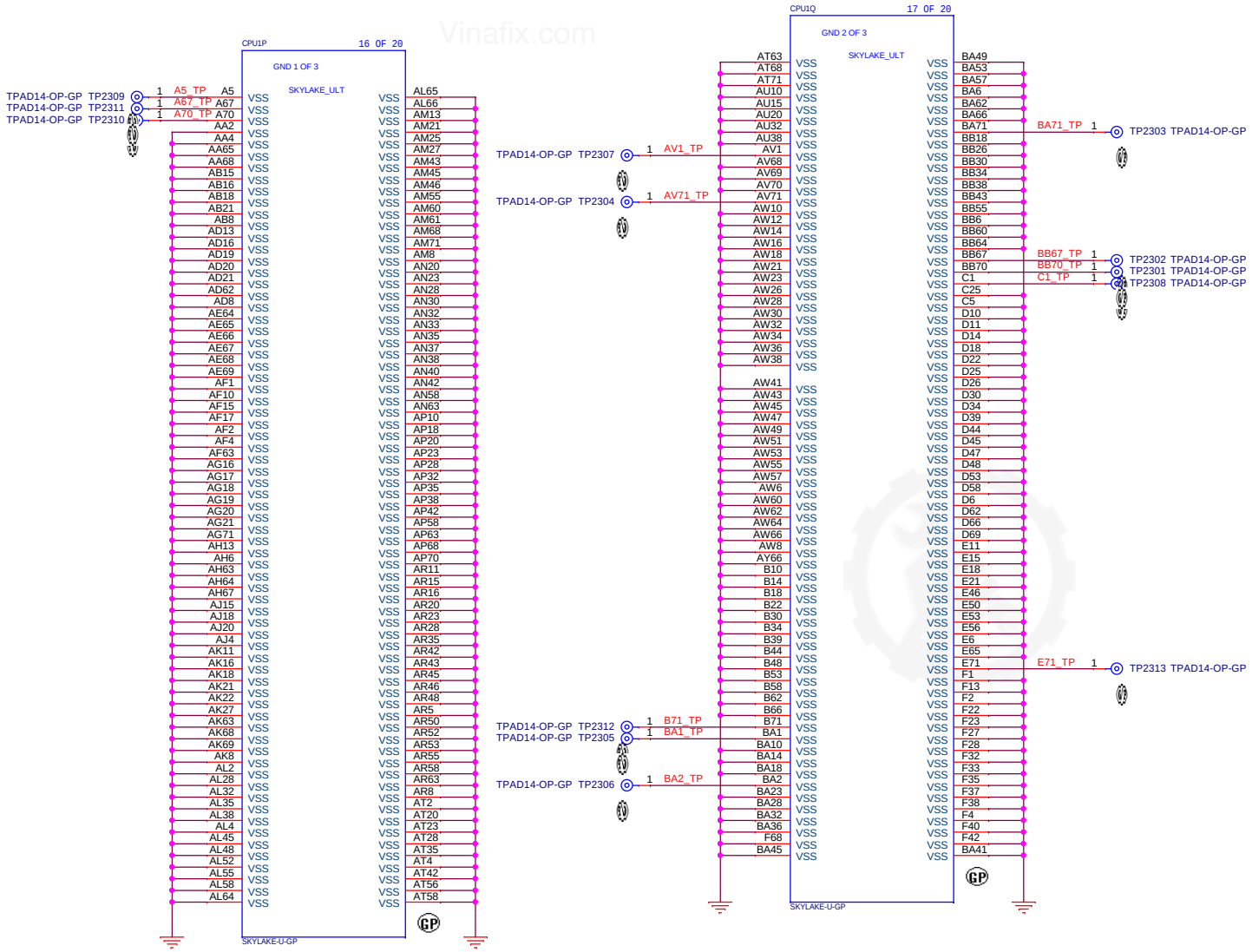
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(RSVD)***

Size	Document Number	Rev
A4	***Keystone 13.3"***	***X00***

Date: Wednesday, November 23, 2016 Sheet 22 of 106

Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 23 of 106

Main Func = KBC

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
EVT (SA) TPM SKU	100.0K	10.0K	3.0V
EVT (SA) NON TPM SKU	100.0K	20.0K	2.75V
DVT1 (SB) DVT1	100.0K	33.0K	2.48V
	100.0K	47.0K	2.24V
DVT2 (SC) DVT2	100.0K	64.9K	2V
	100.0K	76.8K	1.87V
X-build (1) A00	100.0K	100.0K	1.65V
	100.0K	143.0K	1.358V
	100.0K	174.0K	1.204V
	100.0K	215.0K	1.048V

MEC1404 PN: 071.01404.0B0E (KS13_Win schematics symbol)
MEC1406 PN: 071.01406.000G (KS13_Win BOM)

Layout Note: Need very close to EC

Layout Note: Need very close to EC

Merge R2404,R2406,R2405 to RN2407 20160624

Layout Note: Connect GND and AGND planes via either 0R resistor or connect directly.

Dummy R2422 & C2427 by EC control PCH_DPWROK 20150416

Layout Note: Need very close to EC / Need very close to EC

Move schematic, 20141118

Reserve by NON DS3 function 20150413

Change symbol part number, because origin symbol is DELL OBS part 20150116 2040

Change to Dummy 20150402

Just for placement 2015/09/23 modify

X00_0804

Q2412 and Q2413 merge 2014/12/23 modify

Modify for backlight connect straightly from PCH, 20160411

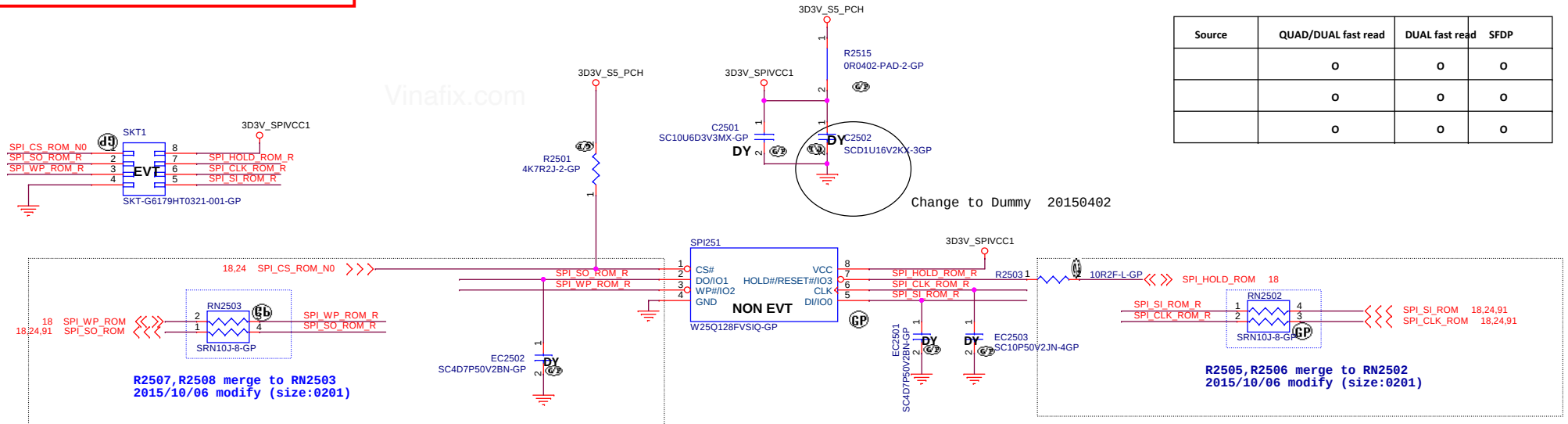
Remove D2403, 20160519 modify

SPI Flash ROM(256K) for EC

Power Switch Logic(PSL)

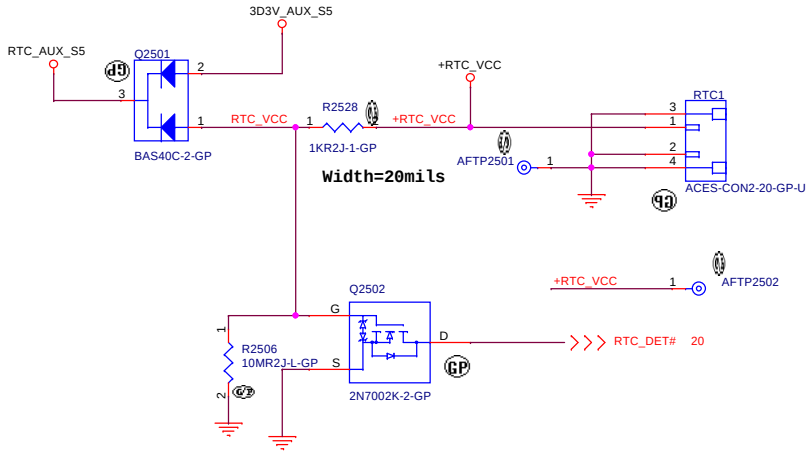
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: KBC Nuvoton NPCE285PA0DX	
Size: A1	Document Number: Keystone 13.3"
Date: Wednesday, November 26, 2014	Sheet 24 of 106

Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
	O	O	O
	O	O	O
	O	O	O

Main Func = RTC



<Core Design>

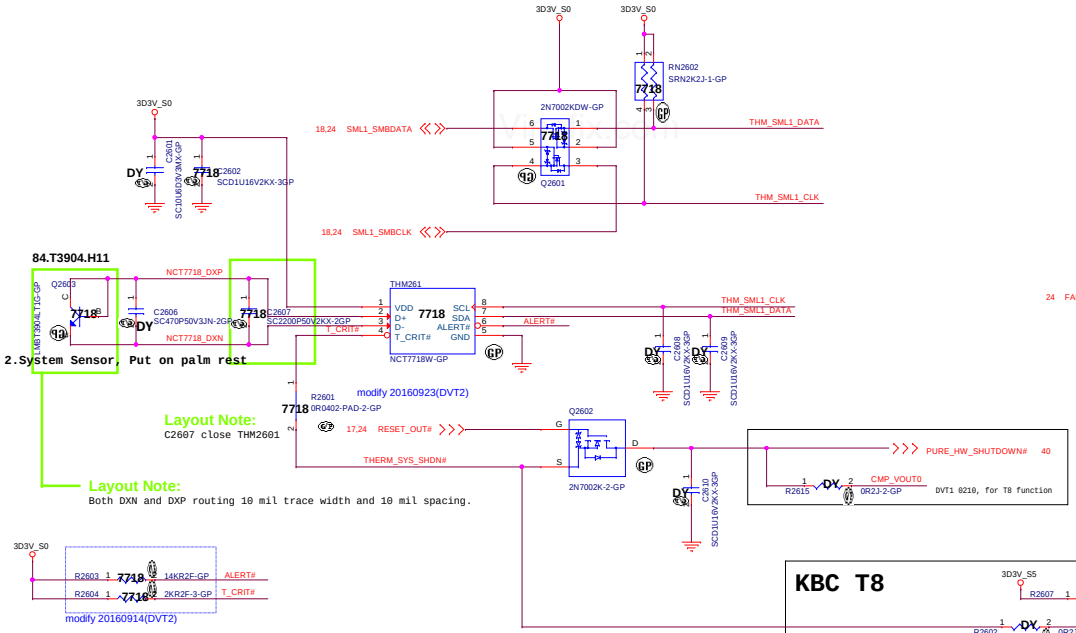
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 25 of 106

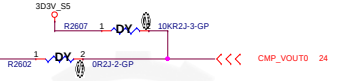
Main Func = Thermal Sensor



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

modify 20160914(DVT2)

KBC T8

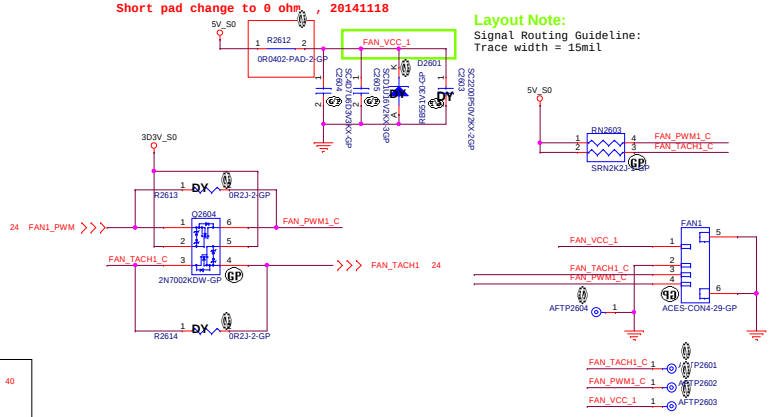


remove R2609 R2608 R2610 C2612 C2613 R2611 (modify 20160914)

PWM FAN1

Short pad change to 0 ohm , 20141118

Layout Note:
Signal Routing Guideline:
Trace width = 15mil



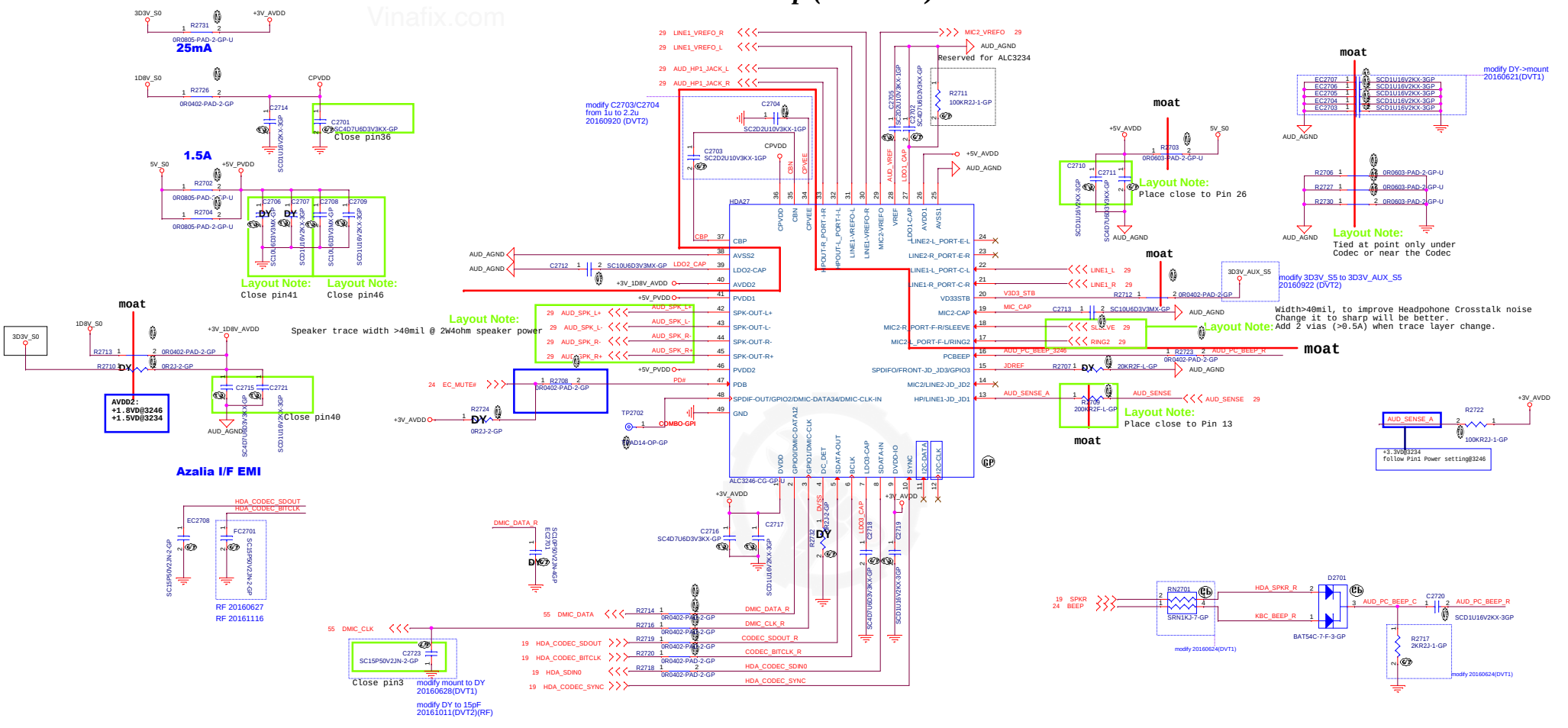
Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 26 of 106

Main Func = Audio

Audio Codec Chip (ALC3246)



Power requirement:
DVDD must >=DVDD_IO

+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3234

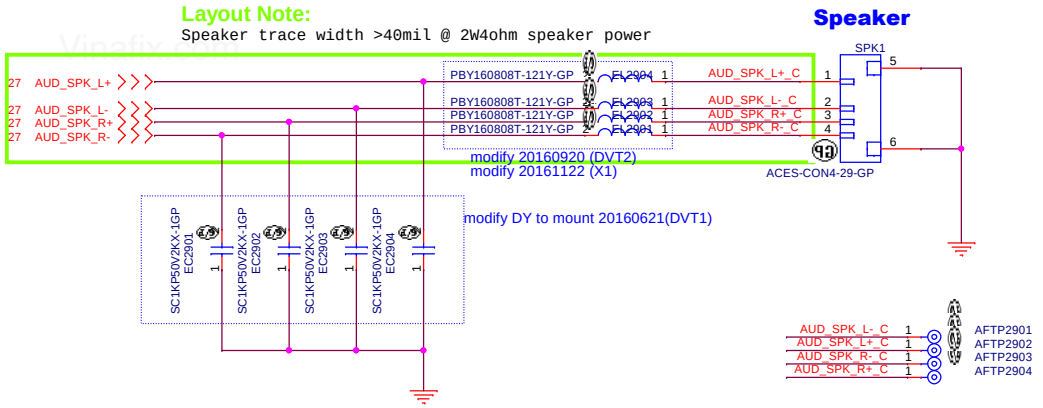
Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 27 of 106

Main Func = Audio

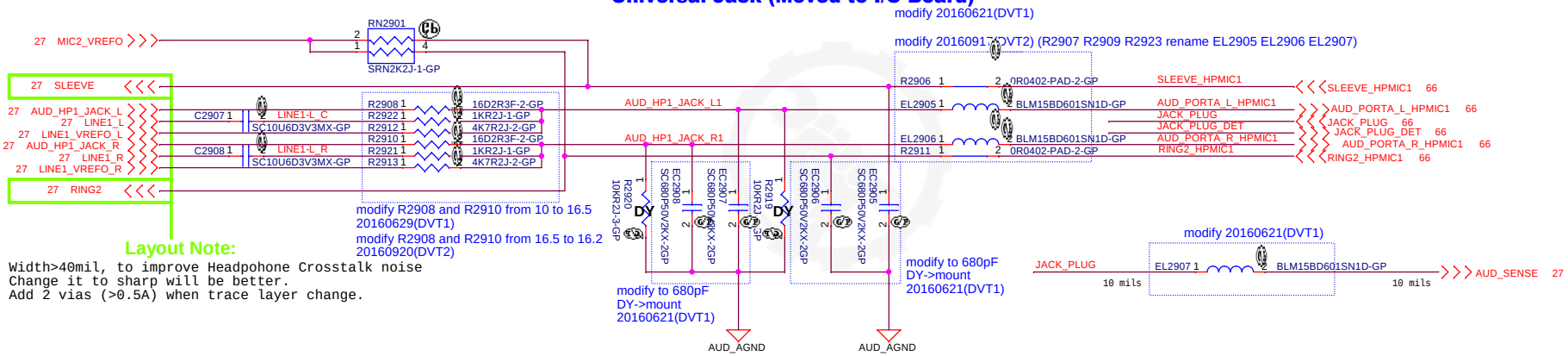
Speaker

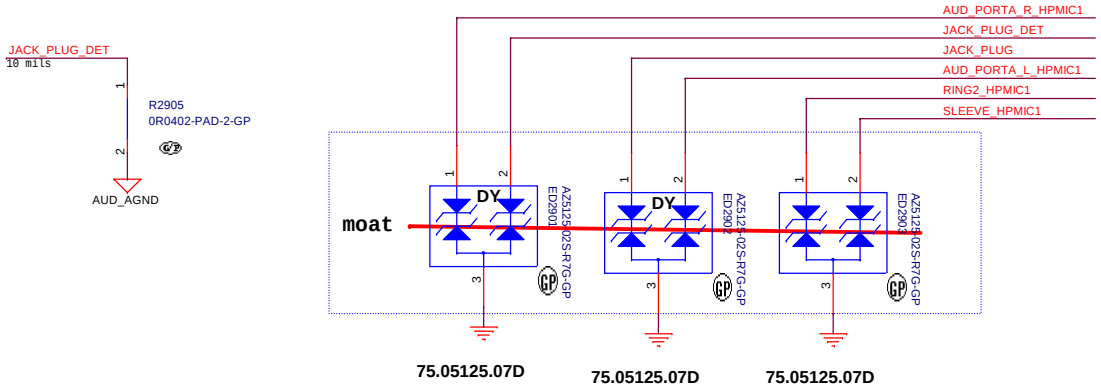
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

Universal Jack (Moved to I/O Board)





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: Keystone 13.3"
Rev: X00
Date: Wednesday, November 23, 2016
Sheet 29 of 106

Main Func = Audio

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

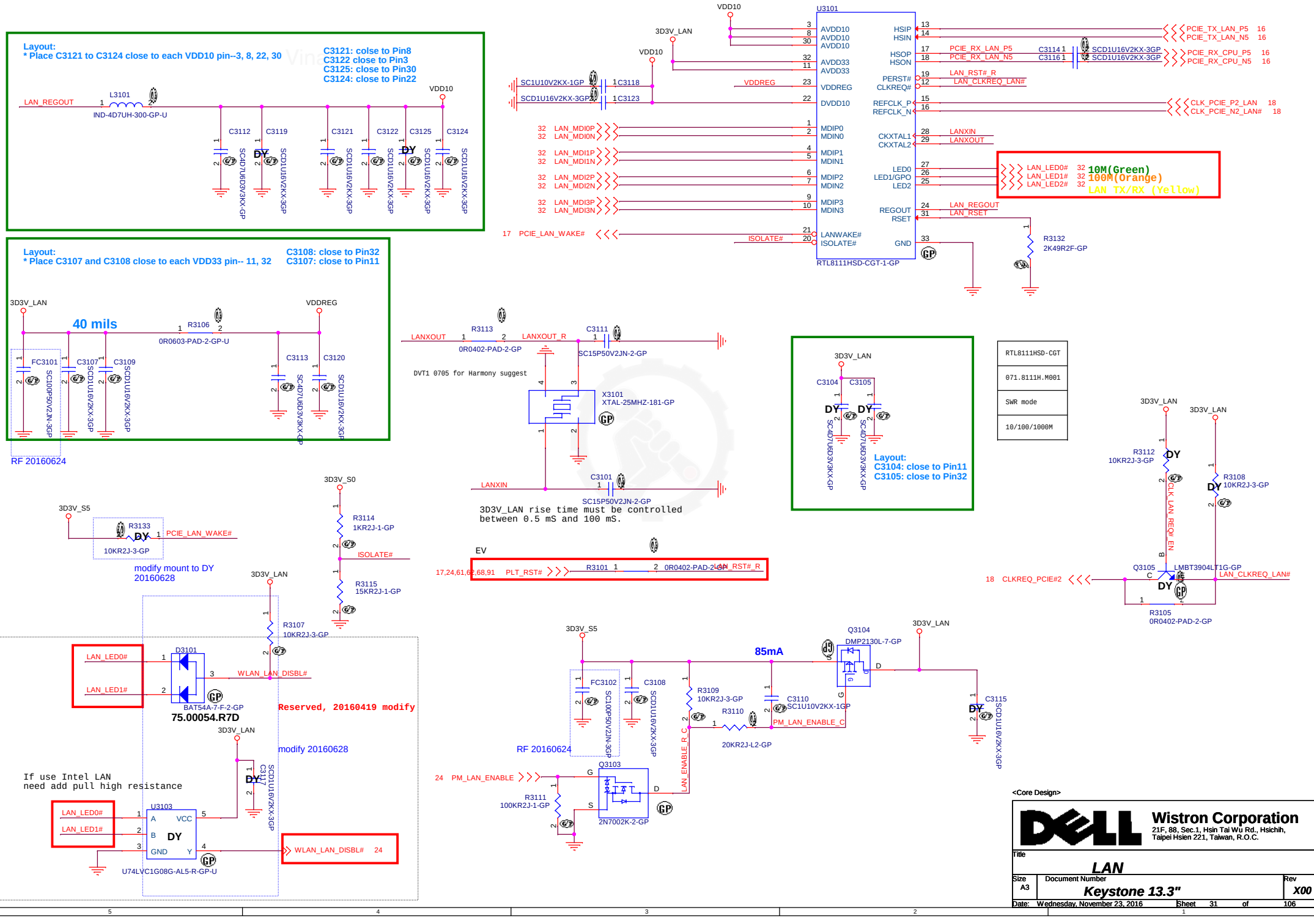
Title

(Reserved)

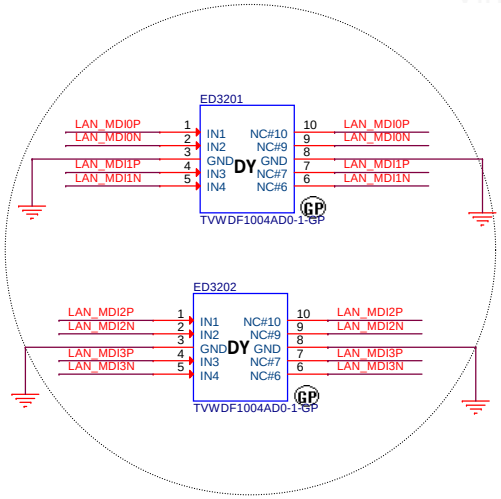
Size	Document Number	Rev
A4	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 30 of 106

SSID = LAN

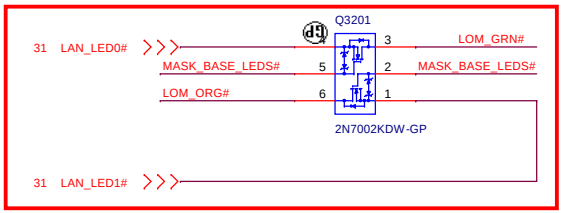

Layout:
* Place C3121 to C3124 close to each VDD10 pin--3, 8, 22, 30
C3121: colse to Pin8
C3122 close to Pin3
C3125: close to Pin30
C3124: close to Pin22
LAN_REGOUT
L3101
IND-4D7UH-300-GP-U
C3112
C3119
C3121
C3122
C3125
C3124
VDD10
SC4D7U6D3V3KX-GP
SCD1U16V2KX-3GP
Layout:
* Place C3107 and C3108 close to each VDD33 pin-- 11, 32
C3108: close to Pin32
C3107: close to Pin11
3D3V_LAN
40 mils
R3106
0R0603-PAD-2-GP-U
VDDREG
FC3101
C3107
C3109
C3113
C3120
SC100P50V2JN-3GP
SCD1U16V2KX-3GP
RF 20160624
U3101
RTL8111HSD-CGT-1-GP
AVDD10
AVDD33
VDDREG
DVDD10
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
LANWAKE#
ISOLATE#
HSIP
HSIN
HSOP
HSON
PERST#
CLKREQ#
REFCLK_P
REFCLK_N
CKXTAL1
CKXTAL2
LED0
LED1/GPO
LED2
REGOUT
RSET
GND
SC1U10V2KX-1GP
SCD1U16V2KX-3GP
C3118
C3123
LAN_MDI0P
LAN_MDI0N
LAN_MDI1P
LAN_MDI1N
LAN_MDI2P
LAN_MDI2N
LAN_MDI3P
LAN_MDI3N
PCIE_LAN_WAKE#
PCIE_TX_LAN_P5
PCIE_TX_LAN_N5
PCIE_RX_LAN_P5
PCIE_RX_LAN_N5
C3114
C3116
PCIE_RX_CPU_P5
PCIE_RX_CPU_N5
LAN_RST# R
LAN_CLKREQ_LAN#
CLK_PCIE_P2_LAN
CLK_PCIE_N2_LAN#
LANXIN
LANXOUT
LAN_LED0#
LAN_LED1#
LAN_LED2#
10M(Green)
100M(Orange)
LAN TX/RX (Yellow)
LAN_REGOUT
LAN_RSET
R3132
2K49R2F-GP
LANXOUT
R3113
0R0402-PAD-2-GP
LANXOUT_R
C3111
SC15P50V2JN-2-GP
DVT1 0705 for Harmony suggest
X3101
XTAL-25MHZ-181-GP
LANXIN
C3101
SC15P50V2JN-2-GP
3D3V_LAN rise time must be controlled
between 0.5 mS and 100 mS.
Layout:
C3104: close to Pin11
C3105: close to Pin32
C3104
C3105
SC4D7U6D3V3KX-GP
RTL8111HSD-CGT
071.8111H.M001
SWR mode
10/100/1000M
3D3V_S5
R3133
10KR2J-3-GP
PCIE_LAN_WAKE#
modify mount to DY
20160628
3D3V_S0
R3114
1KR2J-1-GP
ISOLATE#
R3115
15KR2J-1-GP
R3107
10KR2J-3-GP
EV
17,24,61,62,68,91
PLT_RST#
R3101
0R0402-PAD-2-GP
LAN_RST#_R
R3112
10KR2J-3-GP
R3108
10KR2J-3-GP
CLK_LAN_REQ#_EN
Q3105
LMBT3904LT1G-GP
18
CLKREQ_PCIE#2
LAN_CLKREQ_LAN#
R3105
0R0402-PAD-2-GP
LAN_LED0#
LAN_LED1#
D3101
BAT54A-7-F-2-GP
WLAN_LAN_DISBL#
75.00054.R7D
Reserved, 20160419 modify
modify 20160628
If use Intel LAN
need add pull high resistance
U3103
U74LVC1G08G-AL5-R-GP-U
WLAN_LAN_DISBL#
24
3D3V_S5
85mA
Q3104
DMP2130L-7-GP
FC3102
C3108
R3109
10KR2J-3-GP
C3110
SC1U10V2KX-1GP
R3110
20KR2J-L2-GP
PM_LAN_ENABLE_C
C3115
RF 20160624
Q3103
2N7002K-2-GP
24
PM_LAN_ENABLE
R3111
100KR2J-1-GP
LAN_ENABLE_R_C
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN
Size
A3
Document Number
Keystone 13.3"
Rev
X00
Date: Wednesday, November 23, 2016
Sheet 31 of 106

SSID = LOM

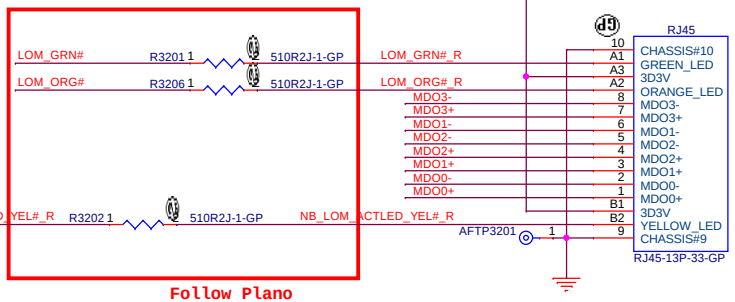


EV EMC

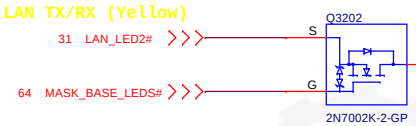
EV



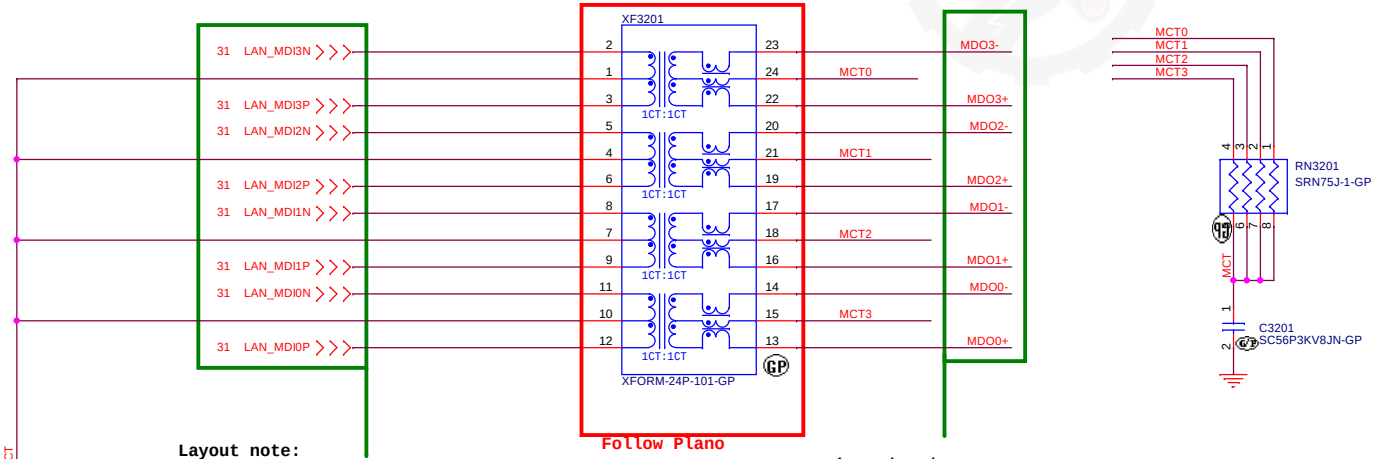
10M(Green)
100M(Orange)
1000M(Green+Orange)



LAN TX/RX (Yellow)



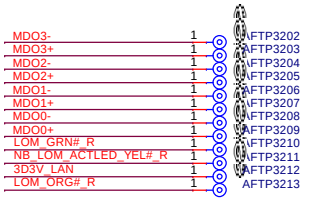
Follow Plano

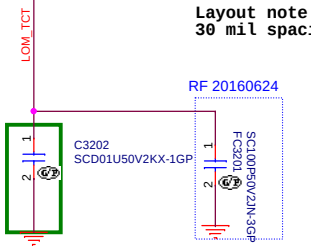


Follow Plano

Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.





Follow Reference Schematic 0.01uF~0.4uF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45/Transformer

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 32 of 106

Main Func = Card Reader

modify DY->mount
20160621(DVT1)

3D3V_CARD_IN_S0

EC3309 SCD1U16V2KX-3GP
C3309 SC3K3V6D7V4DF-3GP
C3310 SCD1U16V2KX-3GP

3D3V_CARD_OUT_S0

U3301
RTS5144-GR-GP

3V3_IN
3V3_IN
3V3_IN
CARD_3V3
DP
DM
SD_CD#
SD_DAT1
RREF
MS_INS#
48MHZ_IN
GND
AV18
GPIO
SDREG
SP1
SP2
SP3
SP4
SP5
SP6
SP7
SP8
SP9
SP10

SD_AV18 C3311 SC1U10V2KX-1GP
CR_GPIO0
SDREFG C3312 SC1U10V2KX-1GP
TP3302
SD_WP_5144
SD_D0 R3313 0R0402-PAD-2-GP SD_D0_C
SD_CLK R3320 0R0402-PAD-2-GP SD_CLK_R
SD_CMD R3314 0R0402-PAD-2-GP SD_CMD_C
SD_D3 R3310 0R0402-PAD-2-GP SD_D3_C
SD_D2 R3315 0R0402-PAD-2-GP SD_D2_C

USB_SDCARD_PP5
USB_SDCARD_PN5
SD_DAT1_C R3312 0R0402-PAD-2-GP
6K2R2F-GP R3308
SD_RREF
SD_48MHZ_IN
R3319 0R0402-PAD-2-GP

DY EC3307 SC10P50V2JN-4GP

KEEP DY
20160629(DVT1)

3D3V_S0
R3309 0R0603-PAD-2-GP-U
3D3V_CARD_IN_S0

16 USB_CPU_PP5
16 USB_CPU_PN5

remove co-lay R3304 R3305
20161117(X1)

EL3301
COIL-90OHM-100MHZ-5-GP
68.00396.001
USB_SDCARD_PP5
USB_SDCARD_PN5

modify EL3301
part number
for common part
20160620

3D3V_S0

For SD read only mode

R3301 10KR2J-3-GP DY
20 SD_READ_MODE#
Q3301 2N7002K-2-GP
SD_WP_5144

3D3V_CARD_OUT_S0

EC3308 SCD1U16V2KX-3GP DY
C3301 SCD1U16V2KX-3GP
C3302 SC4D7U6D3V3KX-GP

3D3V_CARD_OUT_S0
400mA

MSD1
SKT-CARDREADER-9P-1-GP
62.10051.D01
Normal Open

MICRO_SD_VDD
MICRO_SD_DAT0
MICRO_SD_DAT1
MICRO_SD_DAT2
MICROSD_SD_CD/DAT3
MICRO_SD_CMD
MICRO_SD_CLK
MICRO_SD_CD
MICRO_SD_VSS
MICRO_SD_GND
GND
GND
GND
GND

AFTP3311

SD_D0_C
SD_DAT1_C
SD_D2_C
SD_D3_C
SD_CMD_C
SD_CLK_C
SD_CD#_C

SD_CLK_R
SD_CD#
R3321 0R0402-PAD-2-GP
R3317 0R0402-PAD-2-GP

EC3311 SC6P50V2CN-1GP
Layout: close to connector

modify DY->mount
20160621(DVT1)

modify 10p to 6.8p vender suggs
20160705(DVT1)

DY EC3312 SC5P50V2CN-2GP
78.5R074.1FL

modify DY->mount
20160621(DVT1)

SD_CMD_C AFTP3302
SD_CLK_C AFTP3303
SD_CD#_C TP3304
SD_D0_C TP3306
SD_DAT1_C AFTP3307
SD_D2_C AFTP3308
SD_D3_C TP3309
3D3V_CARD_OUT_S0 TP3310

For EMI Reserved

SD_D0_C
SD_CLK_C
SD_CMD_C
SD_D3_C
SD_D2_C
SD_DAT1_C

EC3313 SC2D2P50V2CC-GP
EC3314 SC2D2P50V2CC-GP
EC3315 SC2D2P50V2CC-GP
EC3316 SC2D2P50V2CC-GP DY
EC3317 SC2D2P50V2CC-GP
EC3318 SC2D2P50V2CC-GP

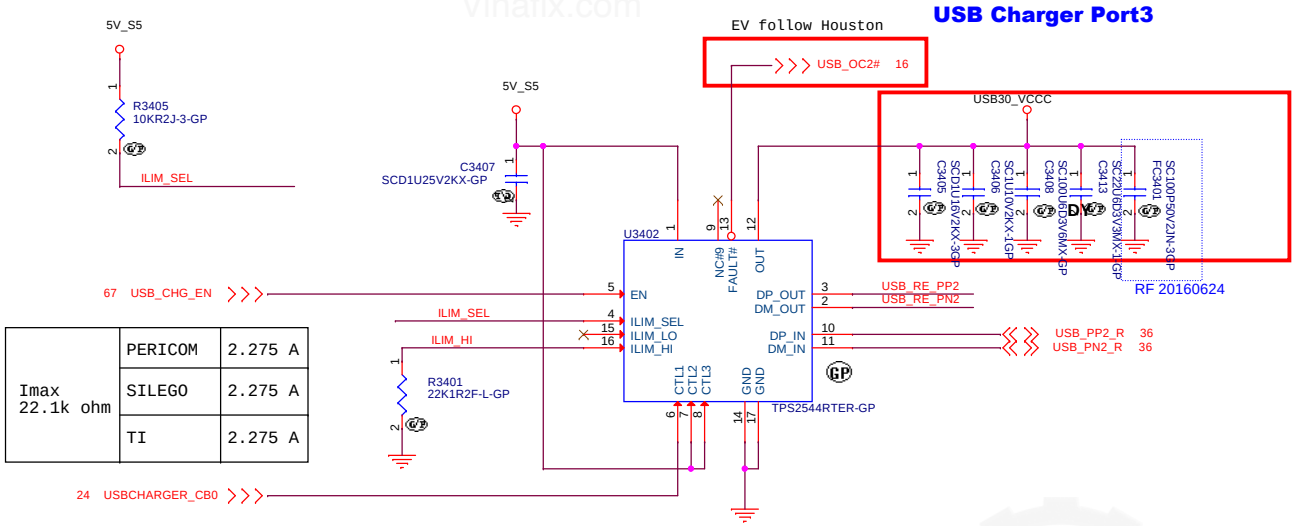
modify DY(ESD)->mount(cap)
20161007(DVT2)(control BOM)
modify CAP symbol
20161114(X1)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5144
Size: A3
Document Number: Keystone 13.3"
Rev: X00
Date: Wednesday, November 23, 2016
Sheet 33 of 106

Main Func = USB3.0 Port1



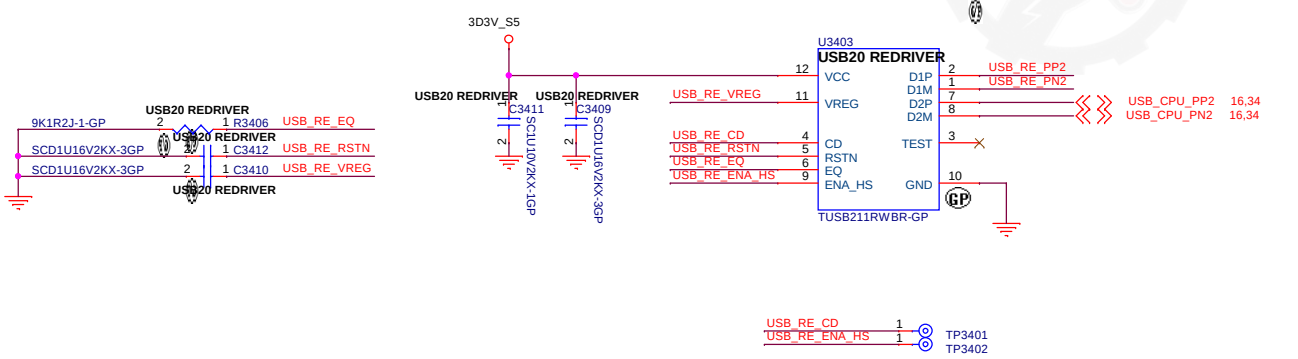
Imax 22.1k ohm	PERICOM	2.275 A
	SILEGO	2.275 A
	TI	2.275 A

PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data lines connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2(1)	ILIM_LO	
1	1	1	1	CDP(1)	ILIM_HI	Data lines connected

Note:
(1) No OUT discharge when changing between 1111 and 1110.

USB2.0 Redriver



EQ gain setting	R1 [ohms]
Level 0	100 +/- 5%
Level 1	1800 +/- 5%
Level 2	3900 +/- 1%
Level 3 [MIN]	9100 +/- 5%

<Core Design>

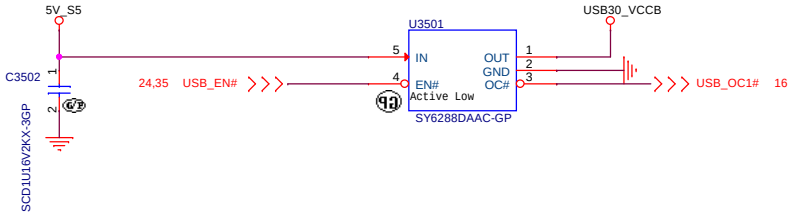
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

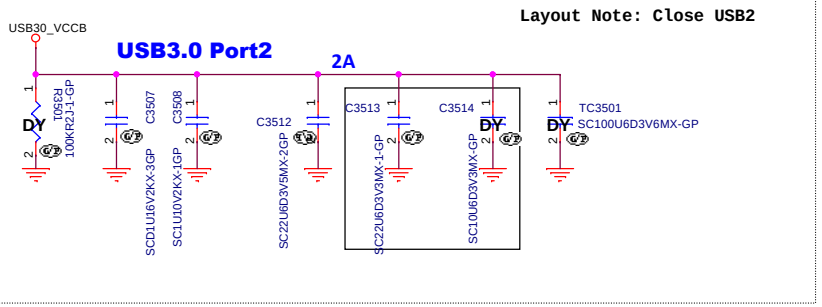
Title: (Reserved)

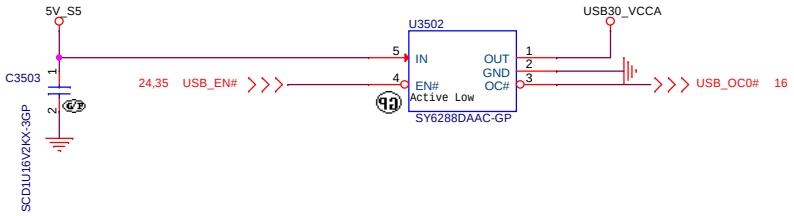
Size: A3 | Document Number: Keystone 13.3" | Rev: X00

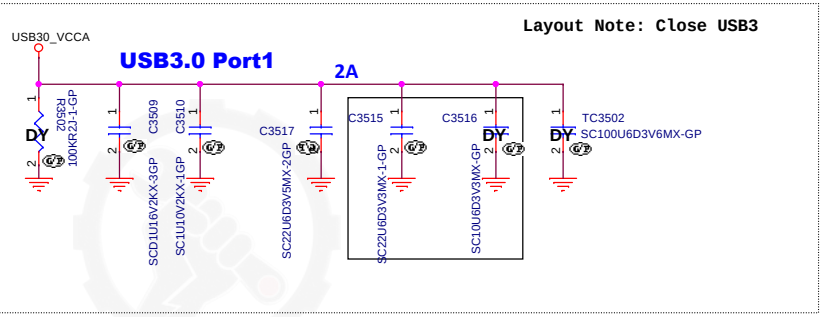
Date: Wednesday, November 23, 2016 | Sheet 34 of 106

Main Func = USB3.0 Port1









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB switch

Size	Document Number	Rev
	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 35 of 106

Main Func = USB3.0 Port1

USB3.0 Port3

16 USB30_TX_CPU_N4 → C3601 SCD1U16V2KX-3GP → USB30_TXDN4_R → R3605 0R0402-PAD-2-GP → USB30_TXDN4_C

16 USB30_RX_CPU_N4 → R3609 0R0402-PAD-2-GP → USB30_RXDN4_C

16 USB30_TX_CPU_P4 → C3602 SCD1U16V2KX-3GP → USB30_TXDP4_R → R3606 0R0402-PAD-2-GP → USB30_TXDP4_C

16 USB30_RX_CPU_P4 → R3610 0R0402-PAD-2-GP → USB30_RXDP4_C

34 USB_PN2_R / 34 USB_PP2_R → EL3602 COIL-90OHM-100MHZ-5-GP 68.00396.001 → USB20_DN2_C / USB20_DP2_C

modify EL3602 part number for common part 20160620

AFTP3601 / AFTP3602 → 20160810

USB30_VCCC

USB3 → SKT-USB13-112-GP 22.10341.E21

USB3		
1	VBUS	
2	D-	USB20_DN2_C
3	D+	USB20_DP2_C
5	STDA_SSRX-	USB30_RXDN4_C
6	STDA_SSRX+	USB30_RXDP4_C
8	STDA_SSTX-	USB30_TXDN4_C
9	STDA_SSTX+	USB30_TXDP4_C
10	CHASSIS#10	
11	CHASSIS#11	
12	CHASSIS#12	
13	CHASSIS#13	
4	GND	
7	GND_DRAIN	

Stuff for ESD R2 spec

ED3601 AOZ8808DI-05-1-GP

USB30_RXDN4_C	1	10	USB30_RXDN4_C
USB30_RXDP4_C	2	9	USB30_RXDP4_C
	3	8	
USB30_TXDN4_C	4	7	USB30_TXDN4_C
USB30_TXDP4_C	5	6	USB30_TXDP4_C

75.08808.073
2nd = 075.01043.0073

modify ED3601 part number for common part 20160620

Stuff for ESD R2 spec

USB30_VCCC

ED3602 AZC099-04S-2-GP

USB20_DN2_C	1	I/O1 / I/O4	6 USB20_DP2_C
	2	GND / VDD	5
	3	I/O2 / I/O3	4

075.09904.0A7C
2nd = 75.00199.07C

modify ED3602 part number for common part 20160620

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 36 of 106

Main Func = USB3.0 Port1

USB3.0 Port2

16 USB30_TX_CPU_N3 → C3706 SCD1U16V2KX-3GP → USB30_TXDN3_R → R3719 0R0402-PAD-2-GP → USB30_TXDN3_C

16 USB30_RX_CPU_N3 → R3722 0R0402-PAD-2-GP → USB30_RXDN3_C

16 USB30_TX_CPU_P3 → C3705 SCD1U16V2KX-3GP → USB30_TXDP3_R → R3721 0R0402-PAD-2-GP → USB30_TXDP3_C

16 USB30_RX_CPU_P3 → R3718 0R0402-PAD-2-GP → USB30_RXDP3_C

16 USB_CPU_PP1 → EL3707 COIL-90OHM-100MHZ-5-GP 68.00396.001 → USB20_DP1_C

16 USB_CPU_PN1 → EL3707 → USB20_DN1_C

modify EL3707 part number for common part 20160620

AFTP3702 / AFTP3703 20160810

USB30_VCCB

USB2 SKT-USB13-112-GP 22.10341.E21

1	VBUS	STDA_SSRX-	5 USB30_RXDN3_C
2	D-	STDA_SSRX+	6 USB30_RXDP3_C
3	D+	STDA_SSTX-	8 USB30_TXDN3_C
10	CHASSIS#10	STDA_SSTX+	9 USB30_TXDP3_C
11	CHASSIS#11	GND	4
12	CHASSIS#12	GND_DRAIN	7
13	CHASSIS#13		

USB20_DN1_C / USB20_DP1_C

Stuff for ESD R2 spec

ED3706 AOZ8808DI-05-1-GP

USB30_RXDN3_C	1	10	USB30_RXDN3_C
USB30_RXDP3_C	2	9	USB30_RXDP3_C
	3	8	
USB30_TXDN3_C	4	7	USB30_TXDN3_C
USB30_TXDP3_C	5	6	USB30_TXDP3_C

75.08808.073
2nd = 075.01043.0073

modify ED3706 part number for common part 20160620

Stuff for ESD R2 spec

ED3705 AZC099-04S-2-GP

USB20_DN1_C	1	6	USB20_DP1_C
GND	2	5	VDD
I/O2	3	4	I/O3

USB30_VCCB

modify ED3705 part number for common part 20160620

USB3.0 Port1

16 USB30_TX_CPU_N1 → C3703 SCD1U16V2KX-3GP → USB30_TXDN1_R → R3711 0R0402-PAD-2-GP → USB30_TXDN1_C

16 USB30_RX_CPU_N1 → R3712 0R0402-PAD-2-GP → USB30_RXDN1_C

16 USB30_TX_CPU_P1 → C3704 SCD1U16V2KX-3GP → USB30_TXDP1_R → R3714 0R0402-PAD-2-GP → USB30_TXDP1_C

16 USB30_RX_CPU_P1 → R3713 0R0402-PAD-2-GP → USB30_RXDP1_C

16 USB_CPU_PP0 → EL3703 COIL-90OHM-100MHZ-5-GP 68.00396.001 → USB20_DP0_C

16 USB_CPU_PN0 → EL3703 → USB20_DN0_C

modify EL3703 part number for common part 20160620

AFTP3704 / AFTP3701 20160810

USB30_VCCA

USB1 SKT-USB13-112-GP 22.10341.E21

1	VBUS	STDA_SSRX-	5 USB30_RXDN1_C
2	D-	STDA_SSRX+	6 USB30_RXDP1_C
3	D+	STDA_SSTX-	8 USB30_TXDN1_C
10	CHASSIS#10	STDA_SSTX+	9 USB30_TXDP1_C
11	CHASSIS#11	GND	4
12	CHASSIS#12	GND_DRAIN	7
13	CHASSIS#13		

USB20_DN0_C / USB20_DP0_C

Stuff for ESD R2 spec

ED3703 AOZ8808DI-05-1-GP

USB30_RXDN1_C	1	10	USB30_RXDN1_C
USB30_RXDP1_C	2	9	USB30_RXDP1_C
	3	8	
USB30_TXDN1_C	4	7	USB30_TXDN1_C
USB30_TXDP1_C	5	6	USB30_TXDP1_C

modify ED3703 part number for common part 20160620

Stuff for ESD R2 spec

ED3704 AZC099-04S-2-GP

USB20_DN0_C	1	6	USB20_DP0_C
GND	2	5	VDD
I/O2	3	4	I/O3

USB30_VCCA

modify ED3704 part number for common part 20160620

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB30	
Size A3	Document Number Keystone 13.3"	Rev X00
Date: Wednesday, November 23, 2016	Sheet 37 of 106	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 38 of 106

Main Func = USB3.0 Port1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

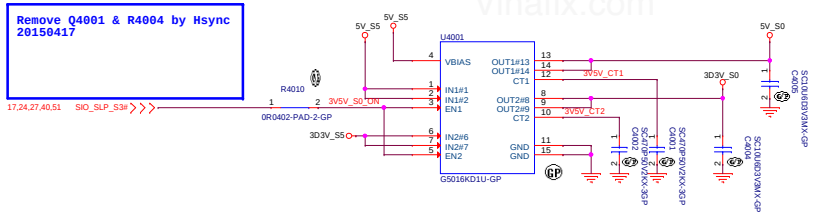
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 39 of 106

Main Func = Power Plane & Sequence

ROSA Run Power

Remove Q4001 & R4004 by Hsync 20150417

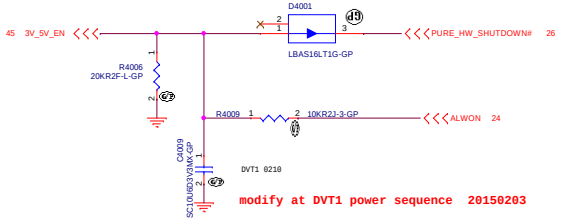


5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

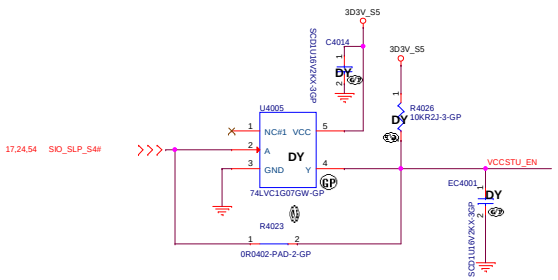


modify at DVT1 power sequence 20150203

20150116 2032

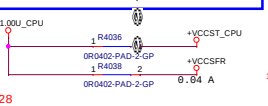
EOPIO and EDRAM

MANAGEMENT RAIL POWER GENERATION

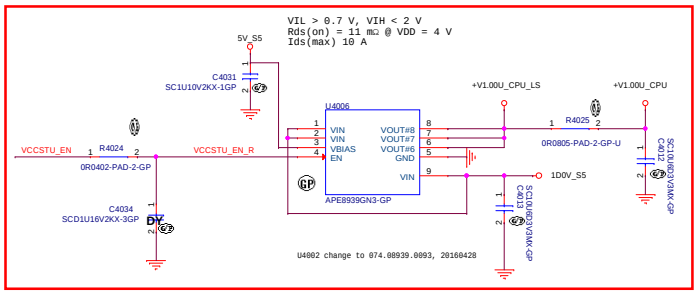


VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

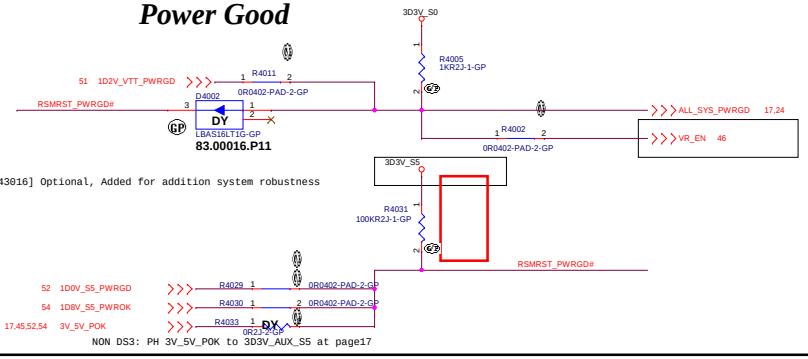
VCCST



Modify power switch IC and relate schematic, 20160428

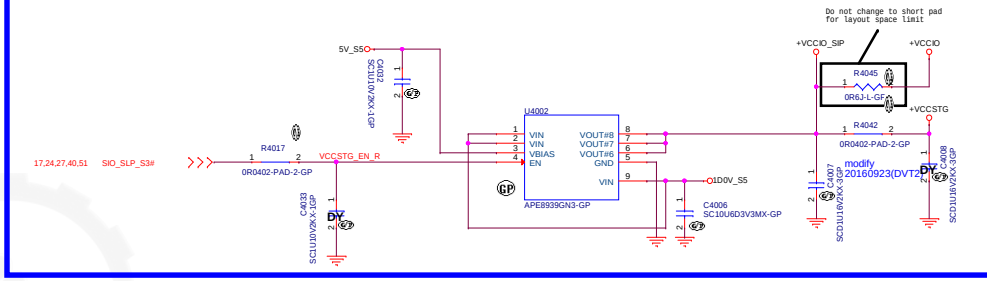


Power Good



VCCIO and VCCSTG

Modify power switch IC and relate schematic
2016/01/07



VCCSTG

V1.8S

<Core Design>

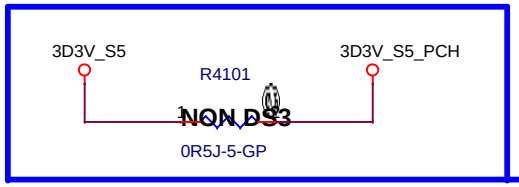
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

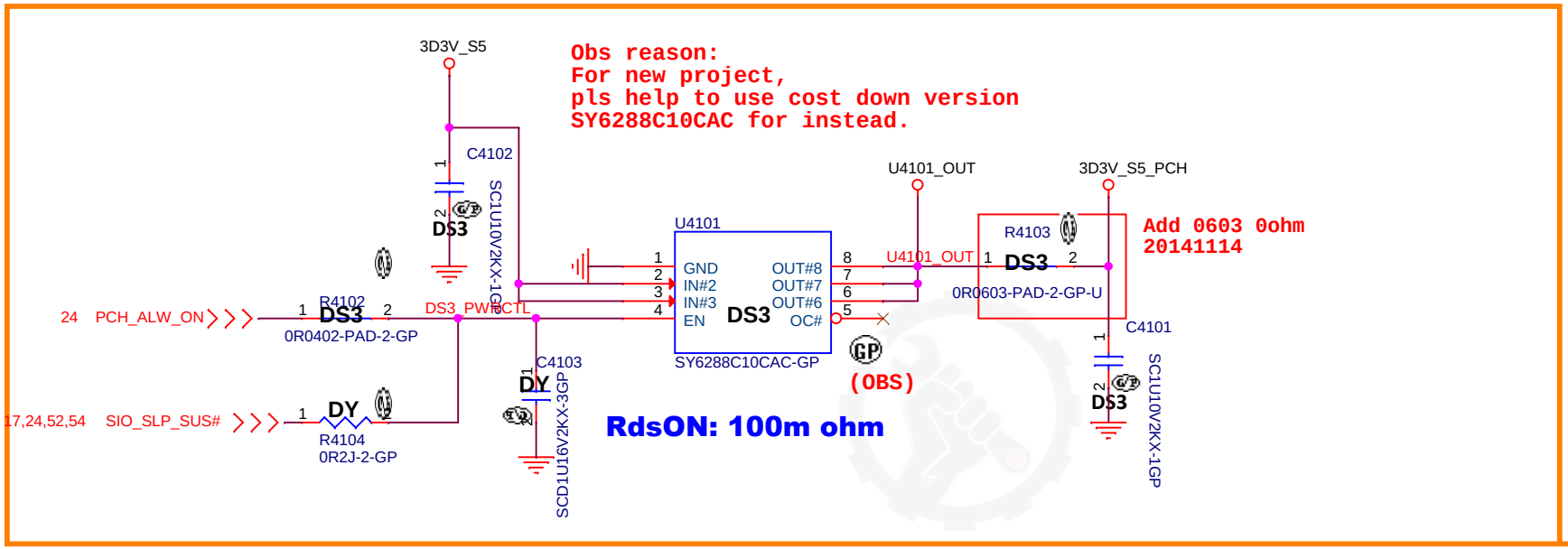
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 40 of 106

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413



DS3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(1/2)+DS3*

Size	Document Number	Rev
A4	*Keystone 13.3"*	*X00*

Date: Wednesday, November 23, 2016 Sheet 41 of 106

Main Func = DIMM1

Main Func = DIMM2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 42 of 106

SSID = PWR.Support

CC for RFQ, 20160226

Batt Connecter

BT+
EC4303 SCD1U25V2KX-GP
PD4302 SMF18A-GP
BATT1
NP1
NP2
ETY-CON10-GP-U
RN4301
SRN100J-4-GP
PBAT_SMBCLK1
PBAT_SMBDAT1
PBAT_PRES1#
SYS_PRES1#
AFTP4309
20160810
AFTP4305
EC4301 SCD10P50V2JN-4GP
EC4302 SCD10P50V2JN-4GP
EC4305 SCD10P50V2JN-4GP
AFTP4301
AFTP4302
AFTP4303
AFTP4304

Placement: Close to Batt Connector

ED4302 LBAV99LT1G-1-GP
ED4303 LBAV99LT1G-1-GP
ED4301 LBAV99LT1G-1-GP
3D3V_S5

change power source to 3D3V_S5 for easy layout and better ESD

R4301 0R0402-PAD

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

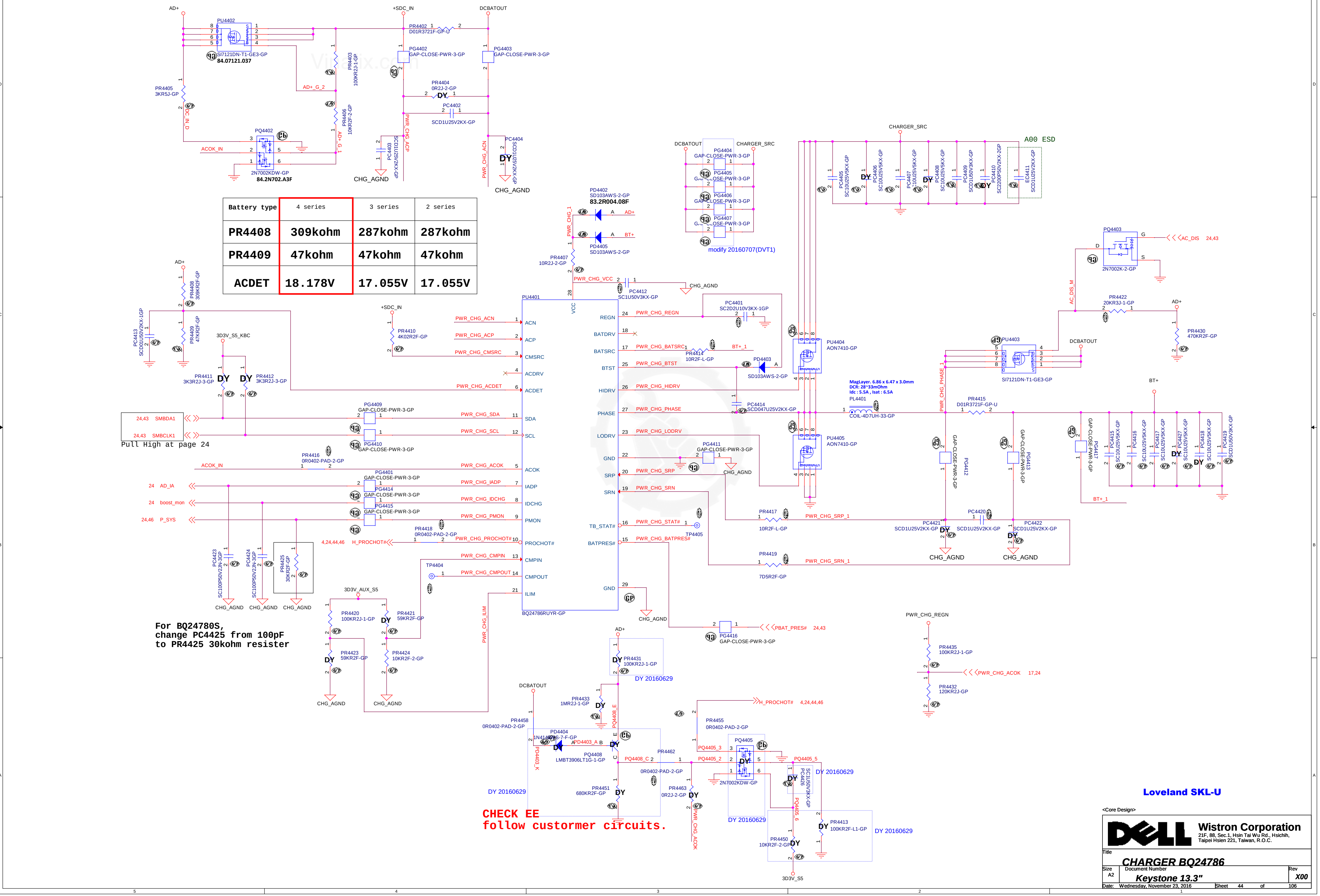
5V_S5
PR4302 15KR2F-GP
PQ4302 LMBT3904LT1G-GP
PR4303 10KR2J-3-GP
PQ3802_1
PR4311 100KR2J-1-GP
PSID_DISABLE#_R_C
PQ4301 DMN5L06K-7-GP
PS_ID_R
PS_ID_S
PR4307 33R2J-2-GP
PD4303 LBAV99LT1G-1-GP
PR4306 2K2R2J-2-GP
PS_ID 24
EC4307 SC10P50V2JN-4GP
JGND
EC4310 SCD1U50V5JX-1-GP
EL4303
EL4304
0R0805-PAD-2-GP-U
DCIN1
ACES-CON5-27-GP-U
AFTP4308
+DC_IN_C
EL4301
EL4302
PR4316 3K3R6J-GP
PQ4209_D
PQ4309 2N7002K-2-GP
modify DY 20160629
PD4301 P6SMB27A-GP
PQ4304
LTC024EUB-FS8-GP
AD_OFF_L
AD_OFF_R
PQ4305
LTA024EUB-FS8-GP
+DC_IN
PR4309 2R4KR5-GP
PR4310 47KR3J-L-GP
PU4301
SI7121DN-T1-GE3-GP
AD+
AC_DIS_R
24,44 AC_DIS
PR4312 0R0402-PAD-1-GP
modify 1k to 0 ohm
20160629
AFTP4306
AFTP4307

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY CONN
Size: A2
Document Number: Keystone 13.3"
Rev: X00
Date: Wednesday, November 23, 2016
Sheet 43 of 106

Main Func = Charger



Battery type	4 series	3 series	2 series
PR4408	309kohm	287kohm	287kohm
PR4409	47kohm	47kohm	47kohm
ACDET	18.178V	17.055V	17.055V

For BQ24780S,
change PC4425 from 100pF
to PR4425 30kohm resister

CHECK EE
follow custormer circuits.

Loveland SKL-U

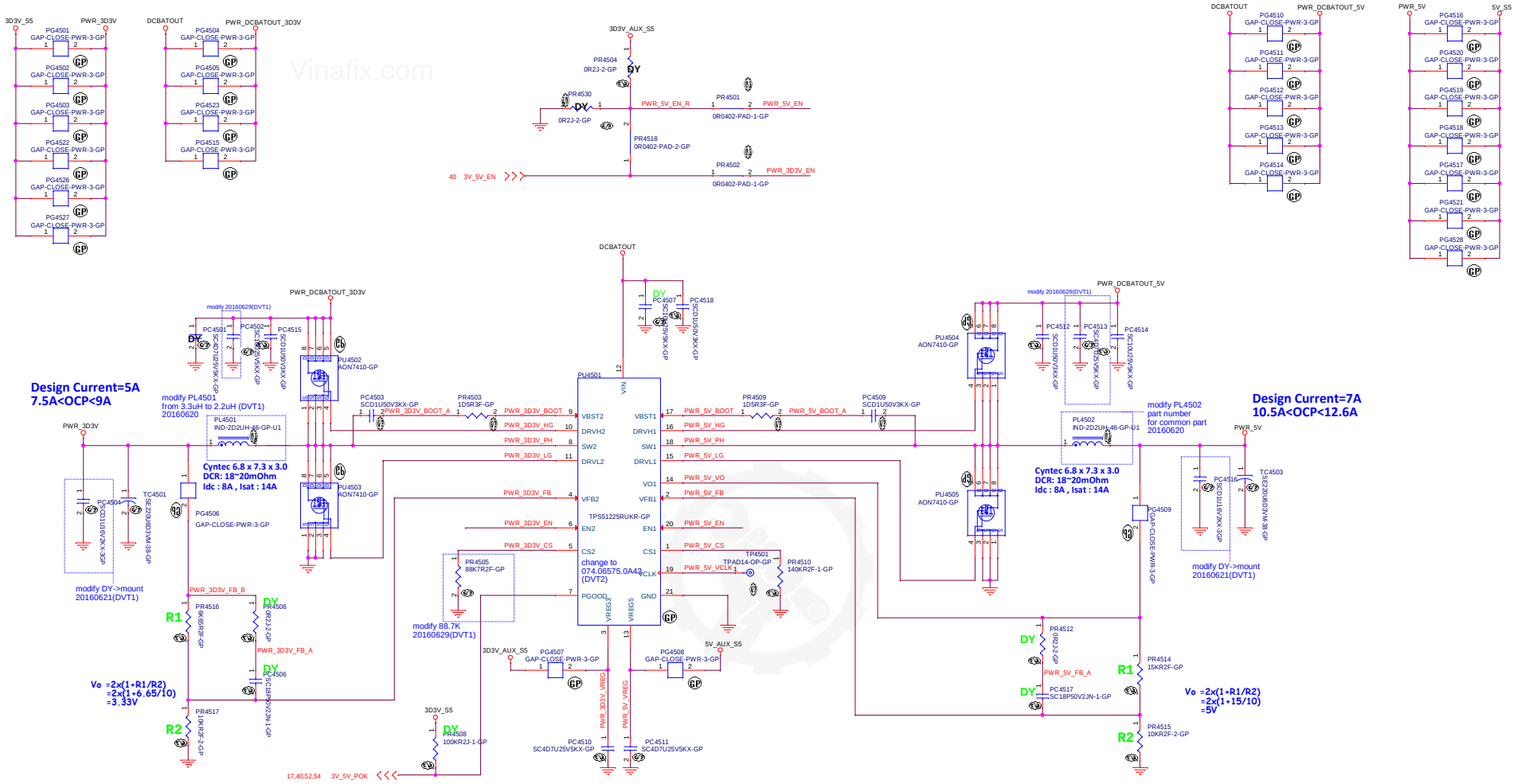
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

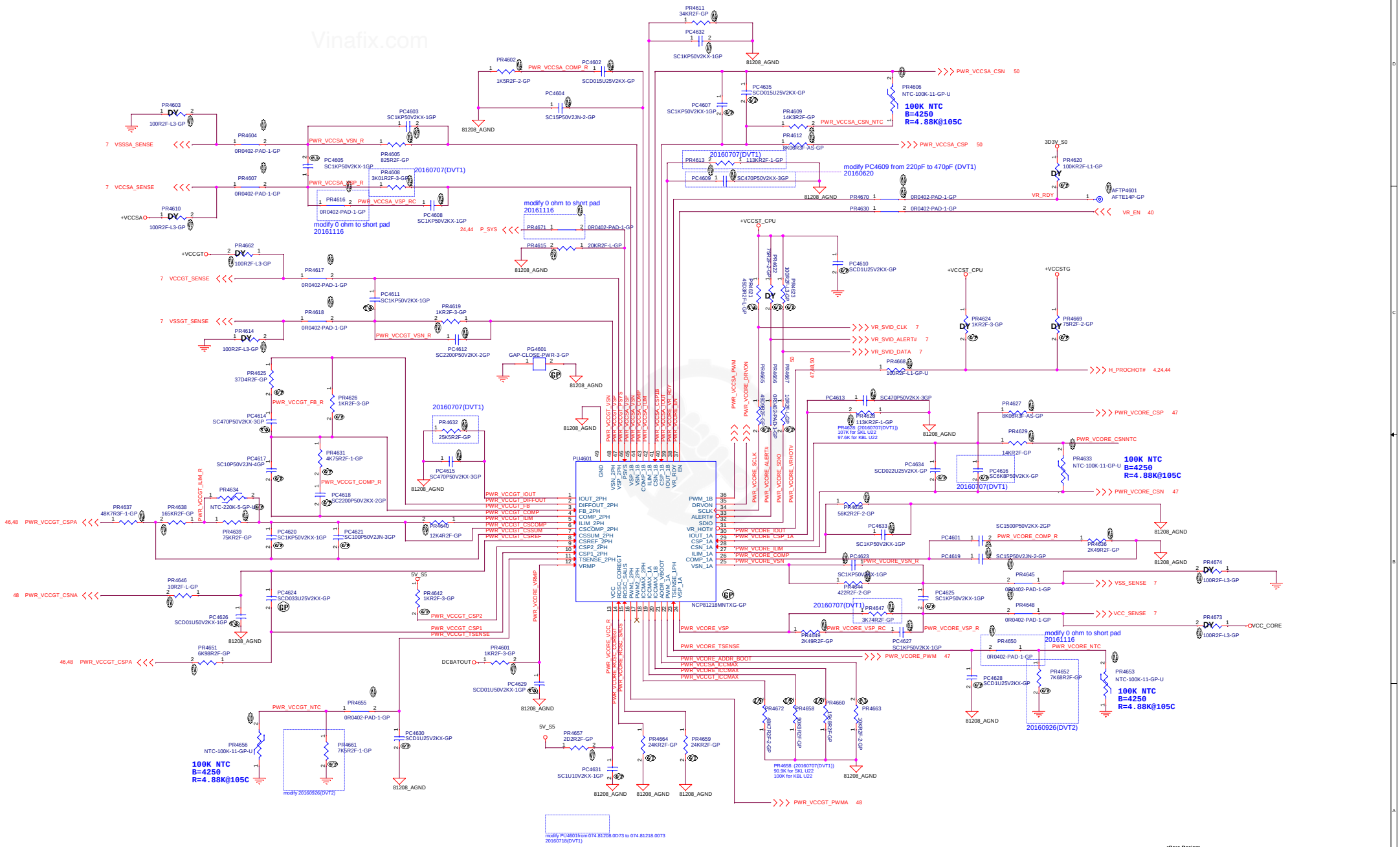
Title: CHARGER BQ24786

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 44 of 106


3D3V_S5
PWR_3D3V
DCBATOUT
PWR_DCBATOUT_3D3V
3D3V_AUX_S5
PR4504 0R2J-2-GP
PR4530 0R2J-2-GP
PWR_5V_EN_R
PR4501 0R0402-PAD-1-GP
PWR_5V_EN
PR4518 0R0402-PAD-2-GP
PR4502 0R0402-PAD-1-GP
PWR_3D3V_EN
40 3V_5V_EN
PWR_DCBATOUT_5V
PWR_5V
5V_S5
Design Current=5A
7.5A<OCP<9A
modify PL4501 from 3.3uH to 2.2uH (DVT1) 20160620
PL4501 IND-2D2UH-46-GP-U1
Cyntec 6.8 x 7.3 x 3.0
DCR: 18~20mOhm
Idc : 8A , Isat : 14A
TPS51225RUKR-GP
change to 074.06575.0A42 (DVT2)
modify 88.7K 20160629(DVT1)
modify DY->mount 20160621(DVT1)
Vo =2x(1+R1/R2) =2x(1+6.65/10) =3.33V
Design Current=7A
10.5A<OCP<12.6A
modify PL4502 part number for common part 20160620
PL4502 IND-2D2UH-46-GP-U1
Cyntec 6.8 x 7.3 x 3.0
DCR: 18~20mOhm
Idc : 8A , Isat : 14A
Vo =2x(1+R1/R2) =2x(1+15/10) =5V
17,40,52,54 3V_5V_POK
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
(Reserved)
Keystone 13.3"
X00
Wednesday, November 23, 2016
45
106

Main Func = CPU_CORE



<Core Design>

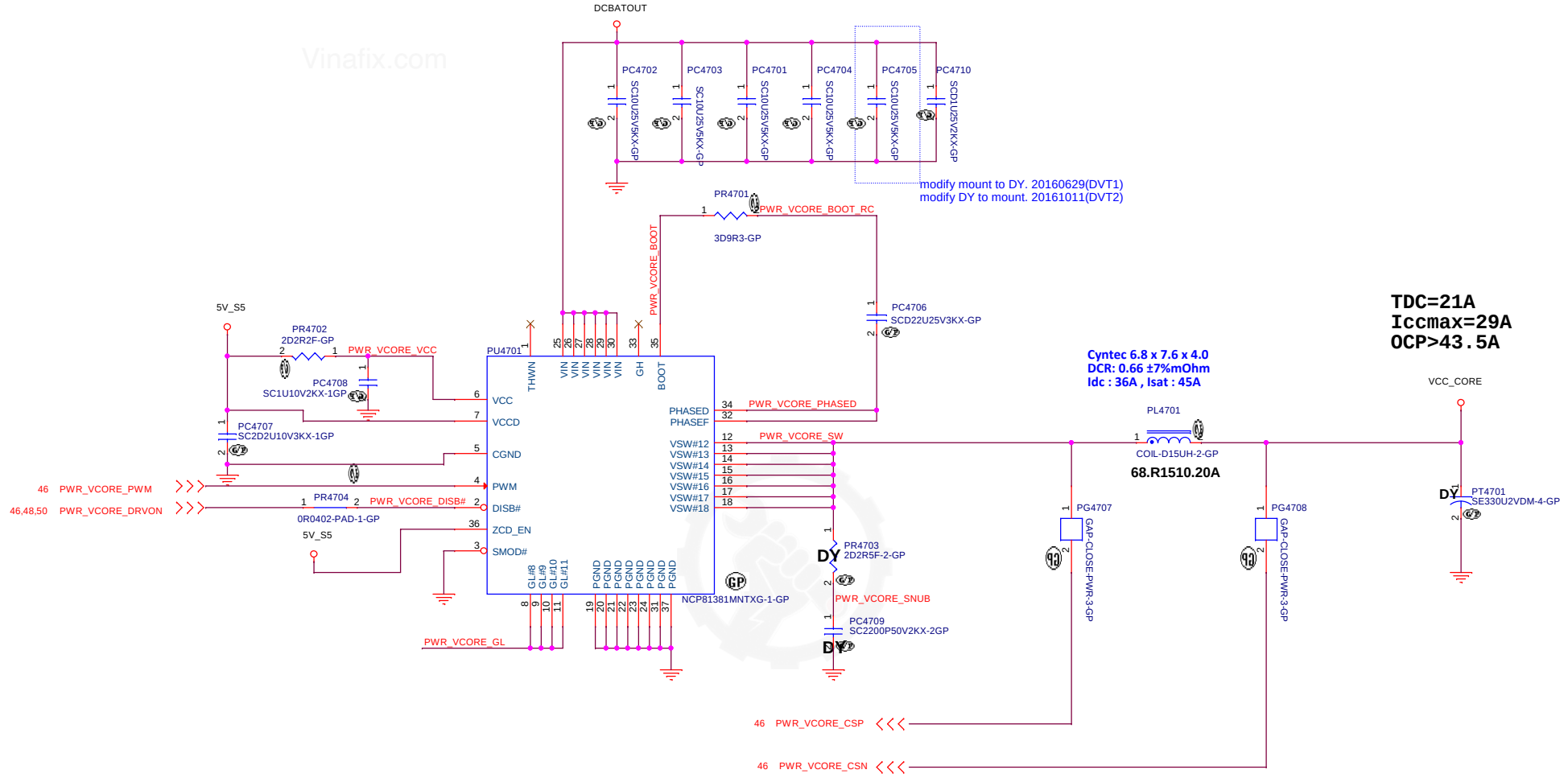
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 46 of 106

Main Func = CPU_CORE

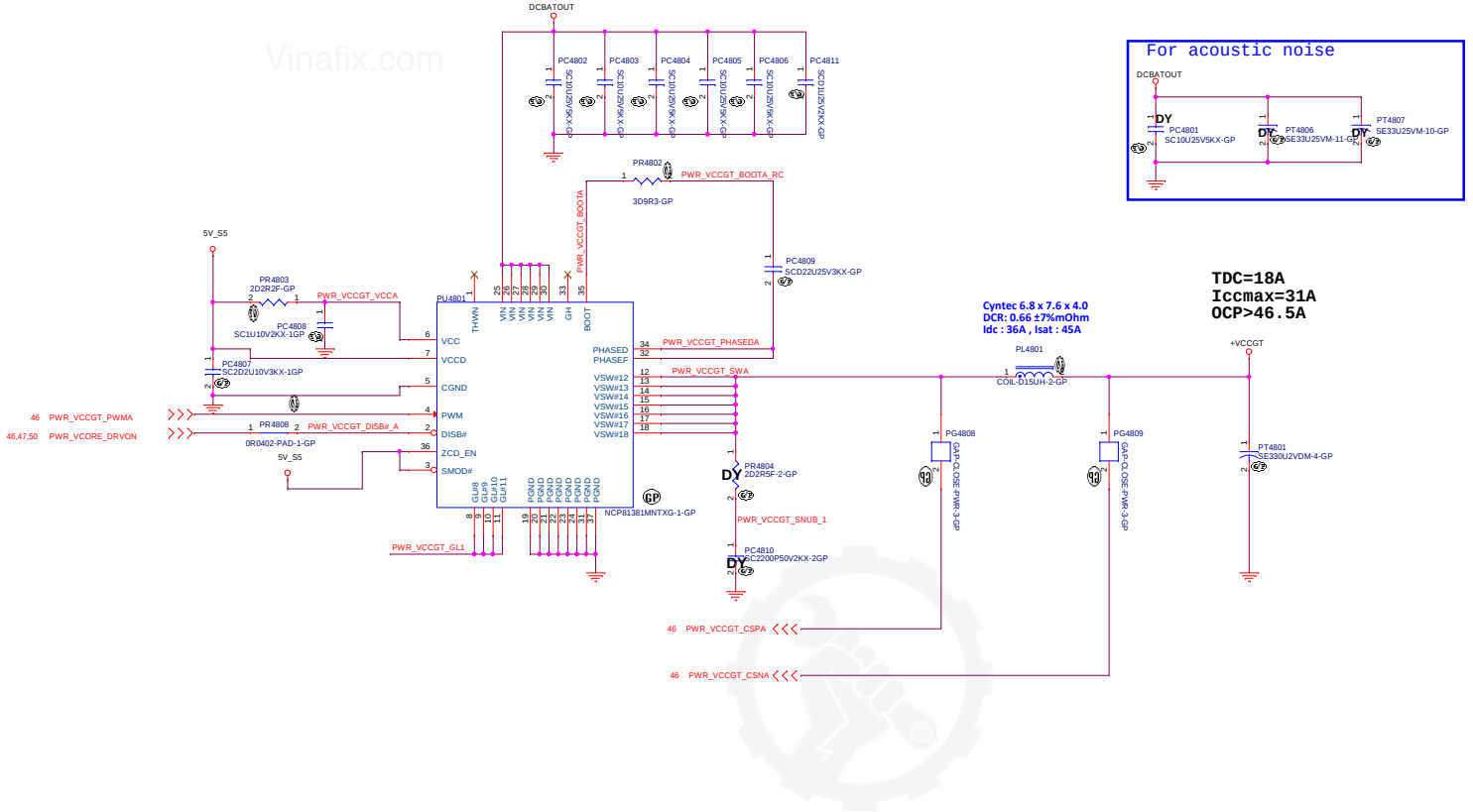


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81382MN_CPU_VCORE(2/3)	
Size A3	Document Number Keystone 13.3"	Rev X00
Date: Wednesday, November 23, 2016	Sheet 47 of 106	

Main Func = VCCGT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 48 of 106

<Core Design>

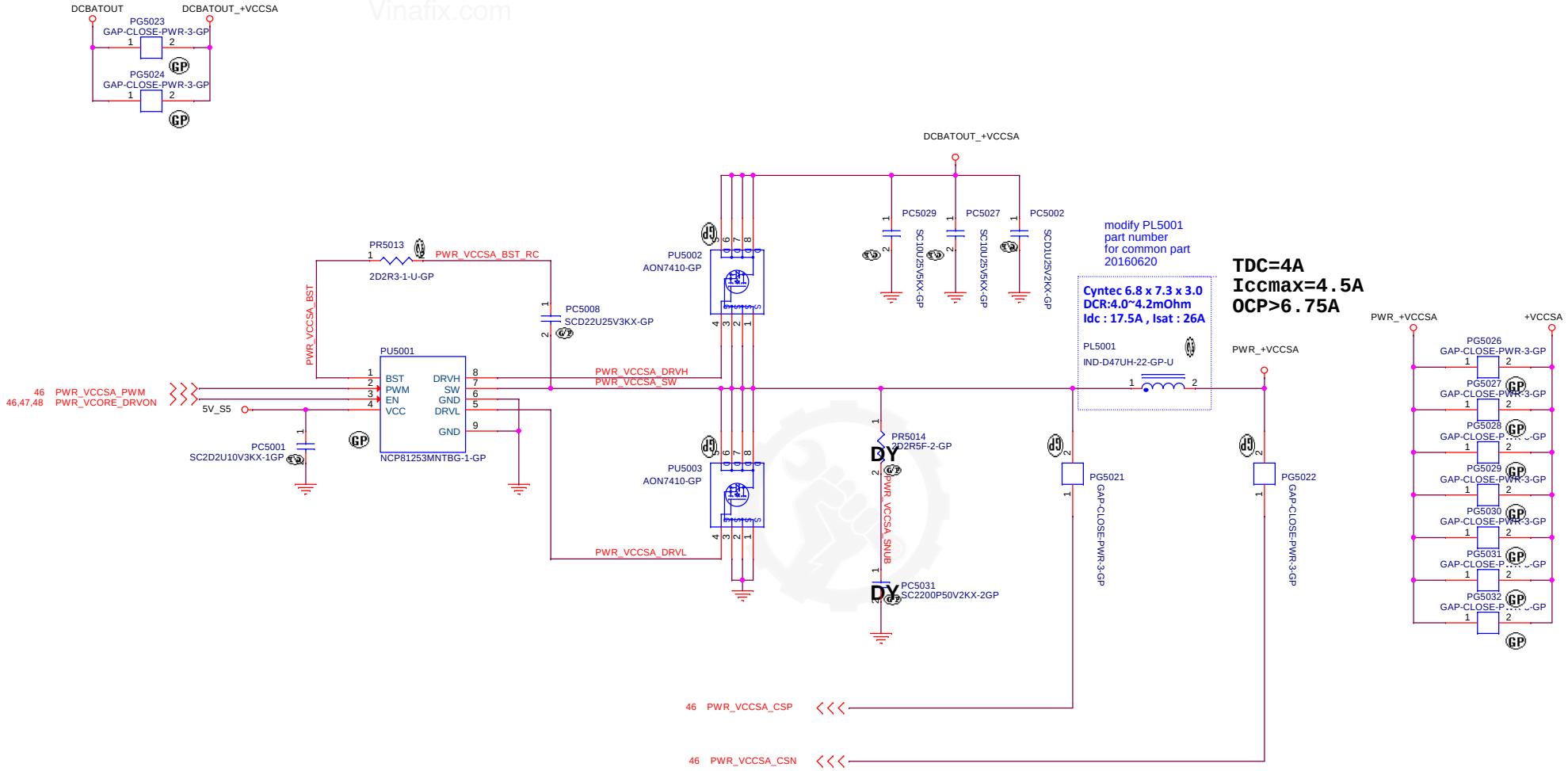
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 49 of 106

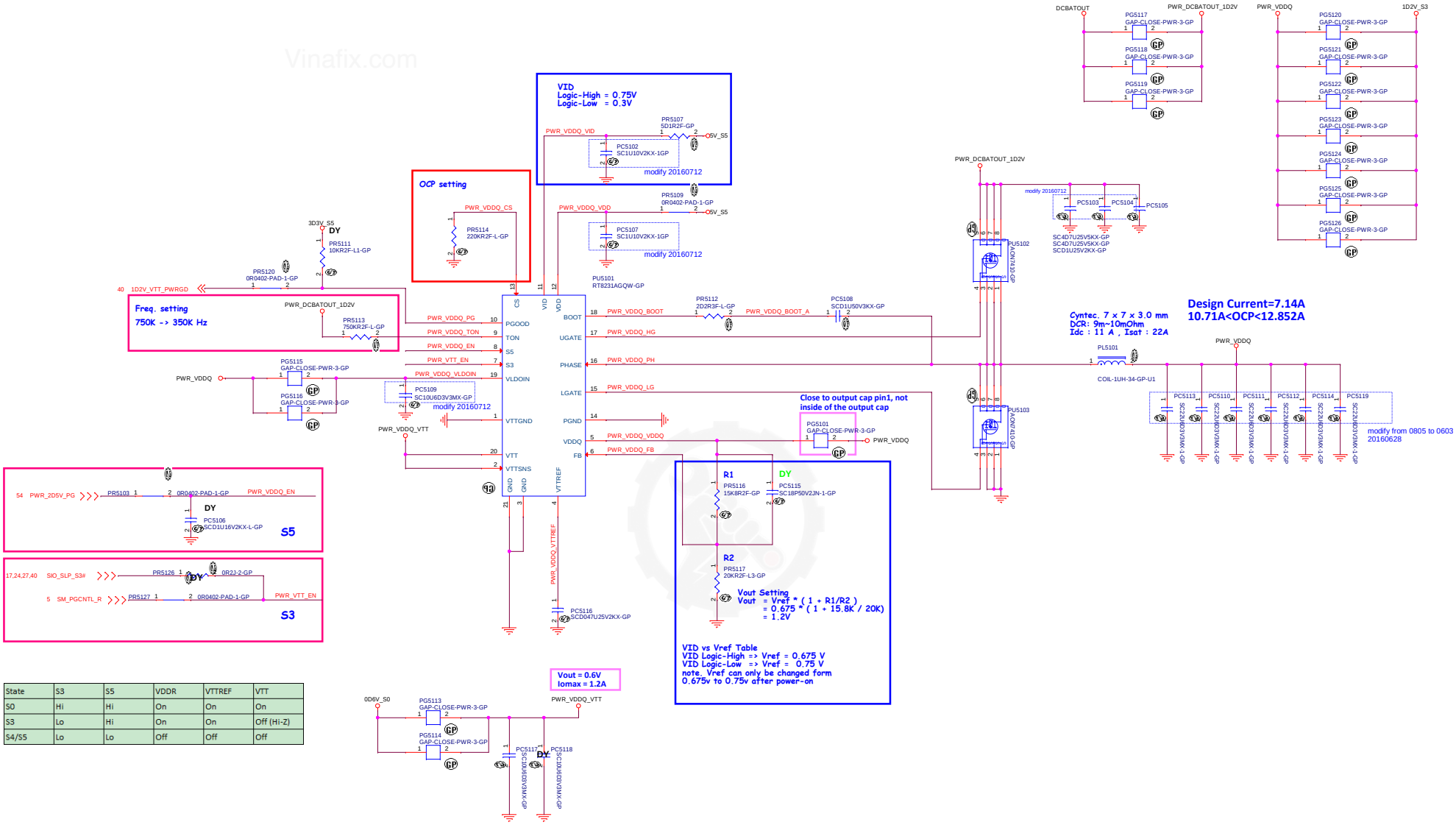
Main Func = CPU_CORE



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
VCCSA		
Size: A3	Document Number: Keystone 13.3"	Rev: X00
Date: Wednesday, November 23, 2016	Sheet 50 of 106	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

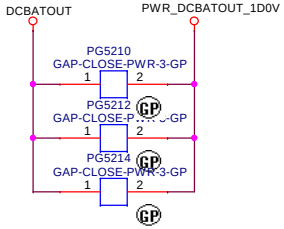
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

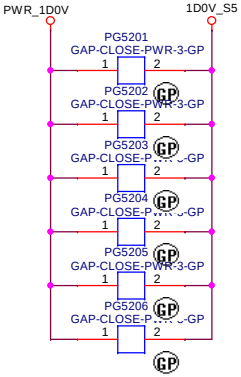
Title: (Reserved)

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

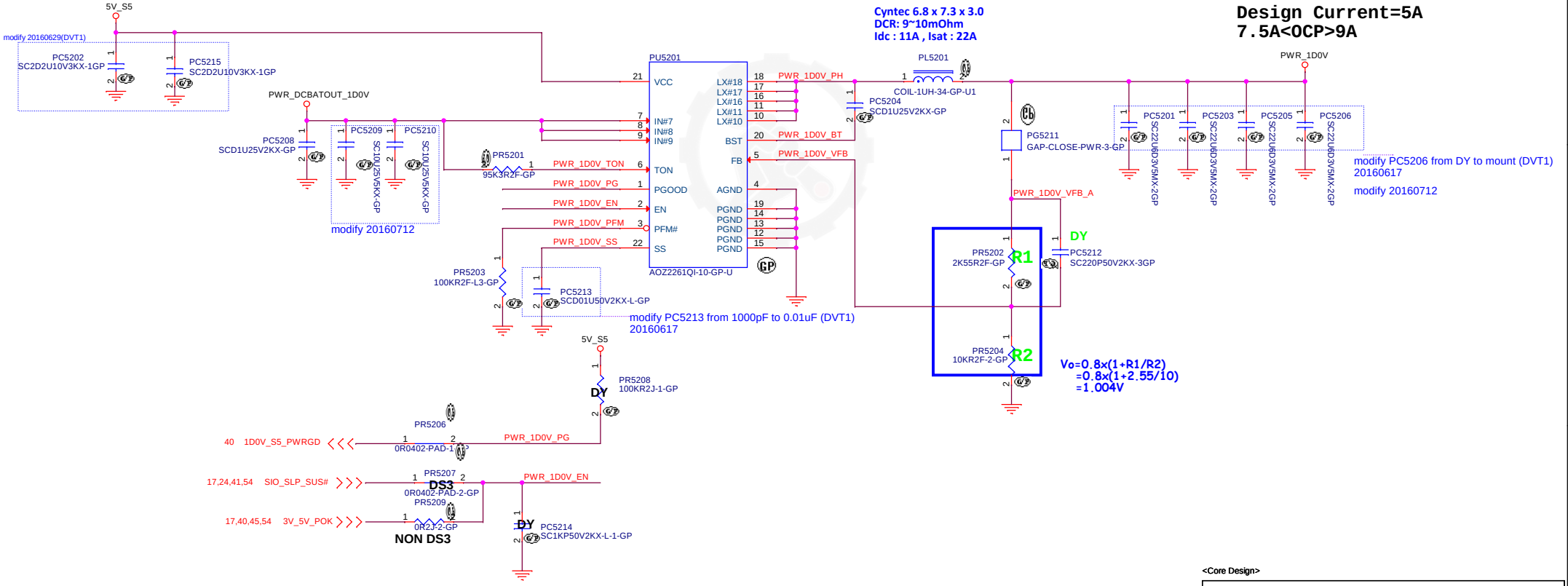
Date: Wednesday, November 23, 2016 | Sheet 51 of 106

SSID = PWR.Plane.Regulator_1D0V





AOZ2261 for 1D0V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Keystone 13.3"* | Rev: *X00*

Date: Wednesday, November 23, 2016 | Sheet 52 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

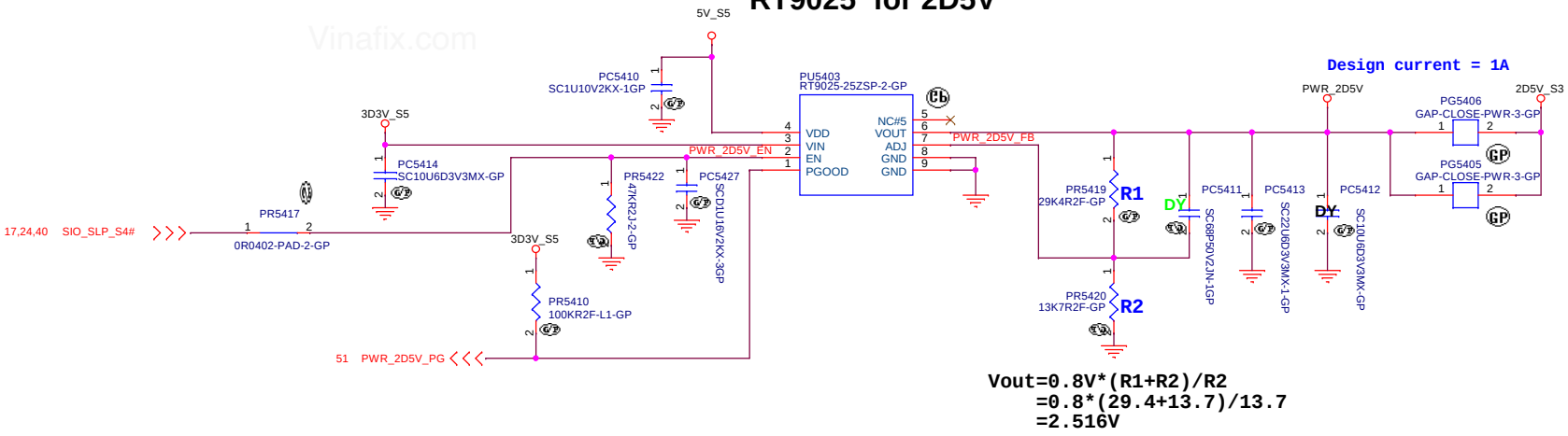
Title: ***(Reserved)***

Size	Document Number	Rev
A3	***Keystone 13.3"***	***X00***

Date: Wednesday, November 23, 2016 Sheet 53 of 106

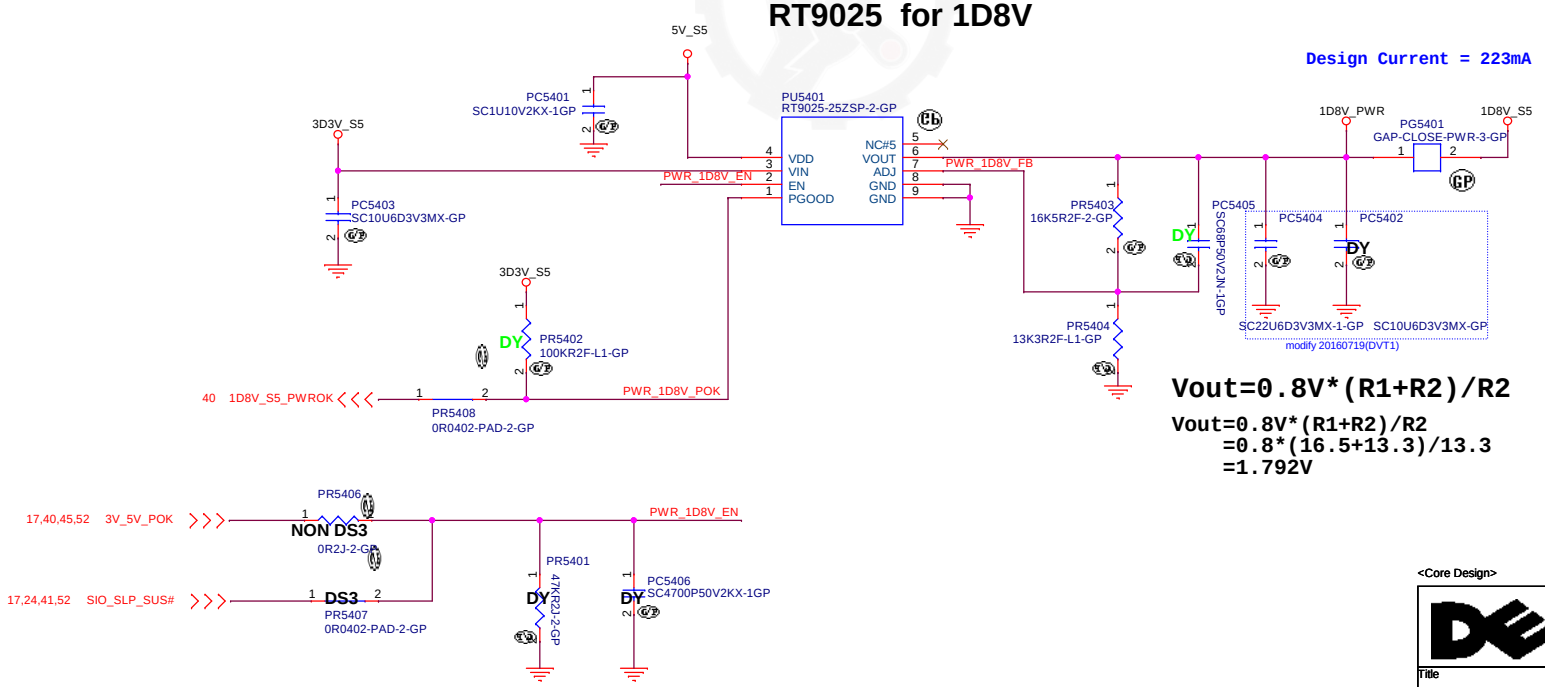
Main Func = 2D5V&1D8V

RT9025 for 2D5V



Vout=0.8V*(R1+R2)/R2
=0.8*(29.4+13.7)/13.7
=2.516V

RT9025 for 1D8V



Vout=0.8V*(R1+R2)/R2

Vout=0.8V*(R1+R2)/R2
=0.8*(16.5+13.3)/13.3
=1.792V

<Core Design>

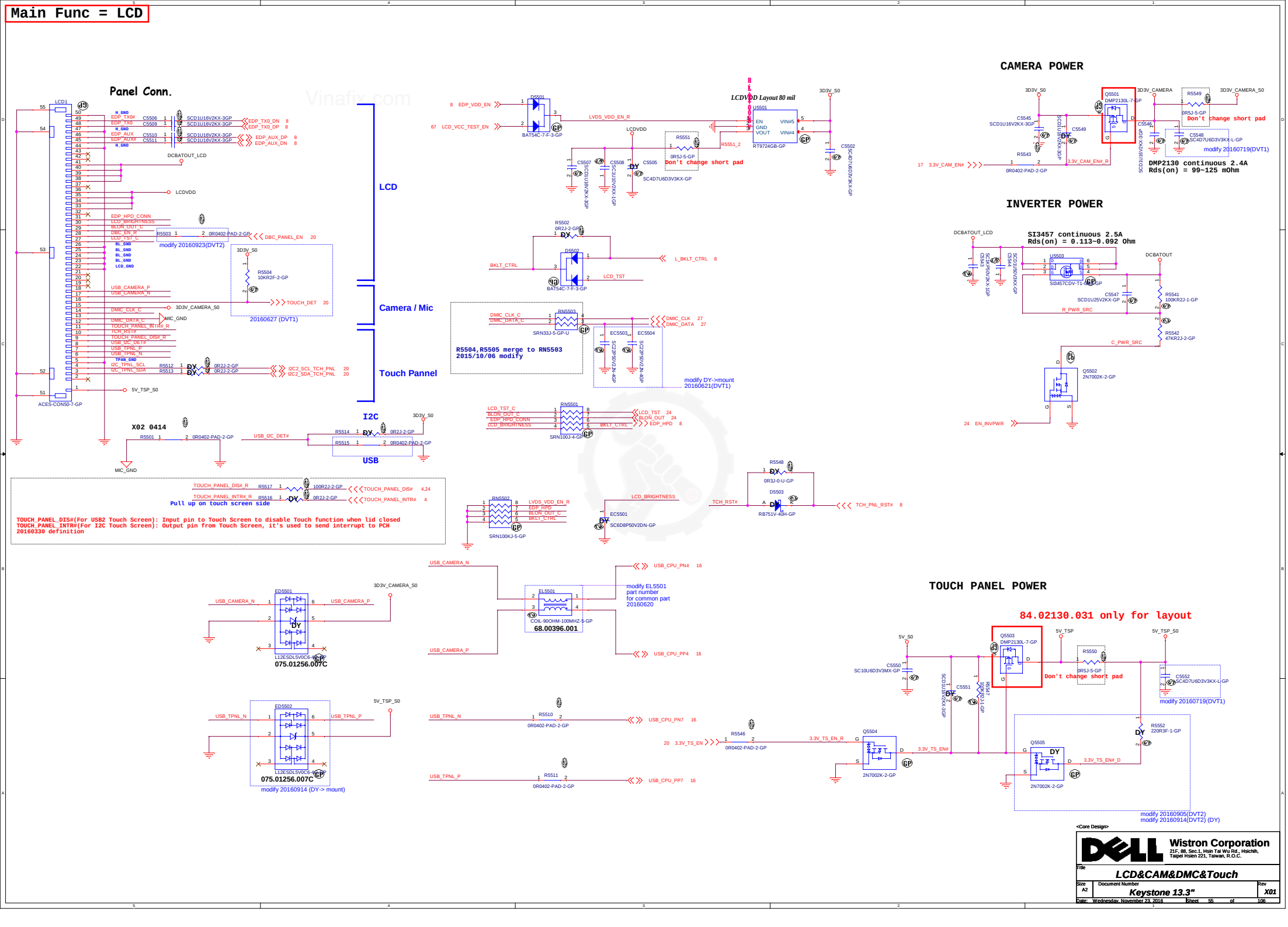
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	*Keystone 13.3"*	*X00*

Date: Wednesday, November 23, 2016 Sheet 54 of 106

Main Func = LCD



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: A2
Document Number: Keystone 13.3"
Rev: X01
Date: Wednesday, November 23, 2016
Sheet 55 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 56 of 106

Main Func = HDMI

8 HDMI_CLK#
8 HDMI_CLK
8 HDMI_DATA0#
8 HDMI_DATA0
8 HDMI_DATA1#
8 HDMI_DATA1
8 HDMI_DATA2#
8 HDMI_DATA2

C5702 1 — SCD1U16V2KX-3GP — HDMI_CLK#_R
C5703 1 — SCD1U16V2KX-3GP — HDMI_CLK_R
C5704 1 — SCD1U16V2KX-3GP — HDMI_DATA0#_R
C5705 1 — SCD1U16V2KX-3GP — HDMI_DATA0_R
C5706 1 — SCD1U16V2KX-3GP — HDMI_DATA1#_R
C5707 1 — SCD1U16V2KX-3GP — HDMI_DATA1_R
C5708 1 — SCD1U16V2KX-3GP — HDMI_DATA2#_R
C5709 1 — SCD1U16V2KX-3GP — HDMI_DATA2_R

5V_S0
Q5703
G
D
S
R5713 1 DY 2 100KR2J-1-GP
2N7002K-2-GP
HDMI_PLL_GND
RN5702 SRN470J-3-GP
RN5703 SRN470J-3-GP
R5718 DY 0R2J-2-GP

HDMI_CLK_R — R5701 — HDMI_CLK_R_C — 0R0402-PAD-2-GP
ER5714 150R2J-L1-GP-U
HDMI_CLK#_R — R5702 — HDMI_CLK#_R_C — 0R0402-PAD-2-GP
HDMI_DATA2_R — R5705 — HDMI_DATA2_R_C — 0R0402-PAD-2-GP
ER5715 150R2J-L1-GP-U
HDMI_DATA2#_R — R5706 — HDMI_DATA2#_R_C — 0R0402-PAD-2-GP

HDMI_DATA0_R — R5703 — HDMI_DATA0_R_C — 0R0402-PAD-2-GP
ER5717 150R2J-L1-GP-U
HDMI_DATA0#_R — R5704 — HDMI_DATA0#_R_C — 0R0402-PAD-2-GP
HDMI_DATA1_R — R5707 — HDMI_DATA1_R_C — 0R0402-PAD-2-GP
ER5716 150R2J-L1-GP-U
HDMI_DATA1#_R — R5708 — HDMI_DATA1#_R_C — 0R0402-PAD-2-GP

modify 20160921(DVT2)
R5714~R5717 rename ER5714~ER5717

remove R5709, F5701 (5V_HDMI_S0)
20160627(DVT1)

5V_S0
D5701 BAW56-9-GP
DDC_DATA_PH2
DDC_CLK_PH1
3D3V_S0
RN5701 SRN2K2J-1-GP
Q5702
2N7002KDW-GP
8 CPU_DP1_CTRL_CLK
8 CPU_DP1_CTRL_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI

modify
20160627(DVT1)
U5701
IN
OUT
GND
AP2331SA-7-GP
C5701 SCD1U16V2KX-3GP
5V_HDMI
C5710 SCD1U16V2KX-3GP

HDMI CONN
HDMI1
SKT-HDMI21-4-GP
HDMI_DATA2_R_C
HDMI_DATA2#_R_C
HDMI_DATA1_R_C
HDMI_DATA1#_R_C
HDMI_DATA0_R_C
HDMI_DATA0#_R_C
HDMI_CLK_R_C
HDMI_CLK#_R_C
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

3D3V_S0
Q5701 LMBT3904LT1G-GP
B HDMI_HPD_B
R5711 150KR2F-L-GP
R5710 200KR2F-L-GP
R5719
8 CPU_DP1_HPD
HDMI_HPD_E
R5712 10KR2J-3-GP
0R0402-PAD-2-GP

EMI Request:

ED5701 — RCLAMP0524P-2-GP
HDMI_DATA1#_R_C
HDMI_DATA1_R_C
HDMI_DATA2#_R_C
HDMI_DATA2_R_C

ED5702 — RCLAMP0524P-2-GP
HDMI_DATA0#_R_C
HDMI_DATA0_R_C
HDMI_CLK_R_C
HDMI_CLK#_R_C

ED5703 — RCLAMP0524P-2-GP
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI
Size: A3
Document Number: Keystone 13.3"
Rev: X00
Date: Wednesday, November 23, 2016
Sheet 57 of 106

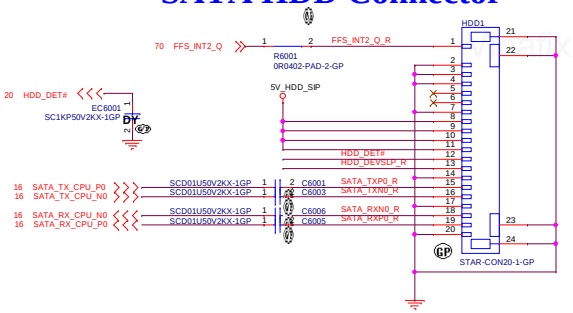
(Blanking)

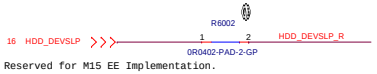
(Blanking)

Main Func = HDD

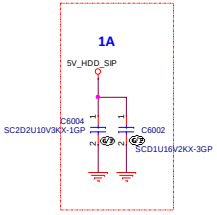
remove HDD1 pin5, pin6 3D3V_S0_HDD to NC (20160603)

SATA HDD Connector



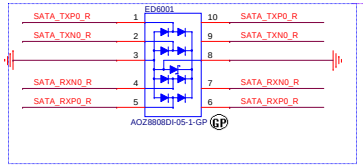


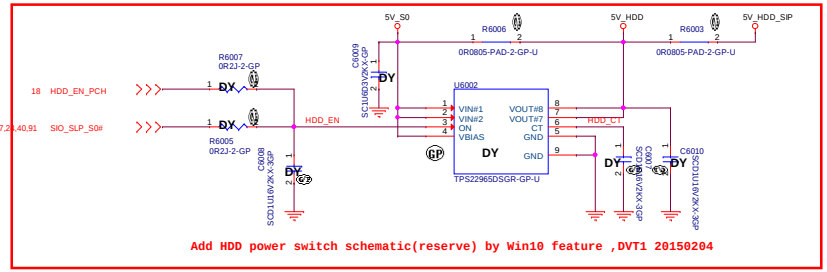
Reserved for M15 EE Implementation.



Close to HDD1
Modify at 20150922

Layout Note:
Place near HDD1





Add HDD power switch schematic(reserve) by Win10 feature ,DVT1 20150204

Add HDD power switch schematic(reserve), 20160201
remove 3D3V_S0_HDD power switch U6003 circuit. 20160603

Main Func = ODD

<Core Design>

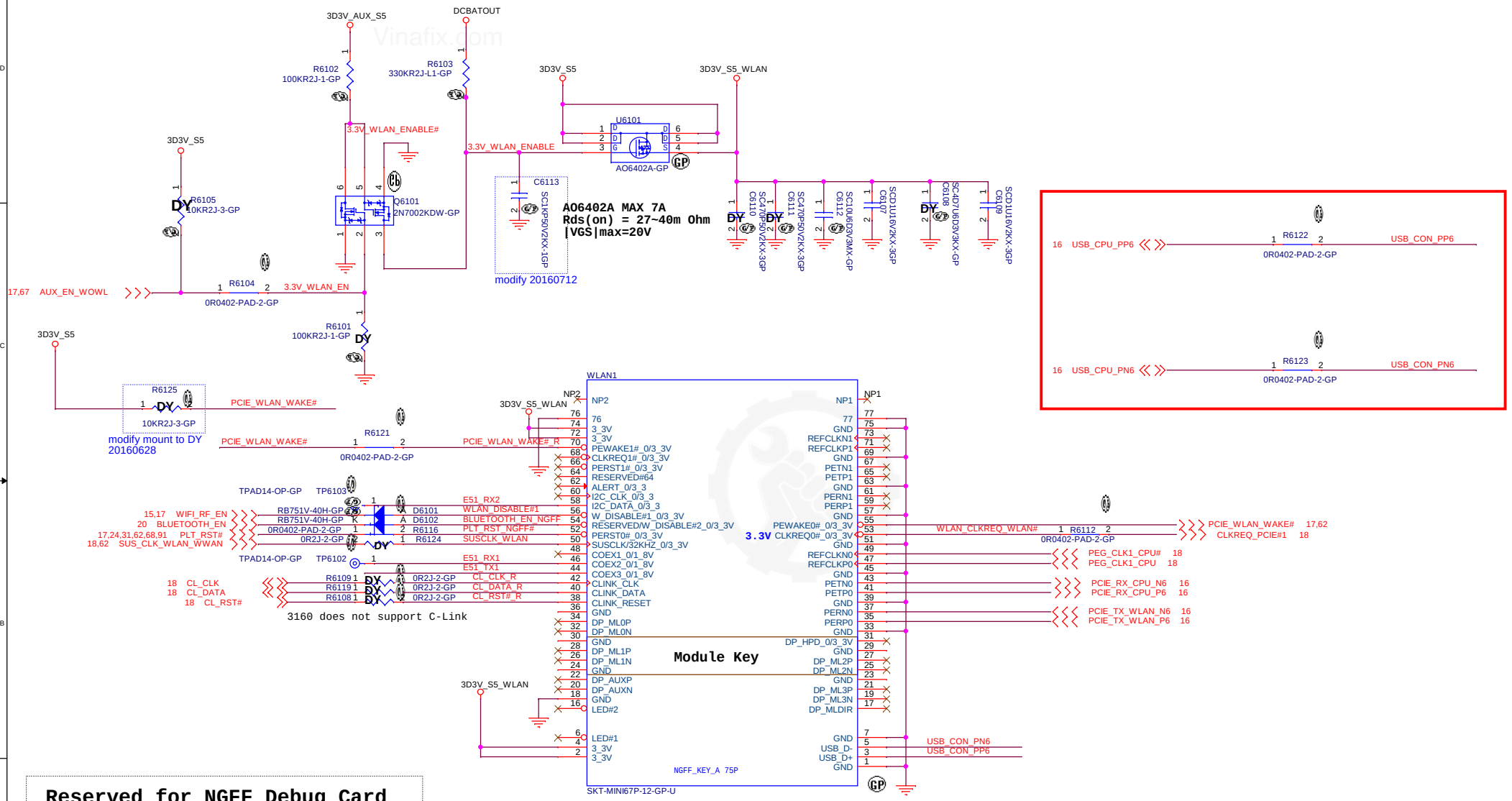
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF HDD/ODD

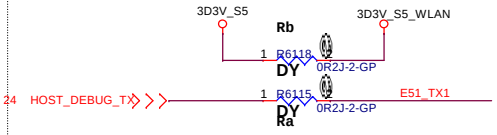
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 60 of 106

Main Func = WLAN

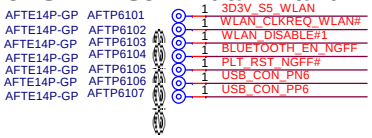


Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.

Support: Intel Dual Band Wireless-AC 3160



<Core Design>

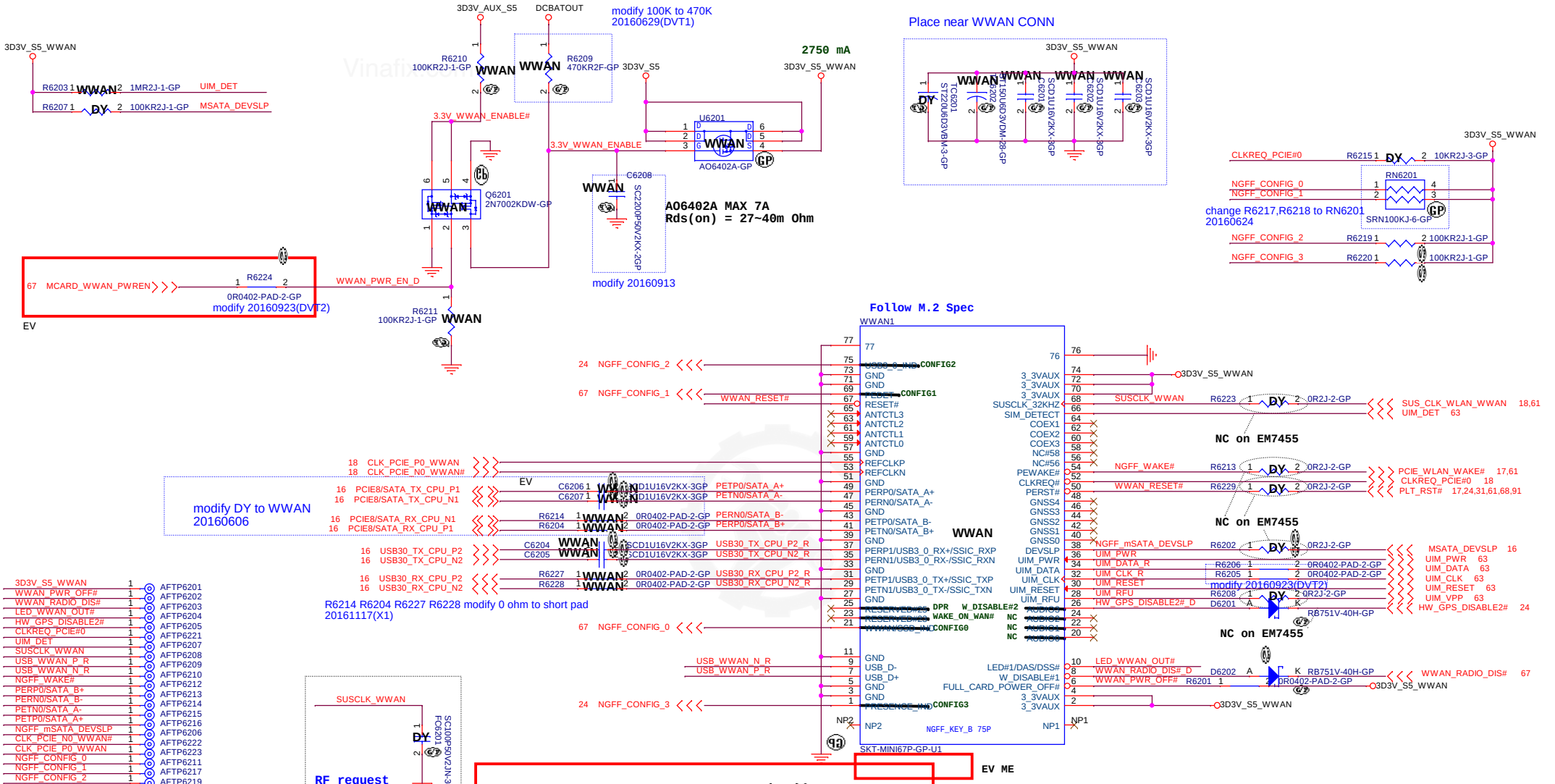
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 61 of 106

SSID = WIRELESS NGFF(WWAN/SSD)



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD – SATA
1	GND	NC	GND	GND	SSD - PCIe
8	NC	GND	GND	GND	WWAN
14	NC	GND	NC	NC	HCA - PCIe
15	NC	NC	NC	NC	No Module Present

<Core Design>

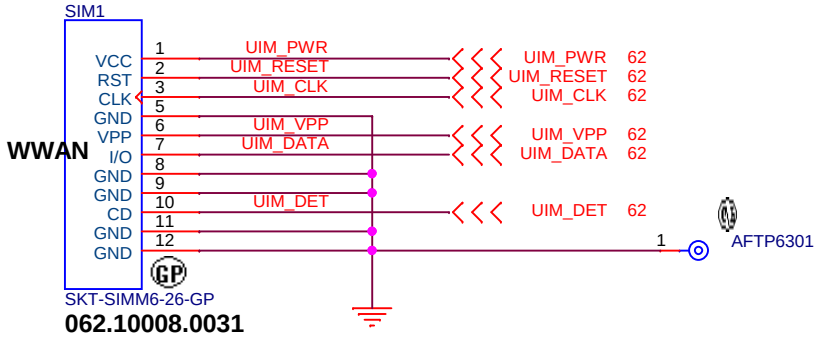
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF-WWAN/SSD

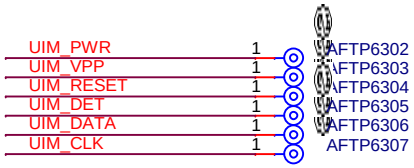
Size: A3 | Document Number: Keystone 13.3" | Rev: X00

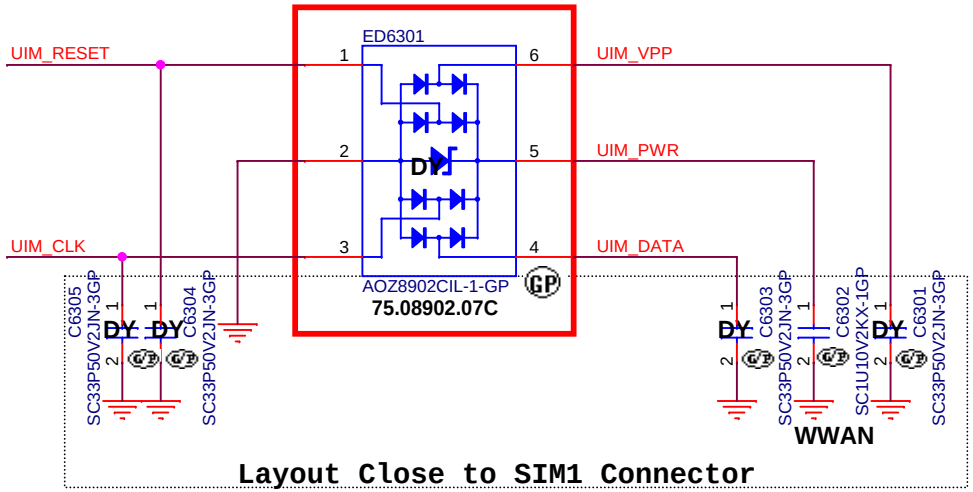
Date: Wednesday, November 23, 2016 | Sheet 62 of 106

SSID =WIRELESS



PIN	062.10008.0031 Micro SIM PinDefine
1	VCC
2	RST
3	CLK
5	GND
6	VPP
7	I/O
8	GND
9	GND
10	SIM Card Detect
11	GND
12	GND





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

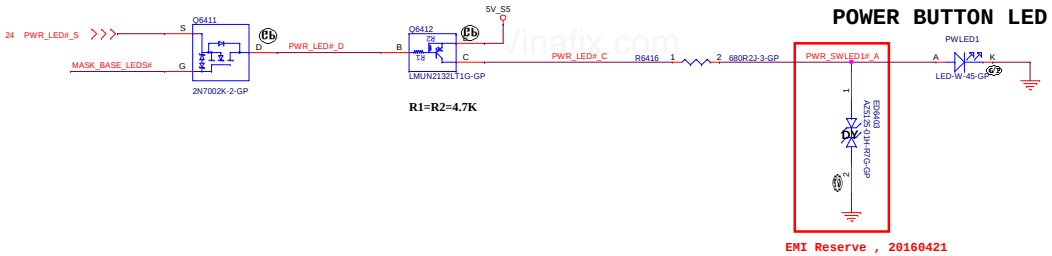
Title: uSIM

Size | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 63 of 106

Main Func = Power BTN

Power LED
LOW actived from KBC GPIO



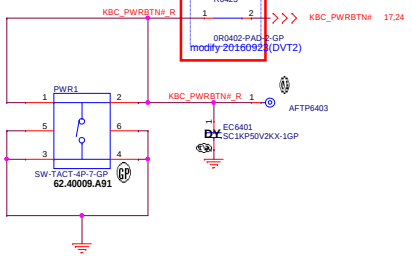
R1=R2=4.7K

POWER BUTTON LED

EMI Reserve , 20160421

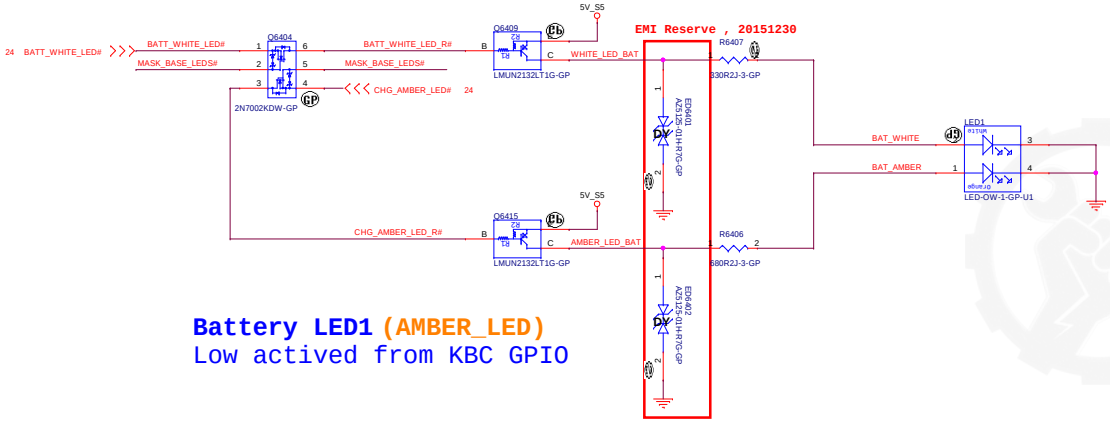
POWER BUTTON

Already reseve on EC side

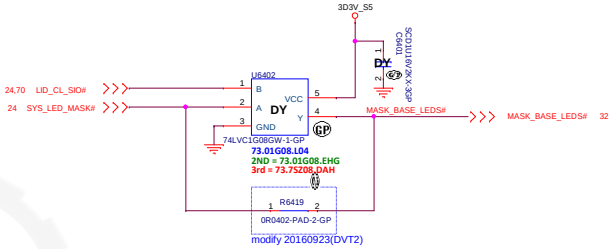


Main Func = Battery LED

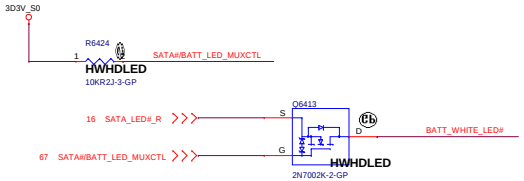
Battery LED2 (WHITE_LED)
Low actived from KBC GPIO



Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Main Func = HDD LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

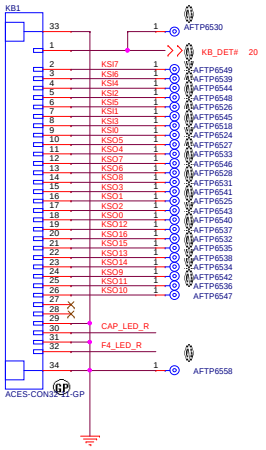
Title: *LED Board&Power Button*

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 64 of 106

Main Func = KB

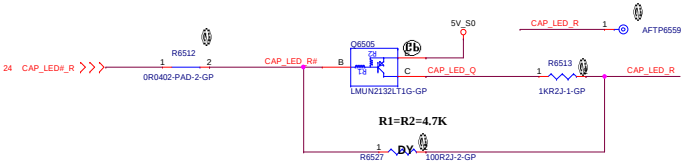
Internal KeyBoard Connector



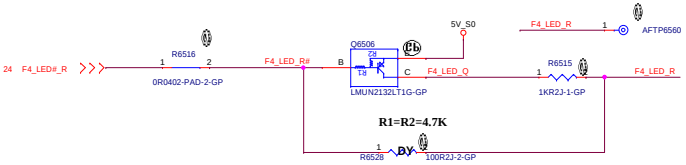
24 KSI[0..7]
24 KSO[0..16]

MB Pin NO.	Description	Module Pin NO.
1	Diagnostic	1
2	KSI[7]:S8	2
3	KSI[6]:S7	3
4	KSI[4]:S5	4
5	KSI[2]:S3	5
6	KSI[5]:S6	6
7	KSI[1]:S2	7
8	KSI[3]:S4	8
9	KSI[0]:S1	9
10	KSO[5]:D6	10
11	KSO[4]:D5	11
12	KSO[7]:D8	12
13	KSO[6]:D7	13
14	KSO[8]:D9	14
15	KSO[3]:D4	15
16	KSO[1]:D2	16
17	KSO[2]:D3	17
18	KSO[0]:D1	18
19	KSO[12]:D13	19
20	KSO[16]:D17	20
21	KSO[15]:D16	21
22	KSO[13]:D14	22
23	KSO[14]:D15	23
24	KSO[9]:D10	24
25	KSO[11]:D12	25
26	KSO[10]:D11	26
27	NC	27
28	NC	28
29	GND	29
30	Caps Lock LED	30
31	GND	31
32	F4 LED(MIC Mute LED)	32

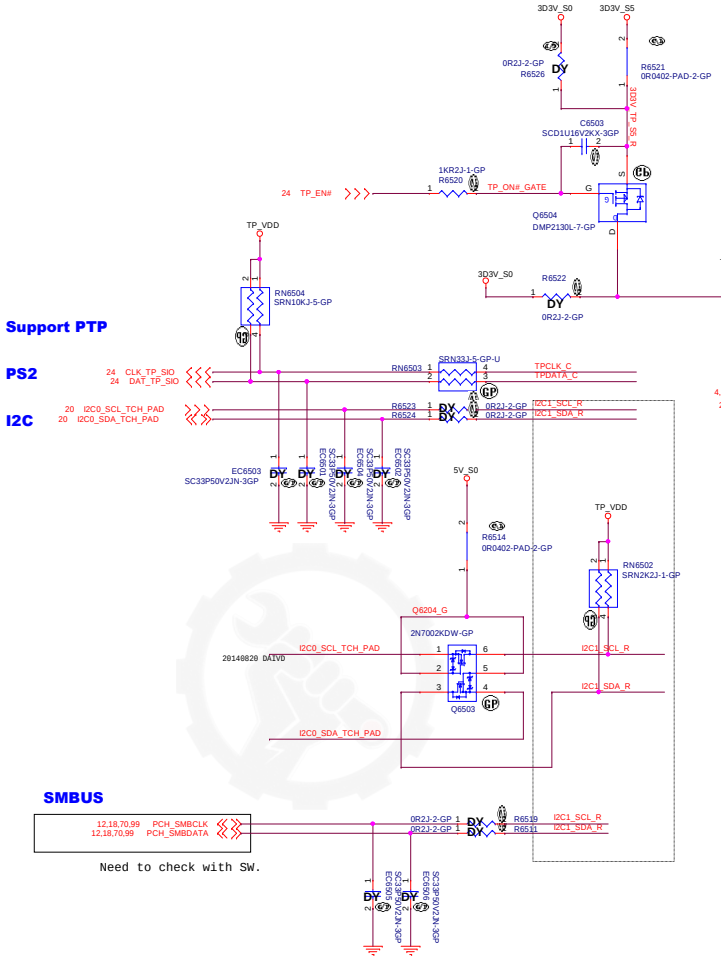
CAP LED Control
LOW actived from KBC GPIO

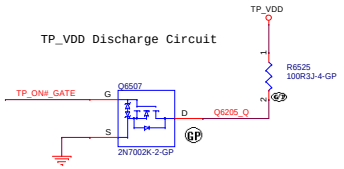


F4 LED (MIC Mute LED) Control
LOW actived from KBC GPIO

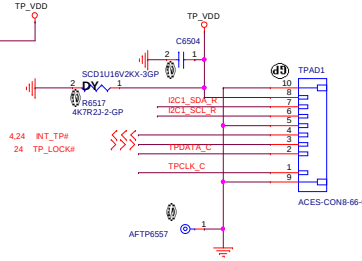


Main Func = TPAD

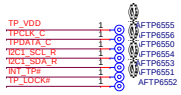




Precision Touch Pad Connector



Pin number	Pin name
8	VDD
7	DAT(I2C)
6	CLK(I2C)
5	GND
4	ATTN
3	GPIO
2	DAT(PS2)
1	CLK(PS2)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

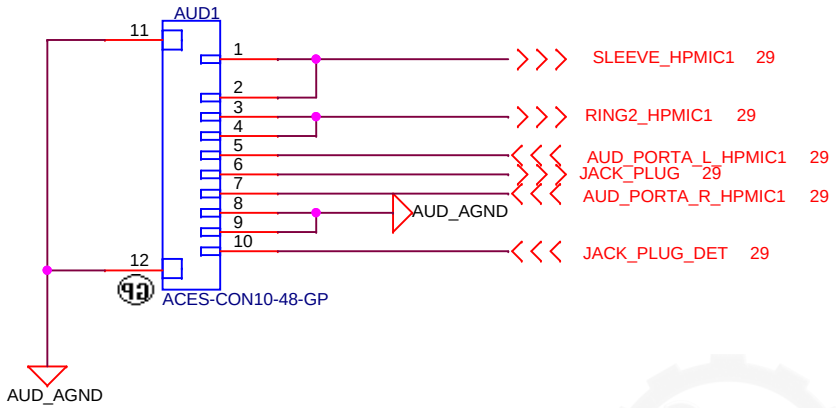
Title: Key Board&Touch Pad

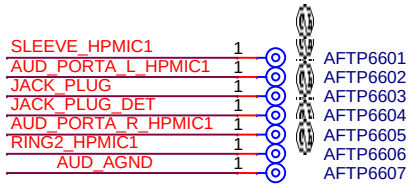
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

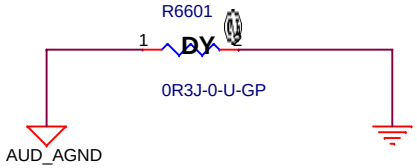
Date: Wednesday, November 23, 2016 | Sheet 65 of 106

Main Func = IO Connector

I/O Board Connector







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

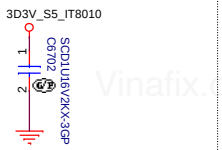
Title: *IO Board Connector*

Size	Document Number	Rev
A4	Keystone 13.3"	X00

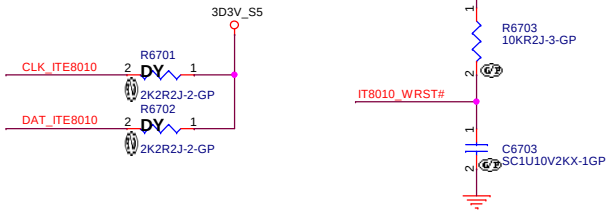
Date: Wednesday, November 23, 2016 Sheet 66 of 106

GPIO Expander

PLACE CLOSED TO PIN

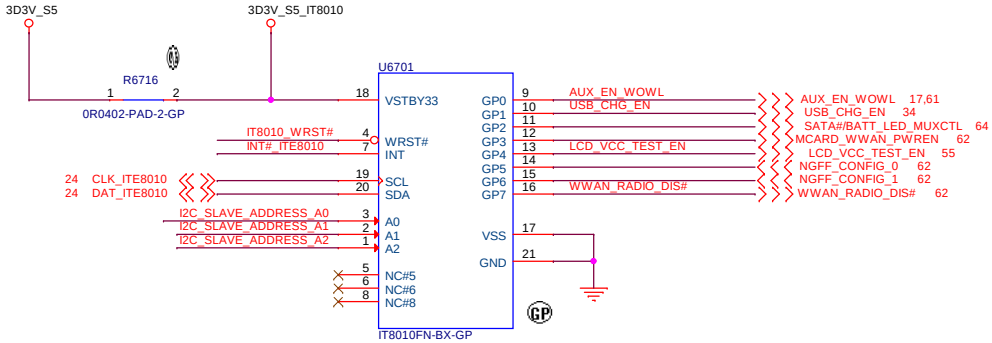


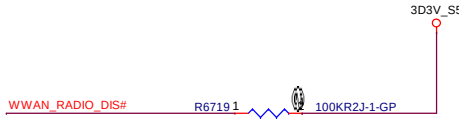
All I/O Signals are 3.3V CMOS Level



IT8010/IT8011/IT8012 difference

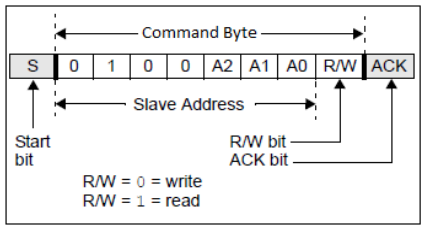
DEVICE	PIN8	PIN18
IT8010	NC	VSTBY33
IT8011	NC	VSTBY18
IT8012	VCOREI	VSTBY33



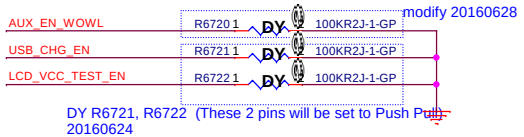


I2C SAD+Read/Write patterns

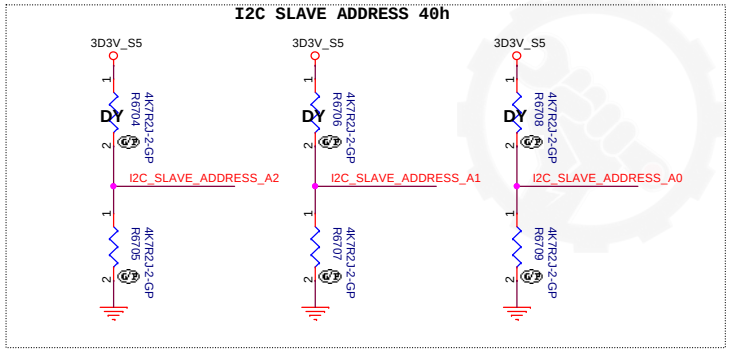
Command	SAD[7:4]	A[2]	A[1]	A[0]	R/W=	SAD+R/W
Read	0100	0	0	0	1	01000001 (41h)
Write	0100	0	0	0	0	01000000 (40h)
Read	0100	0	0	1	1	01000011 (43h)
Write	0100	0	0	1	0	01000010 (42h)
			•			
			•			
			•			
Read	0100	1	1	1	1	01001111 (4Fh)
Write	0100	1	1	1	0	01001110 (4Eh)



(U6701 DVT2 use 071.23008.0003. BOM control)



I2C SLAVE ADDRESS 40h

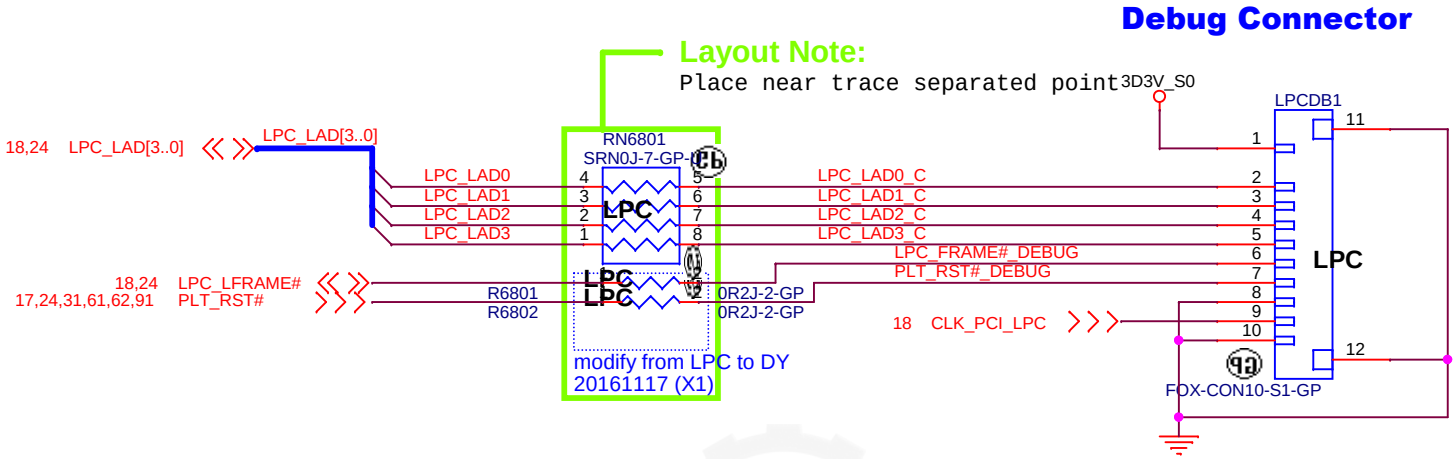


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPIO Expander (IT8010FN)	
Size: A3	Document Number: Keystone 13.3"	Rev: X00
Date: Wednesday, November 23, 2016	Sheet 67 of 106	

Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
A4	*Keystone 13.3"*	*X00*

Date: Wednesday, November 23, 2016 Sheet 68 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

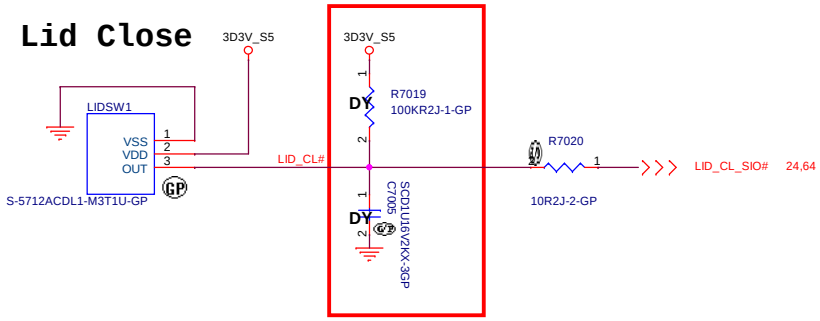
Size	Document Number	Rev
A3	***Keystone 13.3"***	***X00***

Date: Wednesday, November 23, 2016 Sheet 69 of 106

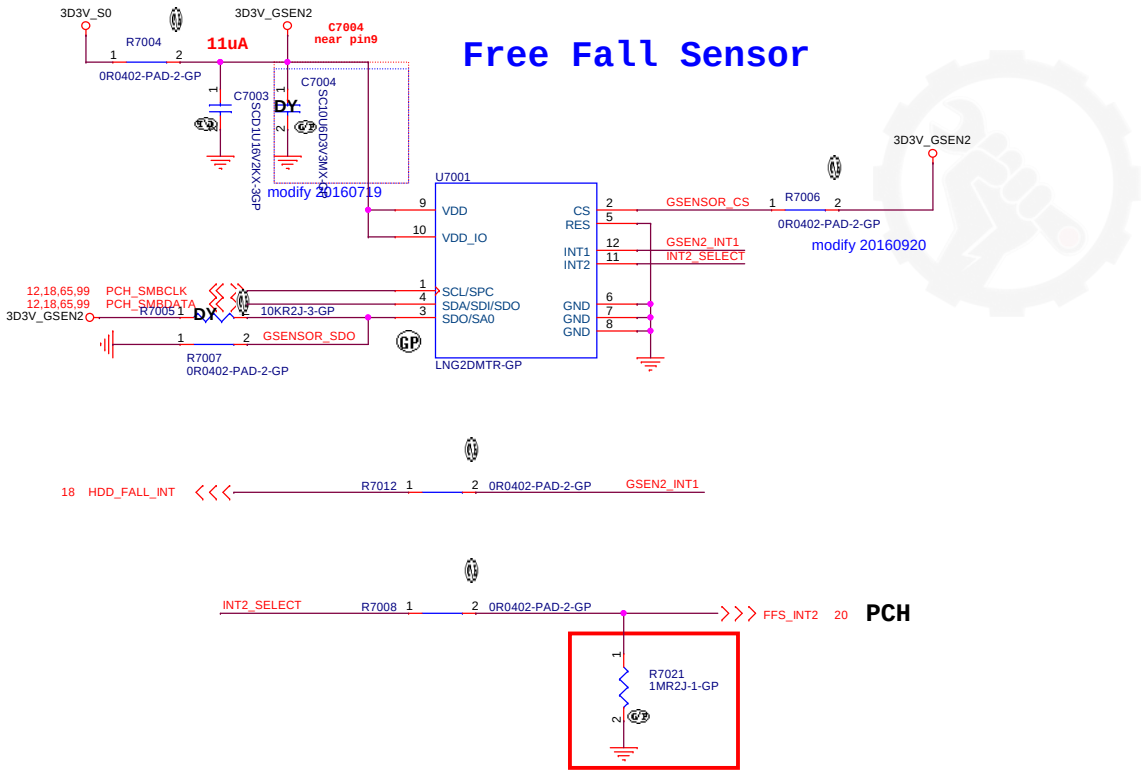
Main Func = Hall Sensor

LID sensoe

EV DY for LIDSW1 is PP



Free Fall Sensor

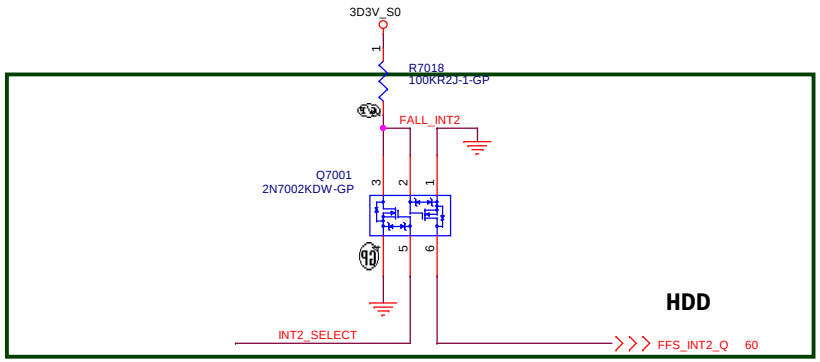


Vender suggest,reserve to prevent error trigger

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	System Sensor	
Size A3	Document Number: Keystone 13.3"	Rev: X00
Date: Wednesday, November 23, 2016	Sheet 70 of 106	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 71 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB3.0 PORT***

Size	Document Number	Rev
A3	***Keystone 13.3"***	***X00***

Date: Wednesday, November 23, 2016 Sheet 72 of 106

(Blanking)

(Blanking)

(Blanking)

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5)PEG

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 76 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 77 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(3/5)VRAM/F

Size	Document Number	Rev
A1	Keystone 13.3"	X00

Date: Wednesday, November 25, 2009 Sheet 78 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(4/5)GPIO/STRAP

Size	Document Number	Rev
Custom	Keystone 13.3"	X00

Date: Wednesday, November 21, 2007 Sheet 79 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU(5/5)PWR/GND*

Size	Document Number	Rev
Custom	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 80 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM1,2 (1/4)*

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 81 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM3,4 (2/4)*

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 82 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 83 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A3	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 84 of 106

Main Func = dGFX_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU CORE

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 85 of 106

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Discrete Power

Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 86 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Keystone 13.3"* | Rev: *X00*

Date: Wednesday, November 23, 2016 | Sheet 87 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Keystone 13.3"***	***X00***

Date: Wednesday, November 23, 2016 Sheet 88 of 106

Main Func = UnusedParts

for HS2 and HS3
34.4SE26.101:orcad symbol
34.4SE26.201:BOM main source
34.4SE26.301:BOM second source

34.41Y19.001

SPR1 SPRING-12-GP-U1
SPR2 SPRING-12-GP-U1
SPR3 SPRING-12-GP-U1
SPR4 SPRING-12-GP-U1

34.49U26.001

SPR5 SPRING-7-GP
SPR6 SPRING-7-GP

34.4YG18.201

HS1 STF236R128H101-2-GP
34.4YG18.101
for HS1
34.4YG18.101:orcad symbol
34.4YG18.201:BOM main source
34.4YG18.401:BOM second source

34.4SE26.201

HS2 STF237R113H62-5-GP
HS3 STF237R113H62-5-GP
34.4SE26.101 34.4SE26.101

ZZ.00PAD.D11

PAD3 HOLE256R115-GP
PAD2 HOLE256R115-GP
PAD7 HOLE256R115-GP
PAD2 modify..20160623

ZZ.00PAD.V71

PAD10 HOLE197R166-1-GP
PAD11 HOLE197R166-1-GP
PAD12 HOLE197R166-1-GP
PAD13 HOLE197R166-1-GP
PAD1 HOLE197R166-1-GP

ZZ.00PAD.J11

PAD4 HOLE296R166-GP
remove PAD5,PAD6..20160603
change PAD1 from ZZ.00PAD.J11 to ZZ.00PAD.V71..20160623

Del PAD9
20161123(X1)

ZZ.00PAD.JU1

PAD8 HOLE95-5P-S-GP
PAD6 HOLE95-5P-S-GP
modify 20160629(DVT1)

SSID = EMI

Mind the voltage rating of the caps.

AUD_AGND
EC8901 EC8902 EC8903 EC8904
modify DY->mount(EC8901,EC8903)
1Kp to 0.1u(EC8902,EC8904)
20160621(DVT1)

DCBATOUT
EC8905 EC8906 EC8907 EC8916
RF 20160627 RF 20160627
modify DY->mount
20160621(DVT1)

3D3V_S0
EC8909 EC8910 EC8911
modify DY->mount
20160621(DVT1)

3D3V_S5
EC8912
modify DY->mount
20160621(DVT1)

+DC_IN
EC8913
modify DY->mount
20160621(DVT1)

5V_S5
EC8914 EC8915
modify DY->mount
20160621(DVT1)

5V_S0
EC8916 EC8917
modify DY->mount
20160621(DVT1)

1D2V_S3
Change to 0.1uF at 20150427 for EMI

1D2V_S3
EC8920 EC8921 EC8922 EC8923 EC8924 EC8925
Change to 0.1uF at 20150427 for EMI

1D2V_S3
EC8933 EC8934 EC8935 EC8936 EC8937 EC8938
Change to 0.1uF at 20150427 for EMI
modify DY->mount
20160621(DVT1)

DCBATOUT
EC8927 EC8928

+VCCIO
EC8926 EC8930
Reserve EC8926, EC8930 for EMI, 20160427

DCBATOUT
EC8931 EC8932 EC8933 EC8934 EC8935 EC8936 EC8937 EC8938 EC8939 EC8940 EC8941 EC8942
EMI: reserve 8pcs cap for DCBATOUT
(TOP side)

DCBATOUT
EC8943 EC8944 EC8945 EC8946 EC8947 EC8948 EC8949 EC8950 EC8951
EMI: reserve 9pcs cap for DCBATOUT
(BOTTOM side)

AD+
EC8956
add EC8956 0.1uF
20160621(DVT1)

moat
5V_S0
DCBATOUT
EC8954 EC8955
modify for EMI
20160621(DVT1)

SSID = RF

Page.7
VCC_COREVCC_CORE +VCCGT +VCCGT 1D2V_S3 +VCCIO +VCCSA +VCCSFR
RF 20160624 RF 20160624

Page.10
VCC_CORE +VCCGT
RF 20160624

Page.12
1D2V_S3 1D2V_S3

Page.24
3D3V_S5 3D3V_S5_KBC

Page.34
USB30_VCCC

Page.35
USB30_VCCB

Page.43
USB30_VCCA AD+

Page.45
PWR_DCBATOUT_5V PWR_5V PWR_DCBATOUT_3D3V PWR_3D3V
RF 20160624 RF 20160624 RF 20160624

Page.47
DCBATOUT

Page.48
VCC_CORE DCBATOUT
RF 20160624

Page.50
DCBATOUT_+VCCSA
RF 20160624

Page.51
PWR_DCBATOUT_1D2V PWR_VDDQ
RF 20160624 RF 20160624

Page.52
5V_S5 PWR_DCBATOUT_1D0V
RF 20160624

Page.54
PWR_1D0V 5V_S5 3D3V_S5 PWR_2D5V 5V_S5 3D3V_S5
RF 20160624 RF 20160624 RF 20160624

Page.55
1D8V_PWR 3D3V_S0 LCDVDD DCBATOUT_LCD
RF 20160624 RF 20160624 RF 20160624 RF 20160624

Page.57
LCDVDD 3D3V_CAMERA_S0 5V_TSP_S0 5V_HDMI
modify
20160627(DVT1)

Page.60

Page.61
5V_HDD_SIP 3D3V_S5 3D3V_S5_WLAN 3D3V_S5_WLAN 3D3V_S5_WLAN
RF 20160624

Page.62
3D3V_S5_WWAN 3D3V_S5_WWAN 3D3V_S5 3D3V_S5_WWAN

Page.99
1D0V_S5 1D0V_S5 DCBATOUT DCBATOUT DCBATOUT DCBATOUT
RF 20160624 RF 20160624 RF 20160624 RF 20160624

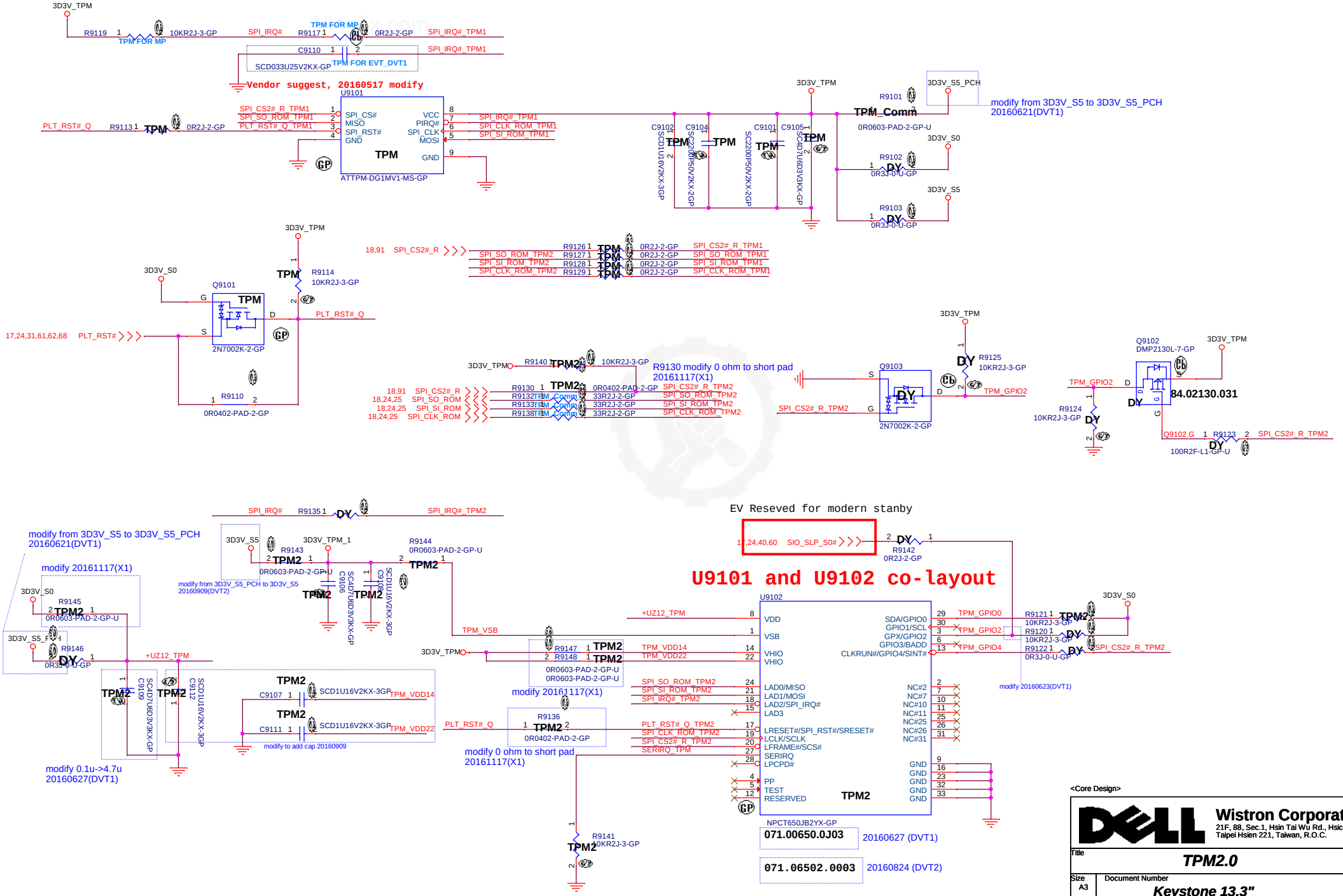
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: Keystone 13.3" | Rev: X00
Date: Wednesday, November 23, 2016 | Sheet 89 of 106

(Blanking)

SSID = TPM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPM2.0	
Size A3	Document Number Keystone 13.3"	Rev X00
Date: Wednesday, November 23, 2016	Sheet 91 of 106	

(Blanking)

(Blanking)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *(Reserved)*	
Size: A3	Document Number: *Keystone 13.3"* — Rev: *X00*
Date: Wednesday, November 23, 2016	Sheet 93 of 106

(Blanking)

(Blanking)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *(Reserved)*	
Size: A3	Document Number: *Keystone 13.3"* — Rev: *X00*
Date: Wednesday, November 23, 2016	Sheet 95 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

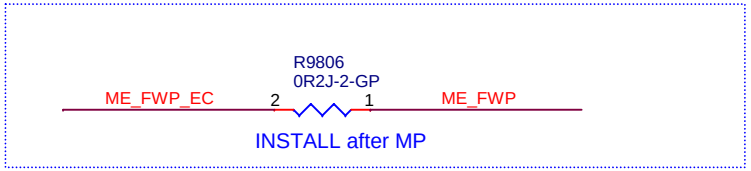
Title: *(Reserved)*

Size	Document Number	Rev
A3	*Keystone 13.3"*	*X00*

Date: Wednesday, November 23, 2016 Sheet 96 of 106

(Blanking)

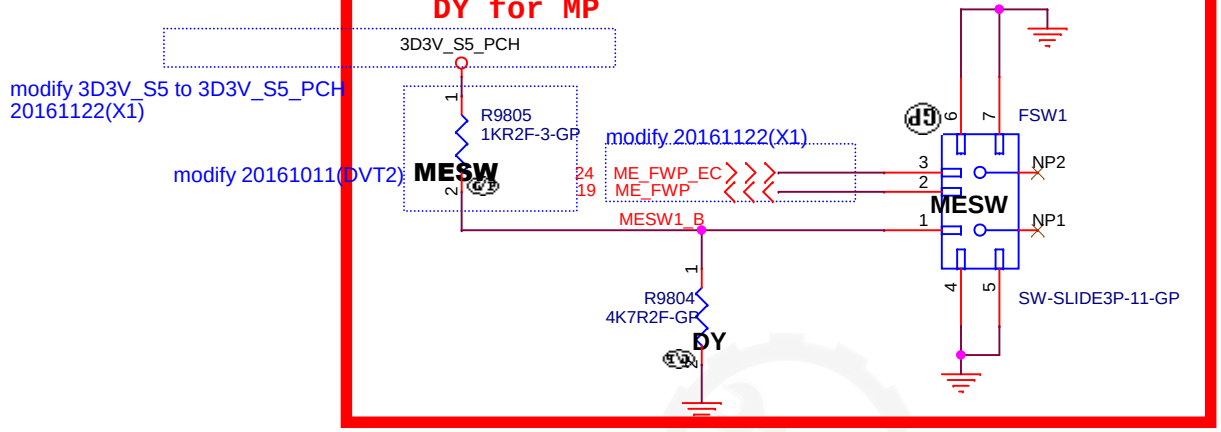
Main Func = Firmware SW



add 0 ohm
20161122(X1)

Firmware SW

Default setting:pull LOW
DY for MP



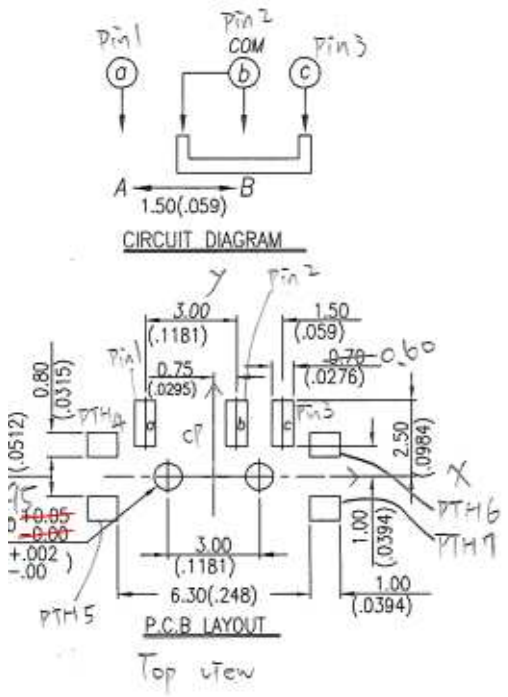
FSW1 change from 62.40018.691 to 62.40018.641
20160623(DVT1)

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

modify 20161122(X1)

modify 20161122(X1)

*Symbol same as 62.40018.461.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Firmware SW***

Size	Document Number	Rev
A4	**Keystone 13.3"**	**X00**

Date: Wednesday, November 23, 2016 Sheet 98 of 106

Main Func = Debug

CPU XDP

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<0>

CFG0 — R9908 1KR2J-1-GP — FIVR_EN_R

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>

CFG3 — R9902 1KR2J-1-GP — XDP_PRSNT_PIN1

17 PM_RSMRST# — R9904 1KR2J-1-GP — PM_RSMRST_PWRGD_XDP

17,24 SIO_PWRBTN# — R9926 0R2J-2-GP — BP_PWRGD_RST#

modify 20160628

C9901 SCD1U16V2KX-3GP

C9903 SCD1U16V2KX-3GP

3D3V_S5 — R9909 3KR2J-2-GP — 18 SPI0_MOSI_XDP

12,18,65,70 PCH_SMBDATA — R9911 0R2J-2-GP — XDP_SMBDAT
12,18,65,70 PCH_SMBCLK — R9912 0R2J-2-GP — XDP_SMBCLK

18 PCIE_CLK_XDP_P — R9913 0R2J-2-GP — PCIE_CLK_XDP_R_P
18 PCIE_CLK_XDP_N — R9923 0R2J-2-GP — PCIE_CLK_XDP_R_N

modify 20160712

6 CFG[19:0] — CFG[19:0]
4 XDP_BPM[3:0] — XDP_BPM[3:0]

XDP_BPM2 — TP9901 TPAD14-OP-GP
XDP_BPM3 — TP9902 TPAD14-OP-GP

+VCCIO — R9906 150R2J-L1-GP-U — FIVR_EN_R

XDP_PRSNT_PIN1

16 XDP_PREQ#
16 XDP_PRDY# — XDP_PRDY#

XDP1 — STC-CONN60A-HSD01

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19

XDP_BPM0 XDP_BPM1

PM_RSMRST_PWRGD_XDP
BP_PWRGD_RST#
FIVR_EN_R
SPI0_MOSI_XDP
XDP_SMBDAT
XDP_SMBCLK
XDP_TCLK1

4 XDP_TCLK

PCIE_CLK_XDP_R_P
PCIE_CLK_XDP_R_N
TP_PMODE_XDP_RST_R_N
XDP_DBRESET#
PCH_JTAG_TDO

XDP_TRST# 4
XDP_TDI 4
XDP_TMS 4
XDP_SPI0_IO2 18

(#543016)Routing of this signal to CFG[0] is OPTIONAL.

1D0V_S5_XDP

EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.

1D0V_S5 — R9928 0R3J-0-U-GP — 1D0V_S5_XDP
modify 20160628

1D0V_S5_XDP — R9927 0R2J-2-GP — +V1.00A_XDP
modify 20160628

C9902 SCD1U16V2KX-3GP
C9904 SCD1U16V2KX-3GP

PLACE THIS NEAR CPU XDP CONNECTOR

C9905 SCD1U16V2KX-3GP

1D0V_S5_XDP — R9925 0R2J-2-GP — XDP_DBRESET# 17
modify 20160712

3D3V_S5 — R9929 100KR2J-1-GP — XDP_SPI0_IO2 — R9931 0R2J-2-GP

+V1.00A_XDP — R9932 1K5R2J-3-GP — 6 ITP_PMODE

(#544669 Rev0.52) NC.

R9933 0R2J-2-GP — TP_PMODE_XDP_RST_R_N
modify 20160712

(#544669)

XDP_TCLK1 — R9914 0R2J-2-GP — PCH_JTAG_TCK 4
XDP_TCLK — R9915 0R2J-2-GP — XDP_TCK_JTAGX 4
4 XDP_TDO_CPU — R9919 0R2J-2-GP — PCH_JTAG_TDO 4
XDP_TDI — R9916 0R2J-2-GP — PCH_JTAG_TDI 4
XDP_TMS — R9917 0R2J-2-GP — PCH_JTAG_TMS 4

modify 20160628

<Core Design>

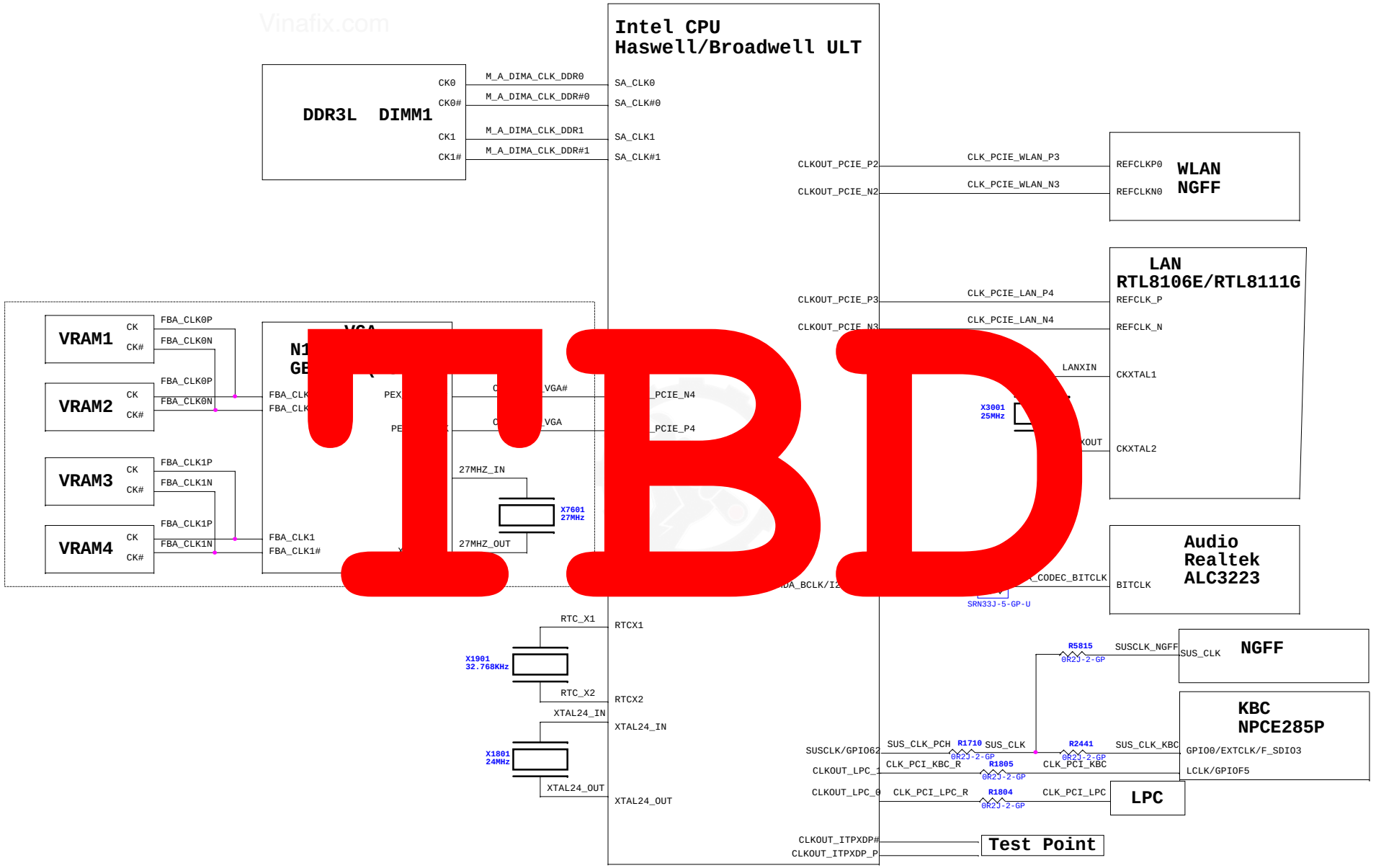
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_XDP;PCH_XDP

Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 99 of 106

CLK Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CLK Block Diagram	
Size: A2	Document Number: Keystone 13.3"	Rev: X00
Date: Wednesday, November 23, 2016	Sheet 100 of 106	

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

<Core Design>

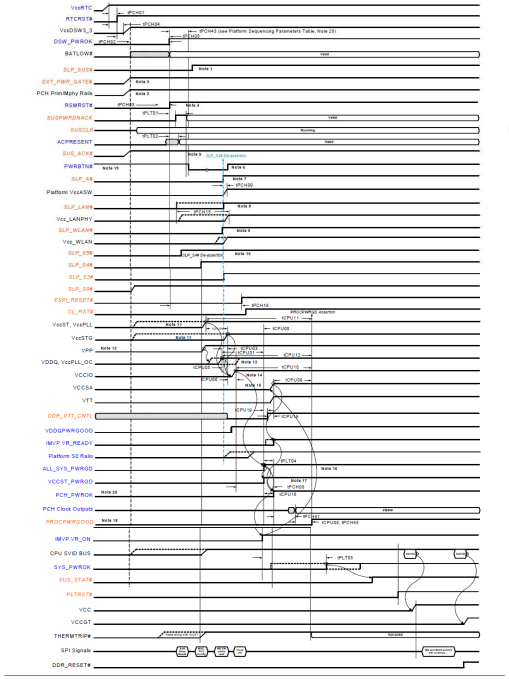
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

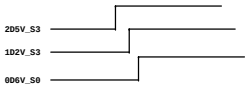
Size: A3 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 101 of 106

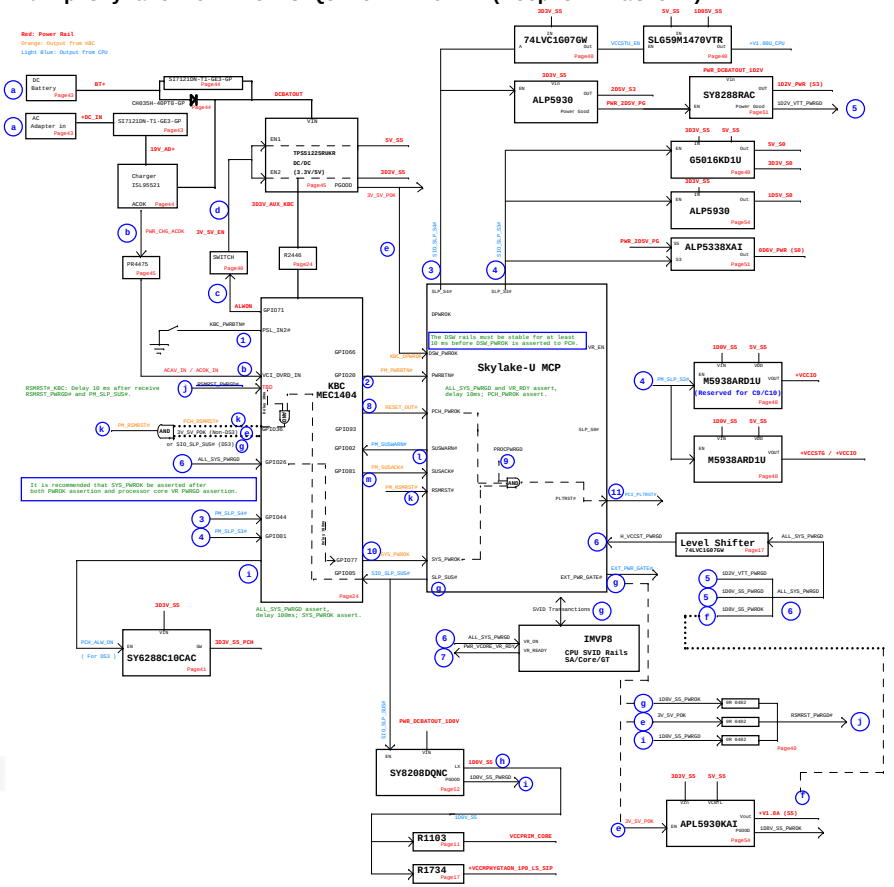
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

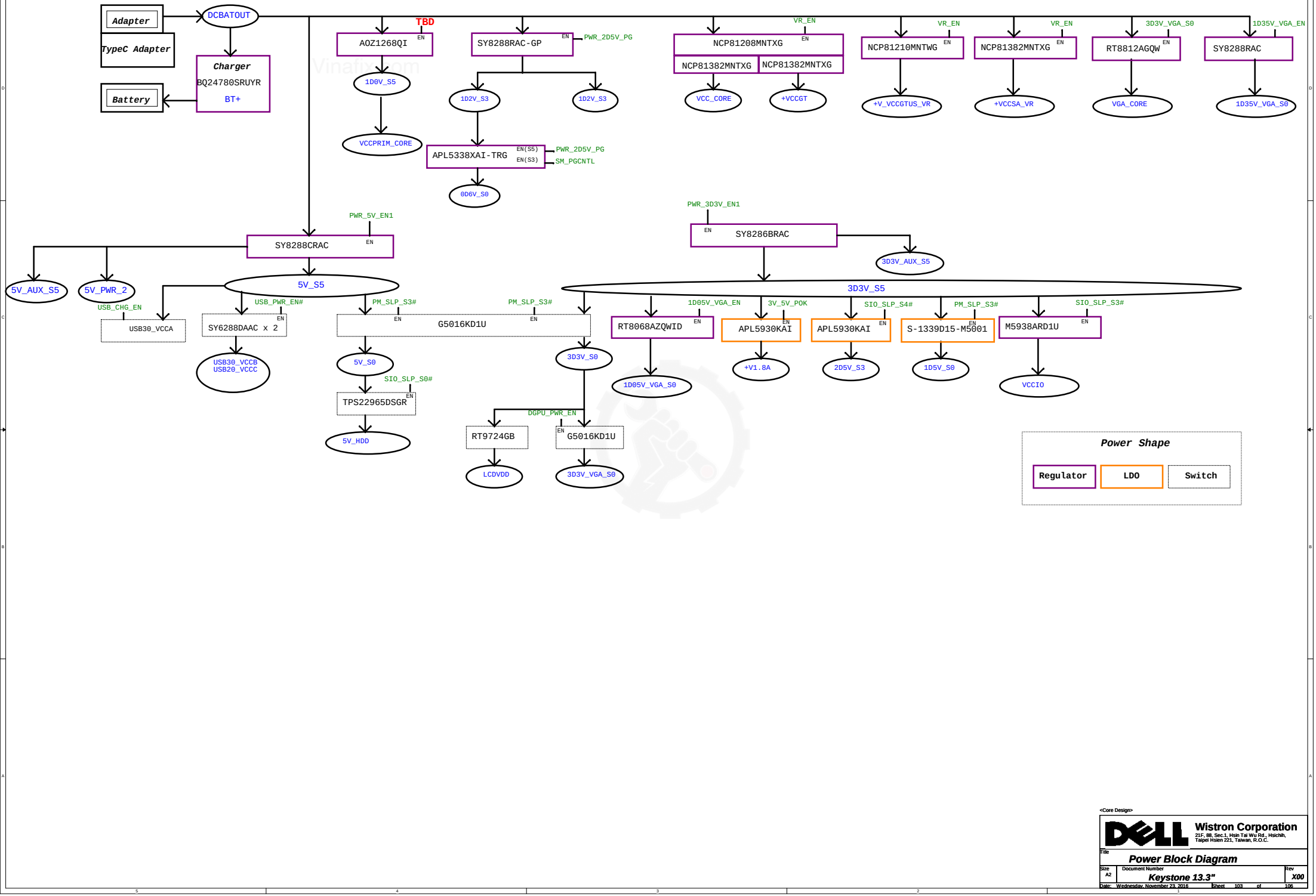


For DDR4 power sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)





<Core Design>

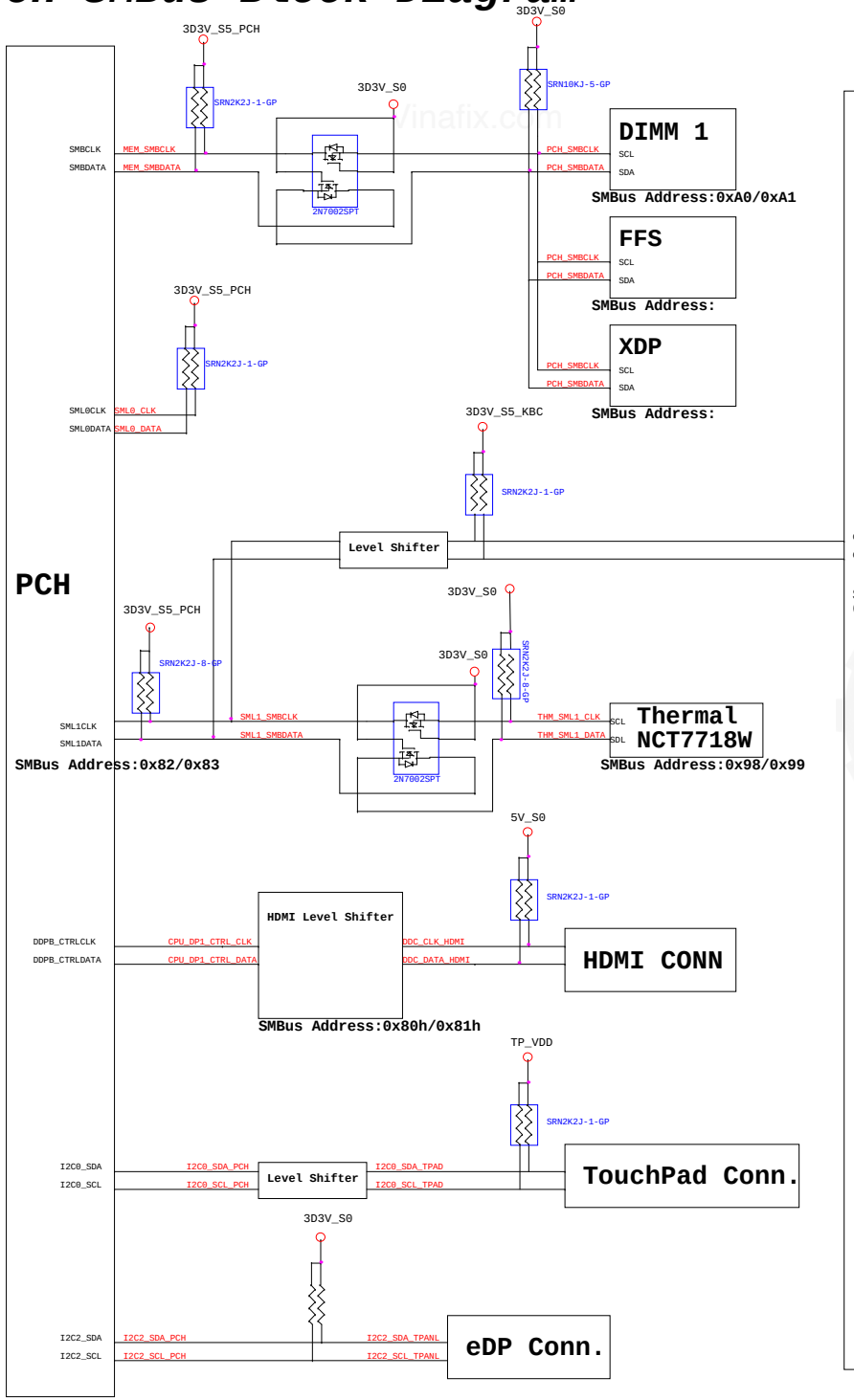
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

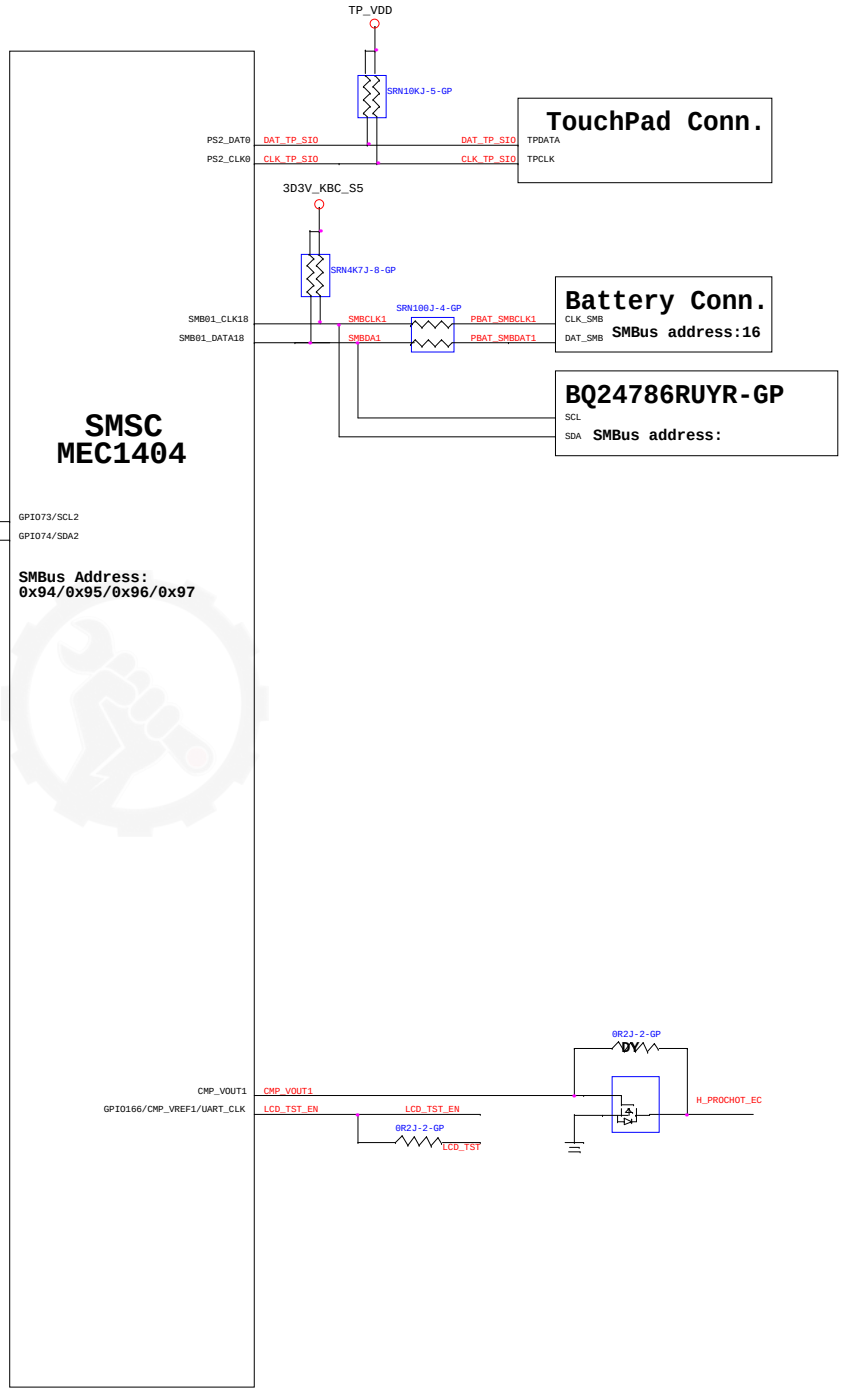
Size: A2 | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 103 of 106

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

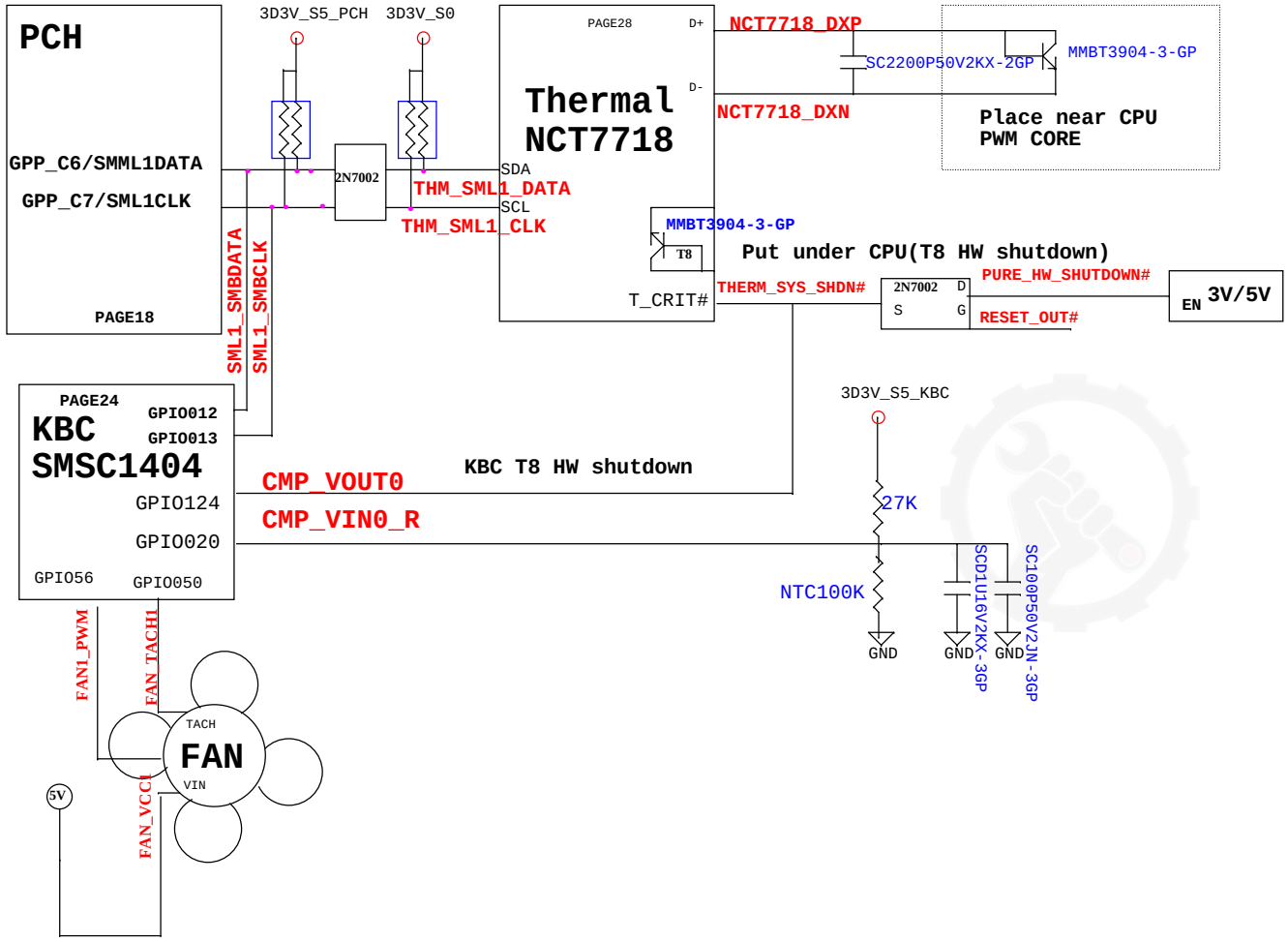
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

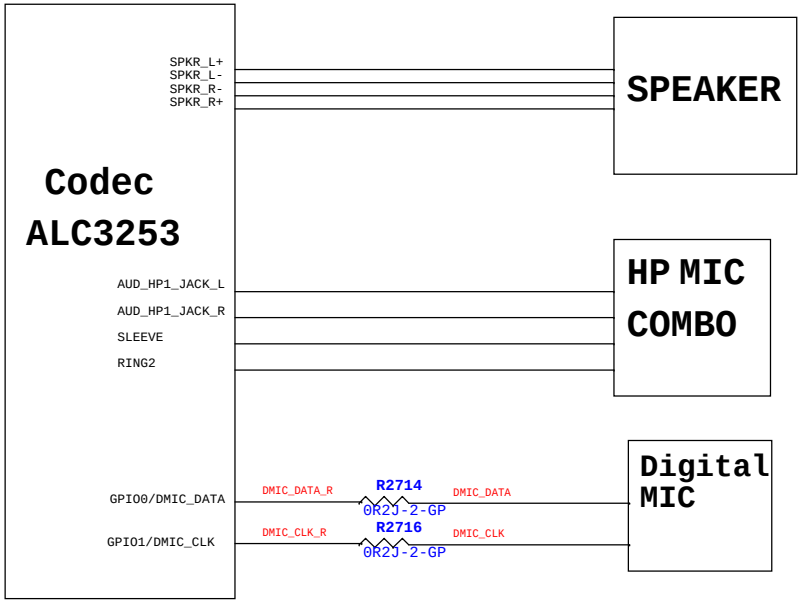
Size	Document Number	Rev
A2	Keystone 13.3"	X00

Date: Wednesday, November 23, 2016 Sheet 104 of 106

Thermal Block Diagram



Audio Block Diagram



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Keystone 13.3" | Rev: X00

Date: Wednesday, November 23, 2016 | Sheet 105 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SIP connector

Size	Document Number	Rev
A	***Keystone 13.3"***	***X00***

Date:	Wednesday, November 23, 2016	Sheet	106	of	106