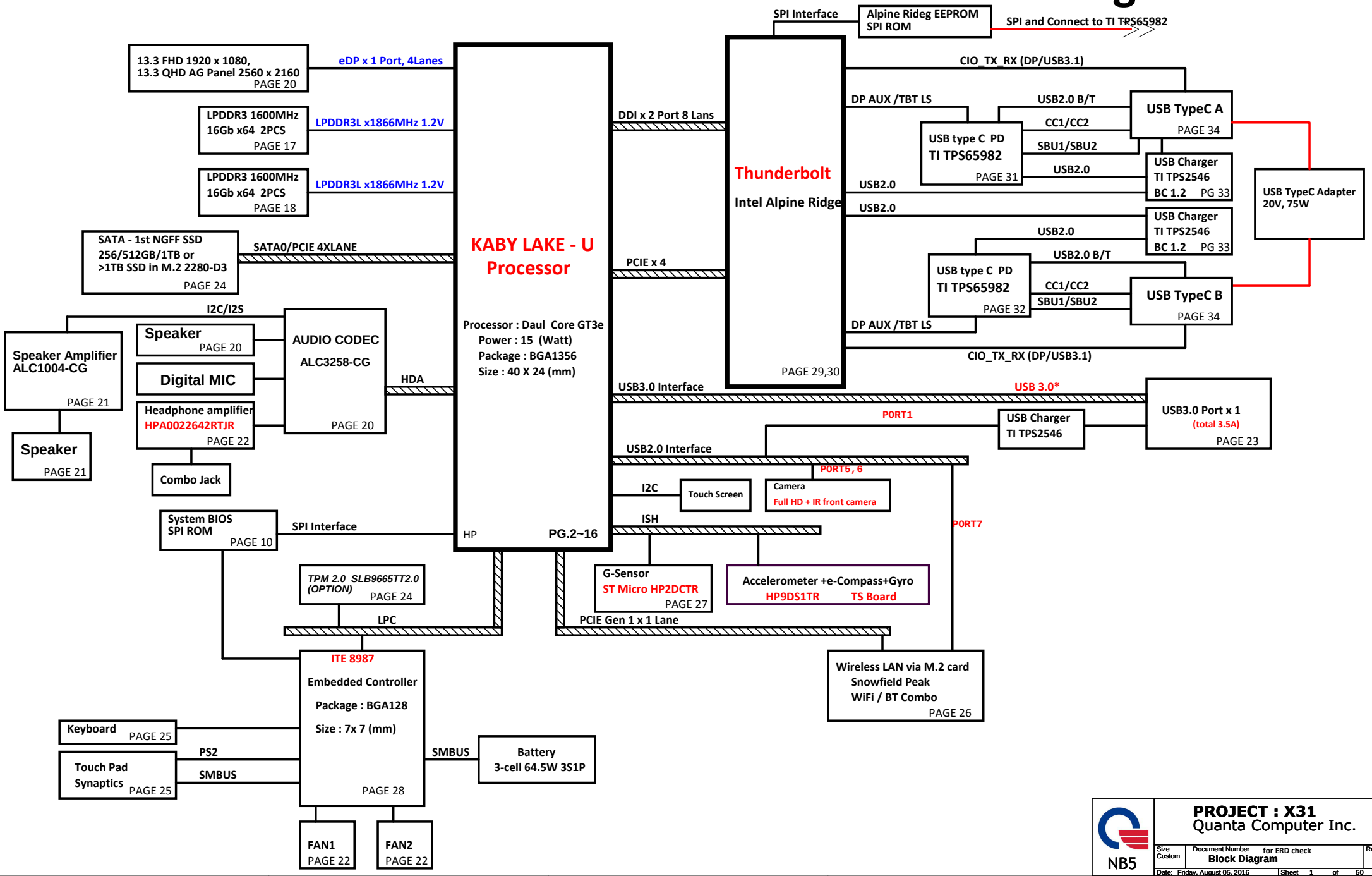
Monster Intel KABY LAKE ULT Platform Block Diagram

01



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Custom	Block Diagram for ERD check	

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+3V
INT_DP_SCL R194 2.2K_2
INT_DP_SDA R195 2.2K_2
SDVO_CLK R191 2.2K_2
SDVO_DATA R192 2.2K_2

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.
DDPD_CTRLDATA R197 10K_2

U1A SKL_ULT ? Need apply PN

DDI1_TX0_DN E55
DDI1_TX0_DP F55
DDI1_TX1_DN E58
DDI1_TX1_DP F58
DDI1_TX2_DN F53
DDI1_TX2_DP G53
DDI1_TX3_DN F56
DDI1_TX3_DP C56
DDI2_TX0_DN C50
DDI2_TX0_DP D50
DDI2_TX1_DN C52
DDI2_TX1_DP D52
DDI2_TX2_DN A50
DDI2_TX2_DP B50
DDI2_TX3_DN D51
DDI2_TX3_DP C51
DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]
DDI2_TXN[0] DDI2_TXP[0] DDI2_TXN[1] DDI2_TXP[1] DDI2_TXN[2] DDI2_TXP[2] DDI2_TXN[3] DDI2_TXP[3]
DDI
DISPLAY SIDEBANDS
EDP
SDVO_CLK L13
SDVO_DATA L12
INT_DP_SCL N7
INT_DP_SDA N8
DDPD_CTRLDATA N11 N12
+VCCIO R220 24.9/F_2 EDP_RCOMP E52
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA
EDP_RCOMP
*SKL_ULT
REV = 1
1 OF 20
?

EDP_TXN[0] C47 INT_EDP_TXN0
EDP_TXP[0] C46 INT_EDP_TXP0
EDP_TXN[1] D46 INT_EDP_TXN1
EDP_TXP[1] C45 INT_EDP_TXP1
EDP_TXN[2] A45 INT_EDP_TXN2
EDP_TXP[2] B45 INT_EDP_TXP2
EDP_TXN[3] A47 INT_EDP_TXN3
EDP_TXP[3] B47 INT_EDP_TXP3
EDP_AUXN E45 INT_EDP_AUXN
EDP_AUXP F45 INT_EDP_AUXP
EDP_DISP_UTIL B52
DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46
GPP_E13/DDPB_HPD0 L9
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD
EDP_BKLTEN R12 PCH_LVDS_BLON
EDP_BKLTCTL R11 PCH_DPST_PWM
EDP_VDDEN U13 PCH_DISP_ON

INT_EDP_TXN0 19
INT_EDP_TXP0 19
INT_EDP_TXN1 19
INT_EDP_TXP1 19
INT_EDP_TXN2 19
INT_EDP_TXP2 19
INT_EDP_TXN3 19
INT_EDP_TXP3 19
INT_EDP_AUXN 19
INT_EDP_AUXP 19
DDI1_AUX_DN 29
DDI1_AUX_DP 29
DDI2_AUX_DN 29
DDI2_AUX_DP 29
DDI1_HPD0 29
DDI2_HPD0 29
ULT_EDP_HPD 19
PCH_LVDS_BLON 19
PCH_DPST_PWM 19
PCH_DISP_ON 19

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!
+3V
R35 *10K_2
ULT_EDP_HPD
R31 100K_2

+3V 4,10,11,12,13,14,15,19,20,21,22,24,25,27,28,29,33,42,46
+1.0V 4,6,28,41
+VCCIO 6,41
+VCCSTPLL 5,6,9,41,42

U1D SKL_ULT ? Need apply PN

+VCCSTPLL
R170 *49.9/F_2 CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63 A65
28,37,42 H_PROCHOT# R188 499/F_4 28
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
BPM#[0] C55
BPM#[1] D55
BPM#[2] B54
BPM#[3] C56
GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5
R248 49.9/F_2 PROC_POPIRCOMP AT16
R249 49.9/F_2 PCH_OPI_RCOMP AU16
R210 49.9/F_2 EDRAM_OPIO_RCOMP H66
R208 49.9/F_2 EOPIO_RCOMP H65
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
*SKL_ULT
REV = 1
4 OF 20

JTAG
PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU
PROC_TRST# B59 XDP_TRST#
PCH_JTAG_TCK B56 JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH R182 *0_2/S XDP_TDI_CPU
PCH_JTAG_TDO A56 JTAG_TDO_PCH R16 *0_2/S XDP_TDO_CPU
PCH_JTAG_TMS C59 JTAG_TMS_PCH R181 *0_2/S XDP_TMS_CPU
PCH_TRST# C61 XDP_TRST#_CPU R177 *0_2/S XDP_TRST#
JTAGX A59 JTAGX_PCH R187 *0_2/S XDP_TCK0

+1.0V
R166 1K_2 H_PROCHOT#

Close to EC
+VCCSTPLL
PM_THRMTRIP# R553 1K_2
Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

+1.0V
JTAG_TMS_PCH R172 51_2
JTAG_TDI_PCH R171 51_2
JTAG_TDO_PCH R10 100_2
JTAG_TCK_PCH R14 51_2
XDP_TCK0 R176 51_2
XDP_TRST#_CPU R175 51_2
Close to Chipset
PVR Change

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KABYLAKE ULT Processor LPDDR3 x32

16 M_A_DQSN[7:0]
16 M_A_DQSP[7:0]
17 M_B_DQSN[7:0]
17 M_B_DQSP[7:0]
16 M_A_DQ[63:0]
17 M_B_DQ[63:0]

Need apply PN

U1B — SKL_ULT — *SKL_ULT REV = 1 — 2 OF 20

U1C — SKL_ULT — *SKL_ULT REV = 1 — 3 OF 20

NIL-DDR CH - A

NIL-DDR CH - B

Place near CPU

DDR Rcomp need follow Intel Spec 12-15 min trance length

Need change to 0ohm open

+1.2VSUS 6,16,17,18,39,41

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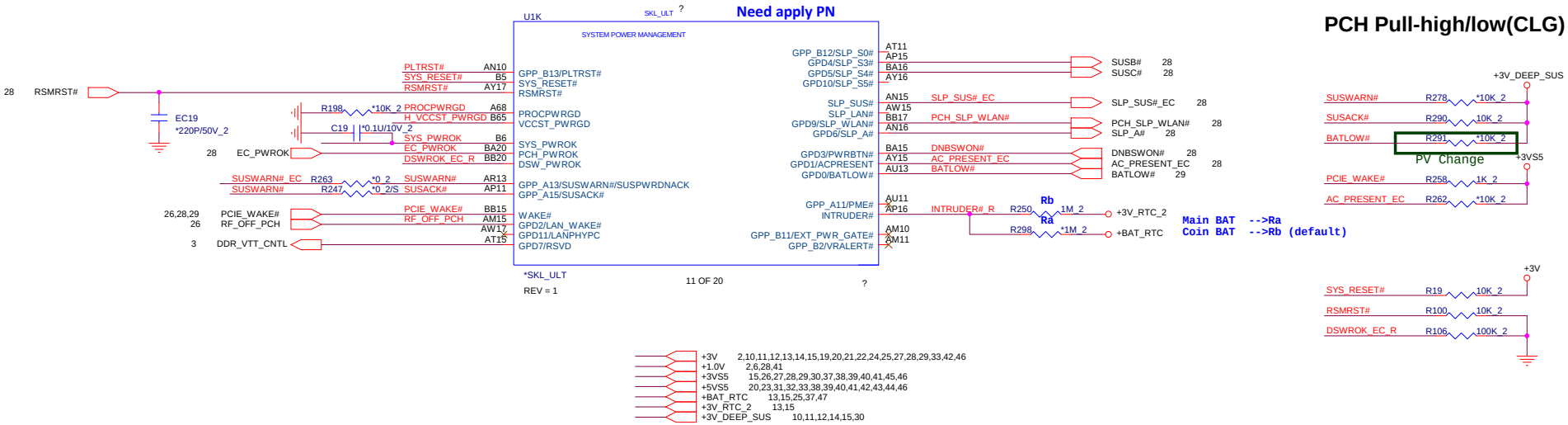
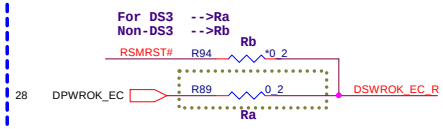
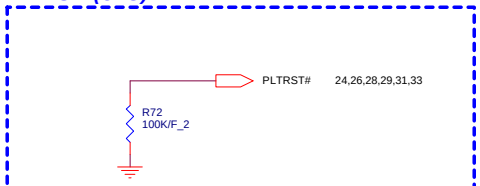


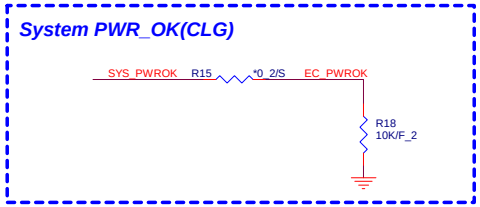
For DS3 Sequence



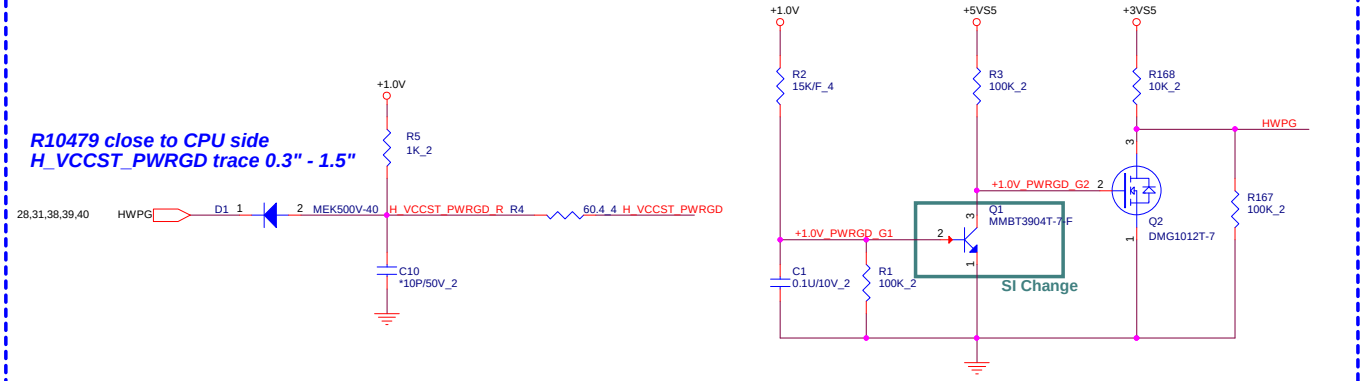
PLTRST#(CLG)



System PWR_OK(CLG)



HW Power Good Circuit



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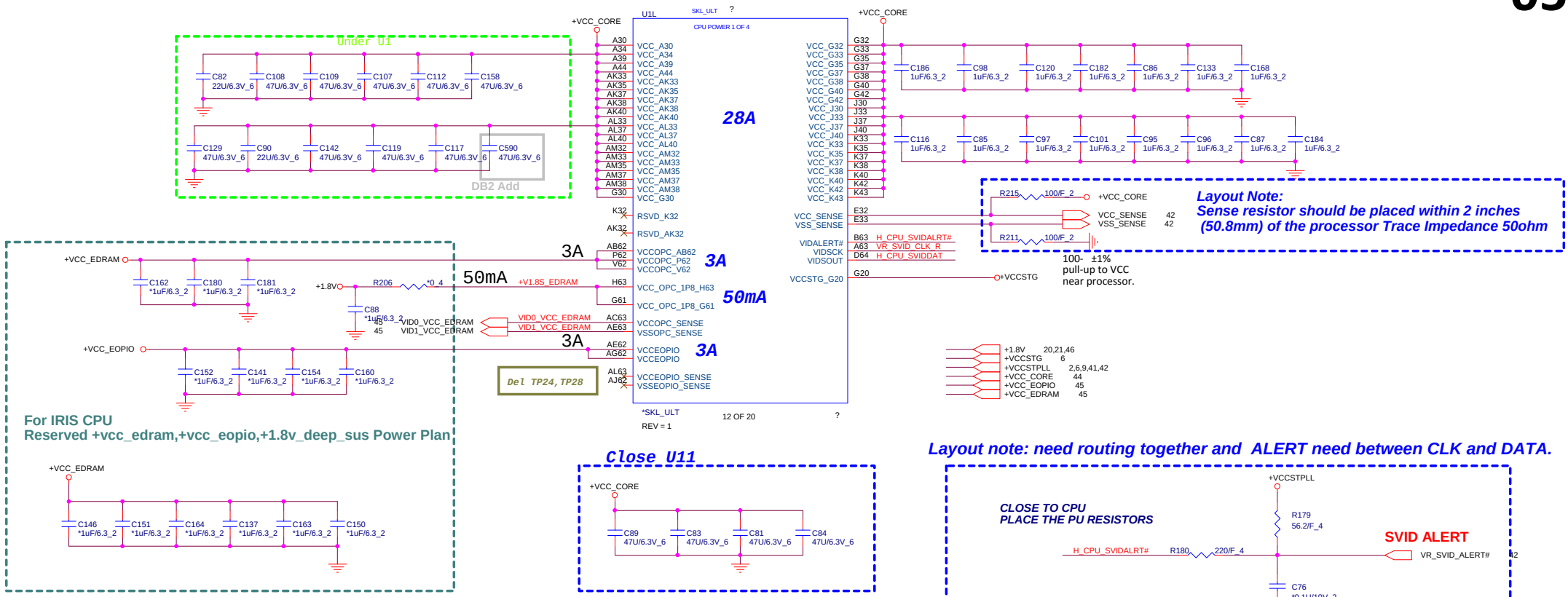
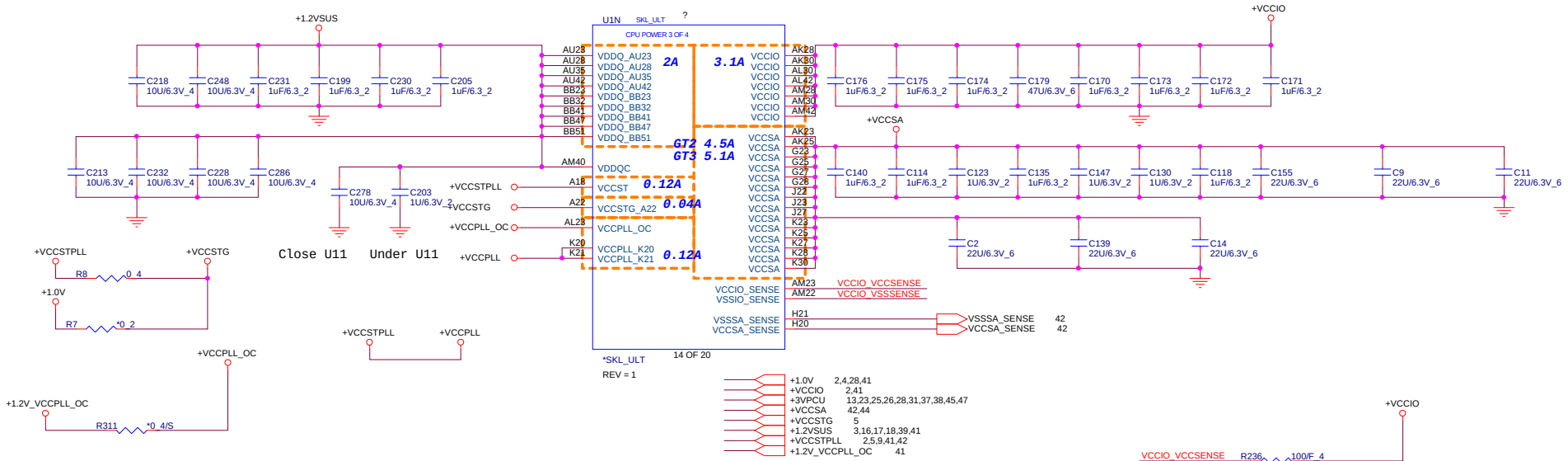
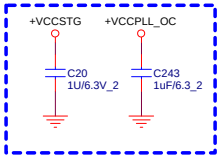


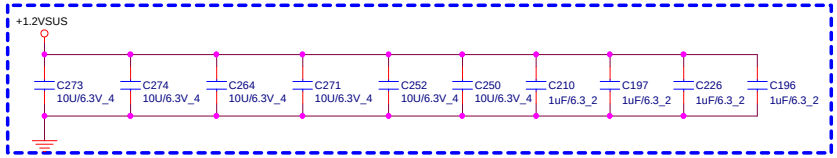
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



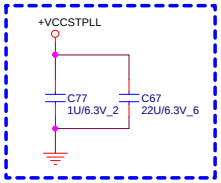
Under U11



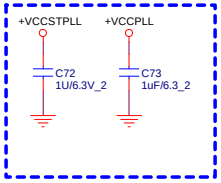
Close to CPU



Close A18 Ball

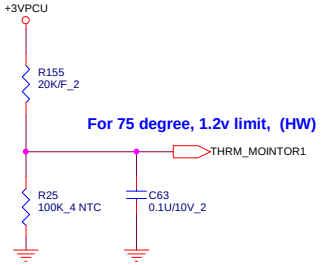


Close U11

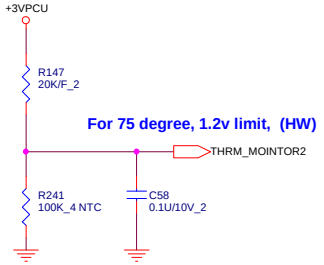


CHOCK Ther Protect

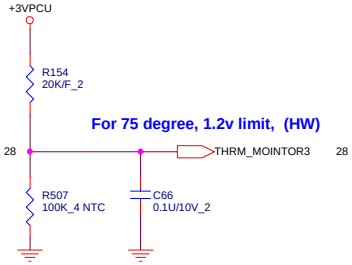
For 65 degree, 1.8v limit, (SW)



DDR Ther Protect



SSD Ther Protect



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Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
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Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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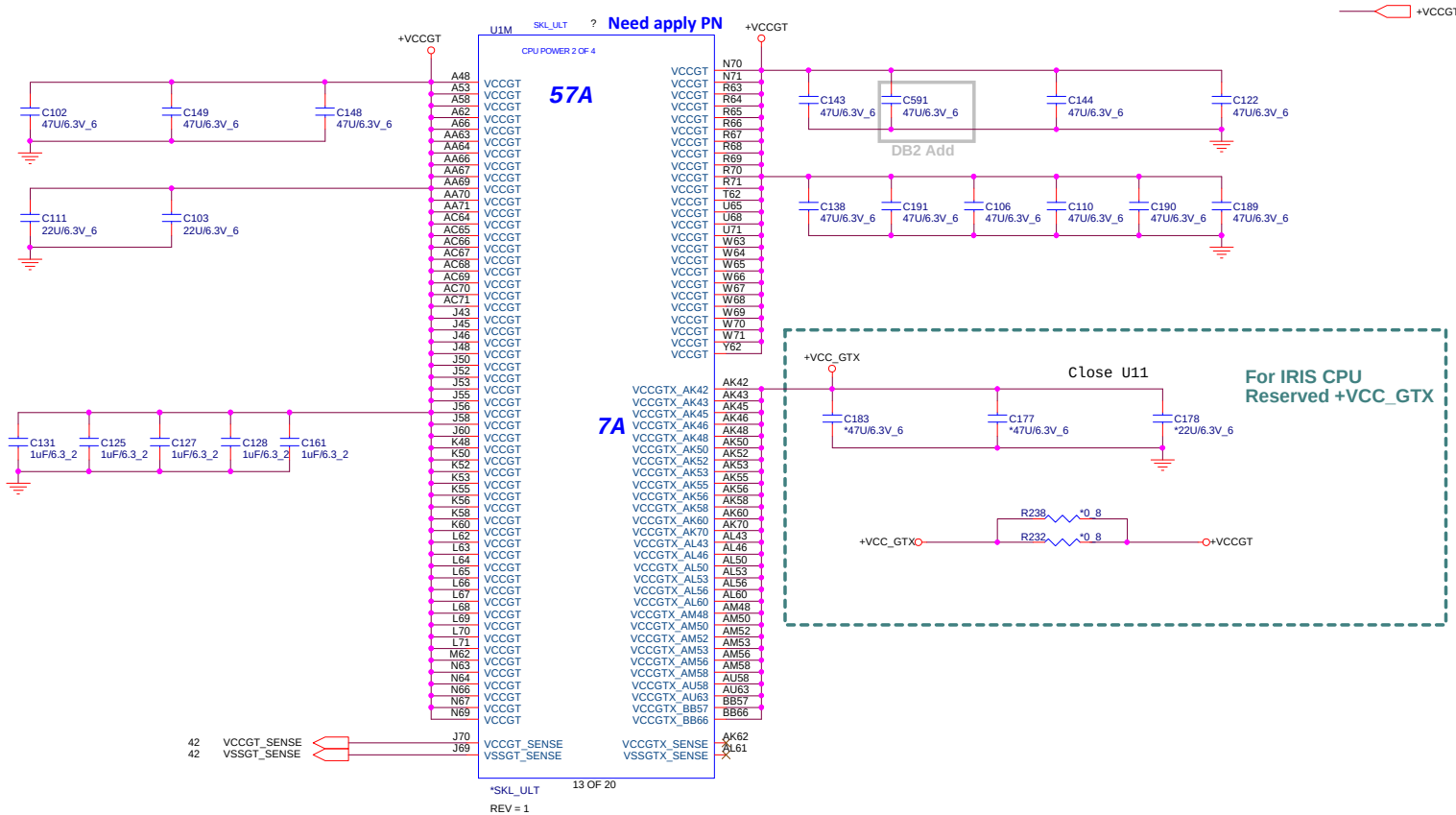

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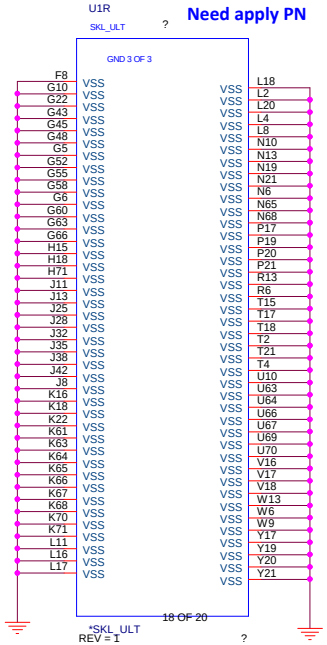

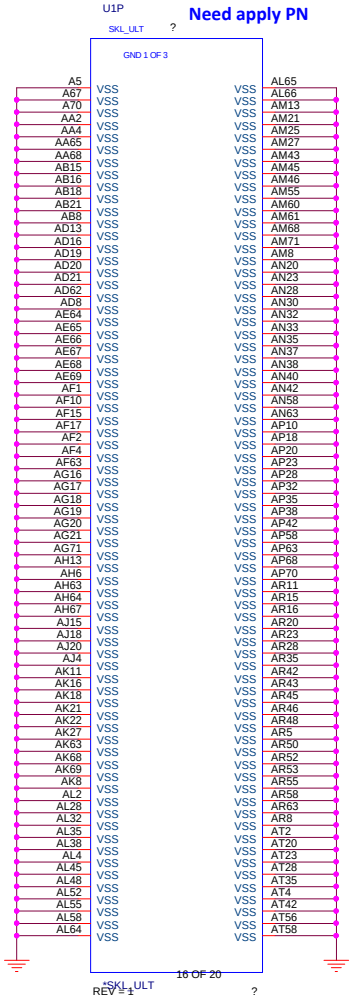

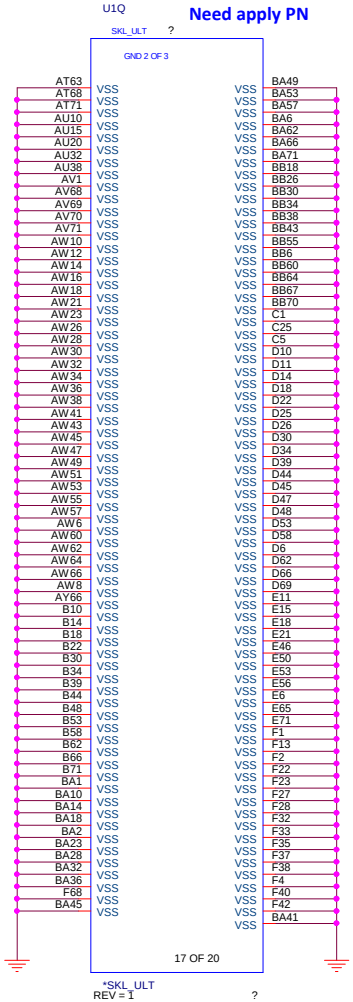

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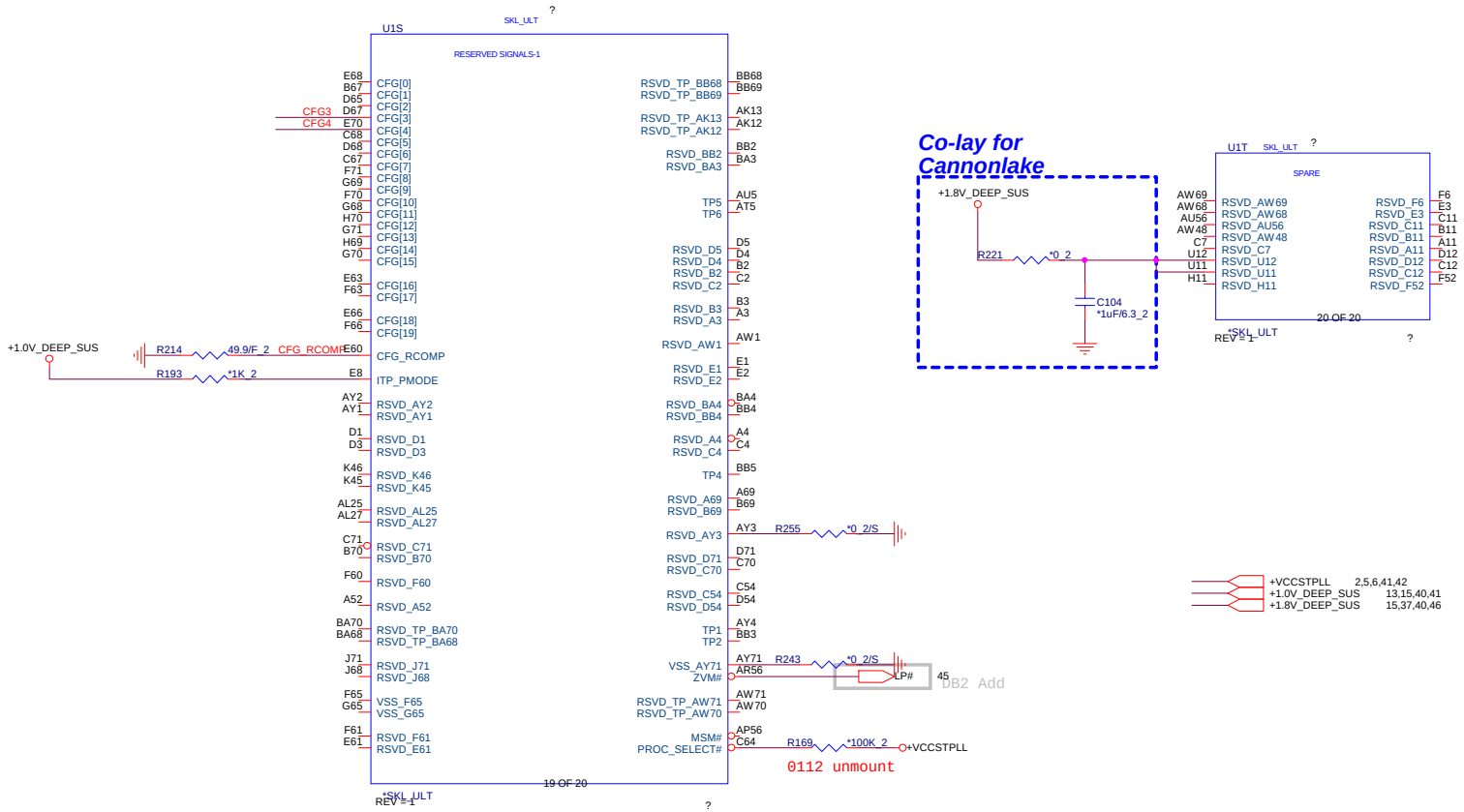
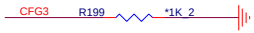
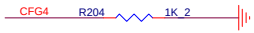


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

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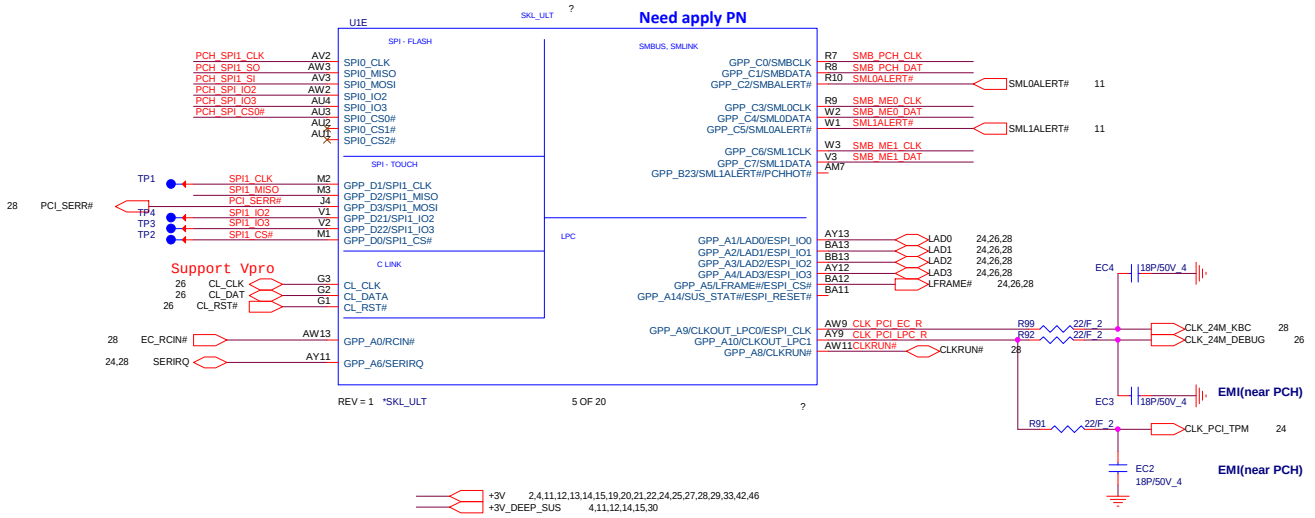
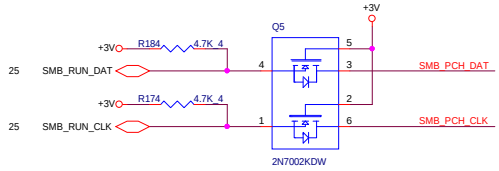


GPIO Pull UP

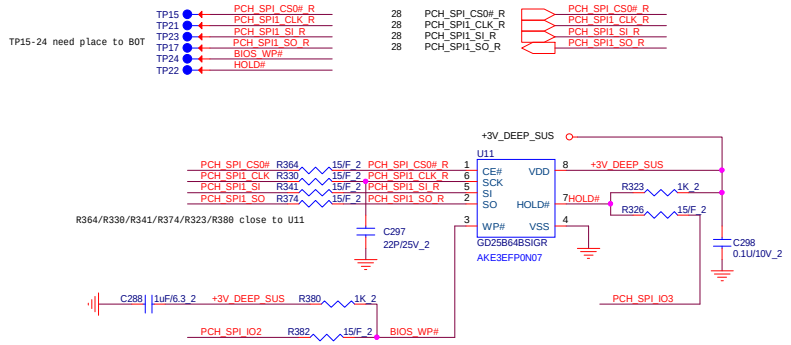
SMBus/Pull-up(CLG)



Touch Pad
XDP
LPDDR3 thermal sensor

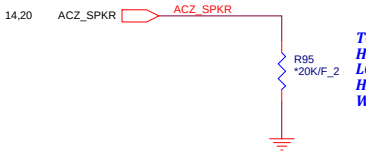
PCH SPI ROM(CLG)

Vender	Size	P/N
	8MB	
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE2EZN0Q00 (GD25B64CSIGR)
Mxic	8MB	AKE3EZ-0Z00 (MX25L6473FM2I-08G)
Socket		DFHS08FS023



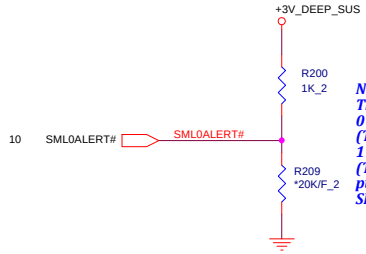
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

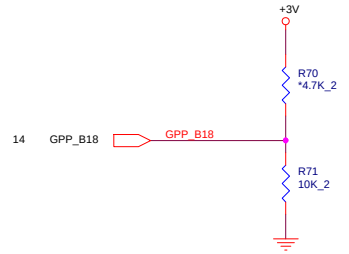


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

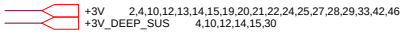
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.

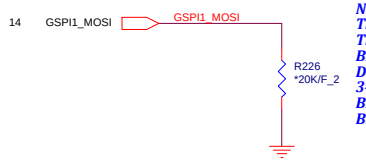


No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



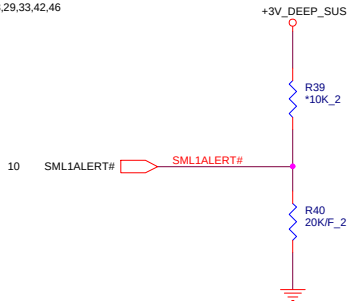
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.





No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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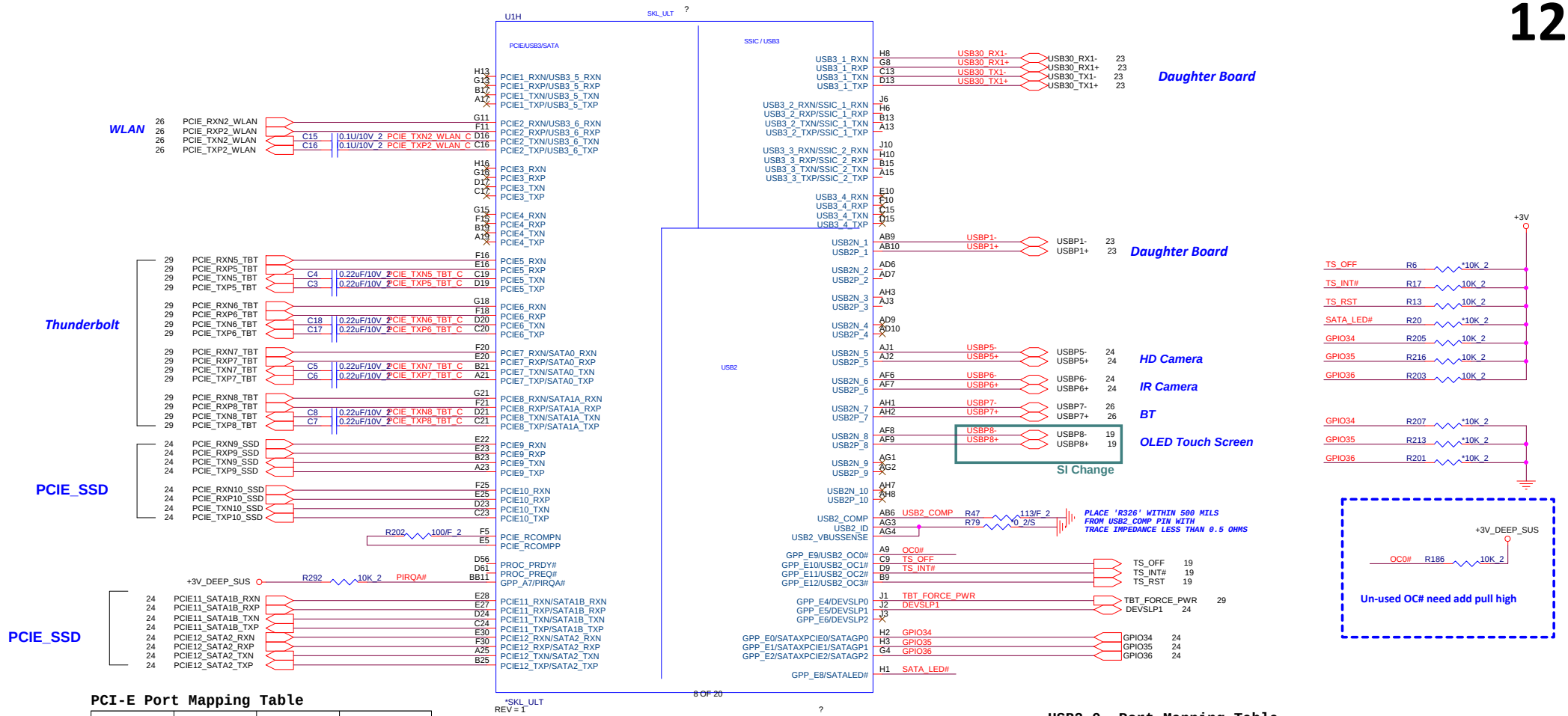

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	WLAN	Port1	Un-used
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	Thunderbolt	Port4	Thunderbolt
Port6	Thunderbolt	Port5	SSD HDD
Port7	Thunderbolt		
Port8	Thunderbolt		
Port9	SSD HDD		
Port10	SSD HDD		
Port11	SSD HDD		
Port12	SSD HDD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	NC
PORT-4	NC
PORT-5	HD Camera
PORT-6	IR Camera
PORT-7	WLAN
PORT-8	OLED Touch Screen
PORT-9	NC
PORT-10	NC

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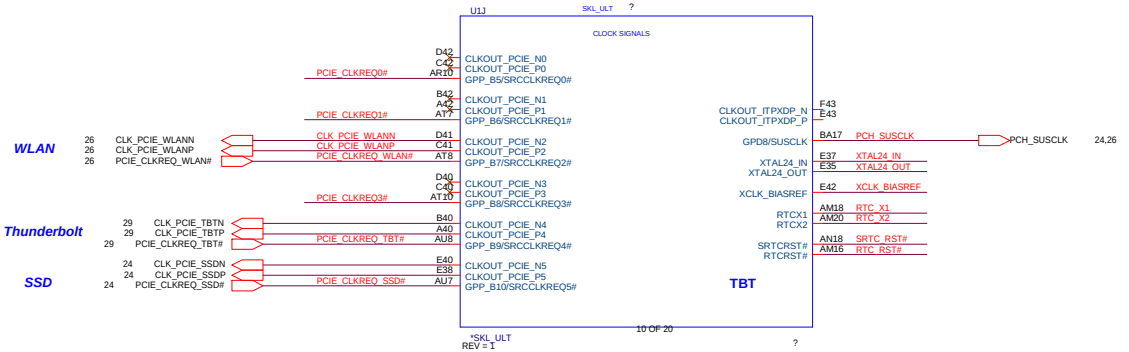
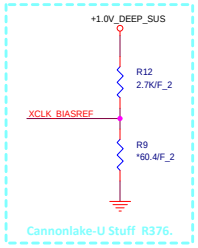
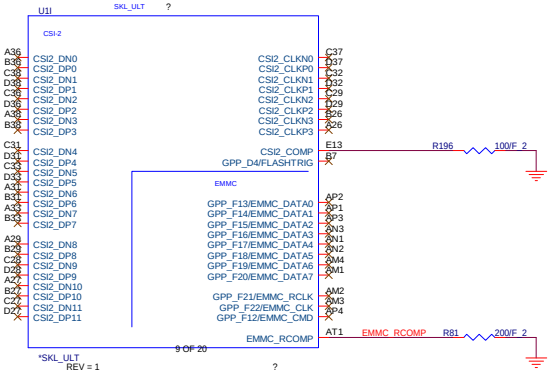
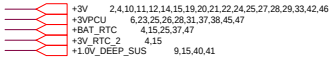
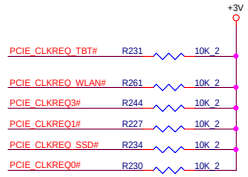




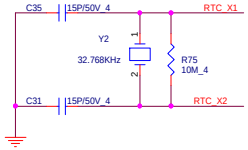




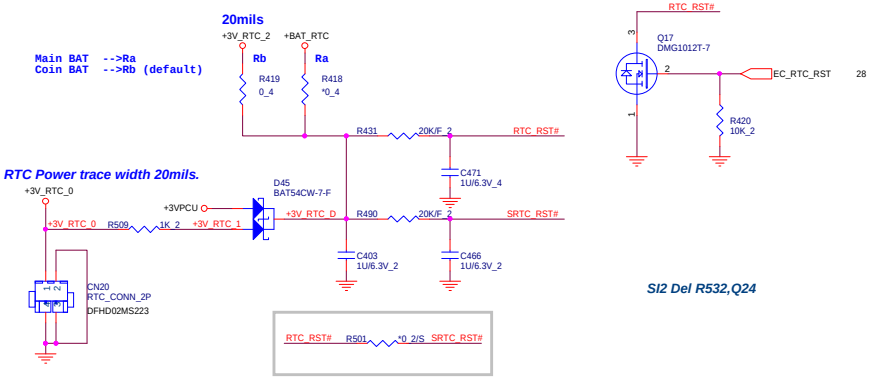
CLK_REQ/Strap Pin(CLG)



RTC Clock 32.768KHz

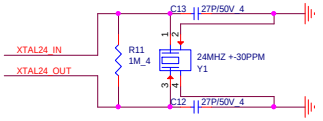


RTC Circuitry(RTC)



SI2 Del R532,Q24

External Crystal



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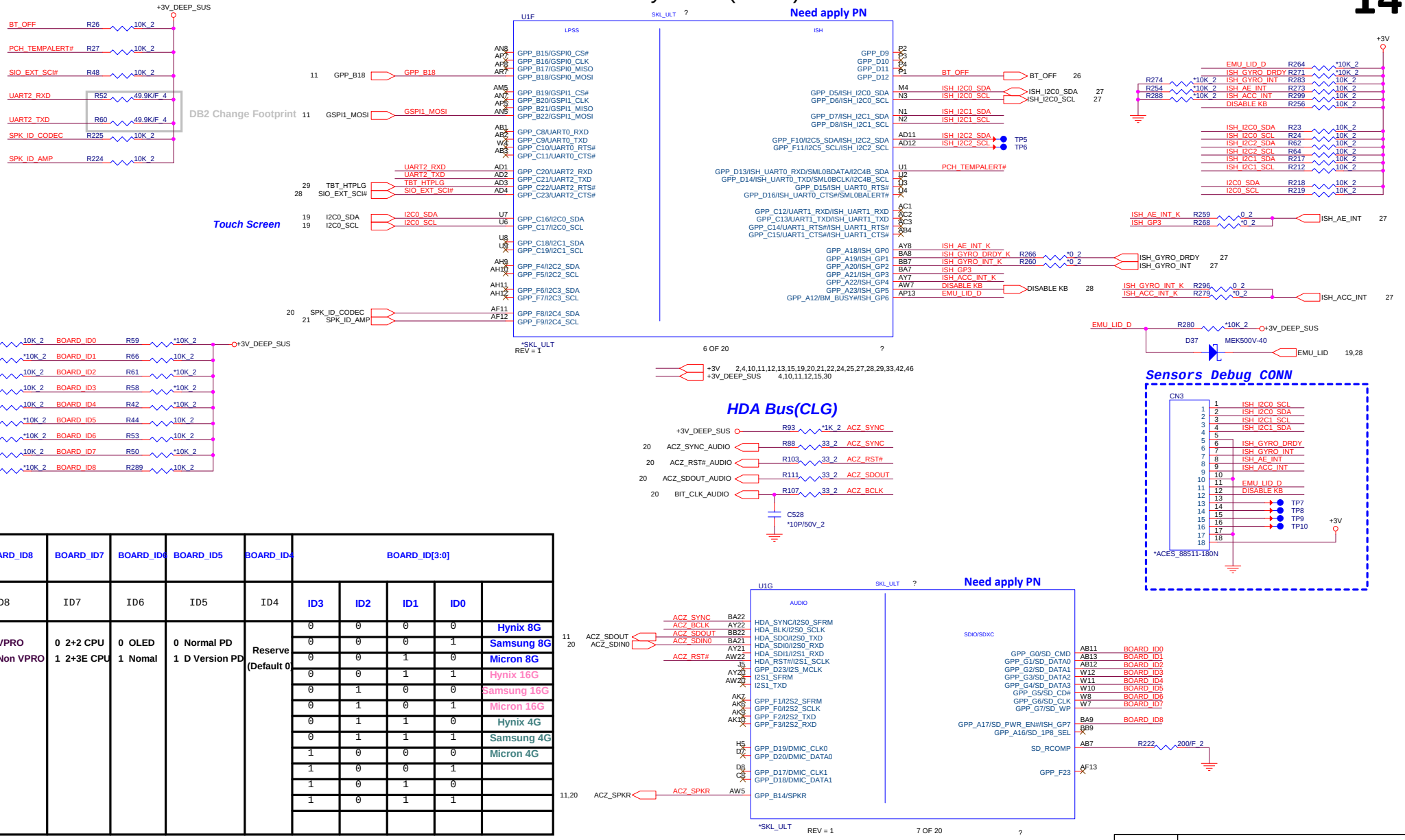
Skylake (GPIO)



KBL - U	BOARD_ID8	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID[3:0]				
Model	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
X31	0 VPRO 1 Non VPRO	0 2+2 CPU 1 2+3E CPU	0 OLED 1 Nomal	0 Normal PD 1 D Version PD	Reserve (Default 0)	0	0	0	0	Hynix 8G
						0	0	0	1	Samsung 8G
						0	0	1	0	Micron 8G
						0	0	1	1	Hynix 16G
						0	1	0	0	Samsung 16G
						0	1	0	1	Micron 16G
						0	1	1	0	Hynix 4G
						0	1	1	1	Samsung 4G
						1	0	0	0	Micron 4G
						1	0	0	1	
						1	0	1	0	
						1	0	1	1	

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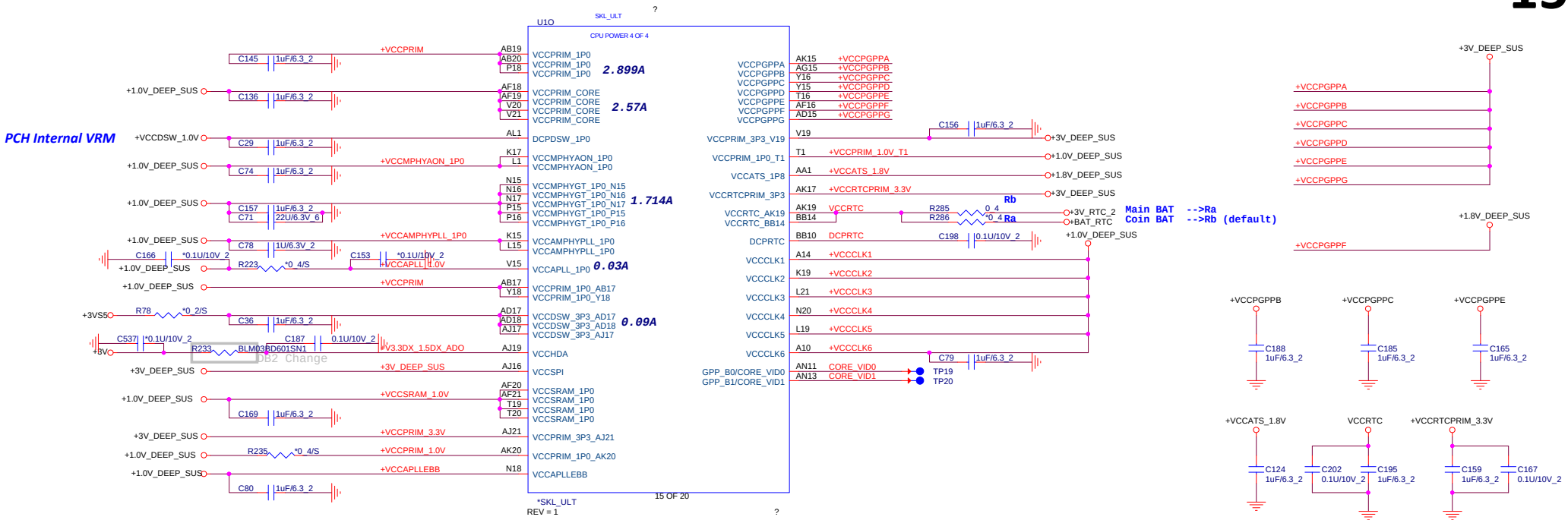

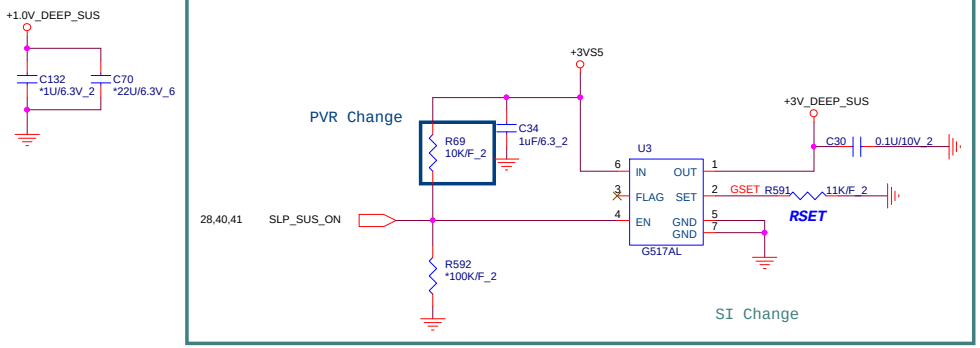

G517AL	
RSET(KΩ)	Current Limit(A)
9.76	2.87
11	2.5
24.9	1.0
37.4	0.7
49.9	0.5
100	0.25

+3V 2,4,10,11,12,13,14,19,20,21,22,24,25,27,28,29,33,42,46
+3VS5 4,26,27,28,29,30,37,38,39,40,41,45,46
+BAT_RTC 4,13,25,37,47
+3V_RTC_2 4,13
+3V_DEEP_SUS 4,10,11,12,14,30
+1.0V_DEEP_SUS 9,13,40,41
+1.8V_DEEP_SUS 9,37,40,46

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CHANNEL A:4Gb/8Gb/16Gb*2 LPDDR3-1866

4G Main Memory Configurable	8G Main Memory Configurable	16G Main Memory Configurable	
AKD5RW0TW44, IC SDRAM(178)H9CCNNN8GTMLAR-NUD TOPBSQ	AKD5RW0TW42, IC SDRAM(178)H9CCNNNBJTMLAR-NUD TOPBSQ	AKD5SW0TW22, IC SDRAM(178) H9CCNNNCLTMLAR-NUD TOP BSQ	Hynix
AKD5QWST523, ICSDRAM(178P)K4E8E304EE-EGCF(FBGA)TOPBSQ	AKD5RZST503, IC SDRAM(178P)K4E6E304EB-EGCF TOP BSQ	AKD5PZST507, ICSDRAM(178P)K4EBE304EB-EGCF(FBGA)TOPBSQ	Samsung
AKD5QWSTL05, IC SDRAM178P MT52L256M32D1PF-107 TOPBSQ	AKD5RWDTL05, IC SDRAM178P MT52L512M32D2PF-107 TOPBSQ	AKD5SWSTL02, IC SDRAM(178P)MT52L1G32D4PG-107 TOP BSQ	Micron

bit:32-63

U9A LPDDR3 — 0126 A Channel B Channel Swapping

U9B LPDDR3 — FBGA-178pin — LPDDR3_FPGA

bit:0-31

U10A LPDDR3 — 0126 A Channel B Channel Swapping

U10B LPDDR3 — FBGA-178pin — LPDDR3_FPGA

12 all trace, do not used shape

M3 VREF + M1 VREF

12 all trace, do not used shape

M3 VREF + M1 VREF

EMI reserve

EMI reserve

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	LPDDR3 A	1A

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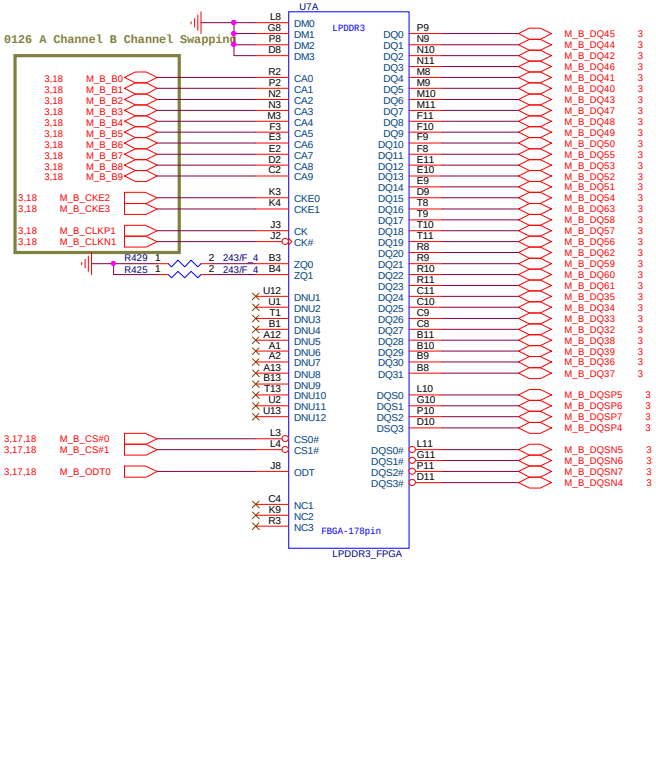
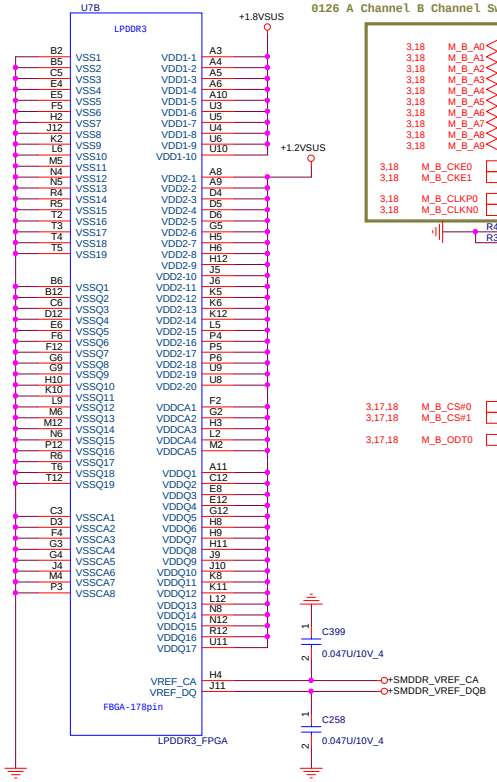
CHANNEL B:4Gb/8Gb/16Gb*2 LPDDR3-1866

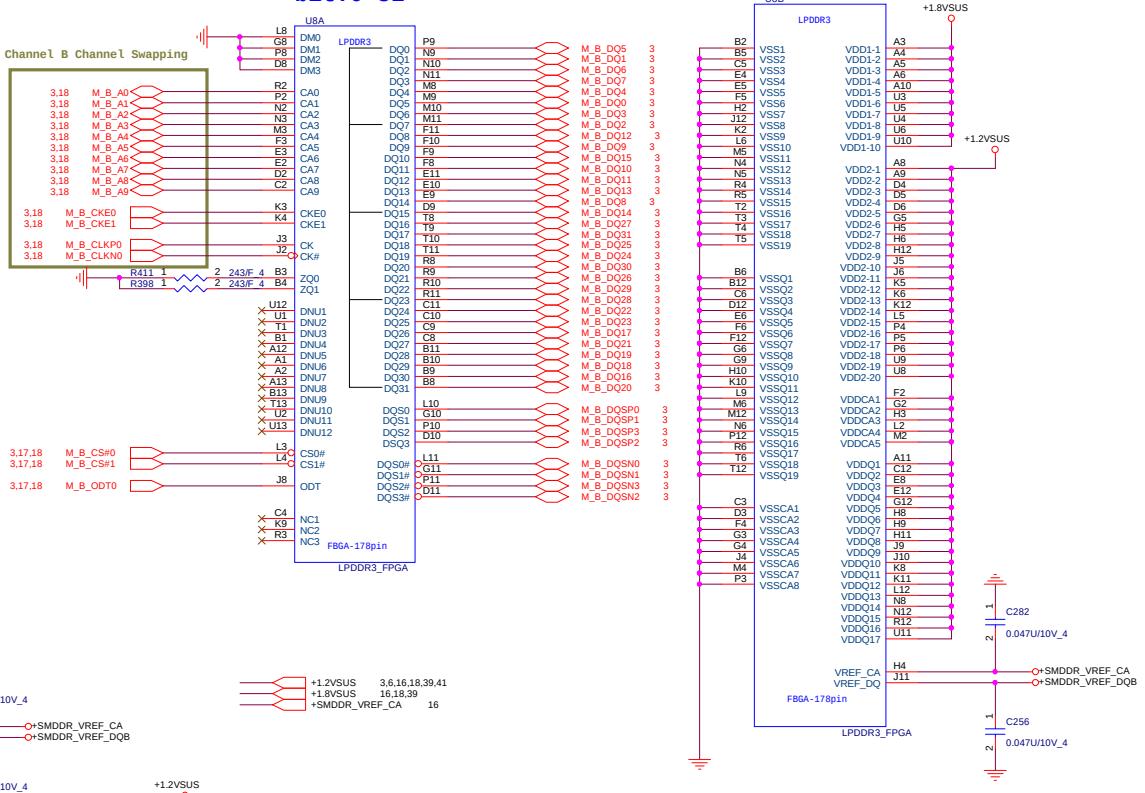
4G Main Memory Configurable	8G Main Memory Configurable	16G Main Memory Configurable	
AKD5RW0TW44, IC SDRAM(178)H9CCNNN8GTMLAR-NUD TOPBSQ	AKD5RW0TW42, IC SDRAM(178)H9CCNNNBJTMLAR-NUD TOPBSQ	AKD5SW0TW22, IC SDRAM(178) H9CCNNNCLTMLAR-NUD TOP BSQ	Hynix
AKD5QWST523, ICSDRAM(178P)K4E8E304EE-EGCF(FBGA)TOPBSQ	AKD5RZST503, IC SDRAM(178P)K4E8E304EB-EGCF TOP BSQ	AKD5PZST507, ICSDRAM(178P)K4EBE304EB-EGCF(FBGA)TOPBSQ	Samsung
AKD5QWSTL05, IC SDRAM178P MT52L256M32D1PF-107 TOPBSQ	AKD5RWDTL05, IC SDRAM178P MT52L512M32D2PF-107 TOPBSQ	AKD5SWSTL02, IC SDRAM(178P)MT52L1G32D4PG-107 TOP BSQ	Micron

bit:32-63



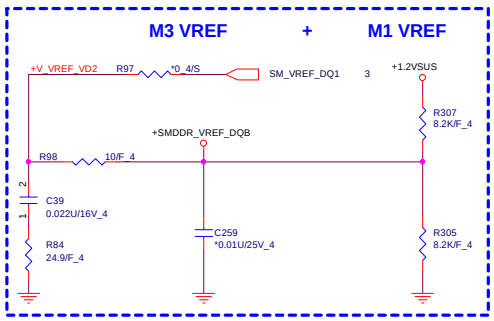


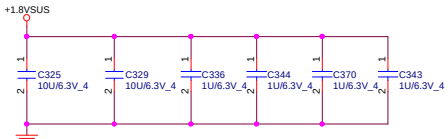
bit:0-31

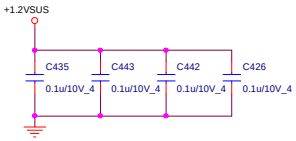


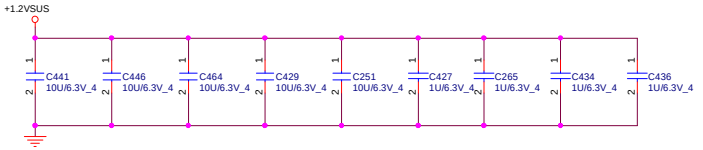
+1.2VSUS 3,6,16,18,39,41
+1.8VSUS 16,18,39
+SMDDR_VREF_CA 16

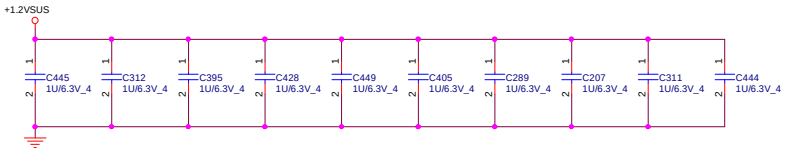
12 All 20mil trace, pleasedo not use shape

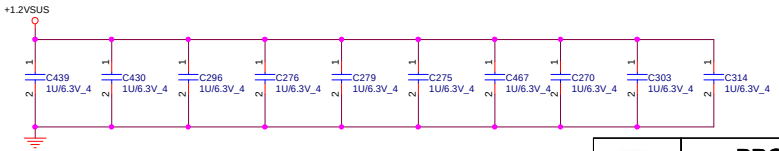












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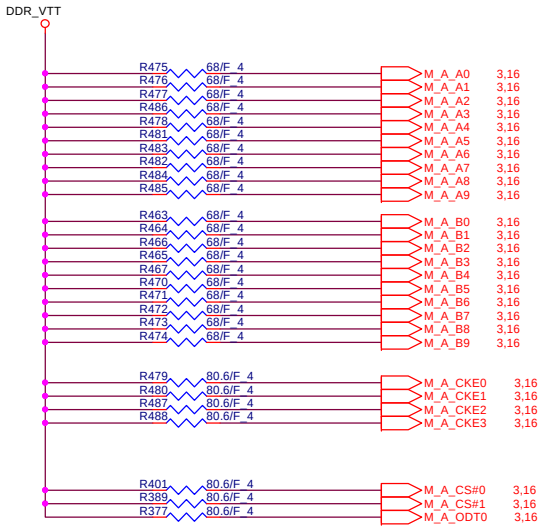

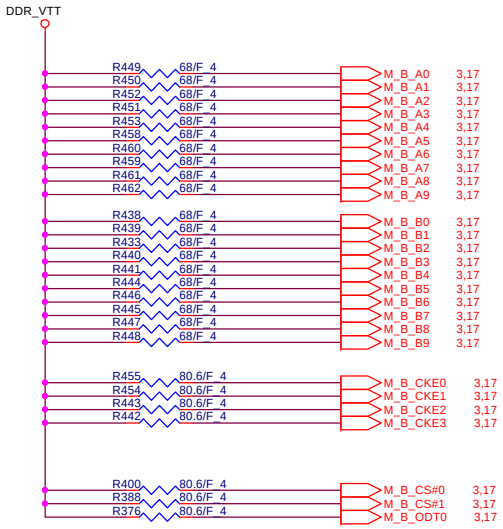

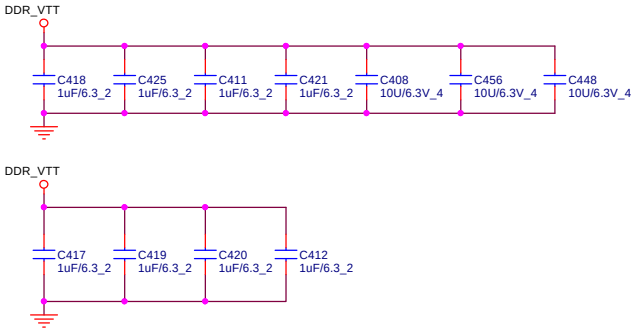

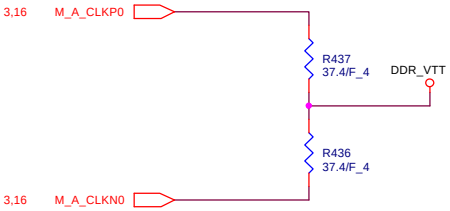

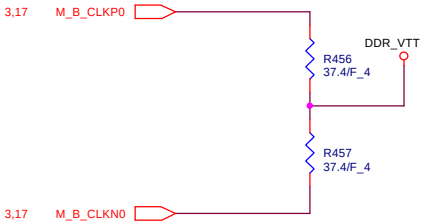

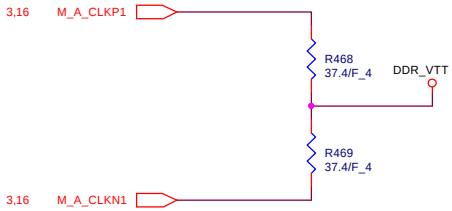

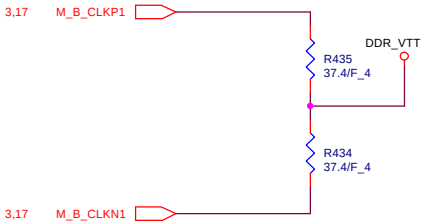

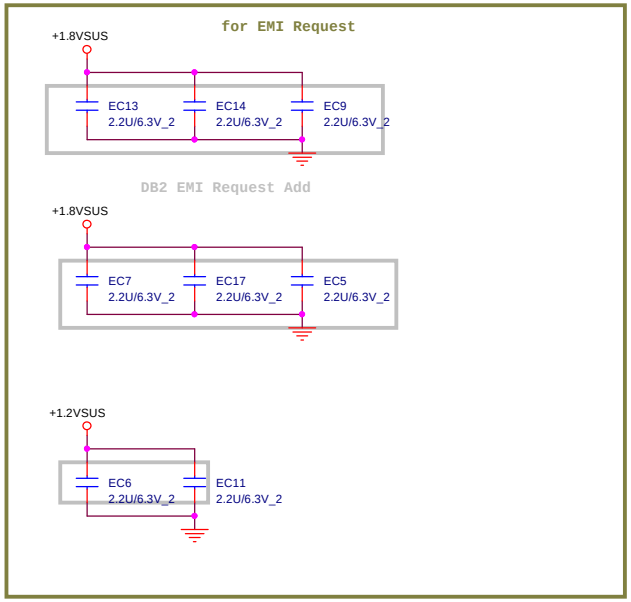

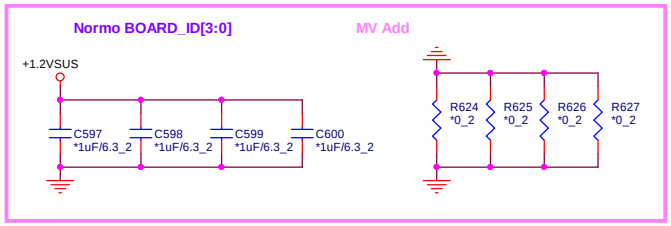

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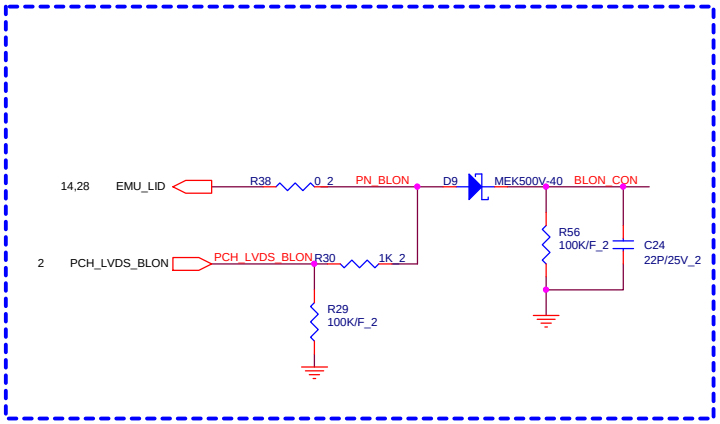
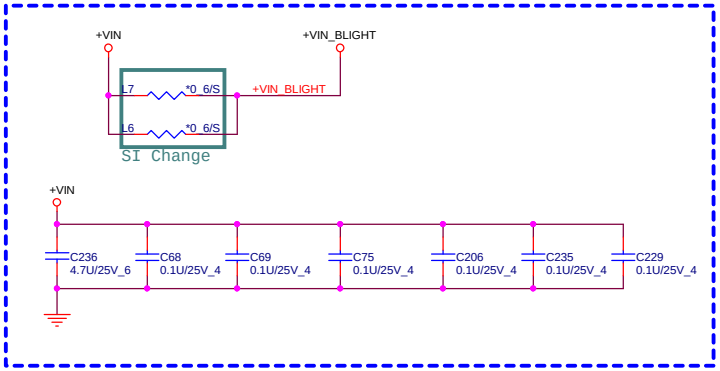
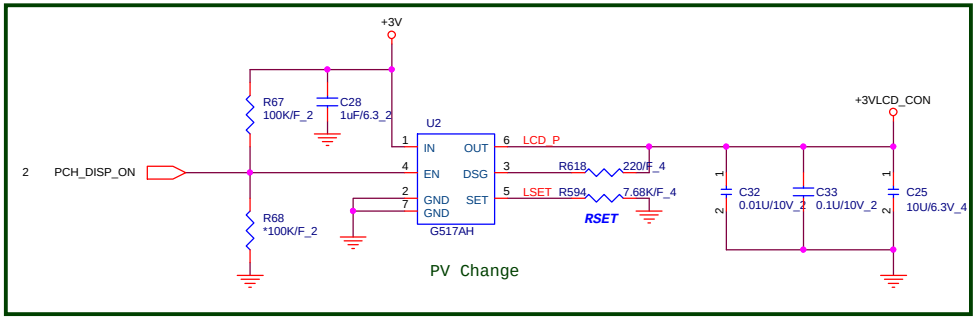
LID Switch

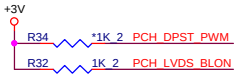


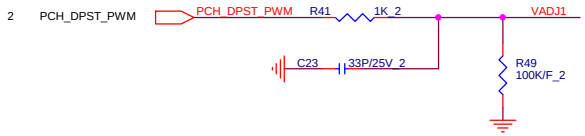
Panel Vin Cap

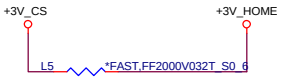


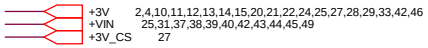


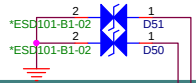
G517AH	
RSET(KΩ)	Current Limit(A)
7.68	2.7
10.5	2
21	1
42	0.5

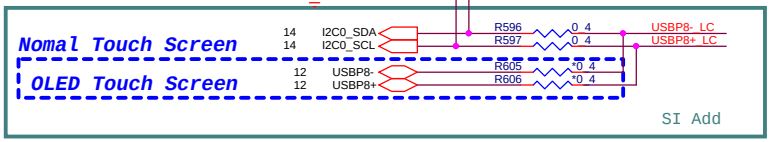


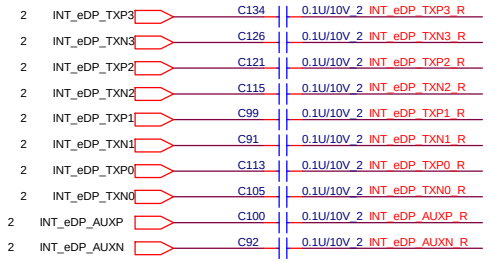




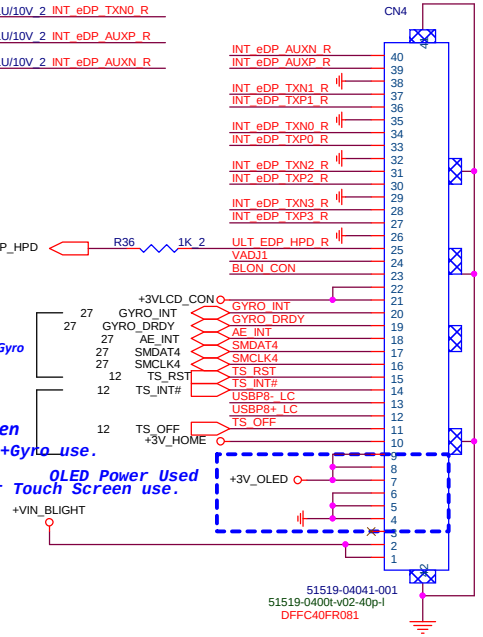








eDP Conn.



Accelerometer +e-Compass+Gyro

Touch Screen

+3V_HOME Power for Accelerometer +e-Compass+Gyro use.

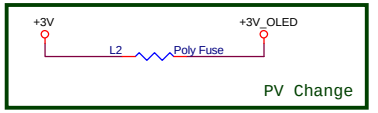
OLED Power Used

No support OLED SKU Pin 9 for Touch Screen use.

Poly Fuse

Vender	Size	P/N
WYN	0805	DK150TPU025 (LP-ISML150)
LFI	0805	DK150TPU022 (0805L150ULYR)
PYS	0805	DK150TPU018 (SPR-P150)

OLED Power Used



PROJECT : X31
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LCD CONN/CAM/LID	
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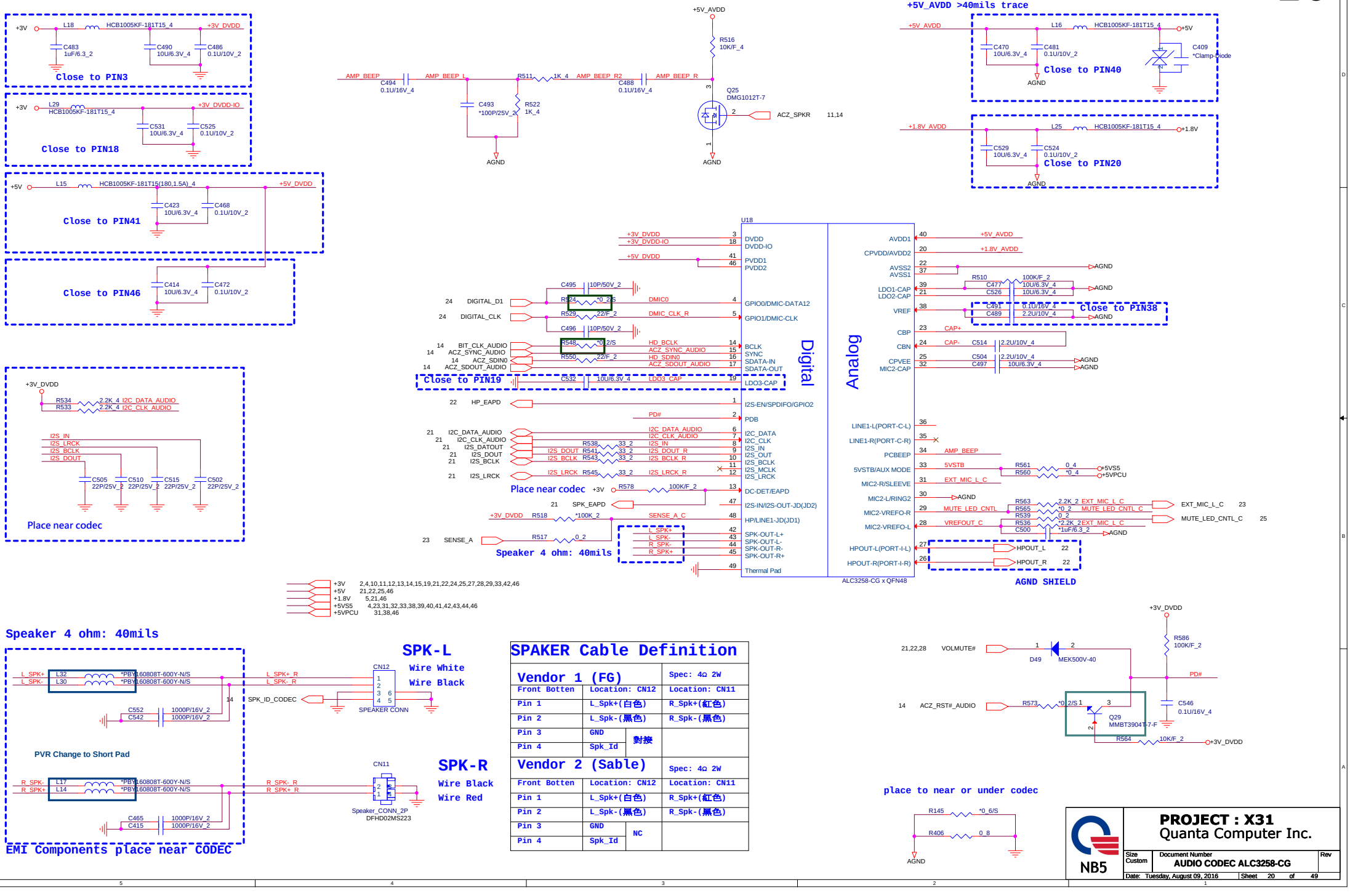
+3V
L18
HCB1005KF-181T15_4
+3V_DVDD
C483 1uF/6.3_2
C490 10U/6.3V_4
C486 0.1U/10V_2
Close to PIN3
+3V
L29
HCB1005KF-181T15_4
+3V_DVDD-IO
C531 10U/6.3V_4
C525 0.1U/10V_2
Close to PIN18
+5V
L15
HCB1005KF-181T15(180,1.5A)_4
+5V_DVDD
C423 10U/6.3V_4
C468 0.1U/10V_2
Close to PIN41
C414 10U/6.3V_4
C472 0.1U/10V_2
Close to PIN46
+3V_DVDD
R534 2.2K_4 I2C_DATA_AUDIO
R533 2.2K_4 I2C_CLK_AUDIO
I2S_IN
I2S_LRCK
I2S_BCLK
I2S_DOUT
C505 22P/25V_2
C510 22P/25V_2
C515 22P/25V_2
C502 22P/25V_2
Place near codec
+5V_AVDD
R516 10K/F_4
AMP_BEEP
C494 0.1U/16V_4
AMP_BEEP_L
R511 1K_4
AMP_BEEP_R2
C488 0.1U/16V_4
AMP_BEEP_R
C493 *100P/25V_2
R522 1K_4
AGND
Q25 DMG1012T-7
ACZ_SPKR 11,14
AGND
+5V_AVDD >40mils trace
+5V_AVDD
L16 HCB1005KF-181T15_4 +5V
C470 10U/6.3V_4
C481 0.1U/10V_2
C409 *Clamp-Diode
Close to PIN40
AGND
+1.8V_AVDD
L25 HCB1005KF-181T15_4 +1.8V
C529 10U/6.3V_4
C524 0.1U/10V_2
Close to PIN20
AGND
U18
Digital
Analog
+3V_DVDD
+3V_DVDD-IO
DVDD
DVDD-IO
+5V_DVDD
PVDD1
PVDD2
DIGITAL_D1
DIGITAL_CLK
C495 10P/50V_2
R524 *0_2/S
R529 22/F_2
DMIC0
DMIC_CLK_R
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
C496 10P/50V_2
R548 *0_2/S
R550 22/F_2
BIT_CLK_AUDIO
ACZ_SYNC_AUDIO
ACZ_SDIN0
ACZ_SDOUT_AUDIO
HD_BCLK
ACZ_SYNC_AUDIO
HD_SDIN0
ACZ_SDOUT_AUDIO
BCLK
SYNC
SDATA-IN
SDATA-OUT
Close to PIN19
C532 10U/6.3V_4
LDO3_CAP
LDO3-CAP
HP_EAPD
I2S-EN/SPDIFO/GPIO2
PD#
PDB
I2C_DATA_AUDIO
I2C_CLK_AUDIO
I2S_DATOUT
I2S_BCLK
I2S_LRCK
R538 33_2
R541 33_2
R543 33_2
R545 33_2
I2S_DOUT
I2S_BCLK_R
I2S_LRCK_R
I2C_DATA
I2C_CLK
I2S_IN
I2S_OUT
I2S_BCLK
I2S_MCLK
I2S_LRCK
Place near codec
+3V
R578 100K/F_2
DC-DET/EAPD
SPK_EAPD
I2S-IN/I2S-OUT-JD(JD2)
+3V_DVDD
R518 *100K_2
SENSE_A_C
HP/LINE1-JD(JD1)
SENSE_A
R517 0_2
L_SPK+
L_SPK-
R_SPK-
R_SPK+
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R-
SPK-OUT-R+
Thermal Pad
Speaker 4 ohm: 40mils
ALC3258-CG x QFN48
AVDD1
CPVDD/AVDD2
AVSS2
AVSS1
LDO1-CAP
LDO2-CAP
VREF
CBP
CBN
CPVEE
MIC2-CAP
+5V_AVDD
+1.8V_AVDD
AGND
R510 100K/F_2
C477 10U/6.3V_4
C526 10U/6.3V_4
C491 0.1U/16V_4
C489 2.2U/10V_4
Close to PIN38
CAP+
CAP-
C514 2.2U/10V_4
C504 2.2U/10V_4
C497 10U/6.3V_4
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
PCBEEP
5VSTB/AUX MODE
MIC2-R/SLEEVE
MIC2-L/RING2
MIC2-VREFO-R
MIC2-VREFO-L
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
AMP_BEEP
5VSTB
EXT_MIC_L_C
MUTE_LED_CNTL
VREFOUT_C
R561 0_4
R560 *0_4
+5VS5
+5VPCU
R563 2.2K_2 EXT_MIC_L_C
R565 *0_2 MUTE_LED_CNTL_C
R539 0_2
R536 *2.2K_2 EXT_MIC_L_C
C500 *1uF/6.3_2
EXT_MIC_L_C 23
MUTE_LED_CNTL_C 25
HPOUT_L 22
HPOUT_R 22
AGND SHIELD
+3V 2,4,10,11,12,13,14,15,19,21,22,24,25,27,28,29,33,42,46
+5V 21,22,25,46
+1.8V 5,21,46
+5VS5 4,23,31,32,33,38,39,40,41,42,43,44,46
+5VPCU 31,38,46
Speaker 4 ohm: 40mils
L_SPK+
L_SPK-
L32 *PBY160808T-600Y-N/S
L30 *PBY160808T-600Y-N/S
C552 1000P/16V_2
C542 1000P/16V_2
PVR Change to Short Pad
R_SPK-
R_SPK+
L17 *PBY160808T-600Y-N/S
L14 *PBY160808T-600Y-N/S
C465 1000P/16V_2
C415 1000P/16V_2
EMI Components place near CODEC
SPK_ID_CODEC
CN12
SPEAKER CONN
SPK-L
Wire White
Wire Black
CN11
Speaker_CONN_2P
DFHD02MS223
SPK-R
Wire Black
Wire Red
SPAKER Cable Definition
Vendor 1 (FG)
Spec: 4Ω 2W
Front Botten
Location: CN12
Location: CN11
Pin 1
L_Spk+(白色)
R_Spk+(紅色)
Pin 2
L_Spk-(黑色)
R_Spk-(黑色)
Pin 3
GND
對接
Pin 4
Spk_Id
Vendor 2 (Sable)
Spec: 4Ω 2W
Front Botten
Location: CN12
Location: CN11
Pin 1
L_Spk+(白色)
R_Spk+(紅色)
Pin 2
L_Spk-(黑色)
R_Spk-(黑色)
Pin 3
GND
NC
Pin 4
Spk_Id
21,22,28
VOLMUTE#
D49 MEK500V-40
+3V_DVDD
R586 100K/F_2
PD#
14
ACZ_RST#_AUDIO
R573 *0_2/S
Q29 MMBT3904T-7-F
C546 0.1U/16V_4
R564 10K/F_2
+3V_DVDD
place to near or under codec
R145 *0_6/S
R406 0_8
AGND
NB5
PROJECT : X31
Quanta Computer Inc.
Size Custom
Document Number
AUDIO CODEC ALC3258-CG
Rev
Date: Tuesday, August 09, 2016
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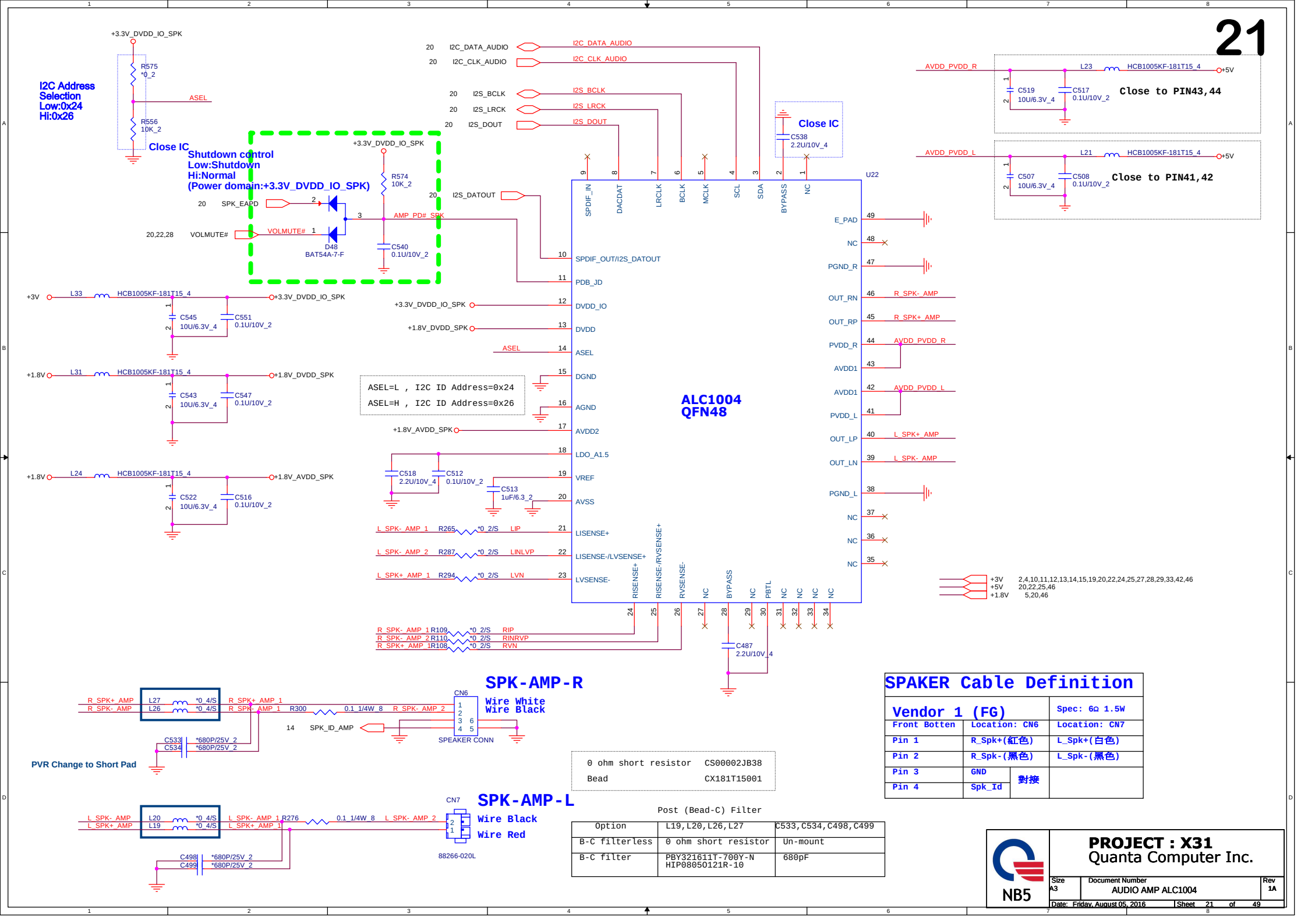
I2C Address Selection
Low:0x24
Hi:0x26
+3.3V_DVDD_IO_SPK
R575 *0_2
R556 10K_2
ASEL
Close IC
Shutdown control
Low:Shutdown
Hi:Normal
(Power domain:+3.3V_DVDD_IO_SPK)
R574 10K_2
20 SPK_EAPD
20,22,28 VOLMUTE#
D48 BAT54A-7-F
C540 0.1U/10V_2
20 I2C_DATA_AUDIO
20 I2C_CLK_AUDIO
20 I2S_BCLK
20 I2S_LRCK
20 I2S_DOUT
20 I2S_DATOUT
Close IC
C538 2.2U/10V_4
U22
SPDIF_IN
DACDAT
LRCLK
BCLK
MCLK
SCL
SDA
BYPASS
NC
SPDIF_OUT/I2S_DATOUT
PDB_JD
DVDD_IO
DVDD
ASEL
DGND
AGND
AVDD2
LDO_A1.5
VREF
AVSS
LISENSE+
LISENSE-/LVSENSE+
LVSENSE-
RISENSE+
RISENSE-/RVSENSE+
RVSENSE-
BYPASS
PBTL
E_PAD
PGND_R
OUT_RN
OUT_RP
PVDD_R
AVDD1
AVDD1
PVDD_L
OUT_LP
OUT_LN
PGND_L
ALC1004
QFN48
ASEL=L , I2C ID Address=0x24
ASEL=H , I2C ID Address=0x26
+3V L33 HCB1005KF-181T15_4 +3.3V_DVDD_IO_SPK
C545 10U/6.3V_4
C551 0.1U/10V_2
+1.8V L31 HCB1005KF-181T15_4 +1.8V_DVDD_SPK
C543 10U/6.3V_4
C547 0.1U/10V_2
+1.8V L24 HCB1005KF-181T15_4 +1.8V_AVDD_SPK
C522 10U/6.3V_4
C516 0.1U/10V_2
+1.8V_AVDD_SPK
C518 2.2U/10V_4
C512 0.1U/10V_2
C513 1uF/6.3_2
L_SPK- AMP_1 R265 *0_2/S LIP
L_SPK- AMP_2 R287 *0_2/S LINLVP
L_SPK+ AMP_1 R294 *0_2/S LVN
R_SPK- AMP_1 R109 *0_2/S RIP
R_SPK- AMP_2 R110 *0_2/S RINRVP
R_SPK+ AMP_1 R108 *0_2/S RVN
C487 2.2U/10V_4
AVDD_PVDD_R
L23 HCB1005KF-181T15_4 +5V
C519 10U/6.3V_4
C517 0.1U/10V_2
Close to PIN43,44
AVDD_PVDD_L
L21 HCB1005KF-181T15_4 +5V
C507 10U/6.3V_4
C508 0.1U/10V_2
Close to PIN41,42
+3V 2,4,10,11,12,13,14,15,19,20,22,24,25,27,28,29,33,42,46
+5V 20,22,25,46
+1.8V 5,20,46
SPK-AMP-R
R_SPK+_AMP L27 *0_4/S R_SPK+_AMP_1
R_SPK-_AMP L26 *0_4/S R_SPK-_AMP_1
R300 0.1_1/4W_8 R_SPK-_AMP_2
14 SPK_ID_AMP
CN6
SPEAKER CONN
Wire White
Wire Black
C533 *680P/25V_2
C534 *680P/25V_2
PVR Change to Short Pad
SPK-AMP-L
L_SPK-_AMP L20 *0_4/S L_SPK-_AMP_1
L_SPK+_AMP L19 *0_4/S L_SPK+_AMP_1
R276 0.1_1/4W_8 L_SPK-_AMP_2
CN7
88266-020L
Wire Black
Wire Red
C498 *680P/25V_2
C499 *680P/25V_2
0 ohm short resistor CS00002JB38
Bead CX181T15001
Post (Bead-C) Filter
Option | L19,L20,L26,L27 | C533,C534,C498,C499
B-C filterless | 0 ohm short resistor | Un-mount
B-C filter | PBY321611T-700Y-N HIP0805O121R-10 | 680pF
SPAKER Cable Definition
Vendor 1 (FG) | Spec: 6Ω 1.5W
Front Botten | Location: CN6 | Location: CN7
Pin 1 | R_Spk+(紅色) | L_Spk+(白色)
Pin 2 | R_Spk-(黑色) | L_Spk-(黑色)
Pin 3 | GND 對接
Pin 4 | Spk_Id
PROJECT : X31
Quanta Computer Inc.
NB5
Size A3
Document Number AUDIO AMP ALC1004
Rev 1A
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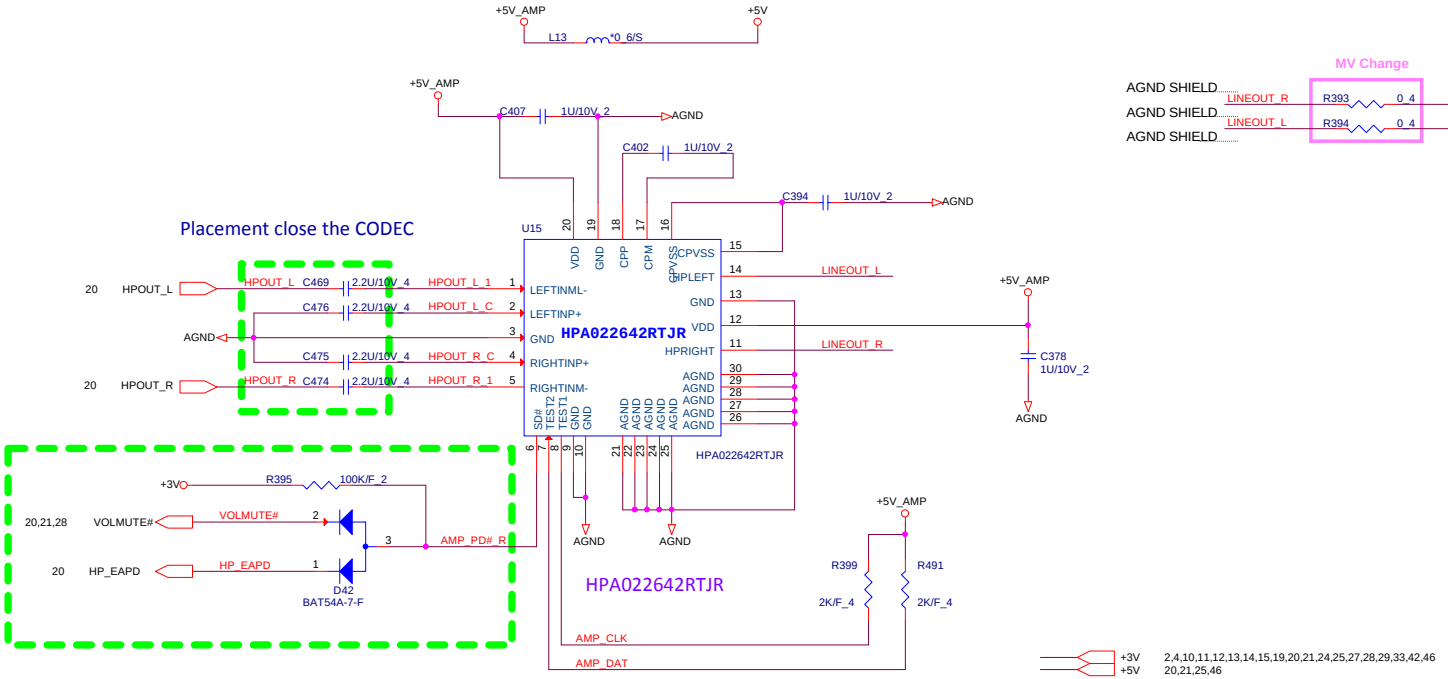
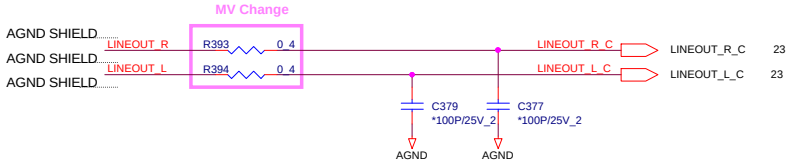
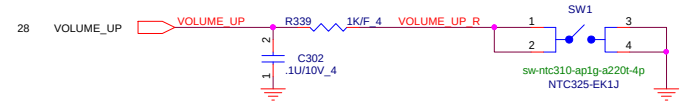
Head Phone out

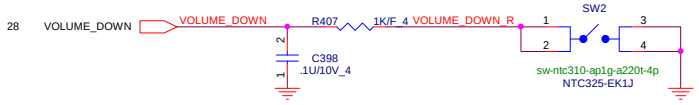


MV Change

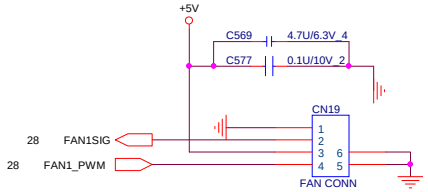


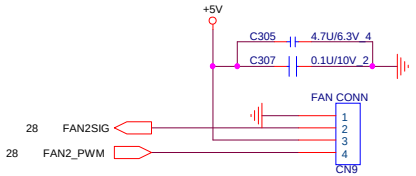
Volume up/down Button

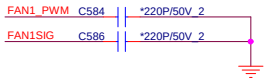


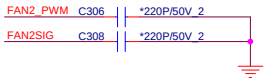


FAN









NB5	PROJECT : X31 Quanta Computer Inc.	
Size: Custom	Document Number: AUDIO AMP/FAN/Volume Button	Rev
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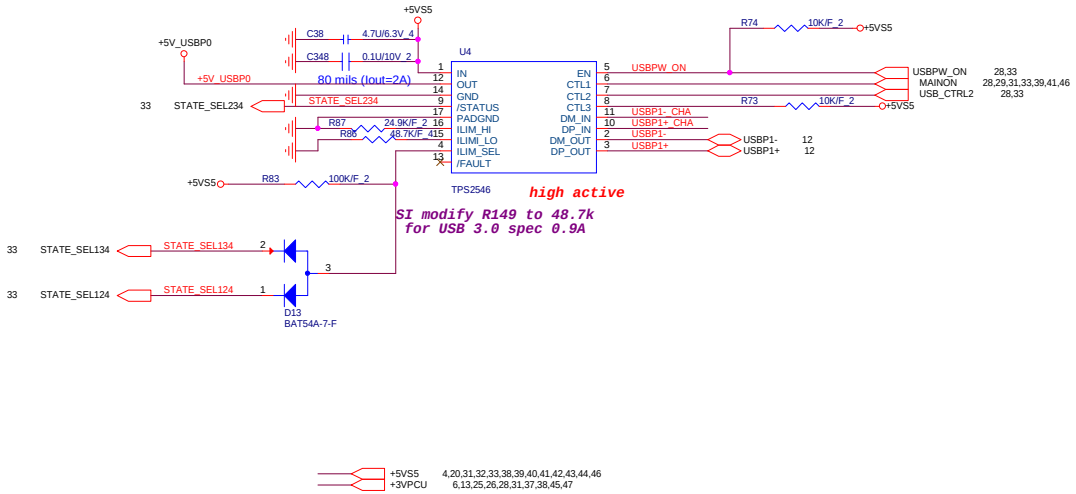
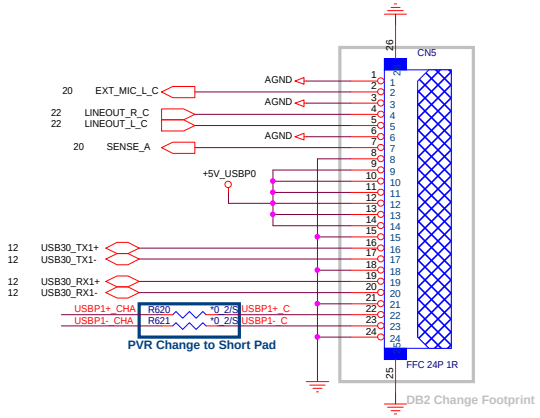
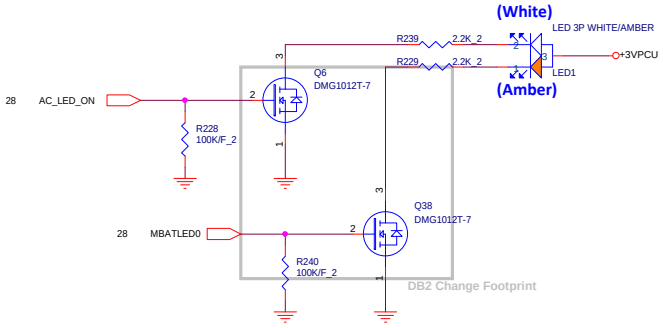
For Daughter USB3.0 CN



AUdio Combo Jack + USB3.0 Daughter Board



AC_IN / BATTERY LOW LED



NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB20/30	1A

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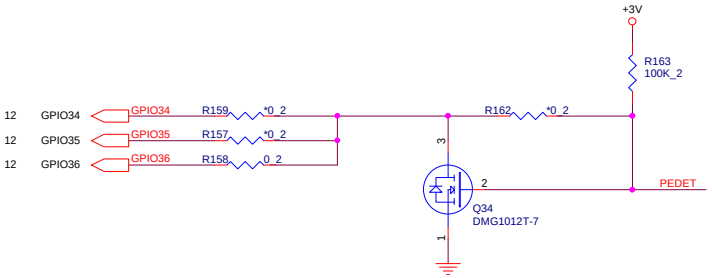
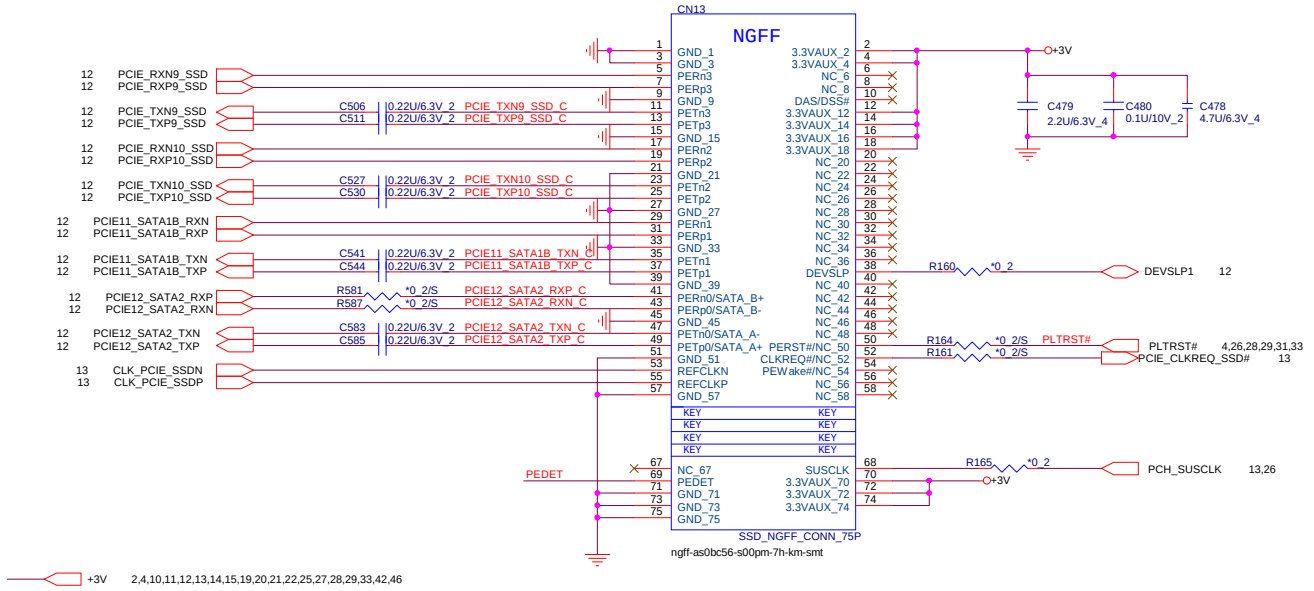
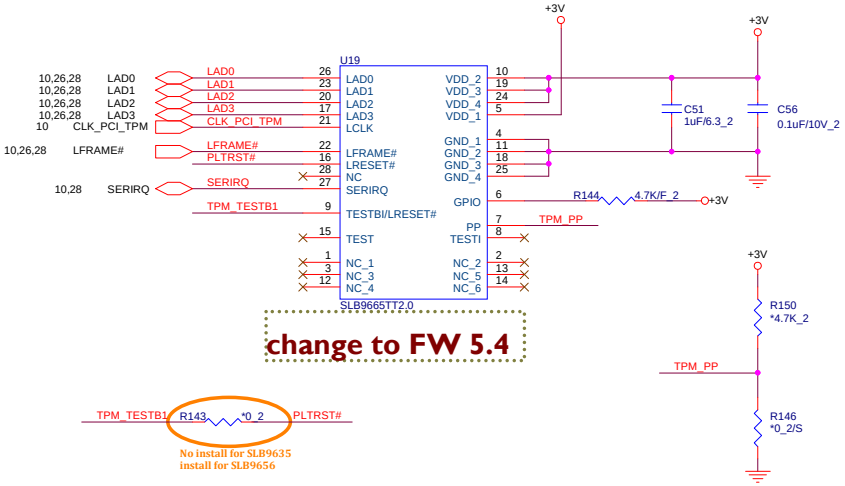
SSD CONN



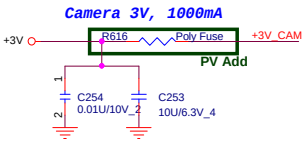
CONN: M KEY
MODULE: N/A



TPM (2.0)

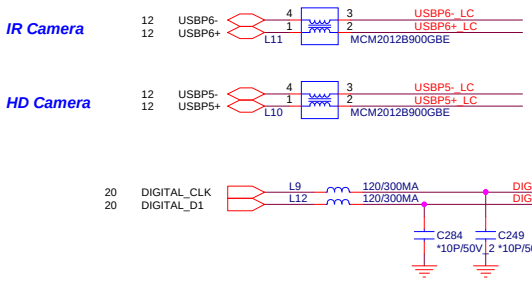


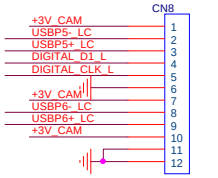
CAMERA CONN



Poly Fuse

Vender	Size	P/N
WYN	0805	DK150TPU025 (LP-ISML150)
LFI	0805	DK150TPU022 (0805L150ULYR)
PYS	0805	DK150TPU018 (SPR-P150)





NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NGFF HDD/TPM/CR	

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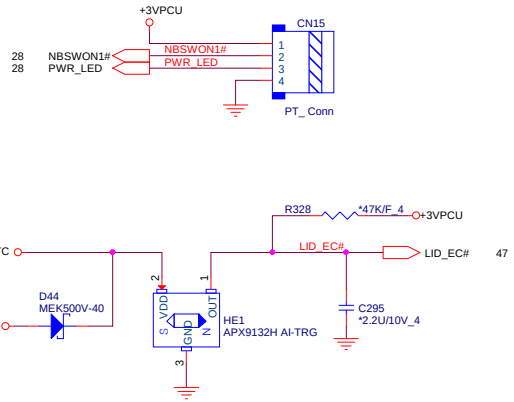
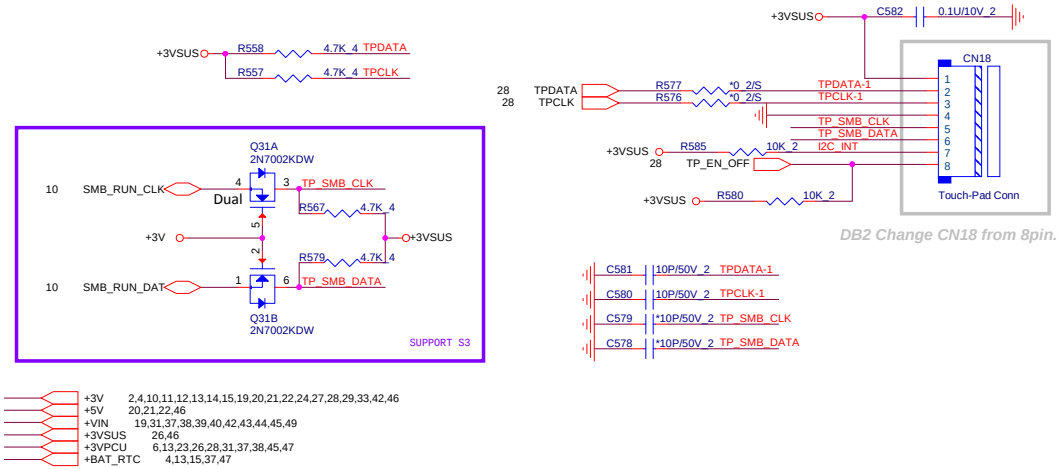
Power Botton Connector and LID



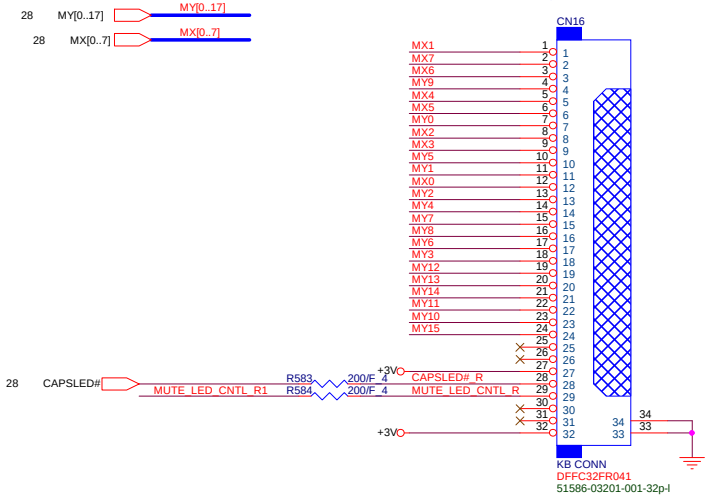
Touch Pad Connector

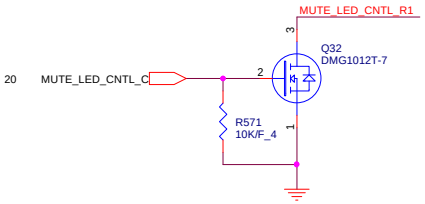


+3V 2,4,10,11,12,13,14,15,19,20,21,22,24,27,28,29,33,42,46
+5V 20,21,22,46
+VIN 19,31,37,38,39,40,42,43,44,45,49
+3VSUS 26,46
+3VPCU 6,13,23,26,28,31,37,38,45,47
+BAT_RTC 4,13,15,37,47

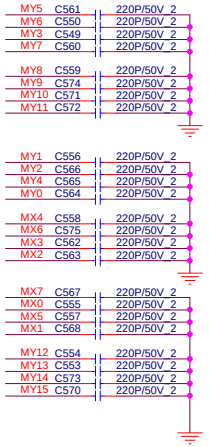
KEYBOARD Con Co-Lay

Not Pen Keyboard

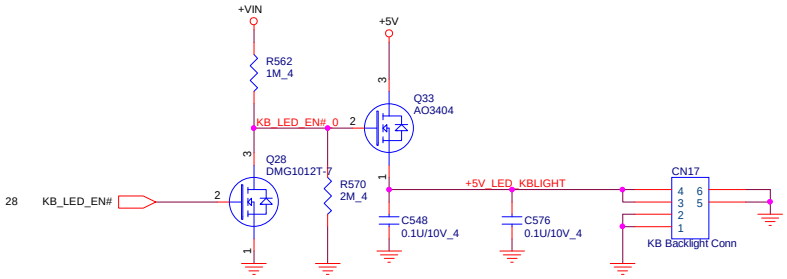




KEYBOARD PULL-UP



KB backlight



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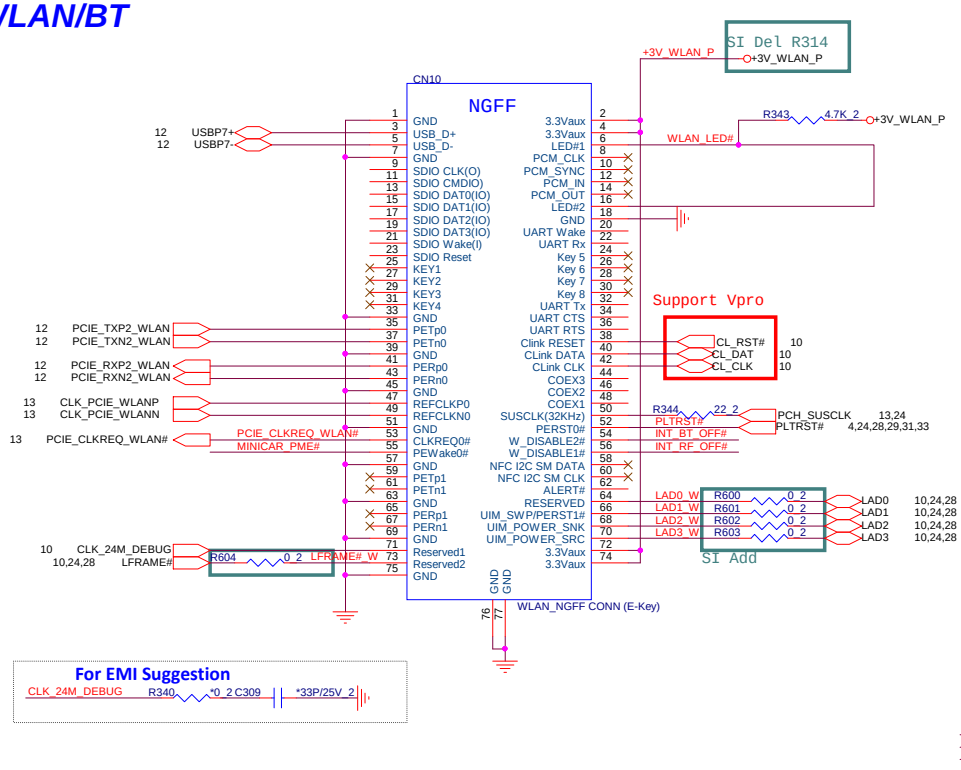
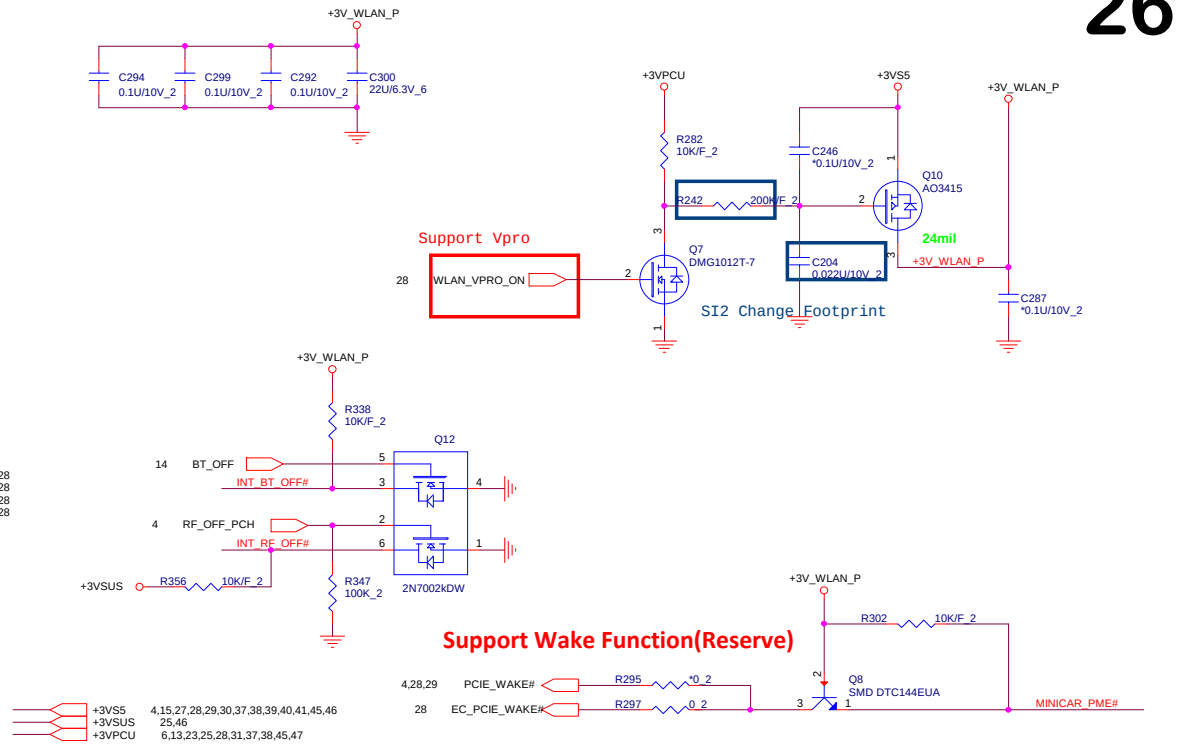
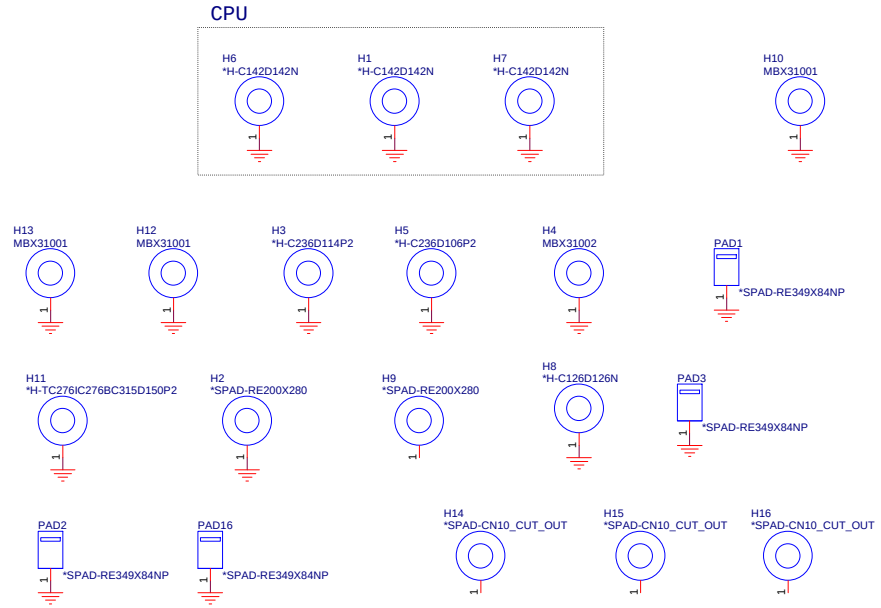
WLAN/BT

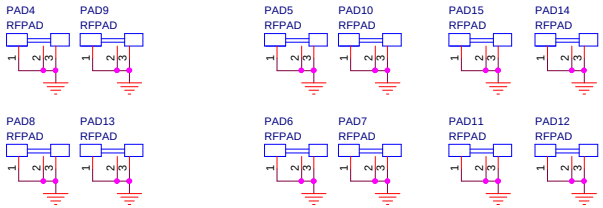




Hole



GND GUARD



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Quanta Computer Inc.

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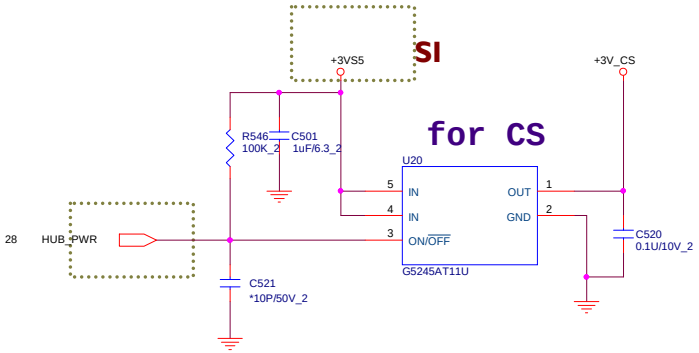
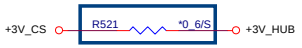
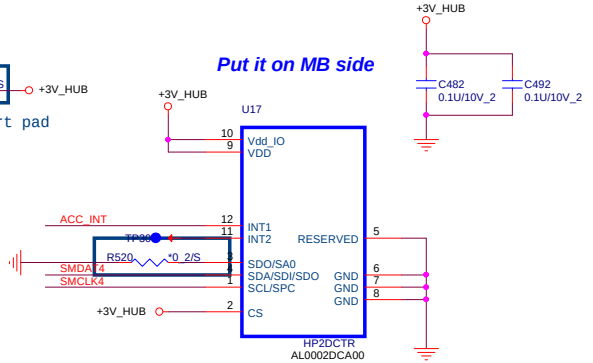
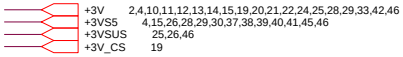
NB5

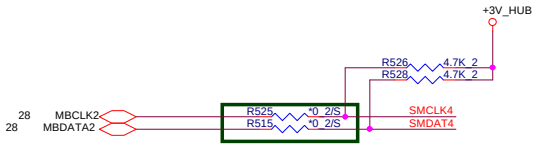
Accelerometer Sensor

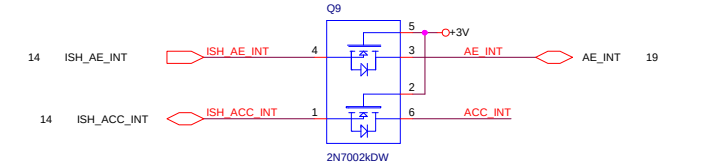


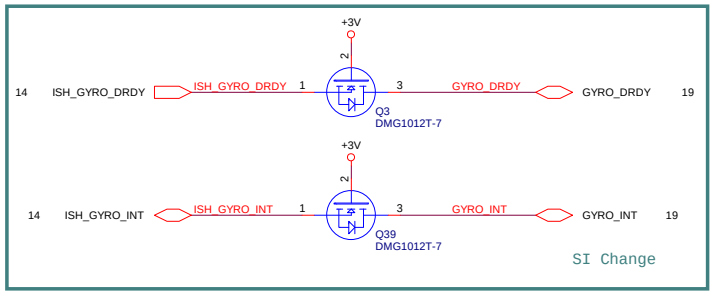


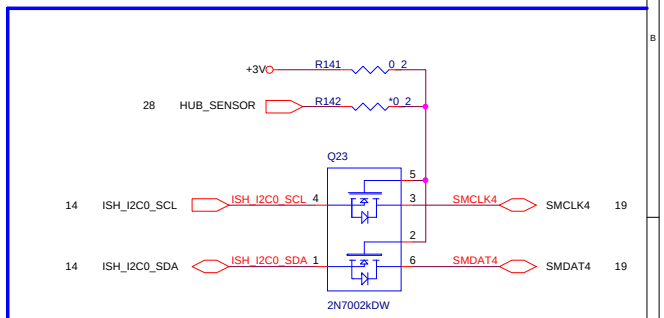












NB5

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Quanta Computer Inc.

Size	Document Number	Rev
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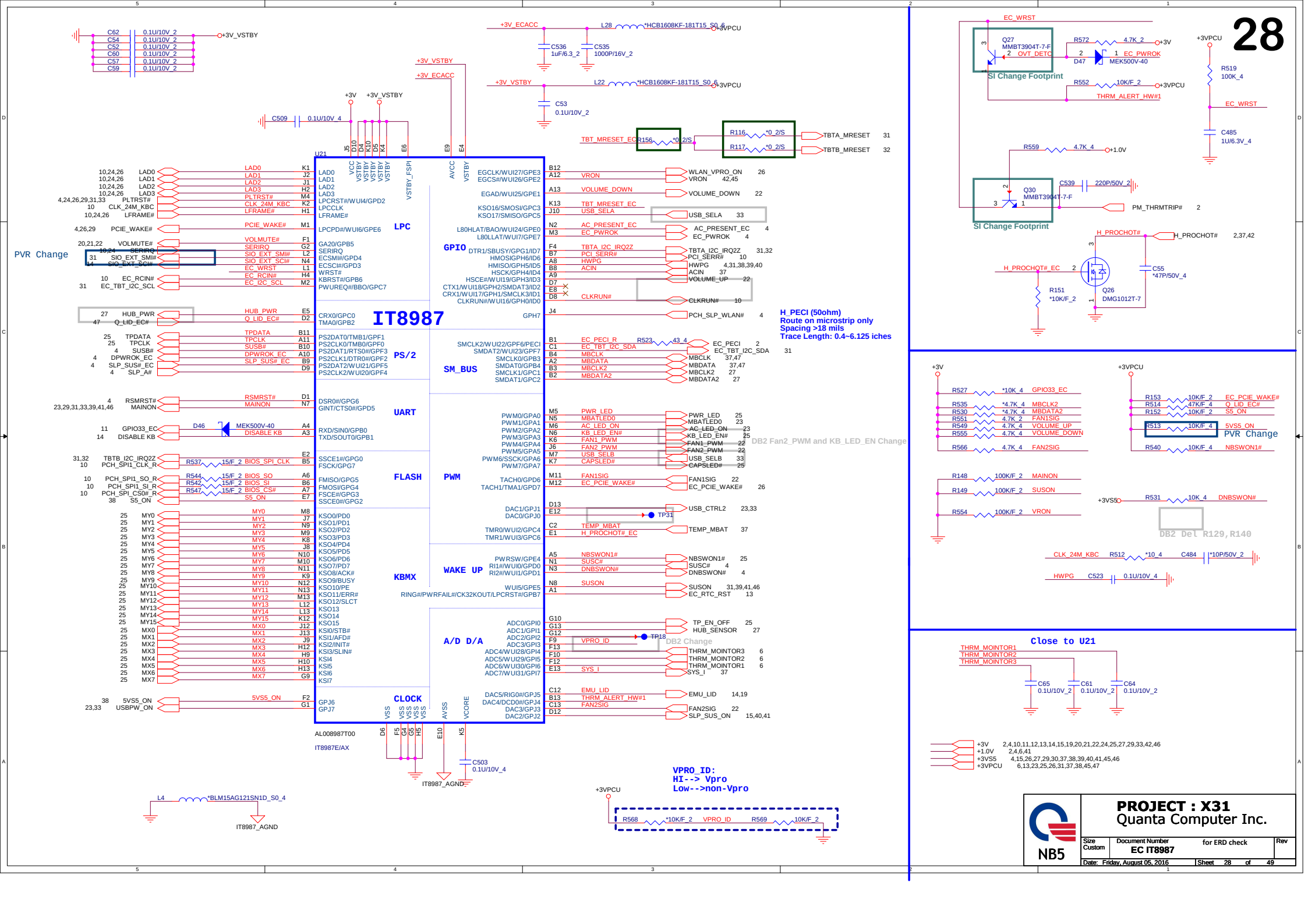
28
IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
PVR Change
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
DB2 Fan2_PWM and KB_LED_EN Change
DB2 Change
SI Change Footprint
Close to U21
VPRO_ID:
HI--> Vpro
Low-->non-Vpro
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25MHz, 30ppm, 10pF AR Crystal

C241 8.2P/50V_4
Y3 25MHZ +-10PPM
C245 8.2P/50V_4
TBT_XTAL_25_IN
TBT_XTAL_25_OUT
PVR Change

TP38 TBT_EE_CS_N
TP39 TBT_EE_DO
TP36 TBT_EE_DI
TP37 TBT_EE_CLK
TP35 TBT_EE_WP_N
TP34 TBT_HOLD_N
TP34-38 need place to BOT

8Mbit Flash (Mutual for AR and ACE)

VCC3V3_FLASH R402 *0_2/S
VCC3V3_FLASH_S
R489 3.32K/F_4
R416 3.32K/F_4
R408 3.32K/F_4
C401 0.1U/10V_2
R424 3.32K/F_4
U16 CS DO WP GND VCC HOLD CLK DI
W25Q80DVSSIG
TBT_EE_CS_N TBT_EE_DO TBT_EE_WP_N TBT_HOLD_N TBT_EE_CLK TBT_EE_DI
AKE3GF00N00
IC FLASH(8P) W25Q80DVZPIG(WSON)
SI Change Footprint
Silk: "NVM"
SPI EE: AR to/from NVM & ACE

AR_DDC_CLK R335 2.2K_2 VCC3P3_S0
AR_DDC_DAT R336 2.2K_2
TBT_HDMI_DDC_DATA R369 2.2K_2
TBT_HDMI_DDC_CLK R372 2.2K_2
TBT_CIO_PLUG_EVENT R397 10K/F_2 +VCC3P3_SX
TBT_I2C_SDA R333 2.2K_2
TBT_I2C_SCL R334 2.2K_2
TBTA_I2C_INT R329 10K/F_2
TBTB_I2C_INT R316 10K/F_2
PCIE_CLKREQ_TBT# R628 10K/F_2
Jun Modify 2016/04/14

TBT_SNK1_DDC_CLK R361 100K/F_2
AR_DDC_EN R332 100K/F_2
TBT_FORCE_PWR R322 100K/F_2
TBT_TMU_CLK_OUT R357 100K/F_2
DDI1_HPD0 R384 100K/F_2
DDI2_HPD0 R359 100K/F_2
TBTA_LSTX R269 1M/F_2
TBTA_HPD R337 100K/F_2
TBTA_LSRX R267 1M/F_2
TBTB_LSTX R105 1M/F_2
TBTB_HPD R324 100K/F_2
TBTB_LSRX R104 1M/F_2

PULL UP - HDMI MODE
DP/HDMI CONFIGURATION
DB2 Change
TBT_GPIO7 R392 *10K/F_2 +3VS5

NOTE:
ASSEMBLE R548, R549 if DPSRC
NOT IN USE
DB2 Change
TBT_GPIO7 R381 1M/F_2
TBT_SRC_HPD R325 1M/F_2

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

NOTE:
SNK0_DDC_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.
SNK1_DDC_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
SNK1_DDC_clk ?connect to 100k PD.

CPU PCIE TX
PCIE_TXP5_TBT PCIE_TXN5_TBT
PCIE_TXP6_TBT PCIE_TXN6_TBT
PCIE_TXP7_TBT PCIE_TXN7_TBT
PCIE_TXP8_TBT PCIE_TXN8_TBT
CLK_PCIE_TBTP CLK_PCIE_TBTN PCIE_CLKREQ_TBT#
PCIe GEN3
PCIE_RX0_P PCIE_RX0_N
PCIE_RX1_P PCIE_RX1_N
PCIE_RX2_P PCIE_RX2_N
PCIE_RX3_P PCIE_RX3_N
PCIE_REFCLK_100_IN_P PCIE_REFCLK_100_IN_N PCIE_CLKREQ_N
PCIE_TX0_P PCIE_TX0_N
PCIE_TX1_P PCIE_TX1_N
PCIE_TX2_P PCIE_TX2_N
PCIE_TX3_P PCIE_TX3_N
PERST_N
PCIE_RBIAS R360 3.01K/F_2
DB2 Change Footprint
PCIE_RXP5_TBT_C PCIE_RXN5_TBT_C PCIE_RXP6_TBT_C PCIE_RXN6_TBT_C PCIE_RXP7_TBT_C PCIE_RXN7_TBT_C PCIE_RXP8_TBT_C PCIE_RXN8_TBT_C
0.22uF/10V_2
PCIE_RXP5_TBT PCIE_RXN5_TBT PCIE_RXP6_TBT PCIE_RXN6_TBT PCIE_RXP7_TBT PCIE_RXN7_TBT PCIE_RXP8_TBT PCIE_RXN8_TBT
CPU PCIE RX
PLTRST# 4,24,26,28,31,33

CPU DDI1
DDI1_TX0_DP DDI1_TX0_DN
DDI1_TX1_DP DDI1_TX1_DN
DDI1_TX2_DP DDI1_TX2_DN
DDI1_TX3_DP DDI1_TX3_DN
DDI1_AUX_DP DDI1_AUX_DN
DDI1_HPD0
0.1U/10V_2
DDI1_TX0_DP_C DDI1_TX0_DN_C DDI1_TX1_DP_C DDI1_TX1_DN_C DDI1_TX2_DP_C DDI1_TX2_DN_C DDI1_TX3_DP_C DDI1_TX3_DN_C DDI1_AUX_DP_C DDI1_AUX_DN_C
SINK PORT 0
DPSNK0_ML0_P DPSNK0_ML0_N
DPSNK0_ML1_P DPSNK0_ML1_N
DPSNK0_ML2_P DPSNK0_ML2_N
DPSNK0_ML3_P DPSNK0_ML3_N
DPSNK0_AUX_P DPSNK0_AUX_N
DPSNK0_HPD
AR_DDC_CLK AR_DDC_DAT
DPSNK0_DDC_CLK DPSNK0_DDC_DATA
SOURCE PORT 0
DPSRC_ML0_P DPSRC_ML0_N
DPSRC_ML1_P DPSRC_ML1_N
DPSRC_ML2_P DPSRC_ML2_N
DPSRC_ML3_P DPSRC_ML3_N
DPSRC_AUX_P DPSRC_AUX_N
DPSRC_HPD
DPSRC_RBIAS R342 14K_2
TBT_SRC_HPD
For HDMI 1.4 ouput, Monster not support

CPU DDI2
DDI2_TX0_DP DDI2_TX0_DN
DDI2_TX1_DP DDI2_TX1_DN
DDI2_TX2_DP DDI2_TX2_DN
DDI2_TX3_DP DDI2_TX3_DN
DDI2_AUX_DP DDI2_AUX_DN
DDI2_HPD0
0.1U/10V_2
DDI2_TX0_DP_C DDI2_TX0_DN_C DDI2_TX1_DP_C DDI2_TX1_DN_C DDI2_TX2_DP_C DDI2_TX2_DN_C DDI2_TX3_DP_C DDI2_TX3_DN_C DDI2_AUX_DP_C DDI2_AUX_DN_C
SINK PORT 1
DPSNK1_ML0_P DPSNK1_ML0_N
DPSNK1_ML1_P DPSNK1_ML1_N
DPSNK1_ML2_P DPSNK1_ML2_N
DPSNK1_ML3_P DPSNK1_ML3_N
DPSNK1_AUX_P DPSNK1_AUX_N
DPSNK1_HPD
TBT_SNK1_DDC_CLK AR_DDC_EN
DPSNK1_DDC_CLK DPSNK1_DDC_DATA
DPSNK_RBIAS R363 14K_2
DB2 Change Footprint
LC GPIO
GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7 GPIO_8
TBT_I2C_SDA TBT_I2C_SCL TBT_EE_WP_N TBT_TMU_CLK_OUT PCIE_WAKE# TBT_CIO_PLUG_EVENT TBT_HDMI_DDC_DATA TBT_HDMI_DDC_CLK TBT_GPIO7
PCIE_WAKE# 4,26,28
D52 MEK500V-40 TBT_HTPLG 14
+3V PV Add R617 10K/F_2
TBT_CIO_PLUG_EVENT_N:
Connect to PCH (Make sure PCH supports SCI)
POC GPIO
POC_GPIO_0 POC_GPIO_1 POC_GPIO_2 POC_GPIO_3 POC_GPIO_4 POC_GPIO_5 POC_GPIO_6
TBTA_I2C_INT TBTB_I2C_INT TBTA_ACE_GPIO0 TBT_FORCE_PWR BATLOW# MAINON TBTB_ACE_GPIO0
R315 *0_2/S R318 *0_2/S
BATLOW# R619 10K_2 +VCC3P3_SX PV Add
Misc
TEST_EN TBT_TEST_EN R317 100/F_2
TEST_PWR_GOOD TBT_TEST_PWG R385 100/F_2
RESET_N TBT_RESET_N 31

TDI TMS TCK TDO
TBT_TDI TBT_TMS TBT_TCK TBT_TDO
MISC
XTAL_25_IN XTAL_25_OUT
TBT_XTAL_25_IN TBT_XTAL_25_OUT
EE_DI EE_DO EE_CS_N EE_CLK
TBT_EE_DI TBT_EE_DO TBT_EE_CS_N TBT_EE_CLK
RBIAS RSENSE
+/-0.5% R313 4.75K/F_2 TBT_RBIAS TBT_RSENSE

TBT PORT A
TBTA_CA2HD_1_P TBTA_CA2HD_1_N
TBTA_HD2CA_1_P TBTA_HD2CA_1_N
TBTA_HD2CA_0_P TBTA_HD2CA_0_N
TBTA_CA2HD_0_P TBTA_CA2HD_0_N
TBTA_DPSRC_AUX_P TBTA_DPSRC_AUX_N
TBTA_USB2_D_P TBTA_USB2_D_N
TBTA_LSTX TBTA_LSRX TBTA_HPD
0.22uF/10V_2
TBTA_TX1_P TBTA_TX1_N TBTA_TX0_P TBTA_TX0_N
0.1uF/10V_2
TBTA_AUX_P TBTA_AUX_N
TBT_PORTS
Port A
PA_RX1_P PA_RX1_N
PA_TX1_P PA_TX1_N
PA_TX0_P PA_TX0_N
PA_RX0_P PA_RX0_N
PA_DPSRC_AUX_P PA_DPSRC_AUX_N
PA_USB2_D_P PA_USB2_D_N
PA_LSTX PA_LSRX PA_DPSRC_HPD
POC
PA_USB2_RBIAS R101 499/F_2 PA_USB2_RBIAS
DB2 Change Footprint
PORT B
PB_RX1_P PB_RX1_N
PB_TX1_P PB_TX1_N
PB_TX0_P PB_TX0_N
PB_RX0_P PB_RX0_N
PB_DPSRC_AUX_P PB_DPSRC_AUX_N
PB_USB2_D_P PB_USB2_D_N
PB_LSTX PB_LSRX PB_DPSRC_HPD
POC
PB_USB2_RBIAS R102 499/F_2 PB_USB2_RBIAS
DB2 Change Footprint
TBTB_CA2HD_1_P TBTB_CA2HD_1_N
TBTB_HD2CA_1_P TBTB_HD2CA_1_N
TBTB_HD2CA_0_P TBTB_HD2CA_0_N
TBTB_CA2HD_0_P TBTB_CA2HD_0_N
TBTB_DPSRC_AUX_P TBTB_DPSRC_AUX_N
TBTB_USB2_D_P TBTB_USB2_D_N
TBTB_LSTX TBTB_LSRX TBTB_HPD
TBT PORT B

THERMDA THERMDA
PCIE_ATEST
TEST_EDM
FUSE_VQPS_64 FUSE_VQPS_128
MONDC_CIO_0 MONDC_CIO_1
DEBUG
MONDC_SVR
ATEST_P ATEST_N
USB2_ATEST
MONDC_DPSNK_0 MONDC_DPSNK_1
MONDC_DPSRC
U6A AR_4C

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

JTAG
DB2 Change
VCC3P3_LC
TBT_TDI R355 10K/F_2
TBT_TMS R345 10K/F_2
TBT_TCK R346 10K/F_2
TBT_TDO R354 10K/F_2

+3V 2,4,10,11,12,13,14,15,19,20,21,22,24,25,27,28,33,42,46
+3VS5 4,15,26,27,28,30,37,38,39,40,41,45,46
VCC3P3_S0 30
VCC3P3_LC 30
+VCC3P3_SX 30
VCC3V3_FLASH 31,32

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A
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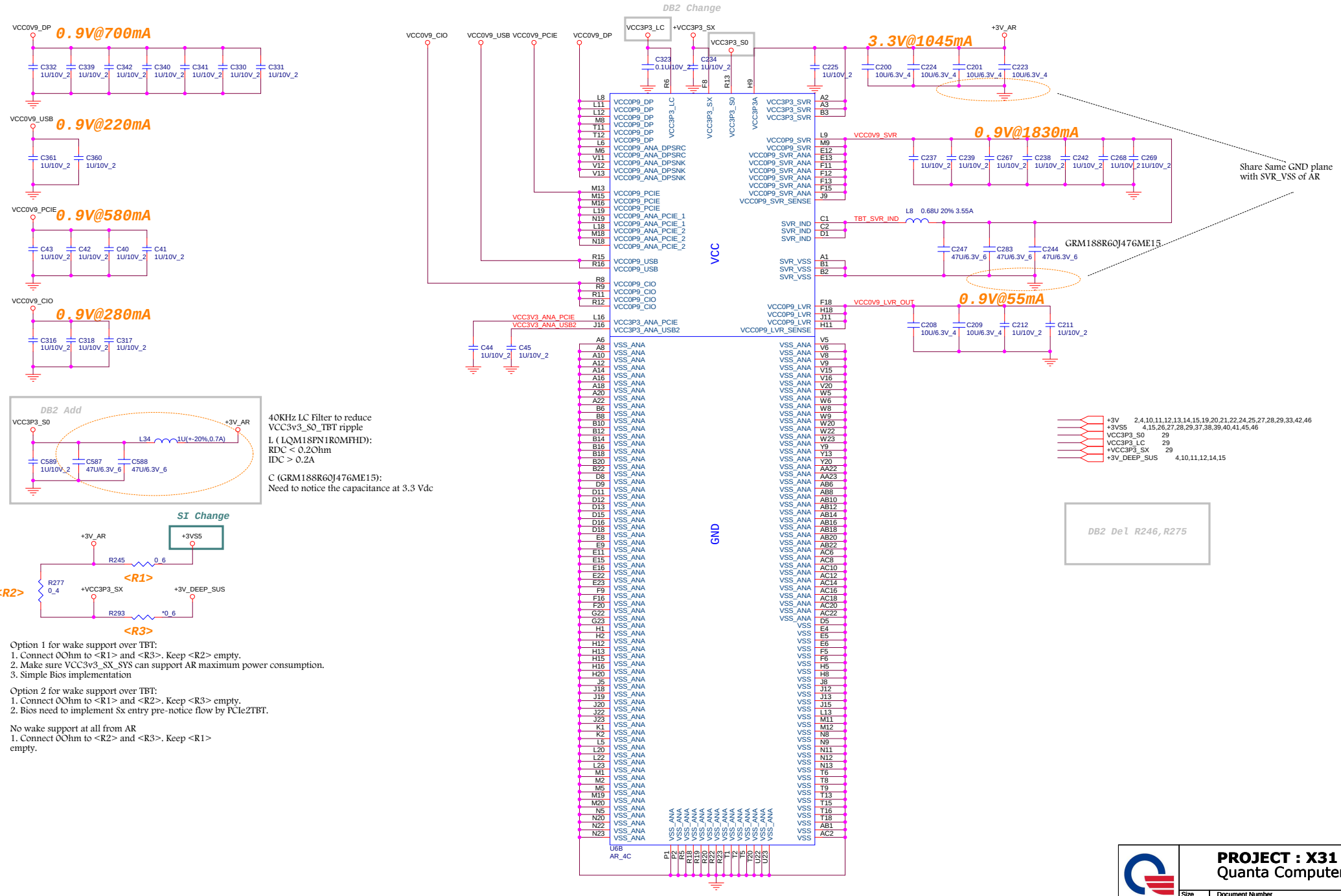

Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A
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Port A Controller - ACE

TPS65982 (ACE) -
USB3.1 PD

DB2 Del R414,R413

PP_EXT circuit

W = 200 mils

W = 120 mils

Supporting up to 60W to VBUS
ACE configuration:
* SENSEP & SENSEN should be connected to 10mOhm resistor
* PP_HV should be tied to GND.

0126 Add

SI Change

PV Change Power Plan

I2C_ADDR
'0' - Sets ACE as Primary
'1' - Sets ACE as Secondary

I2C1
Connect to AR and PD2

I2C2
Directly to EC

FOR EMI

DB2 Change

Primary

Type-C USB1 Top

Type-C USB1 Bot

Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes

SI Change. Delete MOS

for TYPE-C B Port Dead Battery used

Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS Power through the PP_EXT path (Host Charging mode from USBC)
BUSPOWERZ > 2.4v --> Disabling system power from VBUS (Host providing power to the USBC)

PV Change Footprint

PVR Change

PVR Add

DB2 Change Footprint

DB2 Add

NOTE:
GPIO MAPPING SUBJECT TO CHANGES BASED ON VENDOR REQURIEMETNS. PLEASE REFER TO DATASHEET FOR MORE DETAILS.

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NB5	Size: — Document Number: AR - TBT (USB2 & DP Part) Rev: 1A
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Port B Controller - ACE

TPS65982 (ACE) -
USB3.1 PD

PP_EXT circuit

W = 120 mils

W = 120 mils

W = 200 mils

Supporting up to 60W to VBUS
ACE configuration:
* SENSEP & SENSEN should be connected to 10mOhm resistor
* PP_HV should be tied to GND.

DB2 Del R430,R504

DB2 Change

I2C_ADDR
'0' - Sets ACE as Primary
'1' - Sets ACE as Secondary

I2C1
Connect to AR and PD2

I2C2
Directly to EC

Secondary

Type-C USB1 Top

Type-C USB1 Bot

Tie RPD_Gn to C_CCn pins to support no-power or dead-battery modes

PV Change Footprint

DB2 Add

SI Change. Delete MOS

SI2 Change Footprint

SI2 Del R331

Dual Power Role:
BUSPOWERZ < 0.8v --> Receiving VBUS Power through the PP_EXT path (Host Charging mode from USBC)
BUSPOWERZ > 2.4v --> Disabling system power from VBUS (Host providing power to the USBC)

NOTE:
GPIO MAPPING SUBJECT TO CHANGES BASED ON VENDOR REQURIEMETNS. PLEASE REFER TO DATASHEET FOR MORE DETAILS.

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Size	Document Number: AR - TBT (USB2 & DP Part) — Rev 1A
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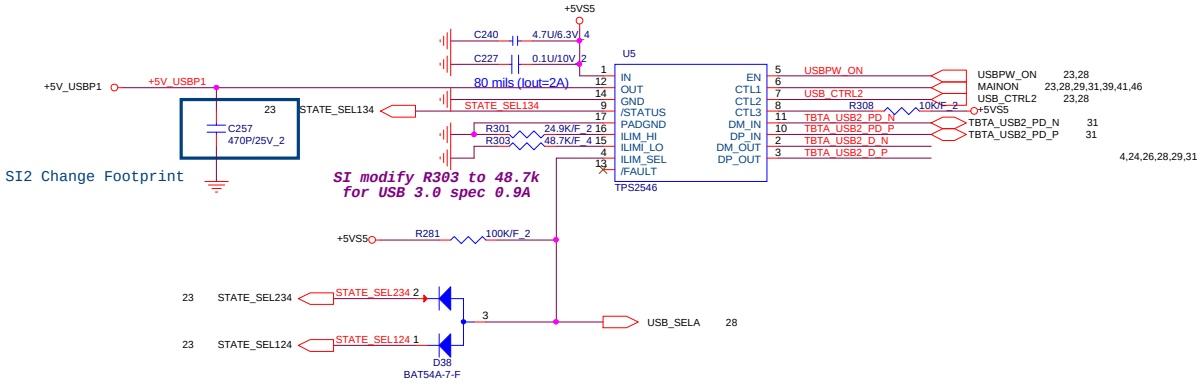
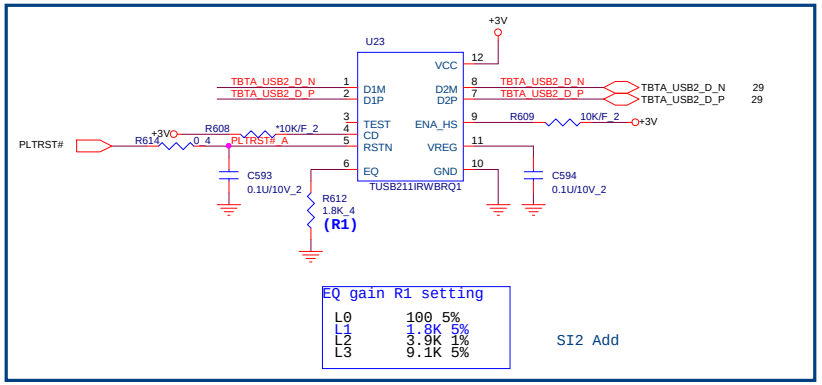
NB5

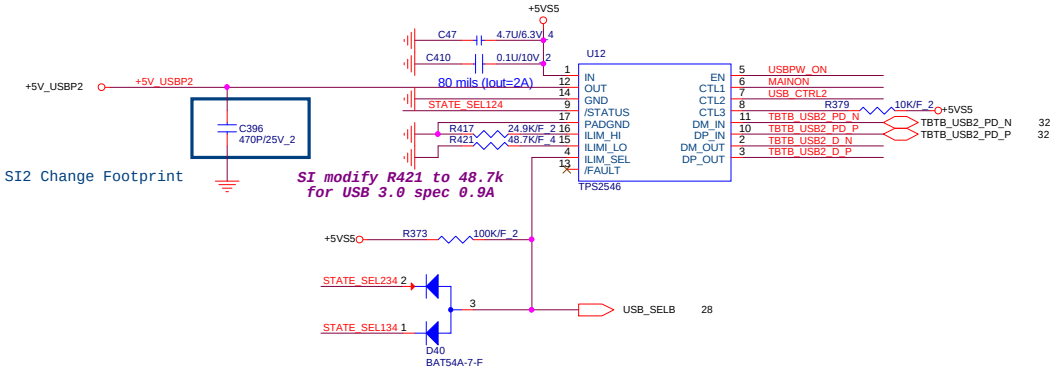
PortA Support BC1.2

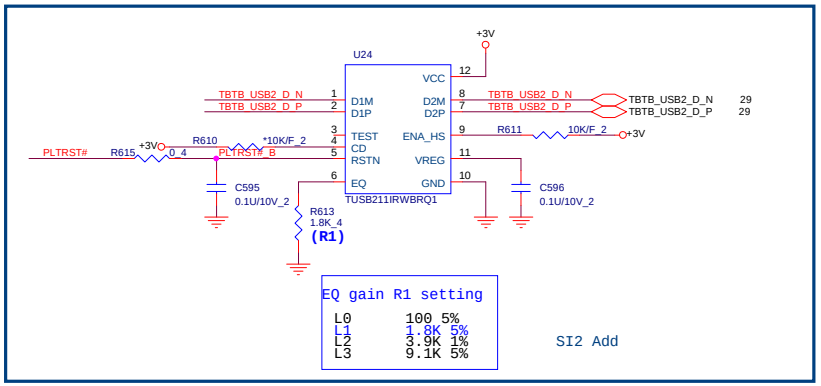




+5VS5 4,20,23,31,32,38,39,40,41,42,43,44,46
+5V_USBP1 31
+5V_USBP2 32

PortB Support BC1.2





NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A

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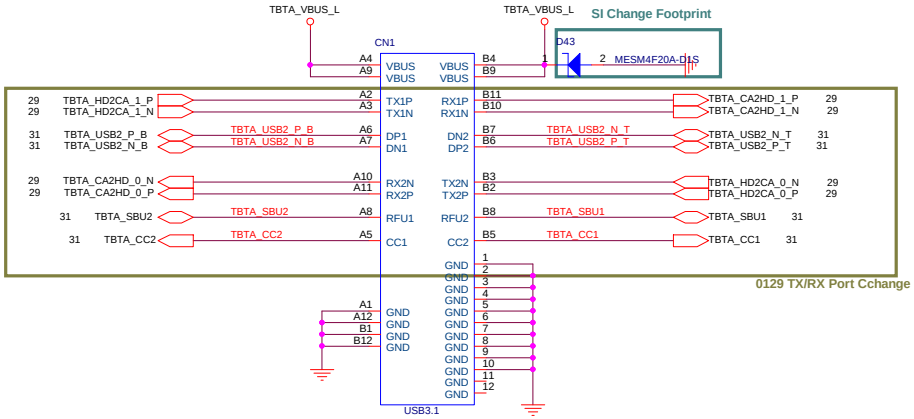
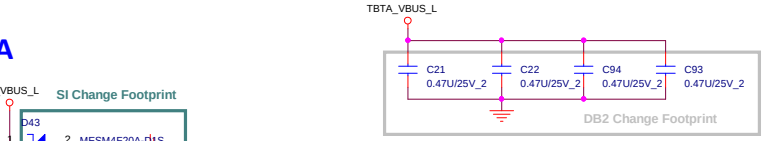
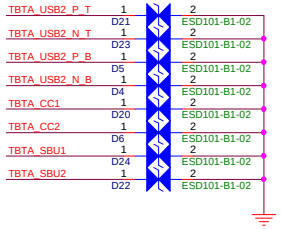
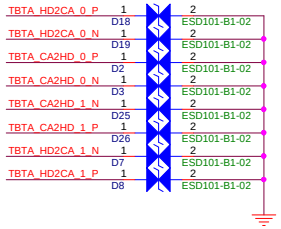
USB Type-C Port A

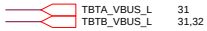




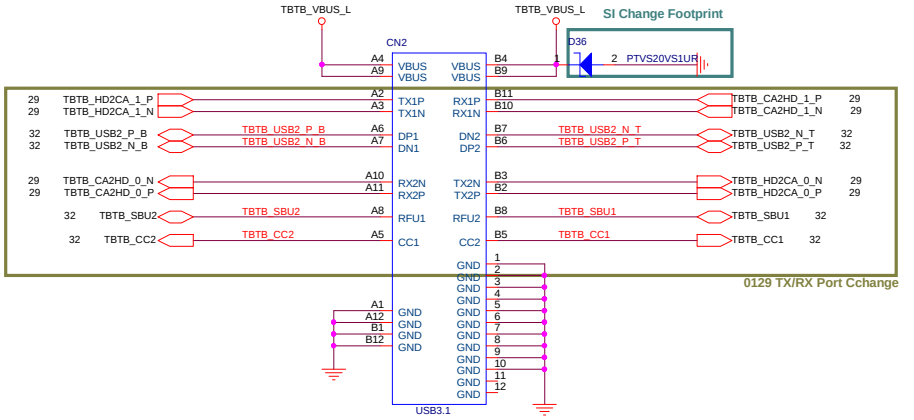
WAIT ESD FP

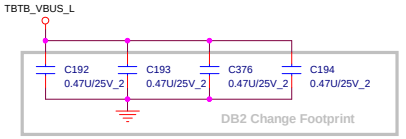


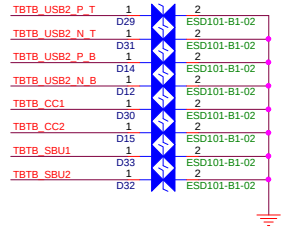


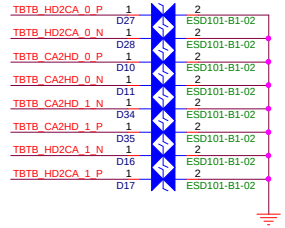


USB Type-C Port B









NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A

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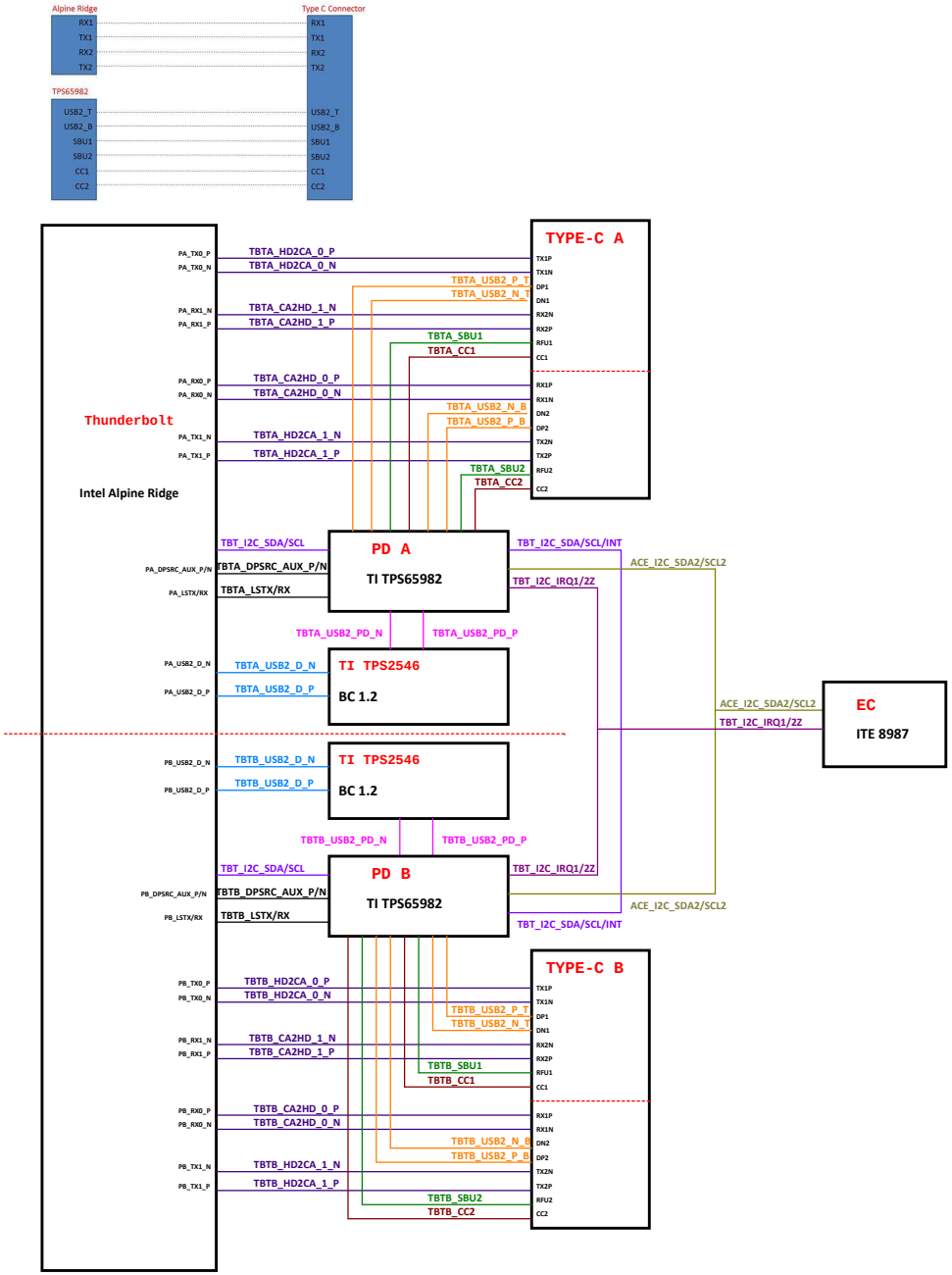
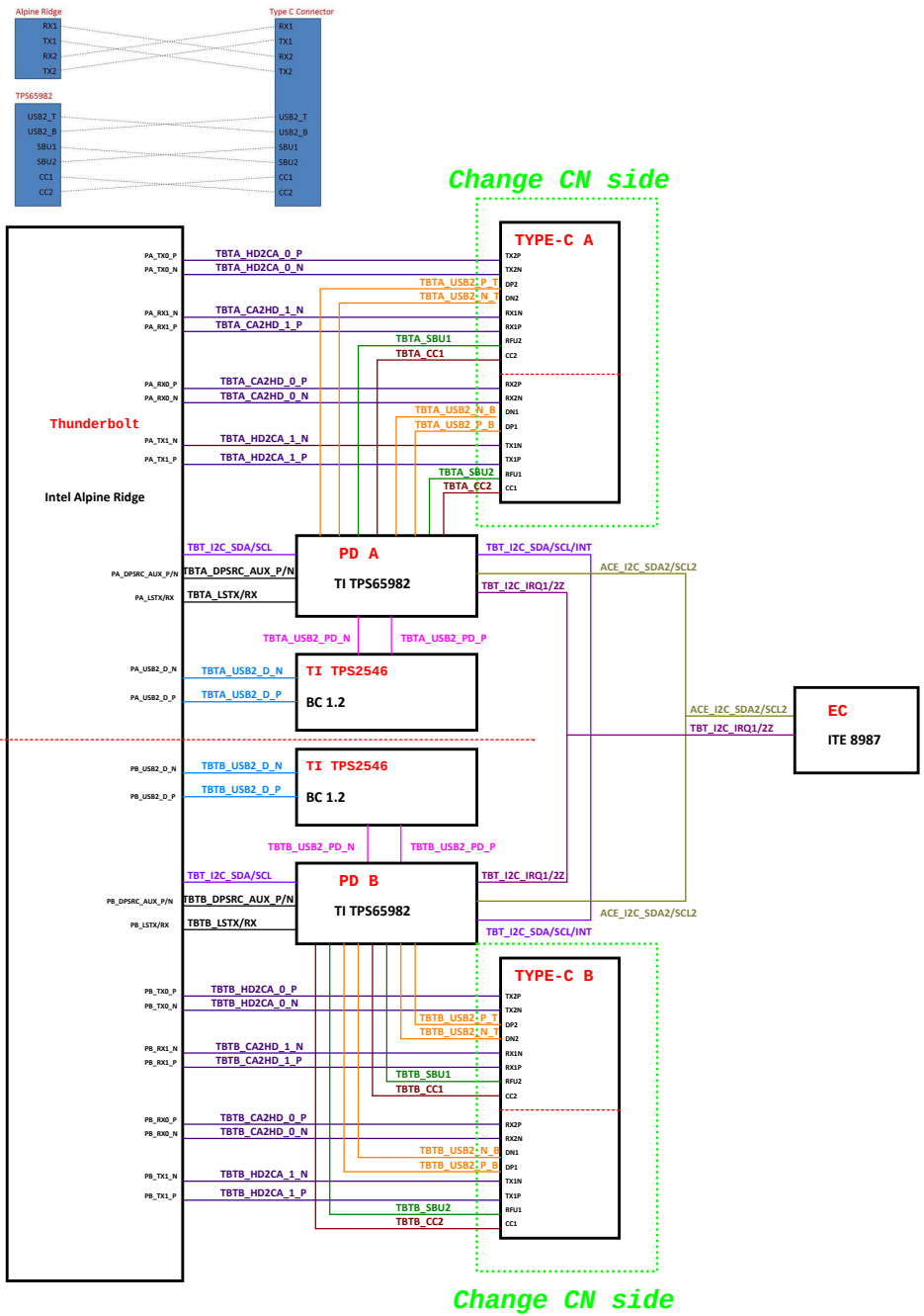
Keep the same Typc-C CN as the same as Intel AR CRB Board



Change CIO connection in Type-C Connector side



PROJECT : X31
Quanta Computer Inc.
NB5
PORT ASSIGNMENT

Dead Battery Block

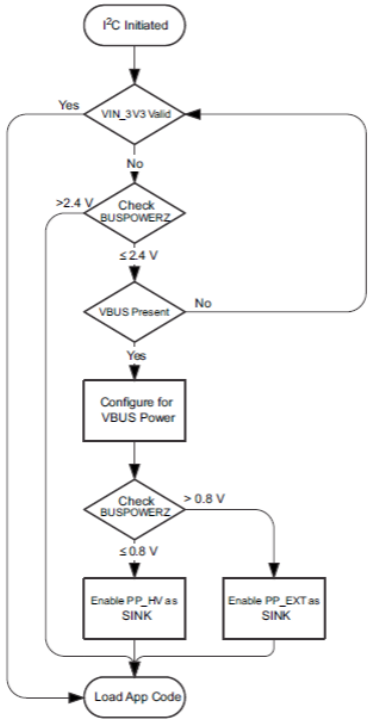


Figure 65. Dead-Battery Condition Flow Diagram

USB Type-C Connector – Pinout and Alignment

Receptacle (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

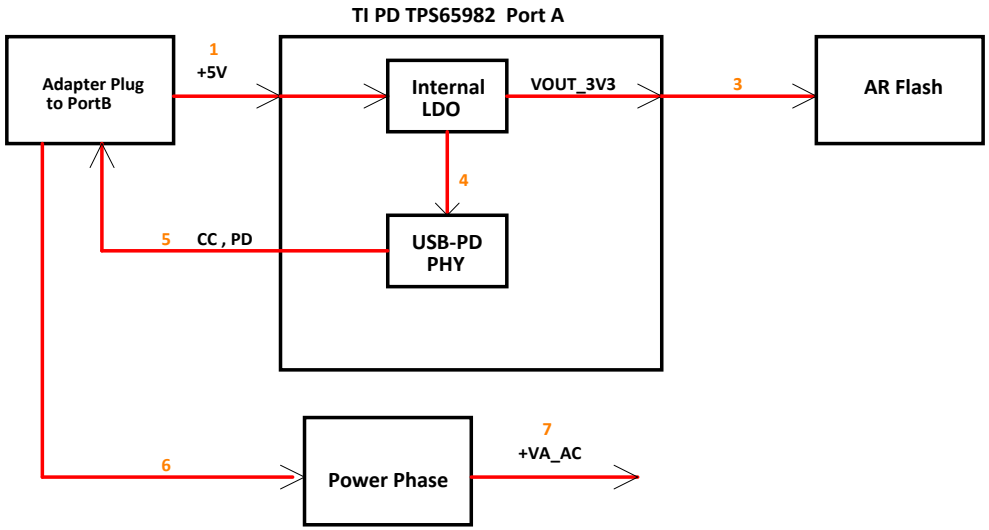
USB3.0 USB2.0 USB3.0

Normal Plug

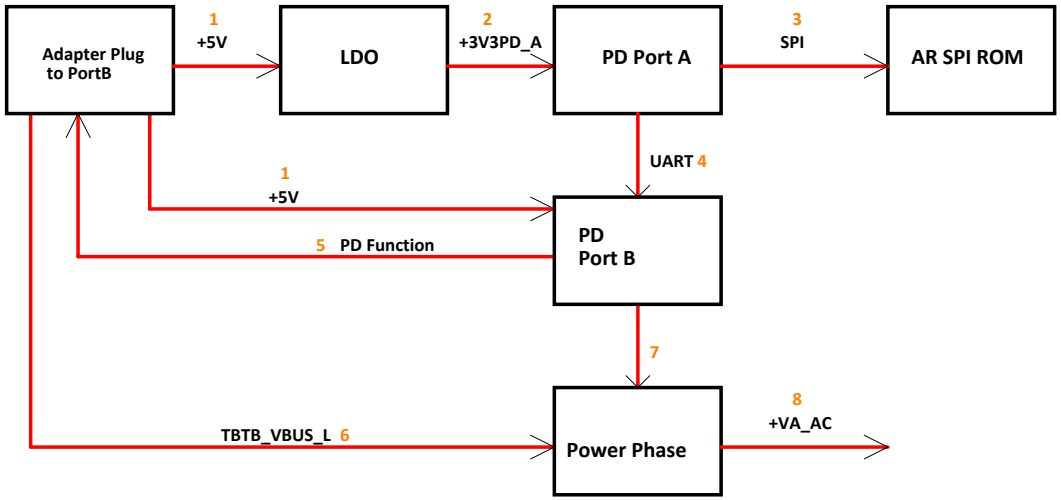
Reverse Plug

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

PortA Dead Battery



PortB Dead Battery



NB5	PROJECT : X31 Quanta Computer Inc.	
	Size: Custom Document Number: Load switch IC	Rev
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+VIN 19,25,31,38,39,40,42,43,44,45,49
+VA_AC 48
+3VPCU 6,13,23,25,26,28,31,38,45,47
+BAT_RTC 4,13,15,25,47
+1.8V_DEEP_SUS 9,15,40,46

+VA_AC
PC268 0.1U/25V_4
PC269 10U/25V_8
PR243 RC1206-R020
PR244 *0_2/S
PR245 *0_2/S
BUCKBOOST_CSP
BUCKBOOST_CSN
PR251 1/F_4
PR252 1/F_4

+PRWSRC
PC270 10U/25V_8
PC271 10U/25V_8
PC272 10U/25V_8
PC273 10U/25V_8
PC274 0.1U/25V_4
PC264 22u/25V_7343_1.4H
PQ37 FDMS3664S
PL22 1uH/8.7A_10x10x1.5H
9237_PHASE1
9237_PHASE2
PR249 *2.2_6
PR250 *2.2_6
PC278 *2200P/50V_4
PC279 *2200P/50V_4

+VIN
PC265 0.1U/25V_4
PC266 10U/25V_8
PC267 10U/25V_8
PC262 *22u/25V_7343_1.4H
PQ41 FDMS3664S
PR246 RC1206-R010
PR247 *0_2/S
PR248 *0_2/S
PC275 10U/25V_8
PC276 10U/25V_8
PC277 0.1U/25V_4
+BATCHG
BATTERY_SRP
BATTERY_SRN
PR253 1/F_4
PR254 1/F_4
PC280 4700P/25V_4
PQ36 AON6413

9237_LGATE1
PC281 0.22U/25V_6
PR255 1_6
9237_BOOT1
9237_LGATE2
9237_PHASE1
9237_UGATE1
PC282 *0.1U/25V_4
PC284 1U/6.3V_4
PC285 *0.1U/25V_4
PR256 1_6
PC283 0.22U/25V_6
PR257 *0_4/S
PC286 *0.1U/25V_4
PC288 1U/6.3V_4
PC289 *0.1U/25V_4

PU20 ISL9237HRZ-T
CSIN
CSIP
DCIN
ADP
ACIN
PROG
SDA
SCL
PSYS
PROCHOT#
AMON/BMON
VDD
VDDP
COMP
ACOK
UGATE1
PHASE1
BOOT1
LGATE1
LGATE2
BOOT2
PHASE2
UGATE2
VSYS
CSOP
CSON
BGATE
VBAT
BATGONE
ASGATE
OTGPG/CMOUT
OTGEN/CMIN
GND

+VIN
PD13 1N4448WS-7-F
PD14 1N4448WS-7-F
PR258 10_6
PC287 1U/25V_4
PC290 0.1U/16V_4
PR259 392K/F_4
PR261 158K/F_4
3S/Fsw=733KHz/ 0.1A
9237_ACIN
Minimum: 3.93V
PR260 105K/F_4
9237_DCIN
9237_ACIN
9237_PROG
MBDATA
MBCLK
PR262 *0_4/S
PR263 *0_4/S
9237_SDA
9237_SCL
42 PMON
PR264 *0_4/S
9237_PSYS
PR265 *6.04K/F_4
H_PROCHOT#
PR266 *0_4/S
PR269 *0_4/S
28 SYS_I
9237_AMON/BMON
PC291 1000P/50V_4
PC292 100P/50V_4
+VDD
VDD=5V
PC293 4.7U/10V_4
PR271 4.7_6
PC294 4.7U/10V_4
9237_COMP
PC295 *470P/50V_4
PR273 1K/F_4
PC296 0.01U/50V_4
PR270 100K/F_4
PR272 150K/F_4
ACIN 28
PR268 100K/F_4
9237_BATGONE
TEMP_MBAT
PC299 10P/50V_4
PR267 100K/F_4
9237_ASGATE
9237_CMOUT
9237_OTGEN/CMIN
TP33
TP32

+3VS5
+VIN
PR276 *1M_4
PR275 *249K/F_4
+1.8V_DEEP_SUS
PR277 *267K/F_4
PC297 *0.1U/16V_4
PC298 *0.1U/16V_4
PU21 *G1363
PR274 *100/F_4
H_PROCHOT# 2,28,42

+BAT_RTC
PR233 100/F_4
PC255 100P/50V_4
PD11 *PDZ5.6B
RTC
CN14 51279-0100T-V01
14"
BAT+
SMD
SMC
GND
B/I
B_TEMP_MBAT
3S1P/58.2 WH
PR278 100/F_4
BATT+
PC227 0.1U/25V_4
PR222 330_4
PR227 330_4
MBDATA 28,47
MBCLK 28,47
PR54 200K/J_4
+3VPCU
PR55 1K/F_4
28 TEMP_MBAT
PC201 0.01U/50V_4
PC241 0.01U/50V_4
PC246 *100P/50V_4
PC248 *100P/50V_4
Place this cap close to EC

+VBATT

PROJECT : X31
Quanta Computer Inc.
NB5
Size Custom
Document Number Charger(ISL9237)
Rev 1A
Date Friday, August 05, 2016
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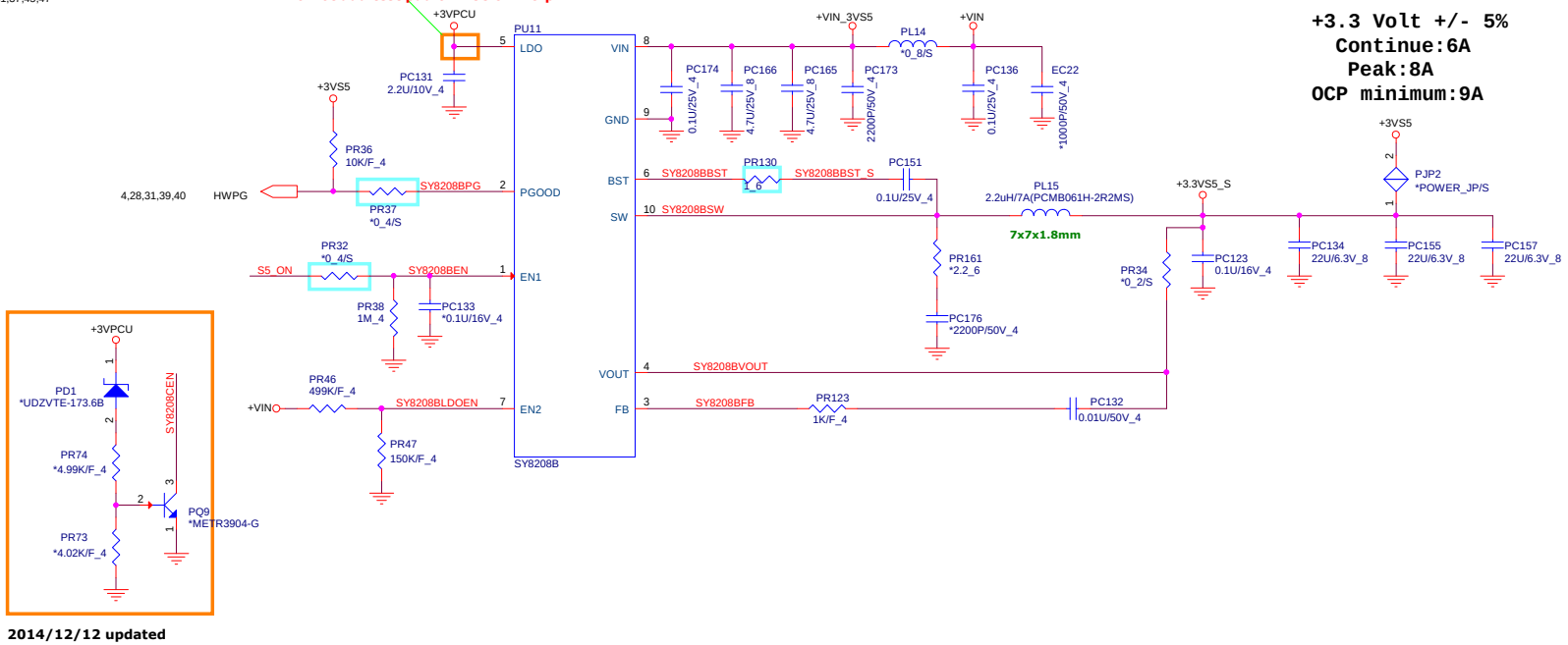
DC/DC +3VS5/+5VS5

+VIN 19,25,31,37,39,40,42,43,44,45,49
+3VS5 4,15,26,27,28,29,30,37,39,40,41,45,46
+5VS5 4,20,23,31,32,33,39,40,41,42,43,44,46
+3VPCU 6,13,23,25,26,28,31,37,45,47
+5VPCU 20,31,46

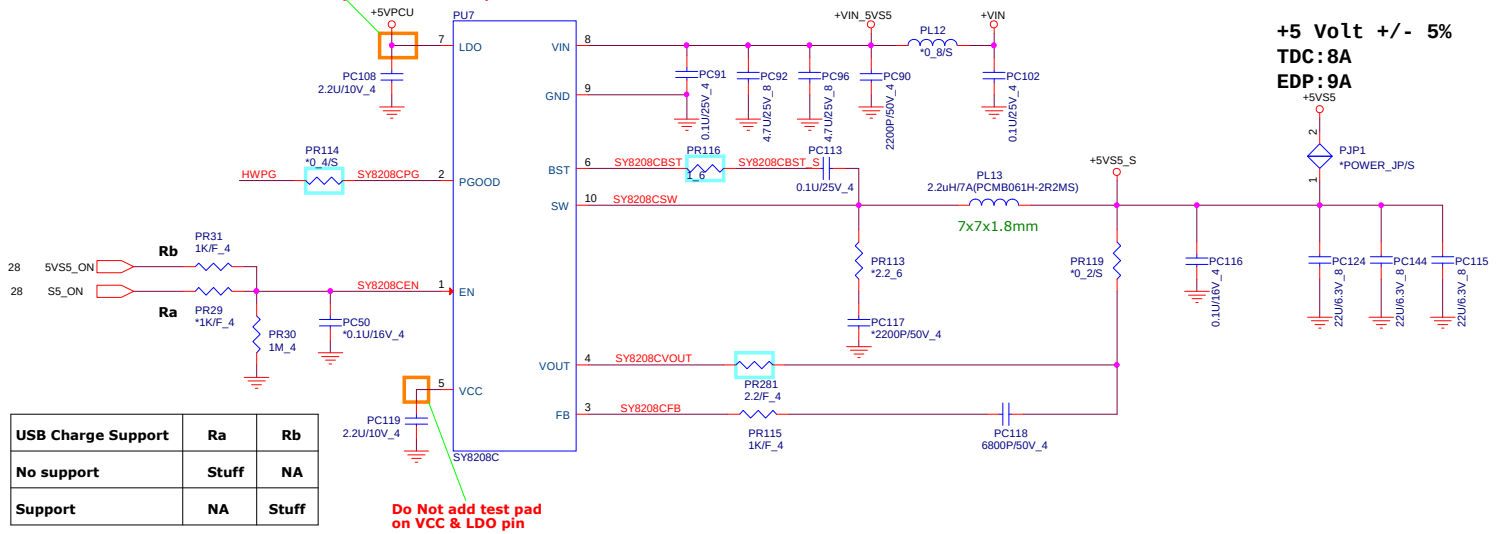
Do Not add test pad on VCC & LDO pin



2014/12/12 updated

+3.3 Volt +/- 5%
Continue:6A
Peak:8A
OCP minimum:9A

Do Not add test pad on VCC & LDO pin



USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
TDC:8A
EDP:9A

NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A

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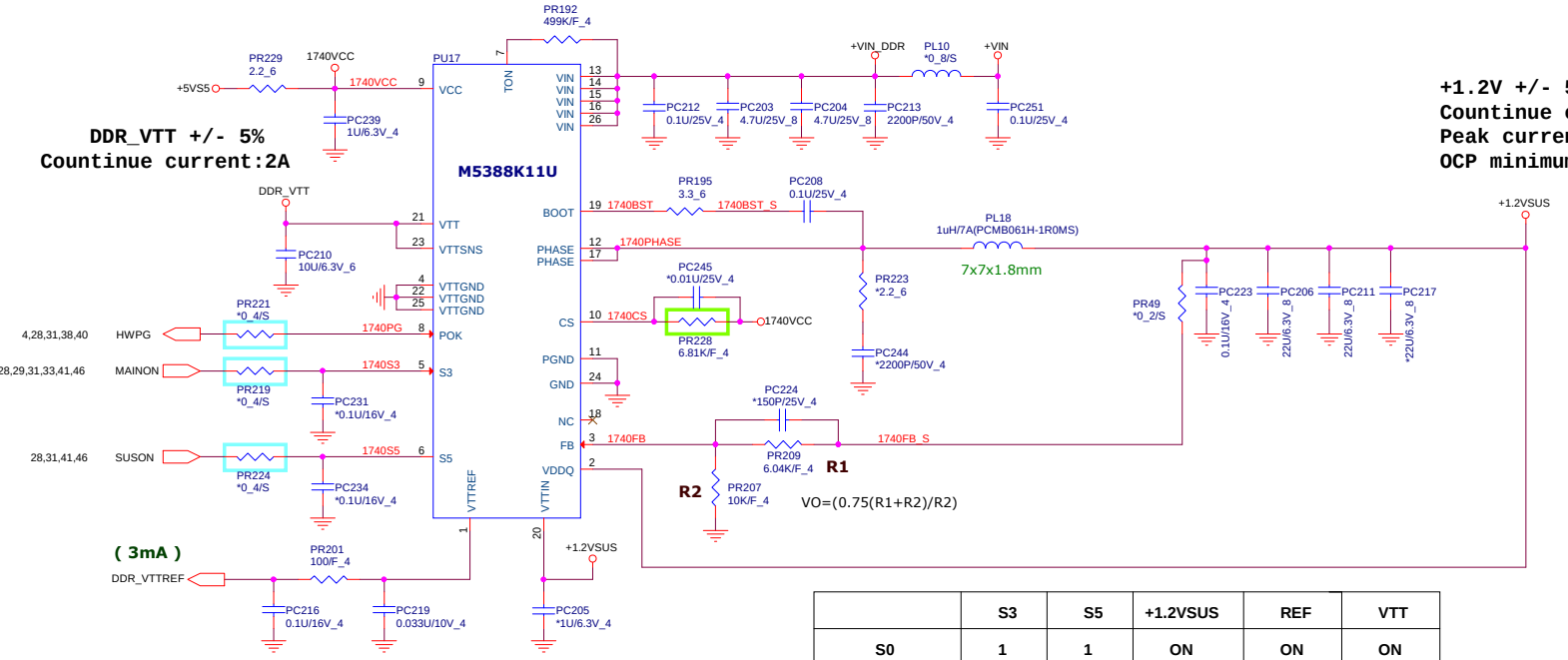
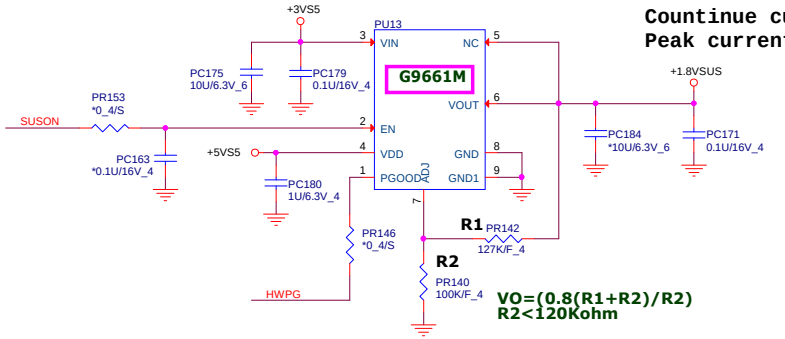
+VIN 19,25,31,37,38,40,42,43,44,45,49
+3VS5 4,15,26,27,28,29,30,37,38,40,41,45,46
+5VS5 4,20,23,31,32,33,38,40,41,42,43,44,46
+1.2VSUS 3,6,16,17,18,41
DDR_VTT 18
+1.8VSUS 16,17,18



	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)/1.8VS5	1A

NB5
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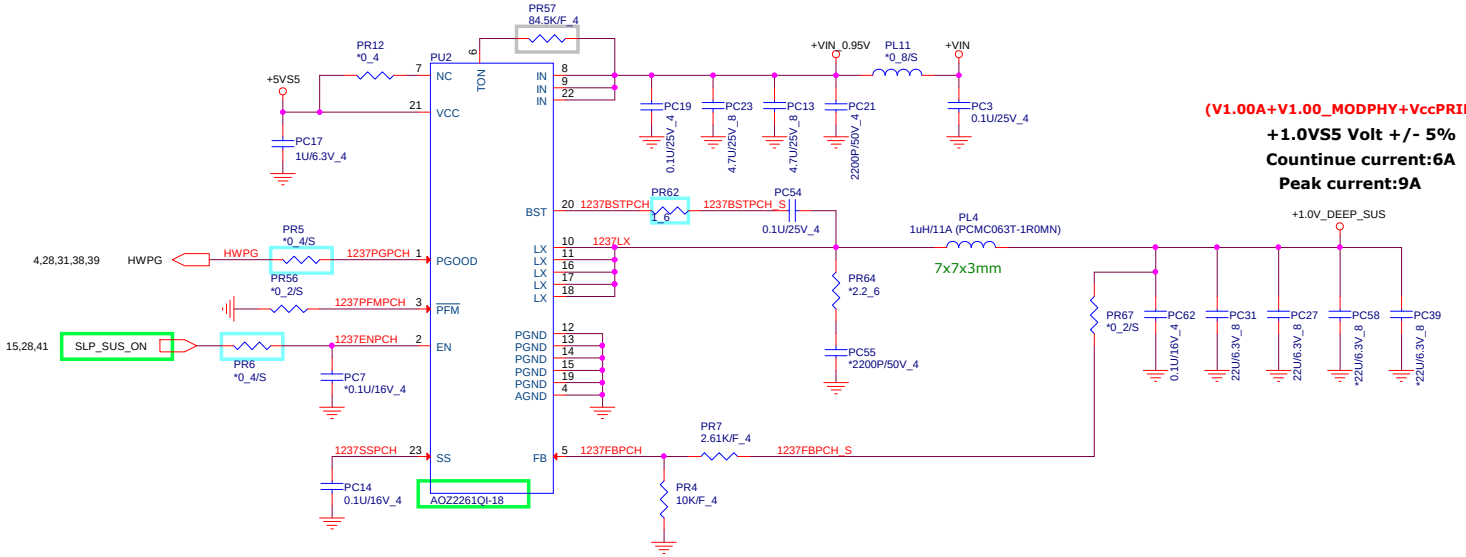
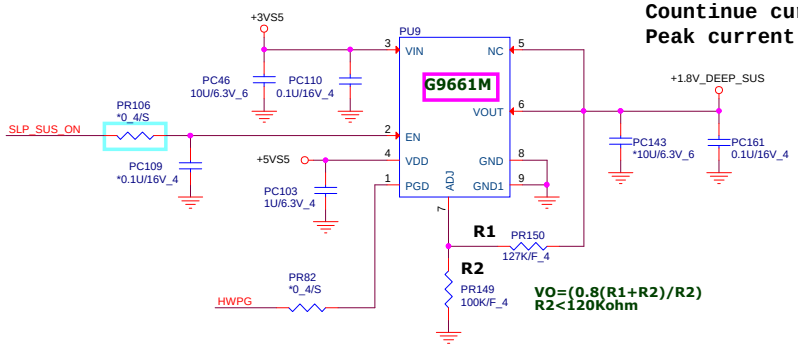
+VIN 19,25,31,37,38,39,42,43,44,45,49
+3VS5 4,15,26,27,28,29,30,37,38,39,41,45,46
+5VS5 4,20,23,31,32,33,38,39,41,42,43,44,46
+1.0V_DEEP_SUS 9,13,15,41
+1.8V_DEEP_SUS 9,15,37,46



(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Countinue current:6A
Peak current:9A

+1.8V_DEEP_SUS +/- 5%
Countinue current:1.0A
Peak current:3A

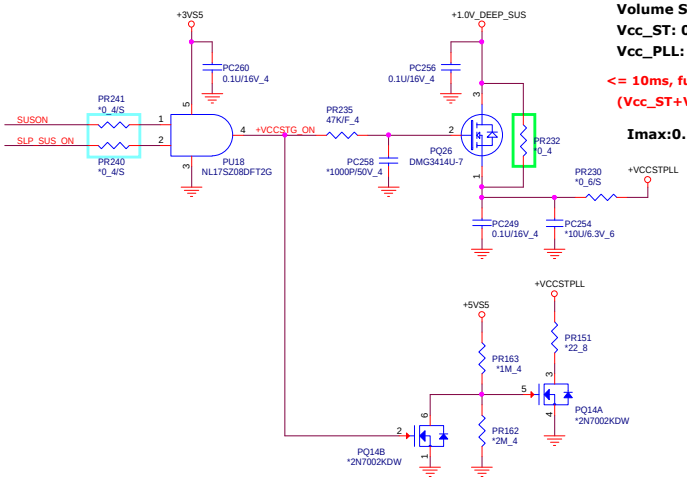


NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Friday, August 05, 2016	Sheet 40 of 49	

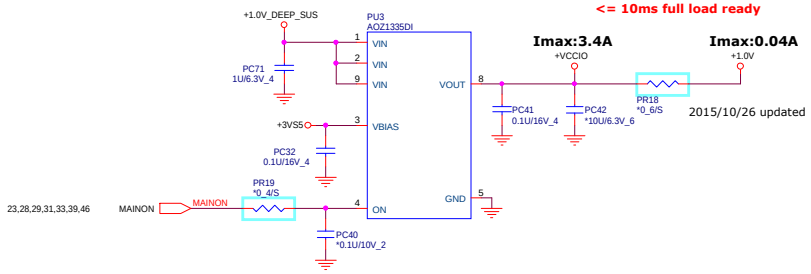
+1.0V 2,4,6,28
+3VS5 4,15,26,27,28,29,30,37,38,39,40,45,46
+5VS5 4,20,23,31,32,33,38,39,40,42,43,44,46
+VCCIO 2,6
+1.2VSUS 3,6,16,17,18,39
+VCCSTPLL 2,5,6,9,42
+1.0V_DEEP_SUS 9,13,15,40
+1.2V_VCCPLL_OC 6



Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Imax:0.24A

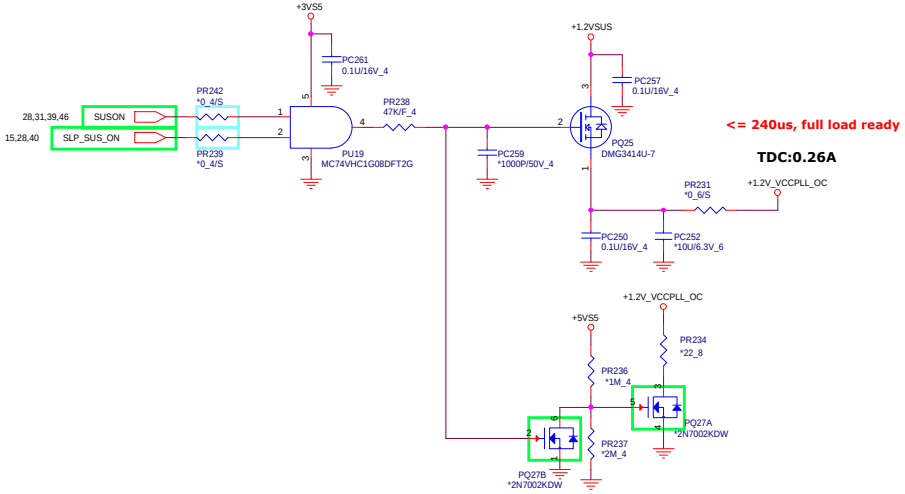


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**

2015/10/26 updated



<= 240us, full load ready

TDC:0.26A

PROJECT : X31
Quanta Computer Inc.

NB5

Size	Document Number	Rev
C	+1.0V/+VCCSTPLL	1A

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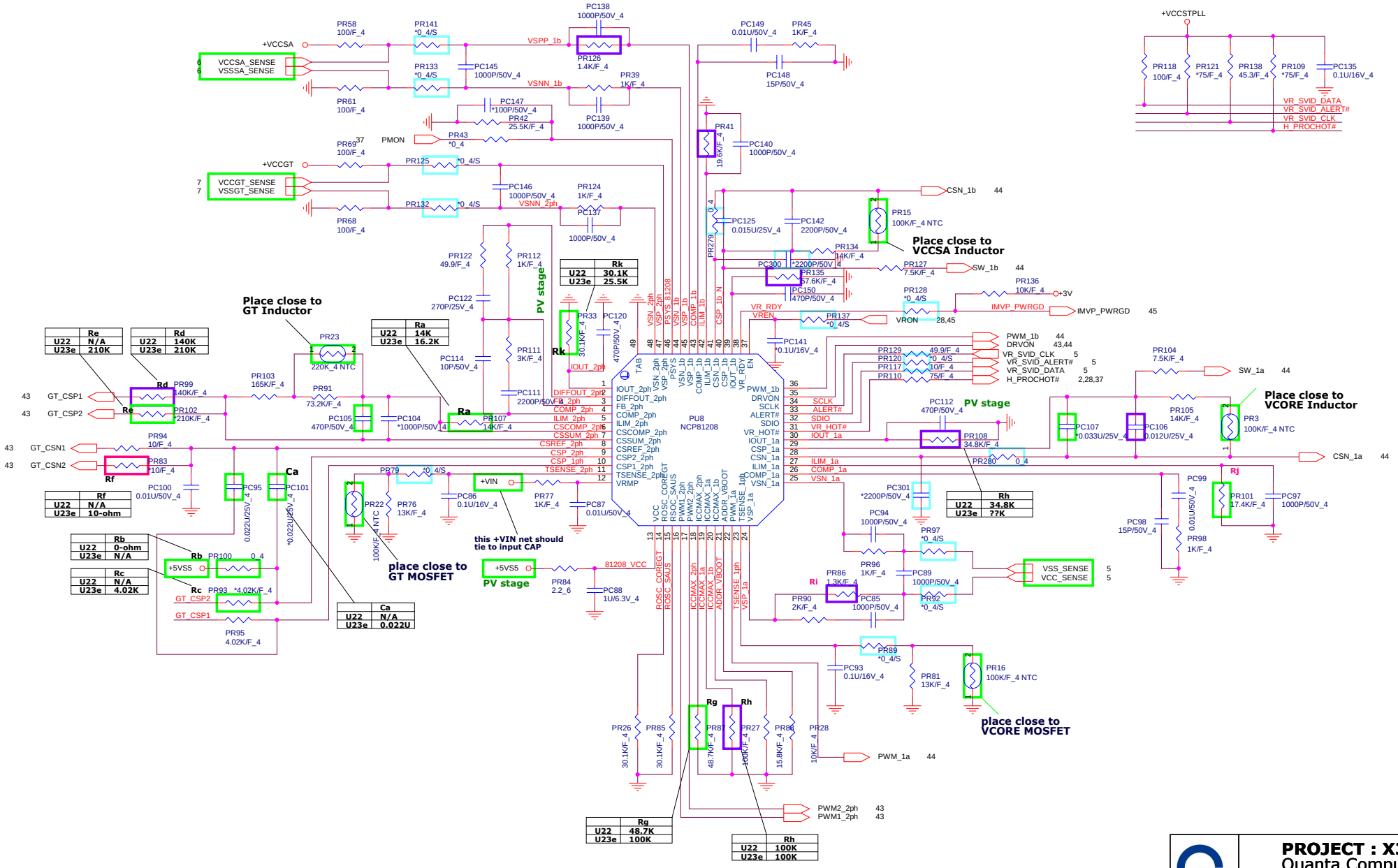
+3V 2,4,10,11,12,13,14,15,19,20,21,22,24,25,27,28,29,33,46
+5V 20,21,22,25,46
+VIN 19,25,31,37,38,39,40,43,44,45,49
+5VPCU 20,31,38,46
+VCCSA 6,44
+VCCGT 7,43
+VCCSTPLL 2,5,6,9,41



Re	
U22	N/A
U23e	210K

Rd	
U22	140K
U23e	210K

Ra	
U22	14K
U23e	16.2K

Rk	
U22	30.1K
U23e	25.5K

Rf	
U22	N/A
U23e	10-ohm

Rb	
U22	0-ohm
U23e	N/A

Rc	
U22	N/A
U23e	4.02K

Ca	
U22	N/A
U23e	0.022U

Rg	
U22	48.7K
U23e	100K

Rh	
U22	100K
U23e	100K

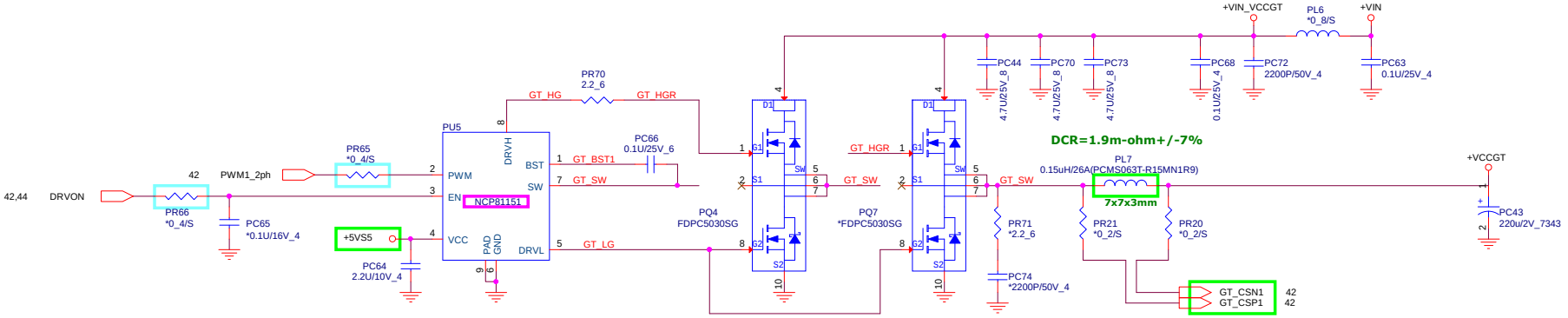
Rh	
U22	34.8K
U23e	??K

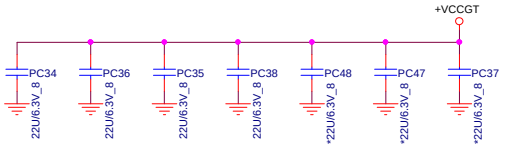
NB5

PROJECT : X31
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VR IC (NCP81206)	2A
Date: Friday, August 05, 2016	Sheet 42 of 49	

+VIN 19,25,31,37,38,39,40,42,44,45,49
+5VS5 4,20,23,31,32,33,38,39,40,41,42,44,46
+VCCGT 7,42





H/W side output CAP list

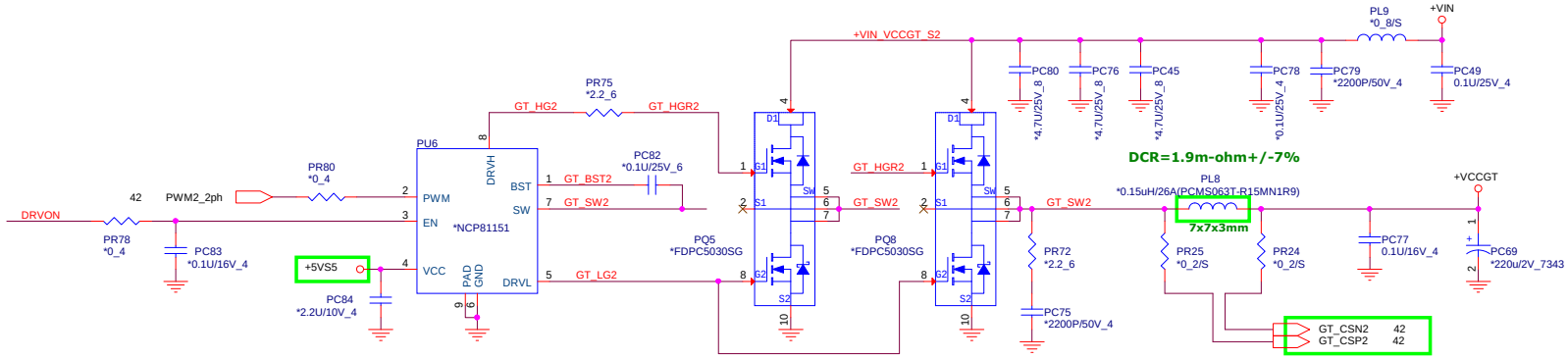
47U/6.3V_0805 X 6
22U/6.3V_0603 X 12 (GTX+5)
10U/6.3V_0402 X 10
1U/6.3V_0402 X 12

+VCC_GT

U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

For U23e --> Add These Components



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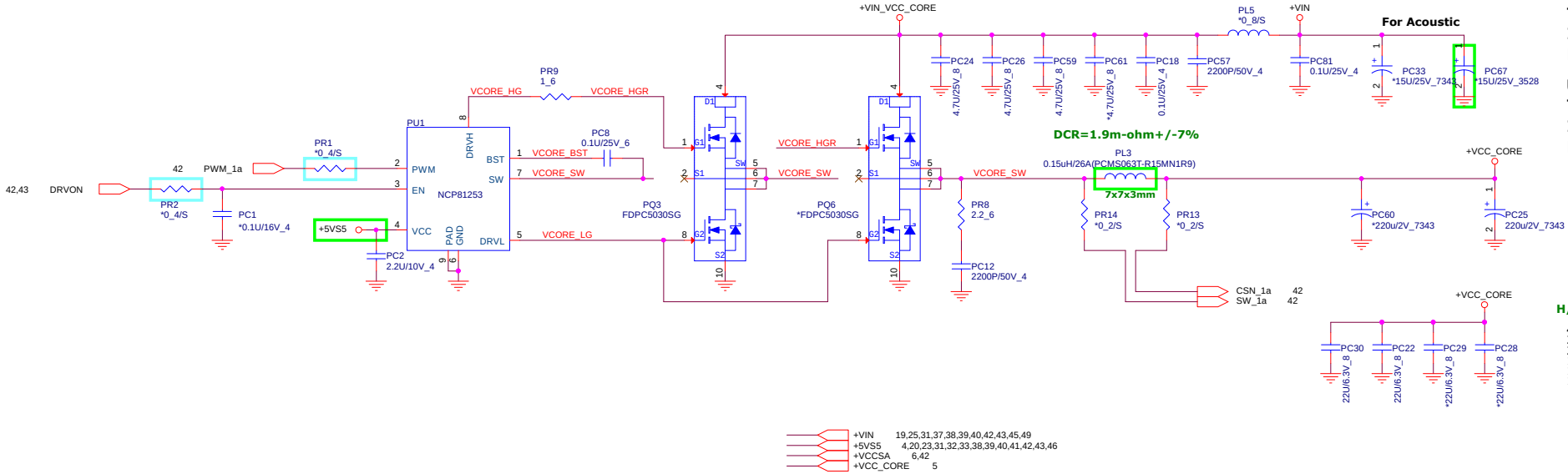
CPU CORE



+VCC_CORE

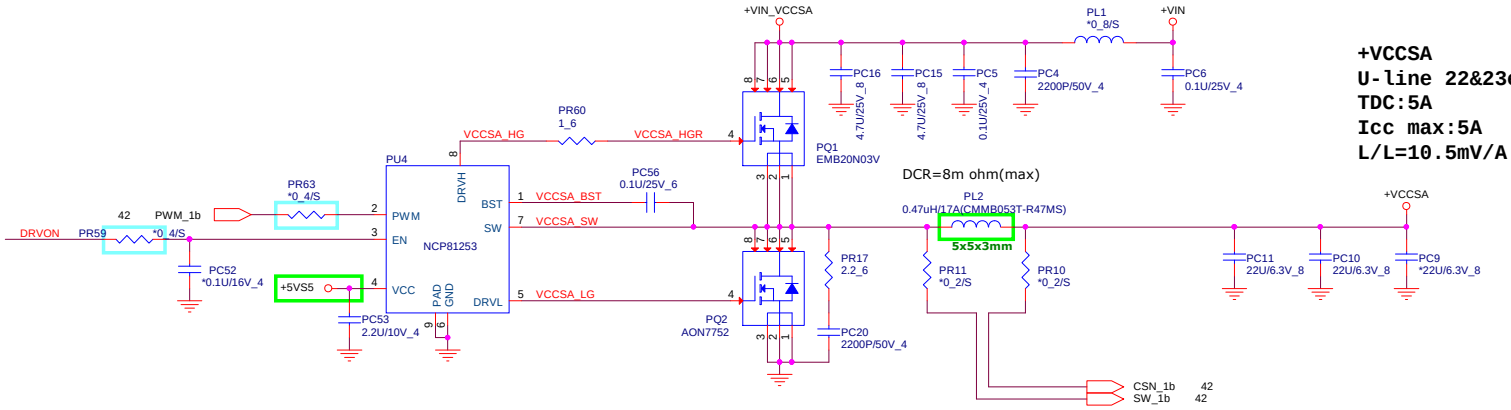
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

H/W side output CAP list

47U/6.3V_0805 X 9
22U/6.3V_0805 X 1
22U/6.3V_0603 X 13
10U/6.3V_0603 X 1
10U/6.3V_0402 X 15
1U/6.3V_0402 X 15

VCCSA



+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

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NB5

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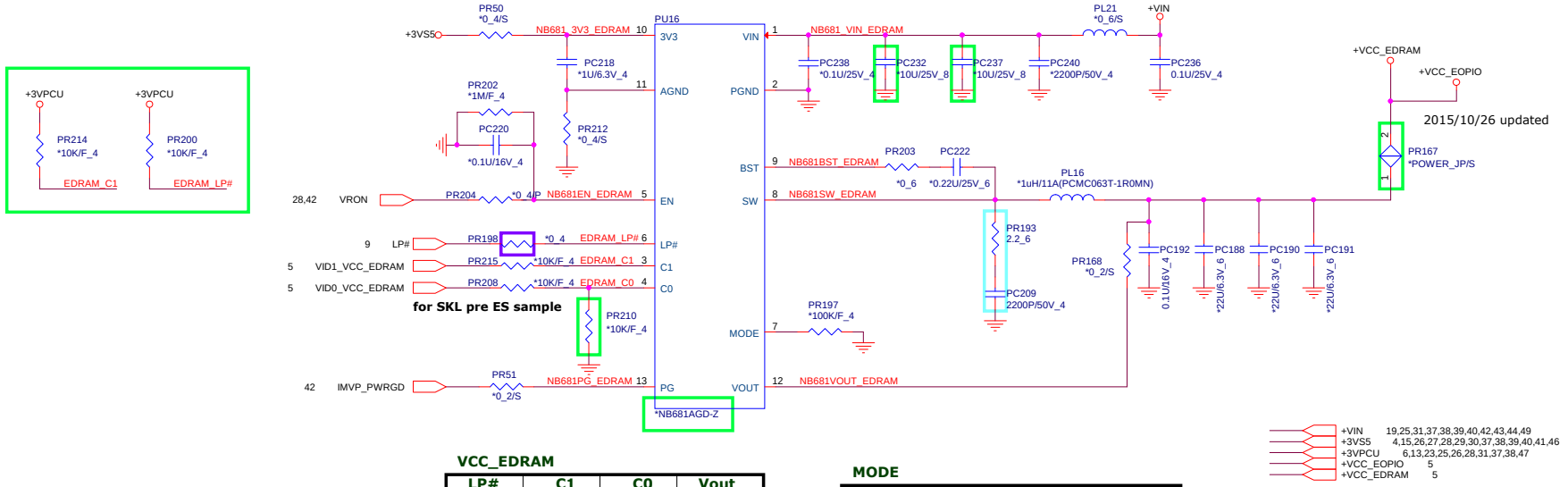
+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A



VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

NB5

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Custom	+VCC_EDRAM (NB681)_23E	
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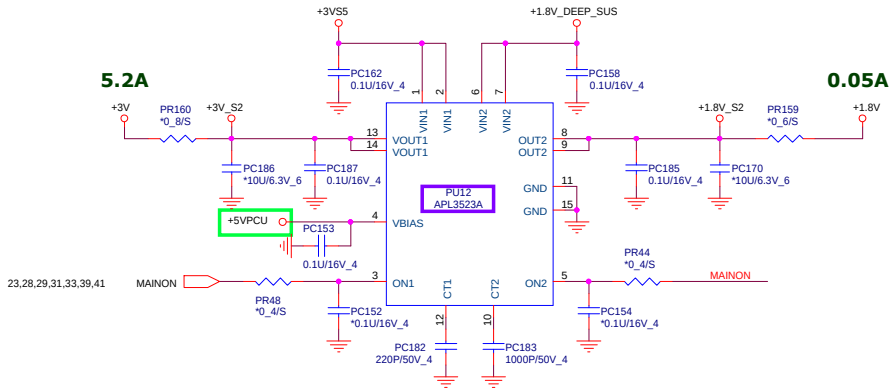
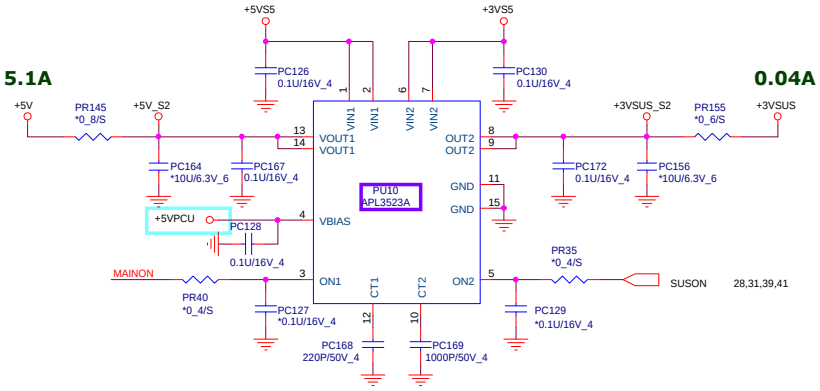
+3V 2,4,10,11,12,13,14,15,19,20,21,22,24,25,27,28,29,33,42
+5V 20,21,22,25
+1.8V 5,20,21
+3VS5 4,15,26,27,28,29,30,37,38,39,40,41,45
+5VS5 4,20,23,31,32,33,38,39,40,41,42,43,44
+3VSUS 25,26
+5VPCU 20,31,38





NB5

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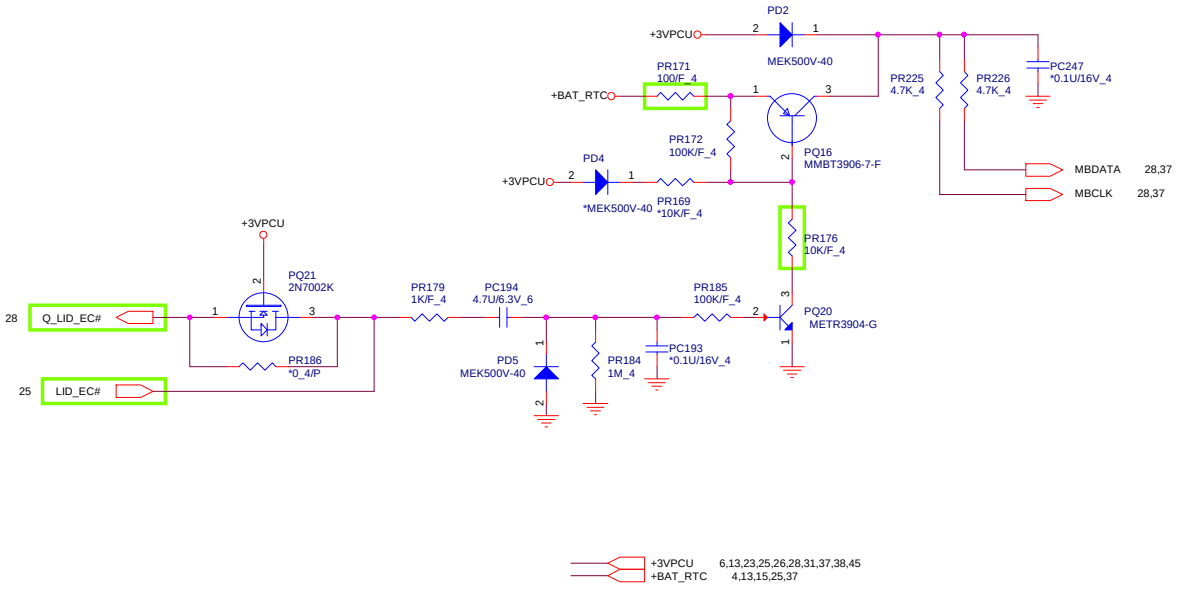

NB5	**PROJECT : X31** Quanta Computer Inc.	
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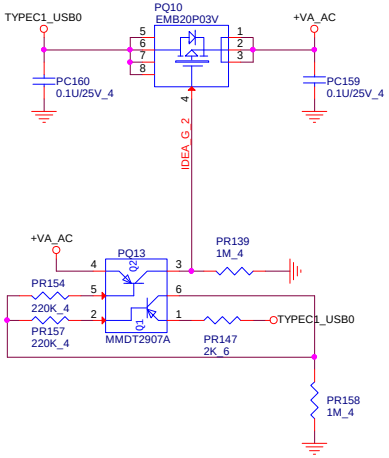
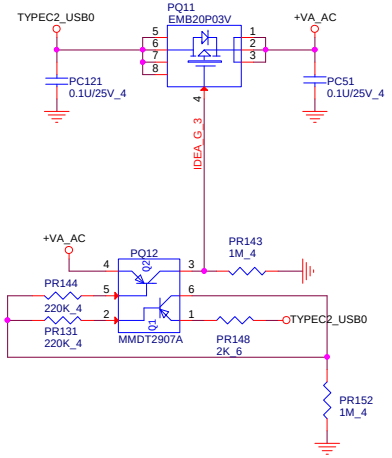
+VA_AC 37
TYPEC1_USB0 31
TYPEC2_USB0 32





NB5

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Custom	TYPE C S/W	1A
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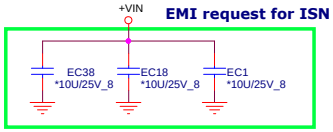

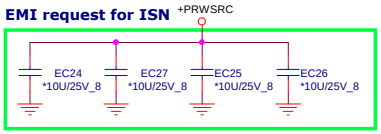

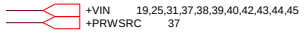

NB5

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Quanta Computer Inc.

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