COMPAL CONFIDENTIAL

MODEL NAME :CAZ30/CAZ40

PCB NO : LA-E112P

BOM P/N : 431A4831L01

Port Map:
Kirkwood Port Map as of 2016-04-01

X8 KBL UMA

Kabylake U

2016-04-20

REV : 0.1 (X00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAA000CM000	PCB 1S3 LA-E112P REV0 MB AR 3

Layout Dell logo

DELL CONFIDENTIAL/PROPRIETARY

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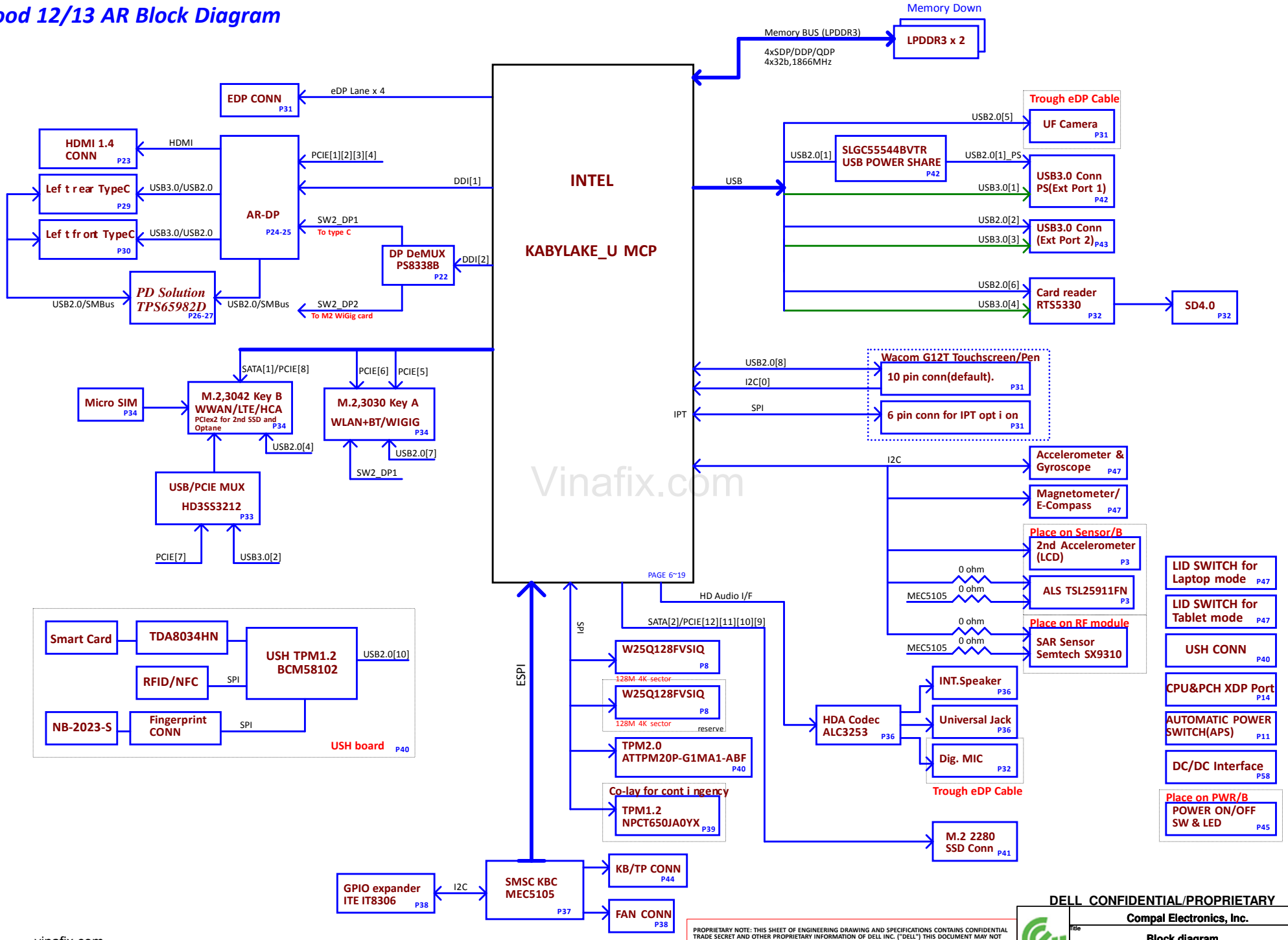
Title: Cover Sheet

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 1 of 58

Kirkwood 12/13 AR Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

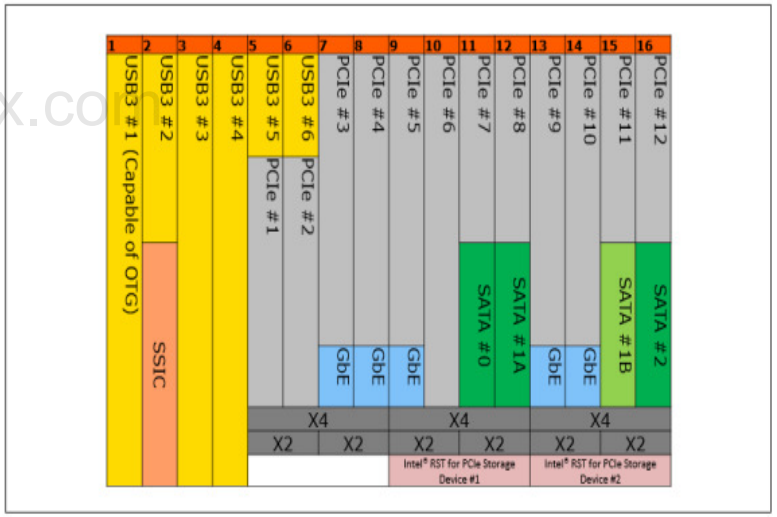
PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

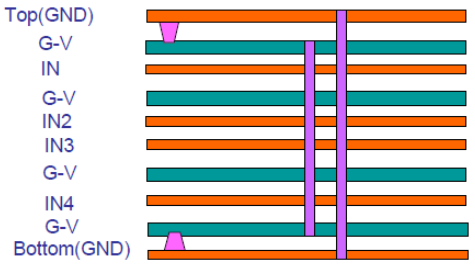
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Lef t
USB3.0-4				SD Card Reader
USB3.0-5		PCIE-1		Alpine Ridge-DP
USB3.0-6		PCIE-2		
		PCIE-3		
		PCIE-4		
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	M.2 3042(SATA Cache or HCA)
		PCIE-8	SATA-1	
		PCIE-9		M.2 2280 SSD (PCIe4 or SATA)
		PCIE-10		
		PCIE-11	SATA-1*	
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Lef t
3	NA
4	M2 3042(WWAN)
5	UF Camera
6	SD Card Reader
7	M.2 3030(BT)
8	Touch Screen
9	NA
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50000
1	Top(GND)		Copper foil + plating	0.33oz+plating	1.40000
		3.8	Prepreg	1080 or 1086	2.80
2	VCC/GND		Copper foil + plating	0.33oz+plating	1.20000
		4.2	Prepreg	1080 or 1086	2.90
3	IN1		Copper foil	0.5 oz	0.65000
		4.1	CORE	3mil	3.00000
4	VCC/GND		Copper foil	0.5 oz	0.65000
		3.6	Prepreg	1080	3.00
5	IN2		Copper foil	1.0 oz	1.35000
		3.6	CORE	5mil	5.00000
6	IN3		Copper foil	1.0 oz	1.35000
		3.6	Prepreg	1080	3.00
7	VCC/GND		Copper foil	0.5 oz	0.65000
		4.1	CORE	3mil	3.00000
8	IN4		Copper foil	0.5 oz	0.65000
		4.2	Prepreg	1080 or 1086	2.90
9	VCC/GND		Copper foil + plating	0.33oz+plating	1.20000
		3.8	Prepreg	1080 or 1086	2.80
10	Bottom(GND)		Copper foil + plating	0.33oz+plating	1.40000
			SolderMask		
Overall Thickness (1.0mm ± 10%)			39.37		39.40000
					1.00076



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Title: Port assignment

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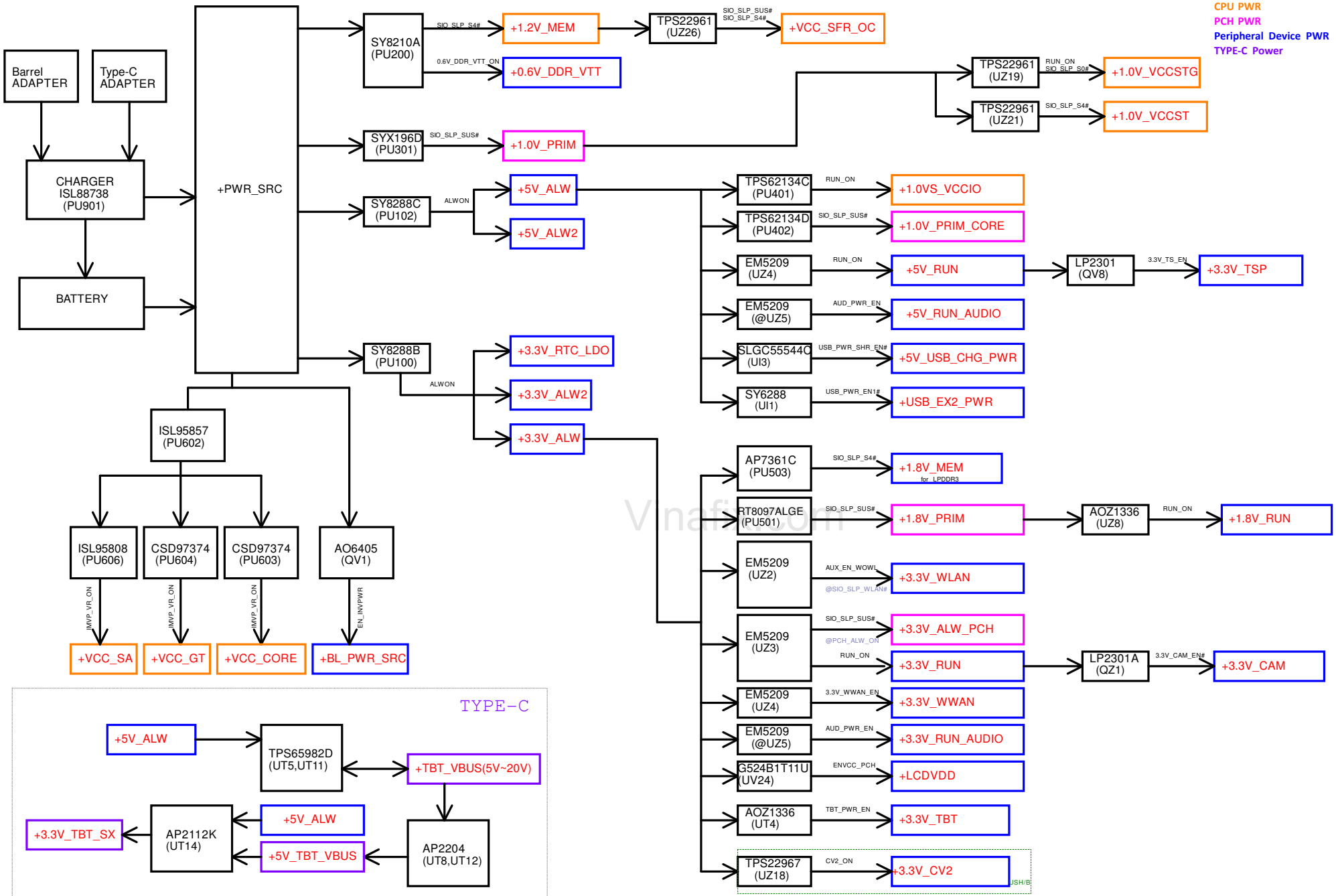
Date: Friday, April 22, 2016 | Sheet 3 of 58



Compal Electronics, Inc.

Title: Power rails

Size | Document Number: LA-XXXXP | Rev: 0.1

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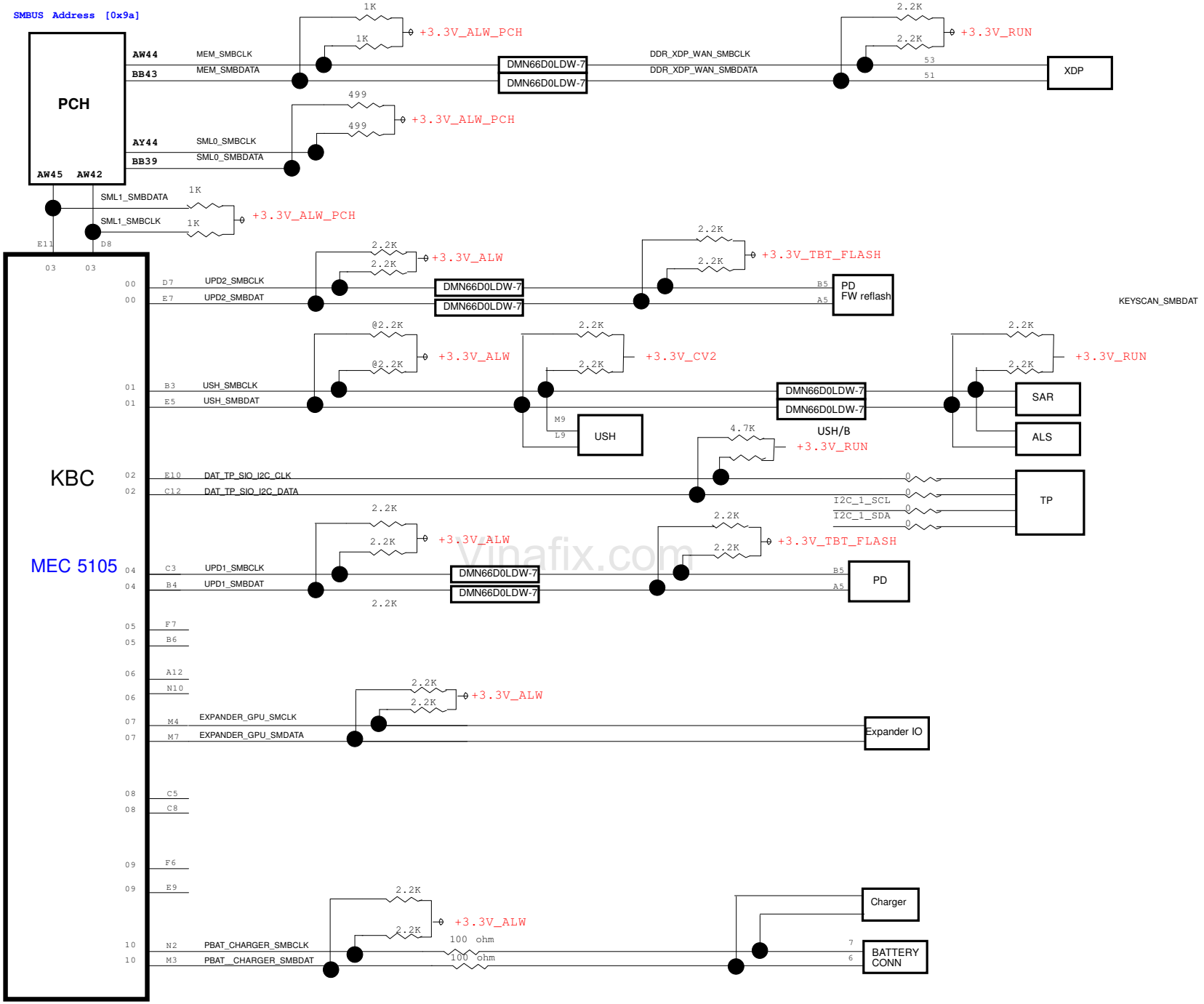

Compal Electronics, Inc.

Title: Port assignment

Size | Document Number: LA-E112P | Rev: 0.1

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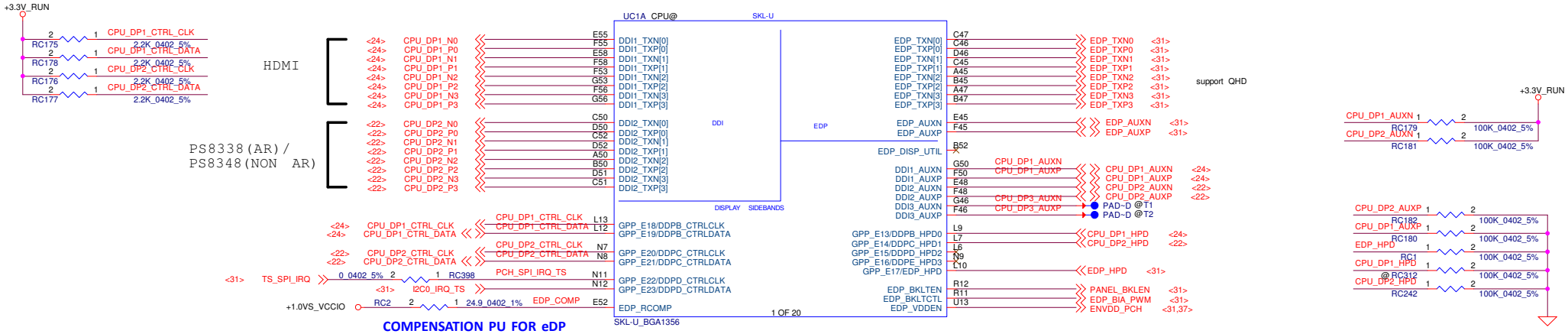

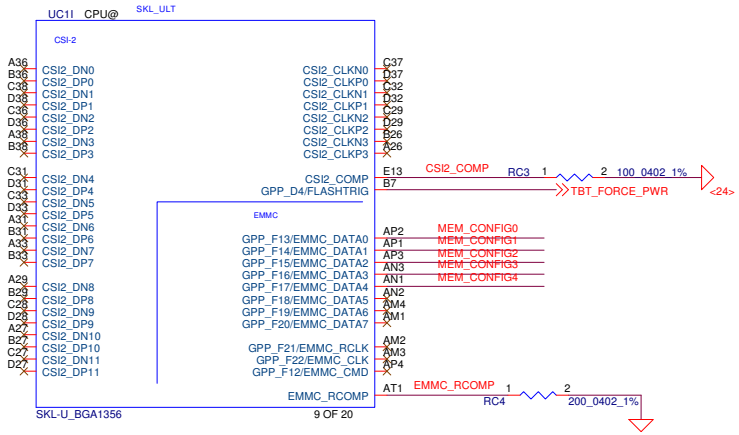

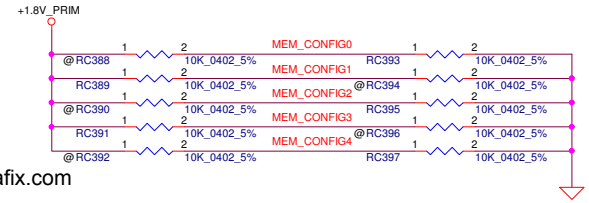

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GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1600 Mbps	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1		0	0	1	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2		0	0	0	0	1	1	1	1	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	0	0

GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1866 Mbps	1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2		0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4		0	0	0	0	0	0	0	1	1

GPIO PIN	PIN NAME	SPEED	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	2133 Mbps (UI)	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4		1	1	1	1	1	1	1	1	1

Compal Electronics, Inc.

Title: CPU (1/14)

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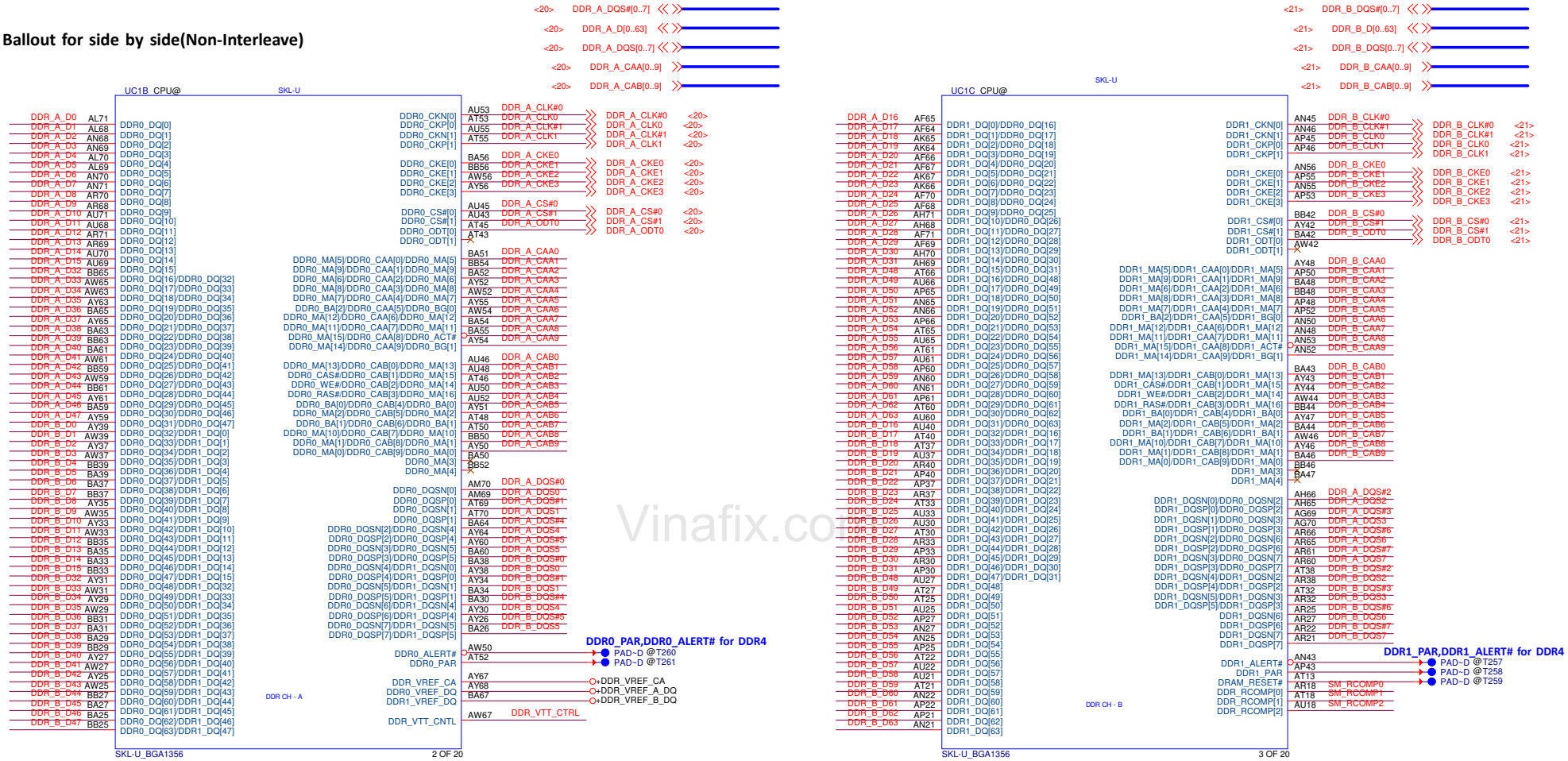
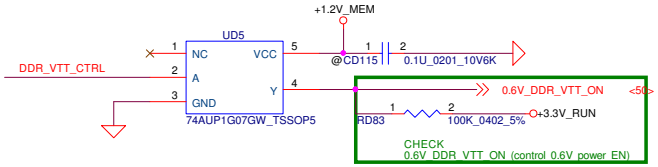
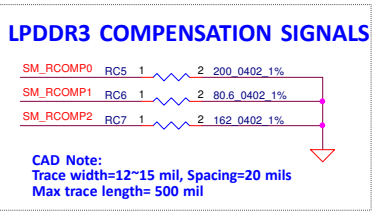
For LPDDR3

LPDDR3, Ballout for side by side(Non-Interleave)







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Title: CPU (2/14)

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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For Kirkwood

UC1E CPU@ SKL-U

SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C LINK
CL_CLK
CL_DATA
CL_RST#

SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#
GPP_A0/RCIN#
GPP_A6/SERIRQ

SKL-U_BGA1356
5 OF 20

+3.3V_1.8V_ESPI?
LPC – 3.3V
ESPI – 1.8V

CHECK LPC_CLK_FOR_DEBUG_CARD?

Reserve

SOFTWARE TAA

RF Request
Place close CPU side

+1.8V?

TLS CONFIDENTIALITY
HIGH ENABLE
LOW(DEFAULT) DISABLE
WEAK INTERNAL 20K PD

EC interface
HIGH ESPI
LOW(DEFAULT) LPC
WEAK INTERNAL 20K PD

EXI BOOT STALL BYPASS
HIGH ENABLED
LOW(DEFAULT) DIABLED
WEAK INTERNAL PD

128Mb Flash ROM
UC5
@UC6
W25Q128FVSIQ_SO8

ACES_50696-0200M-P01
JSPI1
CONN@

	ESPI	LPC
RC39	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RC33,RC34,RC35,RC36,RC38,RC40	33 ohm	25 ohm

Need check

Compal Electronics, Inc.
Title: CPU (3/14)
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Date: Monday, April 25, 2016
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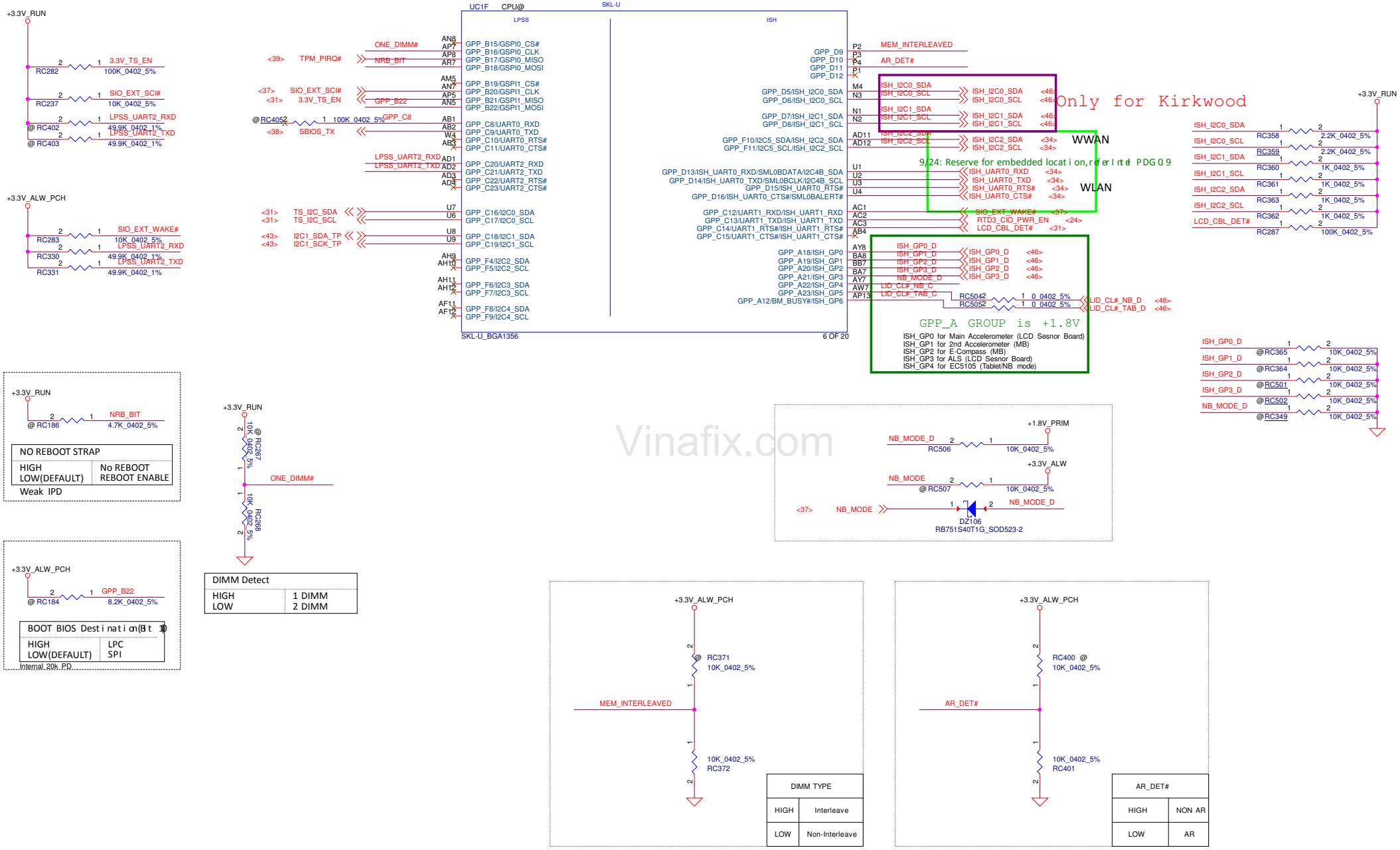

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Title: CPU (4/14)

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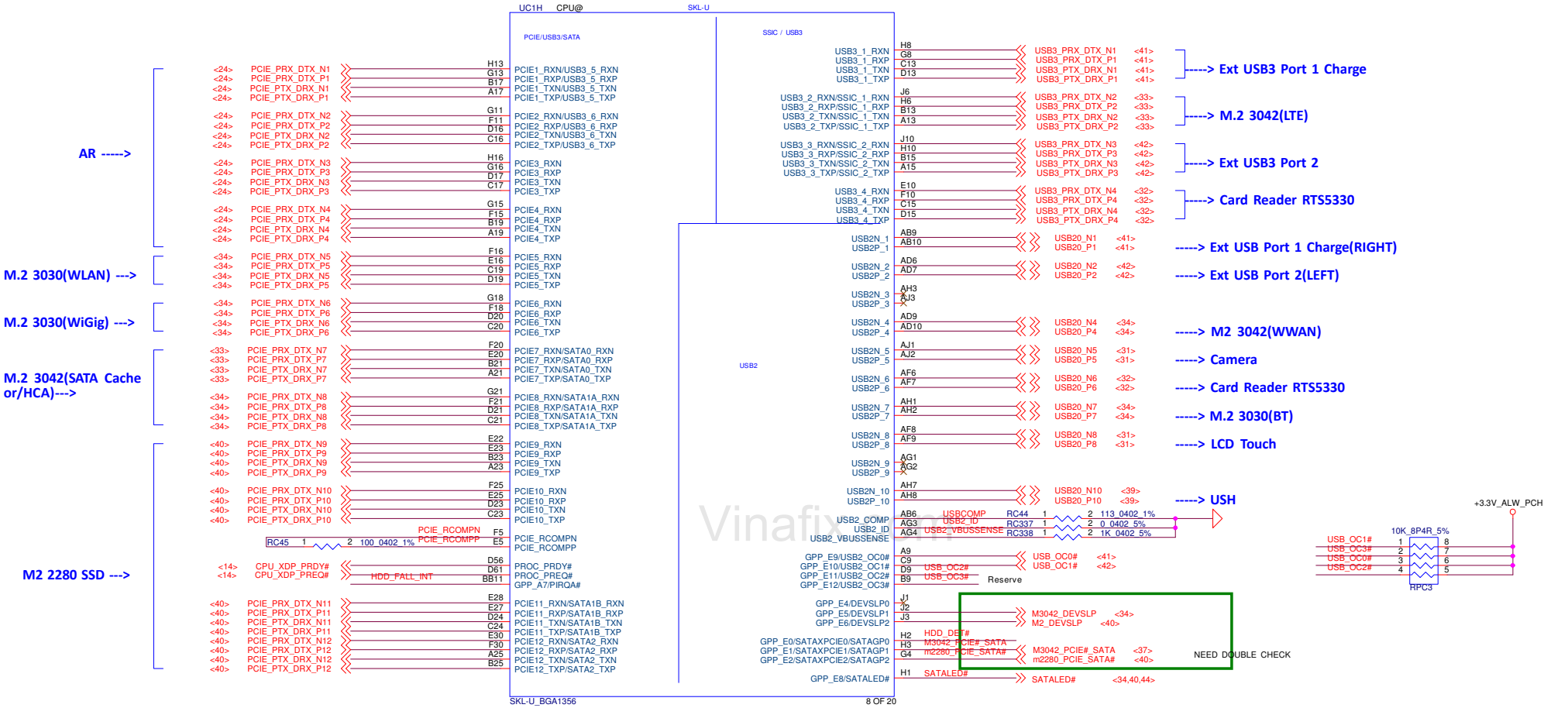
For AR, Kirkwood



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Compal Electronics, Inc.

Title: CPU (5/14)

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For UMA CONFIG

WWAN---> CLK_PCIE_N0 / CLK_PCIE_P0 / CLKREQ_PCIE#0 — RF@RC373 0_0402_5% — RC189 10K_0402_5% — +3.3V_RUN

WLAN---> CLK_PCIE_N1 / CLK_PCIE_P1 / CLKREQ_PCIE#1 — RF@RC374 0_0402_5% — RC47 10K_0402_5% — +3.3V_RUN

WIGIG---> CLK_PCIE_N2 / CLK_PCIE_P2 / CLKREQ_PCIE#2 — RF@RC375 0_0402_5% — RC50 10K_0402_5% — +3.3V_RUN

M.2 SDD---> CLK_PCIE_N3 / CLK_PCIE_P3 / CLKREQ_PCIE#3 — RF@RC376 0_0402_5% — RC59 10K_0402_5% — +3.3V_RUN

LAN--->

AR ---> CLK_PCIE_N5 / CLK_PCIE_P5 / CLKREQ_PCIE#5 — RF@RC378 0_0402_5% — RC190 10K_0402_5% — +3.3V_RUN

UC1J CPU@ SKL_ULT

CLOCK SIGNALS

D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#

B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
AT7 GPP_B6/SRCCLKREQ1#

D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
AT8 GPP_B7/SRCCLKREQ2#

D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#

B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#

E40 CLKOUT_PCIE_N5
E38 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#

SKL-U_BGA1356 10 OF 20

CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RTCX1
RTCX2
SRTCRST#
RTCRST#

F43 CLK_ITPXDP_N — @RC297 0_0402_5% — CLK_ITPXDP_N_R <14>
E43 CLK_ITPXDP_P — @RC298 0_0402_5% — CLK_ITPXDP_P_R <14>

BA17 SUSCLK — SUSCLK <34,40>

E37 XTAL24_IN
E35 XTAL24_OUT

XTAL24_IN — RC46 1M_0402_1% — XTAL24_OUT
YC1 24MHZ_12PF_X3G024000DC1H
CC21 15P_0402_50V8J
CC22 15P_0402_50V8J
RC295 0_0402_5% XTAL24_OUT_R
For Skylake,YC1 24 MHz (50 Ohm ESR) For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

E42 XCLK_BIASREF

AM18 PCH_RTCX1
AM20 PCH_RTCX2

RC52 2.7K_0402_1% — +1.0V_CLK5
@RC324 59_0402_1%
For Skylake, pop RC52,depop RC324
For Cannonlake, pop RC324,depop RC52
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

PCH_RTCX1 — RC54 10M_0402_5% — PCH_RTCX2
YC2 32.768KHZ_12.5PF_9H03200042 ESR MAX=50k ohm
CC23 15P_0402_50V8J
CC26 12P_0402_50V8J
RC296 0_0402_5% PCH_RTCX2_R

AN18 SRTCRST#
AM16 RTCRST#

RC56 20K_0402_5% — +RTC_CELL
CC24 1U_0402_6.3V6K
PCH_RTCRST# <37>
PCH_RTCRST# — RC57 20K_0402_5%
CC25 1U_0402_6.3V6K

SHORT PADS~D
@CMOS1

CMOS1 must take care short & touch risk on layout placement

PCH_PLTRST# — RC244 0_0402_5% — PCH_PLTRST#_EC <38>

+3.3V_ALW_PCH
UC7 TC7SH08FU_SSOP5~D
PCH_PLTRST#_AND — @RC65 100K_0402_5%
PCH_PLTRST#_AND <24,31,34,39,40>

PCH_PLTRST# — @RC60 0_0402_5% — PLTRST_TPM# <39>
PCH_PLTRST#_AND — RC325 0_0402_5%

8/21 can change to 10K for merge to RP
+3.3V_ALW_DSW
PCH_BATLOW# — RC72 8.2K_0402_5%
AC_PRESENT — RC243 10K_0402_5%

+3.3V_ALW_DSW — RC323 LAN_WAKE# 10K_0402_5%
RC67 PCH_PCIE_WAKE# 1K_0402_5%

+1.0V_VCCST — RC71 VCCST_PWRGD 1K_0402_5%

+3.3V_ALW_PCH — @RC74 ME_SUS_PWR_ACK 10K_0402_5%
10/6 depop, prevent singal step.
@RC411 PCH_PWROK 10K_0402_5%

+RTC_CELL
INTRUDER# — RC69 1M_0402_5%

+3.3V_ALW_PCH
MPHYP_PWR_EN — @RC387 100K_0402_5%
VRALERT# — @RC73 10K_0402_5%
@RC344 10K_0402_5%

+3.3V_ALW
SIO_SLP_LAN# — @RC68 10K_0402_5%
SUSCLK — @RC48 1K_0402_5%

UC1K CPU@ SKL-U

SYSTEM POWER MANAGEMENT

PCH_PLTRST# — AN10 GPP_B13/PLTRST#
SYS_RESET# — B5 SYS_RESET#
PCH_RSMRST#_AND — AY17 RSMRST#
<14,43> PCH_RSMRST#_AND
H_CPUPWRGD_R — @RC77 2K_0402_5%
T9 @ PAD~D — RC78 60.4_0402_1%
<14,37,38> VCCST_PWRGD
H_CPUPWRGD — A68 PROCPWRGD
VCCST_PWRGD_CPU — B65 VCCST_PWRGD
B6
<14,37> SYS_PWROK — BA20 SYS_PWROK
<54> PCH_PWROK — BB20 PCH_PWROK
<38> PCH_DPWROK DSW_PWROK
<37> ME_SUS_PWR_ACK — AR13 GPP_A13/SUSWARN#/SUSPWRDNACK
<37> SUSACK# — AP11 GPP_A15/SUSACK#
<37,38> PCH_PCIE_WAKE# — BB15 WAKE#
<37> LAN_WAKE# — AM15 GPD2/LAN_WAKE#
AW17 GPD1/LANPHYPC
<31> 3.3V_CAM_EN# — AT15 GPD7/RSVD
RC311 10K_0402_5%

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GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

AT11 SIO_SLP_S0# — SIO_SLP_S0# <17,52>
AP15 — SIO_SLP_S3# <24,37,38>
BA16 — SIO_SLP_S4# <17,37,50,53>
AY16 — SIO_SLP_S5# <37>
AN15 SIO_SLP_SUS# <17,37,45,51,52,53>
AW15 SIO_SLP_LAN# <37>
BB17 SIO_SLP_WLAN# <37,45>
AN16 SIO_SLP_A# <37>
BA15 SIO_PWRBTN# <14,37>
AY15 AC_PRESENT <37>
AU13 PCH_BATLOW#
AU11 PME#
AP16 INTRUDER# — PAD~D @T115
AM10 MPHYP_PWR_EN
AM11 VRALERT#

connect to VCCMPHYGTAON_1P0 enable pin

JAPS1
+3.3V_ALW_PCH — SIO_SLP_S3#
+3.3V_ALW — SIO_SLP_S5#
SIO_SLP_S4#
SIO_SLP_A#
+3.3V_ALW
PCH_RTCRST#
<38,44> POWER_SW#_MB
SYS_RESET#
SIO_SLP_S0#
GND GND
CVILU_CF4218FH0R0-05-NH
CONN@

H_CPUPWRGD — ESD@ CC300 100P_0402_50V8J
VCCST_PWRGD — ESD@ CC301 100P_0402_50V8J
ESD Request:place near CPU side

SYS_RESET# — @ESD@ CC302 0.1U_0402_25V6
ESD Request:place near CPU side

RC215
POP NO Support Deep sleep
DE-POP Support Deep sleep

PCH_DPWROK — @RC215 0_0402_5% — PCH_RSMRST#_AND
@CC266 0.01UF_0402_25V7K
RC220 100K_0402_1%
RC75 10K_0402_5%

<14> XDP_DBRESET# — XDP_DBRESET#
+3.3V_RUN — RC290 0_0402_5%
+3.3V_RUN — @RC291 10K_0402_5%
@RC225 8.2K_0402_5%
@RC227 8.2K_0402_5%
ME_RESET#
@UC12 74AHC1G09GW_TSSOP5
SYS_RESET#_R — RC224 1K_0402_5% — SYS_RESET#

if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

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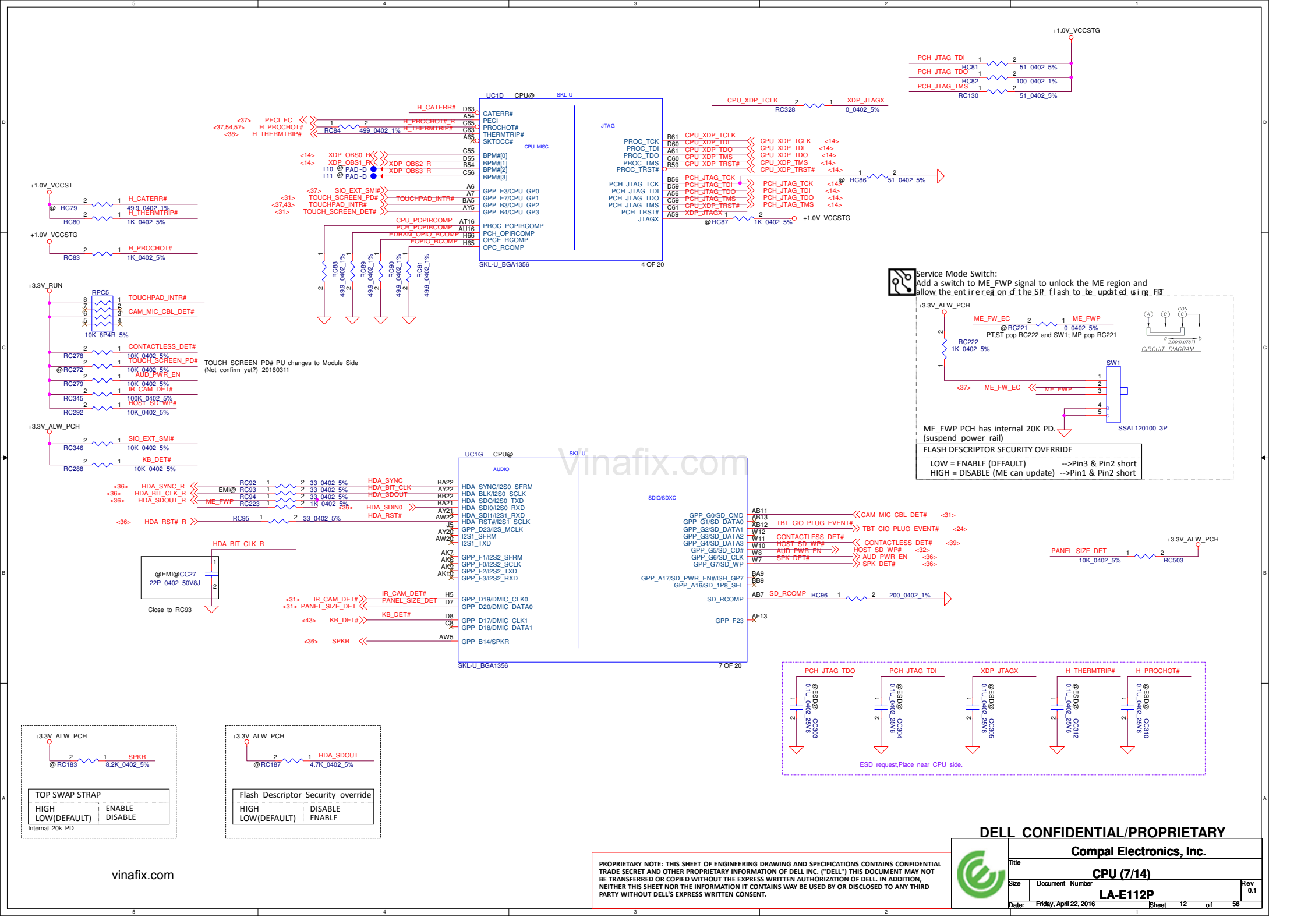
Compal Electronics, Inc.

Title: CPU (6/14)

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 11 of 58


+1.0V_VCCSTG
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
RC81 51_0402_5%
RC82 100_0402_1%
RC130 51_0402_5%
UC1D CPU@ SKL-U
CPU_XDP_TCLK
RC328 0_0402_5%
XDP_JTAGX
JTAG
CPU MISC
H_CATERR#
PECI_EC
H_PROCHOT#
H_THERMTRIP#
RC84 499_0402_1%
XDP_OBS0_R
XDP_OBS1_R
XDP_OBS2_R
XDP_OBS3_R
SIO_EXT_SMI#
TOUCHPAD_INTR#
TOUCH_SCREEN_PD#
TOUCH_SCREEN_DET#
CPU_POPIRCOMP
PCH_POPIRCOMP
EDRAM_OPIO_RCOMP
EOPIO_RCOMP
RC88 RC89 RC90 RC91 499_0402_1%
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST#
PCH_JTAG_TCK
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_TRST#
JTAGX
RC86 51_0402_5%
RC87 1K_0402_5%
CPU_XDP_TCLK
CPU_XDP_TDI
CPU_XDP_TDO
CPU_XDP_TMS
CPU_XDP_TRST#
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
SKL-U_BGA1356
4 OF 20
+1.0V_VCCST
RC79 49.9_0402_1%
RC80 1K_0402_5%
RC83 1K_0402_5%
+3.3V_RUN
RPC5 10K_8P4R_5%
RC278 RC272 RC279 RC345 RC292 10K_0402_5%
AUD_PWR_EN
+3.3V_ALW_PCH
RC346 RC288 10K_0402_5%
TOUCH_SCREEN_PD# PU changes to Module Side
(Not confirm yet?) 20160311
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT
ME_FW_EC
ME_FWP
RC221 0_0402_5%
PT,ST pop RC222 and SW1; MP pop RC221
RC222 1K_0402_5%
SW1
SSAL120100_3P
CIRCUIT DIAGRAM
ME_FWP PCH has internal 20K PD.
(suspend power rail)
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = ENABLE (DEFAULT) -->Pin3 & Pin2 short
HIGH = DISABLE (ME can update) -->Pin1 & Pin2 short
UC1G CPU@ SKL-U
AUDIO
HDA_SYNC
HDA_BIT_CLK
HDA_SDOUT
HDA_SDIN0
HDA_RST#
RC92 RC93 RC94 RC223 33_0402_5%
RC95 33_0402_5%
HDA_BIT_CLK_R
@EMI@CC27 22P_0402_50V8J
Close to RC93
IR_CAM_DET#
PANEL_SIZE_DET
KB_DET#
SPKR
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1
GPP_B14/SPKR
SKL-U_BGA1356
7 OF 20
SDIO/SDXC
GPP_G0/SD_CMD
GPP_G1/SD_DATA0
GPP_G2/SD_DATA1
GPP_G3/SD_DATA2
GPP_G4/SD_DATA3
GPP_G5/SD_CD#
GPP_G6/SD_CLK
GPP_G7/SD_WP
GPP_A17/SD_PWR_EN#/ISH_GP7
GPP_A16/SD_1P8_SEL
SD_RCOMP
GPP_F23
CAM_MIC_CBL_DET#
TBT_CIO_PLUG_EVENT#
CONTACTLESS_DET#
HOST_SD_WP#
AUD_PWR_EN
SPK_DET#
RC96 200_0402_1%
PANEL_SIZE_DET
RC503 10K_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TDI
XDP_JTAGX
H_THERMTRIP#
H_PROCHOT#
@ESD@ CC303 CC304 CC305 CC312 CC310 0.1U_0402_25V6
ESD request,Place near CPU side.
+3.3V_ALW_PCH
@RC183 SPKR 8.2K_0402_5%
TOP SWAP STRAP
HIGH ENABLE
LOW(DEFAULT) DISABLE
Internal 20k PD
@RC187 HDA_SDOUT 4.7K_0402_5%
Flash Descriptor Security override
HIGH DISABLE
LOW(DEFAULT) ENABLE
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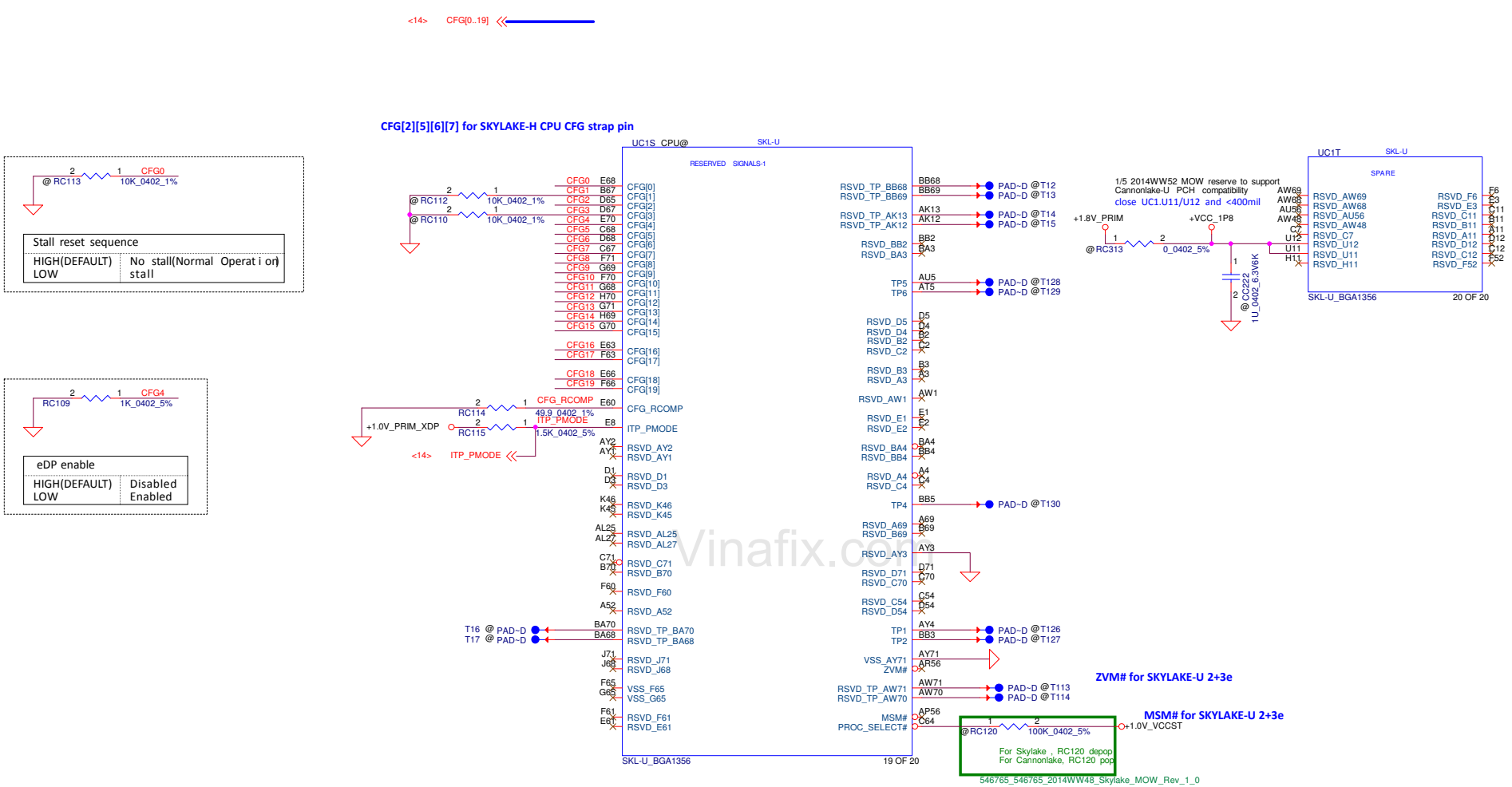
Compal Electronics, Inc.
Title CPU (7/14)
Size Document Number LA-E112P
Rev 0.1
Date: Friday, April 22, 2016 Sheet 12 of 58

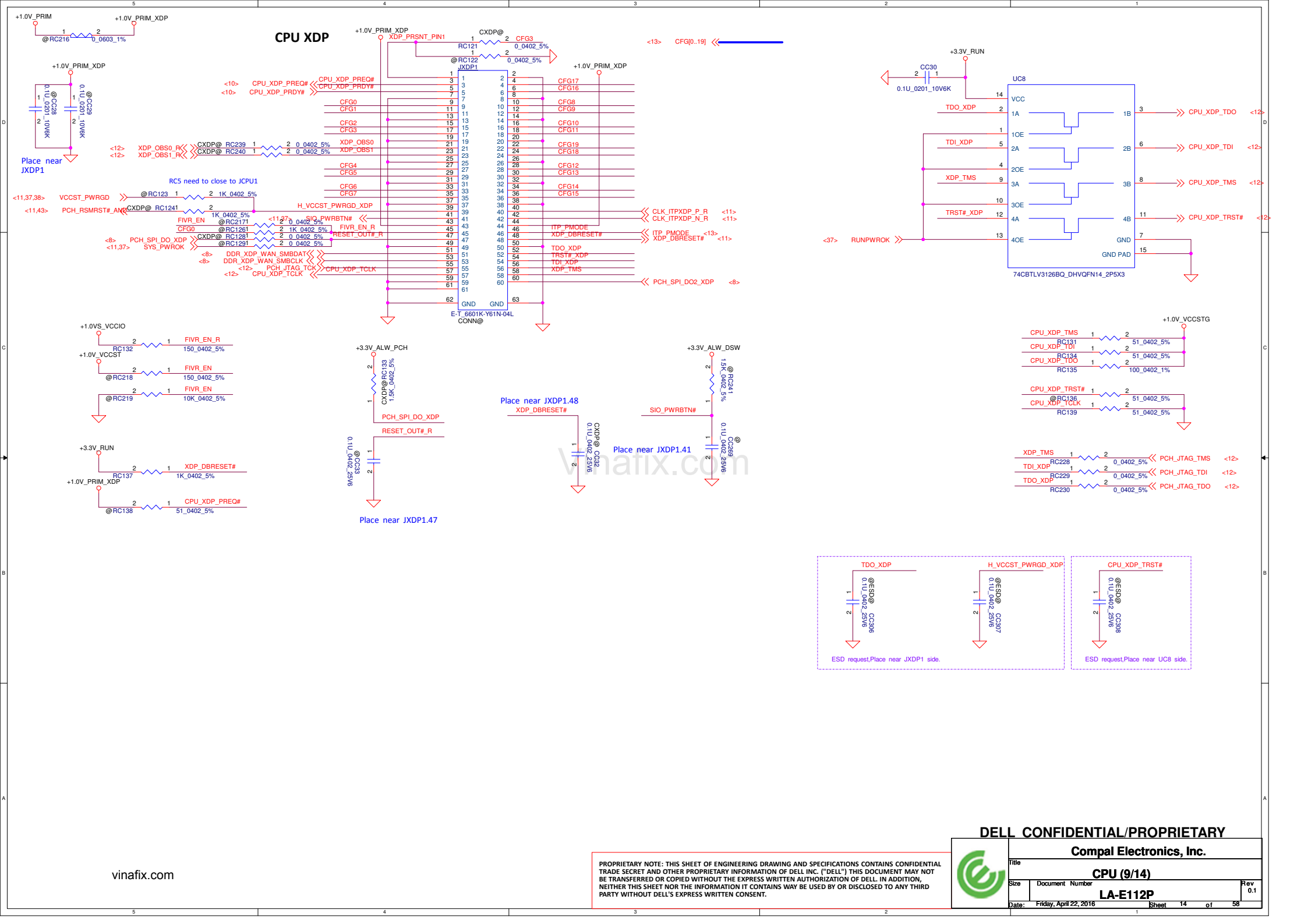


Compal Electronics, Inc.

Title: CPU (8/14)

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 13 of 58



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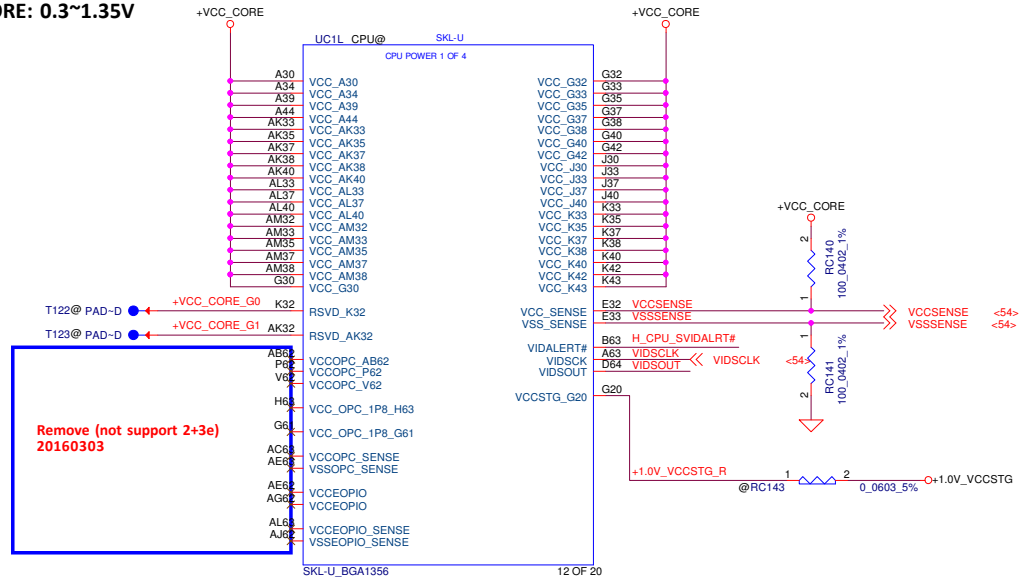
Title: CPU (9/14)

Size | Document Number: LA-E112P | Rev: 0.1

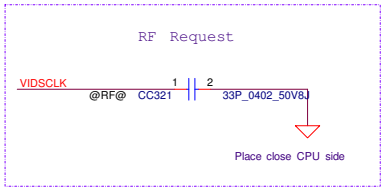
Date: Friday, April 22, 2016 | Sheet 14 of 58

+VCC_CORE: 0.3~1.35V



Remove (not support 2+3e)
20160303

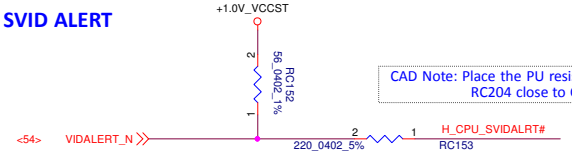
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



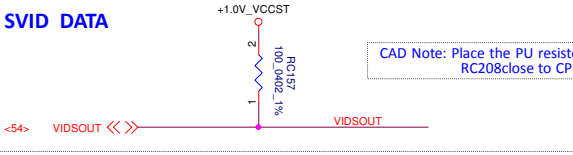
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

SVID ALERT



SVID DATA



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Title: CPU (10/14)

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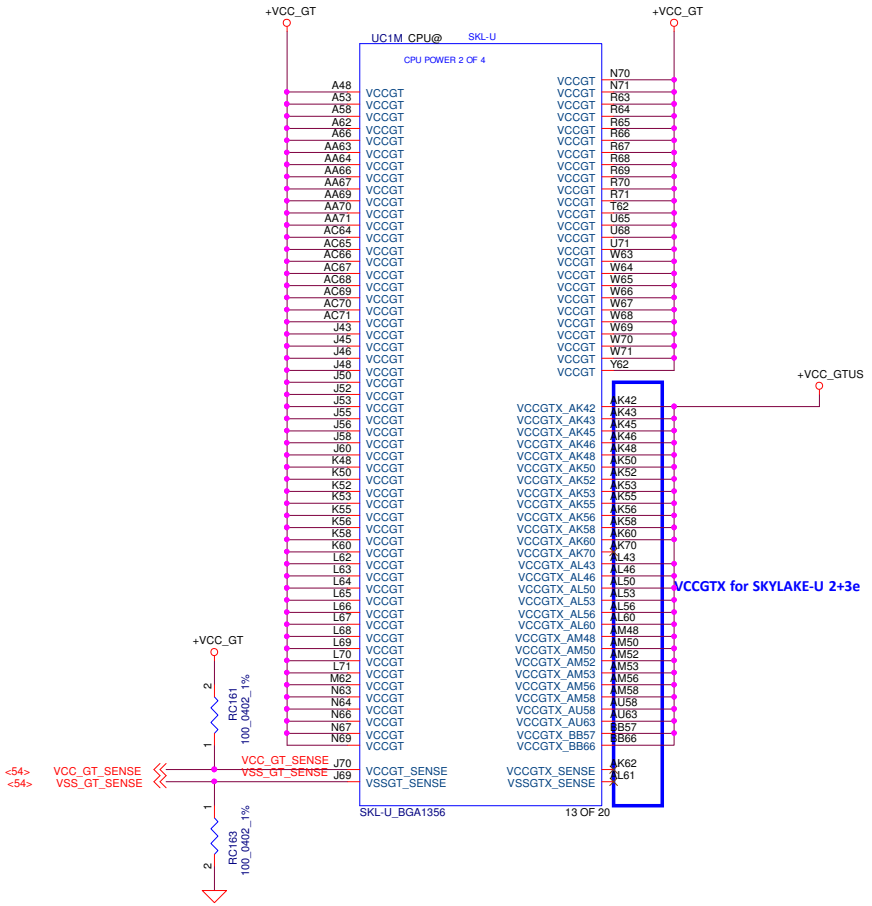
Date: Friday, April 22, 2016 | Sheet 15 of 58

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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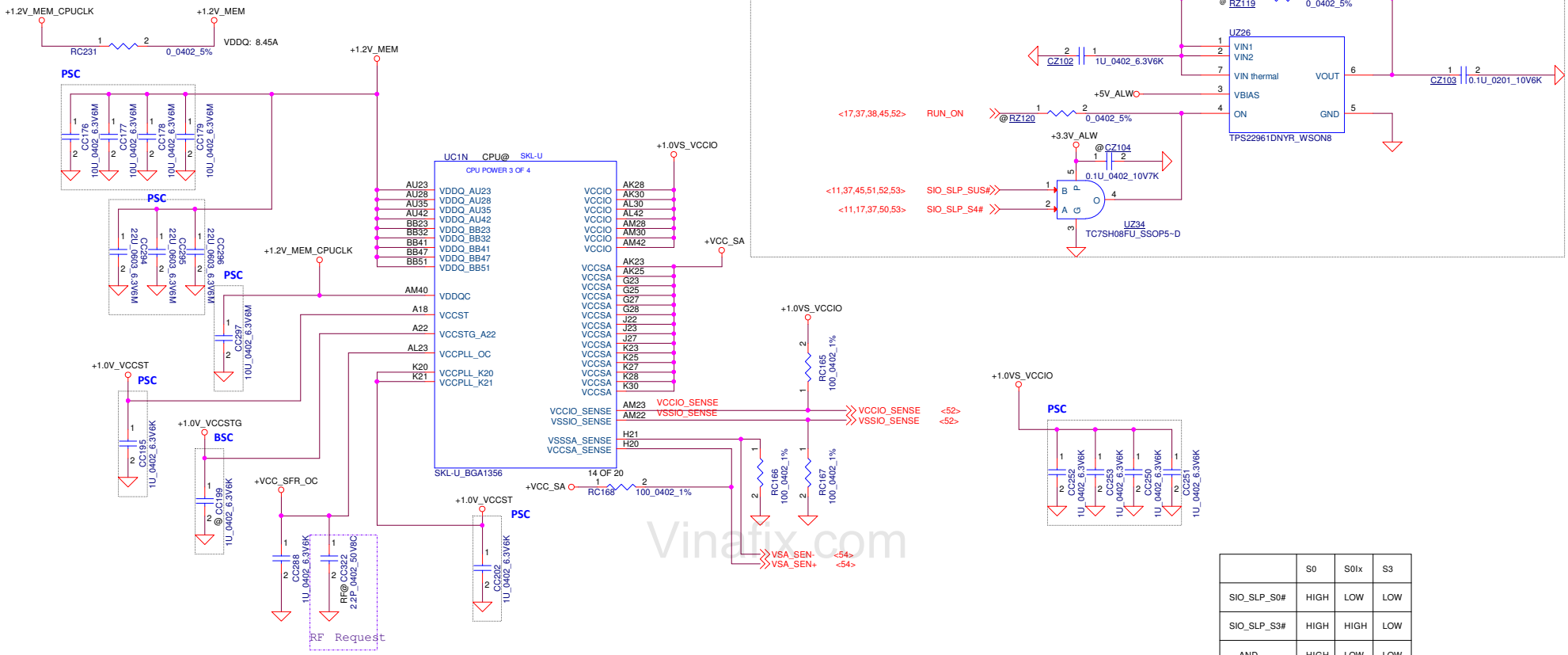
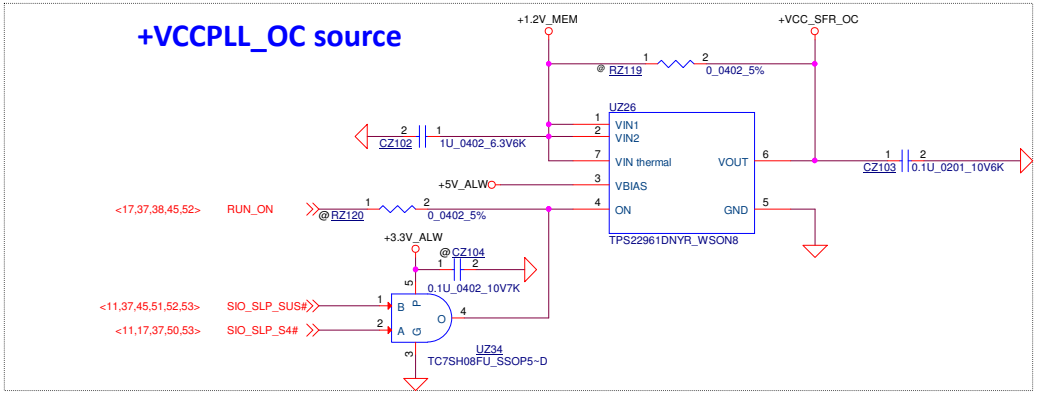
Title: CPU (11/14)

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 16 of 58

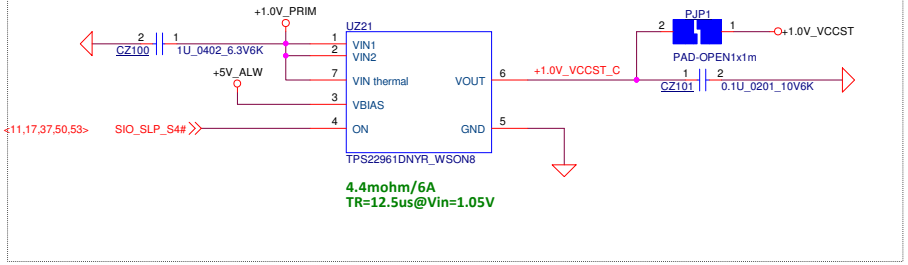


+VCCPLL_OC source

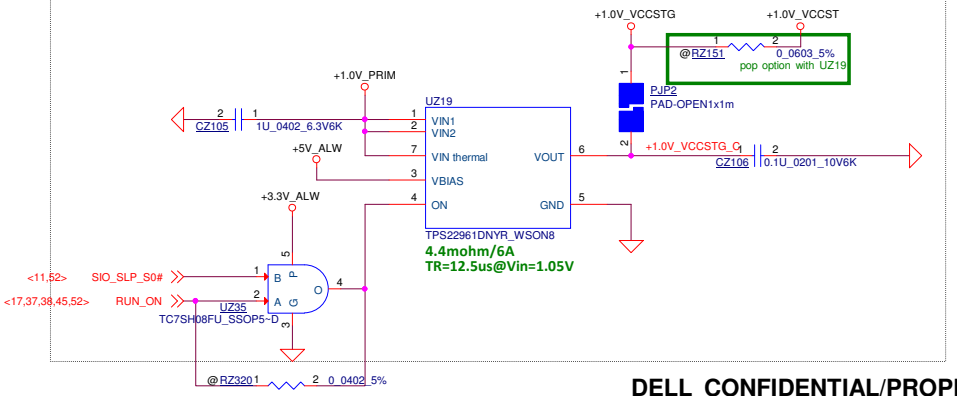


	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCST source



+1.0V_VCCSTG source



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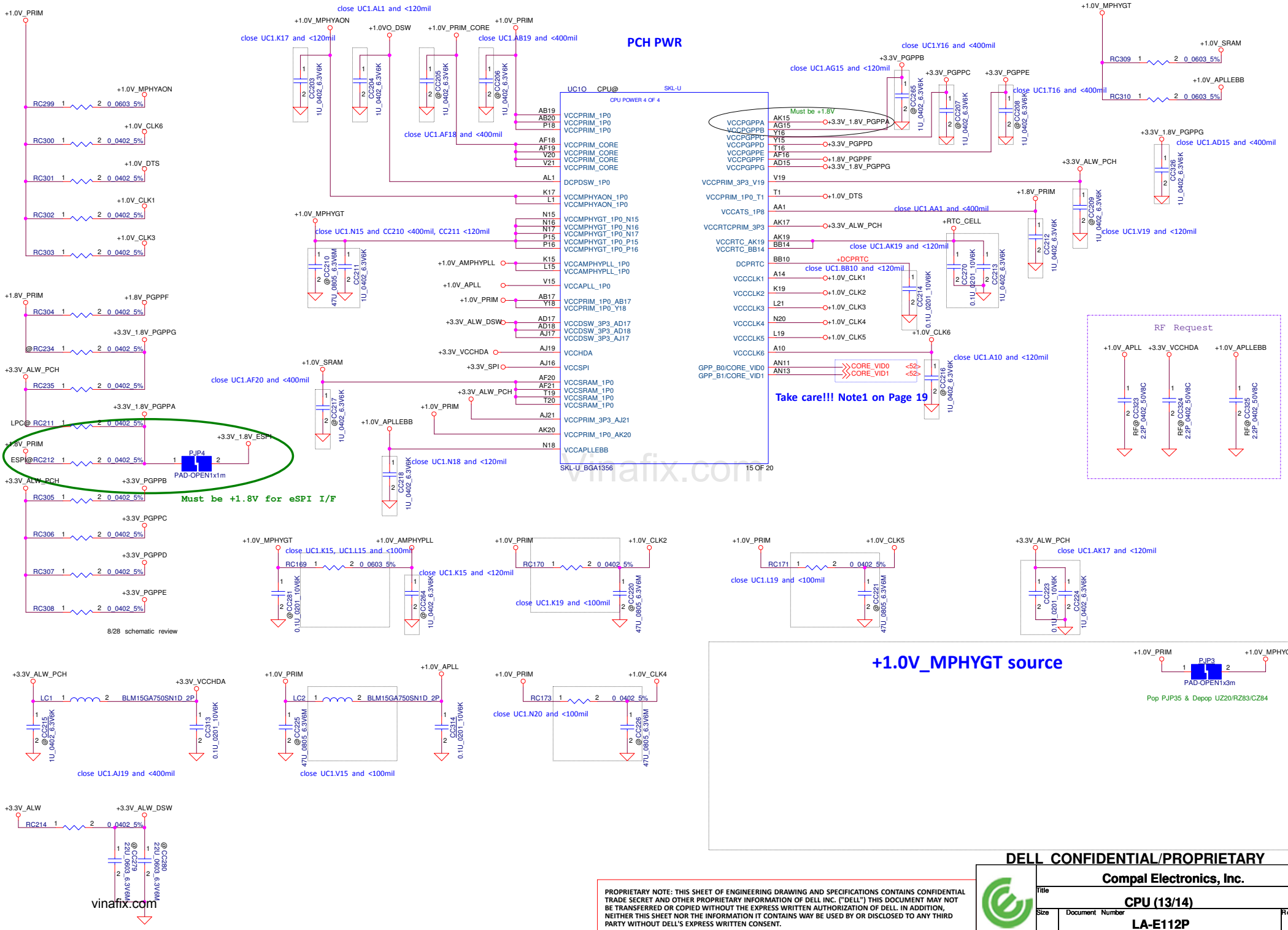
Compal Electronics, Inc.

Title: CPU (12/14)

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 17 of 58


PCH PWR
SKL-U
CPU POWER 4 OF 4
SKL-U_BGA1356
15 OF 20
Must be +1.8V for eSPI I/F
Must be +1.8V
Take care!!! Note1 on Page 19
RF Request
+1.0V_MPHYGT source
Pop PJP35 & Depop UZ20/RZ83/CZ84
8/28 schematic review
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Compal Electronics, Inc.
CPU (13/14)
LA-E112P
Friday, April 22, 2016
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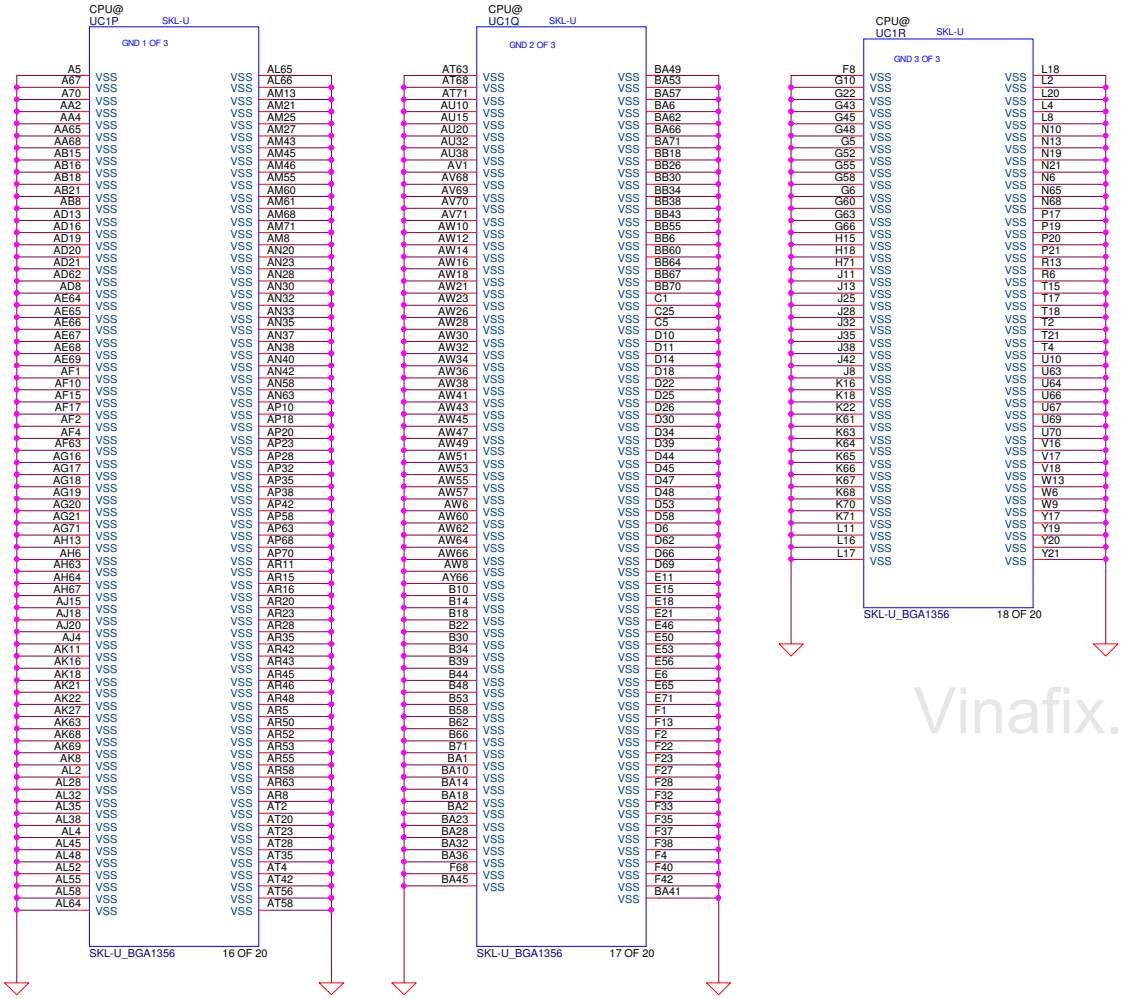
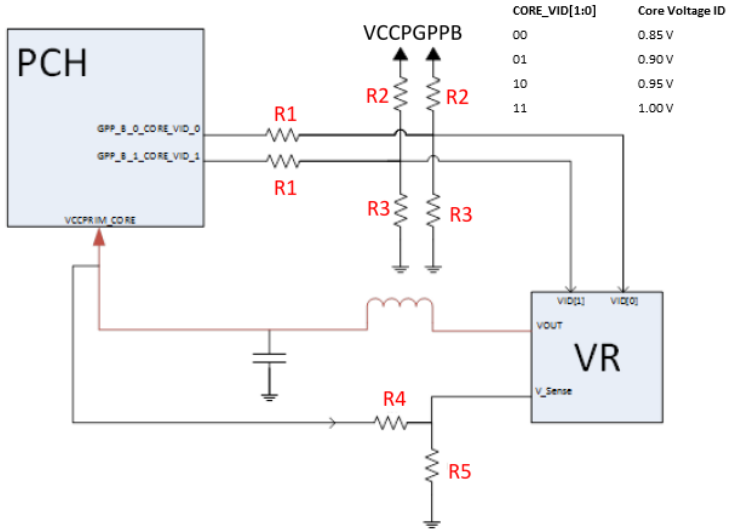


Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Title	CPU (14/14)
Size	Document Number: LA-E112P
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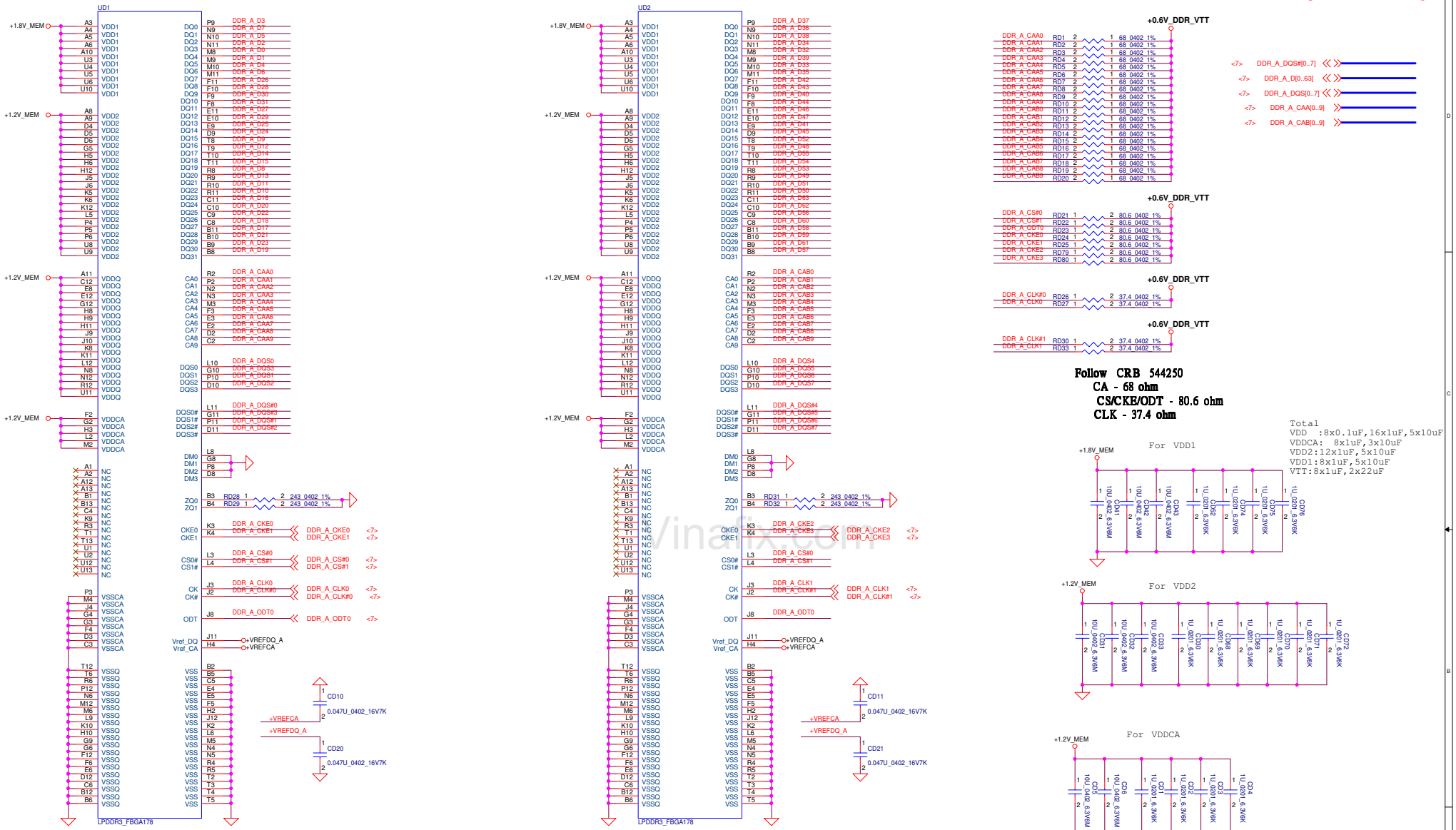
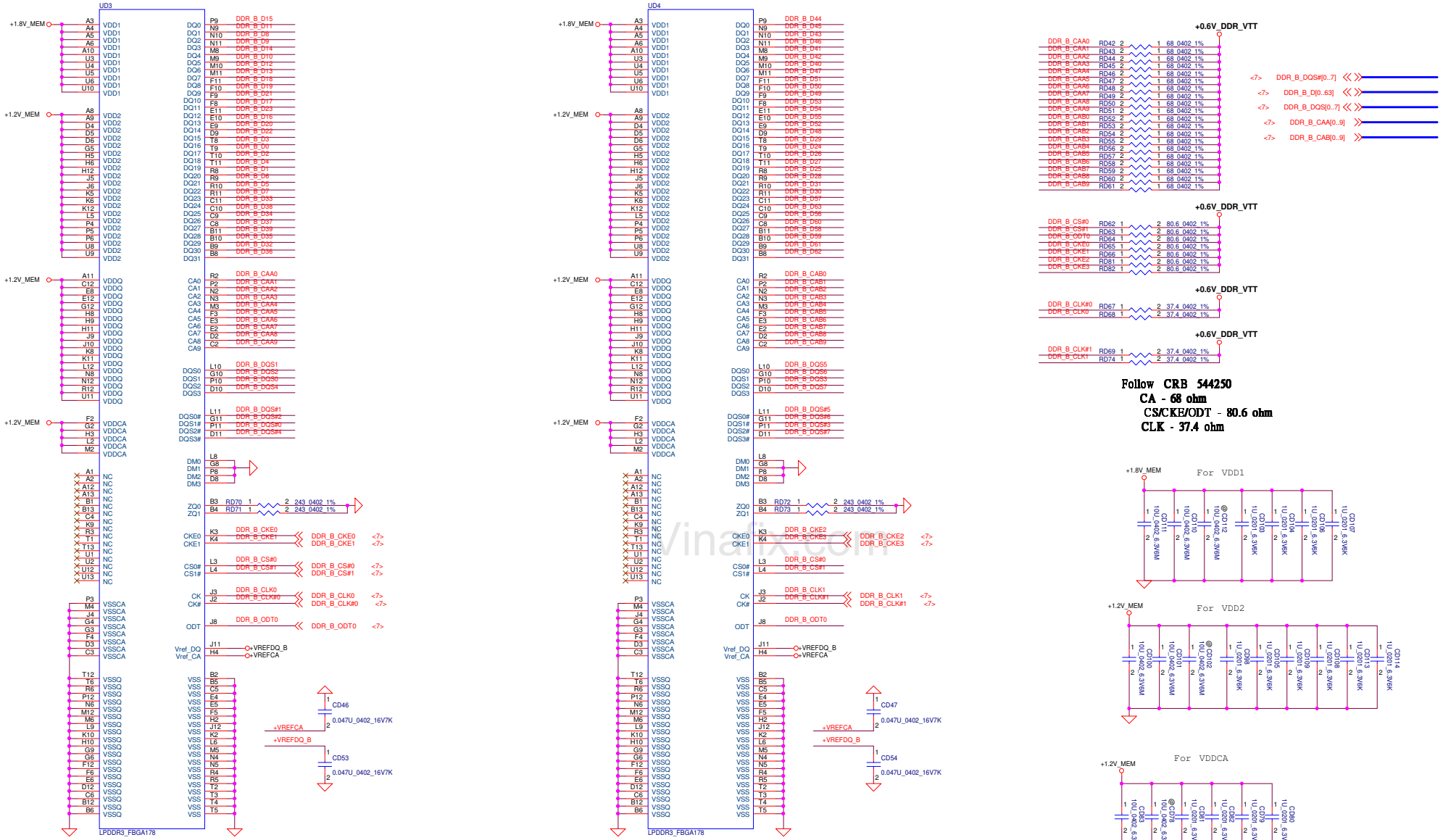
Date: Friday, April 22, 2016	Sheet 19 of 58

For LPDDR3

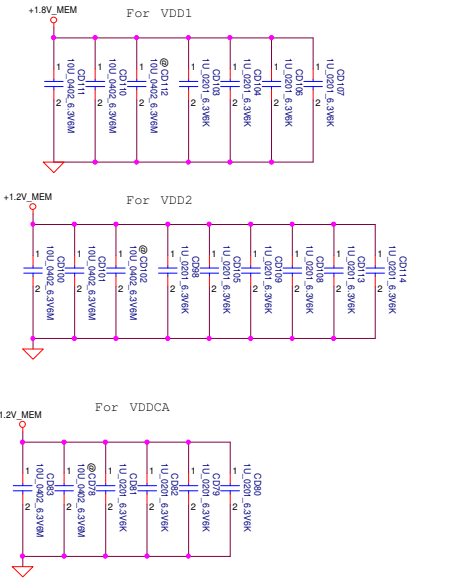


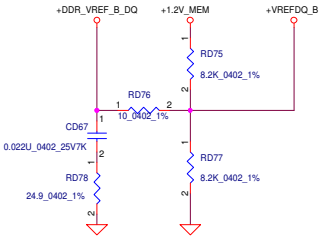
Compal Electronics, Inc.	
Title	LPDDR3
Size	Document Number: LA-E112P
Rev	0.1
Date:	Friday, April 22, 2016
Sheet	20 of 58

For LPDDR3



Follow CRB 544250
CA - 68 ohm
CS/CKE/ODT - 80.6 ohm
CLK - 37.4 ohm





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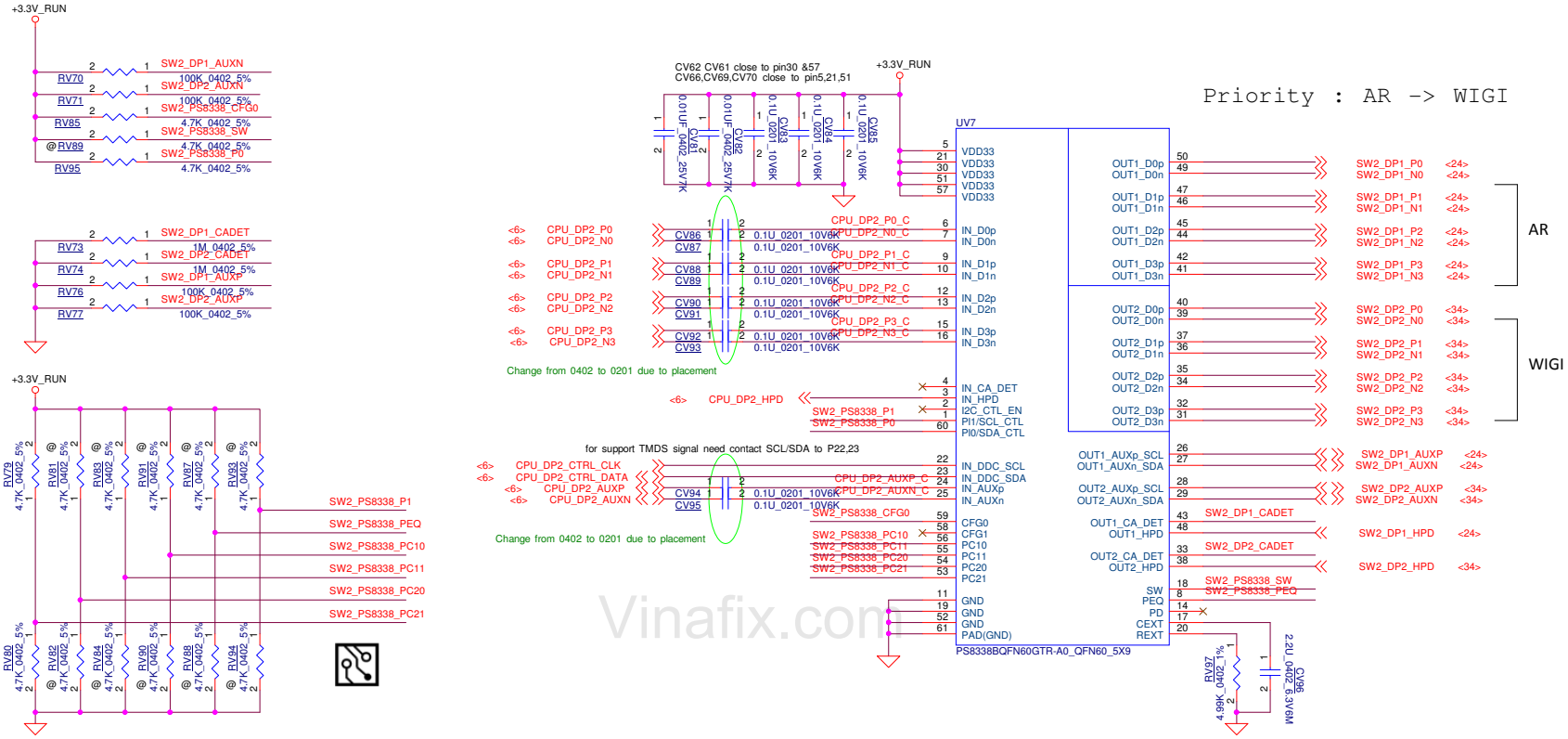
Title: LPDDR3			
Size	Document Number: LA-E112P		Rev: 0.1
Date: Friday, April 22, 2016		Sheet 21 of 58	

For Steamboat12/14 &Kirkwood



Port switching control or priority configuration. Internal pull down ~150KΩ , 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged (default)
SW = H: Port2 has higher priority when both ports are plugged

vender sugguest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

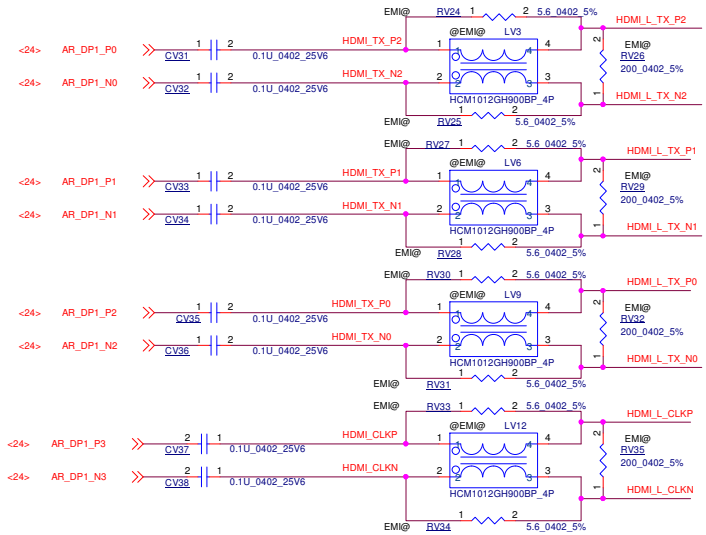
PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

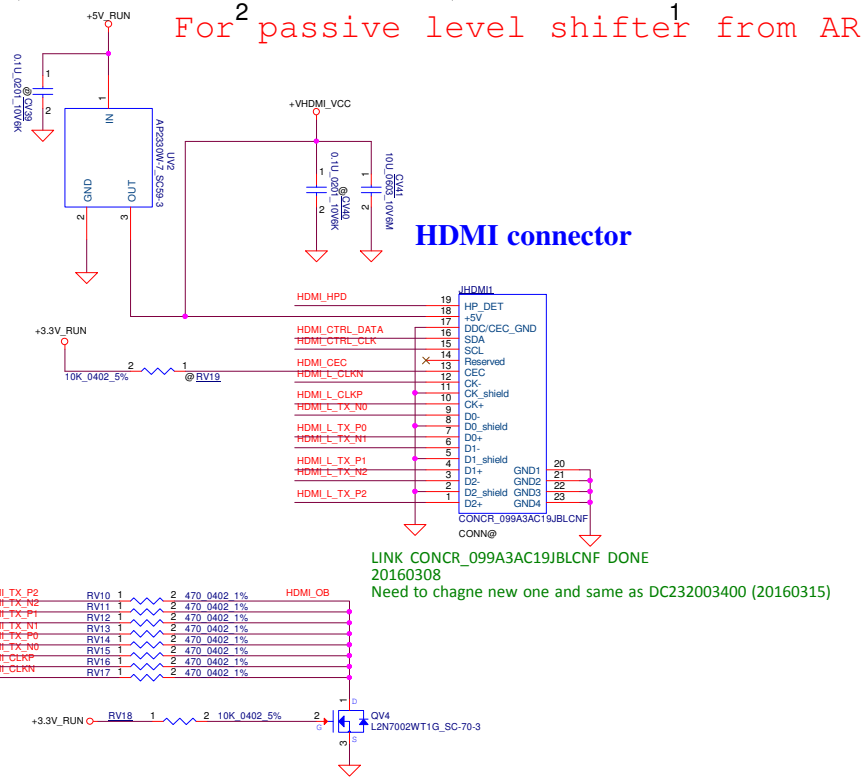
Compal Electronics, Inc.

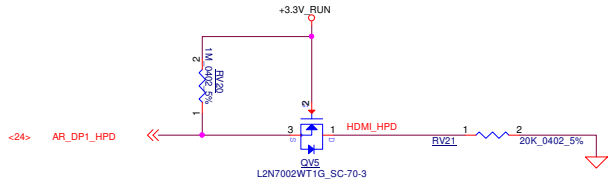
Title: DP SW2 PS8338

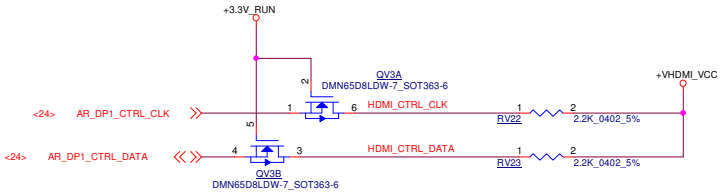
Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 22 of 58









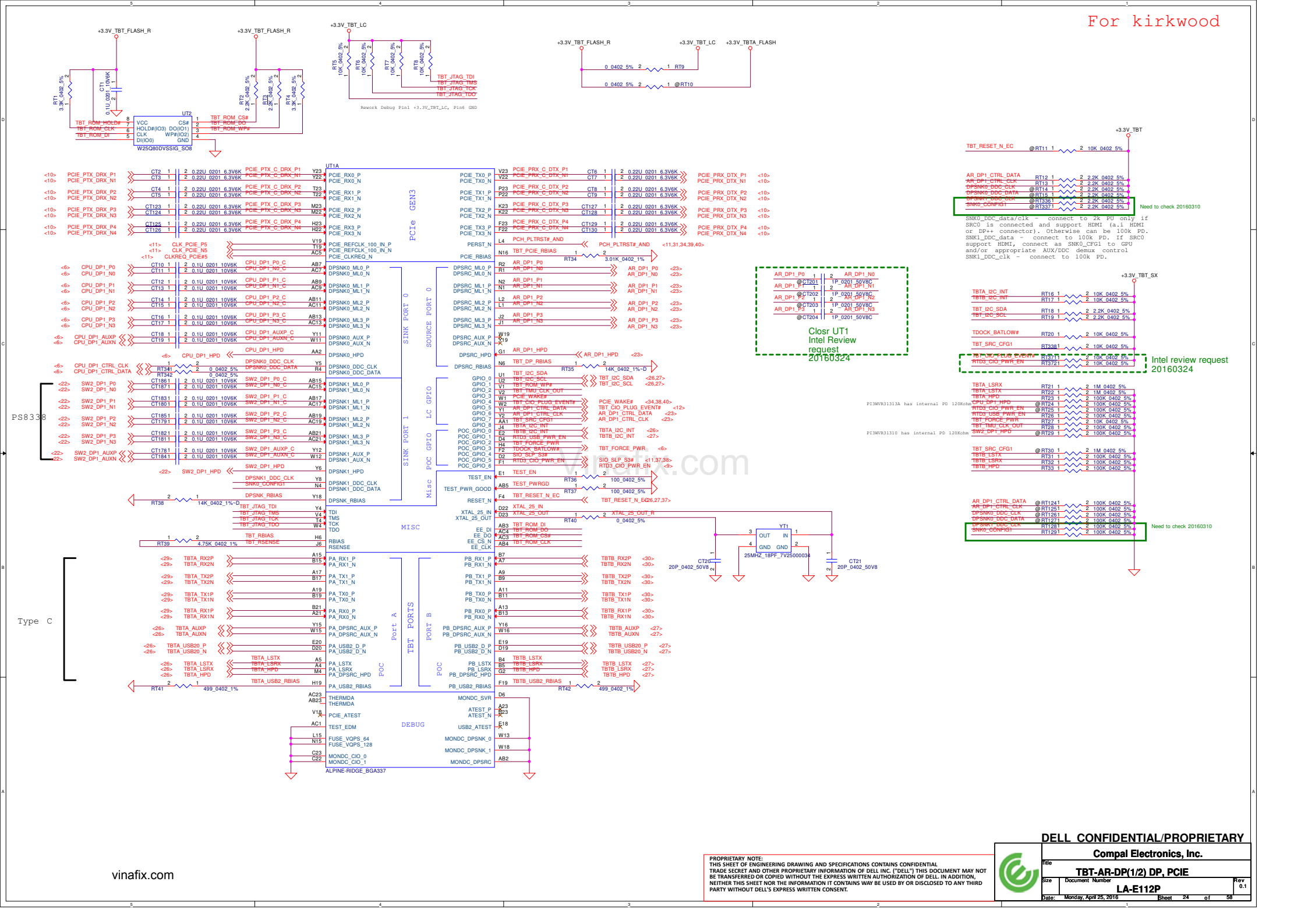
Compal Electronics, Inc.

Title: HDMI CONN

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 23 of 58

For kirkwood

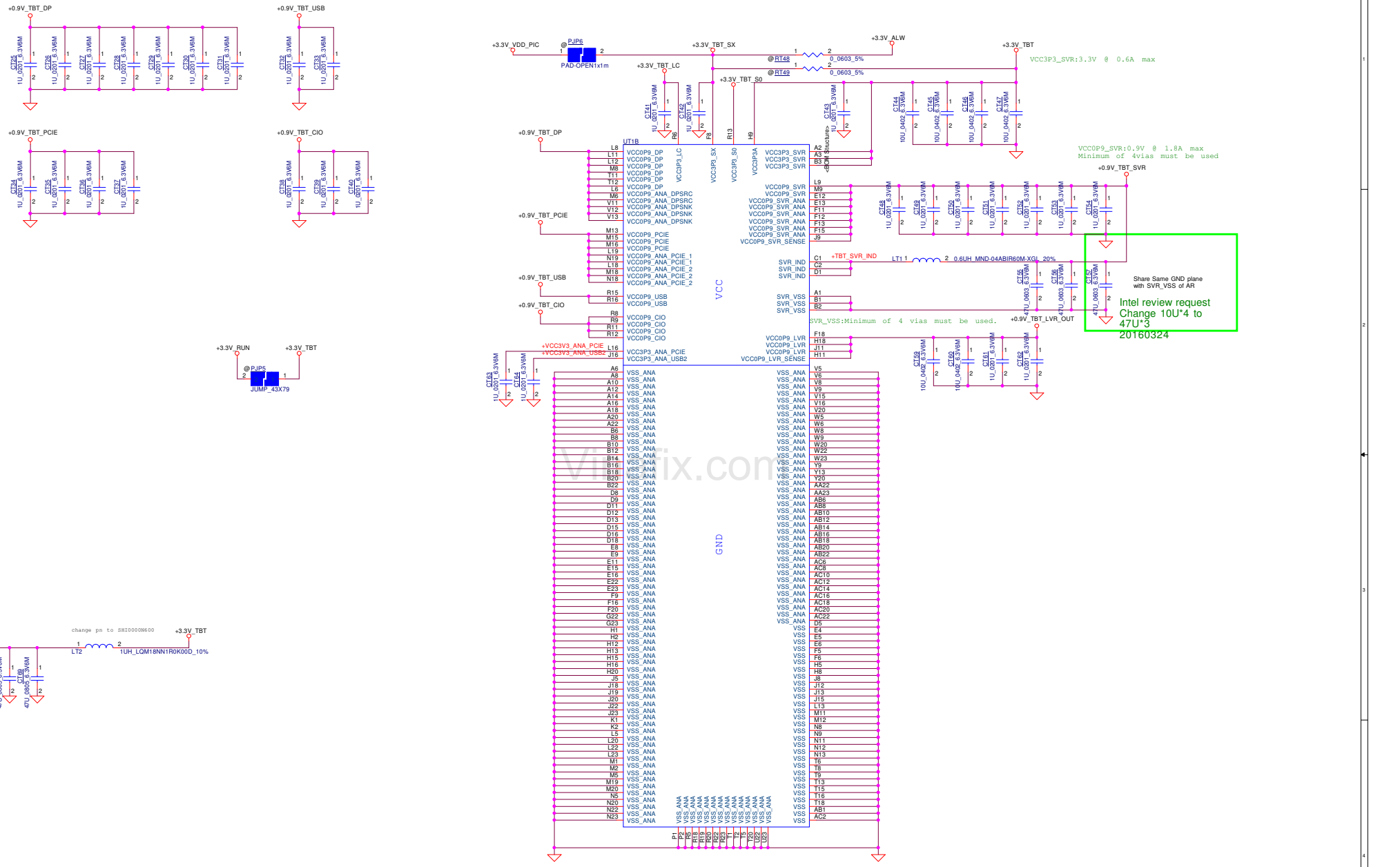


Compal Electronics, Inc.

Title: TBT-AR-DP(1/2) DP, PCIE

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 24 of 58

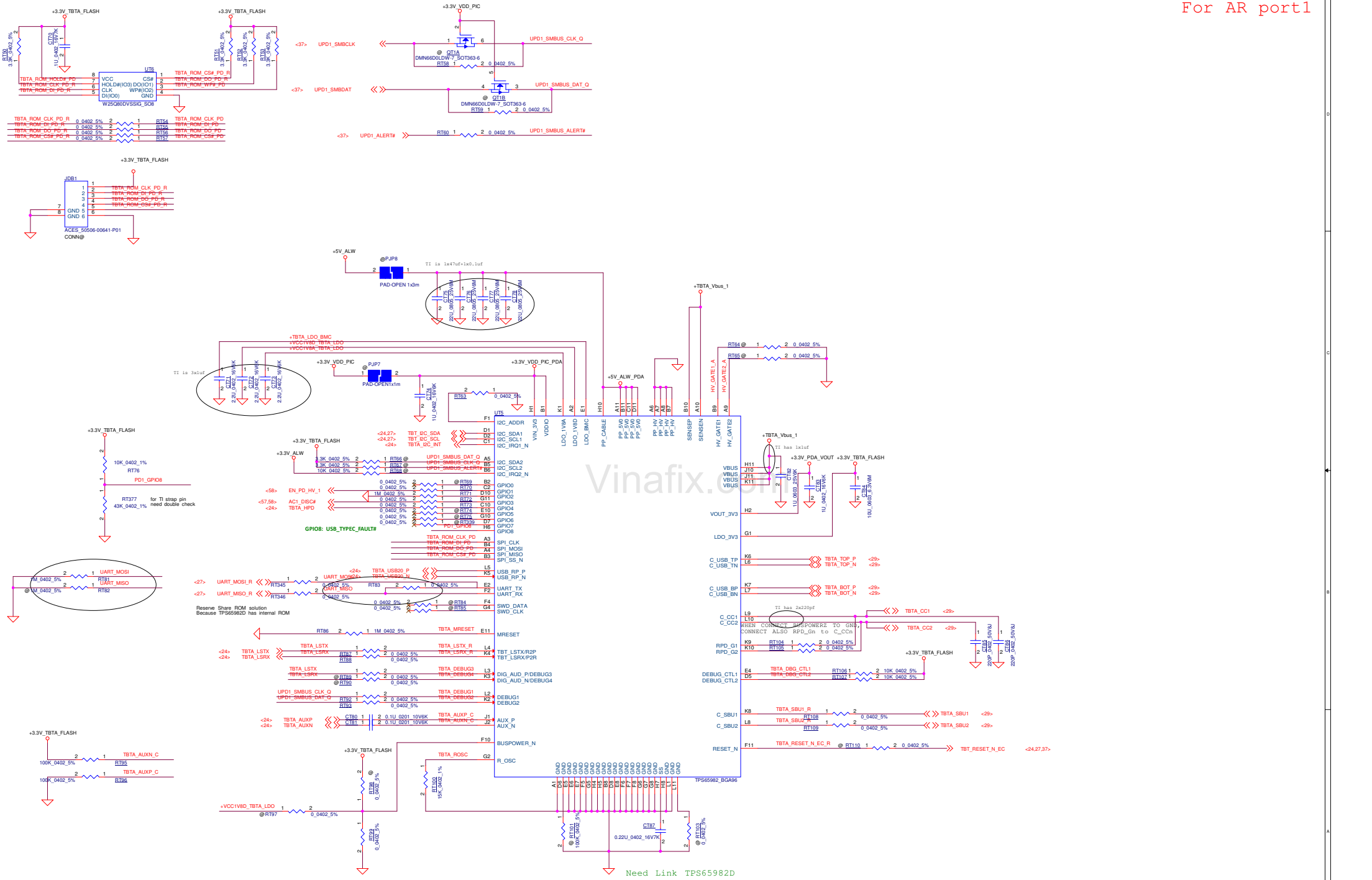


Compal Electronics, Inc.

Title: TBT-AR-SP(2/2) PWR,VSS

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 25 of 58



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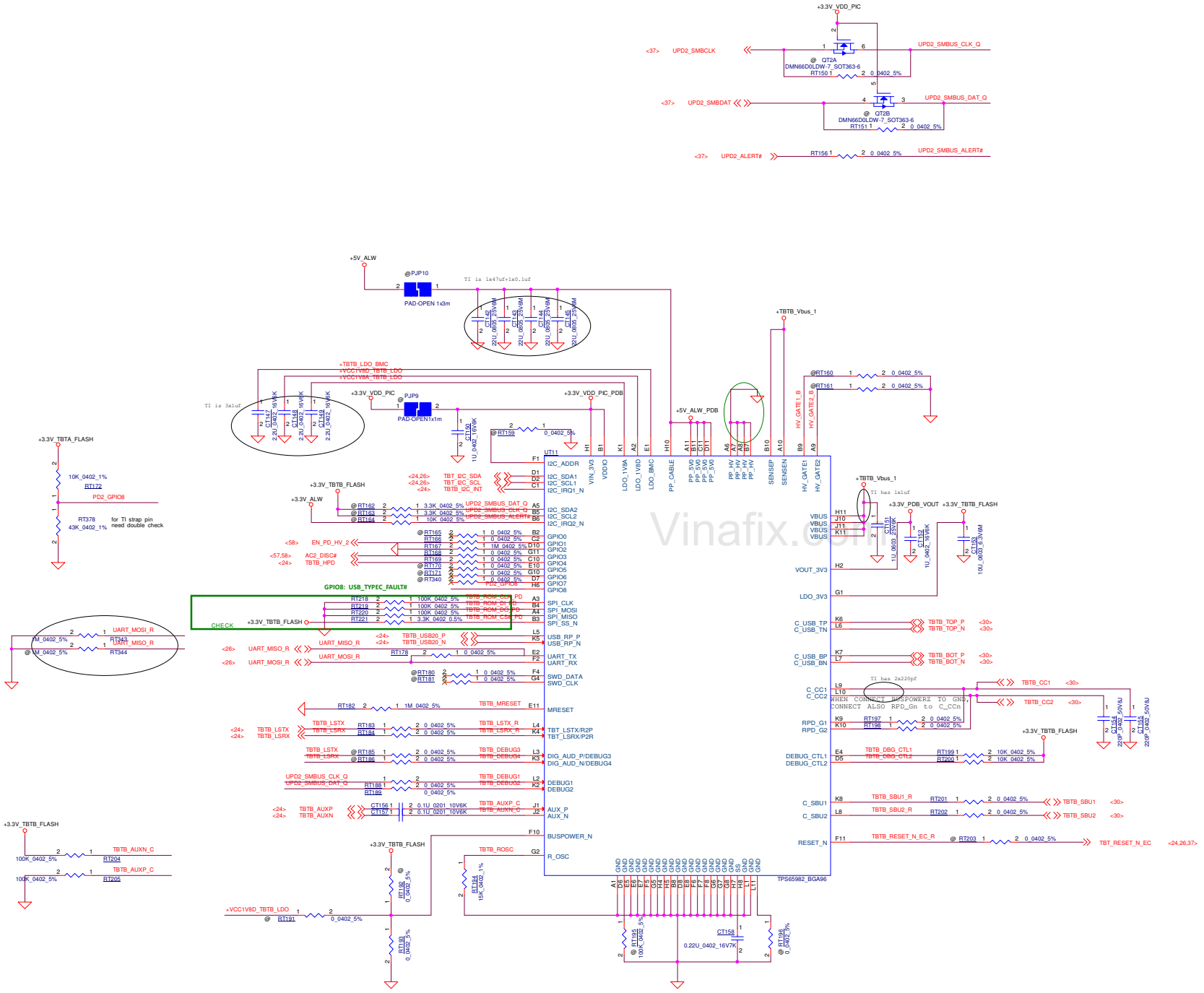
Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 26 of 58



Compal Electronics, Inc.

Title: [Type C]PD Controller TI-2

Size: | Document Number: LA-E112P | Rev: 0.1

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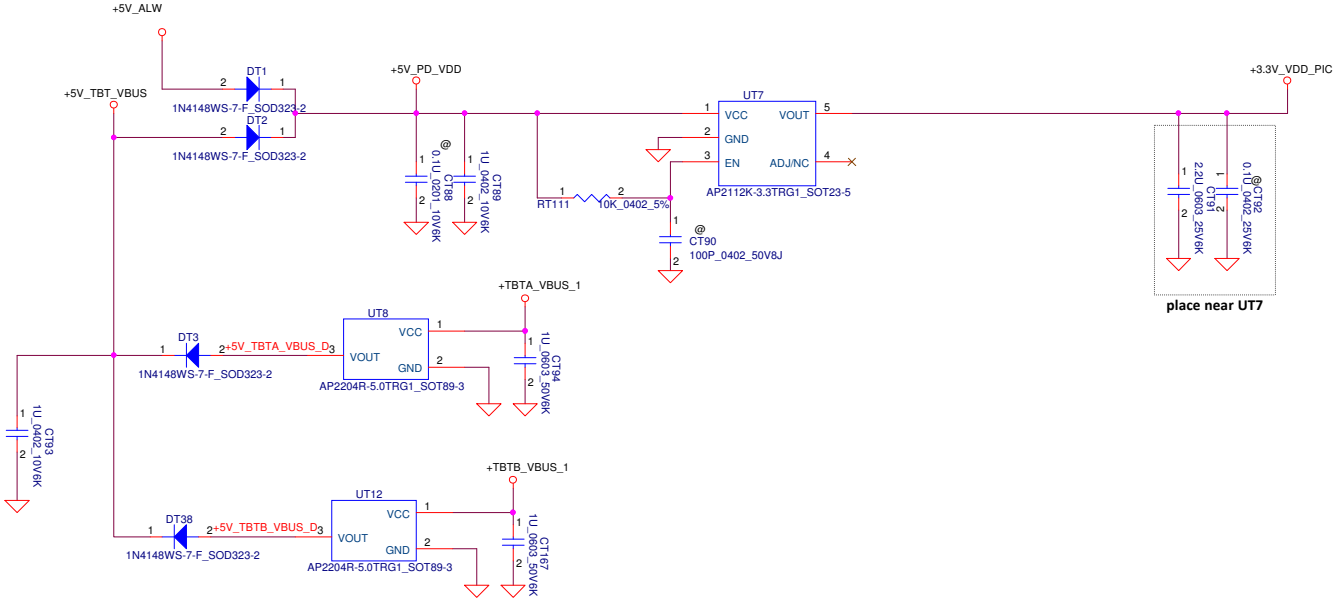
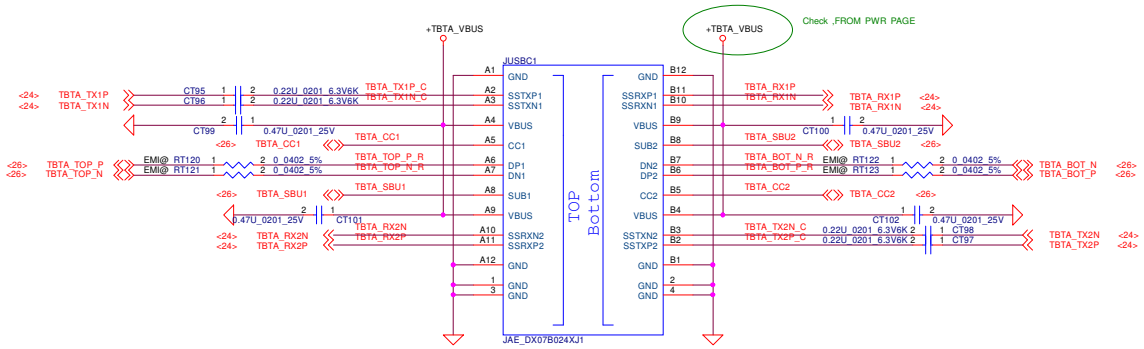
For kirkwood



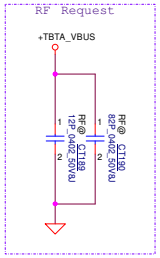
DELL CONFIDENTIAL/PROPRIETARY

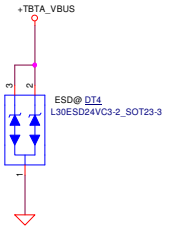
Compal Electronics, Inc.		
Title: [Type C]PD Power-2		
Size	Document Number: LA-E112P	Rev: 0.1
Date: Friday, April 22, 2016	Sheet 28 of 58	

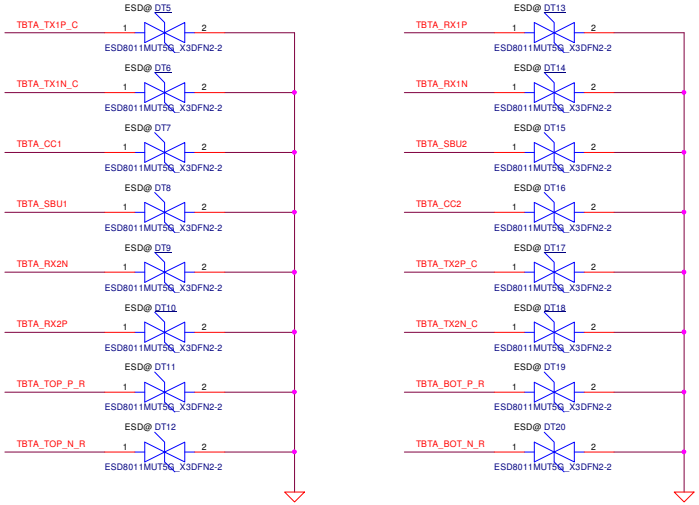
For AR Config

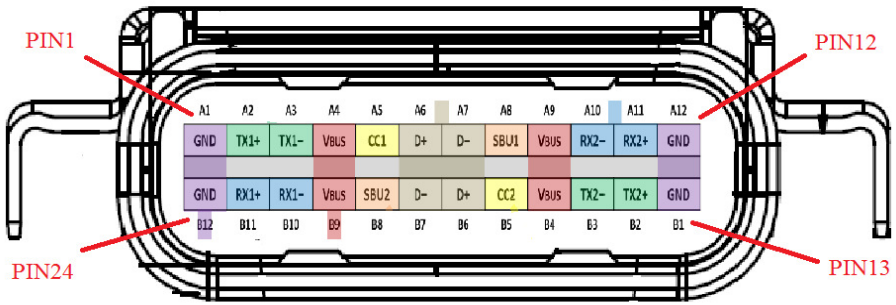


LINK JAE_DX07B024XJ1 DONE
20160321









Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E112P | Rev: 0.1

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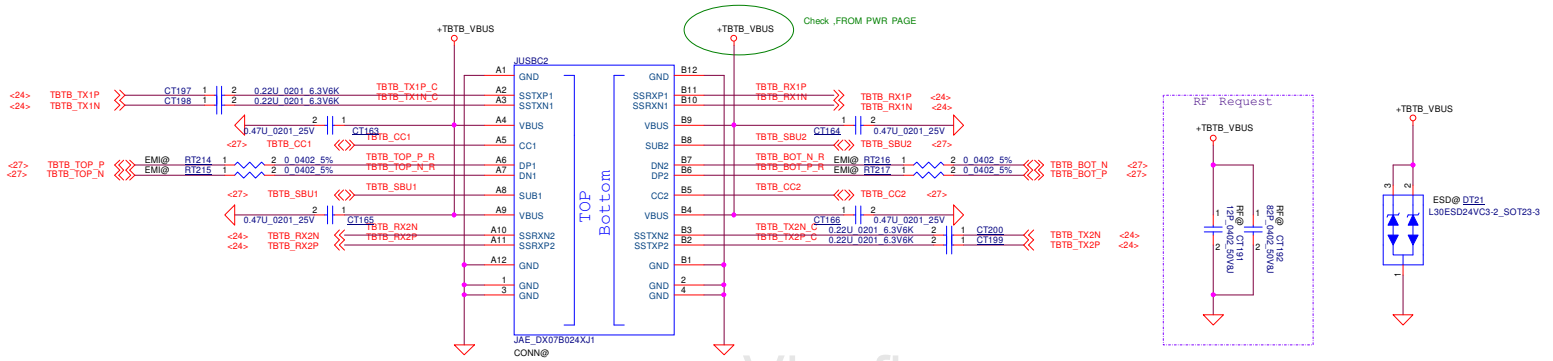
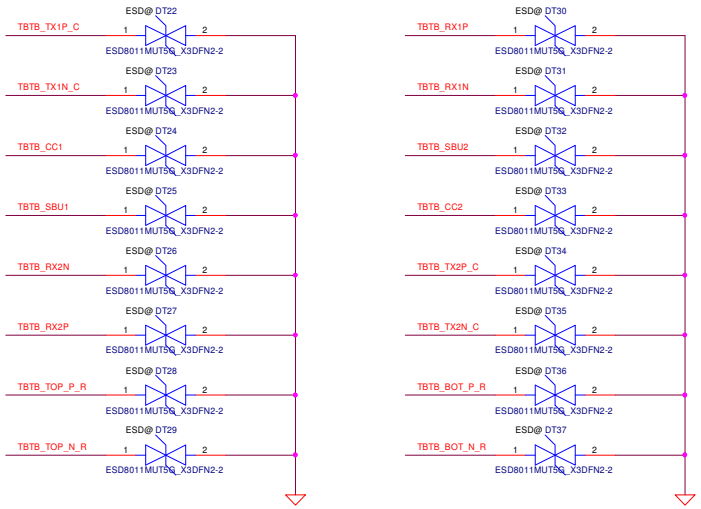
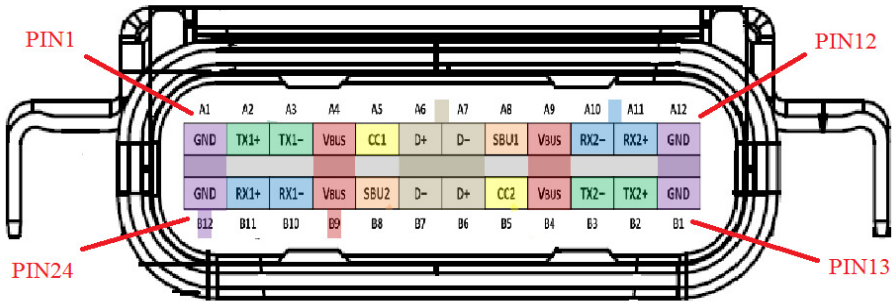


LINK JAE_DX07B024XJ1 DONE
20160321





Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C-2

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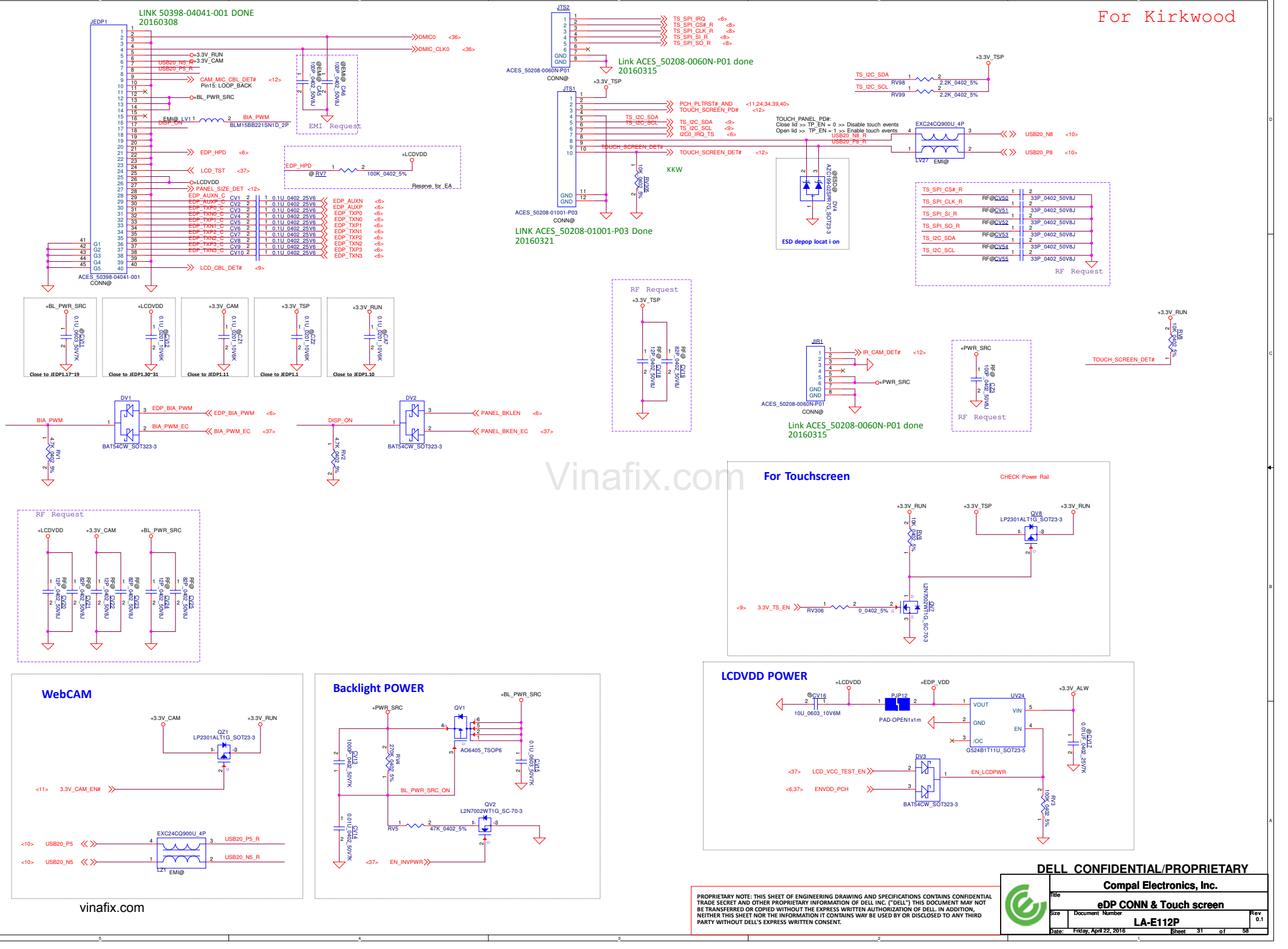
For Kirkwood
LINK 50398-04041-001 DONE
20160308
JEDP1
ACES_50398-04041-001
CONN@
DMIC0
DMIC_CLK0
+3.3V_RUN
+3.3V_CAM
USB20_N5
USB20_P5_R
CAM_MIC_CBL_DET#
Pin15: LOOP_BACK
+BL_PWR_SRC
EMI@ LV1
BLM15BB221SN1D_2P
BIA_PWM
DISP_ON
EMI Request
EDP_HPD
LCD_TST
+LCDVDD
PANEL_SIZE_DET
EDP_AUXN_C
EDP_AUXP_C
EDP_TXP0_C
EDP_TXN0_C
EDP_TXP1_C
EDP_TXN1_C
EDP_TXP2_C
EDP_TXN2_C
EDP_TXP3_C
EDP_TXN3_C
LCD_CBL_DET#
Reserve for EA
JTS2
ACES_50208-0060N-P01
CONN@
TS_SPI_IRQ
TS_SPI_CS#_R
TS_SPI_CLK_R
TS_SPI_SI_R
TS_SPI_SO_R
Link ACES_50208-0060N-P01 done
20160315
JTS1
ACES_50208-01001-P03
CONN@
PCH_PLTRST#_AND
TOUCH_SCREEN_PD#
TS_I2C_SDA
TS_I2C_SCL
I2C0_IRQ_TS
TOUCH_SCREEN_DET#
KKW
Link ACES_50208-01001-P03 Done
20160321
TOUCH_PANEL_PD#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events
EXC24CQ900U_4P
LV27 EMI@
USB20_N8
USB20_P8
ESD depop locat i on
RF Request
IR_CAM_DET#
+PWR_SRC
3.3V_TS_EN
BIA_PWM
DISP_ON
BAT54CW_SOT323-3
EDP_BIA_PWM
BIA_PWM_EC
PANEL_BKLEN
PANEL_BKEN_EC
For Touchscreen
CHECK Power Rail
LP2301ALT1G_SOT23-3
L2N7002WT1G_SC-70-3
WebCAM
3.3V_CAM_EN#
Backlight POWER
AO6405_TSOP6
BL_PWR_SRC_ON
EN_INVPWR
LCDVDD POWER
PJP12
PAD-OPEN1x1m
G524B1T11U_SOT23-5
LCD_VCC_TEST_EN
ENVDD_PCH
EN_LCDPWR
BAT54CW_SOT323-3
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vinafix.com
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Compal Electronics, Inc.
Title
eDP CONN & Touch screen
Size
Document Number
LA-E112P
Rev
0.1
Date: Friday, April 22, 2016
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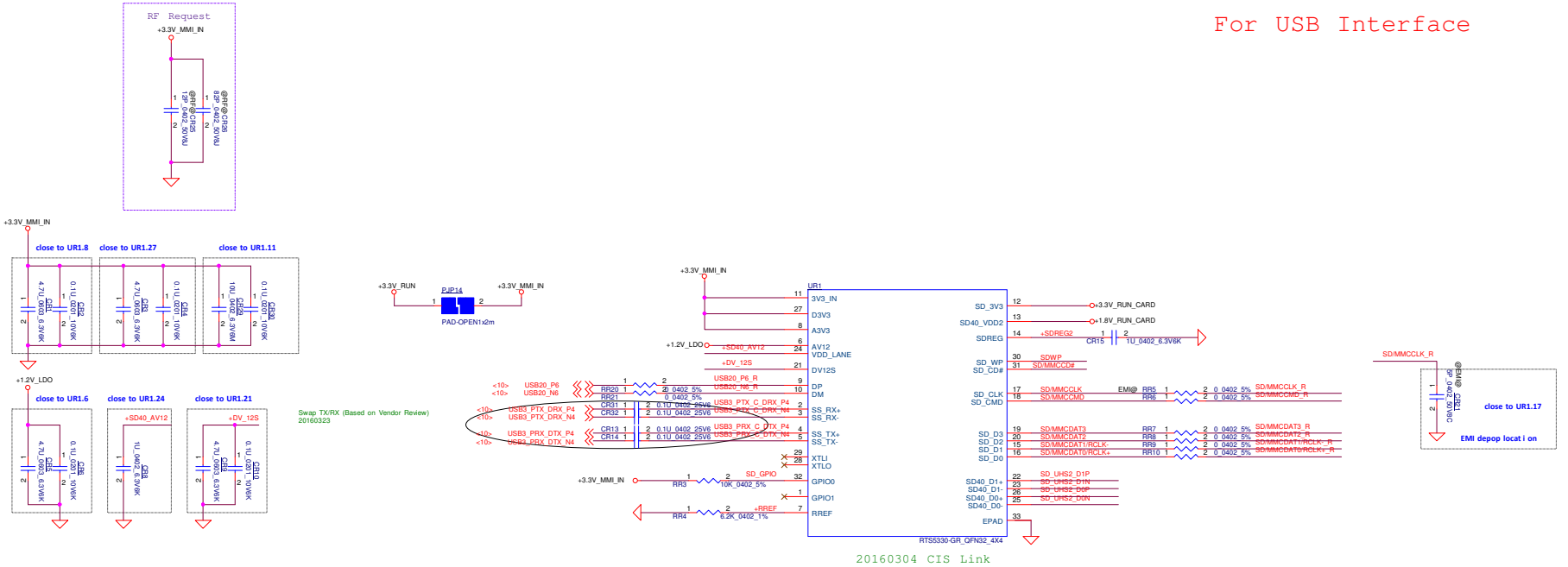
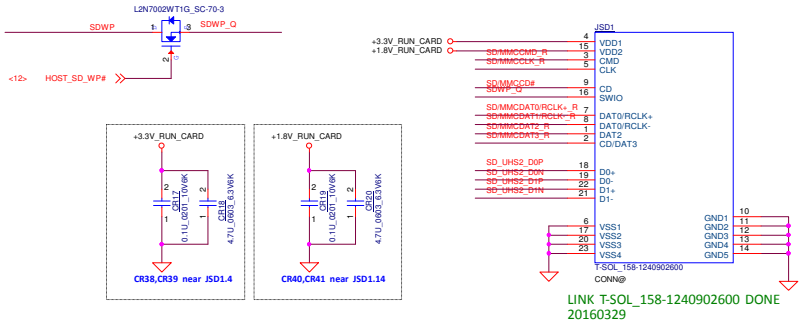


HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



Compal Electronics, Inc.

Title: Card Reader RTS5330

Size: Document Number: LA-E112P

Rev: 0.1

Date: Friday, April 22, 2016

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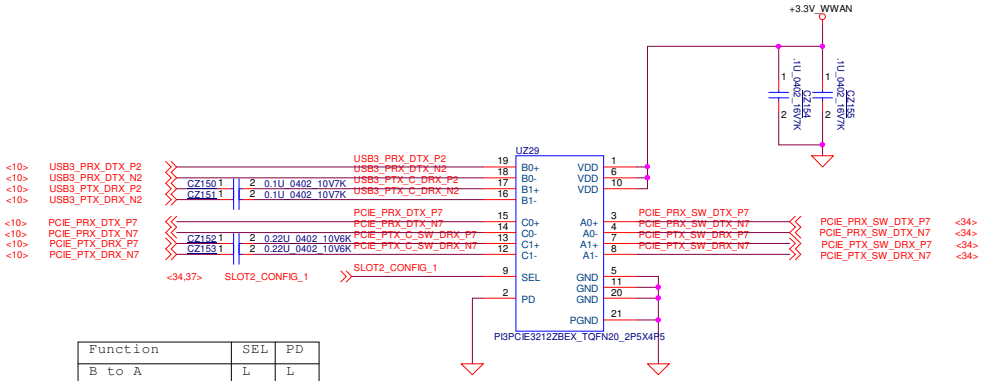
PCIE/USB MUX

NEED LINK TI HD3SS3212 as main



Function	SEL	PD
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H

STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Compal Electronics, Inc.

Title: USB/PCIE MUX

Size | Document Number: LA-E112P | Rev: 0.1

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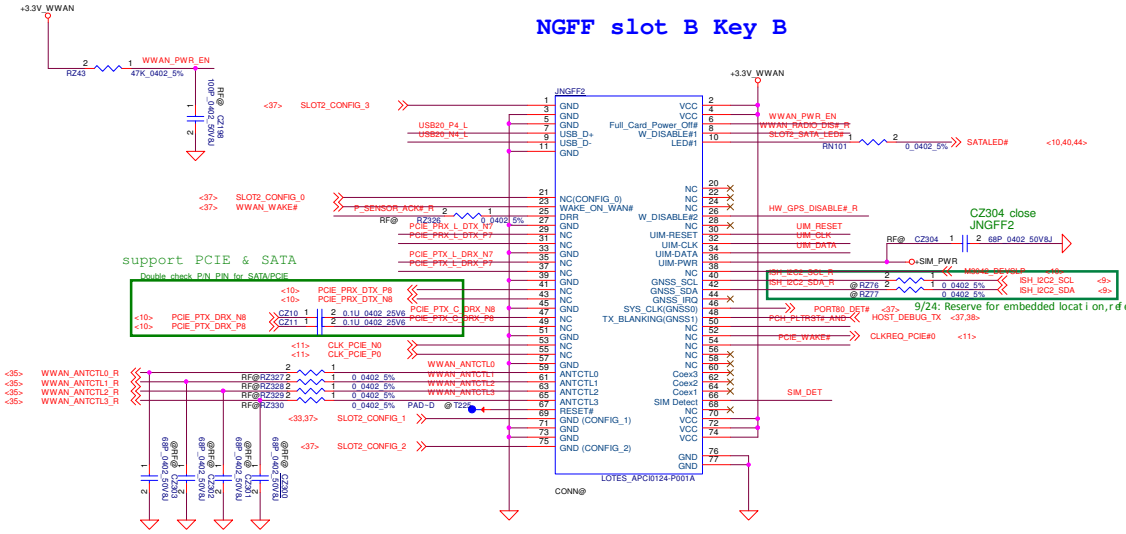
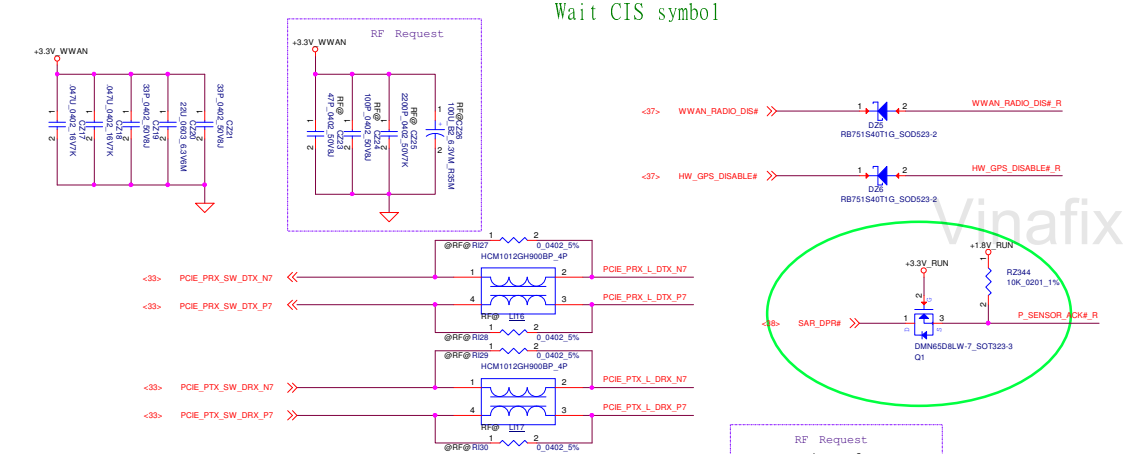
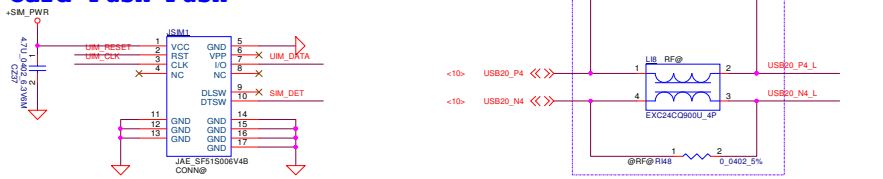
NGFF slot B Key B



Wait CIS symbol

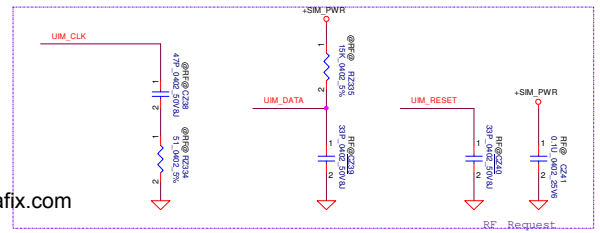


SIM Card Push-Push



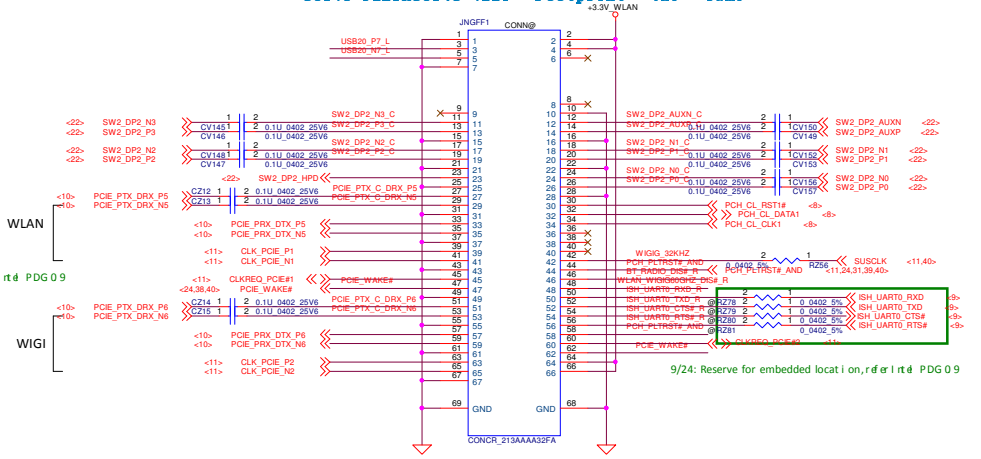
JAE_SF51S006V4DR1000Q LINK DONE

20160321 (Temp symbol is correct, SP number is wrong on DTSW)

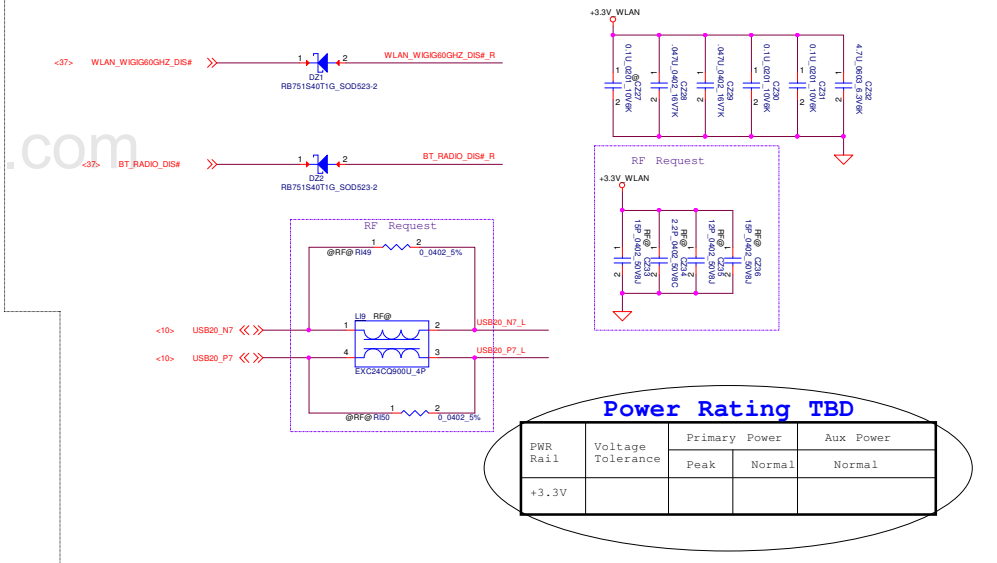


NGFF slot A Key A Only for Kirkwood

80148-3221&80148-4221 Footprint the same



Wait CIS symbol



Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power Peak	Primary Power Normal	Aux Power Normal
+3.3V				

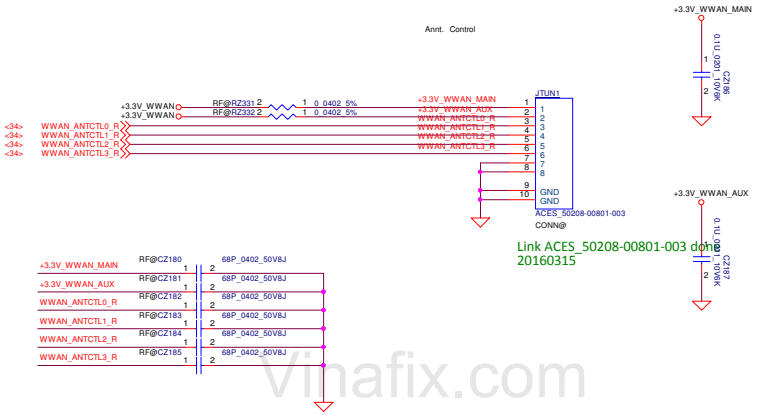
Compal Electronics, Inc.

Title: NGFF Card

Size: Document Number: LA-E112P Rev: 0.1

Date: Friday, April 22, 2016 Sheet 34 of 58

Only for Kirkwood



Link ACES_50208-00801-003 done 20160315

Compal Electronics, Inc.

Title: RF Tunable Conn

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

Change to 6pin to support 2 SPK vendor
Link ACES_50278-00601-001 DONE
20160325

Close to UA1

Close to UA1 pin6

place close to UA1 pin6

Place closely to Pin 14.

Add for solve pop noise and detect issue

need link SM01000NS00
Realtek suggest rated current : 2A

Place CA29 close to Codec

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

SLEEVE/RING2 please keep 40 mils trace width

RF Request

Add this Filter to avoid other components/chips be influenced

HP-Out-Right
HP-Out-Lef t
Nokia-MIC
iPhone-MIC

Global Headset
Universal Jack

Normal
Open

Link SINGA_2SJ3095-085111F DONE
20160308

CLASS-D POWER DOWN CONTROL CIRCUIT

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

HDA_Link is 3.3V,no need level shift circuit

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

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Compal Electronics, Inc.	
Title	Codec ALC3253
Size	Document Number: LA-E112P
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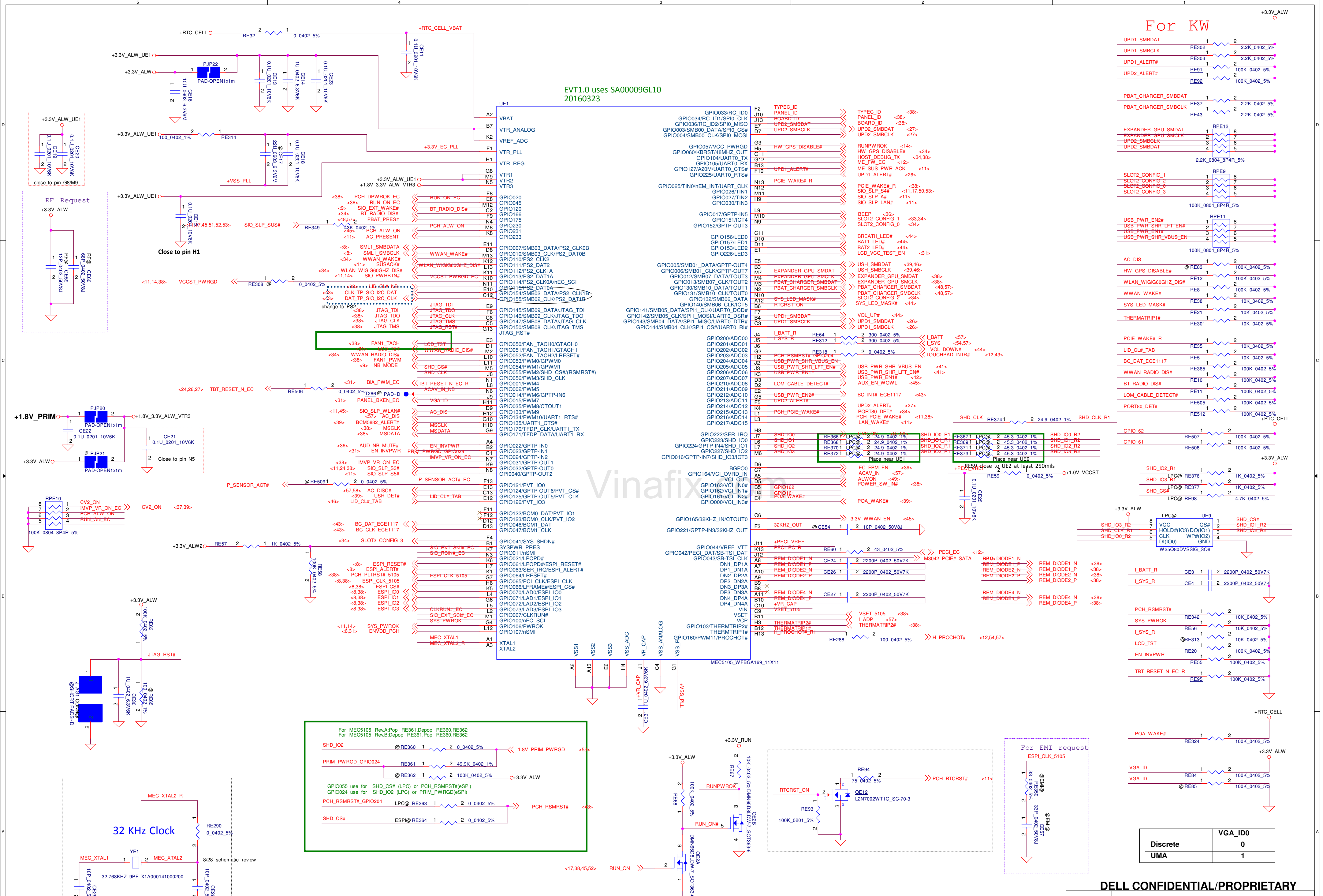

For KW
EVT1.0 uses SA00009GL10
20160323
UE1
MEC5105_WFBGA169_11X11
Close to pin H1
close to pin G8/M9
Close to pin N5
RF Request
change to PS2
Place near UE1
Place near UE9
RE59 close to UE2 at least 250mils
W25Q80DVSSIG_SO8
For MEC5105 Rev.A:Pop RE361,Depop RE360,RE362
For MEC5105 Rev.B:Depop RE361,Pop RE360,RE362
GPIO055 use for SHD_CS# (LPC) or PCH_RSMRST#(eSPI)
GPIO024 use for SHD_IO2 (LPC) or PRIM_PWRGD(eSPI)
32 KHz Clock
32.768KHZ_9PF_X1A000141000200
8/28 schematic review
For EMI request
L2N7002WT1G_SC-70-3
DMN65D8LDW-7_SOT363-6
vinafix.com

	VGA_ID0
Discrete	0
UMA	1

Compal Electronics, Inc.

Title: EC MEC5105

Size | Document Number: LA-E112P | Rev 0.1

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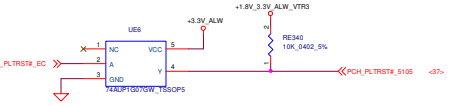
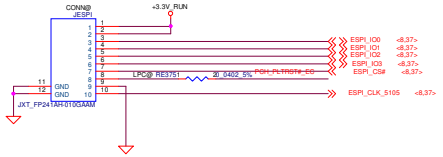
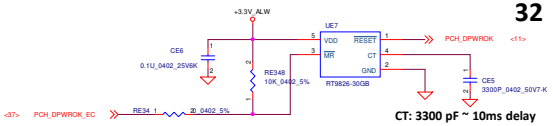
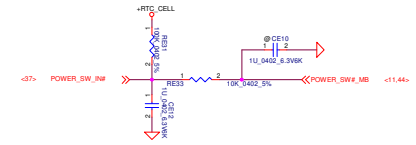


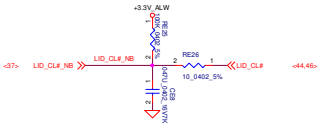
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

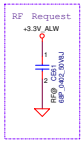


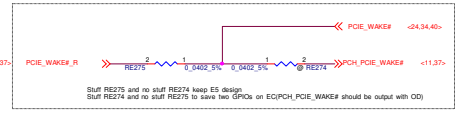


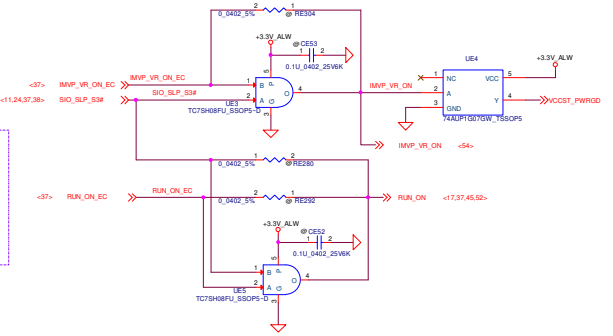
Reset Threshold Level 3.0V

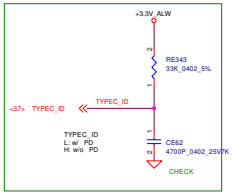




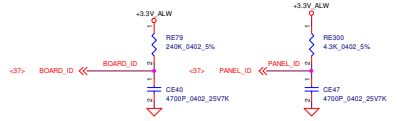








RE343	CE40	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

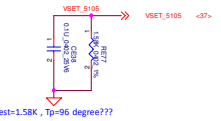


RE79	CE40	REV
* 240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

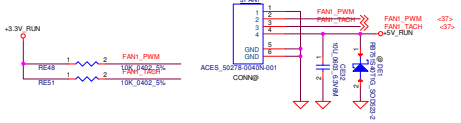
RE300	CE47	PANEL SIZE
240K	4700p	SB/BR 12"
130K	4700p	SB/BR 14"
33K	4700p	BR 15"
* 4.3K	4700p	KW 12/13"

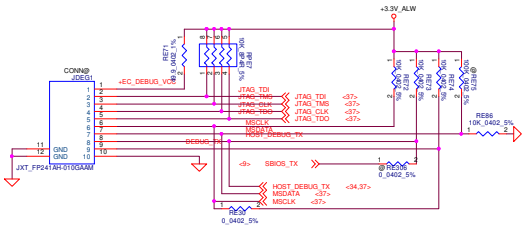
BOARD_ID rise ti me is measured from 5%~68%

PANEL_ID rise ti me is measured from 5%~68%



Link ACES_50278-0040N-001 DONE
20160331



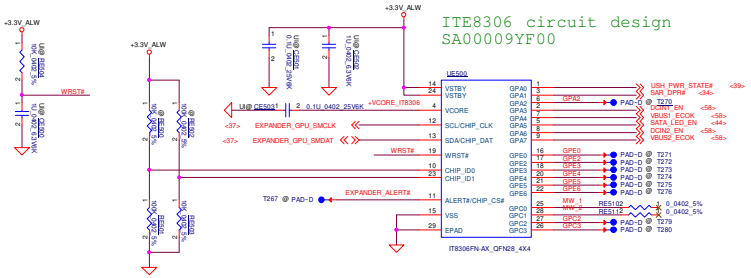


Control Byte

0	1	0	0	A1	A0	R/W

R/W = 0 = Wirte
R/W = 1 = Read

SMBus address 0x40



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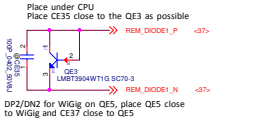
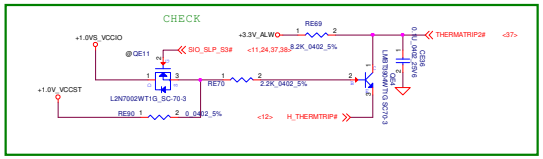
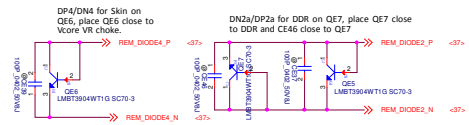
Thermal diode mapping

5085 Channel	Locat i on
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DP2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)







File	MEC5085	
Size	Document Number	Rev 0.1
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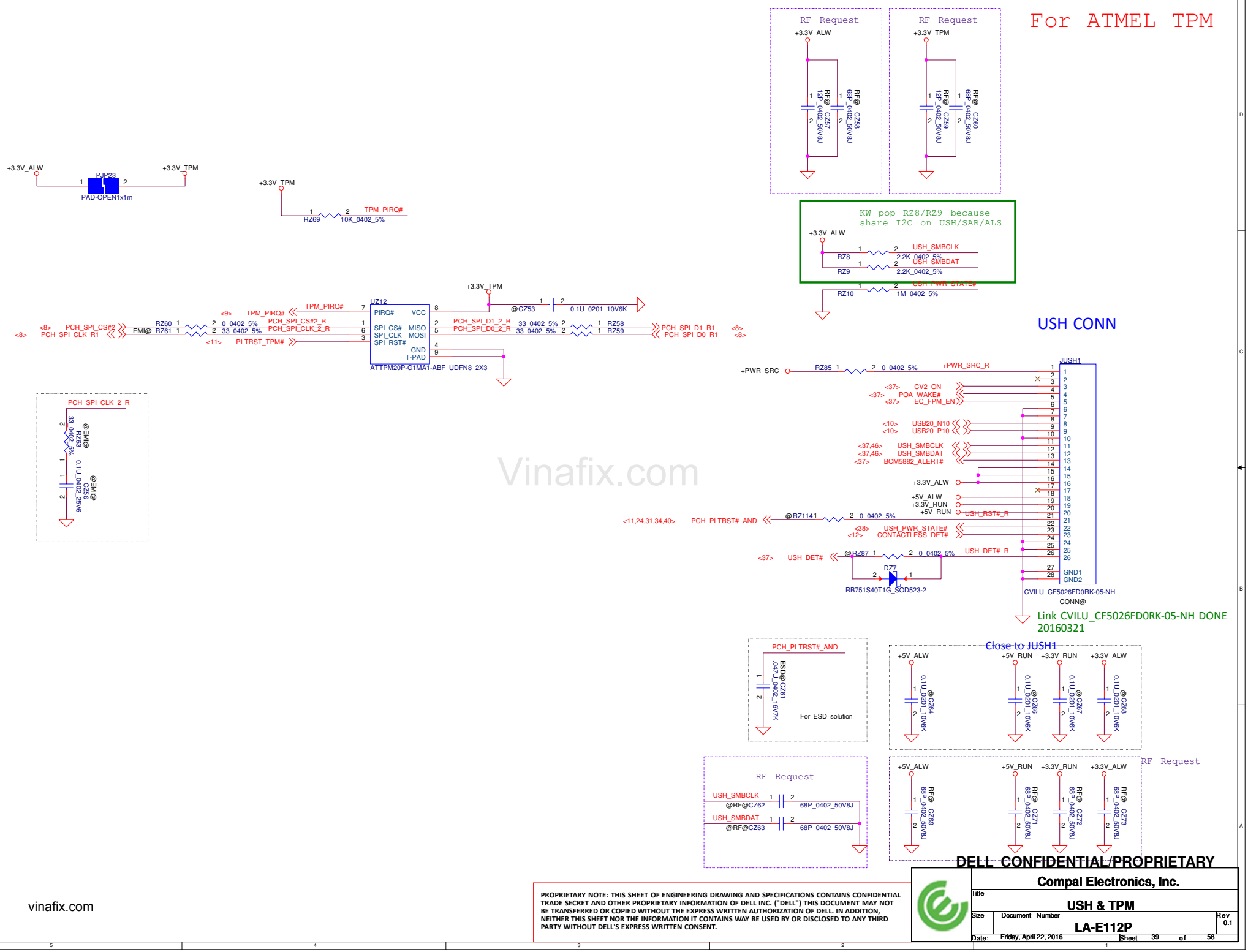
For ATMEL TPM
RF Request
+3.3V_ALW
RF@ 12P_0402_50V8J CZ57
RF@ 68P_0402_50V8J CZ58
RF Request
+3.3V_TPM
RF@ 12P_0402_50V8J CZ59
RF@ 68P_0402_50V8J CZ60
+3.3V_ALW
PJP23
PAD-OPEN1x1m
+3.3V_TPM
+3.3V_TPM
RZ69 10K_0402_5%
TPM_PIRQ#
KW pop RZ8/RZ9 because share I2C on USH/SAR/ALS
+3.3V_ALW
RZ8 2.2K_0402_5% USH_SMBCLK
RZ9 2.2K_0402_5% USH_SMBDAT
RZ10 1M_0402_5% USH_PWR_STATE#
USH CONN
+3.3V_TPM
@CZ53 0.1U_0201_10V6K
UZ12
PIRQ# VCC
SPI_CS# MISO
SPI_CLK MOSI
SPI_RST#
GND
T-PAD
ATTPM20P-G1MA1-ABF_UDFN8_2X3
PCH_SPI_CS#2
PCH_SPI_CLK_R1
RZ60 0_0402_5%
RZ61 33_0402_5%
PCH_SPI_CS#2_R
PCH_SPI_CLK_2_R
PLTRST_TPM#
PCH_SPI_D1_2_R
PCH_SPI_D0_2_R
33_0402_5%
RZ58
RZ59
PCH_SPI_D1_R1
PCH_SPI_D0_R1
PCH_SPI_CLK_2_R
RZ63 33_0402_5% @EM@
CZ56 0.1U_0402_25V6 @EM@
+PWR_SRC
RZ85 0_0402_5%
+PWR_SRC_R
JUSH1
CV2_ON
POA_WAKE#
EC_FPM_EN
USB20_N10
USB20_P10
USH_SMBCLK
USH_SMBDAT
BCM5882_ALERT#
+3.3V_ALW
+5V_ALW
+3.3V_RUN
+5V_RUN
USH_RST#_R
PCH_PLTRST#_AND
@RZ1141 0_0402_5%
USH_PWR_STATE#
CONTACTLESS_DET#
USH_DET#
@RZ87 0_0402_5%
USH_DET#_R
DZ7
RB751S40T1G_SOD523-2
GND1
GND2
CVILU_CF5026FD0RK-05-NH
CONN@
Link CVILU_CF5026FD0RK-05-NH DONE 20160321
Close to JUSH1
PCH_PLTRST#_AND
ESD@ CZ61 .047U_0402_16V7K
For ESD solution
+5V_ALW
+5V_RUN
+3.3V_RUN
+3.3V_ALW
0.1U_0201_10V6K @CZ264
0.1U_0201_10V6K @CZ266
0.1U_0201_10V6K @CZ267
0.1U_0201_10V6K @CZ268
RF Request
USH_SMBCLK
@RF@CZ62
USH_SMBDAT
@RF@CZ63
68P_0402_50V8J
RF@ 68P_0402_50V8J CZ269
RF@ 68P_0402_50V8J CZ271
RF@ 68P_0402_50V8J CZ272
RF@ 68P_0402_50V8J CZ273
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USH & TPM
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For PCIEX4,Kirkwood

RF Request

+3.3V_HDD_M2

@RF@CN60 68P_0402_50V8J

+3.3V_HDD_M2

@CN61 0.1U_0201_10V6K

CN62 0.1U_0201_10V6K

CN63 22U_0603_6.3V6M

CN64 22U_0603_6.3V6M

Place near HDD CONN

2280 SSD

NGFF slot C Key M

Need update! CHECK Kirkwood Port Mapping

+3.3V_HDD_M2 2.5A

PJP31 PAD-OPEN1x2m

+3.3V_RUN

JNGFF3_CONN@

LOTES_YPCI0016-P003A

<10> PCIE_PRX_DTX_N9
<10> PCIE_PRX_DTX_P9
<10> PCIE_PTX_DRX_N9
<10> PCIE_PTX_DRX_P9
<10> PCIE_PRX_DTX_N10
<10> PCIE_PRX_DTX_P10
<10> PCIE_PTX_DRX_N10
<10> PCIE_PTX_DRX_P10
<10> PCIE_PRX_DTX_N11
<10> PCIE_PRX_DTX_P11
<10> PCIE_PTX_DRX_N11
<10> PCIE_PTX_DRX_P11
<10> PCIE_PRX_DTX_P12
<10> PCIE_PRX_DTX_N12
<10> PCIE_PTX_DRX_N12
<10> PCIE_PTX_DRX_P12

CN65 0.22U_0402_10V6K
CN66 0.22U_0402_10V6K
CN67 0.22U_0402_10V6K
CN68 0.22U_0402_10V6K
CN69 0.22U_0402_10V6K
CN70 0.22U_0402_10V6K
CN71 0.22U_0402_10V6K
CN72 0.22U_0402_10V6K

PCIE_PRX_DTX_N9
PCIE_PRX_DTX_P9
PCIE_PTX_C_DRX_N9
PCIE_PTX_C_DRX_P9
PCIE_PRX_DTX_N10
PCIE_PRX_DTX_P10
PCIE_PTX_C_DRX_N10
PCIE_PTX_C_DRX_P10
PCIE_PRX_DTX_N11
PCIE_PRX_DTX_P11
PCIE_PTX_C_DRX_N11
PCIE_PTX_C_DRX_P11
PCIE_PRX_DTX_P12
PCIE_PRX_DTX_N12
PCIE_PTX_C_DRX_N12
PCIE_PTX_C_DRX_P12

<11> CLK_PCIE_N3
<11> CLK_PCIE_P3

NVME_LED# 1 RN100 2 0_0402_5% SATALED# <10,34,44>

M2_DEVSLP <10>

PCH_PLTRST#_AND <11,24,31,34,39>
CLKREQ_PCIE#3 <11>
PCIE_WAKE# PCIE_WAKE# <24,34,38>

SUSCLK_R 1 RN99 2 0_0402_5% SUSCLK <11,34>

<10> m2280_PCIE_SATA#

GND GND

+3.3V_HDD_M2

M2_DEVSLP 1 @RN37 2 10K_0402_5%

if signal is PCIE GEN3/SATA GEN3 maybe change C value or no need for DG0.9 SATA EXPRESS HDD

Link LOTES_YPCI0016-P003A Done (Key M)
20160315

Compal Electronics, Inc.

Title: M2 2280 Socket

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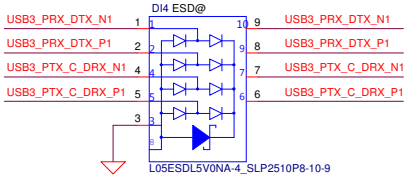
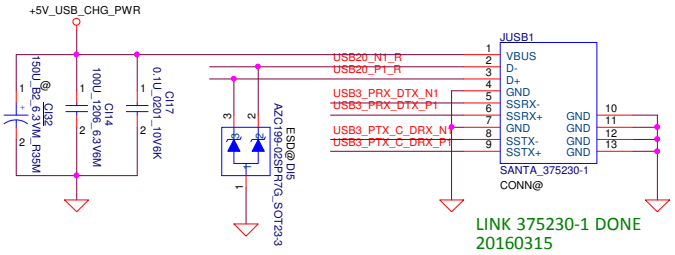
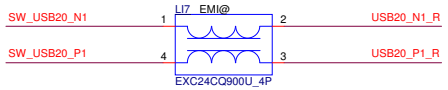
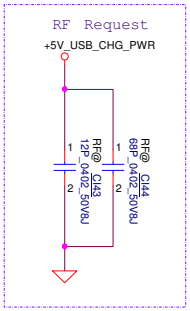
For PWR SW + Charger combine IC

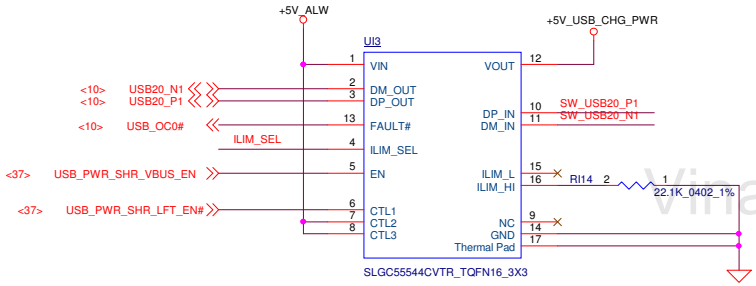


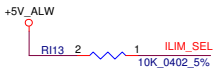


LINK 375230-1 DONE
20160315

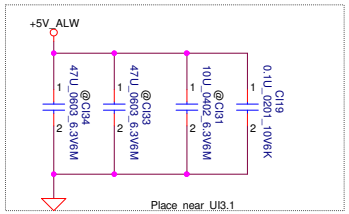








CIS Link Seligro SA000097E10 20160304
MAIN:SLGC55544CVTR



Compal Electronics, Inc.	
Title	JUSB1+PS
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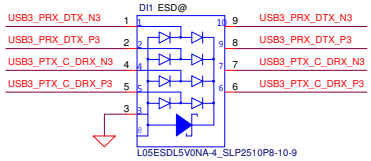
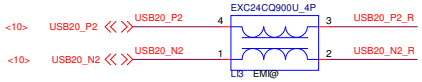
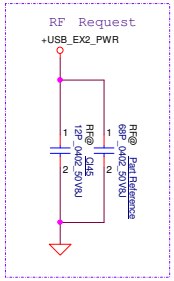
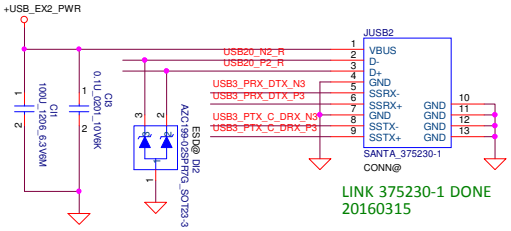


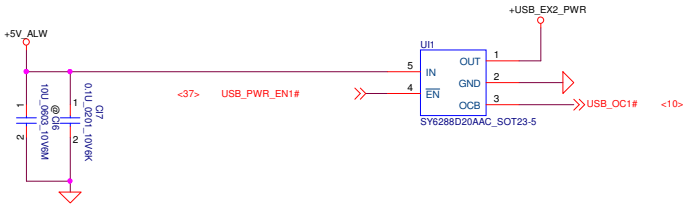


DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm





LINK 375230-1 DONE
20160315



Compal Electronics, Inc.		
Title: JUSB2		
Size	Document Number: LA-E112P	Rev: 0.1
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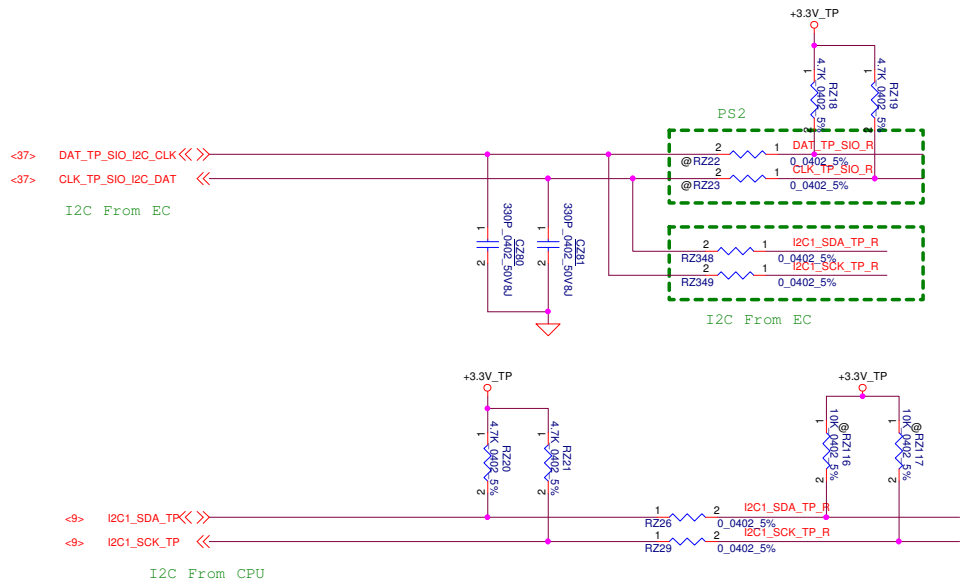
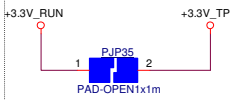
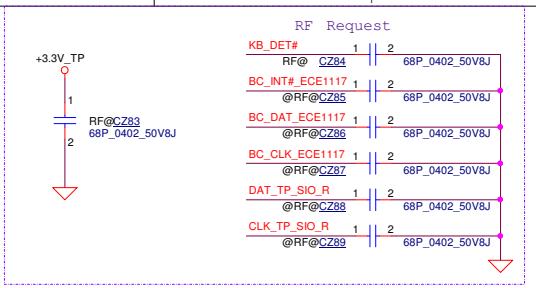
Touch Pad

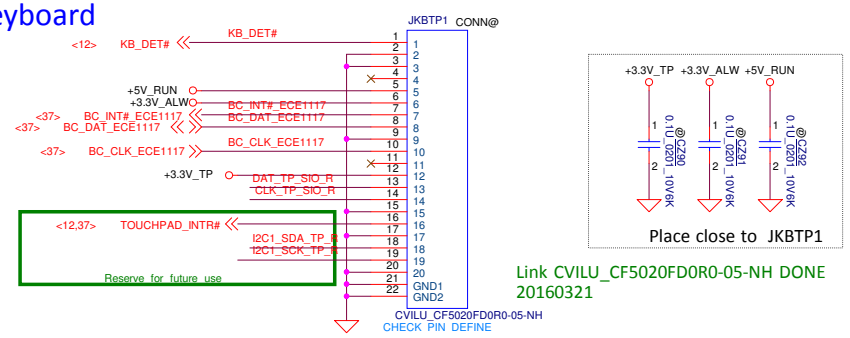


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



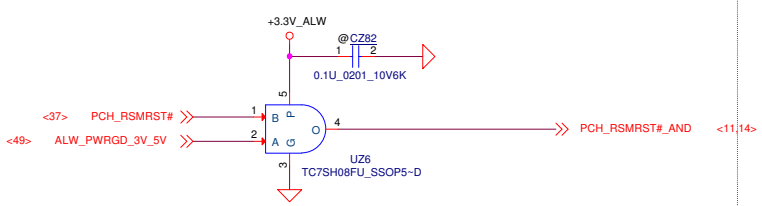


Keyboard



Link CVILU_CF5020FD0R0-05-NH DONE
20160321

RSMRST circuit



@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK 2JX 2.0W 4 OHM FG

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Compal Electronics, Inc.	
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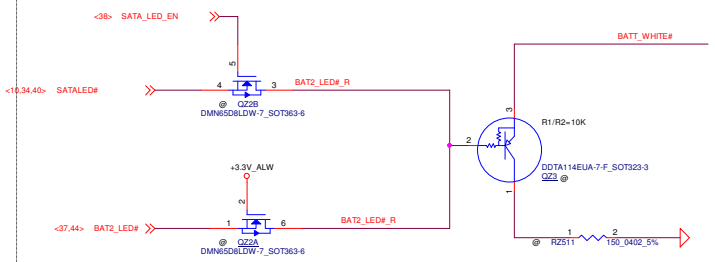
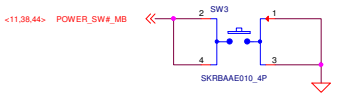
HDD LED MUX

means EC can switch battery white led and HDD LED by hot key " Fn+H"



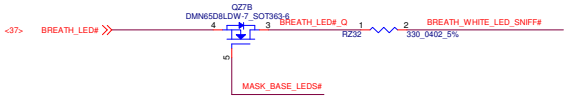
Bat t ery LED

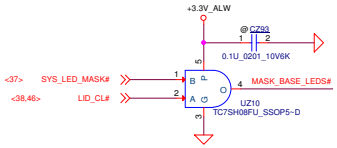
POWER & INSTANT ON SWITCH For NPI USE



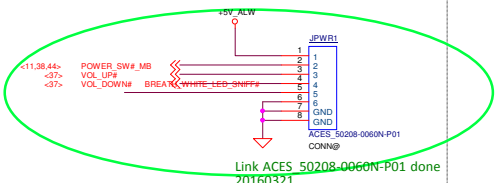
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00



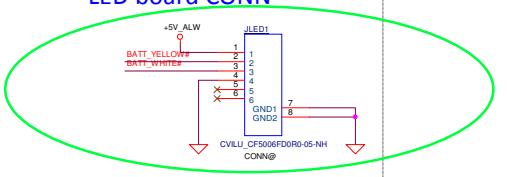


PWR board CONN



Link ACES_50208-0060N-P01 done
20160321

LED board CONN



Link CVILU_CF5006FD0R0-05-NH done
20160325

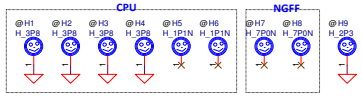
Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

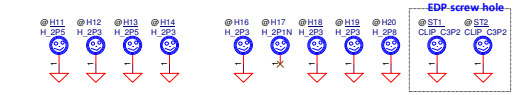
LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

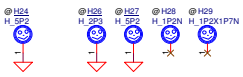
CPU



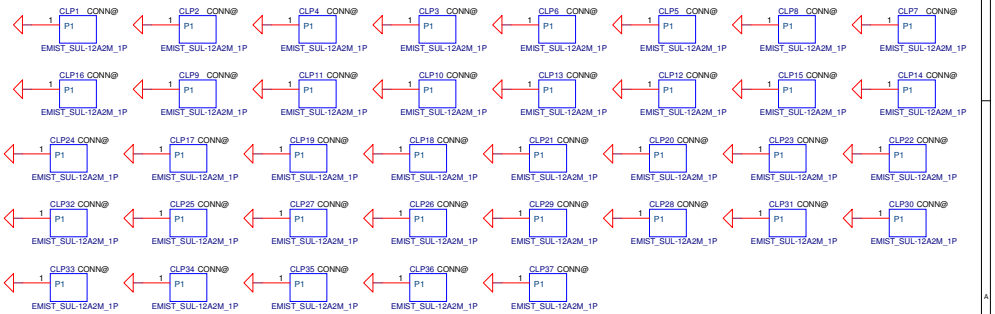
NGFF



EDP screw hole



For JAE JSIM1 boss hole



Compal Electronics, Inc.

Title: PAD, LED

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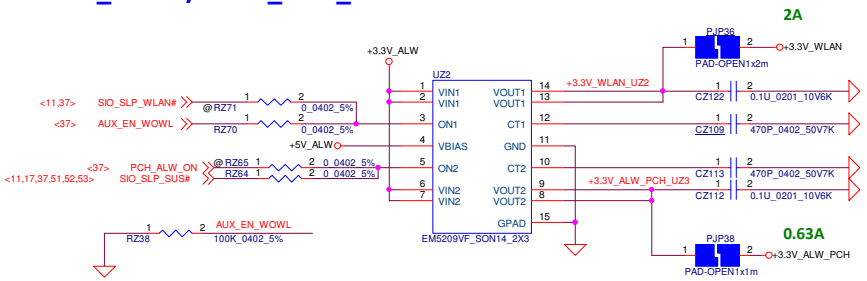
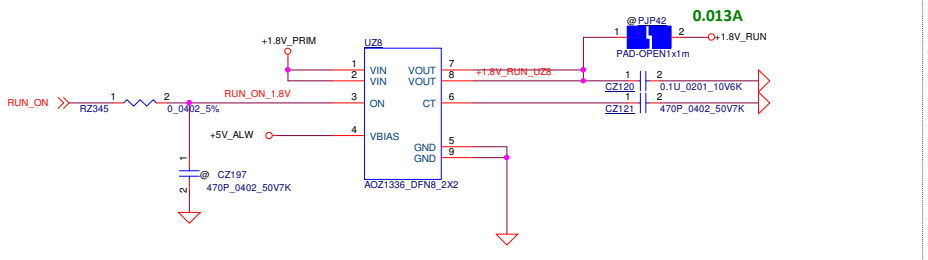
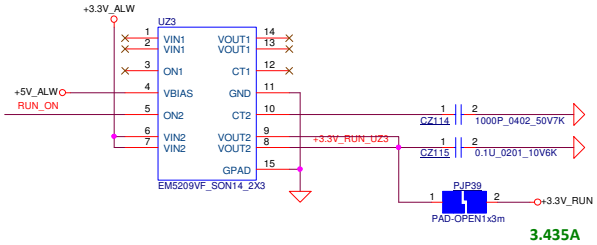
+3.3V_WLAN/+3.3V_ALW_PCH source



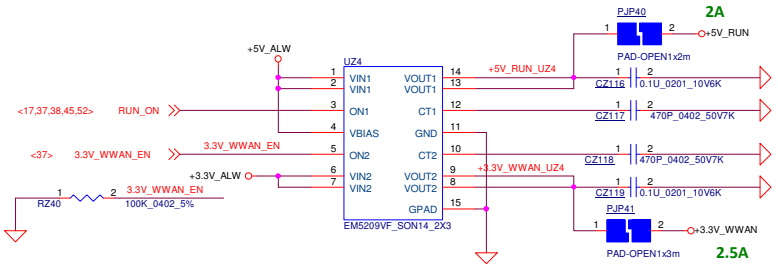
+1.8V_RUN source

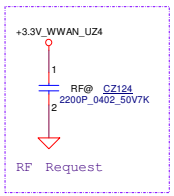


+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source





Compal Electronics, Inc.

Title: Power control

Size | Document Number: LA-E112P | Rev: 0.1

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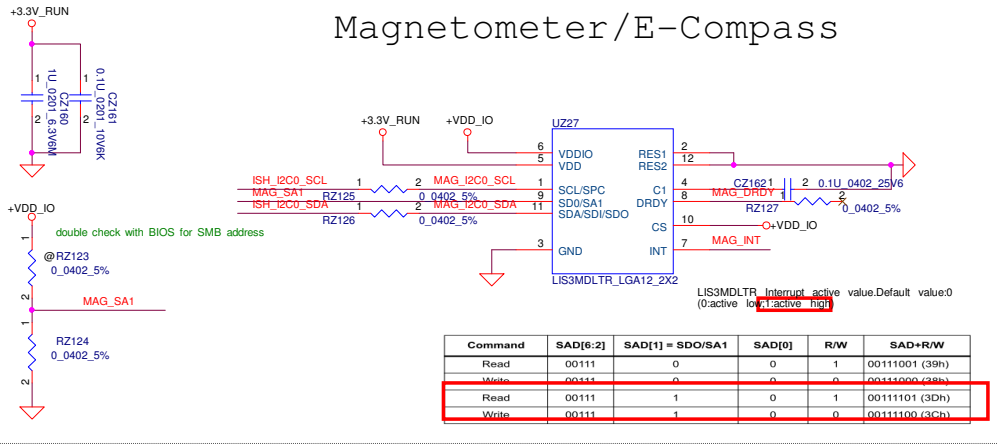
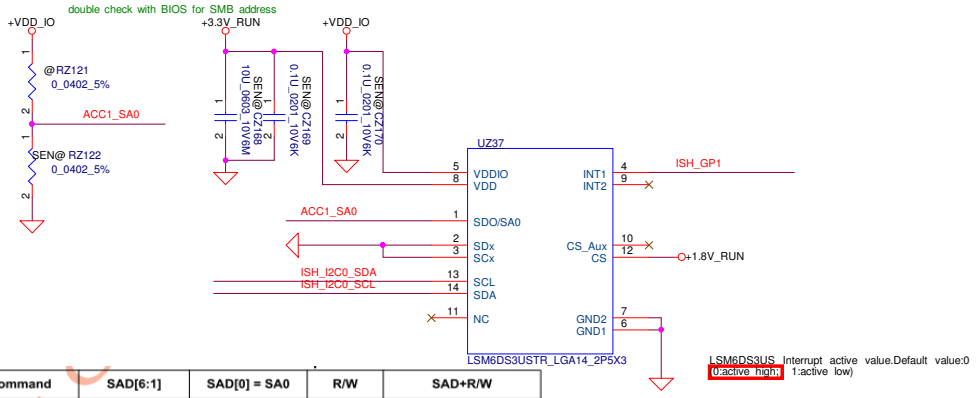
Only for Kirkwood

Magnetometer/E-Compass



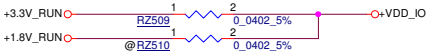
Command	SAD[6:2]	SAD[1] = SDO/SA1	SAD[0]	R/W	SAD+R/W
Read	00111	0	0	1	00111001 (39h)
Write	00111	0	0	0	00111000 (38h)
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)

3D accelerometer and Gyro sensor

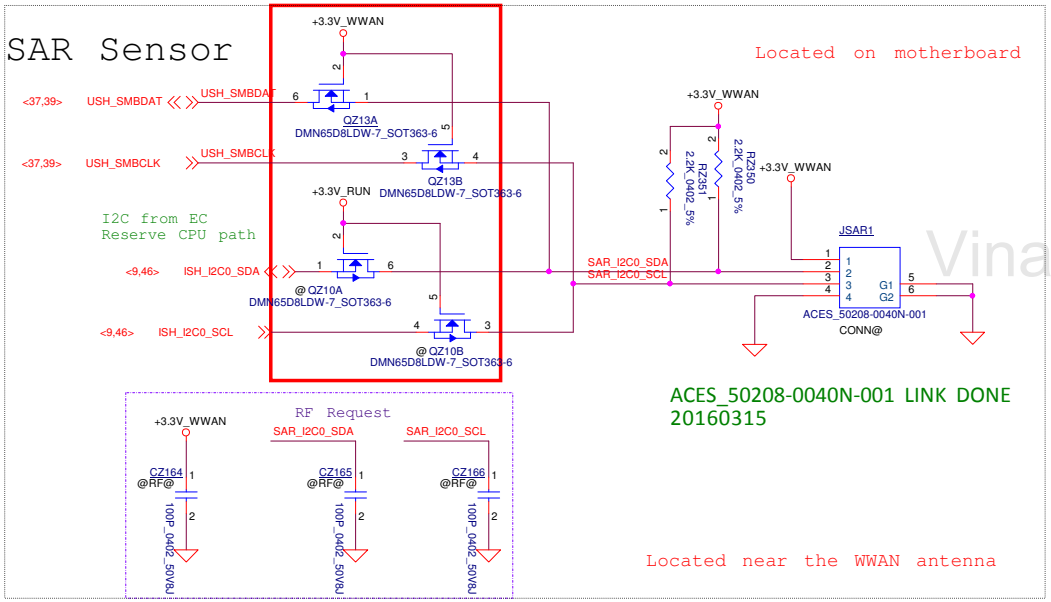


Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Located on MB



SAR Sensor

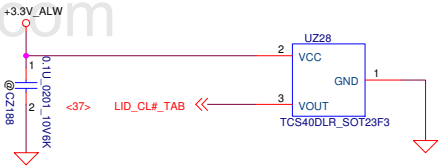


Located on motherboard

ACES_50208-0040N-001 LINK DONE
20160315

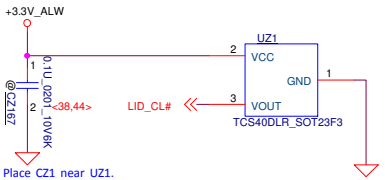
Located near the WWAN antenna

Detect closed in tablet position



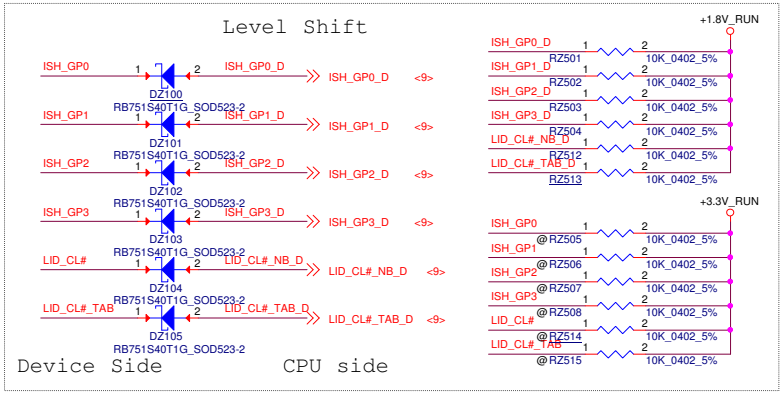
Hall sensor: SA00009CB00

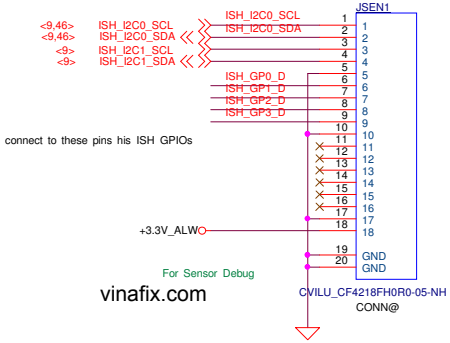
Detect clamshell closed

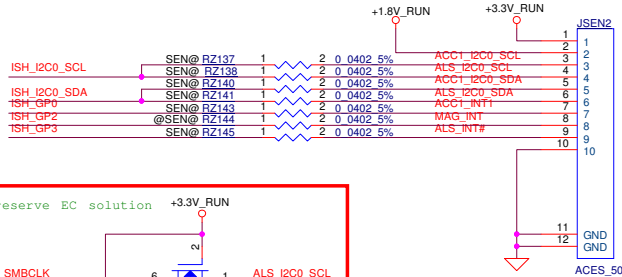


Hall sensor: SA00009CB00

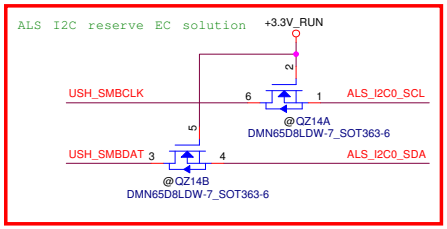
Level Shift







LINK ACES_50208-01001-P03 Done
20160321



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Compal Electronics, Inc.

Title: SENSOR

Size | Document Number: LA-E112P | Rev: 0.1

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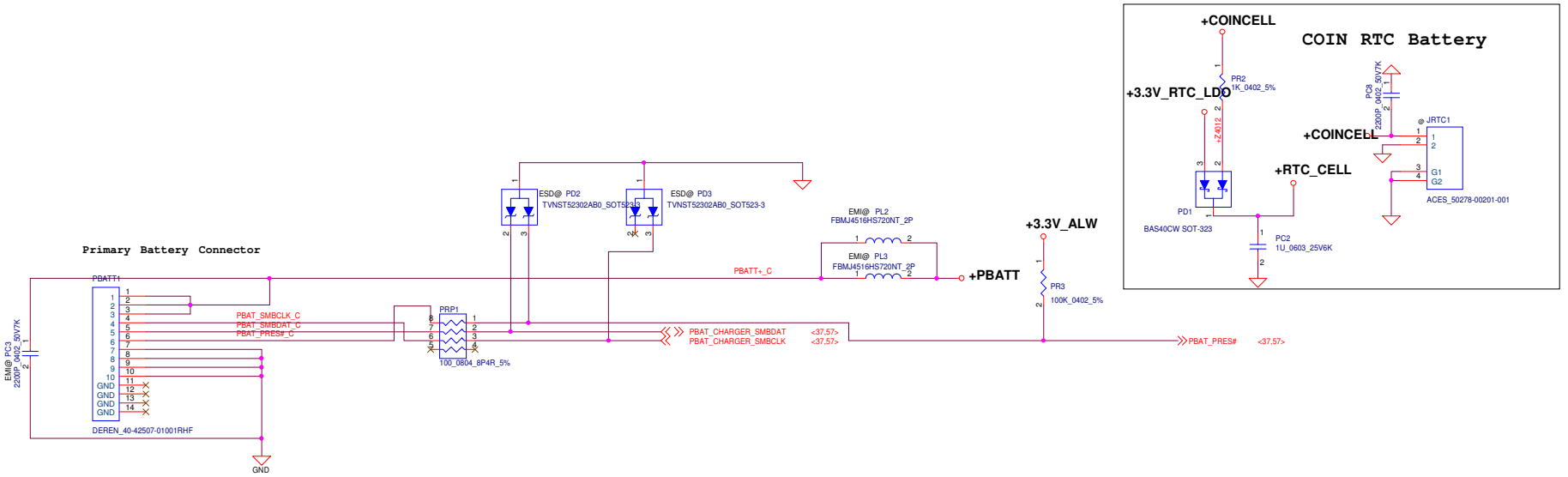

Compal Electronics, Inc.

Title: +DCIN

Size | Document Number: LA-E112P | Rev: 0.1

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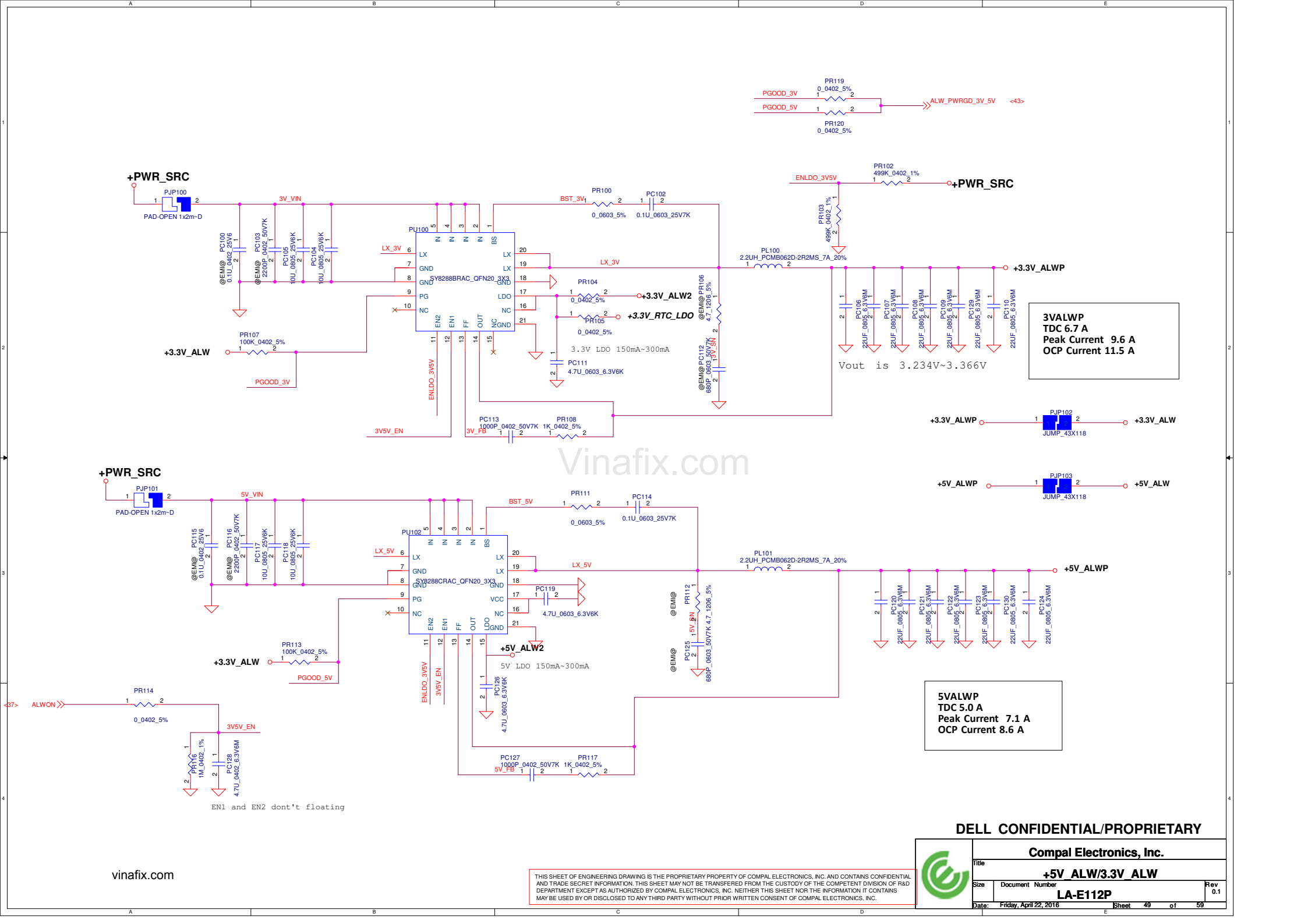

Compal Electronics, Inc.	
Title	+5V_ALW/3.3V_ALW
Size	Document Number: LA-E112P
Rev	0.1
Date:	Friday, April 22, 2016
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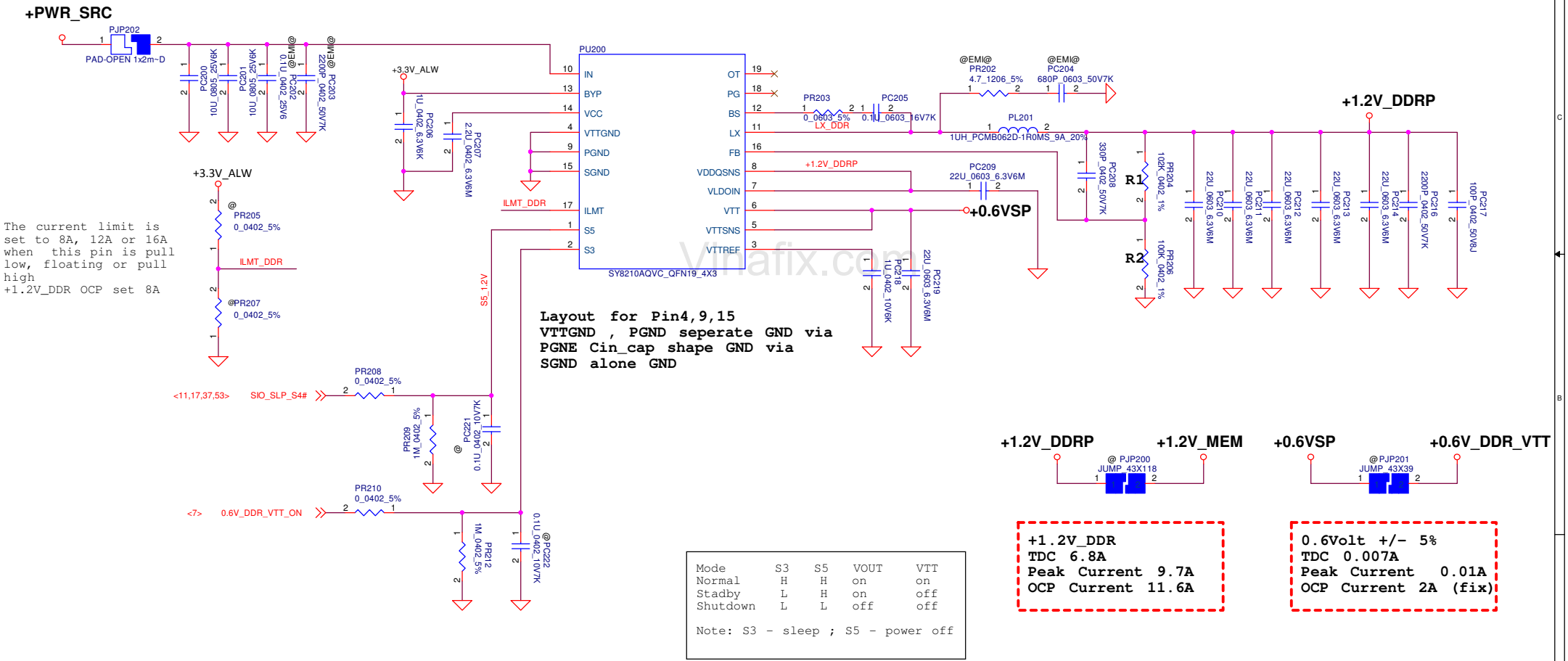

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Compal Electronics, Inc.	
Title	+1.2V_MEN/+0.6V_DDR_VTT
Size	Document Number: LA-E112P
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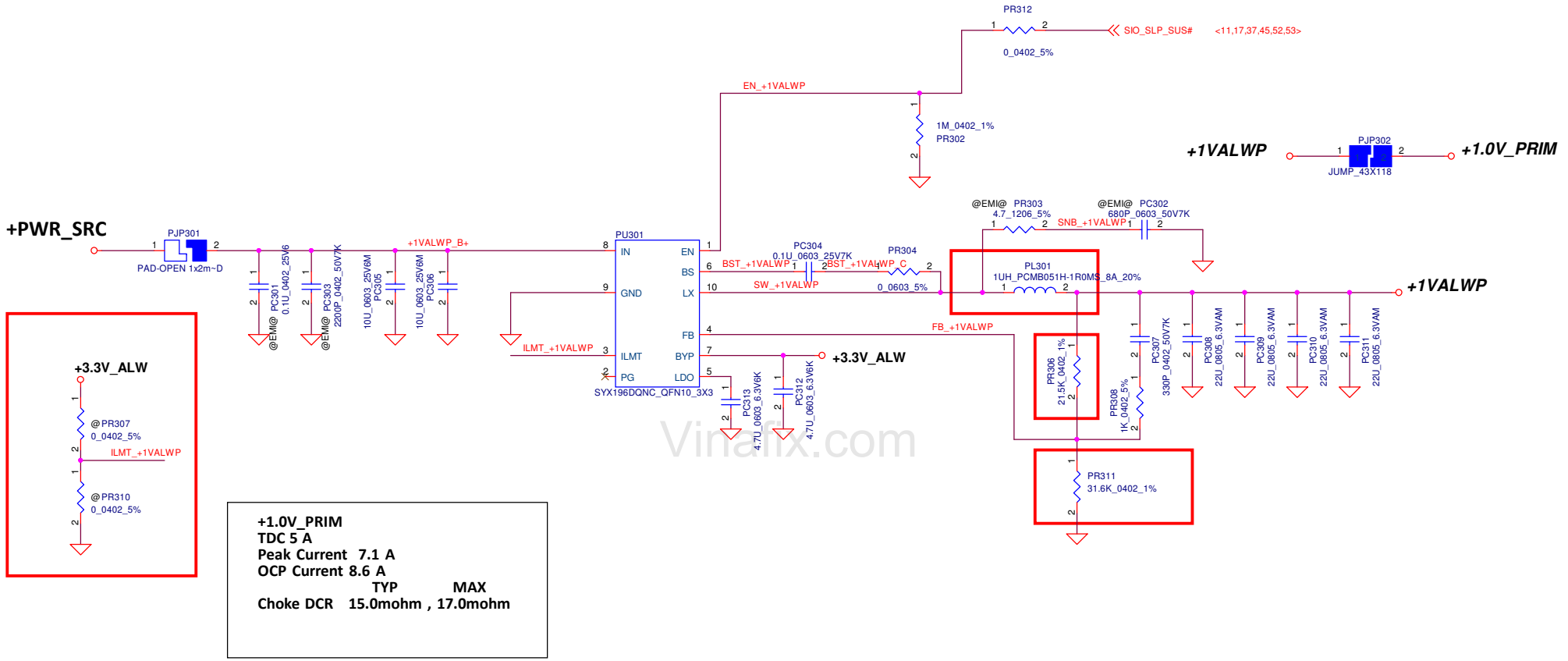

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

Compal Electronics, Inc.

Title: +1VALWP

Size | Document Number: LA-E112P | Rev: 0.1

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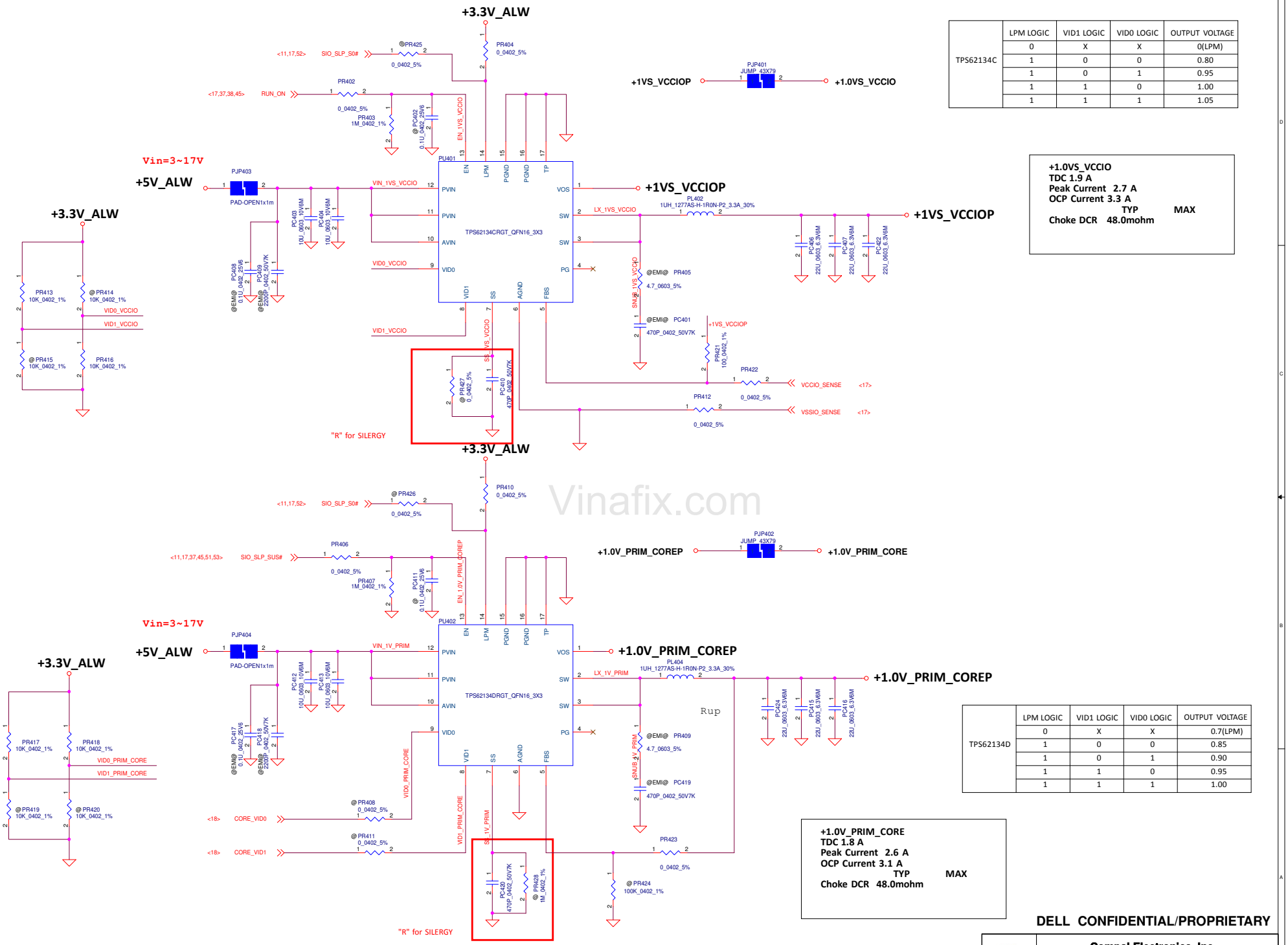


TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A
TYP MAX
Choke DCR 48.0mohm

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

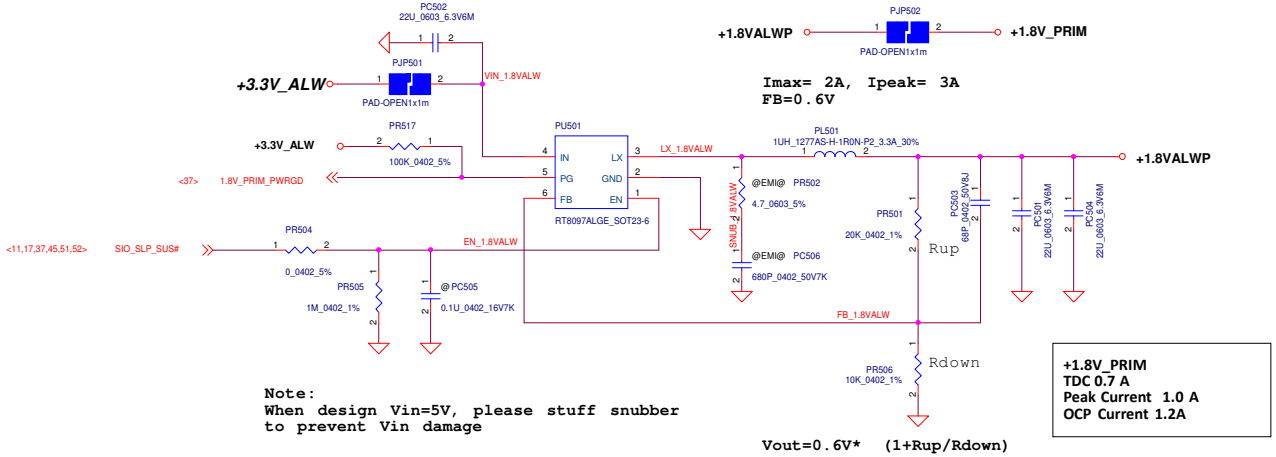
+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A
TYP MAX
Choke DCR 48.0mohm

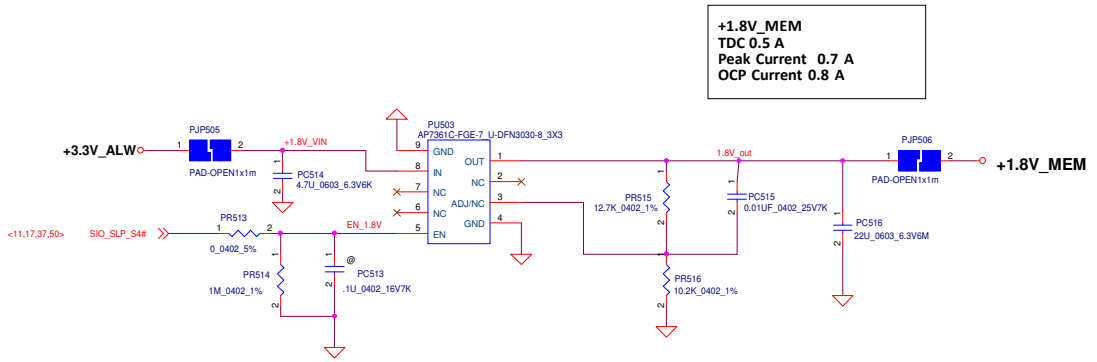
Compal Electronics, Inc.

Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

Size: | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 52 of 59



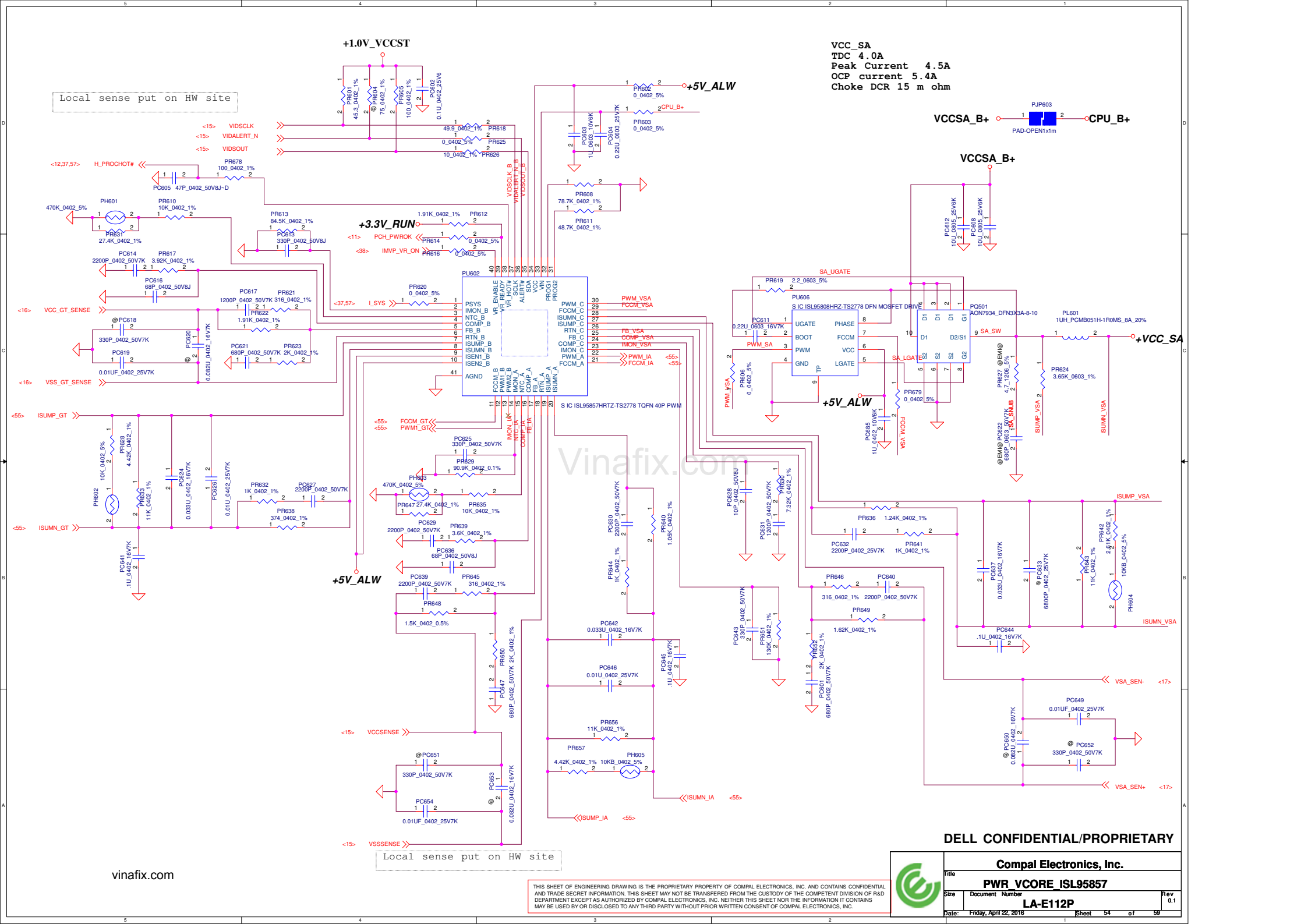


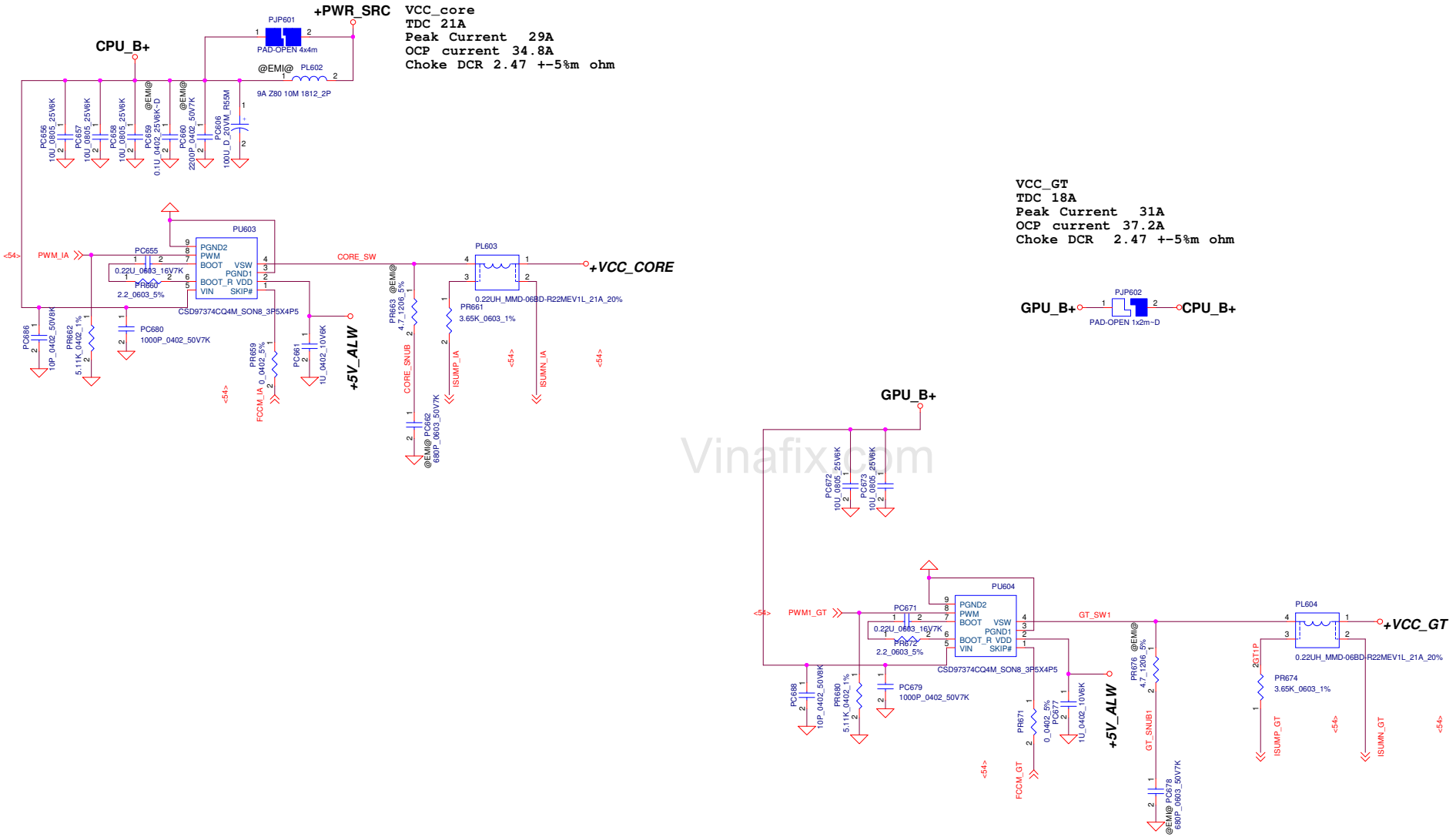
Compal Electronics, Inc.

Title: +1.8VALWP/1.8V_MEN

Size | Document Number: LA-E112P | Rev: 0.1

Date: Friday, April 22, 2016 | Sheet 53 of 59





Compal Electronics, Inc.

Title: PWR_VCORE_ISL95857

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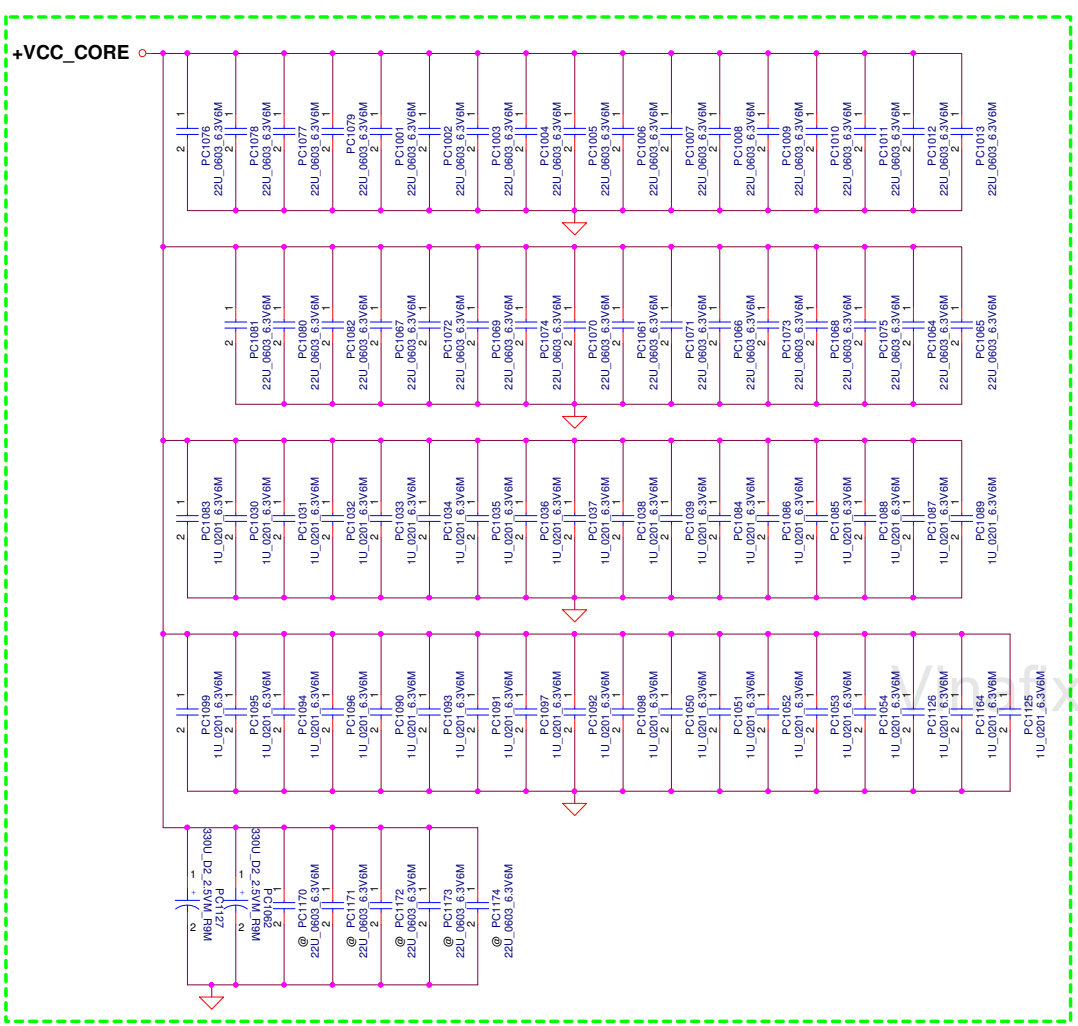
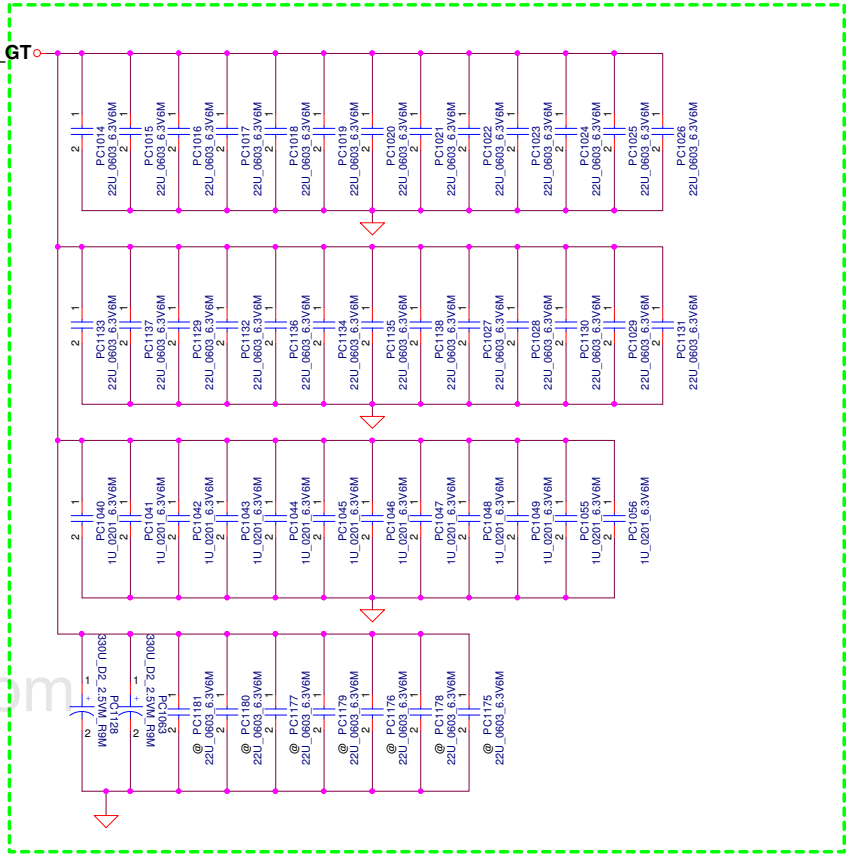
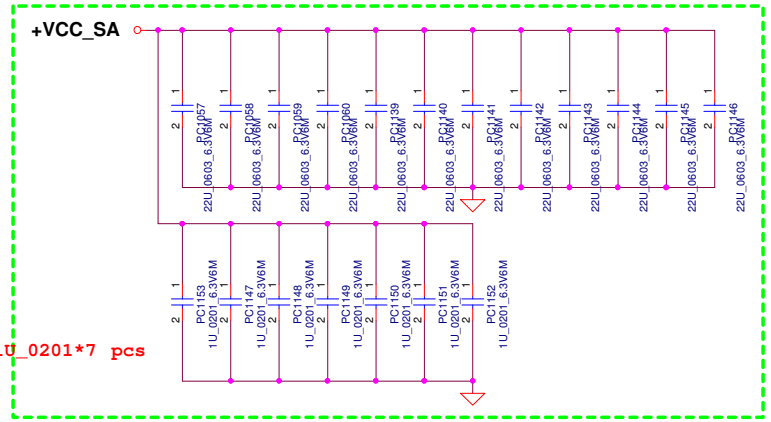
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U23E)
22U_0603 * 48 pcs +1U_0201*12 pcs
+330u_D2*3 pcs







VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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Compal Electronics, Inc.	
Title	PROCESSOR DECOUPLING
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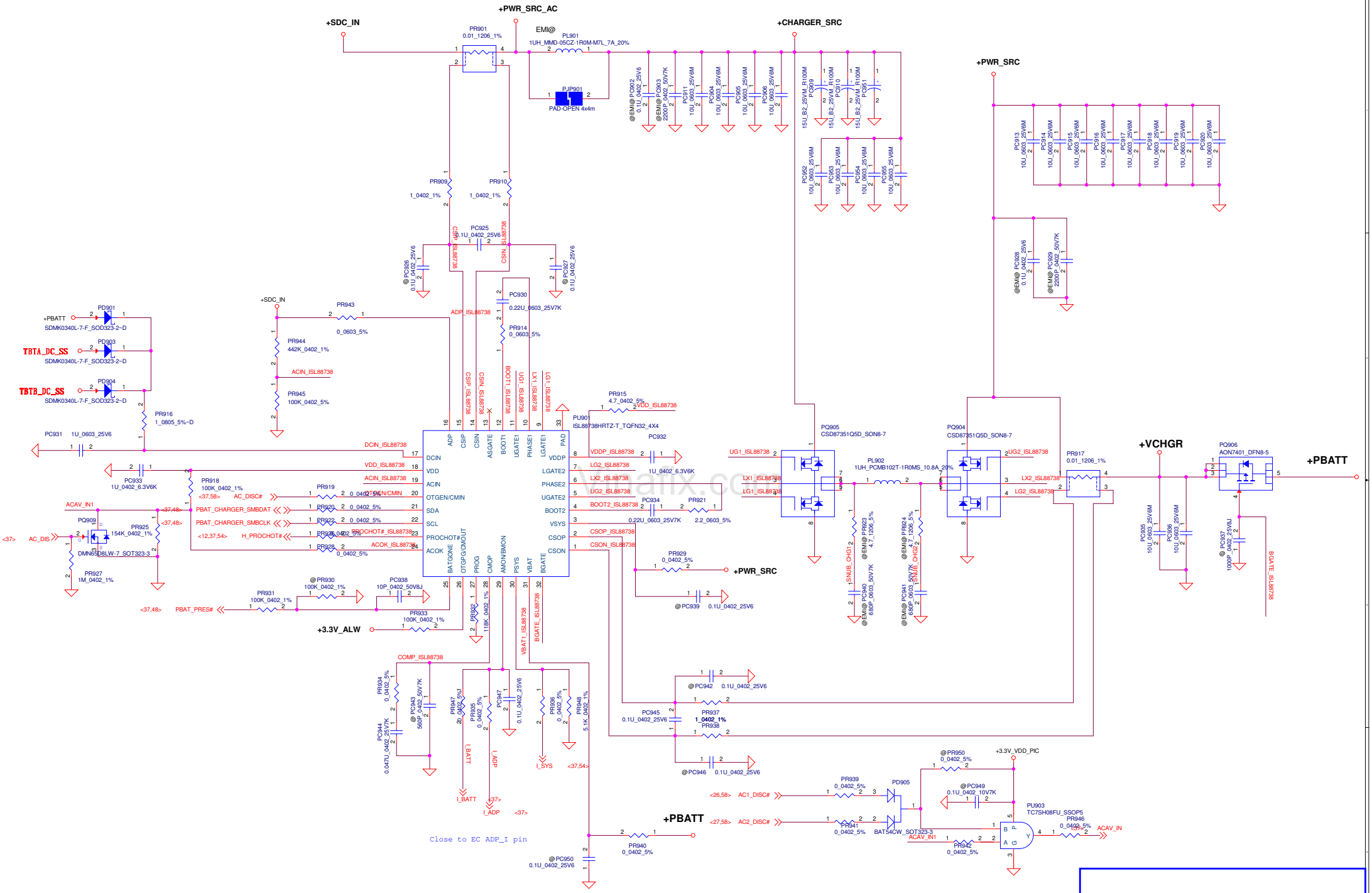

Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/08/31

Compal Electronics, Inc.

Title: **P47-PWR_CHARGER_ISL9237 (Colay)**

Size: | Document Number: **LA-E112P** | Rev: 0.1

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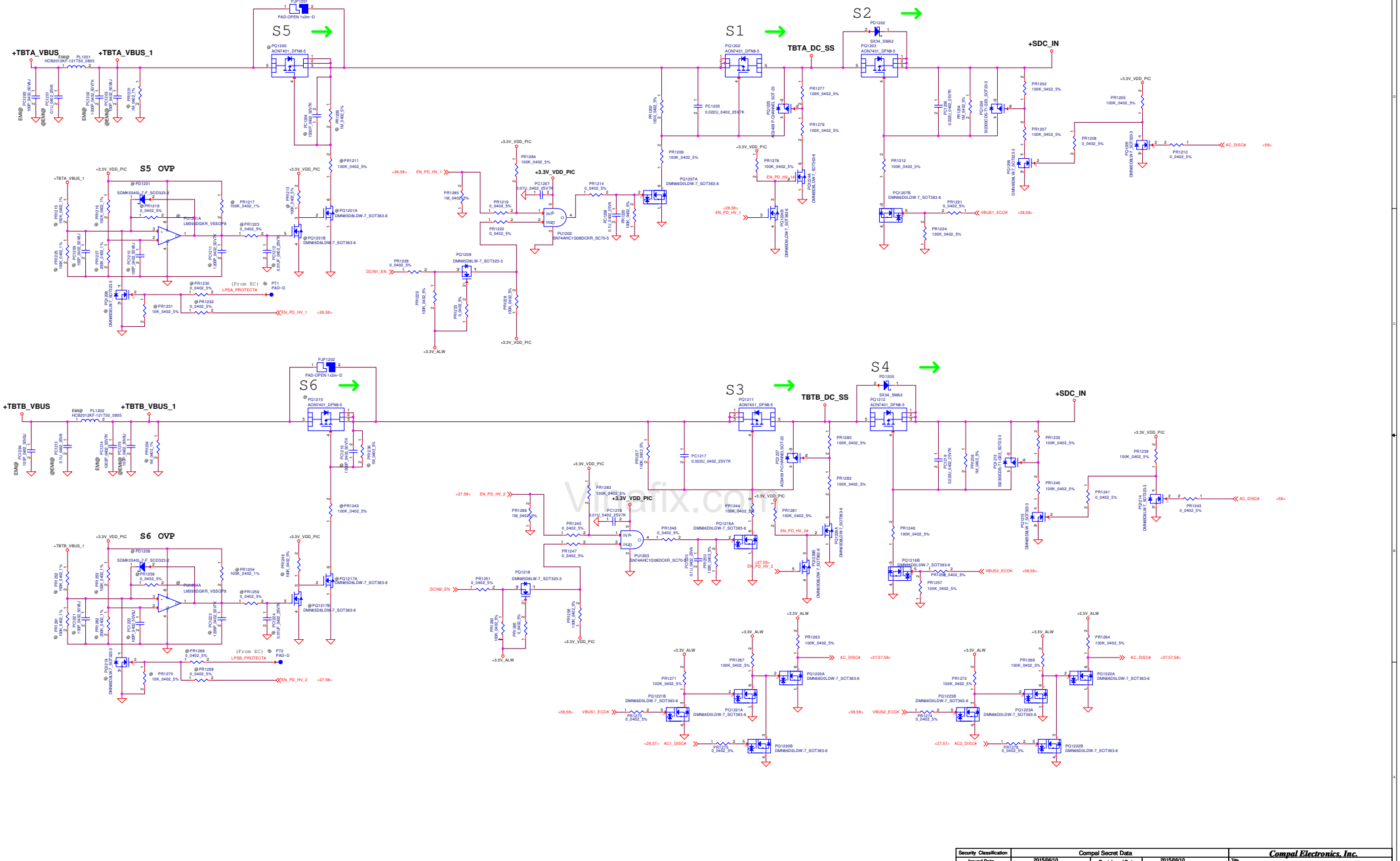

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/06/10	Deciphered Date	2015/06/10
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			Size: Document Number: LA-E112P Rev: 0.1
			Date: Friday, April 22, 2016 Sheet 58 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	New add 1.2V_RUN (From 3.3V_RUN) by use power regulator SW ,only for HDMI PS8407 EE request	modify power rail PU502, change PR508 from 8.87K to 5.1K	X00
2	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	For LPDDR3 power , add +1.8v_MEM	modify power rail PU503, change PR515 from 21.5K to 12.7K	X00
3	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 02/23	Compal	PU501 PG connect to +1.8V_RPIM_PWRGD & Pull high to 3.3V	modify power rail PU501, pull high to 3.3V and connect netname +1.8V_PRIM_PWRGD	X00
4	55	1.8VALW/+1.2V/ 1.8V_MEN	2016 03/01	Compal	HW dropped PS8407 solution.	Remove 1.2V_RUN (PU502) power rail.	X00
5	52	+1.2V_MEM/ +0.6V_DDR	2016 03/07	Compal	remove 1.2V_DDR_PG	remove 1.2V_DDR_PG,remove PR201	X00
6	60	1Type-C PD Selector	2016 03/17	Compal	to add S4 quick turn off 3/14 by chris	add PQ1224 PQ1225 PQ1226 PQ1227	X00
7	60	1Type-C PD Selector	2016 03/23	Compal	EMI requiest	add PR1283 PR1284	X00
8							
9							
10							
11							
12							
13							
14							

Compal Electronics, Inc.

Title: PWR P.I.R

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