Compal Confidential

YOGA 730 13.3"
UMA M/B Schematics Document

Intel Whiskeylake Processor with DDR4 Memory Down

Only UMA Design

2018-02-02

LA-G581P

REV:0.2

Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.		
Title	*Cover Page*	
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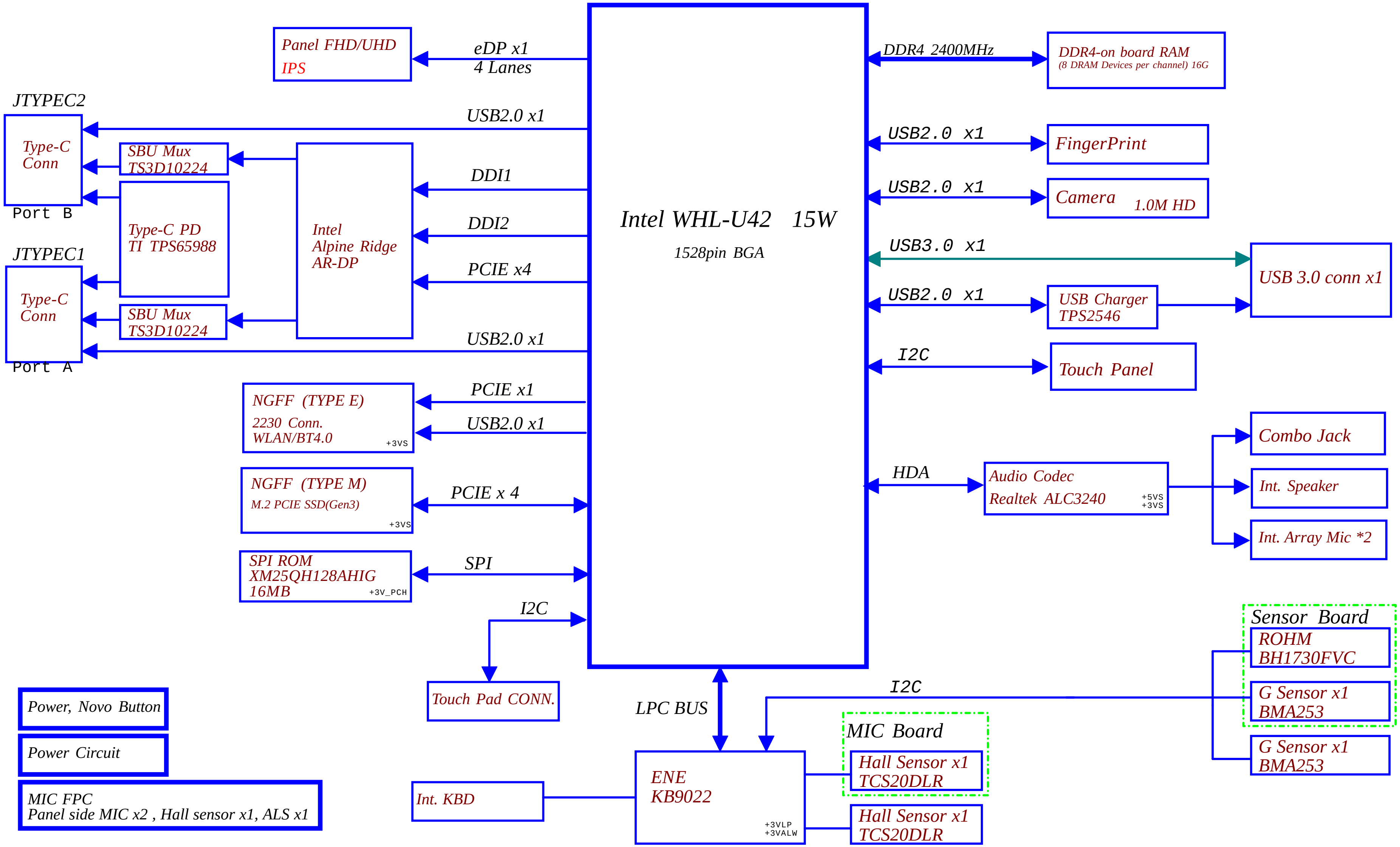
Compal Confidential
Pluto 3A (13")

Whiskeylake U4+2



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Issued Date	2018/02/06	Deciphered Date	2020/5/17	Title: BLOCK DIAGRAM		
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Voltage Rails

power plane / State	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +1.05VS_VCCOPC +VCCCORE +VCCGT +1.05V_VCCST +1.05VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
EMI part	EMI@
EMI unpop	@EMI@
ESD part	ESD@
ESD unpop	@ESD@
RF part	RF@
RF unpop	@RF@
Connector	ME@
Test Point	TP@
Thunderbolt	TBT@
Non Keyboard backlight	NOKBL@
Keyboard backlight	KBL@
For Intel DCI debug	DCI@
For thermal sensor	EX_THM@
For 4G, 8G DARM	SDP@
For 16G DARM	DDP@
For 12G DARM	DDP_SDP@
For DARM X76	X76RAM@
For SSD DET	SSD_DET@

ZZZ1 @ BARCODE_8X8

ZZZ2 @ BARCODE_12X4

ZZZ3 @ BARCODE_20X4

ZZZ4 @ BARCODE_10X10

DDR4 Onboard RAM

	DDR4 Onboard RAM		
4G	ZZZ8 @ DDR4-Samsung 4G X7676238LC7	ZZZ14 @ DDR4-Hynix 4G X7676238LC9	ZZZ23 @ DDR4-Micron 4G X7676238LC8
8G	ZZZ15 @ DDR4-Samsung 8G X7676238LC4	ZZZ16 @ DDR4-Hynix 8G X7676238LC6	ZZZ17 @ DDR4-Micron 8G X7676238LC5
16G	ZZZ19 @ DDR4-Hynix 16G(2400) X7676238LC3`		
16G	ZZZ18 @ DDR4-Samsung 16G X7676238LC1		ZZZ20 @ DDR4-Micron 16G X7676238LC2

ZZZ21 DA8001FT000 PCB 279 LA-G581P REV0 M/B

ZZZ22 <BOM Structure> X4EADG38L01

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
GPU	1001 111x 9Eh

PCH SM Bus address

Device	Address
Touch Pad	

SMBUS Control Table

	SOURCE	PD	BATT	CHARGER	TP	PCH
EC_SMB_CK1 EC_SMB_DA1	NPCE388 +3VALW	V +3VALW	V +3VALW	V +19V_VIN	X	X
EC_SMB_CK2 EC_SMB_DA2	NPCE388 +3VS	X	X	X	X	V +3VS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VS	X	X	X	V +3VS	X

USB 2.0 Port Table

Port	
1	
2	USB2/3 (Charger)
3	USB2 (Type-C) (JTYPEC1)
4	USB2 (Type-C) (JTYPEC2)
5	Camera
6	Finger print
7	NGFF WLAN+BT
8	

USB 3.0 Port Table

Port	
1	
2	USB2/3(charge)
3	
4	
5	
6	

PCIE Port Table

Port	Lane	
1	1	
2	2	
3	3	
4	4	
5	0	Thunderbolt
6	1	
7	2	
8	3	
9	1	NGFF WLAN+BT
10	2	
11	3	
12	4	
13	3	SSD
14	2	
15	1	
16	0	

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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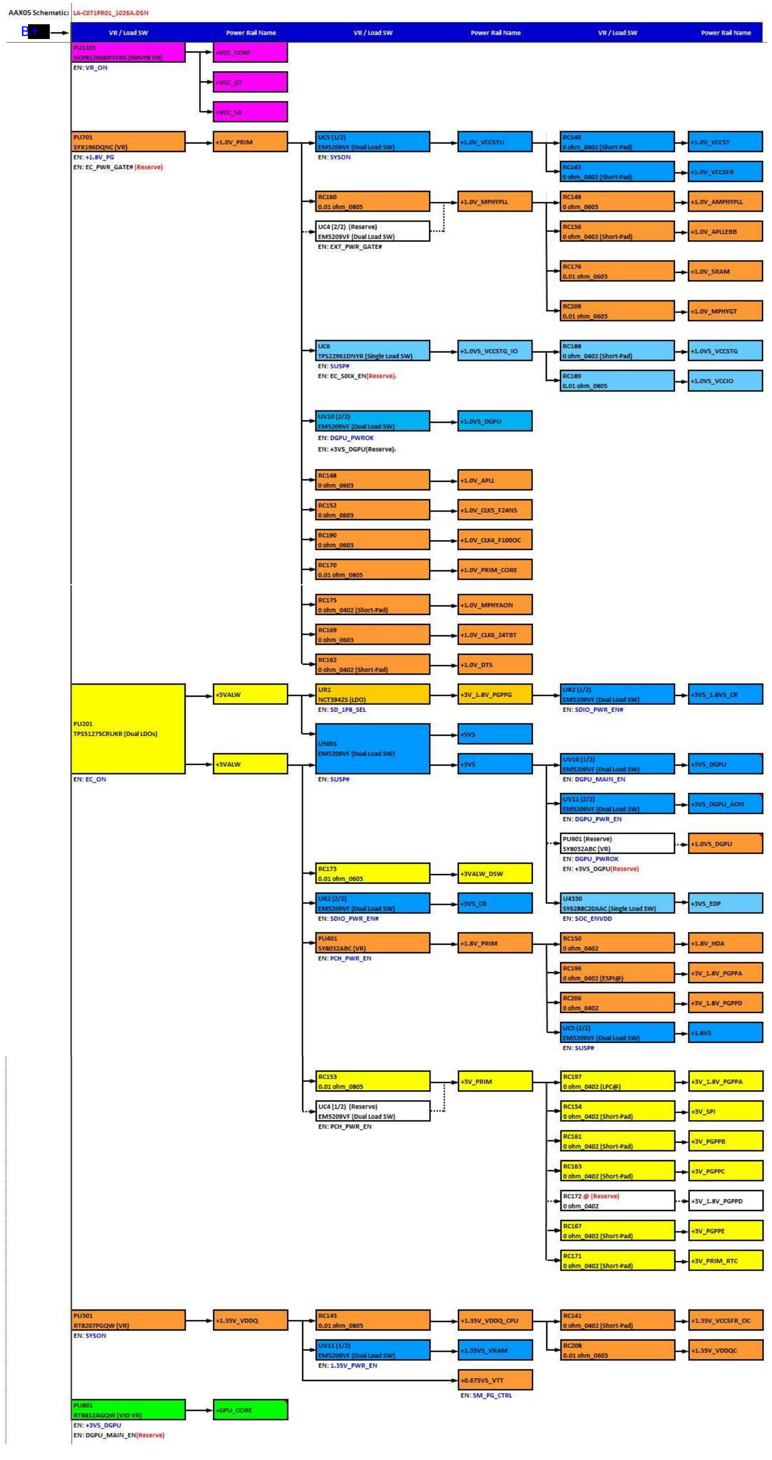
Title: Notes List

Size: C Document Number: LA-G581P Rev: 0.1

ELZP3 -PowerMap_WHL-U_DDR4_Volume_NON CS]



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[ELZP3-PWR Sequence_WHL-U42_DDR4_Volume_NON CS]

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Title: ***Power Sequence***

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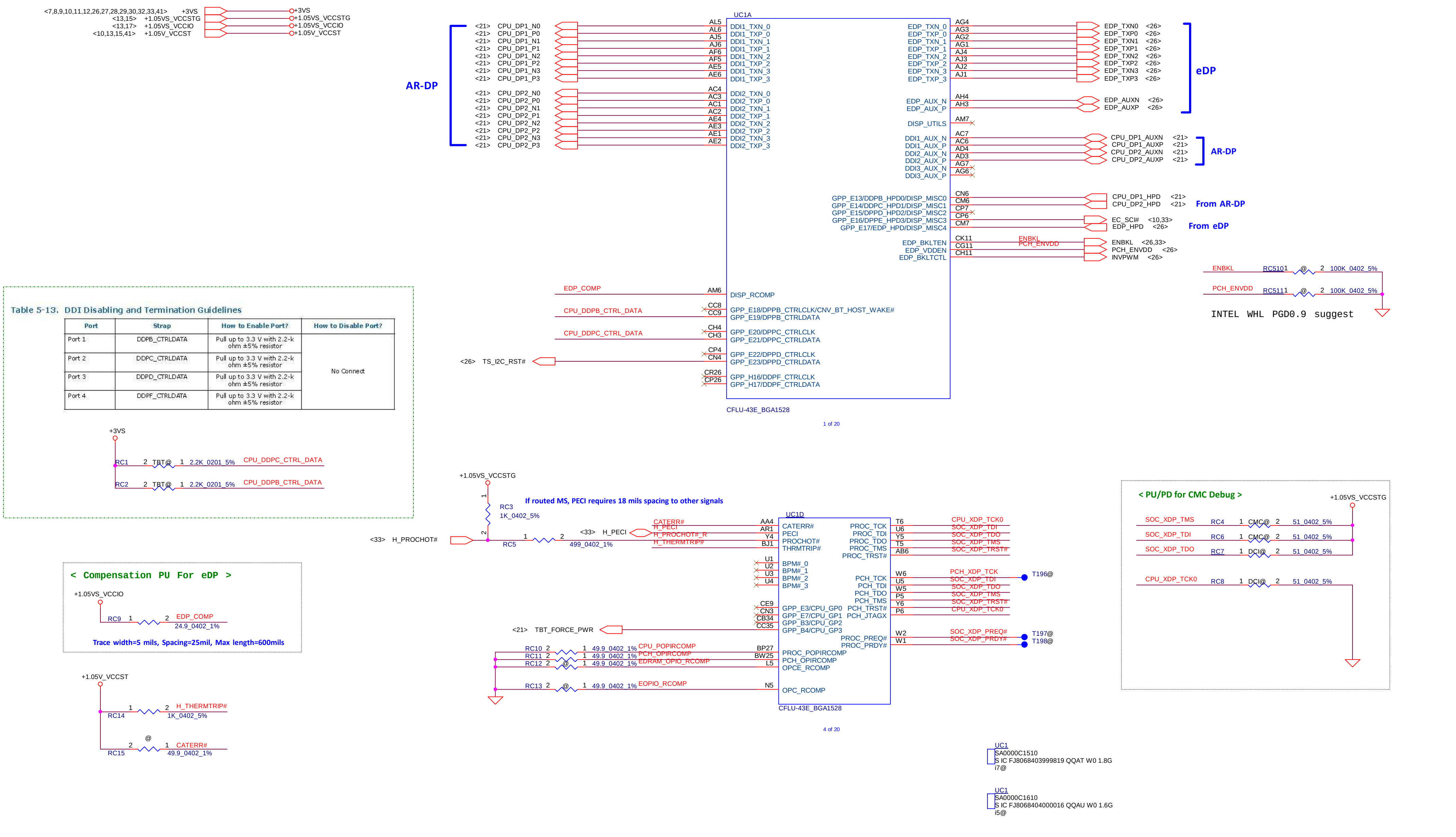

Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

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Title: **WHL-U(1/12)DDI,EDP,MISC,CMC**

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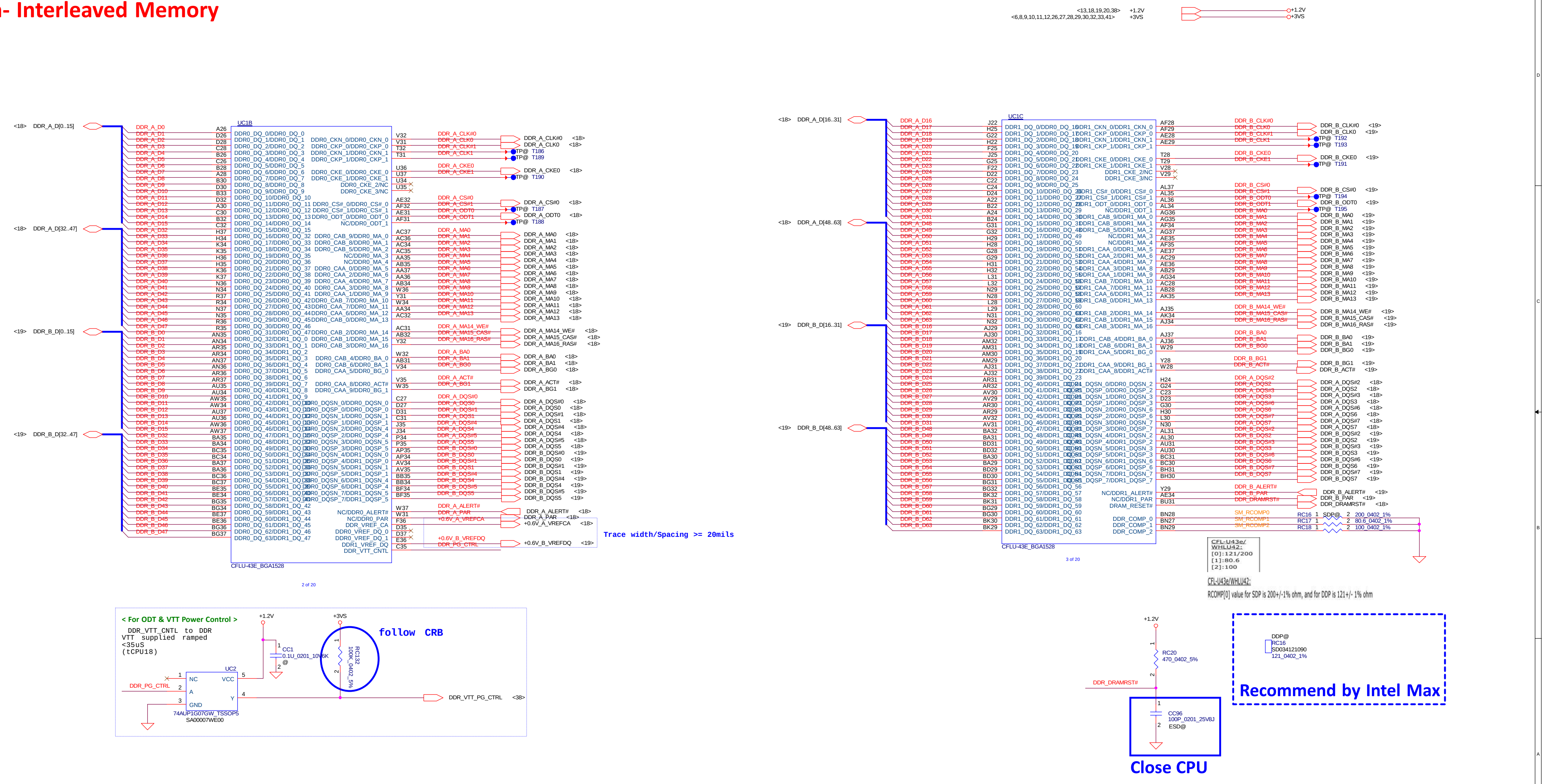
Non- Interleaved Memory



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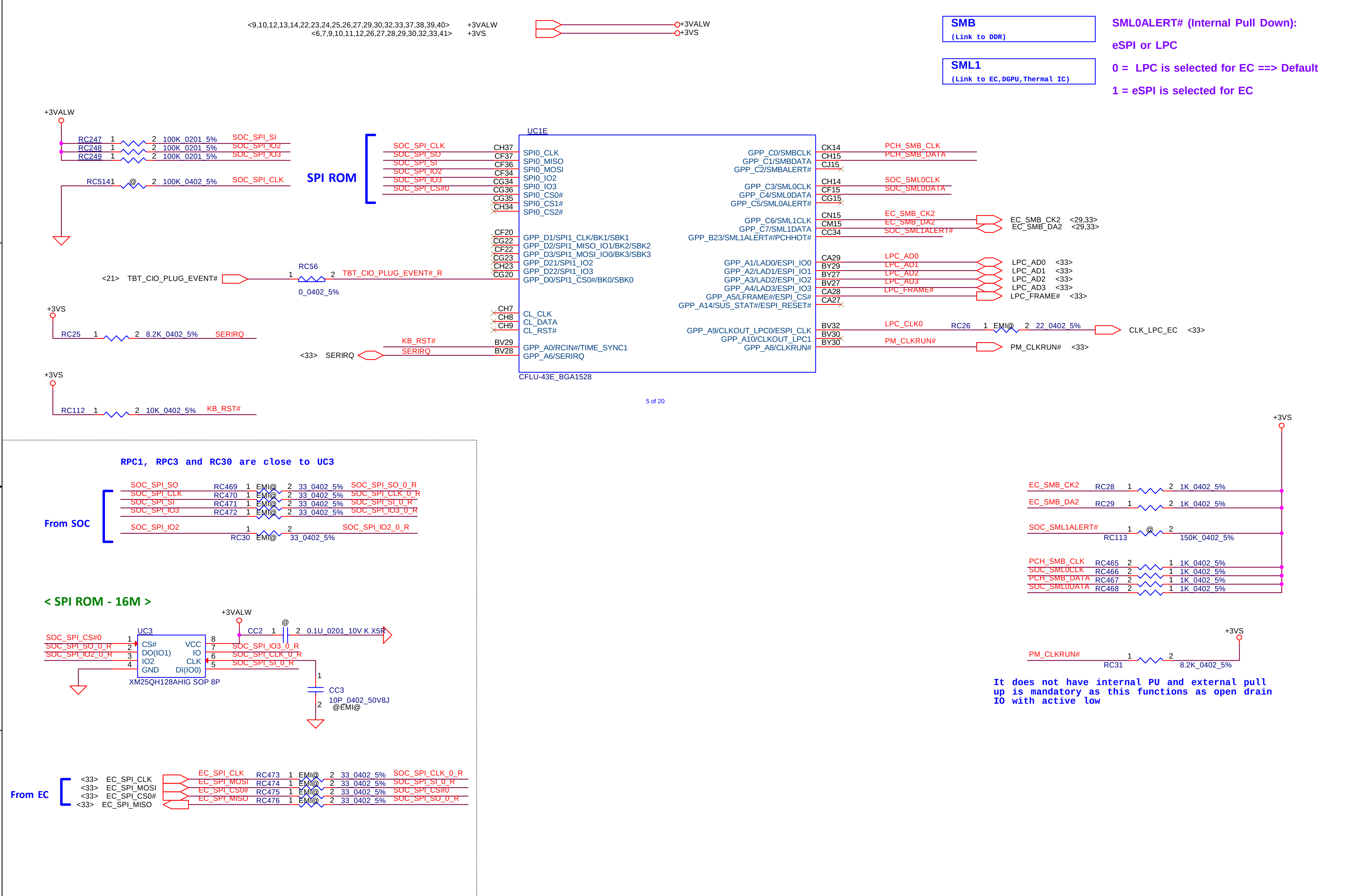

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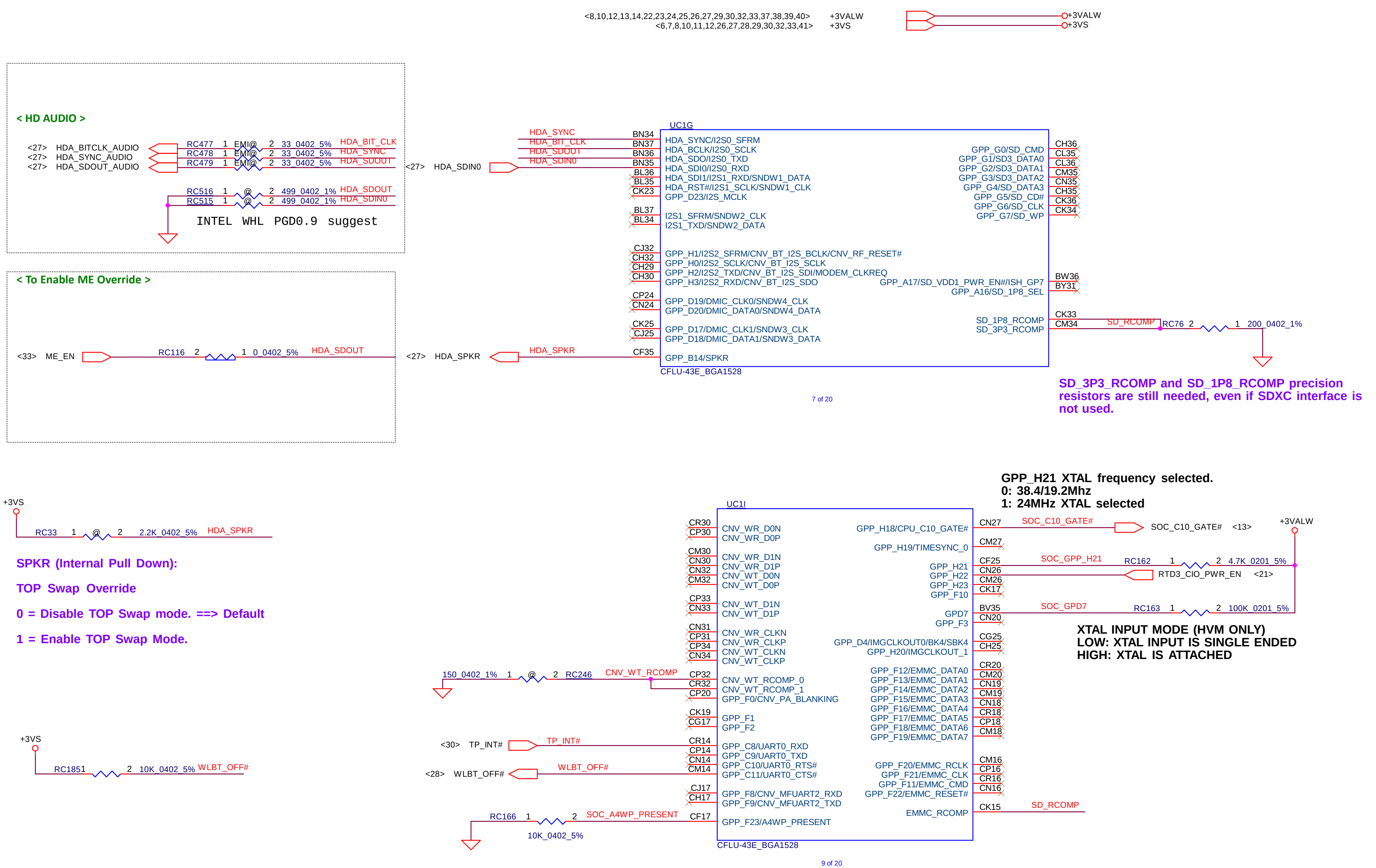
Compal Electronics, Inc.

Title: **WHL-U(3/12)SPI,SMB,LPC,ESPI**

Size	Document Number	Rev
Custom	LA-G581P	0.1

Date: Monday, June 04, 2018 Sheet 8 of 45



A4WP_PRESENT is intended to detect wireless charging system, but is not used on the platform anymore.so recommend a PD(8-10k) on the signal

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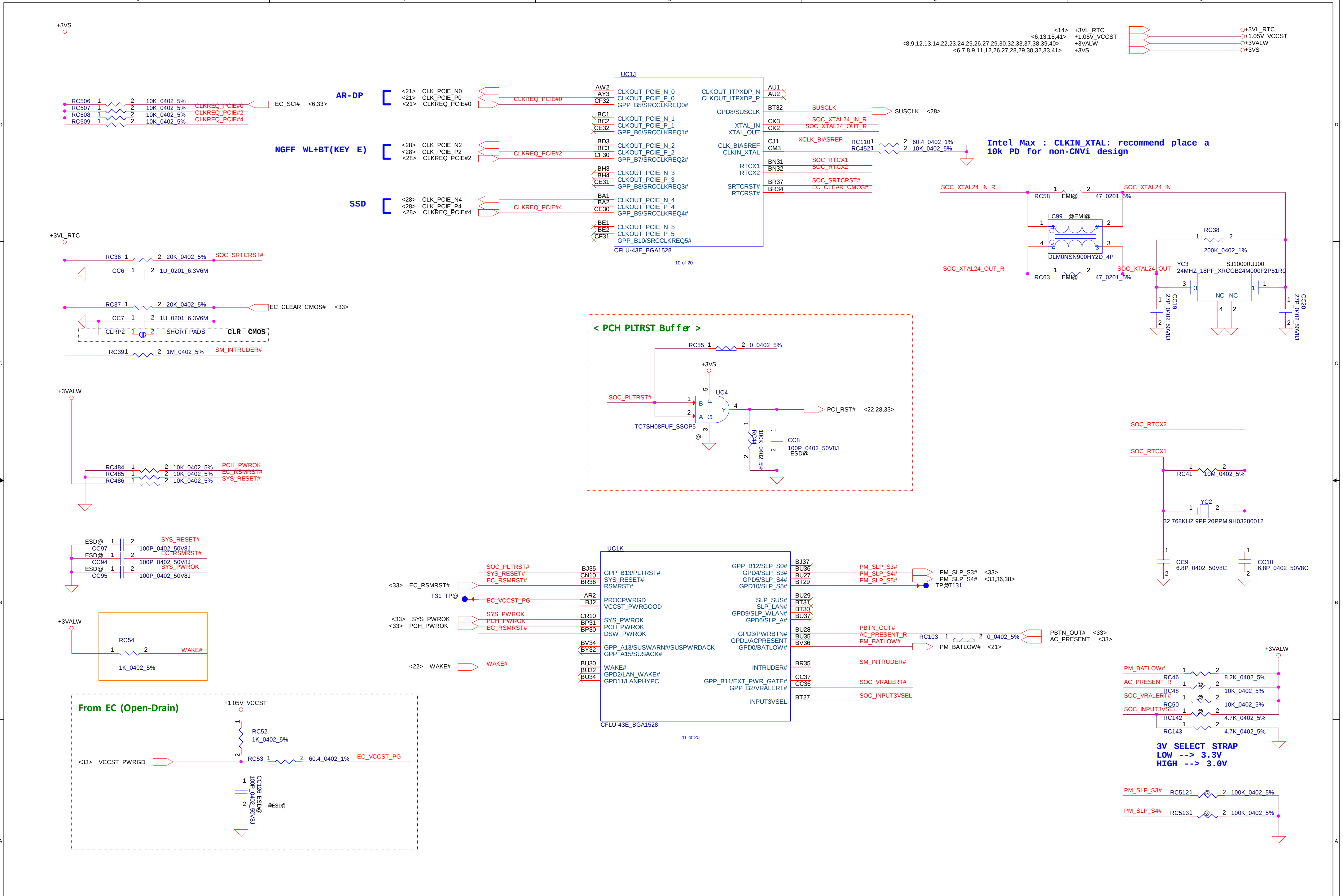
				Date: Monday, June 04, 2018; Sheet 9 of 45



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Compal Electronics, Inc.

Title: **WHL-U(5/12)CLK,PM,GPIO**

Size: Custom | Document Number: **LA-G581P** | Rev: 0.1

Date: Monday, June 04, 2018 |

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

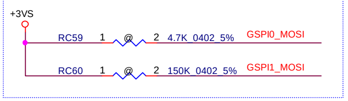
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i on i s usef ul when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

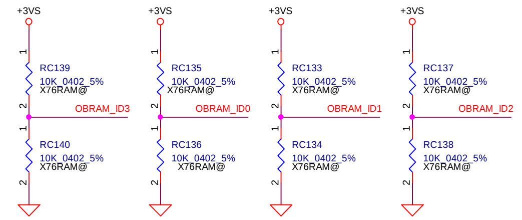
Boot BIOS Strap Bit

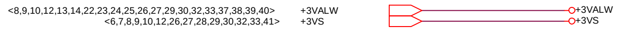
0 = SPI Mode ==> Default

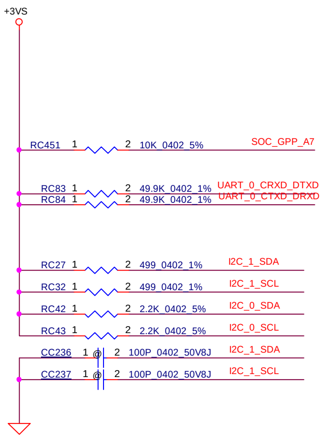
1 = LPC Mode

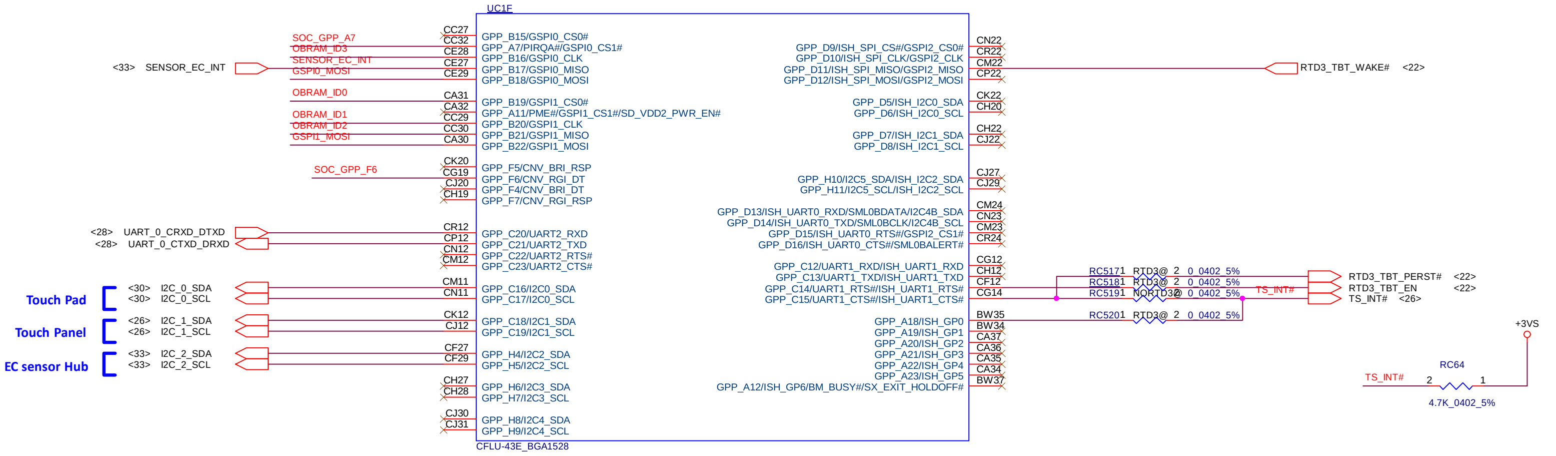


Capacity	RAM vendor	GGP_B16	GGP_B19	GGP_B20	GGP_B21
		OBRAM_ID3	OBRAM_ID0	OBRAM_ID1	OBRAM_ID2
4GB	Samsung K4A8G165WC-BCTD	0	0	0	0
	Micron MT40A512M16LY-075:E	0	0	0	1
	Hynix H5AN8G6NCJR-VKC	0	0	1	0
8GB	Samsung K4A8G165WC-BCTD	0	0	1	1
	Micron MT40A512M16LY-075:E	0	1	0	0
	Hynix H5AN8G6NCJR-VKC	0	1	0	1
16GB	Samsung K4AAG165WB-MCTD	0	1	1	0
	Micron MT40A1G16KNR-075:E	0	1	1	1
	Hynix H5ANAG6NCMR-VKC	1	0	0	0
16GB(2400)		1	0	0	1
		1	0	1	0
	Hynix H5ANAG6NAMR-UHC	1	0	1	1
		1	1	0	0
		1	1	0	1
		1	1	1	0
		1	1	1	1









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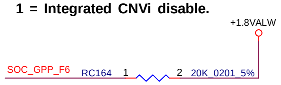
PCH EDS : M.2 CNV Mode Select

GPP_F6/CNV_RGI_DT

0 = Integrated CNVi enable.

1 = Integrated CNVi disable.



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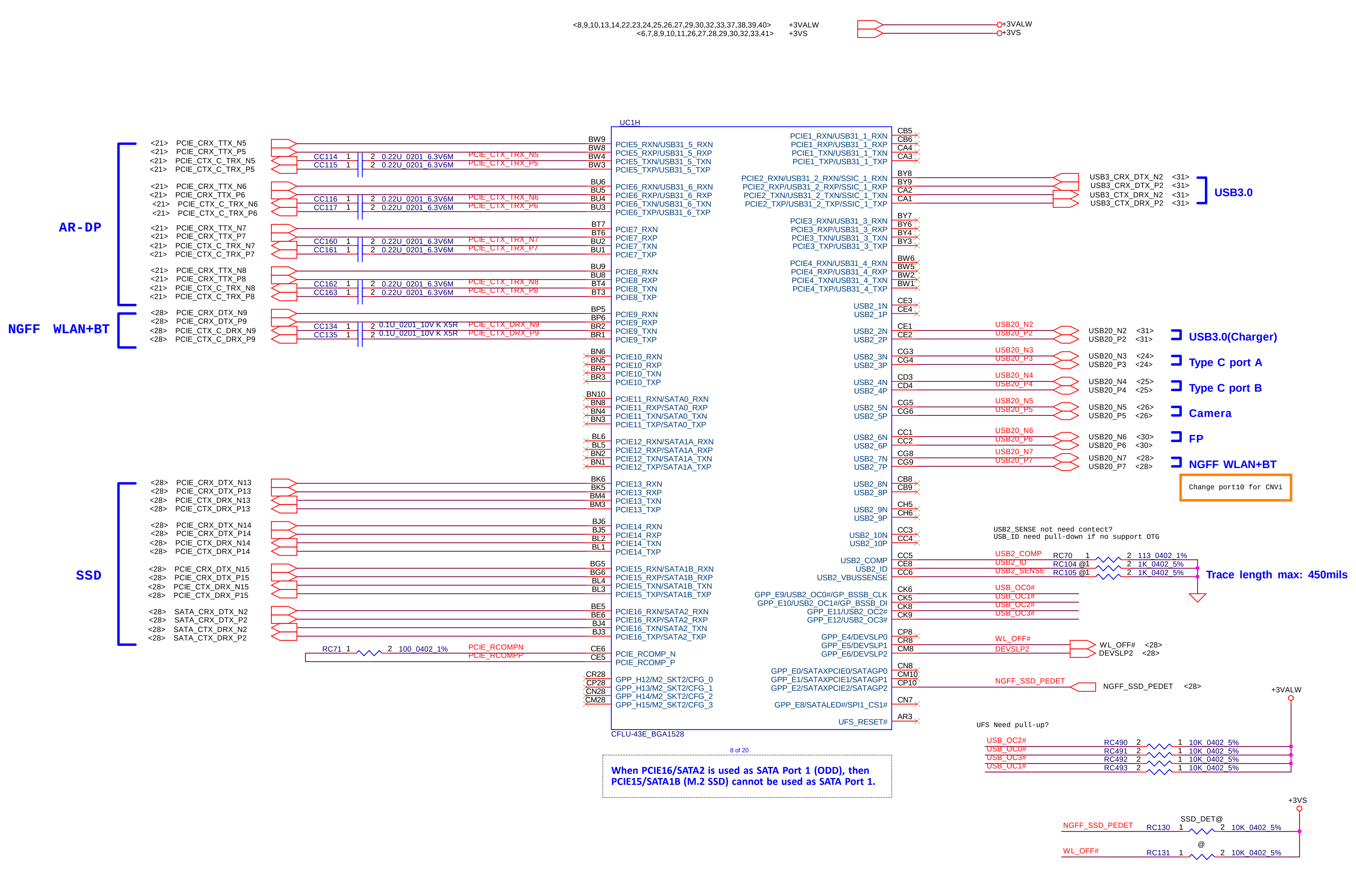

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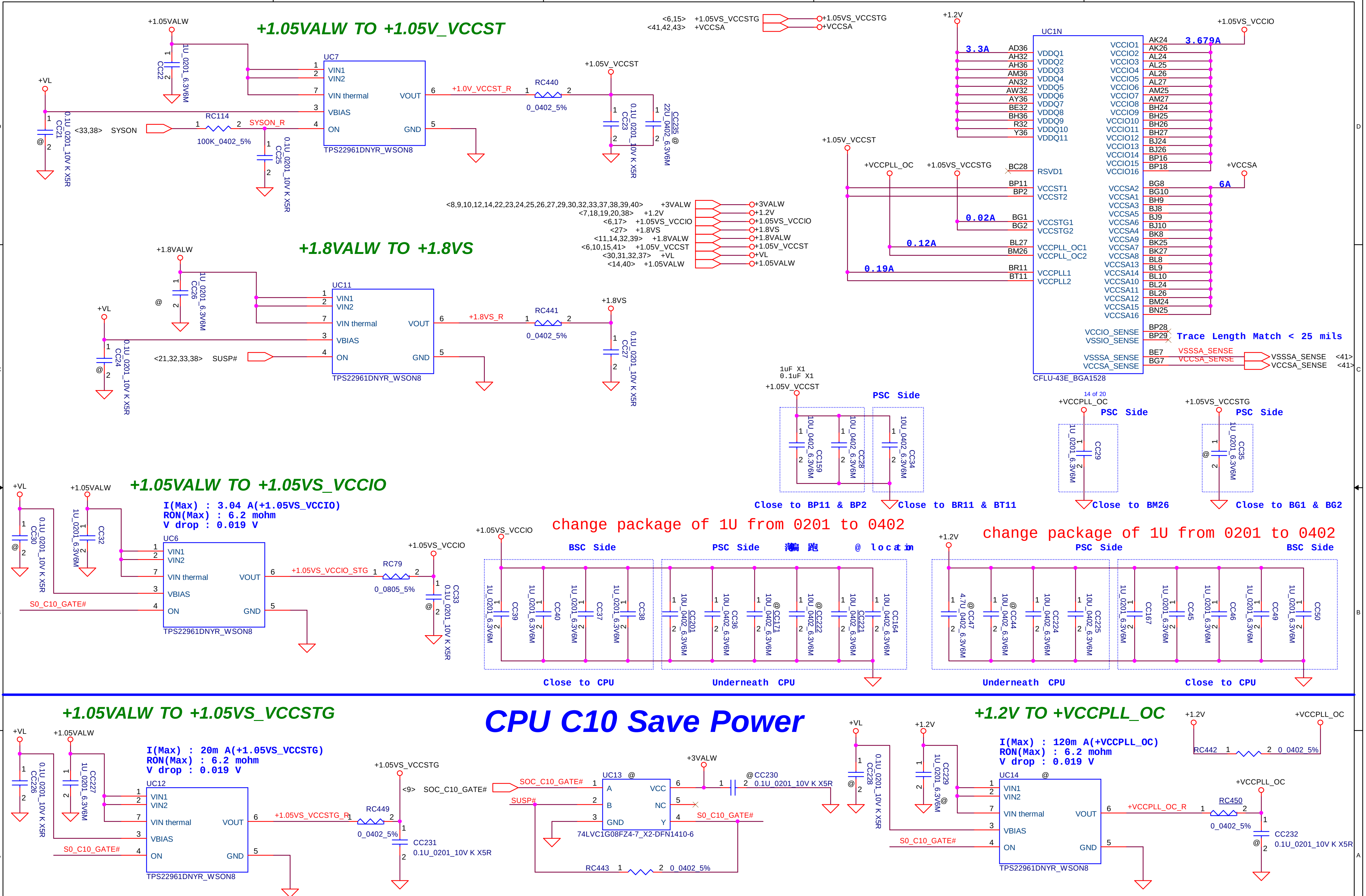

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Title: WHL-U(8/12)Power

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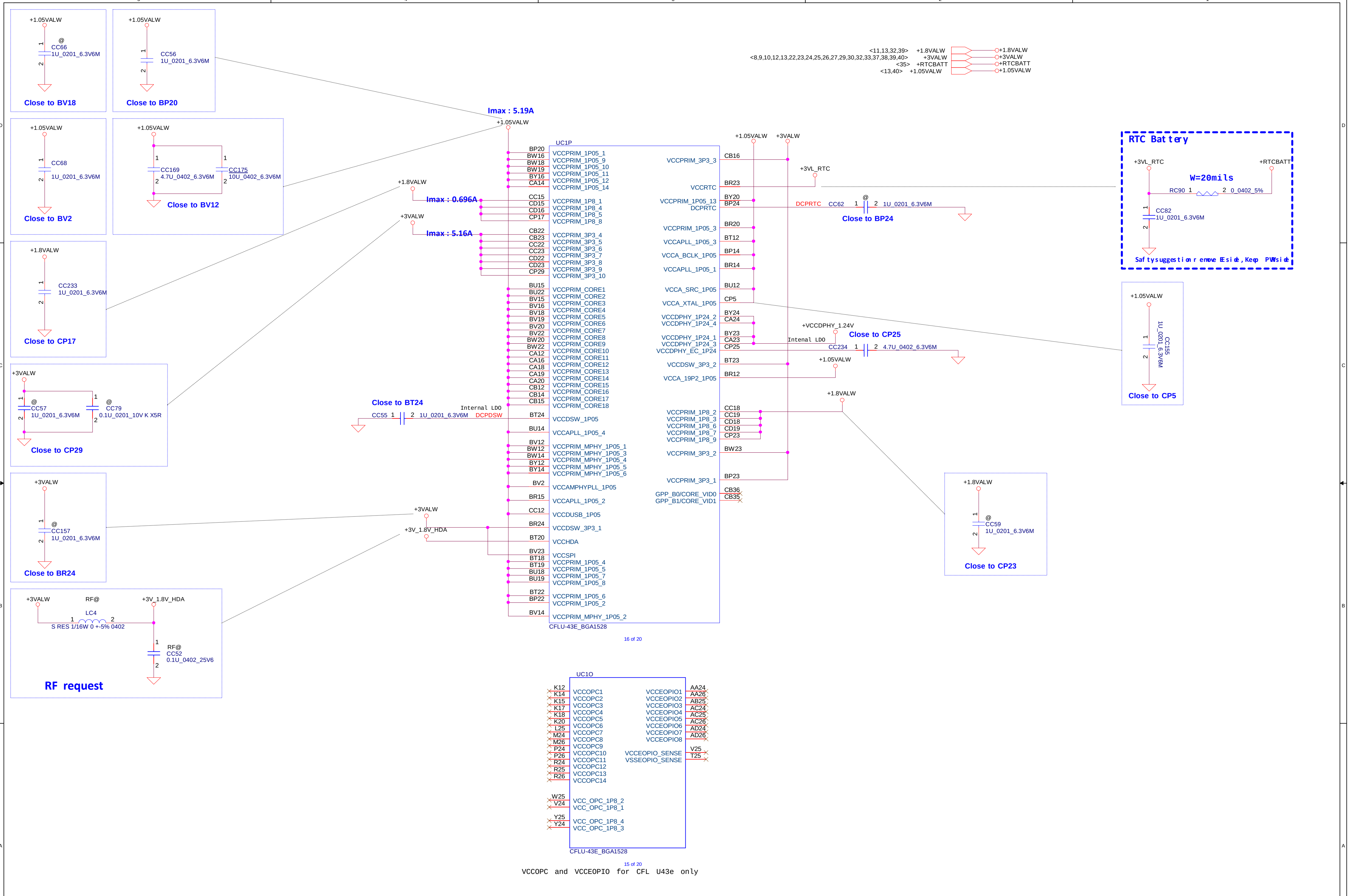

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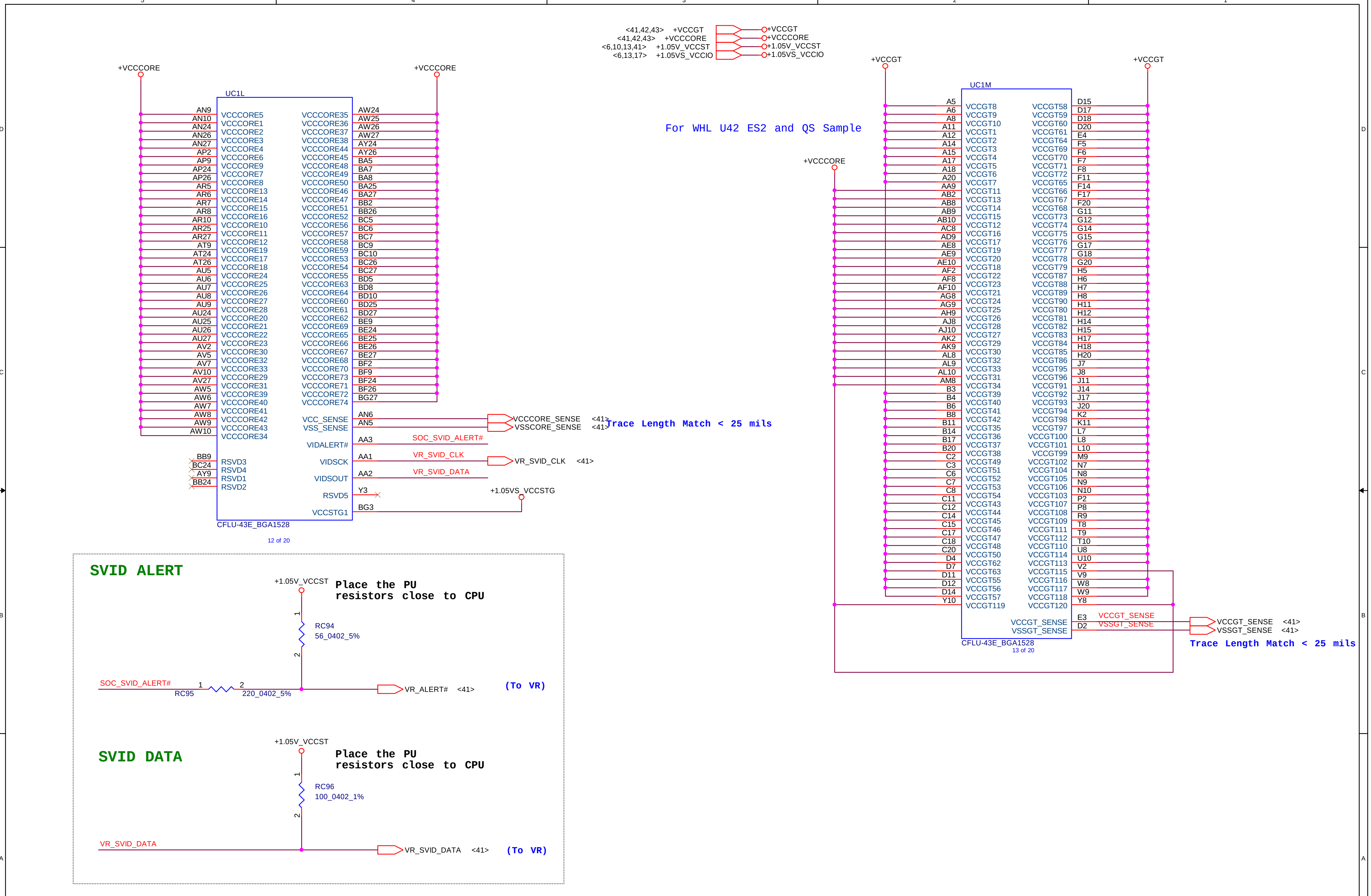

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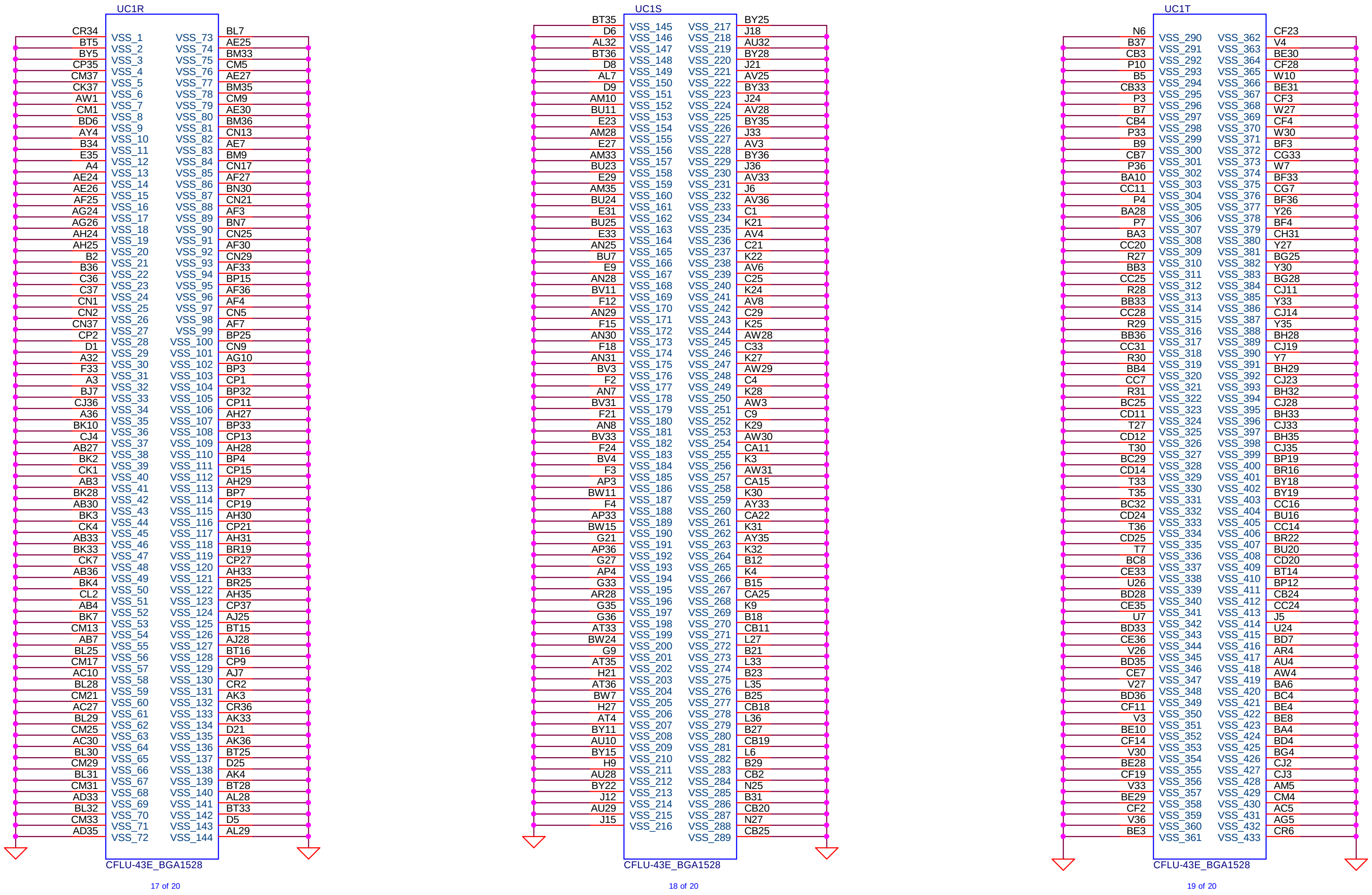

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Title	WHL-U(11/12)GND	
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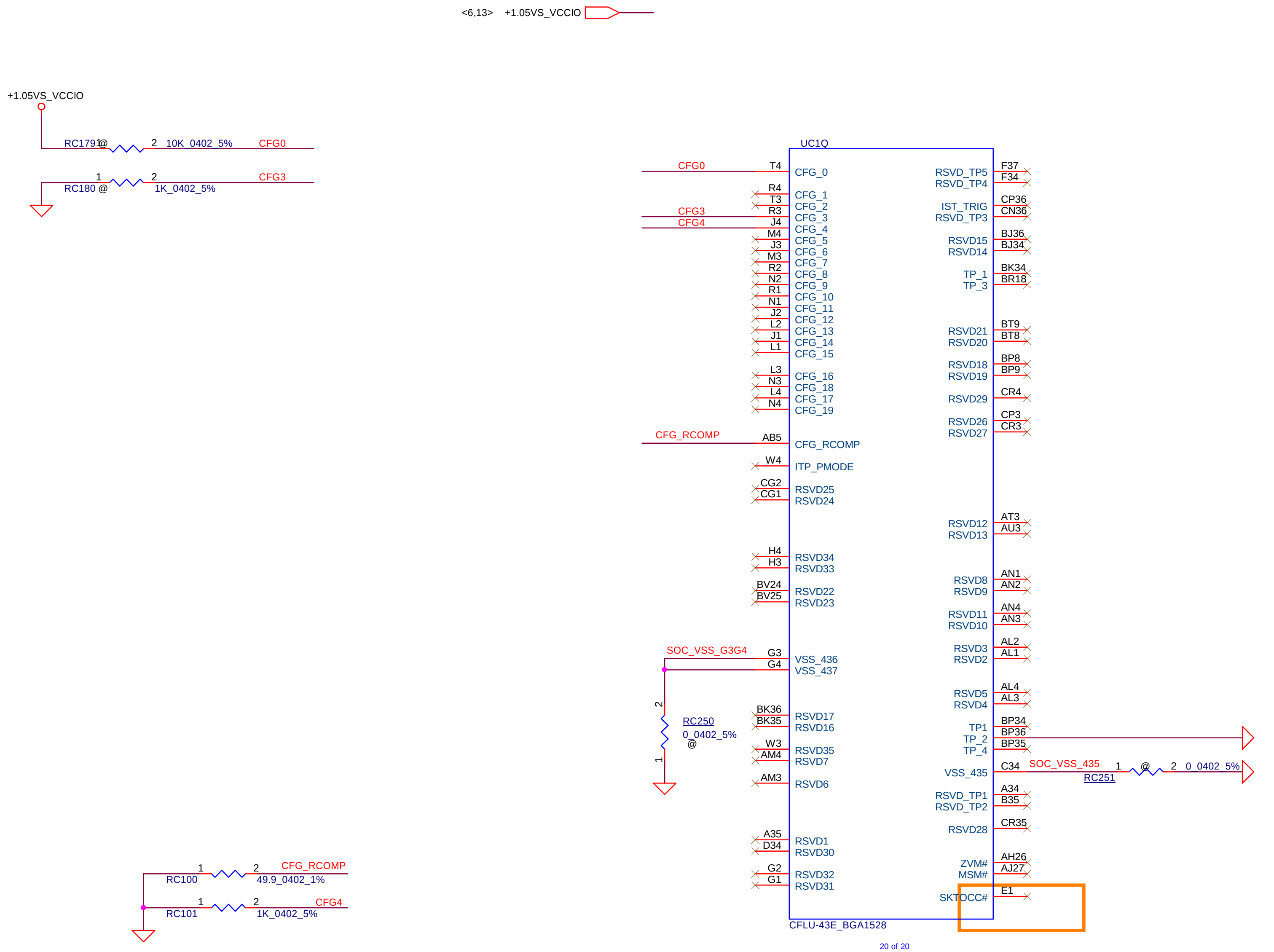

DFX Privacy Strap

CFG3	1 : Disabled; Set DFX disable bit in debug interface MSR 0 : Enabled; Set DFX enable bit in debug interface MSR

Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: **WHL-U(12/12)CFG,RSVD**

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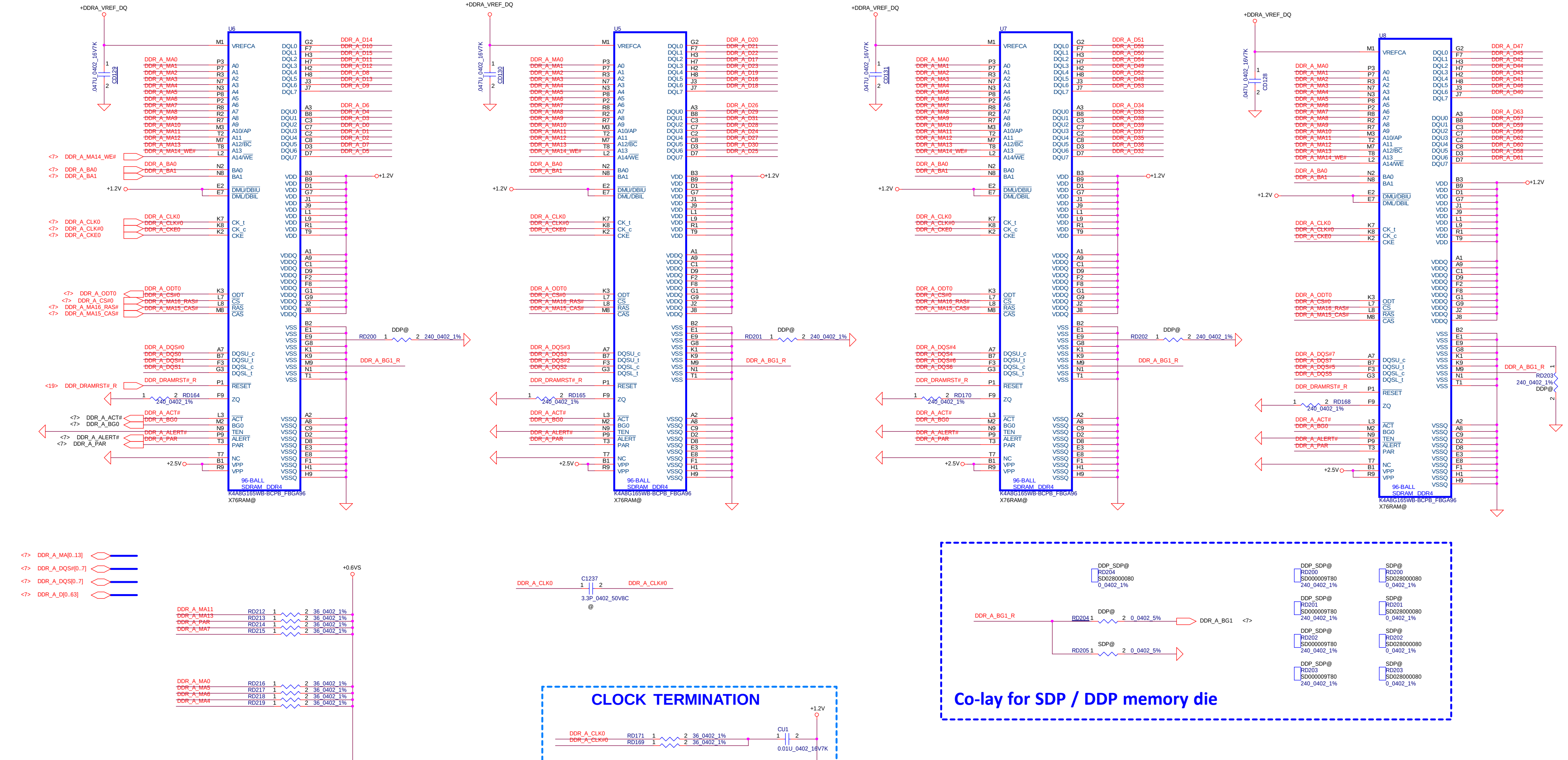
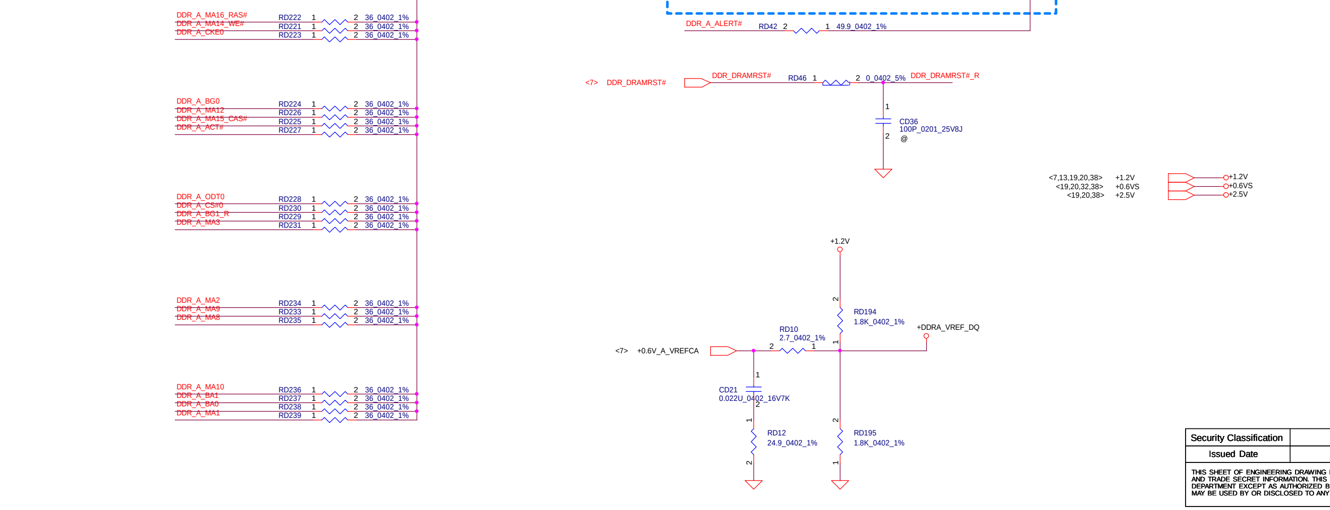
Custom	LA-G581P	0.1





Data mapping

U6	DQ	U5	DQ	U7	DQ	U8	DQ
DQL0	D14	DQL0	D23	DQL0	D51	DQL0	D47
DQL1	D10	DQL1	D19	DQL1	D55	DQL1	D45
DQL2	D15	DQL2	D18	DQL2	D50	DQL2	D42
DQL3	D11	DQL3	D22	DQL3	D54	DQL3	D44
DQL4	D12	DQL4	D21	DQL4	D49	DQL4	D43
DQL5	D8	DQL5	D16	DQL5	D52	DQL5	D41
DQL6	D13	DQL6	D17	DQL6	D48	DQL6	D46
DQL7	D9	DQL7	D20	DQL7	D53	DQL7	D40
DQU0	D7	DQU0	D27	DQU0	D34	DQU0	D63
DQU1	D5	DQU1	D31	DQU1	D33	DQU1	D57
DQU2	D3	DQU2	D29	DQU2	D38	DQU2	D59
DQU3	D4	DQU3	D28	DQU3	D39	DQU3	D56
DQU4	D2	DQU4	D30	DQU4	D37	DQU4	D62
DQU5	D1	DQU5	D25	DQU5	D35	DQU5	D60
DQU6	D6	DQU6	D26	DQU6	D36	DQU6	D58
DQU7	D0	DQU7	D24	DQU7	D32	DQU7	D61

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Title: **DDR4 Memory Down**

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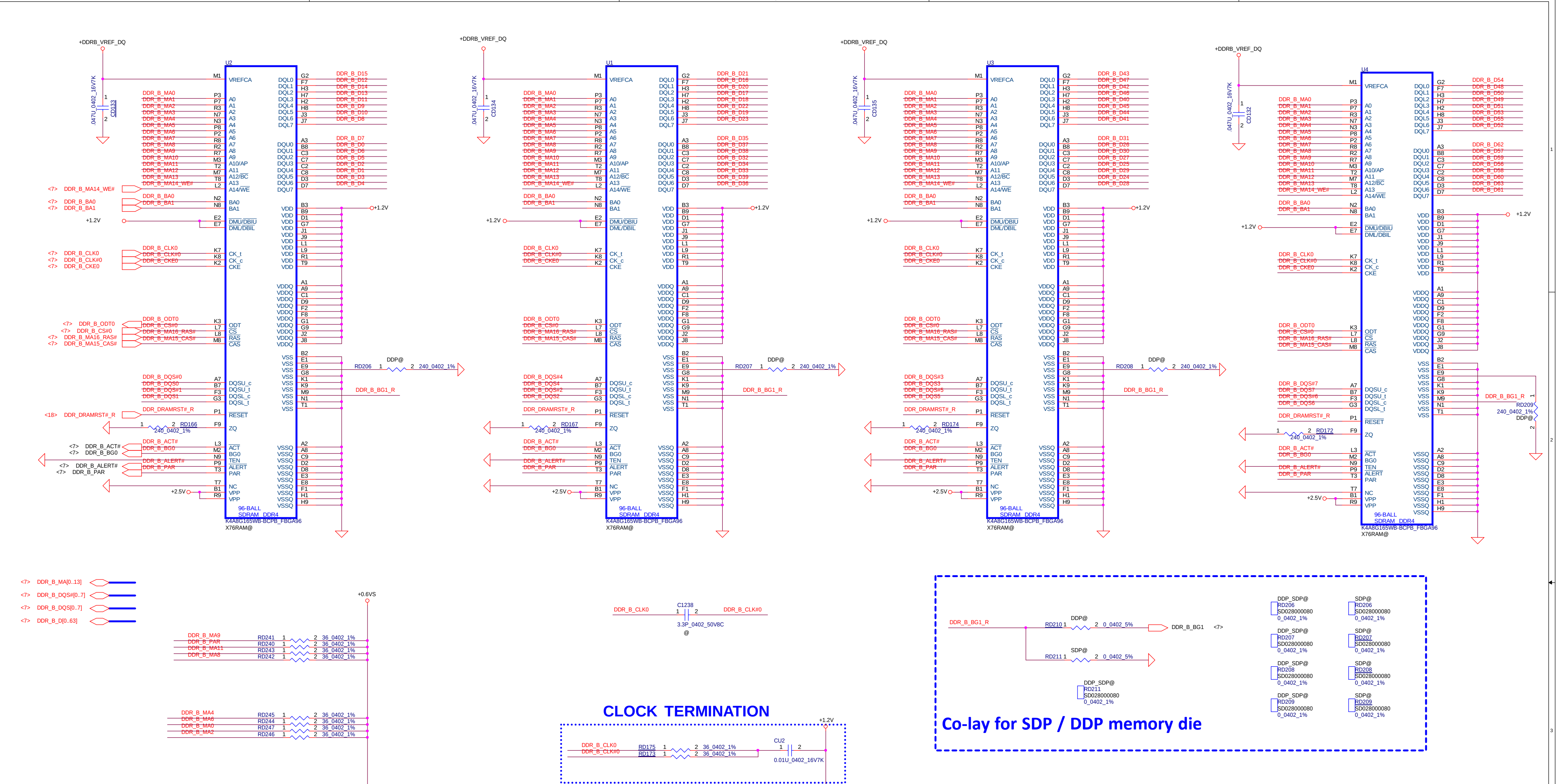
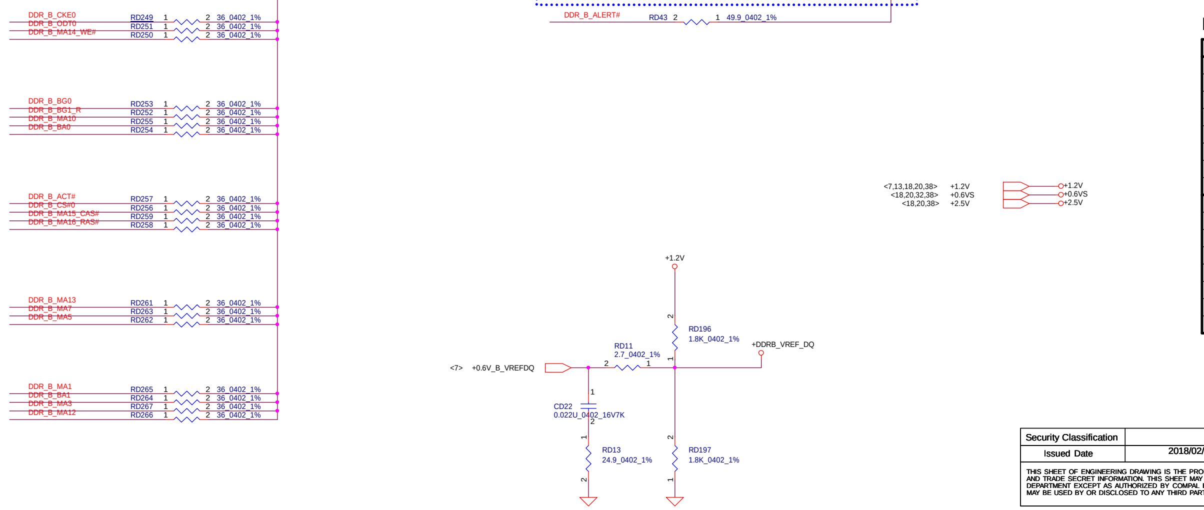




Data mapping

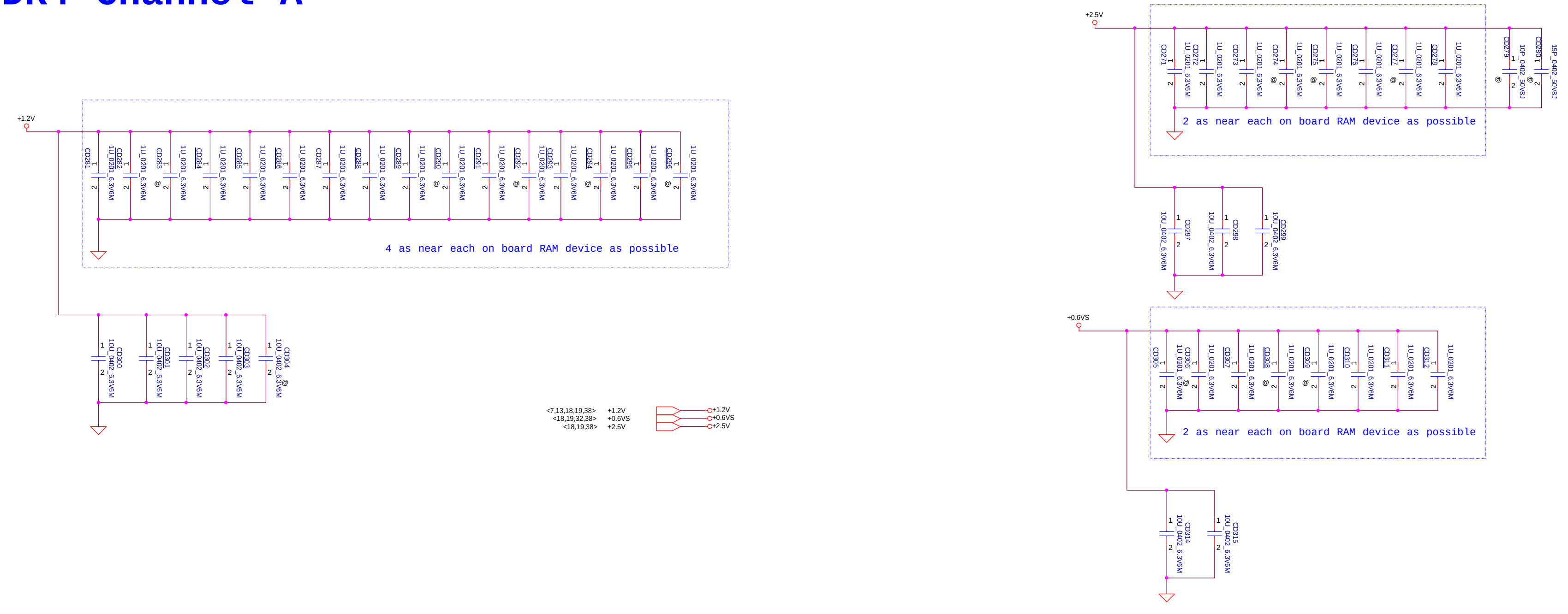
U2	DQ	U1	DQ	U3	DQ	U4	DQ
DQL0	D15	DQL0	D22	DQL0	D45	DQL0	D54
DQL1	D12	DQL1	D21	DQL1	D47	DQL1	D48
DQL2	D14	DQL2	D23	DQL2	D44	DQL2	D50
DQL3	D13	DQL3	D20	DQL3	D46	DQL3	D49
DQL4	D11	DQL4	D19	DQL4	D43	DQL4	D51
DQL5	D9	DQL5	D17	DQL5	D41	DQL5	D53
DQL6	D10	DQL6	D18	DQL6	D42	DQL6	D55
DQL7	D8	DQL7	D16	DQL7	D40	DQL7	D52
DQU0	D7	DQU0	D35	DQU0	D31	DQU0	D62
DQU1	D0	DQU1	D37	DQU1	D26	DQU1	D57
DQU2	D6	DQU2	D38	DQU2	D30	DQU2	D59
DQU3	D5	DQU3	D32	DQU3	D27	DQU3	D56
DQU4	D2	DQU4	D34	DQU4	D25	DQU4	D58
DQU5	D1	DQU5	D33	DQU5	D29	DQU5	D60
DQU6	D3	DQU6	D39	DQU6	D24	DQU6	D63
DQU7	D4	DQU7	D36	DQU7	D28	DQU7	D61

Compal Electronics, Inc.

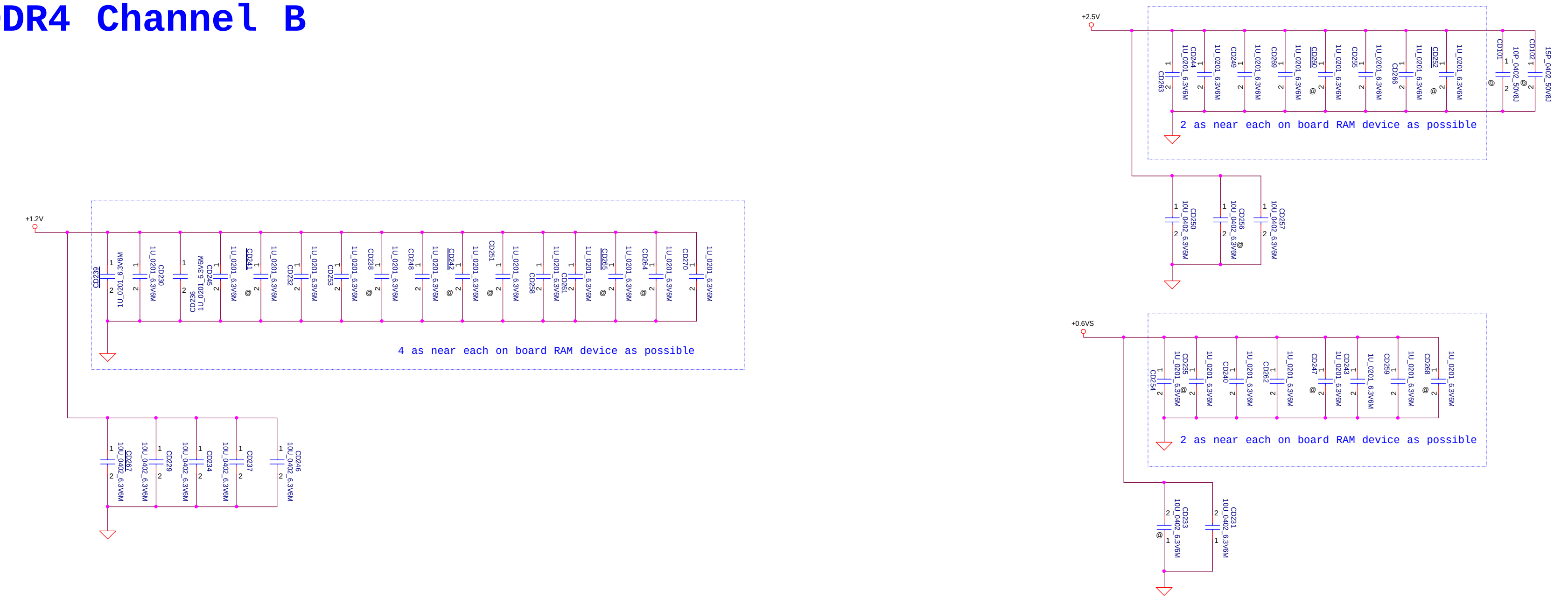
Title: **DDR4 Memory Down**

Size: Custom | Document Number: LA-G581P | Rev: 0.1

DDR4 Channel A



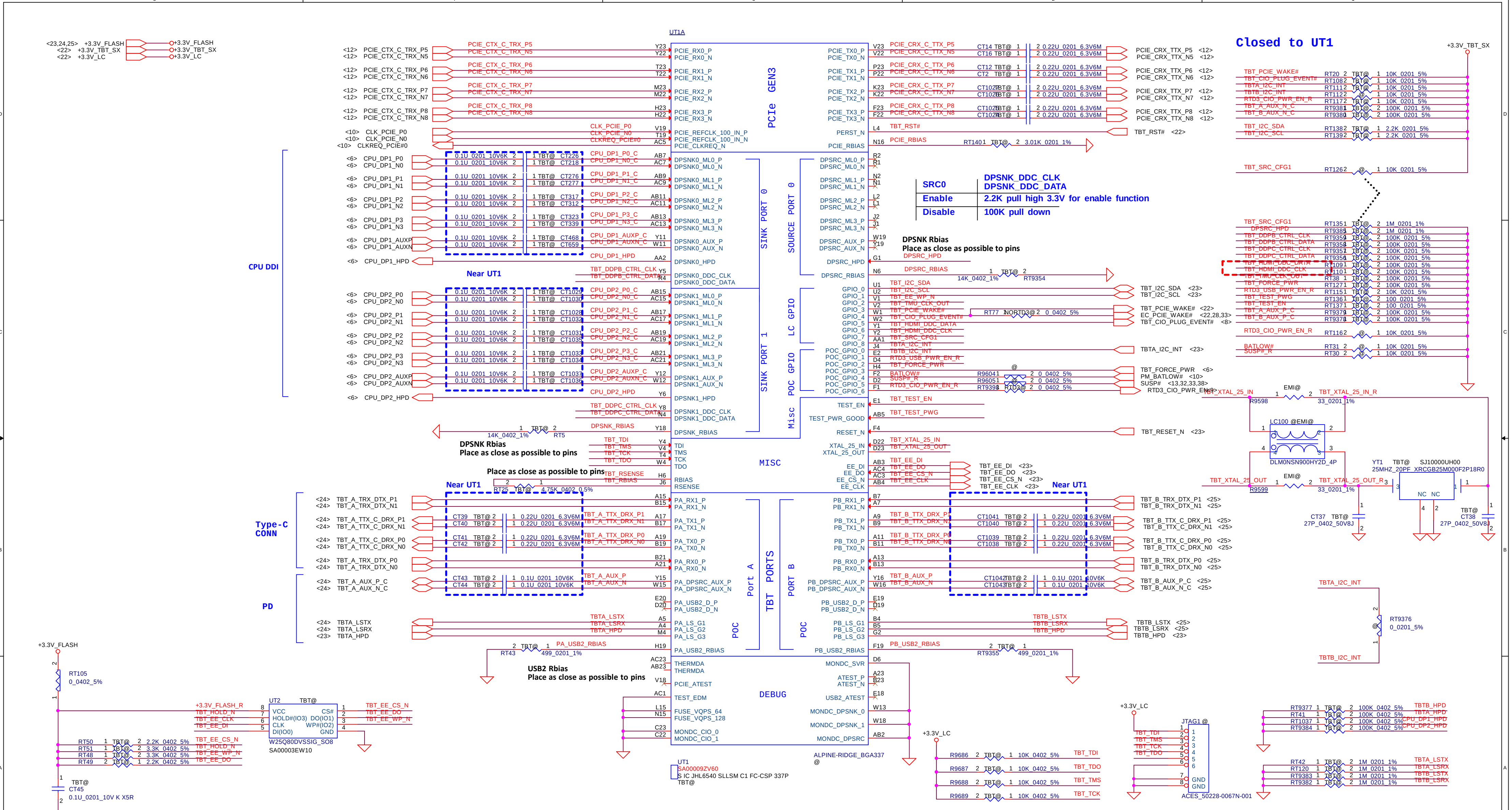
DDR4 Channel B



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title	DDR4_DIMM	
Size: Custom	Document Number: LA-G581P	Rev: 0.1
Date: Monday, June 04, 2018	Sheet 20 of 45	



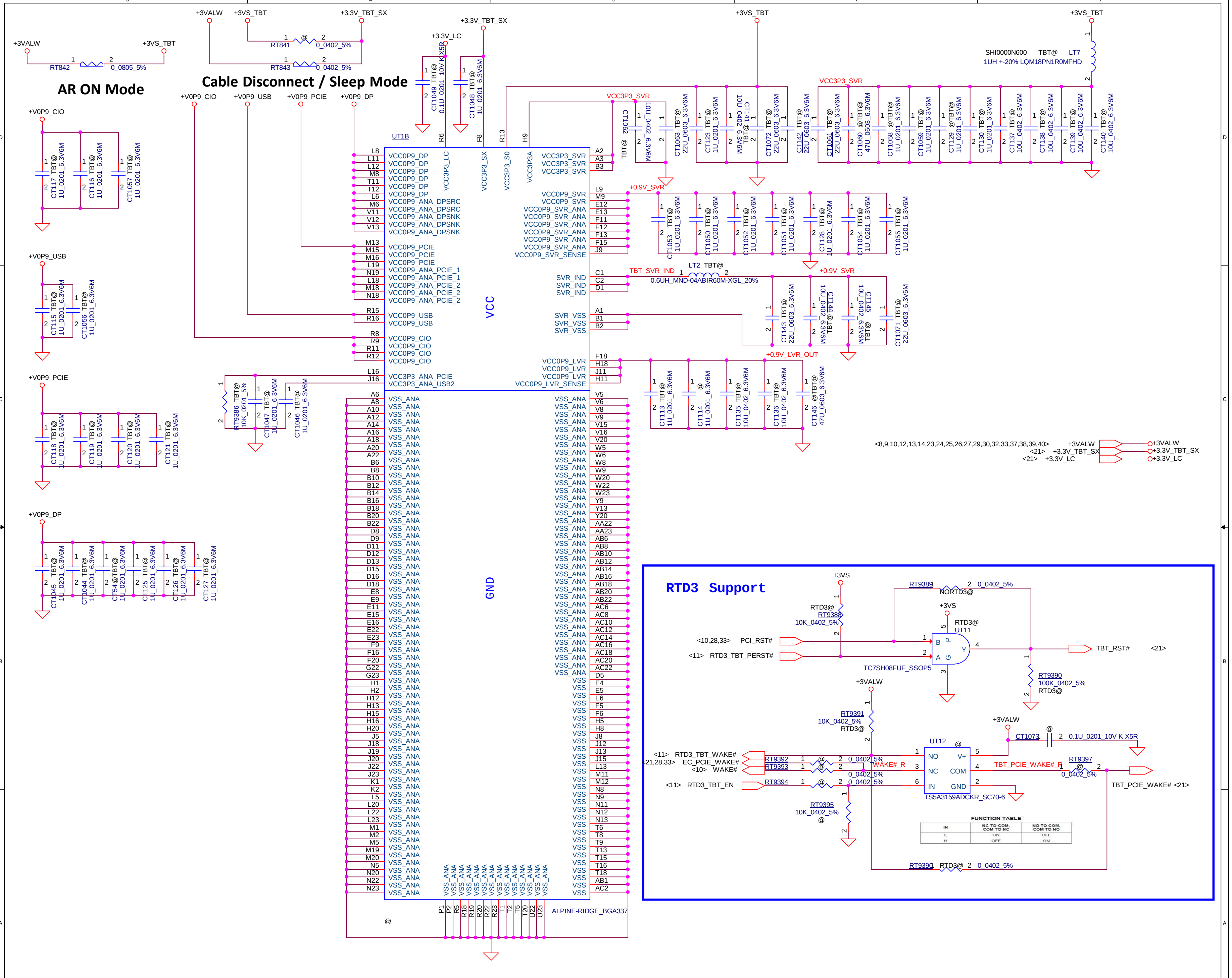
Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title: **Thunderbolt AR-DP(1/2)**

Size	Document Number	Rev
Custom	LA-G581P	0.1

Date: Monday, June 04, 2018 | Sheet 21 of 45



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

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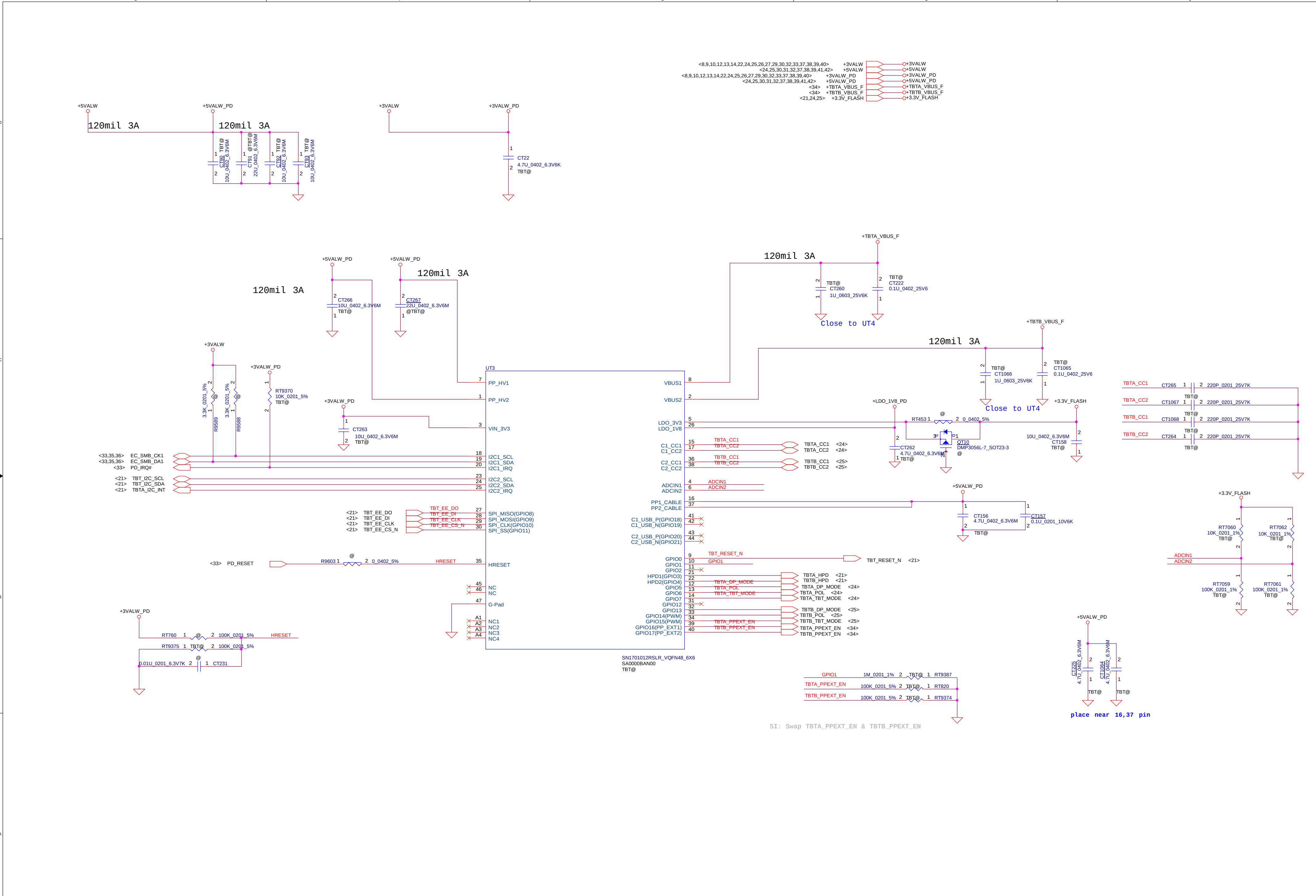
Compal Electronics, Inc.

Title: **Thunderbolt AR-DP(2/2)**

Size: Custom | Document Number: **LA-G581P** | Rev: 0.1

Date: Monday, June 04, 2018 | Sheet 22 of 45



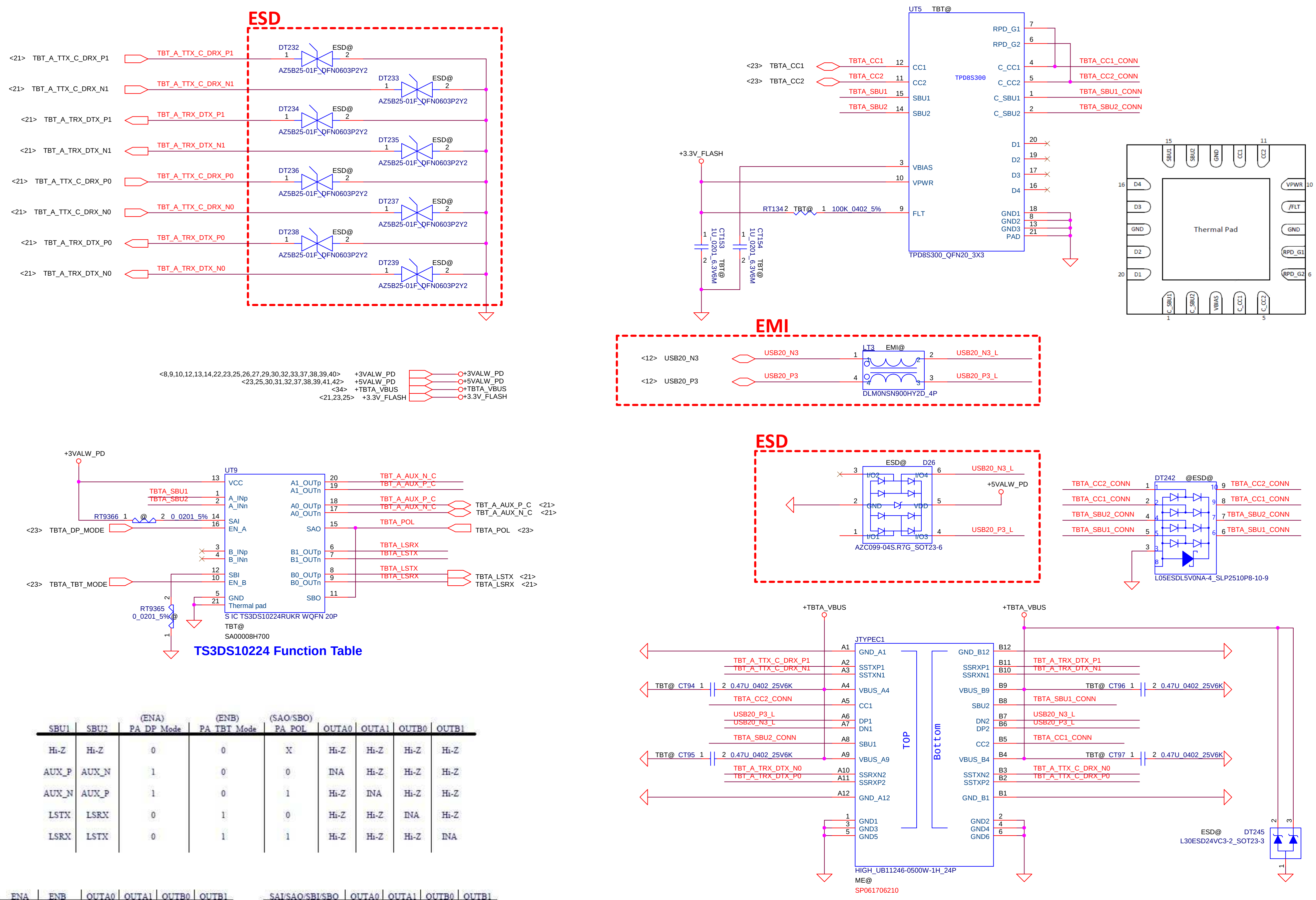
Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title: **TI TPS65988BC**

Size: Custom | Document Number: **LA-G581P** | Rev 0.1

Date: Monday, June 04, 2018 | Sheet 23 of 45



TS3DS10224 Function Table

SBU1	SBU2	(ENA) PA_DP_Mode	(ENB) PA_TBT_Mode	(SAO/SBO) PA_POL	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	INA	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	INA	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	INA	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	Hi-Z	INA

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN

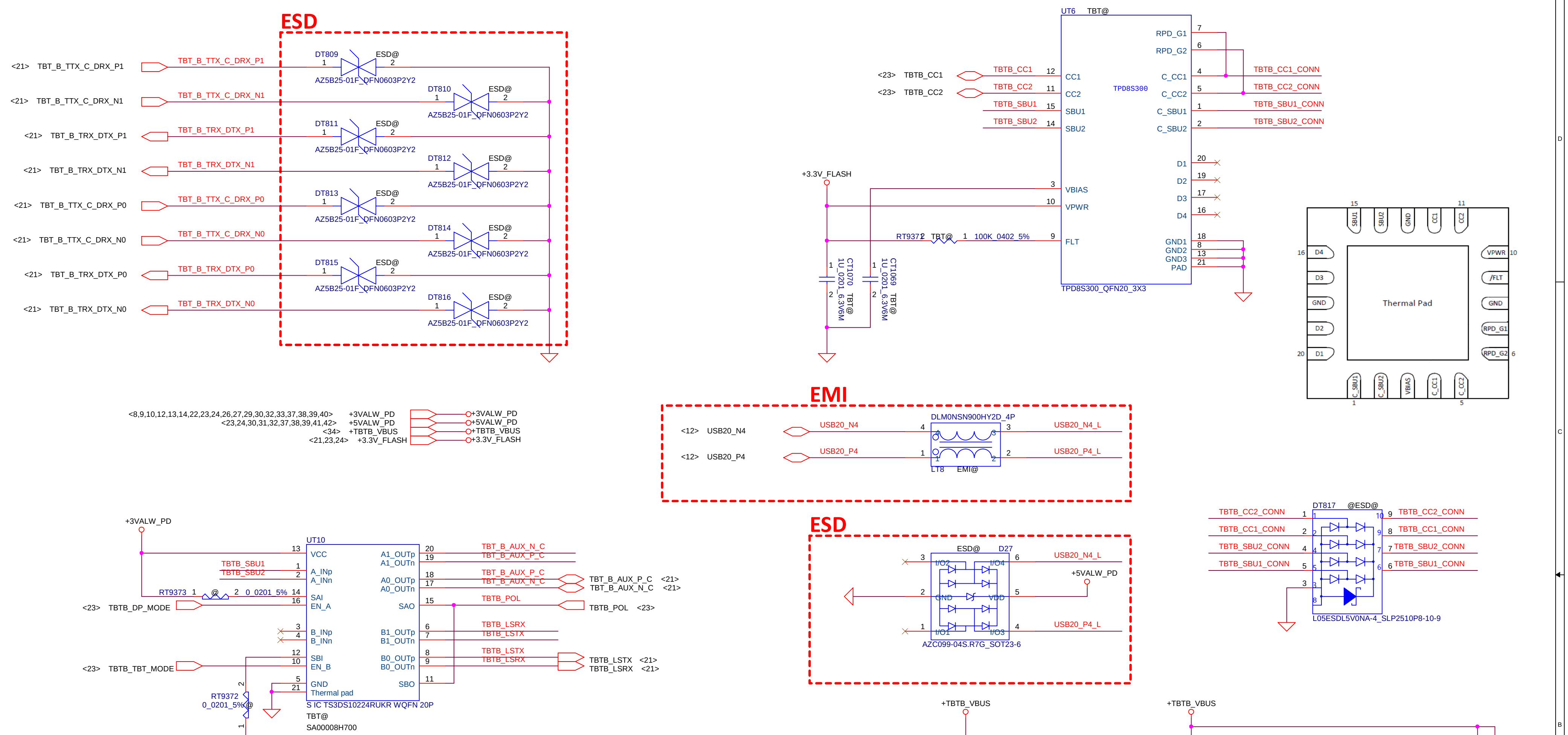
SAI/SAO/SBI/SBO	OUTA0	OUTA1	OUTB0	OUTB1
1 0 0 0	INA	Hi-Z	INA	Hi-Z
1 1 0 1	Hi-Z	INA	Hi-Z	INA

Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title: **Typec-C CONN_A**

Size: Custom | Document Number: **LA-G581P** | Rev: 0.1

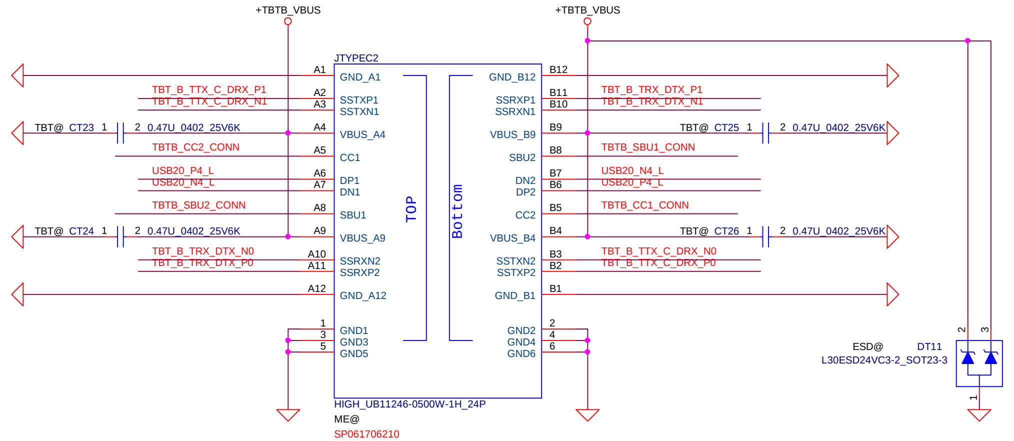


TS3DS10224 Function Table

SBU1	SBU2	(ENA) PA_DP_Mode	(ENB) PA_TBT_Mode	(SAO/SBO) PA_POL	OUTA0	OUTA1	OUTB0	OUTB1
Hi-Z	Hi-Z	0	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
AUX_P	AUX_N	1	0	0	INA	Hi-Z	Hi-Z	Hi-Z
AUX_N	AUX_P	1	0	1	Hi-Z	INA	Hi-Z	Hi-Z
LSTX	LSRX	0	1	0	Hi-Z	Hi-Z	INA	Hi-Z
LSRX	LSTX	0	1	1	Hi-Z	Hi-Z	Hi-Z	INA

ENA	ENB	OUTA0	OUTA1	OUTB0	OUTB1
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	Hi-Z	EN	EN
1	0	EN	EN	Hi-Z	Hi-Z
1	1	EN	EN	EN	EN

SAI/SAO/SBI/SBO	OUTA0	OUTA1	OUTB0	OUTB1
1 0 0 0	INA	Hi-Z	INA	Hi-Z
1 1 0 1	Hi-Z	INA	Hi-Z	INA

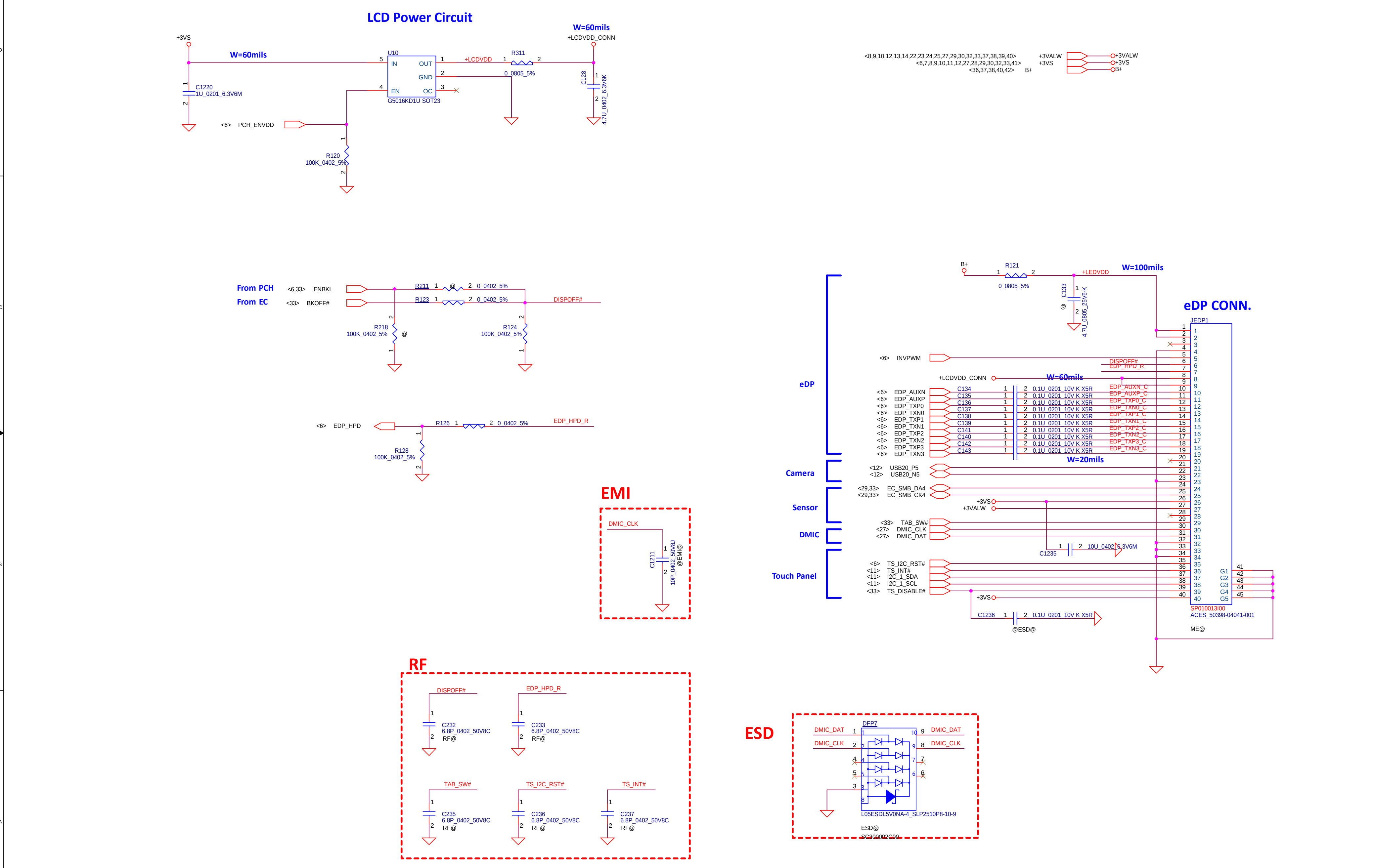


Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title: **Type-C CONN. B**

Size: Custom | Document Number: **LA-G581P** | Rev: 0.1



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

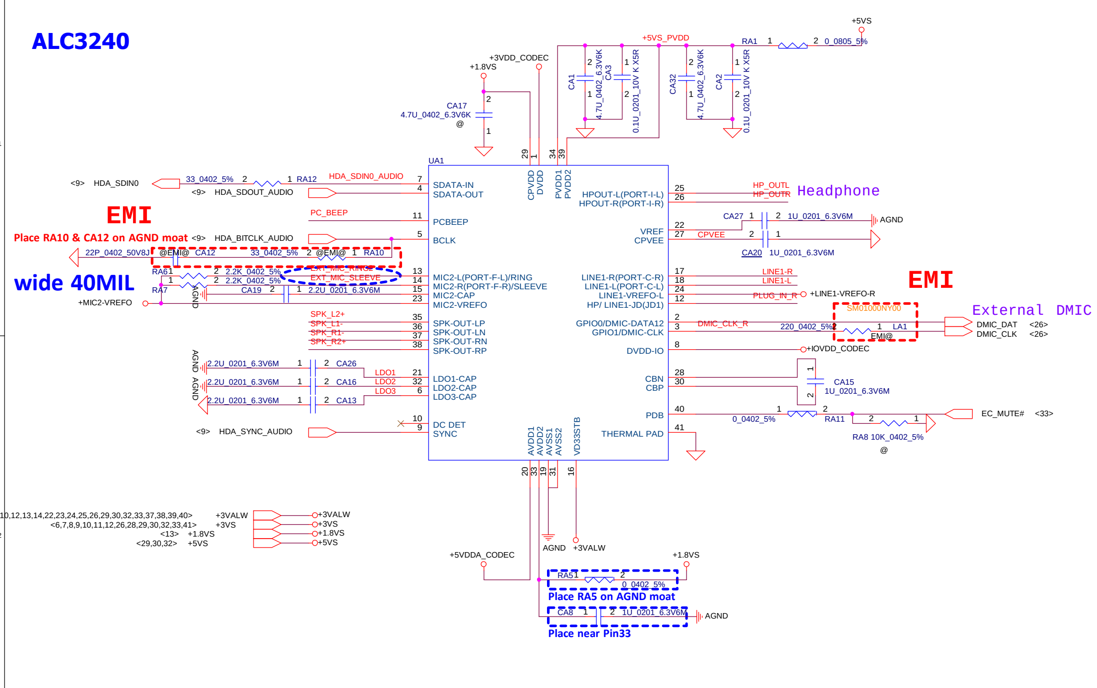
Compal Electronics, Inc.

Title: **eDP/Camera**

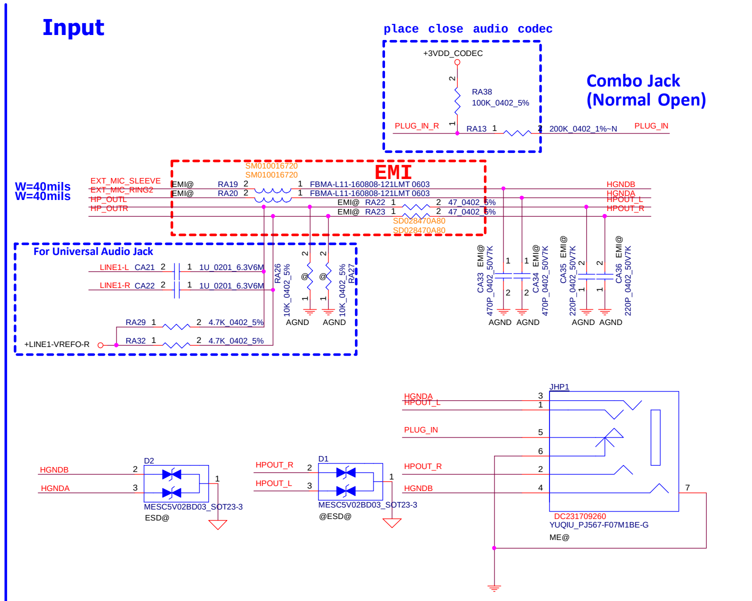
Size	Document Number	Rev
C	LA-G581P	0.1

Date: Monday, June 04, 2018 Sheet 26 of 45

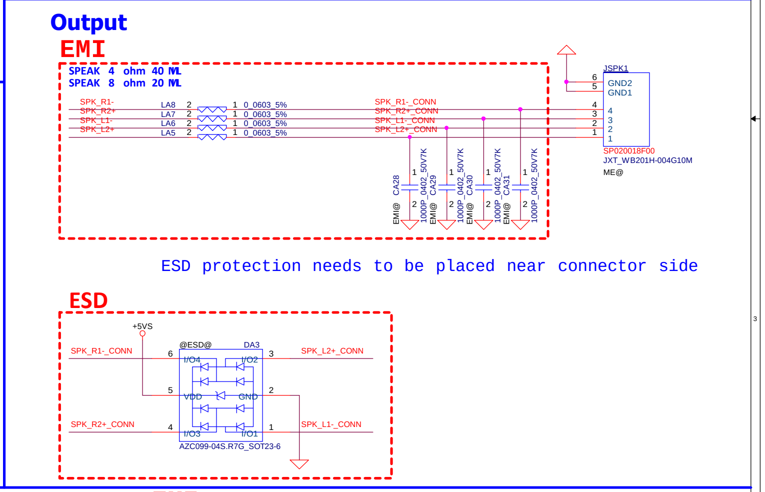
ALC3240



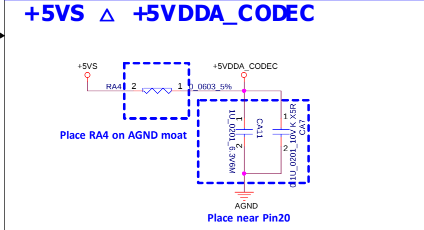
Input



Output



+5VS △ +5VDDA_CODEC



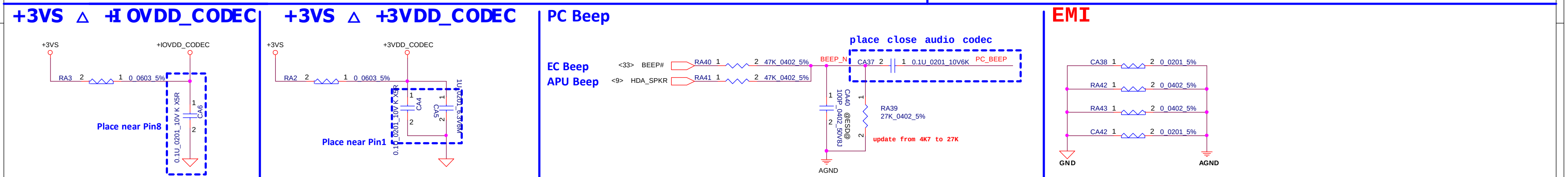
Each Platform Power Net Support list

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

Each Platform HDA Link Voltage Support (Pin 8)

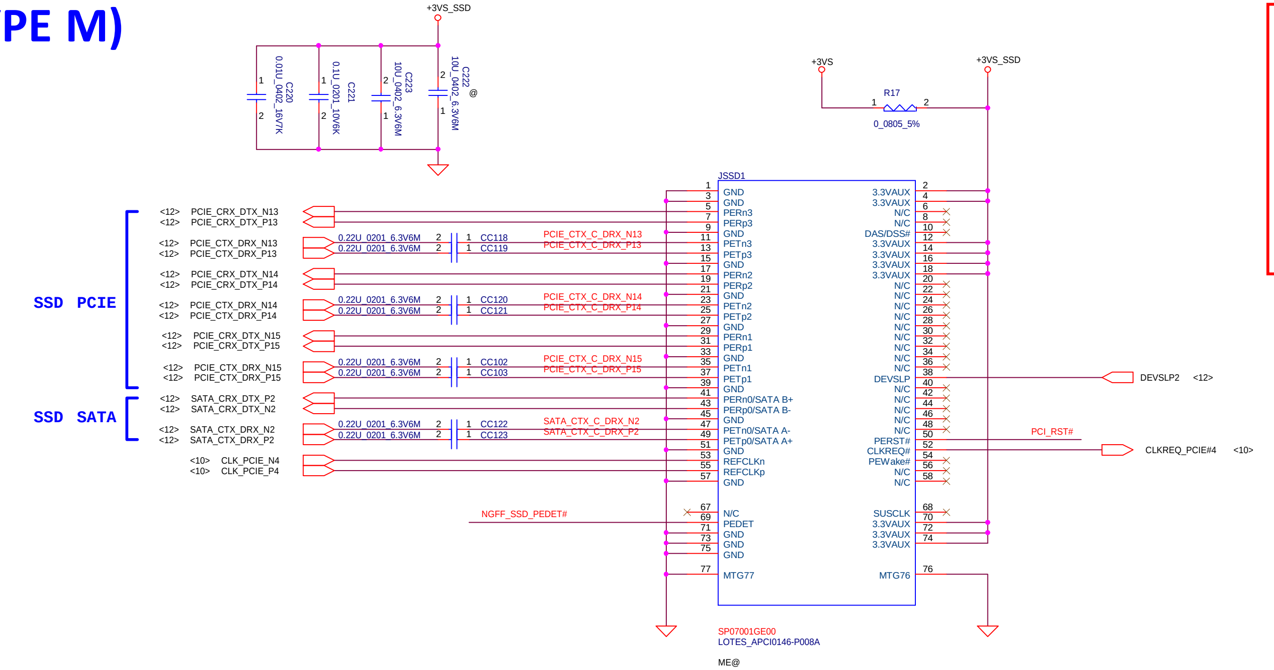
	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

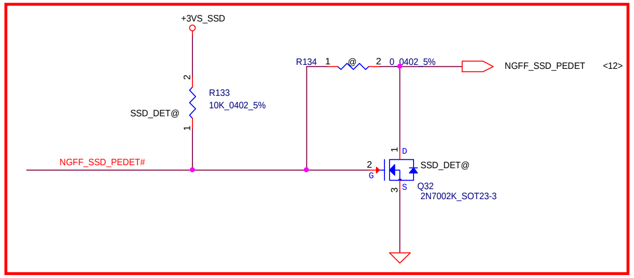
+3VS △ +IOVDD_CODEC   +3VS △ +3VDD_CODEC   PC Beep   EMI



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/02/06	Deciphered Date 2020/5/17	Title: HD Audio Codec ALC3240
			Size: Custom; Document Number: LA-G581P; Rev 0.1
			Date: Monday, June 04, 2018; Sheet 27 of 45

SSD(TYPE M)





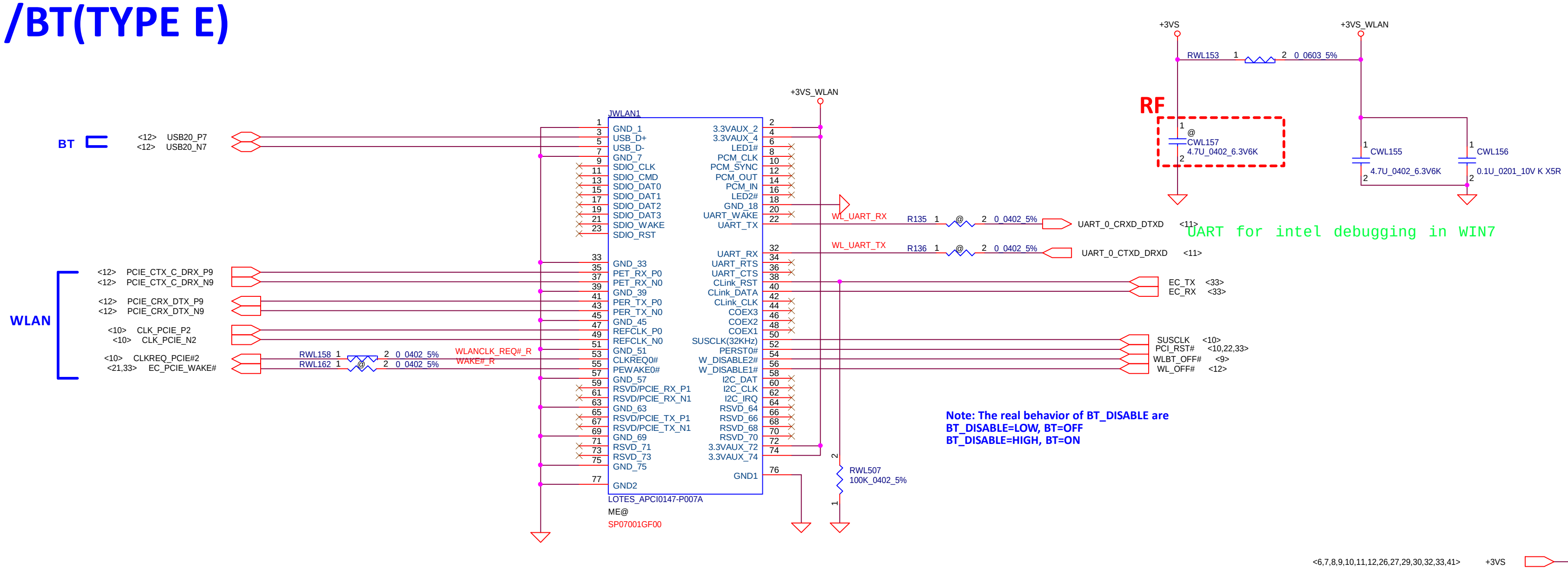
NGFF_SSD_PEDET#

H : PCIE Interface

L : SATA Interface

Fellow 543016_SKL_U_Y_PDG_0_9

NGFF WLAN /BT(TYPE E)



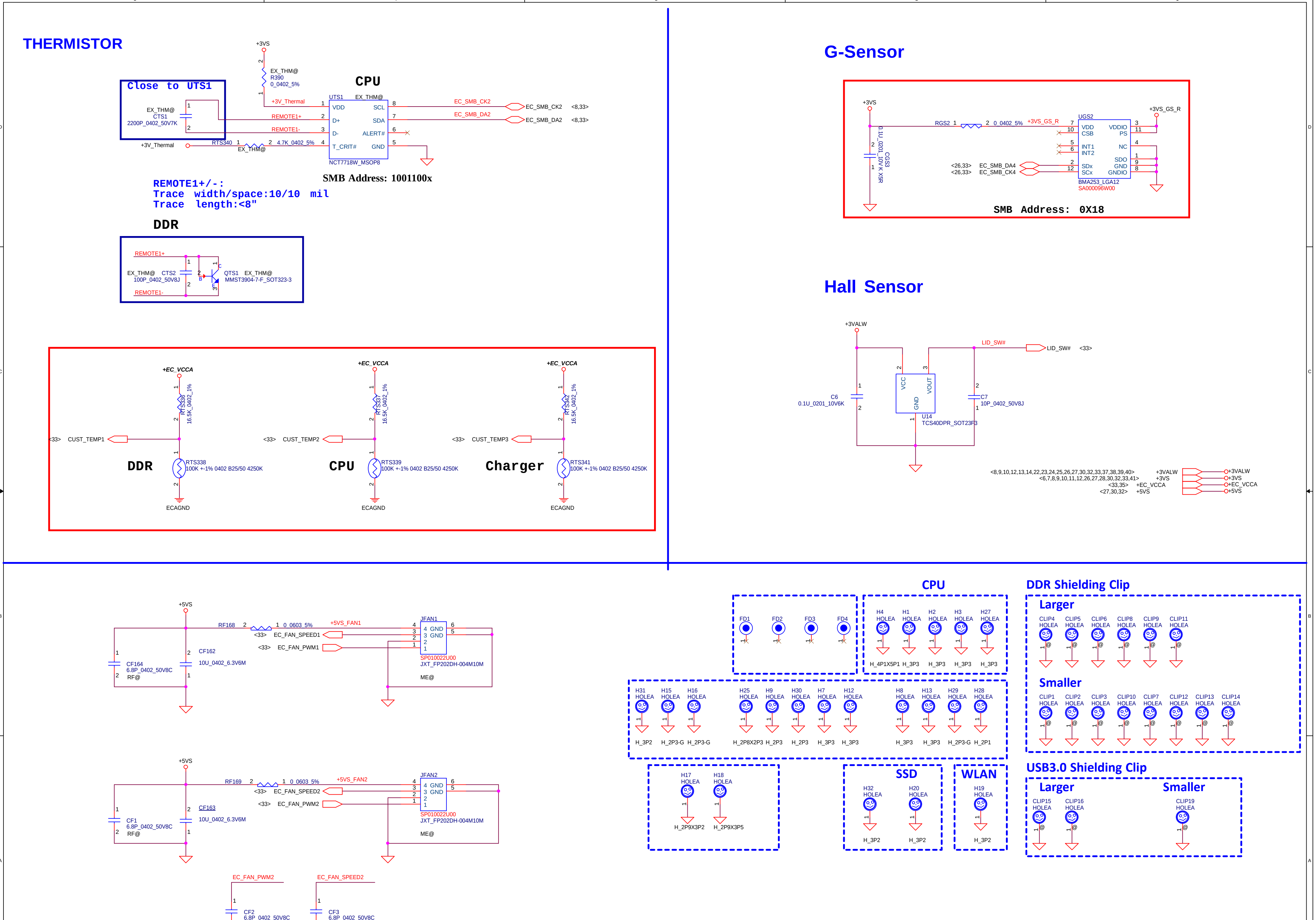
<6,7,8,9,10,11,12,26,27,29,30,32,33,41> +3VS +3VS

Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

Compal Electronics, Inc.

Title: **NGFF WLAN/SSD**

Size	Document Number	Rev
C	LA-G581P	0.1



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

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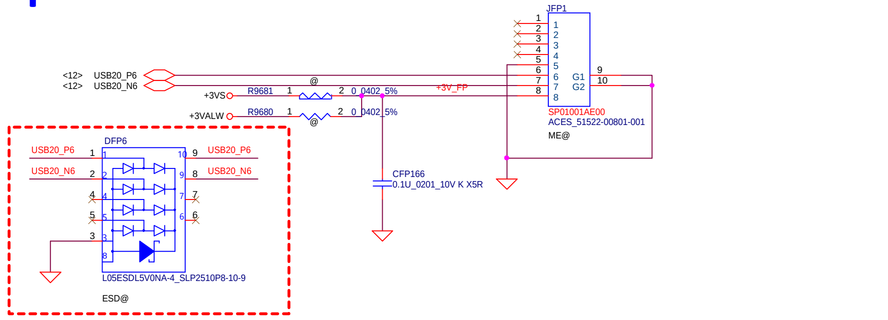
Compal Electronics, Inc.

Title: **FAN/Thermal sensor**

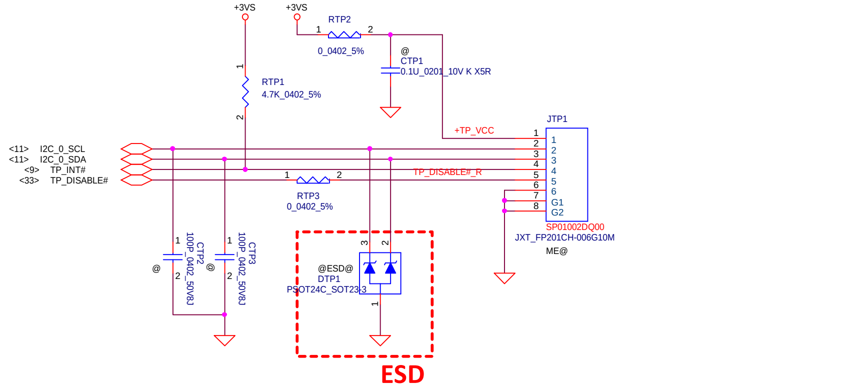
Size	Document Number	Rev
C	LA-G581P	0.1

Date: Monday, June 04, 2018 | Sheet 29 of 45

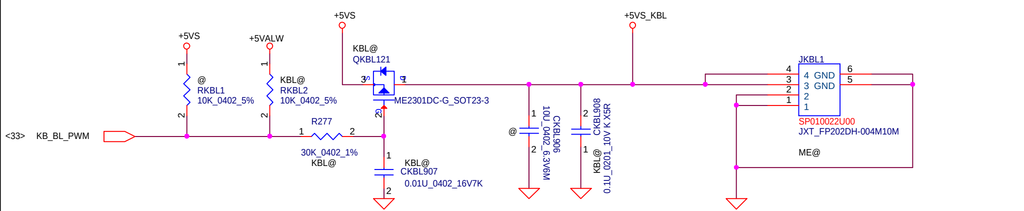
Finger printer



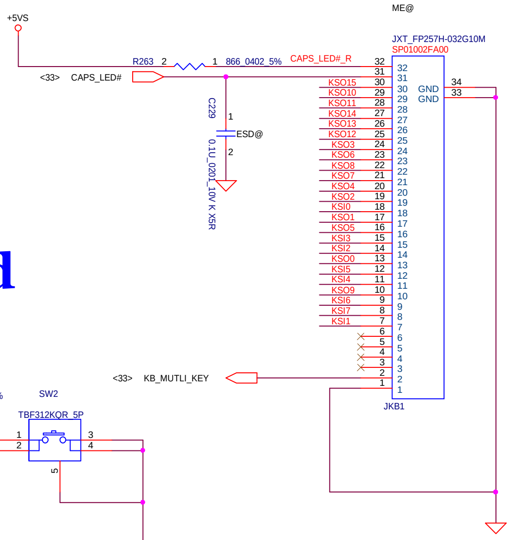
Touch Pad



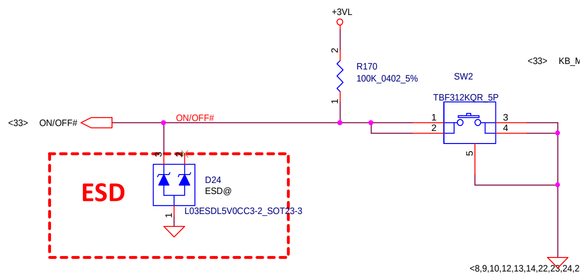
Keyboard Backlight

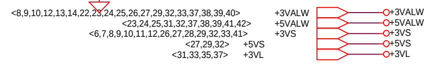


Keyboard

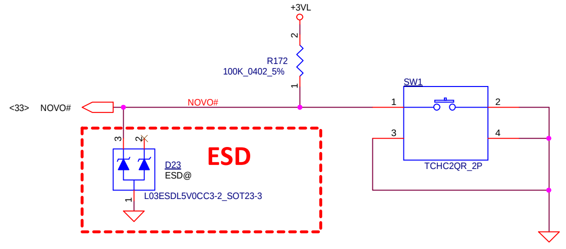


Power Button Pad

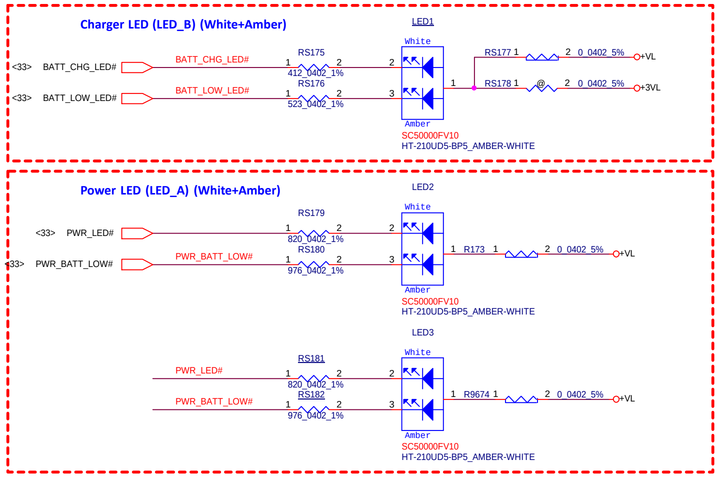




Novo Button



LED



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

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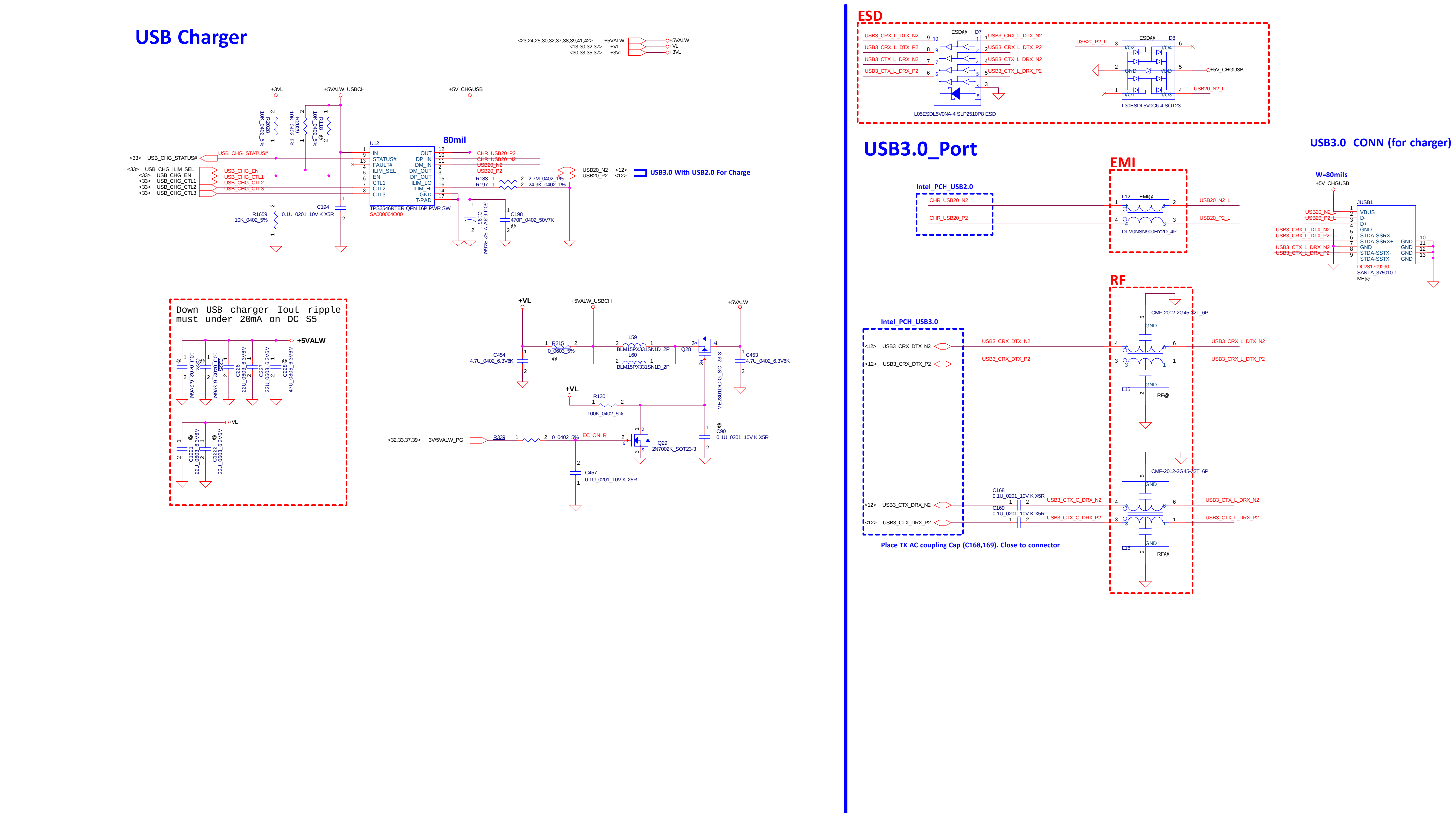
Compal Electronics, Inc.

Title	KB/KBD/LED/TP/HS Conn.		
Size C	Document Number LA-G581P		Rev 0.1
Date: Monday, June 04, 2018	Sheet 30 of 45		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/02/06	Deciphered Date 2020/5/17	Title: USB3.0 W/ Charger
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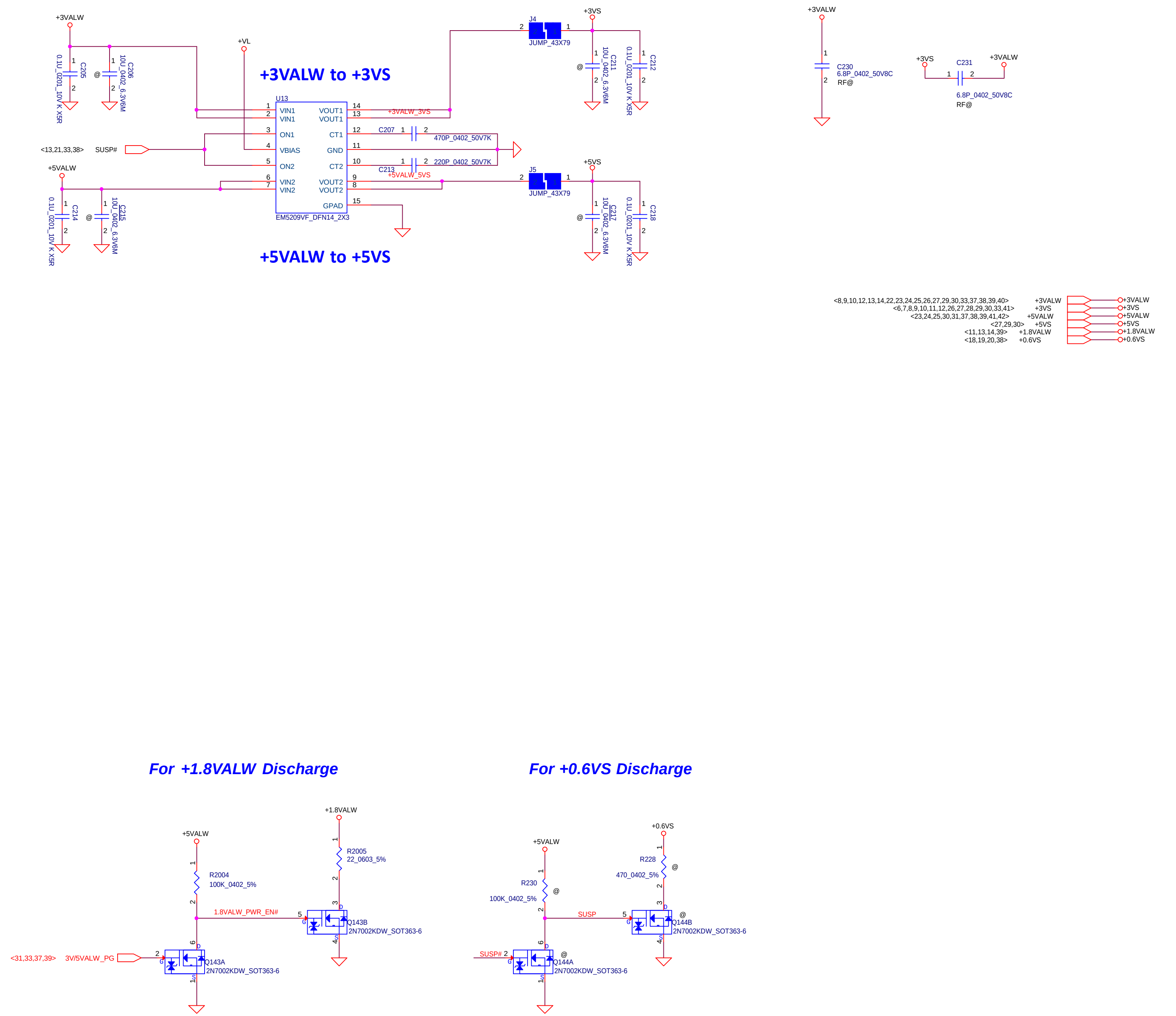
			Date: Monday, June 04, 2018; Sheet 31 of 45



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

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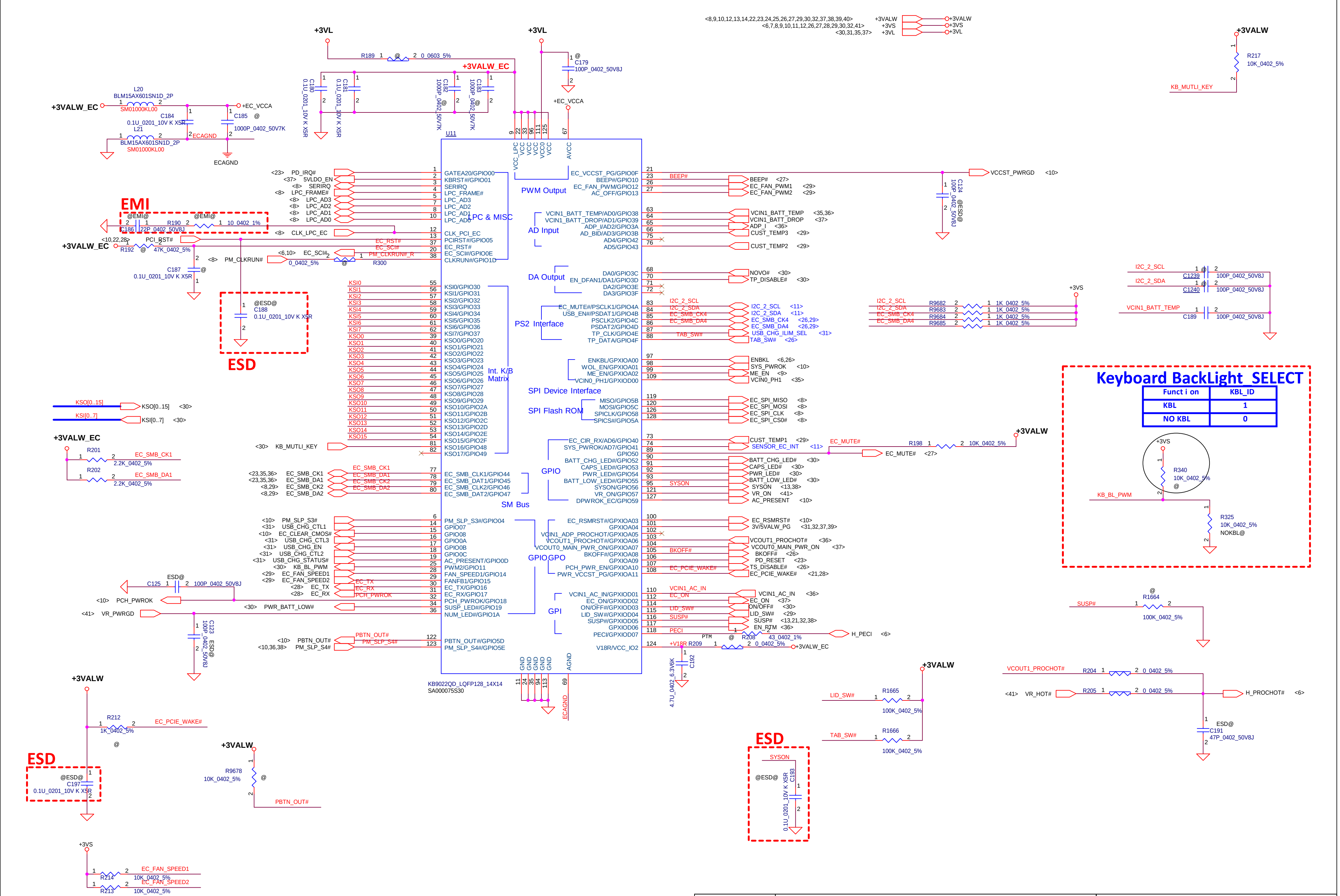
Compal Electronics, Inc.

Title: **DC to DC**

Size: C | Document Number: **LA-G581P** | Rev 0.1

Date: Monday, June 04, 2018 | Sheet 32 of 45



Security Classification	Compal Secret Data		
Issued Date	2018/02/06	Deciphered Date	2020/5/17

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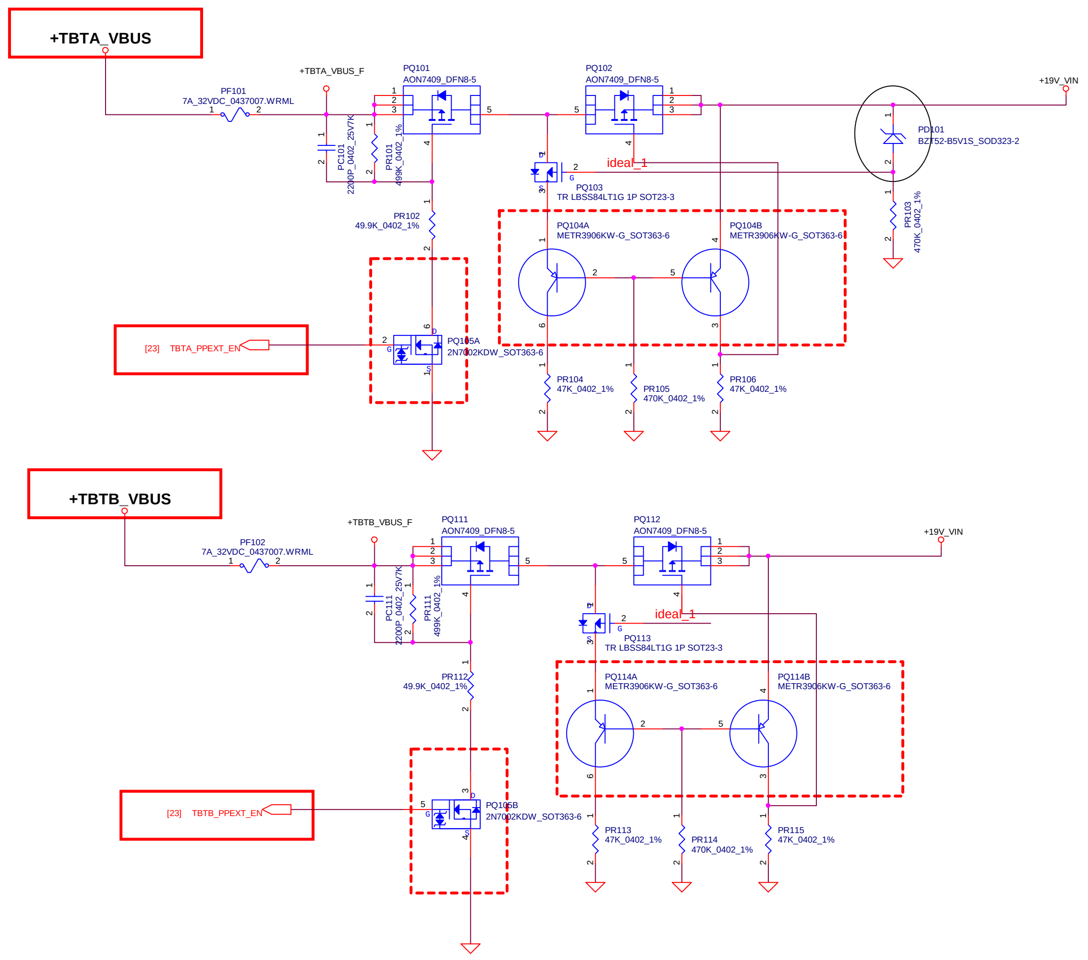
Compal Electronics, Inc.

Title: EC KB9022

Size: C | Document Number: LA-G581P | Rev: 0.1

Date: Monday, June 04, 2018 | Sheet 33 of 45



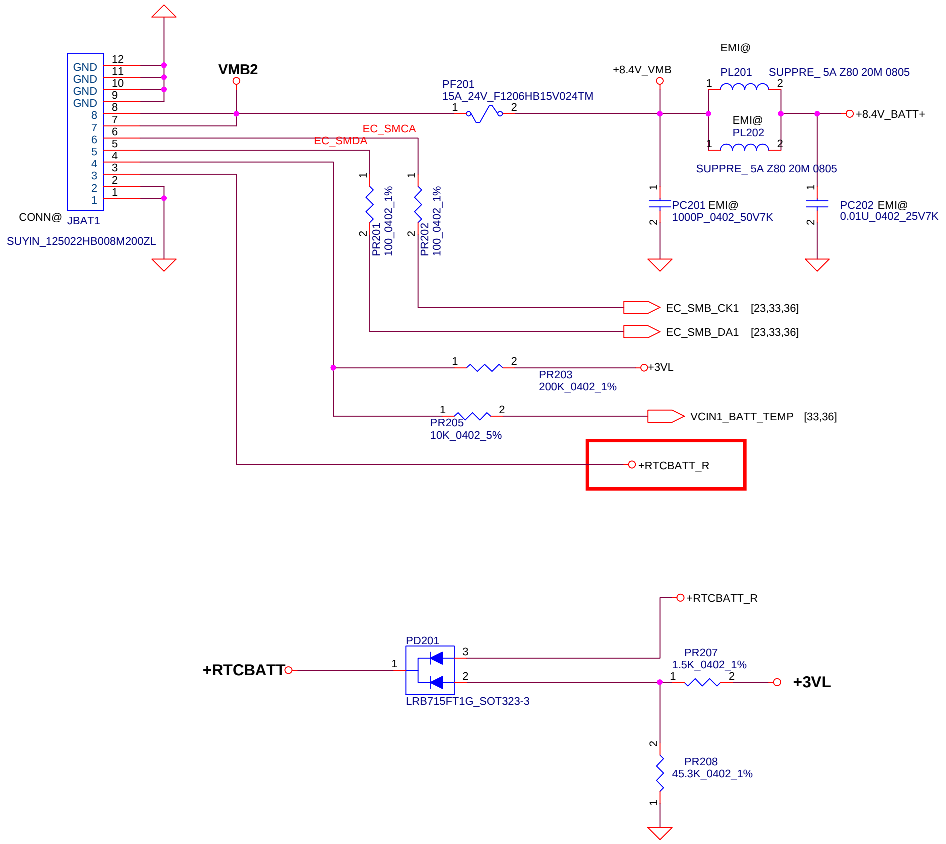
Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

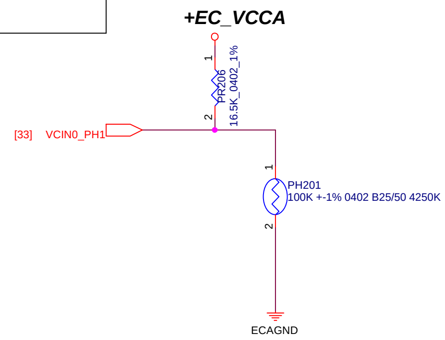
Title: **TYPE-C IN**

Size: Custom | Document Number: **LA-E5513P** | Rev: 0.1

Date: Monday, June 04, 2018 | Sheet 34 of 45



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



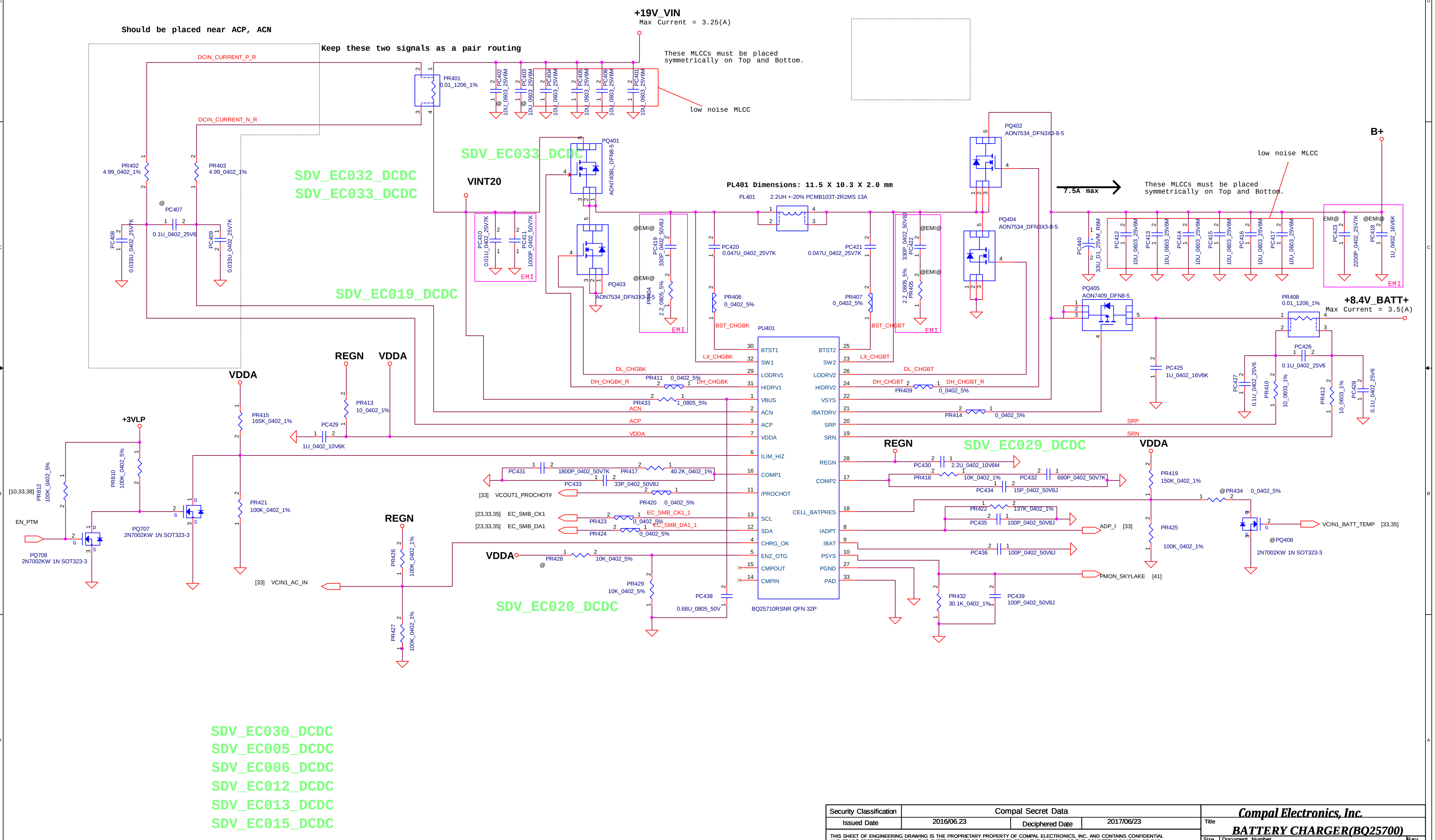
Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	LAE551P	0.1

Date: Monday, June 04, 2018 | Sheet 35 of 45



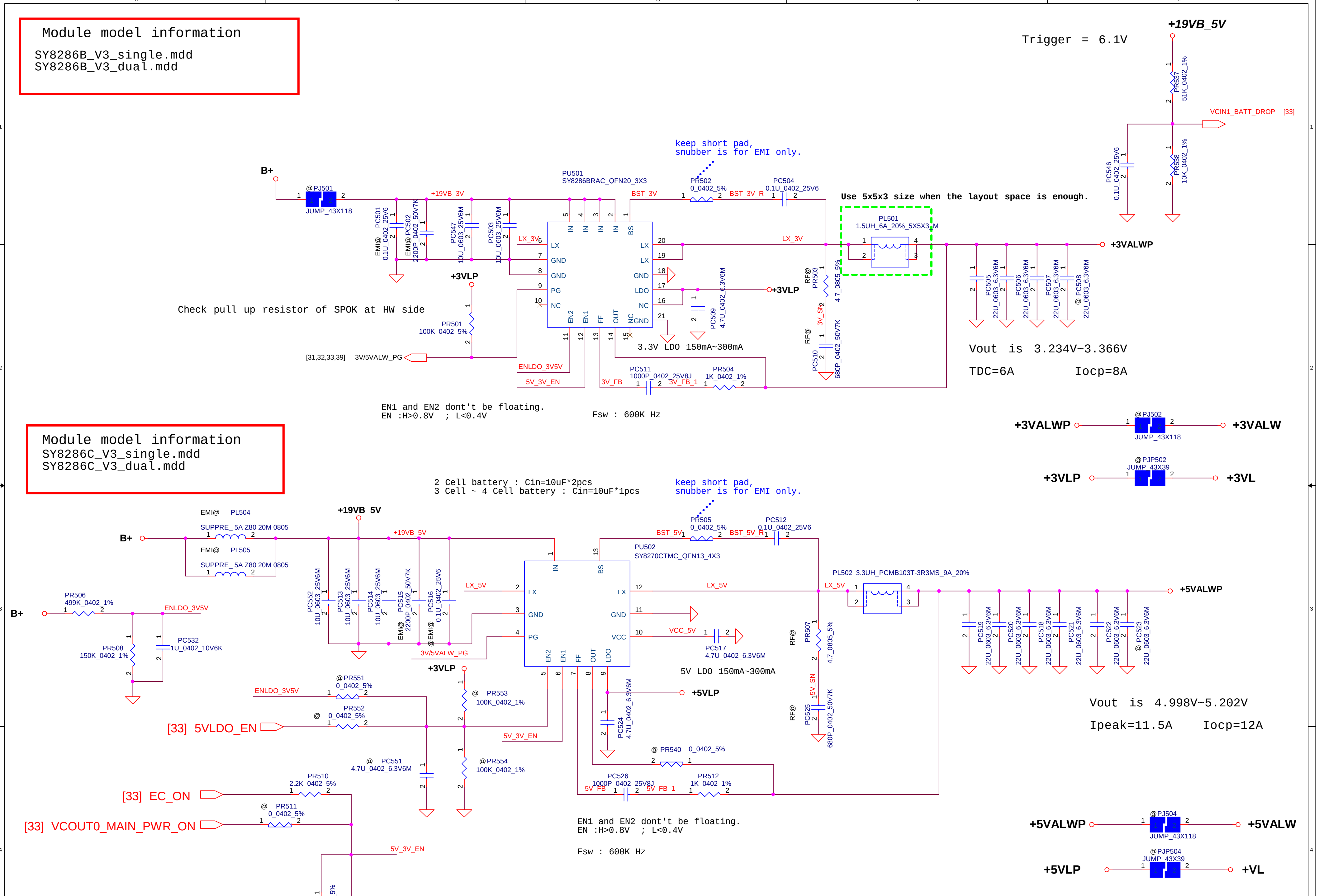
Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

Title: **BATTERY CHARGER(BQ25700)**

Size: Custom | Document Number: LA-E5513P | Rev: 0.1

Date: Monday, June 04, 2018 | Sheet 36 of 45



Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

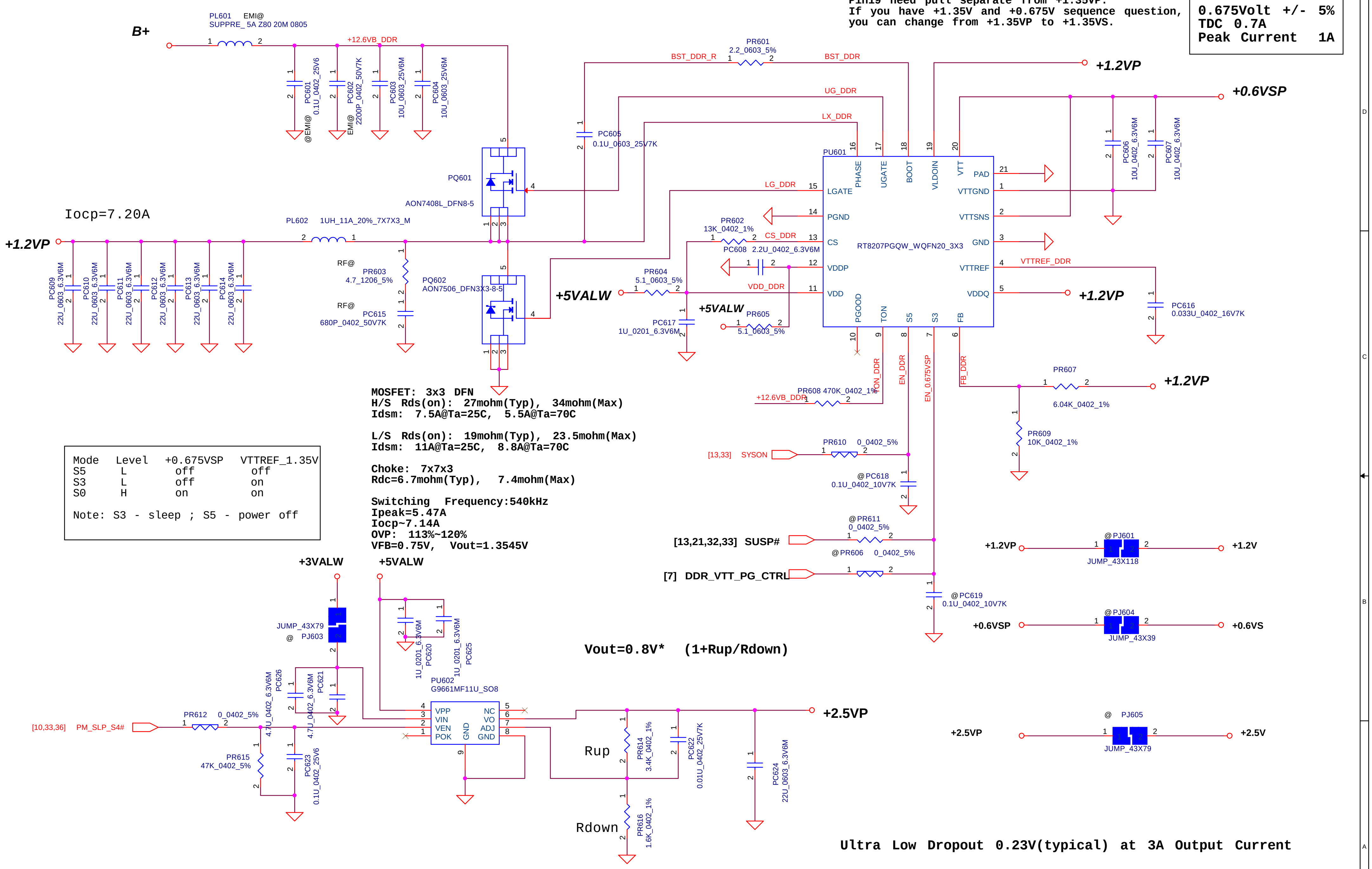
Title
+3VALW/+5VALW

Size Custom | Document Number | Rev 0.1

Date: Monday, June 04, 2018 | Sheet 37 of 45

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/-	5%
TDC 0.7A	
Peak Current	1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=5.47A
Iocp~7.14A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Vout=0.8V* (1+Rup/Rdown)

Ultra Low Dropout 0.23V(typical) at 3A Output Current

Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

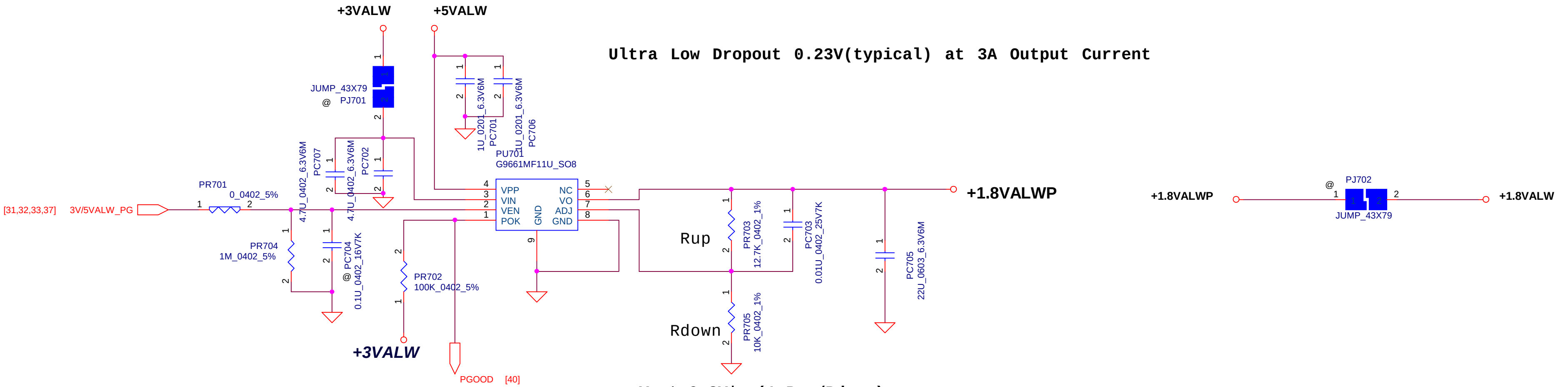
Compal Electronics, Inc.

Title: **RT8207P**

Size: Custom | Document Number | Rev 0.1

Module model information

APL5930_V2.mdd

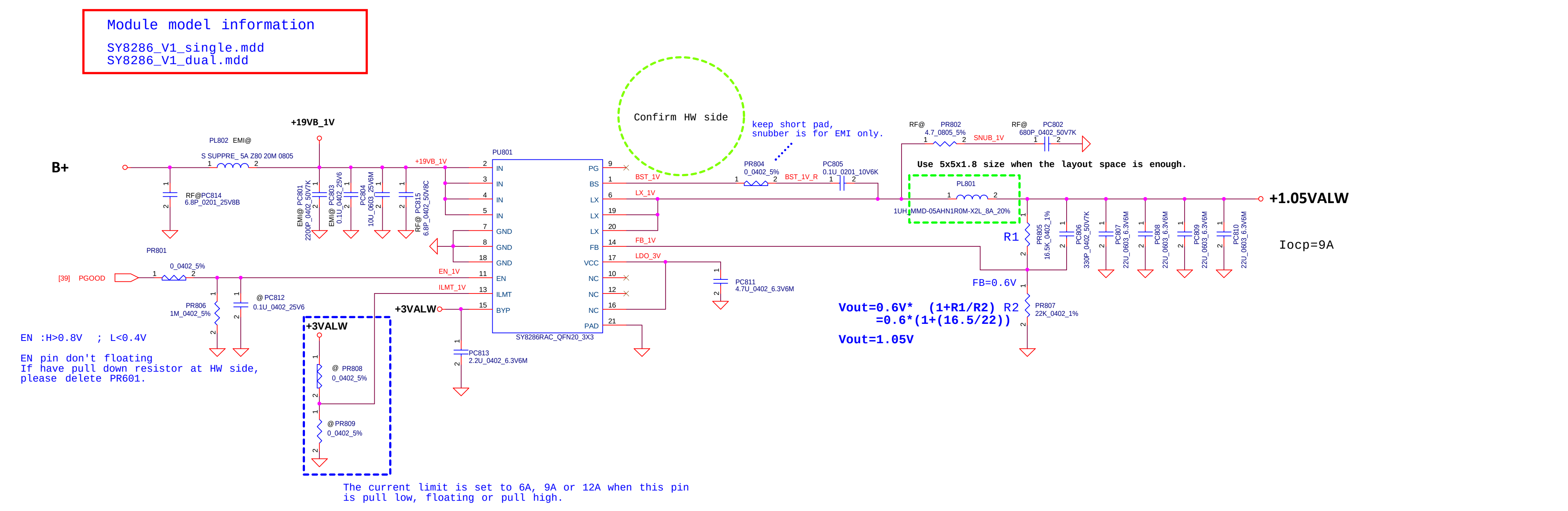


Vout=0.8V* (1+Rup/Rdown)

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2016/06.23	Deciphered Date	2017/06/23	Title: APL5930

Size: Custom | Document Number | Rev 0.1

Date: Monday, June 04, 2018 | Sheet 39 of 45



Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

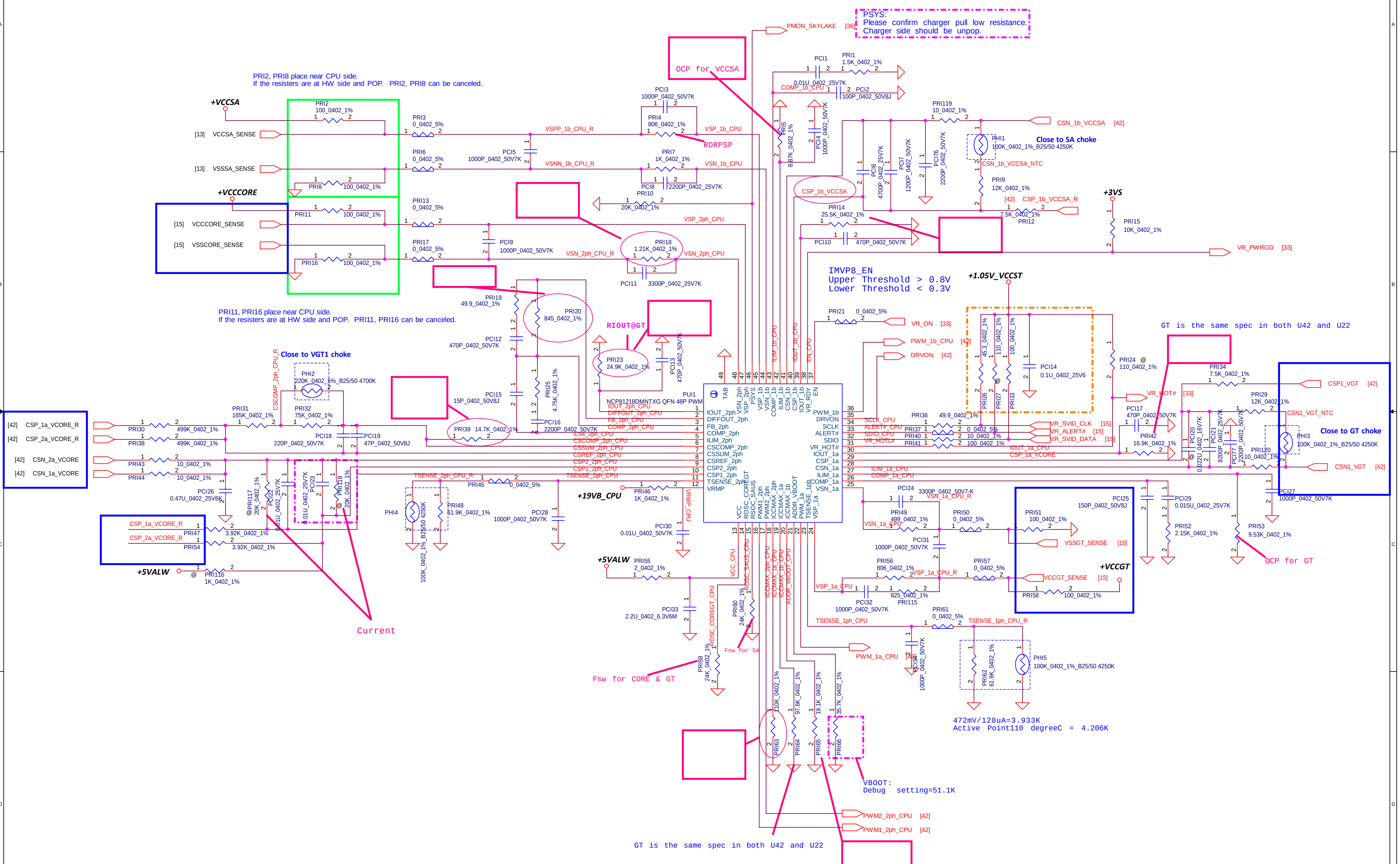
Compal Electronics, Inc.

Title: SY8286

Size: C | Document Number | Rev: 0.1

Date: Monday, June 04, 2018 |

CPU CORE



Title	NCP81218(U22&U42)	
Size	Document Number	Rev 0.1
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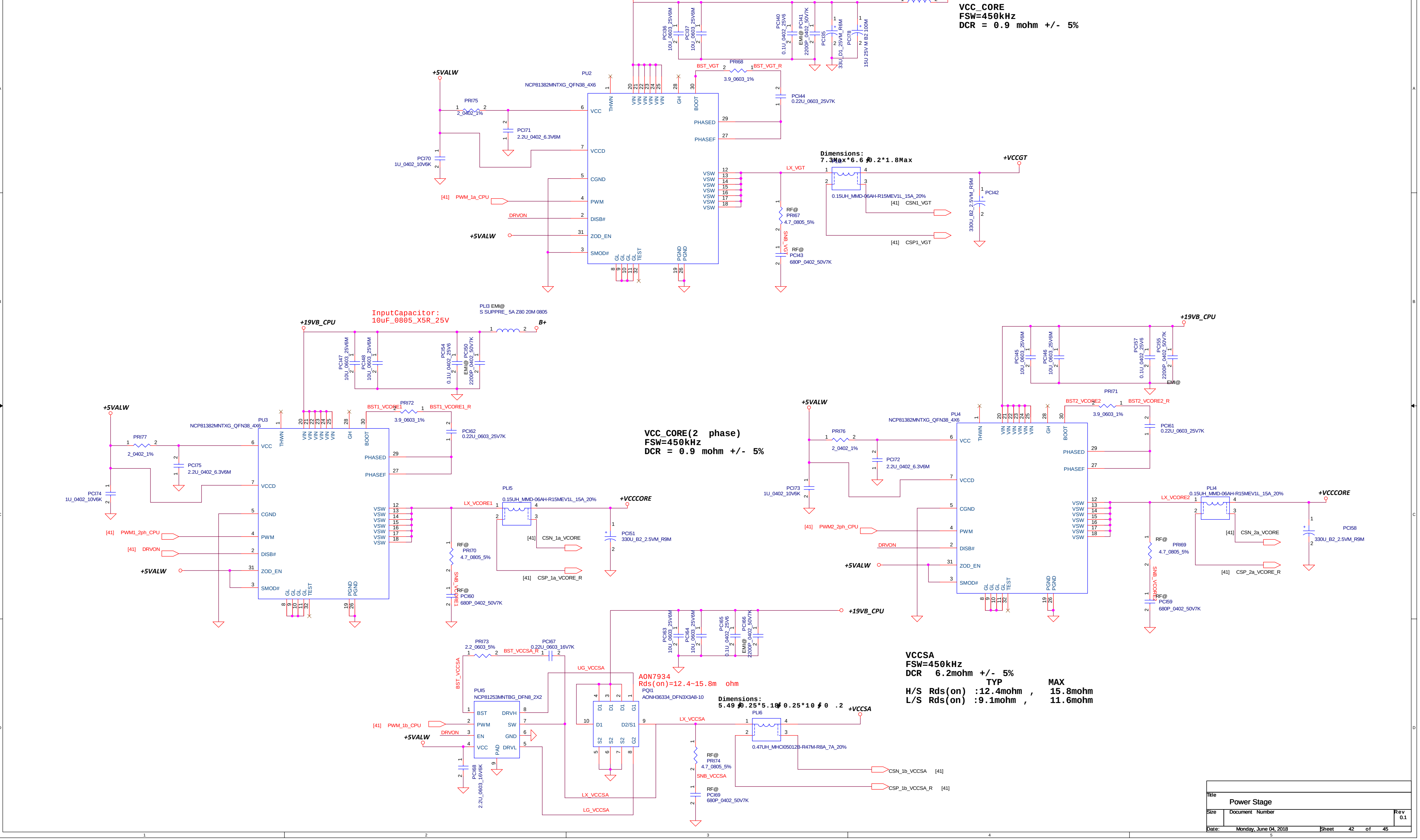
CPU POWER STAGES



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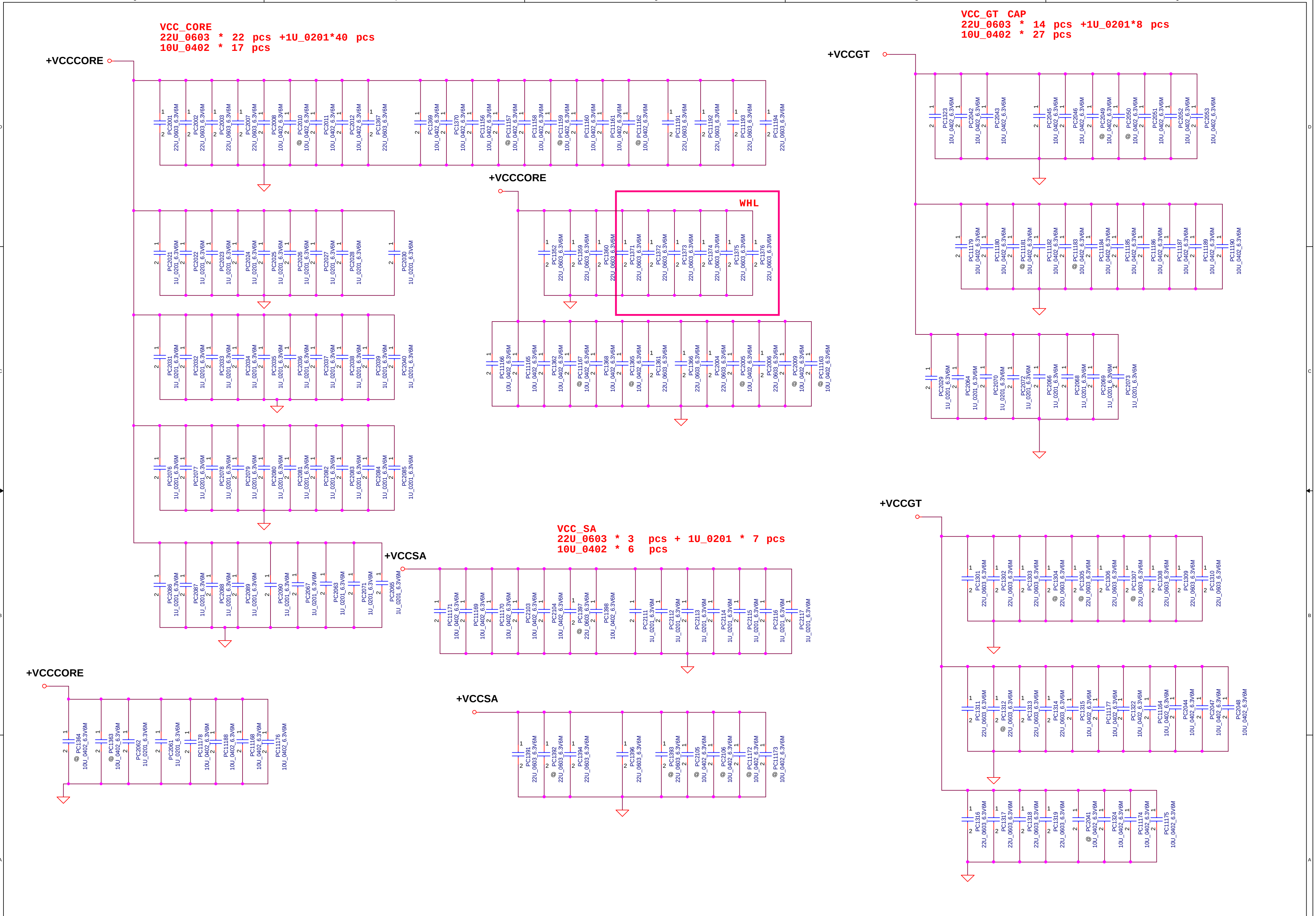

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