LCFC Confidential

Y550 M/B Schematics Document

Comet Lake H-Processor with DDR4 + NV GN20P- GPU

2021-04-06

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: Cover Page		
Size: Custom	Document Number: Y550-CML GN20P	Rev: 1.0
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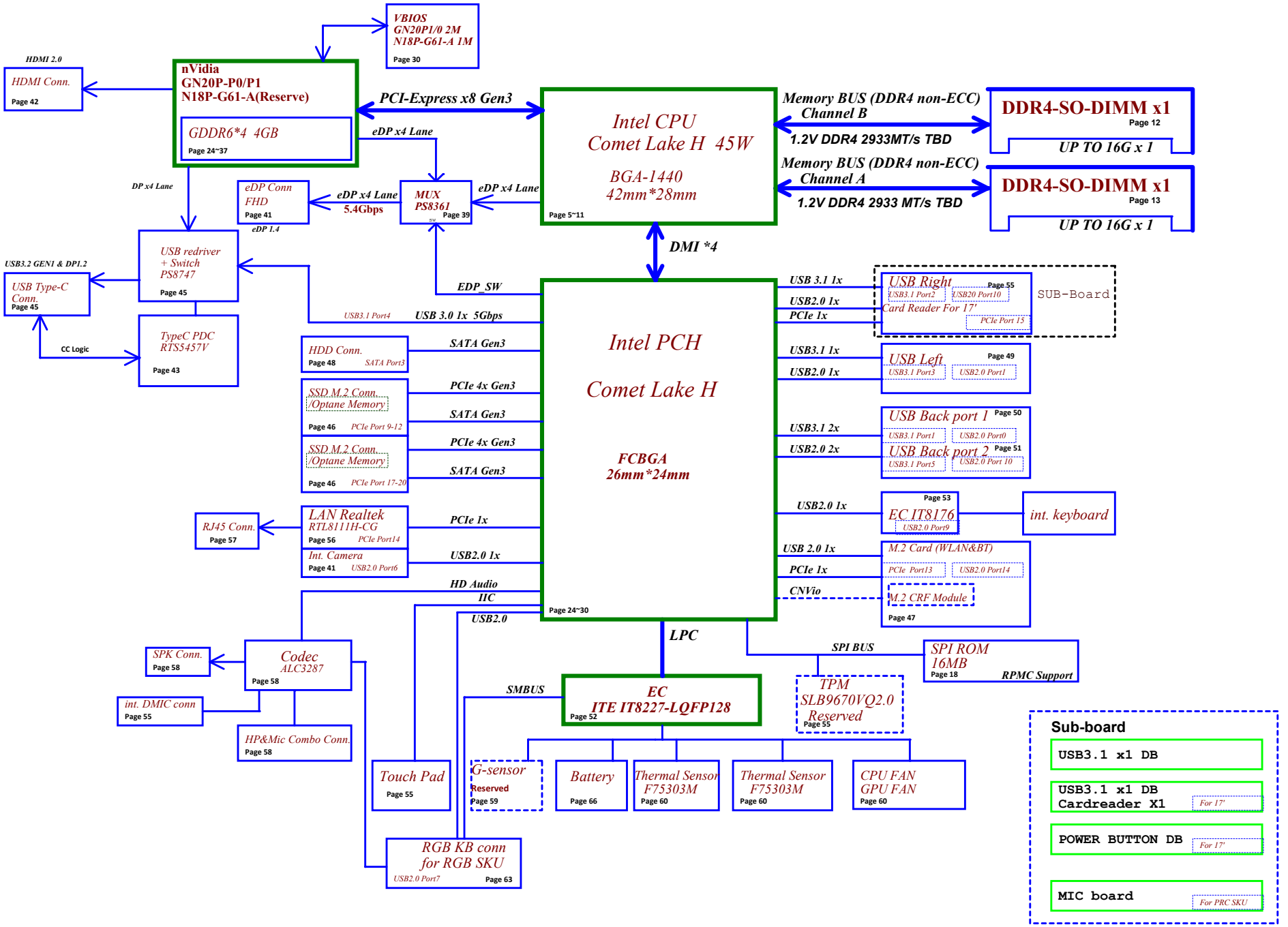

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
i5@i7@i9@	CPU Part
PRC@	PRC
WW@	Worldwide
OPT@	NV GPU part
M4GX4@S4GX4@	VRAM part
N18PG61@	N18PG61 PART
N18PG62@	N18PG62 PART
GYSNC@	GSYNC support part
DDS@	Dynamic Display Switch part
MUX@	EDP MUX Switch part
MUX1@	Colay DDS and MUX
HDMI@	HDMI logo
CNVI@	CNVi support part
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
EMC_8111H@	LAN 8111H EMC Part
AG@	Anti-ghost Part
BL@	BL Part
RGB@	RGB Part
MP@	Mass Production Stage Part

BOM Structure	BTO Item
USB@	USB2.0 port1 for USB Port
NPI@	NPI stage stuff
DCI@	DCI
Debug@	USB2.0 port 1for Debug
TPM@	For support TPM sku part
GS@	Reserved for G-sensor
OPTANE@	For Optane SKU stuff
MIRROR@	MIRROR
NOMIRROR@	No MIRROR
ME@	ME part(connector)
EMC@	EMC part
EMC_NS@	EMC not stuff
RF@	RF part
RF-NS@	RF No part
CD@	Cost down part
UP9632_@	UP9632 part stuff

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7	RGB
8	NA
9	AG
10	Back USB3.0
11:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Right USB3.0(DB)
3	Left USB3.0
4	Type-C Port
5	Back USB3.0
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	NA
1B	NA
2	NA
3	HDD Gen3
4	NA
5	NA
7	NA

PCIE Port table	
Port	Function
1:8	NA
9:12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15	Card Reader
17:20	M.2 SSD/Optane

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Title: **Notes List**

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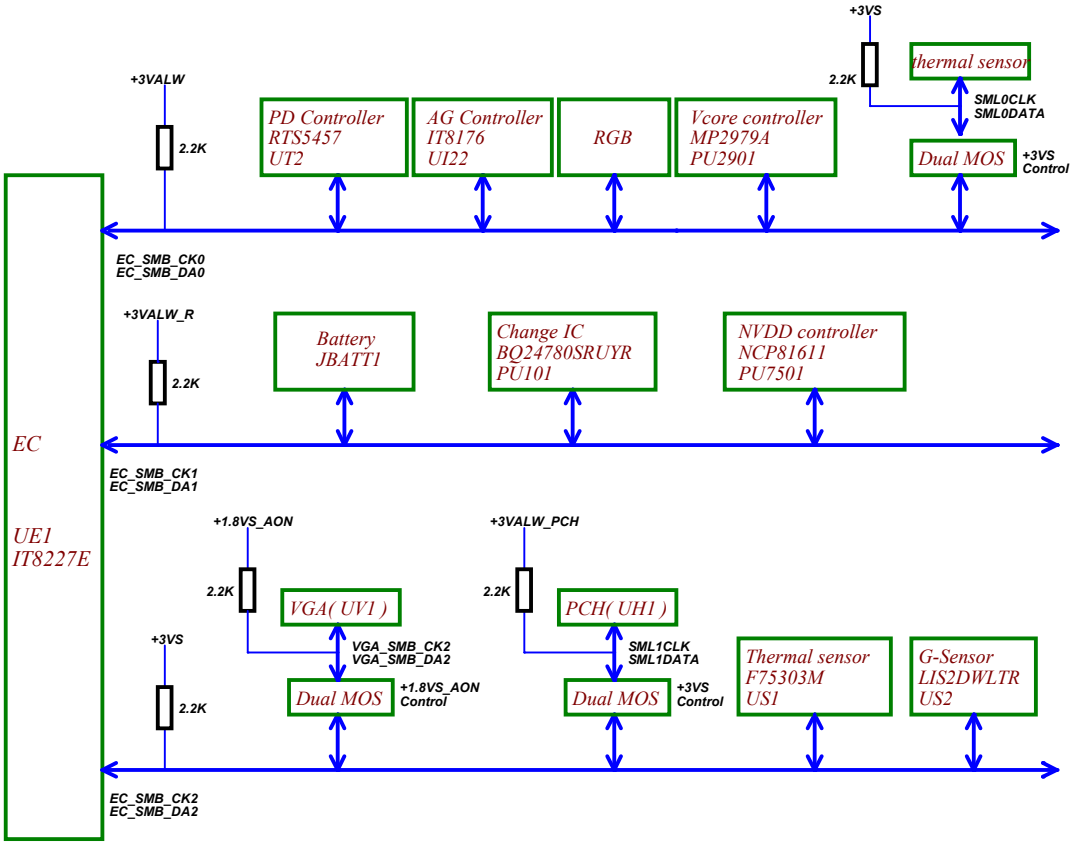


SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HiFi Audio	Anti-ghost
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS Reserve	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

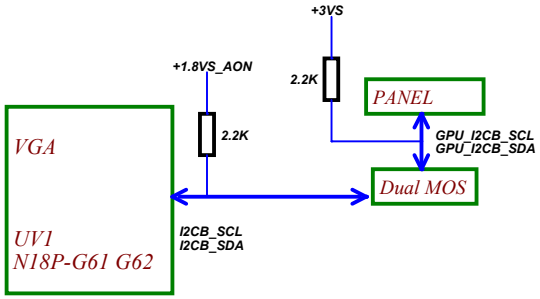
Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default) Need to update
PCH	
Thermal Sensor NCT7718W	1001100xb

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update



Security Classification	LC Future Center Secret Data		Title: I2C Block
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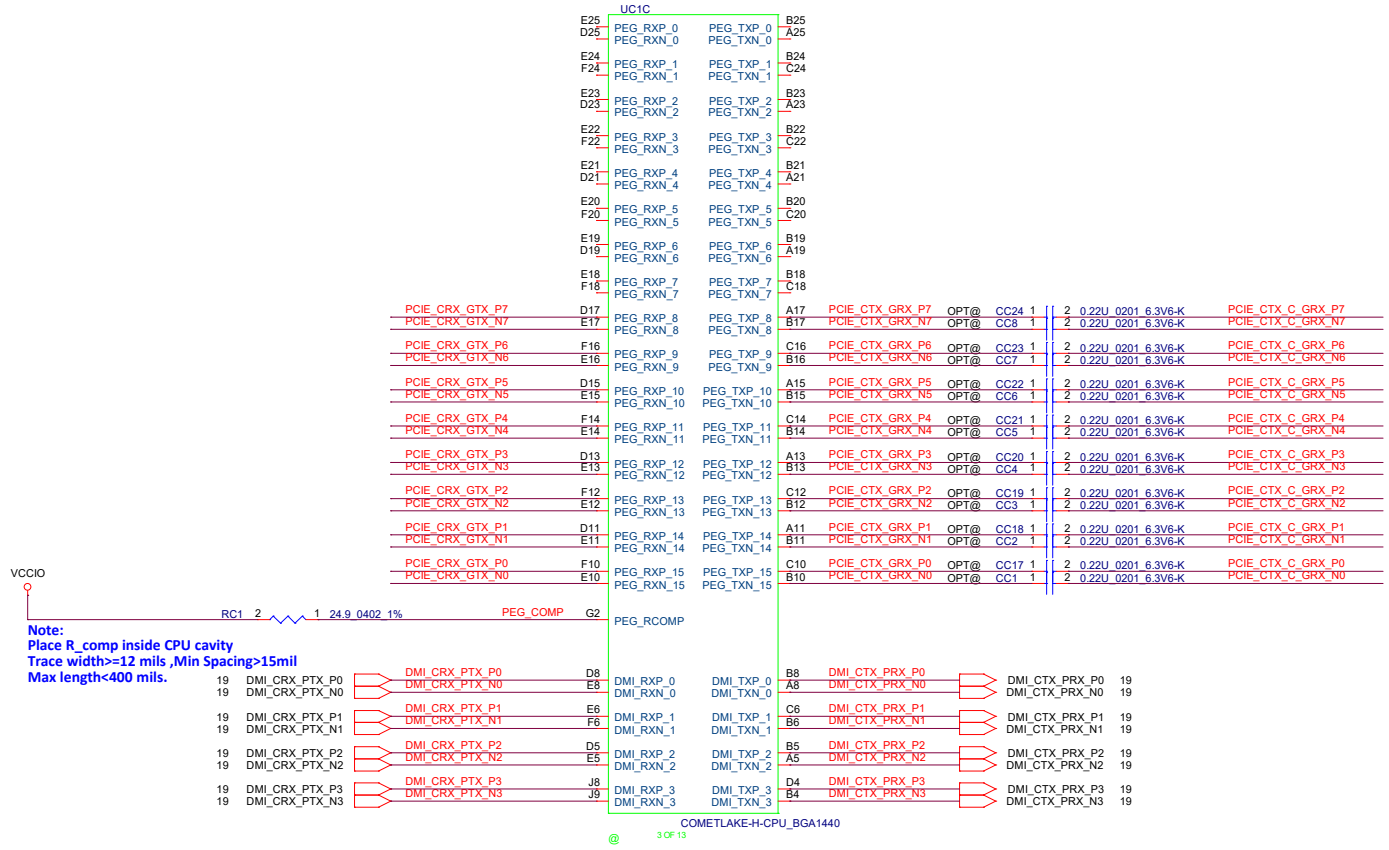
26 PCIE_CRX_GTX_N[0..7]

26 PCIE_CRX_GTX_P[0..7]

PCIE_CTX_C_GRX_N[0..7] 26

PCIE_CTX_C_GRX_P[0..7] 26



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (1/7) DMI,PEG

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CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation * 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. * 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* * 11 = 1 x16 PCI Express*

PEG Training	
CFG7	* 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.

Reserved configuration lane	
CFG[19:8]	N/A

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Title	CPU (2/7) PM, XDP, CLK, CFG		
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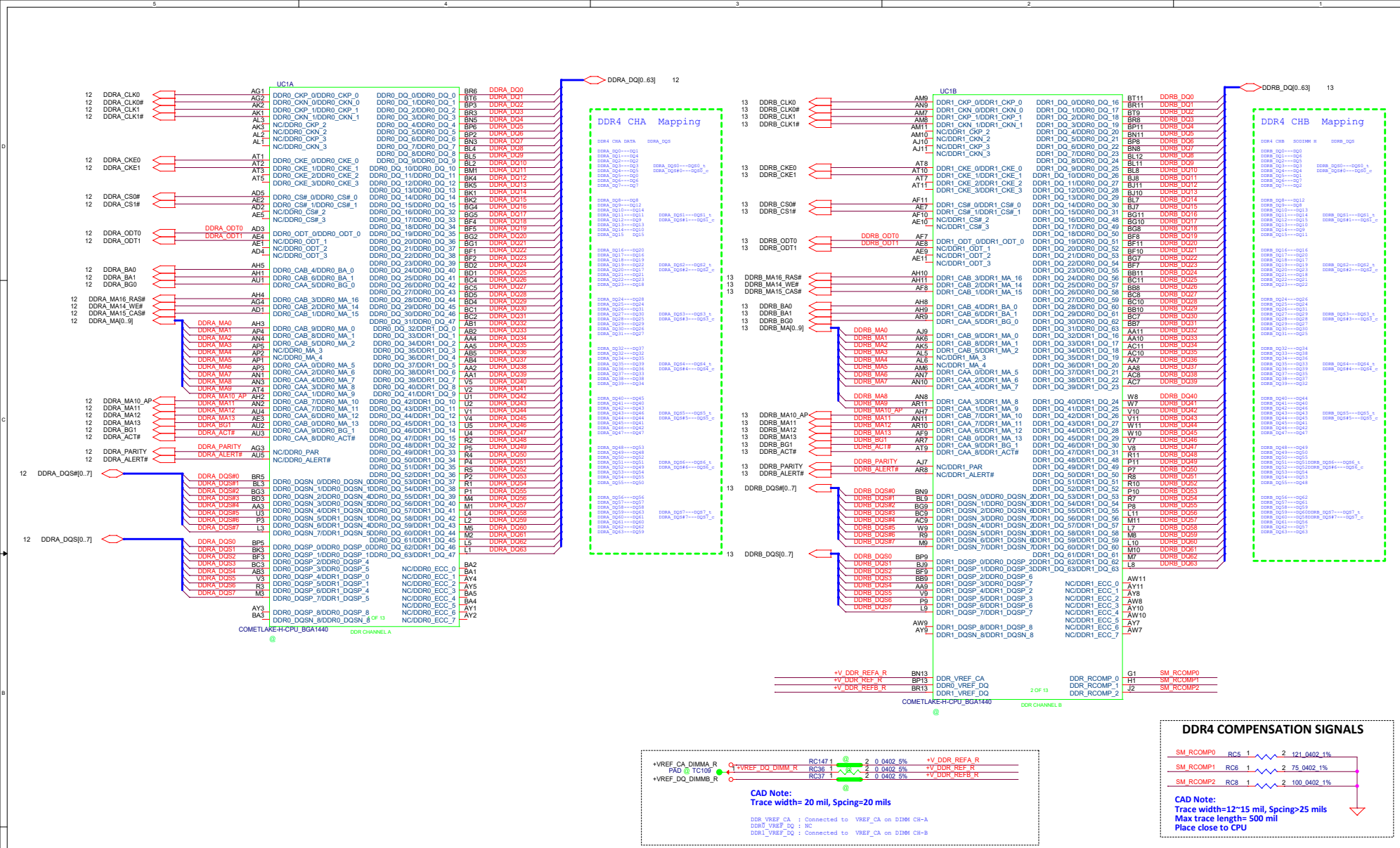

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	CPU (3/7) DDRVI		
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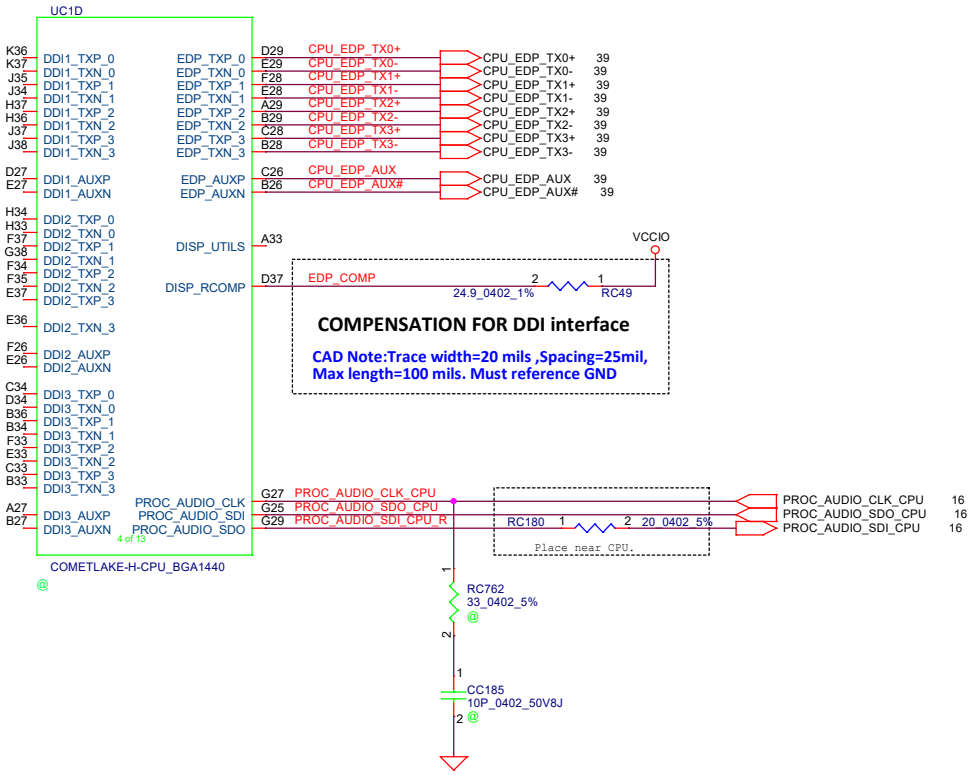

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
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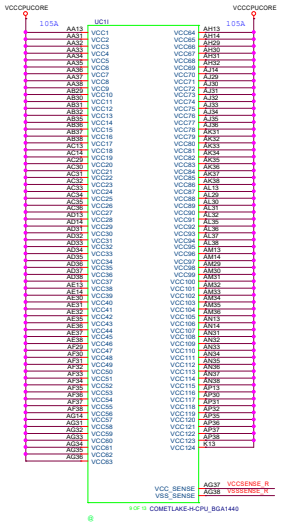
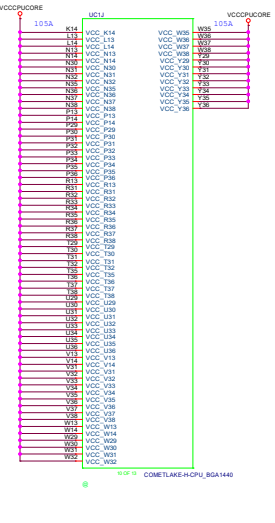
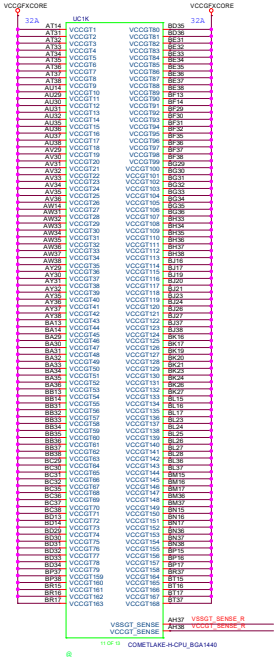
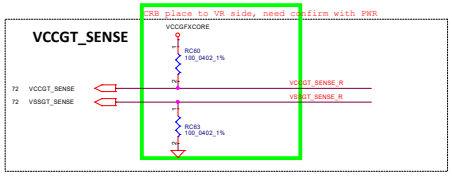
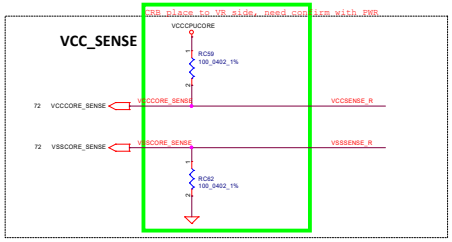




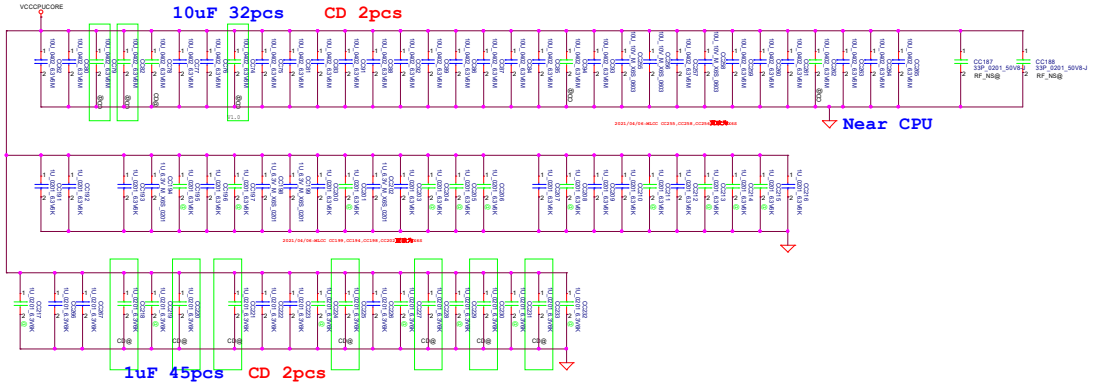


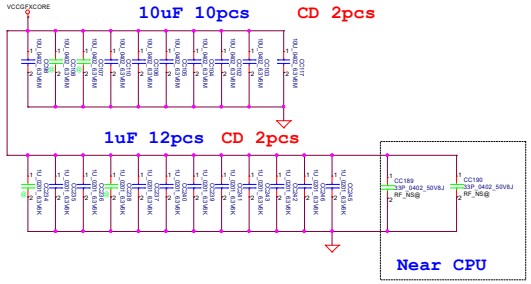




PDG near: 470uf*4 47uf*20
Backside:10uf*32 1uf*45

PDG near: 470uf*4 47uf*20
Backside:10uf*32 1uf*45





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Title	CPU (5/7) PWR, BYPASS		
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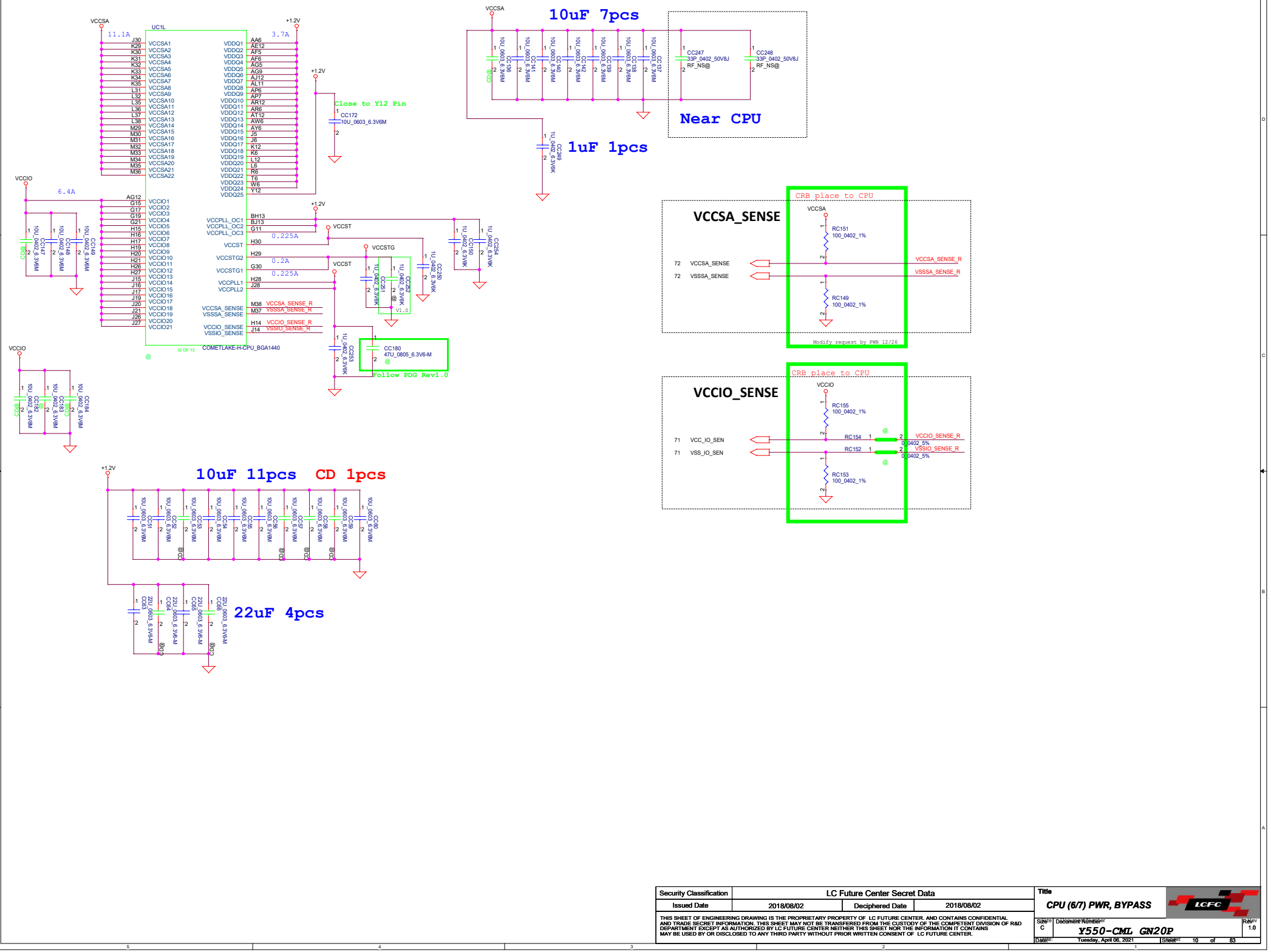

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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	CPU (6/7) PWR, BYPASS		
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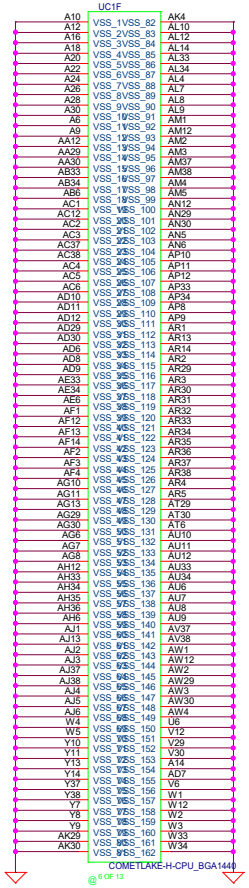

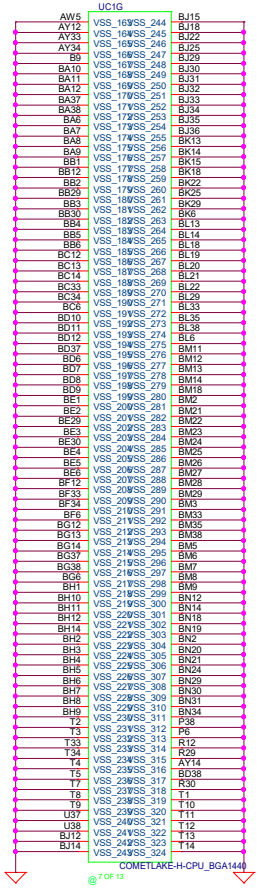

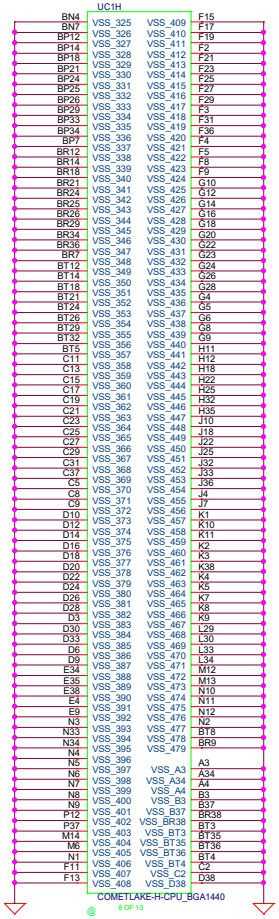

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU (6/7) PWR, VSS

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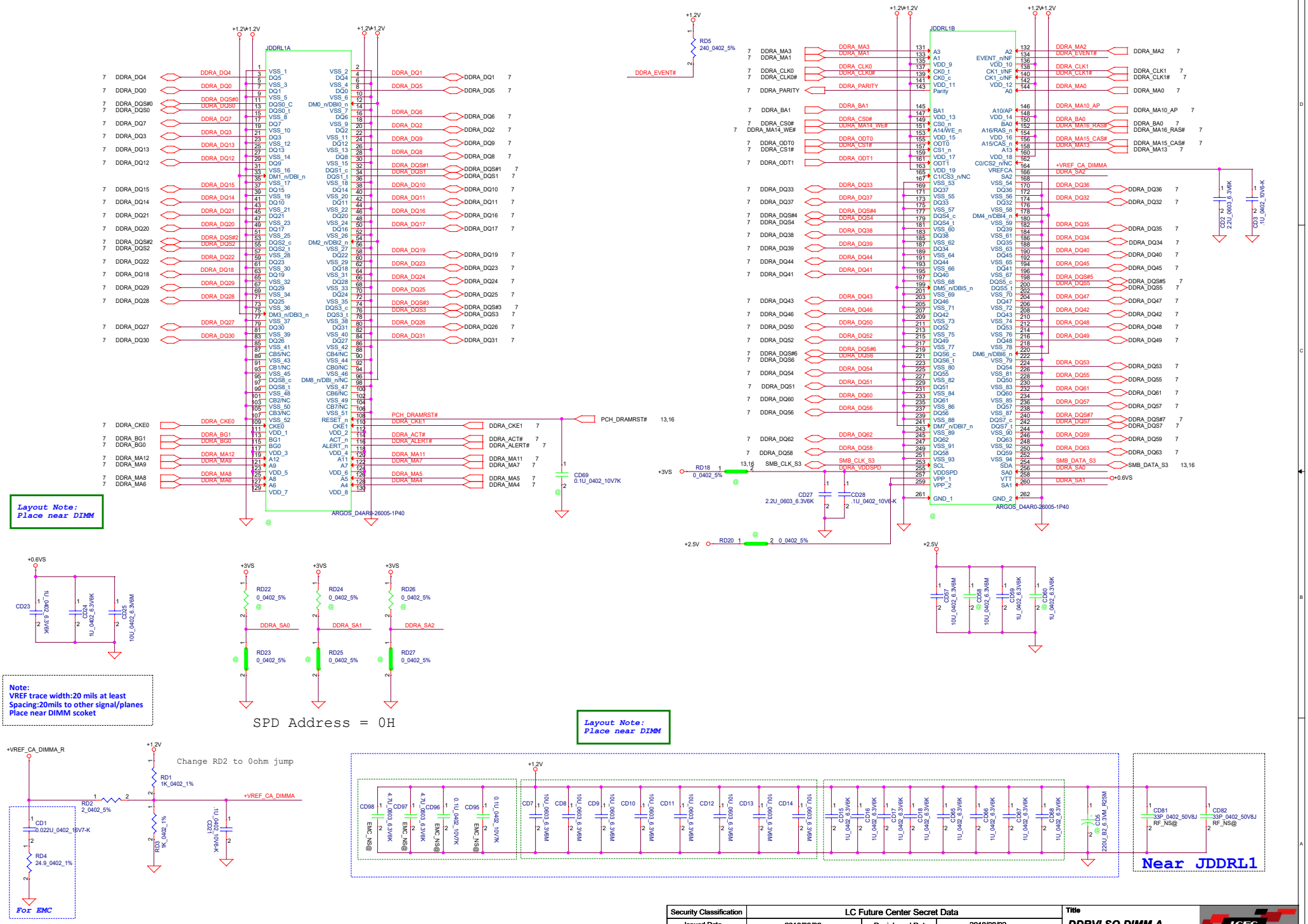
DDR4 SO-DIMM A



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Title	DDRVI SO-DIMM A		
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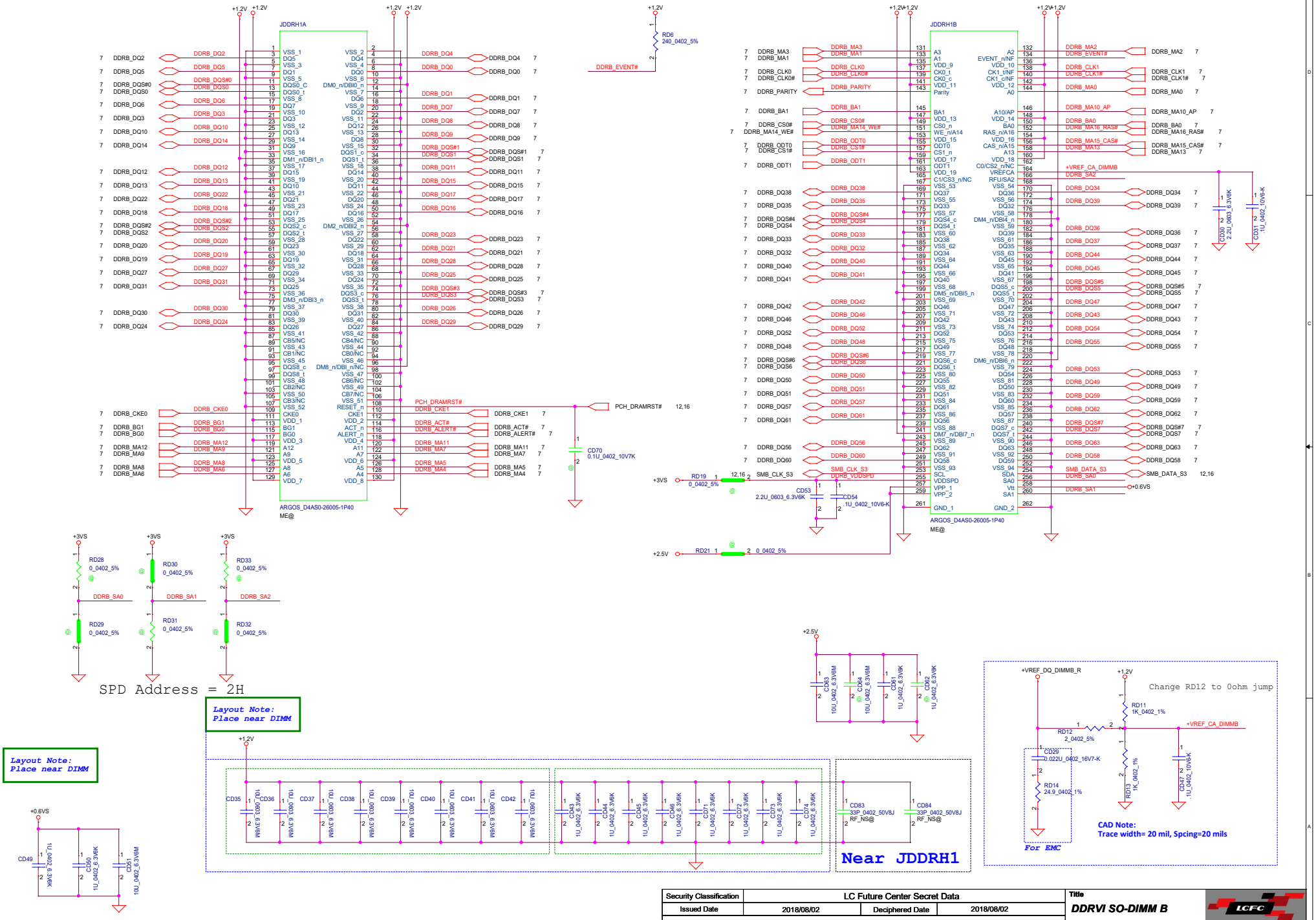
DDR4 SO-DIMM B



Security Classification	LC Future Center Secret Data		
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Title	DDRVI SO-DIMM B
Size	C
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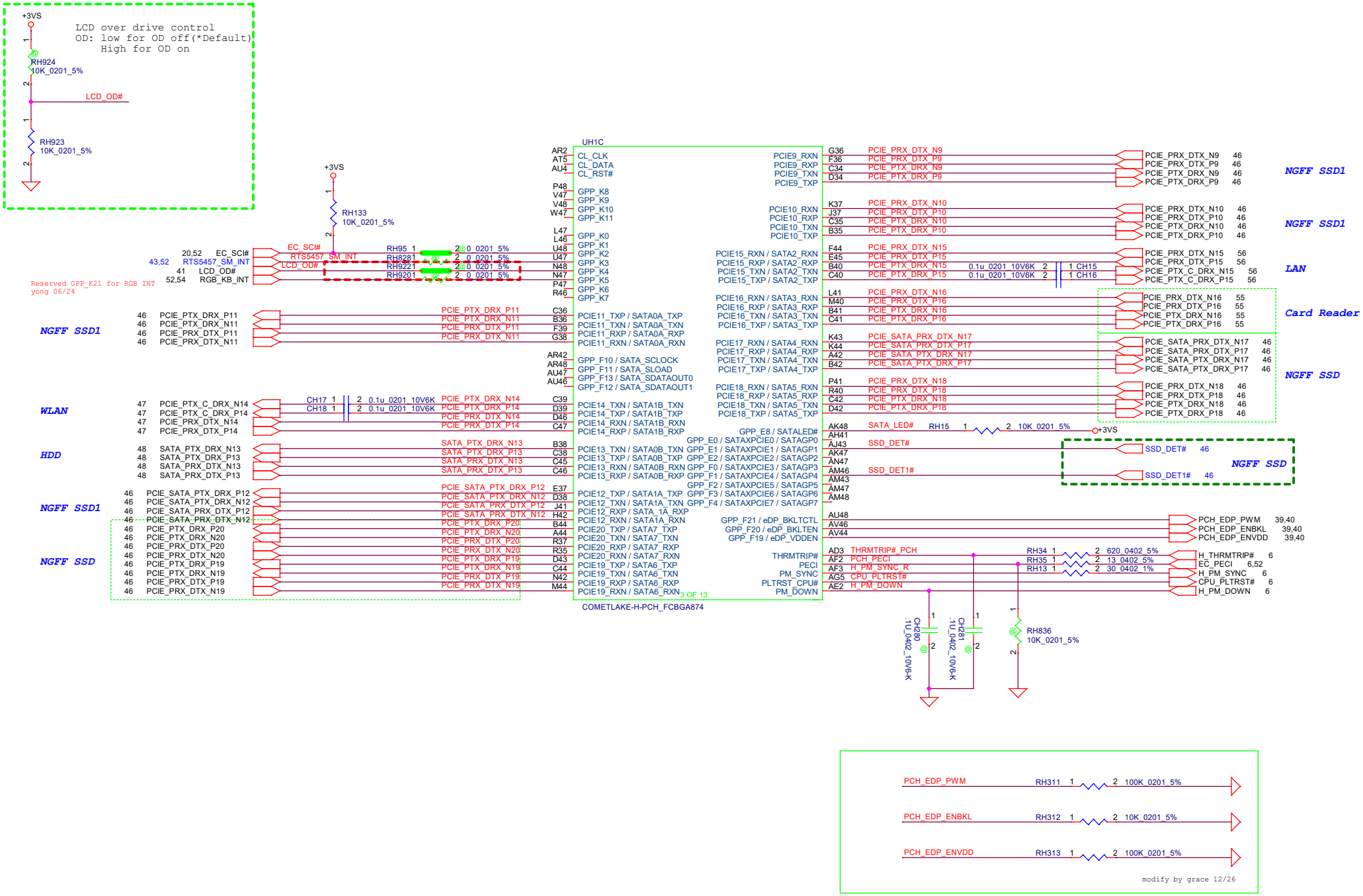

Security Classification	LC Future Center Secret Data		
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Title: PCH (1/9) PCIe/SATA/GPPFG

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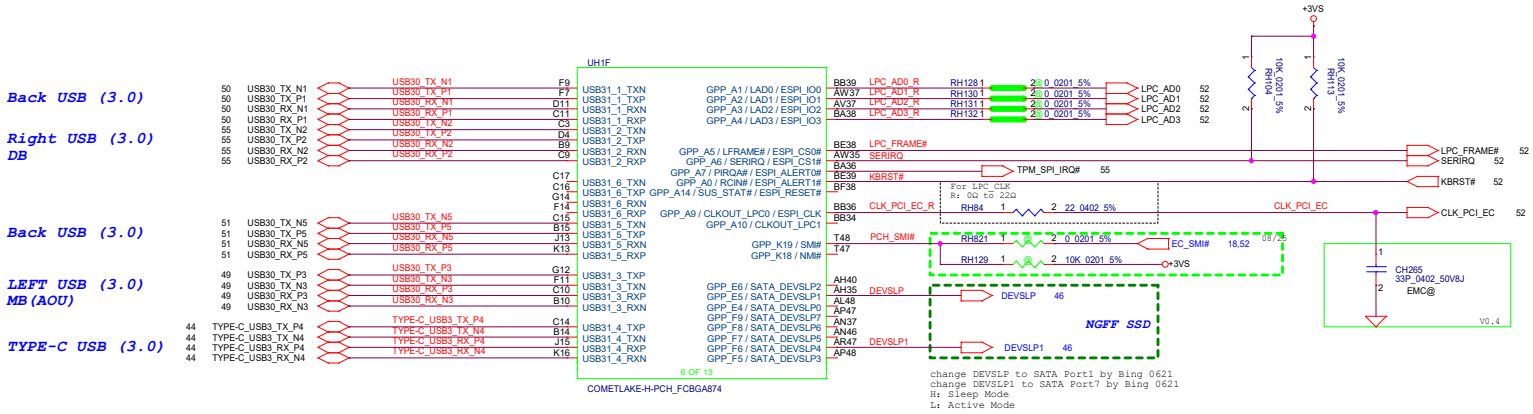

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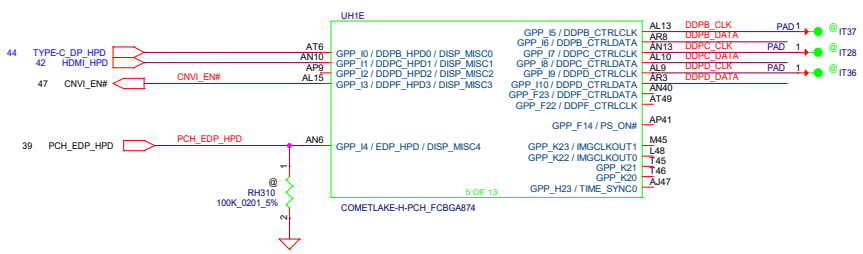

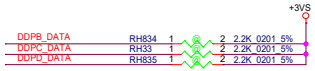

DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
★ L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
★ L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
★ L Port D is not detected. (Default)

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Title	PCH (2/9) USB3/GPPAEFGHI		
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HDA_SDO This signal has a weak internal pull-down.
* 0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
* 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.(Default)

GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
* 0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

GPP_B23 /SML1ALERT# /PCHHOT#
* 0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

+3VALW_PCH
RH25 1K_0201_5%
52 ME_FLASH
RH9 0_0201_5%
58 PCH_HDA_BIT_CLK
58 PCH_HDA_SDIN0
58 PCH_HDA_SDOUT
58 PCH_HDA_SYNC
RH805 33_0402_5%
RH806 33_0402_5%
RH804 33_0402_5%
HDA_BIT_CLK
HDA_SDOUT
HDA_SYNC
PLACE NEAR PCH
PAD TH39
HDA_RST#

UH1D
HDA_BCLK / I2S0_SCLK
HDA_SDI0 / I2S0_RXD
HDA_SDO / I2S0_TXD
HDA_SYNC / I2S0_SFRM
HDA_RST# / I2S1_SCLK
HDA_SDI1 / I2S1_RXD
I2S1_TXD / SNDW2_DATA
I2S1_SFRM / SNDW2_CLK
BD11 BE11 BF12 BG13 BE10 BF10 BE12 BD12

PLACE NEAR PCH
8 PROC_AUDIO_SDO_CPU
8 PROC_AUDIO_SDI_CPU
8 PROC_AUDIO_CLK_CPU
RH754 30_0402_5%
RH755 30_0402_5%
PROC_AUDIO_SDO_PCH
PROC_AUDIO_CLK_PCH
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
AM2 AN3 AM3

CNVI_MODEM_CLKREQ
CNVI_RF_RESET#
GPP_D8 / I2S2_SCLK
GPP_D7 / I2S2_RXD
GPP_D6 / I2S2_TXD / MODEM_CLKREQ
GPP_D5 / I2S2_SFRM / CNV_RF_RESET#
GPP_D20 / DMIC_DATA0 / SNDW4_DATA
GPP_D19 / DMIC_CLK0 / SNDW4_CLK
GPP_D18 / DMIC_DATA1 / SNDW3_DATA
GPP_D17 / DMIC_CLK1 / SNDW3_CLK
AV18 AW18 BA17 BE16 BF15 BD16 AV16 AW15

52 PCH_RTCRST#
PCH_RTCRST#
PCH_SRTCRST#
RTCRST#
SRTCRST#
BE47 BD46

52 PCH_PWROK
52,61 EC_RSMRST#
RH12 0_0201_5%
RH14 0_0201_5%
PCH_PWROK_R
PCH_RSMRST#_R
PCH_PWROK
RSMRST#
AY42 BA47

RH239 0_0201_5%
PCH_DPWROK_R
DSW_PWROK
AW41

52,60 SMB1_ALERT#
SMB_ALERT#
PCH_SMBCLK
PCH_SMBDATA
SMB0_ALERT#
SMLOCLK
SMLODATA
SML1CLK
SML1DATA
SML1ALERT#
SML1CLK
SML1DATA
BE25 BE26 BF26 BF24 BF25 BE24 BD33 BF27 BE27

GPP_C2 / SMBALERT#
GPP_C0 / SMBCLK
GPP_C1 / SMBDATA
GPP_C5 / SML0ALERT#
GPP_C3 / SML0CLK
GPP_C4 / SML0DATA
GPP_B23 / SML1ALERT# / PCHHOT#
GPP_C6 / SML1CLK
GPP_C7 / SML1DATA

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COMETLAKE-H-PCH_FCBGA874

GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8 / CLKRUN#
GPD11 / LANPHYPC
GPD9 / SLP_WLAN#
DRAM_RESET#
GPP_B2 / VRALERT#
GPP_B1 / GSPI1_CS1# / TIME_SYNC1
GPP_B0 / GSPI0_CS1#
GPP_K17 / ADR_COMPLETE
GPP_B1T / I2S_MCLK
SYS_PWROK
WAKE#
GPD6 / SLP_A#
SLP_LAN#
GPP_B12 / SLP_S0#
GPD4 / SLP_S3#
GPD5 / SLP_S4#
GPD10 / SLP_S5#
GPD8 / SUSCLK
GPD0 / BATLOW#
GPP_A15 / SUSACK#
GPP_A13 / SUSWARN# / SUSPWRDNACK
GPD2 / LAN_WAKE#
GPD1 / ACPRESENT
SLP_SUS#
GPD3 / PWRBTN#
SYS_RESET#
GPP_B14 / SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
BF36 AV32 BF41 BD42 BB46 BE32 BF33 BE29 R47 AP29 AU3 BB47 BE40 BE40 BC28 BF42 BE42 BC42 BE45 BF44 BE35 BC37 BG44 BG42 BD39 BE46 AU2 AW29 AE3 AL3 AH4 AJ4 AH3 AH2 AJ3

PM_CLKRUN#
PM_SLP_WLAN# 47
SYS_PWROK
WAKE#
SLP_A#
SLP_LAN#
SLP_S0#
PM_SLP_S3#_R
PM_SLP_S4#_R
PM_SLP_S5#_R
SUSCLK
BATLOW#
SUSACK#_R
SUSWARN#_R
PCH_LAN_WAKE#
PCH_AC_PRESENT_R
SLP_SUS#
PM_PWRBTN#_R
SYS_RESET#
H_CPUPWRGD 6
ITP_PMODE 61
JTAGX 61
PCH_TMS 61
PCH_TDO 61
PCH_TDI 61
PCH_TCK 61

+1.2V
RH756 470_0201_5%
PCH_DRAMRST# 12,13
SYS_PWROK 52
PCIE_WAKE# 47,52,56
PM_SLP_S3# 52
PM_SLP_S4# 52
SUSCLK 47
AC_PRESENT 52
PBTN_OUT# 52,61
SYS_RESET# 61
PCH_BEEP 58
TOP_SWAP_EN 52
08/15

+3VALW_PCH
RH56 10K_0201_5% SUSWARN#_R

+3VALW
RH17 10K_0201_5% PM_PWRBTN#_R
RH58 10K_0201_5% PCH_AC_PRESENT_R
RH60 10K_0201_5% BATLOW#
RH80 4.7K_0201_5% WAKE#
RH747 10K_0201_5% PCH_LAN_WAKE#

+3VS
RH67 10K_0201_5% SYS_RESET#
RH65 8.2K_0201_5% PM_CLKRUN#

RH921 10K_0201_5% PCH_AC_PRESENT_R
RH18 100K_0201_5% SYS_PWROK_R
RH54 10K_0201_5% PCH_PWROK_R
RH59 100K_0201_5% PCH_RSMRST#_R
CH304 0.1U_25V_K_X5R_0402
EMC_NS@
RH61 100K_0201_5% PCH_DPWROK_R
EMC request
place close to PCH ball
08/22

+3VS
RH849 150K_0402_5% SMB1_ALERT#

+3VALW_PCH
RH28 1K_0201_5% PCH_BEEP
SPKR / GPP_B14
The signal has a weak internal pull-down.
* 0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

CMOS
VCCRTC
CH4 1U_0402_6.3V6K
RH31 20K_0402_5% PCH_SRTCRST#
RH41 20K_0402_5% PCH_RTCRST#
CH5 1U_0402_6.3V6K
CH1 1U_0402_6.3V6K
JCMOS1 SHORT PADS

+3VALW_PCH
RPH3 2.2K_0404_4P2R_5%
SML0CLK
SML0DATA

RH765 2.2K_0201_5% SMB_ALERT#
RH766 2.2K_0201_5% SMB0_ALERT#
RH767 2.2K_0201_5% SMB1_ALERT#
RH768 2.2K_0201_5%
RH769 2.2K_0201_5%
RH770 2.2K_0201_5%
Strap

GPU, EC, Thermal Sensor
+3VALW_PCH
RPH8 2.2K_0404_4P2R_5%
+3VS
SML1CLK
SML1DATA
QH2A L2N7002KDW1T1G_SOT363-6
QH2B L2N7002KDW1T1G_SOT363-6
EC_SMB_CK2 29,39,52,59,60
EC_SMB_DA2 29,39,52,59,60

DIMM1, DIMM2
+3VALW_PCH
RPH4 2.2K_0404_4P2R_5%
+3VS
2N7002KDWH Vth= min 1V, max 2.5V ESD 2KV
RPH7 2.2K_0404_4P2R_5%
69 PCH_SMBCLK
69 PCH_SMBDATA
QH1A L2N7002KDW1T1G_SOT363-6
QH1B L2N7002KDW1T1G_SOT363-6
SMB_CLK_S3 12,13
SMB_DATA_S3 12,13

68,69 ALW_PWRGD
RH284 0_0201_5%
DH13 RB751V-40_SOD323-2
EC_RSMRST#

RSMRST# sequence control circuit

CNVI_MODEM_CLKREQ
RH830 71.5K_0402_1% CNVI@
Place close to PCH yong 06/25
CNVI_MODEM_CLKREQ 47

CNVI_RF_RESET#
RH829 75K_0402_5% CNVI@
Place close to PCH yong 06/25
CNVI_RF_RESET# 47

AS EMC request
close to PCH
PCH_PWROK_R
SYS_PWROK_R
PCH_DPWROK_R
HDA_SDOUT
PCH_HDA_SDIN0
CH88 CH94 CH98 CH283 CH284
1U_0402_10V6-K
2.2P_0402_50V8-C
EMC_NS@

EMC request
08/21
HDA_BIT_CLK
EMC_NS@
CH303 22P_0201_25V8J

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (3/9) HDA,RTC,SMBUS,PM
Size: C
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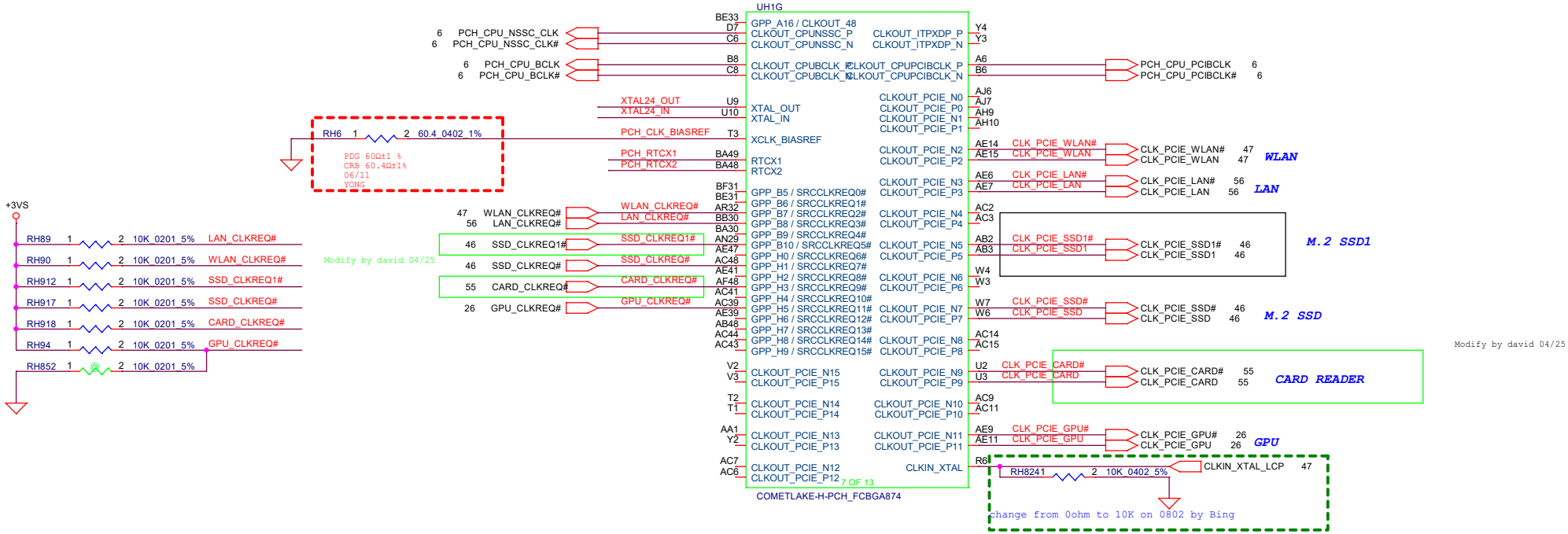

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (3/9) CLOCK,GPPBH

Size	Document Number	Rev
A3	Y550-CML GN20P	1.0

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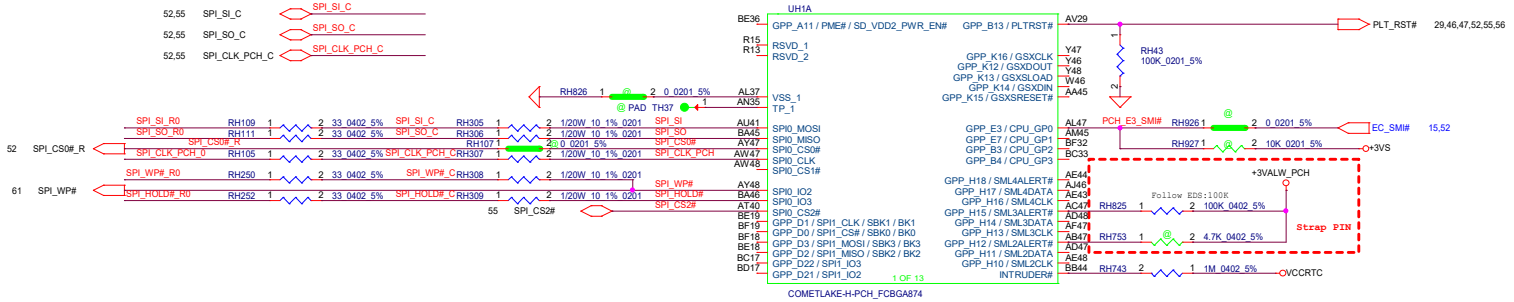
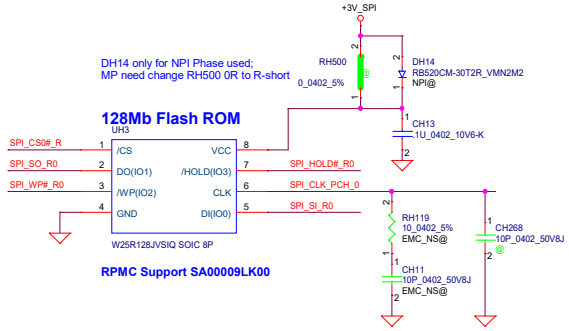
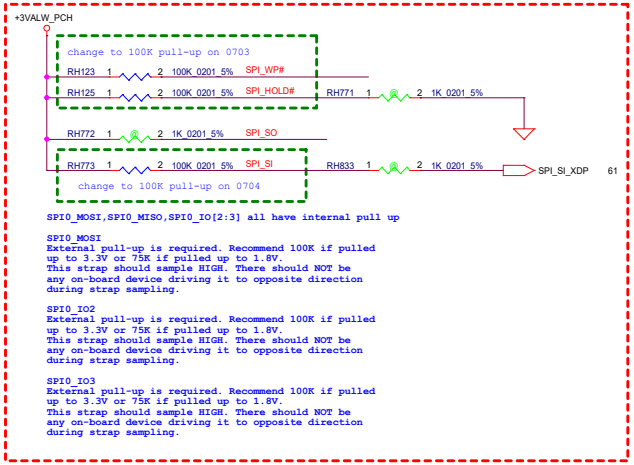




+3V_SPI

1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



SPI0_MOSI,SPI0_MISO,SPI0_IO[2:3] all have internal pull up

SPI0_MOSI
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_H15 /SML3ALERT# (Strap reserved)
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Power Plane: Primary Well

GPP_H12 /SML2ALERT#
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI i s disabled)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
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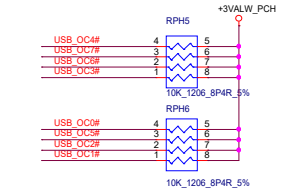
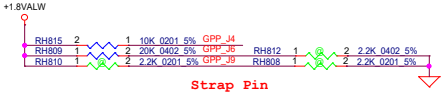
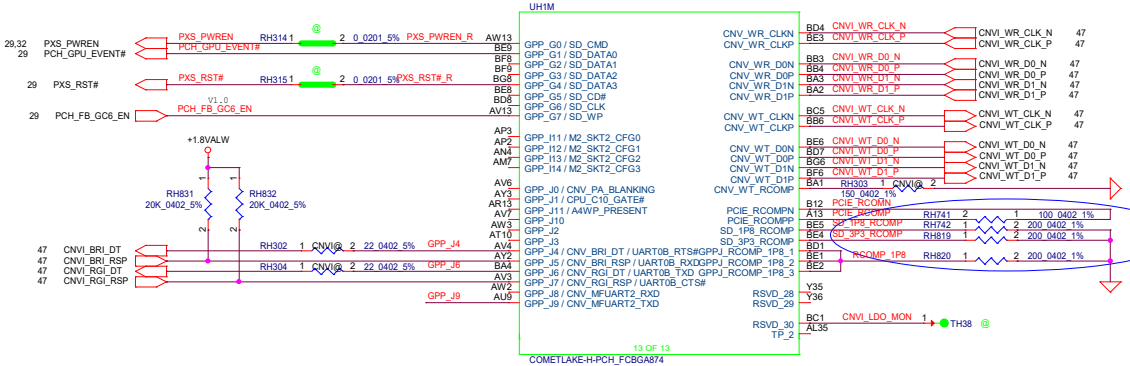




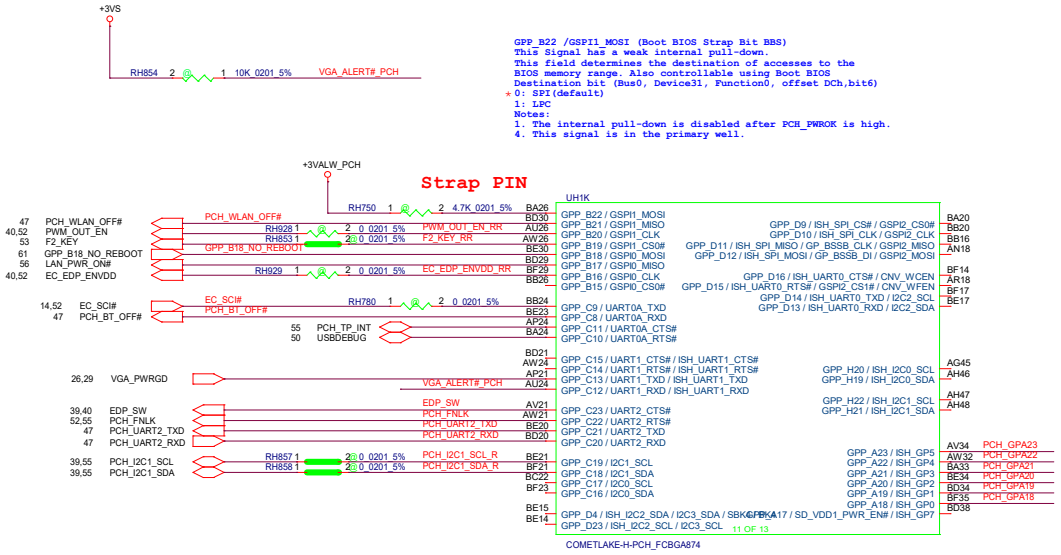
Primary Well Group J (1.8 V Only)

Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

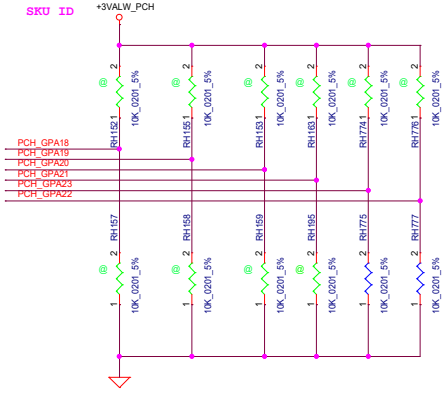


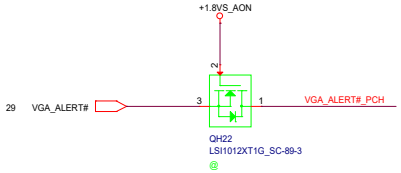
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

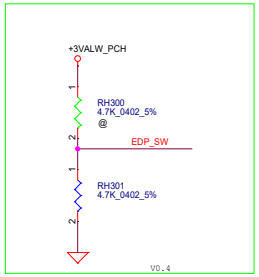
Title	Blank		
Size C	Document Number	Y550-CML GN20P	Rev 1.0
Date: Tuesday, April 06, 2021	Sheet 19 of 83		



Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC







Board ID table need modify
yong 07/10

PCH_GPA22 add for distinguish
L350: H
Y550:L
yong 07/11

Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22 (L340: H Y550: L)	PCH_GPA23 (Reserved)
Y550-15-GN20P0	0	0	0	0	0	0
Y550-15-GN20P1	0	0	0	1	0	0
Y550-15-N18P G61	0	0	1	0	0	0
Y550-15-N18P G62	0	0	1	1	0	0
Y550-17-GN20P0	0	1	0	0	0	0
Y550-17-GN20P1	0	1	0	1	0	0
Y550-17-N18P G61	0	1	1	0	0	0
Y540-17-N18P G62	0	1	1	1	0	0

Title	PCH (6/9) GPPPABCD, I2C	
Size: C	Document Number: Y550-CML GN20P	Rev: 1.0
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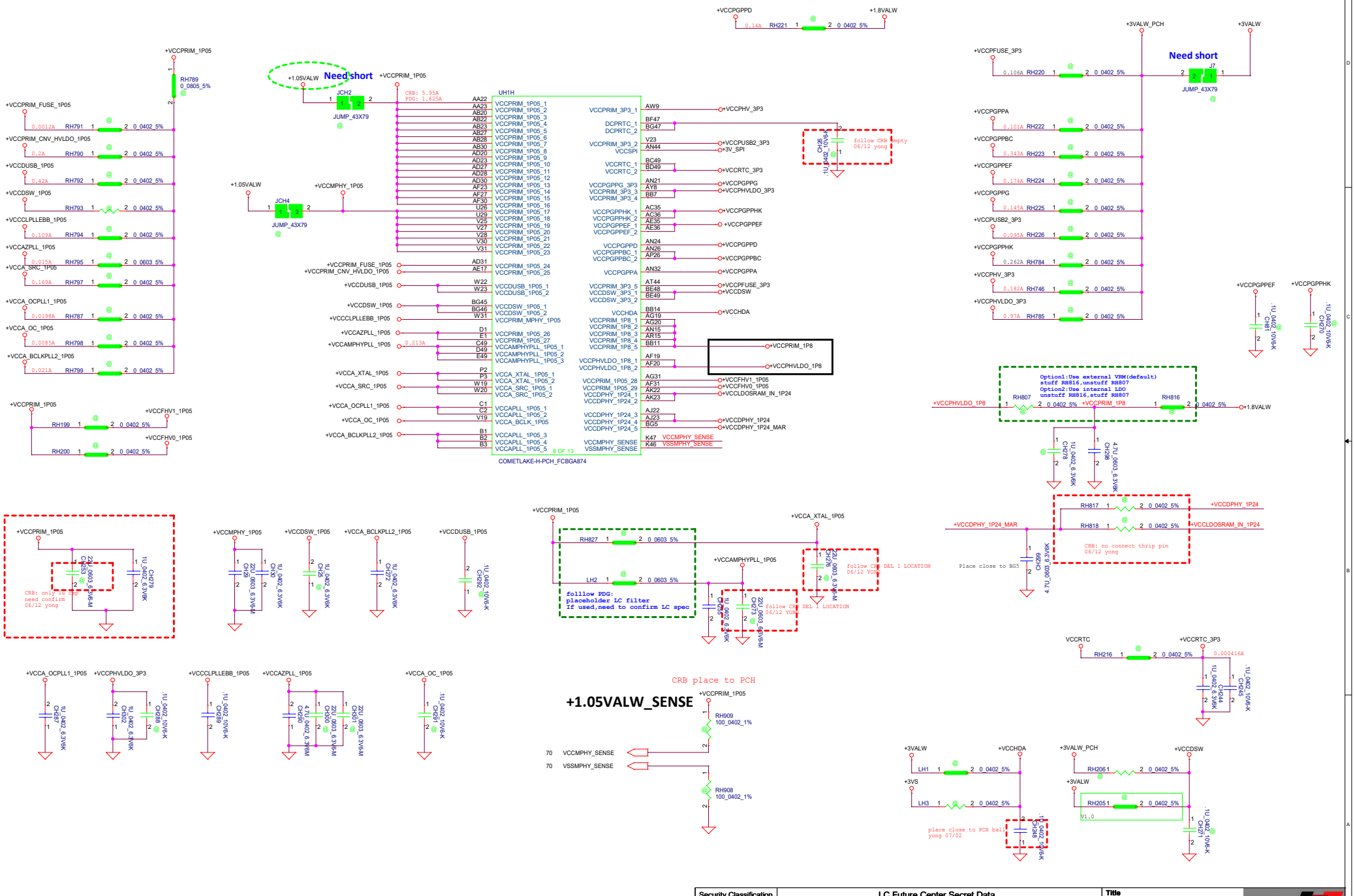

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title	PCH (7/9) PWR		
Size	C	Document Number	Y550-CML GN20P
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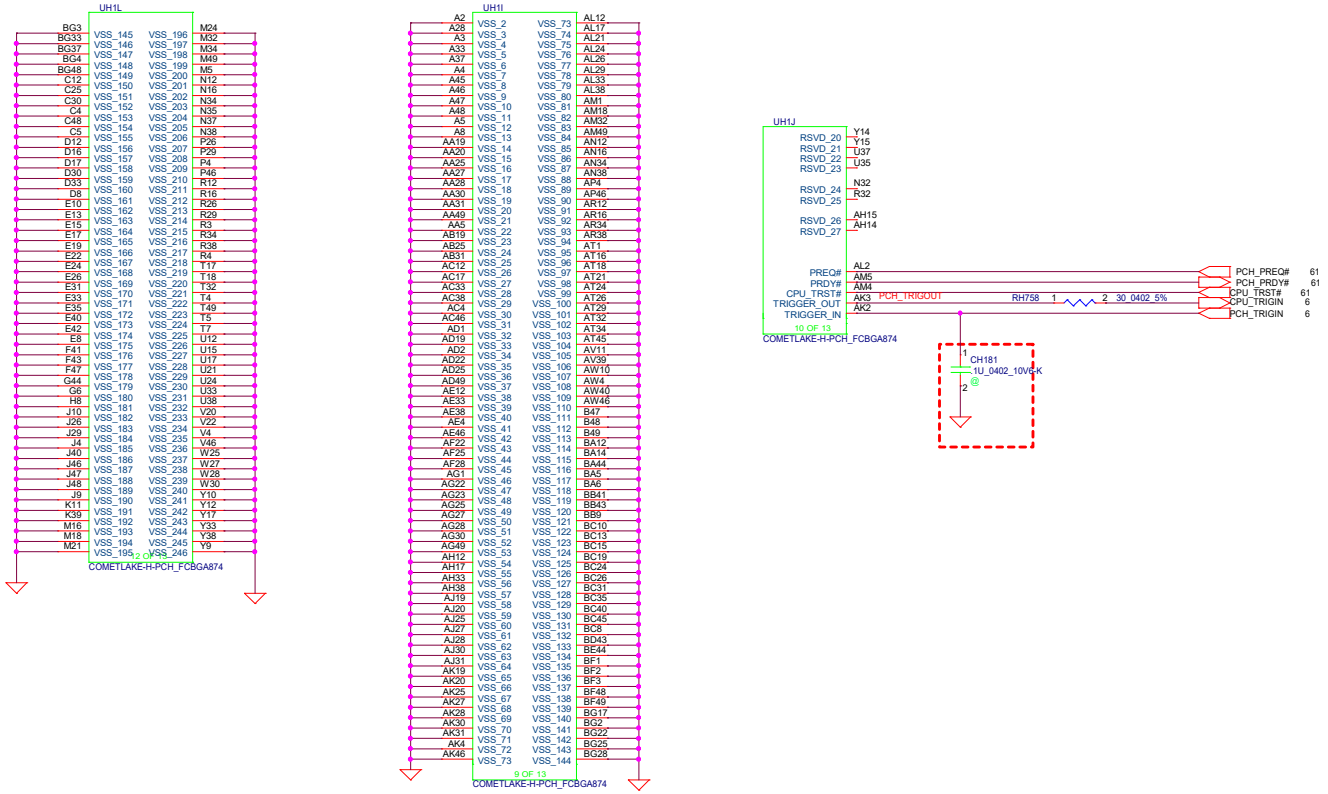

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PCH (9/9) VSS

Size	Document Number	Rev
C	Y550-CML GN20P	1.0

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Title: *Blank*

Size	Document Number	Rev
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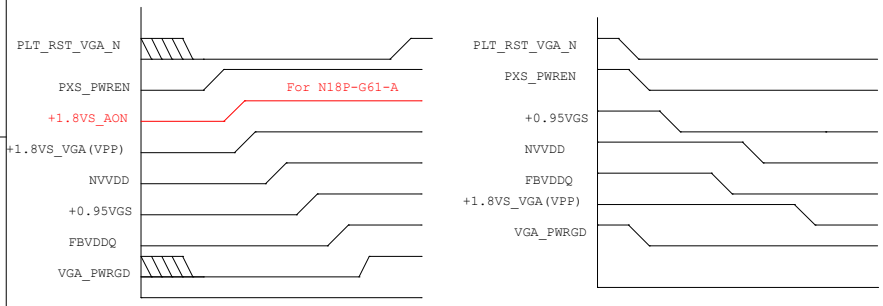
GN20x-P/N18P-G61-A GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN 1V8_MAIN_EN	GN20x-P GPU power sequencing for GC6 ---MSVDD_EN N18P-G61-A 1V8_MAIN_EN	GPIO4_GC6_MSVDD_EN 1V8_MAIN_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	iGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED	UNUSED		test point
GPIO24	IN	HPD_IFPF*	Hot Plug Detect for IFPF	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	test point
GPIO26	OUT	ROM_WP* FP_FUSE	GN20x-P Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)

GN20x-P/N18P-G61-A Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from 1V8 on to PEXVDD/GPU_PGOOD assertion not exceed 20ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90% before PEXVDD can ramp-up.
5. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6

1. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
2. All 3.3V devices that connect to the GPU must be ramp down before 1V8; GPU can NOT have any 3.3V leakage path after 1V8 power down.
3. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down.

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-P/N18P-G61-A VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	Hynix Only For GN20x-P H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION ENABLE

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	N18P-G61-A ENABLE OVERT*
L	L	H	GN20x-P ENABLE OVERT*

BOM NOTE:
1.BOM Structure:
GN20x-P1/P0-->GN20@
N18P-G61-A-->N18P@

2.1.0V_GS voltage different: need Power setting
GN20x-P1/P0-->0.95V
N18P-G61-A-->1.0V

3.VBIOS ROM partnumber need BOM control
GN20x-P1/P0-->2MB PN:SA0000AU500
N18P-G61-A-->1MB PN:SA000080E00

4.ROM_SO,ROM_SI,ROM_CLK setting
GN20x-P1/P0-->LLH
N18P-G61-A-->LLL

5.VRAM_FB(RG702 STUFF package 0402)
GN20x-P1/P0 :2.49K ohm (PN:SD03424918J)
N18P-G61-A: 49.9 ohm (PN:SD034499A8J)

6.+FUSE_1V8
GN20x-P1/P0 :RG1200:10K CG1104:1U
N18P-G61-A: RG1200:2.21K CG1104:2.2U

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
OPT@	GN20-P1/P0 N18P-G61 Stuff
GN20@	GN20P1/P0 Stuff
N18P@	N18P-G61 Stuff

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Title			
GPU Notes List			LCFC
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GN20x-P and N18P-G61-A CO-LAY

VRAM_FB setting

VBIOS ROM PN

+FUSE_1V8

SIT new Change

SKU1/2/5/6/7

SKU3/4

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GPU Virtual

Size: B	Document Number: Y550-CML GN20P	Rev: 1.0
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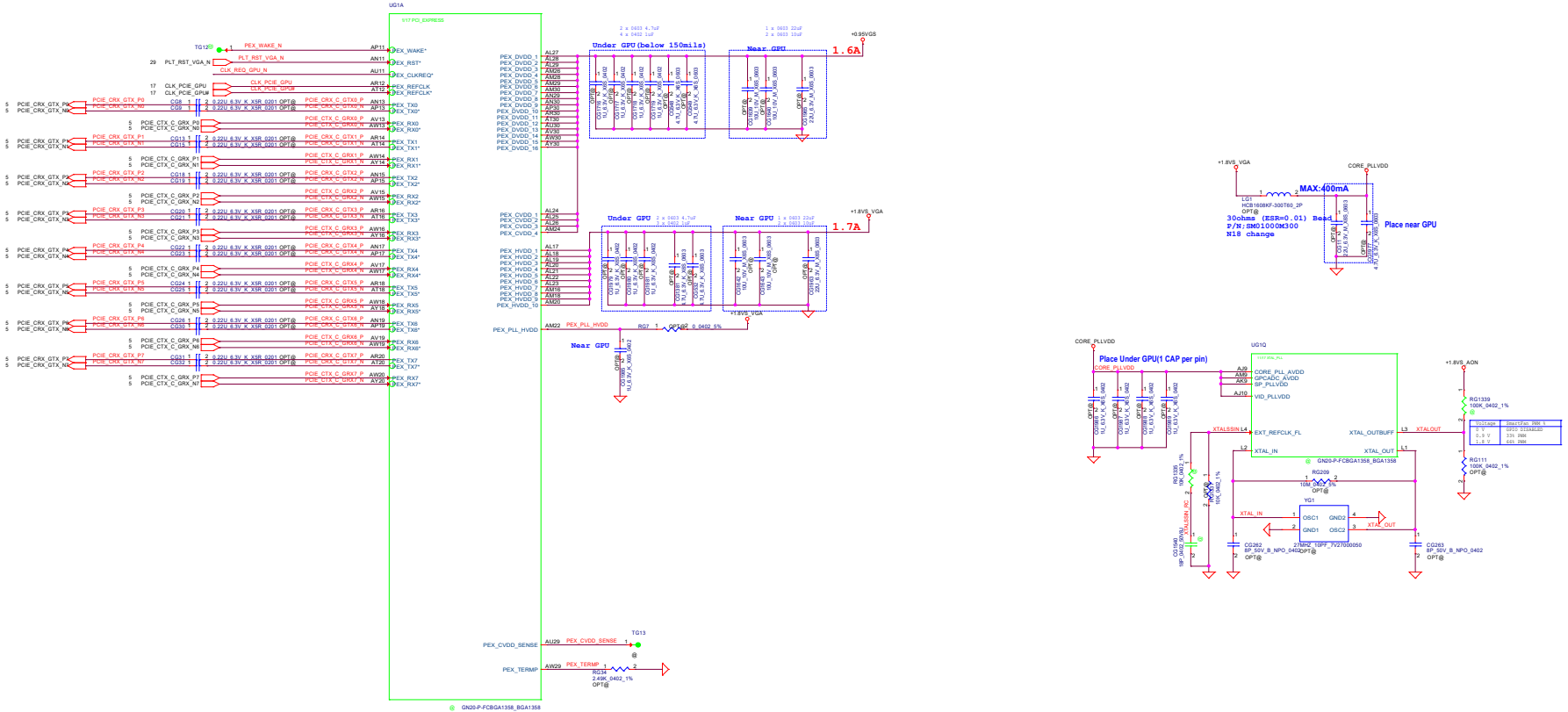
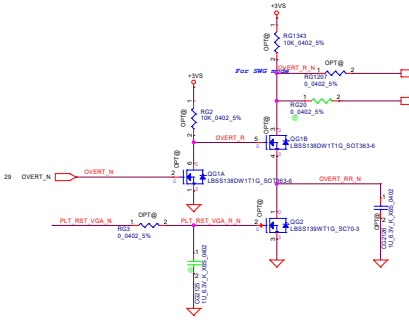
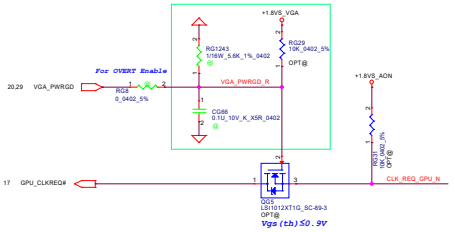


FS_OVERT# FUNCTION



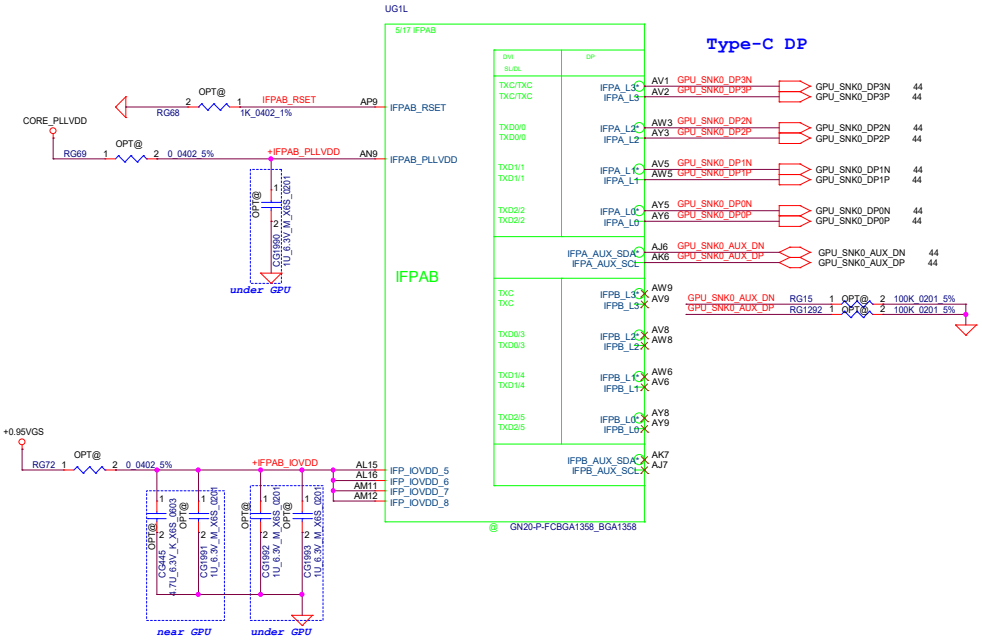


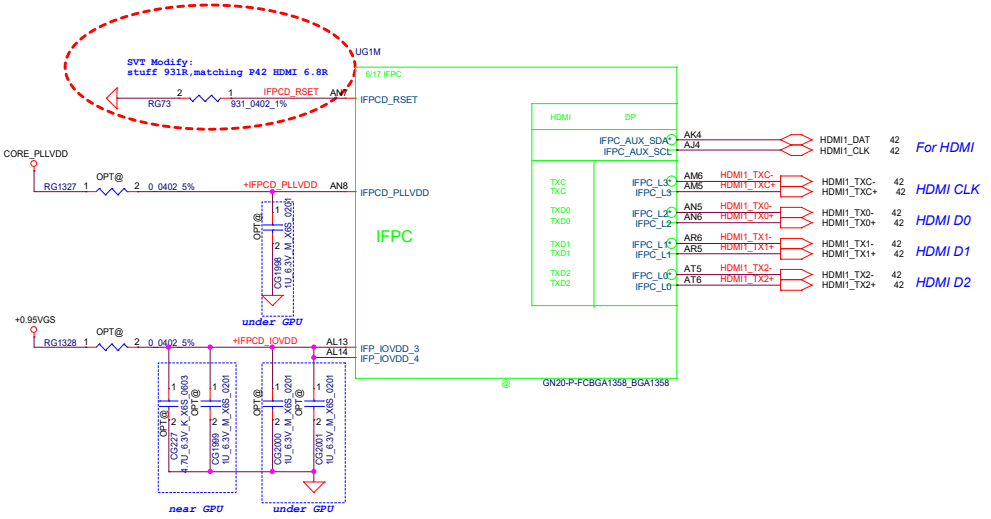
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_(1/6):PEG I/F

Size: D | Document Number: Y550-CML GN20P | Rev: 1.0

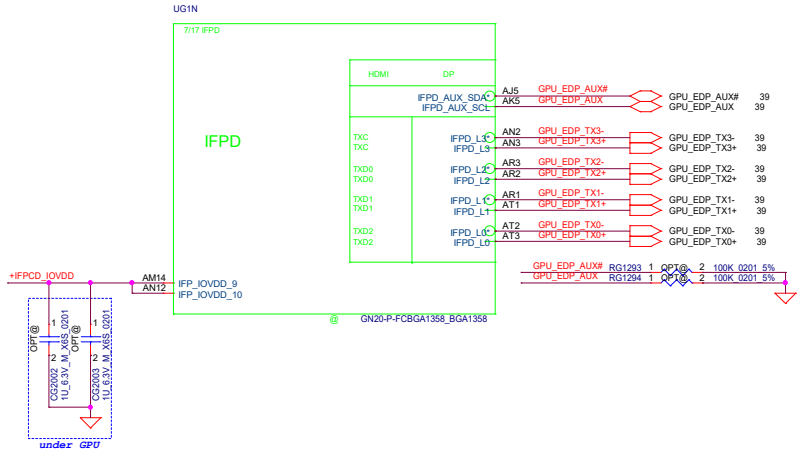
Date: Tuesday, April 06, 2021 | Sheet 28 of 63

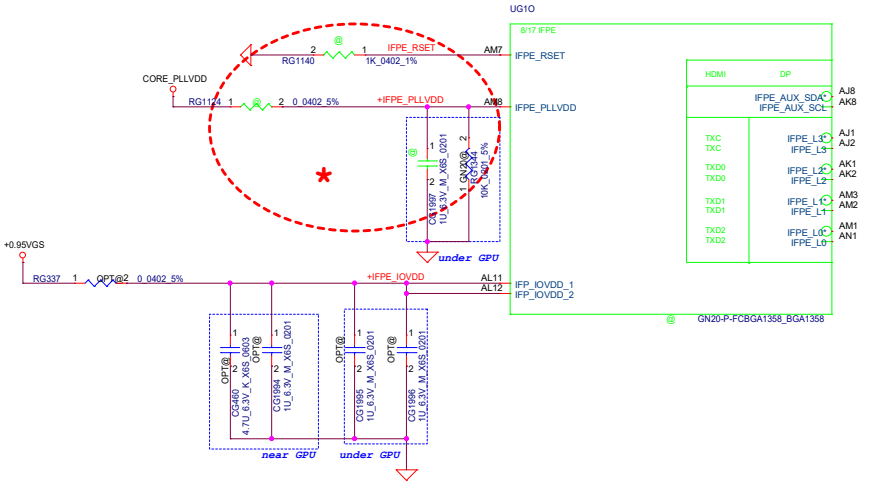




1.If an IFP link is unused, The main and AUX links, IFPxy_RSET can be left unconnected,and IFPxy_PLLVDD should be 10K PD to GND.

2.IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.





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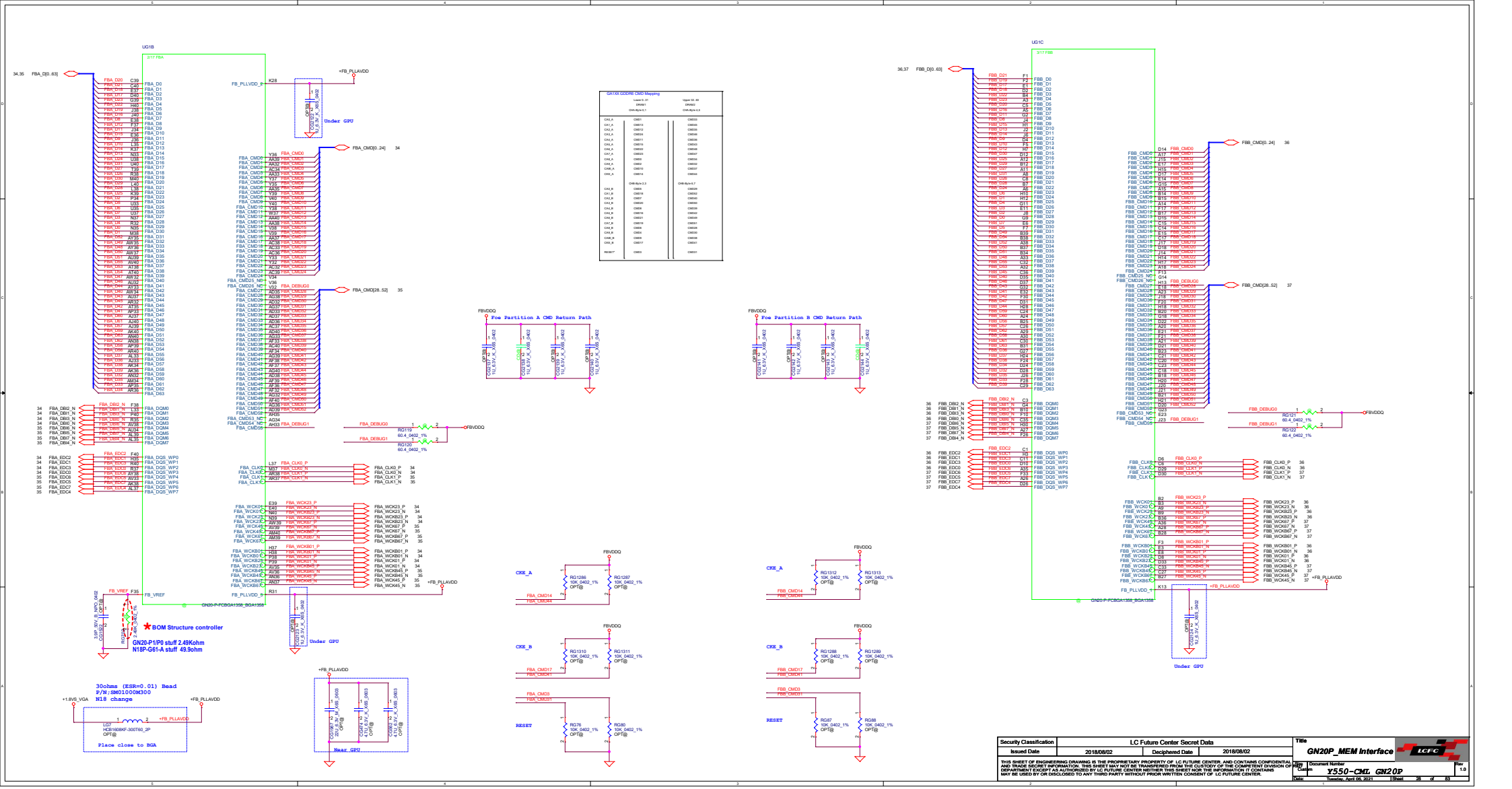
Title	GN20P_Dispaly Interface		
Size C	Document Number Y550-CML GN20P		Rev 1.0
Date: Tuesday, April 06, 2021	Sheet 27 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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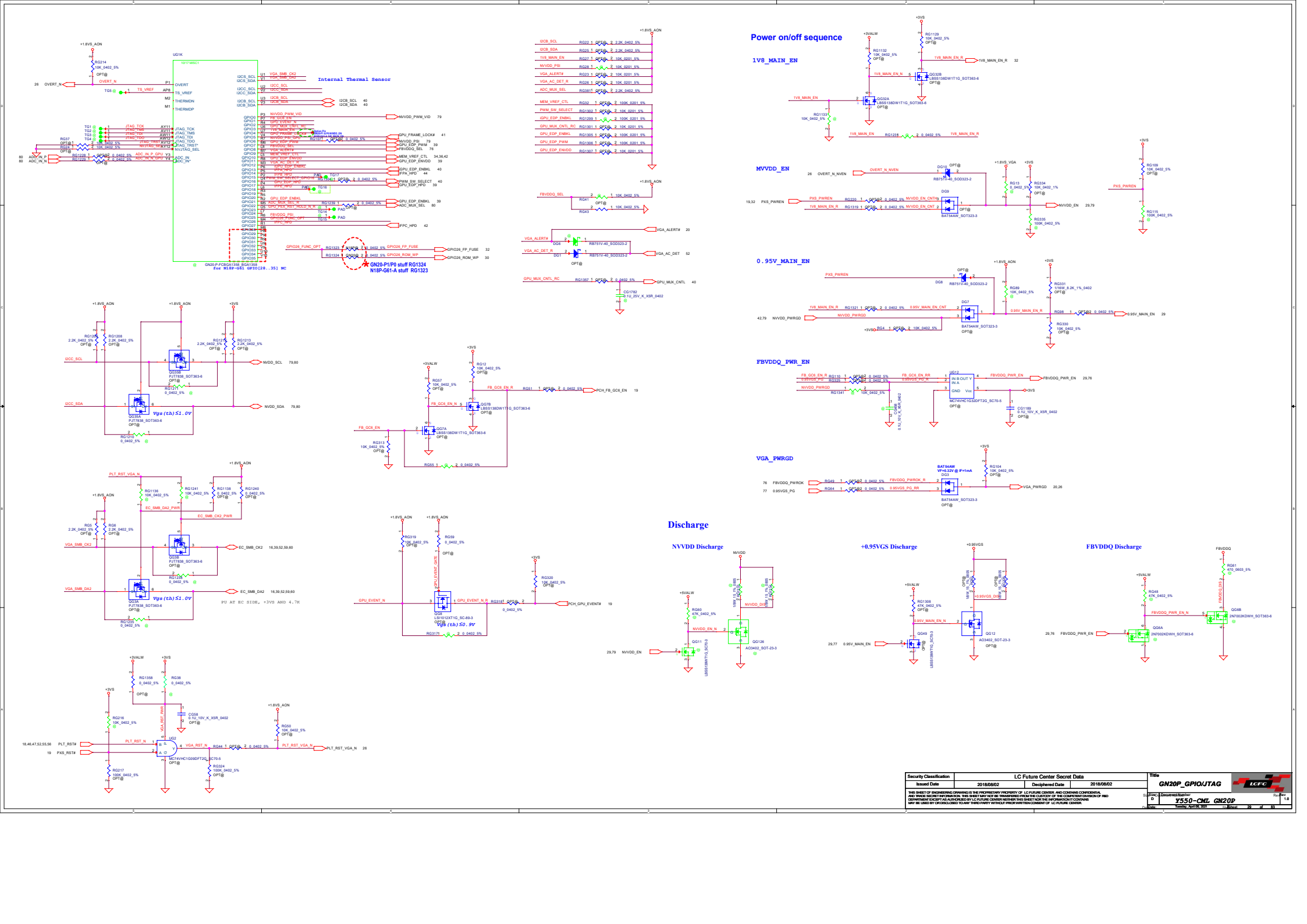
Title	GN20P_MEM Interface		
Size	Document Number		Rev
Custom	Y550-CML GN20P		1.0
Date:	Tuesday, April 06, 2021	Sheet 28 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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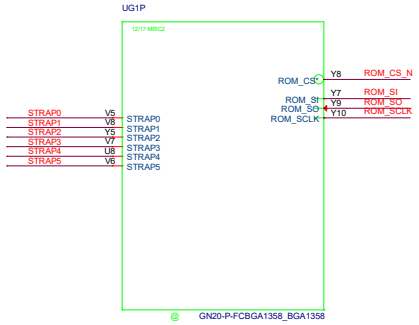
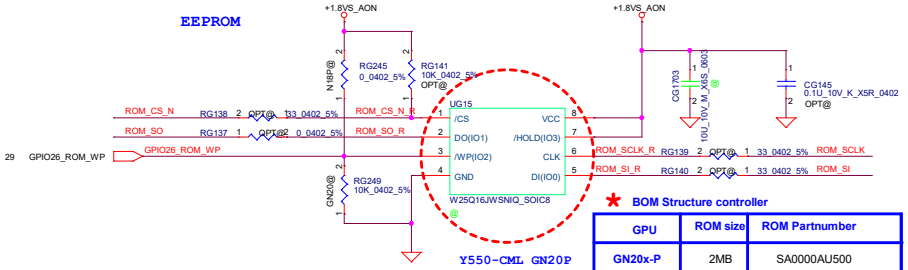
Title: GN20P_GPIO/JTAG

Size: D | Document Number: Y550-CML GN20P | Rev: 1.0

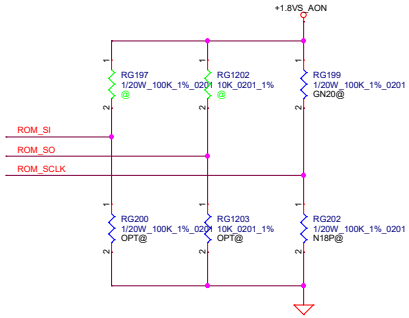
Date: Tuesday, April 06, 2021 | Sheet 29 of 63





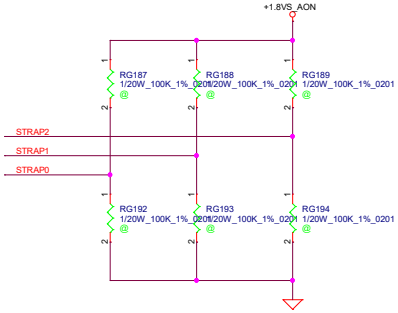
BOM Structure controller

GPU	ROM size	ROM Partnumber
GN20x-P	2MB	SA0000AU500
N18P-G61-A	1MB	SA000080E00



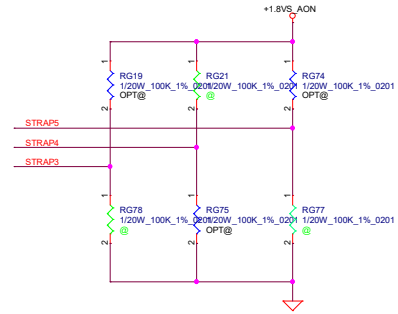
1:ENABLE 0:DISABLE
SOR0 DISABLE
SOR1/2/3 ENABLE

GPU	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N18P-G61-A	L	L	L	ENABLE OVERT*
GN20x-P	L	L	H	ENABLE OVERT*



VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
GN20x-P1 GN20x-P0 N18P-G61-A 4GB	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H
	Hynix 8Gb	H56C8H24AIR-S2C	2(0x0002)	L	H	L



VGA_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

1:DEVID_SEL for G-SYNC SKU

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

Title			
GN20P_Strap			
Size: A2	Document Number: Y550-CML GN20P		Rev: 1.0
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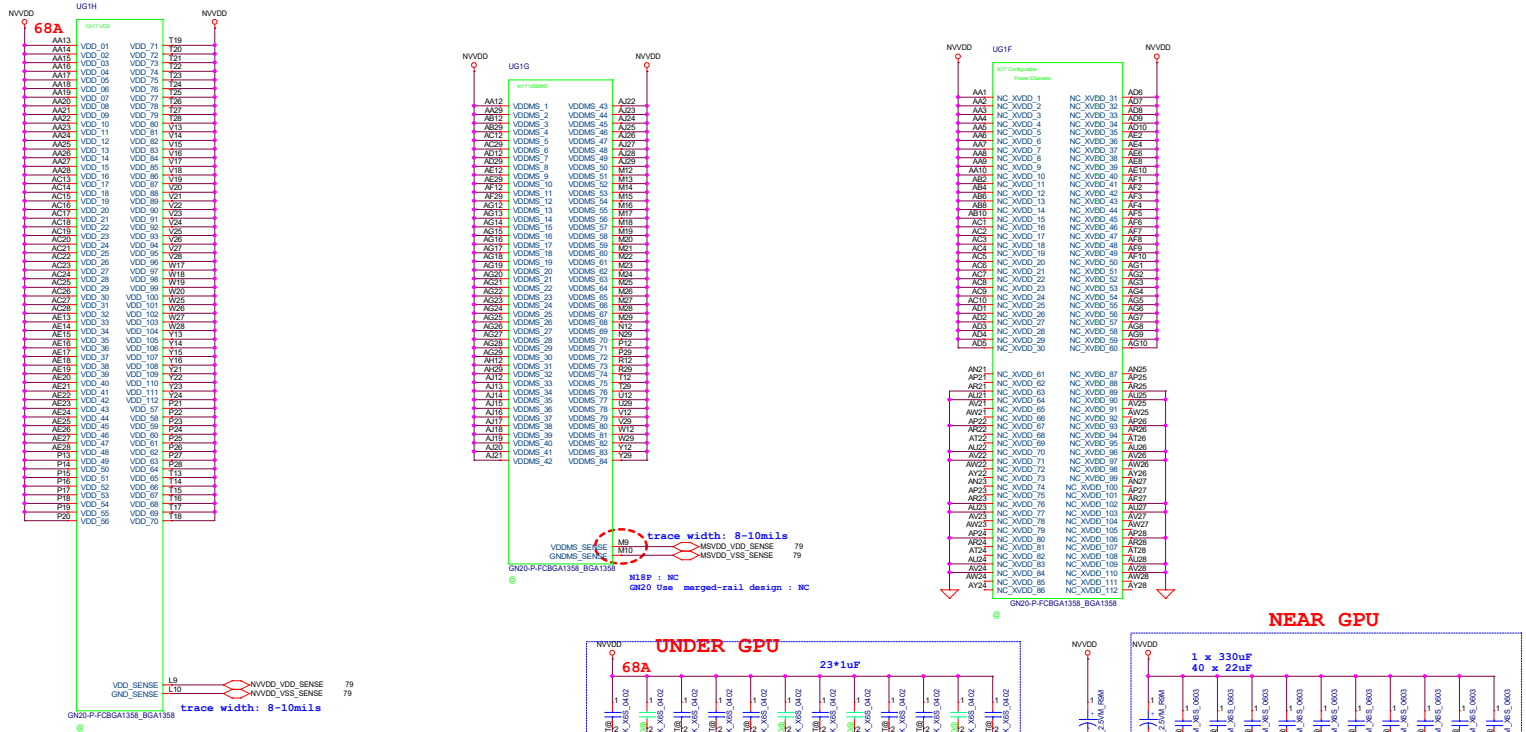

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_PWR1

Size	Document Number	Rev
Custom	Y550-CML GN20P	1.0
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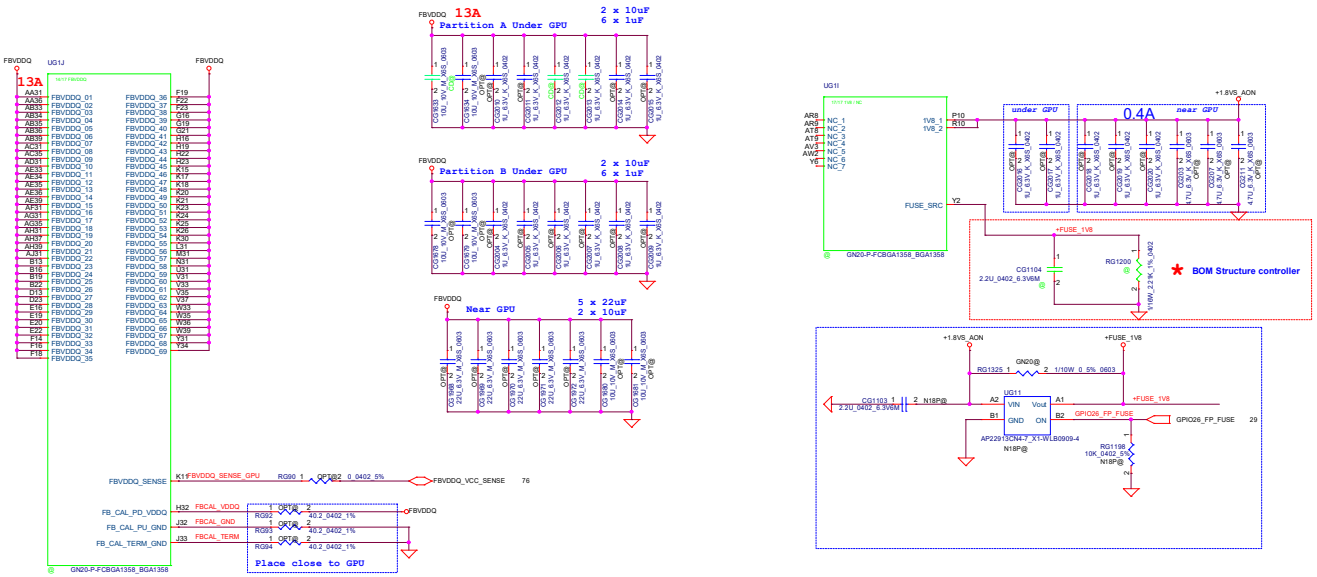

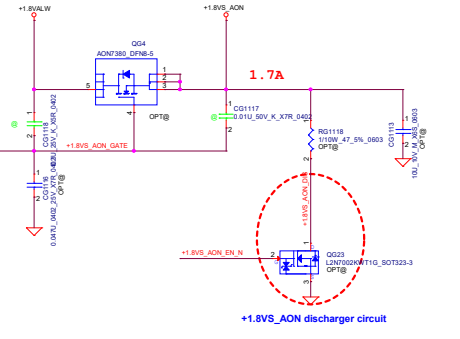

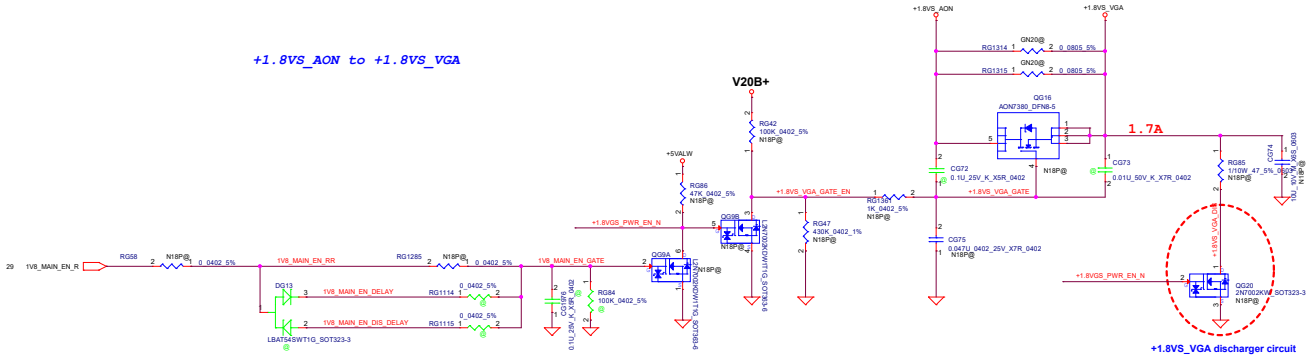

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_PWR2

Size: Custom | Document Number: Y550-CML GN20P | Rev: 1.0

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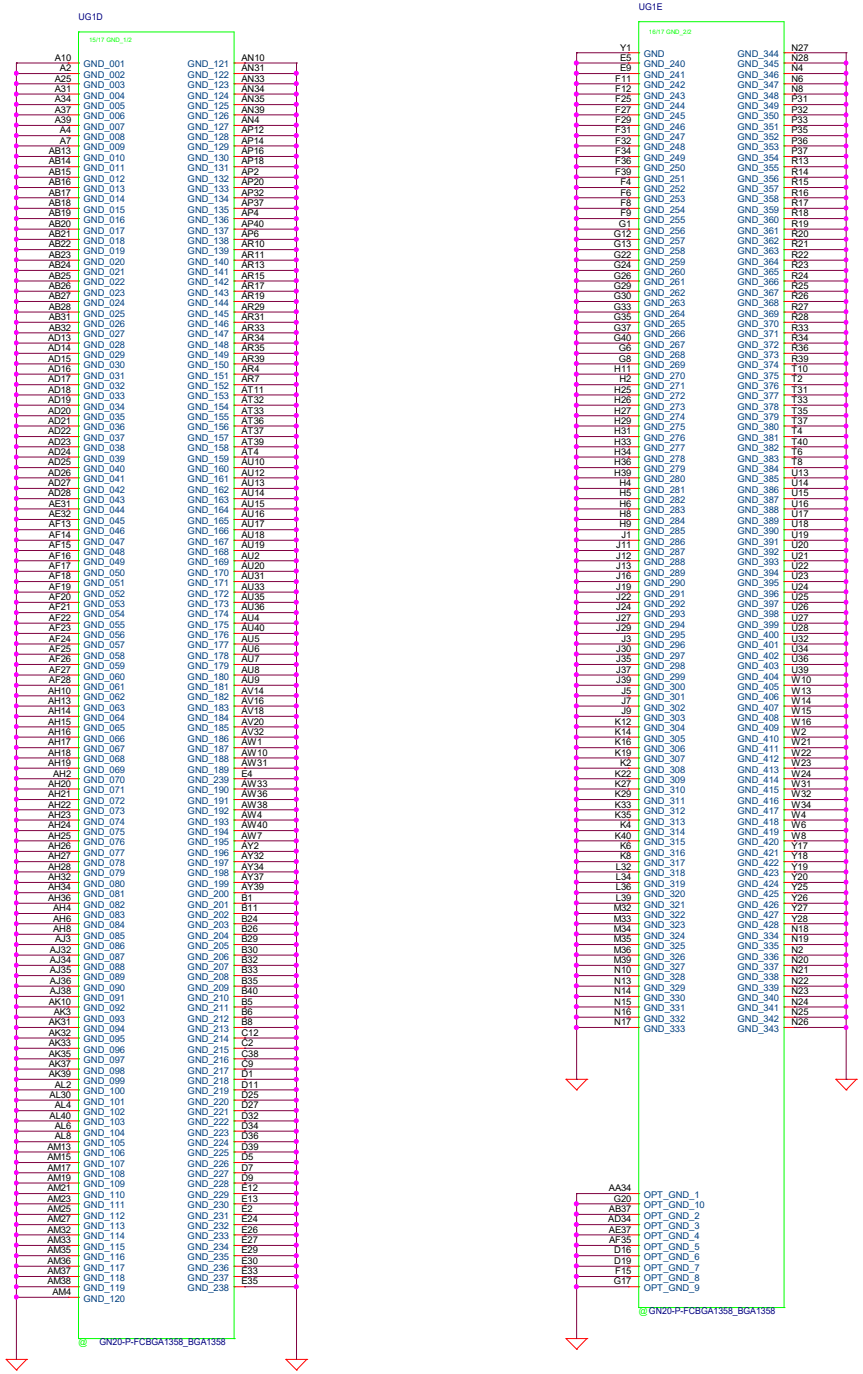

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_GND

LCFC

Size	Document Number	Rev
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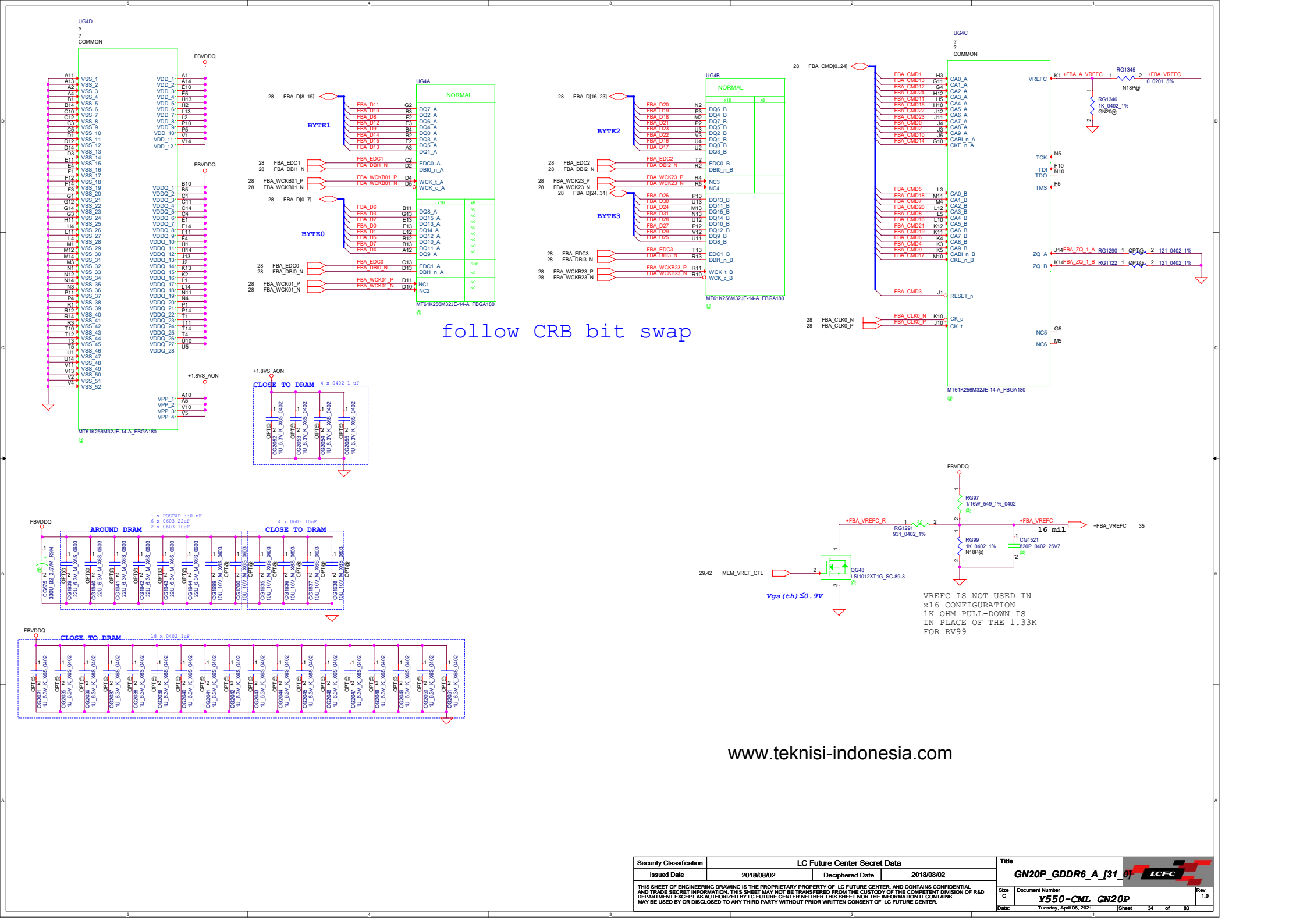
UG4D
COMMON
MT61K256M32JE-14-A_FBGA180
UG4A
NORMAL
BYTE1
BYTE0
UG4B
BYTE2
BYTE3
UG4C
follow CRB bit swap
CLOSE TO DRAM
AROUND DRAM
+1.8VS_AON
FBVDDQ
Vgs(th)≤0.9V
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV99
www.teknisi-indonesia.com
Security Classification
LC Future Center Secret Data
Issued Date
2018/08/02
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2018/08/02
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Title
GN20P_GDDR6_A_[31_0]
Size C
Document Number
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Rev 1.0
Date: Tuesday, April 06, 2021
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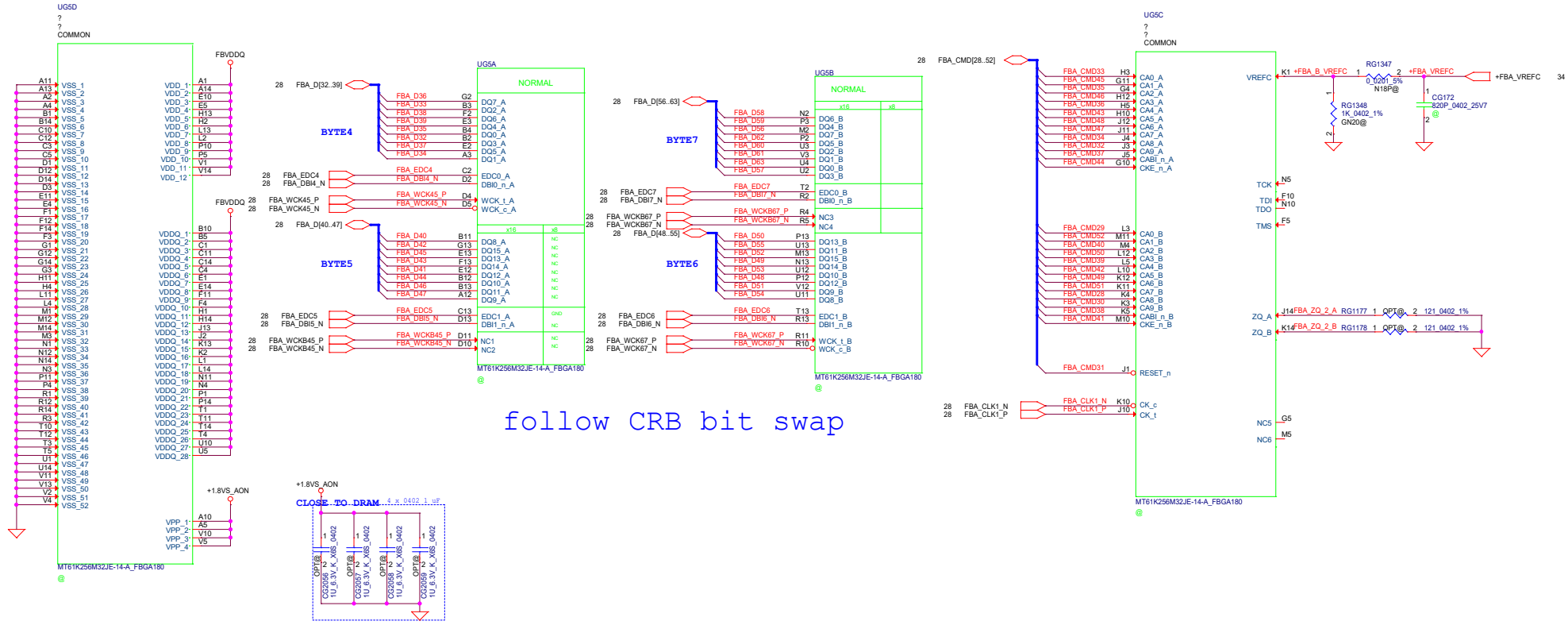

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_GDDR6_A_[63_32]

Size	Document Number	Rev
C	Y550-CML GN20P	1.0

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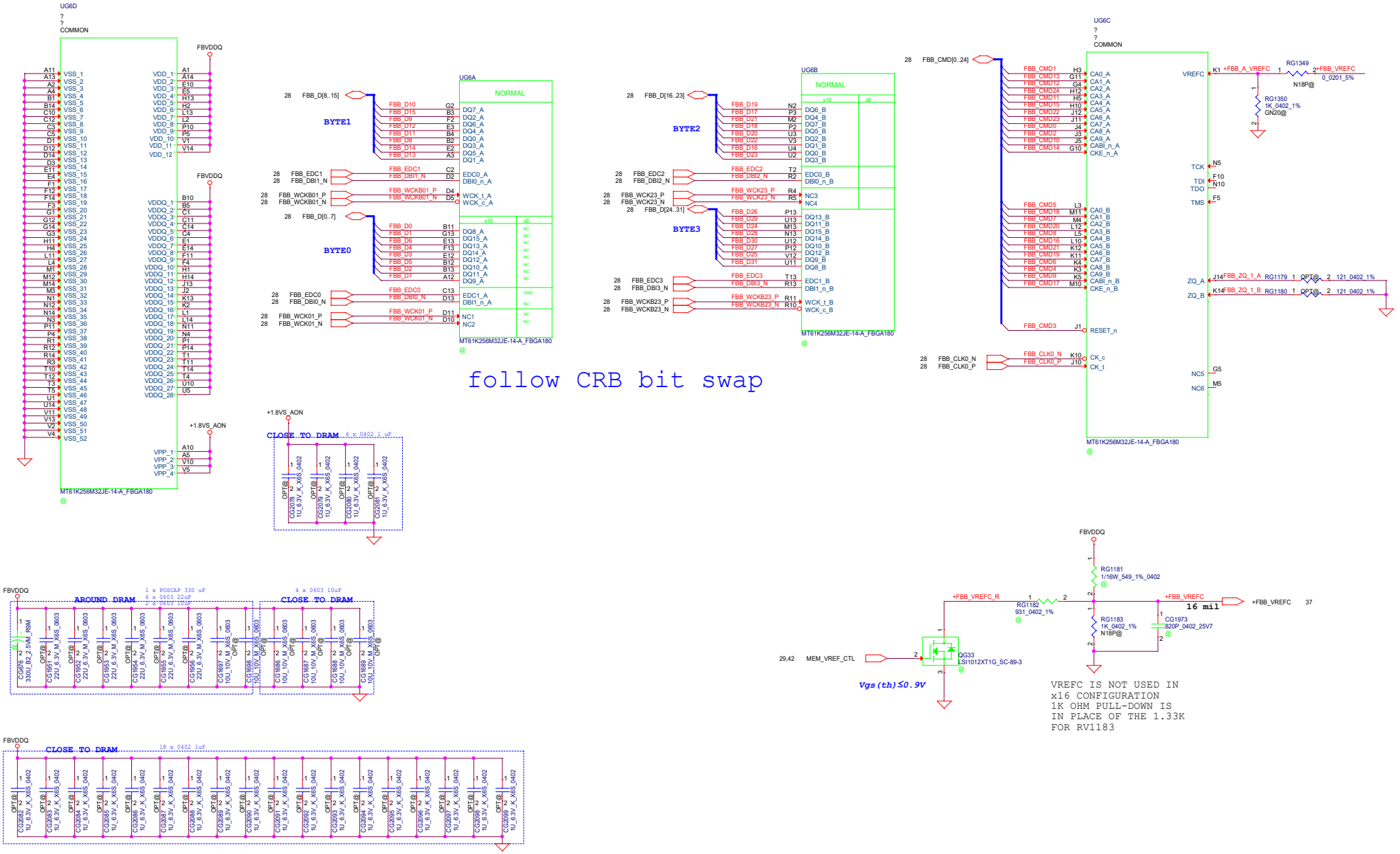
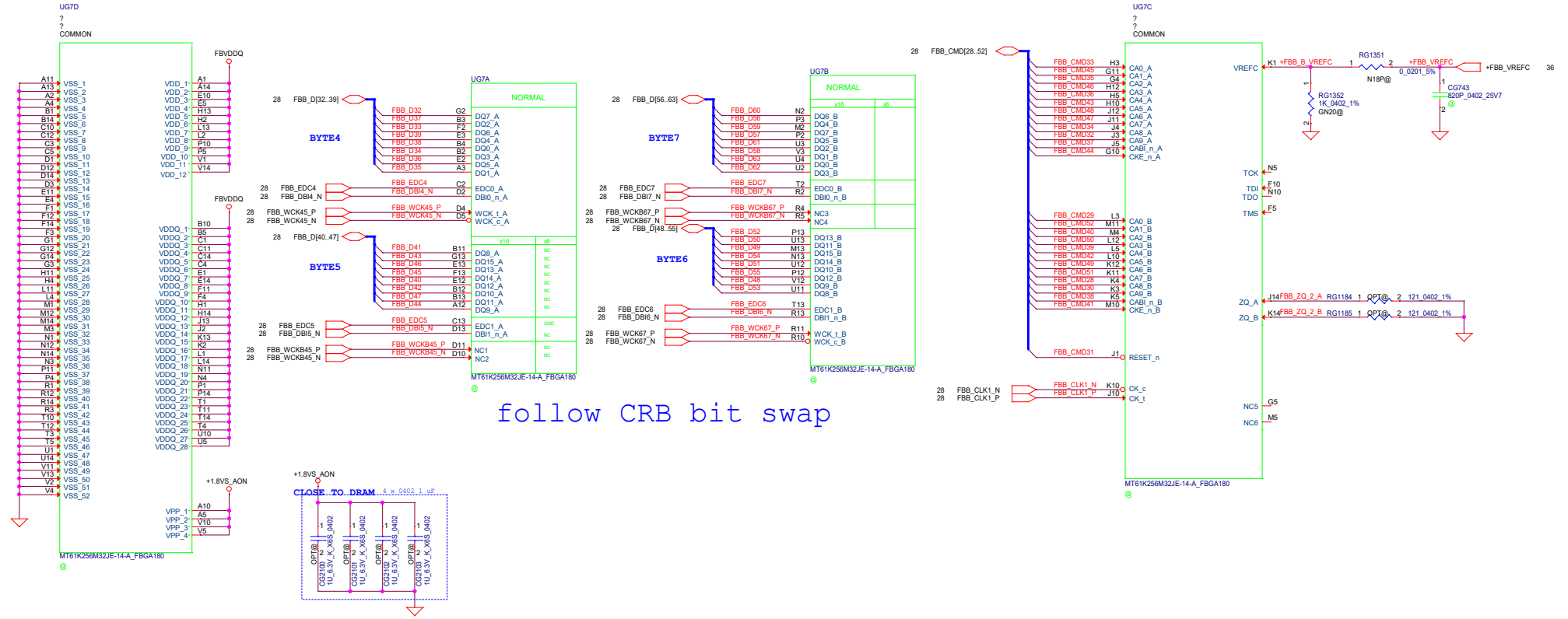


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	GN20P_GDDR6_B_[31_0]		
Size C	Document Number Y550-CML GN20P		Rev 1.0
Date: Tuesday, April 06, 2021	Sheet 36 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GN20P_GDDR6_B_[63_32]

Size	Document Number	Rev
C	Y550-CML GN20P	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *Blank*

Size	Document Number	Rev
B	*Y550-CML GN20P*	1.0

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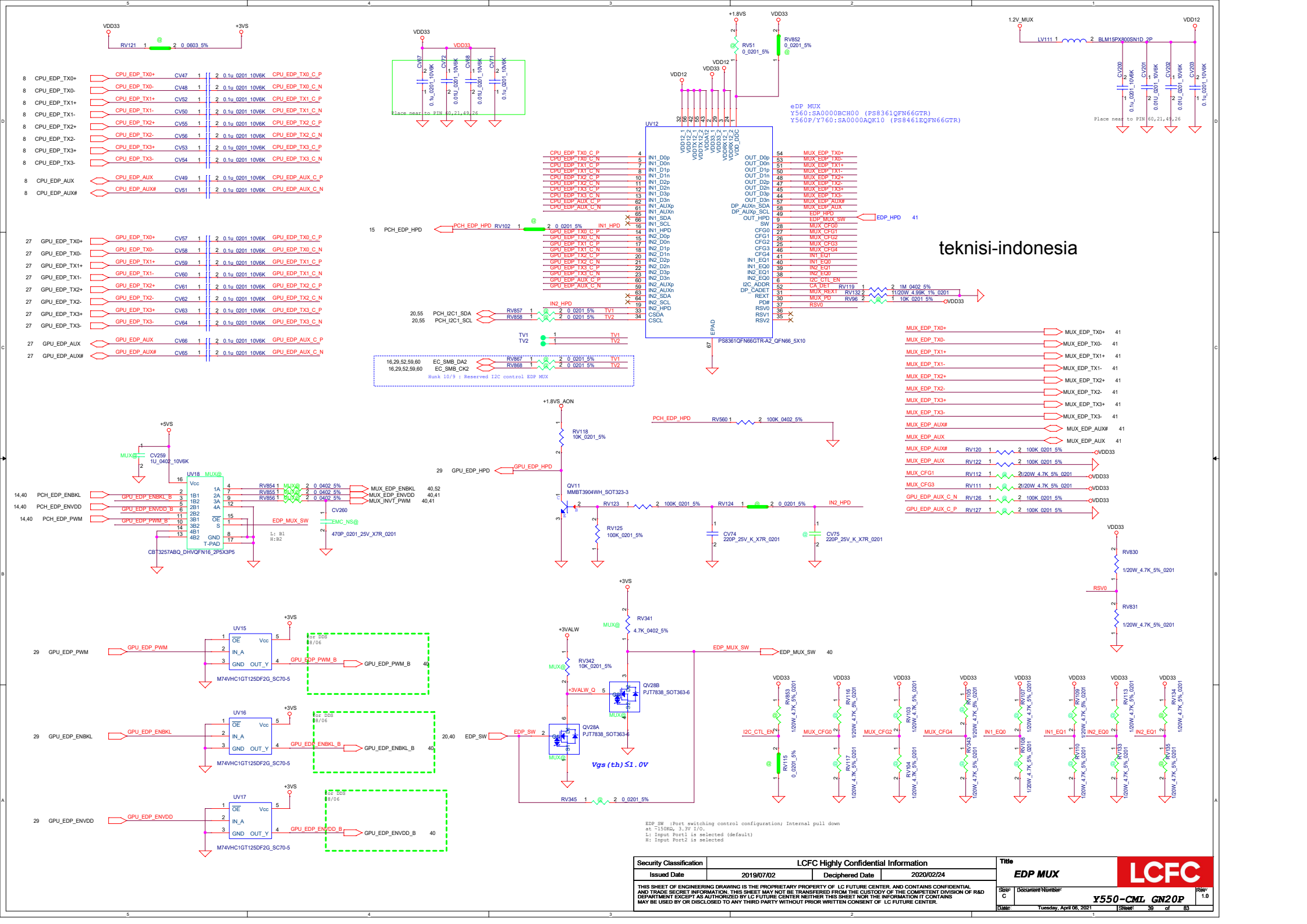
eDP MUX
Y560:SA0000BCH00 (PS8361QFN66GTR)
Y560P/Y760:SA0000AQK10 (PS8461EQFN66GTR)
UV12
PS8361QFN66GTR-A2_QFN66_5X10
teknisi-indonesia
Vgs(th)≤1.0V
EDP_SW :Port switching control configuration; Internal pull down at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected
Hunk 10/9 : Reserved I2C control EDP MUX
EDP MUX
Y550-CML GN20P
LCFC Highly Confidential Information
Issued Date 2019/07/02
Deciphered Date 2020/02/24
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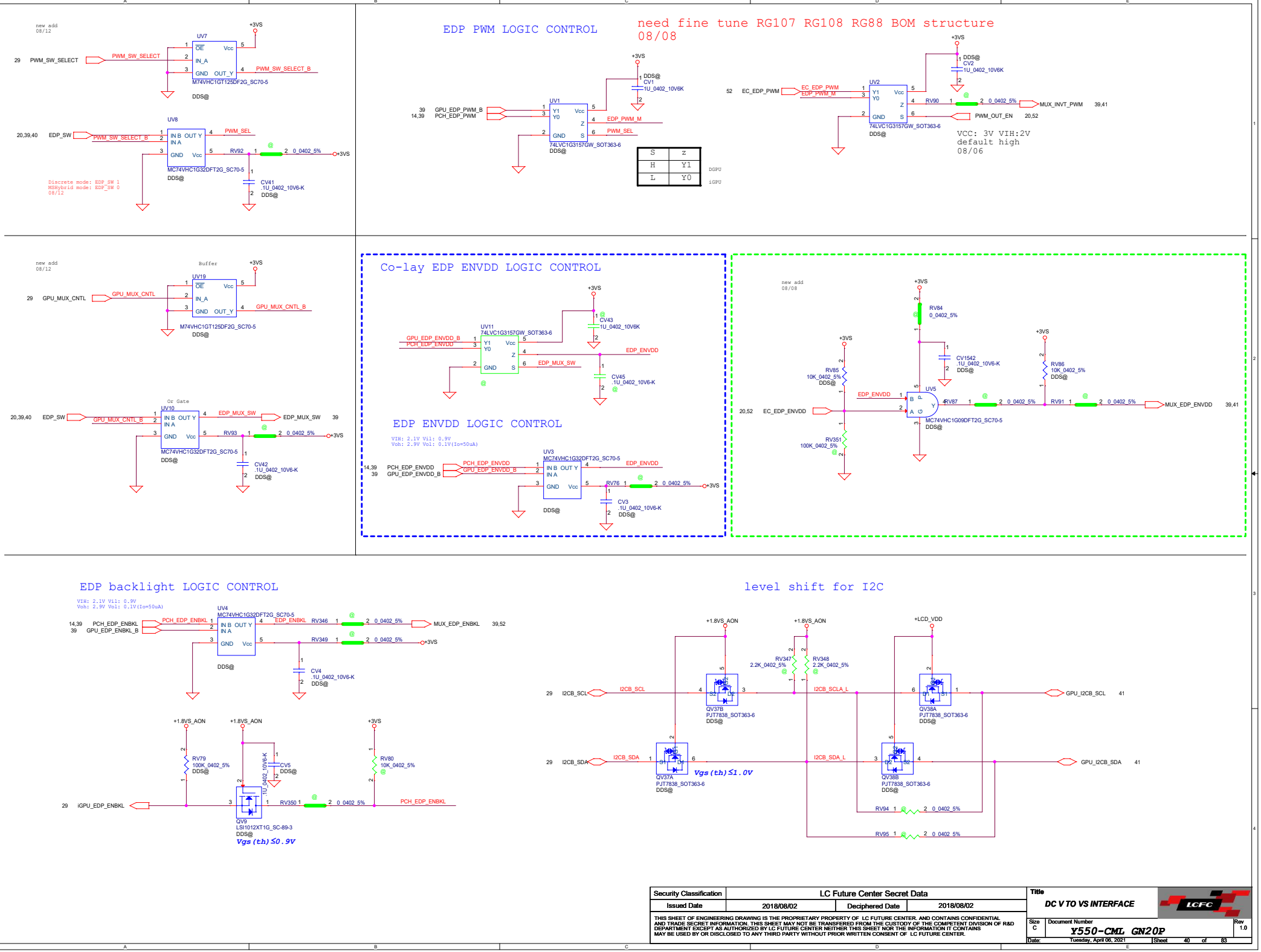

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
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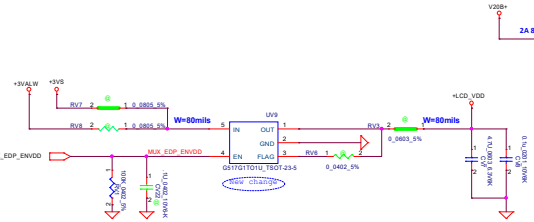
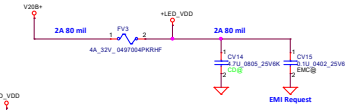
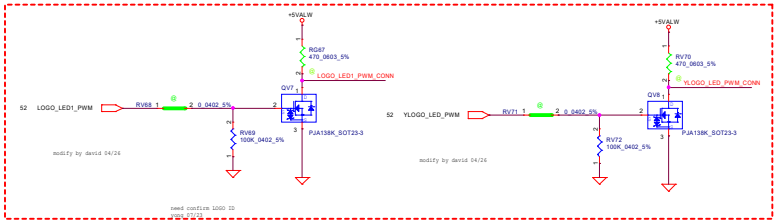
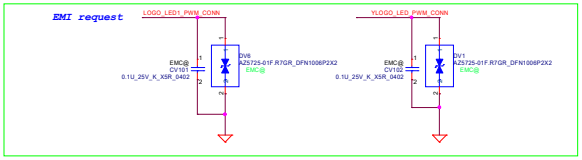
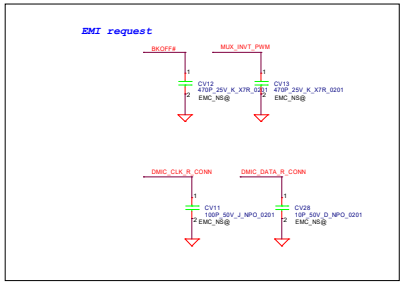
LCD POWER CIRCUIT

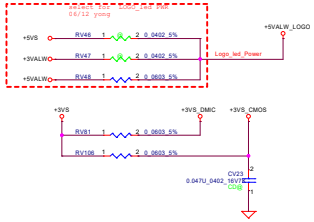


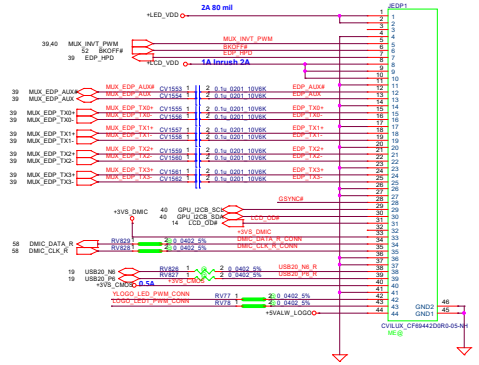


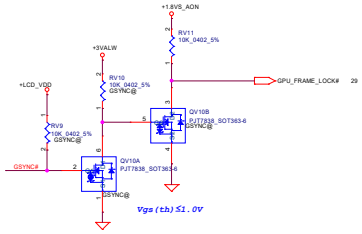


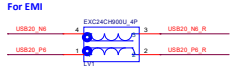












Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	eDP/ CMOS/Touch screen		
Size D	Document Number Y550-CML GN20P		Rev 1.0
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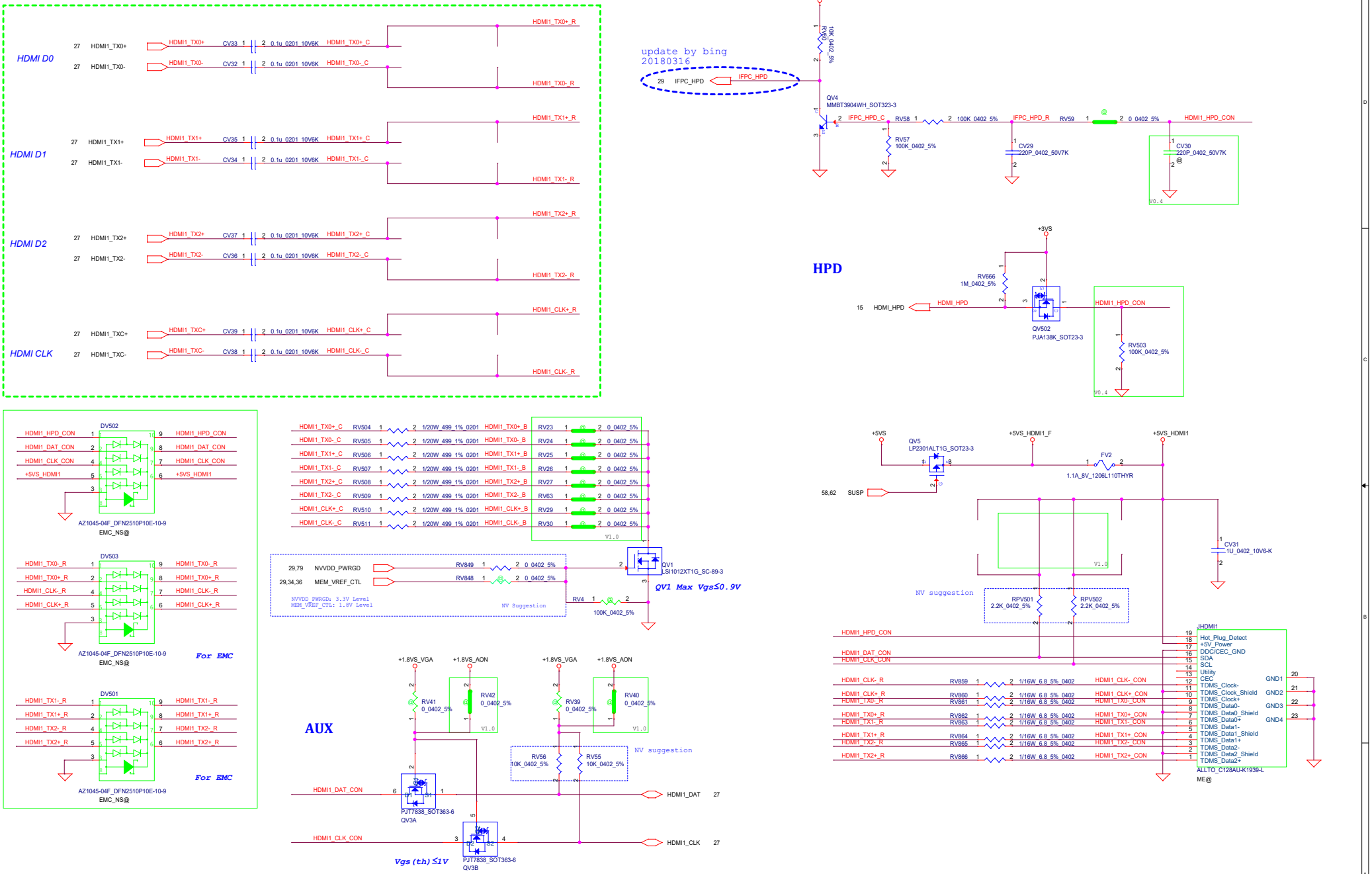

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title	HDMI_CONN		
Size	C	Document Number	Y550-CML GN20P
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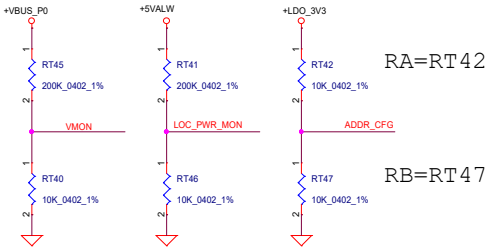
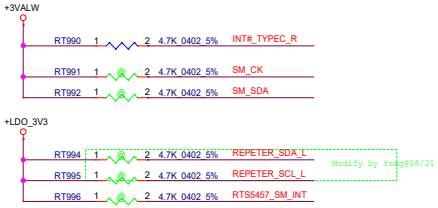
Date:	Tuesday, April 06, 2021	Sheet	42 of 83

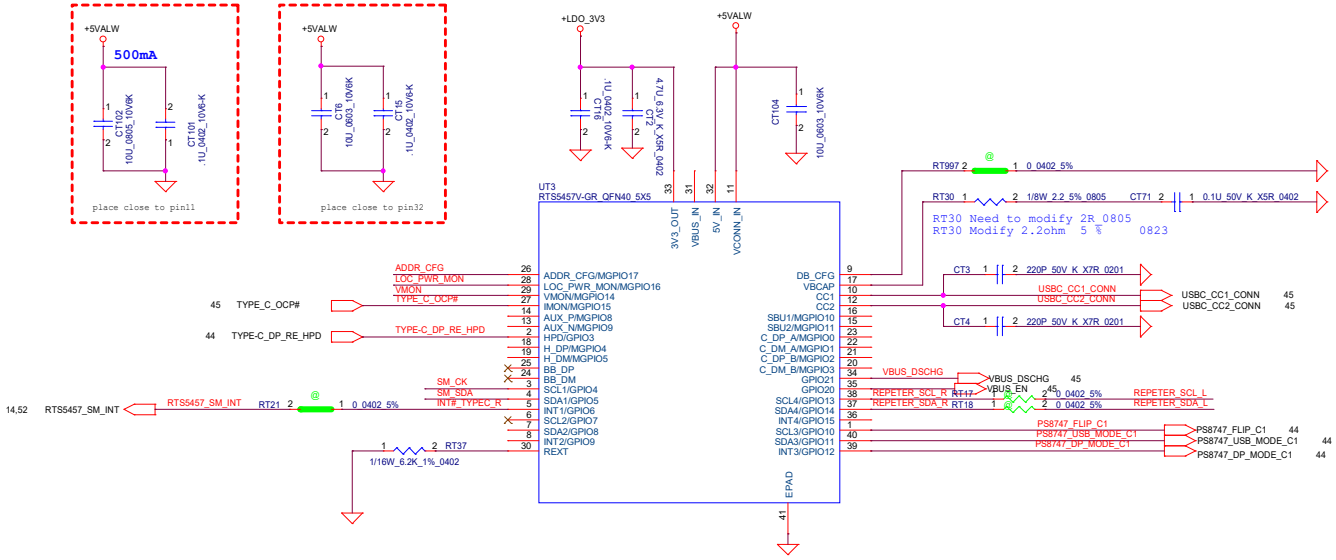


Y550-CML GN20P Project PD Slave Addr: 0xD2

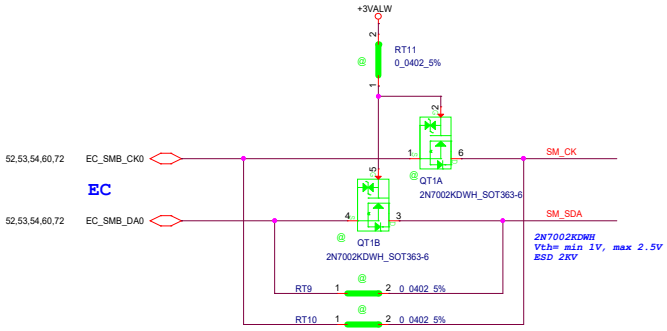
Slave Addr	Ra 5%	Rb 5%	
addr0:0xCC	NC	10K	<0.2V
addr1:0xCE	75K	10K	>=0.2V&&<0.6V
addr2:0xD0	33K	10K	>=0.6V&&<1.0V
addr3:0xD2	10K	10K	>=1.0V

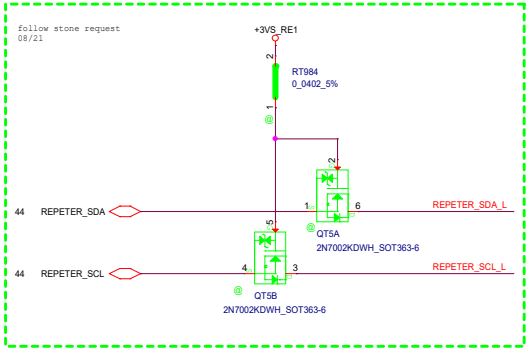
It's is used for SMBUS slave addr0/1/2/3 setting during power on initialization.





For Y550-CML GN20P USE
SA0000ACM80, S IC RTS5457V-GR QFN 40P PD CONTROLLER Y550





Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: USB TYPE-C Controller

Size: C | Document Number: Y550-CML GN20P | Rev: 1.0

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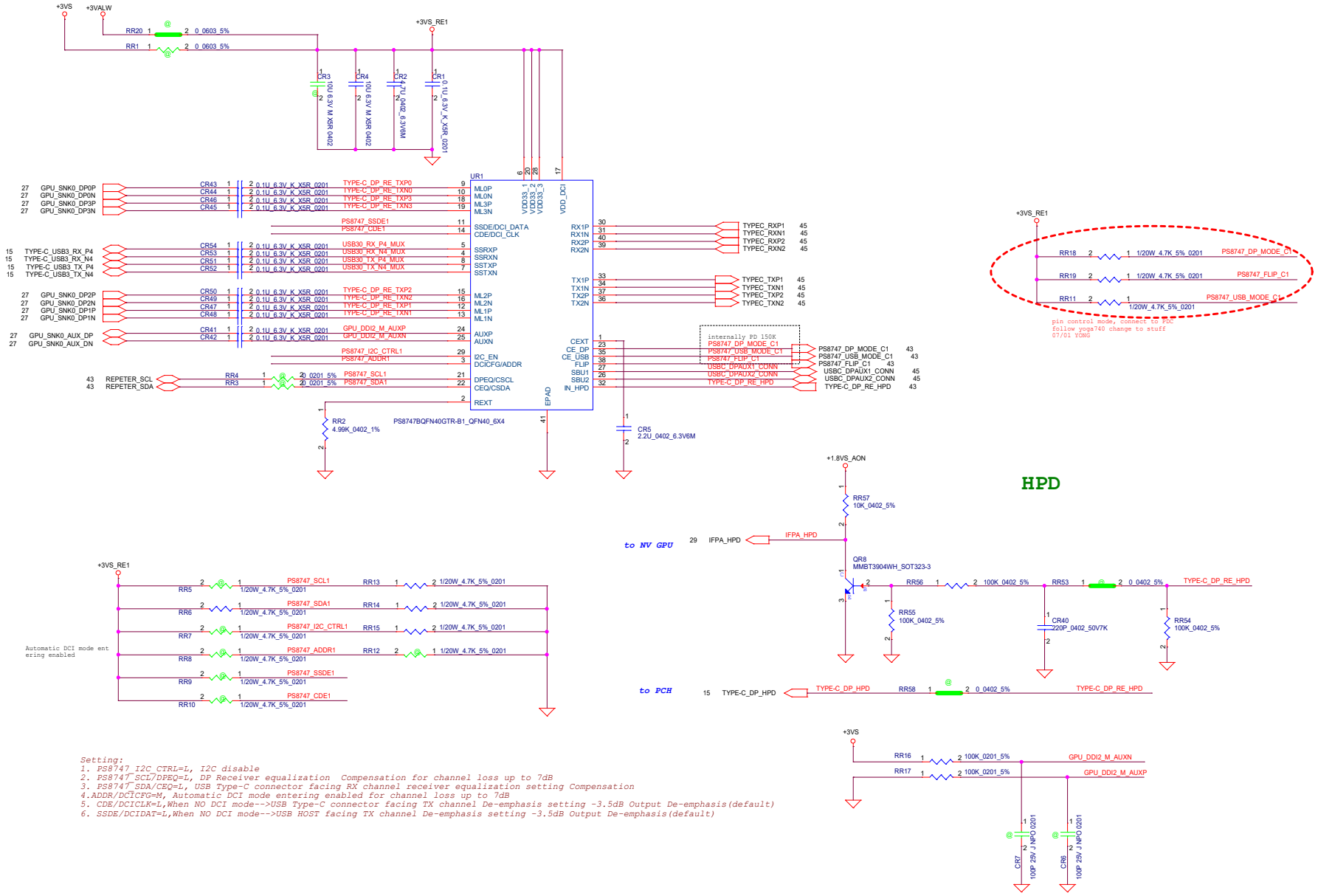
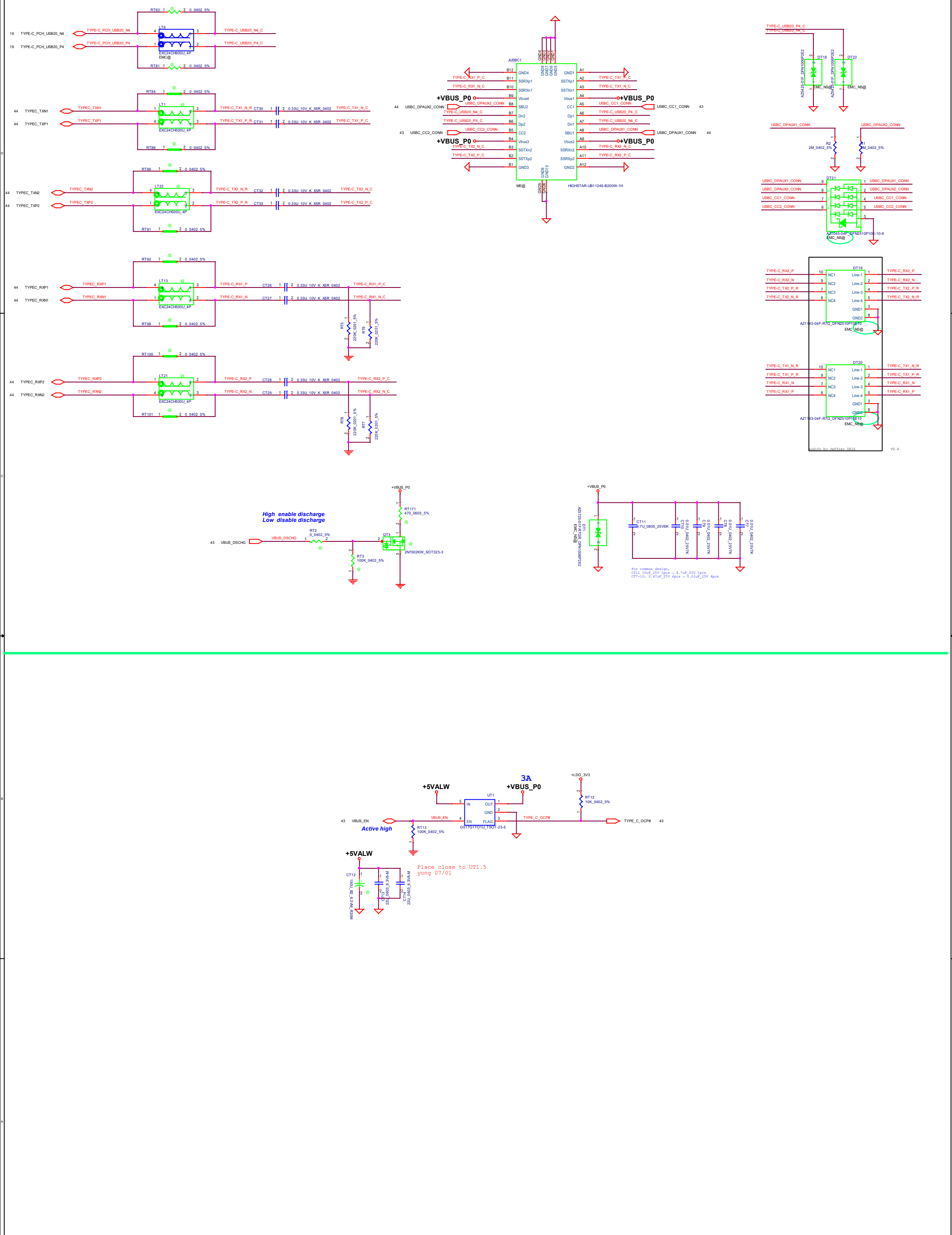


Setting:
1. PS8747_I2C_CTRL=L, I2C disable
2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
4.ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
5. CDE/DCICLK=L,When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
6. SSDE/DCIDAT=L,When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	DDI Redriver PS8330		
Size C	Document Number Y550-CML GN20P		Rev 1.0
Date: Tuesday, April 06, 2021	Sheet 44 of 83		



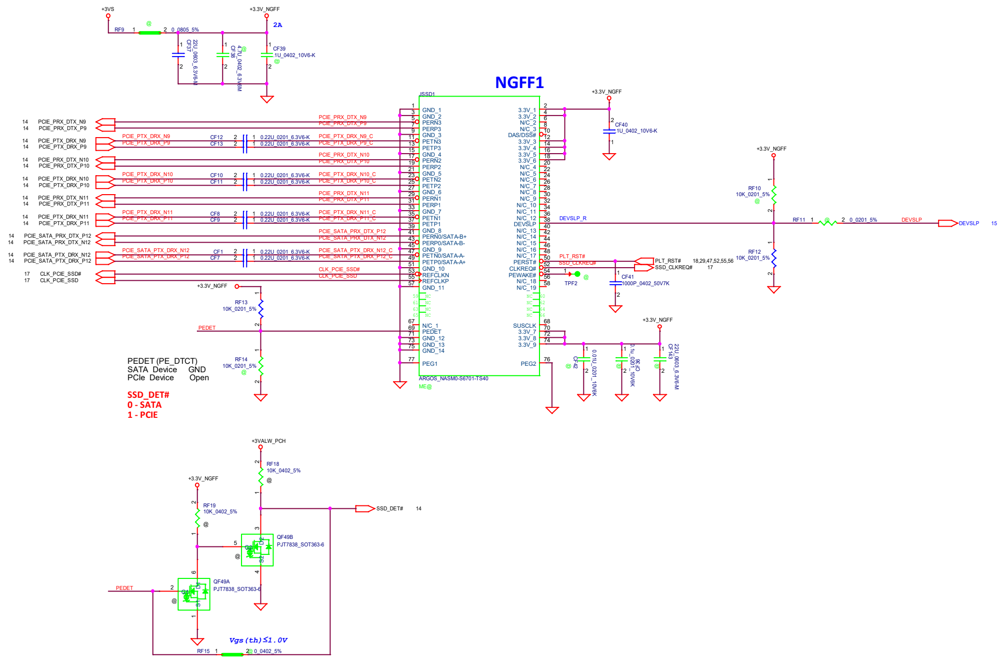
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB TYPE-C Port**

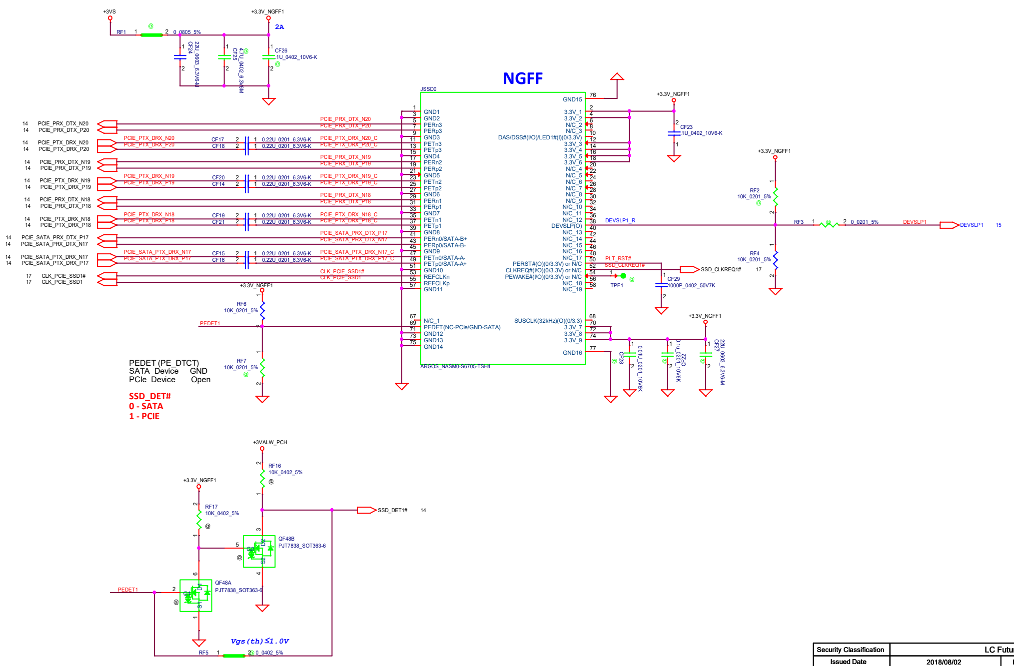
Size	Document Number	Rev
Custom	Y550-CML GN20P	1.0

Date: Tuesday, April 06, 2021

M.2 SSD(SATA/PCIE)



M.2 SSD(SATA/PCIE)



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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title: NGFF WLAN

Size: Custom | Document Number: Y550-CML GN20P | Rev: 1.0

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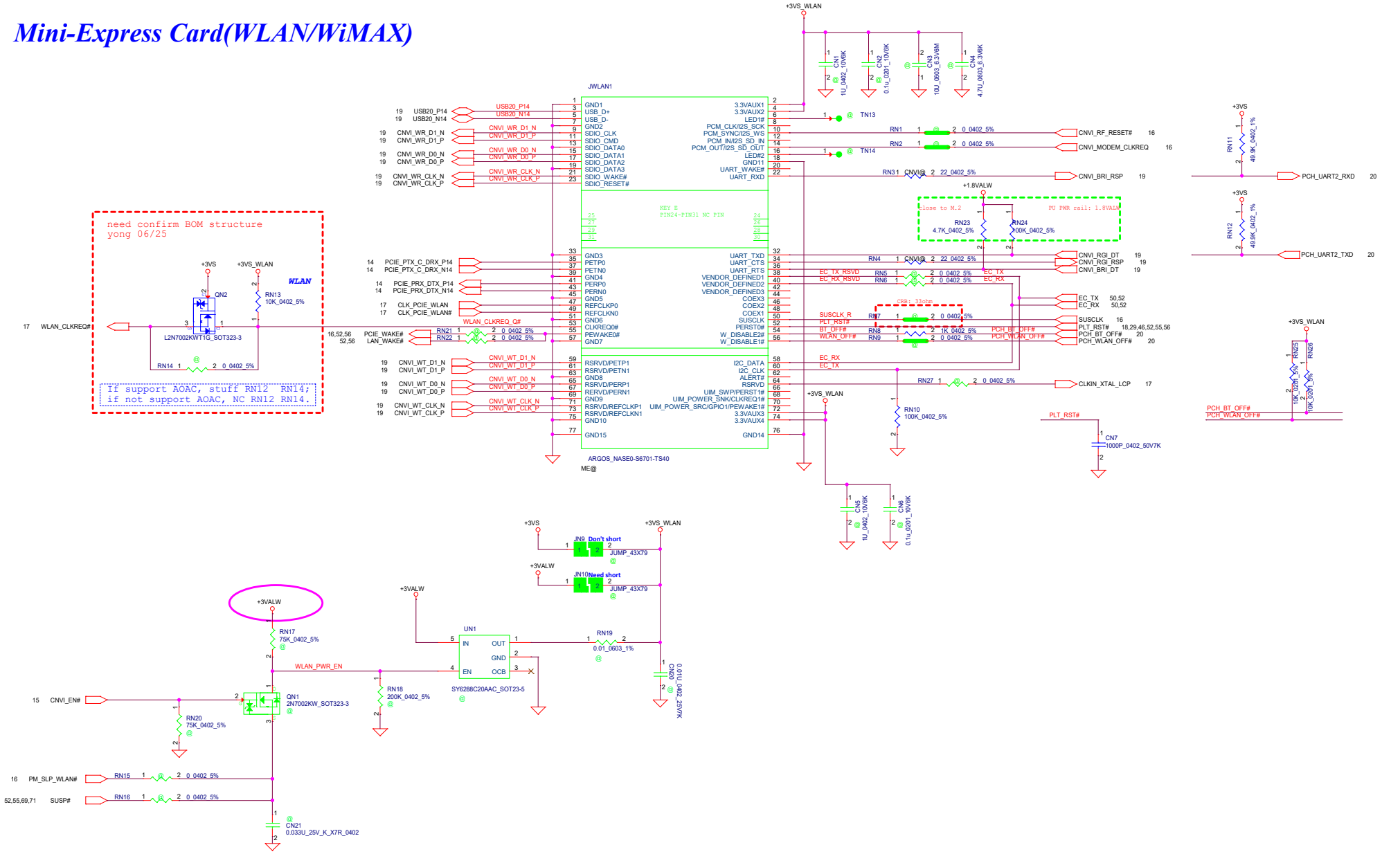
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	CNVi		
Size C	Document Number Y550-CML GN20P		Rev 1.0
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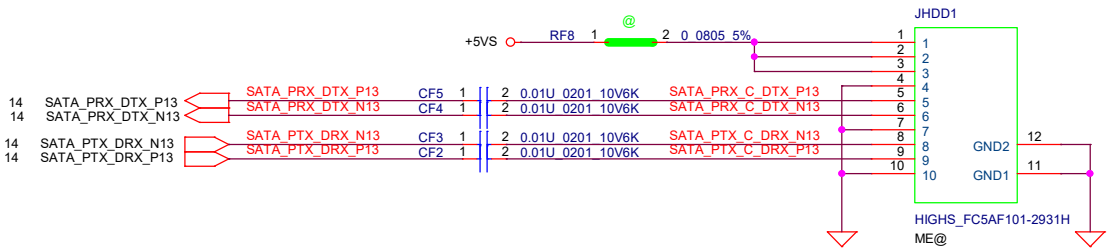
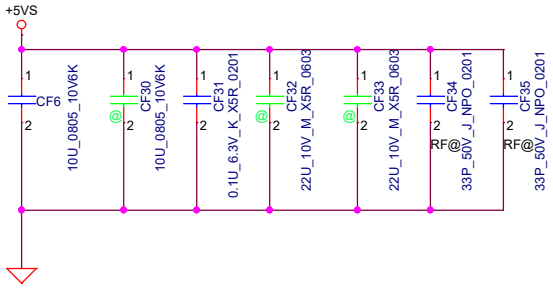
SATA HDD Conn.





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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	HDD/XBOX CONN		
Size B	Document Number Y550-CML GN20P		Rev 1.0
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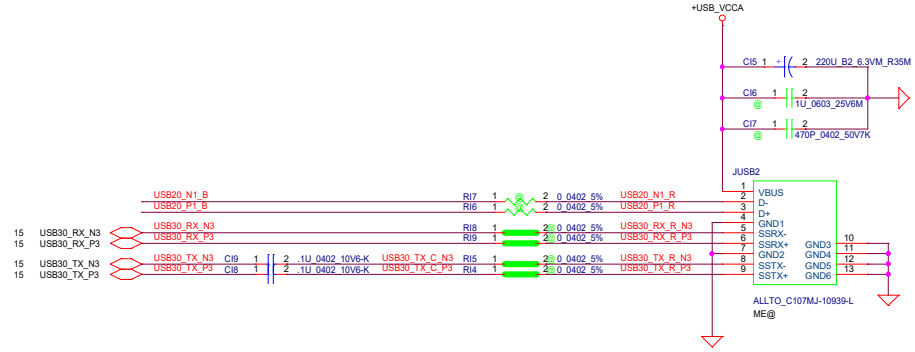
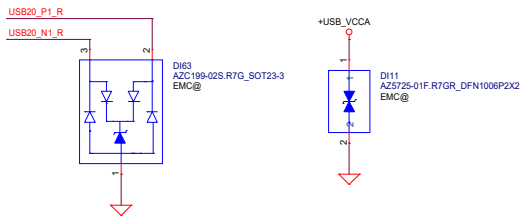
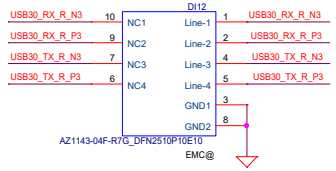
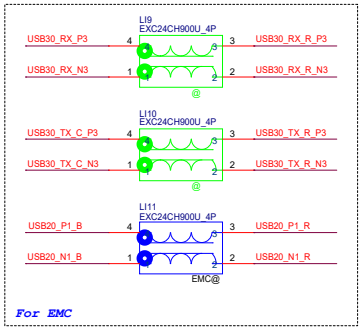




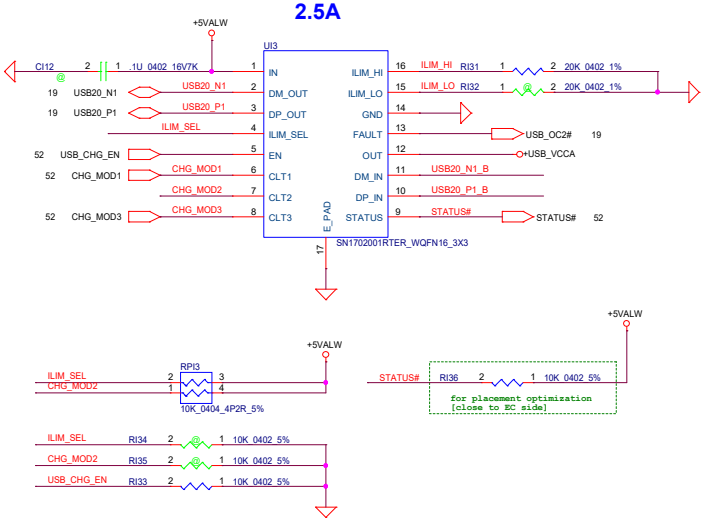


For EMC



For EMC

USB charger
2.5A



CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
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Title	USB2.0/USB3.0 PORT (LEFT)		
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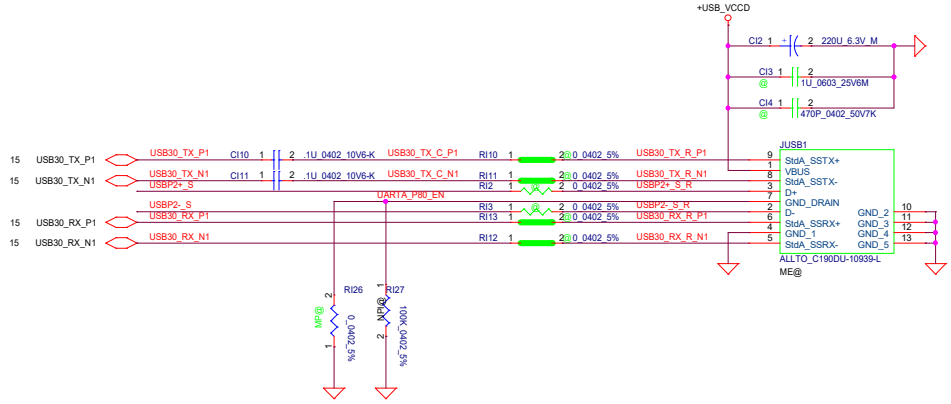
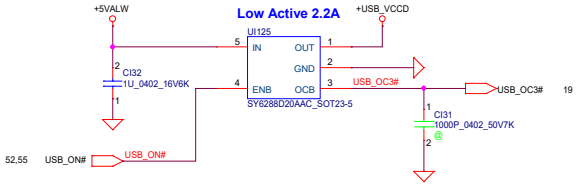
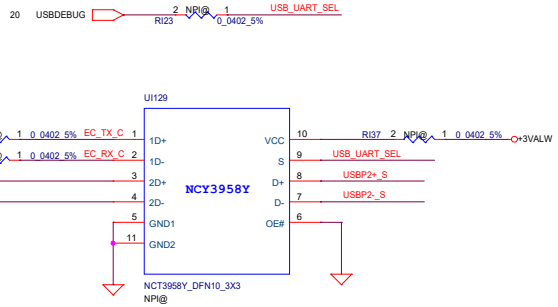


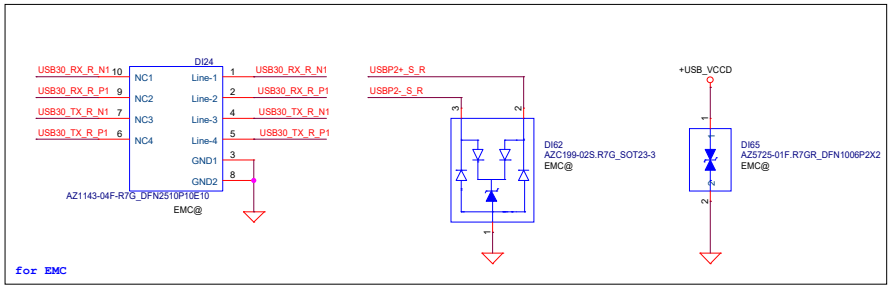
USB3.1 PORT x2

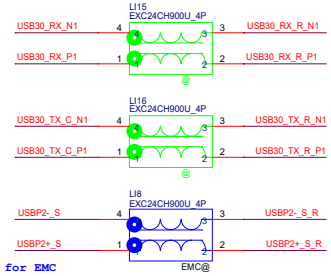


teknisi-indonesia

For USB Debug Function



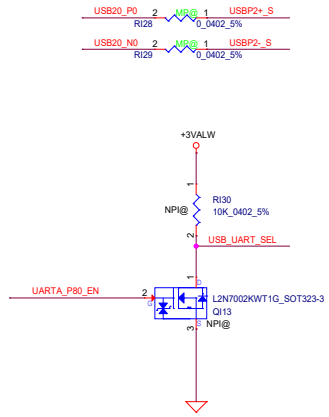




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title			
USB2.0			
Size C	Document Number	Y550-CML GN20P	Rev 1.0
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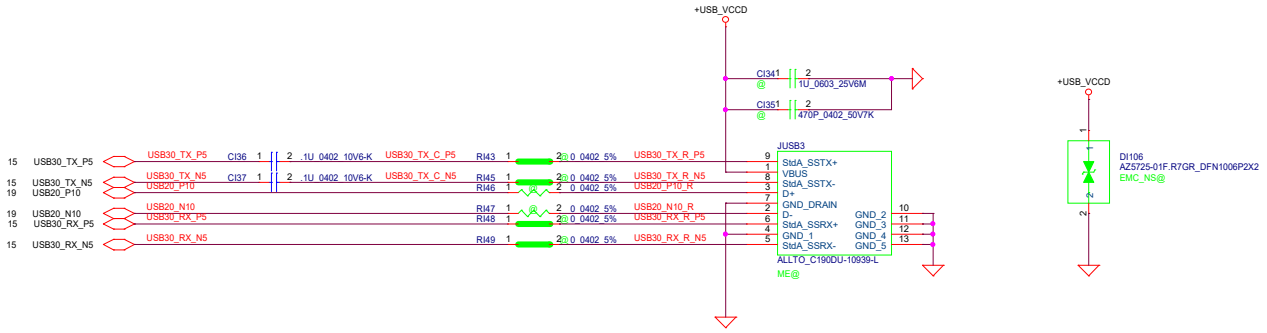

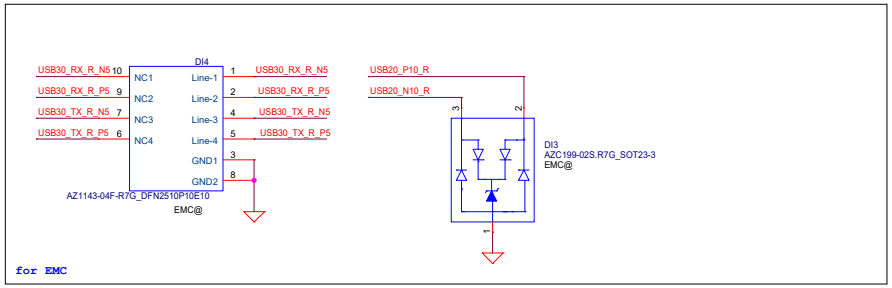

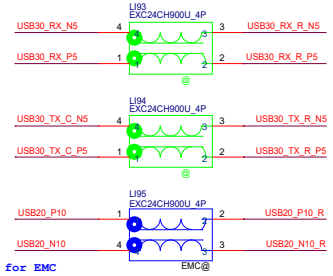

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **USB2.0**

Size	Document Number	Rev
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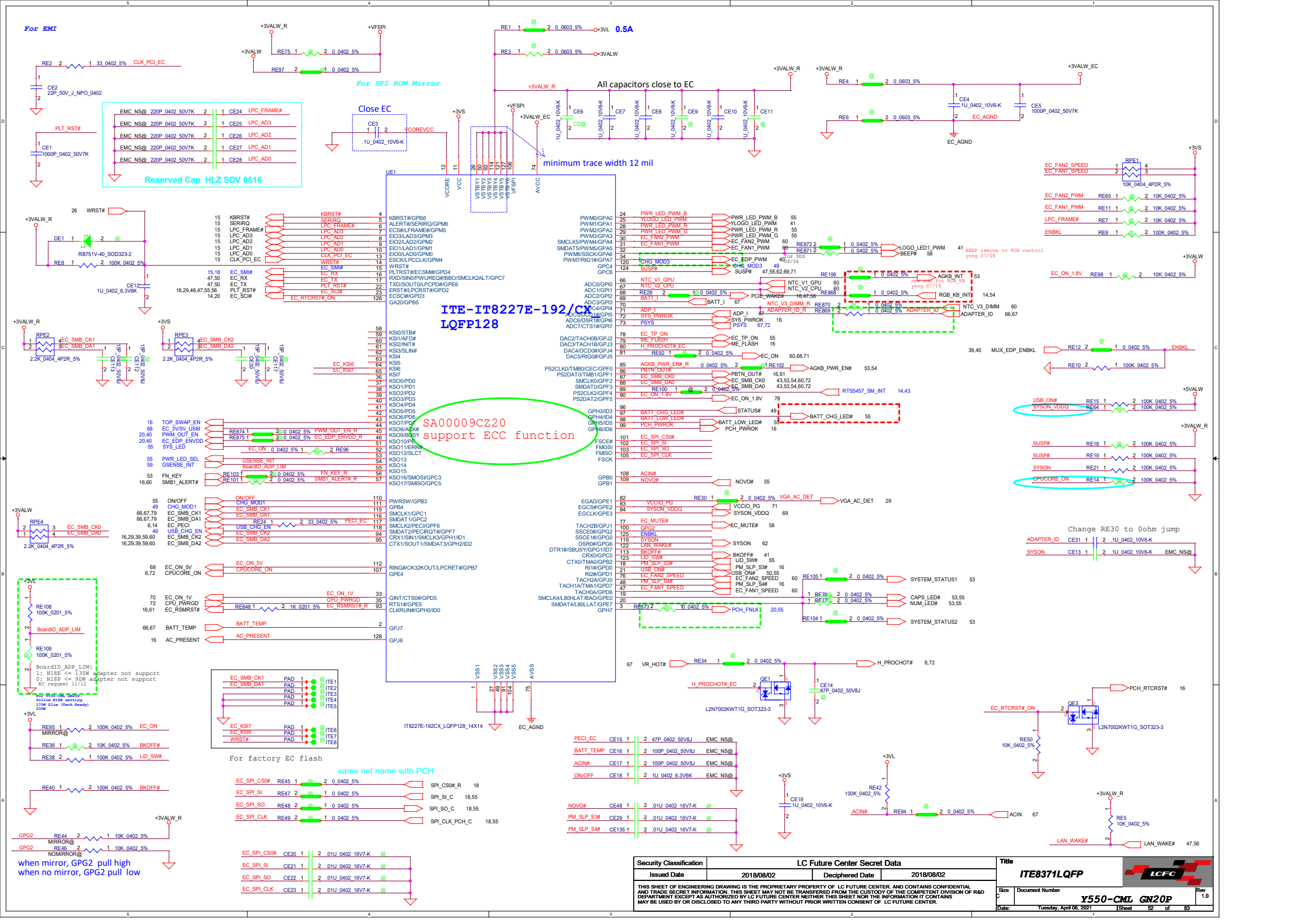
For EMI
For SPI ROM Mirror
Close EC
All capacitors close to EC
minimum trace width 12 mil
Reserved Cap HLZ SDV 0616
ITE-IT8227E-192/CX
LQFP128
SA00009CZ20
support ECC function
Change RE30 to 0ohm jump
For factory EC flash
same net name with PCH
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2018/08/02
Deciphered Date
2018/08/02
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Title
ITE8371LQFP
Size
C
Document Number
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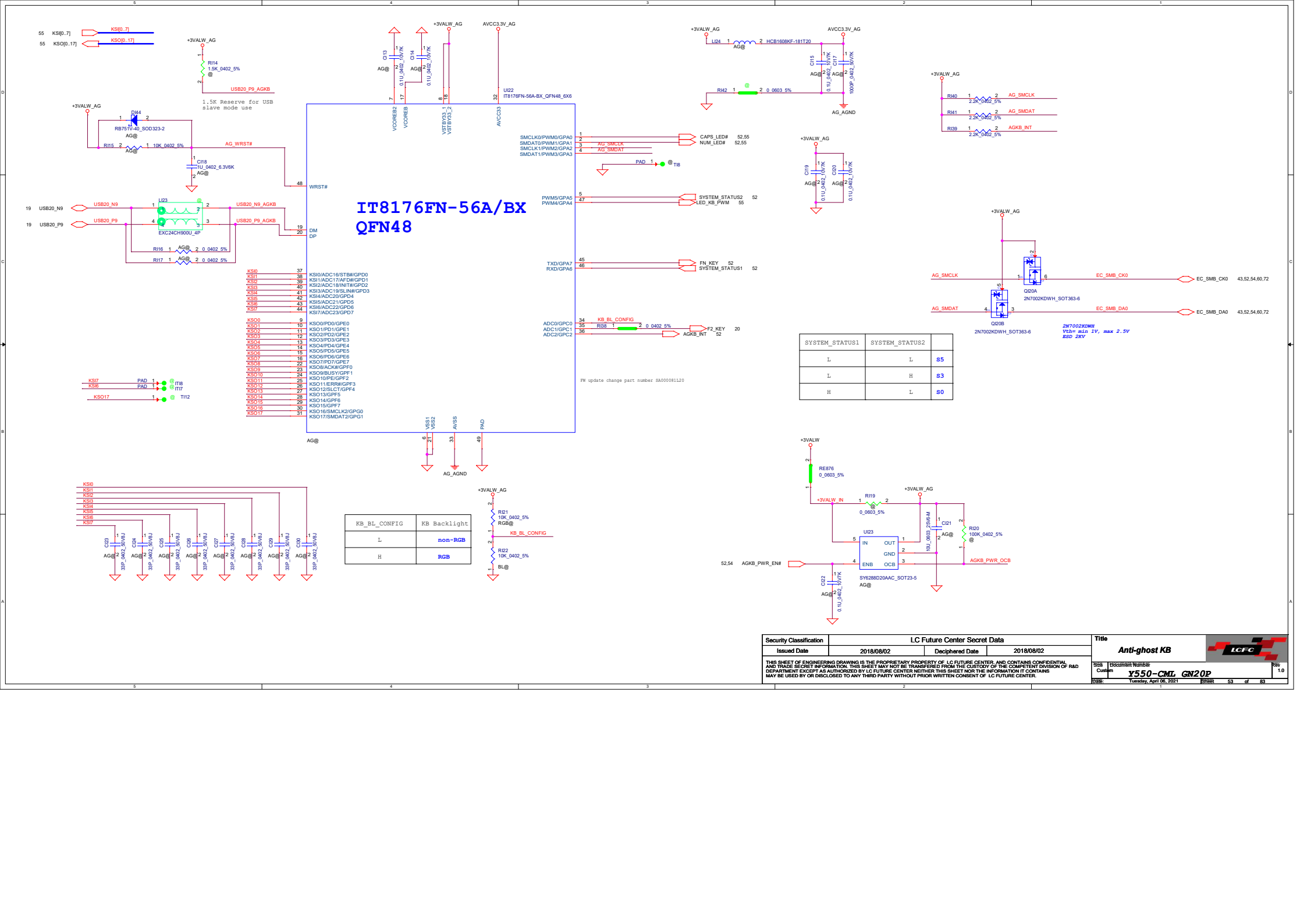
IT8176FN-56A/BX
QFN48
55 KSI[0..7]
55 KSO[0..17]
KSI[0..7]
KSO[0..17]
+3VALW_AG
AVCC3.3V_AG
RI14 1.5K_0402_5%
USB20_P9_AGKB
1.5K Reserve for USB slave mode use
DI44 RB751V-40_SOD323-2
RI15 10K_0402_5%
AG_WRST#
CI18 1U_0402_6.3V6K
LI23 EXC24CH900U_4P
USB20_N9
USB20_P9
USB20_N9_AGKB
USB20_P9_AGKB
RI16 0_0402_5%
RI17 0_0402_5%
CI13 0.1U_0402_10V7K
CI14 0.1U_0402_10V7K
UI22 IT8176FN-56A-BX_QFN48_6X6
VCOREB2
VCOREB
VSTBY33_1
VSTBY33_2
AVCC33
WRST#
DM
DP
KSI0/ADC16/STB#/GPD0
KSI1/ADC17/AFD#/GPD1
KSI2/ADC18/INIT#/GPD2
KSI3/ADC19/SLIN#/GPD3
KSI4/ADC20/GPD4
KSI5/ADC21/GPD5
KSI6/ADC22/GPD6
KSI7/ADC23/GPD7
KSO0/PD0/GPE0
KSO1/PD1/GPE1
KSO2/PD2/GPE2
KSO3/PD3/GPE3
KSO4/PD4/GPE4
KSO5/PD5/GPE5
KSO6/PD6/GPE6
KSO7/PD7/GPE7
KSO8/ACK#/GPF0
KSO9/BUSY/GPF1
KSO10/PE/GPF2
KSO11/ERR#/GPF3
KSO12/SLCT/GPF4
KSO13/GPF5
KSO14/GPF6
KSO15/GPF7
KSO16/SMCLK2/GPG0
KSO17/SMDAT2/GPG1
SMCLK0/PWM0/GPA0
SMDAT0/PWM1/GPA1
SMCLK1/PWM2/GPA2
SMDAT1/PWM3/GPA3
CAPS_LED# 52,55
NUM_LED# 52,55
AG_SMCLK
AG_SMDAT
PAD
TI8
PWM5/GPA5
PWM4/GPA4
SYSTEM_STATUS2 52
LED_KB_PWM 55
TXD/GPA7
RXD/GPA6
FN_KEY 52
SYSTEM_STATUS1 52
ADC0/GPC0
ADC1/GPC1
ADC2/GPC2
KB_BL_CONFIG
RI38 0_0402_5%
F2_KEY 20
AGKB_INT 52
FW update change part number SA000081L20
VSS1
VSS2
AVSS
PAD
AG_AGND
KSI7
KSI6
KSO17
TI18
TI17
TI12
LI24 HCB1608KF-181T20
RI42 0_0603_5%
CI15 0.1U_0402_10V7K
CI17 1000P_0402_50V7K
AG_AGND
RI40 2.2K_0402_5%
RI41 2.2K_0402_5%
RI39 2.2K_0402_5%
AG_SMCLK
AG_SMDAT
AGKB_INT
CI19 0.1U_0402_10V7K
CI20 0.1U_0402_10V7K
QI20A 2N7002KDWH_SOT363-6
QI20B 2N7002KDWH_SOT363-6
EC_SMB_CK0 43,52,54,60,72
EC_SMB_DA0 43,52,54,60,72
2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV
SYSTEM_STATUS1 SYSTEM_STATUS2
L L S5
L H S3
H L S0
KB_BL_CONFIG KB Backlight
L non-RGB
H RGB
RI21 10K_0402_5% RGB@
RI22 10K_0402_5% BL@
KB_BL_CONFIG
RE876 0_0603_5%
+3VALW_IN
RI19 0_0603_5%
UI23 SY8288D20AAC_SOT23-5
IN
OUT
GND
ENB
OCB
CI21 10U_0603_25V6M
RI20 100K_0402_5%
AGKB_PWR_EN# 52,54
AGKB_PWR_OCB
CI22 0.1U_0402_10V7K
C23 C24 C25 C26 C27 C28 C29 C30 33P_0402_50V8J
Security Classification LC Future Center Secret Data
Issued Date 2018/08/02
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Title Anti-ghost KB
Size Custom
Document Number Y550-CML GN20P
Rev 1.0
Date: Tuesday, April 06, 2021
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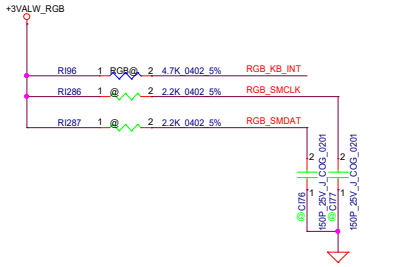

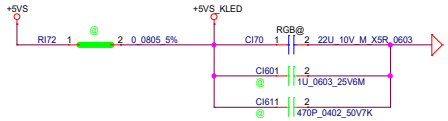

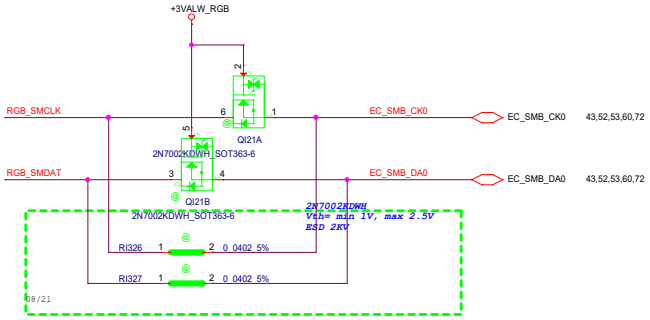

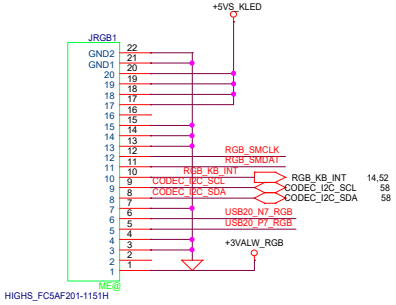

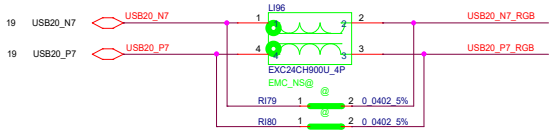

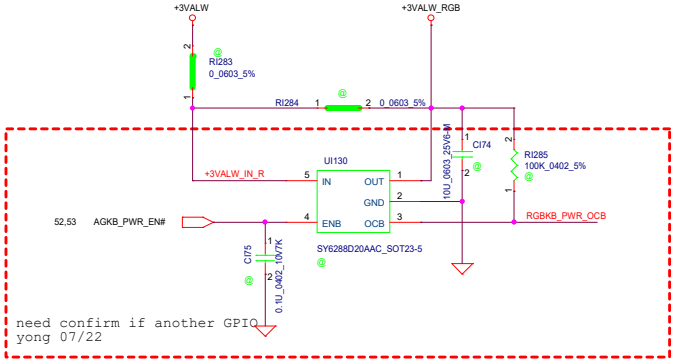

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	RGB KB		
Size C	Document Number	Y550-CML GN20P	Rev 1.0
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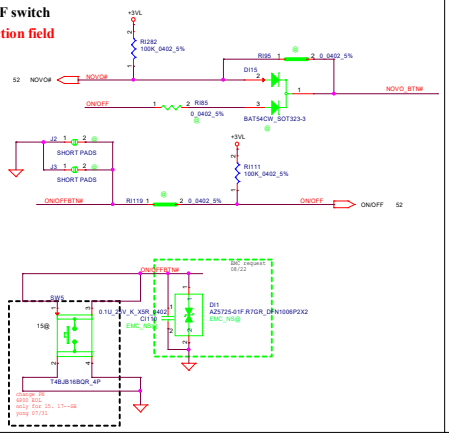
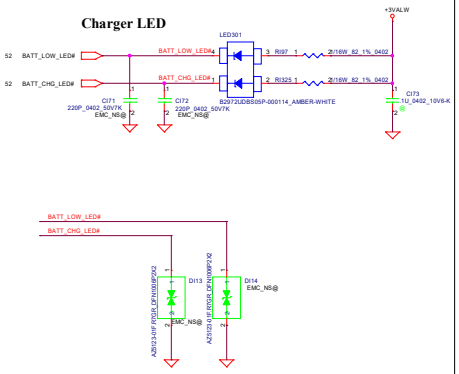
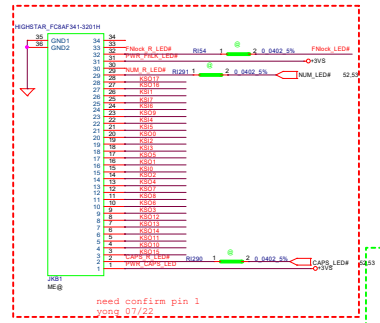
ON/OFF switch

No function field

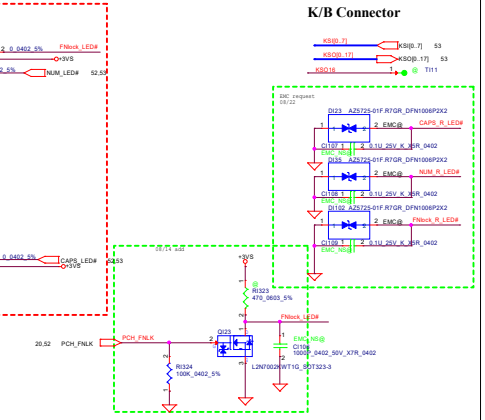


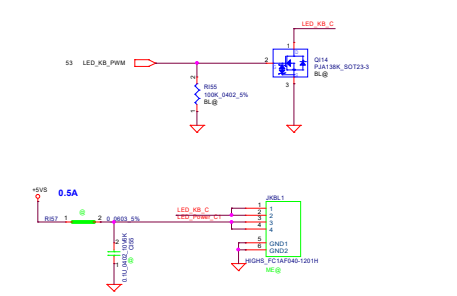
Charger LED

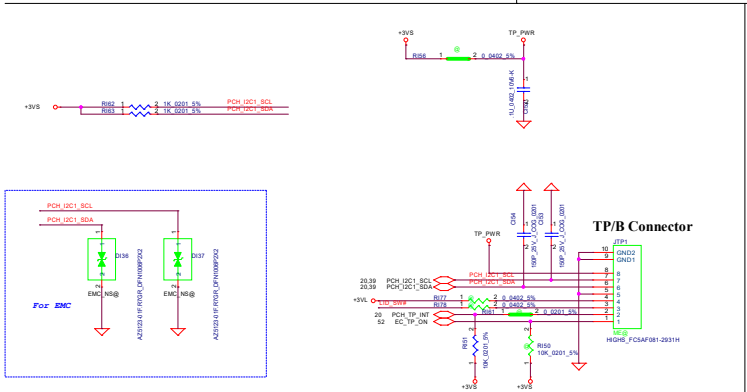




K/B Connector

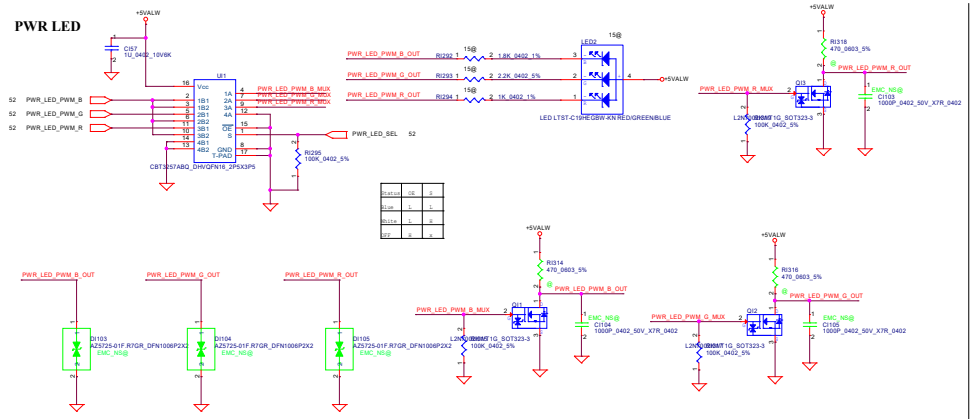






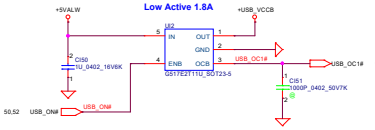
TP/B Connector

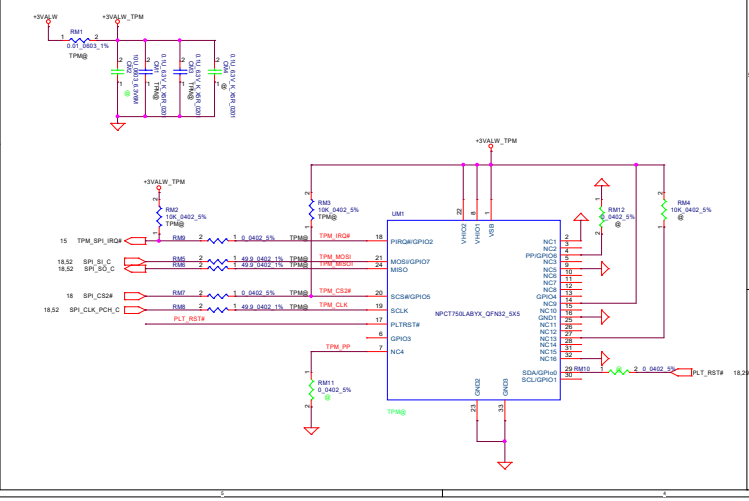
PWR LED



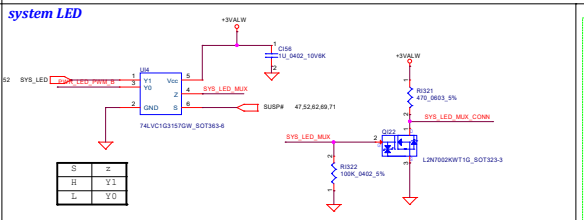
USB3.1 PORT x1

Low Active 1.8A

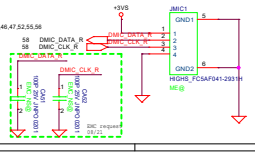




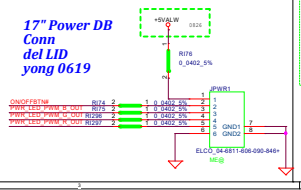
system LED

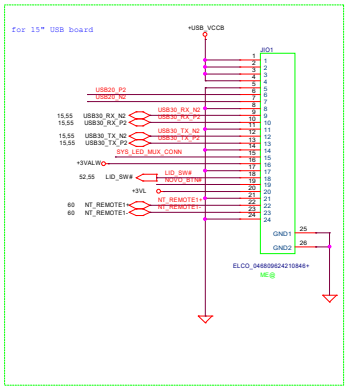


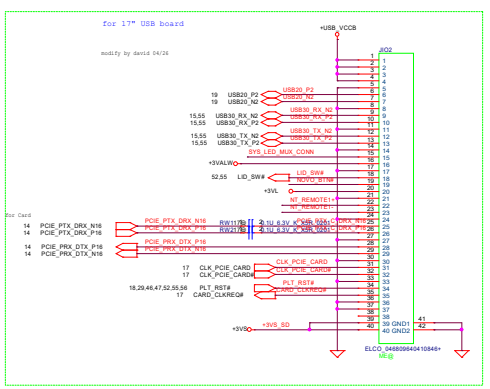
MIC board



17" Power DB Conn del LID yong 0619







Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

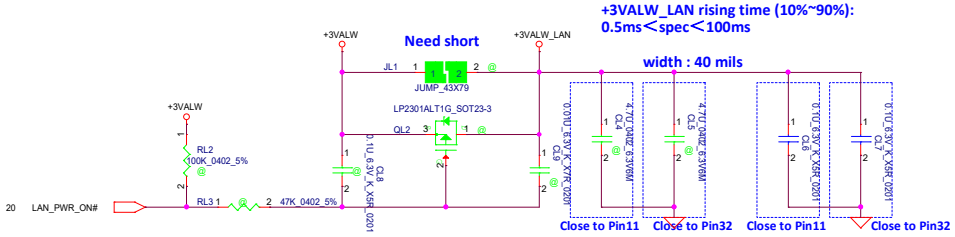
Title	KBD/PWR/IO/LED/TP Conn.
Size: LCD	Document Number: Y550-CML GN20P
Date: Tuesday, April 09, 2019	Sheet 55 of 63

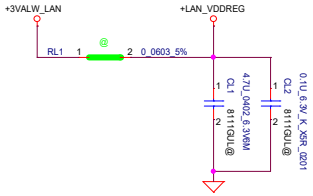
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms＜spec＜100ms

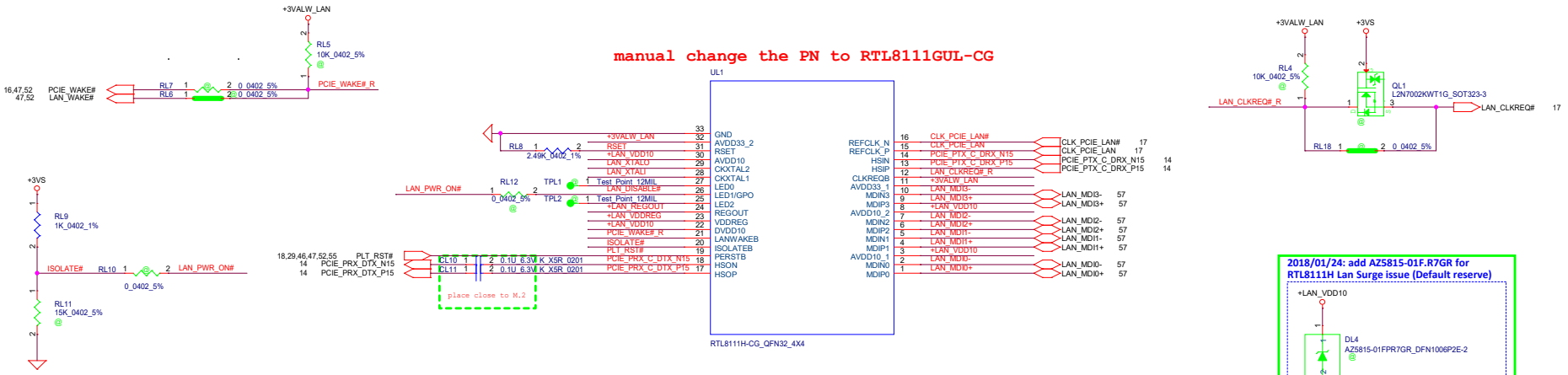
Need short

width : 40 mils

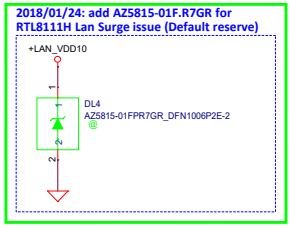




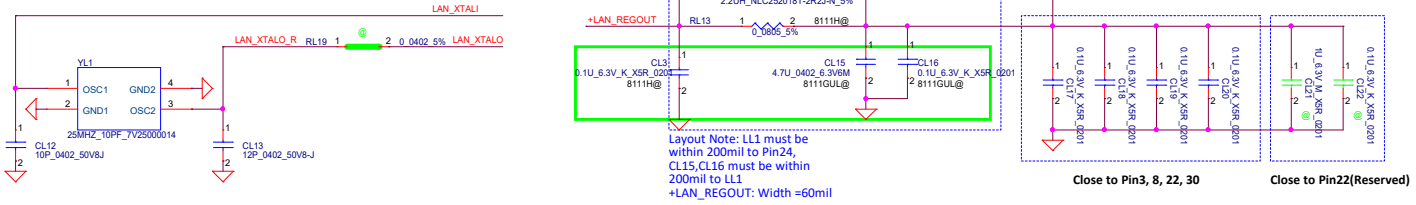
manual change the PN to RTL8111GUL-CG



2018/01/24: add AZ5815-01F.R7GR for RTL8111H Lan Surge issue (Default reserve)



For RTL8111GUL(SWR mode)
For RTL8111H (LDO mode)



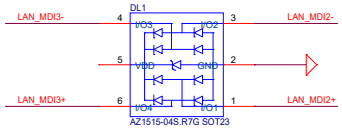
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Security Classification	LC Future Center Secret Data		
Issued Date	2019/02/13	Deciphered Date	2019/02/13

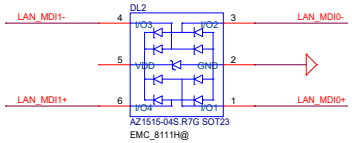
Title	LAN_RTL8111GUL_H		
Size	Document Number		Rev
C	Y550-CML GN20P		1.0
Date:	Tuesday, April 06, 2021	Sheet	56 of 83

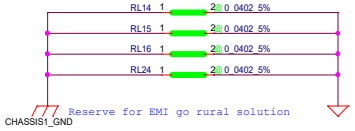
DL1/DL2
1'S PN:SC300008P00

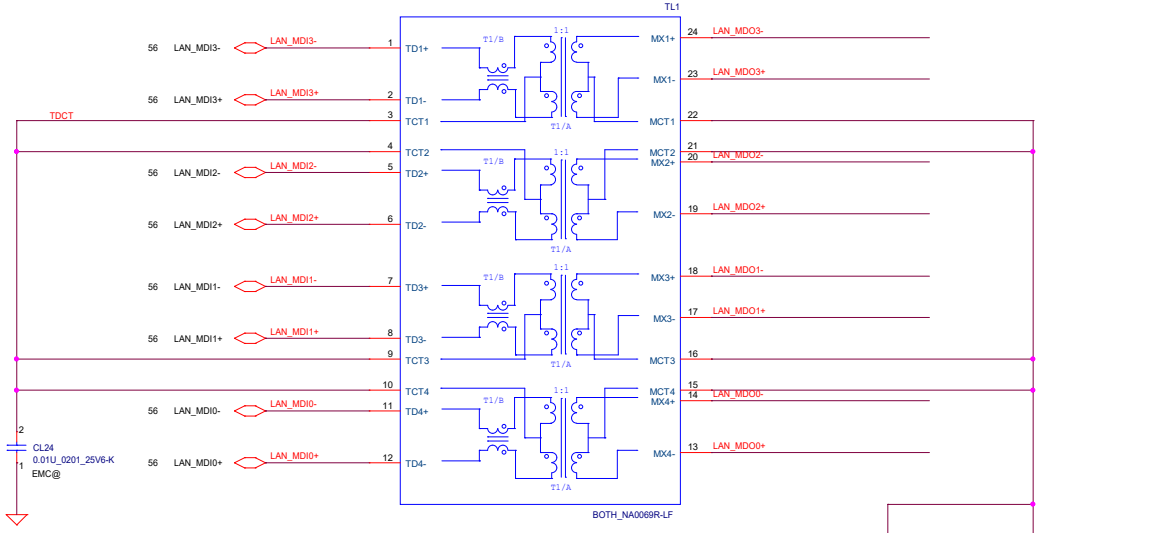
Place Close to TL1

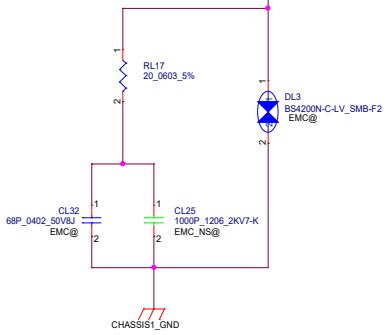


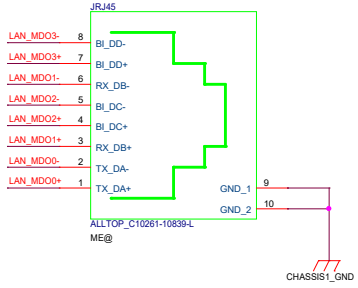
AZ1215-04S SC300005900 2021/10 EOL
New substitute material:
change to AZ1515-04S SC300008P00 2020/12/07









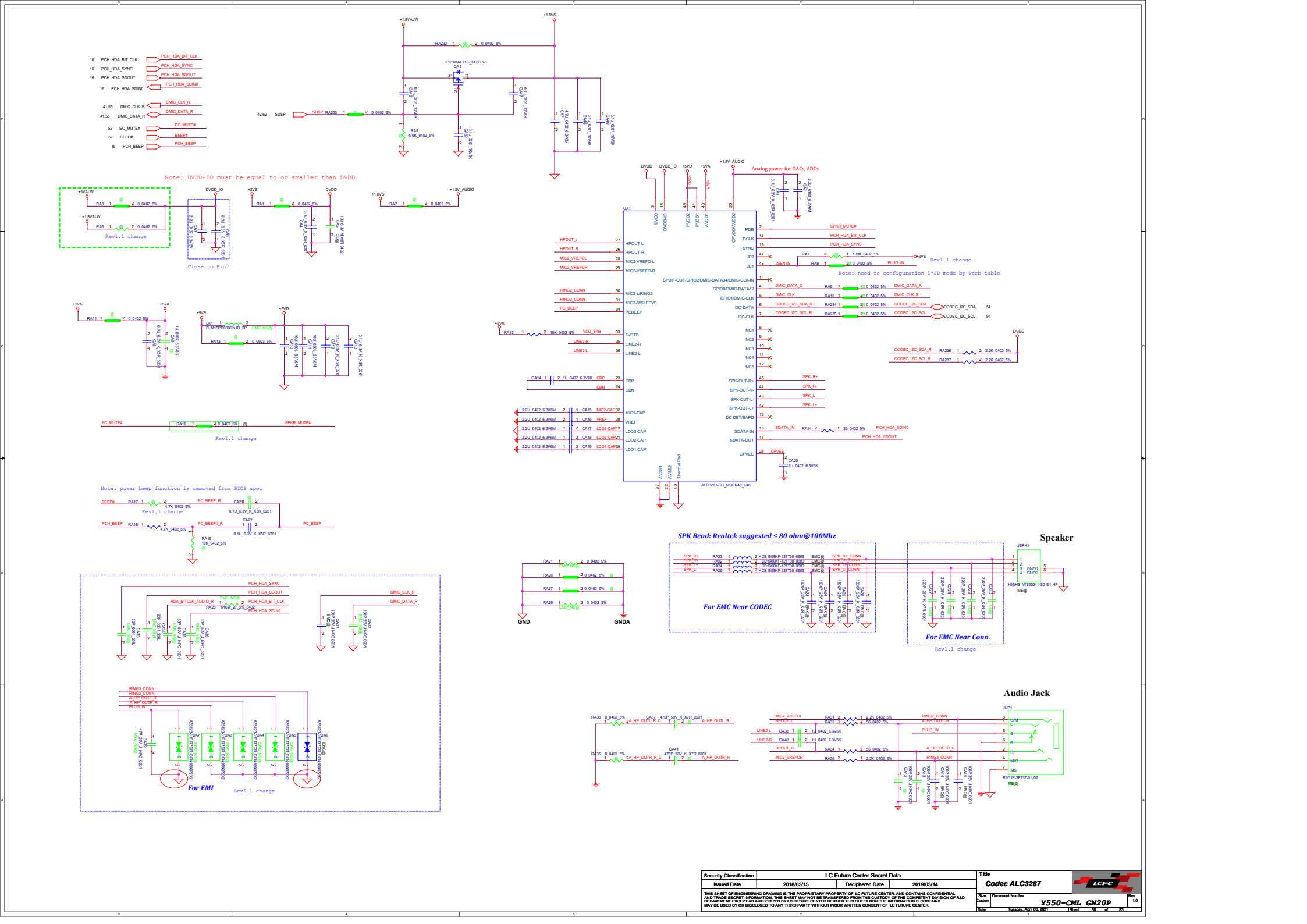


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: LAN_Transformer

Size	Document Number	Rev
C	Y550-CML GN20P	1.0

Date: Tuesday, April 06, 2021 Sheet 57 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/03/15	Deciphered Date	2019/03/14

Title	Codec ALC3287		
Size: Custom	Document Number: Y550-CML GN20P		Rev: 1.0
Date: Tuesday, April 06, 2021	Sheet 58 of 83		

APS G-Sensor

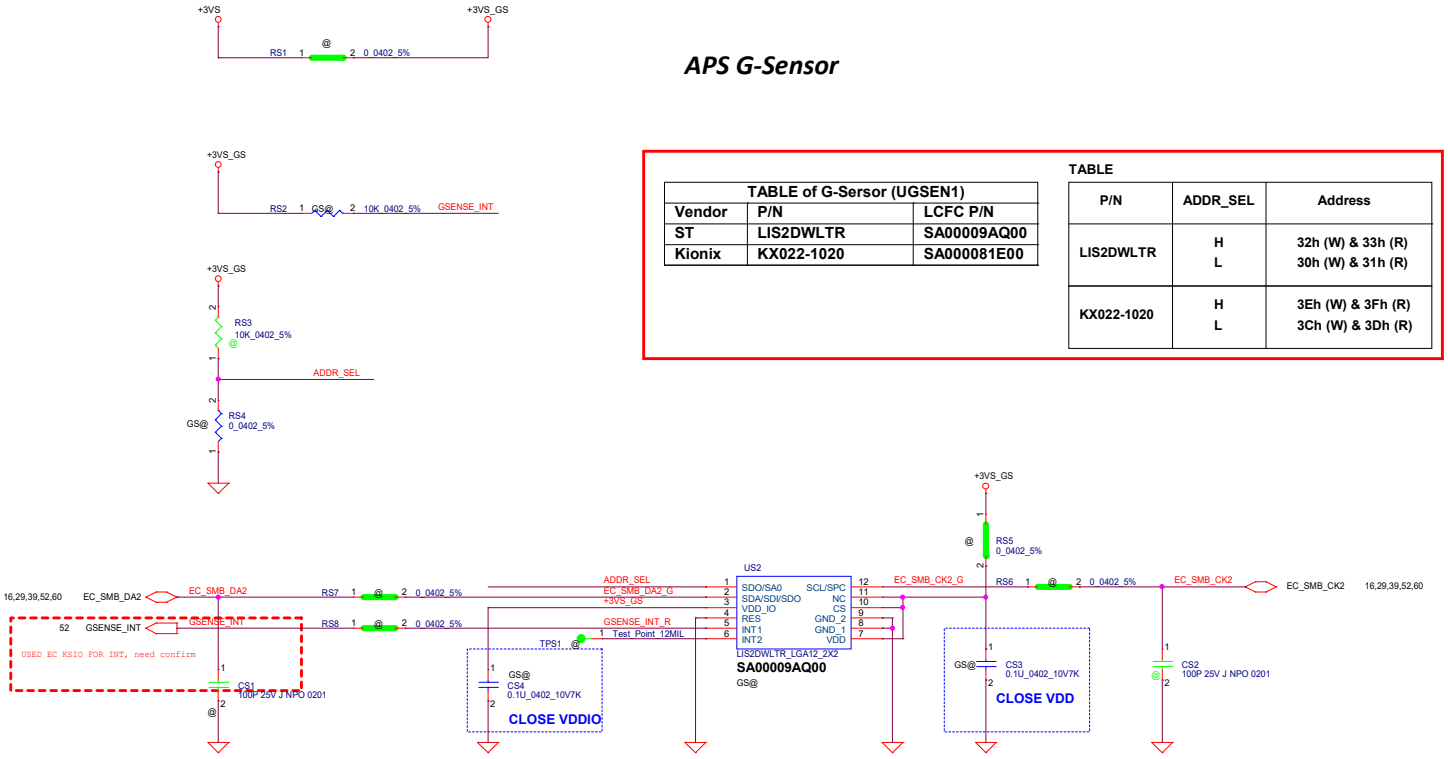


TABLE of G-Sersor (UGSEN1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00

TABLE

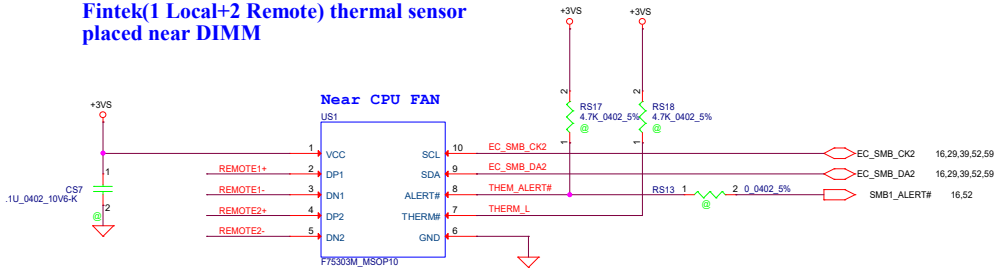
P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

Title: USB2.0

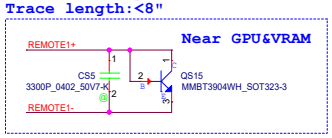
Size	Document Number	Rev
C	Y550-CML GN20P	1.0

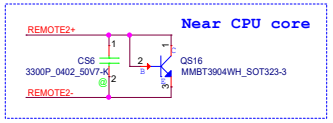
Date: Tuesday, April 06, 2021 Sheet 59 of 83

Fintek(1 Local+2 Remote) thermal sensor placed near DIMM

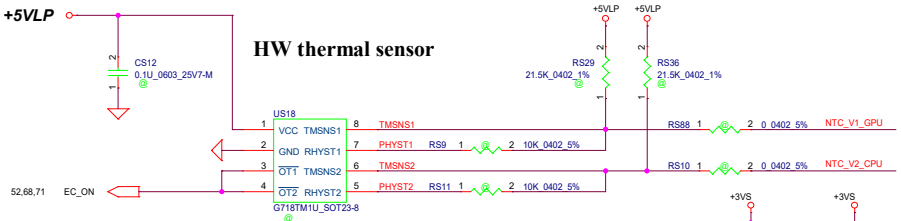


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

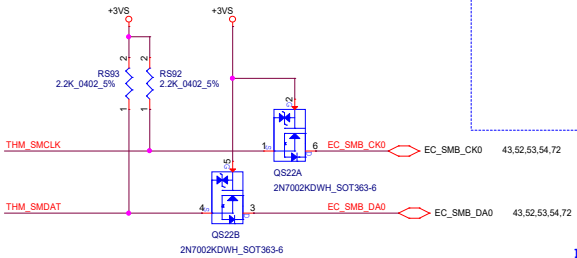


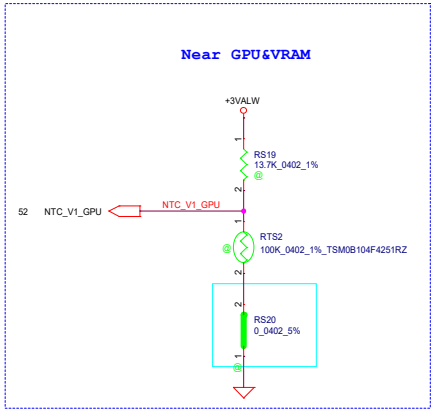


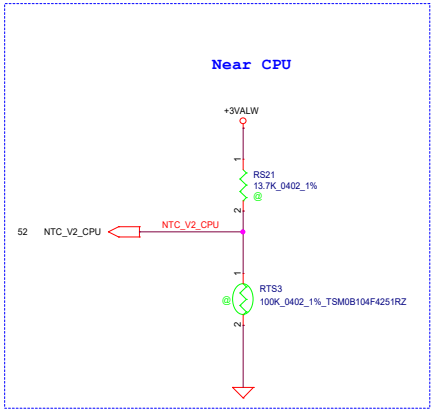
HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

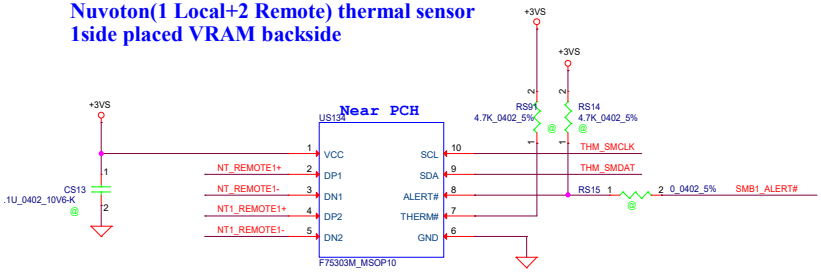




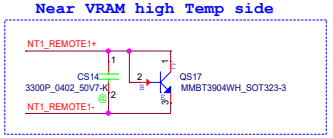


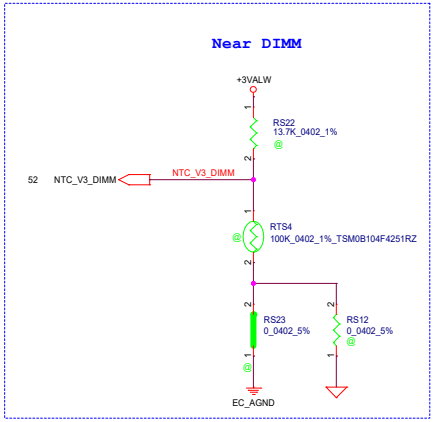
for layout optimized, change the EC_AGND to GND

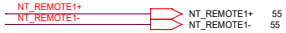
Nuvoton(1 Local+2 Remote) thermal sensor 1side placed VRAM backside



teknisi-indonesia



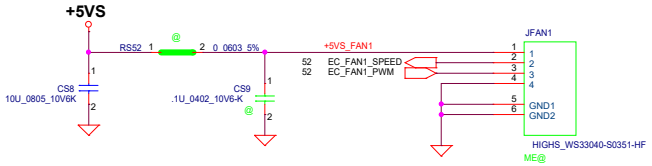




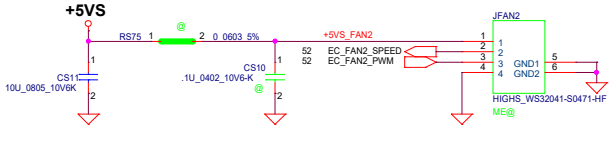
Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

FAN Conn Right



FAN Conn LEFT



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	Thermal sensor/FAN CONN		
Size C	Document Number Y550-CML GN20P		Rev 1.0
Date: Tuesday, April 06, 2021		Sheet 60 of 83	

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

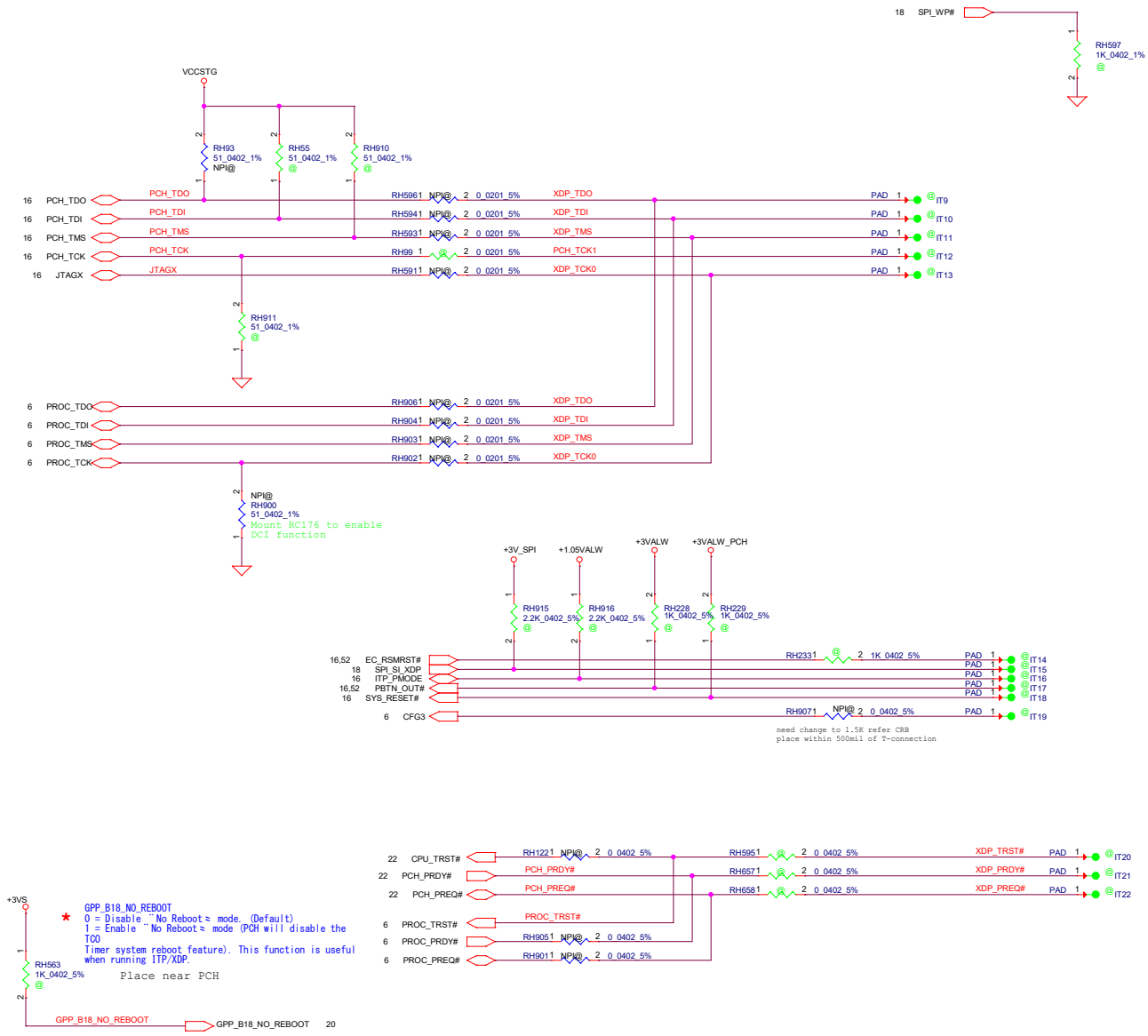
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



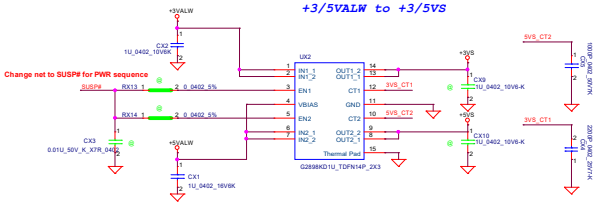
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

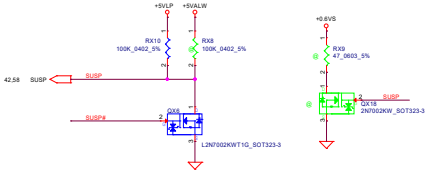
Title: XDP

Size: Custom | Document Number: Y550-CML GN20P | Rev: 1.0

Date: Tuesday, April 06, 2021 | Sheet 61 of 83

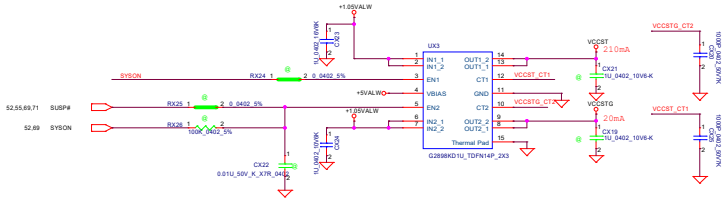
+3/5VALW to +3/5VS





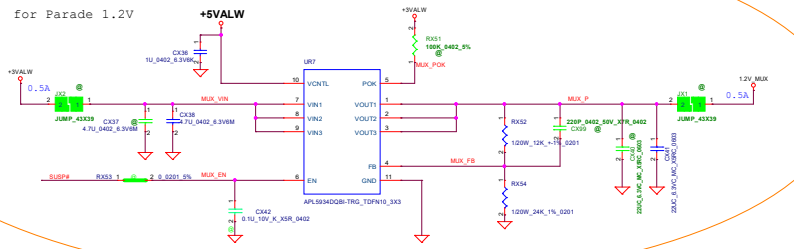
+1.8VALW to +1.8VS_AON

Page 32 contain "+1.8VALW to +1.8VS_AON "



eDP MUX power

for Parade 1.2V



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title	DC V TO VS INTERFACE	
Size: D	Document Number: Y550-CML GN20P	Rev: 1.0
Date: Tuesday, April 06, 2021	Sheet 62 of 63	

SKU ID	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21
Y550-15-GN20P0	0	0	0	0
Y550-15-GN20P1	0	0	0	1

HDMI Logo(SVT Phase need add)

HDMI Logo

1.NPI Phase 43J --- MB PCB PN;
2.SVT PCB version upgraded to 1.0, 43J ---Panel PCB DAZ PN(MB+DB).

PCB MB

CPU

PCH

GPU

GN20x-P P0-QS2 sample

GN20x-P P1-MP sample

Samsung 4GB VRAM

STRAP0: L *STRAP1: L* *STRAP2: L*

Hynix 4GB VRAM

STRAP0: L *STRAP1: H* *STRAP2: L*

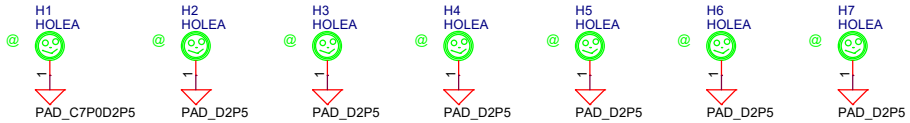
Micron 4GB VRAM

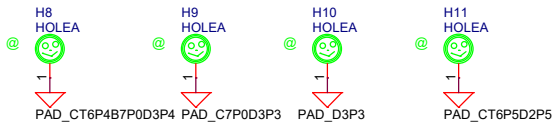
STRAP0: H *STRAP1: L* *STRAP2: L*

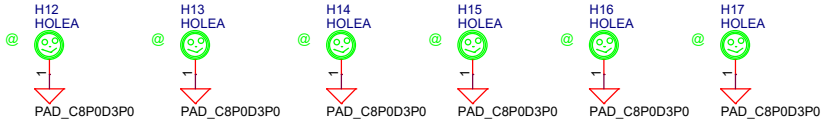
Title: *Virtual symbol*

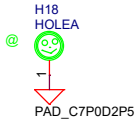
Size	Document Number	Rev
C	Y550-CML GN20P	1.0

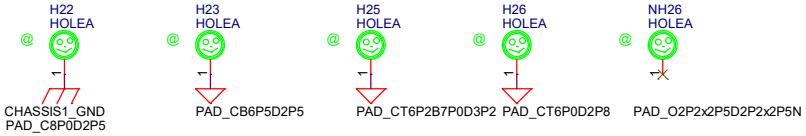
Date: Tuesday, April 06, 2021 Sheet 63 of 83

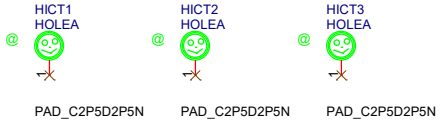


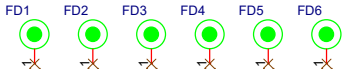


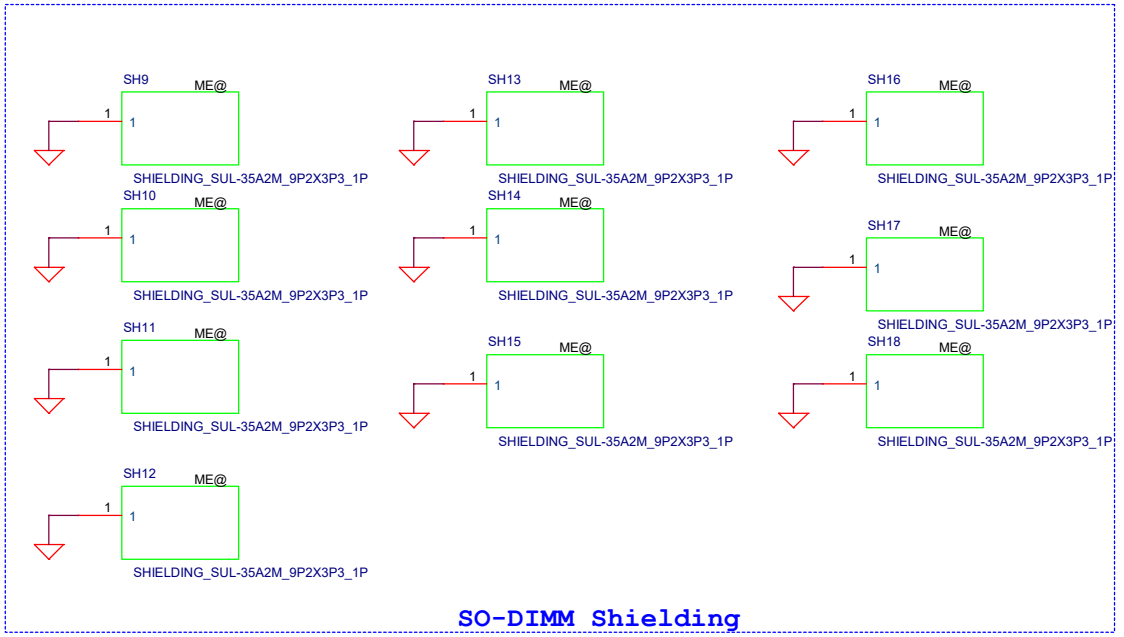












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Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **Hole**

Size	Document Number	Rev
B	Y550-CML GN20P	1.0

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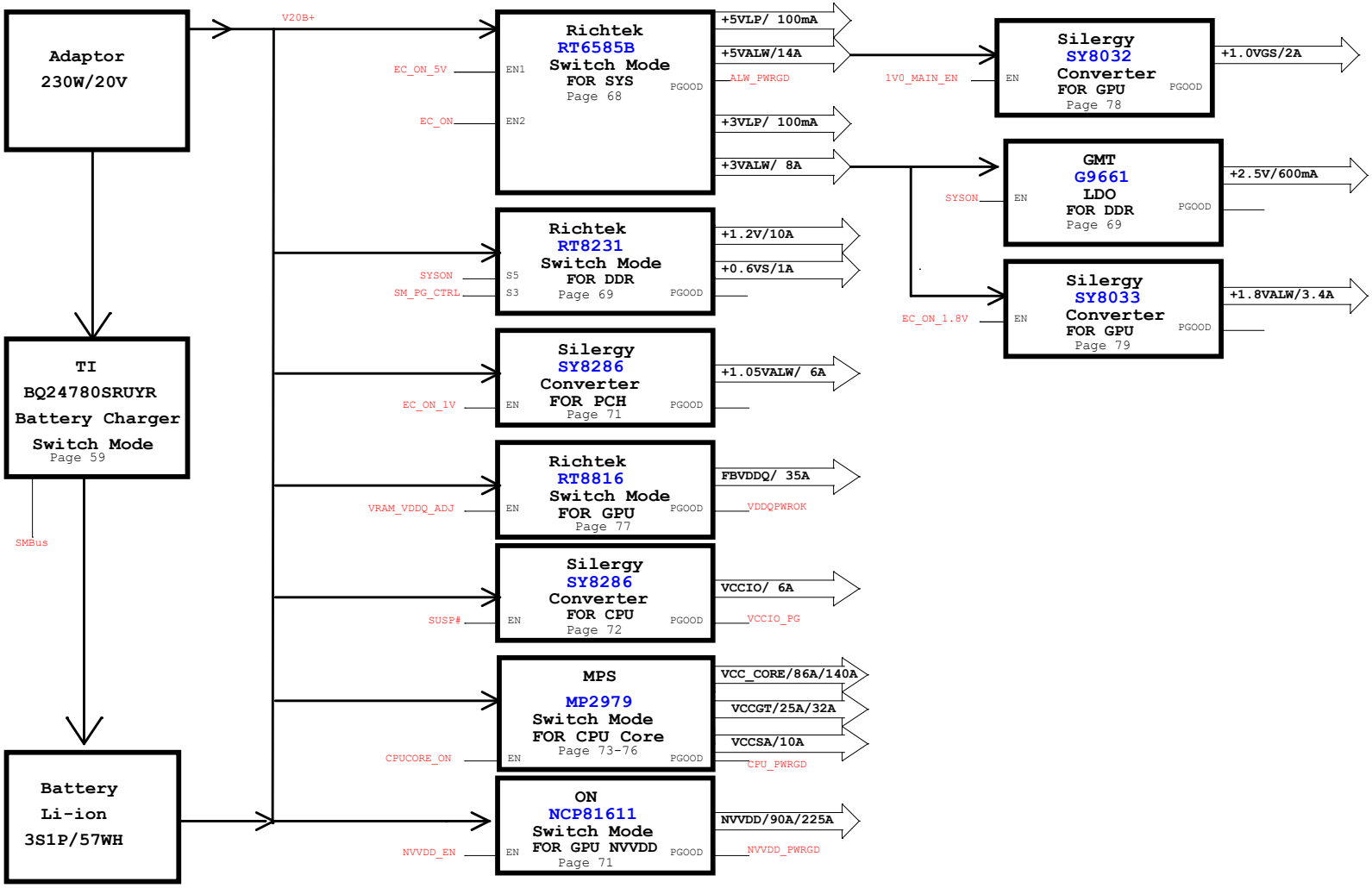
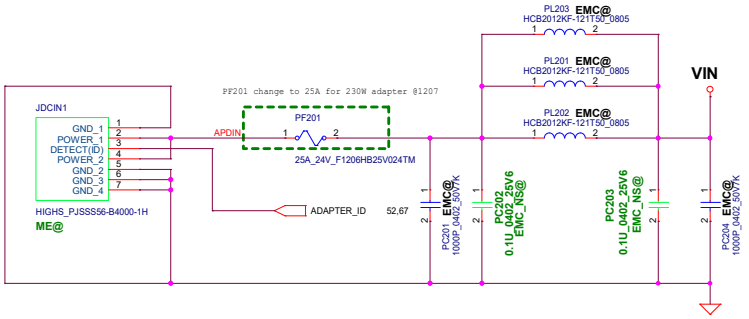


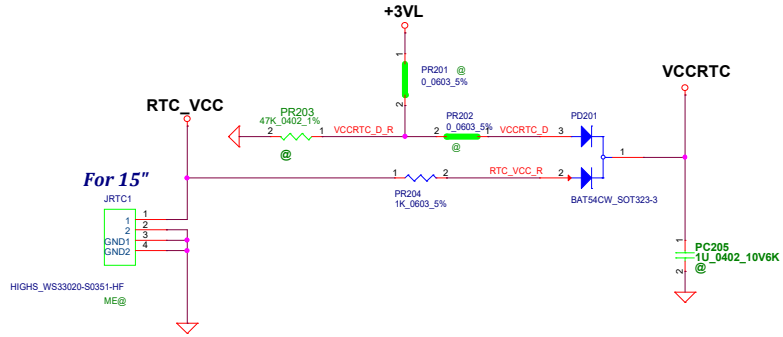
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

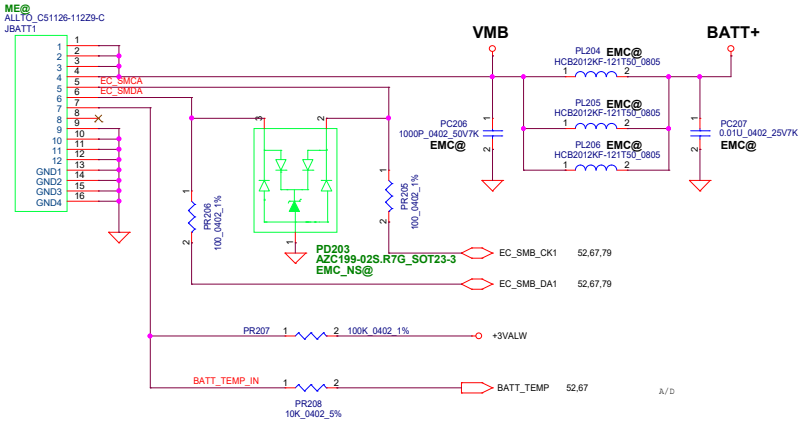
Title: **Power Diagram**

Size	Document Number	Rev
Custom	Y550	1.0

Date: Tuesday, April 06, 2021 Sheet 65 of 83

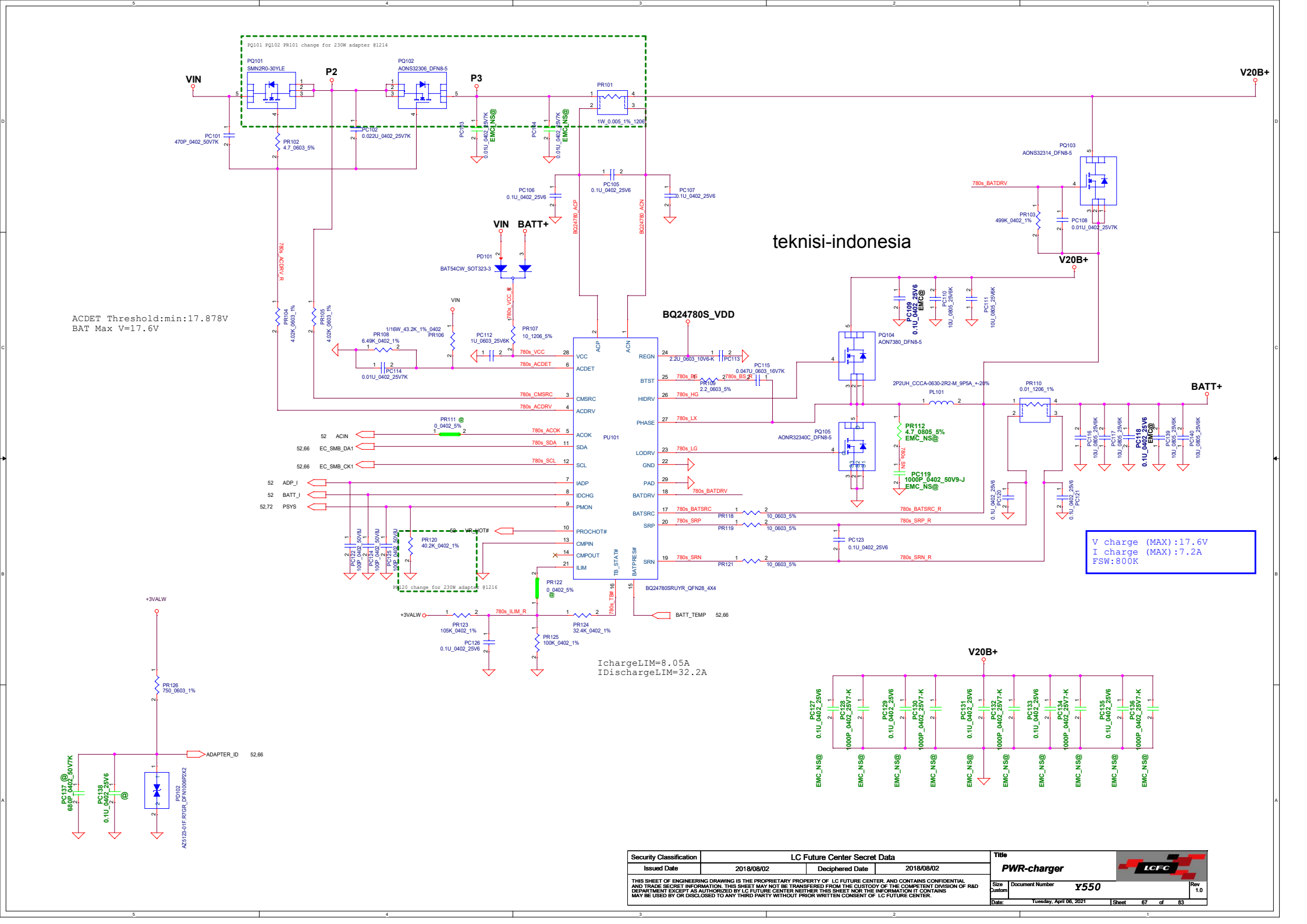






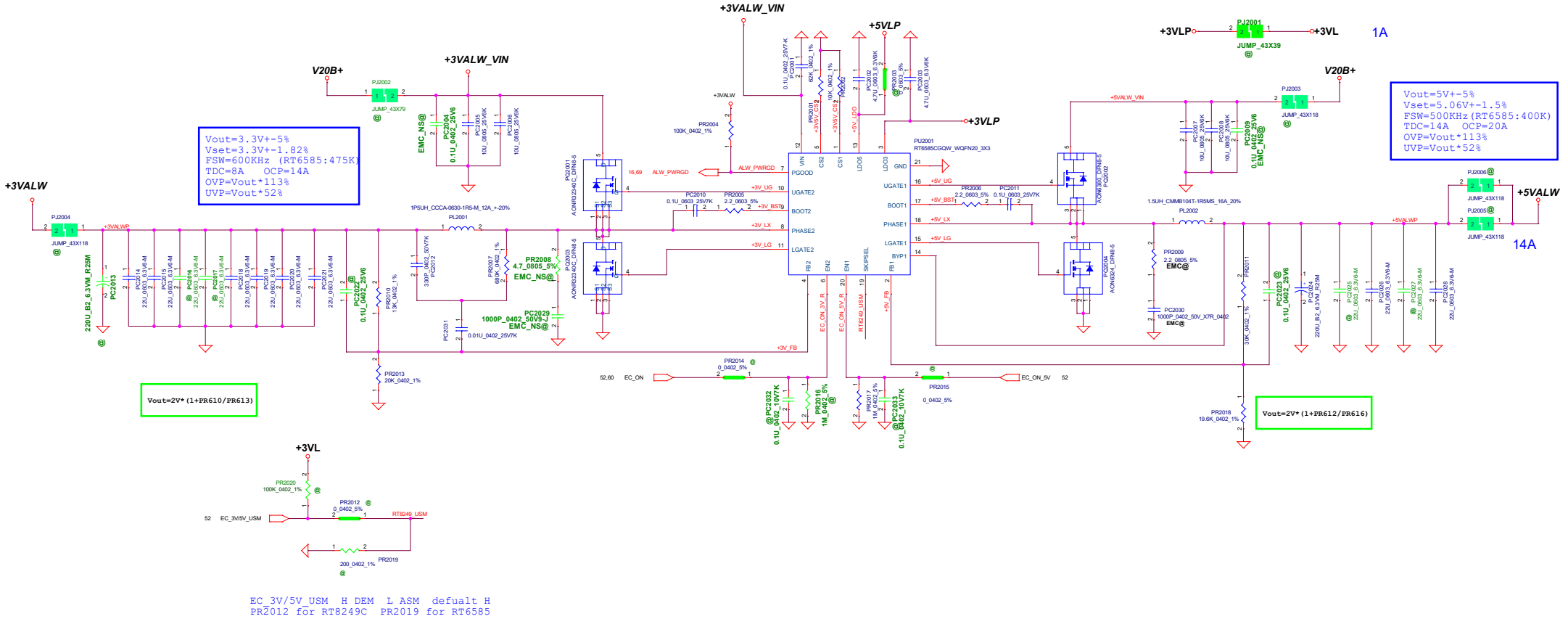
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-DCIN/BATT/RTC		
Size	Document Number	Rev	
C	Y550	1.0	
Date:	Tuesday, April 06, 2021	Sheet	66 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-charger		
Size	Custom	Document Number	Y550
Rev	1.0		
Date:	Tuesday, April 06, 2021	Sheet	67 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-3/5VALW		
Size: A3	Document Number: ¥550		Rev: 1.0
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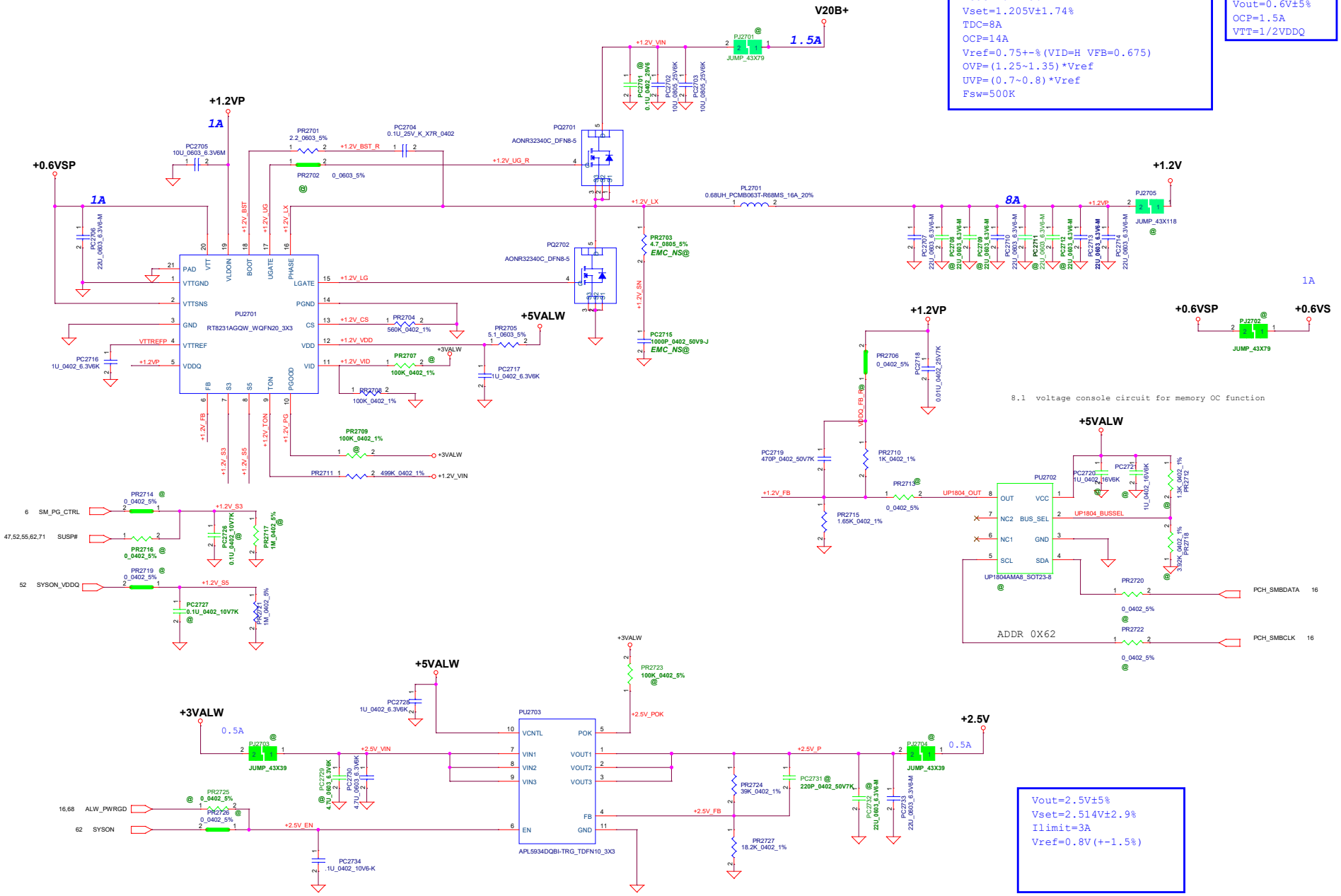
Vout=1.2V±5%
Vset=1.205V±1.74%
TDC=8A
OCP=14A
Vref=0.75+-%(VID=H VFB=0.675)
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=500K

Vout=0.6V±5%
OCP=1.5A
VTT=1/2VDDQ



8.1 voltage console circuit for memory OC function

Vout=2.5V±5%
Vset=2.514V±2.9%
Ilimit=3A
Vref=0.8V(+-1.5%)

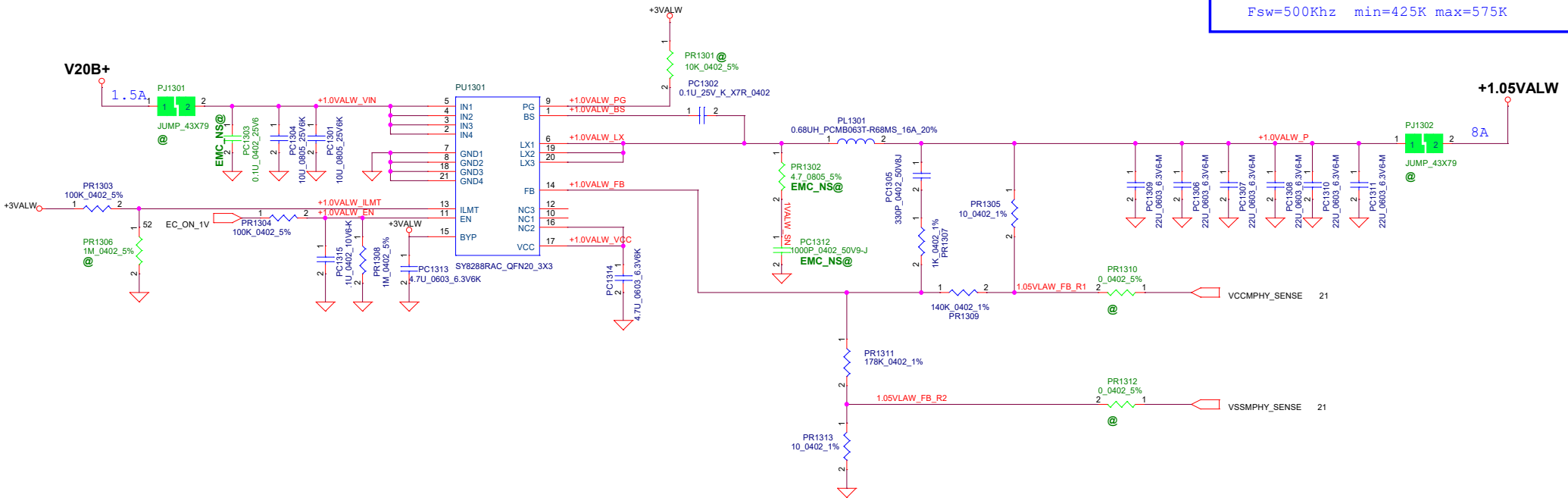
STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

Title: PWR-VDDQ/VTT
Size: Custom | Document Number: Y550 | Rev: 1.0
Date: Tuesday, April 06, 2021 | Sheet 69 of 83

Vout=1.05V±5%
Vset=1.072V±1.87%
Vref=0.6V(+-1%)
TDC=8A
OCP=16A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.0VALW**

Size	Document Number	Rev
Custom	Y550	1.0

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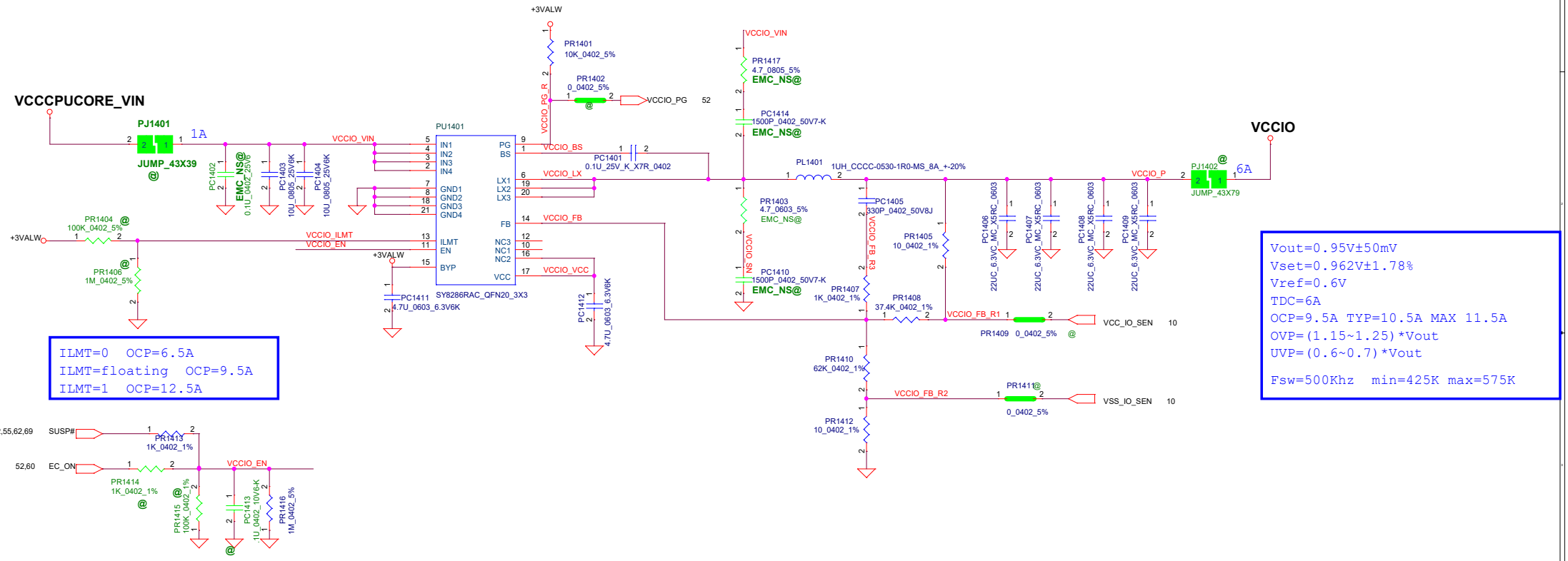

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-VCCIO**

Size	Document Number	Rev
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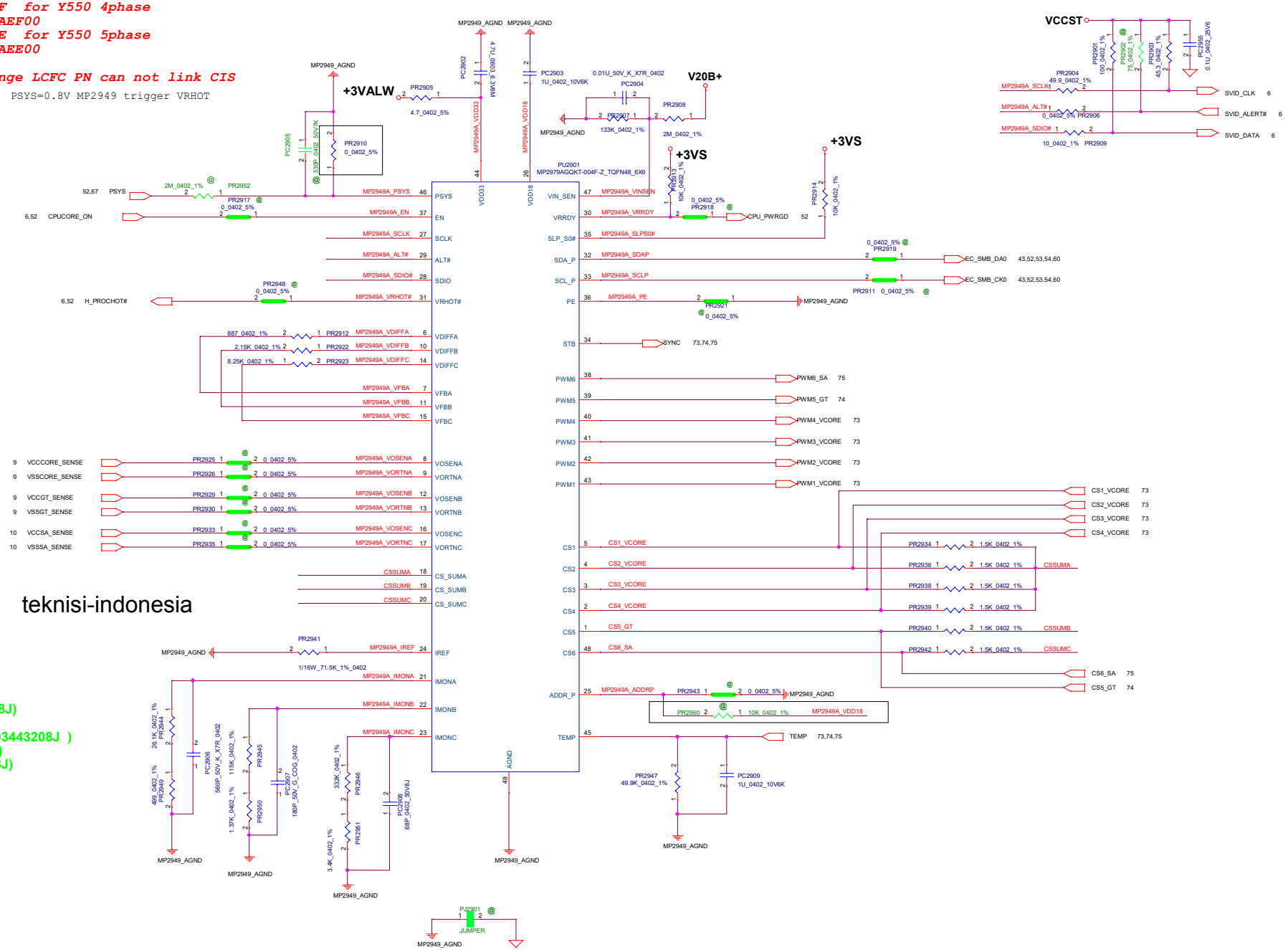
MP2979AGQKT-004F for Y550 4phase
LCFC PN: SA0000AEF00
MP2979AGQKT-004E for Y550 5phase
LCFC PN: SA0000AEE00

PU2901 only change LCFC PN can not link CIS

PSYS=0.8V MP2949 trigger VRHOT



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5Phase
PR2912=887ohm(SD00000XK8J)
PR2944+PR2949=22.567K
(22.1K SD03422128J+432 SD03443208J)
PC2907=180pF(SE000017A00)
PR2939=750ohm(SD03475008J)

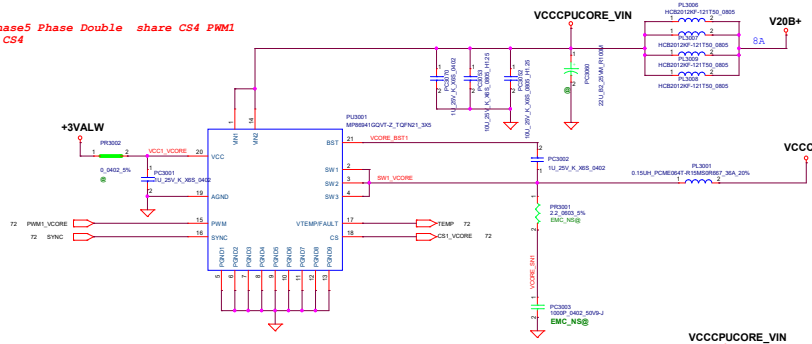
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

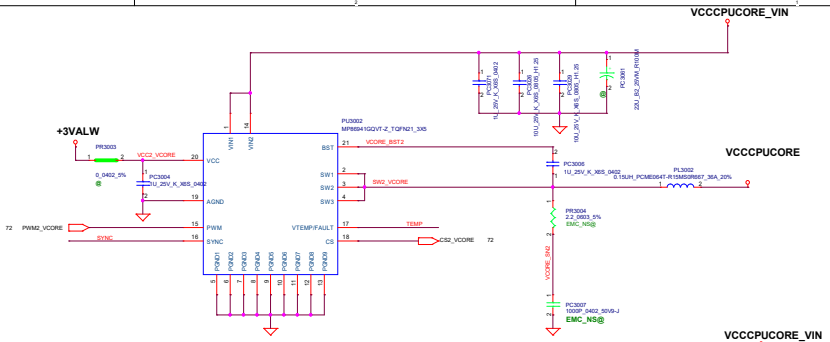
Title: PWR-IMVP8_MP2949

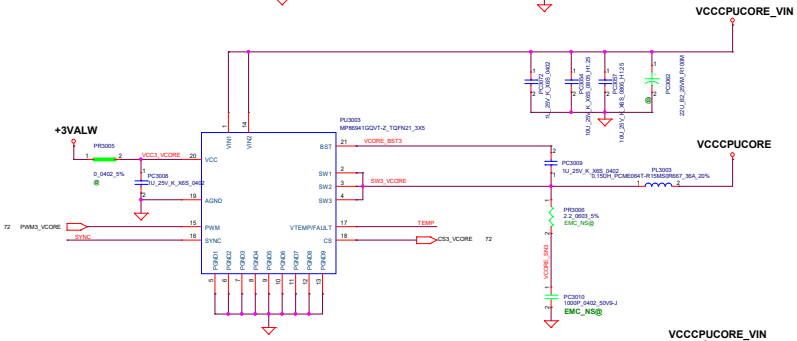
Size: Custom | Document Number: Y550 | Rev: 1.0

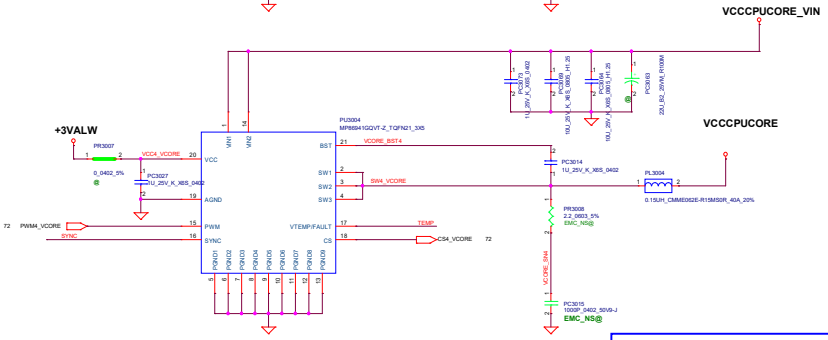
Date: Tuesday, April 06, 2021 | Sheet 72 of 83

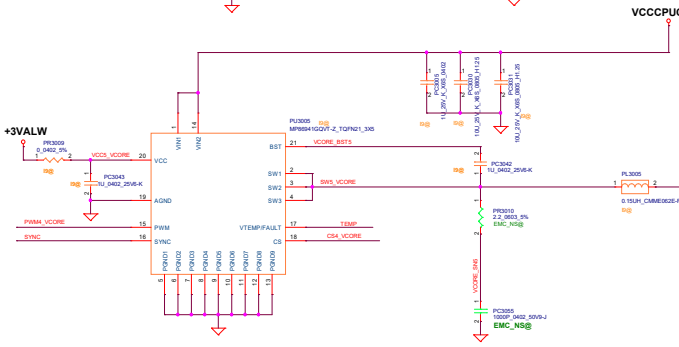
Phase4 Phase5 Phase Double share CS4 PWM1
CS share CS4





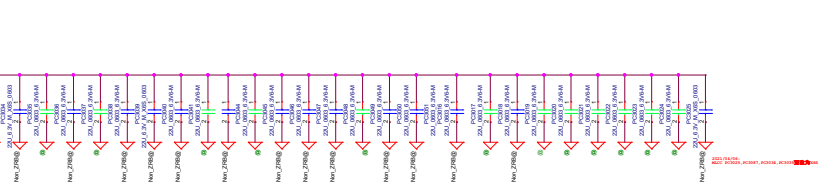


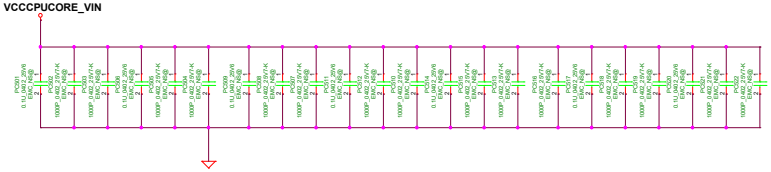


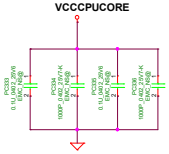


Y540:330u*2PCS+22u*19PCS
Y550:follow Y540 Vendor
PDG:470uF*4pcs+47uF*33pcs
Actual:330u*3PCS+22u*19PCS

Vboot=0V Loadline=1.1mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=±10mV(0.5A-TDC)
Ripple=±15mV(TDC-Iccmax)
TDC=125A Performance Line(5phase) Iccmax=165A
TDC=86A Base Line(4phase) Iccmax=140A
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz







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Issued Date	2018/08/02	Deciphered Date	2018/08/02

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Title: PWR-VCCCPUCORE
Size: Custom | Document Number: Y550 | Rev: 1.0
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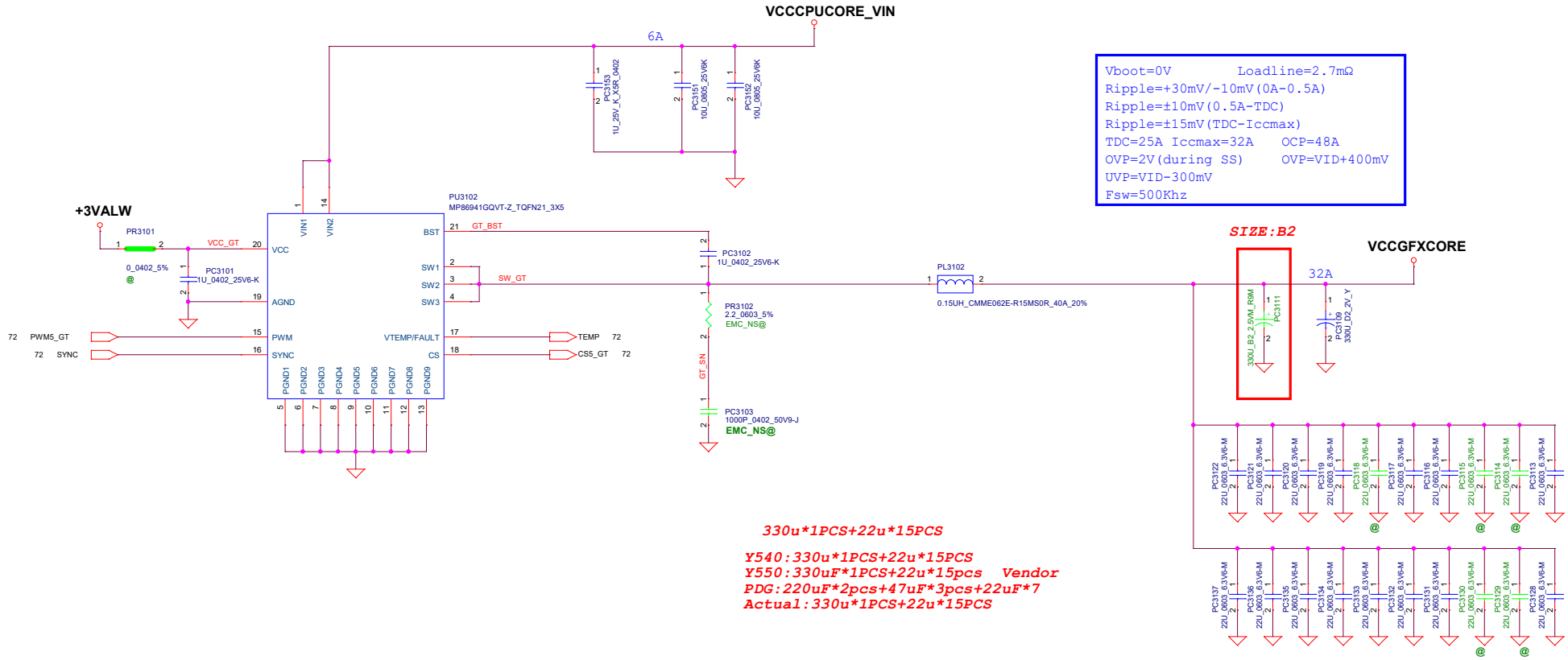

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-VCCGFXCORE

Size: Custom	Document Number: Y550	Rev: 1.0
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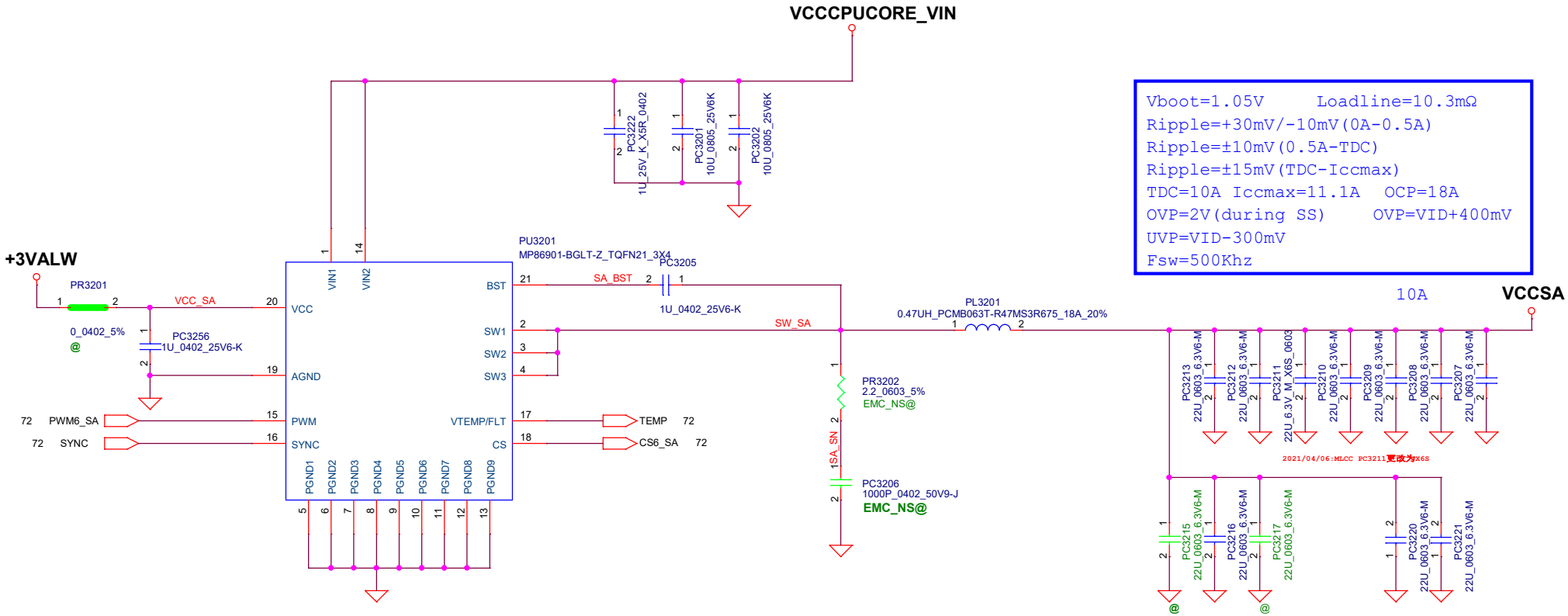
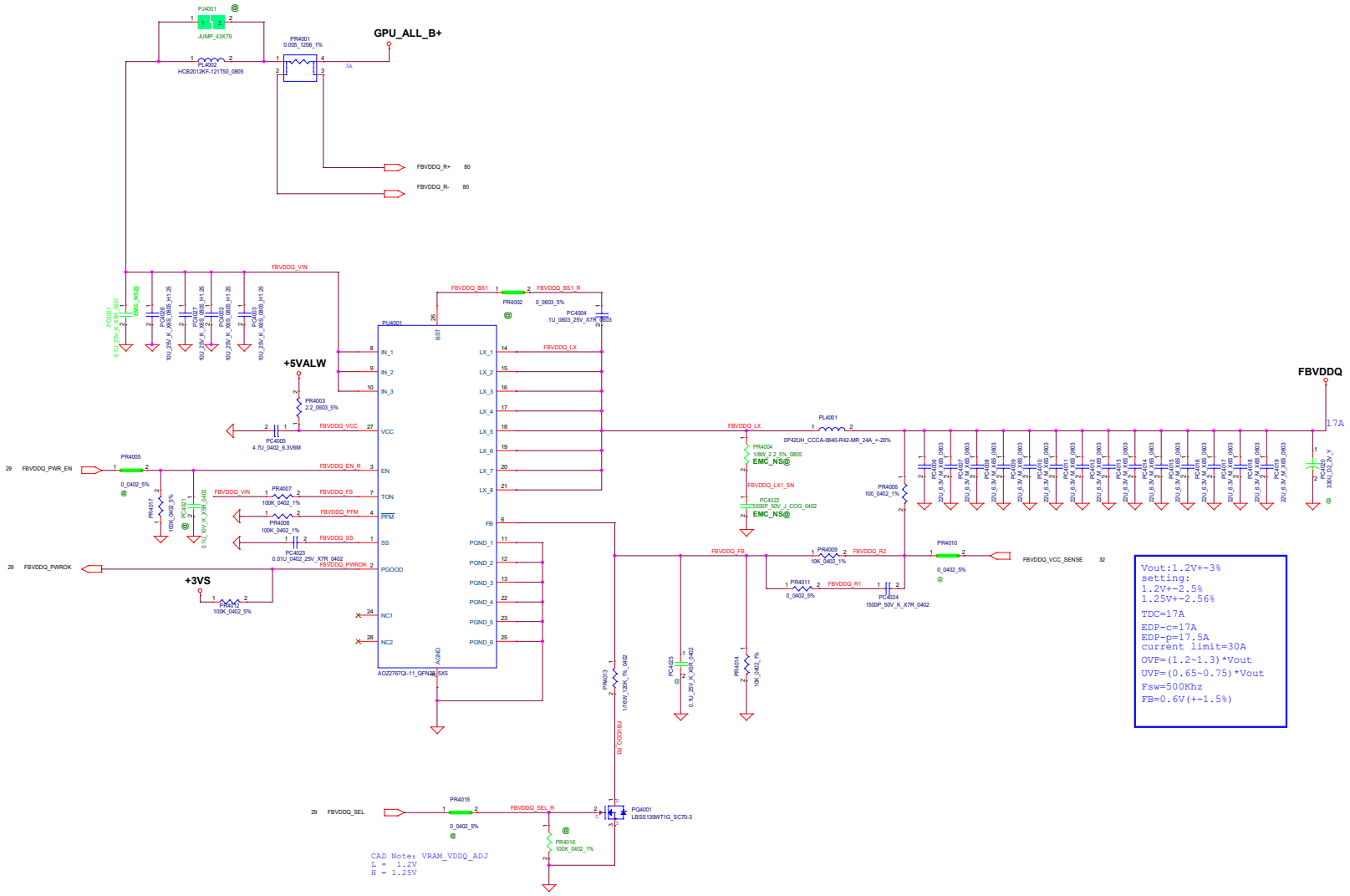


Y540:22u*10PCS
Y550:22u*10pcs Vendor
PDG:220uF*1pcs+47uF*4pcs+22uF*4
Actual:22u*10PCS

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-VCCSA		
Size B	Document Number Y550		Rev 1.0
Date: Tuesday, April 06, 2021	Sheet 75 of 83		



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-FBVDDQ		
Size	Document Number	Rev	
Custom	Y550	1.0	
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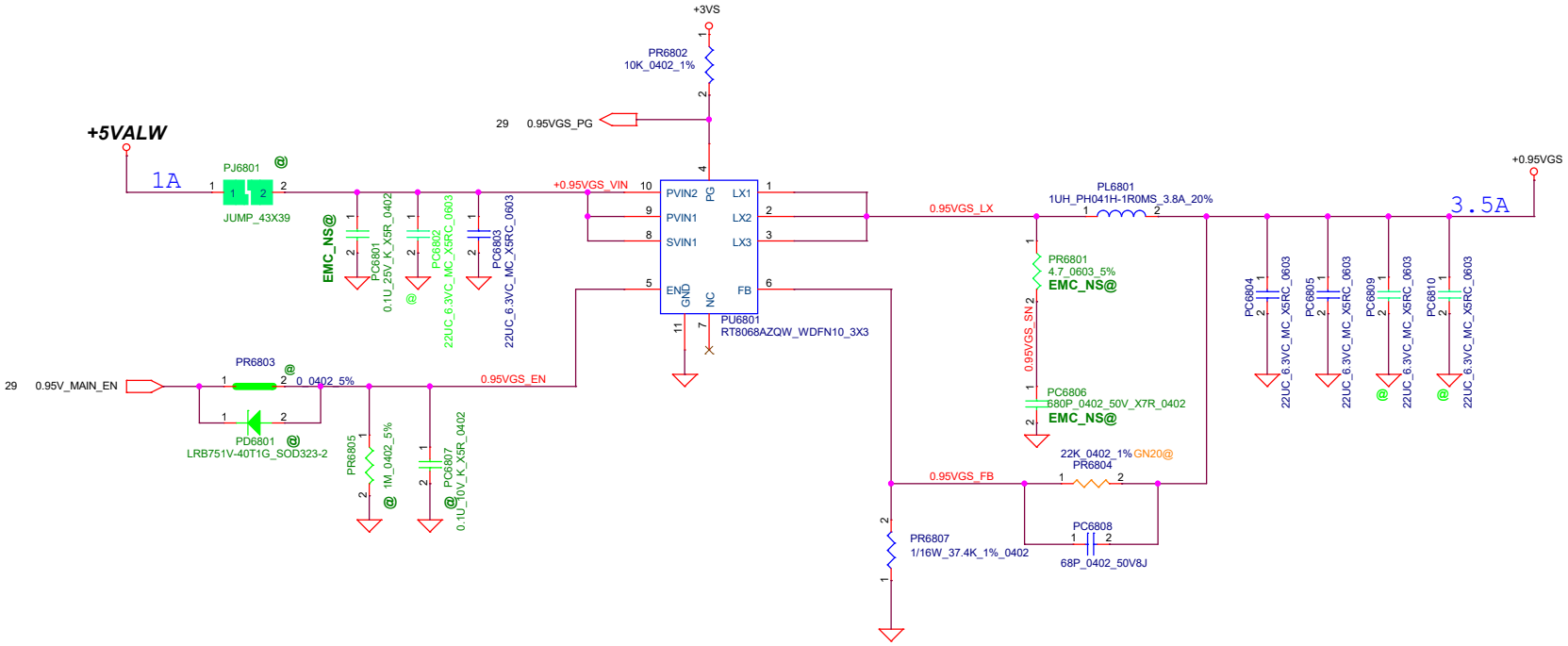


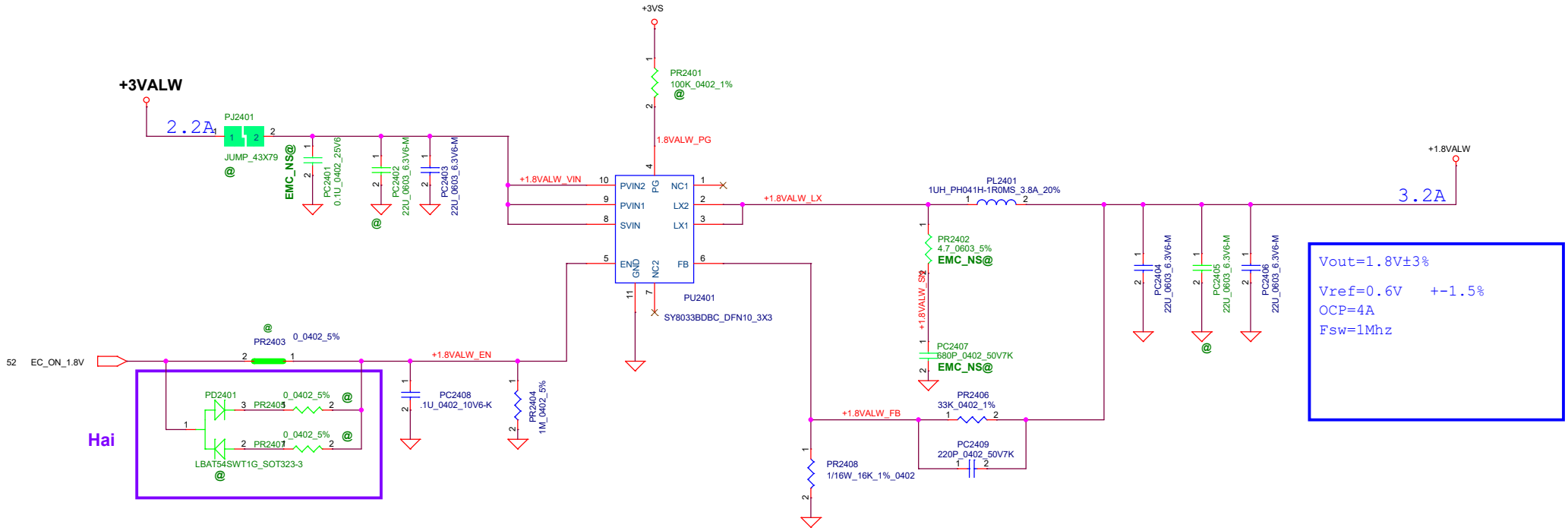
GN20 PR6804=22K
Vout=0.953V±3%
Vref=0.6V
OCP>4A
Fsw=1Mhz

N18P PR6804=26.1K
SD03426128J
Vout=0.953V±3%
Vref=0.6V
OCP>4A
Fsw=1Mhz

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-0.95VGS**

Size: Custom	Document Number: Y550	Rev: 1.0
Date: Tuesday, April 06, 2021	Sheet 77 of 83	



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: **PWR-1.8/1.0VGS**

Size	Document Number	Rev
Custom	Y550	1.0

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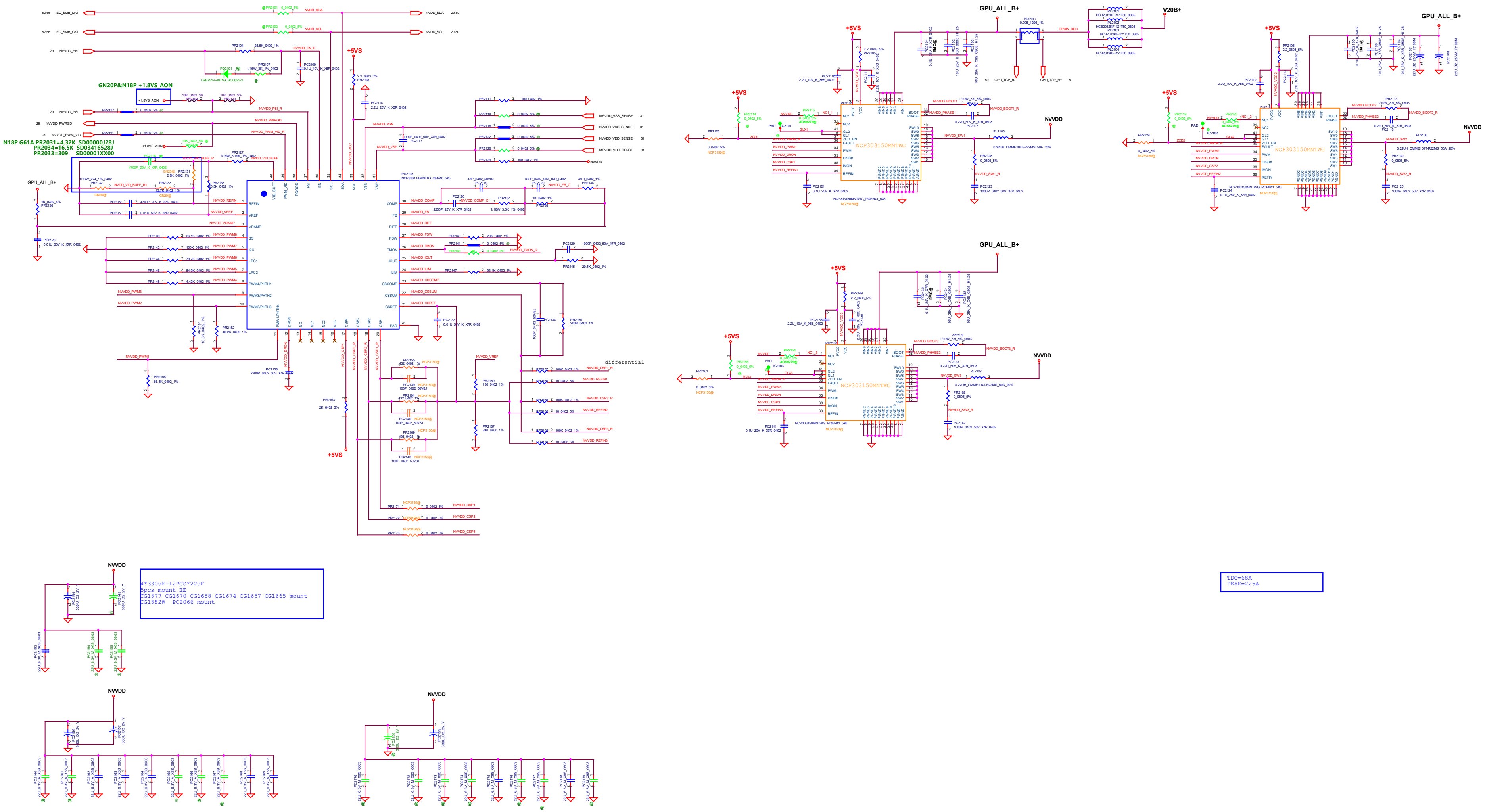
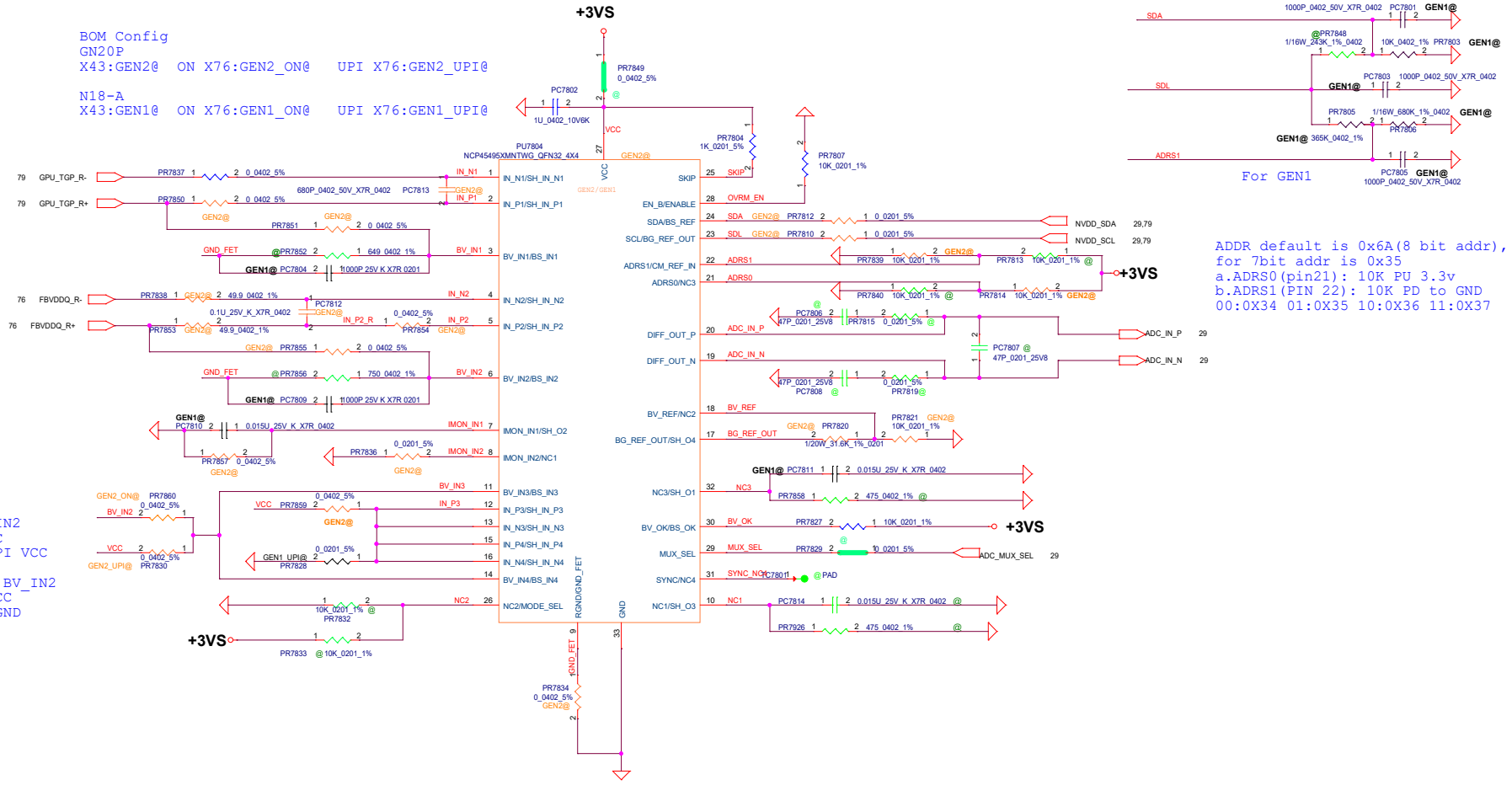


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: PWR-NVVDD

Document Number: Y550 Rev 1.0

Date: Tuesday, April 06, 2021



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	PWR-NVVDDS		
Size	Document Number	Rev	
C	Y550	1.0	
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Title

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Size	Document Number	Rev
C	***¥550***	1.0

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Title
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C	¥550	1.0

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Title
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C	¥550	1.0

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