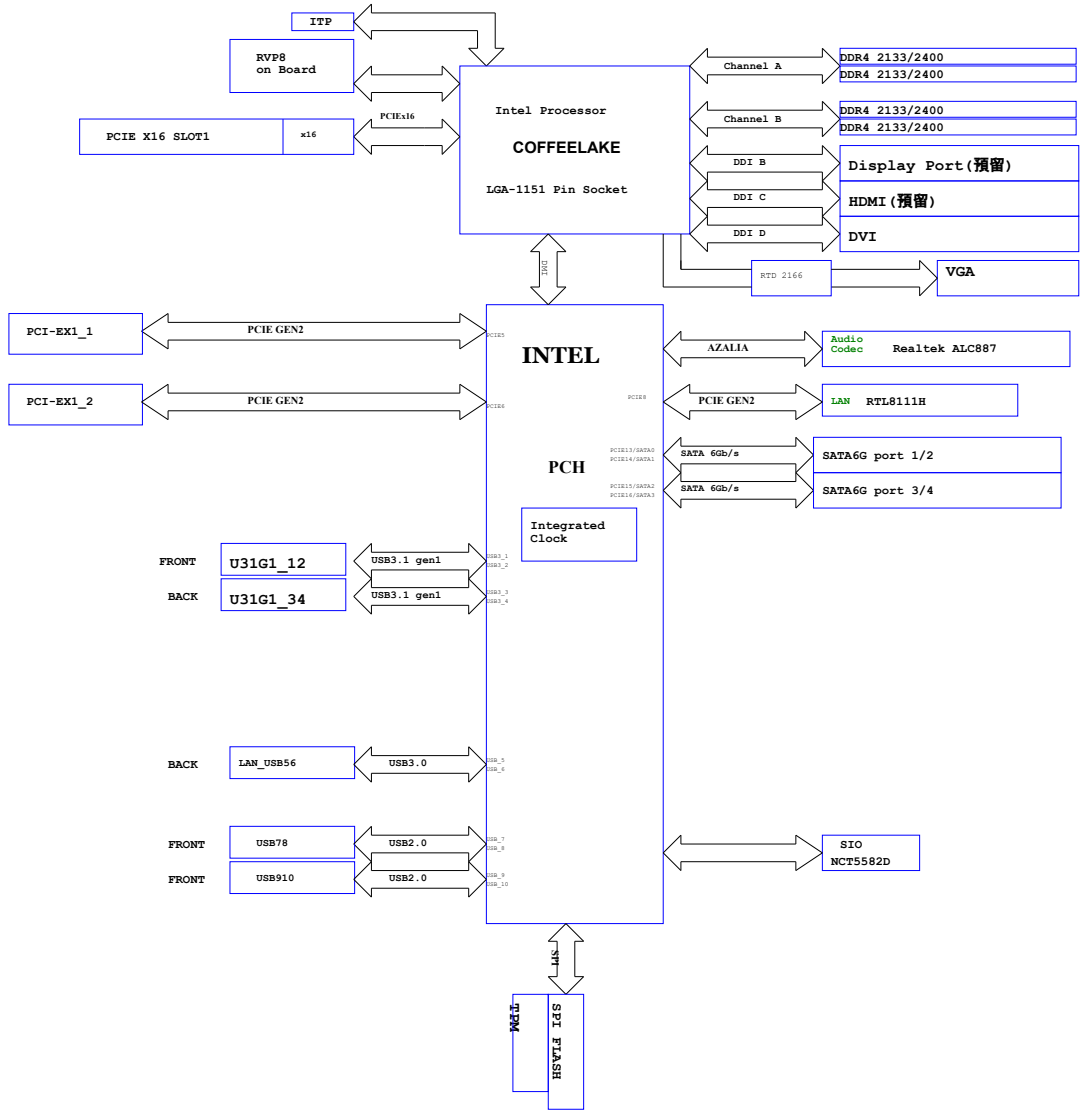
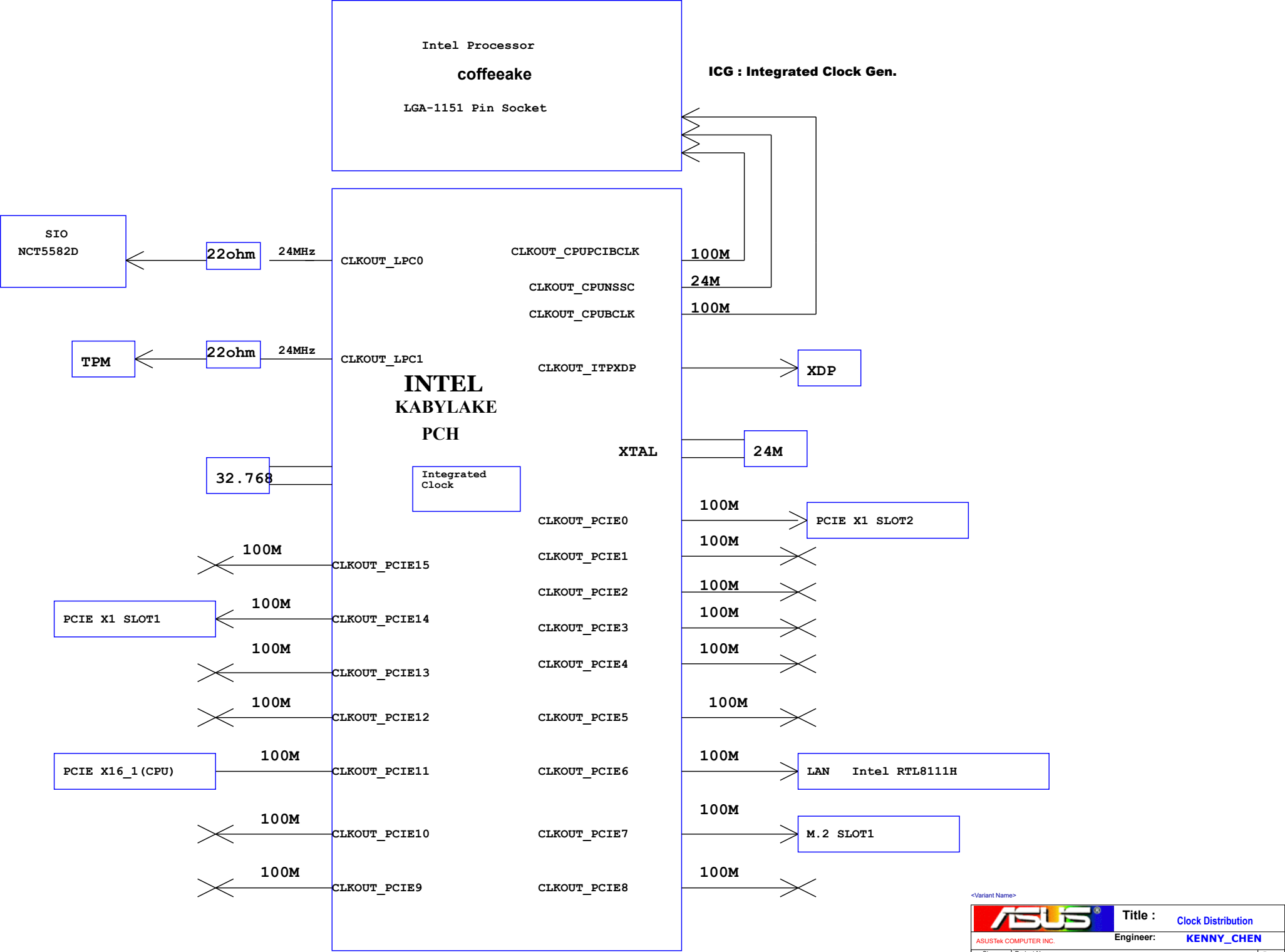
PRIME H310M-K R2.0

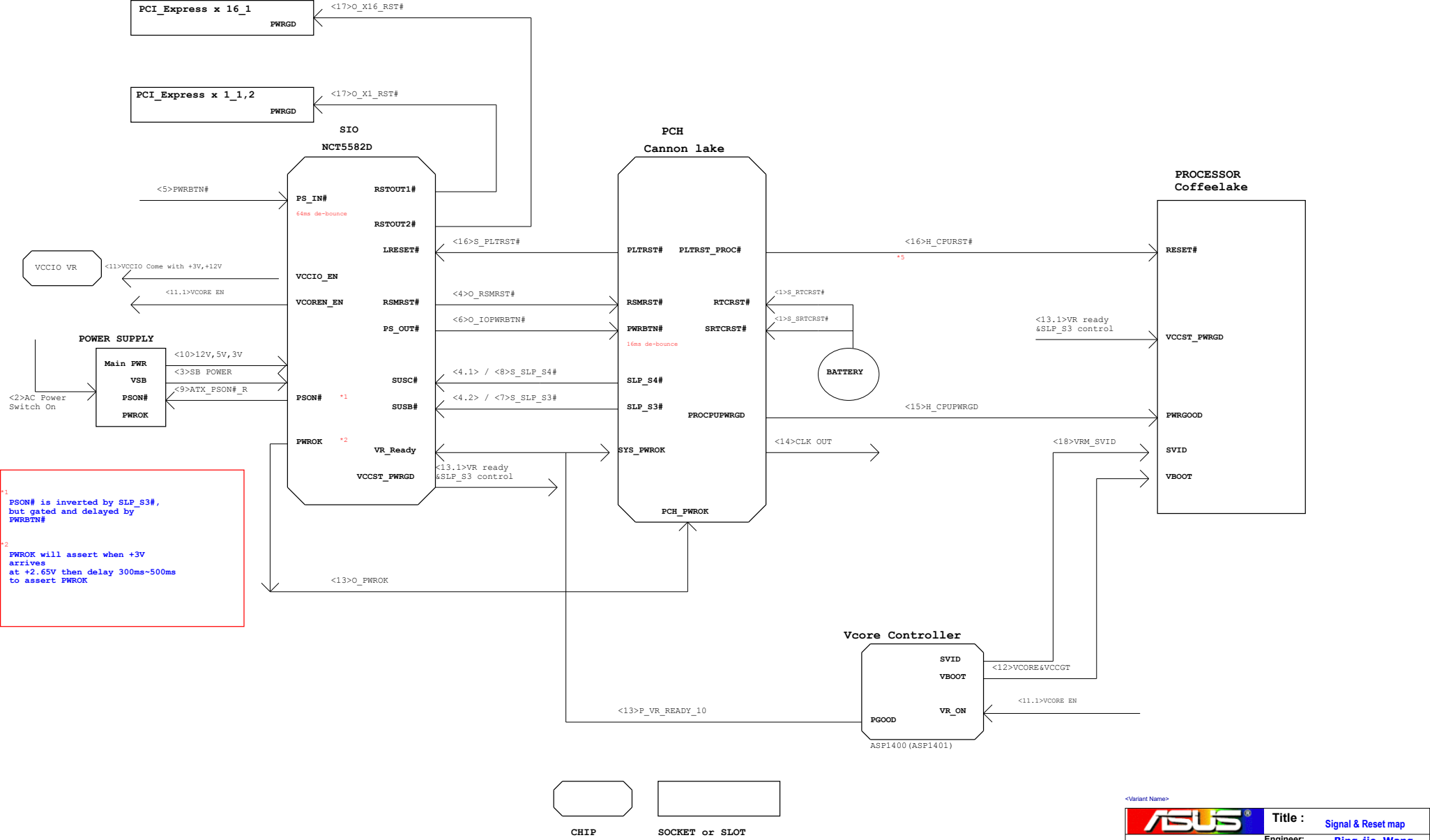
Rev 1.01A 2018.06





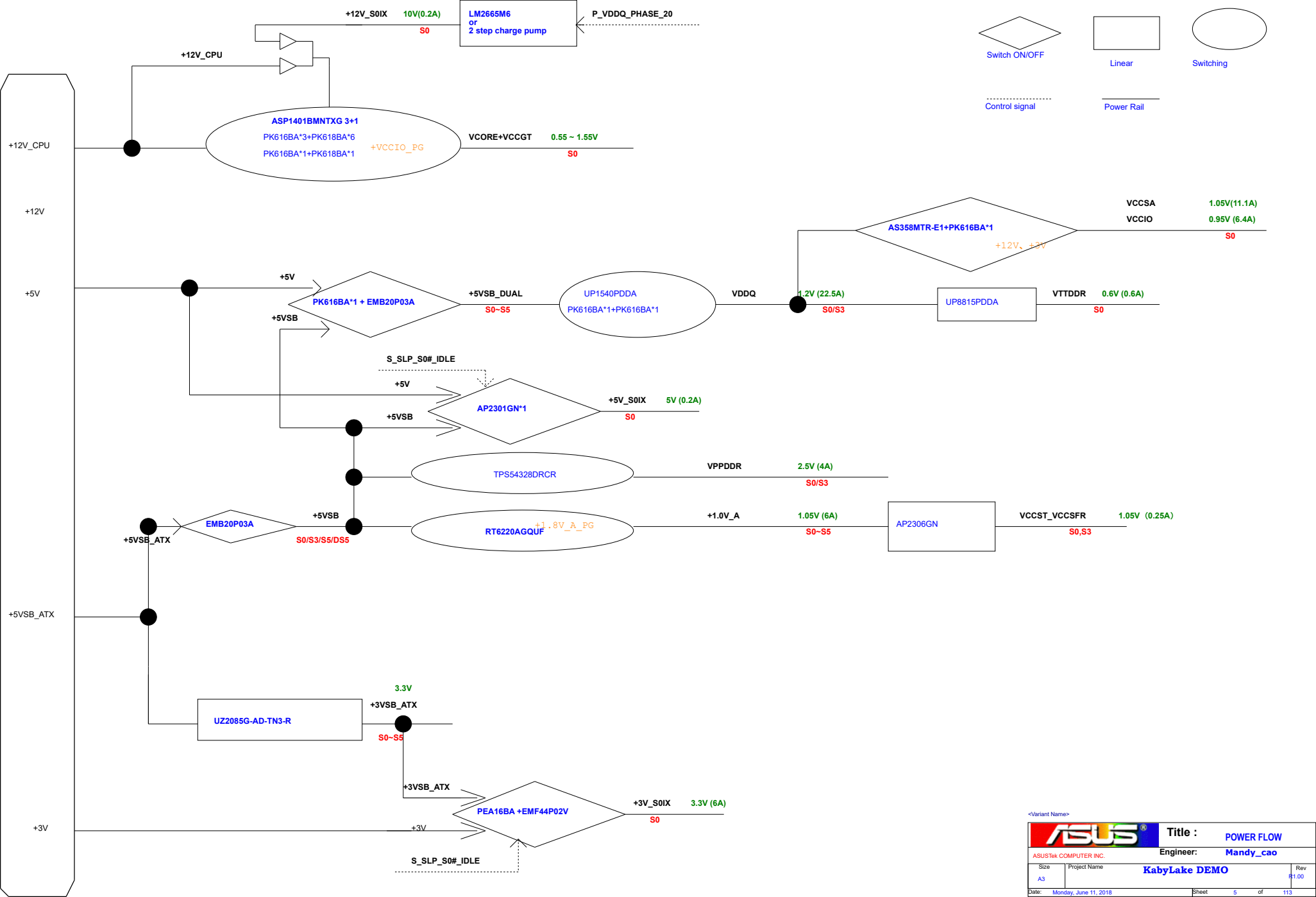
<Variant Name>

ASUSTek COMPUTER INC.	Title : Clock Distribution	
	Engineer: KENNY_CHEN	
Size: A3	Project Name: SKYLAKE CHIPSET DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 2 of 113	



<Variant Name>

ASUSTek COMPUTER INC.	Title : Signal & Reset map	
	Engineer: Bing-jie_Wang	
Size: A3	Project Name: SKYLAKE CHIPSET DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 3 of 113	



<Variant Name>

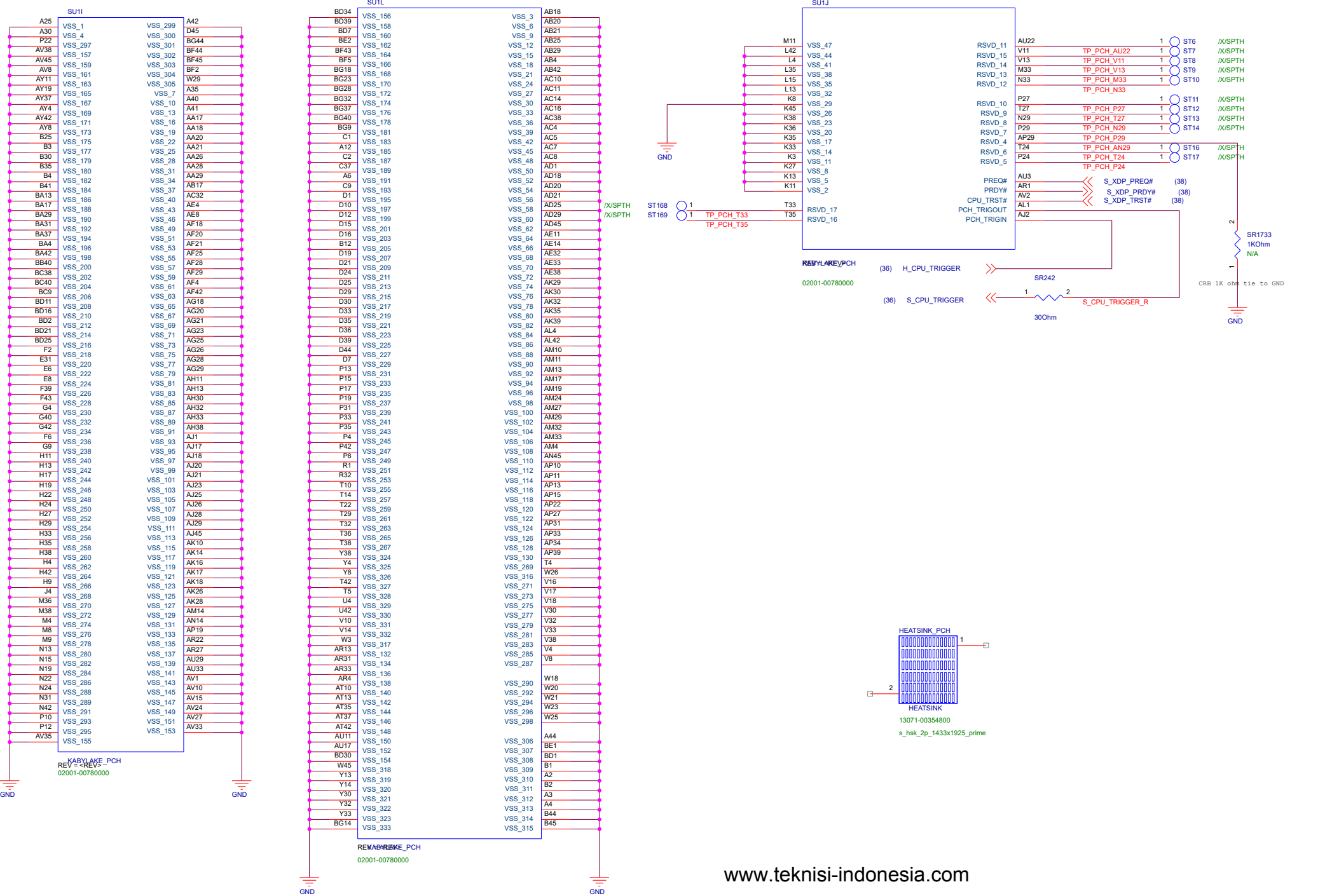
ASUSTek COMPUTER INC.

Title : POWER FLOW

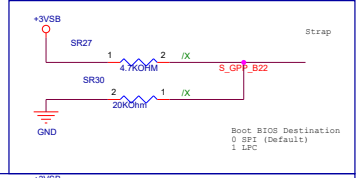
Engineer: Mandy_cao

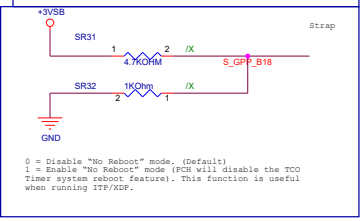
Size	Project Name	Rev
A3	KabyLake DEMO	R1.00

Date: Monday, June 11, 2018 Sheet 5 of 113

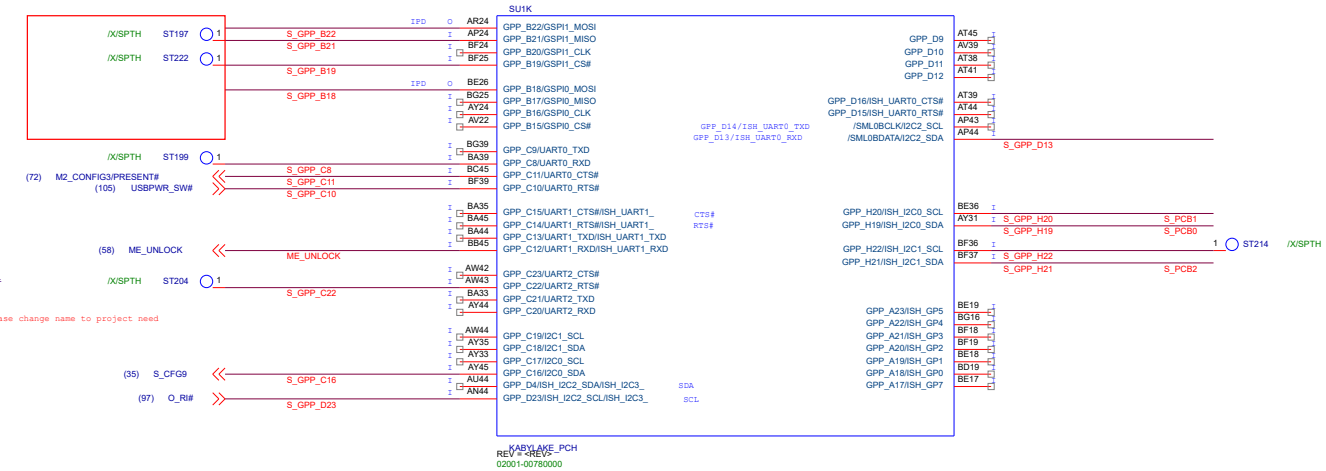


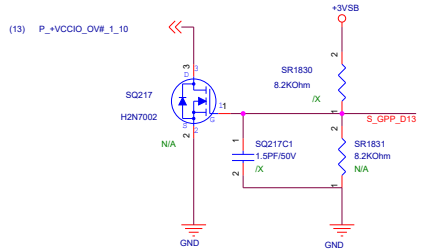
ASUSTek Computer Inc.	Title :	LYNX (GND)	
	Engineer:	IAN	
Size: A3	Project Name: Z87-PRO		Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 61 of 113		

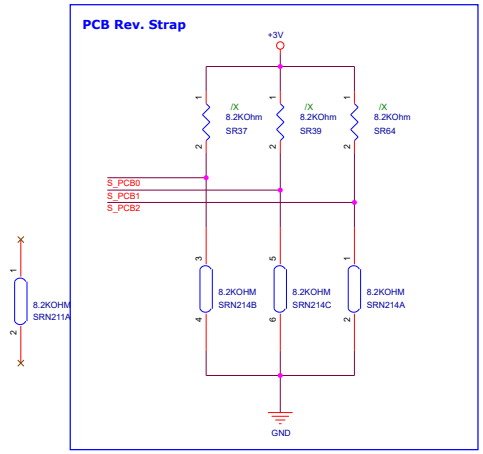




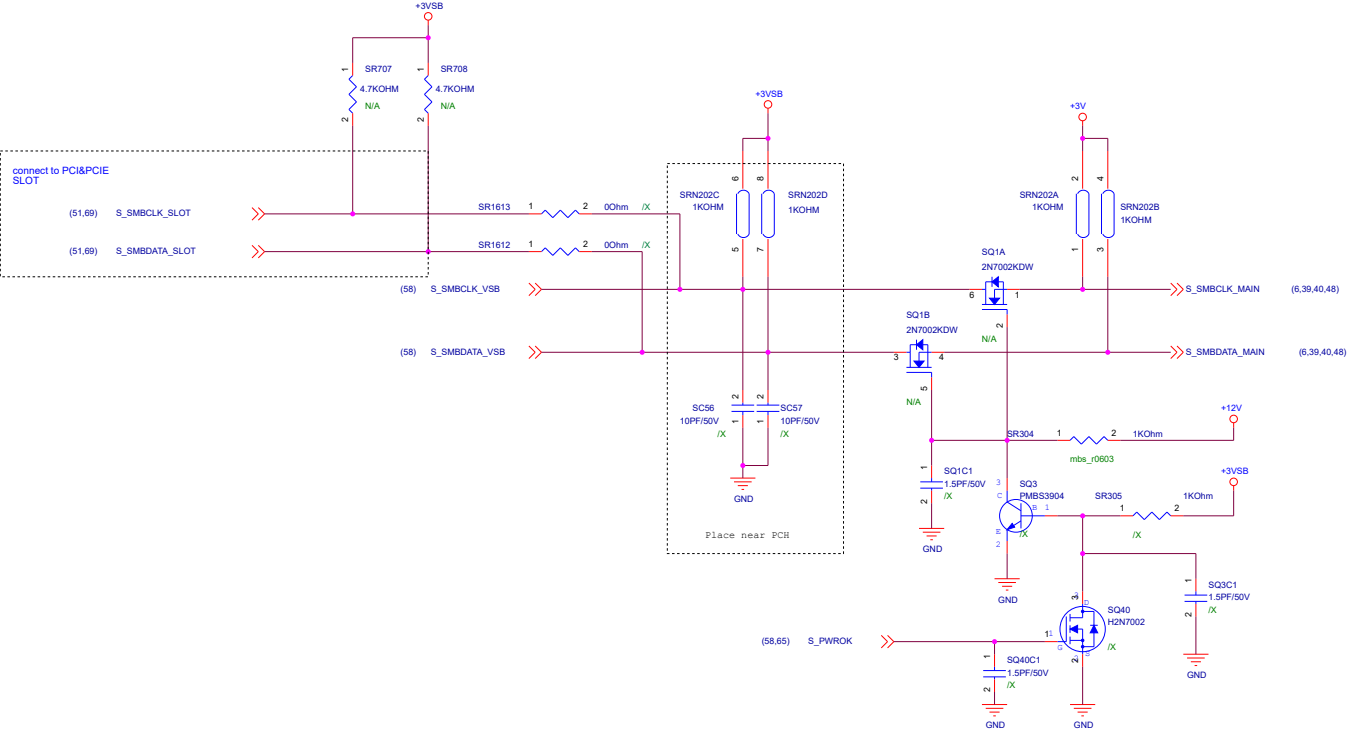
GPI PU





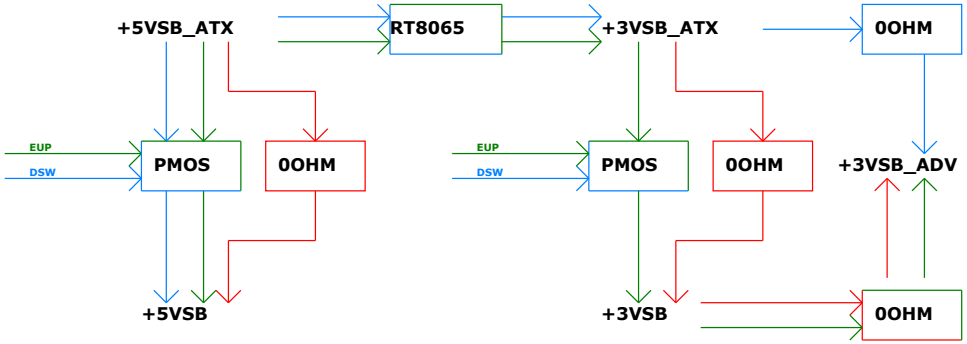


ASUSTek Computer Inc.	Title :	SPTH (GPIO)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 62 of 113		



ASUSTek Computer Inc.	Title : SPTH (SMBUS/CLRTC)		
	Engineer: Morse_Peng		
Size A3	Project Name SkyLake VC		Rev R1.00
Date: Monday, June 11, 2018	Sheet 63 of 113		

POWER FLOW



PS:the common part design by power team,no-eup part and eup part in SIO demo circuit

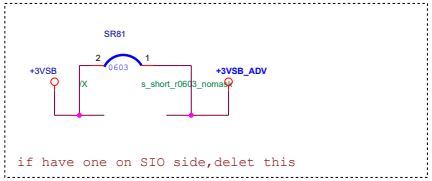
No-EUP Part

EUP Part

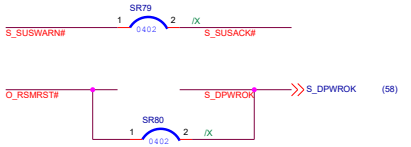
DSW Part

NOT SUPPORT DSW

Power plane



Control link

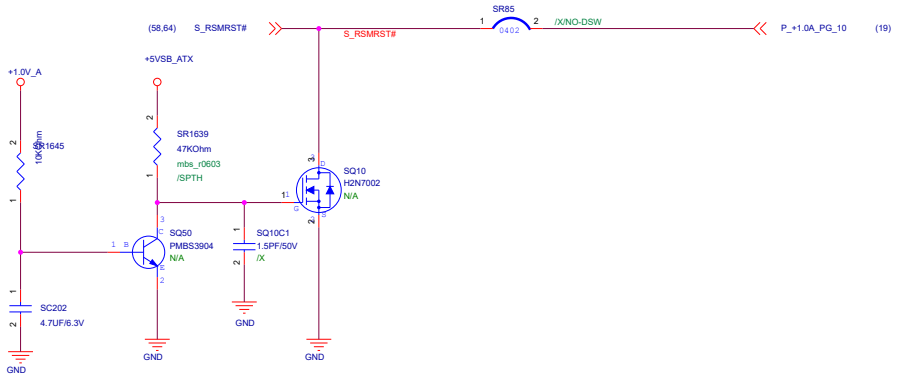


if NO DSW , please use shortpin

SUPPORT DSW

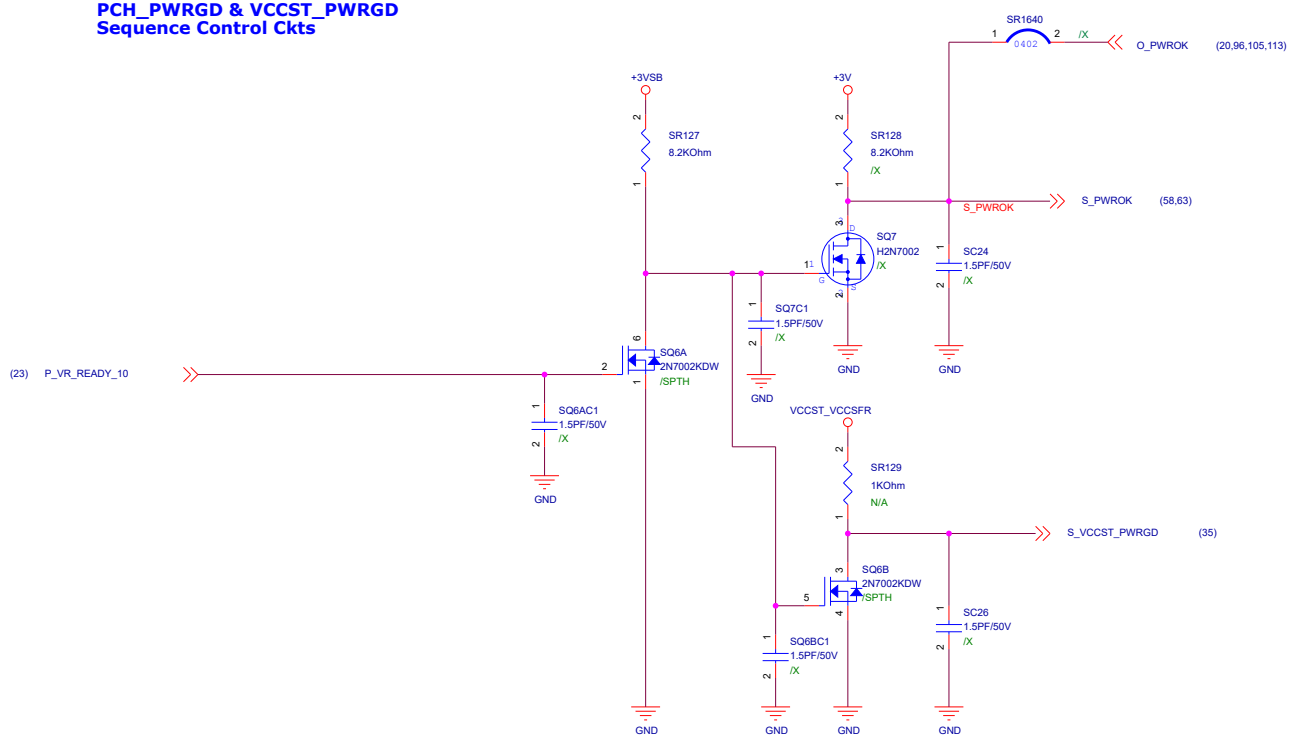
Power plane

Control link

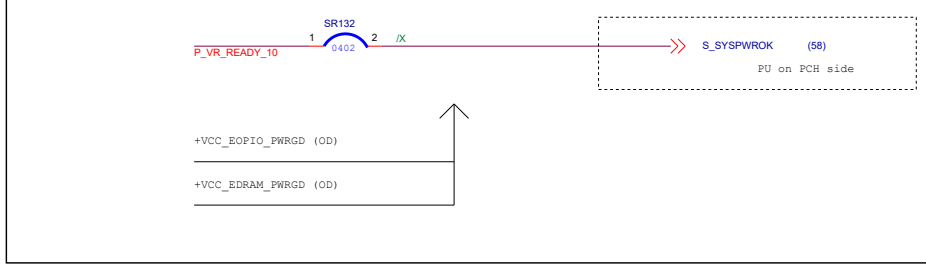


ASUSTek Computer Inc.	Title : SPTH (DSW SEQUENCE)		
	Engineer: IAN		
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 64 of 113		

PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



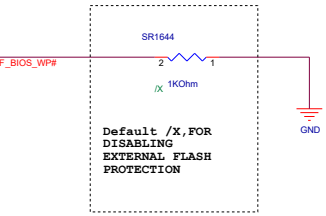
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.
2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation
3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor
4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

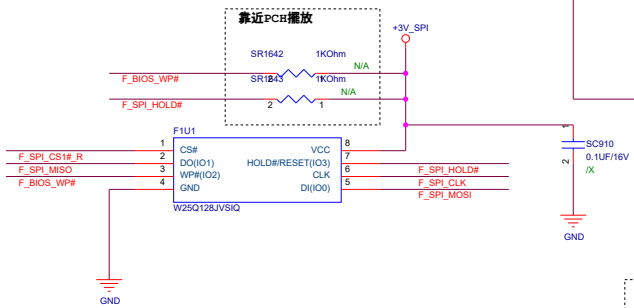
ASUSTek Computer Inc.	Title : SRTH (PCH/SYS/PROC_PWROK)	
	Engineer: IAN	
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 65 of 113	

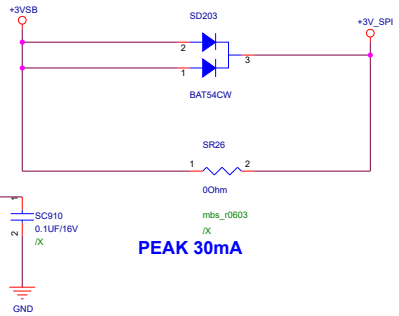
Standard Circuit	
BIOS	SPI
REV.	F1_0.3G_Beta

SPI /X/SPI

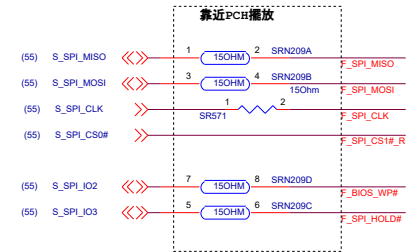
SMD BIOS

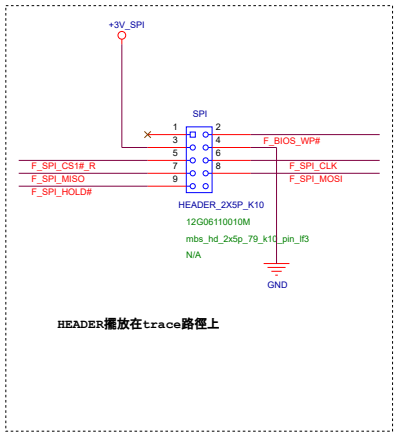




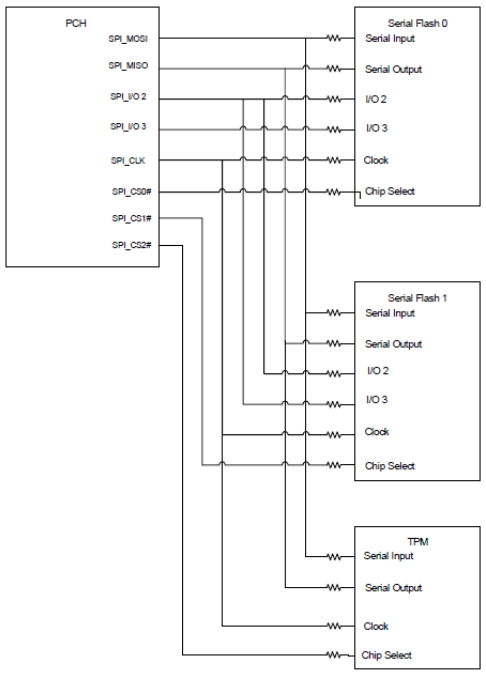


PEAK 30mA





HEADER擺放在trace路徑上

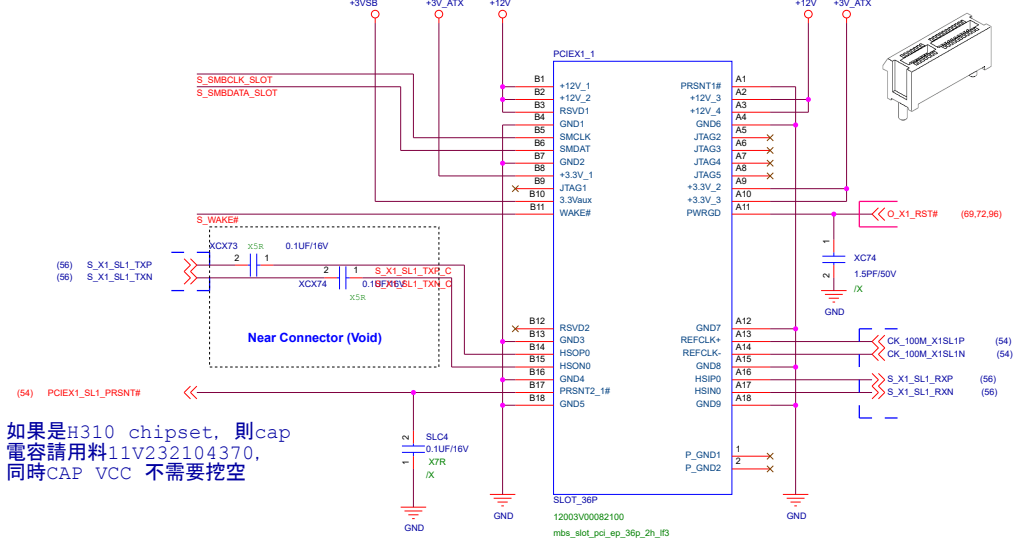


ASUSTek COMPUTER INC.

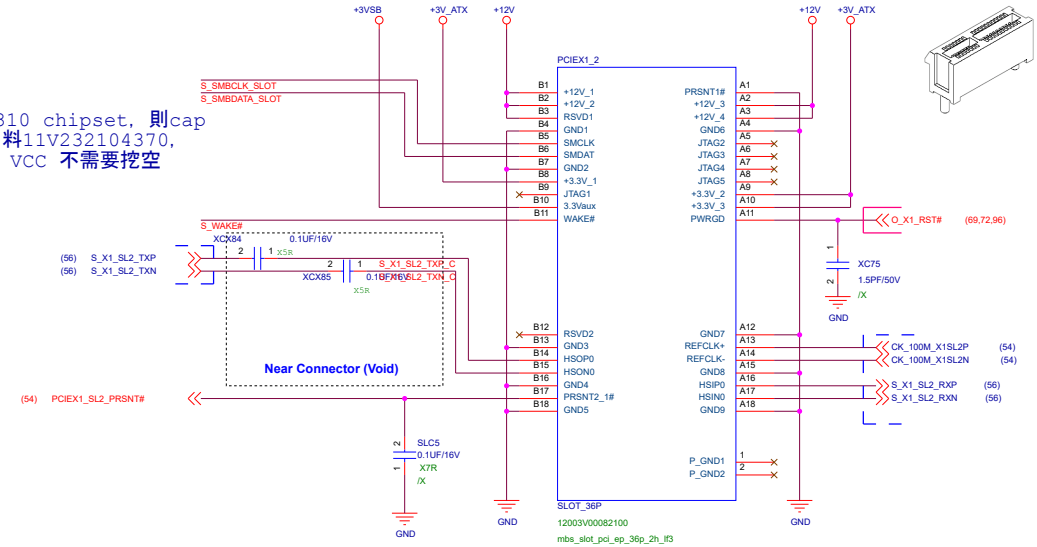
Engineer: IAN

Size	Project Name	Rev
A3	Z87-PRO	R1.02A

Date: Monday, June 11, 2018 Sheet 67 of 113

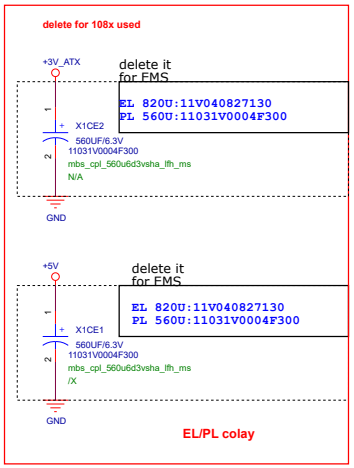


如果是H310 chipset, 則cap
電容請用料11V232104370,
同時CAP VCC 不需要挖空



如果是H310 chipset, 則cap
電容請用料11V232104370,
同時CAP VCC 不需要挖空

delete for 108x used



EL/PL colay

to SB SMBus(standby power)

(51,63) S_SMBCLK_SLOT
(51,63) S_SMBDATA_SLOT

(51,58,72,89) S_WAKE#

Pull-high at SB side

<Variant Name>

ASUSTek COMPUTER INC.

Title : PCIEX1_1

Engineer: KENNY_CHEN

Size	Project Name	Rev
A3	Z87-PRO	P1.02A

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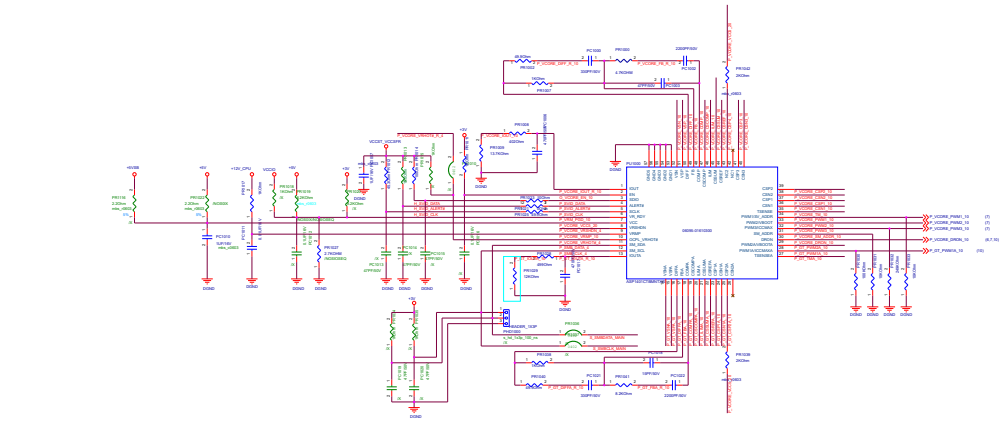

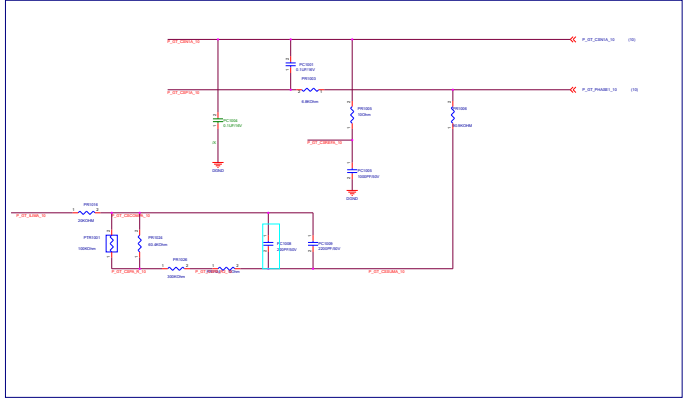

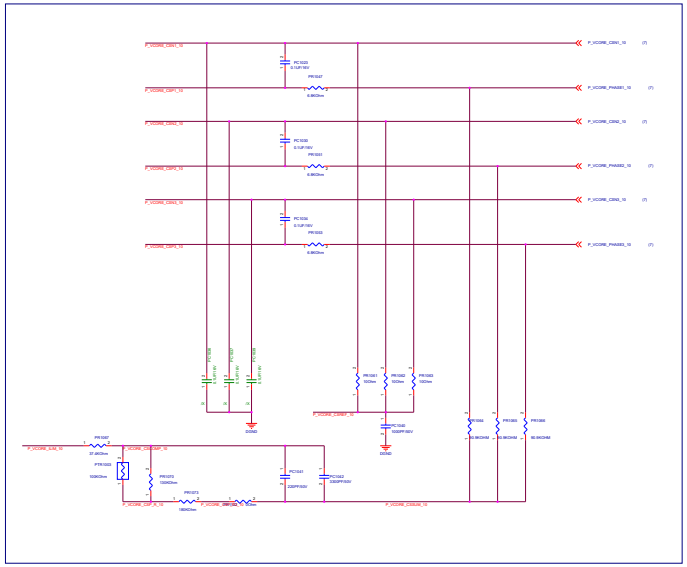

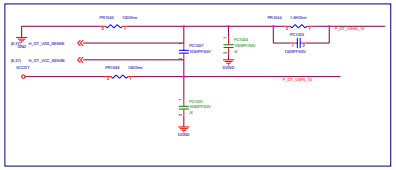

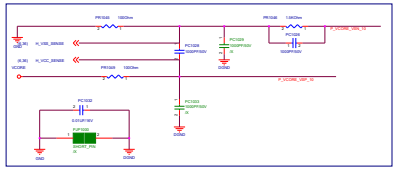

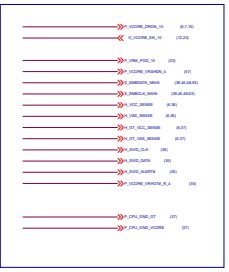

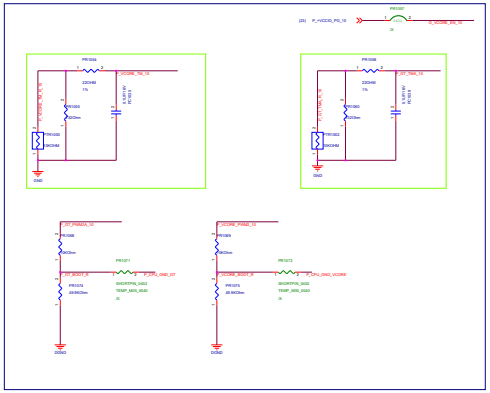

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Size	Document Number		Rev
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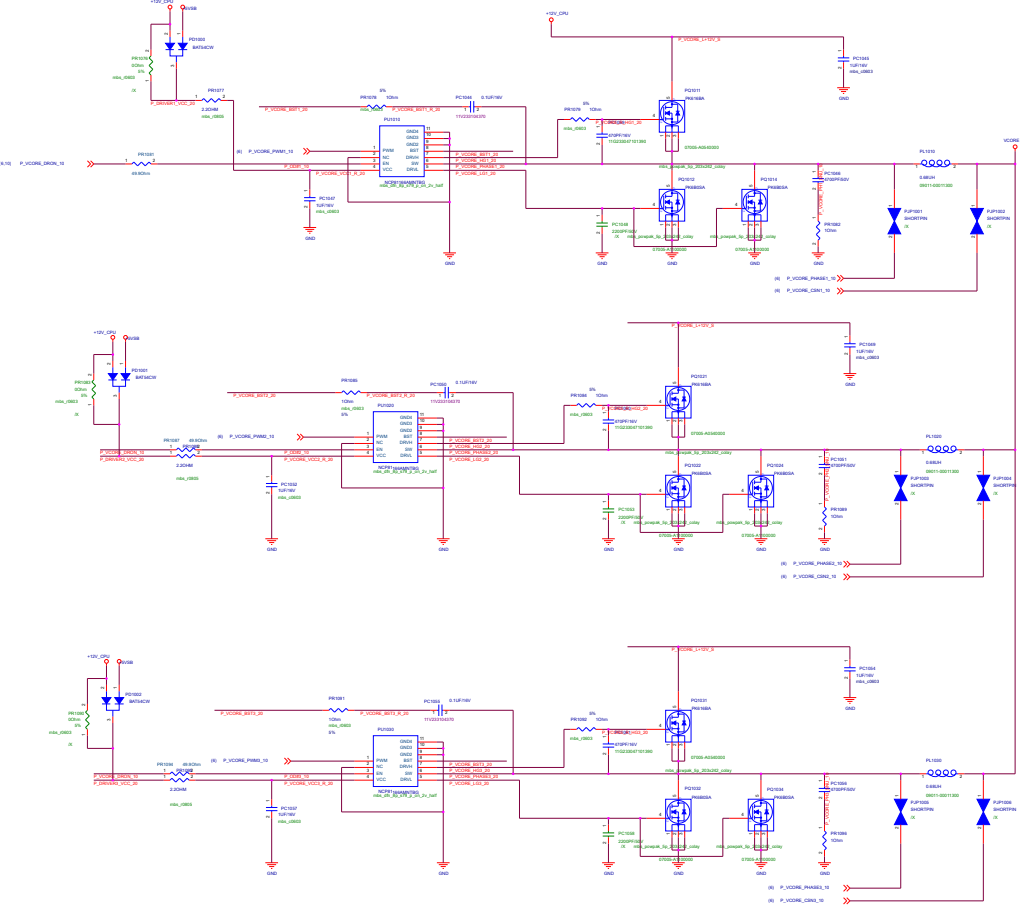
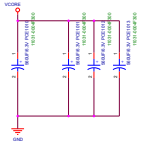
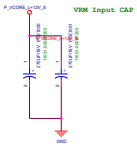
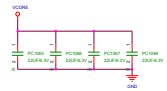
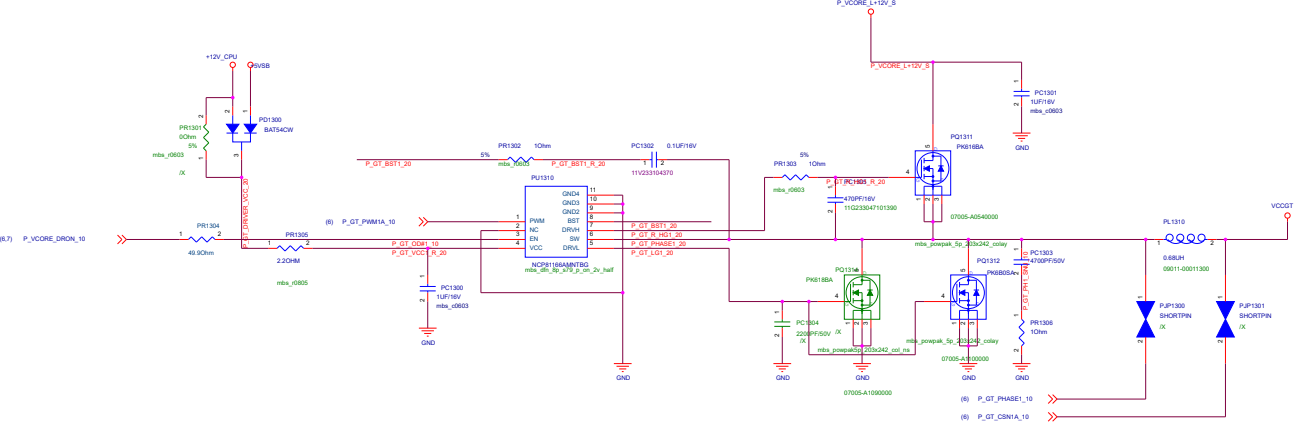
Date: Monday, June 11, 2018	Sheet 6 of 113		

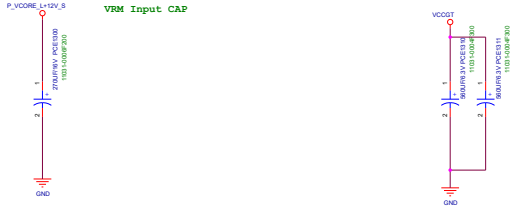





VRM Input CAP







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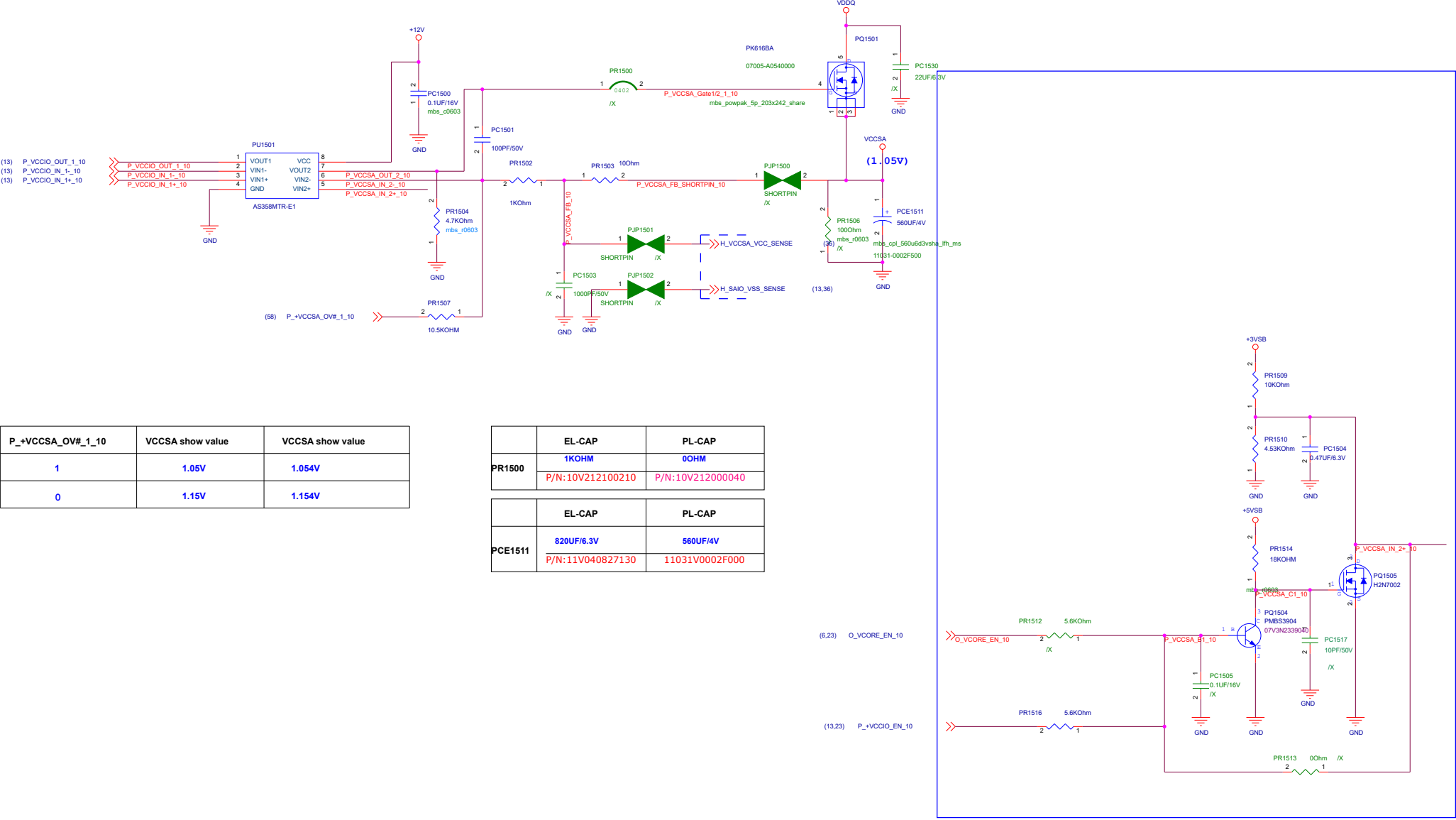
ASUSTek COMPUTER INC.	Title :	VCCGT DRIVER	
	Engineer:	RAY	
Size: A2	Project Name:	SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet: 10	of: 113	



P_+VCCSA_OV#_1_10	VCCSA show value	VCCSA show value
1	1.05V	1.054V
0	1.15V	1.154V

	EL-CAP	PL-CAP
PR1500	1KOHM	0OHM
	P/N:10V212100210	P/N:10V212000040

	EL-CAP	PL-CAP
PCE1511	820UF/6.3V	560UF/4V
	P/N:11V040827130	11031V0002F000

<Variant Name>

ASUSTek COMPUTER INC.

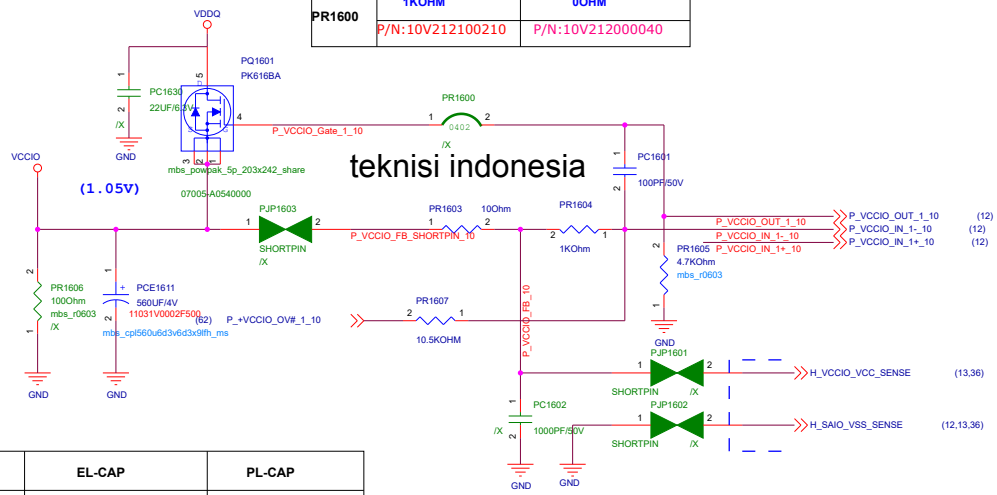
Title : VCCSA

Engineer: Mandy_cao

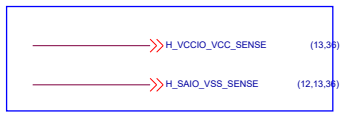
Size	Project Name	Rev
A3	KabyLake DEMO	R1.00

Date: Monday, June 11, 2018 Sheet 12 of 113

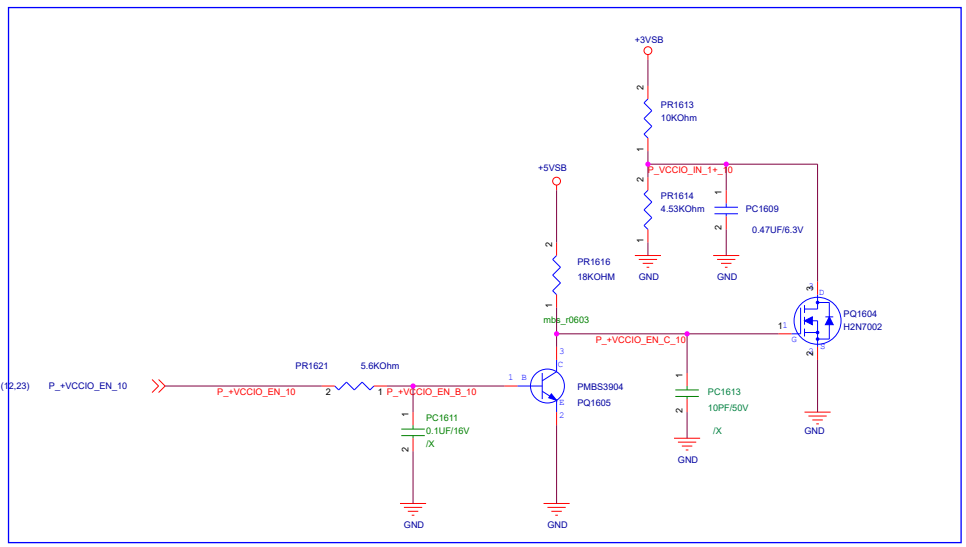
	EL-CAP	PL-CAP
PR1600	1KOHM	0OHM
	P/N:10V212100210	P/N:10V212000040



	EL-CAP	PL-CAP
PCE1611	820UF/6.3V	560UF/4V
	P/N:11V040827130	11031V0002F000



P_+VCCIO_OV#_1_10	VCCIO show value	VCCIO design value
1	1.05V	1.054V
0	1.15V	1.154V



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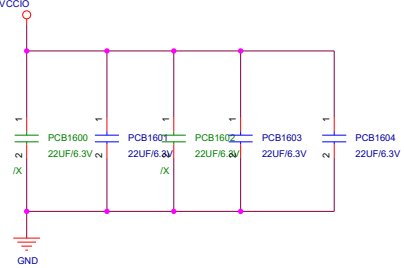
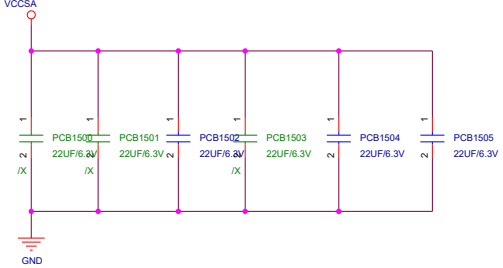
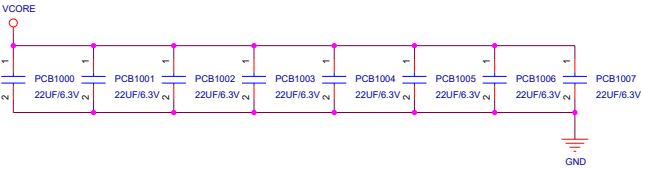
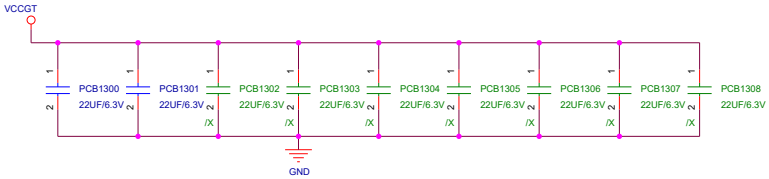
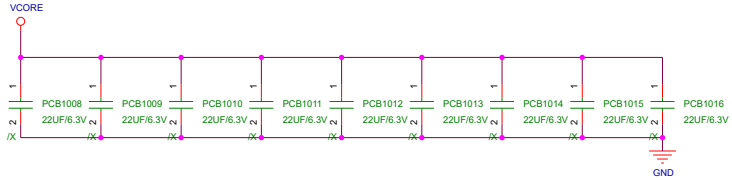
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Monday, June 11, 2018		Sheet 13 of 113	

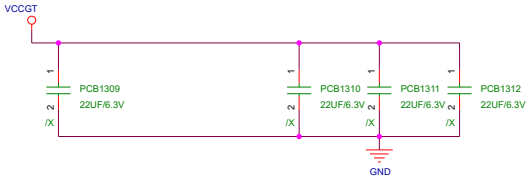






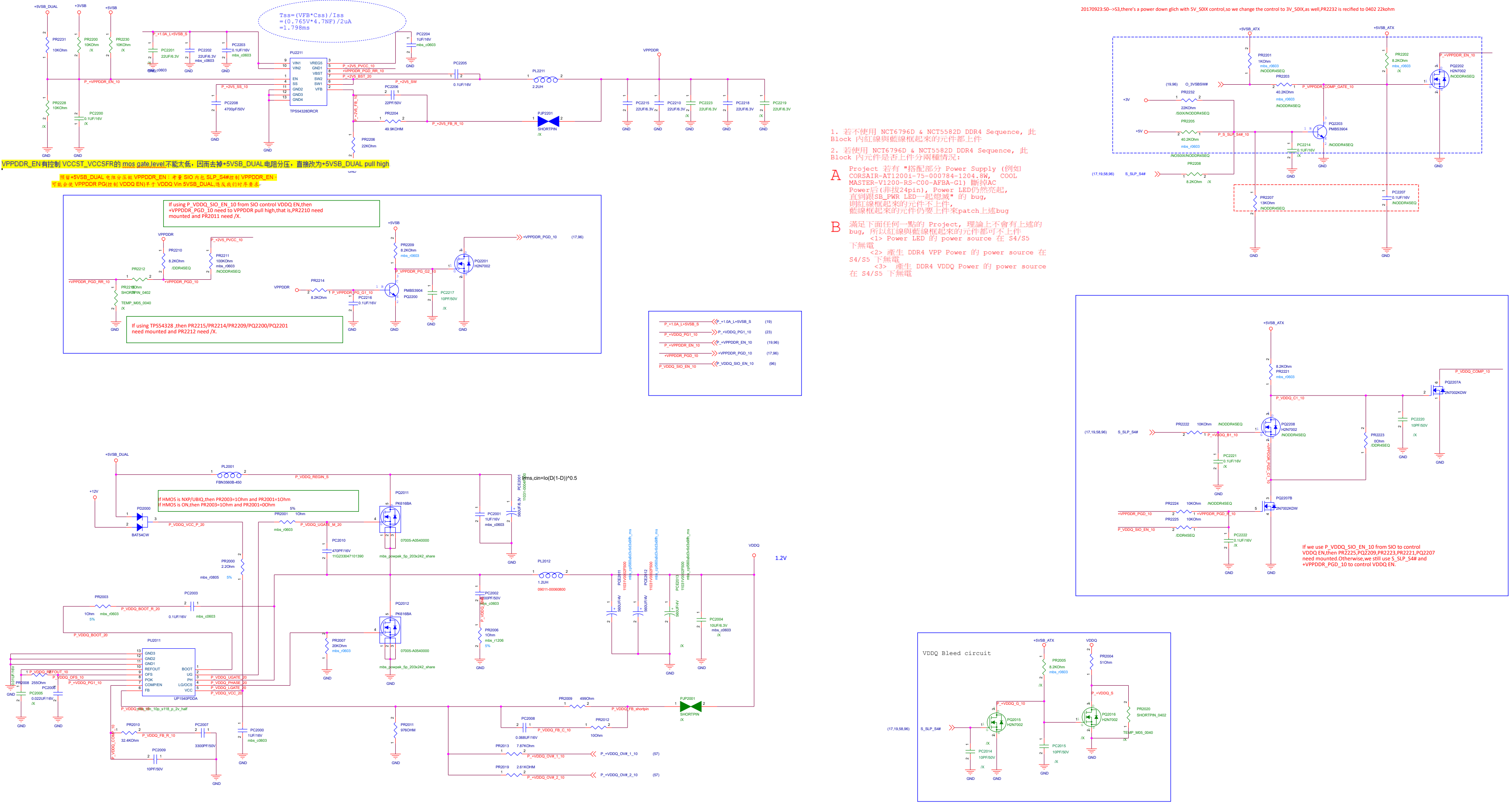






<Variant Name>

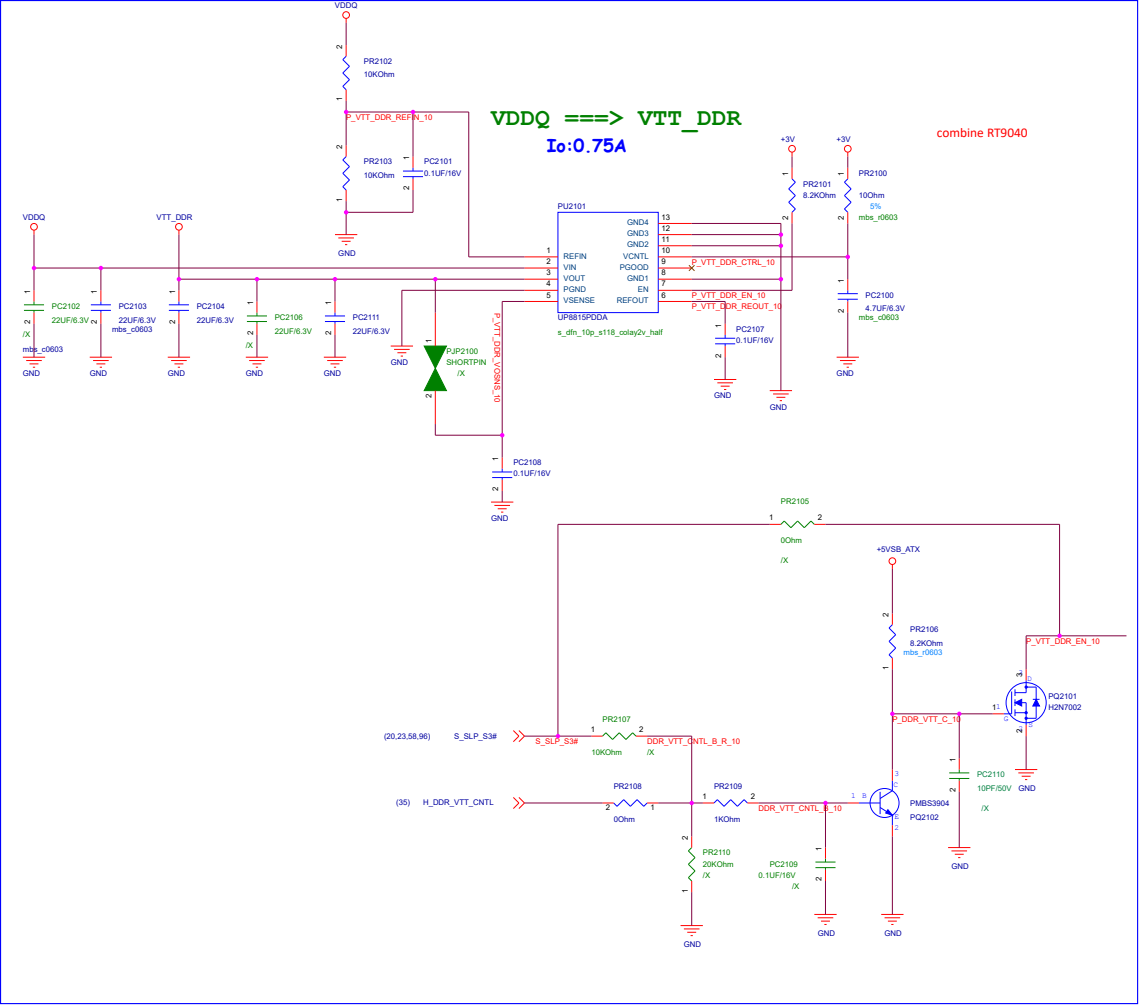
ASUSTek COMPUTER INC.	Title : VCCGT DRIVER	
	Engineer: RAY	
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 16 of 113	



P_+VDDQ_OV#_1_10	P_+VDDQ_OV#_2_10	VDDQ show value	VDDQ design value
X	X	1.2V	1.209V
0	X	1.25V	1.256V
X	0	1.35V	1.362V
0	0	1.40V	1.413V

<Variant Name>

ASUSTek COMPUTER INC.	Title : 1.2VDUAL		
	Engineer: RAY		
Size: A1	Project Name: SkyLake VC		Rev: R1.00
Date: Monday, June 11, 2018		Sheet 17 of 113	

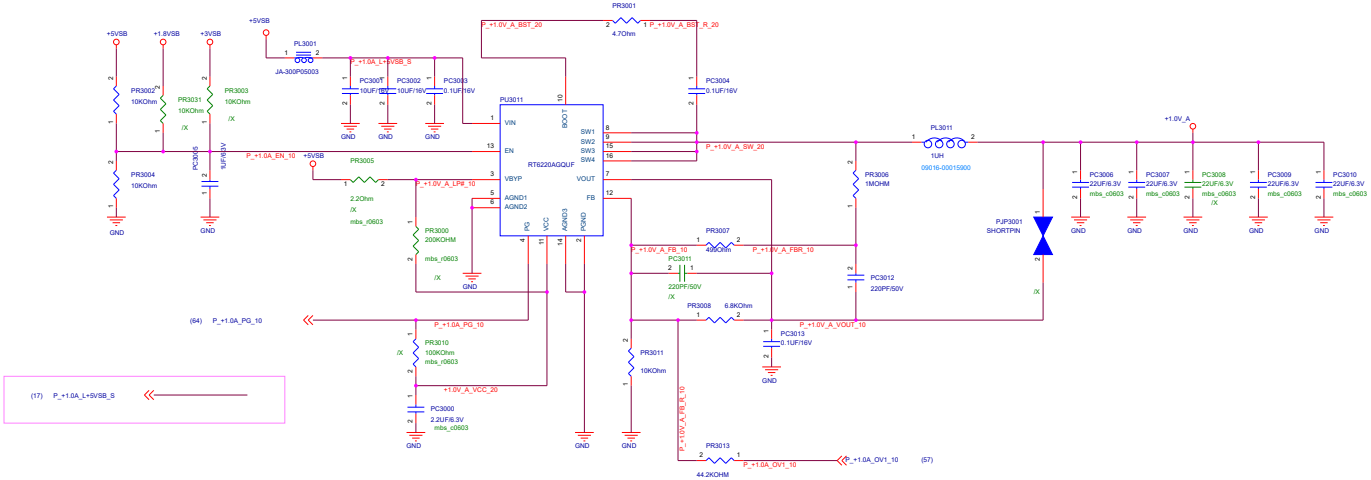


<Variant Name>

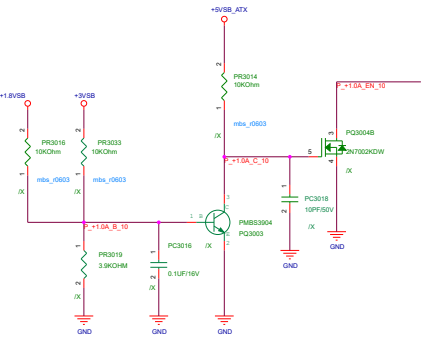
ASUSTek COMPUTER INC.	Title : VPPDDR	
	Engineer: Mandy_cao	
Size: A2	Project Name: SkyLake DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 18 of 113	

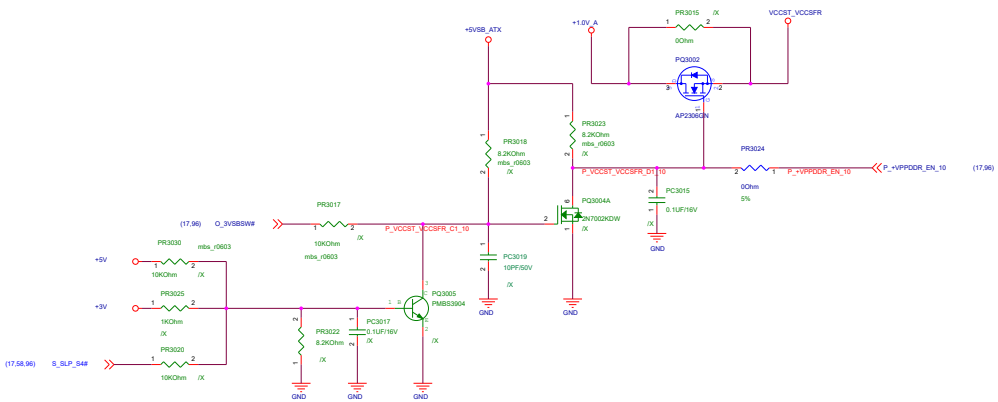
If IC is NB671LB,then PR300's optional is N/A.

If IC is RT6220A,then PR3000's optional is /X.



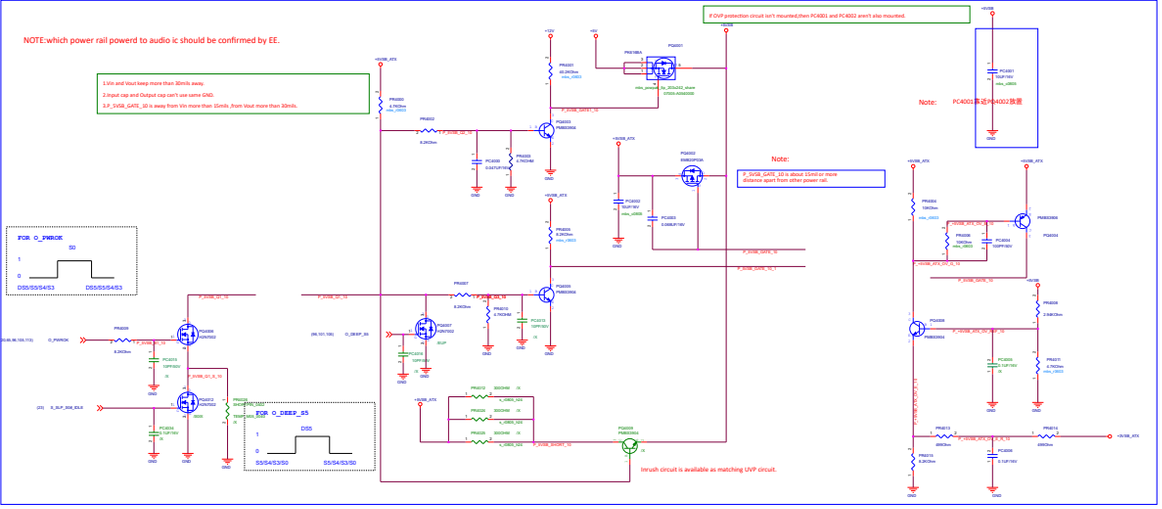
P_+1.0A_OV1_10	+1.0A Show value	+1.0A Design value
1	1.00V	1.008V(deafault)
0	1.1V	1.1098V



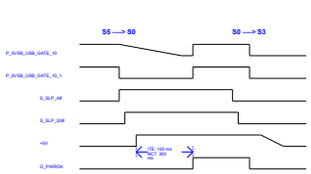


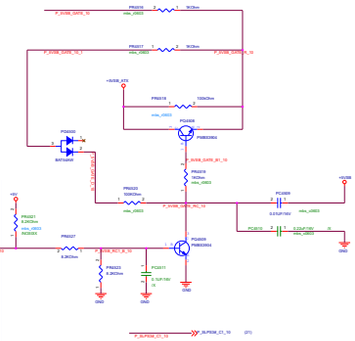
<variant_name>

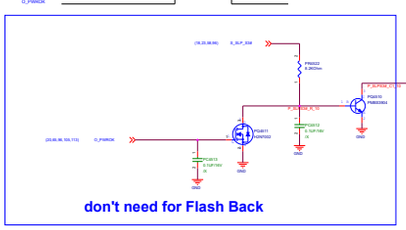
ASUSTek COMPUTER INC.	Title :	+1.0A/VCCST_VCCSFR
	Engineer:	Jun_Zhang
Size: A2	Project Name: Coffeelake	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 19 of 113	

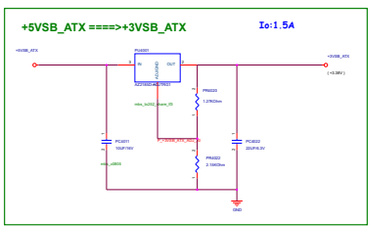


Inrush Circuit for USB Port default have Power or Flash Back Function









Title :	+5VSB>3VSB_ATX>1.5V_A		
Engineer:	Mandy_cao		
Rev	Project name	KabyLake DEMO	Sheet
A0			59
Date:	Monday, June 12, 2017	Time:	08:47:56

If OVP protection circuit isn't mounted,then PC4501 isn't also mounted.

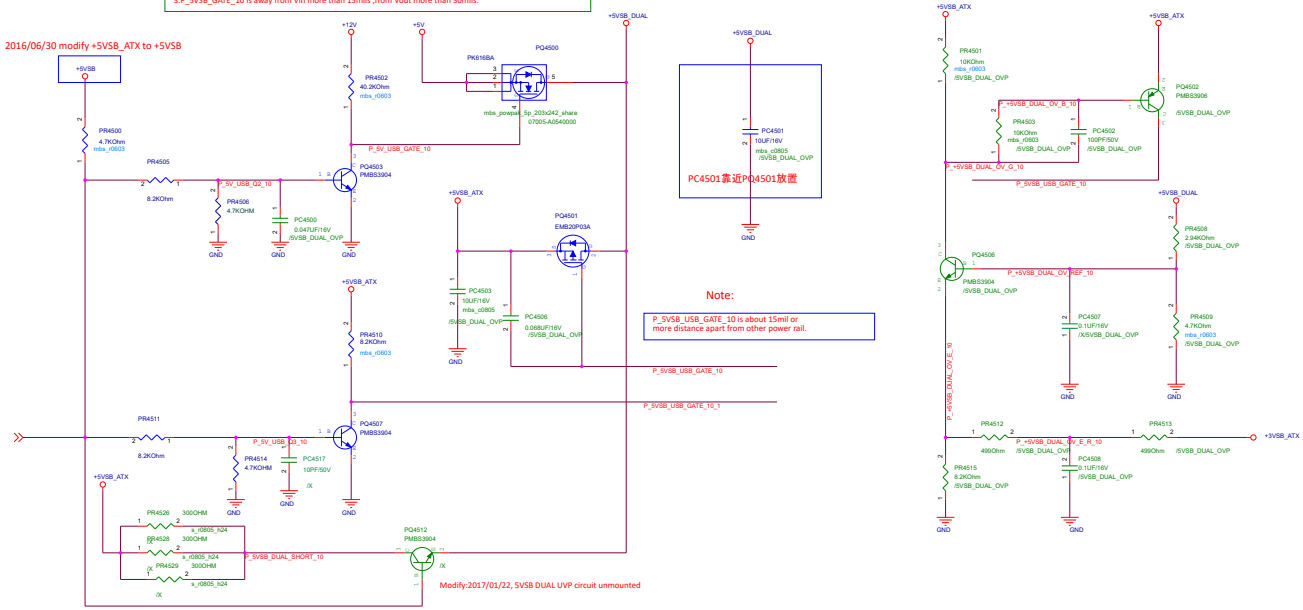
BOM	主板上+5VSB_DUAL 上有接不耐 12V 高壓的元件且上件，例如用在 Type-C 上的 Power Switch G517 08016-01100500	主板上+5VSB_DUAL 上沒有接不耐 12V 高壓的元件或者主板上+5VSB_DUAL 上有接不耐 12V 高壓的元件但不上件
/5VSB_DUAL_OVP	mount	unmount

1.Vin and Vout keep more than 30mils away.

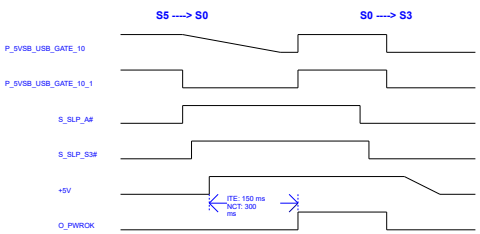
2.Input cap and Output cap can't use same GND.

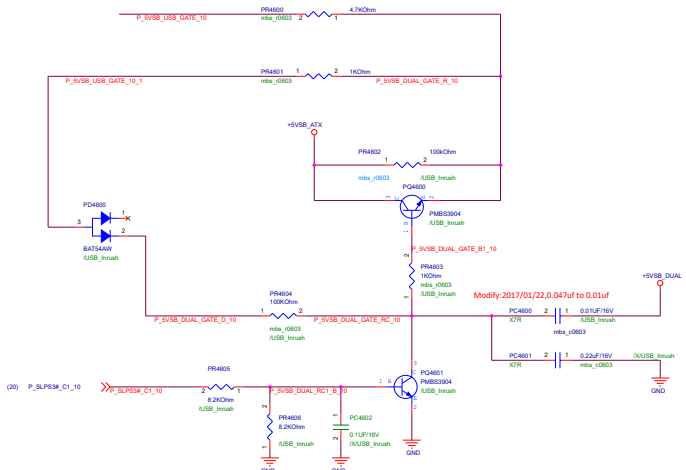
3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

2016/06/30 modify +5VSB_ATX to +5VSB



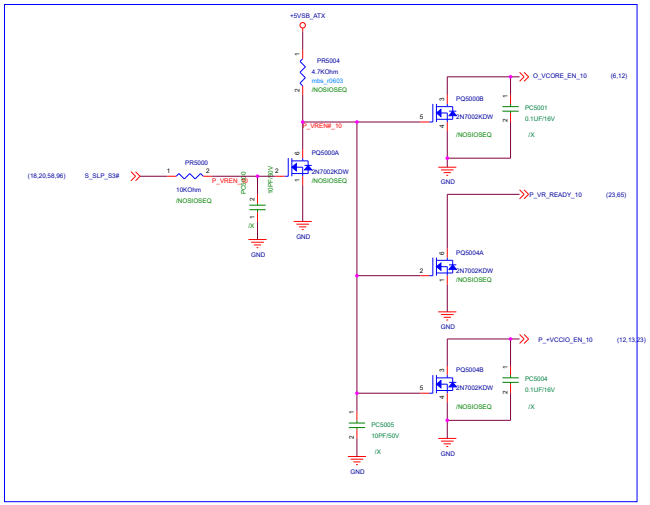
+5VSB_DUAL Inrush Circuit for USB Port default have Power

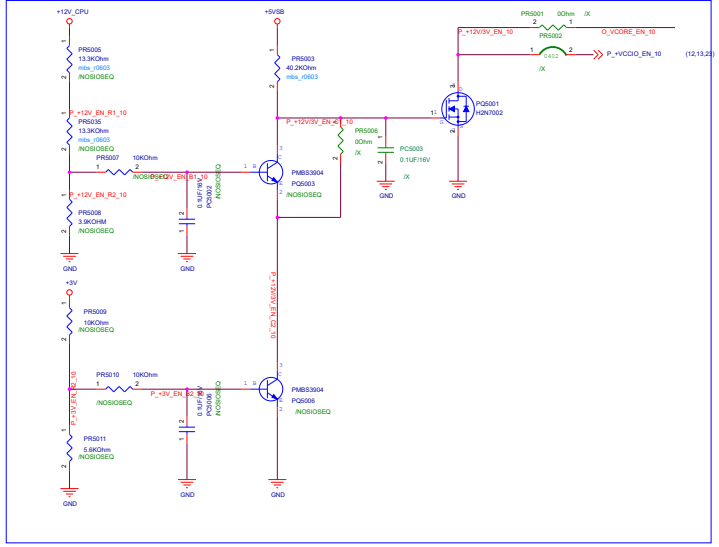


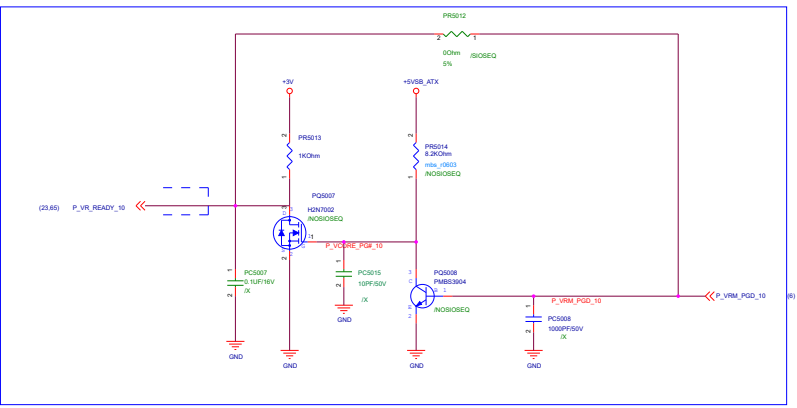


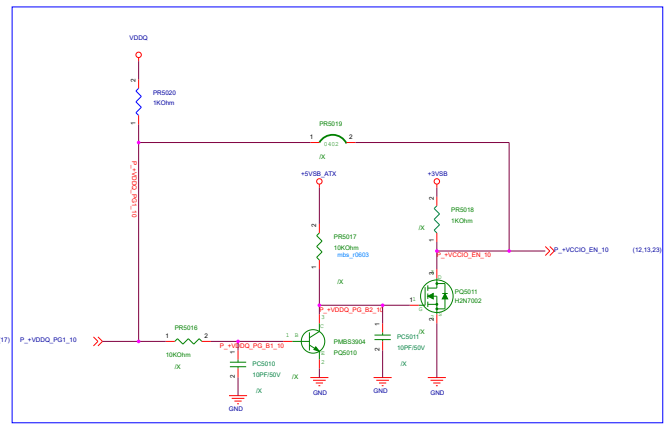
<Variant Name>

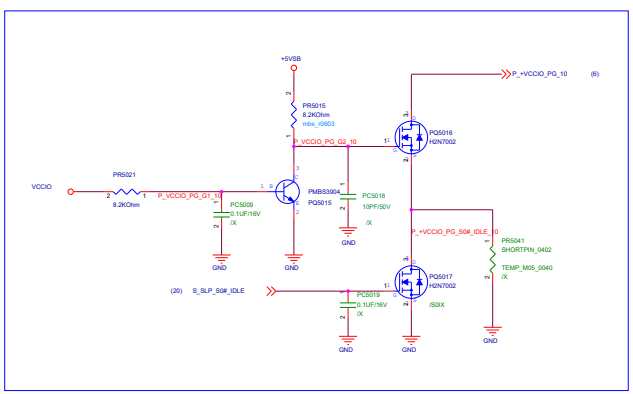
ASUSTeK COMPUTER INC.	Title : +5VSB	
	Engineer: Mandy_cao	
Size: A2	Project Name: Kabylake demo	Rev: 91.00
Date: Monday, June 11, 2018	Sheet 21 of 113	







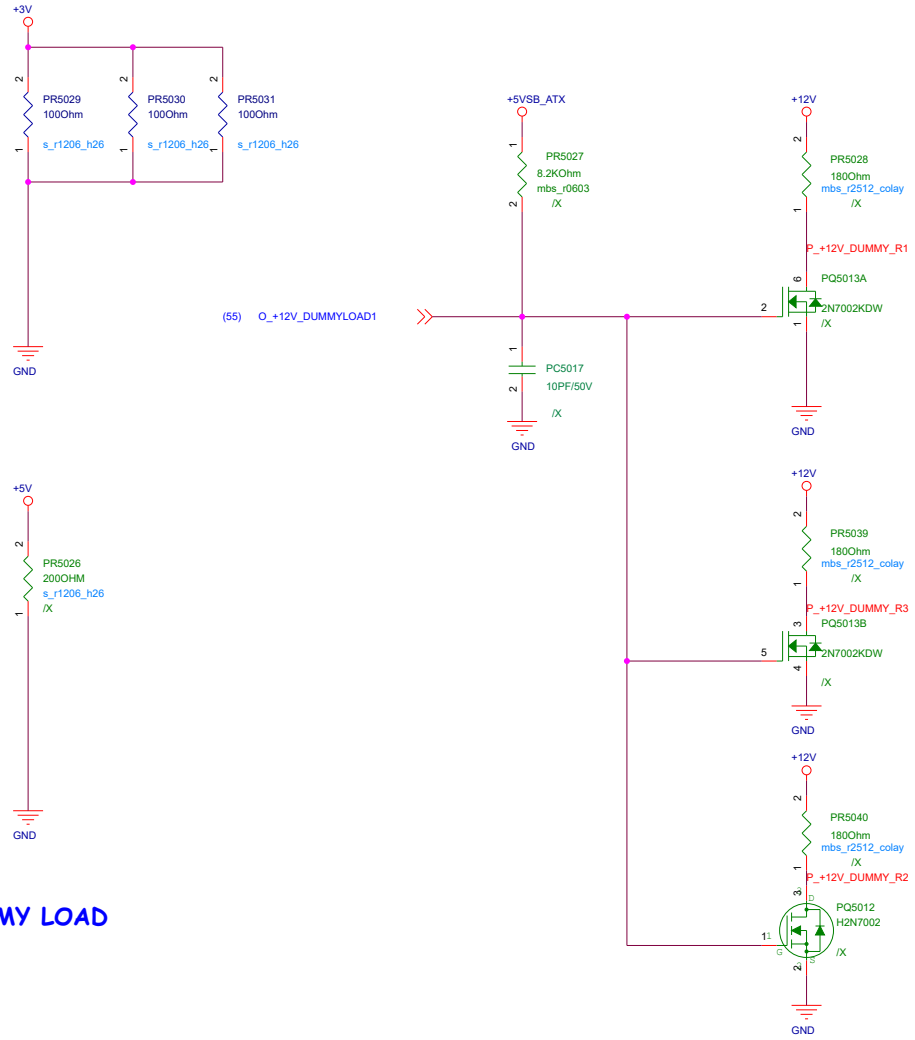




<variant_name>

ASUSTek COMPUTER INC.	Title :	POWER SEQUENCE	
	Engineer:	Mandy_cao	
Size: A2	Project Name: coffeelake demo		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 23 of 115		

whether 5V&3V dummy load need mounting,please confirm with EE.



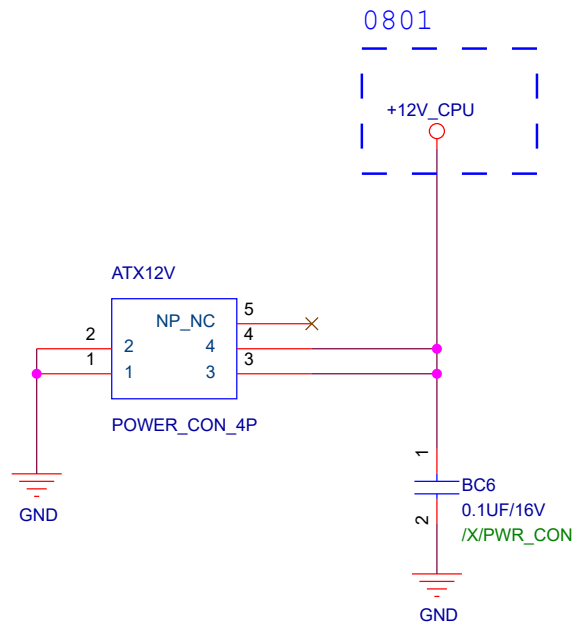
DUMMY LOAD

<Variant Name>

ASUSTek COMPUTER INC.	Title : NA	
	Engineer: Mandy_cao	
Size: A3	Project Name: KabyLake DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 25 of 113	

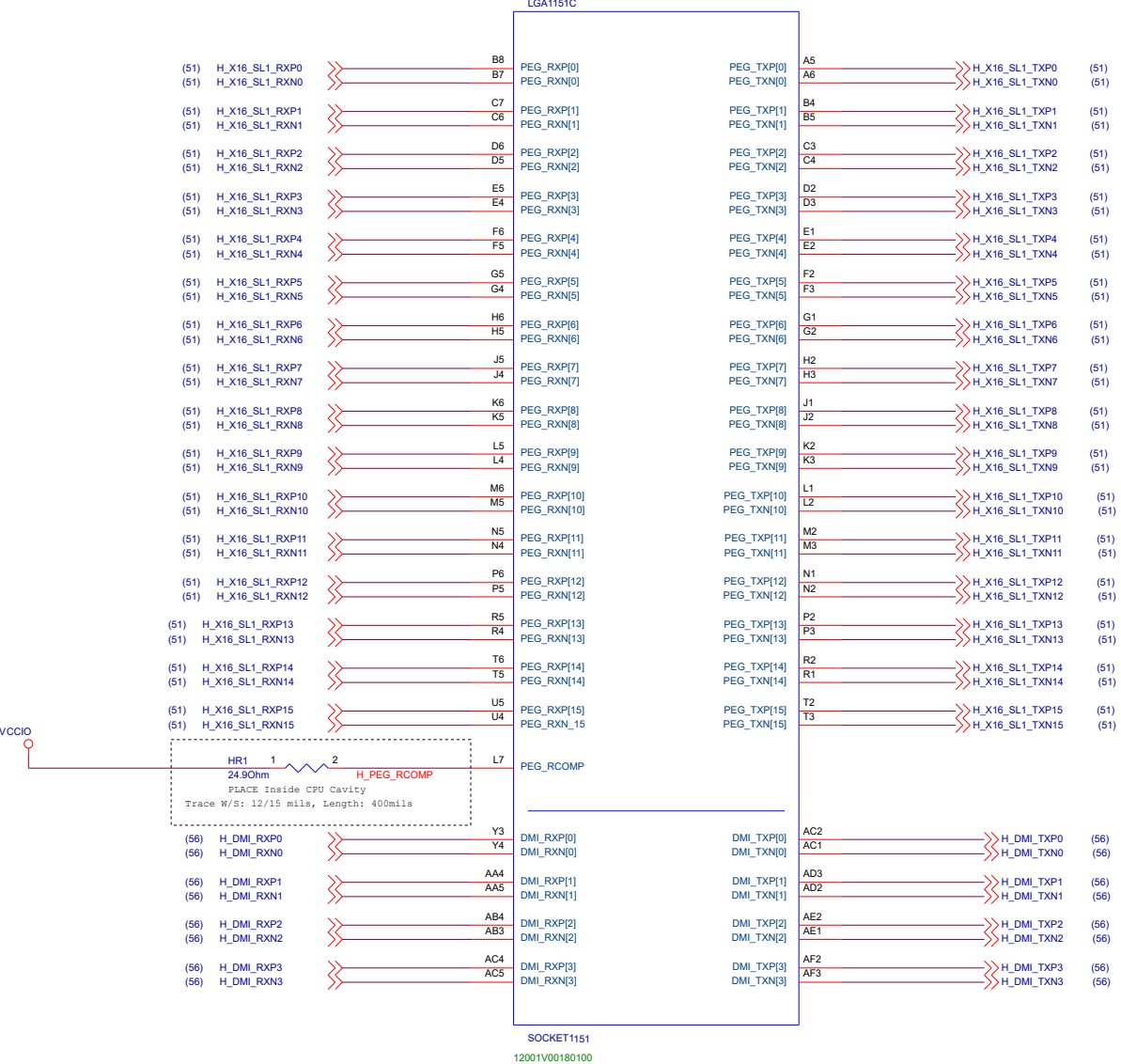
4 Pin +12V Connector

顏色：W

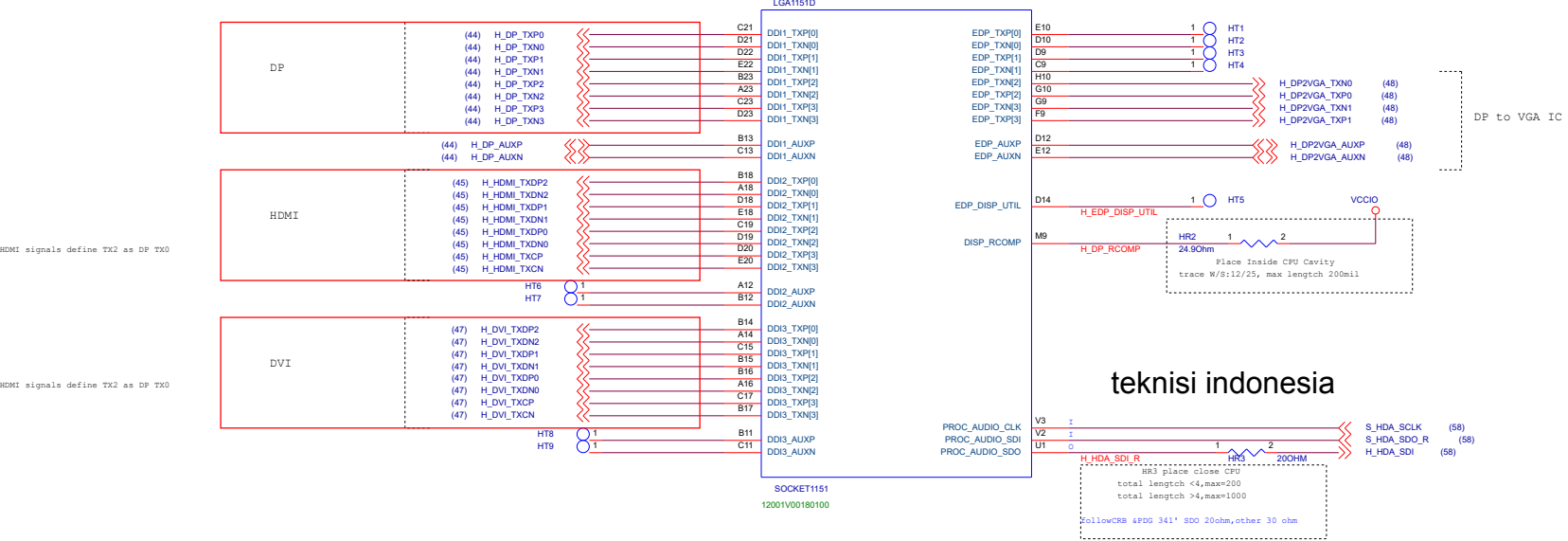


<Variant Name>

ASUSTek COMPUTER INC.	Title : NA	
	Engineer: Mandy_cao	
Size: A	Project Name: KabyLake DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 30 of 113	



ASUSTek Computer Inc.	Title :	LGA1151 (DMI/PEG)	
	Engineer:	Jay_Tong	
Size: A3	Project Name: CFL CHIPSET DEMO		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 31 of 113		



ASUSTek Computer Inc.	Title : LGA1150 (FDI/DISPLAY)		
	Engineer: Bing-jie_Wang		
Size: A3	Project Name: SKYLAKE CHIPSET DEMO		Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 32 of 113		

Channel A
4 Layer routing

(39) D4_DQ_A[0:63]

LGA1151A

AE38	D4_DQ_A5	DDR0_DQ[0]
AE37	D4_DQ_A1	DDR0_DQ[1]
AG38	D4_DQ_A2	DDR0_DQ[2]
AG37	D4_DQ_A3	DDR0_DQ[3]
AE39	D4_DQ_A4	DDR0_DQ[4]
AE40	D4_DQ_A0	DDR0_DQ[5]
AG39	D4_DQ_A6	DDR0_DQ[6]
AG40	D4_DQ_A7	DDR0_DQ[7]
AJ38	D4_DQ_A13	DDR0_DQ[8]
AJ37	D4_DQ_A9	DDR0_DQ[9]
AL38	D4_DQ_A10	DDR0_DQ[10]
AL37	D4_DQ_A11	DDR0_DQ[11]
AJ40	D4_DQ_A8	DDR0_DQ[12]
AJ39	D4_DQ_A12	DDR0_DQ[13]
AL39	D4_DQ_A14	DDR0_DQ[14]
AL40	D4_DQ_A15	DDR0_DQ[15]
AN38	D4_DQ_A21	DDR0_DQ[16]/DDR0_DQ[32]
AN40	D4_DQ_A16	DDR0_DQ[17]/DDR0_DQ[33]
AR38	D4_DQ_A18	DDR0_DQ[18]/DDR0_DQ[34]
AR37	D4_DQ_A19	DDR0_DQ[19]/DDR0_DQ[35]
AN39	D4_DQ_A20	DDR0_DQ[20]/DDR0_DQ[36]
AN37	D4_DQ_A17	DDR0_DQ[21]/DDR0_DQ[37]
AR39	D4_DQ_A22	DDR0_DQ[22]/DDR0_DQ[38]
AR40	D4_DQ_A23	DDR0_DQ[23]/DDR0_DQ[39]
AW37	D4_DQ_A25	DDR0_DQ[24]/DDR0_DQ[40]
AU38	D4_DQ_A28	DDR0_DQ[25]/DDR0_DQ[41]
AV35	D4_DQ_A27	DDR0_DQ[26]/DDR0_DQ[42]
AW35	D4_DQ_A31	DDR0_DQ[27]/DDR0_DQ[43]
AU37	D4_DQ_A29	DDR0_DQ[28]/DDR0_DQ[44]
AV37	D4_DQ_A24	DDR0_DQ[29]/DDR0_DQ[45]
AT35	D4_DQ_A30	DDR0_DQ[30]/DDR0_DQ[46]
AU35	D4_DQ_A26	DDR0_DQ[31]/DDR0_DQ[47]
AY8	D4_DQ_A32	DDR0_DQ[32]/DDR1_DQ[0]
AW8	D4_DQ_A36	DDR0_DQ[33]/DDR1_DQ[1]
AV6	D4_DQ_A34	DDR0_DQ[34]/DDR1_DQ[2]
AU6	D4_DQ_A35	DDR0_DQ[35]/DDR1_DQ[3]
AU8	D4_DQ_A33	DDR0_DQ[36]/DDR1_DQ[4]
AV8	D4_DQ_A37	DDR0_DQ[37]/DDR1_DQ[5]
AW6	D4_DQ_A39	DDR0_DQ[38]/DDR1_DQ[6]
AY6	D4_DQ_A38	DDR0_DQ[39]/DDR1_DQ[7]
AY4	D4_DQ_A44	DDR0_DQ[40]/DDR1_DQ[8]
AV4	D4_DQ_A40	DDR0_DQ[41]/DDR1_DQ[9]
AT1	D4_DQ_A47	DDR0_DQ[42]/DDR1_DQ[10]
AT2	D4_DQ_A43	DDR0_DQ[43]/DDR1_DQ[11]
AV3	D4_DQ_A41	DDR0_DQ[44]/DDR1_DQ[12]
AW4	D4_DQ_A45	DDR0_DQ[45]/DDR1_DQ[13]
AT4	D4_DQ_A46	DDR0_DQ[46]/DDR1_DQ[14]
AT3	D4_DQ_A42	DDR0_DQ[47]/DDR1_DQ[15]
AP2	D4_DQ_A49	DDR0_DQ[48]/DDR1_DQ[32]
AM4	D4_DQ_A54	DDR0_DQ[49]/DDR1_DQ[33]
AP3	D4_DQ_A53	DDR0_DQ[50]/DDR1_DQ[34]
AM3	D4_DQ_A50	DDR0_DQ[51]/DDR1_DQ[35]
AP4	D4_DQ_A52	DDR0_DQ[52]/DDR1_DQ[36]
AM2	D4_DQ_A51	DDR0_DQ[53]/DDR1_DQ[37]
AP1	D4_DQ_A48	DDR0_DQ[54]/DDR1_DQ[38]
AM1	D4_DQ_A55	DDR0_DQ[55]/DDR1_DQ[39]
AK3	D4_DQ_A61	DDR0_DQ[56]/DDR1_DQ[40]
AH1	D4_DQ_A63	DDR0_DQ[57]/DDR1_DQ[41]
AK4	D4_DQ_A60	DDR0_DQ[58]/DDR1_DQ[42]
AH2	D4_DQ_A59	DDR0_DQ[59]/DDR1_DQ[43]
AH4	D4_DQ_A62	DDR0_DQ[60]/DDR1_DQ[44]
AK2	D4_DQ_A57	DDR0_DQ[61]/DDR1_DQ[45]
AH3	D4_DQ_A58	DDR0_DQ[62]/DDR1_DQ[46]
AK1	D4_DQ_A56	DDR0_DQ[63]/DDR1_DQ[47]

AU33	DDR0_ECC[0]
AT33	DDR0_ECC[1]
AW33	DDR0_ECC[2]
AV31	DDR0_ECC[3]
AU31	DDR0_ECC[4]
AV33	DDR0_ECC[5]
AW31	DDR0_ECC[6]
AY31	DDR0_ECC[7]

AW18	DDR0_CKP[0]	D4_MA_CLK0 (39)
AV18	DDR0_CKN[0]	D4_MA_CLK#0 (39)
AW17	DDR0_CKP[1]	D4_MA_CLK1 (39)
AY17	DDR0_CKN[1]	D4_MA_CLK#1 (39)
AW16	DDR0_CKP[2]	
AV16	DDR0_CKN[2]	
AT16	DDR0_CKP[3]	
AU16	DDR0_CKN[3]	
AY24	DDR0_CKE[0]	D4_CKE_A0 (39)
AW24	DDR0_CKE[1]	D4_CKE_A1 (39)
AV24	DDR0_CKE[2]	
AV25	DDR0_CKE[3]	
AW12	DDR0_CS#[0]	D4_CS_A#0 (39)
AU11	DDR0_CS#[1]	D4_CS_A#1 (39)
AV13	DDR0_CS#[2]	
AV10	DDR0_CS#[3]	
AW11	DDR0_ODT[0]	D4_ODT_A0 (39)
AU14	DDR0_ODT[1]	D4_ODT_A1 (39)
AU12	DDR0_ODT[2]	
AY10	DDR0_ODT[3]	
AY13	DDR0_BA[0]	D4_BAA0 (39)
AV15	DDR0_BA[1]	D4_BAA1 (39)
AW23	DDR0_BG[0]	D4_BGA0 (39)

D4_MAA[0:16] (39)

AW13	DDR0_MA[16]	D4_MAA16
AV14	DDR0_MA[14]	D4_MAA14
AY11	DDR0_MA[15]	D4_MAA15
AW15	DDR0_MA[0]	D4_MAA0
AU18	DDR0_MA[1]	D4_MAA1
AT17	DDR0_MA[2]	D4_MAA2
AV19	DDR0_MA[3]	D4_MAA3
AT19	DDR0_MA[4]	D4_MAA4
AU20	DDR0_MA[5]	D4_MAA5
AV20	DDR0_MA[6]	D4_MAA6
AU21	DDR0_MA[7]	D4_MAA7
AT20	DDR0_MA[8]	D4_MAA8
AT22	DDR0_MA[9]	D4_MAA9
AY14	DDR0_MA[10]	D4_MAA10
AU22	DDR0_MA[11]	D4_MAA11
AV22	DDR0_MA[12]	D4_MAA12
AV12	DDR0_MA[13]	D4_MAA13
AV23	DDR0_BG[1]	D4_BGA1 (39)
AU24	DDR0_ACT#	D4_A_ACT# (39)
AY15	DDR0_PAR	D4_A_PAR (39)
AT23	DDR0_ALERT#	D4_A_ALERT# (39)

AF39	DDR0_DQSN[0]	D4_DQS_A#0 (39)
AK39	DDR0_DQSN[1]	D4_DQS_A#1 (39)
AP39	DDR0_DQSN[2]/DDR0_DQSN[4]	D4_DQS_A#2 (39)
AU36	DDR0_DQSN[3]/DDR0_DQSN[5]	D4_DQS_A#3 (39)
AW7	DDR0_DQSN[4]/DDR1_DQSN[0]	D4_DQS_A#4 (39)
AU3	DDR0_DQSN[5]/DDR1_DQSN[1]	D4_DQS_A#5 (39)
AN3	DDR0_DQSN[6]/DDR1_DQSN[4]	D4_DQS_A#6 (39)
AJ3	DDR0_DQSN[7]/DDR1_DQSN[5]	D4_DQS_A#7 (39)
AF38	DDR0_DQSP[0]	D4_DQS_A0 (39)
AK38	DDR0_DQSP[1]	D4_DQS_A1 (39)
AP38	DDR0_DQSP[2]/DDR0_DQSP[4]	D4_DQS_A2 (39)
AV36	DDR0_DQSP[3]/DDR0_DQSP[5]	D4_DQS_A3 (39)
AV7	DDR0_DQSP[4]/DDR1_DQSP[0]	D4_DQS_A4 (39)
AU2	DDR0_DQSP[5]/DDR1_DQSP[1]	D4_DQS_A5 (39)
AN2	DDR0_DQSP[6]/DDR1_DQSP[4]	D4_DQS_A6 (39)
AJ2	DDR0_DQSP[7]/DDR1_DQSP[5]	D4_DQS_A7 (39)
AV32	DDR0_DQSP[8]	
AU32	DDR0_DQSN[8]	

SOCKET1151
12001V00180100

ASUSTek Computer Inc.

Title : LGA1151 (DDR4_A Control)

Engineer: Bing-jie_Wang

Size	Project Name	Rev
A3	SKYLAKE CHIPSET DEMO	R1.00

Date: Monday, June 11, 2018 Sheet 33 of 113

Follow CRB

Channel B
4 Layer routing

(40) D4_DQ_B[0:63]

LGA1151B

AD34	D4_DQ_B4	DDR1_DQ[0]/DDR0_DQ[16]
AD35	D4_DQ_B5	DDR1_DQ[1]/DDR0_DQ[17]
AG35	D4_DQ_B7	DDR1_DQ[2]/DDR0_DQ[18]
AH35	D4_DQ_B3	DDR1_DQ[3]/DDR0_DQ[19]
AE35	D4_DQ_B1	DDR1_DQ[4]/DDR0_DQ[20]
AE34	D4_DQ_B0	DDR1_DQ[5]/DDR0_DQ[21]
AG34	D4_DQ_B6	DDR1_DQ[6]/DDR0_DQ[22]
AH34	D4_DQ_B2	DDR1_DQ[7]/DDR0_DQ[23]
AK35	D4_DQ_B13	DDR1_DQ[8]/DDR0_DQ[24]
AL35	D4_DQ_B9	DDR1_DQ[9]/DDR0_DQ[25]
AK32	D4_DQ_B14	DDR1_DQ[10]/DDR0_DQ[26]
AL32	D4_DQ_B15	DDR1_DQ[11]/DDR0_DQ[27]
AK34	D4_DQ_B12	DDR1_DQ[12]/DDR0_DQ[28]
AL34	D4_DQ_B8	DDR1_DQ[13]/DDR0_DQ[29]
AK31	D4_DQ_B10	DDR1_DQ[14]/DDR0_DQ[30]
AL31	D4_DQ_B11	DDR1_DQ[15]/DDR0_DQ[31]
AP35	D4_DQ_B16	DDR1_DQ[16]/DDR0_DQ[48]
AN35	D4_DQ_B20	DDR1_DQ[17]/DDR0_DQ[49]
AN32	D4_DQ_B22	DDR1_DQ[18]/DDR0_DQ[50]
AP32	D4_DQ_B23	DDR1_DQ[19]/DDR0_DQ[51]
AN34	D4_DQ_B17	DDR1_DQ[20]/DDR0_DQ[52]
AP34	D4_DQ_B21	DDR1_DQ[21]/DDR0_DQ[53]
AN31	D4_DQ_B18	DDR1_DQ[22]/DDR0_DQ[54]
AP31	D4_DQ_B19	DDR1_DQ[23]/DDR0_DQ[55]
AL29	D4_DQ_B28	DDR1_DQ[24]/DDR0_DQ[56]
AM29	D4_DQ_B24	DDR1_DQ[25]/DDR0_DQ[57]
AP29	D4_DQ_B30	DDR1_DQ[26]/DDR0_DQ[58]
AR29	D4_DQ_B26	DDR1_DQ[27]/DDR0_DQ[59]
AM28	D4_DQ_B25	DDR1_DQ[28]/DDR0_DQ[60]
AL28	D4_DQ_B29	DDR1_DQ[29]/DDR0_DQ[61]
AR28	D4_DQ_B27	DDR1_DQ[30]/DDR0_DQ[62]
AP28	D4_DQ_B31	DDR1_DQ[31]/DDR0_DQ[63]
AR12	D4_DQ_B32	DDR1_DQ[32]/DDR1_DQ[16]
AP12	D4_DQ_B33	DDR1_DQ[33]/DDR1_DQ[17]
AM13	D4_DQ_B38	DDR1_DQ[34]/DDR1_DQ[18]
AL13	D4_DQ_B34	DDR1_DQ[35]/DDR1_DQ[19]
AR13	D4_DQ_B36	DDR1_DQ[36]/DDR1_DQ[20]
AP13	D4_DQ_B37	DDR1_DQ[37]/DDR1_DQ[21]
AM12	D4_DQ_B39	DDR1_DQ[38]/DDR1_DQ[22]
AL12	D4_DQ_B35	DDR1_DQ[39]/DDR1_DQ[23]
AP10	D4_DQ_B44	DDR1_DQ[40]/DDR1_DQ[24]
AR10	D4_DQ_B45	DDR1_DQ[41]/DDR1_DQ[25]
AR7	D4_DQ_B46	DDR1_DQ[42]/DDR1_DQ[26]
AP7	D4_DQ_B42	DDR1_DQ[43]/DDR1_DQ[27]
AR9	D4_DQ_B41	DDR1_DQ[44]/DDR1_DQ[28]
AP9	D4_DQ_B40	DDR1_DQ[45]/DDR1_DQ[29]
AR6	D4_DQ_B47	DDR1_DQ[46]/DDR1_DQ[30]
AP6	D4_DQ_B43	DDR1_DQ[47]/DDR1_DQ[31]
AM10	D4_DQ_B52	DDR1_DQ[48]
AL10	D4_DQ_B53	DDR1_DQ[49]
AM7	D4_DQ_B55	DDR1_DQ[50]
AL7	D4_DQ_B51	DDR1_DQ[51]
AM9	D4_DQ_B48	DDR1_DQ[52]
AL9	D4_DQ_B49	DDR1_DQ[53]
AM6	D4_DQ_B54	DDR1_DQ[54]
AL6	D4_DQ_B50	DDR1_DQ[55]
AJ6	D4_DQ_B61	DDR1_DQ[56]
AJ7	D4_DQ_B56	DDR1_DQ[57]
AE6	D4_DQ_B63	DDR1_DQ[58]
AF7	D4_DQ_B58	DDR1_DQ[59]
AH7	D4_DQ_B60	DDR1_DQ[60]
AH6	D4_DQ_B57	DDR1_DQ[61]
AE7	D4_DQ_B59	DDR1_DQ[62]
AF6	D4_DQ_B62	DDR1_DQ[63]

AR25		DDR1_ECC[0]
AR26		DDR1_ECC[1]
AM26		DDR1_ECC[2]
AM25		DDR1_ECC[3]
AP26		DDR1_ECC[4]
AP25		DDR1_ECC[5]
AL25		DDR1_ECC[6]
AL26		DDR1_ECC[7]

AM20	D4_MB_CLK0 (40)	DDR1_CKP[0]
AM21	D4_MB_CLK#0 (40)	DDR1_CKN[0]
AP22	D4_MB_CLK1 (40)	DDR1_CKP[1]
AP21	D4_MB_CLK#1 (40)	DDR1_CKN[1]
AN20		DDR1_CKP[2]
AN21		DDR1_CKN[2]
AP19		DDR1_CKP[3]
AP20		DDR1_CKN[3]
AY29		DDR1_CKE[0]
AV29	D4_CKE_B0 (40)	DDR1_CKE[1]
AW29	D4_CKE_B1 (40)	DDR1_CKE[2]
AU29		DDR1_CKE[3]
AP17	D4_CS_B#0 (40)	DDR1_CS#_0
AN15	D4_CS_B#1 (40)	DDR1_CS#_1
AN17		DDR1_CS#_2
AM15		DDR1_CS#_3
AM16	D4_ODT_B0 (40)	DDR1_ODT[0]
AL16	D4_ODT_B1 (40)	DDR1_ODT[1]
AP15		DDR1_ODT[2]
AL15		DDR1_ODT[3]
AN18		DDR1_MA[16]
AL17	D4_MAB16	DDR1_MA[14]
AP16	D4_MAB14	DDR1_MA[15]
	D4_MAB15	
AL18		DDR1_BA[0]
AM18	D4_BAB0 (40)	DDR1_BA[1]
AW28	D4_BAB1 (40)	DDR1_BG[0]
	D4_BGB0 (40)	
AL19		DDR1_MA[0]
AL22	D4_MAB0	DDR1_MA[1]
AM22	D4_MAB1	DDR1_MA[2]
AM23	D4_MAB2	DDR1_MA[3]
AP23	D4_MAB3	DDR1_MA[4]
AL23	D4_MAB4	DDR1_MA[5]
AW26	D4_MAB5	DDR1_MA[6]
AY26	D4_MAB6	DDR1_MA[7]
AU26	D4_MAB7	DDR1_MA[8]
AW27	D4_MAB8	DDR1_MA[9]
AP18	D4_MAB9	DDR1_MA[10]
AU27	D4_MAB10	DDR1_MA[11]
AV27	D4_MAB11	DDR1_MA[12]
AR15	D4_MAB12	DDR1_MA[13]
AY28	D4_MAB13	DDR1_BG[1]
AU28	D4_BGB1 (40)	DDR1_ACT#
	D4_B_ACT# (40)	
AL20	D4_B_PAR (40)	DDR1_PAR
AY25	D4_B_ALERT# (40)	DDR1_ALERT#

D4_MAB[0:16] (40)

AF34		DDR1_DQSN[0]/DDR0_DQSN[2]
AK33	D4_DQS_B#0 (40)	DDR1_DQSN[1]/DDR0_DQSN[3]
AN33	D4_DQS_B#1 (40)	DDR1_DQSN[2]/DDR0_DQSN[6]
AN29	D4_DQS_B#2 (40)	DDR1_DQSN[3]/DDR0_DQSN[7]
AN13	D4_DQS_B#3 (40)	DDR1_DQSN[4]/DDR1_DQSN[2]
AR8	D4_DQS_B#4 (40)	DDR1_DQSN[5]/DDR1_DQSN[3]
AM8	D4_DQS_B#5 (40)	DDR1_DQSN[6]
AG6	D4_DQS_B#6 (40)	DDR1_DQSN[7]
	D4_DQS_B#7 (40)	
AF35		DDR1_DQSP[0]/DDR0_DQSP[2]
AL33	D4_DQS_B0 (40)	DDR1_DQSP[1]/DDR0_DQSP[3]
AP33	D4_DQS_B1 (40)	DDR1_DQSP[2]/DDR0_DQSP[6]
AN28	D4_DQS_B2 (40)	DDR1_DQSP[3]/DDR0_DQSP[7]
AN12	D4_DQS_B3 (40)	DDR1_DQSP[4]/DDR1_DQSP[2]
AP8	D4_DQS_B4 (40)	DDR1_DQSP[5]/DDR1_DQSP[3]
AL8	D4_DQS_B5 (40)	DDR1_DQSP[6]
AG7	D4_DQS_B6 (40)	DDR1_DQSP[7]
	D4_DQS_B7 (40)	
AN25		DDR1_DQSP[8]
AN26		DDR1_DQSN[8]

AB40	H_D4_VREFCA_A (43)	DDR_VREF_CA
AC40		DDR0_VREF_DQ
AC39	TP_DIMM_DQ0 H_D4_VREFCA_B (43)	DDR1_VREF_DQ

1 HT10 /X/1151

SOCKET1151

12001V00180100

D4C1 0.022UF/16V

D4C2 0.022UF/16V

D4R13 24.9Ohm

D4R14 24.9Ohm

GND GND

CRB & Z97
High frequency
termination, can absorb
any high frequency
noise coming from
CPU/board crosstalk.

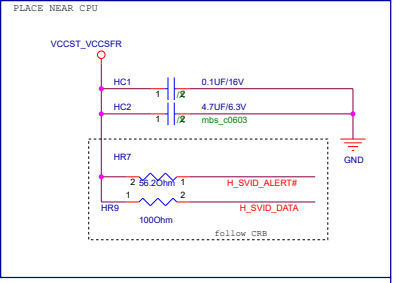
Title : LGA1151 (DDR4_B Control)

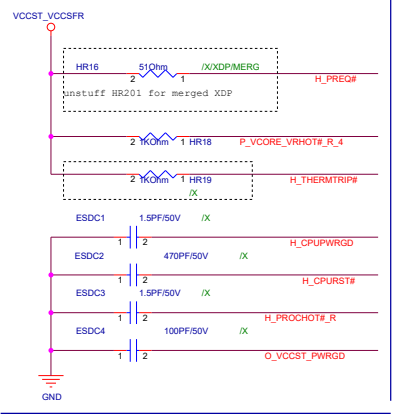
ASUSTek Computer Inc.

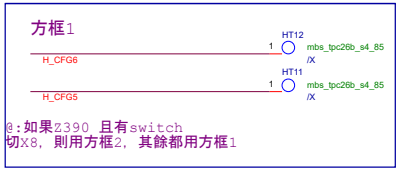
Engineer: CASPAR

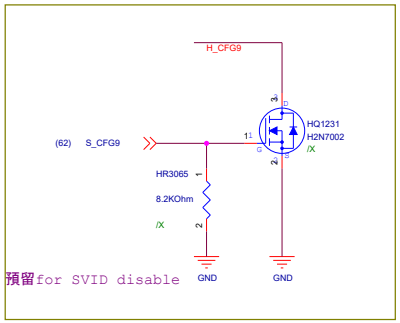
Size	Project Name	Rev
A3	SKYLAKE G	R1.00

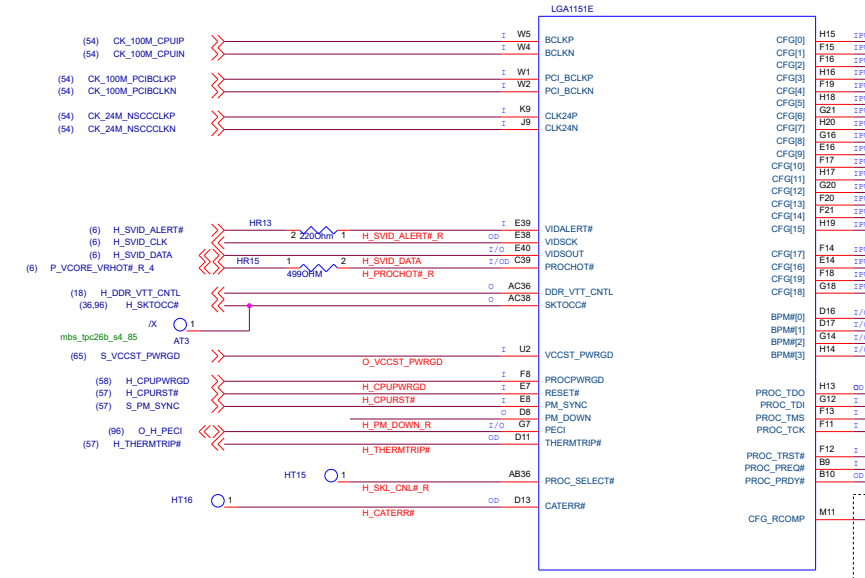
Date: Monday, June 11, 2018 Sheet 34 of 113

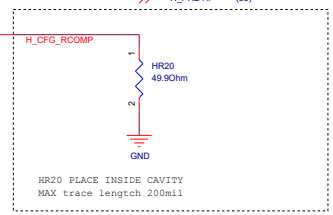


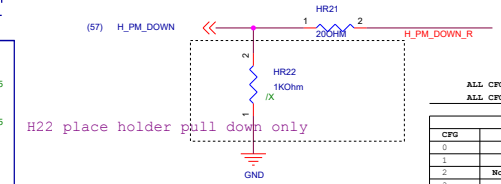












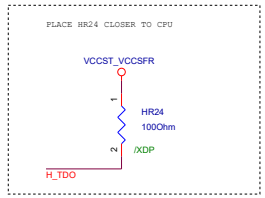
ALL CFG 1 = NO TERMINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD

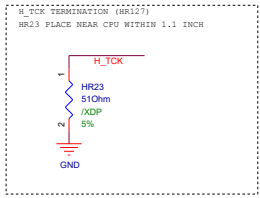
Skylake Strap Table Rev 0.85

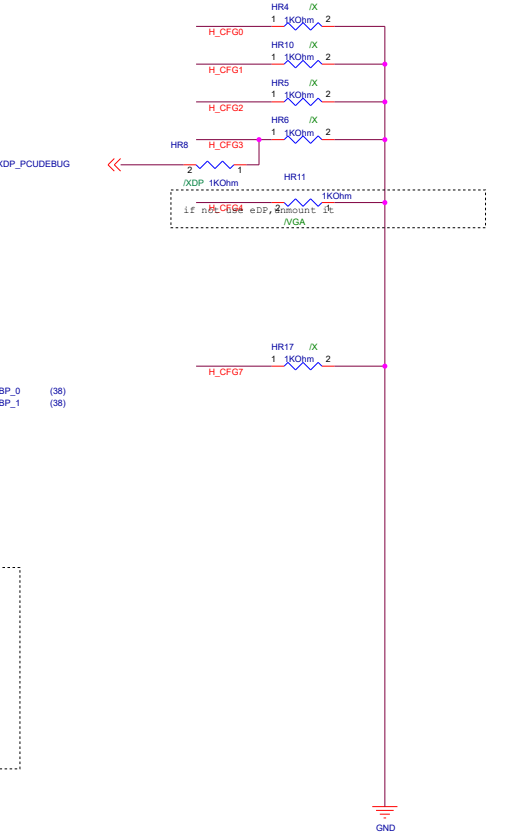
All Have Internal Pull-Ups +VCCIO

CFG	H = 1	L = 0	Description
0	Normal	STALL	EAR
1			Reserved
2	**Normal**	**Lane Reverse**	**PCIEX16 Lane Reversal**
3			Reserved
4	disable	enable	eDP
5	**PCIE Config**	**PCIE Config**	**SEL[0]**
6	**PCIE Config**	**PCIE Config**	**SEL[1]**
7	RESET#	BIOS REQ	
8-19			Reserved

- CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- CFG[1]: Reserved configuration lane.
- CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- CFG[3]: Reserved configuration lane.
- CFG[4]: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- CFG[6:5]: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- CFG[7]: PEG Training:
  - 1 = (default) PEGTrain immediately following RESET# de-assertion.
  - 0 = PEG Wait for BIOS for training.
- CFG[19:8]: Reserved configuration lanes.







ASUSTek Computer Inc.	Title :	LGA1151 (Control)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 35 of 113		

XDP Card USB3 CON1

CT1P1 1 H_CFG0 (35)
CT1P2 1 H_CFG1 (35)
CT1P3 1 H_CFG2 (35)
CT1P4 1 H_CFG3 (35)

CT1P8 1 H_CFG13 (35)
CT1P9 1 H_CFG12 (35)
CT1P10 1 H_CFG11 (35)
CT1P11 1 H_CFG10 (35)

CT1P13 1 H_CFG8 (35)
CT1P14 1 H_CFG7 (35)
CT1P15 1 H_TRST# (35)

XDP Card USB3 CON2

+VCCIO請從DIP電容跳線至XDP Card CON2 Pin1

CT2P1 1 H_CFG14 (35)
CT2P2 1 H_CFG15 (35)
CT2P3 1 H_CFG16 (35)
CT2P4 1 H_CFG17 (35)

GND請跳線至XDP Card CON2 Pin7

CT2P5 1 H_CFG18 (35)
CT2P6 1 H_CFG19 (35)
CT2P7 1 SKL_XDP_MBP_1 (35)
CT2P8 1 SKL_XDP_MBP_0 (35)
CT2P9 1 H_TDI (35)
CT2P10 1 H_PRDY# (35)
CT2P11 1 H_PREQ# (35)
CT2P12 1 XDP_PCUDEBUG (35)

+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19

XDP Card USB3 CON3

CT3P1 1 S_XDP_PREQ# (61)
CT3P2 1 S_XDP_PRDY# (61)

CT3P5 1 S_ITP_PMODE (58)

讓VCCST在插入XDP制具時有電

CT311請跳線至CON3 Pin11

CT3P9 1 S_JTAG_TMS (58)
CT3P10 1 S_JTAG_TDI (58)
CT3P11 1 S_JTAG_TCK (58)
CT3P12 1 S_XDP_TRST# (61)
CT3P13 1 S_JTAGX (38,58)

+VCCST請從DIP電容跳線至XDP Card CON3 Pin19

XDP Card USB3 CON4

+3VSB請從DIP電容跳線至XDP Card CON4 Pin1

CT4P6 1 H_TCK (35)
CT4P7 1 H_TMS (35)
CT4P8 1 C_CPU_XDP (54)
CT4P9 1 C_CPU_XDP# (54)
CT4P10 1 H_TDO (35)
CT4P11 1 S_JTAG_TDO (58)

+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19

HR128
H_TCK 2 0Ohm 1 S_JTAGX (38,58)
/X

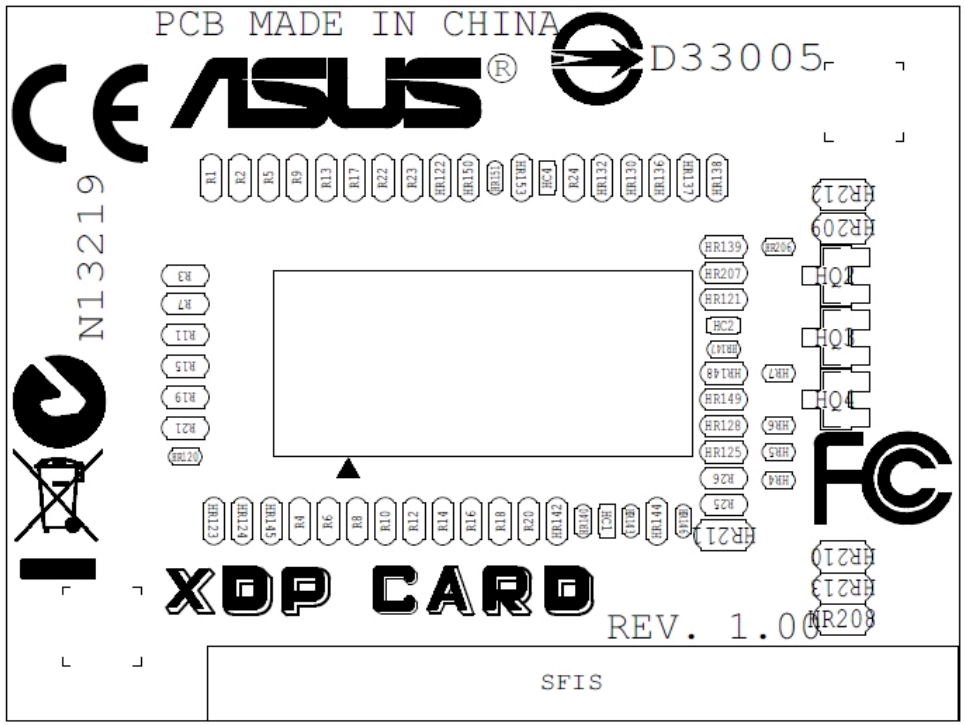
O_RSMRST#	H_CFG4
O_IOPWRBTN#	H_CFG5
O_RSTCON#	H_CFG6
H_CPUPWRGD	H_CFG9
S_SYSPWROK	
H_CPURST#	
S_SMBCLK_MAIN	
S_SMBDATA_MAIN	

由於RD CT*test pin會被做 no test
處理，所以刪除這些需要有test pin屬性，要layout額外加

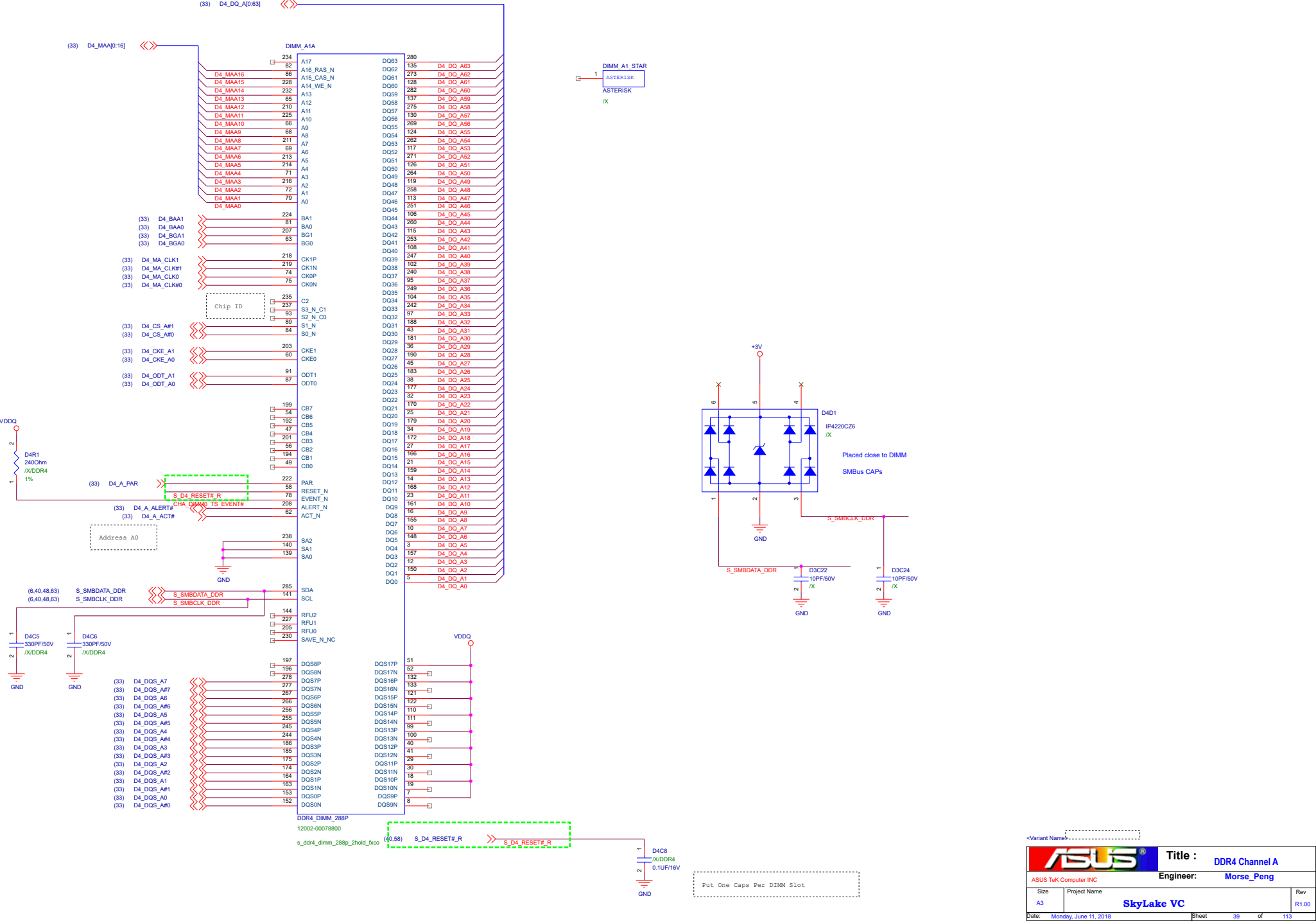
Naming Rule:
CTxPy==>請跳線到XDP Card CONx connector的Piny

Placement Rule:
此頁面測點全部放置背面靠近輸出端，
Layout會協助把Reference文字面開出，
若有需求初期PCB版本可洗背面文字，
但低階機種PVT PCB版本請記得通知板廠不洗背面文字

Power Rework:
+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19
+3VSB請從DIP電容跳線至XDP Card CON4 Pin1
+VCCST請從DIP電容跳線至XDP Card CON3 Pin19
+VCCIO請從DIP電容跳線至XDP Card CON2 Pin1
+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19
GND請跳線至XDP Card CON2 Pin7

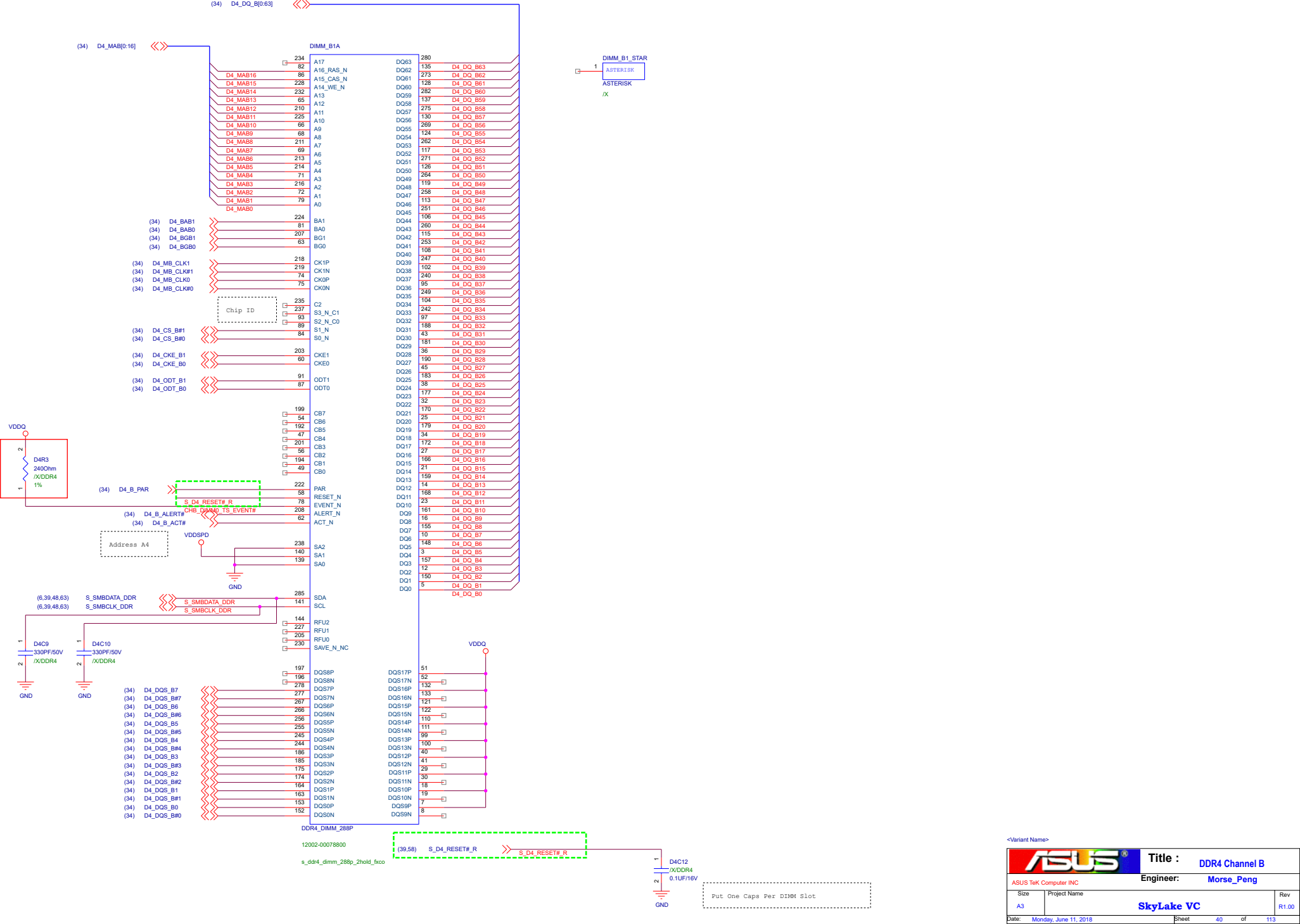


ASUSTek Computer Inc.	Title :	LGA1150 (XDP)	
	Engineer:	Grace	
Size: A3	Project Name: Z170 Series		Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 38 of 113		



<Variant Name>

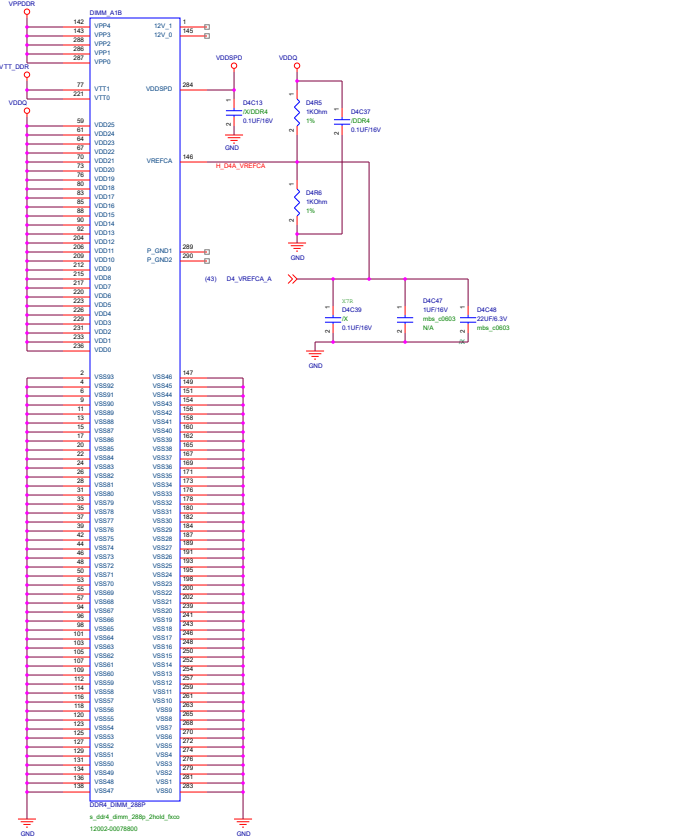
ASUS TeK Computer INC	Title :	DDR4 Channel A
	Engineer:	Morse_Peng
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 39 of 113	

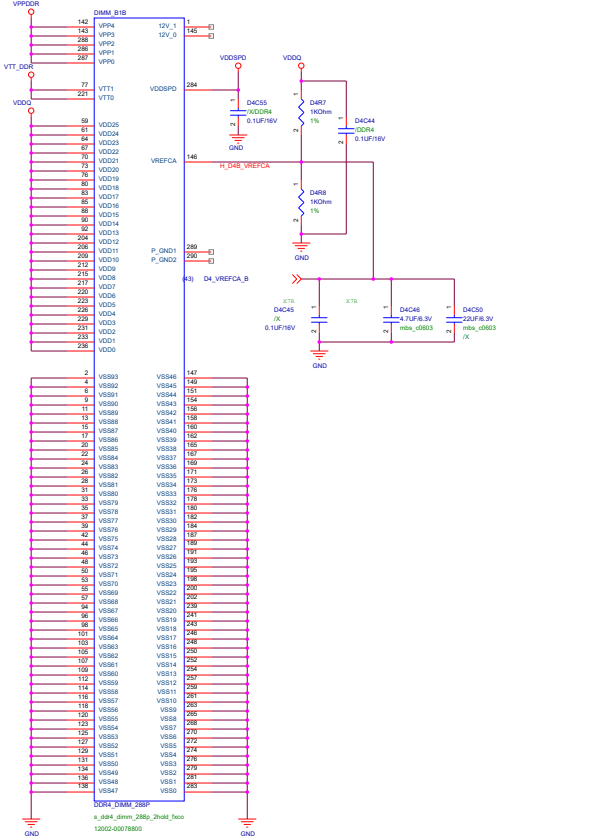


<Variant Name>

ASUS TeK Computer INC

Title :	DDR4 Channel B	
Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 40 of 113	

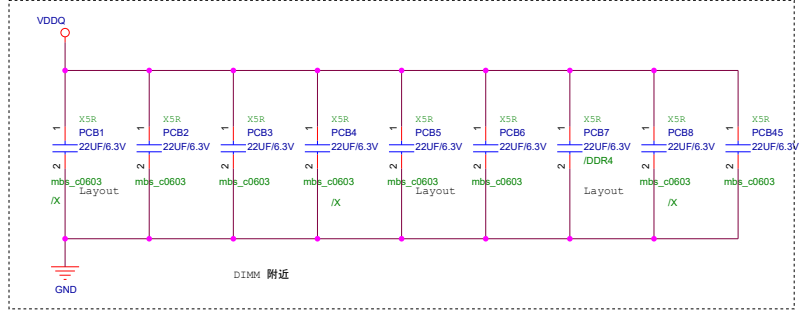


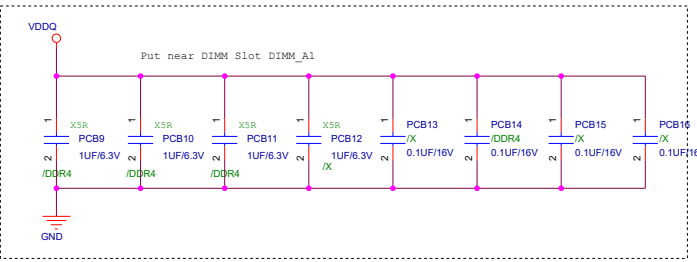


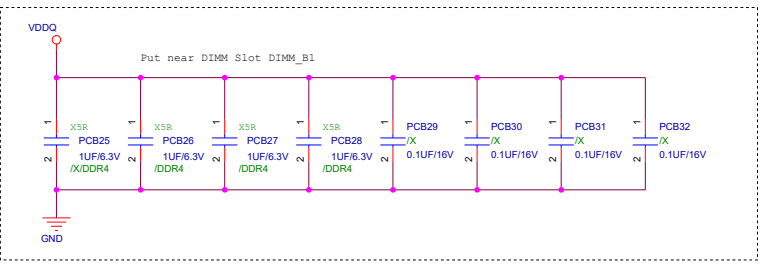
<variant_name>

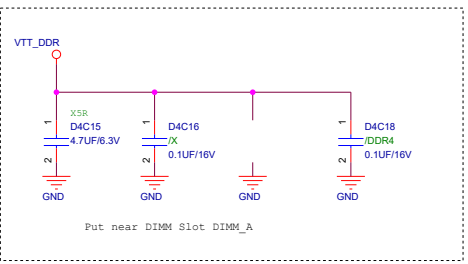
ASUS TeK Computer INC	Title : -12V	
	Engineer: IAN	
Size: A2	Project Name: Z87-PRO	Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 41 of 113	

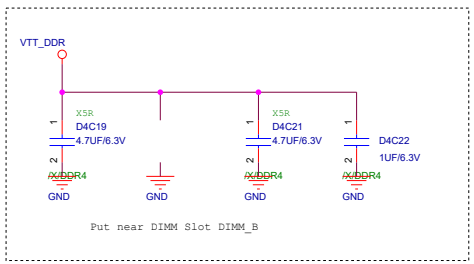
Layout to 0603

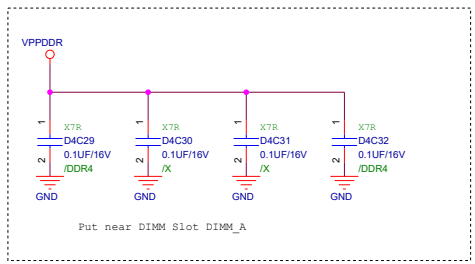


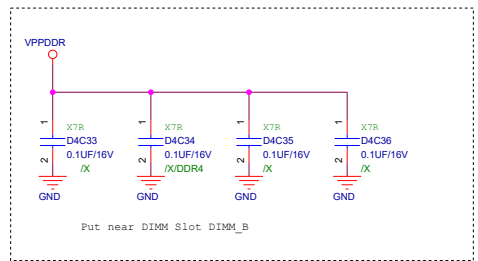












<Variant Name>

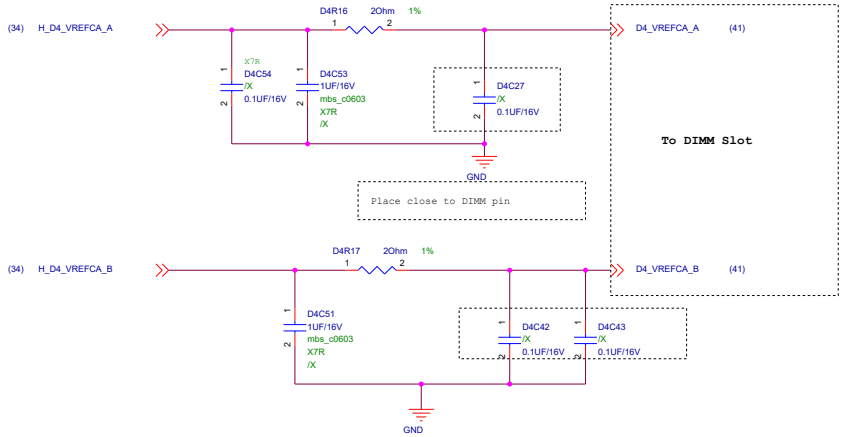
ASUSTek Computer Inc.	Title : DDR4 (Power CAPs)	
	Engineer: Miles Liu	
Size: A3	Project Name: X99_Deluxe	Rev: 1.00
Date: Monday, June 11, 2018	Sheet 42 of 113	

(6,39,40,48,63) S_SMBCLK_MAIN
(6,39,40,48,63) S_SMBDATA_MAIN

S_SMBCLK_DDR (6,39,40,48,63)
S_SMBDATA_DDR (6,39,40,48,63)

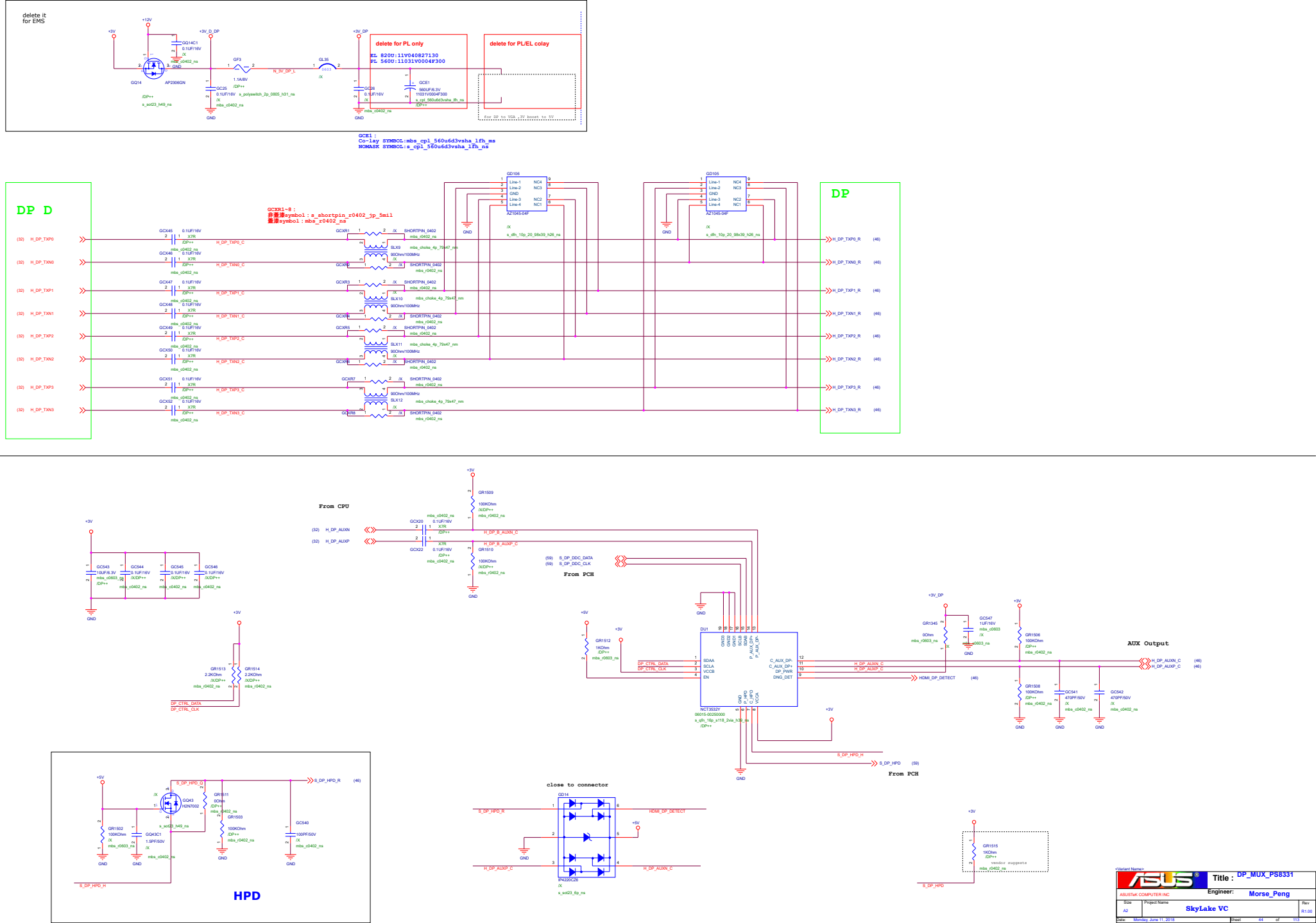
CPU DDR Vref

For CPU DDR Vref



<Variant Name>

ASUSTeK Computer Inc.	Title : DDR4 (SMBUS/SPD)	
	Engineer: Payton_Lin	
Size: A3	Project Name: X99 VC Rev1.00	Rev: 1.00
Date: Monday, June 11, 2018	Sheet 43 of 113	



Variant Name	
Title	DP_MUX_PS8331
Engineer	Morse_Peng
Company	ASUSTeK COMPUTER INC
Size	A2
Project Name	SkyLake VC
Rev	R1.00
Date	Monday, June 11, 2018
Sheet	44 of 113

delete it
for ESD

delete this page for HDMI/DVI colay

(32) H_HDMI_TXCN
(32) H_HDMI_TXCP
(32) H_HDMI_TXDN2
(32) H_HDMI_TXDP2
(32) H_HDMI_TXDN1
(32) H_HDMI_TXDP1
(32) H_HDMI_TXDN0
(32) H_HDMI_TXDP0

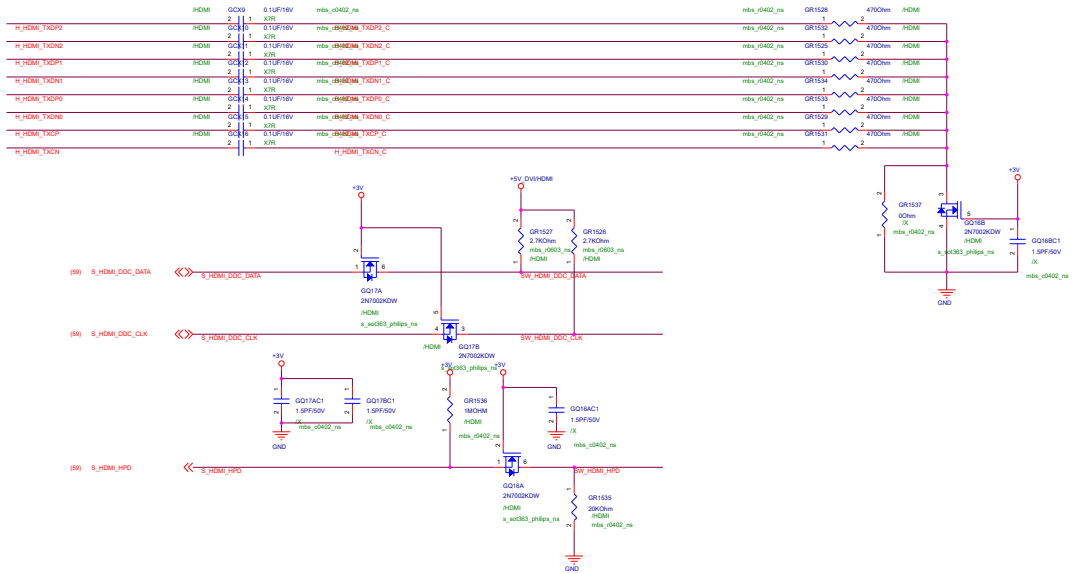
H_HDMI_TXCN
H_HDMI_TXCP
H_HDMI_TXDN2
H_HDMI_TXDP2
H_HDMI_TXDN1
H_HDMI_TXDP1
H_HDMI_TXDN0
H_HDMI_TXDP0

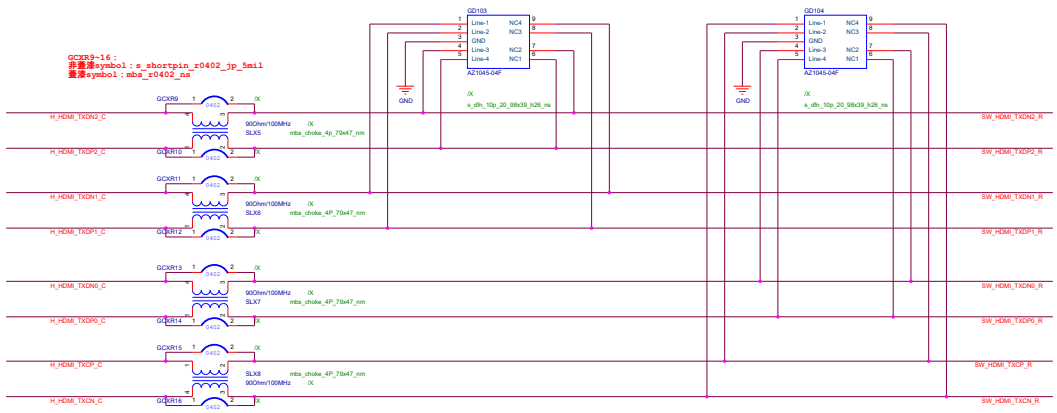
SW_HDMI_TXDP2_R
SW_HDMI_TXDN2_R
SW_HDMI_TXDP1_R
SW_HDMI_TXDN1_R
SW_HDMI_TXDP0_R
SW_HDMI_TXDN0_R
SW_HDMI_TXCP_R
SW_HDMI_TXCN_R

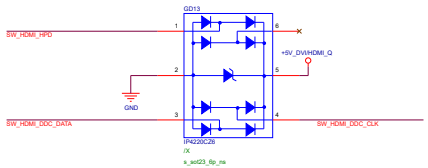
SW_HDMI_TXDP2_R (46)
SW_HDMI_TXDN2_R (46)
SW_HDMI_TXDP1_R (46)
SW_HDMI_TXDN1_R (46)
SW_HDMI_TXDP0_R (46)
SW_HDMI_TXDN0_R (46)
SW_HDMI_TXCP_R (46)
SW_HDMI_TXCN_R (46)

SW_HDMI_DDC_CLK
SW_HDMI_DDC_DATA
SW_HDMI_HPD

SW_HDMI_DDC_CLK (46)
SW_HDMI_DDC_DATA (46)
SW_HDMI_HPD (46)



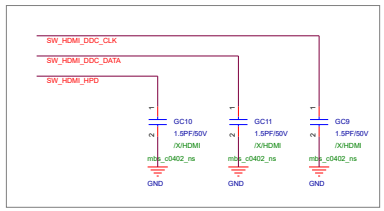


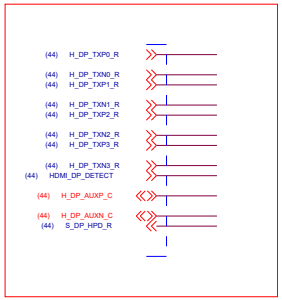


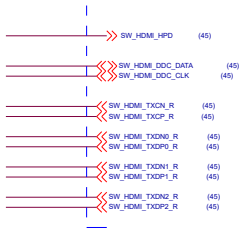
ESD

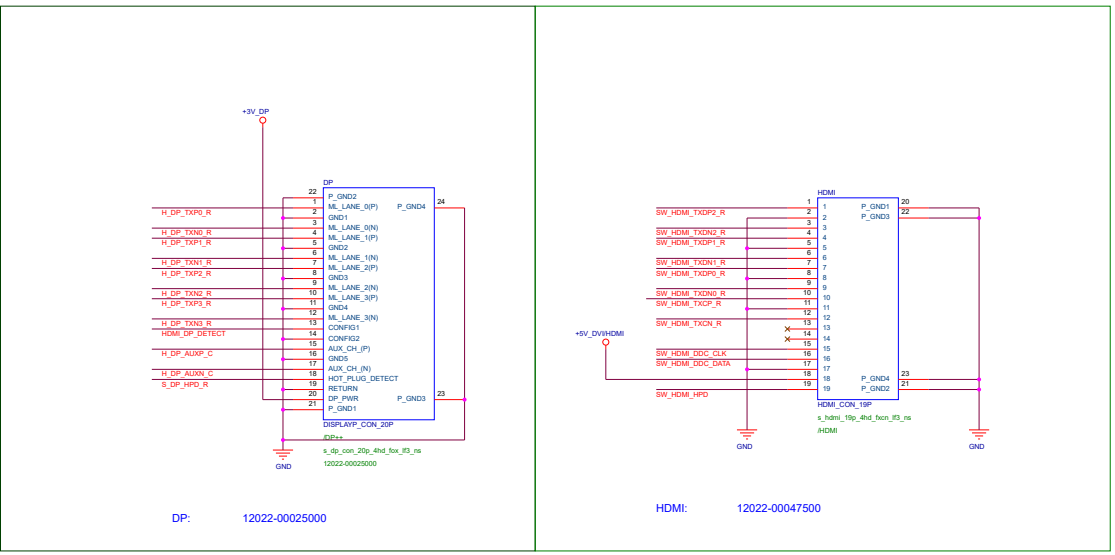
<Variant Name>

ASUSTeK Computer Inc.	Title : HDMI	
	Engineer: alex_zhou	
Size: A2	Project Name: Standard Circuit	Rev: 0.01A
Date: Monday, June 11, 2018	Sheet: 45 of 113	









DP: 12022-00025000

HDMI: 12022-00047500

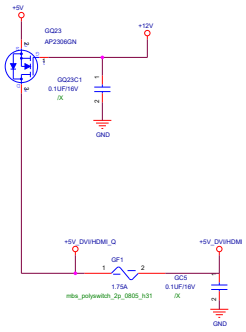
<Variant Name>

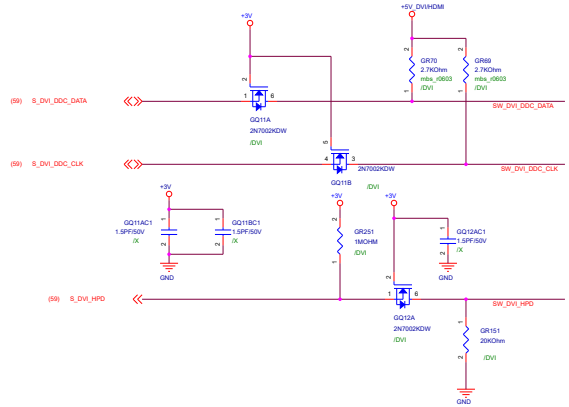
ASUSTek COMPUTER INC.	Title : BACK IO_VGA/DVI/HDMI/DP	
	Engineer: KENNY_CHEN	
Size: A2	Project Name: Z87-PRO	Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 46 of 113	

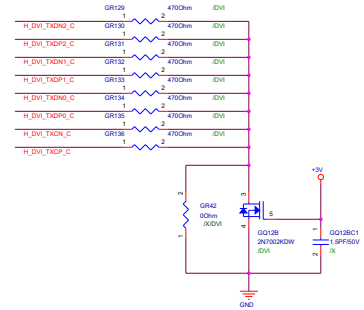
delete it
for EMS

POWER for HDMI & DVI

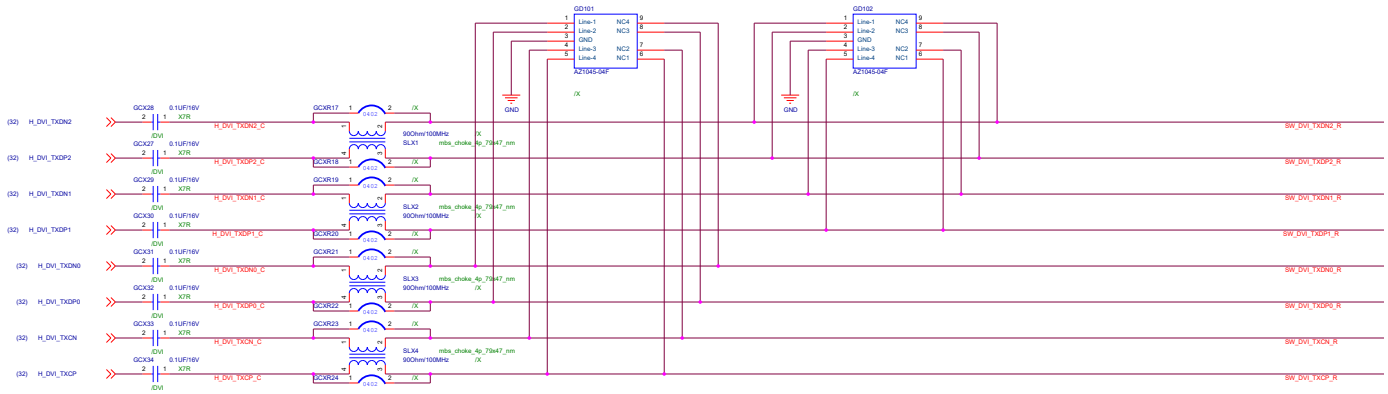
If only HDMI,this power must still need



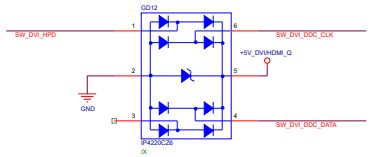


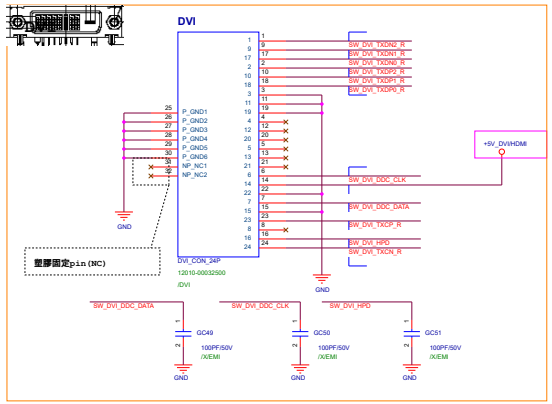


Passive/Active Devices					
Max Capacitance (Backdrive I Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	$R1/R2_t$	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Ron/Cout	NA	NA	Ω/pF	3ohm/10pF	NA



close to connector





<Variant Name>

ASUSTek COMPUTER INC.

Title : DVI REDUCED LEV-SHFT

Engineer: Morse_Peng

Size	Project Name	Rev
A2	SkyLake VC	R1.00

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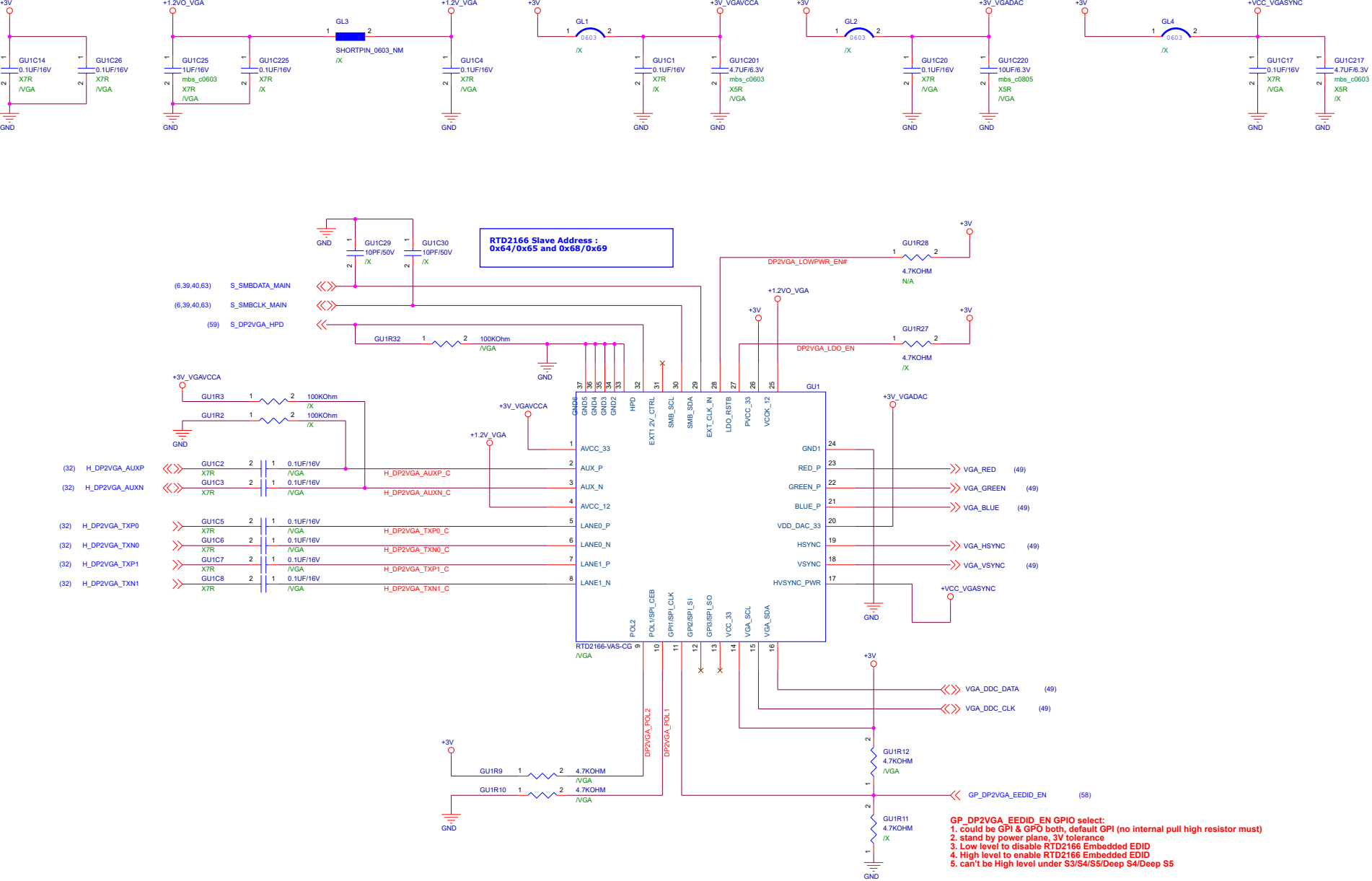


STANDARD CIRCUIT	
XUMB	OTHER
SZ_DP2VGA_1.0B	

LOGO_HD_DEMO_OTHER
/X

BOM	need DP2VGA	no DP2VGA
/VGA	mount	unmount
/X	unmount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : RTD2166

Engineer: SZ Design IP

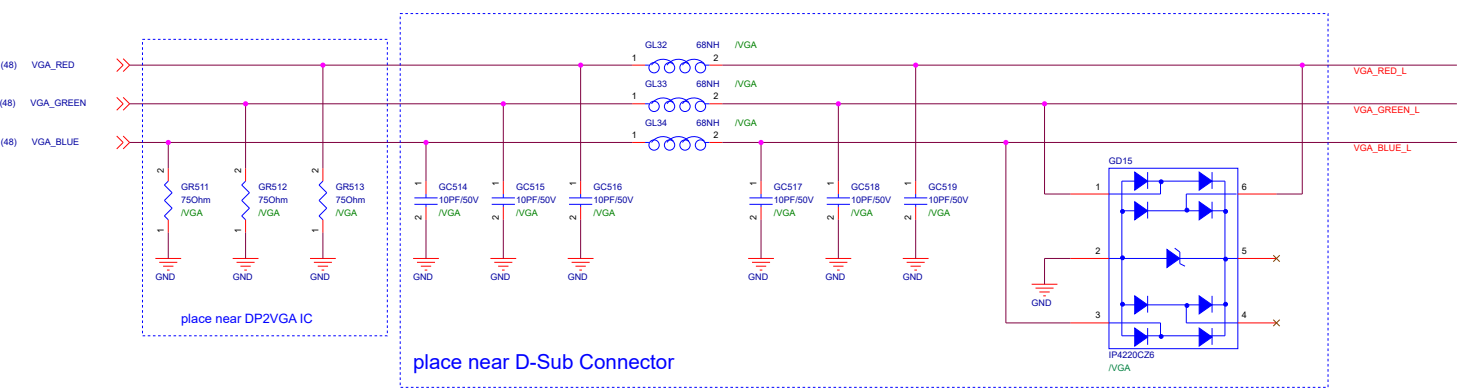
Size	Project Name	Rev
A3	DP2VGA Demo Circuit	0.0

Date: Monday, June 11, 2018 Sheet 48 of 113

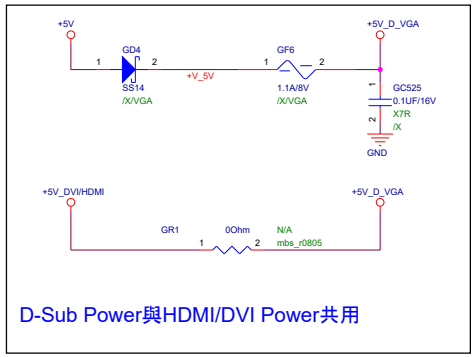
D-Sub Connector Circuit for RTD2166

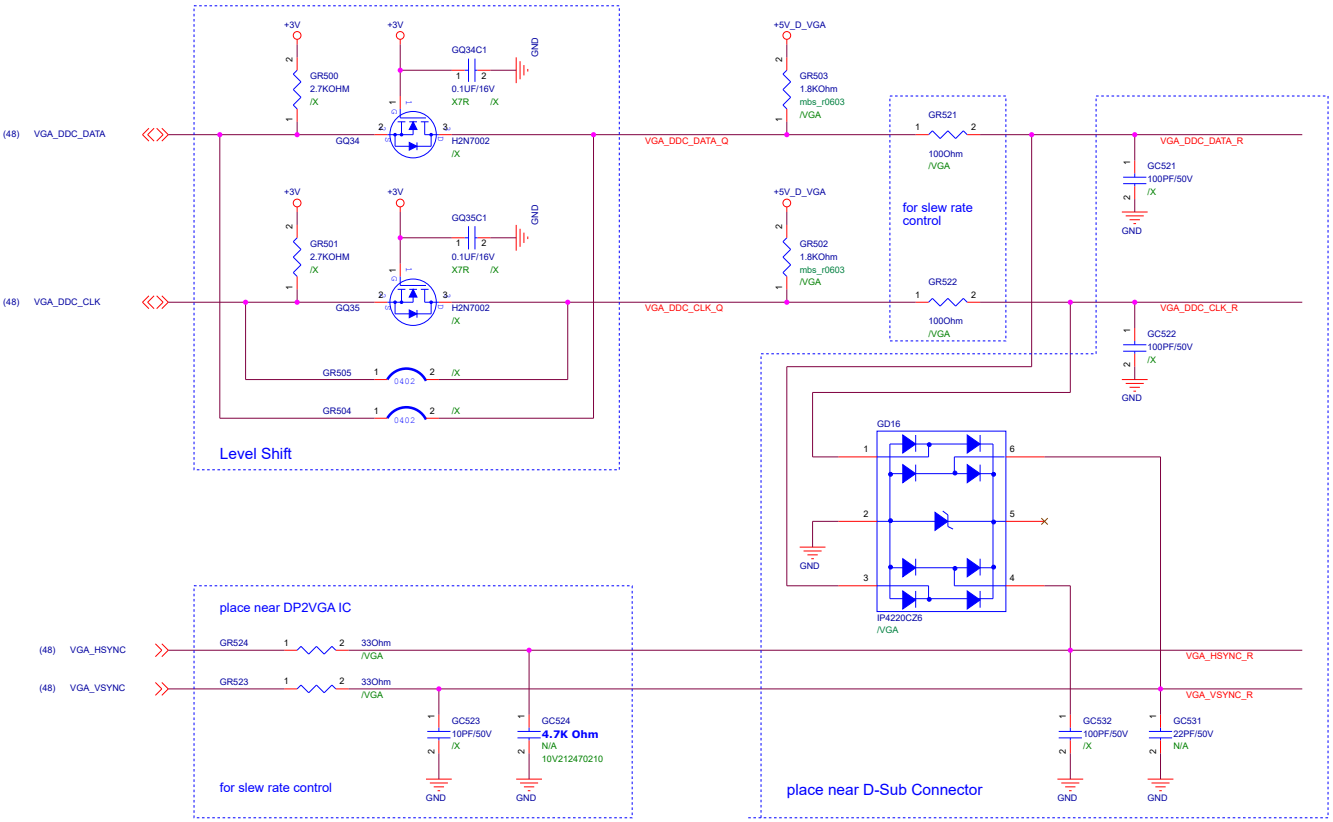
A. Choose D-Sub Connector Type by Project

B. Modify Part Number of D-Sub Connector by Color



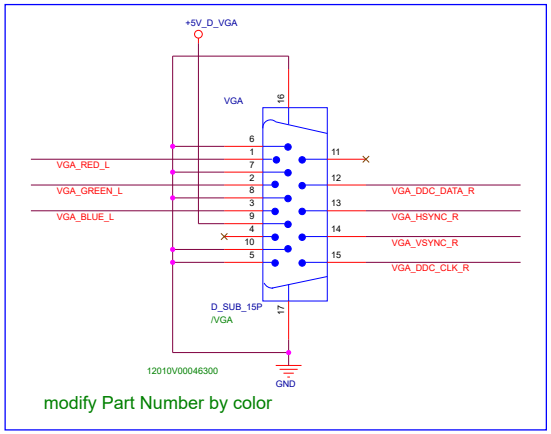
delete it for EMS





A.2

High Rise D-Sub Connector



<Variant Name>

ASUSTEK COMPUTER INC

Title : RTD2166 D-Sub

Engineer: SZ Design IP

Size: A3

Project Name: DP2VGA Demo Circuit

Rev: 0.0

Date: Monday, June 11, 2018

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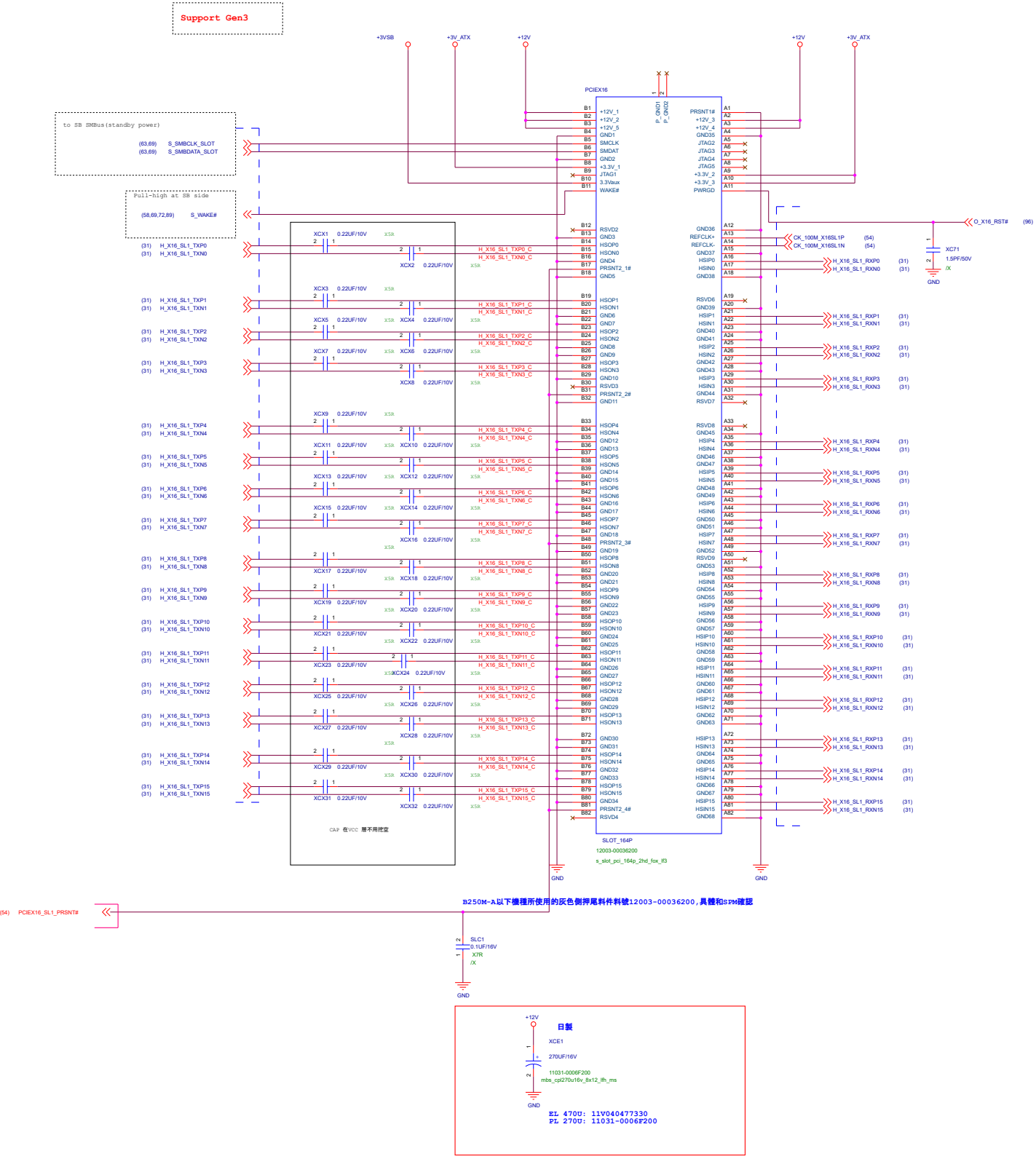
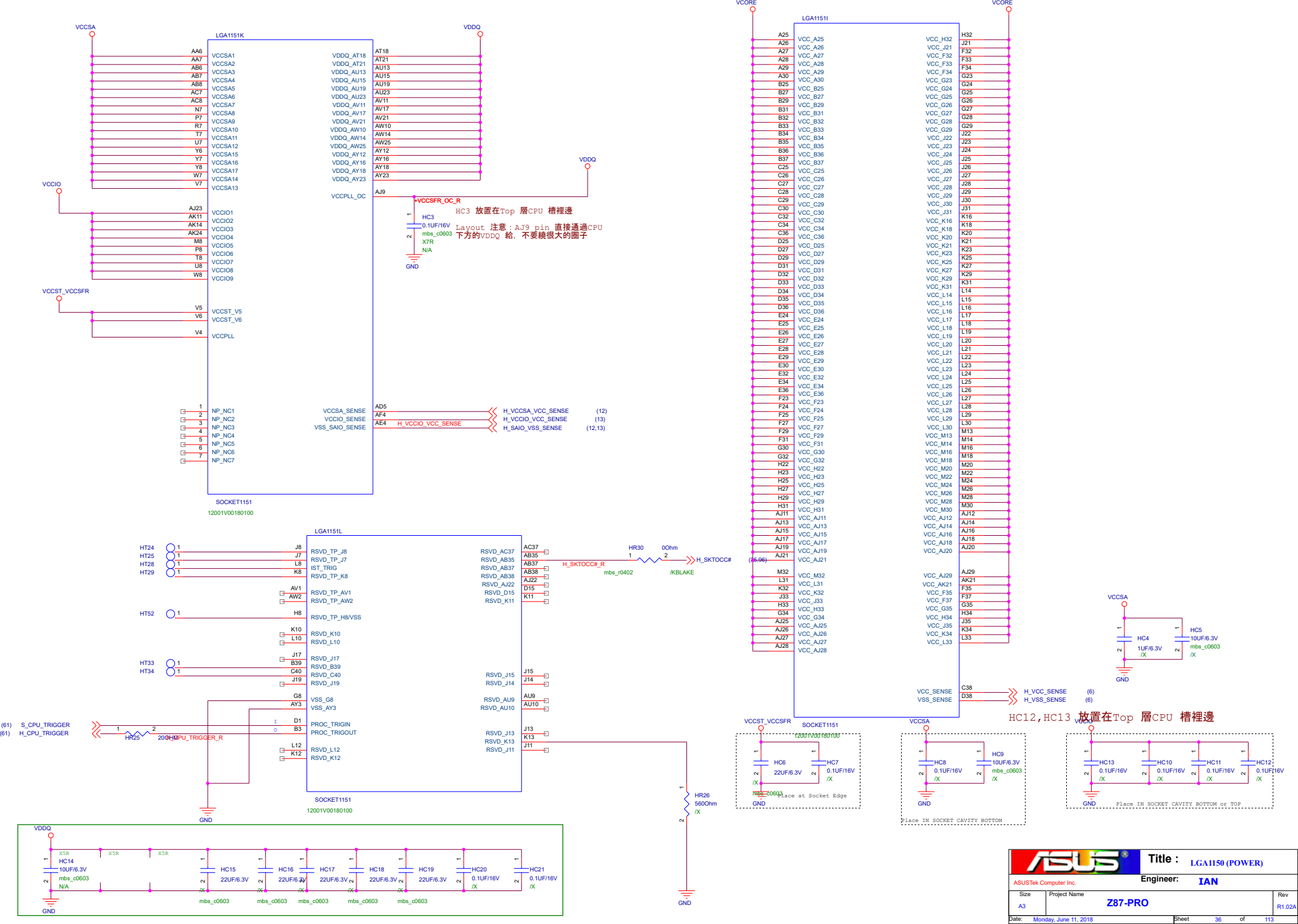
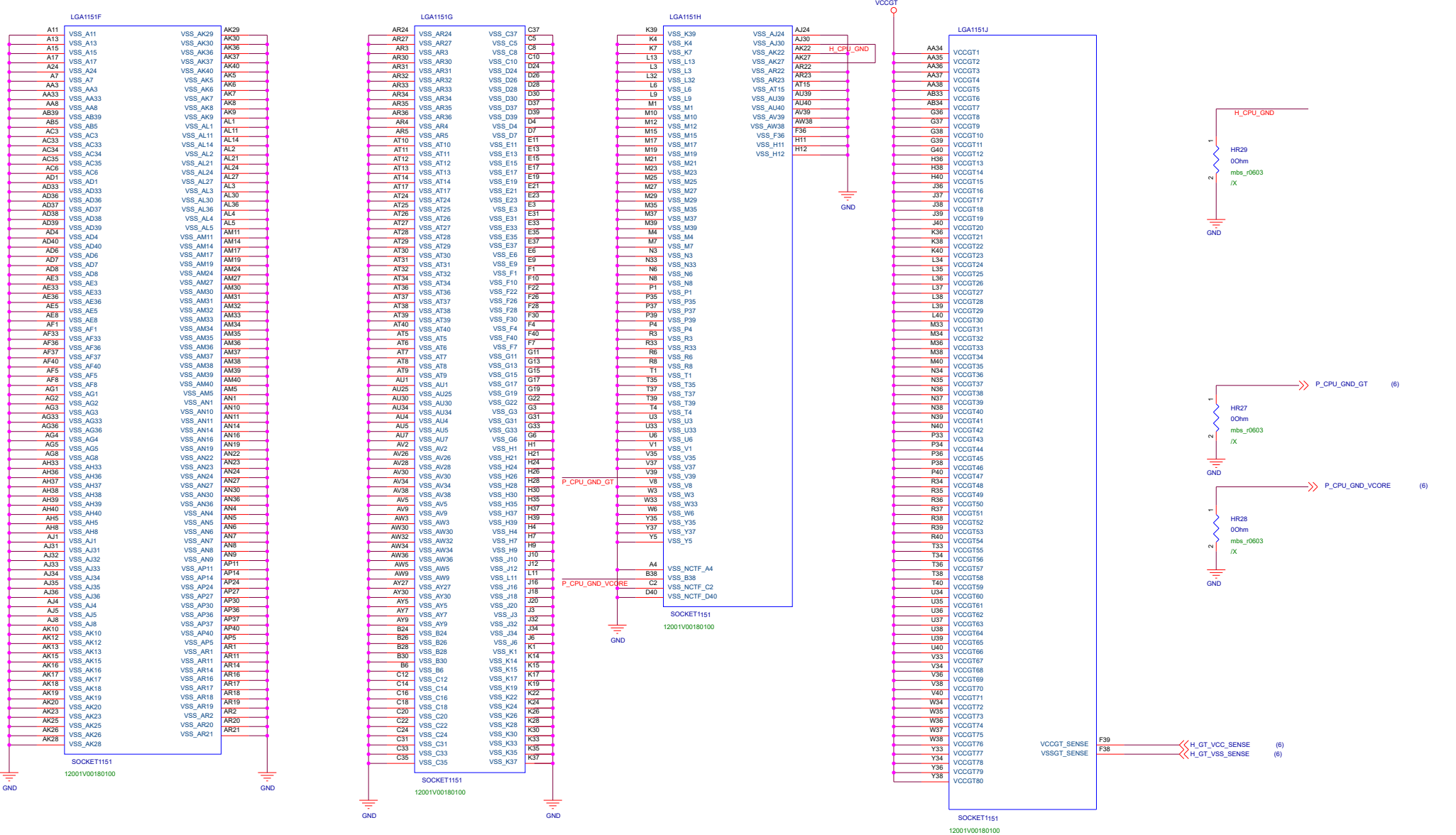


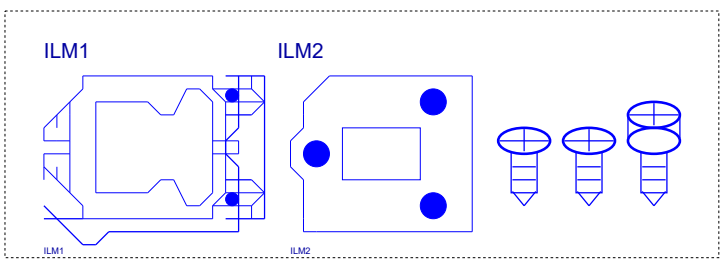
<Variant Name>

ASUSTek COMPUTER INC.	Title :	PCIEX16_1(NAVY BLUE)
	Engineer:	IAN
Size: A2	Project Name: Z87-PRO	Rev: R1.02A
Date: Monday, June 11, 2018	Sheet: 51 of 113	

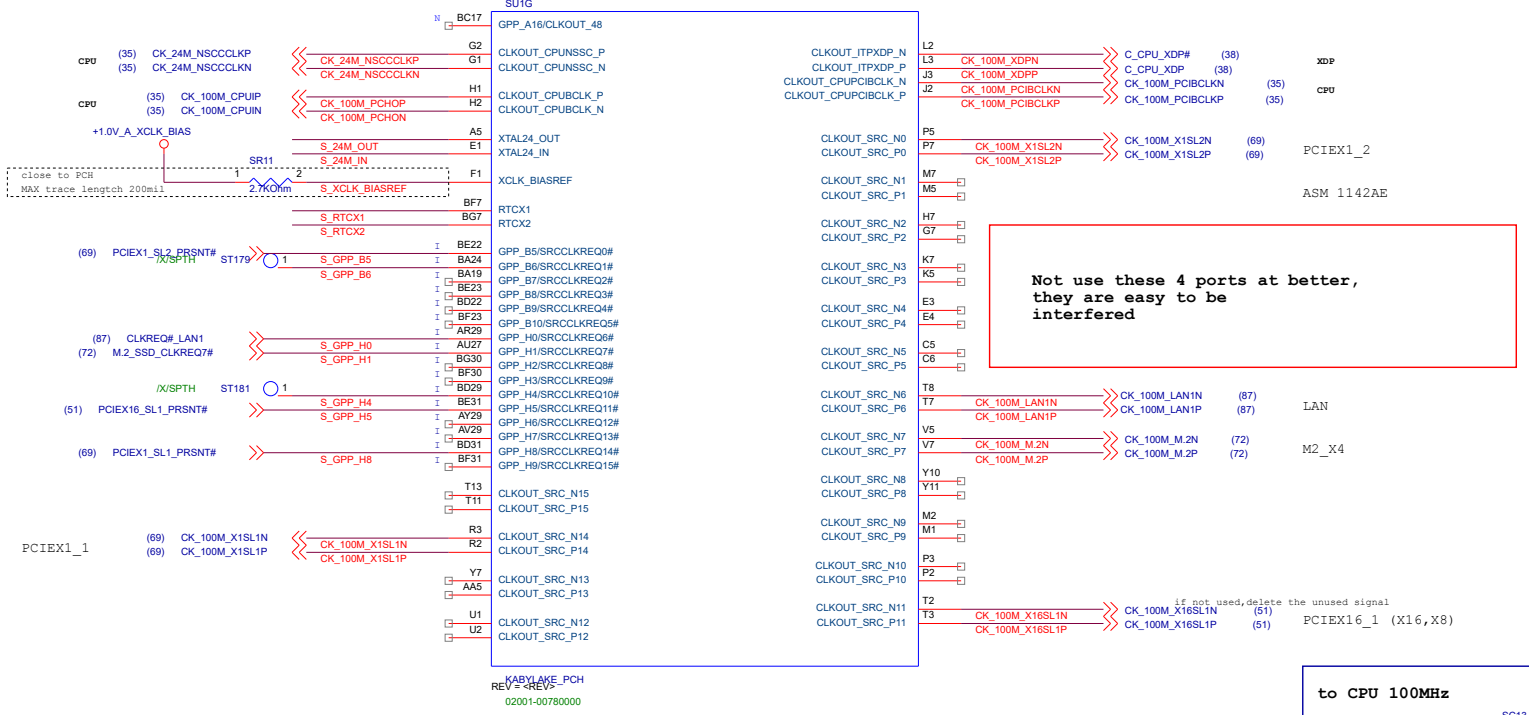


ASUSTek Computer Inc.	Title :	LGA1150 (POWER)	
	Engineer:	IAN	
Size: A3	Project Name: Z87-PRO		Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 36 of 113		



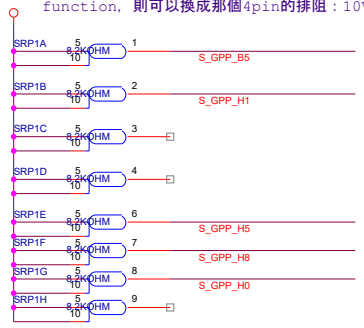


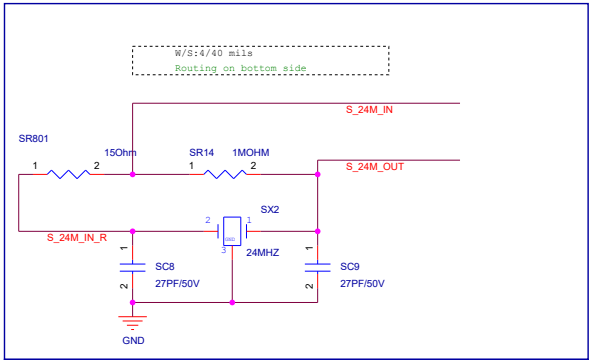
ASUSTek Computer Inc.	Title :	LGA1151 (GND)
	Engineer:	Morse_Peng
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 37 of 113	

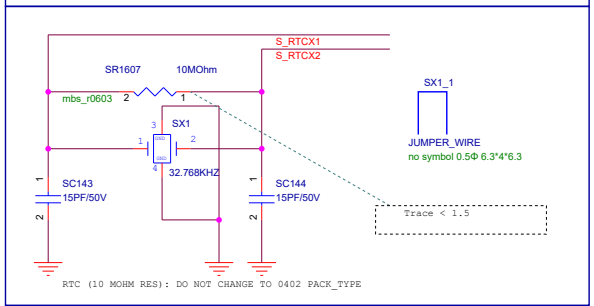


+3V

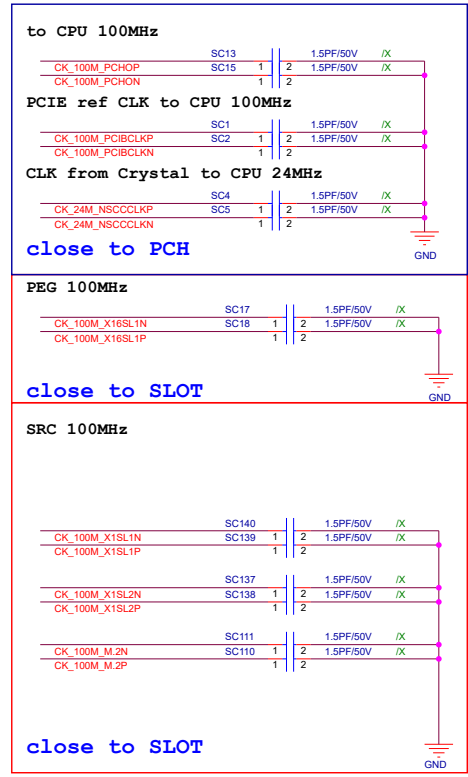
@:各個案子不同，如果那麼多的CLK_REQ function，則可以換成那個4pin的排阻：10V253820240







@:如果沒有CLK，旁邊的電容需移除



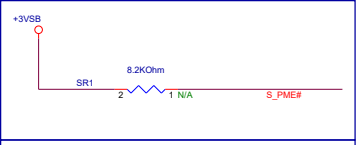
ASUSTek Computer Inc.

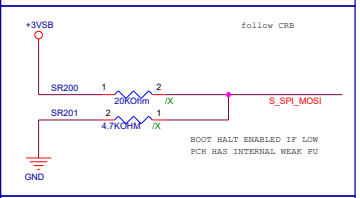
Title : PCH (CLOCK)

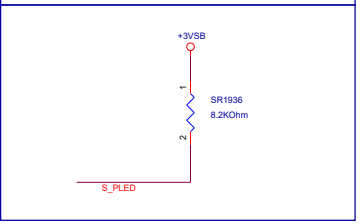
Engineer: Bing-jie_Wang

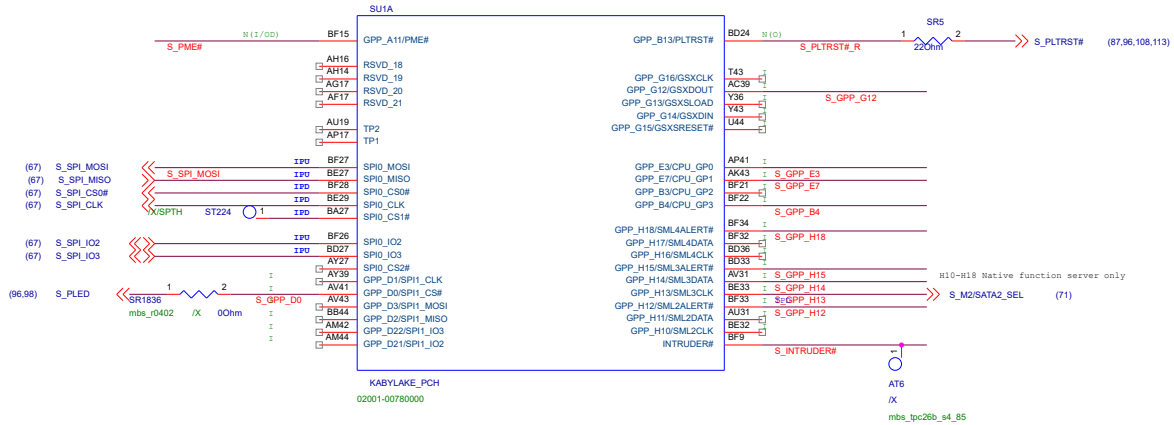
Size	Project Name	Rev
Custom	Skylake Chipset DEMO	R1.00

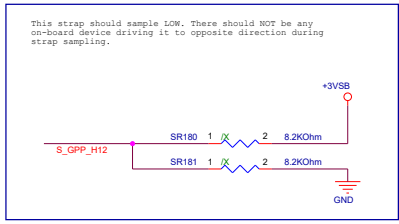
Date: Monday, June 11, 2018 Sheet 54 of 113

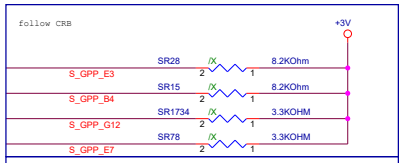


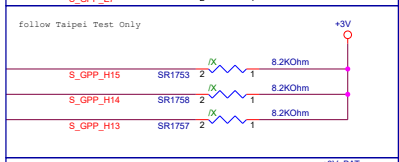


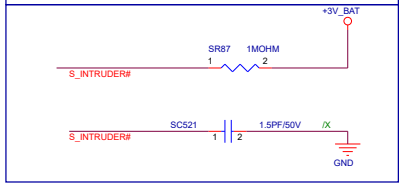


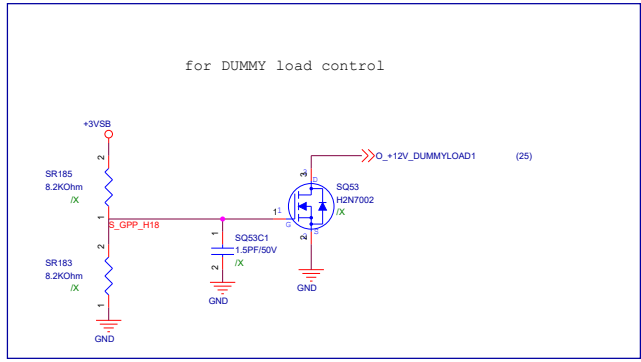




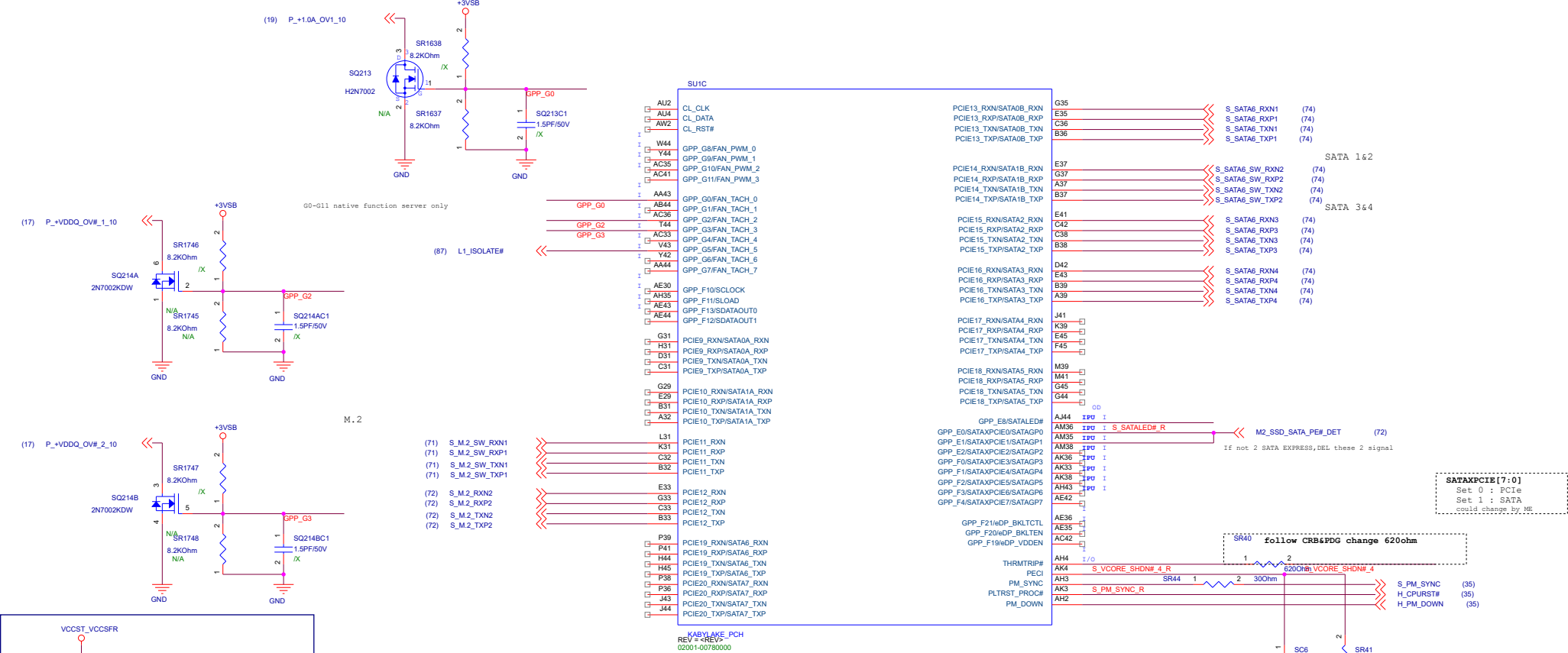








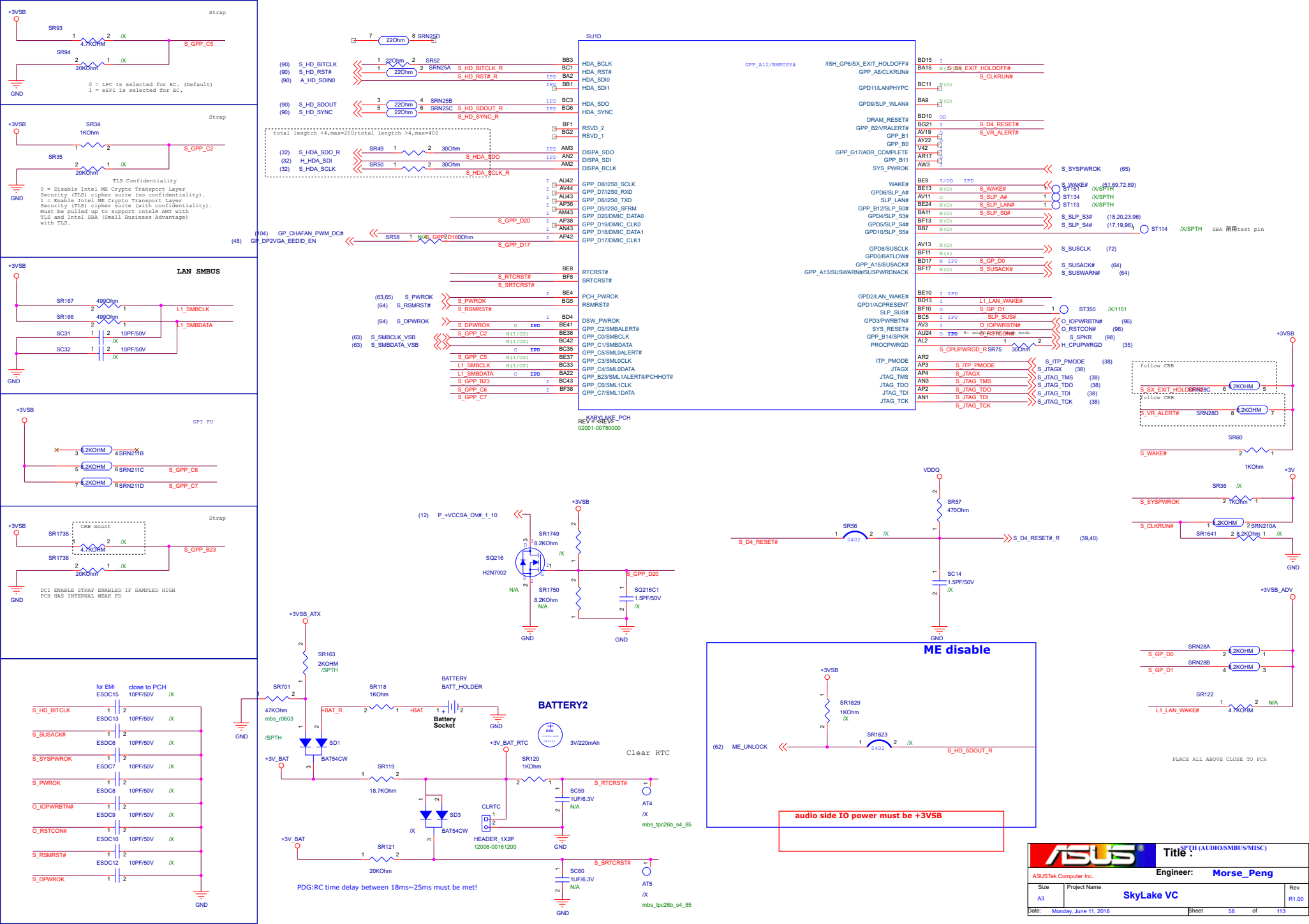
ASUSTek Computer Inc.	Title :	SPTH (PCI/SPI)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.02A
Date: Monday, June 11, 2018	Sheet 55 of 113		

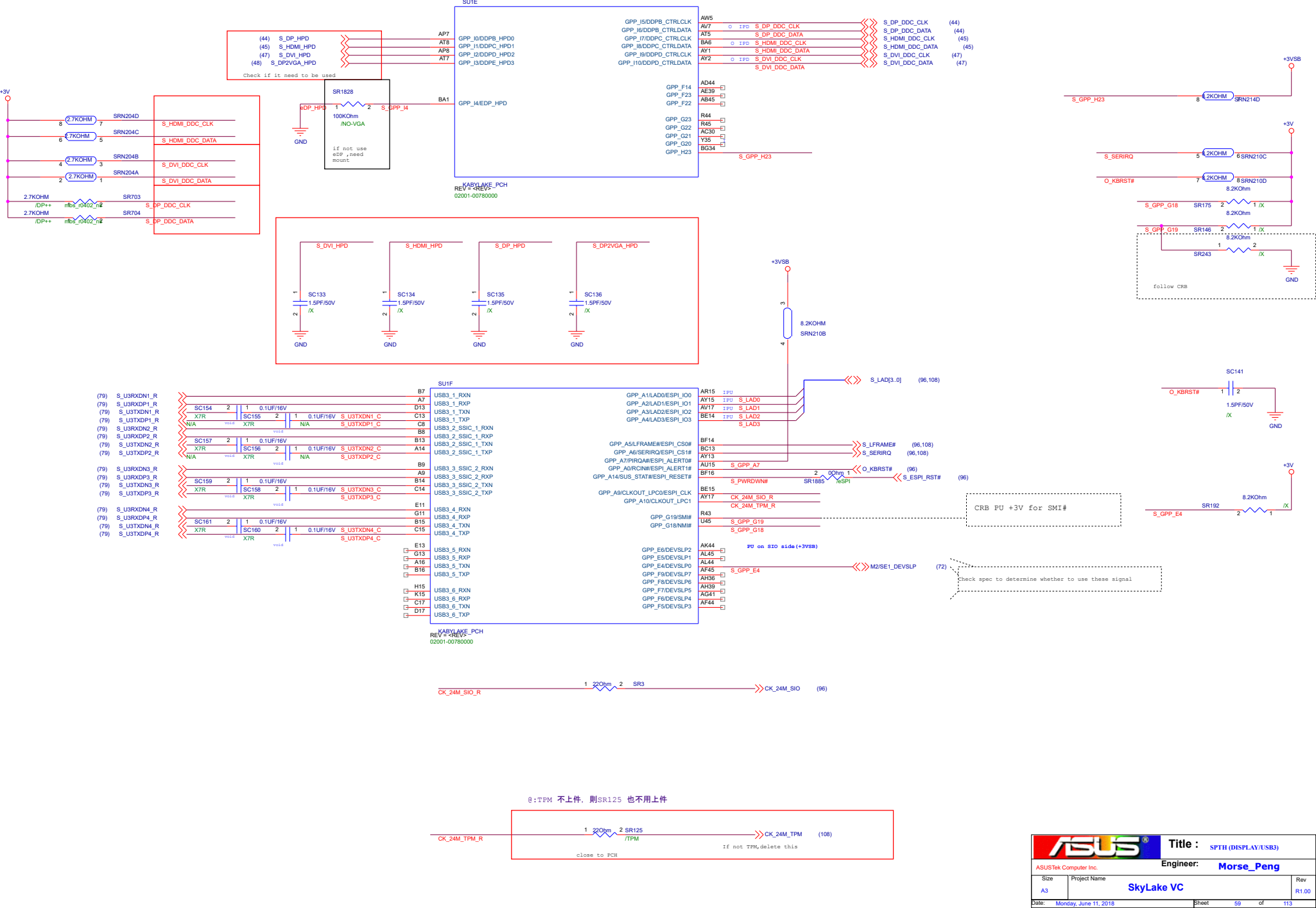


Note:

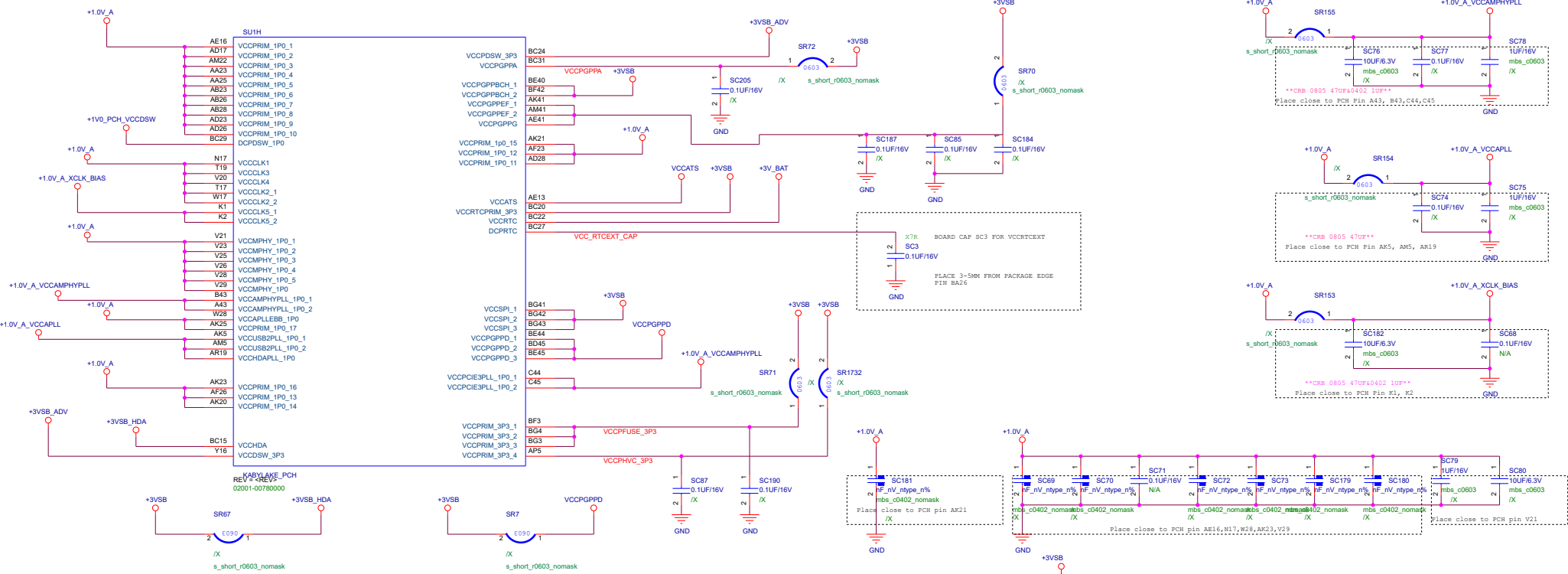
1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions – the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).

ASUSTek Computer Inc.	Title : SPTH (HOST/FAN/SATA)	
	Engineer: Morse_Peng	
Size: Custom	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 57 of 113	


Strap
SR93
4.7KOHM
S_GPP_C5
SR94
20KOHM
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
GND
Strap
SR34
1KOhm
S_GPP_C2
SR35
20KOHm
TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
Must be pulled up to support Intel® AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
LAN SMBUS
SR167
SR166
SC31
SC32
10PF/50V
L1_SMBCLK
L1_SMBDATA
GPI PU
6.2KOHM
SRN211B
SRN211C
SRN211D
S_GPP_C6
S_GPP_C7
Strap
CRB mount
SR1735
SR1736
S_GPP_B23
DCI ENABLE STRAP ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD
for EMI
close to PCH
ESDC15
ESDC13
ESDC6
ESDC7
ESDC8
ESDC9
ESDC10
ESDC12
S_HD_BITCLK
S_SUSACK#
S_SYSPWROK
S_PWROK
O_IOPWRBTN#
O_RSTCON#
S_RSMRST#
S_DPWROK
SU1D
KABYLAKE_PCH
REV = <REV>
02001-00780000
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD_2
RSVD_1
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
/ISH_GP6/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
S_SYSPWROK
S_WAKE#
S_SUSCLK
S_SUSACK#
S_SUSWARN#
S_D4_RESET#
S_VR_ALERT#
L1_LAN_WAKE#
S_GP_D1
S_SLP_S0#
S_SLP_S3#
S_SLP_S4#
S_CLKRUN#
S_SX_EXIT_HOLDOFF#
S_GP_D0
S_SPKR
H_CPUPWRGD
S_ITP_PMODE
S_JTAGX
S_JTAG_TMS
S_JTAG_TDO
S_JTAG_TDI
S_JTAG_TCK
S_CPUPWRGD_R
S_SRTCRST#
S_RSMRST#
S_PWROK
S_DPWROK
S_GPP_C2
S_GPP_C5
S_GPP_B23
S_GPP_C6
S_GPP_C7
S_GPP_D20
S_GPP_D17
S_HDA_SDO_R
S_HDA_SDI
S_HDA_SCLK
S_HDA_SDOUT_R
S_HDA_SYNC_R
S_HDA_BITCLK_R
S_HDA_RST#_R
total length <4,max=200;total length >4,max=400
GP_CHAFAN_PWM_DC#
GP_DP2VGA_EEDID_EN
S_SHD_BITCLK
S_SHD_RST#
A_HD_SDIN0
S_SHD_SDOUT
S_SHD_SYNC
ST114
SBA 所用test pin
follow CRB
SR60
1KOhm
SR36
S_SYSPWROK
S_CLKRUN#
SR1641
8.2KOhm
SRN210A
+3VSB_ADV
SRN28A
SRN28B
SR122
4.7KOHM
PLACE ALL ABOVE CLOSE TO PCH
P_+VCCSA_OV#_1_10
SR1749
8.2KOhm
SQ216
H2N7002
SR1750
SQ216C1
1.5PF/50V
SR57
470Ohm
SR56
SC14
+3VSB_ATX
SR163
2KOHM
/SPTH
SR701
47KOhm
mbs_r0603
SR118
1KOhm
BATTERY
BATT_HOLDER
Battery Socket
BATTERY2
3V/220mAh
SD1
BAT54CW
SR119
18.7KOhm
SR120
1KOhm
SC59
1UF/6.3V
SD3
CLRTC
HEADER_1X2P
12006-00161200
SR121
20KOhm
SC60
AT4
AT5
mbs_tpc26b_s4_85
Clear RTC
PDG:RC time delay between 18ms~25ms must be met!
ME disable
SR1829
SR1623
ME_UNLOCK
audio side IO power must be +3VSB
Title : SPTH (AUDIO/SMBUS/MISC)
Engineer: Morse_Peng
ASUSTek Computer Inc.
Size A3
Project Name SkyLake VC
Rev R1.00
Date: Monday, June 11, 2018
Sheet 58 of 113



ASUSTek Computer Inc.	Title :	SPTH (DISPLAY/USB3)	
	Engineer:	Morse_Peng	
Size: A3	Project Name: SkyLake VC		Rev: R1.00
Date: Monday, June 11, 2018	Sheet 59 of 113		



GROUP D POWER
LPT-H : 3.3V (FOR INTERPOSER) CRB
SPT-H : 1.8V

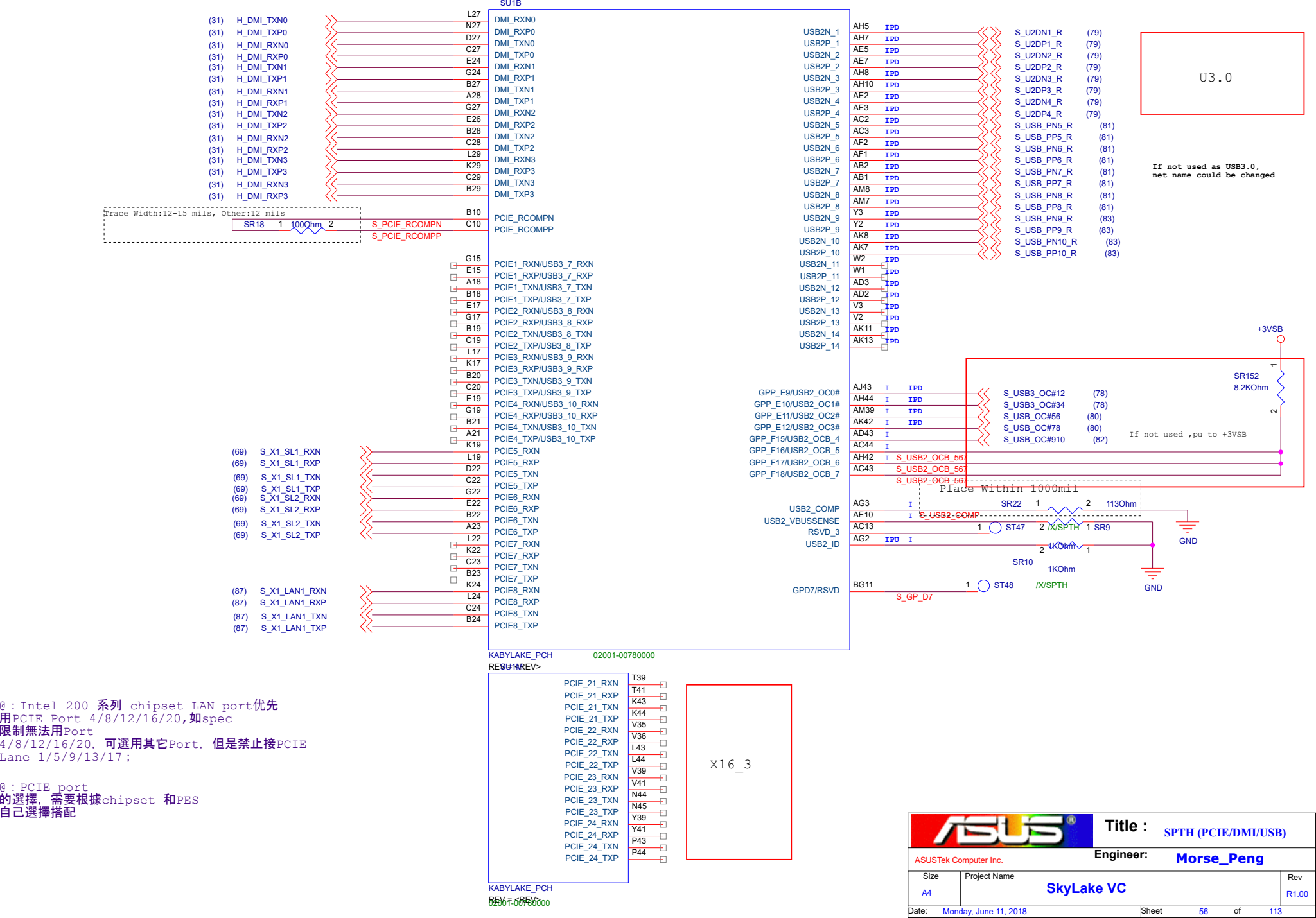
注意PCH GPIO D Group power plane

PCH-H SPEC : GPP A~G 1.8V or 3.3V

PCH-H SPEC : GPP I only 3.3V

Deep Sleep Well Group (GPD) only 3.3V

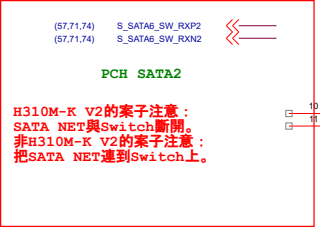
ASUSTek Computer Inc.	Title : SPTH (POWER)	
	Engineer: Morse_Peng	
Size: A3	Project Name: SkyLake VC	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 60 of 113	

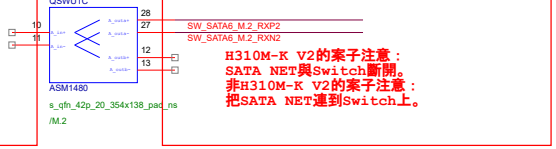


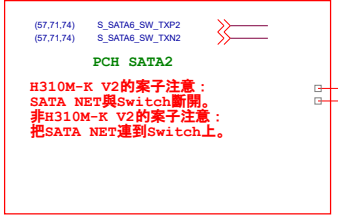
@：Intel 200 系列 chipset LAN port优先用PCIE Port 4/8/12/16/20,如spec限制無法用Port 4/8/12/16/20，可選用其它Port，但是禁止接PCIE Lane 1/5/9/13/17；

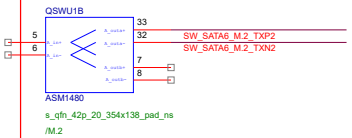
@：PCIE port的選擇，需要根據chipset 和PES自己選擇搭配

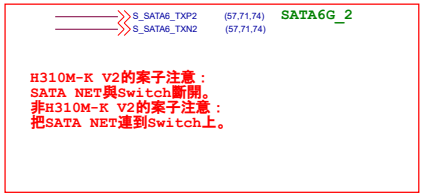
ASUSTek Computer Inc.	Title : SPTH (PCIE/DMI/USB)		
	Engineer: Morse_Peng		
Size A4	Project Name SkyLake VC		Rev R1.00
Date: Monday, June 11, 2018	Sheet 56 of 113		

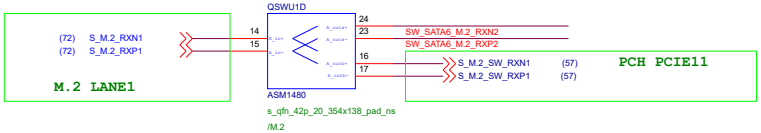


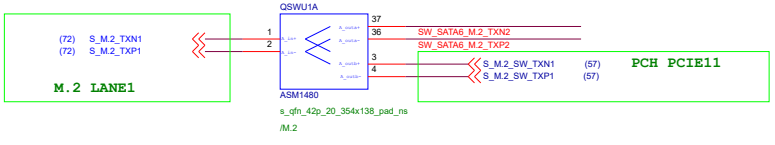


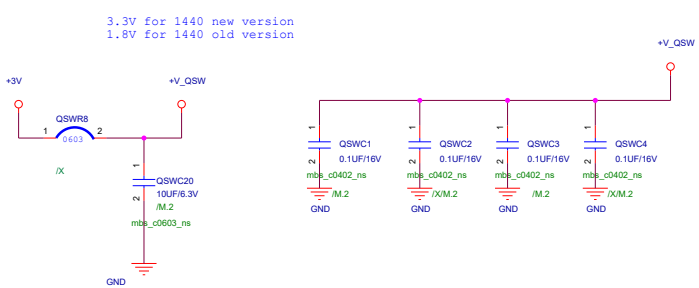


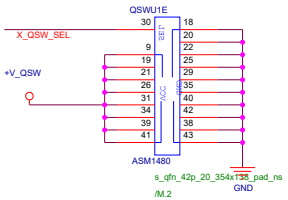








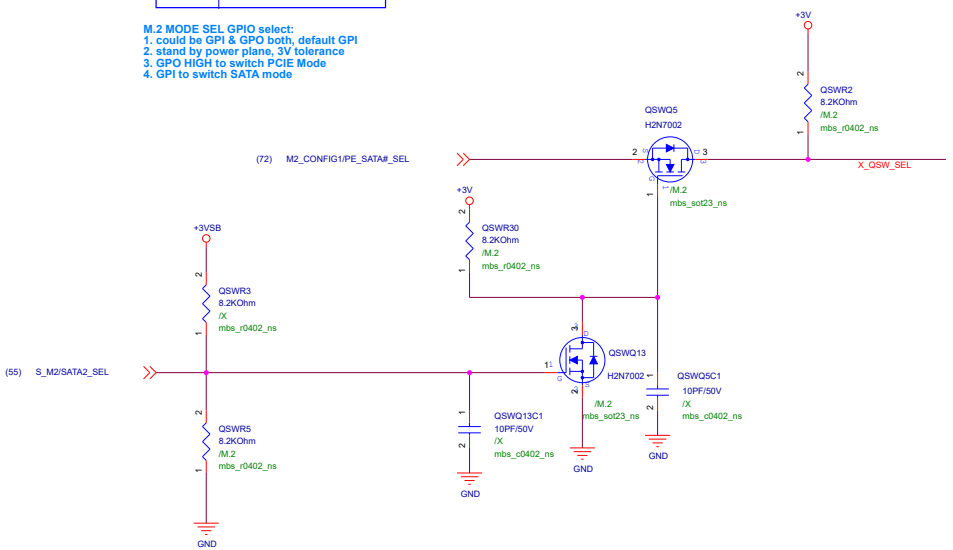


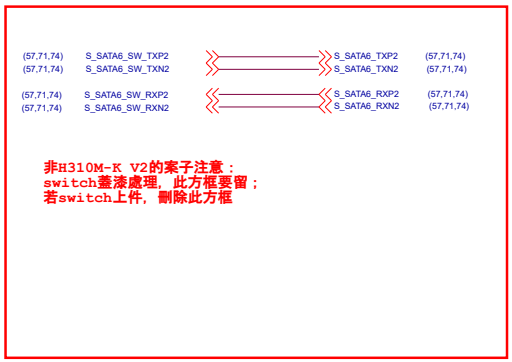


X_QSW_SEL	Function	
L	N_in to N_outa	M.2 SATA Mode
H	N_in to N_outb	M.2 PCIE Mode

M.2 MODE SEL	
0	M.2 SATA Mode
1	M.2 PCIE Mode

M.2 MODE SEL GPIO select:
1. could be GPI & GPO both, default GPI
2. stand by power plane, 3V tolerance
3. GPO HIGH to switch PCIE Mode
4. GPI to switch SATA mode





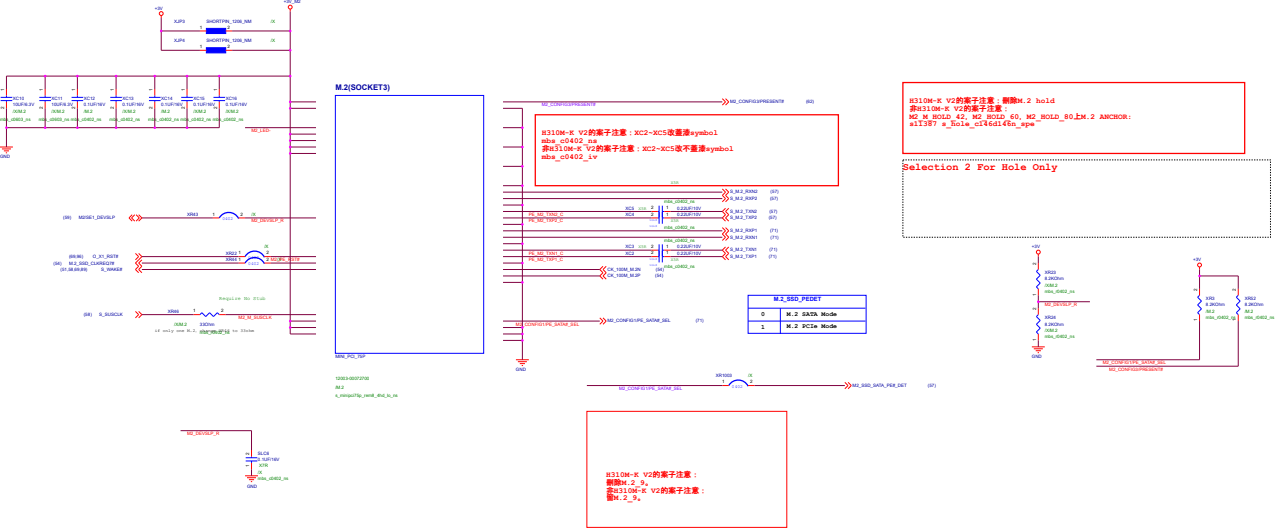
<variant_name>

ASUSTek Computer Inc.

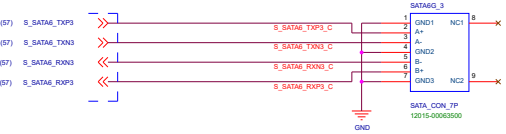
Title :

Engineer:

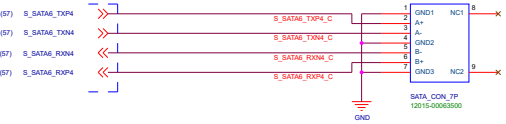
Size	Project Name	Rev
Date:	Sheet 71 of 113	

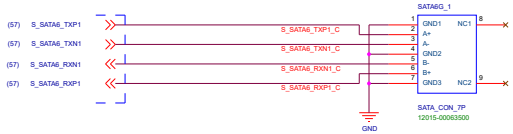

M.2(SOCKET3)
H310M-K V2的案子注意：XC2~XC5改電源symbol
mbs_c0402_ns
改H310M-K V2的案子注意：XC2~XC5改不要源symbol
mbs_c0402_iv
H310M-K V2的案子注意：刪除M.2 hold
改H310M-K V2的案子注意：
M2_M_HOLD_42, M2_HOLD_60, M2_HOLD_80上M.2 ANCHOR:
all387_a_hole_c24ed145n_mpa
Selection 2 For Hole Only
M.2_SSD_PEDET
0 M.2 SATA Mode
1 M.2 PCIe Mode
H310M-K V2的案子注意：
刪除M.2_9。
改H310M-K V2的案子注意：
留M.2_9。

note：台北和蘇州機種去掉電容直連后在QTC測試PASS，經leaders討論后決定去除電容變為直連

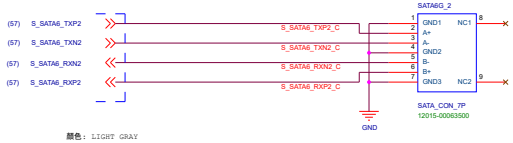


180度connector





180度connector

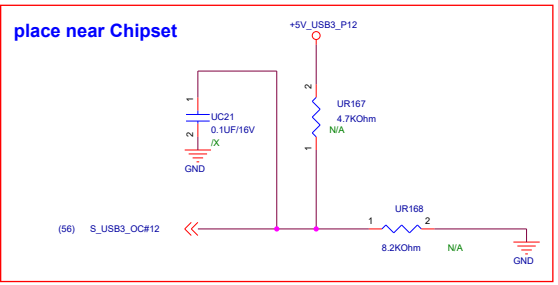


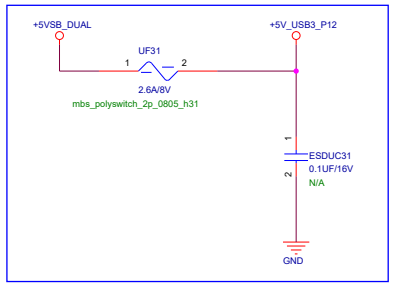
顏色：LIGHT GRAY

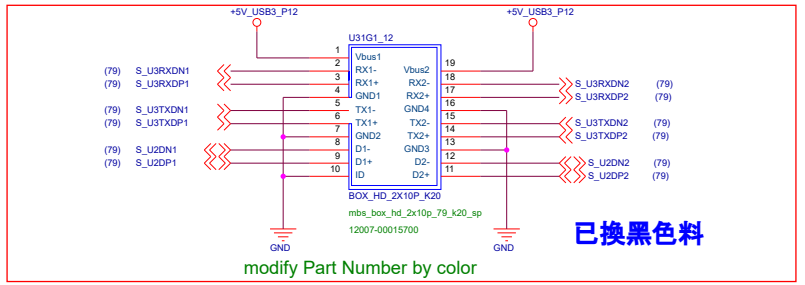
<Variant Name>

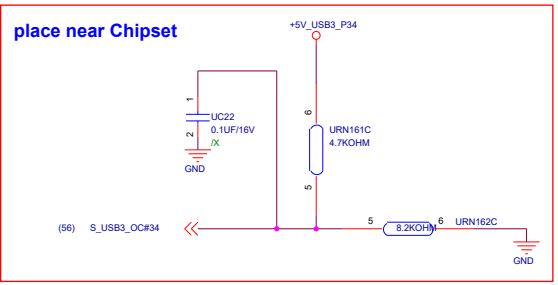
ASUSTek COMPUTER INC.	Title : SATA6G_123456(CHIPSET)	
	Engineer: KENNY_CHEN	
Size: A2	Project Name: Z87-PRO	Rev: 1.00
Date: Monday, June 11, 2018	Sheet 74 of 113	

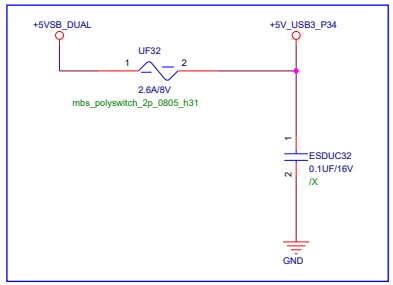
OC# circuit for Intel

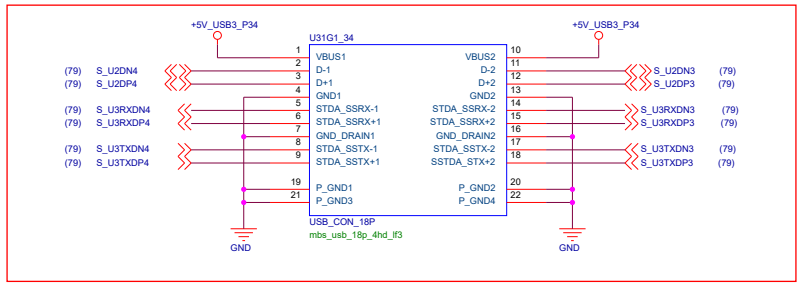












<Variant Name>

ASUSTEK COMPUTER INC

Title : USB3 Port

Engineer: Kell_Huang

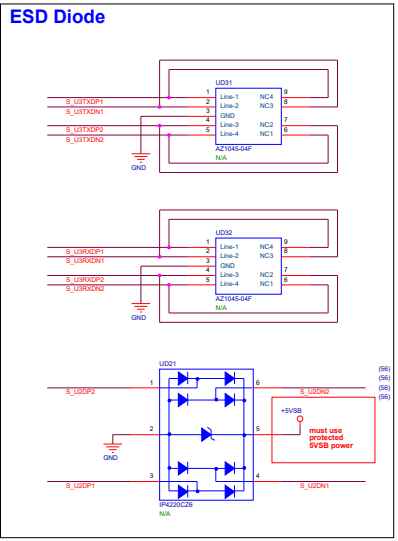
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

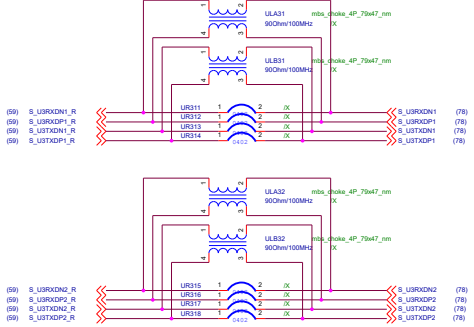
Date: Monday, June 11, 2018 Sheet 78 of 113

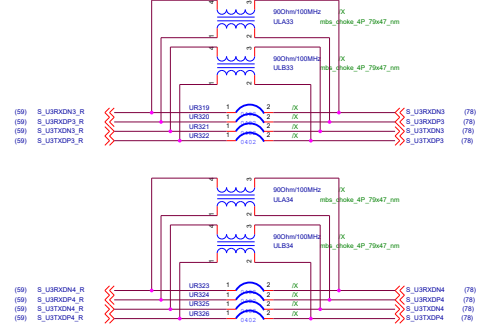
Port 12

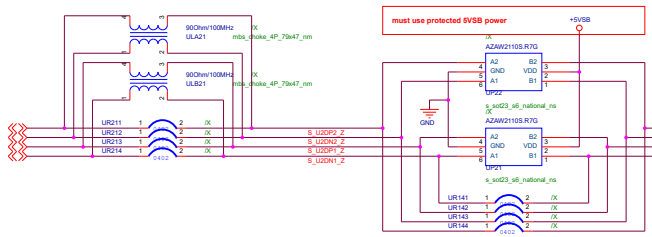
Delete it for EMS

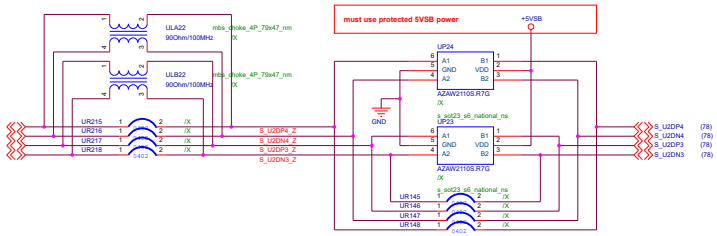
ESD Diode

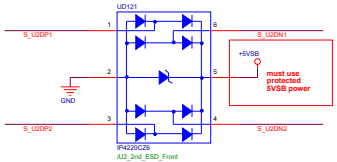


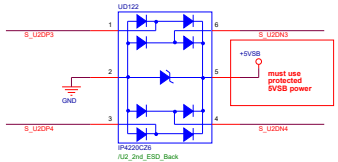






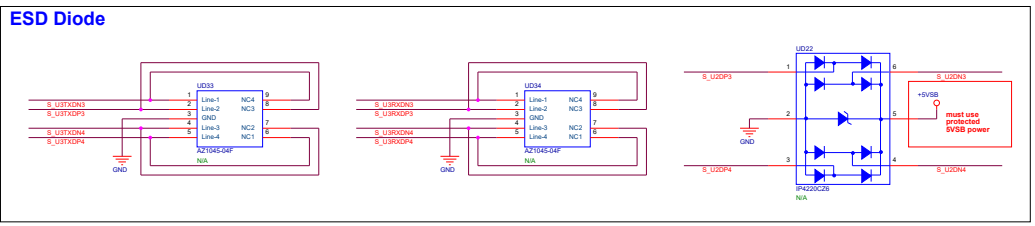






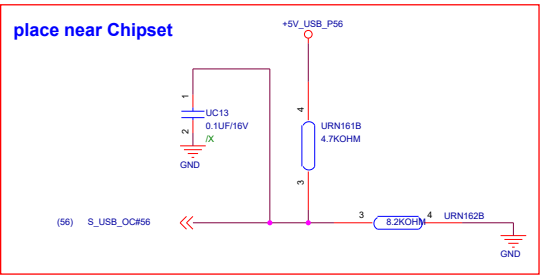
Delete it for EMS

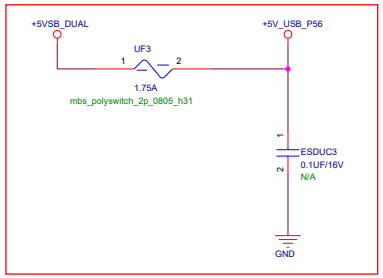
ESD Diode



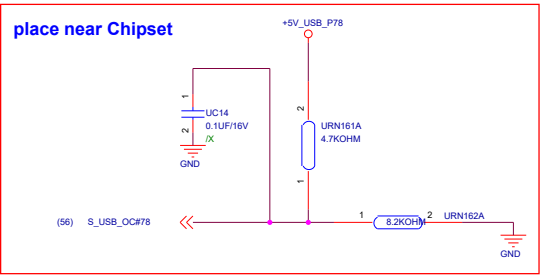
Port 34

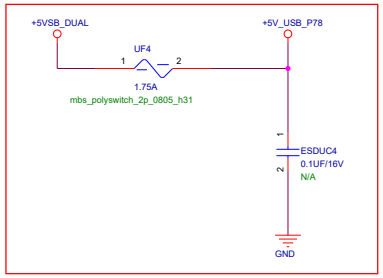
OC# circuit for Intel

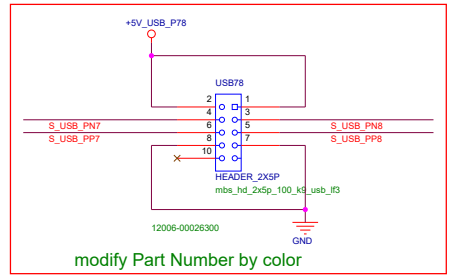




(81,88) S_USB_PN5
(81,88) S_USB_PP5
(81,88) S_USB_PN6
(81,88) S_USB_PP6







(81) S_USB_PN7
(81) S_USB_PP7
(81) S_USB_PN8
(81) S_USB_PP8

<Variant Name>

ASUSTEK COMPUTER INC

Title : USB2 Port

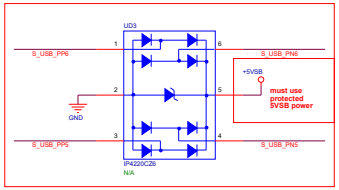
Engineer: Kell_Huang

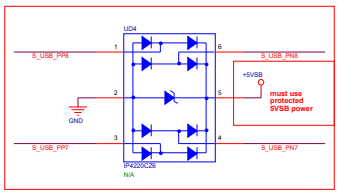
Size	Project Name	Rev
A3	Chipset USB Demo Circuit	0.0

Date: Monday, June 11, 2018 Sheet 80 of 113

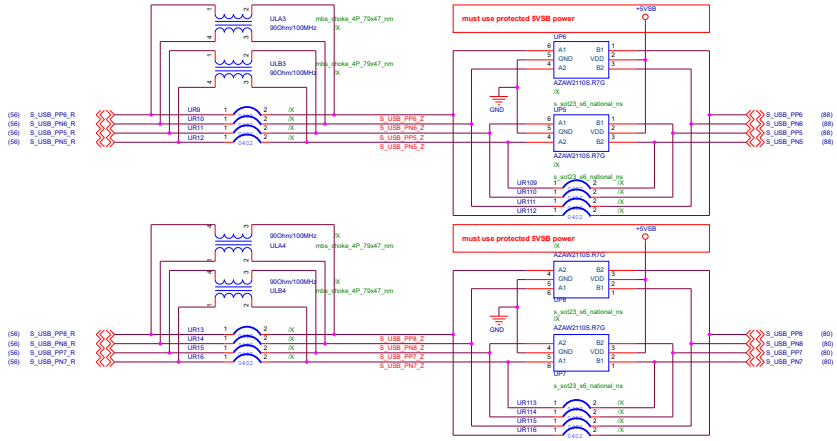
Delete it for EMS

ESD Diode



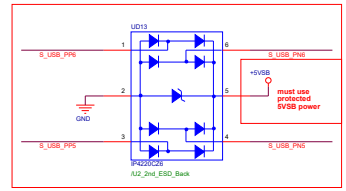


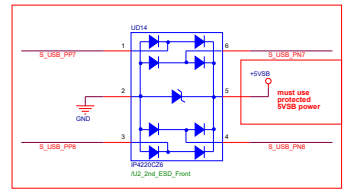
Reserve USB Guard with short pin



Delete it for EMS

2nd ESD Diode

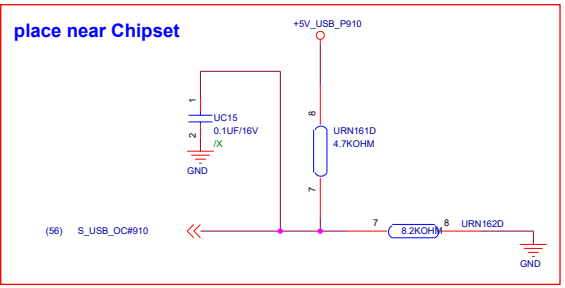


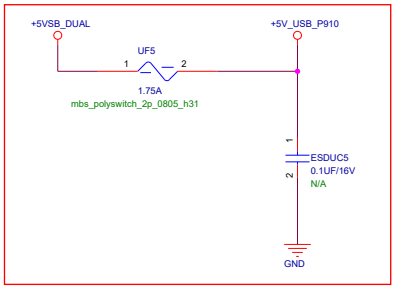


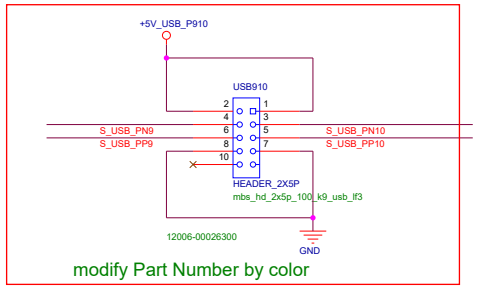
<variant_name>

ASUSTEK COMPUTER INC	Title :	USB2 Port	
	Engineer:	Kell_Huang	
Size: A2	Project Name:	Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet	81 of 113	

OC# circuit for Intel







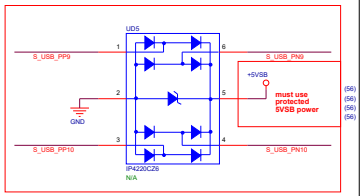
(83) S_USB_PN10
(83) S_USB_PP10
(83) S_USB_PN9
(83) S_USB_PP9

<Variant Name>

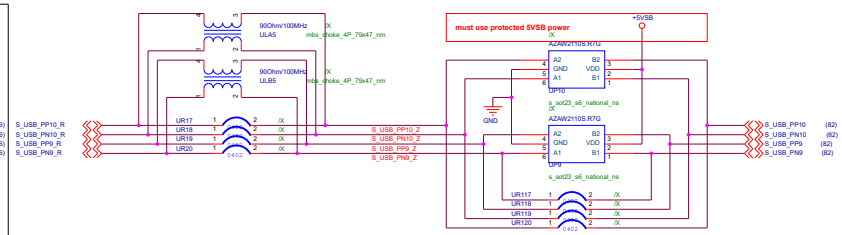
ASUSTEK COMPUTER INC	Title : USB2 Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 82 of 113	

Delete it for EMS

ESD Diode

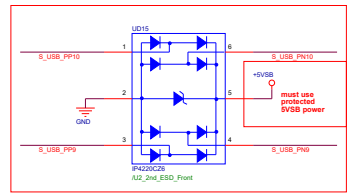


Reserve USB Guard with short pin



Delete it for EMS

2nd ESD Diode



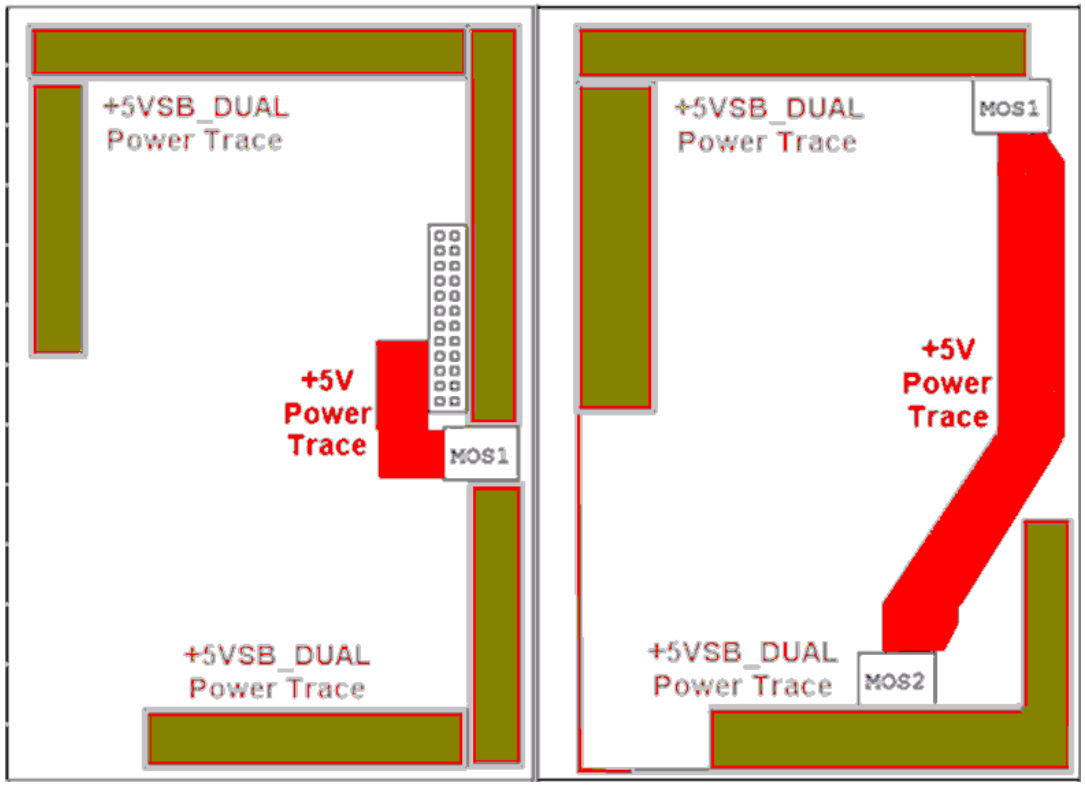
<Variant Name>

ASUSTEK COMPUTER INC	Title : USB2 Port	
	Engineer: Kell_Huang	
Size: A2	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 83 of 113	

+5VSB_DUAL current:
DIMM*4=7A, DIMM*2=5A, DIMM not generate from +5VSB_DUAL=0A
USB 2.0=0.5A/port
USB 3.x=1A/port
USB Type C=3A/port
if +5VSB_DUAL current (DIMM+USB 2.0 Port+USB 3.x Port) > 15A, add UQ706

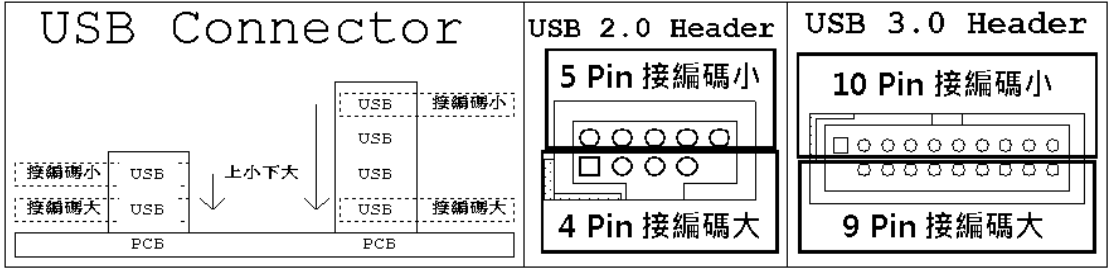
N-MOS	Max Current
Power PAK MOS 4 mohm	15A
Power PAK MOS 6 mohm	13A
DPAK MOS 9 mohm	10A

1. 當 +5VSB_DUAL current (DIMM+USB Port) <= 13A 時, N-MOS1 使用 Power PAK MOS 6 mohm, 沒有 N-MOS2
2. 當 13A < +5VSB_DUAL current (DIMM+USB Port) <= 15A 時, N-MOS1 使用 Power PAK MOS 4 mohm, 沒有 N-MOS2
3. 當 15A < +5VSB_DUAL current (DIMM+USB Port) <= 25A 時, N-MOS1 使用 Power PAK MOS, N-MOS2 使用 DPAK MOS 9 mohm
   <1> 當 DIMM 電流+ PCB Layout 由 N-MOS1 供電的 USB Port 電流 <= 13A 時, N-MOS1 使用 Power PAK MOS 6 mohm
   <2> 當 13A < DIMM 電流+ PCB Layout 由 N-MOS1 供電的 USB Port 電流 <= 15A 時, N-MOS1 使用 Power PAK MOS 4 mohm
4. 當 +5VSB_DUAL current (DIMM+USB Port) > 25A 時, 請與 Power Team 另外討論 N-MOS Solution
5. 若 Meomory Power 不是用 +5VSB_DUAL 產生, 則 DIMM 電流按 0A 計算
6. 因為 N-MOS1 在 Power Team Circuit 中, 請注意與 Power Team check Power Circuit 中 N-MOS1 是否正確
7. N-MOS2 若因為 PCB 面積不足放不下 DPAK MOS 9 mohm, 可改用 Power PAK MOS 6 mohm

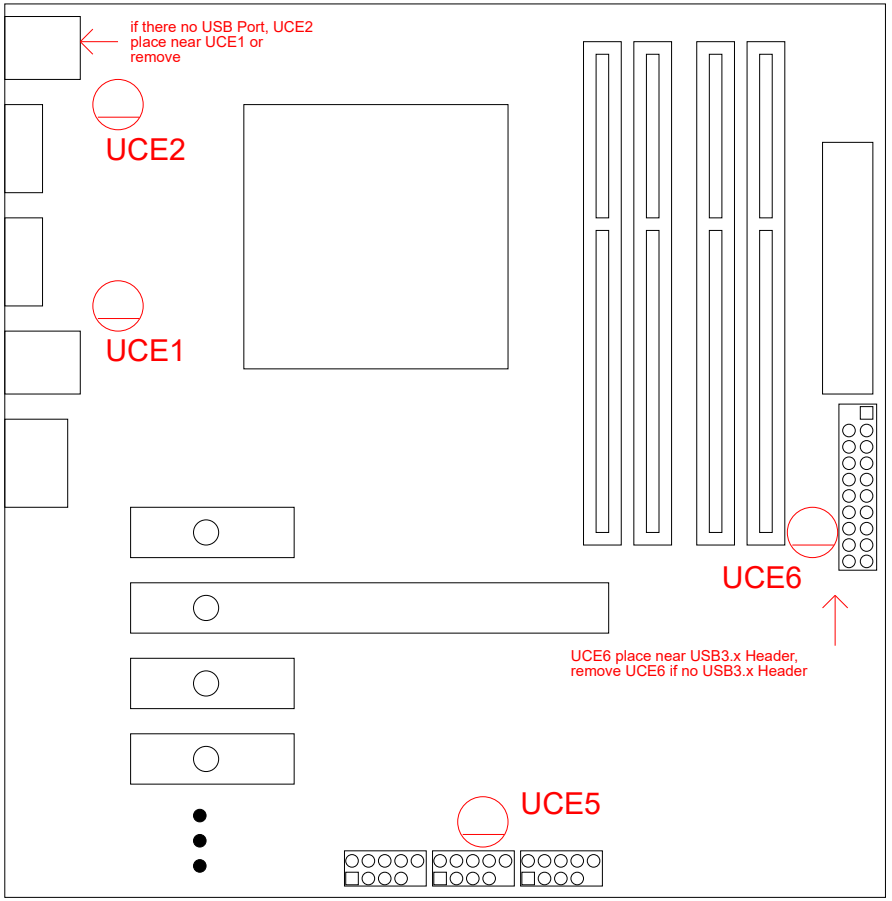


<Variant Name>

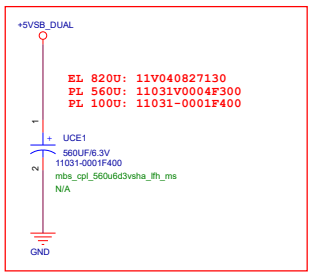
ASUSTEK COMPUTER INC	Title : N-MOS2	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 84 of 113	



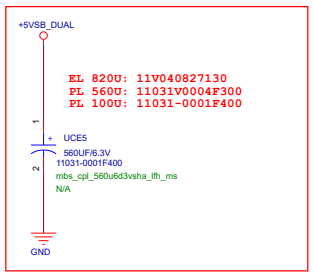
USB Power CAP recommend placement

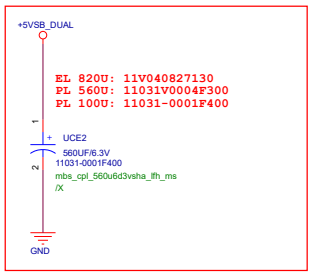


PL CAP & EL CAP co-lay



PL CAP & EL CAP co-lay



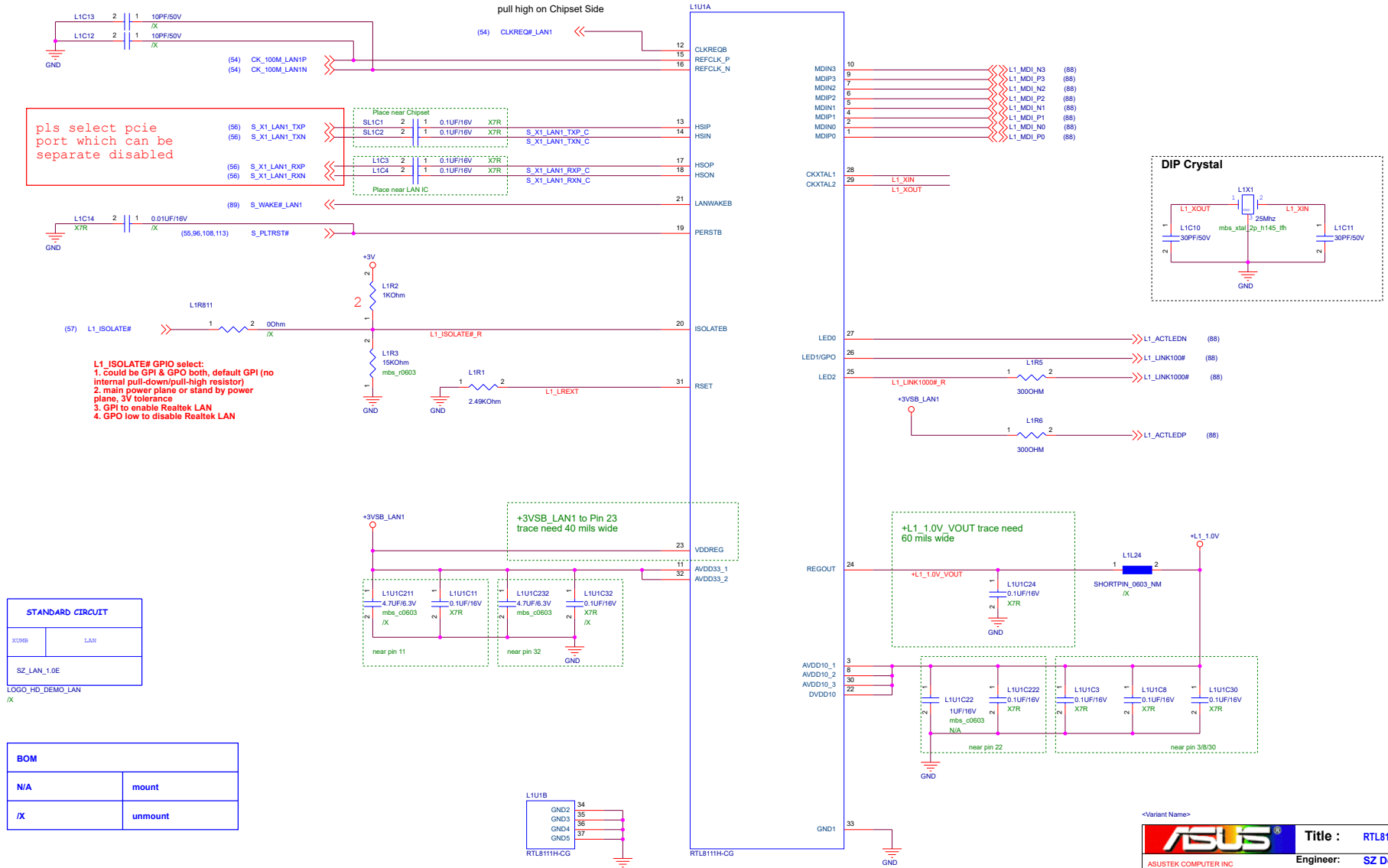


<Variant Name>

ASUSTEK COMPUTER INC	Title : USB Power CAP	
	Engineer: Kell_Huang	
Size: A3	Project Name: Chipset USB Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 85 of 113	

RTL8111H Circuit

1. If support Deep S4/S5 wake-up, rename S_WAKE# to S_WAKE#_LAN1
2. Modify PCIE Reset Signal Net Name by Project
3. Choose Crystal Type by Project
4. Check +3VSB_LAN1 Power Source by Project,
5. Delete CLKREQ#_LAN1 if not need
6. select block 1 or 2 according to if you support S0IX



STANDARD CIRCUIT	
XUMB	LAN
SZ_LAN_1.0E	

LOGO_HD_DEMO_LAN
/X

BOM	
N/A	mount
/X	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : RTL8111H

Engineer: SZ Design IP

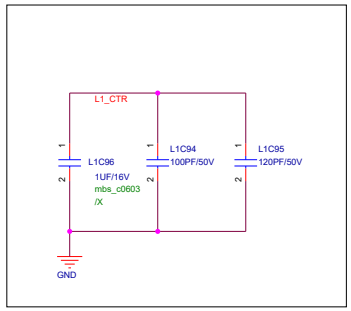
Size	Project Name	Rev
A3	LAN Demo Circuit	0.0

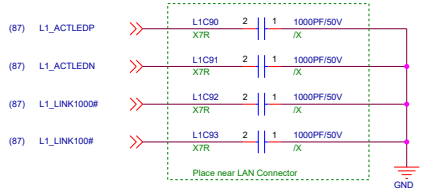
Date: Monday, June 11, 2018 Sheet 87 of 113

1. change LAN_USB12 name ,part, partnumber to what you want,copy from page24
2. change vcc source name
3. change usb signal name

4. del L1C96,L1C94,L1C95 according what lan you use

for Realtek LAN

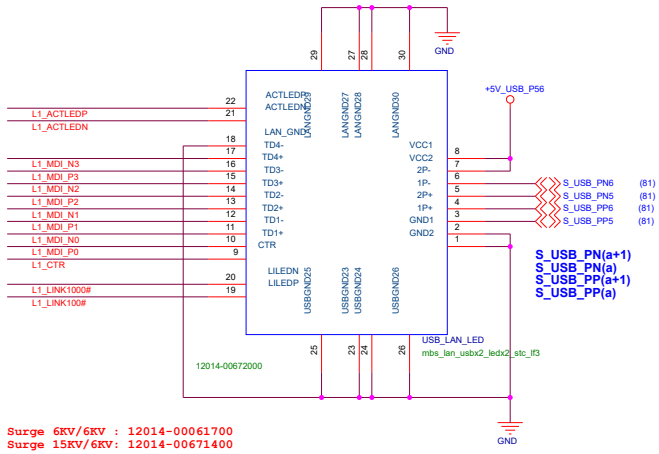




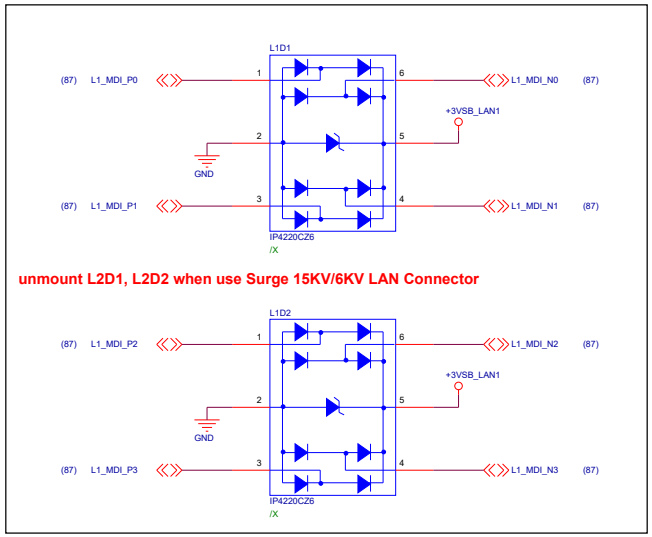
GLAN + USB2 *2 Connector

single LAN named LAN_USBxx
dual LAN named LAN1_USBxx

LAN_USB56



Delete it for EMS

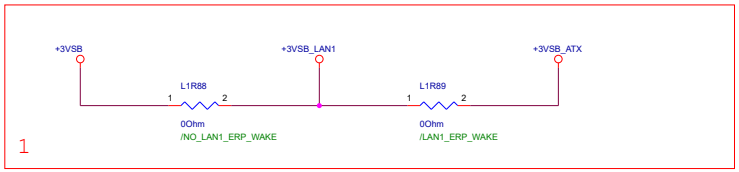


<Variant Name>

ASUSTEK COMPUTER INC	Title :	LAN Connector
	Engineer:	SZ Design IP
Size: A3	Project Name: LAN Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 88 of 113	

LAN1 Deep S4/S5 Wake-up Circuit

1. Remove Short-Pin L1R88 in LAN1 IC Page



for Intel PHY

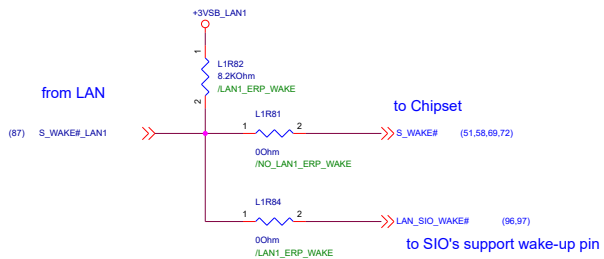
2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN1 IC Page

3. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN1 IC Page

for PCIE LAN1

4. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN1 IC Page

5. for Intel PCIE LAN, make sure L1_DEV_OFF# choose +3VSB_ATX power plane GPIO



<Variant Name>

ASUSTEK COMPUTER INC

Title : Deep S4/S5 Wake

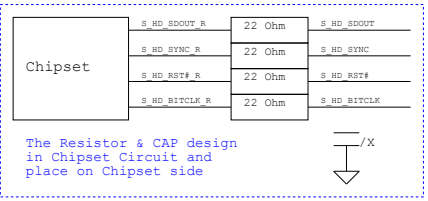
Engineer: SZ Design IP

Size	Project Name	Rev
A3	LAN Demo Circuit	0.0

Date: Monday, June 11, 2018 Sheet 89 of 113

ALC887-VD2 & ALC892 Circuit

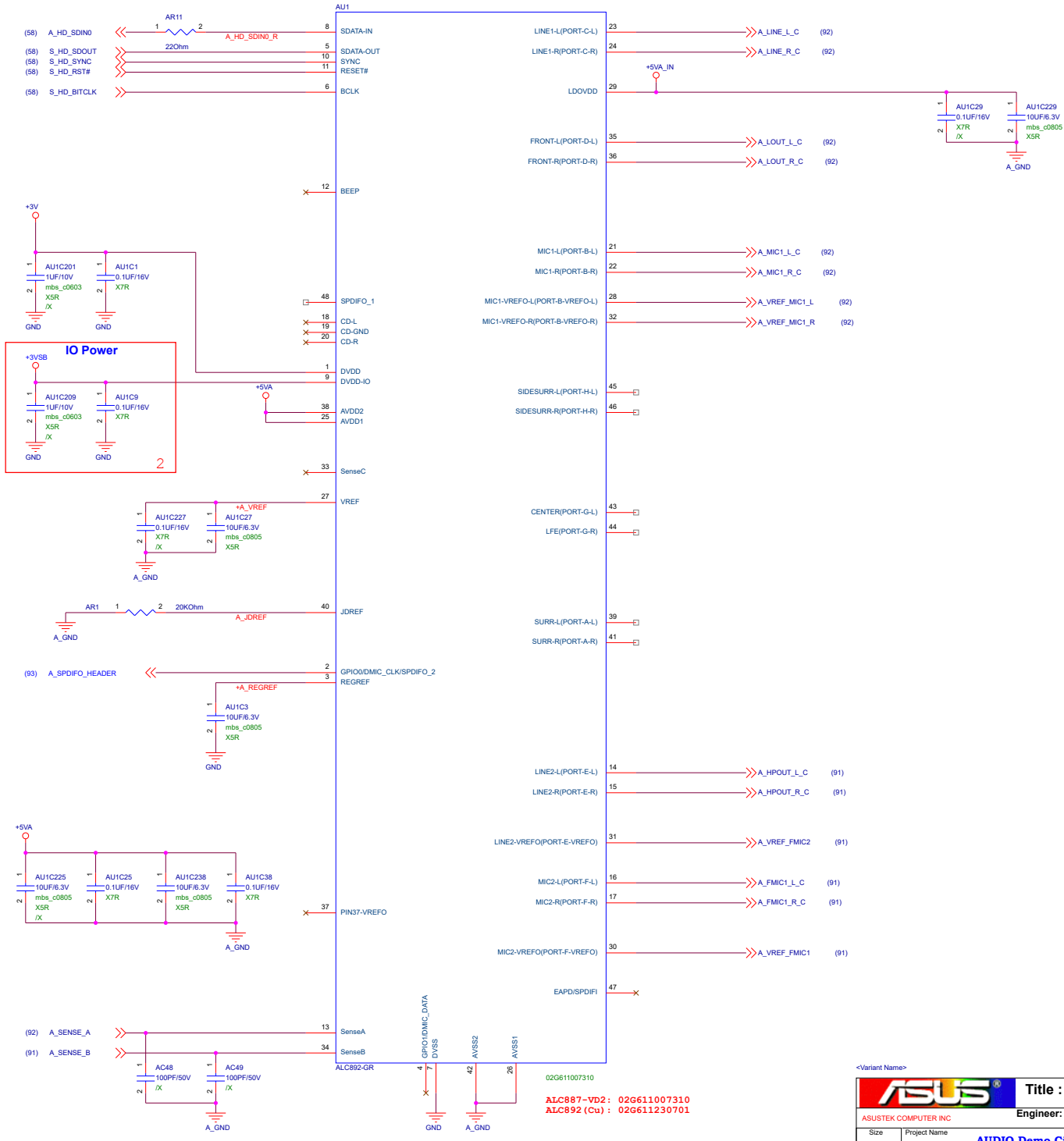
1. Modify AU1 Part Number by Project
2. Modify IO Power by Project
3. Delete A_EAPD if not need
4. Delete A_SPDIFO_HEADER if not need
5. Delete A_SPDIFO_OPTICAL if not need
6. Delete Side Surround for Rear 3 Jacks or 5Jacks
7. Delete CEN/LFE & Surround for Rear 3 Jacks
8. Block 8,9, select one of them according if support s0ix



BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT	
XUMB	Audio
SZ_Audio_1.0F	

HD_STANDARD_AUDIO
/X



<Variant Name>

ASUSTEK COMPUTER INC

Title : ALC887-VD2_ALC892

Engineer: SZ Design IP

Size	Project Name	Rev
Custom	AUDIO Demo Circuit	0.0

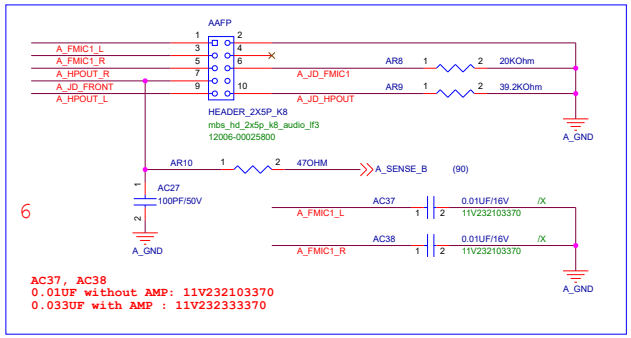
Date: Monday, June 11, 2018 Sheet 90 of 113

AAFP Circuit

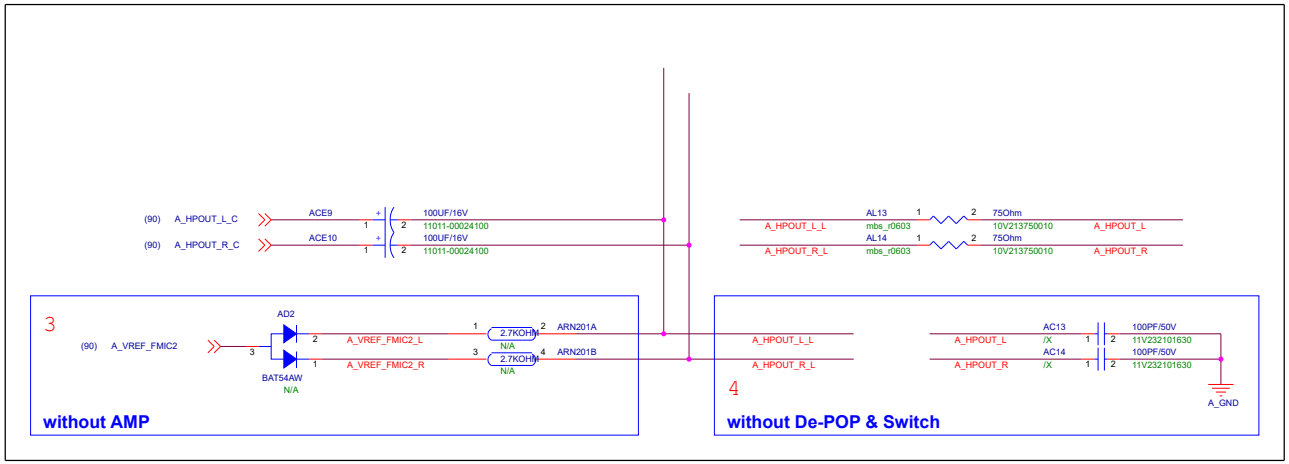
1. Choose AAFP Header Circuit by Codec,and change AAFP part number by your request,block 6,7, or 8
2. Choose HP Circuit with or without AMP/De-POP/Switch by Project,block 1,2,3,4
3. Modify ACE9, ACE10 Part Number by Project
4. IF you use 1220, AC13,AC14,AC15,AC16 option must change to N/A and change part number to varistor
5. Modify ARN202 value to 4.7k if you use 887,block 5
6. For Gamer Project with ALC1150, AL13, AL14 change to 47Ohm
7. change AC37,AC38 part number if you have AMP,block 6

AAFP

for ALC887-VD2/ALC892



for ALC887-VD2/ALC892/ALC1150/ALC1220X



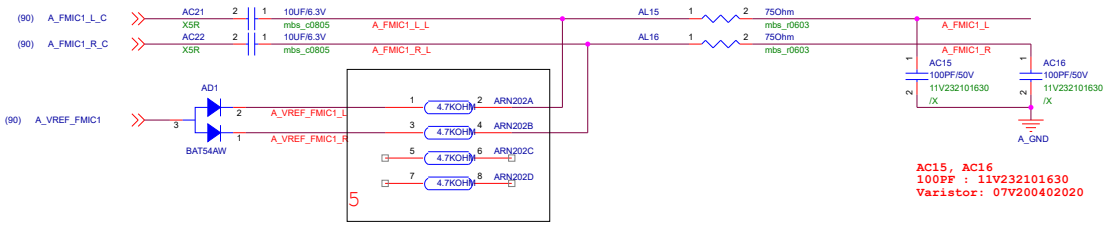
DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000
Nichicon 100U: 11011-00026100
Elan 100U :11011-00025000

AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010

AC13, AC14
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
Chemicon 100U T: 11011-00024100

Taping DIP CAP
PL 100U T:11031V0001F400



ARN202 change to 4.7K Ohm for ALC887-VD2

AC15, AC16
100PF : 11V232101630
Varistor: 07V200402020

Delete it for EMS

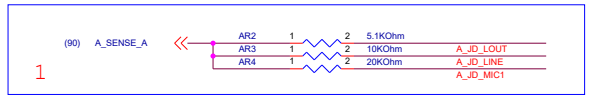
<Variant Name>

ASUSTEK COMPUTER INC	Title : AAFP	
	Engineer: SZ Design IP	
Size: A3	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 91 of 113	

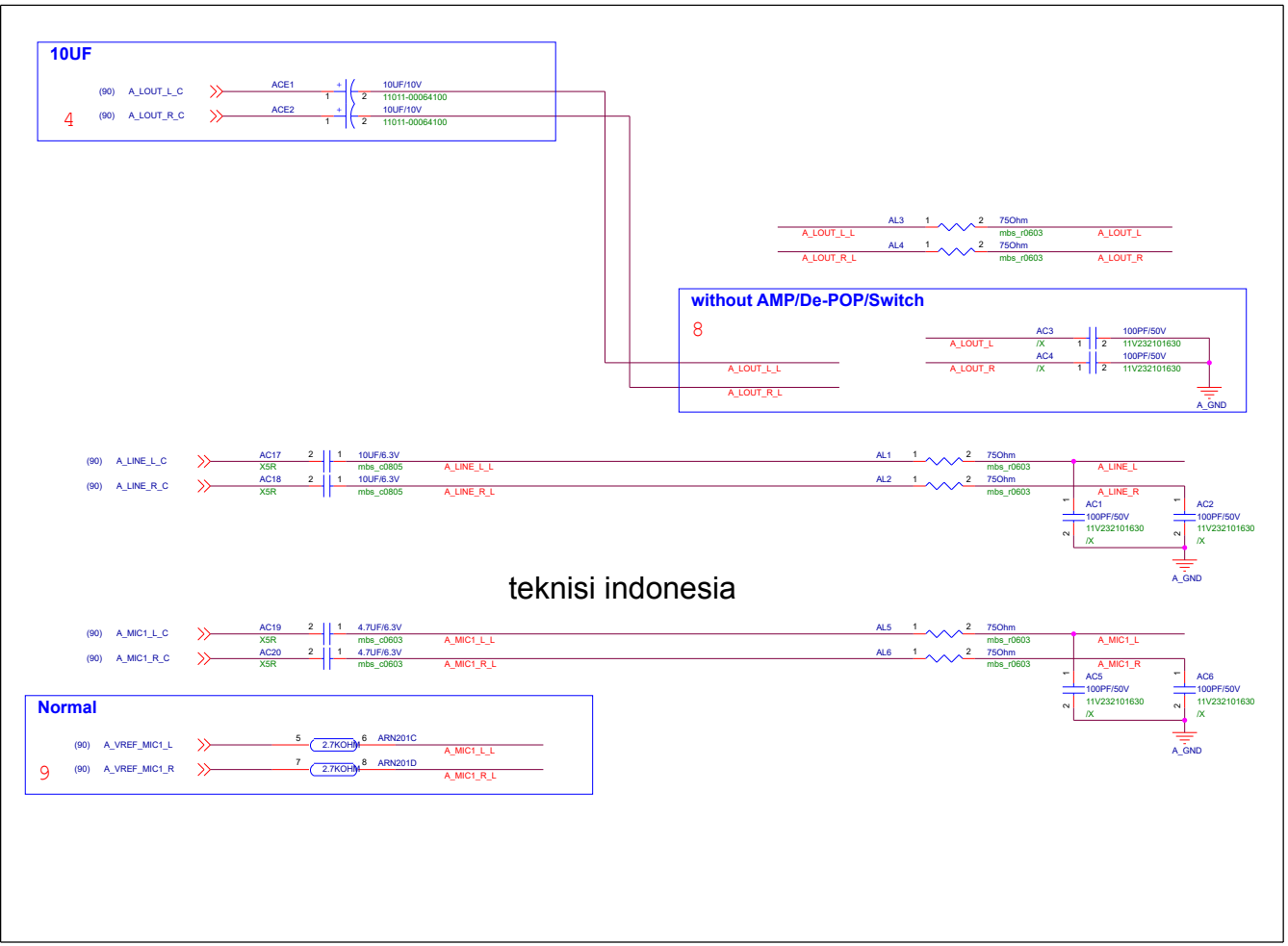
Rear 3Jacks Circuit

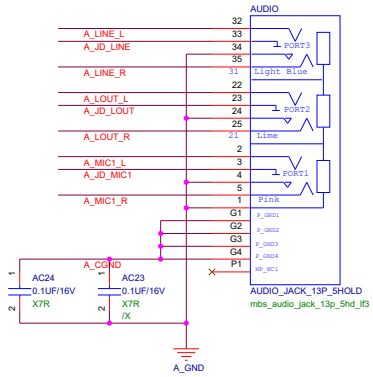
1. Choose Jack Detect Circuit by Codec,block 1,2,3
2. Choose LOUT DIP CAP Type by Codec & Project,block 4,5,6
3. Choose LOUT Circuit with or without De-POP/Switch by Project,block 7,8
4. Modify ACE1, ACE2 Part Number by Project
5. Choose Rear MIC VREF Circuit by Project ,block9,10
6. For Gamer/Gaming modity AC17, AC18 part by request
7 if you use 1220 ,Modify AC1,AC2,AC3, AC4, ,AC5,AC6, Part Number to varistor and Optional to N/A

for ALC887-VD2/ALC892



Delete it for EMS





Audio CAP using rule,pls change all dip caps partnumber according bellow rule

Z390,B450 ROG / Strix series	Nichicon
Z390,B450 PRIME / TUF Series	ELNA
Intel H310,H310C,H110&AMD A320 series	Chemicon
other chipsets except above series	Nichicon

<Variant Name>

DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207
Nichicon 10U: 11011-00066100
Elan 10U:11011-00065000

Taping DIP CAP
Chemicon 10U T: 11011-00064100

DIP CAP
EL 100U : 11V040107321
PL 100U : 11031V0001F000
Nichicon 100U: 11011-00026100
Elan 100U :11011-00025000

Taping DIP CAP
Chemicon 100U T: 11011-00024100

AC1, AC2, AC3, AC4, AC5, AC6
100PF : 11V232101630
Varistor: 07V200402020

Taping DIP CAP
PL 100U T:11031V0001F400

ASUSTEK COMPUTER INC

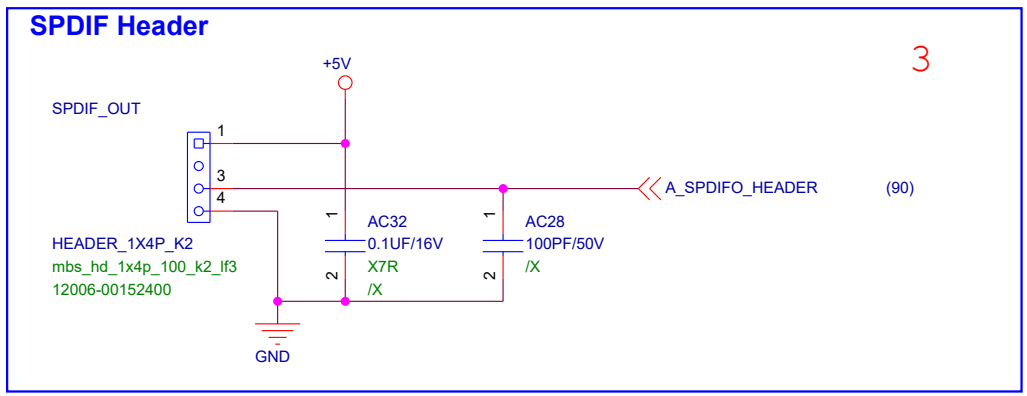
Title : 3 Jacks
Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Monday, June 11, 2018 Sheet 92 of 113

SPDIF

1. select block 1,2, or 3 by project



<Variant Name>

ASUSTEK COMPUTER INC	Title : SPDIF	
	Engineer: SZ Design IP	
Size: A	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 93 of 113	

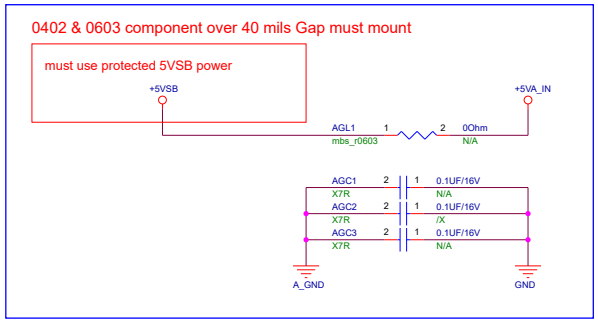
Audio GAP & Power Circuit

1. Choose Resistor & Capacitor over GAP Circuit by Project

2. Keep or delete Audio Power LDO Circuit by Project

3. Modify APCE4 Part Number by Project

40 mils Gap for XU



BOM	Audio Power from 5VSB	Audio Power from 12V LDO 5V
/AUDIO_PWR_5VSB	mount	unmount
/AUDIO_PWR_LDO	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : GAP_Power

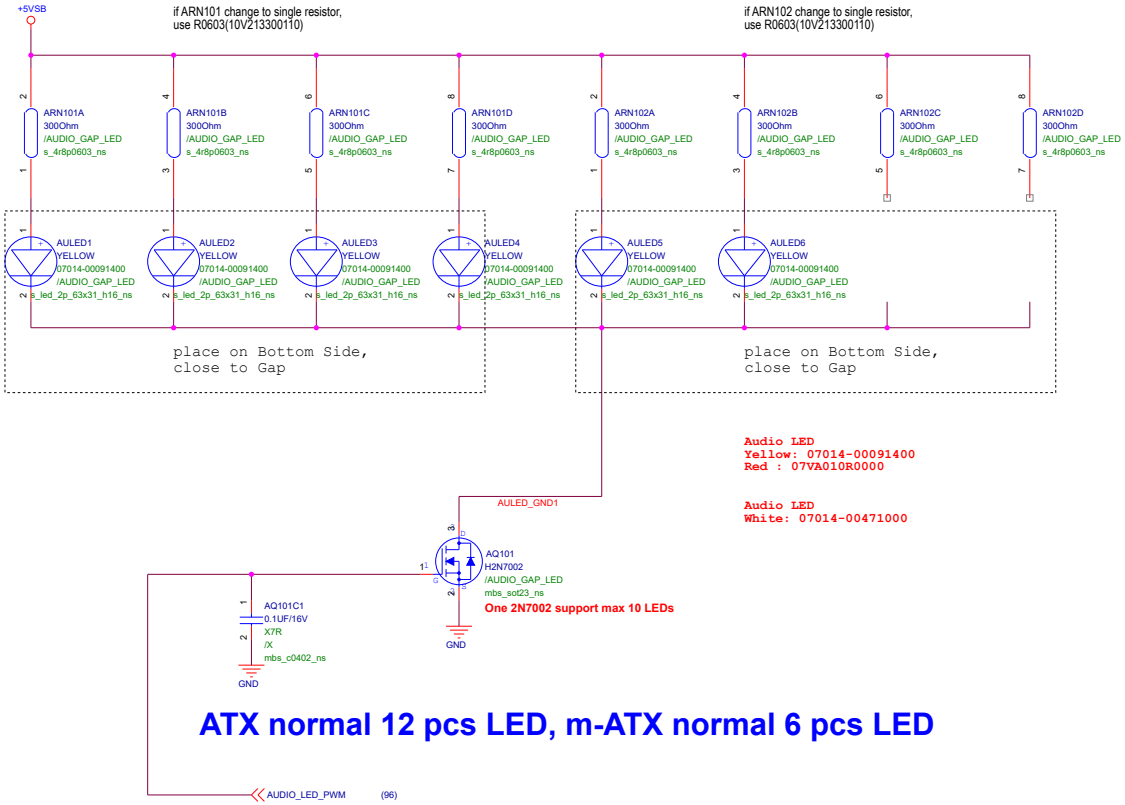
Engineer: SZ Design IP

Size	Project Name	Rev
A3	AUDIO Demo Circuit	0.0

Date: Monday, June 11, 2018 Sheet 94 of 113

AUDIO LED Circuit

1. Modify Audio LED part number by Project
2. Choose or delete Codec Cover by Project
3. Keep or delete Codec Cover LED by Project
4. Modify Codec Cover Part Number by Project
5. One 2N7002 support max 10 LEDs



Audio LED
Yellow: 07014-00091400
Red : 07VA010R0000

Audio LED
White: 07014-00471000

AUDIO_LED_PWM GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. could mapping to Fading PWM function
3. stand by power plane, 3V tolerance
4. GPI to turn on Audio LED
5. GPO low to turn off Audio LED
6. Fading PWM to be Breathing LED

<Variant Name>

ASUSTEK COMPUTER INC	Title : Cover_LED	
	Engineer: SZ Design IP	
Size: A3	Project Name: AUDIO Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 95 of 113	

NCT5582D Circuit

A. Choose +3V_SIO Power Source

B. Check Pin 59 VTT Power should be CPU PECI Power

C. Delete LPC Bus Signal Pull High Resistor if don't need

D. Delete Pin 13 KBRST# Circuit if not connect KBRST# to Chipset

E. Choose Pin 48 THERMTRIP#/CASEOPEN0# circuit by Project

F. Delete COM1 Port Signal if don't need, but keep Strapping Pin Signal

G. Choose NCT5582D DDR4 Power Sequence Circuit by Project

SMBUS	AUDIO_LED_PWM	DDR4 Power Seugence
Not use	GPI32(GRN_LED)	Can use
Use	GRN_LED(GP23 or GP84)	Can use
Use	GP24(MULED)	Can not use

H. Modify FAN IN/PWM/GPP/GPL Signal by Project

I. Add SMBUS Circuit by Project

J. If use COM Port RI# do Deep S4/S5 wake-up, modify Pin 21 net name to LAN_SIO_WAKE#

K. Delete AUDIO_LED_PWM Signal if don't need

L. If SIO Breathing LED is reserved, unmount AUDIO_LED_PWM pull high resistor

M. AUDIO_LED_PWM use GRN_LED or MLED or YLW_LED

N. Other Flash/Breathing LED could use YLW_LED or MLED or GRN_LED, but not same with AUDIO_LED_PWM

O. Add COM Debug Signal by Project, use Pin 33 or 19

P. Add SMI#/BEEP Signal by Project, use GPIO mapping function

Q. If use Pin 41 as OVT#, should add external RSTCON# De-bounce Circuit

R. If use MS as FAN or GPIO, remove pull high resistor ORN404A/ORN404D, but keep MS Signal default pull high with other resistor to main power

S. If need turn off Stand By Power LED, choose a SIO GPIO connect to O_SBPWRLED; if the GPIO default output high, could unmount O1R207

T. If use SIO Anti Surge Function, mount O1C32, O1C34

NCT5582D FAN Header Pin Table for Intel 300 Series

SIO FAN	FAN IN	FAN PWM	GPP	GPL	FAN Header
CPUFAN	Pin 61	Pin 62	Pin 33	Pin 2	CPU_FAN
SYSFAN	Pin 63	Pin 64			CHA_FANCHA_FAN1
AUXFAN2	Pin 36 or 43 or 27	Pin 37 or 44 or 26			CHA_FAN2
AUXFAN3	Pin 25	Pin 24			AIO_PUMP

FAN Net Name Table

FAN	FAN IN	FAN PWM	FAN GPP with 3941	FAN GPP with 3949	FAN GPL with 3949
CPU_FAN	O_CPUFANIN	O_CPUFAN_PWM		GP_CPUFAN_MODE_SEL	GP_CPUFAN_EQM_EN#
CPU_OPT	O_CPUOPTIN				
CHA_FAN1	O_CHAFANIN1	O_CHAFAN_PWM	GP_CHAFAN_PWM_DC#	GP_CHAFAN_MODE_SEL	GP_CHAFAN_EQM_EN#
CHA_FAN2	O_CHAFANIN2	O_CHAFAN_PWM2	GP_CHAFAN_PWM_DCR2	GP_CHAFAN_MODE_SEL2	GP_CHAFAN_EQM_EN#2
CHA_FAN3	O_CHAFANIN3	O_CHAFAN_PWM3	GP_CHAFAN_PWM_DCR3	GP_CHAFAN_MODE_SEL3	GP_CHAFAN_EQM_EN#3
CHA_FAN4	O_CHAFANIN4	O_CHAFAN_PWM4	GP_CHAFAN_PWM_DCR4	GP_CHAFAN_MODE_SEL4	GP_CHAFAN_EQM_EN#4
AIO_PUMP	O_AIO_PUMP_FANIN	O_AIO_PUMP_PWM		O_AIO_PUMP_MODE	
W_PUMP+1	O_PUMP_FANIN	O_PUMP_PWM		O_PUMP_MODE	
W_PUMP+2	O_PUMP2_FANIN	O_PUMP2_PWM		O_PUMP2_MODE	
M.2_FAN	O_M2_FANIN	O_M2_FAN_PWM		GP_M2_FAN_MODE_SEL	GP_M2_FAN_EQM_EN#

NCT5582D VIN Table

SIO VIN	CPUVCORE	VIN0	VIN1	VIN9
VIN IN	VCORE	+12V	+5V	

NCT5582D TIN Table

SIO TIN	CPUTIN	SYSTIN
TIN IN	CPU	MB

NCT5582D SMBUS Table

	SMBUS Master to RGB LED EC
SIO SMBUS	Pin 36, 37

C

could delete this block when LPC Bus Signal with Chipset side pull-high

Choose SIO Power Source

A.2

E.2

Pin 48 used as CASEOPEN0#

D

F

J

K

L

G

for use or reserve NCT5582D DDR4 Power Sequence

Use SIO DDR4 Power Sequence, mount O1R187, O1R188, O1R189, O1R43, unmount O1R42

Unuse SIO DDR4 Power Sequence, unmount O1R187, O1R188, O1R189, O1R43, mount O1R42

Near monitor point

HW Monitor

+3V_SIO, +3VSB or +1.8VSB by Project

Nuvoton SIO COM Port Strapping Pin pull down with 680 Ohm, pull high with 680 - 1K Ohm

BOM	use SIO DDR4 Sequence	unuse SIO DDR4 Sequence
/DDR4SEQ	mount	unmount
/NODDR4SEQ	unmount	mount

BOM	LPC Mode	eSPI Mode
/LPC	mount	unmount
/eSPI	unmount	mount

BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT

SIZE	Project 1.0
SZ_SIO_1.0F	
X	

<Variant Name>

ASUSTeK COMPUTER INC.

Title : NCT5582D_Intel

Engineer: SZ Design IP

Size: Custom | Project Name: Super I/O Demo Circuit | Rev: 0.0

Date: Monday, June 11, 2018 | Sheet 96 of 113

COM PORT

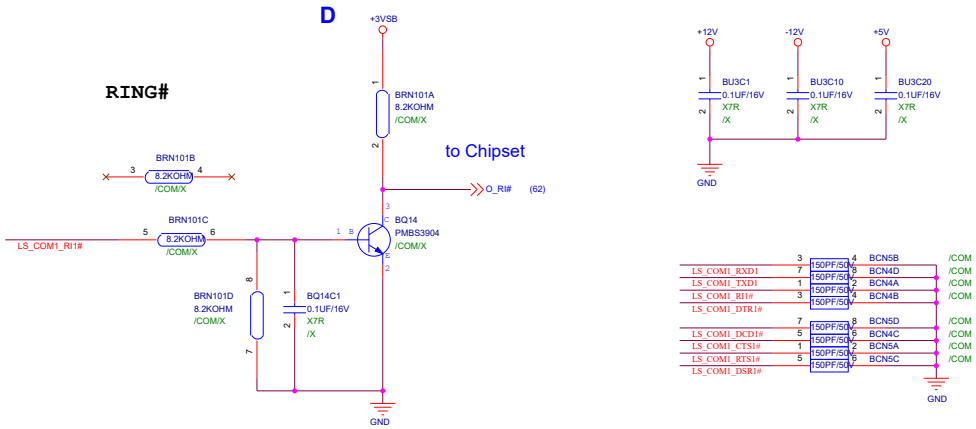
COM Circuit

A. Choose COM Port Connector/Header Type

B. Choose use RI# to do Deep S4/S5 wake-up or not by Project

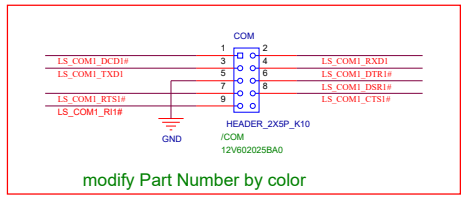
C. Modify Part Number of COM Connector/Header by Color

D. Modify O_RI# pill-high power by Project



A.2

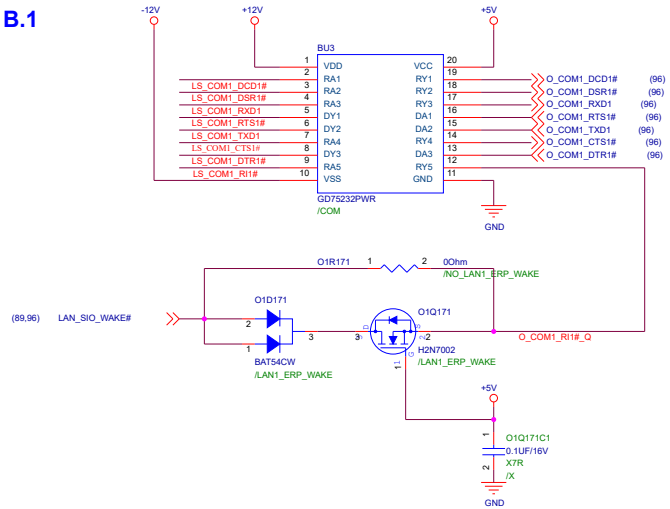
COM Header



for use COM Port RI# to do Deep S4/S5 wake-up function

modify SIO RI# Pin net name to LAN_SIO_WAKE#

B.1



for not use COM Port RI# to do Deep S4/S5 wake-up function

When mount /COM

LAN Deep S4/S5 wake-up	O1R171	O1Q171 & O1D171
support	unmount	mount
not support	mount	unmount

When unmount /COM

LAN Deep S4/S5 wake-up	O1R171	O1Q171 & O1D171
support	unmount	unmount
not support	unmount	unmount

BOM	need COM Port	no COM Port
/COM	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : COM

Engineer: SZ Design IP

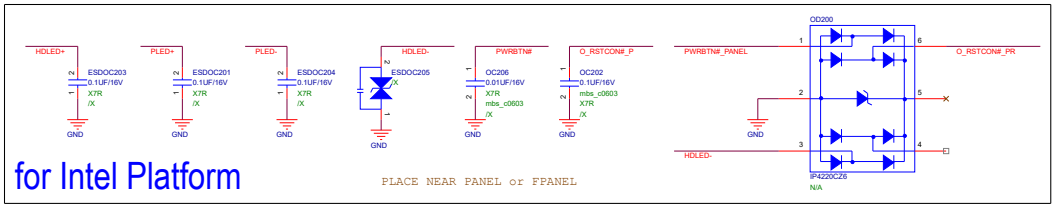
Size	Project Name	Rev
A3	Super I/O Demo Circuit	0.0

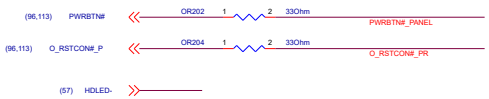
Date: Monday, June 11, 2018 Sheet 97 of 113

Panel Circuit

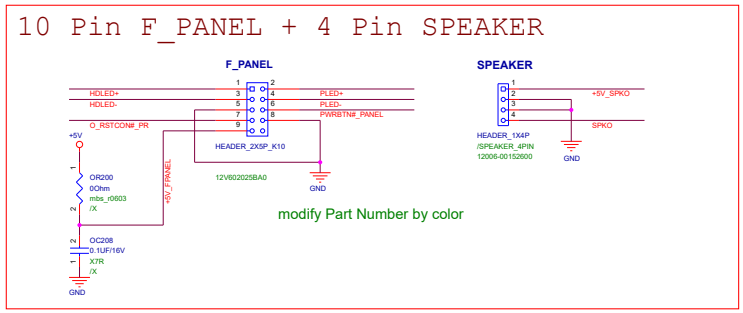
A. Choose PANEL/F_PANEL Signal ESD Solution by Project
B. Choose PANEL/F_PANEL Circuit + Chassis Inturder Circuit by Project
C. Choose Chassis Inturder Signal connect to SIO or Chipset by Project
D. Choose SPEAKER Header Circuit + BUZZER Circuit by Project
E. Choose PLED Circuit by Project
F. Choose PLED control by SIO or Chipset
G. If use Memory Power control PLED, check Memory Power Net Name
H. Modify Part Number of PANEL/F_PANEL/SPEAKER Header by Color

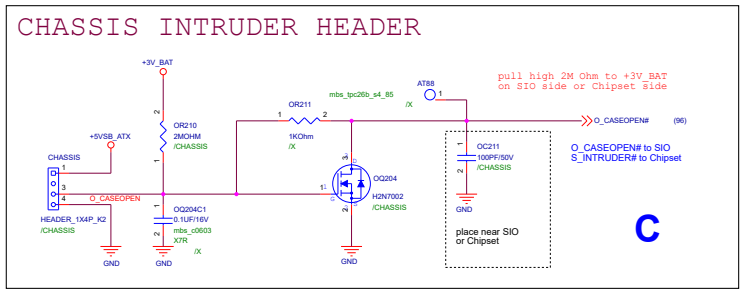
A.1



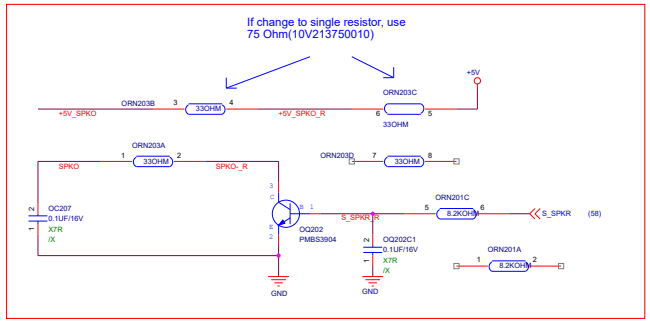


B.1





D.1



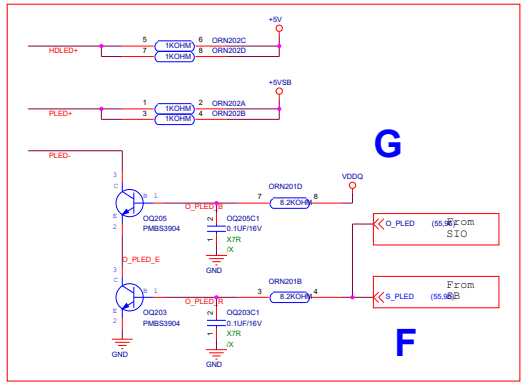
BOM	need SPEAKER	no SPEAKER
/SPEAKER_4PIN	mount	unmount

BOM	need BUZZER	no BUZZER
/BUZZER	mount	unmount

BOM	need CHASSIS	no CHASSIS
/CHASSIS	mount	unmount

E.1

Power LED power source use +5VSB



O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI(no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. Porting Guide: default keep GPI, enable blink 0.5Hz or 1Hz function when enter S3, disable blink function and back to GPI when resume from S3

<Variant Name>

ASUSTEK COMPUTER INC

Title :	PANEL		
Engineer:	SZ Design IP		
Size: Custom	Project Name: Super I/O Demo Circuit		Rev: 0.0
Date: Monday, June 11, 2018	Sheet 98 of 113		

EATX Power Circuit

A. Choose EATX Power Circuit by Project

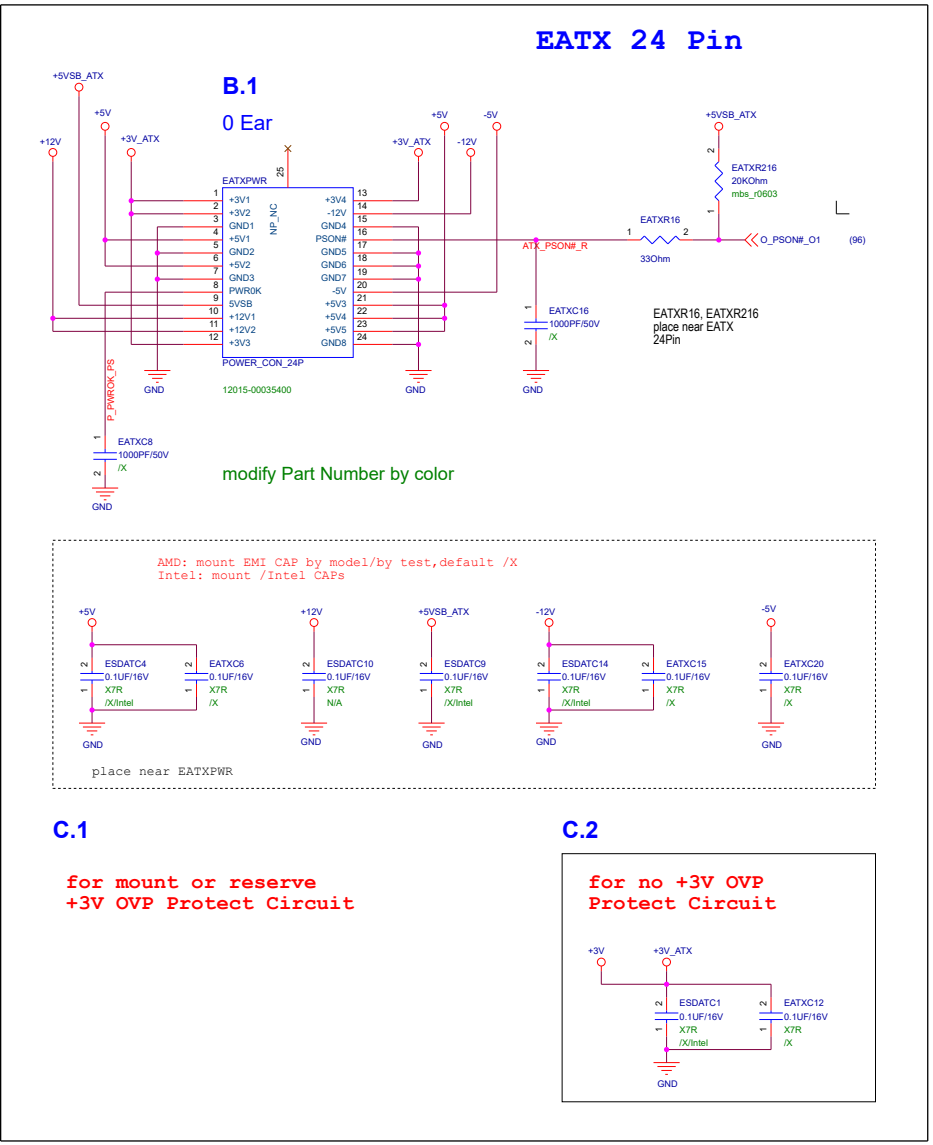
B. If choose EATX 24Pin Circuit, choose EATX Connector with 0 Ear, 1 Ear or 2 Ears by Project

C. If choose EATX 24Pin Circuit, choose +3V_ATX & +3V Circuit by Project

D. If support Intel S0ix, add SC945, SC946 & Off-Page Net O_PSON#_O1 change to ATX_PSON#

E. Modify Part Number of EATX Connector by Color

A.1



<Variant Name>

ASUSTEK COMPUTER INC	Title : EATX	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 99 of 113	

KBMS Circuit

A. Choose KBMS Power Source by Project

B. If KBMS share power with USB Port, modify Share Power Net Name by Project

C. Choose KBMS Port Connector by Project

D. If choose KBMS Connector, KBMS Signal to-GND Cap choose Single Capacitor or RES Cap by Project

E. If choose KB & USB 2.0 Connector, check USB 2.0 Port D+/D- Signal begin with 0 or 1, then modify USB 2.0 Port D+/D- Signal Net Name by Project

F. If choose KB & USB 3.0 Connector, modify USB Port TX/RX/D+/D- Signal Net Name by Project

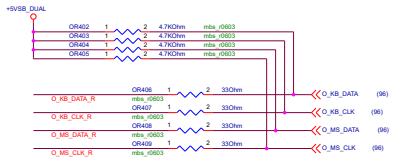
G. If choose KB & USB Connector, modify USB Port Power Net Name by Project

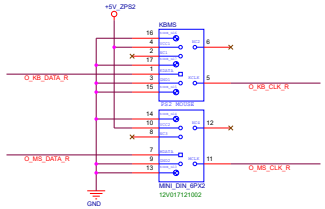
H. If choose KB & USB Connector, modify Connector Part Reference by Project

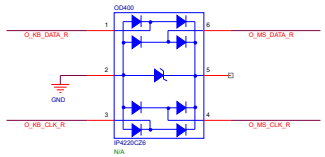
I. If choose KB & USB Connector, for ITE SIO, ORN404 could /X for cost down

C.2

KBMS







D.1

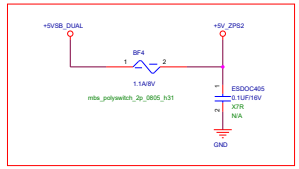
RES Capacitor

D.2 for SI

Single Capacitor

A.2

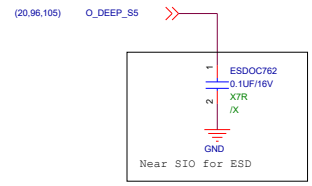
Dedicated Power



ERP Circuit

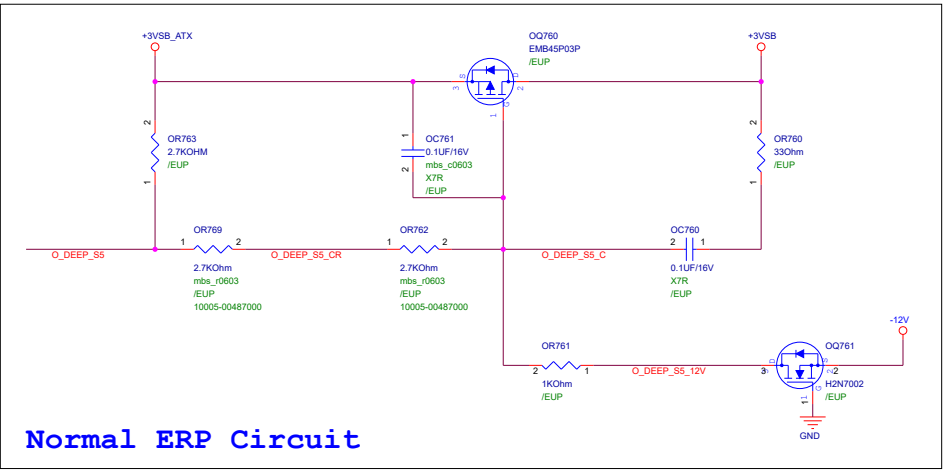
A. Choose ERP Circuit by Project

B. OR764, OR765 choose Short-Pin, Resistor or delete by Project

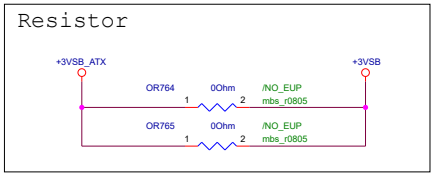


BOM	no SIO ERP & SIO DSW	SIO ERP	SIO DSW
/NO_EUP	mount	unmount	unmount
/EUP	unmount	mount	mount
/NO_SIODSW	mount	mount	unmount
/SIODSW	unmount	unmount	mount

A.2



B.2



<Variant Name>

ASUSTEK COMPUTER INC

Title : ERP

Engineer: SZ Design IP

Size: Custom | Project Name: Super I/O Demo Circuit | Rev: 0.0

Date: Monday, June 11, 2018 | Sheet 101 of 113

Stand By LED & HW Monitor Circuit

A. Choose Stand By LED Circuit by Project

B. Keep or delete TR_PCH Circuit by Project

C. Keep or delete T_SENSOR Circuit by Project

D. Keep or delete VCORE Power Controller TEMP Detect Circuit by Project

E. Keep or delete GFX Power Controller TEMP Detect Circuit by Project

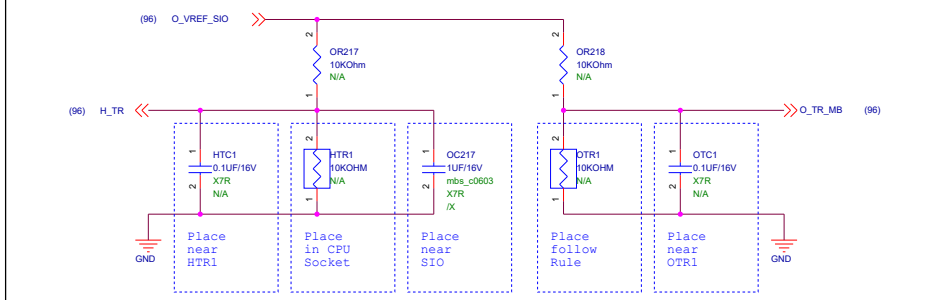
F. Modify Part Number of T_SENSOR Header by Color

BOM	no Stand By LED	need Stand By LED without GPIO control	need Stand By LED with GPIO control
/StandByLED	unmount	mount	mount
/StandByLED_without_GPIO	unmount	mount	unmount
/StandByLED_with_GPIO	unmount	unmount	mount

BOM	need TR_PCH	no TR_PCH
/TR_PCH	mount	unmount

BOM	need T_SENSOR	no T_SENSOR
/T_SENSOR	mount	unmount

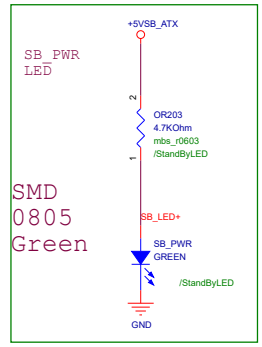
HW Monitor



If no CPU thermistor, unmount components HTR1, HTC1, OR217

If no MB thermistor, unmount components OTR1, OTC1, OR218

A.1



<Variant Name>

ASUSTEK COMPUTER INC	Title : SBLED_HWM	
	Engineer: SZ Design IP	
Size: Custom	Project Name: Super I/O Demo Circuit	Rev: 0.0
Date: Monday, June 11, 2018	Sheet 102 of 113	

CHA_FAN PWM Mode & DC Mode QFAN Circuit use Single Resistor

A. Choose QFAN Mode Type by Project

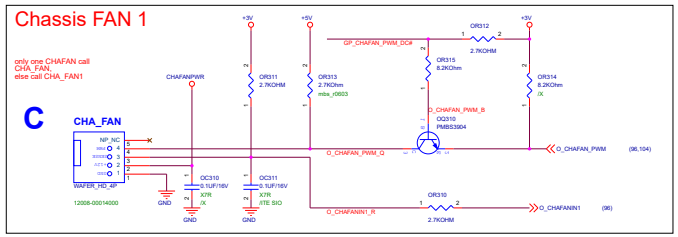
B. Remove the CHA_FAN which don't need

C. If only one CHA_FAN, rename CHA_FAN1 to CHA_FAN

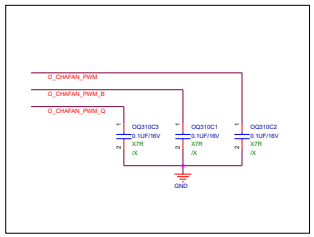
D. Modify Part Number of CHA FAN Header by Color

A.1

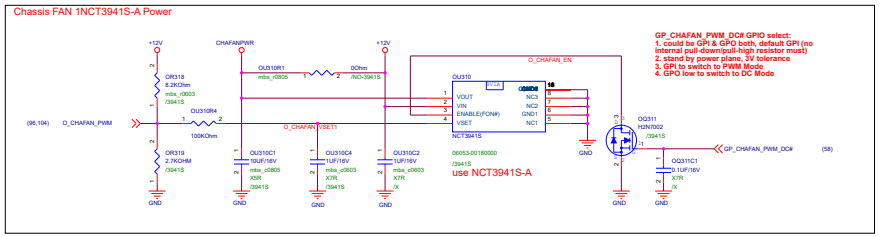
4 Pin PWM Mode & DC Mode



BJT Cap



PWM Mode & DC Mode Power Solution



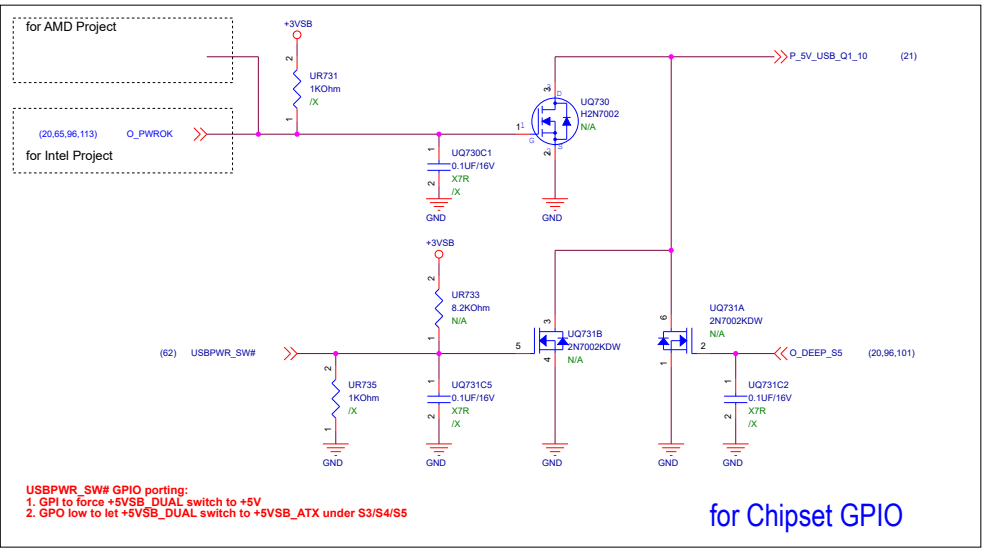
USBPWR_SW# Circuit for Chipset GPIO

1. Choose USBPWR_SW# Circuit by Project

2. Check PWROK Signal Net Name by Platform

USBPWR_SW# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance

+5VSB_DUAL default no power, reserve USB Inrush Circuit



<Variant Name>

ASUSTEK COMPUTER INC

Title : USB Power Control

Engineer: SZ Design IP

Size	Project Name	Rev
Custom		0.0

Date: Monday, June 11, 2018 Sheet 105 of 113

Debug Header Circuit

A. Choose Debug Header by Project

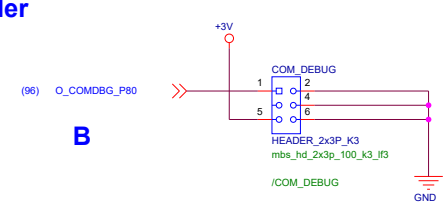
B. If choose COM Debug Header, take care Debug Signal Net Name is different by Project

C. If choose LPC Debug Header, modify Clock Signal Net Name by Project

A.2

Delete it for EMS

COM Debug Header



COM Debug Signal from Nuvoton 128 Pin SIO SOUTB_P80 or SOUTC_P80 Signal

BOM	need COM Debug Header	no COM Debug Header
/COM_DEBUG	mount	unmount

BOM	need LPC Debug Header	no LPC Debug Header
/LPC_DEBUG	mount	unmount

<Variant Name>

ASUSTEK COMPUTER INC

Title : Debug Header

Engineer: SZ Design IP

Size	Project Name	Rev
B	Super I/O Demo Circuit	0.0

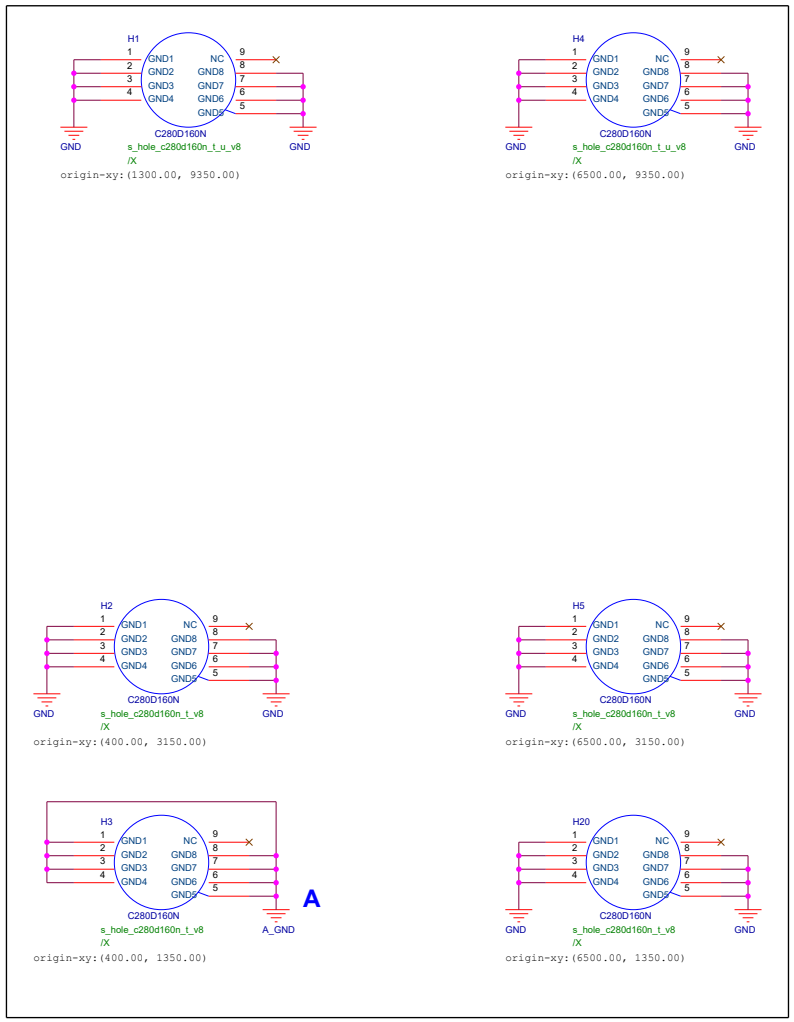
Date: Monday, June 11, 2018 Sheet 106 of 113

m-ATX Screw Hole Circuit

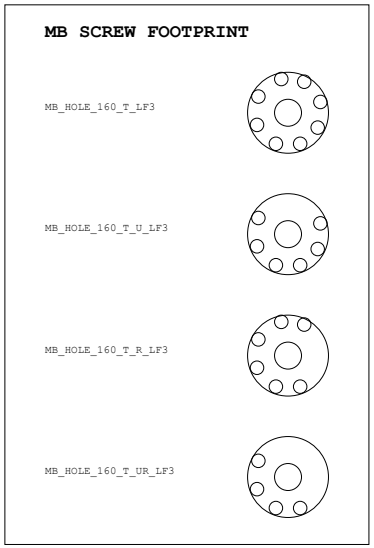
A. Connect H3 to GND or A_GND by Project

Delete it for EMS

m-ATX Screw Hole



MB SCREW FOOTPRINT



<Variant Name>

ASUSTEK COMPUTER INC	Title :	Screw Hole	
	Engineer:	SZ Design IP	
Size: A3	Project Name: Other Demo Circuit		Rev: 1.0D
Date: Monday, June 11, 2018	Sheet 107 of 113		

LPC TPM Circuit

A. Del LPC TPM Header if don't need

B. Modify LPC TPM Header Clock Net Name by Project

C. Modify Part Number of LPC TPM Header by Color

D. Del Onboard LPC TPM IC if don't need

E. Modify Onboard LPC TPM IC Clock Net Name by Project

F. Modify Onboard LPC TPM IC's Part Number by Project

G. Modify Optional of TMR13, TMR14, TMR15 by Onboard LPC TPM IC

H. Modify +3V to +3V_S0IX if support Intel S0ix

I. Choose TPM_CLKRUN# Circuit by Project

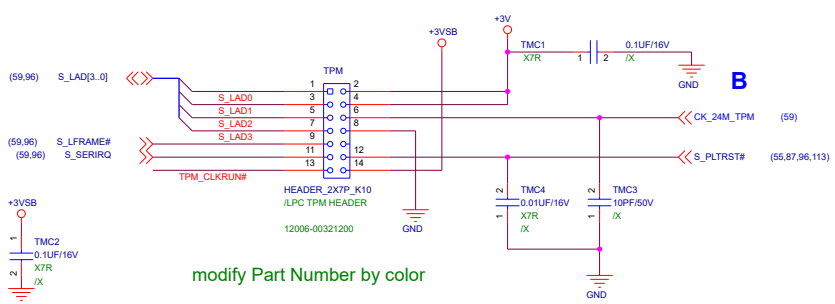
I.2

for no Intel S0ix

A

2x7 Pin LPC TPM Header

H



B

BOM	LPC TPM Header	Onboard LPC TPM
N/A	mount	mount
/X	unmount	unmount
/LPC TPM HEADER	mount	unmount
/LPC TPM IC	unmount	mount

<Variant Name>

ASUSTEK COMPUTER INC

Title : LPC TPM

Engineer: SZ Design IP

Size	Project Name	Rev
A3	Other Demo Circuit	1.0D

Date: Monday, June 11, 2018 Sheet 108 of 113

Fiducial Mask (光學點)

Delete it for EMS

圓形光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

大顆光學點

小顆光學點

Delete it for EMS

十字光學點

LayoutRD會依空間大小，
擺放大顆或小顆光學點；
所以兩種光學點都需畫入線路中，
最後再做刪除.

大顆光學點

小顆光學點

<Variant Name>

ASUSTEK COMPUTER INC	Title : Fiducial Mask	
	Engineer: SZ Design IP	
Size: A3	Project Name: Silkscreen Demo Circuit	Rev: 1.0C
Date: Monday, June 11, 2018	Sheet 111 of 113	

Intel Platform

You can only choose **8** pcs PCB Impedance point for your project

Priority 0 (must choose if use ASM1142/2142/3142)

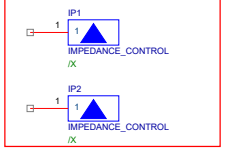
ASMedia USB 3.1 TX/RX

80 Ohm +/- 10%

Priority 1, must choose if MB have these functions

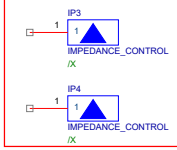
1

LAN



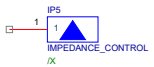
2

PCIE GEN2/3



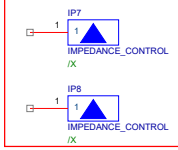
3

DDR3 DATA&CTRL



4

USB2.0

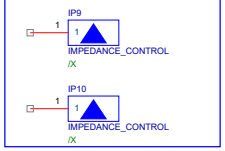


*** You can only choose 1 function to place point per block ***

Priority 2, can choose if MB have these functions (by project)

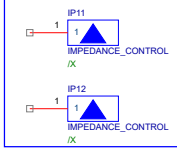
1

DP/DVI/HDMI



2

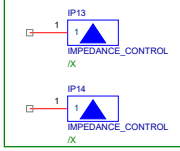
USB3.0



Priority 3, can choose if MB have these functions (by project)

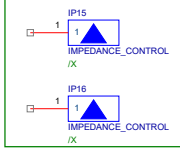
1

DMI



2

DDR3 CLK



Delete it for EMS

<Variant Name>

ASUSTEK COMPUTER INC

Title : PCB Impedance Point

Engineer: SZ Design IP

Size: A3 | Project Name: Silkscreen Demo Circuit | Rev: 1.0C

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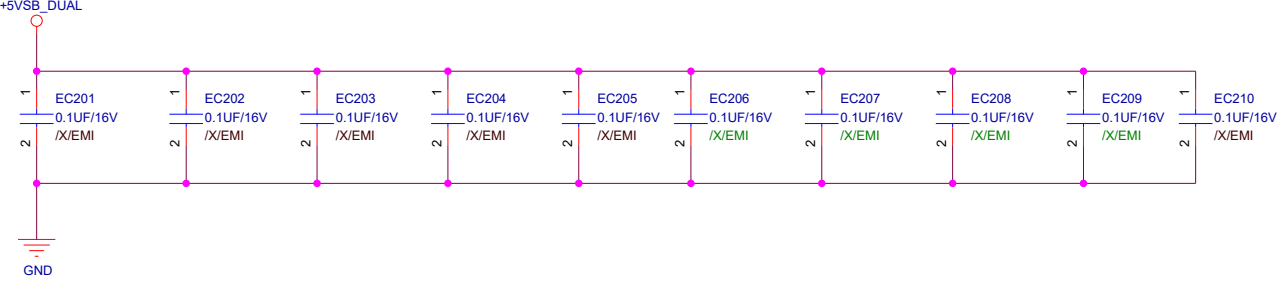

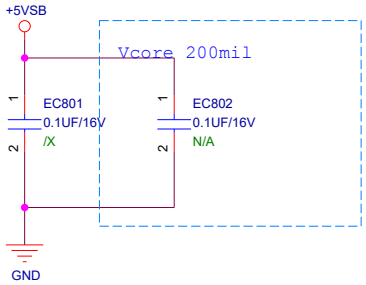

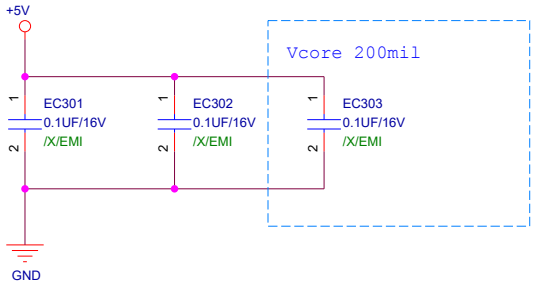

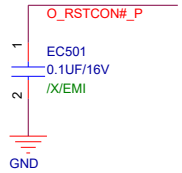

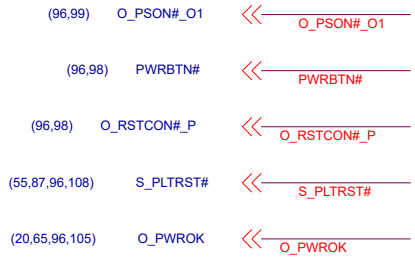

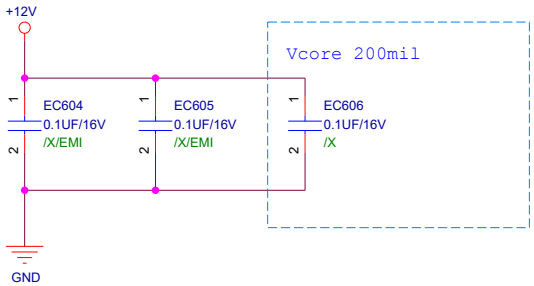

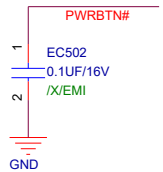

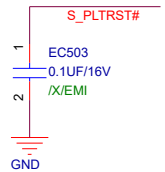

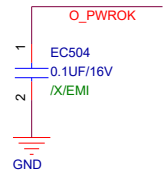

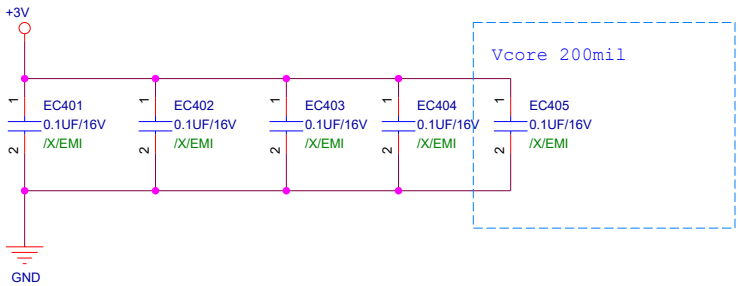

Title	<Title>	
Size A4	Document Number <Doc>	Rev <RevCode>
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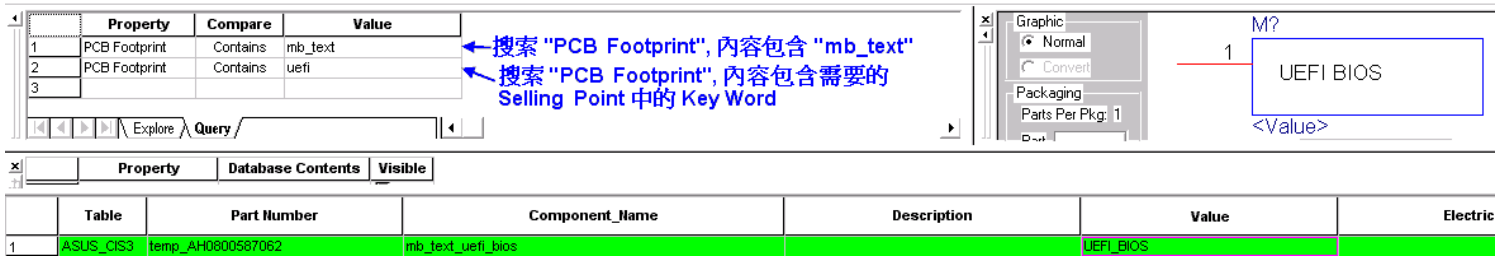
Selling Point

1. Selling Point 新增流程及窗口人員

2. 如何抓取 Selling Point Part, 如下圖



3. Example

ASUS PCB Logo Circuit

A. Choose ASUS Logo by Project

B. Choose KCC Logo by Project

C. Keep or remove NEED_COMP_SILK by Project

A

LOGO2
FCC
FCC
/X

LOGO7
PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

PCB MADE IN CHINA

LOGO3
RCM
RCM
/X

LOGO9
CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

CAN ICES-3 (B)/NMB-3(B)

LOGO1
EMI_D33005_H
EMI_D33005_H
/X

D33005
RoHS

LOGO8
VCCI
VCCI
/X

LOGO5
WEEE_LOGO
WEEE_LOGO
/X

LOGO6
CE
CE
/X

LOGO11
SFIS_LABEL
SFIS_LABEL
/X

SFIS

B

10mm without Wifi

LOGO10
KC R-REM-MSQ-XXXXXXXXXXXXX
KC_R_REM_LOGO
/X

KCC Logo without Wifi

KCC Logo with Wifi

<Variant Name>

ASUSTEK COMPUTER INC	Title : PCB Logo	
	Engineer: SZ Design IP	
Size: A3	Project Name: Silkscreen Demo Circuit	Rev: 1.0C
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Note :

1.Symbol value is not dispaly in layout

2.Symbol part reference change by project,

modify layout delete it, that put M.2 name to this place

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Size: A3	Document Number: <Doc>	Rev: <RevCode>
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<Variant Name>

Title: SPTH EUP Control

ASUSTeK COMPUTER INC

Engineer: Morse_Peng

Size	Project Name	Rev
A3	SkyLake VC	R1.00

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CHA_FAN Circuit use Single Resistor

A. Choose QFAN Mode Type by Project

B. If choose PWM Mode, choose with FAN RGB Header or not by Project

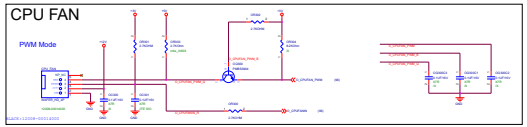
C. Remove CPU_OPT if don't need

D. Choose O_PWROK or O_PWROK_SB by Platform for FAN Expert 3 and above Mode

E. Modify Part Number of CPU_FAN & CPU_OPT by Color

A.1

PWM Mode **B.1**



Title : CPU_FAN

Engineer: 1st Design IP

Super I/O Dome Circuit

Title <Title>		
Size D	Document Number <Doc>	Rev <RevCode>
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<Variant Name>

Title : DVI REDUCED LEV-SHIFT

ASUSTek COMPUTER INC.

Engineer: Morse_Peng

Size	Project Name	Rev
A3	SkyLake VC	R1.00

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<Variant Name>

Title : DVI REDUCED LEV-SHIFT

ASUSTek COMPUTER INC.

Engineer: Morse_Peng

Size	Project Name	Rev
A2	SkyLake VC	R1.00

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<Variant Name>

Title : PS_ON#

ASUSTEK COMPUTER INC

Engineer: Jay_Tong

Size	Project Name	Rev
A3	Chipset Demo Circuit	0.0

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<Variant Name>

Title : DVI REDUCED LEV-SHIFT

ASUSTek COMPUTER INC.

Engineer: Morse_Peng

Size	Project Name	Rev
A2	SkyLake VC	R1.00

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<Variant Name>

Title : NA

ASUSTek COMPUTER INC.

Engineer: Mandy_cao

Size	Project Name	Rev
A	KabyLake DEMO	R1.00

Date:	Monday, June 11, 2018	Sheet	27	of	113

<Variant Name>

Title : NA

ASUSTek COMPUTER INC.

Engineer: Mandy_cao

Size	Project Name	Rev
A	KabyLake DEMO	R1.00

Date:	Monday, June 11, 2018	Sheet	28	of	113

<Variant Name>

Title : NA

ASUSTek COMPUTER INC.

Engineer: Mandy_cao

Size	Project Name	Rev
A	KabyLake DEMO	R1.00

Date:	Monday, June 11, 2018	Sheet	29	of	113

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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<Variant Name>

ASUSTEK COMPUTER INC	Title : USB3 Port	
	Engineer: Kell_Huang	
Size: A2	Project Name: **Chipset USB Demo Circuit**	Rev: 0.0
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<Variant Name>

ASUSTek COMPUTER INC.	Title : NA	
	Engineer: Mandy_cao	
Size: A	Project Name: KabyLake DEMO	Rev: R1.00
Date: Monday, June 11, 2018	Sheet 14 of 113	

<Variant Name>

Title : +3V_S0IX/+5V_S0IX/+12V_S0IX

ASUSTEK COMPUTER INC

Engineer: Mandy_Cao

Size	Project Name	Rev
A2	coffeelake demo	0.0

Date:	Monday, June 11, 2018	Sheet	22	of	113

<Variant Name>

Title : NA

ASUSTek COMPUTER INC.

Engineer: Mandy_cao

Size	Project Name	Rev
A	KabyLake DEMO	R1.00

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Title : +5VSB_DUAL/+1.1VSB

Engineer:

ASUSTek Computer Inc.

Size	Project Name	Rev
A2	FM2 PLUS	1.00

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<Variant Name>

Title : NA

ASUSTek COMPUTER INC.

Engineer: Mandy_cao

Size	Project Name	Rev
A	KabyLake DEMO	R1.00

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<Variant Name>

Title : DVI REDUCED LEV-SHIFT

ASUSTek COMPUTER INC.

Engineer: Morse_Peng

Size	Project Name	Rev
A1	SkyLake VC	R1.00

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<Variant Name>

Title :

Engineer:

ASUSTek COMPUTER INC.

Size	Project Name	Rev
A3		R1.00

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Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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Title <Title>		
Size D	Document Number <Doc>	Rev <RevCode>
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Title <Title>		
Size A2	Document Number <Doc>	Rev <RevCode>
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