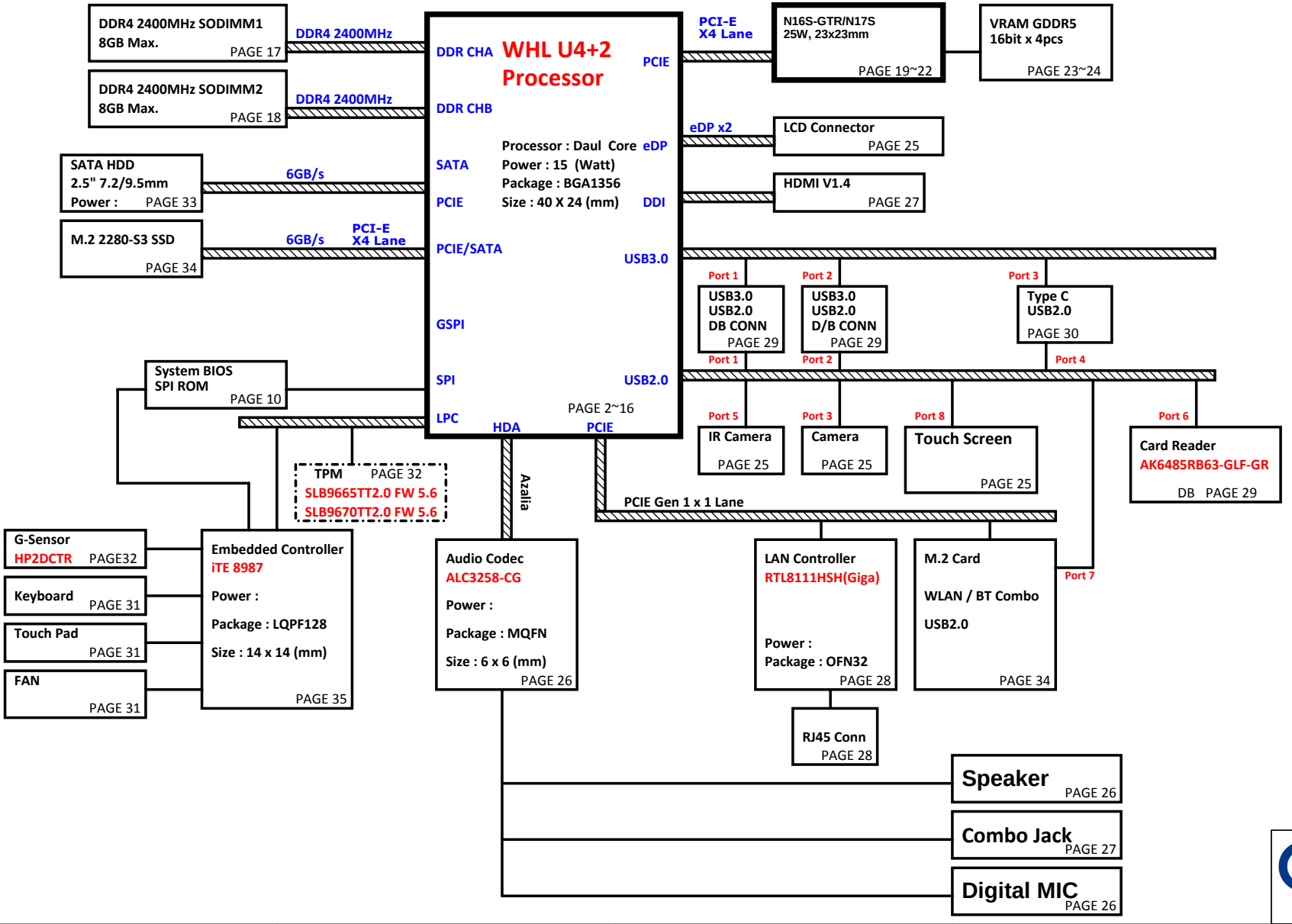
G7BD 1SPD DIS/UMA 15"
Intel WLH-U Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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+3V <4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47>
+1.05V <6,35,41>
+VCCSTPLL <4,5,6,41,42>

HDMI

U30015A

<27> IN_D2# → IN_D2# AL5 DDI1_TXN_0
<27> IN_D2 → IN_D2 AL6 DDI1_TXP_0
<27> IN_D1# → IN_D1# AJ5 DDI1_TXN_1
<27> IN_D1 → IN_D1 AJ6 DDI1_TXP_1
<27> IN_D0# → IN_D0# AF6 DDI1_TXN_2
<27> IN_D0 → IN_D0 AF5 DDI1_TXP_2
<27> IN_CLK# → IN_CLK# AE5 DDI1_TXN_3
<27> IN_CLK → IN_CLK AE6 DDI1_TXP_3

AC4 DDI2_TXN_0
AC3 DDI2_TXP_0
AC1 DDI2_TXN_1
AC2 DDI2_TXP_1
AE4 DDI2_TXN_2
AE3 DDI2_TXP_2
AE1 DDI2_TXN_3
AE2 DDI2_TXP_3

EDP_TXN_0 AG4 INT_EDP_TXN0 → INT_EDP_TXN0 <25>
EDP_TXP_0 AG3 INT_EDP_TXP0 → INT_EDP_TXP0 <25>
EDP_TXN_1 AG2 INT_EDP_TXN1 → INT_EDP_TXN1 <25>
EDP_TXP_1 AG1 INT_EDP_TXP1 → INT_EDP_TXP1 <25>
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1

EDP_AUX AH4 INT_EDP_AUXN → INT_EDP_AUXN <25>
EDP_AUX_P AH3 INT_EDP_AUXP → INT_EDP_AUXP <25>

DISP_UTILS AM7

DDI1_AUX AC7
DDI1_AUX_P AC6
DDI2_AUX AD4
DDI2_AUX_P AD3
DDI3_AUX AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_HPD_CON → HDMI_HPD_CON <27>
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7 ULT_EDP_HPD → ULT_EDP_HPD <25>

EDP_BKLTEN CK11 PCH_LVDS_BLON → PCH_LVDS_BLON <25>
EDP_VDDEN CG11 PCH_DISP_ON → PCH_DISP_ON <25>
EDP_BKLTCTL CH11 PCH_DPST_PWM → PCH_DPST_PWM <25>

DISP_RCOMP signals should be shorted near balls and routed with typical impedance <20 mohms

+VCCIO → R30233 24.9_1%_4 → EDP_RCOMP AM6 DISP_RCOMP

<27> SDVO_CLK → CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
<27> SDVO_DATA → CC9 GPP_E19/DPPB_CTRLDATA

CH4 GPP_E20/DPPC_CTRLCLK
CH3 GPP_E21/DPPC_CTRLDATA

CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA

CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

*CFL_U_43E_IL_IP_DDR4
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Reserve EDP_HPD opposites circuit!

ULT_EDP_HPD → R30274 100K_5%_4

PCH_DPST_PWM
PCH_LVDS_BLON
C91187 0.033u/16V_4
C91188 0.033u/16V_4
close SOC

JTAG_TDI_PCH → R30244 *0_4/S → XDP_TDI_CPU
JTAG_TDO_PCH → R30245 0_4/S → XDP_TDO_CPU
JTAG_TMS_PCH → R30243 0_4/S → XDP_TMS_CPU
XDP_TRST#_CPU → R30232 0_4/S → PROC_TRST#
JTAGX_PCH → R124543 0_4/S → XDP_TCK0
DCI Debug

Close to EC
+VCCSTPLL
PM_THRMTRIP# → R30249 1K_5%_4
Processor pull-up (CPU)

U30015D

+VCCSTPLL → R30250 *49.9/F_4 → CATERR#
CATERR# AA4
PECI AR1
PROCHOT# Y4
THRMTRIP# BJ1

<35,42> H_PROCHOT# → R30247 499_1%_4 → PROCHOT#
<35> EC_PECI → EC_PECI
<35> PM_THRMTRIP# → PM_THRMTRIP#

<16> XDP_BPM0 → U1 BPM#_0
<16> XDP_BPM1 → U2 BPM#_1
U3 BPM#_2
U4 BPM#_3

PROC_TCK T6 XDP_TCK0 → XDP_TCK0 <16>
PROC_TDI U6 XDP_TDI_CPU → XDP_TDI_CPU <16>
PROC_TDO Y5 XDP_TDO_CPU → XDP_TDO_CPU <16>
PROC_TMS T5 XDP_TMS_CPU → XDP_TMS_CPU <16>
PROC_TRST# AB6 PROC_TRST# → PROC_TRST# <16>

PCH_TCK W6 JTAG_TCK_PCH → JTAG_TCK_PCH <16>
PCH_TDI U5 JTAG_TDI_PCH → JTAG_TDI_PCH <16>
PCH_TDO W5 JTAG_TDO_PCH → JTAG_TDO_PCH <16>
PCH_TMS P5 JTAG_TMS_PCH → JTAG_TMS_PCH <16>
PCH_TRST# Y6 XDP_TRST#_CPU
PCH_JTAGX P6 JTAGX_PCH

CE9 GPP_E3/CPU_GP0 PROC_PREQ# W2 → XDP_PREQ#_CPU <16>
CN3 GPP_E7/CPU_GP1 PROC_PRDY# W1 → XDP_PRDY#_CPU <16>
CB34 GPP_B3/CPU_GP2
CC35 GPP_B4/CPU_GP3

PROC_POPIRCOMP BP27 ← R30083 49.9_1%_4 PROC_POPIRCOMP
PCH_OPIRCOMP BW25 ← R30131 49.9_1%_4 PCH_OPI_RCOMP
OPCE_RCOMP L5 ← R30241 49.9_1%_4 EDRAM_OPIO_RCOMP
OPC_RCOMP N5 ← R30265 49.9_1%_4 EOPIO_RCOMP

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*CFL_U_43E_IL_IP_DDR4

+1.05V → R30218 *1K_5%_4 → JTAGX_PCH
R30266 51_5%_4 JTAG_TMS_PCH
R30220 51_5%_4 JTAG_TDI_PCH
R30268 100_1%_4 JTAG_TDO_PCH
R30269 *51_5%_4 JTAG_TCK_PCH
Close to Chipset

PLACE NEAR CPU
+1.05V
XDP_TMS_CPU → R30219 *51_4
XDP_TDI_CPU → R30267 51_4
XDP_TDO_CPU → R30221 100_1%_4

+1.05V
H_PROCHOT# → R30222 1K_5%_4
XDP_TCK0 → R30242 51_5%_4
XDP_TRST#_CPU → R30231 *51_5%_4

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 1/15 eDP/DDI/MISC	1A

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WHL ULT Processor (DDR4)

<17> M_A_DQSN[7:0]
<17> M_A_DQSP[7:0]
<18> M_B_DQSN[7:0]
<18> M_B_DQSP[7:0]
<17> M_A_DQ[63:0]
<18> M_B_DQ[63:0]

+1.2VSUS <3,6,17,18,39,41>

WHL ULT Processor (MEM-A)

U30015B

M_A_DQ0	A26	DDR0_DQ_0/DDR0_DQ_0	DDR0_CKN_0/DDR0_CKN_0	V32	M_A_CLKN0 <17>
M_A_DQ1	D26	DDR0_DQ_1/DDR0_DQ_1	DDR0_CKP_0/DDR0_CKP_0	V31	M_A_CLKP0 <17>
M_A_DQ2	D28	DDR0_DQ_2/DDR0_DQ_2	DDR0_CKN_1/DDR0_CKN_1	T32	M_A_CLKN1 <17>
M_A_DQ3	C28	DDR0_DQ_3/DDR0_DQ_3	DDR0_CKP_1/DDR0_CKP_1	T31	M_A_CLKP1 <17>
M_A_DQ4	B26	DDR0_DQ_4/DDR0_DQ_4			
M_A_DQ5	C26	DDR0_DQ_5/DDR0_DQ_5	DDR0_CKE_0/DDR0_CKE_0	U36	M_A_CKE0 <17>
M_A_DQ6	B28	DDR0_DQ_6/DDR0_DQ_6	DDR0_CKE_1/DDR0_CKE_1	U37	M_A_CKE1 <17>
M_A_DQ7	A28	DDR0_DQ_7/DDR0_DQ_7	DDR0_CKE_2/NC	U34	
M_A_DQ8	B30	DDR0_DQ_8/DDR0_DQ_8	DDR0_CKE_3/NC	U35	
M_A_DQ9	D30	DDR0_DQ_9/DDR0_DQ_9			
M_A_DQ10	B33	DDR0_DQ_10/DDR0_DQ_10	DDR0_CS#_0/DDR0_CS#_0	AE32	M_A_CS#0 <17>
M_A_DQ11	D32	DDR0_DQ_11/DDR0_DQ_11	DDR0_CS#_1/DDR0_CS#_1	AF32	M_A_CS#1 <17>
M_A_DQ12	A30	DDR0_DQ_12/DDR0_DQ_12	DDR0_ODT_0/DDR0_ODT_0	AE31	M_A_DIM0_ODT0 <17>
M_A_DQ13	C30	DDR0_DQ_13/DDR0_DQ_13	NC/DDR0_ODT_1	AF31	M_A_DIM0_ODT1 <17>
M_A_DQ14	B32	DDR0_DQ_14/DDR0_DQ_14			
M_A_DQ15	C32	DDR0_DQ_15/DDR0_DQ_15	DDR0_CAB_9/DDR0_MA_0	AC37 M_A_A0	M_A_A0 <17>
M_A_DQ16	H37	DDR0_DQ_16/DDR0_DQ_32	DDR0_CAB_8/DDR0_MA_1	AC36 M_A_A1	M_A_A1 <17>
M_A_DQ17	H34	DDR0_DQ_17/DDR0_DQ_33	DDR0_CAB_5/DDR0_MA_2	AC34 M_A_A2	M_A_A2 <17>
M_A_DQ18	K34	DDR0_DQ_18/DDR0_DQ_34	NC/DDR0_MA_3	AC35 M_A_A3	M_A_A3 <17>
M_A_DQ19	K35	DDR0_DQ_19/DDR0_DQ_35	NC/DDR0_MA_4	AA35 M_A_A4	M_A_A4 <17>
M_A_DQ20	H36	DDR0_DQ_20/DDR0_DQ_36	DDR0_CAA_0/DDR0_MA_5	AB35 M_A_A5	M_A_A5 <17>
M_A_DQ21	H35	DDR0_DQ_21/DDR0_DQ_37	DDR0_CAA_2/DDR0_MA_6	AA37 M_A_A6	M_A_A6 <17>
M_A_DQ22	K36	DDR0_DQ_22/DDR0_DQ_38	DDR0_CAA_4/DDR0_MA_7	AA36 M_A_A7	M_A_A7 <17>
M_A_DQ23	K37	DDR0_DQ_23/DDR0_DQ_39	DDR0_CAA_3/DDR0_MA_8	AB34 M_A_A8	M_A_A8 <17>
M_A_DQ24	N36	DDR0_DQ_24/DDR0_DQ_40	DDR0_CAA_1/DDR0_MA_9	W36 M_A_A9	M_A_A9 <17>
M_A_DQ25	N34	DDR0_DQ_25/DDR0_DQ_41	DDR0_CAB_7/DDR0_MA_10	Y31 M_A_A10	M_A_A10 <17>
M_A_DQ26	R37	DDR0_DQ_26/DDR0_DQ_42	DDR0_CAA_7/DDR0_MA_11	W34 M_A_A11	M_A_A11 <17>
M_A_DQ27	R34	DDR0_DQ_27/DDR0_DQ_43	DDR0_CAA_6/DDR0_MA_12	AA34 M_A_A12	M_A_A12 <17>
M_A_DQ28	N37	DDR0_DQ_28/DDR0_DQ_44	DDR0_CAB_0/DDR0_MA_13	AC32 M_A_A13	M_A_A13 <17>
M_A_DQ29	N35	DDR0_DQ_29/DDR0_DQ_45			
M_A_DQ30	R36	DDR0_DQ_30/DDR0_DQ_46	DDR0_CAB_2/DDR0_MA_14	AC31	
M_A_DQ31	R35	DDR0_DQ_31/DDR0_DQ_47	DDR0_CAB_1/DDR0_MA_15	AB32	M_A_WE# <17>
M_A_DQ32	AN35	DDR0_DQ_32/DDR1_DQ_0	DDR0_CAB_3/DDR0_MA_16	Y32	M_A_CAS# <17>
M_A_DQ33	AN34	DDR0_DQ_33/DDR1_DQ_1			M_A_RAS# <17>
M_A_DQ34	AR35	DDR0_DQ_34/DDR1_DQ_2	DDR0_CAB_4/DDR0_BA_0	W32	
M_A_DQ35	AR34	DDR0_DQ_35/DDR1_DQ_3	DDR0_CAB_6/DDR0_BA_1	AB31	M_A_BS#0 <17>
M_A_DQ36	AN37	DDR0_DQ_36/DDR1_DQ_4	DDR0_CAA_5/DDR0_BG_0	V34	M_A_BS#1 <17>
M_A_DQ37	AN36	DDR0_DQ_37/DDR1_DQ_5			M_A_BG#0 <17>
M_A_DQ38	AR36	DDR0_DQ_38/DDR1_DQ_6	DDR0_CAA_8/DDR0_ACT#	V35	
M_A_DQ39	AR37	DDR0_DQ_39/DDR1_DQ_7	DDR0_CAA_9/DDR0_BG_1	W35	M_A_ACT# <17>
M_A_DQ40	AU35	DDR0_DQ_40/DDR1_DQ_8			M_A_BG#1 <17>
M_A_DQ41	AU34	DDR0_DQ_41/DDR1_DQ_9	DDR0_DQSN_0/DDR0_DQSN_0	C27 M_A_DQSN0	
M_A_DQ42	AW35	DDR0_DQ_42/DDR1_DQ_10	DDR0_DQSP_0/DDR0_DQSP_0	D27 M_A_DQSP0	
M_A_DQ43	AW34	DDR0_DQ_43/DDR1_DQ_11	DDR0_DQSN_1/DDR0_DQSN_1	D31 M_A_DQSN1	
M_A_DQ44	AU37	DDR0_DQ_44/DDR1_DQ_12	DDR0_DQSP_1/DDR0_DQSP_1	C31 M_A_DQSP1	
M_A_DQ45	AU36	DDR0_DQ_45/DDR1_DQ_13	DDR0_DQSN_2/DDR0_DQSN_4	J35 M_A_DQSN2	
M_A_DQ46	AW36	DDR0_DQ_46/DDR1_DQ_14	DDR0_DQSP_2/DDR0_DQSP_4	J34 M_A_DQSP2	
M_A_DQ47	AW37	DDR0_DQ_47/DDR1_DQ_15	DDR0_DQSN_3/DDR0_DQSN_5	P34 M_A_DQSN3	
M_A_DQ48	BA35	DDR0_DQ_48/DDR1_DQ_32	DDR0_DQSP_3/DDR0_DQSP_5	P35 M_A_DQSP3	
M_A_DQ49	BA34	DDR0_DQ_49/DDR1_DQ_33	DDR0_DQSN_4/DDR1_DQSN_0	AP35 M_A_DQSN4	
M_A_DQ50	BC35	DDR0_DQ_50/DDR1_DQ_34	DDR0_DQSP_4/DDR1_DQSP_0	AP34 M_A_DQSP4	
M_A_DQ51	BC34	DDR0_DQ_51/DDR1_DQ_35	DDR0_DQSN_5/DDR1_DQSN_1	AV34 M_A_DQSN5	
M_A_DQ52	BA37	DDR0_DQ_52/DDR1_DQ_36	DDR0_DQSP_5/DDR1_DQSP_1	AV35 M_A_DQSP5	
M_A_DQ53	BA36	DDR0_DQ_53/DDR1_DQ_37	DDR0_DQSN_6/DDR1_DQSN_4	BB35 M_A_DQSN6	
M_A_DQ54	BC36	DDR0_DQ_54/DDR1_DQ_38	DDR0_DQSP_6/DDR1_DQSP_4	BB34 M_A_DQSP6	
M_A_DQ55	BC37	DDR0_DQ_55/DDR1_DQ_39	DDR0_DQSN_7/DDR1_DQSN_5	BF34 M_A_DQSN7	
M_A_DQ56	BE35	DDR0_DQ_56/DDR1_DQ_40	DDR0_DQSP_7/DDR1_DQSP_5	BF35 M_A_DQSP7	
M_A_DQ57	BE34	DDR0_DQ_57/DDR1_DQ_41			
M_A_DQ58	BG35	DDR0_DQ_58/DDR1_DQ_42	NC/DDR0_ALERT#	W37 M_A_ALERT#	M_A_ALERT# <17>
M_A_DQ59	BG34	DDR0_DQ_59/DDR1_DQ_43	NC/DDR0_PAR	W31 M_A_PARITY	M_A_PARITY <17>
M_A_DQ60	BE37	DDR0_DQ_60/DDR1_DQ_44			
M_A_DQ61	BE36	DDR0_DQ_61/DDR1_DQ_45	DDR_VREF_CA	F36 SM_VREF	SM_VREF <17>
M_A_DQ62	BG36	DDR0_DQ_62/DDR1_DQ_46	DDR0_VREF_DQ_0	D35	
M_A_DQ63	BG37	DDR0_DQ_63/DDR1_DQ_47	DDR0_VREF_DQ_1	D37	
			DDR1_VREF_DQ	E36 SMDDR_VREF_DQ1_M3	SMDDR_VREF_DQ1_M3 <18>
			DDR_VTT_CNTL	C35 DDR_VTT_CNTL	TP30088

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*CFL_U_43E_IL_IP_DDR4

WHL ULT Processor (MEM-B)

U30015C

M_B_DQ0	J22	DDR1_DQ_0/DDR0_DQ_16	DDR1_CKN_0/DDR1_CKN_0	AF28	M_B_CLKN0 <18>
M_B_DQ1	H25	DDR1_DQ_1/DDR0_DQ_17	DDR1_CKP_0/DDR1_CKP_0	AF29	M_B_CLKP0 <18>
M_B_DQ2	G22	DDR1_DQ_2/DDR0_DQ_18	DDR1_CKN_1/DDR1_CKN_1	AE28	M_B_CLKN1 <18>
M_B_DQ3	H22	DDR1_DQ_3/DDR0_DQ_19	DDR1_CKP_1/DDR1_CKP_1	AE29	M_B_CLKP1 <18>
M_B_DQ4	F25	DDR1_DQ_4/DDR0_DQ_20			
M_B_DQ5	J25	DDR1_DQ_5/DDR0_DQ_21	DDR1_CKE_0/DDR1_CKE_0	T28	M_B_CKE0 <18>
M_B_DQ6	G25	DDR1_DQ_6/DDR0_DQ_22	DDR1_CKE_1/DDR1_CKE_1	T29	M_B_CKE1 <18>
M_B_DQ7	F22	DDR1_DQ_7/DDR0_DQ_23	DDR1_CKE_2/NC	V28	
M_B_DQ8	D22	DDR1_DQ_8/DDR0_DQ_24	DDR1_CKE_3/NC	V29	
M_B_DQ9	C22	DDR1_DQ_9/DDR0_DQ_25			
M_B_DQ10	C24	DDR1_DQ_10/DDR0_DQ_26	DDR1_CS#_0/DDR1_CS#_0	AL37	M_B_CS#0 <18>
M_B_DQ11	D24	DDR1_DQ_11/DDR0_DQ_27	DDR1_CS#_1/DDR1_CS#_1	AL35	M_B_CS#1 <18>
M_B_DQ12	A22	DDR1_DQ_12/DDR0_DQ_28	DDR1_ODT_0/DDR1_ODT_0	AL36	M_B_DIM0_ODT0 <18>
M_B_DQ13	B22	DDR1_DQ_13/DDR0_DQ_29	NC/DDR1_ODT_1	AL34	M_B_DIM0_ODT1 <18>
M_B_DQ14	A24	DDR1_DQ_14/DDR0_DQ_30	DDR1_CAB_9/DDR1_MA_0	AG36 M_B_A0	M_B_A0 <18>
M_B_DQ15	B24	DDR1_DQ_15/DDR0_DQ_31	DDR1_CAB_8/DDR1_MA_1	AG35 M_B_A1	M_B_A1 <18>
M_B_DQ16	G31	DDR1_DQ_16/DDR0_DQ_48	DDR1_CAB_5/DDR1_MA_2	AF34 M_B_A2	M_B_A2 <18>
M_B_DQ17	G32	DDR1_DQ_17/DDR0_DQ_49	NC/DDR1_MA_3	AG37 M_B_A3	M_B_A3 <18>
M_B_DQ18	H29	DDR1_DQ_18/DDR0_DQ_50	NC/DDR1_MA_4	AE35 M_B_A4	M_B_A4 <18>
M_B_DQ19	H28	DDR1_DQ_19/DDR0_DQ_51	DDR1_CAA_0/DDR1_MA_5	AF35 M_B_A5	M_B_A5 <18>
M_B_DQ20	G28	DDR1_DQ_20/DDR0_DQ_52	DDR1_CAA_2/DDR1_MA_6	AE37 M_B_A6	M_B_A6 <18>
M_B_DQ21	G29	DDR1_DQ_21/DDR0_DQ_53	DDR1_CAA_4/DDR1_MA_7	AC29 M_B_A7	M_B_A7 <18>
M_B_DQ22	H31	DDR1_DQ_22/DDR0_DQ_54	DDR1_CAA_3/DDR1_MA_8	AE36 M_B_A8	M_B_A8 <18>
M_B_DQ23	H32	DDR1_DQ_23/DDR0_DQ_55	DDR1_CAA_1/DDR1_MA_9	AB29 M_B_A9	M_B_A9 <18>
M_B_DQ24	L31	DDR1_DQ_24/DDR0_DQ_56	DDR1_CAB_7/DDR1_MA_10	AG34 M_B_A10	M_B_A10 <18>
M_B_DQ25	L32	DDR1_DQ_25/DDR0_DQ_57	DDR1_CAA_7/DDR1_MA_11	AC28 M_B_A11	M_B_A11 <18>
M_B_DQ26	N29	DDR1_DQ_26/DDR0_DQ_58	DDR1_CAA_6/DDR1_MA_12	AB28 M_B_A12	M_B_A12 <18>
M_B_DQ27	N28	DDR1_DQ_27/DDR0_DQ_59	DDR1_CAB_0/DDR1_MA_13	AK35 M_B_A13	M_B_A13 <18>
M_B_DQ28	L28	DDR1_DQ_28/DDR0_DQ_60			
M_B_DQ29	L29	DDR1_DQ_29/DDR0_DQ_61	DDR1_CAB_2/DDR1_MA_14	AJ35	
M_B_DQ30	N31	DDR1_DQ_30/DDR0_DQ_62	DDR1_CAB_1/DDR1_MA_15	AK34	M_B_WE# <18>
M_B_DQ31	N32	DDR1_DQ_31/DDR0_DQ_63	DDR1_CAB_3/DDR1_MA_16	AJ34	M_B_CAS# <18>
M_B_DQ32	AJ29	DDR1_DQ_32/DDR1_DQ_16			M_B_RAS# <18>
M_B_DQ33	AJ30	DDR1_DQ_33/DDR1_DQ_17	DDR1_CAB_4/DDR1_BA_0	AJ37	
M_B_DQ34	AM32	DDR1_DQ_34/DDR1_DQ_18	DDR1_CAB_6/DDR1_BA_1	AJ36	M_B_BS#0 <18>
M_B_DQ35	AM31	DDR1_DQ_35/DDR1_DQ_19	DDR1_CAA_5/DDR1_BG_0	W29	M_B_BS#1 <18>
M_B_DQ36	AM30	DDR1_DQ_36/DDR1_DQ_20			M_B_BG#0 <18>
M_B_DQ37	AM29	DDR1_DQ_37/DDR1_DQ_21	DDR1_CAA_9/DDR1_BG_1	Y28	
M_B_DQ38	AJ31	DDR1_DQ_38/DDR1_DQ_22	DDR1_CAA_8/DDR1_ACT#	W28	M_B_BG#1 <18>
M_B_DQ39	AJ32	DDR1_DQ_39/DDR1_DQ_23			M_B_ACT# <18>
M_B_DQ40	AR31	DDR1_DQ_40/DDR1_DQ_24	DDR1_DQSN_0/DDR0_DQSN_2	H24 M_B_DQSN0	
M_B_DQ41	AR32	DDR1_DQ_41/DDR1_DQ_25	DDR1_DQSP_0/DDR0_DQSP_2	G24 M_B_DQSP0	
M_B_DQ42	AV30	DDR1_DQ_42/DDR1_DQ_26	DDR1_DQSN_1/DDR0_DQSN_3	C23 M_B_DQSN1	
M_B_DQ43	AV29	DDR1_DQ_43/DDR1_DQ_27	DDR1_DQSP_1/DDR0_DQSP_3	D23 M_B_DQSP1	
M_B_DQ44	AR30	DDR1_DQ_44/DDR1_DQ_28	DDR1_DQSN_2/DDR0_DQSN_6	G30 M_B_DQSN2	
M_B_DQ45	AR29	DDR1_DQ_45/DDR1_DQ_29	DDR1_DQSP_2/DDR0_DQSP_6	H30 M_B_DQSP2	
M_B_DQ46	AV32	DDR1_DQ_46/DDR1_DQ_30	DDR1_DQSN_3/DDR0_DQSN_7	L30 M_B_DQSN3	
M_B_DQ47	AV31	DDR1_DQ_47/DDR1_DQ_31	DDR1_DQSP_3/DDR0_DQSP_7	N30 M_B_DQSP3	
M_B_DQ48	BA32	DDR1_DQ_48/DDR1_DQ_48	DDR1_DQSN_4/DDR1_DQSN_2	AL31 M_B_DQSN4	
M_B_DQ49	BA31	DDR1_DQ_49/DDR1_DQ_49	DDR1_DQSP_4/DDR1_DQSP_2	AL30 M_B_DQSP4	
M_B_DQ50	BD31	DDR1_DQ_50/DDR1_DQ_50	DDR1_DQSN_5/DDR1_DQSN_3	AU31 M_B_DQSN5	
M_B_DQ51	BD32	DDR1_DQ_51/DDR1_DQ_51	DDR1_DQSP_5/DDR1_DQSP_3	AU30 M_B_DQSP5	
M_B_DQ52	BA30	DDR1_DQ_52/DDR1_DQ_52	DDR1_DQSN_6/DDR1_DQSN_6	BC31 M_B_DQSN6	
M_B_DQ53	BA29	DDR1_DQ_53/DDR1_DQ_53	DDR1_DQSP_6/DDR1_DQSP_6	BC30 M_B_DQSP6	
M_B_DQ54	BD29	DDR1_DQ_54/DDR1_DQ_54	DDR1_DQSN_7/DDR1_DQSN_7	BH31 M_B_DQSN7	
M_B_DQ55	BD30	DDR1_DQ_55/DDR1_DQ_55	DDR1_DQSP_7/DDR1_DQSP_7	BH30 M_B_DQSP7	
M_B_DQ56	BG31	DDR1_DQ_56/DDR1_DQ_56			
M_B_DQ57	BG32	DDR1_DQ_57/DDR1_DQ_57	NC/DDR1_ALERT#	Y29 M_B_ALERT#	M_B_ALERT# <18>
M_B_DQ58	BK32	DDR1_DQ_58/DDR1_DQ_58	NC/DDR1_PAR	AE34 M_B_PARITY	M_B_PARITY <18>
M_B_DQ59	BK31	DDR1_DQ_59/DDR1_DQ_59	DRAM_RESET#	BU31	
M_B_DQ60	BG29	DDR1_DQ_60/DDR1_DQ_60			
M_B_DQ61	BG30	DDR1_DQ_61/DDR1_DQ_61	DDR_COMP_0	BN28 SM_RCOMP_0	R30087 121_1%_4
M_B_DQ62	BK30	DDR1_DQ_62/DDR1_DQ_62	DDR_COMP_1	BN27 SM_RCOMP_1	R30086 80.6_1%_4
M_B_DQ63	BK29	DDR1_DQ_63/DDR1_DQ_63	DDR_COMP_2	BN29 SM_RCOMP_2	R30095 100_1%_4

3 of 20

*CFL_U_43E_IL_IP_DDR4

+1.2VSUS

R30143 470_1%_4

R30144 *0_4/S DDR4_DRAMRST# <17,18>

DDR4_DRAMRST#

C30265 0.1u/16V_4

Layout: DDR Rcomp need follow Intel Spec 15 mil trance length

+1.2VSUS <3,6,17,18,39,41>
+3V_DEEP_SUS <4,10,11,13,14,15,16,32>

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 2/15(DDR4 I/F)	1A

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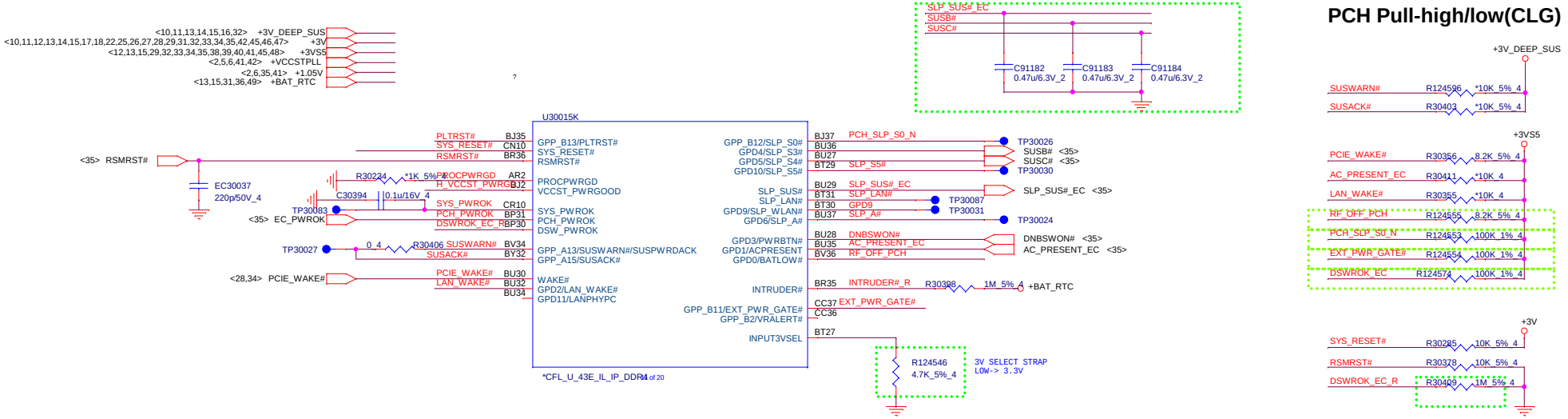
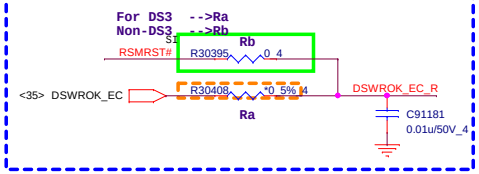
PCH Pull-high/low(CLG)

04



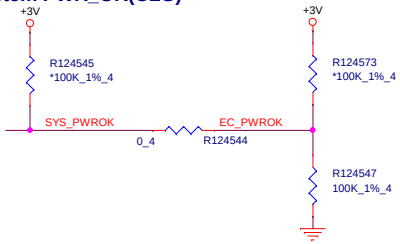
For DS3 Sequence

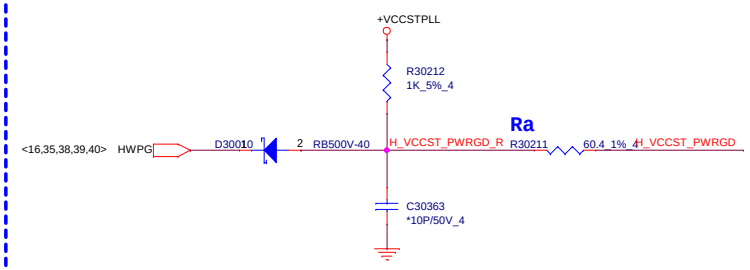


PLTRST#(CLG)

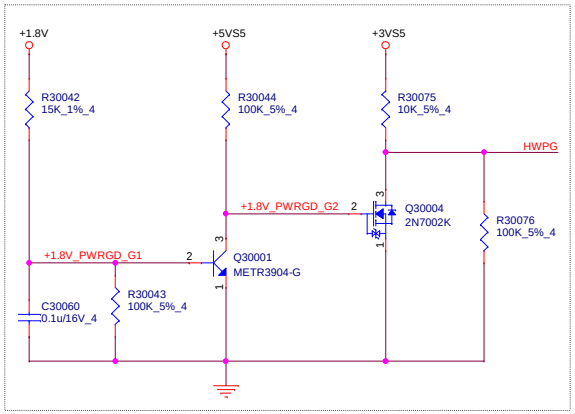
Check Rise/Fall time less than 100ns

System PWR_OK(CLG)





Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 3/15(PowerManger)	1A

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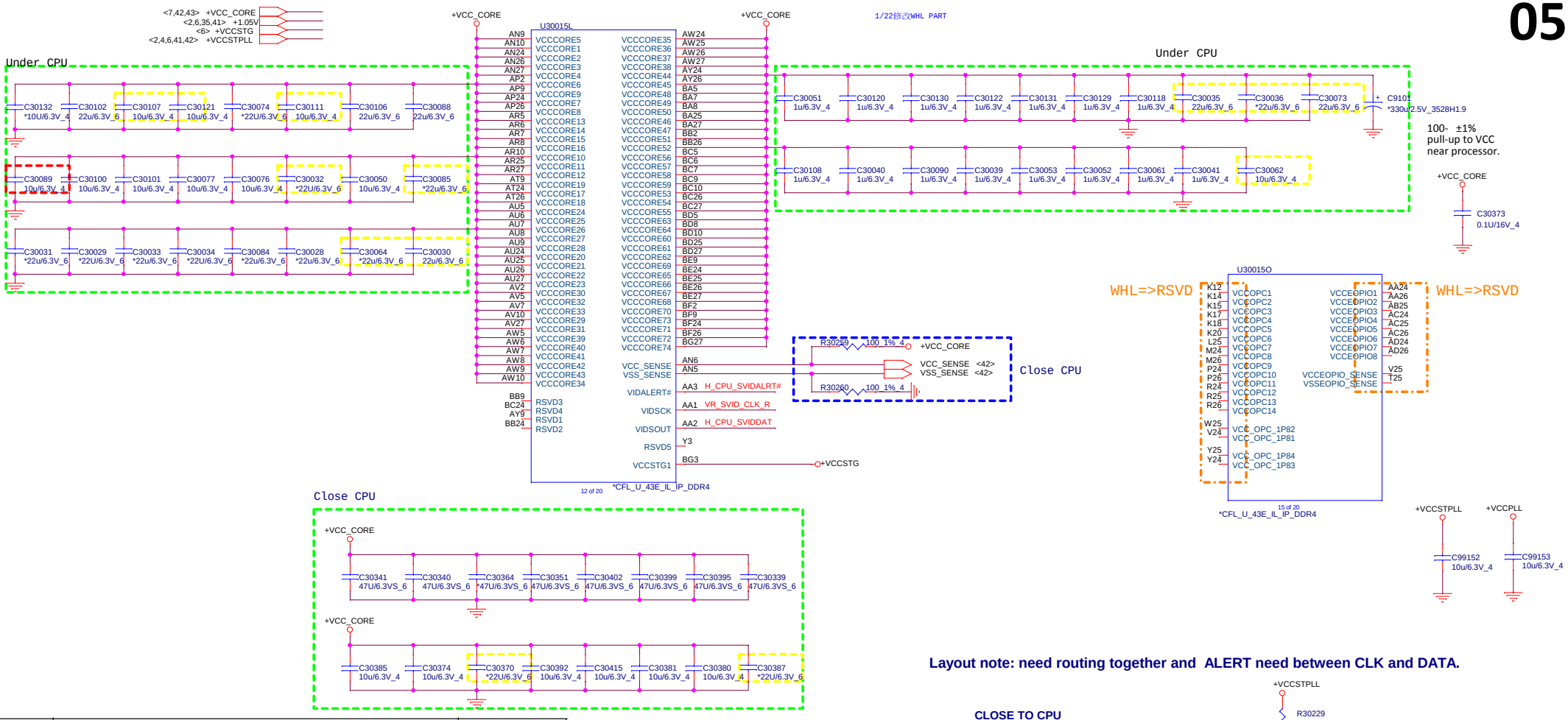
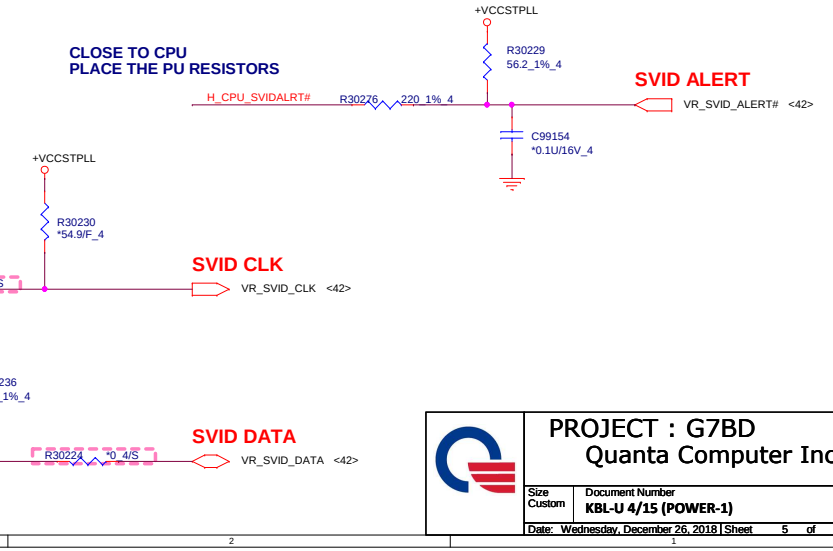


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Layout note: need routing together and ALERT need between CLK and DATA.



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 4/15 (POWER-1)	1A

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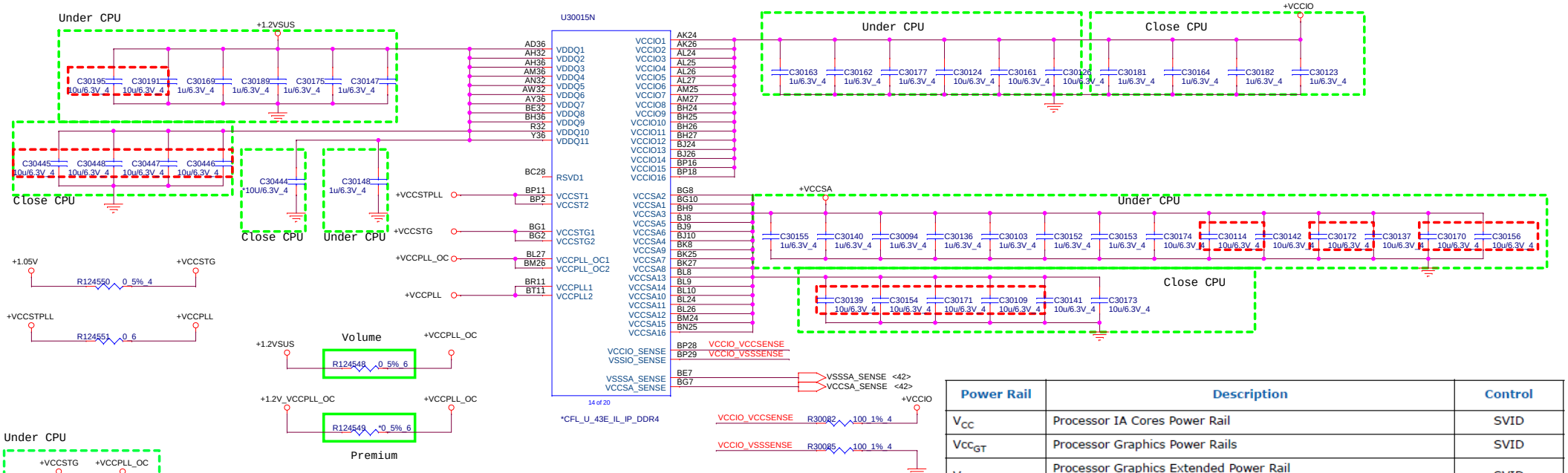
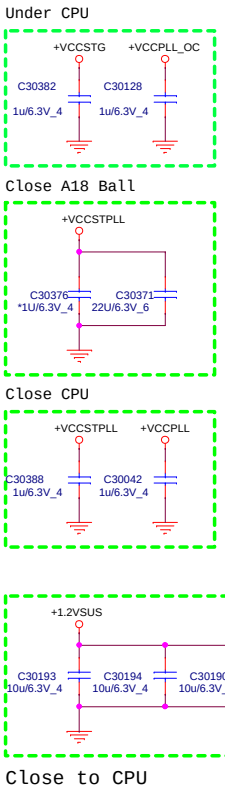
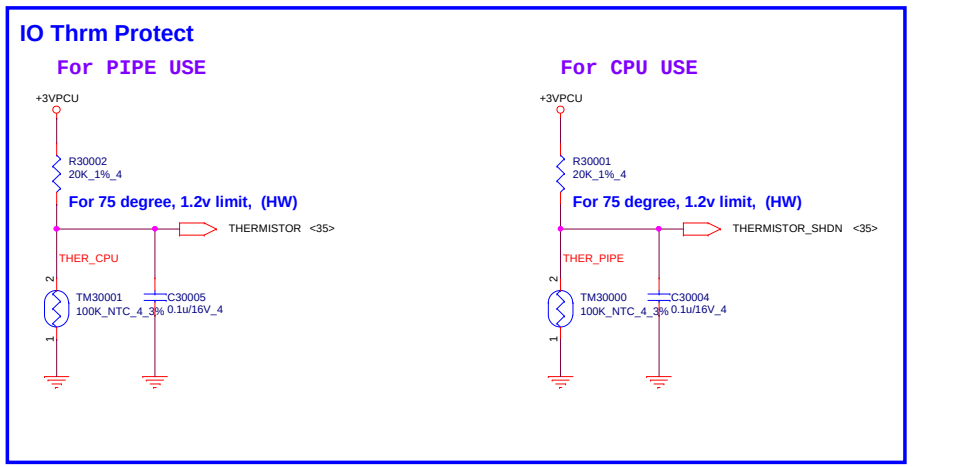
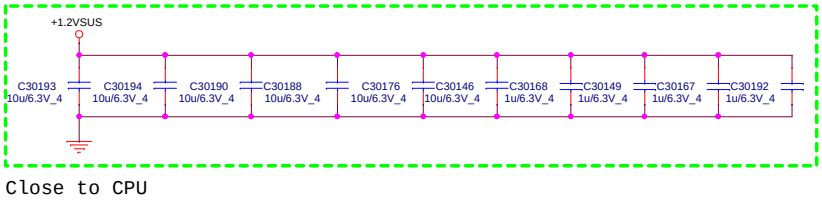
+VCCSTPLL <2,4,5,41,42>
+VCCSA <42,44>
+1.2VSUS <3,17,18,39,41>
+1.05V_DEEP_SUS <9,15,33,40,41>
+1.05V <2,35,41>
+3VPCU <13,31,34,35,36,38,49>



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed







PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 5/15 (POWER-2)	1A

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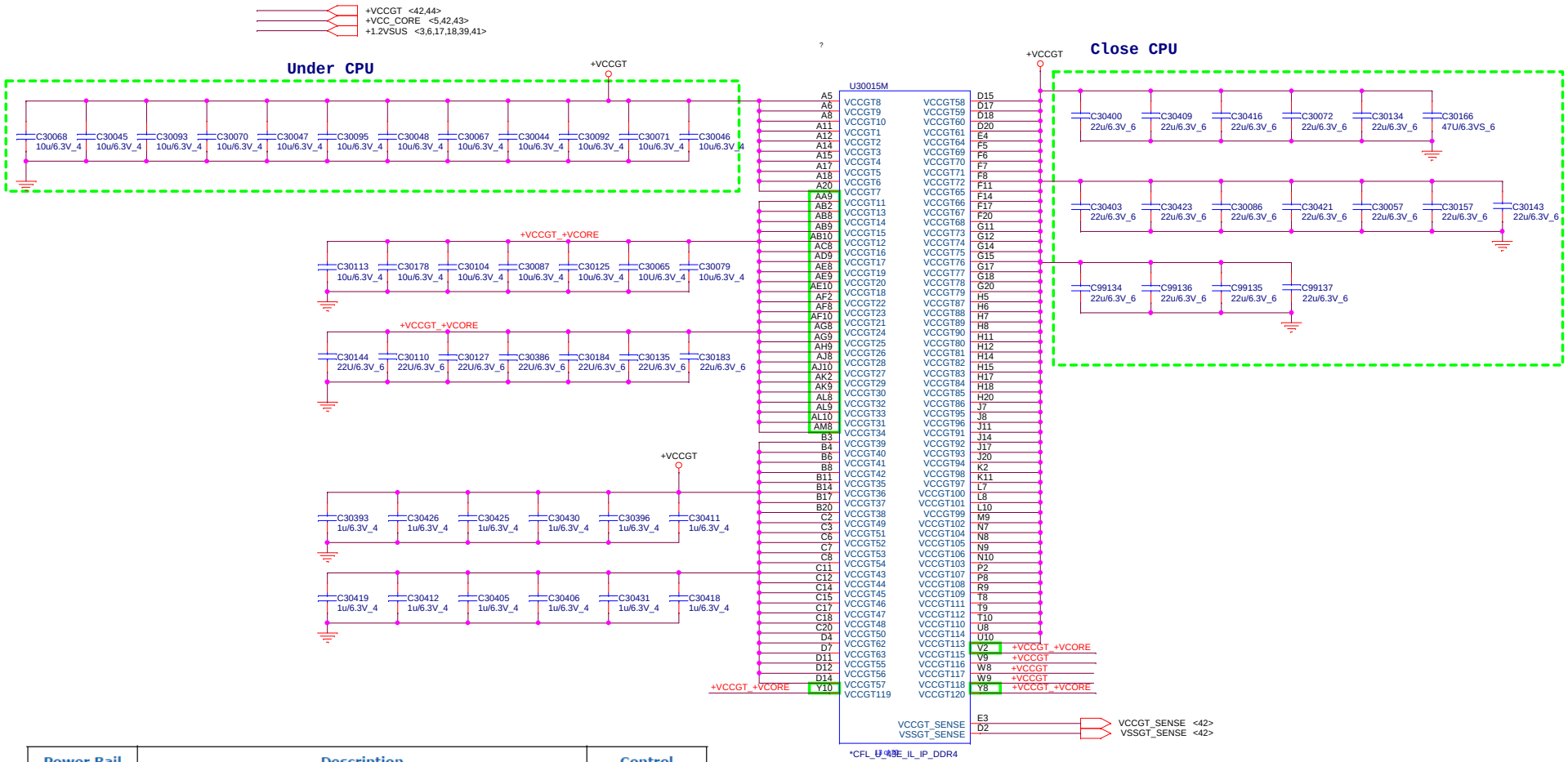
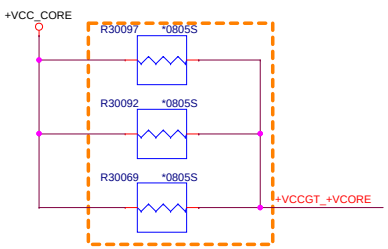
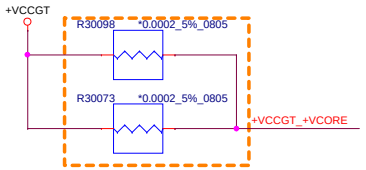


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



For WHL U42 ES2 上件/0122



For WHL U42 ES1 上件/0122

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 6/15 (POWER-3)	1A

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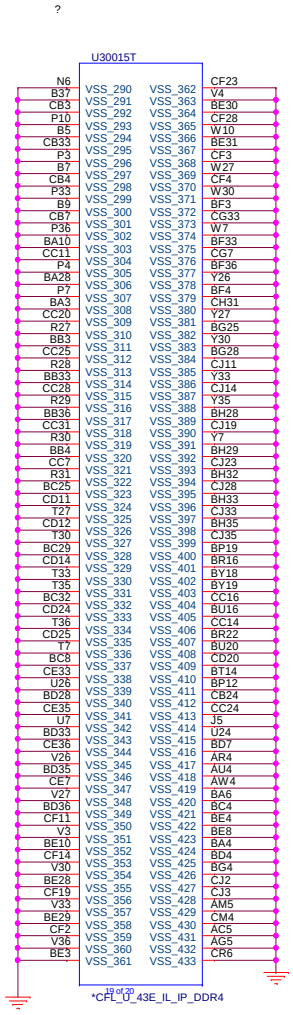

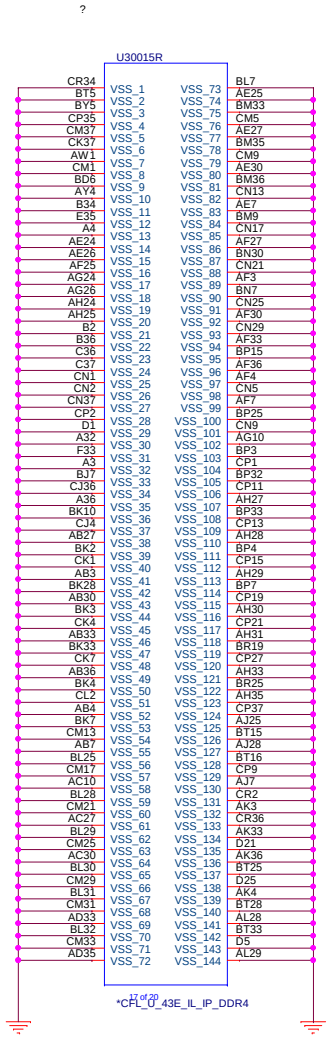

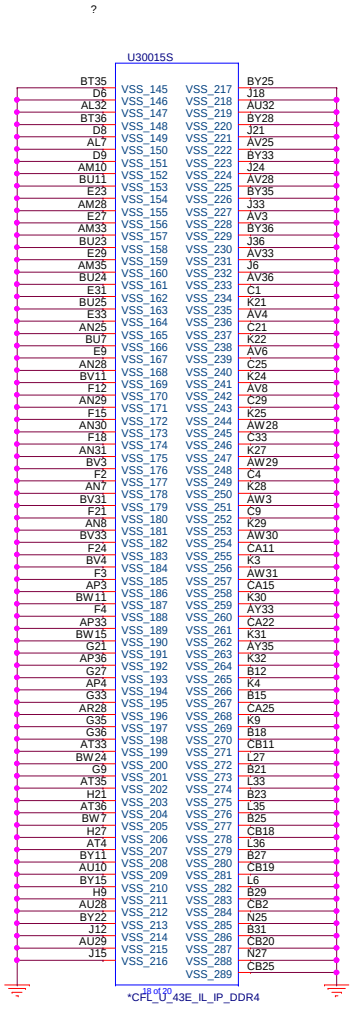

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 7/15 (GND)	1A

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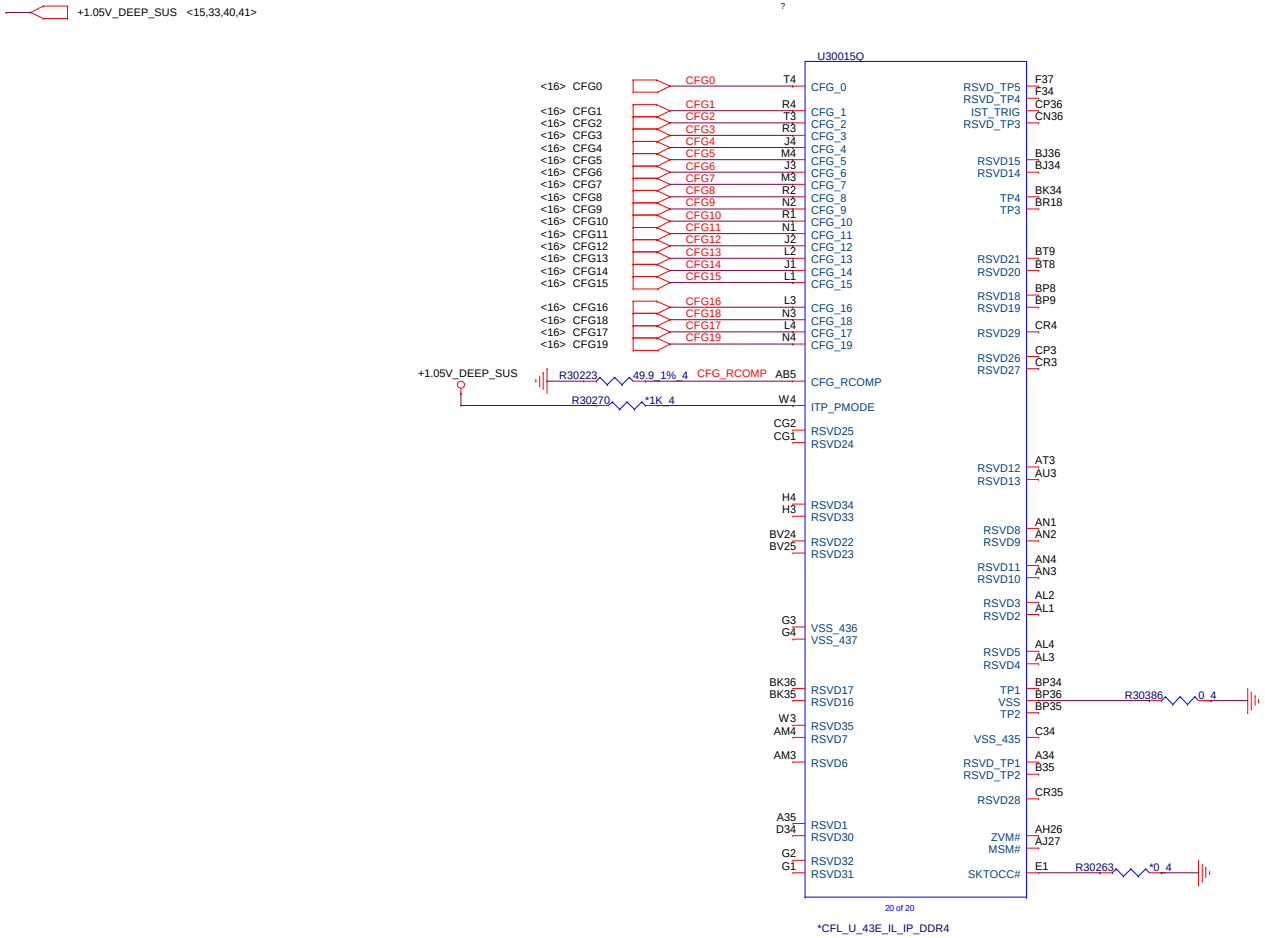
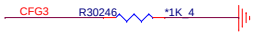


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 8/15 (RSV)	1A

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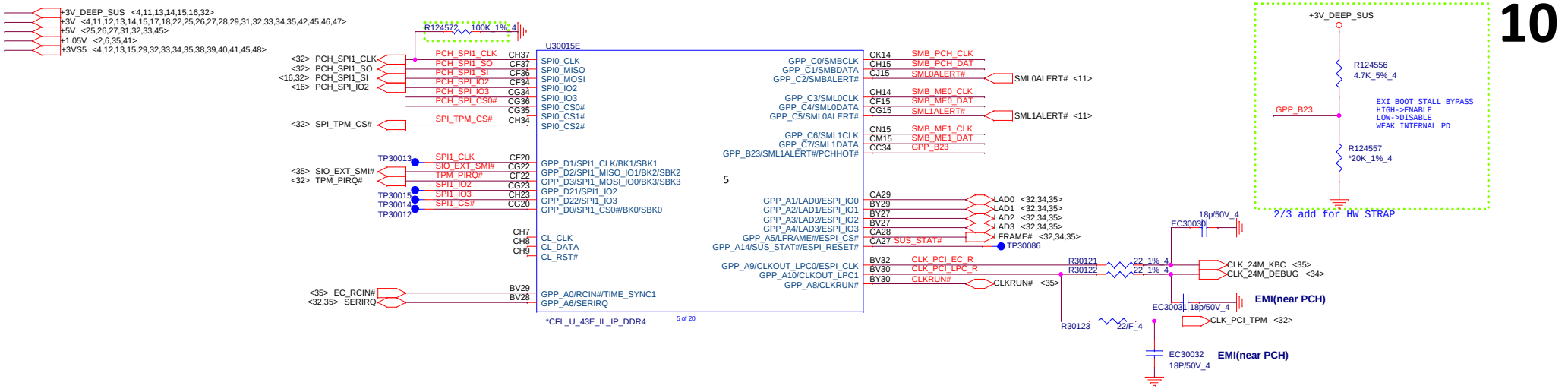
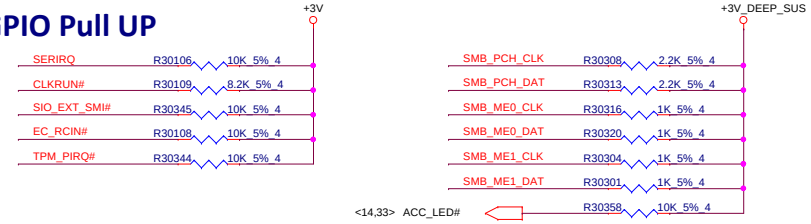


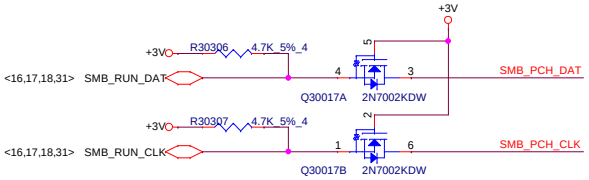
GPIO Pull UP



SMBus/Pull-up(CLG)

CPU heat pipe local thermal sensor
DDR thermal sensor
EC

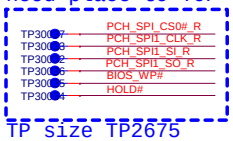
Touch Pad
XDP
DDR4



PCH SPI ROM(CLG)

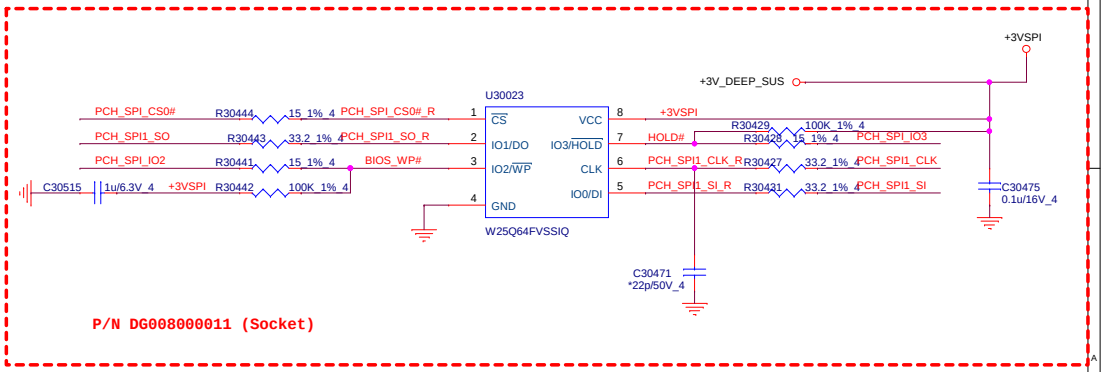
Vender	Size	P/N
MXIC	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSIQ)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DG008000011

need place to TOP

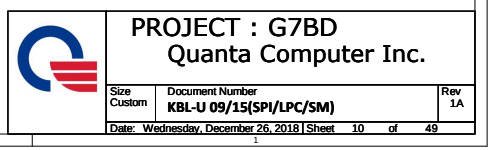


TP size TP2675

PCH SPI ROM(CLG)

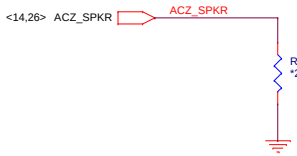


P/N DG008000011 (Socket)

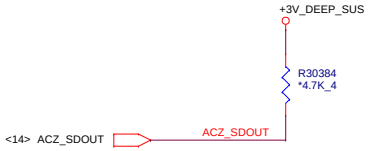


Functional Strap Definitions

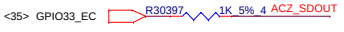
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

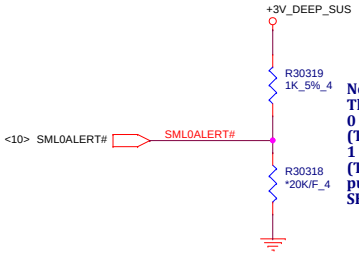


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

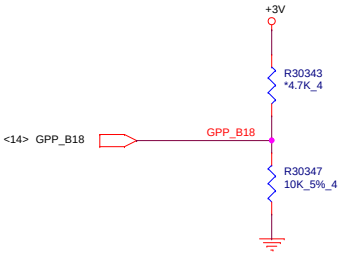


No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

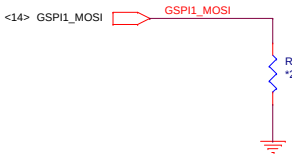




No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

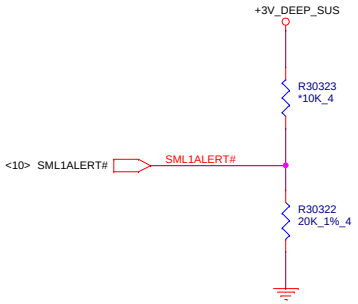


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 10/15(HDA)	1A

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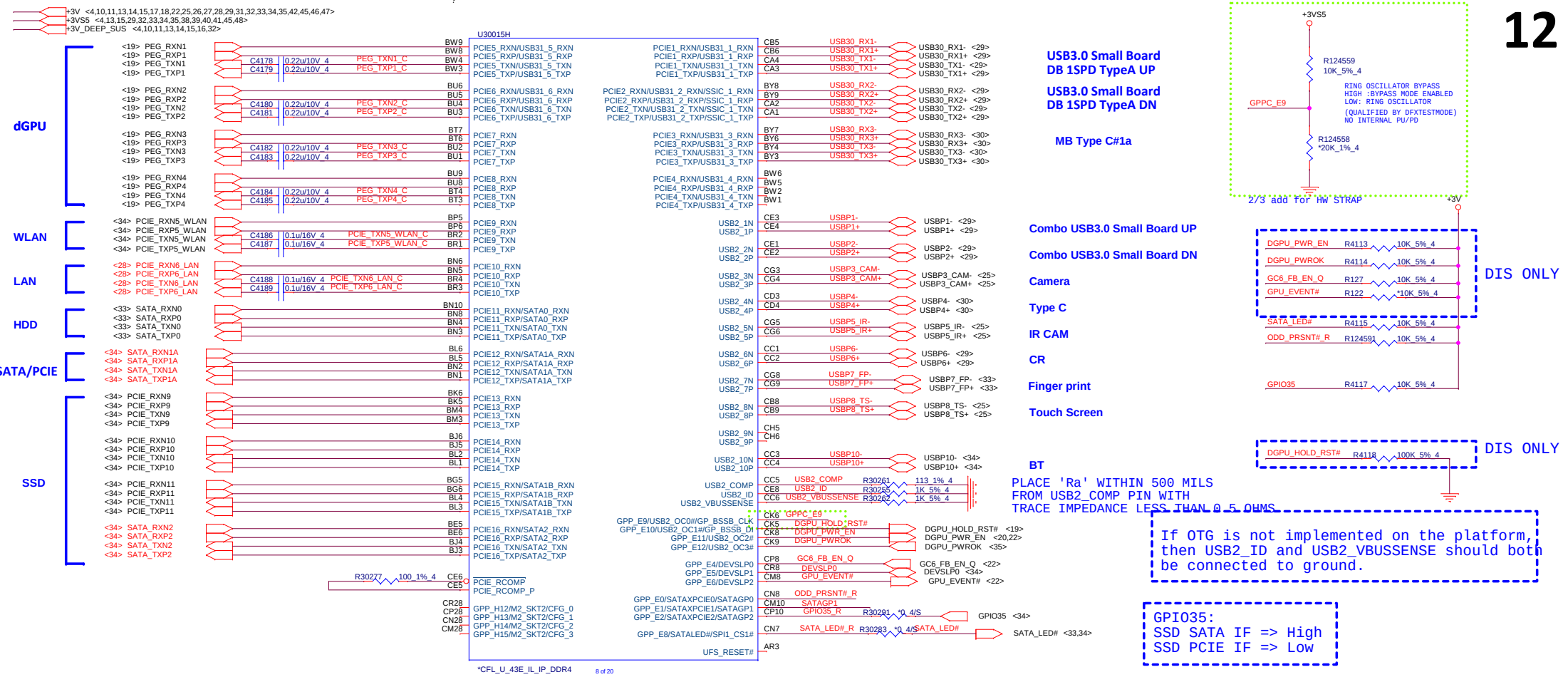

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port5	dGPU	Port0	VGA
Port6	dGPU	Port1	CR
Port7	dGPU	Port2	SSD
Port8	dGPU	Port3	WLAN
Port9	WLAN	Port4	LAN
Port10	LAN	Port5	Un-used
Port11	HDD		
Port12	ODD		
Port13	PCIE SSDx4		
Port14	PCIE SSDx4		
Port15	PCIE SSDx4		
Port16	PCIE SSDx4 /SATA SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Type C
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 Small Board
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Card reader
PORT-7	NC
PORT-8	NC
PORT-9	NC
PORT-10	BT

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 11/15 (PCIE/USB)	1A

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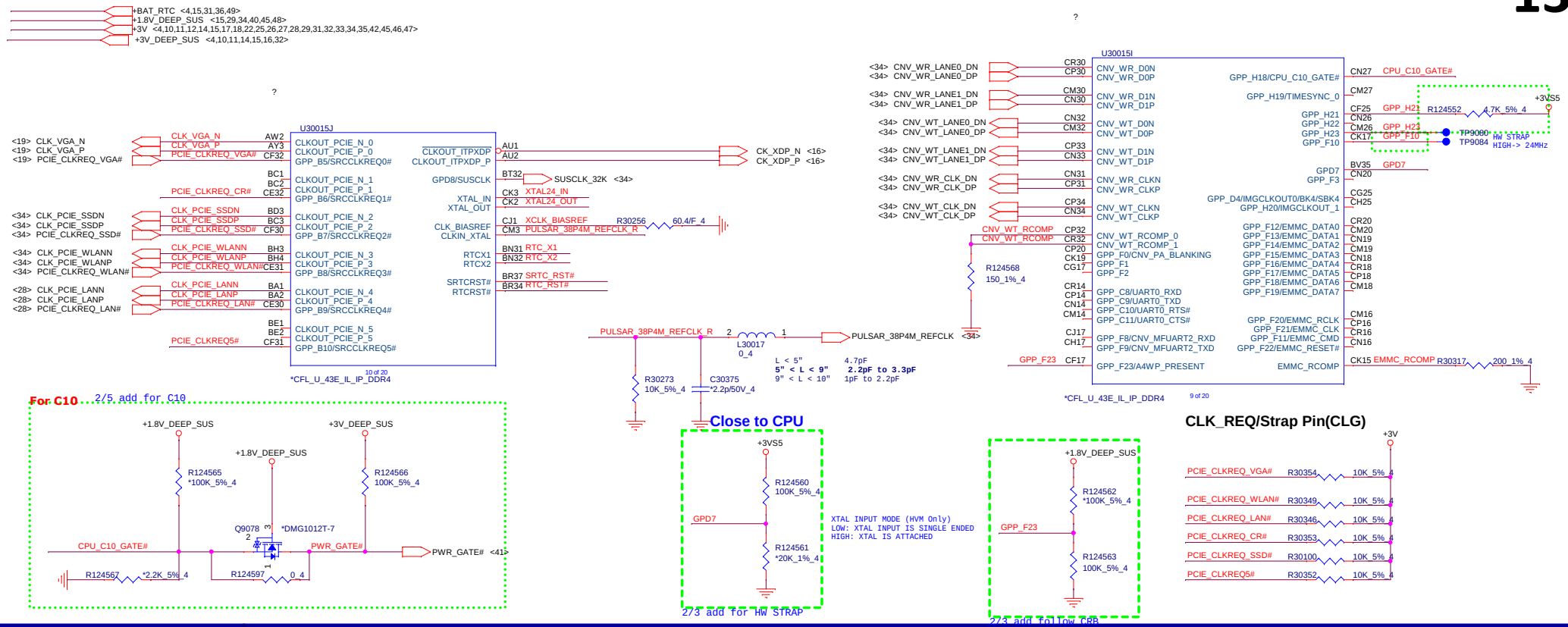
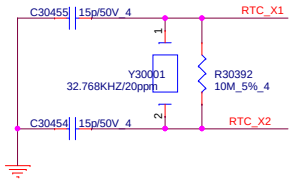


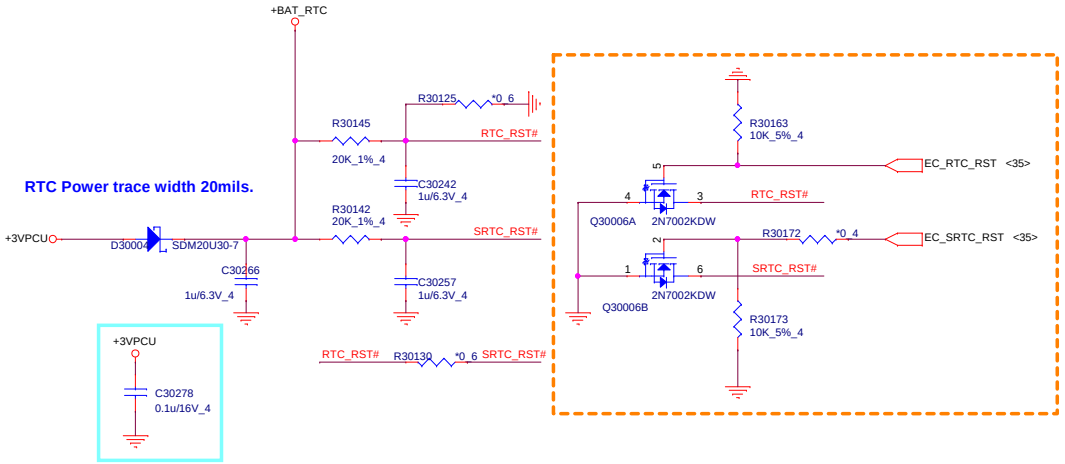
RTC Clock 32.768KHz



RTC Circuitry(RTC)

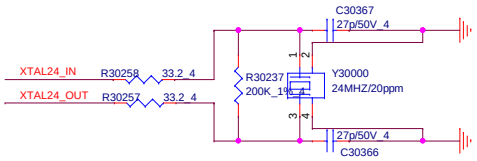
30mils

RTC Power trace width 20mils.



External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 12/15 (CLK/EMMC)	1A

Date: Wednesday, December 26, 2018 | Sheet 13 of 49

WHLake (GPIO)

+3V <4,10,11,12,13,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47>
+3V_DEEP_SUS <4,10,11,13,15,16,32>

U30015F

*CFL_U_43E_IL_IP_DDR4 6 of 20

M.2 CNVI MODES
LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE

2/7 add for HW STRAP

HDA Bus(CLG)

Add cap for RF issue

close to CPU/1004

U30015G

*CFL_U_43E_IL_IP_DDR4 7 of 20

Board ID6 default High,when device insert will become low

WHL	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	BOARD_ID[3:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3 ID2 ID1	ID0
Definition	Reserve (Default = 00)	0:Finger Print 1:Non-Finger Print	0 : AMD 1 : Nvidia GPU setting	0 : 2G VRAM 1 : 4G VRAM	100 : 14" (WHL) 000 : 14" 101 : 15" 1SPD (WHL) 001 : 15 1SPD 110 : 2SPD (WHL) 010 : MAX-Q 111 : 13" (WHL) 011 : 2SPD	0 : UMA 1 : DIS

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBL-U 13/15 (GPIO)	1A

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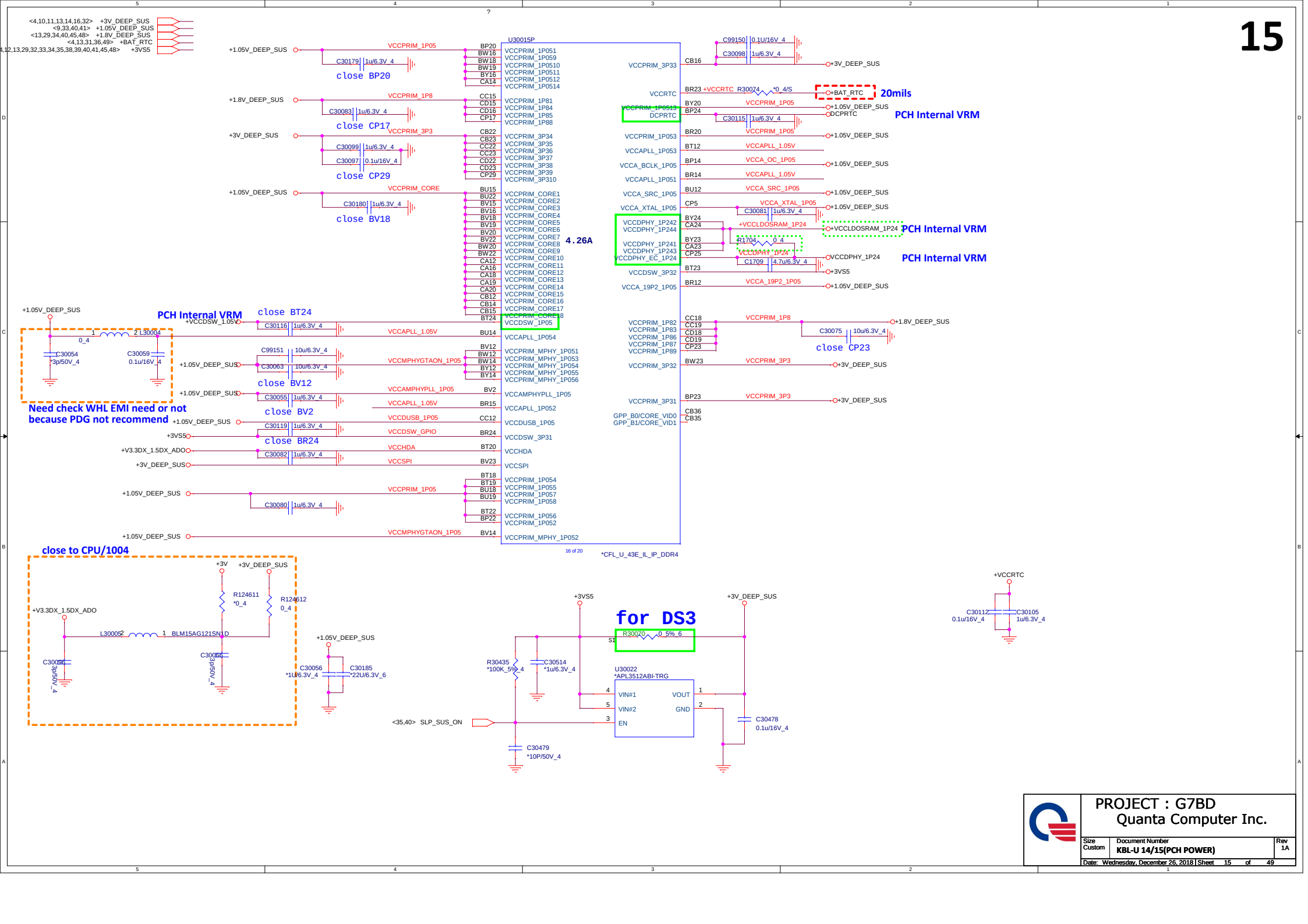
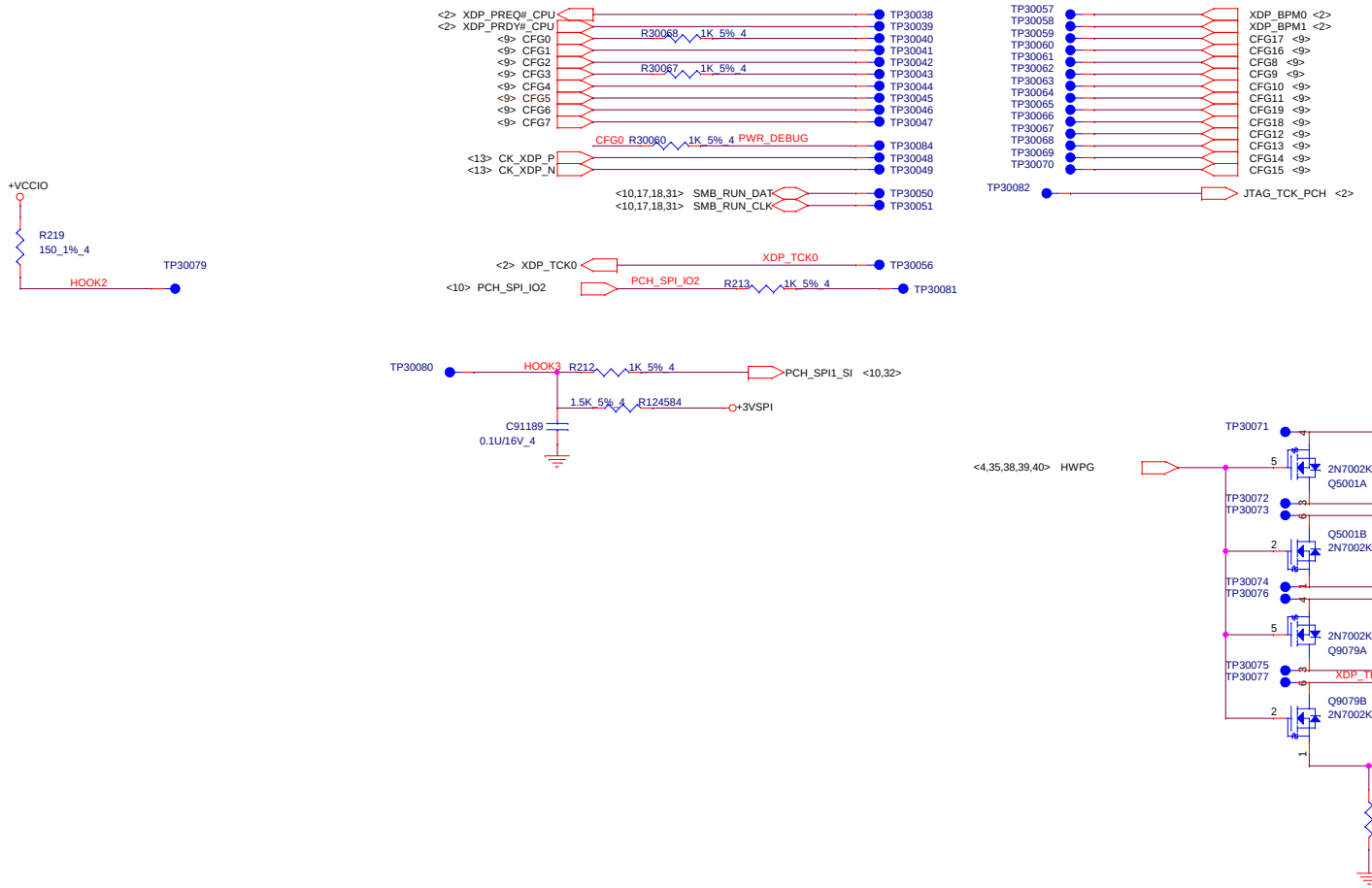

U30015P
4.26A
PCH Internal VRM
close BP20
close CP17
close CP29
close BV18
close BT24
close BV12
close BV2
close BR24
close CP23
Need check WHL EMI need or not because PDG not recommend
close to CPU/1004
for DS3
20mils
*CFL_U_43E_IL_IP_DDR4

XDP Debug



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
	KBL-U 15/15 XDP&APS *	1A

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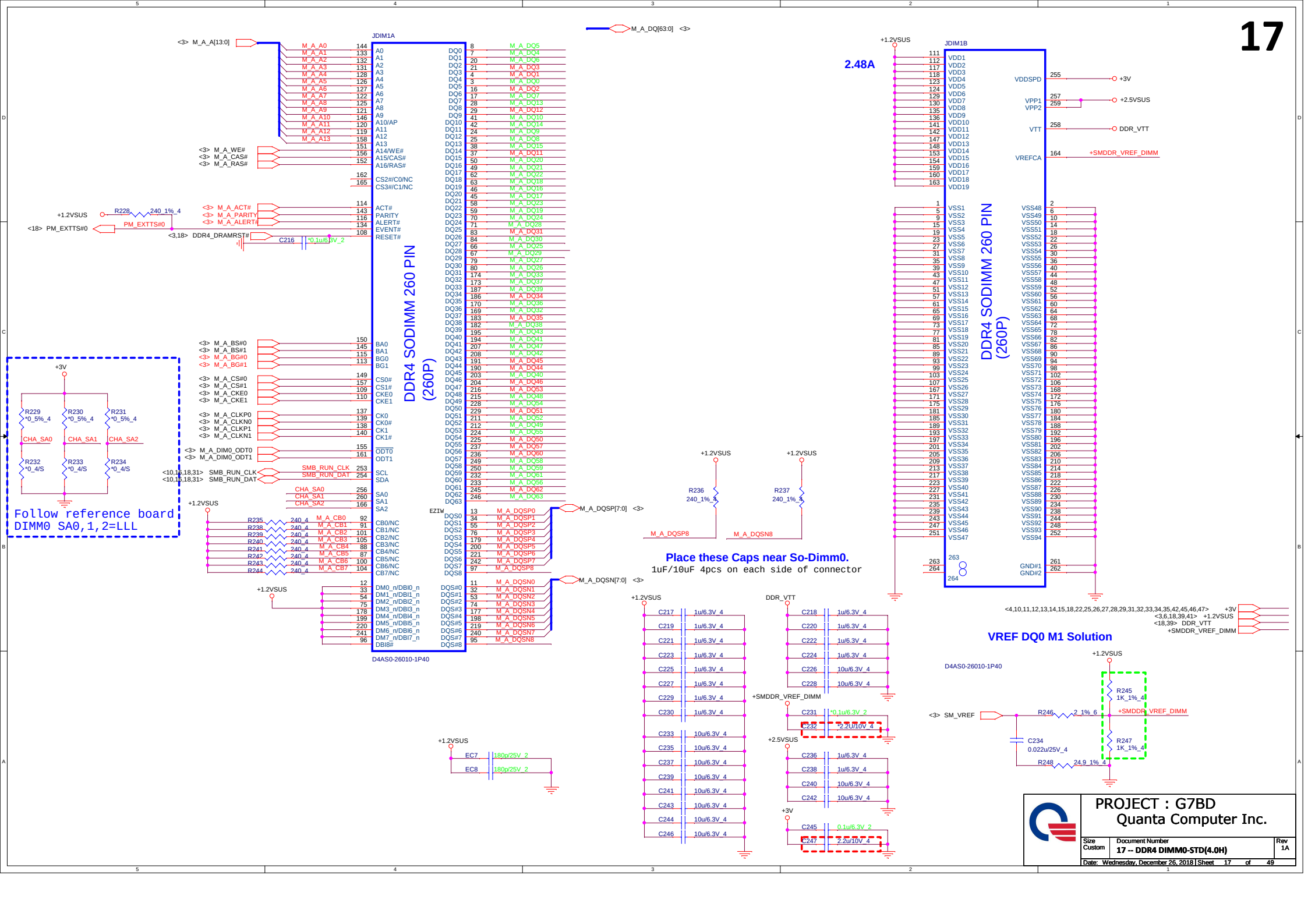

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	17 -- DDR4 DIMM0-STD(4.0H)	1A

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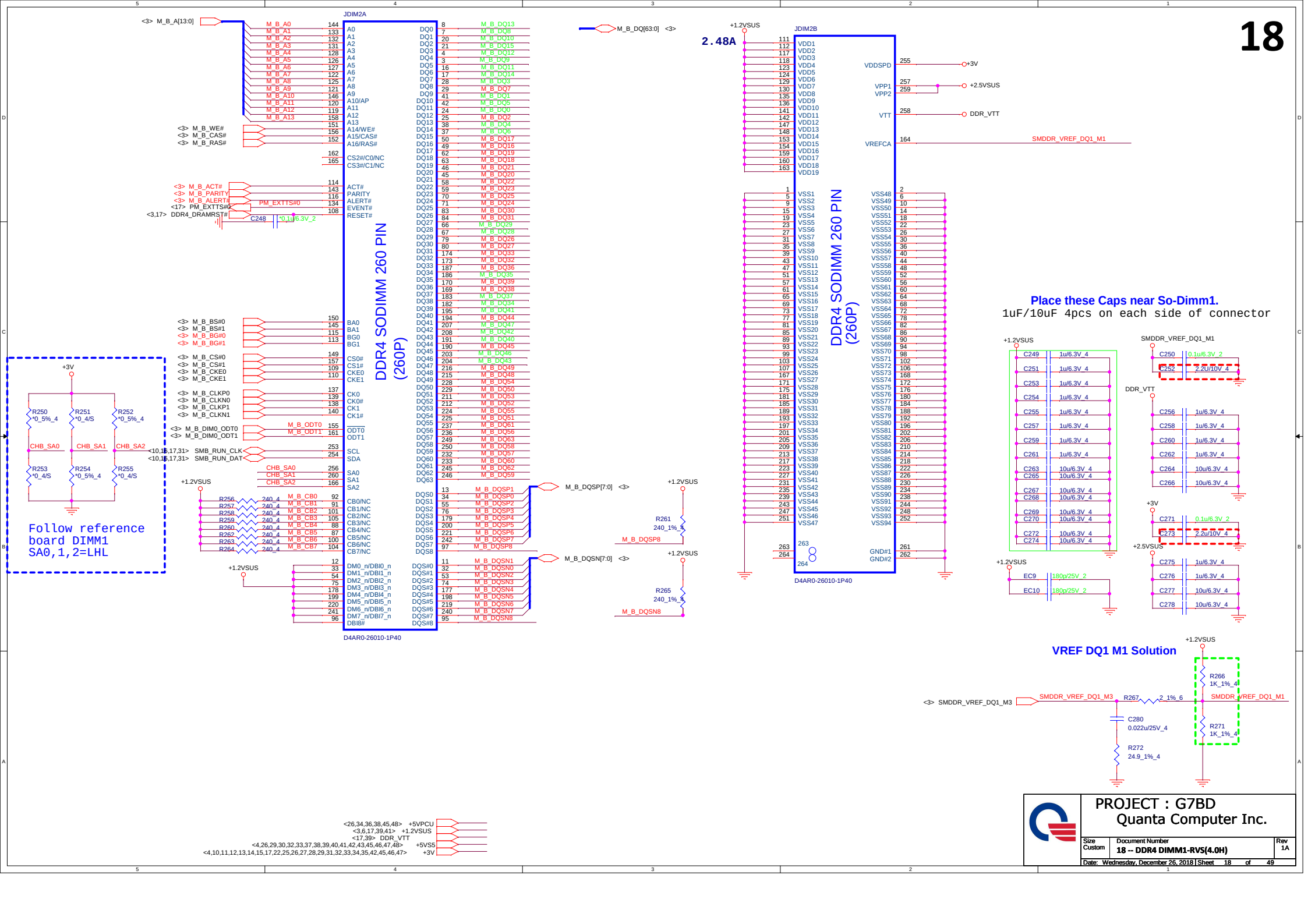
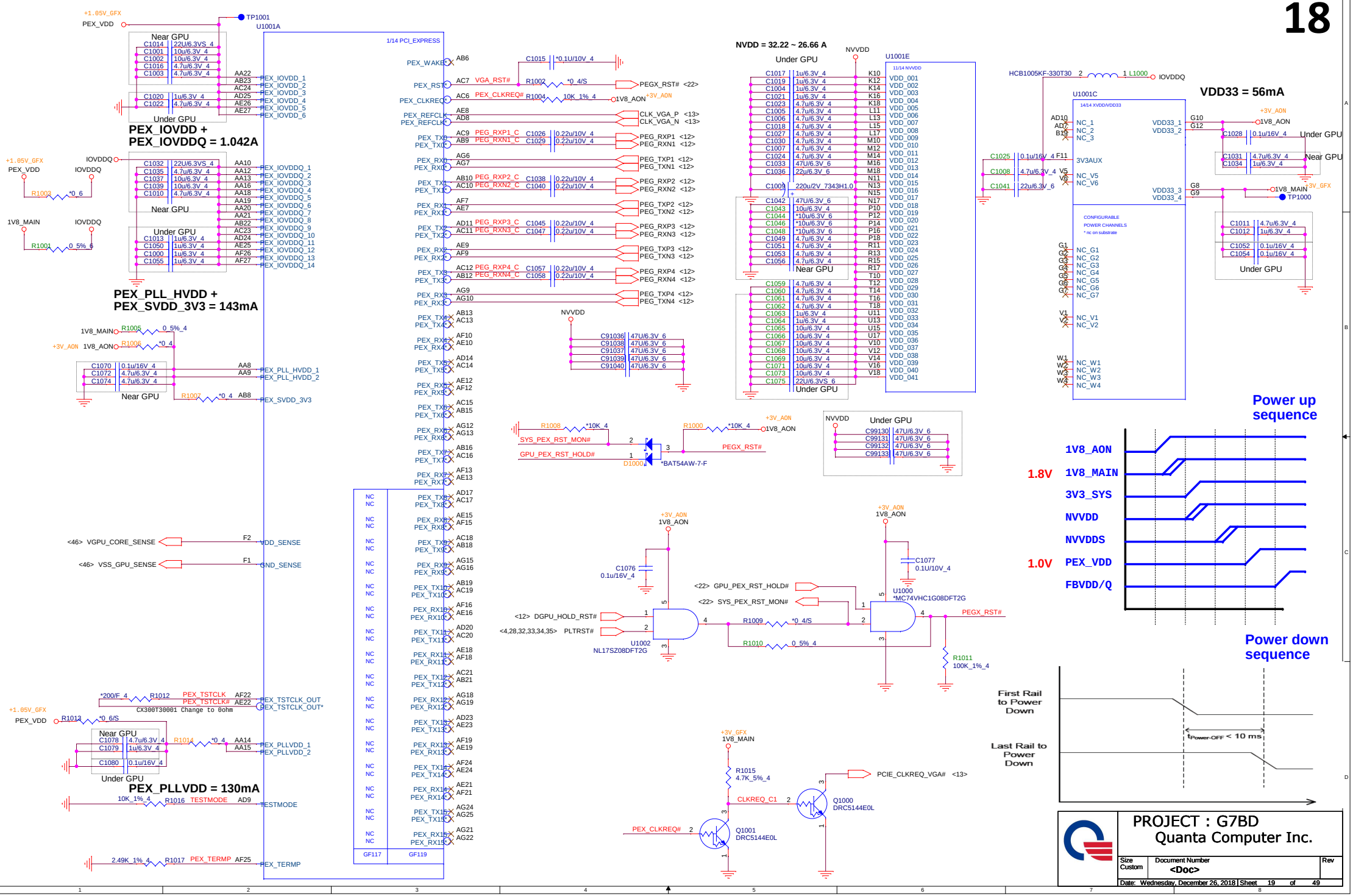
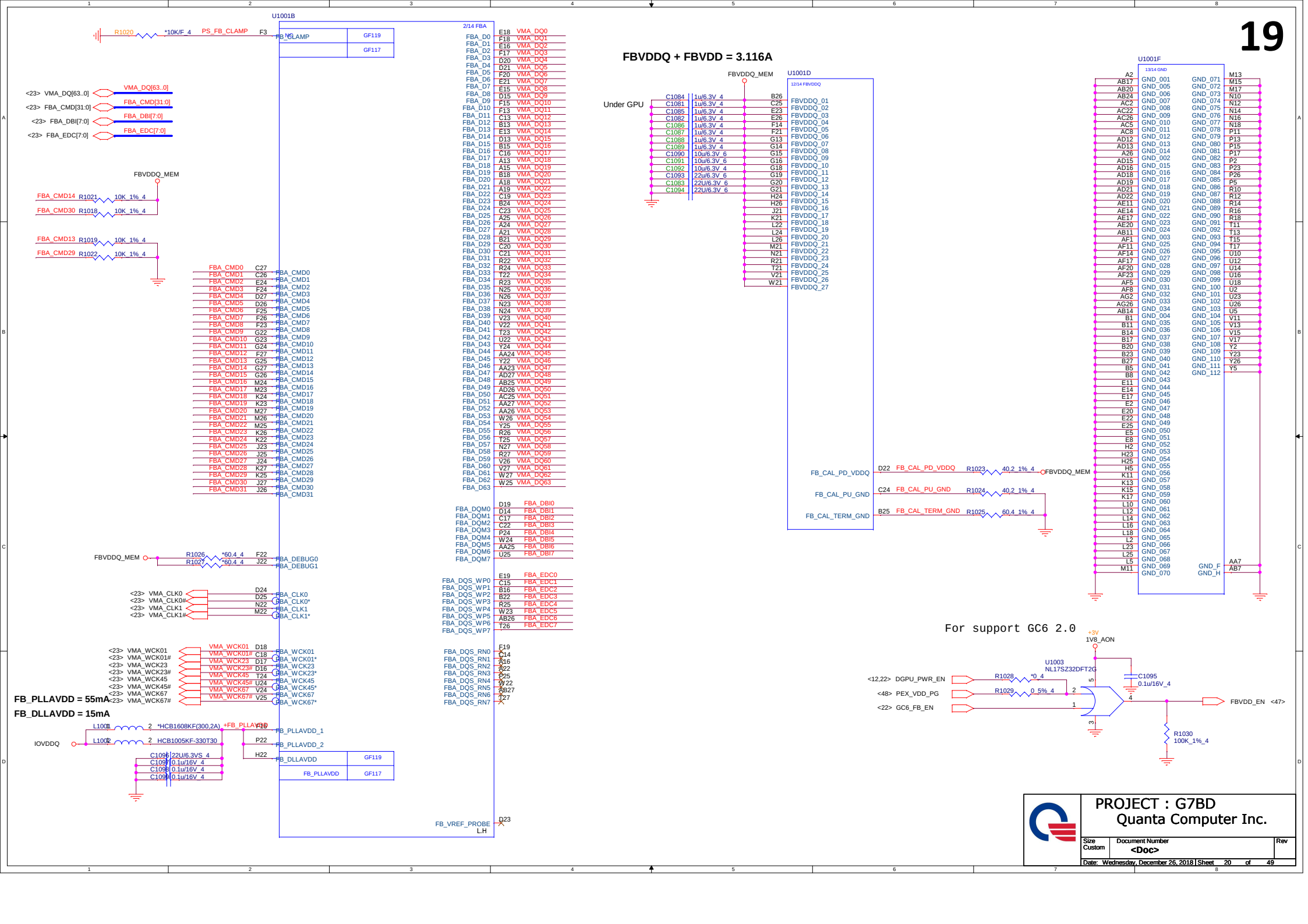
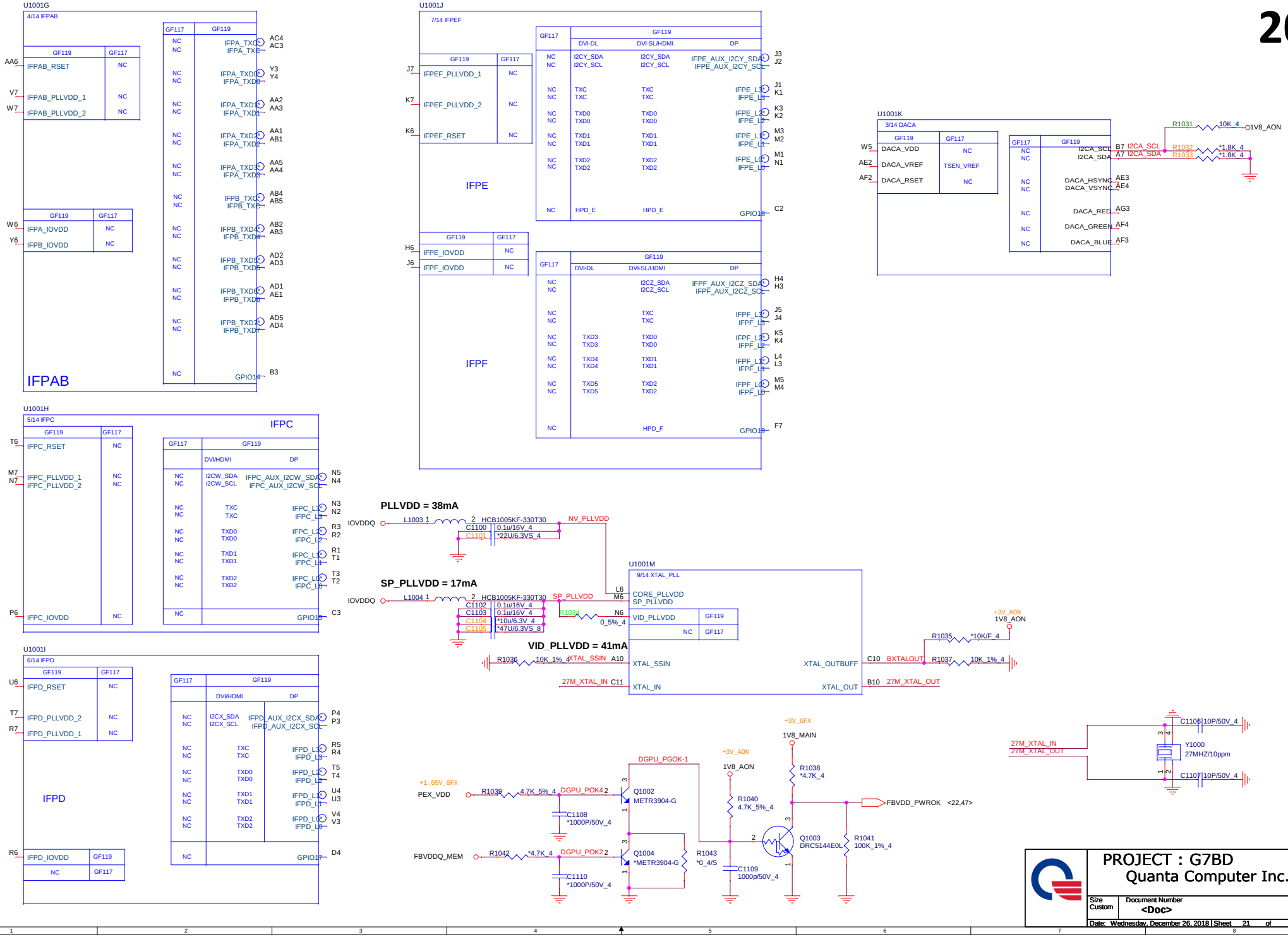
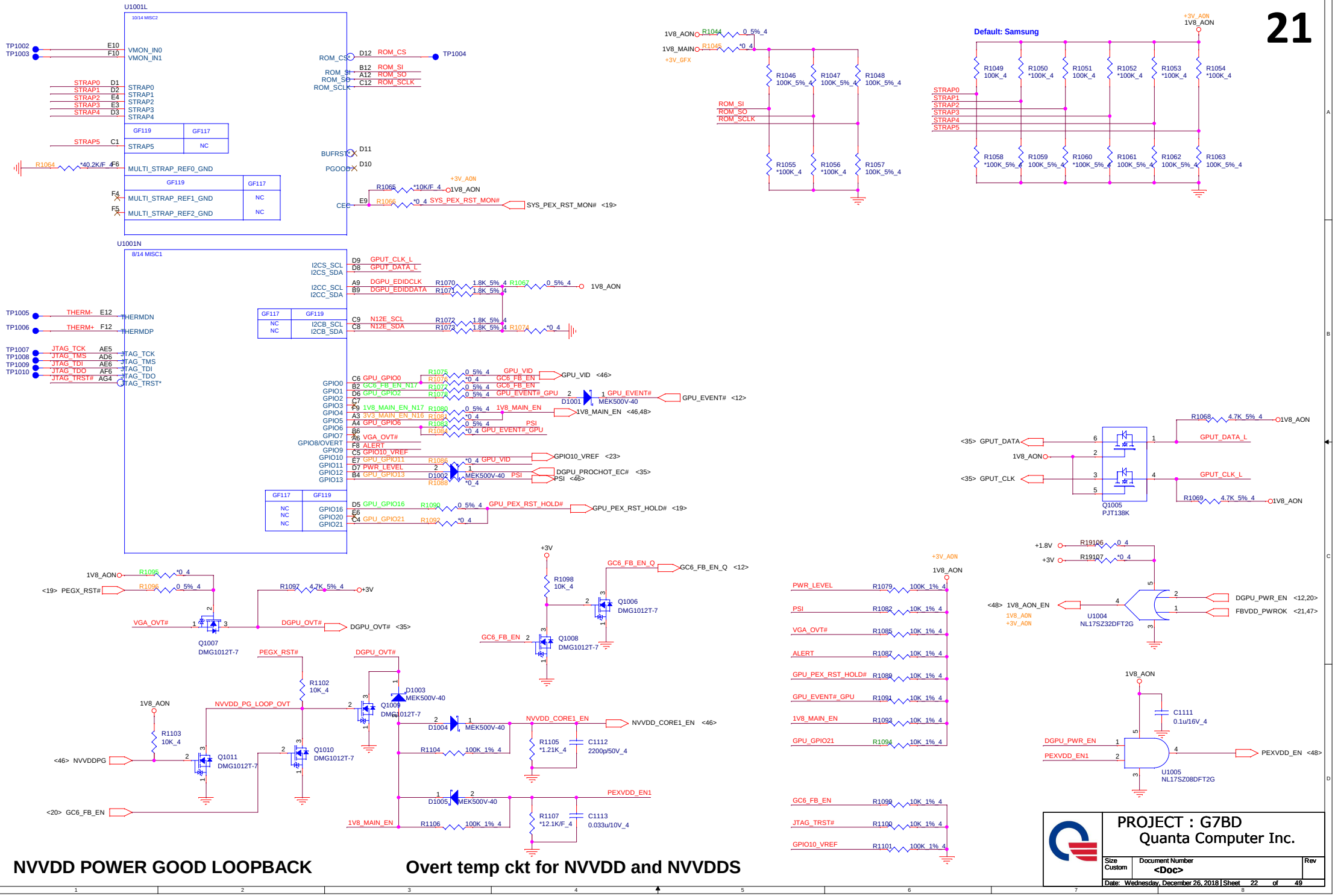

JDIM2A
DDR4 SODIMM 260 PIN (260P)
D4AR0-26010-1P40
JDIM2B
2.48A
DDR4 SODIMM 260 PIN (260P)
D4AR0-26010-1P40
Follow reference board DIMM1 SA0,1,2=LHL
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
PROJECT : G7BD
Quanta Computer Inc.
Size Custom
Document Number
18 -- DDR4 DIMM1-RVS(4.0H)
Rev 1A
Date: Wednesday, December 26, 2018 | Sheet 18 of 49


PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up sequence
1V8_AON
1V8_MAIN
3V3_SYS
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
1.8V
1.0V
Power down sequence
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
PROJECT : G7BD
Quanta Computer Inc.
Size Custom
Document Number
<Doc>
Rev
Date: Wednesday, December 26, 2018 Sheet 19 of 49


U1001B
R1020 *10K/F_4 PS_FB_CLAMP F3
FB_CLAMP
GF119
GF117
2/14 FBA
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
FBA_DBI0 D19
FBA_DBI1 D14
FBA_DBI2 C17
FBA_DBI3 C22
FBA_DBI4 P24
FBA_DBI5 W24
FBA_DBI6 AA25
FBA_DBI7 U25
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBA_EDC0 E19
FBA_EDC1 C15
FBA_EDC2 B16
FBA_EDC3 B22
FBA_EDC4 R25
FBA_EDC5 W23
FBA_EDC6 AB26
FBA_EDC7 T26
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBA_DQS_RN0 F19
FBA_DQS_RN1 C14
FBA_DQS_RN2 A16
FBA_DQS_RN3 A22
FBA_DQS_RN4 C25
FBA_DQS_RN5 W22
FBA_DQS_RN6 AB27
FBA_DQS_RN7 T27
FB_VREF_PROBE D23
L.H
FBA_CMD0 C27
FBA_CMD1 C26
FBA_CMD2 E24
FBA_CMD3 F24
FBA_CMD4 D27
FBA_CMD5 D26
FBA_CMD6 F25
FBA_CMD7 F26
FBA_CMD8 F23
FBA_CMD9 G22
FBA_CMD10 G23
FBA_CMD11 G24
FBA_CMD12 F27
FBA_CMD13 G25
FBA_CMD14 G27
FBA_CMD15 G26
FBA_CMD16 M24
FBA_CMD17 M23
FBA_CMD18 K24
FBA_CMD19 K23
FBA_CMD20 M27
FBA_CMD21 M26
FBA_CMD22 M25
FBA_CMD23 K26
FBA_CMD24 K22
FBA_CMD25 J23
FBA_CMD26 J25
FBA_CMD27 J24
FBA_CMD28 K27
FBA_CMD29 K25
FBA_CMD30 J27
FBA_CMD31 J26
<23> VMA_DQ[63..0]
VMA_DQ[63..0]
<23> FBA_CMD[31:0]
FBA_CMD[31:0]
<23> FBA_DBI[7:0]
FBA_DBI[7:0]
<23> FBA_EDC[7:0]
FBA_EDC[7:0]
FBVDDQ_MEM
FBA_CMD14 R1021 10K_1%_4
FBA_CMD30 R1018 10K_1%_4
FBA_CMD13 R1019 10K_1%_4
FBA_CMD29 R1022 10K_1%_4
FBVDDQ_MEM R1026 *60.4_4 F22
R1027 *60.4_4 J22
FBA_DEBUG0
FBA_DEBUG1
<23> VMA_CLK0 D24
<23> VMA_CLK0# D25
<23> VMA_CLK1 N22
<23> VMA_CLK1# M22
FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*
<23> VMA_WCK01 D18
<23> VMA_WCK01# C18
<23> VMA_WCK23 D17
<23> VMA_WCK23# D16
<23> VMA_WCK45 T24
<23> VMA_WCK45# U24
<23> VMA_WCK67 V24
<23> VMA_WCK67# V25
FBA_WCK01
FBA_WCK01*
FBA_WCK23
FBA_WCK23*
FBA_WCK45
FBA_WCK45*
FBA_WCK67
FBA_WCK67*
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
IOVDDQ
L1001 2 *HCB1608KF(300,2A) +FB_PLLAVDD
L1002 2 HCB1005KF-330T30
C1096 22U/6.3VS_4
C1097 0.1u/16V_4
C1098 0.1u/16V_4
C1099 0.1u/16V_4
P16 FB_PLLAVDD_1
P22 FB_PLLAVDD_2
H22 FB_DLLAVDD
FB_PLLAVDD
GF119
GF117
FBVDDQ + FBVDD = 3.116A
Under GPU
FBVDDQ_MEM
C1084 1u/6.3V_4
C1081 1u/6.3V_4
C1085 1u/6.3V_4
C1082 1u/6.3V_4
C1086 1u/6.3V_4
C1087 1u/6.3V_4
C1088 1u/6.3V_4
C1089 1u/6.3V_4
C1090 10u/6.3V_6
C1091 10u/6.3V_6
C1092 10u/6.3V_4
C1093 22u/6.3V_6
C1083 22U/6.3V_6
C1094 22U/6.3V_6
U1001D
12/14 FBVDDQ
B26 FBVDDQ_01
C25 FBVDDQ_02
E23 FBVDDQ_03
E26 FBVDDQ_04
F14 FBVDDQ_05
F21 FBVDDQ_06
G13 FBVDDQ_07
G14 FBVDDQ_08
G15 FBVDDQ_09
G16 FBVDDQ_10
G18 FBVDDQ_11
G19 FBVDDQ_12
G20 FBVDDQ_13
G21 FBVDDQ_14
H24 FBVDDQ_15
H26 FBVDDQ_16
J21 FBVDDQ_17
K21 FBVDDQ_18
L22 FBVDDQ_19
L24 FBVDDQ_20
L26 FBVDDQ_21
M21 FBVDDQ_22
N21 FBVDDQ_23
R21 FBVDDQ_24
T21 FBVDDQ_25
V21 FBVDDQ_26
W21 FBVDDQ_27
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1023 40.2_1%_4 FBVDDQ_MEM
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1024 40.2_1%_4
FB_CAL_TERM_GND B25 FB_CAL_TERM_GND R1025 60.4_1%_4
U1001F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11
GND_001 GND_005 GND_006 GND_007 GND_008 GND_009 GND_010 GND_011 GND_012 GND_013 GND_014 GND_002 GND_015 GND_016 GND_017 GND_018 GND_019 GND_020 GND_021 GND_022 GND_023 GND_024 GND_003 GND_025 GND_026 GND_027 GND_028 GND_029 GND_030 GND_031 GND_032 GND_033 GND_034 GND_004 GND_035 GND_036 GND_037 GND_038 GND_039 GND_040 GND_041 GND_042 GND_043 GND_044 GND_045 GND_046 GND_047 GND_048 GND_049 GND_050 GND_051 GND_052 GND_053 GND_054 GND_055 GND_056 GND_057 GND_058 GND_059 GND_060 GND_061 GND_062 GND_063 GND_064 GND_065 GND_066 GND_067 GND_068 GND_069 GND_070
GND_071 GND_072 GND_073 GND_074 GND_075 GND_076 GND_077 GND_078 GND_079 GND_080 GND_081 GND_082 GND_083 GND_084 GND_085 GND_086 GND_087 GND_088 GND_089 GND_090 GND_091 GND_092 GND_093 GND_094 GND_095 GND_096 GND_097 GND_098 GND_099 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5
GND_F AA7
GND_H AB7
For support GC6 2.0
+3V
1V8_AON
U1003
NL17SZ32DFT2G
<12,22> DGPU_PWR_EN
<48> PEX_VDD_PG
<22> GC6_FB_EN
R1028 *0_4
R1029 0_5%_4
C1095 0.1u/16V_4
R1030 100K_1%_4
FBVDD_EN <47>
PROJECT : G7BD
Quanta Computer Inc.
Size Custom
Document Number <Doc>
Rev
Date: Wednesday, December 26, 2018 Sheet 20 of 49


U1001G
4/14 IFPAB
IFPAB
U1001J
7/14 IFPEF
IFPE
IFPF
U1001K
3/14 DACA
U1001H
5/14 IFPC
IFPC
U1001I
6/14 IFPD
IFPD
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
U1001M
9/14 XTAL_PLL
PROJECT : G7BD
Quanta Computer Inc.
Size Custom
Document Number
<Doc>
Rev
Date: Wednesday, December 26, 2018 | Sheet 21 of 49



NVVDD POWER GOOD LOOPBACK

Overt temp ckt for NVVDD and NVVDDS

CHANNEL A: 2G GDDR5

Channel A <0-31>

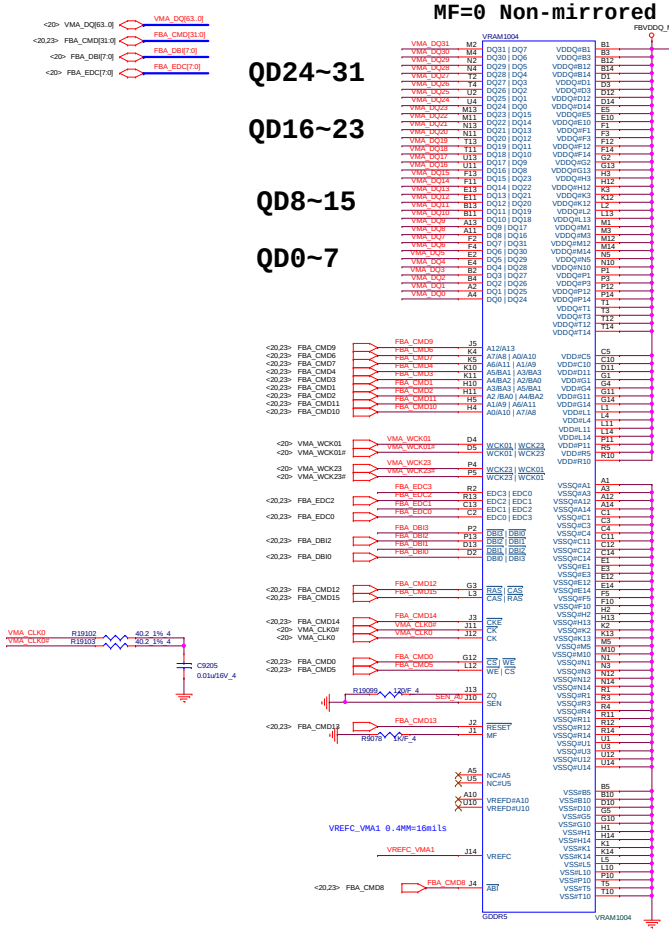
MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7



Channel A <32-63>

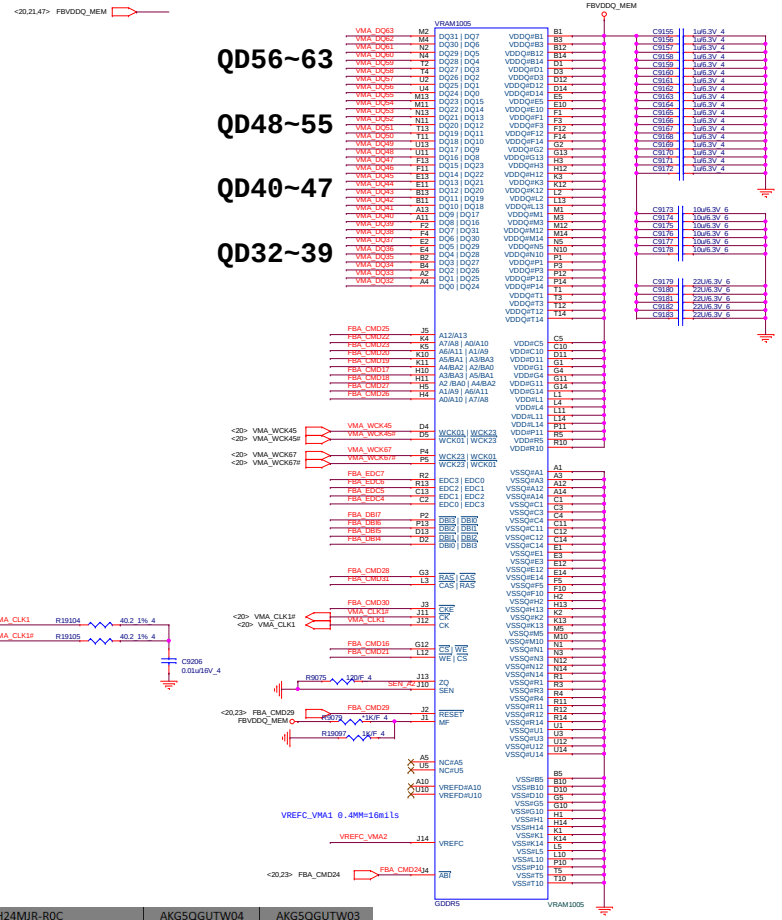
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39



GDDR5 256 x 32			
	Hynix H5GC8H24MJR-R0C	AKG5QGUTW04	AKG5QGUTW03
	Micron MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06
	Samsung K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	23 – VRAM GDDR5 - RANK1	1A

Date: Wednesday, December 26, 2018 | Sheet 23 of 49

N16S strap setting

```
ROM_SI    = VRAM Configuration follow VRAM table
ROM_SO    = Stuff 4.99K Pull Up      CS24992FB26
ROM_SCLK  = Stuff 4.99K Pull Down    CS24992FB26

STRAP0  =  Stuff 49.9K Pull Up     CS34992FB10
STRAP1  =  NC
STRAP2  =  NC
STRAP3  =  NC
STRAP4  =  NC
STRAP5  =  NC
```

N17S strap setting

```
ROM_SI    = Stuff 100K Pull Up   CS41002JB20
ROM_SO    = Stuff 100K Pull Up   CS41002JB20
ROM_SCLK  = Stuff 100K Pull Up and 100K Pull Down
                                 CS41002JB20

STRAP0  =  VRAM Configuration follow VRAM table
STRAP1  =  VRAM Configuration follow VRAM table
STRAP2  =  VRAM Configuration follow VRAM table
STRAP3  =  Stuff 100K Pull Down   CS41002JB20
STRAP4  =  Stuff 100K Pull Down   CS41002JB20
STRAP5  =  Stuff 100K Pull Down   CS41002JB20
```

	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0000
Micron	H	L	L	0x0004
Hynix	H	L	H	0x0005

STRAP[2:0] VRAM Table for N17S-G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508
0x4	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x5	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

ROM_SI VRAM Table for N16S-GTR GDDR5 Recommended Memories

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508
0x8	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x9	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

R1055	SAMSUNG	0000	4.99k	CS24992FB26
R1046	Micron	1000	4.99k	CS24992FB26
R1046	HYNIX	1001	10k	CS31002FB26

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	24 – VRAM CONFIG	1A

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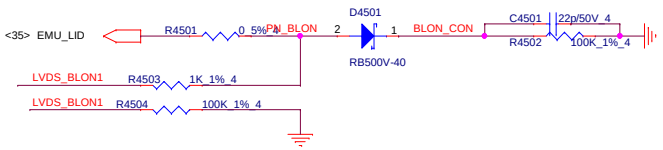
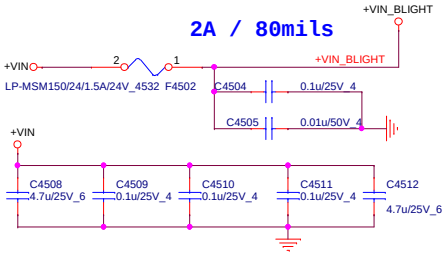
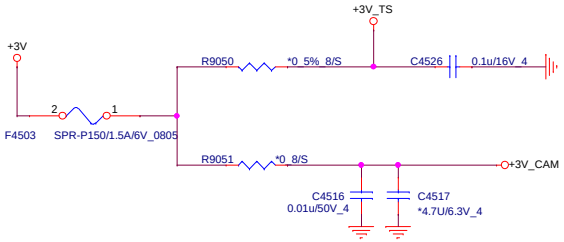
LID Switch

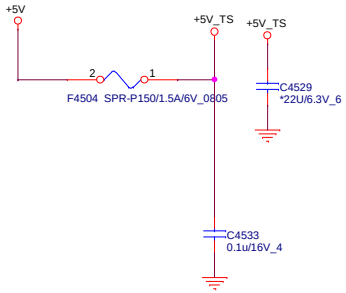


2A / 80mils

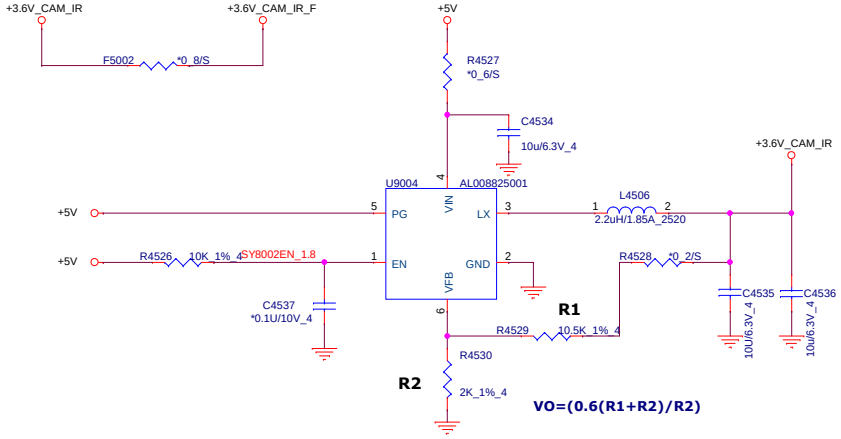


Touch screen



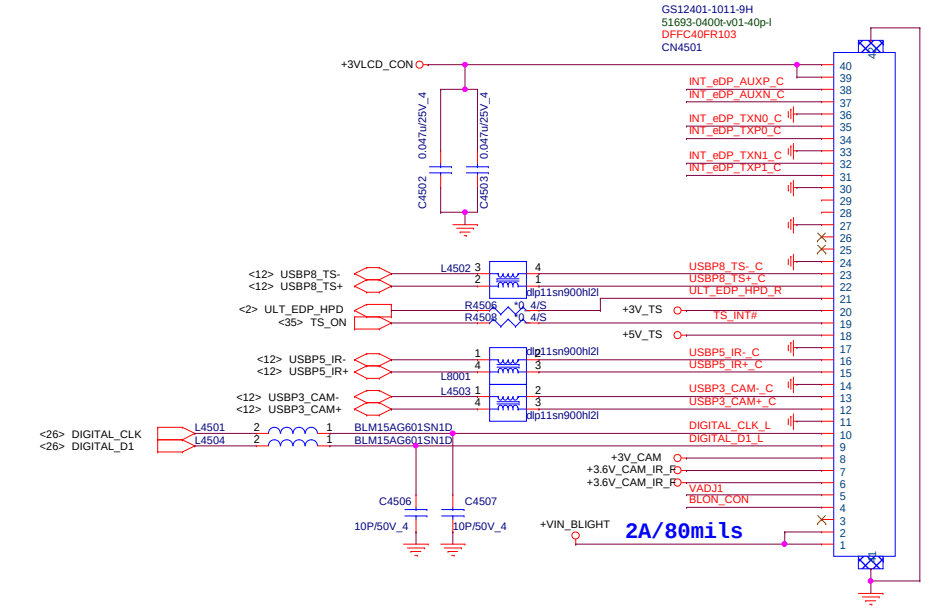


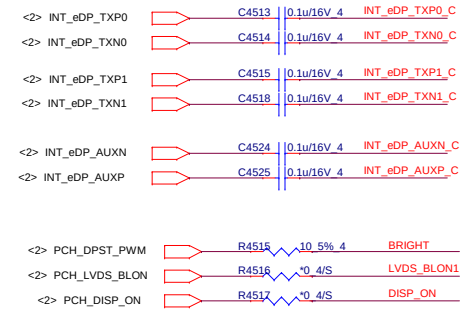
IR CAM

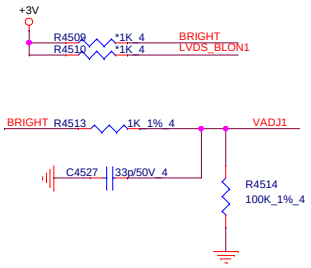


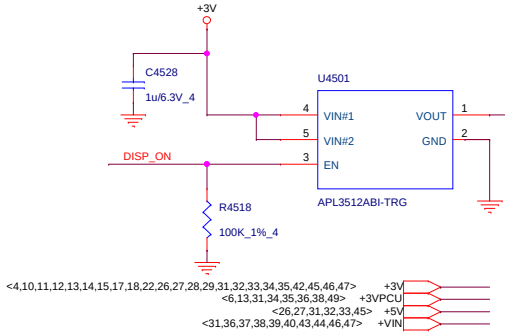
+3.6V +/- 5%
TDC:1A
EDP:2A

eDP Conn.









<4,10,11,12,13,14,15,17,18,22,26,27,28,29,31,32,33,34,35,42,45,46,47> +3V
<6,13,31,34,35,36,38,49> +3VPCU
<26,27,31,32,33,45> +5V
<31,36,37,38,39,40,43,44,46,47> +VIN

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- eDP CONN/LID/CAM/D-MIC/TS	1A

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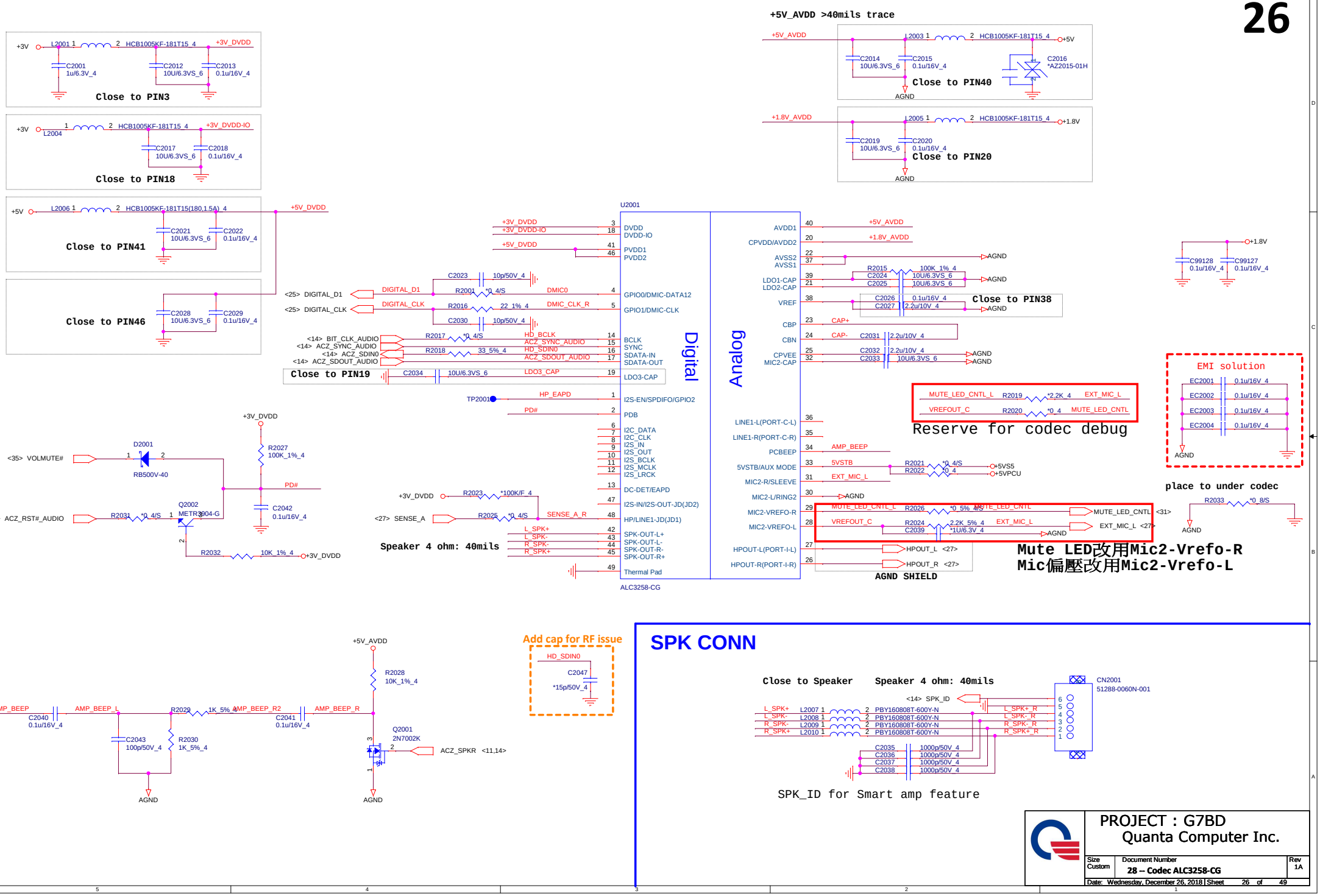

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 -- Codec ALC3258-CG	1A

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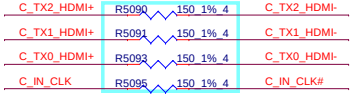
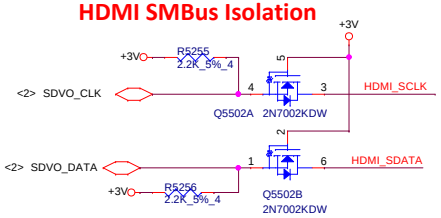
HDMI CONN

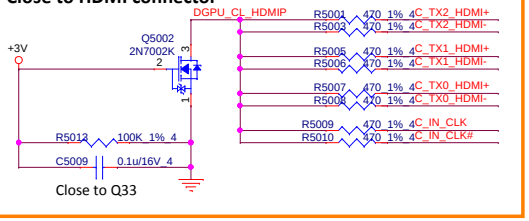
EMI Solution

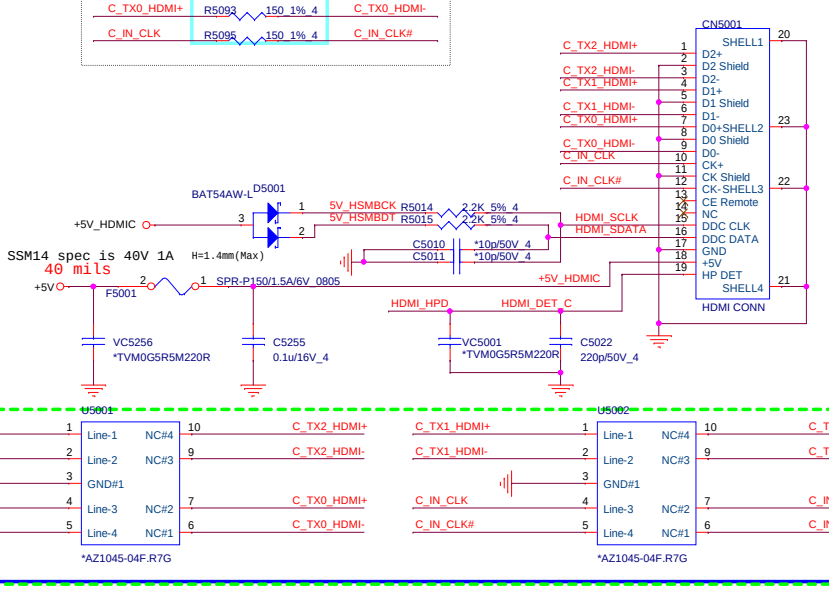


HDMI SMBus Isolation

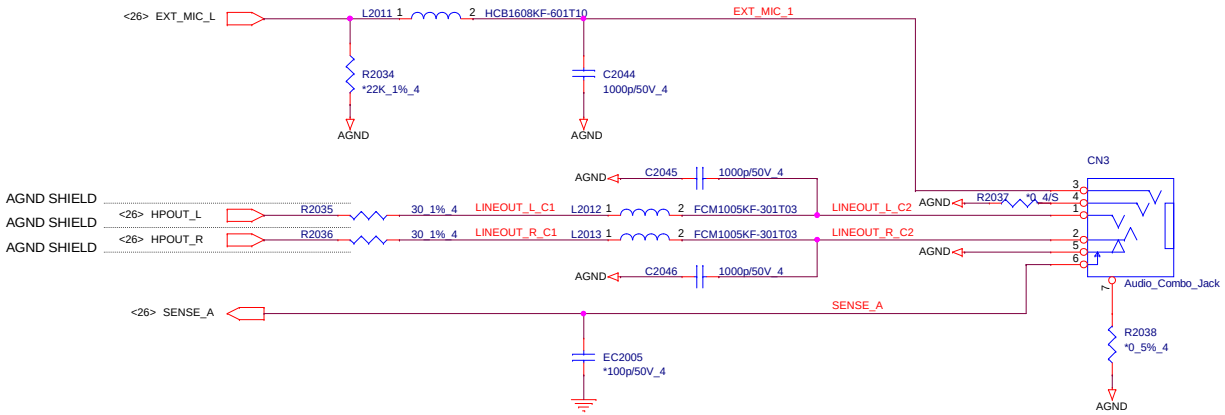


Close to HDMI connector

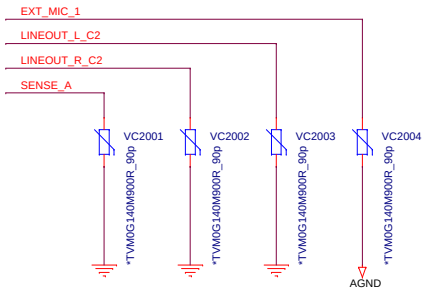




Audio Jack



Audio JACK ESD



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29 – HDMI/AMP HPA022642RTJR	1A

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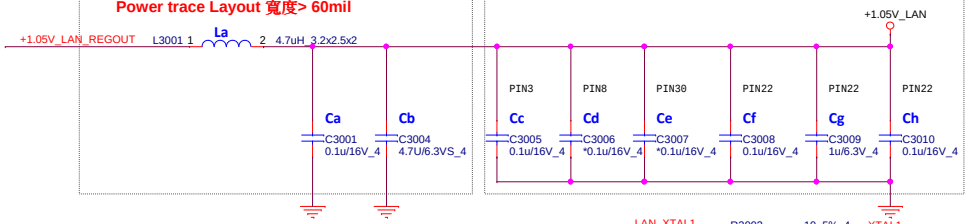
LAN RTL8111HSH-CG

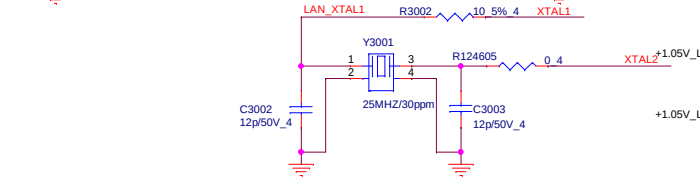
For SWR mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca ,Cb

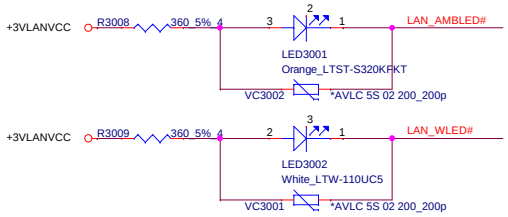
* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil





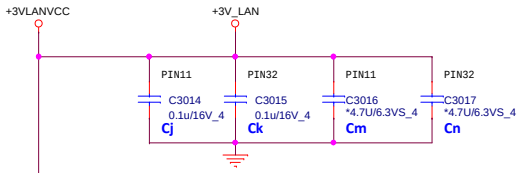


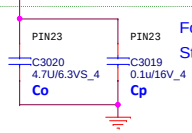
if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8107ESH-CG/RTL8111HSH-CG

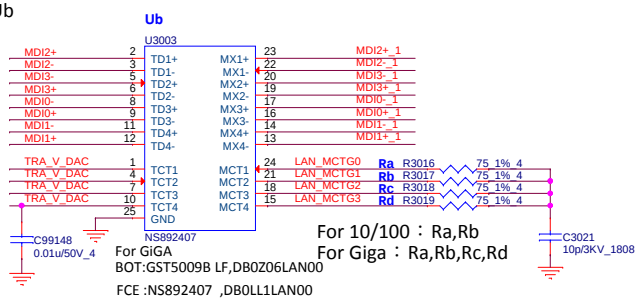
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



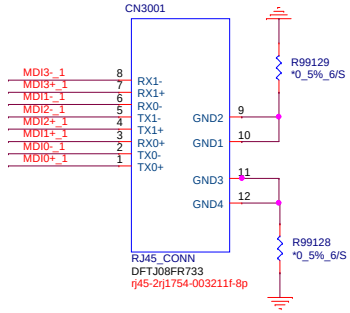


For SWR mode support RTL8107ESH-CG/RTL8111HSH-CG
Stuff Co, Cp

For Giga：Ub



RJ45



PROJECT：G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	30 -- LAN RTL8166EH/RTL8111HSH	1A

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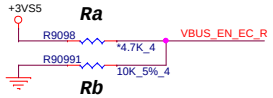
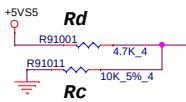
USB TYPEC POWER SWITCH



For C_VBUS power switch enable pin	Ra/Rb Note
Low Active	R16/R17 mount
High Active (default)	R17 mount,R16 don't mount

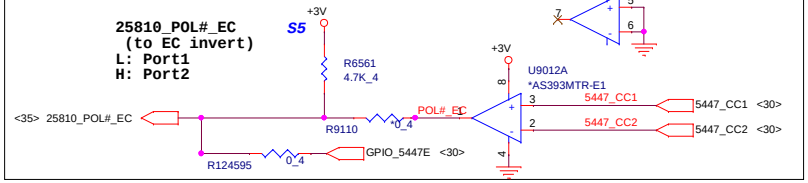


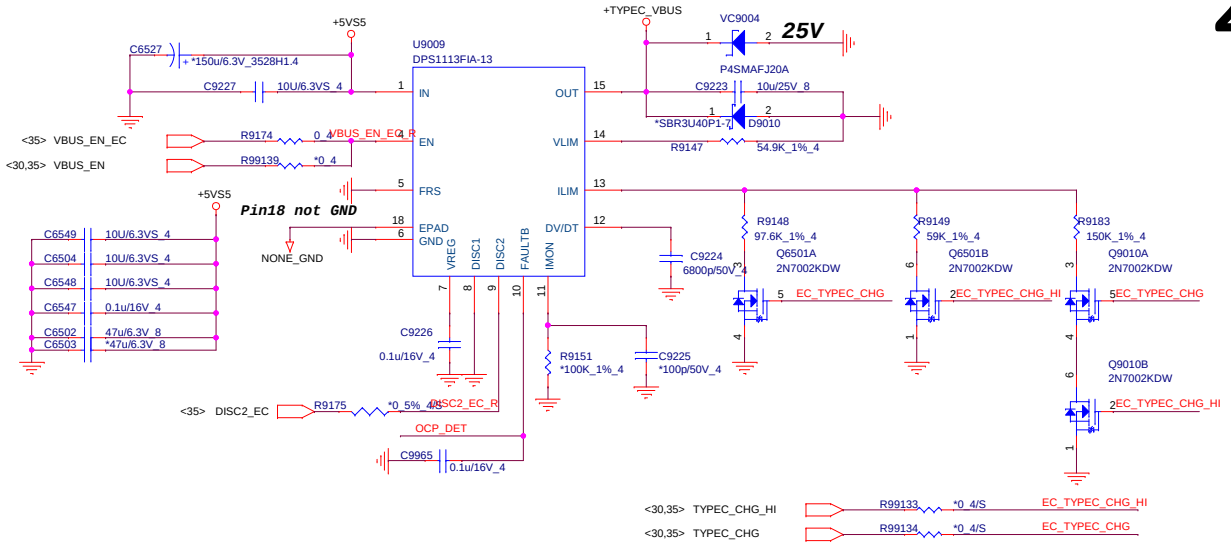
Power switch OCP pin	Rc/Rd Note
Low Active (default)	R18/R19 mount
High Active	R18 mount,R19 don't mount

For C_VBUS power switch OCP pin

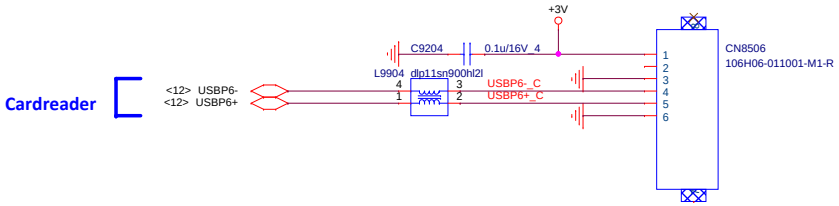
If can identify port1 or 2

25810_POL#_EC (to EC invert)
L: Port1
H: Port2

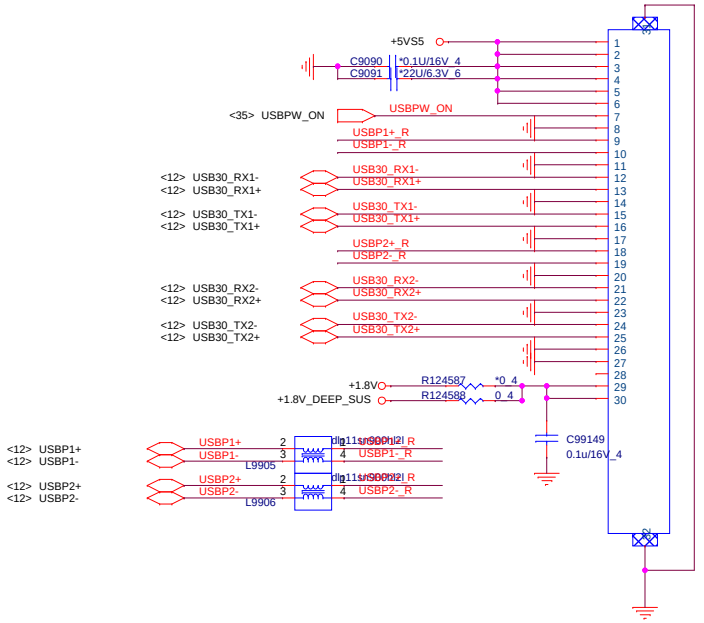




SD Board



USB Board



CN5502
DFFC30FR148
51519-03001-v01-30p-l
51519-0300T-V01

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	31 -- USB3.0/DB	1A

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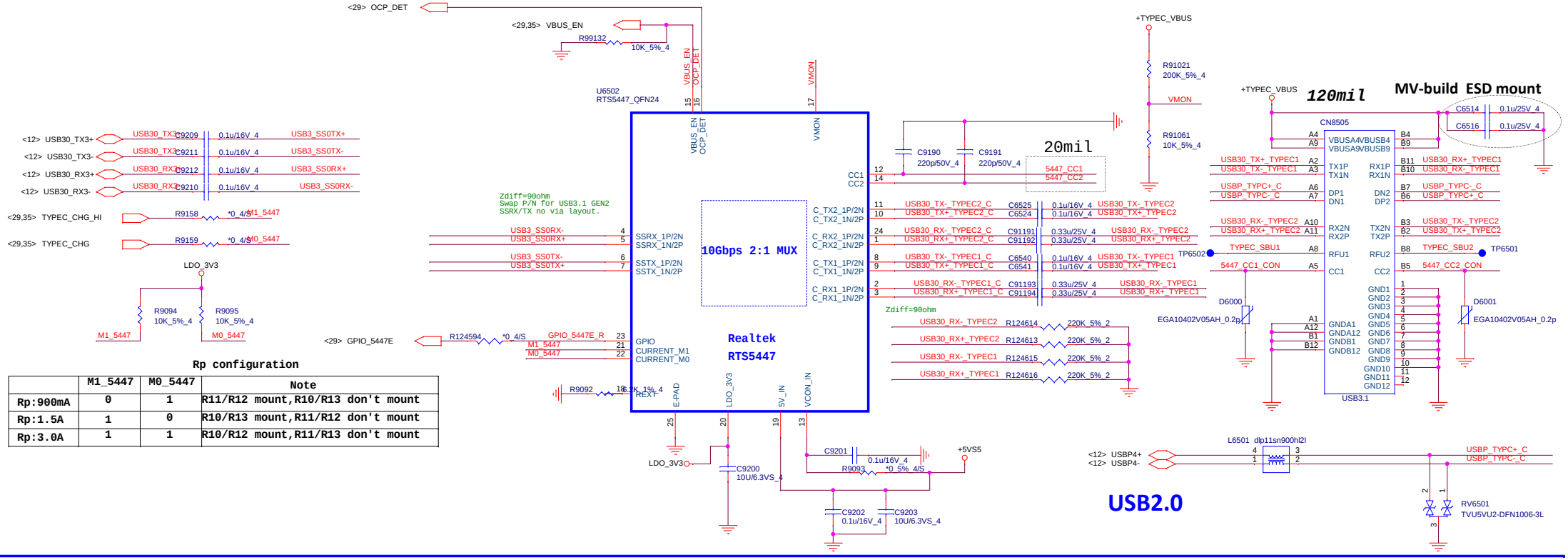
TYPE C MUX RTS5447

<4,26,29,32,33,37,38,39,40,41,42,43,45,46,47,48> +5VS5
<4,12,13,15,29,32,33,34,35,38,39,40,41,45,48> +3VS5
<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47> +3V
<29> +TYPEC_VBUS

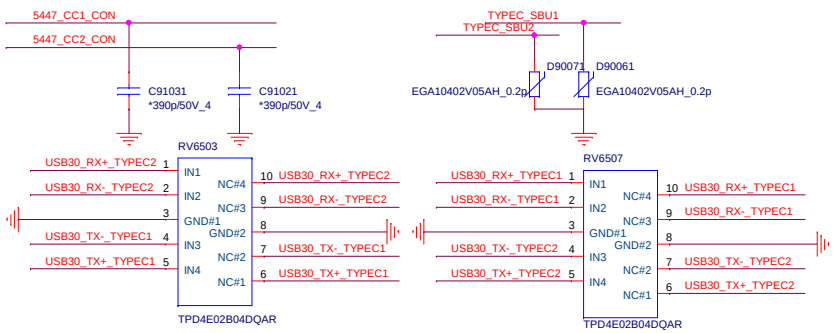


Rp configuration

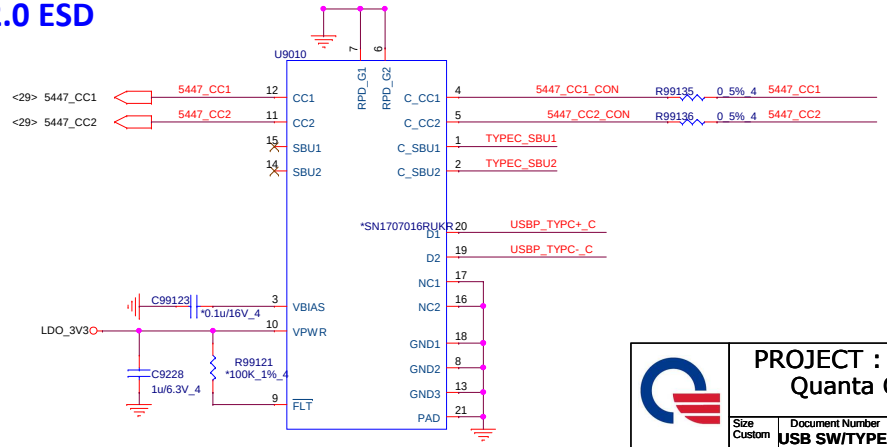
	M1_5447	M0_5447	Note
Rp:900mA	0	1	R11/R12 mount,R10/R13 don't mount
Rp:1.5A	1	0	R10/R13 mount,R11/R12 mount
Rp:3.0A	1	1	R10/R13 mount,R11/R12 mount

USB2.0

TYPE C USB3.0 ESD



TYPE C USB2.0 ESD



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB SW/TYPE-C RT5447 & Re-driver	3A

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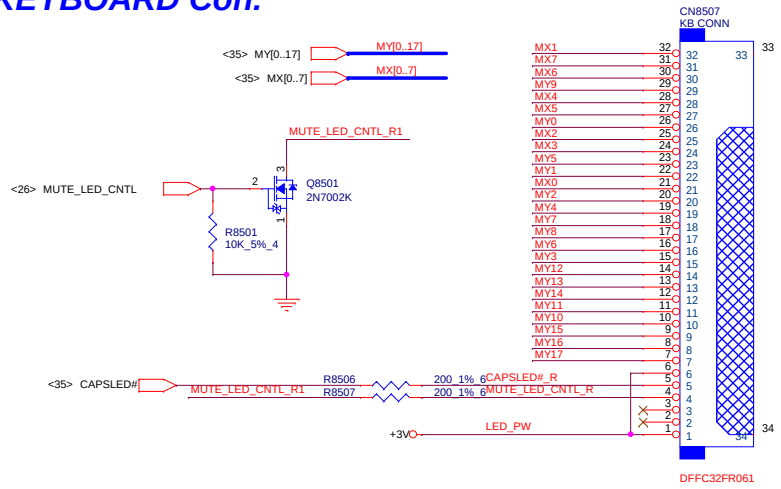
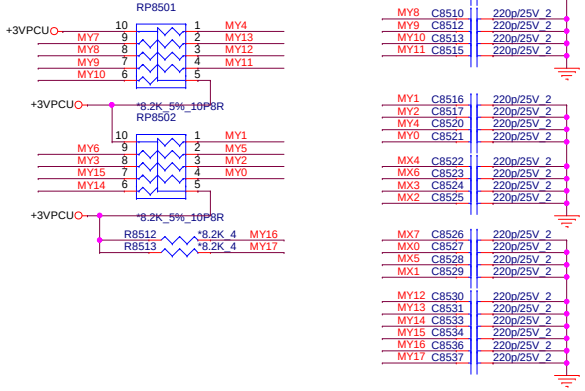
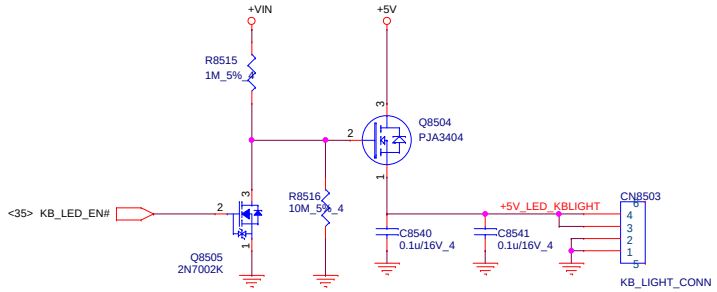
KEYBOARD Con.



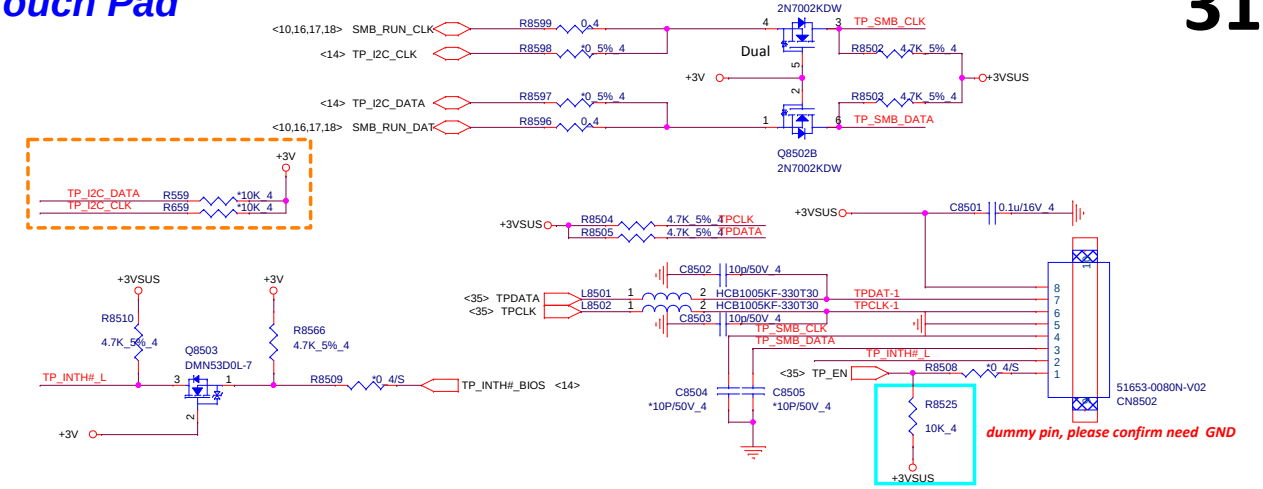
KEYBOARD PULL-UP



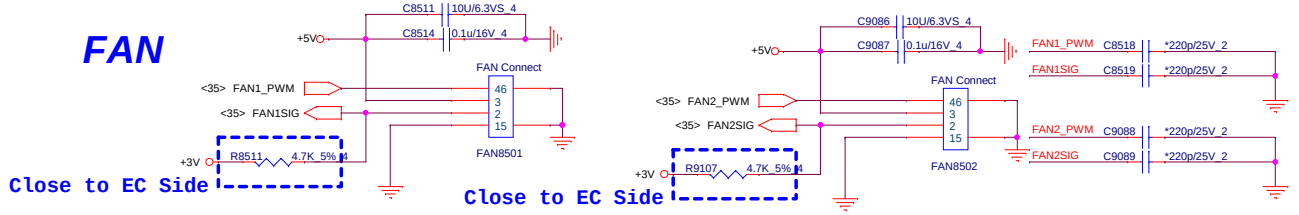
KB LIGHT CONN



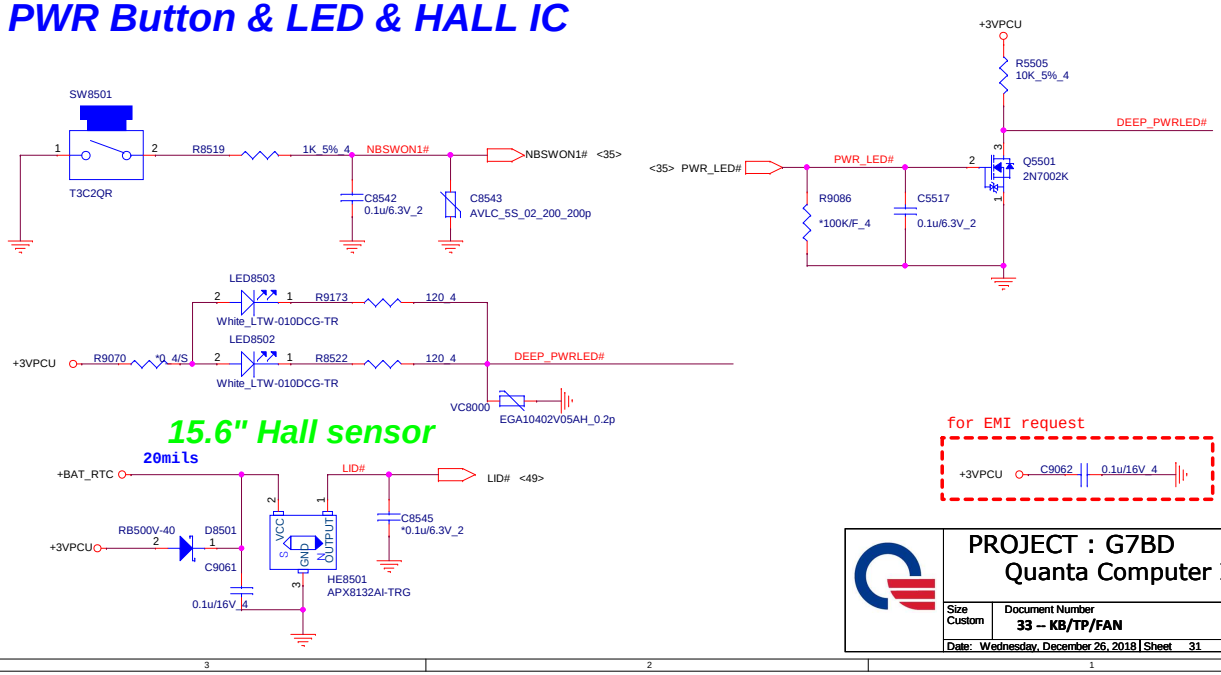
Touch Pad



FAN



PWR Button & LED & HALL IC



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- KB/TP/FAN	1A

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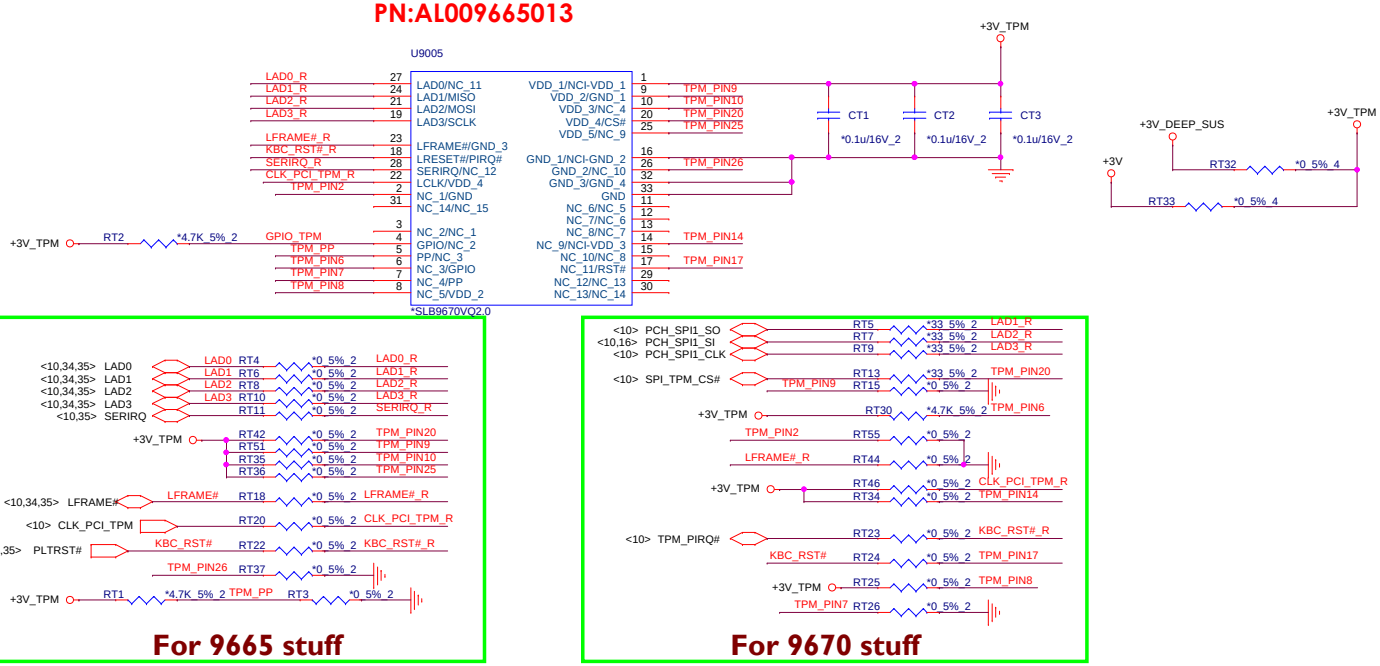
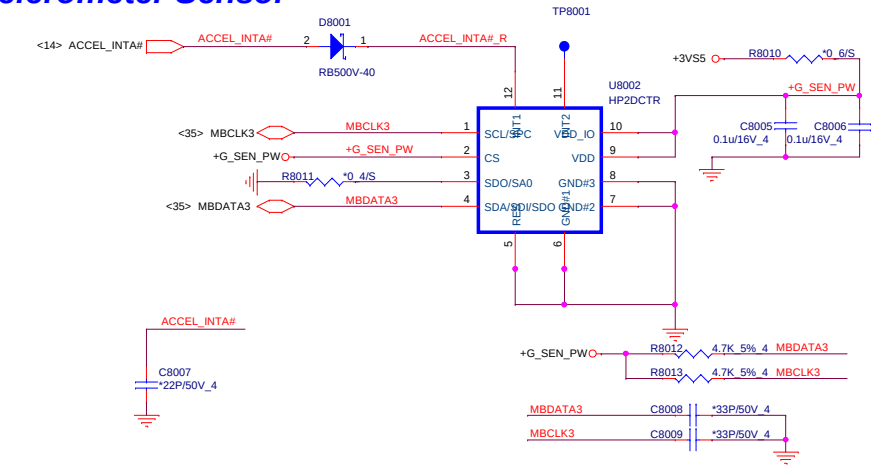
TPM (2.0)

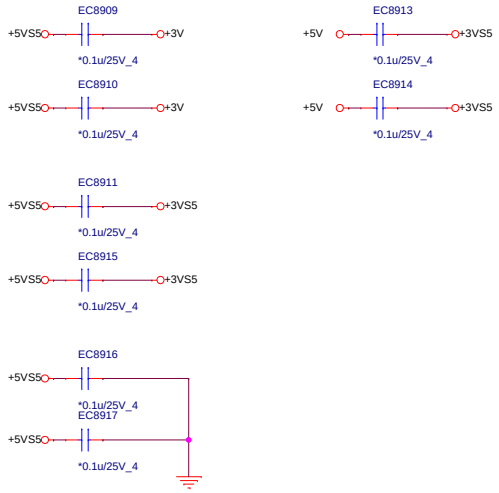
change to FW 5.61
PN:AL009665013



Accelerometer Sensor



EMI Solution



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	34 – TPM/G-Sensor/IR CAM	1A

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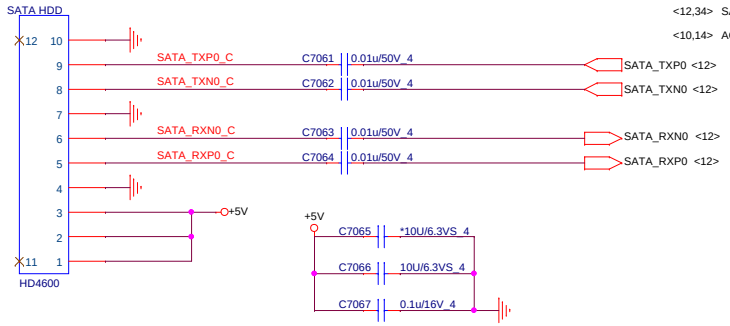
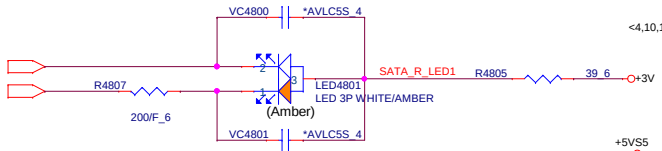
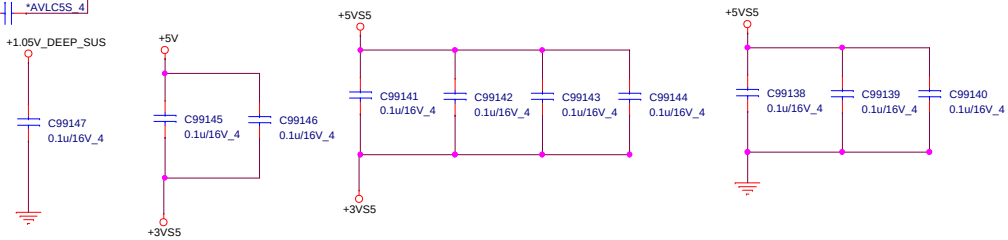
SATA HDD & LED

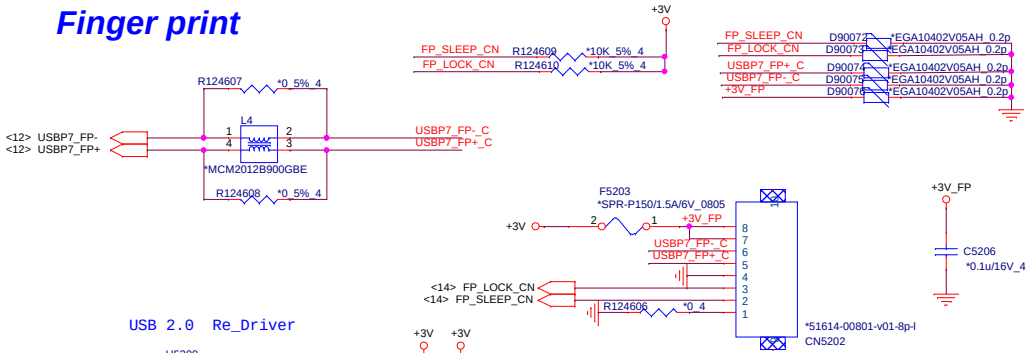
SATA LED



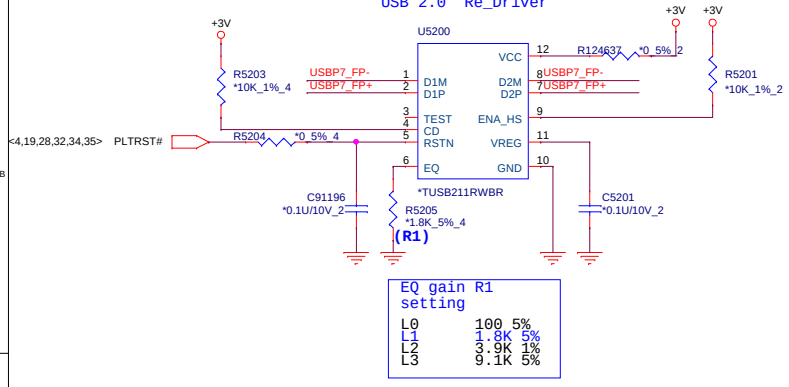




Finger print

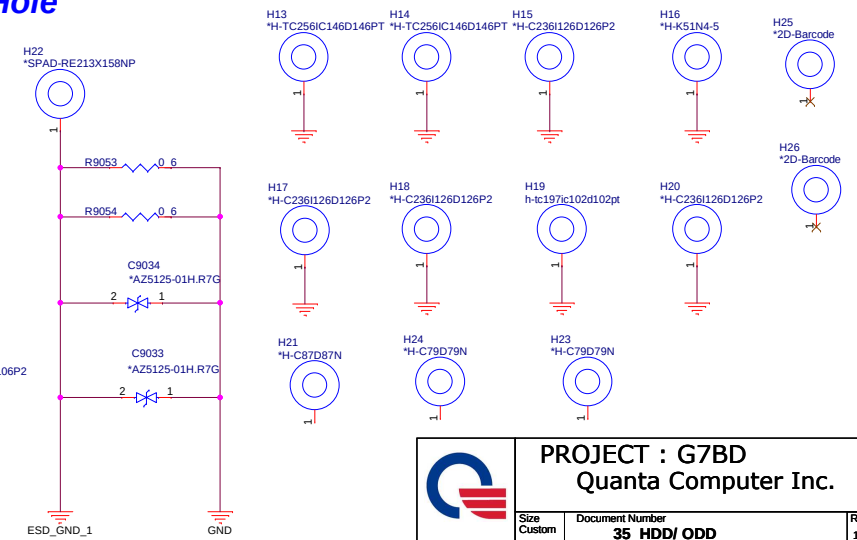


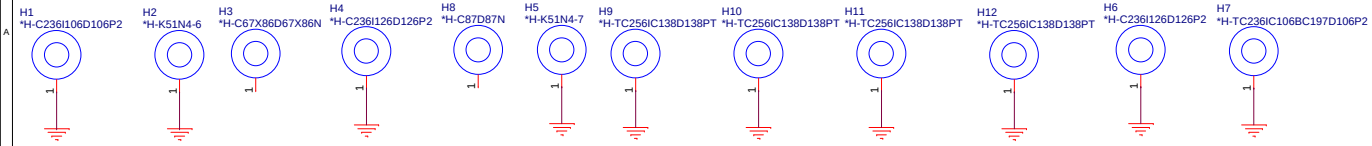
USB 2.0 Re_Driver



EQ gain R1 setting	
L0	100 5%
L1	1.8K 5%
L2	3.9K 1%
L3	9.1K 5%

Hole





PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 HDD/ ODD	1A

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PCIE/SATA SSD

CN6001
SSD_NGFF_CONN_75P

NGFF

100 mils

<12> PCIE_RXN9
<12> PCIE_RXP9
<12> PCIE_TXN9
<12> PCIE_TXP9
<12> PCIE_RXN10
<12> PCIE_RXP10
<12> PCIE_TXN10
<12> PCIE_TXP10
<12> PCIE_RXN11
<12> PCIE_RXP11
<12> PCIE_TXN11
<12> PCIE_TXP11
<12> SATA_RXP2
<12> SATA_RXN2
<12> SATA_TXN2
<12> SATA_TXP2
<13> CLK_PCIE_SSDN
<13> CLK_PCIE_SSDP

SATA_TXN9 C9080 0.22U/10V_4 SATA_TXN9_C
SATA_TXP9 C9081 0.22U/10V_4 SATA_TXP9_C
SATA_TXN10 C9082 0.22U/10V_4 SATA_TXN10_C
SATA_TXP10 C9083 0.22U/10V_4 SATA_TXP10_C
SATA_TXN11 C9056 0.22U/10V_4 SATA_TXN11_C
SATA_TXP11 C9057 0.22U/10V_4 SATA_TXP11_C
R9166 0_4 SATA_RXP2_C
R9168 0_4 SATA_RXN2_C
C6055 0.22U/10V_4 SATA_TXN2_C
C6056 0.22U/10V_4 SATA_TXP2_C

+3V_SSD 1.4A
R6002 *0_8/S +3V
C6004 0.01u/50V_4
C6002 0.1u/16V_4
C6003 4.7u/6.3V_4

For PCIe SSD SATA LED
D6541 RB500V-40
SATA_LED# <12,33>
R6669 10K_5%_4
R6003 10K_5%_4 +3V
R6004 *0_4 DEVSLP0 <12>

R6006 *0_4/S
PLTRST# <4,19,28,32,33,34,35>
PCIE_CLKREQ_SSD# <13>

<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,35,42,45,46,47> +3V
<25,26,27,31,32,33,45> +5V
<6,13,31,35,36,38,49> +3VPCU

<12> SATA_RXN1A
<12> SATA_RXP1A
<12> SATA_TXN1A
<12> SATA_TXP1A
C91032 *0.1u/16V_4 SATA_RXN2_C
C91033 *0.1u/16V_4 SATA_RXP2_C
C91034 *0.1u/16V_4 SATA_TXN2_C
C91035 *0.1u/16V_4 SATA_TXP2_C

Colay SATA SSD

+3V
R6008 100K_1%_4
PEDET
<12> GPIO35
R6010 *0_4/S
Q6001 2N7002K
R9167 *0_4

M key
only SATA-->GND

N/A_1 SUSCLK
PEDET(NC-PCIE/GND-SATA)
GND10 3.3Vaux_7
GND11 3.3Vaux_8
GND12 3.3Vaux_9
TP6002
R6009 *0_8/S +3V
EC6002 470p/50V_4
EC6003 10u/6.3V_4
EC6004 10u/6.3V_4

ngff-apci0050-p002h-75p-km

Support Wake Function(Reserve)

+3V_WLAN_P
REQ_WLAN# Q6004A *2N7002KDW PCIE_CLKREQ_WLAN# <13,34>
+3V_WLAN_P
MINICAR_PME# Q6004B *2N7002KDW PCIE_WAKE# <4,28>

R6016 4.7K_5%_4 MINICAR_PME#
R6019 *10K_4 REQ_WLAN#

For EMI Suggestion
CLK_24M_DEBUG R6020 *0_4 EC6001 *33P/50V_4
PCIE_WAKE# EC6005 *220P/50V_4

REQ_WLAN# R124592 0_4 PCIE_CLKREQ_WLAN# <13,34>

100mils
C99125 0.01U/50V_4
C99126 0.1u/16V_4
C99124 10U/6.3VS_4

100mils
C6013 0.01U/50V_4
C6014 0.1u/16V_4
C6015 10U/6.3VS_4

WLAN

+3VPCU
R124593 10K_5%_4
R4451 10K_5%_4
R4454 200K_5%_4
Q20A 2N7002KDW
C4683 0.022u/25V_4
+3VS5
Q19 PJA3415
100mils
+3V_AOCS
+3V_WLAN_P
C4684 *0.1u/6.3V_2
Q20B 2N7002KDW
<14> CNVi_EN#
R4456 75K_1%_4
<35,39,41,45> MAINON
+5VPCU
R124634 *1M_5%_4
R124635 *22_5%_8
Q20036A *2N7002KDW
R124636 *2M_1%_4
Q20036B *2N7002KDW

CN6002
NFSE0-S6710-TP48

NGFF EKEY

<12> USBP10+
<12> USBP10-
<13> CNV_WR_LANE1_DN
<13> CNV_WR_LANE1_DP
<13> CNV_WR_LANE0_DN
<13> CNV_WR_LANE0_DP
<13> CNV_WR_CLK_DN
<13> CNV_WR_CLK_DP
<12> PCIE_TXP5_WLAN
<12> PCIE_TXN5_WLAN
<12> PCIE_RXP5_WLAN
<12> PCIE_RXN5_WLAN
<13> CLK_PCIE_WLANP
<13> CLK_PCIE_WLANN
REQ_WLAN#
MINICAR_PME#
<13> CNV_WT_LANE1_DN
<13> CNV_WT_LANE1_DP
<13> CNV_WT_LANE0_DN
<13> CNV_WT_LANE0_DP
<13> CNV_WT_CLK_DN
<13> CNV_WT_CLK_DP

WLAN_LED# R6013 4.7K_5%_4 +3V_WLAN_P
R6014 *0_4/S
CNV_RF_RESET#_L
MODEM_CLKREQ_L
CNV_BRI_RSP_L R99161 22/F_4 CNV_BRI_RSP <14>
+1.8V_DEEP_SUS
R124589 20K_1%_4 CNV_BRI_RSP
R124590 20K_1%_4 CNV_RGI_RSP
R124598 *20K_1%_4 CNV_BRI_DT_L
CNV_RGI_DT_L R99160 33.2_1%_4 CNV_RGI_DT <14>
CNV_RGI_RSP_L R99162 22/F_4 CNV_RGI_RSP <14>
CNV_BRI_DT_L R99163 33.2_1%_4 CNV_BRI_DT <14>
+1.8V_DEEP_SUS R124575 20K_1%_4 CNV_RGI_DT_L
SUSCLK_32KHZ R99164 *0_4/S SUSCLK_32K <13>
INT_BT_OFF# PLTRST# <4,19,28,32,33,34,35>
INT_RF_OFF# R6017 10K_5%_4 R6018 10K_5%_8 +3V_WLAN_P
LAD0_R R124601 0_4 LAD0 <10,32,35>
CLK_24M_DEBUG_R R124602 0_4 CLK_24M_DEBUG <10>
LFRAME#_R R124603 0_4 LFRAME# <10,32,35>
PULSAR_38P4M_REFCLK <13>
LAD1 LAD1 <10,32,35>
LAD2 LAD2 <10,32,35>
LAD3 LAD3 <10,32,35>

R124618 0_4
U4023 *NL17SZ08DFT2G
CNV_RF_RESET#_L
CNV_RF_RESET# <14>
R4467 *75K_1%_4
R4468 75K_1%_4
+1.8V_DEEP_SUS

R124617 0_4
U4022 *NL17SZ08DFT2G
MODEM_CLKREQ_L
MODEM_CLKREQ <14>
R4465 *71.5K_1%_4
R4466 71.5K_1%_4
+1.8V_DEEP_SUS

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 -- HDD/WLAN(NGFF)	1A

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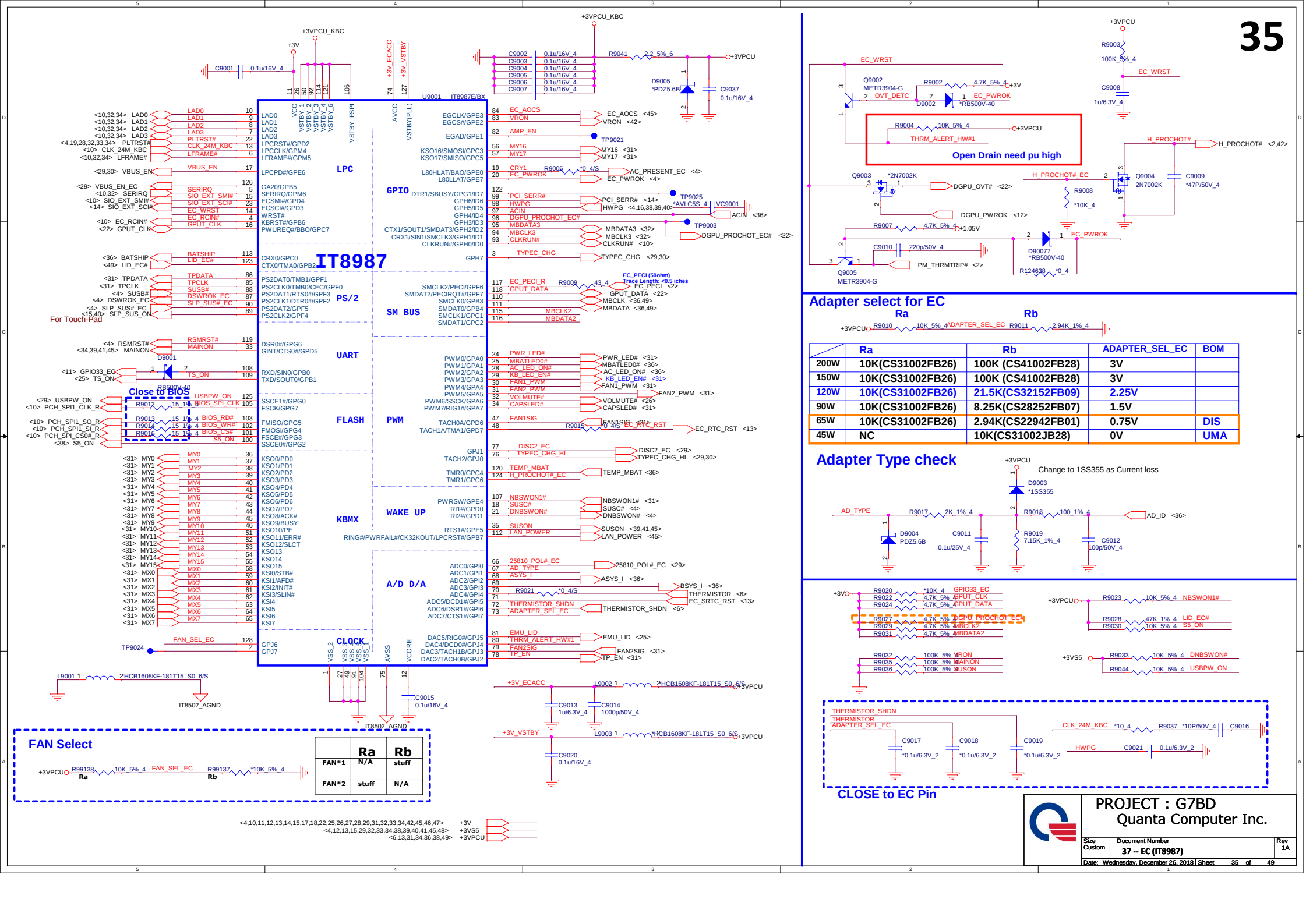

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K(CS32152FB09)	2.25V	
90W	10K(CS31002FB26)	8.25K(CS28252FB07)	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

	Ra	Rb
FAN*1	N/A	stuff
FAN*2	stuff	N/A

DCIN_CONN

G7B WHL_N17S 0202

PV change

PV change

PV change

PV change

PV change

PV change

PV change

MV

3S1P 41Wh

ACDET=14.3V

MIN. BATV=7.2V

4S CELL

SI change

SI change

SI change

SI change

Place this ZVS close to Diode away +VIN

Do Not add test pad on ISLASGATE_1 signal

Do Not add test pad on ISLBGATE signal

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

Fsw=678Khz

default setting 3S battery 2S: 165k 3S:182k 4S: 150K

ICCLIMHW=VCCLIMHW/0.32
ICCLIMHW=120W

ICCLIMHW=VCCLIMHW/0.32
ICCLIMHW=5A

ISL88739BHRZ-T

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL88750)	1A

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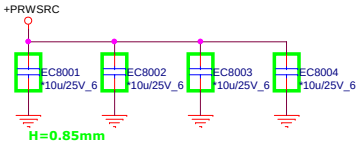
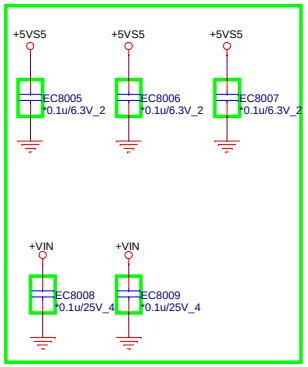
Acoustic Solution



EMI suggestion to reserve



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI FOR POWER RESERVE	1A

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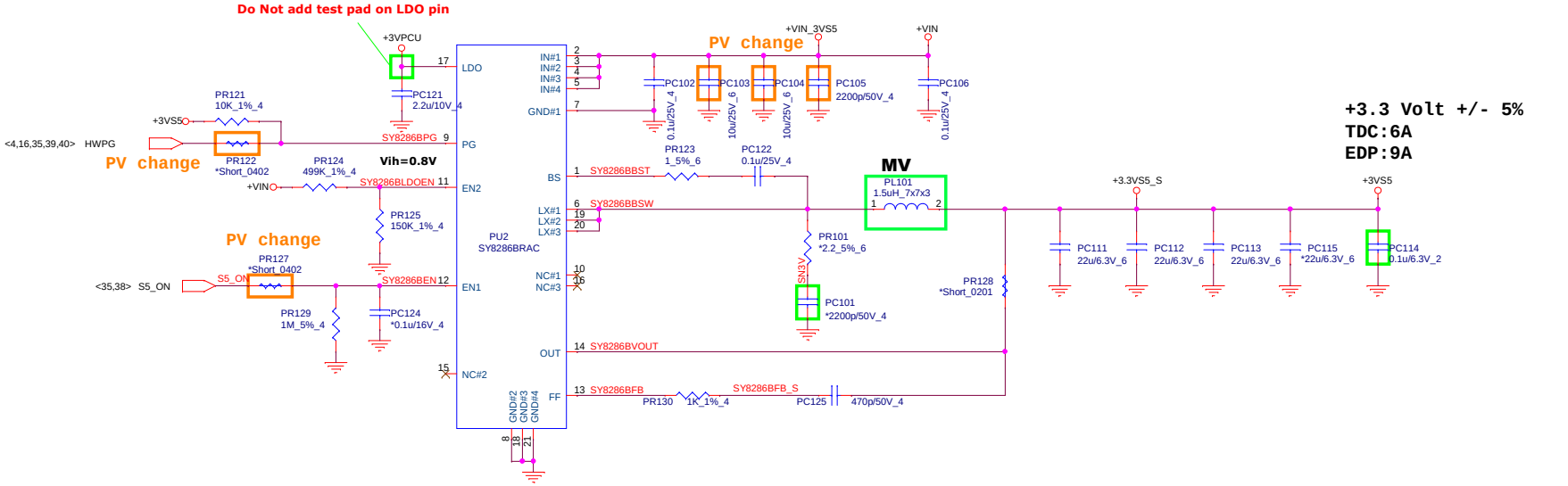
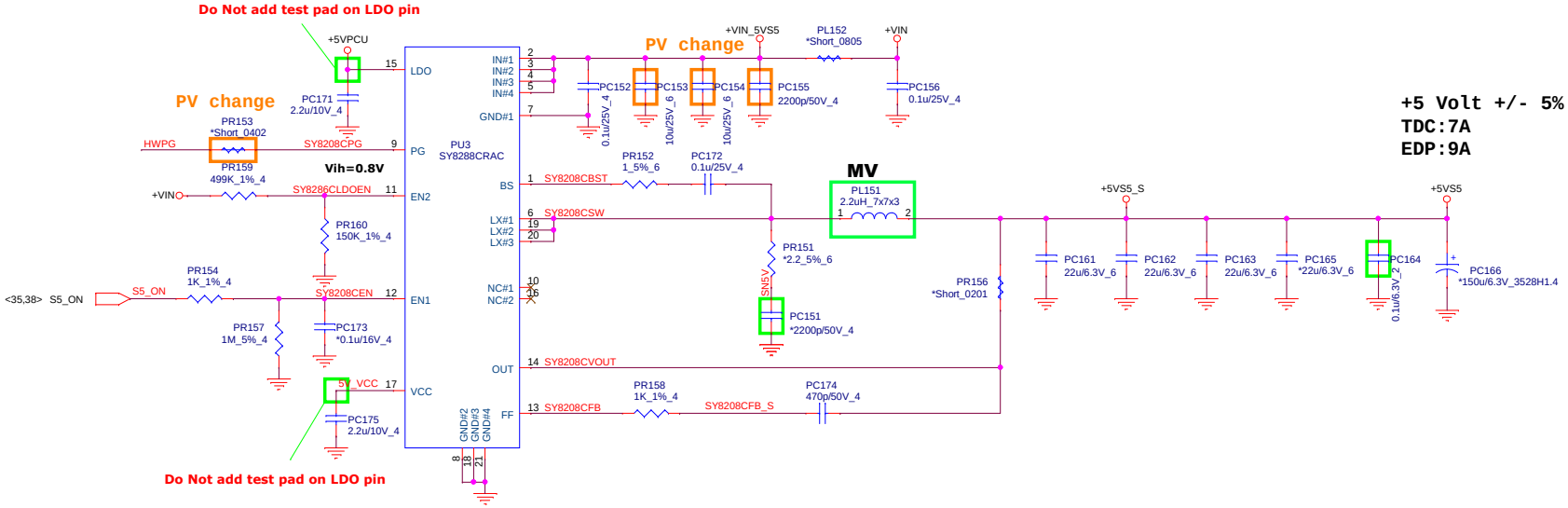
DC/DC +3VS5/+5VS5

+VIN <25,31,36,37,39,40,43,44,46,47>
+3VS5 <4,12,13,15,29,32,33,34,35,39,40,41,45,48>
+5VS5 <4,26,29,30,32,33,37,39,40,41,42,43,45,46,47,48>
+3VPCU <6,13,31,34,35,36,49>
+5VPCU <26,34,36,45,48>





PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3/5VS5(SY8286B/SY8286C)	1A

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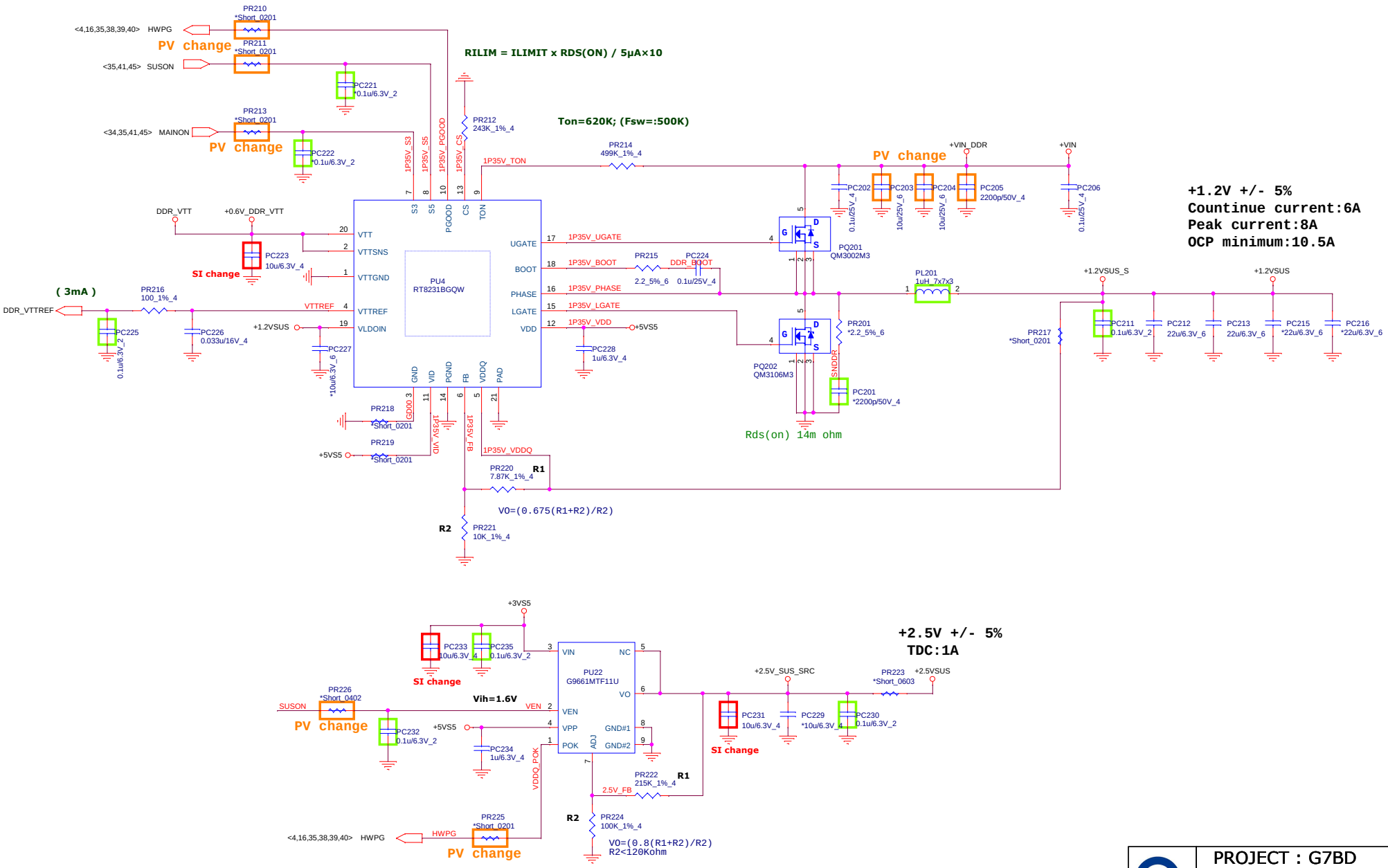
+VIN <25,31,36,37,38,40,43,44,46,47>
+2.5VSUS <17,18>
+1.2VSUS <3,6,17,18,41>
DDR_VTT <17,18>



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR/2.5VSUS(RT8231B)	1A

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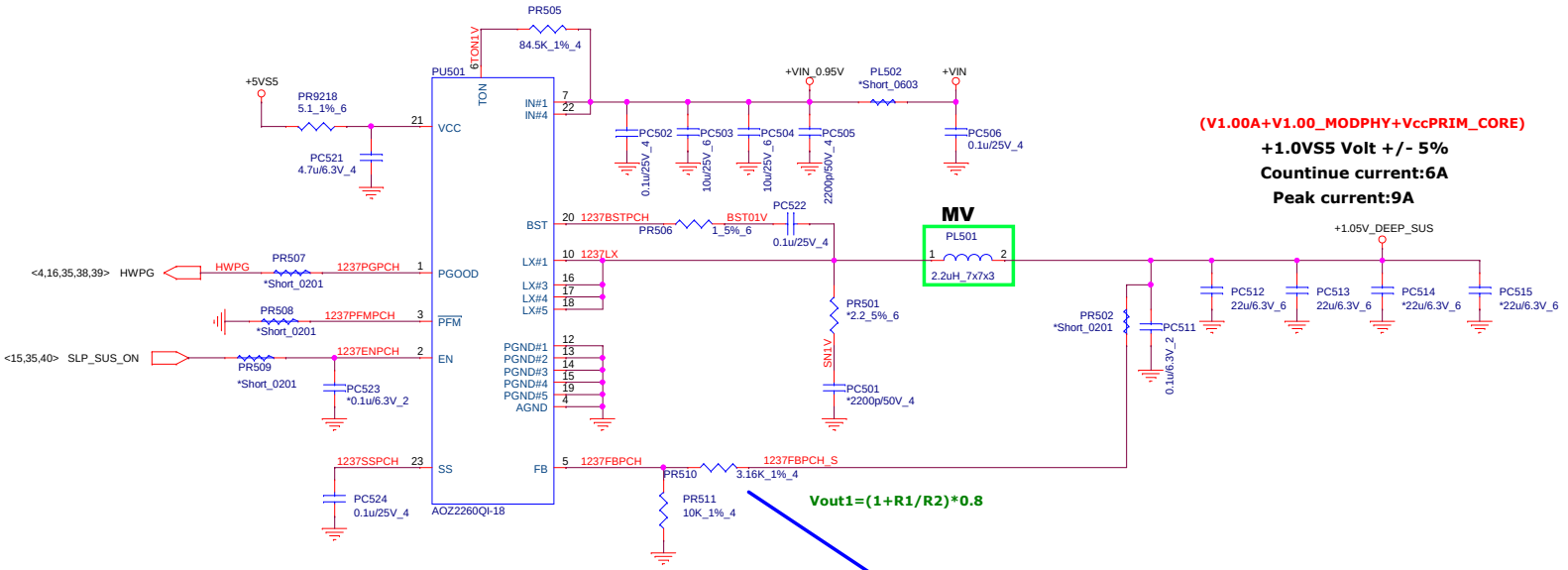
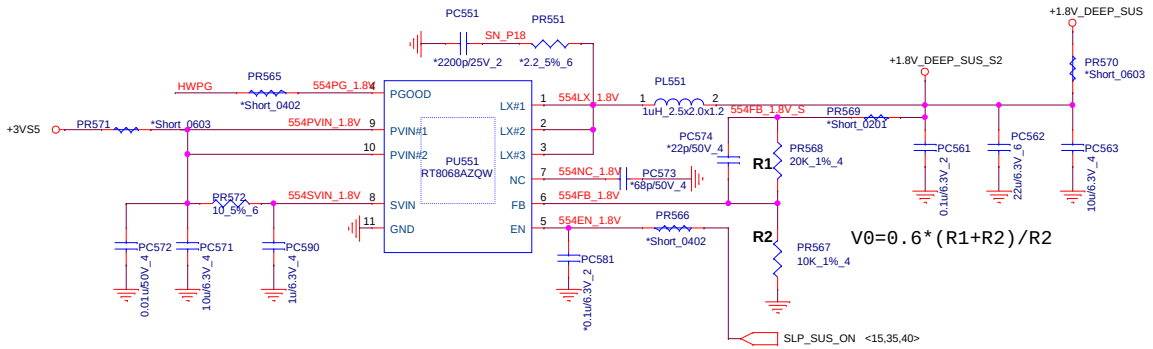
+VIN <25,31,36,37,38,39,43,44,46,47>
+3VS5 <4,12,13,15,29,32,33,34,35,38,39,41,45,48>
+5VS5 <4,26,29,30,32,33,37,38,39,41,42,43,45,46,47,48>
+1.05V_DEEP_SUS <9,15,33,41>
+1.8V_DEEP_SUS <13,15,29,34,45,48>
MAINON <34,35,39,41,45>
+1.5V

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL/WHL	3.16K	CS23162FB04	1.05V

1.8VS5 +/- 3%
TDC:3A
EDP:4A



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+1.8V_DEEP_SUS	1A

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Volume Segment
SKY/KBY-U22/U42/U23e
KBY-G/WHL-U
Vcc_IO: 3.4A/1V
Stuff PU601

Volume Segment
SKY/KBY-H 22/42/44e
Vcc_IO: 5.5A/0.95V
Stuff PU601 & merge 1V_deep_sus

Volume Segment
CNL U22
Vcc_IO: 5.1A/0.95V
Vcc_IO: Can merge +1.05V_deep_sus
Unstuff PU603
Unstuff PU601

Default setting
Volume Segment
CFL H6/H4
Vcc_IO: 6.4A/0.95V
Stuff PU603
Unstuff PU601

Volume Segment
Vcc_ST: 0.19A
Vcc_PLL: 0.19A
<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Volume Segment
Vcc_STG: 0.02A
Vcc_IO: 4.06A
<= 10ms full load ready

Imax:4.06A
Imax:0.02A
Imax:0.02A

<= 240us, full load ready
TDC:0.26A

+5VS5
PC1557 0.1u/6.3V_2
PU1503 M74VHC1GT08DFT2G
PR1552 *Short_0201
PR1551 *0_5%_2
<9,45> SUSON

+1.05V_DEEP_SUS
PC629 0.1u/6.3V_2
PR653 47K_1%_4
VCCSTPLL_EN_1
PC630 *1000p/25V_2
PQ607 DMG3414U-7
+VCCSTPLL_S2
PR652 *Short_0603
+VCCSTPLL
PC631 0.1u/6.3V_2
PC632 *10u/6.3V_4

+VCCSTPLL
PR655 *22_5%_8
VCCSTPLL_DIS2
PR657 *1M_5%_4
VCCSTPLL_DIS1
PQ608A *2N7002KDW
PR656 *2M_1%_4
PQ608B *2N7002KDW

+1.05V_DEEP_SUS
PC601 1u/6.3V_4
PU601
VIN#1
VIN#2
VIN#3
VBIAS
VOUT
GND
ON
AOZ1335DI_2
+3VS5
PC620 0.1u/6.3V_2
PC621 *0.1u/6.3V_2
MAINON
PR610 *0_5%_2
PR651 *Short_0201
VCCIO_EN
VCCIO_EN1

+VCCIO
PR649 *0_5%_6
+1.05V
PC611 0.1u/6.3V_2
PC612 *10u/6.3V_4

+5VS5
PC622 *0.1u/6.3V_2
<13,41> PWR_GATE#
<34,35,39,41,45> MAINON
PR611 *0_5%_2
PR612 *0_5%_2
17SZ_EN1
17SZ_EN2
PU602 *M74VHC1GT08DFT2G
VCCPLL_OC_EN_2
PR617 *0_5%_2
VCCIO_EN
PR654 *0_5%_2

PR613 *47K_1%_4
VCCPLL_OC_EN_1
+1.2VSUS
PC602 *0.1u/6.3V_2
PC623 *1000p/25V_2
PQ601 *DMG3414U-7
+1.2V_VCCPLL_OC_S2
PL603 *Short_0603
+1.2V_VCCPLL_OC
PC615 *0.1u/6.3V_2
PC616 *10u/6.3V_4

+1.2V_VCCPLL_OC
PR614 *22_5%_8
VCCPLL_OC_DIS2
+5VS5
PR615 *1M_5%_4
VCCPLL_OC_DIS1
PQ603A *2N7002KDW
PR616 *2M_1%_4
PQ603B *2N7002KDW

+5VS5
PC624 0.1u/6.3V_2
<13,41> PWR_GATE#
<34,35,39,41,45> MAINON
PR620 *Short_0201
PR619 *Short_0201
17SZ_EN5
17SZ_EN6
PU603 M74VHC1GT08DFT2G
VCCIO_EN

PR647 47K_1%_4
VCCSTG_EN_1
PC627 *1000p/25V_2
PQ606 DMG3414U-7
VCCSTG_S2
PR650 *Short_0603
+1.05V
PC625 0.1u/6.3V_2
PC628 *10u/6.3V_4

+1.05V_DEEP_SUS
PC626 0.1u/6.3V_2

+1.05V
+5VS5
PR648 *22_5%_8
VCCSTG_DIS2
PR645 *1M_5%_4
VCCSTG_DIS1
PQ602A *2N7002KDW
PR646 *2M_1%_4
PQ602B *2N7002KDW

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

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31A for ICCMAX=1V

6A for ICCMAX=1V

70A for ICCMAX=1V

Default setting

	Rd
U22	
U42	

	Re
U22	
U42	

	Rf
U22	
U42	

place close to core inductor

place close to GT MOSFET

place close to VCORE MOSFET

PU301 RT3602AHGQW

	Ra	Rb/Rc
U22	N/A	stuff
U42	stuff	N/A

Default setting

PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VR IC (RT3602AH)	3A

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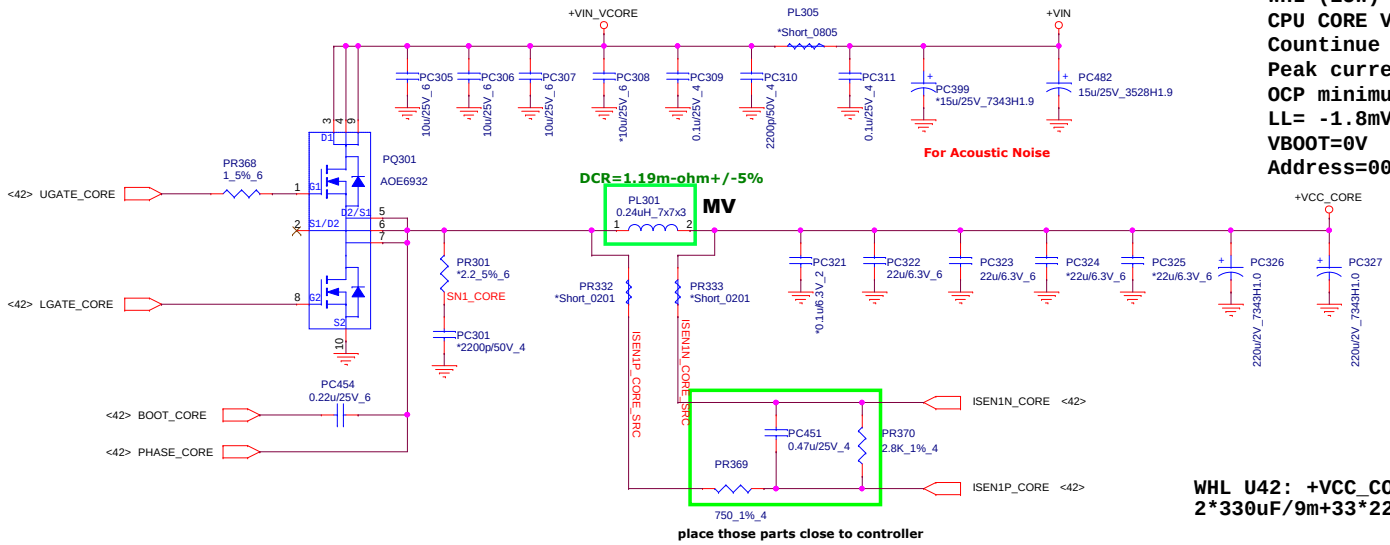
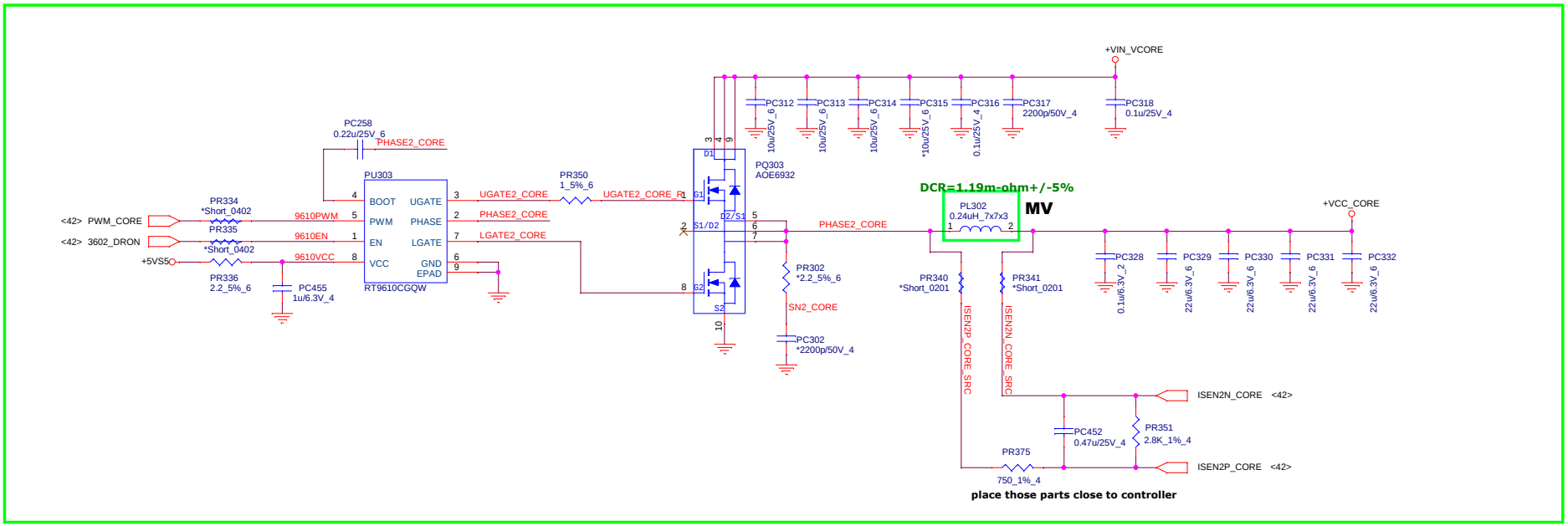
+VIN <25,31,36,37,38,39,40,44,46,47>
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,45,46,47,48>

WHL (15W)
CPU CORE Volt
Countinue current:42A
Peak current:70A
OCP minimum:110A
LL= -1.8mV/A/TBD
VBOOT=0V
Address=00h



WHL U42: +VCC_CORE
2*330uF/9m+33*22uF MLCC (total with EE)



PROJECT : G7BD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	3A

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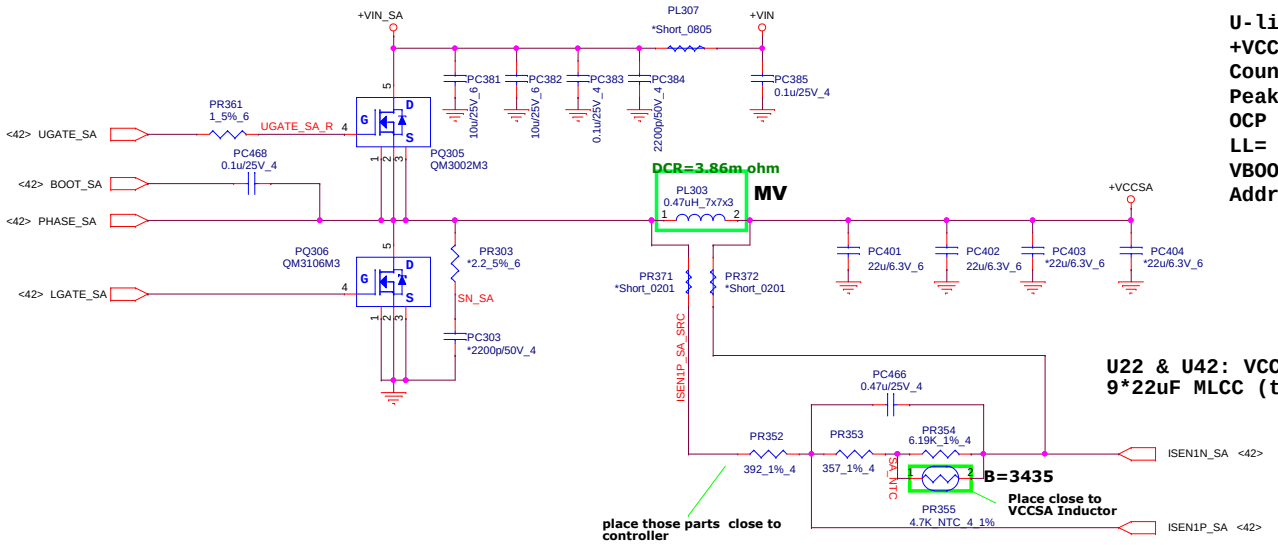
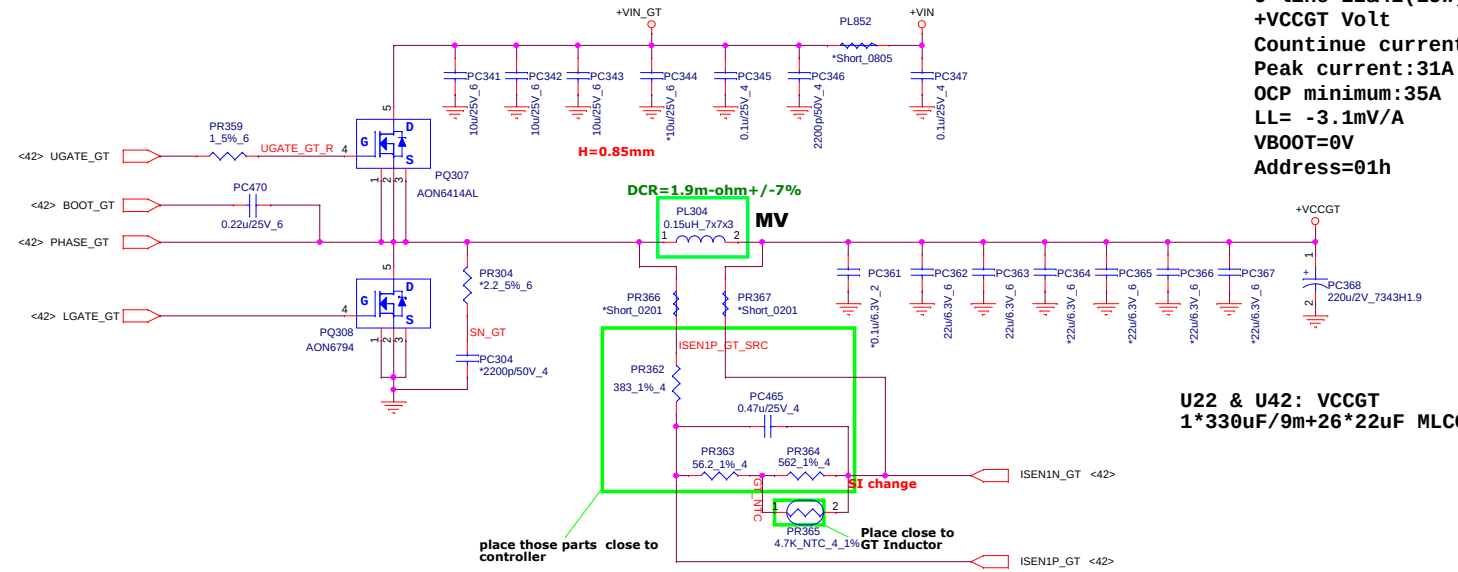
+VIN <25,31,36,37,38,39,40,43,46,47>
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,47,48>
+VCCSA <6,42>
+VCCGT <7,42>



U-line 22&42(15W)
+VCCSA Volt
Countinue current:4A
Peak current:6A
OCP minimum:8A
LL= -10.3mV/A
VBOOT=1.05V
Address=02h

U22 & U42: VCCSA
9*22uF MLCC (total with EE)



U-line 22&42(15W)
+VCCGT Volt
Countinue current:18A
Peak current:31A
OCP minimum:35A
LL= -3.1mV/A
VBOOT=0V
Address=01h

U22 & U42: VCCGT
1*330uF/9m+26*22uF MLCC (total with EE)

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Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	3A

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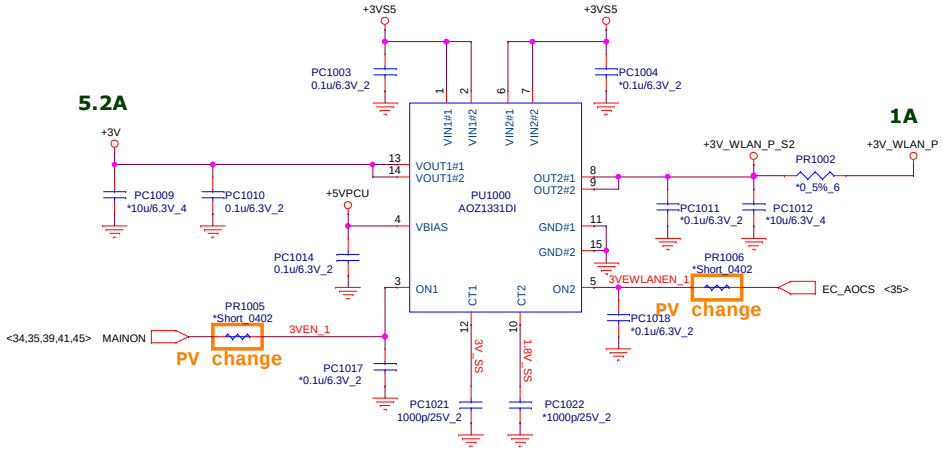

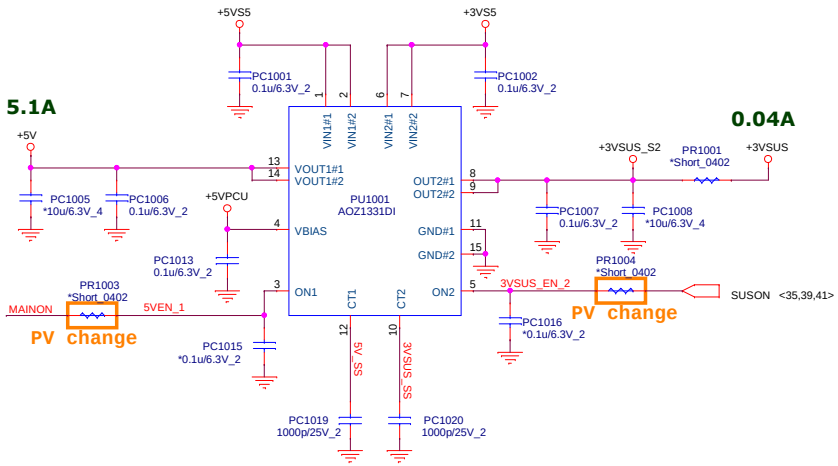

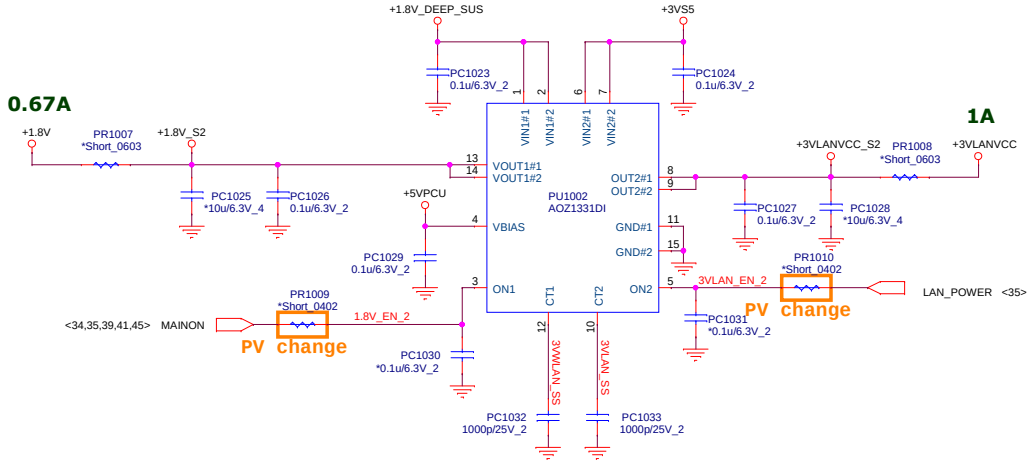

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Size	Document Number	Rev
	Load switch IC(APL3523A)	1A

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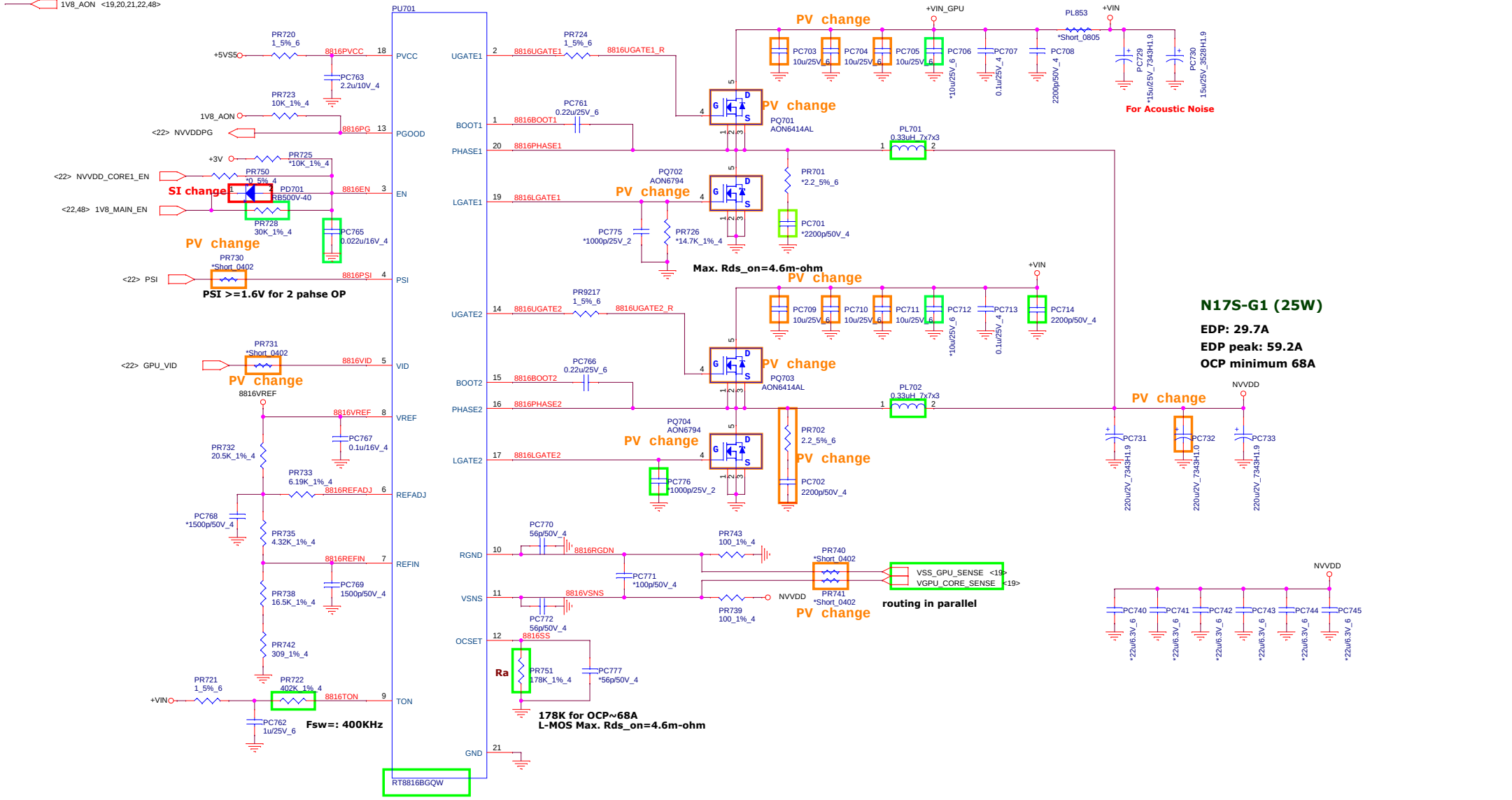
VGA Core

+3V <4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,47>
+VIN <25,31,36,37,38,39,40,43,44,47>
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,47,48>
NVVDD <19>
1V8_AON <19,20,21,22,48>



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Size	Document Number	Rev
Custom	+VGACORE (RT8813A)	3A

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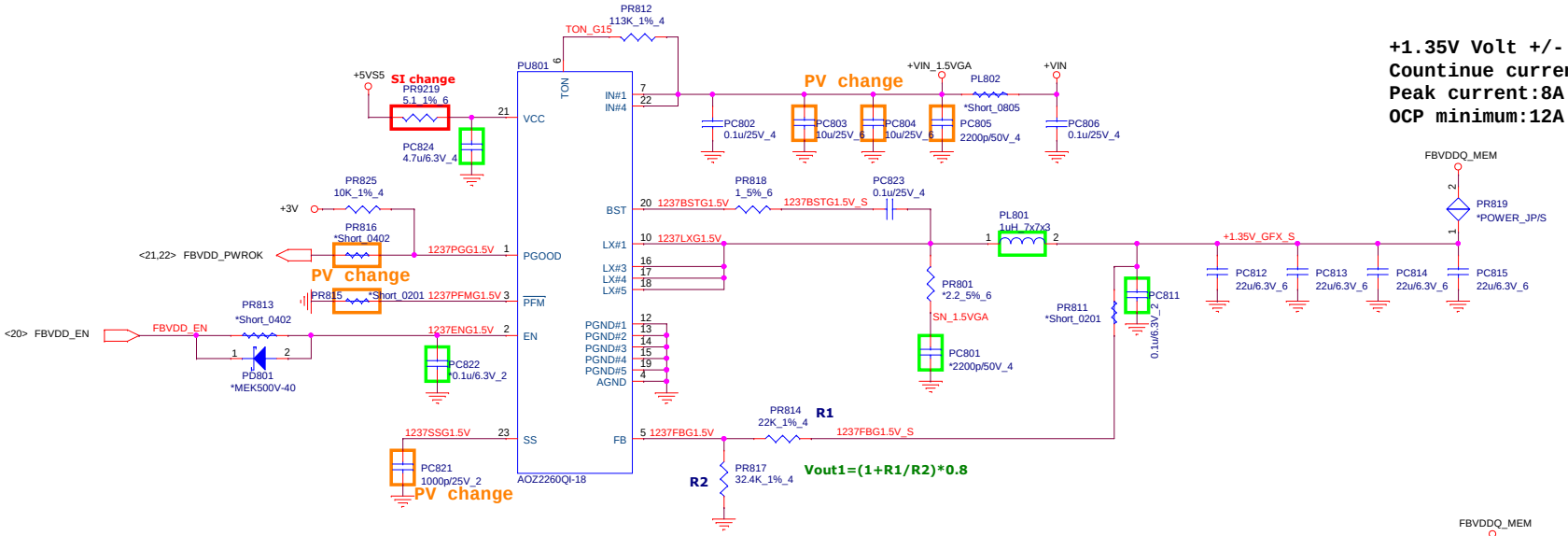
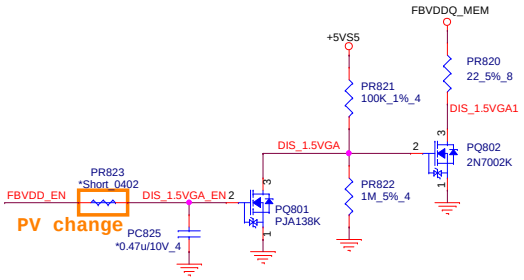
+VIN <25,31,36,37,38,39,40,43,44,46>
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,48>
FBVDDQ_MEM <20,21,23>



+1.35V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



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Size	Document Number	Rev
Custom	+1.35V_VGA(AOZ1237)	1A

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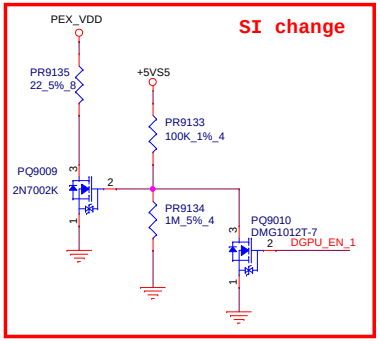
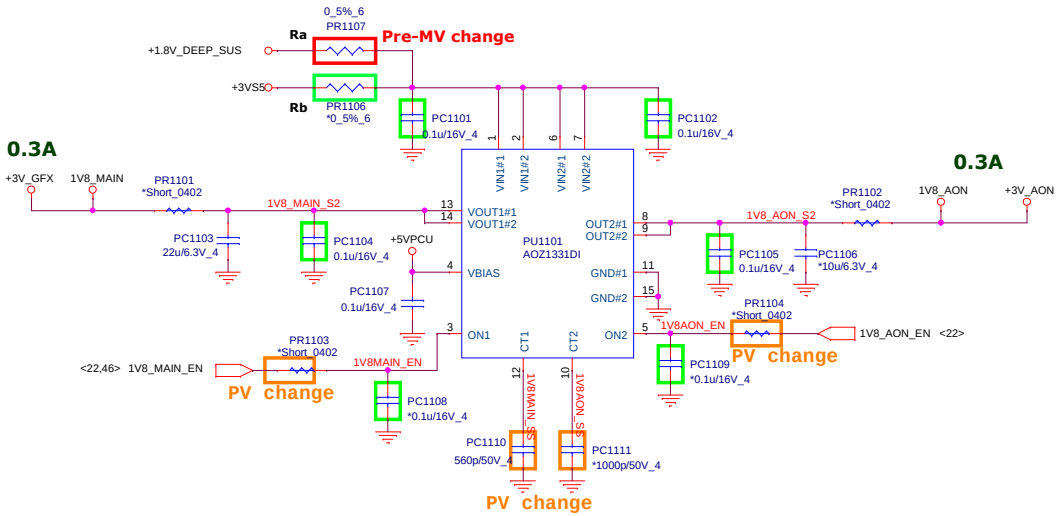
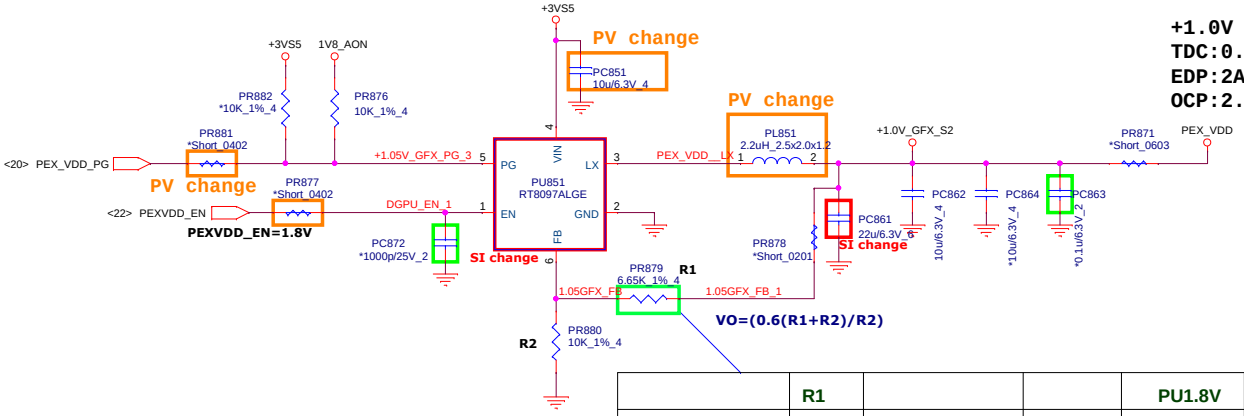
+3VS5 <4,12,13,15,29,32,33,34,35,38,39,40,41,45>
+5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,47>
1V8_MAIN <19,21,22>
1V8_AON <19,20,21,22,46>
+1.2VSUS <3,6,17,18,39,41>
PEX_VDD <19,21>
MAINON <34,35,39,41,45>

N17S stuff Ra & N/A Rb
N16S stuff Rb & N/A Ra







+1.0V +/- 5%
TDC:0.79A
EDP:2A
OCP:2.5A

	R1			PU1.8V	Rc	Rd
N17P N17S	6.65K	CS26652FB06	1V	Unstuff	Unstuff	Stuff
N16S GTR	7.5K	CS27502FB11	1.05V	Unstuff	Stuff	Unstuff

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Size	Document Number	Rev
Custom	1.05V_VGA/3V_VGA	1A
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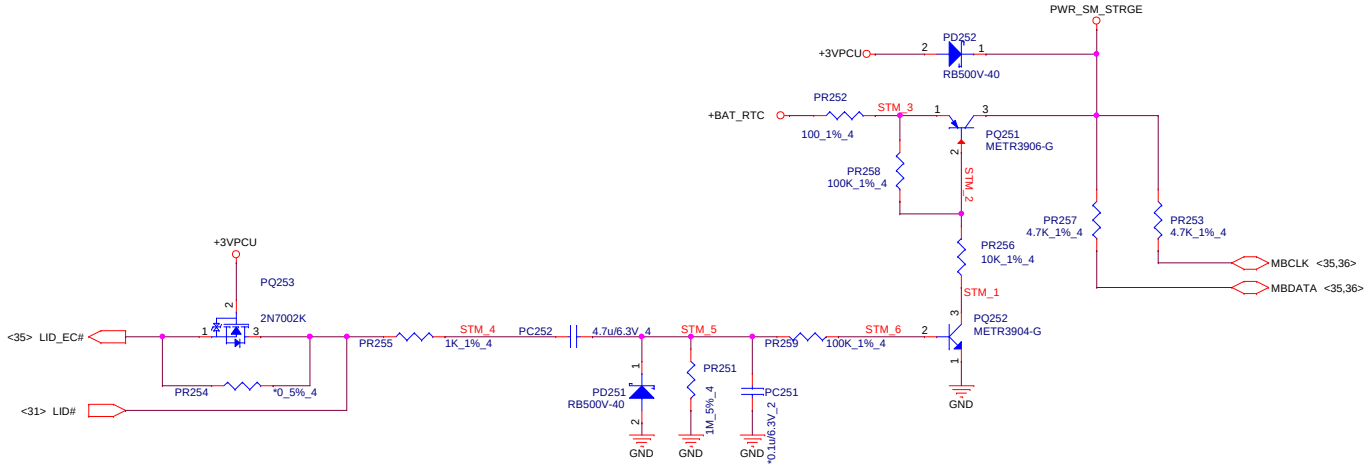
<4,13,15,31,36> +BAT_RTC
<6,13,31,34,35,36,38> +3VPCU



PROJECT : G7BD Quanta Computer Inc.		
Size Custom	Document Number STORAGE MODE	Rev 1A
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