Compal Confidential

Intel MB Schematic Document

2019 OMEN 17.3" Santorini

FPC72 LA-H492PR01

Date : 2018/09/28

Version: v0.1

15.6": FPC54 LA-H481PR(N17)
LA-H482P(N18)
17" : FPC72 LA-H491P(N17)
FPC72 LA-H492P(N18)

15" to 17" different:
01. Add SSD#2
02. Combo HP Jack to separated MIC jack
03. JDIMM2 to STD. revision.
04. Screw Location
05. BATT from SMT to DIP
06. ACIN CONN
07. GPU Core from 6phase to 4phase

(Modified&Ref from: 01."DPF50_LA-F842PR1A_201800411(PPAV)")
02.GPU:"DPF50_LA-F863PR01_180723(PPAV)")
03.GPU reference:"EH78F_LA-G161PR01_0810")

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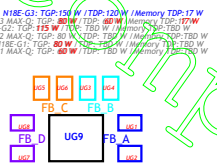
Size	Custom	Document Number	FPC72 LA-H492P
Rev	v0.1		
Date:	Friday, September 28, 2018	Sheet	1 of 100



UG108 OVR-M NCP45491XMNTWG P.22

UG2,UG1 8Gb_256Mx2Chx16 :2pcs P.35 — FBA x64
UG4,UG3 8Gb_256Mx2Chx16 :2pcs P.35 — FBB x64
UG6,UG5 8Gb_256Mx2Chx16 :2pcs P.36 — FBC x64
UG8,UG7 8Gb_256Mx2Chx16 :2pcs P.36 — FBD x64

UG9 GPU nVidia N18E-G3
256bits Two Channelsx16 (single sided)
37.5mm x 37.5mm P.27-34
*GB4B-256

PEG x16 P.9

UC1 Intel Coffee Lake- H 6C+GT2 P.7 P.8
TDP: 45W
42mm x 28mm
BGA 1440-Pin
14nm
0.65mm Ball Pitch
1 Die 6+2:16.5x9.1mm 8+2:19.4x9.1mm P.6~13
P.9

DDR4_1.2V Interleaved (*1DPC)

AREA BACK
Ch0 (REV.) DDR4 SO-DIMM JDIMM1 P.23
Ch1 (STD.) DDR4 SO-DIMM JDIMM2 P.24
AREA FRONT
*(17" Ch1:JDIMM2 is REV. type)

JHDMI1 HDMI Conn. P.40 — HDMI Redriver UV3 PS8409 P.40 — HDMI 2.0 — IFPC
JmDP1 Mini_DP Conn. P.39 — DP Repeter UV43 TUSB546 P.40 — DP 1.4 — IFPA
JEDP1 eDP Conn. P.38 — eDP — IFPD

x4 DMI 3.0 P.16

UH1 HM370
Cannon Lake PCH-H
24mm x 25mm
BGA 874-Pin
0.5mm Ball Pitch
P.14~21

JRJ45 RJ-45 P.51 — GLAN UL1 RTL8118AS P.51 — x1, Port #14 — PCIe P.14 P.17

JUSB1 USB3.0 Conn.
UR1 Card Reader RTS5237S-GRT — x1, Port #15
HDD LED
JIO1 I/O Conn. P.71
US1 USB Charger TPS2546 P.71 — USB 2.0 Port #1
USB 3.0 Port #1
x1, Port #15

JWLAN1 WLAN+BT (M.2 Key E) P.52 — CNVi
USB 2.0 Port #14
x1, Port #16

JSSD1 SSD#1 (M.2 Key M) P.67 — x4, Port #12/11/10/9 (SATA#1A)

JSSD2 SSD#2 (M.2 Key M) P.68 — *for 17" only — x4, Port #21/22/23/24 (SATA#4)

PJP1 ACIN Conn. P.82
JPWR1 PWR BTN Conn.
JKBL1 KBL Conn. P.63
PUB01 Charger P.84
PJPB1 Battery Conn. P.83
U9 G-Sensor HP2DCTR P.66

JHDD1 2.5" HDD P.67 — SATA Port #0b P.17 P.18

UK1 EC ENE KB9542Q-B P.58
SMBus#1 SMBus#2
LPC P.17
ESB PS2#3
SMBus P.18
JTP1 Touch Pad P.63

UG9 GPU P.25
JKB1 Int. KBD P.63
JFAN1 JFAN2 FAN P.77
U7 Hall Sensor P.63
UC3 Thermal Sensor P.66

JLB1 RGB Conn. P62
UE1 RGB LED Driver TLC59116 P62
UK2 Extend I/O KC3810 P.59

SPI P.16
UT1 TPM 2.0 SLB9670VQ2.0 P.66
UH2 BIOS 16MB W25Q128JVSIQ P.16

GPU IFPE
UT11 DP Repeter TUSB546 P.47
JTAG1 Debug
U1 Thunderbolt Titan Ridge JHL7340 P.48
JUSBC1 USB Type-C P.50
PCIex4, Port #17/18/19/20
UU4 Type-C PD TPS65987S P.50 — Port #4
UU5 SPI ROM W25X20CLSNIG P.50

USB 3.0 P.17
Port #2 — JUSB2 USB3.0 Conn. P.71
Port #3 — JUSB3 USB3.0 Conn. P.71
USB 2.0 P.14
Port #5 — JEDP1 HD/IR Camera P.38

HDA P.18
UA1 Codec AL3292 P.56
JHP1 Combo Jack P.56
JMIC1 Stereo Mic Jack P.56 — *for 17" only
I2S
UAA1 ALC1305 P.57
JSPK1 Speaker Conn. P.57

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Date: Friday, September 28, 2018	Sheet 2 of 100		

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
1 --> 0.2	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
2 --> 0.3	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
3 --> 0.4	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
4 --> 0.5					
5 --> 0.6					
6 --> 0.7					
7 --> 0.8					
8 --> 0.9					
9 --> 1.0					
10 --> 1.1					
11 --> 1.2					
12 --> 1.3					
13 --> 1.4					
14 --> 1.5					
15 --> 1.6					
16 --> 1.7					
17 --> 1.8					
18 --> 1.9					
19 --> 2.0					

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	---		
DDI2	---		
DDI3	---		
eDP	---		PCH_EDP_HPD_R

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM2	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x4F	0X9E	0X9F

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
SMBUS Port2	+3VL	PCH	TBC		
		GPU	0x4F	0X9E	0X9F
		THERMAL	0x48	0X90	0x91
		PD (Default)	0x38	0X70	0x71
		Type-C MUX	0x10 0x11	0X20 0X22	0x21 0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3V_PCH_PRIM				
I2C_1_SCL I2C_1_SDA	+3VS				

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
UMA	UMA@	
DIS	DIS@	
eSPI I/F	ESPI@	LPC@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@ VGAEMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1 Gen1/Gen2	1			USB3.1 Port 1		
1	USB3.1_2 Gen1/Gen2	2			USB3.1 Port 2		
2	USB3.1_3 Gen1/Gen2	3			USB3.1 Port 3		
3	USB3.1_4 Gen1/Gen2	4			USB Type-C Port		TBT
4	USB3.1_5 Gen1	5					
5	USB3.1_6 Gen1	6					
6	USB3.1_7 Gen1	7					
7	USB3.1_8 Gen1	8					
8	HM370 disable						
9	HM370 disable						
10	/ GbE						
11	HM370 disable						
12	HM370 disable						
13	HM370 disable						
14	PCIE_9 / GbE		9		SSD-1	CLK2 & CLKREQ#2	
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0			
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	Ethernet	CLK5 & CLKREQ#5	
20	PCIE_15		15		Card Reader	CLK3 & CLKREQ#3	
21	PCIE_16		16		WLAN	CLK1 & CLKREQ#1	
22	PCIE_17 / SATA_4		17	4	Thunderbolt	CLK0 & CLKREQ#0	
23	PCIE_18 / SATA_5		18	5			
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21		SSD-2 or Optane	CLK6 & CLKREQ#6	
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 Port 1
2	USB3.1 Port 2
3	USB3.1 Port 3
4	USB3.1 Type-C Port
5	
6	Camera/IR Camera
7	
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

GPU IFPx Table

Port	Function
A	mDP
B	--
C	HDMI 2.0
D	eDP
E	DP source to TBT
F	--

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

BOM Number	Load BOM Option
431AAN32L01	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNCT@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@
431AAN32L02	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNVH@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@

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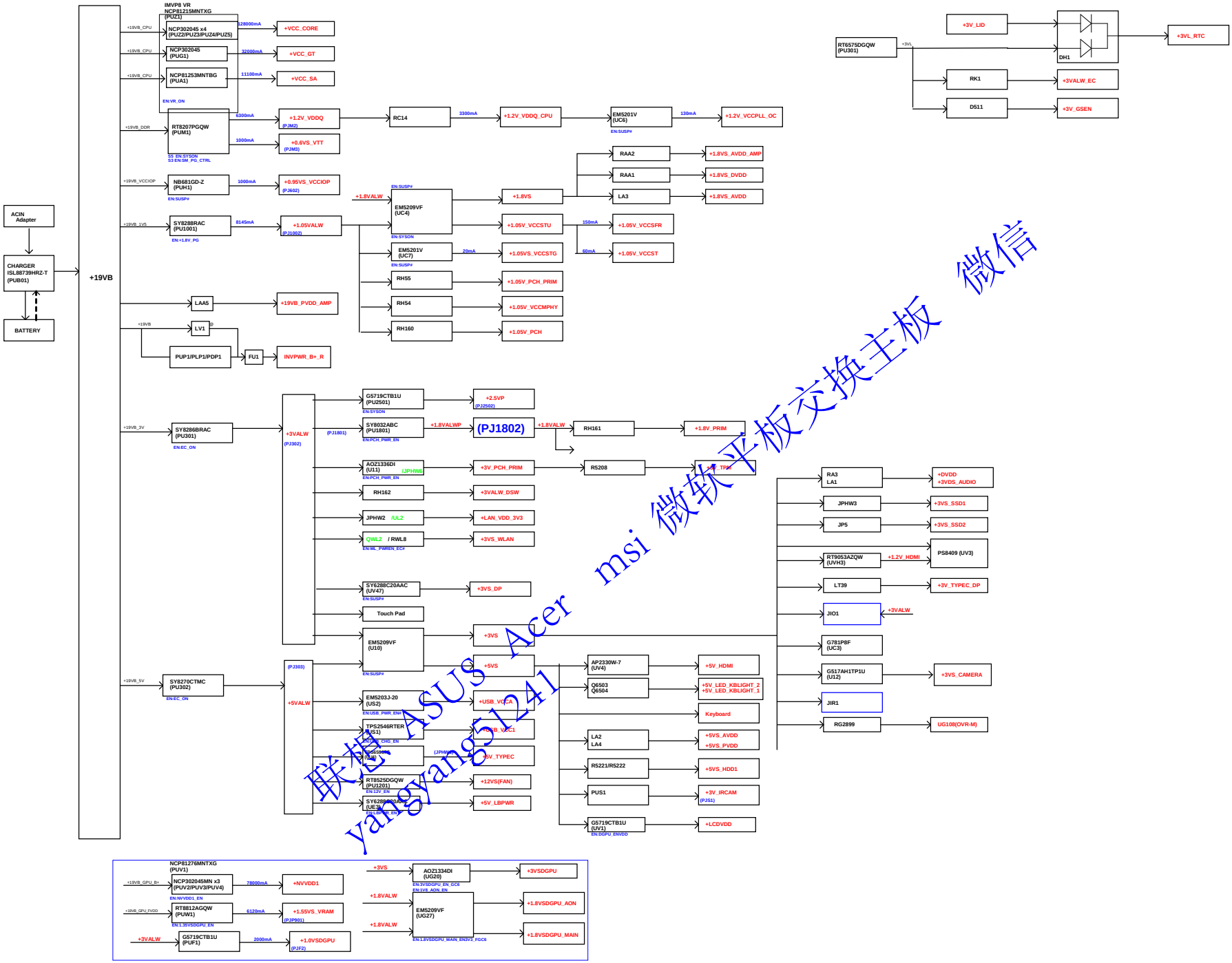
Title: Notes List

Size: Custom | Document Number: FPC72 LA-H492P | Rev: V0.1

Date: Friday, September 28, 2018 | Sheet 3 of 100



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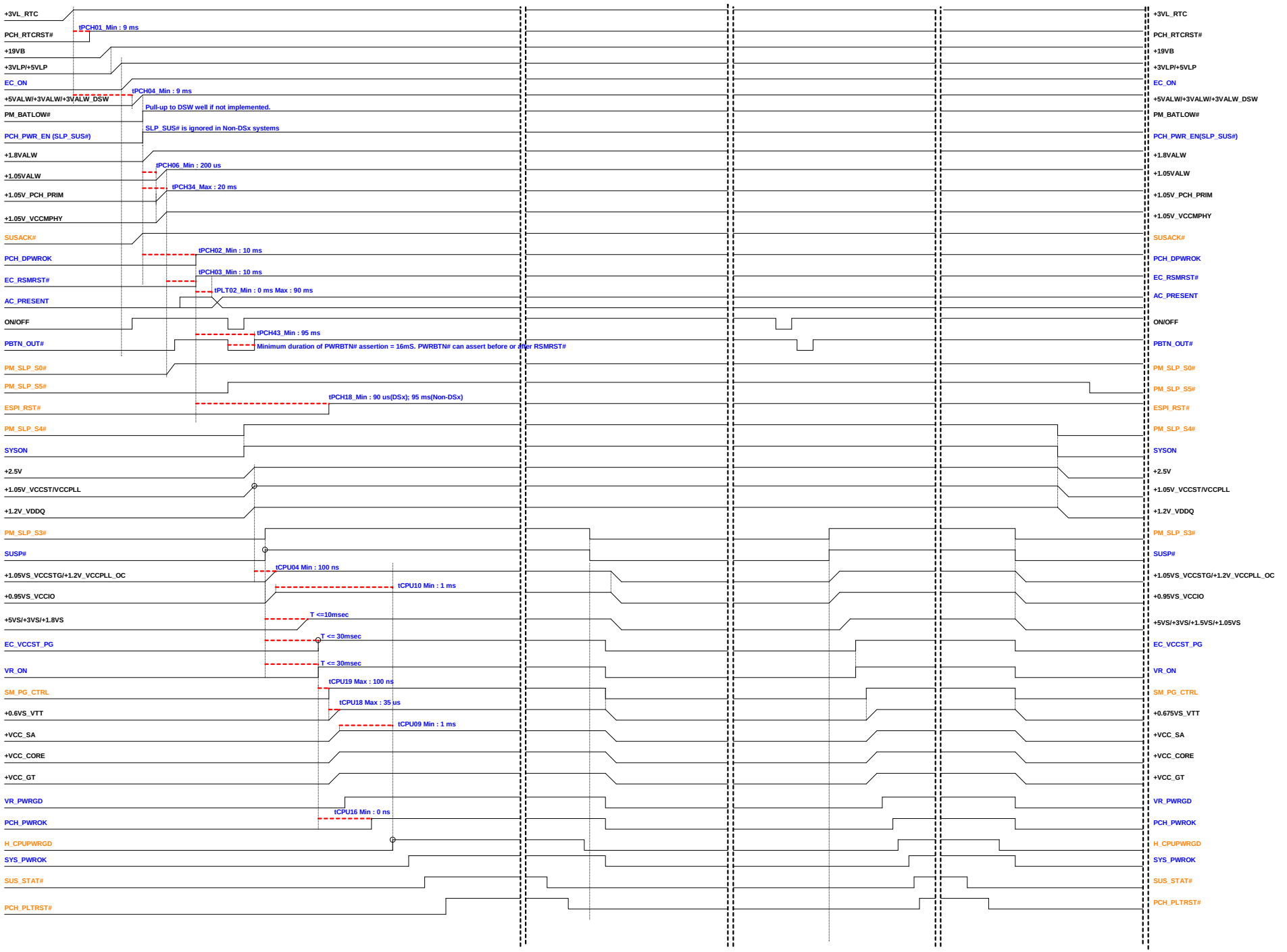
			Power Map
			Document Number: PPC54 LA-H482P
			Rev: 0.1
			Date: Friday, November 30, 2018 Sheet: 4 of 48

[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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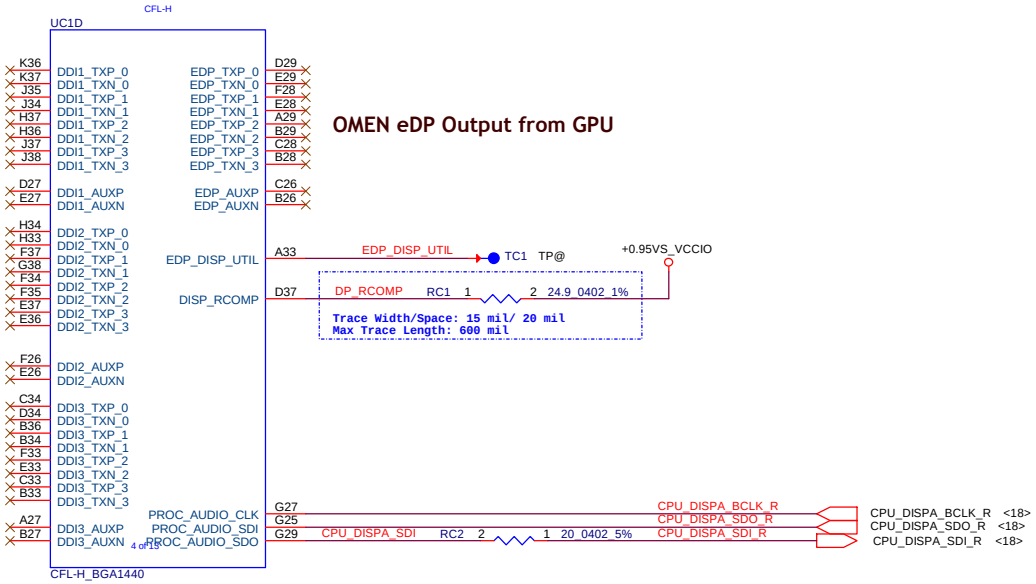
Title: Power Sequence

Size	Document Number	Rev
Custom	FPC54 LA-H482P	v0.1

Date: Friday, September 28, 2018 Sheet 5 of 100

OMEN: TR DDI input from GPU for DP v1.4

OMEN eDP Output from GPU



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Compal Electronics, Inc.

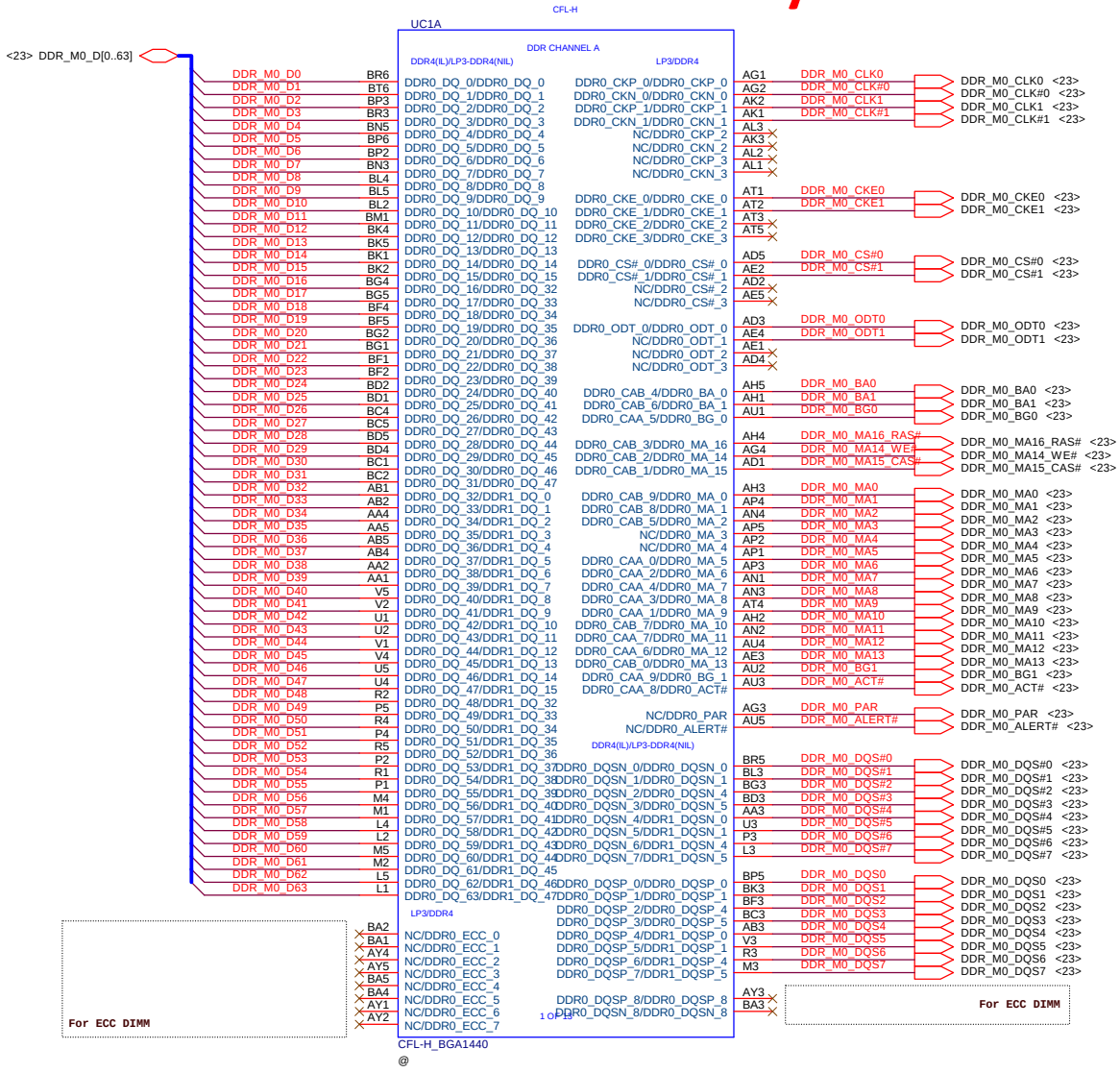
Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 6 of 100

CHANNEL - A

Interleaved Memory



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: CFL-H(2/8)DIMMA			
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 7 of 100		

CHANNEL - B

Interleaved Memory

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Title: CFL-H(3/8)DIMMB

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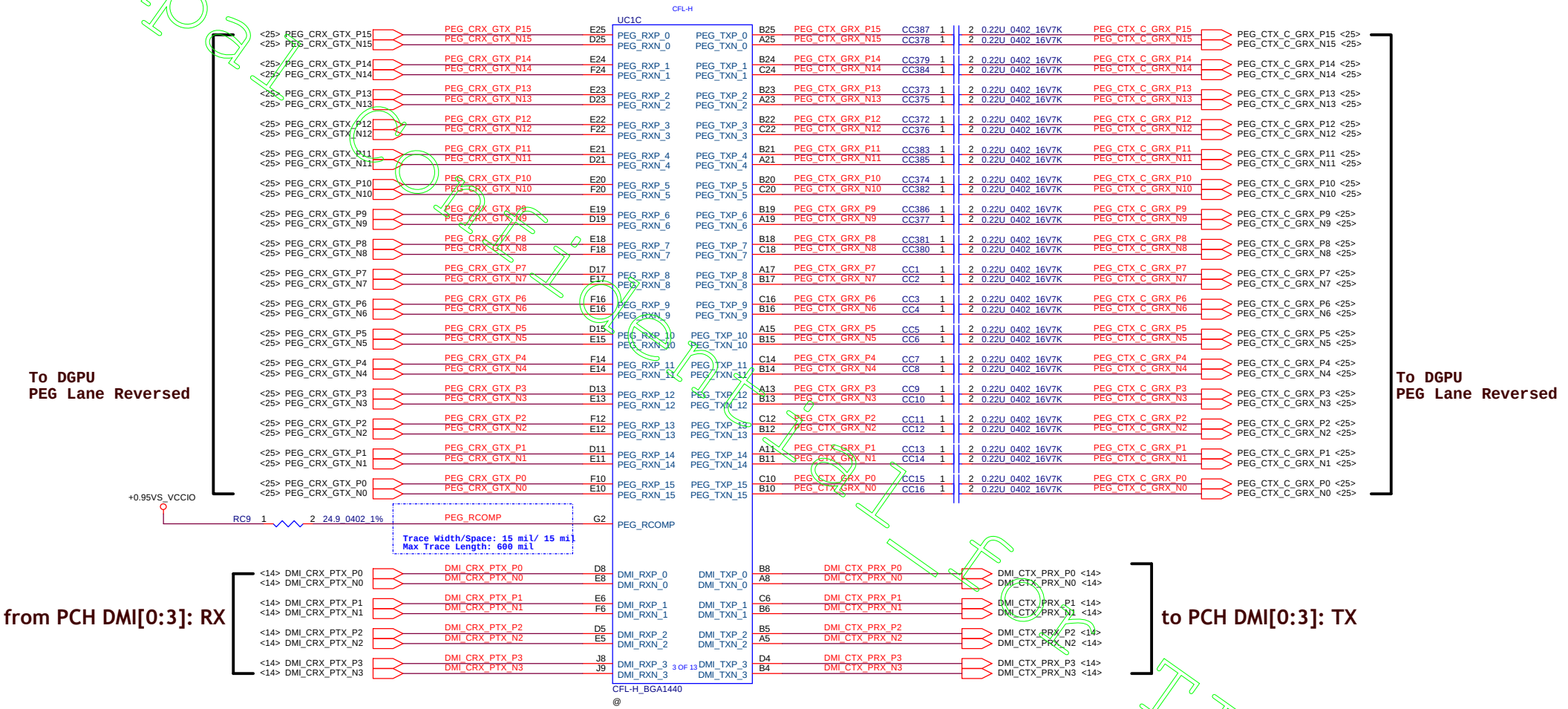
Date: Friday, September 28, 2018 | Sheet 8 of 100



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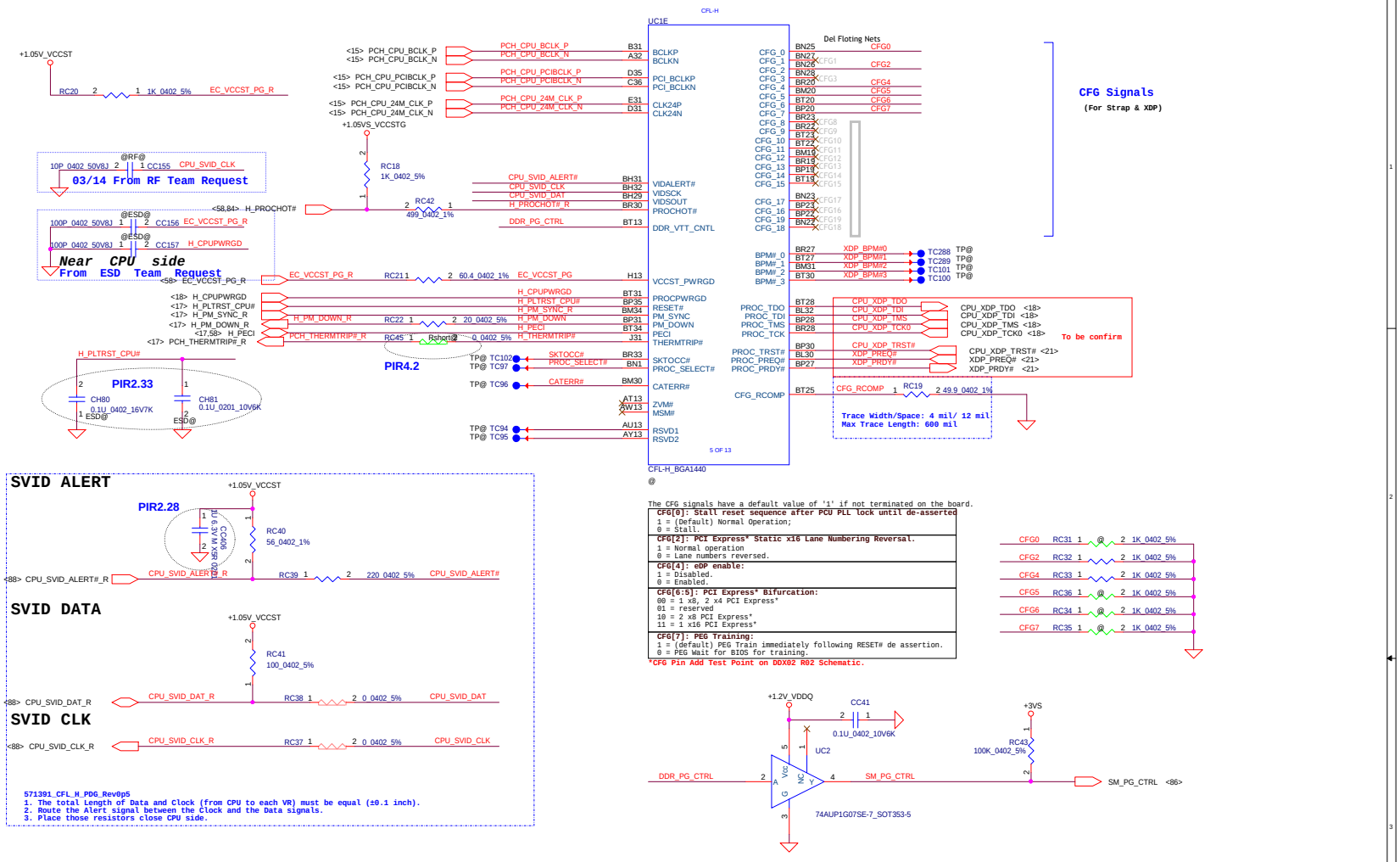
Date: Friday, September 28, 2018	Sheet 9 of 100		



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Title: CFL-H(5/8)CFG,SVID

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 10 of 100

GT
55000mA(Hexa Core GT2)

+VCC_GT

CFL-H

UC1K

AT14	VCCGT1	VCCGT80	BD35
AT31	VCCGT2	VCCGT81	BD36
AT32	VCCGT3	VCCGT82	BE31
AT33	VCCGT4	VCCGT83	BE32
AT34	VCCGT5	VCCGT84	BE33
AT35	VCCGT6	VCCGT85	BE34
AT36	VCCGT7	VCCGT86	BE35
AT37	VCCGT8	VCCGT87	BE36
AT38	VCCGT9	VCCGT88	BE37
AU14	VCCGT10	VCCGT89	BE38
AU29	VCCGT11	VCCGT90	BF13
AU30	VCCGT12	VCCGT91	BF14
AU31	VCCGT13	VCCGT92	BF29
AU32	VCCGT14	VCCGT93	BF30
AU35	VCCGT15	VCCGT94	BF31
AU36	VCCGT16	VCCGT95	BF32
AU37	VCCGT17	VCCGT96	BF35
AU38	VCCGT18	VCCGT97	BF36
AV29	VCCGT19	VCCGT98	BF37
AV30	VCCGT20	VCCGT99	BF38
AV31	VCCGT21	VCCGT100	BG29
AV32	VCCGT22	VCCGT101	BG30
AV33	VCCGT23	VCCGT102	BG31
AV34	VCCGT24	VCCGT103	BG32
AV35	VCCGT25	VCCGT104	BG33
AV36	VCCGT26	VCCGT105	BG34
AW14	VCCGT27	VCCGT106	BG35
AW31	VCCGT28	VCCGT107	BG36
AW32	VCCGT29	VCCGT108	BH33
AW33	VCCGT30	VCCGT109	BH34
AW34	VCCGT31	VCCGT110	BH35
AW35	VCCGT32	VCCGT111	BH36
AW36	VCCGT33	VCCGT112	BH37
AW37	VCCGT34	VCCGT113	BH38
AW38	VCCGT35	VCCGT114	BJ16
AY29	VCCGT36	VCCGT115	BJ17
AY30	VCCGT37	VCCGT116	BJ19
AY31	VCCGT38	VCCGT117	BJ20
AY32	VCCGT39	VCCGT118	BJ21
AY35	VCCGT40	VCCGT119	BJ23
AY36	VCCGT41	VCCGT120	BJ24
AY37	VCCGT42	VCCGT121	BJ26
AY38	VCCGT43	VCCGT122	BJ27
BA13	VCCGT44	VCCGT123	BJ37
BA14	VCCGT45	VCCGT124	BJ38
BA29	VCCGT46	VCCGT125	BK16
BA30	VCCGT47	VCCGT126	BK17
BA31	VCCGT48	VCCGT127	BK19
BA32	VCCGT49	VCCGT128	BK20
BA33	VCCGT50	VCCGT129	BK21
BA34	VCCGT51	VCCGT130	BK23
BA35	VCCGT52	VCCGT131	BK24
BA36	VCCGT53	VCCGT132	BK26
BB13	VCCGT54	VCCGT133	BK27
BB14	VCCGT55	VCCGT134	BL15
BB31	VCCGT56	VCCGT135	BL16
BB32	VCCGT57	VCCGT136	BL17
BB33	VCCGT58	VCCGT137	BL23
BB34	VCCGT59	VCCGT138	BL24
BB35	VCCGT60	VCCGT139	BL25
BB36	VCCGT61	VCCGT140	BL26
BB37	VCCGT62	VCCGT141	BL27
BB38	VCCGT63	VCCGT142	BL28
BC29	VCCGT64	VCCGT143	BL36
BC30	VCCGT65	VCCGT144	BL37
BC31	VCCGT66	VCCGT145	BM15
BC32	VCCGT67	VCCGT146	BM16
BC35	VCCGT68	VCCGT147	BM17
BC36	VCCGT69	VCCGT148	BM36
BC37	VCCGT70	VCCGT149	BM37
BC38	VCCGT71	VCCGT150	BN15
BD13	VCCGT72	VCCGT151	BN16
BD14	VCCGT73	VCCGT152	BN17
BD29	VCCGT74	VCCGT153	BN36
BD30	VCCGT75	VCCGT154	BN37
BD31	VCCGT76	VCCGT155	BN38
BD32	VCCGT77	VCCGT156	BP15
BD33	VCCGT78	VCCGT157	BP16
BD34	VCCGT79	VCCGT158	BP17
BP37	VCCGT159	VCCGT164	BR37
BP38	VCCGT160	VCCGT165	BT15
BR15	VCCGT161	VCCGT166	BT16
BR16	VCCGT162	VCCGT167	BT17
BR17	VCCGT163	VCCGT168	BT37

11 OF 13

VSSGT_SENSE
VCCGT_SENSE

AH37 VSSGT_SENSE
AH38 VCCGT_SENSE

CFL-H_BGA1440

@

+VCC_CORE

CFL-H

UC1I

AA13	VCC1	VCC64	AH13
AA31	VCC2	VCC65	AH14
AA32	VCC3	VCC66	AH29
AA33	VCC4	VCC67	AH30
AA34	VCC5	VCC68	AH31
AA35	VCC6	VCC69	AH32
AA36	VCC7	VCC70	AJ14
AA37	VCC8	VCC71	AJ29
AA38	VCC9	VCC72	AJ30
AB29	VCC10	VCC73	AJ31
AB30	VCC11	VCC74	AJ32
AB31	VCC12	VCC75	AJ33
AB32	VCC13	VCC76	AJ34
AB35	VCC14	VCC77	AJ35
AB36	VCC15	VCC78	AJ36
AB37	VCC16	VCC79	AK31
AB38	VCC17	VCC80	AK32
AC13	VCC18	VCC81	AK33
AC14	VCC19	VCC82	AK34
AC29	VCC20	VCC83	AK35
AC30	VCC21	VCC84	AK36
AC31	VCC22	VCC85	AK37
AC32	VCC23	VCC86	AK38
AC33	VCC24	VCC87	AL13
AC34	VCC25	VCC88	AL29
AC35	VCC26	VCC89	AL30
AC36	VCC27	VCC90	AL31
AD13	VCC28	VCC91	AL32
AD14	VCC29	VCC92	AL35
AD31	VCC30	VCC93	AL36
AD32	VCC31	VCC94	AL37
AD33	VCC32	VCC95	AL38
AD34	VCC33	VCC96	AM13
AD35	VCC34	VCC97	AM14
AD36	VCC35	VCC98	AM29
AD37	VCC36	VCC99	AM30
AD38	VCC37	VCC100	AM31
AE13	VCC38	VCC101	AM32
AE14	VCC39	VCC102	AM33
AE30	VCC40	VCC103	AM34
AE31	VCC41	VCC104	AM35
AE32	VCC42	VCC105	AM36
AE35	VCC43	VCC106	AN13
AE36	VCC44	VCC107	AN14
AE37	VCC45	VCC108	AN31
AE38	VCC46	VCC109	AN32
AF29	VCC47	VCC110	AN33
AF30	VCC48	VCC111	AN34
AF31	VCC49	VCC112	AN35
AF32	VCC50	VCC113	AN36
AF33	VCC51	VCC114	AN37
AF34	VCC52	VCC115	AN38
AF35	VCC53	VCC116	AP13
AF36	VCC54	VCC117	AP30
AF37	VCC55	VCC118	AP31
AF38	VCC56	VCC119	AP32
AG14	VCC57	VCC120	AP35
AG31	VCC58	VCC121	AP36
AG32	VCC59	VCC122	AP37
AG33	VCC60	VCC123	AP38
AG34	VCC61	VCC124	K13
AG35	VCC62		
AG36	VCC63		

9 OF 13

VCC_SENSE
VSS_SENSE

AG37 VCCSENSE
AG38 VSSSENSE

CFL-H_BGA1440

@

96000mA(Hexa Core GT2)

+VCC_CORE

RC10
100_0402_1%

VCCSENSE <88>
VSSSENSE <88>

RC11
100_0402_1%

1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU

+VCC_GT

RC12
100_0402_1%

VCCGT_SENSE
VSSGT_SENSE

VCCGT_SENSE <88>
VSSGT_SENSE <88>

RC13
100_0402_1%

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

+VCC_CORE

CFL-H

UC1J

K14	VCC1	VCC64	W35
L13	VCC2	VCC65	W36
L14	VCC3	VCC66	W37
N13	VCC4	VCC67	W38
N14	VCC5	VCC68	Y29
N30	VCC6	VCC69	Y30
N31	VCC7	VCC70	Y31
N32	VCC8	VCC71	Y32
N35	VCC9	VCC72	Y33
N36	VCC10	VCC73	Y34
N37	VCC11	VCC74	Y35
N38	VCC12	VCC75	Y36
P13	VCC13		
P14	VCC14		
P29	VCC15		
P30	VCC16		
P31	VCC17		
P32	VCC18		
P33	VCC19		
P34	VCC20		
P35	VCC21		
P36	VCC22		
R13	VCC23		
R31	VCC24		
R32	VCC25		
R33	VCC26		
R34	VCC27		
R35	VCC28		
R36	VCC29		
R37	VCC30		
R38	VCC31		
T29	VCC32		
T30	VCC33		
T31	VCC34		
T32	VCC35		
T35	VCC36		
T36	VCC37		
T37	VCC38		
T38	VCC39		
U29	VCC40		
U30	VCC41		
U31	VCC42		
U32	VCC43		
U33	VCC44		
U34	VCC45		
U35	VCC46		
U36	VCC47		
V13	VCC48		
V14	VCC49		
V31	VCC50		
V32	VCC51		
V33	VCC52		
V34	VCC53		
V35	VCC54		
V36	VCC55		
V37	VCC56		
V38	VCC57		
W13	VCC58		
W14	VCC59		
W29	VCC60		
W30	VCC61		
W31	VCC62		
W32	VCC63		

10 OF 13

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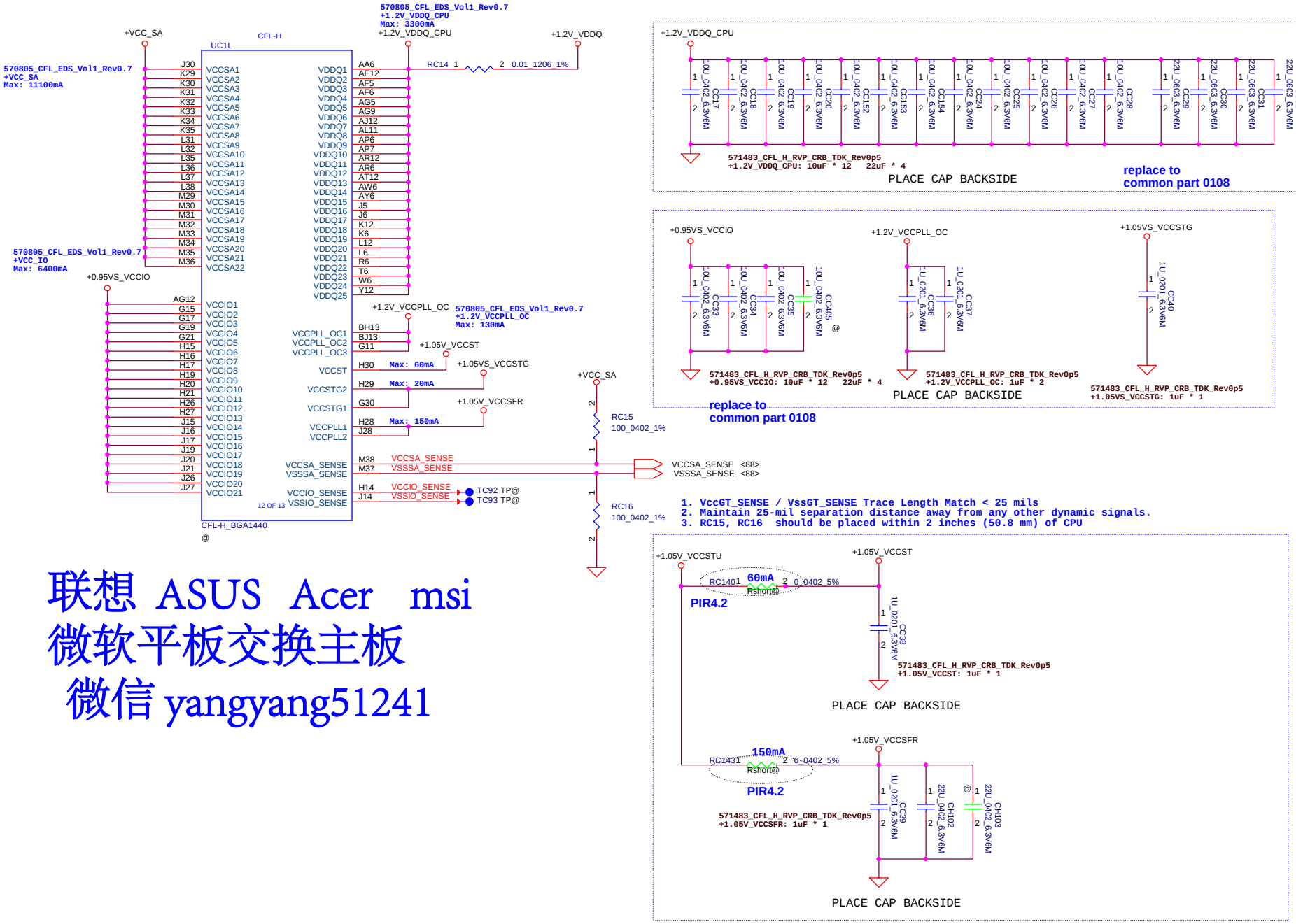

联想 ASUS Acer msi
微软平板交换主板
微信 yangyang51241

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Size	Document Number	Rev
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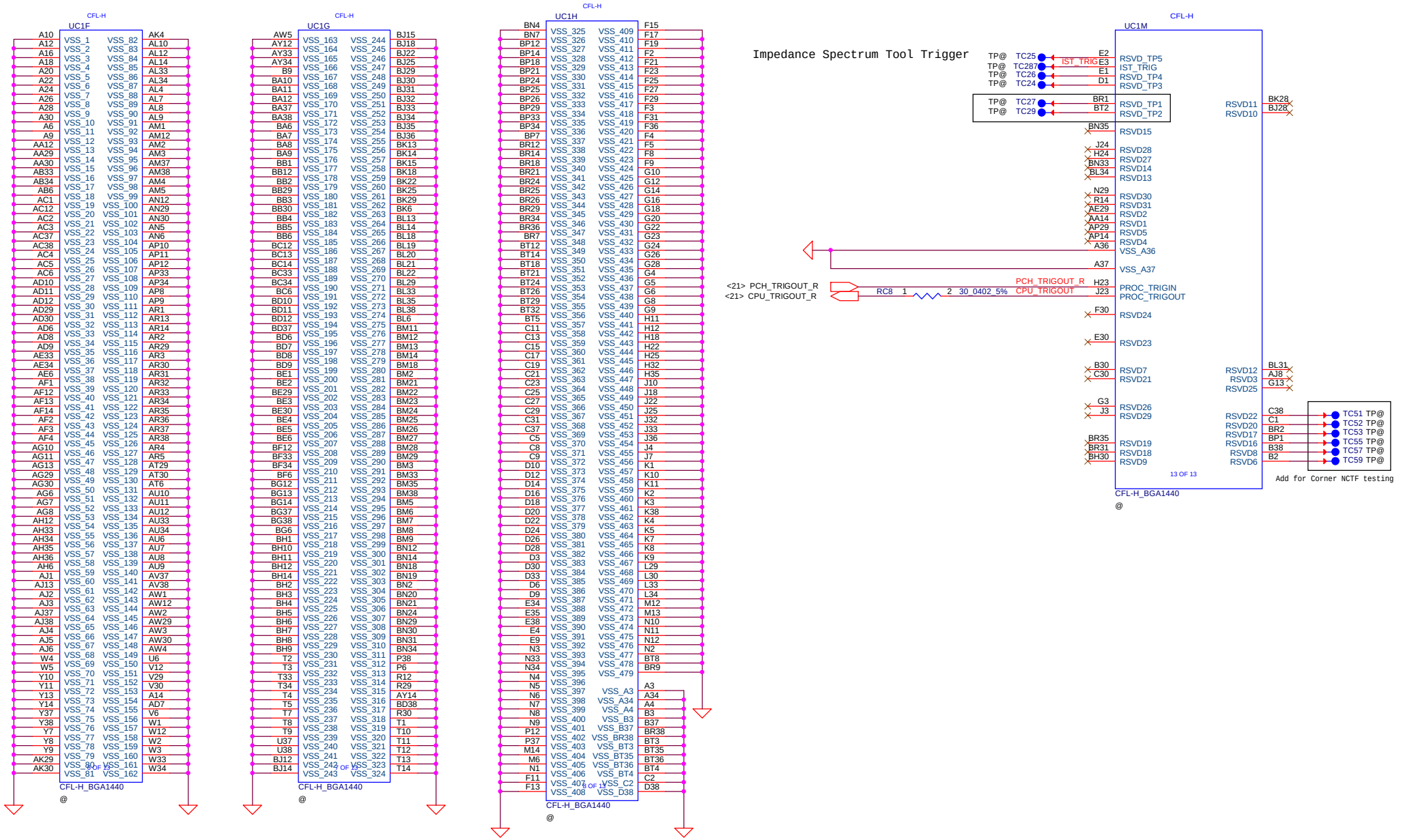

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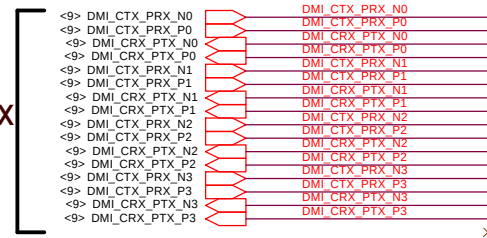
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 13 of 100		

from/to CPU DMI[0:3]:RX/TX



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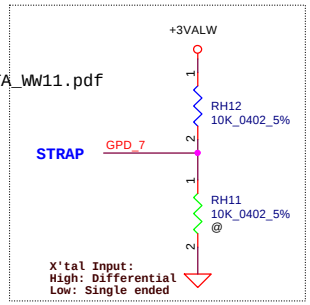


PIR3.3

SSD #2[0:3]

Flex I/O Lane	HM370
0	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2
4	USB3.1 Gen1
5	USB3.1 Gen1
6	USB3.1 Gen1
7	USB3.1 Gen1
8	N/A
9	N/A
10	GbE
11	N/A
12	N/A
13	N/A
14	PCIe*, GbE
15	PCIe*
16	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B
20	PCIe*
21	PCIe*

PCIE Port 5

22	PCIe*, SATA 4
23	PCIe*, SATA 5
24	PCIe*
25	PCIe*
26	PCIe*
27	PCIe*
28	PCIe*
29	PCIe*

571182-CNL-PCH-H-EDS-Rev2p2 P.198

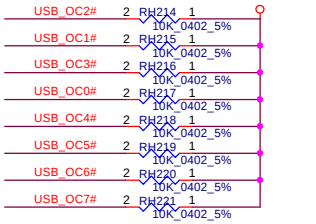
Figure 26-1. Supported PCI Express* Link Configurations

PCH-H Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 (Cycle Router #1)				PCIe* Controller #4				PCIe* Controller #5 (Cycle Router #3)				PCIe* Controller #6 (Cycle Router #2)			
Flex I/O Lane #		6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HM370 HM375	1x4									RP 9 SSD#1				RP 13				SSD#2 RP 17				TR RP 21			
	1x4 LR									RP 9				RP 13				RP 17				RP 21			
	2x2									RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1									RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2									RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1									RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
QM370 QM375	1x4					RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR					RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2					RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1					RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2					RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1					RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
CM246 CM248	1x4	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
—A maximum of 16 PCIe* Ports (or devices) can be enabled
- When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
— PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
— A maximum of 6 SATA Ports (or devices) can be enabled
— SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
— SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
— A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
— A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
— x2 and x4 PCIe* NVMe SSD
— x2 IntelR Optane? Memory Device
— See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations
— SATA lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6 SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe or SATA, must be statically assigned to SATA or PCIe via the SATA/PCIe Combo Port Soft Straps described in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

+3V_PCH_PRIM



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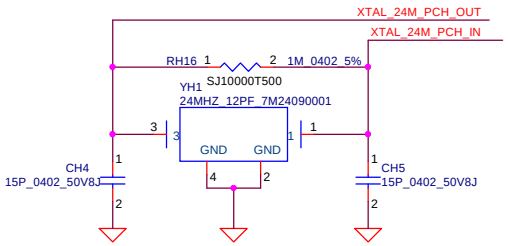
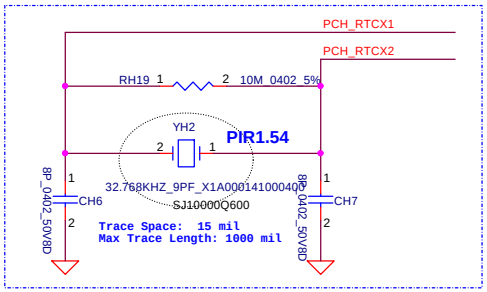
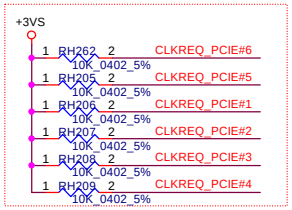
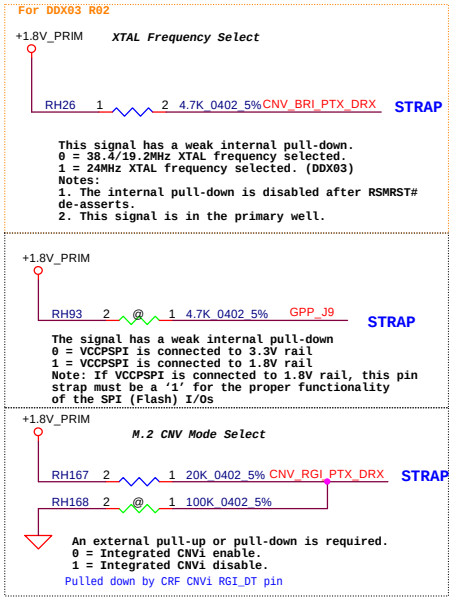
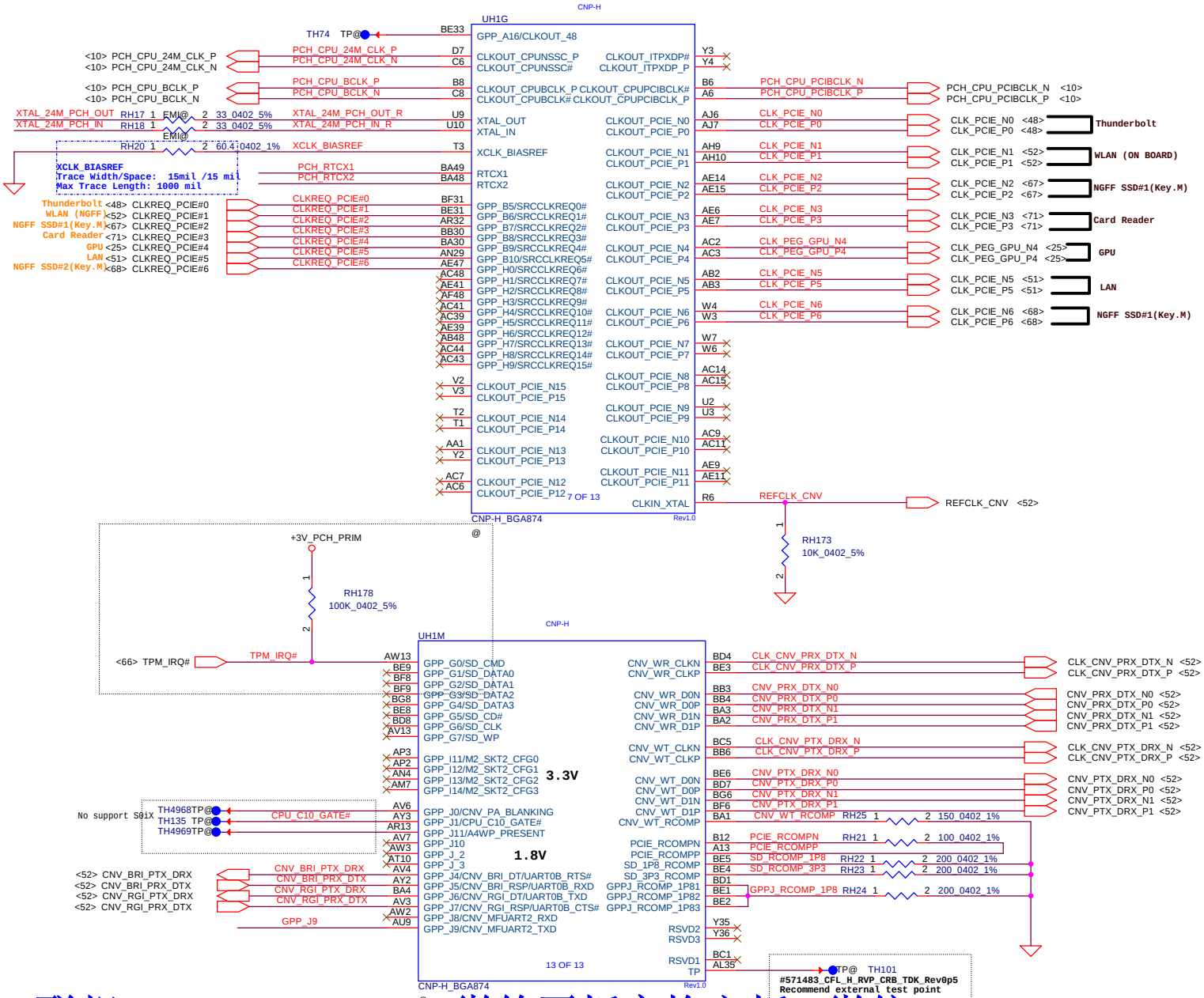
PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf











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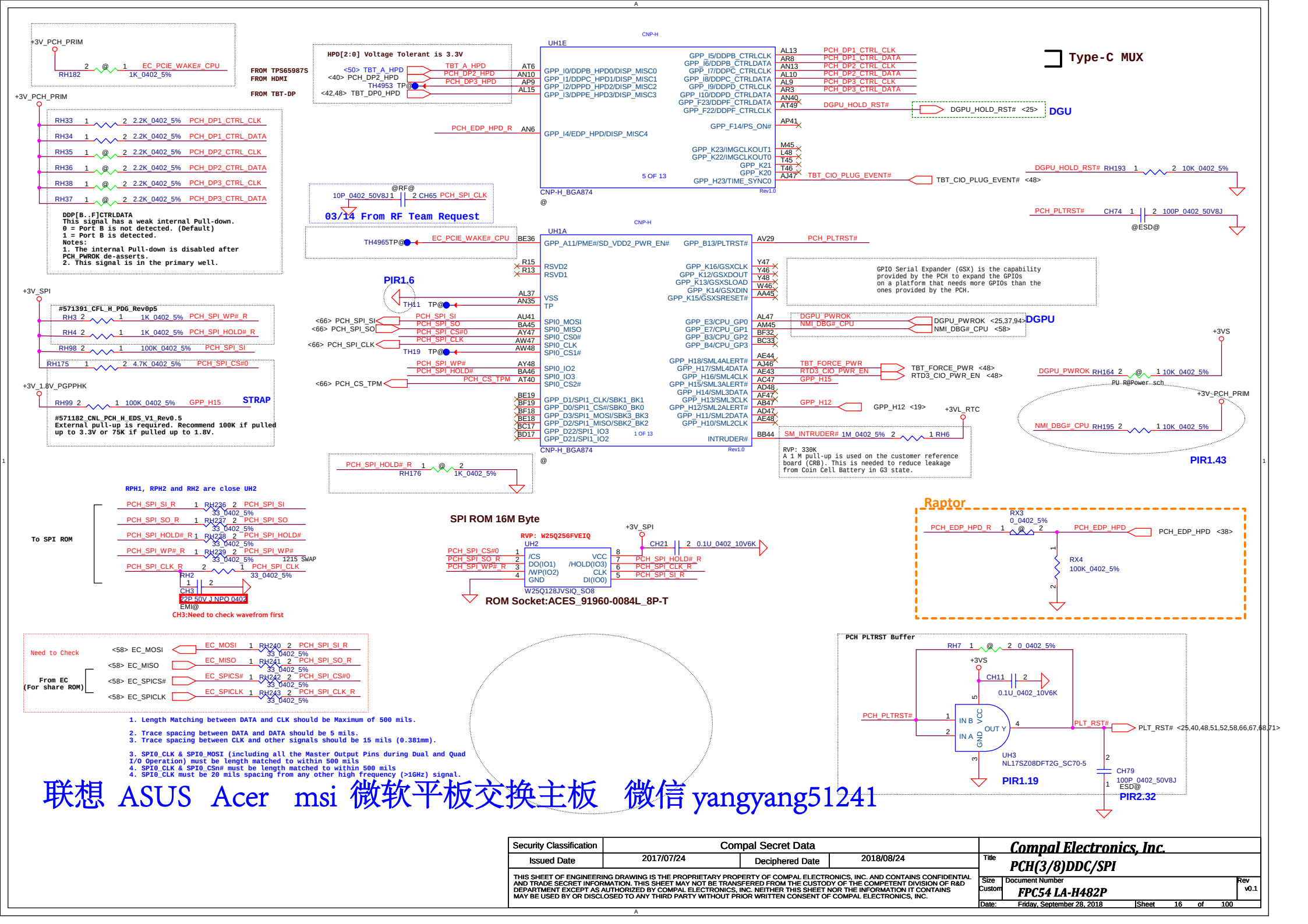

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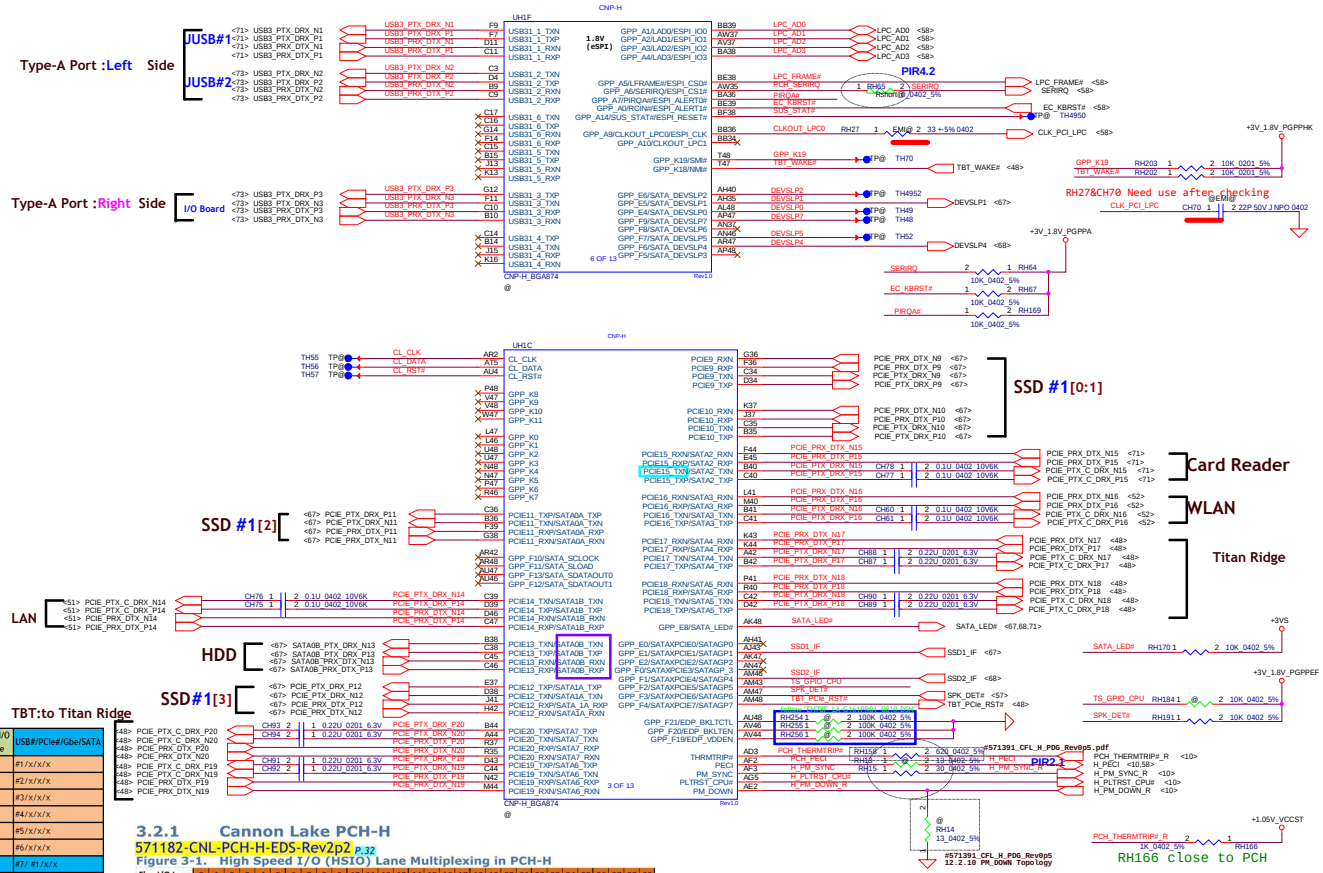
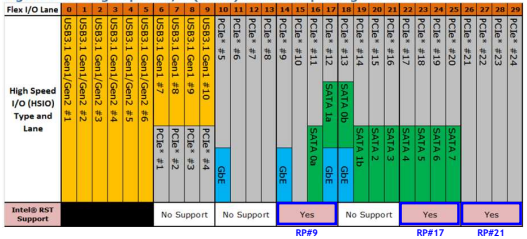


RST	Flex I/O Lane	USB#/PCIe#/Gbe/SATA	
	0	#1/x/x/x	
	1	#2/x/x/x	
	2	#3/x/x/x	
	3	#4/x/x/x	
	4	#5/x/x/x	
	5	#6/x/x/x	
x	6	#7/ #1/x/x	
	7	#8/ #2/x/x	
x	8	#9/ #3/x/x	
	9	#10/ #4/x/x	
	10	x/#5/Gbe/x	
x	11	x/#6/x/x	
	12	x/#7/x/x	
	13	x/#8/x/x	
Yes	14	x/#9/Gbe/x	
	15	x/#10/x/x	SSD#1
	16	x/#11/x/#0a	
	17	x/#12/Gbe/#1a	
x	18	x/#13/Gbe/#0b	HDD
	19	x/#14/x/#1b	LAN
	20	x/#15/x/#2	CR
	21	x/#16/x/#3	WLAN
Yes	22	x/#17/x/#4	
	23	x/#18/x/#5	SSD#2
	24	x/#19/x/#6	
Yes	25	x/#20/x/#7	
	26	x/#21/x/x	
	27	x/#22/x/x	Titan Ridge
	28	x/#23/x/x	
	29	x/#24/x/x	

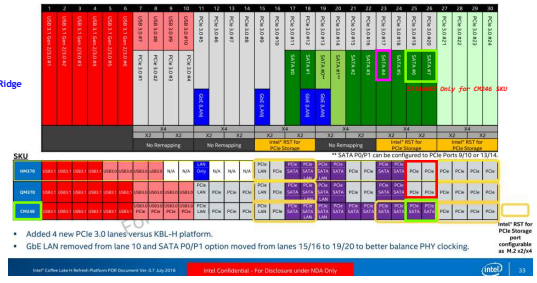
3.2.1 Cannon Lake PCH-H

571182-CNL-PCH-H-EDS-Rev2p2 P.32

Figure 3-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H



HSIO Lane Assignments – Cannon Lake PCH-H



- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA P0/P1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

571182-CNL-PCH-H-EDS-Rev2p2 P.198

Figure 26-1. Supported PCI Express* Link Configurations

PCH-H Details	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3 (Cycle Router #1)	PCIe* Controller #4 (Cycle Router #1)	PCIe* Controller #5 (Cycle Router #3)	PCIe* Controller #6 (Cycle Router #2)
Flex I/O Lane #	6 7 8 9	10 11 12 13	14 15 16 17	18 19 20 21	22 23 24 25	26 27 28 29
PCIe* Lane #	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24
HM370 / HM375	1x4		RP 9	RP 13	RP 17	RP 21
	1x4 LR		RP 9	RP 13	RP 17	RP 21
	2x2		RP 9 RP 11	RP 13 RP 15	RP 17 RP 19	RP 21 RP 23
	1x2+2x1		RP 9 RP 11 RP 12	RP 13 RP 15 RP 16	RP 17 RP 19 RP 20	RP 21 RP 23 RP 24
	2x1+1x2		RP 12 RP 11 RP 9	RP 16 RP 15 RP 13	RP 20 RP 19 RP 17	RP 24 RP 23 RP 21
	4x1		RP 3 RP 10 RP 11 RP 12	RP 13 RP 14 RP 15 RP 16	RP 17 RP 18 RP 19 RP 20	RP 21 RP 22 RP 23 RP 24
QM370 / QM375	1x4	RP 5	RP 9	RP 13	RP 17	RP 21
	1x4 LR	RP 5	RP 9	RP 13	RP 17	RP 21
	2x2	RP 5 RP 7	RP 9 RP 11	RP 13 RP 15	RP 17 RP 19	RP 21 RP 23
	1x2+2x1	RP 5 RP 7 RP 8	RP 9 RP 11 RP 12	RP 13 RP 15 RP 16	RP 17 RP 19 RP 20	RP 21 RP 23 RP 24
	2x1+1x2	RP 8 RP 7 RP 5	RP 12 RP 11 RP 9	RP 16 RP 15 RP 13	RP 20 RP 19 RP 17	RP 24 RP 23 RP 21
	4x1	RP 5 RP 6 RP 7 RP 8	RP 3 RP 10 RP 11 RP 12	RP 13 RP 14 RP 15 RP 16	RP 17 RP 18 RP 19 RP 20	RP 21 RP 22 RP 23 RP 24
CM246 / CM248	1x4	RP 1 RP 5	RP 3	RP 13	RP 17	RP 21
	1x4 LR	RP 1 RP 5	RP 9	RP 13	RP 17	RP 21
	2x2	RP 1 RP 3 RP 5 RP 7	RP 9 RP 11	RP 13 RP 15	RP 17 RP 19	RP 21 RP 23
	1x2+2x1	RP 1 RP 3 RP 4 RP 5 RP 7 RP 8	RP 9 RP 11 RP 12	RP 13 RP 15 RP 16	RP 17 RP 19 RP 20	RP 21 RP 23 RP 24
	2x1+1x2	RP 4 RP 3 RP 1 RP 8 RP 7 RP 5	RP 12 RP 11 RP 9	RP 16 RP 15 RP 13	RP 20 RP 19 RP 17	RP 24 RP 23 RP 21
	4x1	RP 1 RP 2 RP 3 RP 4 RP 5 RP 6 RP 7 RP 8	RP 3 RP 10 RP 11 RP 12	RP 13 RP 14 RP 15 RP 16	RP 17 RP 18 RP 19 RP 20	RP 21 RP 22 RP 23 RP 24

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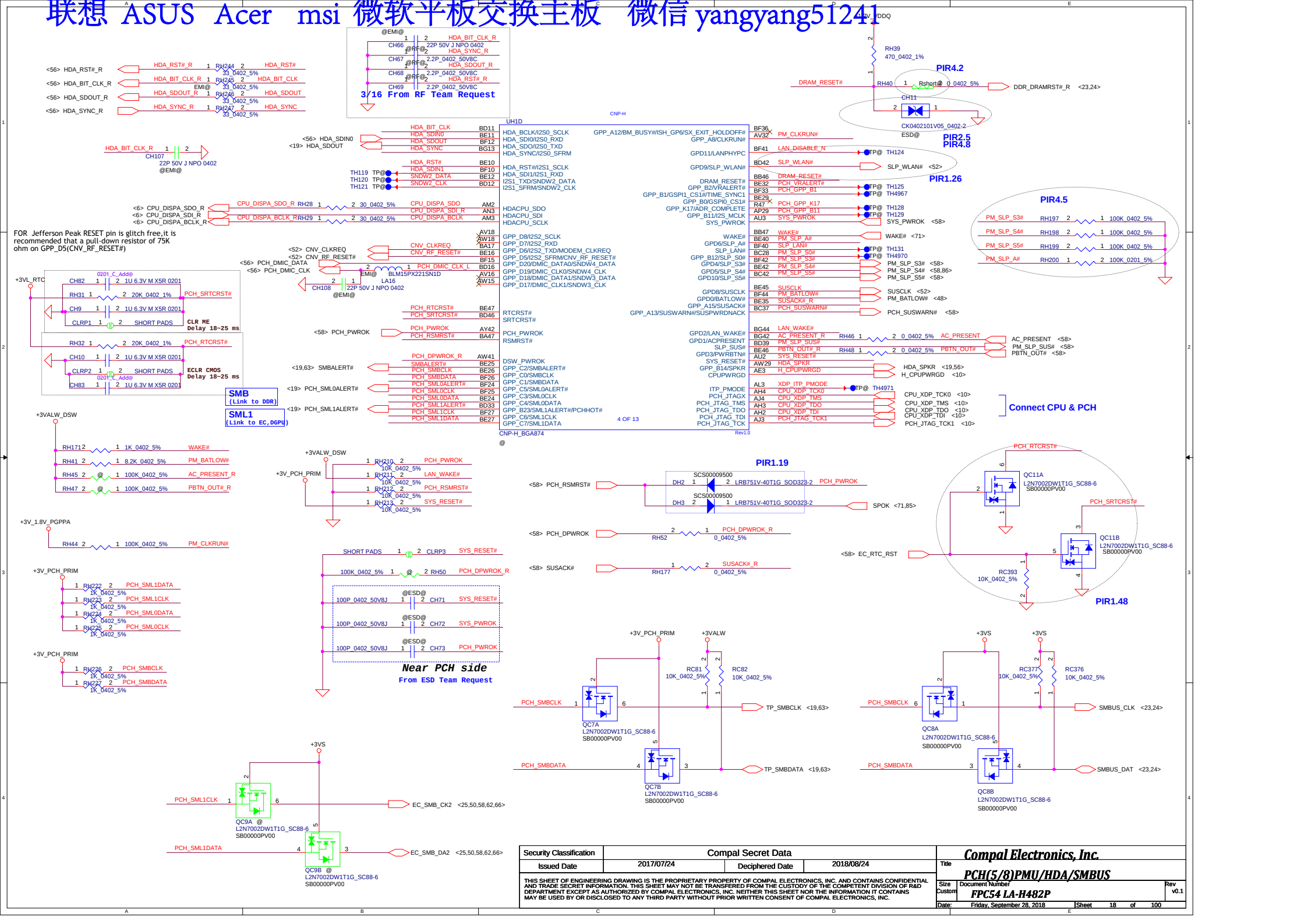
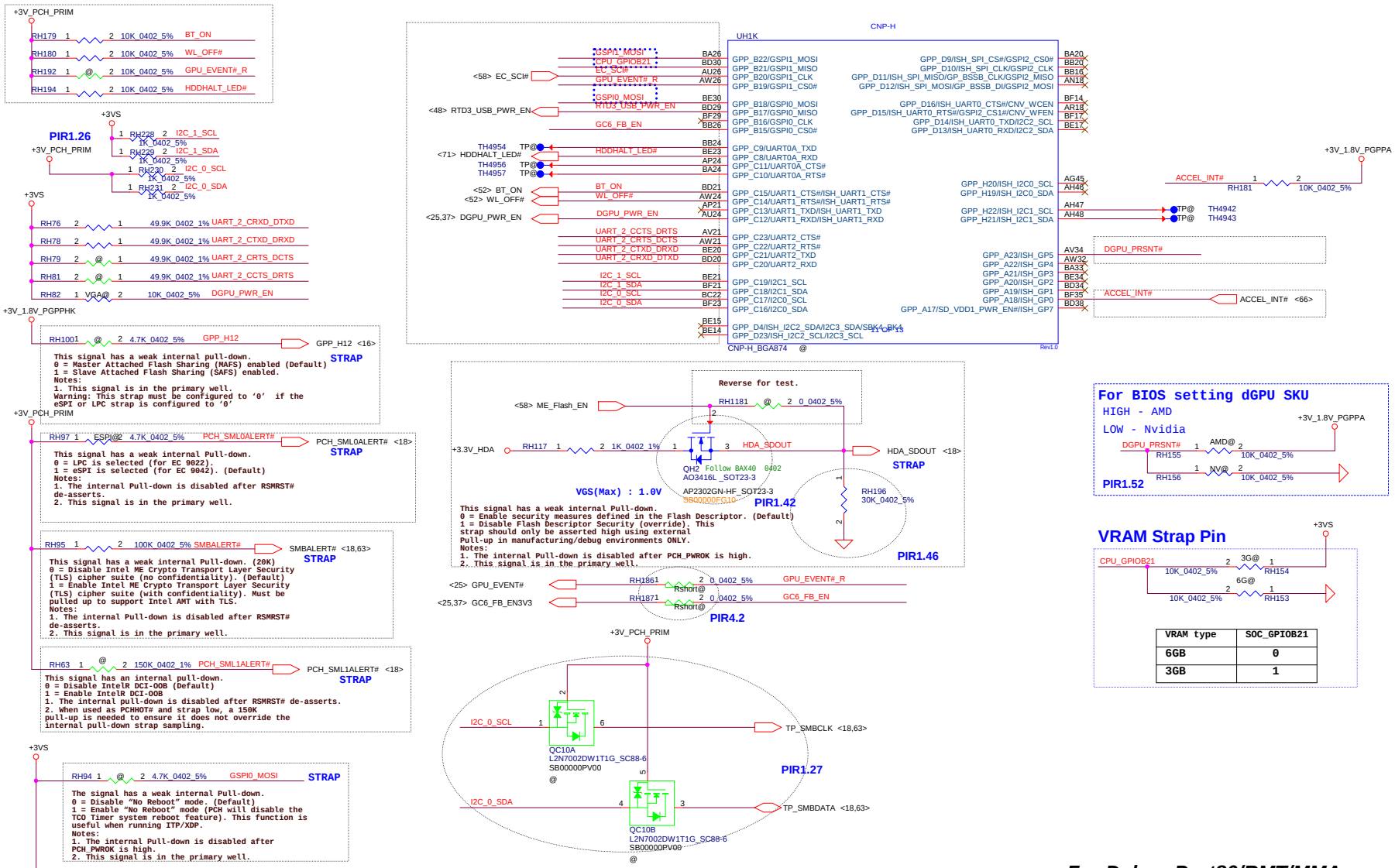
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
Date: Friday, September 28, 2018	Sheet 17 of 100	



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS		
Size	Document Number		Rev
Custom	FPC54 LA-H482P		v0.1
Date:	Friday, September 28, 2018	Sheet	18 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	FPC54 LA-H482P	V0.1

Date: Friday, September 28, 2018 Sheet 19 of 100

GPIO Group	Voltage
GPPA	LPC: 3.3V eSPI: 1.8V *
GPPB GPPC	3.3V
GPPD	1.8V for SOC_DMIC 3.3V for IR_DMIC *
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

PLACE 3-5MM FROM PACKAGE EDGE

VCCPHVLDO_1P8 (External VRM mode RH172 unmount)

For DDX03 R02

RH174 for 571391_CFL_H_PDG_Rev0p71.pdf

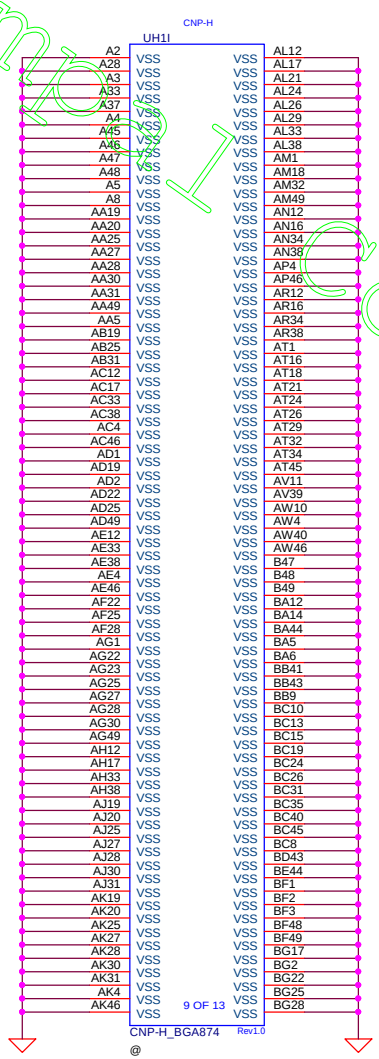
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

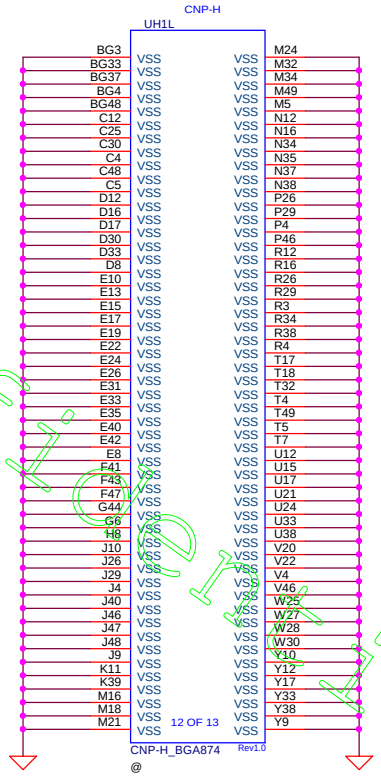
Compal Electronics, Inc.

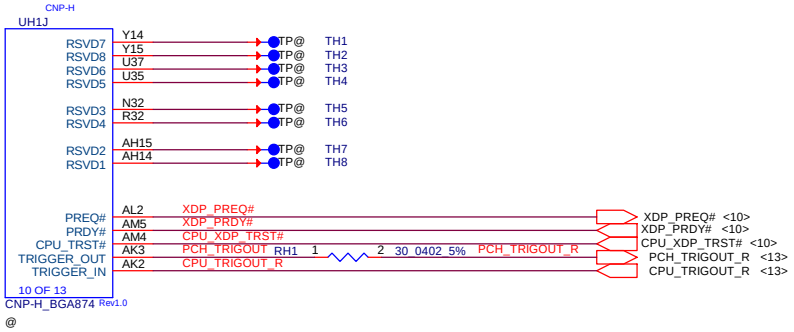
Title: PCH(7/8)Power

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 20 of 100

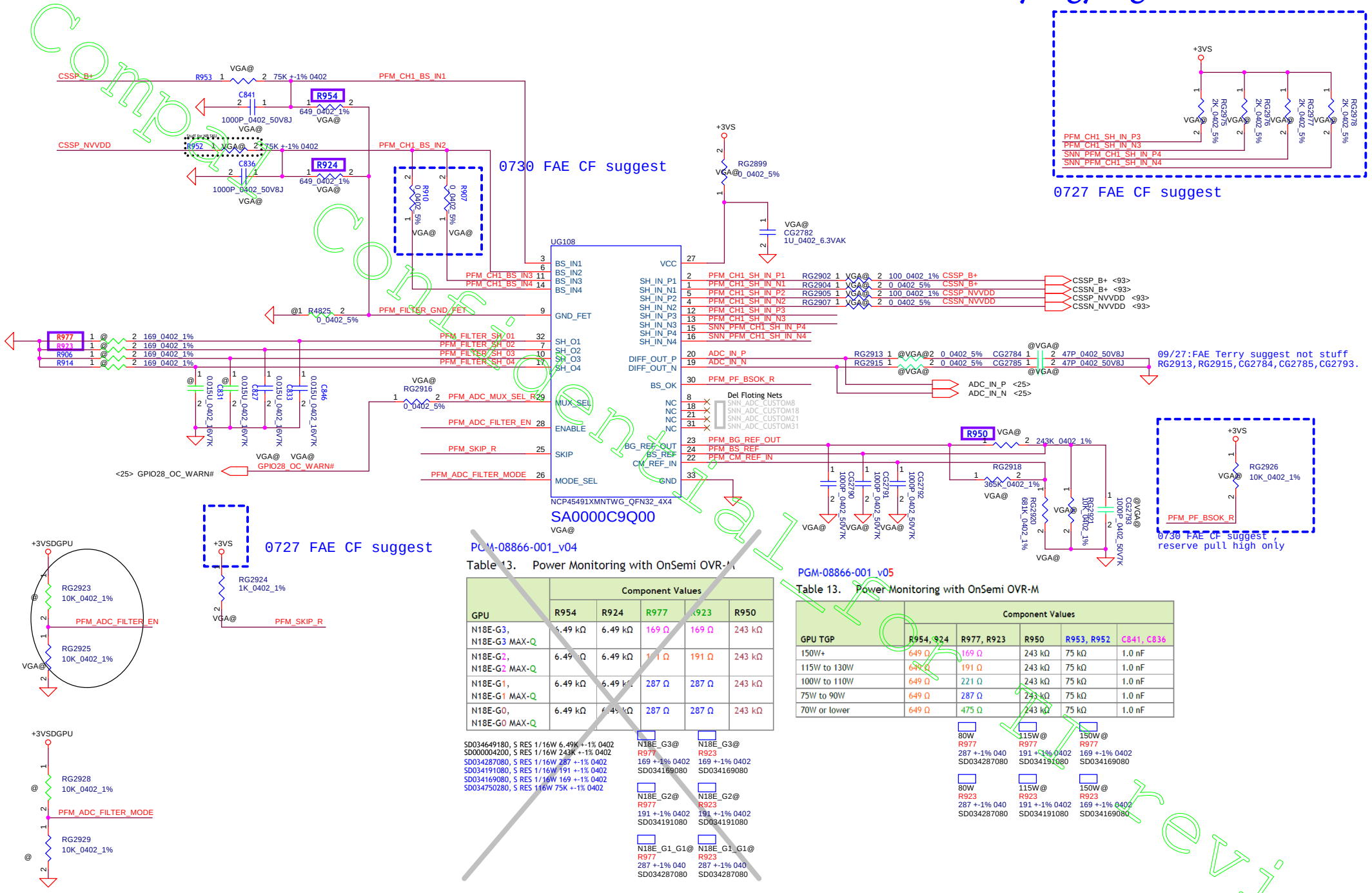






Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title	PCH(8/8)GND/RSVD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 21 of 100		



Security Classification	Compal Secret Data			
Issued Date	2017/11/23	Deciphered Date	2018/09/01	

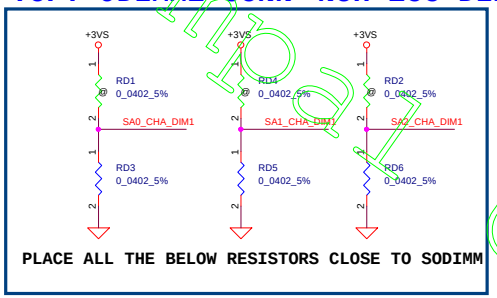
Compal Electronics, Inc.			
Title: OVR-M			
Size: Custom	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Friday, September 28, 2018	Sheet 22 of 100		

CHANNEL-A

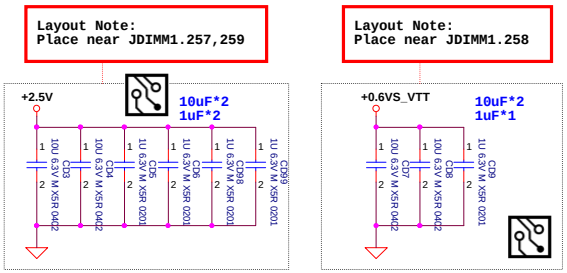
REVERSE TYPE

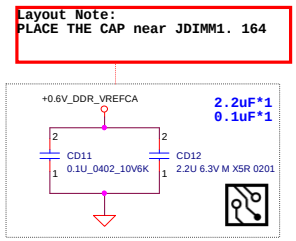
Interleaved Memory

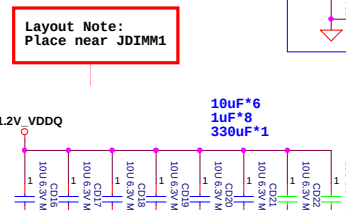
TOP: JDIMM1 CONN Non-ECC DIMM

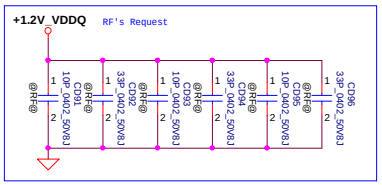


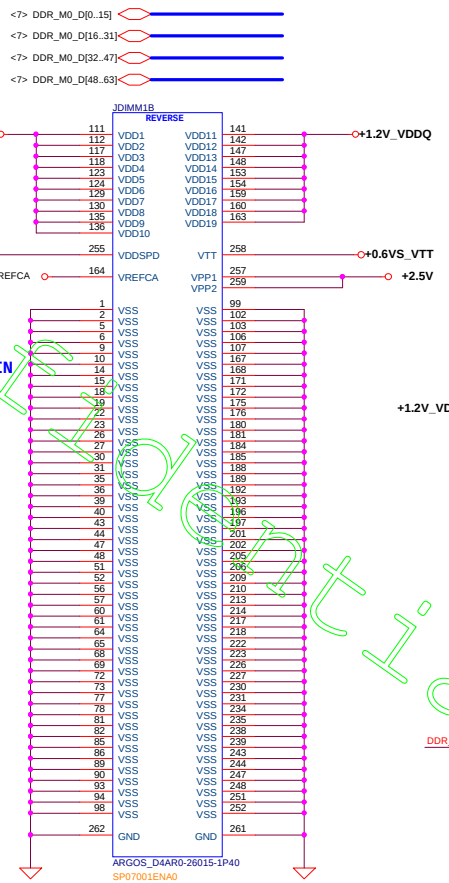
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

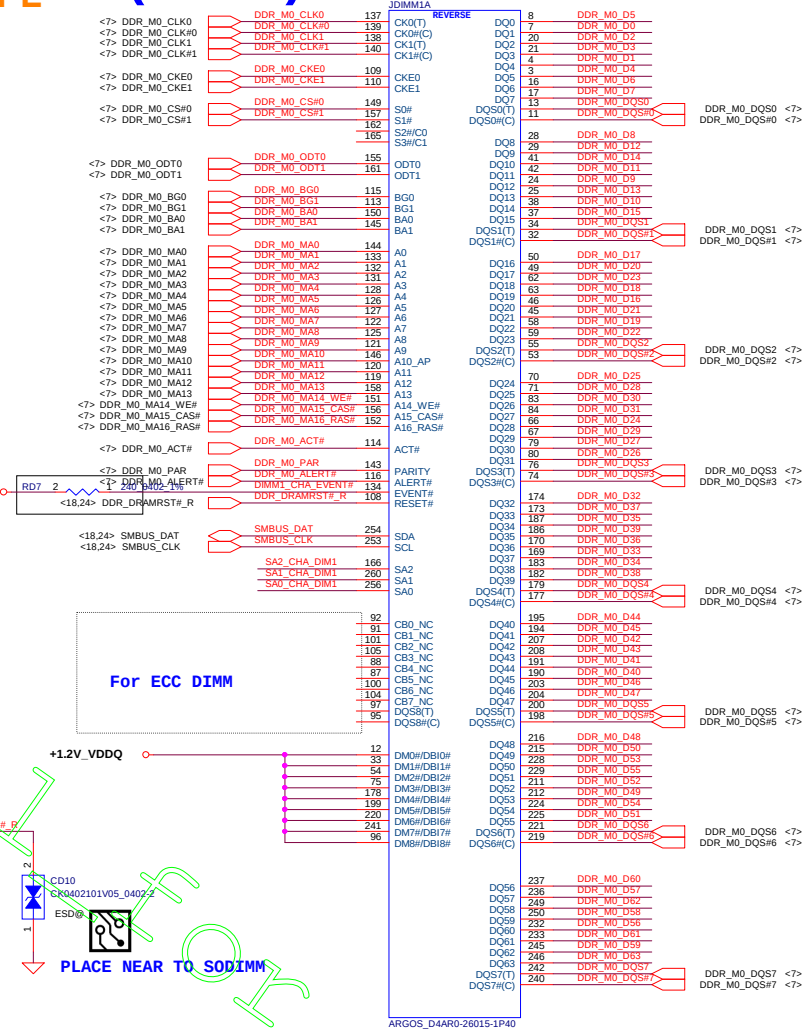


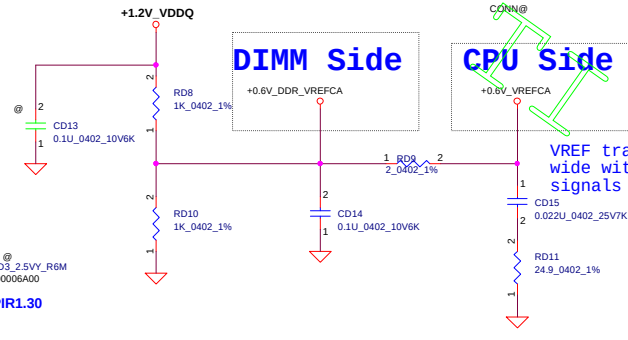


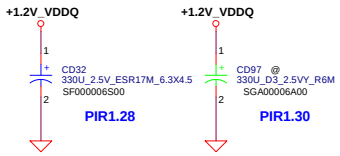












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Issued Date	2017/07/24	Deciphered Date	2018/08/24

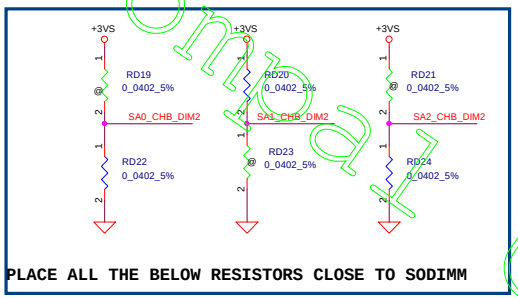
Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Size	Document Number: FPC54 LA-H482P
Rev	v0.1
Date: Friday, September 28, 2018	Sheet 23 of 100

CHANNEL-B

TOP: JDIMM2 CONN Non-ECC DIMM

17.3"=>Reverse TYPE (8 mm)

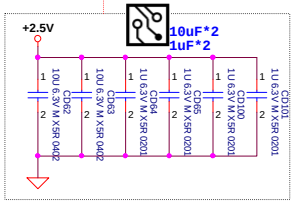
Interleaved Memory



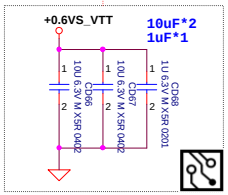
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

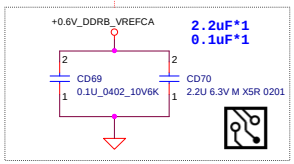
Layout Note:
Place near JDIMM2.257,259



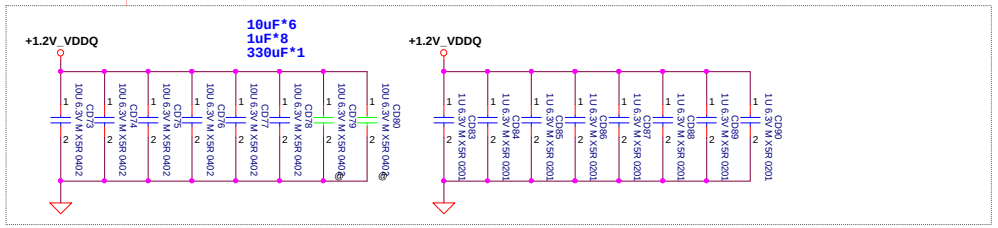
Layout Note:
Place near JDIMM2.258

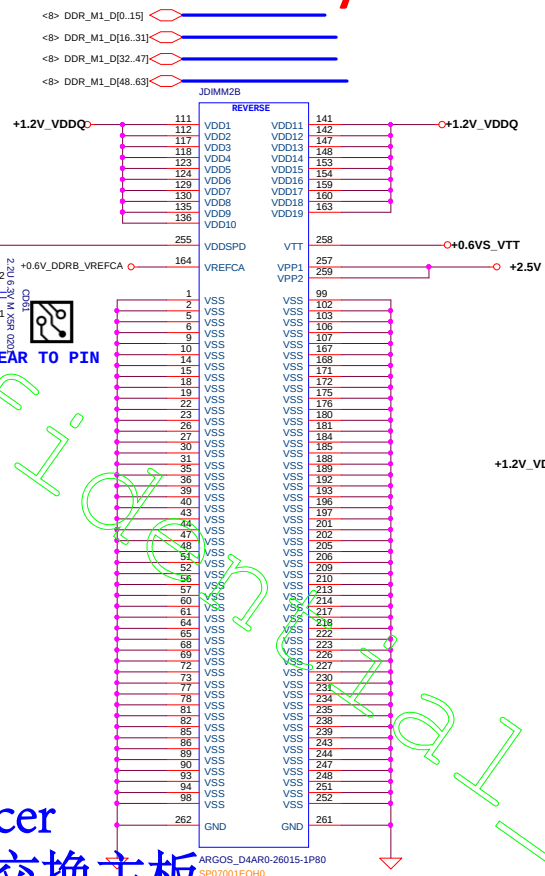


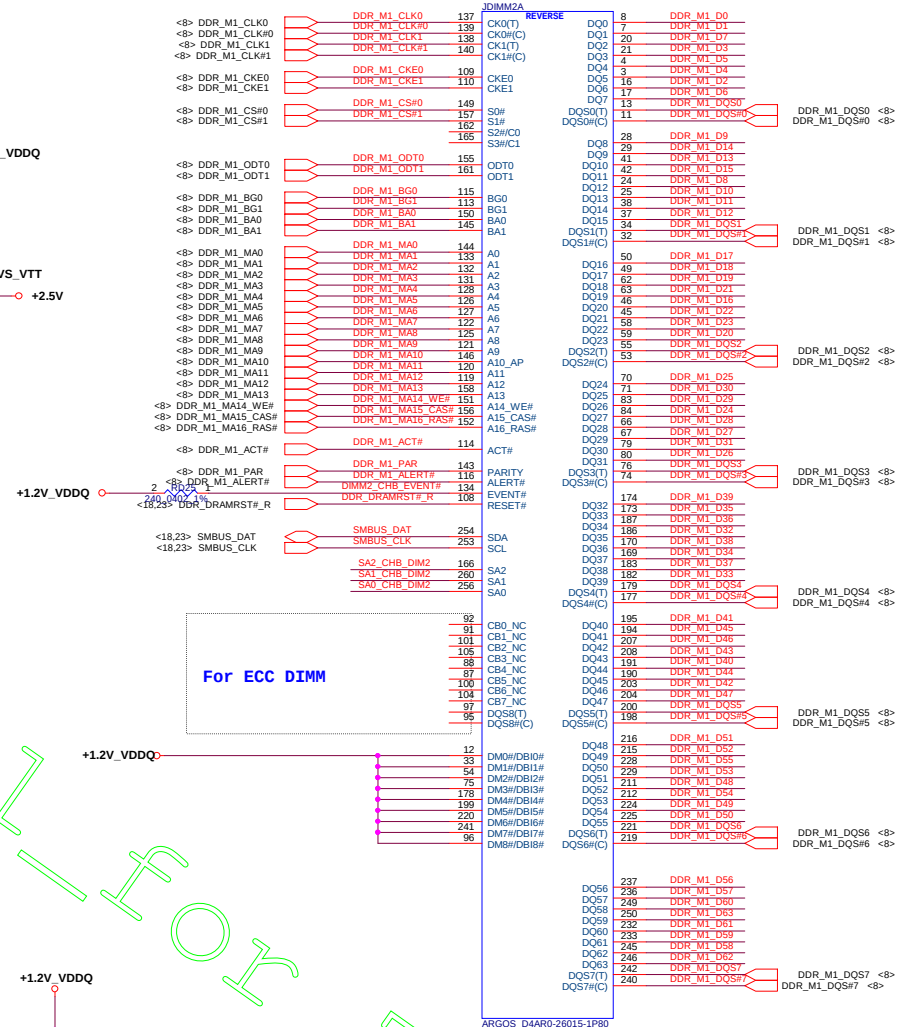
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

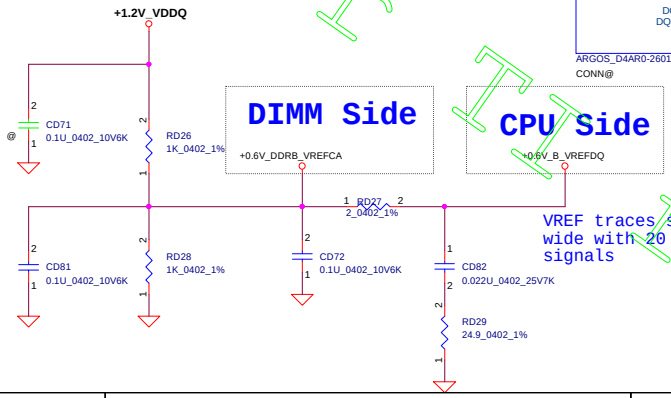


Layout Note:
Place near JDIMM2









VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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msi 微软平板交换主板
微信 yangyang51241

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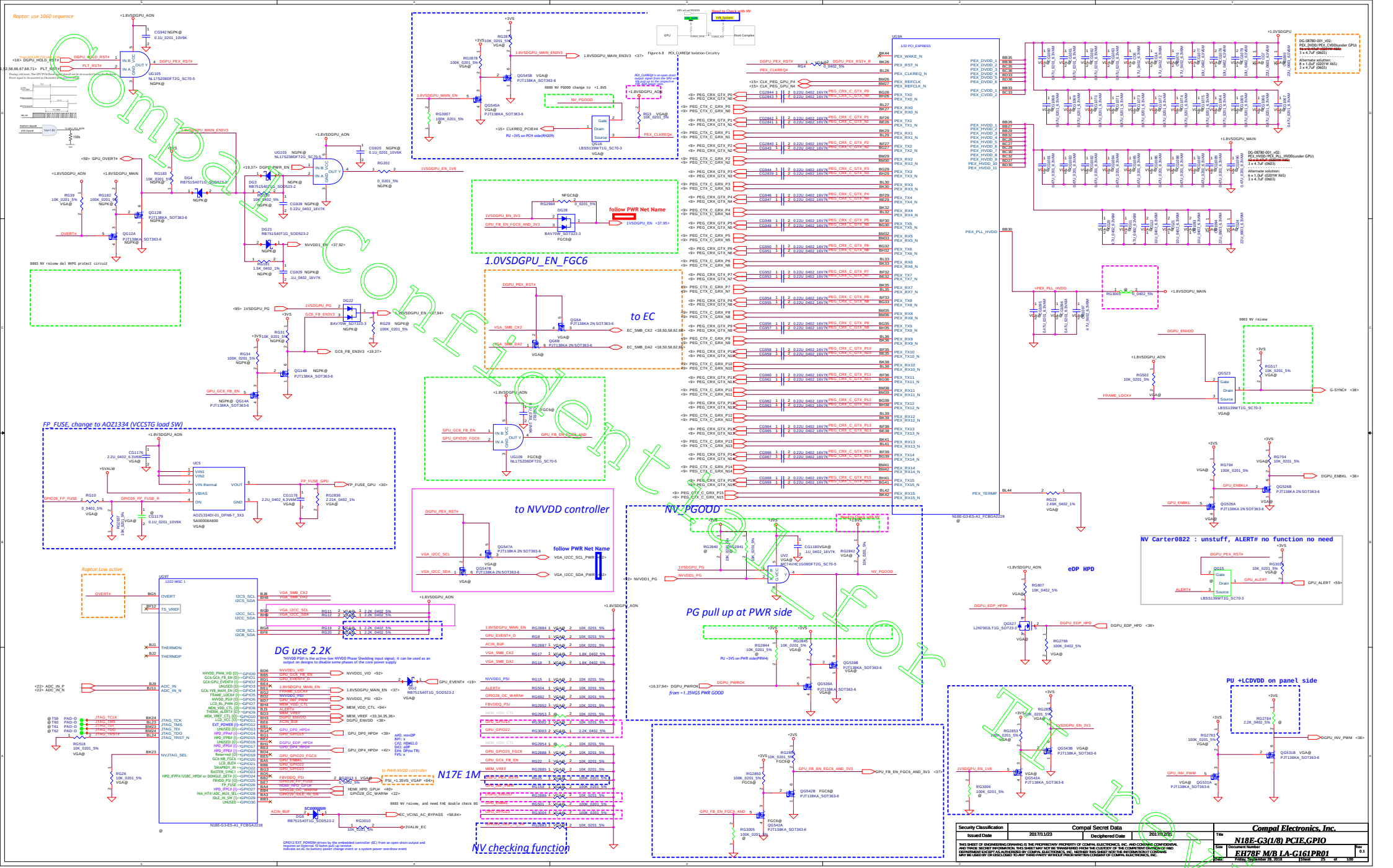
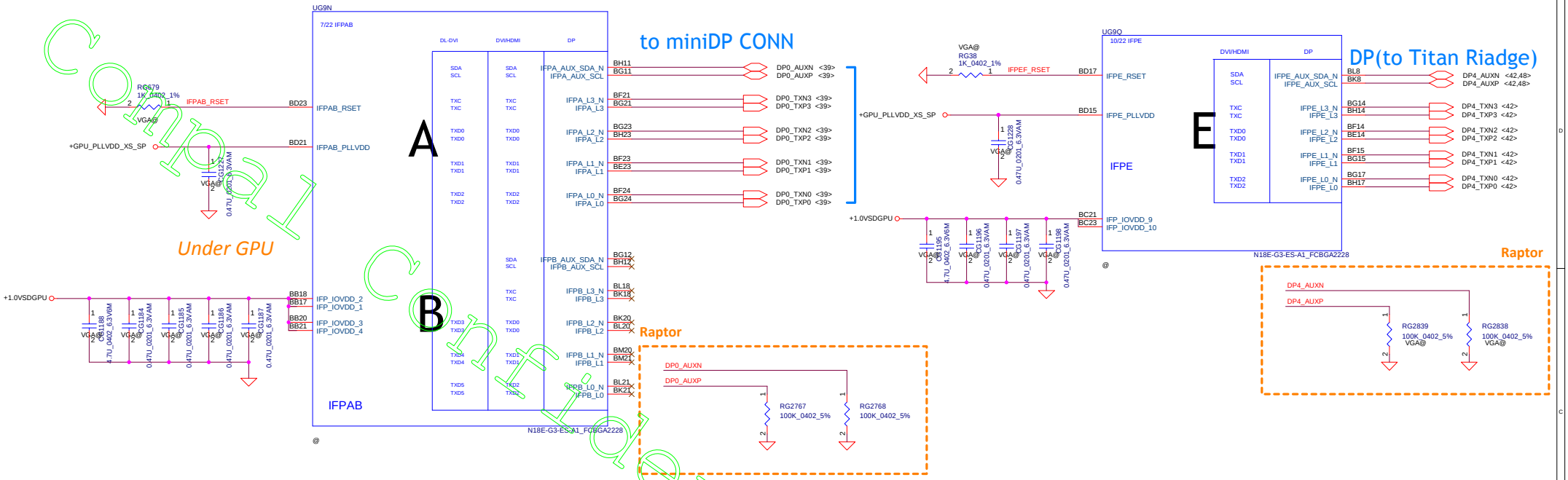
Compal Electronics, Inc.	
Title	DDRIV_CHB: DIMM0
Size	Document Number: FPC72 LA-H492P
Rev	v0.1
Date: Friday, September 28, 2018	Sheet 24 of 100


Raptor: use 1060 sequence
1.0VSDGPU_EN_FGC6
to EC
to NVVDD controller
NV_PGOOD
PG pull up at PWR side
DG use 2.2K
N17E 1M
NV checking function
FP_FUSE_change to AOZ1334 (VCCSTG load SW)
eDP HPD
PU +LCDVDD on panel side
NV Carter0822 : unstuff, ALERT# no function no need
follow PWR Net Name
Compal Secret Data
N18E-G3(1/8) PCIE,GPIO
EH78F M/B LA-G161PR01
联想 ASUS Acer msi 微软平板交换主板 微信 yangyang51241



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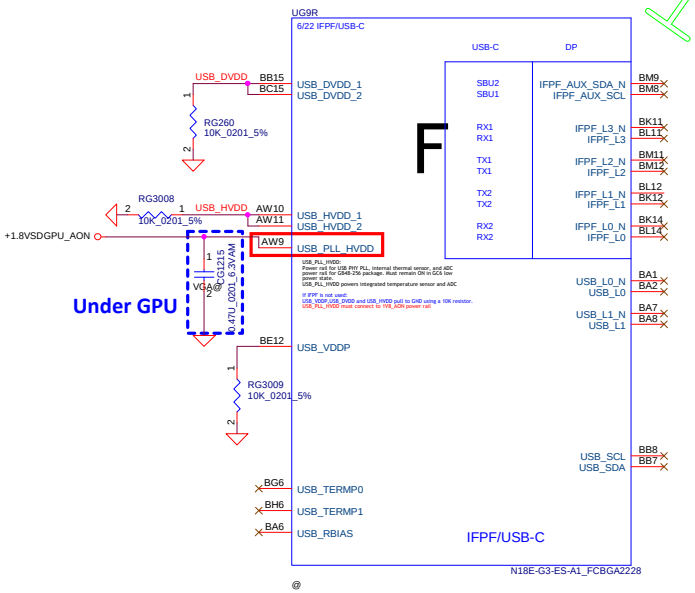

Table 9.1 PCB Display Link Summary (GB4B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort	USBC	
If USB-C is Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		DP(typeC)
IFPB (Link B)	✓(Dual Link with IFPA)			✓		
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓	✓		eDP
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)					✓	
If USB-C is Not Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		DP(typeC)
IFPB (Link B)	✓(Dual Link with IFPA)			✓		
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓			eDP
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)				✓		

Table 9.3 Display Link Power Rail Applicability

Display Link Rail	Display Links that Receive Power from This Rail					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	miniDP ✓	✓	HDMI ✓	eDP ✓	DP(typeC) ✓	✓
IFPAB_PLLVDD	miniDP ✓	✓				
IFPCD_PLLVDD			HDMI ✓	eDP ✓		
IFPEF_PLLVDD					DP(typeC) ✓	✓

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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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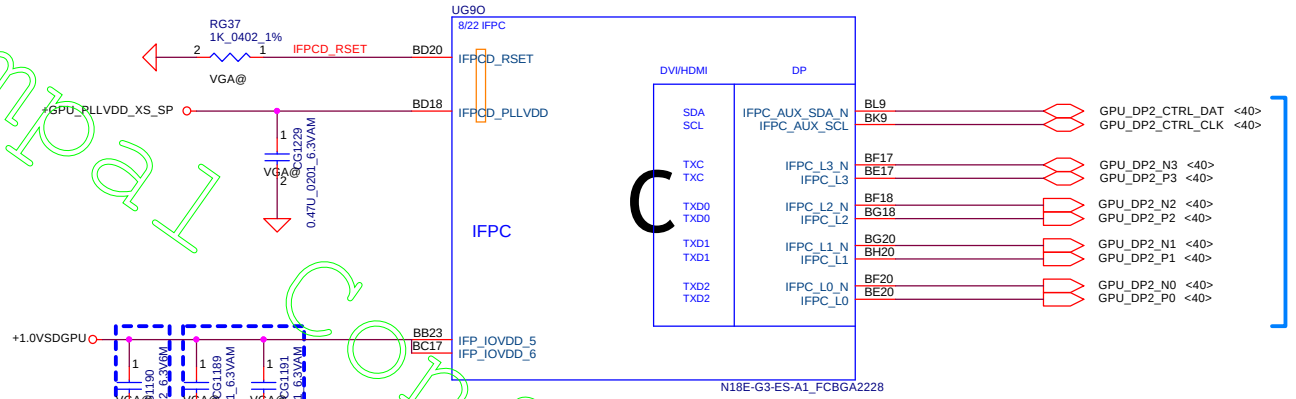
Title	N18E-G3(2/8) DP
Size	Document Number: EH78F M/B LA-G161PR01
Rev	0.1
Date: Friday, September 28, 2018	Sheet 26 of 100



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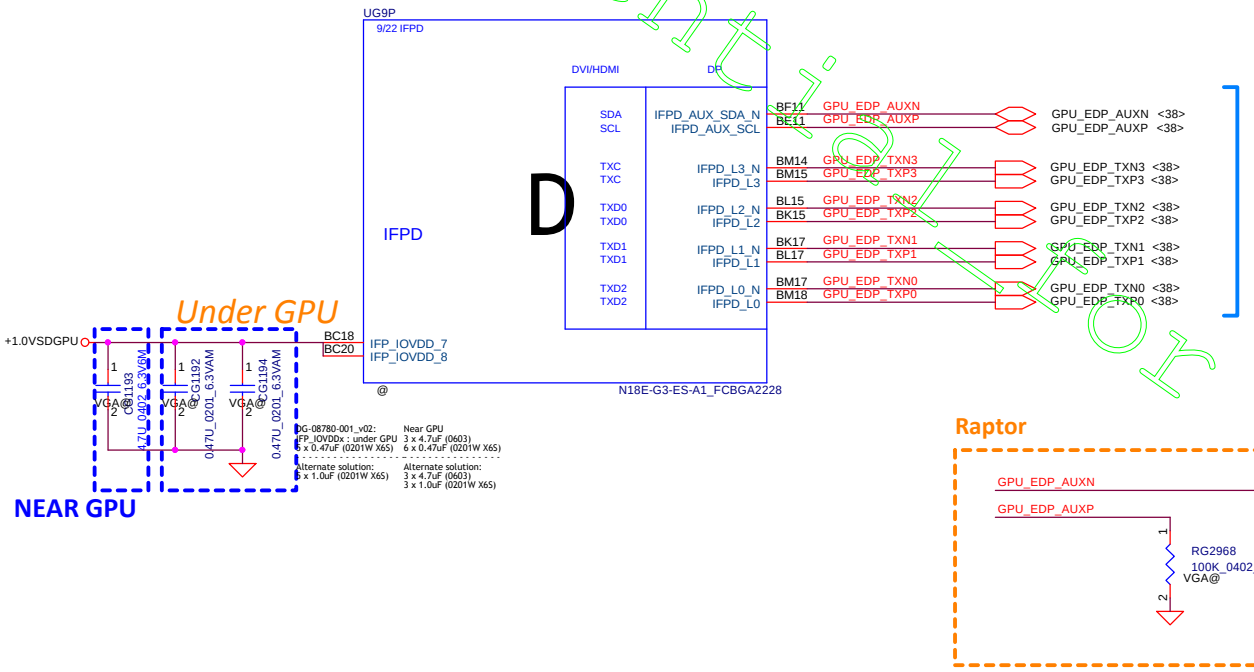
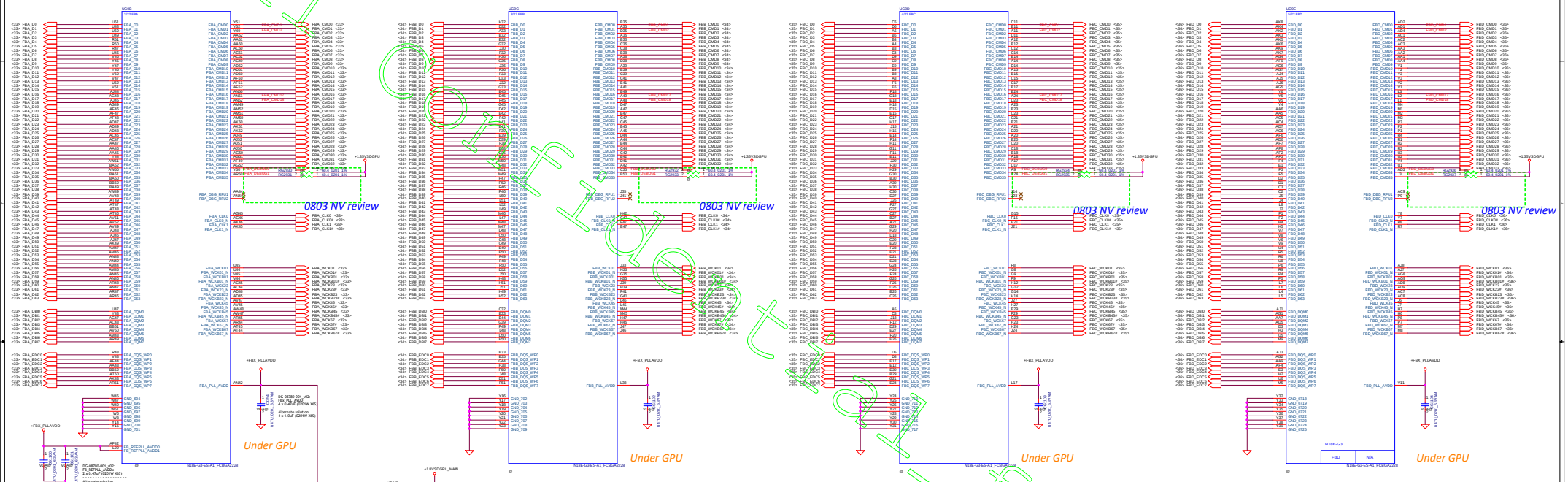
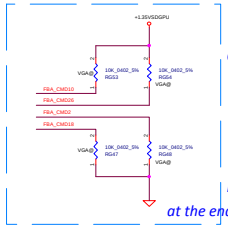
yangyang51241

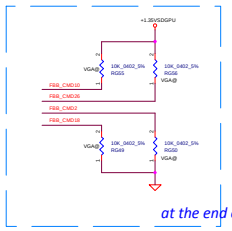


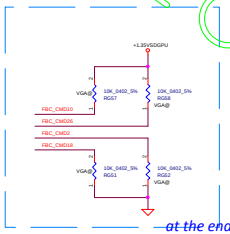
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

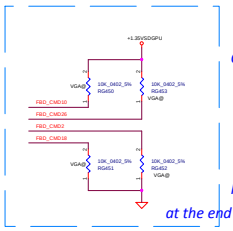
Compal Electronics, Inc.			
Title	N18E-G3(3/8) eDP,HDMI		
Size	Document Number		Rev
	EH78F M/B LA-G161PR01		0.1
Date:	Friday, September 28, 2018	Sheet	27 of 100



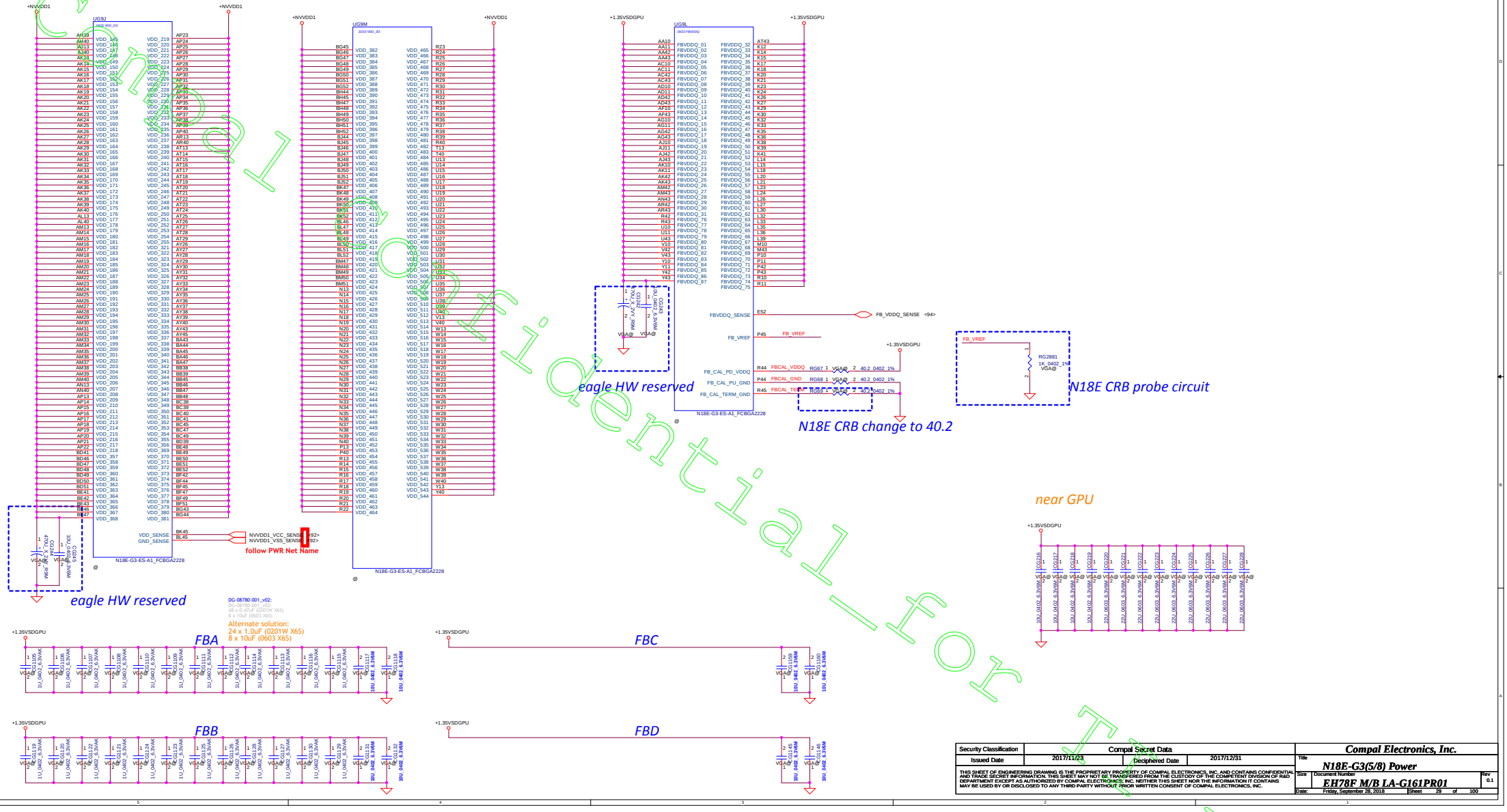








Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/11/23	Deciphered Date	2017/12/31
			Title: N18E-G34(4/8) MEM
			Size: Document Number: FH78F M/B LA-G161P R01
			Date: Tuesday, December 26, 2017 Sheet 39 of 45



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Title: **N18E-G3(5/8) Power**

Size: | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

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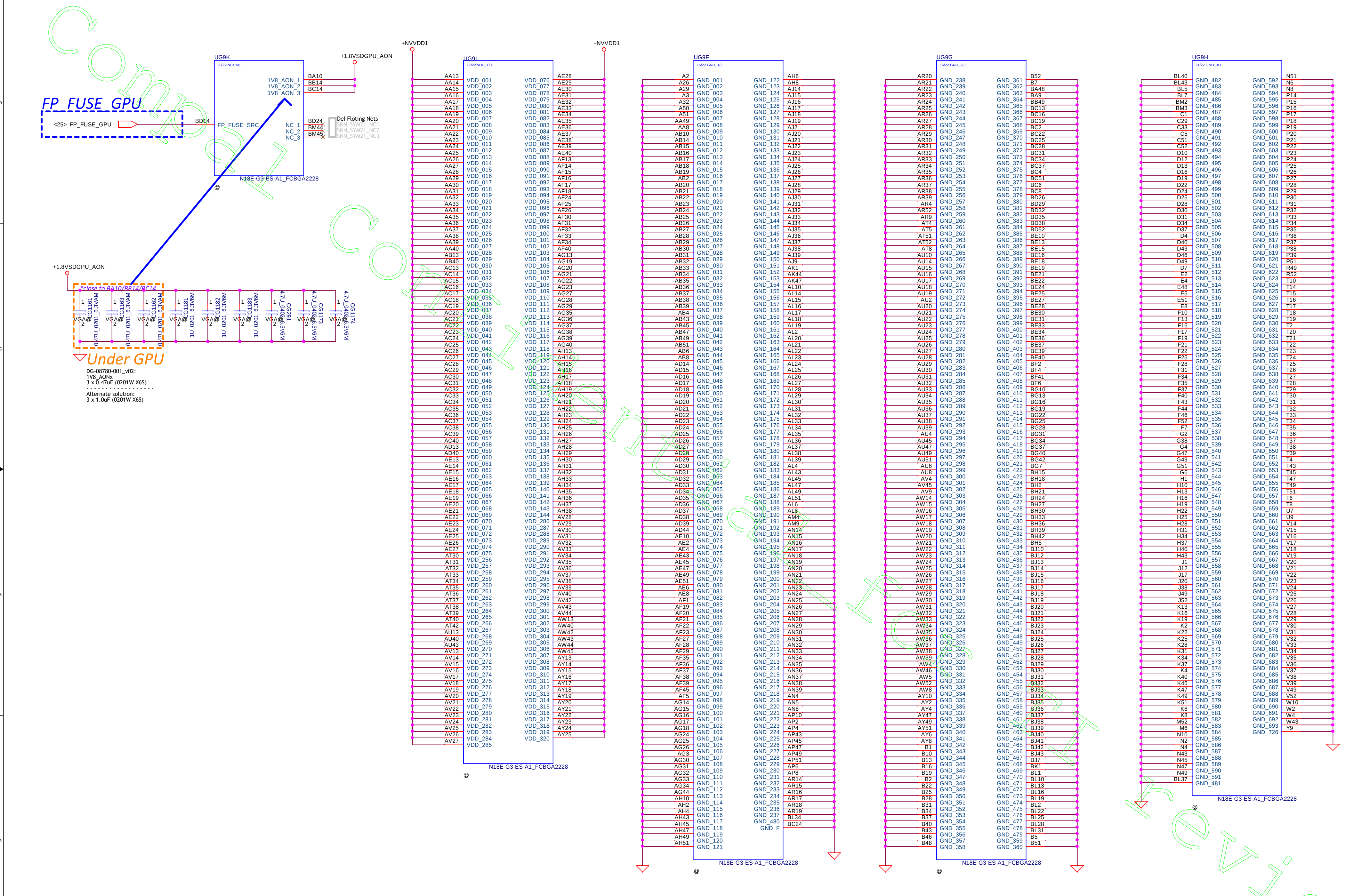

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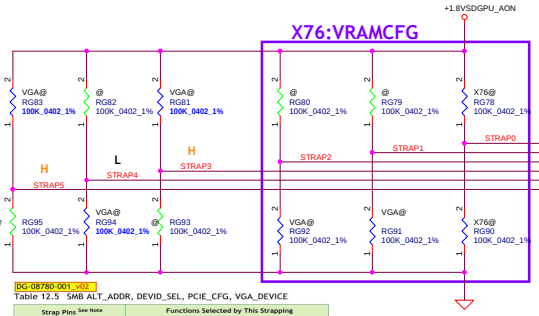
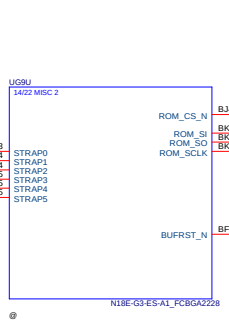
Title: **N18E-G3(6/8) Power,GND**

Size	Document Number	Rev
	EH78F M/B LA-G161PR01	0.1

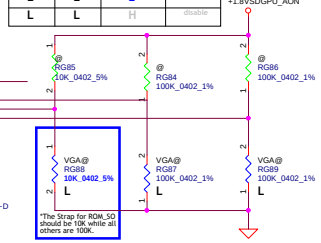
Date: Friday, September 28, 2018 Sheet 30 of 100

X76:VRAMCFG





ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT#
L	L	L	Enable
L	L	H	disable



DG-08780-001_v02

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

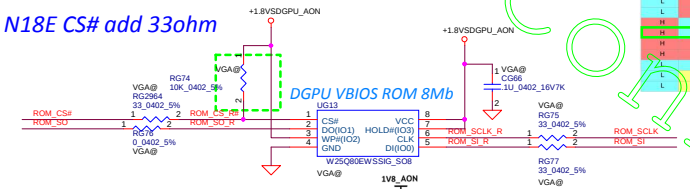
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

DEVID_SEL:
0: Normal Panel
1:G-SYNC Panel

VGA_DEVICE:
0: No Display out
1:GPU Display out=1

N18E CS# add 33ohm

DGPU VBIOS ROM 8Mb



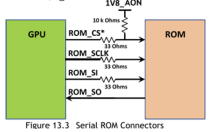
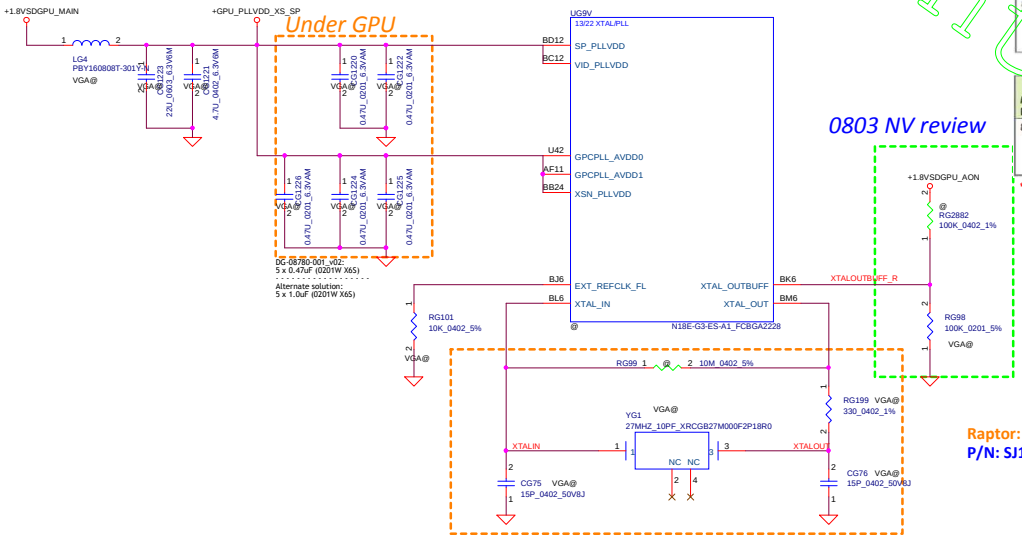


Figure 13.3 Serial ROM Connectors

Under GPU



0803 NV review

RVL-08928-001_v03	N18E G3	N18E G2	N18E G1	(MSB) Strap2	Strap1	(LSB) Strap0	(MSB) Strap5	Strap4	(LSB) Strap3	ROM_SO	ROM_SI	ROM_SCLK	Note
Micron MT61K256M32JE-14:A (0x1)	V	V	TBD	PD 100kOhm	PD 100kOhm	PU 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Samsung K4Z80325BC-HC14 (0x0)	V	V	TBD	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Hynix H56C8H24MJR-S2C (0x2)		V	TBD	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
TBD													

Note: GPU Discrete or Hybrid impact Strap3~Strap5 deisgn

RVL-08928-001_v04

Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 3. N18E-G0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

*DVS is required. WCK: TBD

Table 12.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	M	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Raptor: change to follow 2018 VX SJ10000UI00
P/N: SJ10000UI00 (S CRYSTAL 27MHZ 10PF XRCGB27M000F2P18R0)

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

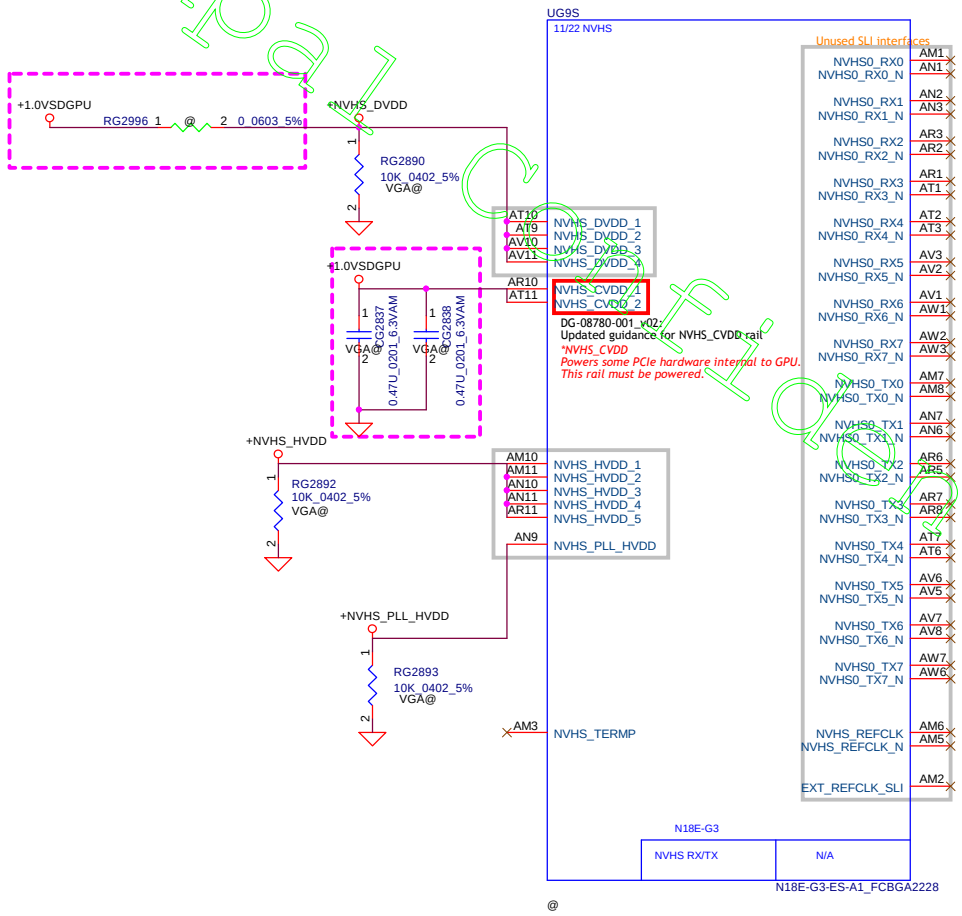
Compal Electronics, Inc.

Title: N18E-G3(7/8) Strap,ROM

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 31 of 100

Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



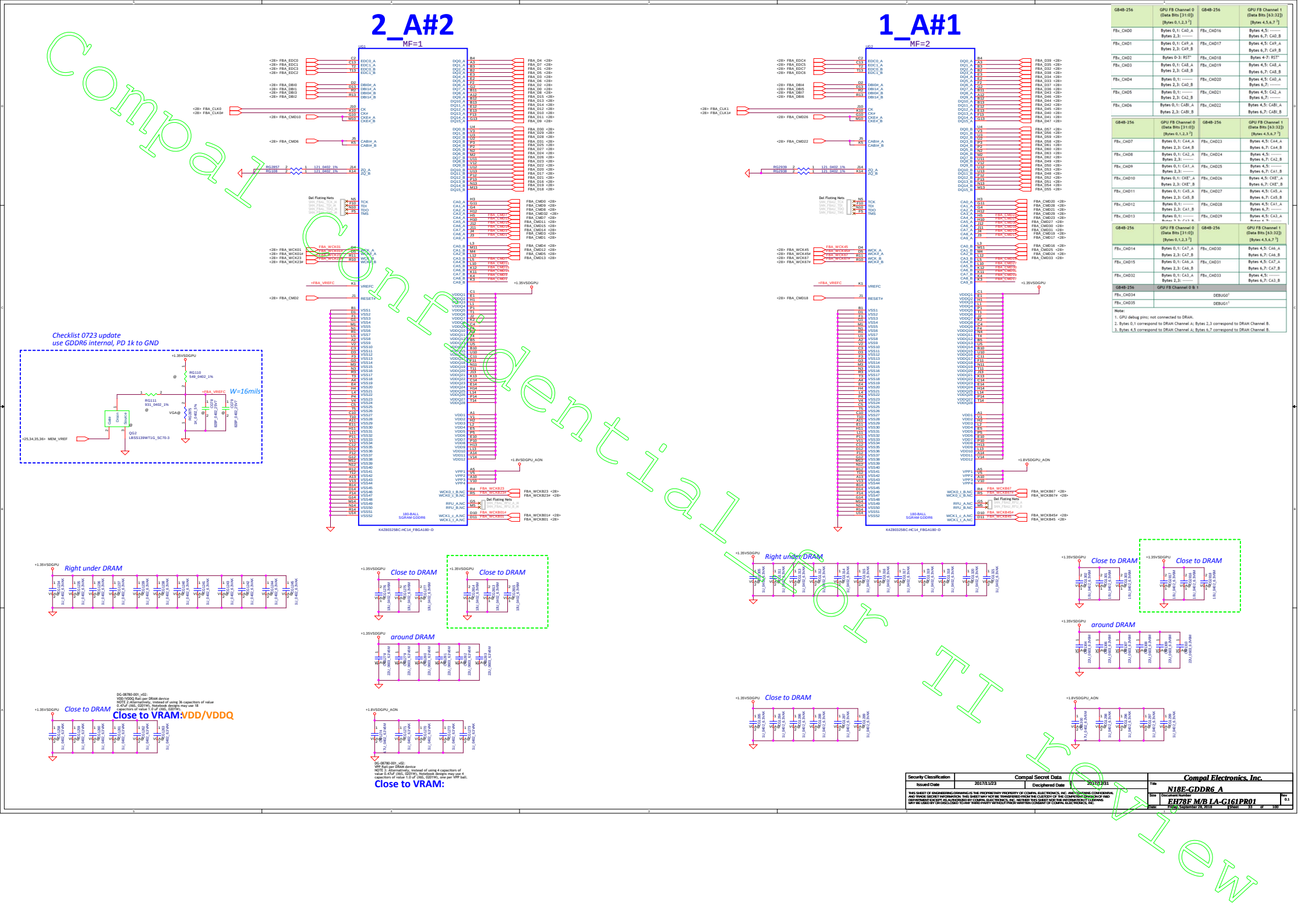
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: **N18E-G3(8/8) NVLINK**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 32 of 100



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: --------	FBx_CMD16	Bytes 4,5: -------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Byte 0-3: RST#	FBx_CMD18	Bytes 4-7: RST#
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: -------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: --------
FBx_CMD5	Bytes 0,1: -------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: --------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: --------	FBx_CMD24	Bytes 4,5: -------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: --------	FBx_CMD25	Bytes 4,5: -------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE'_A Bytes 2,3: CKE'_B	FBx_CMD26	Bytes 4,5: CKE'_A Bytes 6,7: CKE'_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: -------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: --------
FBx_CMD13	Bytes 0,1: -------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: --------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: --------	FBx_CMD33	Bytes 4,5: -------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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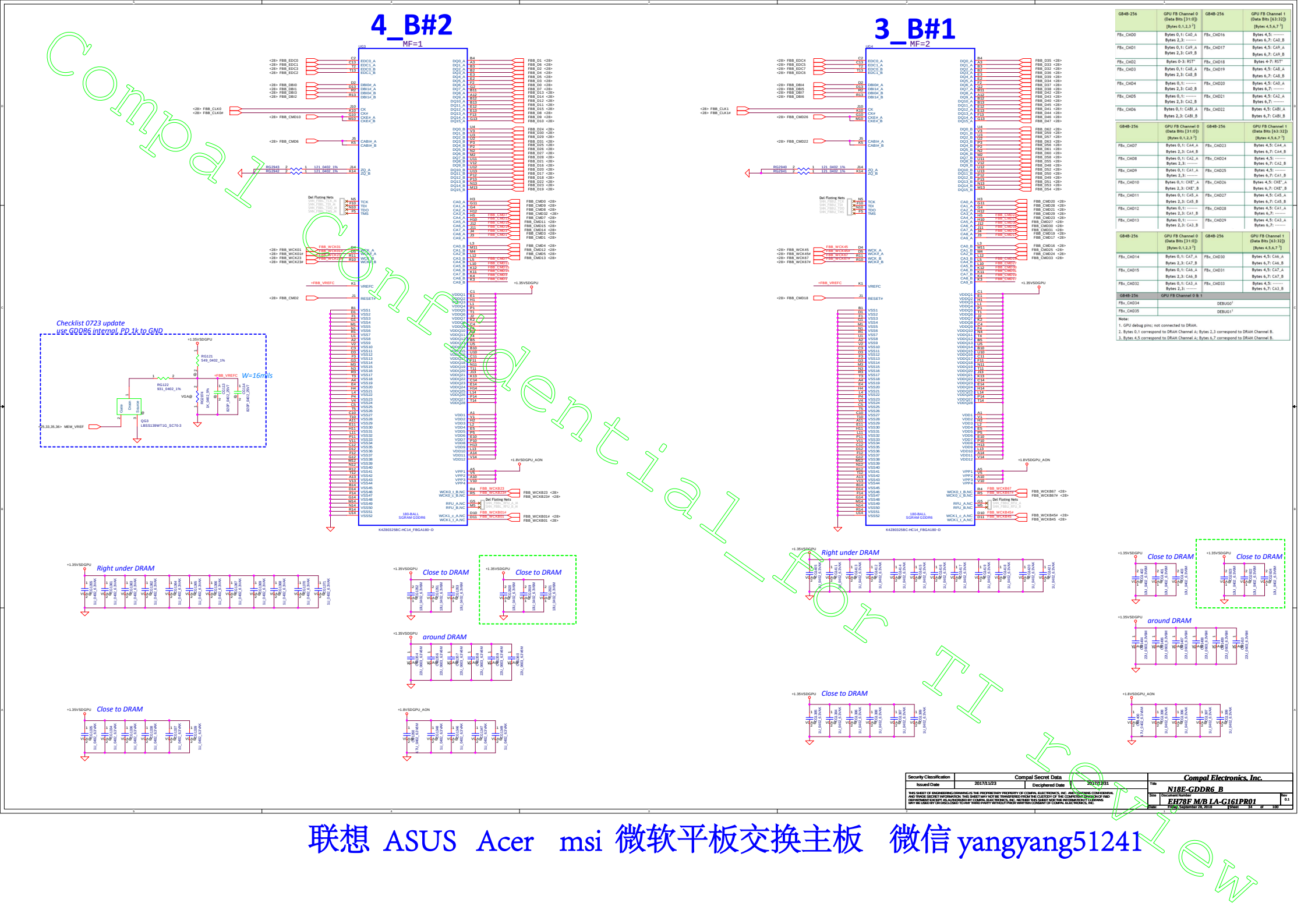

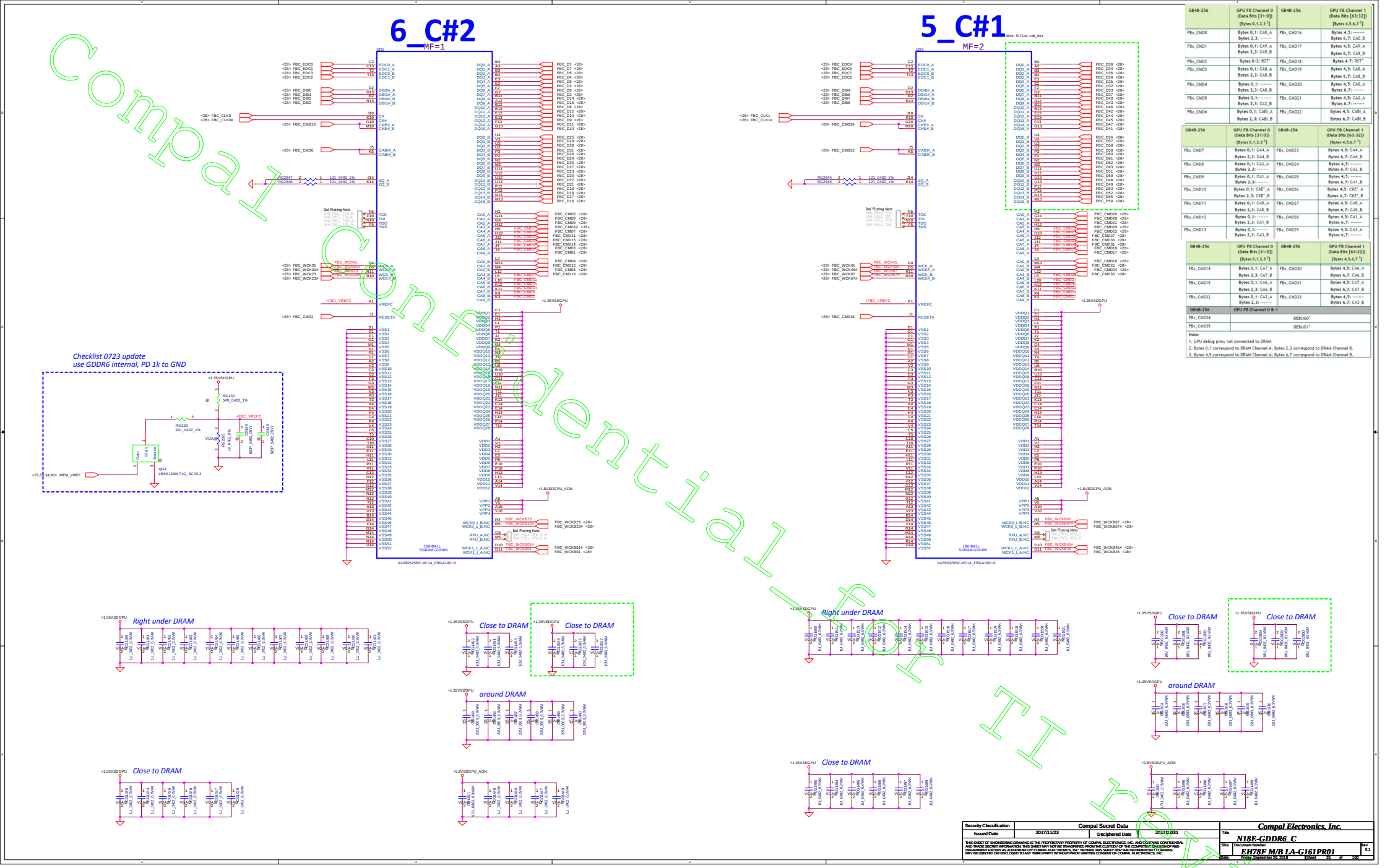

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0 [1]
FBx_CMD35	DEBUG1 [1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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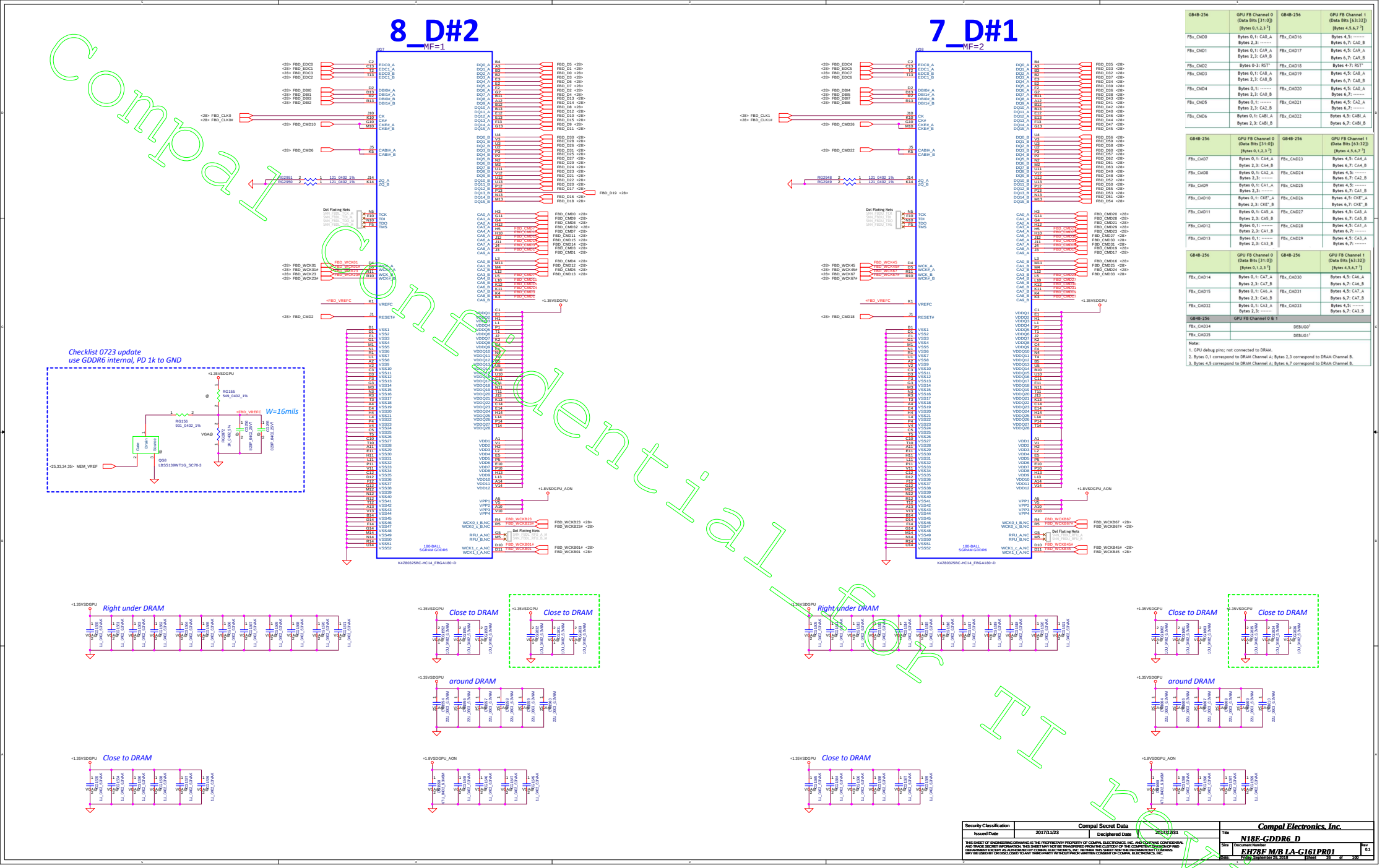
			Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1
			Date: Friday, September 28, 2018 Sheet 35 of 100



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: ------	FBx_CMD16	Bytes 4, 5: ------ Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------ Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: ------
FBx_CMD5	Bytes 0, 1: ------ Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: ------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: ------	FBx_CMD24	Bytes 4, 5: ------ Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: ------	FBx_CMD25	Bytes 4, 5: ------ Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------ Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: ------
FBx_CMD13	Bytes 0, 1: ------ Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: ------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: ------	FBx_CMD33	Bytes 4, 5: ------ Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

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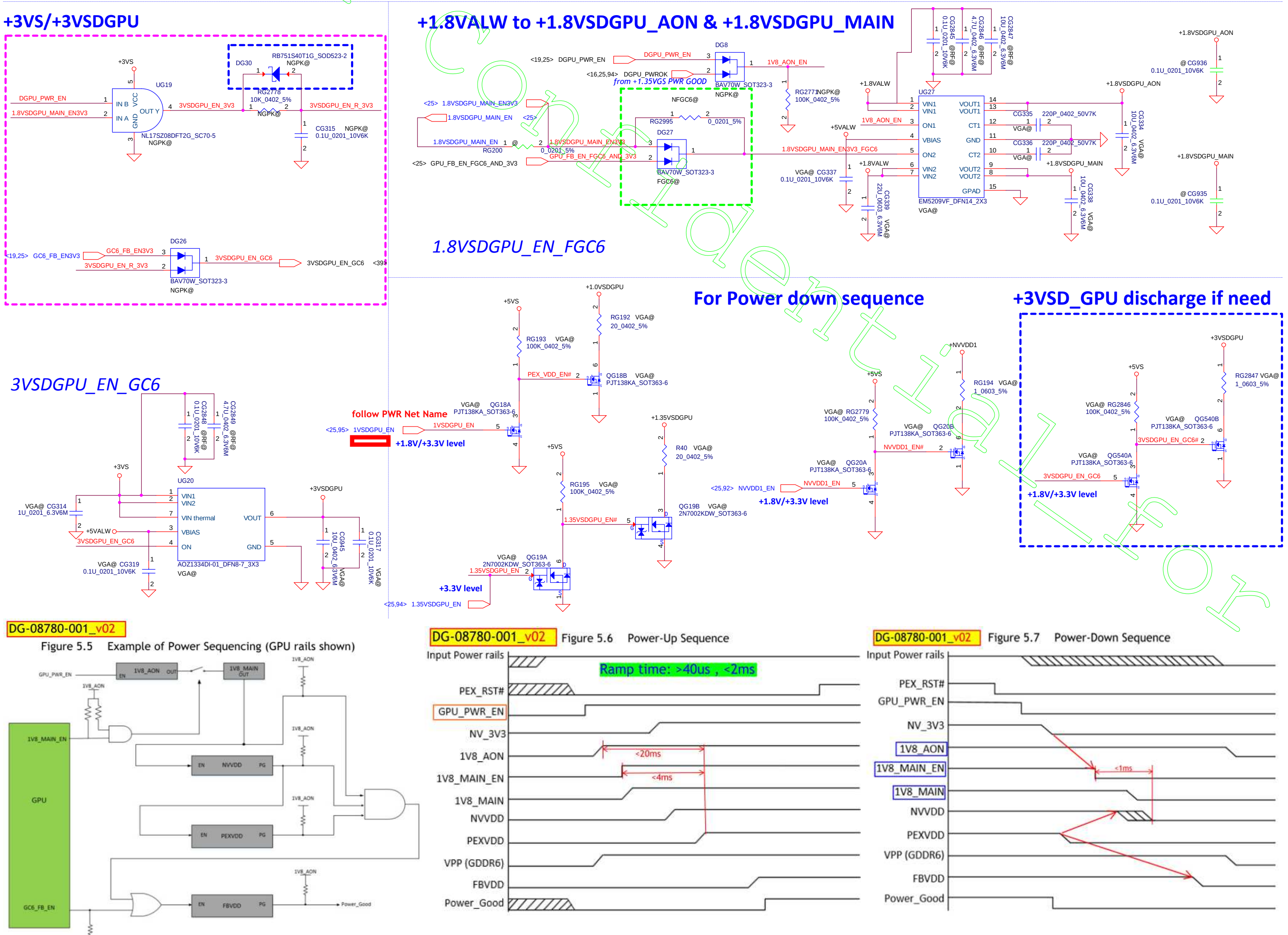
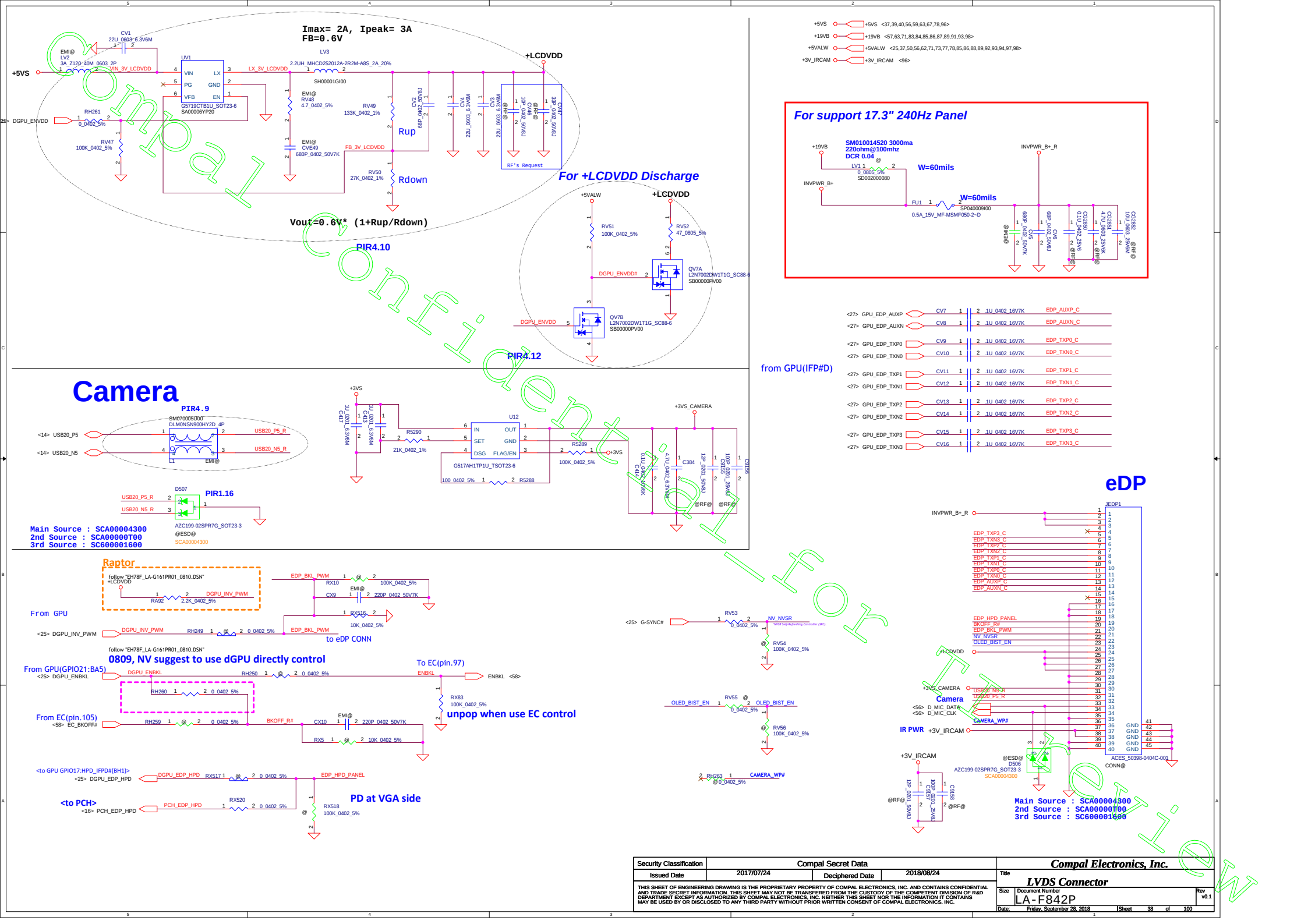
		Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1
		Date: Friday, September 28, 2018 Sheet 35 of 105

No Reserved NV Sequence IC: SILEGO GreenPAK
SA0000B9H00, S IC SLG4U41989VTR STQFN 20P LOGIC SOC



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date 2017/11/23	Deciphered Date 2017/12/15		Title: N18E-GPU Power control
			Document Number: EH78F M/B LA-G161PR01 Rev 0.1
			Date: Friday, September 28, 2018 Sheet 37 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title: LVDS Connector			
Size	Document Number: LA-F842P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 38 of 100		

0 = GPIO mode (I2C disabled)

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

bit[2]H:1
bit[1]L:0
bit[1]L:0

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

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DP only

DP only

Need Check

CAD_SNK/29:
H = AUX snoop disabled with all lanes active
L = AUX snoop enabled
HPDIN(32):
Input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX to SBU switch will remain closed.

Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC0000001600

DP++ and isolated circuit

minDP HPD

0921 change souce to +3VALW, CTRL to SUSP#

OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1 (0:DP)
L	H	B2	A=B2 (1:HDMI)
H	X	Z	NC

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

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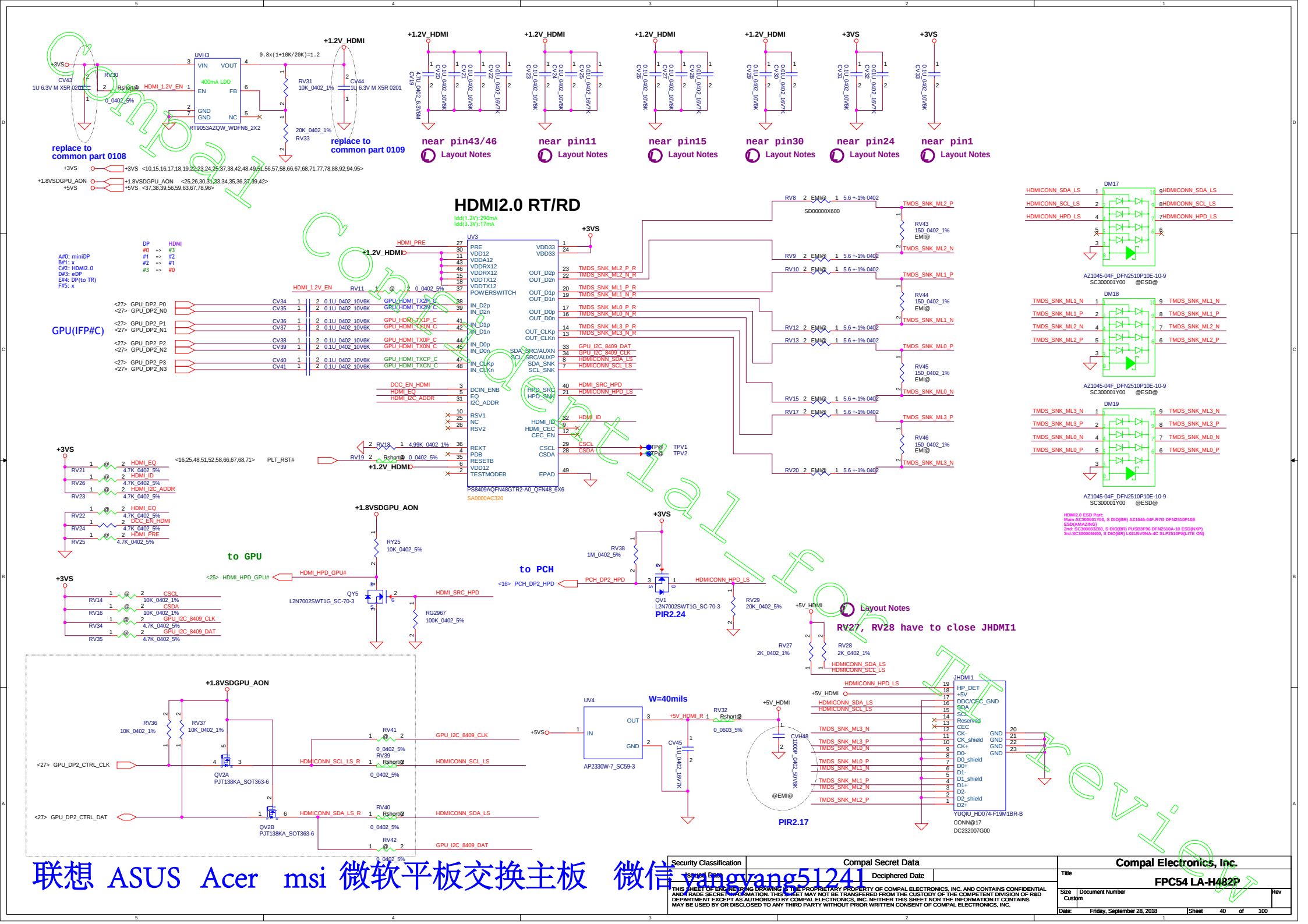
Compal Electronics, Inc.

Title: mDP redriver(TUSB546)

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 39 of 100



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Issued Date	Deciphered Date	Title	FPC54 LA-H482P
		Size: Custom	Document Number: Rev
		Date: Friday, September 28, 2018	Sheet 40 of 100

联想 ASUS Acer msi 微软平板交换主板 微信 yangyang51241

TBD: Empty Page

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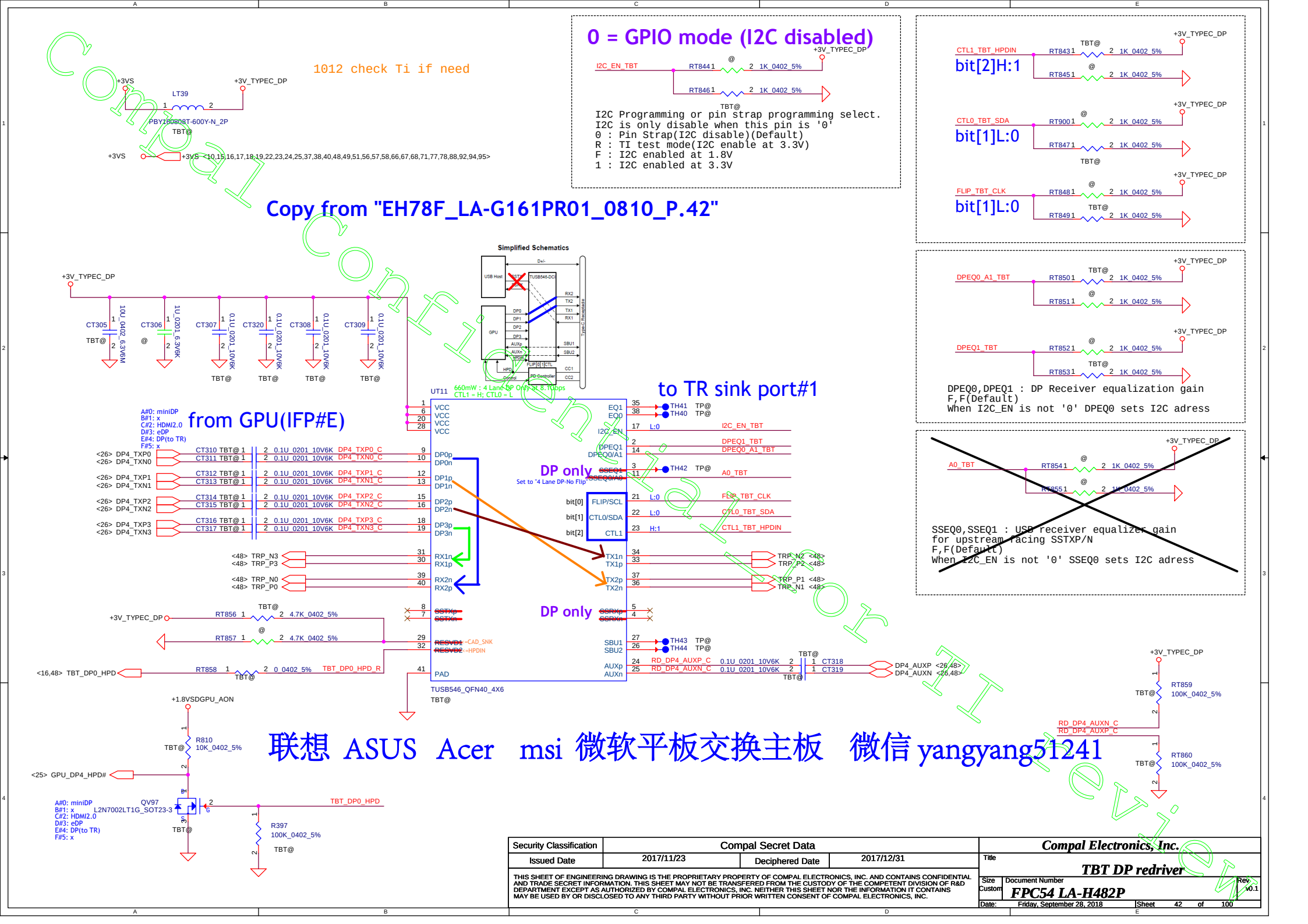
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 41 of 100		


1012 check Ti if need
+3VS
+3V_TYPEC_DP
LT39
PBY160808T-600Y-N_2P
TBT@
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,48,49,51,56,57,58,66,67,68,71,77,78,88,92,94,95>
0 = GPIO mode (I2C disabled)
I2C_EN_TBT
RT8441 2 1K_0402_5%
RT8461 2 1K_0402_5%
I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V
CTL1_TBT_HPDIN
bit[2]H:1
RT8431 2 1K_0402_5%
RT8451 2 1K_0402_5%
CTL0_TBT_SDA
bit[1]L:0
RT9001 2 1K_0402_5%
RT8471 2 1K_0402_5%
FLIP_TBT_CLK
bit[1]L:0
RT8481 2 1K_0402_5%
RT8491 2 1K_0402_5%
Copy from "EH78F_LA-G161PR01_0810_P.42"
Simplified Schematics
DPEQ0_A1_TBT
RT8501 2 1K_0402_5%
RT8511 2 1K_0402_5%
DPEQ1_TBT
RT8521 2 1K_0402_5%
RT8531 2 1K_0402_5%
DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress
CT305 10U_0402_6.3V6M
CT306 1U_0201_6.3V6K
CT307 0.1U_0201_10V6K
CT320 0.1U_0201_10V6K
CT308 0.1U_0201_10V6K
CT309 0.1U_0201_10V6K
UT11
660mW : 4 Lane DP Only at 8.1Gbps
CTL1 = H; CTL0 = L
TUSB546_QFN40_4X6
from GPU(IFP#E)
to TR sink port#1
DP only
Set to "4 Lane DP-No Flip"
A0_TBT
RT8541 2 1K_0402_5%
RT8551 2 1K_0402_5%
SSEQ0,SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress
RT856 4.7K_0402_5%
RT857 4.7K_0402_5%
RT858 0_0402_5%
TBT_DP0_HPD_R
R810 10K_0402_5%
QV97 L2N7002LT1G_SOT23-3
R397 100K_0402_5%
RT859 100K_0402_5%
RT860 100K_0402_5%
RD_DP4_AUXN_C
RD_DP4_AUXP_C
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TBT DP redriver
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Sheet
42
of
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Date: Friday, September 28, 2018	Sheet 47 of 100		

Copy from "DDX03_LS-F262PR02_0309A"

"559414-manufacturing-test-thunderbolt-mas-rev-2-3-from-9-21-2017"
CNL supports HBR3 (8.1G), but no DSC (so only DP1.3), DP1.4 supported in TR, but only via discrete GFX silicon w/ DP1.4 logic

Titan Ridge SP - High Speed (CIO, USB and PCIe) Parts

Titan Ridge
Dual Port(TR-DP): JHL7540
Single Port(TR-SP):JHL7340

(Default Port)

+3VALW <14,18,20,39,49,50,51,52,58,63,66,71,78,85,86,87,91,92,94,95>
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,49,51,56,57,58,66,67,68,71,77,78,88,92,94,95>
+3V_TBT_LC <49>

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used

From SoC PCIe TX

To SoC PCIe RX

PCIe_IN#0

PCIe GEN3

U1A

PCIE_RX0_P / PCIE_RX0_N
PCIE_RX1_P / PCIE_RX1_N
PCIE_RX2_P / PCIE_RX2_N
PCIE_RX3_P / PCIE_RX3_N
PCIE_TX0_P / PCIE_TX0_N
PCIE_TX1_P / PCIE_TX1_N
PCIE_TX2_P / PCIE_TX2_N
PCIE_TX3_P / PCIE_TX3_N
PERST#
AN_PCIE_RBIAS
TBT_WAKE#
REFCLK_100_IN_P / REFCLK_100_IN_N
PCIE_CLKREQ#

PCIE RBIAS
Place as close as possible to pins

GPU(IFP#E)+Repeater TUSB546
From dGPU DDIx4 for DPv1.4

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

DP_IN#1
DP_IN#2
DP_OUT#0

SINK PORT 1
SINK PORT 2
SOURCE PORT 0
LC GPIO
POC GPIO
USB
M1sc
M1SC
TBT PORTS
Port A
PORT B
DEBUG

DPSNK1_ML0_N / DPSNK1_ML0_P
DPSNK1_ML1_P / DPSNK1_ML1_N
DPSNK1_ML2_P / DPSNK1_ML2_N
DPSNK1_ML3_P / DPSNK1_ML3_N
DPSNK1_AUX_P / DPSNK1_AUX_N
DPSNK1_HPD
DPSNK2_ML0_P / DPSNK2_ML0_N
DPSNK2_ML1_P / DPSNK2_ML1_N
DPSNK2_ML2_P / DPSNK2_ML2_N
DPSNK2_ML3_P / DPSNK2_ML3_N
DPSNK2_AUX_P / DPSNK2_AUX_N
DPSNK2_HPD
U0_SSRXn1 / U0_SSRXp1 / U0_SSTXn1 / U0_SSTXp1
DPSRC_ML0_P / DPSRC_ML0_N
DPSRC_ML1_P / DPSRC_ML1_N
DPSRC_ML2_P / DPSRC_ML2_N
DPSRC_ML3_P / DPSRC_ML3_N
DPSRC_AUX_P / DPSRC_AUX_N
DPSRC_HPD
GPIO_0 / GPIO_1 / TMU_CLKOUT / CIO_PLUG_EVENT# / TMU_CLKIN
I2C_SDA / I2C_SCL / USB_FORCE_PWR / FORCE_PWR / BATLOW# / SLP_S3# / RTD3_PWR_EN
RESET#
XTAL_25_IN / XTAL_25_OUT
TDI / TMS / TCK / TDO
RBIAS / RSENSE
EE_DI / EE_DO / EE_CS# / EE_CLK / EE_WP#
ASSRXp1 / ASSRXn1 / ASSTXp1 / ASSTXn1
ASSRXp2 / ASSRXn2 / ASSTXp2 / ASSTXn2
ASBU1 / ASBU2
PA_USB2_D_P / PA_USB2_D_N
PA_HPD / PA_I2C_INT / PA_USB2_MXCTL / PA_USB2_RBIAS
THERMDA
TEST_EDM / FUSE_VQPS_64
PA_MONDC / PB_MONDC / PC_MONDC / USB_MONDC / MONDC_SVR
TEST_PWR_GOOD / TEST_EN / USB2_ATEST / PCIE_ATEST / ATEST_P / ATEST_N / VGA_RES

NC

Titan Ridge Single Port_JHL7340_BGA337
JHL7340-SLWKY-C1_FC-CSP_337P

DG_FORCE_PWR:
'0' - Regular Mode, Force Power is disabled (Default)
'1' - Force Power Mode is enabled
DG_USB_FORCE_PWR:
Might be use for seperatly force USB domain - connect to EC/PCH
'0' - by default

DG_FORCE_PWR:
Connect to EC/PCH for FW update
'0' - by default
'1' - for debug only

DG_CIO_PLUG_EVENT# should be conncted to PCH SCI GPIO

TBT_GPIO_8
'0' - Unsecure mode
'1' - Secure mode

From TPS65987S.

Follow TR_DP_TI_PD_HOST_REF_DESIGN_R0V95
PE isn't POR -
Please don't use

Place as close as possible to pins

Port_OUT#A

USB2 Rbias Place as close as possible to pins

Need Check if 10K?(RT33)

Figure 1. Titan Ridge SP Controller Block Diagram

Remove JTAG1 Conn

25M XTAL

Y1 25MHZ 20PF FL2500123Z
CT38 20P 50V +-2% NPO 0402
CT39 20P 50V +-2% NPO 0402

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

Dead Battery Mode (Default):
To Support Dead Battery mode R5 should be populate.
+3V_TBT_A_LDO should be connected to +3V_Flash
Desktop:
To support Desktop/RVP, R4 should be populate.
+3VALW should be connected to +3V_Flash

Main Source:SC40000DS00
2nd Source : SC40000AT00
3rd Source : SC40000DM00

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Title: P04-Thunderbolt Titanrid (1/2)		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
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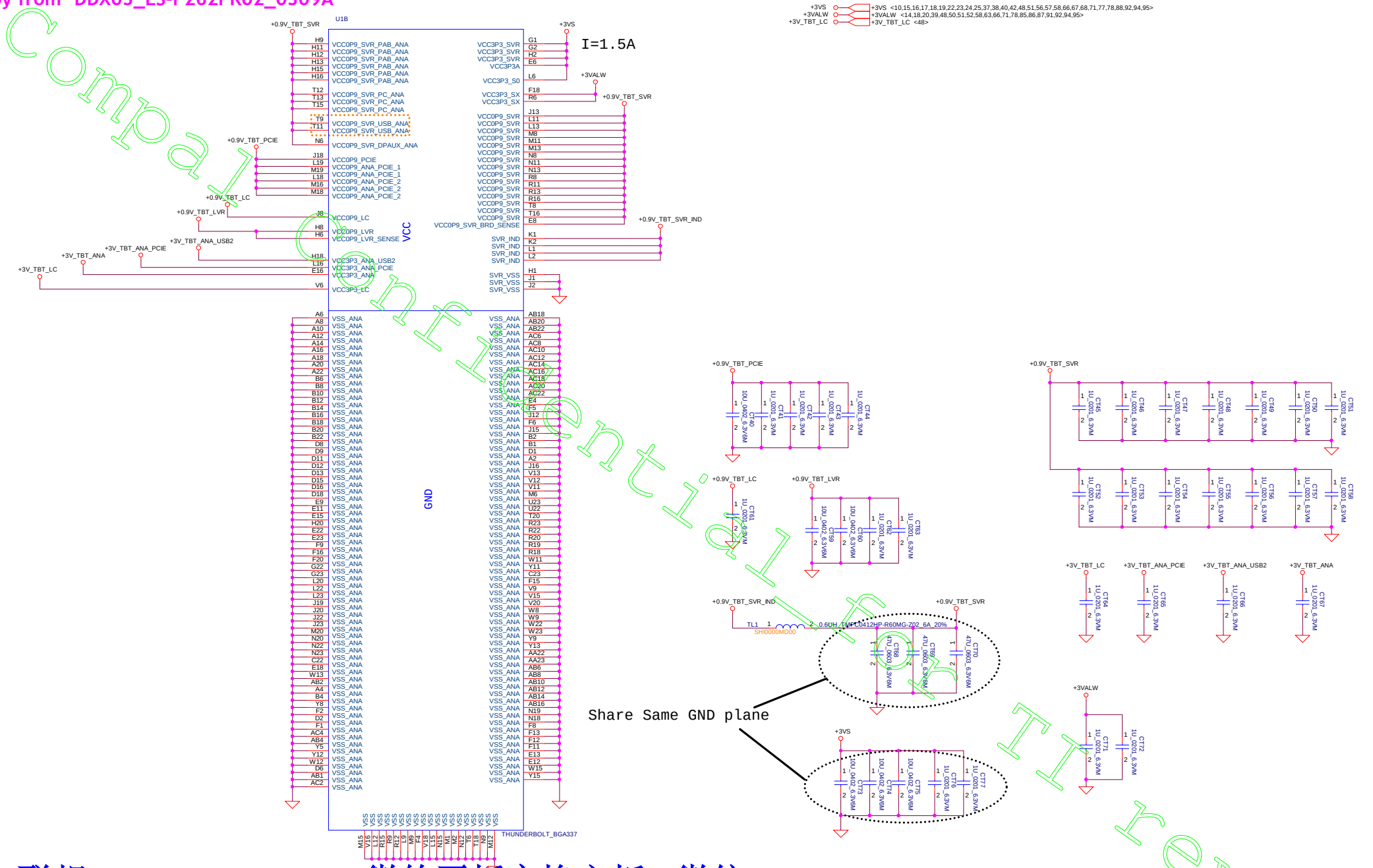

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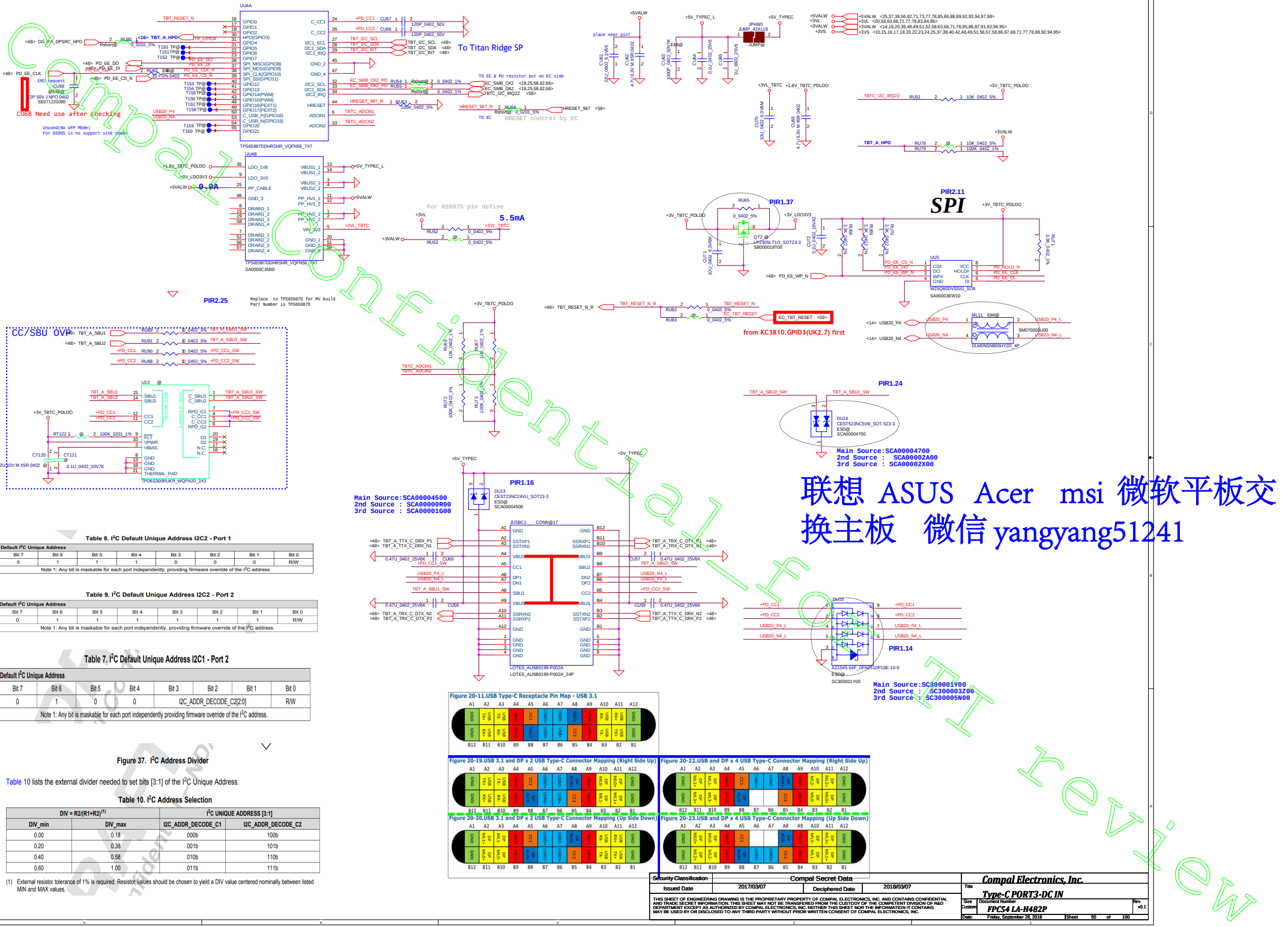

Table 8. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 9. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Figure 20-11.USB Type-C Receptacle Pin Map - USB 3.1

Figure 20-19.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Right Side Up)

Figure 20-22.USB and DP x 4 USB Type-C Connector Mapping (Right Side Up)

Figure 20-10.USB 3.1 and DP x 2 USB Type-C Connector Mapping (Up Side Down)

Figure 20-23.USB and DP x 4 USB Type-C Connector Mapping (Up Side Down)

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Issued Date	2017/03/07	Deciphered Date 2018/03/07

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Title	Type-C PORT3-DC IN
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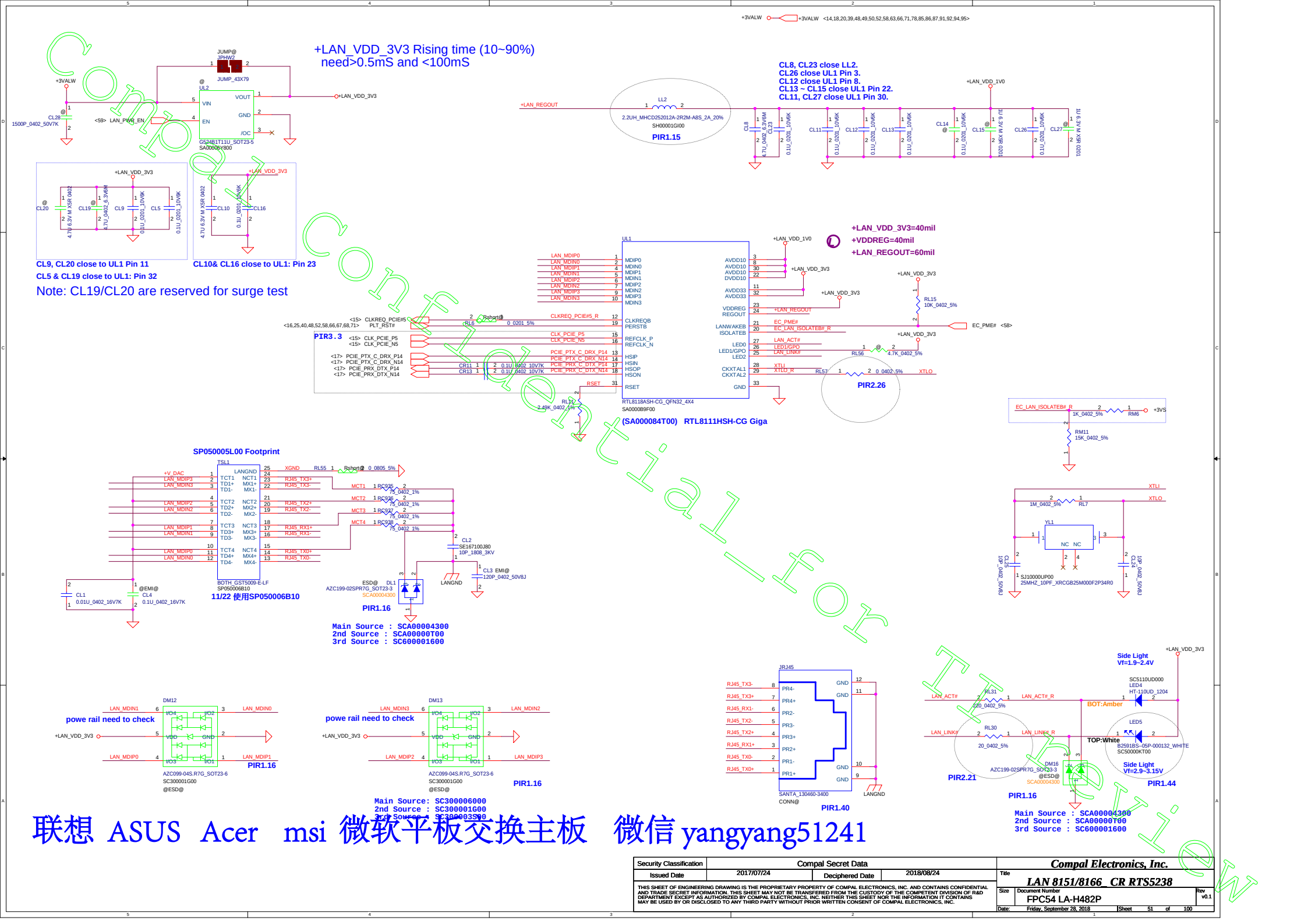

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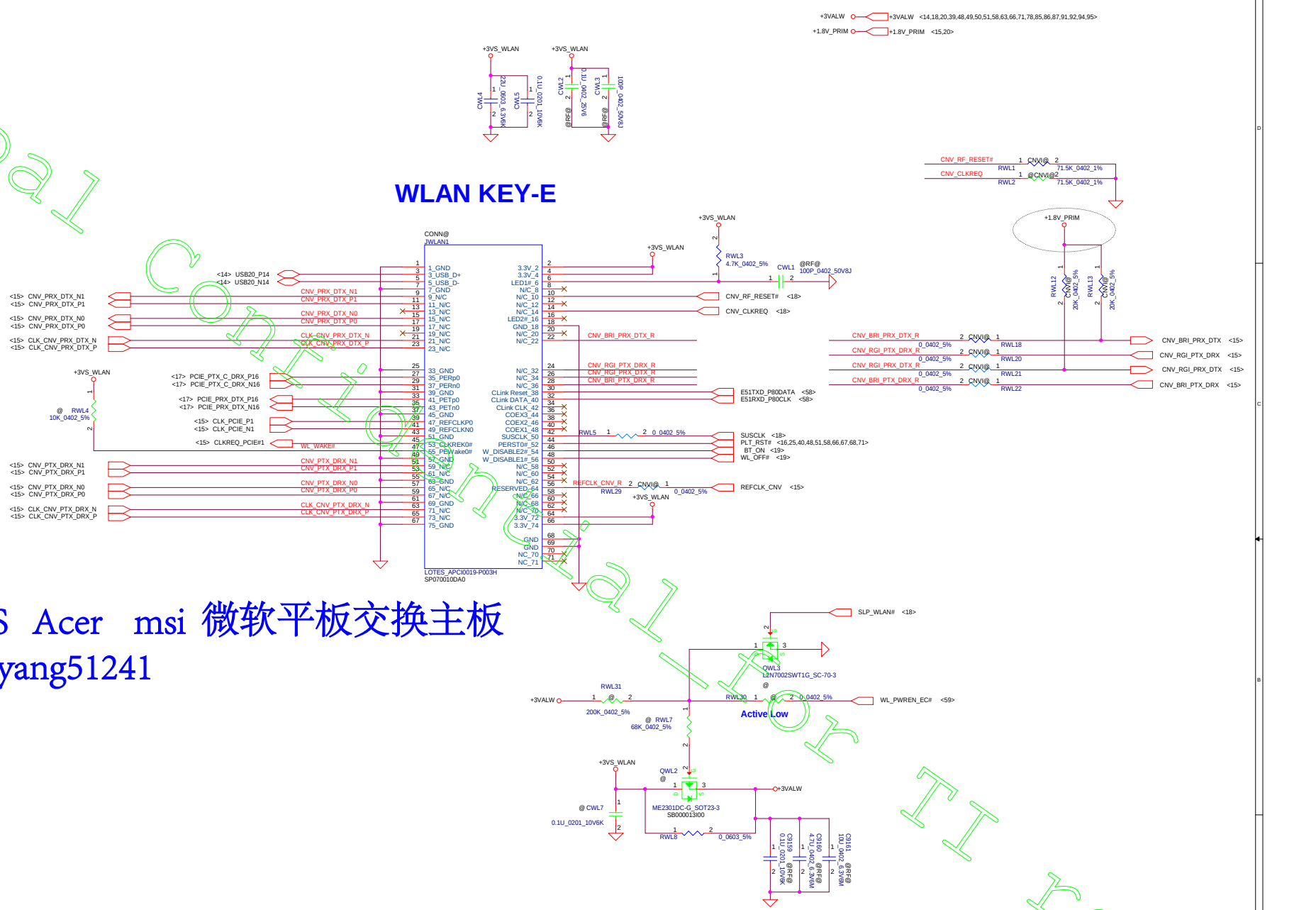
Date:	Friday, September 28, 2018	Sheet	51 of 100

WLAN KEY-E



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Date: Friday, September 28, 2018	Sheet 53 of 100		

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Date: Friday, September 28, 2018	Sheet 54 of 100		

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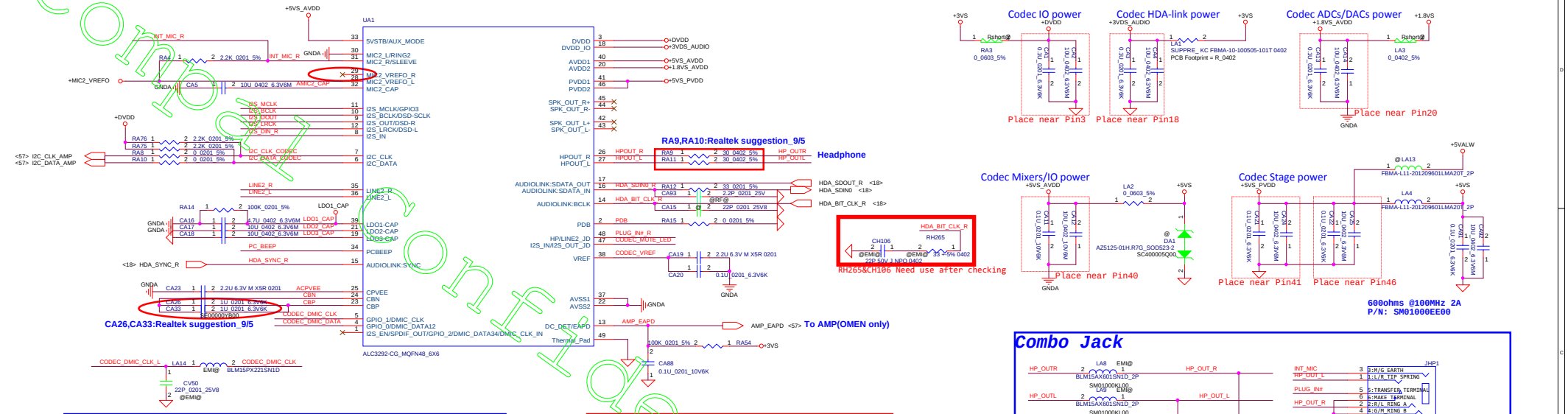
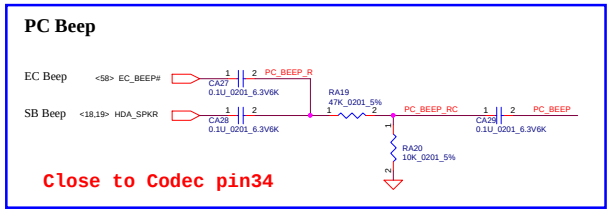
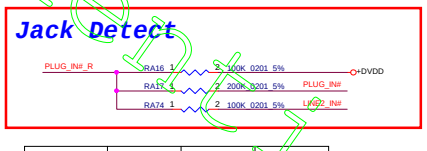
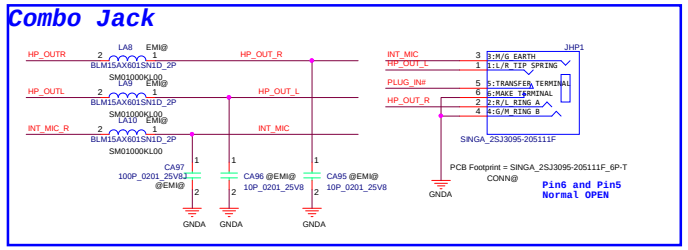
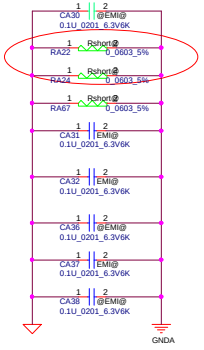


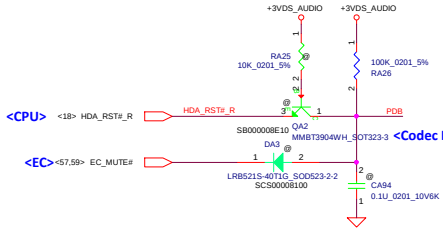


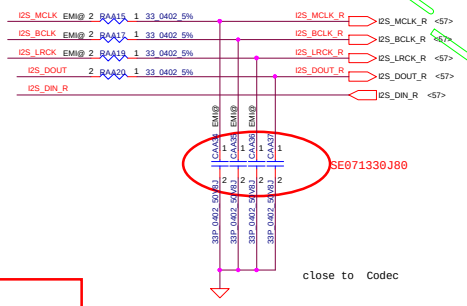


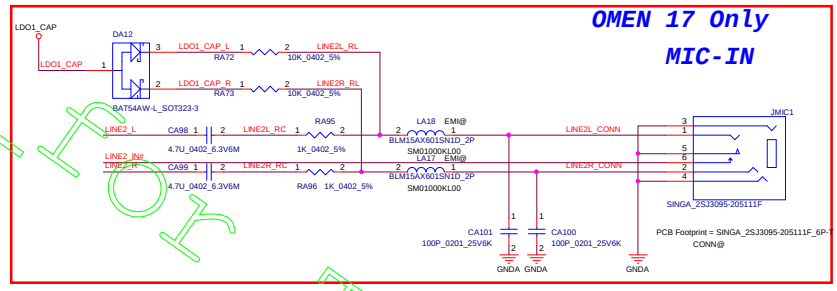
	RA16	RA17	RA74
OMEN_15	@	0_ohm	@
OMEN_17	100K	200K	100K

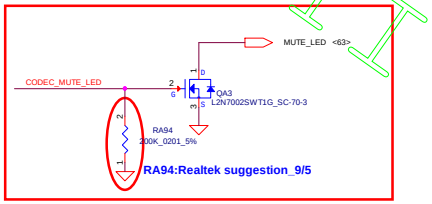


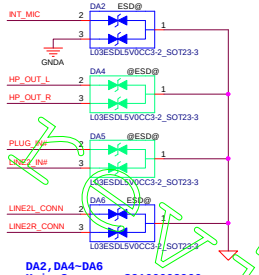


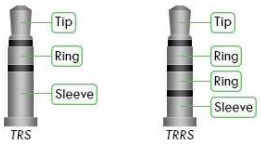


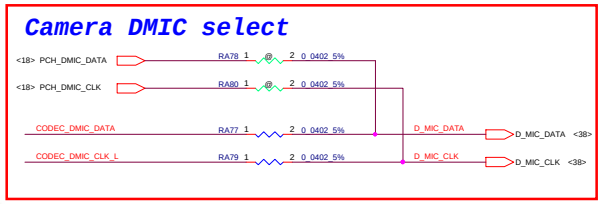












Headphone Jack Type

Audio jack must be plastic without conductive coatings (no chrome)

Individual Audio Jack for Headphone & Microphone

Audio jack pin configuration:
Combo Jack (Headset / Headphone compatible)
Tip = Left
1st ring = Right
2nd ring = Ground
Sleeve = Mono microphone

Microphone Jack (Milos/Santorini Only)
Tip = Left
Ring = Right
Sleeve = Ground

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: AUDIO ALC3292-CG

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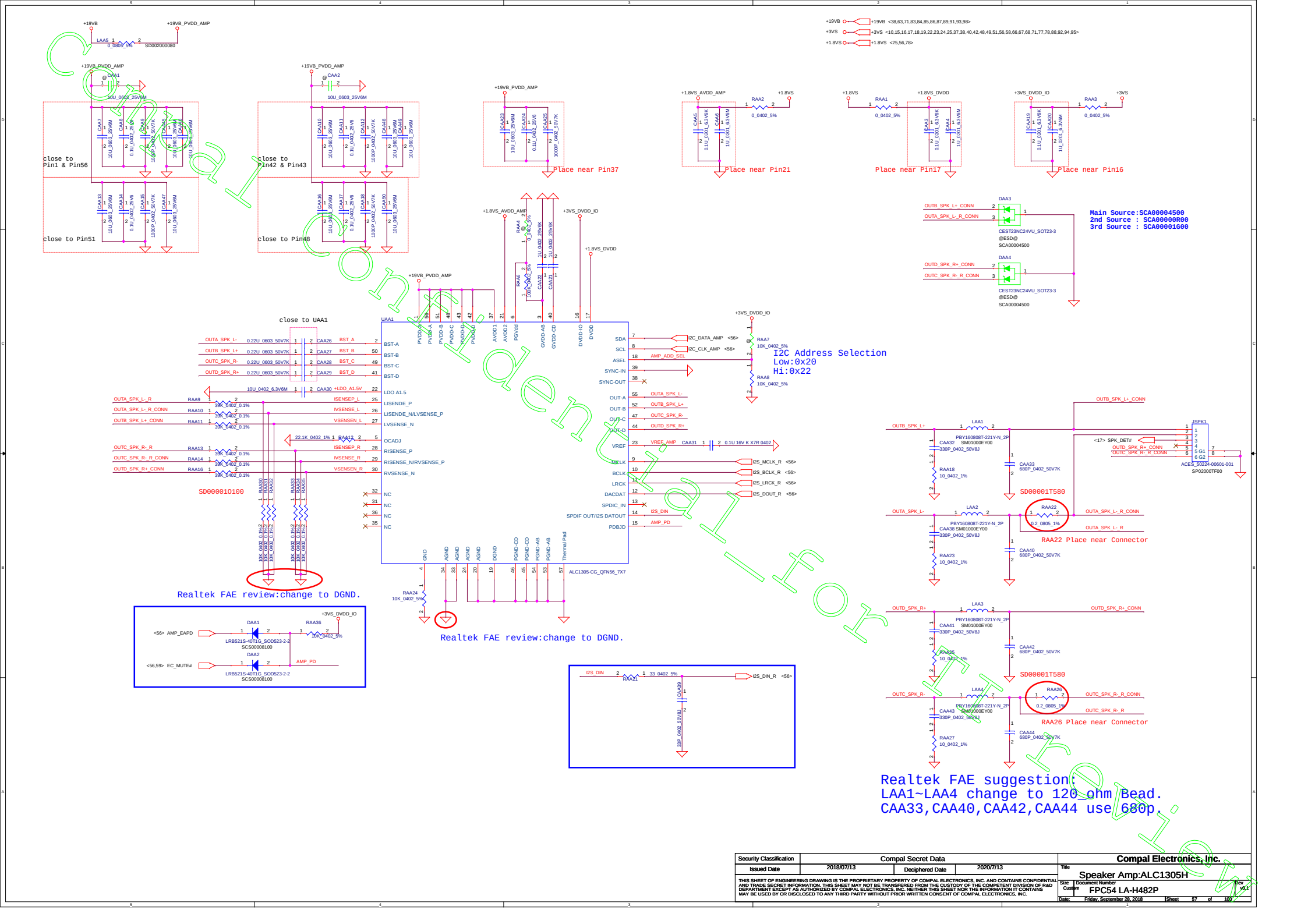

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			Date: Friday, September 28, 2018; Sheet 57 of 100

EC Board ID (DIS, phase) control table

2018 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N17E-G1	33K	43K	56K	75K
R17M-G1-70	100K	130K	160K	200K

2019 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N18P-G0/G1	33K	43K	56K	75K
N18E-G1	100K	130K	160K	200K
R19M-G50-70	240K	270K	330K	430K

2019 OMEN

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N18P-G0/G1	33K	43K	56K	75K
N18E-G1/G2/G3	100K	130K	160K	200K

RH264&CH105 Need use after checking

PIR1.48

PIR2.31

PIR1.29
PIR2.3
PIR4.3

PIR1.38

replace to common part 0108

Need Check

CC144/ RC369 place near EC Side

EMI request

LPC/eSPI & MISC

PWM Output

AD Input

DA Output

PS2 Interface

Int. K/B Matrix

SPI ROM

GPIO

SMBUS

KB9022QD LQFP 128P

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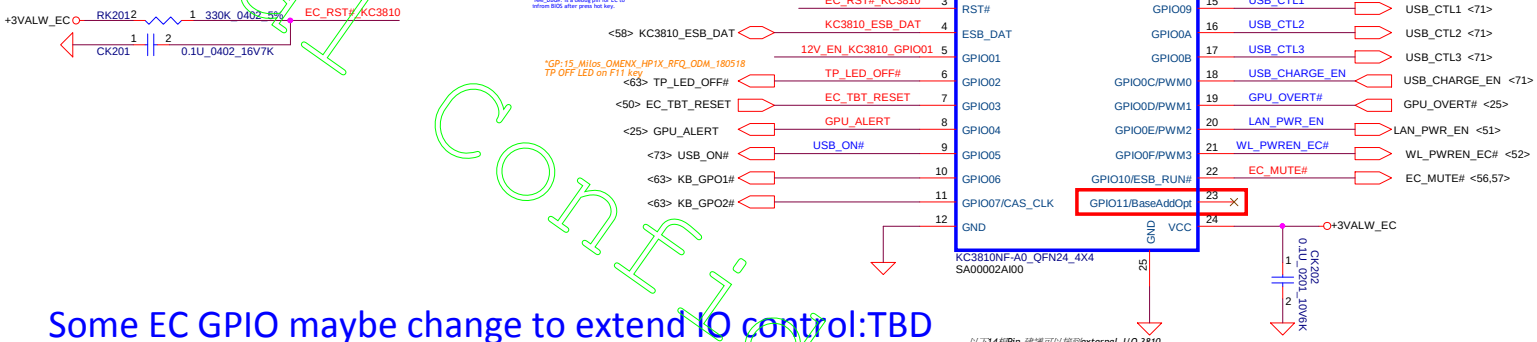
Date: Friday, September 28, 2018 | Sheet 58 of 100

+3VALW_EC
+5VS

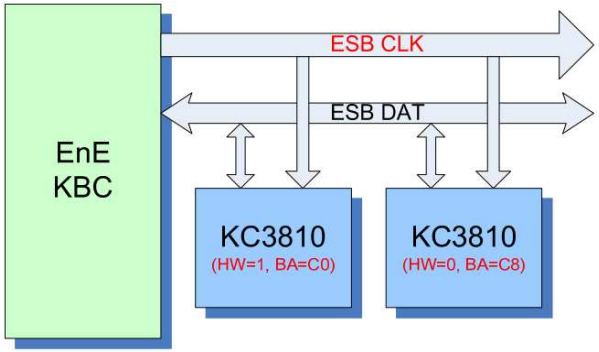
+3VALW_EC <25,58,82>
+5VS <37,38,39,40,56,63,67,78,96>

OMEN New ESB CLK&DAT for Extend I/O

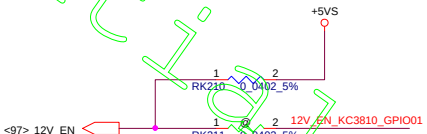
Some EC GPIO maybe change to extend IO control:TBD



Some EC GPIO maybe change to extend IO control:TBD



以下14個Pin 建議可以接到external I/O 3810,
1. USB_CTL1(GPIO4B Pin84),
2. USB_CTL2(GPIO3F Pin72),
3. USB_CTL3(GPIO1D Pin38),
4. USB_CHARGE_EN(GPIO1A Pin36),
5. GPU_OVERT#(GPIO0D Pin19) => DPF50 NO USE
6. LAN_PWR_EN(GPIO4D Pin86),
7. WL_PWREN_EC#(GPIO61 Pin98),
8. DCHG_I(GPIO40 Pin73) => DPF50 NO USE
9. USB_ONH(GPIO37 Pin 121),
10. LED : 5 Pin.



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Date: Friday, September 28, 2018	Sheet 59 of 100		

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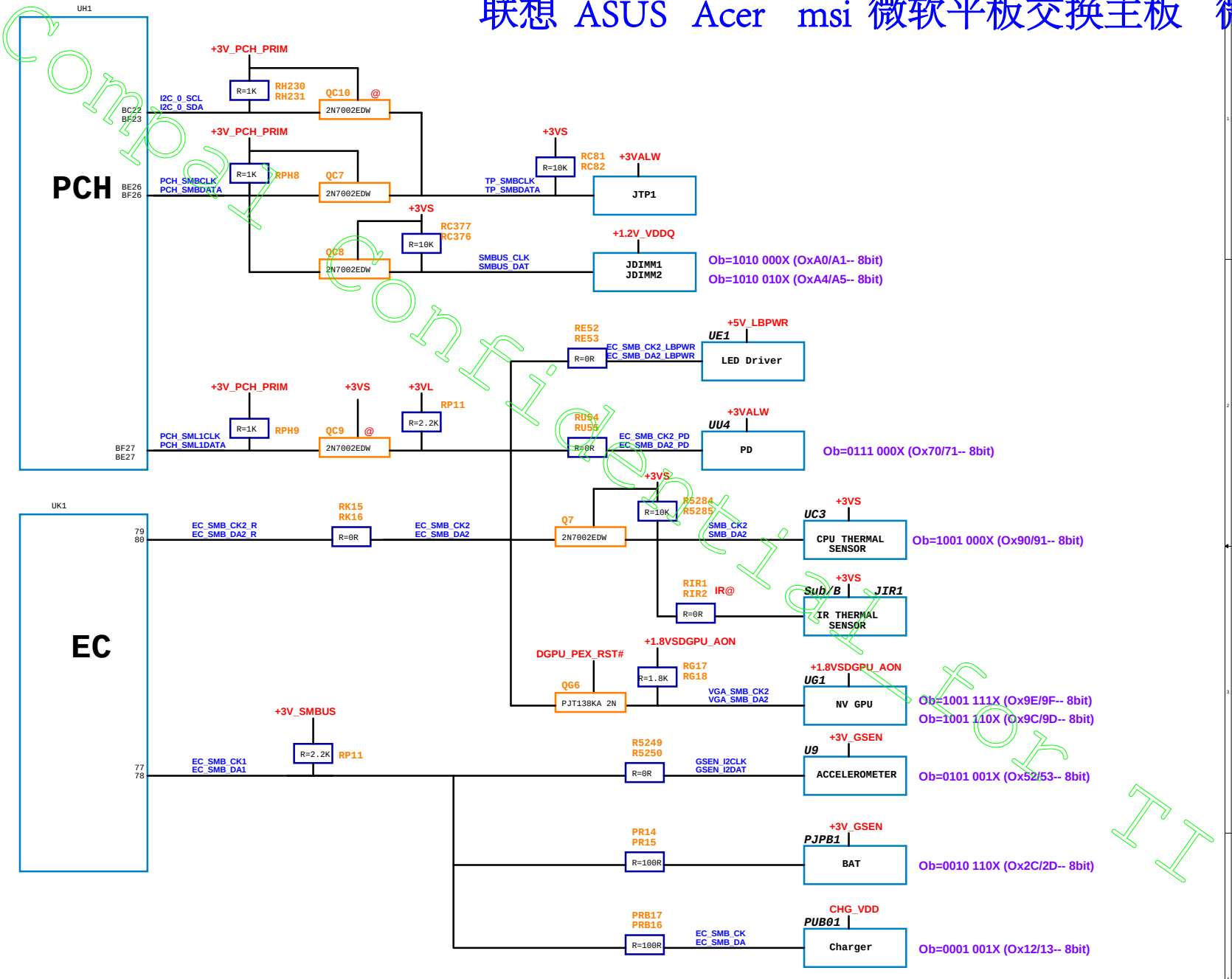
Date: Friday, September 28, 2018	Sheet 60 of 100		



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Compal Electronics, Inc.	
Title	SMBus Block Diagram
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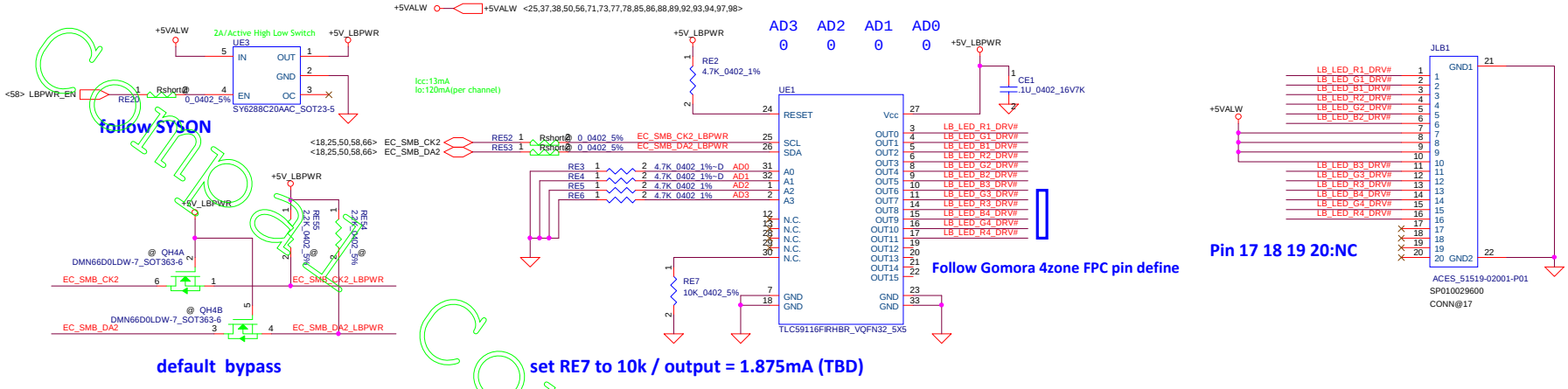
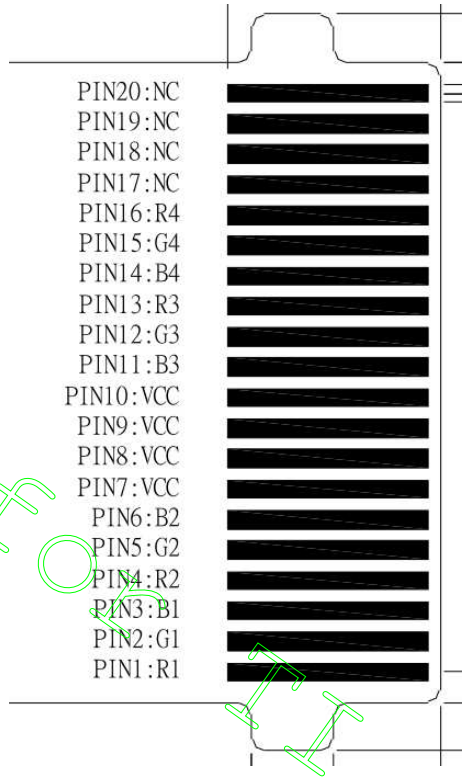
Rev: v0.1	
Date: Friday, September 28, 2018	Sheet 61 of 100





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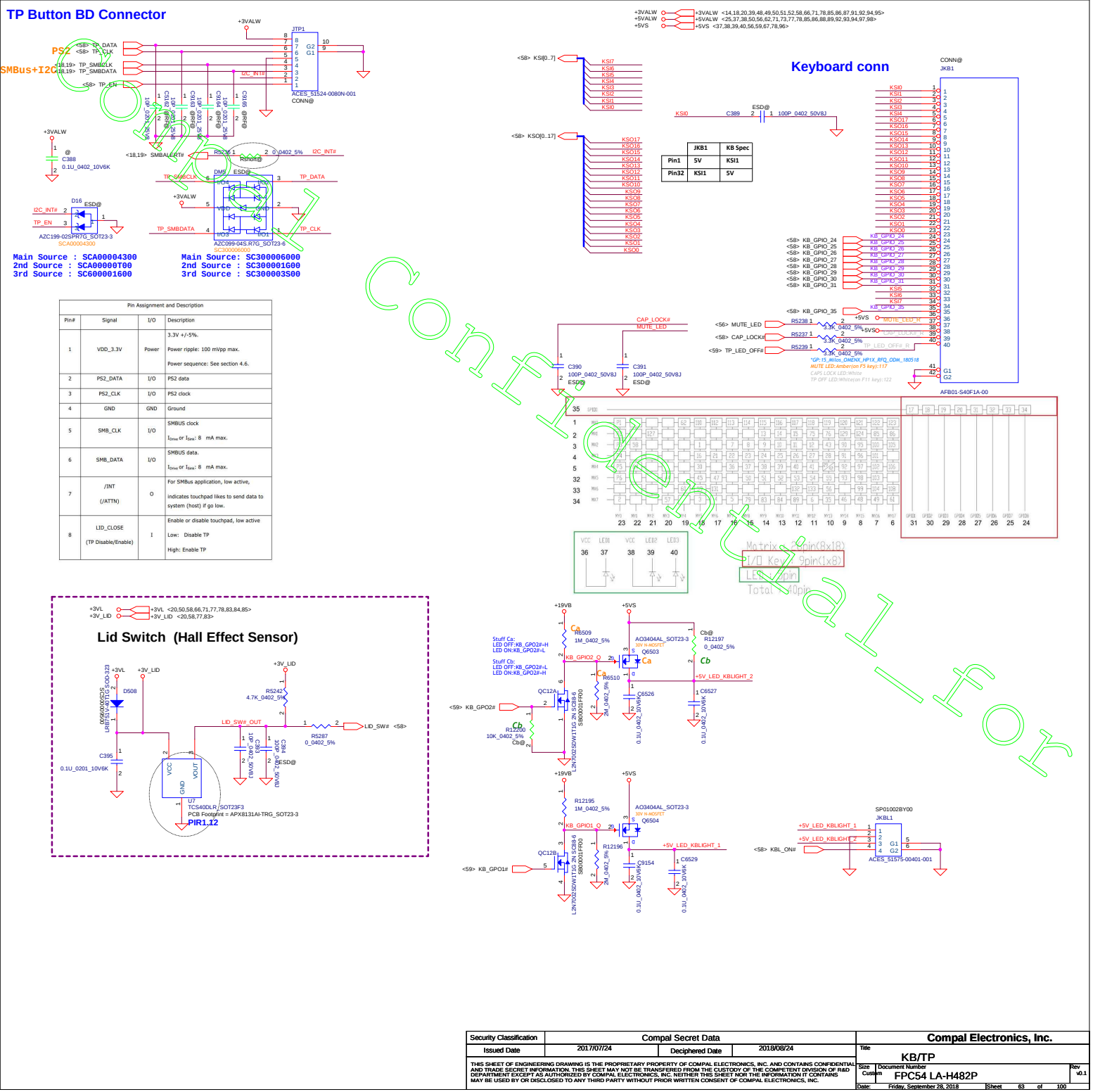
Date:	Friday, September 28, 2018	Sheet	62 of 100



Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock I_{SINK} or I_{SRA}: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. I_{SINK} or I_{SRA}: 8 mA max.
7	/INT (/ATTN)	O	For SMBus application, low active, indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP

JKB1	KB Spec
Pin1	5V	KSI1
Pin32	KSI1	5V

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Date: Friday, September 28, 2018	Sheet 64 of 100		

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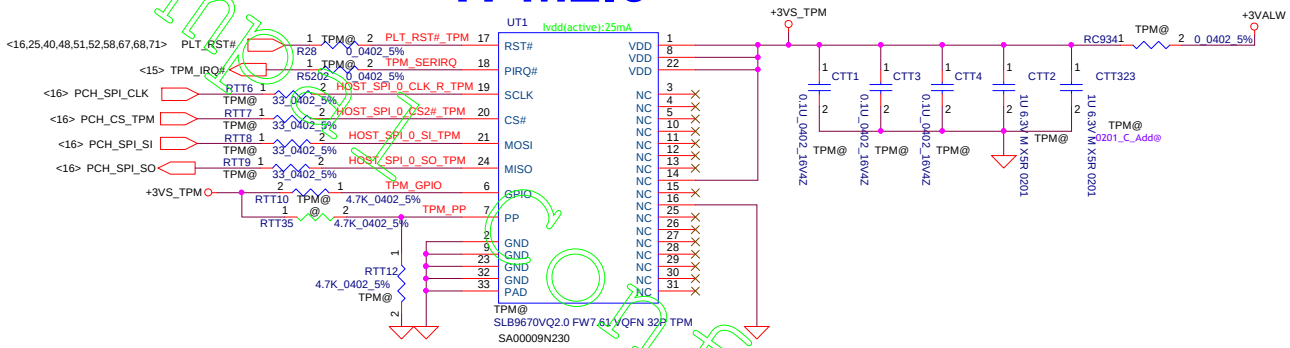
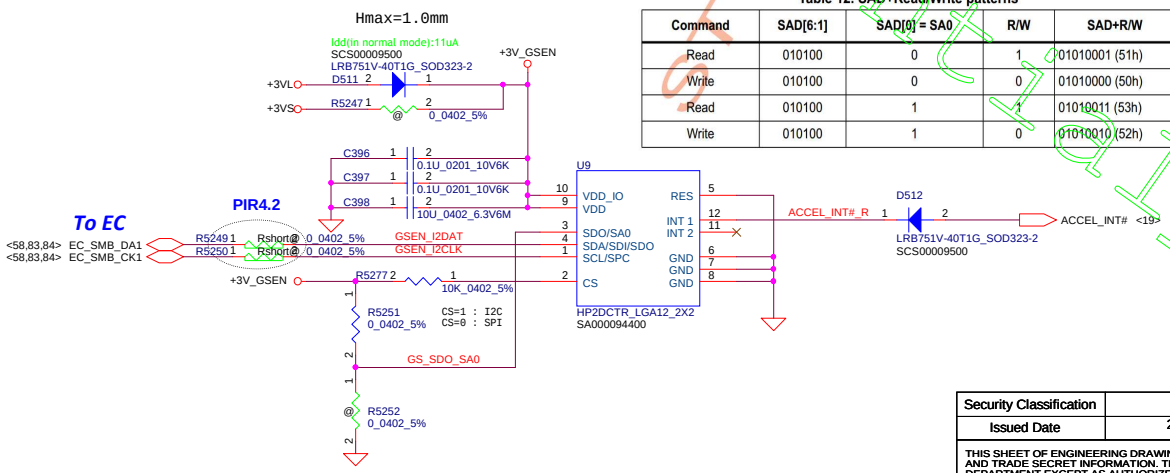
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24
Title	TBD		
Size	Custom	Document Number	FPC54 LA-H482P
Rev	v0.1		
Date:	Friday, September 28, 2018	Sheet	65 of 100

+3VALW <+3VALW <14,18,20,39,48,49,50,51,52,58,63,71,78,85,86,87,91,92,94,95>
+3VS <+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,48,49,51,56,57,58,67,68,71,77,78,88,92,94,95>

TPM2.0



ACCELEROMETER
ST Micro HP2DC

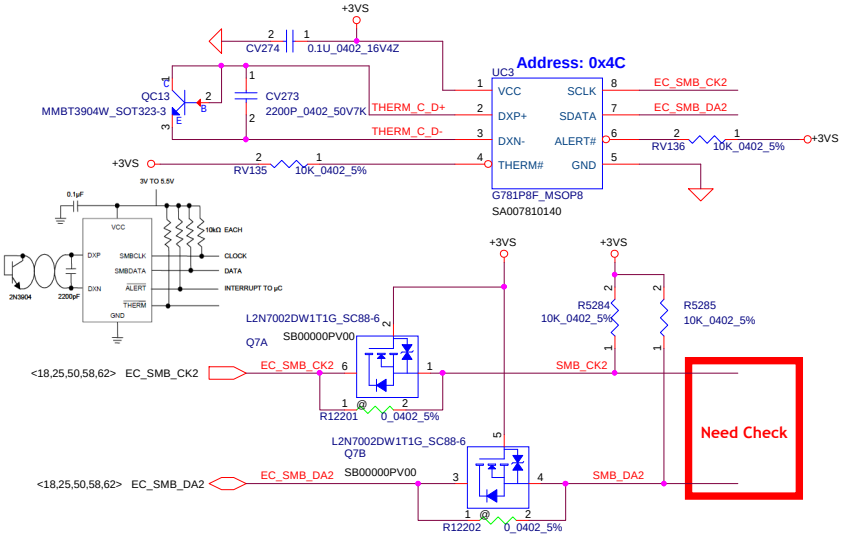


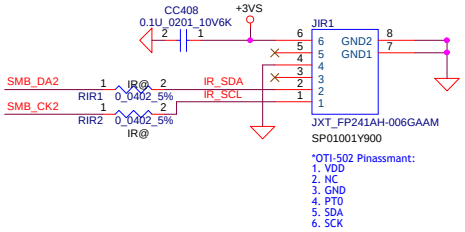
+3VL <+3VL <20,50,58,63,71,77,78,83,84,85>

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

CPU THERMAL SENSOR





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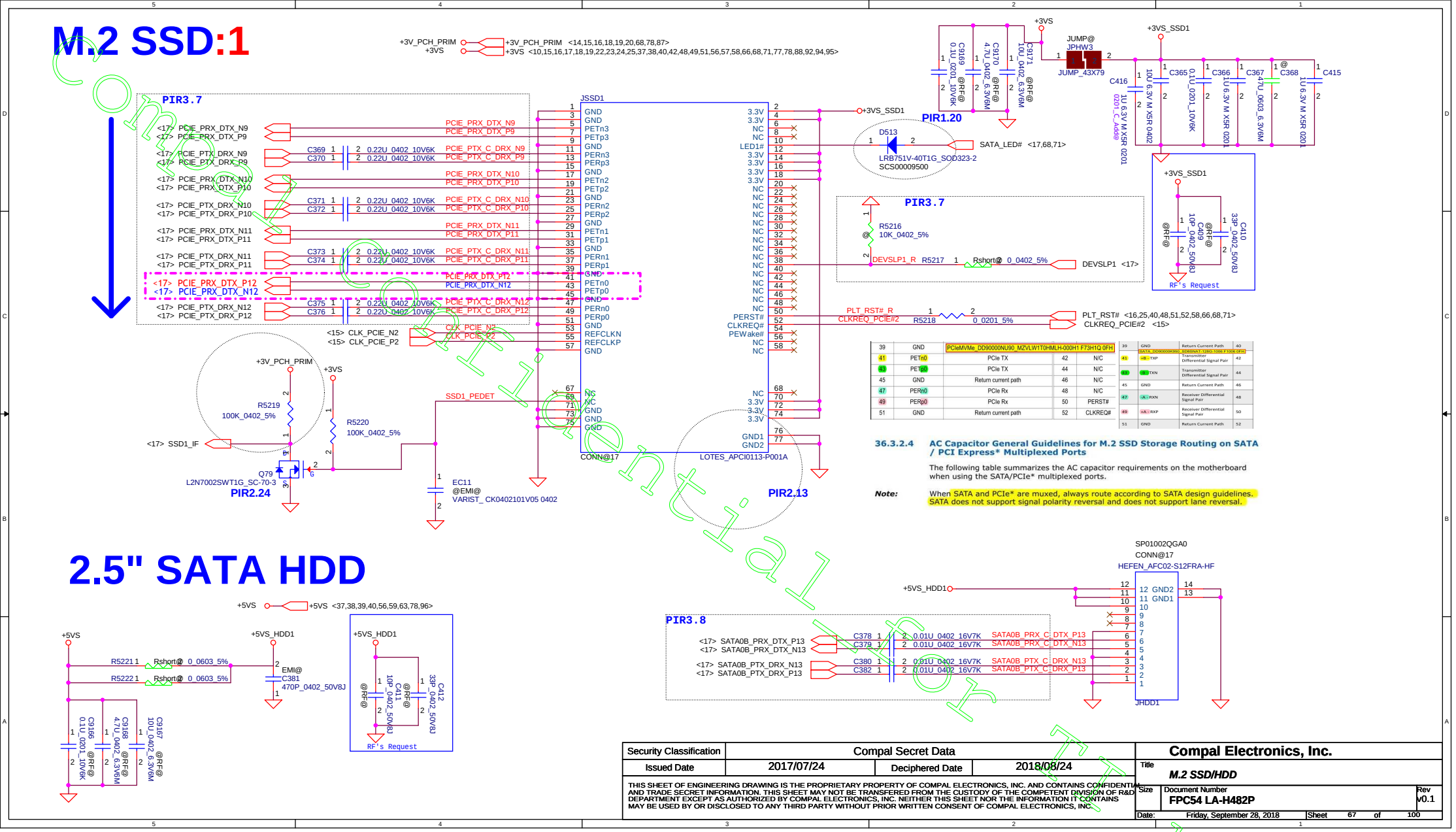
Compal Electronics, Inc.

Title: **TPM&Thermal&G-sensor**

Size	Document Number	Rev
Custom	FPC54 LA-H482P	v0.1

Date: Friday, September 28, 2018 Sheet 66 of 100

M.2 SSD:1



2.5" SATA HDD

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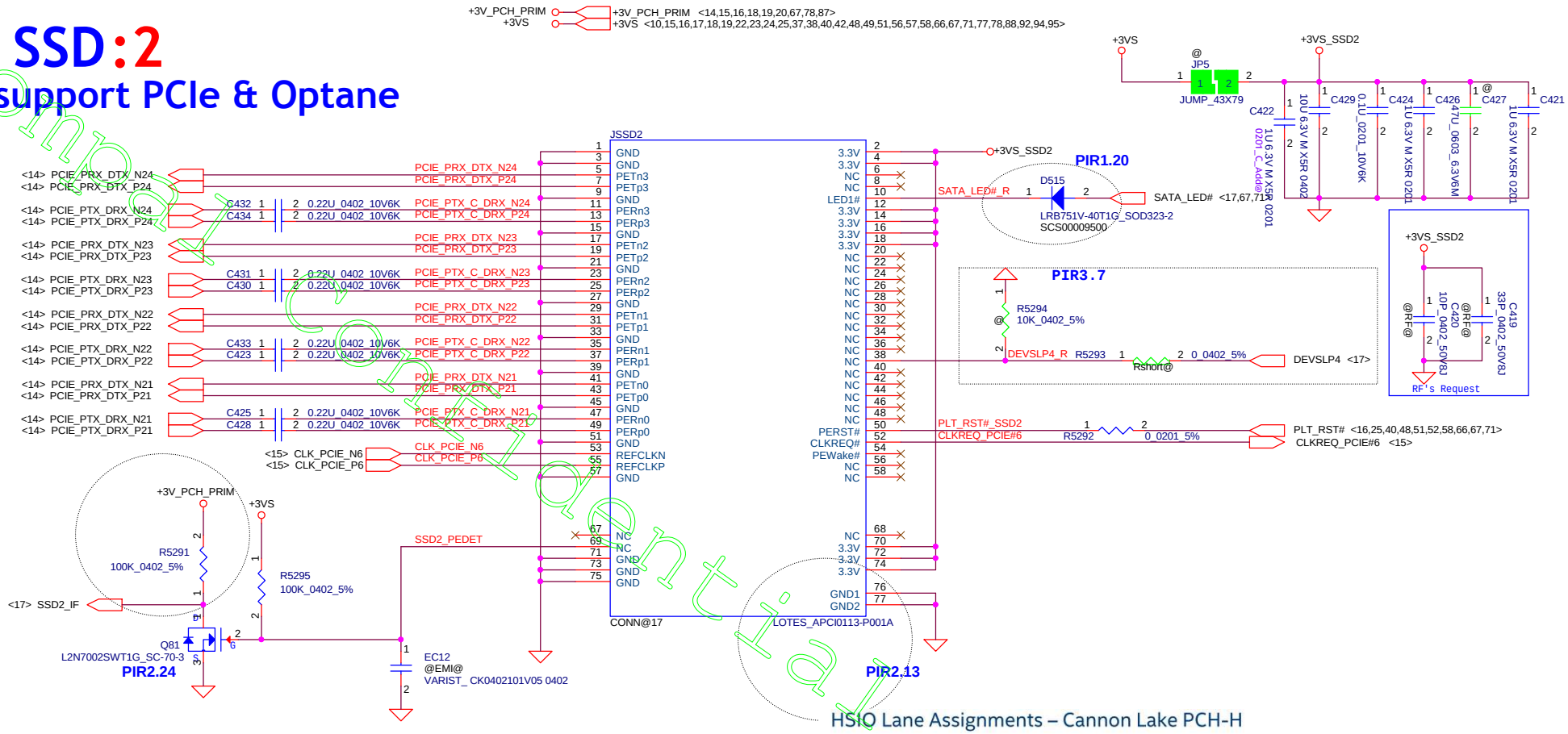
Date: Friday, September 28, 2018 | Sheet 67 of 100

M.2 SSD:2

Only support PCIe & Optane



36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	Return Current Path	40
41	+B TXP	Transmitter Differential Signal Pair	42
43	-B TXN	Transmitter Differential Signal Pair	44
45	GND	Return Current Path	46
47	-A RXN	Receiver Differential Signal Pair	48
49	+A RXP	Receiver Differential Signal Pair	50
51	GND	Return Current Path	52

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

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	FPC54 LA-H482P		v0.1
Date:	Friday, September 28, 2018	Sheet	68 of 100

TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 69 of 100		

TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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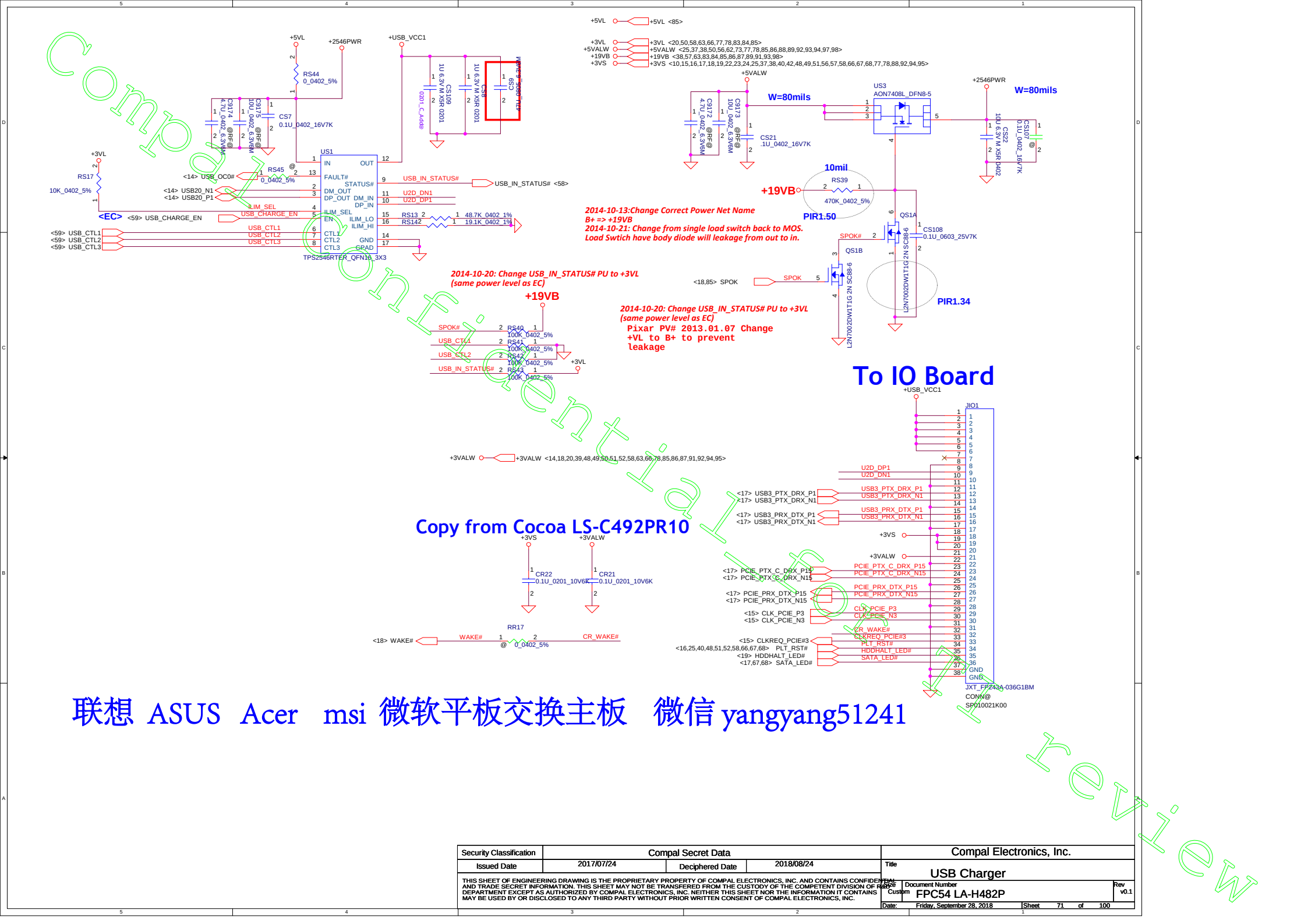
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 70 of 100		



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Date: Friday, September 28, 2018 | Sheet 71 of 100

TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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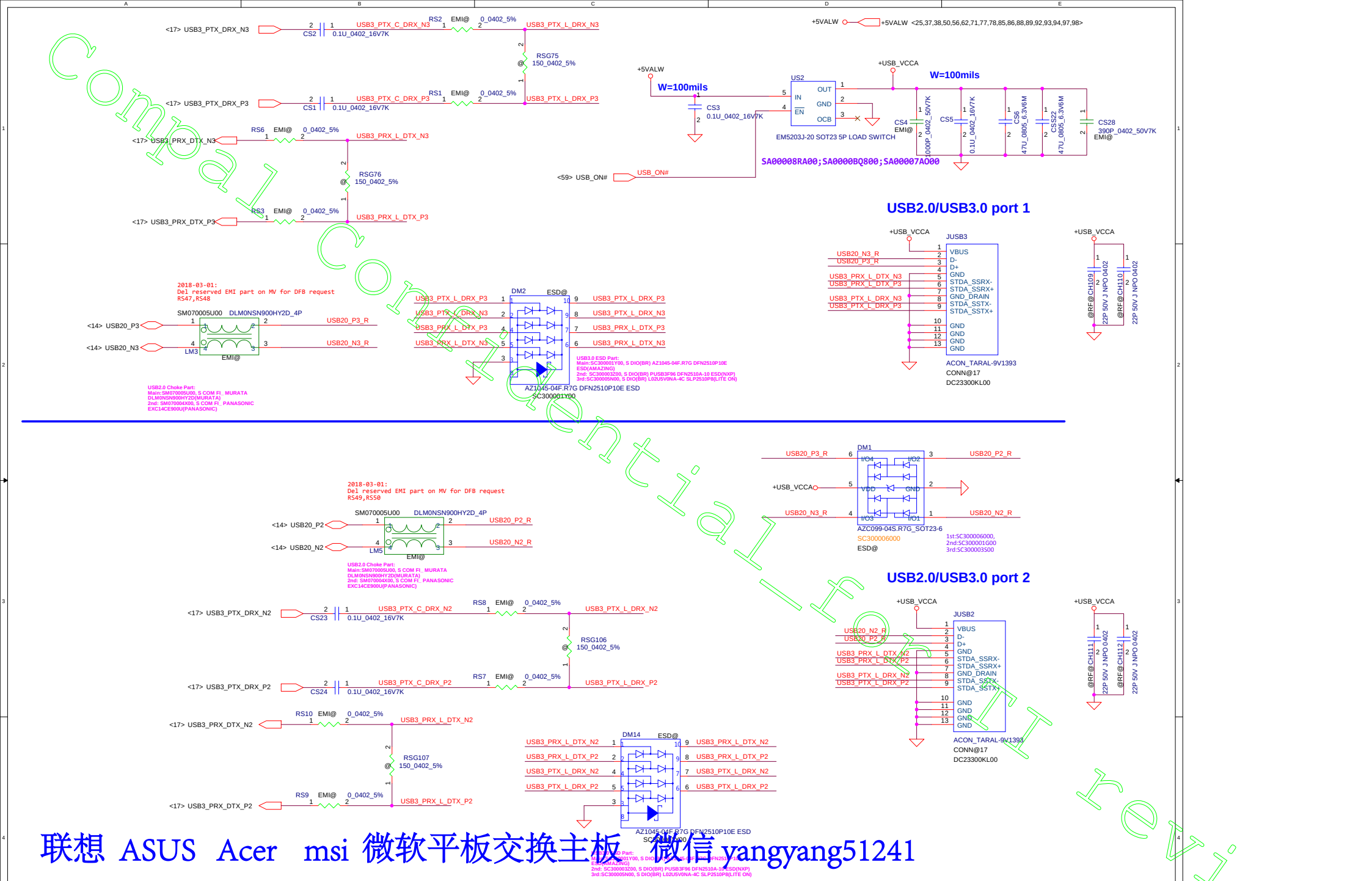
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 72 of 100		



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Title: USB 3.0/2.0 conn

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Date: Friday, September 28, 2018 | Sheet 73 of 100

TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24
Title	TBD		
Size	Custom	Document Number	FPC54 LA-H482P
Rev	v0.1		
Date:	Friday, September 28, 2018	Sheet	74 of 100

TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 75 of 100		

TBD: Empty Page

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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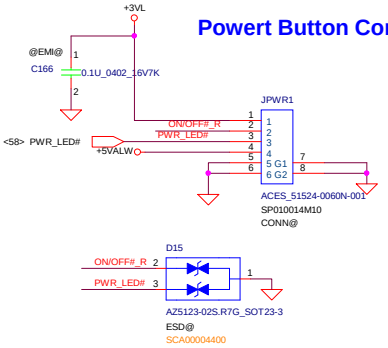
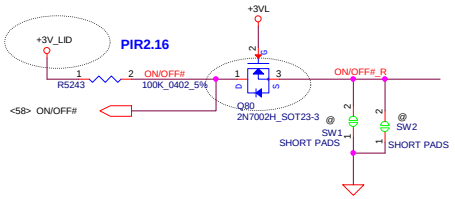
Date: Friday, September 28, 2018	Sheet 76 of 100		

+3V_LID <20,58,63,83>
+3VL <20,50,58,63,66,71,78,83,84,85>
+5VALW <25,37,38,50,56,62,71,73,78,85,86,88,89,92,93,94,97,98>
+12VS <97>
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,48,49,51,56,57,58,66,67,68,71,78,88,92,94,95>

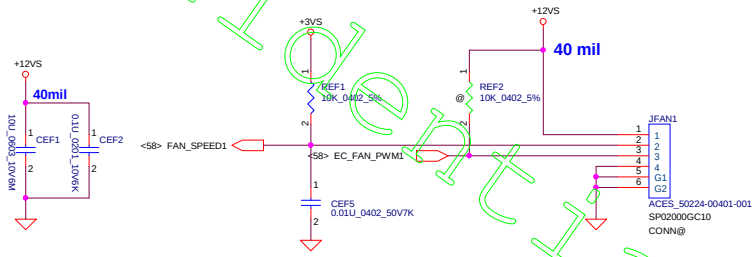
Powert Button Connector



Main Source : SCA00004400
2nd Source : SCA00001B00
3rd Source : SCA00003400



FAN1 conn



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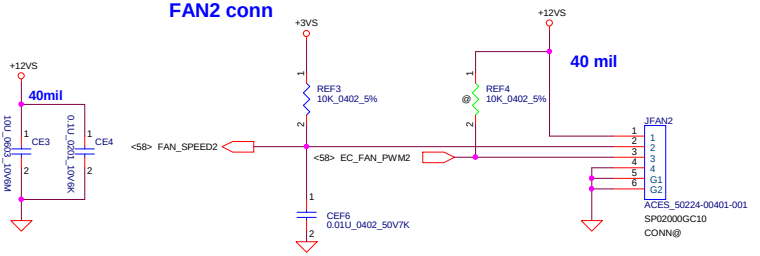
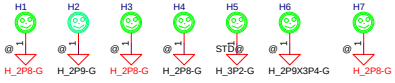
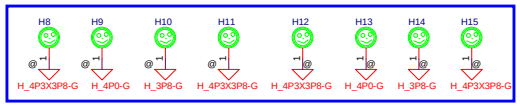
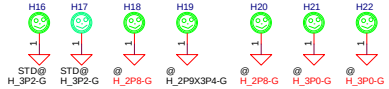


Screw Hole



CPU/GPU bracket





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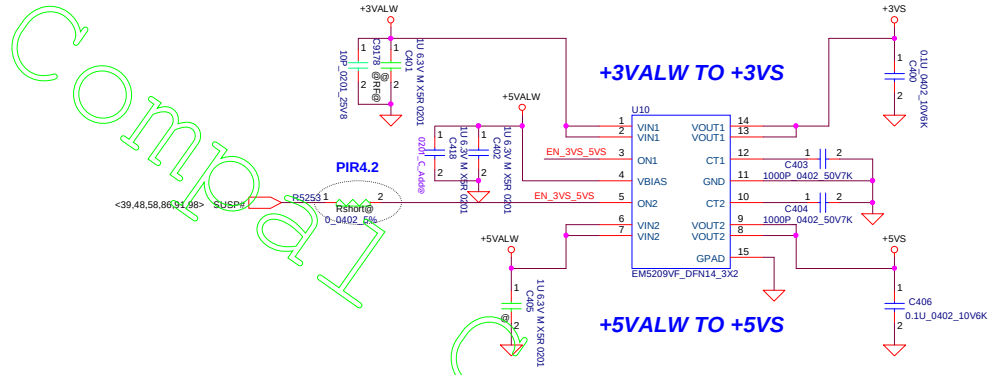
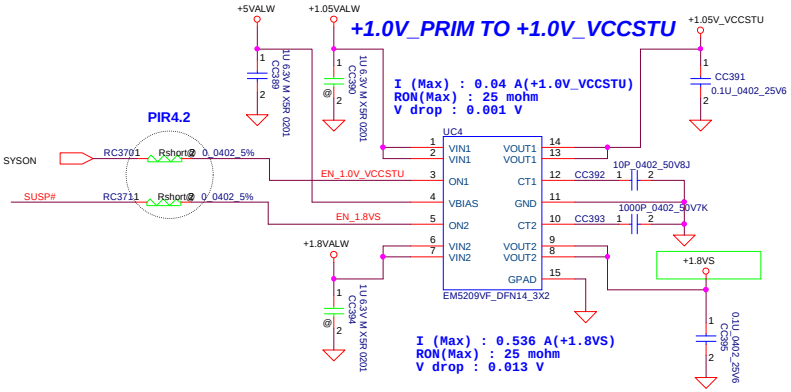
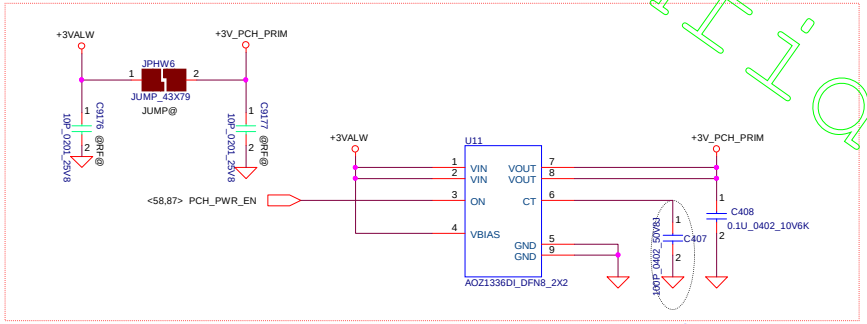
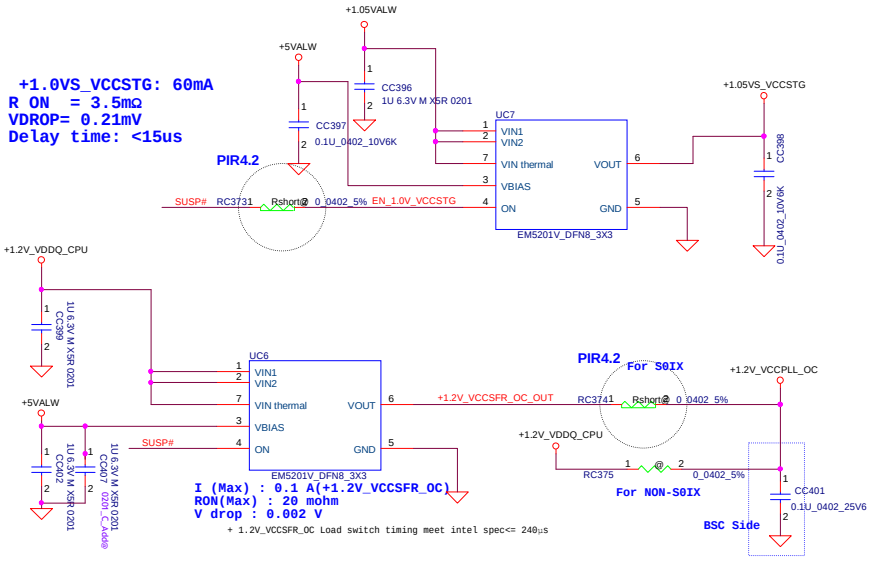
Date: Friday, September 28, 2018	Sheet 77 of 100	

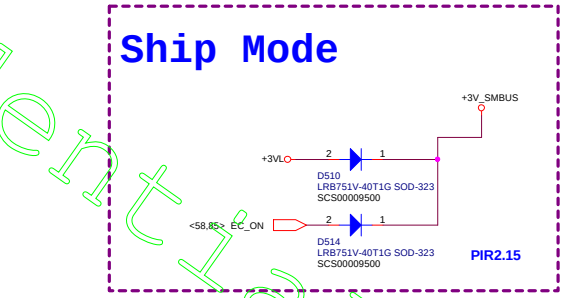


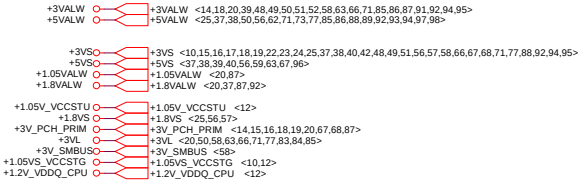




+1VALW TO +1.0VS_VCCSTG







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Rev	v0.1
Date: Friday, September 28, 2018	Sheet 78 of 100

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24
Title	TBD		
Size	Custom	Document Number	FPC54 LA-H482P
Rev	v0.1		
Date:	Friday, September 28, 2018	Sheet	79 of 100

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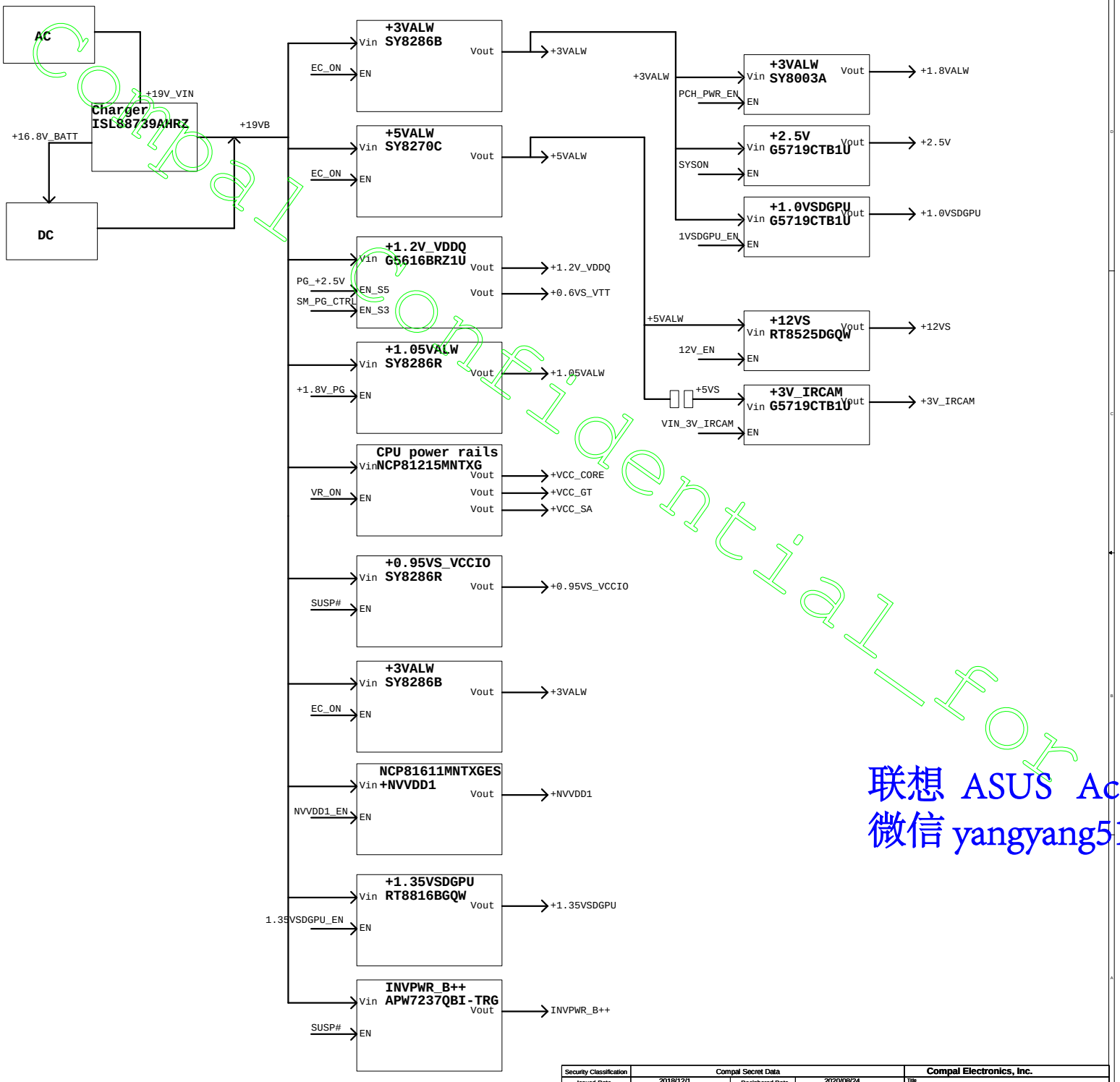
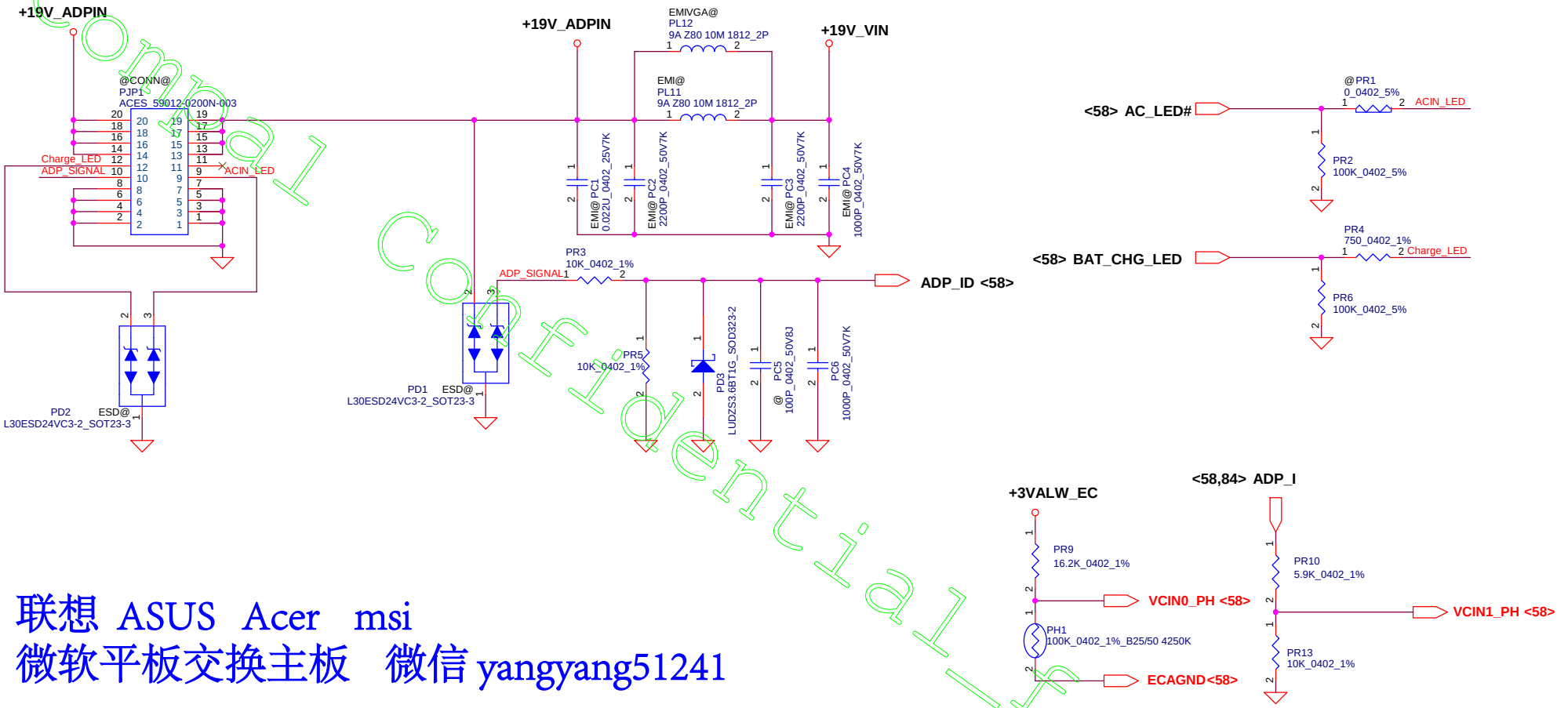
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 80 of 100		



Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.			
Title	Power Block Diagram		
Size	Document Number		Rev 0.1
Date: Friday, September 28, 2018		Sheet 61 of 100	



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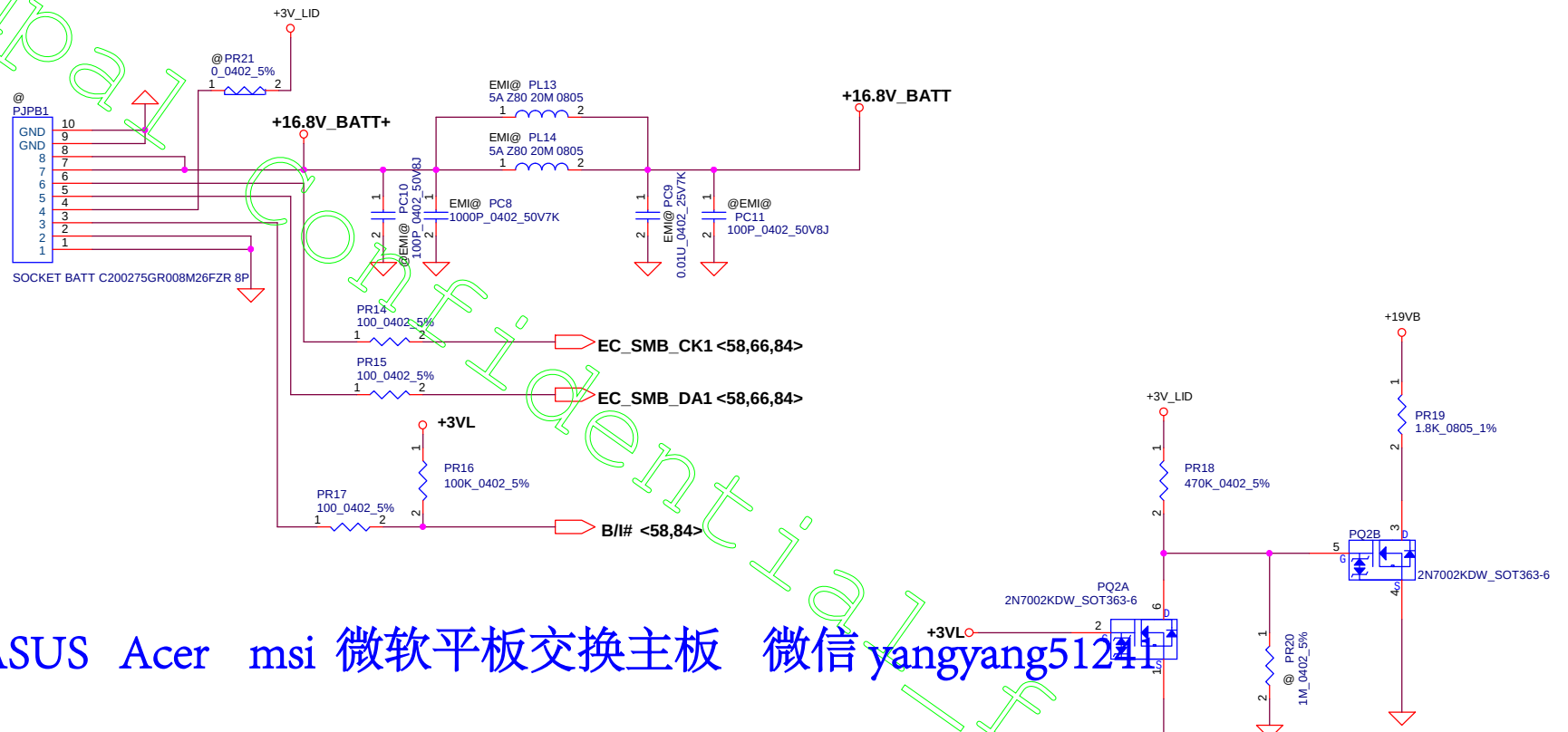
Title	DC Conn		
Size	Document Number		Rev 0.1
Date:	Friday, September 28, 2018	Sheet	82 of 100



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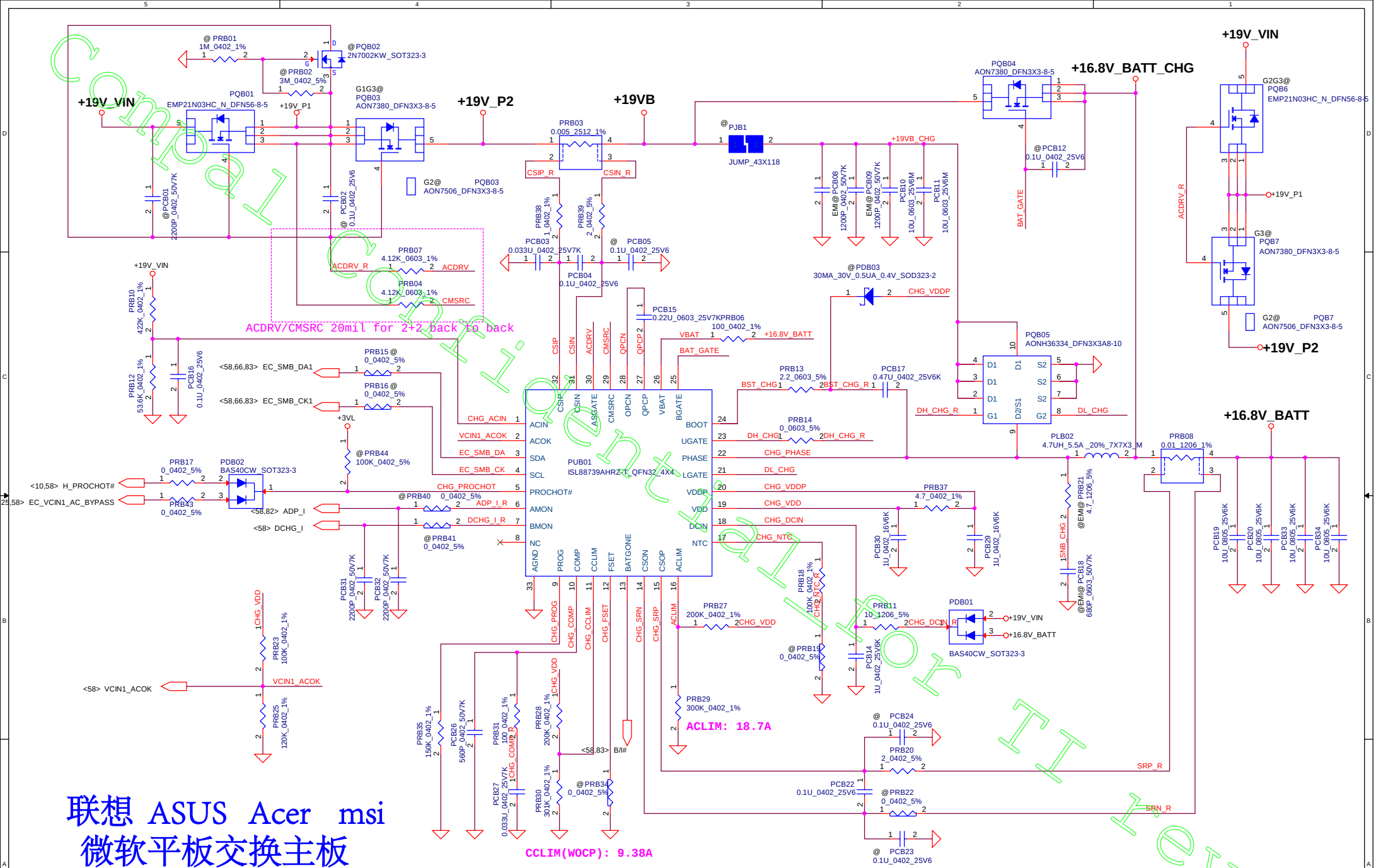
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: BATT Conn

Size: | Document Number: | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 83 of 100



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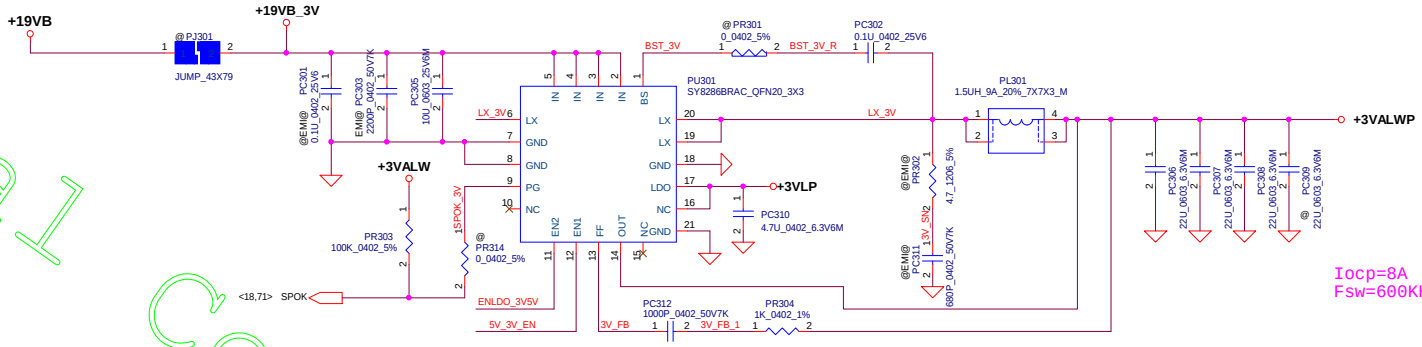
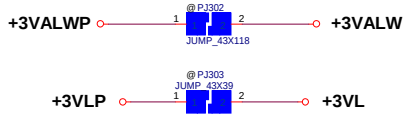
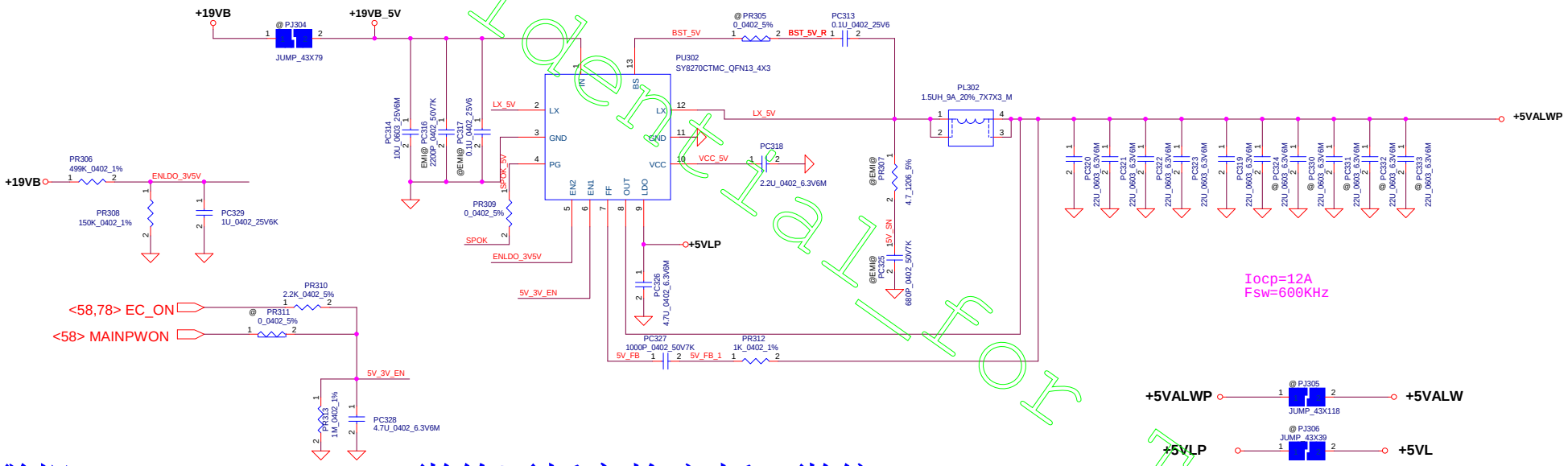
Size	Custom
Document Number	
Rev	0.1
Date:	Friday, September 28, 2018
Sheet	84 of 100







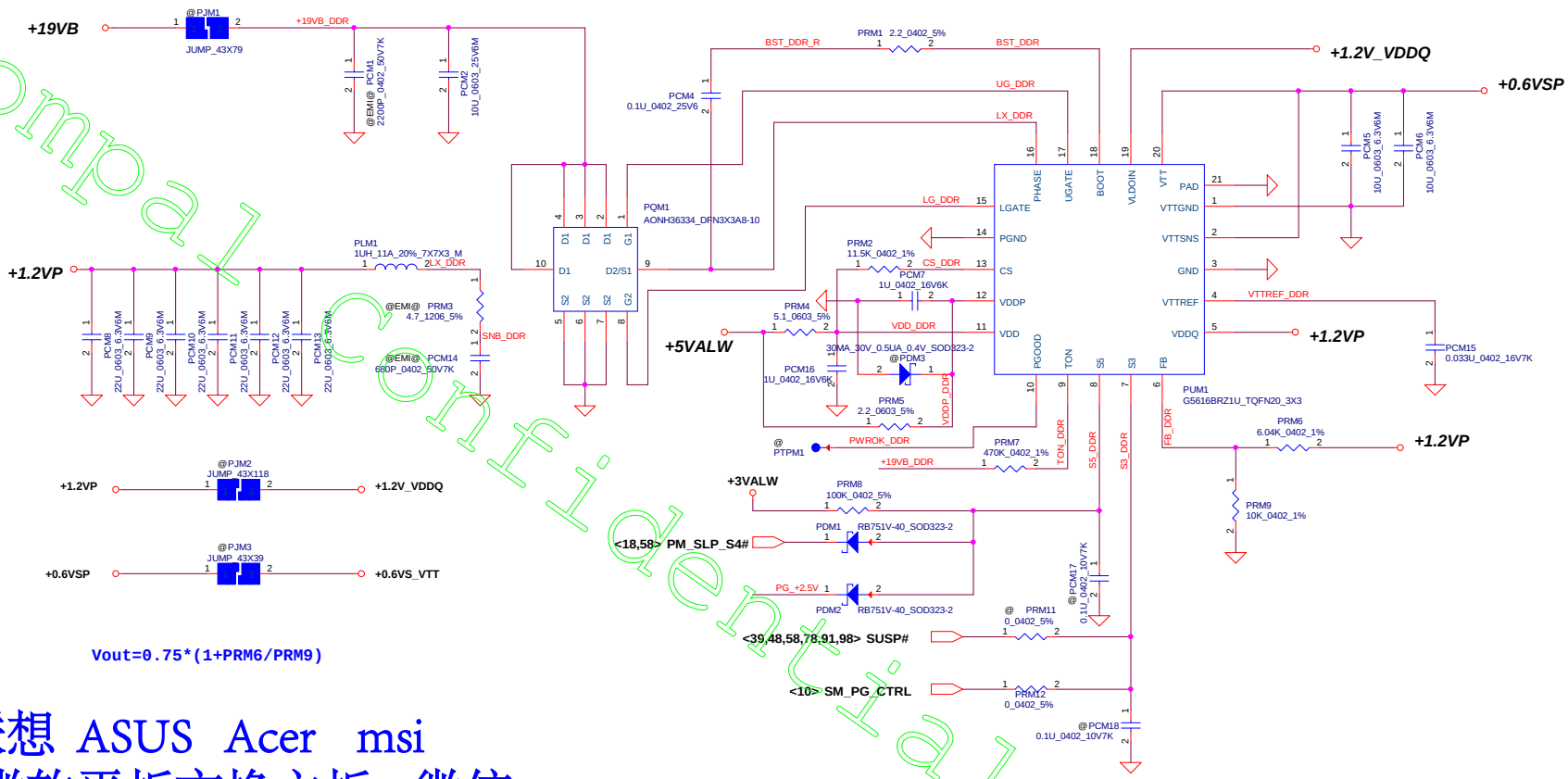
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 85 of 100



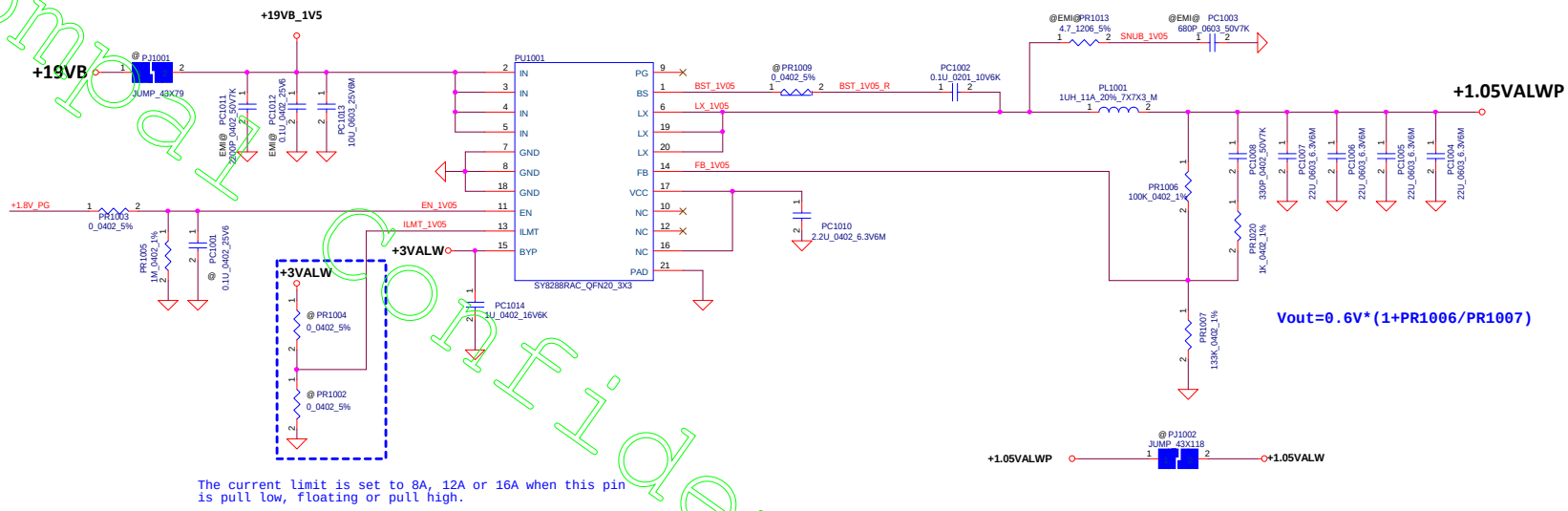
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 86 of 100



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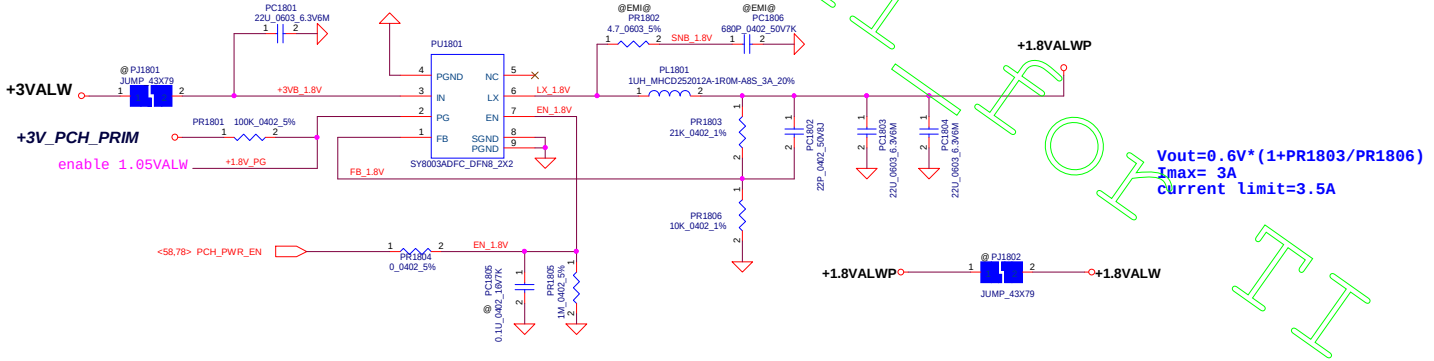
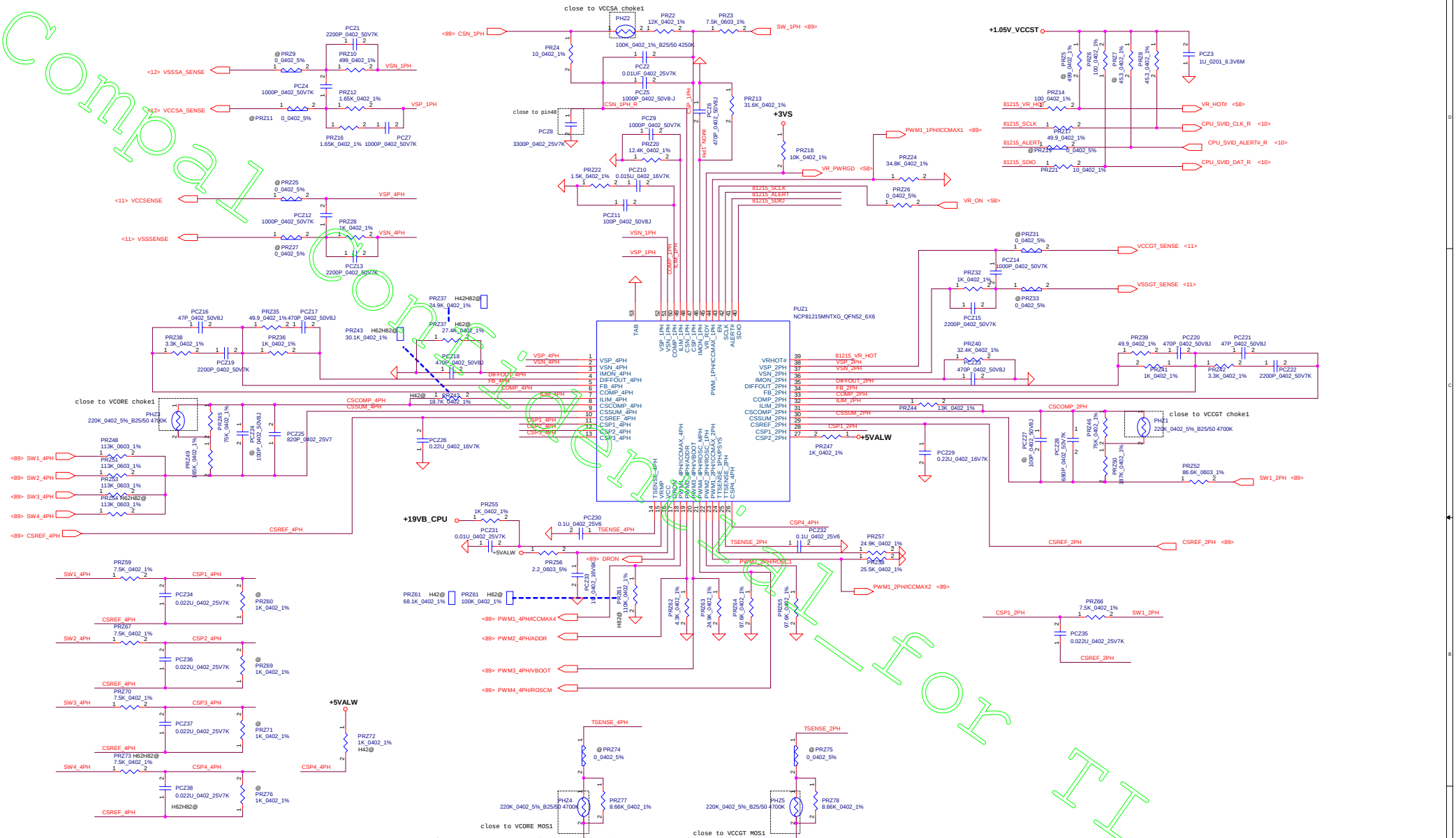


Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.	
Title	1.05V/1.8V
Size C	Document Number
Rev 0.1	
Date: Friday, September 28, 2018	Sheet 87 of 100



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Issued Date	2018/12/1	Deciphered Date 2020/08/24	Title: VCORE
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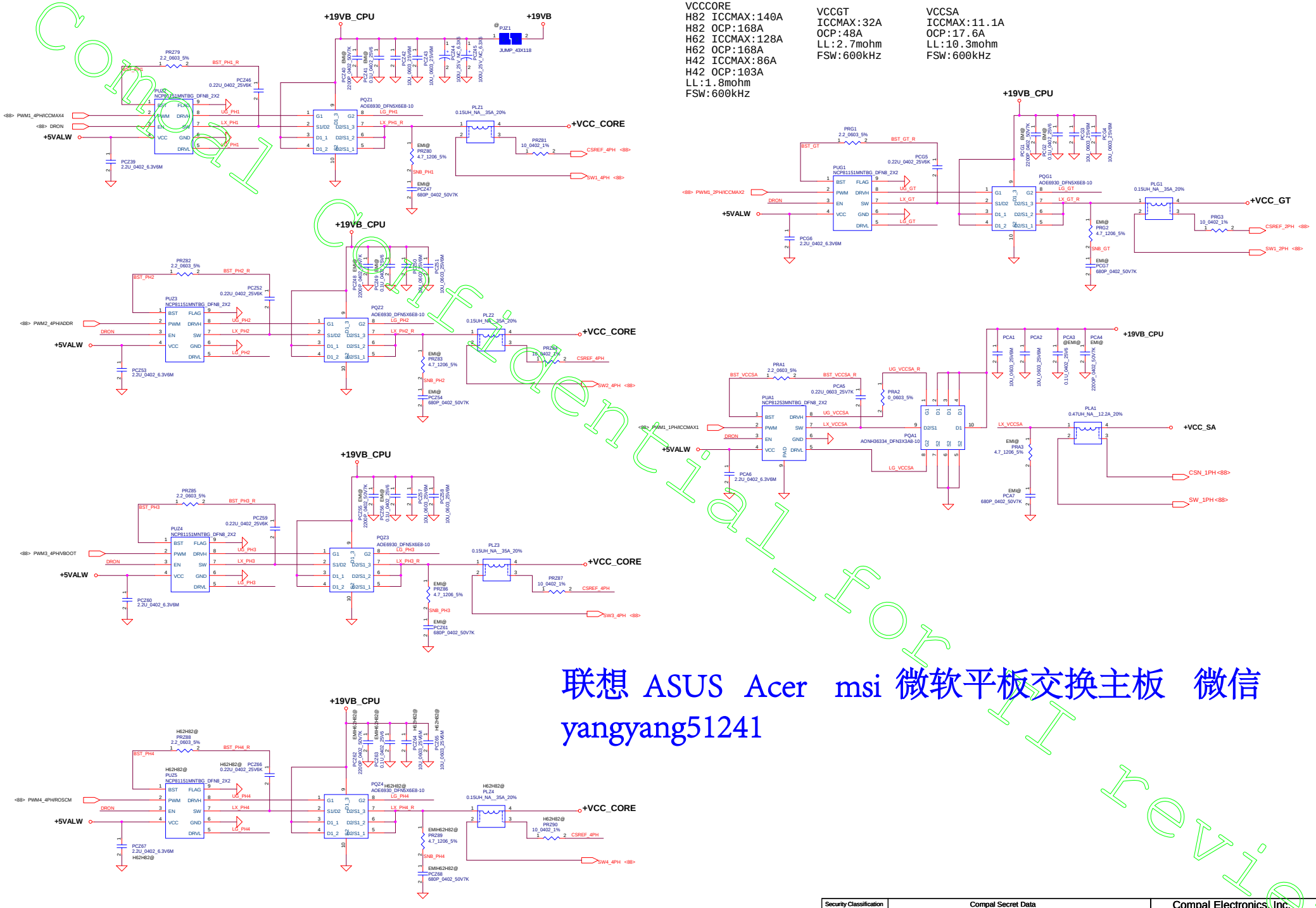
			Date: Friday, September 28, 2018; Sheet 88 of 100


VCCCORE
H82 ICCMAX:140A
H82 OCP:168A
H62 ICCMAX:128A
H62 OCP:168A
H42 ICCMAX:86A
H42 OCP:103A
LL:1.8mohm
FSW:600kHz
VCCGT
ICCMAX:32A
OCP:48A
LL:2.7mohm
FSW:600kHz
VCCSA
ICCMAX:11.1A
OCP:17.6A
LL:10.3mohm
FSW:600kHz
+19VB_CPU
+19VB
+VCC_CORE
+VCC_GT
+VCC_SA
+5VALW
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2020/08/24
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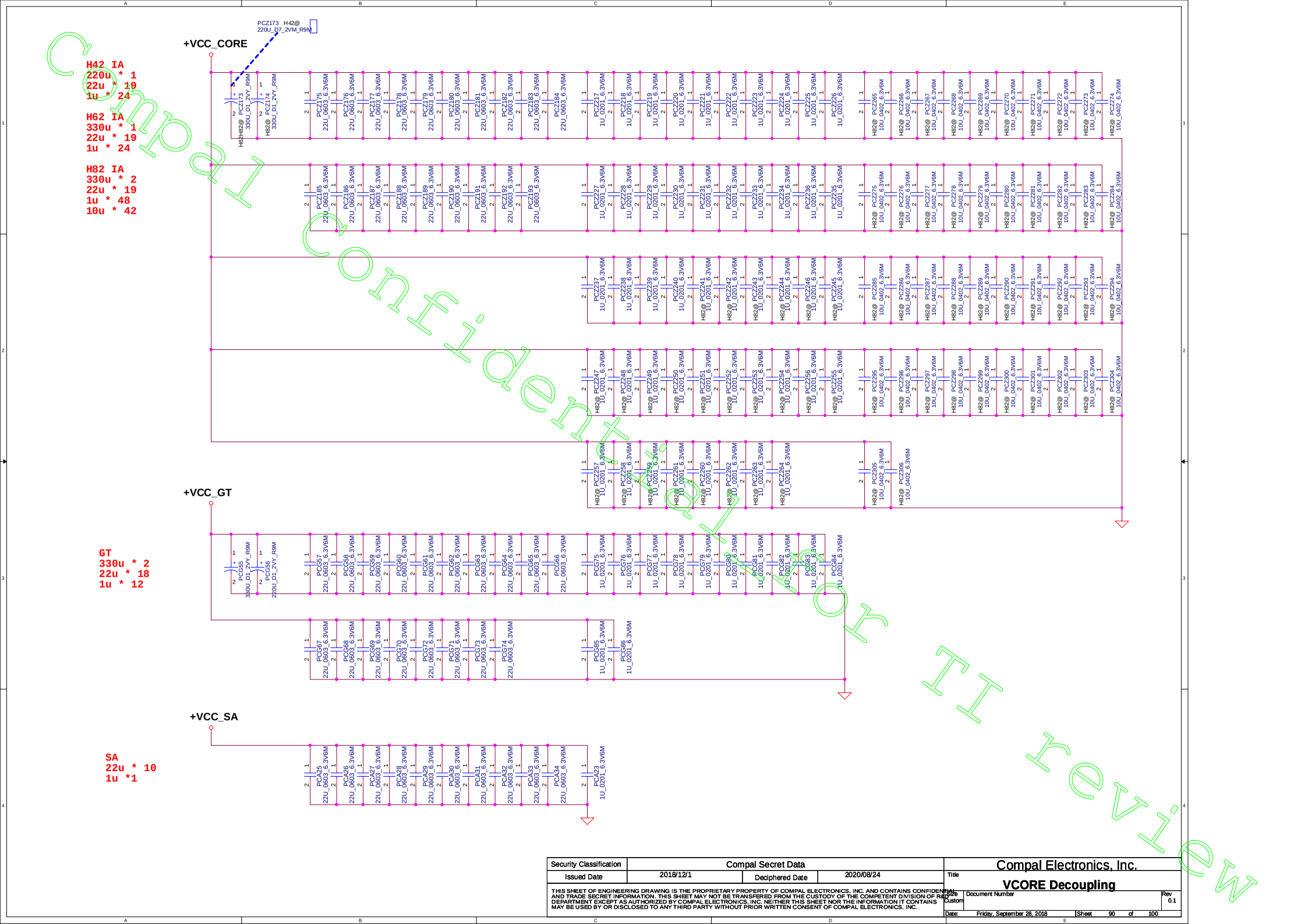
VCORE SW
Friday, September 28, 2018



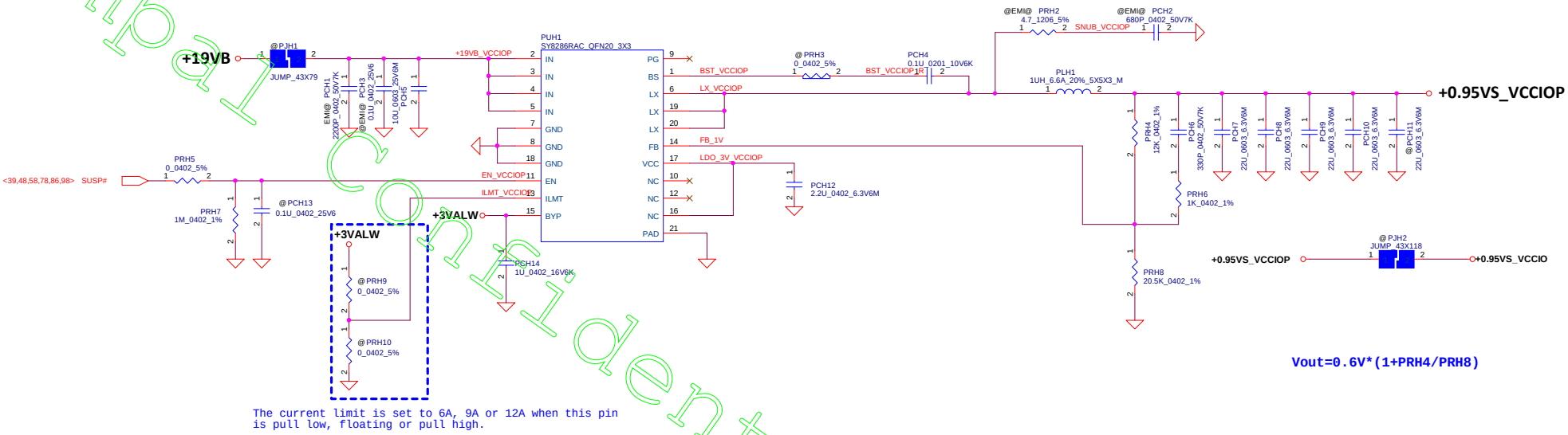
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: VCORE Decoupling

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 90 of 100



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Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Title: VCCIO

Size	Document Number	Rev
Custom		0.1

Date: Friday, September 28, 2018 Sheet 91 of 100

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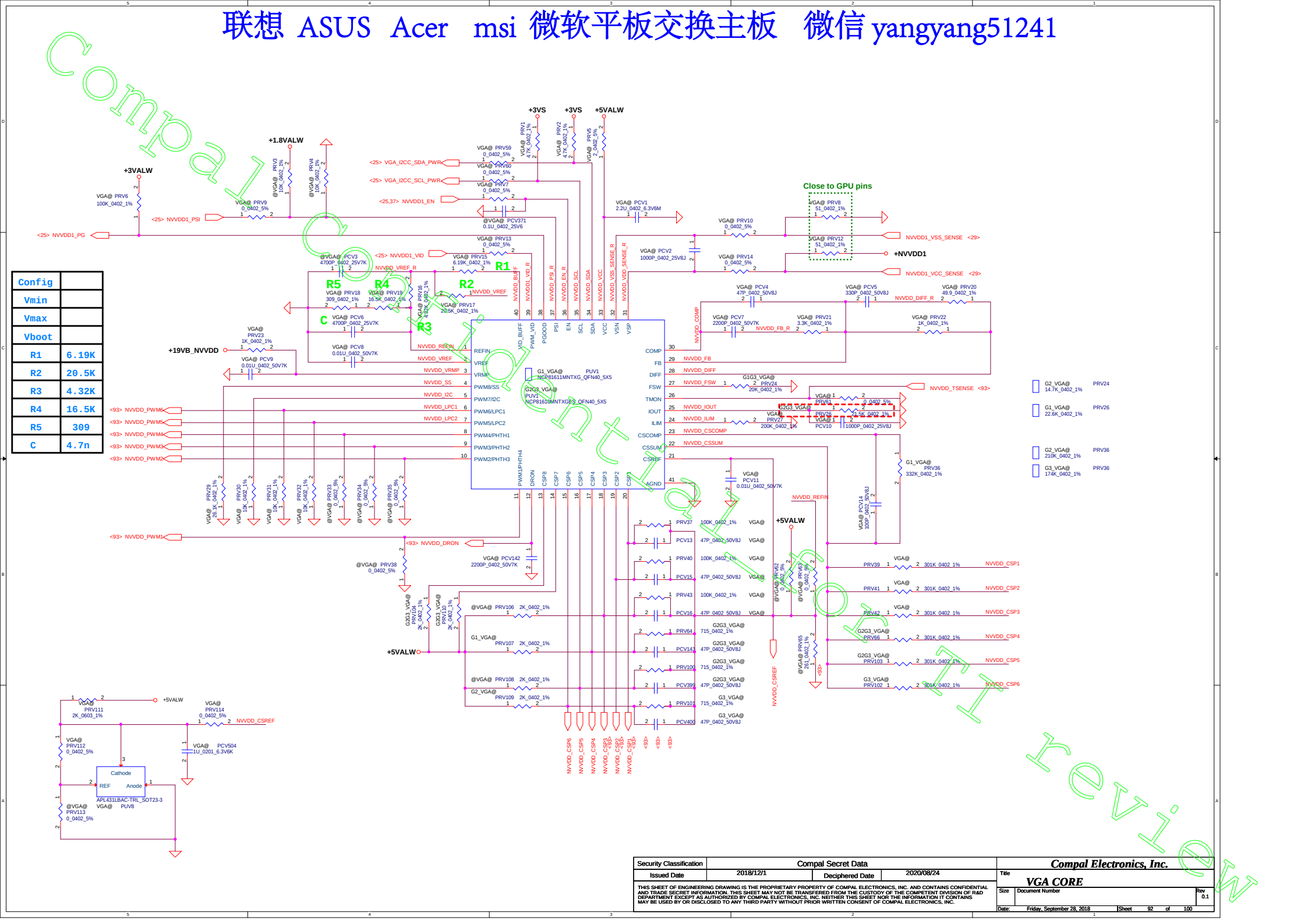


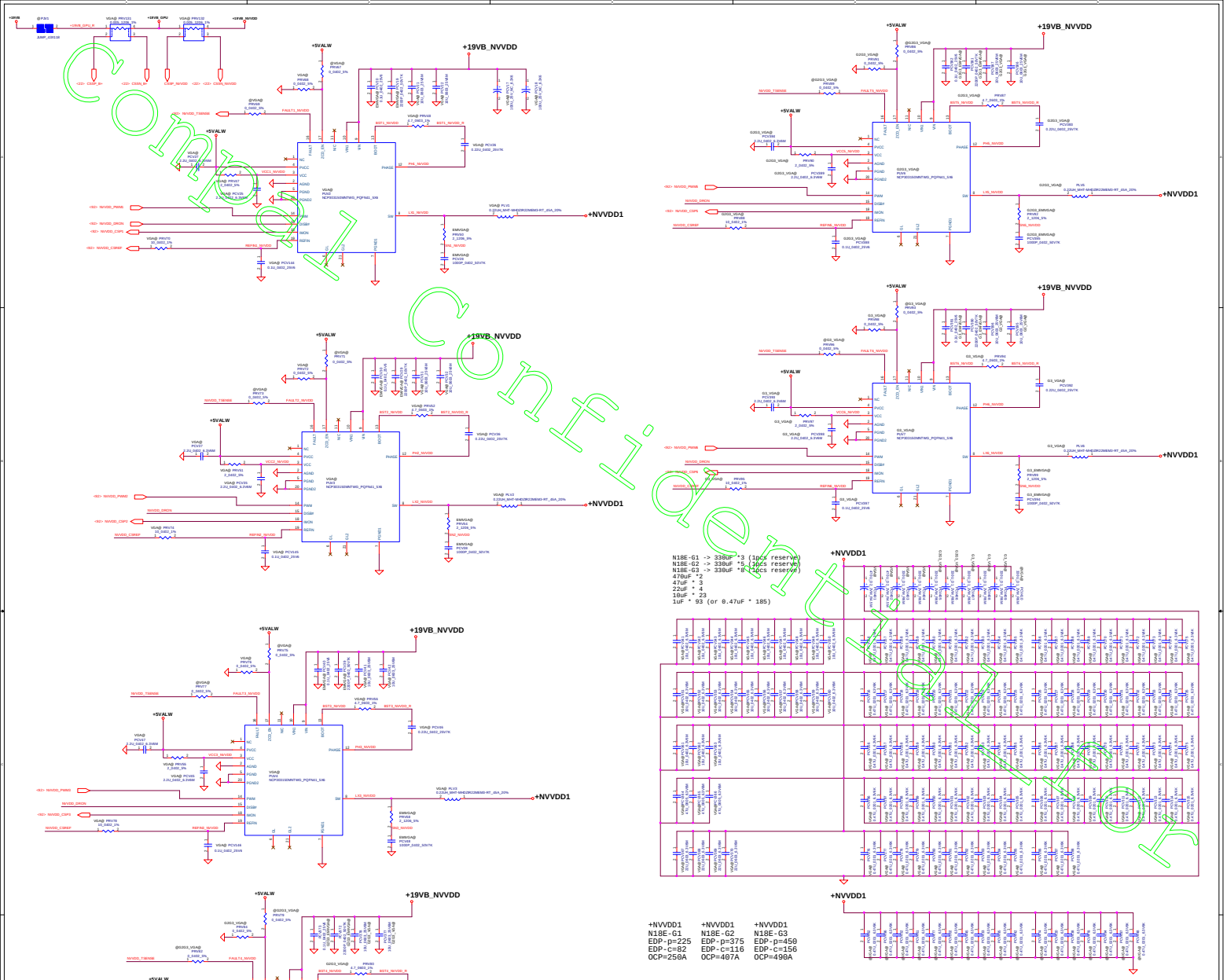
Security Classification	Compal Secret Data
Issued Date	2018/12/1
Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: VGA CORE

Size | Document Number | Rev 0.1

Date: Friday, September 28, 2018 | Sheet 92 of 100



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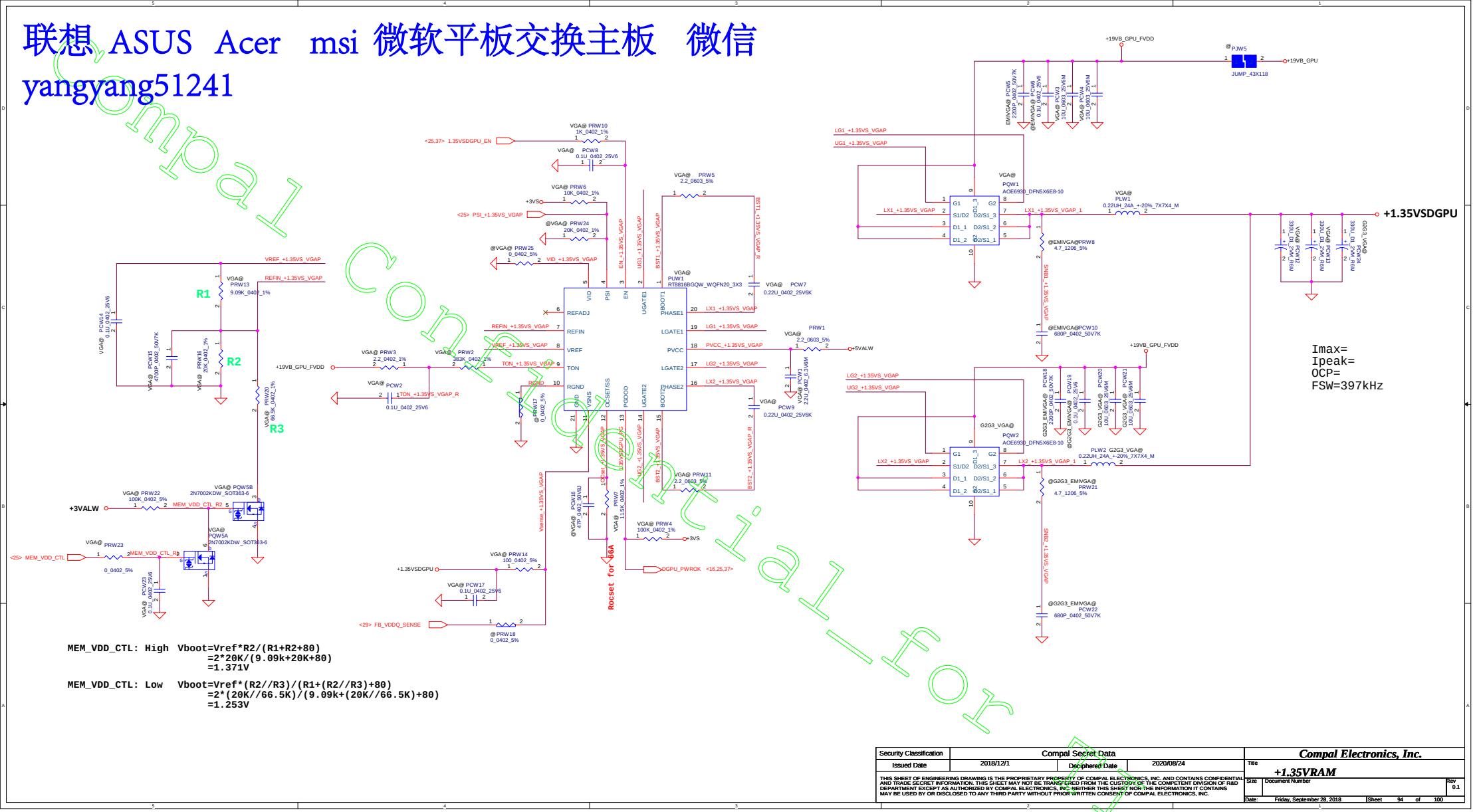
Issued Date	2010/12/1	Deciphered Date	2020/09/04
			Title: VGA CORE SW/DECOUPLING
			Size: Document Number: Rev: 0.4
			Date: Friday, September 04, 2015 Sheet: 53 of 55



Imax=
Ipeak=
OCP=
FSW=397kHz

MEM_VDD_CTL: High Vboot=Vref*R2/(R1+R2+80)
=2*20K/(9.09k+20K+80)
=1.371V

MEM_VDD_CTL: Low Vboot=Vref*(R2//R3)/(R1+(R2//R3)+80)
=2*(20K//66.5K)/(9.09k+(20K//66.5K)+80)
=1.253V

Security Classification	Compal Secret Data		
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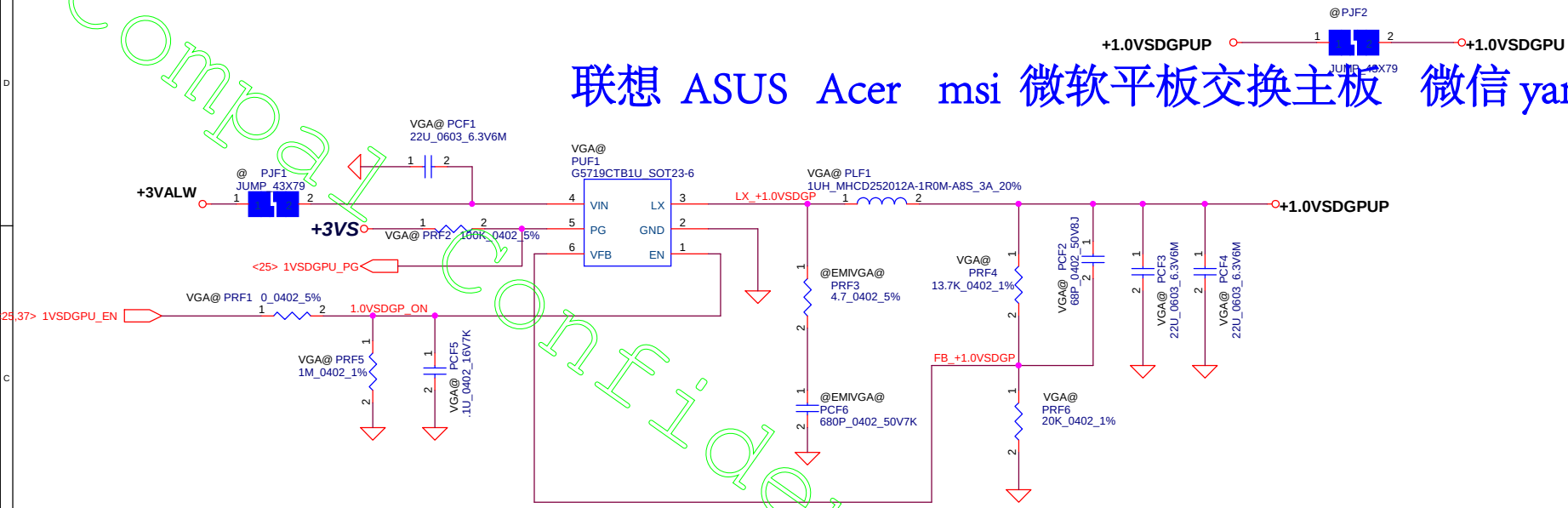
Compal Electronics, Inc.

Title: **+1.35VRAM**

Size	Document Number	Rev
		0.1

Date: Friday, September 28, 2018 Sheet 94 of 100

SKL_H 42



Vout=0.6V* (1+PRF4/PRF6)
Imax= 2A
Ipeak= 3A

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Security Classification	Compal Secret Data		
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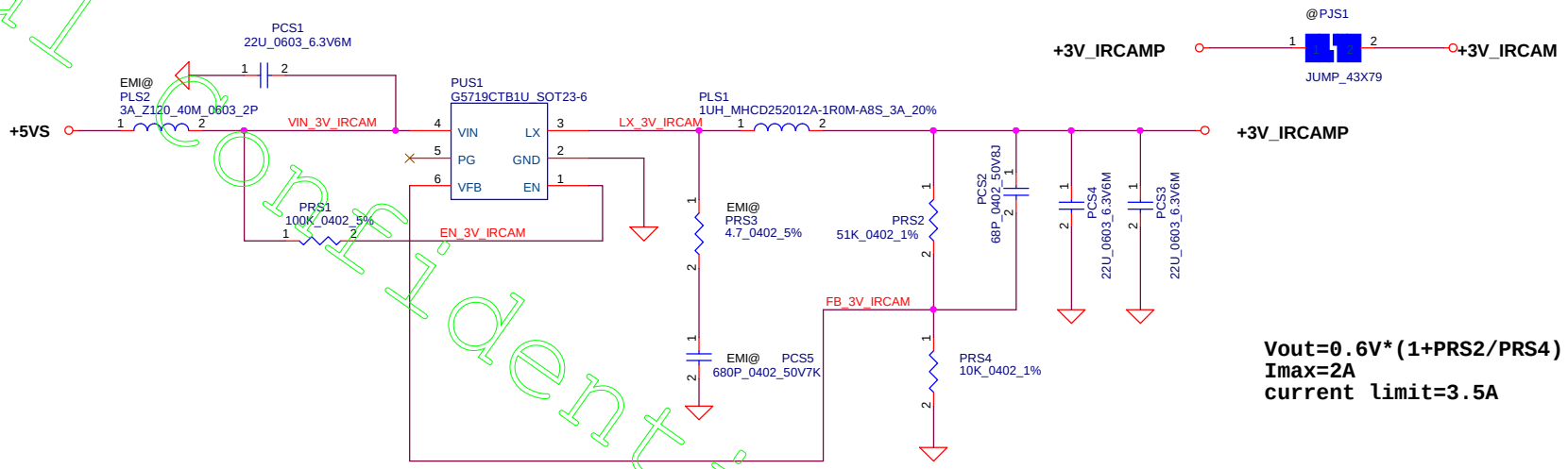
Compal Electronics, Inc.

Title: **+1.0VSDGPUP**

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 95 of 100



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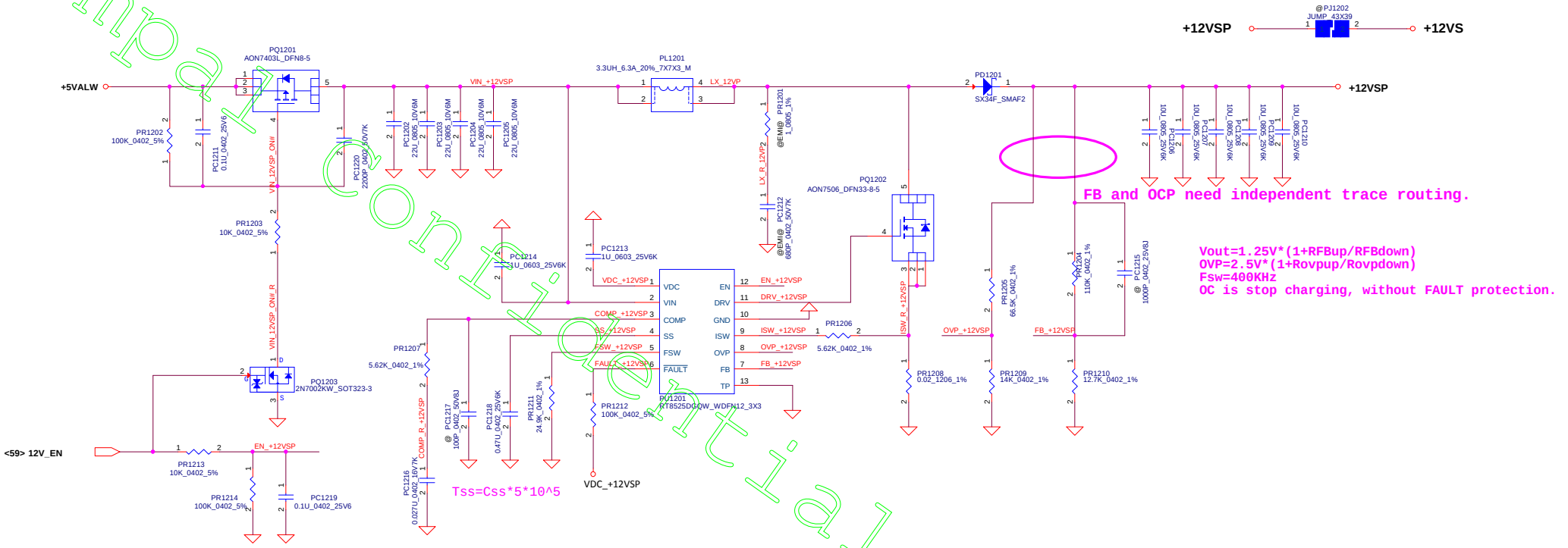
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: +3V_IRCAMP

Size: B | Document Number: | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 96 of 100



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Security Classification	Compal Secret Data		
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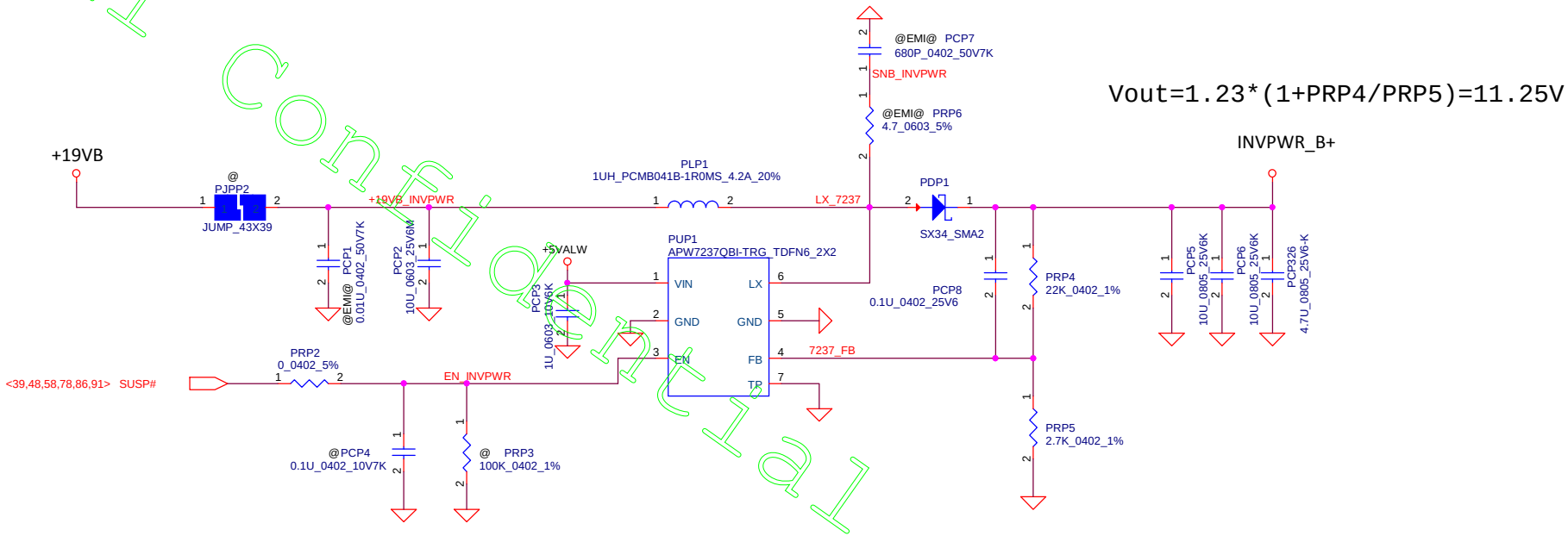
Title: +12VS

Size	Document Number	Rev
Custom		0.1

Date: Friday, September 28, 2018 | Sheet 97 of 100



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Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **INVPWR_B++**

Size: B	Document Number:	Rev: 0.1
Date: Friday, September 28, 2018	Sheet 98 of 100	

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Title	PIR		
Size B	Document Number		Rev 0.1
Date: Friday, September 28, 2018		Sheet 99 of 100	

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **Reserve for PWR**

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 100 of 100