ROGUE ONE 15"/17" Schematics
WhiskyLake - U/2GB VRAM

2018-07-12

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

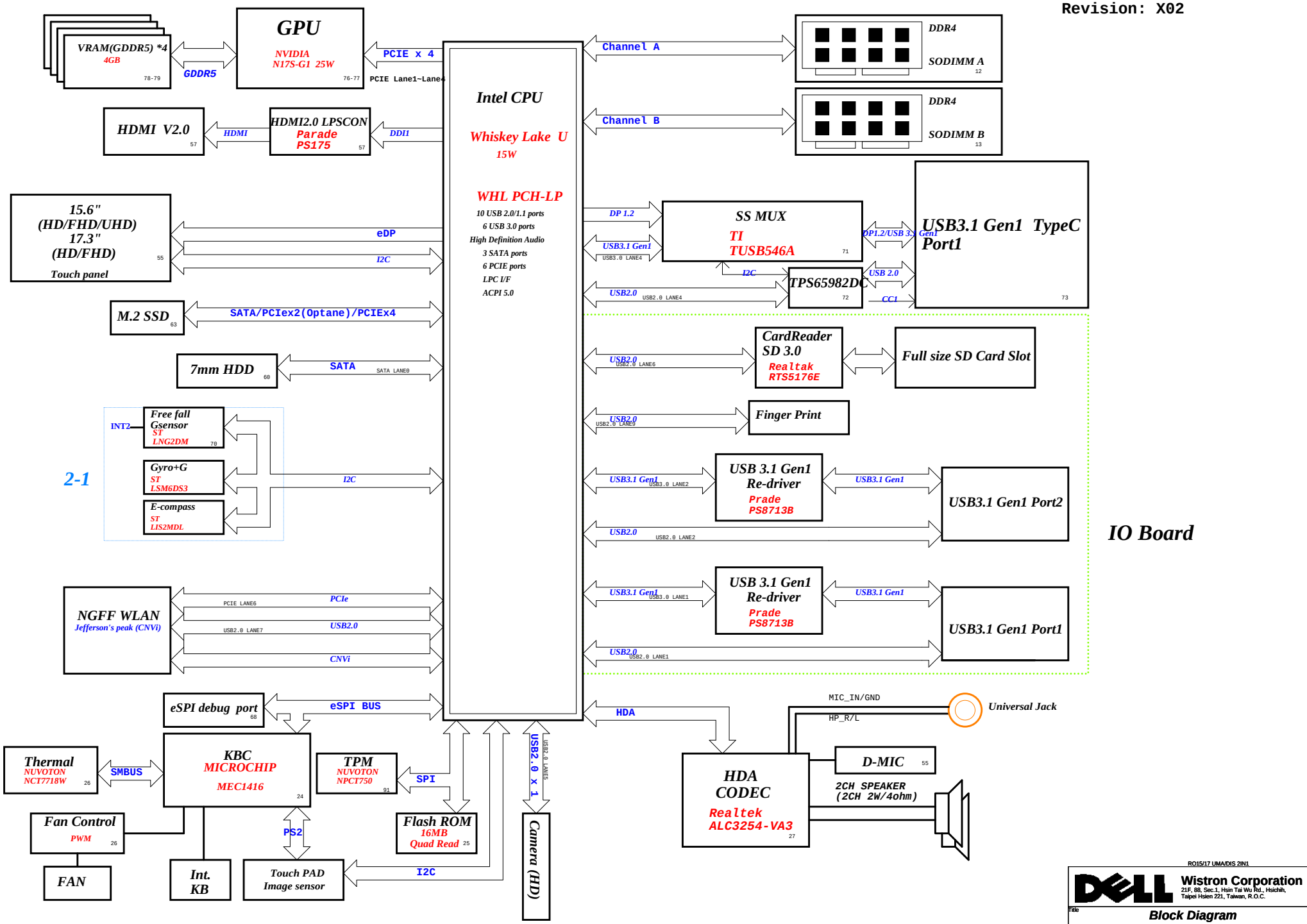
RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Rogue One 15"/17" WHL-U	Rev: A00
Date: Tuesday, July 24, 2018	Sheet 1 of 106	

ROGUE ONE 15"/17" CPU 15W + GPU 25W Block Diagram

Project code: 4PD0EZ01A001
PCB P/N: 18706
Revision: X02



RO15/17 UMA/DIS 2IN1

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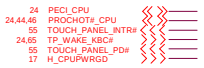
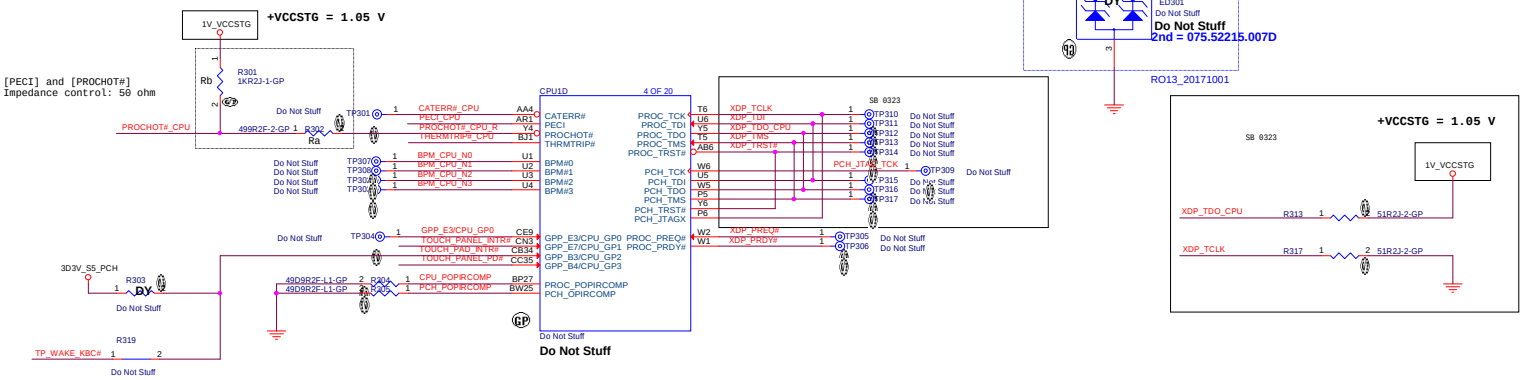
Title	Block Diagram	
Size: C	Document Number: Rogue One 15"/17" WHL-U	Rev: A00
Date: Tuesday, July 24, 2018	Sheet 2 of 106	

Main Func = CPU





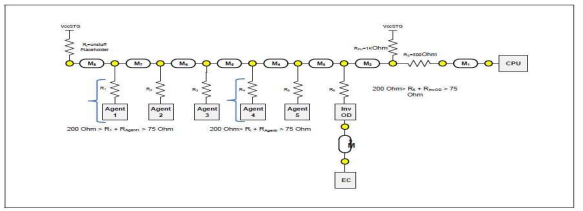


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

RO15/17 UMA/DIS 2IN1

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Title: CPU (THML/JTAG)

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 3 of 106

Main Func = CPU

DP to HDMI2.0

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3
57 DP1_AUX_CPU_N
57 DP1_AUX_CPU_P
57 HDMI_HPD_CPU

DP for Type-C Mux

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3
71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU
71,72 DP1_HPD_CPU

24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN

15 GPP_H17_STRAP

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

3D3V_S0
RN401 SRN2K2J-5-GP
1 2 4 3
CPU_DP1_CTRL_DATA
CPU_DP1_CTRL_CLK

3D3V_S0
RN402 SRN2K2J-5-GP
2 1 4
CPU_DP2_CTRL_DATA
CPU_DP2_CTRL_CLK

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Port B DP to HDMI2.0

Port C DP for Type-C Mux

CPU1A 1 OF 20

HDMI_DDI_TX_N0 AL5
HDMI_DDI_TX_P0 AL6
HDMI_DDI_TX_N1 AJ6
HDMI_DDI_TX_P1 AJ5
HDMI_DDI_TX_N2 AF6
HDMI_DDI_TX_P2 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3

DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2
DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3

EDP_TXN0 AG4 eDP_TX_CPU_N0
EDP_TXP0 AG3 eDP_TX_CPU_P0
EDP_TXN1 AG2 eDP_TX_CPU_N1
EDP_TXP1 AG1 eDP_TX_CPU_P1
EDP_TXN2 AJ4 eDP_TX_CPU_N2
EDP_TXP2 AJ3 eDP_TX_CPU_P2
EDP_TXN3 AJ2 eDP_TX_CPU_N3
EDP_TXP3 AJ1 eDP_TX_CPU_P3

EDP_AUX_N AH4 eDP_AUX_CPU_N
EDP_AUX_P AH3 eDP_AUX_CPU_P
DISP_UTILS AM7
SA 0131

DDI1_AUX_N AC7 DP1_AUX_CPU_N
DDI1_AUX_P AC6 DP1_AUX_CPU_P
DDI2_AUX_N AD4 DP2_AUX_CPU_N
DDI2_AUX_P AD3 DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

for HDMI2.0

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_HPD_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP1_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7 eDP_HPD_CPU

EDP_BKLTEN CK11 L_BKLT_EN
EDP_VDDEN CG11 EDP_VDD_EN
EDP_BKLTCTL CH11 L_BKLT_CTRL

RO13_20170626
RCOMP SHOULD BE VSS REFERNCE AND SHIELDED
1V_VCCIO
CHECK WHL design guide: DISP_RCOMP
1 R491 24D9R2F-1-GP
eDP_RCOMP_CPU AM6
DISP_RCOMP

CPU_DP1_CTRL_CLK CC8
CPU_DP1_CTRL_DATA CC9
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA
CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

Do Not Stuff TP402 1 GPP_E23 CP4 CN4
SA 0105 strap reserve
GPP_H17_STRAP CP26 CP28
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA
Do Not Stuff

Do Not Stuff

3D3V_S0
SIO_EXT_SMI# 1 R402 2 10KR2J-3-GP

Add RTC Gen 9 reset circuit_20170814 leakage issue

3D3V_S5_PCH
R406 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R405 10KR2J-3-GP
RTC_RST
RO13_20171011
Q401 2N7002KDW-1-GP
common part
75.27002.F7C
2nd = 075.27002.0E7C
DP1_HPD_CPU_R
DP1_HPD_CPU
CPU_DP_HPD_P
RTC_RST
DY
R407 Do Not Stuff
SB 0403

RTC Gen 9 reset circuit_20170814
DP1_HPD_CPU_R
R404 1 Do Not Stuff DP1_HPD_CPU
NON_RTC_RST
R403 100KR2J-1-GP

DP for Type-C Mux

RO15/17 UMA/DIS 2IN1

Wistron Corporation
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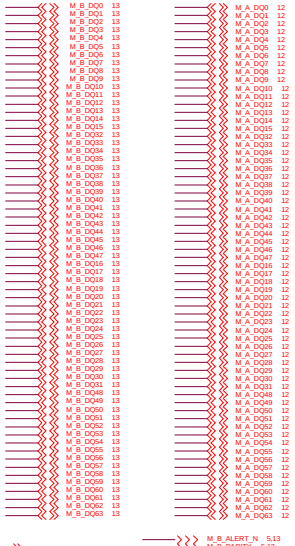
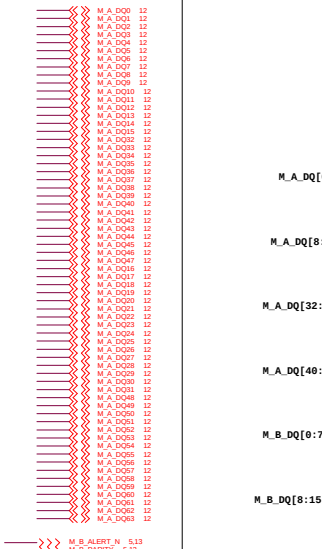
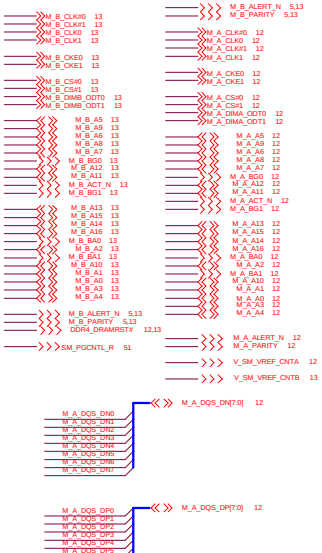
Title: CPU (DDI/EDP)
Size: A2
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
Sheet 4 of 106

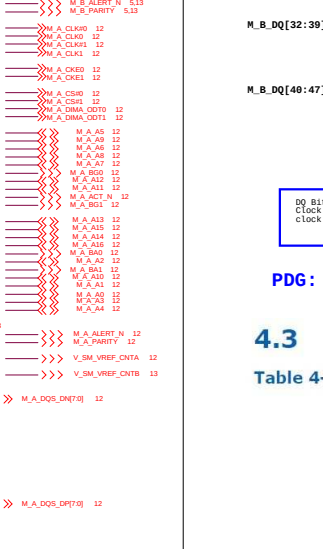
Main Func = CPU

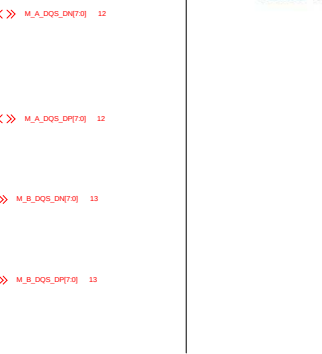
DDR4 ball type: NON-Interleaved Type

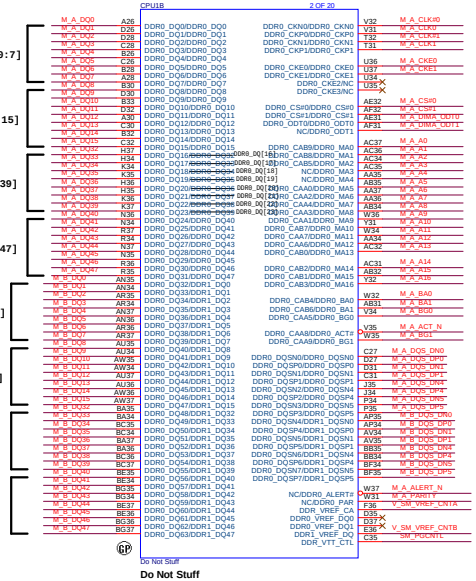


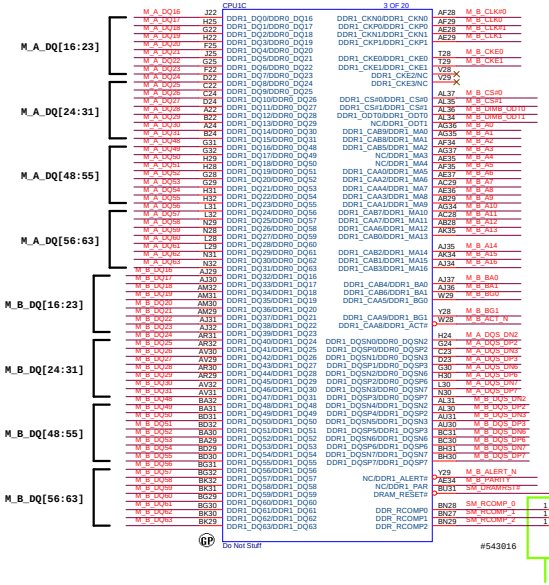












DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

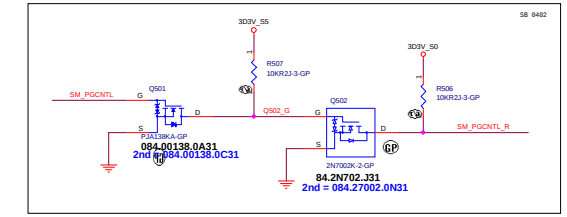
4.3 ODT Connectivity

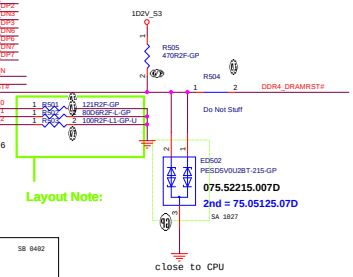
Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

Note:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.





#543016

RO1S/17 UMA/DIS 2IN1

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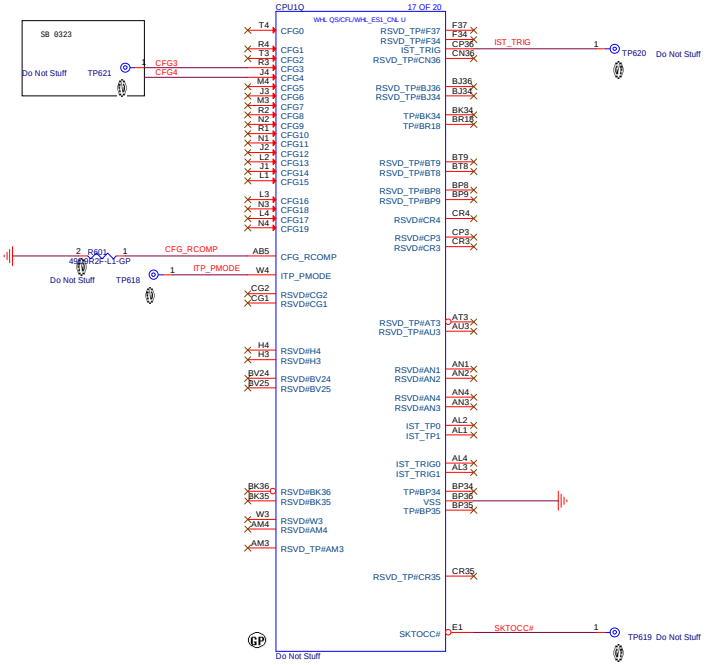
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)
Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 5 of 106

Main Func = CPU

15 CFG3

15 CFG4



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

RO15/17 UMA/DIS 2IN1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CFG/IST)

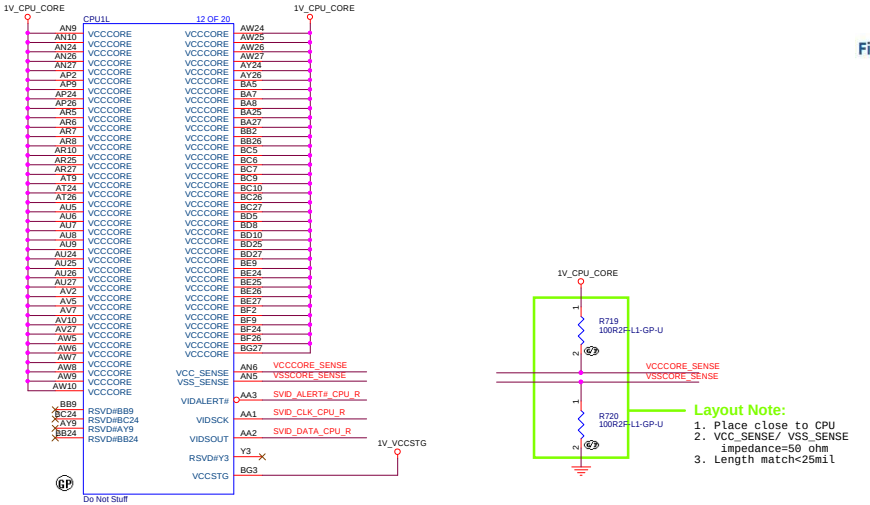
Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 6 of 106

Main Func = CPU

46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU



Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

SVID DATA

SVID CLOCK

SVID ALERT

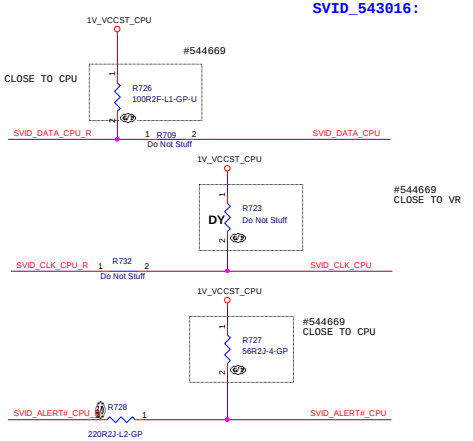


Figure 7-19. Routing Illustration for SVID Topology

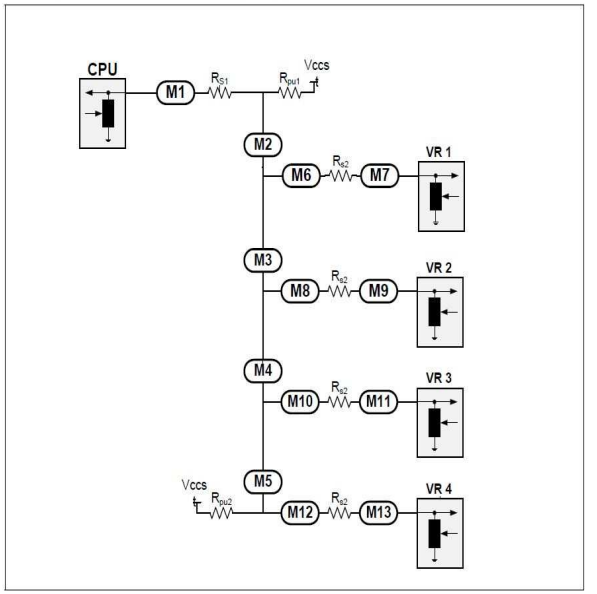


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

RO15/17 UMA/DIS 2IN1

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Title: CPU (VCORE/VID)

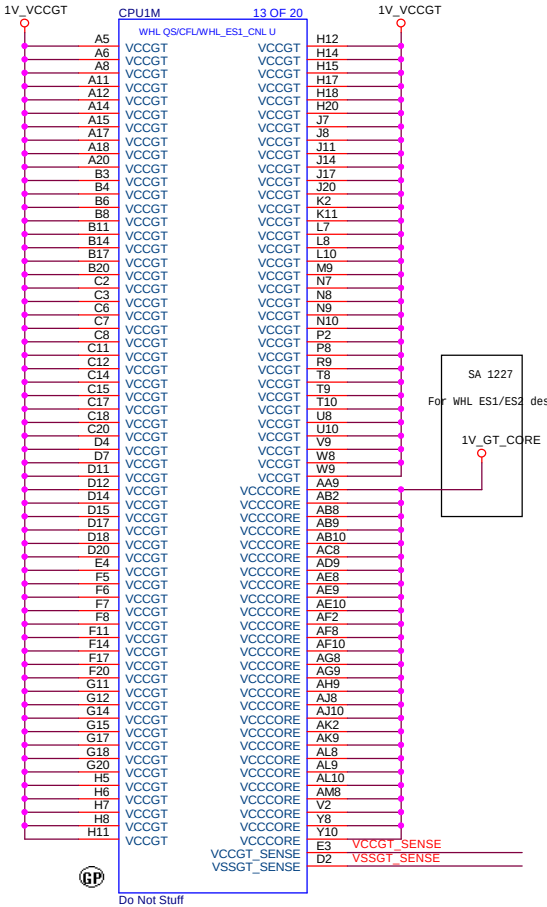
Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

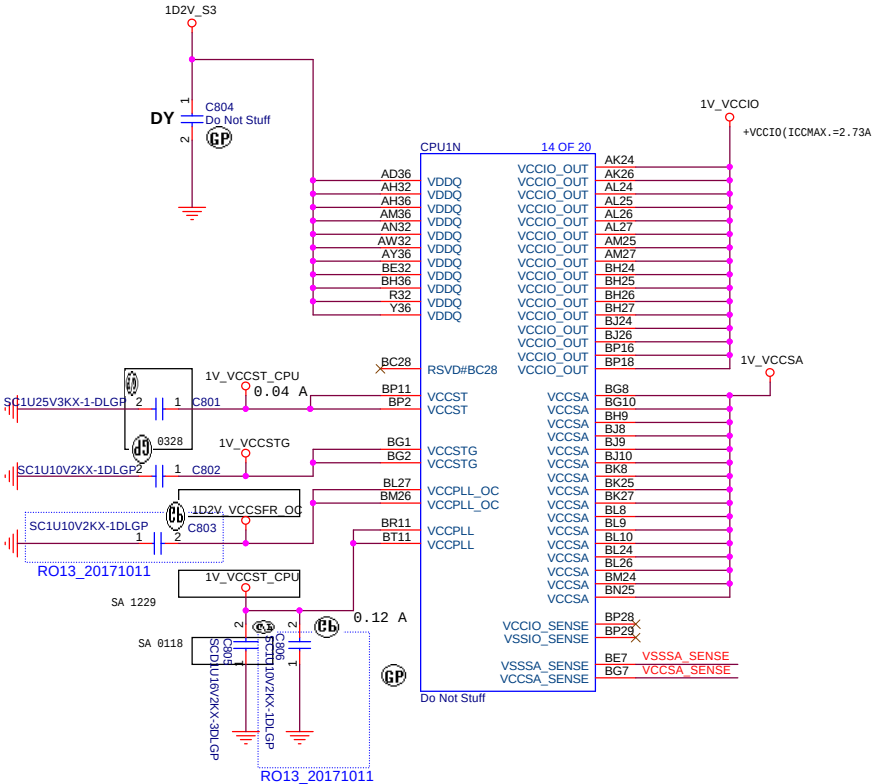
Date: Tuesday, July 24, 2018 | Sheet 7 of 106

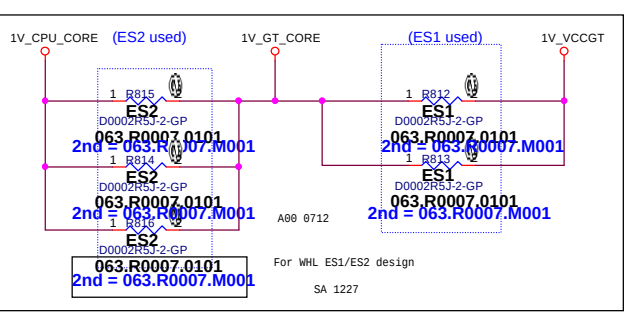
Main Func = CPU

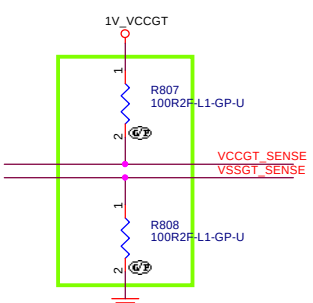
46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE

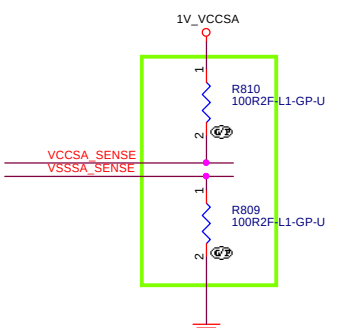
Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE











RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCGT/VCCIO/VDDQ/VCCSA)

Size: A3 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 8 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RSVD)

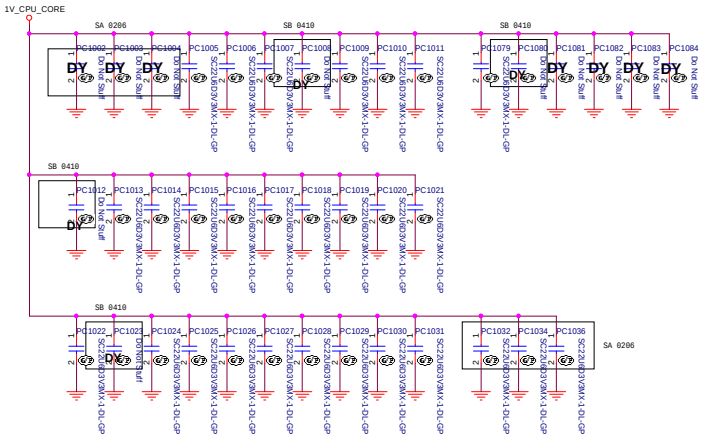
Size: A3 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 9 of 106

Main Func = CPU

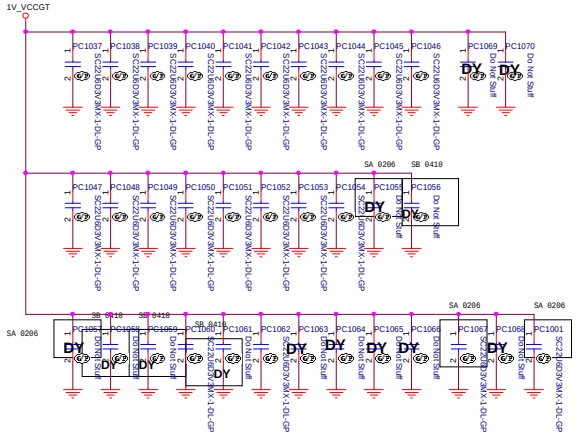
1V_CPU_CORE

22U 0603 x 39 (3DY)



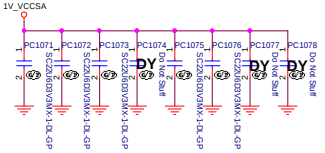
VCCGT

22U 0603 x 35 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



11.3.1 Whiskey Lake U 4+2 Decoupling Requirement

Table 11-1. Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

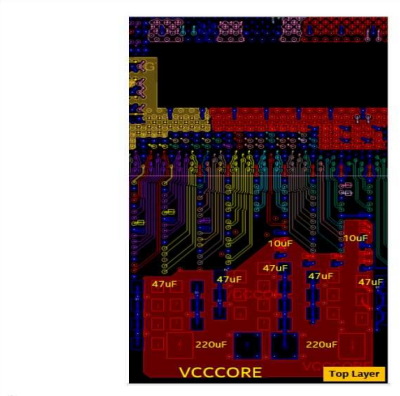
Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
Vcc_{GT}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

Figure 11-8. Whiskey Lake U 4+2 Vcc_{CORE} Routing Guideline



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

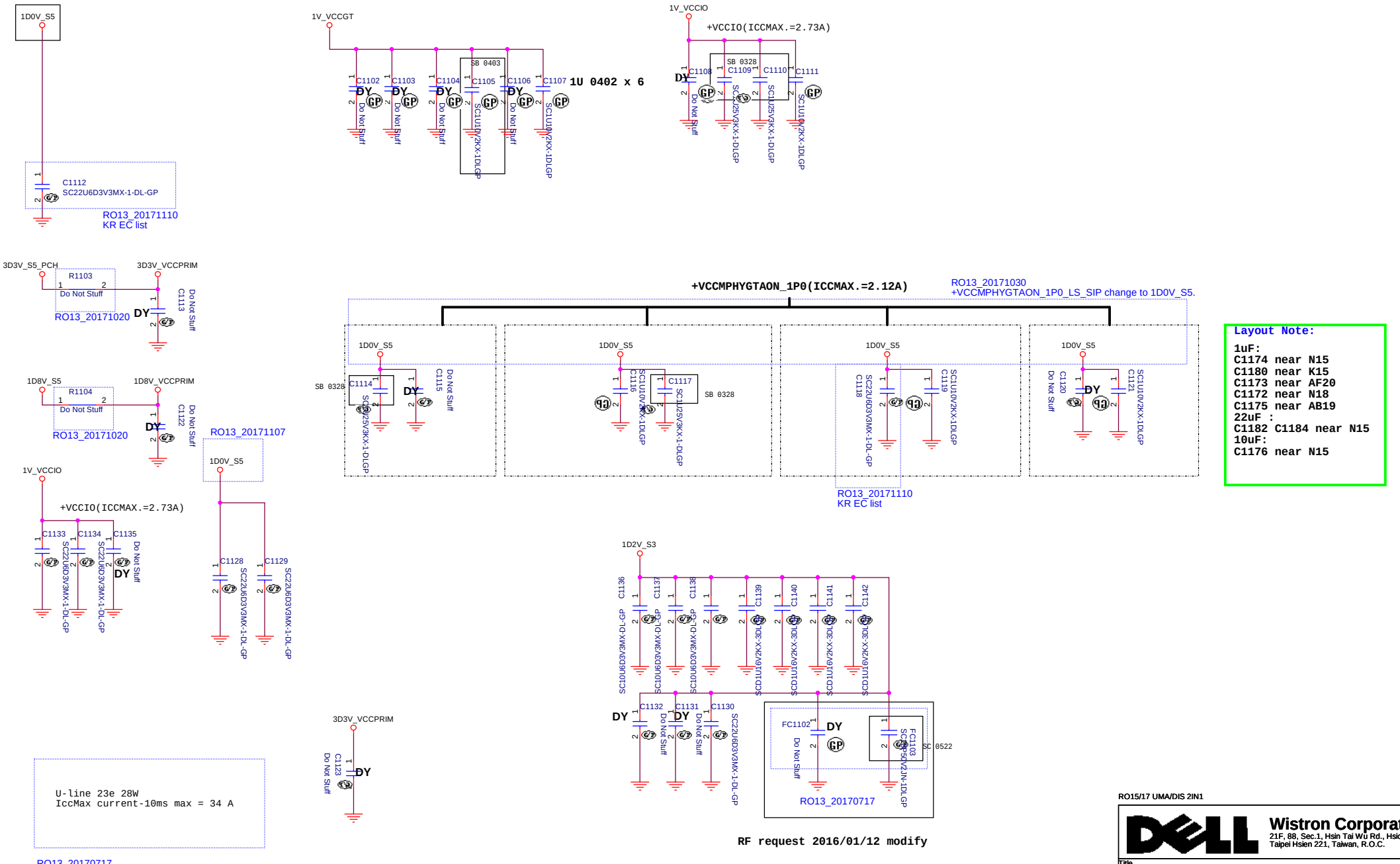
Title: CPU (CORE Power Cap1)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 10 of 106

Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



RO15/17 UMA/DIS 2IN1

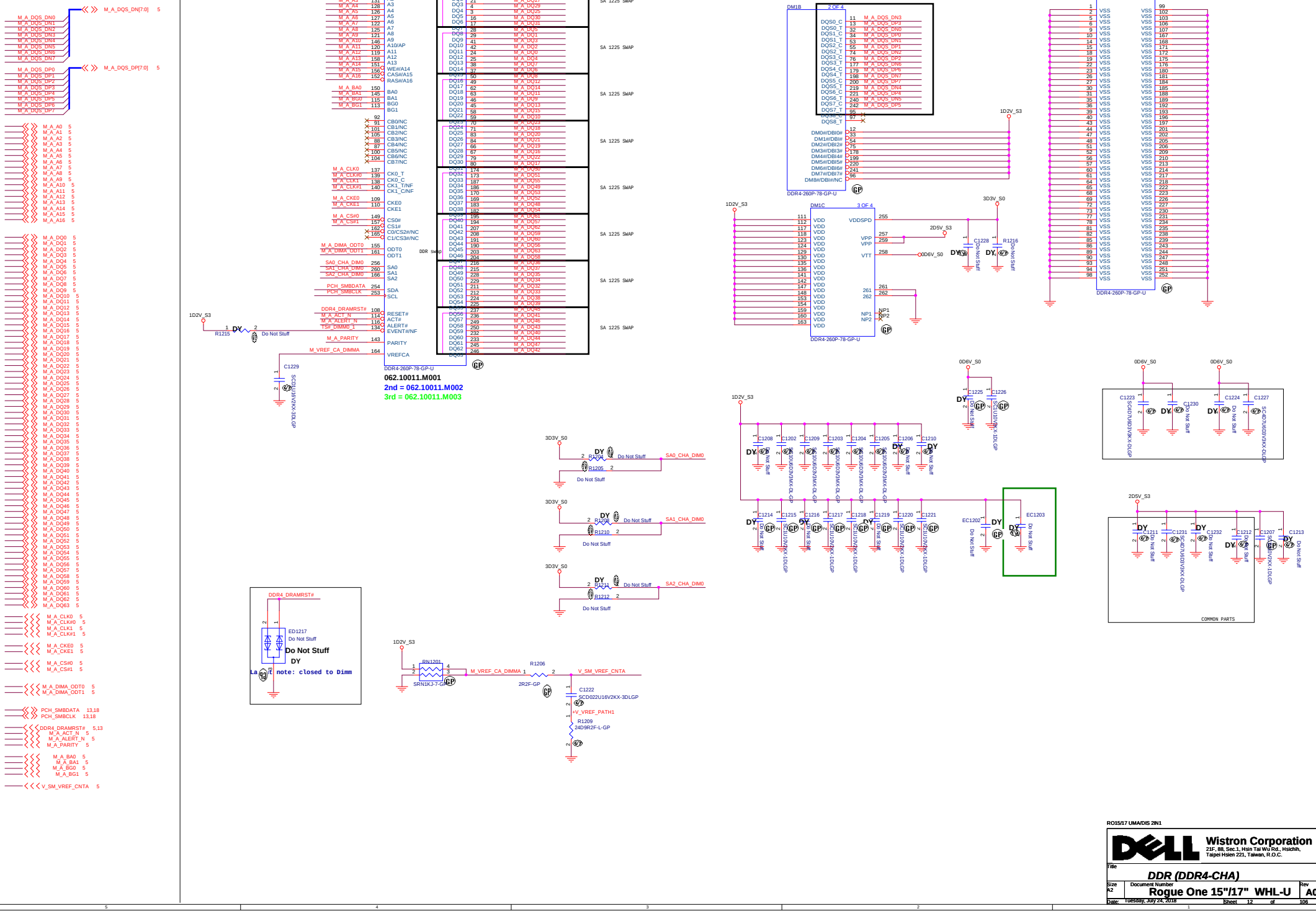
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (Power Cap2)

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 11 of 106

Main Func = MEMORY



RO15/17 UMA/DIS 2IN1

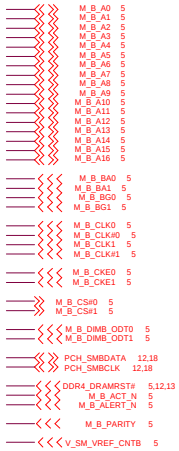
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

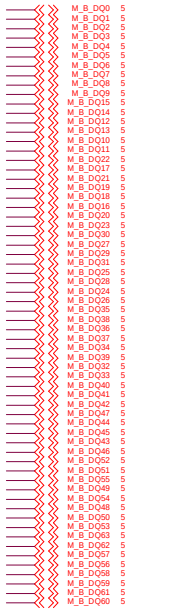
Title: DDR (DDR4-CHA)

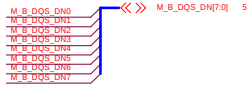
Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

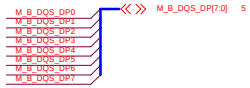
Date: Tuesday, July 24, 2018 | Sheet 12 of 106

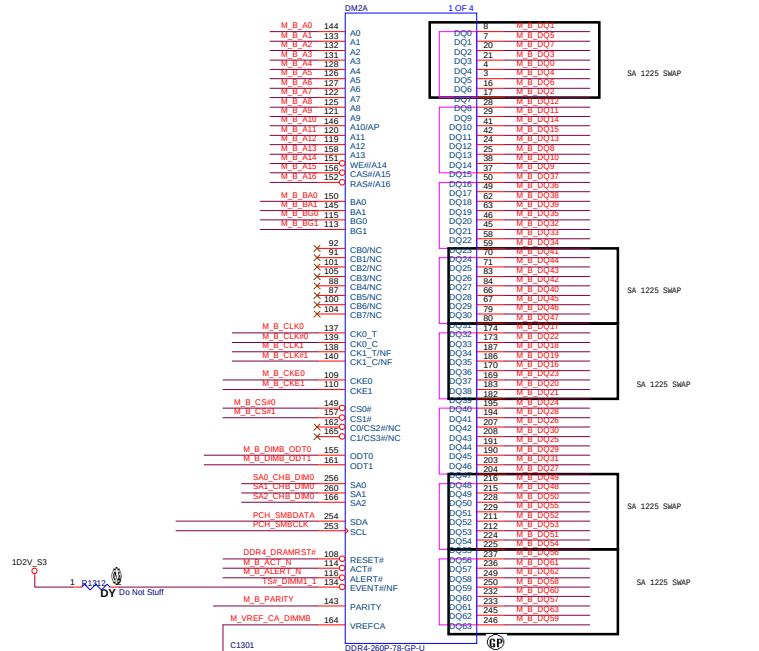
Main Func = MEMORY

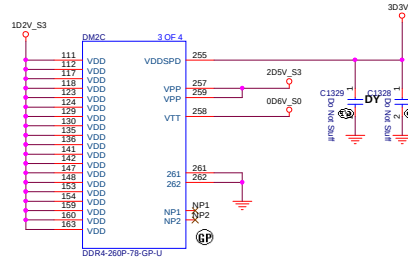


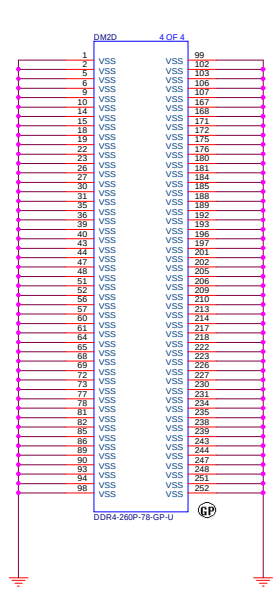


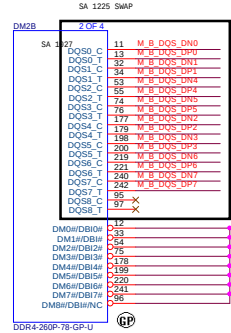


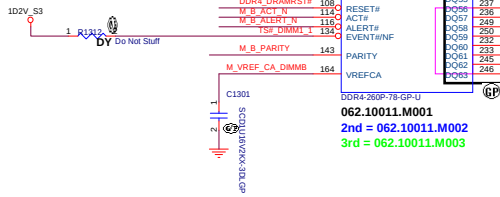


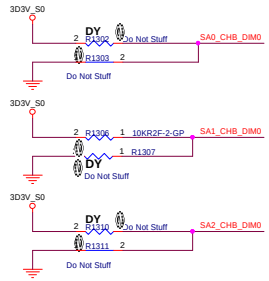


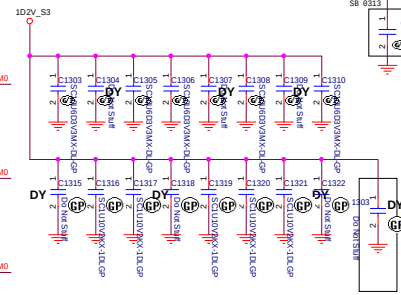


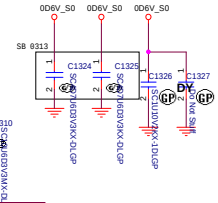


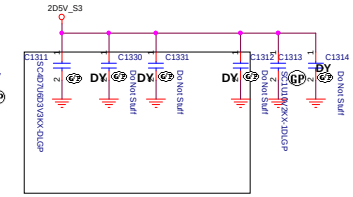


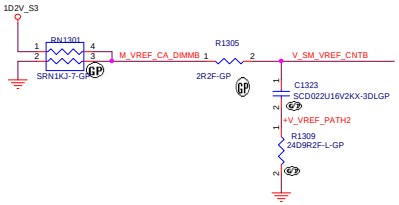












RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (DDR4-CHB)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 13 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

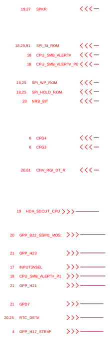
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR (RSVD) (DDR4-CHA1)***

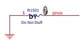
Size	Document Number	Rev
A4	***Rogue One 15"/17" WHL-U***	***A00***

Date: Tuesday, July 24, 2018 Sheet 14 of 106

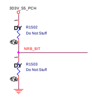
Main Func = PCH



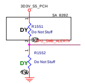
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.



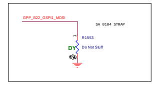
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



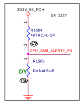
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



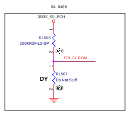
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.



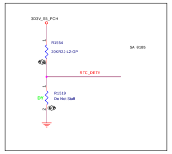
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**



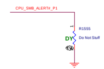
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



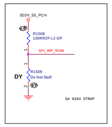
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



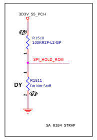
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.



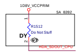
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

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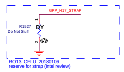
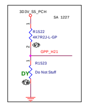
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.



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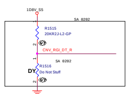
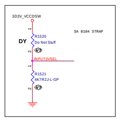
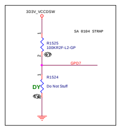
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.



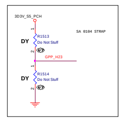
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

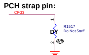


GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**



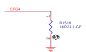
[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

PCH strap pin:



(#543016)

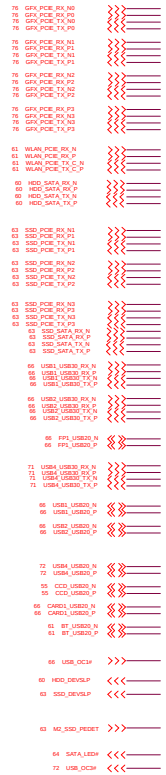
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



RO15/17 UMA/DIS 2IN1

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (STRAP)		
Size: A0	Document Number: Rogue One 15"/17" WHL-U	Rev: A00
Date: Tuesday, July 24, 2018	Sheet 15 of 106	

Main Func = PCH



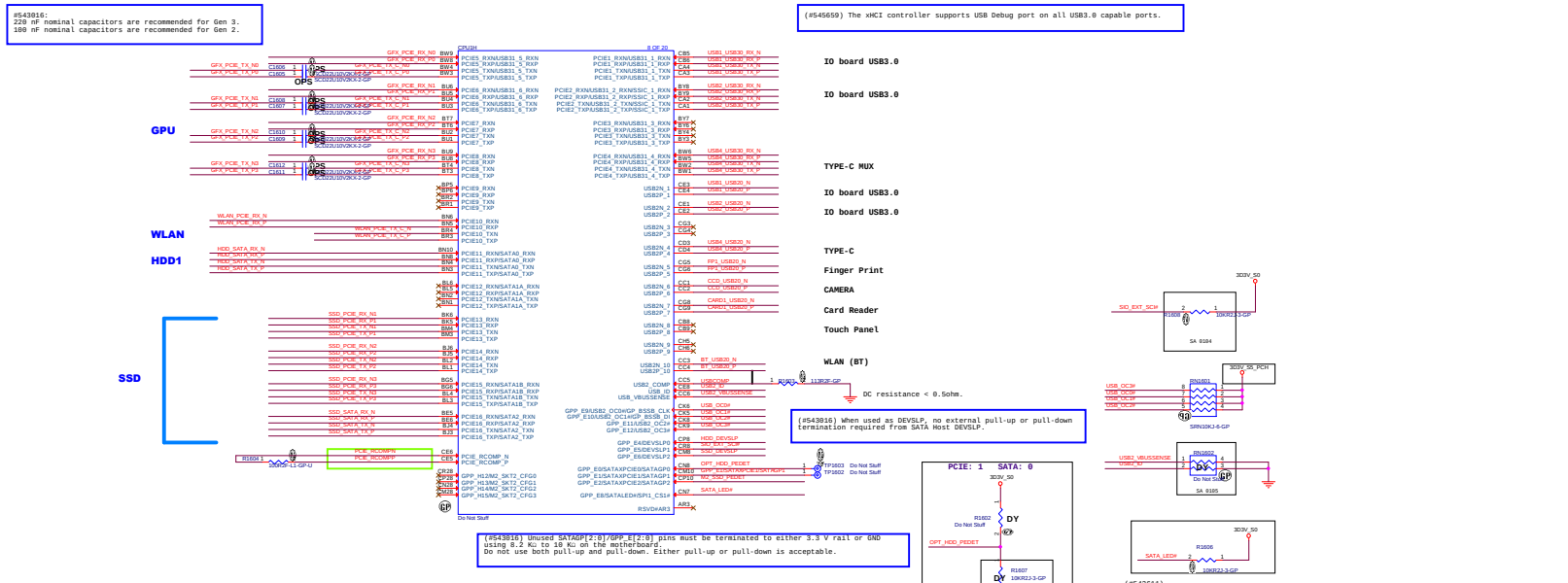


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

6.3.1 PCH PCI Express* Interface Configuration Details

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3		RP1	RP8	RP7		RP5	RP12	RP11		RP9	RP16	RP15		RP13
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

RC15/17 UMA/DIS 2IN1

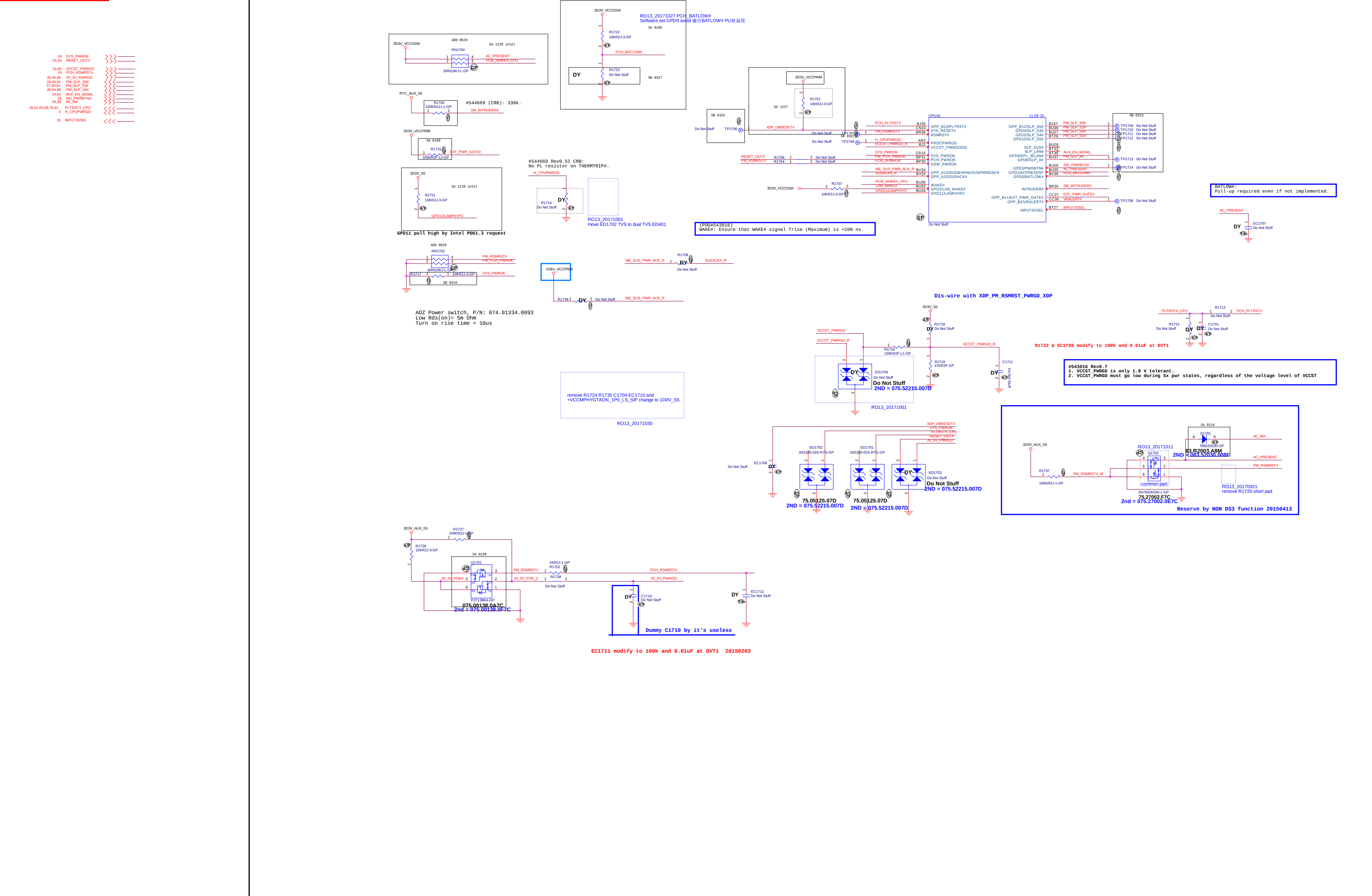
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

CPU (PCIE/SATA/USB)

Size: A1 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 16 of 106

Main Func = PCH



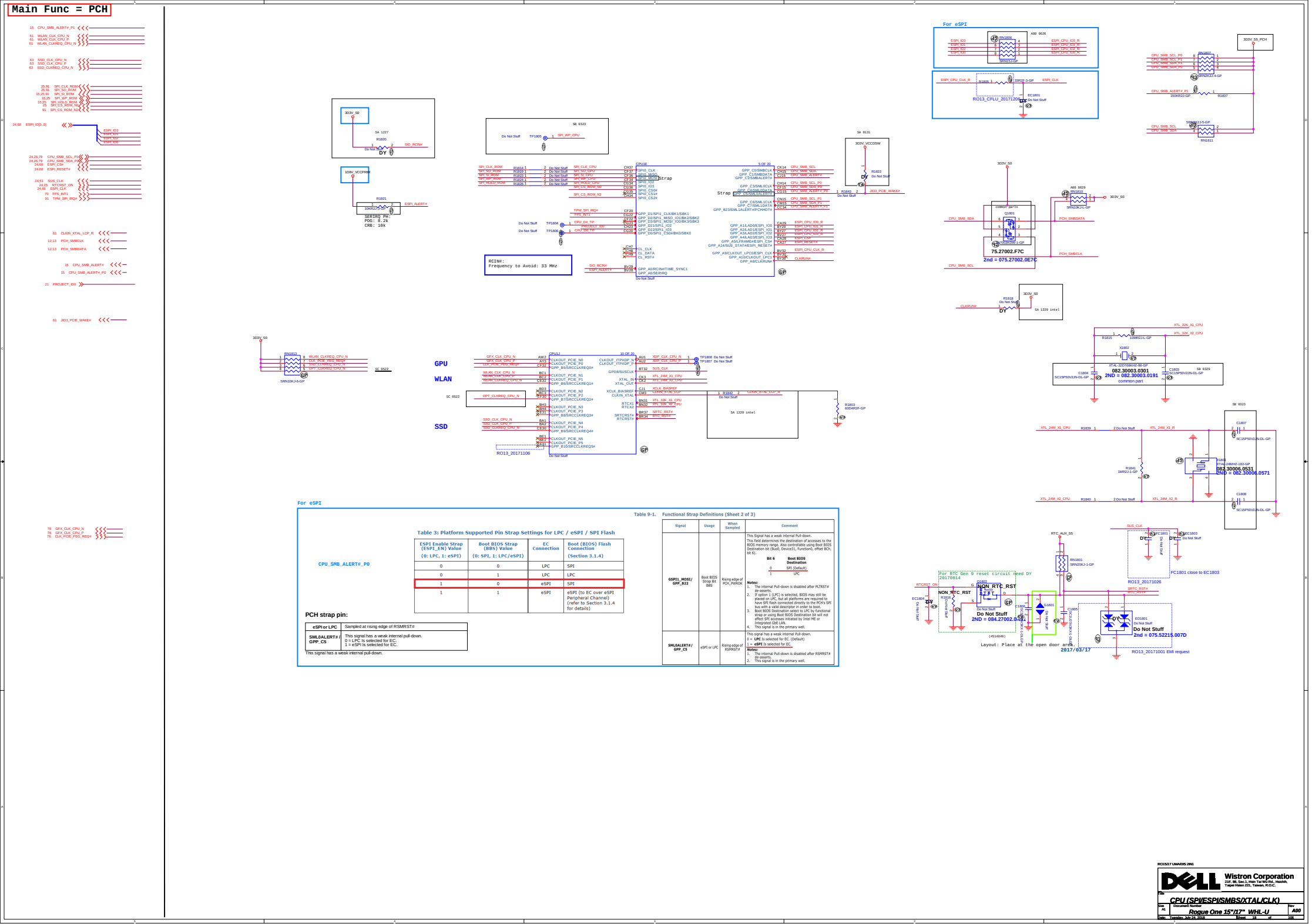
SYS_PWROK
RESET_OUT#
VCCST_PWRGD
PCH_RSMRST#
3V_5V_PWRGD
PM_SLP_S0#
PM_SLP_S3#
PM_SLP_S4#
AUX_EN_WOWL
SIO_PWRBTN#
AC_IN#
PLTRST#_CPU
H_CPUPWRGD
INPUT3VSEL
3D3V_VCCDSW
RN1704
SRN10KJ-L-GP
AC_PRESENT
PCIE_WAKE#_CPU
SA 1228 intel
RTC_AUX_S5
R1730
330KR2J-L1-GP
SM_INTRUDER#
#544669 (CRB): 330k.
3D3V_VCCPRIM
R1731
100KR2F-L2-GP
EXT_PWR_GATE#
3D3V_S5
R1721
10KR2J-3-GP
GPD11/LANPHYPC
GPD11 pull high by Intel PDG1.3 request
R1722
10KR2J-3-GP
PCH_BATLOW#
R1723
Do Not Stuff
RO13_20171027 PCH_BATLOW#
Software set GPD0 avoid 關閉BATLOW# PU會漏電
#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.
R1714
Do Not Stuff
RO13_20171001
move ED1702 TVS to dual TVS ED401
R1701
10KR2J-3-GP
XDP_DBRESET#
TP1706
CPU1K
11 OF 20
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGOOD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
BATLOW#:
Pull-up required even if not implemented.
(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.
RN1703
PM_RSMRST#
PM_PCH_PWROK
R1717
10KR2J-3-GP
1D8V_VCCPRIM
R1738
ME_SUS_PWR_ACK_R
R1708
SUSACK#_R
AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us
Dis-wire with XDP_PM_RSMRST_PWRGD_XDP
3D3V_S0
R1718
R1716
100KR2F-L1-GP
VCCST_PWRGD_R
R1719
47KR2F-GP
C1711
ED1704
Do Not Stuff
2ND = 075.52215.007D
RO13_20171001
R1722 & EC1708 modify to 100k and 0.01uF at DVT1
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
remove R1724 R1735 C1704 EC1710 and
+VCCMPHYGTAON_1P0_LS_SIP change to 1D0V_S5.
RO13_20171030
ED1702
ED1701
AZ5125-02S-R7G-GP
75.05125.07D
2ND = 075.52215.007D
ED1703
EC1706
R1713
PCH_PLTRST#
R1715
C1701
3D3V_AUX_S5
R1737
100KR2J-1-GP
PM_RSMRST#_M
Q1702
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
common part
D1701
RB520S30-GP
83.R2003.A8M
2ND = 083.52030.008F
RO13_20171011
RO13_20170921
remove R1720 short pad
Reserve by NON DS3 function 20150413
R1727
100KR2J-1-GP
R1726
10KR2J-3-GP
Q1701
PJT138KA-GP
075.00138.0A7C
2nd = 075.00138.0F7C
R1702
1KR2J-1-GP
R1728
3V_5V_POK#
3V_5V_POK_C
PCH_RSMRST#
3V_5V_PWRGD
C1710
EC1712
Dummy C1710 by it's useless
EC1711 modify to 10k and 0.01uF at DVT1 20150203

RO15/17 UMA/DIS 2IN1

DELL — Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (PMU)		
Size A1	Document Number: Rogue One 15"/17" WHL-U		Rev A00
Date: Tuesday, July 24, 2018	Sheet 17 of 106		

Main Func = PCH



Main Func = PCH

61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
15,27 SPKR
27 HDA_SDIN0_CPU
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
68 ME_FWP_SW
27 HDA_SDOUT_CODEC
65 KB_LED_BL_DET
24 GC6_THM_DIS#
15 HDA_SDOUT_CPU
24,85 DGPU_PWROK

3D3V_S5
fTPM
R1910 10KR2J-3-GP
TPM_ID
TPM
R1911 Do Not Stuff

CPU1G 7 OF 20
HDA_SYNC_CPU BN34 HDA_SYNC/I2S0_SFRM
HDA_BITCLK_CPU BN37 HDA_BCLK/I2S0_SCLK
HDA_SDOUT_CPU BN36 HDA_SDO/I2S0_TXD
HDA_SDIN0_CPU BN35 HDA_SDI0/I2S0_RXD
BL36 HDA_SDI1/I2S1_RXD/SNDW1_DATA
Do Not Stuff TP1903 1 HDA_RST_N_CPU BL35 HDA_RST#/I2S1_SCLK/SNDW1_CLK
CK23 GPP_D23/I2S_MCLK
BL37 I2S1_SFRM/SNDW2_CLK
BL34 I2S1_TXD/SNDW2_DATA
BT_PCMFRM_RSTN 1 R1923 33R2J-2-GP
BT_PCMOUT_CLKREQ0 1 R1922 33R2J-2-GP
SA 1229 intel
GPP_H1_SFRM CJ32 GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#
GPP_H2_CLKREQ0 CH29 GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK
CH30 GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO
SA 1229
DMIC_PCH_CLK CP24 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7
DMIC_PCH_DATA CN24 GPP_D19/DMIC_CLK0/SNDW4_CLK GPP_A16/SD_1P8_SEL
GPP_D20/DMIC_DATA0/SNDW4_DATA
TPM_ID CK25 SD_1P8_RCOMP
DGPU_PWROK CJ25 GPP_D17/DMIC_CLK1/SNDW3_CLK SD_3P3_RCOMP
GPP_D18/DMIC_DATA1/SNDW3_DATA
SPKR CF35 GPP_B14/SPKR
Do Not Stuff
GPP_G0/SD_CMD CH36
GPP_G1/SD_DATA0 CL38 GC6_THM_DIS#
GPP_G2/SD_DATA1 CL36
GPP_G3/SD_DATA2 CM35
GPP_G4/SD_DATA3 CN35
GPP_G5/SD_CD# CH35
GPP_G6/SD_CLK CK36 KB_LED_BL_DET
GPP_G7/SD_WP CK34
BW36
BY31
CK33 SD_RCOMP
CM34
R1901 1 2.200R2F-L-GP
RO13_CFLU_20171207

EC1901 DY HDA_BITCLK_CODEC
Do Not Stuff

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin: SPKR

TOP SWAP OVERRIDE	
HDA_SPKR	* High = TOP SWAP ENABLED Low = DISABLED (WEAK INTERNAL PD)

The internal pull-up

RO13_CFLU_20171212

RO13_20171027
delete ED1901

HDA_SYNC_CODEC 1 R1908 2 HDA_SYNC_CPU
Do Not Stuff

R1920~R1921 need to close for merge prepare

HDA_BITCLK_CODEC HDA_BITCLK_CPU
HDA_SDOUT_CODEC R1920 1 Do Not Stuff HDA_SDOUT_CPU
R1921 1 33R2J-2-GP
SA 1229 intel
ME_FWP_SW R1909 1 1KR2J-1-GP

HDA_SDOUT_CODEC
EC1903 DY
Do Not Stuff

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HAD/I2S/SD/DMIC)
Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 19 of 106

Main Func = PCH

79,86 GC6_FB_EN
55 CPU_I2C_SDA_P1
55 CPU_I2C_SCL_P1
65 CPU_I2C_SDA_P0
65 CPU_I2C_SCL_P0
55 DBC_PANEL_EN

68 UART_2_CRXD_DTXD
68 UART_2_CTXD_DRXD
24 SIO_EXT_WAKE#
65 KB_DET#

55 GSEN_INT1
55 GSEN_INT2
70 GSEN2_INT1_C
70 GSEN2_INT2_C
70 GYRO_INT_C
55 GYRO_DRDY
15,25 RTC_DET#
55,70 CPU_I2C_SDA_ISH
55,70 CPU_I2C_SCL_ISH
70 FFS_INT2

91 PIRQA#
21 BOARD_ID2

61 CNV_BRI_RSP
15,61 CNV_RGI_DT_R
61 CNV_BRI_DT_R
61 CNV_RGI_RSP

76 DGPU_HOLD_RST#
79 GPU_EVENT#
86 DGPU_PWR_EN
15 NRB_BIT
15 GPP_B22_GSPI1_MOSI
24 NB_MODE#

EC2002 DY DGPU_HOLD_RST#
Do Not Stuff
RN2009 DGPU_HOLD_RST#
OPS DGPU_PWR_EN
SRN10KJ-7-GP
A00 0629

1D8V_VCCPRM
R2053 Do Not Stuff PIRQA#
DY

3D3V_S0
Do Not Stuff R2048 UART_2_CRXD_DTXD
Do Not Stuff R2049 UART_2_CTXD_DRXD
DEBUG
Do Not Stuff DY R2043 DBC_PANEL_EN
10KR2J-3-GP R2044 FFS_INT2
10KR2J-3-GP R2045 KB_DET#
10KR2J-3-GP R2046 IR_CAM_DET#
SA 0112

3D3V_S5_PCH
10KR2J-3-GP R2041 SIO_EXT_WAKE#

1D8V_S5
SB 0326
R2029 DY 20KR2J-L2-GP CNV_RGI_RSP
R2030 DY 20KR2J-L2-GP CNV_BRI_RSP
A00 0626

GPU_EVENT# R2003 Do Not Stuff GPU_EVENT_MCP#
GC6_FB_EN R2004 Do Not Stuff PIRQA#
GC6_FB_EN_MCP
VRAM_ID1
NRB_BIT
DBC_PANEL_EN
GPP_B22_GSPI1_MOSI

SA 1212 For CNVi
SA 0109 CNV_RGI_DT_R R2006 SSR2J-1-GP CNV_RGI_DT
CNV_BRI_DT_R R2007 SSR2J-1-GP CNV_BRI_DT
CNV_BRI_RSP
CNV_RGI_RSP

UART_2_CRXD_DTXD
UART_2_CTXD_DRXD
SIO_EXT_WAKE#
KB_DET#
CPU_I2C_SDA_P0
CPU_I2C_SCL_P0
CPU_I2C_SDA_P1
CPU_I2C_SCL_P1

TPAD
Touch panel

CPU1F 6 OF 20
CC27 GPP_B15/GSPI0_CS0#
CC32 GPP_A7/PIRQA#/GSPI0_CS1#
CE28 GPP_B16/GSPI0_CLK
CE27 GPP_B17/GSPI0_MISO
CE29 GPP_B18/GSPI0_MOSI Strap
CA31 GPP_B19/GSPI1_CS0#
CA32 GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
CC29 GPP_B20/GSPI1_CLK
CC30 GPP_B21/GSPI1_MISO
CA30 GPP_B22/GSPI1_MOSI
CB20 CNV_BRI_RSP
CB19 GPP_F5/CNV_BRI_RSP
CJ20 GPP_F6/CNV_RGI_DT
CH19 GPP_F4/CNV_BRI_DT
GPP_F7/CNV_RGI_RSP
CR12 GPP_C20/UART2_RXD
CP12 GPP_C21/UART2_TXD
CN12 GPP_C22/UART2_RTS#
CM12 GPP_C23/UART2_CTS#
CM11 GPP_C16/I2C0_SDA
CN11 GPP_C17/I2C0_SCL
CK12 GPP_C18/I2C1_SDA
CJ12 GPP_C19/I2C1_SCL
CF27 GPP_H4/I2C2_SDA
CF29 GPP_H5/I2C2_SCL
CH27 GPP_H6/I2C3_SDA
CH28 GPP_H7/I2C3_SCL
CJ30 GPP_H8/I2C4_SDA
CJ31 GPP_H9/I2C4_SCL
Do Not Stuff

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# CN22
GPP_D10/ISH_SPI_CLK/GSPI2_CLK CR22 DGPU_HOLD_RST#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO CM22 IR_CAM_DET#
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI CP22 RTC_DET#
GPP_D5/ISH_I2C0_SDA CK22 CPU_I2C_SDA_ISH0 R2021 2 Do Not Stuff CPU_I2C_SDA_ISH
GPP_D6/ISH_I2C0_SCL CH20 CPU_I2C_SCL_ISH0 R2020 2 Do Not Stuff CPU_I2C_SCL_ISH
GPP_D7/ISH_I2C1_SDA CH22 CPU_I2C_SDA_ISH1
GPP_D8/ISH_I2C1_SCL CJ22 CPU_I2C_SCL_ISH1
GPP_H10/I2C5_SDA/ISH_I2C2_SDA CJ27
GPP_H11/I2C5_SCL/ISH_I2C2_SCL CJ29
KBLR:GPP_F10~F11: 1.8V only
CFLU:GPP_H10~H11: ?V
GPP_D13/ISH_UART0_RXD CM24 DGPU_PWR_EN
GPP_D14/ISH_UART0_TXD CN23 VRAM_ID2
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# CM23
GPP_D16/ISH_UART0_CTS#/SML0BALERT# CR24
GPP_C12/UART1_RXD/ISH_UART1_RXD CG12 BOARD_ID1
GPP_C13/UART1_TXD/ISH_UART1_TXD CH12 FFS_INT2
GPP_C14/UART1_RTS#/ISH_UART1_RTS# CF12 UART1_RTS# 1 TP2001 Do Not Stuff
GPP_C15/UART1_CTS#/ISH_UART1_CTS# CG14 UART1_CTS# 1 TP2002 Do Not Stuff
GPP_A18/ISH_GP0 BW35 ISH_KB_DISABLE
GPP_A19/ISH_GP1 BW34 GSEN_INT1
GPP_A20/ISH_GP2 CA37 GSEN_INT2
GPP_A21/ISH_GP3 CA36 GSEN2_INT1_ISH R2025 2 Do Not Stuff GSEN2_INT1_C
GPP_A22/ISH_GP4 CA35 GSEN2_INT2_ISH R2026 2 Do Not Stuff GSEN2_INT2_C
GPP_A23/ISH_GP5 CA34 GYRO_INT_ISH R2027 2 Do Not Stuff GYRO_INT_C
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF# BW37 GYRO_DRDY_ISH R202a 2 Do Not Stuff GYRO_DRDY
DY

3D3V_S0
RN2007 SRN1KJ-7-GP
CPU_I2C_SDA_ISH0 CPU_I2C_SCL_ISH0
CPU_I2C_SDA_ISH1 CPU_I2C_SCL_ISH1
DY Do Not Stuff RN2008
SA 1228 intel

(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

VRAM_ID[2:1] 11: UMA
01: DIS+4G VRAM
00: DIS+2G VRAM

2016/11/07 modify

3D3V_S0 R2038 Do Not Stuff UMA VRAM_ID2 R2037 10KR2J-3-GP OPS
3D3V_S0 R2035 Do Not Stuff VRAM_ID_4G/UMA VRAM_ID1 R2034 10KR2J-3-GP VRAM_ID_2G
3D3V_S0 R2005 10KR2J-3-GP 2IN1 BOARD_ID2 R2008 Do Not Stuff DY
3D3V_S0 R2010 Do Not Stuff DY BOARD_ID1 R2009 10KR2J-3-GP WHL-U

CNV_BRI_DT
XTAL FREQUENCY SELECTION
1 = 24MHZ
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD

RO13_CFLU_20171226
BOARD_DI[2:1]=10 for WHLU

CNV_RGI_DT
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT
1 = CLKIN_XTAL_LCP
0 = XTAL_IN
PCH HAS INTERNAL 20K PU

3D3V_S5 R2001 10KR2F-2-GP 2IN1 KB_DISABLE_CPU_R
Vth(max)=1.1V
Q2001 PJT138KA-GP
ISH_KB_DISABLE
NB_MODE#
075.00138.0A7C
2nd = 075.00138.0F7C
3D3V_S5 R2050 10KR2J-3-GP 2IN1 NB_MODE# R2002 Do Not Stuff DY

1D8V_S0 R2052 Do Not Stuff DY GYRO_DRDY_ISH R2051 Do Not Stuff DY
2017/03/17

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

PCH strap pin: NRB_BIT

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 20 of 106

Main Func = PCH

40 GPPC_H18_BOOTMPC
61 WIFI_RF_EN
29 SPK_ID
61 BLUETOOTH_EN
55 TOUCH_DETECT
20 BOARD_ID2
15 GPP_H23
15 GPD7

61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WR_CLK_DP
61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1

18 PROJECT_ID0
15 GPP_H21

CPU1I 9 OF 20

CNV_WR_DN0 CR30 CNV_WR_D0N
CNV_WR_DP0 CP30 CNV_WR_D0P
CNV_WR_DN1 CM30 CNV_WR_D1N
CNV_WR_DP1 CN30 CNV_WR_D1P
CNV_WT_DN0 CN32 CNV_WT_D0N
CNV_WT_DP0 CM32 CNV_WT_D0P
CNV_WT_DN1 CP33 CNV_WT_D1N
CNV_WT_DP1 CN33 CNV_WT_D1P
CNV_WR_CLK_DN CN31 CNV_WR_CLKN
CNV_WR_CLK_DP CP31 CNV_WR_CLKP
CNV_WT_CLK_DN CP34 CNV_WT_CLKN
CNV_WT_CLK_DP CN34 CNV_WT_CLKP
CNV_WT_RCOMP CP32 CNV_WT_RCOMP#CP32
CR32 CNV_WT_RCOMP#CR32
CP20 GPP_F0/CNV_PA_BLANKING
PROJECT_ID1 CK19 GPP_F1
PROJECT_ID2 CG17 GPP_F2
SPK_ID CR14 GPP_C8/UART0_RXD
BLUETOOTH_EN CP14 GPP_C9/UART0_TXD
TOUCH_DETECT_R CN14 GPP_C10/UART0_RTS#
BOARD_ID2 CM14 GPP_C11/UART0_CTS#
CJ17 GPP_F8/CNV_MFUART2_RXD
CH17 GPP_F9/CNV_MFUART2_TXD
CF17 GPP_F23/A4WP_PRESENT
Do Not Stuff

GPP_H18/CPU_C10_GATE# CN27 GPPC_H18_BOOTMPC
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 GPP_H21
GPP_H22 CN26
GPP_H23 CM26 GPP_H23
GPP_F10 CK17
GPD7 BV35 GPD7
GPP_F3 CN20 PROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 WIFI_RF_EN
GPP_H20/IMGCLKOUT1 CH25
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN18
GPP_F15/EMMC_DATA3 CM18
GPP_F16/EMMC_DATA4 CR18
GPP_F17/EMMC_DATA5 CP18
GPP_F18/EMMC_DATA6 CM18
GPP_F19/EMMC_DATA7
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16
EMMC_RCOMP CK15 EMMC_RCOMP
GP

GPP_F: VCCPGPPF = 1.8V Only

150R2F-1-GP R2101 1
TOUCH_DETECT 1 DY 2 R2102 Do Not Stuff
R2108 200R2F-1-GP

3D3V_S0
WIFI_RF_EN 2 R2107 1 DY Do Not Stuff
Change to Dummy 20150402

3D3V_S0
Do Not Stuff 1 DY 2 R2109 BLUETOOTH_EN
3D3V_S0 R2110 10KR2J-3-GP
SPK_ID
RO13_20171023

PROJECT_ID[1:0] 01: 7000 Series
PROJECT_ID[3:2] 11: Inspiron

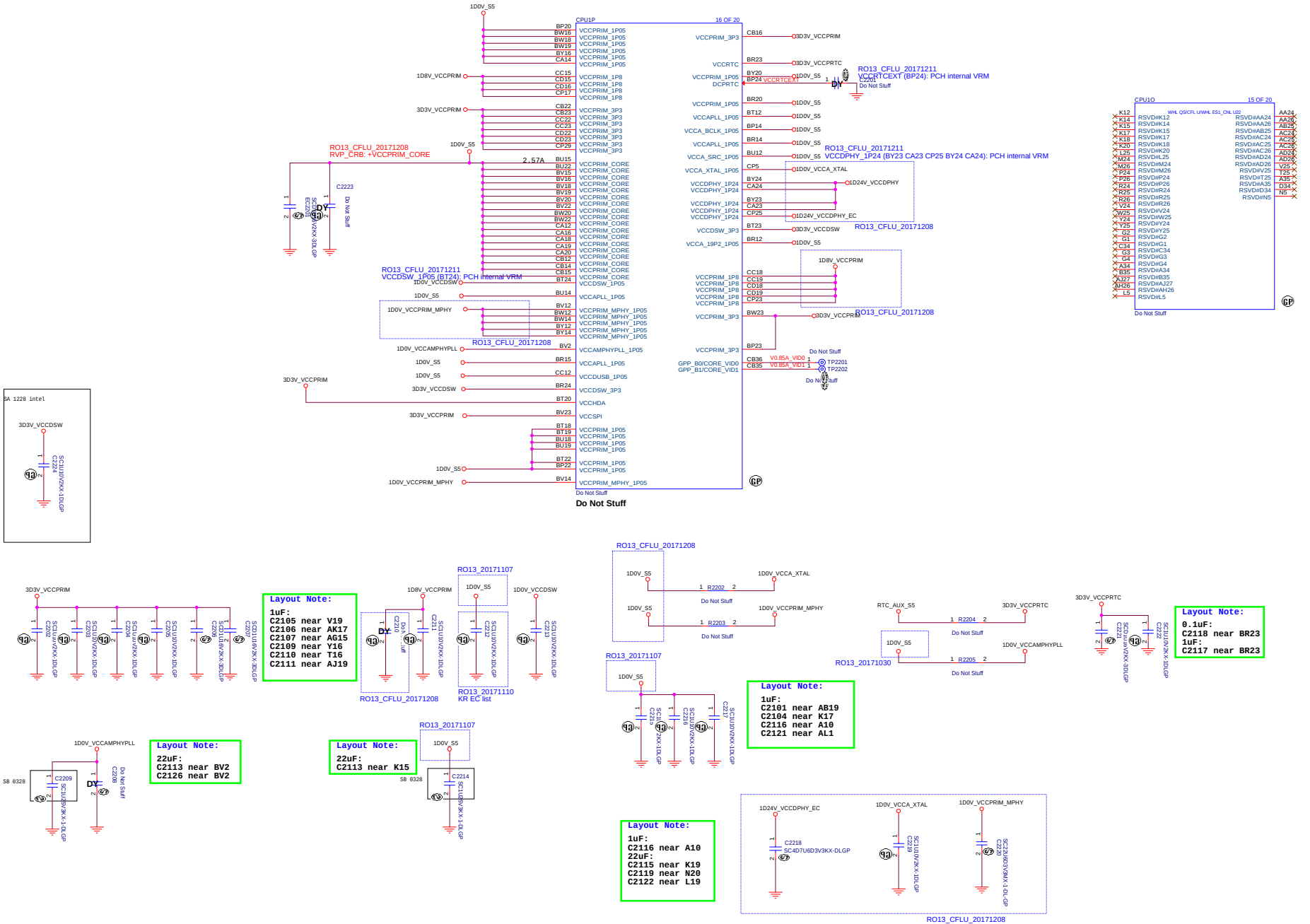
1D8V_VCCPRIM
R2111 Do Not Stuff DY
PROJECT_ID1
R2112 10KR2J-3-GP
R2113 10KR2J-3-GP
PROJECT_ID0
R2114 Do Not Stuff DY
R2115 10KR2J-3-GP
PROJECT_ID3
R2116 Do Not Stuff DY
R2117 10KR2J-3-GP
PROJECT_ID2
R2118 Do Not Stuff DY
RO13_20171025

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVi)
Size: A2
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
Sheet 21 of 106

Main Func = PCH



Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1

Layout Note:
0.1uF:
C2118 near BR23
1uF:
C2117 near BR23

Layout Note:
22uF:
C2113 near BV2
C2126 near BV2

Layout Note:
22uF:
C2113 near K15

Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

RO15/17 UMA/DIS 2IN1

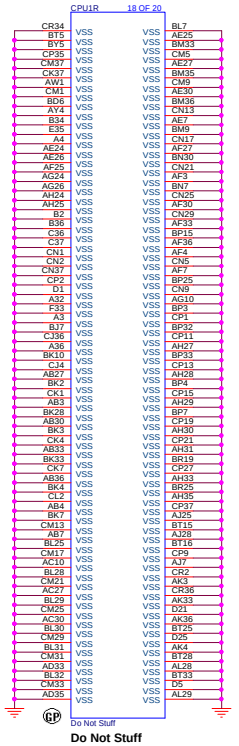
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

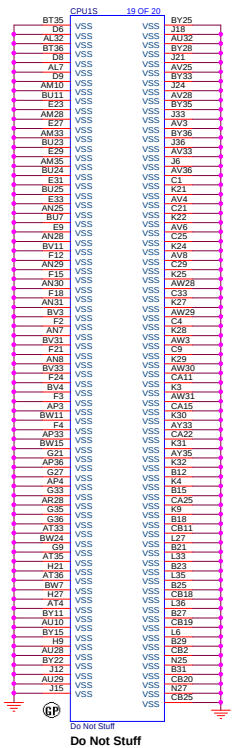
Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 22 of 106

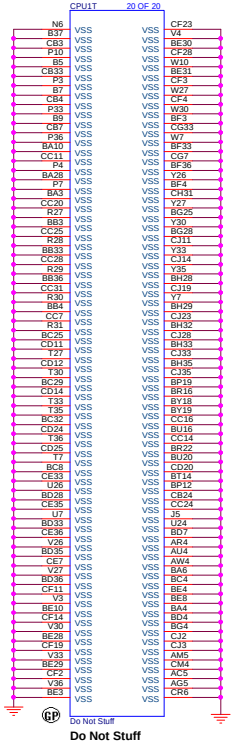
Main Func = PCH



Do Not Stuff



Do Not Stuff



Do Not Stuff

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

RO15/17 UMA/DIS 2IN1

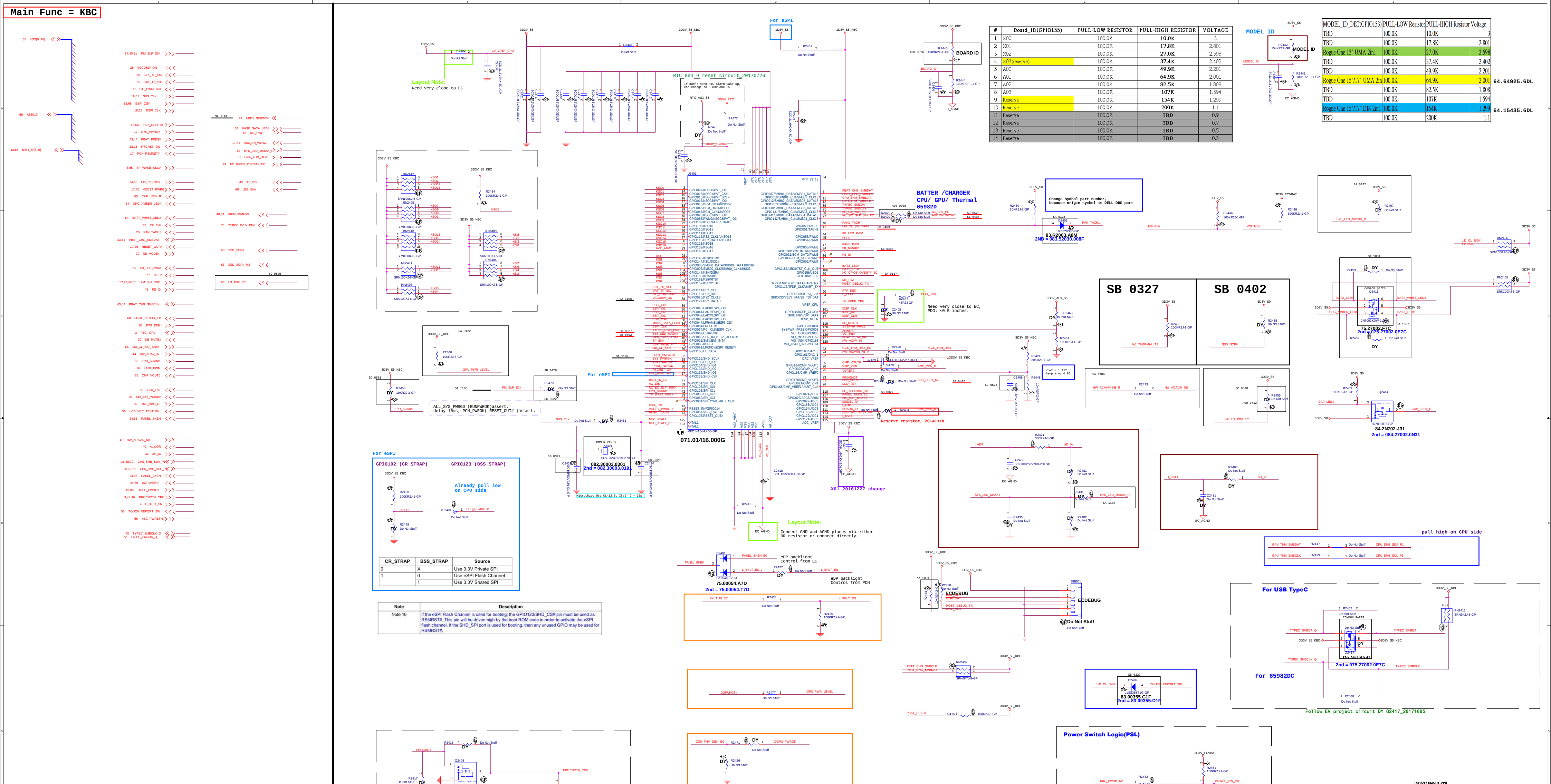
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 23 of 106

Main Func = KBC



#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

MODEL_ID_DET(GPIO153)	PULL-LOW Resistor	PULL-HIGH Resistor	Voltage	
TBD	100.0K	10.0K	3	
TBD	100.0K	17.8K	2.801	
Rogue One 13" UMA 2in1	100.0K	27.0K	2.598	
TBD	100.0K	37.4K	2.402	
TBD	100.0K	49.9K	2.201	
Rogue One 15"/17" UMA 2in	100.0K	64.9K	2.001	64.64925.6DL
TBD	100.0K	82.5K	1.808	
TBD	100.0K	107K	1.594	
Rogue One 15"/17" DIS 2in1	100.0K	154K	1.299	64.15435.6DL
TBD	100.0K	200K	1.1	

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ECIO(SMSC 1416)

Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 24 of 106

Main Func = SPI Flash

Source	QUAD/DUAL fast read	DUAL fast read	SFDP
072.25128.0B51	O	O	O
072.25127.0001	O	O	O
072.25128.0D61	O	O	O

SPI Flash ROM(16M) for PCH

072.25128.0B51
2nd = 072.25127.0001
3rd = 072.25128.0D61

RO13_CFLU_20171206
0 ohm to 33 ohm

Main Func = RTC

(R2505 量產後不要改成short pad)

29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

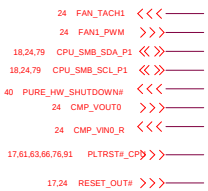
Add RTC Gen 9 reset circuit_20170726

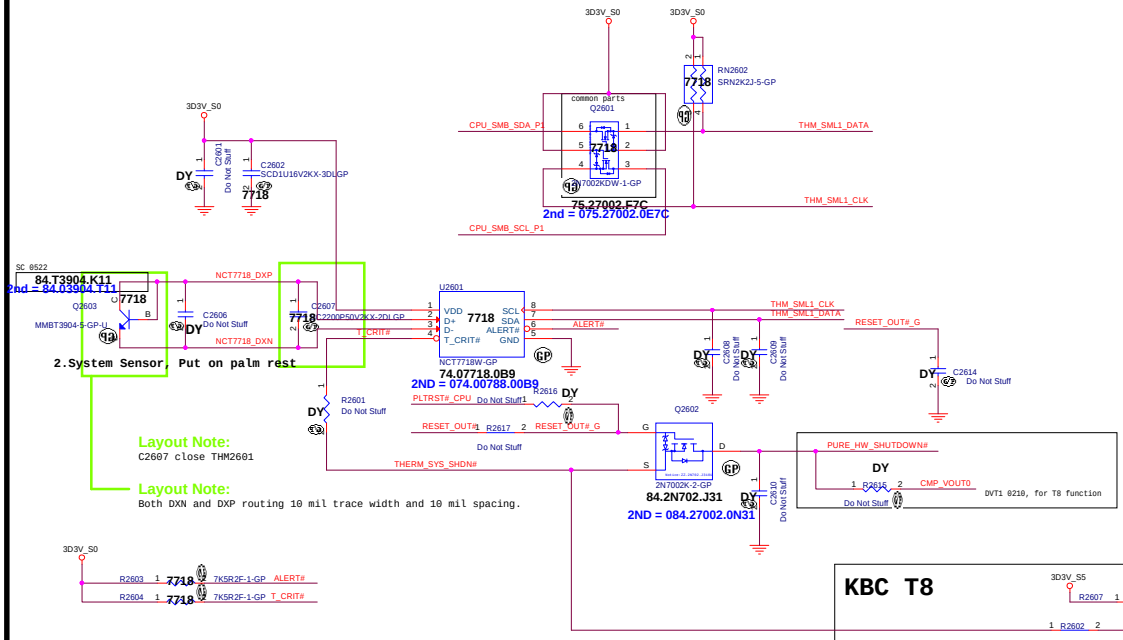
RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 25 of 106

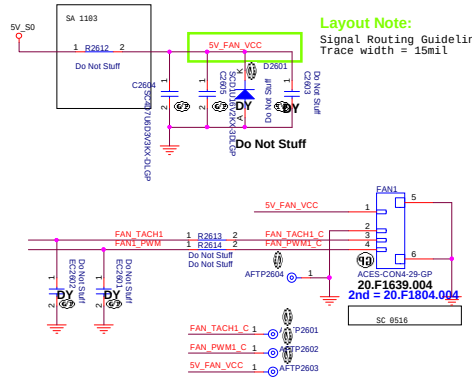
Main Func = Thermal Sensor



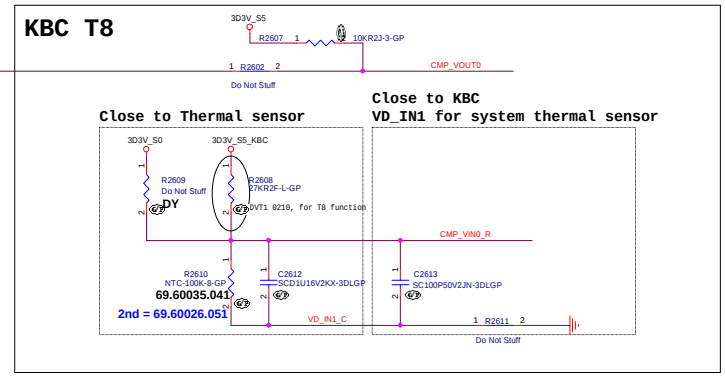


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



KBC T8



RO15/17 UMA/DIS 2IN1

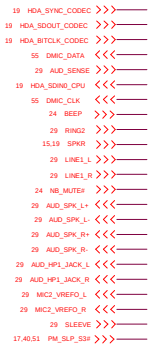
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

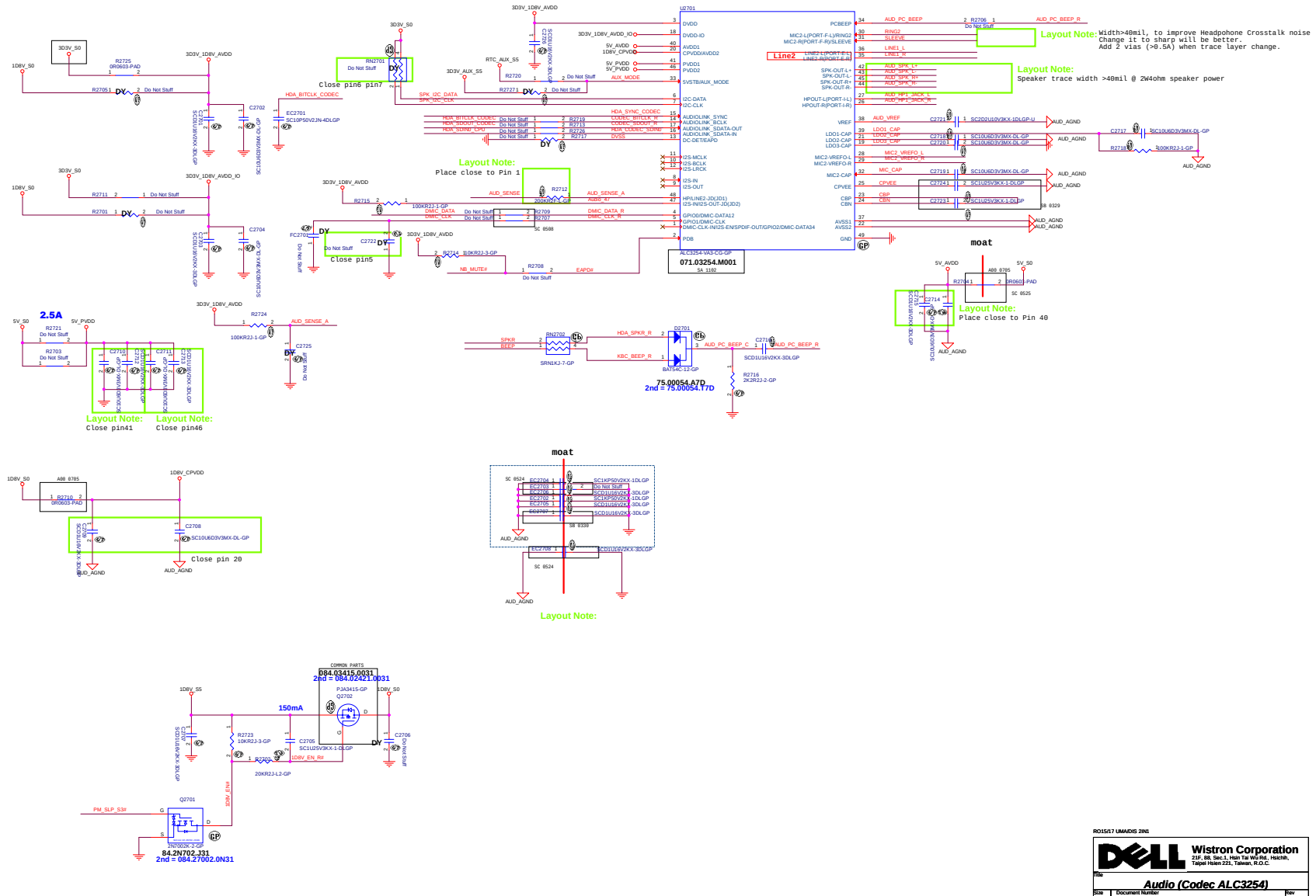
Title: INT IO (Thermal/Fan)

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 26 of 106

Main Func = Audio





RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: Audio (Codec ALC3254)

Size	Document Number	Rev
Custom	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 27 of 105

(Blanking)

Main Func = Audio

21 SPK_ID
27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R-
27 AUD_SPK_R+
27 MIC2_VREFO_R
27 MIC2_VREFO_L
27 RING2
27 LINE1_L
27 LINE1_R
27 SLEEVE

27 AUD_HP1_JACK_L
27 AUD_HP1_JACK_R
27 AUD_SENSE

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

SPK_ID 1: YG
0: FG

ACES-CON6-20-GP-U
20.F1639.006
2nd = 20.F1804.006

AFTP TESTPOINT

Layout Note:
EC2908 EC2907 should place nearby codec IC.

SB 0326 pin3/4 switch

022.10002.01H1
2nd = 022.10002.01L1
3rd = 022.10002.01Z1

Delay circuit
(JACK_PLUG_DET: on IO Board)

CLOSS TO HPMIC1

75.05125.07D
2nd = 075.52215.007D

20160812 EMI

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio (HP/SPK/MIC Jack)*
Size: A2
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
Sheet 29 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio (RSVD)

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 30 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 31 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD) (RJ45+Transfor

Size: A3 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 32 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARDREADER (SDIO/SD Conn)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 33 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB2.0 CONN)

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 34 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Conn)

Size	Document Number	Rev
	Rogue One 15"/17" WHL-U	***A00***

Date: Tuesday, July 24, 2018 Sheet 35 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB Charger)

Size	Document Number	Rev
A3	***Rogue One 15"/17" WHL-U***	***A00***

Date: Tuesday, July 24, 2018 Sheet 36 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (PCIE to USB3.0)

Size	Document Number	Rev
A4	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 37 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB (RSVD) (USB3.0 Redriver)

Size	Document Number	Rev
A4	*Rogue One 15"/17" WHL-U*	*A00*

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (RSVD)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 39 of 106

Main Func = Power Plane & Sequence

17,27,51 PM_SLP_S3#
51 VDDQ_PWRGD
17,24 VCCST_PWRGD
45 3V_5V_EN
46 VR_EN
24 ALWON
26 PURE_HW_SHUTDOWN#
17,54,66 PM_SLP_S4#
52 1D0V_S5_PWRGD
24,54 PRIM_PWRGD
17,25,45 3V_5V_PWRGD
17,24,91 PM_SLP_S0#
21 GPPC_H18_BOOTBIOSC

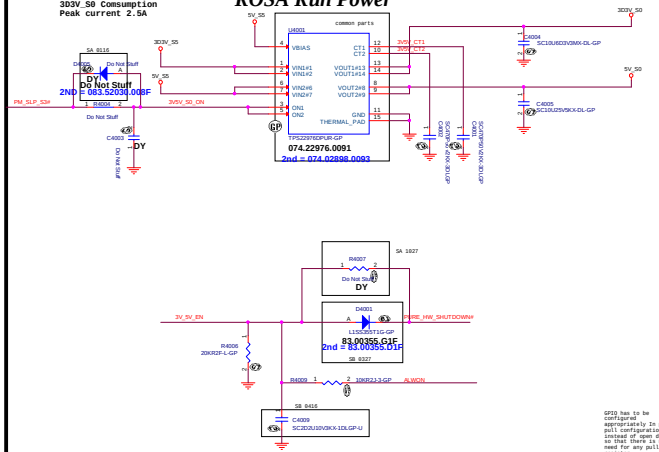
5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

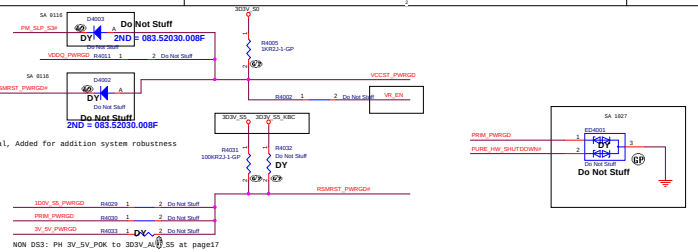
3D3V_S0 Comsumption
Peak current 2.5A

ROSA Run Power



GPIO has to be configured appropriately to push high and low instead of open drain so that there is no need for any pull up resistor.

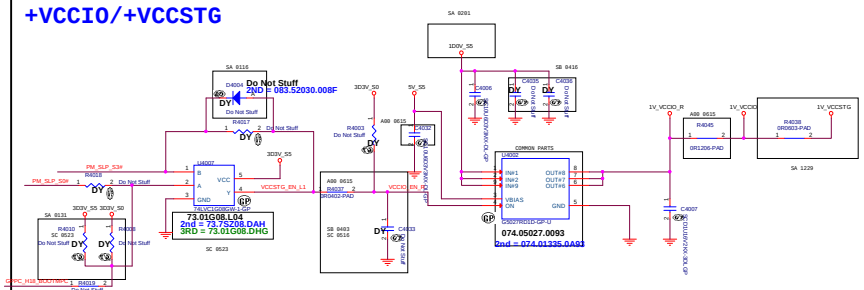
Power Good



[#543816] Optional, Added for addition system robustness

NON DS3: PH 3V_5V_POK to 3D3V_AON_S5 at page17

+VCCIO/+VCCSTG



EOPIO and EDRAM

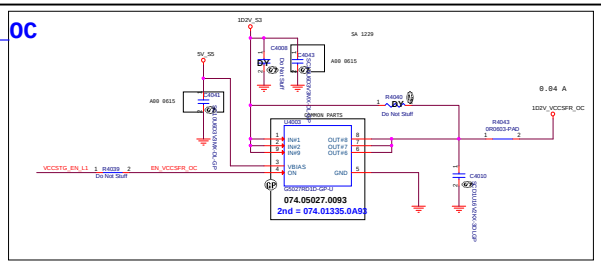
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

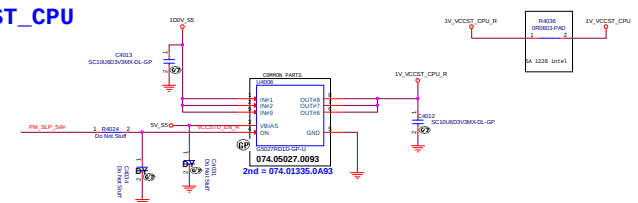
1D2V_VCCSFR_OC



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

MANAGEMENT RAIL POWER GENERATION

VCCST_CPU



+V1.8S0

RC15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: Sequence (Power Enable)

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 40 of 105

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD) (DS3/S0ix)

Size	Document Number	Rev
A4	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 41 of 106

RO15/17 UMA/DIS 2IN1

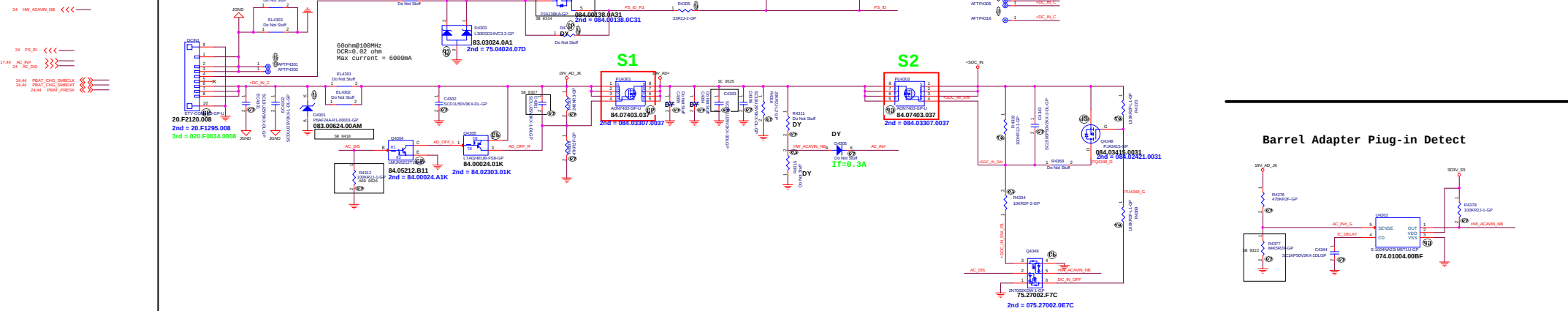
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD)*

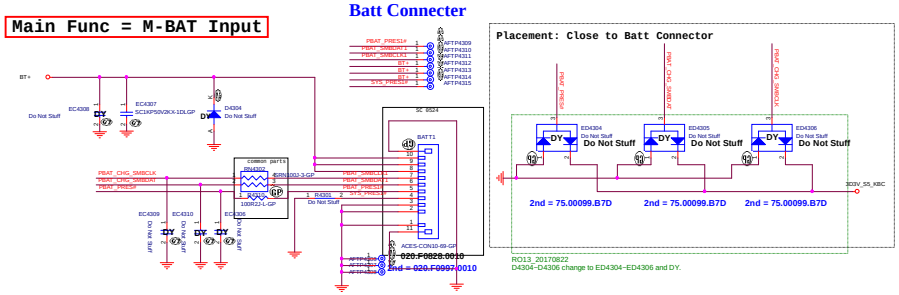
Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 42 of 106

Main Func = ADT Input



Main Func = M-BAT Input



RO15/17 LIMA/DIS 28N1

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: INT IO (ATX/ DC/ BATT Conn)

Size	Document Number	Rev
A1	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 43 of 106

Main Func = Charger

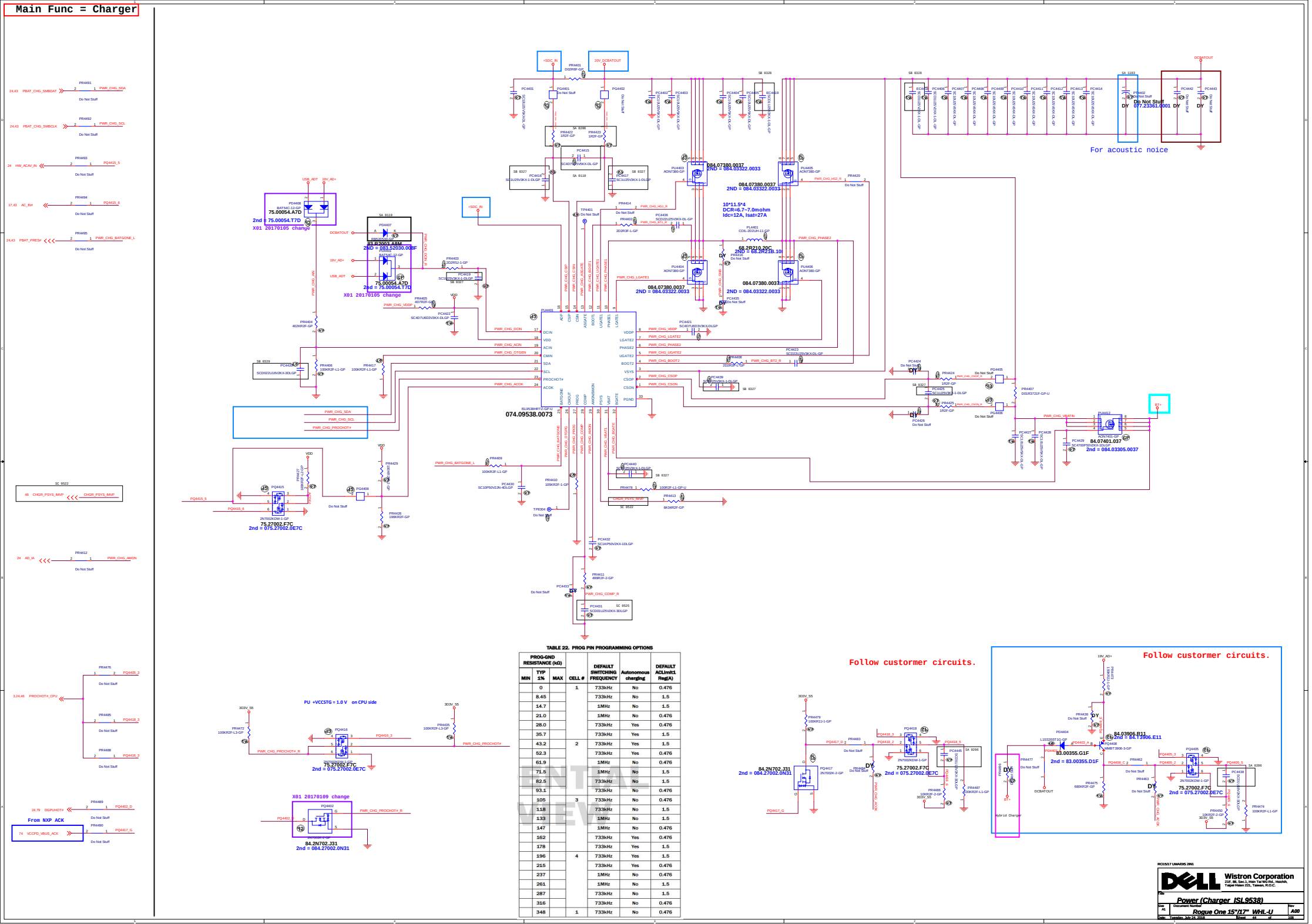


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX				
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

RC15/17 UMA/DIS 2IN1

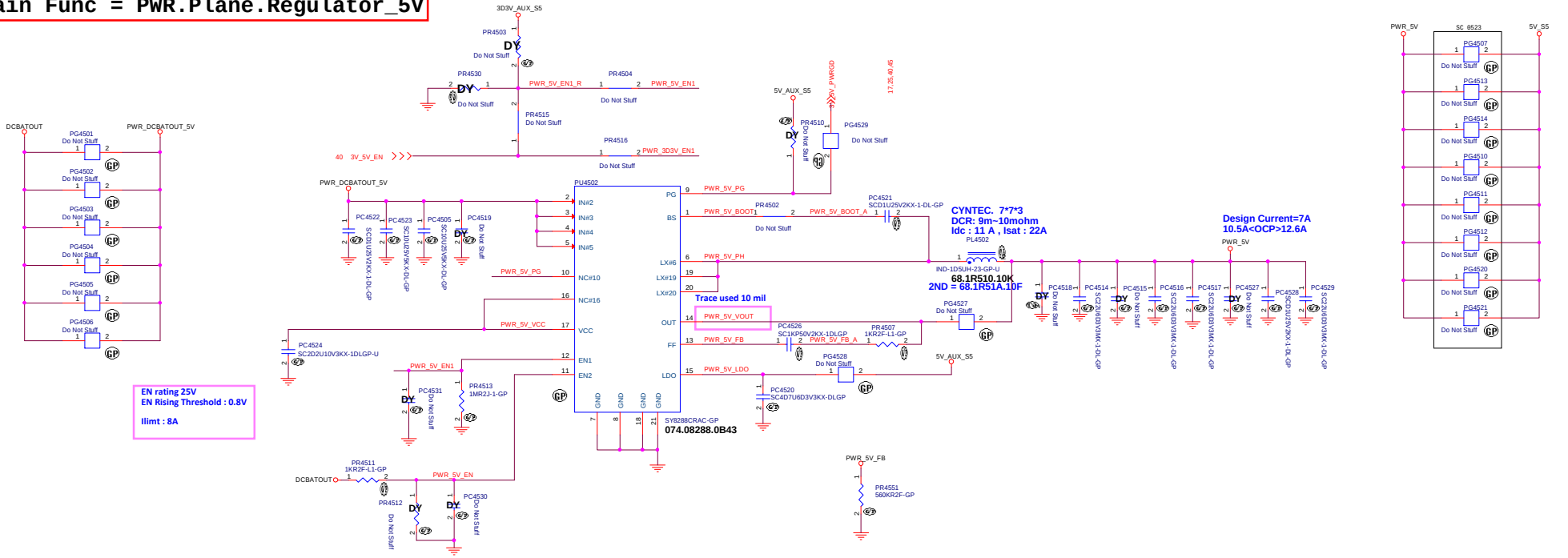
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Power (Charger_ISL9538)

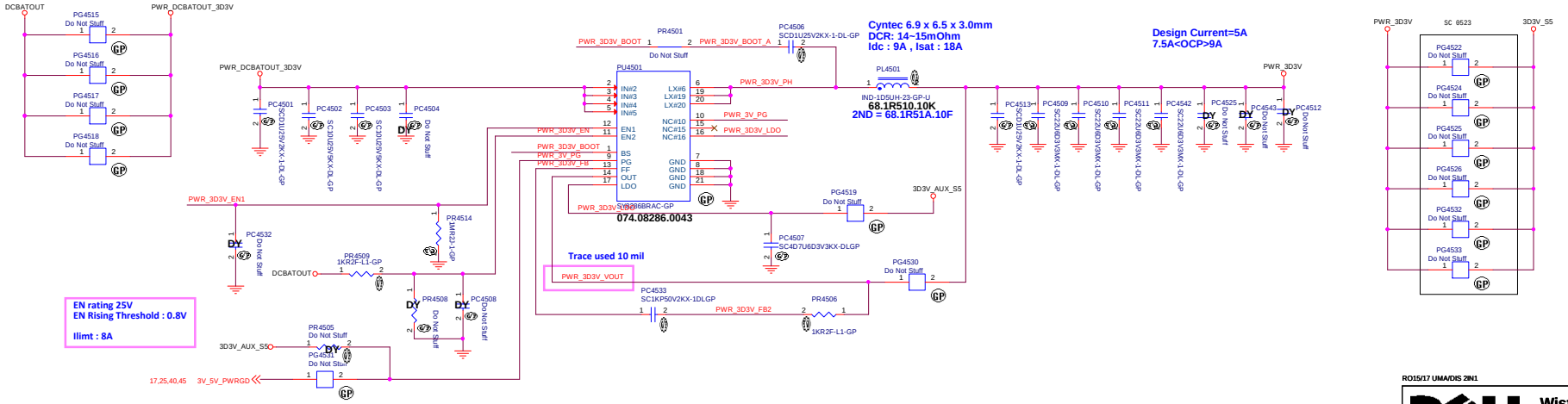
Size: A1 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 25, 2017 | Sheet 44 of 105

Main Func = PWR.Plane.Regulator_5V



Main Func = PWR.Plane.Regulator_3D3V



RO15/17 UMA/DIS 2IN1

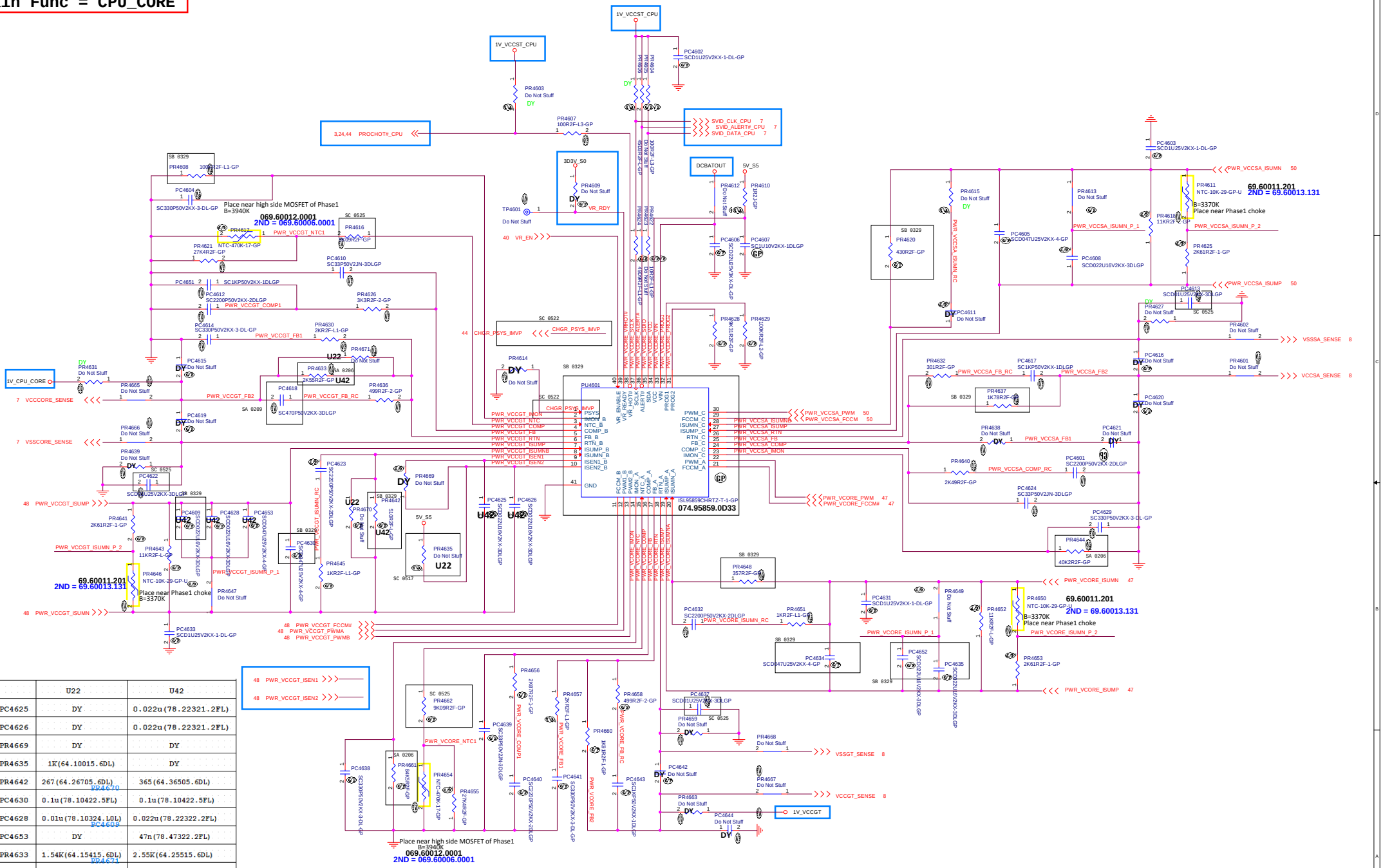
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (SY8288/8286_5V/3D3V)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 45 of 106

Main Func = CPU_CORE



	U22	U42
PC4625	DY	0.022u(78.22321.2FL)
PC4626	DY	0.022u(78.22321.2FL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL) PR4670	365(64.36505.6DL)
PC4630	0.1u(78.10422.5FL)	0.1u(78.10422.5FL)
PC4628	0.01u(78.10324.L0L) PC4603	0.022u(78.22322.2FL)
PC4653	DY	47n(78.47322.2FL)
PR4633	1.54K(64.15415.6DL) PR4671	2.55K(64.25515.6DL)
PR4608	76.8K(64.76825.6DL)	95.3K(64.95325.6DL)

RO15/17 UMA/DIS 2IN1

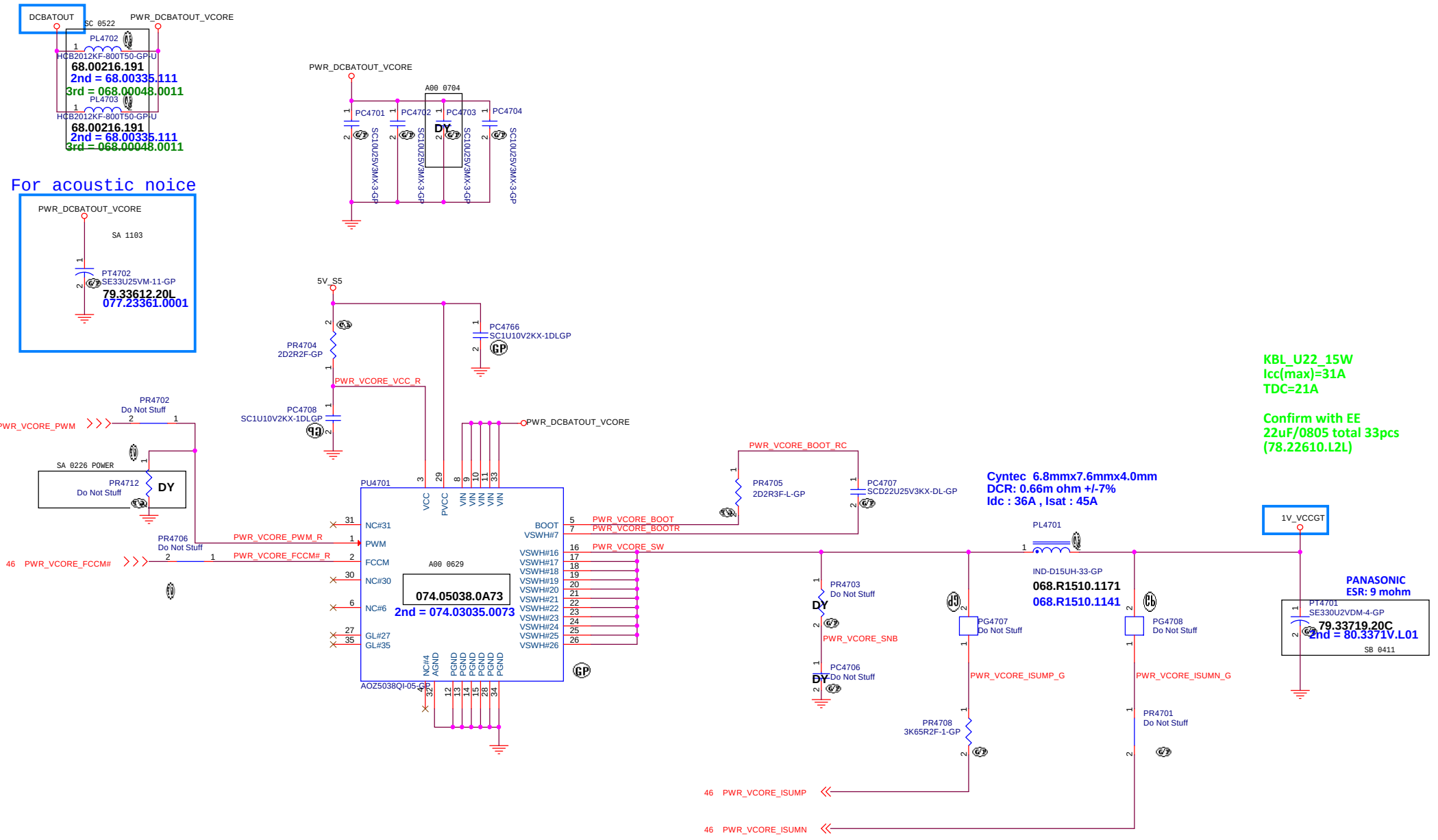
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power(ISL95859_CPUCORE(1/3))

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 46 of 106

Main Func = CPU_CORE

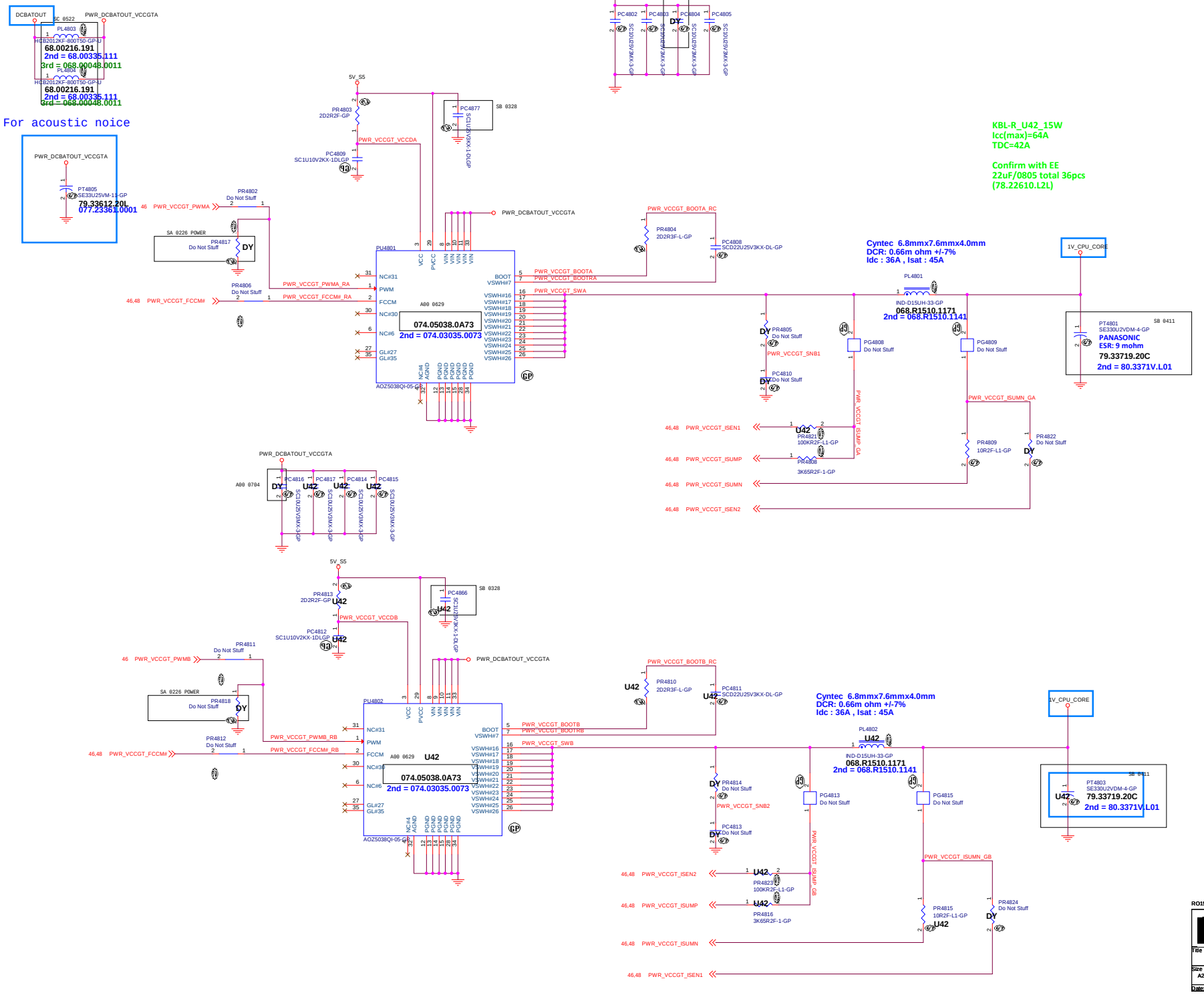


RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power(AOZ5038_CPUCORE(2/3))	
Size A3	Document Number Rogue One 15"/17" WHL-U	Rev A00
Date: Tuesday, July 24, 2018	Sheet 47 of 106	

Main Func = CPU_CORE



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power(AOZ5038_CPUCORE(3/3))

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 48 of 106

RO15/17 UMA/DIS 2IN1

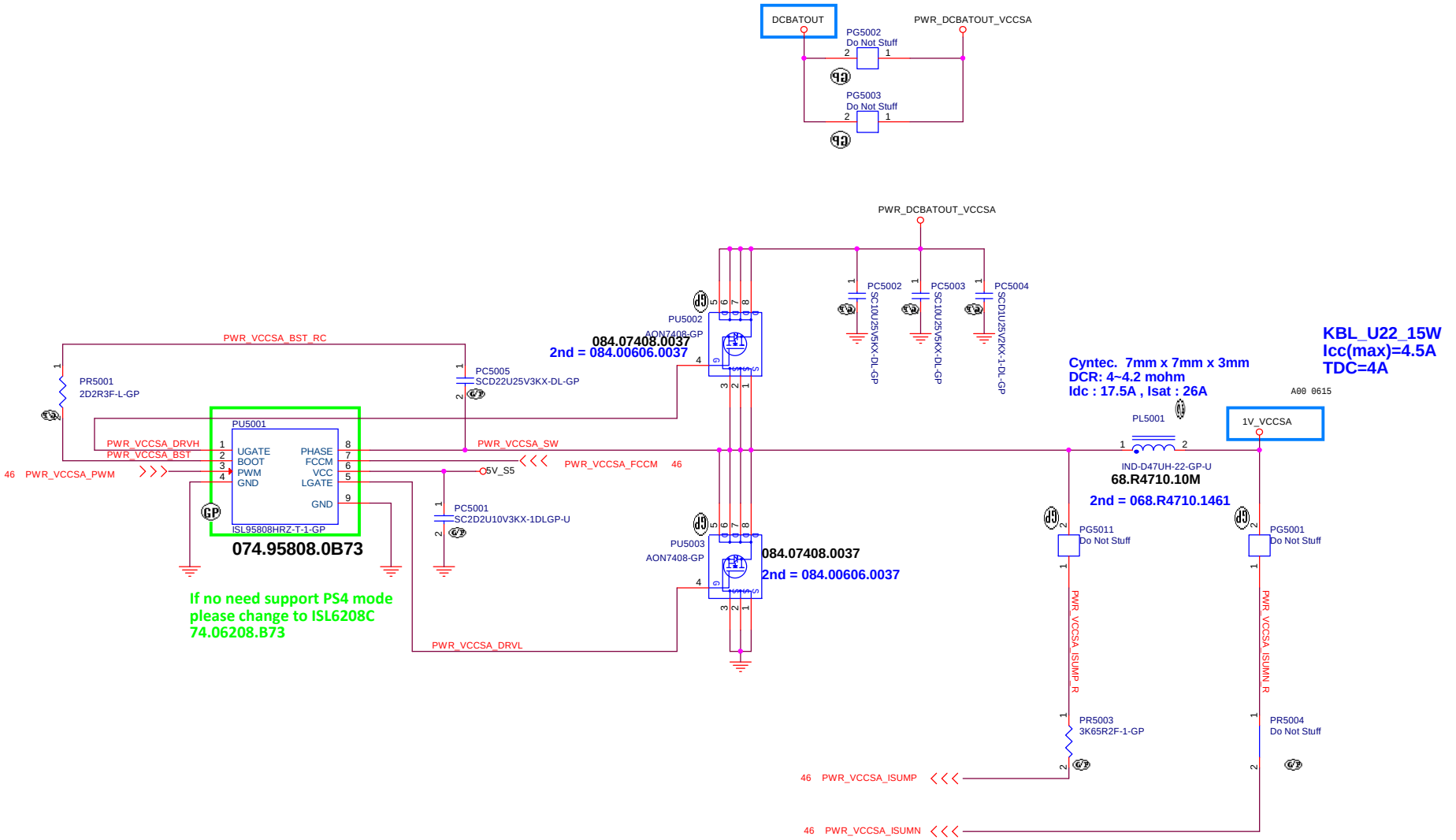
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (RSVD)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 49 of 106

Main Func = CPU_CORE

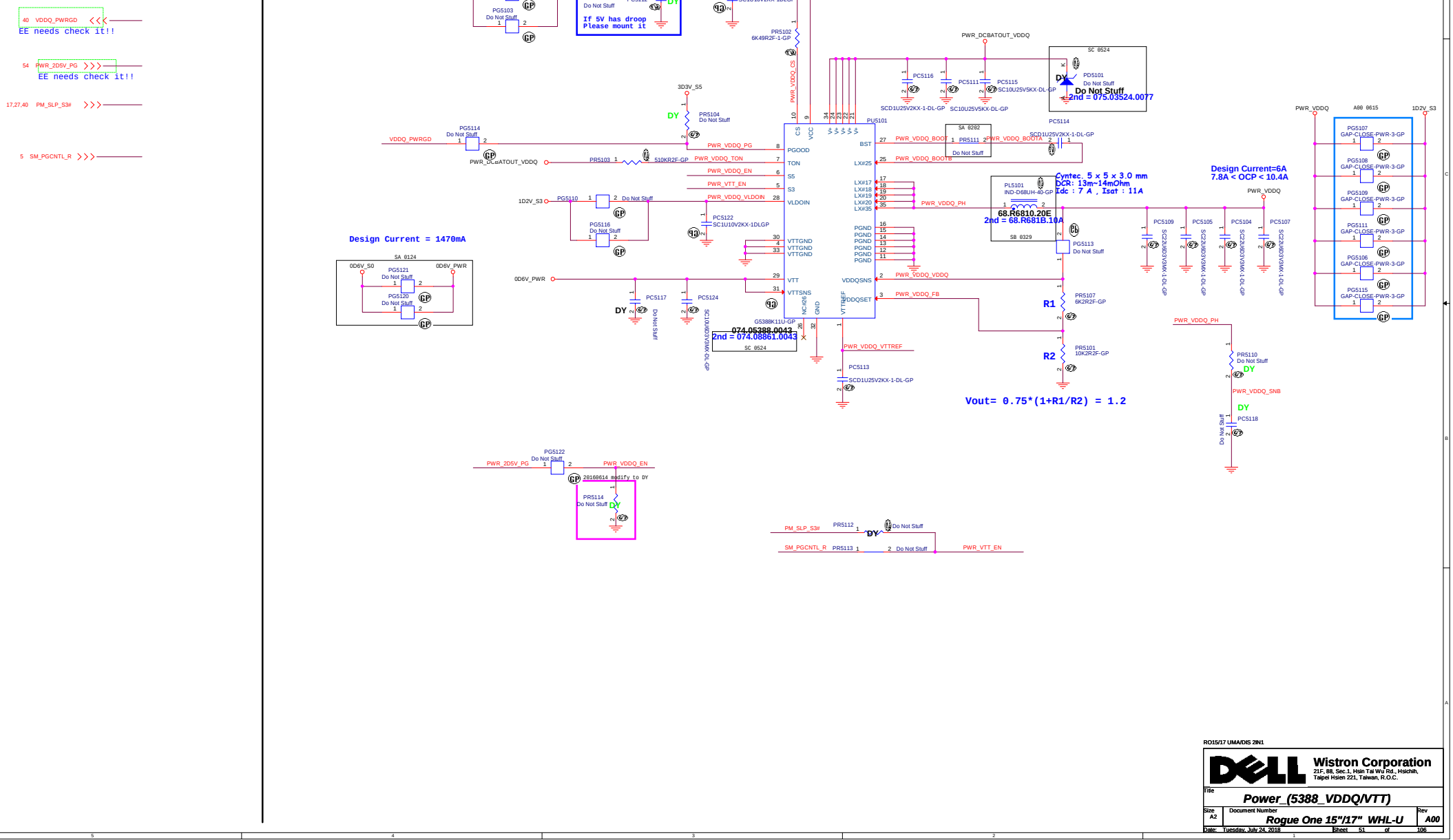


RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power (ISL95808 VCCSA)	
Size A3	Document Number Rogue One 15"/17" WHL-U	Rev A00
Date: Tuesday, July 24, 2018	Sheet 50 of 106	

Main Func = PWR.Plane.Regulator_1D2V/0D6V



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

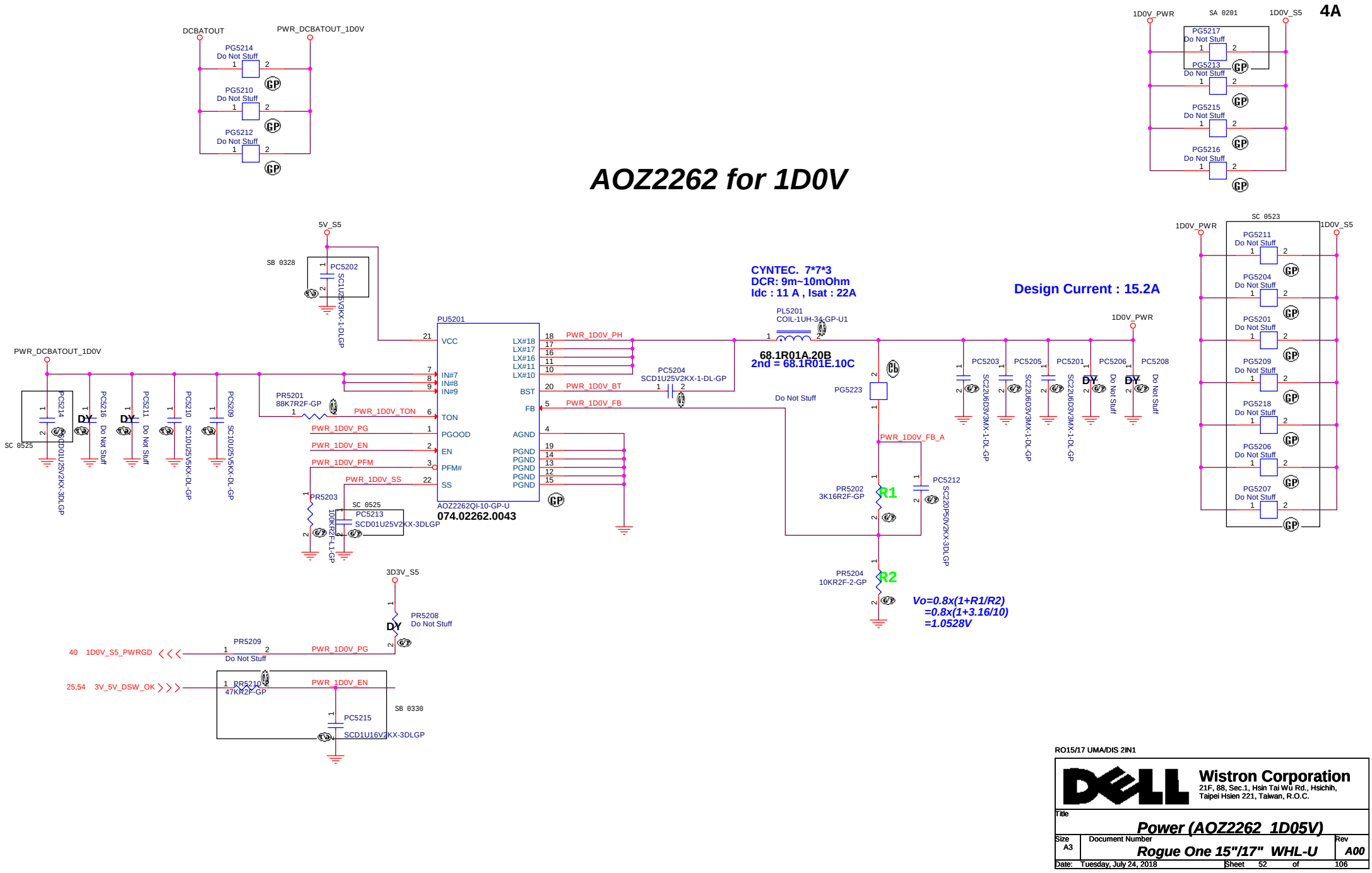
Title: Power_(5388_VDDQ/VTT)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 51 of 106

Main Func = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Power (AOZ2262 1D05V)	
Size A3	Document Number: Rogue One 15"/17" WHL-U	Rev A00
Date: Tuesday, July 24, 2018	Sheet 52 of 106	

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

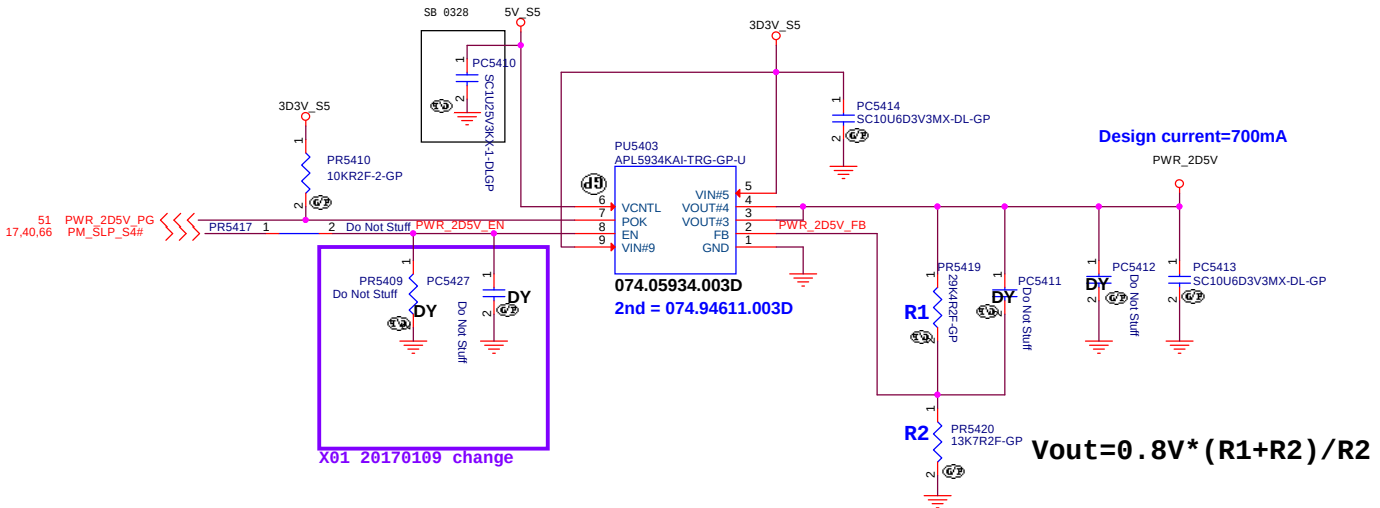
Power (RSVD(VCCIO/VCC_PRIM)

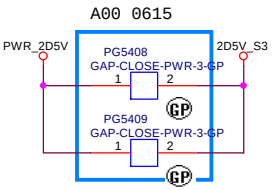
Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 53 of 106

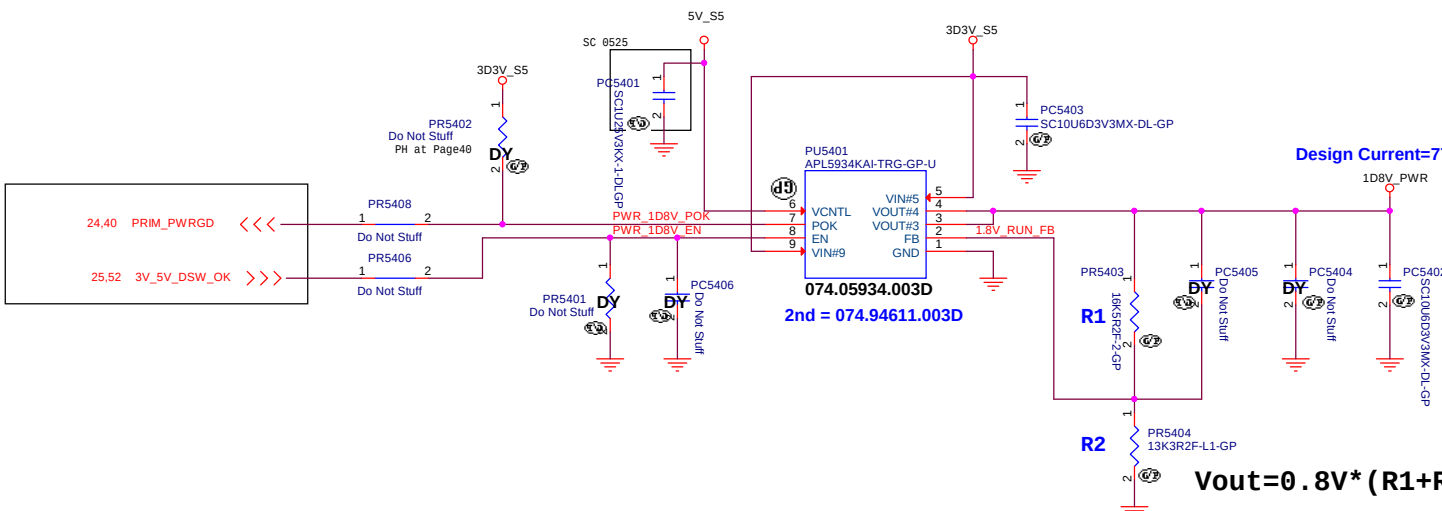
Main Func = 2D5V/ 1D8V

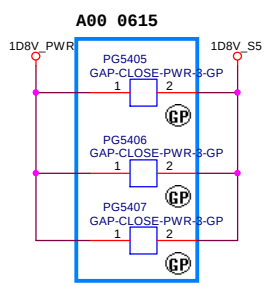
APL5934 for 2D5V





APL5934 for 1D8V_S5





RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (APL5934 1D8V/2D5V)

Size: A3 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 54 of 106

Main Func = LCD

Panel / Camera/ DMIC

Coaxial

Camera Wire

AFTP TESTPOINT

Sensor/ Touch Panel

Sensor

Touch Panel

AFTP TESTPOINT

TP	PIN DEFINE
1	VUSB_3.3V
2	NC
3	SCL
4	SDA
5	UA_INT
6	RESET
7	Report Switch
8	NC
9	GND
10	GND

CAMERA POWER

INVERTER POWER

SENSOR POWER

TOUCH PANEL POWER

EN > 1.6V
Disable < 0.4V

Design Current = 125mA

VOUT=0.8*(1+R1/R2)

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (LCD/Inverter)

Size	Document Number	Rev
Custom	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 55 of 108

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

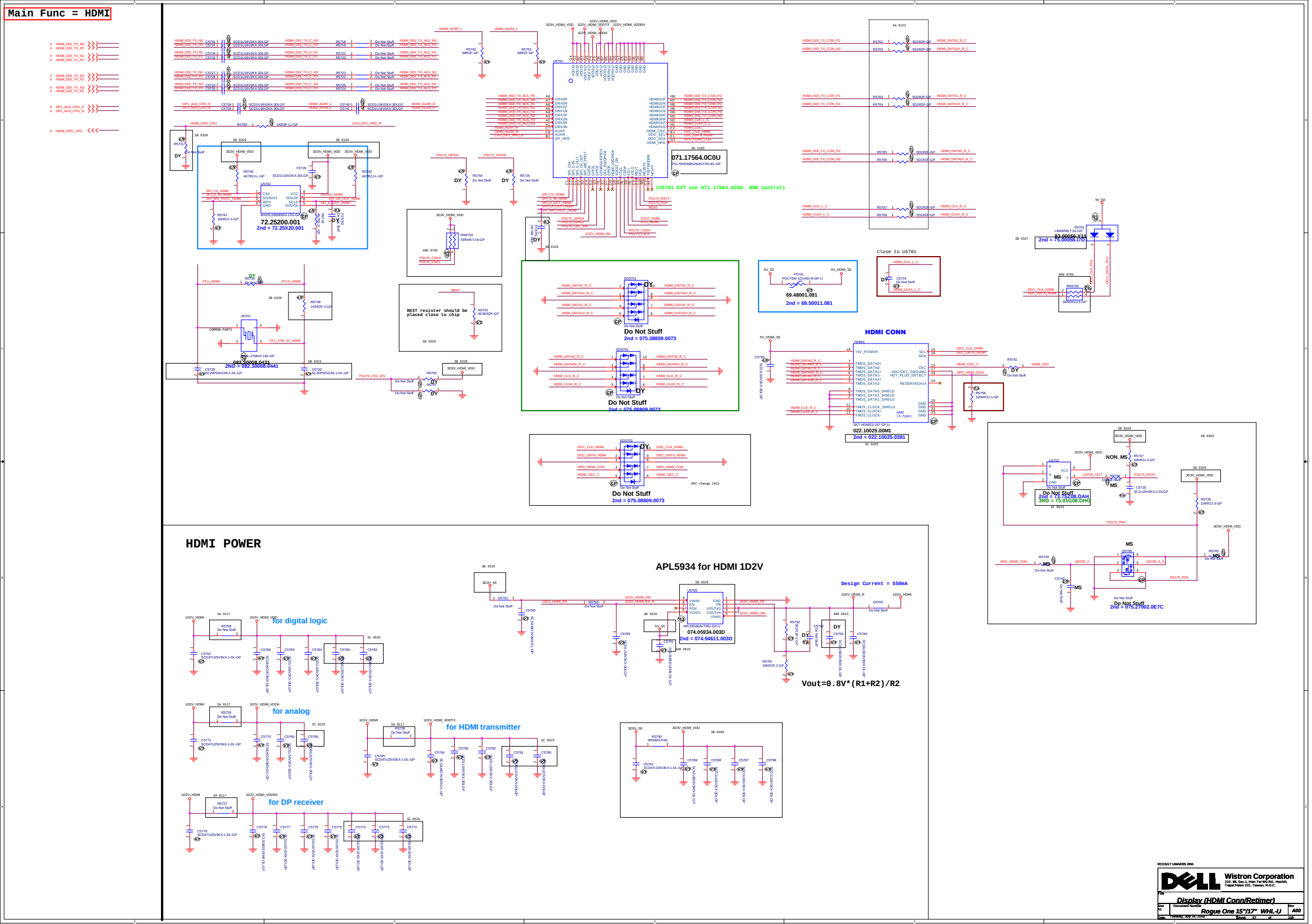
Title

Display (CRT/IR Camera)

Size	Document Number	Rev
A2	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 56 of 106

Main Func = HDMI



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display (RSVD) DP***

Size	Document Number	Rev
Custom	***Rogue One 15"/17" WHL-U***	***A00***

Date: Tuesday, July 24, 2018 Sheet 58 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

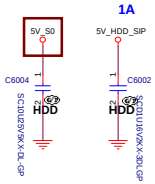
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

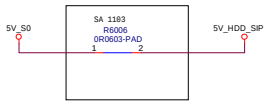
Title: *Display (RSVD) DVI*

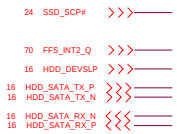
Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

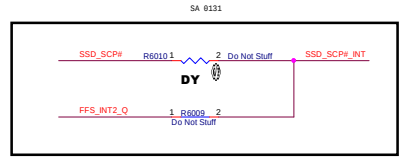
Date: Tuesday, July 24, 2018 Sheet 59 of 106

Main Func = HDD

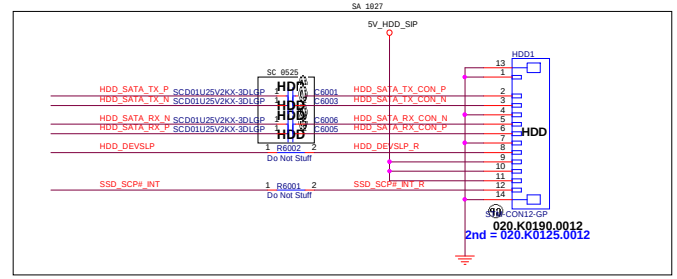




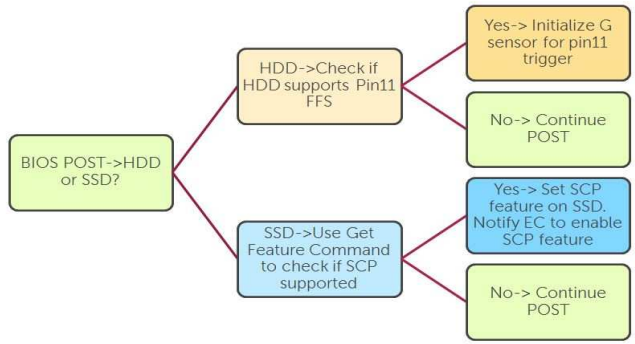


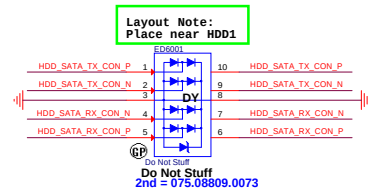


SATA HDD Connector



- BIOS today already check whether the device is HDD and whether it supports FFS before enabling sensor chip to trigger pin11. The plan is to add a check on the SSD path to decide if device supports SCP and notify EC whether to support SCP.





RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (HDD/ODD)*

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 60 of 106

Main Func = WLAN

3.3 Peak current consumption

Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply	1360	

16 BT_USB20_P
16 BT_USB20_N
17,24 AUX_EN_WOWL
21 WIFI_RF_EN
16 WLAN_PCIE_TX_C_N
16 WLAN_PCIE_TX_C_P
17,26,63,66,76,91 PLTRST#_CPU
21 BLUETOOTH_EN
18 WLAN_CLKREQ_CPU_N
18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
16 WLAN_PCIE_RX_N
16 WLAN_PCIE_RX_P
18 CLKIN_XTAL_LCP_R
19 BT_PCMOUT_CLKREQ0
19 BT_PCMFRM_RSTN
18 JIO3_PCIE_WAKE#

18,24 SUS_CLK
20 CNV_RGI_RSP
20 CNV_BRI_RSP
20 CNV_BRI_DT_R
15,20 CNV_RGI_DT_R

3D3V_S5 — 1.4A — C6103 DY — R6107 Do Not Stuff — C6101 Do Not Stuff — R6105 DY Do Not Stuff — WLAN_EN_R# — WLANPWR — R6103 Do Not Stuff DY — C6102 DY Do Not Stuff

COMMON PARTS
Do Not Stuff
2nd = 084.02421.0031
Do Not Stuff
Q6101

3D3V_S5 — R6113 0R0805-PAD — 3D3V_WLAN_S0
3D3V_S0 — R6106 DY Do Not Stuff
SA 1228 intel

3D3V_WLAN_S0 — 1.4A — SA 0206 — C6105 SCD1U16V2KX-3DLGP — C6106 SCD47U6D3VKX-1DLGP — C6104 SCD1U16V2KX-3DLGP — FC6101 DY Do Not Stuff

BT_USB20_R_P — R6111 Do Not Stuff — BT_USB20_P
SC 0425
BT_USB20_R_N — R6112 Do Not Stuff — BT_USB20_N

AUX_EN_WOWL — R6104 DY Do Not Stuff — AUX_EN_WOWL_R — Q6102 DY Do Not Stuff — WLAN_EN#

Do Not Stuff
2nd = 084.27002.0N31

3D3V_WLAN_S0 — R6101 DY Do Not Stuff — R6108 DY Do Not Stuff — WIFI_RF_EN — WIFI_RF_EN_R — D6102 Do Not Stuff DY
Do Not Stuff
2ND = 083.52030.008F
SA 0116

3D3V_WLAN_S0 — R6102 DY Do Not Stuff — R6109 DY Do Not Stuff — BLUETOOTH_EN — BLUETOOTH_EN_R — D6101 Do Not Stuff DY
Do Not Stuff
2ND = 083.52030.008F
SA 0116

WIFI_RF_EN — R6101 DY Do Not Stuff

SA 0131 — R6114 10KR2J-3-GP — CLKIN_XTAL_LCP_R — SA 1229 intel

X02 20170316 change

WLAN1

76	76	77	77
74	3_3VAUX	GND	75
72	3_3VAUX	RESERVED#73	73
70	RESERVED#70	RESERVED#71	71
68	RESERVED#68	GND	69
66	RESERVED#66	RESERVED#67/2ND_LANE_PERN1	67
64	GPIO0_NFC_RESET#/MGPIO7	RESERVED#65/2ND_LANE_PERP1	65
62	NFC_I2C_IRQ/MGPIO5	GND	63
60	NFC_I2C_SM_CLK	RESERVED#61/2ND_LANE_PETN1	61
58	NFC_I2C_SM_DATA	RESERVED#59/2ND_LANE_PETP1	59
56	W_DISABLE#1	GND	57
54	RESERVED#54/W_DISABLE#2	PEWAKE0#	55
52	PERST0#	CLKREQ0#	53
50	SUSCLK_32KHZ	GND	51
48	COEX1	REFCLKN0	49
46	COEX2	REFCLKP0	47
44	COEX3	GND	45
42	CLINK_CLK	PERN0	43
40	CLINK_DATA	PERP0	41
38	CLINK_RESET	GND	39
36	UART_CTS	PETN0	37
34	UART_RTS	PETP0	35
32	UART_TX	GND	33
22	UART_RX	SDIO_RESET	23
20	UART_WAKE	SDIO_WAKE	21
18	GND	SDIO_DAT3	19
16	LED#2	SDIO_DAT2	17
14	PCM_OUT	SDIO_DAT1	15
12	PCM_IN	SDIO_DAT0	13
10	PCM_SYNC	SDIO_CMD	11
8	PCM_CLK	SDIO_CLK	9
6	LED#1	GND	7
4	3_3VAUX	USB_D-	5
2	3_3VAUX	USB_D+	3
		GND	1
NP2	NP2	NP1	NP1

NGFF_KEY_E_75P
SKT-MINI67P-2-GP-U
62.10043.I91
2nd = 062.10003.0B11
SA 1212 For CNVi

CNV_WT_CLK_DP_R — R6129 Do Not Stuff — CNV_WT_CLK_DP
CNV_WT_CLK_DN_R — R6130 Do Not Stuff — CNV_WT_CLK_DN
CNV_WT_DP0_R — R6126 Do Not Stuff — CNV_WT_DP0
CNV_WT_DN0_R — R6131 Do Not Stuff — CNV_WT_DN0
CNV_WT_DP1_R — R6128 Do Not Stuff — CNV_WT_DP1
CNV_WT_DN1_R — R6127 Do Not Stuff — CNV_WT_DN1
JIO3_PCIE_WAKE#_R — R6110 Do Not Stuff — JIO3_PCIE_WAKE#
WLAN_CLKREQ_CPU_N — Do Not Stuff
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
WLAN_PCIE_RX_N
WLAN_PCIE_RX_P
WLAN_PCIE_TX_N — C6115 — SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_C_N
WLAN_PCIE_TX_P — C6116 — SCD1U16V2KX-3DLGP — WLAN_PCIE_TX_C_P
CNV_WR_CLK_DP_R — R6124 Do Not Stuff — CNV_WR_CLK_DP
CNV_WR_CLK_DN_R — R6122 Do Not Stuff — CNV_WR_CLK_DN
CNV_WR_DP0_R — R6120 Do Not Stuff — CNV_WR_DP0
CNV_WR_DN0_R — R6125 Do Not Stuff — CNV_WR_DN0
CNV_WR_DP1_R — R6121 Do Not Stuff — CNV_WR_DP1
CNV_WR_DN1_R — R6123 Do Not Stuff — CNV_WR_DN1
BT_USB20_R_N
BT_USB20_R_P

SUS_CLK — R6117 33R2J-2-GP — SUSCLK_WLAN
SA 1228 intel

CNV_RGI_RSP — R6118 22R2J-2-GP — CNV_RGI_RSP_R — CNV_RGI_DT_R
SA 0109
CNV_BRI_RSP — R6132 22R2J-2-GP — CNV_BRI_RSP_R — CNV_BRI_DT_R

BT_PCMOUT_CLKREQ0
BT_PCMFRM_RSTN
SC 0517 — R6134 75KR2F-GP — R6133 DY Do Not Stuff
SA 1229 intel

WIFI_RF_EN_R
BLUETOOTH_EN_R
PLTRST#_CPU
SUSCLK_WLAN

AFTP TESTPOINT

JIO3_PCIE_WAKE#_R — AFTP6123
WLAN_CLKREQ_CPU_N — AFTP6124
BT_PCMFRM_RSTN — AFTP6137
BT_PCMOUT_CLKREQ0 — AFTP6138
SUSCLK_WLAN — AFTP6143
3D3V_WLAN_S0 — AFTP6113
PLTRST#_CPU — AFTP6108
WIFI_RF_EN_R — AFTP6110
BLUETOOTH_EN_R — AFTP6112

1D8V_S5 — SB 0326 — R6115 20KR2J-L2-GP — CNV_BRI_DT_R

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)
Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 61 of 106

(Blanking)

RO15/17 UMA/DIS 2IN1

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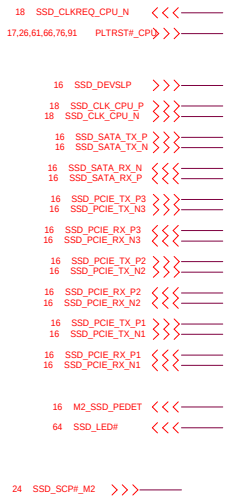
Title

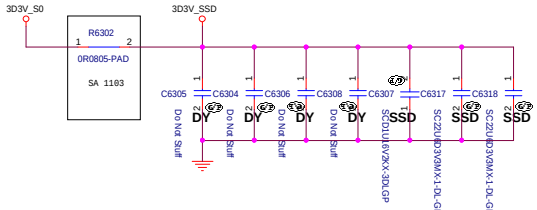
INT IO (RSVD) WWAN

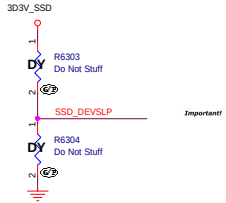
Size	Document Number	Rev
A4	***Rogue One 15"/17" WHL-U***	***A00***

Date: Tuesday, July 24, 2018 Sheet 62 of 106

Main Func = SSD M.2







Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

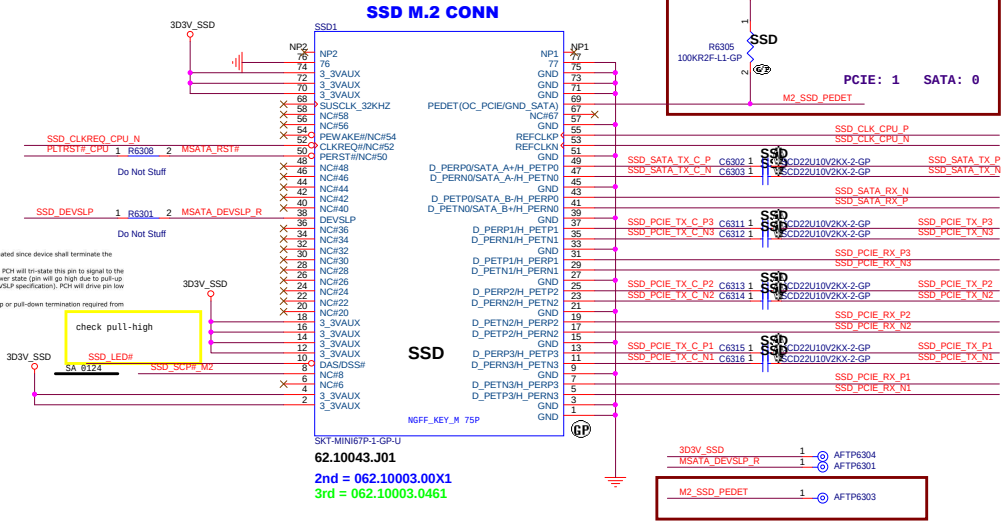


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (SSD M.2/ eMMC)

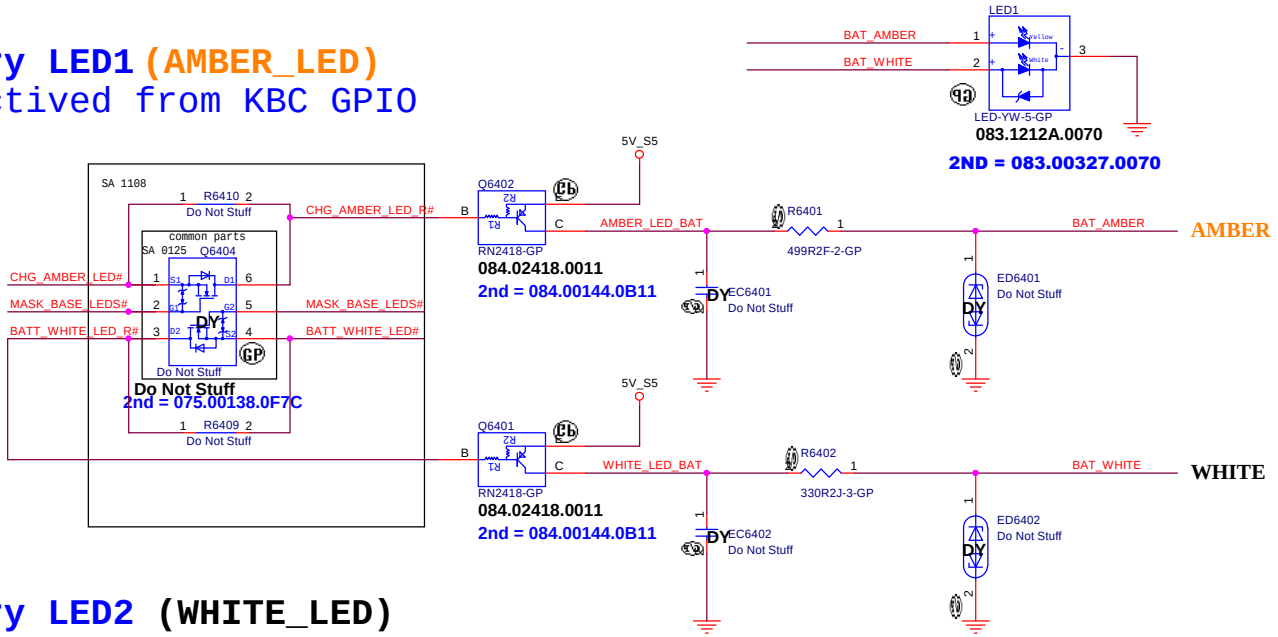
Size: Custom | Document Number: Rogue One 15"/17" WHL-UA00 | Rev: 00

Date: Tuesday, July 24, 2018 | Sheet 63 of 106

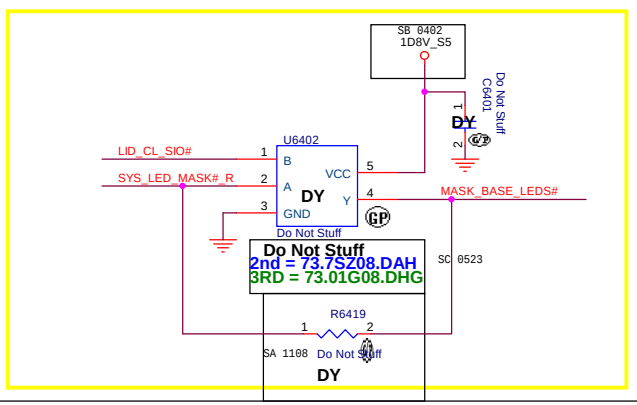
Main Func = Power BTN

24 CHG_AMBER_LED#
24 BATT_WHITE_LED#
24,66 LID_CL_SIO#
24 SYS_LED_MASK#_R

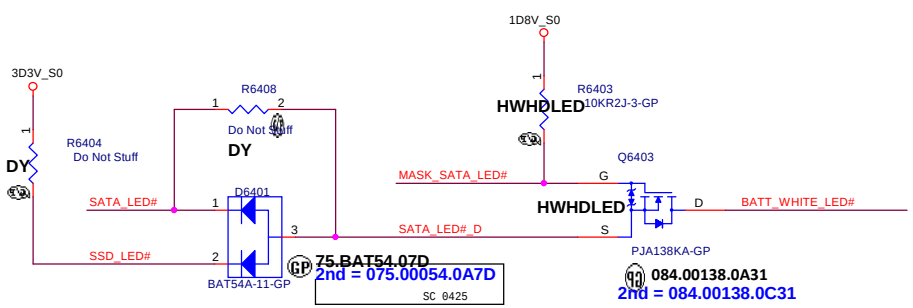
Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO



16 SATA_LED#
63 SSD_LED#
24 MASK_SATA_LED#



RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 64 of 106

Main Func = Keyboard

24 KSI[0..7]
24 KSO[0..18]

3,24 TP_WAKE_KBC#
24 PTP_DIS#
24 TP_EN#
24 CLK_TP_SIO
24 DAT_TP_SIO
20 CPU_I2C_SCL_P0
20 CPU_I2C_SDA_P0
19 KB_LED_BL_DET
20 KB_DET#
24 KB_LED_PWM
24 CAP_LED#_R

KB Backlight Power Consumption: 285mA max.

5V_S0 — F6501 POLYSW-1D1A6V-9GP — 2=5V_KB_BL_L — R6501 Do Not Stuff — 5V_KB_BL
C6501 SCD1U16V2KX-3DLGP — KBBL
69.48001.081
2nd = 69.50011.081
KBBL COMMON PARTS

5V_KB_BL — KBBL1 — KBBL
KB_LED_DET_C
KB_BL_CTRL#
EC6505 EC6506 Do Not Stuff
ACES-CON4-90-GP-U
020.K0298.0004
2nd = 020.K0311.0004

AFTP TESTPOINT
5V_KB_BL — AFTP6529
KB_BL_CTRL# — AFTP6530
KB_LED_DET_C — AFTP6538

AFTP6567 — KB1
KB_DET# — KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0
KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
CAP_LED — AFTP6541
ACES-CON30-28-GP
020.K0236.0030
2nd = 020.K0210.0030

KB_BL_CTRL# — Q6501 PJA3402-R1-00001-GP — KBBL
KB_LED_PWM — R6509 Do Not Stuff — DY
084.03402.0031
2nd = 084.02306.0031
A00 0622

KB_LED_BL_DET — R6507 51KR2J-1-GP — KBBL
KB_LED_DET_C — R6508 100KR2J-1-GP — DY — C6504 Do Not Stuff

CAP LED Control
LOW actived from KBC GPIO

CAP_LED#_R — R6512 Do Not Stuff — CAP_LED_R# — Q6505 RN2418-GP — CAP_LED_Q — R6513 — CAP_LED 1KR2J-1-GP
5V_S5
084.02418.0011
2nd = 084.00144.0B11
CAP_LED_Q — EC6507 Do Not Stuff

Main Func = TPAD

COMMON PARTS
3D3V_S0 — 084.03415.0031
2nd = 084.02421.0031
PJA3415-GP Q6502
NON TP_WAKE — R6502 Do Not Stuff — 3D3V_TP_VDD
Q6502_D — R6514 Do Not Stuff
C6502 SCD1U16V2KX-3DLGP
TP_WAKE — TP_EN# — R6504 20KR2F-L-GP — TP_ON#_GATE

TP_VDD Discharge Circuit
TP_ON#_GATE — Q6503 2N7002K-2-GP — TP_WAKE
3D3V_TP_VDD — R6503 100KR3J-4-GP — TP_WAKE — Q6205_Q
84.2N702.J31
2nd = 084.27002.0N31

GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

PS2
I2C

3D3V_TP_VDD — RN6501 SRN10KJ-L-GP — A00 0629
CLK_TP_SIO — TPCLK_C
DAT_TP_SIO — TPDAT_C
CPU_I2C_SCL_P0 — I2C0_SCL_R
CPU_I2C_SDA_P0 — I2C0_SDA_R
RN6502 SRN33J-5-GP-U — R6505 R6506 Do Not Stuff — NON TP_WAKE
EC6501 Do Not Stuff — EC6502 EC6503 EC6504 Do Not Stuff

3D3V_TP_VDD — C6505 SCD1U16V2KX-3DLGP
TPAD1 — I2C0_SDA_R I2C0_SCL_R TP_WAKE_KBC# PTP_DIS# TPDAT_C TPCLK_C
PTWO-CON8-16-GP
AFTP6540
020.K0255.0008
2nd = 020.K0151.0008

AFTP TESTPOINT
3D3V_TP_VDD — AFTP6531
TPCLK_C — AFTP6532
TPDAT_C — AFTP6533
I2C0_SCL_R — AFTP6534
I2C0_SDA_R — AFTP6535
TP_WAKE_KBC# — AFTP6536
PTP_DIS# — AFTP6537
Change pindefine DVT1 0218 1330

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

5V_S0 — A00 0609 — R6510 Do Not Stuff — 3D3V_TP_VDD
RN6503 SRN2K2J-5-GP — TP_WAKE
Q6504 common parts — CPU_I2C_SCL_P0 — I2C0_SCL_R — CPU_I2C_SDA_P0 — I2C0_SDA_R — TP_WAKE
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

X02 0415
3D3V_TP_VDD — R6511 10KR2J-3-GP — TP_WAKE_KBC#

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)
Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00
Date: Tuesday, July 24, 2018 | Sheet 65 of 106

Main Func = IO Connector

16 CARD1_USB20_N
16 CARD1_USB20_P
24,64 LID_CL_SIO#
24 LID_CL_SIO_TAB#
24 KBC_PWRBTN#
17,26,61,63,76,91 PLTRST#_CPU
16 USB2_USB20_P
16 USB2_USB20_N
16 USB1_USB20_P
16 USB1_USB20_N
16 USB1_USB30_RX_N
16 USB1_USB30_RX_P
16 USB1_USB30_TX_N
16 USB1_USB30_TX_P
16 USB2_USB30_RX_N
16 USB2_USB30_RX_P
16 USB2_USB30_TX_N
16 USB2_USB30_TX_P
17,40,54 PM_SLP_S4#
24 U3_PD#_EC
SC 0525
24 FPR_SCAN#
24 USB_EN#
16 USB_OC1#
16 FP1_USB20_N
16 FP1_USB20_P

IOBD1
STAR-CON50-GP
020.F0341.0050
2nd = 020.F0285.0050
SB 0419
SA 1213
SA 1027
SA 1107
USB1_USB20_P
USB1_USB20_N
USB2_USB20_P
USB2_USB20_N
USB2_USB30_RX_P
USB2_USB30_RX_N
USB2_USB30_TX_P
USB2_USB30_TX_N
USB1_USB30_RX_P
USB1_USB30_RX_N
USB1_USB30_TX_P
USB1_USB30_TX_N
CARD1_USB20_P
CARD1_USB20_N
FP1_USB20_P
FP1_USB20_N
U3_PD#_EC
FPR_SCAN#
USB_EN#
USB_OC1#
LID_CL_SIO#
LID_CL_SIO_TAB#
KBC_PWRBTN#
PM_SLP_S4#
5V_S5
3D3V_S0
3D3V_S5

AFTP TESTPOINT

AFTP6603 AFTP6604 AFTP6605 AFTP6606 AFTP6607 AFTP6608 AFTP6609 AFTP6610
AFTP6619 AFTP6620 AFTP6621 AFTP6622 AFTP6623 AFTP6624 AFTP6625
AFTP6626 AFTP6627 AFTP6628 AFTP6629 AFTP6630
AFTP6631 AFTP6632
AFTP6633 AFTP6634

3D3V_S5
R6604
100KR2J-1-GP
LID_CL_SIO_TAB#

EMI Reserve , 20141118

KBC_PWRBTN#
PLTRST#_CPU
EC6601
EC6602
Do Not Stuff

KBC_PWRBTN#
PWSW1
Do Not Stuff
DEBUG
Do Not Stuff

AFTP TESTPOINT

KBC_PWRBTN#
AFTP6601
AFTP6602

SA 1025
ED6602
USB2_USB30_RX_P
USB2_USB30_RX_N
USB2_USB30_TX_P
USB2_USB30_TX_N
DY
Do Not Stuff
Do Not Stuff
2nd = 075.08809.0073

ED6604
USB1_USB30_RX_P
USB1_USB30_RX_N
USB1_USB30_TX_N
USB1_USB30_TX_P
DY
Do Not Stuff
Do Not Stuff
2nd = 075.08809.0073

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Conn (USB/CARD)
Size: Custom
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
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RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sensor (Hall-Sensor)*

Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 67 of 106

Main Func = Debug

Vinafix.com

24 HOST_DEBUG_TX

20 UART_2_CTXD_DRXD

20 UART_2_CRXD_DTXD

18,24 ESPI_CLK

18,24 ESPI_RESET#

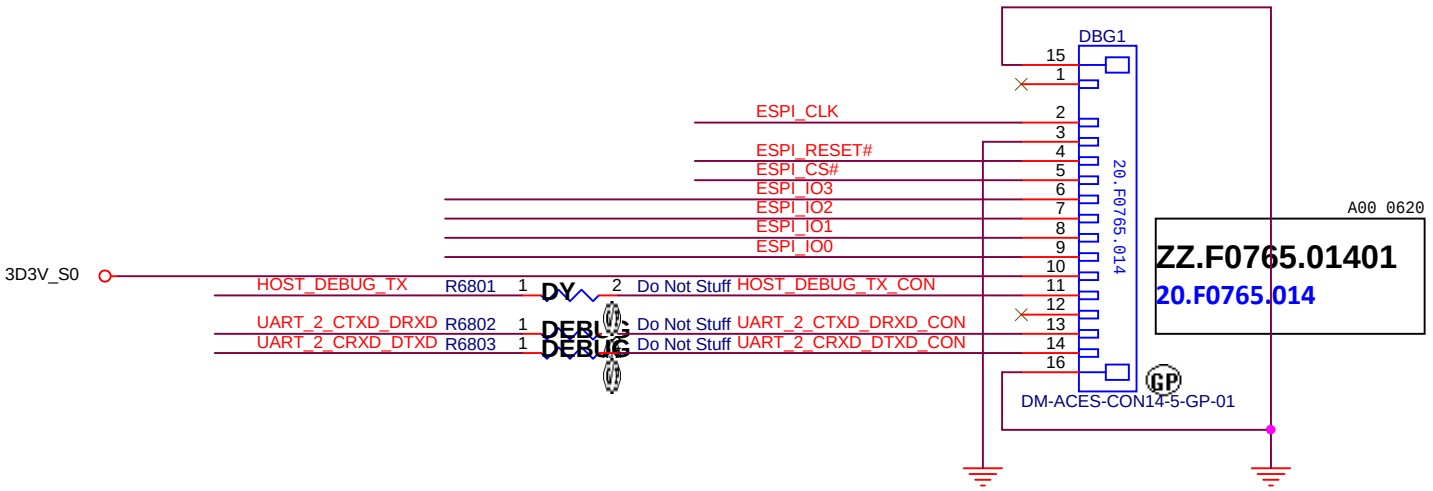
18,24 ESPI_CS#

18,24 ESPI_IO[3..0]

24 ME_FWP

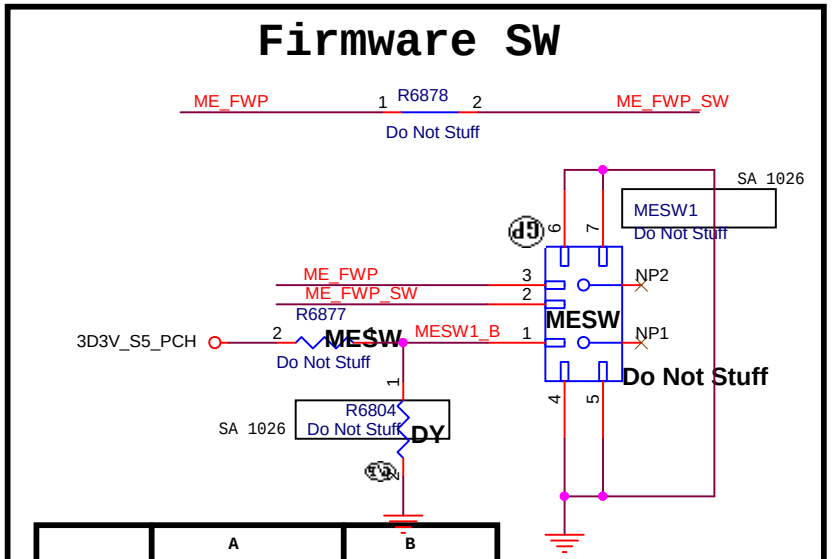
19 ME_FWP_SW

Debug Connector



Use ZZ.F0765.01401 DUMMY PAD for MP

Firmware SW



	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug (LPC debug)*

Size	Document Number	Rev
A4	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 68 of 106

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (RSVD)***

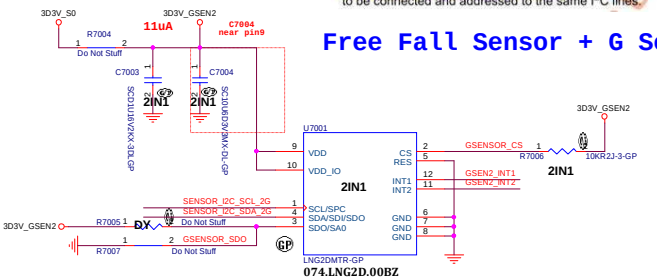
Size	Document Number	Rev
A3	***Rogue One 15"/17" WHL-U***	***A00***

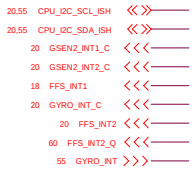
Date: Tuesday, July 24, 2018 Sheet 69 of 106

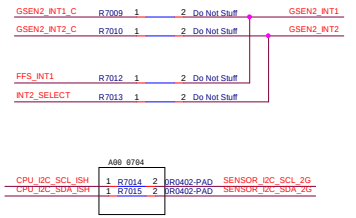
Main Func = Free Fall Sensor

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

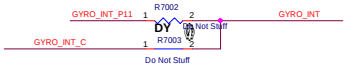
Free Fall Sensor + G Sensor

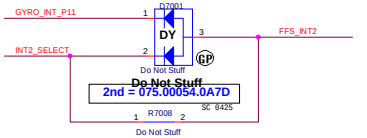






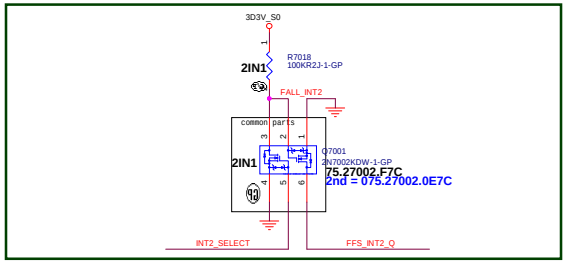
combine G





Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U7001



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

RO15/17 UMA/DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sensor (G-sensor)*

Size: A2 | Document Number: *Rogue One 15"/17" WHL-U* | Rev: *A00*

Date: Tuesday, July 24, 2018 | Sheet 70 of 106

Main Func = TYPEC MUX

DisplayPort Source

4 DP2_DDI_TX_P0
4 DP2_DDI_TX_N0
4 DP2_DDI_TX_P1
4 DP2_DDI_TX_N1
4 DP2_DDI_TX_P2
4 DP2_DDI_TX_N2
4 DP2_DDI_TX_P3
4 DP2_DDI_TX_N3

DisplayPort HPD

4,72 DP1_HPD_CPU

DisplayPort AUX

4 DP2_AUX_CPU_P
4 DP2_AUX_CPU_N
73 TYPEC_CON_SBU1
73 TYPEC_CON_SBU2

USB HOST

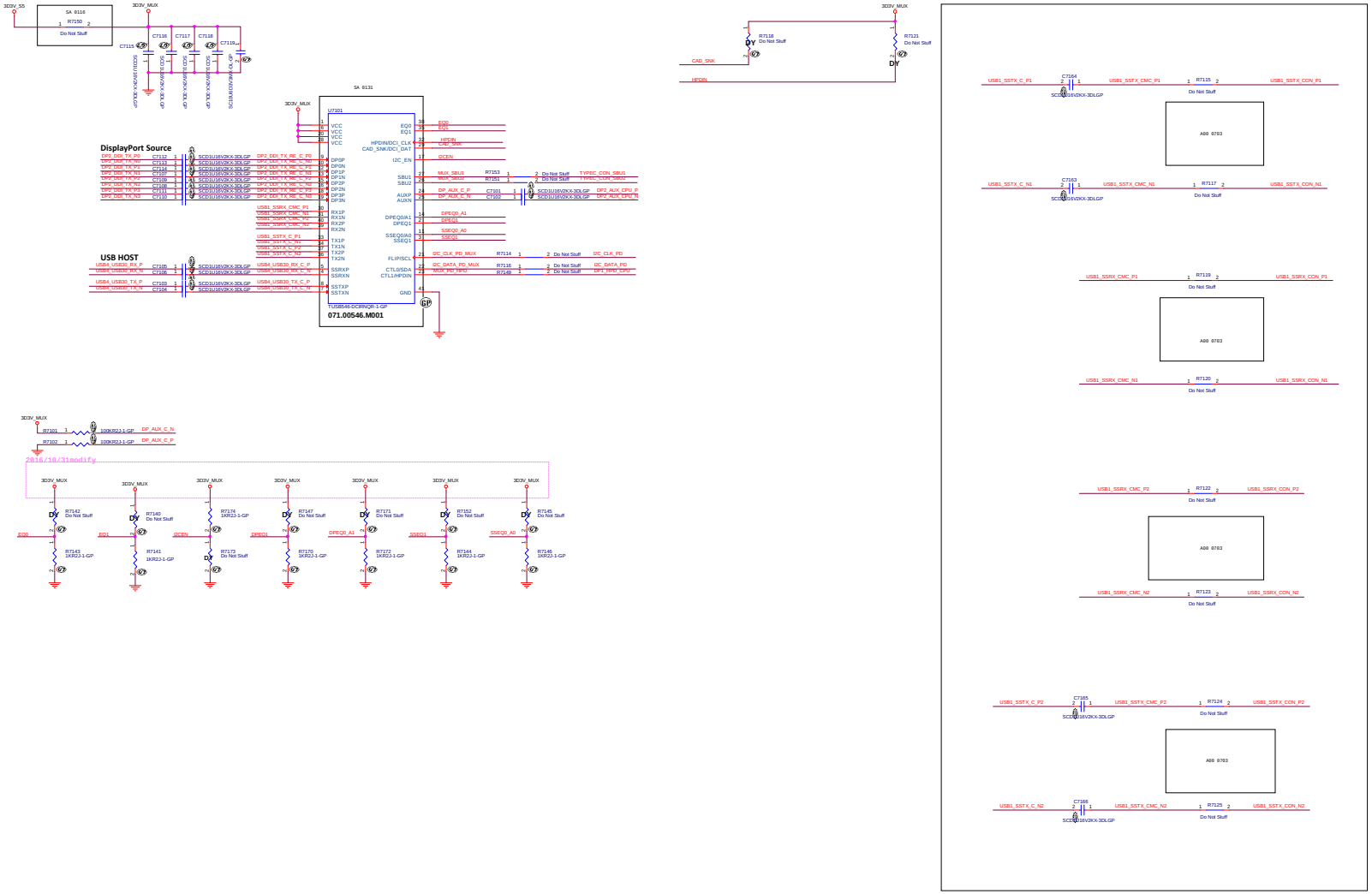
16 USB4_USB30_RX_P
16 USB4_USB30_RX_N
16 USB4_USB30_TX_P
16 USB4_USB30_TX_N

USB3.0 TYPEC CONNECTOR

73 USB1_SSTX_CON_N1
73 USB1_SSTX_CON_P1
73 USB1_SSTX_CON_N2
73 USB1_SSTX_CON_P2
73 USB1_SSRX_CON_N1
73 USB1_SSRX_CON_P1
73 USB1_SSRX_CON_N2
73 USB1_SSRX_CON_P2

I2C TO PD

72 I2C_CLK_PD
72 I2C_DATA_PD



RC15/17 UMA/DIS 2IN1

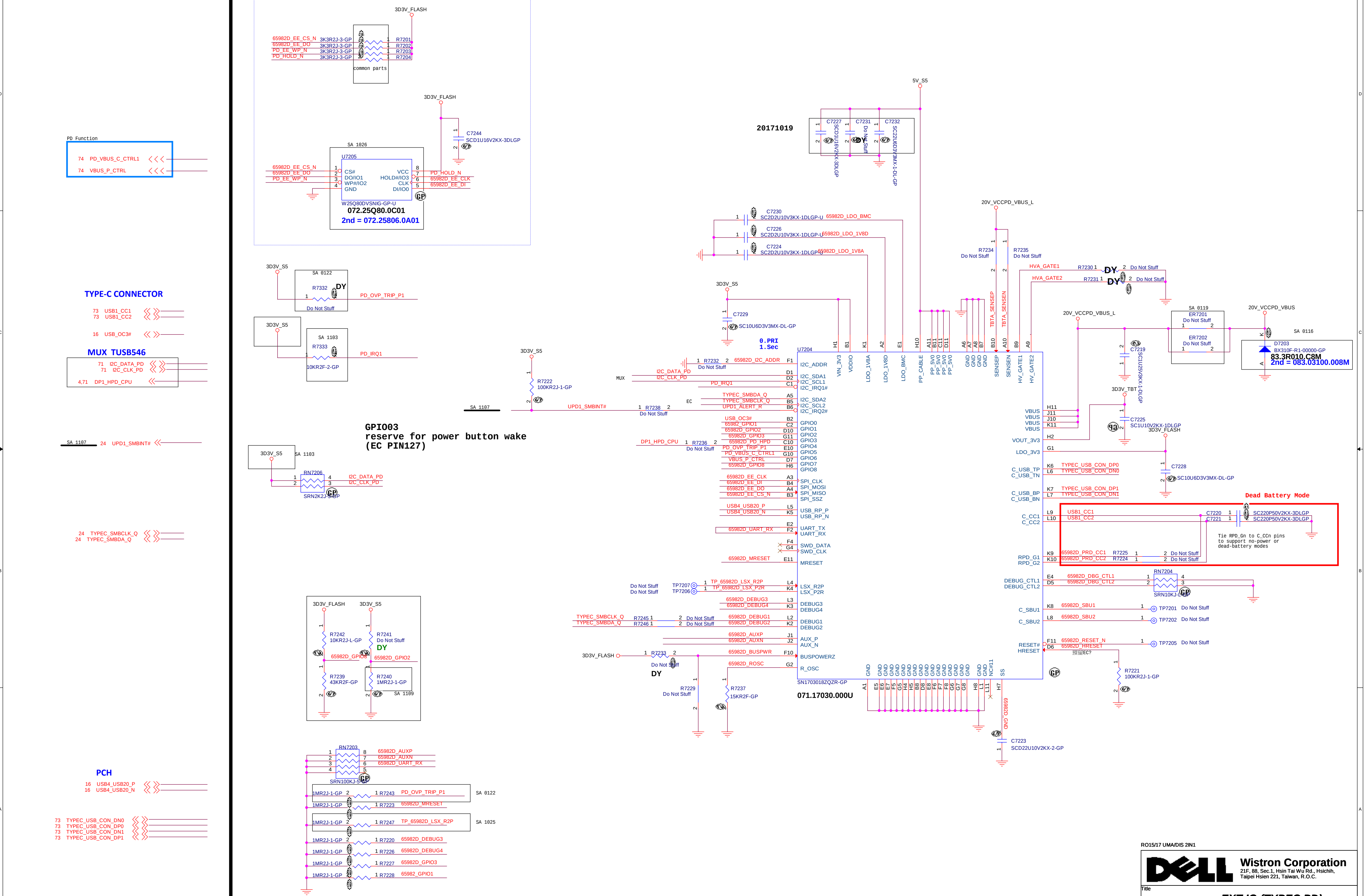
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File:

EXT IO(TBT(1/3)/Re-timer)

Size: A1	Document Number: Rogue One 15"/17" WHL-U	Rev: A00
Date: Tuesday, July 24, 2018	Sheet 71 of 106	

Main Func = TPS65982DC



RO15/17 UMA/DIS 2IN1

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Title	EXT IO (TYPEC PD)		
Size A2	Document Number: Rogue One 15"/17" WHL-U		Rev A00
Date: Tuesday, July 24, 2018	Sheet 72 of 106		

Main Func = TYPEC CONNECTOR

RO13_20170821 for EMI request

ED7303
TYPEC_USB_CON_DN0 — I/O1 — I/O4 — TYPEC_USB_CON_DP0
GND — VDD — SA 1110
TYPEC_USB_CON_DN1 — I/O2 — I/O3 — TYPEC_USB_CON_DP1
AZC099-04S-2-GP
075.09904.0A7C
2nd = 75.08902.07C

ED7304
USB1_CC2 — I/O1 — I/O4 — USB1_CC1
GND — VDD — SA 1110
TYPEC_CON_SBU2 — I/O2 — I/O3 — TYPEC_CON_SBU1
AZC099-04S-2-GP
075.09904.0A7C
2nd = 75.08902.07C

71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2
72 TYPEC_USB_CON_DN0
72 TYPEC_USB_CON_DP0
72 TYPEC_USB_CON_DN1
72 TYPEC_USB_CON_DP1
71 TYPEC_CON_SBU1
71 TYPEC_CON_SBU2

check
72 USB1_CC1
72 USB1_CC2

USB1_SSRX_CON_P1 C7308 1 — SCD33U6D3V2KX-1-GP — USB1_SSRX_CON_R_P1
USB1_SSRX_CON_N1 C7309 1 — SCD33U6D3V2KX-1-GP — USB1_SSRX_CON_R_N1
USB1_SSRX_CON_P2 C7310 1 — SCD33U6D3V2KX-1-GP — USB1_SSRX_CON_R_P2
USB1_SSRX_CON_N2 C7311 1 — SCD33U6D3V2KX-1-GP — USB1_SSRX_CON_R_N2
SA 1226
220KR2F-L-GP R7334
220KR2F-L-GP R7335
220KR2F-L-GP R7336
220KR2F-L-GP R7337

ED7301
USB1_SSTX_CON_N1 — USB1_SSTX_CON_N1
USB1_SSTX_CON_P1 — USB1_SSTX_CON_P1
USB1_SSRX_CON_N1 — USB1_SSRX_CON_N1
USB1_SSRX_CON_P1 — USB1_SSRX_CON_P1
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
SA 1227

ED7302
USB1_SSRX_CON_P2 — USB1_SSRX_CON_P2
USB1_SSRX_CON_N2 — USB1_SSRX_CON_N2
USB1_SSTX_CON_P2 — USB1_SSTX_CON_P2
USB1_SSTX_CON_N2 — USB1_SSTX_CON_N2
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073

AFTP TESTPOINT

20V_VCCPD_VBUS 1 — 20V_VCCPD_VBUS 1 — AFTP7317 AFTP7318

20V_VCCPD_VBUS
C7307 SCD1U25V2KX-1-DLGP
C7306 SC1U25V3KX-1-DLGP
C7302 SCD1U25V2KX-1-DLGP
C7303 SCD1U25V2KX-1-DLGP
C7304 SCD1U25V2KX-1-DLGP
C7305 DY Do Not Stuff

USB1
A4 VBUS#A4
A9 VBUS#A9
B4 VBUS#B4
B9 VBUS#B9
SSTXP1 A2 — USB1_SSTX_CON_P1
SSTXN1 A3 — USB1_SSTX_CON_N1
SSTXP2 B2 — USB1_SSTX_CON_P2
SSTXN2 B3 — USB1_SSTX_CON_N2
GND G1
GND G2
GND A1
GND A12
GND B1
GND B12
USB1_SSRX_CON_R_P1 B11 — SSRXP1
USB1_SSRX_CON_R_N1 B10 — SSRXN1
USB1_SSRX_CON_R_P2 A11 — SSRXP2
USB1_SSRX_CON_R_N2 A10 — SSRXN2
USB1_CC1 A5 — CC1
USB1_CC2 B5 — CC2
TYPEC_CON_SBU1 A8 — RFU1
TYPEC_CON_SBU2 B8 — RFU2
TYPEC_USB_CON_C_DP0 A6 — DP1
TYPEC_USB_CON_C_DN0 A7 — DN1
TYPEC_USB_CON_C_DP1 B6 — DP2
TYPEC_USB_CON_C_DN1 B7 — DN2
CHASSIS#13 13
CHASSIS#14 14
CHASSIS#15 15
CHASSIS#16 16
CHASSIS#17 17
CHASSIS#18 18
CHASSIS#19 19
CHASSIS#20 20
NP1 — NP1
NP2 — NP2
SKT-USB36-27-GP
022.10005.M035
2nd = 022.10005.M036
SC 0425

R7330 2MR2F-GP
R7331 2MR2F-GP

SC 0425
EL7301
TYPEC_USB_CON_DP0 — TYPEC_USB_CON_C_DP0
TYPEC_USB_CON_DN0 — TYPEC_USB_CON_C_DN0
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001
SC 0608

EL7302
TYPEC_USB_CON_DP1 — TYPEC_USB_CON_C_DP1
TYPEC_USB_CON_DN1 — TYPEC_USB_CON_C_DN1
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001
SC 0608

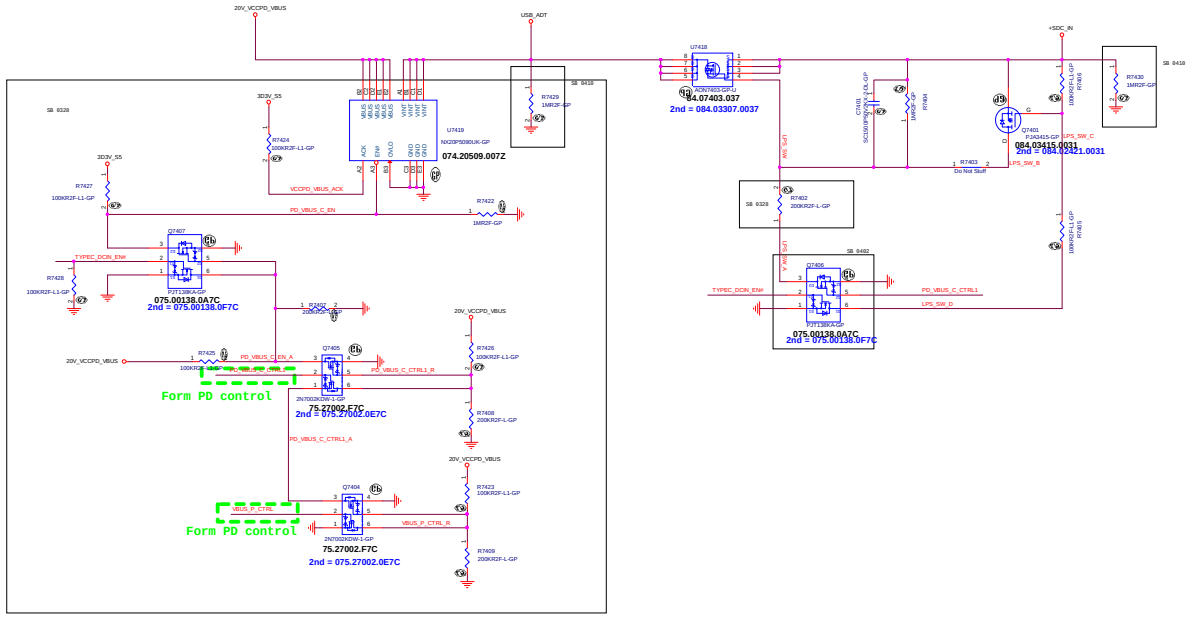
RO15/17 UMA/DIS 2IN1

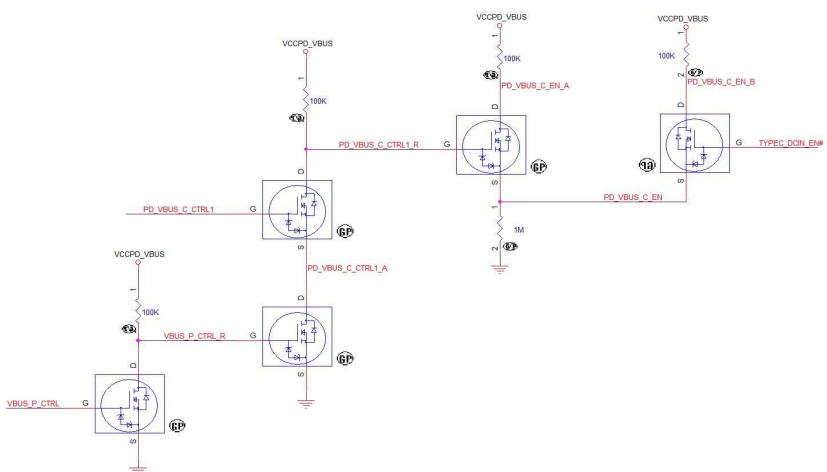
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO_(TBT(3/3)/TypeC CON)
Size: A3
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
Sheet 73 of 106

Main Func = TYPEC protect

72 PD_VBUS_C_CTRL1
72 VBUS_P_CTRL
24 TYPEC_DCIN_EN#
44 VCCPD_VBUS_ACK





RO15/17 UMA/DIS 28N1

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (LPS)

Size	Document Number	Rev
A1	Rogue One 15"/17" WHL-U	A00
Date: Tuesday, July 24, 2018	Sheet 74 of 105	

RO15/17 UMA/DIS 2IN1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (TYPEC Redriver/MUX)

Size	Document Number	Rev
A	**Rogue One 15"/17" WHL-U**	**A00**

Date: Tuesday, July 24, 2018 Sheet 75 of 106

Main Func = dGPU

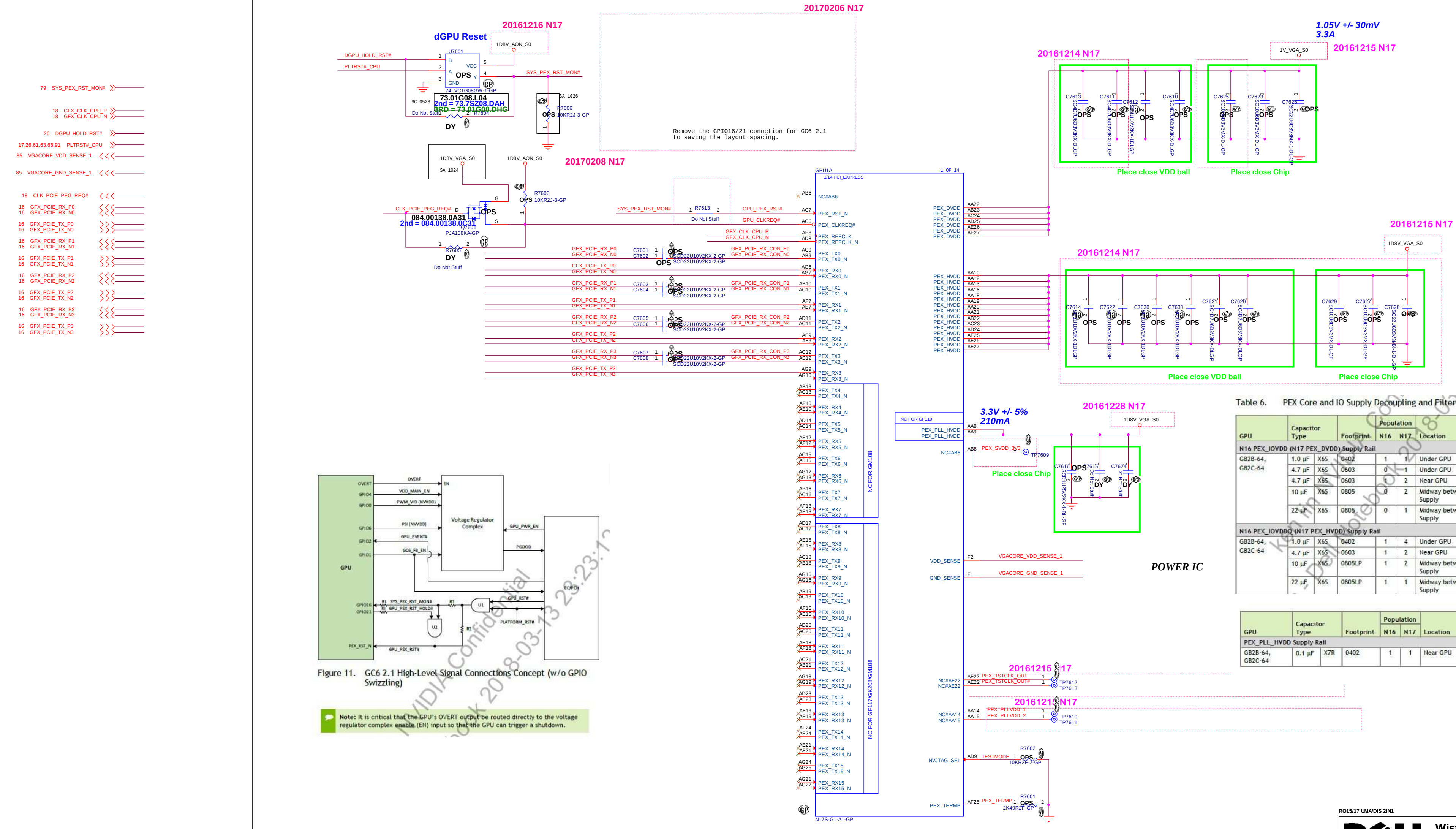

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

RO15/17 UMA/DIS 2IN1

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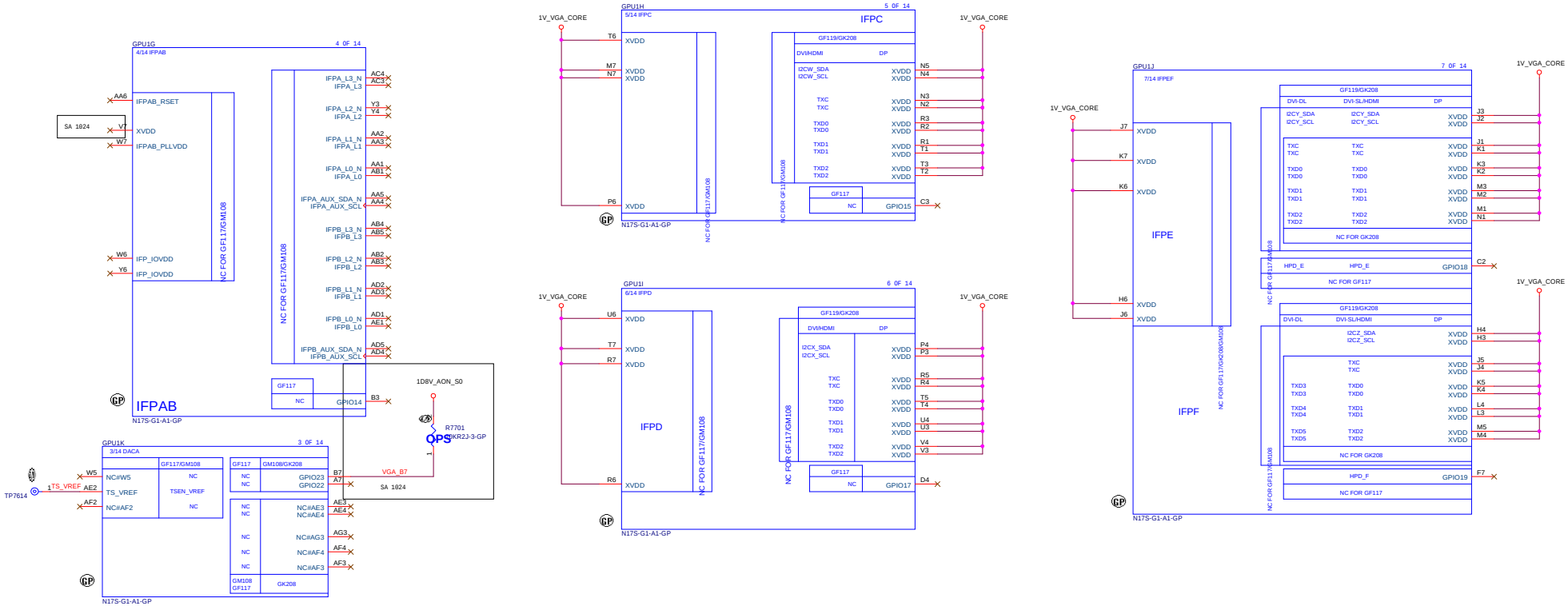
Title: GPU (PEG 1/5)

Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 76 of 106

Main Func = dGPU



RO15/17 UMA/DIS 2IN1

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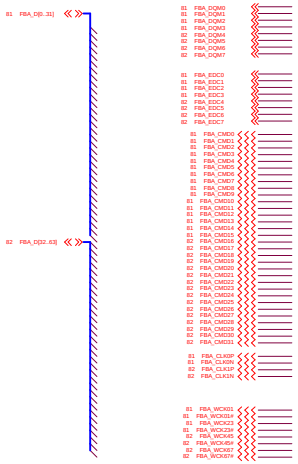
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (DIGITAL 2/5)

Size: A2 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 77 of 106

Main Func = dGPU



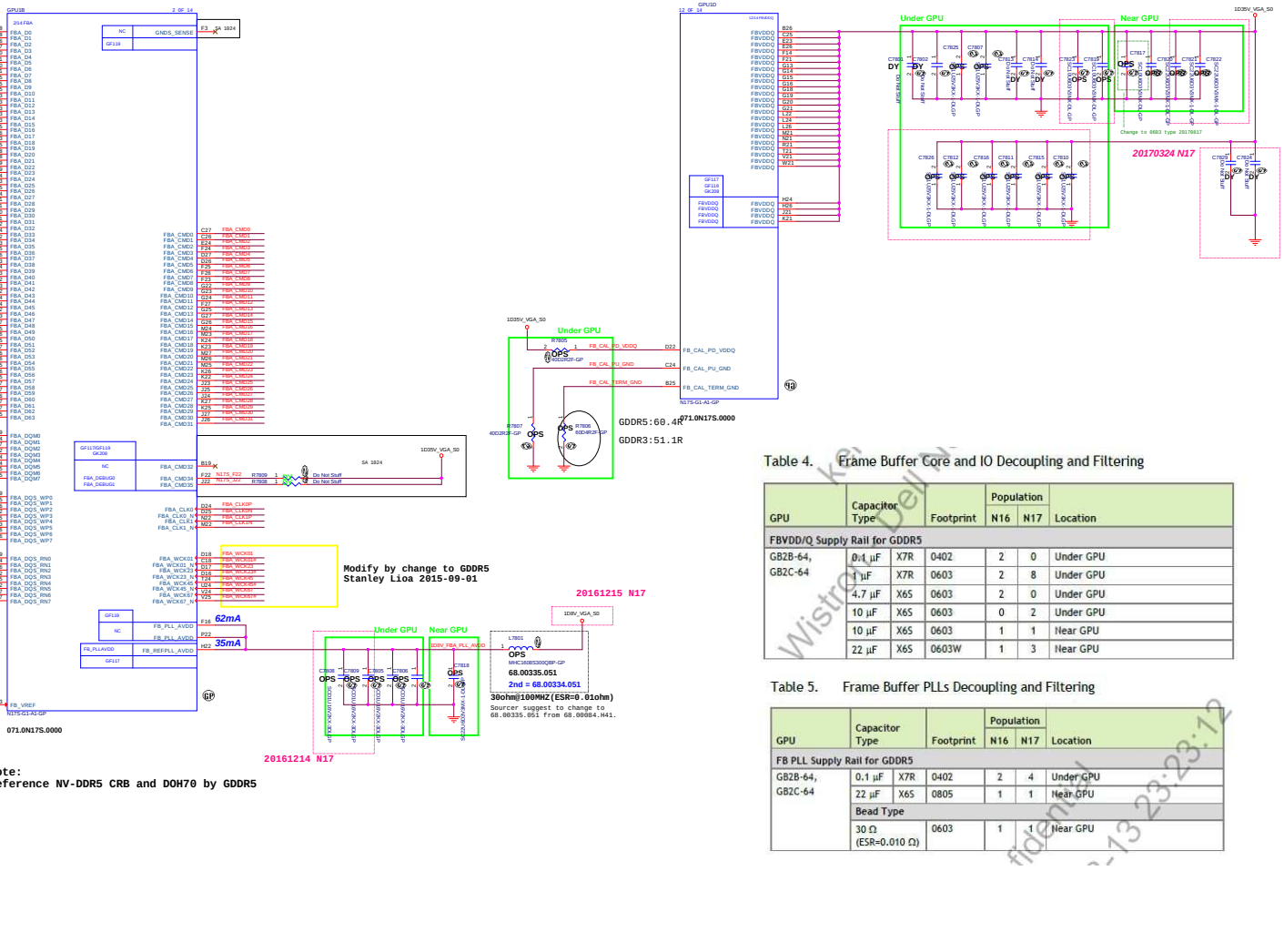


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type				
	30 Ω (ESR=0.010 Ω)	0603	1	1	Near GPU

RC15/17 UMA/DIS 2IN1

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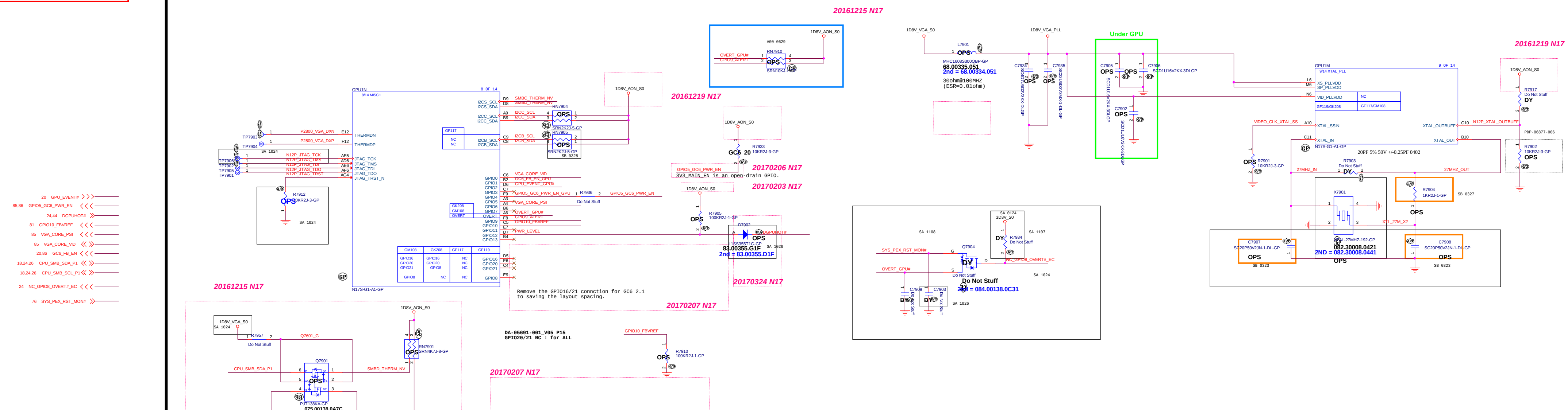
GPU (VRAM 3/5)

Size: B1 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Thursday, July 09, 2015 | Sheet 19 of 105

Main Func = dGPU



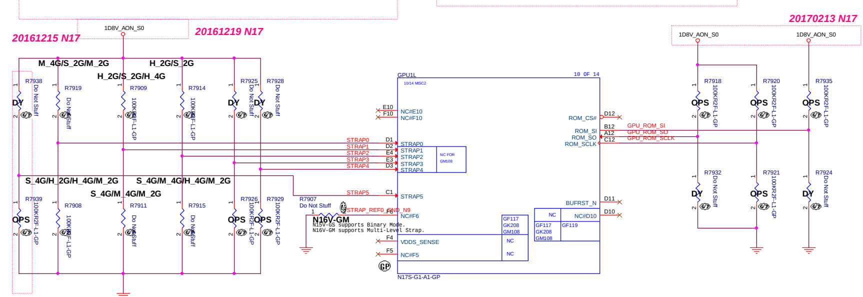


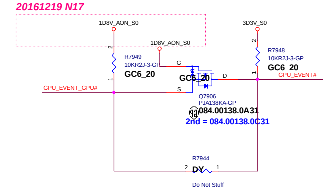
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

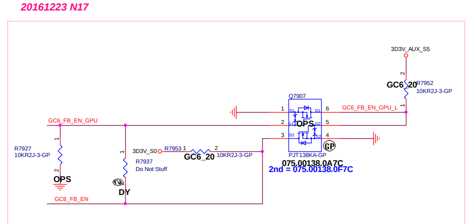
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

20161215 N17

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0





64 bits	
GDDR5 @ 1.35V	
2GB	4GB
2pcs x 8Gb(256M x 32)	4pcs x 8Gb(512Mx 16)
Hynix - H5GC8H24MJR-R0C (029XX)	Hynix - H5GC8H24MJR-R0C (029XX)
Micron - MT51J256M32HF-70:A (V15MH)	Micron - MT51J256M32HF-70:A (V15MH)
Samsung - K4G80325FB-HC28 (N1MMH)	Samsung - K4G80325FB-HC28 (N1MMH)

Table 4. N17S-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
4 Gb	128Mx32 256Mx16	1.35V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready

Notes:

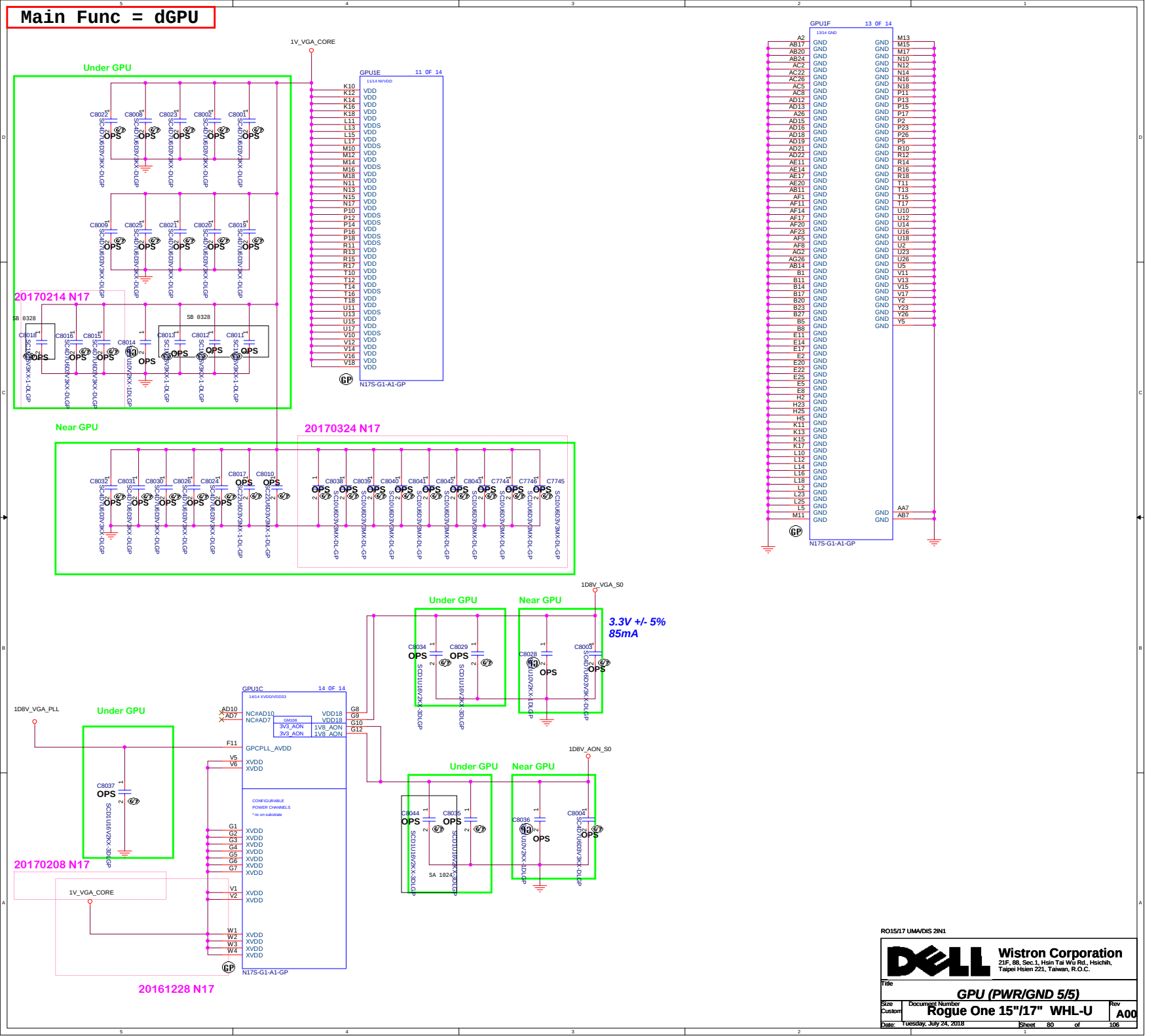
1. For N17S-G1, the maximum allowable memory case temperature is 85 °C.
2. Higher-speed grade memory devices can be used on N17x GPU designs in accordance with written waivers from the memory vendors. An acceptable waiver should indicate that the higher speed grade memory can be used as a substitute for lower-speed grade memory without any changes to spec parameters, including but not limited to timing, BIOS, and voltage.

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)	
STRAP2	STRAP1	STRAP0		
L	L	L	0 (0x0000)	Samsung 4G 2G
L	L	H	1 (0x0001)	Micron 4G 2G
L	H	L	2 (0x0002)	Hynix 4G 2G
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	

RO15/17 UMA/DIS 2IN1

Main Func = dGPU



RO15/17 UMA/DIS 2IN1

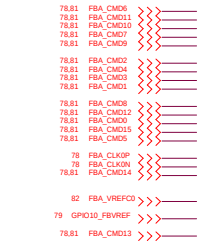
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

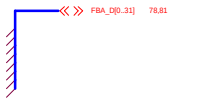
Title: GPU (PWR/GND 5/5)

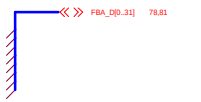
Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

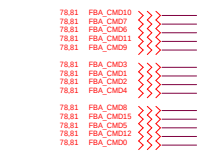
Date: Tuesday, July 24, 2018 | Sheet 80 of 106

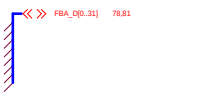
SSID = VRAM

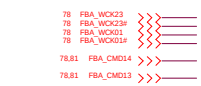


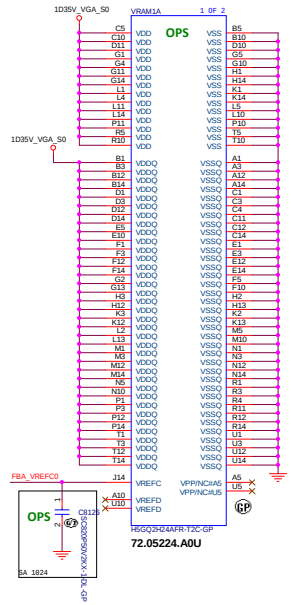


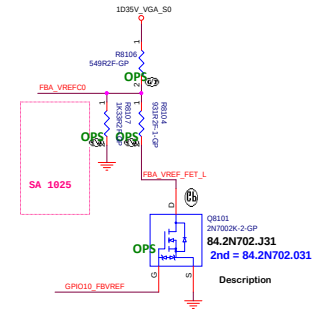






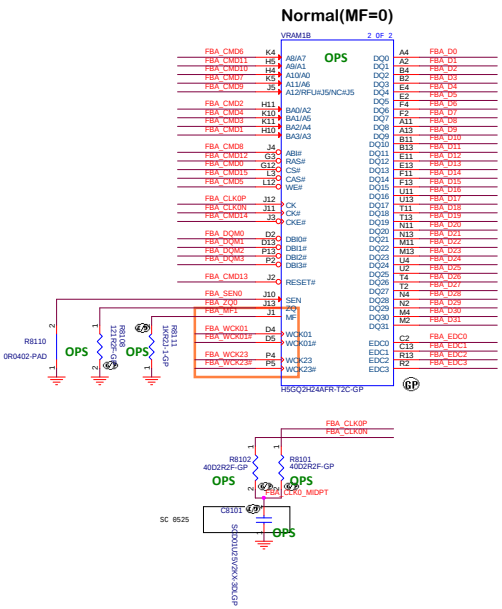


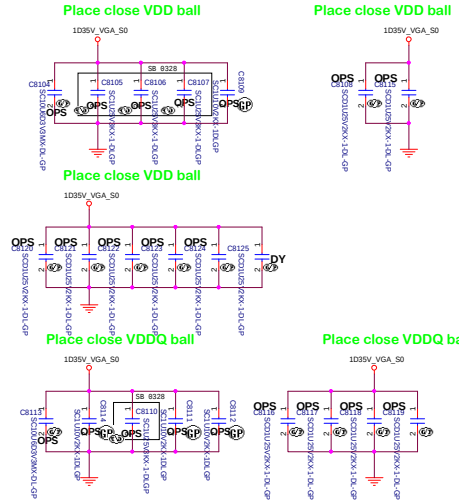




FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





KR DIS 2IN1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: Custom | Document Number: Starload-KBL-R GPU | Rev: X02

Date: Tuesday, July 24, 2018 | Sheet 81 of 13

SSID = VRAM

FBA_D[32..63] 78,82

FBA_D[32..63] 78,82

78,82 FBA_CMD22
78,82 FBA_CMD27
78,82 FBA_CMD26
78,82 FBA_CMD23
78,82 FBA_CMD25

78,82 FBA_CMD19
78,82 FBA_CMD20
78,82 FBA_CMD18
78,82 FBA_CMD17

78,82 FBA_CMD24
78,82 FBA_CMD28
78,82 FBA_CMD21
78,82 FBA_CMD31
78,82 FBA_CMD16

78 FBA_CLK1P
78 FBA_CLK1N
78,82 FBA_CMD30

81 FBA_VREFC0
79,81 GPIO10_FBVREF
78,82 FBA_CMD29

FBA_D[32..63] 78,82

FBA_D[32..63] 78,82

78,82 FBA_CMD26
78,82 FBA_CMD23
78,82 FBA_CMD22
78,82 FBA_CMD27
78,82 FBA_CMD25

78,82 FBA_CMD19
78,82 FBA_CMD17
78,82 FBA_CMD18
78,82 FBA_CMD20

78,82 FBA_CMD24
78,82 FBA_CMD31
78,82 FBA_CMD21
78,82 FBA_CMD28
78,82 FBA_CMD16

78,82 FBA_CMD30

78,82 FBA_CMD29

78 FBA_WCK67
78 FBA_WCK67#
78 FBA_WCK45
78 FBA_WCK45#

78 FBA_DQM4
78 FBA_DQM5
78 FBA_DQM6
78 FBA_DQM7

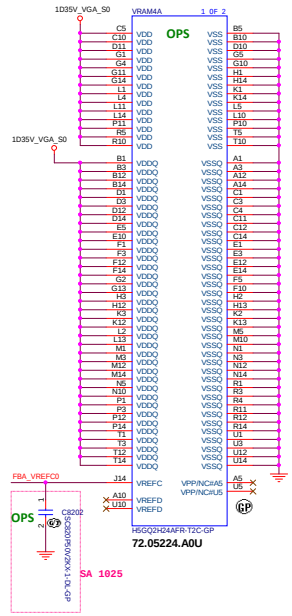
78 FBA_EDC4
78 FBA_EDC5
78 FBA_EDC6
78 FBA_EDC7

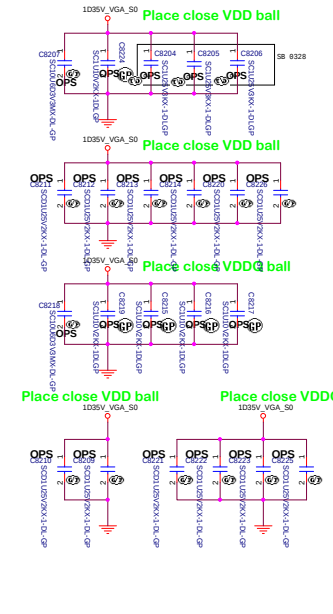
Frame Buffer Patition A-Upper Half

SA 1025

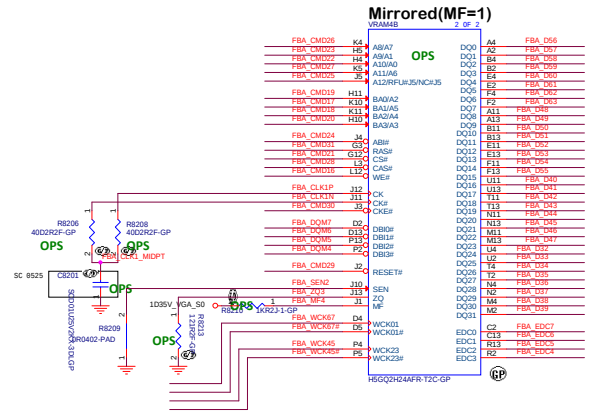
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





Mirrored(MF=1)



KR DIS 2IN1

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Title: **GPU-VRAM3.4 (2/4)**

Size	Document Number	Rev
Custom	Starload-KBL-R GPU	X02

Date: Tuesday, July 24, 2018 Sheet 82 of 13

RO15/17 UMA/DIS 2IN1

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Title

GPU (VRAM5,6 3/4)

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 83 of 106

RO15/17 UMA/DIS 2IN1

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Title

GPU (VRAM7,8 4/4)

Size	Document Number	Rev
A3	**Rogue One 15"/17" WHL-U**	**A00**

Date: Tuesday, July 24, 2018 Sheet 84 of 106

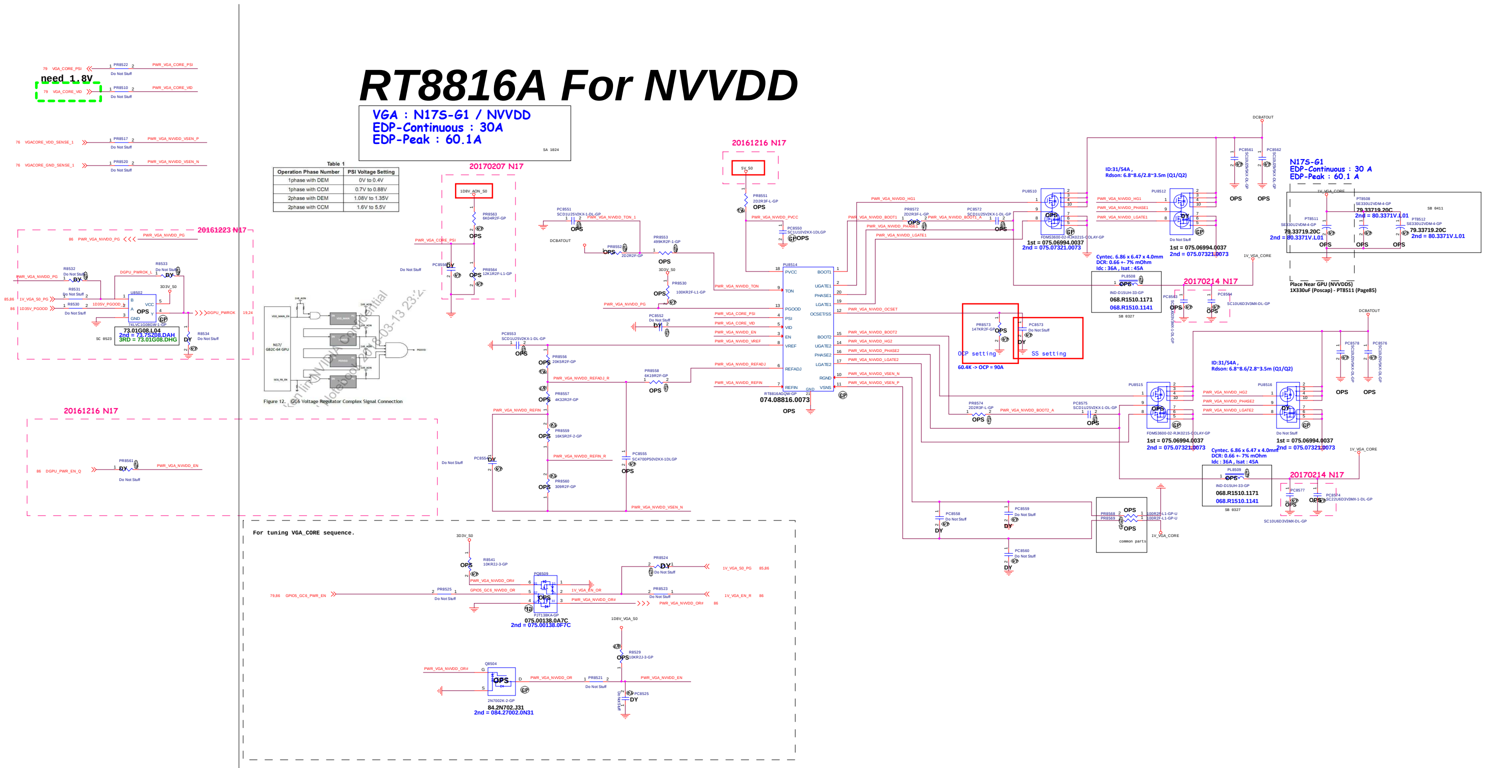
Main Func = dGPU

RT8816A For NVVDD

VGA : N17S-G1 / NVVDD
EDP-Continuous : 30A
EDP-Peak : 60.1A

Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V



RO15/17 UMA/DIS 2IN1

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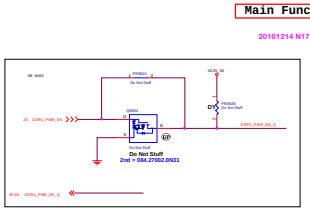
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU (VGA_CORE)	
Size A0	Document Number: Rogue One 15"/17" WHL-U	Rev A00
Date: Tuesday, July 24, 2018	Sheet 85 of 106	

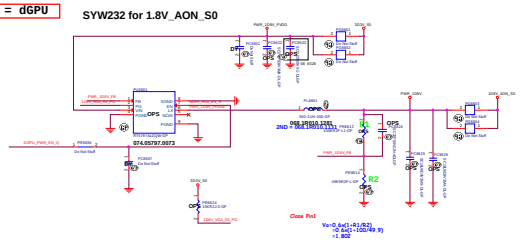
Main Func = dGPU



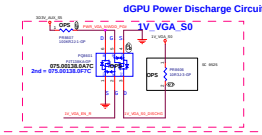
Main Func = dGPU

20161214 N17

SYW232 for 1.8V_AON_S0



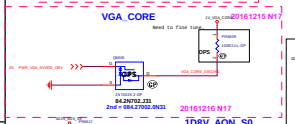
dGPU Power Discharge Circuit



1V_VGA_S0

VGA_CORE

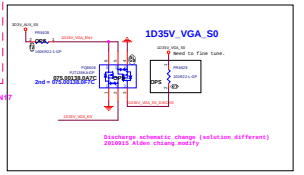
20161215 N17



20161216 N17

1D8V_AON_S0

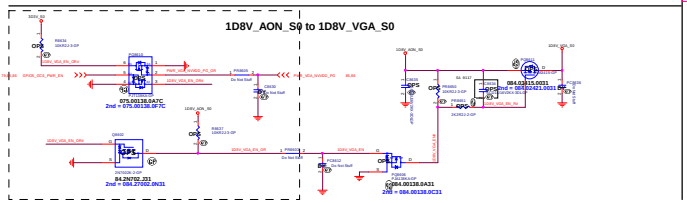
20161219 N17



1D35V_VGA_S0

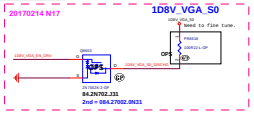
Discharge schematic change (solution different)
20180815 Aiden chiang modify

1D8V_AON_S0 to 1D8V_VGA_S0



20170214 N17

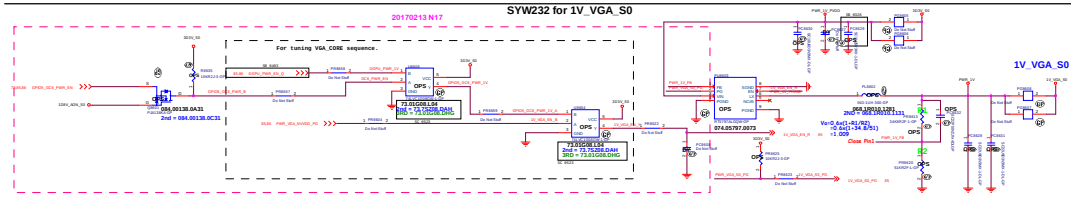
1D8V_VGA_S0



SYW232 for 1V_VGA_S0

20170213 N17

For tuning VGA_CORE sequence.

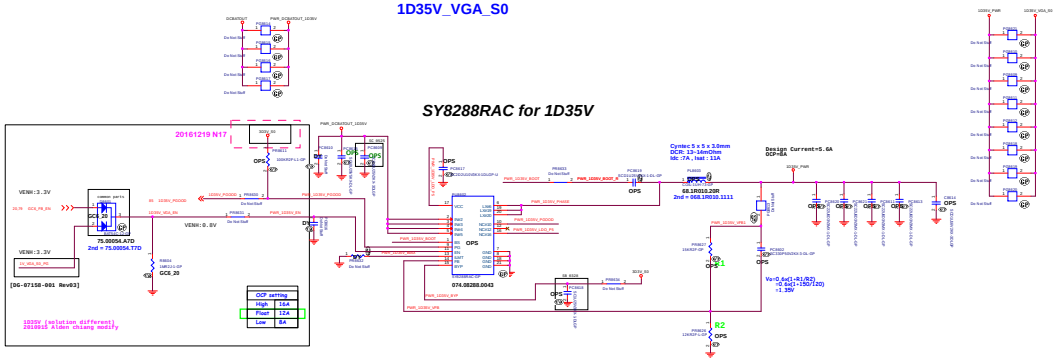


1V_VGA_S0

1D35V_VGA_S0

SY8288RAC for 1D35V

20161219 N17



OCP setting

High	16A
Flow	12A
Low	8A

1D35V (solution different)
20180815 Aiden chiang modify

RO15/17 UMA/DIS 2IN1

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A3	**Rogue One 15"/17" WHL-U**	**A00**

Date: Tuesday, July 24, 2018 Sheet 87 of 106

RO15/17 UMA/DIS 2IN1

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Title

UNUSED PARTS_(RSVD)

Size	Document Number	Rev
A	**Rogue One 15"/17" WHL-U**	**A00**

Date: Tuesday, July 24, 2018 Sheet 88 of 106

Main Func = UnusedParts

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H4 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H7 Do Not Stuff
H10 Do Not Stuff
H11 Do Not Stuff
H12 Do Not Stuff

WLAN

HS1 STF237R113H86-GP
434.07K0E.0001

EMI STOP

SPR1 SPRING-U4-GP
SPR2 SPRING-U4-GP
SPR3 Do Not Stuff
34.40U07.001
34.40U07.001
Do Not Stuff
SC 0524 RF

3D3V_S0
5V_S0
3D3V_S5
5V_S5

SSID = EMI

Mind the voltage rating of the caps.

DCBATOUT
3D3V_S0
1D2V_S3

SSID = RF

1D2V_S3
DCBATOUT
+SDC_IN
1V_VGA_CORE
1V_CPU_CORE
1V_VCCSA
1V_VCCIO
1D35V_VGA_S0
3D3V_SSD

For GPU

Mind the voltage rating of the caps.

DCBATOUT

EMI reserve , 20141118

1V_CPU_CORE
1V_VCCGT
1V_VCCSA

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Title: UNUSED PARTS (RF/EMI Caps)
Size: A2
Document Number: Rogue One 15"/17" WHL-U
Rev: A00
Date: Tuesday, July 24, 2018
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RO15/17 UMA/DIS 2IN1

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Title: INT IO (RSVD)(NFC)

Size: A3 | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

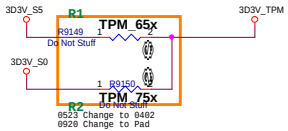
Date: Tuesday, July 24, 2018 | Sheet 90 of 106

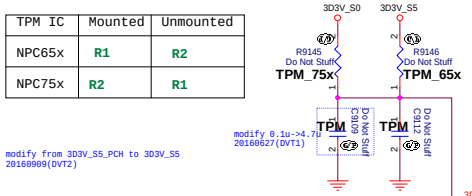
Main Func = TPM

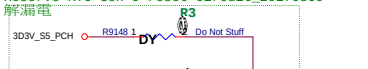
17,24,40,91	PM_SLP_S0#	>>>
18,91	SPI_CS_ROM_N2	>>>
18,25,91	SPI_SO_ROM	<<<
15,18,25,91	SPI_SI_ROM	>>>
18,25,91	SPI_CLK_ROM	>>>
20	PIRQA#	>>>
17,26,61,63,66,76	PLTRST#_CPU	>>>
17,24,40,91	PM_SLP_S0#	>>>
18	TPM_SPI_IRQ#	<<<

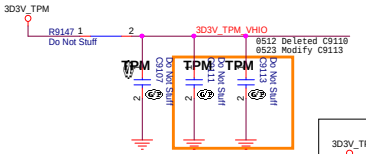
	NPCT650		NPCT750	
Pin define	Power Name	Power status	Power Name	Power status
Pin1	VSB	VALW	VSB	VALW
Pin8	VDD	VRUN	VHIO	VRUN (S0)
Pin14	VHIO	VSPI	NC	nc
Pin22	VHIO	VSPI	VHIO	VRUN (S0)

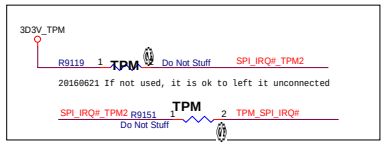
TPM IC	Mounted	Unmounted
NPC65x	R1	R2
NPC75x	R2	R1

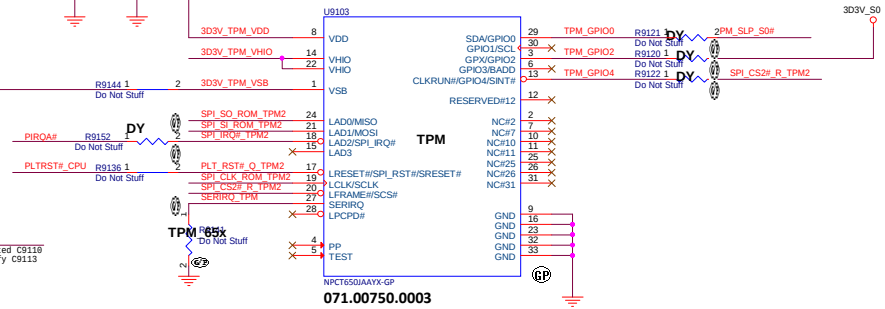


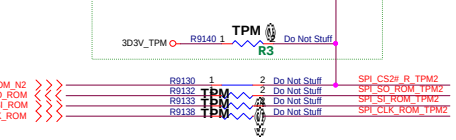












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Title: INT IO_(TPM)

Size: Custom | Document Number: Rogue One 15"/17" WHL-U | Rev: A00

Date: Tuesday, July 24, 2018 | Sheet 91 of 106

RO15/17 UMA/DIS 2IN1

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Title: ***Finger Print***

Size	Document Number	Rev
A3	***Rogue One 15"/17" WHL-U***	***A00***

Date: Tuesday, July 24, 2018 Sheet 92 of 106

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Title

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Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 93 of 106

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Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 94 of 106

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Title

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Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 95 of 106

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Title

(Reserved)

Size	Document Number	Rev
A3	*Rogue One 15"/17" WHL-U*	*A00*

Date: Tuesday, July 24, 2018 Sheet 96 of 106

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Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 97 of 106

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Title: *CRT_Switch*

Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

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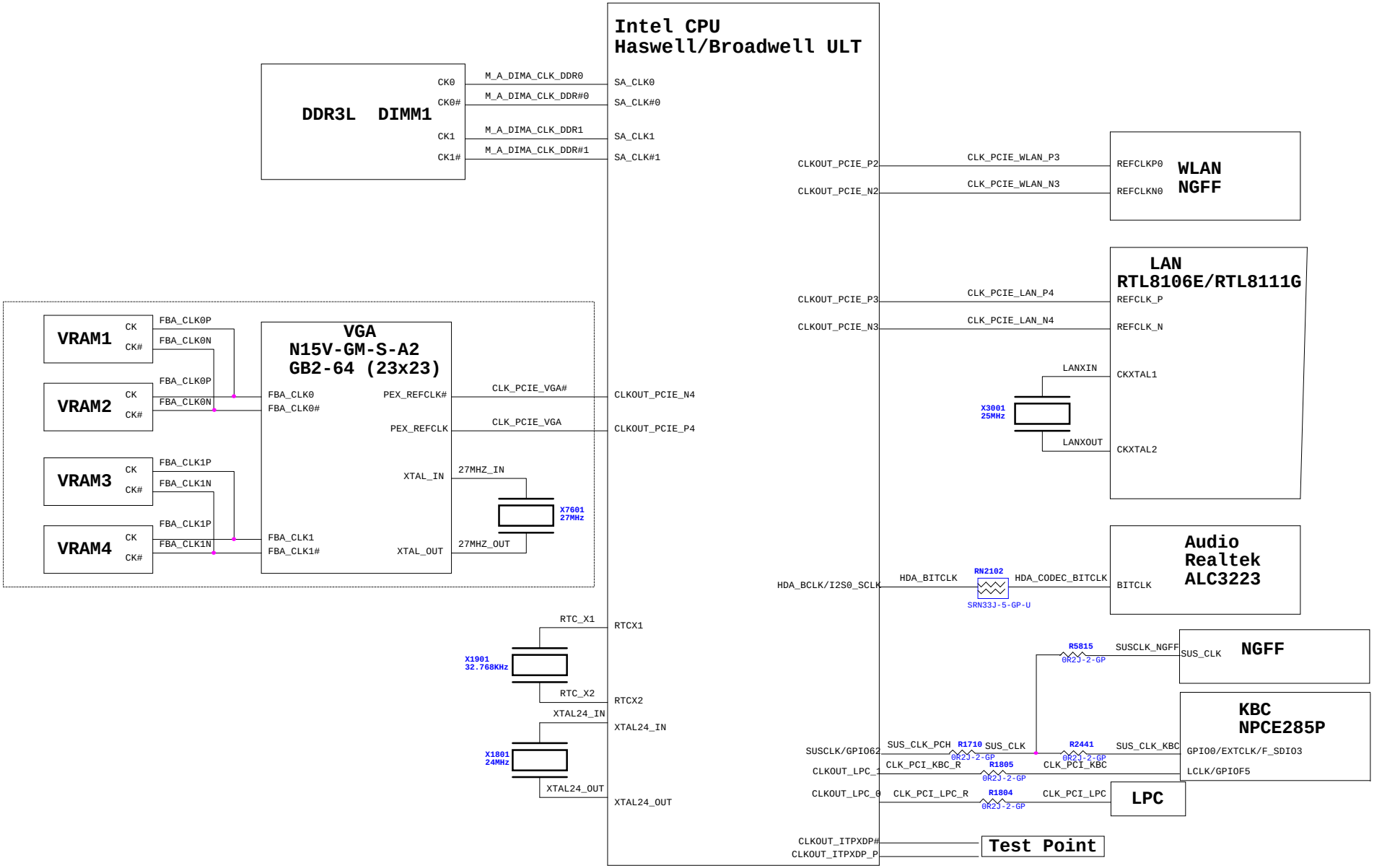
Title

Debug (XDP debug)

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 99 of 106

CLK Block Diagram



RO15/17 UMA/DIS 2IN1

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Title: CLK Block Diagram		
Size: A2	Document Number: Rogue One 15"/17" WHL-U	Rev: A00
Date: Tuesday, July 24, 2018	Sheet 100 of 106	

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

RO15/17 UMA/DIS 2IN1

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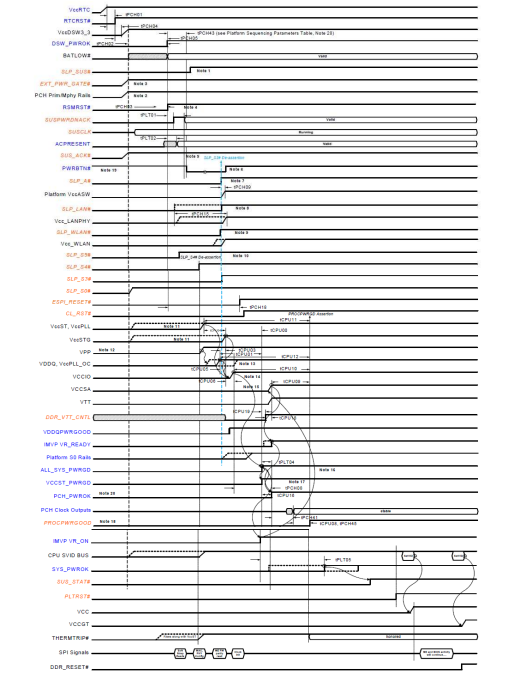
Title: Change History

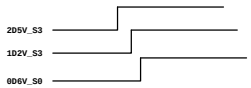
Size	Document Number	Rev
A3	Rogue One 15"/17" WHL-U	A00

Date: Tuesday, July 24, 2018 Sheet 101 of 106

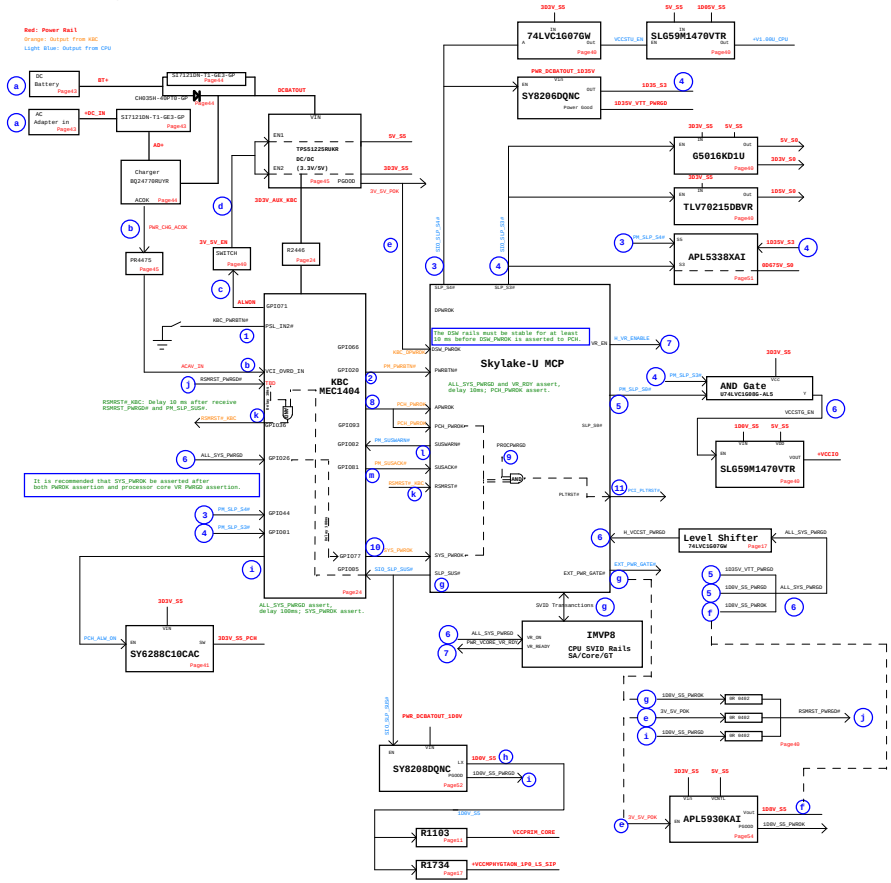
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



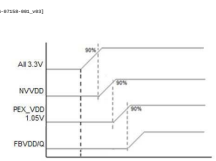
For DDR4 power sequence



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

> **Note:**
> - The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
> - The ramp up overshoot should not exceed the silicon reliability limit voltage.
> - The previous power rail must ramp up to 90% before the next power rail can start ramping up.
> - No signal should be applied to the GPU before the power rails are fully ramped
> - Refer to the JEDEC Memory Specification for memory related power sequencing.
> - The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

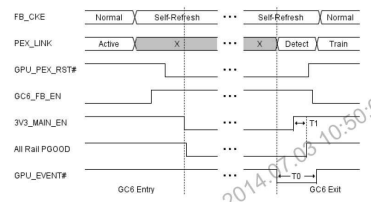
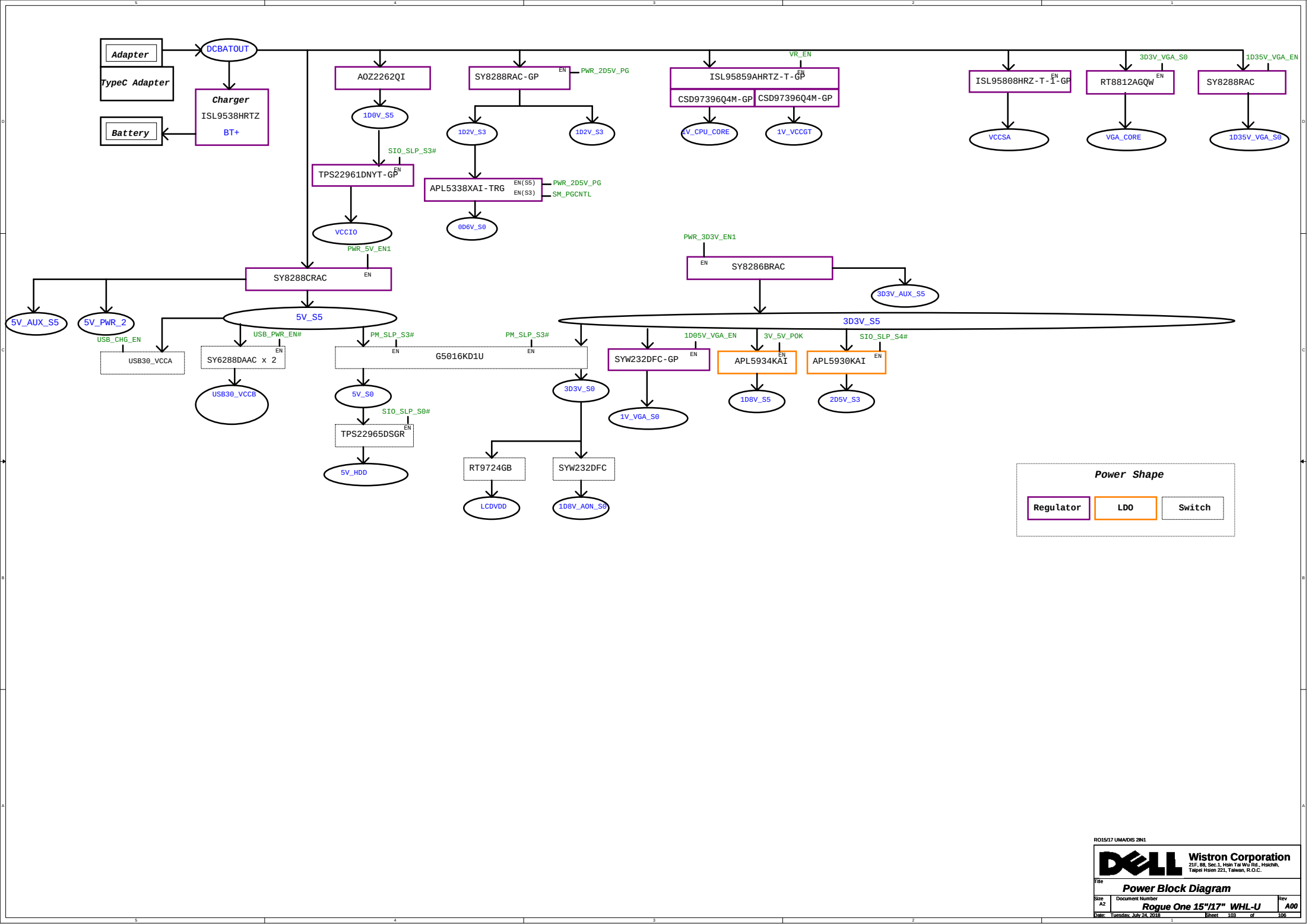


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

> **Note:**
> - ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
> - During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
> - All delays should be minimized to increase time spent in GC6 for maximum power saving.
> - The entire entry/exit sequence must complete within 200 ms.



RO15/17 UMA/DIS 2IN1

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Title: Power Block Diagram

Size	Document Number	Rev
A2	Rogue One 15"/17" WHL-U	A00

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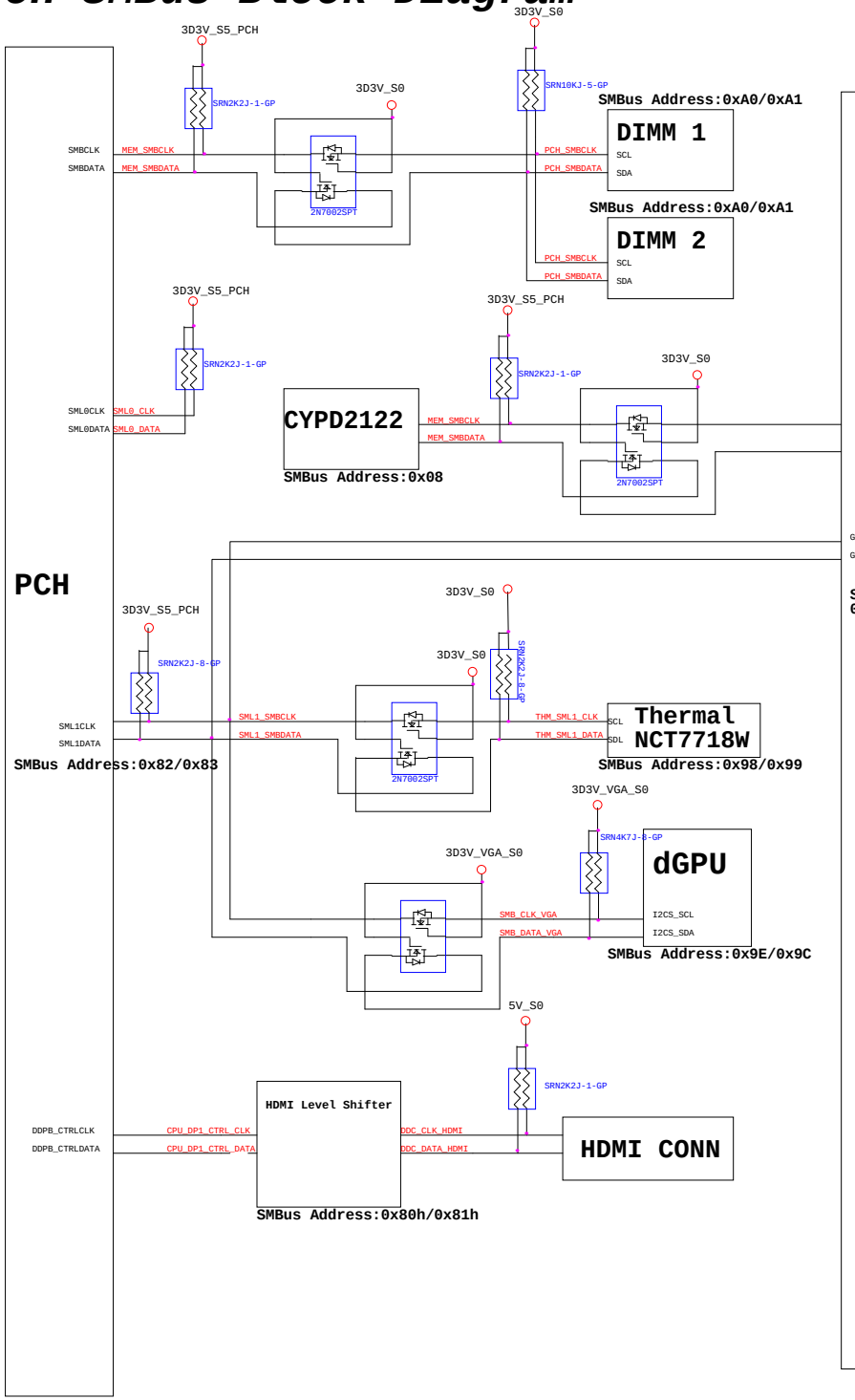
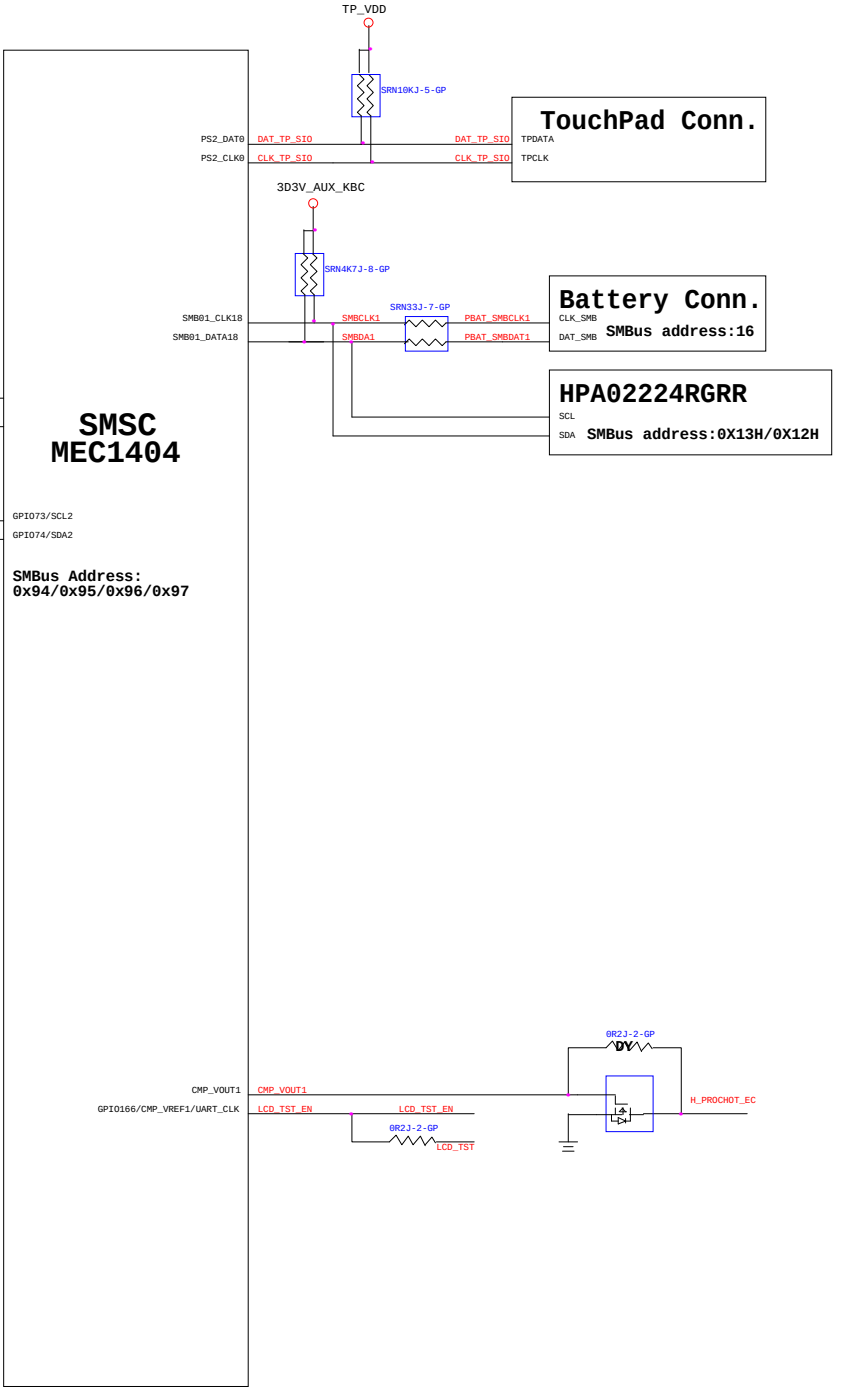
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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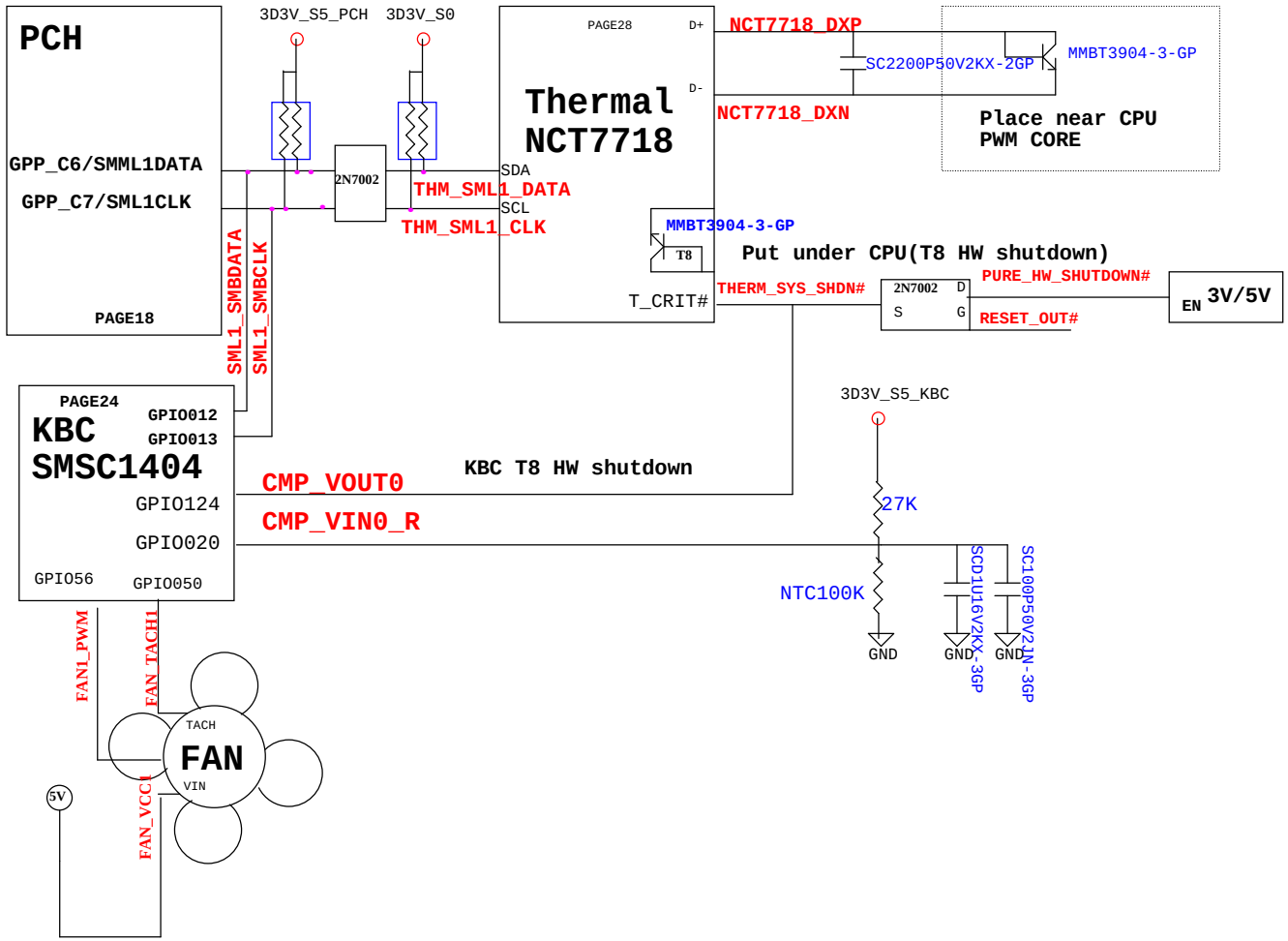
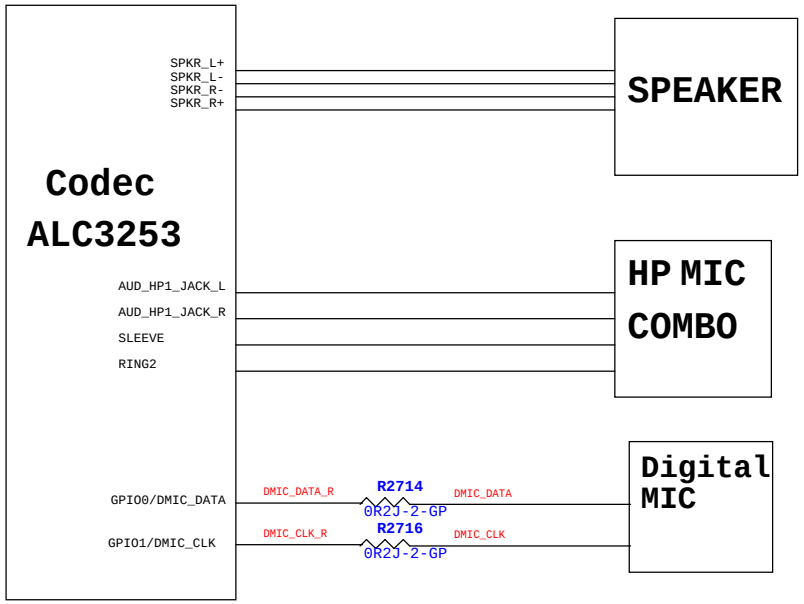
Thermal Block Diagram



Audio Block Diagram



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