Project Name: PIBTDL-Madrid Lite
Project Code: 3PD018010001
PCB Number : 13142-1
PCB Size : 150mmx240mm

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1801	CPU	25M	+/-30ppm CL:12P	C1814=12pF C1815=12pF
X1802	CPU	32.768K	+/-20ppm CL:7P	C1817=4pF C1818=4pF
X3	LAN	25M	+/-30ppm CL:12P	C294=15pF C295=15pF
X3501	HUB	12M	+/-20ppm CL:20P	C4603=18pF C4604=18pF
X5	SCALAR	14.318M	+/-20ppm CL:20P	C532=15pF C533=15pF
X7	GPU	27M	+/-30ppm CL:12P	C738=10pF C734=10pF

BOM Configuration

G_: GPU
GH_: Hynix VRAM and HW strap
GS_: Samsung VRAM and HW strap
NG_: Non-GPU
S_: Scalar
NS_: Non-Scalar
A_: AMP
NA_: Non-AMP
O_: OCP
O6_: 65W adaptor
O9_: 90W adaptor
R_: Reserve

CPU: INTEL BAY TRAIL-D
J2900 - KC.BTD01.29C
J1900 - KC.BTD01.19C
J1800 - KC.BTD01.18C
GPU: GT820M N15V-GM-S-A2
071.0N15V.0B0U
KG.VGM0V.002
GPU VRAM:
HYNIX H5TC2G63FFR-11C
KN.2GB0G.038
SAMSUNG K4W2G1646Q-BC1A
KN.2GB0B.040
MICRON MT41J128M16JT-093G:K
KN.2GB04.022

SIO: IT8732F
BX - 71.08732.00E
CX - 71.08732.A0E
SCALAR: RTD2486
71.02486.D0G
LAN: RTL8111GA
71.08111.Y03
Audio Codec: ALC269Q
71.00269.H03
Amplifier: TAS5707
74.05707.01T
USB3.0 redriver: PS8713
71.08713.003
SATA3.0 redriver: PS8520
71.08520.003
LVDS translator: RTD2136
71.02136.B04

KC.BTD01.29C : Bay Trail-D PENTIUM J2900 4C 2.4G C0
KC.BTD01.19C : Bay Trail-D CELERON J1900 4C 2.0G C0
KC.BTD01.18C : Bay Trail-D CELERON J1800 2C 2.4G C0

071.00BAY.0C6U : Bay Trail-D PENTIUM J2900 4C 2.4G C0
071.00BAY.0C4U : Bay Trail-D CELERON J1900 4C 2.0G C0
071.00BAY.0C5U : Bay Trail-D CELERON J1800 2C 2.4G C0

VRAM ID [0-3]:

Mount	Un-mount	VRAM Type	P/N
R488、R490、R489、R924	R483、R486、R929、R934	Hynix 1GHz H5TC2G63FFR-11C	KN.2GB0G.038
R483、R490、R929、R934	R488、R486、R489、R924	MICRON 1GHz MT41J128M16JT-093G:K	KN.2GB04.022
R488、R486、R489、R924	R483、R490、R929、R934	SAMSUNG 1G K4W2G1646Q-BC1A	KN.2GB0B.040

Mount 10K 64.10025.6DL

Madrid Lite UMA SKU : NS,NA,O,O6,NG
Madrid Lite GPU with Hynix SKU : NS,NA,O,O9,G,GH
Madrid Lite GPU with Samsung SKU : NS,NA,O,O9,G,GS

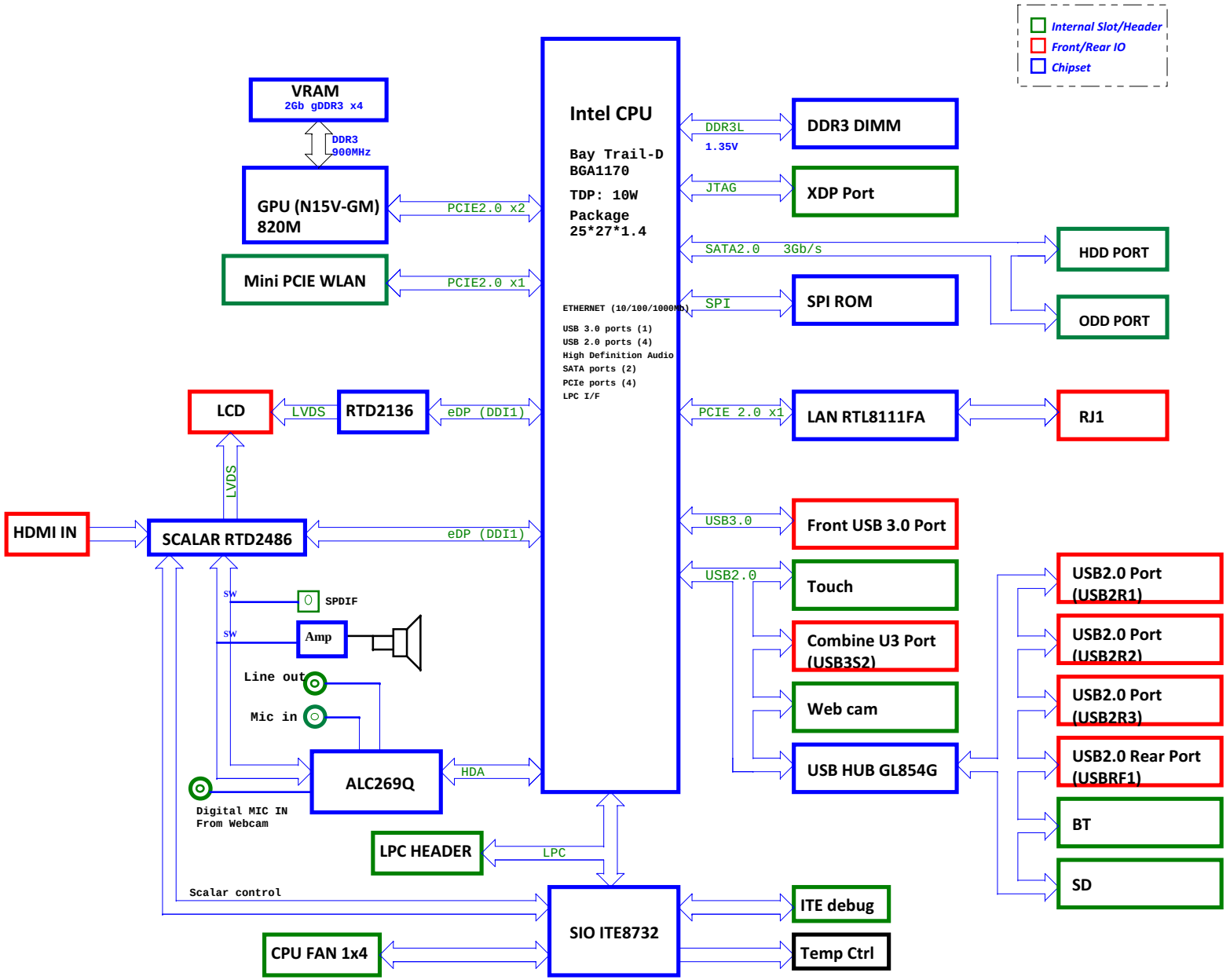
Madrid Lite

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Cover Page
Size: Custom | Document Number: Madrid Lite | Rev: 1A
Date: Friday, June 27, 2014 | Sheet 1 of 62

Project Name: PIBTDL-Madrid Lite
Project Code: 3PD018010001
PCB Version: -1
PCB Number : 13142-1
PCB Size : 150mmx240mm



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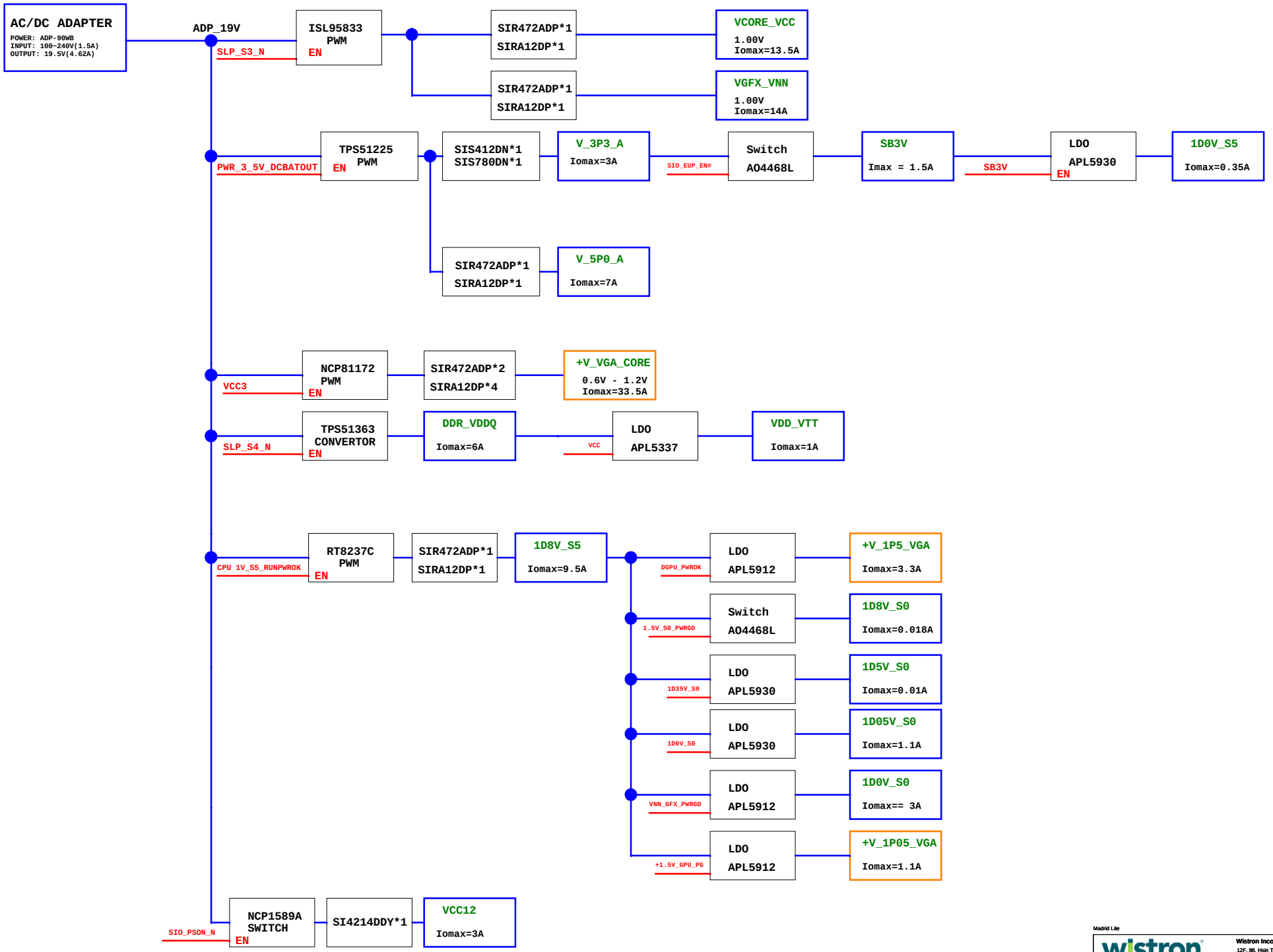
Hsichih, Taipei

Title: Block Diagram

Size: Custom | Document Number: Madrid Lite | Rev: 1A

Date: Monday, July 21, 2014 | Sheet 2 of 62



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Hsichih, Taipei

Title: Power Delivery

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Date: Wednesday, June 18, 2014 | Sheet 3 of 62

Power-up Sequencing for the BAY TRAIL-D Platform

Source	Destination	Signal
RTC Battery	CPU/SIO	RTC_VCC
RTC Battery	CPU/SIO	RTC_TEST# RTC_RST#
Adaptor	MB	DCBATOUT
VRs	CPU/SIO	V_3P3_A
Button	SIO	PWRBTN_N
SIO	VRs	SIO_EUP_EN#
VRs	MB	SB3V/SB5V
VRs	MB	1D0V_S5
VRs	MB	1D8V_S5
SIO	CPU	RSMRST_N
CPU	SIO	PMC_SUSCLK
CPU	MB	PMC_SUSPWRDNACK
SIO	CPU	PMC_PWBTN_N
CPU	SIO / VRs	SLP_S4#
VRs	MB	DDR_VDDQ
MB	CPU	DDR3_DRAM_PWROK
CPU	SIO / VRs	SLP_S3#
SIO	VRs	SIO_PSON#
VRs	MB	VCC12
VRs	CPU	VNN/VCORE
VRs	MB	1D0V_S0
VRs	MB	1D05V_S0
VRs	MB	1D35V_S0
VRs	MB	1D5V_S0
VRs	MB	1D8V_S0
VRs	MB	VCC3/VCC5
VRs	SO-DIMM	V_SM_VTT
SIO	MB	PWRGD_3V
SIO	CPU	PMC_CORE_PWROK
SIO	CPU	DRAM_CORE_PWROK
CPU	MB	PMC_SUS_STAT#
CPU	MB	PMC_PLTRST#

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Title: Power Sequence

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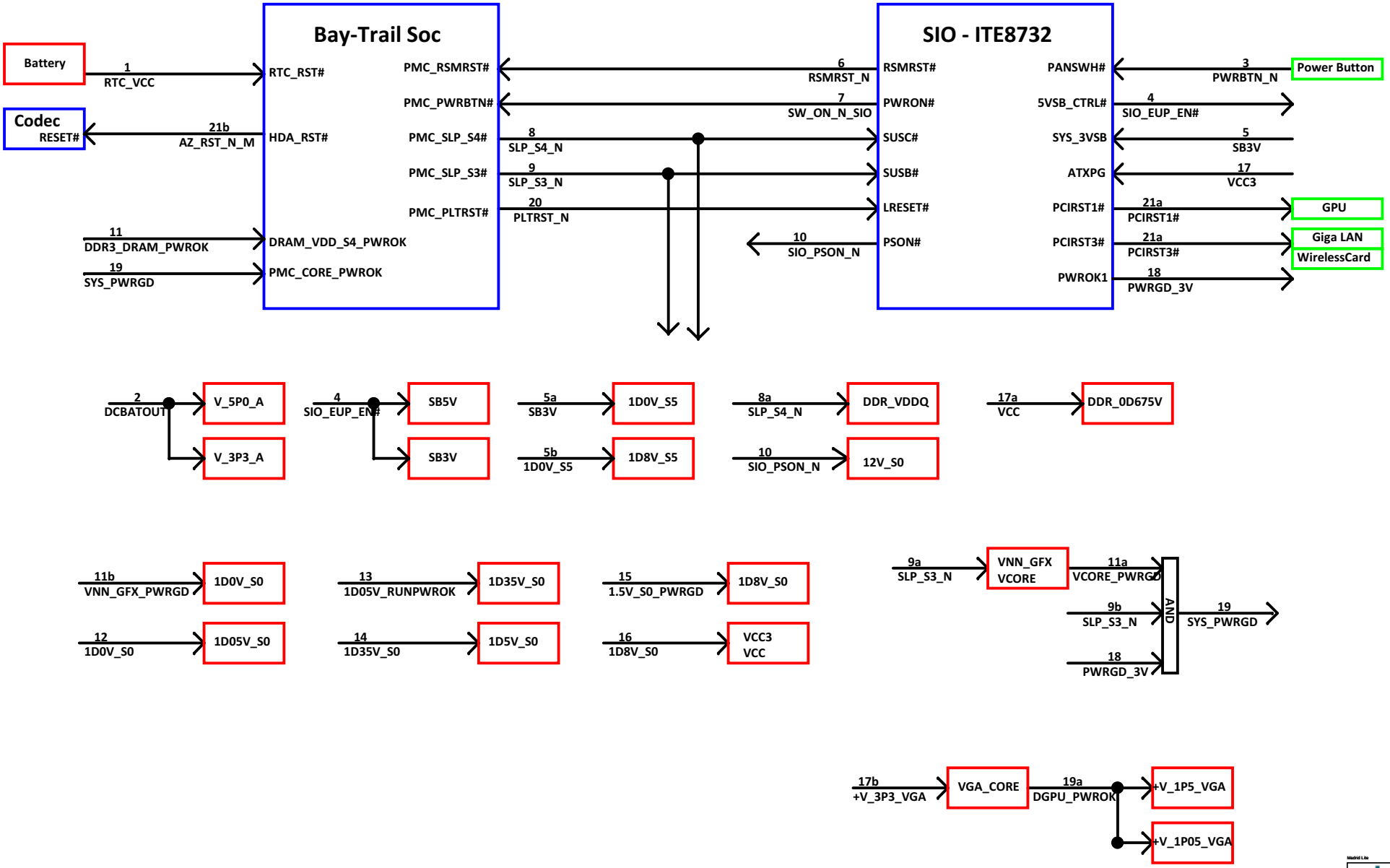
Date: Wednesday, June 18, 2014 | Sheet 4 of 62



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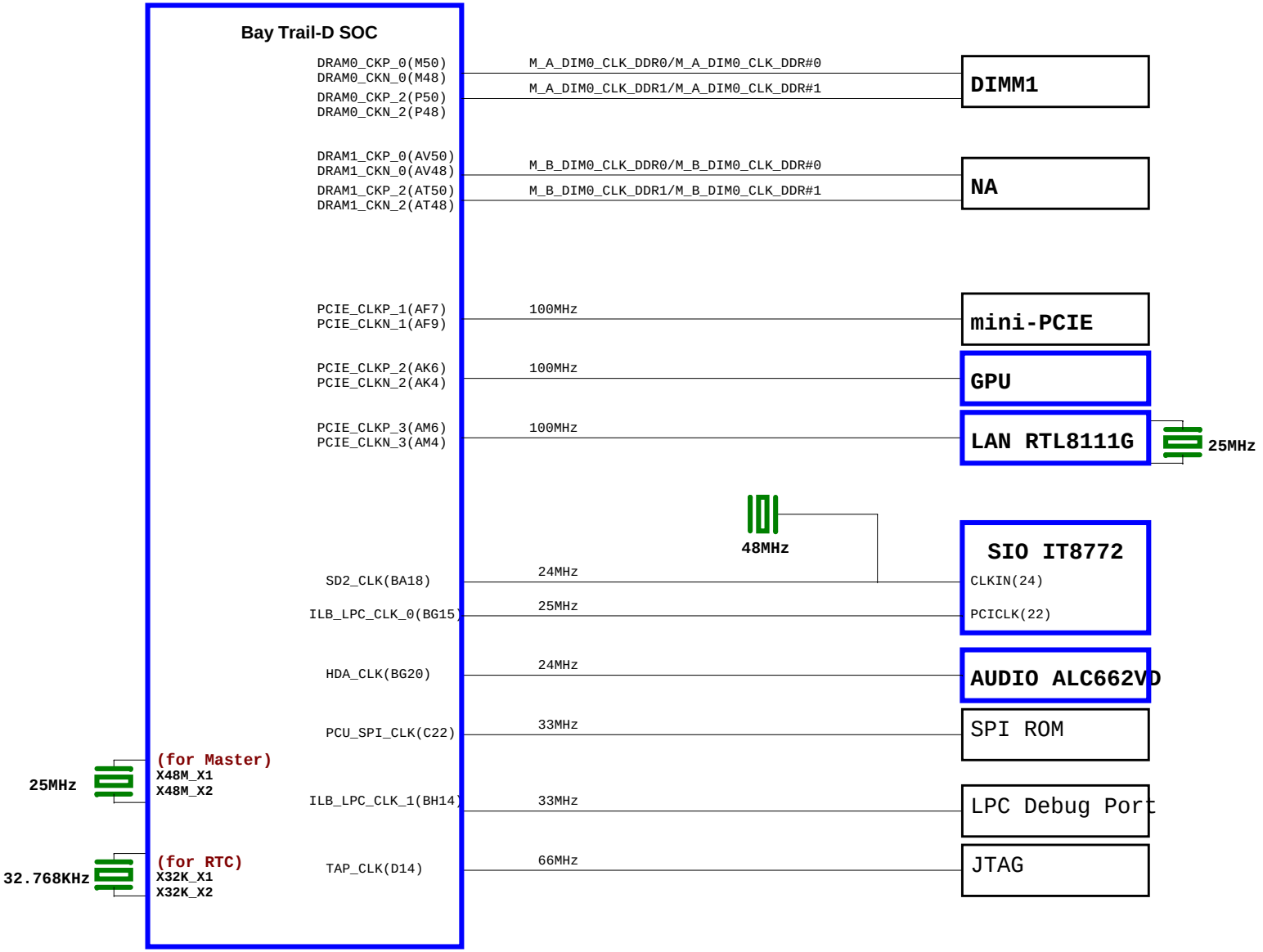
Title: Power Good & Reset Diagram

Size: D | Document Number: Madrid Lite | Rev: 1A

Date: Wednesday, June 18, 2014 | Sheet 5 of 62



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Title: Clock Map

Size: C | Document Number: Madrid Lite | Rev: 1A

Date: Friday, June 27, 2014 | Sheet 6 of 62

Dallas GPIO Table
Version: 2012/11/27

IC Pin Name	Power Well	Default	Default State	Signal Name	Usage	BIOS Programming					Comment
						S0	S1	S3	S4	S5	
GENINT1_L/GPIO32	VDD_33	null	Input, 15K PU	no use	no use						
GENINT2_L/GPIO33	VDD_33	null	Input, 15K PU	no use	no use						
SCL0/GPIO43	VDD_33	null	Input	SMB0_CLK	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SD_LED/GPIO45	VDD_33	null	Output	no use	no use						
SDA0/GPIO47	VDD_33	null	Input	SMB0_DATA	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SERIRQ/GPIO48	VDD_33	SERIRQ	Input, 15K PU	SERIRQ_N	SERIRQ	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GPIO49	VDD_33	GPIO49	Input	no use	no use						
GPIO50	VDD_33	GPIO50	Input, 15K PU	KEY0_TEST	BTN test	GPI	GPI	GPI	GPI	GPI	1K to 3D3V_S0
GPIO51	VDD_33	GPIO51	Input	TP51	no use						
FANOUT0/GPIO52	VDD_33	null	Output, 15K PU	no use	no use						
DEVSLP[0]/GPIO55	VDD_33	GPIO55	Input, 15K PU	TP29	no use						
FANIN0/GPIO56	VDD_33	null	Input, 15K PU	no use	no use						
GPIO57	VDD_33	GPIO57	Input, 15K PU	TP48	no use						
GPIO58	VDD_33	GPIO58	Input, 15K PU	TP49	no use						
DEVSLP[1]/GPIO59	VDD_33	GPIO59	Input, 15K PU	PANEL_OFF_R	panel ON/OFF	GPI	GPI	GPI	GPI	GPI	EC: 10K to 3D3V_A scalar: 10K to P3P3V
CLK_REQ0_L/ SATA_IS0_L/ SATA_ZP0_L/GPIO60	VDD_33	null	Input, 15K PU	BLANCLK_REQ_N_1	clock request (Reserved)						10k(R) to 3D3V_S0
CLK_REQ1_L/GPIO61	VDD_33	null	Input, 15K PU	CLK_PCIE_WLAN_REQ#	clock request (Reserved)						
CLK_REQ2_L/GPIO62	VDD_33	null	Input, 15K PU	no use	no use						
CLK_REQ3_L/ SATA_IS1_L/ SATA_ZP1_L/GPIO63	VDD_33	null	Input, 15K PU	no use	no use						
GPIO64	VDD_33	GPIO64	Input, 15K PU	SMBUS_ISP	scalar FW	GPO L	GPO L	GPO L	GPO L	GPO L	100k to GND controlled by SW tool
CLK_REQG_L/GPIO65/ OSCIN	VDD_33	null	Input, 15K PU	PEG_CLKREQ#	clock request (Reserved)						
SPKR/GPIO66	VDD_33	SPKR	Output	SPKR	beep	Native	Native	Native	Native	Native	
SATA_ACT_L/GPIO67	VDD_33	SATA_ACT_L	Output	no use	no use						
GPIO68	VDD_33	GPIO68	Input, 15K PU	SYS_ID2	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO69	VDD_33	GPIO69	Input, 15K PU	SYS_ID3	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO70	VDD_33	GPIO70	Input, 15K PU	APU_PROCHOT#_R	thermal (Reserved)						1K to 3D3V_S0
GPIO71	VDD_33	GPIO71	Input	SYS_ID1	SYS ID	GPI	GPI	GPI	GPI	GPI	
SD_CLK/SCLK_2/ GPIO73	VDD_33	null	Input, 50K PU	no use	no use						
SD_CMD/GPIO74	VDD_33	null	Input, 50K PU	no use	no use						
SD_CD/GPIO75	VDD_33	null	Input, 50K PU	no use	no use						
SD_WP/GPIO76	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA0/ SDATI_2/ GPIO77	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA1/ SDATO_2/ GPIO78	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA2/GPIO79	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA3/GPIO80	VDD_33	null	Input, 50K PU	no use	no use						
SPI_WP_L/GPIO161	VDD_33_ALW	SPI_WP_L	Input	ROM_RST#	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CLK/GPIO162	VDD _33	SPI_CLK	Input, 15K PD	SPI_CLK	SPI	Native	Native	Native	Native	Native	
SPI_DO/GPIO163	VDD_33_ALW	SPI _ DO	Input, 15K PD	SPI_DATAOUT	SPI	Native	Native	Native	Native	Native	
SPI_DI/GPIO164	VDD_33_ALW	SPI _ DI	Input, 15K PD	SPI_DATAIN	SPI	Native	Native	Native	Native	Native	
SPI_CS1_L/GPIO165	VDD _33	SPI _ CS 1_ L	Input, 15K PU	SPI_CS0_N	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CS2_L/GPIO166	VDD _33	SPI _ CS 2_ L	Input, 15K PU	EDID_RDY	EDID for APU	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5
AZ_SDIN0/GPIO167	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN0	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN1/GPIO168	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN1	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN2/GPIO169	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN2	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_SDIN3/GPIO170	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_SDIN3	AZ	Native	Native	Native	Native	Native	10k(R) to GND
GPIO174	VDD_33_ALW	GPIO 174	Input	Wake#_PCIE	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
IR_LED_L/LLB_L/GPIO184	VDD_33_ALW	null	Input, 15K PU	Wake#_LOM	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SCL1/GPIO227	VDD_33_ALW	null	Input	SMB1_CLK	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
SDA1/GPIO228	VDD_33_ALW	null	Input	SMB1_DATA	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
GA20IN/GEVENT0#	VDD_33	GA 20 IN	Input, 15K PU	KA20GATE	GA20IN	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GEVENT2#	VDD_33_ALW	null	Input, 15K PU	SPI_SW	only strapping						strap low
LPC_PME#/ GEVENT3#	VDD_33_ALW	null	Input, 15K PU	PME#_M	LPC	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
GEVENT4#	VDD_33_ALW	null	Input	THERMAL_SHUT#	thermal (Reserved)						10k(R) to 3D3V_S5
LPC_PD#/ GEVENT5#	VDD_33_ALW	null	Output	TP_LPC_PD#	no use						
IR_TX1/ GEVENT6#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT7#	VDD_33_ALW	null	Input	EC_SMI#	(Reserved)						10k to 3D3V_S5
WAKE#/ GEVENT8#	VDD_33_ALW	null	Input, 15K PU	PCIE_WAKE#	wake up	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	Strap	Input	SST_HOLDJ_1_R	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
GEVENT10#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT11#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC0#/ SPI_TPM_CS#/ TRST#/ GEVENT12#	VDD_33_ALW	USB_OC0#	Input, 15K PU	USB_OC_01	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OC1#/TDI/ GEVENT13#	VDD_33_ALW	null	Input, 15K PU	USB_OC_23	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
AC_PRES/IR_RX0/ GEVENT16#	VDD_33_ALW	null	Input, 15K PU	AC_PRES	no use						
GEVENT17#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
BLINK/ GEVENT18#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
SYS_RESET#/ GEVENT19#	VDD_33_ALW	SYS_RESET_L	Input, 15K PU	FP_RST_N	no use						
IR_RX1/ GEVENT20#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
IR_TX0/ GEVENT21#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT22#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
LPC_SMI#/ GEVENT23#	VDD_33_ALW	null	Input, 15K PU	no use	no use						

IC Pin Name	Power Well (GPIO)	Default	Default State	Signal Name	Usage	Open Drain / Push Pull	BIOS Programming					Comment
							S0	S1	S3	S4	S5	
PCIRST3#/GP10	3VSB	PCIRST3#	Native	AMP_PDN#	mute	DO/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC H: ON, L: OFF/mute
PCIRST2#/GP11	3VSB	PCIRST2#	Native	PCIRST2#	RESET	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PCIRST1#/GP12	3VSB	PCIRST1#	Native	PCIRST1#	RESET	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PWROK1/GP13	3VSB	PWROK1	Native	PWROK3_1	PWROK	DOD/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_S0 set delay to 200ms
VCORE_EN/PCH_C1/GP14	3VSB	VCORE_EN	Native	LAN_PWR_EN	LAN power (reserved)	DOD/DIOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	390k to 3D3V_S5
PCIRSTIN#/CIRTX2/GP15/CPU_PG	3VSB	CIRTX2	Native	SIO_PCIRSTIN#	RESET	DI/DOD/DIOD/DOD	Native	Native	Native	Native	Native	10k to 3D3V_A
5VSB_CTRL#/ CIRRX2/GP16	3VSB	5VSB_CTRL#	Native	EC_EUP	EUP	DOD/DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
RI2#/GP17	3VSB	null		SPI_WP_R_N	SPI WP	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A H: can be write L: write protect
CTS2#/GP20	3VSB	GP20		PANEL_SW_EC	panel ON/OFF	DI/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
DCD2#/GP21	3VSB	GP21		PANEL_CTRL	panel ctrl (reserved)	DI/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
SCK/GP22	3VSB	GP22		SIO_SCK_R	EC EPROM	DO/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
SI/GP23	3VSB	GP23		SIO_SI	EC EPROM	DO/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
RTS2#/GP24	3VSB	GP24		THERMAL_SHUT#_SIO	thermal (reserved)	DO/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k(R) to 3D3V_S5
DSR2#/GP25	3VSB	GP25		SIO_Audio_Mute	mute (reserved)	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A
SOUT2/GP26	3VSB	GP26		SIO_UART1_TX	UART	DO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
SIN2/GP27	3VSB	GP27		SIO_UART1_RX	UART	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A
ATXPG/GP30	3VSB	ATXPG	Native	SIO_ATXPG	sequence	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S0
PWMOUT/GP31	3VSB	PWMOUT	Native	W3_DISABLE_N	wake up	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
DPWROK/GP32	3VSB	DPWROK	Native	W1_DISABLE_N	wake up	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
SUSACK#/GP33	3VSB	SUSACK#	Native	SIO_BOARD_ID3	board ID	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	controlled by EC H: scalar, L: non-scalar
SUSWARN#/GP34	3VSB	SUSWARN#	Native	SIO_BOARD_ID2	board ID	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	board stage
FAN_TAC4/GP35	3VSB	FAN_TAC4	Native	SIO_BOARD_ID1	board ID	DI/DIOD	GPI	GPI	GPI	GPI	GPI	board stage
FAN_CTL3/GP36	3VSB	FAN_CTL3	Native	no use	no use	DOD/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	
FAN_TAC3/GP37	3VSB	FAN_TAC3	Native	EC_AMP_RST	mute	DI/DIOD	GPO L	GPO L	GPO L	GPO H	GPO H	10k to 3D3V_A controlled by EC H: reset/mute, L: normal
3VSBSW#/GP40	3VSB	3VSBSW#	Native	SLP_S3_N_R3	sequence	DOD/DIOD	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5 controlled by EC
PWROK2/GP41	3VSB	PWROK2	Native	PWROK3_2	PWROK (reserved)	DOD/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
PSON#/GP42	3VSB	PSON#	Native	SIO_PSON_N	S0 power (reserved)	DOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_A
PANSWH#/GP43	3VSB	PANSWH#	Native	PB_IN_N_1	PWR BTN	DI/DIOD	Native	Native	Native	Native	Native	330k to 3D3V_A
PWRON#/GP44	3VSB	PWRON#	Native	SW_ON_N_SIO	sequence	DOD/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
D_RX0/SMCLK2/ GP46	3VSB	null		SMBCLK2_SIO	SIO SMBUS2	DI/DIO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
D_TX0/SMDAT2/ GP47	3VSB	null		SMBDAT2_SIO	SIO SMBUS2	DO/DIO/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
SO/GP50	3VSB	SO	Native	SIO_SO	EC EPROM	DI/DIOD	Native	Native	Native	Native	Native	1k to 3D3V_A
FAN_CTL2/GP51	3VSB	FAN_CTL2	Native	SUSLED_R_N	LED	DOD/DIOD	Native	Native	Native	Native	Native	10k to USB30_VCCA
FAN_TAC2/GP52	3VSB	FAN_TAC2	Native	EC_SMI#	(Reserved)	DI/DIOD	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SUSC#/GP53	3VSB	SUSC#	Native	SLP_S5_N_R	sequence	DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
PME#/GP54	3VSB	PME#	Native	LPC_PME_N	LPC	DOD/DIOD	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
RSMRST#/CIRRX1/GP55	3VSB	RSMRST#	Native	ICH_RSMRST_N_R	sequence	DOD/DI/DIOD	Native	Native	Native	Native	Native	10k to 3D3V_S5
MCLK/GP56	3VSB	MCLK	Native	MCLK	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
MDAT/GP57	3VSB	MDAT	Native	MDAT	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KCLK/GP60	3VSB	KCLK	Native	KBCLK	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KDAT/GP61	3VSB	KDAT	Native	KDAT	no use	DIOD/DIOD	Native	Native	Native	Native	Native	10k to 5V_S5
KRST#/GP62	3VSB	KRST#	Native	KBRST_N	KBRST	DO/DIOD	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
SLP_SUS#/VLDT_EN/GP63	3VSB	SLP_SUS#	Native	APU_PROCHOT#	(Reserved)	DI/DOD/DIOD	GPI	GPI	GPI	GPI	GPI	1k to 3D3V_S0 controlled by EC
GP70/KSI0	3VSB	KSI0	Native	DET_HDMI	scalar/HDMI	DIOD/DI	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP71/KSI1	3VSB	KSI1	Native	SCALAR_EN	scalar/HDMI	DIOD/DI	GPO H	GPO H	GPO H	GPO L	GPO L	10k to 3D3V_A controlled by EC H: enable scalar
GP72/KSO0	3VSB	KSO0	Native	EUP_DSW_SEL	strap	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A ?
GP73/KSO1	3VSB	KSO1	Native	SIO_PANEL_ON	panel ON/OFF	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel ON
GP74/KSO2	3VSB	KSO2	Native	SIO_PANEL_OFF	panel ON/OFF	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel OFF
GP75/KSO3	3VSB	KSO3	Native	LVDS_BL_EN_1	panel ON/OFF	DIOD/DO	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP76/KSO4	3VSB	KSO4	Native	no use	no use	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	
GP77/KSO5	3VSB	KSO5	Native	SIO_MEM_EVENT_L	power consum. (reserved)	DIOD/DO	GPO H	GPO H	GPO H	GPO H	GPO H	controlled by EC
IO_SCI#/GP85/SMDAT0	3VSB			SIO_SMDAT0	SIO SMBUS0	DO/DIOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC
GP86/SMCLK0	3VSB			SIO_SMCLK0	SIO SMBUS0	DIOD/DIOD	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC

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Title: GPIO Table

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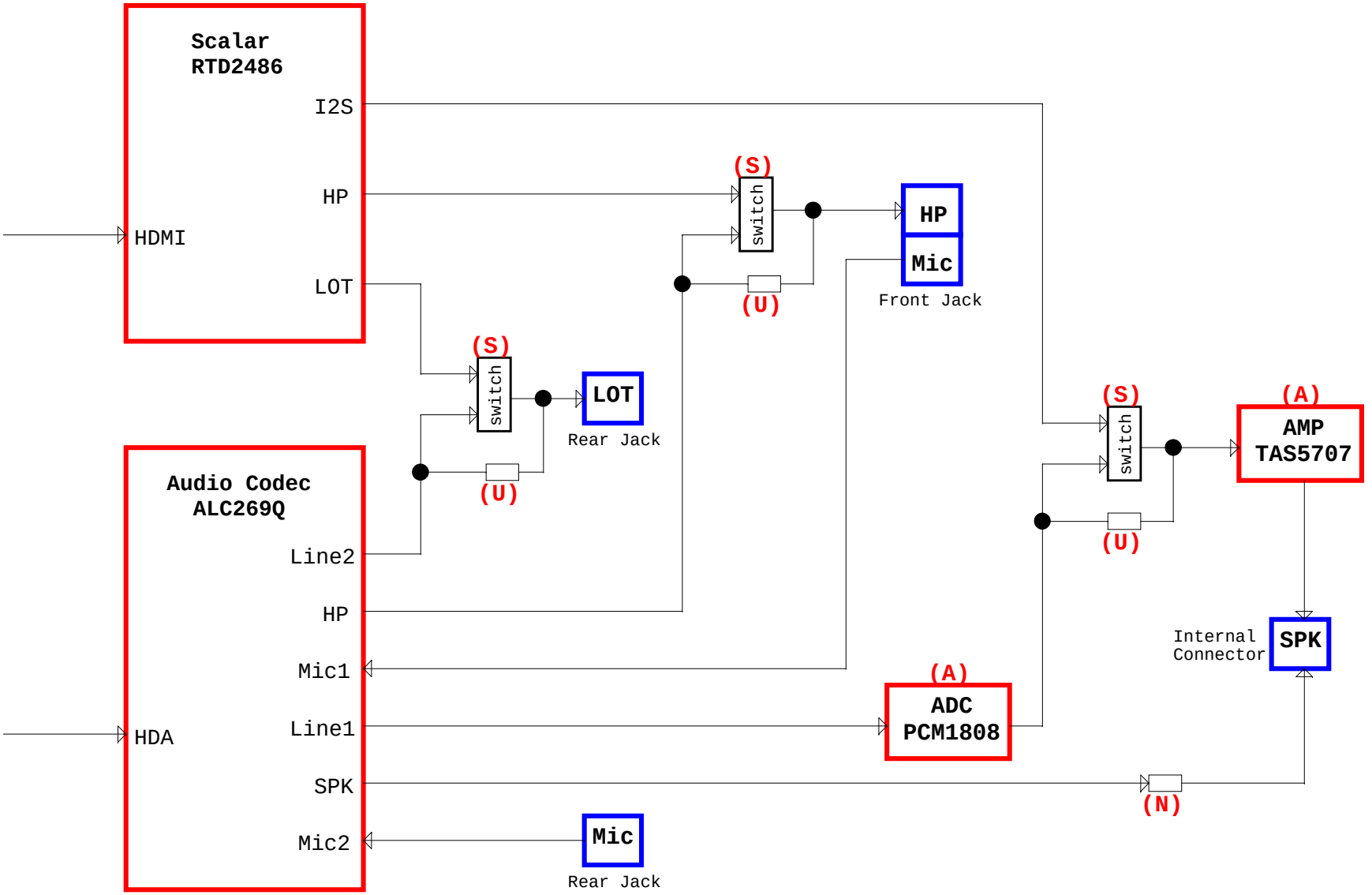

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Title: Audio Block Diagram

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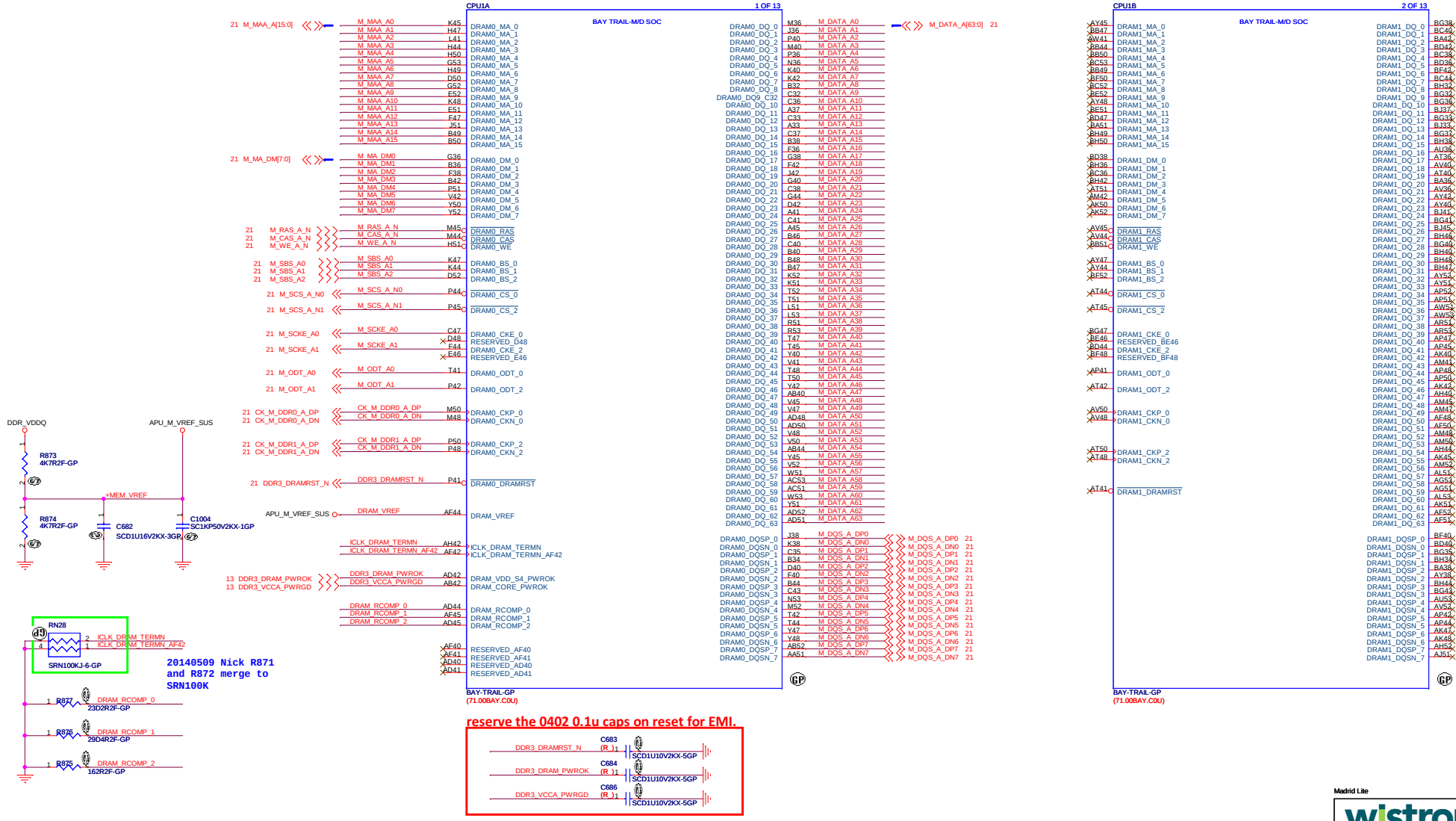

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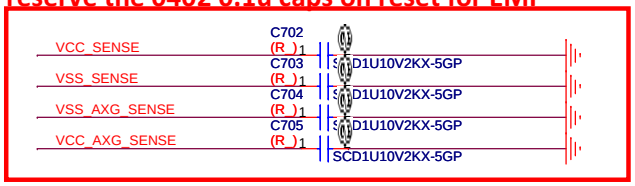
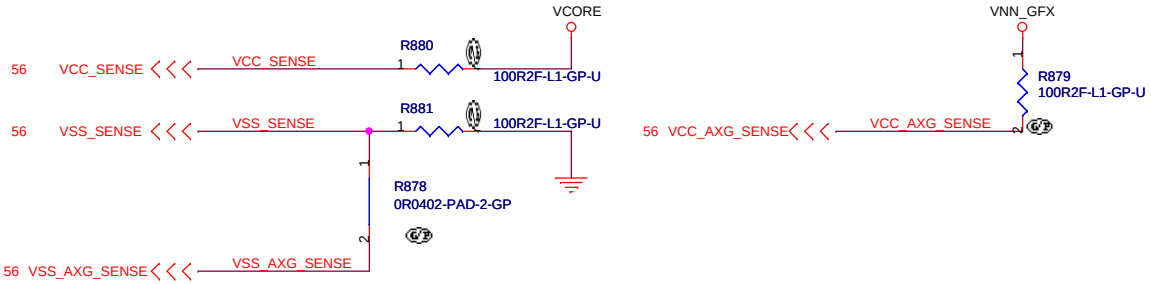
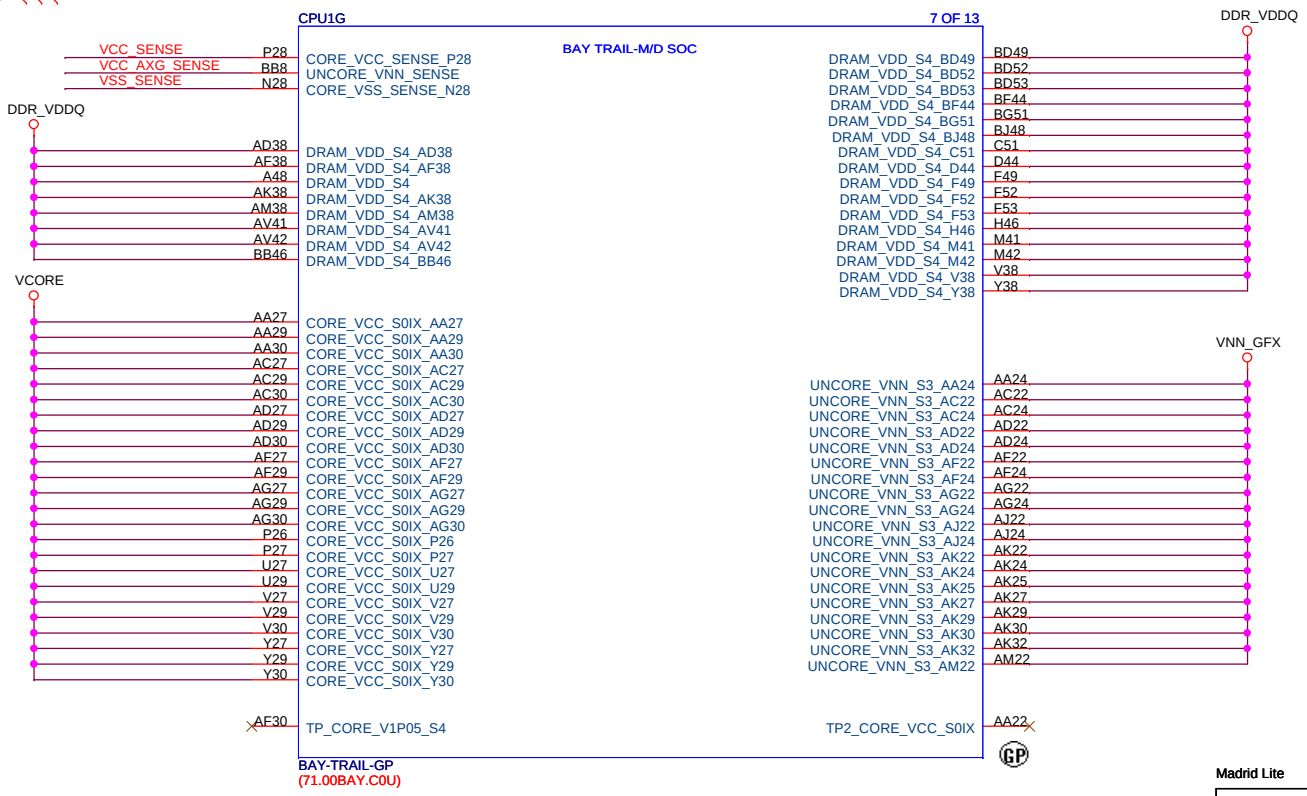
reserve the 0402 0.1u caps on reset for EMI







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Title: CPU (VCC CORE)

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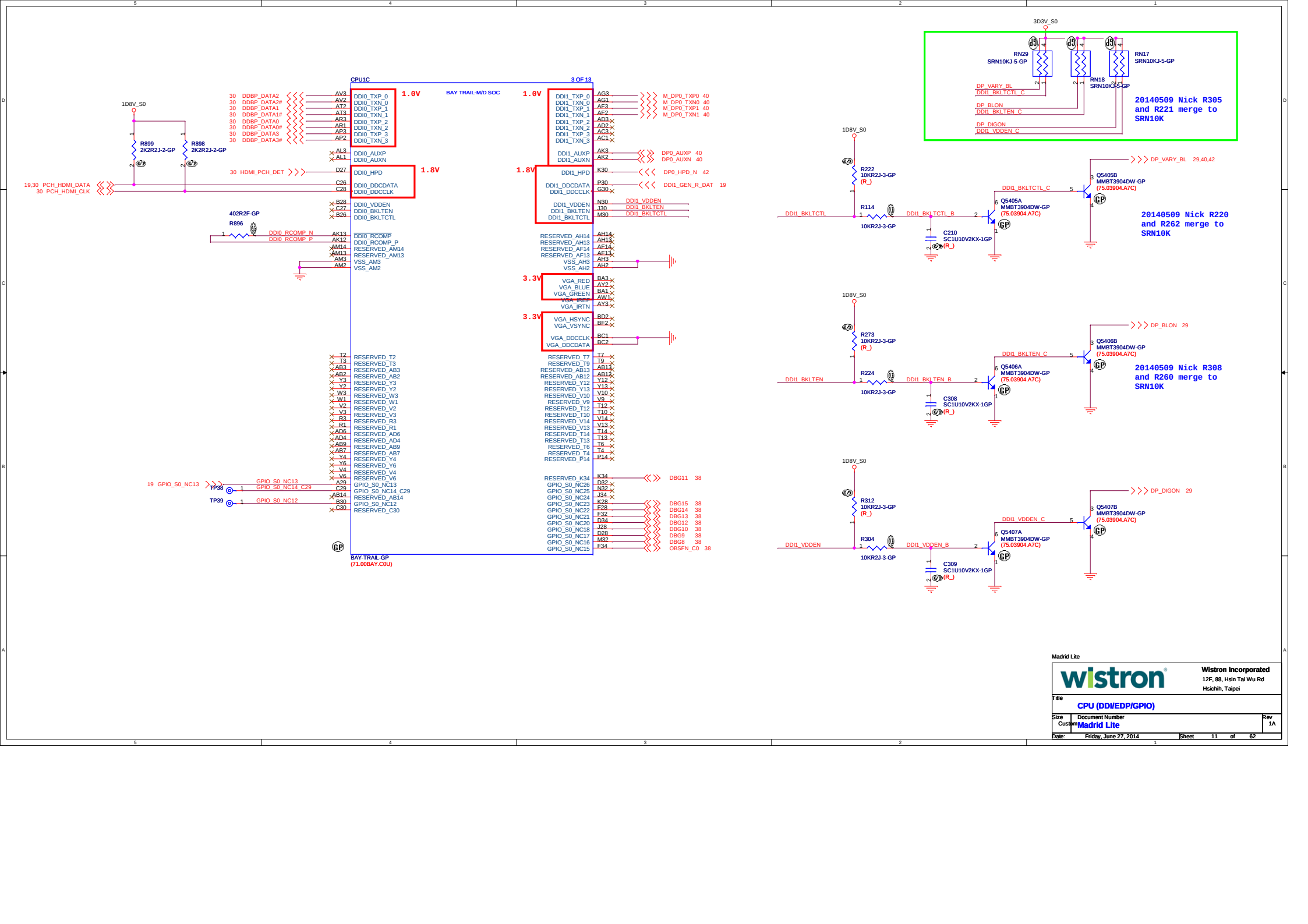

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Title: CPU (DDI/EDP/GPIO)

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USB Table

Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	TOUCH1

Make sure the signal routing is as short as possible
and isolated from high speed data signal.
Parasitic resistance for the overall routing should be less than 100 Ω.

PANEL OFF

KEY TEST

	ID1	ID2	ID3
Default	0	0	0
	1	1	1

SYSID1	GPU	UMA
GPIO_S0_SC_058	1	0
	0	1

20140509 Nick R1225 and R1226 merge to SRN2.2K

LPC DEBUG PORT

Pin height 2.3mm

Layout Close SIO

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Size	C
Document Number	Madrid Lite
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Date:	Friday, July 18, 2014
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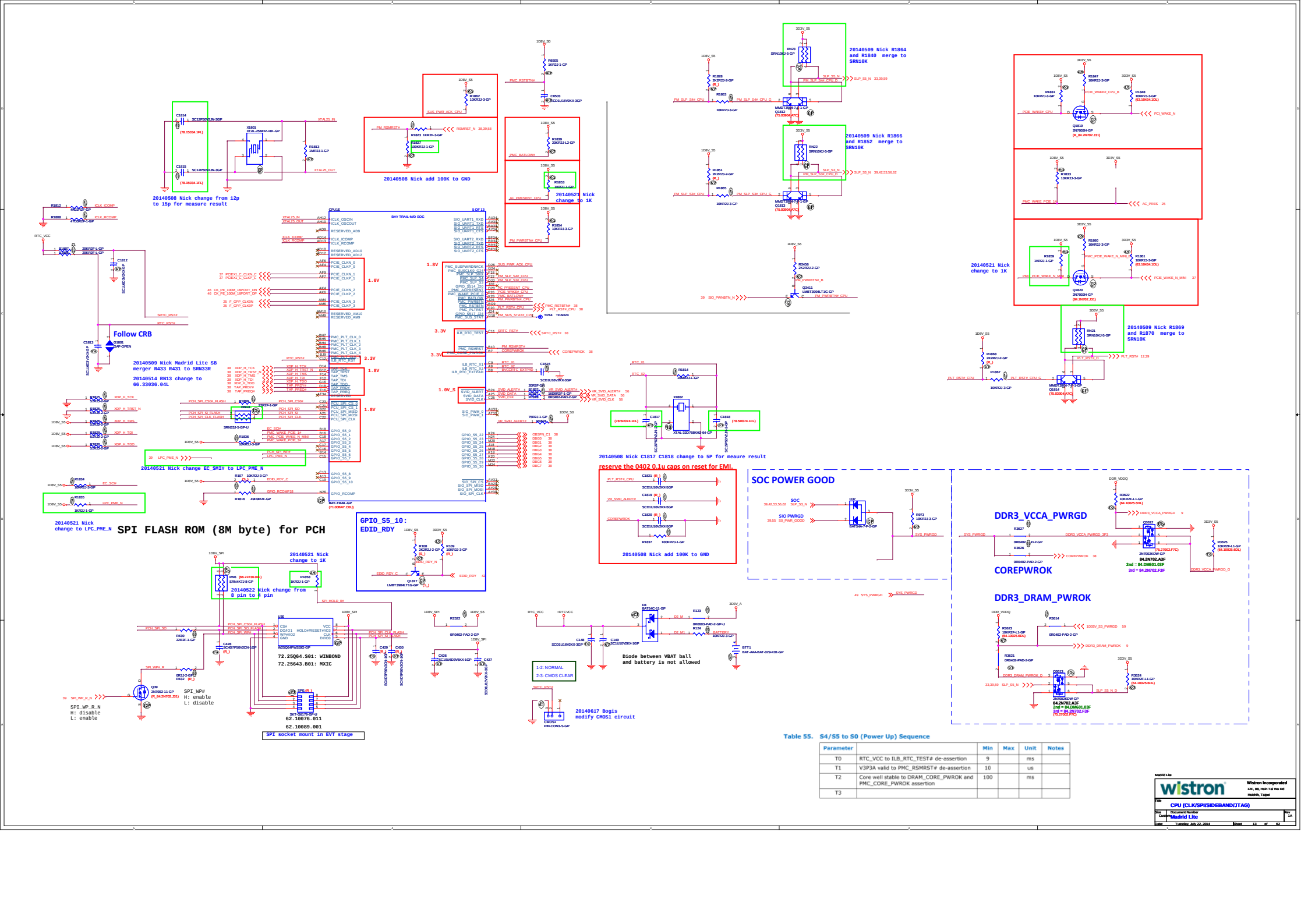

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

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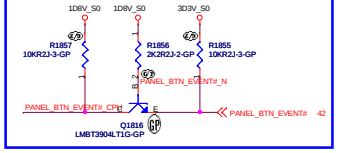
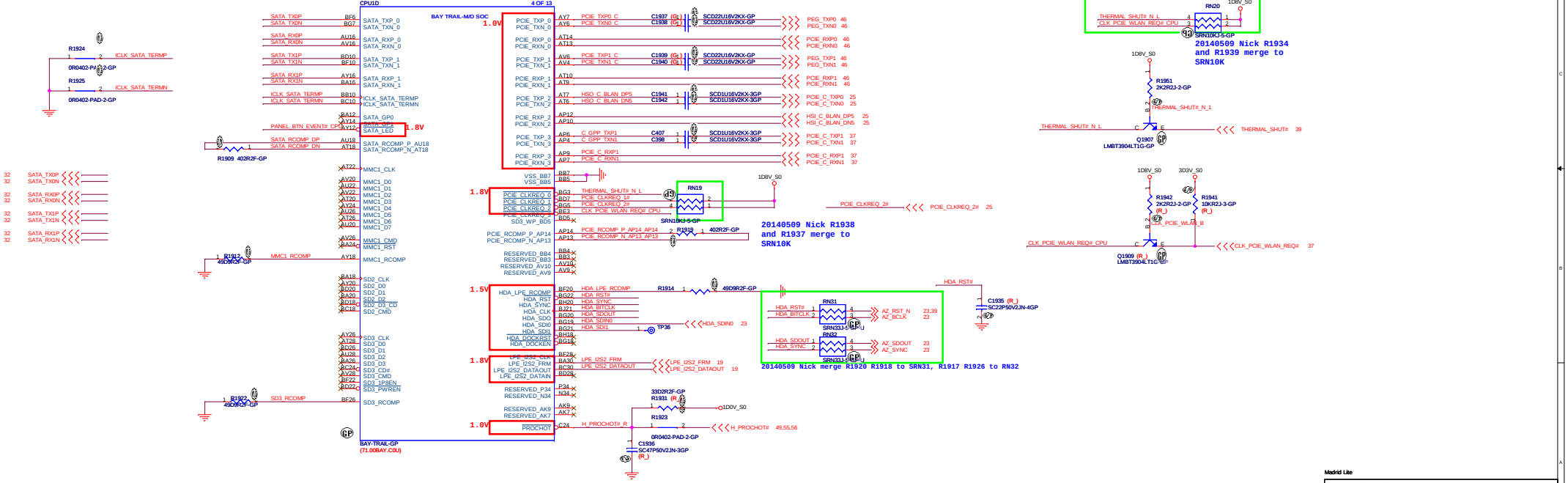
GPIO_S0_SC[002]/SATA_LED#





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Title: CPU (SATA/PCIE/IHDA)		
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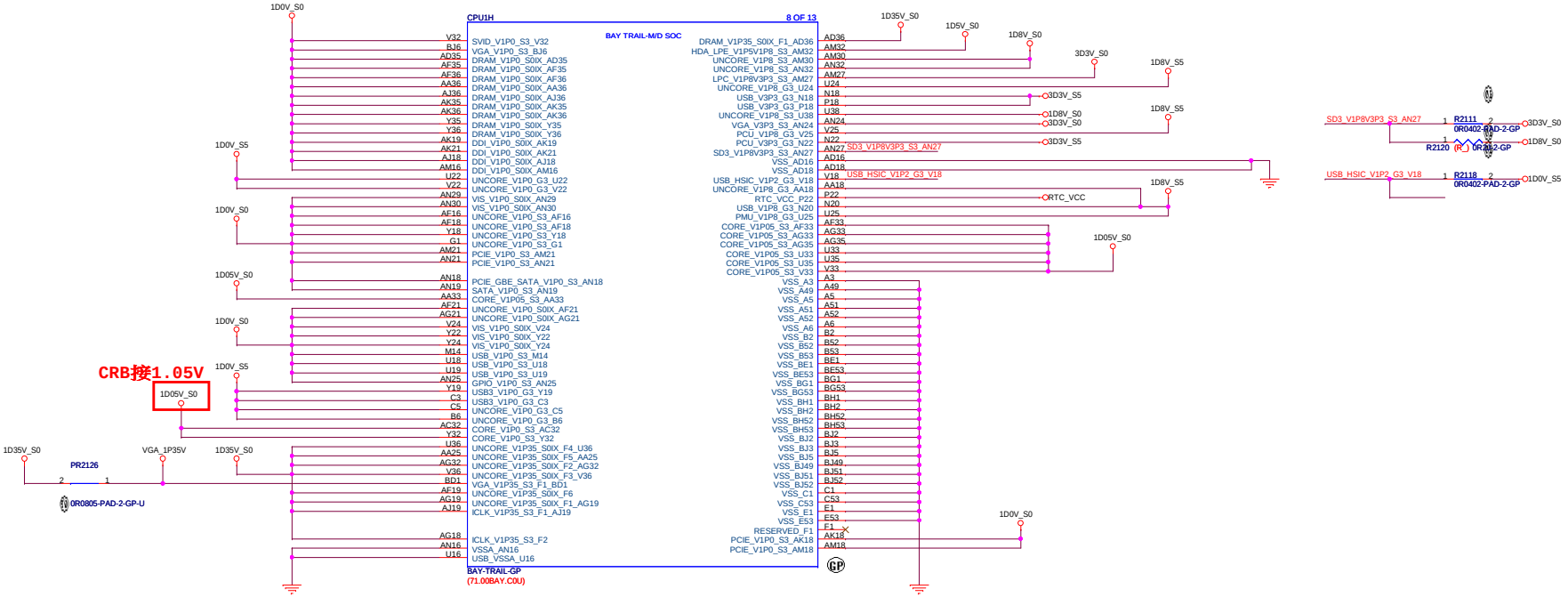

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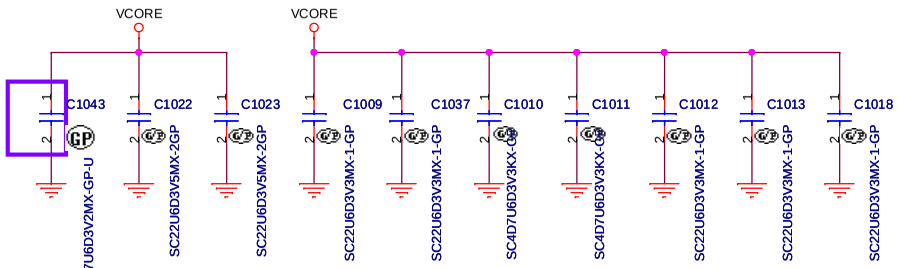
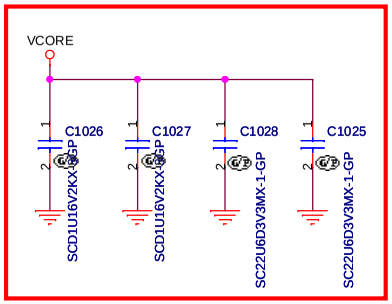
VCORE

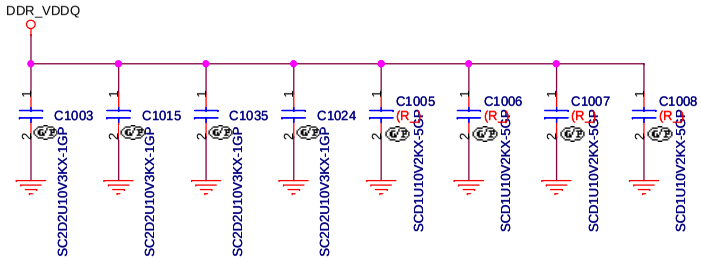


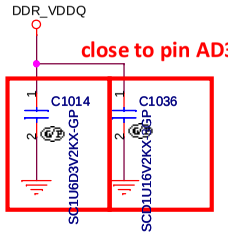
reserve the 0402 0.1u caps on reset for EMI(5/9).



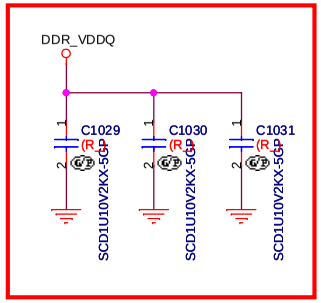
20150515 Nick add for power request

DDR_VDDQ

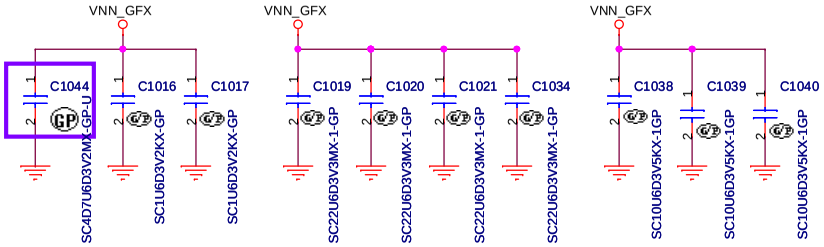




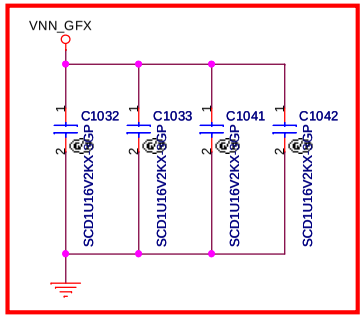
reserve the 0402 0.1u caps on reset for EMI(5/9).



VNN_GFX



reserve the 0402 0.1u caps on reset for EMI(5/9).



20150515 Nick add for power request

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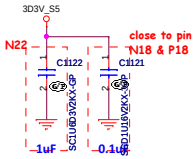
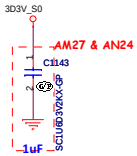
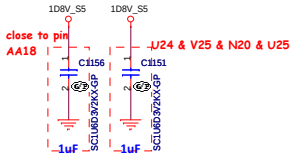
3D3V_S5



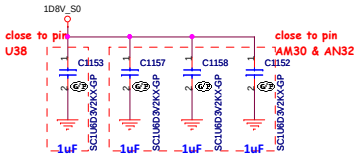
3D3V_S0



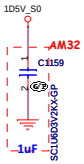
1D8V_S5



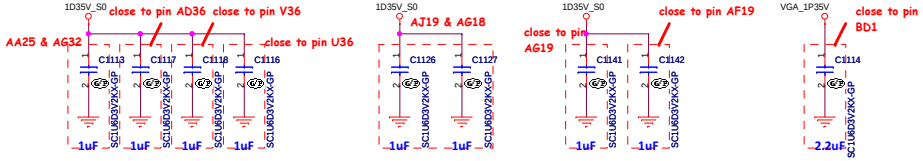
1D8V_S0



1D5V_S0

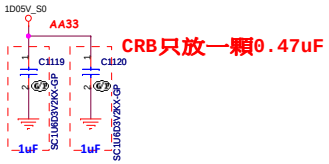


1D35V_S0

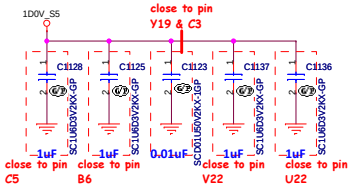


VGA_1P35V

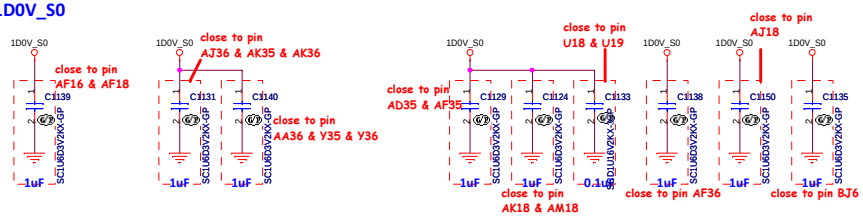
1D05V_S0

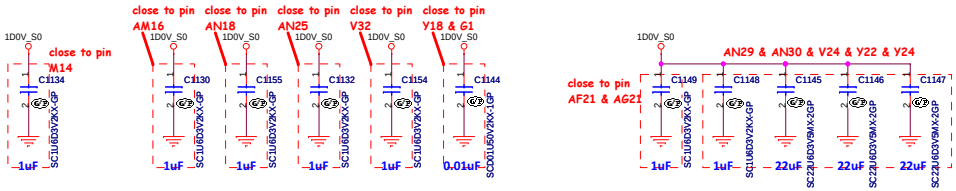


1D0V_S5



1D0V_S0





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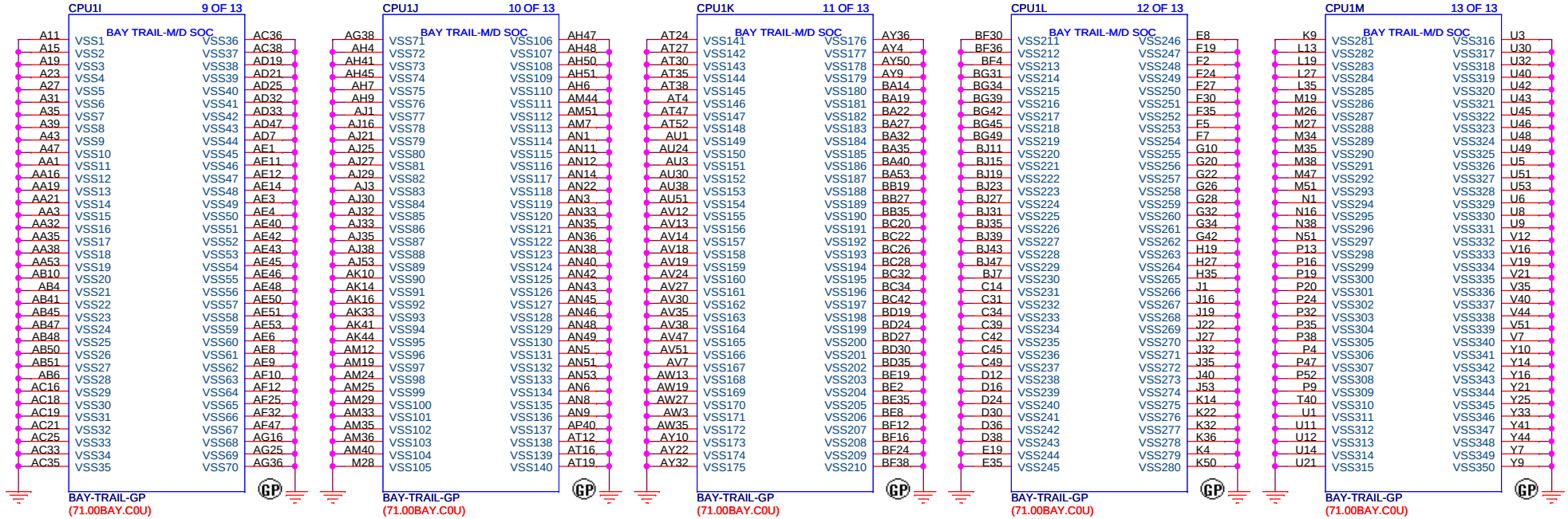

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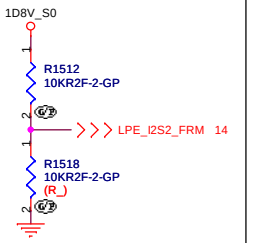
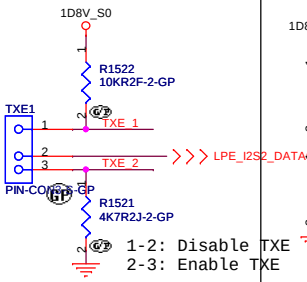
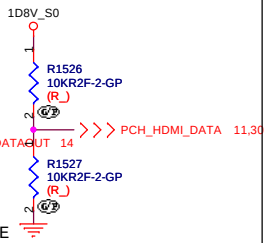
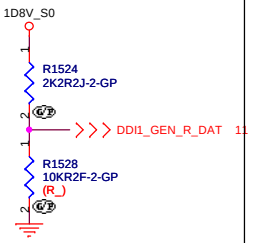
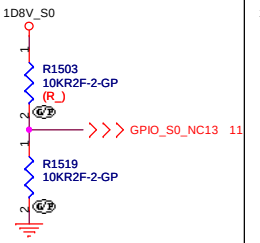
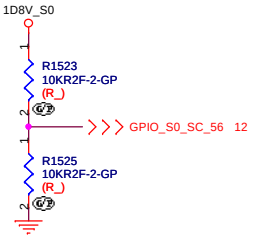
STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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Title: DDR3L-SODIMM1

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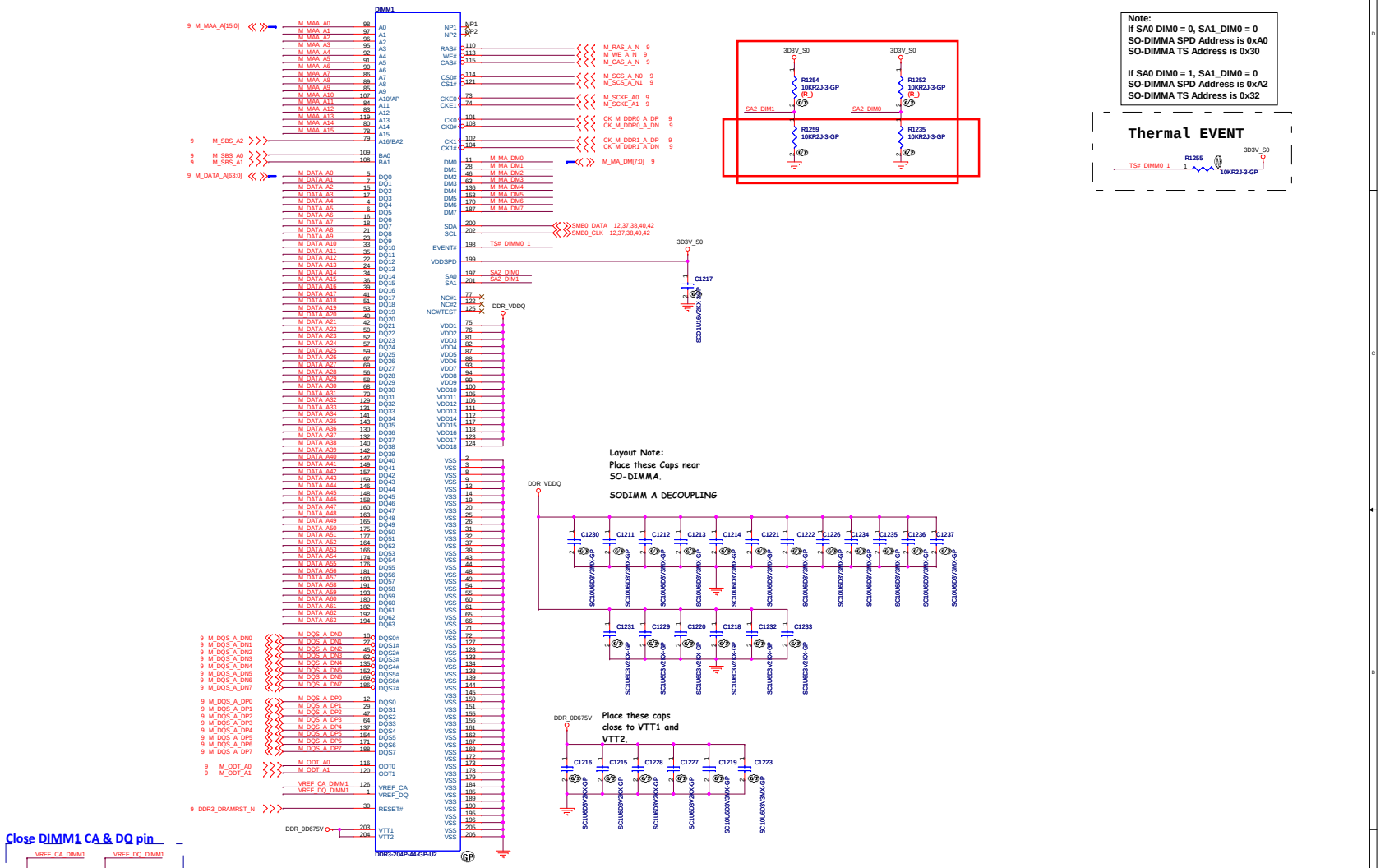

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Title: DDR3L-SODIMM2

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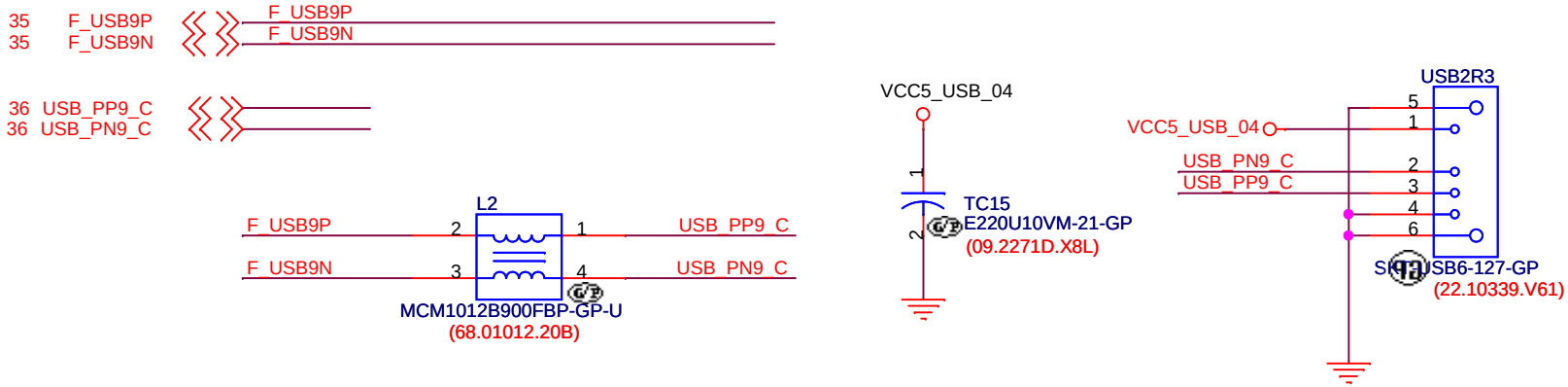

22.10339.V61

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Title: Front BD Connector

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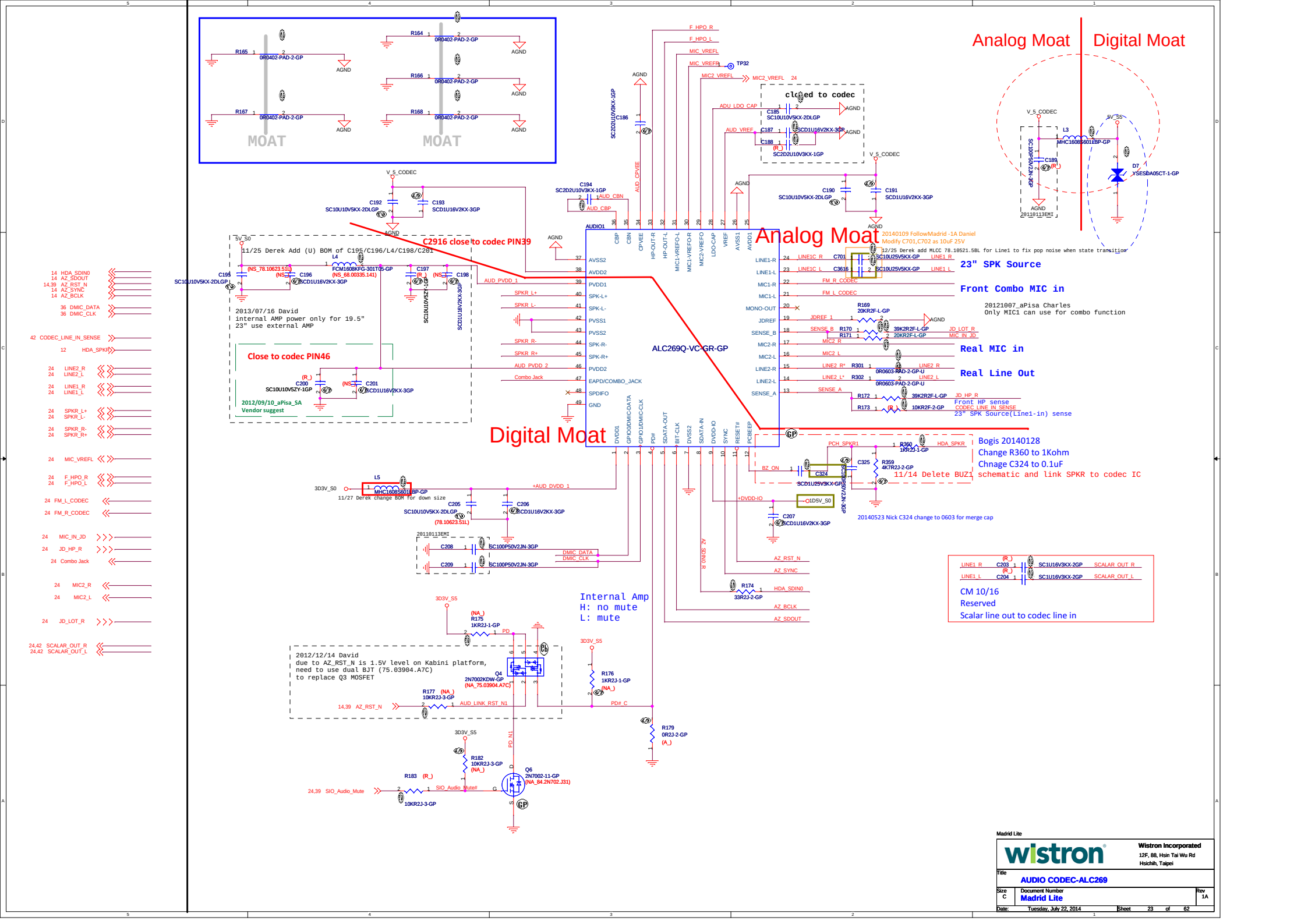
Analog Moat
Digital Moat
MOAT
MOAT
C2916 close to codec PIN39
Close to codec PIN46
11/25 Derek Add (U) BOM of C195/C196/L4/C198/C201
2013/07/16 David
internal AMP power only for 19.5"
23" use external AMP
2012/09/10_aPisa_SA
Vendor suggest
ALC269Q-VC-GR-GP
Analog Moat
20140109 FollowMadrid -1A Daniel
Modify C701,C702 as 10uF 25V
12/25 Derek add MLCC 78.10521.5BL for Line1 to fix pop noise when state transition
23" SPK Source
Front Combo MIC in
20121007_aPisa Charles
Only MIC1 can use for combo function
Real MIC in
Real Line Out
Front HP sense
23" SPK Source(Line1-in) sense
Digital Moat
Bogis 20140128
Change R360 to 1Kohm
Chnage C324 to 0.1uF
11/14 Delete BUZ1 schematic and link SPKR to codec IC
20140523 Nick C324 change to 0603 for merge cap
Internal Amp
H: no mute
L: mute
2012/12/14 David
due to AZ_RST_N is 1.5V level on Kabini platform,
need to use dual BJT (75.03904.A7C)
to replace Q3 MOSFET
CM 10/16
Reserved
Scalar line out to codec line in
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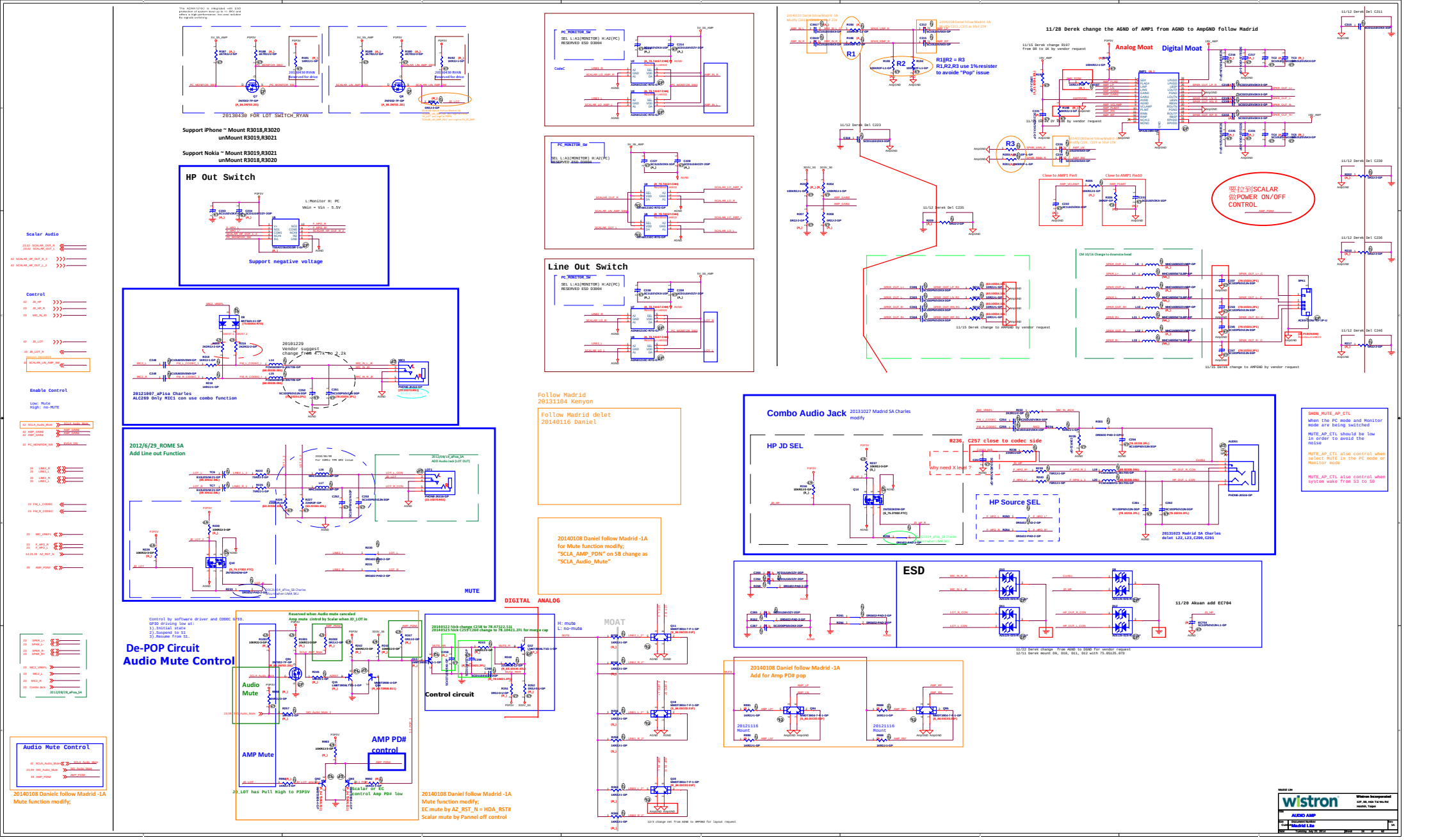
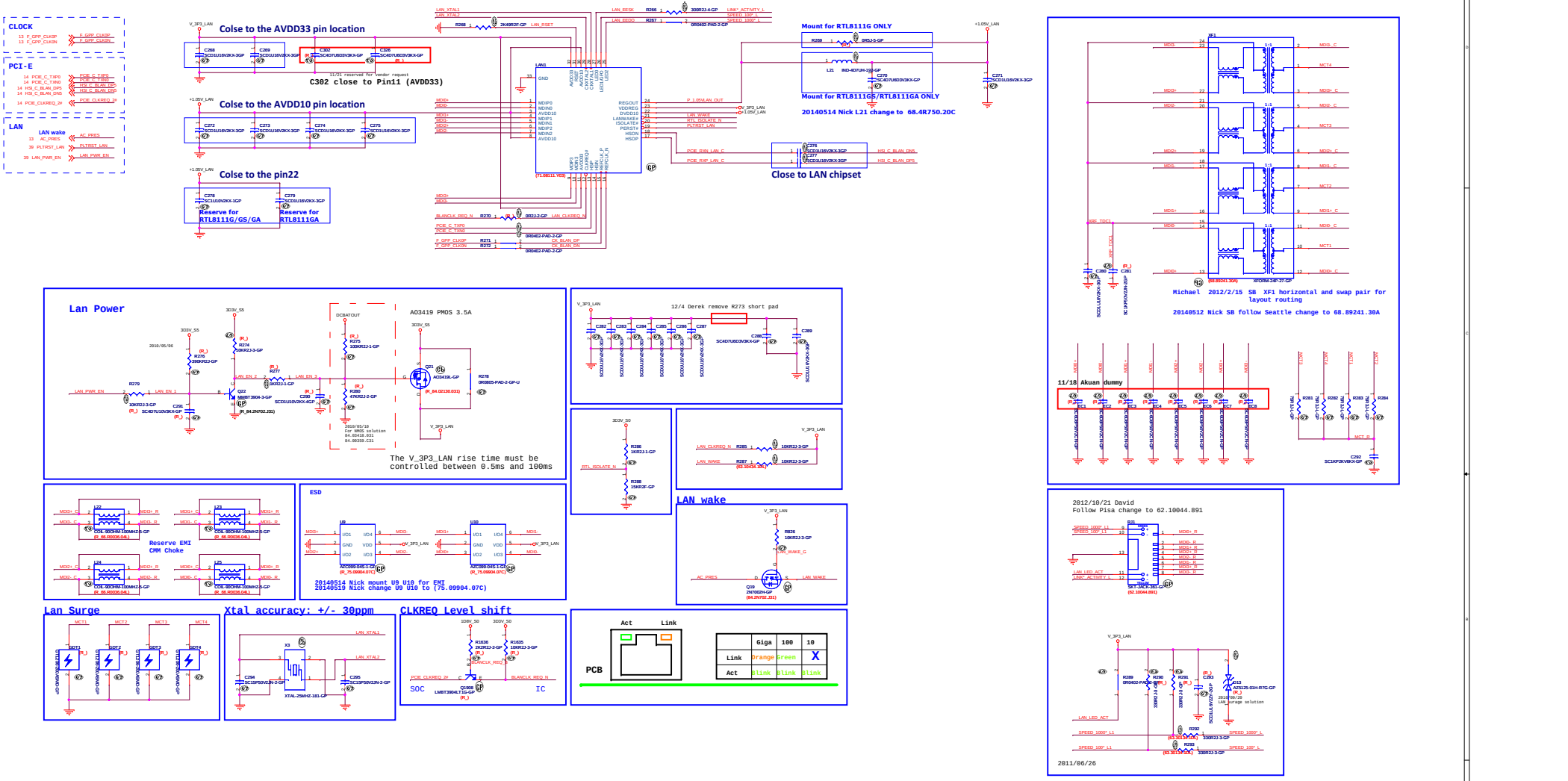
AUDIO CODEC-ALC269
Madrid Lite
Tuesday, July 22, 2014
Sheet 23 of 62


20130430 FOR LOT SWITCH_RYAN
Support iPhone ~ Mount R3018,R3020
unMount R3019,R3021
Support Nokia ~ Mount R3019,R3021
unMount R3018,R3020
HP Out Switch
L:Monitor H: PC
Vmin < Vin - 5.5V
Support negative voltage
Line Out Switch
PC_MONITOR_SW
SEL L:A1(MONITOR) H:A2(PC)
RESERVED ESD D3004
20101229
Vendor suggest
change from 4.7k to 2.2k
20121007 aPisa Charles
ALC269 Only MIC1 con use combo function
2012/6/29_ROME SA
Add Line out Function
MUTE
Follow Madrid
20131104 Kenyon
Follow Madrid delet
20140116 Daniel
20140108 Daniel follow Madrid -1A
for Mute function modify;
"SCLA_AMP_PDN" on SB change as
"SCLA_Audio_Mute"
DIGITAL ANALOG
H: mute
L: no-mute
MOAT
20140522 Nick change C258 to 78.47522.531
20140523 Nick C257,C269 change to 78.10421.2FL for merge cap
Control circuit
Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.
De-POP Circuit
Audio Mute Control
Audio Mute
AMP Mute
AMP PD# control
JD_LOT has Pull High to P3P3V
Scalar to EC
Control Amp PD# low
20140108 Daniel follow Madrid -1A
Mute function modify;
EC mute by A2_RST_N = HDA_RST#
Scalar mute by Pannel off control
11/28 Derek change the AGND of AMP1 from AGND to AmpGND follow Madrid
R1
R2
R3
R1||R2 = R3
R1,R2,R3 use 1%resister
to avoide "Pop" issue
Analog Moat
Digital Moat
11/15 Derek change R157
from 8R to 1A by vendor request
11/15 Derek change to AMPGND by vendor request
11/12 Derek Del C223
11/12 Derek Del C235
Close to AMP1 Pin9
Close to AMP1 Pin10
CM 10/16 Change to downsize bead
11/20 Derek change to AMPGND by vendor request
11/12 Derek Del C211
11/12 Derek Del C230
11/12 Derek Del C236
11/12 Derek Del C246
要拉到SCALAR
做POWER ON/OFF
CONTROL
Combo Audio Jack
20131027 Madrid SA Charles
modify
HP JD SEL
R236, C257 close to codec side
why need X load ?
HP Source SEL
20131023 Madrid SA Charles
delet L22,L23,C290,C291
ESD
11/20 Akuan add EC704
11/22 Derek change from AGND to 3GND for vendor request
12/11 Derek mount D9, D10, D11, D12 with 75.60120.07G
20140108 Daniel follow Madrid -1A
Add for Amp PD# pop
20121116
Mount
SHDN_MUTE_AP_CTL
When the PC mode and Monitor
mode are being switched
MUTE_AP_CTL should be low
in order to avoid the
noise
MUTE_AP_CTL also control when
select MUTE in the PC mode or
Monitor mode
MUTE_AP_CTL also control when
system wake from S3 to S0
Scalar Audio
Control
Enable Control
Low: Mute
High: no-MUTE
Audio Mute Control
20140108 Danielc follow Madrid -1A
Mute function modify;
AUDIO AMP
Wistron Incorporated
Madrid Lite


CLOCK
PCI-E
LAN
LAN wake
Colse to the AVDD33 pin location
C302 close to Pin11 (AVDD33)
Colse to the AVDD10 pin location
Colse to the pin22
Reserve for RTL8111G/GS/GA
Reserve for RTL8111GA
Mount for RTL8111G ONLY
Mount for RTL8111GS/RTL8111GA ONLY
20140514 Nick L21 change to 68.4R750.20C
Close to LAN chipset
Michael 2012/2/15 SB XF1 horizontal and swap pair for layout routing
20140512 Nick SB follow Seattle change to 68.89241.30A
11/18 Akuan dummy
Lan Power
AO3419 PMOS 3.5A
The V_3P3_LAN rise time must be controlled between 0.5ms and 100ms
12/4 Derek remove R273 short pad
LAN wake
ESD
20140514 Nick mount U9 U10 for EMI
20140519 Nick change U9 U10 to (75.09904.07C)
Reserve EMI CMM Choke
Lan Surge
Xtal accuracy: +/- 30ppm
CLKREQ Level shift
SOC
IC
PCB
Act
Link
Giga
100
10
Orange
Green
Blink
2012/10/21 David
Follow Pisa change to 62.10044.891
2011/06/26
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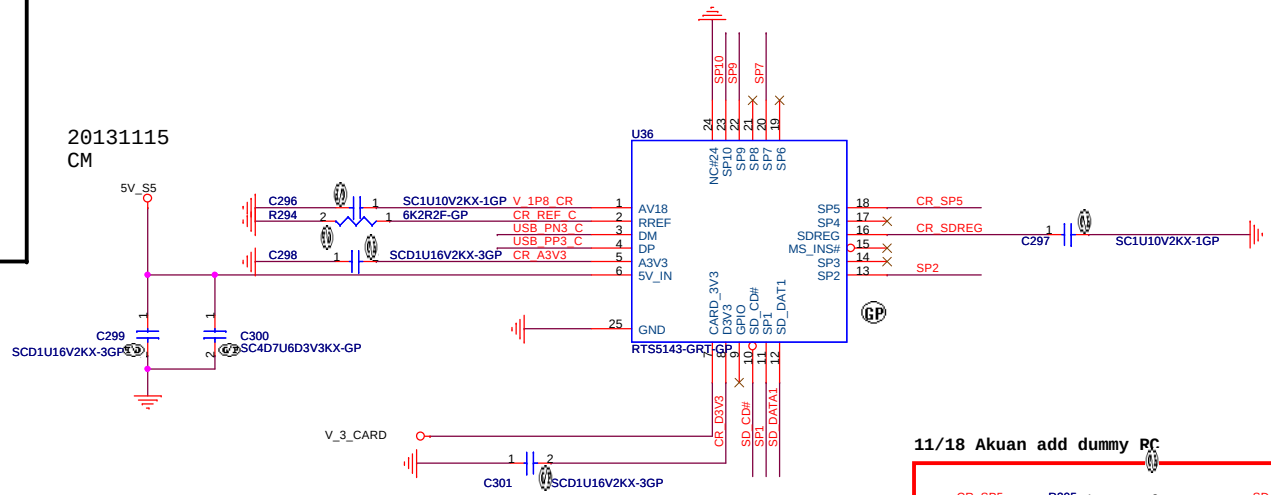
LAN-RTL8111GA
Madrid Lite
Thursday, July 24, 2014

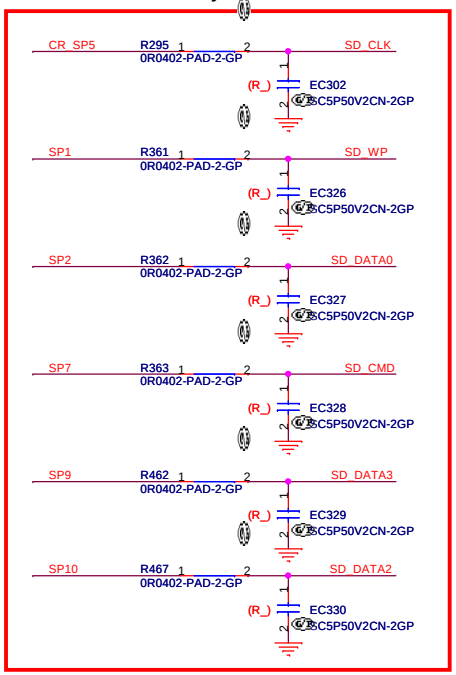
(SD only)

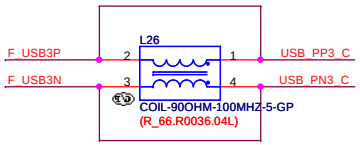
35 F_USB3P
35 F_USB3N

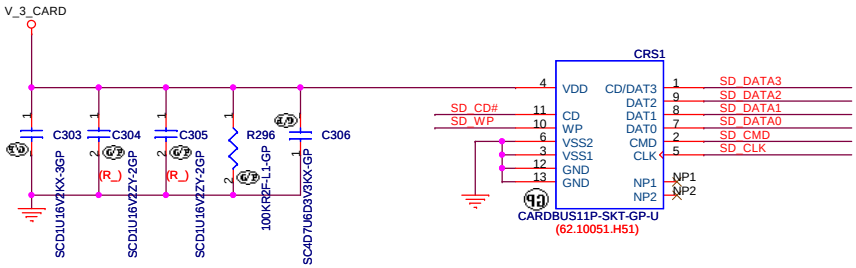
20131115
CM



11/18 Akuan add dummy RC







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Title: RTS5143 (CARD READER)

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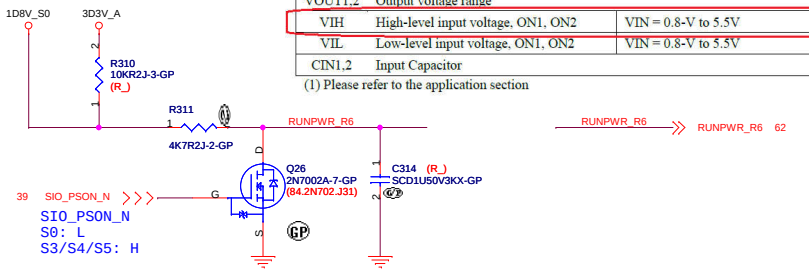
Date: Friday, July 25, 2014 | Sheet 26 of 62

ANNIE Run Power

			MIN	MAX	UNIT
VIN1,2	Input voltage range		0.8	5.5	V
VBIAS	Bias voltage range		4.75	5.25	V
VON1,2	ON voltage range		0	5.5	V
VOUT1,2	Output voltage range			VIN1,2	V
VIH	High-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V	1.05	5.5	V
VIL	Low-level input voltage, ON1, ON2	VIN = 0.8-V to 5.5V		0.6	V
CIN1,2	Input Capacitor		0.1 (1)		µF

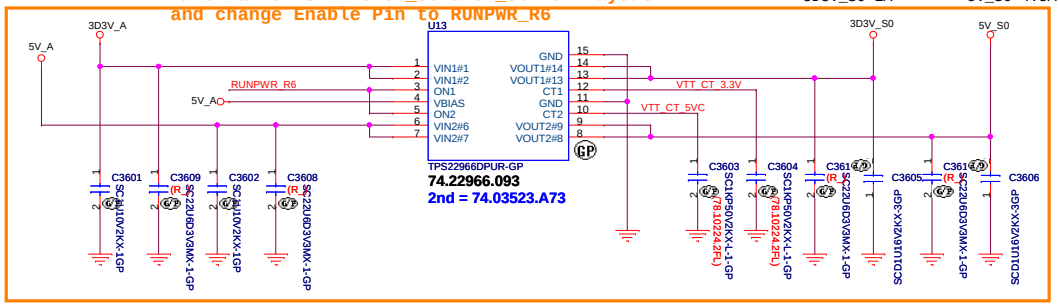
(1) Please refer to the application section

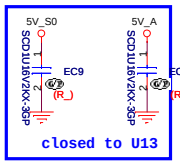


12/25 Derek
Delete U13/U15 power MOS
Add TPS22966 for 3V/5V_S0 power
1/14 Daniel Change EN pin from 12V_S0_PG
1/16 Daniel SWAP 3D3V_S0 & 5V_S0 for Layout and change Enable Pin to RUNPWR_R6

Dallas 3D3V_S0=2A

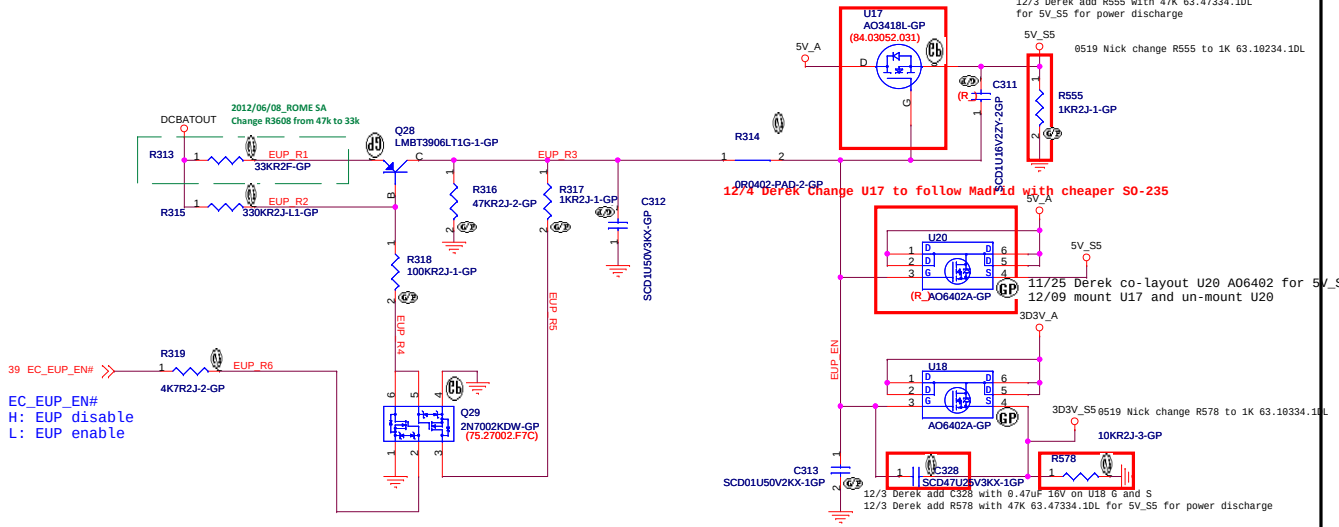
Dallas 5V_S0=4.5A





2012/10/19 David
change from 84.04468.A37(11.6A)
to 84.06402.B3D(7A)

EUP Power



2012/10/21 David
Removed PS_S3CNTRL

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Title: RUN POWER & SEQUENCE

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Date: Tuesday, July 22, 2014 | Sheet 27 of 62

AspireLink

TBD

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Title: AspireLink		
Size: A	Document Number: Madrid Lite	Rev: 1A
Date: Wednesday, June 18, 2014	Sheet 28 of 62	

SSID = VIDEO

Modified by Kenyon. Use CMC to choose signal source. 2012/11/07

2012/10/15 David
Reserved for EMI
Closed to LVDS1

2012/10/15 David
Down size to 1210
Symbol: 68.01210.20G(higher)
0 ohm: 66.R0036.04L
EMI: Murata 68.00396.001

Change to suitable type
20131023 Kenyon
20131113 Derek delete L27~L39

For UMA
Low: Disable
High: Enable

For Scalar
Low: Enable
High: Disable

2012/12/26 David
add for EC to do
panel control

2013/12/3 Derek
Delete Q31/R370/R371
without ECIO BL_EN

11/13 20mils for sense

12/25 Derek delete CNVBD1

12/2 Derek change F1 from 69.50013.001 to 69.50007.A31

2012/10/5 David
change to polysw

01/14 Daniel change U59 symbel to 74.00554.073

CNVBD1 Co-Layout with CNVBD2

40mils

20mils

EC LCD ID GPIO

12/2 Derek link to ECIO with ECIO GPI power

11/26 Derek Change U59 net name from AGND to LEDGND

11/27 Jimmy change to 32 25V

Roger modify 2013/2/4

20140116 EMI ISSUE Daniel mont 1000P

19V boost to 50V

12/4 Derek Change L27 to P/N 68.33010.20J ; Q78 to P/N 84.04468.A37 with smaller size

1st source: 83.3R010.08M
2rd source: 83.3R010.A8M

12/13 Derek change Q78 to 084.PA010.0037

LVDS1 from 20.K0792.030 change to 20.K0631.030 ---
1/31'13 Jerry Feng(Pisa):插入排線后推桿很難閉合到位

20.K0792.030

20.K0631.030

20140522 Nick change R377 to 499ohm

High: Enable
Low: Disable

11/27 Jimmy update Cable Spec

Panel Model	Cable Spec			
	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF5-TLF1	0	0	1	3,4 Vout 1,6 RTN 2,5 N.C
LG LM230WF3-SLL1	0	1	0	3,4 Vout 1,6 RTN 2,5 N.C
CMI M195FGE-L23 C1	1	0	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C3	1	1	0	1,2,5,6 Vout 3,4 RTN
CMI M195FGE-L20 C1	1	1	1	1,2,5,6 Vout 3,4 RTN

LCD ID

CONVERTOR SMB

LVDS For Scalar

LVDS For eDP translator

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Title: LCD CONN/CVR

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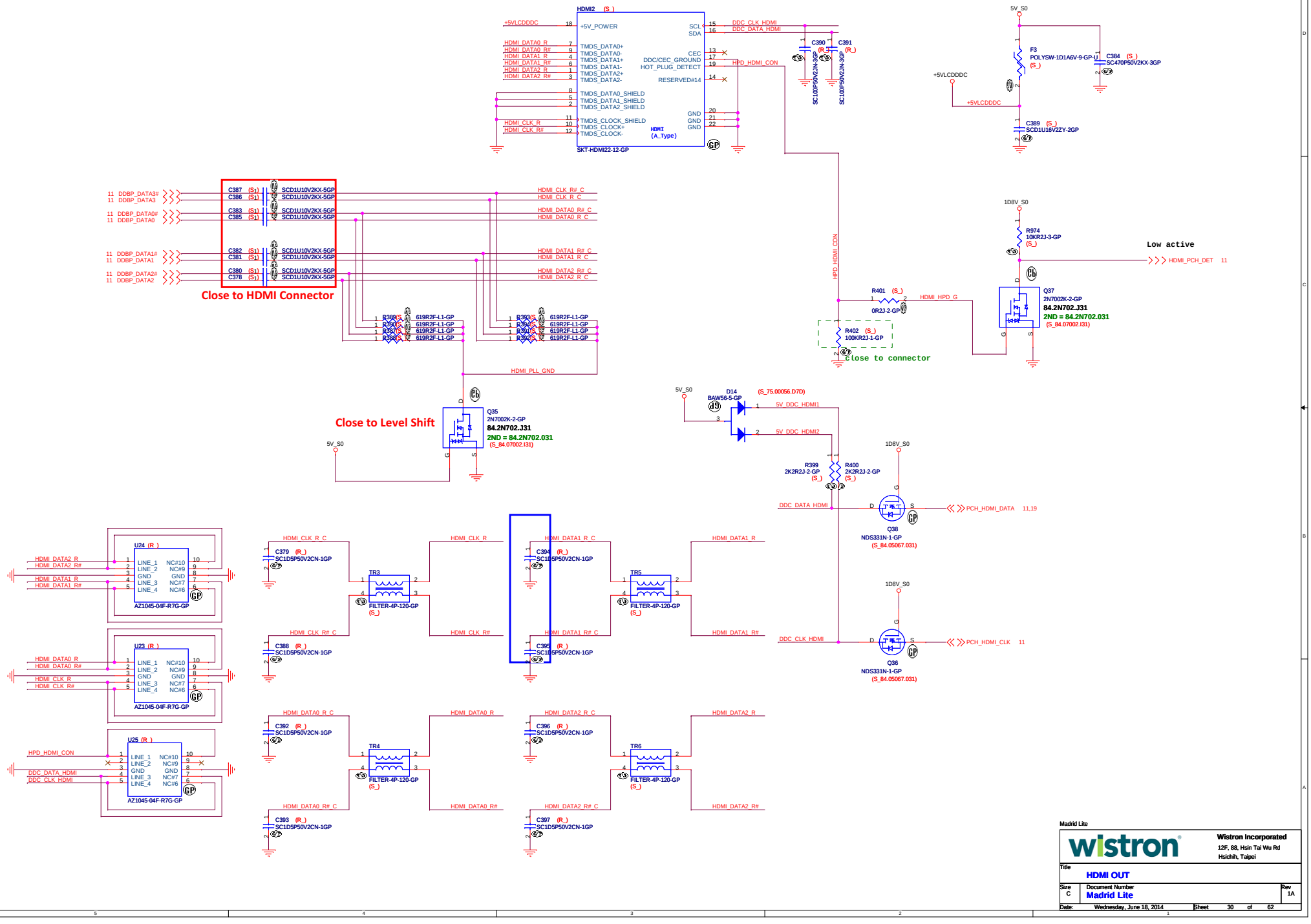
Date: Tuesday, July 22, 2014 | Sheet 29 of 62

HDMI Level Shifter & CONNECTOR



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Title: HDMI OUT

Size	Document Number	Rev
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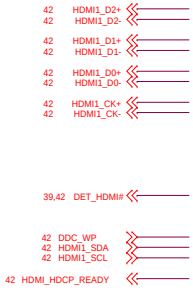
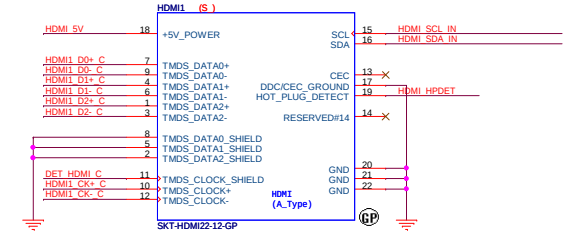
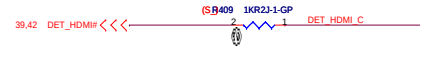
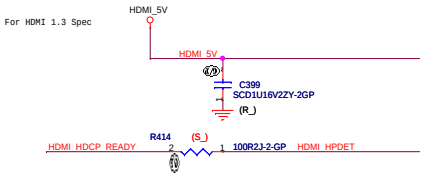
Date: Wednesday, June 18, 2014 Sheet 30 of 62

HDMI-IN



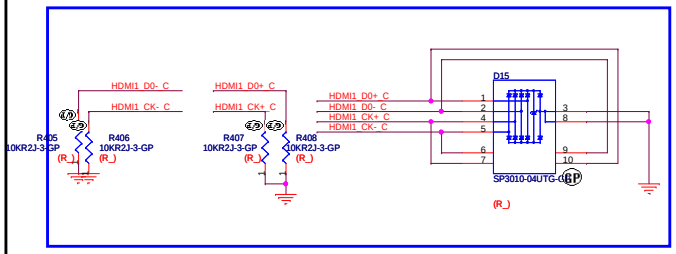


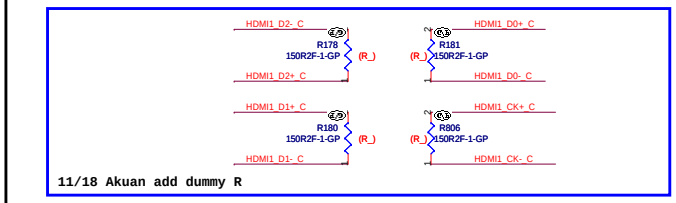




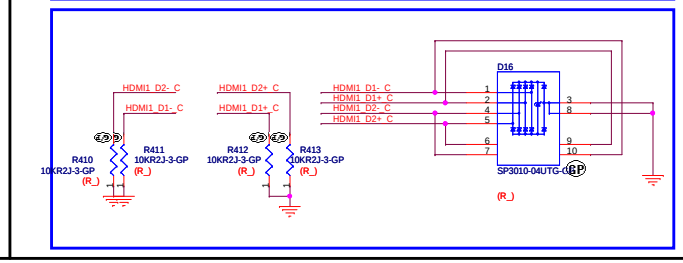
7/2 Richard
Del the resistor for NV suggestion.

EMI/ESD near Connector



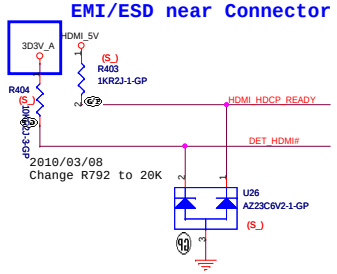


11/18 Akuan add dummy R

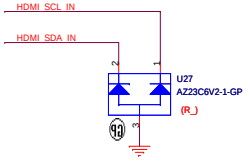


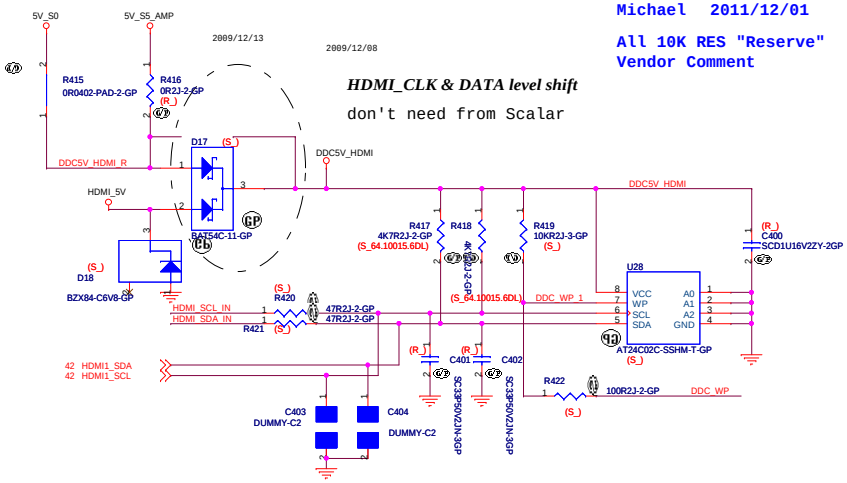
change the 3D3V_S5 to 3D3V_A

EMI/ESD near Connector



2010/03/08
Change R792 to 20K





HDMI_CLK & DATA level shift

don't need from Scalar

Michael 2011/12/01

All 10K RES "Reserve"
Vendor Comment

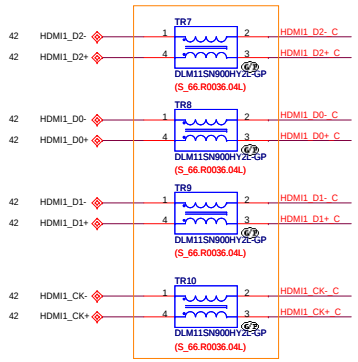
Michael 2011/12/01

change R283 and R305 from 100ohm to 47ohm

Vendor Comment

Michael 2011/12/02

Add 0ohm and unmount
Common mode chloke



Change to suitable type
20131023 Kenyon

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Title: HDMI IN

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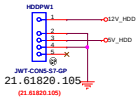
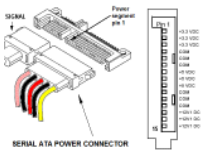
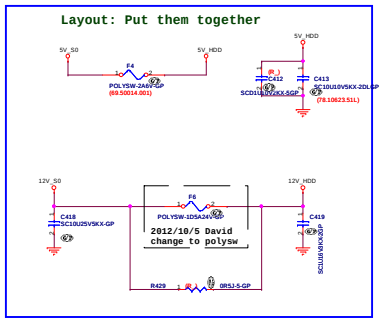
SSID = SATA

SATA HDD Connector

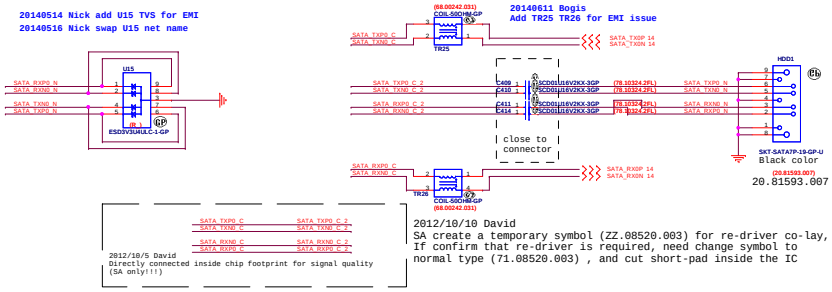




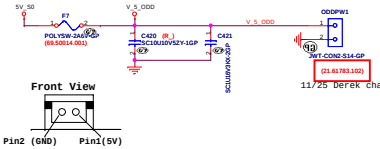


20140514 Nick add U15 TVS for EMI
20140516 Nick swap U15 net name

20140611 Bogis
Add TR25 TR26 for EMI issue



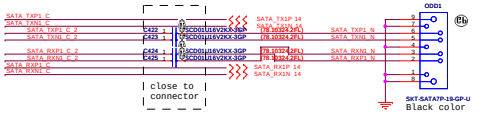
2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC



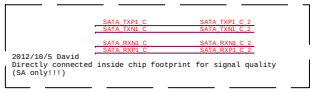
11/25 Derek changes to 21.61783.102

2012/10/23 David
change to PS8520 for SATA gen3

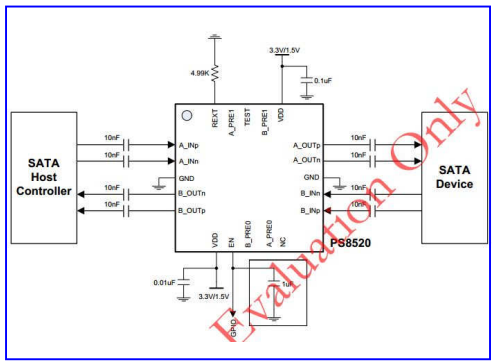
2013/05/21 David
Deleted SATA re-driver since
test PASS and to fix P/R issue

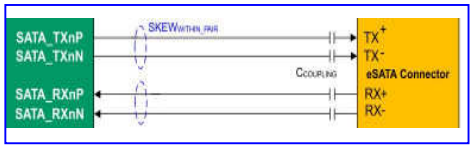


2012/10/24 David
EN pin and TEST pin can be floating for normal working.
Pin20 (REXT) should be connect to 4.99K ohm to GND



2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
If confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC





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Hsichih, Taipei

File: HDD/ODD

Size	Document Number	Rev
D	Madrid Lite	1A

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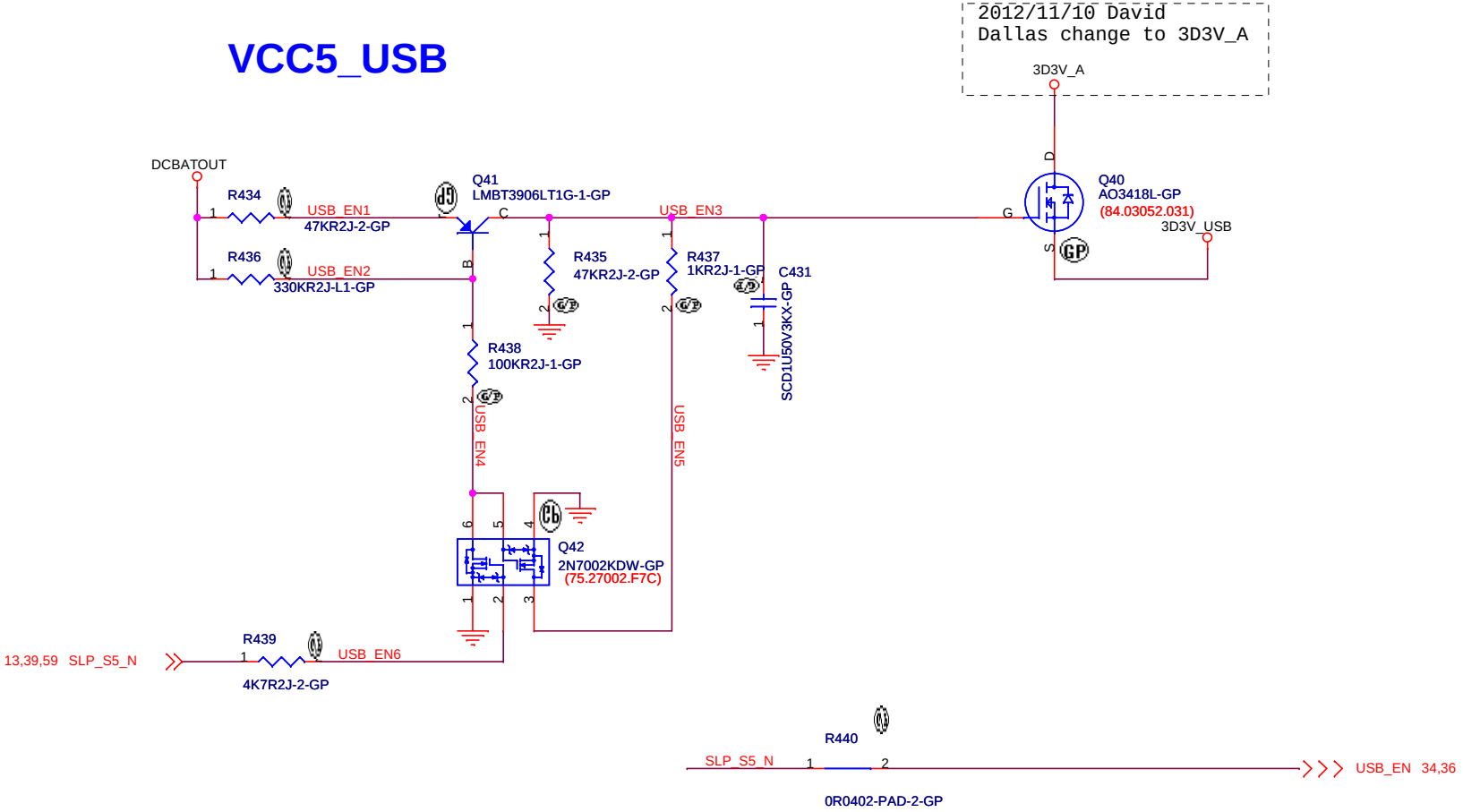
SSID = USB

VCC5_USB

2012/11/10 David
Dallas change to 3D3V_A



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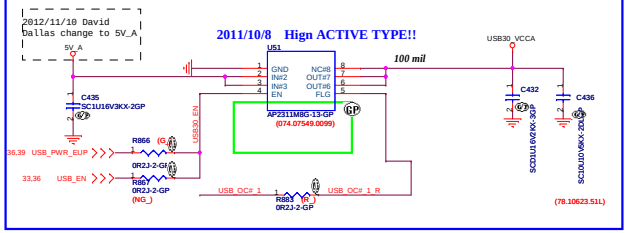
Title: USB 2.0 Power SW		
Size: Custom	Document Number: Madrid Lite	Rev: 1A
Date: Tuesday, July 22, 2014	Sheet 33 of 62	

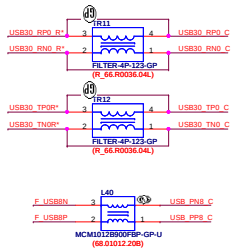
20140508 Nick change F7 to 074.07549.0099

2012/11/10 David
Ballas change to 5V_A

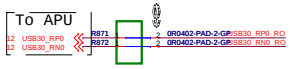
2011/10/8 Hign ACTIVE TYPE!!



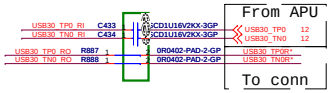
0ohm: 66.R0036.04L



To APU



From APU

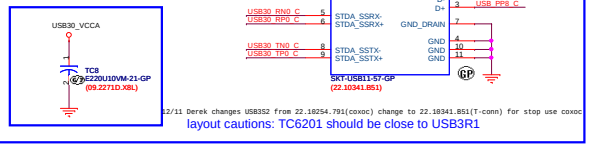


To conn

2012/07/12
If use NXP
R126,R136= 0ohm
R81=NC

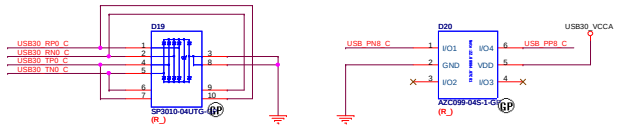
If use TI
R126,R136,R81= 0ohm

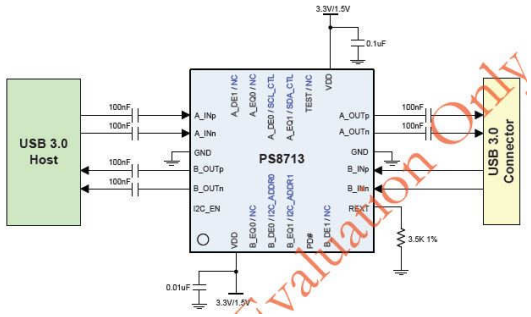
2012/10/5 David
Directly connected inside chip footprint for signal quality
(SA only!!)



12/11 Derek changes USB3S2 from 22.10254.791(coxoc) change to 22.10341.851(T-conn) for stop use coxoc

layout cautions: TC6201 should be close to USB3R1





Evaluation Only

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

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Hsichih, Taipei

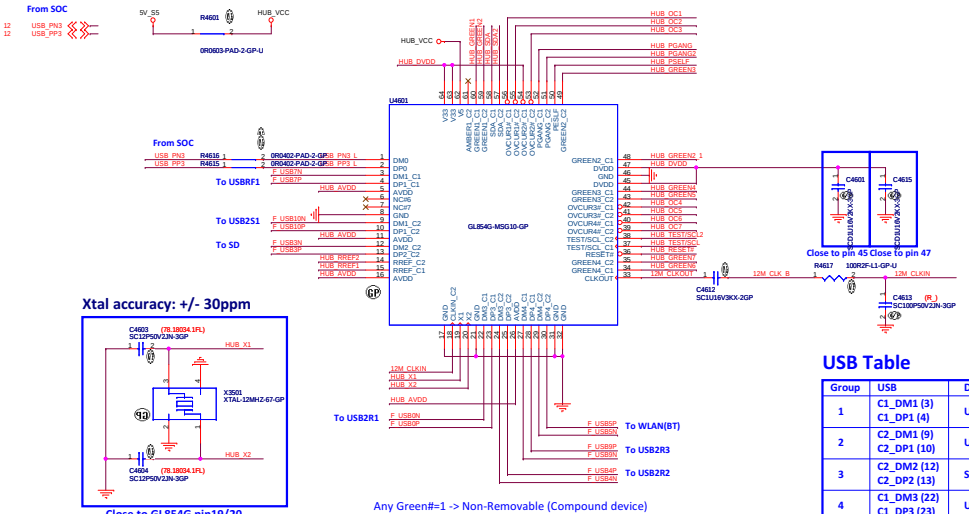
Title: USB 3.0 Port

Size: Custom | Document Number: Madrid Lite | Rev: 1A

Date: Friday, July 25, 2014 | Sheet 34 of 62

GL850G
Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
Set USB port to be internal (non-removable): set OC pin is floating
Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

GL852G
Enable/Disable USB output port: setting by EEPROM
Set USB port to be internal (non-removable) or external (removable): setting by EEPROM



Xtal accuracy: +/- 30ppm

Close to GL854G pin19/20

1st: 82.30006.641
2nd: 82.30006.501

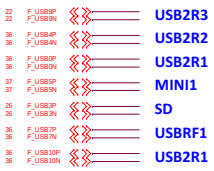
Any Green#=1 -> Non-Removable (Compound device)

	PGreen1	PGreen2	PGreen3	PGreen4	PGreen5	PGreen6	PGreen7
Non-Removable	X	1	1	1	1	1	1

Note -- x : Not support
1 : Pull up 15K to DVDD
PGreen2 & PGreen3 do not set to 1 concurrently

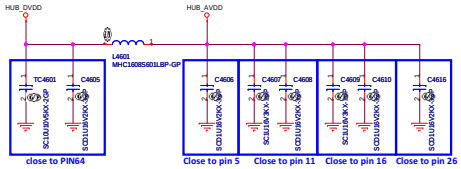
USB Table

Group	USB	Device	
1	C1_DM1 (3) C1_DP1 (4)	USBRF1	external
2	C2_DM1 (9) C2_DP1 (10)	USB2S1	external
3	C2_DM2 (12) C2_DP2 (13)	SD	internal
4	C1_DM3 (22) C1_DP3 (23)	USB2R1	external
5	C2_DM3 (24) C2_DP3 (25)	USB2R2	external
6	C1_DM4 (27) C1_DP4 (28)	USB2R3	external
7	C2_DM4 (29) C2_DP4 (30)	MINI1	internal

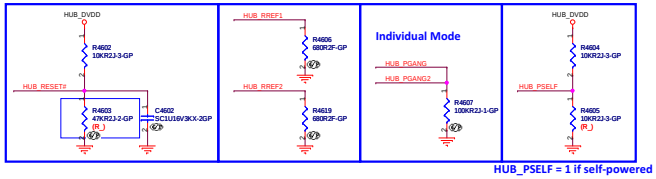


Internal Power

(Hub Internal VR output from pin 63/64 V33 = HUB_DVDD)



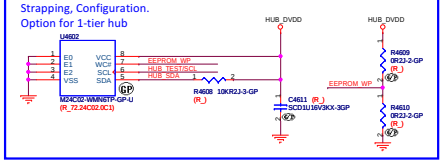
Fine tune resistor value for USB driving
590ohm: 64.59005.6DL



HUB_PSELF = 1 if self-powered
HUB_PSELF = 0 if bus-powered

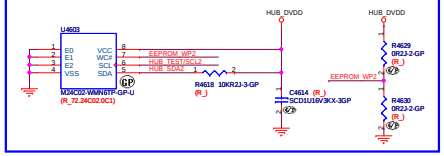
EEPROM

Option:
24C02 for VID, PID,
Strapping, Configuration.
Option for 1-tier hub

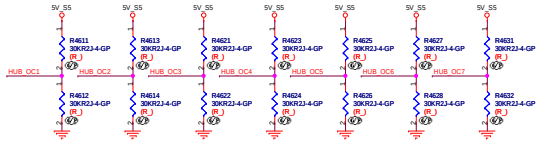


EEPROM

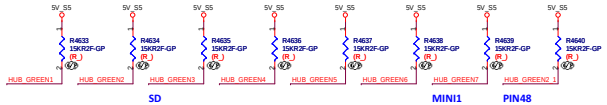
Option for 2-tier hub



Over Current



Green LED



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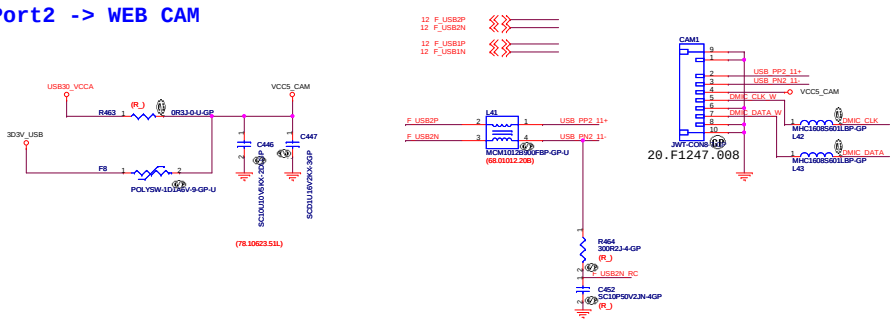
wistron Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

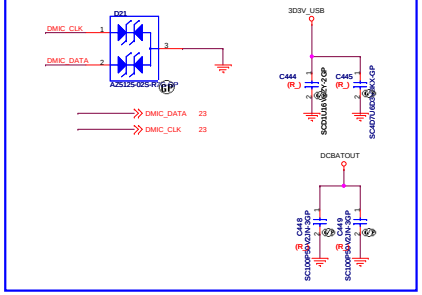
Title: USB HUB IC
Size: Custom | Document Number: Madrid Lite | Rev: 1A
Date: Tuesday, July 22, 2014 | Sheet 35 of 62

SSID =USB2.0

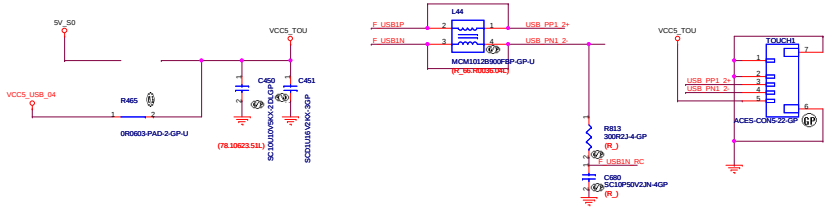
USB Port2 -> WEB CAM



DMIC Connector



USB Port 1 -> TOUCH

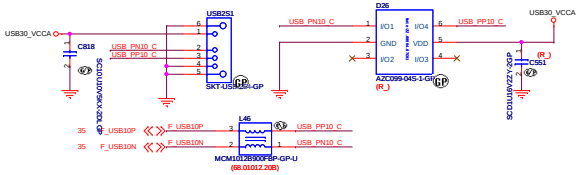


Mas touch Connector Pin Define

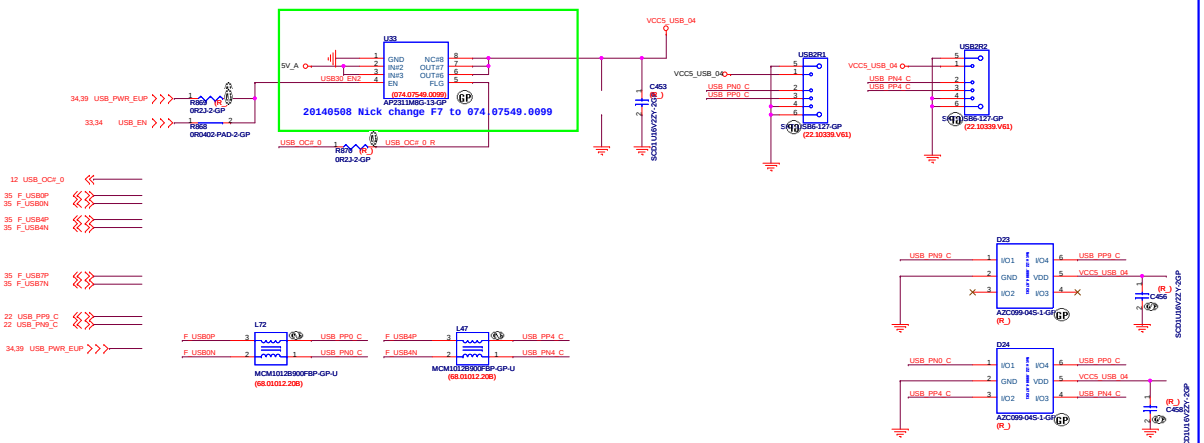
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

TPK touch Connector Pin Define

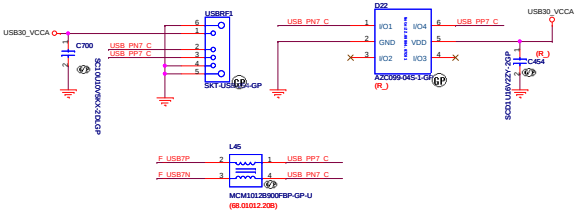
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield



USB Port 0,1,4-> REAR I/O



USB Port 7-> RF KB Dongle



Madrid Lite

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

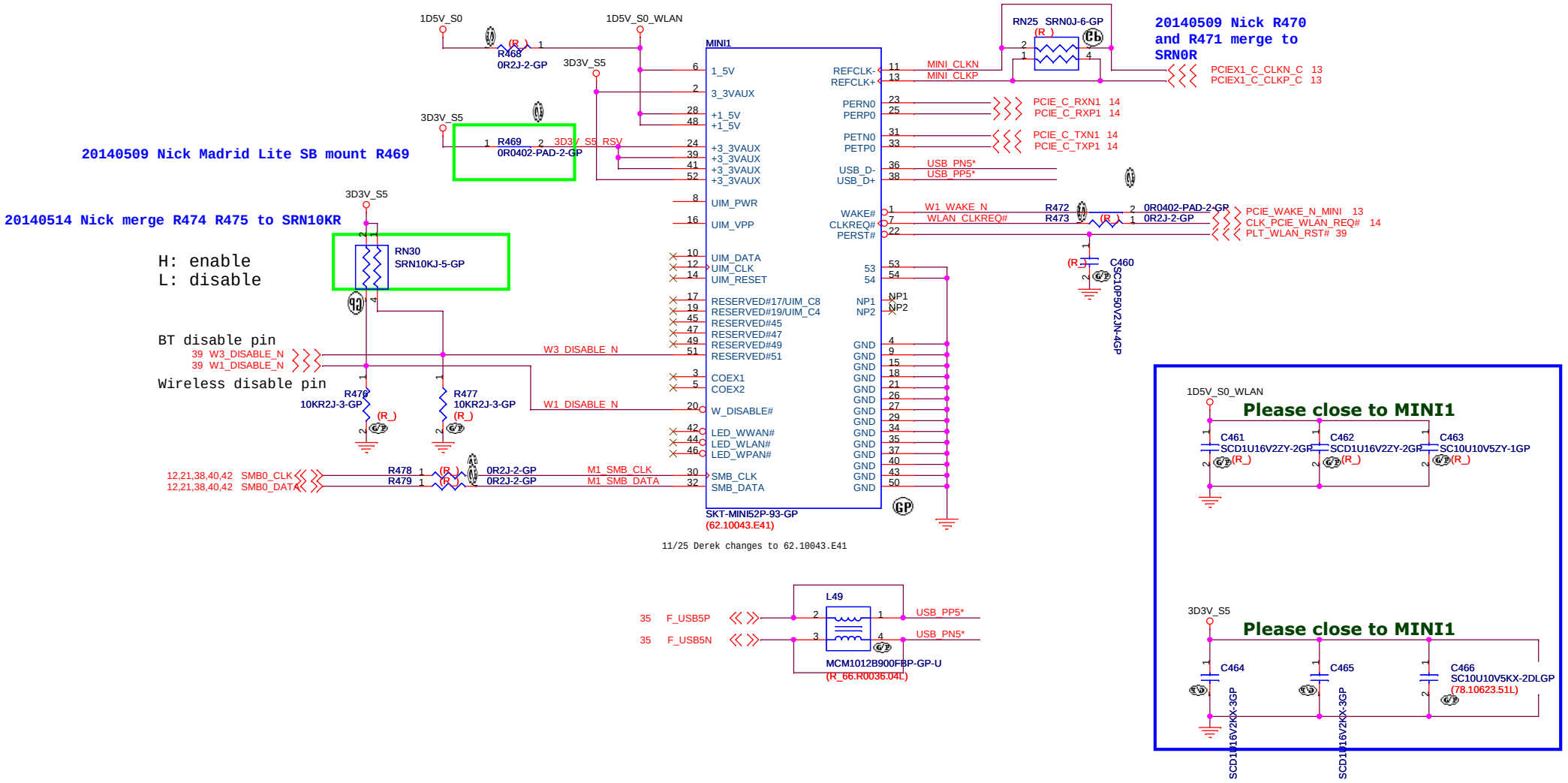
Title: REAR USB / TOU / WEBCAM

Size	Document Number	Rev
Custom	Madrid Lite	1A

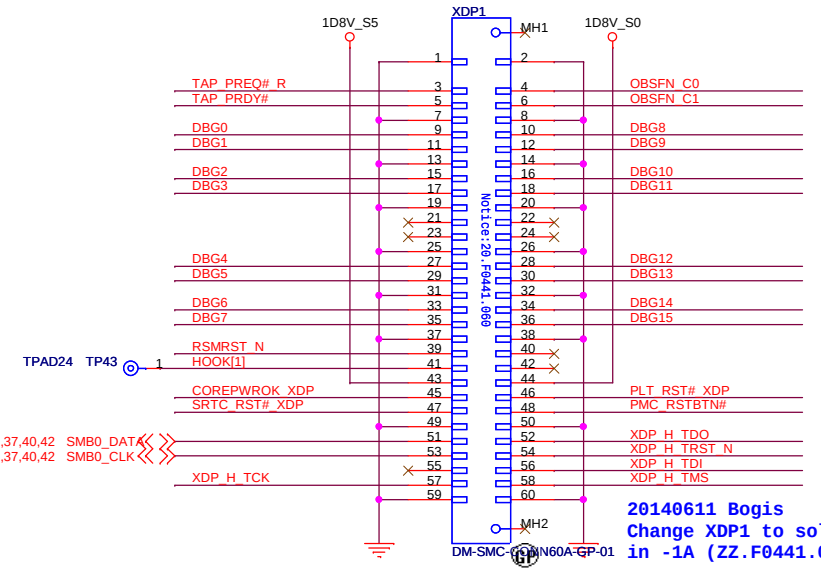
Date: Friday, July 25, 2014 Sheet 36 of 62

SSID = Wireless and Bluetooth

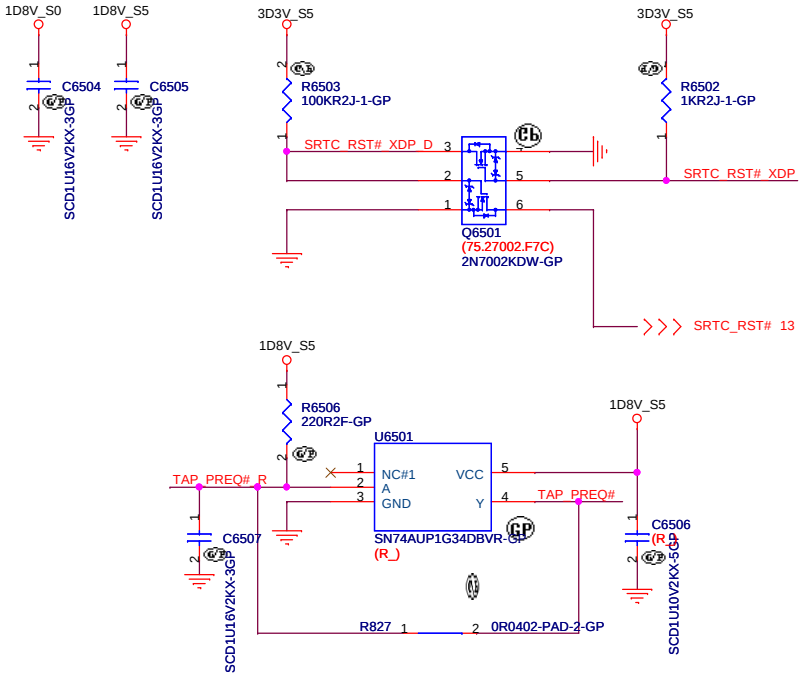
Mini Card Connector(Wireless LAN+BT)

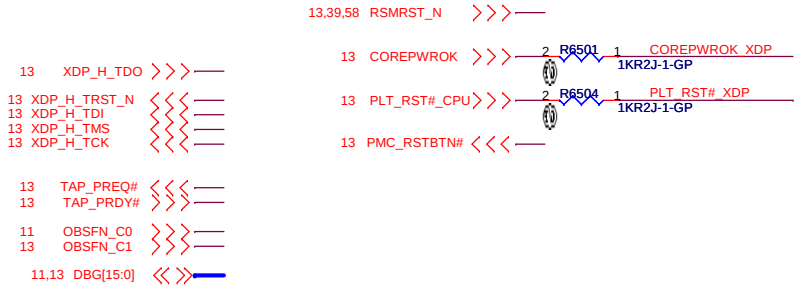


Wistron Incorporated	12F, 88, Hsin Tai Wu Rd, Hsichih, Taipei
Title	MINI PCIE CARD (WLAN/BT)
Size: Custom	Document Number: Madrid Lite
Rev	1A
Date: Friday, July 25, 2014	Sheet 37 of 62



20140611 Bogis
Change XDP1 to solder mask P/N in -1A (ZZ.F0441.06001)





Madrid Lite

wistron

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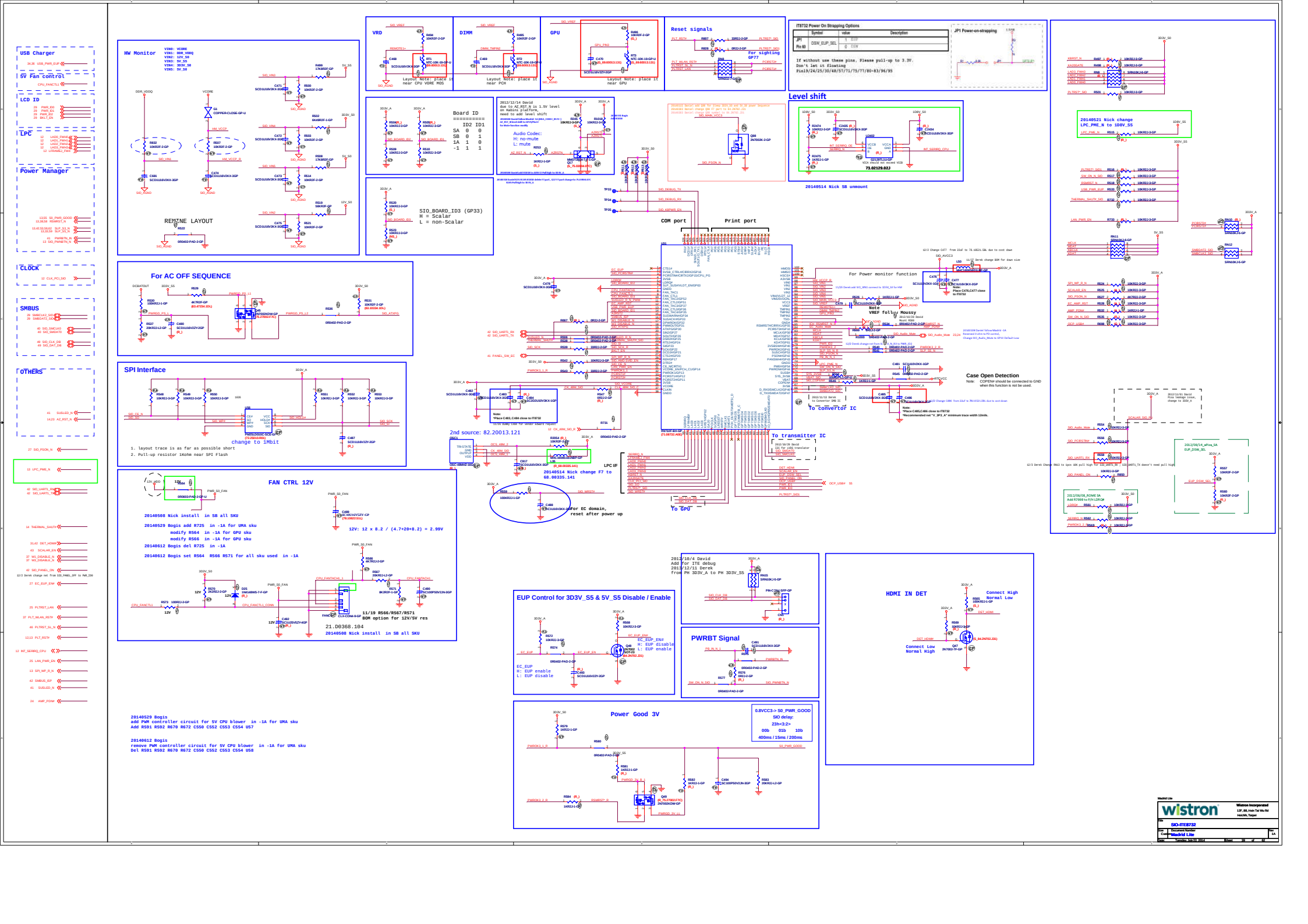
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: XDP

Size	Document Number	Rev
B	Madrid Lite	1A

Date: Tuesday, July 22, 2014 Sheet 38 of 62


USB Charger
5V Fan control
LCD ID
LPC
Power Manager
CLOCK
SMBUS
OTHERS
HW Monitor
REMINE LAYOUT
VRD
DIMM
GPU
Reset signals
Board ID
Audio Code:
H: no-mute
L: mute
SIO_BOARD_ID3 (GP33)
H = Scalar
L = non-Scalar
Level shift
20140514 Nick SB unmount
20140521 Nick change
LPC_PME_N to 1D8V_S5
For AC OFF SEQUENCE
SPI Interface
change to 1Mbit
1. layout trace is as far as possible short
2. Pull-up resistor 1kohm near SPI Flash
FAN CTRL 12V
20140508 Nick install in SB all SKU
20140529 Bogis add R725 in -1A for UMA sku
modify R564 in -1A for GPU sku
modify R566 in -1A for GPU sku
20140612 Bogis del R725 in -1A
20140612 Bogis set R564 R566 R571 for all sku used in -1A
12V: 12 x 8.2 / (4.7+20+8.2) = 2.99V
11/19 R566/R567/R571
BOM option for 12V/5V res
21.D0368.104
20140508 Nick install in SB all SKU
20140529 Bogis
add PWM controller circuit for 5V CPU blower in -1A for UMA sku
Add R591 R592 R670 R672 C550 C552 C553 C554 U57
20140612 Bogis
remove PWM controller circuit for 5V CPU blower in -1A for UMA sku
Del R591 R592 R670 R672 C550 C552 C553 C554 U58
COM port
Print port
To convertor IC
To transmitter IC
To CPU
2nd source: 82.20013.121
20140514 Nick change F7 to 68.00335.141
For EC domain, reset after power up
LPC I/F
Case Open Detection
EUP Control for 3D3V_S5 & 5V_S5 Disable / Enable
PWRBT Signal
HDMI IN DET
Power Good 3V
0.8VCC3-> S0_PWR_GOOD
SIO delay:
23h<3:2>
00b 01b 10b
400ms / 15ms / 200ms
Wistron Incorporated
SIO-ITE8732
Madrid Lite

20140514 Nick change F7 to 68.00335.181

Closed to RTD2136 pin 5

Closed to RTD2136 pin 22

Closed to RTD2136 pin 18

Closed to RTD2136 pin 15

Closed to RTD2136 pin 11

Closed to RTD2136 pin 43

20140509 Nick RS91 and R592 merge to SRN4.7K

20140514 Nick RN7 change to 66.10336.04L

2012/10/14 David reserved slave address 0x94 & 0x6A

SMBUS

From APU

From EC

2012/10/24 David Reserve the EEPROM (72.24C64.E01) for SA usage. Once the panel is work normally, can remove EEPROM, and transfer the initial job to EC

2013/04/24 David if external EEPROM no use (use EC or BIOS), un-mount R655/R645, mount R899/R646

MODE_CFG0(PIN48)	MODE_CFG1(PIN47)	0	1
	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

RTD2136 Supports three operation mode for system design. Reserved 4.7K resistor pull up/low for mode selection

ROM ONLY Mode : PIN47 4.7K pull low, PIN48 4.7K pull high
EP Mode : PIN47 4.7K pull high, PIN48 4.7K pull low
EEPROM Mode : PIN47 4.7K pull high, PIN48 4.7K pull high

APU HPD:
L: un-plugged
H: plugged

High active

12/11 Derek change from PH 3D3V_A to PH 3D3V_S5

EEPROM Mode

In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

I2C address=0xA8

EP Mode

External device connect to DP2LVDS by PIn13/Pin14, I2C protocol is used

EC

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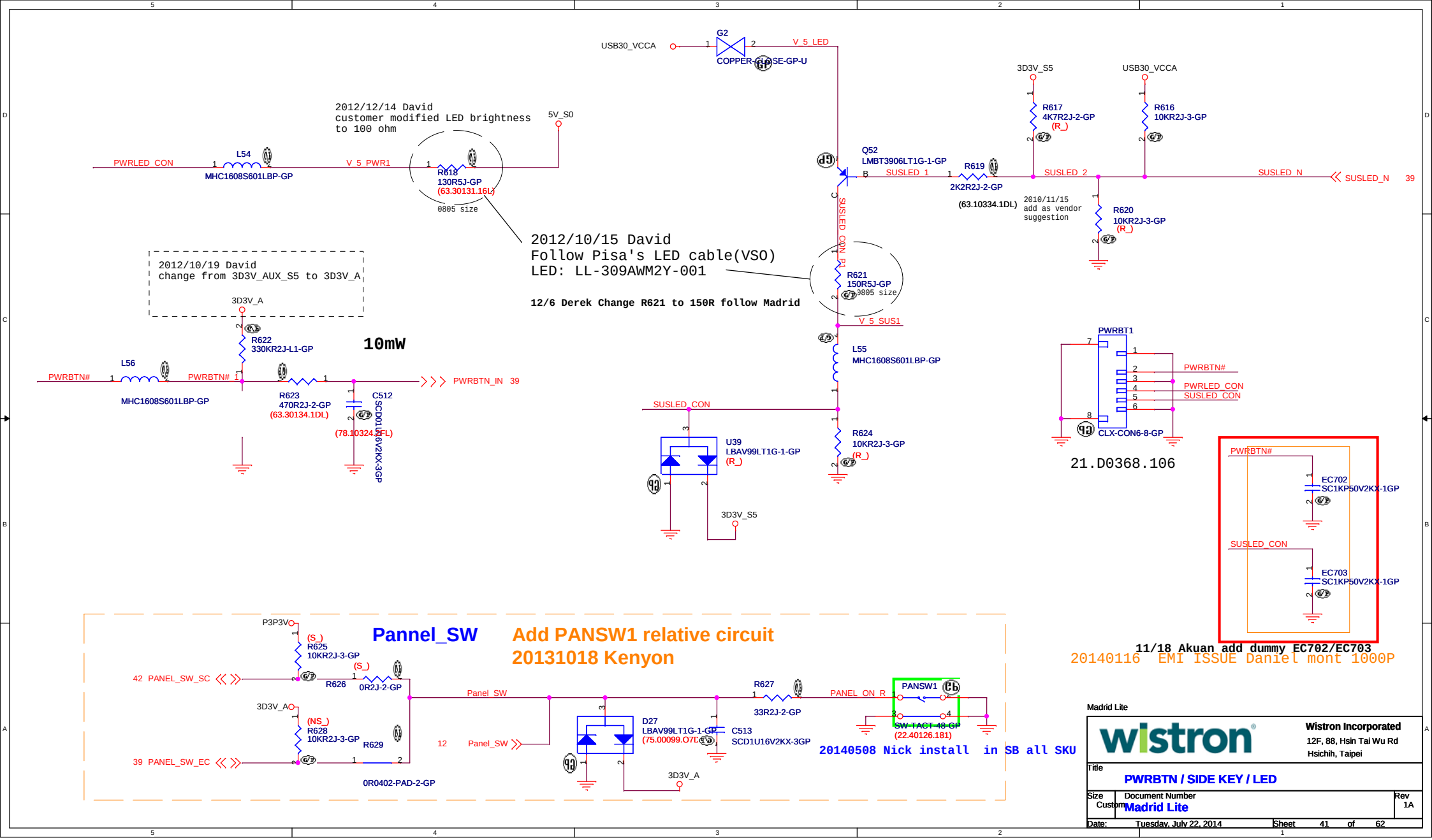
Hsichih, Taipei

Title: RTD2136 eDP to LVDS

Size: Custom | Document Number: Madrid Lite | Rev: 1A

Date: Tuesday, July 22, 2014 | Sheet 40 of 62


USB30_VCCA
G2
COPPER-BASE-GP-U
V_5_LED
3D3V_S5
USB30_VCCA
R617
4K7R2J-2-GP
(R_)
R616
10KR2J-3-GP
2012/12/14 David
customer modified LED brightness
to 100 ohm
5V_S0
PWRLED_CON
L54
MHC1608S601LBP-GP
V_5_PWR1
R618
130R5J-GP
(63.30131.16L)
0805 size
Q52
LMBT3906LT1G-1-GP
B
SUSLED_1
R619
2K2R2J-2-GP
(63.10334.1DL)
2010/11/15
add as vendor
suggestion
SUSLED_2
SUSLED_N
SUSLED_N 39
R620
10KR2J-3-GP
(R_)
2012/10/15 David
Follow Pisa's LED cable(VS0)
LED: LL-309AWM2Y-001
12/6 Derek Change R621 to 150R follow Madrid
SUSLED_CON_P1
R621
150R5J-GP
0805 size
2012/10/19 David
change from 3D3V_AUX_S5 to 3D3V_A
3D3V_A
10mW
R622
330KR2J-L1-GP
L56
PWRBTN#
PWRBTN# 1
MHC1608S601LBP-GP
R623
470R2J-2-GP
(63.30134.1DL)
C512
SCD01U16V2KX-3GP
(78.10324.5FL)
PWRBTN_IN 39
V_5_SUS1
L55
MHC1608S601LBP-GP
SUSLED_CON
U39
LBAV99LT1G-1-GP
(R_)
3D3V_S5
R624
10KR2J-3-GP
(R_)
PWRBT1
PWRBTN#
PWRLED_CON
SUSLED_CON
CLX-CON6-8-GP
21.D0368.106
PWRBTN#
EC702
SC1KP50V2KX-1GP
SUSLED_CON
EC703
SC1KP50V2KX-1GP
11/18 Akuan add dummy EC702/EC703
20140116 EMI ISSUE Daniel mont 1000P
Pannel_SW
Add PANSW1 relative circuit
20131018 Kenyon
P3P3V
R625
10KR2J-3-GP
(S_)
42 PANEL_SW_SC
R626
0R2J-2-GP
(S_)
3D3V_A
R628
10KR2J-3-GP
(NS_)
R629
39 PANEL_SW_EC
0R0402-PAD-2-GP
Panel_SW
12 Panel_SW
D27
LBAV99LT1G-1-GP
(75.00099.07D)
C513
SCD1U16V2KX-3GP
3D3V_A
R627
33R2J-2-GP
PANEL_ON_R
PANSW1
SW-TACT-48-GP
(22.40126.181)
20140508 Nick install in SB all SKU
Madrid Lite
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
PWRBTN / SIDE KEY / LED
Size
Custom
Document Number
Madrid Lite
Rev
1A
Date: Tuesday, July 22, 2014
Sheet 41 of 62

SSID = Scalar

Audio Out

LVDS-OUT

DHMI-IN

CONRTOL

DVI-IN

OSD

Panel On Off CTRL

PC_MONITOR_SW

According to the IR decode or side key value to switch the satus of monitor mode and PC mode

BEAD 要30ohm@100MHz(1A)

如果有使用OD，建議在這邊放10uF(MLCC)

Main EEPROM

Need Check

Shielding

Michael 2012/2/6

EEPROM for OSD

72.24C16.S01, ST
72.24C16.U01, ATMEL

Michael 2011/11/30
Remove EEPROM for OSD from GPU

LCD ON/OFF

Michael 2011/12/02
Need check the Panel power later

Pin55

Pin 118
PW ON Latch功能選項:
Internal MCU :Pull High
External MCU :Pull Low

B-EVEN

A-ODD

Michael 2012/4/11 -1

2013/03/19 David
change to cap for
scalar HP-Out voltage level

11/6 Delete unconnected net

SB add

Colay with RTD2136

Michael 2012/2/15
change EDID_RDY connction
from pin35 to pin41

To Line Out

To AMP

Vef power

Michael 2011/12/28
Pull down to 10 for depop when AC ON

2012/10/4 David
Follow Pisa 0920, removed MODE_SEL

Monitor mode			
Monitor	DET_HDMI#	SCALAR_EN	Panel EN/PWM/CTRL
	0	1	Active

DET_HDMI# : connect to SIO and Scalar

To SIO: make scalar workable -> Scalar_EN 1(From SIO)

To Scalar: Let scalar know HDMI IN, and make related signal active, Panel and AMP

2012/10/4 David
Follow Pisa SB

from EC

To APU GPIO

from scalar

Xtal accuracy: +/- 20ppm

HDMI side:
HDMI0 => RX2 pair
HDMI1 => RX1 pair
HDMI2 => RX0 pair
HDMICK => RC pair

2012/10/14 David
Connect to AMD DP1
through eDP I/F

Colay with RTD2136
Change DP1_TX[N] to DP0_TX[N]
20111021 Kenyon

PC mode: PWM_SW_EN -> H
Monitor: PWM_SW_EN -> L

for leakage

11/18 Derek add R830 for RTD2136R vendor Peter request

Colay with RTD2136
Change DP1_HPD_N to DP0_HPD_N
20131021 Kenyon

Firmware update by SMBUS

2013/05/28 David
reserved for ISP tool use SMBUS8

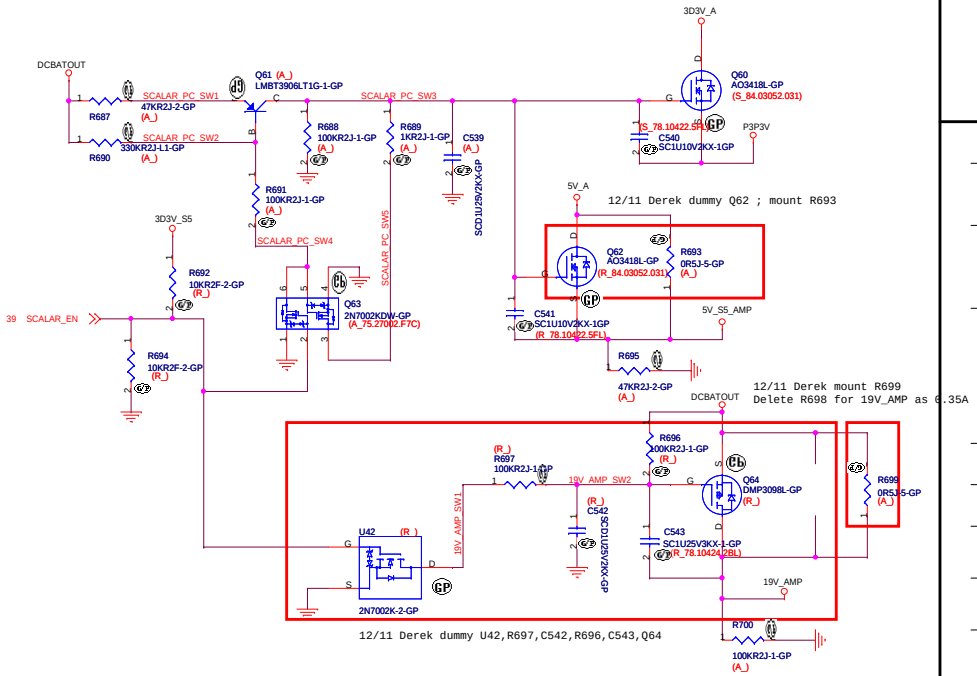
SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode

Panel ID Selectiong

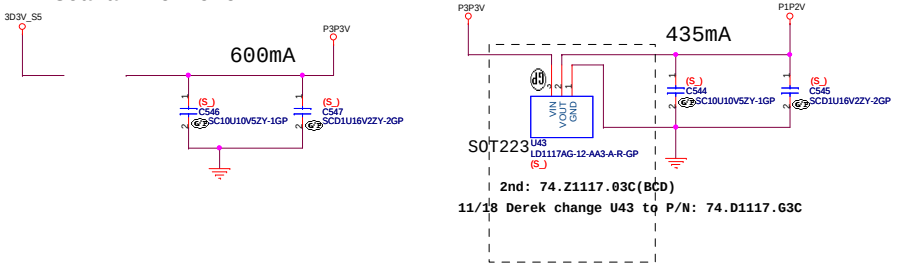
Madrid Lite	
Wistron Incorporated	13F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	SCALAR-RTD2486
Size	Document Number
Custom	Madrid Lite
Rev	1A
Date	Tuesday, July 09, 2013
Sheet	49 of 58

SSID = SDIO

AO3418 NMOS 3.1A, 60mohm,Vgs=10V
NMOS H: Enable L:Disable
3.1A 60 mohm(10V)
(Vds 30V,Vgs 12V)



Scalar IC Power



2nd: 74.Z1117.03C(BCD)
11/18 Derek change U43 to P/N: 74.D1117.G3C

Scalar Spec Table

	GPI input		From	High	Low	Default
Pin69	GPI-1 PC Power ON	→ SLP_S3_N 13,39,42,53,56,62	SB	PC	Monitor	Monitor
Pin109	GPI-2 Mode change/ Panel OnOff		SW	Normal	Touch	PC: PC (PC->HDMI) Monitor: HDMI, VGA (HDMI)

GPO output

Pin55	GPO-2 Panel On/OFF	→ SCALAR_VDD_EN 29,42	Scalar	ON	OFF	PC: ON Monitor: Detect Signal
Pin104	GPO-3 PC/Monitor	→ PC_MONITOR_SW 24,42	Scalar	PC	Monitor	PC: PC, Monitor: HDMI, VGA
Pin101	GPO-5 Video	→ BLON_EN# 29,42	Scalar	Disable	Enable	Disable
Pin72	GPO-6 Audio Mute	→ SHDN_MUTE_AP_CTL 42	Scalar	on-Mute	MUTE	MUTE

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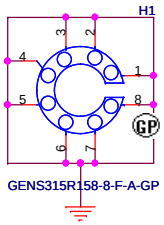
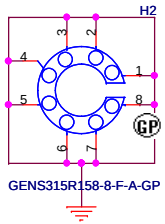
Hsichih, Taipei

Title: SCALAR POWER

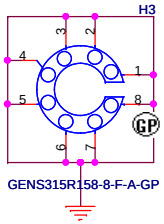
Size: Custom | Document Number: Madrid Lite | Rev: 1A

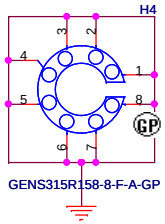
Date: Wednesday, June 18, 2014 | Sheet 43 of 62

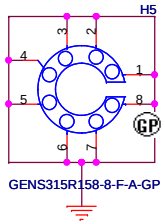




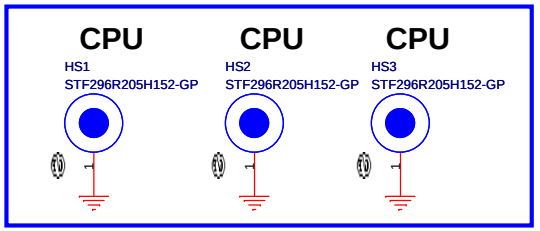
ZZ.SCREW.541



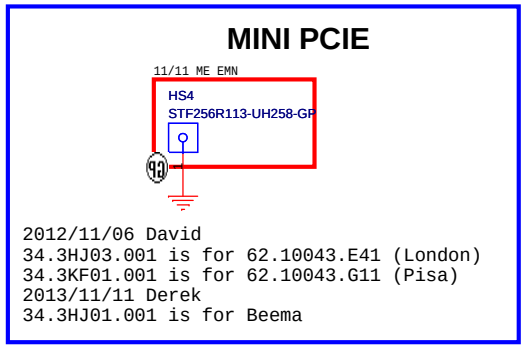




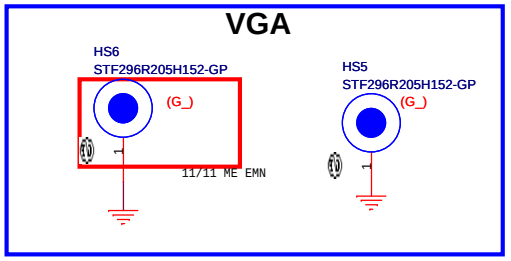
2012/10/2 David
Dallas no Chrome OS



34.3HJ01.001



2012/11/06 David
34.3HJ03.001 is for 62.10043.E41 (London)
34.3KF01.001 is for 62.10043.G11 (Pisa)
2013/11/11 Derek
34.3HJ01.001 is for Beema



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Title: STAND OFF / HOLE / EMI CAP

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B	Madrid Lite	1A

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Material part

LGA115x CPU SOCKET Symbol

Vendor:LOTES
P/N:22.78003.011

Vendor:FOXCONN
P/N:22.78006.001

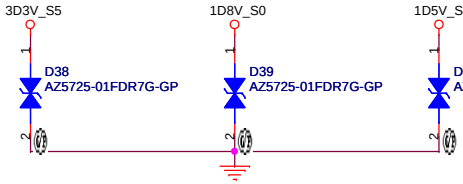
Vendor: LOTES
P/N:22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)

Vendor: FOXCONN
P/N:22.78006.011
Thickness:2.0mm(含mylar)

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

2013/03/19 David
Removed CPU socket & back plate & cover

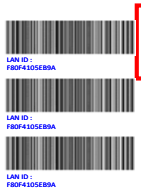


20140618 Bogis
add ESD component
D38 for 3D3V_S5
D39 for 1D8V_S0
D40 for 1D5V_S0

Vendor:LOTES
P/N: 22.78005.171

Vendor:FOXCONN
P/N: 22.78005.161

LABEL



LBL1
LABEL
(45.41107.011)

LBL2
LABEL
(R_)

LBL3
LABEL
(R_)

MB serial NO# and MAC address
40.3KP03.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for aDallas

12/2 Derek change to 70x8mm between CPU and DIMM

HeatSink Symbol

2013/03/19 David
Removed HeatSink

Vendor
P/N:
60.3ET05.001
60.3ET05.011
60.3ET05.021

Stand-off

2013/03/19 David
Removed Stand-off
since already exist

34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41

Battery Symbol

BTT2
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

PCB Symbol

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Hsichih, Taipei

Title: HeatSink/Battery/etc

Size: B | Document Number: Madrid Lite | Rev: 1A

Date: Tuesday, July 22, 2014 | Sheet 45 of 62

PCIEX2

14 PEG_TXP0
14 PEG_TXN0
14 PEG_TXP1
14 PEG_TXN1

14 PCIE_RXP0
14 PCIE_RXN0
14 PCIE_RXP1
14 PCIE_RXN1

13 CK_PE_100M_16PORT_DP
13 CK_PE_100M_16PORT_DN

39 PLTRST_SL_N

49 PEX_RST_GPU

54 PWR_VGA_CORE_SENCE+ → PWR_VGA_CORE_SENCE+

54 PWR_VGA_CORE_SENCE- → PWR_VGA_CORE_SENCE-

+V_3P3_VGA
R679 10KR2J-3-GP (G_)

PLTRST_SL_N — R1212 (G_) 0R2J-2-GP — PEX_RST_GPU
PEX_CLKREQ
CK_PE_100M_16PORT_DP — R1213 (G_) 0R2J-2-GP — CK_PE_100M_16PORT_DP_G
CK_PE_100M_16PORT_DN — R1214 (G_) 0R2J-2-GP — CK_PE_100M_16PORT_DN_G
PCIE_RXP0 — C689 (G_) SCD22U16V2KX-GP — PCIE_RXP_GPU0
PCIE_RXN0 — C691 (G_) SCD22U16V2KX-GP — PCIE_RXN_GPU0
PEG_TXP0
PEG_TXN0
PCIE_RXP1 — C709 (G_) SCD22U16V2KX-GP — PCIE_RXP_GPU1
PCIE_RXN1 — C708 (G_) SCD22U16V2KX-GP — PCIE_RXN_GPU1
PEG_TXP1
PEG_TXN1

GPU1A (G_KG.VGM0V.002) 1 OF 14
1/14 PCI_EXPRESS

GK208/GF117/GF119	
PEX_WAKE#	NC
PEX_RST#	
PEX_CLKREQ#	
PEX_REFCLK	
PEX_REFCLK#	
PEX_TX0	
PEX_TX0#	
PEX_RX0	
PEX_RX0#	
PEX_TX1	
PEX_TX1#	
PEX_RX1	
PEX_RX1#	
PEX_TX2	
PEX_TX2#	
PEX_RX2	
PEX_RX2#	
PEX_TX3	
PEX_TX3#	
PEX_RX3	
PEX_RX3#	
PEX_TX4	
PEX_TX4#	
PEX_RX4	
PEX_RX4#	
PEX_TX5	
PEX_TX5#	
PEX_RX5	
PEX_RX5#	
PEX_TX6	
PEX_TX6#	
PEX_RX6	
PEX_RX6#	
PEX_TX7	
PEX_TX7#	
PEX_RX7	
PEX_RX7#	
PEX_TX8	NC
PEX_TX8#	NC
PEX_RX8	NC
PEX_RX8#	NC
PEX_TX9	NC
PEX_TX9#	NC
PEX_RX9	NC
PEX_RX9#	NC
PEX_TX10	NC
PEX_TX10#	NC
PEX_RX10	NC
PEX_RX10#	NC
PEX_TX11	NC
PEX_TX11#	NC
PEX_RX11	NC
PEX_RX11#	NC
PEX_TX12	NC
PEX_TX12#	NC
PEX_RX12	NC
PEX_RX12#	NC
PEX_TX13	NC
PEX_TX13#	NC
PEX_RX13	NC
PEX_RX13#	NC
PEX_TX14	NC
PEX_TX14#	NC
PEX_RX14	NC
PEX_RX14#	NC
PEX_TX15	NC
PEX_TX15#	NC
PEX_RX15	NC
PEX_RX15#	NC
GF119	GF117
	GK208

N14M-GE-S-A2-GP

PEX_IOVDD ×10 — +V_1P05_VGA
C688 SC1U16V3KX-1-GP (G_78.10520.5FL)
C690 SC1U16V3KX-1-GP (G_78.10520.5FL)
C712 SCD1U16V3KX-1-GP (G_78.47520.5BL)
C715 SCD1U16V3KX-1-GP (G_)
C714 SCD1U16V3KX-1-GP (G_)
C721 SC22U6D3V5MX-2-1-GP (G_78.22610.51L)
C722 SC22U6D3V5MX-2-1-GP (G_78.22610.51L)

PEX_IOVDD ×10 — +V_1P05_VGA
C710 SC1U16D3V3KX-1-GP (G_78.10520.5FL)
C706 SC1U16D3V3KX-1-GP (G_78.10520.5FL)
C720 SCD1U16D3V3KX-1-GP (G_78.47520.5BL)
C718 SCD1U16D3V3KX-1-GP (G_)
C711 SCD1U16D3V3KX-1-GP (G_)
C713 SC22U6D3V5MX-2-1-GP (G_78.22610.51L)
C725 SC22U6D3V5MX-2-1-GP (G_78.22610.51L)

PEX_PLL_HVDD ×2 — +V_3P3_VGA
PEX_SVDD_3V3
C719 SC1U10V2KX-1-GP (G_78.10421.2FL)
C717 SCD1U16D3V3KX-1-GP (G_78.47520.5BL)
C707 SCD1U16D3V3KX-1-GP (G_78.47520.5BL)

VDD_SENSE F2 — PWR_VGA_CORE_SENCE+ → PWR_VGA_CORE_SENCE+ 54
GND_SENSE F1 — PWR_VGA_CORE_SENCE- → PWR_VGA_CORE_SENCE- 54

PEX_TSTCLK_OUT AF22 — PEX_TSTCLK_OUT — R370 (G_) 200R2F-L-GP — PEX_TSTCLK_OUT# AF22

PEX_PLLVDD ×2 — PEX_PLLVDD_GPU — +V_1P05_VGA
L28 MCB1608S121IBP-GP (G_68.00335.141)
C723 SC1U16V3KX-2GP (G_)
C716 SC1U10V2KX-1-GP (G_78.10421.2FL)
C724 SC4D7U25V5KX-GP (G_)
C467 SC4D7U25V5KX-GP (G_)
C687 SC4D7U25V5KX-GP (G_)

TESTMODE AD9 — GPU_TESTMODE — R371 (G_) 10KR2J-3-GP

PEX_TERMP AF25 — PEX_TERMP — R480 (G_) 2K49R2F-GP

1U Under GPU

4.7U NEAR TO GPU

10U mid TO GPU

Michael 2011/12/12

Add two 1uF Caps according to the NV Comment

20140514 Nick change F7 to 68.00335.141

100MHZ 120mohm

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Hsichih, Taipei

Title: GPU(1/5): PCI Express

Size	Document Number	Rev
C	Madrid Lite	1A

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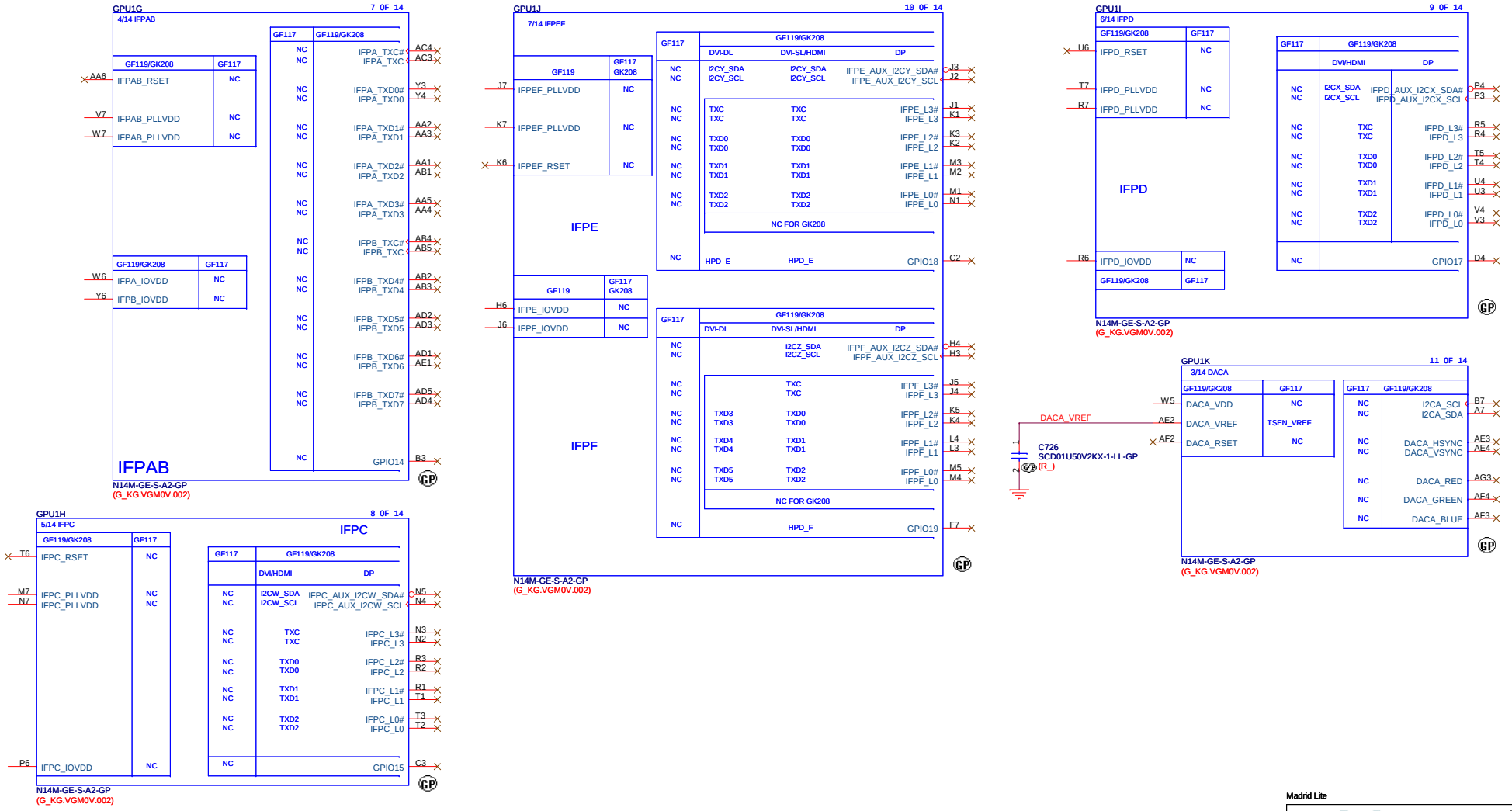

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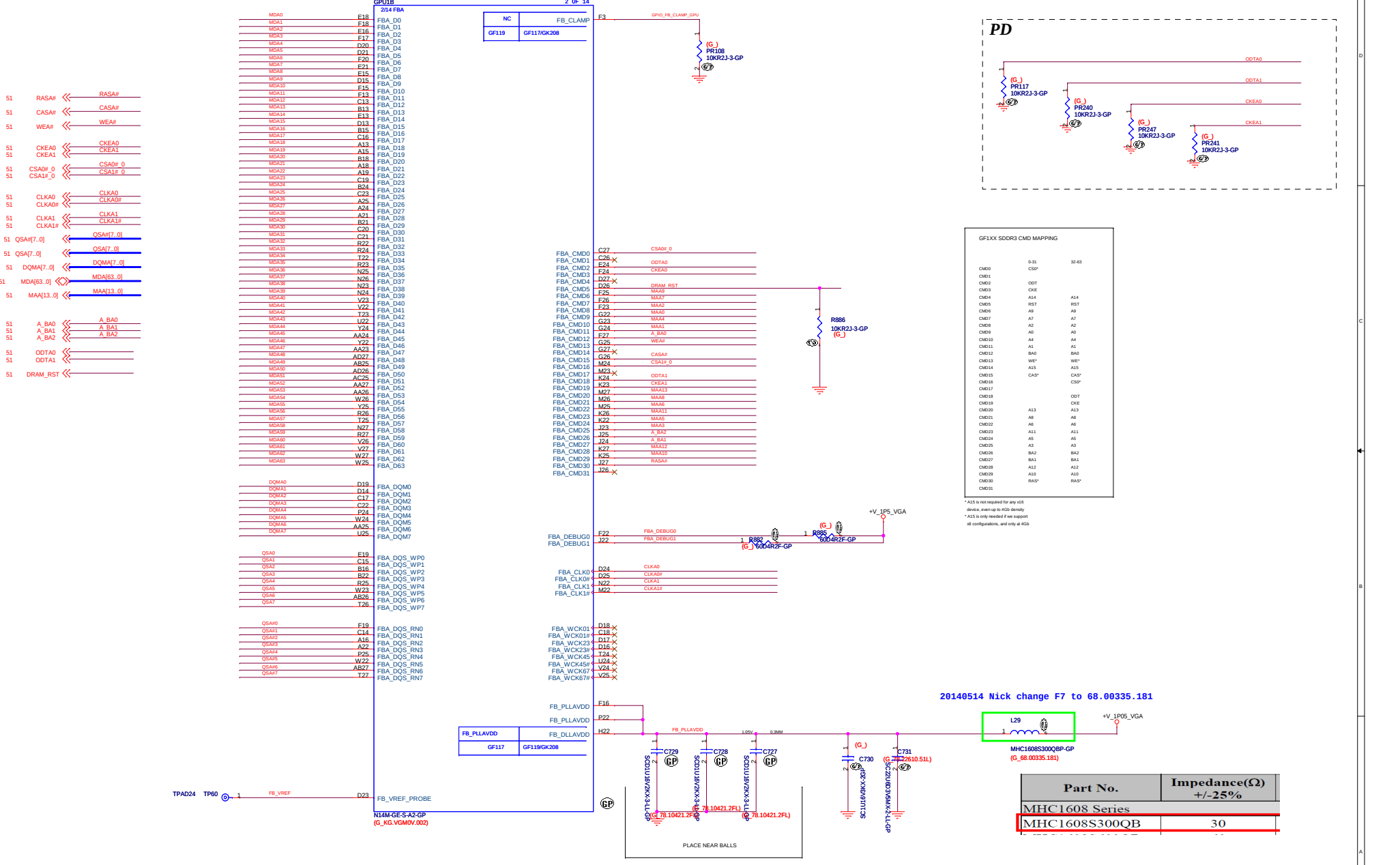
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: GPU(2/5): IFB(IO)

Size: Custom | Document Number: Madrid Lite | Rev: 1A

Date: Thursday, June 19, 2014 | Sheet 47 of 62


GPU1B
2 OF 14
2/14 FBA
N14M-GE-S-A2-GP
(G_KG.VGM0V.002)
PD
GF1XX SDDR3 CMD MAPPING
20140514 Nick change F7 to 68.00335.181
Part No.
Impedance(Ω) +/-25%
MHC1608 Series
MHC1608S300QB
30
PLACE NEAR BALLS
Madrid Lite
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
GPU(3/5): MEMORY FBA
Madrid Lite
Thursday, June 19, 2014
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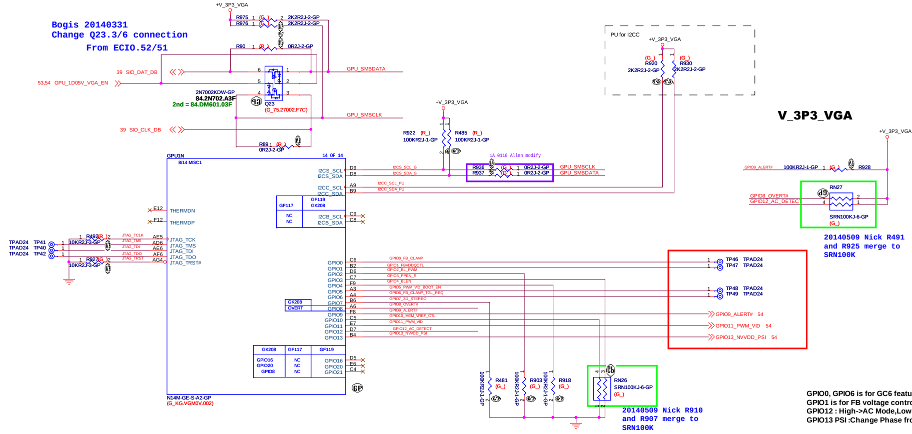
Bogis 20140331
Change Q23.3/6 connection
From ECIO.52/51



V_3P3_VGA

20140509 Nick R491
and R925 merge to
SRN100K

20140509 Nick R910
and R907 merge to
SRN100K

GPIO	GF117
GPIO 0	FAN_PWM/FB_CLAMP/DEBUG Service
GPIO 1	MEM_VDD_CTL
GPIO 2	UNUSED
GPIO 3	UNUSED
GPIO 4	UNUSED
GPIO 5	Reserved
GPIO 6	FB_CLAMP_TGL_REQ
GPIO 7	3DVision(UNUSED)
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert
GPIO 10	FB Vref Control
GPIO 11	NVVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	UNUSED(No Need to Set in VBIOS)
GPIO 14	N/A on Package
GPIO 15	N/A on Package
GPIO 16	N/A on Package
GPIO 17	N/A on Package
GPIO 18	N/A on Package
GPIO 19	N/A on Package
GPIO 20	N/A on Package
GPIO 21	N/A on Package

Table 115. GB2-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: Strap to boot FBVDD/Q
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 78
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 78
GPIO16	FRM_LCK	O	JT Frame Lock signal	
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 78
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 78
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB used as DisplayPort	See Figure 78
GPIO20	Reserved			
GPIO21	Reserved			

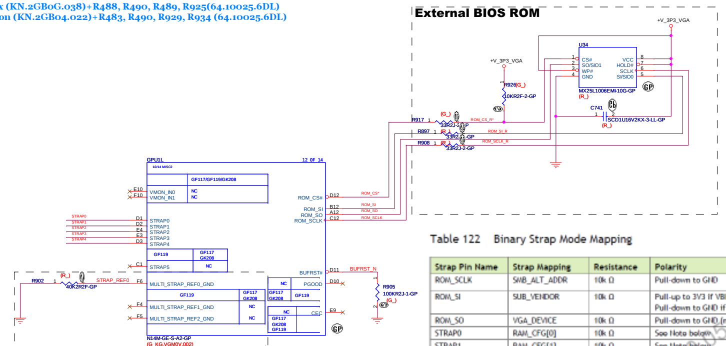
- GPIO20 and GPIO21 are only available on N14M-LP/-GS/-HE/-HS & N14P-GV/-GV2
- The greyed out section of Table 107 indicates GPIOs that are not available for N14M-GE/-GL

GPIO0, GPIO6 is for GC6 feature, no need to connect since this project won't support GC6.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12 : High->AC Mode,Low->Battery Mode enter slow down functionpull for power saving.Recommand:Pull-High for AC mode.
GPIO13 PSI :Change Phase from two to one, and thean enter slow down functionpull for power saving.

STRAP

QVL1: Hynix (KN.2GB0G.038)+R488, R490, R489, R925(64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R483, R490, R929, R934 (64.10025.6DL)

External BIOS ROM



STRAP PIN MODE TABLE

PIN NAME	BINARY BRINGUP
STRAP0	3GIO_PADCFG_LUT_ADR0
STRAP1	3GIO_PADCFG_LUT_ADR1
STRAP2	3GIO_PADCFG_LUT_ADR2
STRAP3	3GIO_PADCFG_LUT_ADR3
STRAP4	PCI_MAX_SPEED
ROM_SCLK	SMB_ALT_ADDR
ROM_SI	SUB_VENDOR
ROM_SO	VGA_DEVICE

NOTE 2: See table 1 for the correct value/location of the strap resistor for the desired modes

NOTE 3: Bring-up SKU(s) have jumper configurable subvendor and DEVID_4 settings see the ROM_SCLK STRAP

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M×16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1150	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-N0C	1000	N/A	Production Candidate
				H5TQ2G63DFR-11C	900	N/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production Candidate
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Refer to the latest version of N14M-GE/-GL *Memory Recommended Vendor List* for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

Table 119. Device Specific Strap Mode Selection

	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Binary	Multi-Level

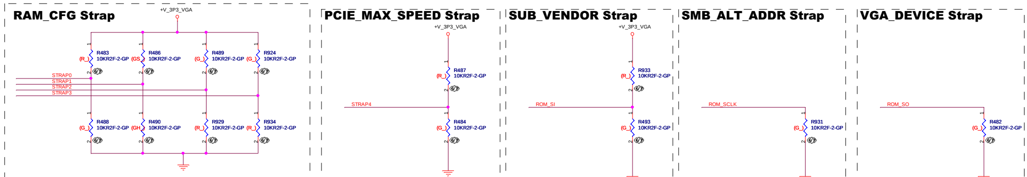
RAM_CFG Strap

PCIE_MAX_SPEED Strap

SUB_VENDOR Strap

SMB_ALT_ADDR Strap

VGA_DEVICE Strap

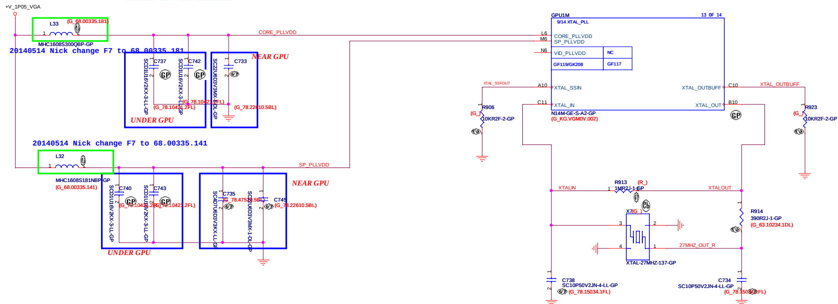


RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

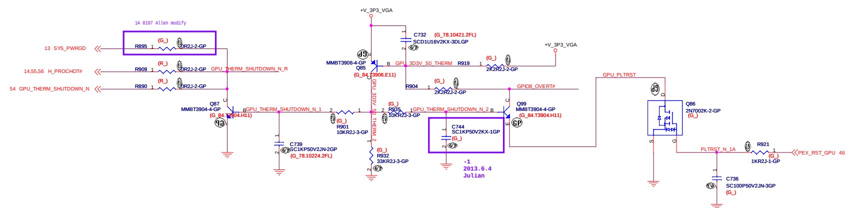
XTAL

20140514 Nick change F7 to 68.00335.181

20140514 Nick change F7 to 68.00335.141



THERMAL PROTECTION



VRAM ID [0-3]:

Mount	Un-mount	VRAM Type	P/N
R488 、R490 、R489 、R924	R483 、R486 、R929 、R934	Hynix 1GHz H5TC2G63FFR-11C	KN.2GB0G.038
R483 、R490 、R929 、R934	R488 、R486 、R489 、R924	MICRON 1GHz MT41J128M16JT-093G:K	KN.2GB04.022
R488 、R486 、R489 、R924	R483 、R490 、R929 、R934	SAMSUNG 1G K4W2G1646Q-BC1A	KN.2GB0B.040

Mount 10K 64.10025.6DL

VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038			V	V
	72.52G63.N0U	V	V		

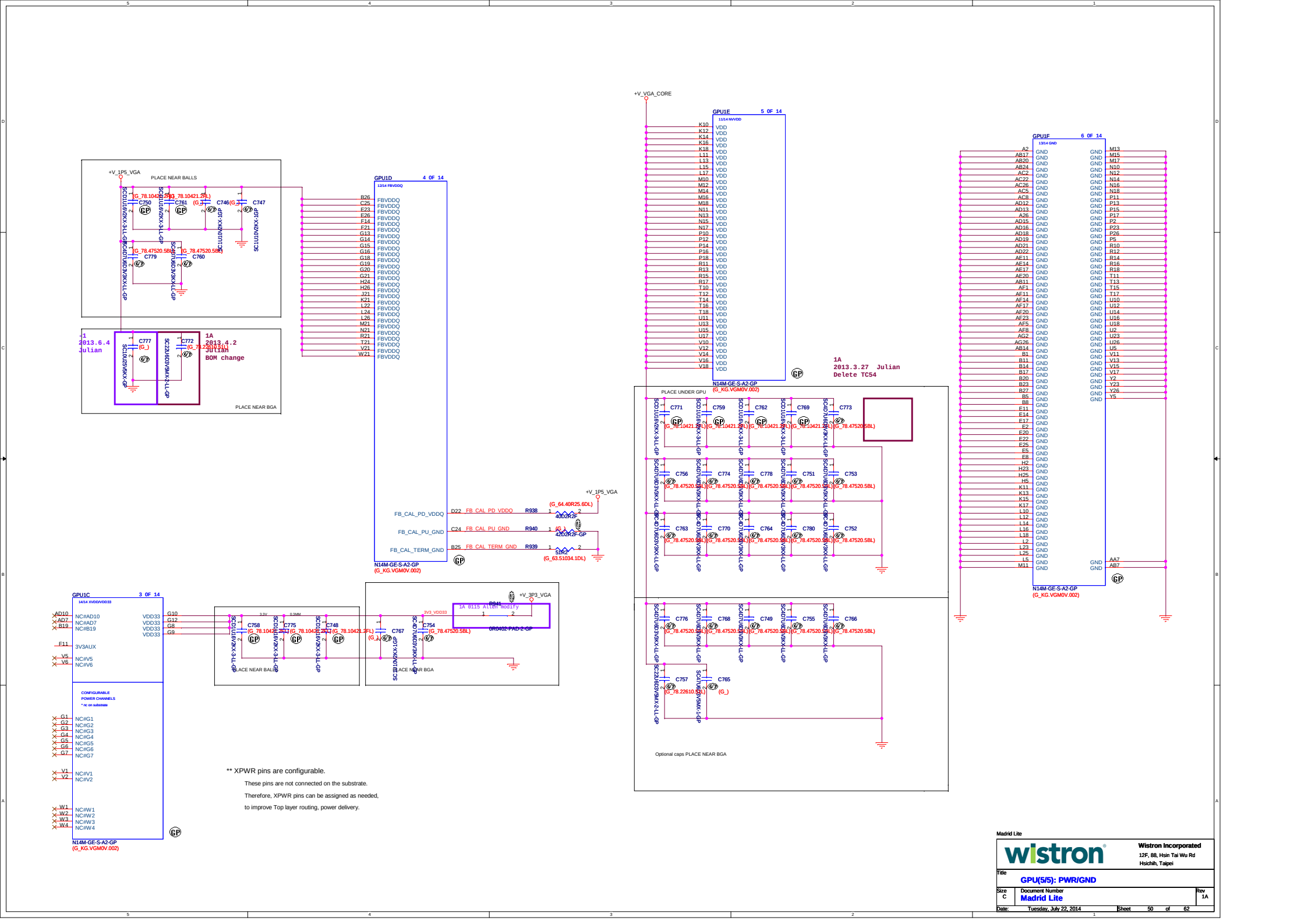
VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022	V			
	72.41128.I0U		V	V	V

VRAM ID [0-3]:

VRAM Type	P/N	0	1	2	3
SAMSUNG 1G K4W2G1646Q-BC1A	KN.2GB0B.040		V	V	V
		V			

KN.2GB0B.041


+V_1P5_VGA
PLACE NEAR BALLS
C750
C761
C746
C747
C779
C760
PLACE NEAR BGA
C777
C772
1A
2013.4.2
Julian
BOM change
+1
2013.6.4
Julian
GPU1D
4 OF 14
12/14 FBVDDQ
FBVDDQ
N14M-GE-S-A2-GP
(G_KG.VGM0V.002)
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
D22
C24
B25
R938
R940
R939
+V_1P5_VGA
(G_64.40R25.6DL)
(G_63.51034.1DL)
+V_VGA_CORE
GPU1E
5 OF 14
11/14 NVVDD
VDD
1A
2013.3.27 Julian
Delete TC54
PLACE UNDER GPU
C771
C759
C762
C769
C773
C756
C774
C778
C751
C753
C763
C770
C764
C780
C752
C776
C768
C749
C755
C766
C757
C765
Optional caps PLACE NEAR BGA
GPU1F
6 OF 14
13/14 GND
GND
N14M-GE-S-A2-GP
(G_KG.VGM0V.002)
GPU1C
3 OF 14
14/14 XVDD/VDD33
NC#AD10
NC#AD7
NC#B19
3V3AUX
NC#V5
NC#V6
CONFIGURABLE
POWER CHANNELS
* nc on substrate
NC#G1
NC#G2
NC#G3
NC#G4
NC#G5
NC#G6
NC#G7
NC#V1
NC#V2
NC#W1
NC#W2
NC#W3
NC#W4
VDD33
C758
C775
C748
C767
C754
3V3_VDD33
+V_3P3_VGA
R941
1A 8115 After modify
0R0402-PAD-2-GP
PLACE NEAR BALLS
PLACE NEAR BGA
** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.
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C
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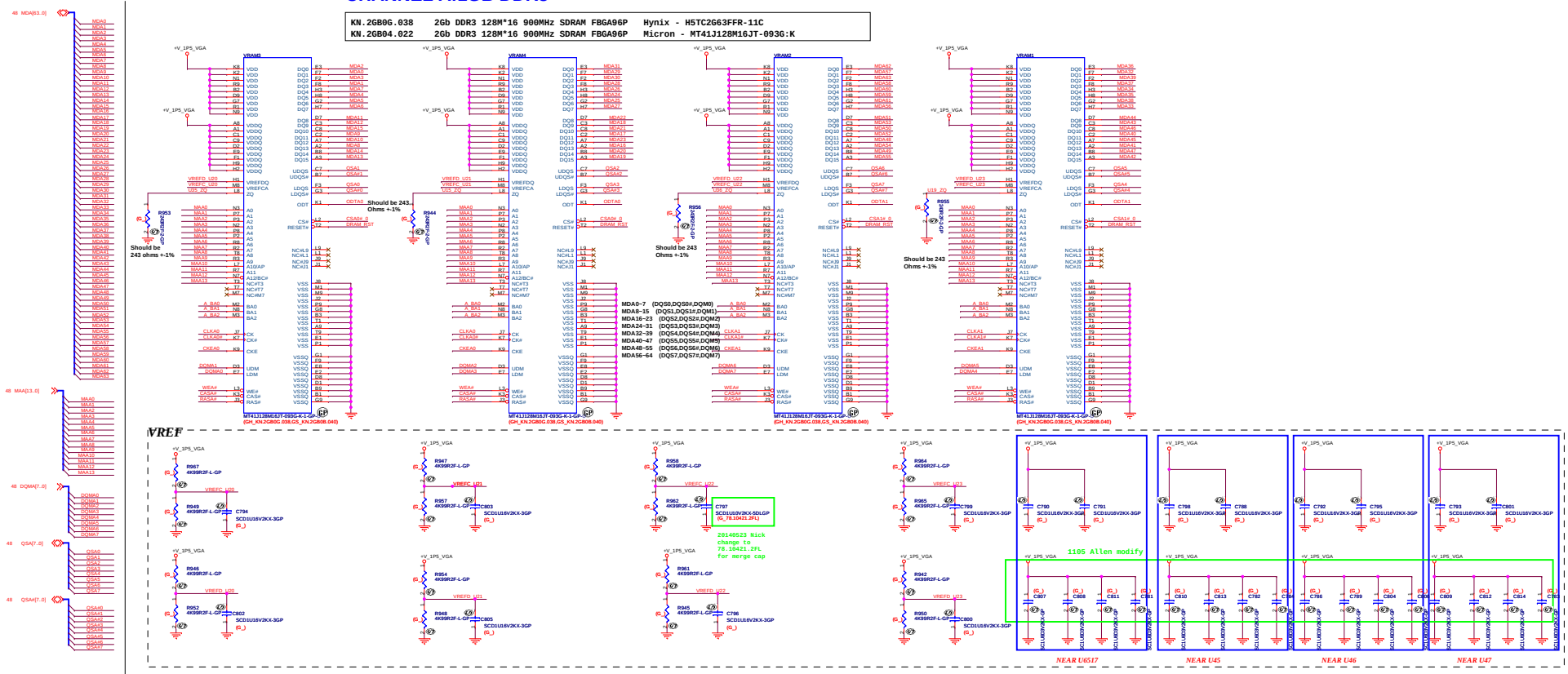
VRAM Type	P/N
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038

QVL1: Hynix (KN.2GB0G.038)+R221, R220, R231, R238 (64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R234, R238, R228, R219 (64.10025.6DL)

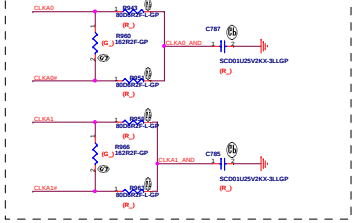
VRAM Type	P/N
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022

CHANNEL A:1GB DDR3

KN.2GB0G.038	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Hynix - H5TC2G63FFR-11C
KN.2GB04.022	2Gb DDR3 128M*16 900MHz SDRAM FBGA96P	Micron - MT41J128M16JT-093G:K



FBCLK Termination place on VRAM side



128M*16 VRAM
KN.2GB0B.040 - Samsung K4W2G1646Q-BC1A
KN.2GB0G.038 - Hynix H5TC2G63FFR-11C

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Data Rate	Interface	Package
H5TC2G63FFR-11C	VDD/VDDQ=1.35V	900MHz	1.8Gbps/pin	SSTL-15	96ball FBGA
	VDD/VDDQ=1.5V	1.0GHz	2.0Gbps/pin		
H5TQ2G63FFR-N1C	VDD/VDDQ=1.5V	1.1GHz	2.2Gbps/pin		

Note) 1.35v speed part provides backward compatibility with the 1.5V DDR3.

1. Ordering Information

[Table 1] Samsung 2Gb gDDR3 Q-die ordering information table

Organization	gDDR3-1600(11-11-11)	gDDR3-1866(13-13-13)[2]	gDDR3L-1866(13-13-13)[2]	gDDR3-2133(14-14-14)[2]	Package
VDD	1.5V	1.5V	1.35V	1.5V	
128Mx16	K4W2G1646Q-BC12	K4W2G1646Q-BC11	K4W2G1646Q-BC1A		96 FBGA

NOTE
1. Speed bin is in order of CL-tRCD-tRP
2. Backward Compatible to gDDR3-1600(13-13-13), gDDR3-1600(11-11-11)
3. Backward Compatible to gDDR3-1600(11-11-11)

RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

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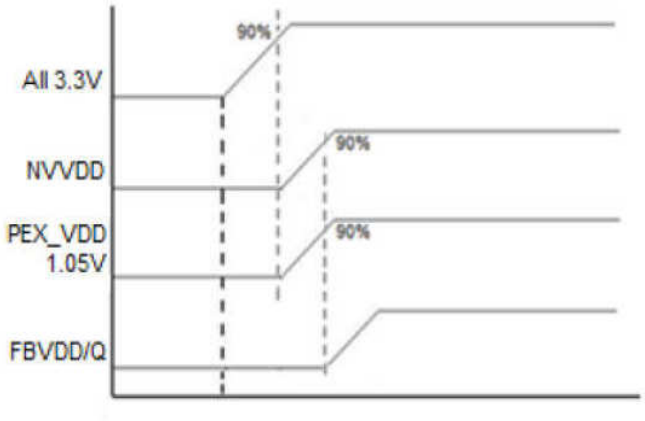
3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

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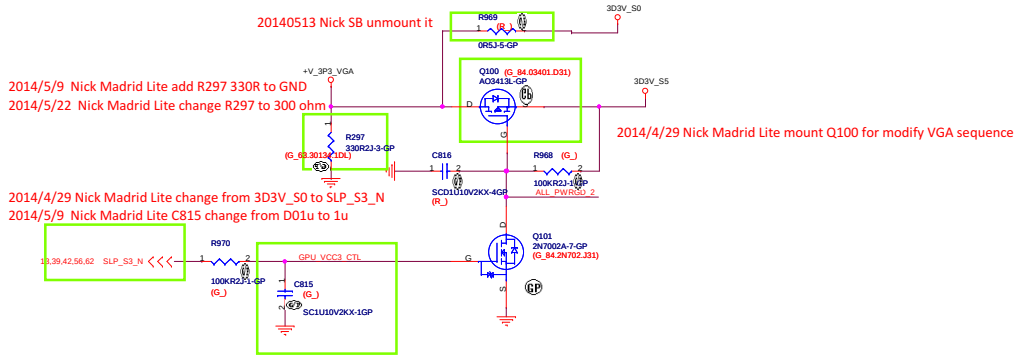
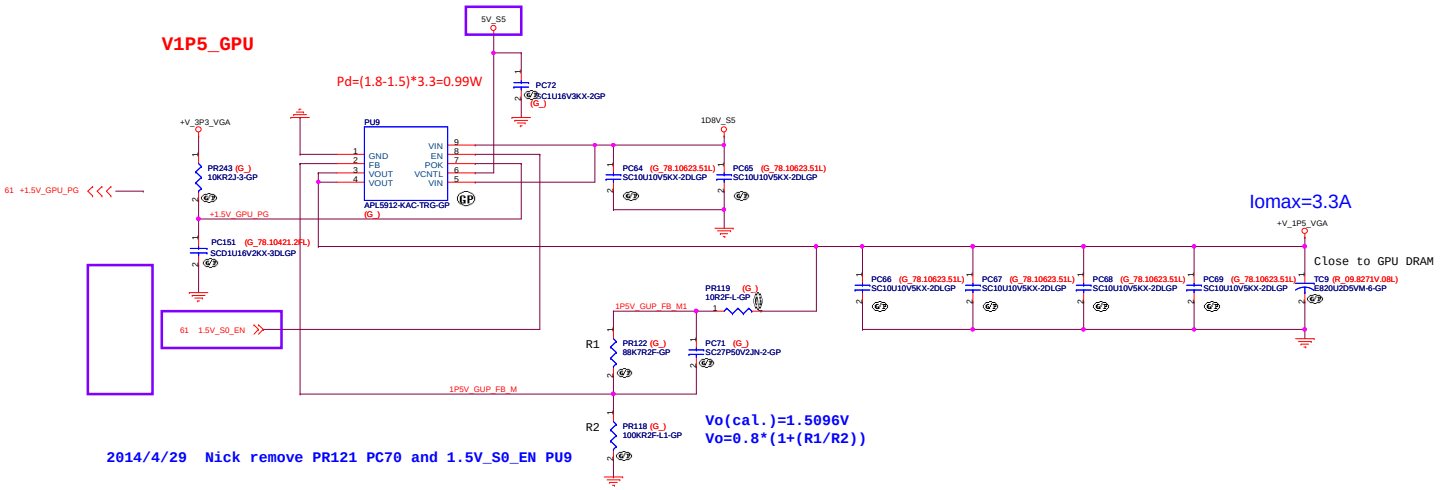
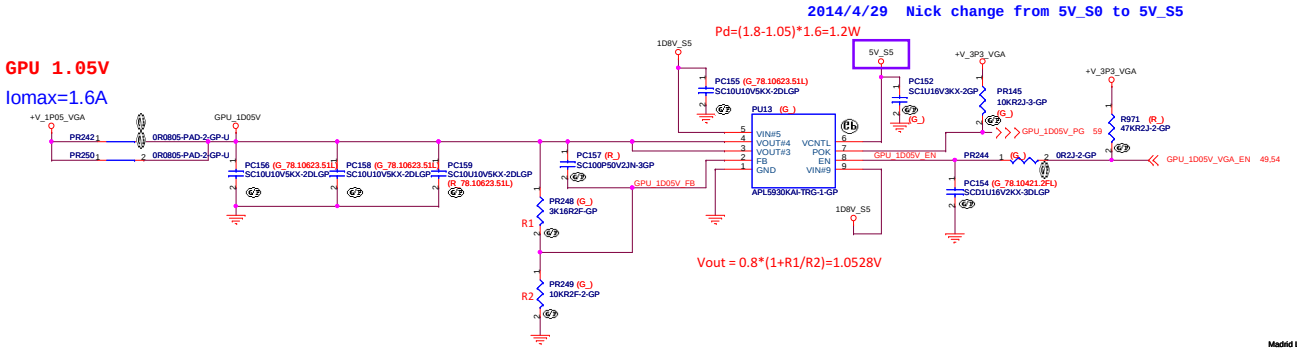
3D3V_S0 to 3D3V_DELAY Transfer



2014/4/29 Nick change from 5V_S0 to 5V_S5



2014/4/29 Nick change from 5V_S0 to 5V_S5



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Title: GPU_CTF/PPLAY/LDO/MVDD

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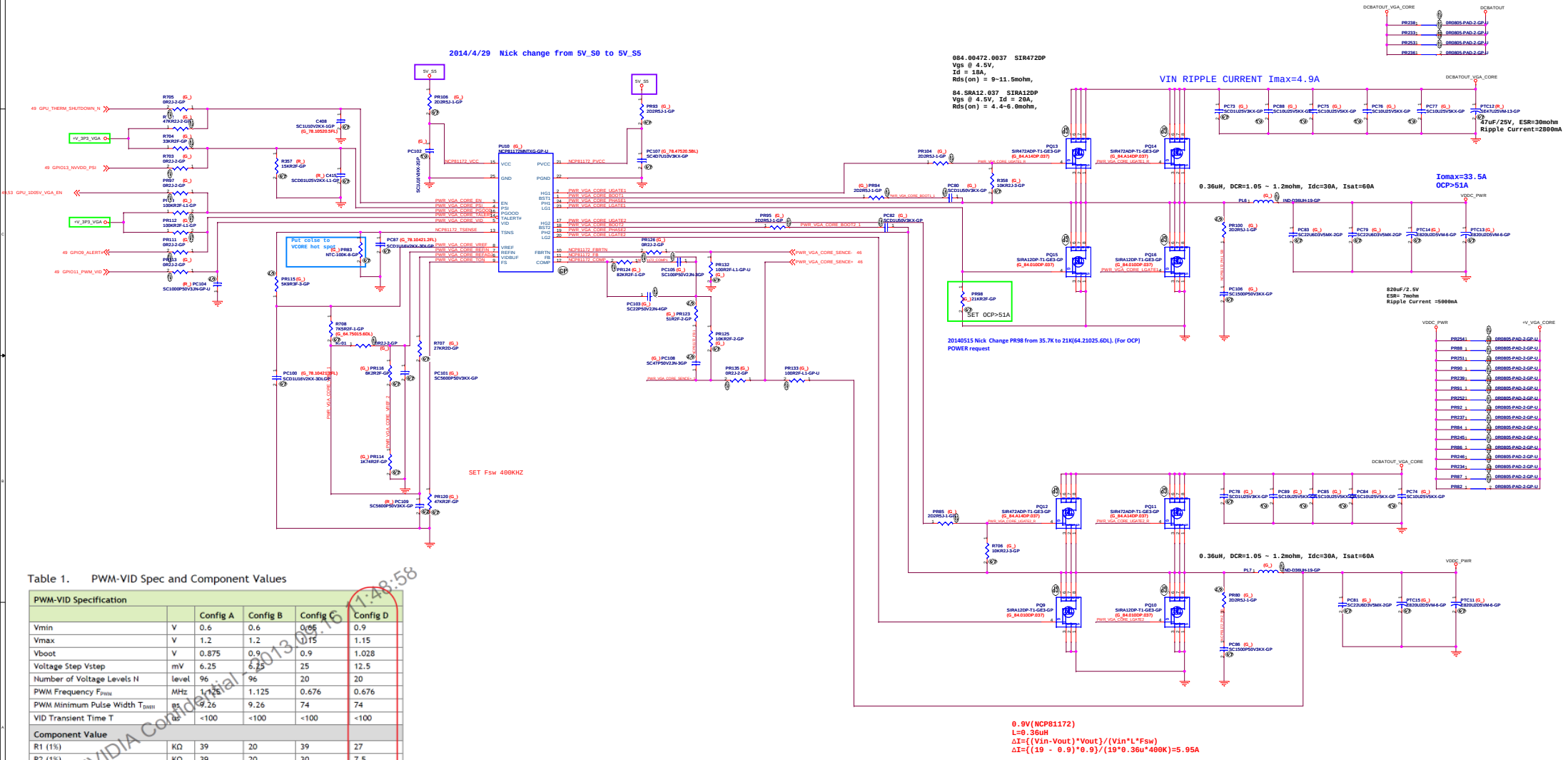

Table 1. PWM-VID Spec and Component Values

PWM-VID Specification					
		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

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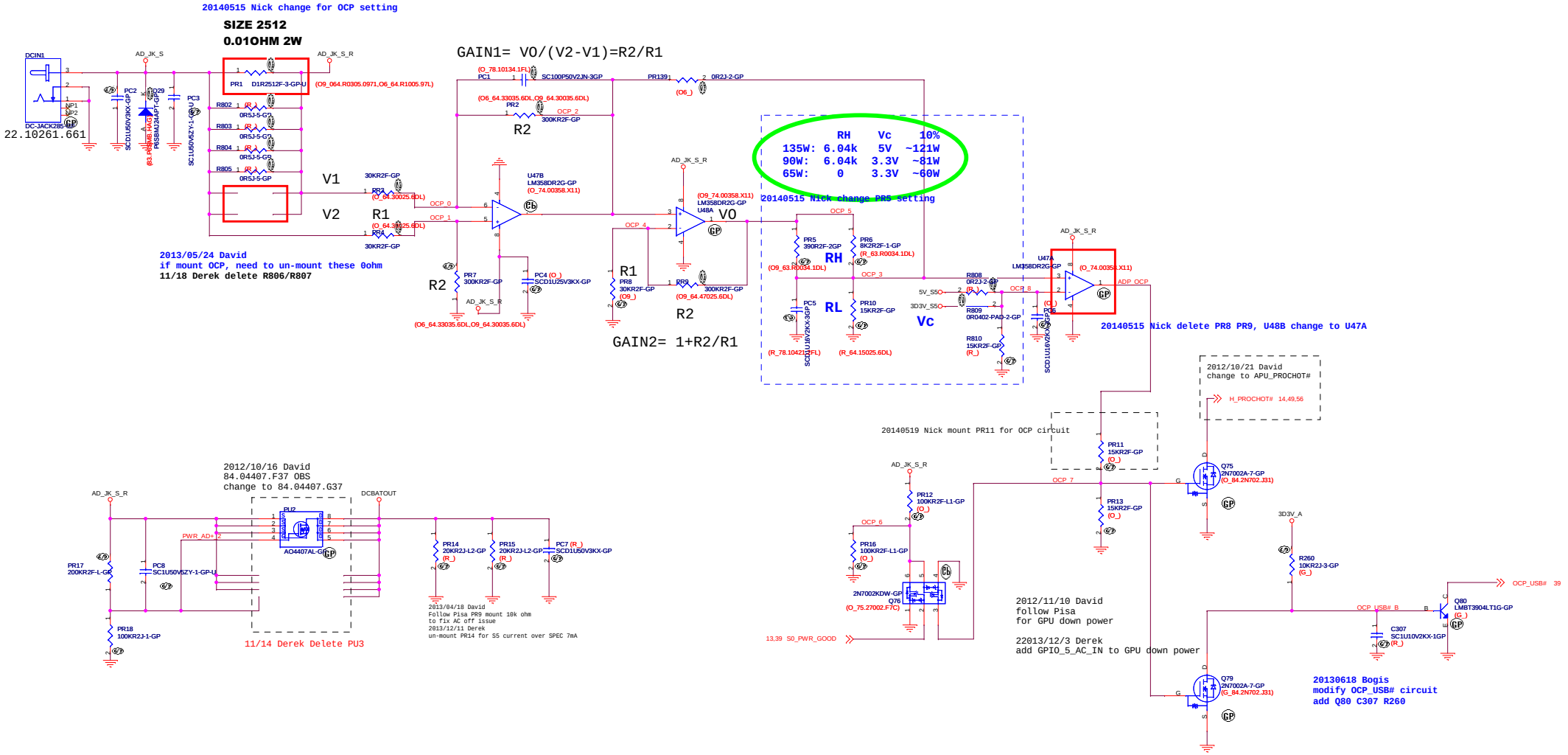
ANNIE solution



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Title: PWR_DCIN JACK

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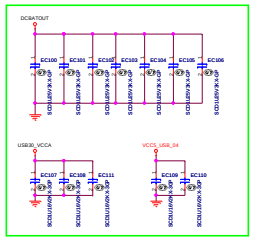
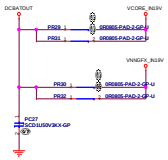


20140514 Nick SB add for EMI
20140516 Nick SB add for EMI

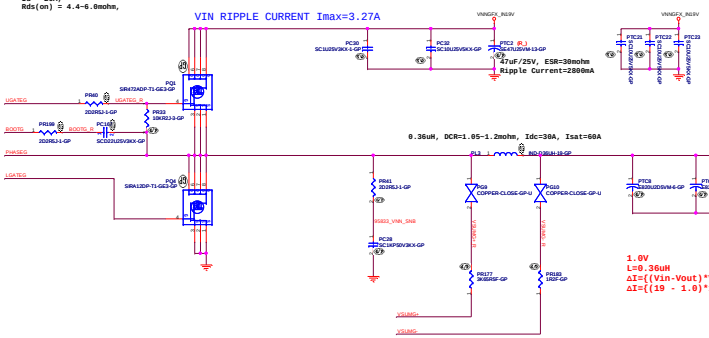


084.00472.0037 SIR472DP
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9~11.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 28A,
Rds(on) = 4.4~6.0mohm,

20140709 PTC2 can unmount and co-layout and change to 3pcs MLCC 78.10622.51L

VIN RIPPLE CURRENT Imax=3.27A



47uF/25V, ESR=30mohm
Ripple Current=2800mA

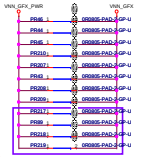
0.36uH, DCR=1.05~1.2mohm, Idc=30A, Isat=60A

Iomax=14A

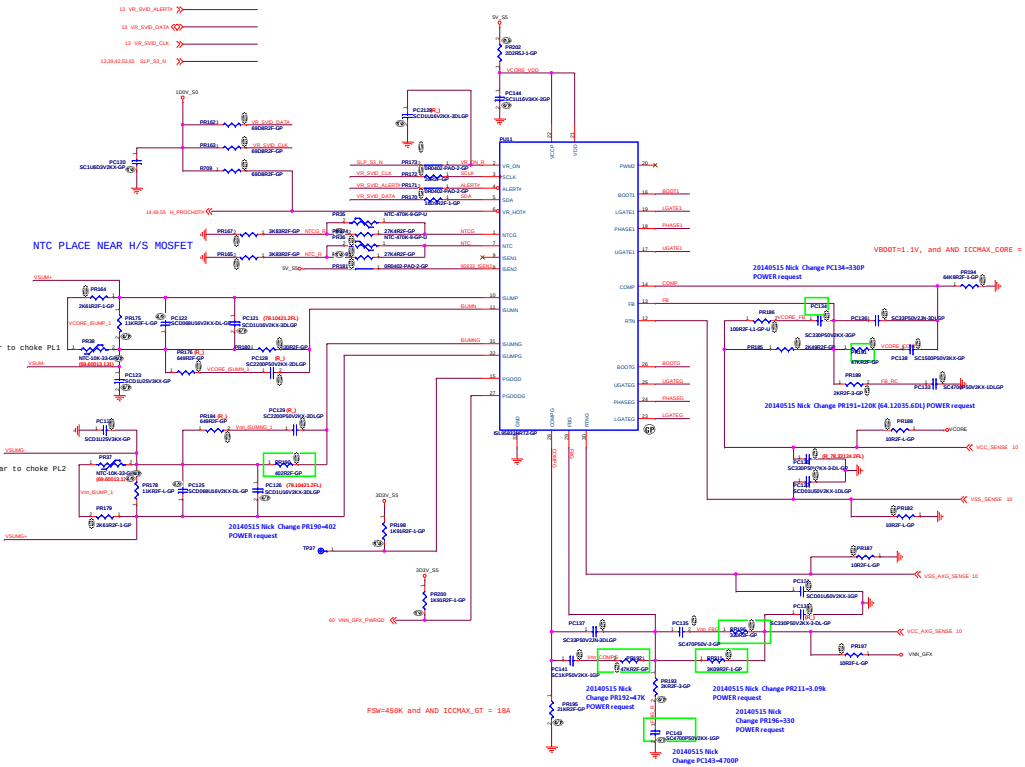
820uF/2.5V
ESR= 7mohm
Ripple Current =5000mA

1.0V
L=0.36uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19 - 1.0)*1.0}/(19*0.36u*450K)=5.85A

20150515 Nick add for power request



NTC PLACE NEAR H/S MOSFET



PR38 place near to choke PL1

PR37 place near to choke PL2

20140515 Nick Change PR190=402 POWER request

20140515 Nick Change PC134=330P POWER request

20140515 Nick Change PR191=120K (64.12035.6DL) POWER request

20140515 Nick Change PR192=47K POWER request

20140515 Nick Change PR211=3.09k POWER request

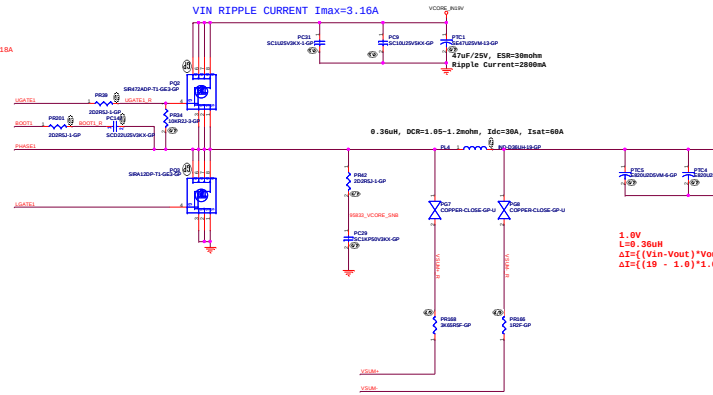
20140515 Nick Change PR196=330 POWER request

20140515 Nick Change PC143=4700P POWER request

VBOOT=1.1V, and AND ICCMAX_CORE = 18A

FSW=450K and AND ICCMAX_GT = 18A

VIN RIPPLE CURRENT Imax=3.16A



47uF/25V, ESR=30mohm
Ripple Current=2800mA

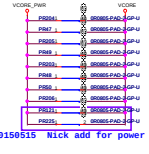
0.36uH, DCR=1.05~1.2mohm, Idc=30A, Isat=60A

Iomax=13.5A

820uF/2.5V
ESR= 7mohm
Ripple Current =5000mA

1.0V
L=0.36uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19 - 1.0)*1.0}/(19*0.36u*450K)=5.85A

20150515 Nick add for power request



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PWR_CPU CORE&VNN

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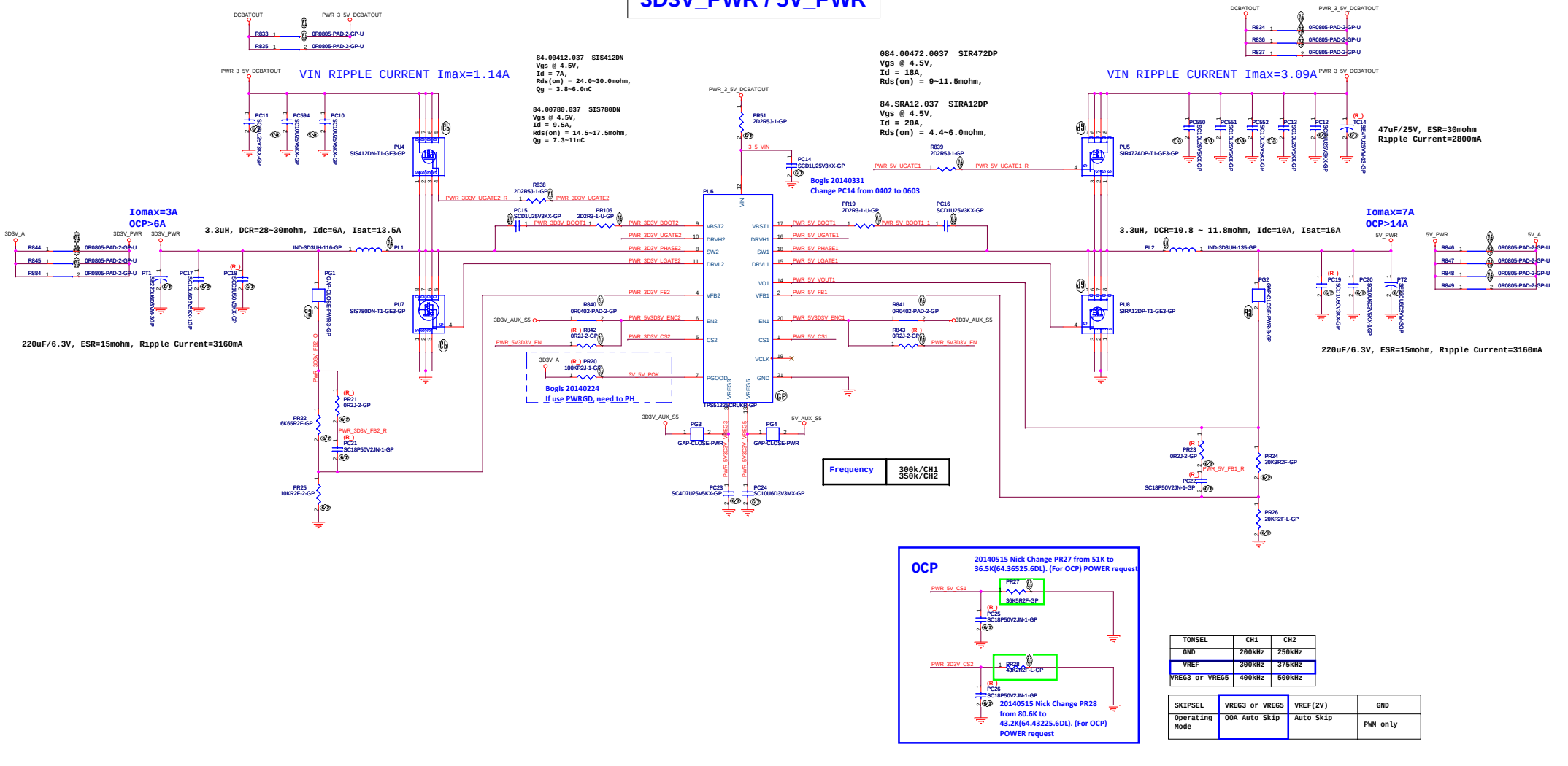
3D3V_PWR / 5V_PWR



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Title: PWR_5V / 3D3V

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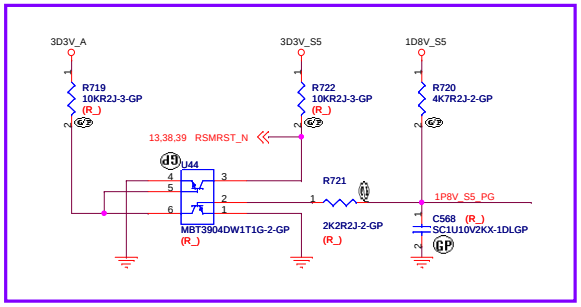

084.00472.0037 SIR472DP
Vgs @ 4.5V,
Id = 18A,
Rds(on) = 9~11.5mohm,

84.SRA12.037 SIRA12DP
Vgs @ 4.5V,
Id = 20A,
Rds(on) = 4.4~6.0mohm,

VIN RIPPLE CURRENT Imax=2.79A

DCBATOUT_1D8V
DCBATOUT
PR55 0R0805-PAD-2-GP-U
PR56 0R0805-PAD-2-GP-U

PC39 SCD1U25V3KX-GP
PC38 SC10U25V5KX-GP
PC33 SC10U25V5KX-GP
PC35 SC10U25V5KX-GP

Imax=9.5A,
IOCP>14.25A

PQ7 SIR472ADP-T1-GE3-GP
PR62 2D2R5J-1-GP
1P8V_PWR_UGATE
1P8V_PWR_UGATE_R
R95 10KR2J-3-GP

PR57 2D2R5J-1-GP
PC42 SCD1U25V3KX-GP
1P8V_PWR_BOOT_R

1.5uH, DCR=3.8~4.2mohm, Idc=16A, Isat=33A

PL8 IND-1D5UH-52-GP

PU12
1P8V_S5_PG
1P8V_PWR_CS
1P8V_PWR_EN
1P8V_PWR_FB
1P8V_PWR_RF
60 1P8V_PWR_EN
PGOOD
CS
EN
FB
RF
GND
BOOT
UGATE
PHASE
VCC
LGATE
1P8V_PWR_BOOT
1P8V_PWR_UGATE
1P8V_PWR_PHASE
1P8V_PWR_LGATE
RT8237CZQW-2-GP

PR64 62KR2F-GP
PR61 470KR2F-GP
PWM Frequency setting

ROSC=46.4K ohm
IOCP=14.25A

RF=470K ohm,
PWM Freq=290K Hz

5V_S5
PR52 2D2R5J-1-GP
1P8V_PWR_VSIN
PC34 SC1U16V3KX-2GP

PQ8 SIRA12DP-T1-GE3-GP

PR53 2D2R5J-1-GP
1P8V_PWR_SNB
PC37 SC1500P50V3KX-GP
PC41 (R_) SC22P50V2JN-L-GP

PR59 15K8R2F-GP
R1
1P8V_PWR_FB
PR58 10KR2F-2-GP
R2

VOUT=(1+R1/R2)*0.7
Vo(cal.)=1.806V

PC36 SC1U16V3KX-2GP
PC40 SC10U6D3V5KX-1GP
PTC9 E820U2D5VM-6-GP

820uF/2.5V
ESR= 7mohm
Ripple Current =5000mA

1P8V_PWR
1D8V_S5
PR60 0R0805-PAD-2-GP-U
PR212 0R0805-PAD-2-GP-U
PR214 0R0805-PAD-2-GP-U
PR213 0R0805-PAD-2-GP-U
PR63 0R0805-PAD-2-GP-U
PR54 0R0805-PAD-2-GP-U

R298
330R2J-3-GP

20140521 Nick add R298 near PR54

1.8V(RT8237C)
L=1.5uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19 - 1.8)*1.8}/(19*1.5u*290K)=3.75A

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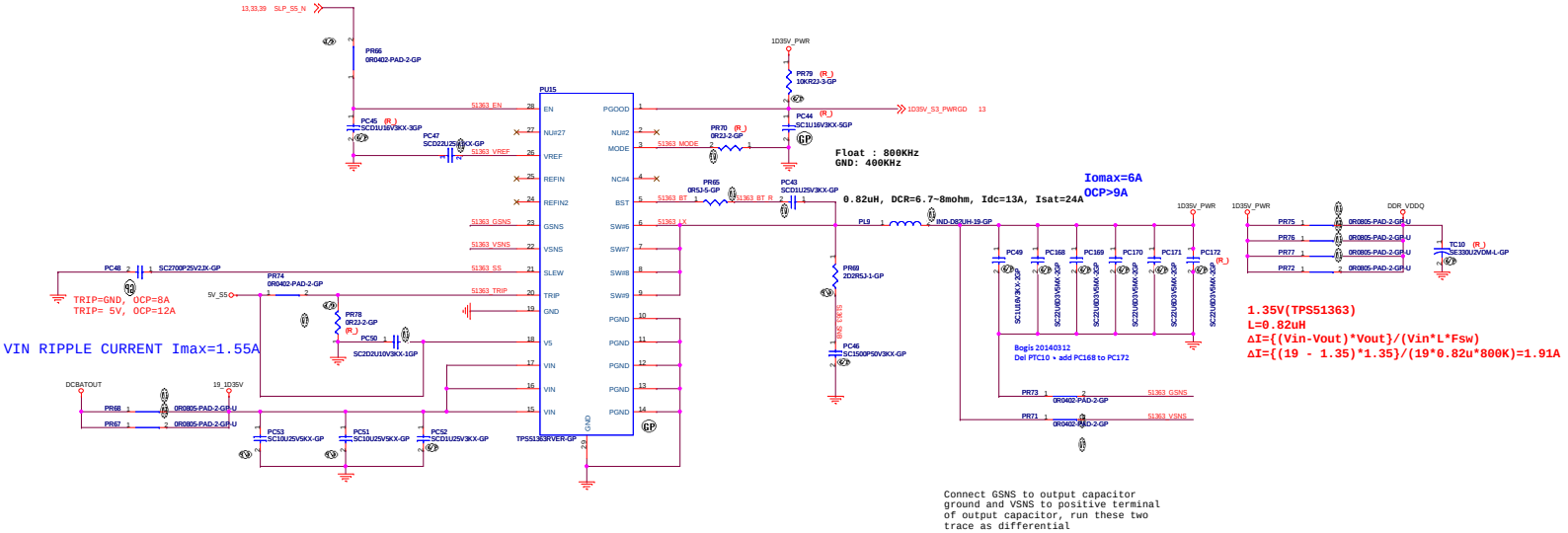
DDR_1.35V

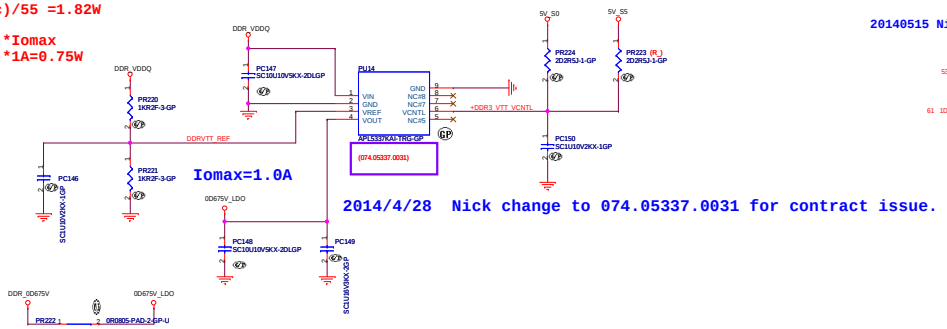


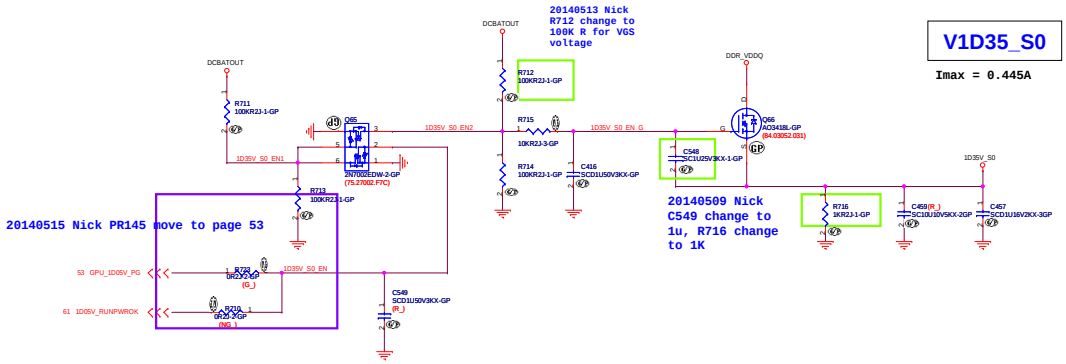
V_SM_VTT

PD Internally Limit
(125'c - 25'c)/55 =1.82W

PD=(Vin-Vout)*Iomax
=(1.5-0.75)*1A=0.75W

DDR3_MEM_VTT
0D675V





V1D35_S0

Imax = 0.445A

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Hsichih, Taipei

Title: PWR_1D35V_0D675_TPS51363

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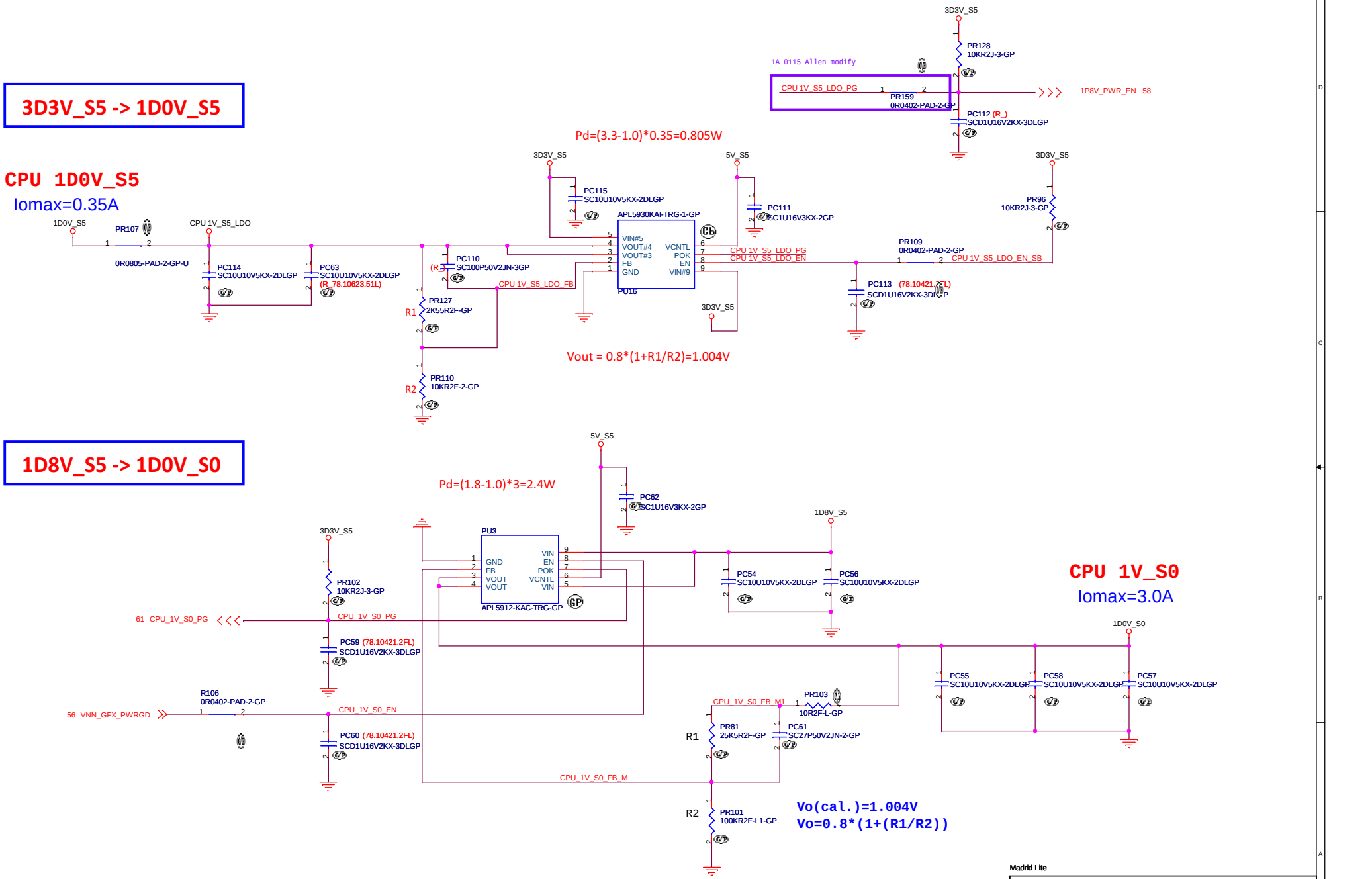

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Title: PWR_CPU 1V_S0&CPU 1V_S5

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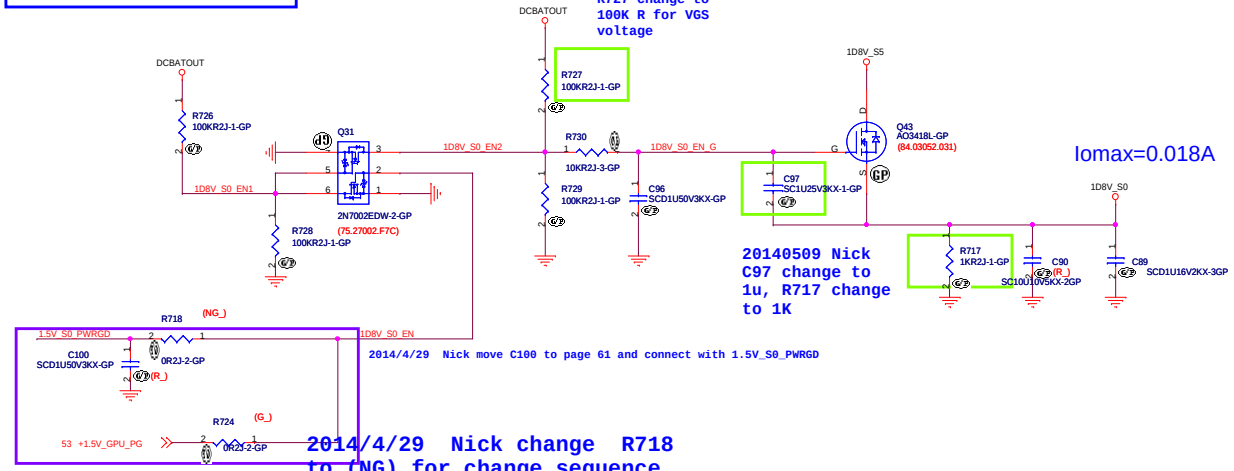
1D8V_S5 -> 1D8V_S0

20140513 Nick R727 change to 100K R for VGS voltage

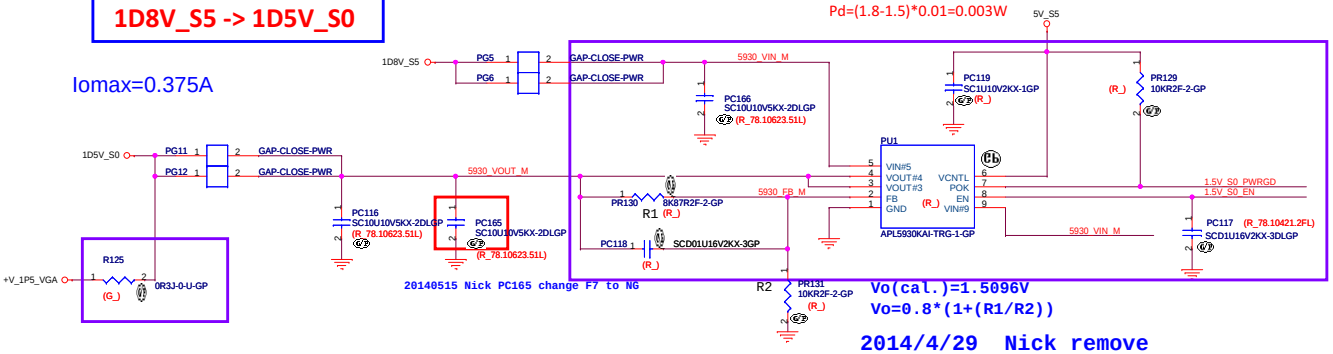


2014/4/29 Nick change R718 to (NG) for change sequence

1D8V_S5 -> 1D5V_S0

Pd=(1.8-1.5)*0.01=0.003W

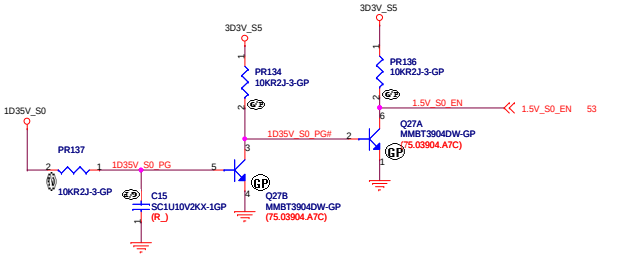
Iomax=0.375A



20140515 Nick PC165 change F7 to NG

Vo(cal.)=1.5096V
Vo=0.8*(1+(R1/R2))

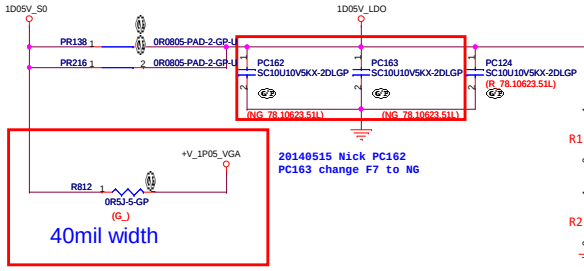
2014/4/29 Nick remove PU1 for change sequence



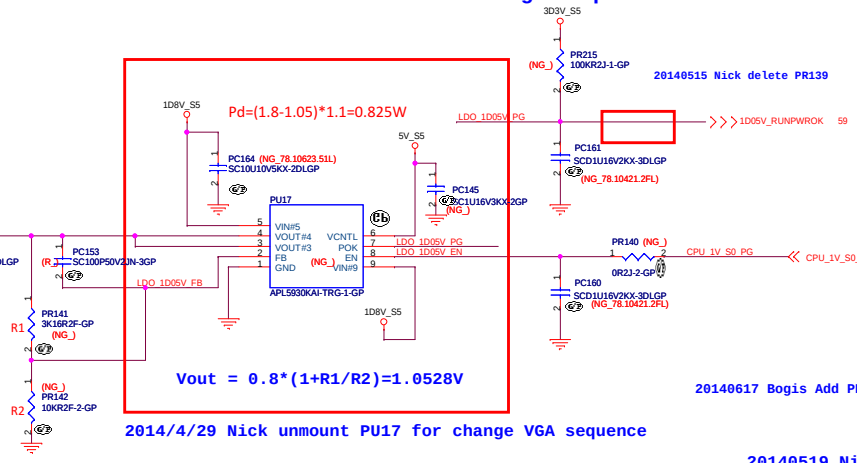
1D8V_S5 -> 1D05V_S0

V1P05_S0

Iomax=1.1A

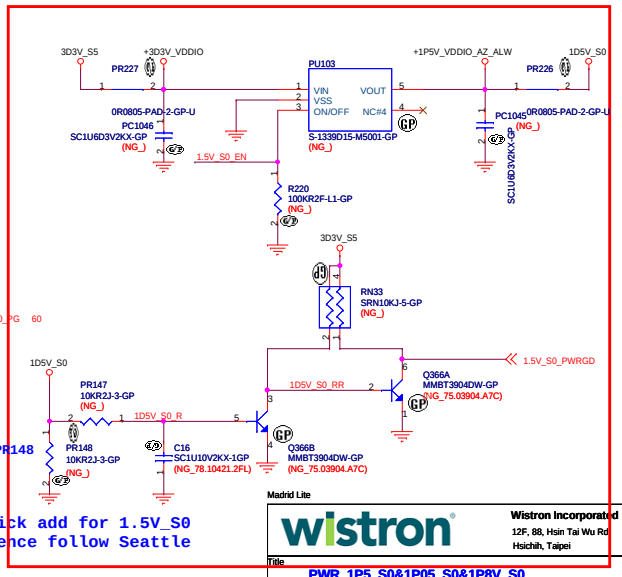


20140515 Nick PC162 PC163 change F7 to NG



Vout = 0.8*(1+R1/R2)=1.0528V

2014/4/29 Nick unmount PU17 for change VGA sequence



20140617 Bogis Add PR148

2014/4/29 Nick mount R812 connect 1D05V_S0 and +V_1P05_VGA

20140519 Nick add for 1.5V_S0 power sequence follow Seattle

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Title: PWR_1P5_S0&1P05_S0&1P8V_S0

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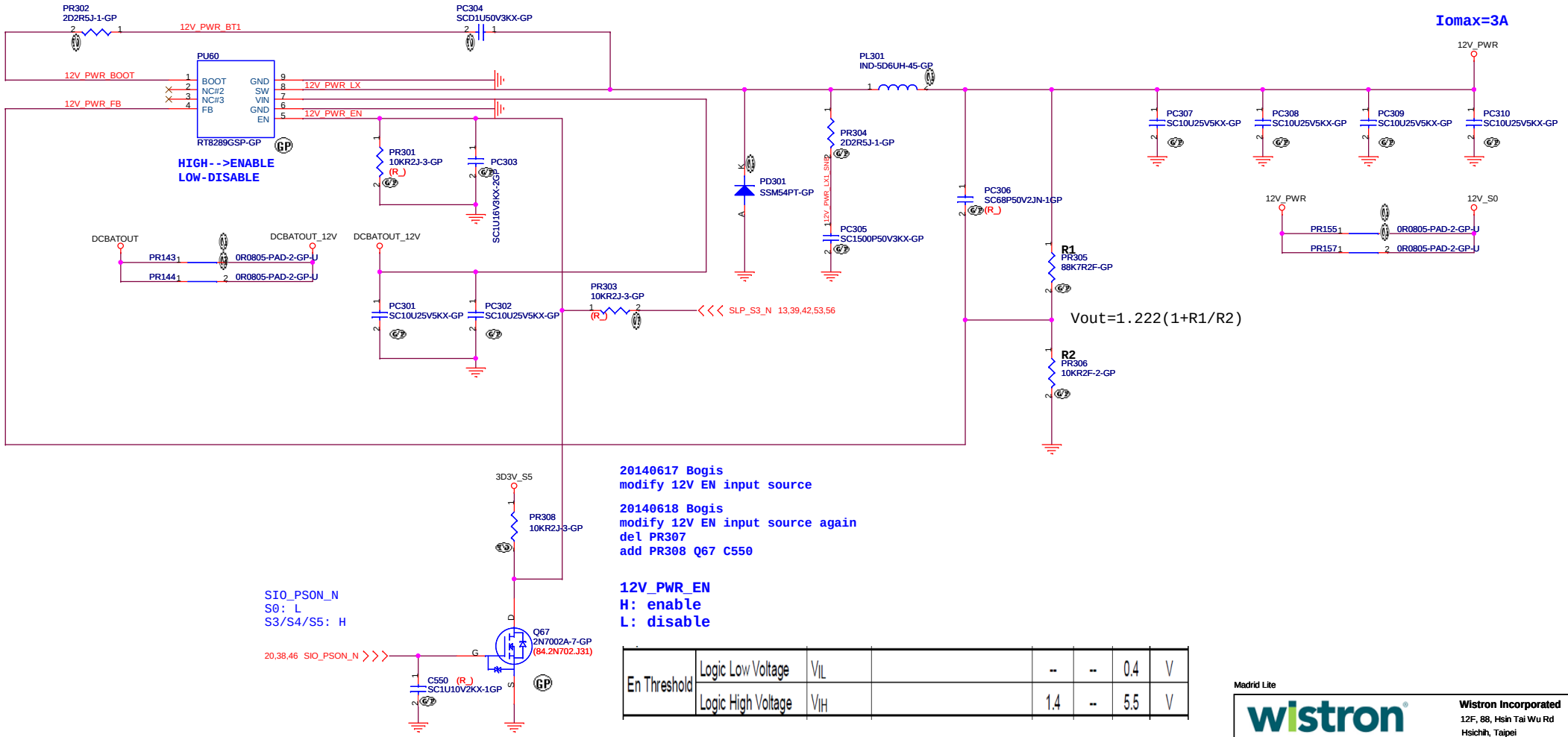

20140617 Bogis
modify 12V EN input source

20140618 Bogis
modify 12V EN input source again
del PR307
add PR308 Q67 C550

12V_PWR_EN
H: enable
L: disable

En Threshold	Logic Low Voltage	V_{IL}		--	--	0.4	V
	Logic High Voltage	V_{IH}		1.4	--	5.5	V

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