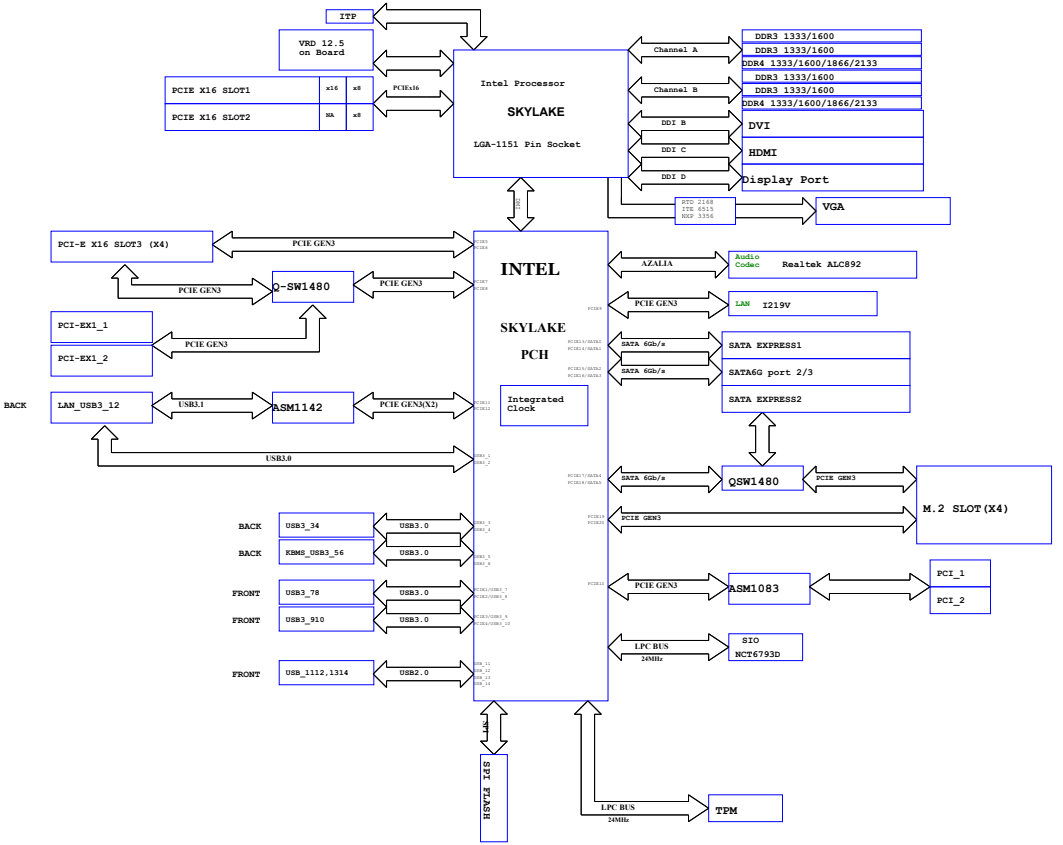
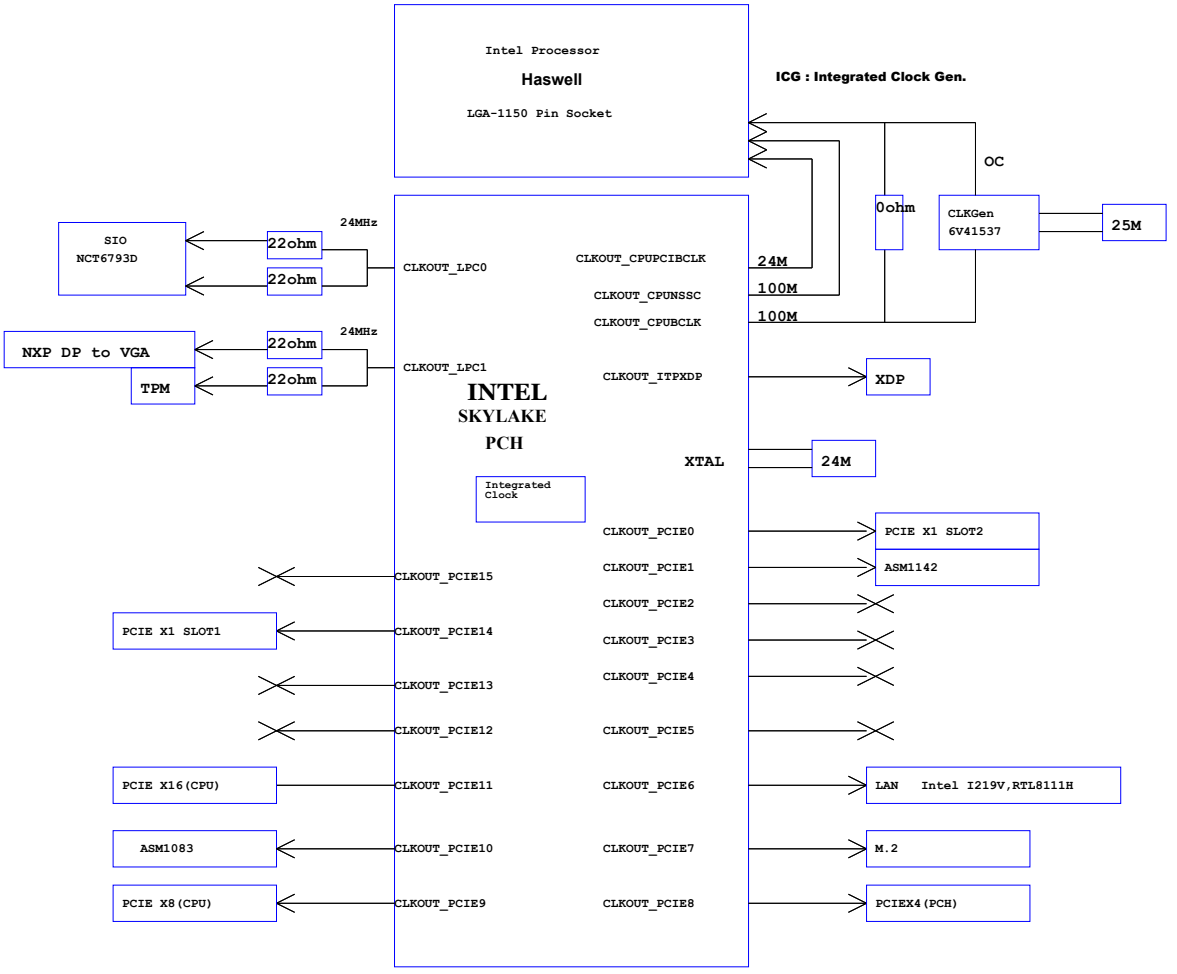
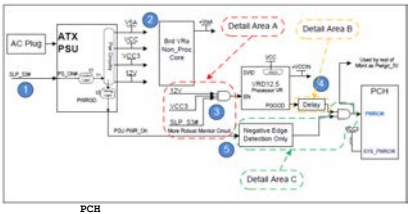
H170M-PLUS

Rev 1.04




Intel Processor
Haswell
LGA-1150 Pin Socket
ICG : Integrated Clock Gen.
OC
0ohm
CLKGen
6V41537
25M
SIO
NCT6793D
22ohm
22ohm
24MHz
CLKOUT_LPC0
NXP DP to VGA
TPM
22ohm
22ohm
24MHz
CLKOUT_LPC1
CLKOUT_CPUPCIBCLK
CLKOUT_CPUNSSC
CLKOUT_CPUBCLK
24M
100M
100M
CLKOUT_ITPXDP
XDP
INTEL
SKYLAKE
PCH
XTAL
24M
Integrated
Clock
CLKOUT_PCIE0
CLKOUT_PCIE1
CLKOUT_PCIE2
CLKOUT_PCIE3
CLKOUT_PCIE4
CLKOUT_PCIE5
CLKOUT_PCIE6
CLKOUT_PCIE7
CLKOUT_PCIE8
PCIE X1 SLOT2
ASM1142
CLKOUT_PCIE15
PCIE X1 SLOT1
CLKOUT_PCIE14
CLKOUT_PCIE13
CLKOUT_PCIE12
PCIE X16(CPU)
CLKOUT_PCIE11
ASM1083
CLKOUT_PCIE10
PCIE X8(CPU)
CLKOUT_PCIE9
LAN Intel I219V,RTL8111H
M.2
PCIEX4(PCH)



PCI_Express x 16_1 — PWRGD — <19>O_PCIRST#_PCIEX16_1
PCI_Express x 16_2 — PWRGD — <19>O_PCIRST#_PCIEX16_2
PCI_Express x 1_1,2 & x16_3 — PWRGD — <19>O_PCIRST#_PCIEX16_3

POWER_SWITCH: PWRBTN, PWRIN — <5>O_PWRBTN#IN

SIO NCT6779D: PS_IN#, PSON# *1, ATXPGD *2, PWROK, PCIRST1#, PCIRST2#, PCIRST3#, LRESET#, KBRST#, RSMRST#, PS_OUT#, SUSC#, SUSB#

POWER SUPPLY: Main PWR, VSB, PSON#, PWROK
<10>12V,5V,3V
<3>+5VSB, +3VSB
<9>O_PSON#
<11>B_ATX_PWROK
<2>AC Power Switch On

<18>S_PLTRST# *8
O_KB_RST#
<4>O_RSMRST#
<6>O_PWRBTN#
<4.1> / <8>S_SLPS4#
<4.2> / <9>S_SLPS3#
<7>S_SLP_A#
<7.1>S_SLP_LAN#
<12>O_PWROK

PCH LYNX POINT: HDA_RST#, PLTRST#, PLTRST_PROC#, RCIN#, RSMRST#, PWRBTN#, SLP_S5#, SLP_S4# *4, SLP_S3# *3, SLP_A# *3, SLP_LAN#, SYS_PWROK, PCH_PWROK, DRAMPWROK, RTCRST#, SRTCRST#, PROCPUPWRGD, DPWROK, MEPWROK

AZ_RST# → RESET# AUDIO ALC898

SYS_RESET# *9
<18>H_CPURST# *5
<13>S_DRAMPWRGD *5
<1>RTCRST#
<1>SRTCRST#
BATTERY
*7 <14>H_CPUPWRGD
<3.1>S_DPWROK
Non-AMT
AMT

RESET_SWITCH: SYS_RESET#
XDP: SYS_RESET#, H_CPURST#, DBR#, RESET#, OBSDATA

PROCESSOR HASWELL: DBR#, RESET#, SM_DRAMPWROK, CFG, PWRGOOD, SVID, VCORE
<15>VRM_SVID
<16>VCORE

ME_POWER: +1.05ME, +3V_DUAL_LAN/EPW
<7.2>S_MEPWROK

Vcore Controller ISL95818: SVID, VCORE, VR_ON, PGOOD
*6 S_SLPS3#
+12V
+3V
<17>VRMPWRGD

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

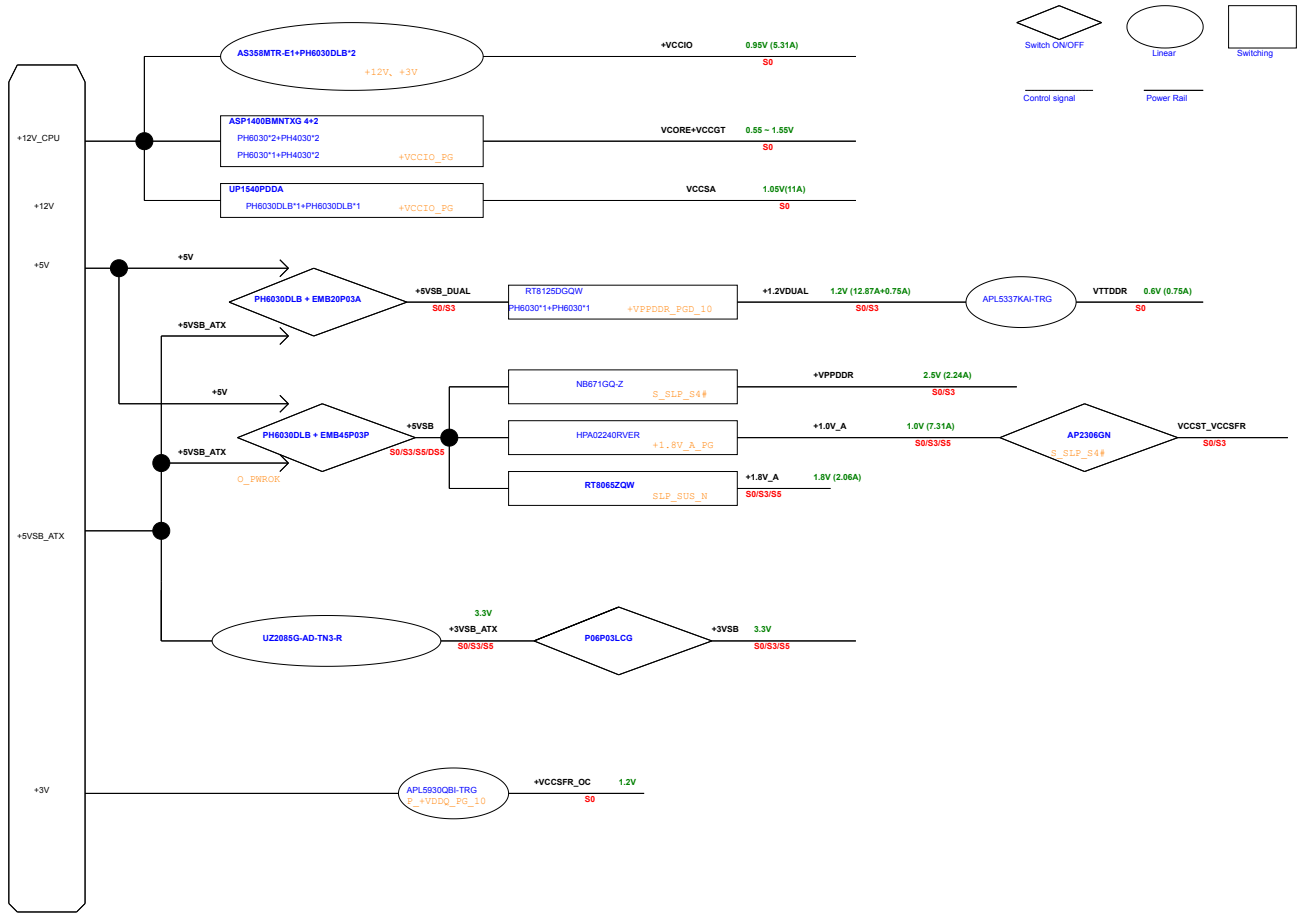
*6 Come with +3V,+12V and gated by SLP_S3#

*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK AND PCH SYS_PWROK

*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

CHIP — SOCKET or SLOT


Switch ON/OFF
Linear
Switching
Control signal
Power Rail
+12V_CPU
+12V
+5V
+5VSB_ATX
+3V
AS358MTR-E1+PH6030DLB*2
+12V, +3V
+VCCIO
0.95V (5.31A)
S0
ASP1400BMNTXG 4+2
PH6030*2+PH4030*2
PH6030*1+PH4030*2
+VCCIO_PG
+VCORE+VCCGT
0.55 ~ 1.55V
S0
UP1540PDDA
PH6030DLB*1+PH6030DLB*1
+VCCIO_PG
VCCSA
1.05V(11A)
S0
+5V
PH6030DLB + EMB20P03A
+5VSB_DUAL
S0/S3
RT8125DGQW
PH6030*1+PH6030*1
+VPPDDR_PGD_10
+1.2VDUAL
1.2V (12.87A+0.75A)
S0/S3
APL5337KAI-TRG
VTTDDR
0.6V (0.75A)
S0
+5VSB_ATX
+5V
PH6030DLB + EMB45P03P
+5VSB
S0/S3/S5/DS5
+5VSB_ATX
O_PWROK
NB671GQ-Z
S_SLP_S4#
+VPPDDR
2.5V (2.24A)
S0/S3
HPA02240RVER
+1.8V_A_PG
+1.0V_A
1.0V (7.31A)
S0/S3/S5
AP2306GN
S_SLP_S4#
VCCST_VCCSFR
S0/S3
RT8065ZQW
SLP_SUS_N
+1.8V_A
1.8V (2.06A)
S0/S3/S5
UZ2085G-AD-TN3-R
3.3V
+3VSB_ATX
S0/S3/S5
P06P03LCG
+3VSB
3.3V
S0/S3/S5
APL5930QBI-TRG
S_+VDDQ_PG_10
+VCCSFR_OC
1.2V
S0


LGA1151C
LGA1151
H_X16_SL1_RXP0
H_X16_SL1_RXN0
H_X16_SL1_RXP1
H_X16_SL1_RXN1
H_X16_SL1_RXP2
H_X16_SL1_RXN2
H_X16_SL1_RXP3
H_X16_SL1_RXN3
H_X16_SL1_RXP4
H_X16_SL1_RXN4
H_X16_SL1_RXP5
H_X16_SL1_RXN5
H_X16_SL1_RXP6
H_X16_SL1_RXN6
H_X16_SL1_RXP7
H_X16_SL1_RXN7
H_X16_SL1_RXP8
H_X16_SL1_RXN8
H_X16_SL1_RXP9
H_X16_SL1_RXN9
H_X16_SL1_RXP10
H_X16_SL1_RXN10
H_X16_SL1_RXP11
H_X16_SL1_RXN11
H_X16_SL1_RXP12
H_X16_SL1_RXN12
H_X16_SL1_RXP13
H_X16_SL1_RXN13
H_X16_SL1_RXP14
H_X16_SL1_RXN14
H_X16_SL1_RXP15
H_X16_SL1_RXN15
B8
B7
C7
C6
D6
D5
E5
E4
F6
F5
G5
G4
H6
H5
J5
J4
K6
K5
L5
L4
M6
M5
N5
N4
P6
P5
R5
R4
T6
T5
U5
U4
PEG_RXP[0]
PEG_RXN[0]
PEG_RXP[1]
PEG_RXN[1]
PEG_RXP[2]
PEG_RXN[2]
PEG_RXP[3]
PEG_RXN[3]
PEG_RXP[4]
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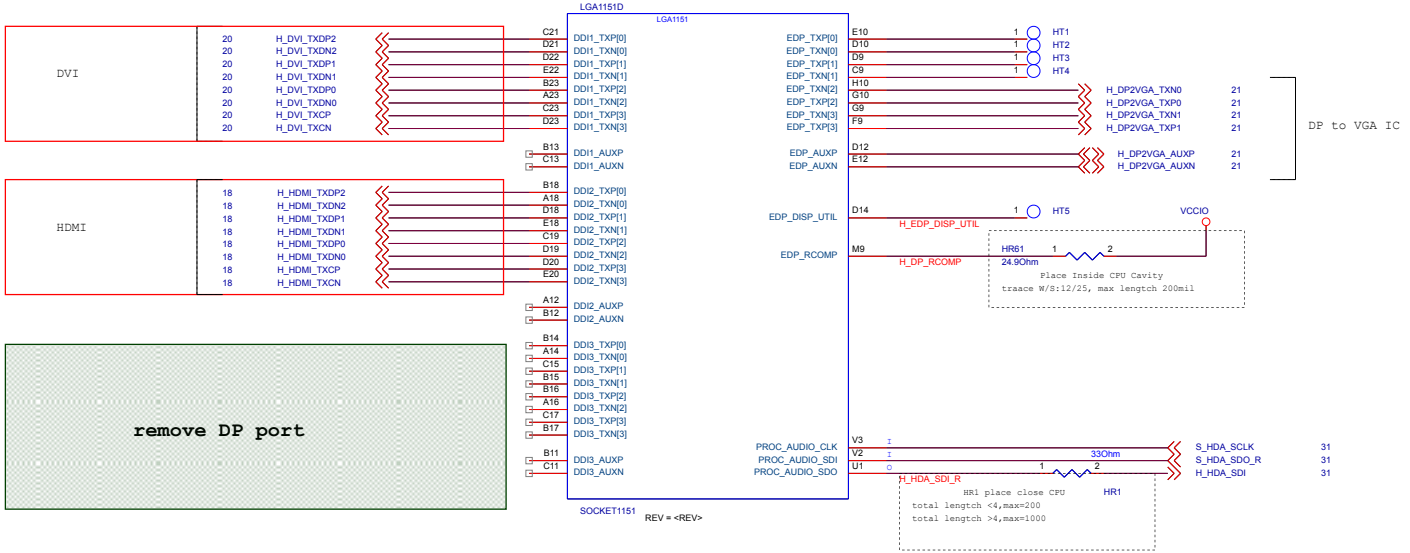
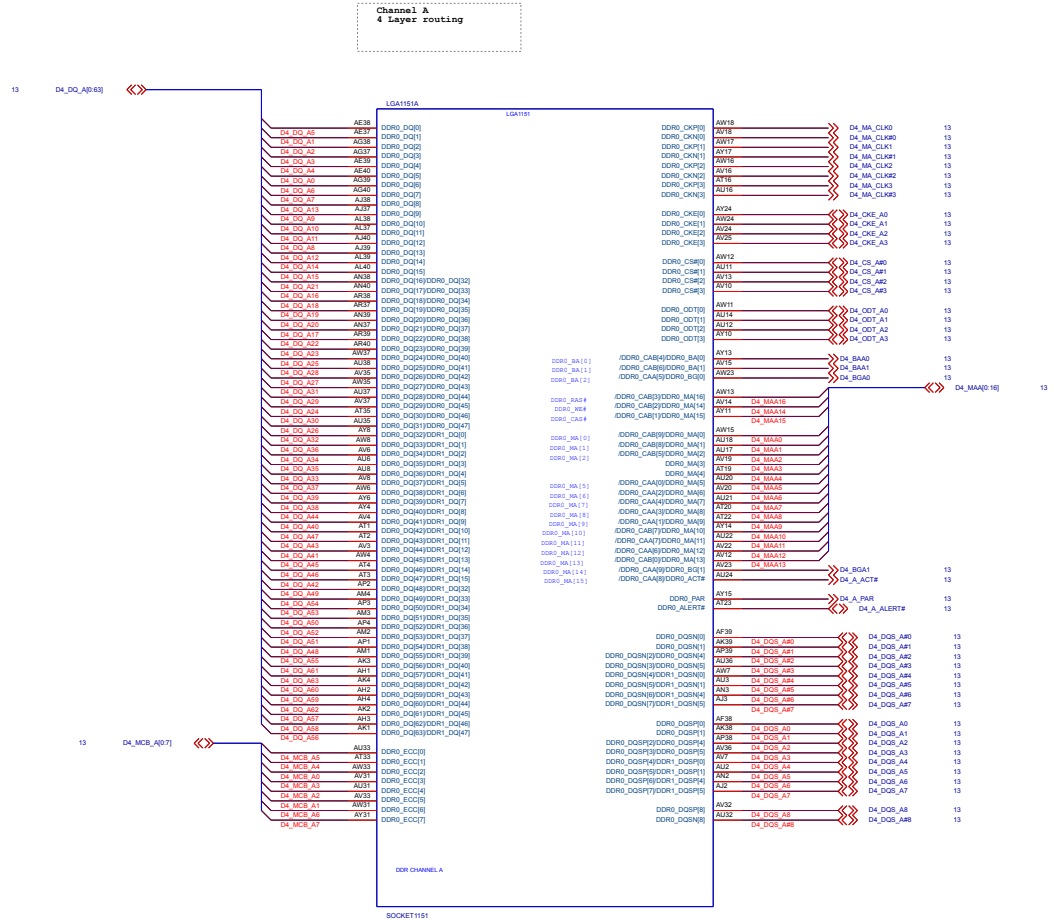
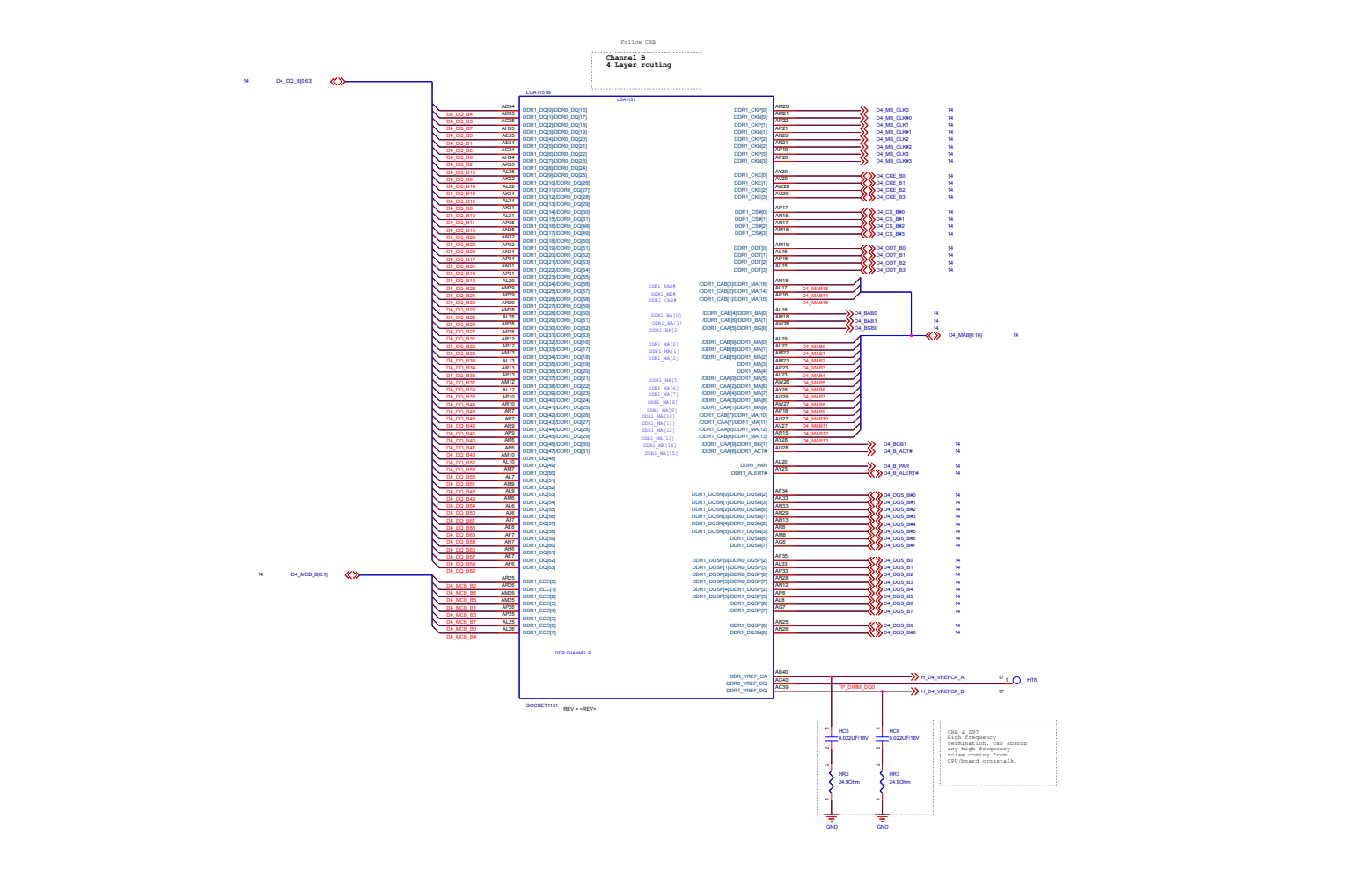
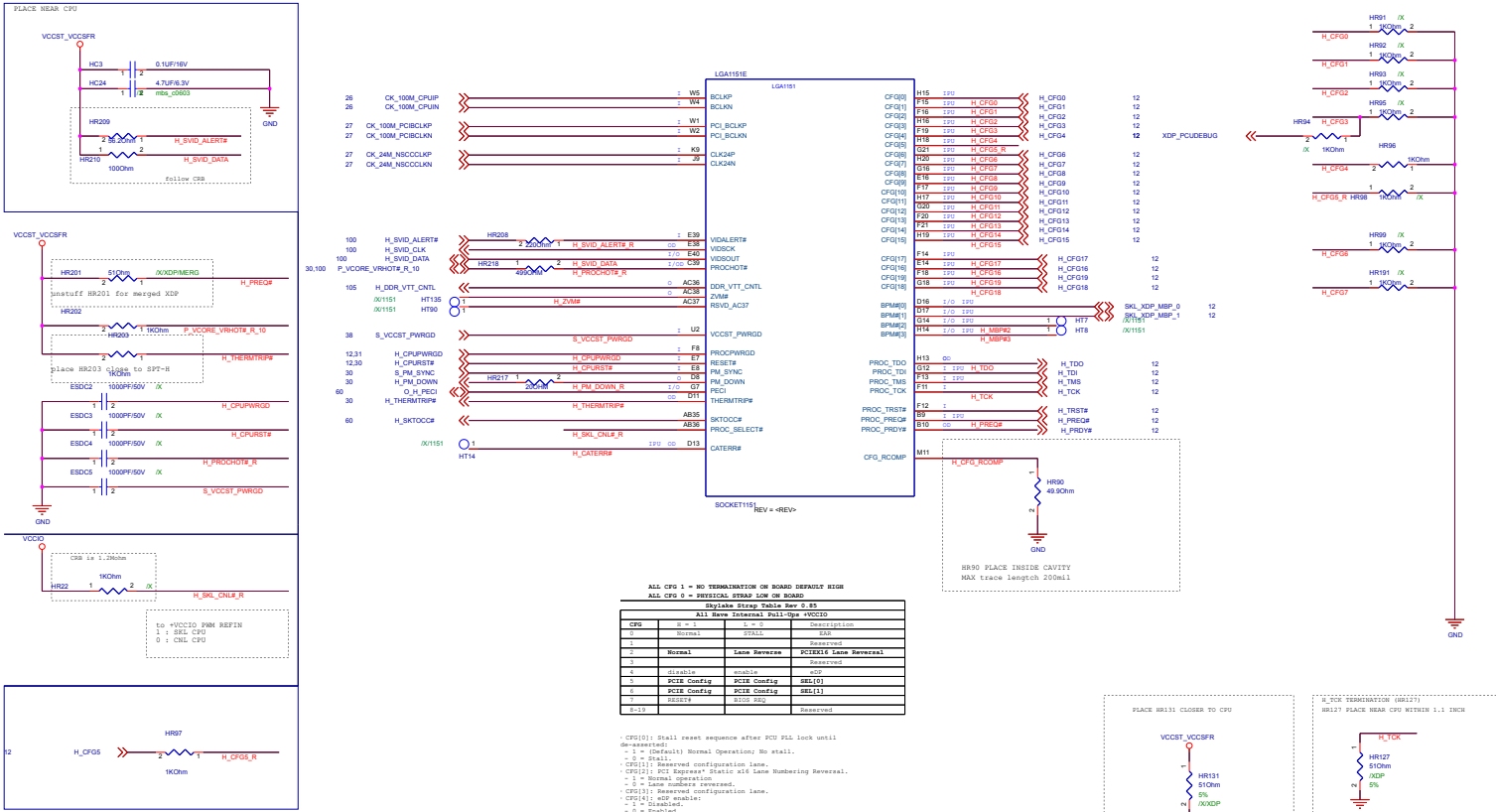
PEG_TXN[11]
PEG_TXP[12]
PEG_TXN[12]
PEG_TXP[13]
PEG_TXN[13]
PEG_TXP[14]
PEG_TXN[14]
PEG_TXP[15]
PEG_TXN[15]
A5
A6
B4
B5
C3
C4
D2
D3
E1
E2
F2
F3
G1
G2
H2
H3
J1
J2
K2
K3
L1
L2
M2
M3
N1
N2
P2
P3
R2
R1
T2
T3
H_X16_SL1_TXP0
H_X16_SL1_TXN0
H_X16_SL1_TXP1
H_X16_SL1_TXN1
H_X16_SL1_TXP2
H_X16_SL1_TXN2
H_X16_SL1_TXP3
H_X16_SL1_TXN3
H_X16_SL1_TXP4
H_X16_SL1_TXN4
H_X16_SL1_TXP5
H_X16_SL1_TXN5
H_X16_SL1_TXP6
H_X16_SL1_TXN6
H_X16_SL1_TXP7
H_X16_SL1_TXN7
H_X16_SL1_TXP8
H_X16_SL1_TXN8
H_X16_SL1_TXP9
H_X16_SL1_TXN9
H_X16_SL1_TXP10
H_X16_SL1_TXN10
H_X16_SL1_TXP11
H_X16_SL1_TXN11
H_X16_SL1_TXP12
H_X16_SL1_TXN12
H_X16_SL1_TXP13
H_X16_SL1_TXN13
H_X16_SL1_TXP14
H_X16_SL1_TXN14
H_X16_SL1_TXP15
H_X16_SL1_TXN15
VCCIO
HR52
1
2
24.9Ohm
H_PEG_RCOMP
PLACE HR52 Inside CPU Cavity
Trace W/S: 12/15 mils, Length: 400mils
L7
PEG_RCOMP
Y3
Y4
AA4
AA5
AB4
AB3
AC4
AC5
DMI_RXP[0]
DMI_RXN[0]
DMI_RXP[1]
DMI_RXN[1]
DMI_RXP[2]
DMI_RXN[2]
DMI_RXP[3]
DMI_RXN[3]
DMI_TXP[0]
DMI_TXN[0]
DMI_TXP[1]
DMI_TXN[1]
DMI_TXP[2]
DMI_TXN[2]
DMI_TXP[3]
DMI_TXN[3]
AC2
AC1
AD3
AD2
AE2
AE1
AF2
AF3
H_DMI_RXP0
H_DMI_RXN0
H_DMI_RXP1
H_DMI_RXN1
H_DMI_RXP2
H_DMI_RXN2
H_DMI_RXP3
H_DMI_RXN3
H_DMI_TXP0
H_DMI_TXN0
H_DMI_TXP1
H_DMI_TXN1
H_DMI_TXP2
H_DMI_TXN2
H_DMI_TXP3
H_DMI_TXN3
SOCKET1151
REV = <REV>


LGA1151D
LGA1151
DVI
20 H_DVI_TXDP2
20 H_DVI_TXDN2
20 H_DVI_TXDP1
20 H_DVI_TXDN1
20 H_DVI_TXDP0
20 H_DVI_TXDN0
20 H_DVI_TXCP
20 H_DVI_TXCN
C21 DDI1_TXP[0]
D21 DDI1_TXN[0]
D22 DDI1_TXP[1]
E22 DDI1_TXN[1]
B23 DDI1_TXP[2]
A23 DDI1_TXN[2]
C23 DDI1_TXP[3]
D23 DDI1_TXN[3]
B13 DDI1_AUXP
C13 DDI1_AUXN
HDMI
18 H_HDMI_TXDP2
18 H_HDMI_TXDN2
18 H_HDMI_TXDP1
18 H_HDMI_TXDN1
18 H_HDMI_TXDP0
18 H_HDMI_TXDN0
18 H_HDMI_TXCP
18 H_HDMI_TXCN
B18 DDI2_TXP[0]
A18 DDI2_TXN[0]
D18 DDI2_TXP[1]
E18 DDI2_TXN[1]
C19 DDI2_TXP[2]
D19 DDI2_TXN[2]
D20 DDI2_TXP[3]
E20 DDI2_TXN[3]
A12 DDI2_AUXP
B12 DDI2_AUXN
remove DP port
B14 DDI3_TXP[0]
A14 DDI3_TXN[0]
C15 DDI3_TXP[1]
B15 DDI3_TXN[1]
B16 DDI3_TXP[2]
A16 DDI3_TXN[2]
C17 DDI3_TXP[3]
B17 DDI3_TXN[3]
B11 DDI3_AUXP
C11 DDI3_AUXN
SOCKET1151
REV = <REV>
EDP_TXP[0]
EDP_TXN[0]
EDP_TXP[1]
EDP_TXN[1]
EDP_TXP[2]
EDP_TXN[2]
EDP_TXP[3]
EDP_TXN[3]
EDP_AUXP
EDP_AUXN
EDP_DISP_UTIL
EDP_RCOMP
PROC_AUDIO_CLK
PROC_AUDIO_SDI
PROC_AUDIO_SDO
E10 1 HT1
D10 1 HT2
D9 1 HT3
C9 1 HT4
H10 H_DP2VGA_TXN0 21
G10 H_DP2VGA_TXP0 21
G9 H_DP2VGA_TXN1 21
F9 H_DP2VGA_TXP1 21
D12 H_DP2VGA_AUXP 21
E12 H_DP2VGA_AUXN 21
DP to VGA IC
D14 1 HT5 VCCIO
H_EDP_DISP_UTIL
M9 H_DP_RCOMP
HR61 1 2
24.9Ohm
Place Inside CPU Cavity
traace W/S:12/25, max lengtch 200mil
V3 S_HDA_SCLK 31
V2 33Ohm S_HDA_SDO_R 31
U1 1 2 H_HDA_SDI 31
H_HDA_SDI_R
HR1 place close CPU
HR1
total lengtch <4,max=200
total lengtch >4,max=1000


Channel A
4 Layer routing
13
D4_DQ_A[0:63]
LGA1151A
LGA1151
AE38
AE37
AG38
AG37
AE39
AE40
AG39
AG40
AJ38
AJ37
AL38
AL37
AJ40
AJ39
AL39
AL40
AN38
AN40
AR38
AR37
AN39
AN37
AR39
AR40
AW37
AU38
AV38
AW35
AU37
AV37
AT35
AU35
AY8
AW8
AV8
AU8
AU9
AV9
AW6
AY6
AY4
AV4
AT1
AT2
AV3
AW4
AT4
AT3
AP2
AM6
AP3
AM3
AP4
AM2
AP1
AM1
AK3
AH1
AK4
AH2
AH4
AK2
AH3
AK1
DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]
13
D4_MCB_A[0:7]
AU33
AT33
AW33
AV31
AU31
AV33
AW31
AY31
D4_MCB_A5
D4_MCB_A4
D4_MCB_A0
D4_MCB_A3
D4_MCB_A2
D4_MCB_A1
D4_MCB_A6
D4_MCB_A7
DDR0_ECC[0]
DDR0_ECC[1]
DDR0_ECC[2]
DDR0_ECC[3]
DDR0_ECC[4]
DDR0_ECC[5]
DDR0_ECC[6]
DDR0_ECC[7]
DDR CHANNEL A
SOCKET1151
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
DDR0_BA[0]
DDR0_BA[1]
DDR0_BA[2]
DDR0_RAS#
DDR0_WE#
DDR0_CAS#
DDR0_MA[0]
DDR0_MA[1]
DDR0_MA[2]
DDR0_MA[5]
DDR0_MA[6]
DDR0_MA[7]
DDR0_MA[8]
DDR0_MA[9]
DDR0_MA[10]
DDR0_MA[11]
DDR0_MA[12]
DDR0_MA[13]
DDR0_MA[14]
DDR0_MA[15]
/DDR0_CAB4)/DDR0_BA(0)
/DDR0_CAB6)/DDR0_BA(1)
/DDR0_CAA(5)/DDR0_BG(0)
/DDR0_CAB3)/DDR0_MA(16)
/DDR0_CAB2)/DDR0_MA(14)
/DDR0_CAB1)/DDR0_MA(15)
/DDR0_CAB9)/DDR0_MA(0)
/DDR0_CAB8)/DDR0_MA(1)
/DDR0_CAB5)/DDR0_MA(2)
DDR0_MA(3)
DDR0_MA(4)
/DDR0_CAA(9)/DDR0_MA(5)
/DDR0_CAA(2)/DDR0_MA(6)
/DDR0_CAA(4)/DDR0_MA(7)
/DDR0_CAA(3)/DDR0_MA(8)
/DDR0_CAA(1)/DDR0_MA(9)
/DDR0_CAB(7)/DDR0_MA(10)
/DDR0_CAA(7)/DDR0_MA(11)
/DDR0_CAA(8)/DDR0_MA(12)
/DDR0_CAB(0)/DDR0_MA(13)
/DDR0_CAA(9)/DDR0_BG(1)
/DDR0_CAA(6)/DDR0_ACT#
DDR0_PAR
DDR0_ALERT#
DDR0_DQSN[0]
DDR0_DQSN[1]
DDR0_DQSN[2]/DDR0_DQSN[4]
DDR0_DQSN[3]/DDR0_DQSN[5]
DDR0_DQSN[4]/DDR1_DQSN[0]
DDR0_DQSN[5]/DDR1_DQSN[1]
DDR0_DQSN[6]/DDR1_DQSN[4]
DDR0_DQSN[7]/DDR1_DQSN[5]
DDR0_DQSP[0]
DDR0_DQSP[1]
DDR0_DQSP[2]/DDR0_DQSP[4]
DDR0_DQSP[3]/DDR0_DQSP[5]
DDR0_DQSP[4]/DDR1_DQSP[0]
DDR0_DQSP[5]/DDR1_DQSP[1]
DDR0_DQSP[6]/DDR1_DQSP[4]
DDR0_DQSP[7]/DDR1_DQSP[5]
DDR0_DQSP[8]
DDR0_DQSN[8]
AW18
AV18
AW17
AV17
AW16
AV16
AT16
AU16
AY24
AW24
AV24
AV25
AW12
AU11
AV13
AU10
AW11
AU14
AU12
AV10
AY13
AV15
AW23
AW13
AU14
AY11
AY15
AU18
AU17
AV19
AT19
AU20
AV20
AU21
AT20
AT22
AY14
AU22
AV22
AY12
AW23
AU24
AY15
AT23
AF39
AK39
AF38
AU36
AW7
AU3
AN3
AJ3
AF38
AK38
AF38
AV36
AV7
AU2
AN2
AJ2
AV32
AU32
D4_CKE_A0
D4_CKE_A1
D4_CKE_A2
D4_CKE_A3
D4_CS_A#0
D4_CS_A#1
D4_CS_A#2
D4_CS_A#3
D4_ODT_A0
D4_ODT_A1
D4_ODT_A2
D4_ODT_A3
D4_BAA0
D4_BAA1
D4_BGA0
D4_MAA[0:16]
D4_MAA16
D4_MAA14
D4_MAA15
D4_MAA0
D4_MAA1
D4_MAA2
D4_MAA3
D4_MAA4
D4_MAA5
D4_MAA6
D4_MAA7
D4_MAA8
D4_MAA9
D4_MAA10
D4_MAA11
D4_MAA12
D4_MAA13
D4_BGA1
D4_A_ACT#
D4_A_PAR
D4_A_ALERT#
D4_DQS_A#0
D4_DQS_A#1
D4_DQS_A#2
D4_DQS_A#3
D4_DQS_A#4
D4_DQS_A#5
D4_DQS_A#6
D4_DQS_A#7
D4_DQS_A#8
D4_DQS_A0
D4_DQS_A1
D4_DQS_A2
D4_DQS_A3
D4_DQS_A4
D4_DQS_A5
D4_DQS_A6
D4_DQS_A7
D4_DQS_A8
13


Follow CRB
Channel B
4 Layer routing
LGA1151/B
LGA1151
14 D4_DQ_B[0:63]
14 D4_MCB_B[0:7]
DDR CHANNEL B
SOCKET1151 REV = <REV>
HC5 0.022UF/16V
HC6 0.022UF/16V
HR2 24.9Ohm
HR3 24.9Ohm
GND
GND
TP_DIMM_DQ0
CRB & Z97 High frequency termination, can absorb any high frequency noise coming from CPU/board crosstalk.

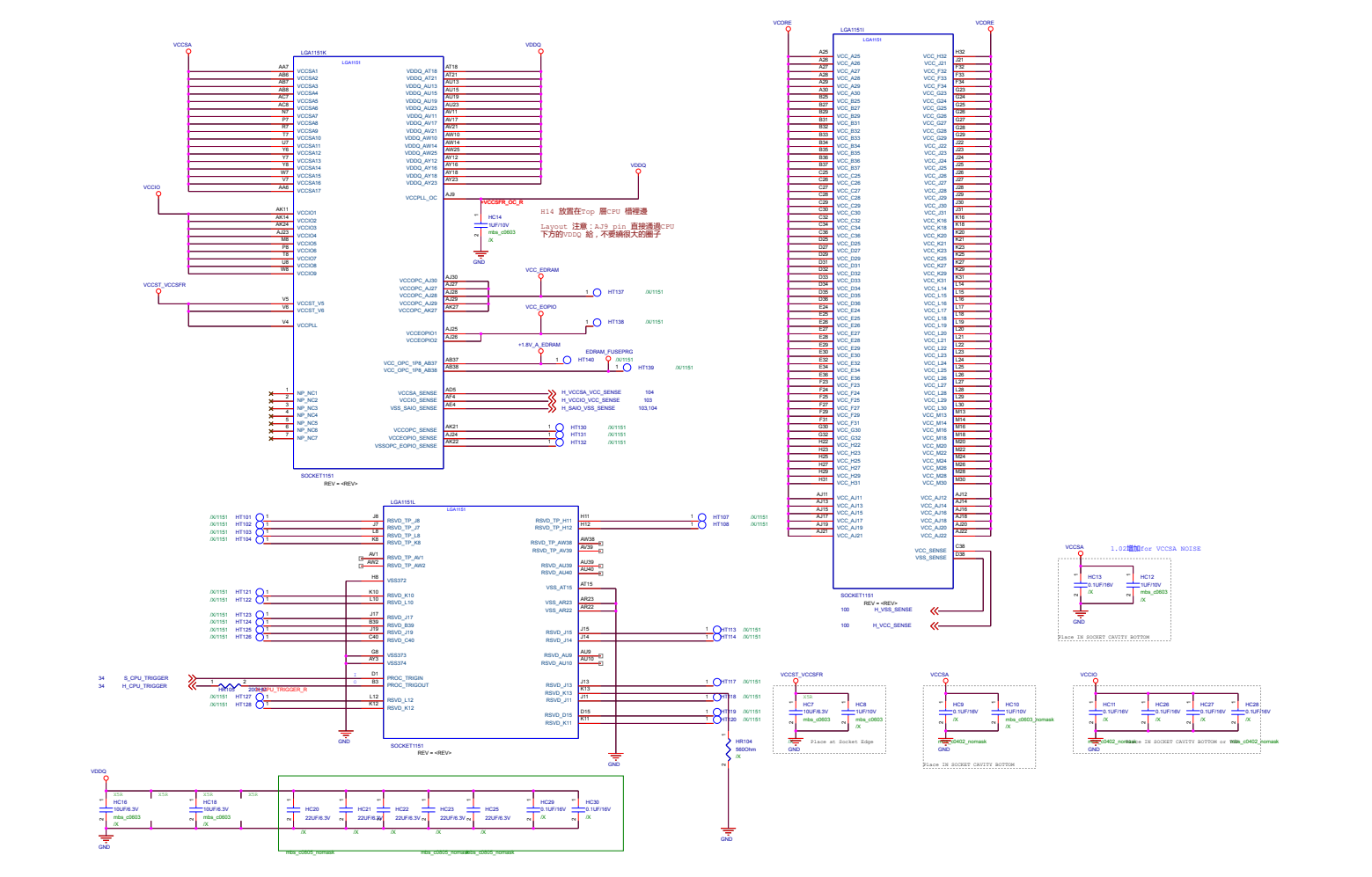


ALL CFG 1 = NO TERMINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD

Skylake Strap Table Rev 0.85

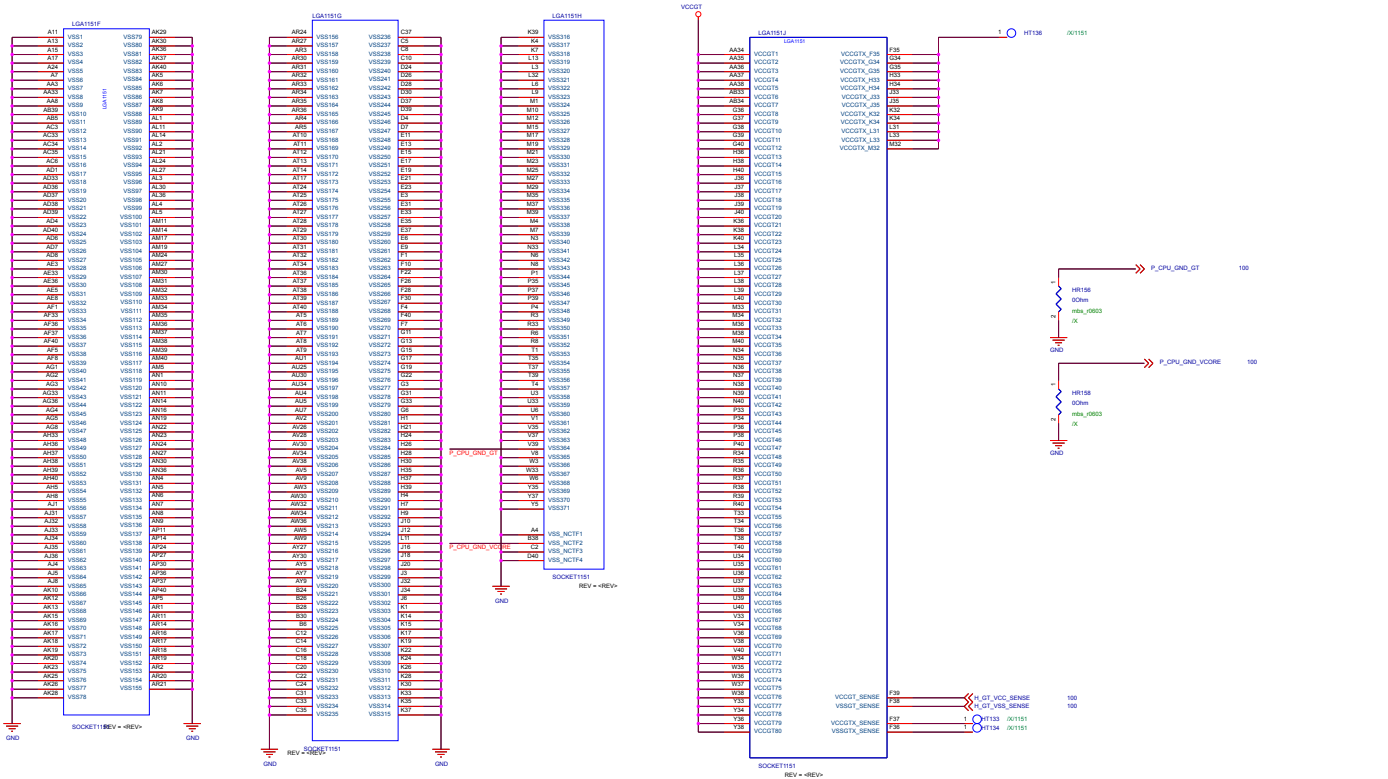
All Have Internal Pull-Ups +VCCIO			
CFG	H = 1	L = 0	Description
0	Normal	STALL	EAR
1			Reserved
2	**Normal**	**Lane Reverse**	**PCIEX16 Lane Reversal**
3			Reserved
4	disable	enable	eDP
5	**PCIE Config**	**PCIE Config**	**SEL[0]**
6	**PCIE Config**	**PCIE Config**	**SEL[1]**
7	RESET#	BIOS REQ	
8-19			Reserved

- CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- CFG[1]: Reserved configuration lane.
- CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- CFG[3]: Reserved configuration lane.
- CFG[4]: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- CFG[6:5]: PCI Express* Bifurcation
  - 00 = 1 x16 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- CFG[7]: PEG Training:
  - 1 = (default) PEGTrain immediately following RESET# de-assertion.
  - 0 = PEG Wait for BIOS for training.
- CFG[19:8]: Reserved configuration lanes.



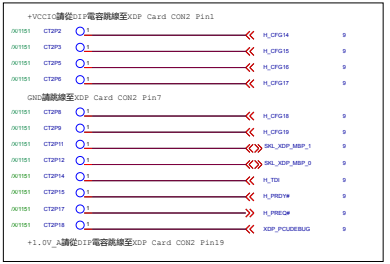
H14 放置在Top 层CPU 插座邊

Layout 注意：AJ9 pin 直接通過CPU 下方的VDDQ 給，不要繞很大的圈子


LGA1151F
LGA1151G
LGA1151H
LGA1151J
SOCKET1151
REV = <REV>
GND
VCCGT
P_CPU_GND_GT
P_CPU_GND_VCORE
HT136
HR156
HR158
0Ohm
mbs_r0603
/X
100
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
H_GT_VCC_SENSE
H_GT_VSS_SENSE
HT133
HT134
/X/1151
ILM1
ILM2

XDP Card USB3 CON1

XDP Card USB3 CON2



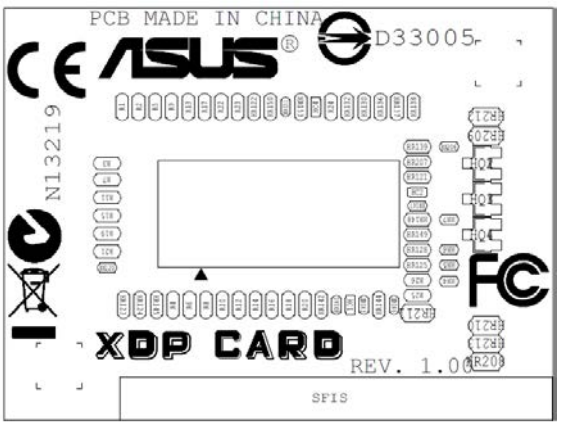
XDP Card USB3 CON3

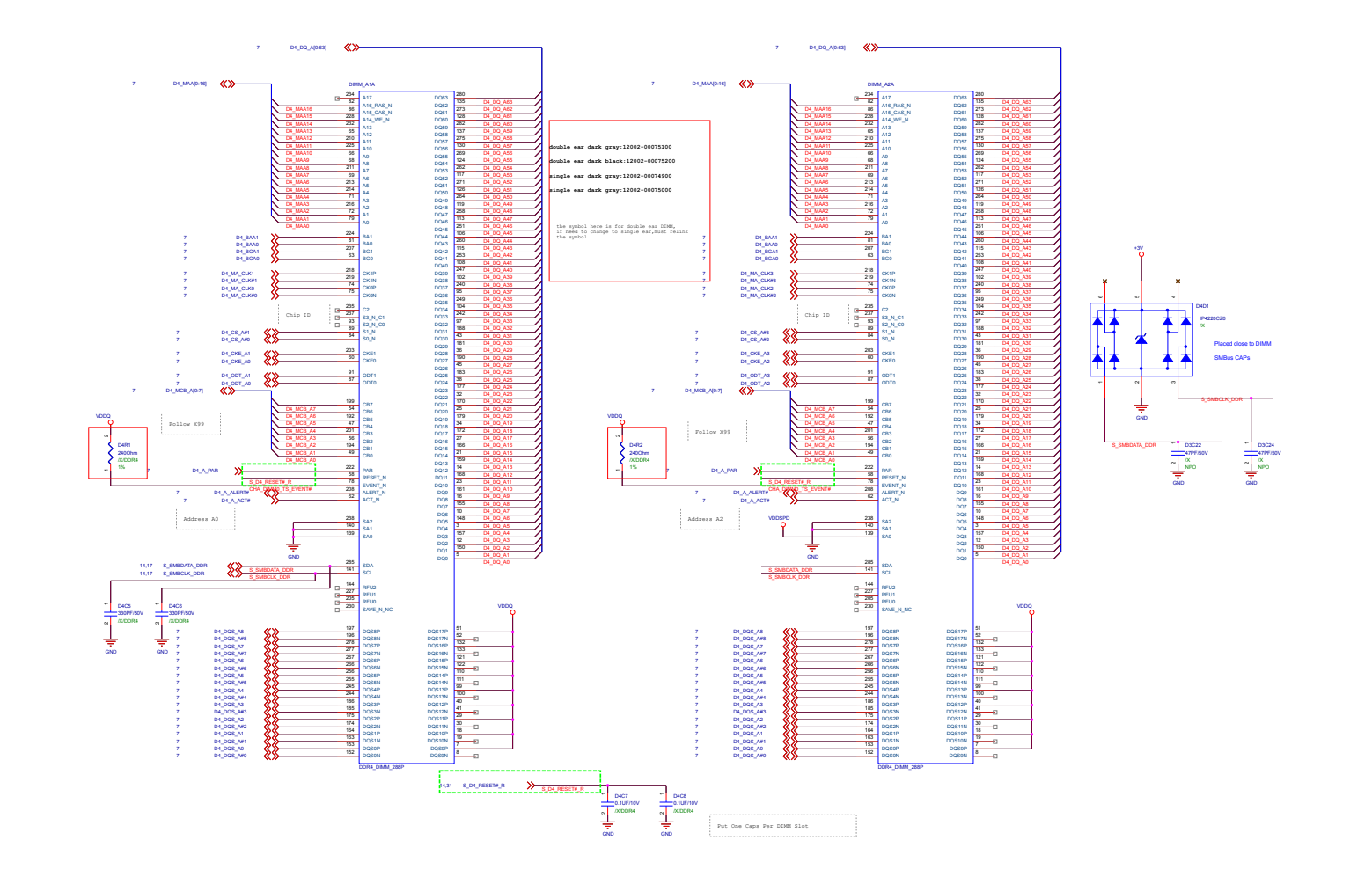
XDP Card USB3 CON4

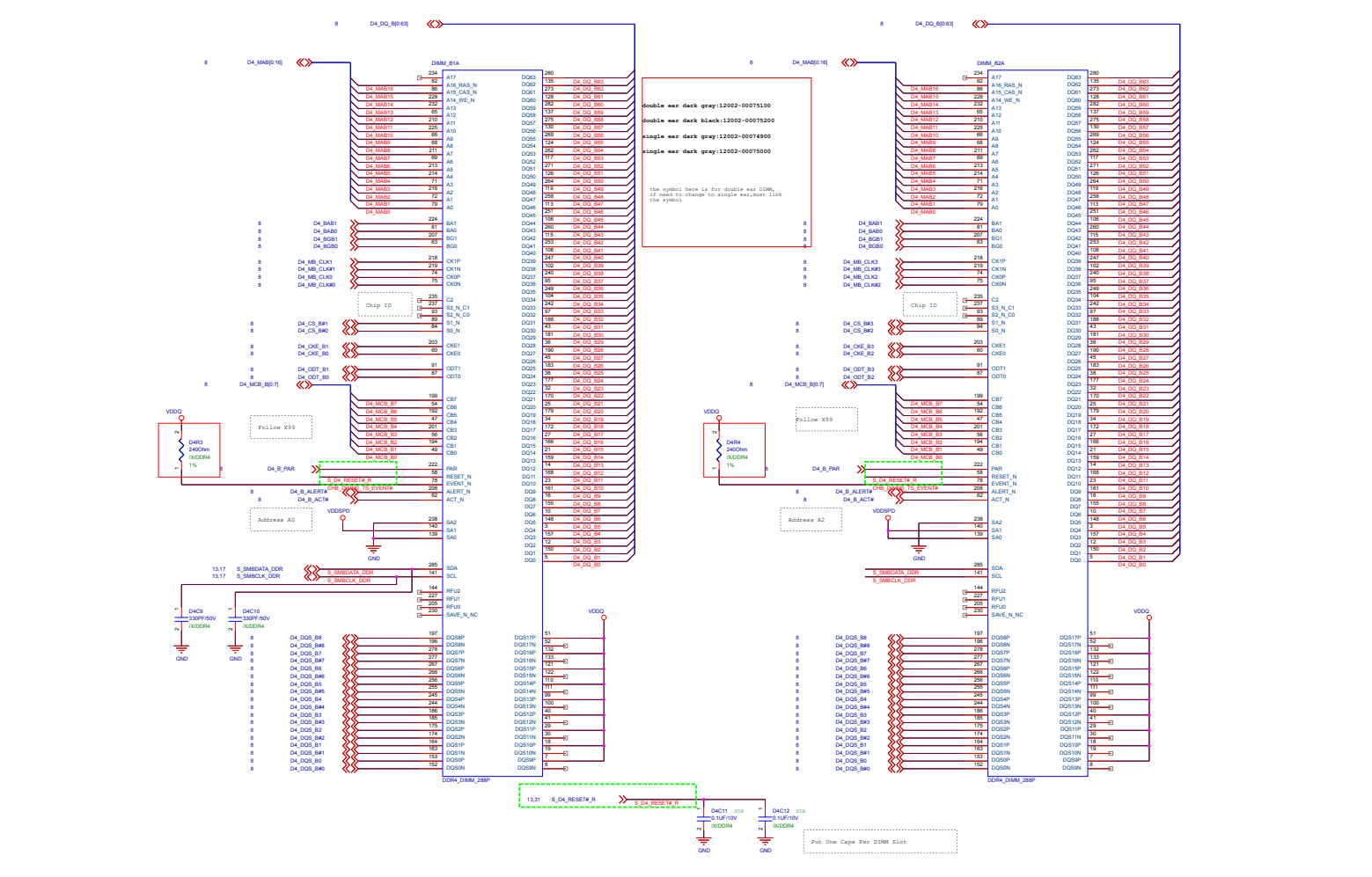
Naming Rule:
CTxPy==>請跳線到XDP Card CONx connector的Piny

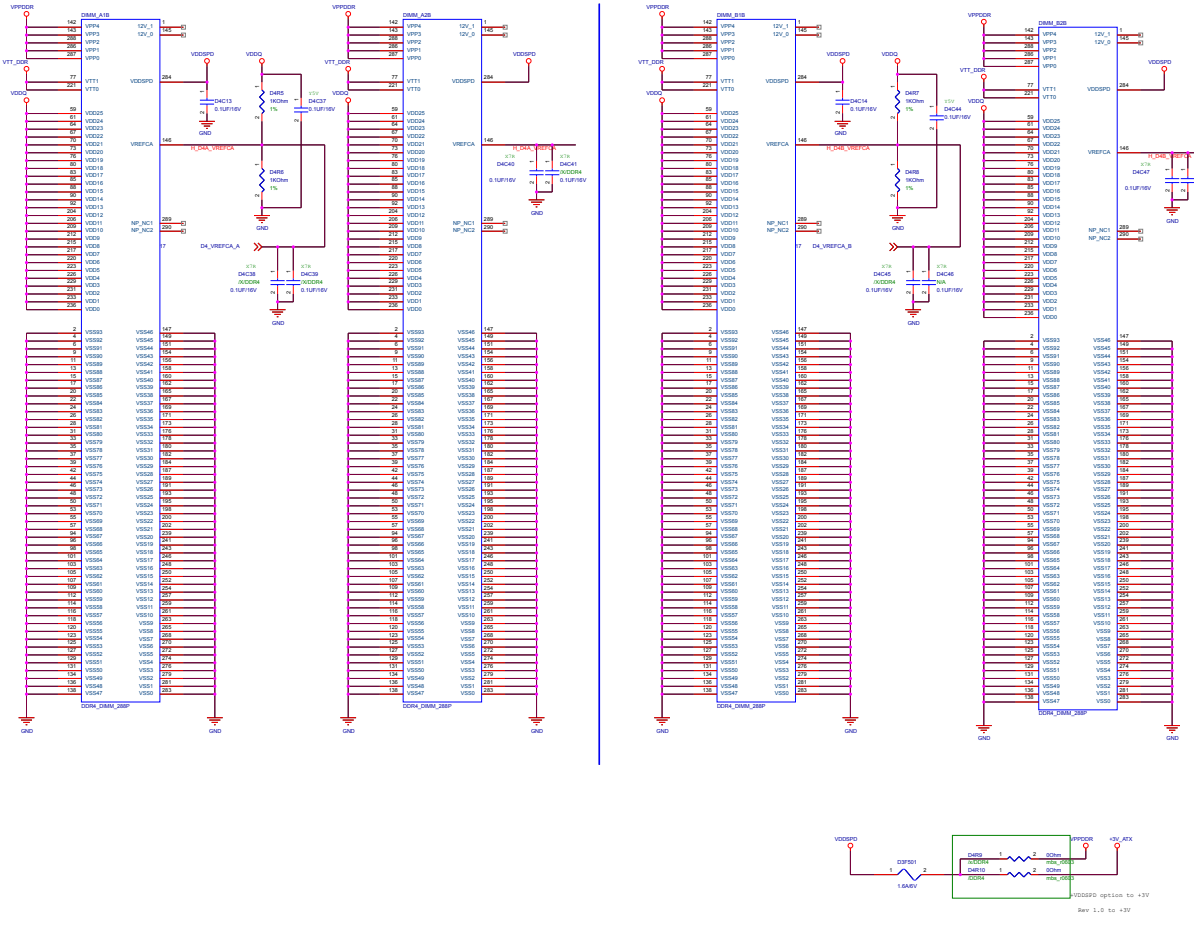
Placement Rule:
此頁面測點全部放置背面靠近輸出端，
Layout會協助把Reference文字面開出，
若有需求初期PCB版本可洗背面文字，
但低階機種PVT PCB版本請記得通知板廠不洗背面文字

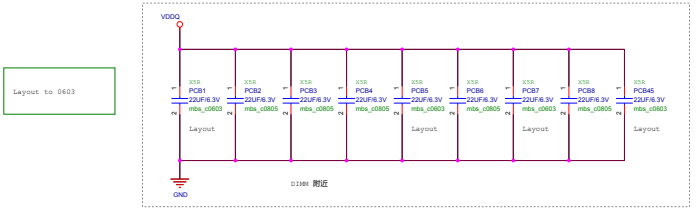
Power Rework:
+1.0V_A請從DIP電容跳線至XDP Card CON2 Pin19
+3VSB請從DIP電容跳線至XDP Card CON4 Pin1
+VCCST請從DIP電容跳線至XDP Card CON3 Pin19
+VCCIO請從DIP電容跳線至XDP Card CON2 Pin1
+3VSB_ATX請從DIP電容跳線至XDP Card CON4 Pin19
GND請跳線至XDP Card CON2 Pin7

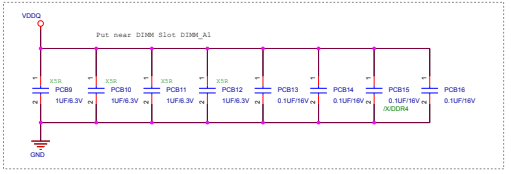


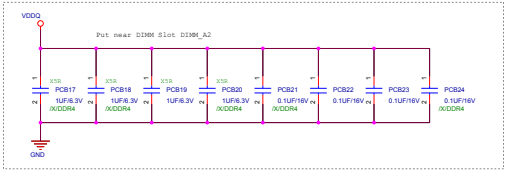

DIMM_A1A
DIMM_A2A
D4_MAA[0:16]
D4_DQ_A[0:63]
D4_MCB_A[0:7]
Chip ID
Follow X99
Address A0
Address A2
Placed close to DIMM
SMBus CAPs
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark gray:12002-00075000
the symbol here is for double ear DIMM, if need to change to single ear,must relink the symbol
Put One Caps Per DIMM Slot
DDR4_DIMM_288P

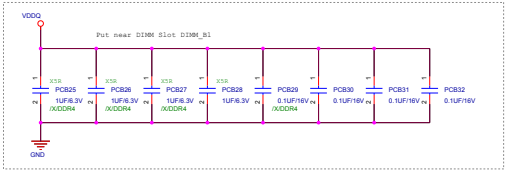

DIMM_B1A
DIMM_B2A
D4_DQ_B[0:63]
D4_MAB[0:16]
D4_MCB_B[0:7]
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark gray:12002-00075000
the symbol here is for double ear DIMM, if need to change to single ear,must link the symbol
Chip ID
Follow X99
Address A0
Address A2
D4R3 240Ohm /XDDR4 1%
D4R4 240Ohm /XDDR4 1%
VDDQ
VDDSPD
GND
D4_B_PAR
D4_B_ALERT#
D4_B_ACT#
D4_RESET#_R
CHB_DRAM_TS_EVENT#
S_SMBDATA_DDR
S_SMBCLK_DDR
D4C9 330PF/50V /XDDR4
D4C10 330PF/50V /XDDR4
D4C11 X5R 0.1UF/10V /XDDR4
D4C12 X5R 0.1UF/10V /XDDR4
Put One Caps Per DIMM Slot
DDR4_DIMM_288P

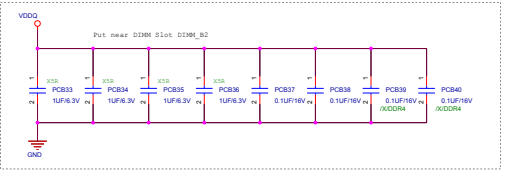

DIMM_A1B
DIMM_A2B
DIMM_B1B
DIMM_B2B
DDR4_DIMM_288P
VPPDDR
VTT_DDR
VDDQ
VDDSPD
VDDQ
D4R5
1KOhm
1%
D4R6
1KOhm
1%
D4C13
0.1UF/16V
D4C37
0.1UF/16V
D4C38
/XODR4
0.1UF/16V
D4C39
/XODR4
0.1UF/16V
D4C40
0.1UF/16V
D4C41
/XODR4
0.1UF/16V
D4R7
1KOhm
1%
D4R8
1KOhm
1%
D4C14
0.1UF/16V
D4C44
0.1UF/16V
D4C45
/XODR4
0.1UF/16V
D4C46
N/A
0.1UF/16V
D4C47
0.1UF/16V
D4C48
N/A
0.1UF/16V
H_D4A_VREFCA
H_D4A_VREFCA
H_D4B_VREFCA
H_D4B_VREFCA
D4_VREFCA_A
D4_VREFCA_B
VREFCA
NP_NC1
NP_NC2
GND
D3F501
1.5A/8V
D4R9
/XODR4
D4R10
/XODR4
0Ohm
mbs_r0603
0Ohm
mbs_r0603
+3V_ATX
/VDDSPD option to +3V
Rev 1.0 to +3V

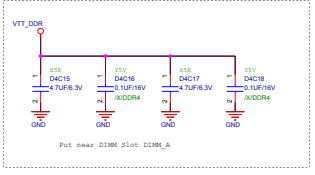

Layout to 0603
VDDQ
PCB1 22UF/6.3V mbs_c0603 Layout
PCB2 22UF/6.3V mbs_c0805
PCB3 22UF/6.3V mbs_c0805
PCB4 22UF/6.3V mbs_c0805
PCB5 22UF/6.3V mbs_c0603 Layout
PCB6 22UF/6.3V mbs_c0805
PCB7 22UF/6.3V mbs_c0603 Layout
PCB8 22UF/6.3V mbs_c0805
PCB45 22UF/6.3V mbs_c0603 Layout
GND
DIMM 附近

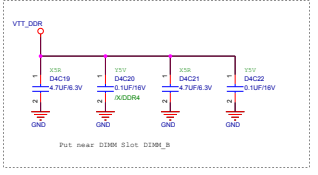

VDDQ
Put near DIMM Slot DIMM_A1
PCB9 1UF/6.3V
PCB10 1UF/6.3V
PCB11 1UF/6.3V
PCB12 1UF/6.3V
PCB13 0.1UF/16V
PCB14 0.1UF/16V
PCB15 0.1UF/16V /X/DDR4
PCB16 0.1UF/16V
GND

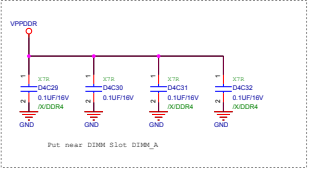

VDDQ
Put near DIMM Slot DIMM_A2
PCB17 1UF/6.3V /X/DDR4
PCB18 1UF/6.3V /X/DDR4
PCB19 1UF/6.3V
PCB20 1UF/6.3V /X/DDR4
PCB21 0.1UF/16V /X/DDR4
PCB22 0.1UF/16V
PCB23 0.1UF/16V
PCB24 0.1UF/16V /X/DDR4
GND

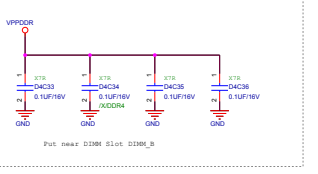

VDDQ
Put near DIMM Slot DIMM_B1
PCB25 1UF/6.3V /X/DDR4
PCB26 1UF/6.3V /X/DDR4
PCB27 1UF/6.3V /X/DDR4
PCB28 1UF/6.3V
PCB29 0.1UF/16V /X/DDR4
PCB30 0.1UF/16V
PCB31 0.1UF/16V
PCB32 0.1UF/16V
GND


VDDQ
Put near DIMM Slot DIMM_B2
PCB33 1UF/6.3V
PCB34 1UF/6.3V
PCB35 1UF/6.3V
PCB36 1UF/6.3V
PCB37 0.1UF/16V
PCB38 0.1UF/16V
PCB39 0.1UF/16V /X/DDR4
PCB40 0.1UF/16V /X/DDR4
GND

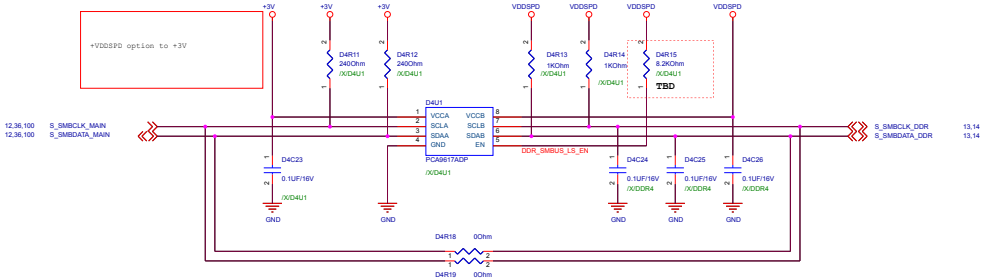

VTT_DDR
D4C15 4.7UF/6.3V
D4C16 0.1UF/16V /X/DDR4
D4C17 4.7UF/6.3V
D4C18 0.1UF/16V /X/DDR4
GND
Put near DIMM Slot DIMM_A


VTT_DDR
D4C19 4.7UF/6.3V
D4C20 0.1UF/16V /X/DDR4
D4C21 4.7UF/6.3V
D4C22 0.1UF/16V
GND
Put near DIMM Slot DIMM_B


VPPDDR
D4C29 0.1UF/16V /X/DDR4
D4C30 0.1UF/16V
D4C31 0.1UF/16V /X/DDR4
D4C32 0.1UF/16V /X/DDR4
GND
Put near DIMM Slot DIMM_A

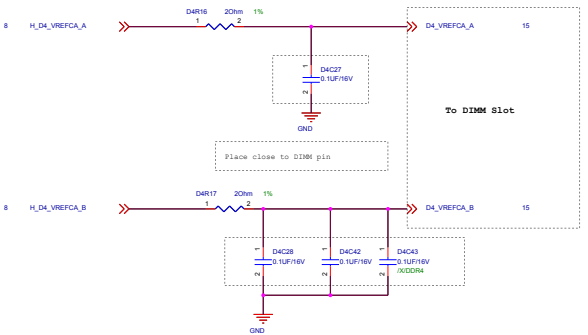

VPPDDR
D4C33 0.1UF/16V
D4C34 0.1UF/16V /X/DDR4
D4C35 0.1UF/16V
D4C36 0.1UF/16V
GND
Put near DIMM Slot DIMM_B

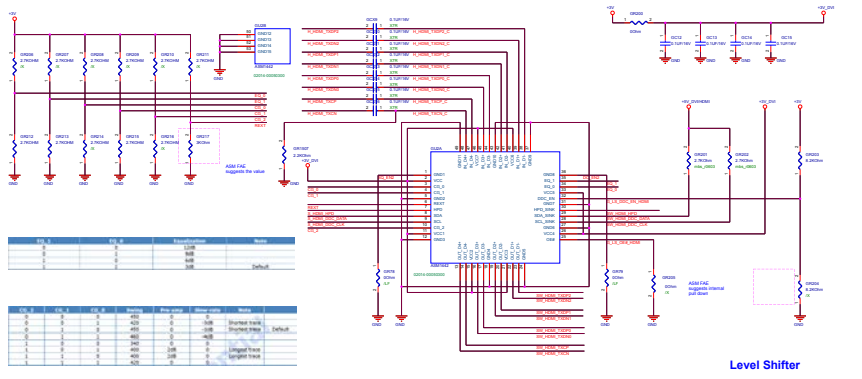
DRAM SMBUS From PCH (Thru Level Shift)



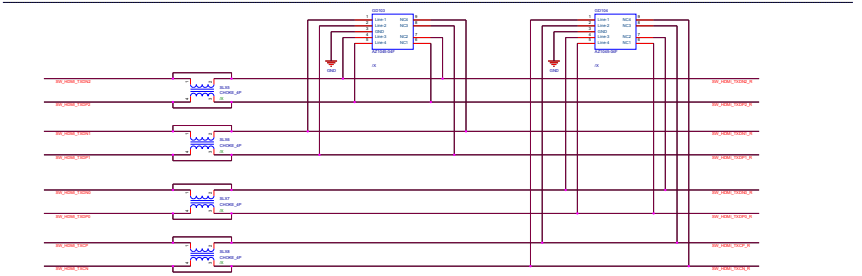
CPU DDR Vref

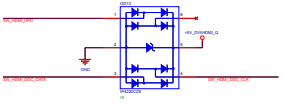
For CPU DDR Vref

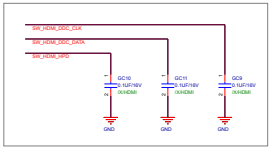


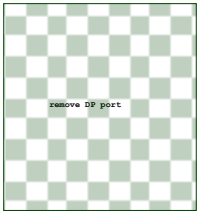


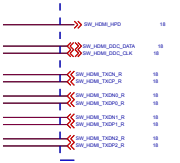
Level Shifter

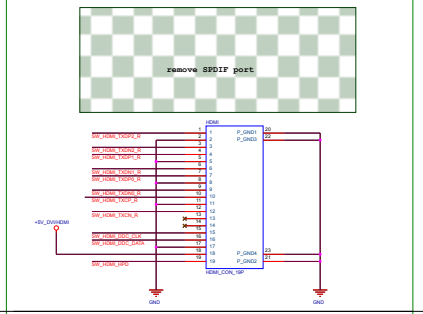












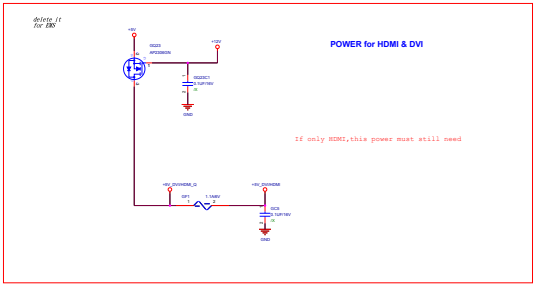
delete it for DVO

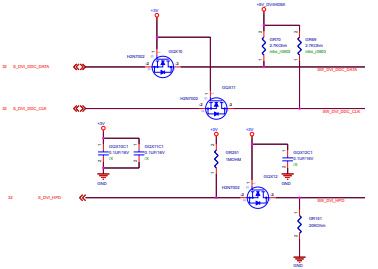
HDMI+SPDIF in two part,P/N:

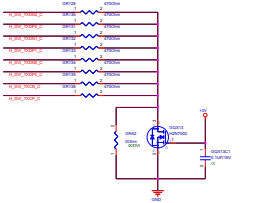
SPDIF: 12G240400301

HDMI: 12022-00046900

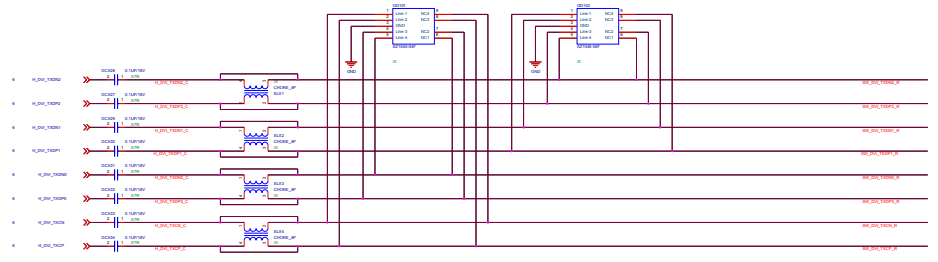
if use one part,delete this block

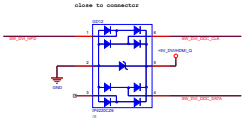


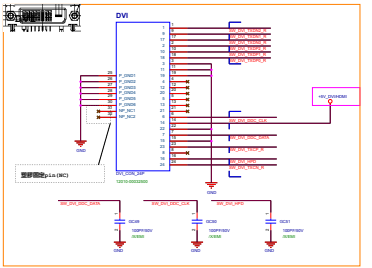


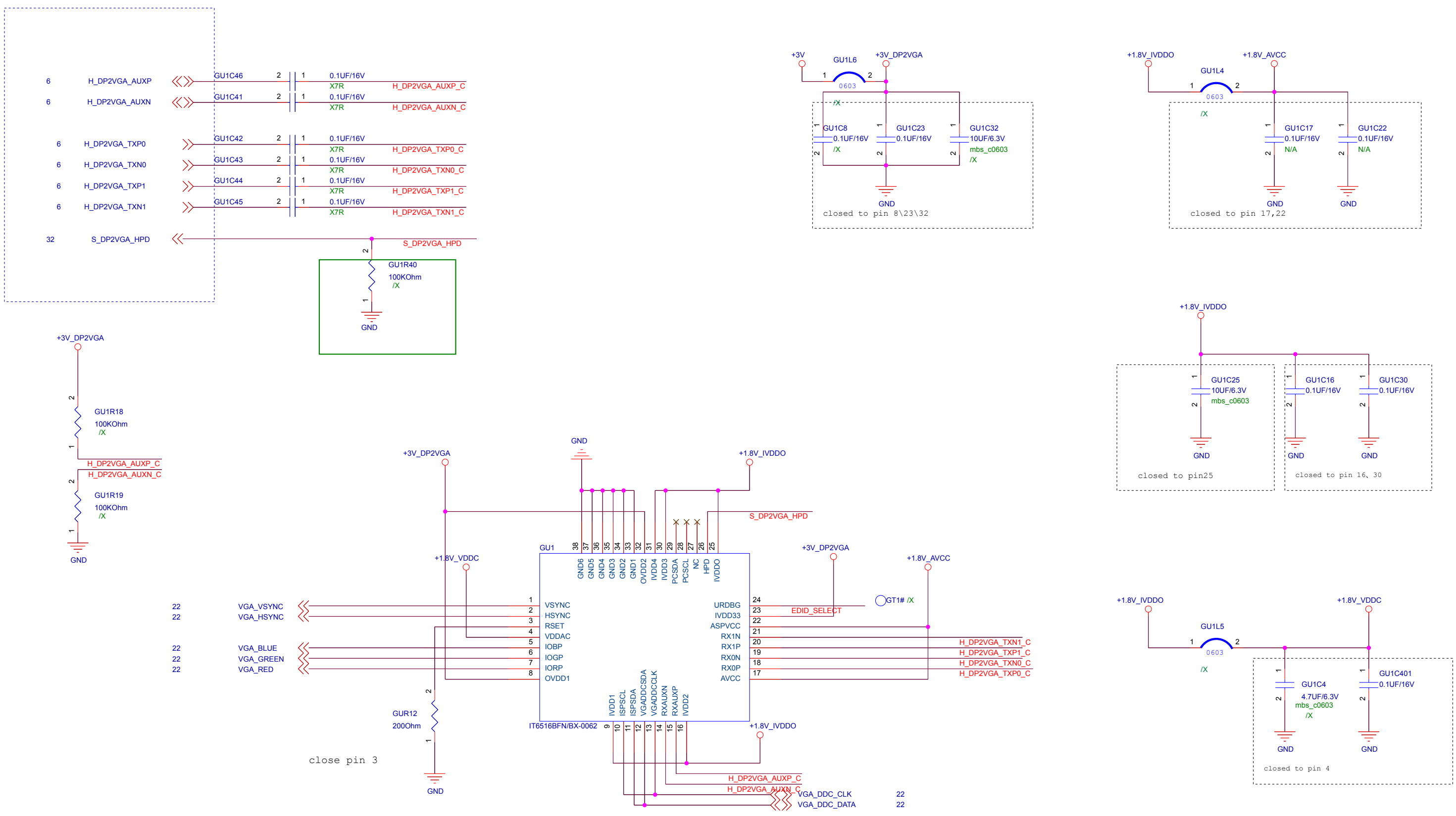


Passive/Active Devices					
Max Capacitance (Backdrive 1 Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	0 ohm	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Ron/Coul	NA	NA	10pF	3ohm/10pF	NA

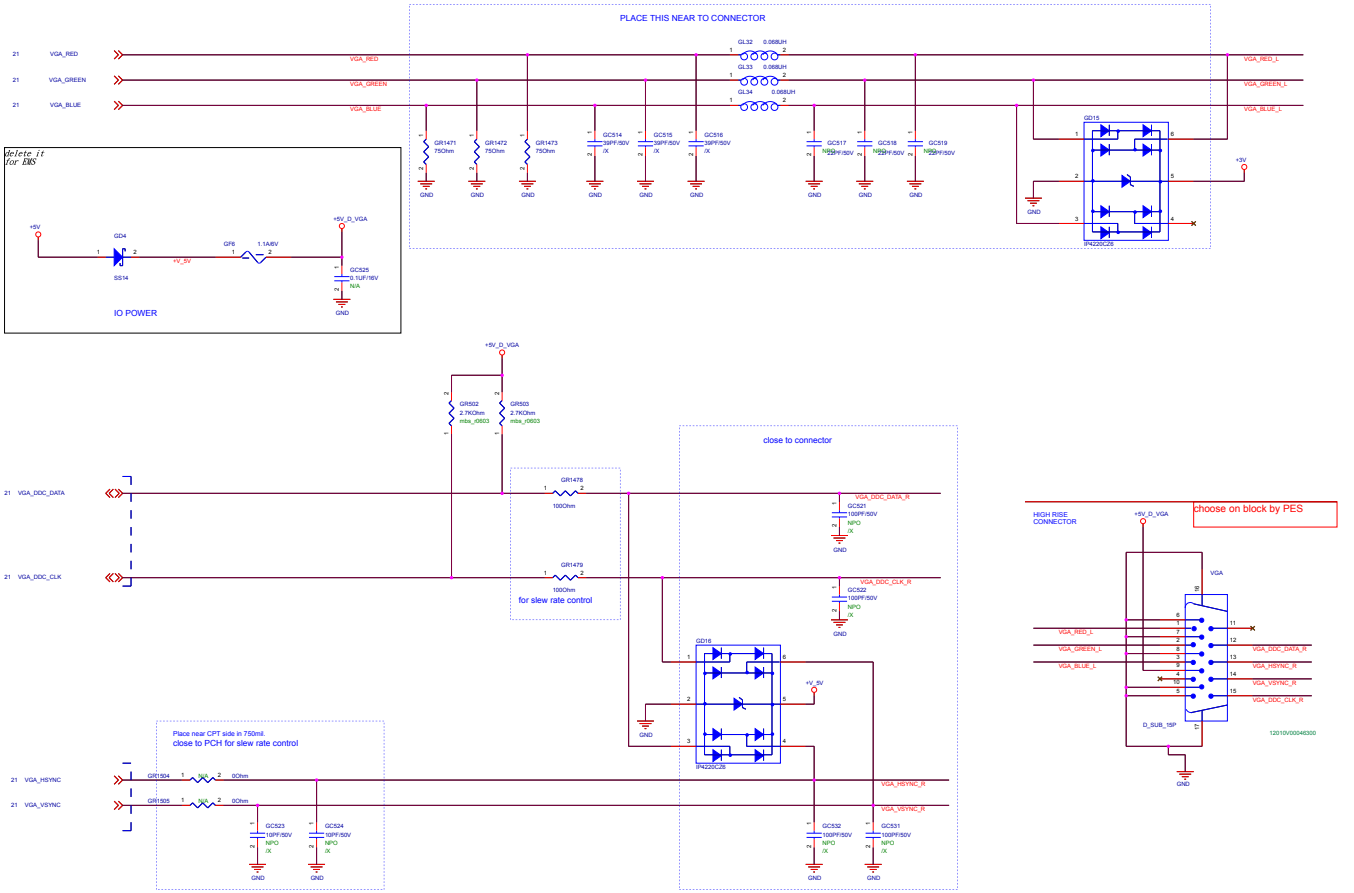




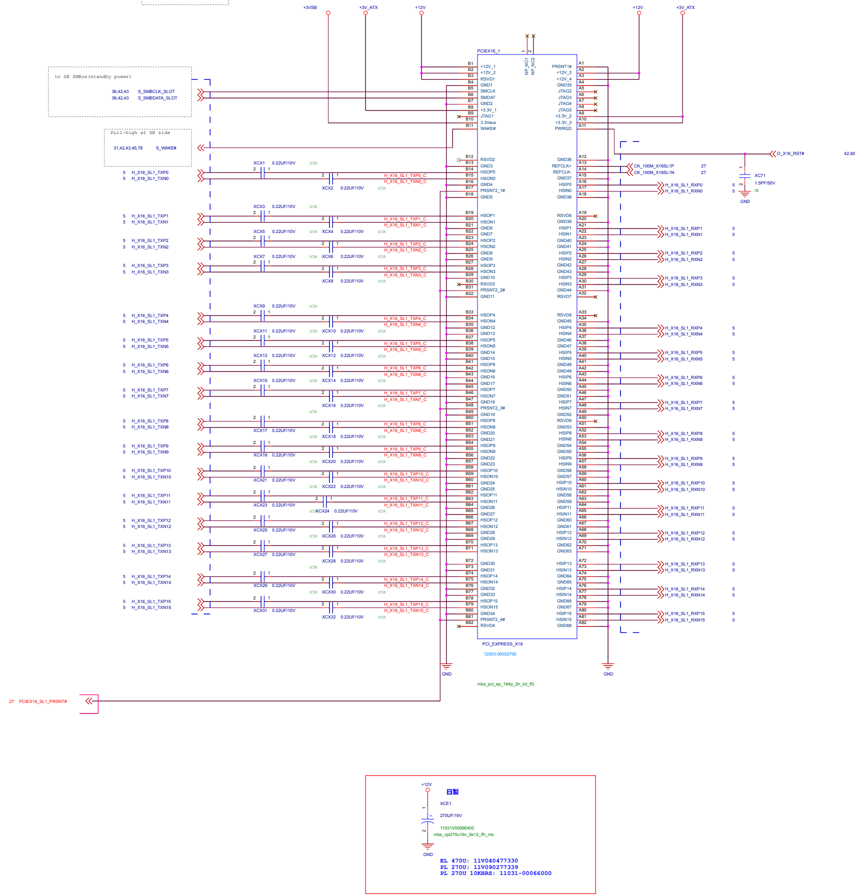




H_DP2VGA_AUXP
H_DP2VGA_AUXN
H_DP2VGA_TXP0
H_DP2VGA_TXN0
H_DP2VGA_TXP1
H_DP2VGA_TXN1
S_DP2VGA_HPD
GU1C46 0.1UF/16V X7R H_DP2VGA_AUXP_C
GU1C41 0.1UF/16V X7R H_DP2VGA_AUXN_C
GU1C42 0.1UF/16V X7R H_DP2VGA_TXP0_C
GU1C43 0.1UF/16V X7R H_DP2VGA_TXN0_C
GU1C44 0.1UF/16V X7R H_DP2VGA_TXP1_C
GU1C45 0.1UF/16V X7R H_DP2VGA_TXN1_C
GU1R40 100KOhm /X
GND
+3V GU1L6 0603 +3V_DP2VGA
GU1C8 0.1UF/16V /X
GU1C23 0.1UF/16V
GU1C32 10UF/6.3V mbs_c0603 /X
closed to pin 8\23\32
+1.8V_IVDDO GU1L4 0603 +1.8V_AVCC
GU1C17 0.1UF/16V N/A
GU1C22 0.1UF/16V N/A
closed to pin 17,22
+3V_DP2VGA
GU1R18 100KOhm /X
GU1R19 100KOhm /X
H_DP2VGA_AUXP_C
H_DP2VGA_AUXN_C
+1.8V_IVDDO
GU1C25 10UF/6.3V mbs_c0603
GU1C16 0.1UF/16V
GU1C30 0.1UF/16V
closed to pin25
closed to pin 16, 30
GU1
IT6516BFN/BX-0062
VSYNC HSYNC RSET VDDAC IOBP IOGP IORP OVDD1
GND6 GND5 GND4 GND3 GND2 GND1 OVDD2 IVDD4 IVDD3 PCSDA PCSCL NC HPD IVDDO
URDBG IVDD33 ASPVCC RX1N RX1P RX0N RX0P AVCC
IVDD1 ISPSCL ISPSDA VGADDCSDA VGADDCCLK RXAUXN RXAUXP IVDD2
VGA_VSYNC
VGA_HSYNC
VGA_BLUE
VGA_GREEN
VGA_RED
+1.8V_VDDC
EDID_SELECT
GT1# /X
+1.8V_AVCC
H_DP2VGA_TXN1_C
H_DP2VGA_TXP1_C
H_DP2VGA_TXN0_C
H_DP2VGA_TXP0_C
GUR12 200Ohm
close pin 3
VGA_DDC_CLK
VGA_DDC_DATA
+1.8V_IVDDO GU1L5 0603 +1.8V_VDDC
GU1C4 4.7UF/6.3V mbs_c0603 /X
GU1C401 0.1UF/16V
closed to pin 4


PLACE THIS NEAR TO CONNECTOR
21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
GL32 0.068UH
GL33 0.068UH
GL34 0.068UH
GR1471 75Ohm
GR1472 75Ohm
GR1473 75Ohm
GCS14 18PF/50V /X
GCS15 18PF/50V /X
GCS16 18PF/50V /X
GC517 220PF/50V NPO /X
GC518 220PF/50V NPO /X
GC519 220PF/50V NPO /X
GD15
IP4220CZ6
+3V
GND
delete it for EMS
+5V
GD4
SS14
+5V_5V
GF6 1.1A/6V
+5V_D_VGA
GC525 0.1UF/16V N/A
IO POWER
+5V_D_VGA
GR502 2.7KOhm mba_r0603
GR503 2.7KOhm mba_r0603
21 VGA_DDC_DATA
21 VGA_DDC_CLK
GR1478 100Ohm
GR1479 100Ohm
for slew rate control
close to connector
VGA_DDC_DATA_R
VGA_DDC_CLK_R
GC521 100PF/50V NPO /X
GC522 100PF/50V NPO /X
GD16
IP4220CZ6
+5V_5V
Place near CPT side in 750mil.
close to PCH for slew rate control
21 VGA_HSYNC
21 VGA_VSYNC
GR1504 0Ohm N/A
GR1505 0Ohm N/A
VGA_HSYNC_R
VGA_VSYNC_R
GC523 10PF/50V NPO /X
GC524 10PF/50V NPO /X
GC532 100PF/50V NPO /X
GC531 100PF/50V NPO /X
HIGH RISE CONNECTOR
choose on block by PES
+5V_D_VGA
VGA
D_SUB_15P
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
VGA_DDC_DATA_R
VGA_HSYNC_R
VGA_VSYNC_R
VGA_DDC_CLK_R
12010V00046300

Support Gen3

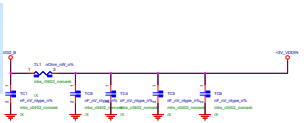


SEL_CLK Function Select Table

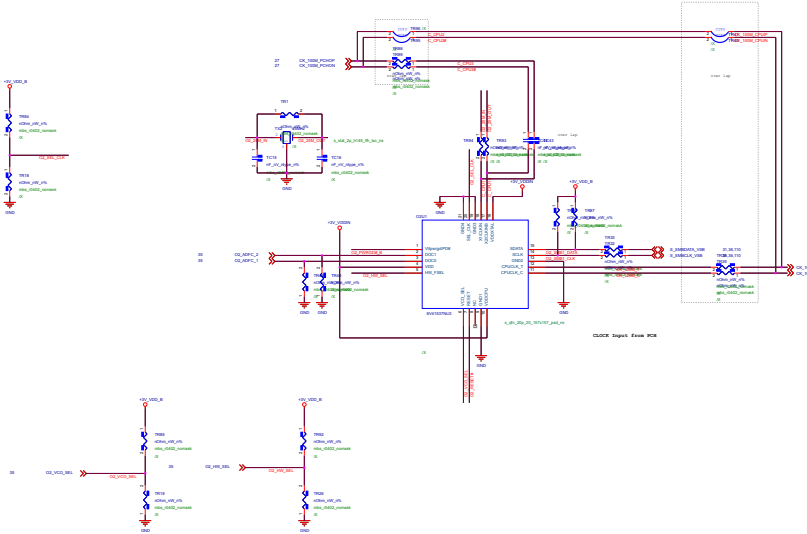
SEL_CLK	X1/CLKIN	X2/CLKINB
0	X1	X2
1	CLKIN	CLKINB

CPU (MHz)	CPU Step (MHz)	Typ 55% 80b3=1 (PWD)	Typ 55% 80b3=0			
100.00	0.25	-0.46%	OFF			
100.00	0.08	-0.46%	OFF			
412.00	412.0	4	103.00	0.25	-0.46%	OFF
1236.00	12	103.00	0.08	-0.46%	OFF	

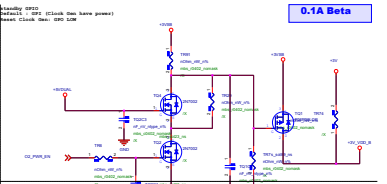
*Default by hardware latch



SLAVE ADDRESS: D2

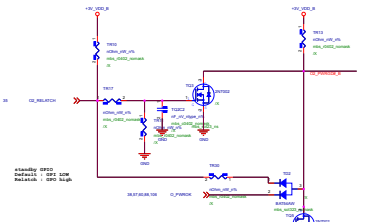


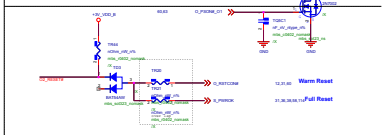
standby SPIO
Default : SPI (Clock Gen have power)
Reset Clock Gen: SPO LOW

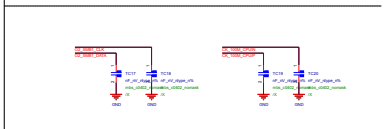


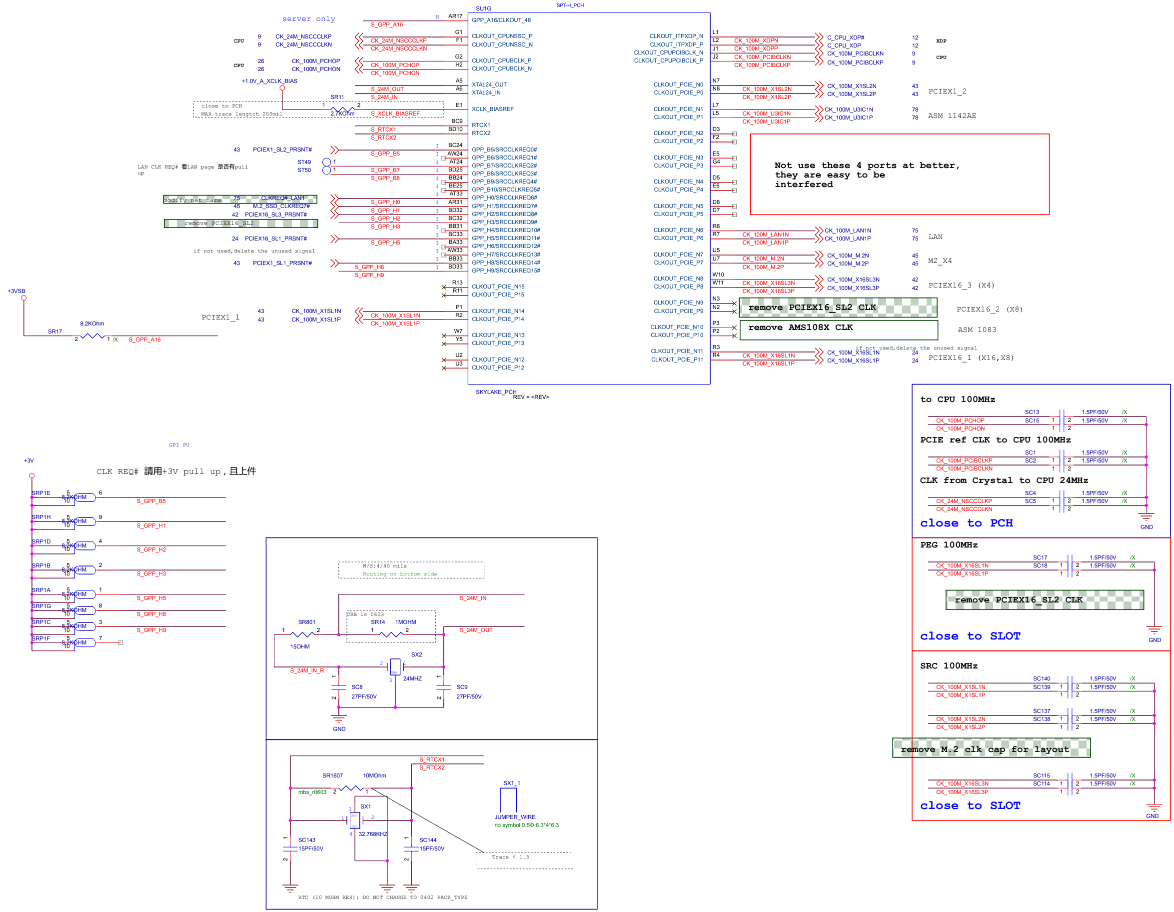
0.1A Beta

standby SPIO
Default : SPI LOW
Switch : SPO high

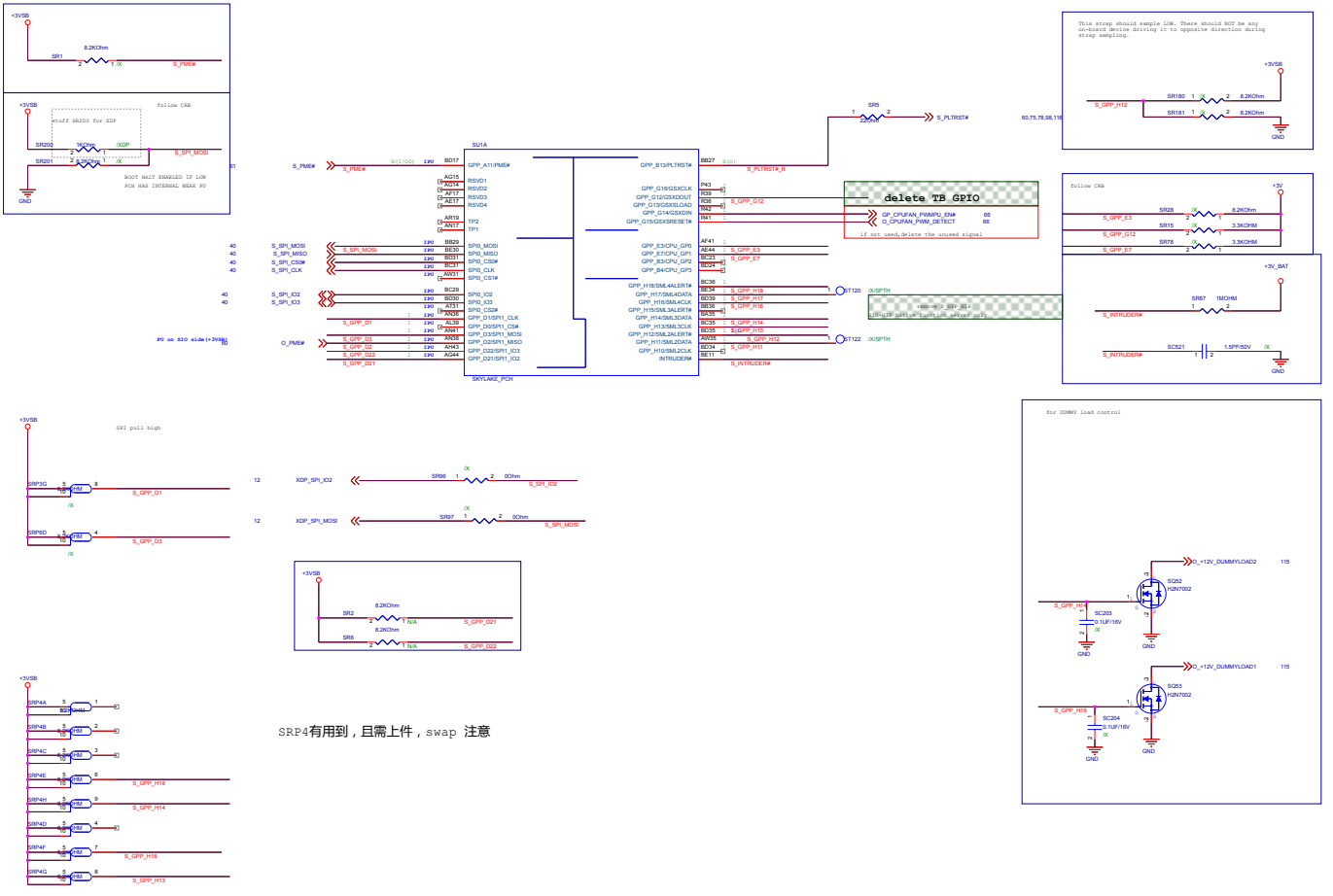




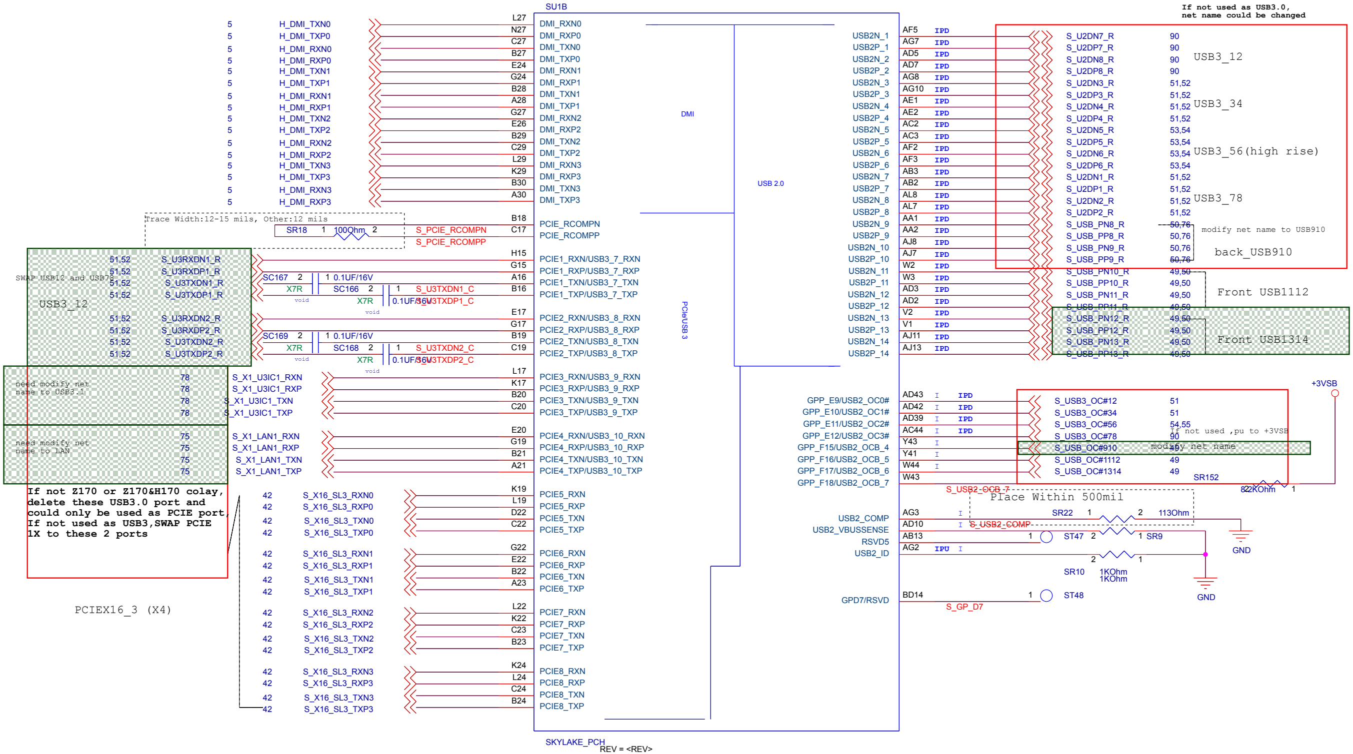


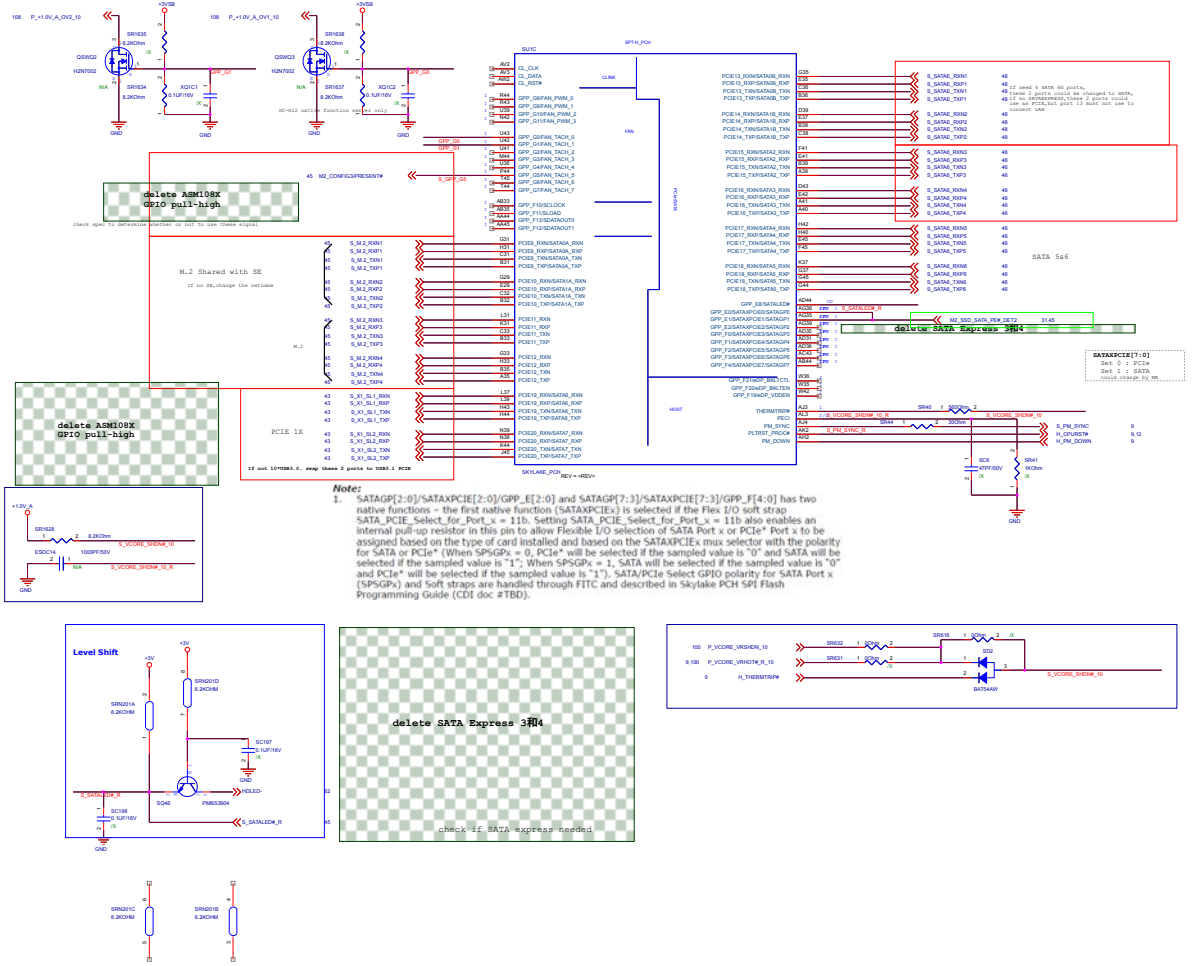


server only
SU1G
SPT-H_PCH
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
RTCX1
RTCX2
close to PCH
MAX trace length 200mil
LAN CLK REQ# 看LAN page 是否有pull up
modify net name
remove PCIEX16_SL2
if not used,delete the unused signal
PCIEX1_1
SKYLAKE_PCH
REV = <REV>
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
XDP
CPU
PCIEX1_2
ASM 1142AE
Not use these 4 ports at better, they are easy to be interferred
LAN
M2_X4
PCIEX16_3 (X4)
remove PCIEX16_SL2 CLK
PCIEX16_2 (X8)
remove AMS108X CLK
ASM 1083
PCIEX16_1 (X16,X8)
GPI PU
CLK REQ# 請用+3V pull up,且上件
W/S:4/40 mils
Routing on bottom side
24MHZ
32.768KHZ
JUMPER_WIRE
Trace < 1.5
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE
to CPU 100MHz
PCIE ref CLK to CPU 100MHz
CLK from Crystal to CPU 24MHz
close to PCH
PEG 100MHz
remove PCIEX16_SL2 CLK
close to SLOT
SRC 100MHz
remove M.2 clk cap for layout
close to SLOT



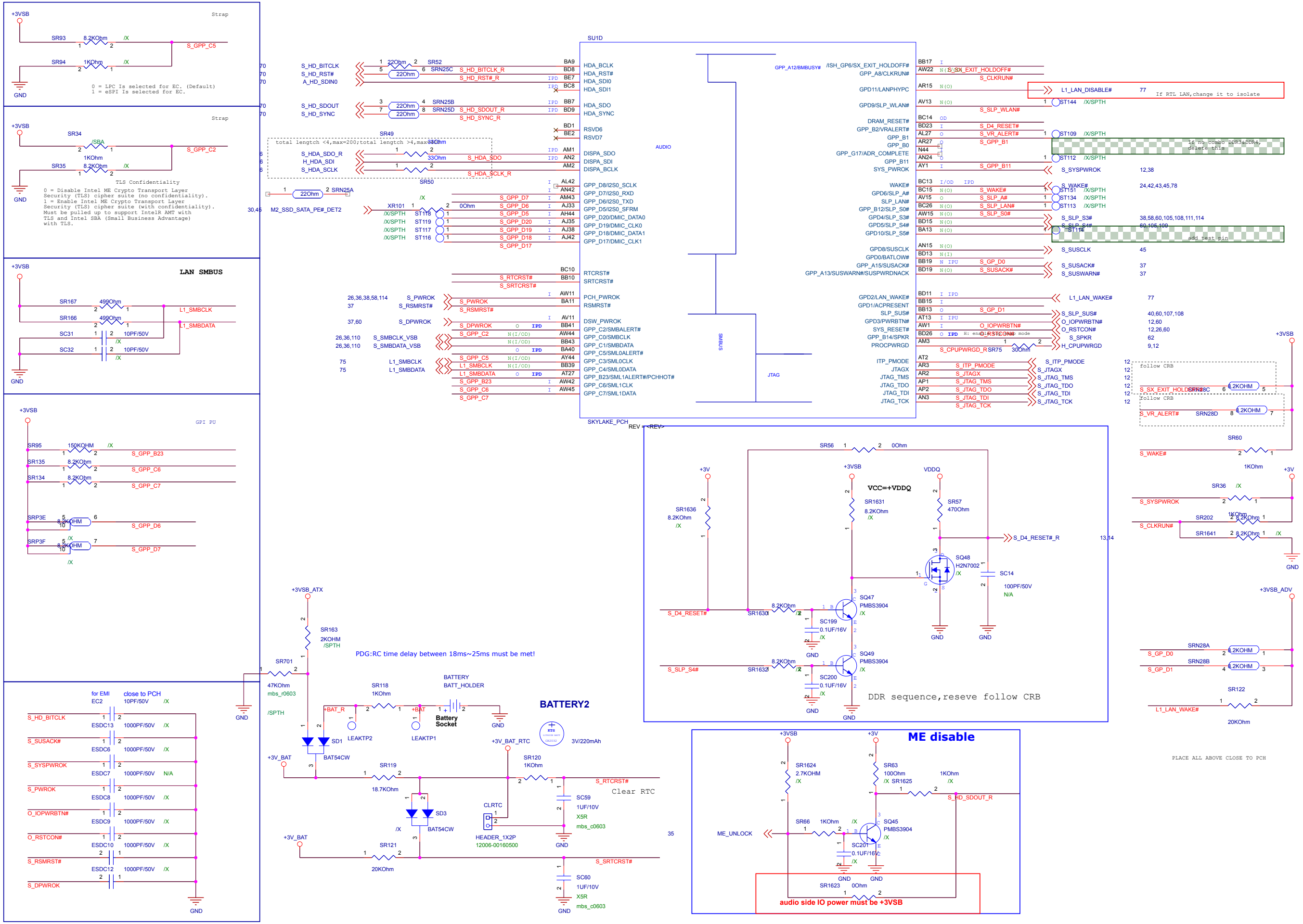
SRP4有用到，且需上件，swap 注意


SU1B
If not used as USB3.0, net name could be changed
H_DMI_TXN0
H_DMI_TXP0
H_DMI_RXN0
H_DMI_RXP0
H_DMI_TXN1
H_DMI_TXP1
H_DMI_RXN1
H_DMI_RXP1
H_DMI_TXN2
H_DMI_TXP2
H_DMI_RXN2
H_DMI_RXP2
H_DMI_TXN3
H_DMI_TXP3
H_DMI_RXN3
H_DMI_RXP3
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI
Trace Width:12-15 mils, Other:12 mils
SR18 100Ohm
S_PCIE_RCOMPN
S_PCIE_RCOMPP
PCIE_RCOMPN
PCIE_RCOMPP
SWAP USB12 and USB78
USB3_12
S_U3RXDN1_R
S_U3RXDP1_R
S_U3TXDN1_R
S_U3TXDP1_R
S_U3RXDN2_R
S_U3RXDP2_R
S_U3TXDN2_R
S_U3TXDP2_R
SC167 0.1UF/16V
SC166 X7R 0.1UF/16V
S_U3TXDN1_C
S_U3TXDP1_C
SC169 0.1UF/16V
SC168 X7R 0.1UF/16V
S_U3TXDN2_C
S_U3TXDP2_C
void
PCIE1_RXN/USB3_7_RXN
PCIE1_RXP/USB3_7_RXP
PCIE1_TXN/USB3_7_TXN
PCIE1_TXP/USB3_7_TXP
PCIE2_RXN/USB3_8_RXN
PCIE2_RXP/USB3_8_RXP
PCIE2_TXN/USB3_8_TXN
PCIE2_TXP/USB3_8_TXP
need modify net name to USB3.1
S_X1_U3IC1_RXN
S_X1_U3IC1_RXP
S_X1_U3IC1_TXN
S_X1_U3IC1_TXP
PCIE3_RXN/USB3_9_RXN
PCIE3_RXP/USB3_9_RXP
PCIE3_TXN/USB3_9_TXN
PCIE3_TXP/USB3_9_TXP
need modify net name to LAN
S_X1_LAN1_RXN
S_X1_LAN1_RXP
S_X1_LAN1_TXN
S_X1_LAN1_TXP
PCIE4_RXN/USB3_10_RXN
PCIE4_RXP/USB3_10_RXP
PCIE4_TXN/USB3_10_TXN
PCIE4_TXP/USB3_10_TXP
If not Z170 or Z170&H170 colay, delete these USB3.0 port and could only be used as PCIE port, If not used as USB3,SWAP PCIE 1X to these 2 ports
PCIEX16_3 (X4)
S_X16_SL3_RXN0
S_X16_SL3_RXP0
S_X16_SL3_TXN0
S_X16_SL3_TXP0
S_X16_SL3_RXN1
S_X16_SL3_RXP1
S_X16_SL3_TXN1
S_X16_SL3_TXP1
S_X16_SL3_RXN2
S_X16_SL3_RXP2
S_X16_SL3_TXN2
S_X16_SL3_TXP2
S_X16_SL3_RXN3
S_X16_SL3_RXP3
S_X16_SL3_TXN3
S_X16_SL3_TXP3
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP
PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
PCIe/USB 3
USB 2.0
USB2N_1
USB2P_1
USB2N_2
USB2P_2
USB2N_3
USB2P_3
USB2N_4
USB2P_4
USB2N_5
USB2P_5
USB2N_6
USB2P_6
USB2N_7
USB2P_7
USB2N_8
USB2P_8
USB2N_9
USB2P_9
USB2N_10
USB2P_10
USB2N_11
USB2P_11
USB2N_12
USB2P_12
USB2N_13
USB2P_13
USB2N_14
USB2P_14
S_U2DN7_R
S_U2DP7_R
S_U2DN8_R
S_U2DP8_R
USB3_12
S_U2DN3_R
S_U2DP3_R
S_U2DN4_R
S_U2DP4_R
USB3_34
S_U2DN5_R
S_U2DP5_R
S_U2DN6_R
S_U2DP6_R
USB3_56(high rise)
S_U2DN1_R
S_U2DP1_R
S_U2DN2_R
S_U2DP2_R
USB3_78
S_USB_PN8_R
S_USB_PP8_R
S_USB_PN9_R
S_USB_PP9_R
modify net name to USB910
back_USB910
S_USB_PN10_R
S_USB_PP10_R
S_USB_PN11_R
S_USB_PP11_R
Front USB1112
S_USB_PN12_R
S_USB_PP12_R
S_USB_PN13_R
S_USB_PP13_R
Front USB1314
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OCB_4
GPP_F16/USB2_OCB_5
GPP_F17/USB2_OCB_6
GPP_F18/USB2_OCB_7
+3VSB
S_USB3_OC#12
S_USB3_OC#34
S_USB3_OC#56
S_USB3_OC#78
If not used ,pu to +3VSB
S_USB_OC#910
modify net name
S_USB_OC#1112
S_USB_OC#1314
SR152 8.2KOhm
S_USB2-OCB-7
Place Within 500mil
USB2_COMP
USB2_VBUSSENSE
RSVD5
USB2_ID
SR22 113Ohm
S_USB2-COMP
ST47
SR9
SR10 1KOhm 1KOhm
GND
GPD7/RSVD
ST48
S_GP_D7
SKYLAKE_PCH
REV = <REV>

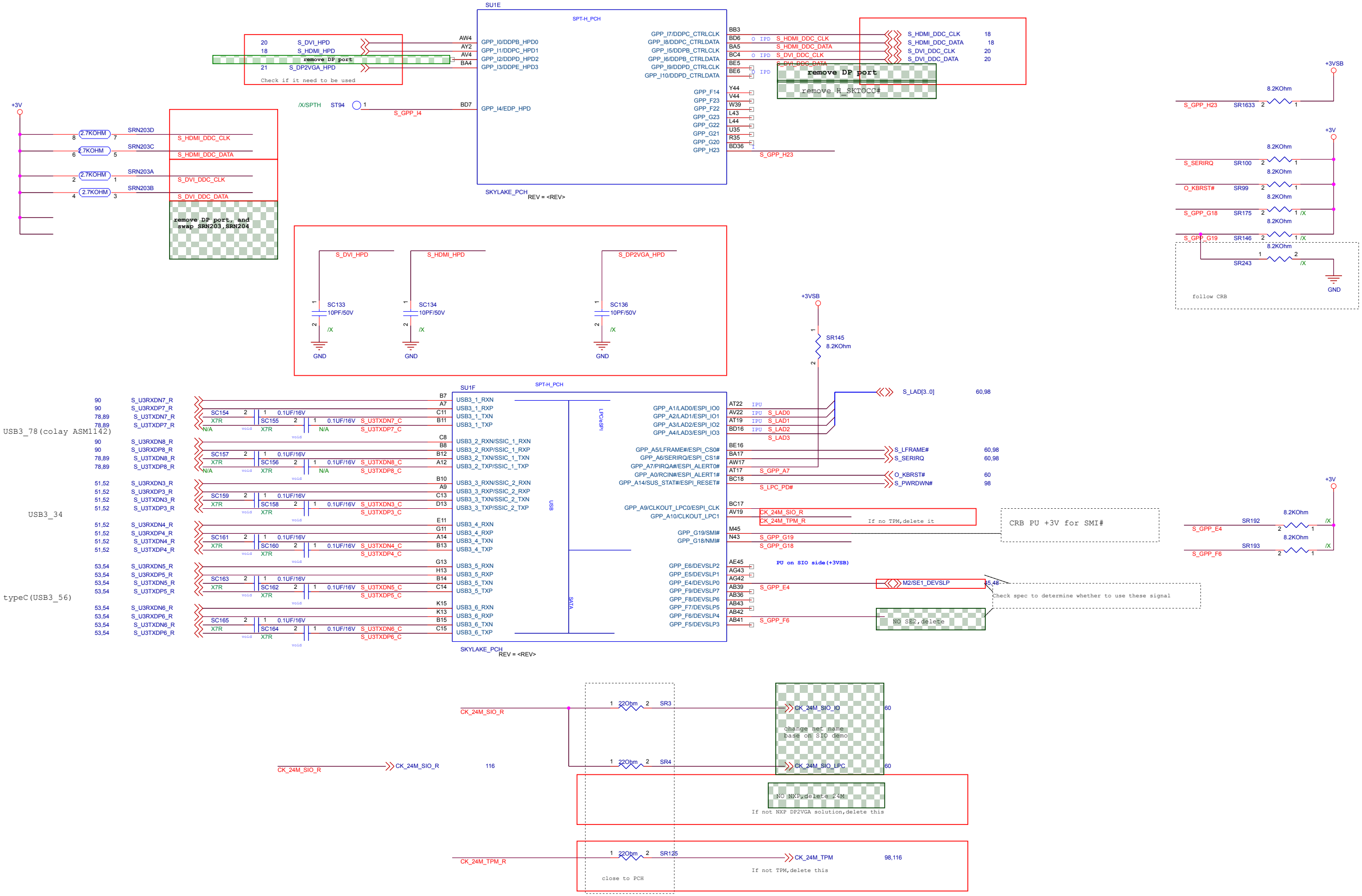


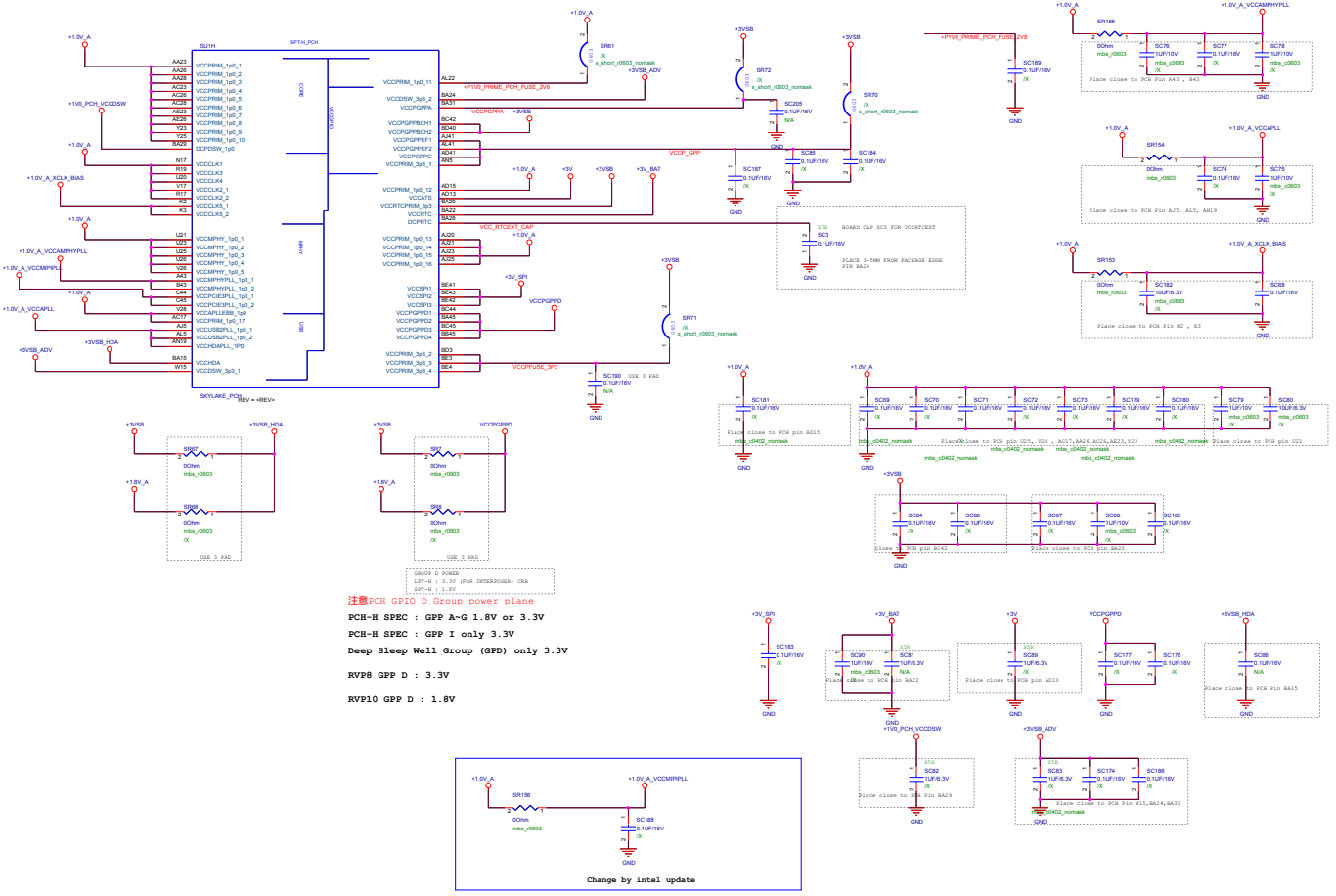
Note:

1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions – the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).



Strap
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
Must be pulled up to support Intel® AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
LAN SMBUS
GPI PU
SU1D
AUDIO
SMBUS
JTAG
SKYLAKE_PCH
total lengtch <4,max=200;total lengtch >4,max=100
If RTL LAN,change it to isolate
If no combo DDR3&DDR4, delete this
add test pin
follow CRB
PDG:RC time delay between 18ms~25ms must be met!
BATTERY2
Clear RTC
VCC=+VDDQ
DDR sequence,reseve follow CRB
ME disable
audio side IO power must be +3VSB
PLACE ALL ABOVE CLOSE TO PCH


SU1E
SPT-H_PCH
S_DVI_HPD
S_HDMI_HPD
remove DP port
S_DP2VGA_HPD
Check if it need to be used
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_F14
GPP_F23
GPP_F22
GPP_G23
GPP_G22
GPP_G21
GPP_G20
GPP_H23
S_HDMI_DDC_CLK
S_HDMI_DDC_DATA
S_DVI_DDC_CLK
S_DVI_DDC_DATA
remove DP port
remove H_SKTOCC#
S_GPP_H23
SKYLAKE_PCH
REV = <REV>
+3V
2.7KOHM
SRN203D
SRN203C
SRN203A
SRN203B
remove DP port, and swap SRN203,SRN204
/X/SPTH
ST94
S_GPP_I4
SC133
SC134
SC136
10PF/50V
GND
+3VSB
8.2KOhm
SR1633
S_SERIRQ
SR100
O_KBRST#
SR99
S_GPP_G18
SR175
S_GPP_G19
SR146
SR243
follow CRB
SR145
SU1F
SPT-H_PCH
USB3_78(colay ASM1142)
USB3_34
typeC(USB3_56)
S_U3RXDN7_R
S_U3RXDP7_R
S_U3TXDN7_R
S_U3TXDP7_R
S_U3RXDN8_R
S_U3RXDP8_R
S_U3TXDN8_R
S_U3TXDP8_R
S_U3RXDN3_R
S_U3RXDP3_R
S_U3TXDN3_R
S_U3TXDP3_R
S_U3RXDN4_R
S_U3RXDP4_R
S_U3TXDN4_R
S_U3TXDP4_R
S_U3RXDN5_R
S_U3RXDP5_R
S_U3TXDN5_R
S_U3TXDP5_R
S_U3RXDN6_R
S_U3RXDP6_R
S_U3TXDN6_R
S_U3TXDP6_R
0.1UF/16V
X7R
N/A
USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP
USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP
USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP
USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP
USB3_5_RXN
USB3_5_RXP
USB3_5_TXN
USB3_5_TXP
USB3_6_RXN
USB3_6_RXP
USB3_6_TXN
USB3_6_TXP
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_G19/SMI#
GPP_G18/NMI#
GPP_E6/DEVSLP2
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_F9/DEVSLP7
GPP_F8/DEVSLP6
GPP_F7/DEVSLP5
GPP_F6/DEVSLP4
GPP_F5/DEVSLP3
S_LAD[3..0]
S_LAD0
S_LAD1
S_LAD2
S_LAD3
S_LFRAME#
S_SERIRQ
S_GPP_A7
O_KBRST#
S_PWRDWN#
S_LPC_PD#
CK_24M_SIO_R
CK_24M_TPM_R
If no TPM,delete it
CRB PU +3V for SMI#
S_GPP_E4
S_GPP_F6
SR192
SR193
PU on SIO side(+3VSB)
M2/SE1_DEVSLP
Check spec to determine whether to use these signal
NO SE2,delete
22Ohm
SR3
SR4
SR125
CK_24M_SIO_IO
change net name base on SIO demo
CK_24M_SIO_LPC
NO NXP,delete 24M
If not NXP DP2VGA solution,delete this
CK_24M_TPM
If not TPM,delete this
close to PCH



注意PCH GPIO D Group power plane

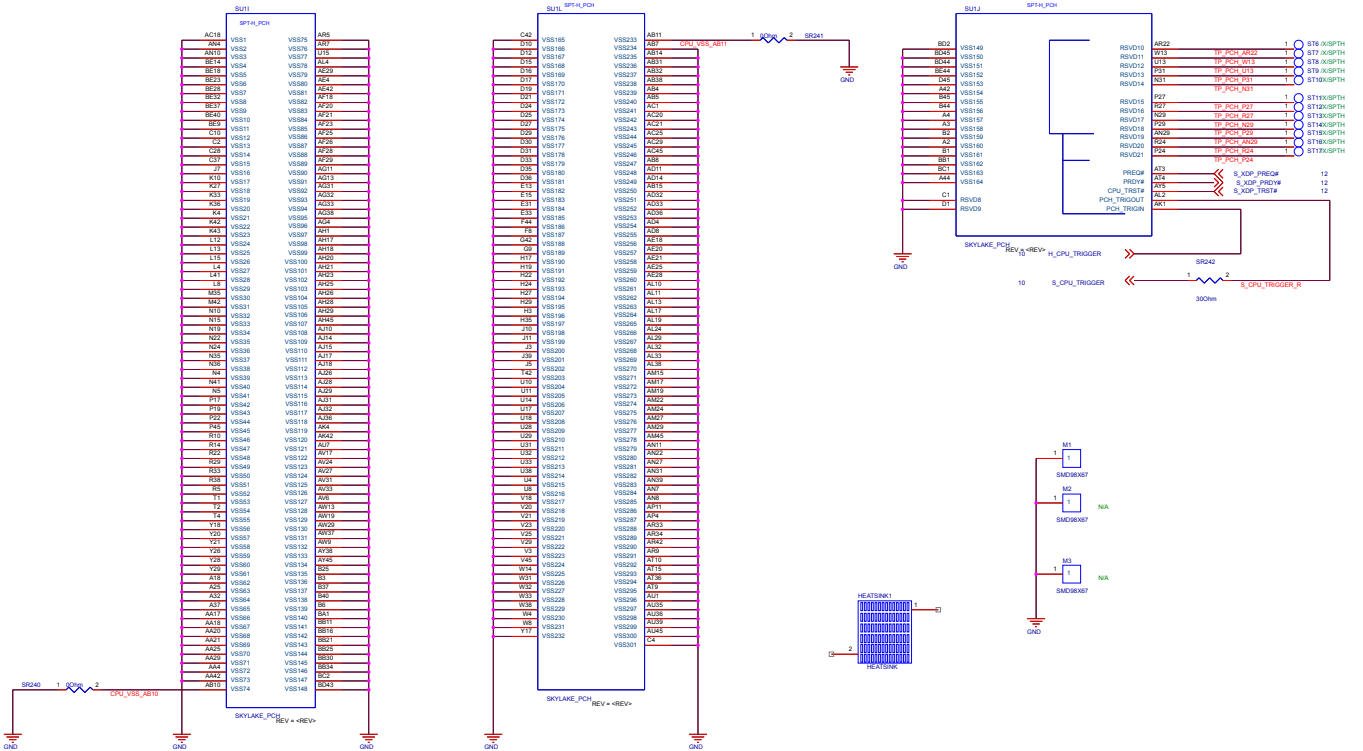
PCH-H SPEC : GPP A~G 1.8V or 3.3V

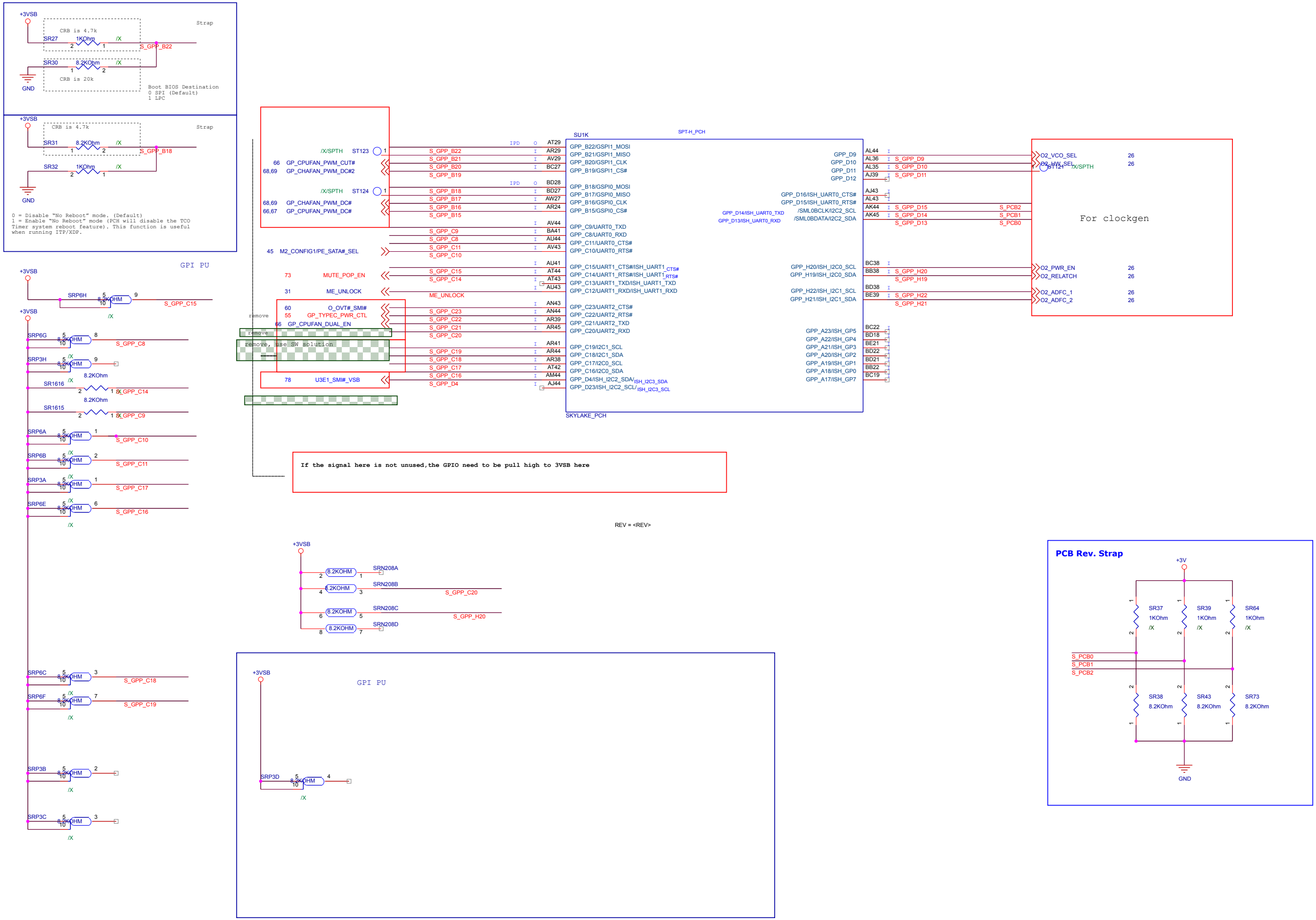
PCH-H SPEC : GPP I only 3.3V

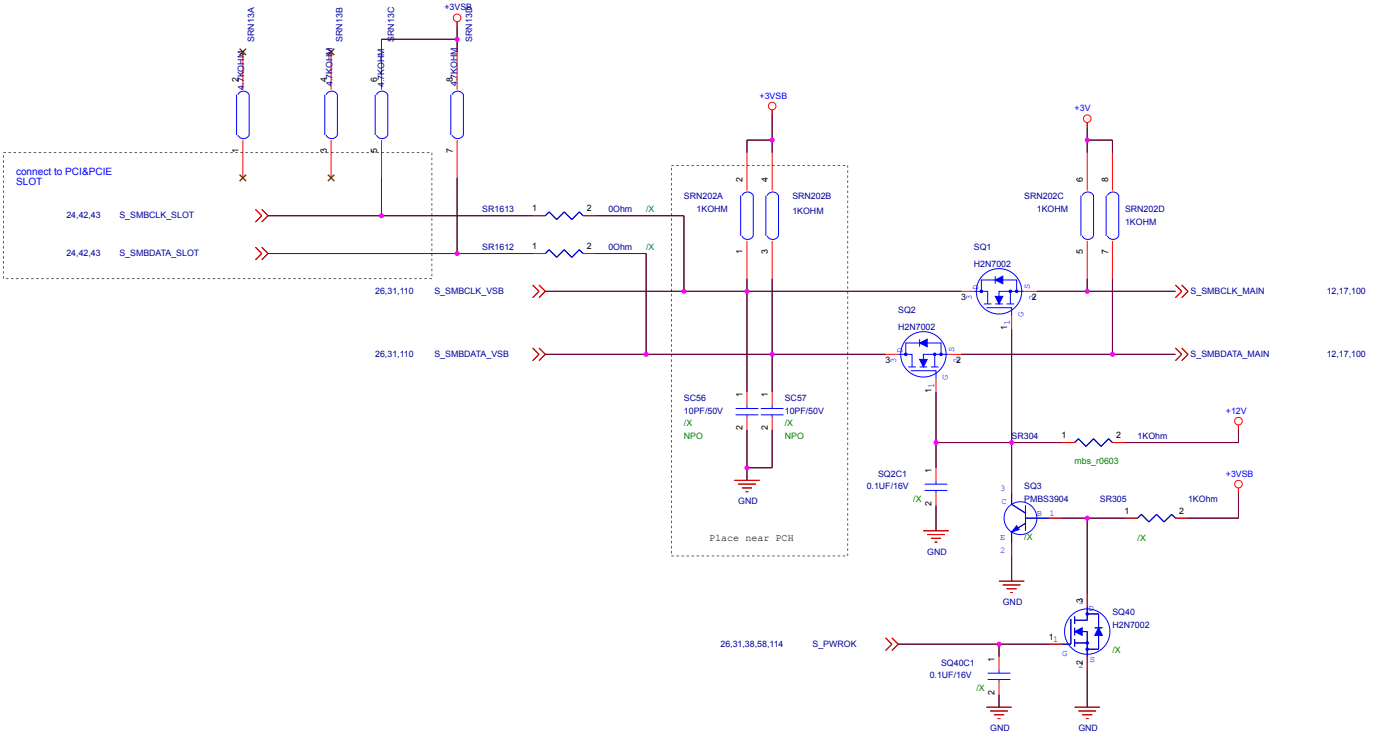
Deep Sleep Well Group (GPD) only 3.3V

RVP8 GPP D : 3.3V

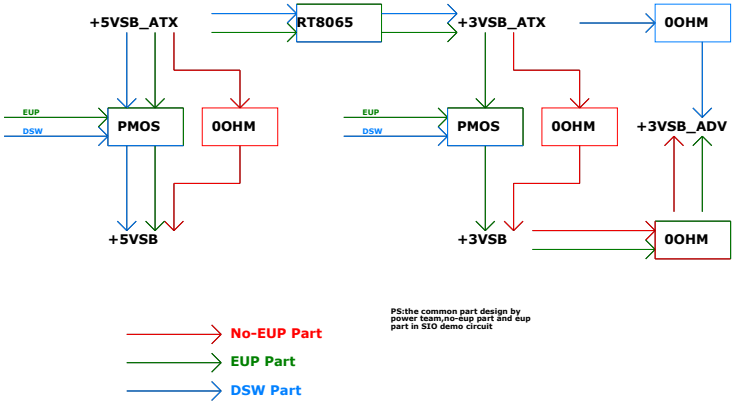
RVP10 GPP D : 1.8V


SU1I
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
SU1L
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
SU1J
SPT-H_PCH
SKYLAKE_PCH
REV = <REV>
SR240
90hm
CPU_VSS_AB10
CPU_VSS_AB11
SR241
90hm
H_CPU_TRIGGER
S_CPU_TRIGGER
SR242
30Ohm
S_CPU_TRIGGER_R
S_XDP_PREQ#
S_XDP_PRDY#
S_XDP_TRST#
TP_PCH_AR22
TP_PCH_W13
TP_PCH_U13
TP_PCH_P31
TP_PCH_N31
TP_PCH_P27
TP_PCH_R27
TP_PCH_N29
TP_PCH_P29
TP_PCH_AN29
TP_PCH_R24
TP_PCH_P24
HEATSINK1
HEATSINK
M1
SMD98X67
M2
SMD98X67
N/A
M3
SMD98X67
N/A
GND


+3VSB
CRB is 4.7k
SR27 1KOhm /X
S_GPP_B22
Strap
SR30 8.2KOhm /X
CRB is 20k
GND
Boot BIOS Destination
0 SPI (Default)
1 LPC
CRB is 4.7k
SR31 8.2KOhm /X
S_GPP_B18
SR32 1KOhm /X
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
GPI PU
SRP6H 8.2KOHM S_GPP_C15
SRP6G S_GPP_C8
SRP3H
SR1616 8.2KOhm S_GPP_C14
SR1615 8.2KOhm S_GPP_C9
SRP6A S_GPP_C10
SRP6B S_GPP_C11
SRP3A S_GPP_C17
SRP6E S_GPP_C16
SRP6C S_GPP_C18
SRP6F S_GPP_C19
SRP3B
SRP3C
/X/SPTH ST123
66 GP_CPUFAN_PWM_CUT#
68,69 GP_CHAFAN_PWM_DC#2
/X/SPTH ST124
68,69 GP_CHAFAN_PWM_DC#
66,67 GP_CPUFAN_PWM_DC#
45 M2_CONFIG1/PE_SATA#_SEL
73 MUTE_POP_EN
31 ME_UNLOCK
60 O_OVT#_SMI#
55 GP_TYPEC_PWR_CTL
66 GP_CPUFAN_DUAL_EN
remove
remove, use SW solution
78 U3E1_SMI#_VSB
SU1K SPT-H_PCH
GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO
GPP_B20/GSPI1_CLK
GPP_B19/GSPI1_CS#
GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO
GPP_B16/GSPI0_CLK
GPP_B15/GSPI0_CS#
GPP_C9/UART0_TXD
GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#
GPP_C21/UART2_TXD
GPP_C20/UART2_RXD
GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA
GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA
GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA
GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL
GPP_D9
GPP_D10
GPP_D11
GPP_D12
GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#
GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD
/SML0BCLK/I2C2_SCL
/SML0BDATA/I2C2_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_A23/ISH_GP5
GPP_A22/ISH_GP4
GPP_A21/ISH_GP3
GPP_A20/ISH_GP2
GPP_A19/ISH_GP1
GPP_A18/ISH_GP0
GPP_A17/ISH_GP7
SKYLAKE_PCH
S_GPP_D9
S_GPP_D10
S_GPP_D11
S_GPP_D15 S_PCB2
S_GPP_D14 S_PCB1
S_GPP_D13 S_PCB0
S_GPP_H20
S_GPP_H19
S_GPP_H22
S_GPP_H21
O2_VCO_SEL 26
O2_HW_SEL 26
ST121 /X/SPTH
For clockgen
O2_PWR_EN 26
O2_RELATCH 26
O2_ADFC_1 26
O2_ADFC_2 26
If the signal here is not unused,the GPIO need to be pull high to 3VSB here
REV = <REV>
+3VSB
SRN208A 8.2KOHM
SRN208B S_GPP_C20
SRN208C S_GPP_H20
SRN208D
+3VSB
GPI PU
SRP3D 8.2KOHM /X
PCB Rev. Strap
+3V
SR37 1KOhm /X
SR39 1KOhm /X
SR64 1KOhm /X
S_PCB0
S_PCB1
S_PCB2
SR38 8.2KOhm
SR43 8.2KOhm
SR73 8.2KOhm
GND


+3VSB
SRN13A
SRN13B
SRN13C
SRN13D
4.7KOHM
connect to PCI&PCIE SLOT
24,42,43 S_SMBCLK_SLOT
24,42,43 S_SMBDATA_SLOT
SR1613 0Ohm /X
SR1612 0Ohm /X
SRN202A 1KOHM
SRN202B 1KOHM
+3V
SRN202C 1KOHM
SRN202D 1KOHM
SQ1 H2N7002
SQ2 H2N7002
26,31,110 S_SMBCLK_VSB
26,31,110 S_SMBDATA_VSB
S_SMBCLK_MAIN 12,17,100
S_SMBDATA_MAIN 12,17,100
SC56 10PF/50V /X NPO
SC57 10PF/50V /X NPO
GND
Place near PCH
+12V
SR304 1KOhm
mbs_r0603
SQ2C1 0.1UF/16V /X
SQ3 PMBS3904
SR305 1KOhm /X
SQ40 H2N7002
26,31,38,58,114 S_PWROK
SQ40C1 0.1UF/16V /X

POWER FLOW

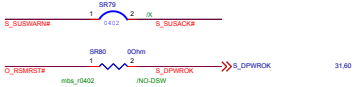


PS:the common part design by power team,no-eup part and eup part in SIO demo circuit

NOT SUPPORT DSW

Power plane

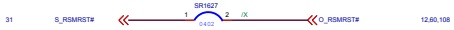
Control link

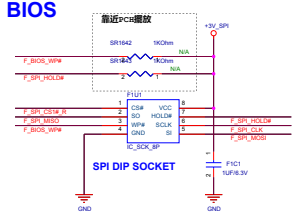


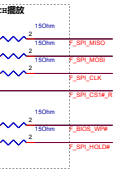
SUPPORT DSW

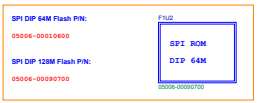
Power plane

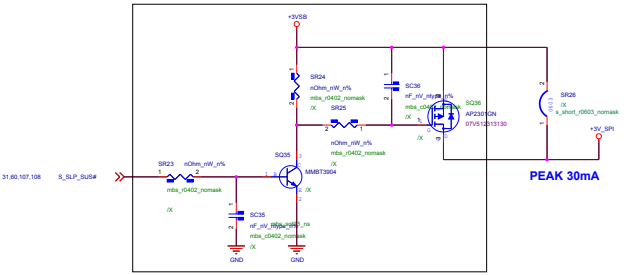
Control link



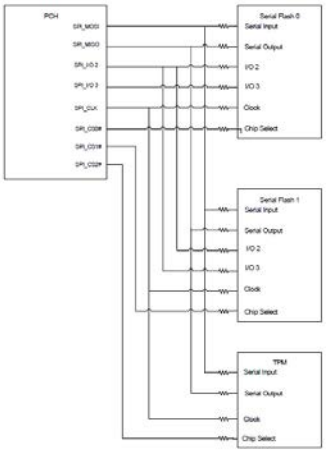








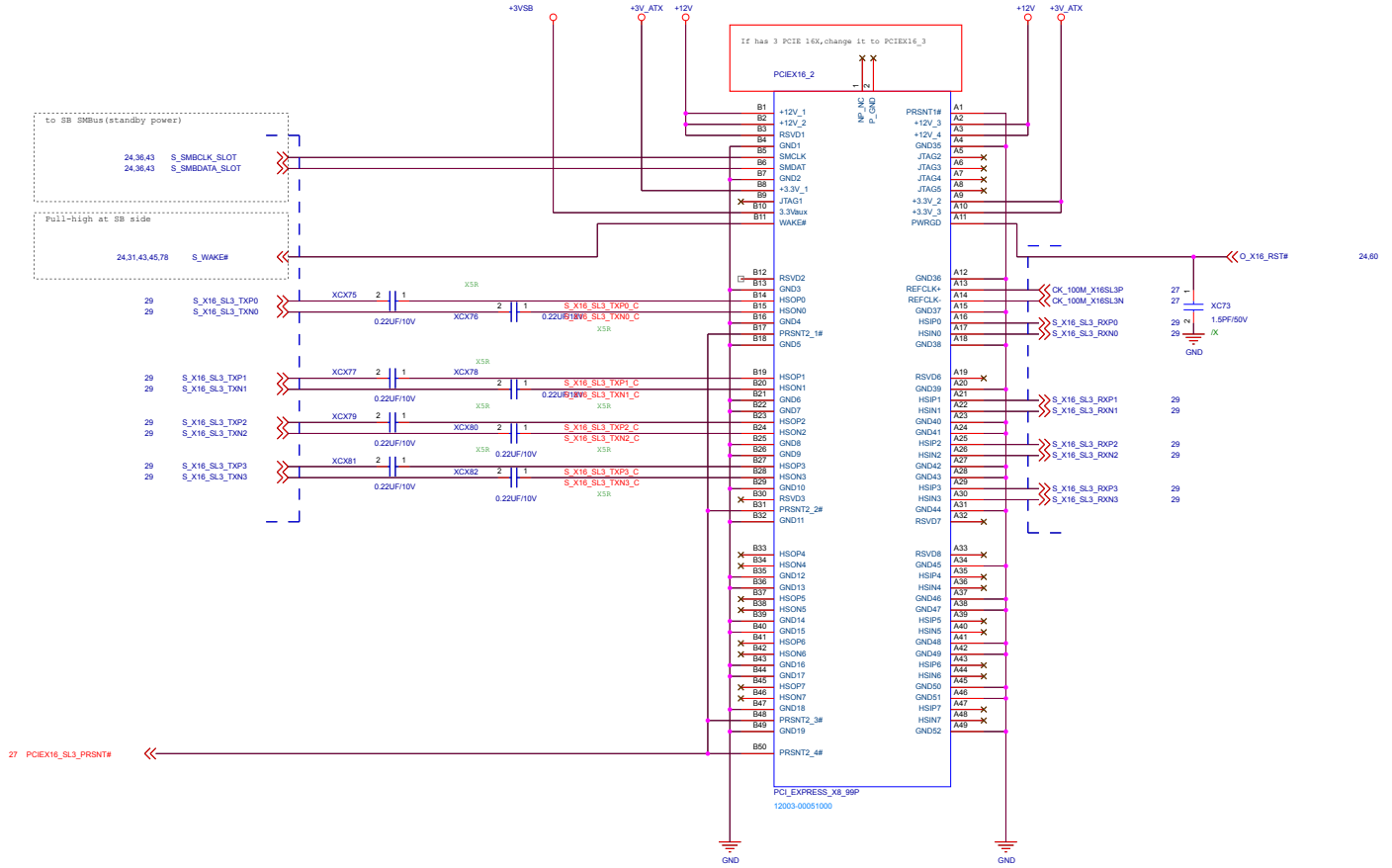
Reserved for support SBA/AMT

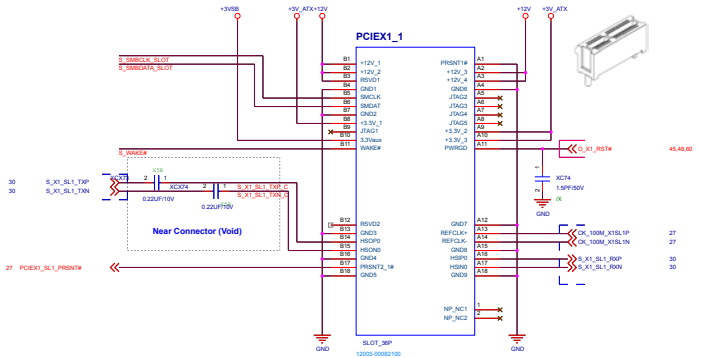


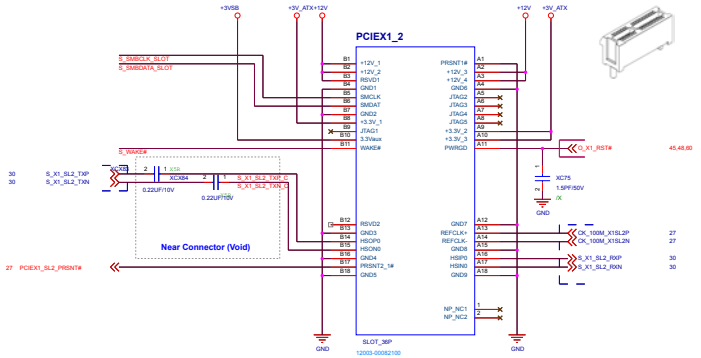
0.3G Beta

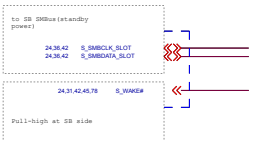
Standard Circuit	
BIOS	SPI
REV.	P1_0.3G_Beta

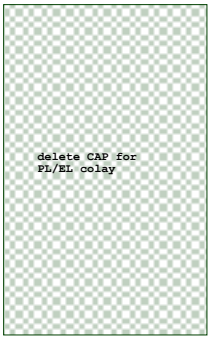
SPI /X/SPI

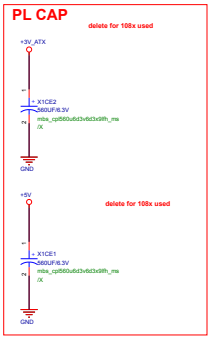

+3VSB
+3V_ATX
+12V
If has 3 PCIE 16X,change it to PCIEX16_3
PCIEX16_2
NP_NC
P_GND
to SB SMBus(standby power)
24,36,43 S_SMBCLK_SLOT
24,36,43 S_SMBDATA_SLOT
Pull-high at SB side
24,31,43,45,78 S_WAKE#
B1 +12V_1
B2 +12V_2
B3 RSVD1
B4 GND1
B5 SMCLK
B6 SMDAT
B7 GND2
B8 +3.3V_1
B9 JTAG1
B10
B11 3.3Vaux
WAKE#
PRSNT1#
+12V_3
+12V_4
GND35
JTAG2
JTAG3
JTAG4
JTAG5
+3.3V_2
+3.3V_3
PWRGD
O_X16_RST# 24,60
B12 RSVD2
B13 GND3
B14 HSOP0
B15 HSON0
B16 GND4
B17 PRSNT2_1#
B18 GND5
GND36
REFCLK+
REFCLK-
GND37
HSIP0
HSIN0
GND38
CK_100M_X16SL3P
CK_100M_X16SL3N
XC73
1.5PF/50V
/X
GND
S_X16_SL3_RXP0
S_X16_SL3_RXN0
29 S_X16_SL3_TXP0
29 S_X16_SL3_TXN0
XCX75
XCX76
0.22UF/10V
X5R
S_X16_SL3_TXP0_C
S_X16_SL3_TXN0_C
B19 HSOP1
B20 HSON1
B21 GND6
B22 GND7
B23 HSOP2
B24 HSON2
B25 GND8
B26 GND9
B27 HSOP3
B28 HSON3
B29 GND10
B30 RSVD3
B31 PRSNT2_2#
B32 GND11
RSVD6
GND39
HSIP1
HSIN1
GND40
GND41
HSIP2
HSIN2
GND42
GND43
HSIP3
HSIN3
GND44
RSVD7
S_X16_SL3_RXP1
S_X16_SL3_RXN1
S_X16_SL3_RXP2
S_X16_SL3_RXN2
S_X16_SL3_RXP3
S_X16_SL3_RXN3
29 S_X16_SL3_TXP1
29 S_X16_SL3_TXN1
XCX77
XCX78
S_X16_SL3_TXP1_C
S_X16_SL3_TXN1_C
29 S_X16_SL3_TXP2
29 S_X16_SL3_TXN2
XCX79
XCX80
S_X16_SL3_TXP2_C
S_X16_SL3_TXN2_C
29 S_X16_SL3_TXP3
29 S_X16_SL3_TXN3
XCX81
XCX82
S_X16_SL3_TXP3_C
S_X16_SL3_TXN3_C
B33 HSOP4
B34 HSON4
B35 GND12
B36 GND13
B37 HSOP5
B38 HSON5
B39 GND14
B40 GND15
B41 HSOP6
B42 HSON6
B43 GND16
B44 GND17
B45 HSOP7
B46 HSON7
B47 GND18
B48 PRSNT2_3#
B49 GND19
B50 PRSNT2_4#
RSVD8
GND45
HSIP4
HSIN4
GND46
GND47
HSIP5
HSIN5
GND48
GND49
HSIP6
HSIN6
GND50
GND51
HSIP7
HSIN7
GND52
27 PCIEX16_SL3_PRSNT#
PCI_EXPRESS_X8_99P
12003-00051000
GND
GND

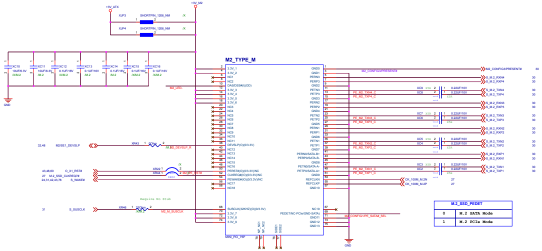

PCIEX1_1
+3VSB
+3V_ATX+12V
+12V
+3V_ATX
S_SMBCLK_SLOT
S_SMBDATA_SLOT
S_WAKE#
S_X1_SL1_TXP
S_X1_SL1_TXN
S_X1_SL1_TXP_C
S_X1_SL1_TXN_C
0.22UF/10V
Near Connector (Void)
PCIEX1_SL1_PRSNT#
S_X1_RST#
XC74
1.5PF/50V
GND
OK_100M_X1SL1P
OK_100M_X1SL1N
S_X1_SL1_RXP
S_X1_SL1_RXN
NP_NC1
NP_NC2
SLOT_36P
12003-00082100


PCIEX1_2
+3VSB
+3V_ATX+12V
+12V
+3V_ATX
S_SMBCLK_SLOT
S_SMBDATA_SLOT
S_WAKE#
S_X1_SL2_TXP
S_X1_SL2_TXN
S_X1_SL2_TXP_C
S_X1_SL2_TXN_C
0.22UF/10V
Near Connector (Void)
PCIEX1_SL2_PRSNT#
S_X1_RST#
XC75
1.5PF/50V
GND
OK_100M_X1SL2P
OK_100M_X1SL2N
S_X1_SL2_RXP
S_X1_SL2_RXN
NP_NC1
NP_NC2
SLOT_36P
12003-00082100

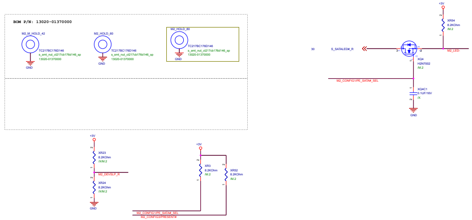

to SB SMBus(standby power)
S_SMBCLK_SLOT
S_SMBDATA_SLOT
S_WAKE#
Pull-high at SB side


delete CAP for PL/EL colay


PL CAP
delete for 108x used
+3V_ATX
X1CE2
360UF/6.3V
mba_cp560u6d3v6d3v9h_ms
GND
+5V
delete for 108x used
X1CE1
360UF/6.3V
mba_cp560u6d3v6d3v9h_ms
GND

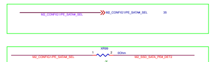


M.2_SSD_PEDET	
0	M.2 SATA Mode
1	M.2 PCIe Mode



remove portion of M.2 and sata express switch

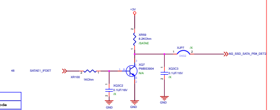
M2_CONFIG1/PE_SATA#_SEL	
0	M.2 SATA Mode
1	M.2 PCIe Mode



If no SATAE,Mount XR99,Unmount XQ7,XR99,XR100

If no SATA EXPRESS SWITCH with M.2 or SATAE switch with M.2 by ME ,Choose this block

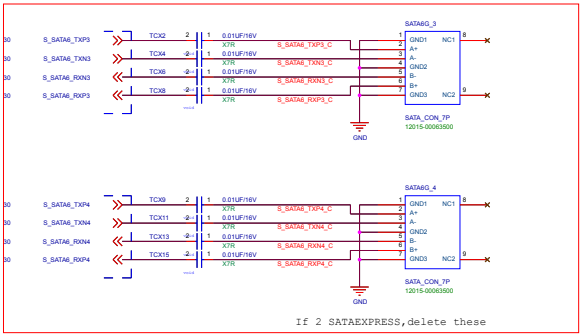
If no M.2&6*SATA ,Choose this block



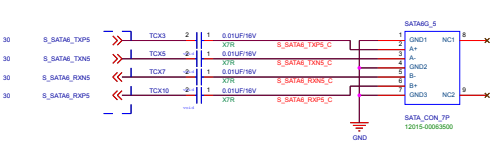
SATAE1_IFDET	
0	SATAe SATA Mode
1	SATAe PCIe Mode

If SATAE switch with M.2 by ME ,Choose this block

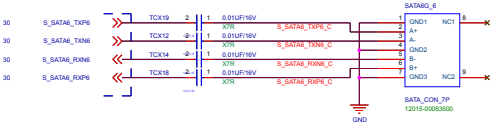
M2_CONFIG1/PE_SATA#_SEL	SATAE1_IFDET	M2_CONFIG3/PRESENT#	Result
0	0	0	M.2 change to SATA mode,PCIe #14 change to SATA,PCIe #13 change to PCIE
0	0	1	M.2 change to SATA mode,PCIe #13&14 change to SATA mode
0	1	0	M.2 change to SATA mode,PCIe #13&14 change to PCIE mode
0	1	1	M.2 keep to SATA mode,PCIe #13&14 change to PCIE mode
1	0	0	M.2 change to PCIE mode,PCIe #13&14 change to SATA mode
1	0	1	M.2 keep to PCIE mode,PCIe #13&14 change to SATA mode
1	1	0	M.2 change to PCIE mode,PCIe #13&14 change to PCIE mode
1	1	1	M.2 keep to PCIE mode,PCIe #13&14 change to PCIE mode



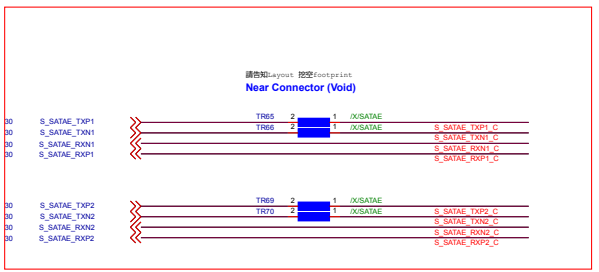
If 2 SATAEXPRESS,delete these

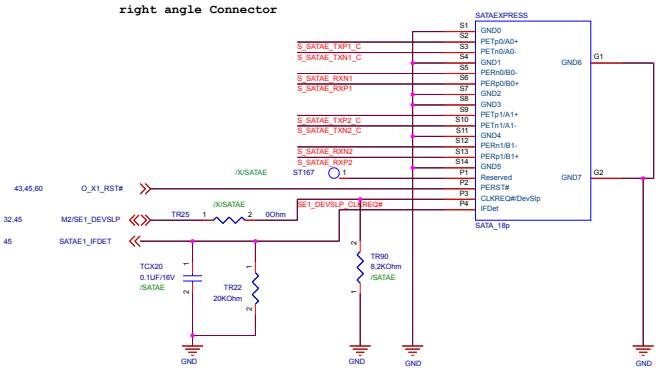


180度connector

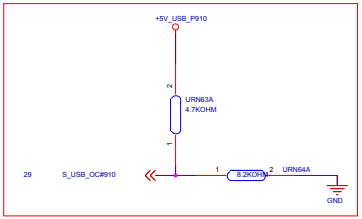


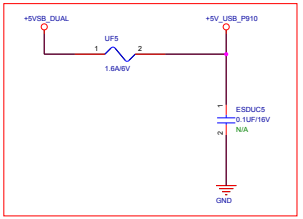
颜色: LIGHT GRAY

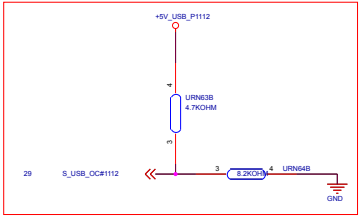

請告知Layout 挖空footprint
Near Connector (Void)
30 S_SATAE_TXP1
30 S_SATAE_TXN1
30 S_SATAE_RXN1
30 S_SATAE_RXP1
TR65 2 1 /X/SATAE
TR66 2 1 /X/SATAE
S_SATAE_TXP1_C
S_SATAE_TXN1_C
S_SATAE_RXN1_C
S_SATAE_RXP1_C
30 S_SATAE_TXP2
30 S_SATAE_TXN2
30 S_SATAE_RXN2
30 S_SATAE_RXP2
TR69 2 1 /X/SATAE
TR70 2 1 /X/SATAE
S_SATAE_TXP2_C
S_SATAE_TXN2_C
S_SATAE_RXN2_C
S_SATAE_RXP2_C

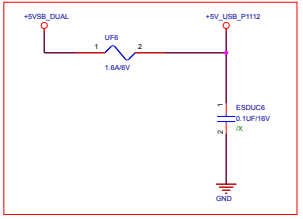

right angle Connector
SATAEXPRESS
S1 GND0
S2 PETp0/A0+
S3 PETn0/A0-
S4 GND1
S5 PERn0/B0-
S6 PERp0/B0+
S7 GND2
S8 GND3
S9 PETp1/A1+
S10 PETn1/A1-
S11 GND4
S12 PERn1/B1-
S13 PERp1/B1+
S14 GND5
P1 Reserved
P2 PERST#
P3 CLKREQ#/DevSlp
P4 IFDet
GND6
GND7
G1
G2
SATA_18p
S_SATAE_TXP1_C
S_SATAE_TXN1_C
S_SATAE_RXN1
S_SATAE_RXP1
S_SATAE_TXP2_C
S_SATAE_TXN2_C
S_SATAE_RXN2
S_SATAE_RXP2
/X/SATAE
ST167
43,45,60 O_X1_RST#
32,45 M2/SE1_DEVSLP
45 SATAE1_IFDET
TR25 1 2 0Ohm
/X/SATAE
SE1_DEVSLP_CLKREQ#
TR90
8.2KOhm
/SATAE
TCX20
0.1UF/16V
/SATAE
TR22
20KOhm
GND
GND
GND
GND

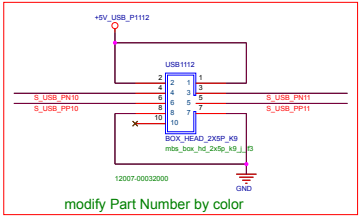
OC# circuit for Intel



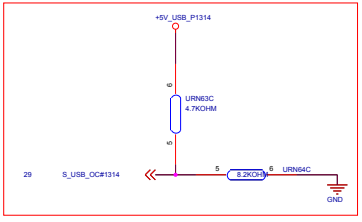


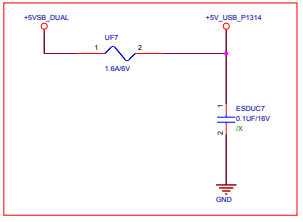


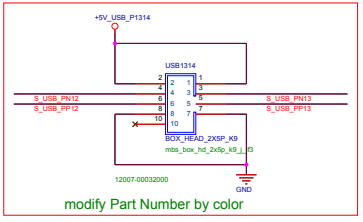




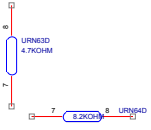
29,50 S_USB_PN10
29,50 S_USB_PP10
29,50 S_USB_PN11
29,50 S_USB_PP11



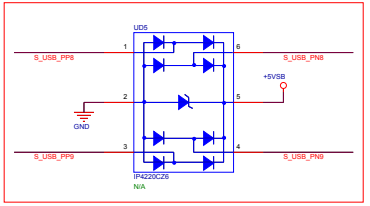


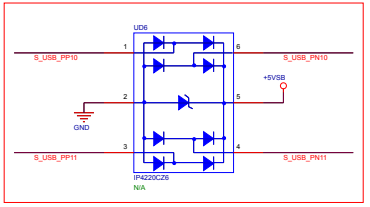


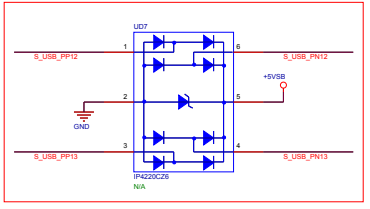
29,50 S_USB_PN12
29,50 S_USB_PP12
29,50 S_USB_PN13
29,50 S_USB_PP13

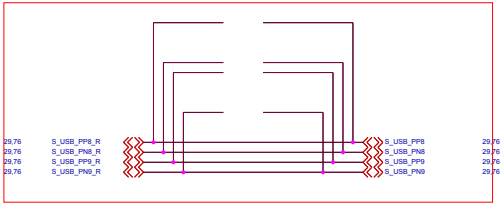


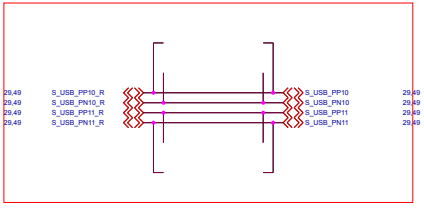
ESD Diode

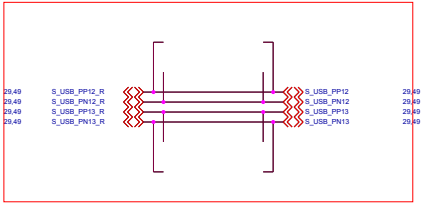




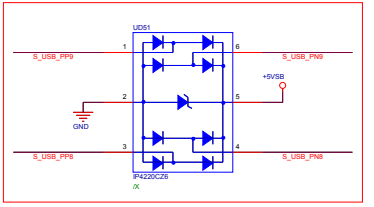


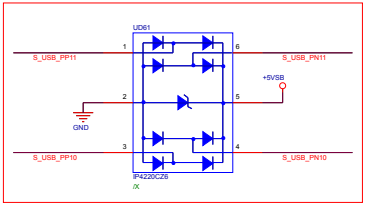


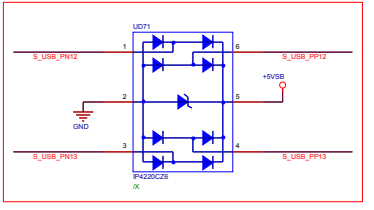




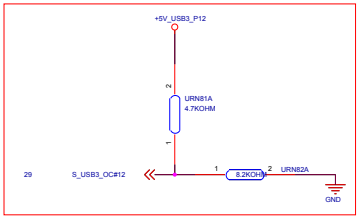
ESD Diode

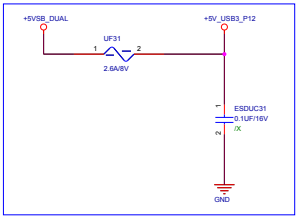


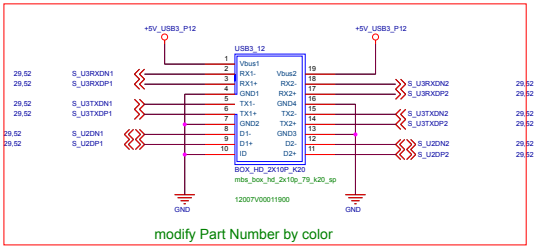


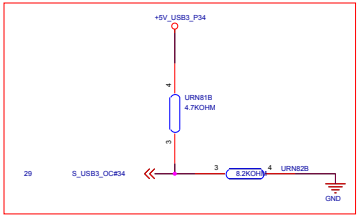


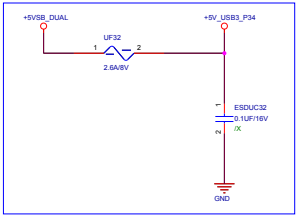
OC# circuit for Intel

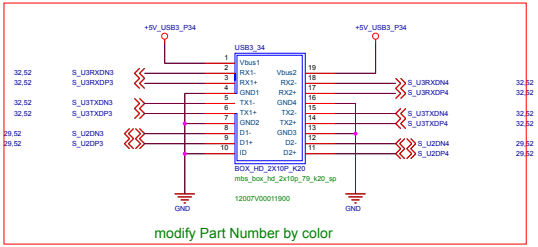


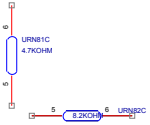


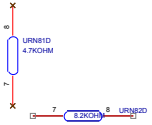






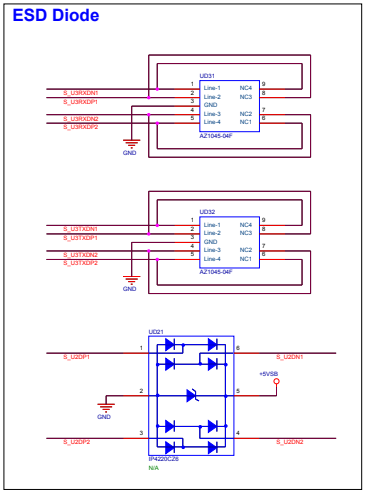




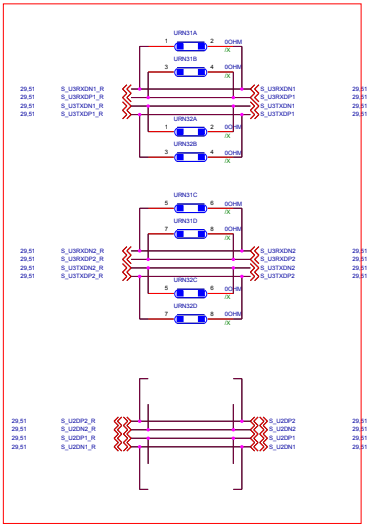


Port 12

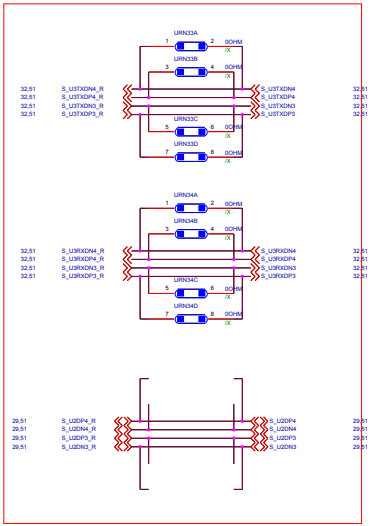
Delete it for EM

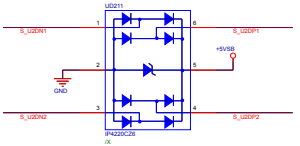


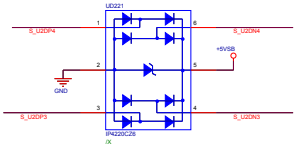
Reserve Location (RES A)



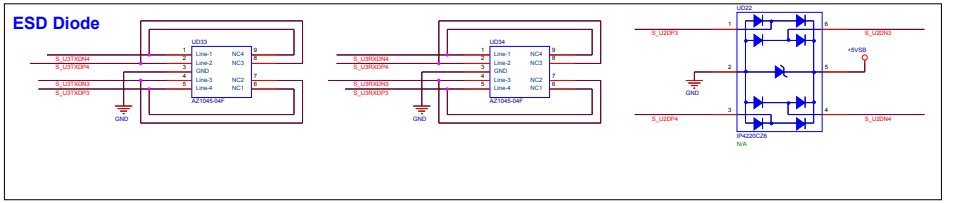
Reserve Location (RES A)







Delete it for EM

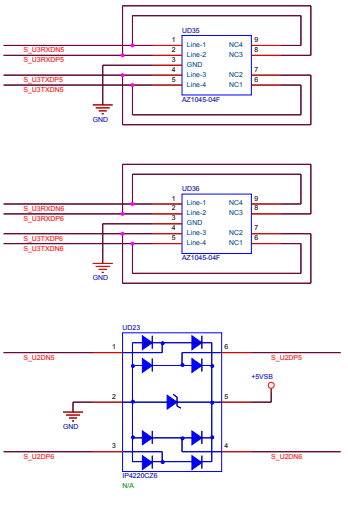


Port 34

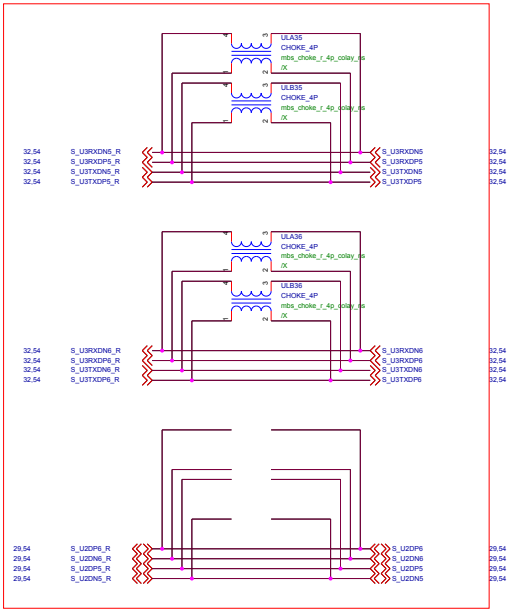
Port 56

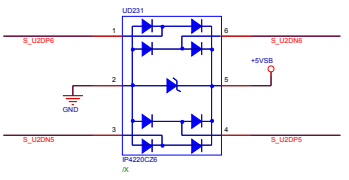
Delete it for EMS

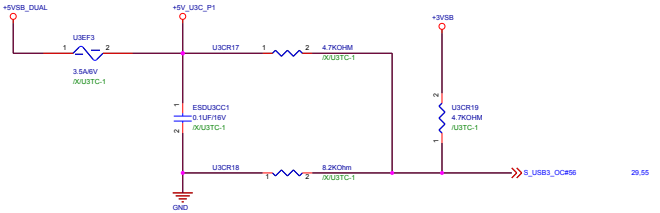
ESD Diode



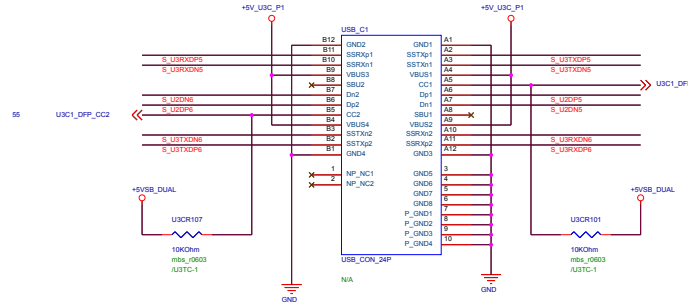
Reserve Location (Single RES)





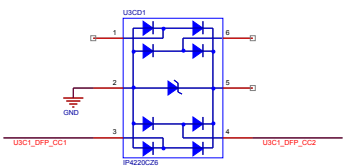

+5VSB_DUAL
+5V_U3C_P1
U3EF3
3.5A/6V
/X/U3TC-1
U3CR17
4.7KOHM
/X/U3TC-1
+3VSB
ESDU3CC1
0.1UF/16V
/X/U3TC-1
U3CR19
4.7KOHM
/U3TC-1
U3CR18
8.2KOhm
/X/U3TC-1
S_USB3_OC#56
29,55
GND

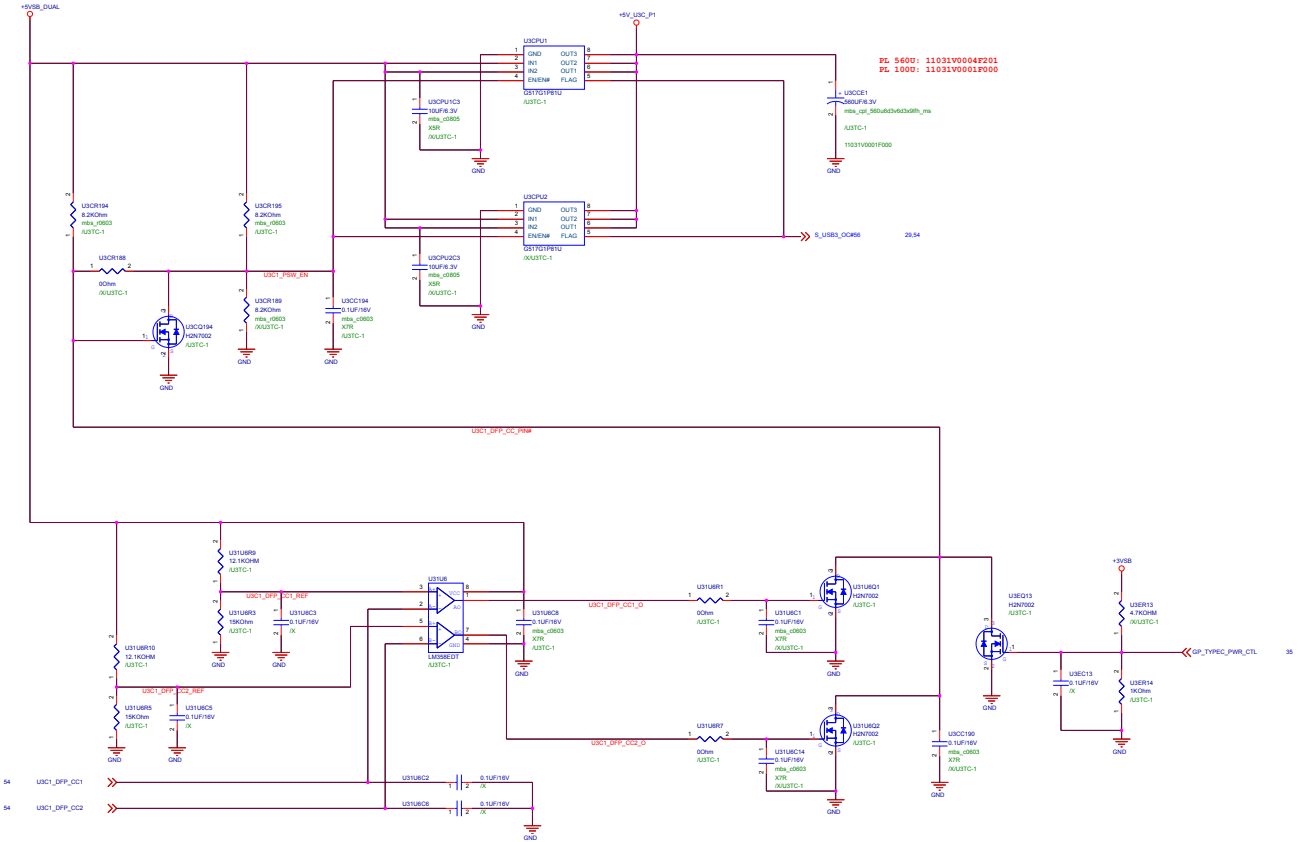

S_U3RXDN5
S_U3RXDP5
S_U3TXDN5
S_U3TXDP5
32,53
32,53
32,53
32,53


+5V_U3C_P1
+5V_U3C_P1
USB_C1
S_U3RXDP5
S_U3RXDN5
S_U2DN6
S_U2DP6
S_U3TXDN6
S_U3TXDP6
U3C1_DFP_CC2
55
S_U3TXDP5
S_U3TXDN5
S_U2DP5
S_U2DN5
S_U3RXDN6
S_U3RXDP6
U3C1_DFP_CC1
55
+5VSB_DUAL
+5VSB_DUAL
U3CR107
U3CR101
10KOhm
mba_r0603
/U3TC-1
USB_CON_24P
N/A
GND
GND

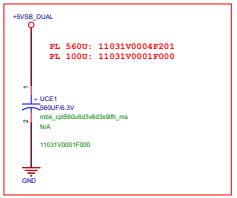

S_U3RXDN6
S_U3RXDP6
S_U3TXDN6
S_U3TXDP6
32,53
32,53
32,53
32,53


S_U2DP6
S_U2DN6
S_U2DP5
S_U2DN5
29,53
29,53
29,53
29,53

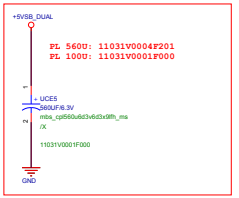

U3CD1
GND
U3C1_DFP_CC1
U3C1_DFP_CC2
IP4220CZ6
/U3TC-1

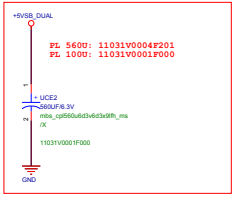

+5VSB_DUAL
+5V_U3C_P1
U3CPU1
GND OUT3
IN1 OUT2
IN2 OUT1
EN/EN# FLAG
GS17G1P61U
/U3TC-1
U3CPU1C3
10UF/6.3V
mba_c0805
X5R
/XU3TC-1
U3CCE1
560UF/6.3V
mba_cpl_560u6d3v6d3x9lfh_ms
/U3TC-1
11031V0001F000
PL 560U: 11031V0004F201
PL 100U: 11031V0001F000
U3CPU2
U3CPU2C3
10UF/6.3V
U3CR194
8.2KOhm
mba_r0603
/U3TC-1
U3CR195
U3CR188
0Ohm
/XU3TC-1
U3C1_PSW_EN
U3CR189
U3CQ194
H2N7002
U3CC194
0.1UF/16V
X7R
U3C1_DFP_CC_PIN#
S_USB3_OC#68
29,54
U31U6R9
12.1KOHM
U31U6R3
15KOhm
U31U6C3
0.1UF/16V
/X
U3C1_DFP_CC1_REF
U31U6
LM358EDT
U31U6C8
U3C1_DFP_CC1_O
U31U6R1
U31U6C1
U31U6Q1
U3EQ13
+3VSB
U3ER13
4.7KOHM
U31U6R10
12.1KOHM
U31U6R5
U31U6C5
U3C1_DFP_CC2_REF
U31U6R7
U31U6C14
U31U6Q2
U3CC190
U3EC13
U3ER14
1KOhm
GP_TYPEC_PWR_CTL
35
54 U3C1_DFP_CC1
54 U3C1_DFP_CC2
U31U6C2
U31U6C6

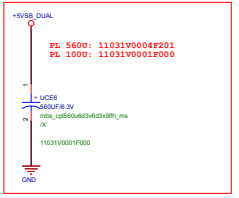
PL CAP



PL CAP



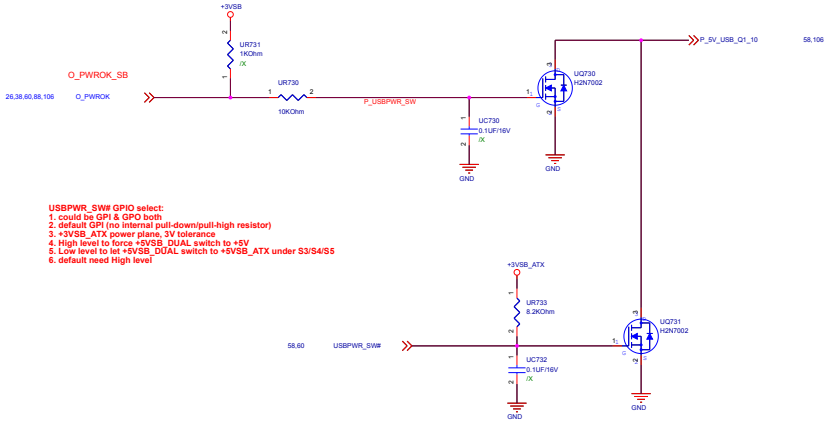


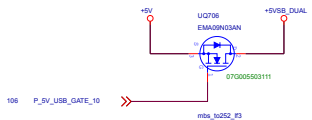


BOM	
N/A	mount
/X	unmount

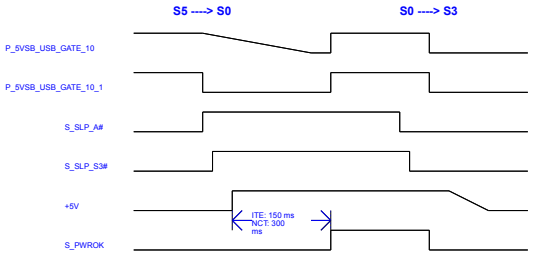
STANDARD CIRCUIT	
XSNB	USB
CS_USB_0.2B	

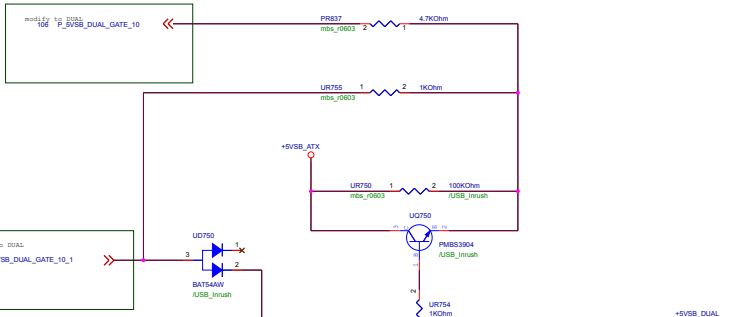
HD_DEMO_USB
/X

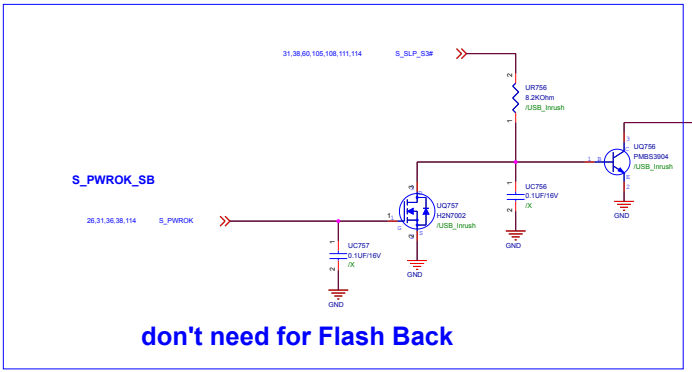


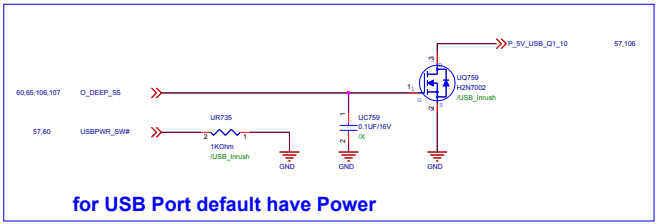


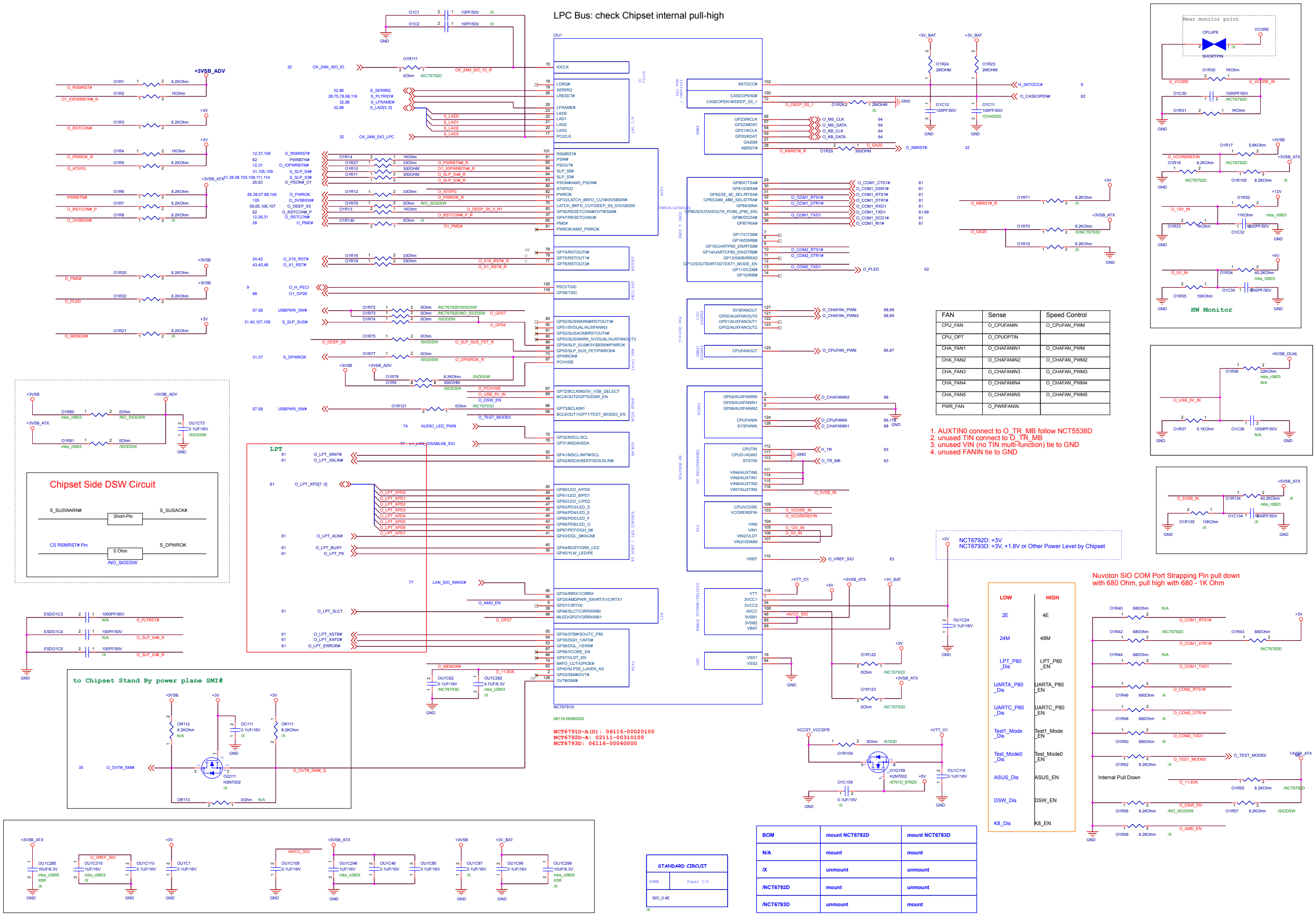
+5VSB_DUAL current:
DIMM*4=7A, DIMM*2=5A
USB 2.0=0.5A/port
USB 3.0=1A/port
if +5VSB_DUAL current (DIMM+USB 2.0 Port+USB 3.0 Port) > 15A, add UQ706


S5 ----> S0
S0 ----> S3
P_5VSB_USB_GATE_10
P_5VSB_USB_GATE_10_1
S_SLP_A#
S_SLP_S3#
+5V
S_PWROK
ITE: 150 ms
NCT: 300 ms


modify to DUAL
106 P_5VSB_DUAL_GATE_10
PR837
mbs_r0603
4.7KOhm
UR755
mbs_r0603
1KOhm
+5VSB_ATX
UR750
mbs_r0603
100KOhm
/USB_Inrush
UQ750
PMBS3904
/USB_Inrush
modify to DUAL
106 P_5VSB_DUAL_GATE_10_1
UD750
BAT54AW
/USB_Inrush
UR754
1KOhm
mbs_r0603
/USB_Inrush
UR751
100KOhm
mbs_r0603
/USB_Inrush
+5VSB_DUAL
UC750
XTR
0.22uF/16V
mbs_c0603
/USB_Inrush
UC751
XTR
0.22uF/16V
mbs_c0603
/X
GND
+5V
UR752
8.2KOhm
mbs_r0603
/USB_Inrush
UR753
8.2KOhm
/USB_Inrush
UC752
0.1UF/16V
/X
UQ751
PMBS3904
/USB_Inrush


31,38,60,105,108,111,114
S_SLP_S3#
UR756
8.2KOhm
/USB_Inrush
UQ756
PMBS3904
/USB_Inrush
UC756
0.1UF/16V
/X
S_PWROK_SB
26,31,36,38,114
S_PWROK
UQ757
H2N7002
/USB_Inrush
UC757
0.1UF/16V
/X
GND
don't need for Flash Back

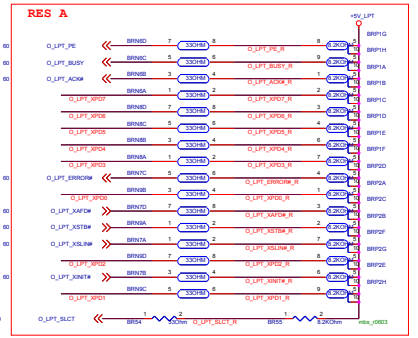

P_5V_USB_O1_10
57,106
60,65,106,107
O_DEEP_S5
57,60
USBPWR_SW#
UR735
1KOhm
/USB_Inrush
UC759
0.1UF/16V
/X
UQ759
H2N7002
/USB_Inrush
GND
for USB Port default have Power



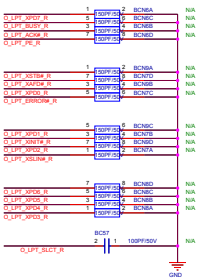
FAN	Sense	Speed Control
CPU_FAN	O_CPUFANIN	O_CPUFAN_PWM
CPU_OPT	O_CPUOPTIN	
CHA_FAN1	O_CHAFANIN1	O_CHAFAN_PWM
CHA_FAN2	O_CHAFANIN2	O_CHAFAN_PWM2
CHA_FAN3	O_CHAFANIN3	O_CHAFAN_PWM3
CHA_FAN4	O_CHAFANIN4	O_CHAFAN_PWM4
CHA_FAN5	O_CHAFANIN5	O_CHAFAN_PWM5
PWR_FAN	O_PWRFANIN	

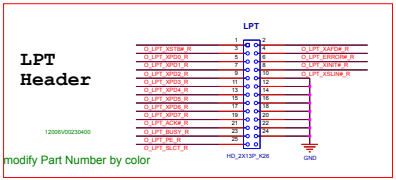
LOW	HIGH
2E	4E
24M	48M
LPT_P80 _Dis	LPT_P80 _EN
UARTA_P80 _Dis	UARTA_P80 _EN
UARTC_P80 _Dis	UARTC_P80 _EN
Test1_Mode _Dis	Test1_Mode _EN
Test_Mode0 _Dis	Test_Mode0 _EN
ASUS_Dis	ASUS_EN
DSW_Dis	DSW_EN
K8_Dis	K8_EN

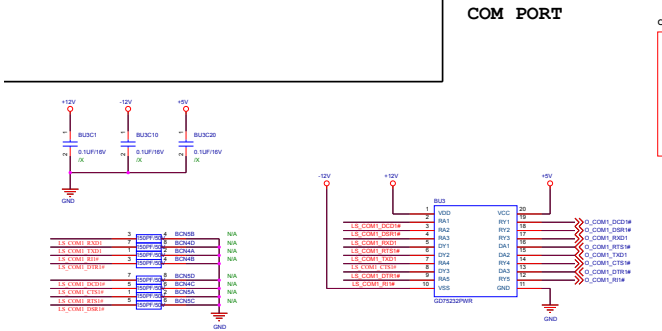
BOM	mount NCT6792D	mount NCT6793D
N/A	mount	mount
/X	unmount	unmount
/NCT6792D	mount	unmount
/NCT6793D	unmount	mount

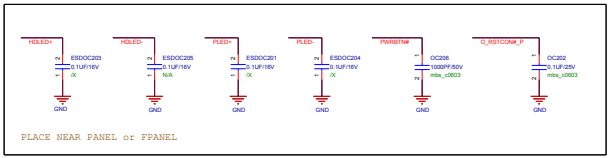

RES A
+5V_LPT
O_LPT_PE
O_LPT_BUSY
O_LPT_ACK#
O_LPT_XFD7
O_LPT_XFD6
O_LPT_XFD5
O_LPT_XFD4
O_LPT_XFD3
O_LPT_ERROR#
O_LPT_XFD0
O_LPT_XAFD#
O_LPT_XSTB#
O_LPT_XSLIN#
O_LPT_XFD2
O_LPT_XINIT#
O_LPT_XFD1
O_LPT_SLCT
O_LPT_SLCT_R
mba_r0603

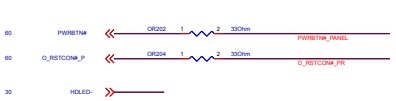

LPT PORT
O_LPT_XFD[7..0]
Power from VGA Port
+5V_D_VGA
+5V_LPT
BJP1
SHORTPIN

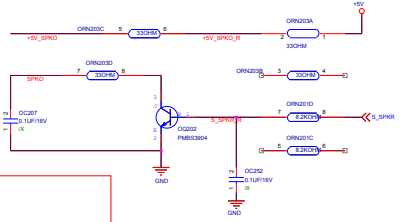

O_LPT_XFD7_R
O_LPT_BUSY_R
O_LPT_ACK#_R
O_LPT_PE_R
O_LPT_XSTB#_R
O_LPT_XAFD#_R
O_LPT_XFD0_R
O_LPT_ERROR#_R
O_LPT_XFD1_R
O_LPT_XINIT#_R
O_LPT_XFD2_R
O_LPT_XSLIN#_R
O_LPT_XFD3_R
O_LPT_XFD4_R
O_LPT_XFD5_R
O_LPT_XFD6_R
BC57
100PF/50V
O_LPT_SLCT_R
GND

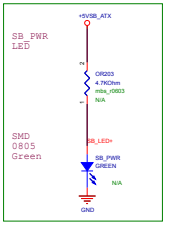

LPT Header
LPT
12006V0023040
modify Part Number by color
HD_2X13P_K26
GND


COM PORT
COM Box Header
COM
BOX_HEAD_2X5P
12007V0030600
modify Part Number by color
RING#
to Chipset
BQ14
PMBS3904
GND



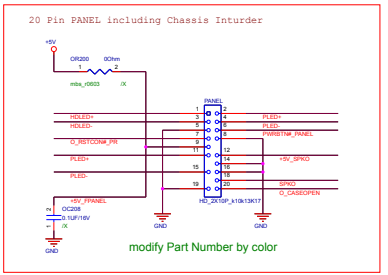


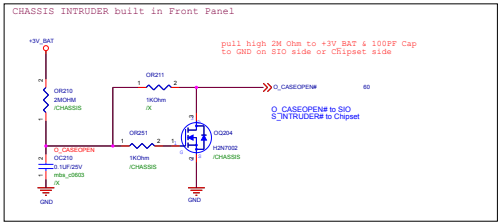




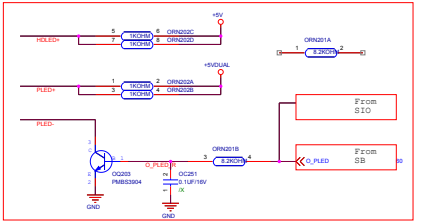
31

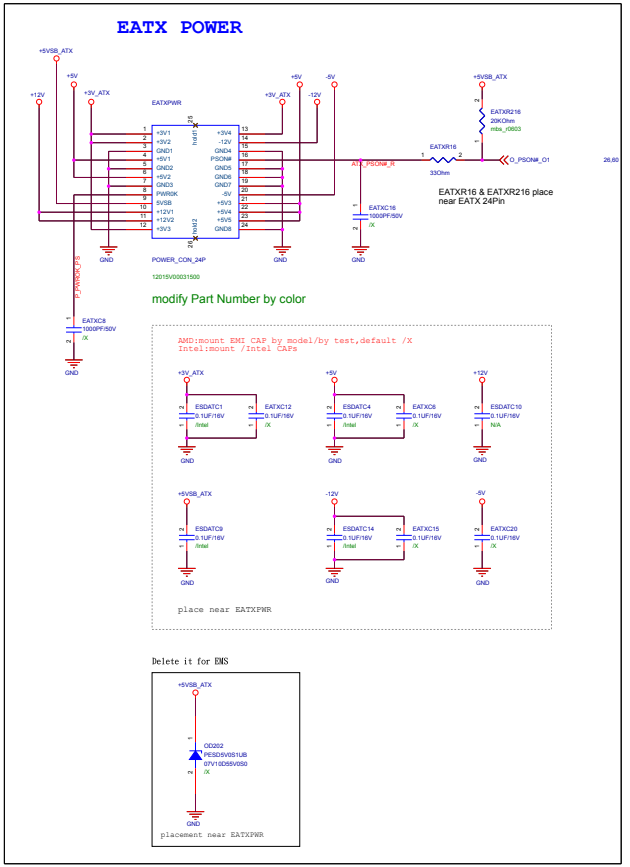
O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI (no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. GPI or GPO high to turn on Power LED
4. GPO low to turn off Power LED
5. blink under S3

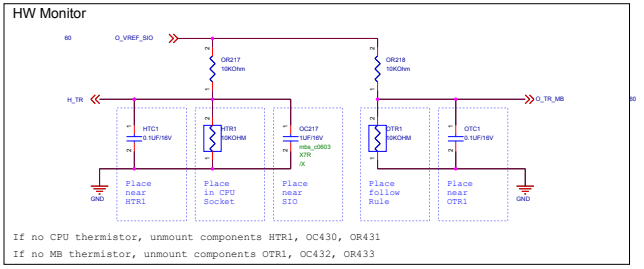




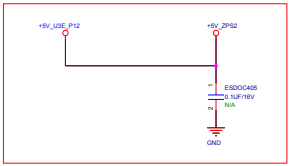
Power LED power source use +5VDUAL



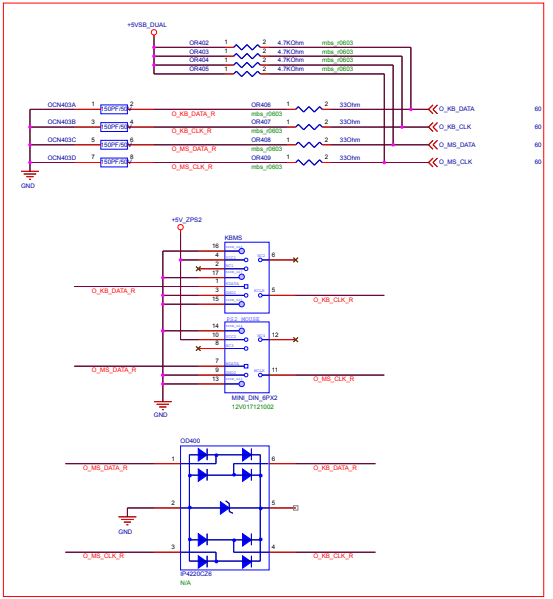

EATX POWER
+5VSB_ATX
+12V
+5V
+3V_ATX
-12V
-5V
EATXPWR
POWER_CON_24P
12015V00031500
EATXR216
20KOhm
mba_r0603
EATXR16
33Ohm
ATX_PSON#_R
O_PSON#_O1
EATXC16
1000PF/50V
/X
EATXC8
1000PF/50V
/X
P_PWROK_PS
GND
EATXR216 & EATXR216 place
near EATX 24Pin
modify Part Number by color
AMD:mount EMI CAP by model/by test,default /X
Intel:mount /Intel CAPs
ESDATC1
0.1UF/16V
/Intel
EATXC12
0.1UF/16V
/X
ESDATC4
EATXC6
ESDATC10
N/A
ESDATC9
ESDATC14
EATXC15
EATXC20
place near EATXPWR
Delete it for EMS
OD202
PESD5V0S1UB
07V1D55V0S0
placement near EATXPWR


HW Monitor
O_VREF_SIO
OR217
10KOhm
OR218
10KOhm
H_TR
O_TR_MB
HTC1
0.1UF/16V
HTR1
10KOHM
OC217
1UF/16V
mba_c0603
X7R
/X
OTR1
10KOHM
OTC1
0.1UF/16V
Place
near
HTR1
Place
in CPU
Socket
Place
near
SIO
Place
follow
Rule
Place
near
OTR1
GND
If no CPU thermistor, unmount components HTR1, OC430, OR431
If no MB thermistor, unmount components OTR1, OC432, OR433

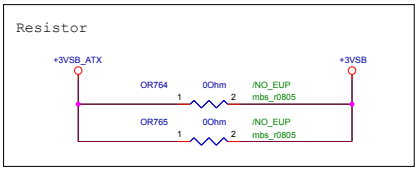
share USB Port Power

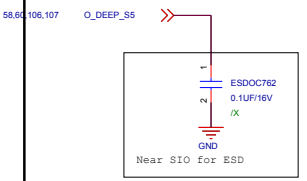


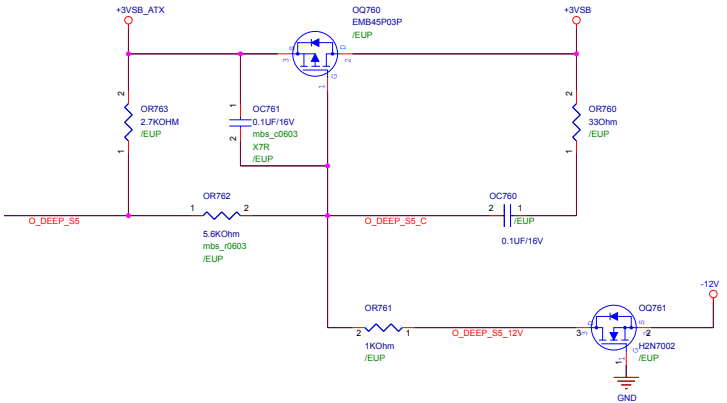
KBMS

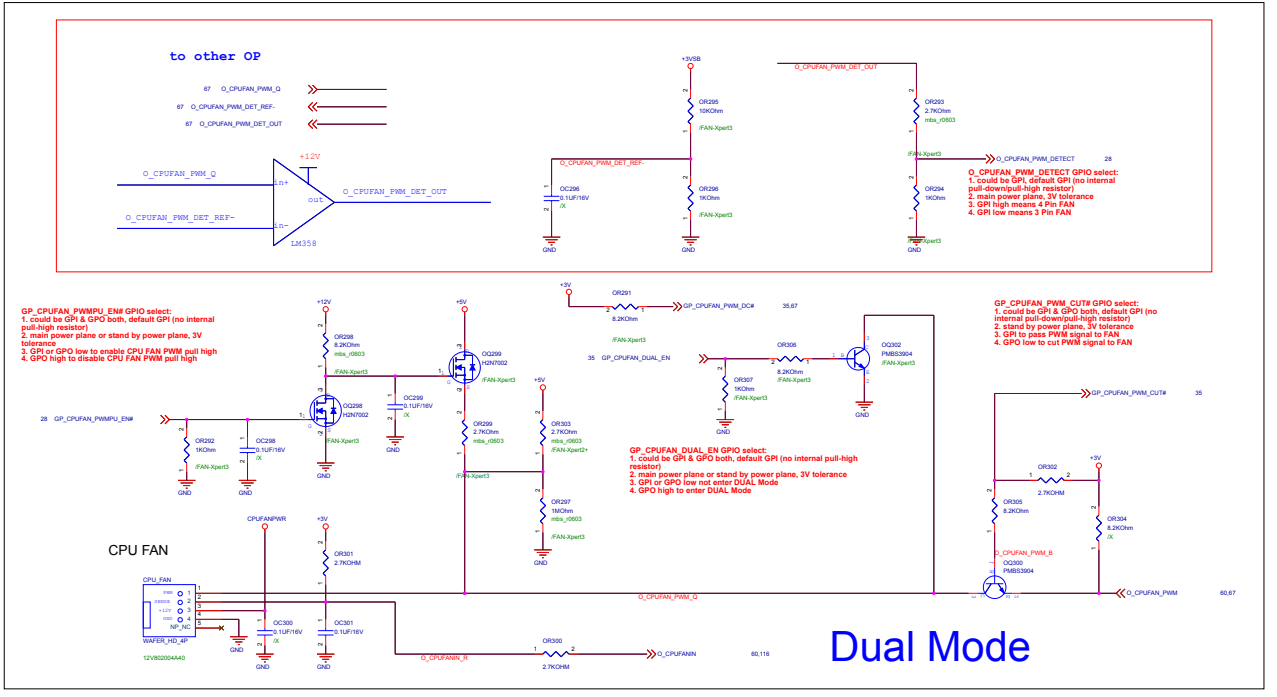


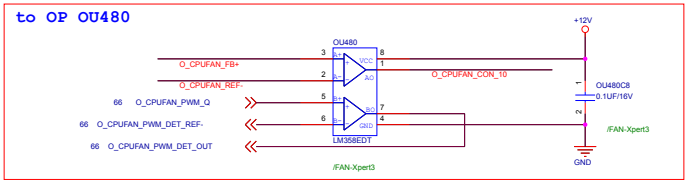
ERP Circuit

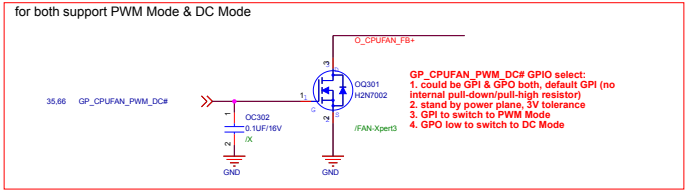

Resistor
+3VSB_ATX
+3VSB
OR764
0Ohm
/NO_EUP
mbs_r0805
OR765
0Ohm
/NO_EUP
mbs_r0805

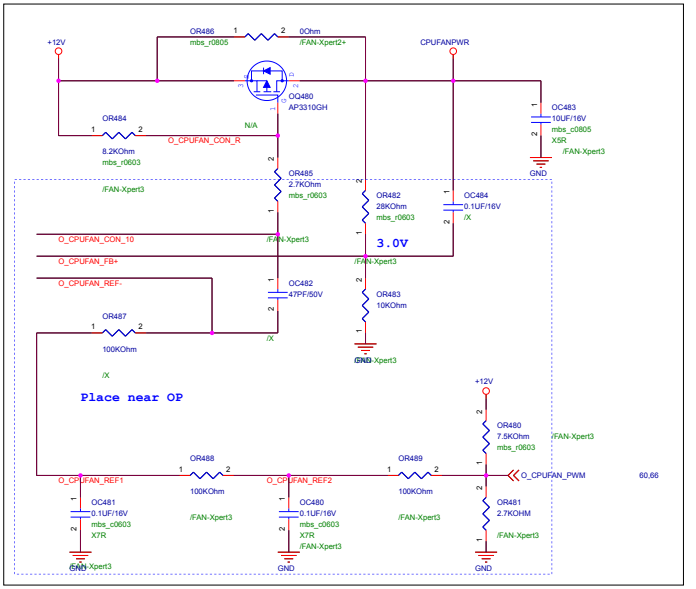

58,60,106,107
O_DEEP_S5
ESDOC762
0.1UF/16V
/X
GND
Near SIO for ESD


+3VSB_ATX
OQ760
EMB45P03P
/EUP
+3VSB
OR763
2.7KOHM
/EUP
OC761
0.1UF/16V
mbs_c0603
X7R
/EUP
OR760
33Ohm
/EUP
OR762
5.6KOhm
mbs_r0603
/EUP
O_DEEP_S5
O_DEEP_S5_C
OC760
/EUP
0.1UF/16V
-12V
OR761
1KOhm
/EUP
O_DEEP_S5_12V
OQ761
H2N7002
/EUP
GND

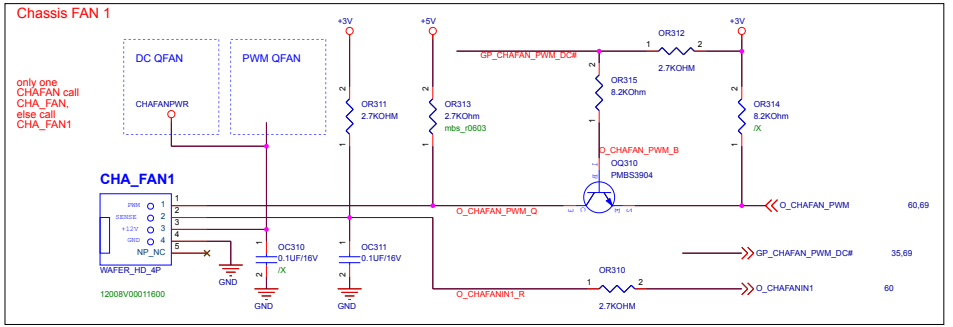

to other OP
67 O_CPUFAN_PWM_Q
67 O_CPUFAN_PWM_DET_REF-
67 O_CPUFAN_PWM_DET_OUT
+12V
O_CPUFAN_PWM_Q
O_CPUFAN_PWM_DET_REF-
O_CPUFAN_PWM_DET_OUT
LM358
+3VSB
OR295 10KOhm /FAN-Xpart3
OR296 1KOhm /FAN-Xpart3
OC296 0.1UF/16V /X
O_CPUFAN_PWM_DET_OUT
OR293 2.7KOhm mbs_r0603
O_CPUFAN_PWM_DETECT 28
OR294 1KOhm
O_CPUFAN_PWM_DETECT GPIO select:
1. could be GPI, default GPI (no internal pull-down/pull-high resistor)
2. main power plane, 3V tolerance
3. GPI high means 4 Pin FAN
4. GPI low means 3 Pin FAN
GP_CPUFAN_PWMPU_EN# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI or GPO low to enable CPU FAN PWM pull high
4. GPO high to disable CPU FAN PWM pull high
28 GP_CPUFAN_PWMPU_EN#
OR292 1KOhm /FAN-Xpart3
OC298 0.1UF/16V /X
OR298 8.2KOhm mbs_r0603
OQ298 H2N7002
OC299 0.1UF/16V /X
OQ299 H2N7002
OR299 2.7KOhm mbs_r0603
OR303 2.7KOhm mbs_r0603 /FAN-Xpart2+
OR297 15KOhm mbs_r0603 /FAN-Xpart3
+3V
OR291 8.2KOhm /FAN-Xpart3
GP_CPUFAN_PWM_DC# 35,67
35 GP_CPUFAN_DUAL_EN
OR306 8.2KOhm /FAN-Xpart3
OR307 1KOhm /FAN-Xpart3
OQ302 PMBS3904 /FAN-Xpart3
GP_CPUFAN_DUAL_EN GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI or GPO low not enter DUAL Mode
4. GPO high to enter DUAL Mode
GP_CPUFAN_PWM_CUT# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance
3. GPI to pass PWM signal to FAN
4. GPO low to cut PWM signal to FAN
GP_CPUFAN_PWM_CUT# 35
OR302 2.7KOHM
OR305 8.2KOhm
OR304 8.2KOhm /X
O_CPUFAN_PWM_B
OQ300 PMBS3904
O_CPUFAN_PWM 60,67
CPU FAN
CPUFANPWR
OR301 2.7KOHM
CPU_FAN
WAFER_HD_4P
12V8020004A40
OC300 0.1UF/16V /X
OC301 0.1UF/16V /X
O_CPUFAN_PWM_Q
O_CPUFANIN_R
OR300 2.7KOHM
O_CPUFANIN 60,116
Dual Mode
O_CPUFAN_PWM
O_CPUFAN_PWM_B
O_CPUFAN_PWM_Q
OC303 0.1UF/16V /X
OC304 0.1UF/16V /X
OC305 0.1UF/16V /X
GND

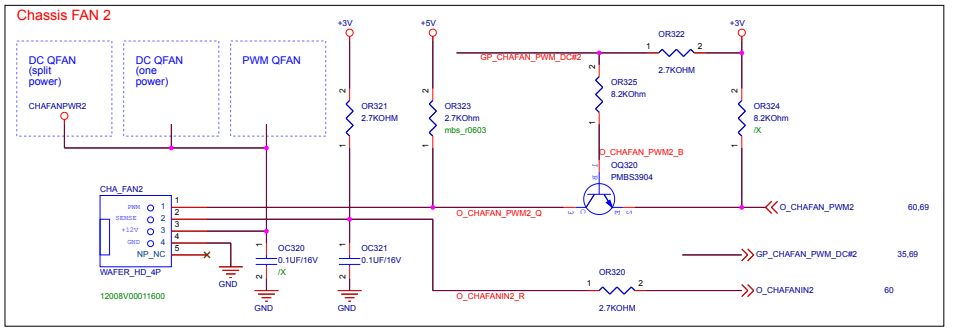

to OP OU480
OU480
O_CPUFAN_FB+
O_CPUFAN_REF-
66 O_CPUFAN_PWM_Q
66 O_CPUFAN_PWM_DET_REF-
66 O_CPUFAN_PWM_DET_OUT
LM358EDT
O_CPUFAN_CON_10
+12V
OU480C8
0.1UF/16V
/FAN-Xpert3
GND

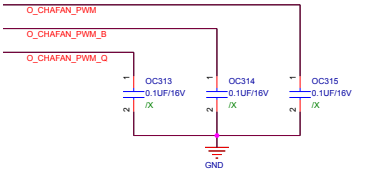

for both support PWM Mode & DC Mode
35,66 GP_CPUFAN_PWM_DC#
OC302
0.1UF/16V
/X
OQ301
H2N7002
O_CPUFAN_FB+
/FAN-Xpert3
GND
GP_CPUFAN_PWM_DC# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance
3. GPI to switch to PWM Mode
4. GPO low to switch to DC Mode

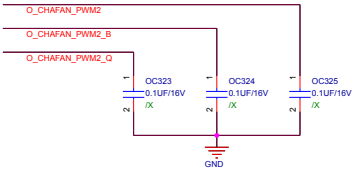

+12V
OR486
mbs_r0805
0Ohm
/FAN-Xpert2+
CPUFANPWR
OQ480
AP3310GH
OR484
8.2KOhm
mbs_r0603
N/A
O_CPUFAN_CON_R
OC483
10UF/16V
mbs_c0805
X5R
/FAN-Xpert3
GND
OR485
2.7KOhm
mbs_r0603
OR482
28KOhm
mbs_r0603
OC484
0.1UF/16V
/X
3.0V
O_CPUFAN_CON_10
O_CPUFAN_FB+
O_CPUFAN_REF-
OC482
47PF/50V
OR483
10KOhm
OR487
100KOhm
Place near OP
OR488
100KOhm
OR489
100KOhm
O_CPUFAN_REF1
O_CPUFAN_REF2
O_CPUFAN_PWM
60,66
OR480
7.5KOhm
mbs_r0603
OC481
0.1UF/16V
mbs_c0603
X7R
OC480
0.1UF/16V
mbs_c0603
X7R
OR481
2.7KOHM

4 Pin PWM Mode & DC Mode

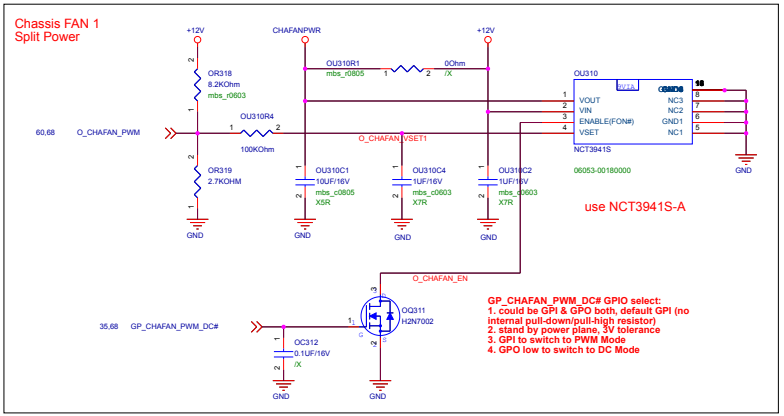


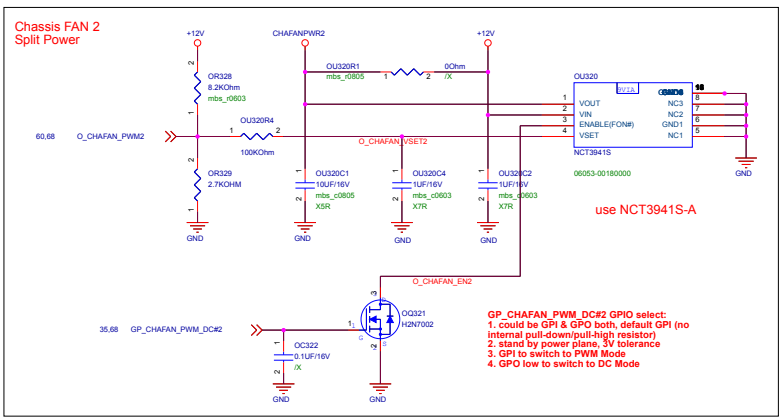


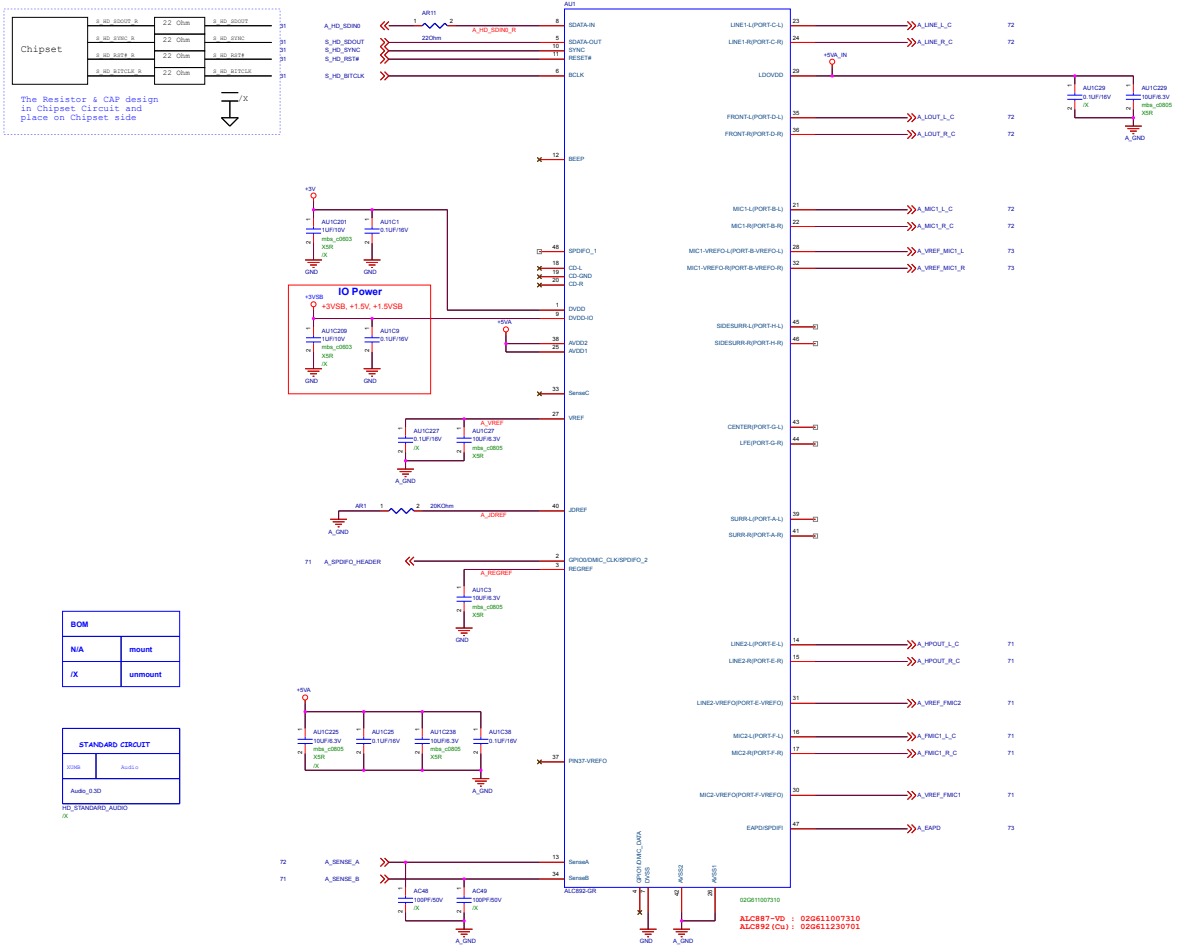




PWM Mode & DC Mode Power Solution





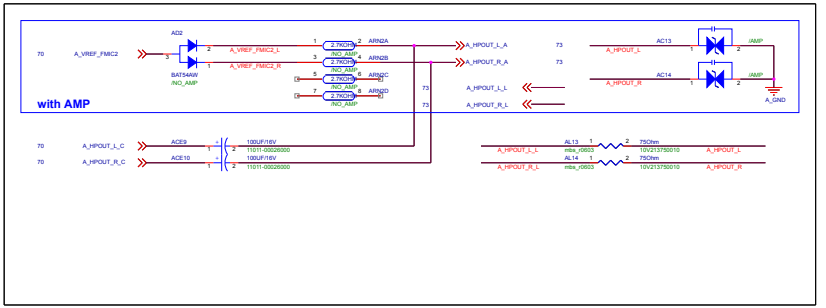


BOM	
N/A	mount
/X	unmount

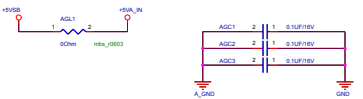
STANDARD CIRCUIT	
XING	Audio
Audio_0.3D	

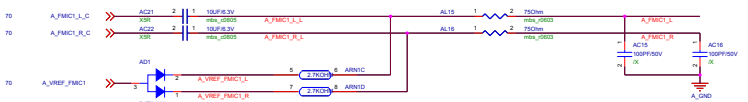
HD_STANDARD_AUDIO
/X

for ALC887-VD2/ALC892/ALC1150



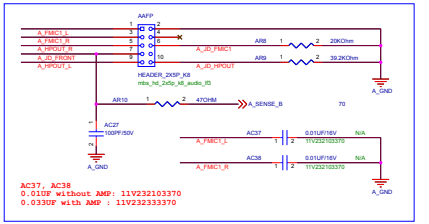
DIP CAP
EL 100U : 11G040810743
PL 100U : 11031V0001F000
Audio 100U: 11011-00026000
Gamer 100U: 11011-00022000



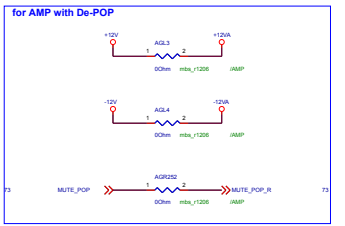


AAFP

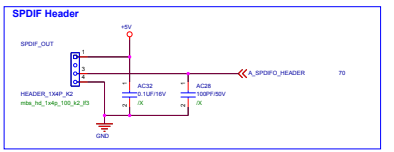
for ALC887-VD2/ALC892



for AMP with De-POP

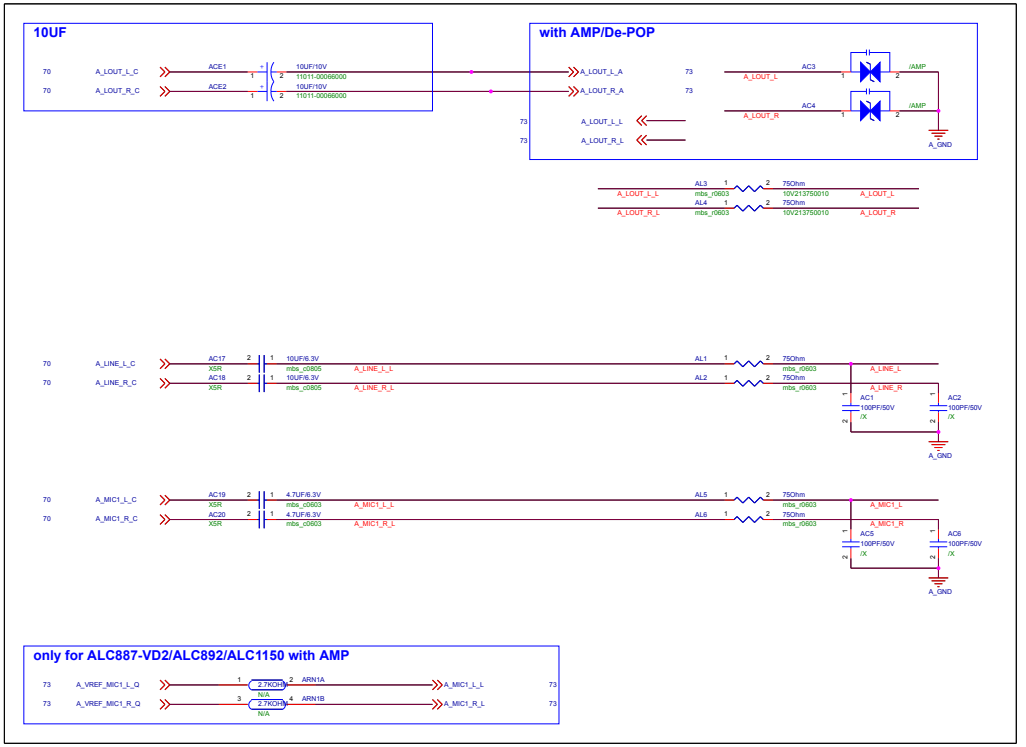


SPDIF Header

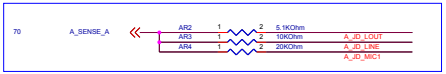


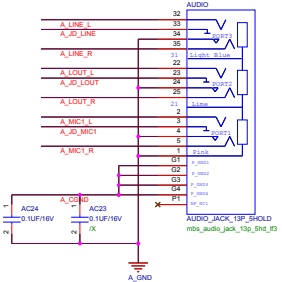
Delete it for EMS

Delete it for EMS

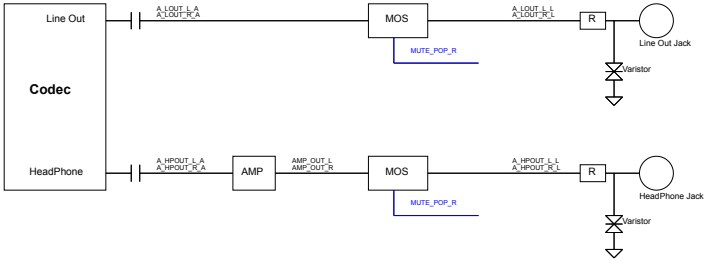


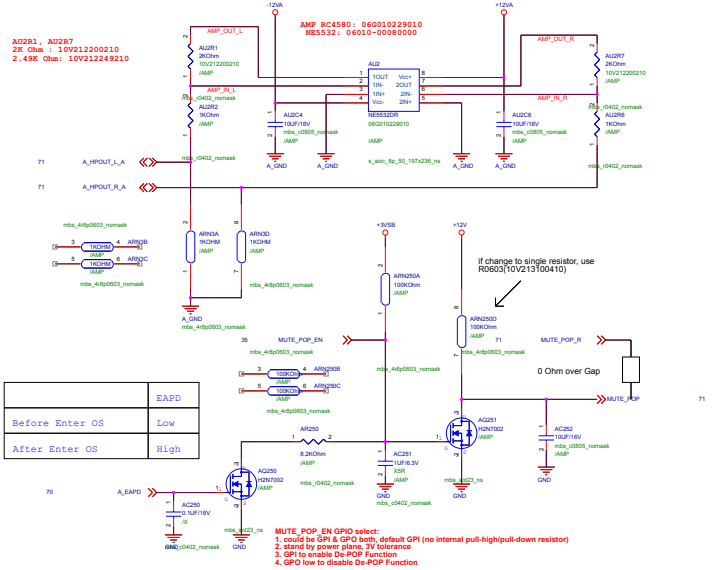
for ALC887-VD2/ALC892





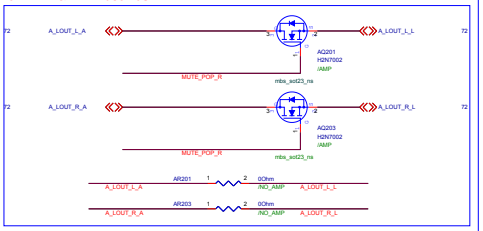
DIP CAP
EL 10U : 11G040822620
PL 10U : 11V090106207
Audio 10U: 11011-00066000
Gamer 10U: 11011-00062000
EL 100U : 11G040810743
PL 100U : 11031V0001P000
Audio 100U: 11011-00026000
Gamer 100U: 11011-00022000

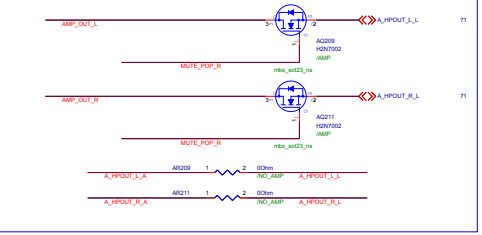




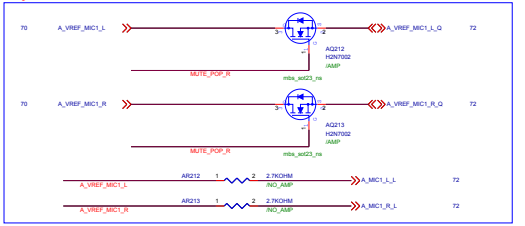
for ALC887-VD2/ALC892/ALC1150

for ACE1 & ACE2 use 10UF

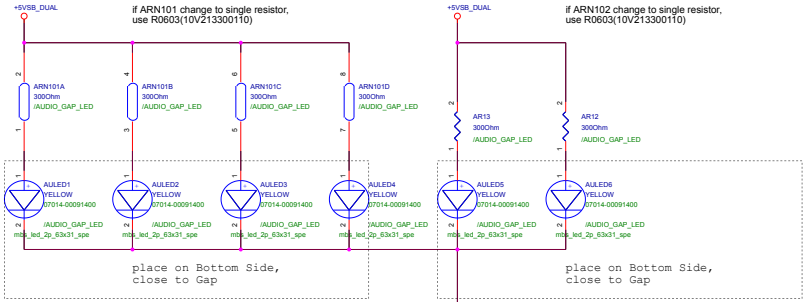




only for ALC887-VD2/ALC892/ALC1150 Rear 3 Jacks

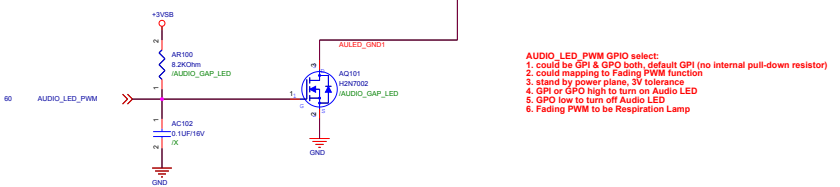


AUDIO LED

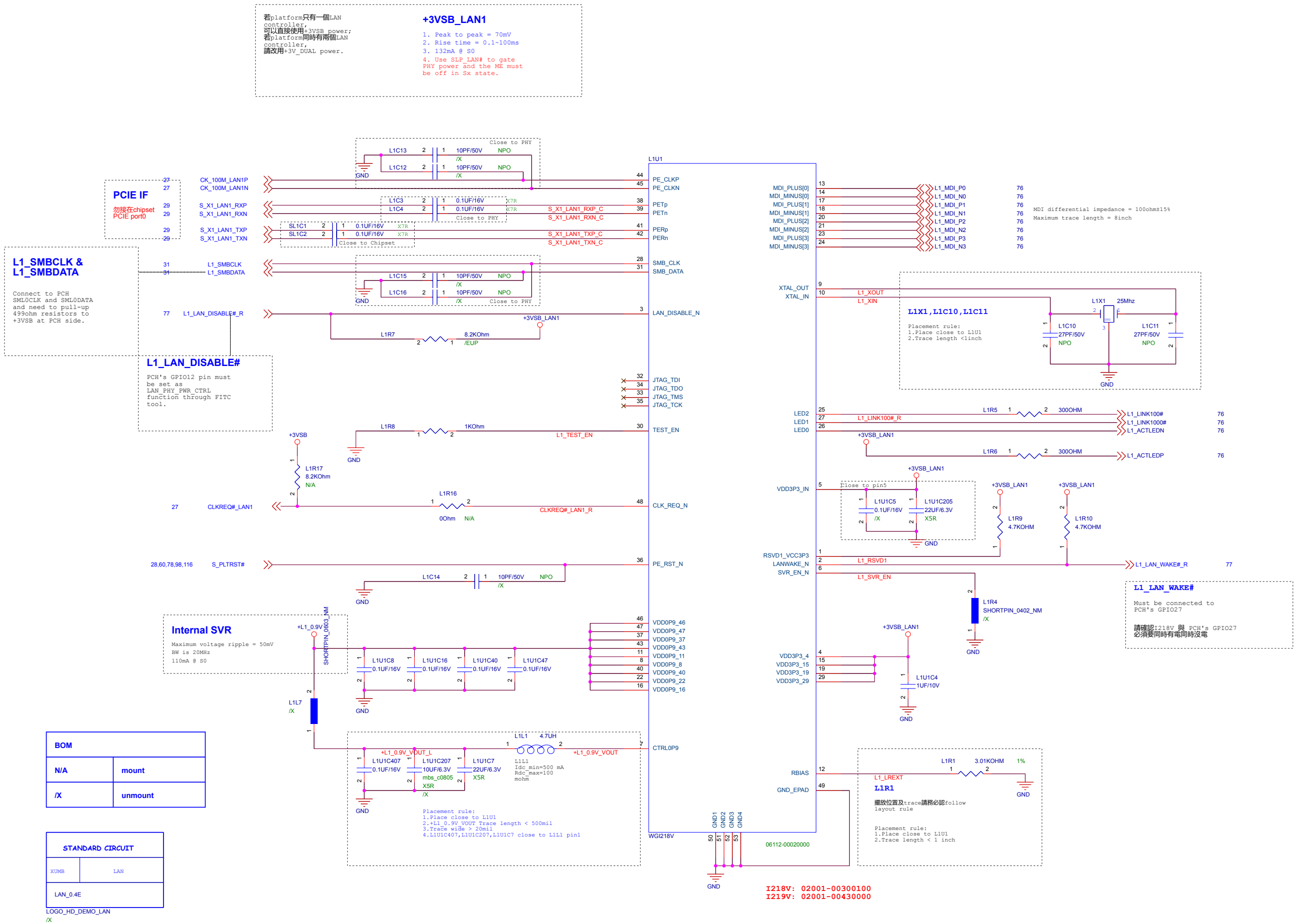


ATX normal 12 pcs LED, m-ATX normal 6 pcs LED

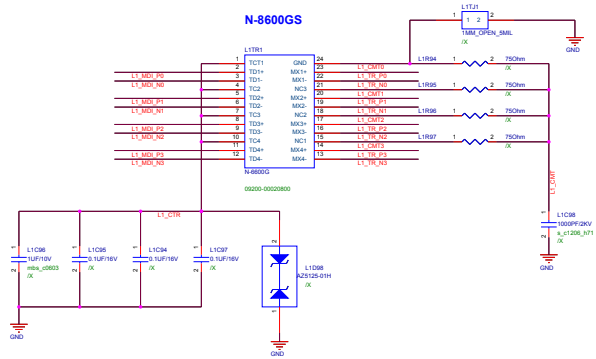
Audio LED
Yellow: 07014-00091400
Red : 07VA010R0000

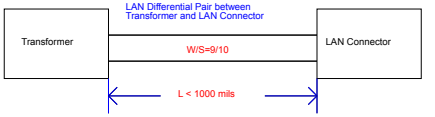


AUDIO_LED_PWM GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. could mapping to Fading PWM function
3. stand by power plane, 3V tolerance
4. GPI or GPO high to turn on Audio LED
5. GPO low to turn off Audio LED
6. Fading PWM to be Respiration Lamp



若platform只有一個LAN controller, 可以直接使用+3VSB power; 若platform同時有兩個LAN controller, 請改用+3V_DUAL power.
+3VSB_LAN1
1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.
Close to PHY
L1C13 10PF/50V NPO /X
L1C12 10PF/50V NPO /X
GND
PCIE IF
勿接在chipset PCIE port0
27 CK_100M_LAN1P
27 CK_100M_LAN1N
29 S_X1_LAN1_RXP
29 S_X1_LAN1_RXN
29 S_X1_LAN1_TXP
29 S_X1_LAN1_TXN
L1C3 0.1UF/16V X7R
L1C4 0.1UF/16V X7R
Close to PHY
SL1C1 0.1UF/16V X7R
SL1C2 0.1UF/16V X7R
Close to Chipset
S_X1_LAN1_RXP_C
S_X1_LAN1_RXN_C
S_X1_LAN1_TXP_C
S_X1_LAN1_TXN_C
L1_SMBCLK & L1_SMBDATA
Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.
31 L1_SMBCLK
31 L1_SMBDATA
L1C15 10PF/50V NPO /X
L1C16 10PF/50V NPO /X
Close to PHY
77 L1_LAN_DISABLE#_R
+3VSB_LAN1
L1R7 8.2KOhm /EUP
L1_LAN_DISABLE#
PCH's GPIO12 pin must be set as LAN_PHY_PWR_CTRL function through FITC tool.
L1U1
PE_CLKP PE_CLKN PETp PETn PERp PERn SMB_CLK SMB_DATA LAN_DISABLE_N
JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TCK TEST_EN CLK_REQ_N PE_RST_N
VDD0P9_46 VDD0P9_47 VDD0P9_37 VDD0P9_43 VDD0P9_11 VDD0P9_8 VDD0P9_40 VDD0P9_22 VDD0P9_16
CTRL0P9
WGI218V
GND1 GND2 GND3 GND4
MDI_PLUS[0] MDI_MINUS[0] MDI_PLUS[1] MDI_MINUS[1] MDI_PLUS[2] MDI_MINUS[2] MDI_PLUS[3] MDI_MINUS[3]
L1_MDI_P0 L1_MDI_N0 L1_MDI_P1 L1_MDI_N1 L1_MDI_P2 L1_MDI_N2 L1_MDI_P3 L1_MDI_N3
MDI differential impedance = 100ohm±15%
Maximum trace length = 8inch
XTAL_OUT XTAL_IN
L1_XOUT L1_XIN
L1X1 25Mhz
L1X1,L1C10,L1C11
Placement rule:
1.Place close to L1U1
2.Trace length <1inch
L1C10 27PF/50V NPO
L1C11 27PF/50V NPO
LED2 LED1 LED0
L1_LINK100#_R
L1R5 300OHM
L1_LINK100# L1_LINK1000# L1_ACTLEDN
L1R6 300OHM
L1_ACTLEDP
L1R8 1KOhm
L1_TEST_EN
+3VSB
L1R17 8.2KOhm N/A
27 CLKREQ#_LAN1
L1R16 0Ohm N/A
CLKREQ#_LAN1_R
VDD3P3_IN
Close to pin5
L1U1C5 0.1UF/16V /X
L1U1C205 22UF/6.3V X5R
L1R9 4.7KOHM
L1R10 4.7KOHM
RSVD1_VCC3P3 LANWAKE_N SVR_EN_N
L1_RSVD1
L1_SVR_EN
L1_LAN_WAKE#_R 77
L1R4 SHORTPIN_0402_NM /X
L1_LAN_WAKE#
Must be connected to PCH's GPIO27
請確認I218V 與 PCH's GPIO27 必須要同時有電同時沒電
28,60,78,98,116 S_PLTRST#
L1C14 10PF/50V NPO /X
Internal SVR
Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0
+L1_0.9V
SHORTPIN_0603_NM
L1U1C8 0.1UF/16V
L1U1C16 0.1UF/16V
L1U1C40 0.1UF/16V
L1U1C47 0.1UF/16V
L1L7 /X
VDD3P3_4 VDD3P3_15 VDD3P3_19 VDD3P3_29
L1U1C4 1UF/10V
L1L1 4.7UH
+L1_0.9V_VOUT_L
+L1_0.9V_VOUT
L1U1C407 0.1UF/16V
L1U1C207 10UF/6.3V mbs_c0805 X5R /X
L1U1C7 22UF/6.3V X5R
L1L1 Idc_min=500 mA Rdc_max=100 mohm
Placement rule:
1.Place close to L1U1
2.+L1_0.9V_VOUT Trace length < 500mil
3.Trace wide > 20mil
4.L1U1C407,L1U1C207,L1U1C7 close to L1L1 pin1
RBIAS
GND_EPAD
L1R1 3.01KOHM 1%
L1_LREXT
L1R1
擺放位置及trace請務必認follow layout rule
Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch
06112-00020000
I218V: 02001-00300100
I219V: 02001-00430000
BOM
N/A mount
/X unmount
STANDARD CIRCUIT
XUMB LAN
LAN_0.4E
LOGO_HD_DEMO_LAN
/X

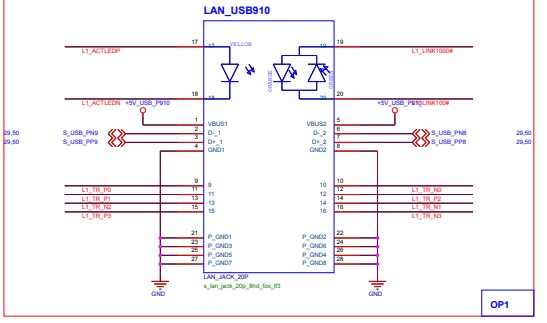




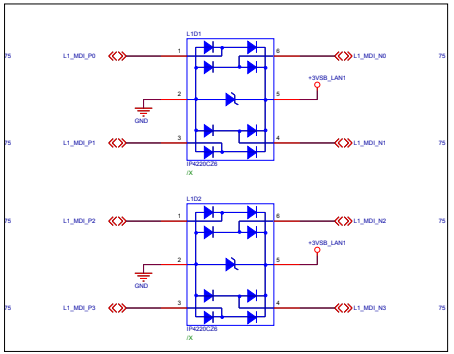
OP1 - Connector

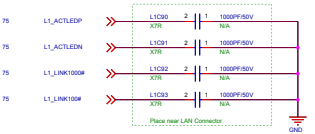
GLAN + USB2 *2 Connector without Transformer

single LAN named LAN_USB12
dual LAN named LAN1_USB12



Delete it for EMS





Note:

1. LAN IC power change to +3VSB_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)

2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN IC Page, and change BOM to use +3VSB_ATX power plane GPIO

3. for Intel PHY LAN, L1_LAN_DISABLE# pull high resistor L1R7 Optional change to /EUP

4. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN IC Page

5. for Intel PCIE LAN, L1_DEV_OFF# choose +3VSB_ATX power plane GPIO

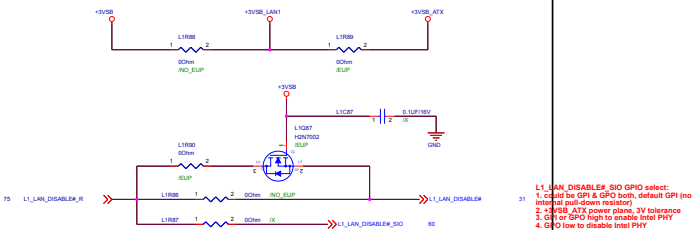
6. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN IC Page

Hardware Solution

1. O_DEEP_S5 require pull high to +3VSB_ATX, if not, do Level Shift

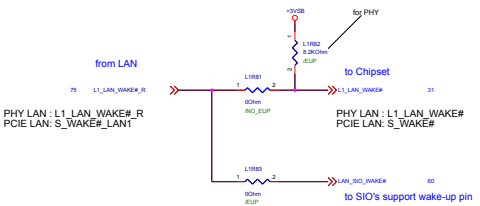
2. O_LAN_WAKE_EN power plane must be same as LAN IC Power

POWER

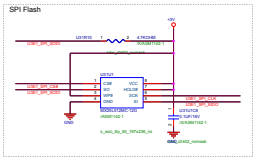


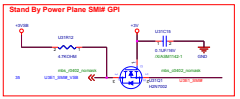
L1_LAN_DISABLE#_SIO GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. +3VSB_ATX power plane, 3V tolerance
3. GPI or GPO high to enable Intel PHY
4. GPO low to disable Intel PHY

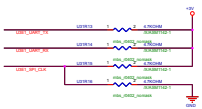
SIO Solution

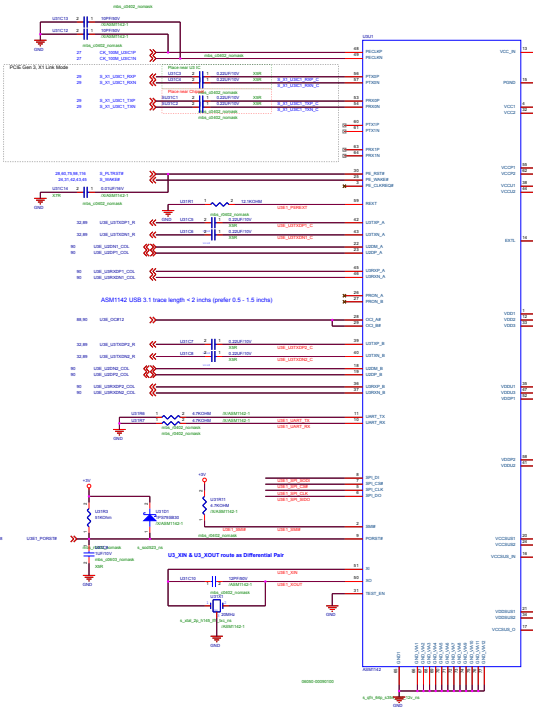


	PCIE Speed	PCIE Link Mode	AC Cap
ASM1042AE	Gen 2	X1 Link Mode	0.1UF
ASM1142	Gen 2	X2 Link Mode	0.1UF
	Gen 3	X1 Link Mode	0.22UF









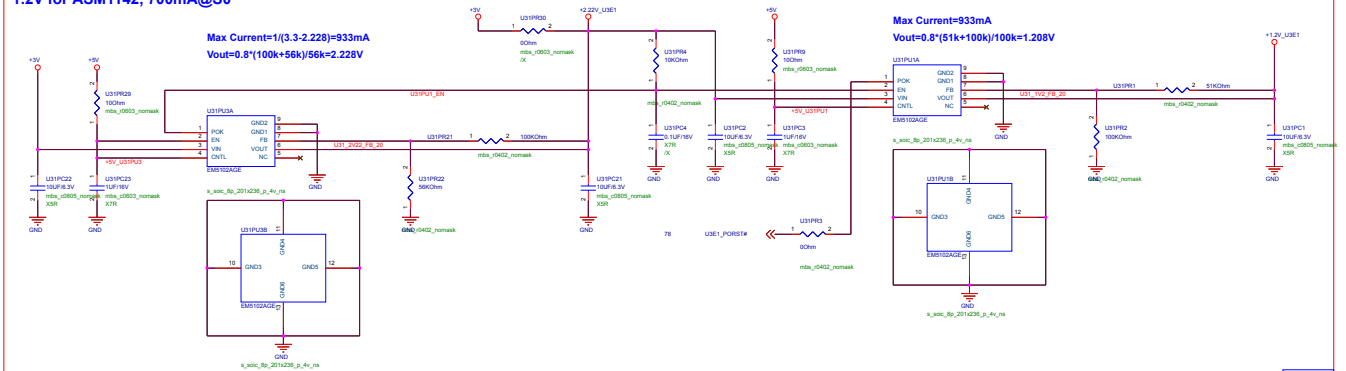
ASM1142 A1: 06050-00090000

ASM1142 A2: 06050-00090100

BOM	mount ASM1142	unmount ASM1142
N/A	mount	mount
/X	unmount	unmount
/ASM1142-1	mount	unmount
/X/ASM1142-1	unmount	unmount
/NO ASM1142-1	unmount	mount

OP5 - Core Power

1.2V for ASM1142, 700mA@S0



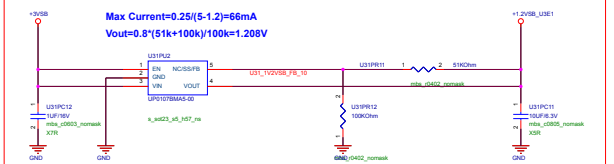
Power Component place near each other!

U31PU1 & U31PU3 place away from ASM1142

OP5

OP6 - Stand By Power

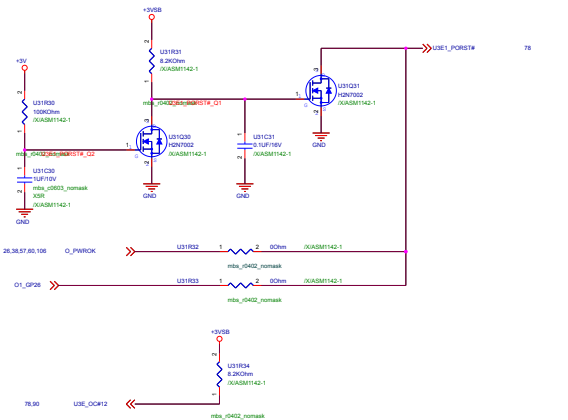
1.2VSB for ASM1142, 5mA@S0, 1mA@S3/S4/S5



Power Component place near each other!

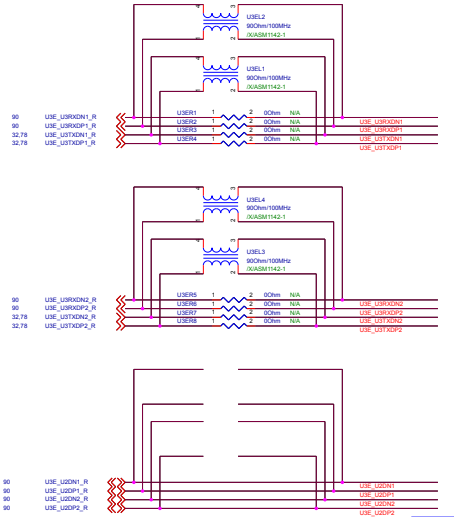
OP6

ASM1142 Power On Reset Sequence



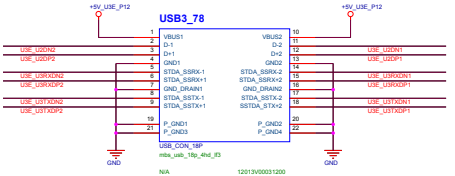
OP1 - EMI Choke

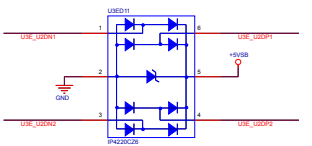
Reserve EMI Choke (Single RES)



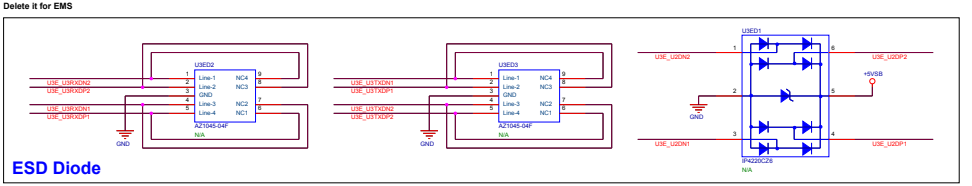
OP3 - Connector

Ext USB 3.1 Connector 1&2

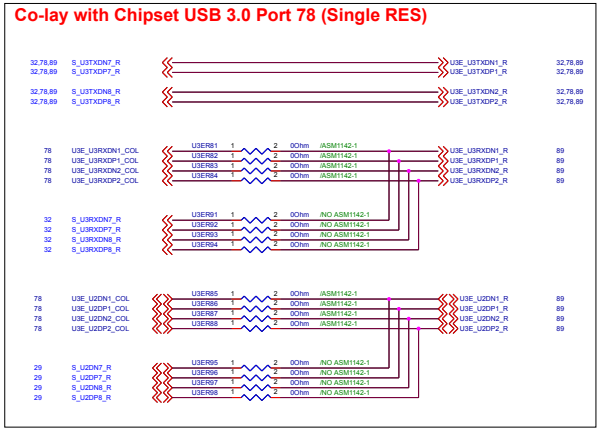




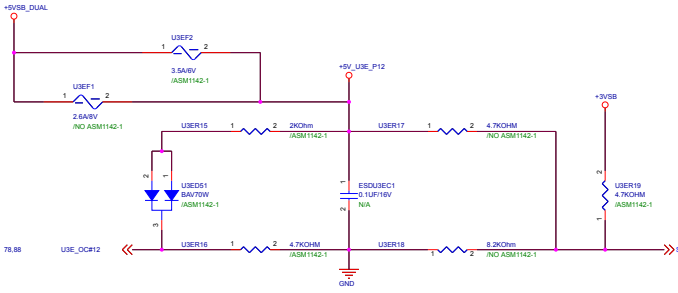
Delete it for EMS



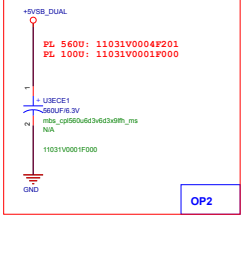
Co-lay with Chipset USB 3.0 Port 78 (Single RES)



Co-lay with Intel Chipset USB 3.0 Port 78



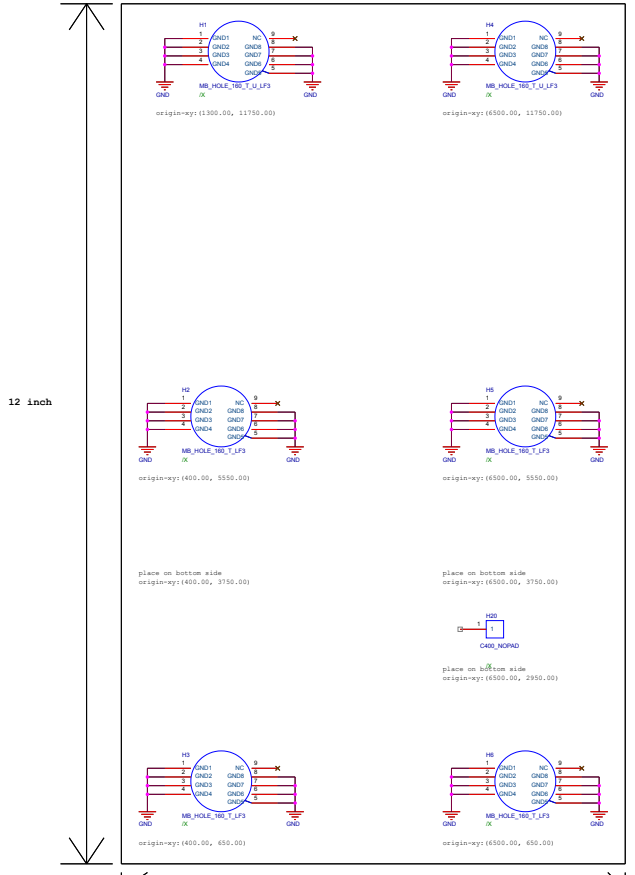
PL CAP

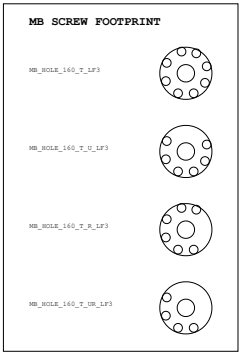


BOM	mount ASM1142	unmount ASM1142
N/A	mount	mount
/X	unmount	unmount
/ASM1142-1	mount	unmount
/X/ASM1142-1	unmount	unmount
/NO ASM1142-1	unmount	mount

Delete it for EMS

ATX Screw Hole

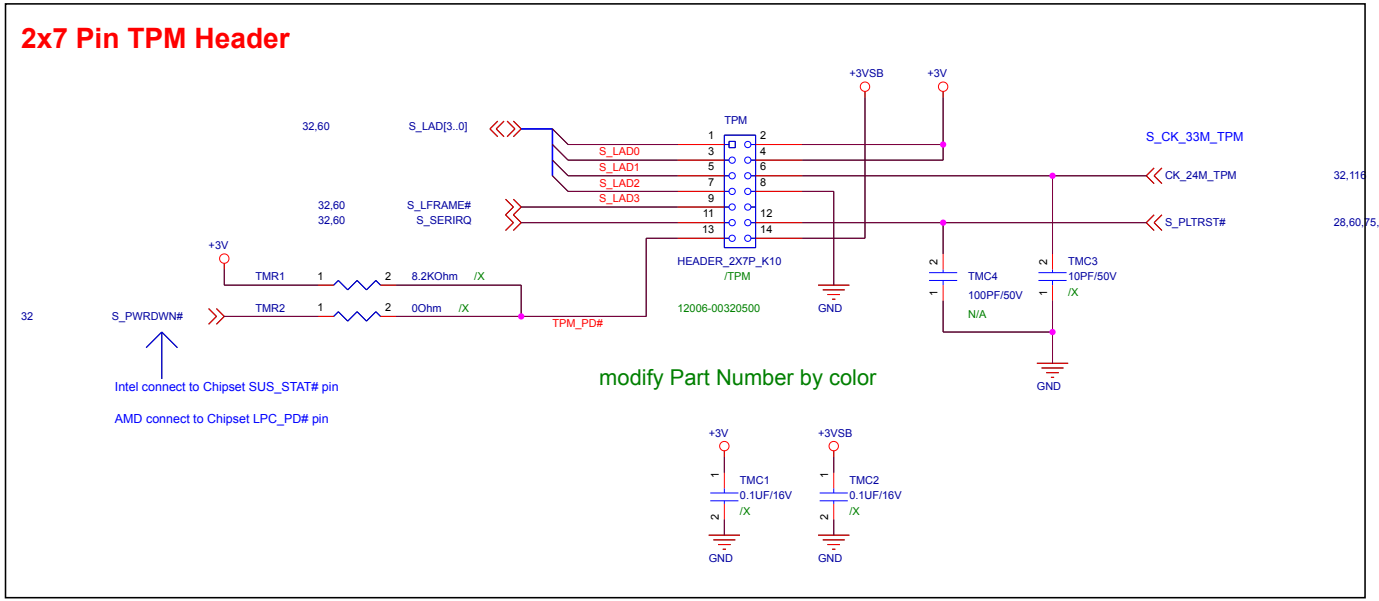




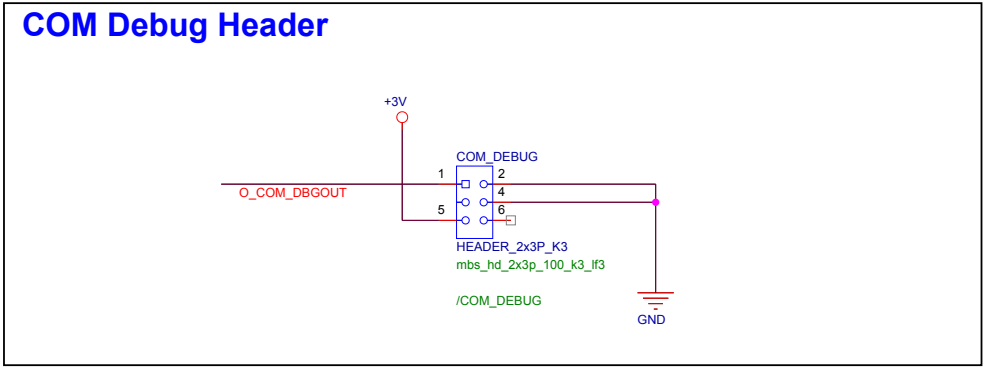
ATX Screw Select

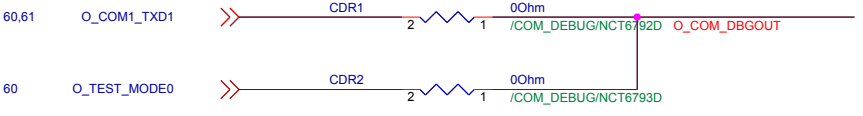
	Standard (12 x 9.6)	Scale down (12 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	X
H8	V	X
H9	V	X
H20	V	V
H21	V	V
H22	V	V

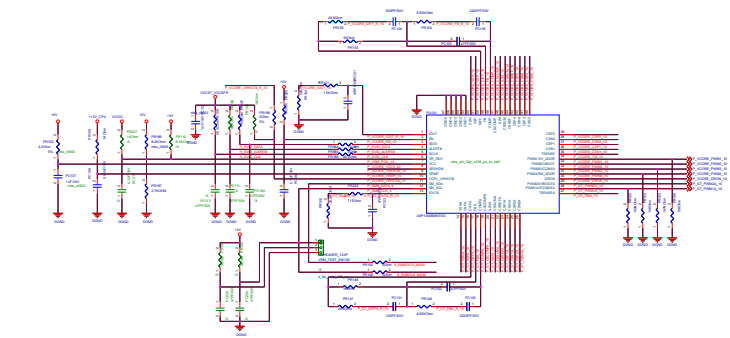
Delete it for EMS

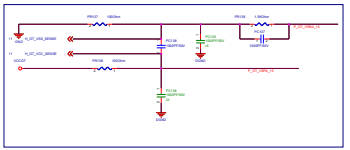


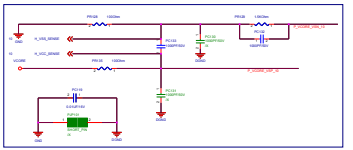
Delete it for EMS

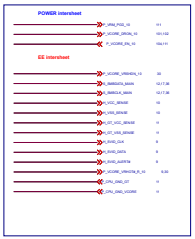


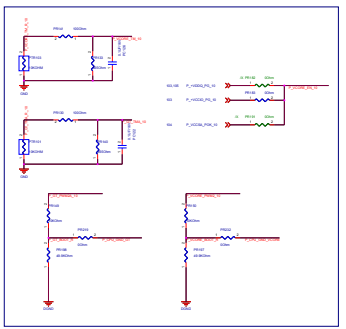


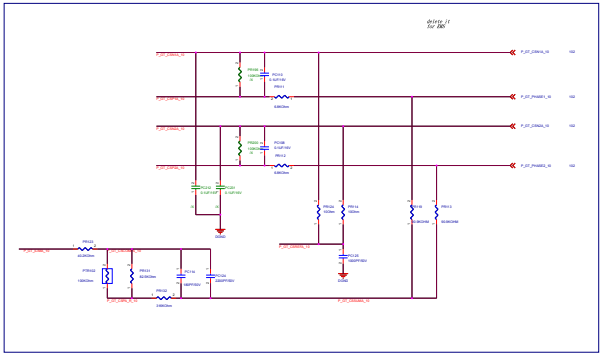


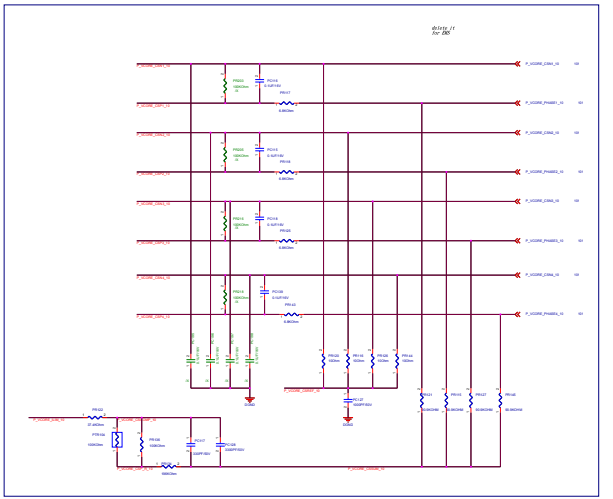


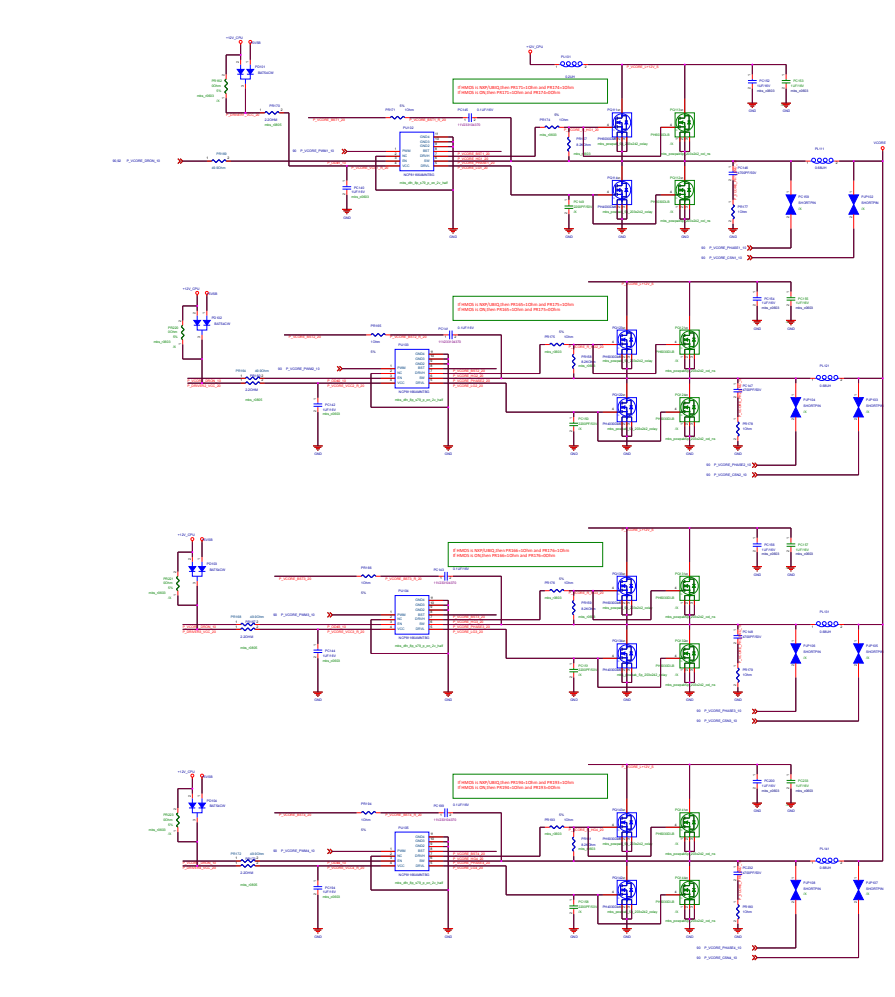


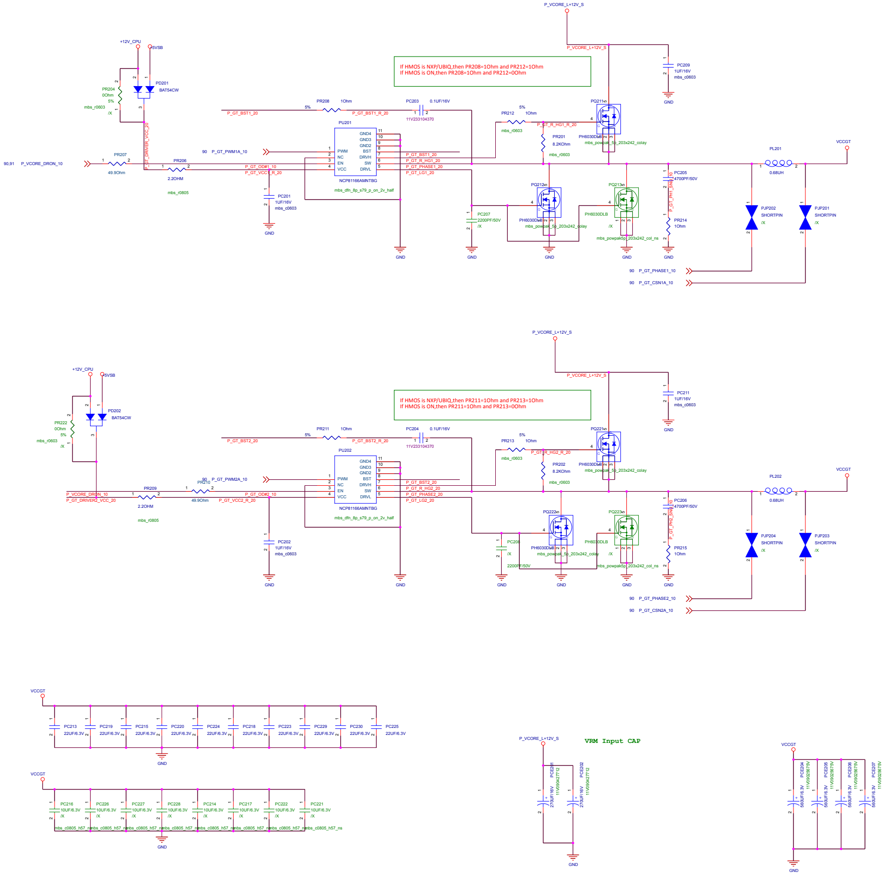

POWER intersheet
P_VBAT_POST_10
P_VCORE_DRON_10
P_VCORE_PG_10
EE intersheet
P_VCORE_VBIASON_10
P_BMBSEN_MAIN
P_BMBSLR_MAIN
P_VCC_SENSE
P_VSS_SENSE
P_DT_VCC_SENSE
P_DT_VSS_SENSE
P_SVID_CLK
P_SVID_DATA
P_SVID_ALERT#
P_VCORE_VBIASON_R_10
CPU_SMD_IDT
CPU_SMD_VCORE

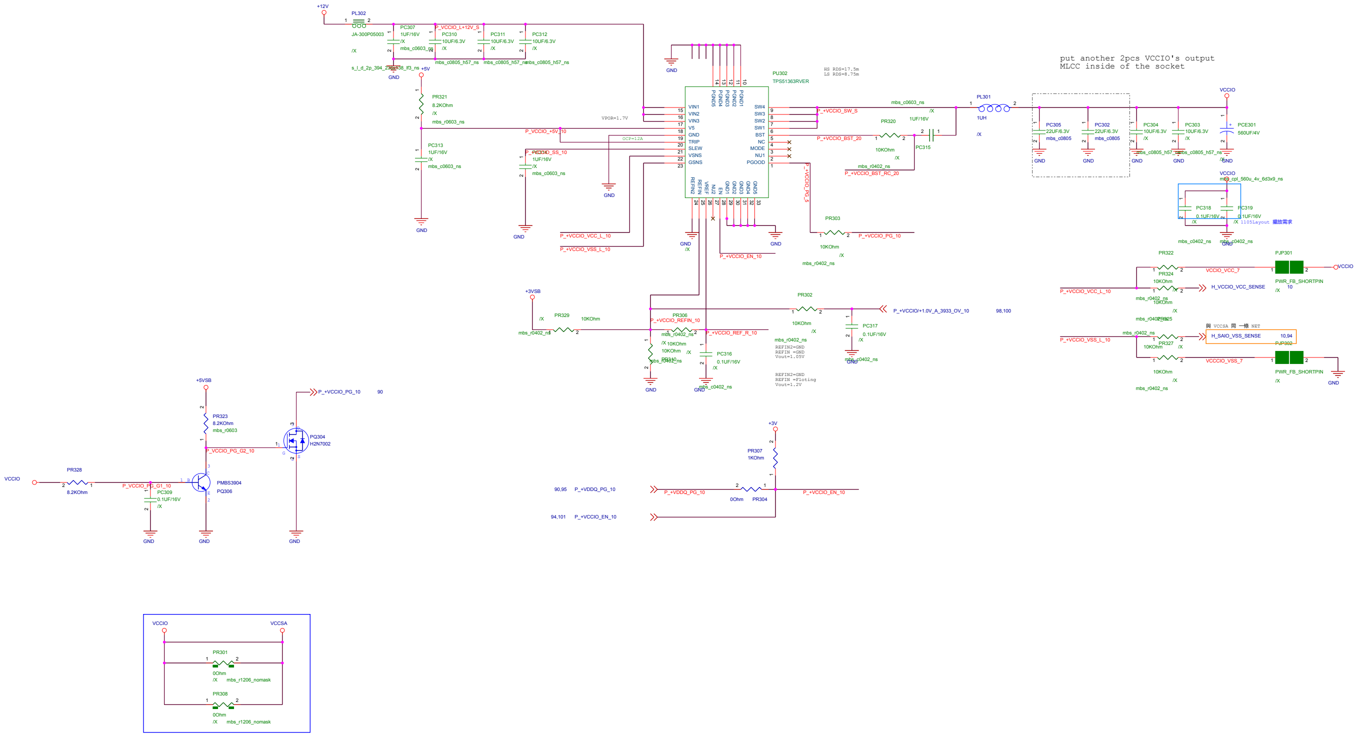


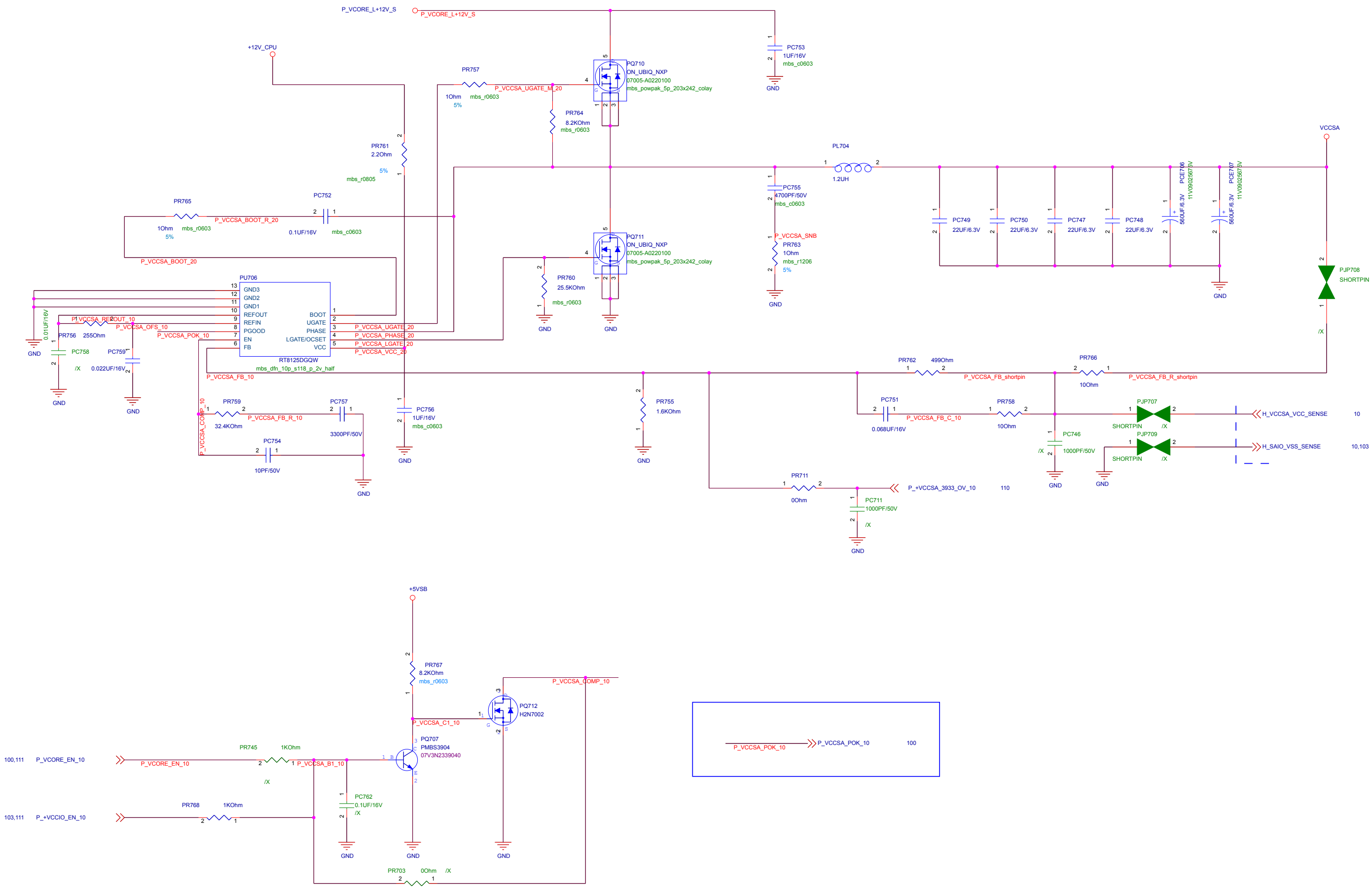

delete it
for BB

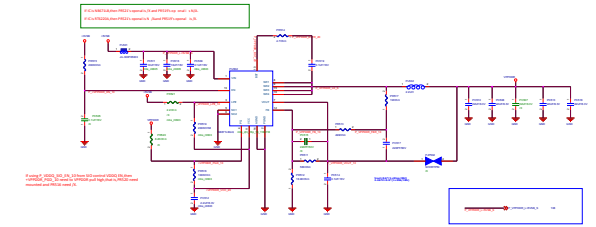

delete it
for BB

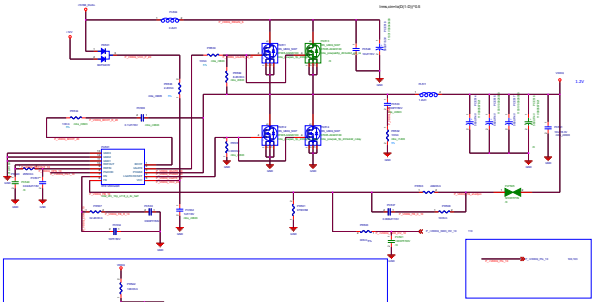

VRM Input CAP

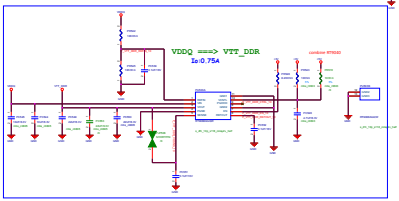

If HMOS is NXP/UBIQ,then PR208=1Ohm and PR212=1Ohm
If HMOS is ON,then PR208=1Ohm and PR212=0Ohm
If HMOS is NXP/UBIQ,then PR211=1Ohm and PR213=1Ohm
If HMOS is ON,then PR211=1Ohm and PR213=0Ohm
P_VCORE_L+12V_S
+12V_CPU
5VSB
PD201
BAT54CW
PD202
PU201
PU202
NCP81166AMNTBG
PWM
NC
EN
VCC
GND4
GND3
GND2
BST
DRVH
SW
DRVL
P_GT_BST1_20
P_GT_BST2_20
P_GT_PWM1A_10
P_GT_PWM2A_10
P_VCORE_DRON_10
PH6030DLB
PL201
PL202
0.68UH
VCCGT
SHORTPIN
P_GT_PHASE1_10
P_GT_CSN1A_10
P_GT_PHASE2_10
P_GT_CSN2A_10
GND
22UF/6.3V
10UF/6.3V
VRM Input CAP
270UF/16V
560UF/6.3V

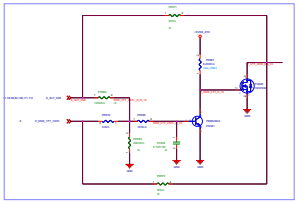

put another 2pcs VCCIO's output
MLCC inside of the socket
PU302
TPS51363RVER
HS RDS=17.5m
LS RDS=8.75m
VPGR=1.7V
OCP=12A
+12V
PL302
JA-300P05003
PC307
1UF/16V
mbs_c0603_ns
PC310
10UF/6.3V
PC311
10UF/6.3V
PC312
10UF/6.3V
mbs_c0805_h57_ns
P_VCCIO_L+12V_S
+5V
PR321
8.2KOhm
mbs_r0603_ns
PC313
1UF/16V
mbs_c0603_ns
P_VCCIO_+5V_10
P_VCCIO_SS_10
PC314
1UF/16V
GND
VIN1
VIN2
VIN3
V5
TRIP
SLEW
VSNS
GSNS
SW4
SW3
SW2
SW1
BST
NC
MODE
NU1
PGOOD
REFIN2
VREF
REFIN
EN
P_+VCCIO_SW_S
P_+VCCIO_BST_20
P_+VCCIO_BST_RC_20
PR320
10KOhm
mbs_r0402_ns
PC315
1UF/16V
mbs_c0603_ns
PL301
1UH
VCCIO
PC305
22UF/6.3V
mbs_c0805
PC302
22UF/6.3V
mbs_c0805
PC304
10UF/6.3V
PC303
10UF/6.3V
PCE301
560UF/4V
mbs_cpl_560u_4v_6d3x9_ns
PC318
0.1UF/16V
PC319
0.1UF/16V
mbs_c0402_ns
1105Layout 擺放需求
P_+VCCIO_PG_5
PR303
10KOhm
mbs_r0402_ns
P_+VCCIO_PG_10
P_+VCCIO_VCC_L_10
P_+VCCIO_VSS_L_10
P_+VCCIO_EN_10
PR322
10KOhm
PR324
10KOhm
VCCIO_VCC_7
H_VCCIO_VCC_SENSE
PJP301
PWR_FB_SHORTPIN
PR325
PR327
10KOhm
與 VCCSA 同 一條 NET
H_SAIO_VSS_SENSE
10,94
PJP302
VCCCIO_VSS_7
+3VSB
PR329
10KOhm
mbs_r0402_ns
PR306
P_+VCCIO_REFIN_10
PR310
10KOhm
P_+VCCIO_REF_R_10
PC316
0.1UF/16V
mbs_c0402_ns
PR302
10KOhm
PC317
0.1UF/16V
P_+VCCIO/+1.0V_A_3933_OV_10
98,100
REFIN2=GND
REFIN =GND
Vout=1.05V
REFIN2=GND
REFIN =Floting
Vout=1.2V
+5VSB
PR323
8.2KOhm
mbs_r0603
P_VCCIO_PG_G2_10
PQ304
H2N7002
P_+VCCIO_PG_10
90
VCCIO
PR328
8.2KOhm
P_VCCIO_PG_G1_10
PC309
0.1UF/16V
PMBS3904
PQ306
+3V
PR307
1KOhm
90,95
P_+VDDQ_PG_10
PR304
0Ohm
P_+VCCIO_EN_10
94,101
VCCSA
PR301
0Ohm
mbs_r1206_nomask
PR308
0Ohm
mbs_r1206_nomask

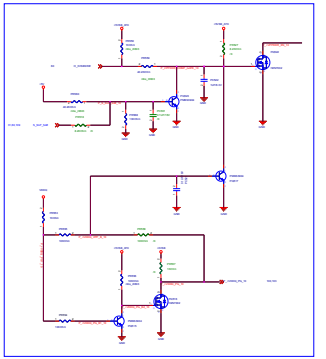

P_VCORE_L+12V_S
+12V_CPU
PQ710
ON_UBIQ_NXP
07005-A0220100
mbs_powpak_5p_203x242_colay
PC753
1UF/16V
mbs_c0603
PR757
1Ohm
5%
mbs_r0603
P_VCCSA_UGATE_M_20
PR764
8.2KOhm
PR761
2.2Ohm
mbs_r0805
VCCSA
PL704
1.2UH
PC755
4700PF/50V
P_VCCSA_SNB
PR763
1Ohm
mbs_r1206
PC749
PC750
PC747
PC748
22UF/6.3V
PCE706
PCE707
560UF/6.3V
PR765
P_VCCSA_BOOT_R_20
PC752
0.1UF/16V
PQ711
PR760
25.5KOhm
P_VCCSA_BOOT_20
PU706
GND3
GND2
GND1
REFOUT
REFIN
PGOOD
EN
FB
BOOT
UGATE
PHASE
LGATE/OCSET
VCC
RT8125DGQW
mbs_dfn_10p_s118_p_2v_half
P_VCCSA_REFOUT_10
P_VCCSA_OFS_10
P_VCCSA_POK_10
P_VCCSA_UGATE_20
P_VCCSA_PHASE_20
P_VCCSA_LGATE_20
P_VCCSA_VCC_20
PJP708
SHORTPIN
PR756
255Ohm
PC758
0.01UF/16V
PC759
0.022UF/16V
P_VCCSA_FB_10
PR762
499Ohm
P_VCCSA_FB_shortpin
PR766
10Ohm
P_VCCSA_FB_R_shortpin
PR759
32.4KOhm
P_VCCSA_FB_R_10
PC757
3300PF/50V
PC754
10PF/50V
P_VCCSA_COMP_10
PC756
1UF/16V
PR755
1.6KOhm
PC751
0.068UF/16V
P_VCCSA_FB_C_10
PR758
10Ohm
PJP707
H_VCCSA_VCC_SENSE
PC746
1000PF/50V
PJP709
H_SAIO_VSS_SENSE
10,103
PR711
0Ohm
P_+VCCSA_3933_OV_10
110
PC711
1000PF/50V
GND
+5VSB
PR767
8.2KOhm
PQ712
H2N7002
P_VCCSA_C1_10
PQ707
PMBS3904
07V3N2339040
100,111
P_VCORE_EN_10
PR745
1KOhm
P_VCCSA_B1_10
PC762
0.1UF/16V
103,111
P_+VCCIO_EN_10
PR768
1KOhm
PR703
0Ohm
P_VCCSA_POK_10
100

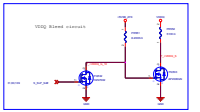


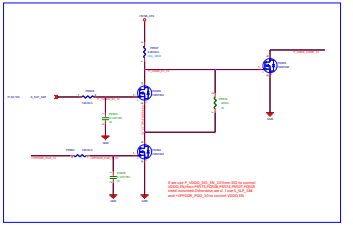


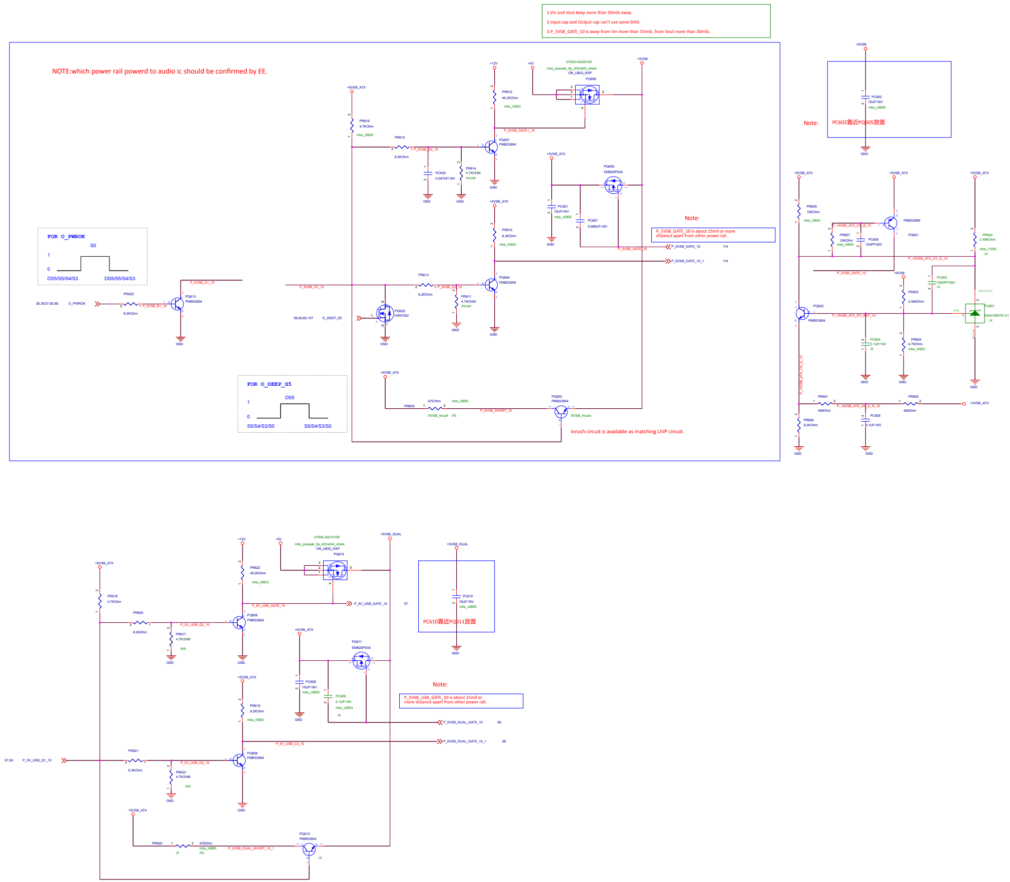

VDDQ ==> VTT_DDR
Io:0.75A



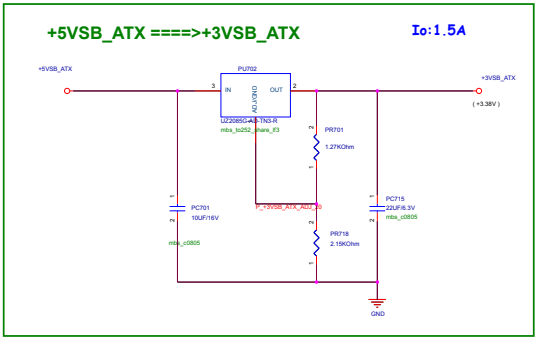


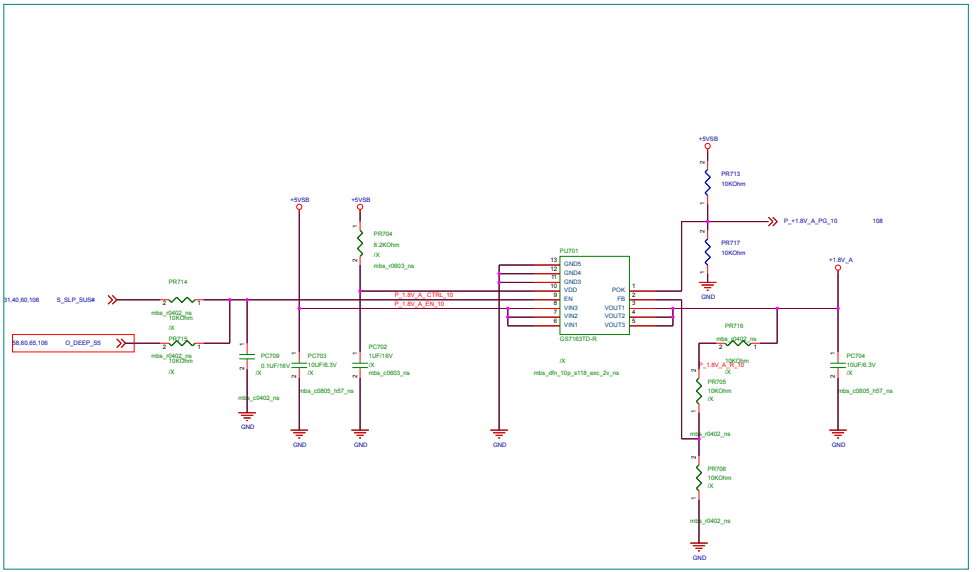

VDDQ Bleed circuit

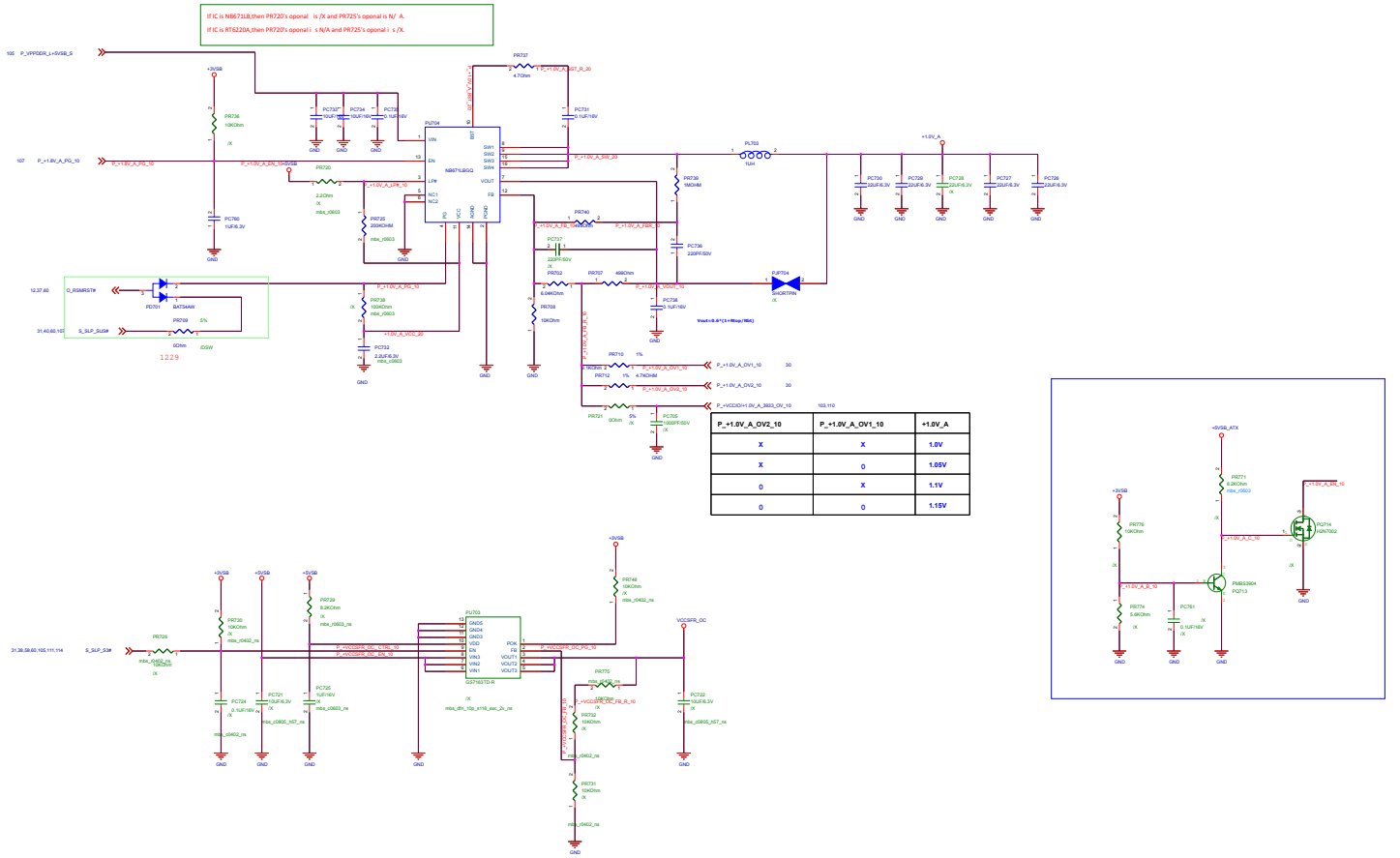




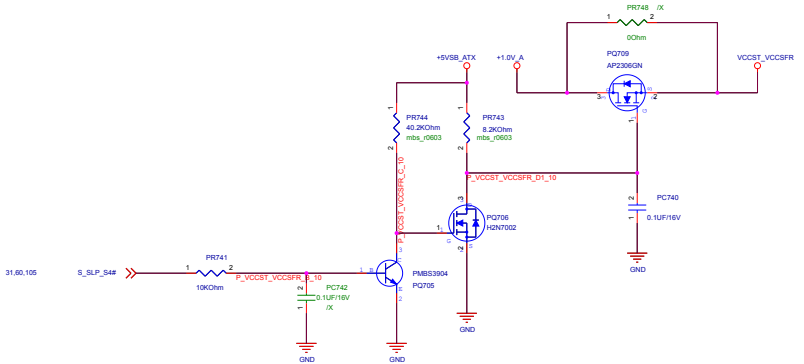
1.Vin and Vout keep more than 30mils away.
2.Input cap and Output cap can't use same GND.
3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.
NOTE:which power rail powerd to audio ic should be confirmed by EE.
Note:
PC602靠近PQ605放置
Note:
P_5VSB_GATE_10 is about 15mil or more distance apart from other power rail.
P_5VSB_GATE_10
P_5VSB_GATE_10_1
FOR O_PWROK
DS5/S5/S4/S3
FOR O_DEEP_S5
S5/S4/S3/S0
Inrush circuit is available as matching UVP circuit.
PC610靠近PQ611放置
Note:
P_5VSB_USB_GATE_10 is about 15mil or more distance apart from other power rail.
P_5VSB_DUAL_GATE_10
P_5VSB_DUAL_GATE_10_1

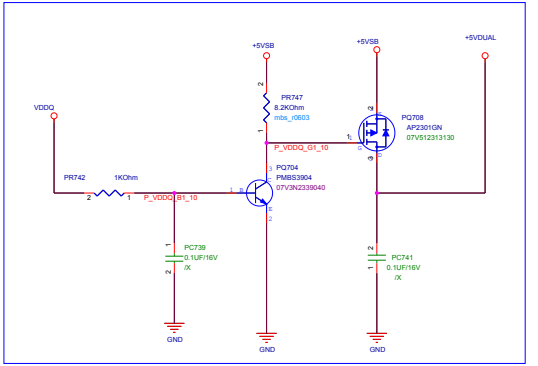

+5VSB_ATX ====>+3VSB_ATX
Io:1.5A
+5VSB_ATX
PU702
IN
GND/ADJ
OUT
3
2
+3VSB_ATX
(+3.38V)
UZ1085CA-3.3TN3-R
mbs_to252_share_lf3
PR701
1.27KOhm
PC701
10UF/16V
mbs_c0805
P_+3VSB_ATX_ADJ_10
PC715
22UF/6.3V
mbs_c0805
PR718
2.19KOhm
GND


+5VSB
+5VSB
PR704
8.2KOhm
/X
mbs_r0603_ns
PU701
GND5
GND4
GND3
VDD
EN
VIN3
VIN2
VIN1
POK
FB
VOUT1
VOUT2
VOUT3
GS7163TD-R
/X
mbs_dfn_10p_a118_exc_2v_ns
+5VSB
PR713
10KOhm
P_+1.8V_A_PG_10
108
PR717
10KOhm
GND
+1.8V_A
31,40,60,108
S_SLP_SUS#
PR714
mbs_r0402_ns
10KOhm
/X
P_1.8V_A_CTRL_10
P_1.8V_A_EN_10
56,60,65,106
O_DEEP_S5
PR715
mbs_r0402_ns
10KOhm
/X
PC709
0.1UF/16V
/X
mbs_c0402_ns
PC703
10UF/6.3V
/X
mbs_c0805_h57_ns
PC702
1UF/16V
/X
mbs_c0603_ns
PR716
mbs_r0402_ns
10KOhm
/X
P_1.8V_A_PG_10
PR705
10KOhm
/X
mbs_r0402_ns
PR706
10KOhm
/X
mbs_r0402_ns
PC704
10UF/6.3V
/X
mbs_c0805_h57_ns
GND

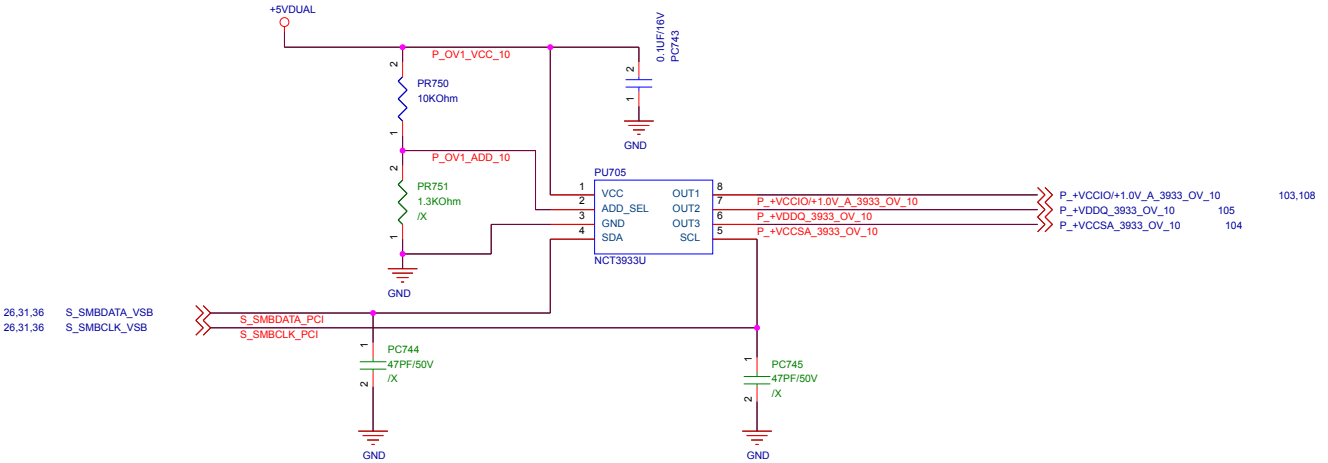


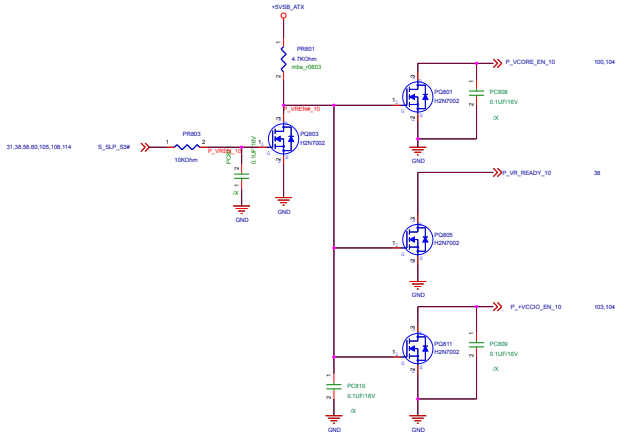
P_+1.0V_A_OV2_10	P_+1.0V_A_OV1_10	+1.0V_A
X	X	1.0V
X	0	1.05V
0	X	1.1V
0	0	1.15V

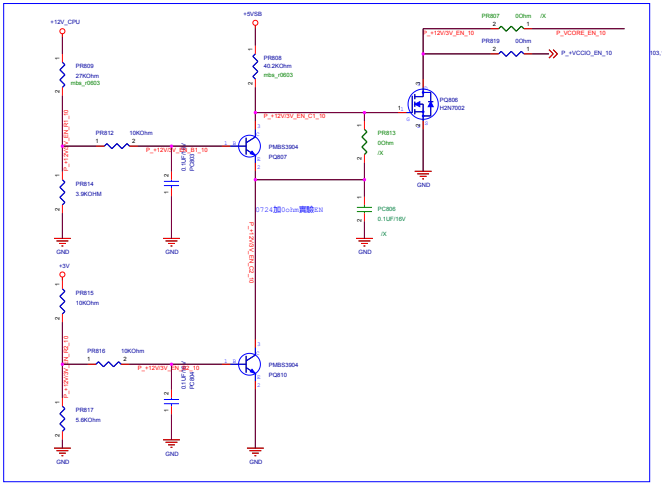

PR748 /X
0Ohm
+5VSB_ATX
+1.0V_A
PQ709
AP2306GN
VCCST_VCCSFR
PR744
40.2KOhm
mbs_r0603
PR743
8.2KOhm
mbs_r0603
P_VCCST_VCCSFR_D1_10
P_VCCST_VCCSFR_C_10
PC740
0.1UF/16V
PQ706
H2N7002
31,60,105
S_SLP_S4#
PR741
10KOhm
P_VCCST_VCCSFR_B_10
PMBS3904
PQ705
PC742
0.1UF/16V
/X
GND

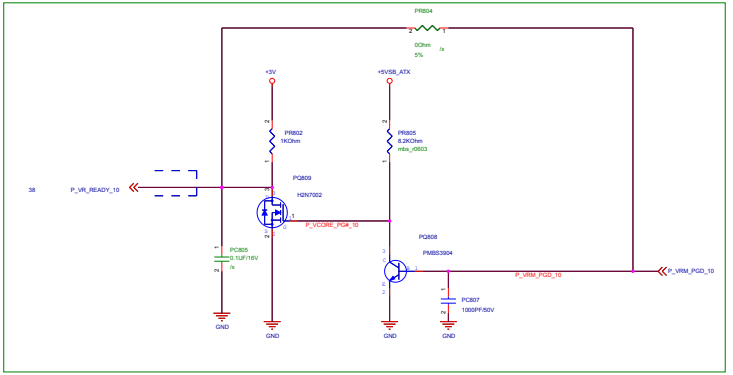

+5VSB
+5VSB
+5VDUAL
VDDQ
PR747
8.2KOhm
mbs_r0603
PQ708
AP2301GN
07V512313130
P_VDDQ_G1_10
PR742
1KOhm
P_VDDQ_B1_10
PQ704
PMBS3904
07V3N2339040
PC739
0.1UF/16V
/X
PC741
0.1UF/16V
/X
GND

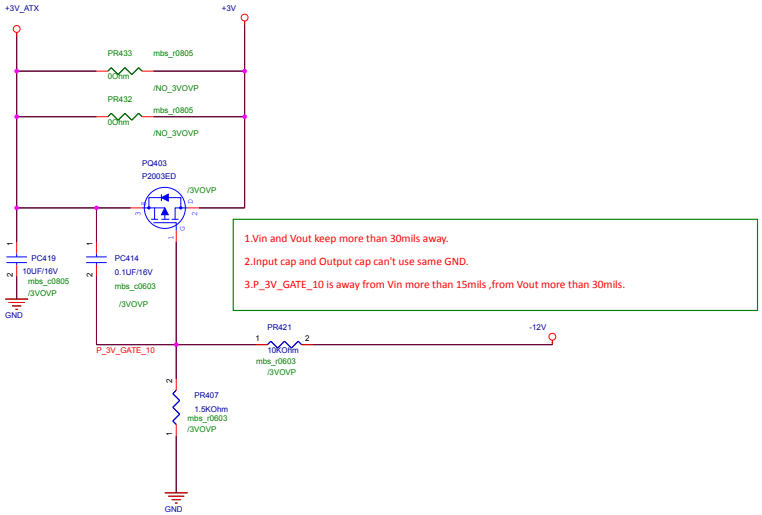
Address : 0x20



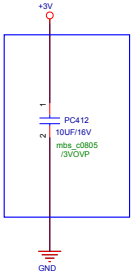

+5VSB_ATX
PR801
4.7KOhm
mba_r0603
P_VRENA_10
PQ803
H2N7002
PR803
10KOhm
S_SLP_S3#
31,38,58,60,105,108,114
PC807
0.1UF/16V
/X
GND
PQ801
H2N7002
PC808
0.1UF/16V
/X
P_VCORE_EN_10
100,104
P_VR_READY_10
38
PQ805
H2N7002
PQ811
H2N7002
PC809
0.1UF/16V
/X
P_+VCCIO_EN_10
103,104
PC810
0.1UF/16V
/X


+12V_CPU
+5VSB
PR809
27KOhm
mba_r0603
PR812
10KOhm
PR814
3.9KOHM
PR808
40.2KOhm
mba_r0603
PMBS3904
PQ807
PR813
0Ohm
/X
PC806
0.1UF/16V
/X
PR807
0Ohm
/X
PR819
0Ohm
PQ806
H2N7002
P_VCORE_EN_10
P_+VCCIO_EN_10
103,104
+3V
PR815
10KOhm
PR816
10KOhm
PR817
5.6KOhm
PMBS3904
PQ810
GND

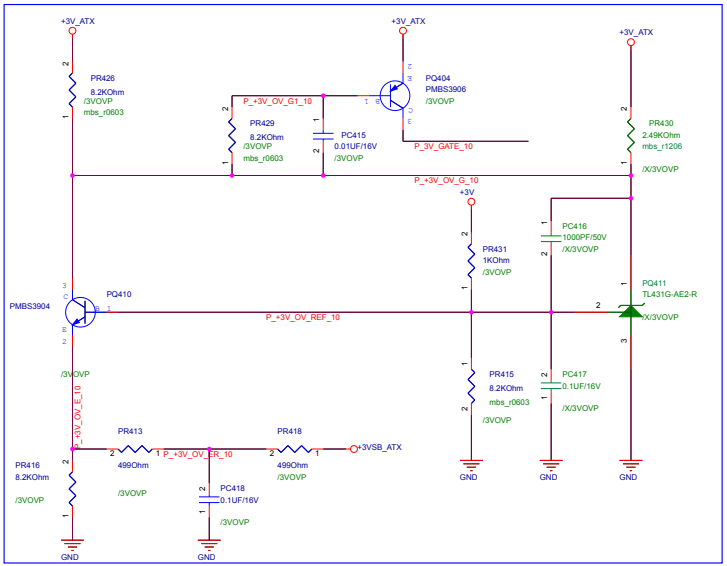

PR804
0Ohm
/x
5%
+3V
+5VSB_ATX
PR802
1KOhm
PR805
8.2KOhm
mba_r0603
38
P_VR_READY_10
PQ809
H2N7002
P_VCORE_PG#_10
PC805
0.1UF/16V
/x
PQ808
PMBS3904
P_VRM_PGD_10
P_VRM_PCD_10
100
PC807
1000PF/50V
GND



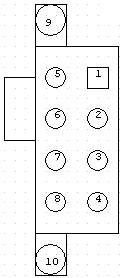
PC412靠近PQ403放置

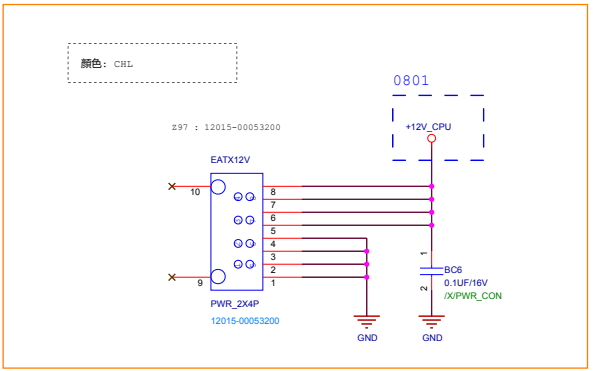


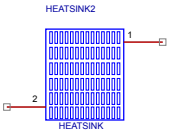
PQ404,PQ410 and other components are be er to place close to PQ403.

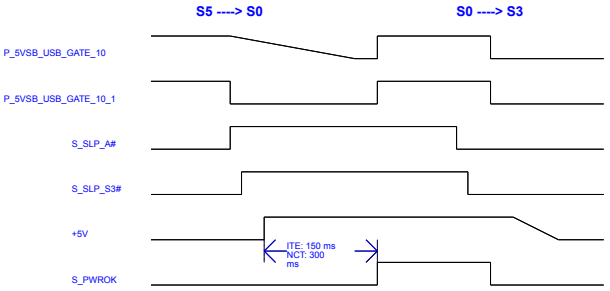


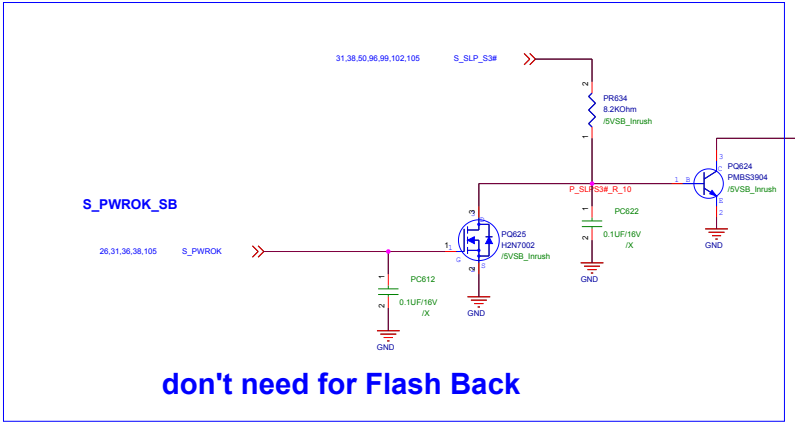
8 Pin +12V Connector

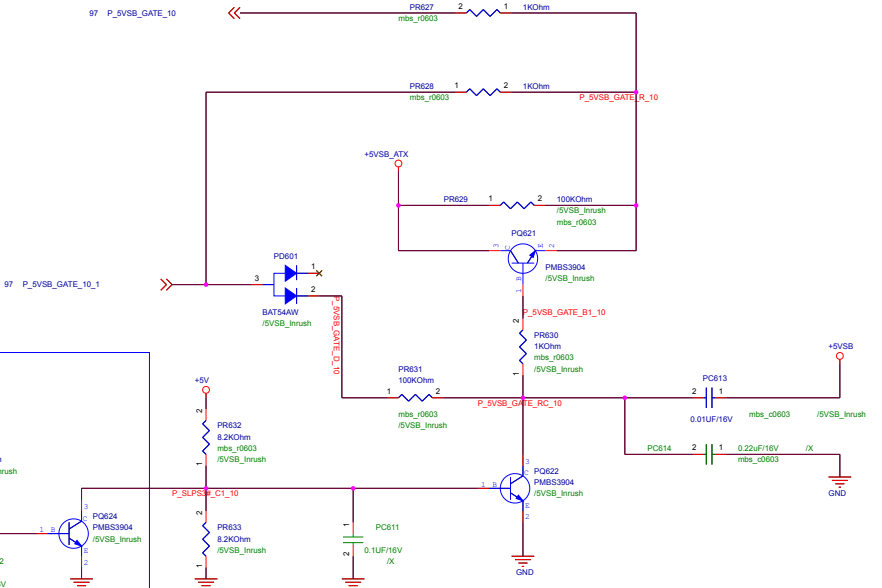


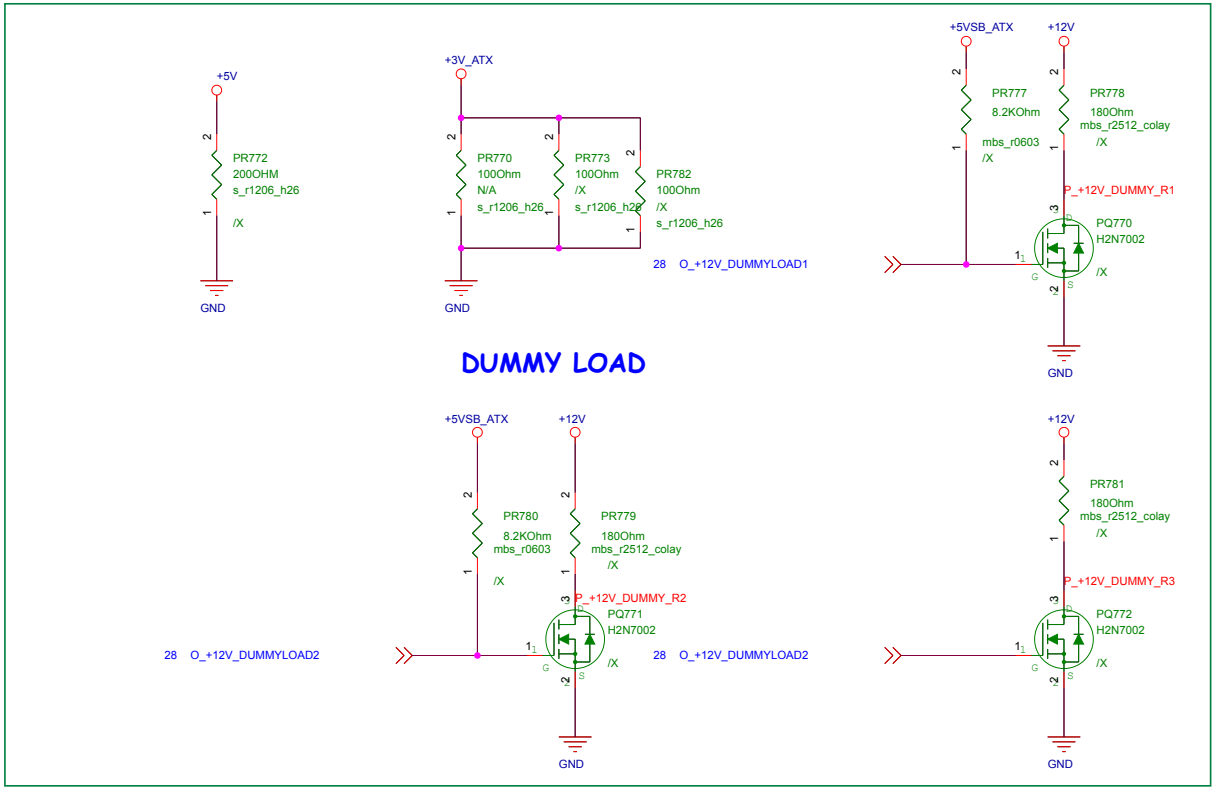


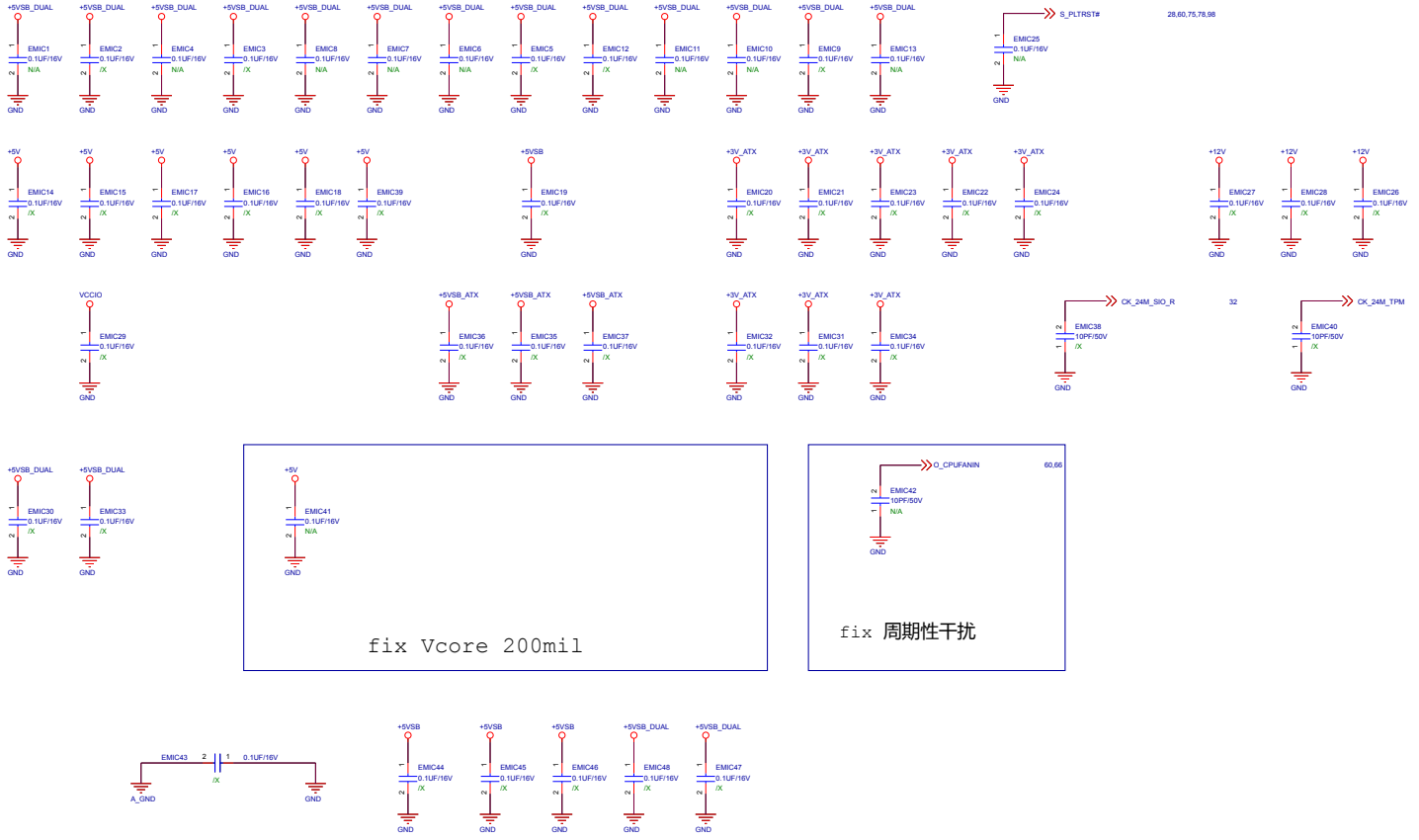



S5 ----> S0
S0 ----> S3
P_5VSB_USB_GATE_10
P_5VSB_USB_GATE_10_1
S_SLP_A#
S_SLP_S3#
+5V
S_PWROK
ITE: 150 ms
NCT: 300 ms


S_PWROK_SB
don't need for Flash Back


97 P_5VSB_GATE_10
PR627
1KOhm
mbs_r0603
PR628
1KOhm
P_5VSB_GATER_10
+5VSB_ATX
PR629
100KOhm
/5VSB_Inrush
mbs_r0603
PQ621
PMBS3904
/5VSB_Inrush
97 P_5VSB_GATE_10_1
PD601
BAT54AW
/5VSB_Inrush
P_5VSB_GATE_B1_10
PR830
1KOhm
mbs_r0603
/5VSB_Inrush
+5VSB
PR631
100KOhm
mbs_r0603
/5VSB_Inrush
P_5VSB_GATE_RC_10
PC613
0.01UF/16V
mbs_c0603
/5VSB_Inrush
PC614
0.22uF/16V
/X
mbs_c0603
GND
+5V
PR632
8.2KOhm
mbs_r0603
/5VSB_Inrush
P_SLPS3#_C1_10
PQ622
PMBS3904
/5VSB_Inrush
PR633
8.2KOhm
/5VSB_Inrush
PC611
0.1UF/16V
/X
31,38,50,96,99,102,105
S_SLP_S3#
PR634
8.2KOhm
/5VSB_Inrush
P_SLPS3#_R_10
PQ624
PMBS3904
/5VSB_Inrush
PC622
0.1UF/16V
/X
26,31,36,38,105
S_PWROK
PQ625
H2N7002
/5VSB_Inrush
PC612
0.1UF/16V
/X


+5V
PR772
200OHM
s_r1206_h26
/X
GND
+3V_ATX
PR770
100Ohm
N/A
s_r1206_h26
PR773
100Ohm
/X
s_r1206_h26
PR782
100Ohm
/X
s_r1206_h26
28 O_+12V_DUMMYLOAD1
GND
+5VSB_ATX
+12V
PR777
8.2KOhm
mbs_r0603
/X
PR778
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R1
PQ770
H2N7002
/X
GND
DUMMY LOAD
+5VSB_ATX
+12V
PR780
8.2KOhm
mbs_r0603
/X
PR779
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R2
PQ771
H2N7002
/X
28 O_+12V_DUMMYLOAD2
28 O_+12V_DUMMYLOAD2
GND
+12V
PR781
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R3
PQ772
H2N7002
/X
GND


+5VSB_DUAL
EMIC1
0.1UF/16V
N/A
GND
EMIC2
/X
EMIC4
EMIC3
EMIC8
EMIC7
EMIC6
EMIC5
EMIC12
EMIC11
EMIC10
EMIC9
EMIC13
S_PLTRST#
28,60,75,78,98
EMIC25
+5V
EMIC14
EMIC15
EMIC17
EMIC16
EMIC18
EMIC39
+5VSB
EMIC19
+3V_ATX
EMIC20
EMIC21
EMIC23
EMIC22
EMIC24
+12V
EMIC27
EMIC28
EMIC26
VCCIO
EMIC29
+5VSB_ATX
EMIC36
EMIC35
EMIC37
EMIC32
EMIC31
EMIC34
CK_24M_SIO_R
32
EMIC38
10PF/50V
CK_24M_TPM
EMIC40
EMIC30
EMIC33
EMIC41
fix Vcore 200mil
O_CPUFANIN
60,66
EMIC42
fix 周期性干扰
EMIC43
A_GND
EMIC44
EMIC45
EMIC46
EMIC48
EMIC47