Anchorbay
TLD Build

NB5

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Quanta Computer Inc.

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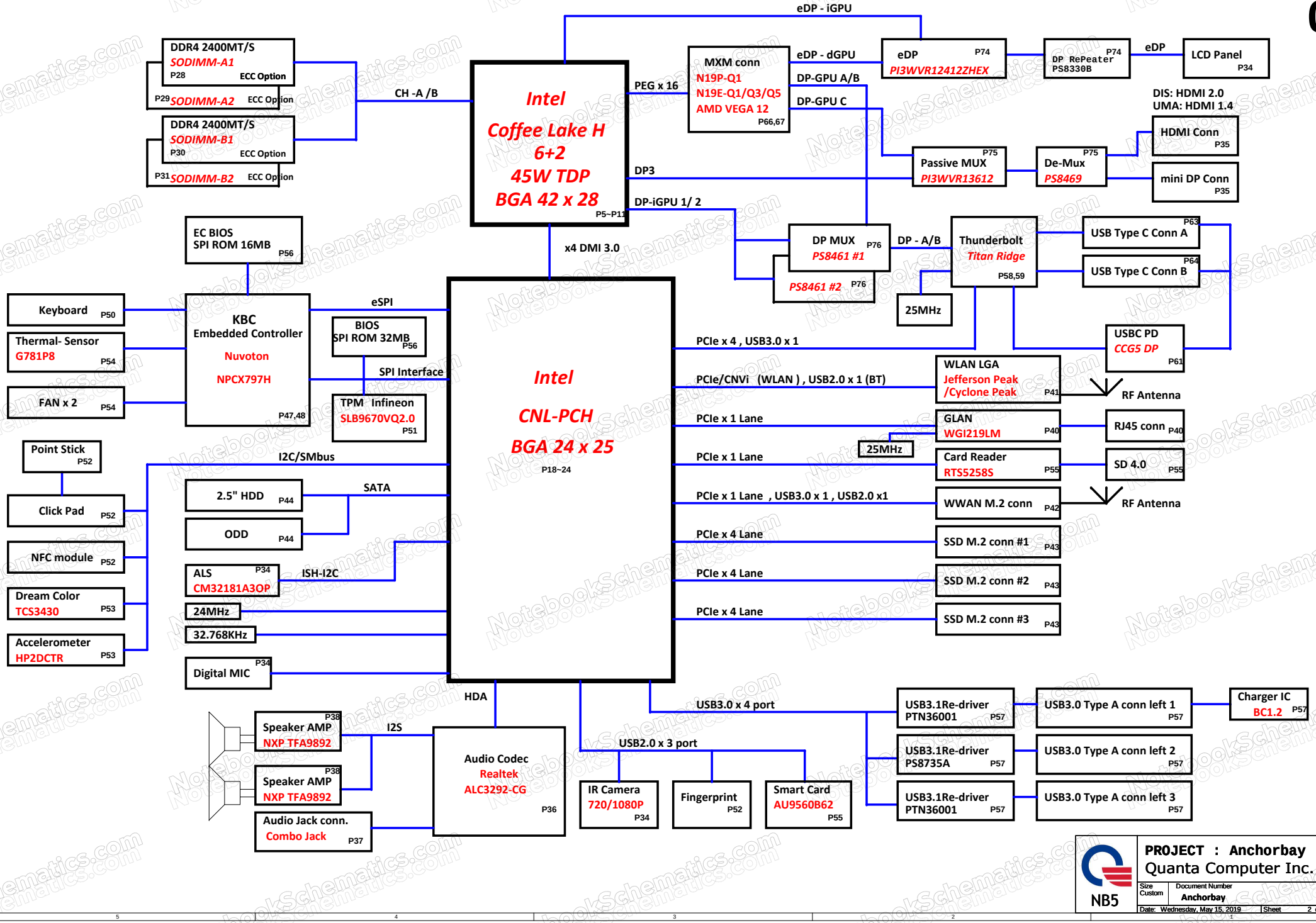

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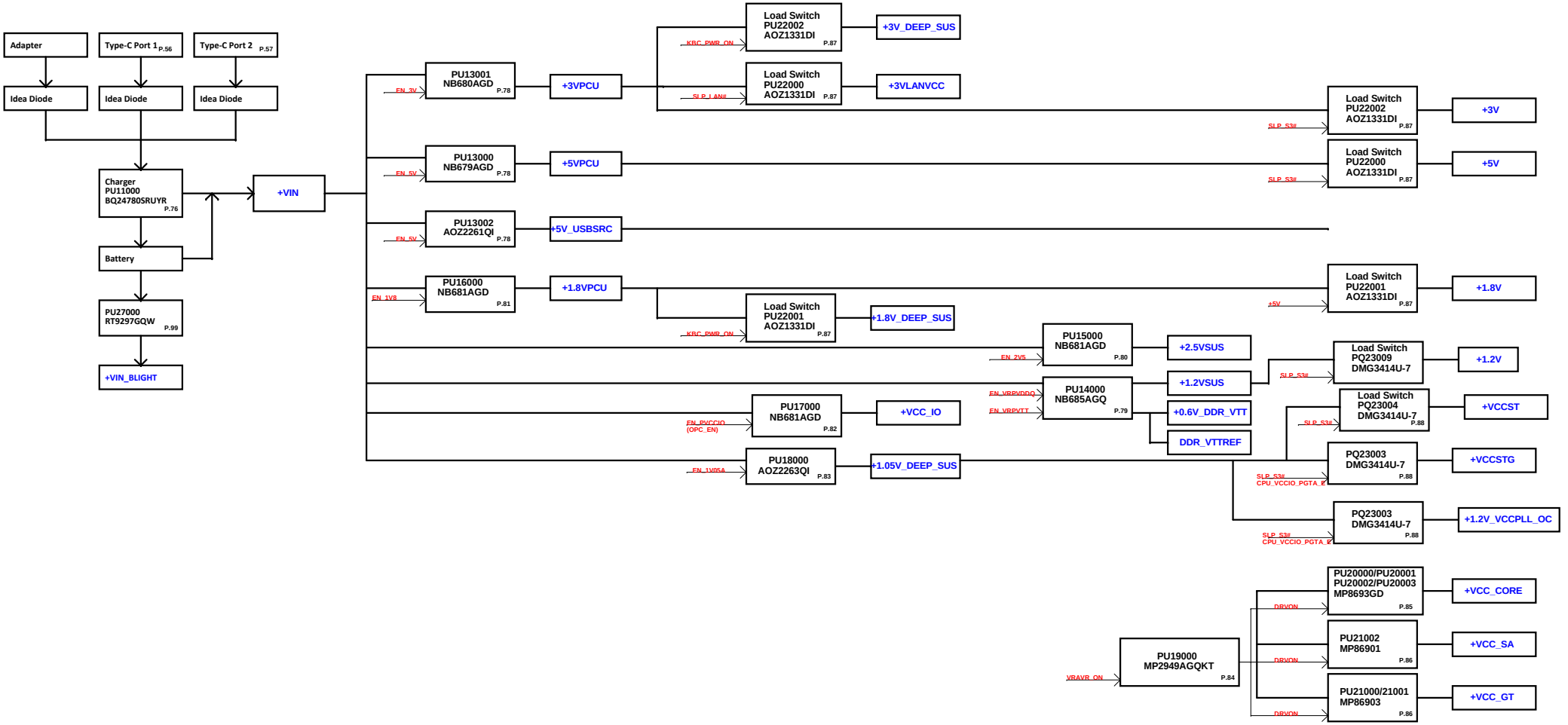
POWER BLOCK DIAGRAM

03



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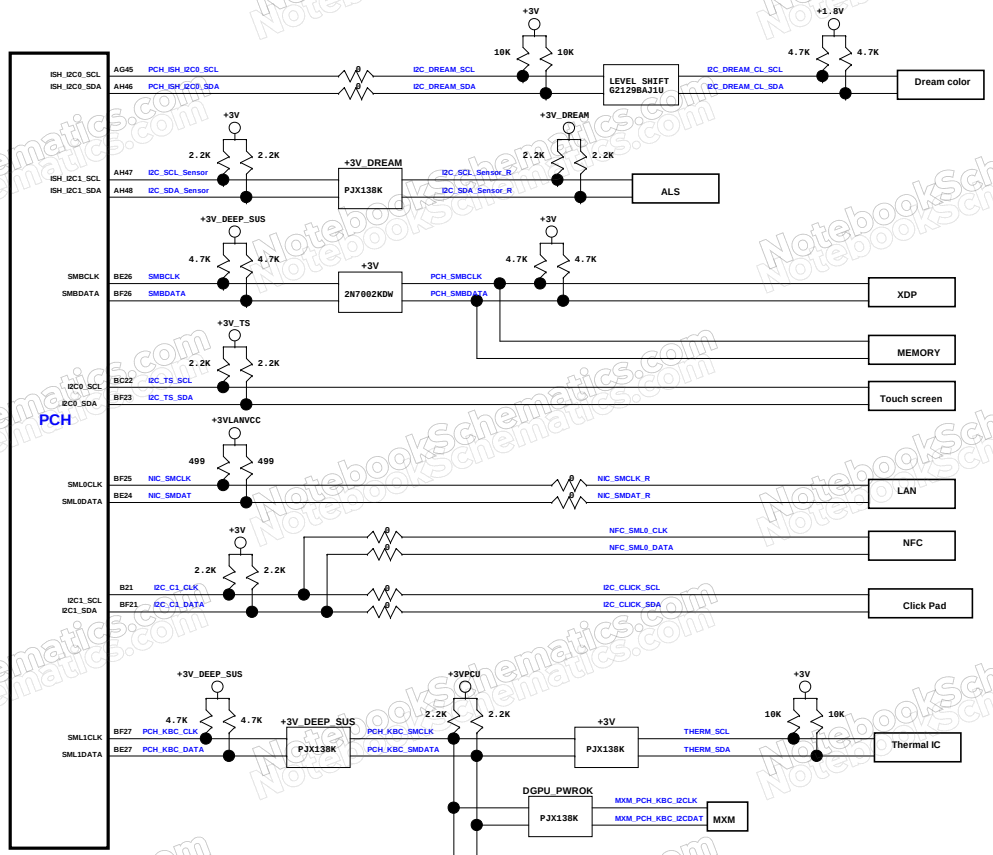

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB3 #2 / SSIC #1	NC
USB3 #3 / SSIC #2	USB2.0/USB3.0 Combo Jack(Light side-1)
USB3 #4	USB2.0/USB3.0 Combo Jack(Light side-2)
USB3 #5	NC
USB3 #6	NC
PCIE1 / USB3 #7	NC
PCIE2 / USB3 #8	NC
PCIE3 / USB3 #9	CARD READER
PCIE4 / USB3 #10	WWAN
PCIE5	Alpine Ridge
PCIE6	Alpine Ridge
PCIE7	Alpine Ridge
PCIE8	Alpine Ridge
PCIE9	SSD 1
PCIE10	SSD 1
PCIE11(SATA0A)	SSD 1(SATA0A)
PCIE12(SATA1)A	SSD 1(SATA1A)
PCIE13(SATA0B)	LAN
PCIE14(SATA1B)	WLAN
PCIE15(SATA2)	ODD
PCIE16(SATA3)	HDD
PCIE17(SATA4)	SSD 2(SATA4)
PCIE18(SATA5)	SSD 2(SATA5)
PCIE19(SATA6)	SSD 2(SATA6)
PCIE20(SATA7)	SSD 2(SATA7)
PCIE21	SSD 3
PCIE22	SSD 3
PCIE23	SSD 3
PCIE24	SSD 3

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Right side)
USB2 #2	WWAN
USB2 #3	NC
USB2 #4	USB2.0/USB3.0 Combo Jack(Left side-1)
USB2 #5	USB2.0/USB3.0 Combo Jack(Left side-2)
USB2 #6	NC
USB2 #7	Camera
USB2 #8	Finger Print
USB2 #9	SmartCard
USB2 #10	NC
USB2 #11	TI PD PORT A
USB2 #12	NC
USB2 #13	TI PD PORT B
USB2 #14	BT

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CFL-H Processor (CLK,MISC,JTAG)

05

For debug only remove from MV

+3V
R5200 360_6
LED5200_P
LED5200 White_19-113/T1D-CP2Q2HY/3T
LED5200_N
+VCCST
+3V
R5233 47K/F_4
R5202 49.9_1%_4
Q5205_D
CATERR#
Q5205A PJX138K
Q5205B PJX138K

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

U5200E

[20] CLK_CPU_BCLKP	CLK_CPU_BCLKP	B31	BCLKP
[20] CLK_CPU_BCLKN	CLK_CPU_BCLKN	A32	BCLKN
[20] CPU_PCI_BCLKP	CPU_PCI_BCLKP	D35	PCI_BCLKP
[20] CPU_PCI_BCLKN	CPU_PCI_BCLKN	C36	PCI_BCLKN
[20] CLK_DPLL_NSCCLKP	CLK_DPLL_NSCCLKP	E31	CLK24P
[20] CLK_DPLL_NSCCLKN	CLK_DPLL_NSCCLKN	D31	CLK24N

H_CPU_SVIDALRT#	BH31	VIDALERT#
VR_SVID_CLK_R	BH32	VIDSCK
H_CPU_SVIDDAT	BH29	VIDSOUT
CPU_PROCHOT#_R	BR30	PROCHOT#
DDR_PG_CNTL	BT13	DDR_VTT_CNTL
R5211 60.4/F_4	TP5202	VCCST_PWRGD H13
[19] PROCPWRGD	PROCPWRGD	BT31 PROCPWRGD
[20] CPU_PLTRST#R	CPU_PLTRST#R	BP35 RESET#
[20] PM_SYNC	PM_SYNC	BM34 PM_SYNC
[20] H_PM_DOWN	R5212 20_4 H_PM_DOWN_R	BP31 PM_DOWN
	PECI	BT34 PECI
	THRMTRIP#	J31 THERMTRIP#
TP5203	SKTOCC_N	BR33 SKTOCC#
	PROC_SEL#	BN1 PROC_SELECT#
TP5204	CATERR#	BM30 CATERR#
		AT13
		AW13 ZVM#
		MSM#
		AU13
		AY13 RSVD#AU13
		RSVD#AY13

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*CPU_CFL-H_1440P

CFG_0	BN25 CFG0		CFG0 [78]
CFG_1	BN27 CFG1		CFG1 [78]
CFG_2	BN26 CFG2		CFG2 [17,78]
CFG_3	BN28 CFG3		CFG3 [78]
CFG_4	BR20 CFG4		CFG4 [17,78]
CFG_5	BM20 CFG5		CFG5 [17,66,78]
CFG_6	BT20 CFG6		CFG6 [17,66,78]
CFG_7	BP20 CFG7		CFG7 [78]
CFG_8	BP23 CFG8		CFG8 [78]
CFG_9	BR22 CFG9		CFG9 [78]
CFG_10	BT23 CFG10		CFG10 [78]
CFG_11	BT22 CFG11		CFG11 [78]
CFG_12	BM19 CFG12		CFG12 [78]
CFG_13	BR19 CFG13		CFG13 [78]
CFG_14	BP19 CFG14		CFG14 [78]
CFG_15	BT19 CFG15		CFG15 [78]
CFG_17	BN23 CFG17		CFG17 [78]
CFG_16	BP23 CFG16		CFG16 [78]
CFG_19	BP22 CFG19		CFG19 [78]
CFG_18	BN22 CFG18		CFG18 [78]
BPM#_0	BR27 XDP_BPM0		XDP_BPM0 [78]
BPM#_1	BT27 XDP_BPM1		XDP_BPM1 [78]
BPM#_2	BM31 XDP_BPM2		TP5200
BPM#_3	BT30 XDP_BPM3		TP5201
PROC_TDO	BT28 H_TDO		H_TDO [19,78]
PROC_TDI	BL32 H_TDI		H_TDI [19,78]
PROC_TMS	BP28 H_TMS		H_TMS [19,78]
PROC_TCK	BR28 H_TCK		H_TCK [19,78]
PROC_TRST#	BP30 H_TRST#		H_TRST# [24,78]
PROC_PREQ#	BL30 H_PREQ#		H_PREQ# [24,78]
PROC_PRDY#	BP27 H_PRDY#		H_PRDY# [24,78]
CFG_RCOMP	BT25 CFG_RCOMP	49.9_1%_4 R5213	

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

H_TDO R5234 100/F_4 +VCCST
H_TMS R5235 51_4
H_TDI R5205 51_4
H_PREQ# R5236 *56.2/F_4
H_TCK R5237 51_4
H_TRST# R5238 *51_4

.CFG[7]:PEG Training:
-1=(default) PEG Train immediately following RESET# de assertion.
-0=PEG Wait for BIOS for assertion.
.CFG[19:8]:Reserved configuration lanes.

+3V_DEEP_SUS
R5209 47K/F_4
Q5201_D
[33,48,67,77,094,095] PWR_GOOD_3
Q5201A PJX138K
Q5201B PJX138K
+VCCST
R5210 1K/F_4
H_VCCST_PWRGD

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

PM_SYNC (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

PECI 13/F_4 R5214
PCH_PECI [20]
PECI [48]

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

+VCCST
R5217 *54.9/F_4
Close to CPU
SVID CLK
VR_SVID_CLK_R R5220 *0_4/S VR_SVID_CLK [089]

CLOSE TO CPU
PLACE THE PU RESISTORS

+VCCST
R5224 56.2/F_4
Close to CPU
SVID ALERT
H_CPU_SVIDALRT# R5227 220/F_4 VR_SVID_ALERT# [089]
C5222 *0.1U/16V_2

CLOSE TO CPU
PLACE THE PU RESISTORS

+VCCST
R5231 100/F_4
Close to CPU
SVID DATA
H_CPU_SVIDDAT R5232 *0_4/S VR_SVID_DATA [089]

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

+VCCST +VCCST
R5215 200/F_4
R5216 1K/F_4
Q5202_B
[20,28,29,30,31,66] PM_THRMTRIP#
THRMTRIP#
Q5202 METR3904-G

Ra(R18) Not install in SKL-H

+VCCST
Ra
R5223 *10K/F_4
PROC_SEL#
R5226 *0_4

Note: please keep plane is enough for VDDQ 2.8A

+1.2VSUS
Placement close to CPU.
C5220 0.1U/16V_2
C5221 *0.1U/16V_2

+3V_DEEP_SUS
R5219 47K/F_4
Q5204 METR3904-G
Q5204_B
DDR_PG_CNTL R5222 10K/F_4
R5225 100K/F_4
Q5206 2N7002KTB
Q5204_C
+3V_DEEP_SUS
R5218 10K/F_4
DDR_VTT_PG_CTRL [33,084]
R5221 *100K/F_4

PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

+VCCSTG
R5228 1K/F_4
[54,082,089] CPU_PROCHOT#
[54] THERM_SC#
R5230 *0_4
R5229 499/F_4 CPU_PROCHOT#_R
Cb
C5223 47p/50V_4

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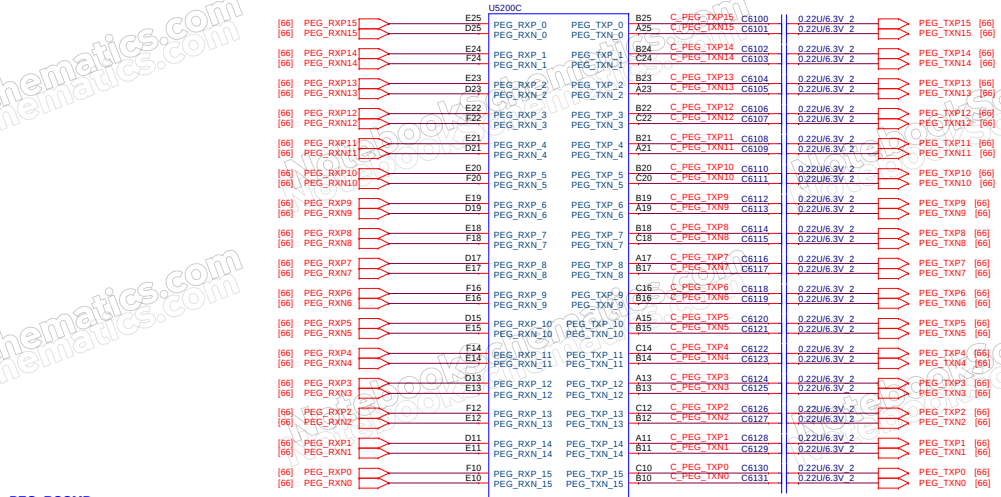
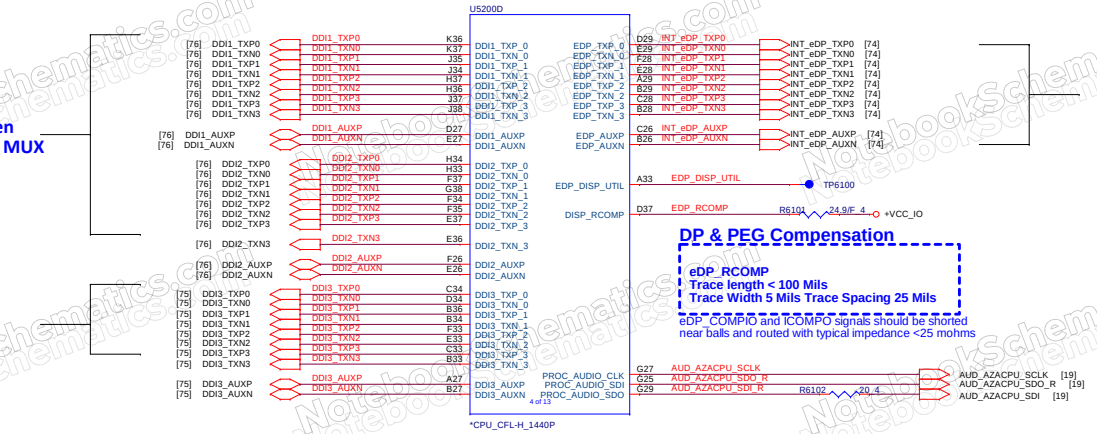
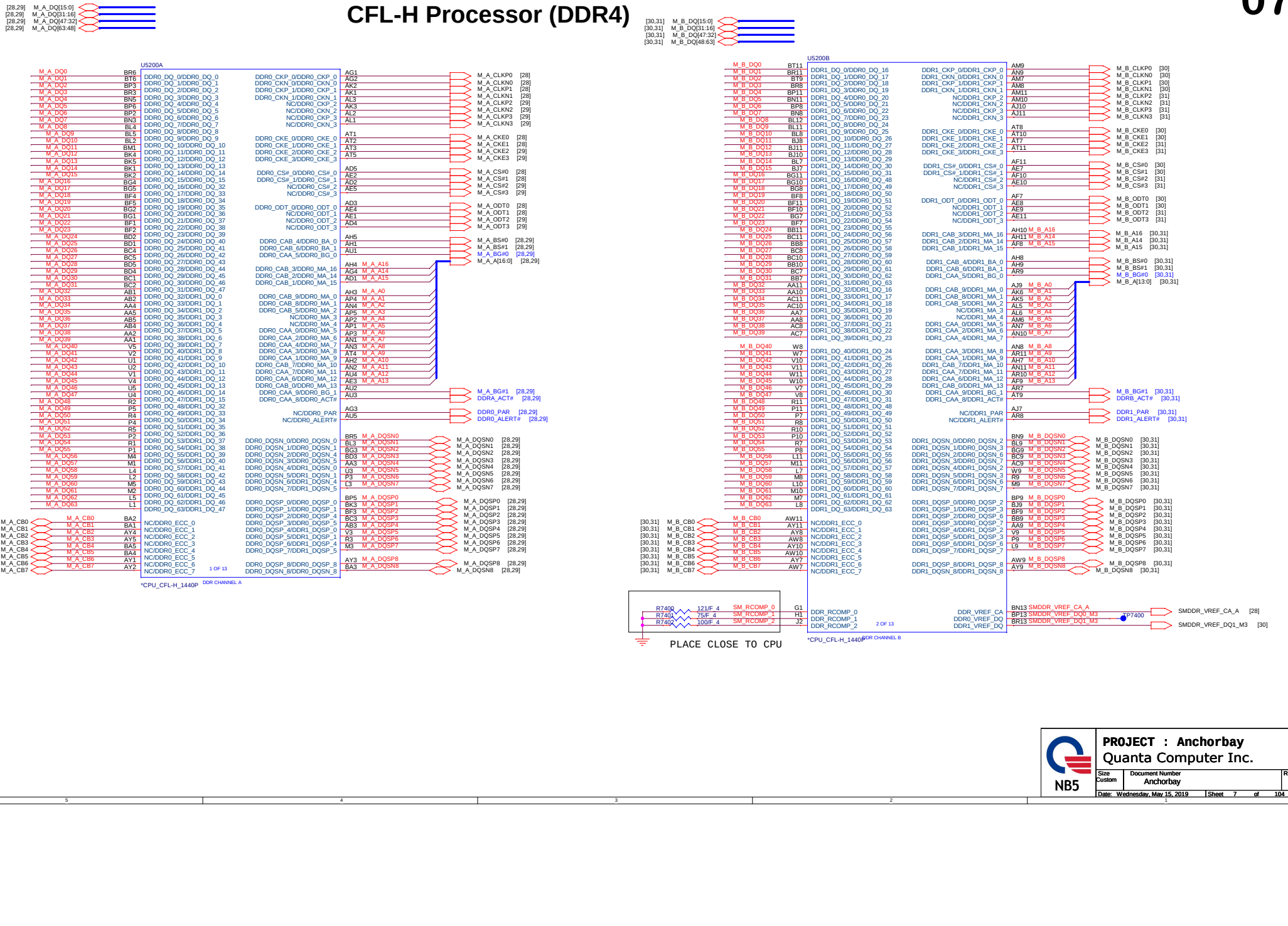
CFL-H Processor (DMI,PEG,FDI)





CFL-H Processor (DDR4)



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VCCGT

Edge cap
3x 47uF 0805
7x 22uF 0603

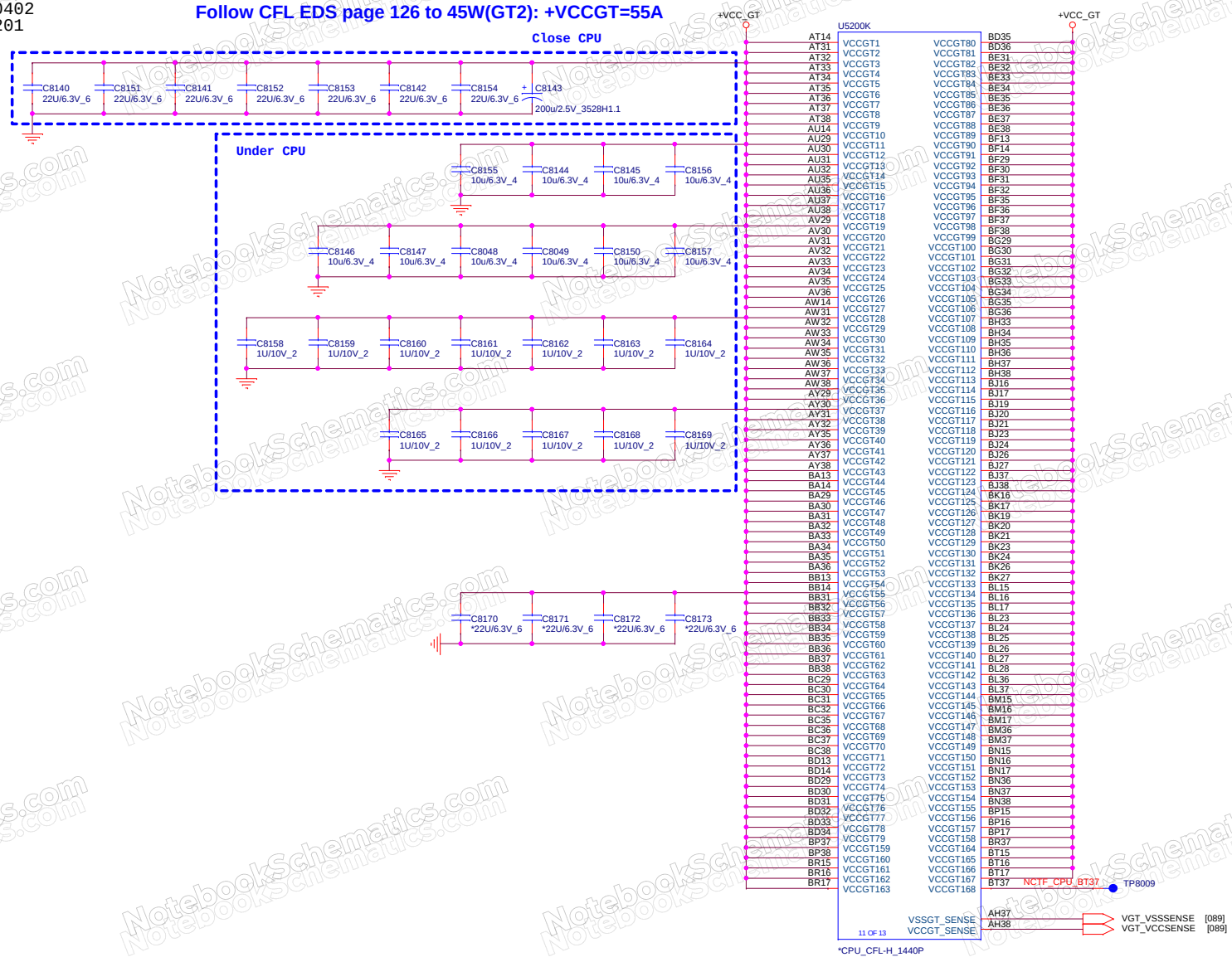
Backside cap
10x 10uF 0402
12x 1uF 0201

CFL-H Processor (POWER)

08

+VCC_GT [089,091]

Follow CFL EDS page 126 to 45W(GT2): +VCCGT=55A



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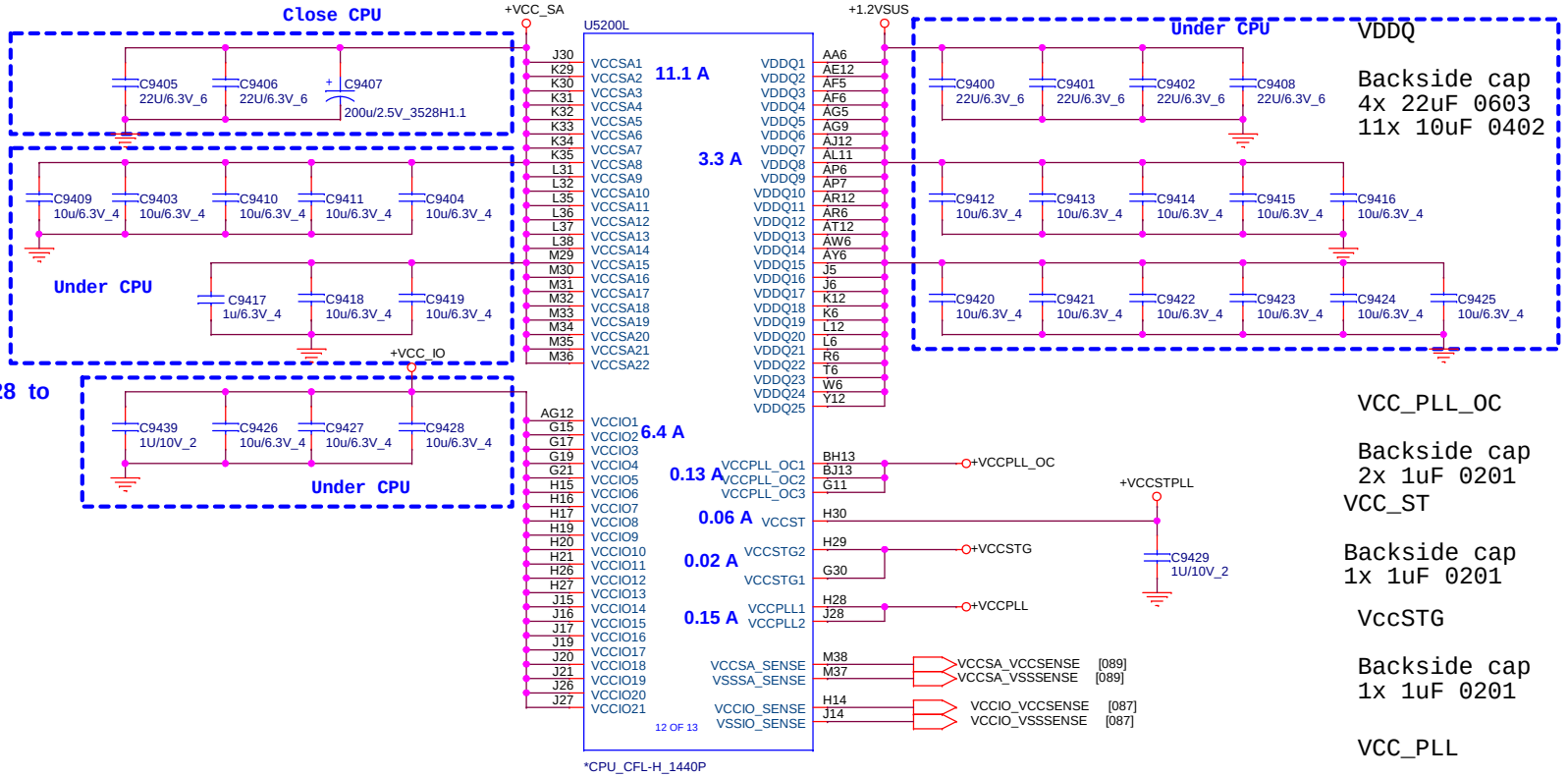
Follow CFL H EDS page 128 to 45W(GT2): VCCSA=11.1A

Follow CFL H EDS page 127 45W: VDDQ=3.3A (LPDDR4)

+VCC_SA

Edge cap
2x 47uF 0805
2x 22uF 0805

Backside cap
7x 10uF 0402
1x 1uF 0201



Follow CFL H EDS P128 to 45W: VCCIO, +VCCIO = 6.4A

+VCC_IO

Backside cap
3x 10uF 0402

VDDQ

Backside cap
4x 22uF 0603
11x 10uF 0402

VCC_PLL_OC

Backside cap
2x 1uF 0201

VCC_ST

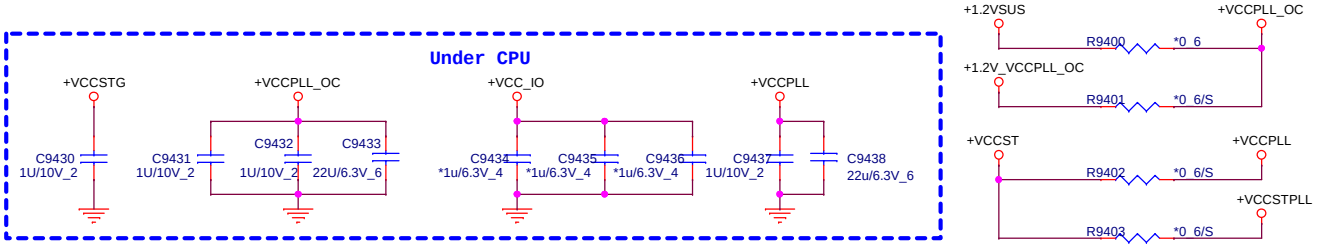
Backside cap
1x 1uF 0201

VccSTG

Backside cap
1x 1uF 0201

VCC_PLL

Backside cap
4x 22uF 0603
11x 10uF 0404



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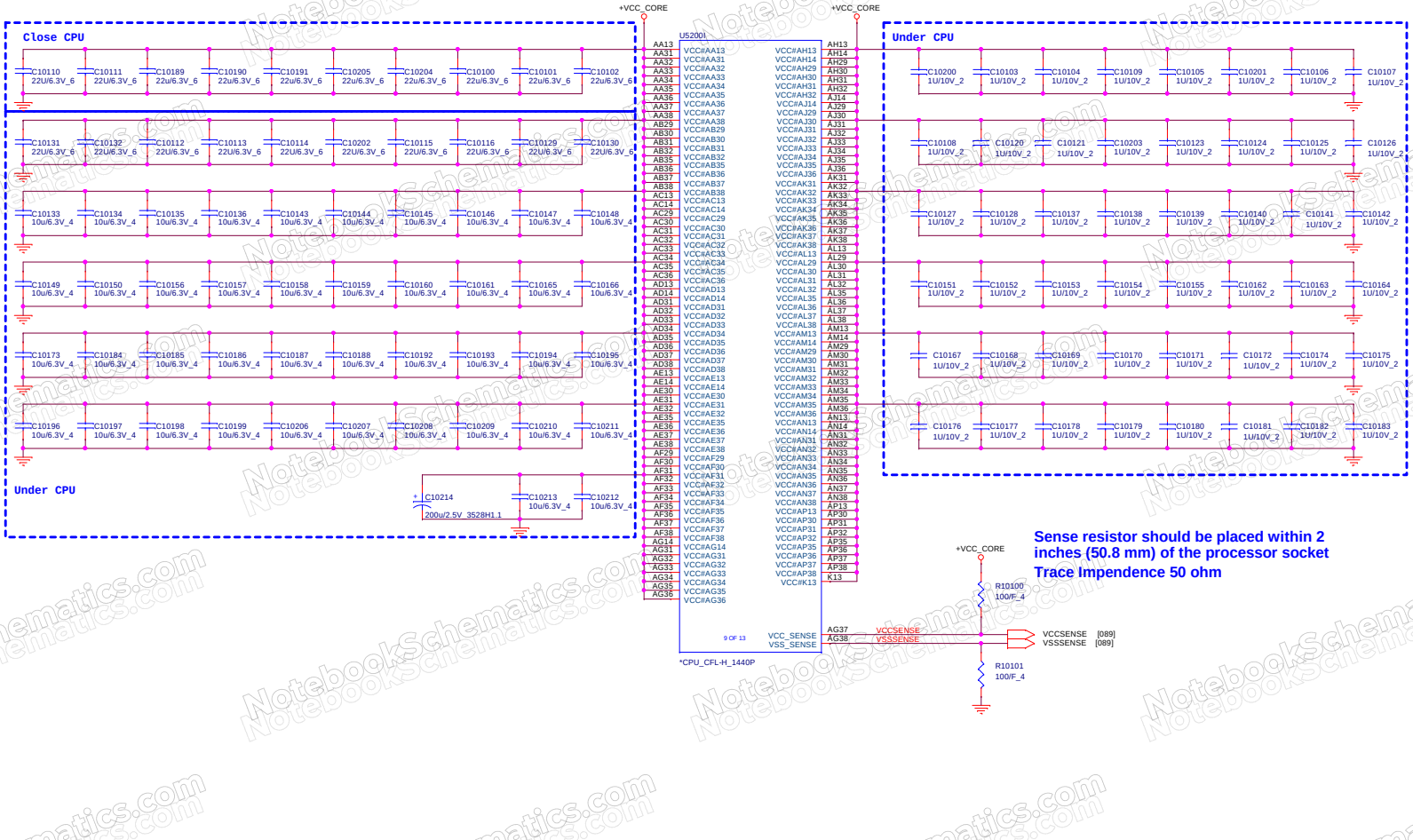
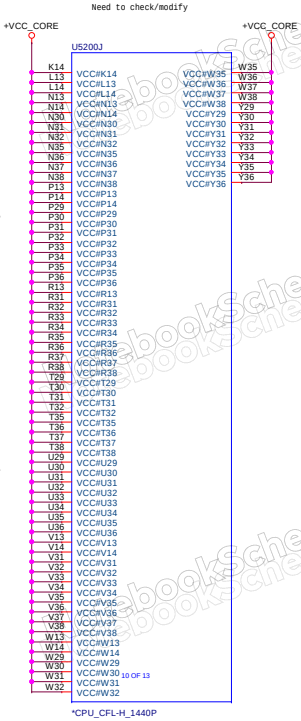
Vcc (VCC_CORE)

Edge cap
8x 47uF 0805
2x 22uF 0603

Backside cap
12x 22uF 0603
42x 10uF 0402
48x 1uF 0201
24x 0201 (placeholder)





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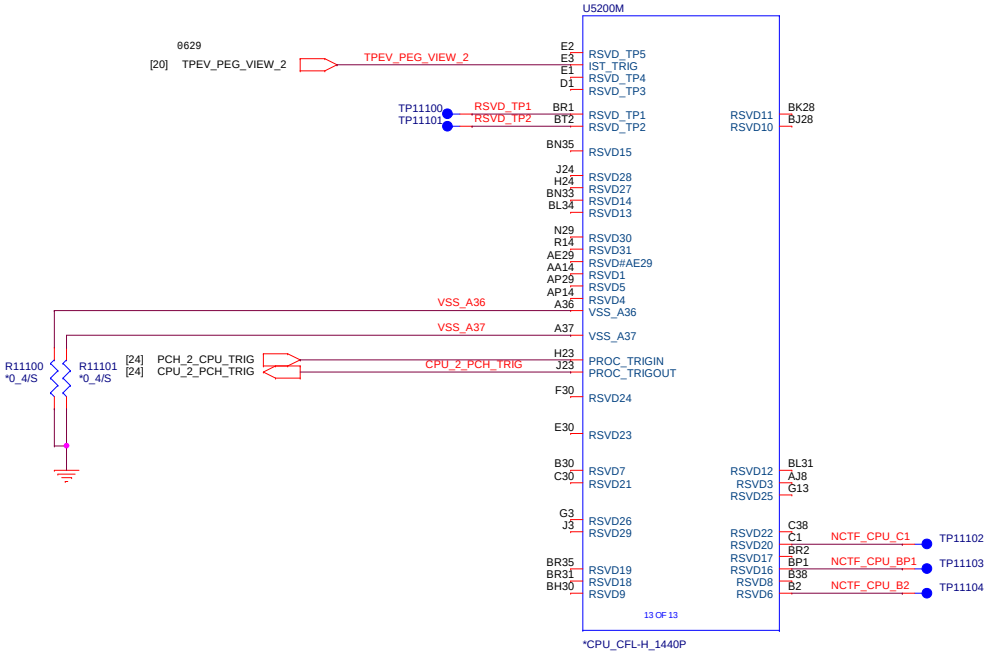
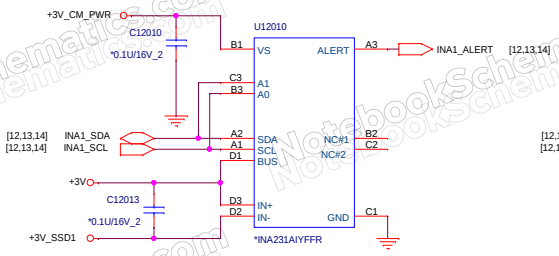
CFL-H Processor (GND)

CFL-H Processor (RESERVED, CFG)



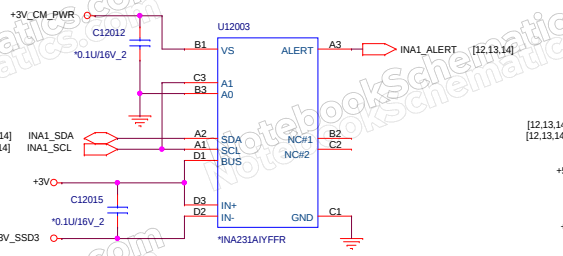
SSD1

L43000 change to CS+0106F901



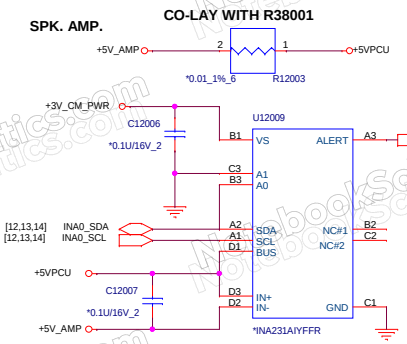
SSD3

L43002 change to CS+0106F901



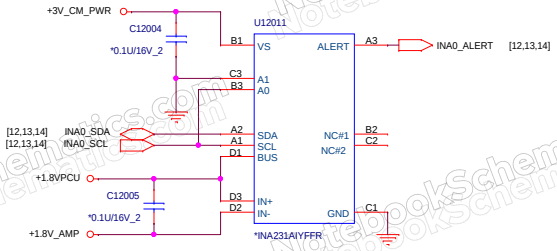
SPK. AMP.

CO-LAY WITH R38001



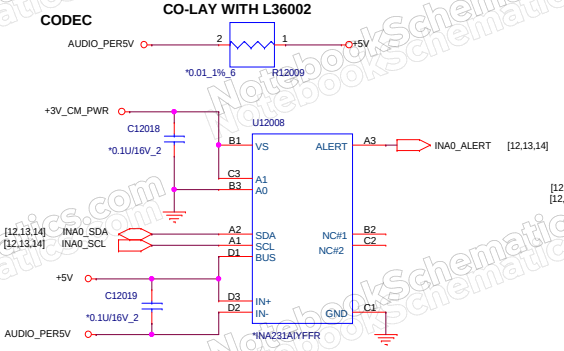
SPK. AMP.

R38002 change to CS+0106F901



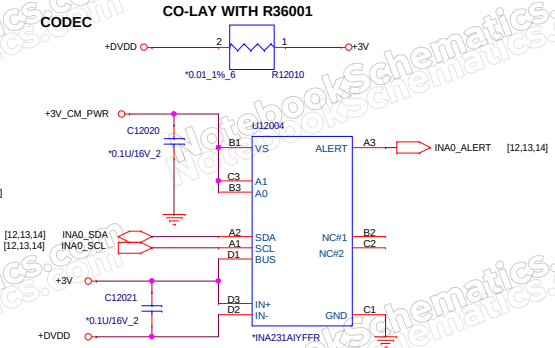
CODEC

CO-LAY WITH L36002



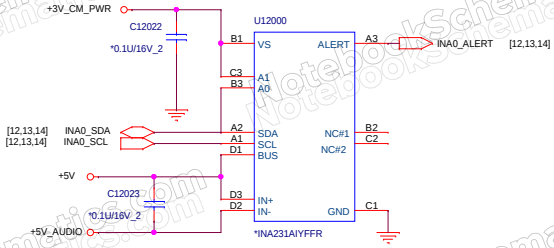
CODEC

CO-LAY WITH R36001



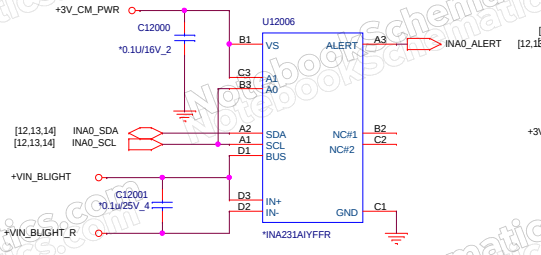
CODEC

R36024 change to CS+0106F901



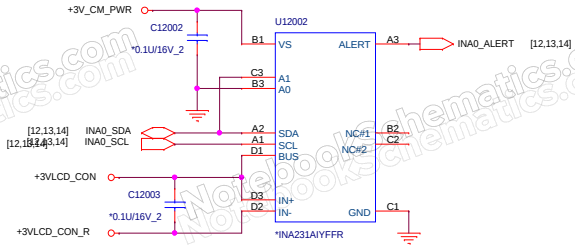
LCD BL

L34001 change to CS+0106F901



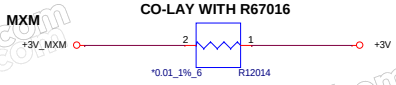
LCD T-CON

L34002 change to CS+0106F901



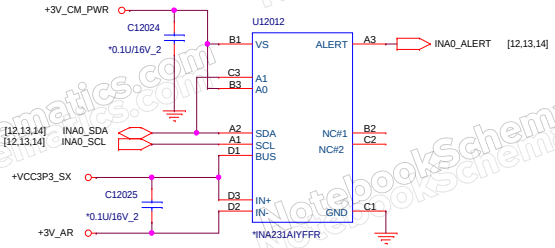
MXM

CO-LAY WITH R67016



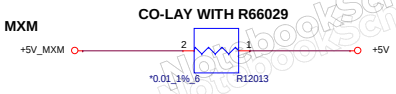
TBT

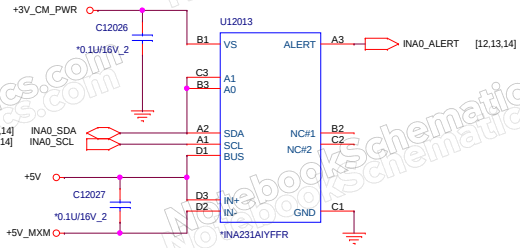
R59003 change to CS+0106F901

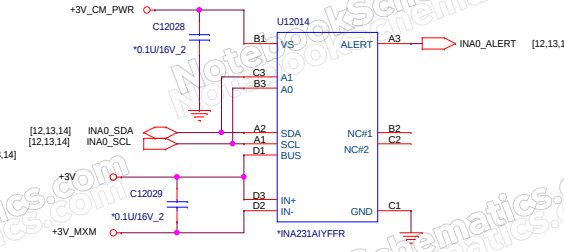


MXM

CO-LAY WITH R66029







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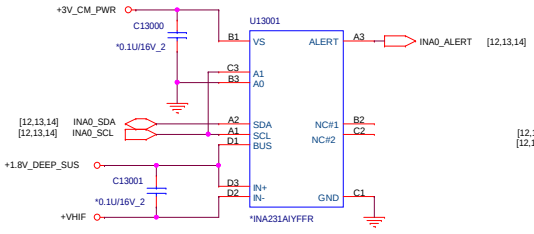
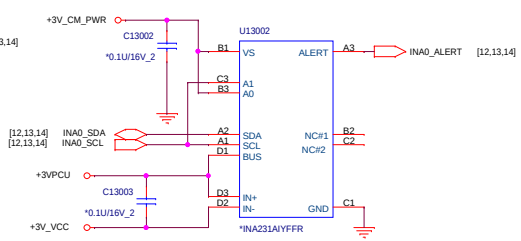
EC

R47000 change to CS+0106F901



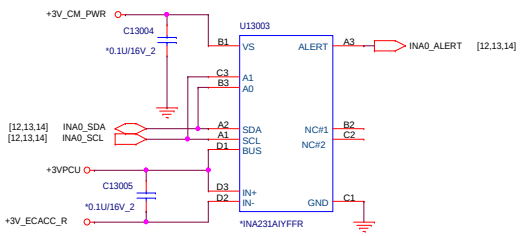
EC

R47051 change to CS+0106F901



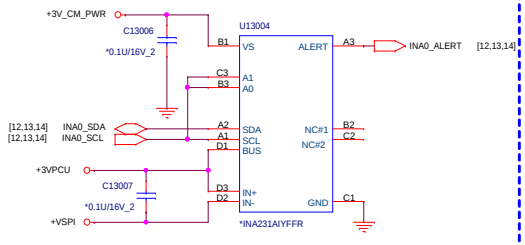
EC

L47000 change to CS+0106F901



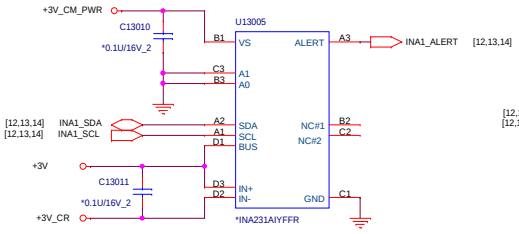
EC

R47050 change to CS+0106F901



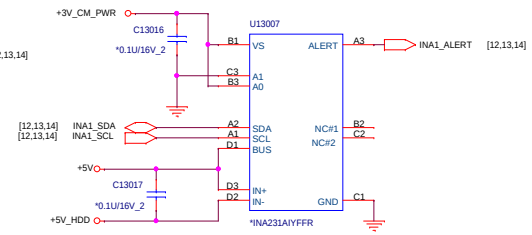
CARD READER

R55023 change to CS+0106F901



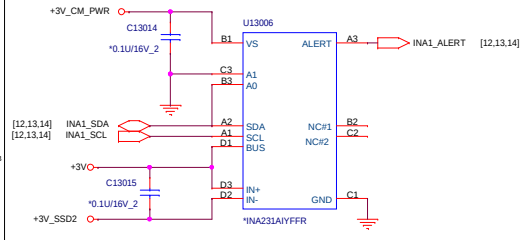
HDD

L44000 change to CS+0106F901



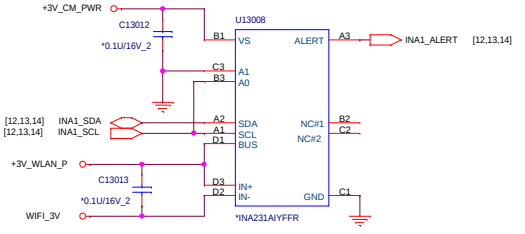
SSD2

L43001 change to CS+0106F901



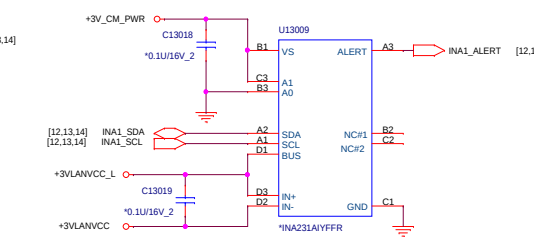
WLAN

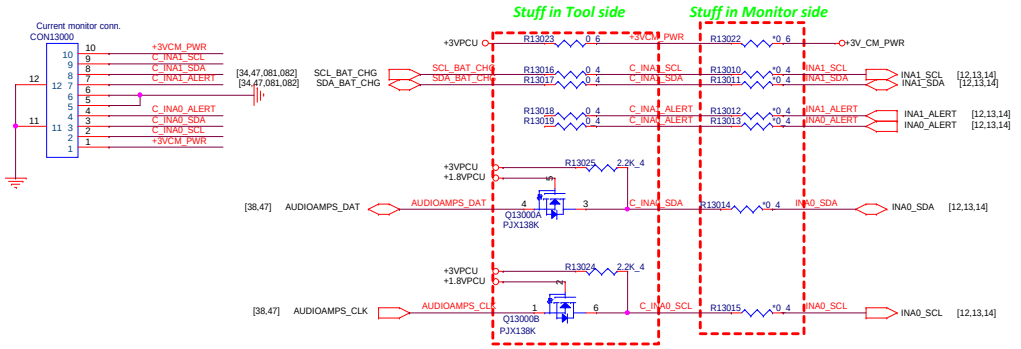
L41001 change to CS+0106F901



LAN

PR22014 change to CS+0106F901





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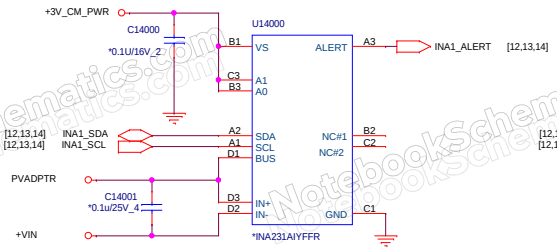
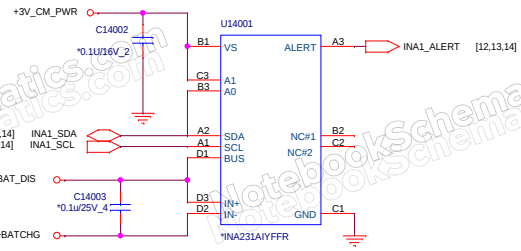
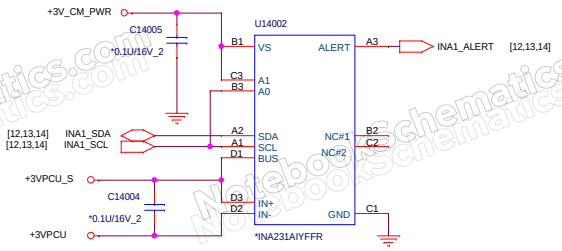
+VIN



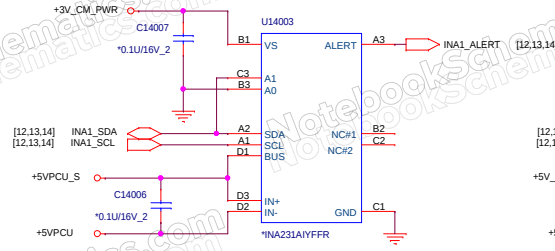
Battery



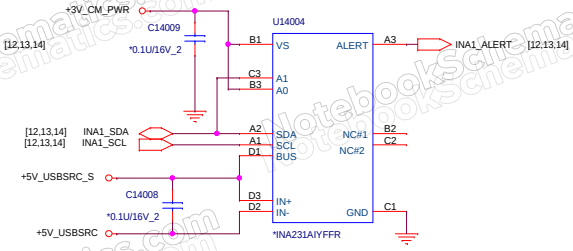
+3VPCU



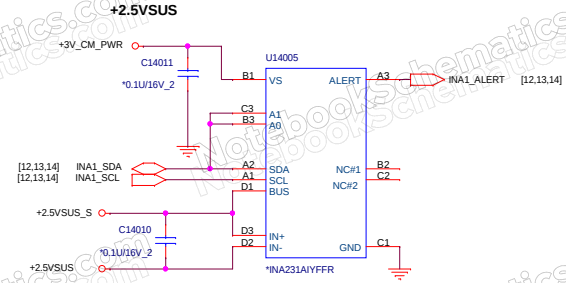
+5VPCU



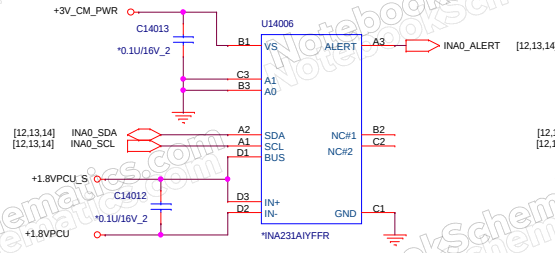
+5V_USBSRC



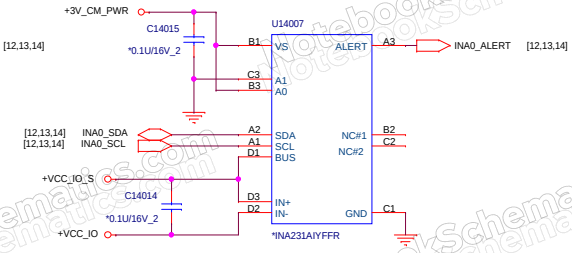
+2.5VSUS



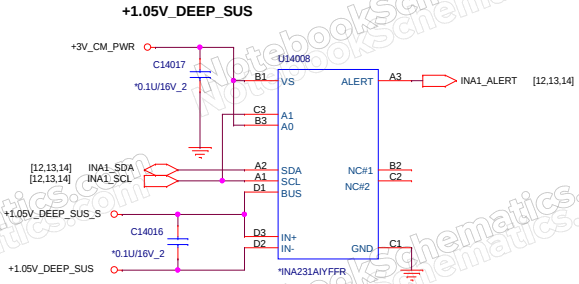
+1.8VPCU



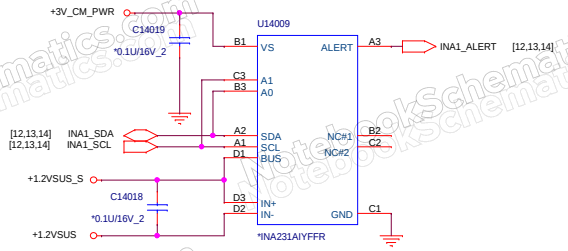
+VCC_IO



+1.05V_DEEP_SUS



+1.2VSUS



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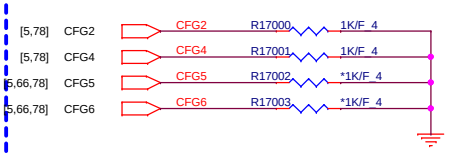
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.



Configuration Signals:			
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	x1 = Normal Operation; No stall x0 = Stall	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train immediately following RESET# de assertion x0 = PEG wait for BIOS fro assertion	

USB2.0(Right) (USBP1_TypeA-1)

WWAN (USBP3)

USB2.0(Left-1) (USBP4_TypeA-2)

USB2.0(Left-2) (USBP5_TypeA-3)

Camera (USBP7)

FPR (USBP8)

Smart Card (USBP9)

TI PD PORT A (USBP11)
(USBP12)

TI PD PORT B (USBP13)

BT (USBP14)

If OTG is not implemented on the platform, then USB2_ID and should both be connected to ground.

CARD READRE

WWAN

TBT PCIE x4

SSD3 PCIE x4

USB3.0 (Right)

USB3.0 (Left-1)

USB3.0 (Left-2)

SSD1

SSD2
HDD

PCH_CFL-H_874P

BRD_ID

BRD_ID TABLE				
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
DB0	0	0	0	0
DB0-1	0	0	0	1
DB1	0	0	1	0
	0	0	1	1
SI1	0	1	0	0
SI1R	0	1	0	1
SI2	0	1	1	0
SI2-R0	0	1	1	1
SI2-R1	1	0	0	0
PV	1	0	0	1
PVR	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

VPRO/NON-VPRO ID (For BOM only, place on TOP side)
VPRO: Un-install R18131
Non-VPRO: Install R18131

PCIE/CNVi ID (For BOM only, place on TOP side)
PCIE: Un-install R18132
CNVi: Install R18132

USB 2.0 PORT	
PORT1	USB2 MB-Right1
PORT2	WWAN
PORT3	NC
PORT4	USB2 MB-Left1
PORT5	USB2 MB-Left2
PORT6	NC
PORT7	CAMERA
PORT8	FPR
PORT9	Smart Card
PORT10	NC
PORT11	USB TYPE C (Port A)
PORT12	NC
PORT13	USB TYPE C (Port B)
PORT14	BT

USB 3.0 PORT	
PORT1	USB3 MB_TYPEA_1
PORT2	NC
PORT3	USB3 MB_TYPEA_2
PORT4	USB3 MB_TYPEA_3
PORT5~6	NC
PORT7	XQD
PORT8~10	NC

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[5,19,20,21,22,23,27,33,41,42,56,57,59,66,78,081,087,092,094,095] +3V_DEEP_SUS

HDA Bus(CLG)

U18100D

PCH_CFL-H_874P

ME Lock

RTC Circuitry(RTC)

RTC Power trace width 20mils.

30mils

XDP/DDR

DP_PWROK

PCH PWROK

From EC(+3VPCU)

PLT_ID TABLE			
	PLT_ID0	PLT_ID1	PLT_ID2
Arnchorbay	0	1	1
Venus	1	0	1

PLT_ID3	
CS	0
360	1

24-MHz Crystal Specifications (Sheet 2 of 2)

Parameter	Symbol	Recommended Value
Temperature Stability	Df/f$_o$	±30ppm
Aging	Df/f$_o$	±5ppm
Crystal Loading	C$_{load}$	18-20pF

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

Crystal Components with Surrounding 10 mil Wide GND Shield Trace Break Out:4-10 mil Wide GND Shield Trace

RTC Clock 32.768KHz
Crytsal ESR<= 50Kohm

SSD1 PCIE x4

SSD2 PCIE x4

WLAN

LAN PCIE 0602

ODD SATA

HDD SATA

For SSD1 Det (SATA1A)

For SSD2 Det (SATA4)

CNVI for WLAN

SATA LED

For debug only remove from MV

GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

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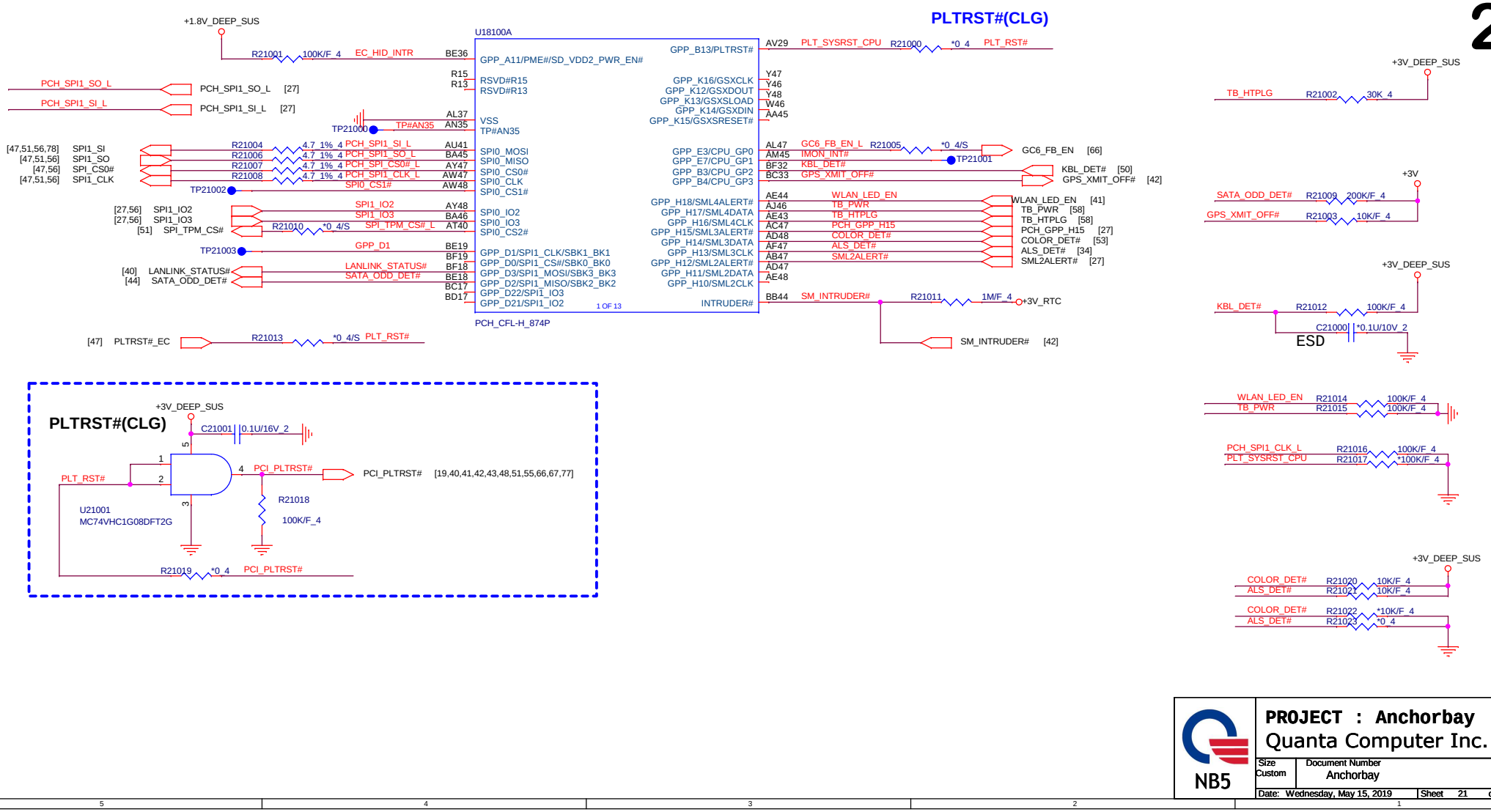

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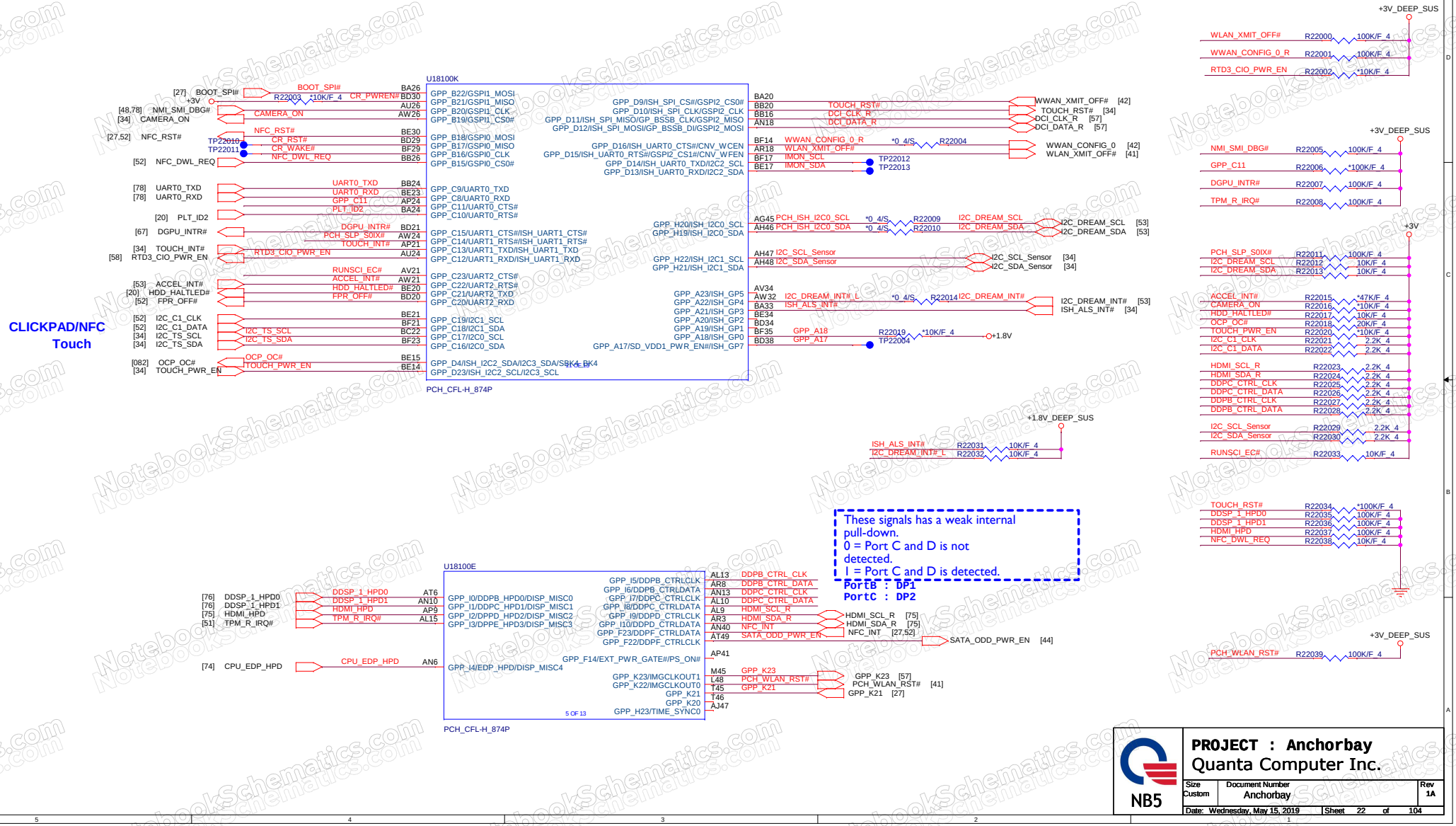
+3V_DEEP_SUS [5,18,19,20,21,23,27,33,41,42,56,57,59,66,78,081,087,092,094,095]



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Quanta Computer Inc.			
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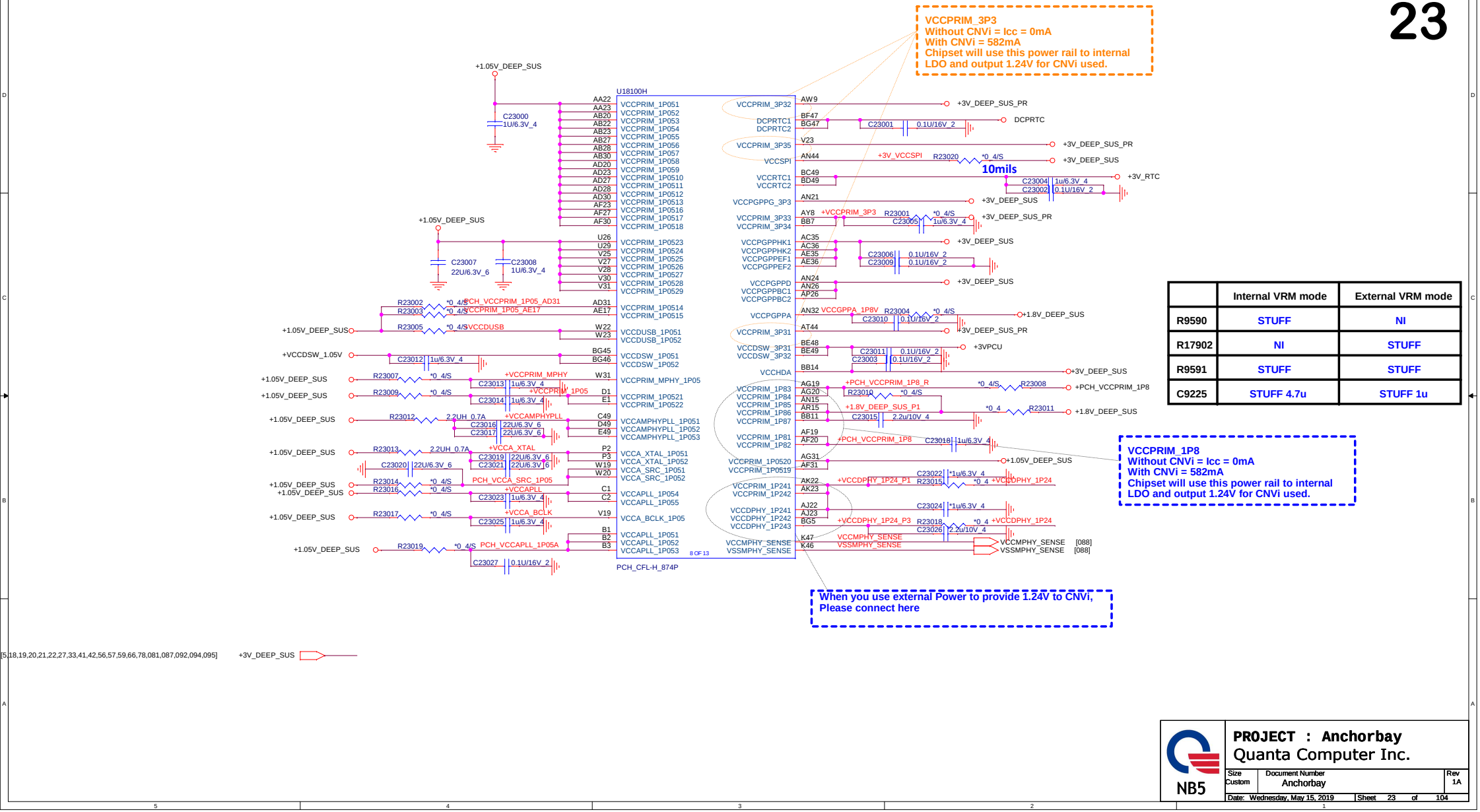

	Internal VRM mode	External VRM mode
R9590	STUFF	NI
R17902	NI	STUFF
R9591	STUFF	STUFF
C9225	STUFF 4.7u	STUFF 1u

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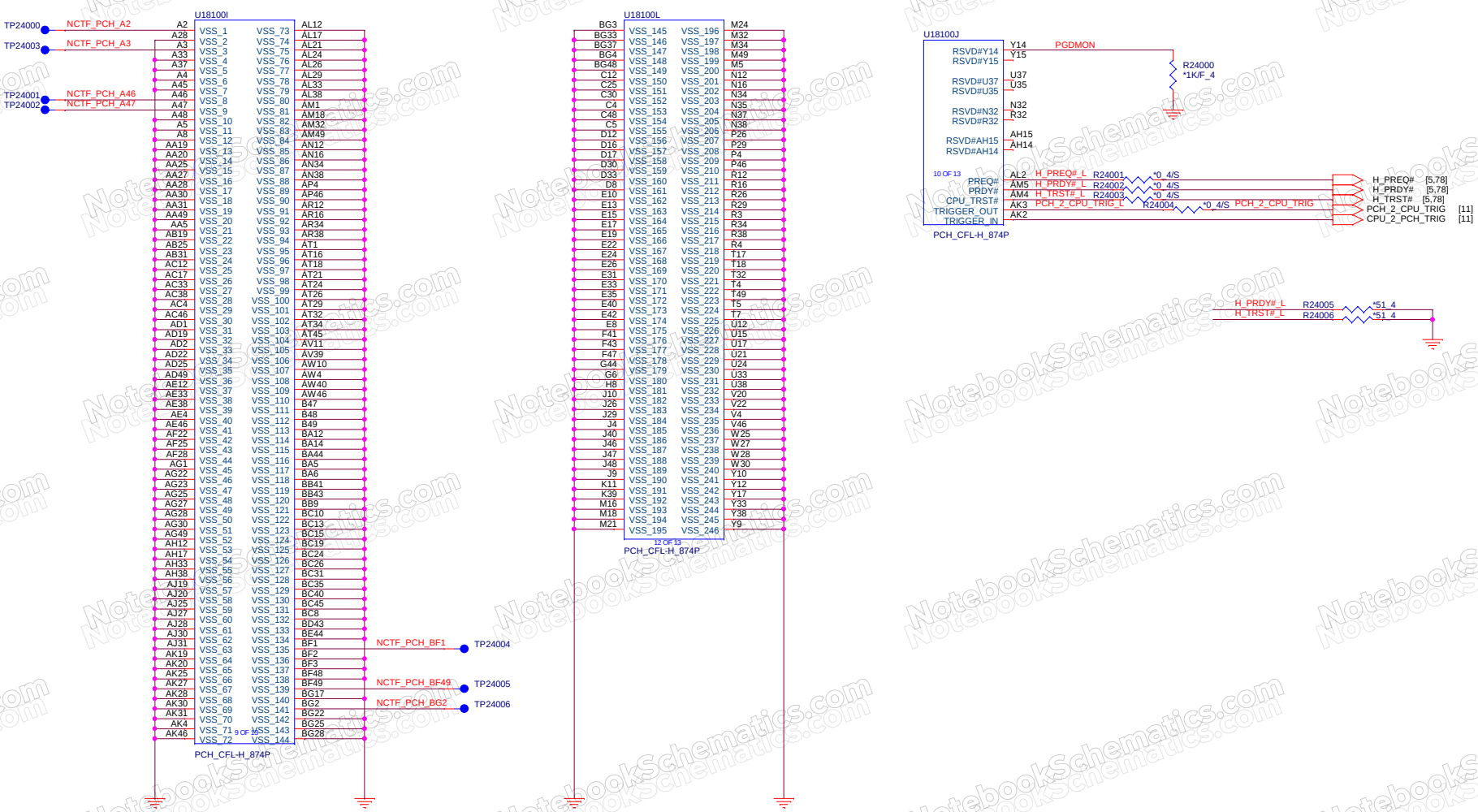

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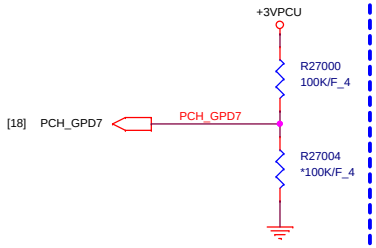
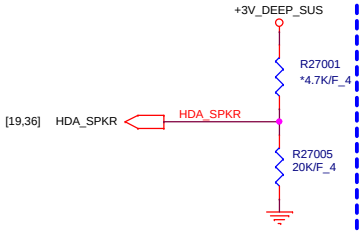
PCH Strap Pin

This strap should sample HIGH.

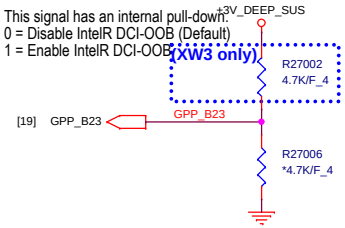


TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)

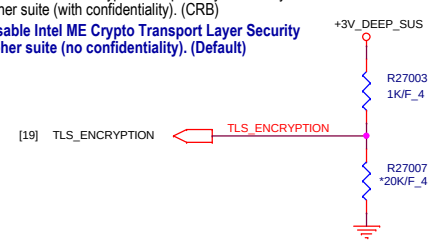


This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB **(XW3 only)**

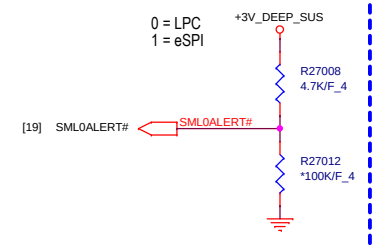


TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

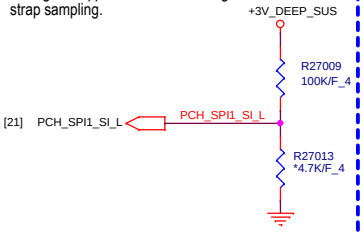


0 = LPC
1 = eSPI



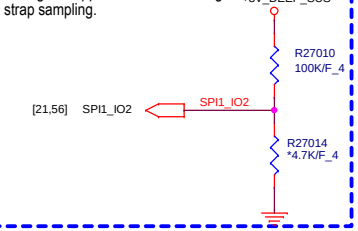
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



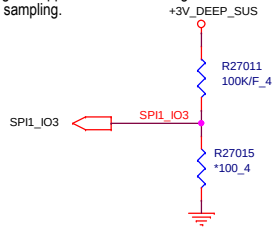
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



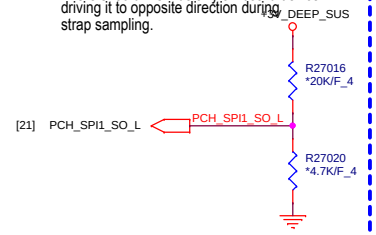
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



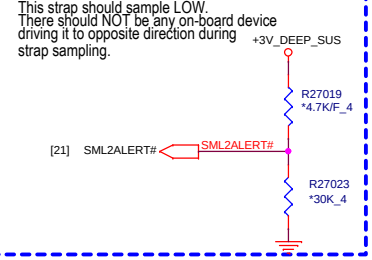
RESERVED

This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

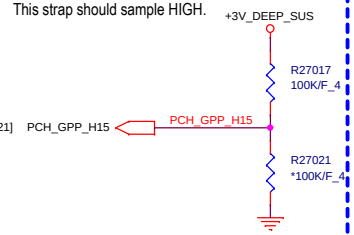


ESPI FLASH SHARING MODE

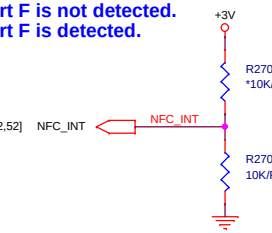
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



This strap should sample HIGH.

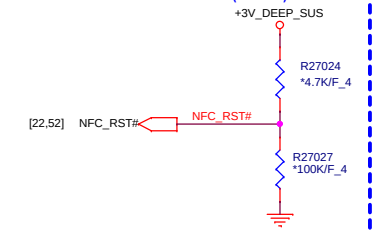


These signals has a weak internal pull-down.
0 = Port F is not detected.
1 = Port F is detected.

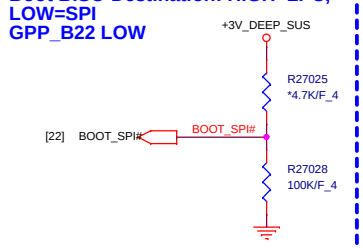


NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



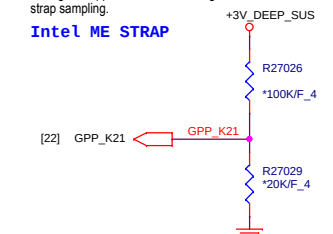
Boot BISO Destination: HIGH=LPC, LOW=SPI
GPP_B22 LOW



RESERVED

This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.

Intel ME STRAP



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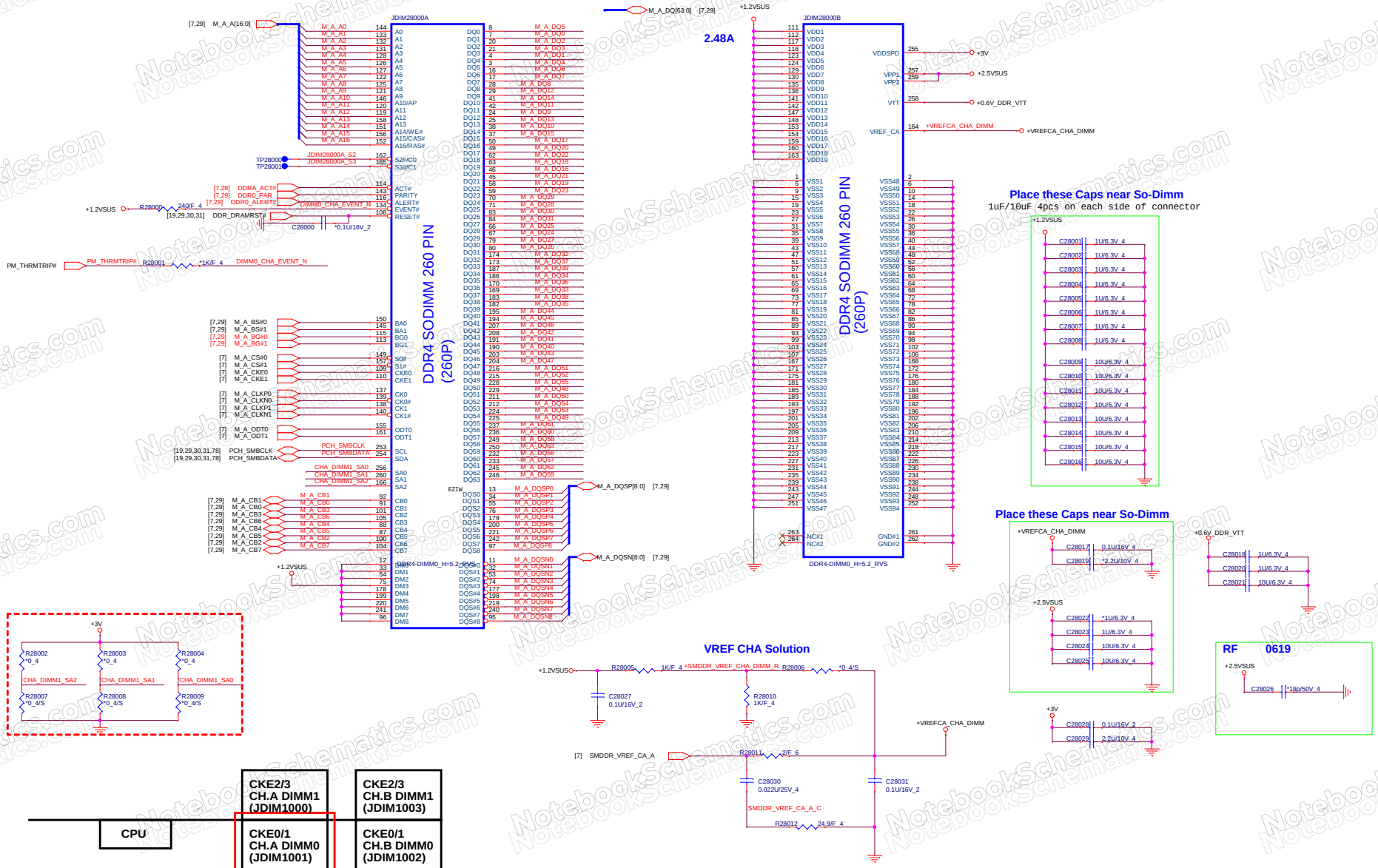

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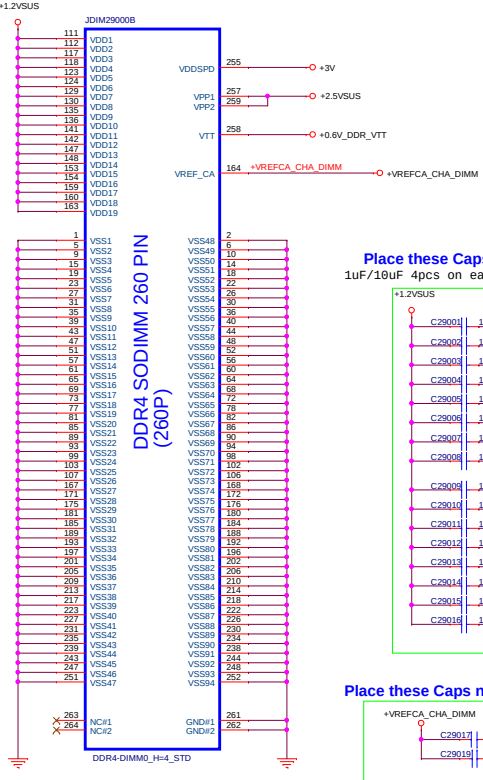
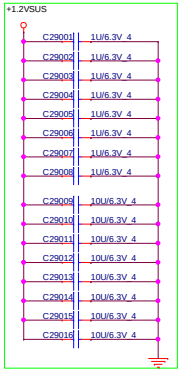
0619 change PN

2.48A

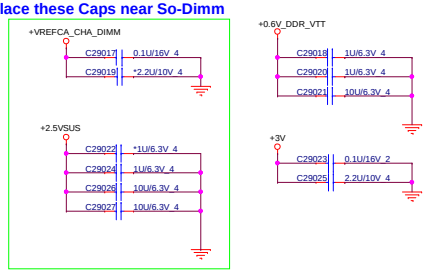


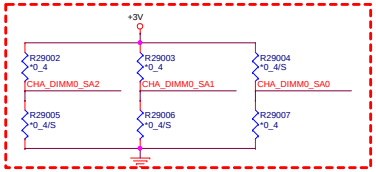
Place these Caps near So-Dimm

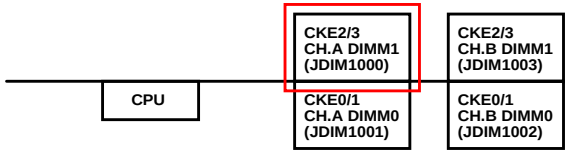
1uF/10uF 4pcs on each side of connector



Place these Caps near So-Dimm







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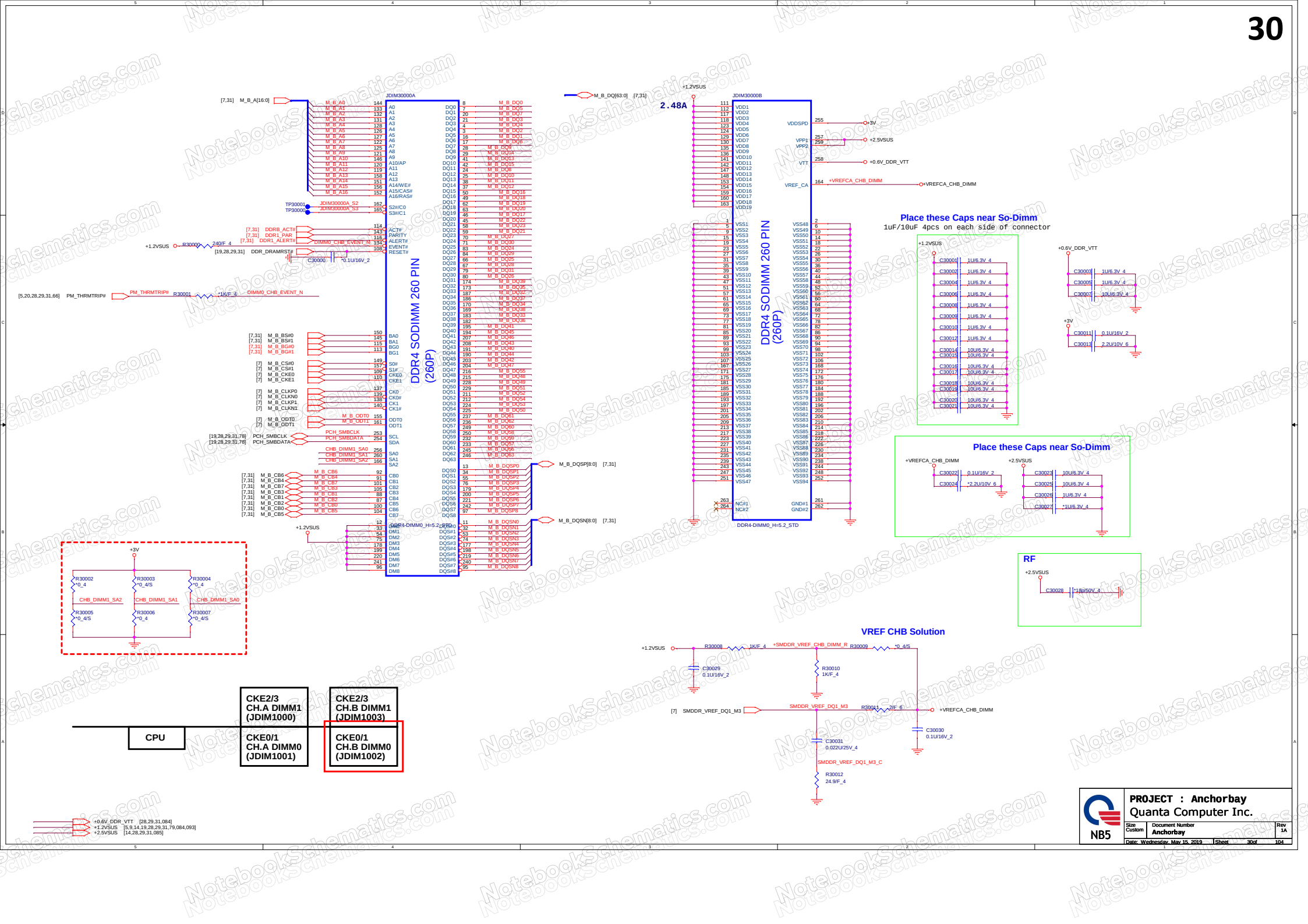
JDIM30000A
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=5.2_STD
JDIM30000B
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=5.2_STD
2.48A
Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector
Place these Caps near So-Dimm
RF
VREF CHB Solution
CPU
CKE2/3 CH.A DIMM1 (JDIM1000)
CKE0/1 CH.A DIMM0 (JDIM1001)
CKE2/3 CH.B DIMM1 (JDIM1003)
CKE0/1 CH.B DIMM0 (JDIM1002)
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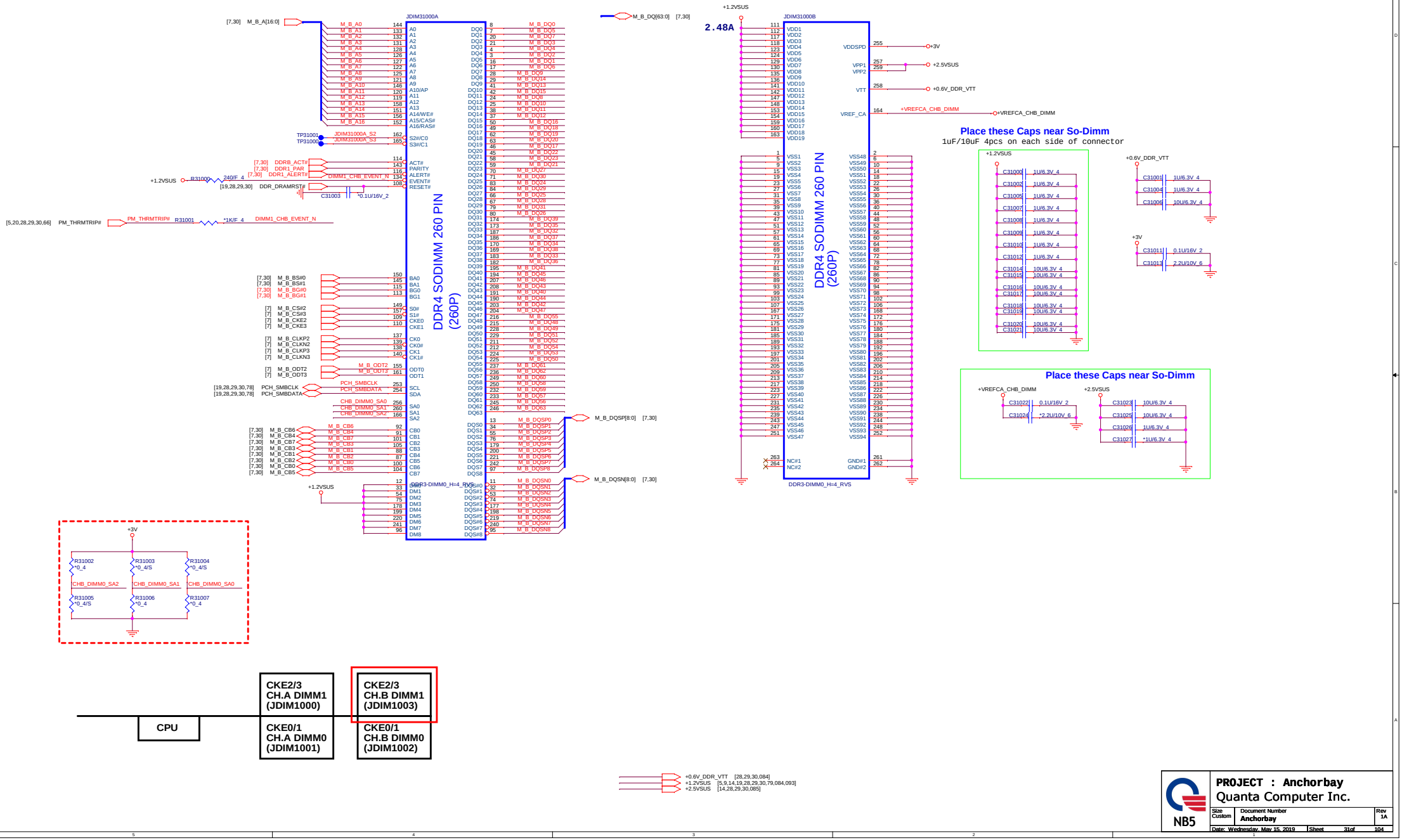
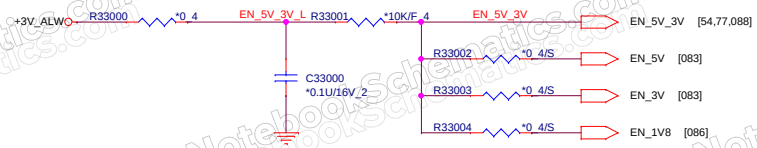
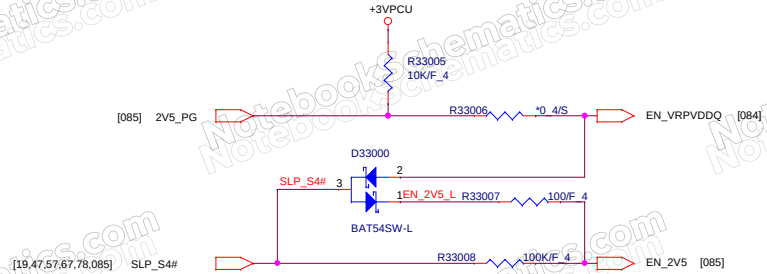
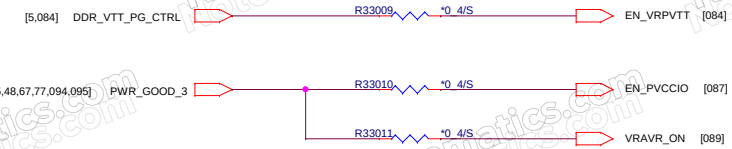
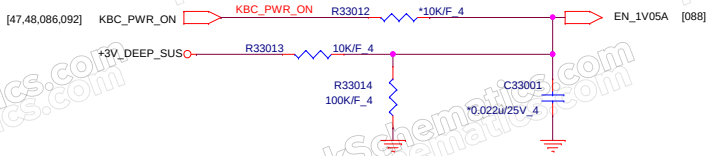
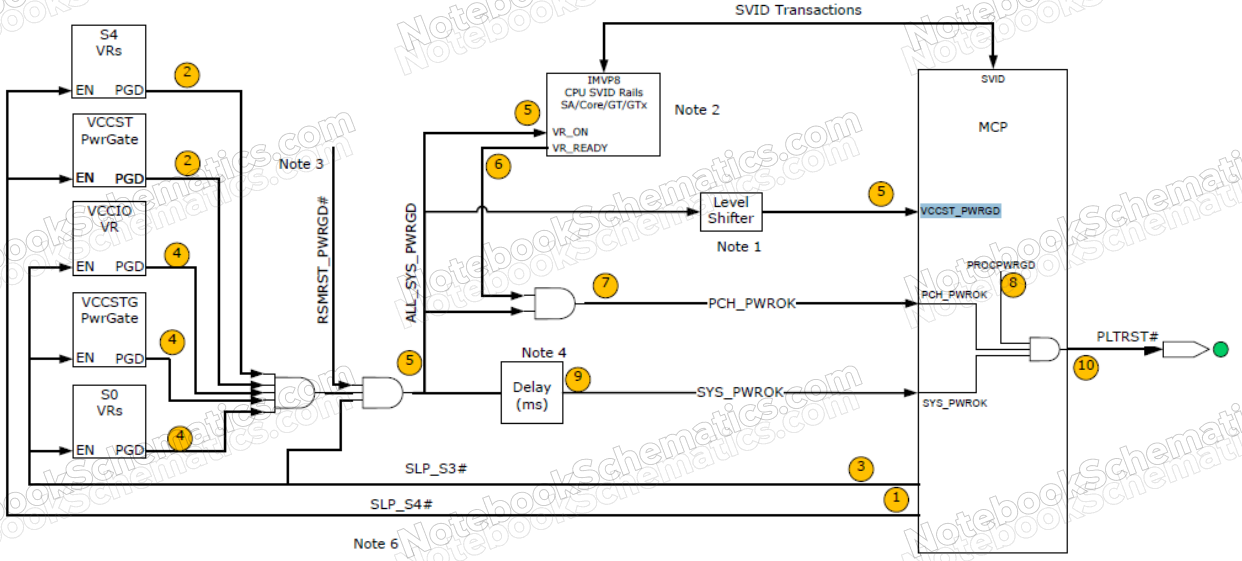

JDIM31000A
DDR4 SODIMM 260 PIN (260P)
JDIM31000B
DDR4 SODIMM 260 PIN (260P)
DDR3-DIMM0_H=4_RVS
2.48A
Place these Caps near So-Dimm
1uF/10uF 4pcs on each side of connector
Place these Caps near So-Dimm
CPU
CKE2/3 CH.A DIMM1 (JDIM1000)
CKE0/1 CH.A DIMM0 (JDIM1001)
CKE2/3 CH.B DIMM1 (JDIM1003)
CKE0/1 CH.B DIMM0 (JDIM1002)











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LID Switch

	Cable side	PP_DETECT#_EDP	PP_DETECT#
Normal FHD	Pin 21 Gnd Bar	Low	High
Normal QHD	Pin21 Gnd Bar	Low	High
Privacy	Pin 21 Floating	High	Low

OCP : 0.8A

OCP : 0.8A

OCP : 3.2A

OCP : 0.4A

HDMI

+5V_HDMIC
C35000
*0.01U/50V_4
for EMI request

ESD chip, reserve
U35001
C_TX1_HDMI- R
C_TX1_HDMI+ R
C_TX2_HDMI- R
C_TX2_HDMI+ R
CH1 CH2 GND#1 CH3 CH4
NC#1 NC#2 GND#2 NC#3 NC#4
*PUSB3FR4

ESD chip, reserve
U35002
C_TX0_HDMI- R
C_TX0_HDMI+ R
C_IN_CLK# R
C_IN_CLK R
CH1 CH2 GND#1 CH3 CH4
NC#1 NC#2 GND#2 NC#3 NC#4
*PUSB3FR4

EMI Solution
C_TX2_HDMI+ R R35004 *120_2 C_TX2_HDMI- R
C_TX1_HDMI+ R R35005 *120_2 C_TX1_HDMI- R
C_TX0_HDMI+ R R35006 *120_2 C_TX0_HDMI- R
C_IN_CLK_R R35007 *120_2 C_IN_CLK# R

+5V_USBSRC
C35001 1u/6.3V_4
U35000
IN OUT GND EN OC
G524B1T11U
[19,35,48,57,58,67,78,084,092,093,095] SLP_S3#
R35001 *100K/F_4
+5V_HDMIC_OC *100K/F_4 R35000
+5V_USBSRC
+5V_HDMIC
C35002 0.01u/50V_4
C35003 0.1U/16V_2
C35004 10u/6.3V_4

[75] HDMI_UP_DATA HDMI_UP_DATA
[75] HDMI_UP_CLK HDMI_UP_CLK

CON35000
X_DP(PWR)
D2+ GND_2 D2- D1+ GND_5 D1- D0+ GND_8 D0- CK+ GND_11 CK- CE Remote NC DDC CLK DDC DATA GND_DPAUX +5V HP DET HD_DP_Option
SHELL1 SHELL2
HDMI CONN
[75] C_TX2_HDMI+_R
[75] C_TX2_HDMI-_R
[75] C_TX1_HDMI+_R
[75] C_TX1_HDMI-_R
[75] C_TX0_HDMI+_R
[75] C_TX0_HDMI-_R
[75] C_IN_CLK_R
[75] C_IN_CLK#_R
+5V_HDMIC
R35002 3.9K/F_4
R35003 3.9K/F_4
HDMI_UP_CLK
HDMI_UP_DATA
C35005 *10P/50V_4
C35006 *10P/50V_4
[75] HDMI_HPD_R
HDMI_HPD_R
VC35000 *TVM0G5R5M220R
C35007 220p/50V_4

Current 1.5A
+3V_MDP
U35003
+3VPCU
[19,35,48,57,58,67,78,084,092,093,095] SLP_S3#
IN#2 IN#1 EN OUT GND
G5245AT11U
C35009 *0.1U/16V_2
C35008 0.1U/16V_2

Mini DP

CON35001
MINI DISPLAY PORT
[75] C_OUT_DP_TXP0
[75] C_OUT_DP_TXN0
[75] C_OUT_DP_TXP1
[75] C_OUT_DP_TXN1
[75] C_OUT_DP_TXP2
[75] C_OUT_DP_TXN2
GND1 L0+ L0- GND2 L1+ L1- GND3 L2+ L2- GND4
HPD Config1 Config2 GND6 L3+ L3- GND5 AUX_CH+ AUX_CH- DP_PWR
SHELL1 SHELL2 SHELL3 SHELL4 SHELL5 SHELL6
Mini DP CONN
R35008 *0_4/S DP_HPD_PCH [75]
INT_DP_HPD
PS8469_DP_CA_DET
MDP_CFG2
R35009 100K/F_4
R35010 5.1M_4
R35011 1M/F_4
PS8469_DP_CA_DET [75]
C_OUT_DP_TXP3
C_OUT_DP_TXN3
C_OUT_DP_TXP3 [75]
C_OUT_DP_TXN3 [75]
1.1A/6V
C_INT_DP_AUXP
C_INT_DP_AUXN_GS
C_INT_DP_AUXP [75]
C_INT_DP_AUXN_GS [75]
+3V_MDP
+3V_MDP
C35010 10U/6.3V_4
C35011 0.1U/16V_2

C_INT_DP_AUXN_GS R35012 100K/F_4 +3V
C_INT_DP_AUXP R35013 100K/F_4

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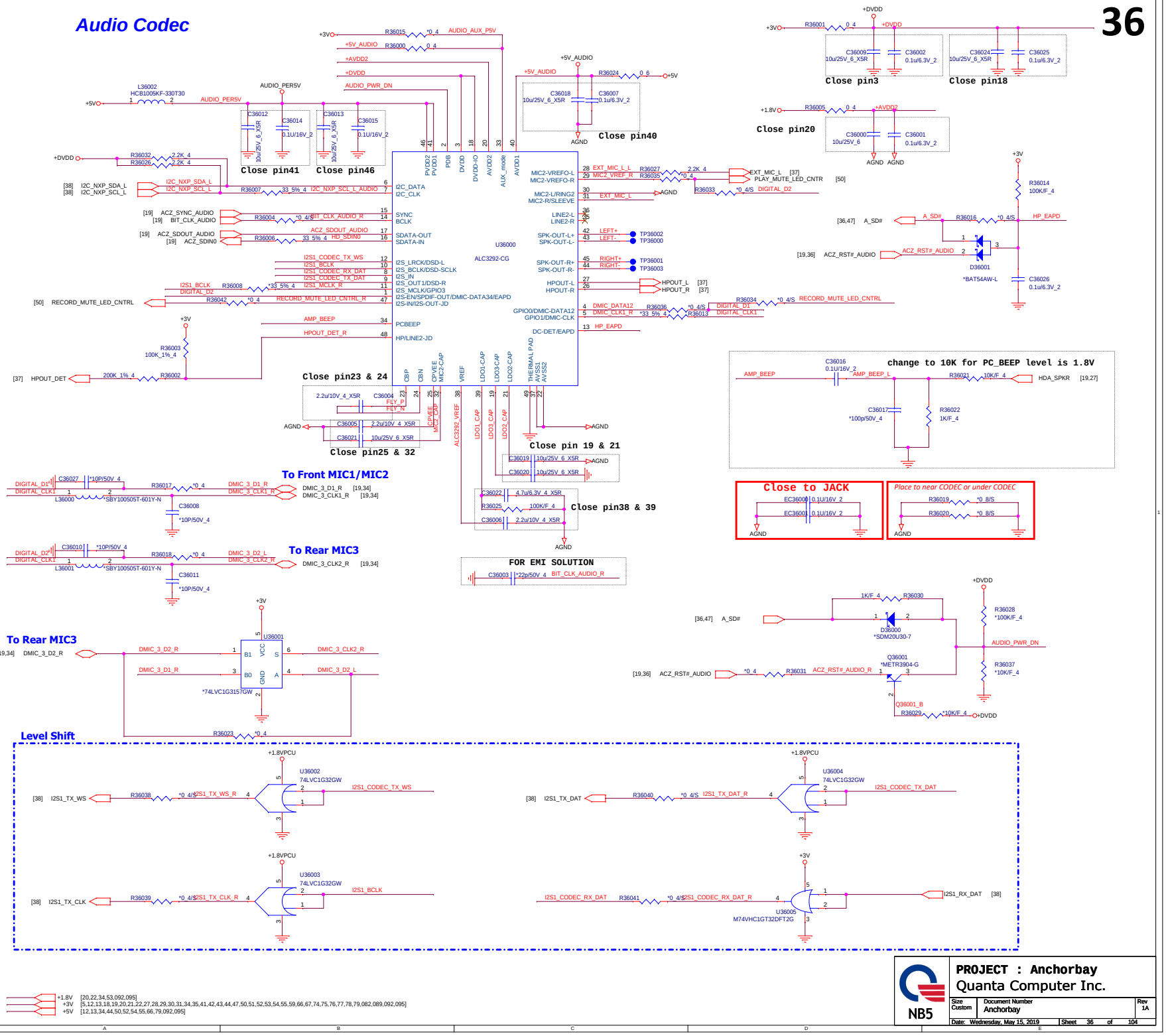
Audio Codec


U36000
ALC3292-CG
Close pin41
Close pin46
Close pin23 & 24
Close pin25 & 32
Close pin40
Close pin20
Close pin3
Close pin18
Close pin19 & 21
Close pin38 & 39
change to 10K for PC_BEEP level is 1.8V
Close to JACK
Place to near CODEC or under CODEC
To Front MIC1/MIC2
To Rear MIC3
To Rear MIC3
FOR EMI SOLUTION
Level Shift
U36001
74LVC1G3157GW
U36002
74LVC1G32GW
U36003
74LVC1G32GW
U36004
74LVC1G32GW
U36005
M74VHC1GT32DFT2G
L36002
HCB1005KF-330T30
L36000
L36001
*SBY100505T-601Y-N
D36000
*SDM20U30-7
D36001
*BAT54AW-L
Q36001
*METR3904-G
Q36001_B
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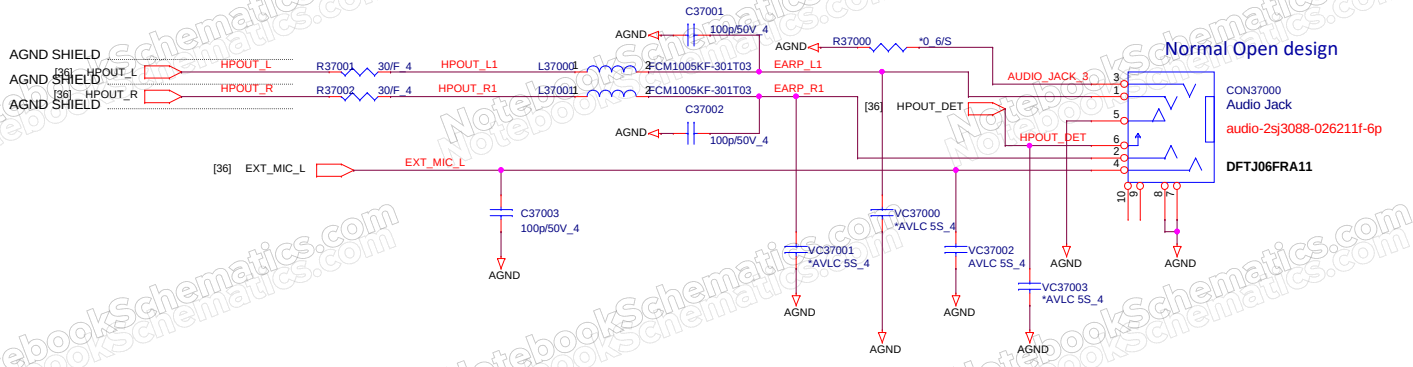
Head Phone/MIC combo jack



NB5

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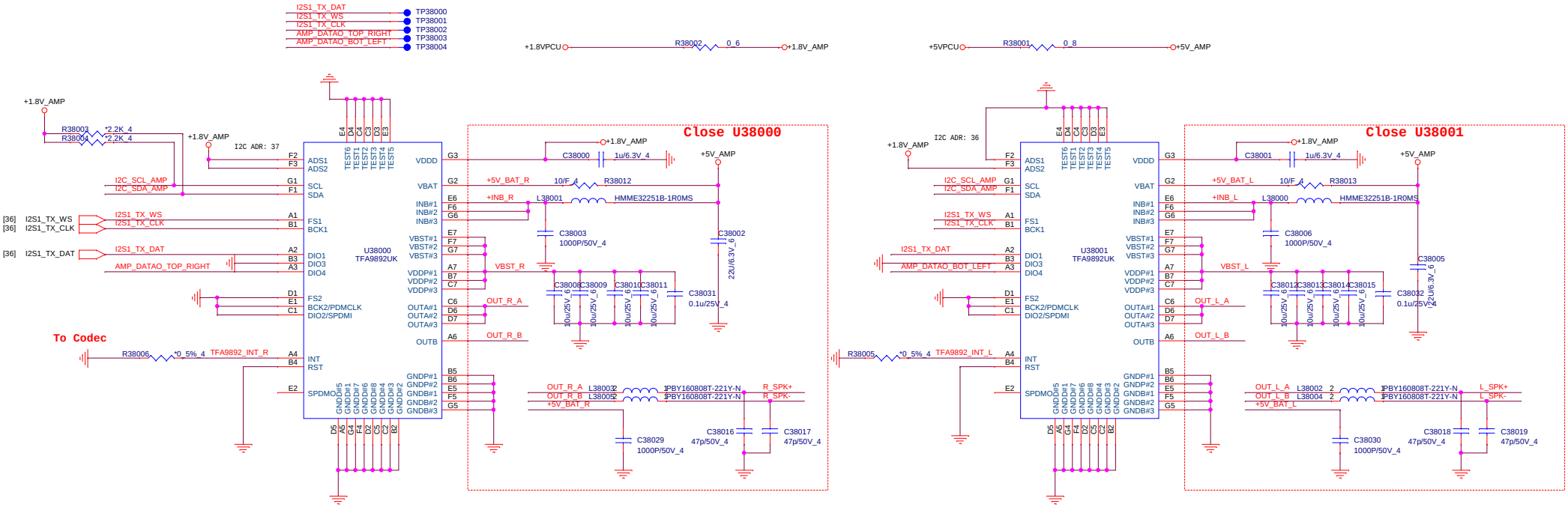
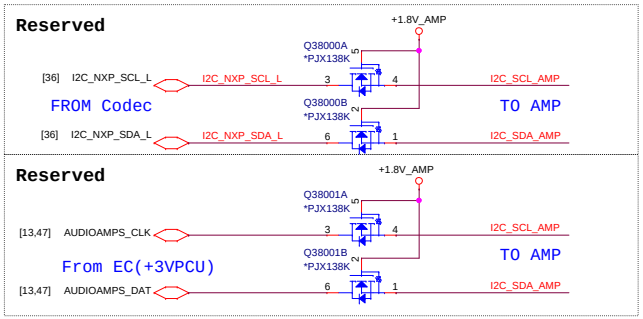
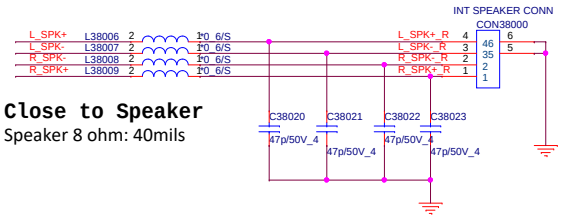
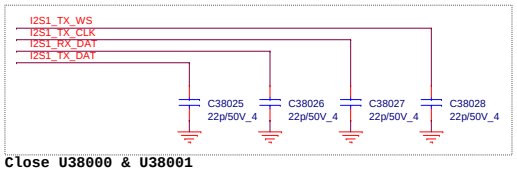
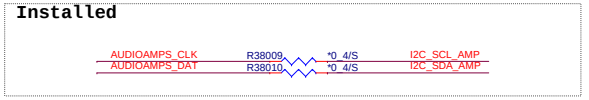


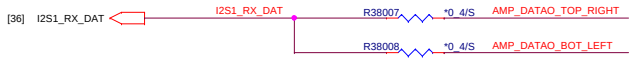


0615
update footprint









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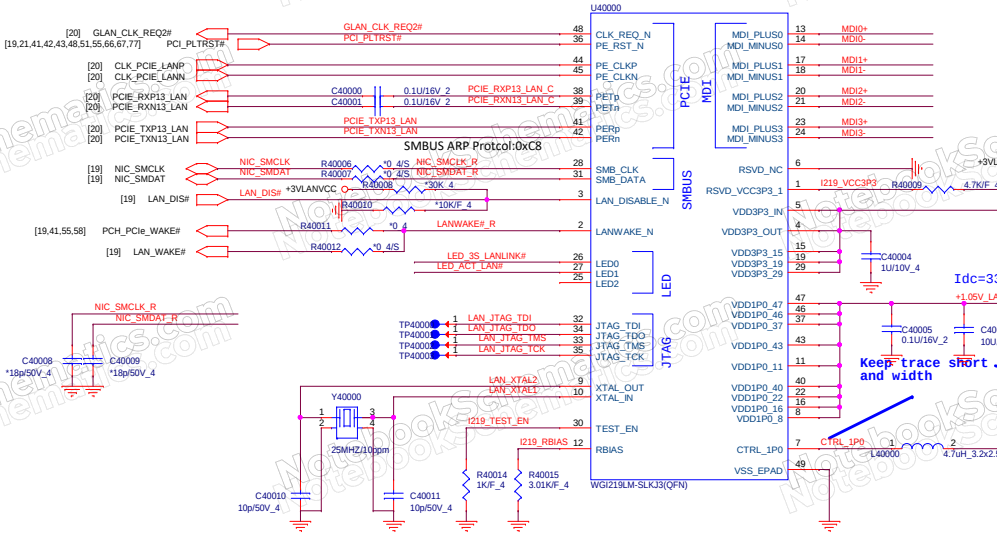
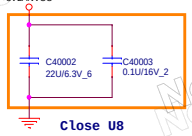
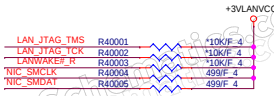
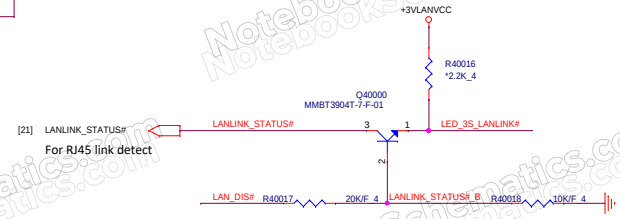


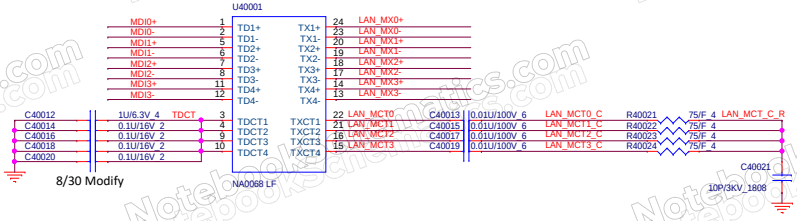


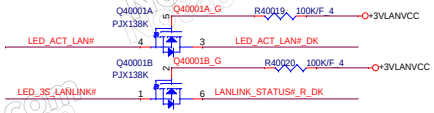


Shared with +1.05V_PCH SVR	Used internal SVR
No stuff L15	Stuff L15
Stuff R151	No stuff R151

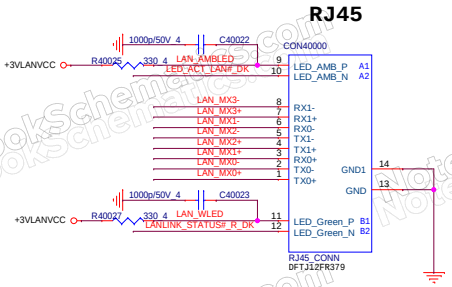


Transformer for 10/100/1000





RJ45



WIFI&BT

Mini Card
WLAN/BT(Option)
Max Load 2.5A for WLAN

If CNVi is present CNVi = Low, load switch will never turn off
If CNVi is not present CNVi = High, load switch EN pin will follow WLAN_DISABLE

Windstorm Peak & Jefferson Peak 2 M.2 1216 co-layout
Intel Dual Band Wireless-AC 8265
Intel Dual Band Wireless-AC 9560

Not used by Jefferson Peak

Not used by Jefferson Peak

Stuff for PCIE module

Place close to WIFI module

Intel LAN		
VPRO 9560.NGWGQ	ADPC9560003	TOP BS
	ADPC9560002	QBCON
NON-VPRO 9560.NGWG.NVQ	ADPC9560005	TOP BS
	ADPC9560004	QBCON

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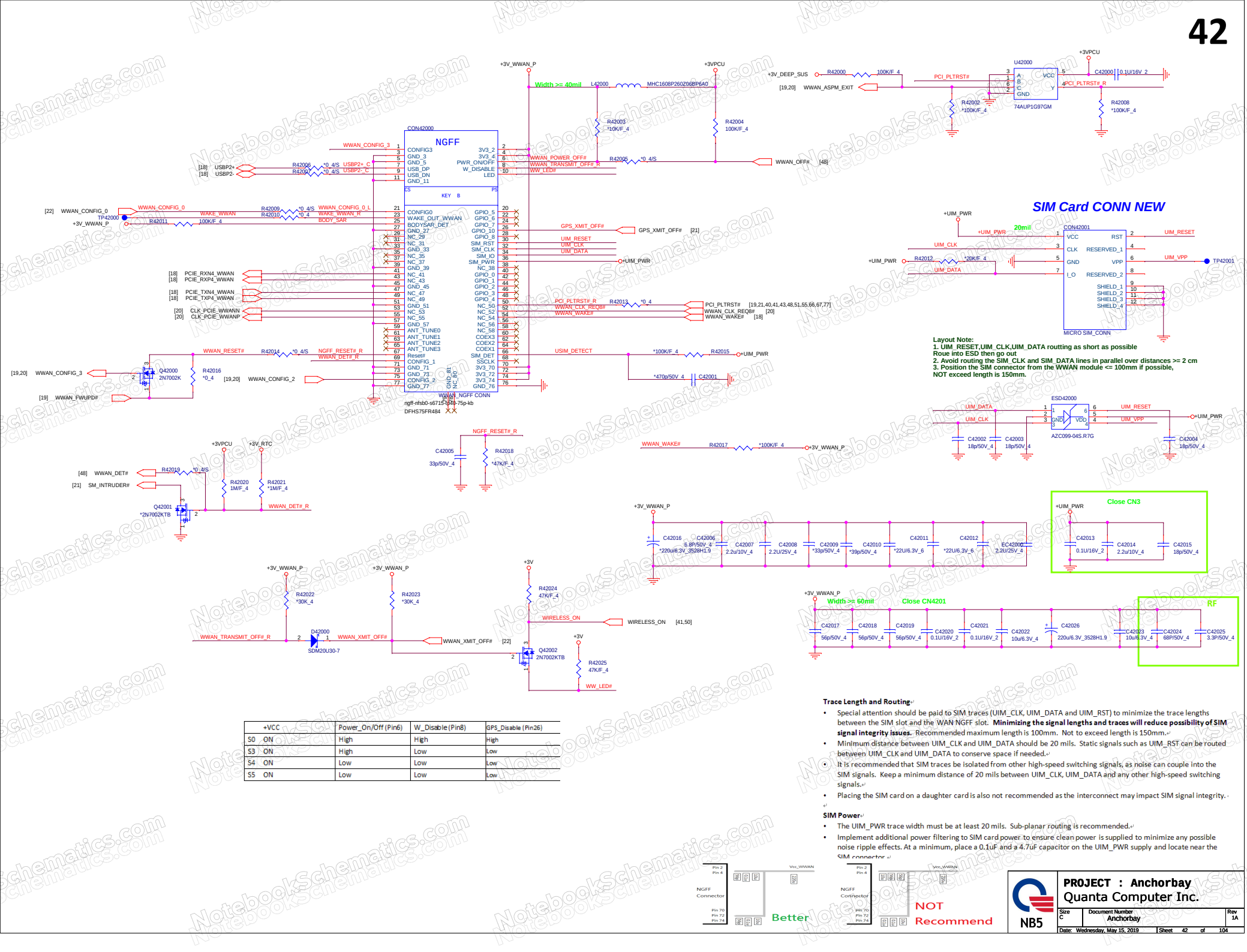
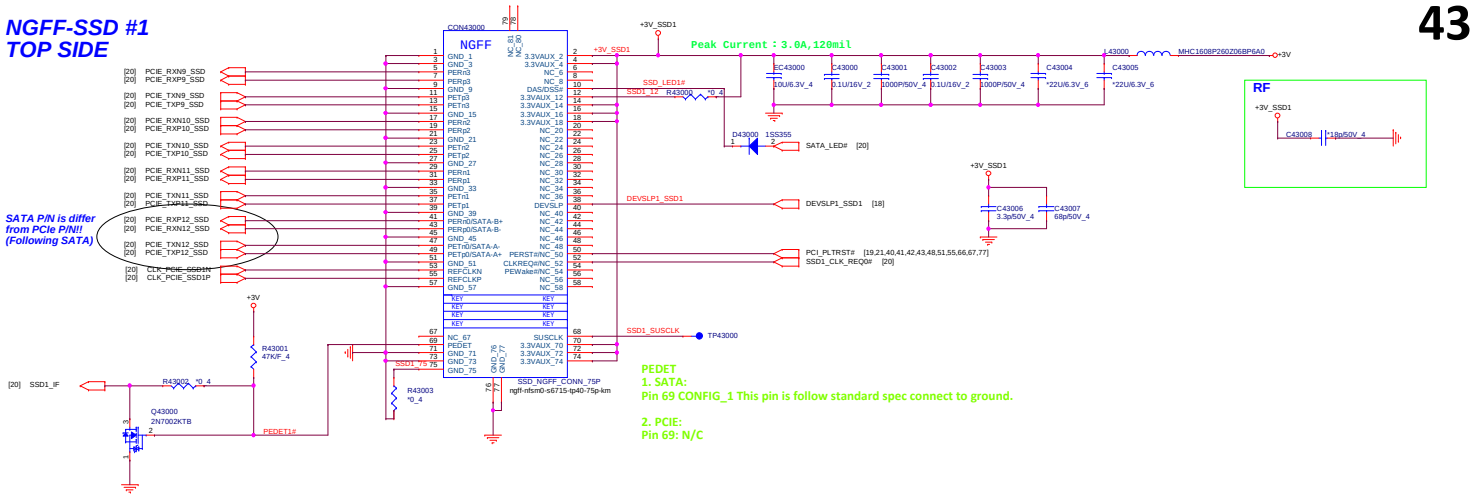


+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

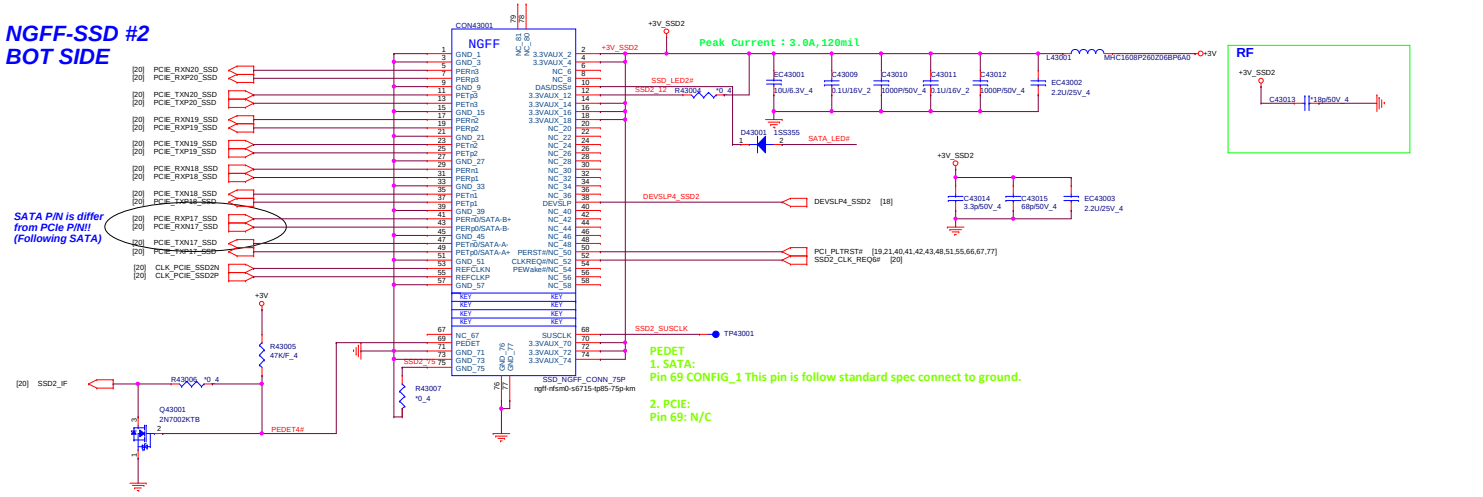
NGFF-SSD #1 TOP SIDE



PEDET
1. SATA:
Pin 69 CONFIG_1 This pin is follow standard spec connect to ground.

2. PCIE:
Pin 69: N/C

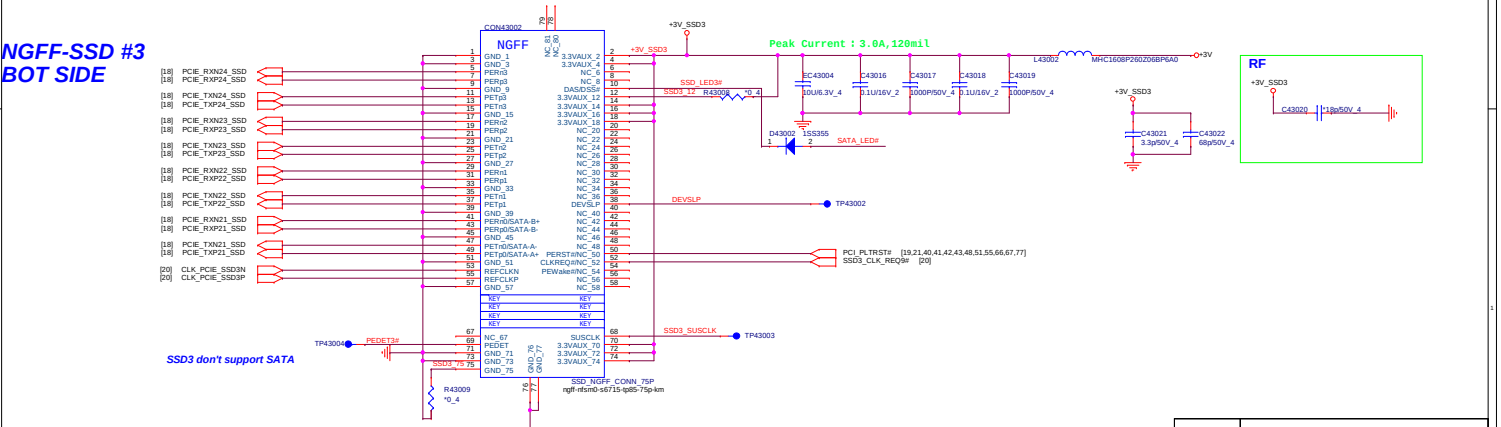
NGFF-SSD #2 BOT SIDE



PEDET
1. SATA:
Pin 69 CONFIG_1 This pin is follow standard spec connect to ground.

2. PCIE:
Pin 69: N/C

NGFF-SSD #3 BOT SIDE



[5,12,13,18,19,20,21,22,27,28,29,30,31,34,35,36,41,42,44,47,50,51,52,53,54,55,59,66,67,74,75,76,77,78,79,082,089,092,095]

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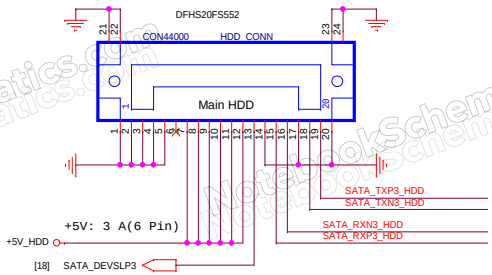
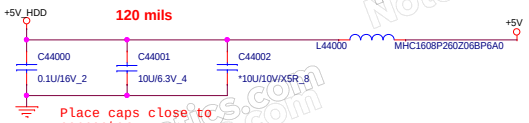
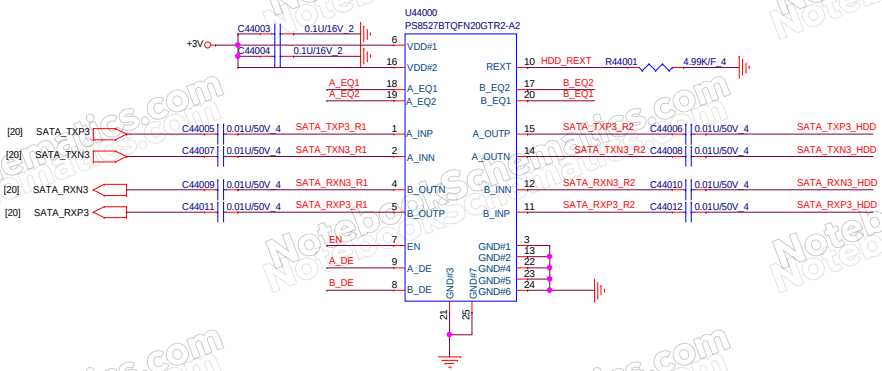
SATA-HDD



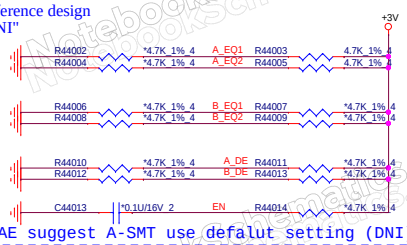




Equalization level setting for Channel x(x=A/B),internally tied to VDD/2 (default:12.2dB)
[x_EQ2, x_EQ1] ==
L/L: for channel loss up to 7.4dB
L/H: for channel loss up to 14.4dB
H/L: for channel loss up to 11.2dB
H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=-3.5dB)
[x_DE] ==
L: 0 dB
H: -6dB

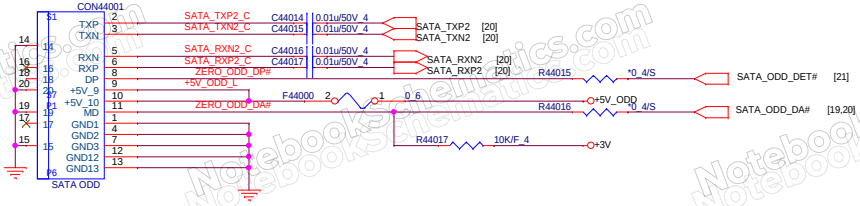
Reference design
"DNI"

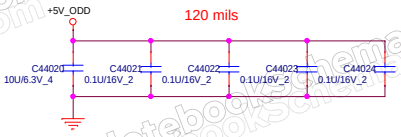


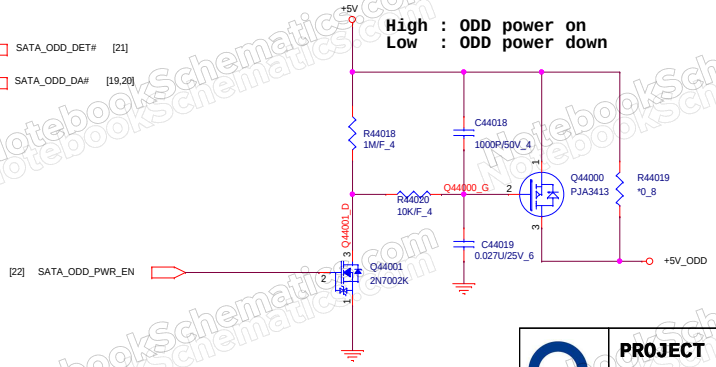
FAE suggest A-SMT use defalut setting (DNI)

SATA ODD CONNECTOR

Bypass CAP close conn







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Quanta Computer Inc.

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EC797 +VHIF
ES Sample: +1.8VPCU
QS Sample: +1.8V_DEP_SUS

	CFLH4	CFLH6
Ra	ADD	NC
Rb	NC	ADD

CHARGE ADD: 0x13/0x12
for Battery charge/charge
for Thermal IC/Accelerometer
for PD1/PD2
for SPK AMP.

PU:Armorhide ; PD:Vortex

NOTE:
Place a 1 uF capacitor as close to the CAP pin as possible.

NOTE:
Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

NPCX797HA1BX
VERSION CLA

NPCE576H_AGND

+SPI_VCC [51,56,78]
+3V [5,12,13,18,19,20,21,22,27,28,29,30,31,34,35,36,41,42,43,44,50,51,52,53,54,55,59,66,67,74,75,76,77,78,79,082,089,092,095]
+3VPCU [13,14,19,23,27,33,34,35,41,42,48,50,52,54,56,59,61,67,77,78,79,080,081,082,083,084,085,086,087,089,091,092,094,095,104]
+3V_DEEP_SUS [5,18,19,20,21,22,23,27,33,41,42,56,57,59,66,78,081,087,092,094,095]
+3V_RTC [19,21,23,42]
+1.8V_DEEP_SUS [13,18,19,20,21,22,23,34,57,78,092,095]

PROJECT : Anchorbay
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NB5
Size C | Document Number Anchorbay | Rev 1A
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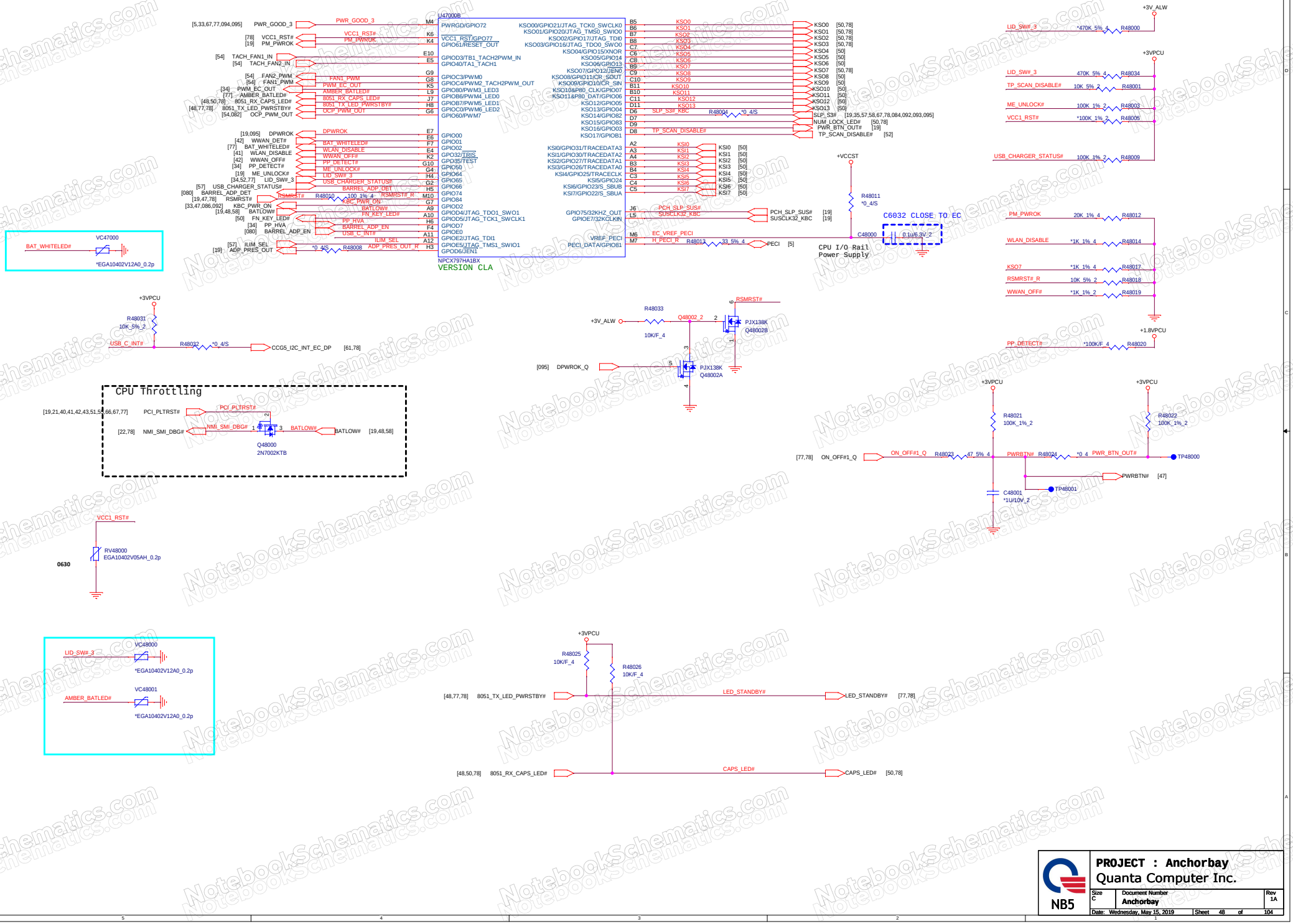

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Quanta Computer Inc.	
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Rev: 1A	
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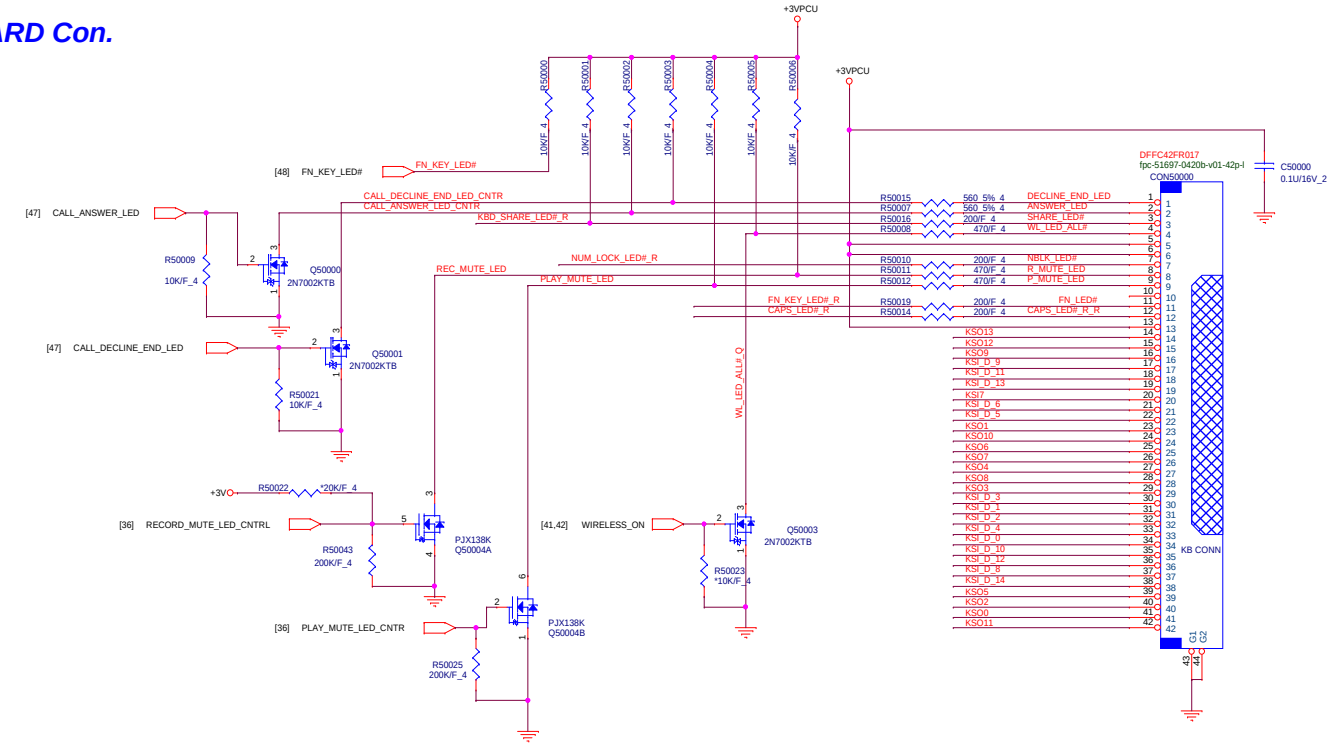
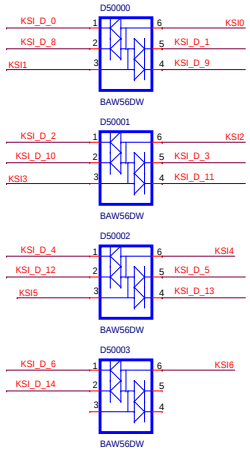
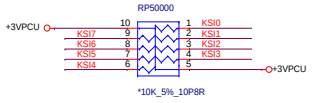
KEYBOARD Con.



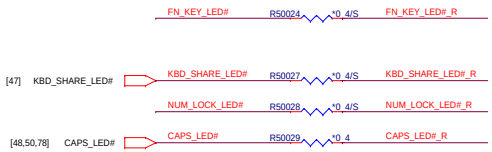


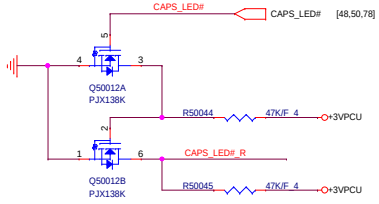
KEYBOARD PULL-UP

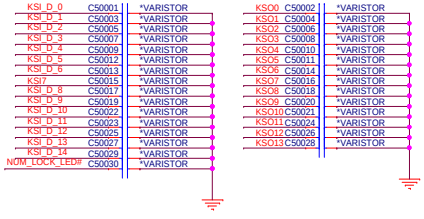


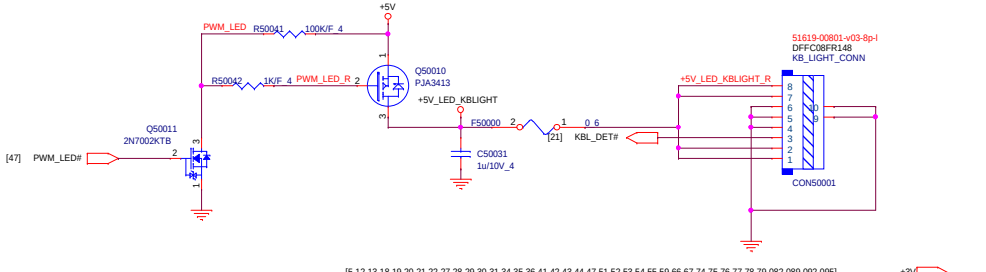
[48,78] KSO[0..13] KSO[0..13]

[48] KSI[0..7] KSI[0..7]









[5,12,13,18,19,20,21,22,27,28,29,30,31,34,35,36,41,42,43,44,47,51,52,53,54,55,59,66,67,74,75,76,77,78,79,082,089,092,095]
[12,13,34,36,44,52,54,55,66,79,092,095]
[13,14,19,23,27,33,34,35,41,42,47,48,52,54,56,59,61,67,77,78,79,080,081,082,083,084,085,086,087,089,091,092,094,095,104]

+3V +5V +3VPCU

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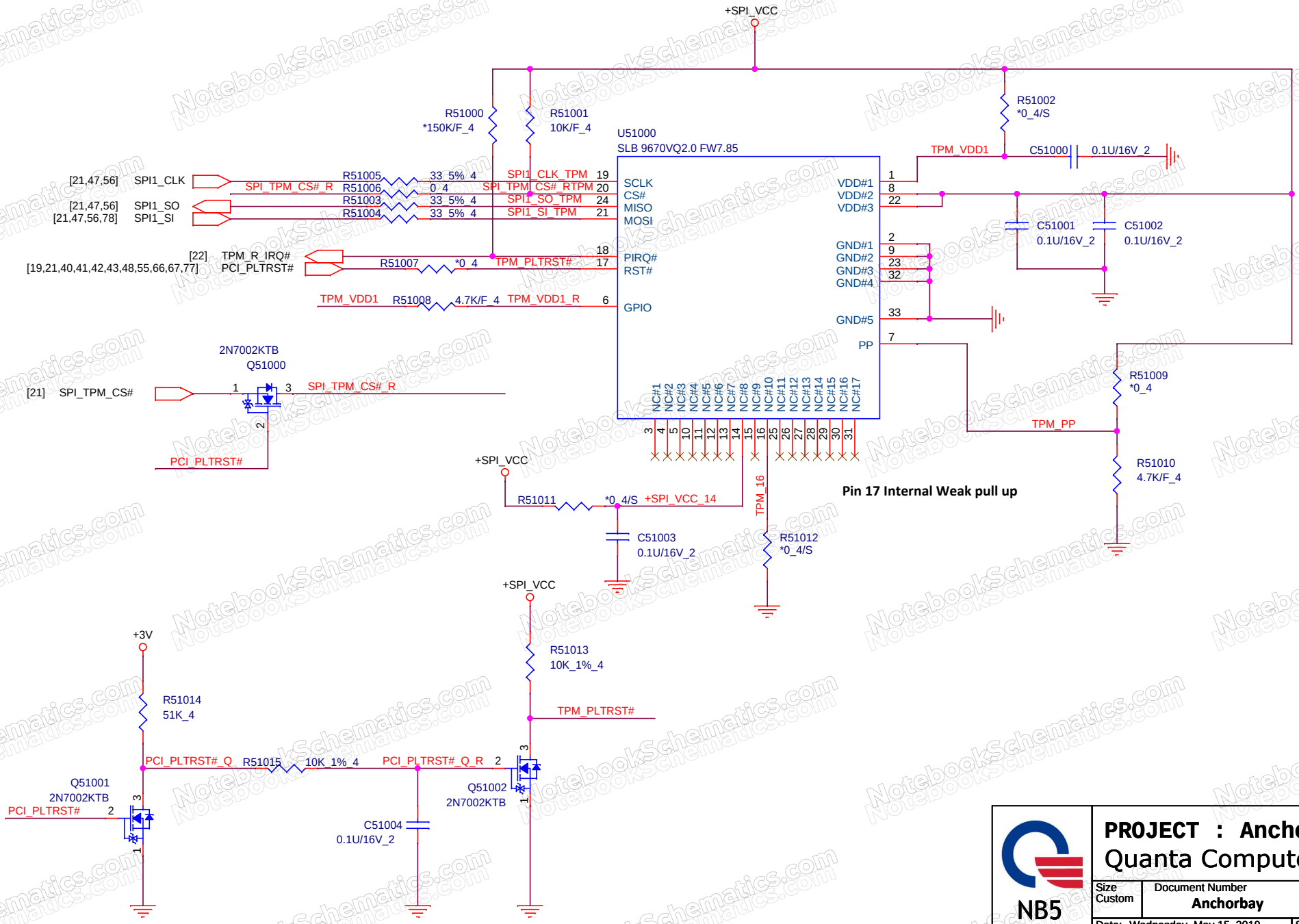
TPM 2.0



PROJECT : Anchorbay

Quanta Computer Inc.

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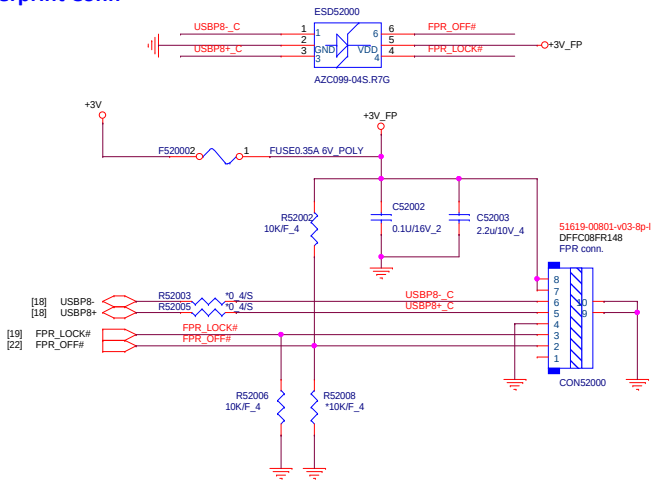
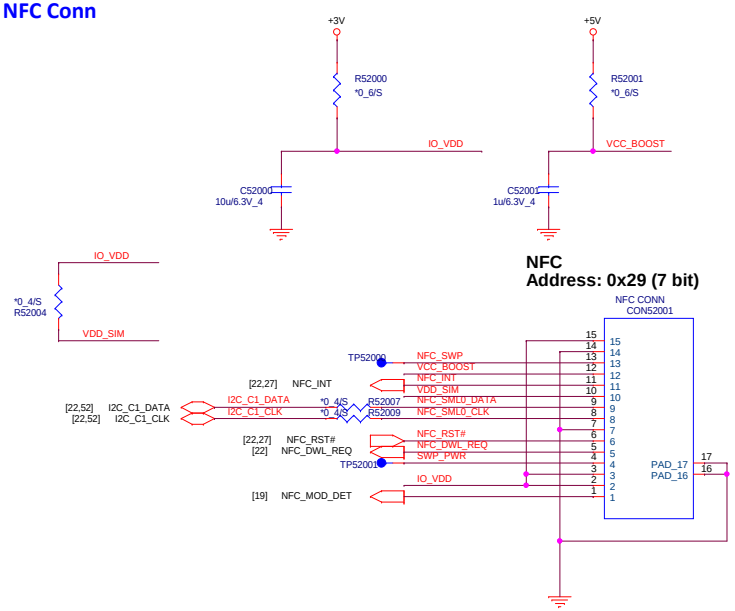
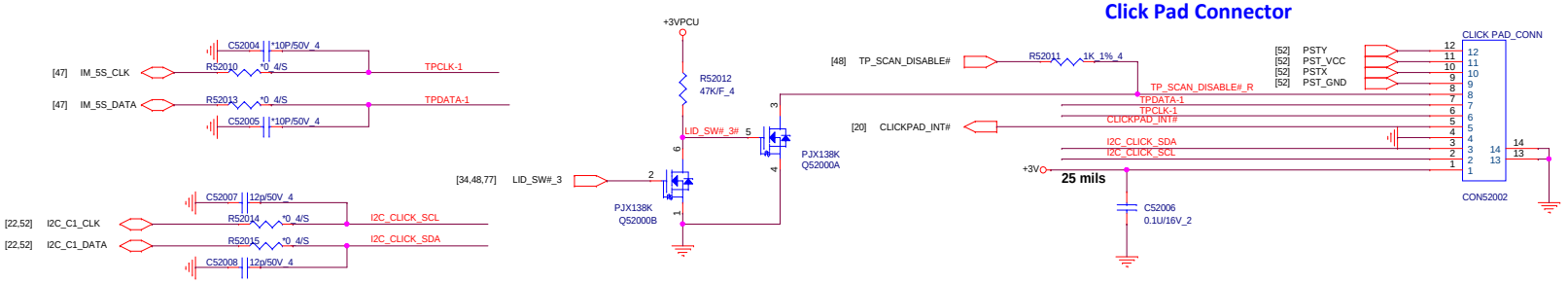
Fingerprint Conn



NFC Conn



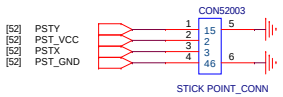
Click Pad Connector

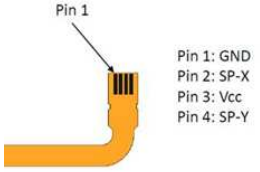


CLICK PAD
Address: 0x2C(7 bit)

PIN NO.	SIGNAL
1	Vdd
2	SCL_I2C
3	SDA_I2C
4	GND
5	Int_I2C
6	CLK_PS2
7	DAT_PS2
8	TP_Disable#
9	PST GND
10	PST X
11	PST Vcc
12	PST Y

STICK POINT_CONN





[5,12,13,18,19,20,21,22,27,28,29,30,31,34,35,36,41,42,43,44,47,50,51,53,54,55,59,66,67,74,75,76,77,78,79,082,089,092,095]
[20,22,34,36,53,092,095]
+3V
+1.8V

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Quanta Computer Inc.

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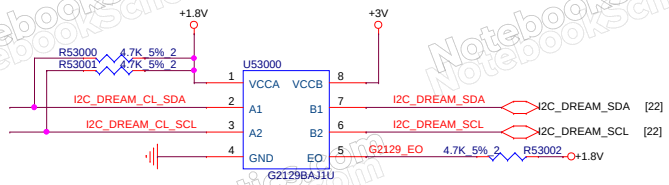
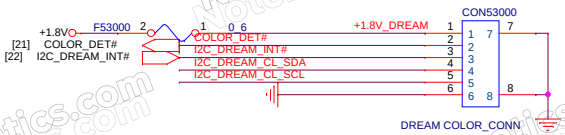
Dream Color Sensor



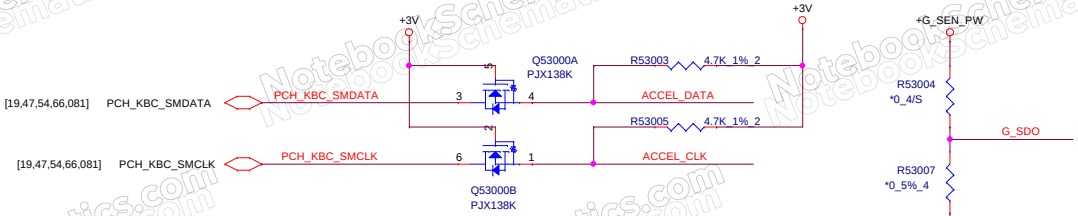
Dream color sensor

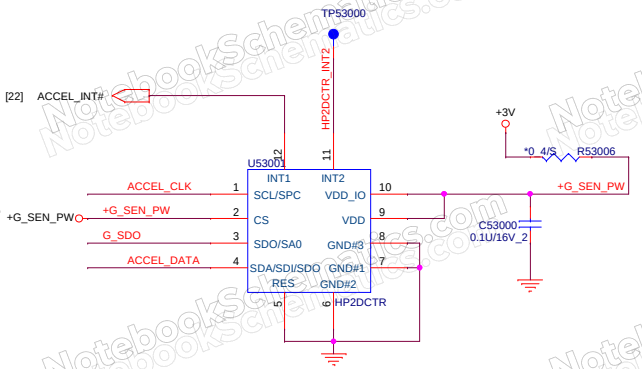
Need to confirm SB!!!



G-Sensor

copy from Bumblebee need check 5/10





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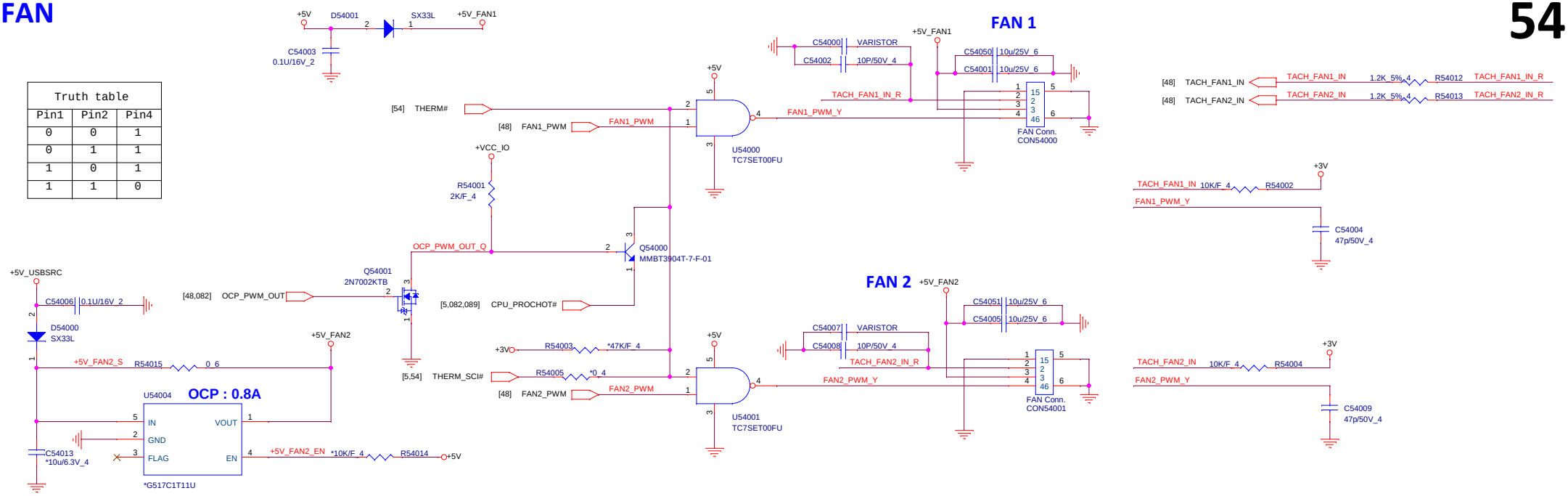
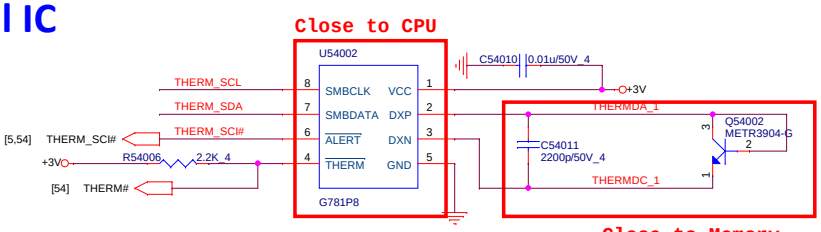
FAN

Truth table		
Pin1	Pin2	Pin4
0	0	1
0	1	1
1	0	1
1	1	0

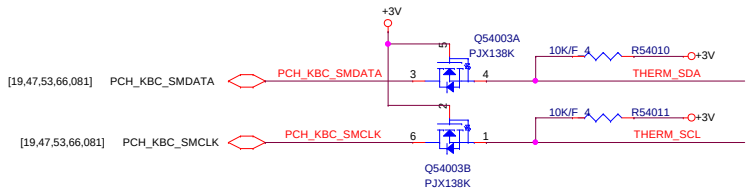


Thermal IC



2nd:AL000431014 TMP431ADGKR

Main: AL000781012 G781P8(98h)



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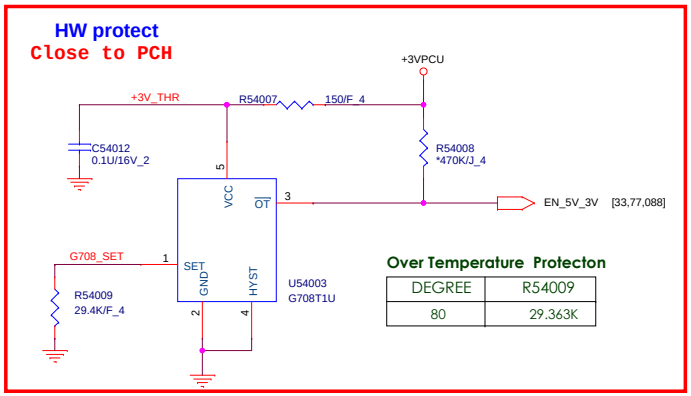
[12,13,34,36,44,50,52,55,66,79,092,095] +5V



Over Temperature Protecton

DEGREE	R54009
80	29.363K

RSET (K OHM) = 0.0012 * T^2 - 0.9308 * T + 96.147

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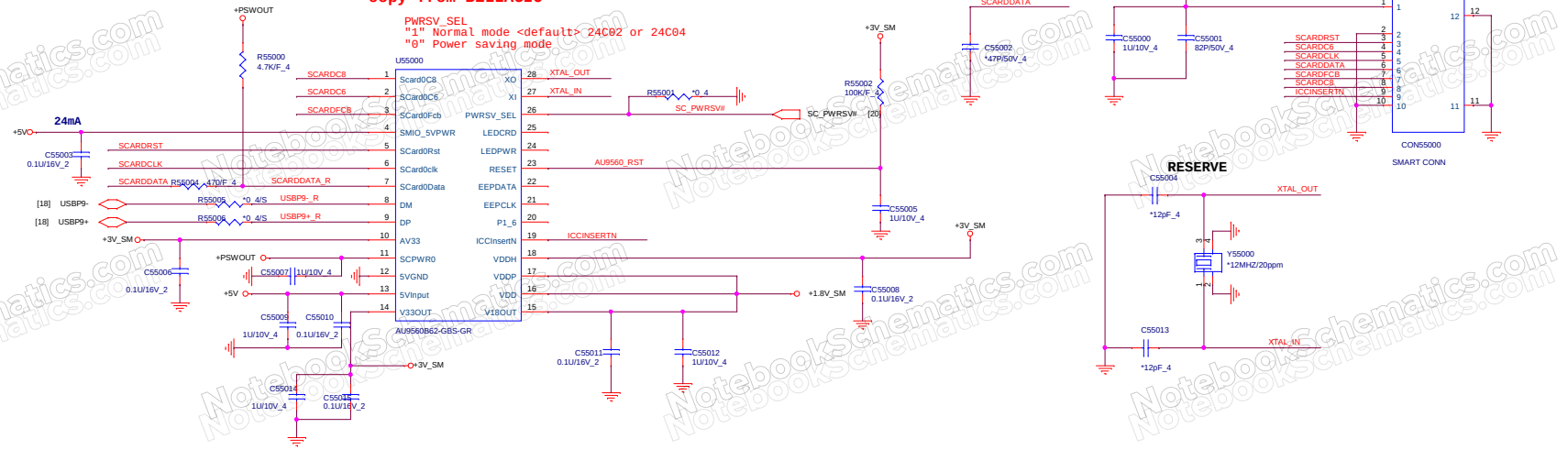
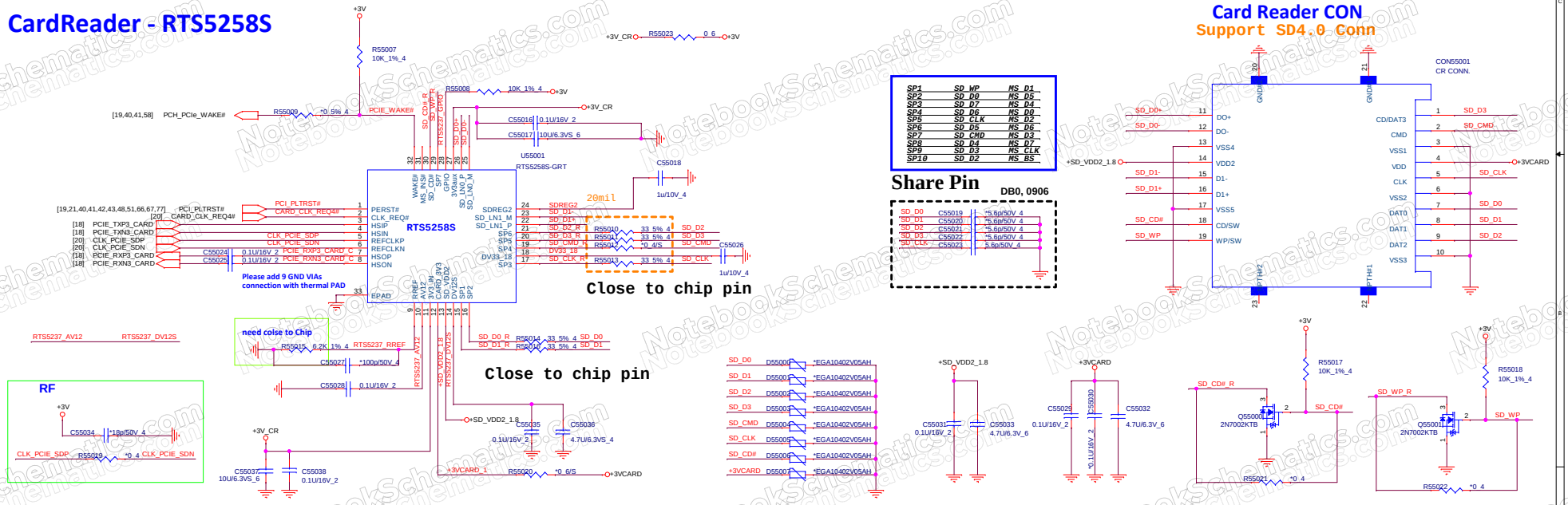
Smart Card

copy from BELLAGIO

PWRSV_SEL
"1" Normal mode <default> 24C02 or 24C04
"0" Power saving mode

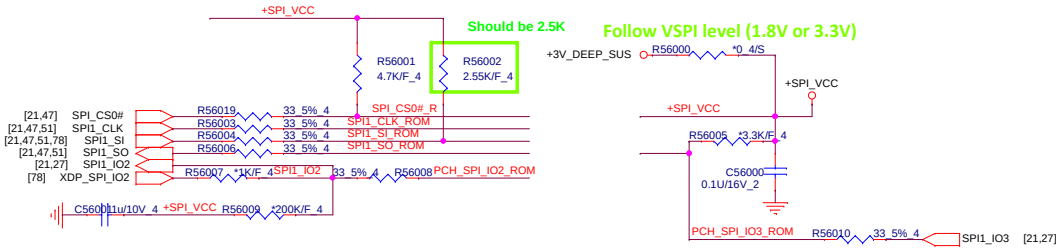


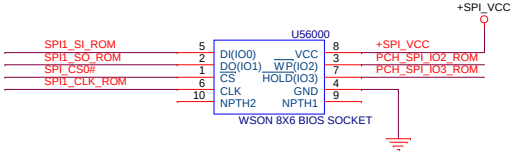
CardReader - RTS5258S



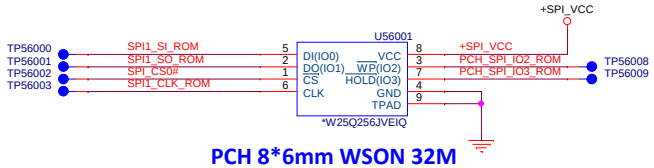
PCH SPI ROM(CLG)

BIOS SPI ROM 32M Byte



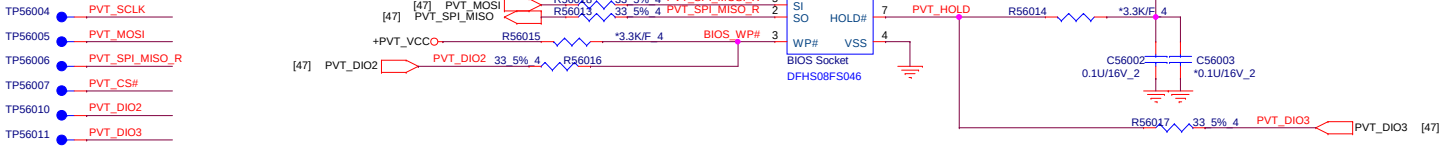


PCH 8*6mm SPI ROM Socket



PCH 8*6mm WSON 32M

SPI ROM 32M 8x6 IC & 8*6 Socket (U56000/U56001)co-lay



SPI ROM Socket

EC 6*5mm WSON 16M

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USB 2.0/3.0 Combo

USB 3.0_LEFT 1

DB0, 0907

2.5A

USB 3.0_LEFT 2

2.5A

USB 3.0_LEFT 3

2.5A

USB 3.0 ESD CHIP

P/N
BCSB3FR4Z00
BC001045Z02
BC000524Z01

USB 2.0 ESD DIODE

P/N
BC5V0X2UZ00
BC005315Z00
BC10063LZ00

ESD chip

ESD chip

ESD chip

USB Charger

IC continuous output current is 2.5A

$$I_{OS\_typ}(mA) = \frac{50,250}{R_{ILIM\_xx}(k\Omega)}$$

ILIM_HI = 22k, typical over current protection will be at 2.284A
ILIM_LO = 39k, typical over current protection will be at 1.28A

100 mils (Iout=2.5A)

high active

high active

high active

$I_{OS} = 48000/RILIM0$

USB3.1 Re-driver IC

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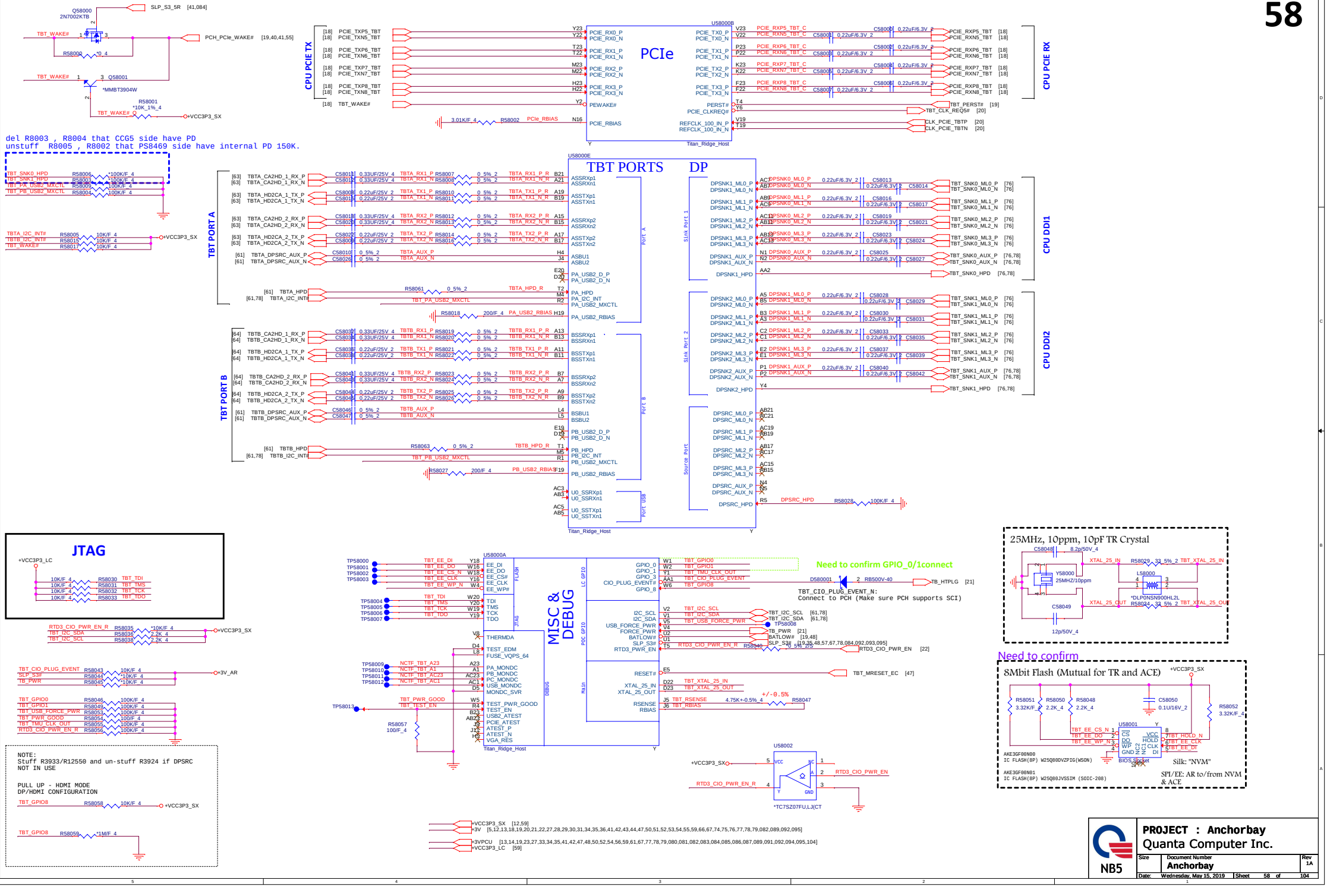
CPU PCIE TX
PCIe
Titan_Ridge_Host
CPU PCIE RX
del R8003 , R8004 that CCG5 side have PD
unstuff R8005 , R8002 that PS8469 side have internal PD 150K.
TBT PORT A
TBT PORT B
TBT PORTS
DP
CPU DDI1
CPU DDI2
JTAG
MISC & DEBUG
Need to confirm GPIO_0/1connect
TBT_CIO_PLUG_EVENT_N:
Connect to PCH (Make sure PCH supports SCI)
25MHz, 10ppm, 10pF TR Crystal
Need to confirm
8Mbit Flash (Mutual for TR and ACE)
Silk: "NVM"
SPI/EE: AR to/from NVM & ACE
NOTE:
Stuff R3933/R12550 and un-stuff R3924 if DPSRC NOT IN USE
PULL UP - HDMI MODE
DP/HDMI CONFIGURATION
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Quanta Computer Inc.
NB5
Anchorbay
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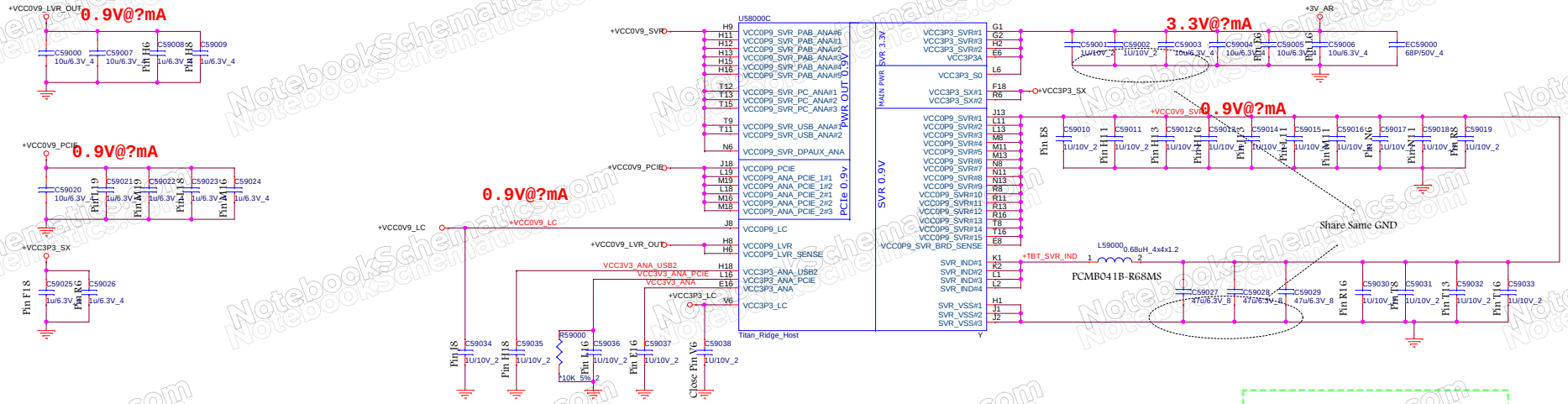
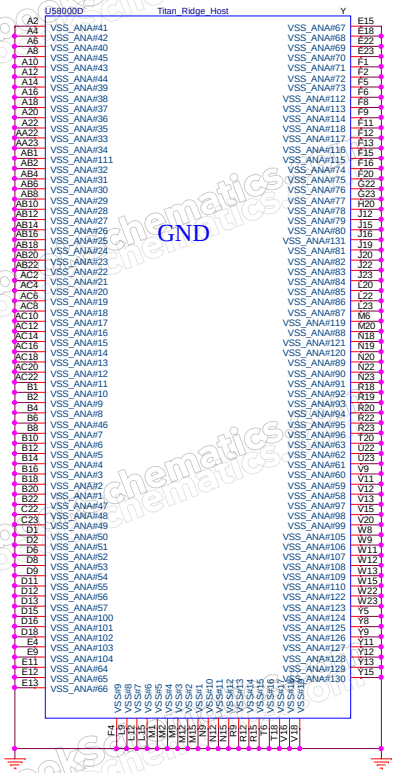
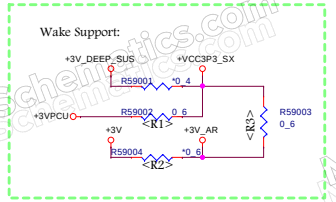


Titan Ridge DP - GND Symbol





Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

+VCC3P3_SX [12,58]
+VCC3P3_LC [58]
+3V [5,12,13,18,19,20,21,22,27,28,29,30,31,34,35,36,41,42,43,44,47,50,51,52,53,54,55,66,67,74,75,76,77,78,79,082,089,092,095]
+3V_DEEP_SUS [5,18,19,20,21,22,23,27,33,41,42,56,57,66,78,081,087,092,094,095]

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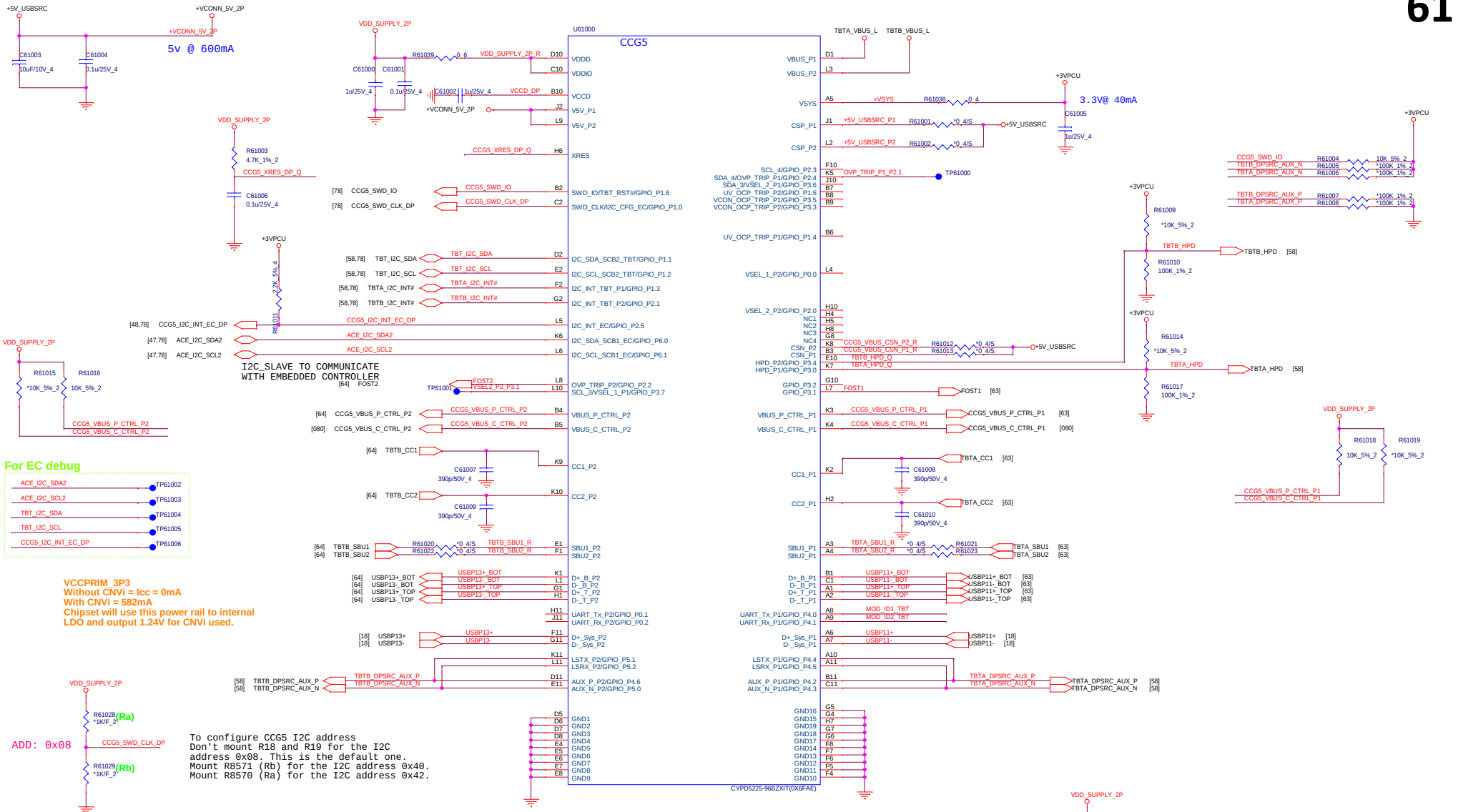

MOD_ID SETTING

	Platform ID		CCG5 Dual Port	
	MOD_ID1	MOD_ID2	Description (Dual port)	
Notebooks	L7	L7	DRP+DP+ AR TBT on 2-ports	L0 = 0V
	L6	L7	DRP+DP on 2-ports	L1 = VDDD/8
	L5	L7	DRP+DP on 2-ports with ANX MUX	L2 = 2* VDDD/8
	L4	L7	Malta	L3 = 3* VDDD/8
	L3	L7	DRP+DP+ TR TBT on 2-ports	L4 = 4* VDDD/8
	L2	L7	Reserved	L5 = 5* VDDD/8
	L1	L7	Reserved	L6 = 6* VDDD/8
	L0	L7	Reserved	L7 = 7* VDDD/8
				x = No Connect

MOD_ID	Pull high	Pull down
L0	None	10K
L1	71.5K	10K
L2	60.4K	22K
L3	200K	120K
L4	10K	10K
L5	30K	49.9K
L6	22K	60.4K
L7	56K	392K

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Quanta Computer Inc.

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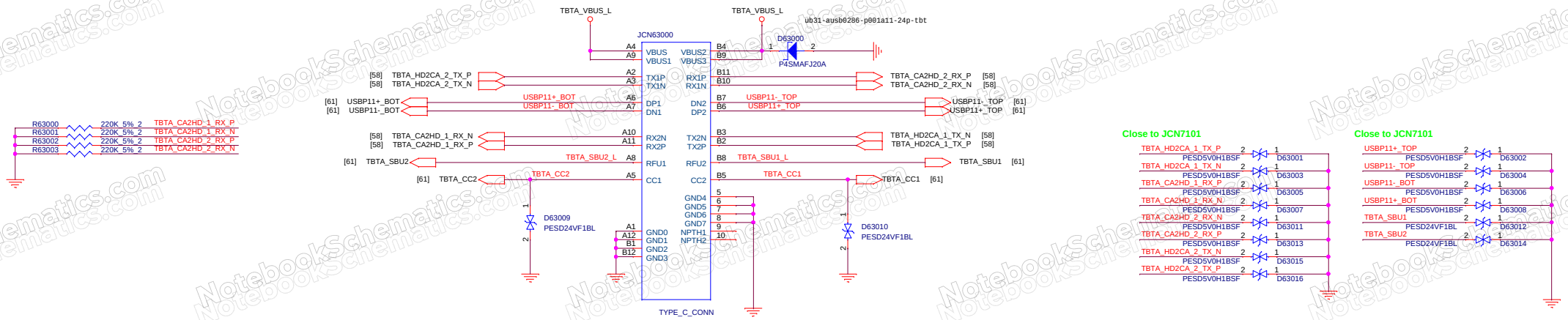

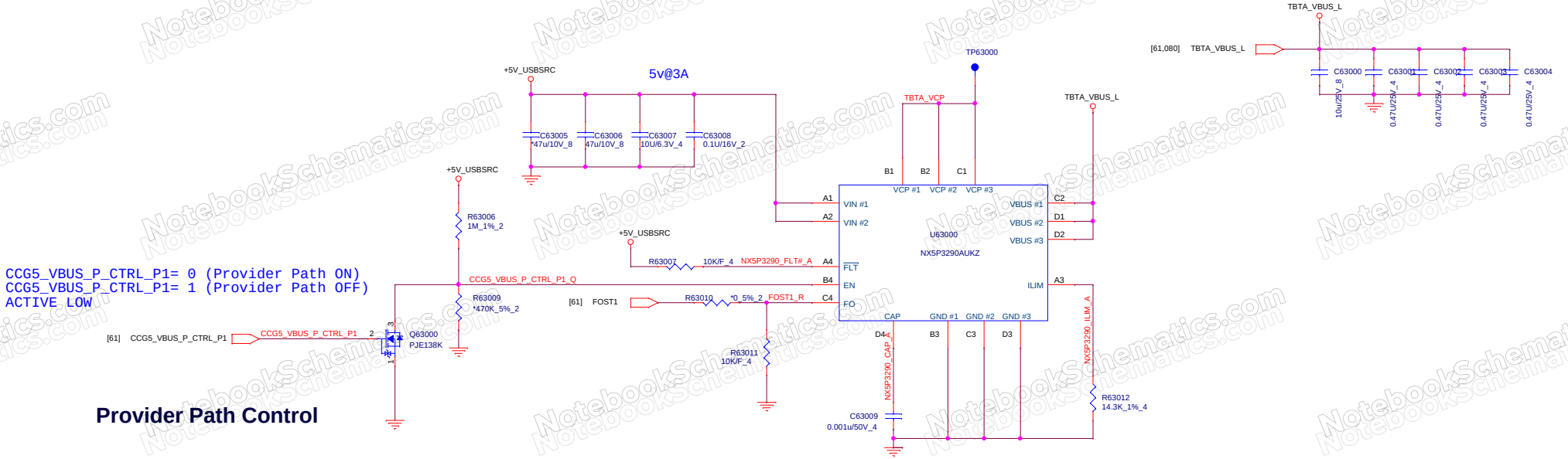

CCG5_VBUS_P_CTRL_P1= 0 (Provider Path ON)
CCG5_VBUS_P_CTRL_P1= 1 (Provider Path OFF)
ACTIVE LOW

Provider Path Control

NB5

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Quanta Computer Inc.

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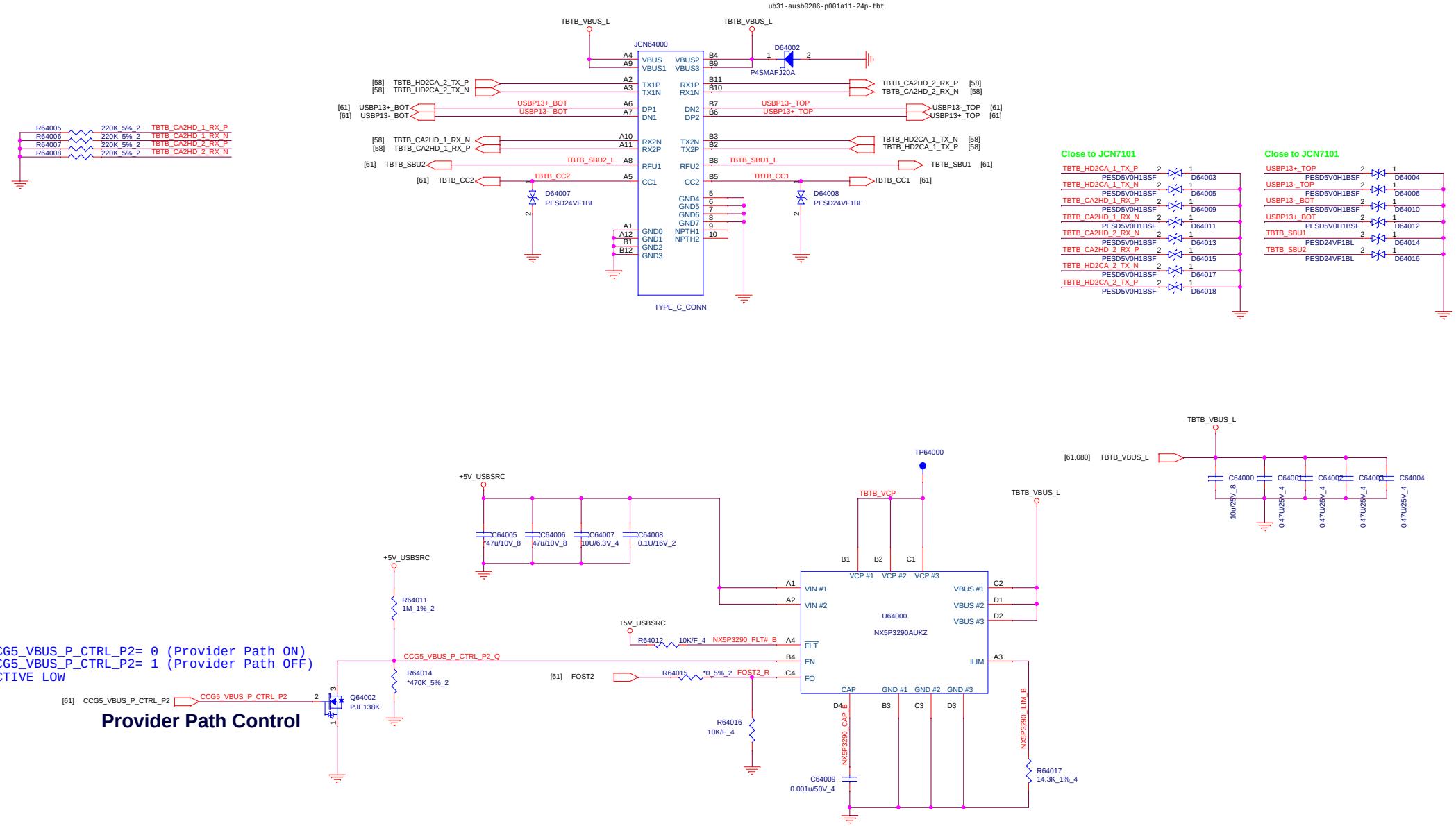

PROJECT : Anchorbay
Quanta Computer Inc.

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NB5

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MXM 3.0 <OEV,PX>

PEX_STD_SWr(MXM IPU)
H: High Swing
L: Low Swing

VGA_DISABLE# (MXM IPU)
Used For Multi-GPU

GPIO	N16-EQS	IO Type
OEM 4	GPU_EVENT#	IN
OEM 5	GC6_FB_EN	OUT
OEM 6	GPIO18_STEREO	OUT
OEM 7	RESERVE	RESERVE
GPIO 9	GPIO26	Tri-State
GPIO 1	NC	NC
GPIO 2	GPIO25	Tri-state

GPU VIN power (10A)

GPU +5V power (2.5A)

RF

MXM 3.0 MODULE BOARD CONNECTOR

CON66000A

within 500mils

Configuration Signals:		
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express (default 11, internal PU)
OEM0		0 = NV DGPU 1 = AMD DGPU
OEM3		VRM OOC setting (TBD)

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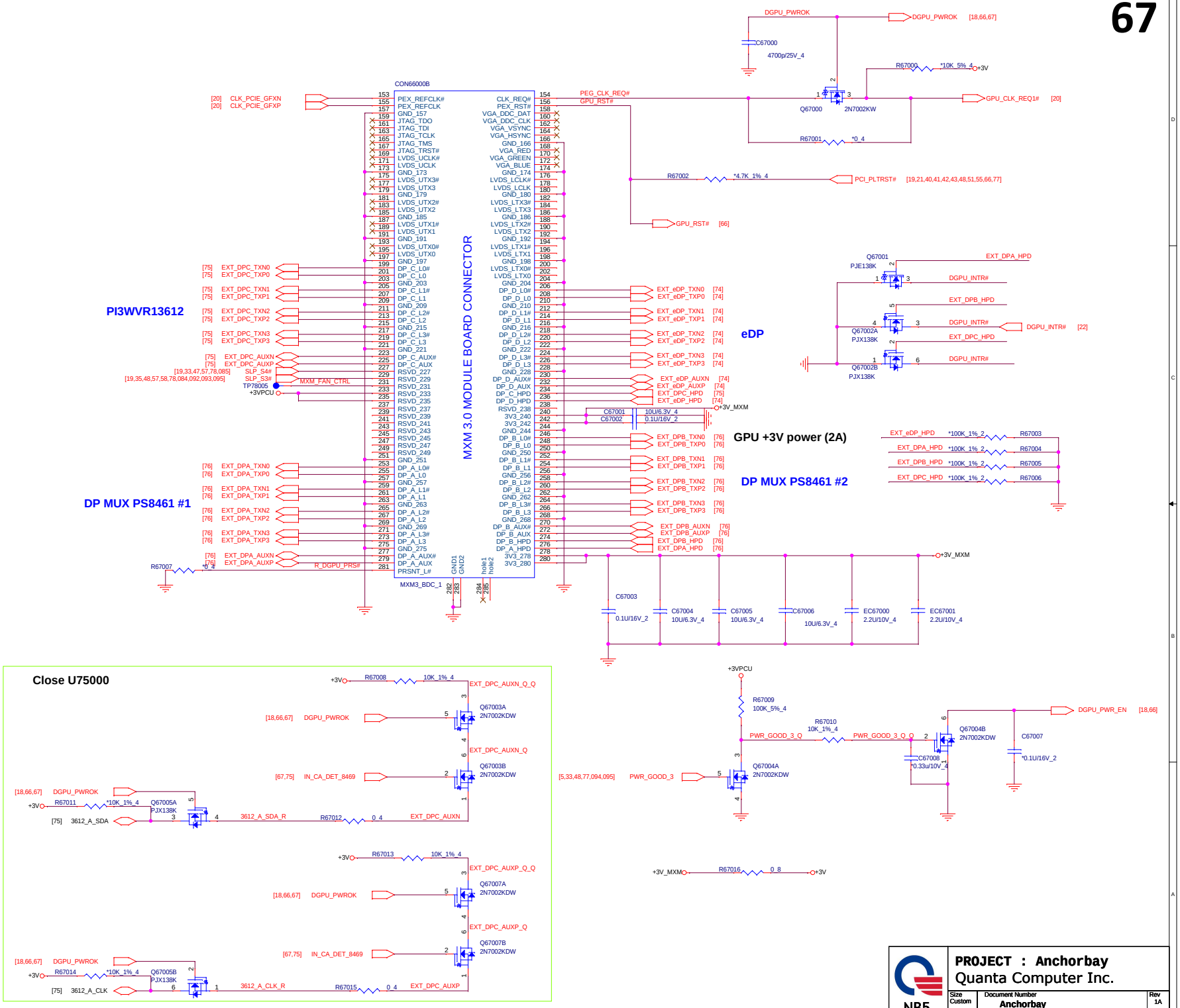

NB5

PROJECT : Anchorbay
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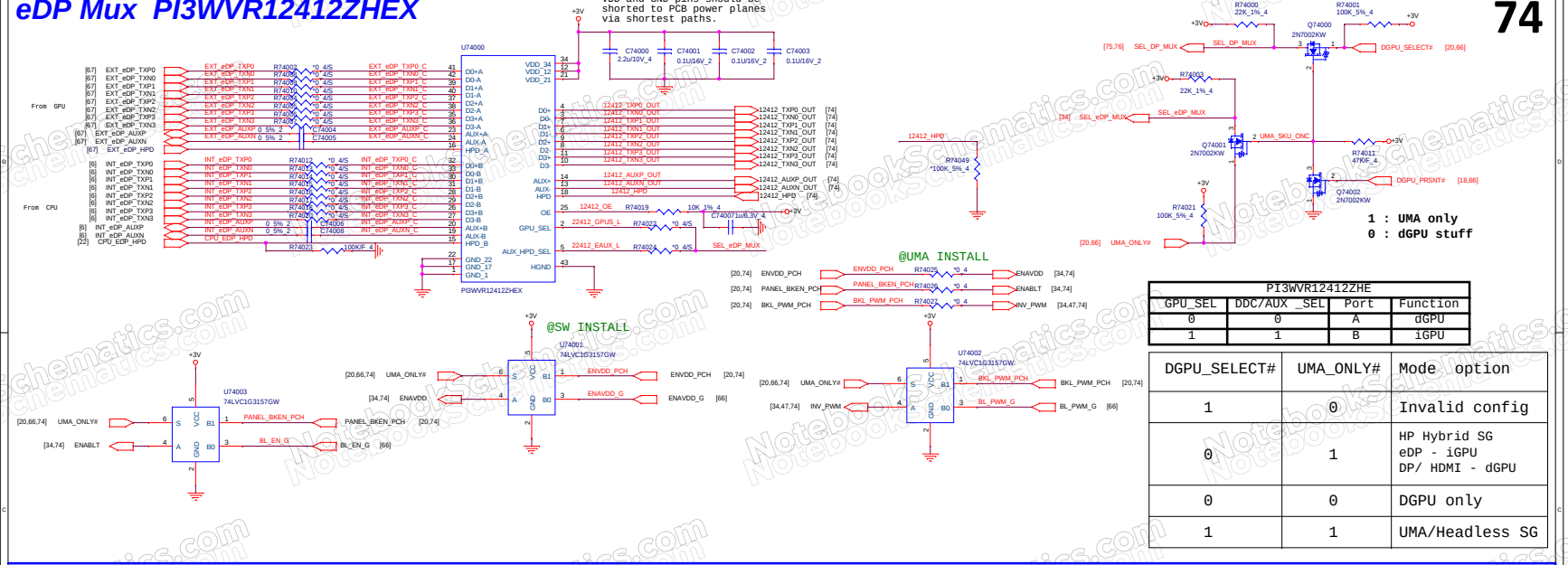
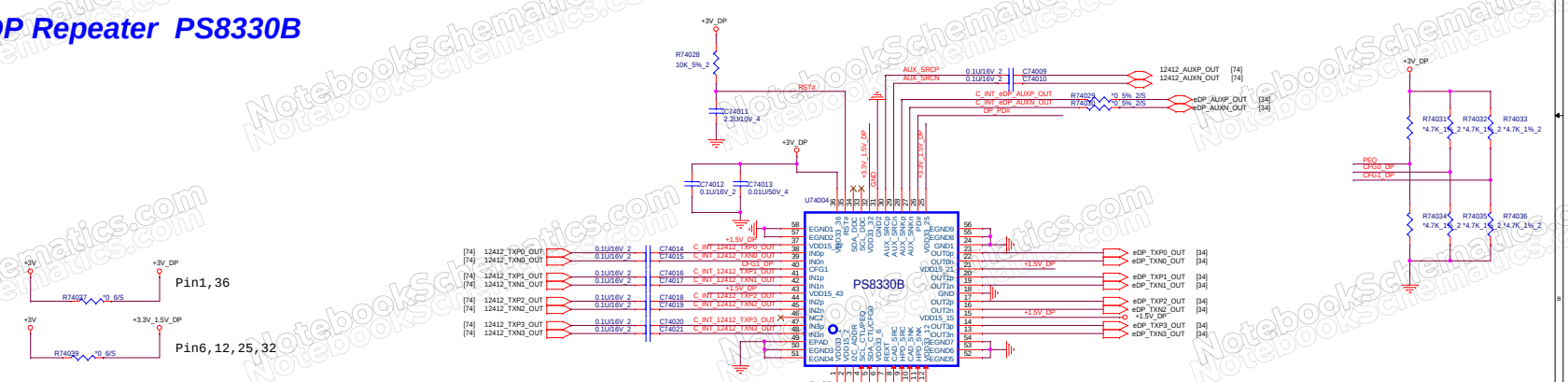
eDP Mux PI3WVR12412ZHEX



PI3WVR12412ZHE			
GPU_SEL	DDC/AUX _SEL	Port	Function
0	0	A	dGPU
1	1	B	iGPU

DGPU_SELECT#	UMA_ONLY#	Mode option
1	0	Invalid config
0	1	HP Hybrid SG eDP - iGPU DP/ HDMI - dGPU
0	0	DGPU only
1	1	UMA/Headless SG

eDP Repeater PS8330B



3 Level Input:
L: LOW
H: HIGH
M: VDD33/2, connect both pull-up and pull-down resistors

CFG0_DP

Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

CFG1_DP

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

PEQ

Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

NB5

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<Title>
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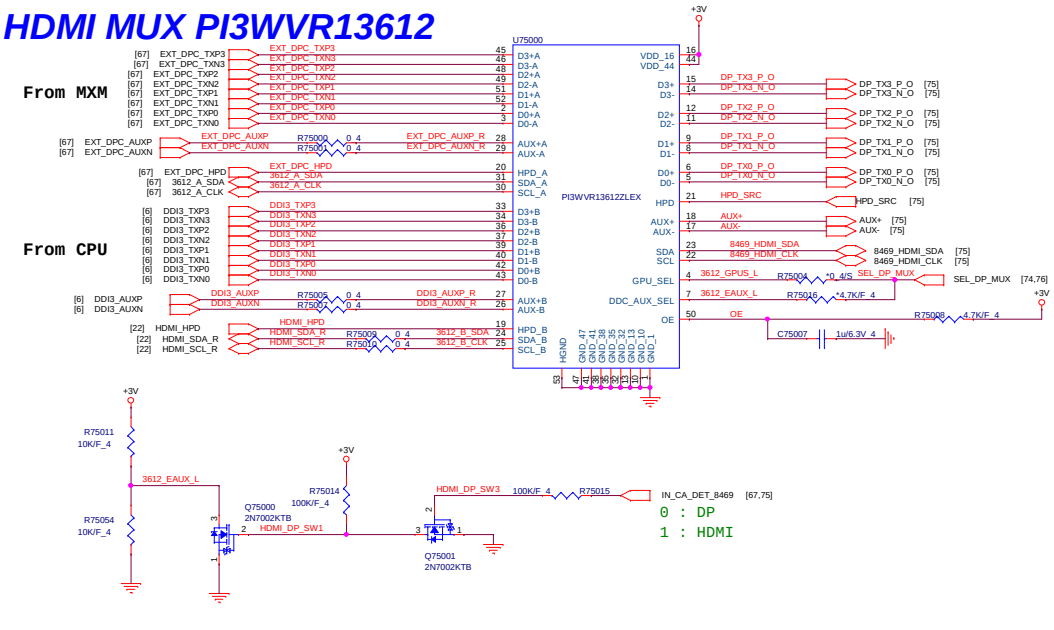
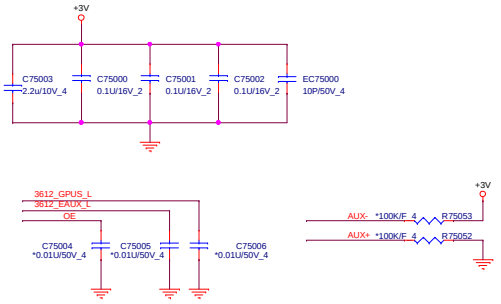
HDMI MUX PI3WVR13612

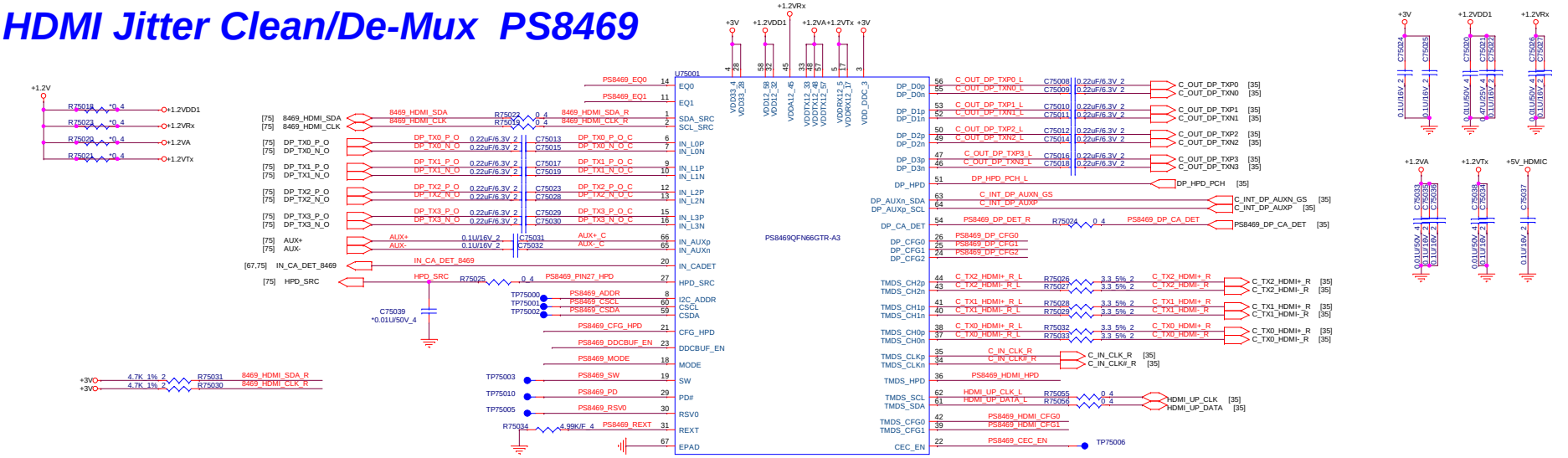




DDC/AUX _SEL : M -> 1/2 VDD

PI3WVR13612ZLE			
GPU_SEL	DDC/AUX _SEL	Port	Function
0	0	A	dGPU-DP
1	0	B	iGPU-DP
0	M	A	dGPU-HDMI
1	M	B	iGPU-HDMI

HDMI Jitter Clean/De-Mux PS8469



Mode = (Internal PD ~150K, 3.3V)
L: Control Switching Mode, HDMI ID enabled(default)
M: Automatic Switching Mode, HDMI ID disabled
H: AUtomatic Switching Mode, HDMI ID enabled

Control Switching Mode:
SW= (Internal PD ~150K, 3.3V)
L: DP Port is selected (default)
H: TMDS Port is selected
Automatic Switching Mode:
SW= (Internal PD ~150K, 3.3V)
L: DP Port has higher priority when both ports are plugged in (default)
H: TMDS Port has higher priority when both ports are plugged in

[EQ1,EQ0] =
LL:Compensate channel loss up to 11 dB @ HBR3
LM:Compensate channel loss up to 13 dB @ HBR3
LH:Compensate channel loss up to 15 dB @ HBR3
ML:Compensate channel loss up to 16 dB @ HBR3
MM:Compensate channel loss up to 17 dB @ HBR3
MH:Compensate channel loss up to 18 dB @ HBR3
HL:Compensate channel loss up to 19 dB @ HBR3
HM:Compensate channel loss up to 20 dB @ HBR3
HH:Compensate channel loss up to 21 dB @ HBR3

TMDS_CFG0 =
L: Default TMDS output swing (default)
M: Decrease TMDS swing by 10%
H: Increase TMDS swing by 10%

TMDS_CFG1 =
L: No pre-emphasis (default)
M: 1.5dB pre-emphasis
H: 3dB pre-emphasis

CFG_HPD:
L: Default HPD delay (default)
M: Minimum HPD delay
H: Maximum HPD delay

DP_CFG0 =
L:DP Port is configured to Auto jitter cleaning mode (default)
M:DP Port is configured to Redriving mode
H:DP Port is configured to Full jitter cleaning mode

DP_CFG1 =
L:Auto EQ enabled (default)
EQ automatically adjusted based on link training.
H:Auto EQ disabled.

DP_CFG2:
L: DP output is dynamic adjusted based on link training (default)
M: DP output is fixed to 400mV/0dB
H: DP output is fixed to 800mV/0dB

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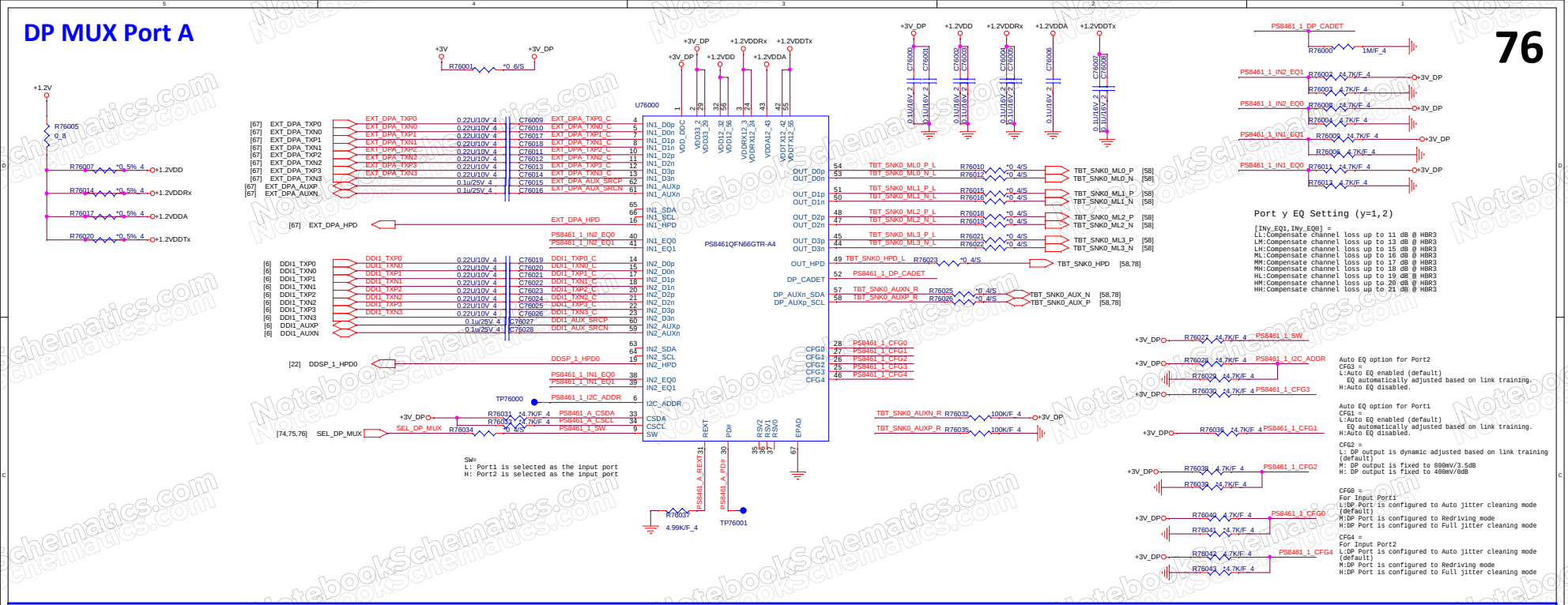
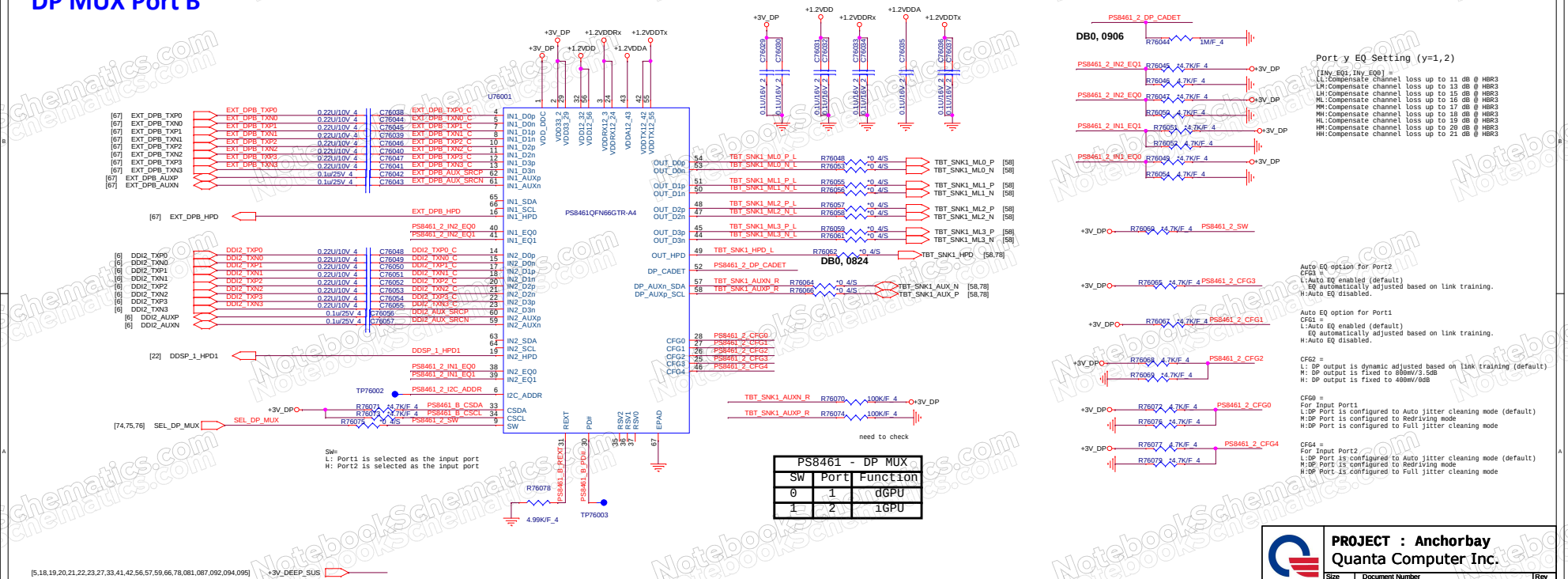
DP MUX Port A



DP MUX Port B



PS8461 - DP MUX		
SW	Port	Function
0	1	dGPU
1	2	iGPU

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NB5	Size	Document Number Anchorbay	Rev 1A
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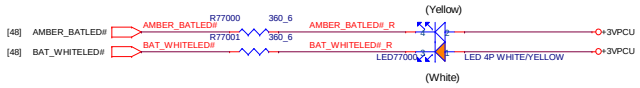
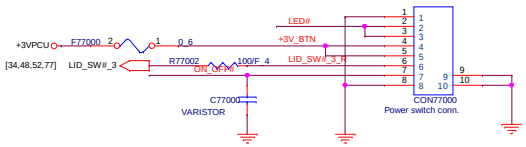
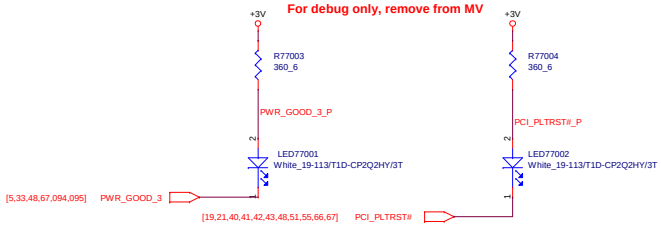
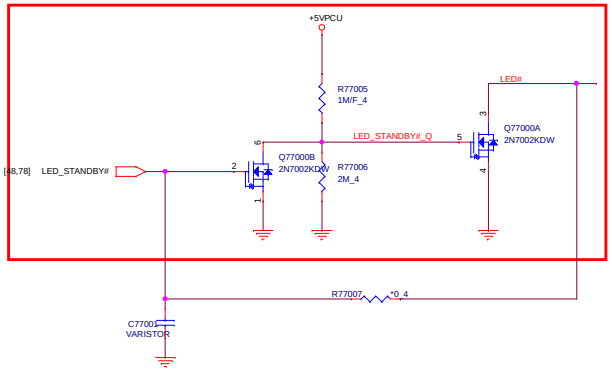
Battery LED

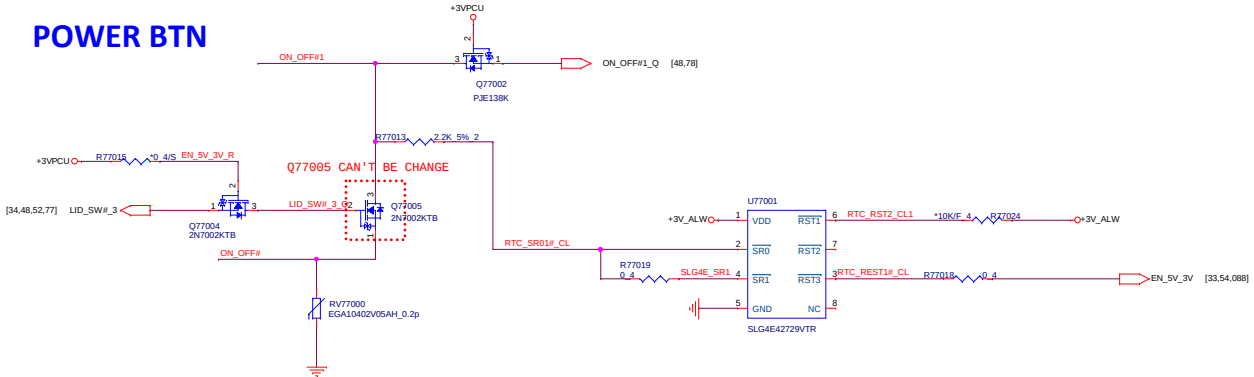


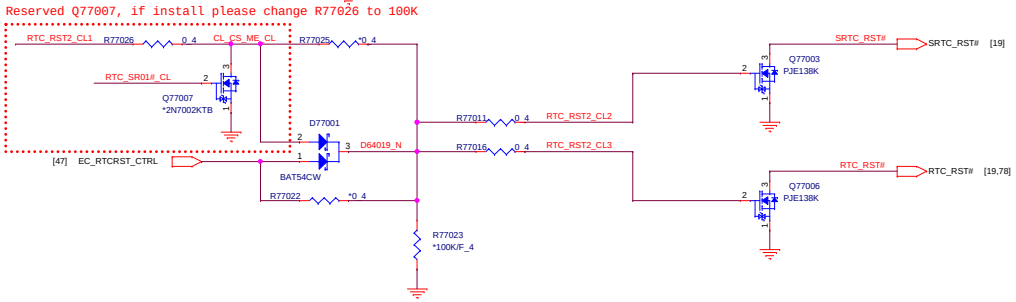






POWER BTN





NB5	PROJECT : Anchorbay Quanta Computer Inc.	
Size: Custom	Document Number: Anchorbay	Rev: 1A
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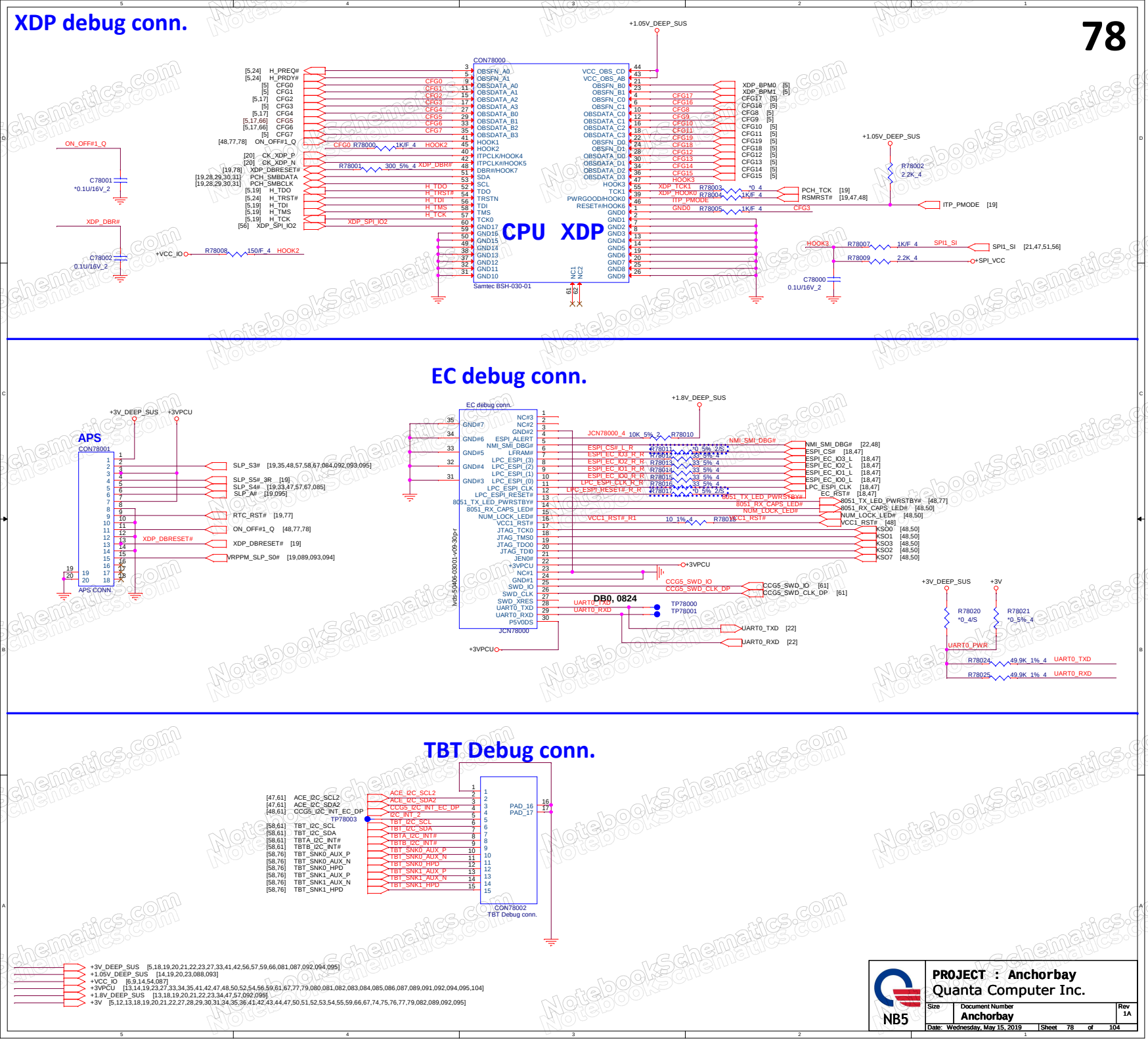
XDP debug conn.
78
CPU XDP
CON78000
Samtec BSH-030-01
EC debug conn.
APS
CON78001
APS CONN.
JCN78000
TBT Debug conn.
CON78002
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Quanta Computer Inc.
NB5
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Screw Hole

H79000 *H-C236I110D110P2
H79001 *H-C276I110D110P2
H79002 *H-TC256BC236I118D118P2
H79003 *H-C276I110D110P2
H79004 *H-TC354BC256I146D146P2
H79005 *H-TC354BC256I146D146P2
H79006 *H-TC354BC256I146D146P2
H79007 *H-TC354BC256I146D146P2
H79008 *H-TBC236I150D110P2
H79009 *H-TC256BC236I118D118P2

H79010 *H-TC256BC236I118D118P2
H79011 *h-tc276ibc236i110d110p2
H79012 *H-C236I110D110P2
H79013 *H-TC256BC236I110D110P2
H79014 *H-C236I110D110P2
H79015 *H-TC256BC236I110D110P2
H79016 *H-TC256BC236I118D118P2
H79017 *H-TC256BC236I110D110P2
H79018 *H-TC256BC236I110D110P2
H79019 *O-MWS-A-1
H79020 *h-xw3a-1
H79021 *h-c79d79n
H79022 *O-XW3A-1

H79023 FAN NUT **FAN NUT**

PAD79000 *spad-re264x59
PAD79001 *spad-re264x59
PAD79002 *spad-re315x59
PAD79003 *spad-re394x59
PAD79004 *spad-s177
PAD79005 *spad-re323x59
PAD79006 *spad-re323x59
PAD79007 *spad-re323x59
PAD79008 *spad-re315x59
*o-xw3a-2
H79029
AGND

Shielding
H79030 *pad-mws-a-1nmp
H79031 *pad-mws-a-1nmp
H79032 *pad-mws-a-4nmp

H79024 SSD NUT **SSD NUT**
Stuff on Top

USB C
H79025 USB C
Stuff on Top

H79026 WWAN NUT **WWAN NUT**

MXM NUT
H79027 MXM NUT
H79028 MXM NUT

H79033 *H-TC157IC79D79PT
H79034 *H-C79D79N
H79035 *H-C79D79N

PAD79009 *spad-s294np
PAD79009_1
C79000 *MLVS0402M04
R79000 *100K/F_4

PAD79010 *SPAD-MWS-A-1
PAD79011 *SPAD-RE79X315NP
PAD79012 *SPAD-MWS-A-2
PAD79013 *SPAD-MWS-A-3
PAD79014 *SPAD-RE630X79NP
PAD79015 *SPAD-C197NP
PAD79016 *SPAD-C197NP
PAD79017 *SPAD-C197NP
PAD79018 *SPAD-MWS-A-4
PAD79019 *SPAD-C197NP
PAD79020 *SPAD-MWS-A-XW3_1
PAD79021 *SPAD-MWS-A-XW3_2
PAD79024 *SPAD-C222NP

Memory Shielding Can Clip
CAS79000 CAS79001 CAS79002 CAS79003 CAS79004 CAS79005
CAS79006 CAS79007 CAS79008 CAS79009 CAS79010 CAS79011
CAS79012 CAS79013 CAS79014 CAS79015 CAS79016
Memory Clip

2D-BARCODE
PAD79022 *2D-BARCODE-8X8-S
PAD79023 *2D-BARCODE-8X8-S

LVDS NUT
H79036 LVDS NUT
H79037 LVDS NUT

+VIN_BLIGHT
EC79081 2.2U/25V_4
+3VPCU
EC79082 0.1u/25V_4
+VIN
EC79084 10P/50V_4
EC79085 2.2U/25V_4
EC79083 0.1u/25V_4
EC79088 2.2U/25V_4
EC79089 68P/50V_4
EC79090 2.2U/25V_4
EC79091 68P/50V_4
EC79092 2.2U/25V_4
EC79093 0.1u/25V_4

+VIN_CPU_GPU
EC79094 0.1u/25V_4
EC79095 2.2U/25V_4
EC79096 68P/50V_4
+VIN_BLIGHT_S
EC79097 0.1u/25V_4
EC79098 0.1u/25V_4

+VIN
EC79000 0.1u/25V_4
EC79001 0.1u/25V_4
EC79002 0.1u/25V_4
EC79003 0.1u/25V_4
EC79004 0.1u/25V_4
EC79005 0.1u/25V_4
EC79006 0.1u/25V_4
EC79007 0.1u/25V_4
EC79008 0.1u/25V_4
EC79009 0.1u/25V_4
EC79010 10P/50V_4
EC79011 10P/50V_4

+5VPCU
EC79012 0.1u/25V_4
EC79013 0.1u/25V_4
EC79014 0.1u/25V_4
EC79015 0.1u/25V_4
EC79016 0.1u/25V_4
EC79017 0.1u/25V_4
EC79018 0.1u/25V_4
EC79019 0.1u/25V_4
EC79020 0.1u/25V_4
EC79021 0.1u/25V_4

+1.2VSUS
EC79022 0.1u/25V_4
EC79023 0.1u/25V_4
EC79024 0.1u/25V_4
EC79025 0.1u/25V_4

+5V
EC79026 0.1u/25V_4
EC79027 0.1u/25V_4
EC79028 0.1u/25V_4
EC79029 0.1u/25V_4
EC79030 0.1u/25V_4

+3V
EC79031 0.1u/25V_4
EC79032 0.1u/25V_4
EC79033 0.1u/25V_4
EC79034 0.1u/25V_4
EC79035 0.1u/25V_4
EC79036 0.1u/25V_4
EC79086 0.1u/25V_4
EC79087 0.1u/25V_4

+3VPCU
EC79037 0.1u/25V_4
EC79038 0.1u/25V_4
EC79039 0.1u/25V_4
EC79040 2.2U/10V_4

+VIN
EC79041 10P/50V_4
EC79042 10P/50V_4
EC79043 2200p/50V_4
EC79044 10P/50V_4
EC79045 2200p/50V_4
EC79046 10P/50V_4
EC79047 2200p/50V_4

+VIN
EC79048 10P/50V_4
EC79049 2200p/50V_4
EC79050 0.1u/25V_4
EC79051 2.2U/25V_4

+VIN
EC79052 10P/50V_4
EC79053 2.2U/25V_4
EC79054 0.1u/25V_4

+VIN
EC79055 10P/50V_4
EC79056 2200p/50V_4
EC79057 0.1u/25V_4

+1.2VSUS
EC79058 10P/50V_4
EC79059 2200p/50V_4

+1.2VSUS
EC79060 10P/50V_4
EC79061 2200p/50V_4

+5V_AMP
EC79079 0.1u/25V_4

+VIN
EC79080 2.2U/25V_4

+1.2VSUS
EC79062 10P/50V_4
EC79063 2200p/50V_4

+1.2VSUS
EC79064 10P/50V_4
EC79065 2200p/50V_4

+1.2VSUS
EC79066 10P/50V_4
EC79067 2200p/50V_4

+5V_USBSRC
EC79068 2.2U/10V_4

+1.2VDD
EC79069 10P/50V_4

+3V
EC79070 10P/50V_4

+5V_MXM
EC79071 2.2U/10V_4

+VIN
EC79072 2.2U/25V_4

+VIN
EC79073 10P/50V_4
EC79075 2.2U/25V_4
EC79074 0.1u/25V_4

+VIN
EC79076 10P/50V_4
EC79077 2.2U/25V_4

PVADPTR
EC79078 0.1u/25V_4

NB5

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Quanta Computer Inc.

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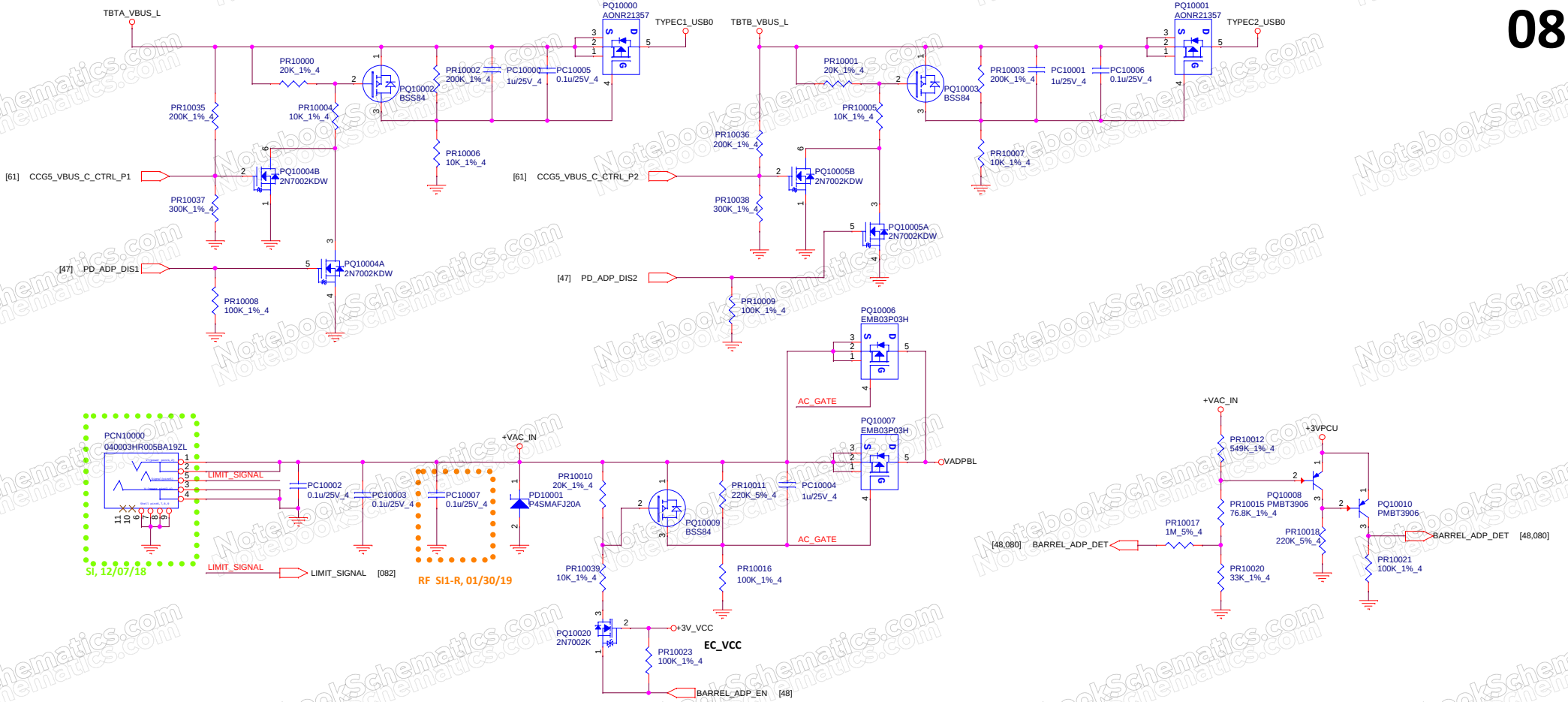

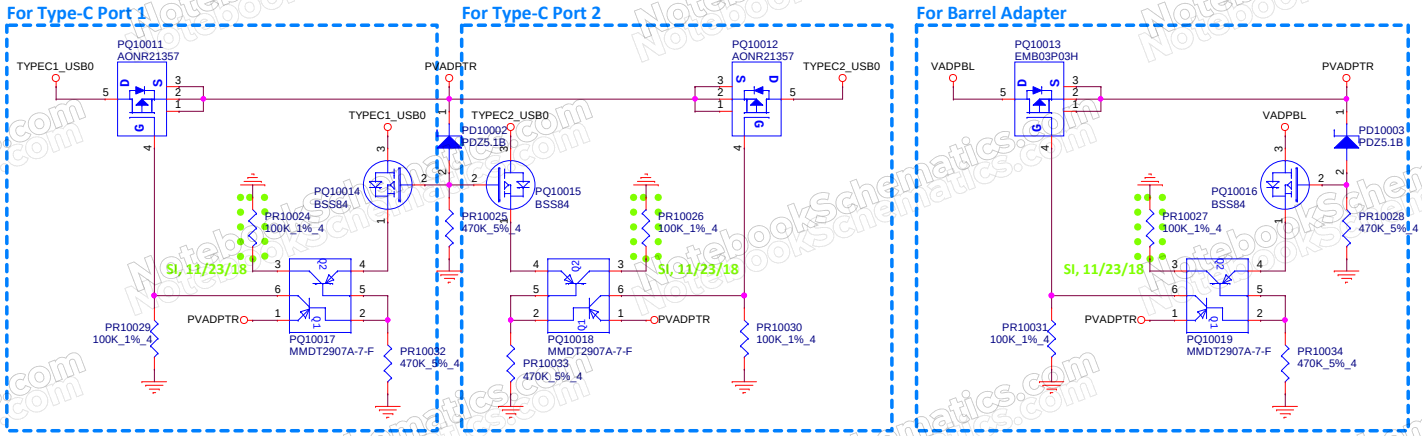

NB5

PROJECT : Anchorbay

Quanta Computer Inc.

Size	Document Number	Rev
Custom	080-- TYPE-C/Barrel switch	1A
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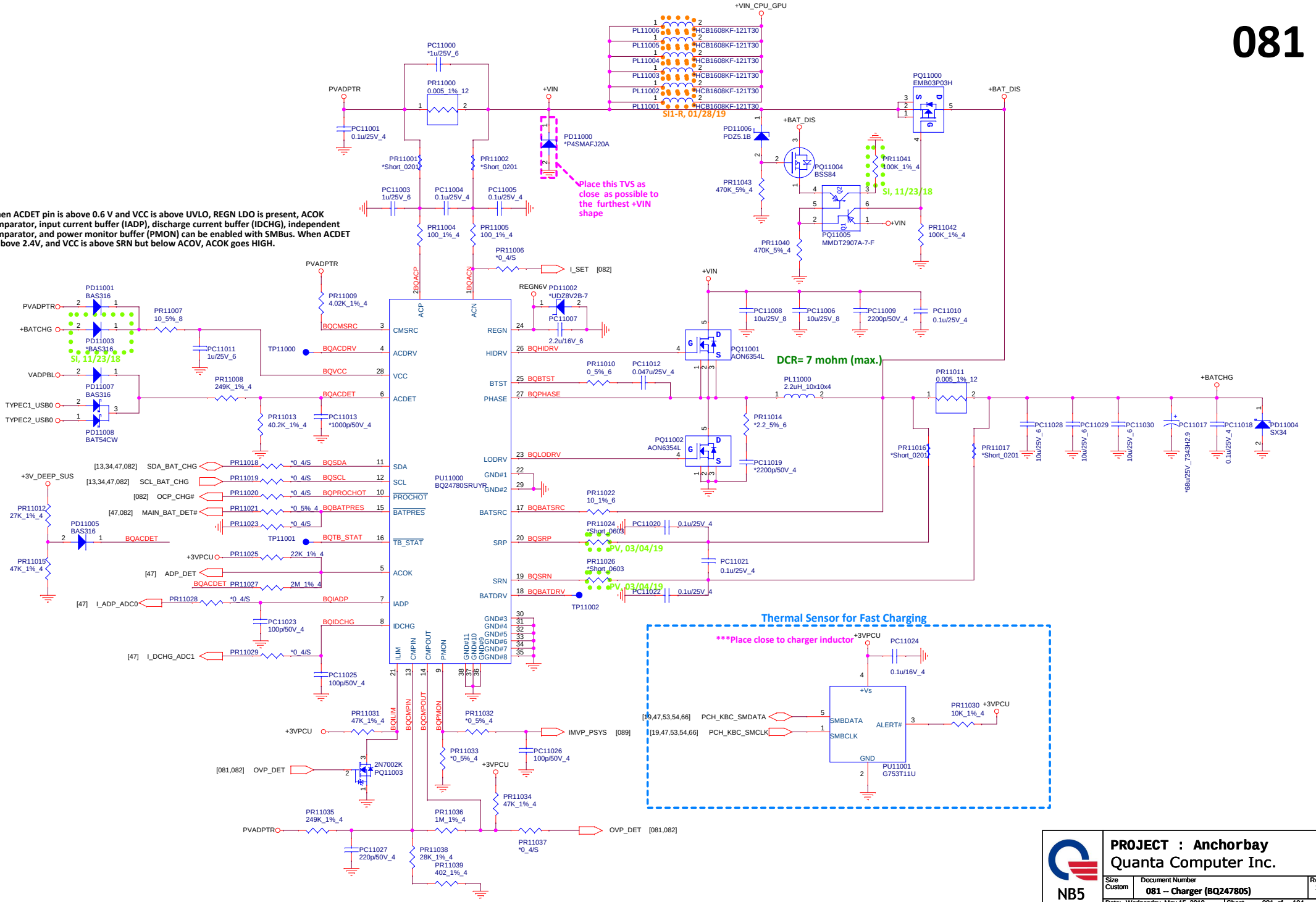
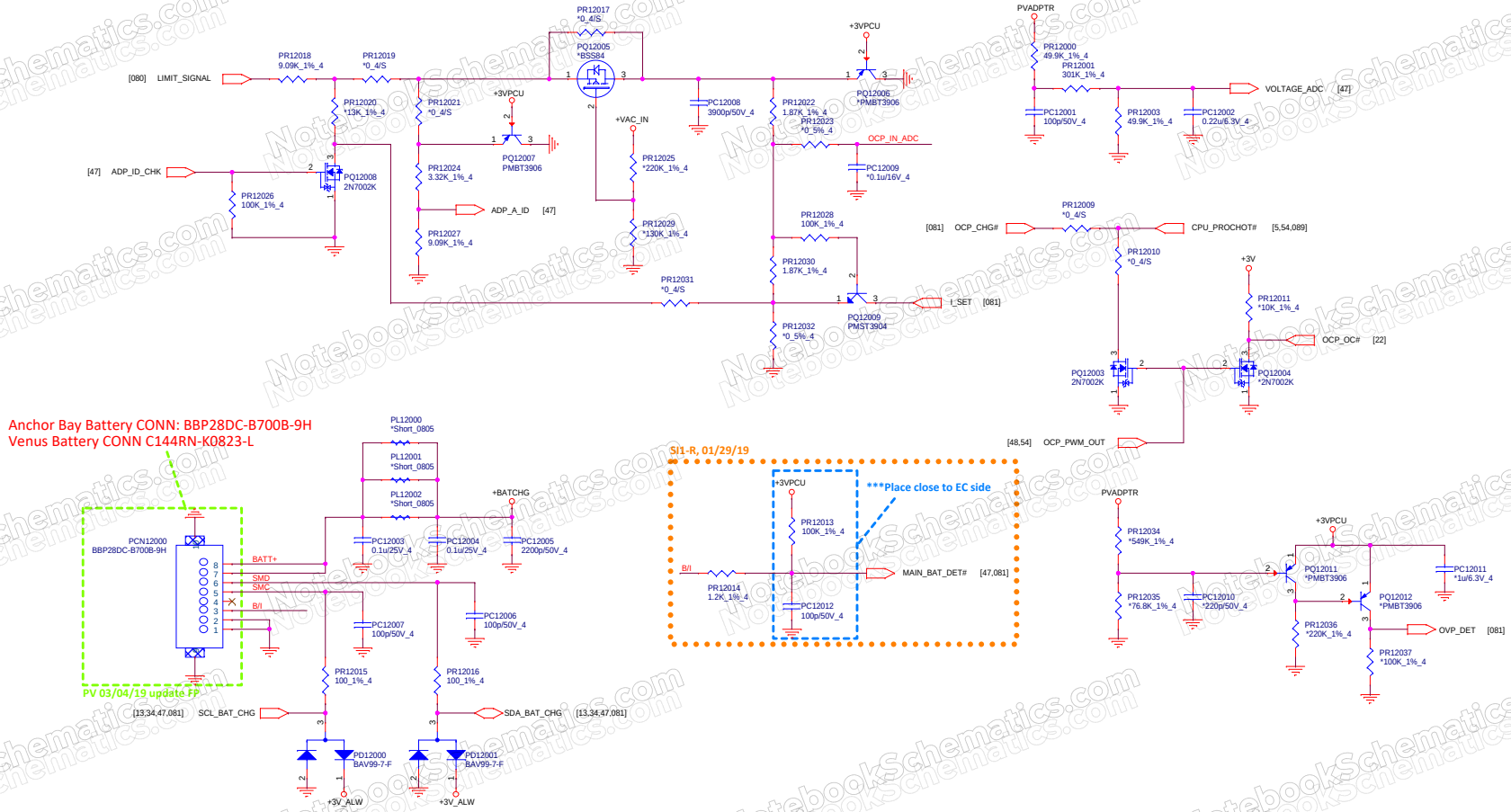
When ACDET pin is above 0.6 V and VCC is above UVLO, REGN LDO is present, ACOK comparator, input current buffer (IADP), discharge current buffer (IDCHG), independent comparator, and power monitor buffer (PMON) can be enabled with SMBus. When ACDET is above 2.4V, and VCC is above SRN but below ACOV, ACOK goes HIGH.



NB5	**PROJECT : Anchorbay** Quanta Computer Inc.
Size: Custom	Document Number: 081 -- Charger (BQ24780S)
Rev: 1A	
Date: Wednesday, May 15, 2019	Sheet: 081 of 104



Anchor Bay Battery CONN: BBP28DC-B700B-9H
Venus Battery CONN C144RN-K0823-L

SI1-R, 01/29/19

NB5	PROJECT : Anchorbay Quanta Computer Inc.	
Size	Document Number 082 -- Charger II	Rev 1A
Date: Wednesday, May 15, 2019	Sheet 082 of 104	

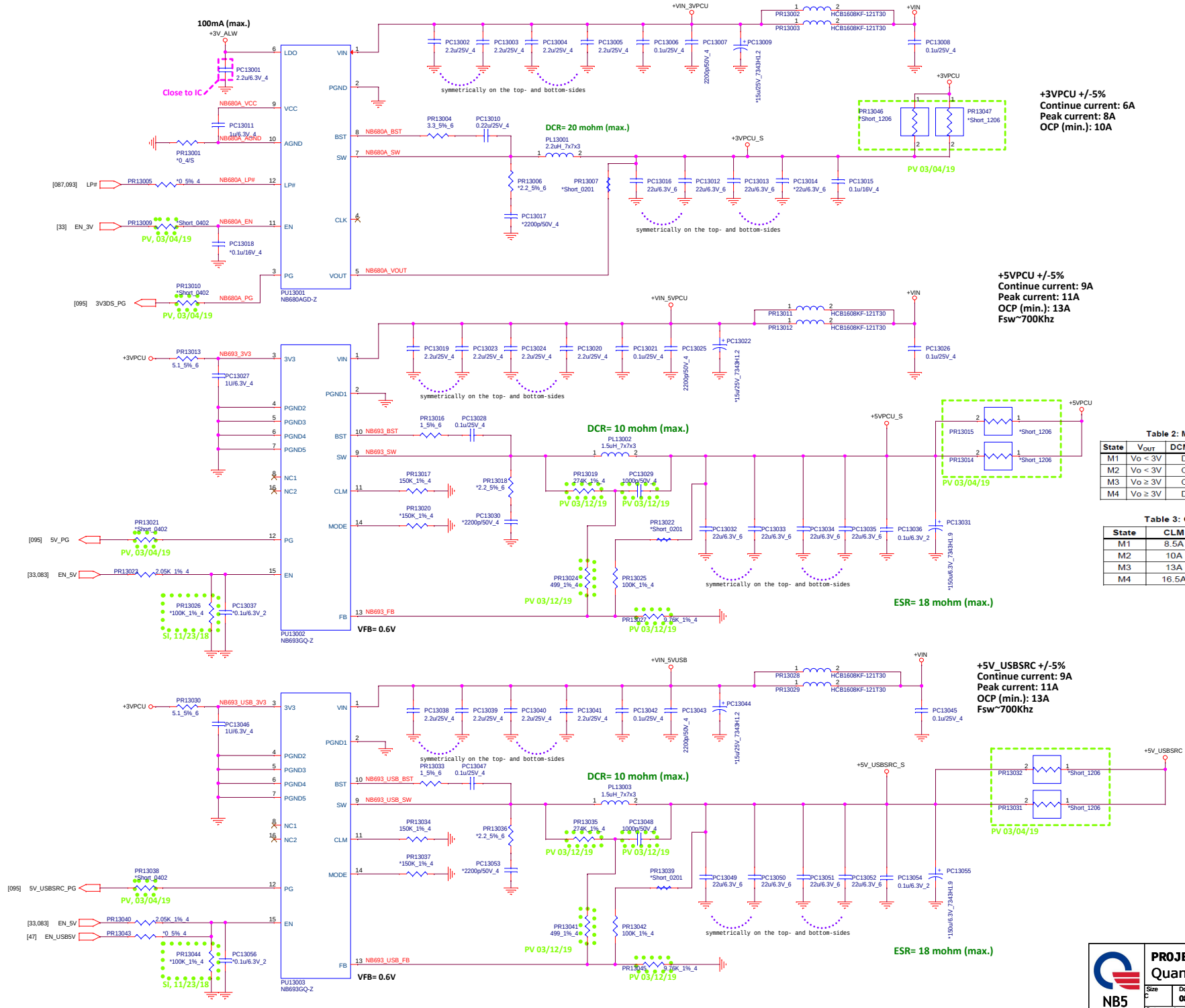


Table 2: MODE Selection

State	V_{OUT}	DCM/CCM	Resistor to GND
M1	Vo < 3V	DCM	0Ω
M2	Vo < 3V	CCM	90kΩ
M3	Vo ≥ 3V	CCM	150kΩ
M4	Vo ≥ 3V	DCM	>230kΩ or float

Table 3: CLM Selection

State	CLM	Resistor to GND
M1	8.5A	0Ω
M2	10A	90kΩ
M3	13A	150kΩ
M4	16.5A	>230kΩ or float

PROJECT :	Anchorbay
	Quanta Computer Inc.
Size: C	Document Number: 083 -- +3VPCU/5VPCU/5V_USBSRC
Rev: 1A	
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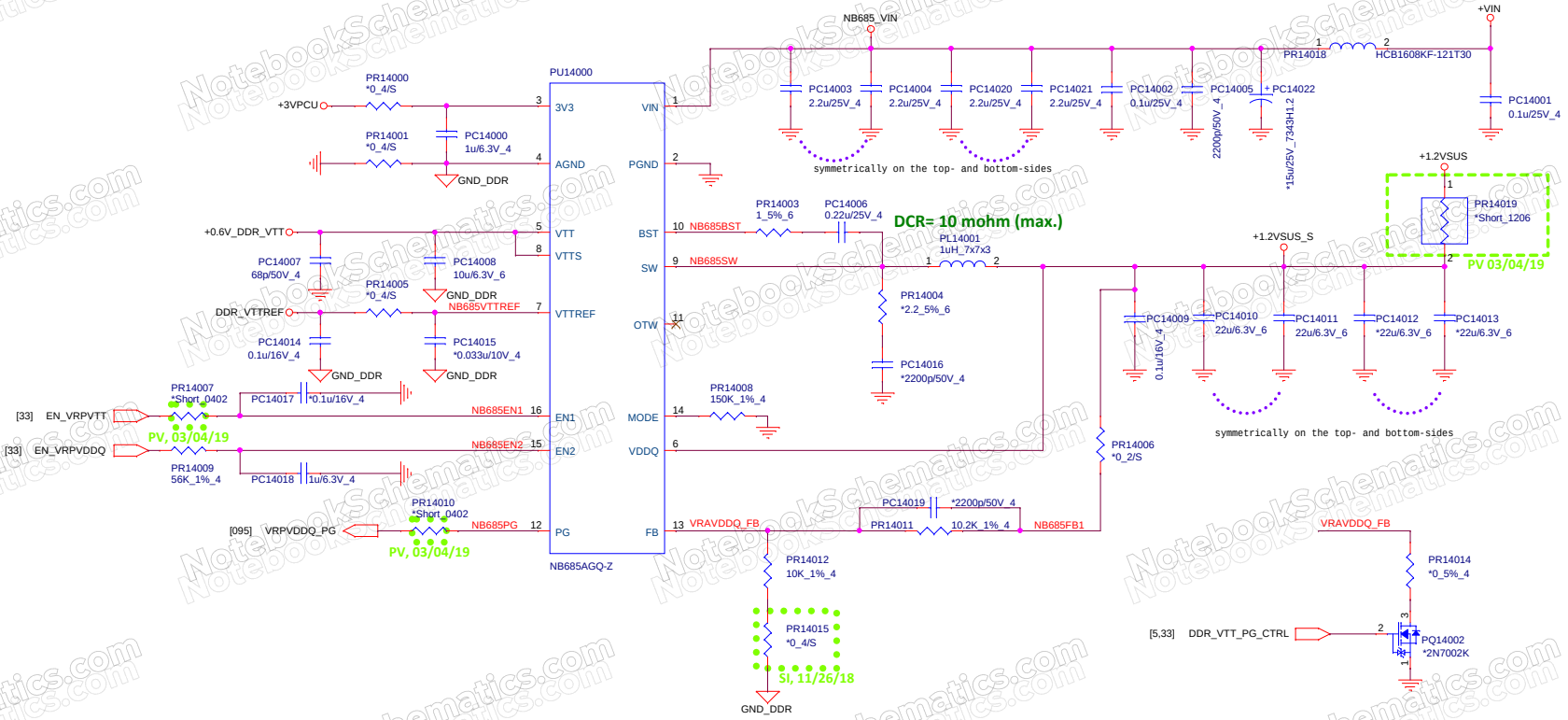
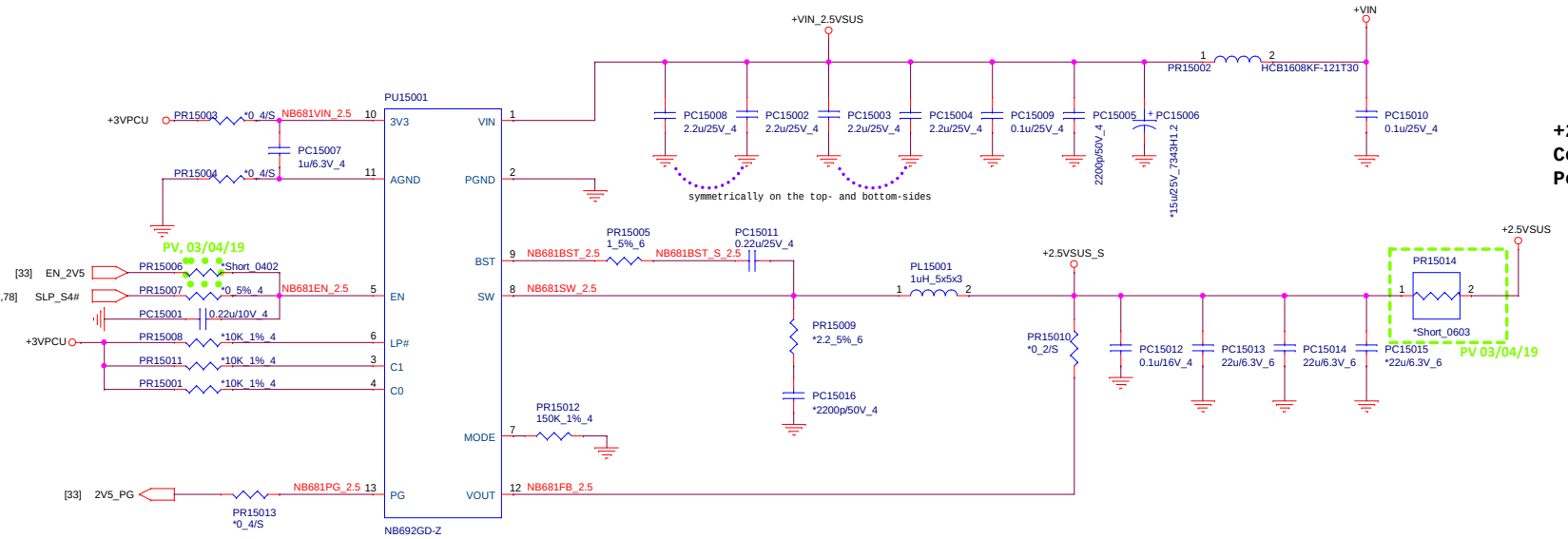
NB5

084



+1.2VSUS +/-5%
Continuous current: 8A
Peak current: 10A
OCP minimum: 12A

NB5	**PROJECT : Anchorbay** Quanta Computer Inc.	
	Size: — Document Number: **084 -- DDR4 (NB685A)**	Rev: 1A
	Date: Wednesday, May 15, 2019	Sheet 084 of 104



+2.5VSUS +/-5%
Continuous current: 2A
Peak current: 3A

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

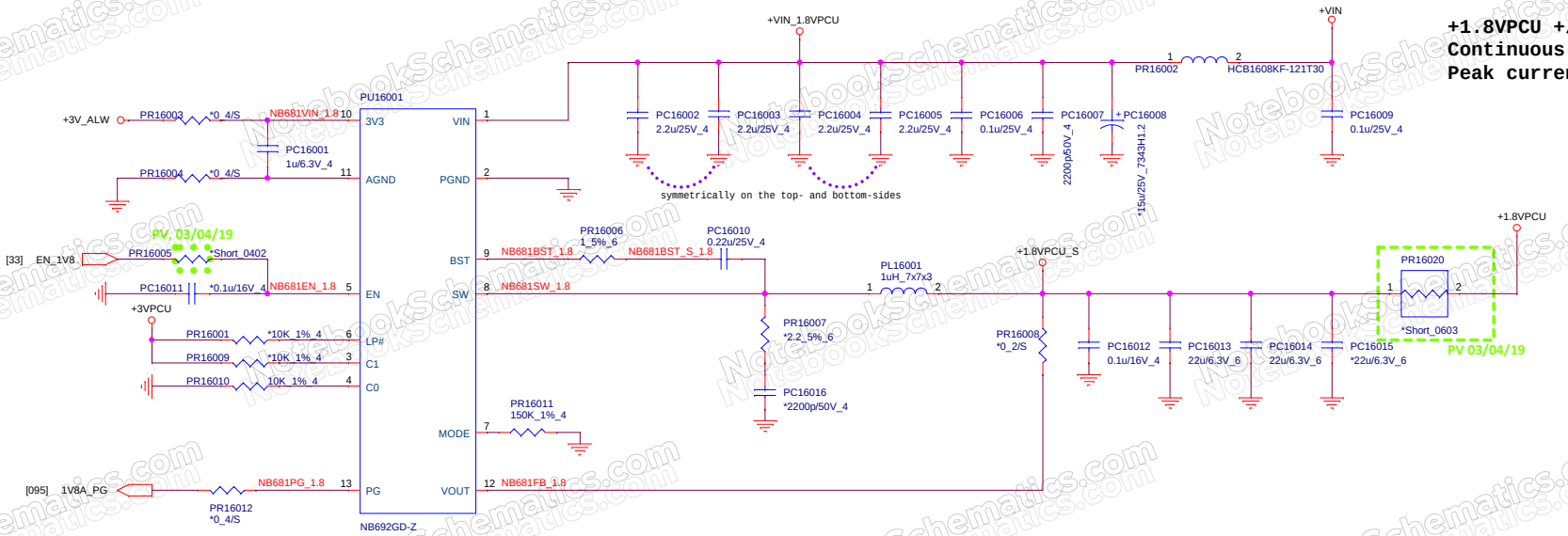
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

NB5

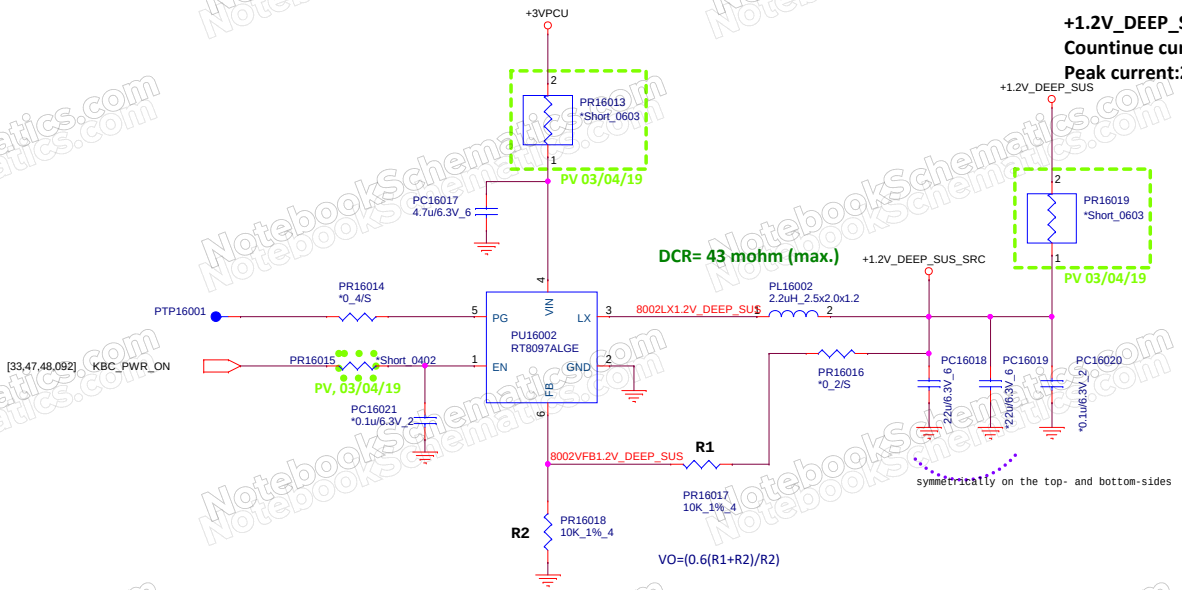
PROJECT : Anchorbay
Quanta Computer Inc.

Size	Document Number	Rev
Custom	085 -- +2.5VSUS (NB681A)	1A
Date: Wednesday, May 15, 2019	Sheet 085 of 104	

086



+1.8VPCU +/-5%
Continuous current:1A
Peak current:2A



DCR= 43 mohm (max.)

+1.2V_DEEP_SUS +/- 5%
Countinue current:1A
Peak current:2A

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

PROJECT : Anchorbay
Quanta Computer Inc.

Size	Document Number	Rev
Custom	086 -- +1.8VPCU (NB681A)	1A
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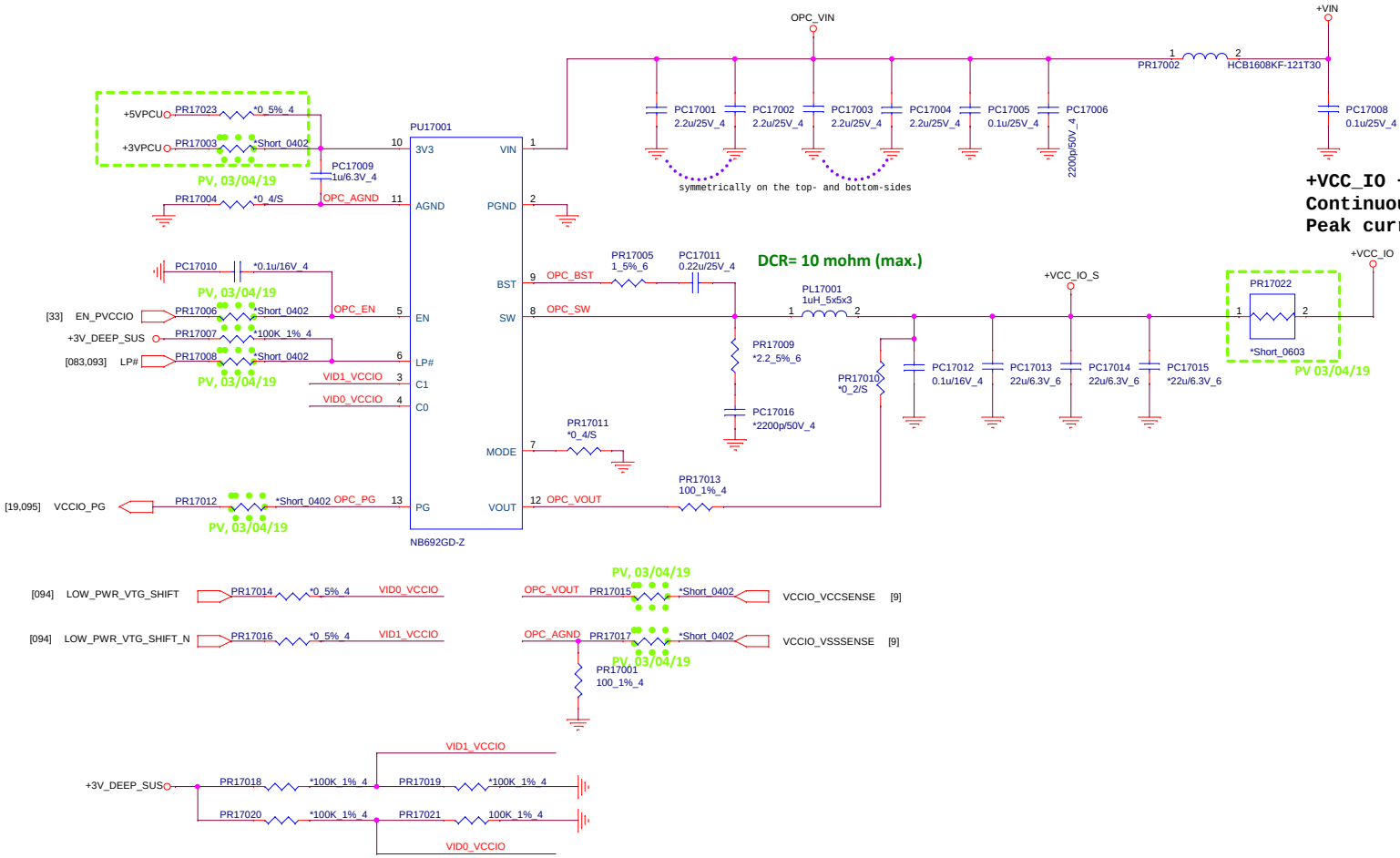
087



MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM_CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

NB5

PROJECT : Anchorbay

Quanta Computer Inc.

Size	Document Number	Rev
	087 -- +VCC_IO (NB681A)	1A

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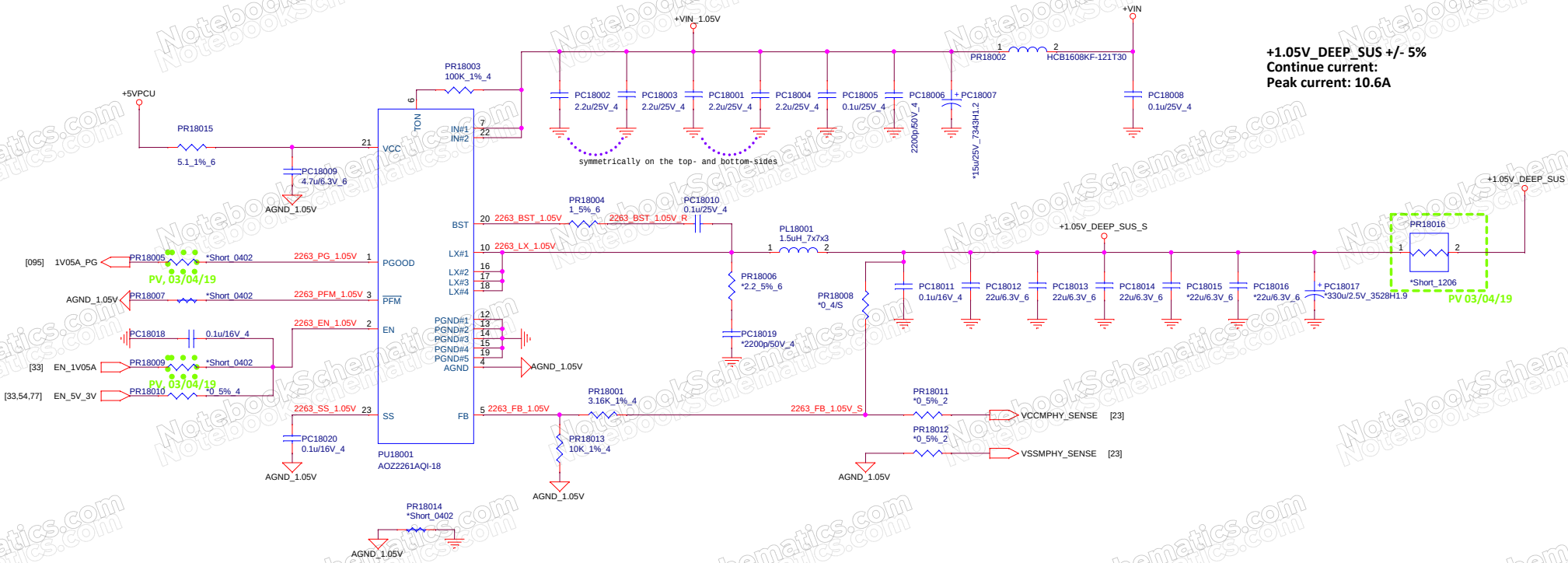
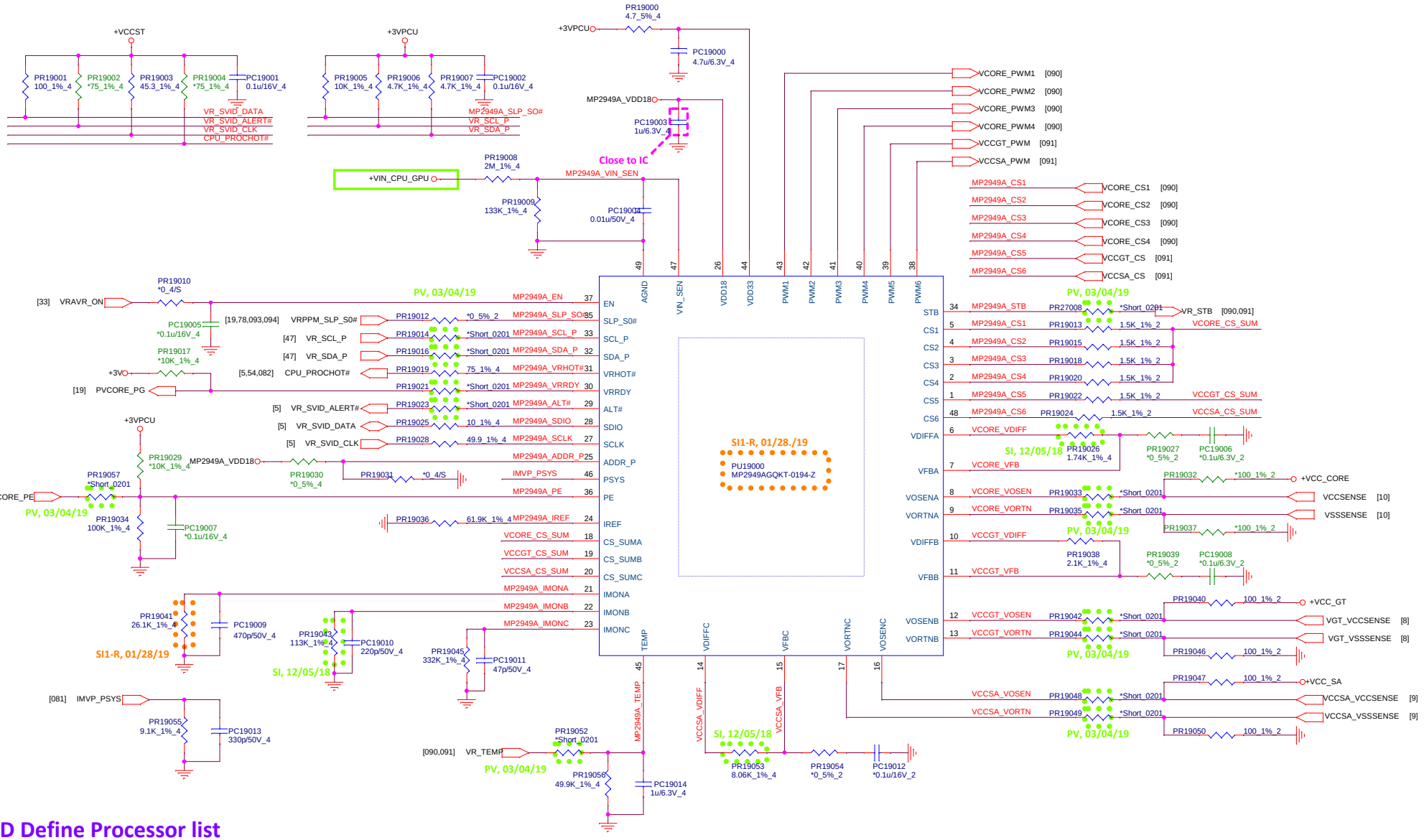


NB5	PROJECT : Anchorbay Quanta Computer Inc.	
Size	Document Number 088 -- +1.05V_ DEEP_SUS(AOZ2263)	Rev 1A
Date: Wednesday, May 15, 2019	Sheet 088 of 104	



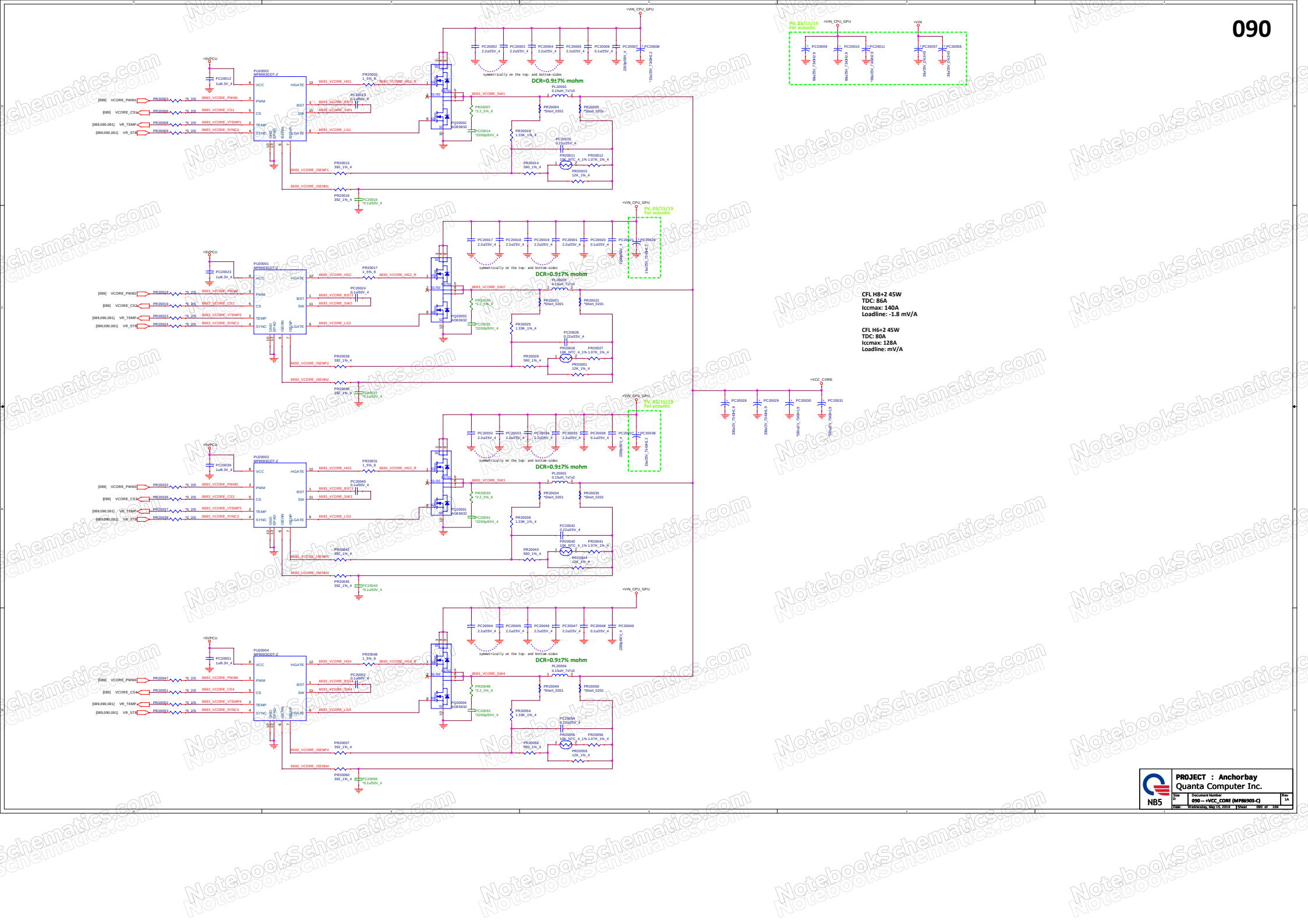
PDD Define Processor list

Category	Specifics	
Processors		processor included in BU AV
	9th Generation Intel® Core™ i5 Processor, Coffee Lake R, Quad-core, BGA:	
	Core i5-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/ X MB L3 cache/45W)	kit processors not available with iAMT
	Core i5-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/ X MB L3 cache/45W)	
	9th Generation Intel® Core™ i7 Processor, Coffee Lake R, Hexa-core, BGA:	
	Core i7-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/ X MB L3 cache/45W)	kit processors not available with iAMT
	Core i7-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/ X MB L3 cache/45W)	
	9th Generation Intel® Core™ i9 Processor, Coffee Lake R, Octa-core, BGA:	
	Core i9-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/ X MB L3 cache/45W)	
	Intel® XEON Processor, Coffee Lake R, Octa-core, BGA:	
	Xeon E-xxxx (X.X GHz (up to X.X GHz)/xxxx MHz/X MB L3 cache/45W)	

NB5

PROJECT : Anchorbay
Quanta Computer Inc.

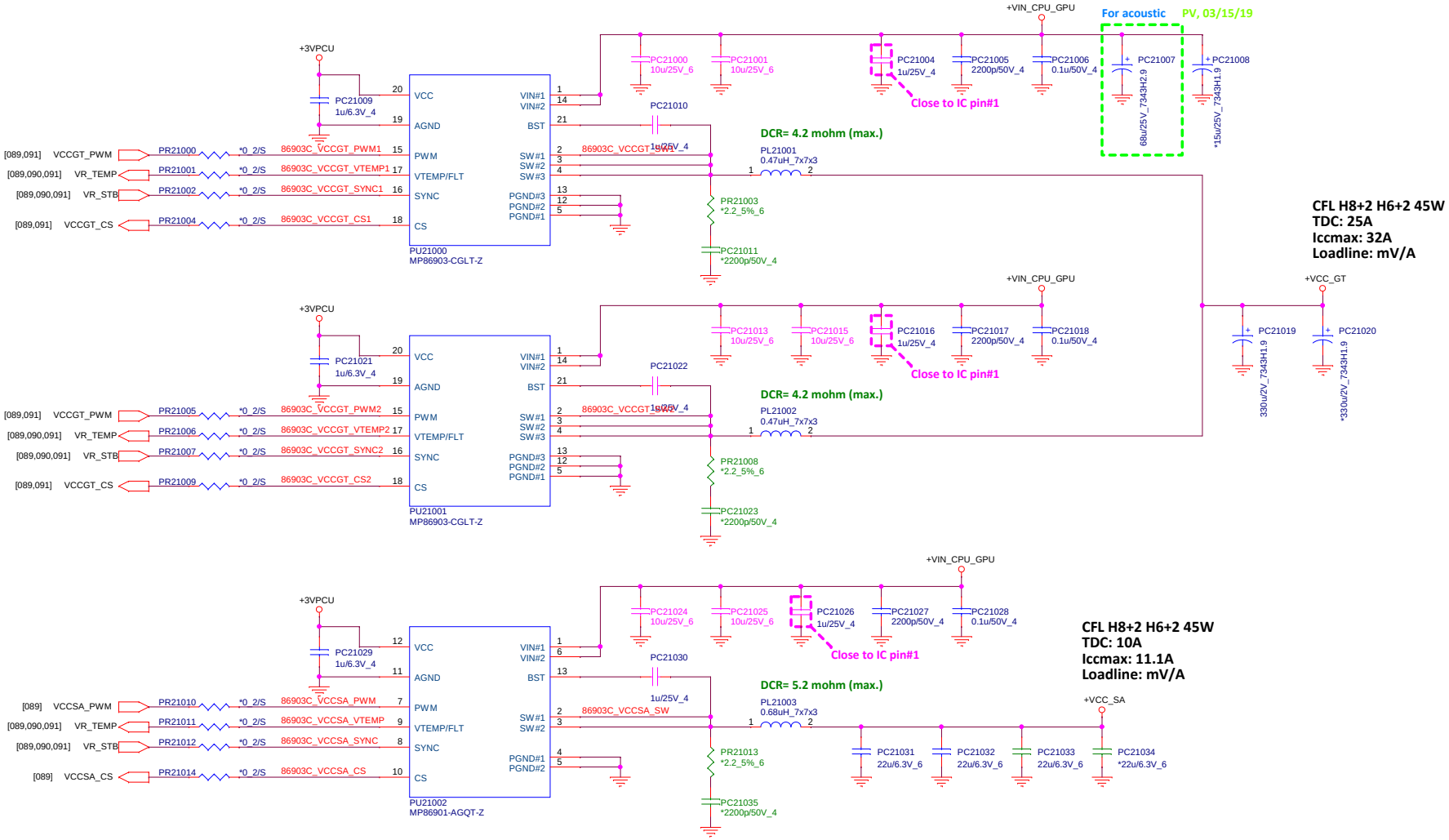
Size	Document Number	Rev
Custom	089 -- CPU CORE VR (MP2949A)	1A
Date: Wednesday, May 15, 2019	Sheet 089 of 104	



PROJECT : Anchorbay
Quanta Computer Inc.

Size	Document Number	Rev
D	090 -- +VCC_CORE (MP86903-C)	1A

Date: Wednesday, May 15, 2019 Sheet 090 of 104



NB5	PROJECT : Anchorbay Quanta Computer Inc.	
Size: Custom	Document Number: 091 -- +VCC_GT/+VCC_SA	Rev: 1A
Date: Wednesday, May 15, 2019	Sheet: 091 of 104	

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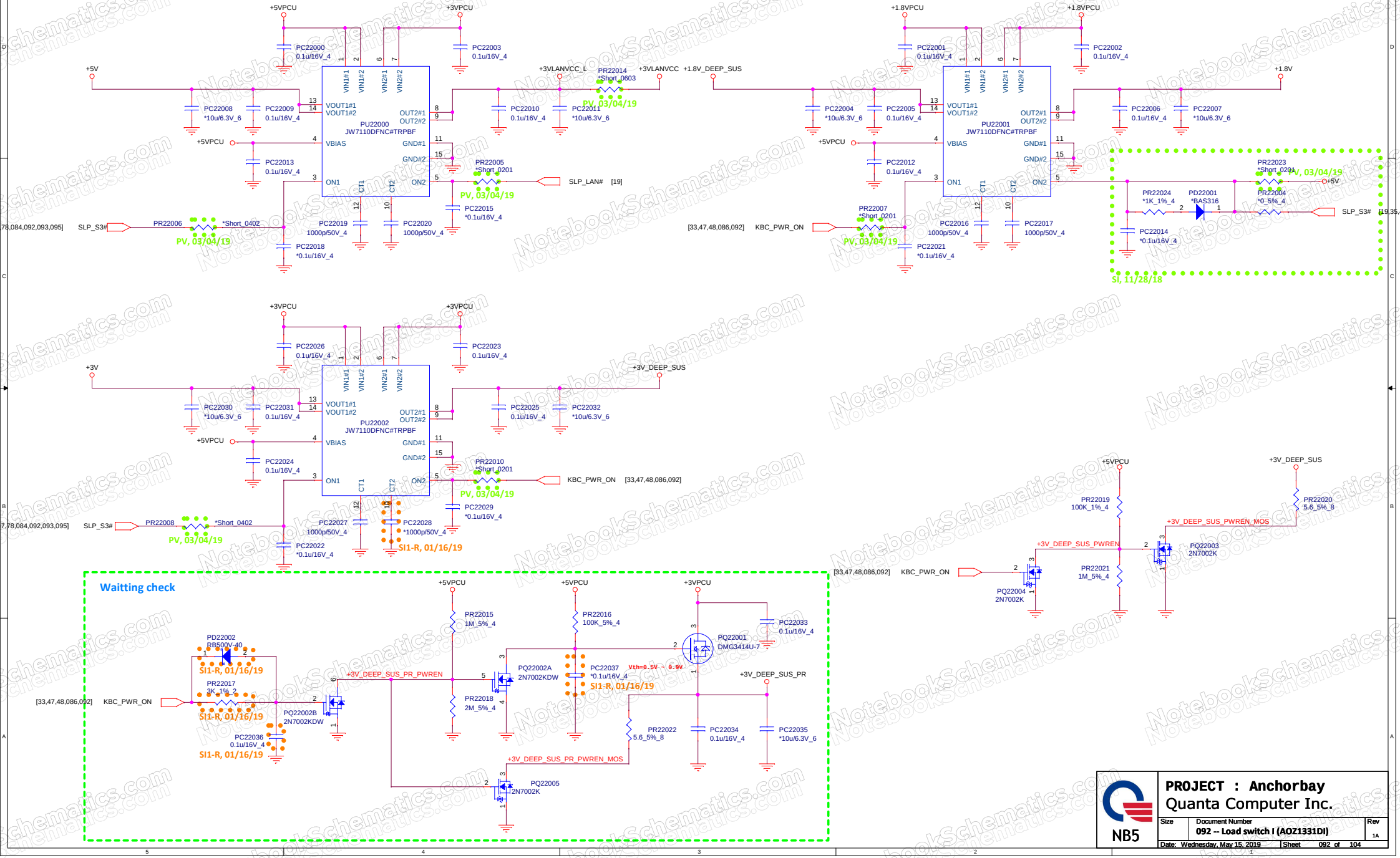
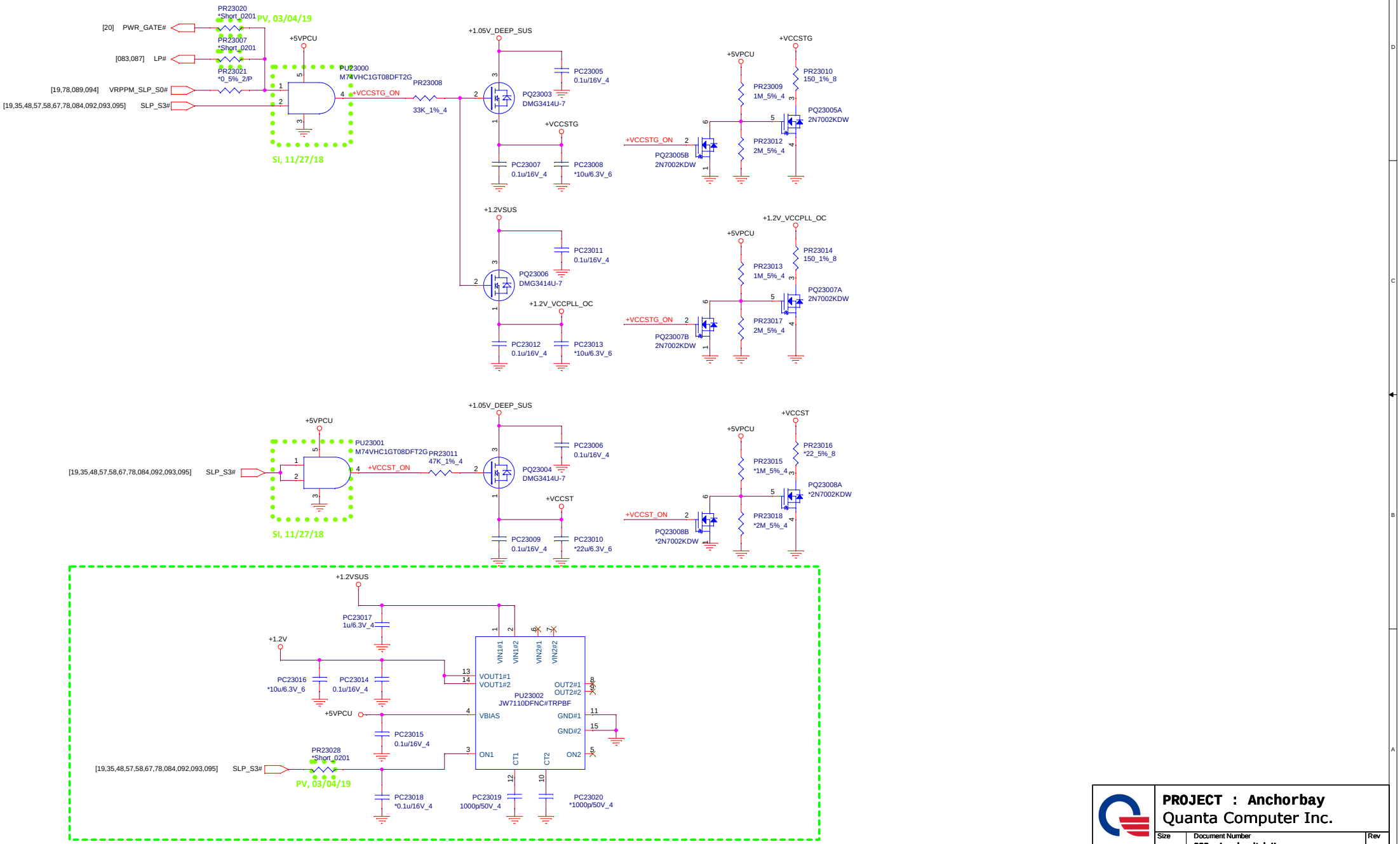


PROJECT : Anchorbay
Quanta Computer Inc.

Size	Document Number	Rev
	092 -- Load switch I (AOZ1331DI)	1A
Date: Wednesday, May 15, 2019	Sheet 092 of 104	

NB5

093



PROJECT : Anchorbay
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	093 -- Load switch II	1A
Date: Wednesday, May 15, 2019	Sheet 093 of 104	

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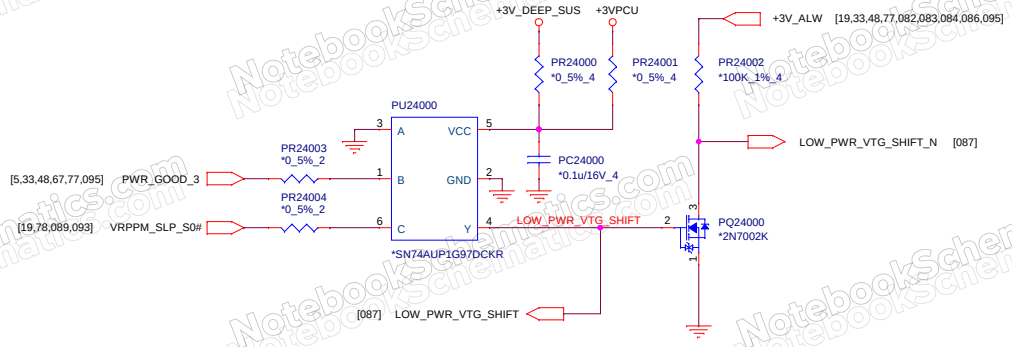


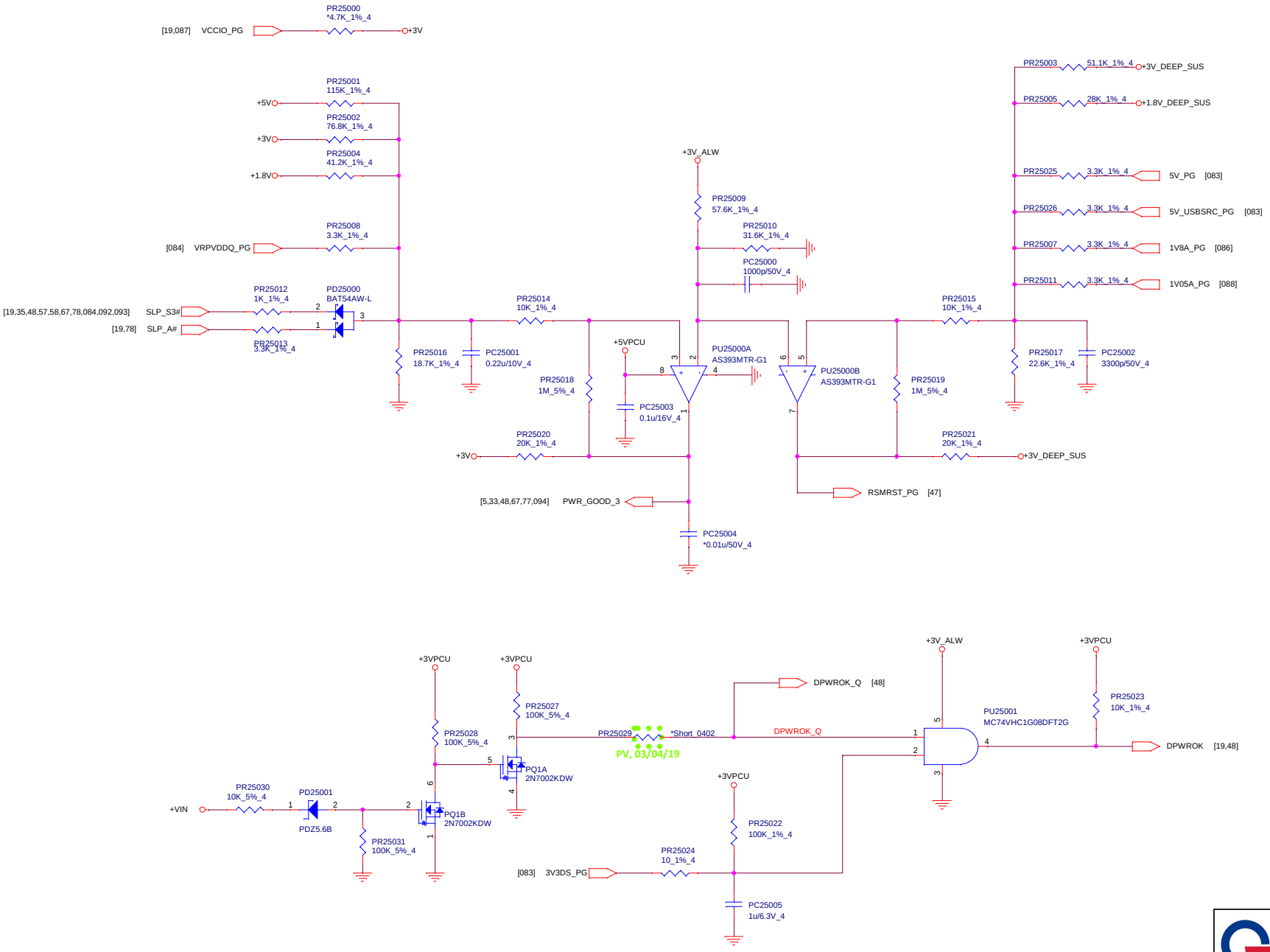
NB5

PROJECT : Anchorbay

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**094 -- Low Power Voltage Shift**	1A

Date: Wednesday, May 15, 2019 | Sheet 094 of 104



NB5

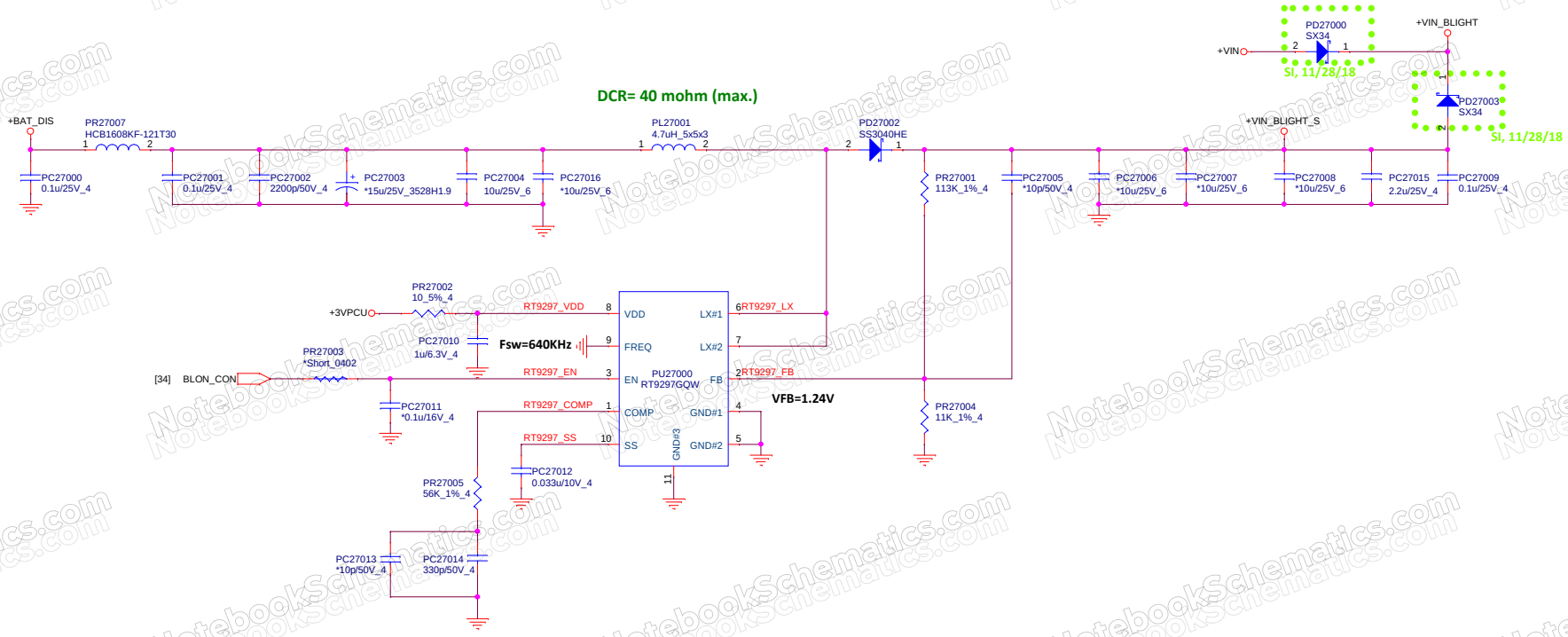
PROJECT : Anchorbay

Quanta Computer Inc.

Size	Document Number	Rev
Custom	095 -- PWROK	1A
Date: Wednesday, May 15, 2019	Sheet 095 of 104	

+VIN_BLIGHT

15.25V +/-5%
Peak current: 650mA



NB5	PROJECT : Anchorbay Quanta Computer Inc.	
Size: Custom	Document Number: 104 -- +VIN_BLIGHT	Rev: 1A
Date: Monday, August 14, 2017	Sheet 104 of 104	