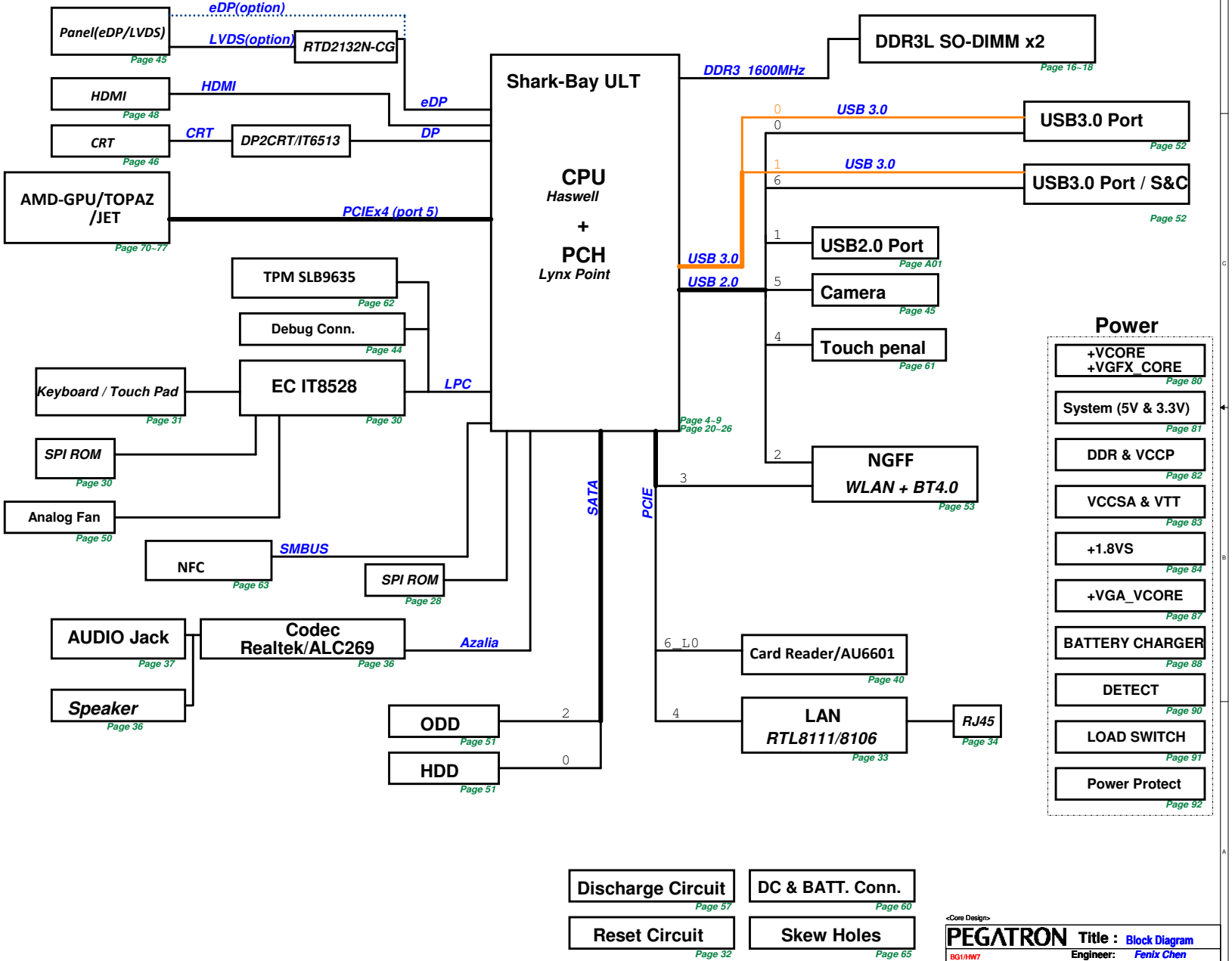
SYSTEM PAGE REF.

CASUG with Shark Bay ULT

BLOCK DIAGRAM



<Core Design>

PEGATRON Title : Block Diagram

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
C	CAS(C)UG	1.0

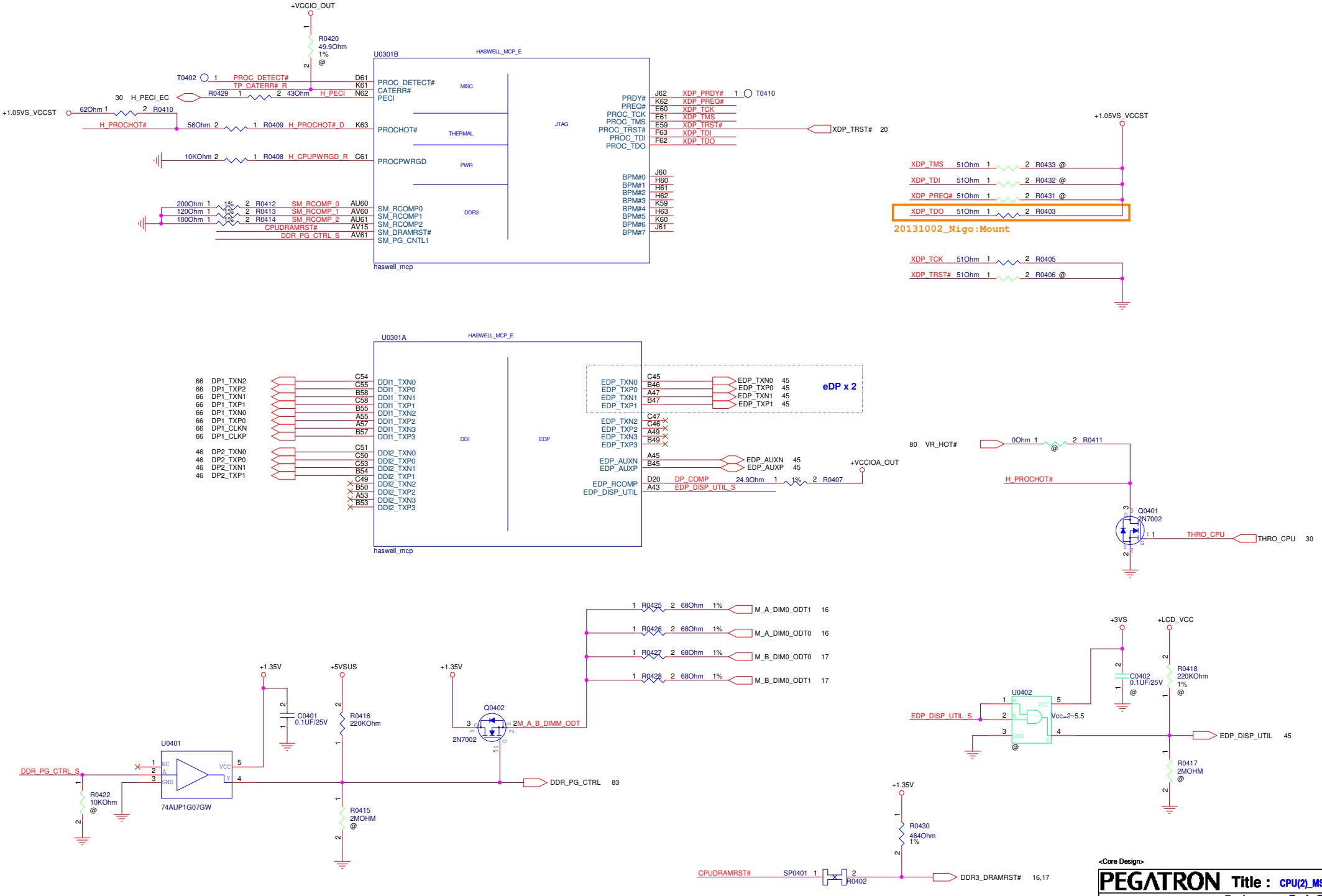
Date: Sunday, December 22, 2013 Sheet 1 of 103

<Core Design>

Title	<Title>	
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 2 of 103	

<Core Design>

Title <Title>		
Size C	Document Number CAS(C)UG	Rev 1.0
Date: Sunday, December 22, 2013	Sheet 3 of 103	



<Core Design>

PEGATRON

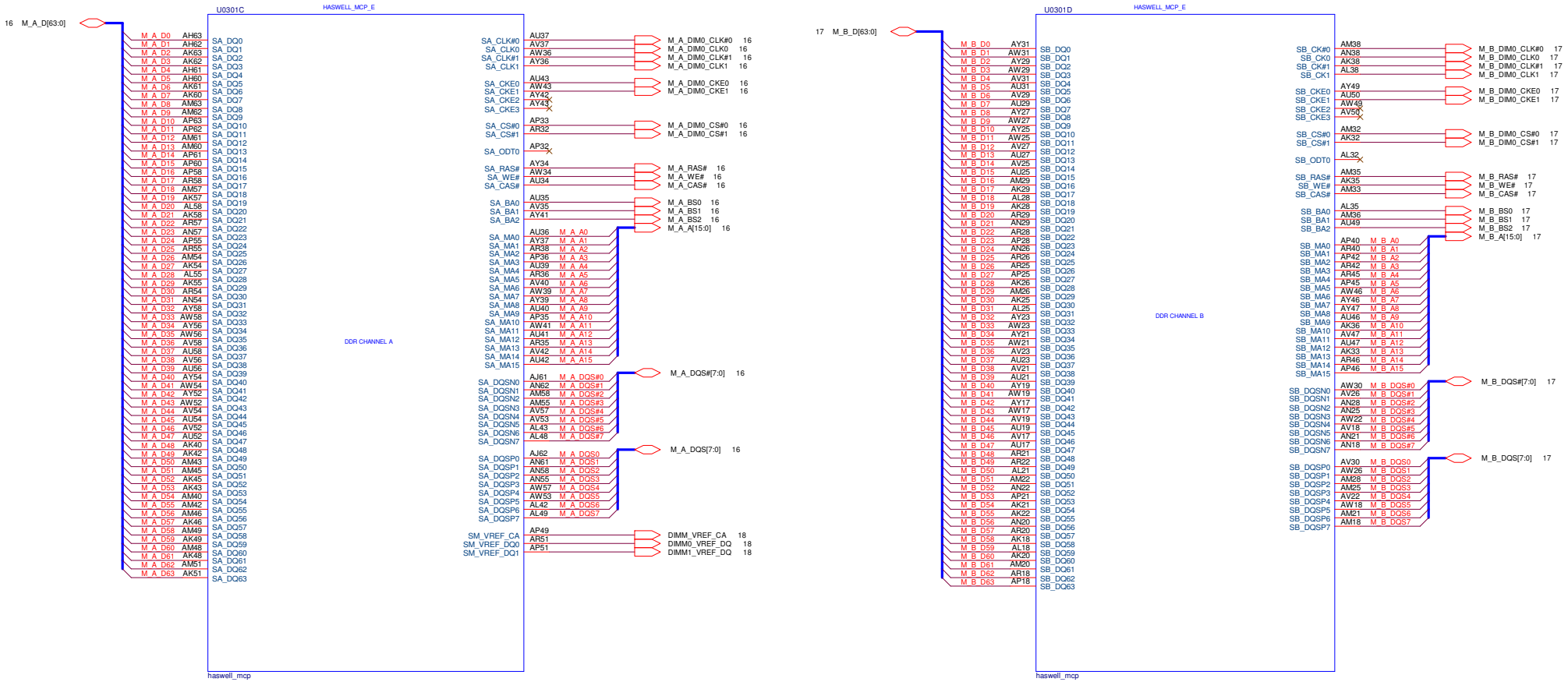
Title : CPU(2)_MSIC,DDI,eDP

BG1/HW7

Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 4 of 103



Vinafix.com

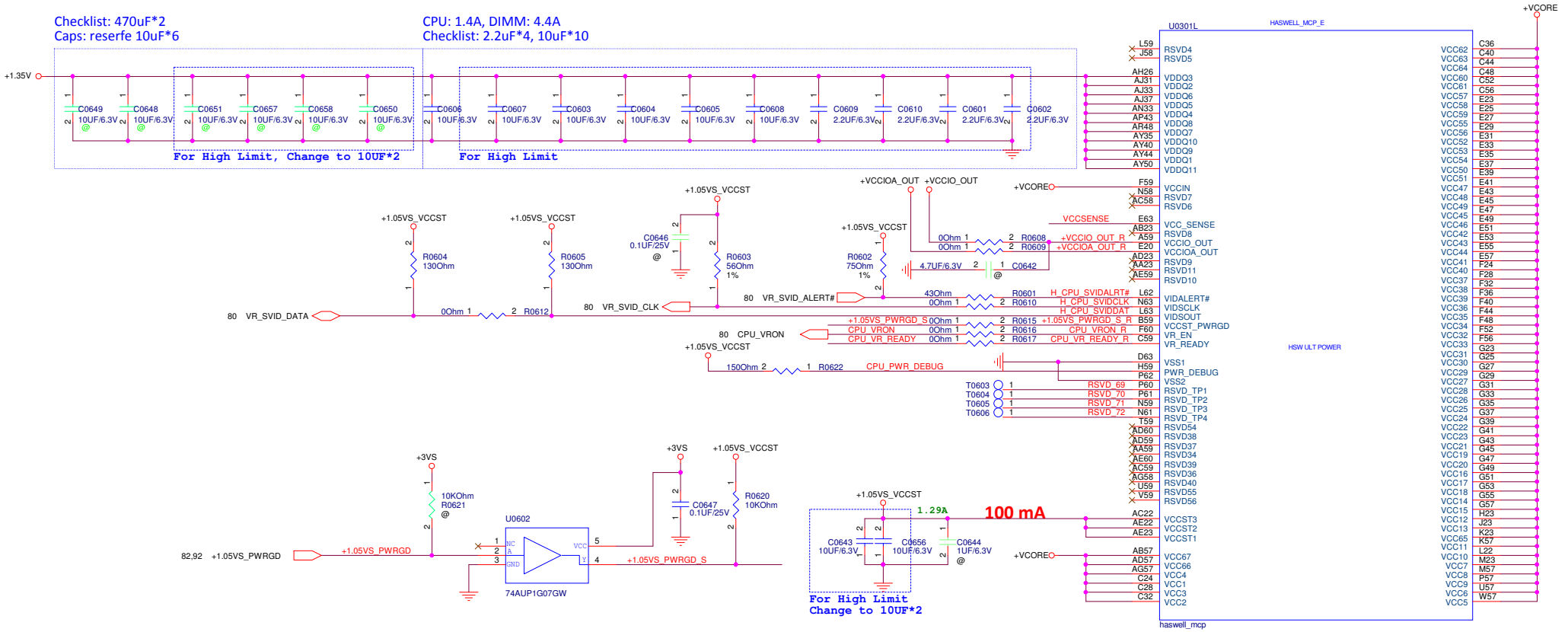
<Core Design>

PEGATRON Title : CPU(3)_DDR3L

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	2.1

Date: Sunday, December 22, 2013 Sheet 5 of 103



+VCORE

C0652 10UF/6.3V

C0653 10UF/6.3V

For High Limit

+VCORE 32A

Intel Checklist: used 30pcs(7pcs un-used)

Power side: 20pcs (4pcs un-used)

VGST: 30pcs (14pcs un-used)

<Core Design>

PEGATRON Title : CPU(4)_PWR

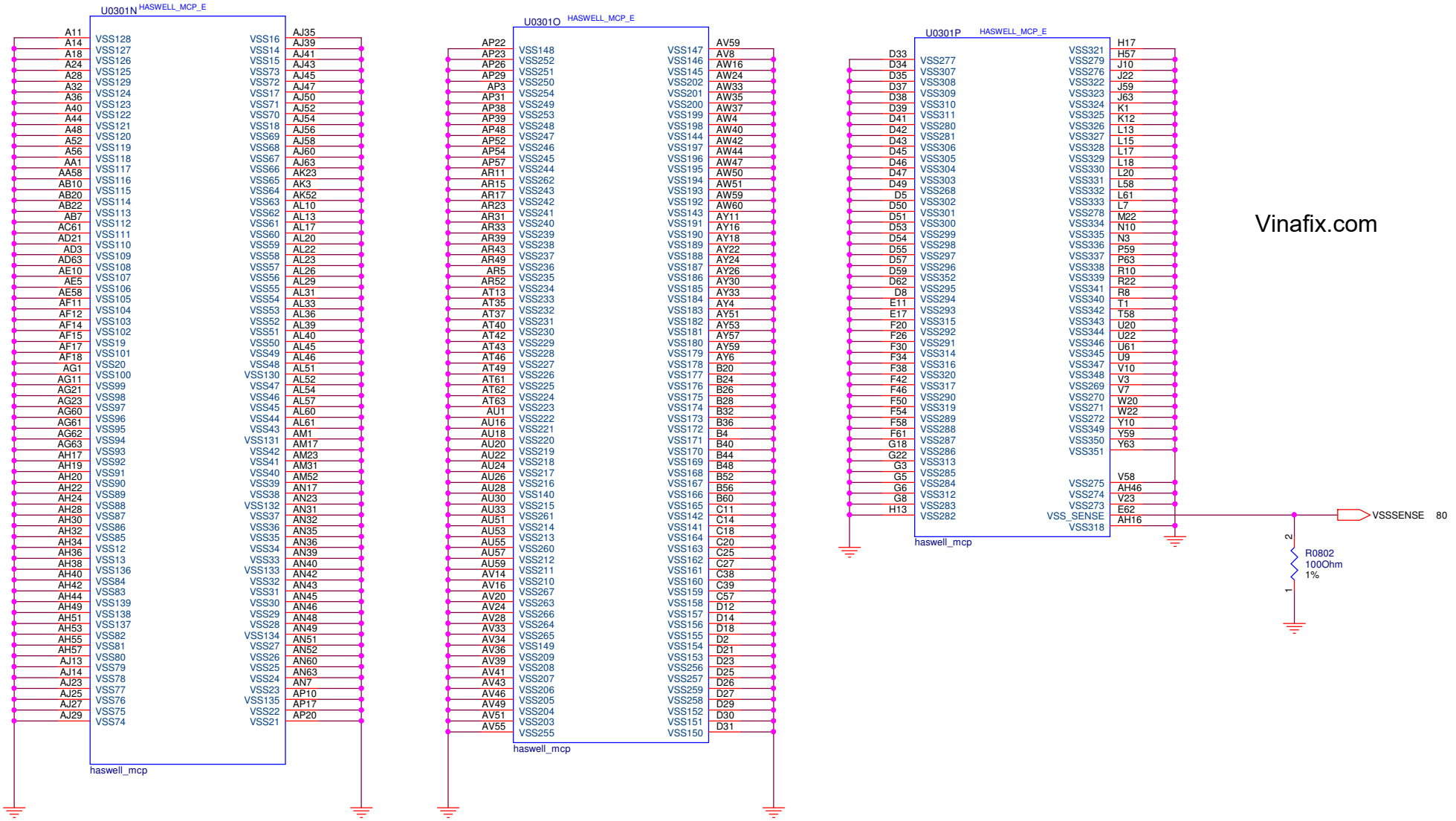
BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 6 of 103

<Core Design>

Title	<Title>	
Size C	Document Number CAS(C)UG	Rev 1.0
Date: Sunday, December 22, 2013	Sheet 7 of 103	



<Core Design>

PEGATRON Title : CPU(6)_CFG,RSVD,GND

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 8 of 103

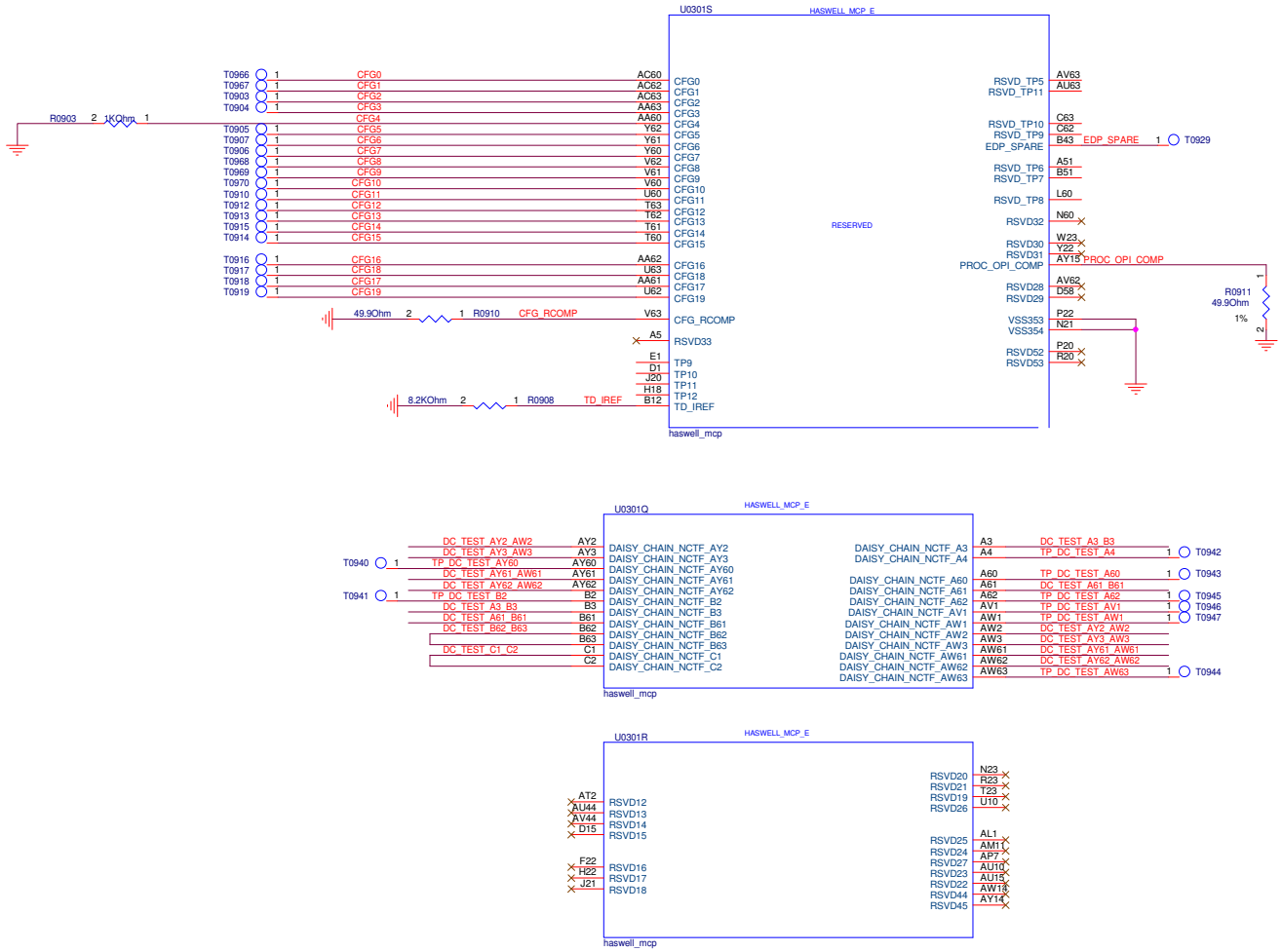
CFG strapping information: The CFG signals have a default value of '1'

CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.

CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[19:5]: Reserved configuration lanes.
A test point may be placed on the board for these lands.



<Core Design>

PEGATRON Title: CPU(7)_CFG,RSVD,GND

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 9 of 103

<Core Design>

Title <Title>		
Size C	Document Number CAS(C)UG	Rev 1.0
Date: Sunday, December 22, 2013	Sheet 10 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 11 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 12 of 103	

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Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 13 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 14 of 103	

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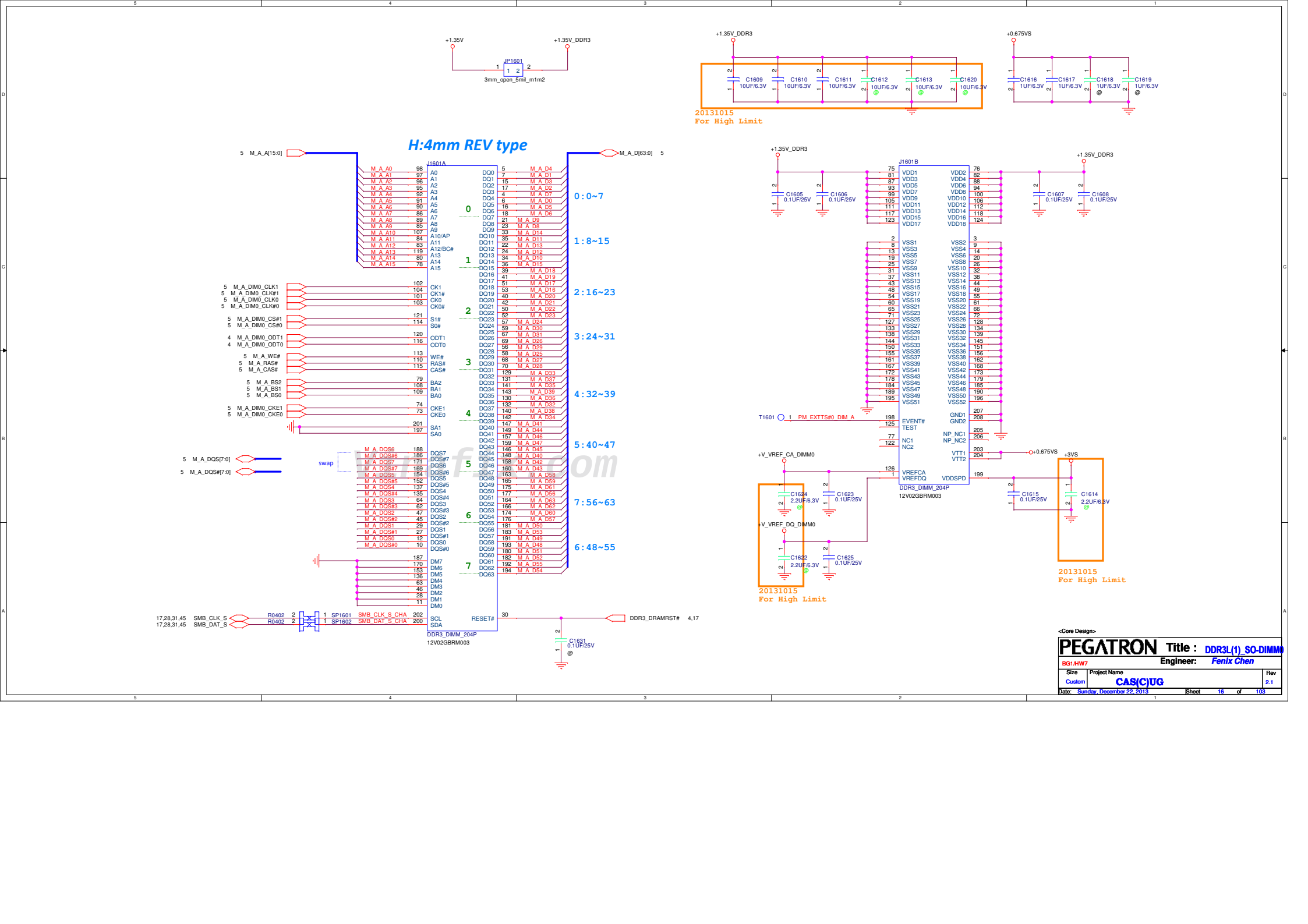
Title: <Title>		
Size: C	Document Number: CAS(C)UG Vinafix.com	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 15 of 103	


+1.35V
+1.35V_DDR3
JP1601
3mm_open_5mil_m1m2
+1.35V_DDR3
C1609 10UF/6.3V
C1610 10UF/6.3V
C1611 10UF/6.3V
C1612 10UF/6.3V @
C1613 10UF/6.3V @
C1620 10UF/6.3V @
20131015
For High Limit
+0.675VS
C1616 1UF/6.3V
C1617 1UF/6.3V
C1618 1UF/6.3V @
C1619 1UF/6.3V @
H:4mm REV type
5 M_A_A[15:0]
J1601A
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15
5 M_A_DIM0_CLK1
5 M_A_DIM0_CLK#1
5 M_A_DIM0_CLK0
5 M_A_DIM0_CLK#0
CK1 CK1# CK0 CK0#
5 M_A_DIM0_CS#1
5 M_A_DIM0_CS#0
S1# S0#
4 M_A_DIM0_ODT1
4 M_A_DIM0_ODT0
ODT1 ODT0
5 M_A_WE#
5 M_A_RAS#
5 M_A_CAS#
WE# RAS# CAS#
5 M_A_BS2
5 M_A_BS1
5 M_A_BS0
BA2 BA1 BA0
5 M_A_DIM0_CKE1
5 M_A_DIM0_CKE0
CKE1 CKE0
SA1 SA0
5 M_A_DQS[7:0]
5 M_A_DQS#[7:0]
swap
M_A_DQS6 M_A_DQS#6 M_A_DQS7 M_A_DQS#7 M_A_DQS5 M_A_DQS#5 M_A_DQS4 M_A_DQS#4 M_A_DQS3 M_A_DQS#3 M_A_DQS2 M_A_DQS#2 M_A_DQS1 M_A_DQS#1 M_A_DQS0 M_A_DQS#0
DQS7 DQS#7 DQS6 DQS#6 DQS5 DQS#5 DQS4 DQS#4 DQS3 DQS#3 DQS2 DQS#2 DQS1 DQS#1 DQS0 DQS#0
DM7 DM6 DM5 DM4 DM3 DM2 DM1 DM0
17,28,31,45 SMB_CLK_S
17,28,31,45 SMB_DAT_S
R0402
SP1601 SMB_CLK_S_CHA
SP1602 SMB_DAT_S_CHA
SCL SDA
RESET#
DDR3_DRAMRST# 4,17
C1631 0.1UF/25V @
DDR3_DIMM_204P
12V02GBRM003
M_A_D[63:0] 5
M_A_D0 M_A_D1 M_A_D2 M_A_D3 M_A_D4 M_A_D5 M_A_D6 M_A_D7 M_A_D8 M_A_D9 M_A_D10 M_A_D11 M_A_D12 M_A_D13 M_A_D14 M_A_D15 M_A_D16 M_A_D17 M_A_D18 M_A_D19 M_A_D20 M_A_D21 M_A_D22 M_A_D23 M_A_D24 M_A_D25 M_A_D26 M_A_D27 M_A_D28 M_A_D29 M_A_D30 M_A_D31 M_A_D32 M_A_D33 M_A_D34 M_A_D35 M_A_D36 M_A_D37 M_A_D38 M_A_D39 M_A_D40 M_A_D41 M_A_D42 M_A_D43 M_A_D44 M_A_D45 M_A_D46 M_A_D47 M_A_D48 M_A_D49 M_A_D50 M_A_D51 M_A_D52 M_A_D53 M_A_D54 M_A_D55 M_A_D56 M_A_D57 M_A_D58 M_A_D59 M_A_D60 M_A_D61 M_A_D62 M_A_D63
0 1 2 3 4 5 6 7
0:0~7
1:8~15
2:16~23
3:24~31
4:32~39
5:40~47
7:56~63
6:48~55
+1.35V_DDR3
C1605 0.1UF/25V
C1606 0.1UF/25V
C1607 0.1UF/25V
C1608 0.1UF/25V
J1601B
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52
GND1 GND2
NP_NC1 NP_NC2
VTT1 VTT2
T1601 1 PM_EXTTS#0_DIM_A
EVENT# TEST
NC1 NC2
VREFCA VREFDQ VDDSPD
+V_VREF_CA_DIMM0
+V_VREF_DQ_DIMM0
C1624 2.2UF/6.3V @
C1623 0.1UF/25V
C1622 2.2UF/6.3V @
C1625 0.1UF/25V
+0.675VS
+3VS
C1615 0.1UF/25V
C1614 2.2UF/6.3V @
20131015
For High Limit
DDR3_DIMM_204P
12V02GBRM003
20131015
For High Limit
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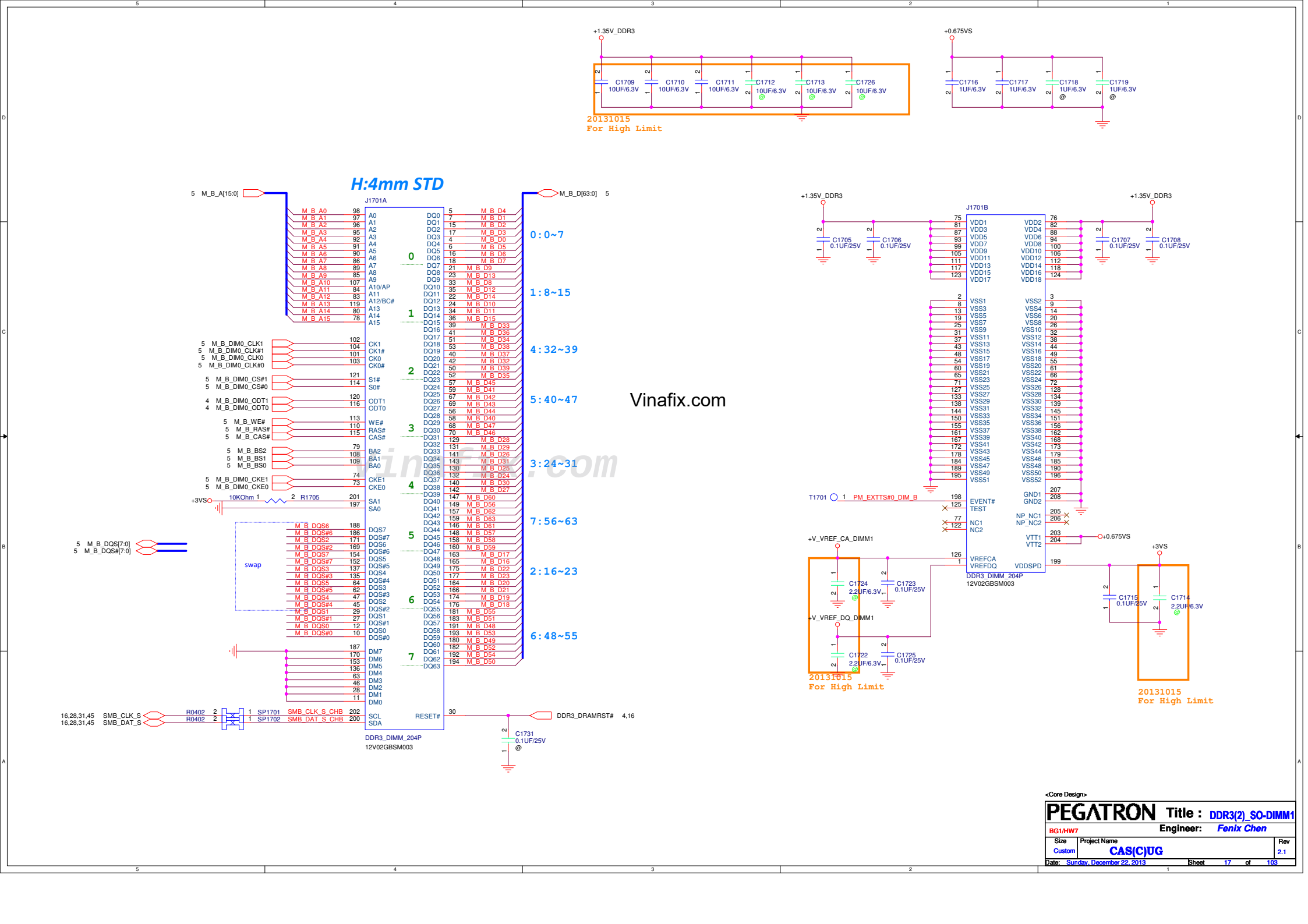
PEGATRON
Title : DDR3L(1)_SO-DIMM0
BG1/HW7
Engineer: Fenix Chen
Size Custom
Project Name CAS(C)UG
Rev 2.1
Date: Sunday, December 22, 2013
Sheet 16 of 103



<Core Design>

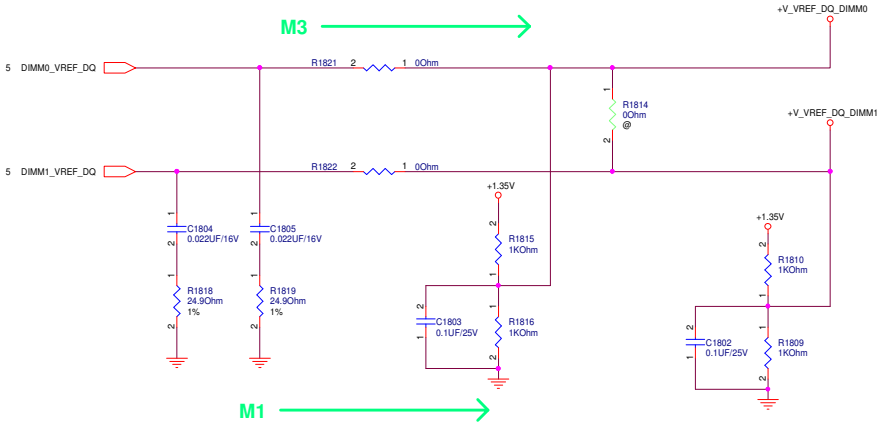
PEGATRON Title : DDR3(2)_SO-DIMM1

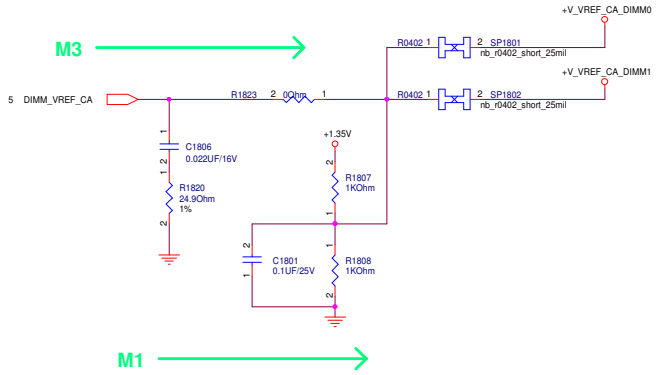
BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	2.1

Date: Sunday, December 22, 2013 Sheet 17 of 103

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off





<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 19 of 103	

for Battery RTC function

20131202: Add R2072 for AC mode.

20131001: 更換為Holder

20131119: Remove Jump and change to 0603

20131203: C2003, C2004, C2005 change to 0604

EC reset CMOS feature

Request by CSC for CMOS clear function

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

20131020: remove MOS

Card Reader

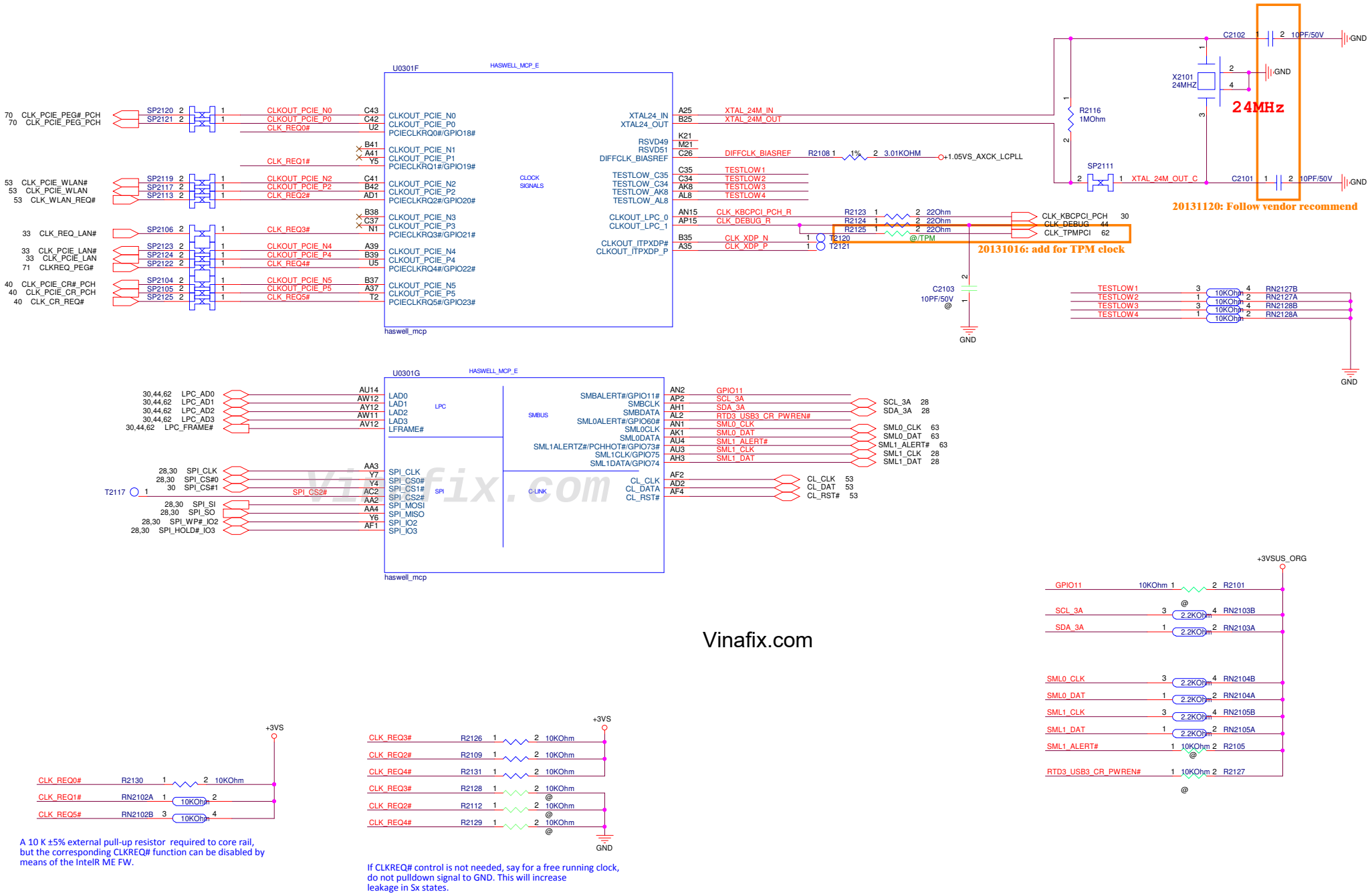
<Core Design>

PEGATRON Title : PCH(1)_SATA,IHDA,RTC

BG1/HW7 Engineer: Fenix Chen

Size: Custom | Project Name: CAS(C)UG | Rev: 1.0

Date: Sunday, December 22, 2013 | Sheet 20 of 103



<Core Design>

PEGATRON

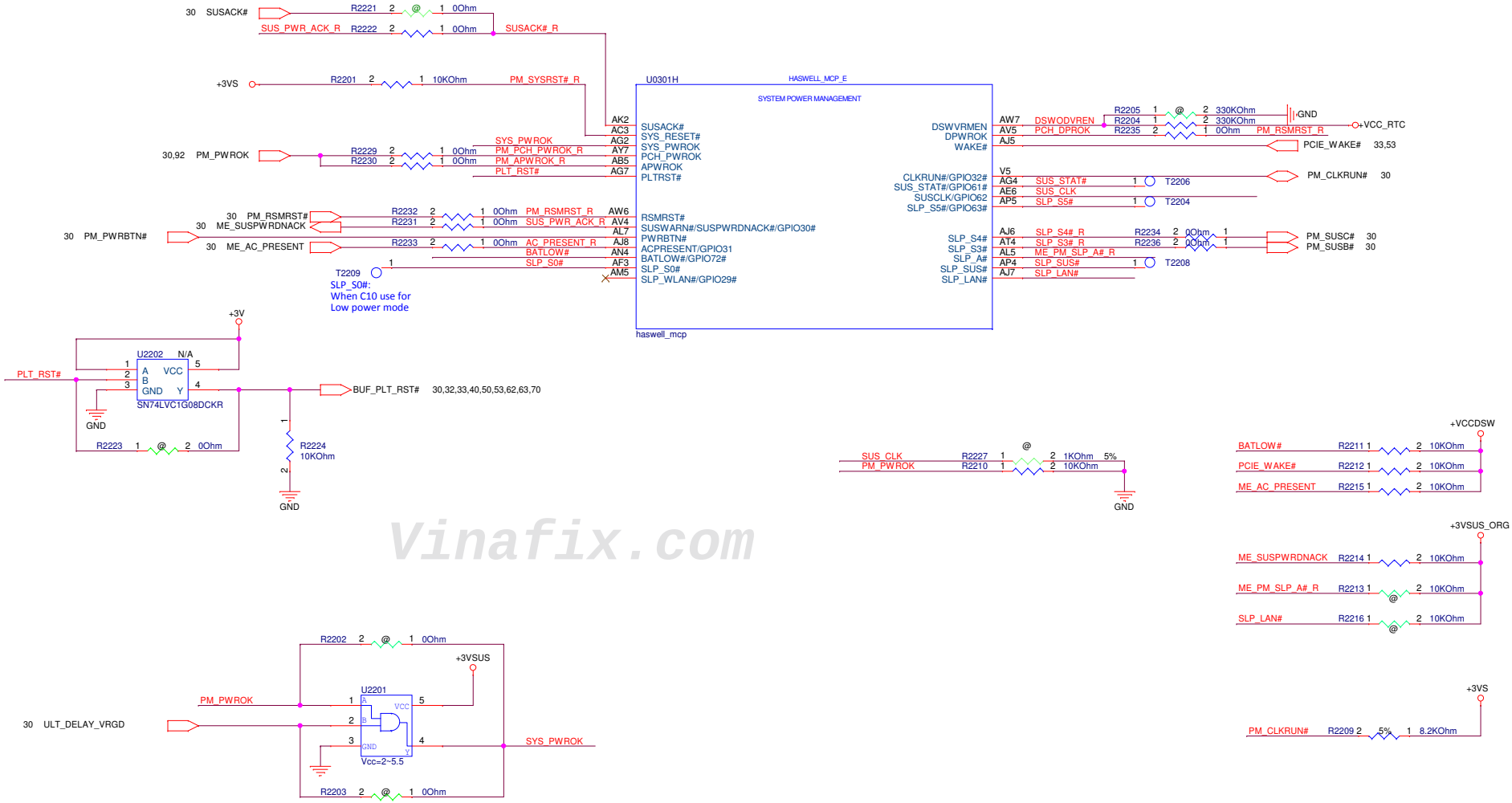
Title : PCH(2)_PCIE,CLK,SME

BG1/HW7

Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 21 of 103



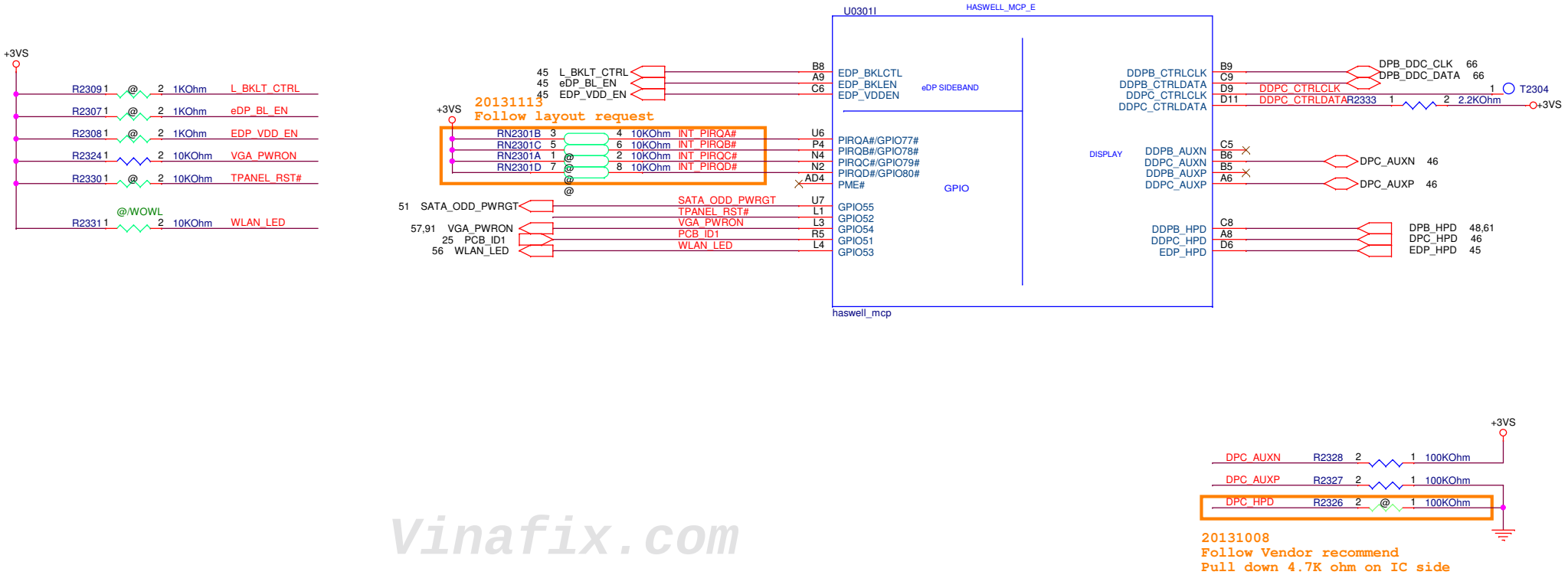
<Core Design>

PEGATRON Title : PCH(3)_FDI,DMI,SYS P

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 22 of 103



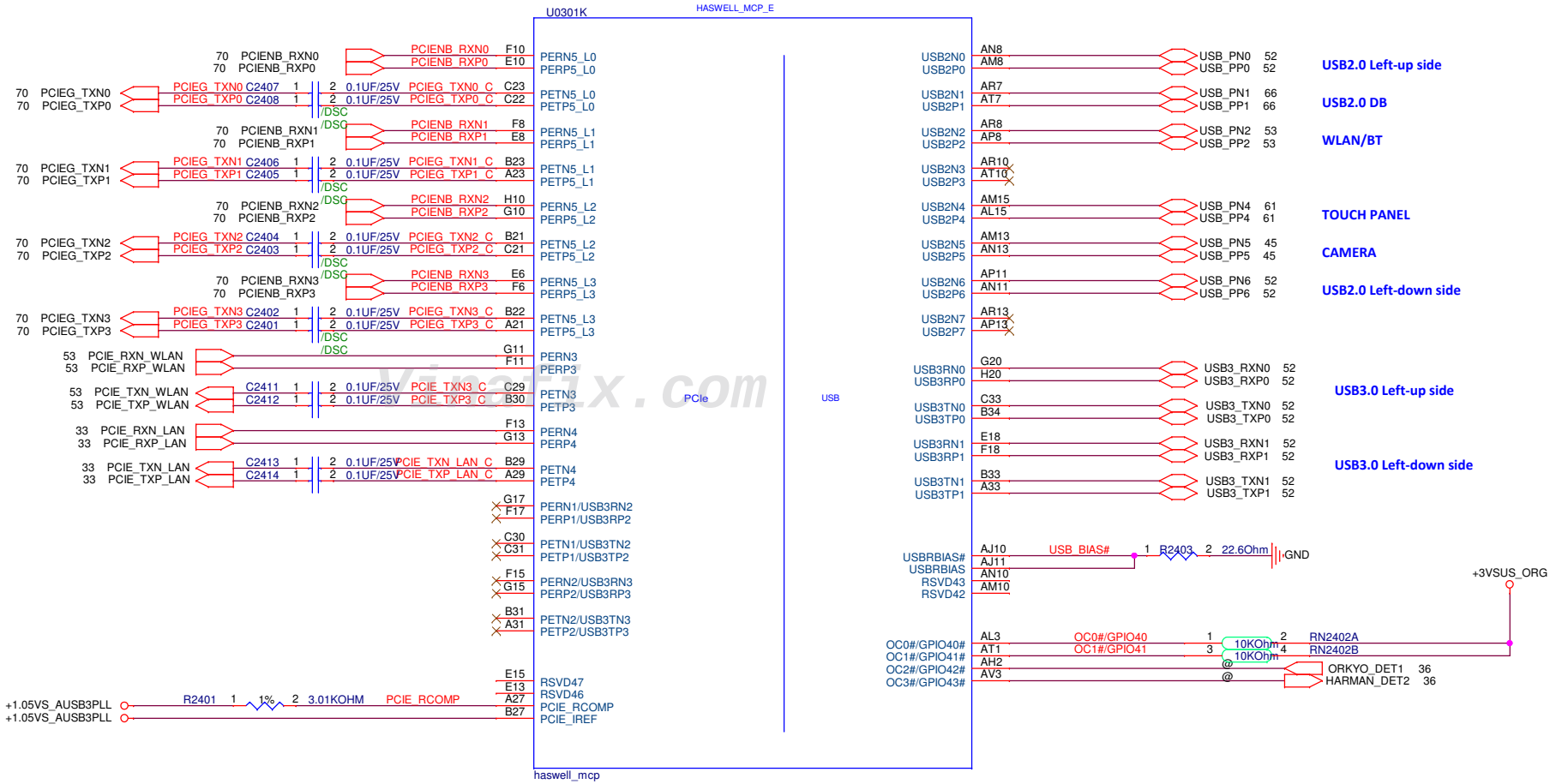
<Core Design>

PEGATRON Title : PCH(4)_DP,LVDS,CRT

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
B	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 23 of 103



<Core Design>

PEGATRON Title : PCH(5)_PCI,NVRAM,USB

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

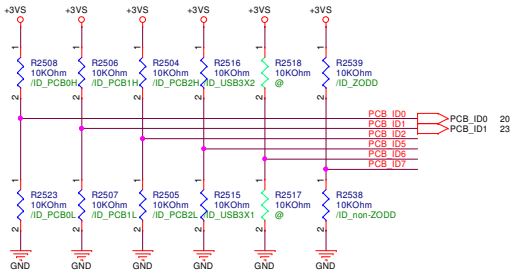
Date: Sunday, December 22, 2013 Sheet 24 of 103

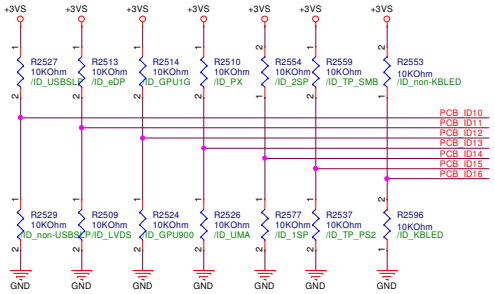
BIOS Rev. SKU

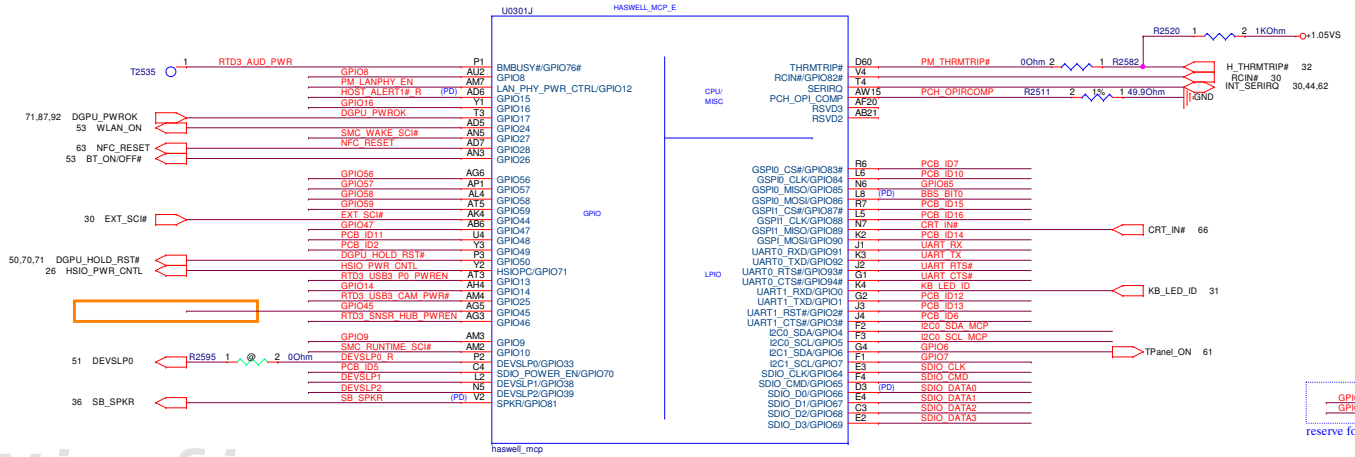
ID2	ID1	ID0	PCB Rev.
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R2.0
0	1	1	R2.1
1	0	0	TBD
1	0	1	TBD
1	1	0	TBD
1	1	1	TBD

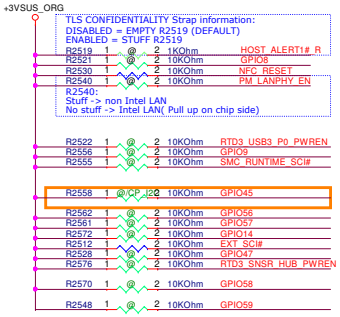
un-used	un-used	CA W/O		un-used	CA W/O					
~~PCB_ID3~~	~~PCB_ID4~~	PCB_ID5	PCB_ID6	PCB_ID7	~~PCB_ID8~~	PCB_ID9	PCB_ID10	PCB_ID11	PCB_ID12	PCB_ID13
~~1: Standard~~	~~1: Premium~~	1:USB3.0*2	1: HDMI	1: Zero_ODD	~~1: PX_UMA~~	1: S&M	1: S&C	1: eDP	1: VRAM 1GHz	1: PX W/NON-IL
~~0: Entry~~	~~0: Mainstream~~	0:USB3.0*1	0: No HDMI	0: Non Zero_ODD	~~0: DSC~~	0: NoS&M	0: No S&C	0: LVDS	0: VRAM 900M	0: UMA W/IL

PCB_ID14	PCB_ID15	PCB_ID16
1: 2 SPIN	1: PS2+SMB+I2C	1: Non-KB_LED
0: 1 SPIN	0: PS2	0: KB_LED



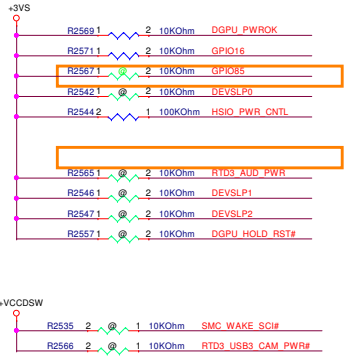






20131128: Changed

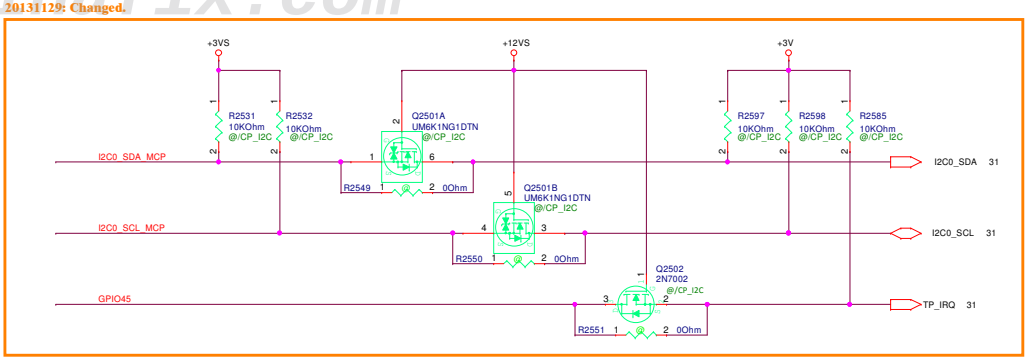
GPIO need to pull high to power with 10Kohm if unused

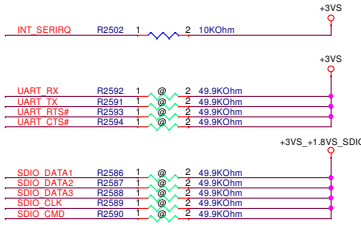


20131011: PCB ID not-stuff Sleep&Music (VG only)

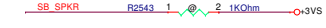
20131011: remove RTD3_SATA1_PWR# Spindle (CA only)

20131129: Changed.



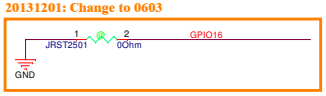


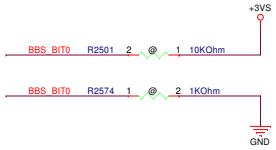
reserve for Audio De-Pop solution

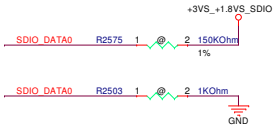


20131003: Follow UMA and reserver it.

20131201: Change to 0603







<Core Design>

PEGATRON Title : PCH(6)_CPU,GPIO,MISC

BG1/HW7 Engineer: Fenix Chen

Size: Custom | Project Name: CAS(C)UG | Rev: 1.0

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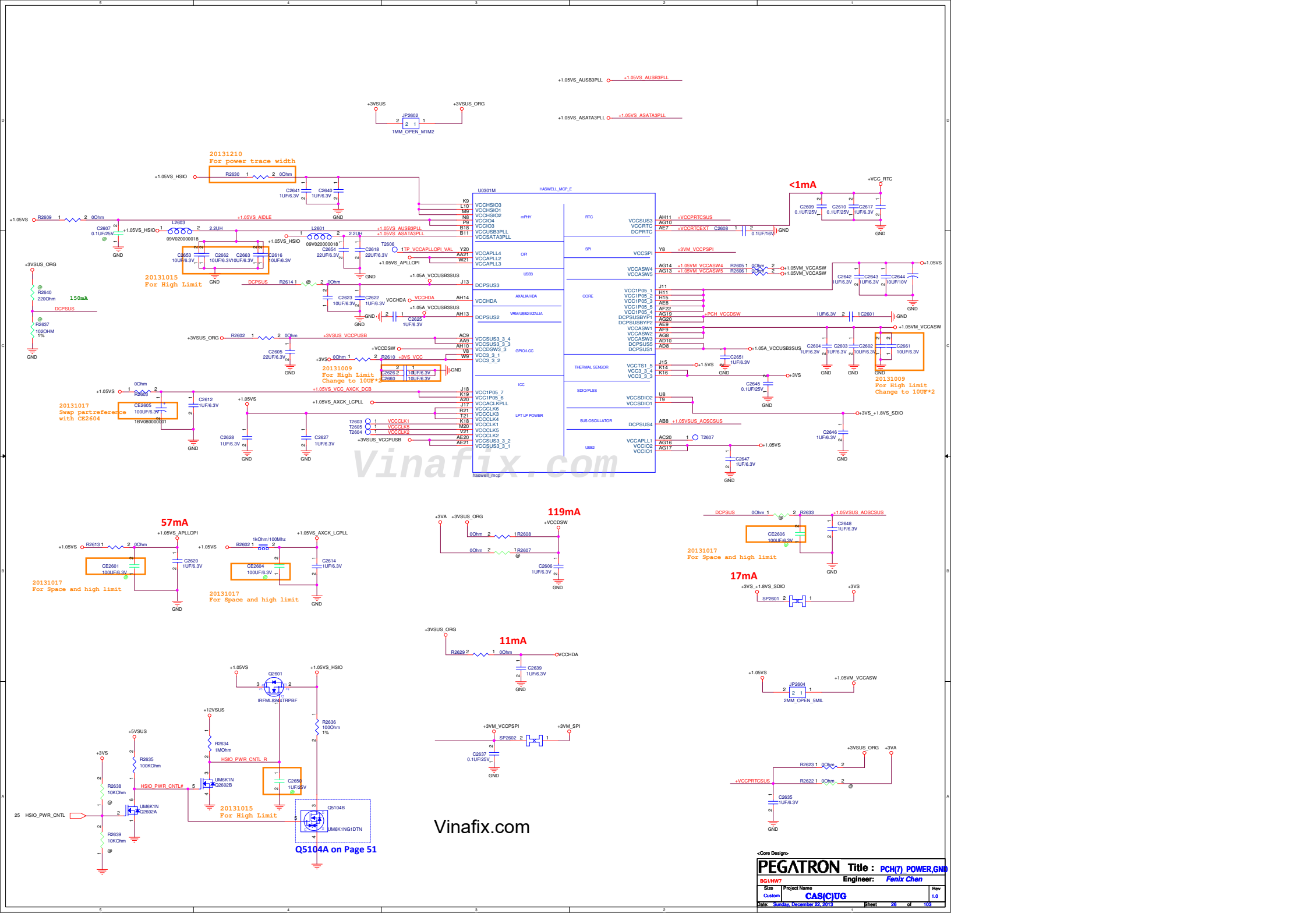
20131210
For power trace width
<1mA
20131015
For High Limit
20131009
For High Limit
Change to 10UF*2
20131017
Swap partreference
with CE2604
57mA
20131017
For Space and high limit
119mA
17mA
11mA
20131015
For High Limit
Q5104A on Page 51
Vinafix.com
Vinafix.com
<Core Design>
PEGATRON
Title : PCH(7)_POWER,GND
Engineer: Fenix Chen
BG1/HW7
Size: Custom
Project Name: CAS(C)UG
Rev: 1.0
Date: Sunday, December 22, 2013
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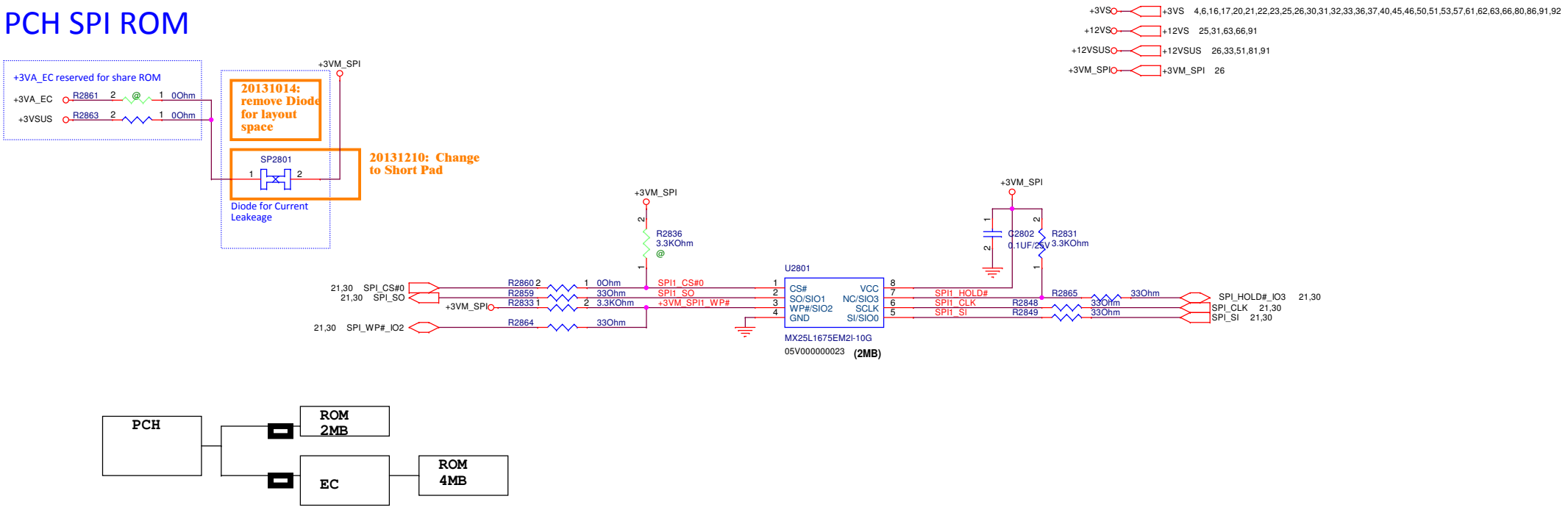
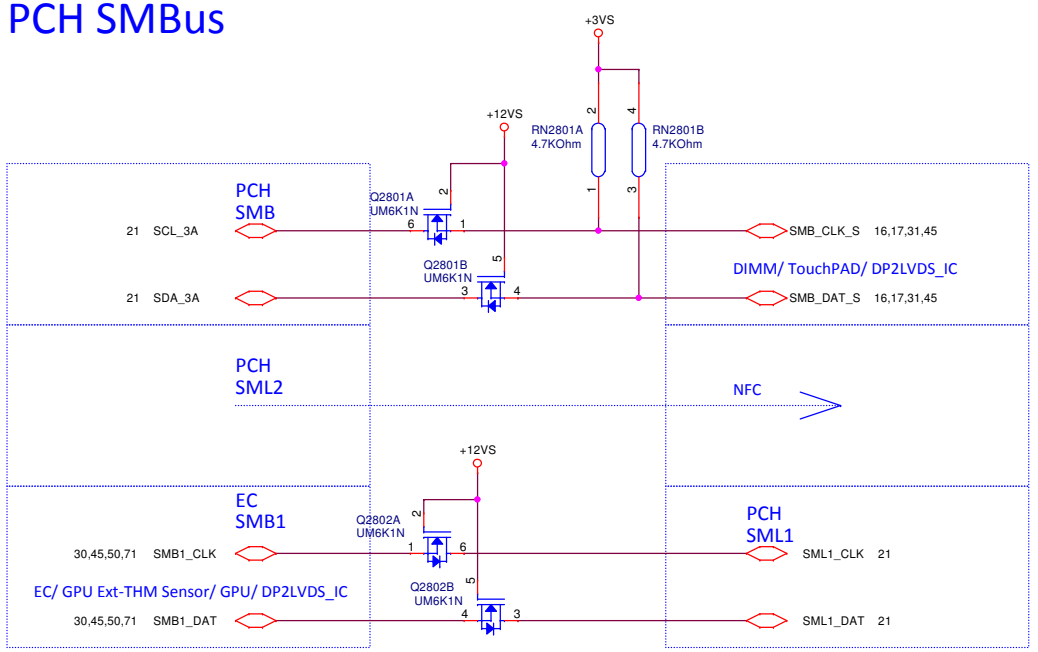
<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 27 of 103	

PCH SPI ROM



PCH SMBus



<Core Design>

PEGATRON Title : PCH(9)_SPI,SMB

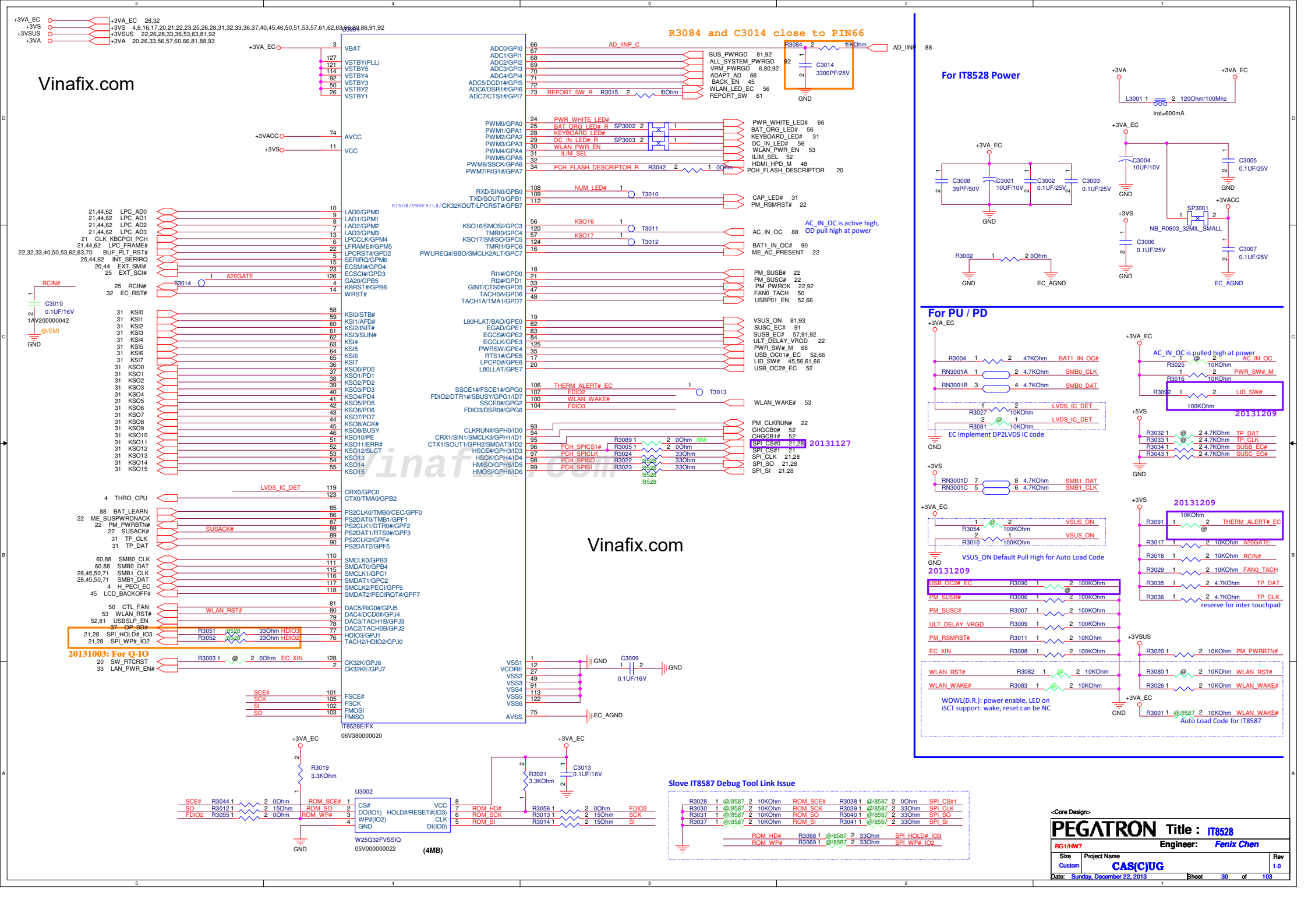
BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

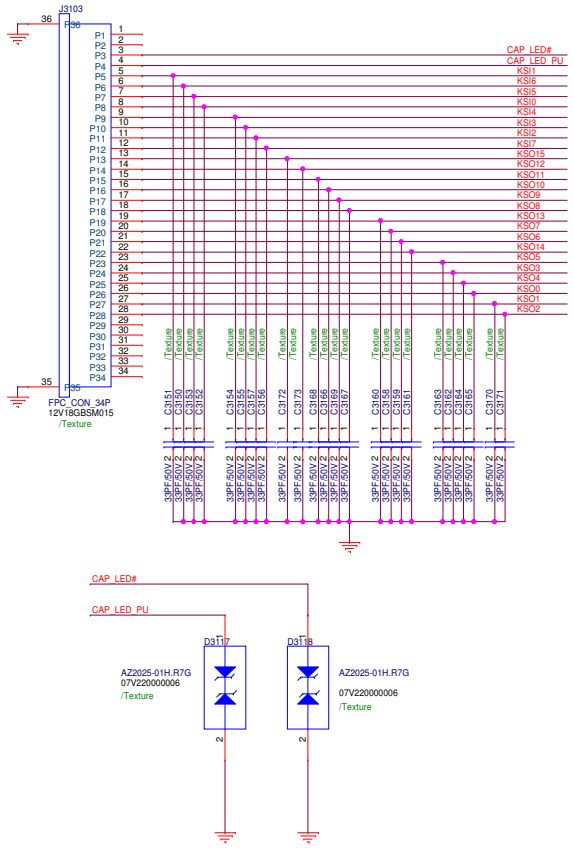
Date: Sunday, December 22, 2013 Sheet 28 of 103

<Core Design>

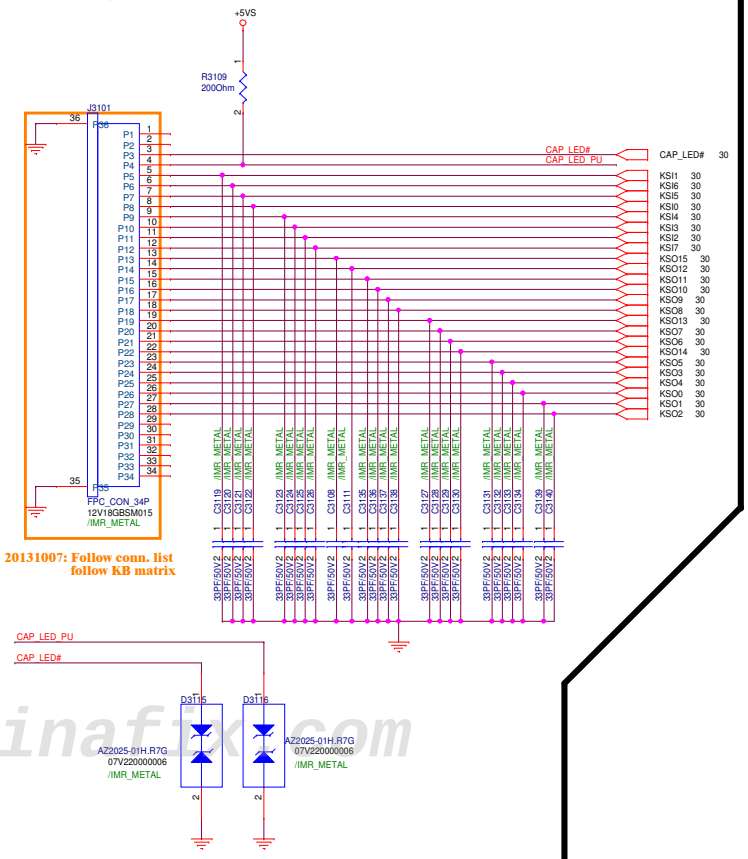
Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 29 of 103	


R3084 and C3014 close to PIN66
Vinafix.com
For IT8528 Power
For PU / PD
AC_IN_OC is active high, OD pull high at power
AC_IN_OC is pulled high at power
EC implement DP2LVDS IC code
VSUS_ON Default Pull High for Auto Load Code
20131209
20131127
20131003: For Q-IO
Slove IT8587 Debug Tool Link Issue
WOWL(D.R.): power enable, LED on iSCT support: wake, reset can be NC
Auto Load Code for IT8587
reserve for inter touchpad
IT8528E/FX
06V380000020
W25Q32FVSSIQ
05V000000022
(4MB)
PEGATRON
Title : IT8528
Engineer: Fenix Chen
BG1/HW7
Project Name CAS(C)UG
Rev 1.0
Date: Sunday, December 22, 2013
Sheet 30 of 103

TOP Keyboard (for Texture)

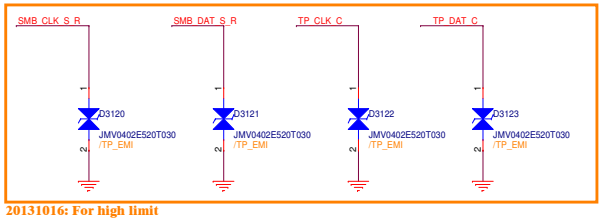


BOT Keyboard(for IMR/Metal)



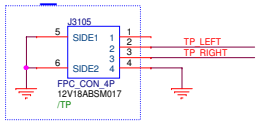
20131007: Follow conn. list
follow KB matrix

Touch_PAD_TOP (for Texture)

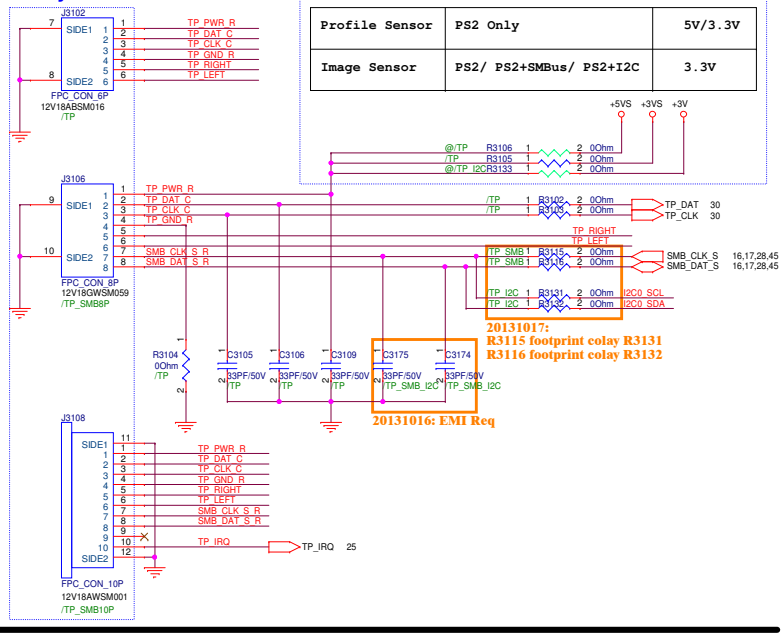


20131016: For high limit

TP_BD



Colay

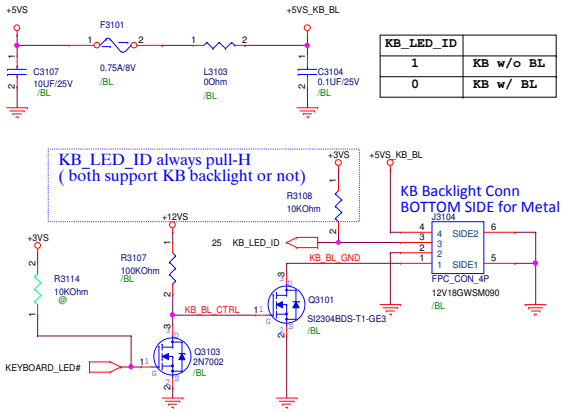


Profile Sensor	PS2 Only	5V/3.3V
Image Sensor	PS2/ PS2+SMBus/ PS2+I2C	3.3V

20131017:
R3115 footprint colay R3131
R3116 footprint colay R3132

20131016: EMI Req

Keyboard LED_BOT (for IMR/Meatl)

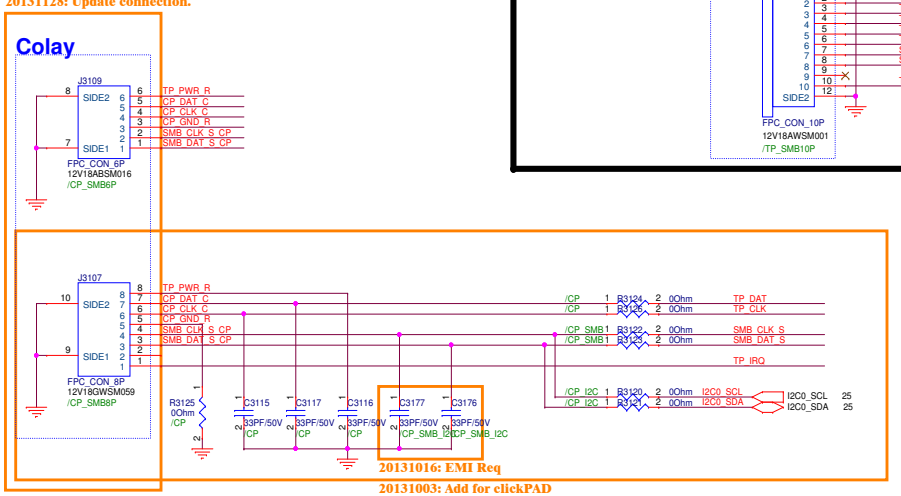


KB_LED_ID	
1	KB w/o BL
0	KB w/ BL

Click_PAD_BOT (for IMR/Meatl)

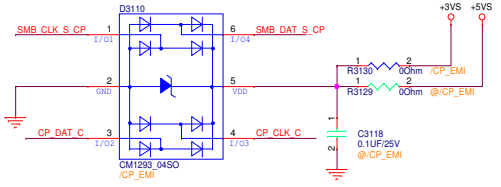
20131128: Update connection.

Colay

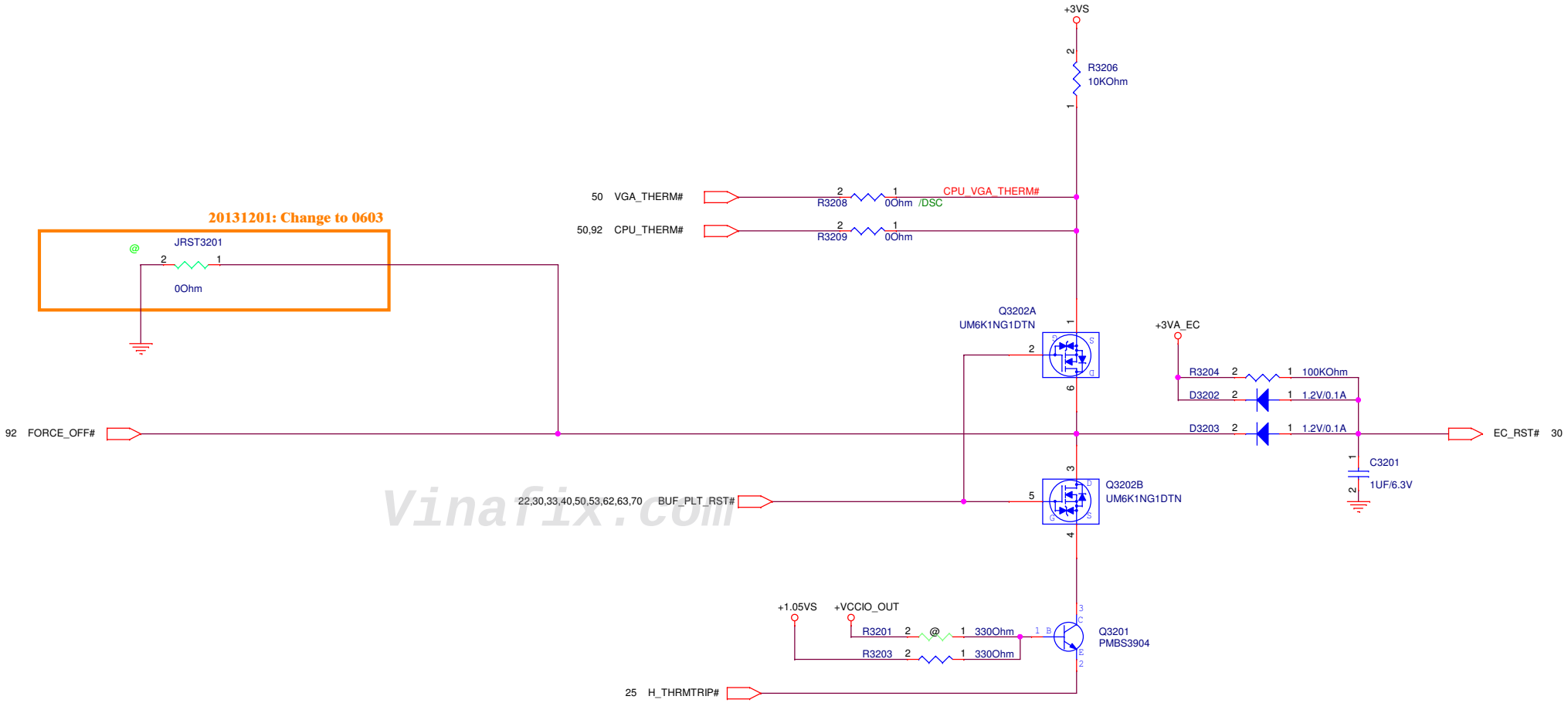


20131016: EMI Req

20131003: Add for clickPAD



PEGATRON	Title : KB/ TP	
BG1/HW7	Engineer: Fenix Chen	
Size: Custom	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 31 of 103	



<Core Design>

PEGATRON Title : RST_Reset Circuit

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
B	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 32 of 103

+3VS +3VS 4,6,16,17,20,21,22,23,25,26,28,30,31,32,36,37,40,45,46,50,51,53,57,61,62,63,66,80,86,91,92

+3VSUS +3VSUS 22,26,28,30,36,53,63,81,92

U3301A

34 LAN_MDI0P
34 LAN_MDI0N
1 MDIP0
2 MDIN0

34 LAN_MDI1P
34 LAN_MDI1N
4 MDIP1
5 MDIN1

34 LAN_MDI2P
34 LAN_MDI2N
6 MDIP2
7 MDIN2

34 LAN_MDI3P
34 LAN_MDI3N
9 MDIP3
10 MDIN3

11 AVDD33_1
32 AVDD33_2 +3VSUS_LAN
23 VDDREG +3VSUS_LAN

24 REGOUT REGOUT10

3 AVDD10_0
8 AVDD10_1
30 AVDD10_2 VDD10

22 DVDD10 VDD10

21 CLK_REQ_LAN#

Host side had Pull-H

+3VS R3301 1 2 10KOhm @ 12 CLKREQB

PCIE_WAKE# LAN

+3VSUS_LAN R3303 2 @ 1 10KOhm 21 LANWAKEB

Host side had Pull-H

20 ISOLATEB

+3VS
R3306 1KOhm
ISOLATE
R3307 15KOhm
GND

27 LED0
26 LED1/GPO
25 LED2

22,30,32,40,50,53,62,63,70 BUF_PLT_RST#

19 PERSTB

R3302 close to pin31

31 RSET

R3302 2.49KOhm 1%
C3327 0.1UF/25V @
C3328 0.1UF/25V
GND GND GND

33 GND

GND

20131011
C3327&C3328
For ESD request
Close to Chip

13 HSIP PCIE_TXP_LAN 24
14 HSIN PCIE_TXN_LAN 24

17 HSOP PCIE_RXP_LAN C3302 1 2 0.1UF/16V PCIE_RXP_LAN 24
18 HSON PCIE_RXN_LAN C3301 1 2 0.1UF/16V PCIE_RXN_LAN 24

C3301and C3302 Close to
U3301 pin17, pin18

15 REFCLK_P CLK_PCIE_LAN 21
16 REFCLK_N CLK_PCIE_LAN# 21

28 CKXTAL1 XTAL1
29 CKXTAL2 XTAL2

RTL8111G-CG
02V0J0000024

U3301B
34 GND1
35 GND2
36 GND3
37 GND4
38 GND5
39 GND6
40 GND7
41 GND8
GND
RTL8111G-CG
02V0J0000024

X3302 25MHZ
XTAL1 XTAL2
C3304 10PF/50V
C3303 10PF/50V
GND GND GND

Width > 60 mils
200 mils
C3306 to C3312 Close To U3301 (length < 200 mil)
200 mils
VDD10

REGOUT10 R3309 2 1 /Giga 0Ohm

C3306 close to pins-- 24
C3307 close to pins-- 3
C3308 close to pins-- 8
C3309 close to pins-- 22
C3310 close to pins-- 30

C3306 C3307 C3308 C3309 C3310 C3312 C3311
0.1UF/16V /Giga
1UF/6.3V
GND

RTL8111G: C3311&C3312 close to pins-- 22
RTL8106E: C3311&C3312 close to pins-- 30

RTL8111G(S): C3316 to C3319 close to pins-- 11, 32
RTL8106E: C3316 to C3317 close to pins-- 23, 32

+3VSUS_LAN
C3316 0.1UF/16V
C3317 0.1UF/16V
C3318 4.7UF/6.3V /Giga
C3319 4.7UF/6.3V /Giga
GND

For RTL8111G surge improvement

G3 to S5 wake on LAN disable

+3VSUS 40 mil R3304 1 2 /G3_WOL 0Ohm vx_r0805_h24_small 40 mil +3VSUS_LAN

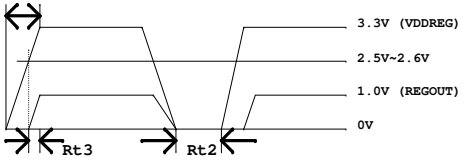
SI2304BDS-T1-GE3
Q3301
@/NON_G3_WOL

+12VSUS
+3VA
R3320 100KOhm @/NON_G3_WOL
R3321 100KOhm @/NON_G3_WOL
LAN_PWR_EN
PCIE_WAKE# LAN
UM6K1N Q3302A @/NON_G3_WOL
R3322 0Ohm /G3_WOL
Q3302B UM6K1N @/NON_G3_WOL
C3350 0.1UF/25V @
30 LAN_PWR_EN#
PCIE_WAKE# 22,53

G3->S5 : High
S5 ->S0 :Low

Power sequence

3.3V rising time must be
more than 0.5ms and less than 100ms.



	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

<Core Design>

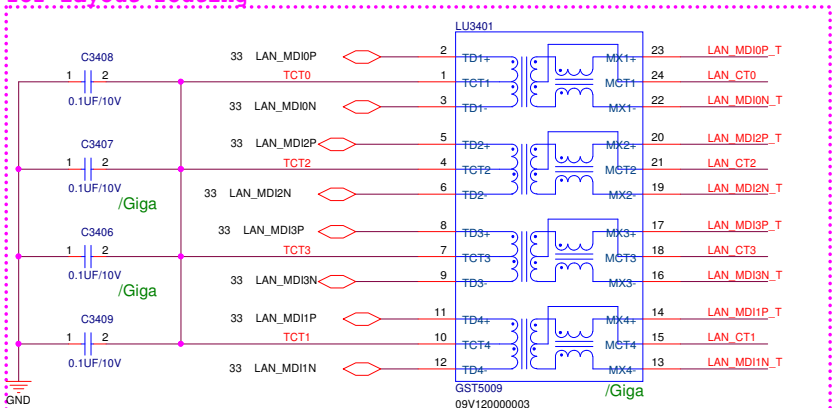
PEGATRON Title : Realtek RTL8111G

BG1/HW7 Engineer: Fenix Chen

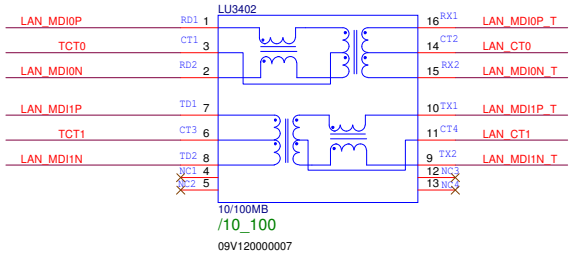
Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 33 of 103

for layout routing



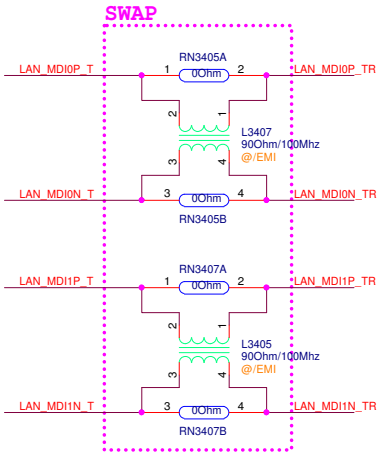
Transformer(1G)
close J3401

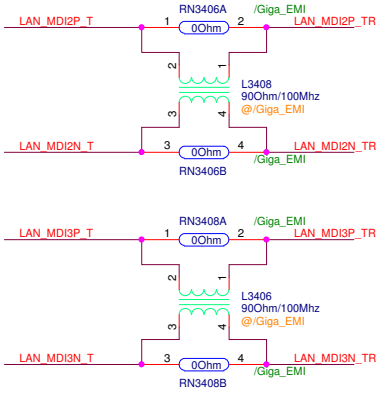


Transformer(10/100)
close J3401

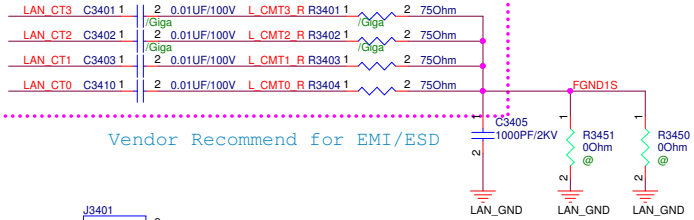
Vinafix.com

SWAP



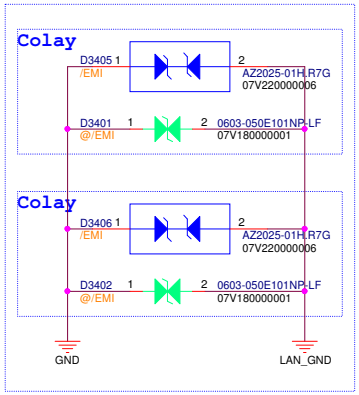


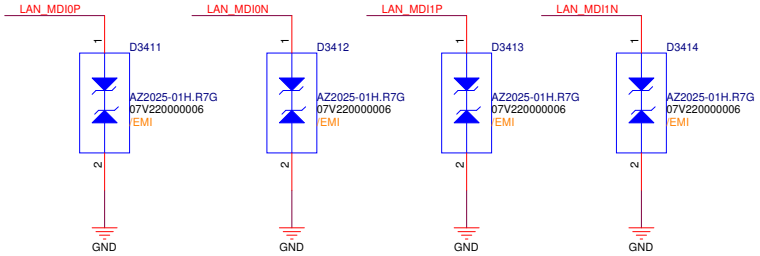
20131014: remove 75 Ohm pull-L for
un-used L_CMT2/3 in 10/100 cable

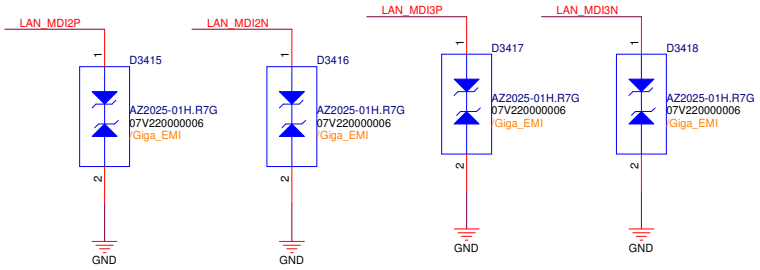


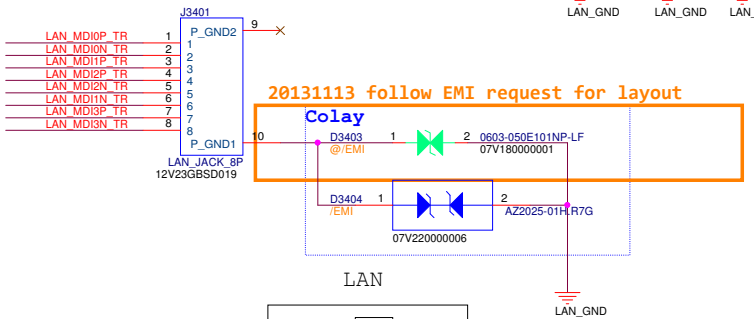
Vendor Recommend for EMI/ESD

Place near chassis GND

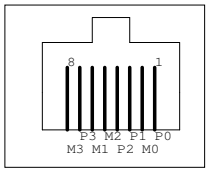








LAN



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PEGATRON

Title : RJ45

BG1/HW7

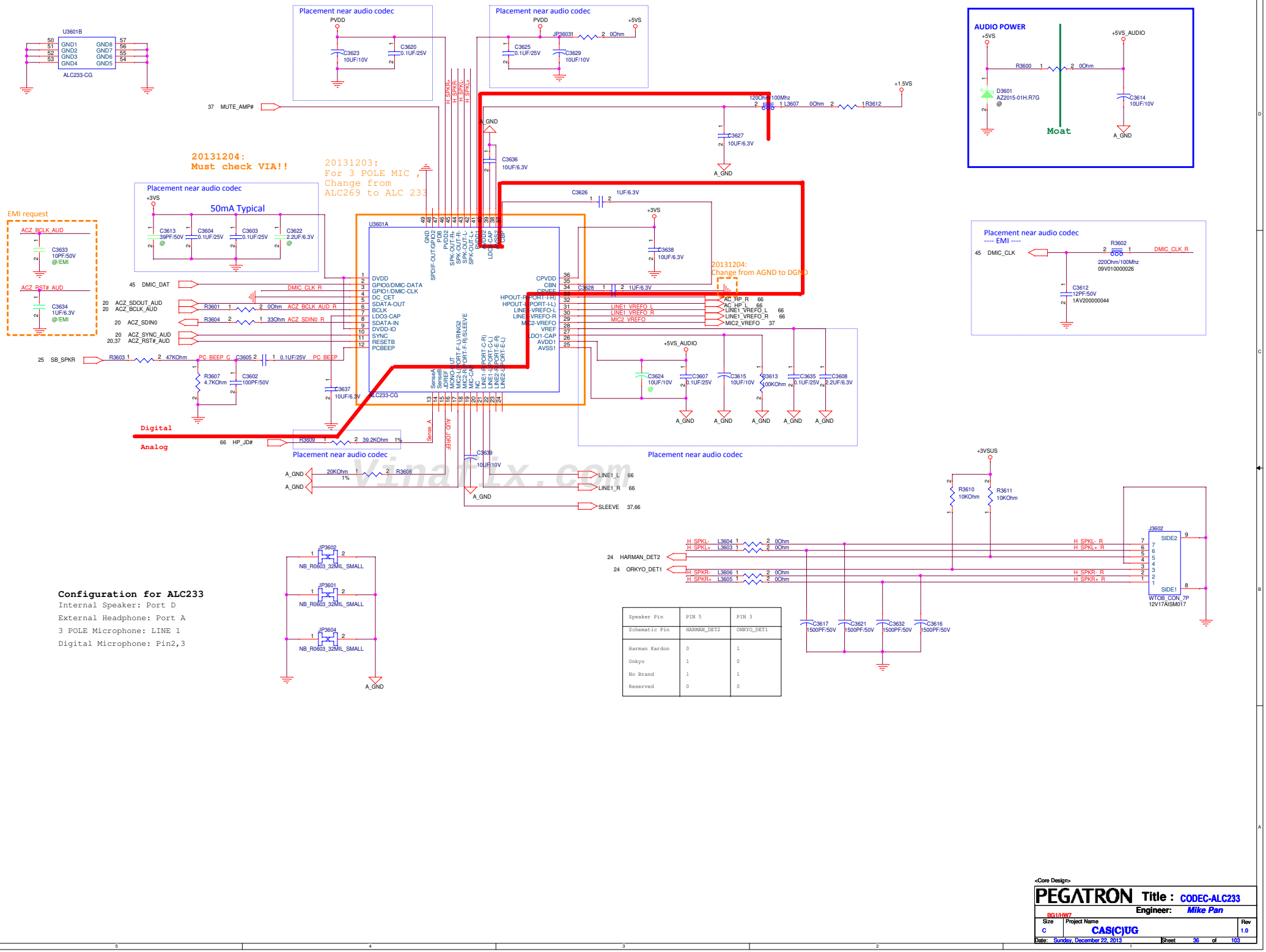
Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0
	P/N	

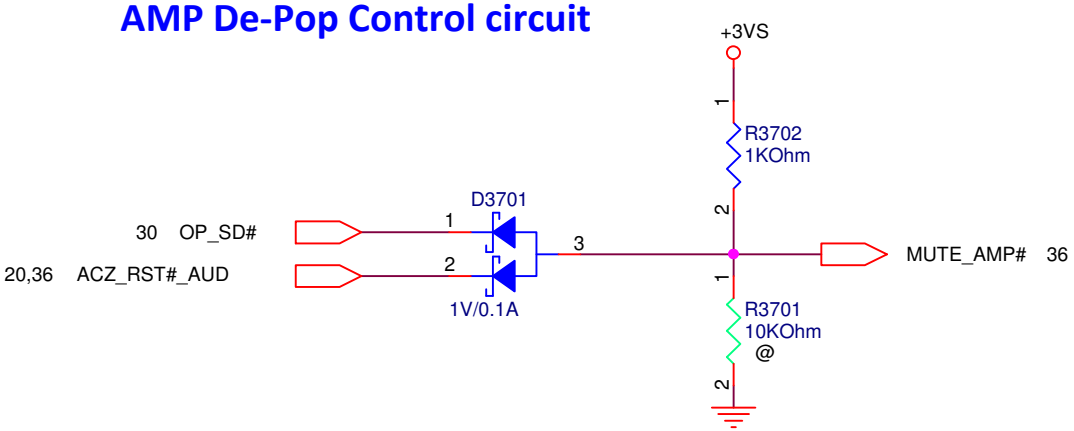
Date: Sunday, December 22, 2013 Sheet 34 of 103

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 35 of 103	


U3601B
ALC233-CG
Placement near audio codec
PVDD
C3623 10UF/10V
C3620 0.1UF/25V
JP36031
C3625 0.1UF/25V
C3629 10UF/10V
+5VS
AUDIO POWER
+5VS_AUDIO
R3600 0Ohm
D3601 AZ2015-01H.R7G
C3614 10UF/10V
Moat
A_GND
37 MUTE_AMP#
+1.5VS
120Ohm/100Mhz
L3607 0Ohm
R3612
C3627 10UF/6.3V
C3636 10UF/6.3V
20131204:
Must check VIA!!
20131203:
For 3 POLE MIC ,
Change from
ALC269 to ALC 233
Placement near audio codec
50mA Typical
+3VS
C3613 39PF/50V @
C3604 0.1UF/25V
C3603 0.1UF/25V
C3622 2.2UF/6.3V @
EMI request
ACZ_BCLK_AUD
C3633 10PF/50V @/EMI
ACZ_RST#_AUD
C3634 1UF/6.3V @/EMI
U3601A
ALC233-CG
C3626 1UF/6.3V
C3638 10UF/6.3V
20131204:
Change from AGND to DGND
45 DMIC_DAT
DMIC_CLK_R
20 ACZ_SDOUT_AUD
20 ACZ_BCLK_AUD
R3601 0Ohm ACZ_BCLK_AUD_R
20 ACZ_SDIN0
R3604 33Ohm ACZ_SDIN0_R
20 ACZ_SYNC_AUD
20,37 ACZ_RST#_AUD
25 SB_SPKR
R3603 47KOhm
PC_BEEP_C
C3605 0.1UF/25V
PC_BEEP
R3607 4.7KOhm
C3602 100PF/50V
C3637 10UF/6.3V
Digital
Analog
66 HP_JD#
R3609 39.2KOhm 1%
Placement near audio codec
C3639 10UF/10V
20KOhm 1% R3608
LINE1_L 66
LINE1_R 66
SLEEVE 37,66
AC_HP_R 66
AC_HP_L 66
LINE1_VREFO_L 66
LINE1_VREFO_R 66
MIC2_VREFO 37
LINE1_VREFO_L
LINE1_VREFO_R
MIC2_VREFO
+5VS_AUDIO
C3624 10UF/10V @
C3607 0.1UF/25V
C3615 10UF/10V
R3613 100KOhm
C3635 0.1UF/25V
C3608 2.2UF/6.3V
Placement near audio codec
---- EMI ----
45 DMIC_CLK
R3602 220Ohm/100Mhz 09V010000026
DMIC_CLK_R
C3612 12PF/50V 1AV200000044
+3VSUS
R3610 10KOhm
R3611 10KOhm
H_SPKL- L3604 0Ohm
H_SPKL+ L3603 0Ohm
H_SPKR- L3606 0Ohm
H_SPKR+ L3605 0Ohm
24 HARMAN_DET2
24 ORKYO_DET1
H_SPKL- R
H_SPKL+ R
H_SPKR- R
H_SPKR+ R
J3602
SIDE2
SIDE1
WTOB_CON_7P
12V17AISM017
C3617 1500PF/50V
C3621 1500PF/50V
C3632 1500PF/50V
C3616 1500PF/50V
JP3602 NB_R0603_32MIL_SMALL
JP3601 NB_R0603_32MIL_SMALL
JP3604 NB_R0603_32MIL_SMALL
A_GND
Configuration for ALC233
Internal Speaker: Port D
External Headphone: Port A
3 POLE Microphone: LINE 1
Digital Microphone: Pin2,3
Speaker Pin | PIN 5 | PIN 3
Schematic Pin | HARMAN_DET2 | ONKYO_DET1
Harman Kardon | 0 | 1
Onkyo | 1 | 0
No Brand | 1 | 1
Reserved | 0 | 0
<Core Design>
PEGATRON
Title : CODEC-ALC233
Engineer: Mike Pan
BG1/HW7
Size C
Project Name CAS(C)UG
Rev 1.0
Date: Sunday, December 22, 2013
Sheet 36 of 103

AMP De-Pop Control circuit



20131203: For 3 Pole MIC

<Core Design>

PEGATRON	Title : COMBO_JACK	
BG1/HW7	Engineer: Mike Pan	
Size: A	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 37 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 38 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 39 of 103	

Power Source

+3VS — JP4001 (1MM_OPEN_M1M2) — +3VS_CR

trace width 60mils — trace width 60mils

From System's PCIE interface

20	PCIE_TXP_CR	PCIE_TXP_CR
20	PCIE_TXN_CR	PCIE_TXN_CR
20	PCIE_RXP_CR	PCIE_RXP_CR
20	PCIE_RXN_CR	PCIE_RXN_CR
21	CLK_PCIE_CR_PCH	CLK_PCIE_CR_PCH
21	CLK_PCIE_CR#_PCH	CLK_PCIE_CR#_PCH
21	CLK_CR_REQ#	CLK_CR_REQ#
22,30,32,33,50,53,62,63,70	BUF_PLT_RST#	BUF_PLT_RST#

J4001 SD_SOCKET_13P 12V21GBRM006

SD_CD# SD_D2 SD_D3 SD_CMD SD_CLK_R SD_D0 SD_D1 SD_WP

CARD_DETECT DAT2 CD/DAT3 CMD VSS1 VDD CLK VSS2 DAT0 DAT1 WRITE_PROTECT GND1 NP_NC1 NP_NC2 GND2

SD_CLK — R4004 0Ohm — C4050 2.2PF/50V 1AV200000056 @ — GND

+3VS_CARD

+3VS_CARD — C4011 4.7UF/6.3V Pin 7 — C4012 0.1UF/16V Pin 7 — C4013 0.1UF/16V Pin 9 — R4002 5.1KOhm @

Close to connector

GND

+3VS_CR — R4017 10KOhm — R4015 10KOhm @

20131112
Follow new datasheet and remove the PCIE_WAKE#
Set 10K PU

BUF_PLT_RST# CLK_CR_REQ# WAKE# V12 SD_CD#

1108

U4002A

GND NC10 CLKREQ RESETN WAKEN PLLV12 MSINS SDCDN NC9 NC8

NC1 PLLV33 REFCLKP REFCLKM REXT RXM RXP TXP TXM V12

NC7 NC6 NC5 OPT0 OPT1 OPT2 SDWP_MSBS SDD1_MSD1 SDD0_MSD0 SDCLK

+3VS_CR — R4016 191Ohm — GND

CLK_PCIE_CR_PCH CLK_PCIE_CR#_PCH PCIE_TXN_CR PCIE_TXP_CR PCIE_RXP_CR PCIE_RXP_CR_C PCIE_RXN_CR PCIE_RXN_CR_C V12

C4002 0.1UF/16V C4001 0.1UF/16V

20131008
Follow Vendor Check

SVID/SSID	R4018	R4019	R4020	
1179/F940(VG20)	@	@	N/A	
1179/F900(CA10)	@	N/A	@	(Default)

CR_SID0 CR_SID1 CR_SID2 — R4018 R4019 R4020 10KOhm

SD_WP SD_D1 SD_D0 SD_CLK — GND

NC2 NC3 NC4 VIO1 AVDD VCPD SDD2_MSCLK SDD3_MSD3 SDDMD_MSD2 VIO2

V33_18 +3VS_CR +3VS_CARD SD_D2 SD_D3 SD_CMD V33_18

AU6601A72-MCF-GR 02V0K0000009

U4002B GND1 GND2 GND3 GND4 AU6601A72-MCF-GR 02V0K0000009

20131017: Refresh Parts for 4vias

+3VS_CR — C4006 4.7UF/6.3V — C4005 0.1UF/16V — GND

V12 — C4007 4.7UF/6.3V — C4008 0.1UF/16V — GND

V33_18 — C4014 4.7UF/6.3V — C4015 0.1UF/16V — GND

+3VS_CARD — C4051 0.1UF/16V — GND

20131118: Close to U4002

PEGATRON Title : AU6601

Engineer:

BG1/HW7

Size	Project Name	Rev
Custom		1.0

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<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
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<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 42 of 103	

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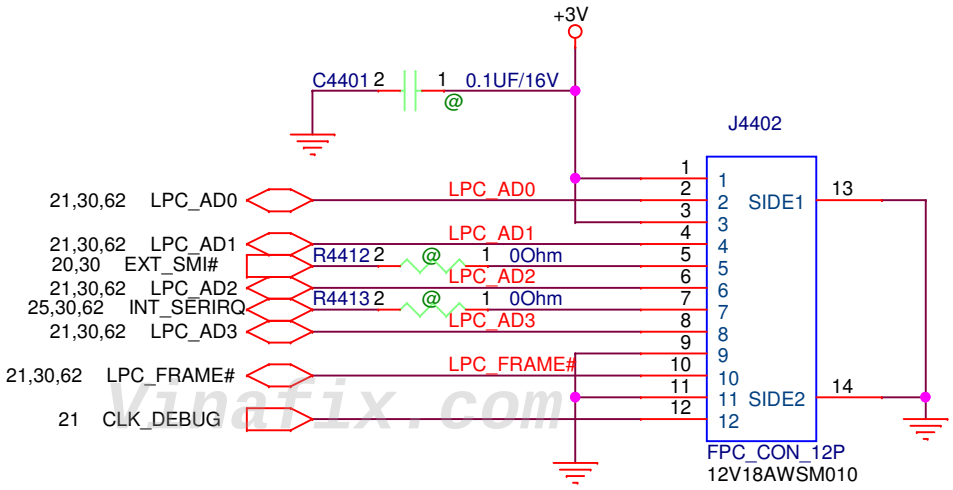
Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 43 of 103	



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PEGATRON

Title : BUG_Debug

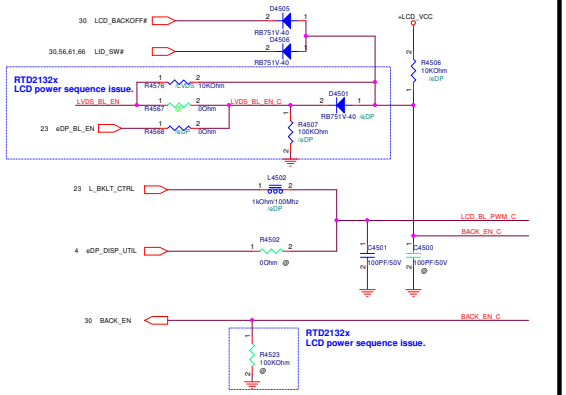
BG1/HW7

Engineer: Fenix Chen

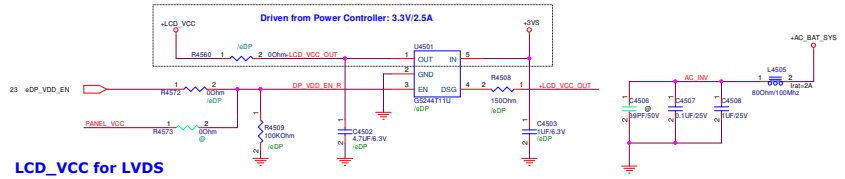
Size	Project Name	Rev
A	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 44 of 103

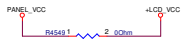
LCD Panel Control



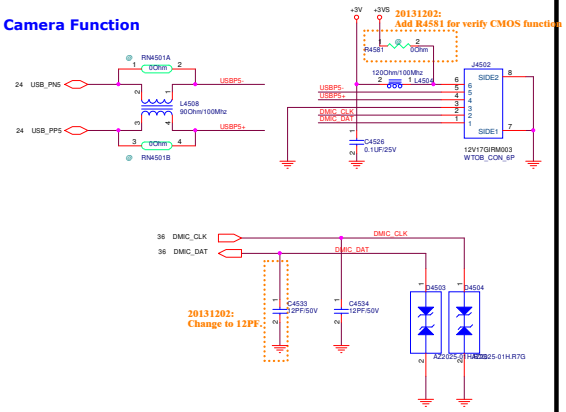
LCD Power Control



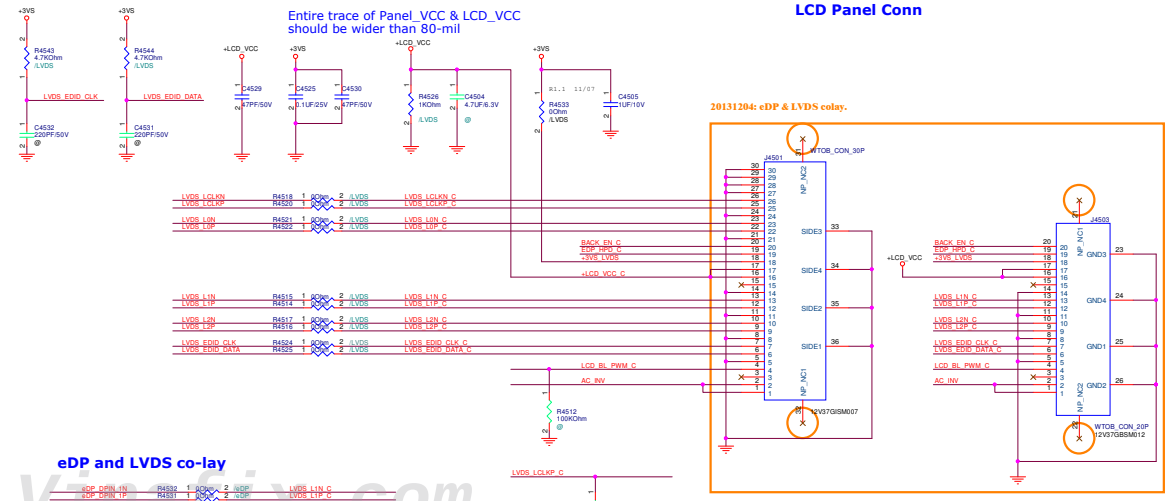
LCD_VCC for LVDS



Camera Function

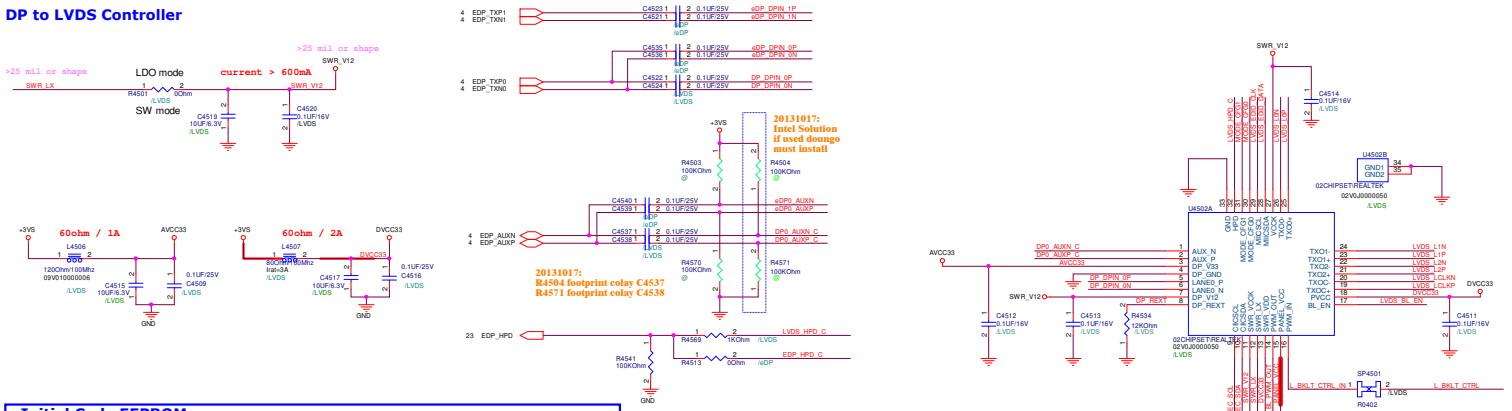


LCD Panel Conn

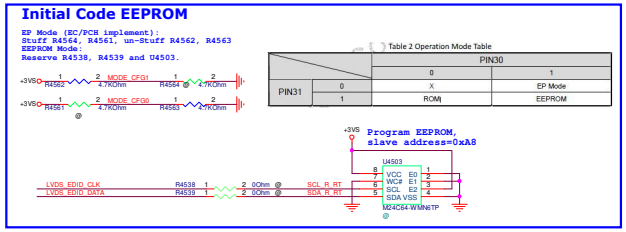


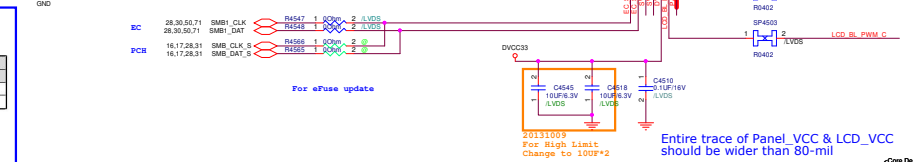
eDP and LVDS co-lay

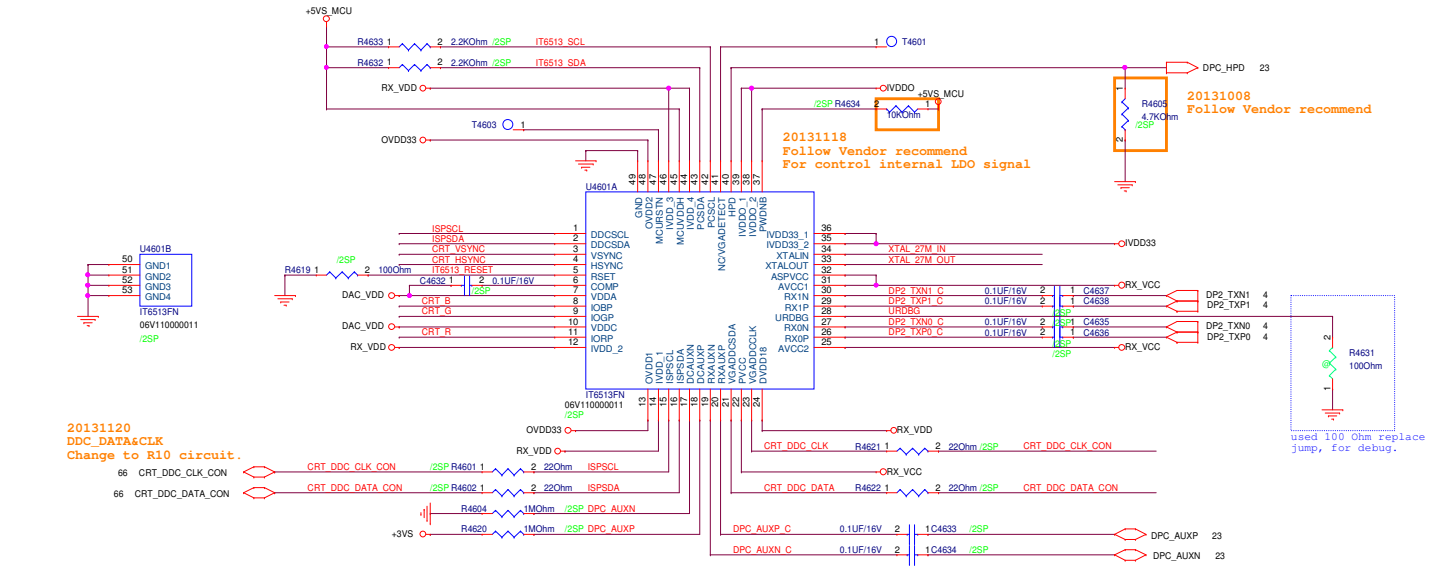
DP to LVDS Controller

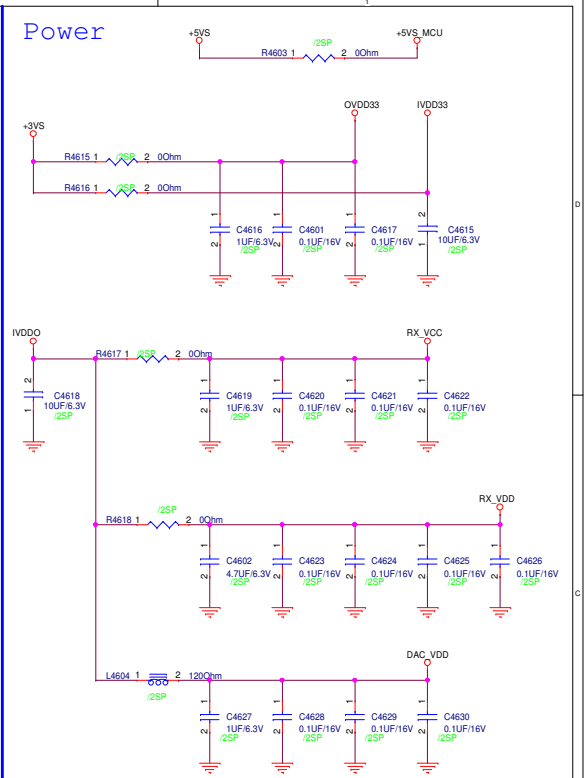


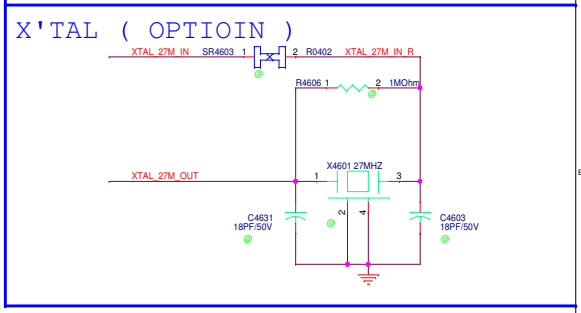
Initial Code EEPROM

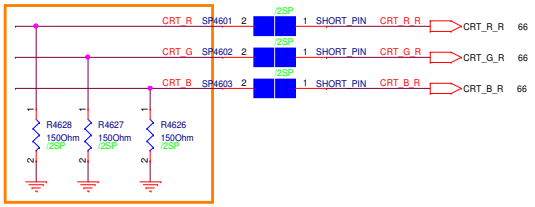


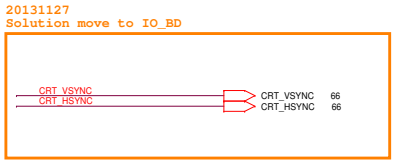












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PEGATRON Title : CRT Output

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
C	CAS(C)UG	1.0

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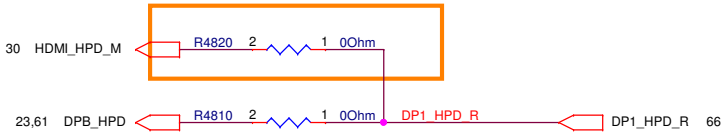
<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 47 of 103	

20131120 For CEC function HPD



<Core Design>

PEGATRON Title : HDMI-4K2K

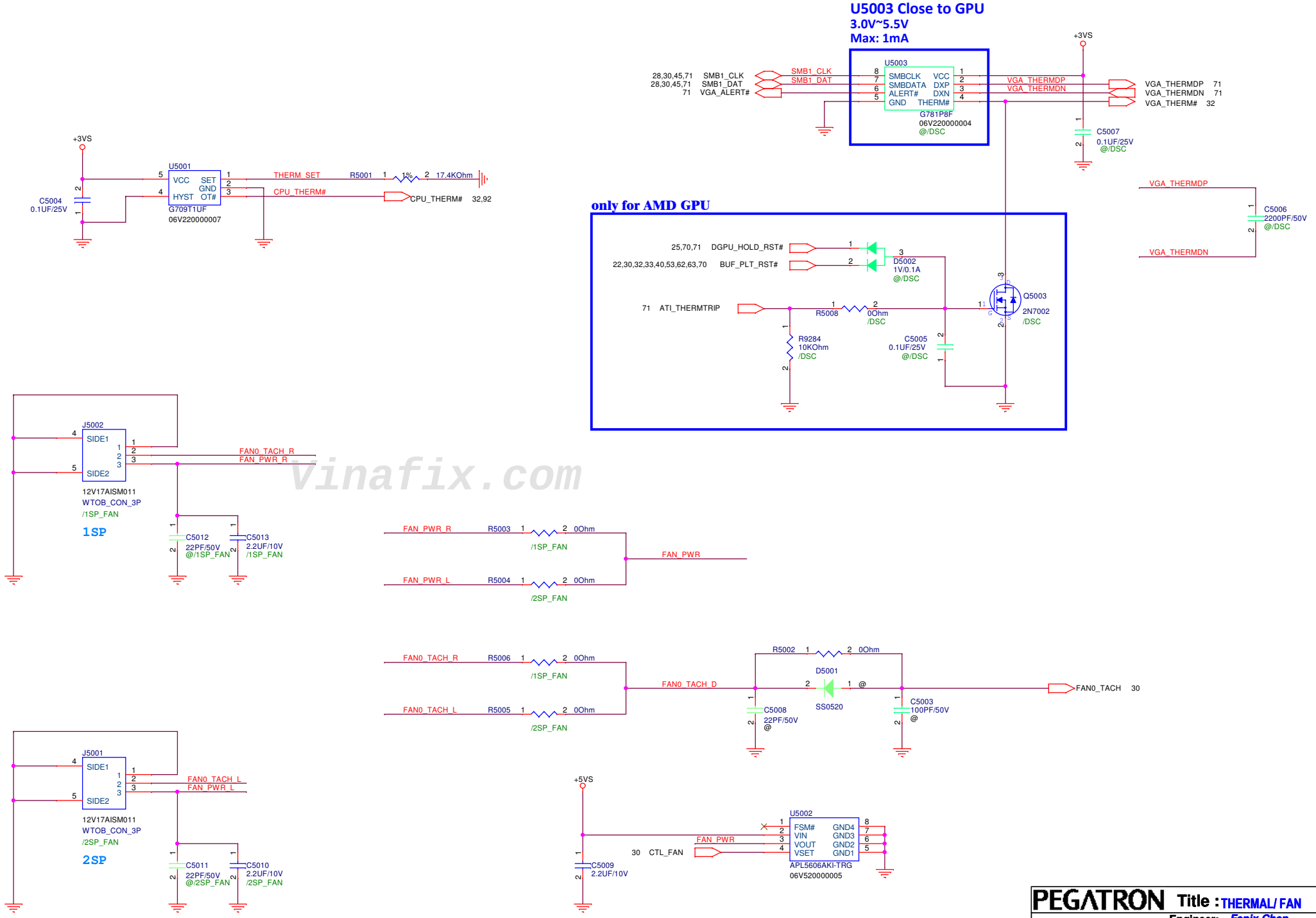
BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
B	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 48 of 103

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 49 of 103	



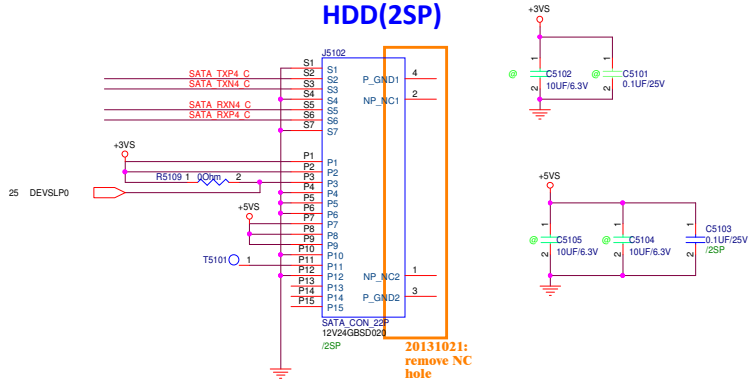
PEGATRON Title : THERMAL/ FAN

BG1/HW7 Engineer: Fenix Chen

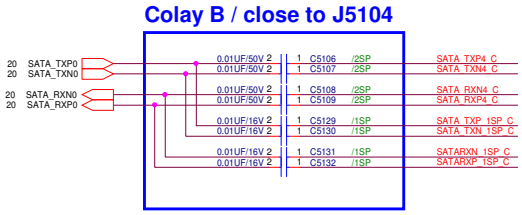
Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 50 of 103

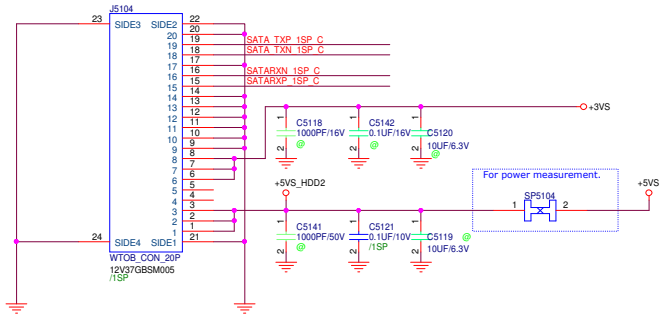
HDD(2SP)



Colay B / close to J5104



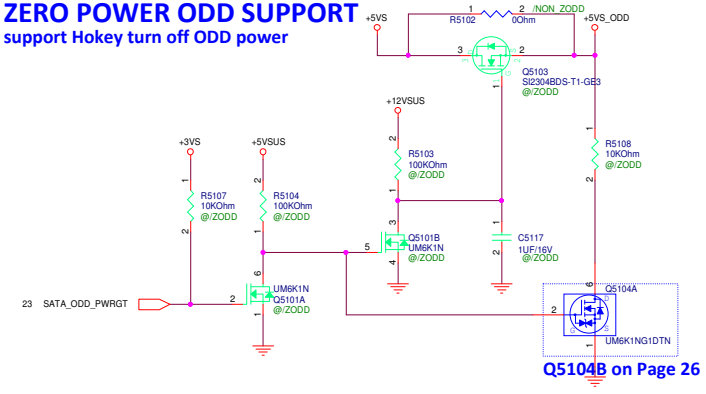
Cable HDD(1SP)



For ME request for use same cable with Z710

ZERO POWER ODD SUPPORT

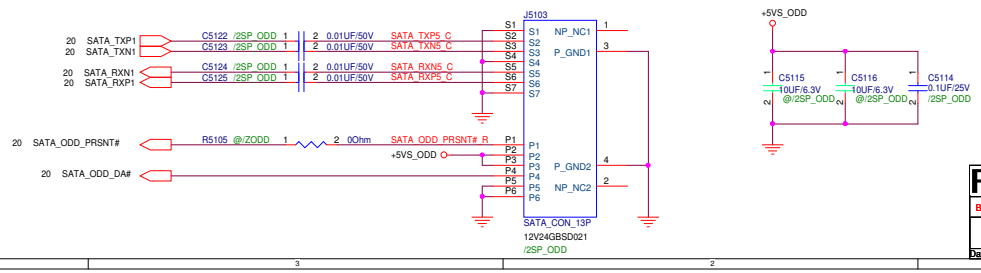
support Hokey turn off ODD power



Q5104B on Page 26

ODD for 2SP

ODD Power Consumption MAX 1.8A /Cuntinue 1.1A



PEGATRON Title : SATA HDD/ ODD

Engineer:

BG1/HW7

Size	Project Name	Rev
C	CAS(C)UG	1.0

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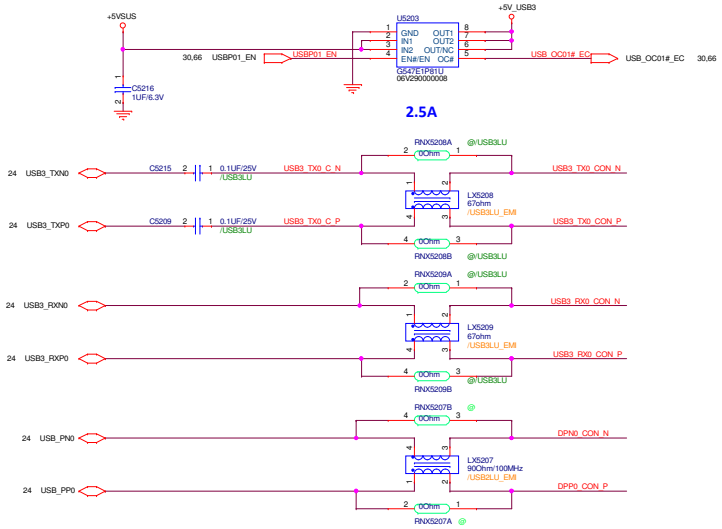
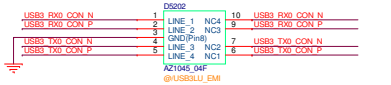
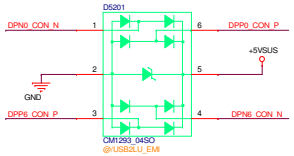
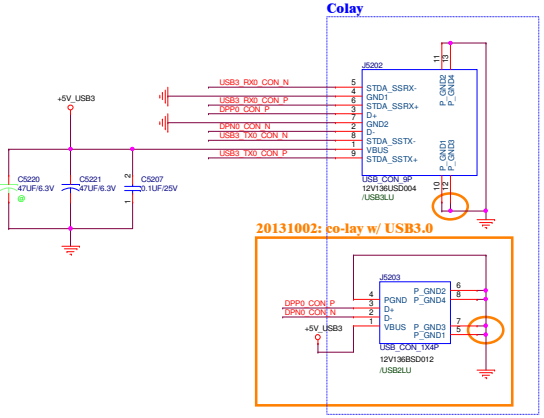
USB 3.0 (USB 2.0 colay) ports x 1 Left_UP





PLACE ESD Diodes near USB Connector





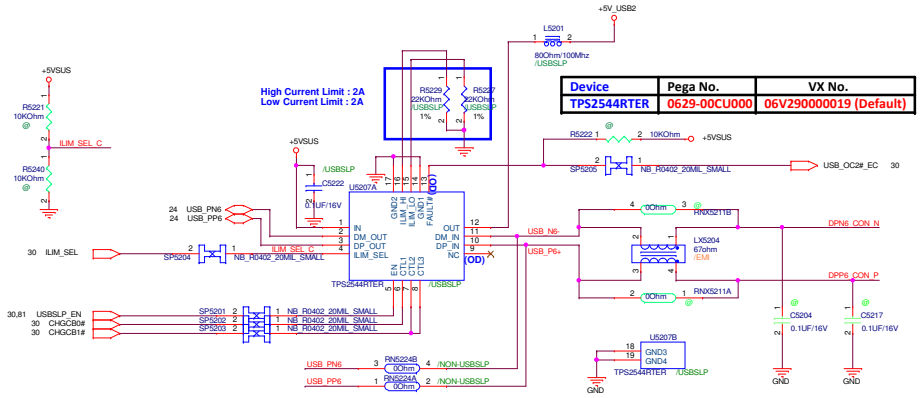
USB 3.0 ports x 1 with Sleep & Charge Left_Down

TPS2544 Device True Table

Sleep & Charge function Setting	State	Charging Mode	Wake up	CHGCB0#	CHGCB1#	ILIM_SEL	USBSLP_EN	Backup
Auto Mode	S0	CDP	NA	1	1	1	1	
	S3~S5	DCP Auto	NA	0	1	1	1	Wake up by KB/MS at S3 state
Alternative Mode	S0	CDP	NA	1	1	1	1	
	S3~S5	DCP Auto	NA	0	1	1	1	Wake up by KB/MS at S3 state
Disable	S0	CDP	NA	1	1	1	1	
	S3	SDP	Enable wake up	1	1	0	1	Wake up by KB/MS at S3 state
			Disable wake up	1	1	0	0	
	S4/S5	Discharge	NA	0	0	1	0	

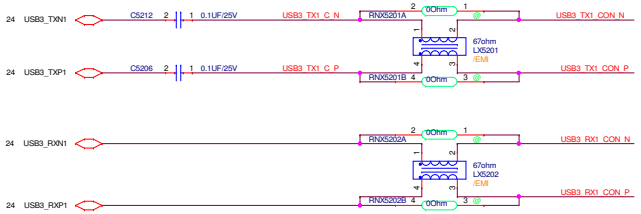
Tod's spec

Battery Charge mode	
Apple 1.0A mode	Yes
DCP mode	Yes
Apple 2.0A mode	Yes

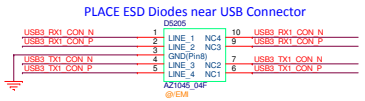


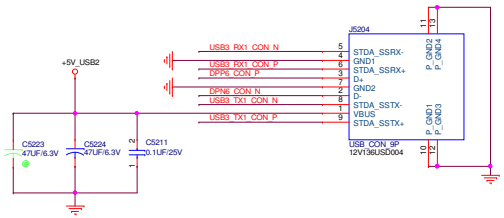
Device	Pega No.	VX No.
TPS2544RTER	0629-00CU000	06V290000019 (Default)

USBSLP / NON_USBSLP



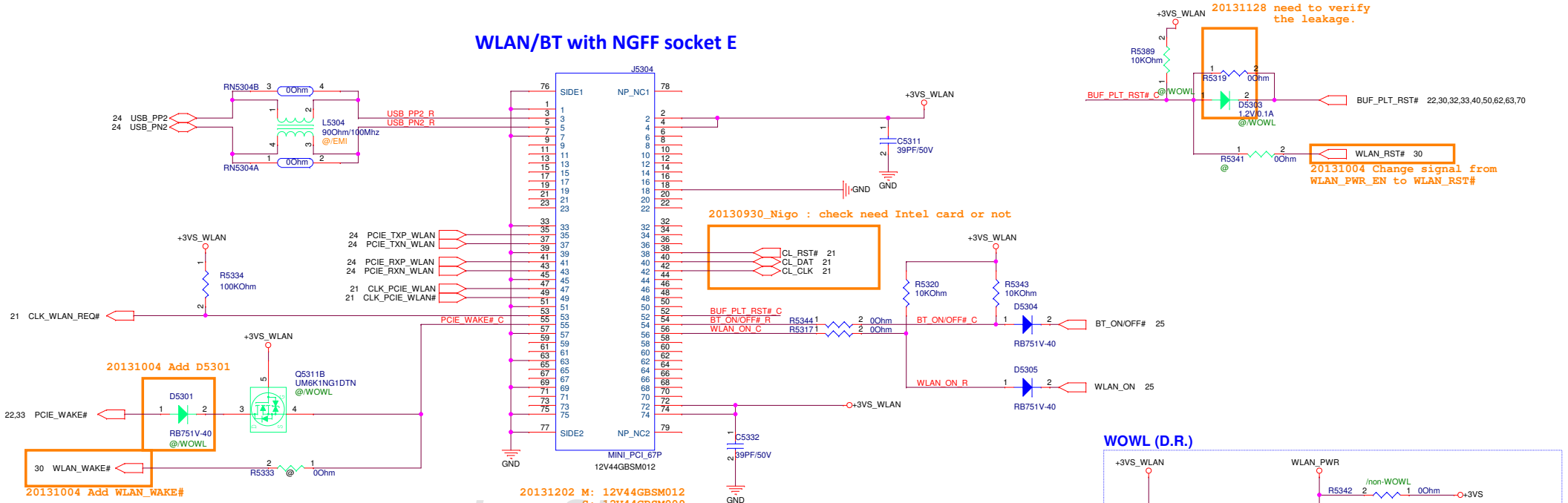
PLACE ESD Diodes near USB Connector





PEGATRON Title : USB JACK
BG1/HW7 Engineer: Fenix Chen
Size: Custom Project Name: CAS(C)UG Rev: 1.0
Date: Sunday, December 22, 2013 Sheet 52 of 103

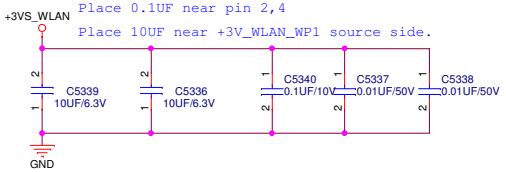
WLAN/BT with NGFF socket E



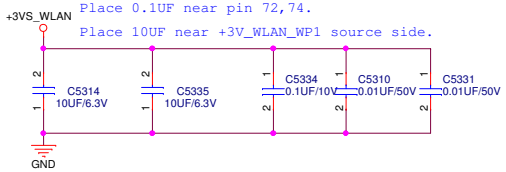
20131128 need to verify the leakage.

20131004 Change signal from WLAN_PWR_EN to WLAN_RST#

+3V_WLAN_WP1 bypass capactor:

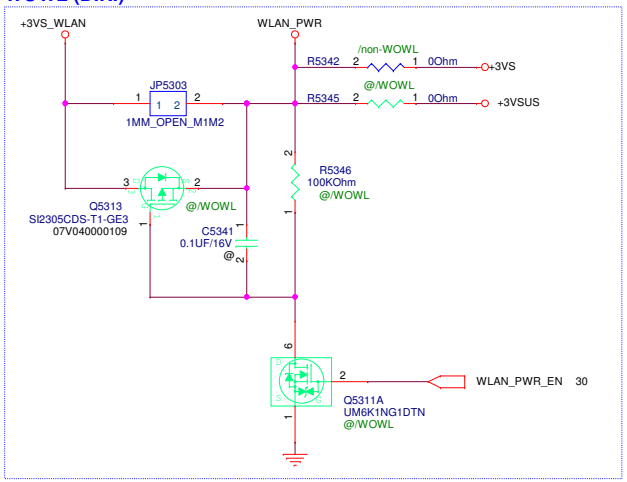


+3V_WLAN_WP1 bypass capactor:



WLAN NUT

WOWL (D.R.)



<Core Design>

PEGATRON Title : WLAN/BT

Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

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<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
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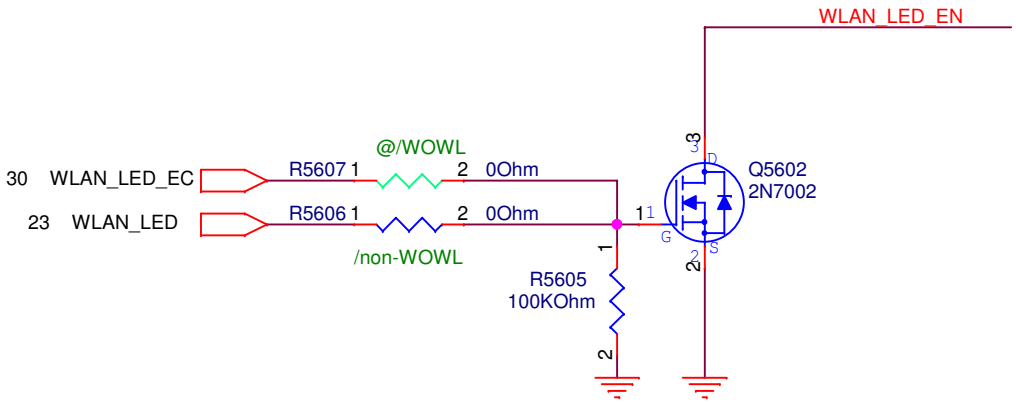
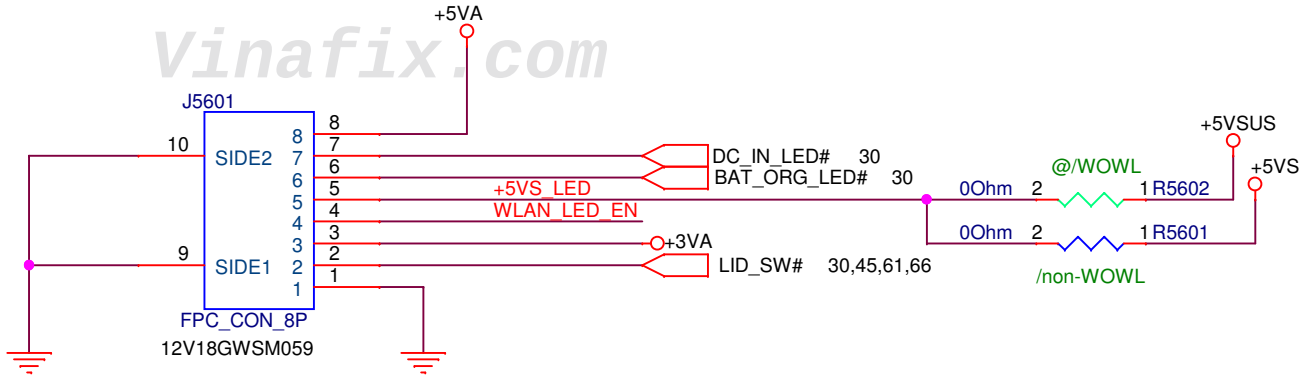
<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 55 of 103	





PEGATRON Title : LED

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
A	CAS(C)UG	1.0

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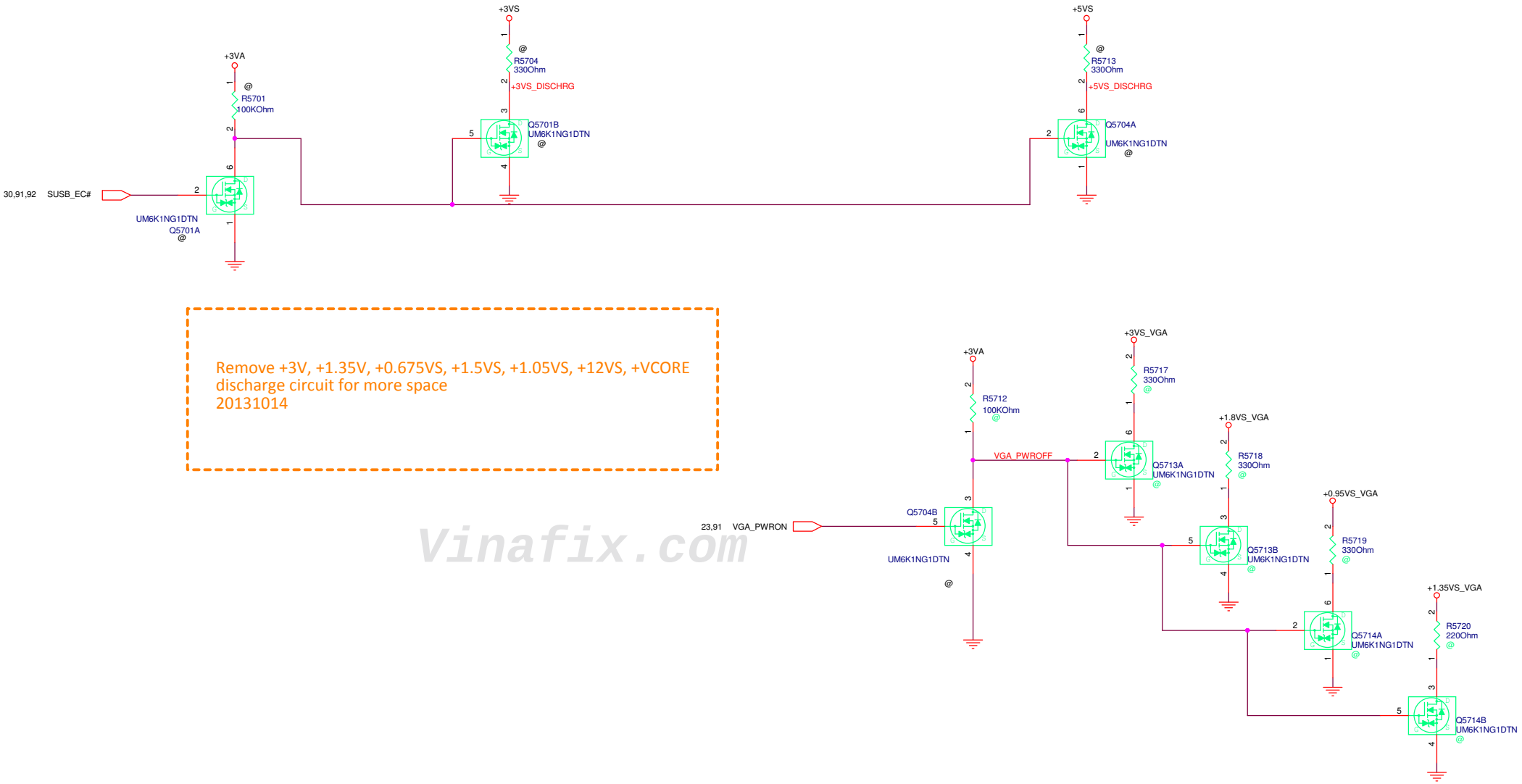

<Core Design>

PEGATRON Title : DSG_Discharge

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 57 of 103

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 58 of 103	

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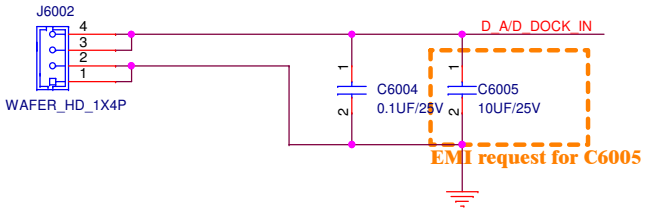
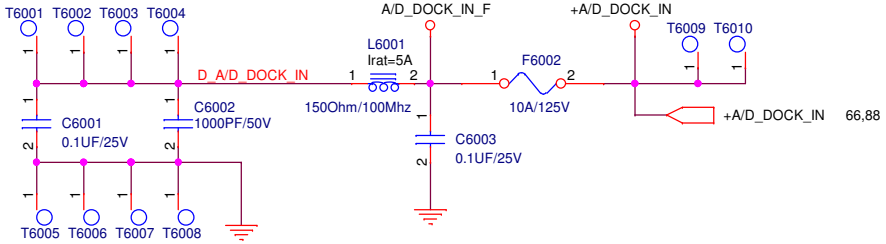
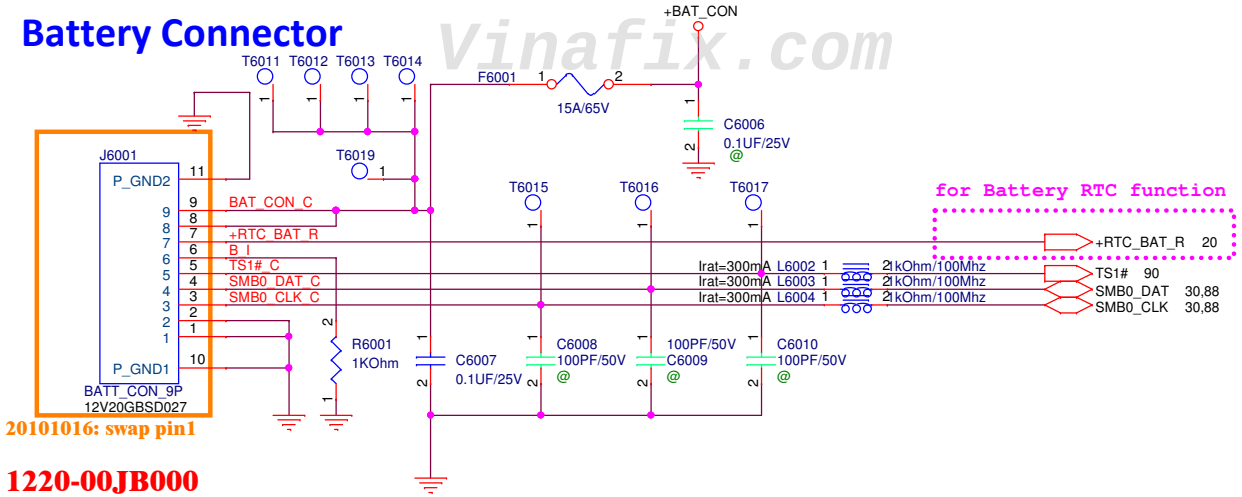
Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 59 of 103	

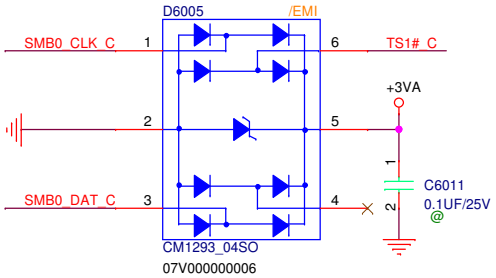
DC IN



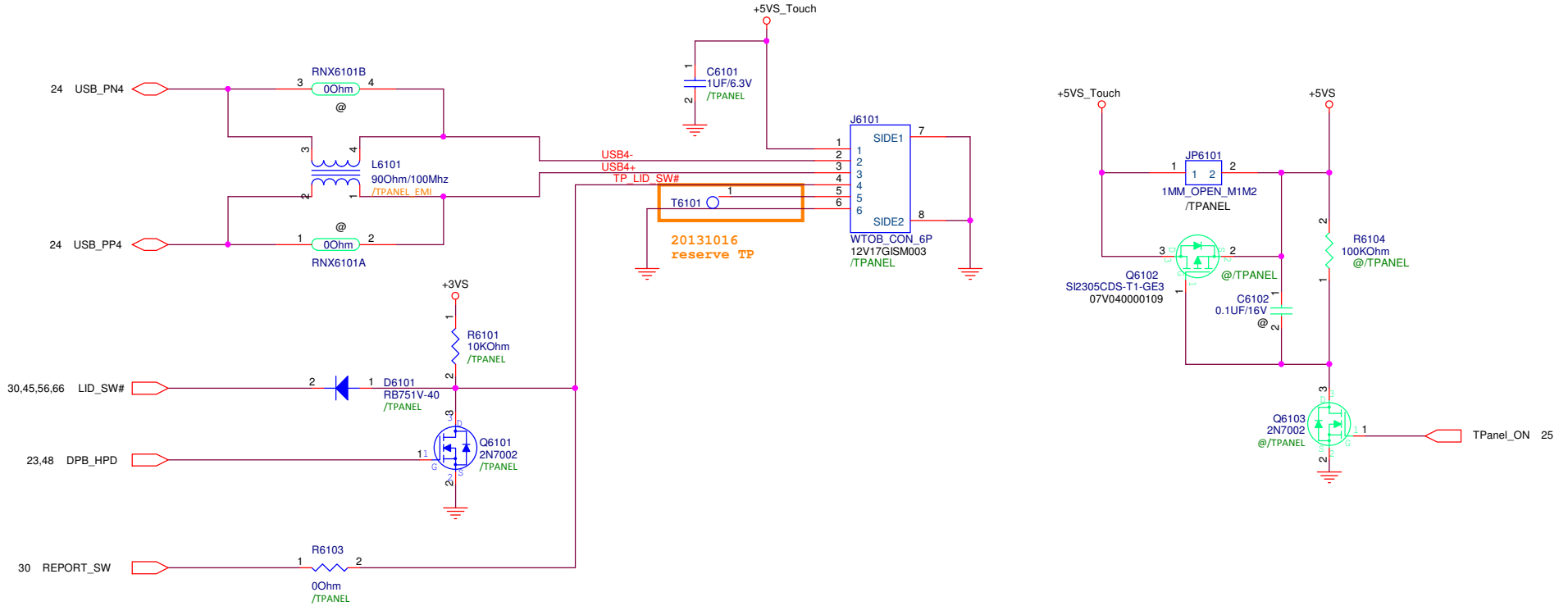


Battery Connector





PEGATRON	Title : DC-IN/ DISCHARGE	
BG1/HW7	Engineer: Fenix Chen	
Size: Custom	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 60 of 103	



Vinafix.com

<Core Design>

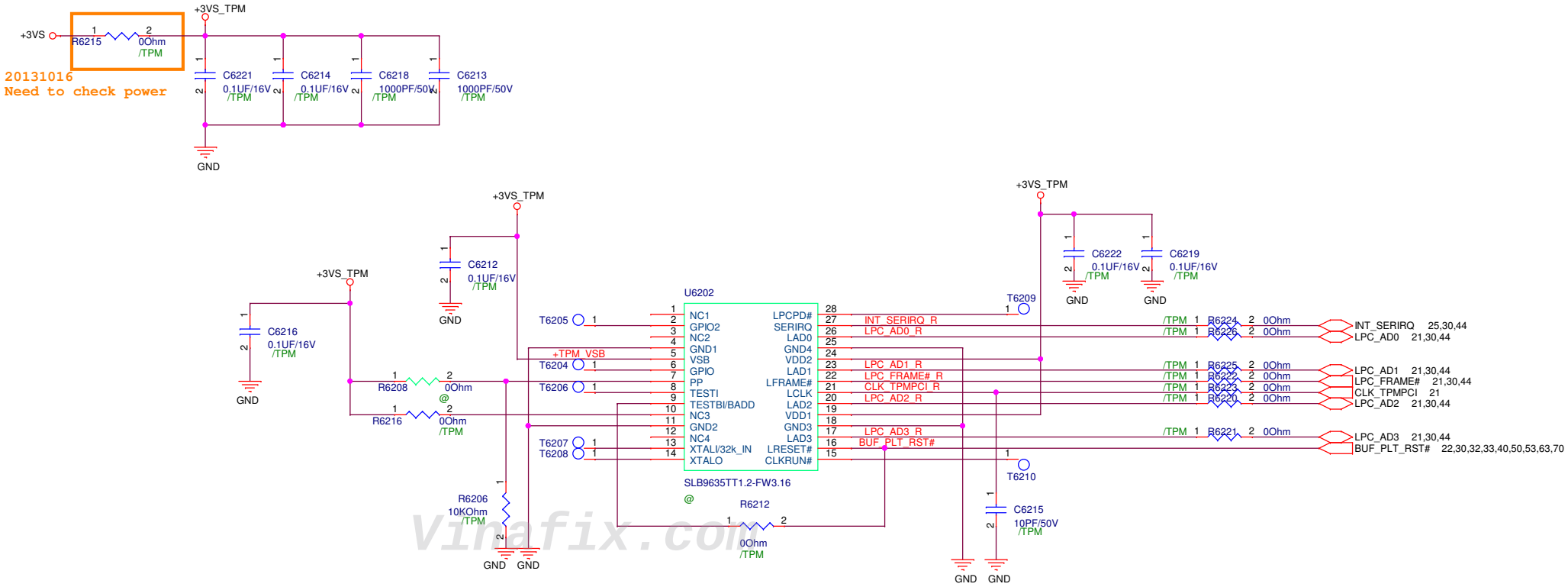
PEGATRON Title : Touch Panel Conn

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
Custom		1.0

Date: Sunday, December 22, 2013 Sheet 61 of 103

Infineon TPM 9660 and 9665 Co-lay



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PEGATRON Title : TPM Chip

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
B	CAS(C)UG	1.0

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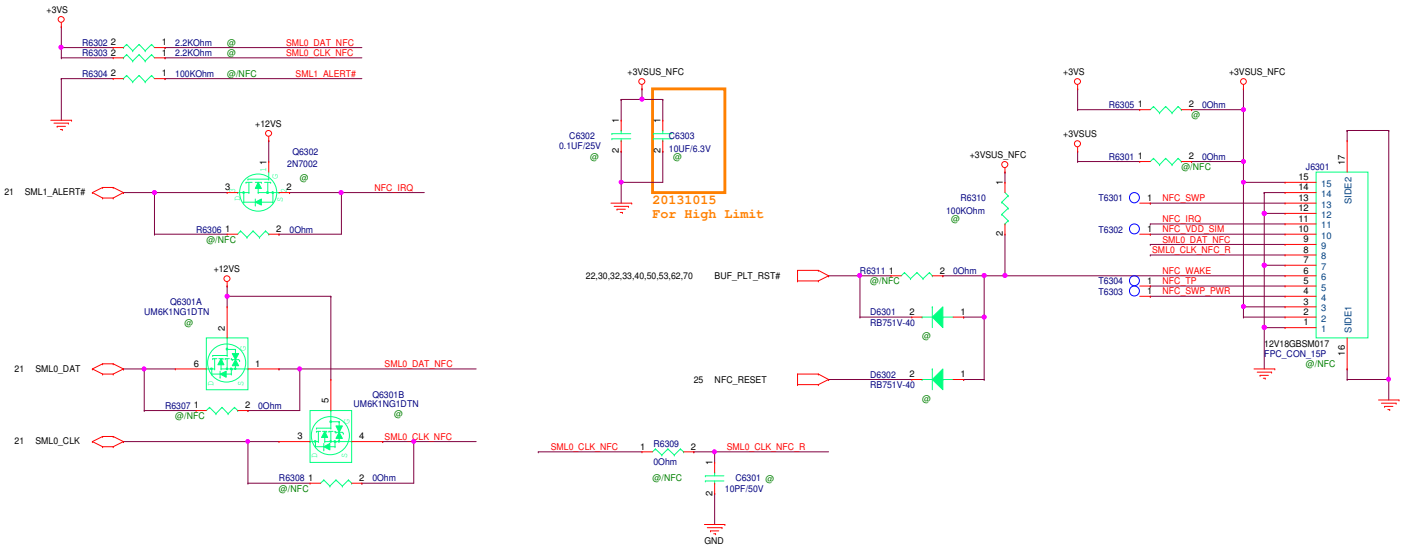
NFC I2C only for Shark Bay platorm



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PEGATRON Title : NFC Conn

BG1/HW7 Engineer: Fenix Chen

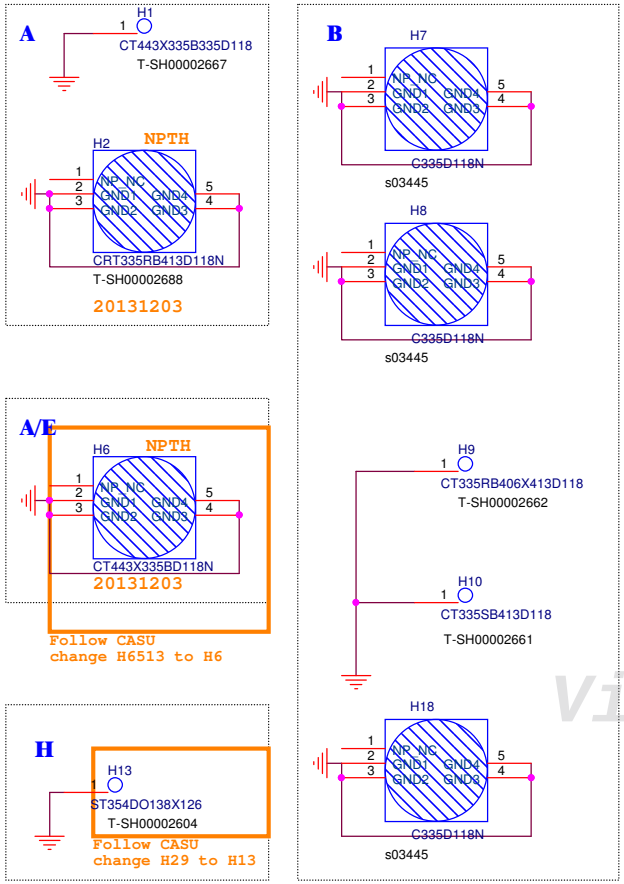
Size	Project Name	Rev
C	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 63 of 103

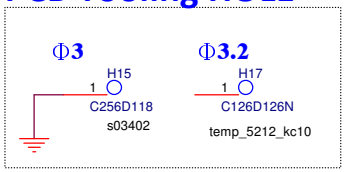
<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 64 of 103	

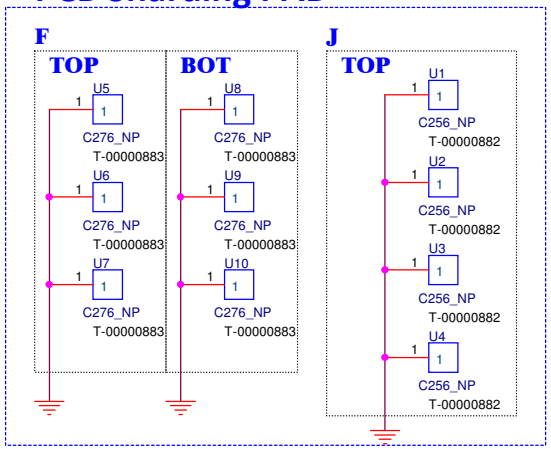
PCB SCREW HOLE



PCB Tooling HOLE

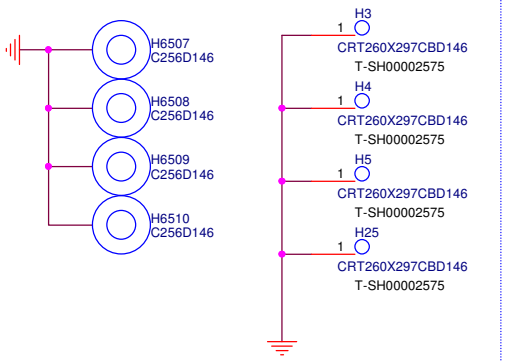


PCB Sharding PAD

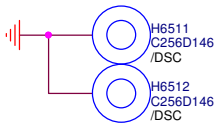


BGA E/H

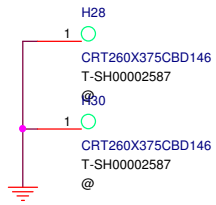
CPU NUTx4



VGA NUTx2



B/F TOP/BOT



<Core Design>

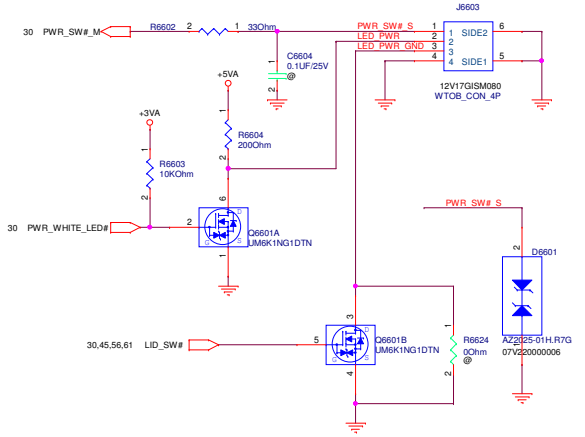
PEGATRON Title: ME_CONN,Skew Hole

Engineer: Fenix Chen

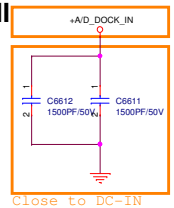
Size	Project Name	Rev
B	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 65 of 103

PWR BRD



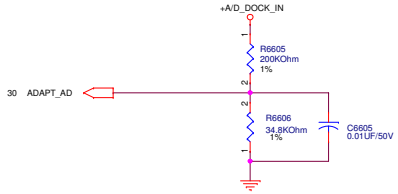
EMI



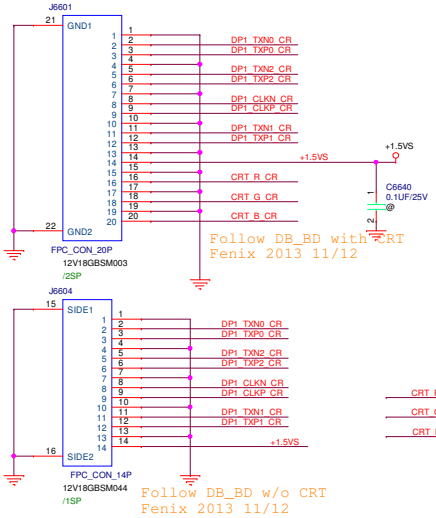
20131015: Change to "+A/D_DOCK_IN" for EMI recommend

Close to DC-IN

ADAPTOR VOLTAGE DETECTOR.

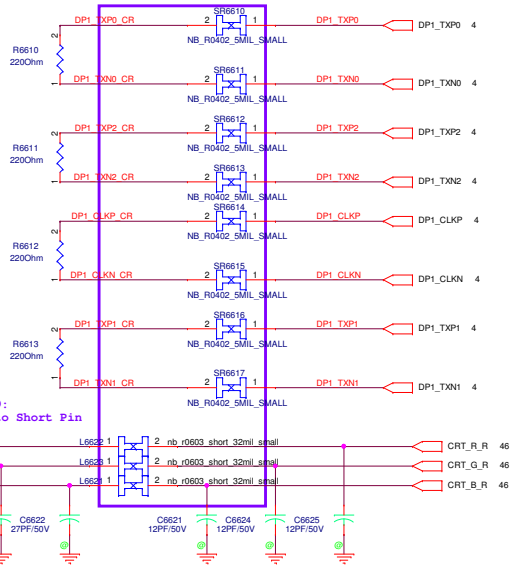


FPC Connector

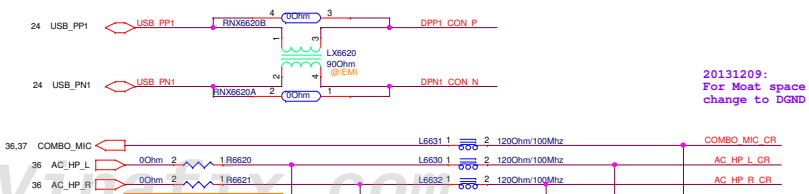


Follow DB_BD with CRT
Fenix 2013 11/12

Follow DB_BD w/o CRT
Fenix 2013 11/12

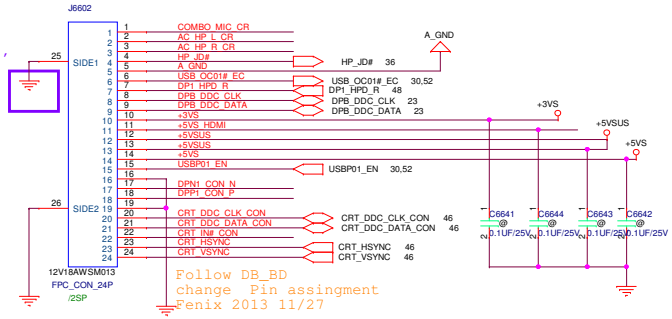


20131209:
Change to Short Pin



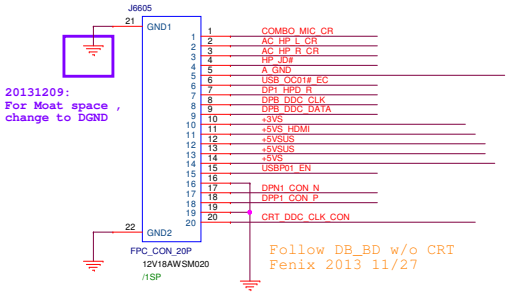
20131203: For 3 Pole MIC

FFC Connector



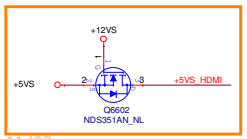
20131209:
For Moat space ,
change to DGND

Follow DB_BD
change Pin assingment
Fenix 2013 11/27

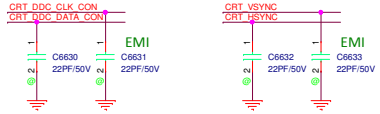


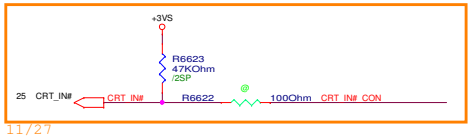
20131209:
For Moat space ,
change to DGND

Follow DB_BD w/o CRT
Fenix 2013 11/27



11/27





11/27

PEGATRON	Title : PWR BRD/ IO BRD	
BG1/HW7	Engineer: Fenix Chen	
Size: Custom	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 66 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 67 of 103	

<Core Design>

Title: <Title>		
Size: C	Document Number: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 68 of 103	

<Core Design>

Title <Title>		
Size B	Document Number CAS(C)UG	Rev 1.0
Date: Sunday, December 22, 2013	Sheet 69 of 103	

+0.95VS_VGA
+3VS_VGA

+0.95VS_VGA 57,75,76,86
+3VS_VGA 57,71,75,87,91

x4 link: two connection options (both TX and RX) supported:

Root		GPU	OR	Root		GPU
0	->	0		0	->	7
1	->	1		1	->	6
2	->	2		2	->	5
3	->	3		3	->	4

U7001A

APU PCIE_TX signal connect to GPU_PCIE_RX signal.

APU PCIE_RX signal connect to GPU_PCIE_TX signal.

24 PCIEG_TXP0	PCIEG_TXP0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIEG_RXP0	C7008 1	2 0.1UF/25V	PCIENB_RXP0	PCIENB_RXP0 24
24 PCIEG_TXN0	PCIEG_TXN0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIEG_RXN0	C7009 1	2 0.1UF/25V	PCIENB_RXN0	PCIENB_RXN0 24
24 PCIEG_TXP1	PCIEG_TXP1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIEG_RXP1	C7012 1	2 0.1UF/25V	PCIENB_RXP1	PCIENB_RXP1 24
24 PCIEG_TXN1	PCIEG_TXN1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIEG_RXN1	C7013 1	2 0.1UF/25V	PCIENB_RXN1	PCIENB_RXN1 24
24 PCIEG_TXP2	PCIEG_TXP2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIEG_RXP2	C7014 1	2 0.1UF/25V	PCIENB_RXP2	PCIENB_RXP2 24
24 PCIEG_TXN2	PCIEG_TXN2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIEG_RXN2	C7015 1	2 0.1UF/25V	PCIENB_RXN2	PCIENB_RXN2 24
24 PCIEG_TXP3	PCIEG_TXP3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIEG_RXP3	C7016 1	2 0.1UF/25V	PCIENB_RXP3	PCIENB_RXP3 24
24 PCIEG_TXN3	PCIEG_TXN3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIEG_RXN3	C7017 1	2 0.1UF/25V	PCIENB_RXN3	PCIENB_RXN3 24
		AB30	PCIE_RX4P	PCIE_TX4P	AC25					
		AA31	PCIE_RX4N	PCIE_TX4N	AB25					
		AA29	PCIE_RX5P	PCIE_TX5P	Y23					
		Y28	PCIE_RX5N	PCIE_TX5N	Y24					
		Y30	PCIE_RX6P	PCIE_TX6P	AB27					
		W31	PCIE_RX6N	PCIE_TX6N	AB26					
		W29	PCIE_RX7P	PCIE_TX7P	Y27					
		V28	PCIE_RX7N	PCIE_TX7N	Y26					
		V30	NC95	NC100	W24					
		U31	NC91	NC99	W23					
		U29	NC89	NC94	V27					
		T28	NC83	NC88	U26					
		T30	NC84	NC87	U24					
		R31	NC78	NC86	U23					
		R29	NC77	NC81	T26					
		P28	NC75	NC82	T27					
		P30	NC76	NC80	T24					
		N31	NC70	NC79	T23					
		N29	NC69	NC74	P27					
		M28	NC66	NC73	P26					
		M30	NC67	NC72	P24					
		L31	NC64	NC71	P23					
		L29	NC63	NC65	M27					
		K30	NC62	NC68	N26					

PCI EXPRESS INTERFACE

20131011: SHB-U/BDW-U all support up to PCIe-Gen2
AC coupling changed to 0.1uF

Freq. : 100M Hz (+/- 300ppm)

21 CLK_PCIE_PEG_PCH — CLK_PCIE_PEG_PCH — AK30 — PCIE_REFCLKP
21 CLK_PCIE_PEG#_PCH — CLK_PCIE_PEG#_PCH — AK32 — PCIE_REFCLKN

CLOCK

GND — R7003 2 1 1KOhm — N10 — TEST_PG

+3VS_VGA — R7005 10KOhm — AL27 — PERSTB

PRO-S3
02V050000023

CALIBRATION

+0.95VS_VGA

Y22 VGA_PCIE_CALRP — R7006 — 1.69KOhm 1% — PCIE_CALR_TX
AA22 VGA_PCIE_CALRN — R7007 — 1KOhm 1% — PCIE_CALR_RX

D7001 1V/0.1A

25,50,71 DGPU_HOLD_RST#
22,30,32,33,40,50,53,62,63 BUF_PLT_RST#

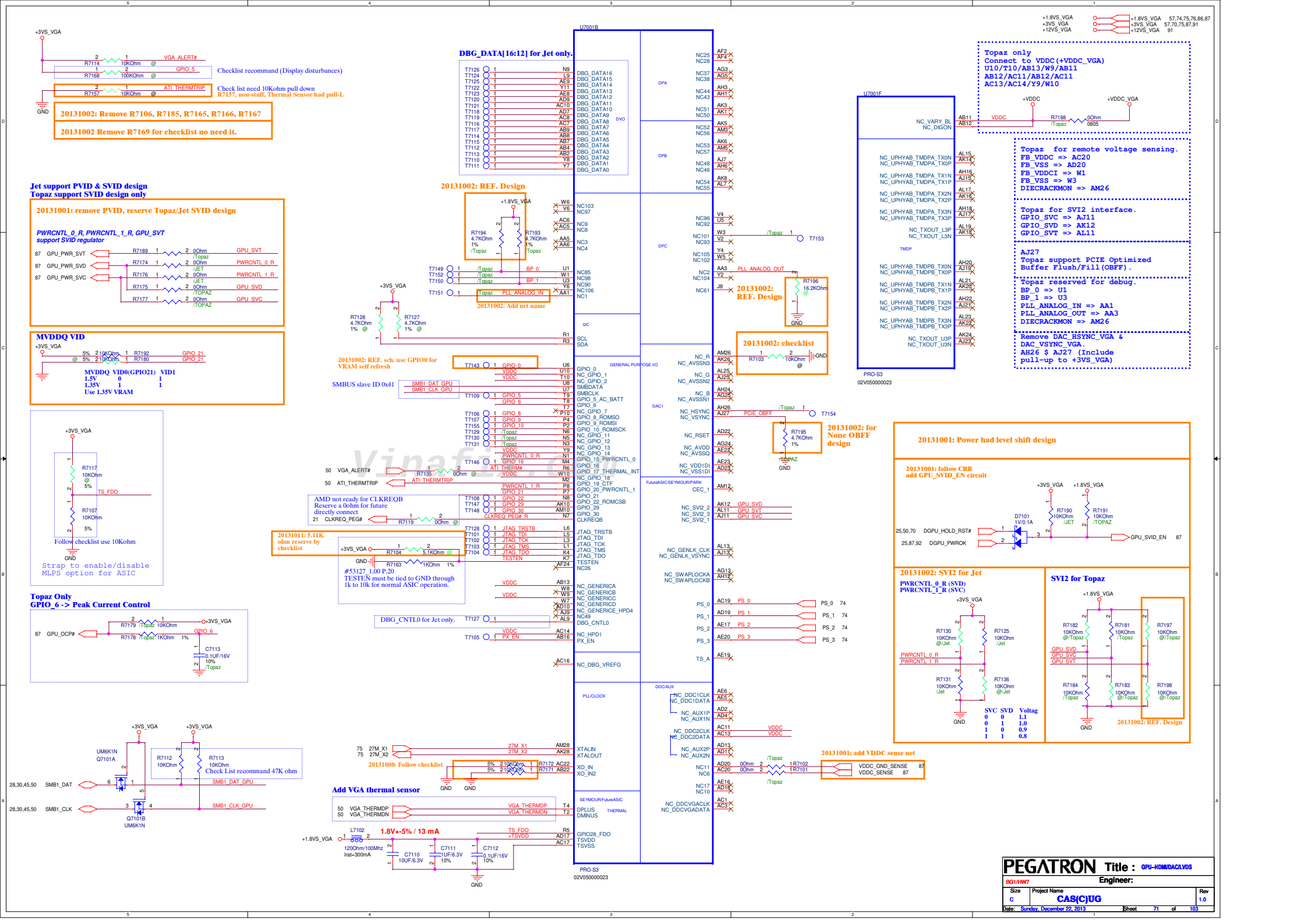
20131001: link to platform reset

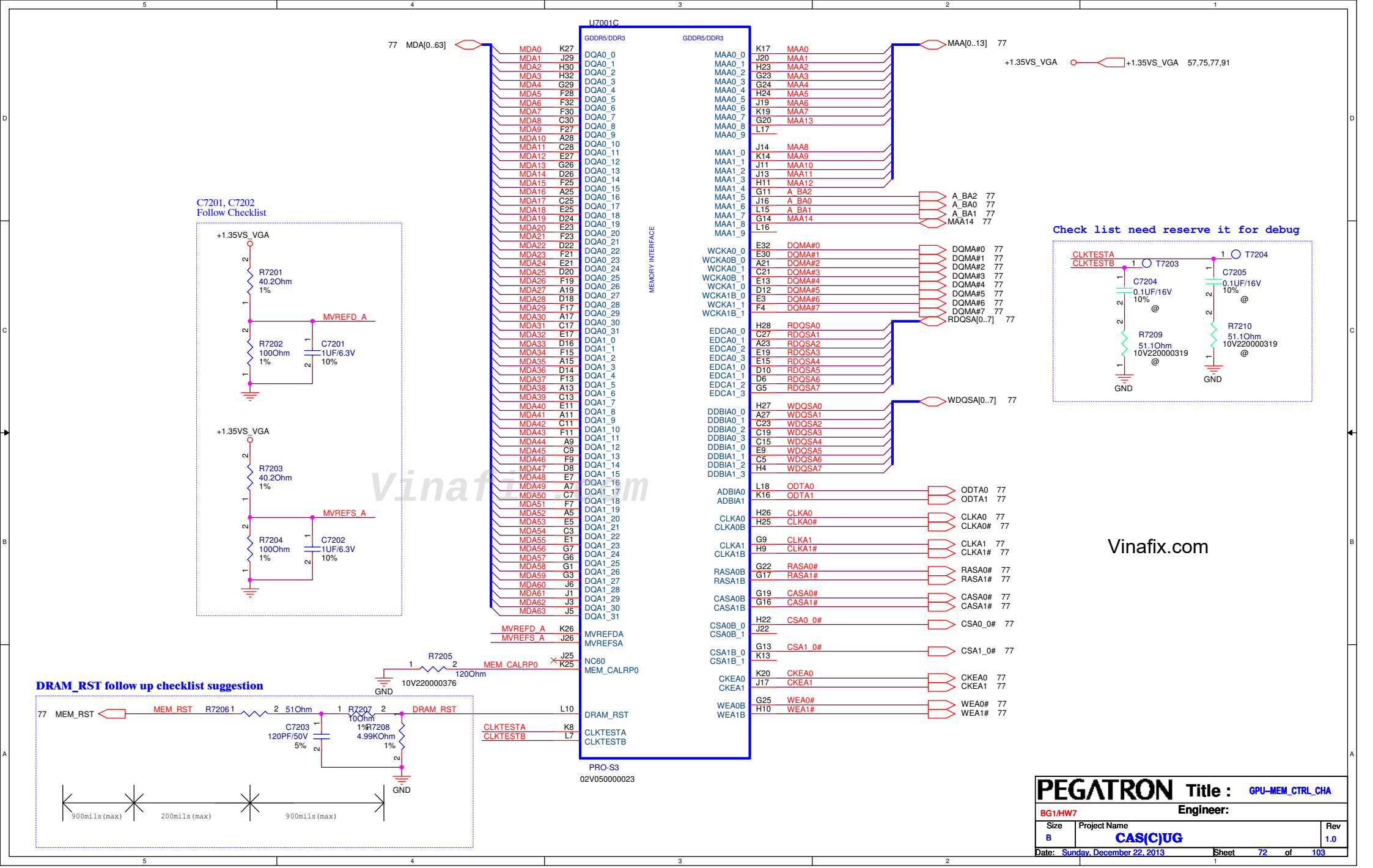
R7004 1 @ 2 0Ohm

PEGATRON Title : GPU-PCIE
BG1/HW7 Engineer:

Size	Project Name	Rev
Custom	CAS(C)UG	1.0

Date: Sunday, December 22, 2013 Sheet 70 of 103

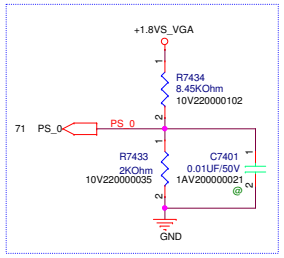

+3VS_VGA
R7114 10KOhm @ VGA_ALERT#
R7168 100KOhm @ GPIO_5
Checklist recommand (Display disturbances)
R7157 10KOhm @ ATI_THERMTRIP
Check list need 10Kohm pull down
R7157, non-stuff, Thermal Sensor had pull-L
GND
20131002: Remove R7106, R7185, R7165, R7166, R7167
20131002 Remove R7169 for checklist no need it.
Jet support PVID & SVID design
Topaz support SVID design only
20131001: remove PVID, reserve Topaz/Jet SVID design
PWRCNTL_0_R, PWRCNTL_1_R, GPU_SVT
support SVID regulator
87 GPU_PWR_SVT R7189 0Ohm /Topaz GPU_SVT
87 GPU_PWR_SVD R7174 0Ohm /JET PWRCNTL_0_R
87 GPU_PWR_SVC R7176 0Ohm /JET PWRCNTL_1_R
R7175 0Ohm /TOPAZ GPU_SVD
R7177 0Ohm /TOPAZ GPU_SVC
MVDDQ VID
MVDDQ VID0(GPIO21) VID1
1.5V 0 1
1.35V 1 1
Use 1.35V VRAM
R7117 10KOhm @ 5%
TS_FDO
R7107 10KOhm 5%
Follow checklist use 10Kohm
Strap to enable/disable MLPS option for ASIC
Topaz Only
GPIO_6 -> Peak Current Control
87 GPU_OCP# R7179 /Topaz 10KOhm R7178 /Topaz 1KOhm 1%
GPIO_6
C7113 0.1UF/16V 10% /Topaz
UM6K1N Q7101A
R7112 10KOhm
R7113 10KOhm
Check List recommand 47K ohm
28,30,45,50 SMB1_DAT
28,30,45,50 SMB1_CLK
SMB1_DAT_GPU
SMB1_CLK_GPU
Q7101B UM6K1N
DBG_DATA[16:12] for Jet only.
T7126 N9 DBG_DATA16
T7124 L9 DBG_DATA15
T7125 AE9 DBG_DATA14
T7122 Y11 DBG_DATA13
T7123 AE8 DBG_DATA12
T7120 AD9 DBG_DATA11
T7121 AC10 DBG_DATA10
T7118 AD7 DBG_DATA9
T7119 AC8 DBG_DATA8
T7116 AC7 DBG_DATA7
T7117 AB9 DBG_DATA6
T7114 AB8 DBG_DATA5
T7115 AB7 DBG_DATA4
T7112 AB4 DBG_DATA3
T7113 AB2 DBG_DATA2
T7110 Y8 DBG_DATA1
T7111 Y7 DBG_DATA0
20131002: REF. Design
+1.8VS_VGA
R7194 4.7KOhm 1% /Topaz
R7193 4.7KOhm 1% /Topaz
T7149 /Topaz BP_0 U1
T7152 /Topaz W1
T7150 /Topaz BP_1 U3
T7151 Topaz PLL_ANALOG_IN AA1
20131002: Add net name
+3VS_VGA
R7128 4.7KOhm 1% @
R7127 4.7KOhm 1% @
SCL R1
SDA R3
20131002: REF. sch. use GPIO0 for VRAM self refresh
T7143 GPIO_0 U6
VDDC U10
VDDC T10
SMBUS slave ID 0x41
SMB1_DAT_GPU U8
SMB1_CLK_GPU U7
T7109 GPIO_5 T9
GPIO_6 T8
GPIO_8 T7
T7106 GPIO_8 P10
T7107 GPIO_9 P4
T7155 GPIO_10 P2
T7129 /Topaz N6
T7130 /Topaz N5
T7131 /Topaz N3
VDDC Y9
PWRCNTL_0_R N1
T7146 GPIO_16 M4
50 VGA_ALERT# R7135 0Ohm @ ATI_THERM# R6
50 ATI_THERMTRIP ATI_THERMTRIP VDDC W10
PWRCNTL_1_R M2
GPIO_21 P8
AMD not ready for CLKREQB
Reserve a 0ohm for future
directly connect
T7108 GPIO_22 P7
T7147 GPIO_29 N8
T7148 GPIO_30 AK10
21 CLKREQ_PEG# R7119 0Ohm @ CLKREQ_PEG# R AM10
20131011: 5.11K ohm reserve by checklist
+3VS_VGA R7104 5.1KOhm @
GND R7163 1KOhm 1%
#53127_1.00 P.20
TESTEN must be tied to GND through 1k to 10k for normal ASIC operation.
T7128 JTAG_TRSTB L6
T7101 JTAG_TDI L5
T7102 JTAG_TCK L3
T7103 JTAG_TMS L1
T7104 JTAG_TDO K4
TESTEN K7
AP24
VDDC AB13
VDDC W8
W9
W7
AD10
AJ9
AL9
DBG_CNTL0 for Jet only. T7127
VDDC AC14
T7105 PX_EN AB16
AC16
75 27M_X1 27M_X1 AM28
75 27M_X2 27M_X2 AK28
20131008: Follow checklist
5% 210KOhm R7172 AC22
5% 210KOhm R7171 AB22
GND GND
Add VGA thermal sensor
50 VGA_THERMDP VGA_THERMDP T4
50 VGA_THERMDN VGA_THERMDN T2
+1.8VS_VGA L7102 120Ohm/100Mhz Irat=300mA
1.8V+-5% / 13 mA
C7110 10UF/6.3V
C7111 1UF/6.3V 10%
C7112 0.1UF/16V 10%
TS_FDO R5
+TSVDD AD17
AC17
GPIO28_FDO
TSVDD
TSVSS
GND
PRO-S3
02V050000023
U7001B
DVO
DPA
DPB
DPC
I2C
GENERAL PURPOSE I/O
DAC1
FutureASIC/SEYMOUR/PARK
PLL/CLOCK
DDC/AUX
SEYMOUR/FutureASIC
THERMAL
DPLUS
DMINUS
GPIO_0
NC_GPIO_1
NC_GPIO_2
SMBDATA
SMBCLK
GPIO_5_AC_BATT
GPIO_6
NC_GPIO_7
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
NC_GPIO_11
NC_GPIO_12
NC_GPIO_13
NC_GPIO_14
GPIO_15_PWRCNTL_0
GPIO_16
GPIO_17_THERMAL_INT
NC_GPIO_18
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21
GPIO_22_ROMCSB
GPIO_29
GPIO_30
CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN
NC26
NC_GENERICA
NC_GENERICB
NC_GENERICC
NC_GENERICD
NC_GENERICE_HPD4
NC49
DBG_CNTL0
NC_HPD1
PX_EN
NC_DBG_VREFG
XTALIN
XTALOUT
XO_IN
XO_IN2
NC103 NC97
NC9 NC8
NC3 NC4
NC85 NC98 NC90 NC106 NC1
NC25 NC28 AF2 AF4
NC37 NC38 AG3 AG5
NC44 NC43 AH3 AH1
NC51 NC50 AK3 AK1
NC52 NC56 AK5 AM3
NC53 NC57 AK6 AM5
NC48 NC46 AJ7 AH6
NC54 NC55 AK8 AL7
NC96 NC92 V4 U5
NC101 NC93 W3 V2
NC105 NC102 Y4 W5
NC2 NC104 AA3 Y2
NC61 J8
PLL_ANALOG_OUT
20131002: REF. Design
R7196 16.2KOhm @
GND
20131002: checklist
R7103 10KOhm @
NC_R NC_AVSSN3 AM26 AK26
NC_G NC_AVSSN2 AL25 AJ24
NC_B NC_AVSSN1 AH24 AG24
NC_HSYNC AH26
NC_VSYNC AJ27
PCIE_OBFF
R7195 4.7KOhm 1%
/TOPAZ
GND
20131002: for None OBFF design
NC_RSET AD22
NC_AVDD AG24
NC_AVSSQ AE22
NC_VDD1DI AE23
NC_VSS1DI AD23
CEC_1 AM12
NC_SVI2_2 AK12 GPU_SVD
NC_SVI2_3 AL11 GPU_SVT
NC_SVI2_1 AJ11 GPU_SVC
NC_GENLK_CLK AL13
NC_GENLK_VSYNC AJ13
NC_SWAPLOCKA AG13
NC_SWAPLOCKB AH12
PS_0 AC19 PS_0 PS_0 74
PS_1 AD19 PS_1 PS_1 74
PS_2 AE17 PS_2 PS_2 74
PS_3 AE20 PS_3 PS_3 74
TS_A AE19
NC_DDC1CLK AE6
NC_DDC1DATA AE5
NC_AUX1P AD2
NC_AUX1N AD4
NC_DDC2CLK AC11 VDDC
NC_DDC2DATA AC13 VDDC
NC_AUX2P AD13
NC_AUX2N AD11
NC11 AD20 0Ohm /Topaz R7102
NC6 AC20 0Ohm /Topaz R7101
AE16
NC17 AD18
NC10
NC_DDCVGACLK AC1
NC_DDCVGADATA AC3
20131001: add VDDC sense net
VDDC_GND_SENSE 87
VDDC_SENSE 87
U7001F
NC_VARY_BL AB11
NC_DIGON AB12
NC_UPHYAB_TMDPA_TX0N AL15
NC_UPHYAB_TMDPA_TX0P AK14
NC_UPHYAB_TMDPA_TX1N AH16
NC_UPHYAB_TMDPA_TX1P AJ15
NC_UPHYAB_TMDPA_TX2N AL17
NC_UPHYAB_TMDPA_TX2P AK16
NC_UPHYAB_TMDPA_TX3N AH18
NC_UPHYAB_TMDPA_TX3P AJ17
NC_TXOUT_L3P AL19
NC_TXOUT_L3N AK18
TMDP
NC_UPHYAB_TMDPB_TX0N AH20
NC_UPHYAB_TMDPB_TX0P AJ19
NC_UPHYAB_TMDPB_TX1N AL21
NC_UPHYAB_TMDPB_TX1P AK20
NC_UPHYAB_TMDPB_TX2N AH22
NC_UPHYAB_TMDPB_TX2P AJ21
NC_UPHYAB_TMDPB_TX3N AL23
NC_UPHYAB_TMDPB_TX3P AK22
NC_TXOUT_U3P AK24
NC_TXOUT_U3N AJ23
PRO-S3
02V050000023
+1.8VS_VGA
+3VS_VGA
+12VS_VGA
+1.8VS_VGA 57,74,75,76,86,87
+3VS_VGA 57,70,75,87,91
+12VS_VGA 91
Topaz only
Connect to VDDC(+VDDC_VGA)
U10/T10/AB13/W9/AB11
AB12/AC11/AB12/AC11
AC13/AC14/Y9/W10
+VDDC
+VDDC_VGA
VDDC R7188 0Ohm /Topaz 0805
Topaz for remote voltage sensing.
FB_VDDC => AC20
FB_VSS => AD20
FB_VDDCI => W1
FB_VSS => W3
DIECRACKMON => AM26
Topaz for SVI2 interface.
GPIO_SVC => AJ11
GPIO_SVD => AK12
GPIO_SVT => AL11
AJ27
Topaz support PCIE Optimized
Buffer Flush/Fill(OBFF).
Topaz reserved for debug.
BP_0 => U1
BP_1 => U3
PLL_ANALOG_IN => AA1
PLL_ANALOG_OUT => AA3
DIECRACKMON => AM26
Remove DAC_HSYNC_VGA &
DAC_VSYNC_VGA.
AH26 $ AJ27 (Include
pull-up to +3VS_VGA)
20131001: Power had level shift design
20131001: follow CRB
add GPU_SVID_EN circuit
+3VS_VGA +1.8VS_VGA
D7101 1V/0.1A
R7190 10KOhm /JET
R7191 10KOhm /TOPAZ
25,50,70 DGPU_HOLD_RST#
25,87,92 DGPU_PWROK
GPU_SVID_EN 87
20131002: SVI2 for Jet
PWRCNTL_0_R (SVD)
PWRCNTL_1_R (SVC)
+3VS_VGA
R7130 10KOhm @/Jet
R7125 10KOhm /Jet
PWRCNTL_0_R
PWRCNTL_1_R
R7131 10KOhm /Jet
R7136 10KOhm @/Jet
GND
SVC SVD Voltag
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
SVI2 for Topaz
+1.8VS_VGA
R7182 10KOhm @/Topaz
R7181 10KOhm /Topaz
R7197 10KOhm @/Topaz
GPU_SVD
GPU_SVC
GPU_SVT
R7184 10KOhm /Topaz
R7183 10KOhm @/Topaz
R7198 10KOhm @/Topaz
GND
20131002: REF. Design
PEGATRON Title : GPU-HDMI/DAC/LVDS
Engineer:
BG1/HW7
Size C
Project Name CAS(C)UG
Rev 1.0
Date: Sunday, December 22, 2013
Sheet 71 of 103


U7001C
GDDR5/DDR3
GDDR5/DDR3
MEMORY INTERFACE
77 MDA[0..63]
MDA0 K27
MDA1 J29
MDA2 H30
MDA3 H32
MDA4 G29
MDA5 F28
MDA6 F32
MDA7 F30
MDA8 C30
MDA9 F27
MDA10 A28
MDA11 C28
MDA12 E27
MDA13 G26
MDA14 D26
MDA15 F25
MDA16 A25
MDA17 C25
MDA18 E25
MDA19 D24
MDA20 E23
MDA21 F23
MDA22 D22
MDA23 F21
MDA24 E21
MDA25 D20
MDA26 F19
MDA27 A19
MDA28 D18
MDA29 F17
MDA30 A17
MDA31 C17
MDA32 E17
MDA33 D16
MDA34 F15
MDA35 A15
MDA36 D14
MDA37 F13
MDA38 A13
MDA39 C13
MDA40 E11
MDA41 A11
MDA42 C11
MDA43 F11
MDA44 A9
MDA45 C9
MDA46 F9
MDA47 D8
MDA48 E7
MDA49 A7
MDA50 C7
MDA51 F7
MDA52 A5
MDA53 E5
MDA54 C3
MDA55 E1
MDA56 G7
MDA57 G6
MDA58 G1
MDA59 G3
MDA60 J6
MDA61 J1
MDA62 J3
MDA63 J5
MVREFD_A K26
MVREFS_A J26
MVREFDA
MVREFSA
J25
K25
NC60
MEM_CALRP0
DRAM_RST
L10
CLKTESTA K8
CLKTESTB L7
CLKTESTA
CLKTESTB
PRO-S3
02V050000023
MAA0 K17
MAA1 J20
MAA2 H23
MAA3 G23
MAA4 G24
MAA5 H24
MAA6 J19
MAA7 K19
MAA13 G20
L17
MAA8 J14
MAA9 K14
MAA10 J11
MAA11 J13
MAA12 H11
A_BA2 G11
A_BA0 J16
A_BA1 L15
MAA14 G14
L16
DQMA#0 E32
DQMA#1 E30
DQMA#2 A21
DQMA#3 C21
DQMA#4 E13
DQMA#5 D12
DQMA#6 E3
DQMA#7 F4
RDQSA0 H28
RDQSA1 C27
RDQSA2 A23
RDQSA3 E19
RDQSA4 E15
RDQSA5 D10
RDQSA6 D6
RDQSA7 G5
WDQSA0 H27
WDQSA1 A27
WDQSA2 C23
WDQSA3 C19
WDQSA4 C15
WDQSA5 E9
WDQSA6 C5
WDQSA7 H4
ODTA0 L18
ODTA1 K16
CLKA0 H26
CLKA0# H25
CLKA1 G9
CLKA1# H9
RASA0# G22
RASA1# G17
CASA0# G19
CASA1# G16
CSA0_0# H22
CSA1_0# G13
CKEA0 K20
CKEA1 J17
WEA0# G25
WEA1# H10
MAA[0..13] 77
+1.35VS_VGA
+1.35VS_VGA 57,75,77,91
A_BA2 77
A_BA0 77
A_BA1 77
MAA14 77
DQMA#0 77
DQMA#1 77
DQMA#2 77
DQMA#3 77
DQMA#4 77
DQMA#5 77
DQMA#6 77
DQMA#7 77
RDQSA[0..7] 77
WDQSA[0..7] 77
ODTA0 77
ODTA1 77
CLKA0 77
CLKA0# 77
CLKA1 77
CLKA1# 77
RASA0# 77
RASA1# 77
CASA0# 77
CASA1# 77
CSA0_0# 77
CSA1_0# 77
CKEA0 77
CKEA1 77
WEA0# 77
WEA1# 77
C7201, C7202
Follow Checklist
+1.35VS_VGA
R7201
40.2Ohm
1%
MVREFD_A
R7202
100Ohm
1%
C7201
1UF/6.3V
10%
+1.35VS_VGA
R7203
40.2Ohm
1%
MVREFS_A
R7204
100Ohm
1%
C7202
1UF/6.3V
10%
R7205
120Ohm
10V220000376
GND
MEM_CALRP0
DRAM_RST follow up checklist suggestion
77 MEM_RST
MEM_RST
R7206
51Ohm
R7207
100Ohm
1%
DRAM_RST
C7203
120PF/50V
5%
R7208
4.99KOhm
1%
GND
900mils(max)
200mils(max)
900mils(max)
Check list need reserve it for debug
CLKTESTA
CLKTESTB
T7203
T7204
C7204
0.1UF/16V
10%
@
R7209
51.1Ohm
10V220000319
@
C7205
0.1UF/16V
10%
@
R7210
51.1Ohm
10V220000319
@
GND
GND
Vinafix.com
PEGATRON
Title : GPU-MEM_CTRL_CHA
BG1/HW7
Engineer:
Size
B
Project Name
CAS(C)UG
Rev
1.0
Date: Sunday, December 22, 2013
Sheet 72 of 103

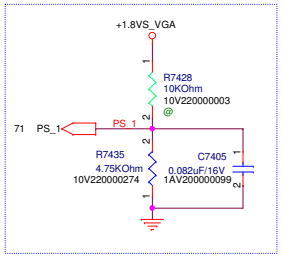
PEGATRON	Title : GPU--MEM_CTRL_CHB	
BG1/HW7	Engineer:	
Size: A	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 73 of 103	

+1.8VS_VGA +1.8VS_VGA 57,71,75,76,86,87

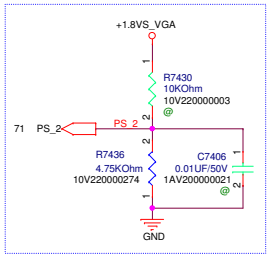
PS_0



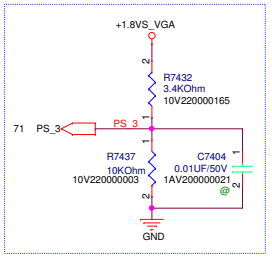
PS_1



PS_2



PS_3



PS_* config	Bits[5,4,3,2,1]
PS_0	1 1 0 0 1
PS_1	0 1 0 0 0
PS_2	1 1 0 0 0
PS_3	1 1 1 1 0

Intel SHB-U/BDW-U support up to PCIe-Gen2
PS_1[5:1]=01000
Follow 2014 VRAM List

Capacitor Value	Bits[5:4]
680nF	00
82nF	01
10nF	10
NC	11

680nF		680nF	1A20-0319600
82nF	1AV200000099	82nF	1A20-030D600
10nF	1AV200000021	10nF	1A20-0062100

R_pu(Ω)	R_pd(Ω)	Bits[3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111
0402 1% resistors are required		

2000	10V220000035	2000	1022-005J000
3240	10V220000057	3240	1022-009S100
3400	10V220000165	3400	1022-00AF000
4530	10V220000377	4530	1022-00CM000
4750	10V220000274	4750	1022-01RH000
4990	10V220000077	4990	1022-02O1000
5620	10V220000085	5620	1022-00EV000
6980	10V220000277	6980	1022-01T8100
8450	10V220000102	8450	1022-00HX000
10000	10V220000003	10000	1022-0009000

2014 VRAM List

Memory ID Board Straps

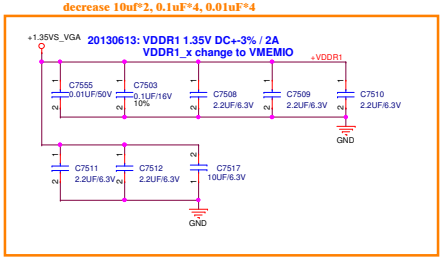
Vendor	PS_3[3:1]	ID	DDR3 Memory Type	VRAM Vendor Part	part number	R7432 R_pu	R7437 R_pd
Hynix	V 000	0	128M*16*4 pcs(1GB)	H5TC2G63FFR-11C (1800Mbps)	0315-012L0TB	NC	4750
	V 001	1	256M*16*4 pcs(2GB)	H5TC4G63AFR-11C (1800Mbps)	0315-01110TB	8450	2000
Samsung	010	2	128M*16*4 pcs(1GB)	K4W2G1646Q-BC1A (1866Mbps)	0315-01550TB	4530	2000
	011	3	256M*16*4 pcs(2GB)	K4W4G1646D-BC1A (1866Mbps)	0315-015P0TB	6980	4990
	100	4				4530	4990
	101	5				3240	5620
Micron	V 110	6	128M*16*4 pcs(1GB)	MT41K128M16JT-107G:K (1800Mbps)	0315-00YF0TB	3400	10000
	V 111	7	256M*16*4 pcs(2GB)	MT41K256M16HA-107G:E (1800Mbps)	0315-00X90TB	4750	NC

Jet/Topaz PIN STRAPS

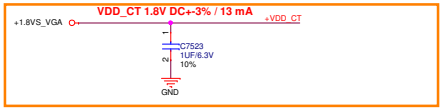
MLPS Bit	Starp Name	Description
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. V If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.
PS_1[1]	BIF_GEN3_EN_A	Re-defined strap to indicate PCIeR GEN3 capability. 1 = PCIeR GEN3 is supported. V 0 = PCIeR GEN3 is not supported.
PS_1[2]	BIF_CLK_PM_EN	PCIe Clk PM capability: 1 = CLKREQB supported V 0 = CLKREQB not supported
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.
PS_1[4]	TX_PWRS_ENB	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. V 1 = Full Tx output swing.
PS_1[5]	TX_DEEMPH_EN	PCI EXPRESSR transmitter, de-emphasis enable. V 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.
PS_2[1]	N/A	Reserved. Set to 0 or 1
PS_2[2]	N/A	Reserved. Set to 0 or 1
PS_2[3]	BIOS_ROM_EN	To enable the external BIOS ROM device. V 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.
PS_2[4]	VGA_DIS	VGA Interface disable determines whether or not the card will be recognized as the system's VGA controller. V 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.
PS_2[5]	N/A	Reserved. Set to 0 or 1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping (such as memory ID).
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. V 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.
AUD[1] AUD[0]	HSYNC VSYNC (Internal PD) not support Jet	AUD[1:0]: V 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if adapter is detected; 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

PEGATRON Title : GPU-STRAP_MISC
BG1/HW7 Engineer:
Size: Custom | Project Name: CAS(C)UG | Rev: 1.0
Date: Sunday, December 22, 2013 | Sheet 74 of 103

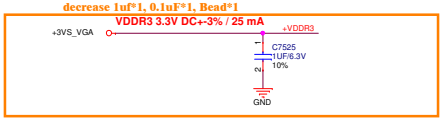
20131002: Follow checklist
decrease 10uf*2, 0.1uF*4, 0.01uF*4



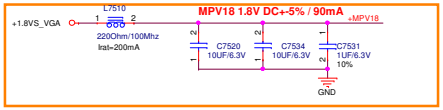
20131002: Follow checklist
decrease 10uF*1, 0.1uF*1, Bead*1



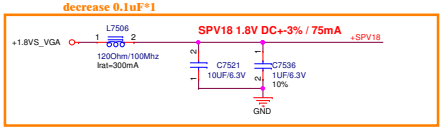
20131002: Follow checklist
decrease 1uF*1, 0.1uF*1, Bead*1



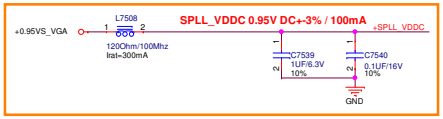
20131002: Follow checklist
decrease 0.1uF*1
add 10uF*1

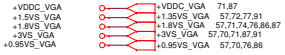


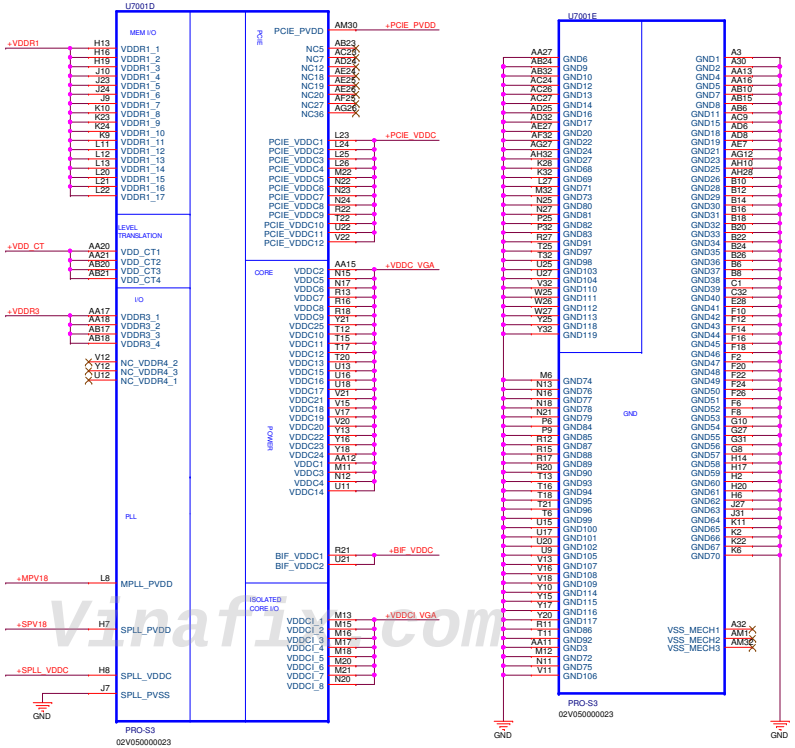
20131002: Follow checklist
decrease 0.1uF*1

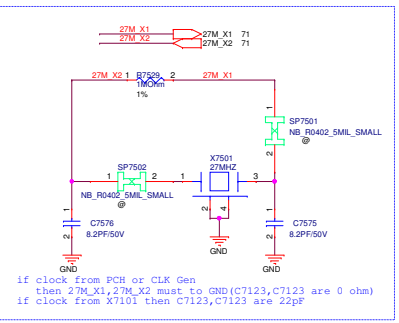


20131002: Follow checklist
decrease 10uF*1

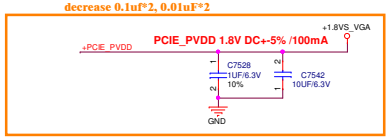




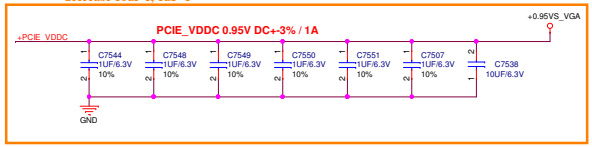




20131002: Follow checklist
decrease 0.1uf*2, 0.01uF*2

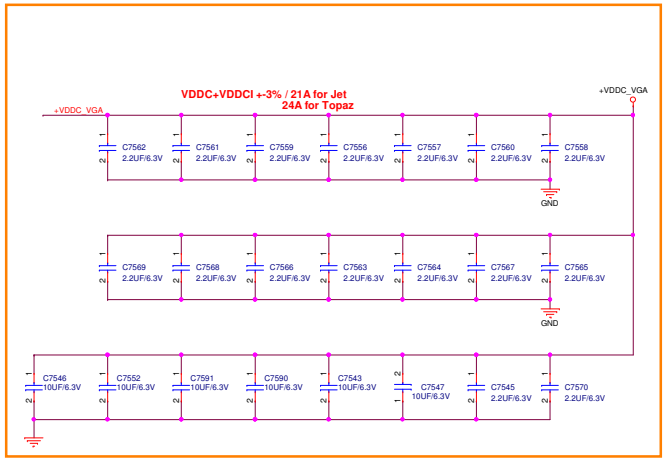


20131002: Follow checklist
decrease 10uf*1, 1uF*1

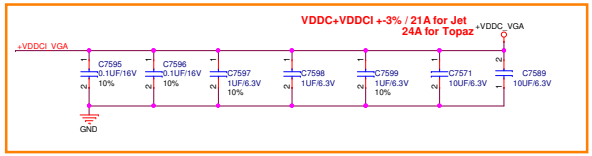


20131002: Follow checklist
decrease 10uf*1, 1uF*2
share with +PCIE_VDDC

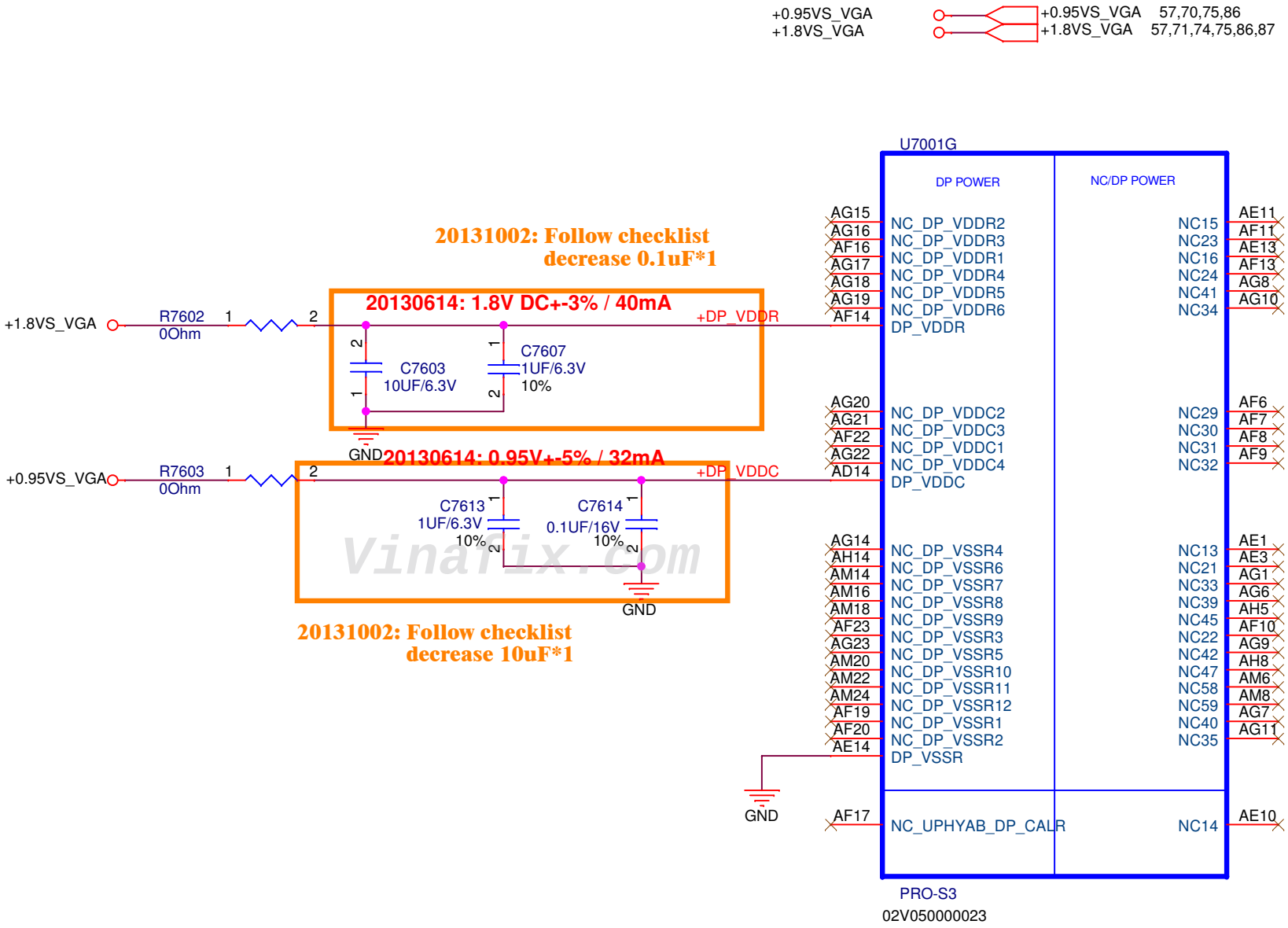
20131002: Follow checklist
decrease 1uF*6



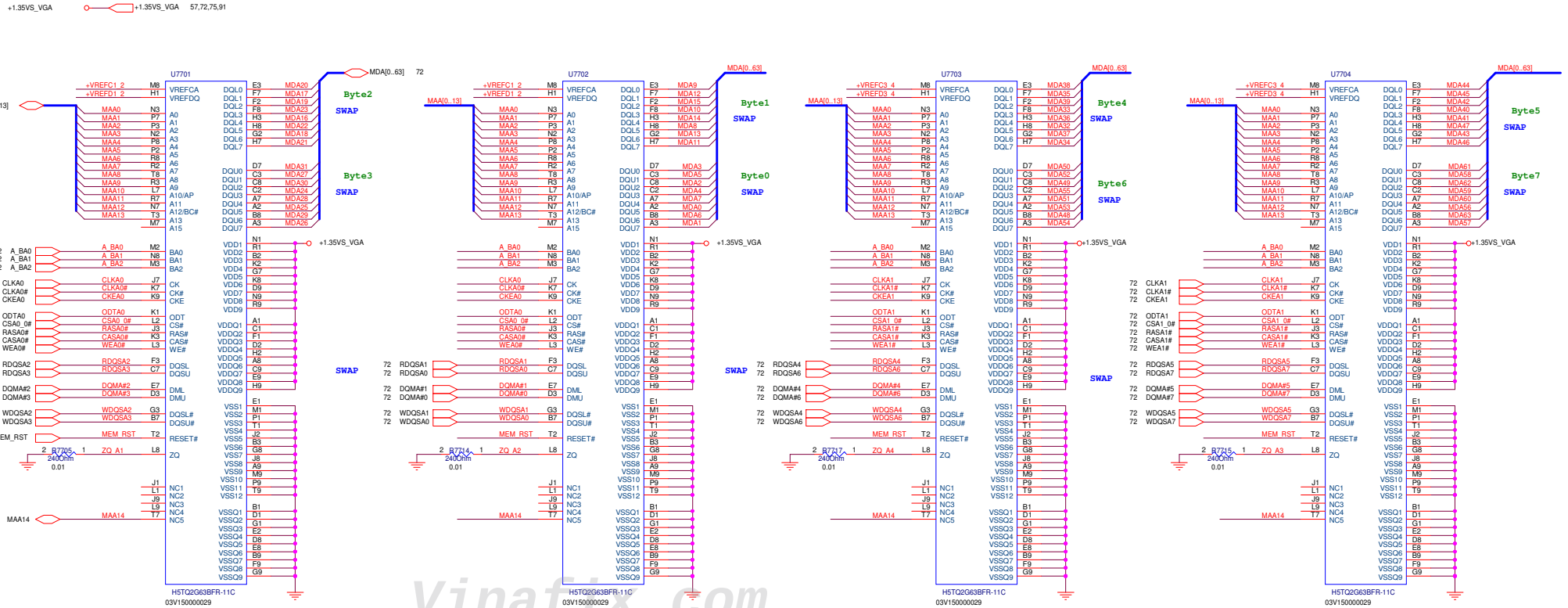
20131002: Follow checklist
Add 10uf*1, 0.1uF*2



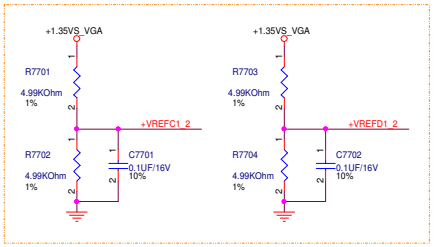
PEGATRON Title : GPU-POWER/GND
BG1/HW7 Engineer:
Size: Custom | Project Name: CAS(C)UG | Rev: 1.0
Date: Sunday, December 22, 2013 | Sheet 75 of 103



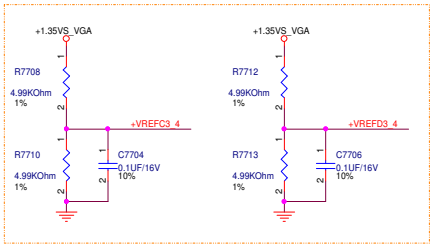
PEGATRON	Title : GPU--DP POWER	
BG1/HW7	Engineer:	
Size: A	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 76 of 103	



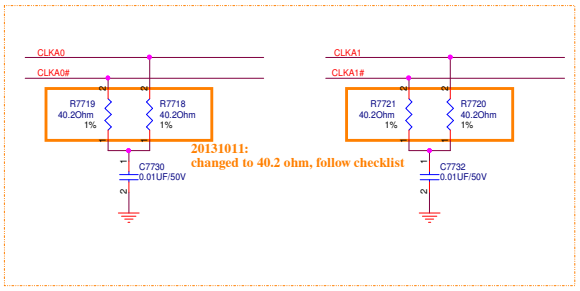
U7701,U7702 share a Verf



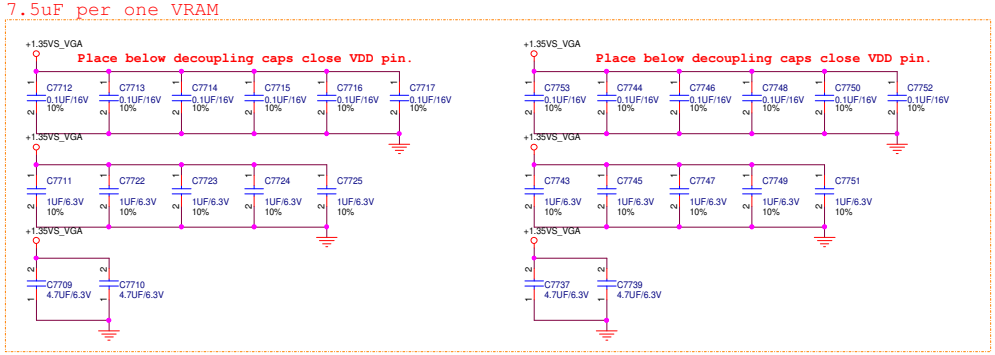
U7703,U7704 share a Verf



Vinafix.com



7.5uF per one VRAM



PEGATRON	Title : GPU-MEM CHA	
BG1/HW7	Engineer:	
Size: C	Project Name: CAS(C)UG	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 77 of 103	

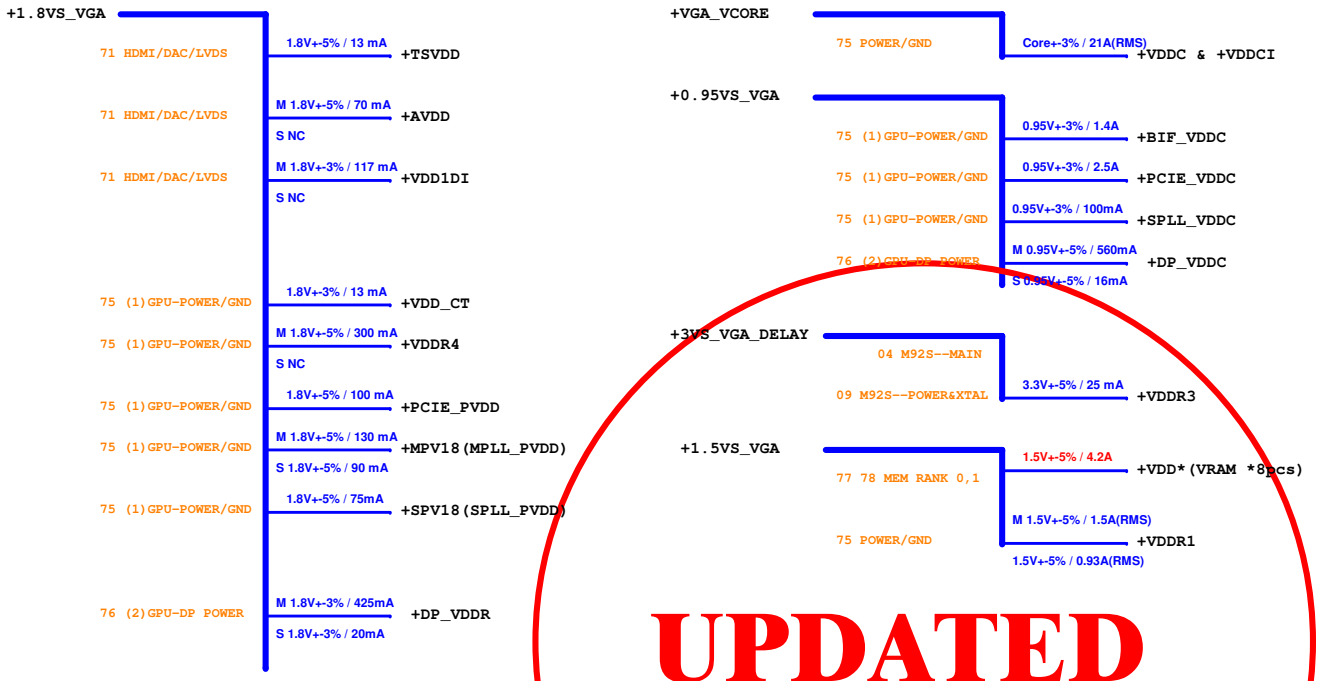
PEGATRON Title : GPU-MEM CHB

BG1/HW7 Engineer:

Size	Project Name	Rev
B	CAS(C)UG	1.0

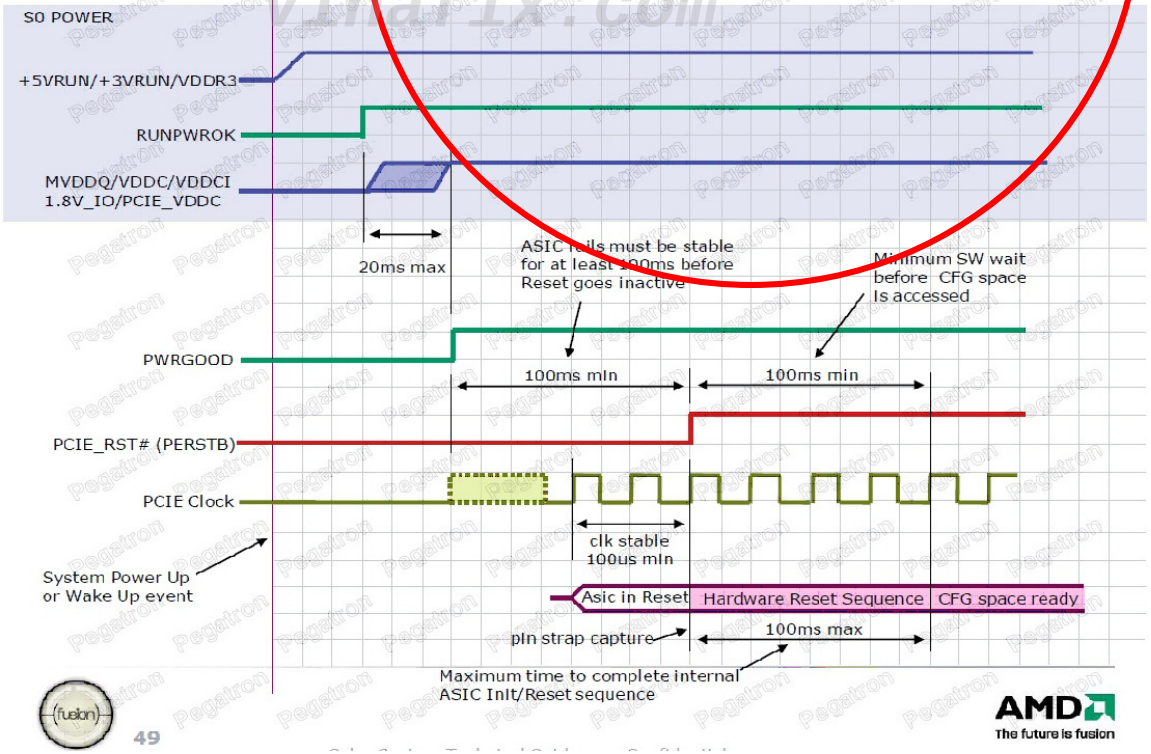
Date: Sunday, December 22, 2013 Sheet 78 of 103

AMD Jet/Topaz Power Rail/Power Sequence



UPDATED

POWER UP RESET SEQUENCE (COLD BOOT)



AMD
The future is fusion

<Core Design>

PEGATRON Title : GPU-POWER FLOW

BG1/HW7 Engineer: Fenix Chen

Size	Project Name	Rev
C	CAS(C)UG	2.1

Date: Sunday, December 22, 2013 Sheet 79 of 103

Crescent Bay 15W CPU

Reserved for compensating IOUT Accurancy
Put R8036 and R8035, R8037 close to R8024

+AC_BAT_SYS
R8036 @ 2MOHM 5% vx_r0402_small
R8035 @ 2MOHM 5% vx_r0402_small
VRM_OCP-I
R8037 @ 27KOhm 1% vx_r0402_small

The R8008 closes to U8001

R8001, R8002, R8004, R8005 are putted together and The R8005 closes to L8000

Differential pair

For Terraira IFDIM test

VR_HOT is adopted, if R8008 and C8018 are stuffed

VR_SVID_ALERT# between VR_SVID_CLK and VR_SVID_DATA

Layout

USR level selection

NOTE 2
OSR level selection

NOTE 1
OSR Enable

U8000A TPS51624RSM

U8000B TPS51624RSM

U8001A CSD97376Q4M

U8001B CSD97376Q4M

C8001 :330pF,470pF

VCORE(15W)
TDC :10A
PL2 :14A
Frequency :1.2MHz
PWR Cap. :264uF(22uF * 12 PCS)
EE Cap. : --uF(22uF * 0 PCS)
Total Cap. :264uF (22uF * 12 PCS) => as follow OSR Setting

(3.5A)

DCR=0.62± 5%

+VCORE

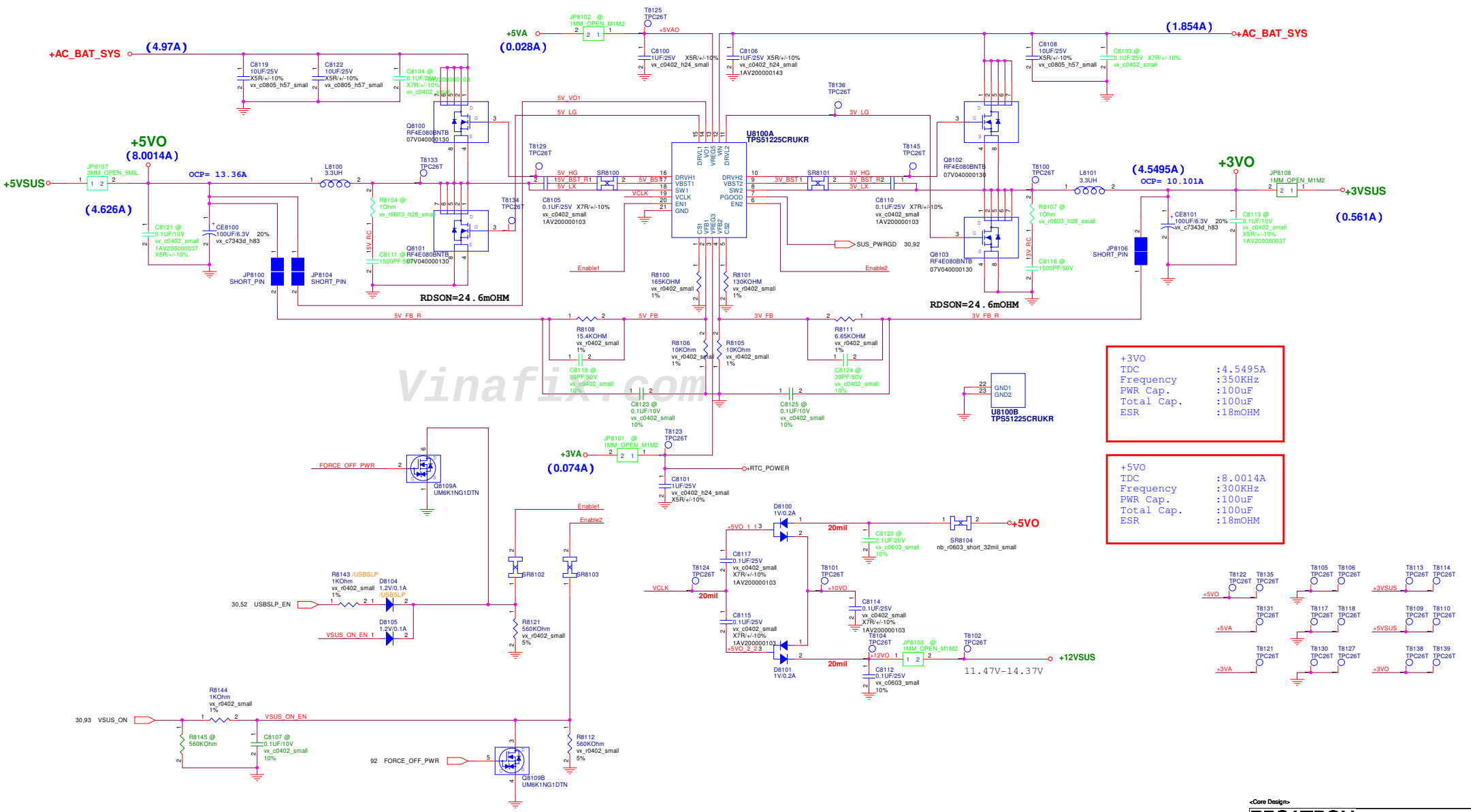
NOTE 1 and 2 : OSR Setting and Quantity on EVM board(15W)

Enable OSR	R8027	R8029	Number of Cap.(PWR + EE) 22uF/6.3V/0805	22uF/6.3V/0603
ON	20Kohm	100Kohm	≧10	≧12
OFF	20Kohm	@	≧12	≧14

Number of Cap. is depended on measured results
Please verify and keep the design margin of "Overshoot" and "Ripple" ≧15%
Related reference:
\\10.195.65.166\power\9.Everest Project\2014 Everest\Test Report

<Core Design>
PEGATRON Title : POWER_VCORE
Engineer: Adams Lin
Size: Custom | Project Name: CACUG/CASUG | Rev: 1.0
Date: Sunday, December 22, 2013 | Sheet 80 of 103

+5VO & +3VO POWER SUPPLY



<Core Design>

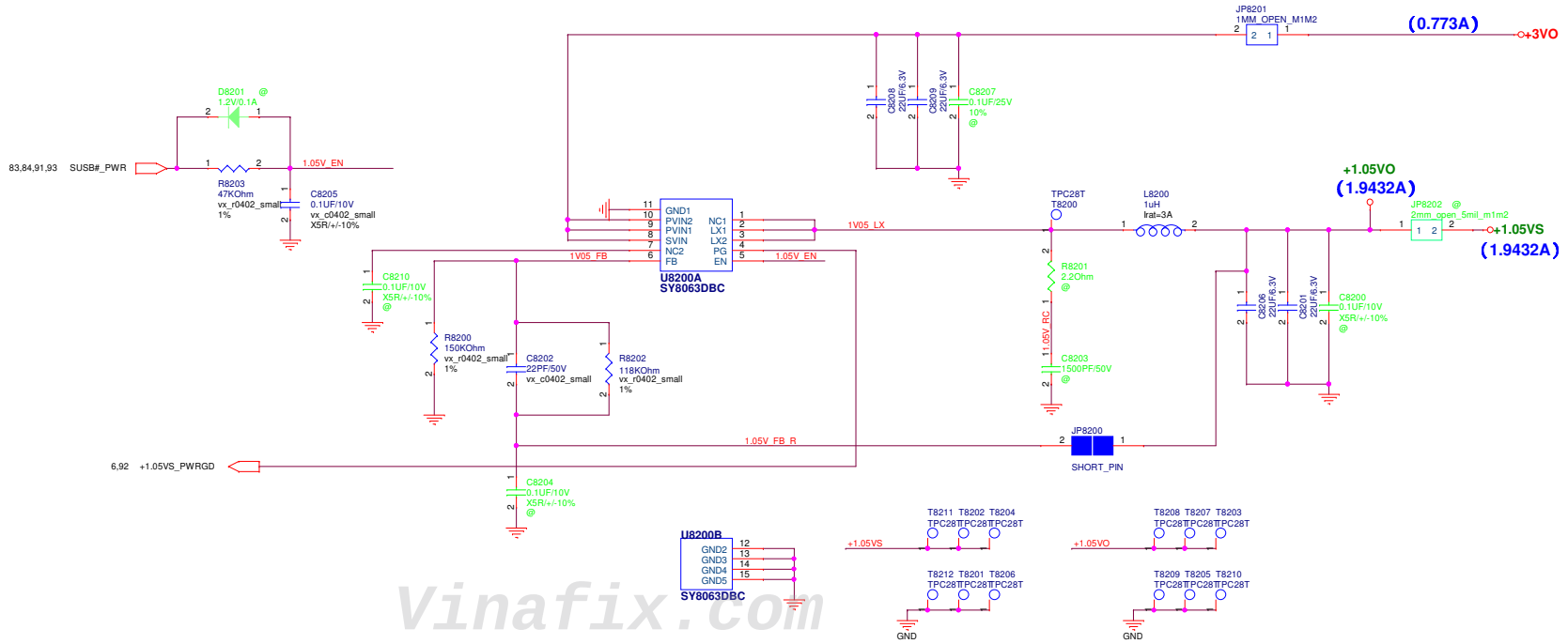
PEGATRON Title : POWER_SYSTEM

Engineer: Adams Lin

Size	Project Name	Rev
Custom	CACUG/CACSG	1.0

Date: Sunday, December 22, 2013 Sheet 81 of 103

+1.05VS POWER SUPPLY



+1.05VO	
TDC	:1.9432A
Frequency	:1MHz
PWR Cap.	:44uF
Total Cap.	:44uF

<Core Design>

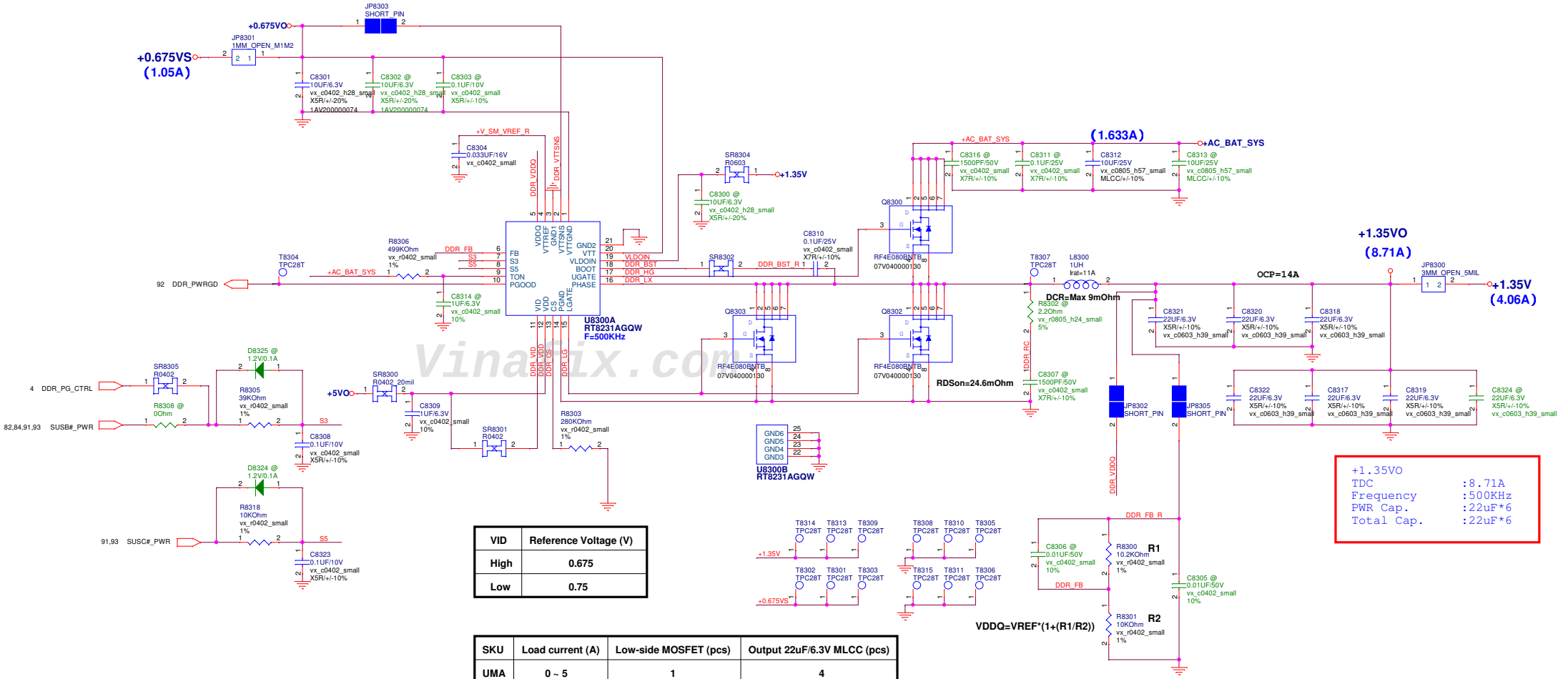
PEGATRON Title : POWER_+1.05VS

BG1-HW3 Engineer: Adams Lin

Size	Project Name	Rev
Custom	CACUG/CASUG	2.0

Date: Sunday, December 22, 2013 Sheet 82 of 103

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

<Core Design>

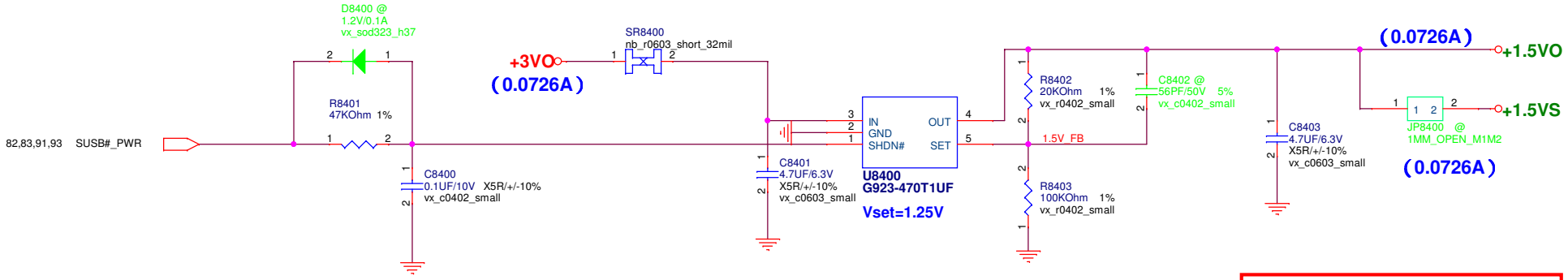
PEGATRON Title : POWER_DDR & VTT

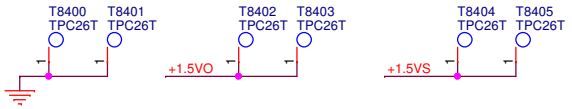
Engineer: Adams Lin

Size	Project Name	Rev
Custom	CACUG/CACSG	1.0

Date: Sunday, December 22, 2013 Sheet 83 of 103

1.5VS POWER SUPPLY





+1.5VS
MAX current :0.0726A
PWR Cap. :4.7uF
EE Cap. :xxuF
Total Cap. :xxuF

<Core Design>

PEGATRON Title : POWER_+1.5V

Engineer: Adams Lin

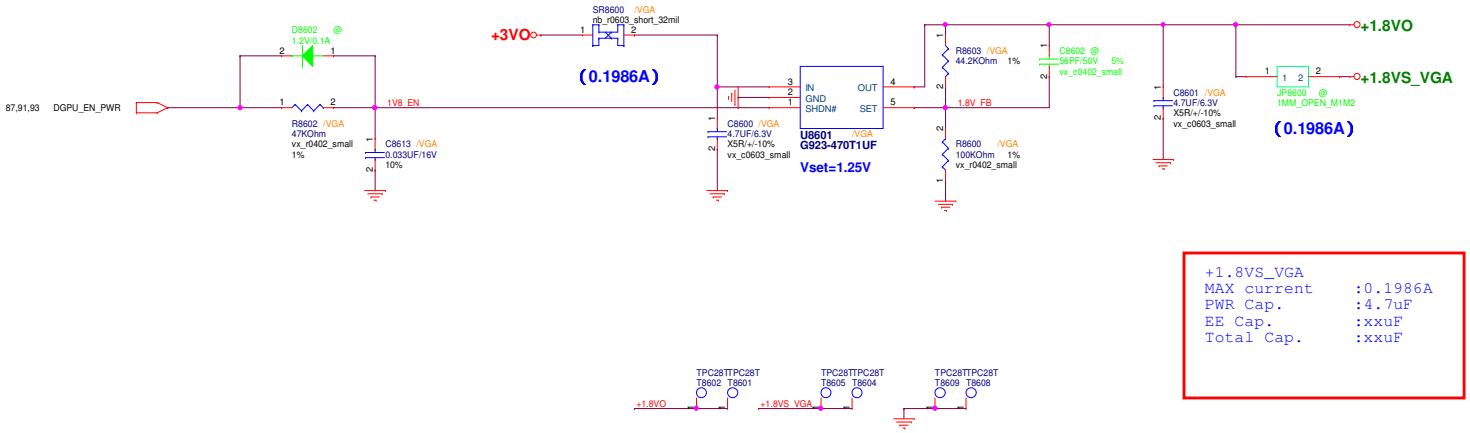
Size	Project Name	Rev
B	CACUG/CACSG	1.0

Date: Sunday, December 22, 2013 Sheet 84 of 103

<Core Design>

Title: <Title>		
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Sunday, December 22, 2013	Sheet 85 of 103	

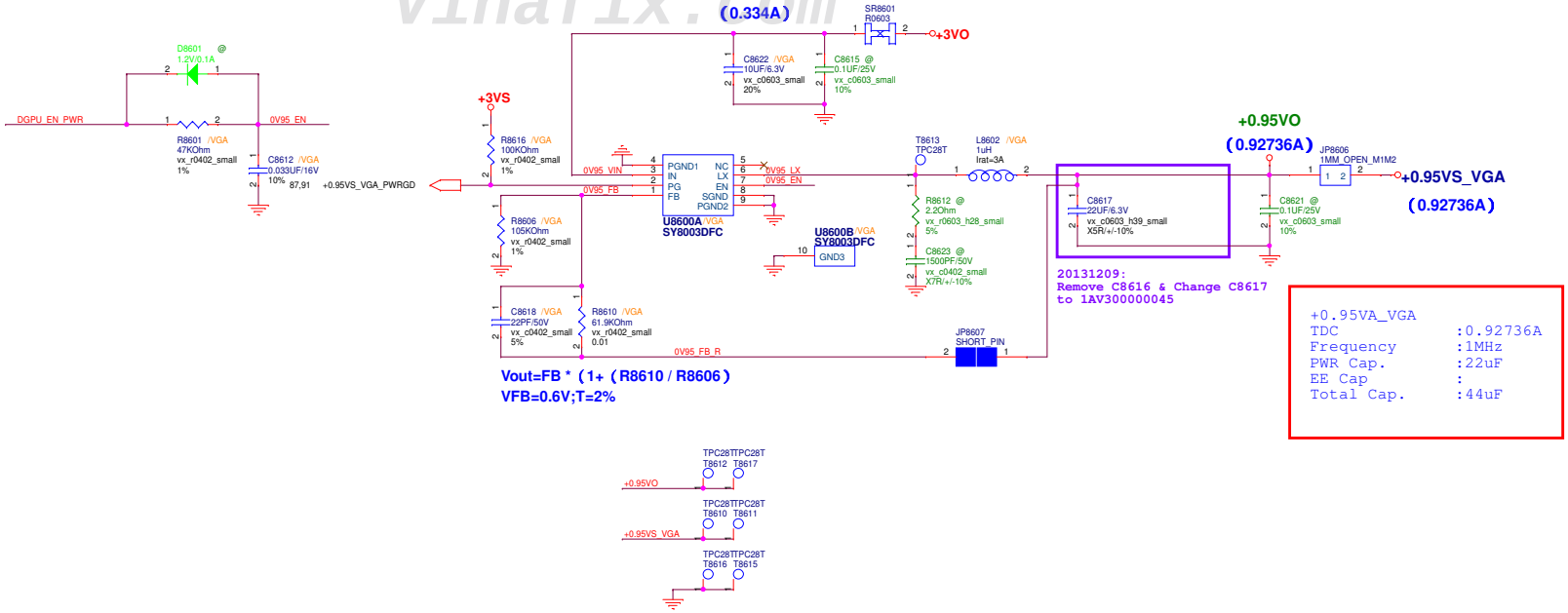
1.8VS_VGA POWER SUPPLY



+1.8VS_VGA
MAX current :0.1986A
PWR Cap. :4.7uF
EE Cap. :xxuF
Total Cap. :xxuF

TPC28TTPC28T T8602 T8601 +1.8VO
TPC28TTPC28T T8605 T8604 +1.8VS_VGA
TPC28TTPC28T T8609 T8608

+0.95VS_VGA POWER SUPPLY



+0.95VA_VGA
TDC :0.92736A
Frequency :1MHz
PWR Cap. :22uF
EE Cap :
Total Cap. :44uF

TPC28TTPC28T T8612 T8617 +0.95VO
TPC28TTPC28T T8610 T8611 +0.95VS_VGA
TPC28TTPC28T T8616 T8615

<Core Design>
PEGATRON Title :+1.8V & +0.95V
Engineer: Adams Lin
Size: Custom | Project Name: CACUG/CACSG | Rev: 1.1
Date: Sunday, December 22, 2013 | Sheet 86 of 103

VGA_CORE POWER SUPPLY

18W	18W
Jet	Topaz
SVID	SVID
Voltage Level 3.3V	Voltage Level 1.8V

Jet (S3) PRO (18W)
VDDC & VDDCI Merged:0.8V ~ 1.075V
TDC:21A EDC:31.5A
Load Line:N/A OCP>40.95A
DC Tol.:+-3%
AC Tol.:+-5%

Split VDDCI:4.5A => Merged VDDCI: ? A

Topaz (S3) XT (18W)
VDDC & VDDCI Merged:0.8V ~ 1.1V
TDC:24A EDC:36A
Load Line:N/A OCP>46.8A
DC Tol.:+-?%
AC Tol.:+-?%

Flow into VDDCI: ? A

1 Phase-> Chock 0.36uH 064T/DCR 1.4mohm
2 Phase-> Chock 0.47uH 063T/DCR 4.2mohm

2-Bit Boot VID Code :

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SIRA14:Rdson MAx 8.5 mOHM

RT8880AGQW FREQ SET : 350K Hz

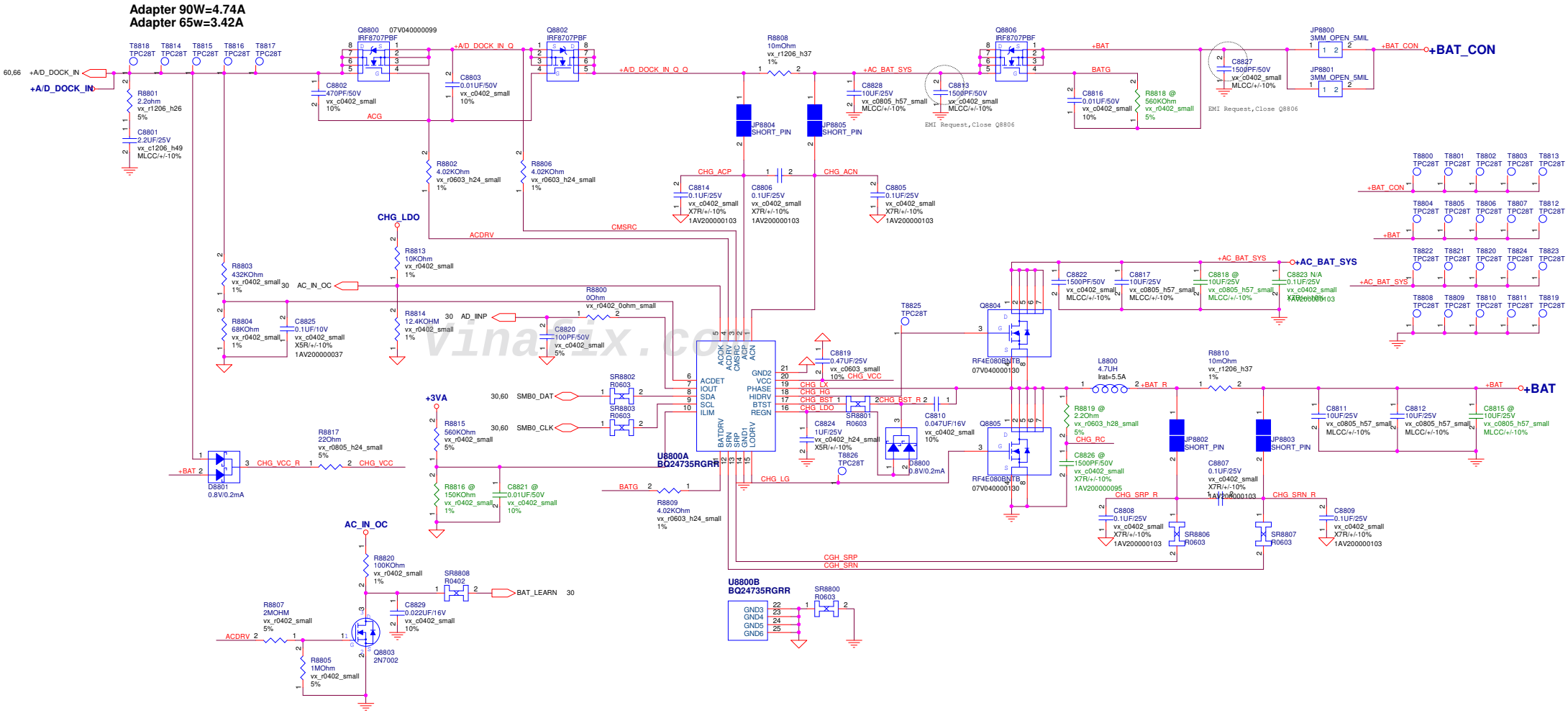
SIRA14:Rdson MAx 8.5 mOHM

Input current=3.2A

Jet/Topaz 18W
+VGA_VCORE_O
TDC :19.2A
Frequency :350KHz
PWR Cap. :940uF
Total Cap. :940uF
ESR :3mOHM

<Core Design>
PEGATRON Title : +VDDC_VGA
Engineer: Adams Lin
Size: Custom | Project Name: CACUG/CACSG | Rev: 1.0
Date: Sunday, December 22, 2013 | Sheet 87 of 103

BATTERY CHARGER



<Core Design>

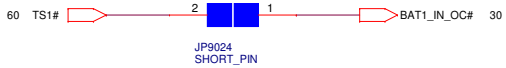
PEGATRON Title : POWER_N/A

Engineer:

Size	Project Name	Rev
A		1.1

Date: Sunday, December 22, 2013 Sheet 89 of 103

BATTERY IN DETECT



<Core Design>

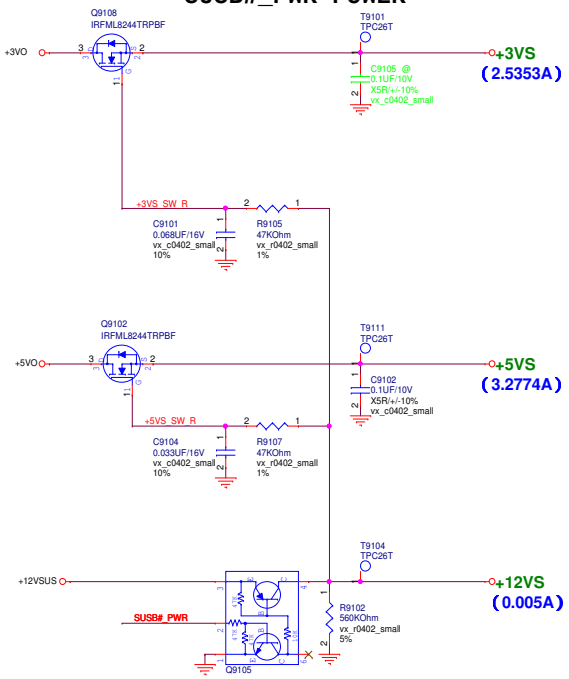
PEGATRON Title : POWER_DETECT

Engineer: Adams Lin

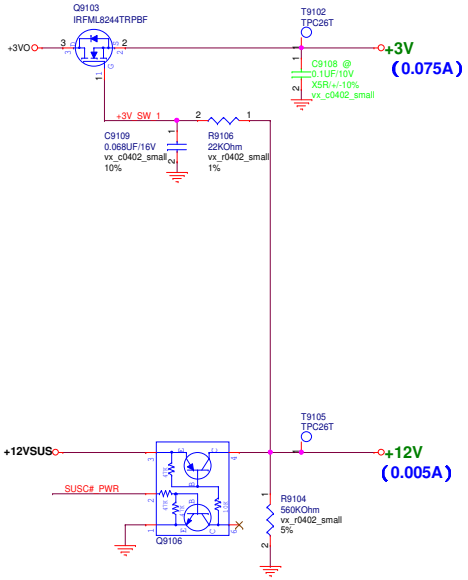
Size	Project Name	Rev
Custom	CACUG/CACSG	1.1

Date: Sunday, December 22, 2013 Sheet 90 of 103

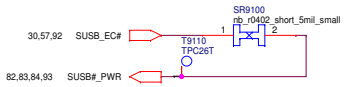
SUSB#_PWR POWER



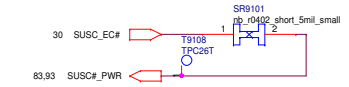
SUSC#_PWR POWER



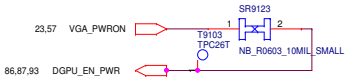
SUSB#_PWR POWER Control



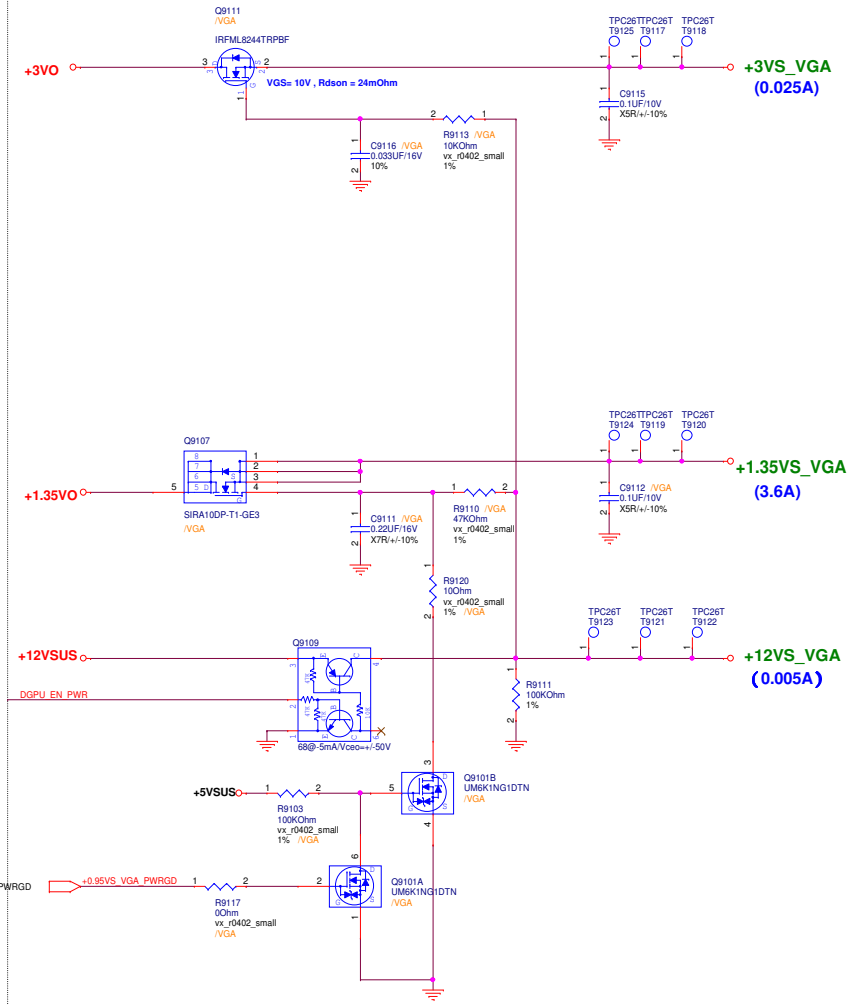
SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



VGA_VRON_PWR_PWR POWER



<Core Design>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Adams Lin

Size	Project Name	Rev
C	CACUG/CACSG	1.0

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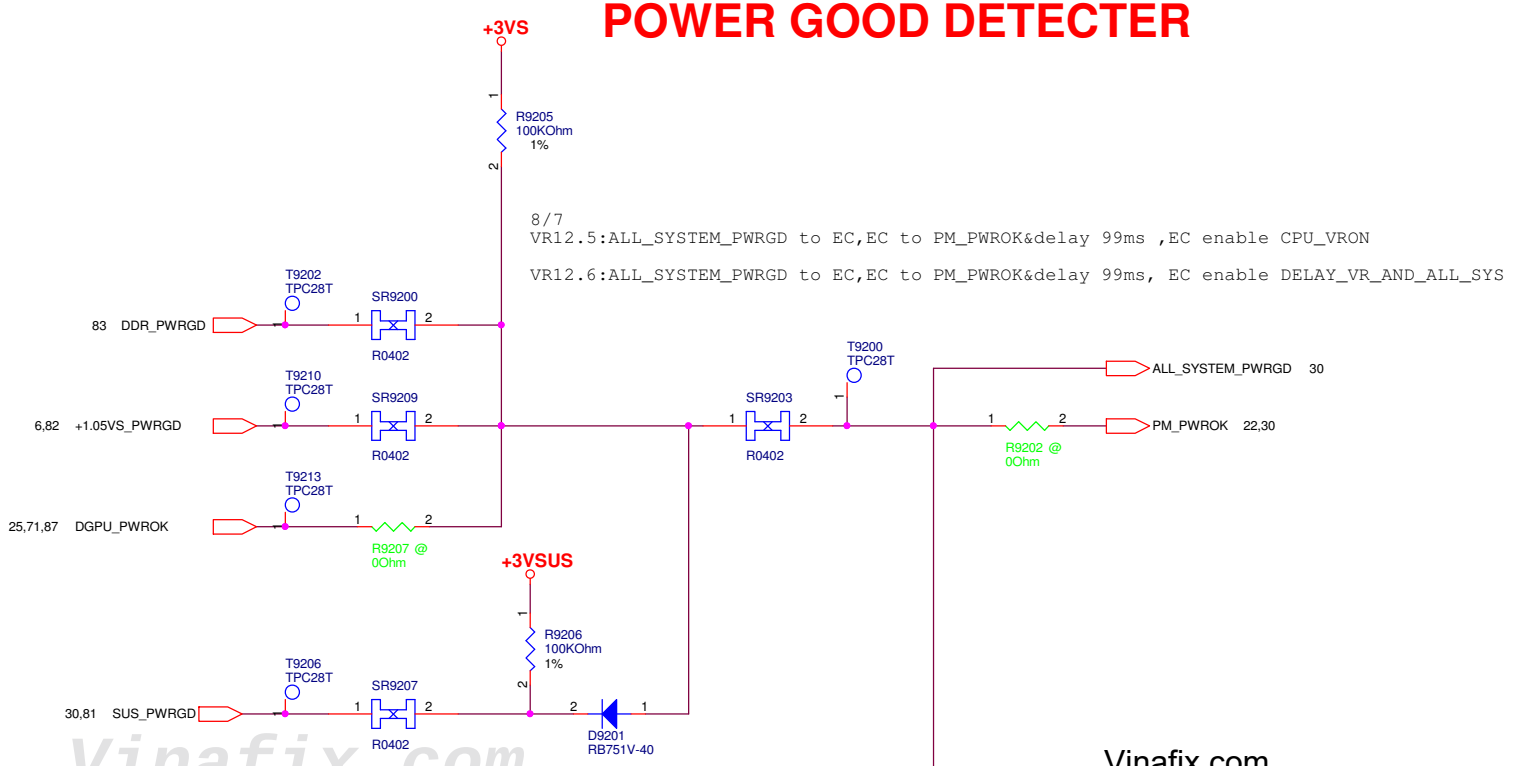
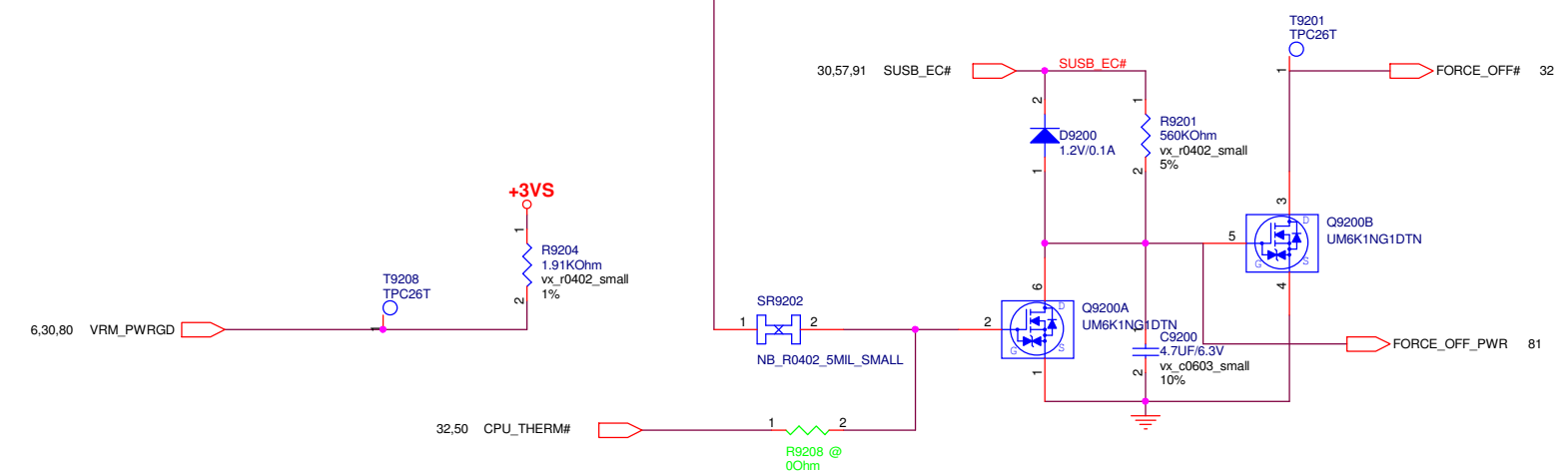
POWER GOOD DETECTER



Vinafix.com



<Core Design>

PEGATRON Title : POWER_PROTECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	CACUG/CACSG	1.0

Date: Sunday, December 22, 2013 Sheet 92 of 103

+A/D_DOCK_IN → +A/D_DOCK_IN 60,66,88

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,83,87,88

+BAT_CON → +BAT_CON 60,88

+BAT → +BAT 88

+5VA → +5VA 56,66,81

+3VA → +3VA 20,26,30,33,56,57,60,66,81,88

+5VO → +5VO 81,83,91

+3VO → +3VO 81,82,84,86,91

+1.8VO → +1.8VO 86

+1.5VO → +1.5VO 84

+1.35VO → +1.35VO 83,91

+1.05VO → +1.05VO 82

+0.95VO → +0.95VO 86

+0.675VO → +0.675VO 83

+12VSUS → +12VSUS 26,33,51,81,91

+5VSUS → +5VSUS 4,26,51,52,56,66,81,91

+3VSUS → +3VSUS 22,26,28,30,33,36,53,63,81,92

+3VS_VGA → +3VS_VGA 57,70,71,75,87,91

+1.35VS_VGA → +1.35VS_VGA 57,72,75,77,91

+12V → +12V 91

+3V → +3V 22,25,31,44,45,91

+1.35V → +1.35V 4,6,16,18,83

+12VS → +12VS 25,28,31,63,66,91

+5VS → +5VS 30,31,36,46,50,51,56,57,61,66,80,87,91

+3VS → +3VS 4,6,16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,40,45,46,50,51,53,57,61,62,63,66,80,86,91,92

+1.5VS → +1.5VS 26,36,66,84

+1.05VS → +1.05VS 6,25,26,32,80,82

+0.675VS → +0.675VS 16,17,83

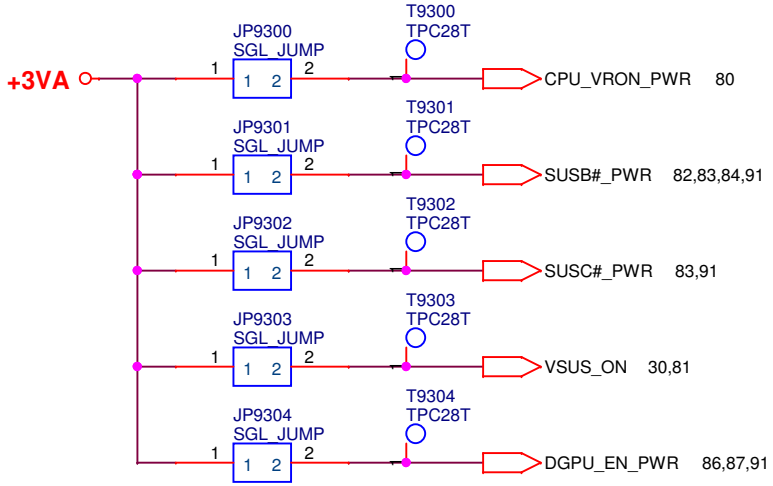
+1.8VS_VGA → +1.8VS_VGA 57,71,74,75,76,86,87

+0.95VS_VGA → +0.95VS_VGA 57,70,75,76,86

+VDDC_VGA → +VDDC_VGA 71,75,87

+VCORE → +VCORE 6,80

FOR POWER TEST



<Core Design>

PEGATRON Title : POWER_SIGNAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	CACUG/CACSG	1.0

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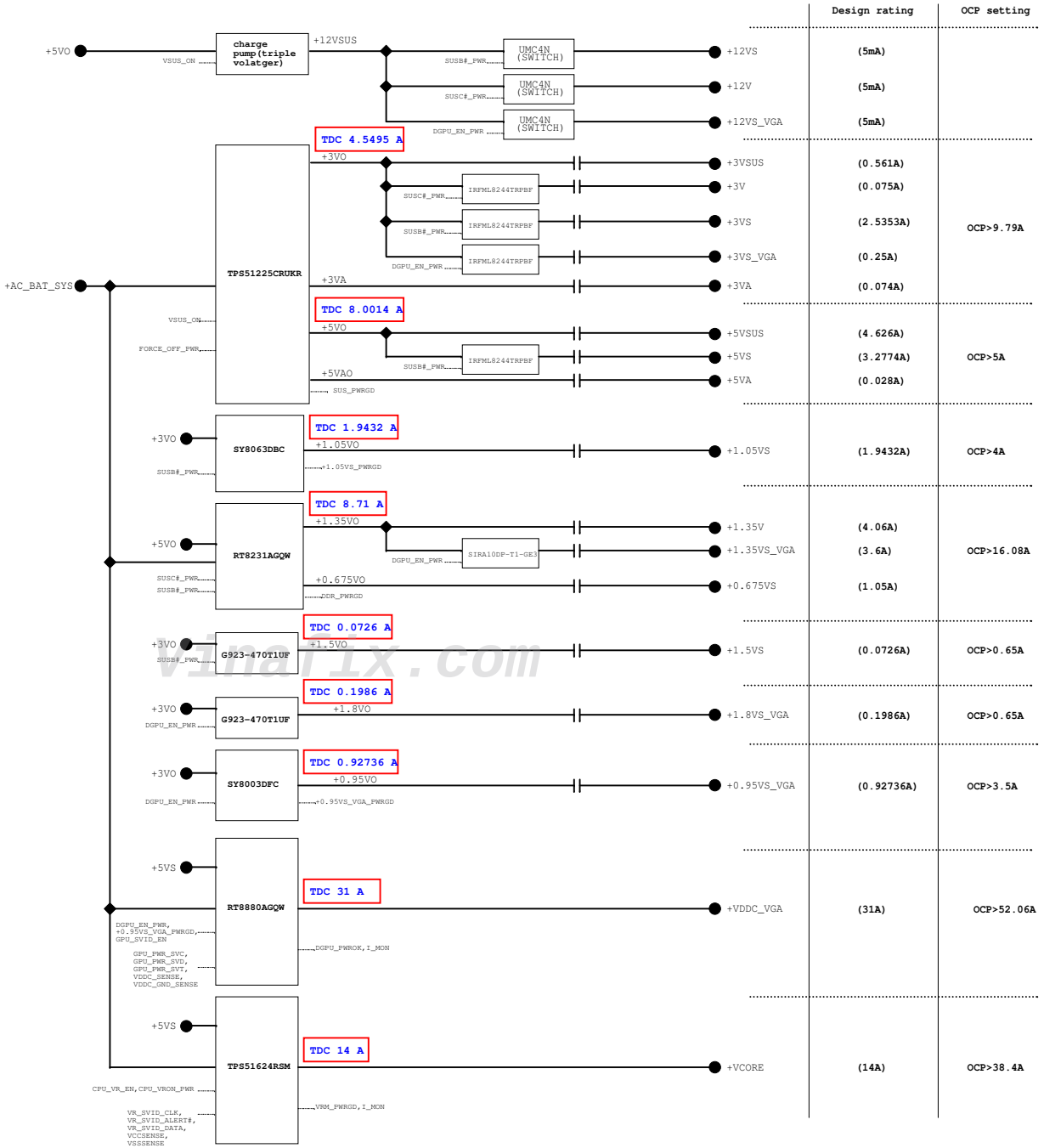

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PEGATRON Title : POWER_FLOWCHART
Engineer: N/A
Size: D | Project Name: Crescent Bay U | Rev: 1.0
Date: Sunday, December 22, 2013 | Sheet 94 of 103

<Core Design>

Title: <Title>		
Size: C	Document Number: <Doc>	Rev: <RevCode>
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Title <Title>		
Size C	Document Number <Doc>	Rev <RevCode>
Date: Sunday, December 22, 2013	Sheet 96 of 103	

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Title <Title>		
Size C	Document Number <Doc>	Rev <RevCode>
Date: Sunday, December 22, 2013	Sheet 97 of 103	

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Title: <Title>		
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Sunday, December 22, 2013	Sheet 98 of 103	

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Title <Title>		
Size C	Document Number <Doc>	Rev <RevCode>
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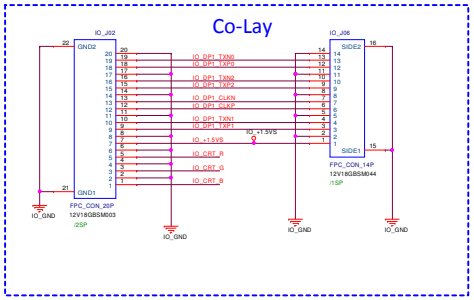
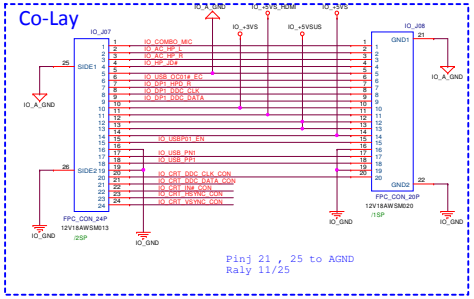
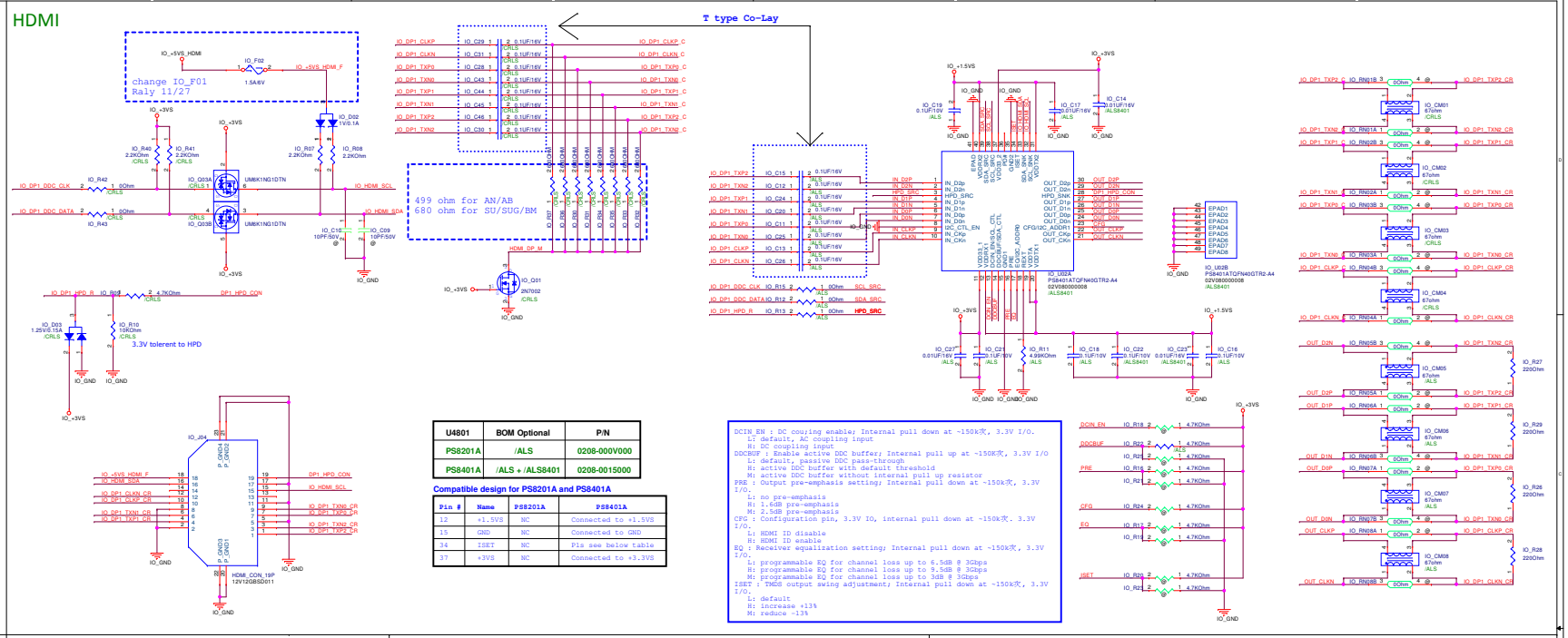
Co-Lay



Co-Lay



HDMI



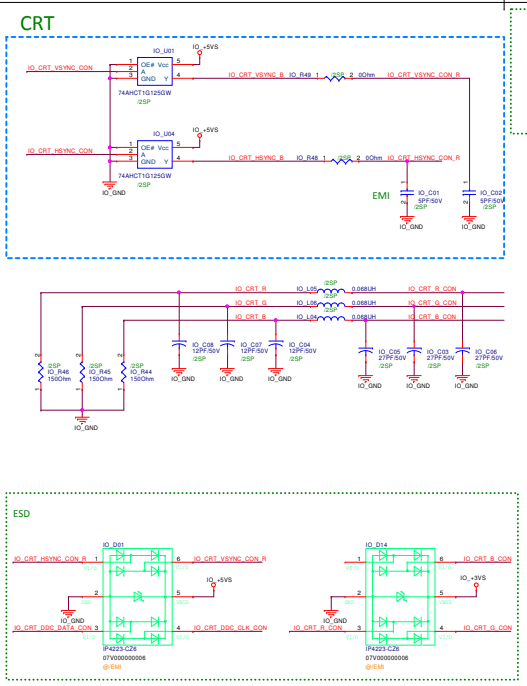
U4801	BOM Optional	P/N
PS8201A	/ALS	0208-000V000
PS8401A	/ALS + /ALS8401	0208-0015000

Compatible design for PS8201A and PS8401A

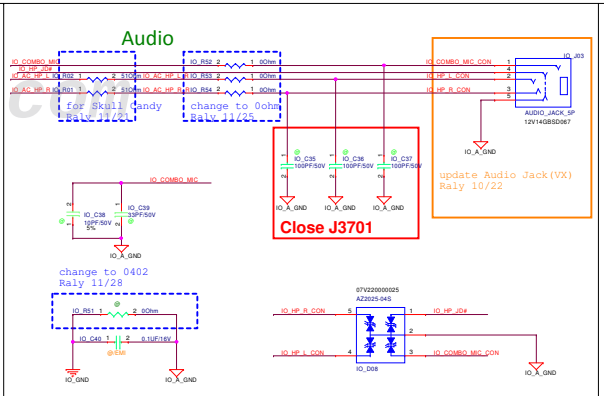
Pin #	Name	PS8201A	PS8401A
12	+1.5VS	NC	Connected to +1.5VS
15	GND	NC	Connected to GND
14	ISET	NC	Pin see below table
17	+3VS	NC	Connected to +3.3VS

DCIN_EN : DC couring enable; Internal pull down at ~150kℵ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input
DDCBUF : Enable active DDC buffer; Internal pull up at ~150kℵ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
H: active DDC buffer without internal pull up resistor
PRE : Output pre-emphasis setting; Internal pull down at ~150kℵ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
H: 2.5dB pre-emphasis
CFG : Configuration pin, 3.3V IO, internal pull down at ~150kℵ. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
EQ : Receiver equalization setting; Internal pull down at ~150kℵ, 3.3V I/O.
L: programmable EQ for channel loss up to 6.5dB @ 3Gbps
H: programmable EQ for channel loss up to 9.5dB @ 3Gbps
H: programmable EQ for channel loss up to 3dB @ 3Gbps
ISET : TMDS output swing adjustment; Internal pull down at ~150kℵ, 3.3V I/O.
L: default
H: increase +13%
H: reduce -13%

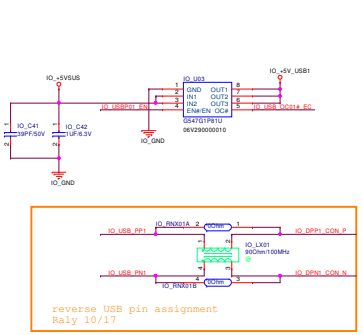
CRT



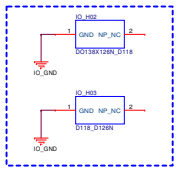
Audio

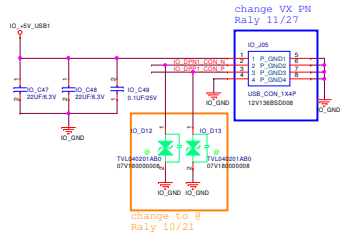


USB



Screw Hole





PEGATRON

Title : IO_USB

Engineer: Raly_Hsieh

Size	Project Name	Rev
D	PIN	1.0

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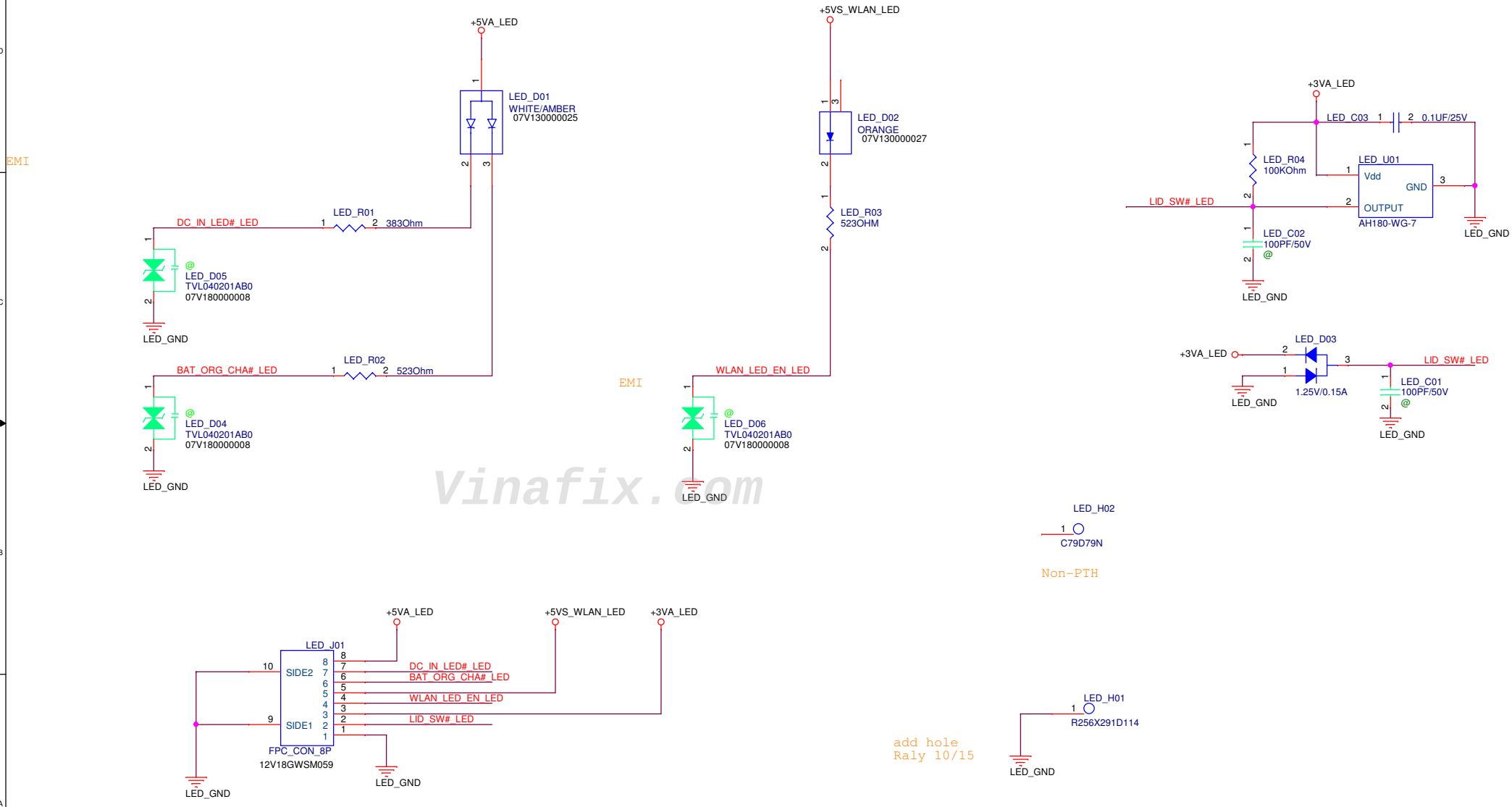

<Core Design>

PEGATRON Title : LED_DB

Engineer: Raly_Hsieh

Size	Project Name	Rev
B	CA	1.0

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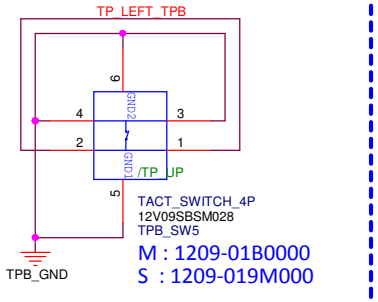
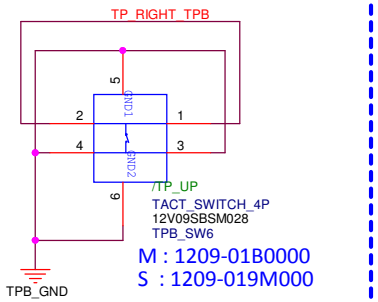
up side
Raly 11/21

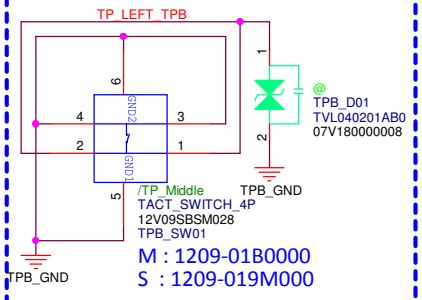


M : 1209-01B0000
S : 1209-019M000



M : 1209-01B0000
S : 1209-019M000

Middle side
Raly 10/21



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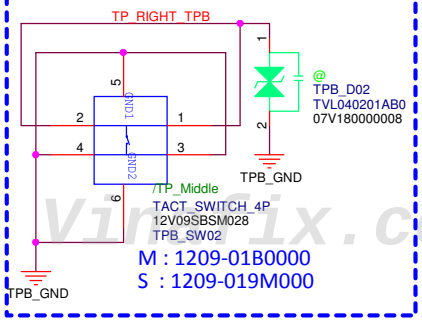

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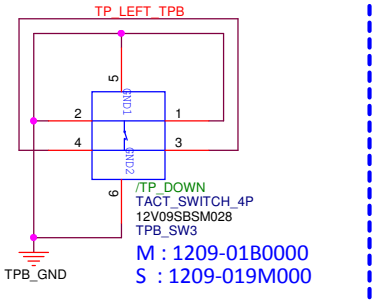
Down side
Raly 11/21



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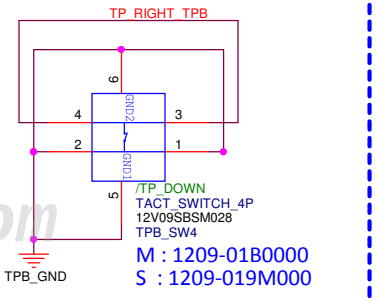

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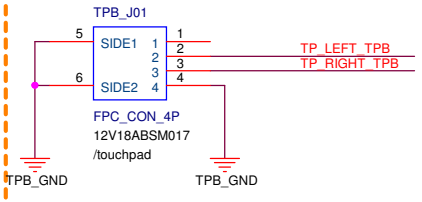
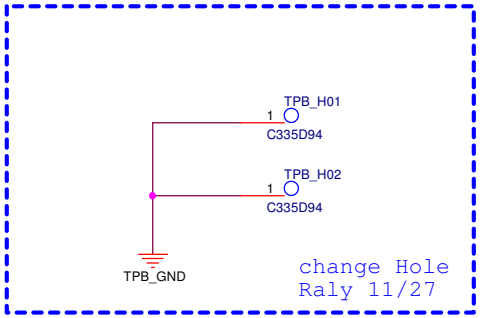
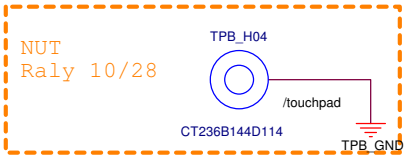
follow Connector list
Raly 11/14





change Hole
Raly 11/27

NUT
Raly 10/28



<Core Design>

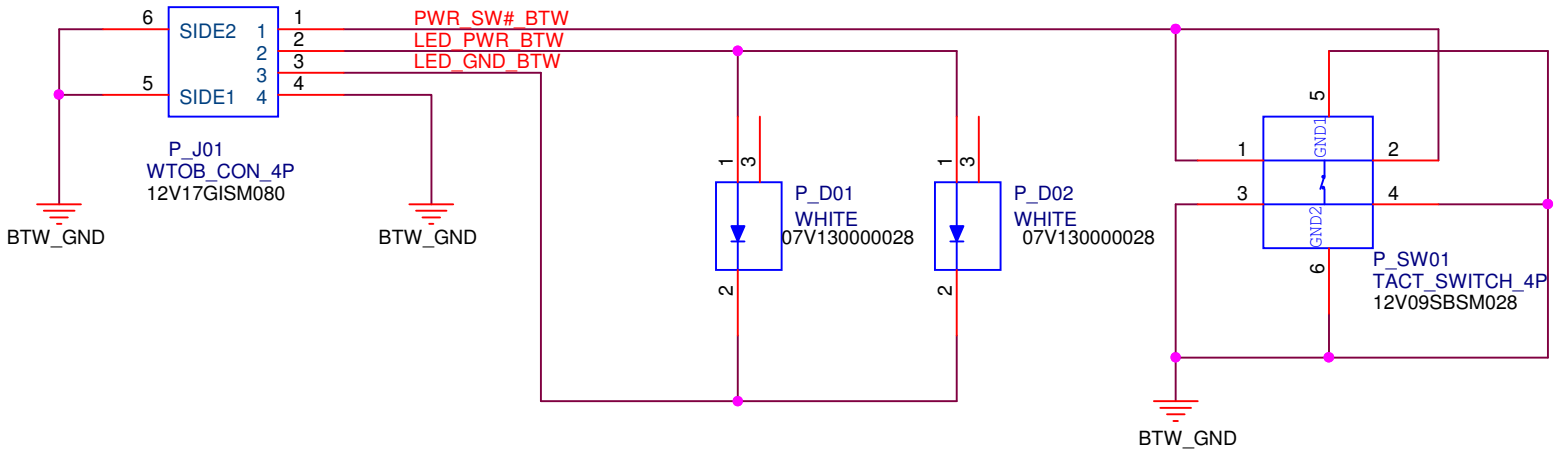
PEGATRON Title : TP_button

<OrgName> Engineer: Raly_Hsieh

Size	Project Name	Rev
B	CA10	1.0

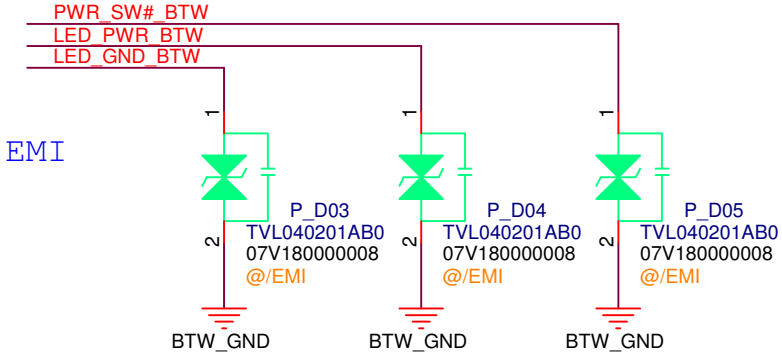
Date: Sunday, December 22, 2013 Sheet 102 of 103

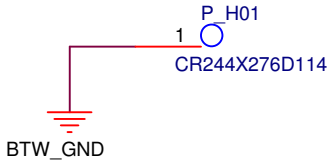
need to check with ME



Vinafix.com

change SW follow ME connector list
Raly 10/14





PEGATRON	Title : Power_BD	
BG1\HW Center	Engineer: Dean Wu	
Size: A	Project Name: CAFU	Rev: 1.0
Date: Sunday, December 22, 2013	Sheet 103 of 103	