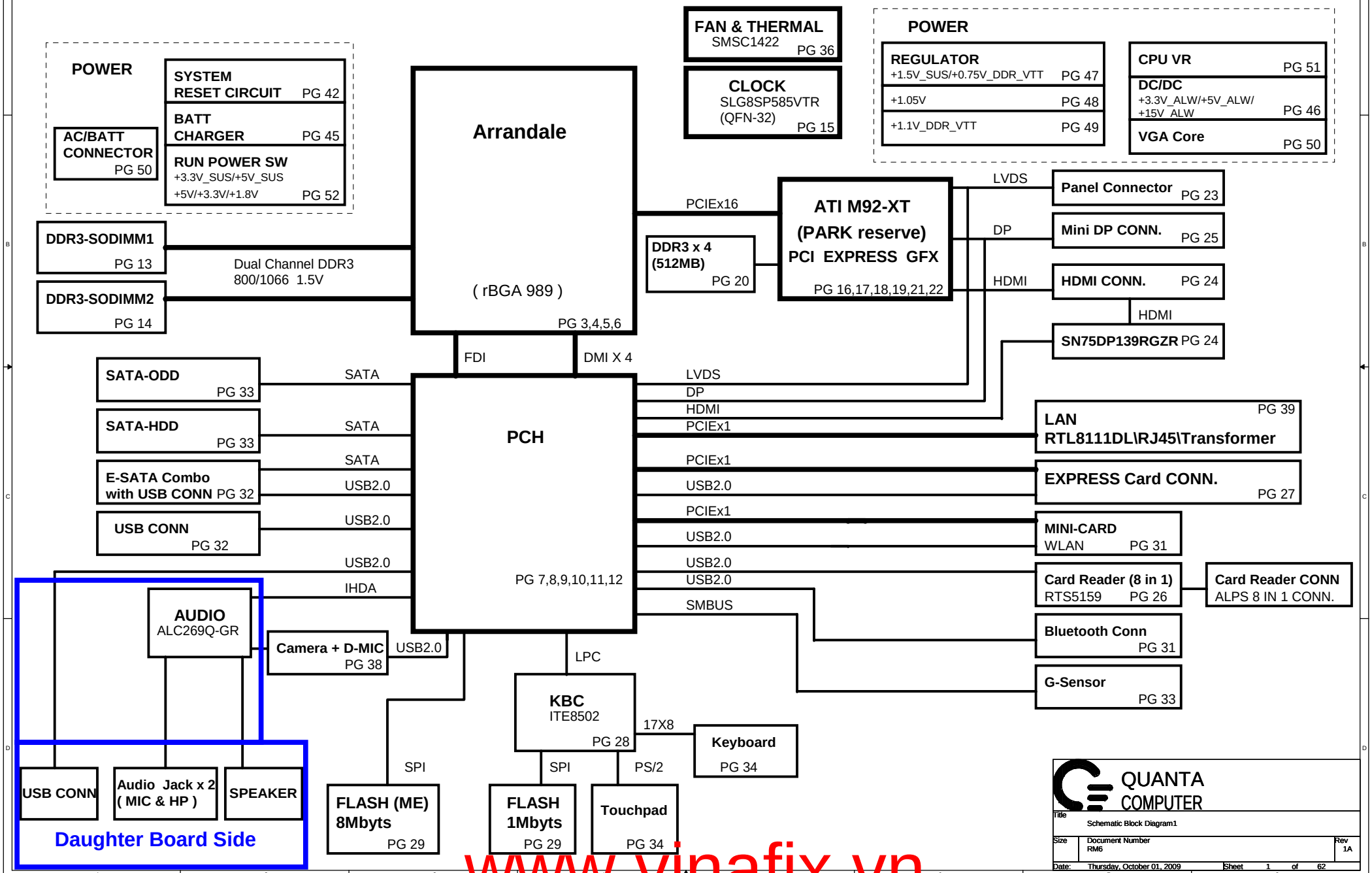
RM6 Intel UMA and Discrete GFX

VER : 1A
PWA:
PWB:



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+3.3V	13,33,37,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,59,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
GND_CHG	46	
GND_1.05V	47	
GND_VGA	50	
GND_SIGNAL	51	
AGND_DC/DC	52	
GND	ALL	

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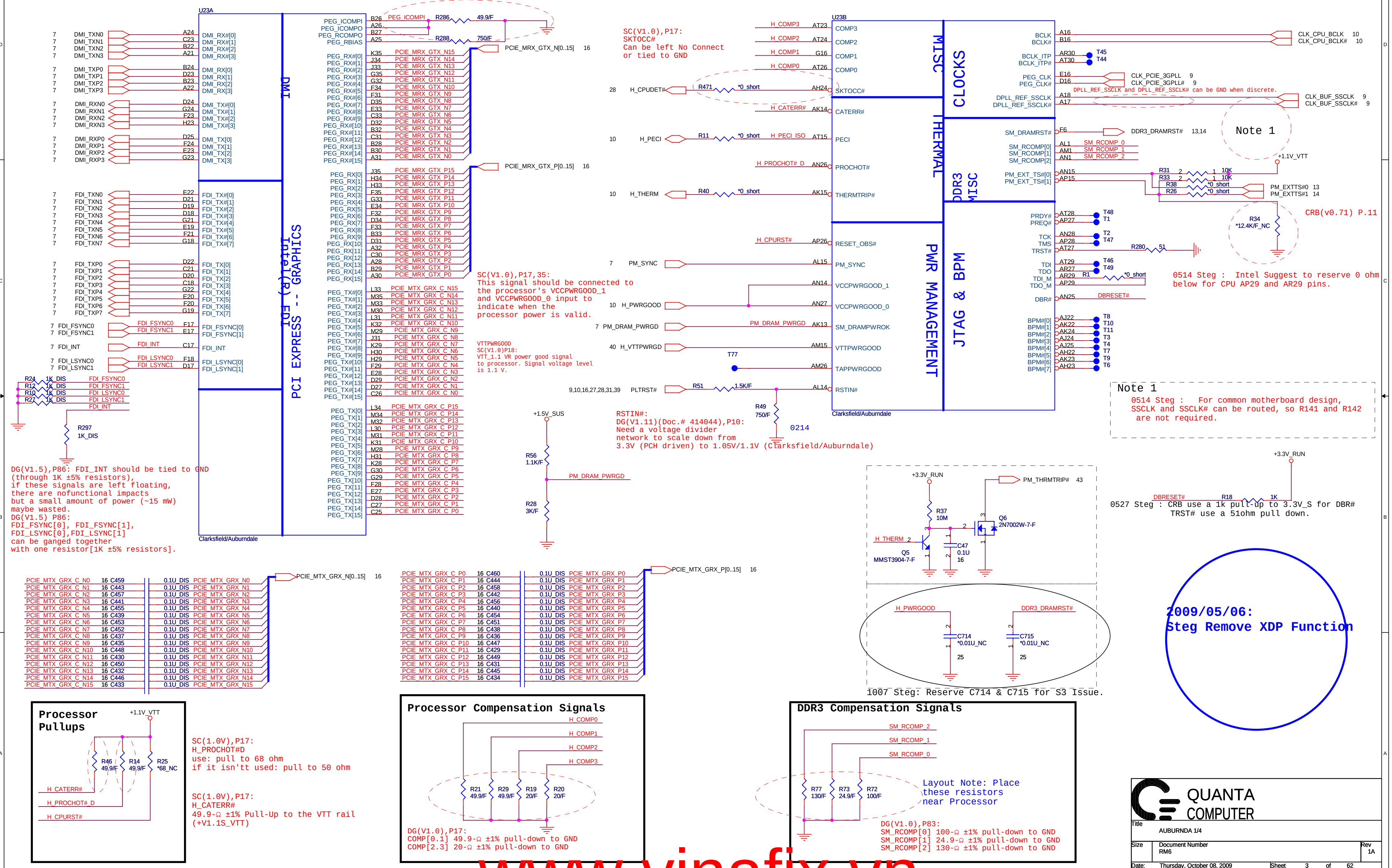
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-[illegible] ±1% resistor, pulled-down to GND on the board.
U23A
DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
Clarksfield/Auburndale
PCIE_MRX_GTX_N[0..15] 16
PCIE_MRX_GTX_P[0..15] 16
SC(V1.0),P17,35: This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.
VTTPWRGOOD SC(V1.0)P18: VTT_1.1 VR power good signal to processor. Signal voltage level is 1.1 V.
SC(V1.0),P17: SKTOCC# Can be left No Connect or tied to GND
U23B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be GND when discrete.
Note 1
CRB(v0.71) P.11
0514 Steg : Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins.
Note 1
0514 Steg : For common motherboard design, SSCLK and SSCLK# can be routed, so R141 and R142 are not required.
0527 Steg : CRB use a 1k pull-up to 3.3V_S for DBR# TRST# use a 51ohm pull down.
RSTIN#: DG(V1.11)(Doc.# 414044),P10: Need a voltage divider network to scale down from 3.3V (PCH driven) to 1.05V/1.1V (Clarksfield/Auburndale)
0214
DG(V1.5),P86: FDI_INT should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.5) P86: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be ganged together with one resistor[1K ±5% resistors].
PCIE_MTX_GRX_N[0..15] 16
PCIE_MTX_GRX_P[0..15] 16
PM_THRMTRIP# 43
Q6 2N7002W-7-F
Q5 MMST3904-7-F
1007 Steg: Reserve C714 & C715 for S3 Issue.
2009/05/06: Steg Remove XDP Function
Processor Pullups
SC(1.0V),P17: H_PROCHOT#D use: pull to 68 ohm if it isn'tt used: pull to 50 ohm
SC(1.0V),P17: H_CATERR# 49.9-[illegible] ±1% Pull-Up to the VTT rail (+V1.1S_VTT)
Processor Compensation Signals
DG(V1.0),P17: COMP[0.1] 49.9-[illegible] ±1% pull-down to GND COMP[2.3] 20-[illegible] ±1% pull-down to GND
DDR3 Compensation Signals
Layout Note: Place these resistors near Processor
DG(V1.0),P83: SM_RCOMP[0] 100-[illegible] ±1% pull-down to GND SM_RCOMP[1] 24.9-[illegible] ±1% pull-down to GND SM_RCOMP[2] 130-[illegible] ±1% pull-down to GND

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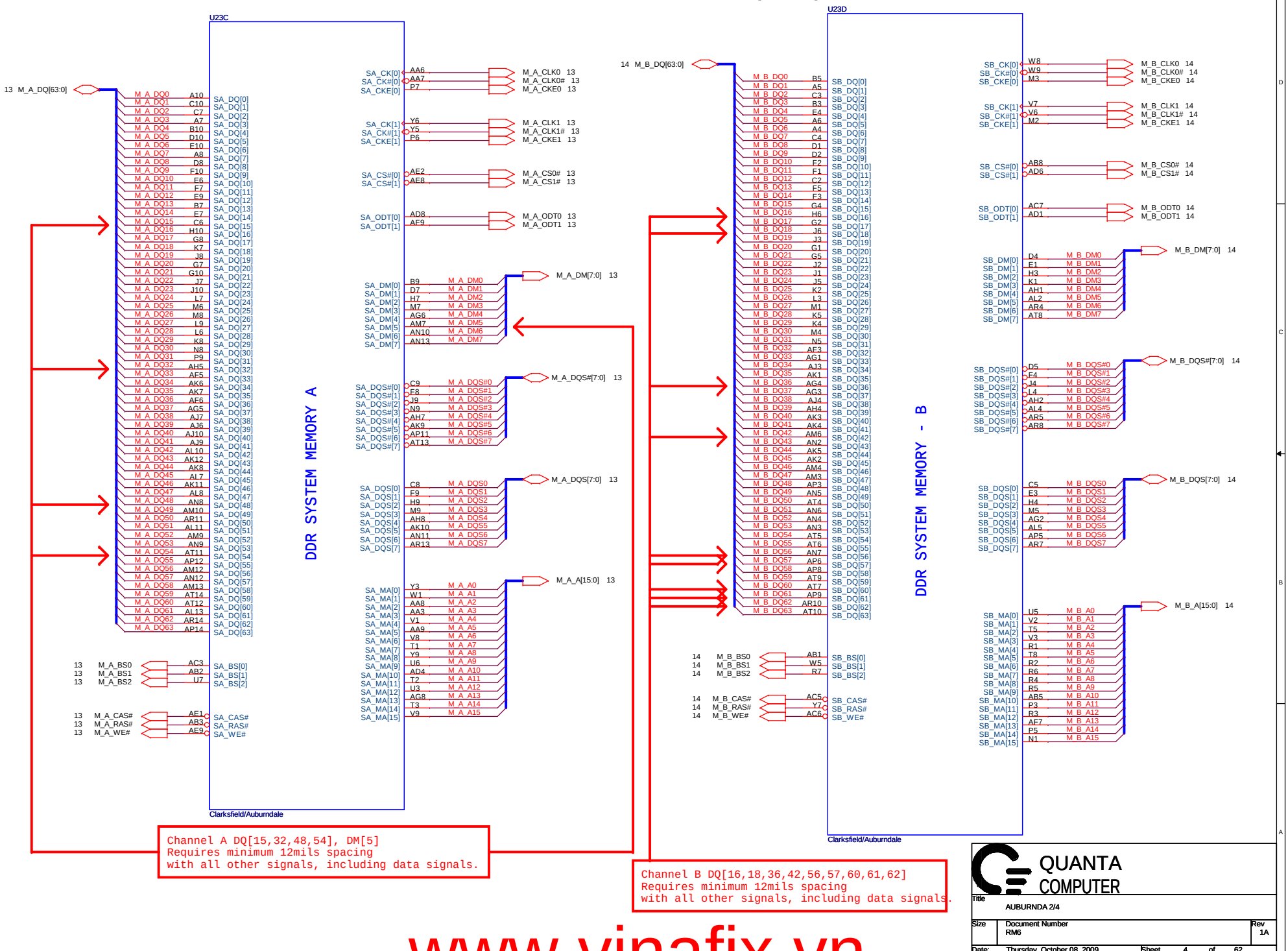
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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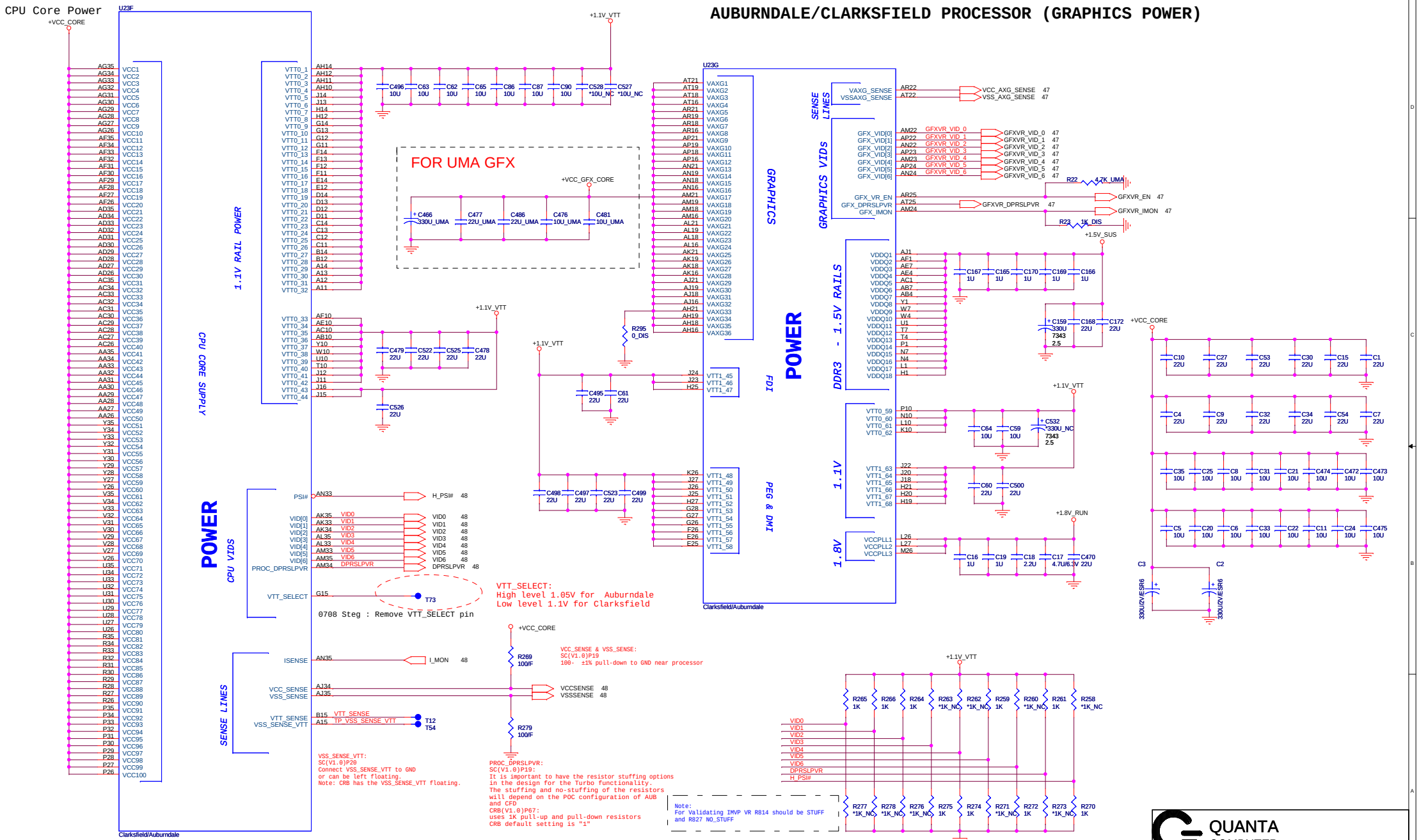
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

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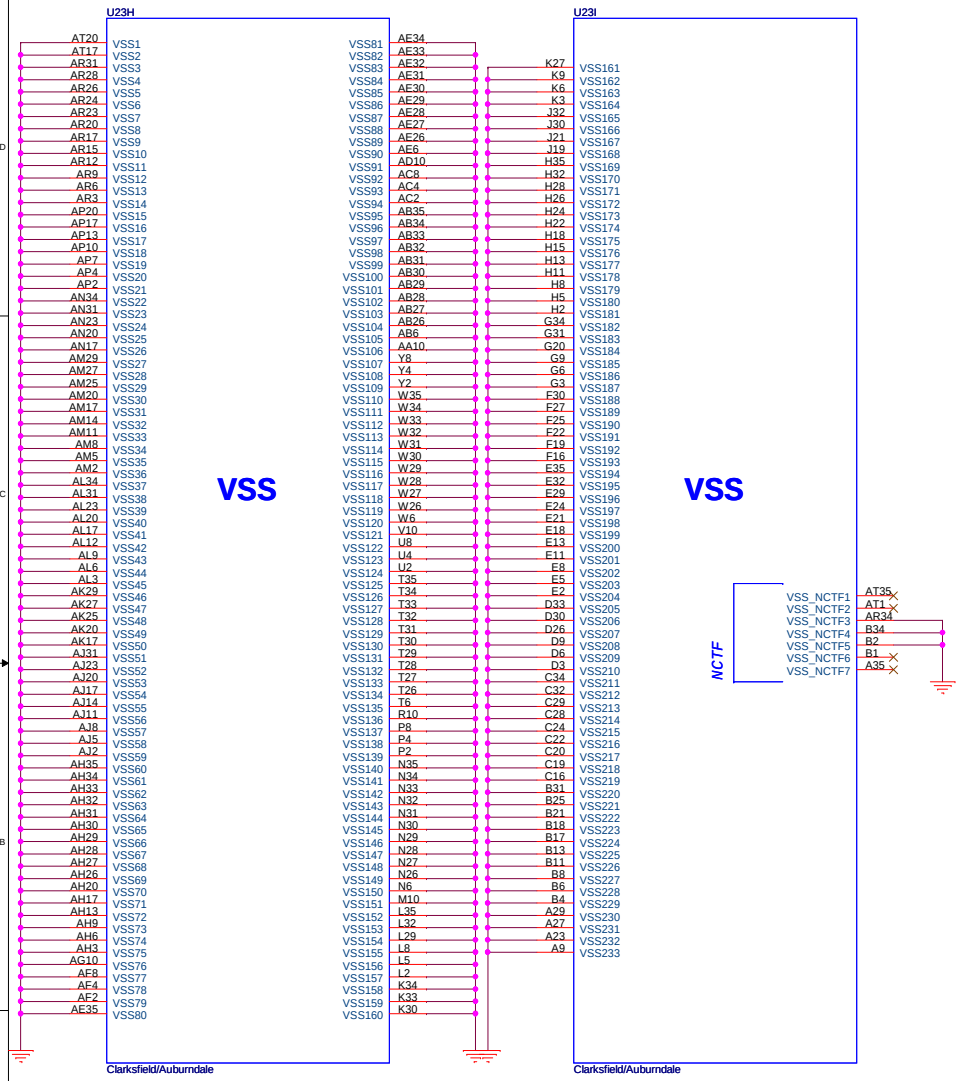
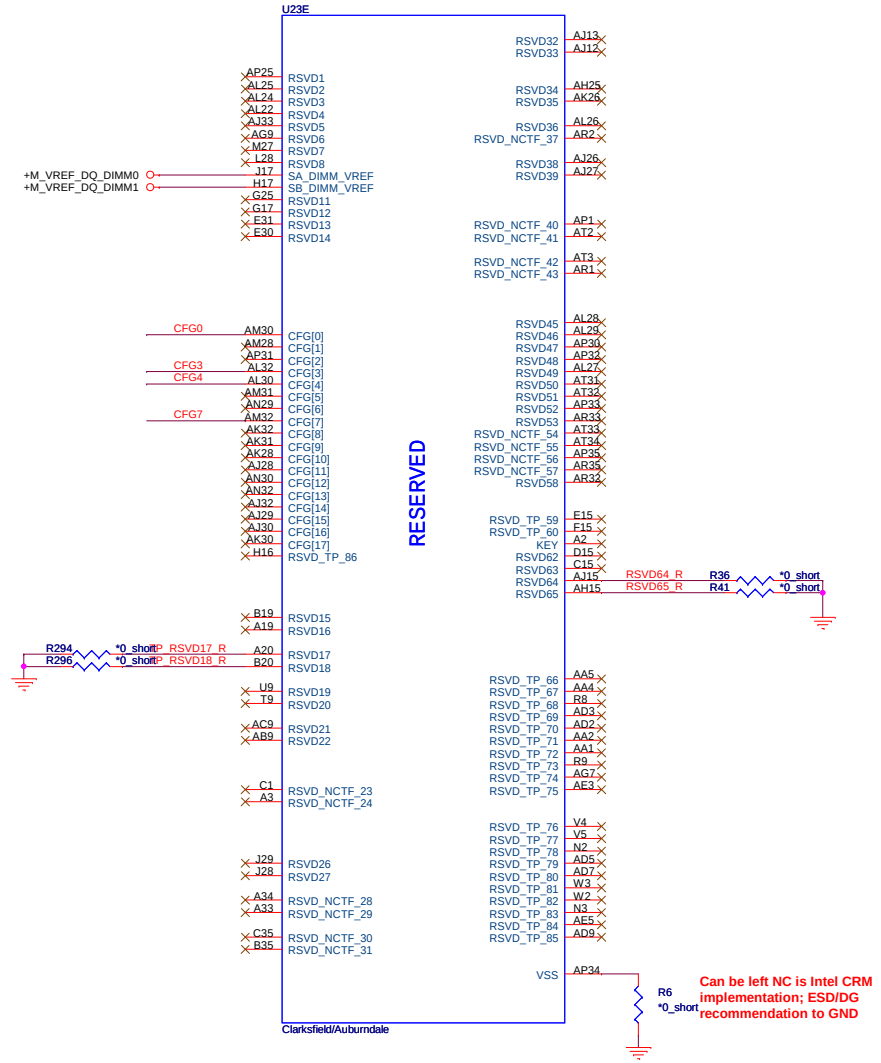
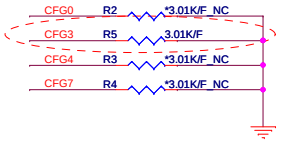
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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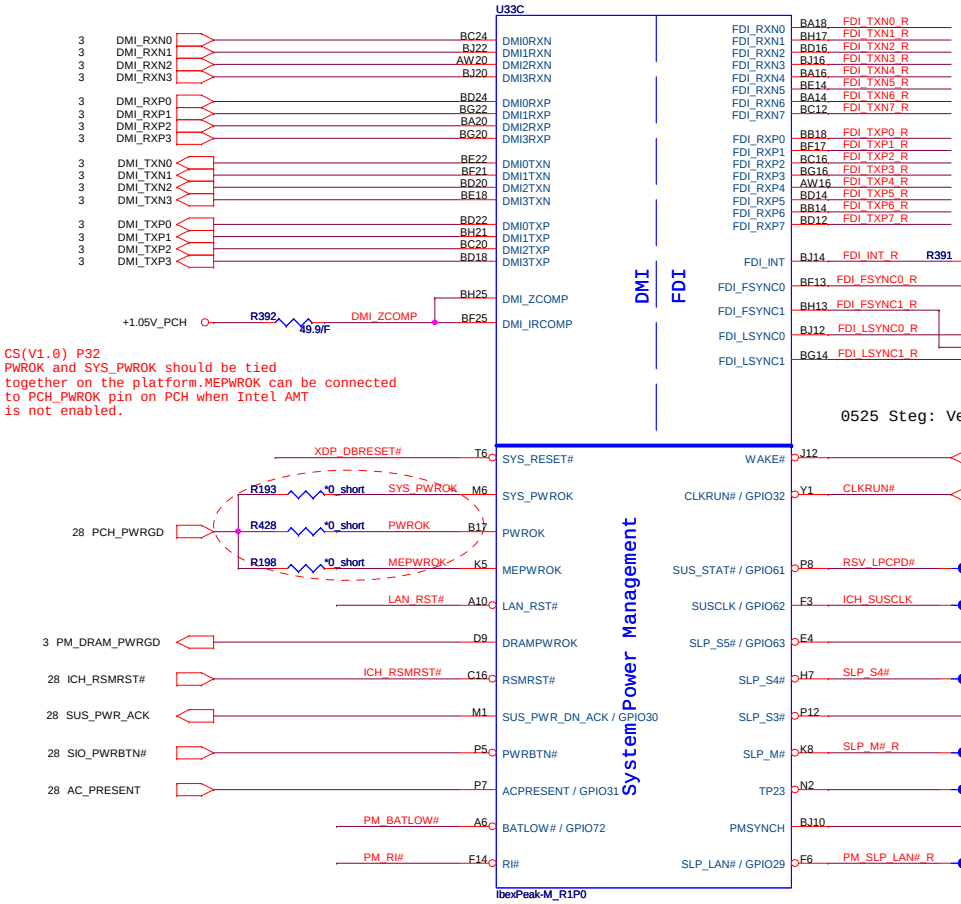
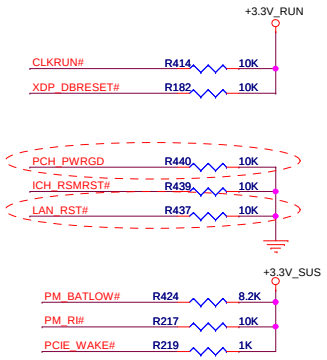
IBEX PEAK-M (DMI,FDI,GPIO)

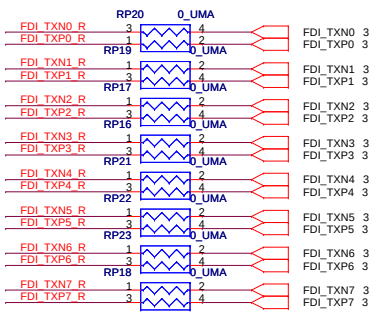


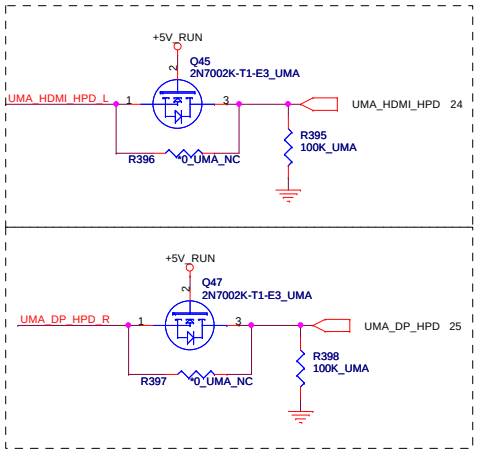
CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform.MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

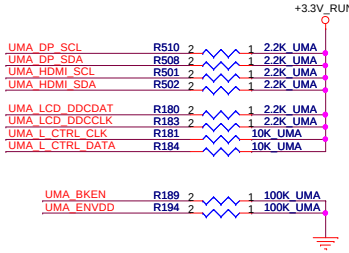
0525 Steg: Vertical RP50 & RP51

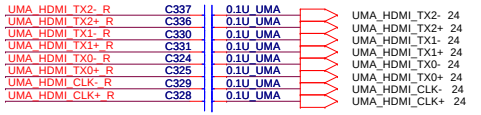
MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



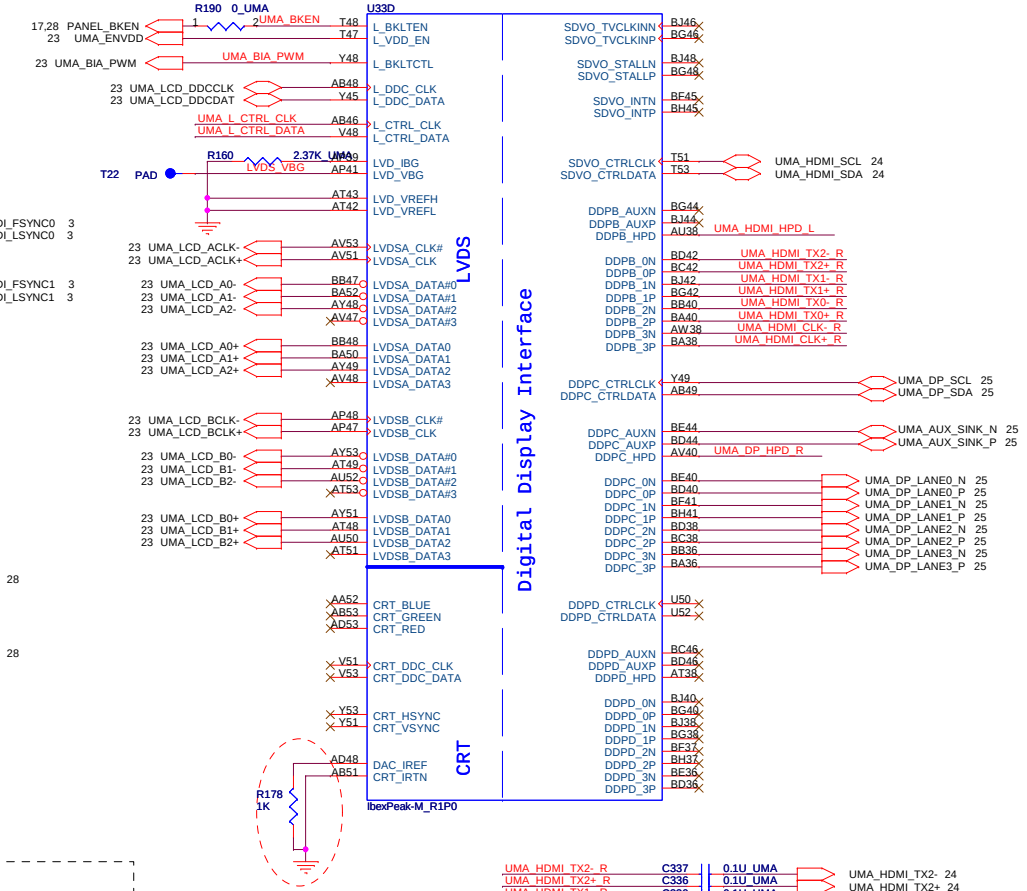








IBEX PEAK-M (LVDS,DDI)



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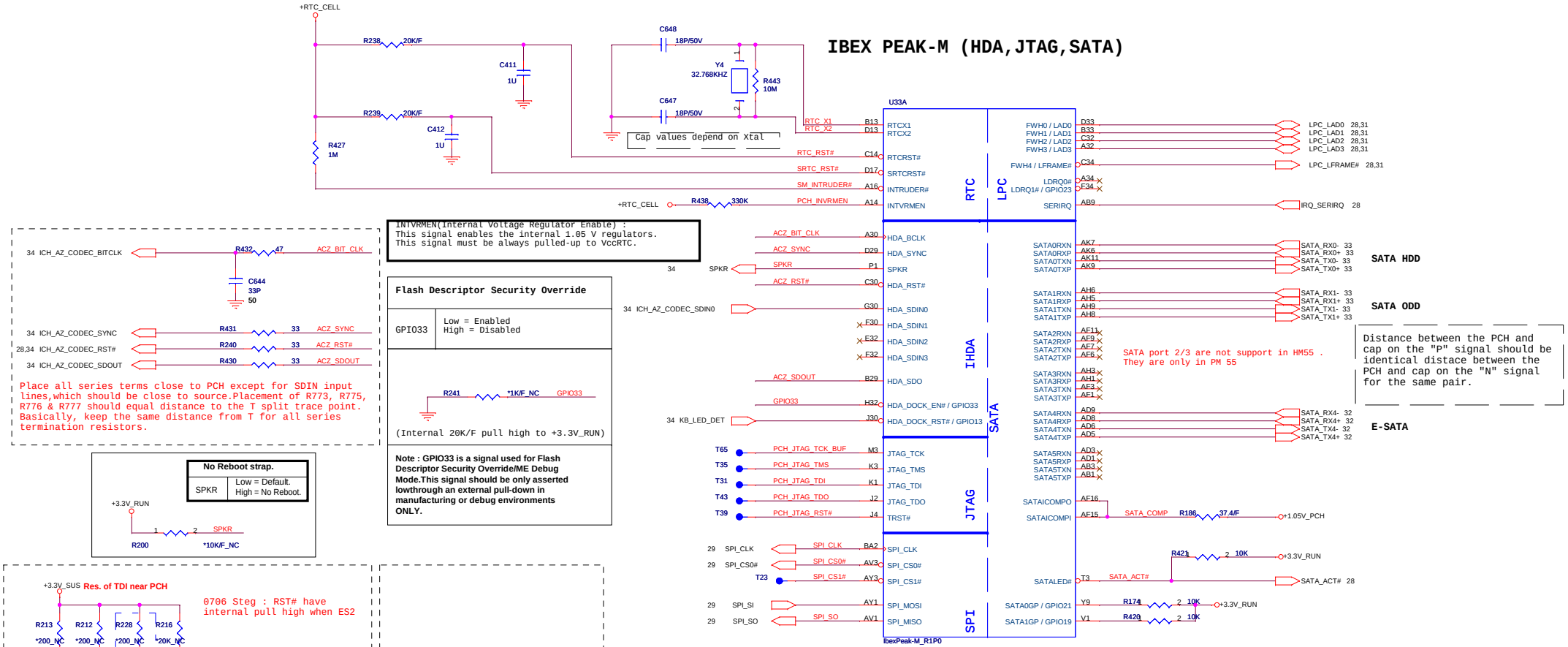
IBEX PEAK-M (HDA,JTAG,SATA)



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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

0901 Steg : Remove Briadwood Function.

SATA + USB Conn

pUSB Conn M/B

USB Conn D/B

Mini Card (WLAN)

BT

USB port 6/7 are not support in HM55 .
They are only in PM 55

Card Reader

Express Card

Camera

Note : place these resistors near to PCIe Slots

PCI-E port 7/8 are not support in HM55 .
They are only in PM 55

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

0610 Steg : CLKOUT_PCI[0..4]:
47 ~ 30 ohm series resistor is recommend (single & double load) on PDG v1.5

OC0#~OC7#:
DG(V1.0)P214

Pin	Default Port Mapping
OC0#	Port0,Port1
OC1#	Port2,Port3

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

CLKOUTFLEX3:
EDS(V1.0) :support 48MHz 33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is recommend (PCI & non PCI routing, single & double load)

CLKIN_PCILOOPBACK:
PDG (V1.1): 22 ohm series resistor is recommend

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

25MHz Clock

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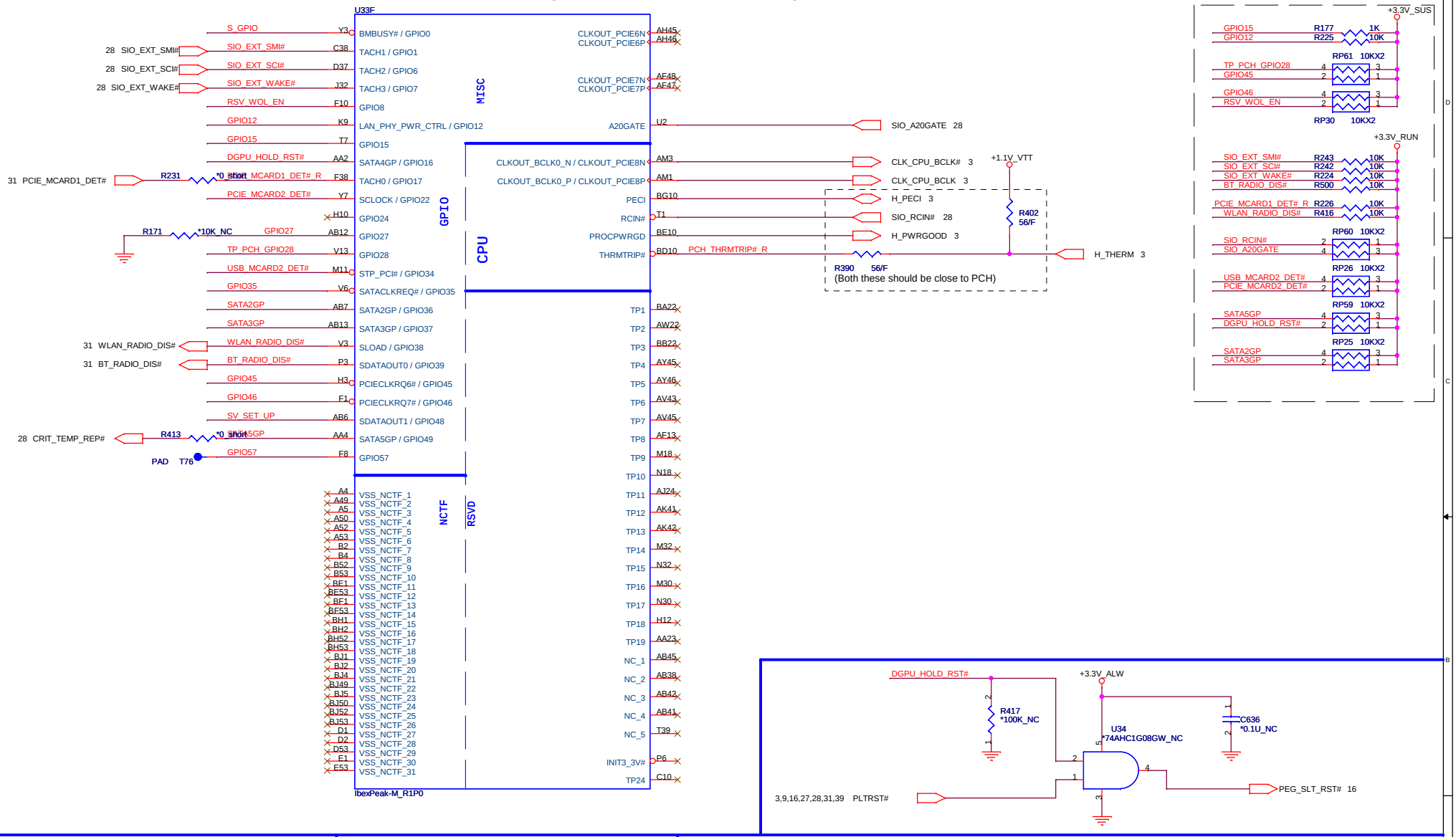
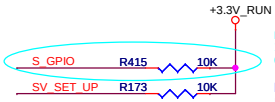
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



6

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high



BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

SV_SET_UP	1-X High = Strong (Default)

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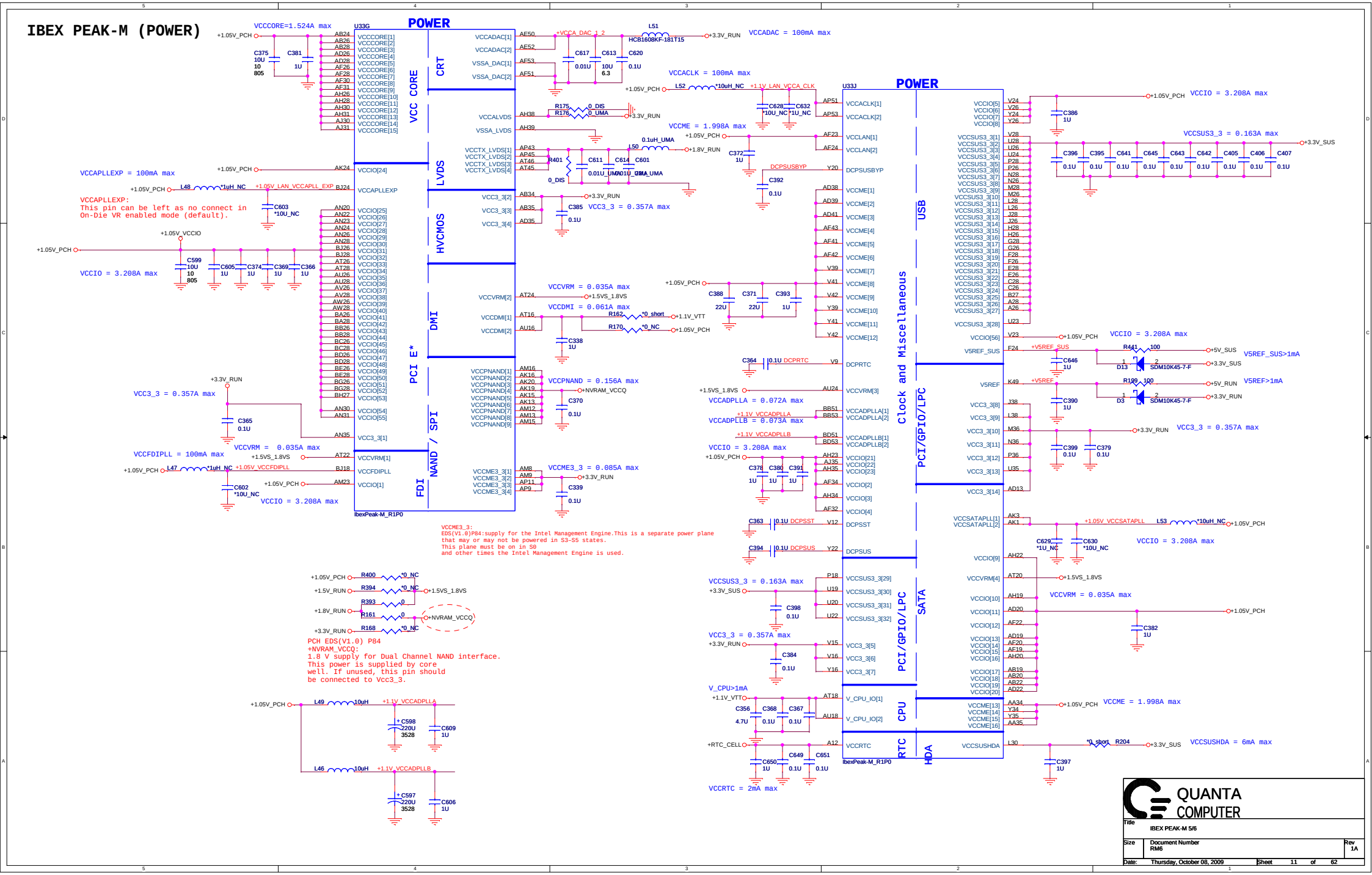
IBEX PEAK-M (POWER)



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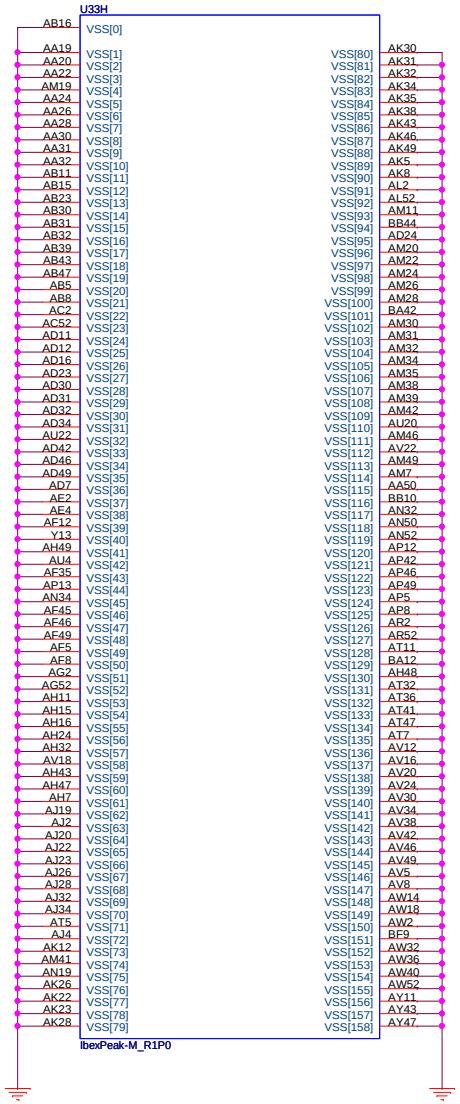
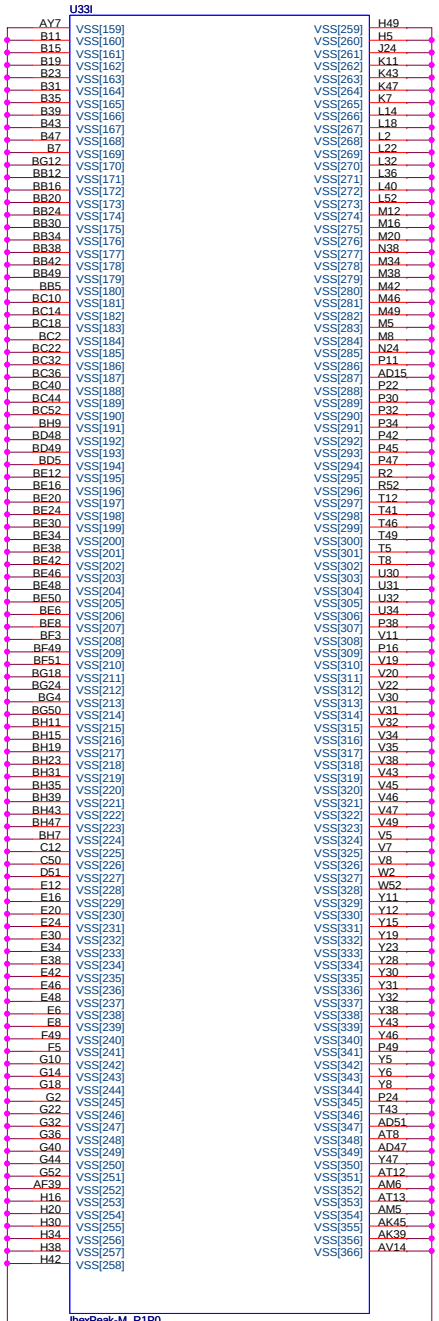
IBEX PEAK-M (GND)





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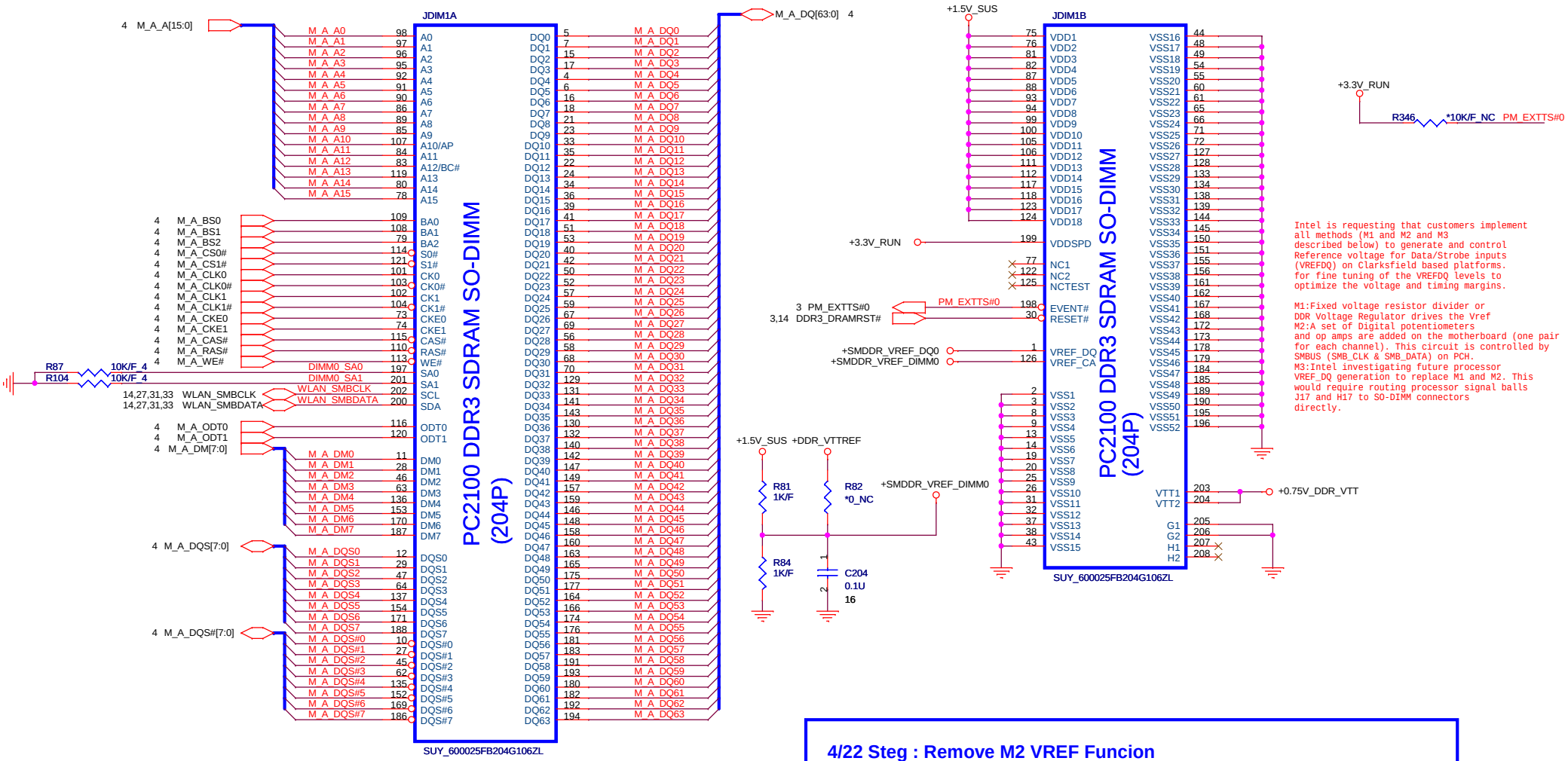
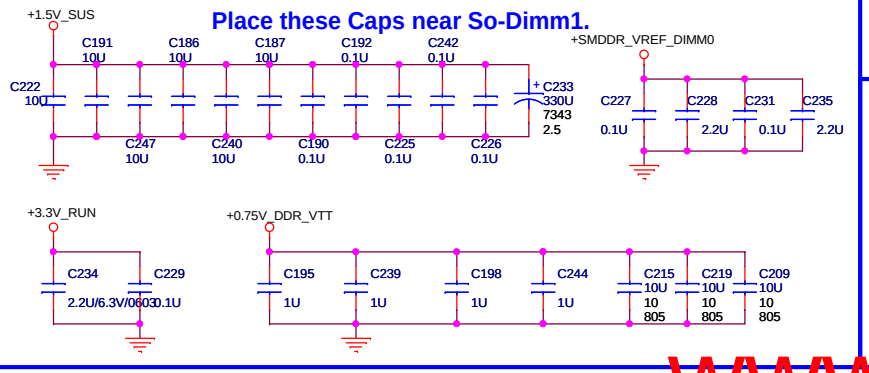
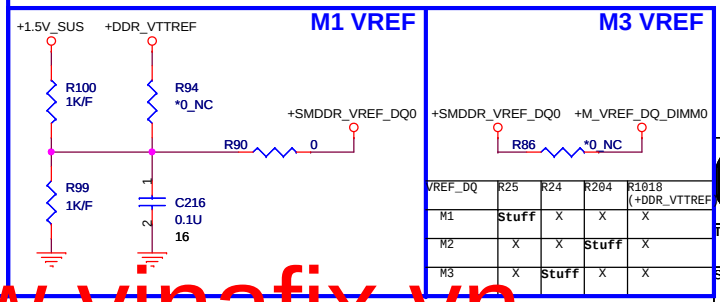


4/22 Steg : Remove M2 VREF Funcion
Intel Design Guide1.5 Had Remove M2 VREF(I2C Programmable VREF)

Place these Caps near So-Dimm1.



0527 Steg : M1&M3 Connection follow FM9 for Layout convenience.



VREF_DQ	R25	R24	R204	R1018 (+DDR_VTTREF)
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

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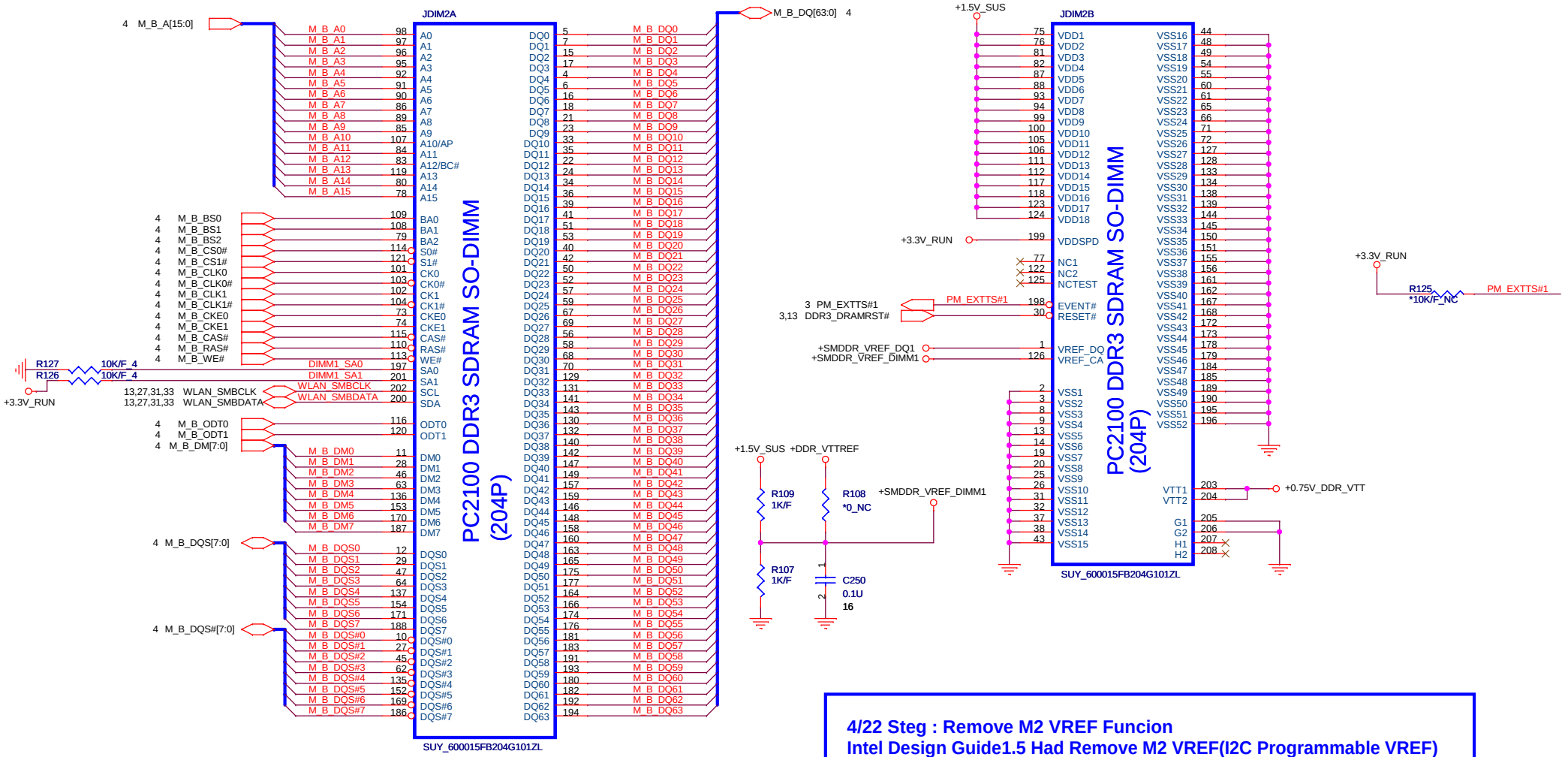
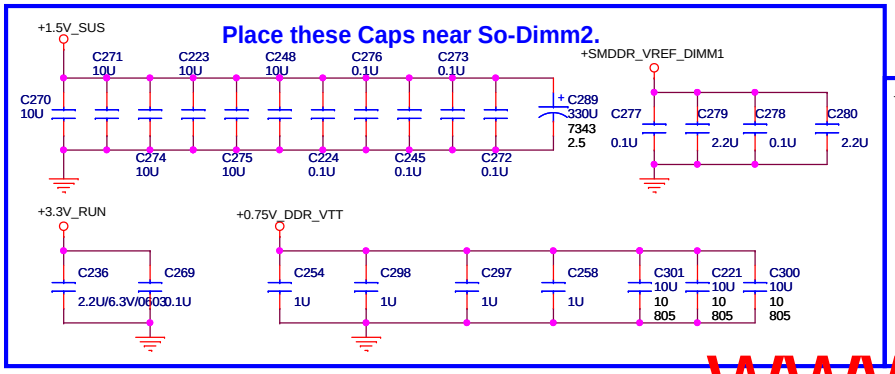
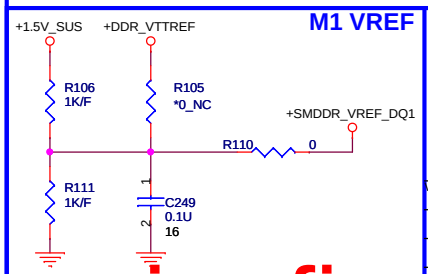


4/22 Steg : Remove M2 VREF Funcion
Intel Design Guide1.5 Had Remove M2 VREF(I2C Programmable VREF)

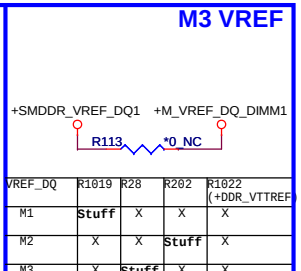


0527 Steg : M1&M3 Connection follow FM9 for Layout convenience.



M1 VREF

M3 VREF



VREF_DQ	R1019	R28	R202	R1022 (+DDR_VTTREF)
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

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Title	DDR3 DIMM-1	
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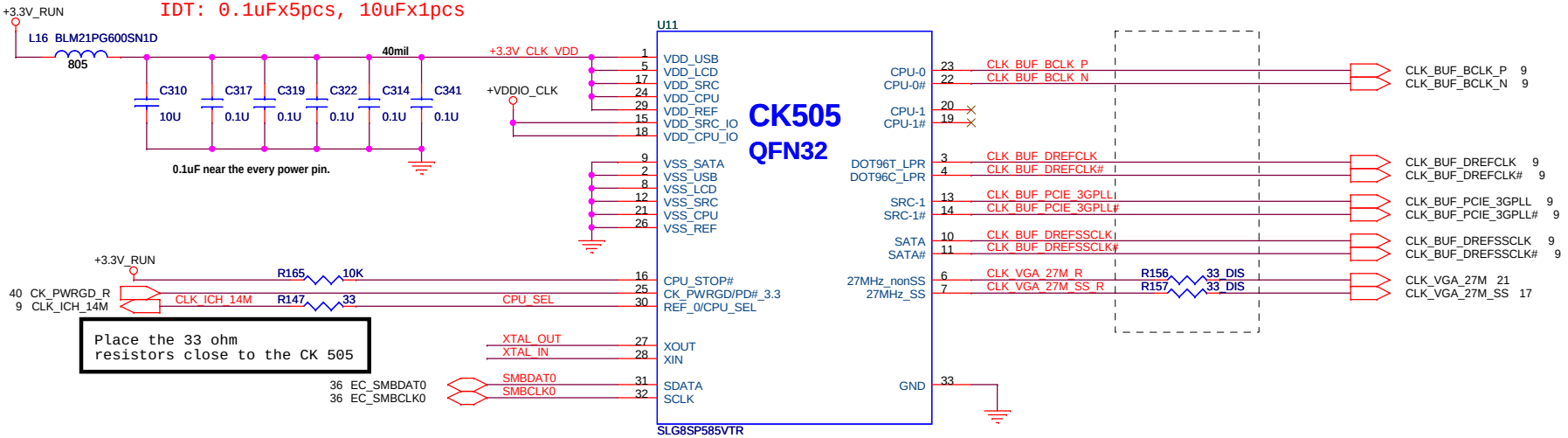
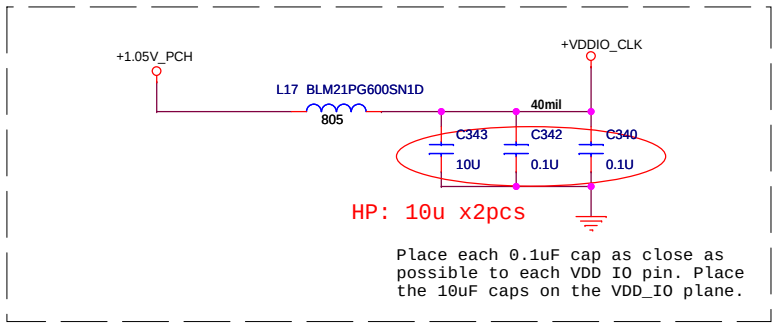
Realtek: 0.1uFx6pcs, 22uFx1pcs
IDT: 0.1uFx5pcs, 10uFx1pcs

Place within 0.5" of CLKGEN

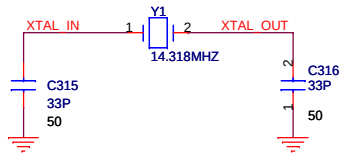


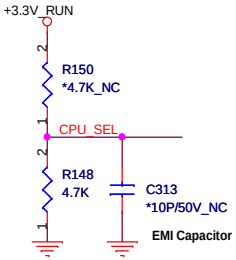
Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.

Add capacitor pads for improving WWAN.



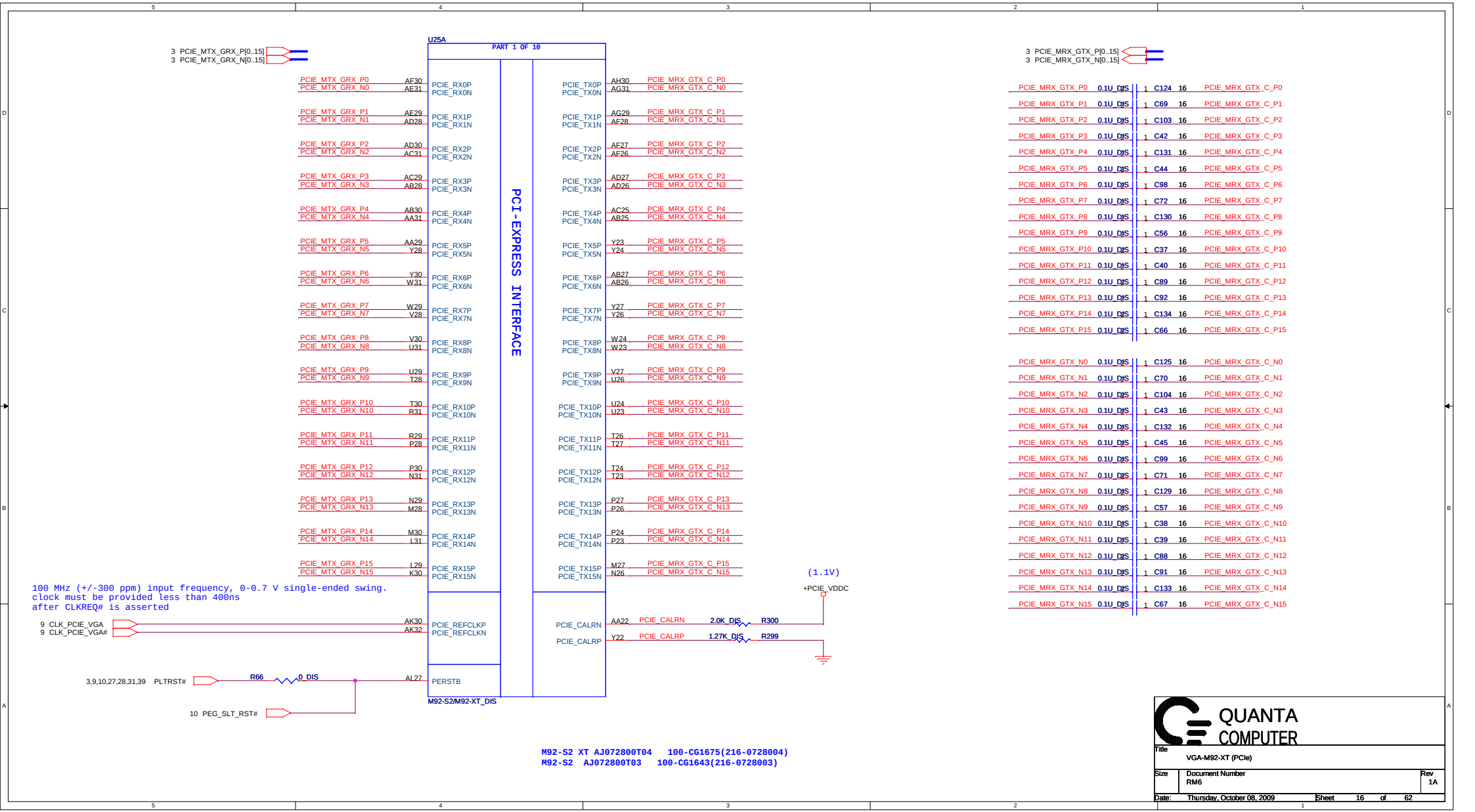


PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

QUANTA COMPUTER

Title	Clock Generator	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 15 of 62	



MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB		0	0	0
256MB		0	0	1
64MB		0	1	0
512MB		1	0	0

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FM9 setting
GPIO0	GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO(1) - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO(2) - BIF_GEN2_EN (5.0 GT/s Enable) 0 : Default. (Driver Controlled Gen2) 1 : Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0 : Battery saving mode = 0.0 V 1 : AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0

DAC1_VGAVSYNC / DAC1_VGAHSYNC	HD Audio straps
0\0	No audio function
0\1	Audio for DisplayPort only
1\0	Audio for DisplayPort and HDMI if dongle is detected
1\1	Audio for both DisplayPort and HDMI

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	

For Park S3:
Reserve All components in this Box
R431,R432,R427,L52,C2499,C545,C56,L23
,C111,R421,33,C2500,C271,C69

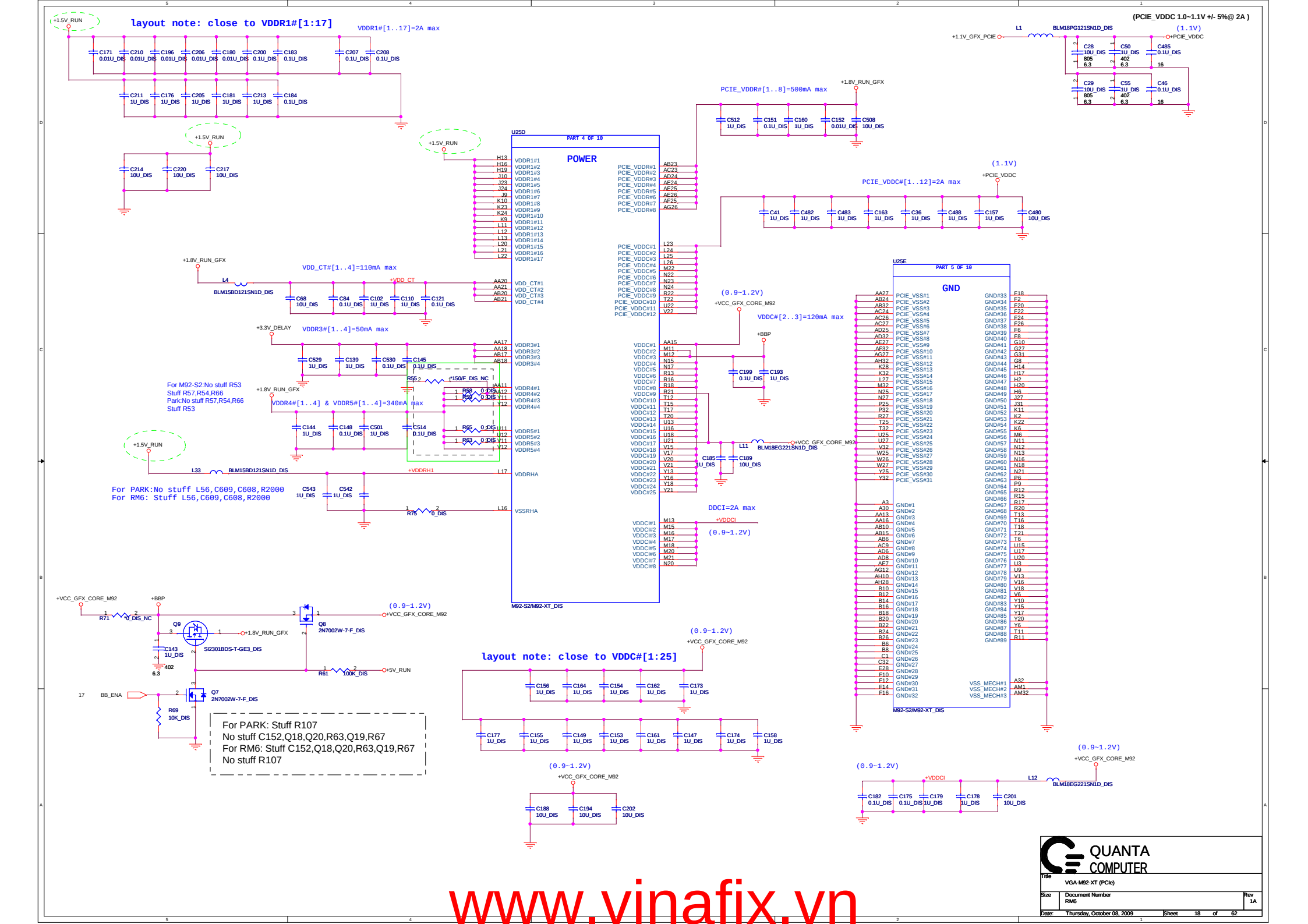
DPC_VDD18#1 and DPC_VDD18#2 are for Future ASIC

For M92-S2: DO NOT Install any Component in this Box.

For M92: No stuff R106
For Park: Stuff R106

Keep A2VSSQ away from noisy ground.

Title	VGA-M92-XT (PCIe)
Size	Document Number RM6
Rev	1A
Date:	Thursday, October 08, 2009
Sheet	17 of 62



MEMORY INTERFACE

U25C
PART 3 OF 10
MEMORY INTERFACE

DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R

	M92	PARK
R87, R86	No stuff	Stuff
R79	240 Ohms(0.5%)	150 Ohms(1%)
C1015,C016 R1036,R1037	No stuff	Stuff
R74,R75	Stuff	No stuff
R2016	No stuff	Stuff

Designator	For M9X-S2 and M93-S3	For Park-S3
R76	NC	10K
R2014	0 ohm/Short	680
R506	2.2K	NC
C175	2200P	68P

THERMAL MONITOR

Only For Park

route 50ohms single-ended 100ohms diff and keep short

Reserve for Park-S3

This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

QUANTA COMPUTER

Title: VGA-M92-XT (PCIe)
Size: Document Number: RM6 Rev: 1A
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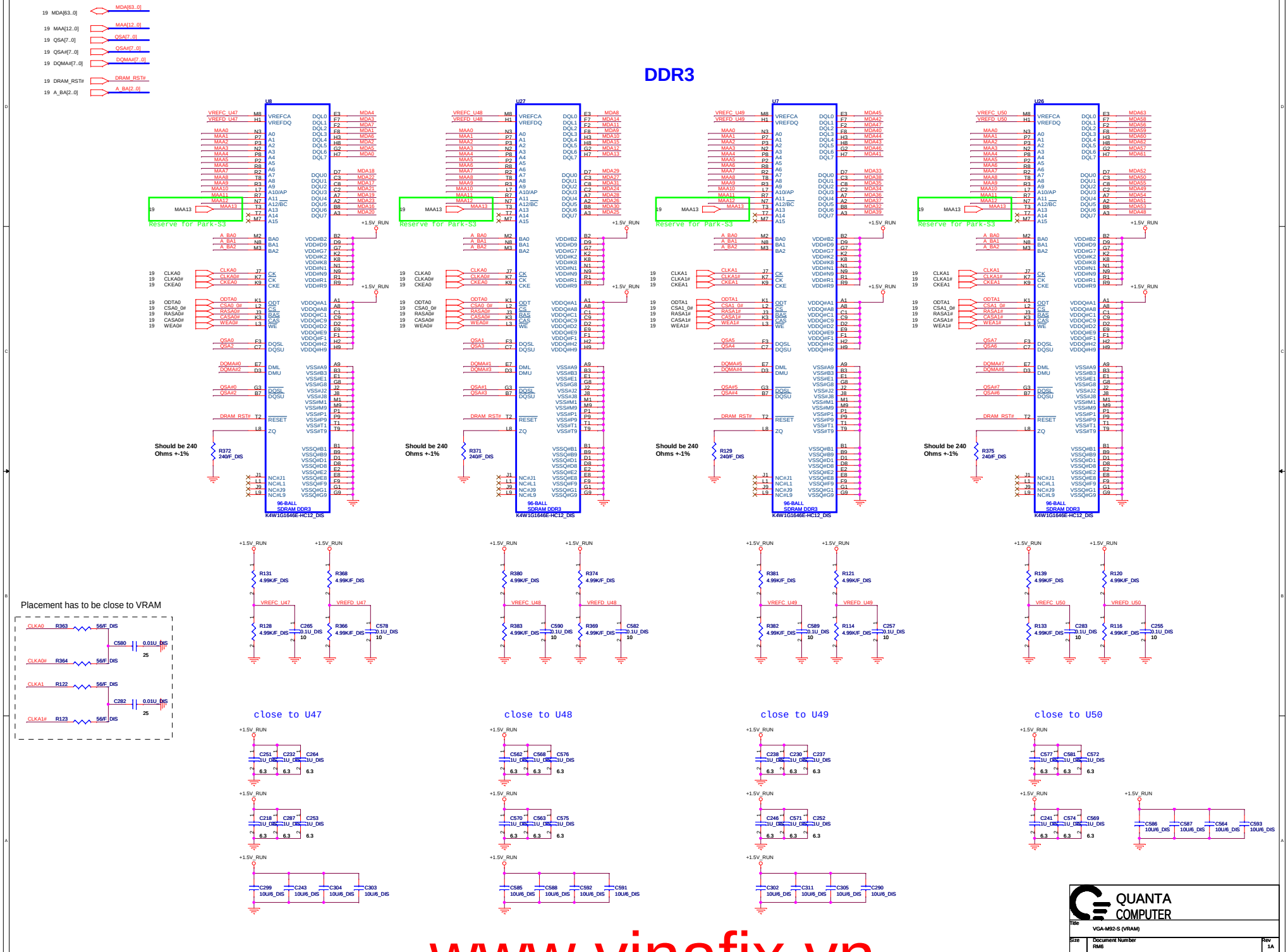
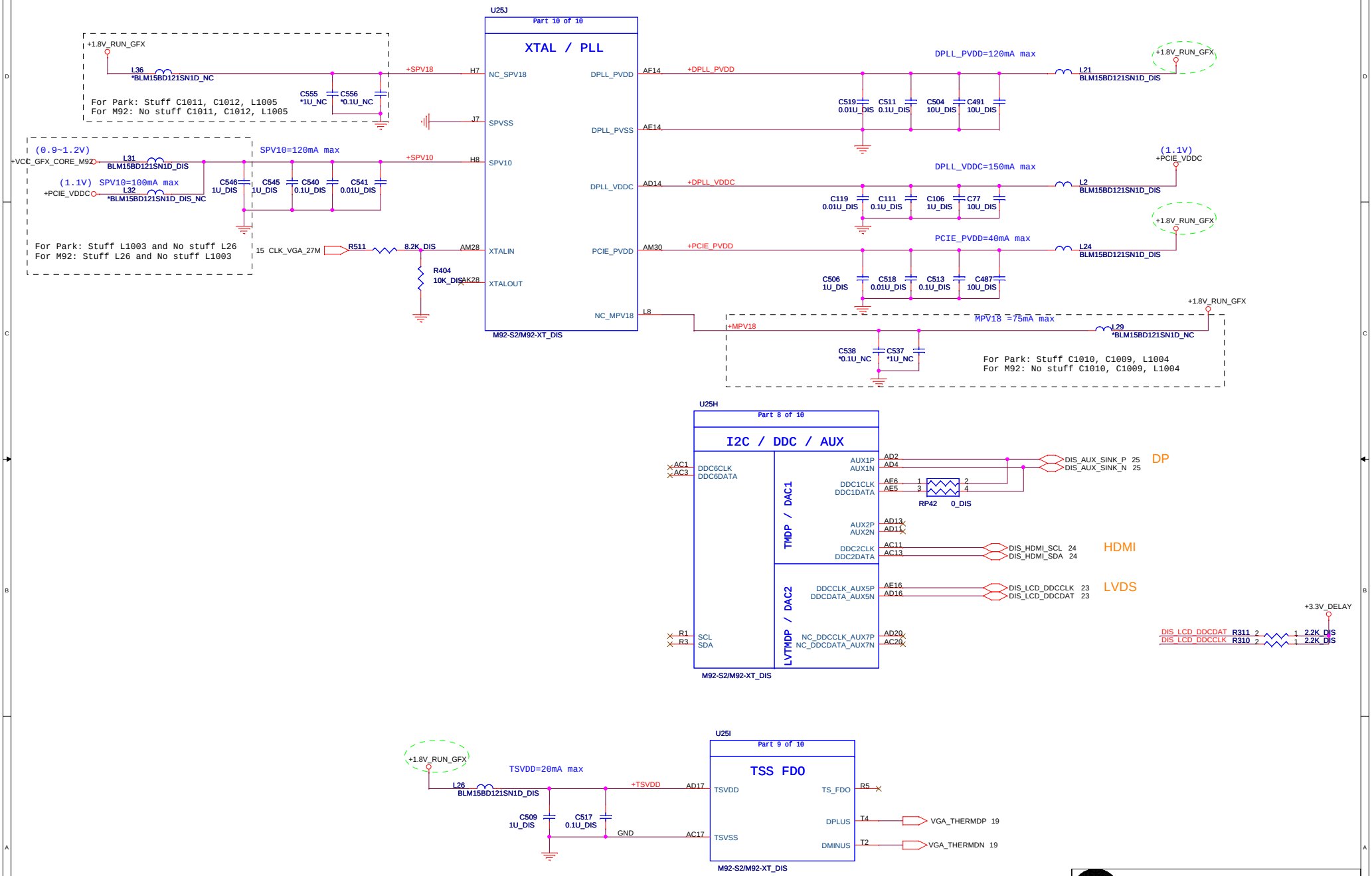
DDR3





QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number RM6	Rev 1A
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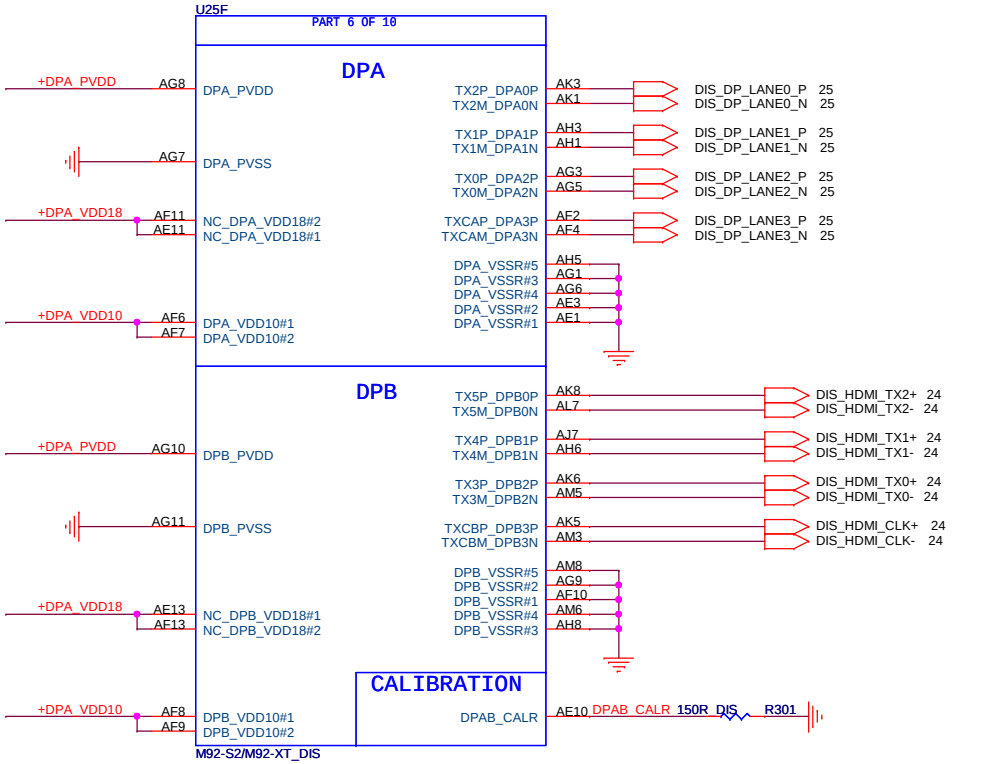
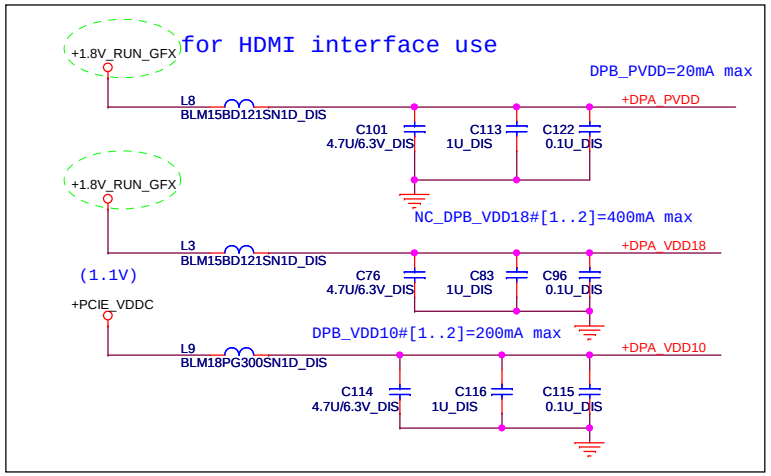
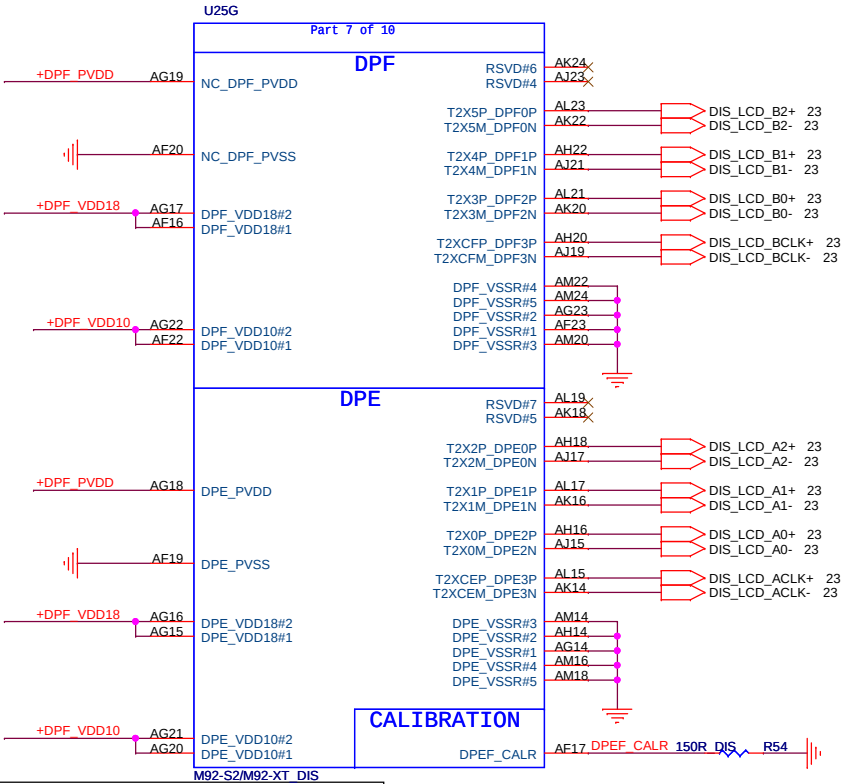
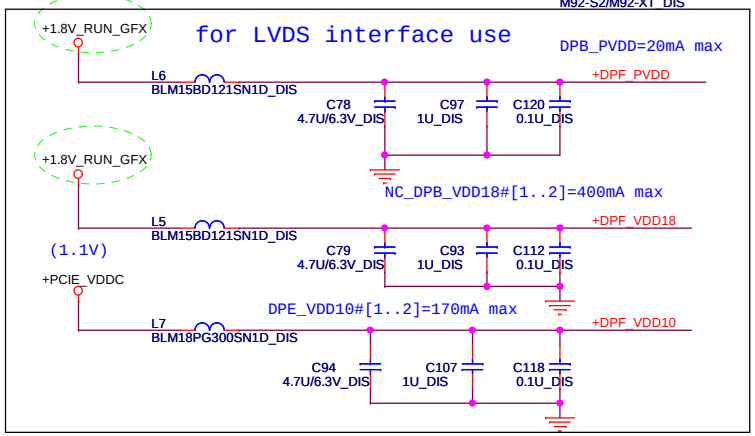
TMDP(HDMI) INTERFACE





LVDS INTERFACE





QUANTA COMPUTER

Title	VGA-M92-XT (PCIe)	
Size	Document Number RM6	Rev 1A
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40Pin LVDS & Array Microphone & Camera Connector

Support the new imbeded diagnostics.

Support DPST enable function

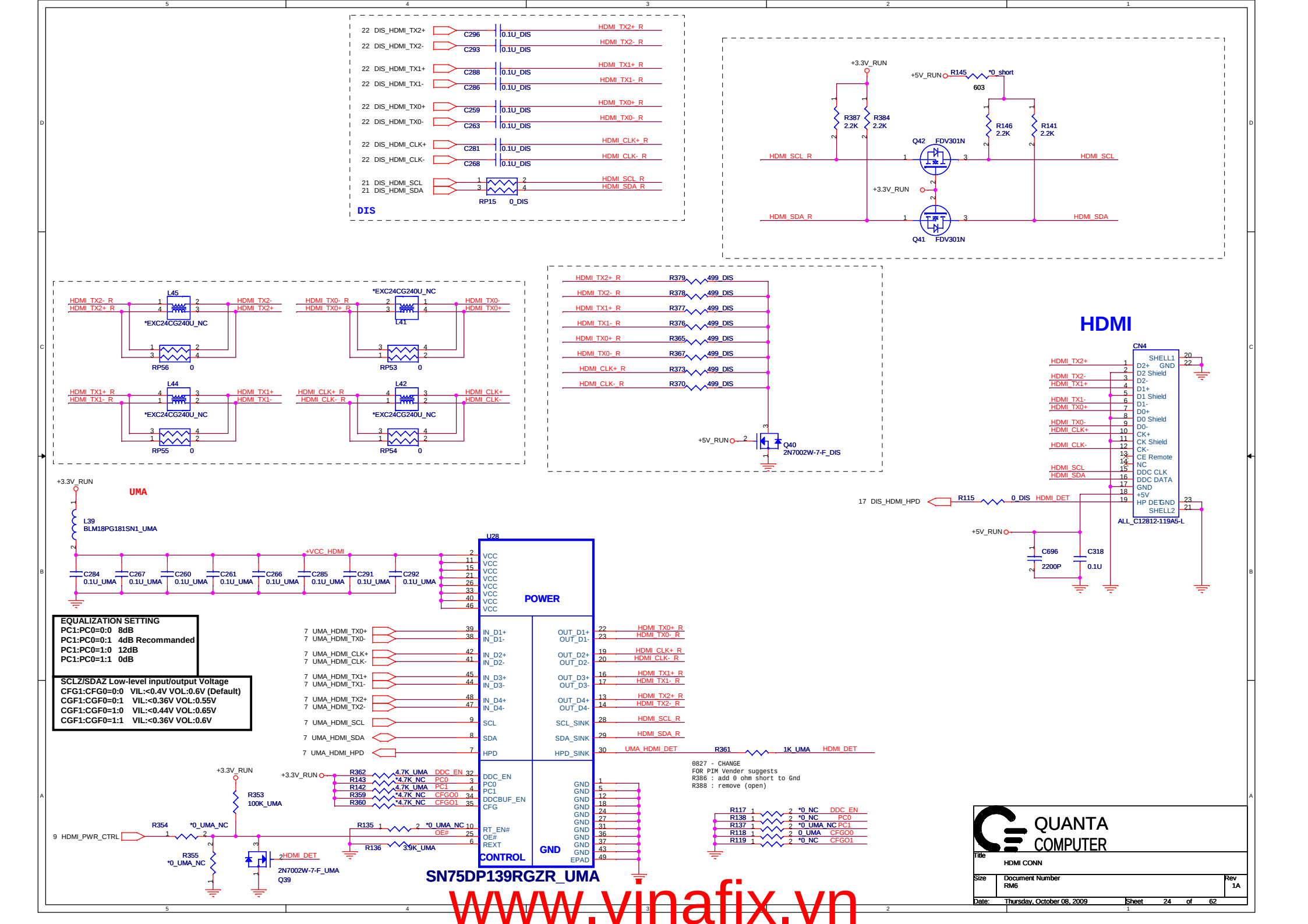
1007 Steg: Use And Gate to control UMA PWM Signal

LVDS Switch STMUX3040QTTR

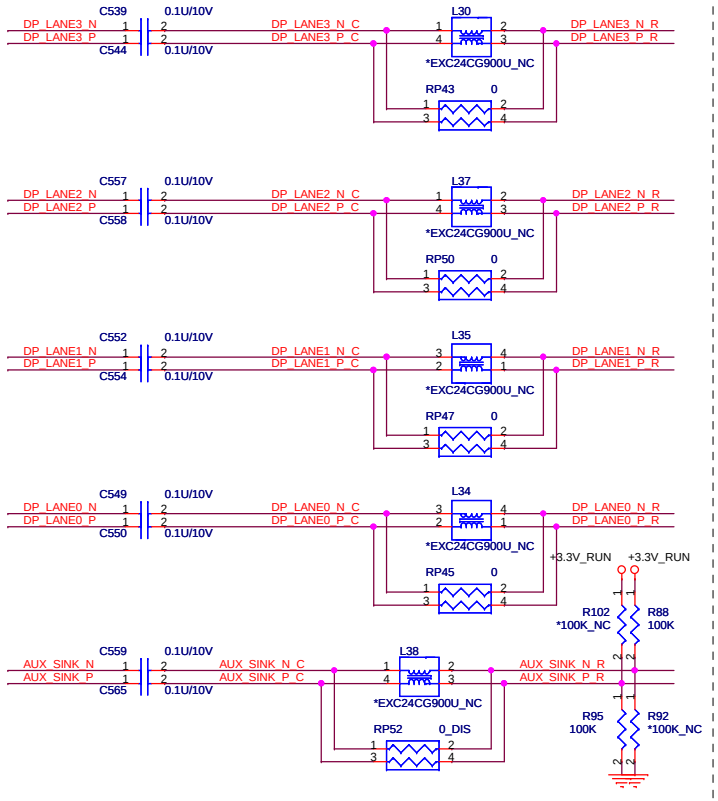
	UMA	DIS
LCD_SEL	0	1

Title	VGA-M82-S (PCIe)
Size	Document Number FM9 — Rev 1A
Date:	Thursday, October 08, 2009 — Sheet 23 of 62

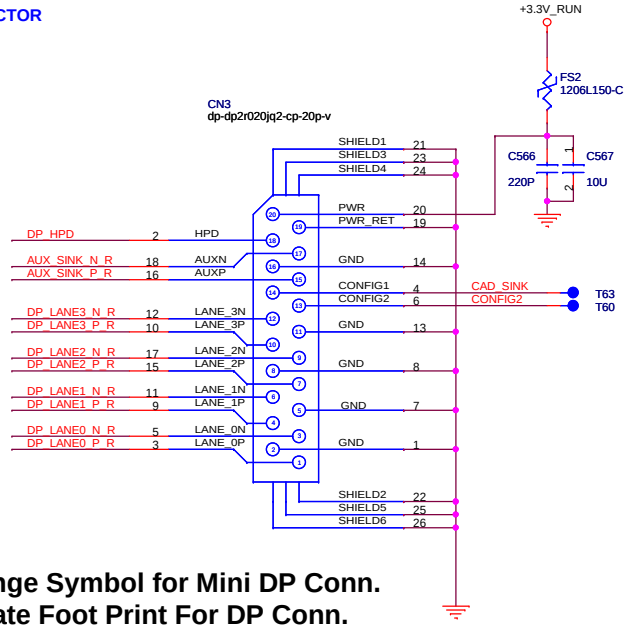
QUANTA COMPUTER


DIS
22 DIS_HDMI_TX2+
22 DIS_HDMI_TX2-
22 DIS_HDMI_TX1+
22 DIS_HDMI_TX1-
22 DIS_HDMI_TX0+
22 DIS_HDMI_TX0-
22 DIS_HDMI_CLK+
22 DIS_HDMI_CLK-
21 DIS_HDMI_SCL
21 DIS_HDMI_SDA
C296 C293 C288 C286 C259 C263 C281 C268 0.1U_DIS
RP15 0_DIS
HDMI_TX2+_R HDMI_TX2-_R HDMI_TX1+_R HDMI_TX1-_R HDMI_TX0+_R HDMI_TX0-_R HDMI_CLK+_R HDMI_CLK-_R HDMI_SCL_R HDMI_SDA_R
+3.3V_RUN
+5V_RUN
R145 *0_short 603
R387 2.2K
R384 2.2K
R146 2.2K
R141 2.2K
Q42 FDV301N
Q41 FDV301N
HDMI_SCL_R
HDMI_SDA_R
HDMI_SCL
HDMI_SDA
L45 L41 L44 L42
*EXC24CG240U_NC
RP56 RP53 RP55 RP54 0
HDMI_TX2- HDMI_TX2+ HDMI_TX0- HDMI_TX0+ HDMI_TX1- HDMI_TX1+ HDMI_CLK- HDMI_CLK+
R379 R378 R377 R376 R365 R367 R373 R370 499_DIS
+5V_RUN
Q40
2N7002W-7-F_DIS
HDMI
CN4
SHELL1 SHELL2
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET GND
ALL_C12812-119A5-L
17 DIS_HDMI_HPD
R115 0_DIS HDMI_DET
C696 2200P
C318 0.1U
UMA
+3.3V_RUN
L39 BLM18PG181SN1_UMA
+VCC_HDMI
C284 C267 C260 C261 C266 C285 C291 C292 0.1U_UMA
U28
POWER
VCC
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V
7 UMA_HDMI_TX0+ 7 UMA_HDMI_TX0- 7 UMA_HDMI_CLK+ 7 UMA_HDMI_CLK- 7 UMA_HDMI_TX1+ 7 UMA_HDMI_TX1- 7 UMA_HDMI_TX2+ 7 UMA_HDMI_TX2- 7 UMA_HDMI_SCL 7 UMA_HDMI_SDA 7 UMA_HDMI_HPD
IN_D1+ IN_D1- IN_D2+ IN_D2- IN_D3+ IN_D3- IN_D4+ IN_D4- SCL SDA HPD
OUT_D1+ OUT_D1- OUT_D2+ OUT_D2- OUT_D3+ OUT_D3- OUT_D4+ OUT_D4- SCL_SINK SDA_SINK HPD_SINK
HDMI_TX0+_R HDMI_TX0-_R HDMI_CLK+_R HDMI_CLK-_R HDMI_TX1+_R HDMI_TX1-_R HDMI_TX2+_R HDMI_TX2-_R HDMI_SCL_R HDMI_SDA_R UMA_HDMI_DET
R361 1K_UMA HDMI_DET
DDC_EN PC0 PC1 DDCBUF_EN CFG RT_EN# OE# REXT
CONTROL
GND
EPAD
SN75DP139RGZR_UMA
+3.3V_RUN
R362 4.7K_UMA DDC_EN
R143 *4.7K_NC PC0
R142 4.7K_UMA PC1
R359 *4.7K_NC CFGO0
R360 *4.7K_NC CFGO1
R353 100K_UMA
R354 *0_UMA_NC
R355 *0_UMA_NC
R135 *0_UMA_NC
R136 3.9K_UMA
9 HDMI_PWR_CTRL
HDMI_DET
2N7002W-7-F_UMA
Q39
0827 - CHANGE
FOR PIM Vender suggests
R386 : add 0 ohm short to Gnd
R388 : remove (open)
R117 R138 R137 R118 R119
*0_NC DDC_EN
*0_NC PC0
*0_UMA_NC PC1
0_UMA CFGO0
*0_NC CFGO1
QUANTA COMPUTER
Title HDMI CONN
Size Document Number RM6 Rev 1A
Date: Thursday, October 08, 2009 Sheet 24 of 62
www.vinafix.vn

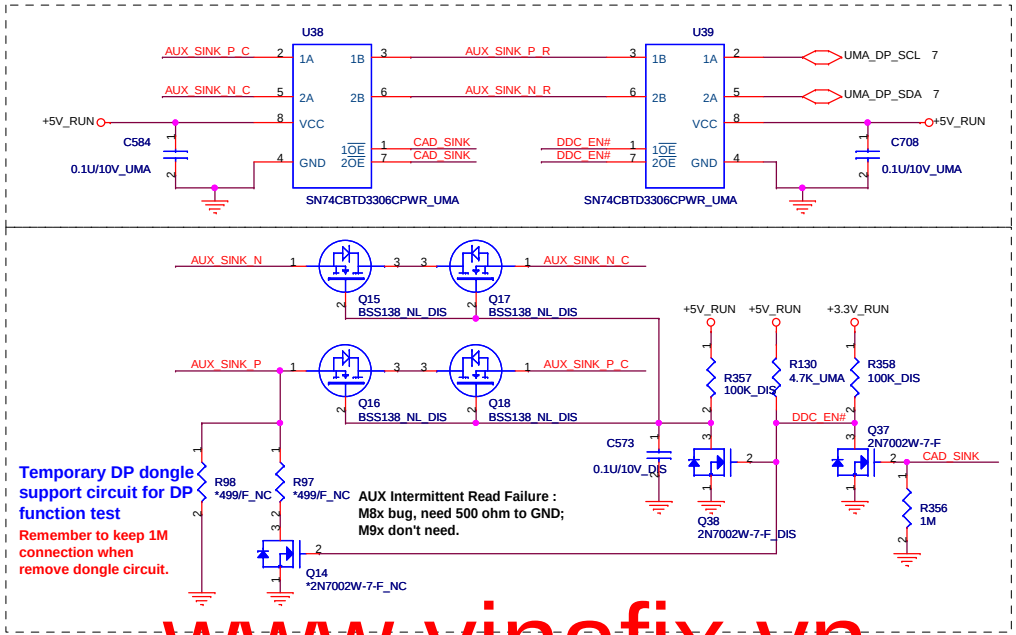
Reserve For EMI

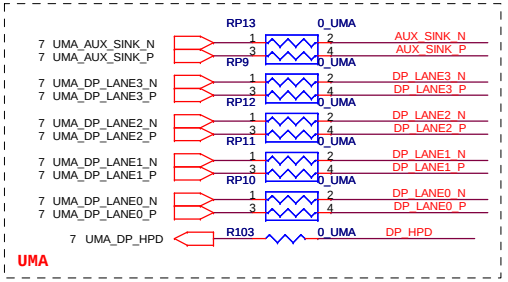


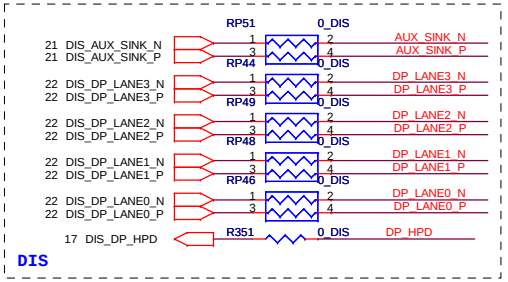
MINI DISPLAY PORT CONNECTOR



7/28 Steg: Change Symbol for Mini DP Conn.
5/18 Steg: Update Foot Print For DP Conn.

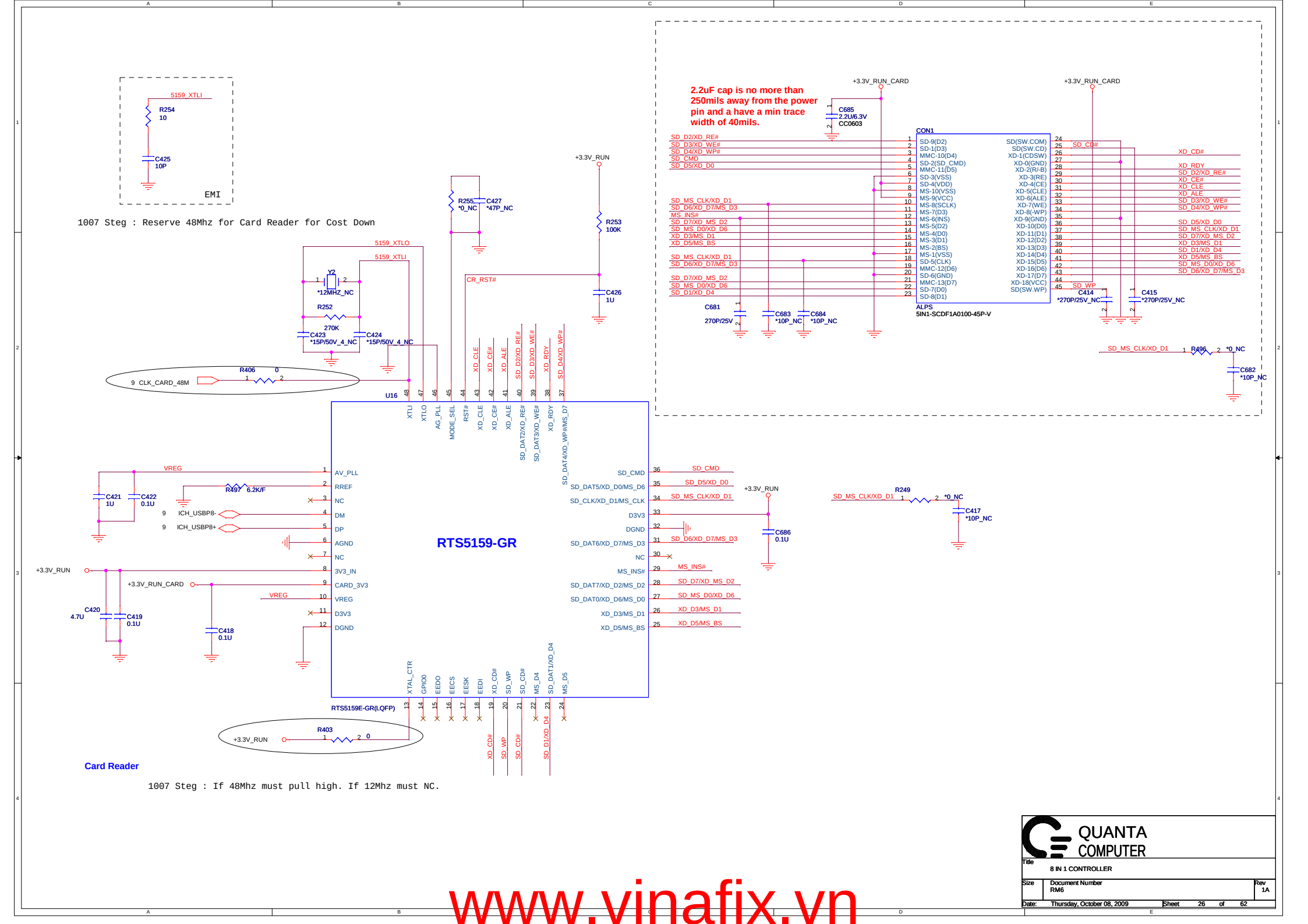






QUANTA COMPUTER

Title	MINI Display Port CONN	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 25 of 62	



QUANTA COMPUTER			
Title	8 IN 1 CONTROLLER		
Size	Document Number RM6		Rev 1A
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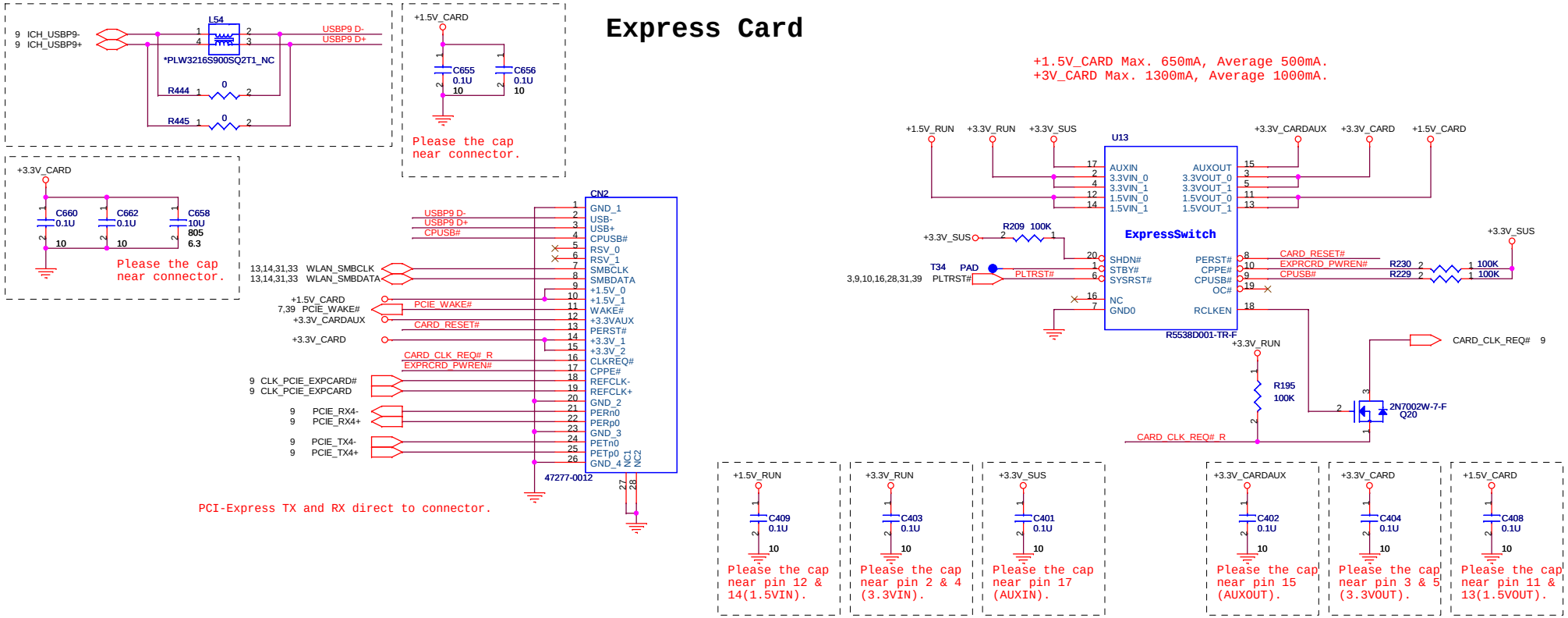
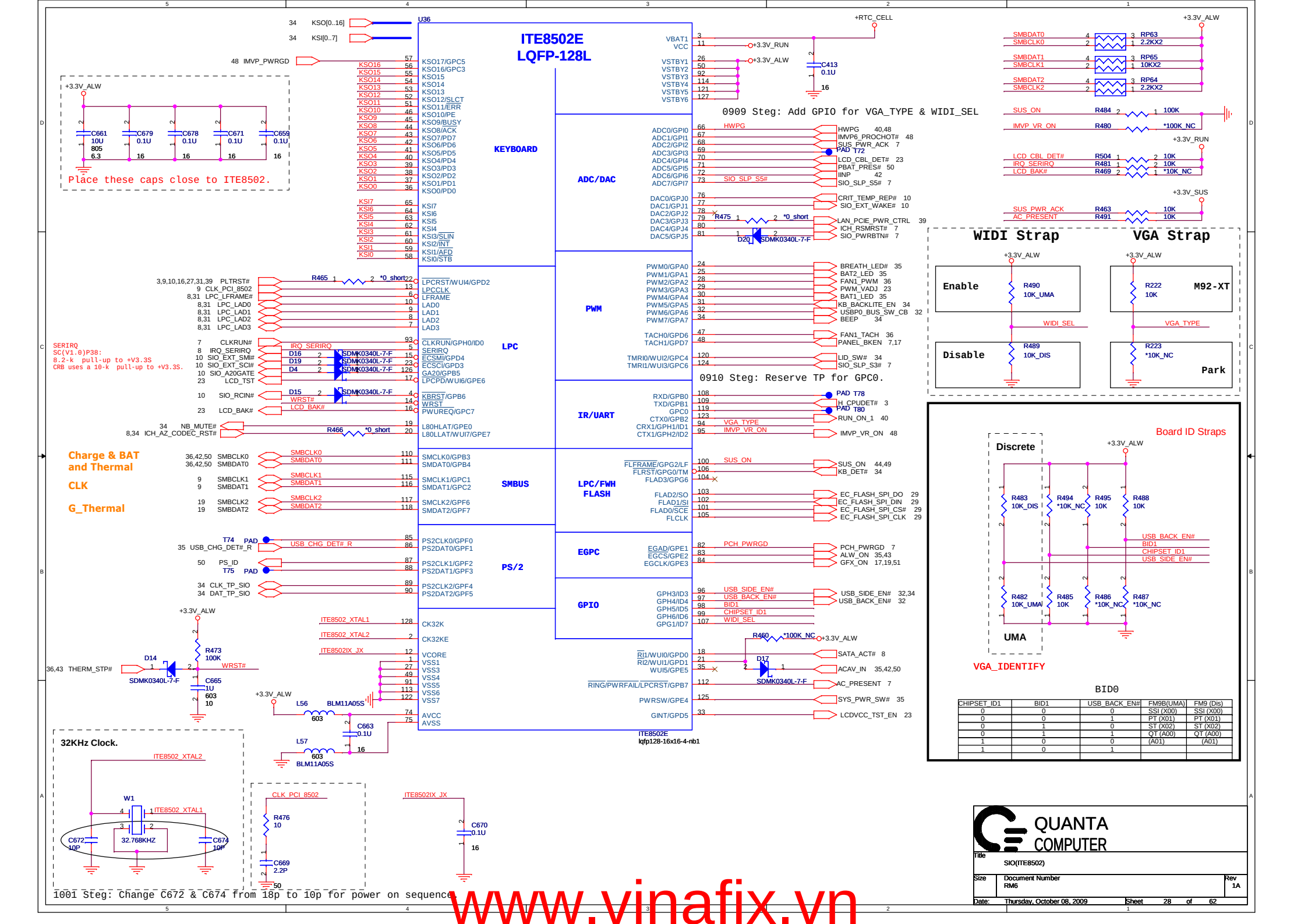
Express Card



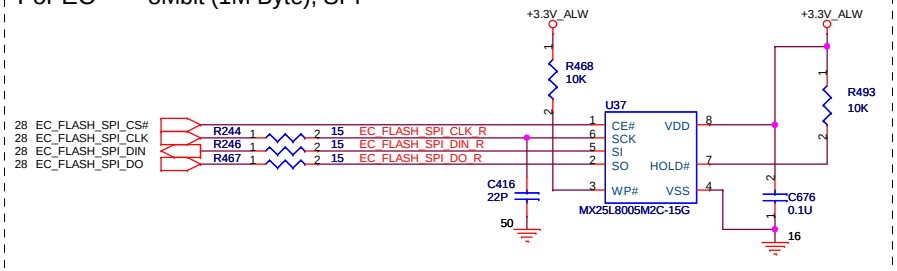
QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 27 of 62	

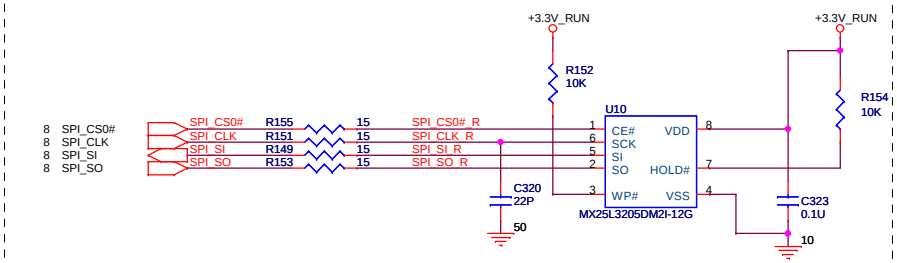


CHIPSET_ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		

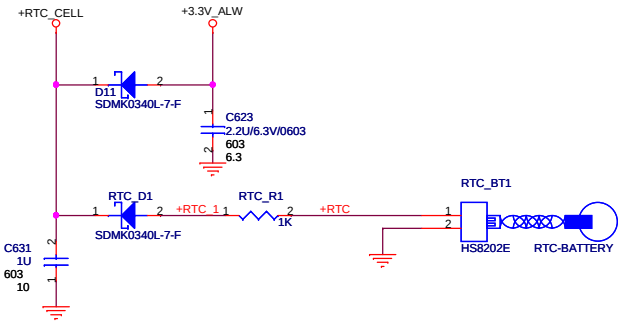
For EC 8Mbit (1M Byte), SPI



For PCH 64Mbit (8M Byte), SPI



RTC BATTERY



0818 Steg: Change Location for RTC_D1 & RTC_R1 & RTC_BT1

QUANTA COMPUTER

Title	FLASH/RTC	
Size	Document Number RM6	Rev 1A
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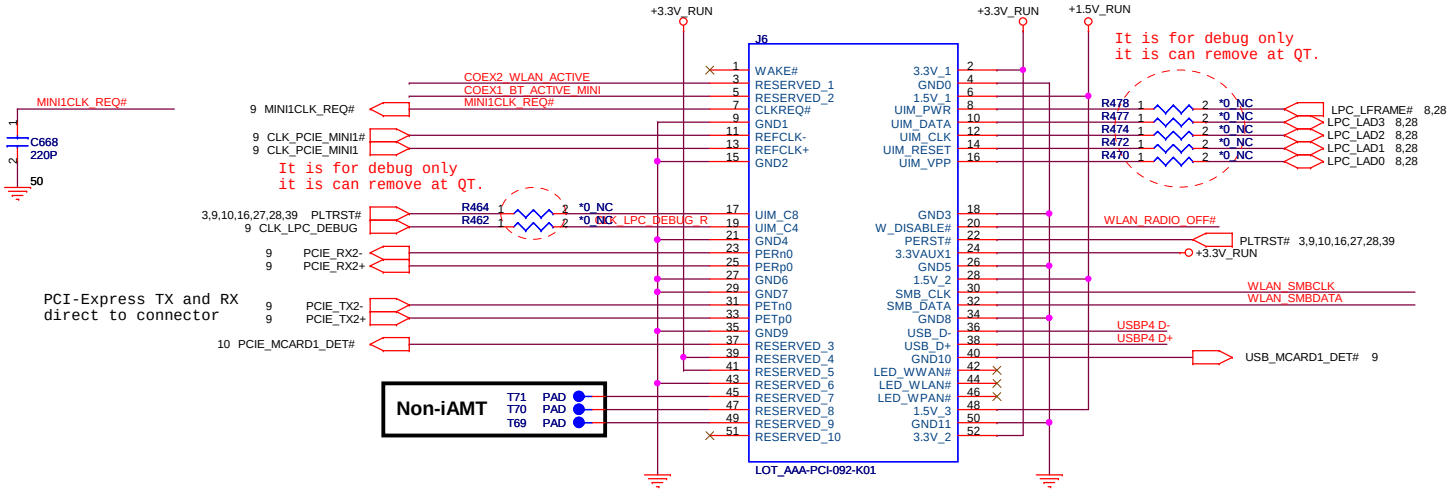
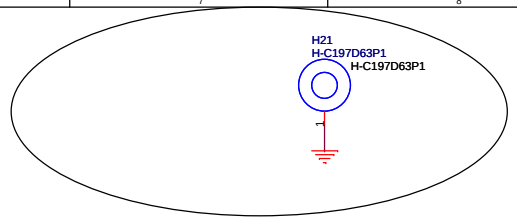
QUANTA COMPUTER

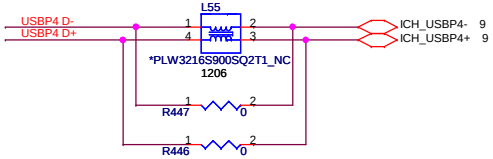
Title	Briadwood & MINI-PCI CONN	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 01, 2009	Sheet 30 of 62	

MiniCard WLAN connector

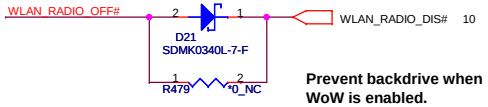




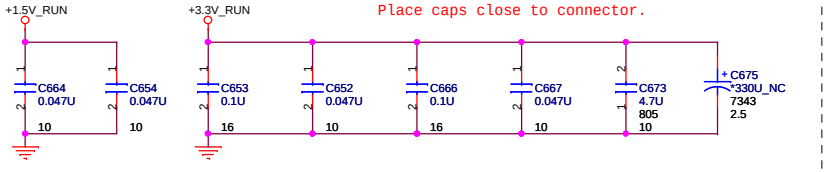
0906 Steg: Remove an Nut H22.



Suport for WoW

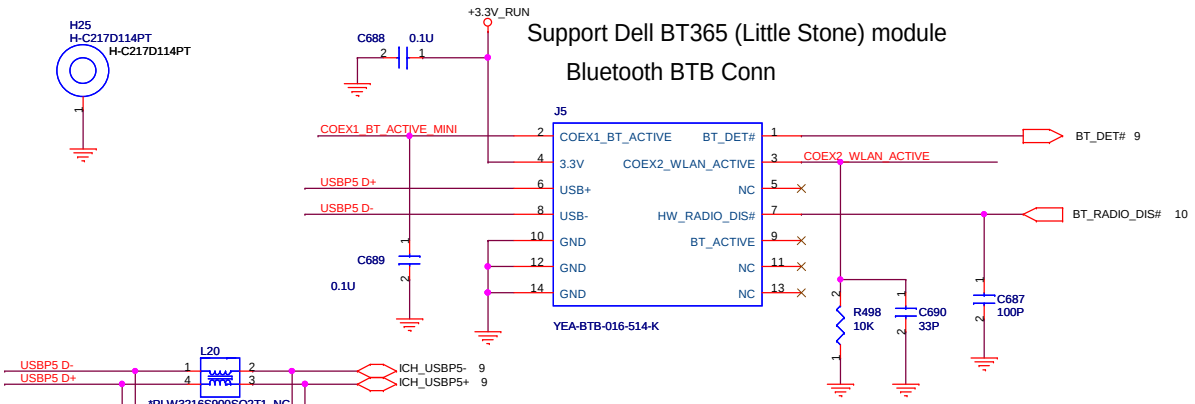


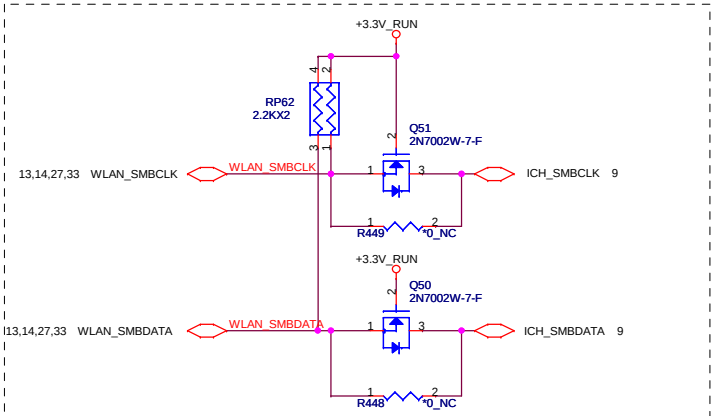
Prevent backdrive when
WoW is enabled.



Support Dell BT365 (Little Stone) module

Bluetooth BTB Conn





QUANTA COMPUTER

Title	WLAN & BT CONN	
Size	Document Number RM6	Rev 1A
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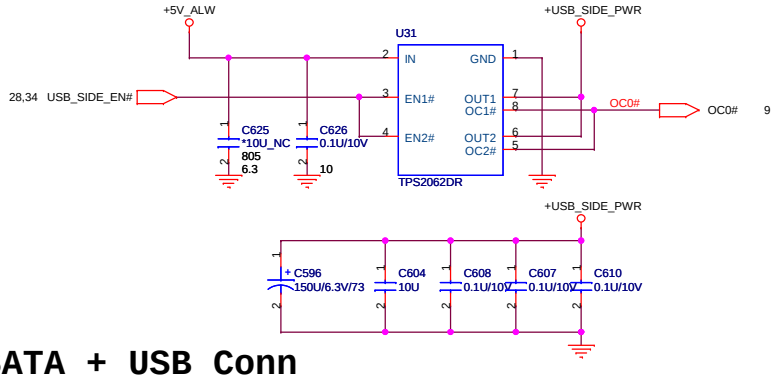
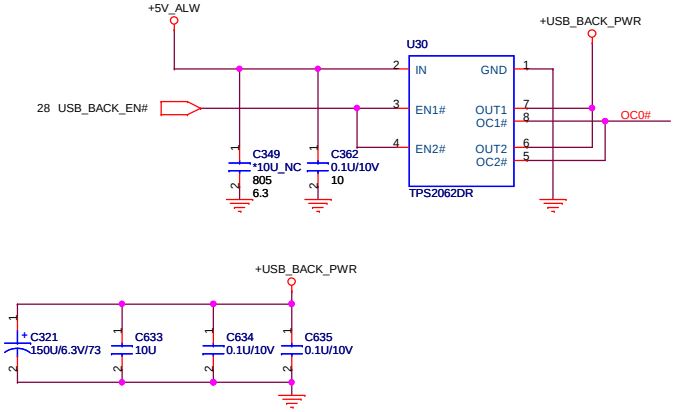
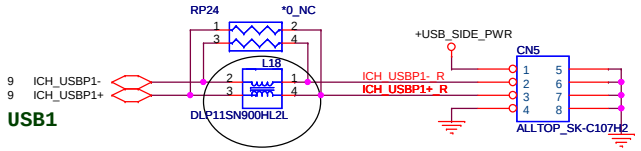
USB Conn

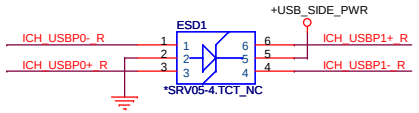


SATA + USB Conn

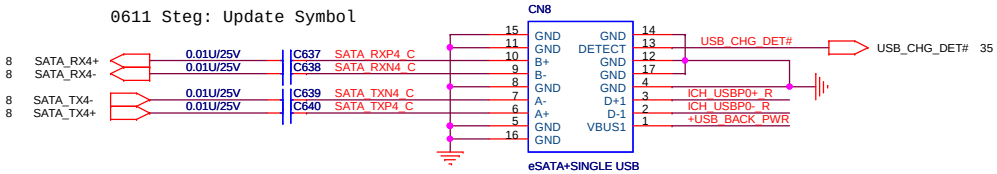


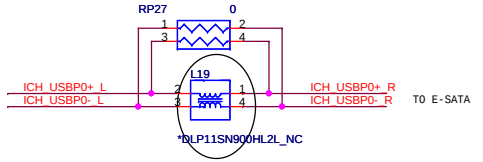
1007 Steg : Change L18,L19 Footprint.



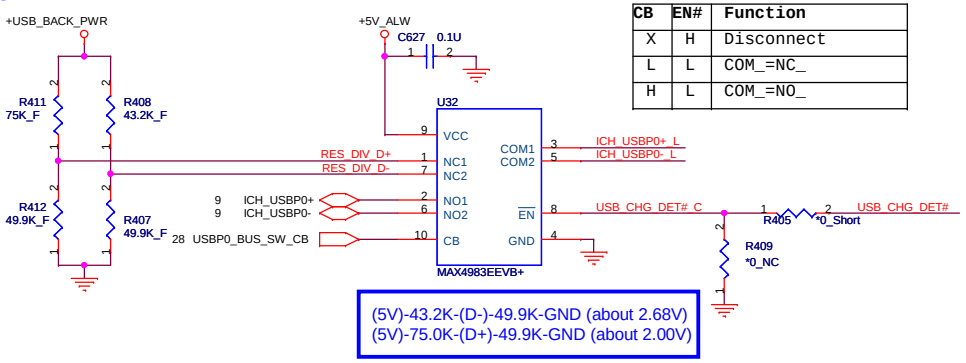


0611 Steg: Update Symbol





USB Charge

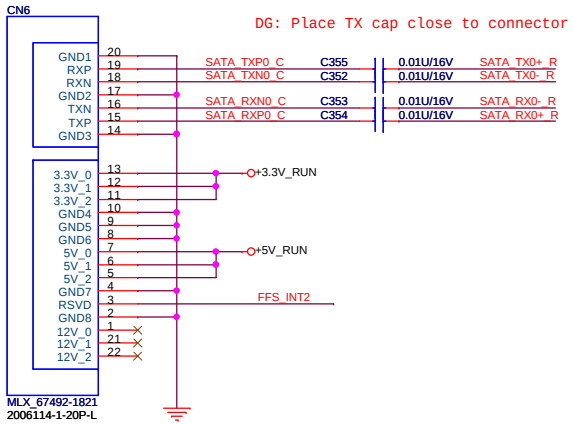


CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

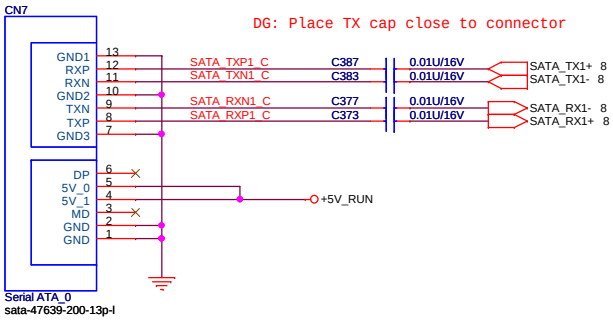
QUANTA COMPUTER

Title	USB & E-SATA CONN	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 32 of 62	

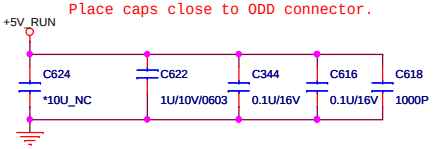
SATA Connector.



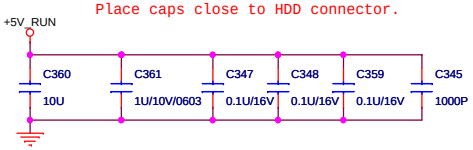
ODD Connector



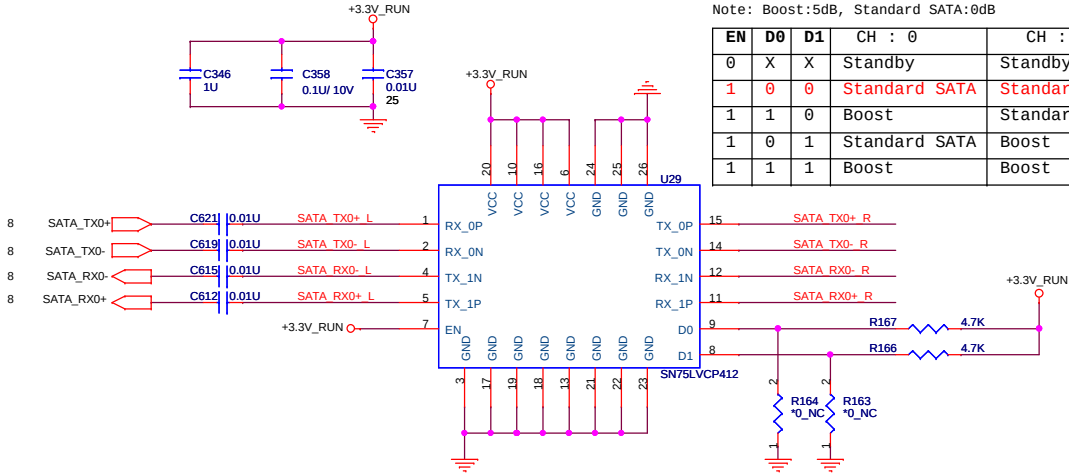
Place caps close to ODD connector.



Place caps close to HDD connector.



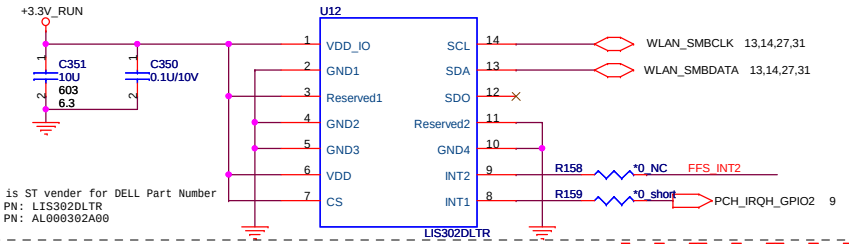
HDD-SATA Re-driver



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

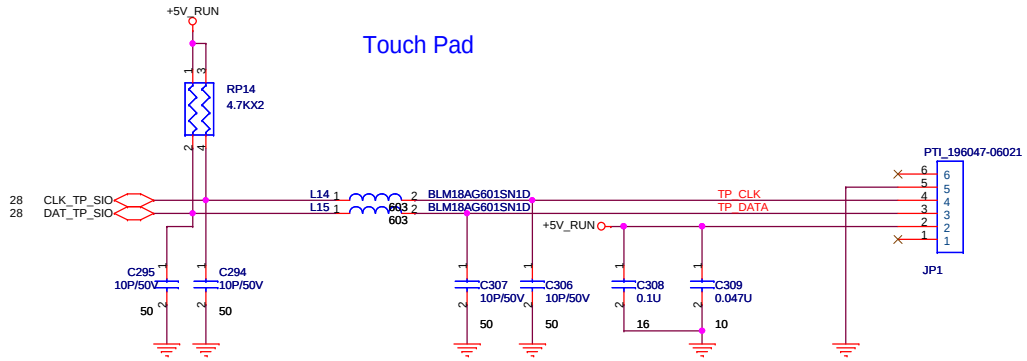
3-axis Fall Sensor (HDD data protector)



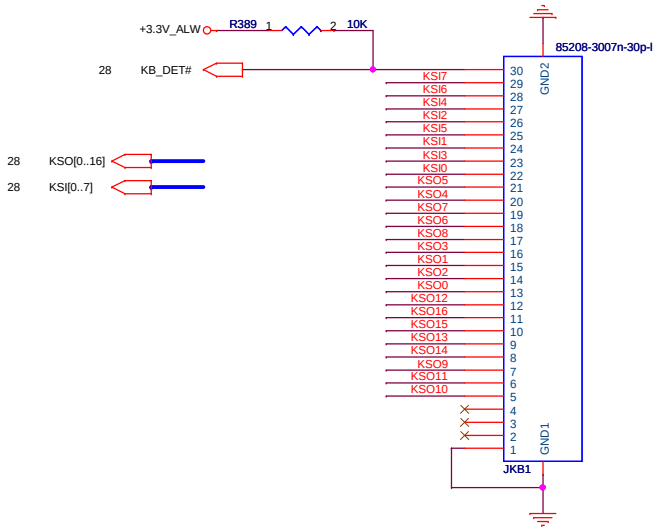
QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 33 of 62	

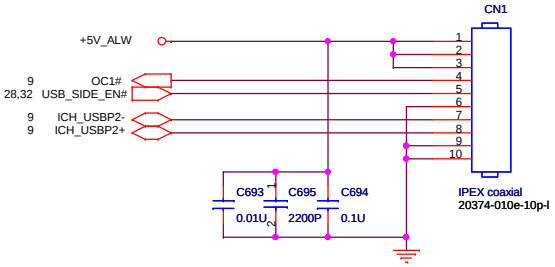
Touch Pad

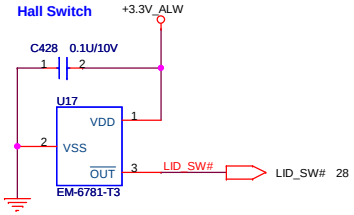


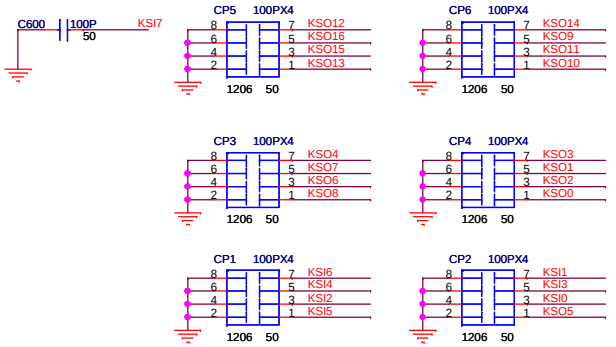
KEYBOARD CONNECTOR



Daughter Board Connector (One USB Port)

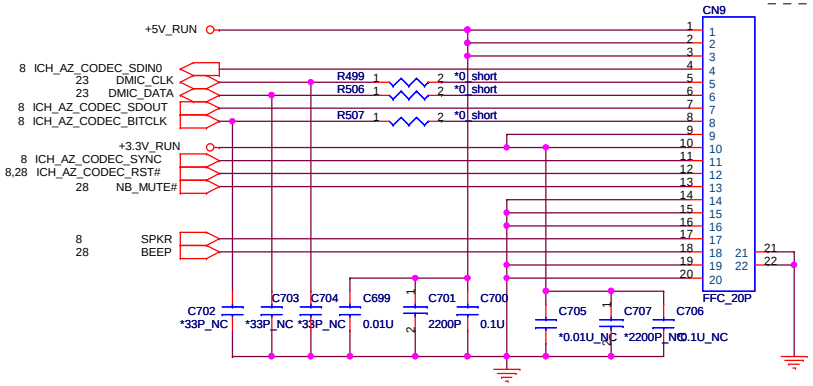






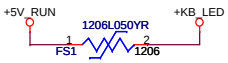
100P CAPS CLOSE TO JKB1

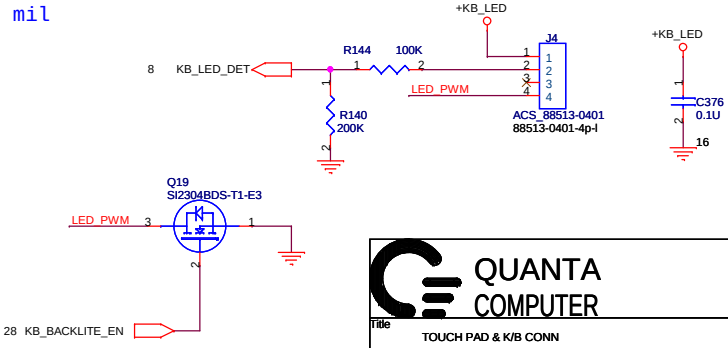
Daughter Board Connector (HP & MIC Jack)



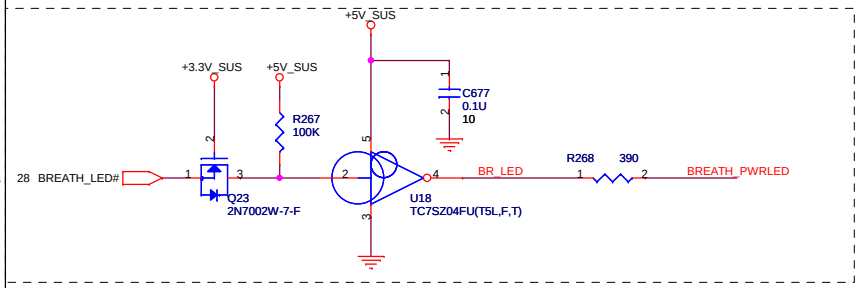
Key board illumination

+KB_LED power trace width >10 mil

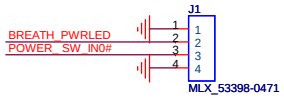




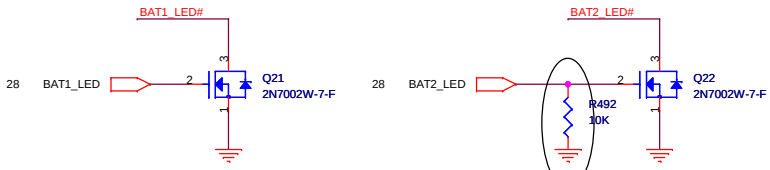
QUANTA COMPUTER		
Title: TOUCH PAD & K/B CONN		
Size	Document Number: RM6	Rev: 1A
Date: Thursday, October 08, 2009	Sheet 34 of 62	



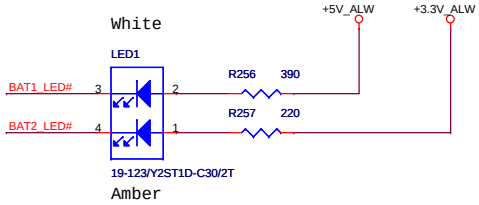
Power button Cable



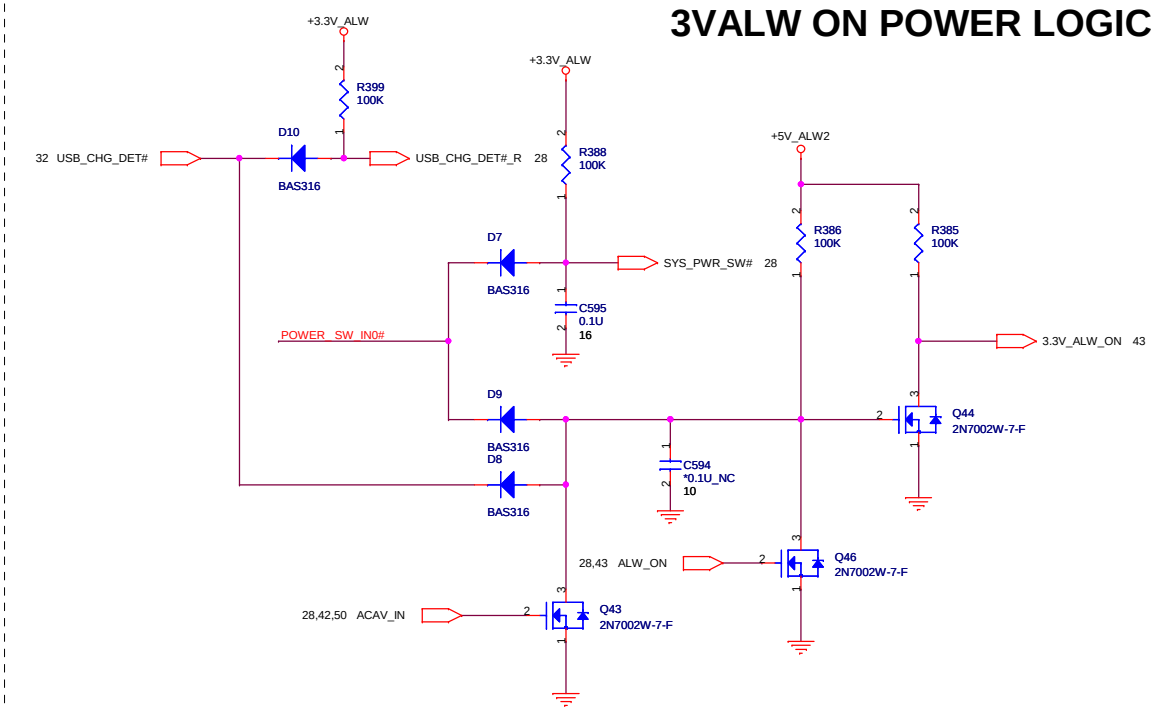
Battery status.



1007 Steg : Add an External Pull Down for BAT2_LED



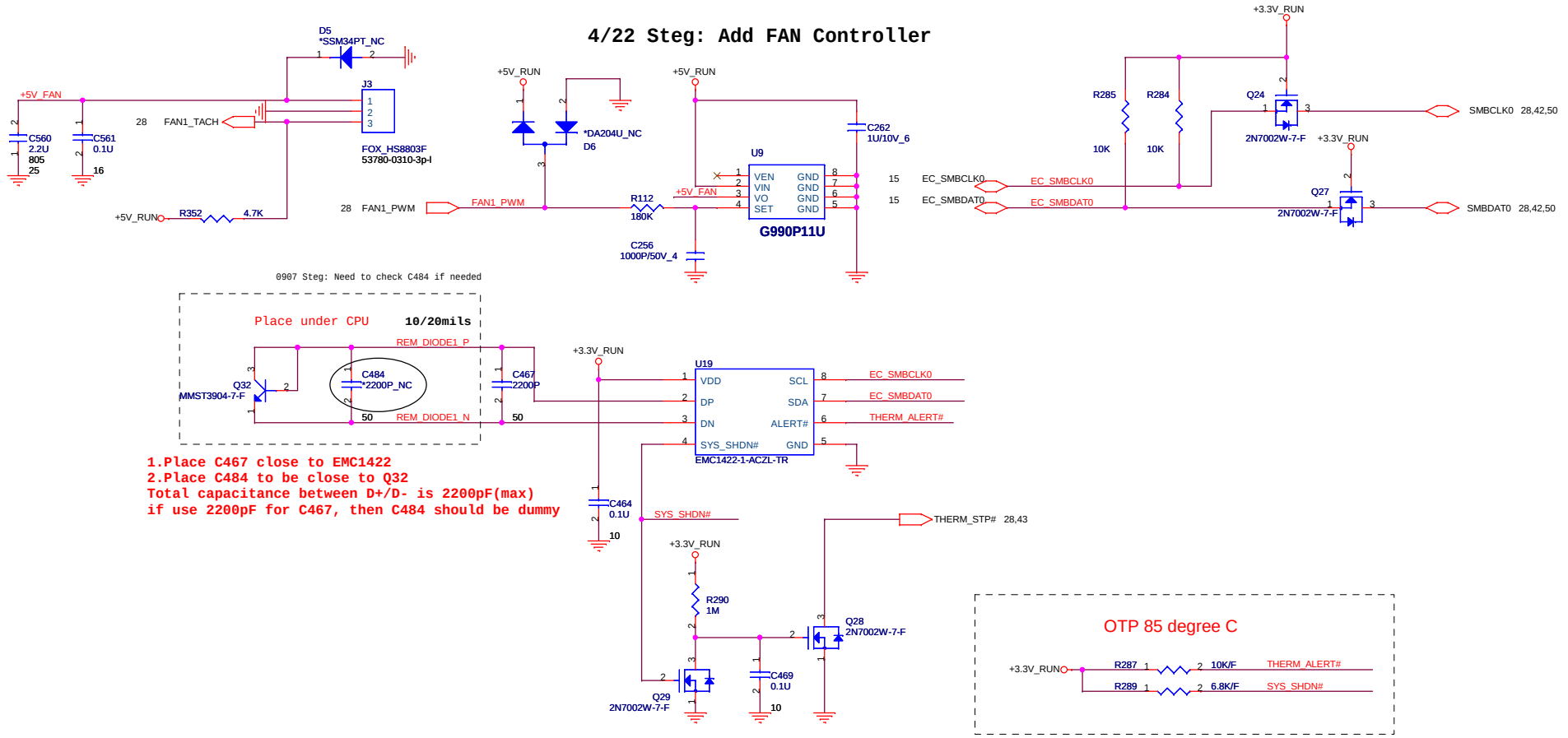
3VALW ON POWER LOGIC



QUANTA COMPUTER

Title	LED 3V_ALW Power Logic	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 35 of 62	

4/22 Steg: Add FAN Controller



Title	FAN & THERMAL	
Size	Document Number RM6	Rev 1A
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QUANTA COMPUTER

Title	Azelia CODEC	
Size	Document Number RM6	Rev 1A
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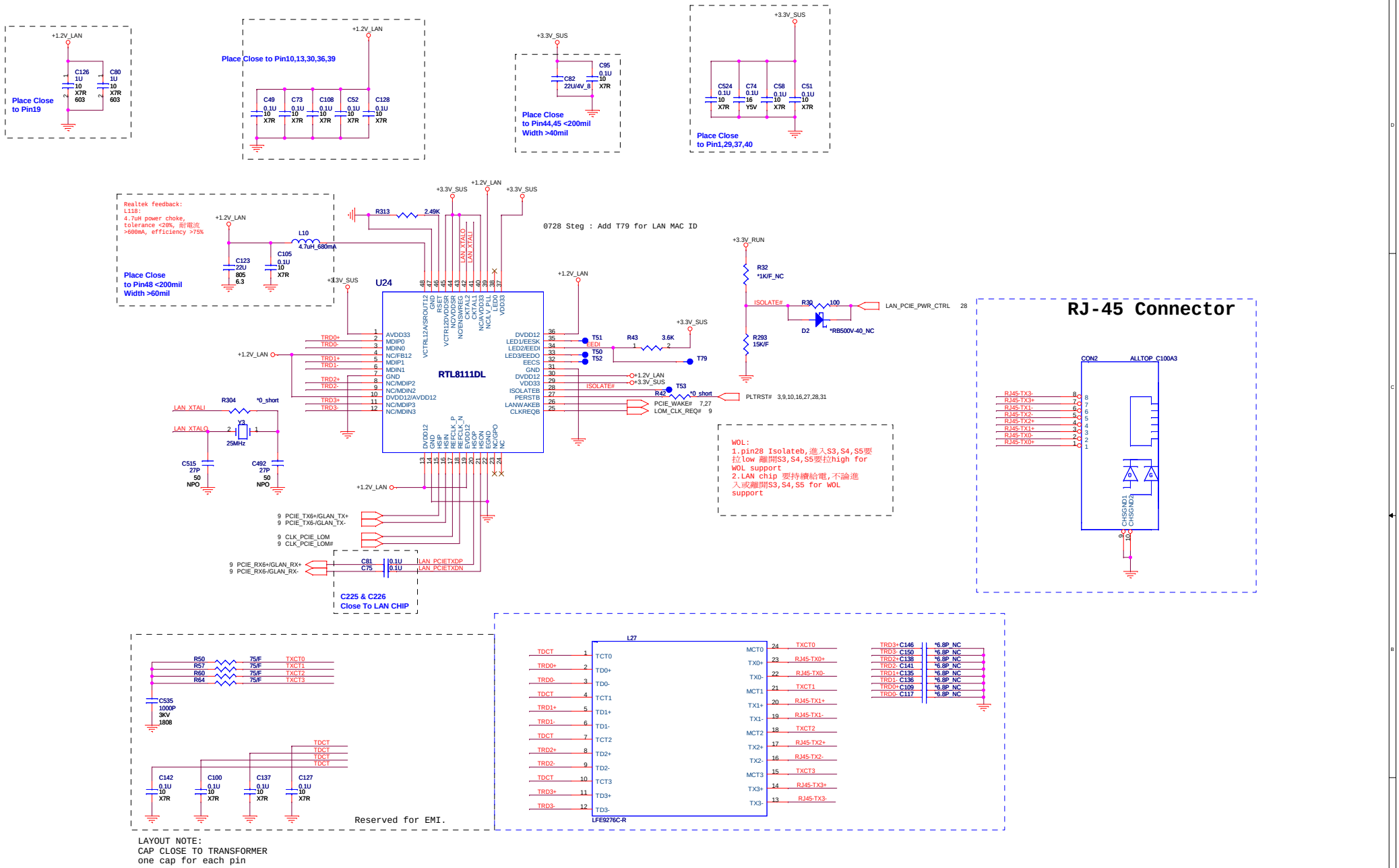
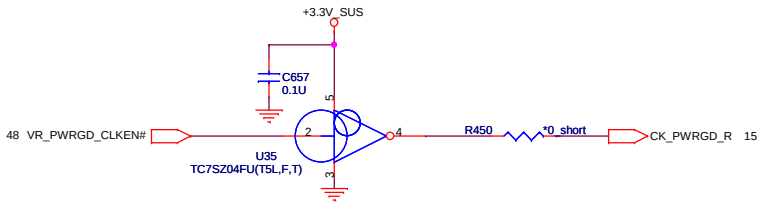
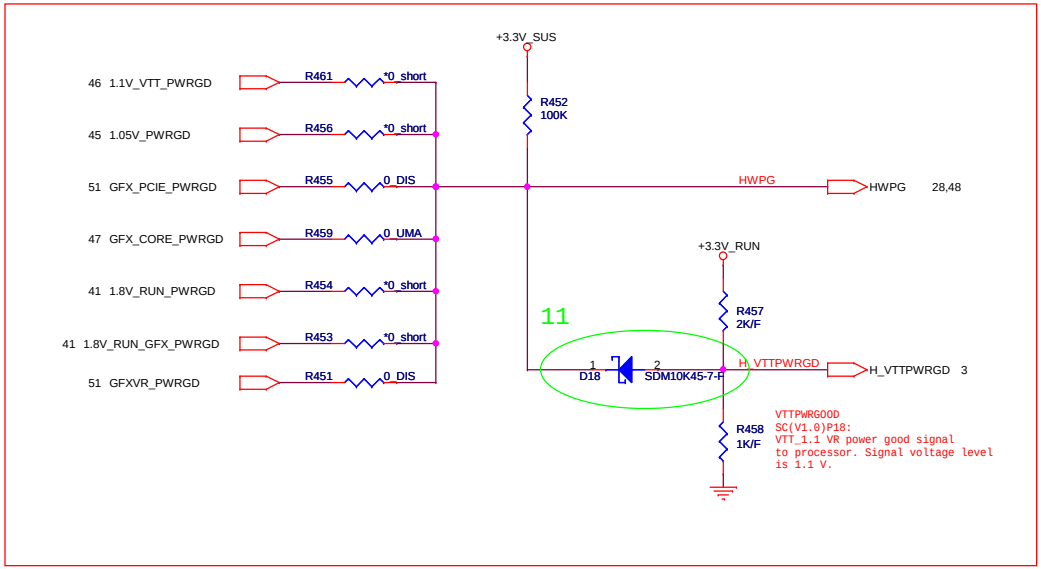
QUANTA COMPUTER

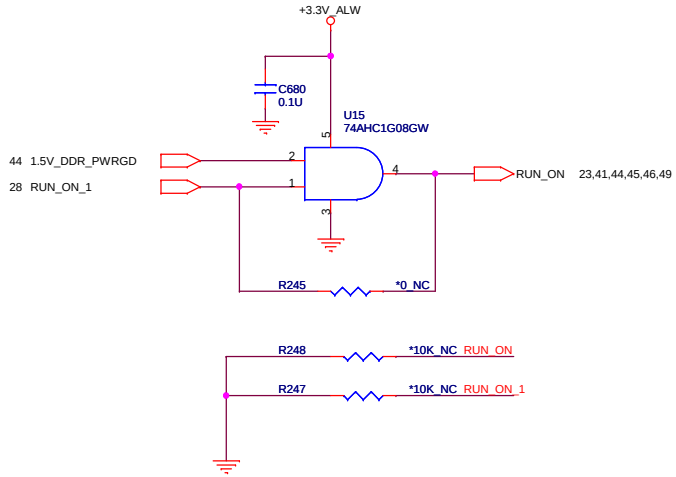
Title	D/B & CCD CONN	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 01, 2009	Sheet 38 of 62	



QUANTA COMPUTER		
Title	LAN	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 39 of 62	

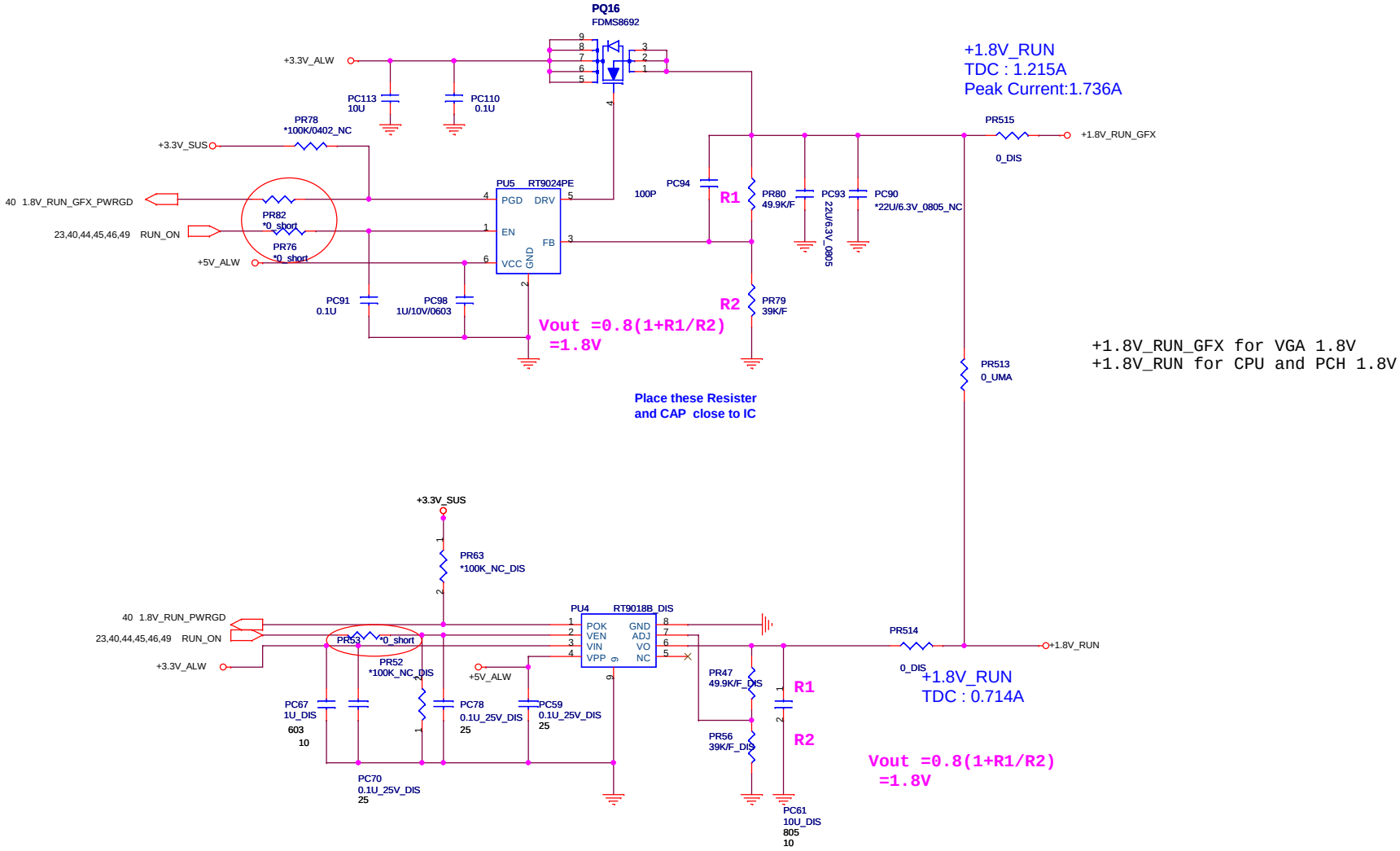




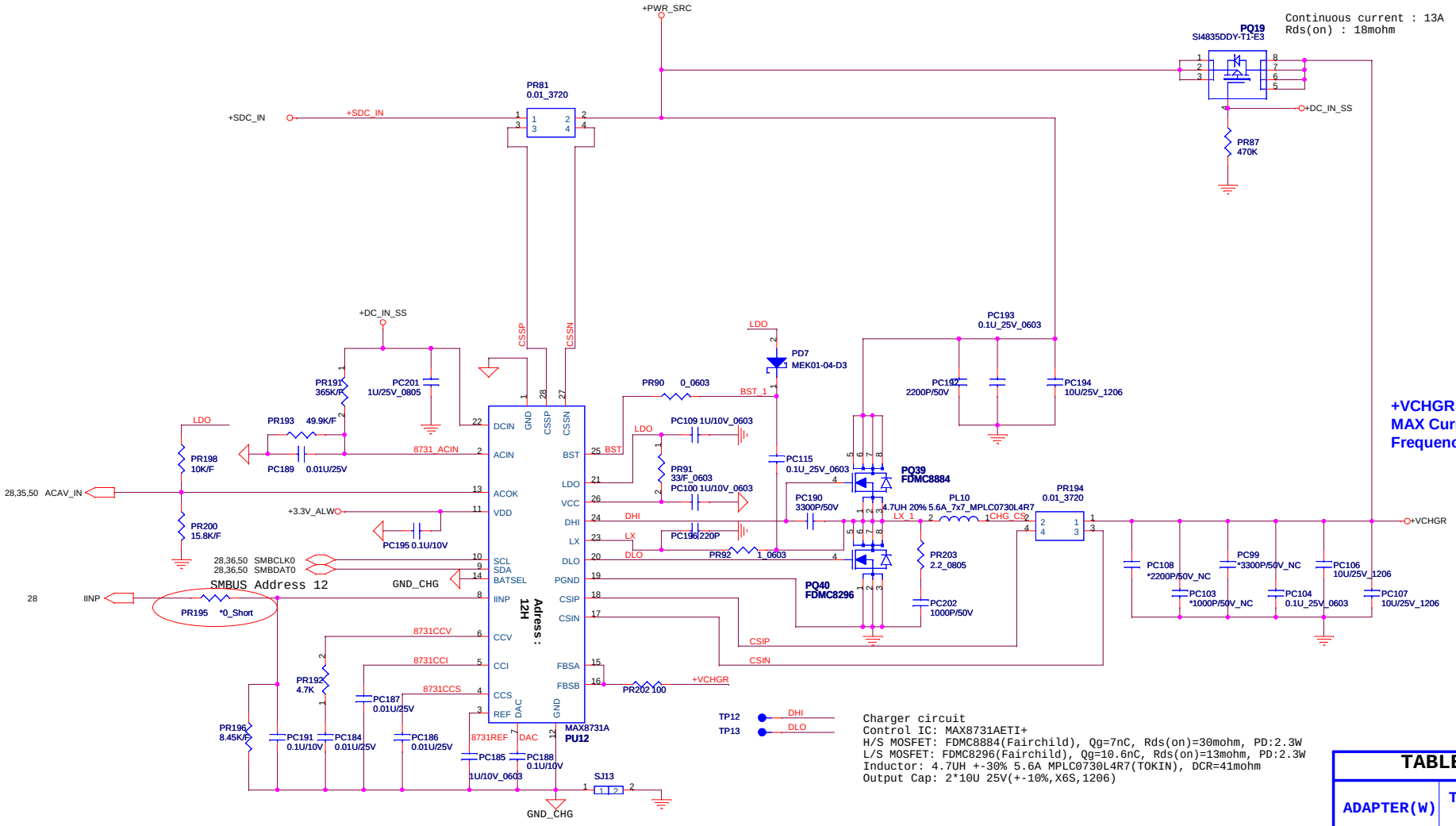


QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number FM9	Rev 1A
Date: Thursday, October 08, 2009	Sheet 40 of 62	



Title	<Title>	
Size	Document Number Custom RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 41 of 62	



+VCHGR
MAX Current : 4.8A
Frequency : 400KHz

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

QUANTA COMPUTER

Title	Charger (MAX8731A)	
Size	Document Number RM6	Rev 1A
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DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

+5V_ALW
Control IC: TPS51427A
H/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD:2.3W
L/S MOSFET: FDMC8678S(Fairchild), Qg=16nC, Rds(on)=8.7mohm, PD:2.3W
Inductor: 1.5UH +-20% 17.1A FDVE1040-H-1R5M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*220U 6.3V(20%,ESR25,7343,H=1.9),ripple current 2700mA

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD:2.3W
L/S MOSFET: FDMC8678S(Fairchild), Qg=16nC, Rds(on)=8.7mohm, PD:2.3W
Inductor: 1.5UH +-20% 17.1A FDVE1040-H-1R5M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

+5V_ALW
Frequency : 400KHz
TDC : 8.271A
Peak current : 11.816A
OCP : 14.18A

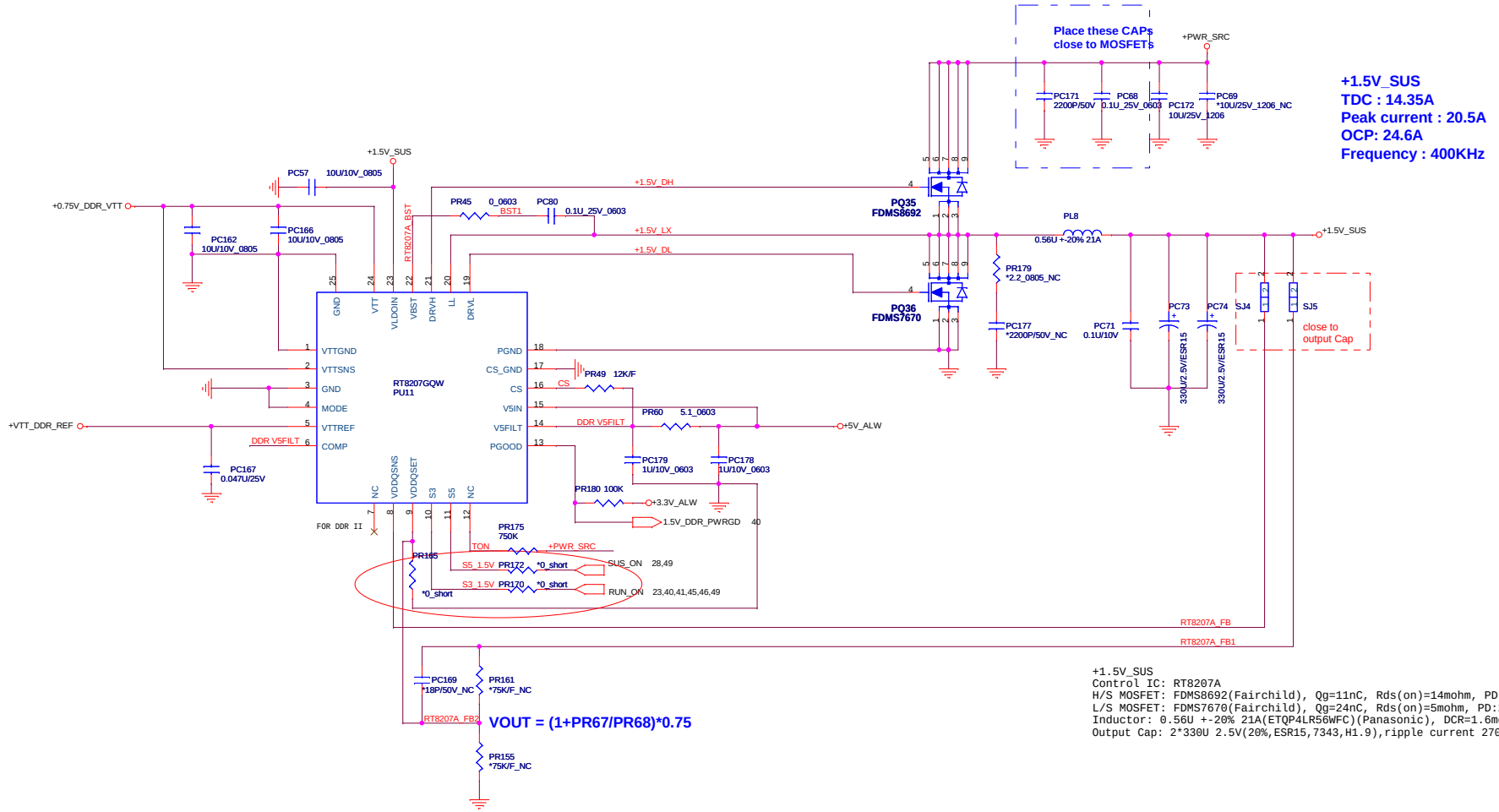
+3.3V_ALW
Frequency : 300KHz
TDC : 8.23A
Peak current : 11.77A
OCP : 14A

Pop for MAX17020

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

0716 Jim: de-pop PD10

Title	3VALW,5V,3V, Power On (MAX17020)		
Size	Document Number RM6		Rev 1A
Date:	Thursday, October 08, 2009	Sheet 43 of 62	



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

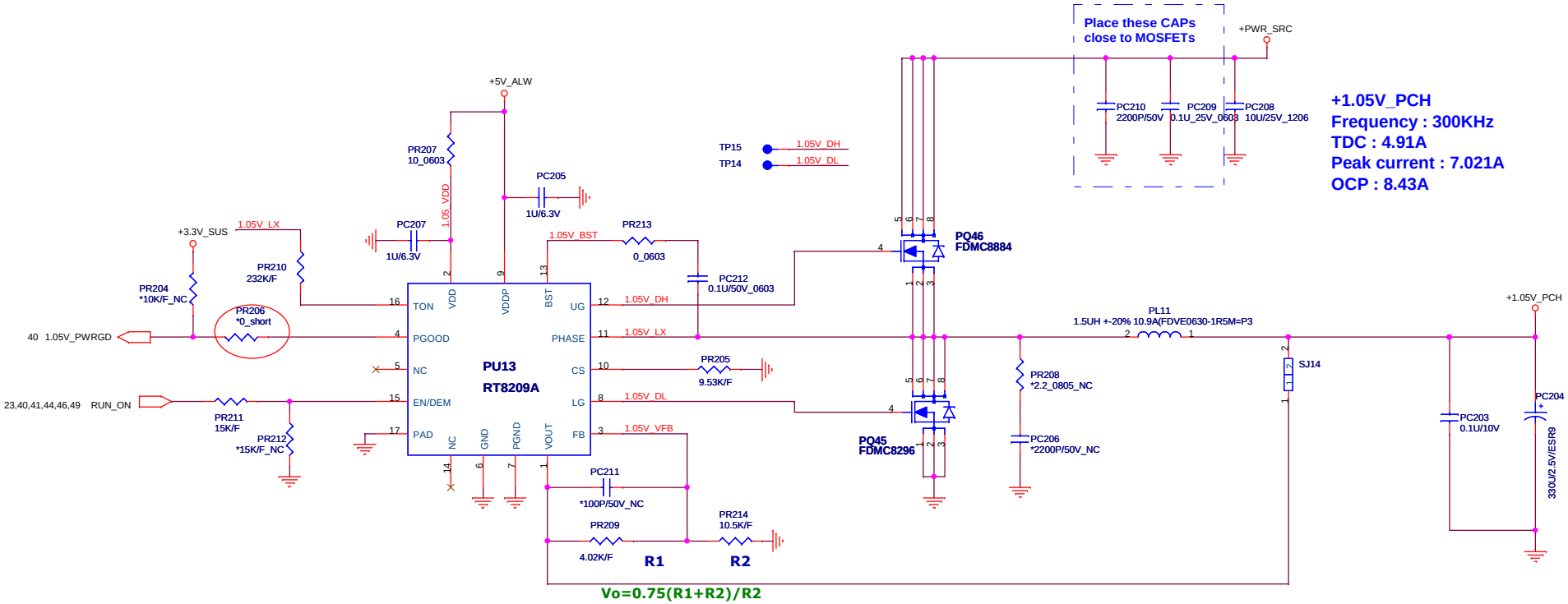
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

QUANTA COMPUTER

Title: 1.8VSUS & 0.9VTT (TPS51116)

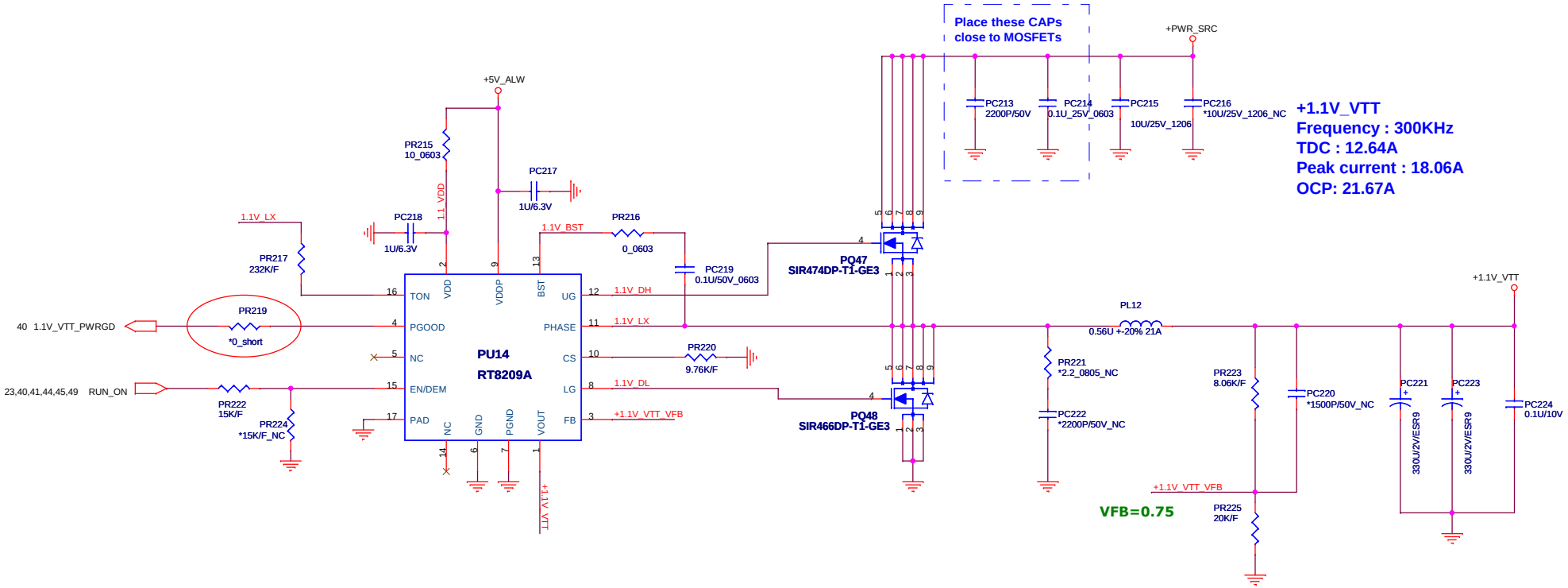
Size: | Document Number: RM6 | Rev: 3A

Date: Thursday, October 08, 2009 | Sheet 44 of 62



+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDMC8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.3W
L/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD:2.3W
Inductor: 1.5UH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR9,7343,H1.9),ripple current 2700mA

Title	<Title>	
Size: CustomRM6	Document Number	Rev: 1A
Date: Thursday, October 08, 2009	Sheet 45 of 62	




```
+1.1V_VTT
Control IC: RT8209A
H/S MOSFET: SIR474DP(Vishay), Qg=12nC, Rds(on)=12mohm, PD:3.9W
L/S MOSFET: SIR466DP(VIshay), Qg=33nC, Rds(on)=5.1mohm, PD:5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA
```

Title	<Title>	
Size: CustomRM6	Document Number	Rev: 1A
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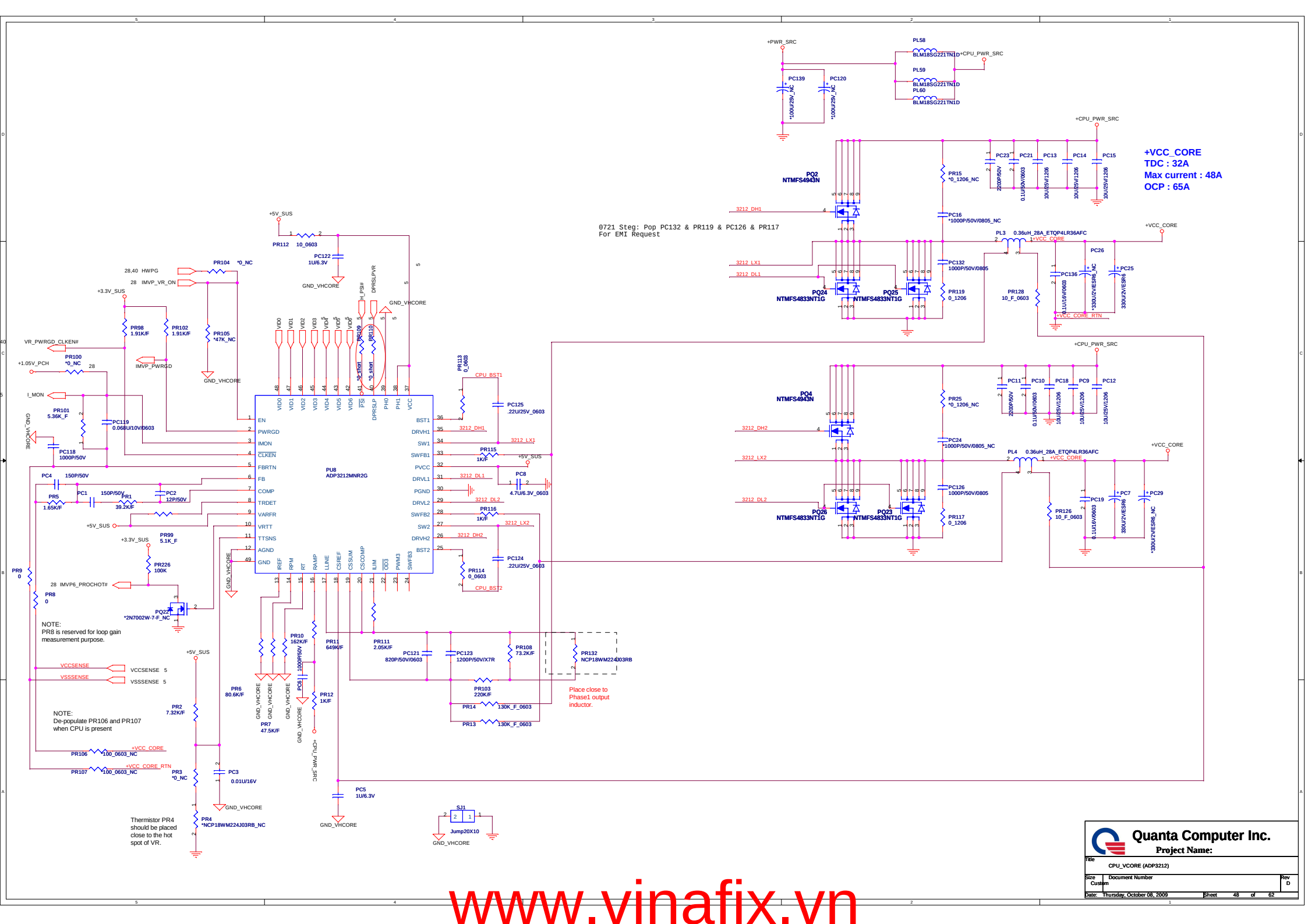
+VCC_GFX_CORE
Control IC: MAX17028
H/S MOSFET: NTMFS4921NT1G(ON-SEMI), Qg=14.4nC, Rds(on)=10.5mohm, PD:2.14W
L/S MOSFET: NTMFS4833NT1G(ON-SEMI), Qg=58nC, Rds(on)=3mohm, PD:2.35W
Inductor: 0.36UH +-20% 24A ETQP4LR36WFC(Panasonic), DCR=1.1mohm
Output Cap: 2*330U 2V(20%,ESR9,7343,H1.9),ripple current 2700mA

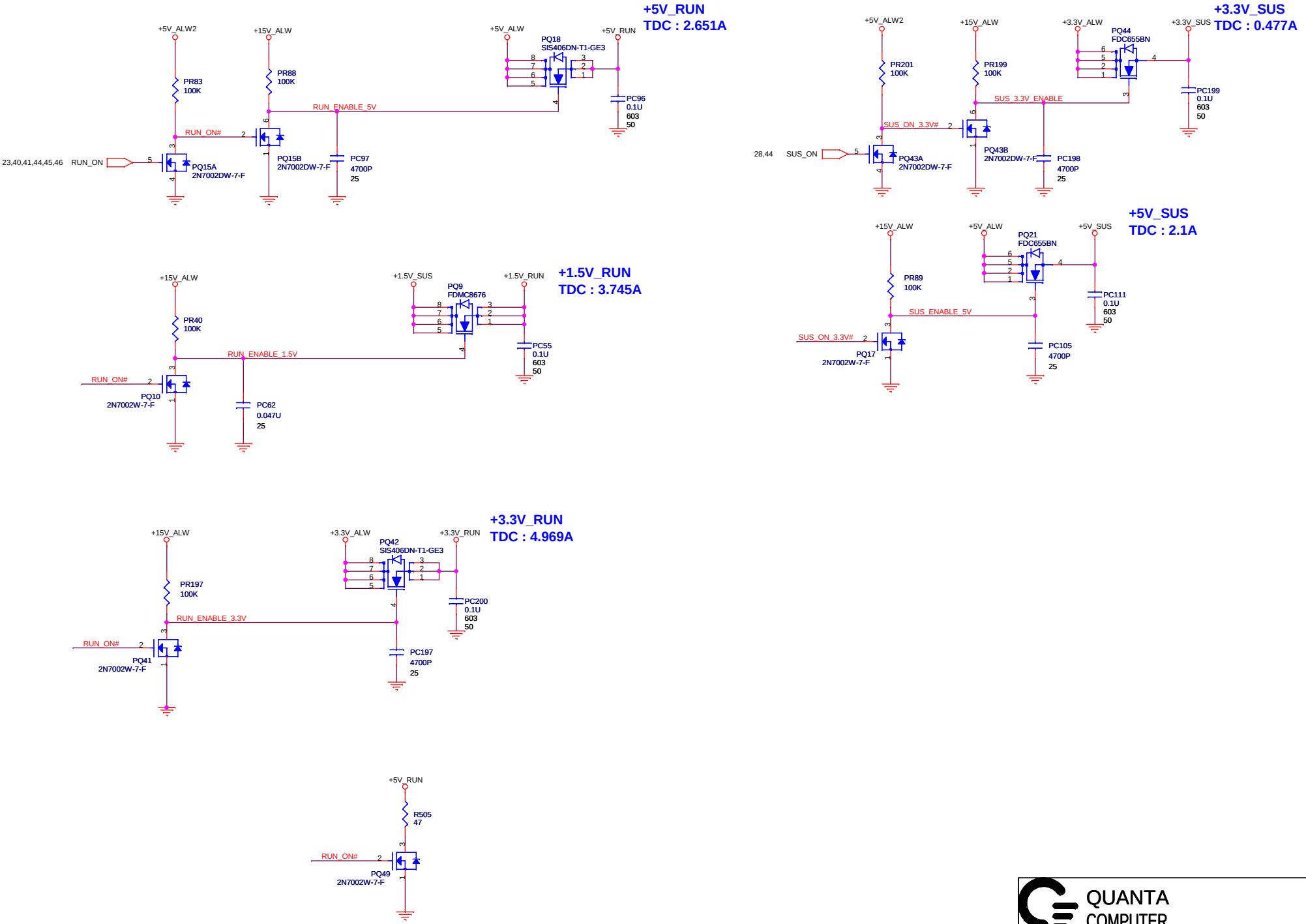
+VCC_GFX_CORE
Frequency : 400K
TDC : 12A
Peak current : 22A
OCP:26.4A

MAX17028_UMA
PQ6 NTMFS4921NT1G_UMA
PQ5 NTMFS4833NT1G_UMA
PL5 0.36uH_24A_ETQP4LR36WFC_UMA

QUANTA COMPUTER

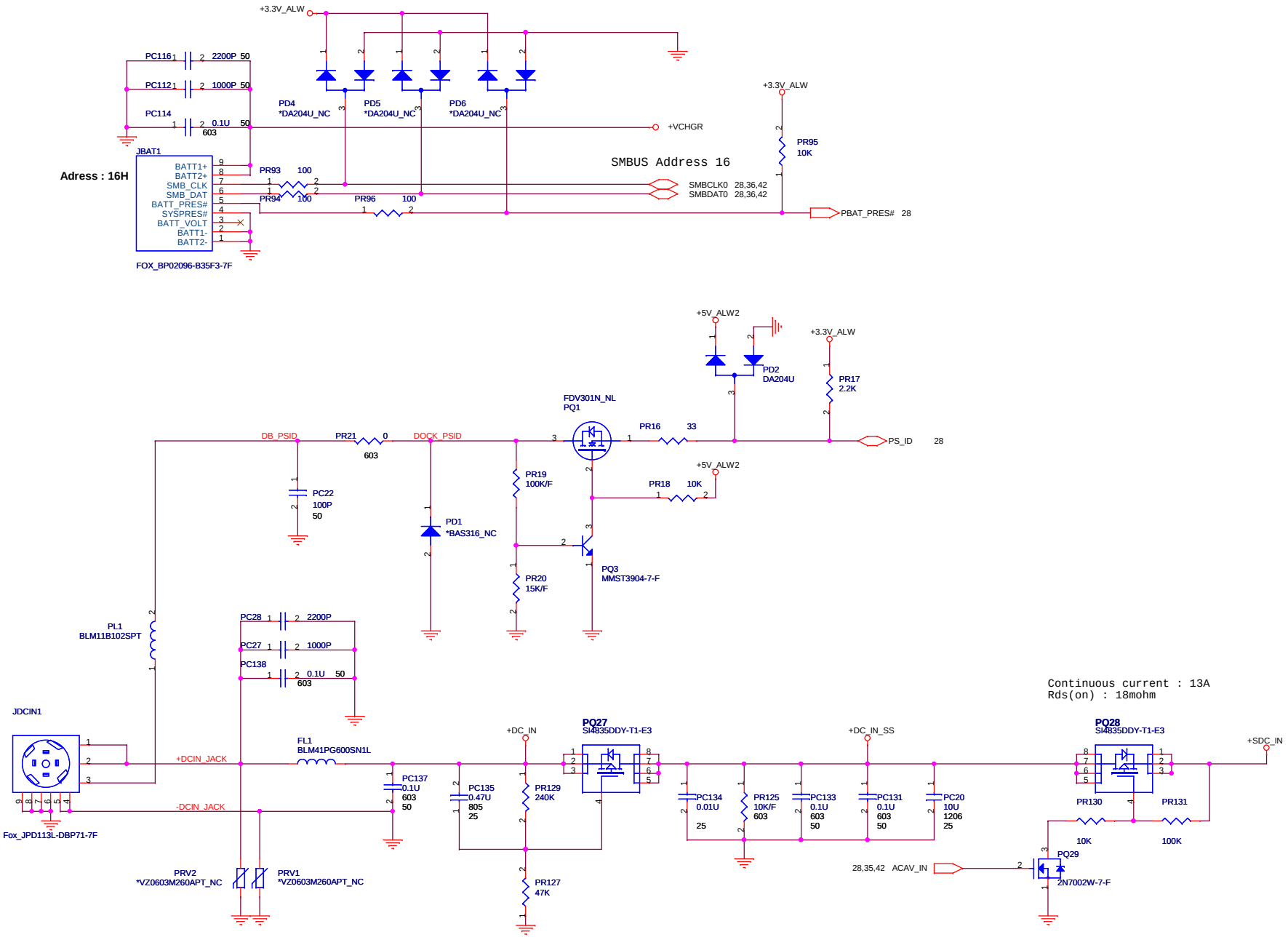
Title: VGA DC/DC
Size: Document Number RM6 Rev 0.5A
Date: Thursday, October 08, 2009 Sheet 47 of 62





QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number RM6	Rev 1A
Date: Thursday, October 08, 2009	Sheet 49 of 62	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number RM6	Rev 1A
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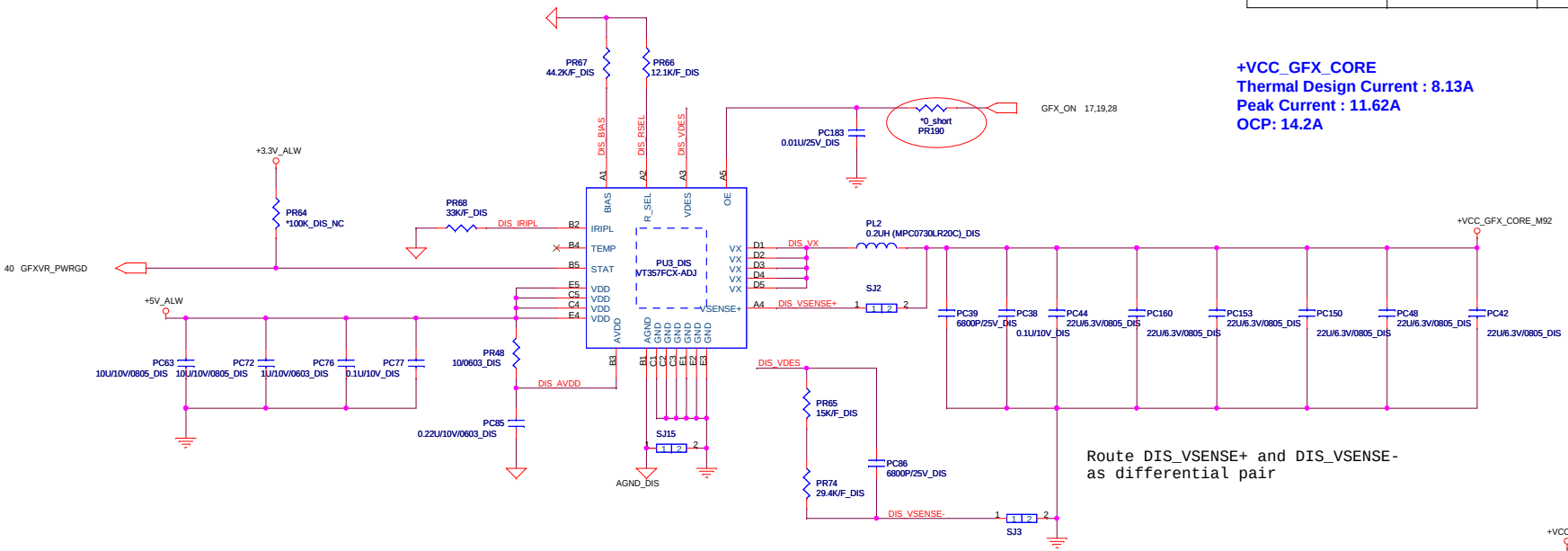
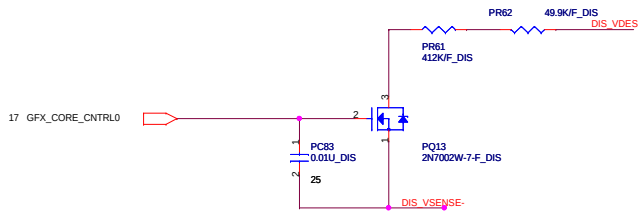
+VCC_GFX_CORE_M92

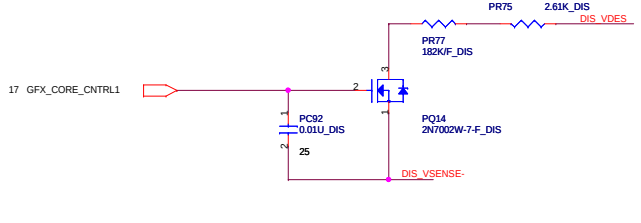
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	1.2V
HIGH	LOW	LOW	1.1V
HIGH	HIGH	LOW	0.9V

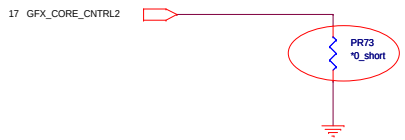
+VCC_GFX_CORE
Thermal Design Current : 8.13A
Peak Current : 11.62A
OCP: 14.2A

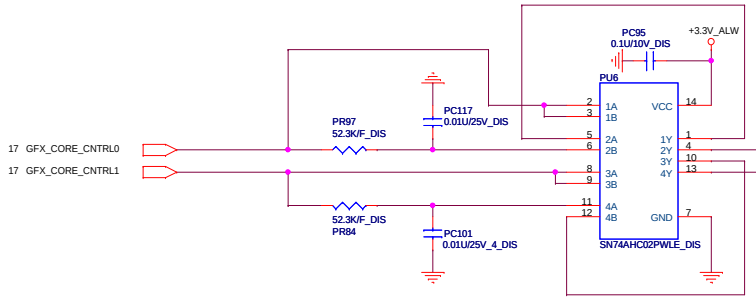


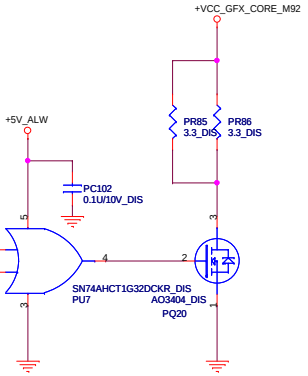
Route DIS_VSENSE+ and DIS_VSENSE- as differential pair

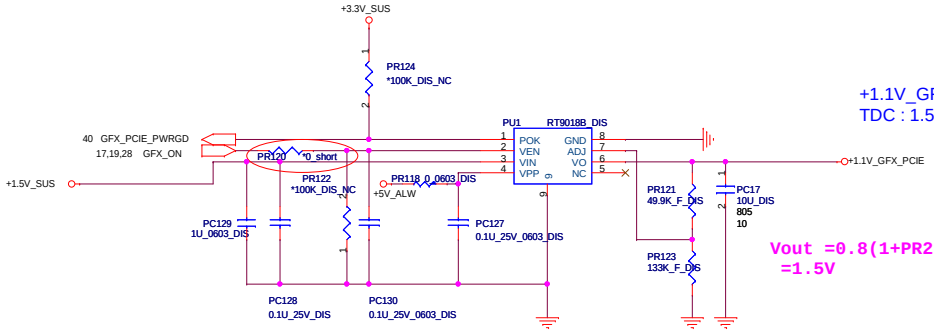












+1.1V_GFX_PCIE
TDC : 1.515A

Vout =0.8(1+PR210/PR212)
=1.5V

Title	VGA power (MAX8792 & RT9018B)		
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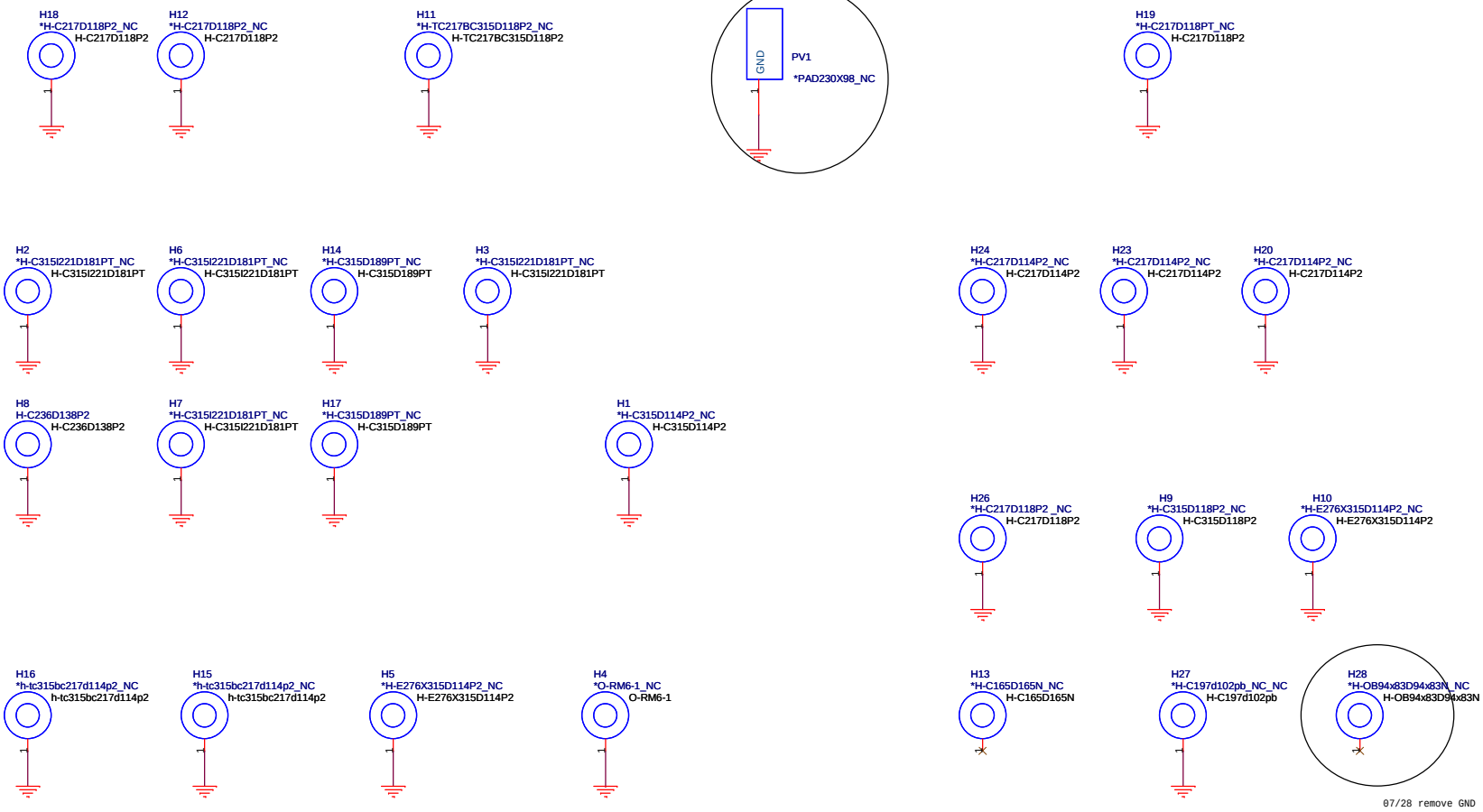
1008 Steg: Add an solder mask between CON1 and screw hole.



07/28 remove GND

QUANTA COMPUTER

Title	SCREW PAD	
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Reserved for EMI.

QUANTA COMPUTER

Title	EMI CAP	
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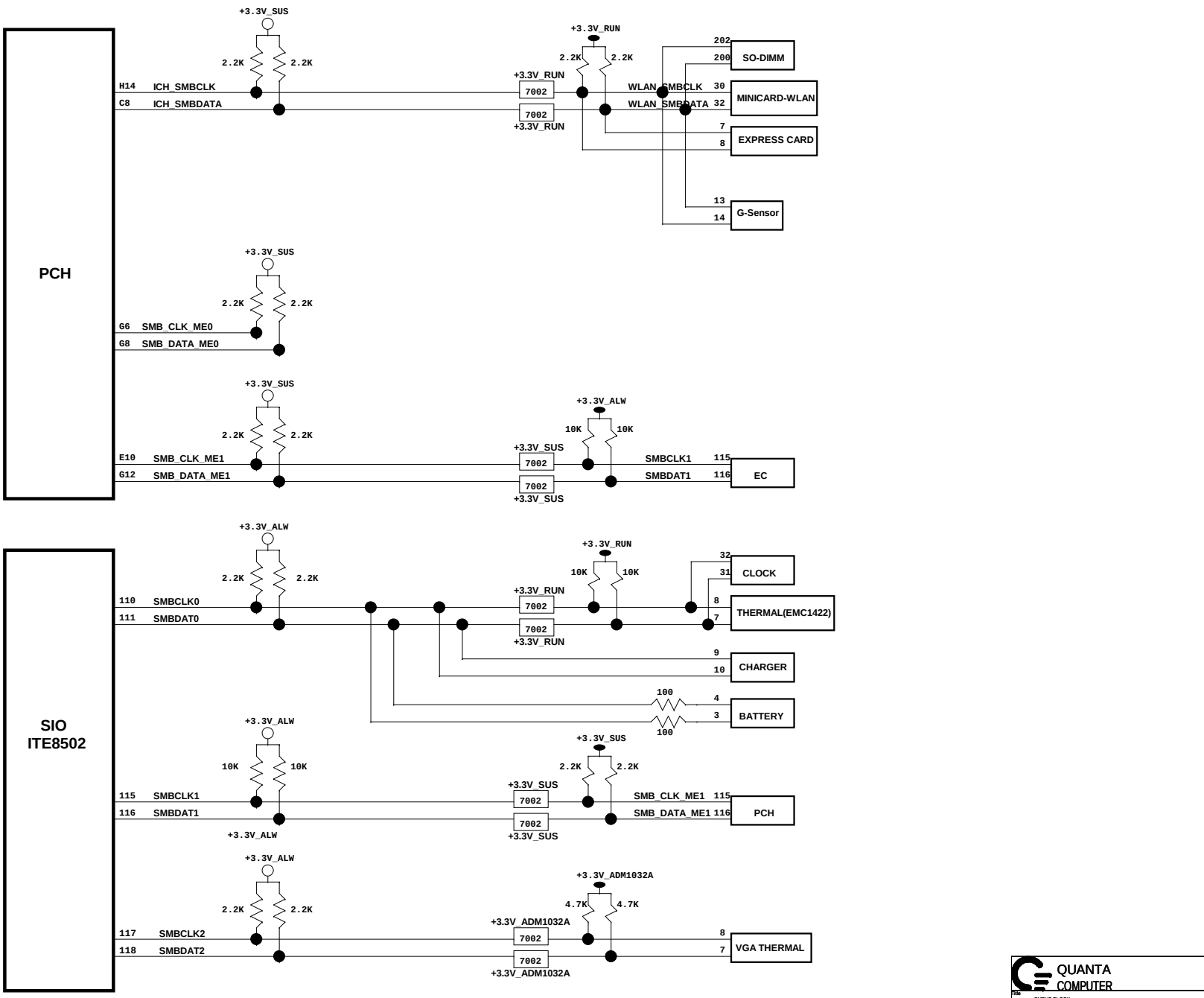

QUANTA COMPUTER

Title: SMBUS BLOCK

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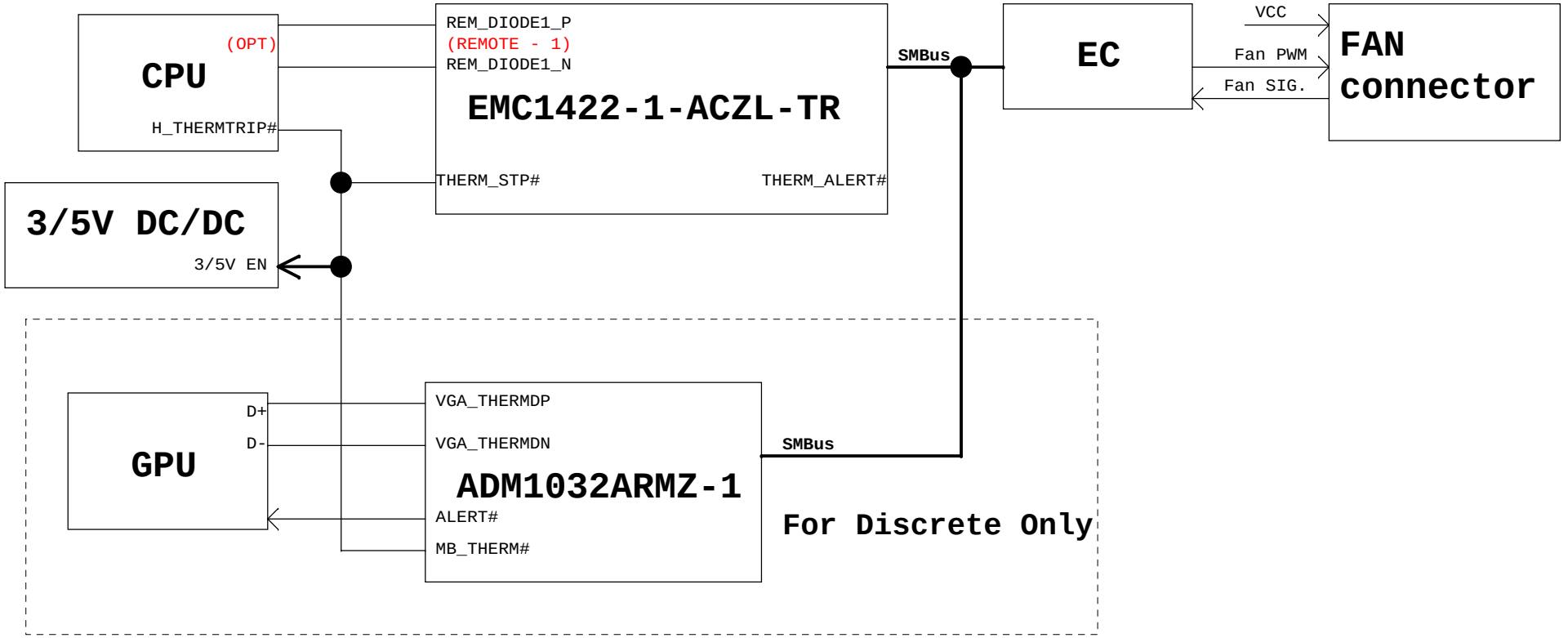

QUANTA COMPUTER

Title: Thermal Map		
Size	Document Number: RM6	Rev: 1A
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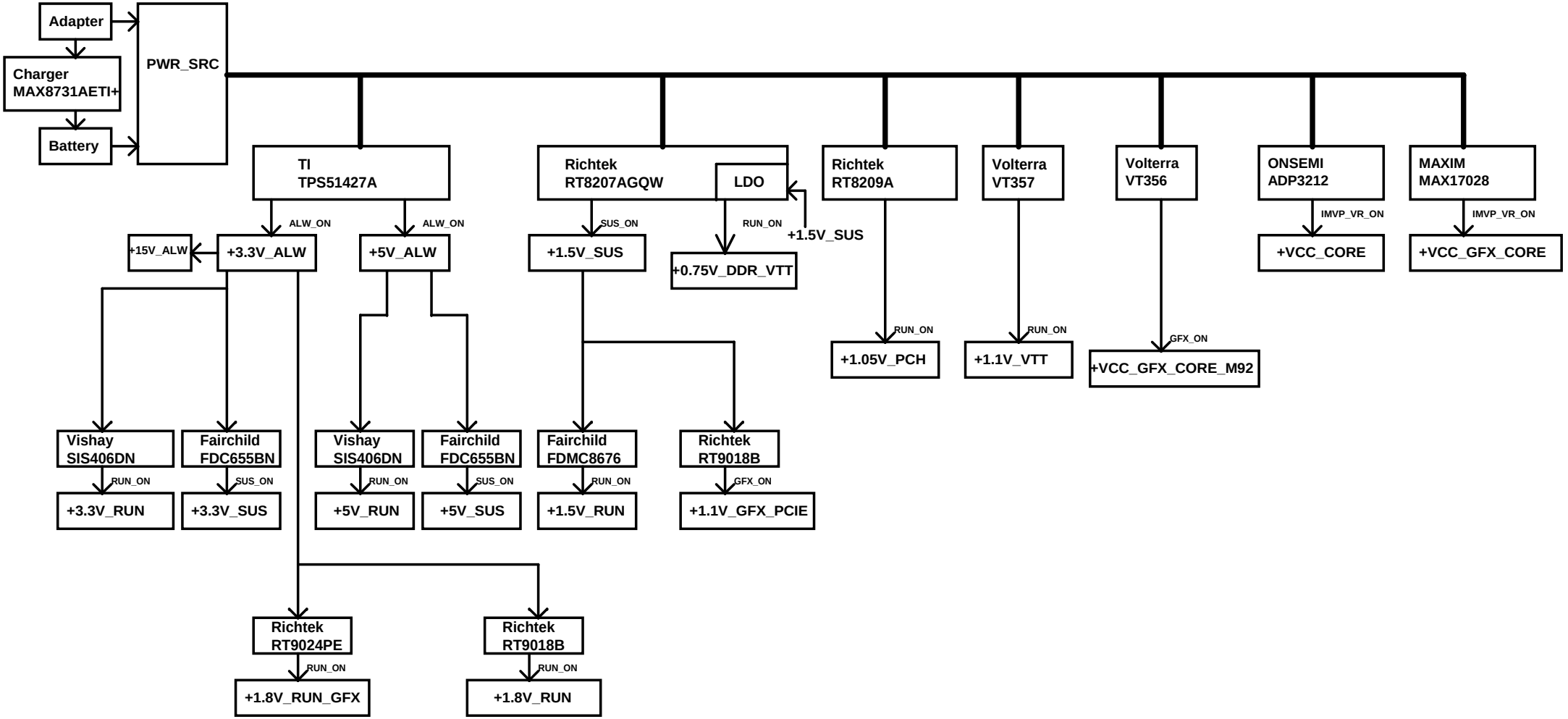
VER : 1A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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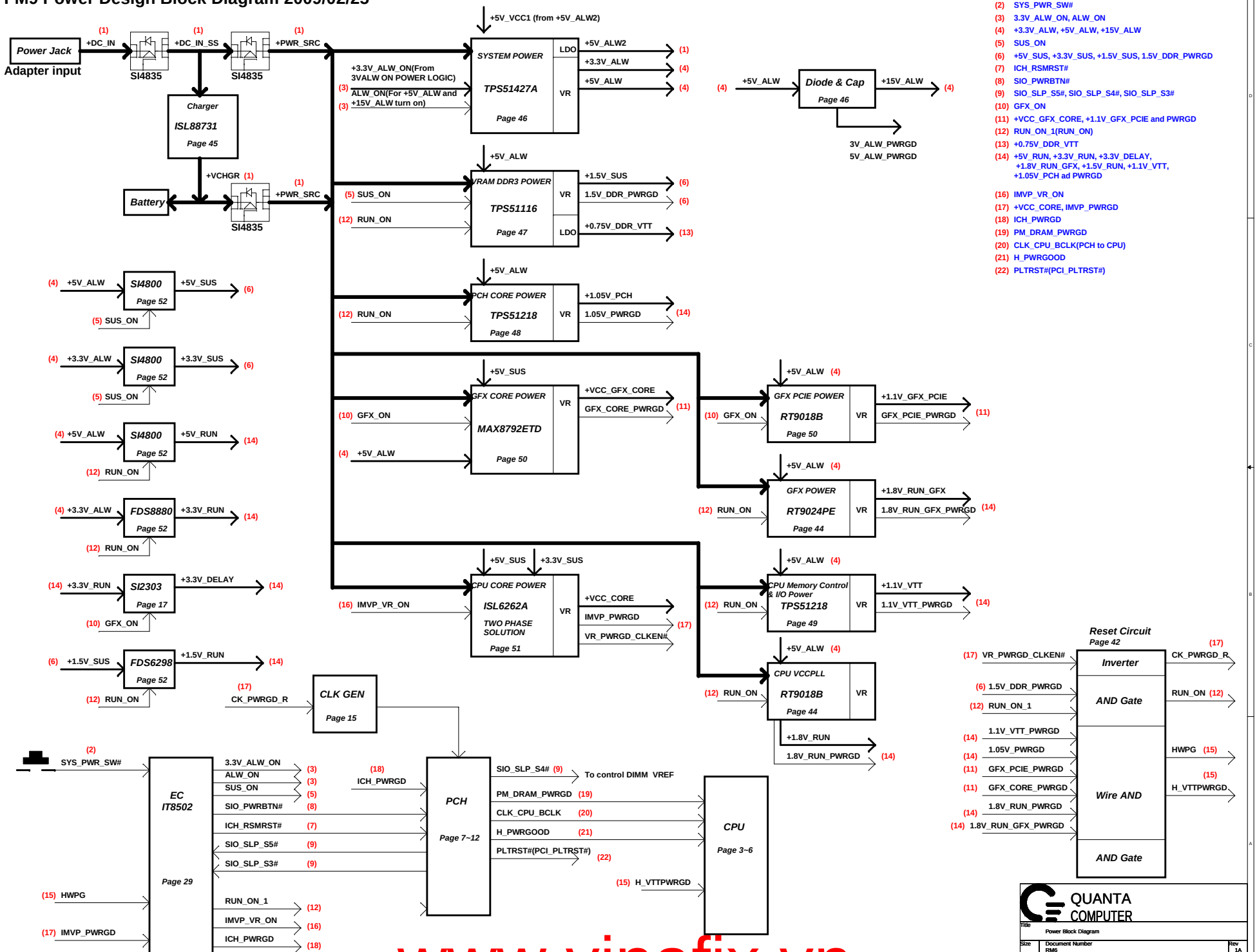
FM9 Power Design Block Diagram 2009/02/25



QUANTA COMPUTER

Title	SMBUS BLOCK	
Size	Document Number RM6	Rev 1A
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