NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

LAIKA

INTEL TIGER LAKE-UP3 14" 360 SODIMM

WLAN

MV2 BUILD
2020.08.28

Marking	Description
I	Install
NI	Non-install
PROTO	Proto type
MP	Mass Production
TAA	Install for TAA
CRITICAL	Critical Parts

EC

Phase_ID	SI	DB	PV / MV
R326	10K_short	10K_short	10K_open
R327	10K_open	10K_short	10K_short
	3V	1.5V	0V

BIOS BUILD ID

	BUILD_ID1	BUILD_ID0
DB	0	0
SI	0	1
PV	1	0
MV	1	1

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	by Andy		
APPROVAL	by Andy		
FILE NAME	MLB 17.1 - RANGERS		
PCB P/N	50.XXXXX.XXXX	PCB VER	XXX

INVENTEC

TITLE	MLB 17" - RANGERS		Main Board
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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EC_IT5571_ICE LAKE (41)
KB conn & LED (42)
40PIN EDP+CAM+TOUCH (43)
SSD_M2_2280_S3_M-Key (44)
TI_TPS659875_TBT (45)
TypeC_w/o re-timer (46)
Type-C CNTR (47)
USB3.0 conn (48)
TPM 2.0 (49)
Audio_Codec_ALC3314 (50)
WLan_M2_2230_NGFF_E-Key (51)
Card Reader (52)
TouchPad & Screw (Intel) (53)
Accelerometer-2D(MB) (54)
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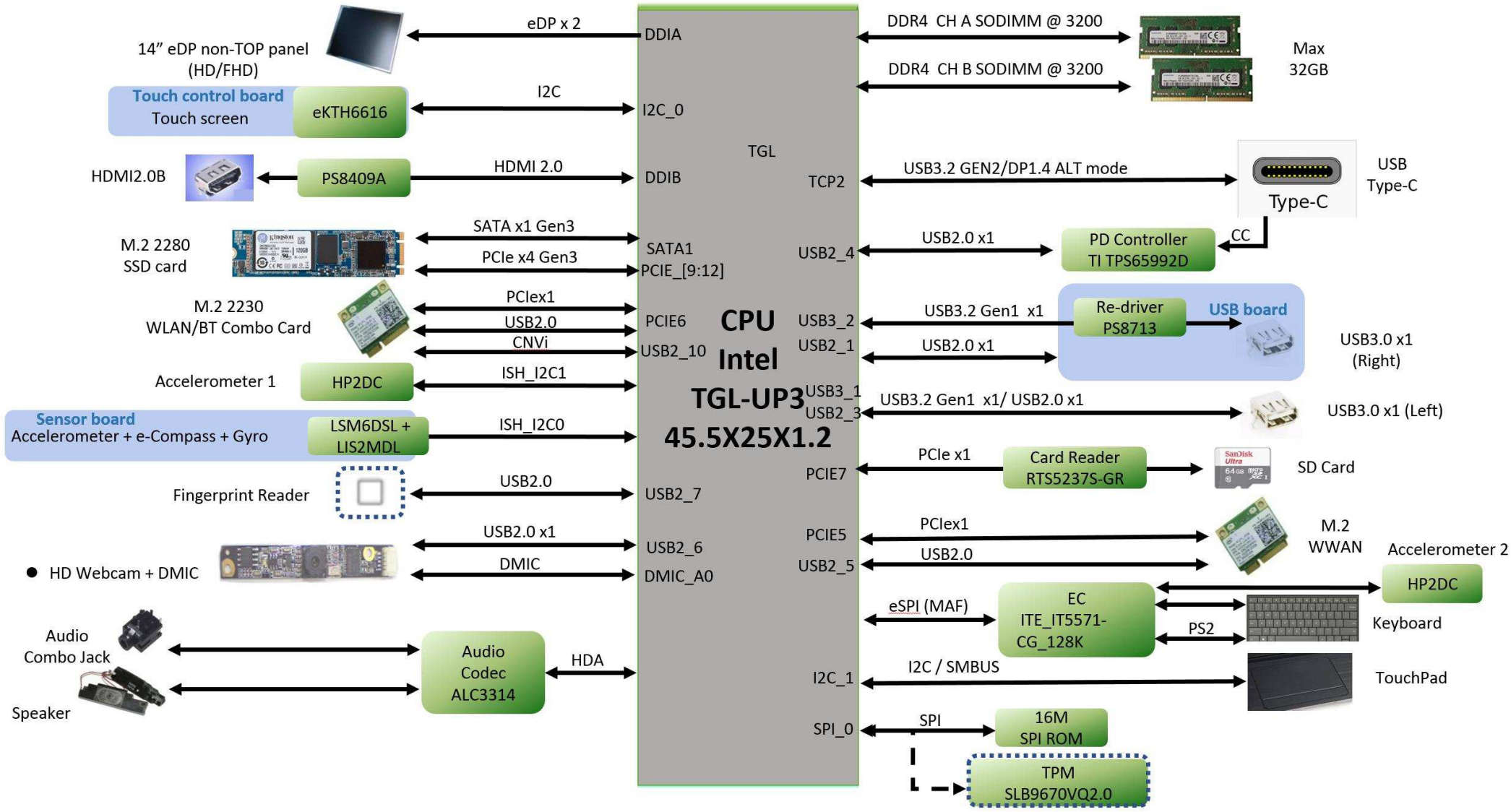
Laika 14”x360 TGL-UP3 Function Block Diagram



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TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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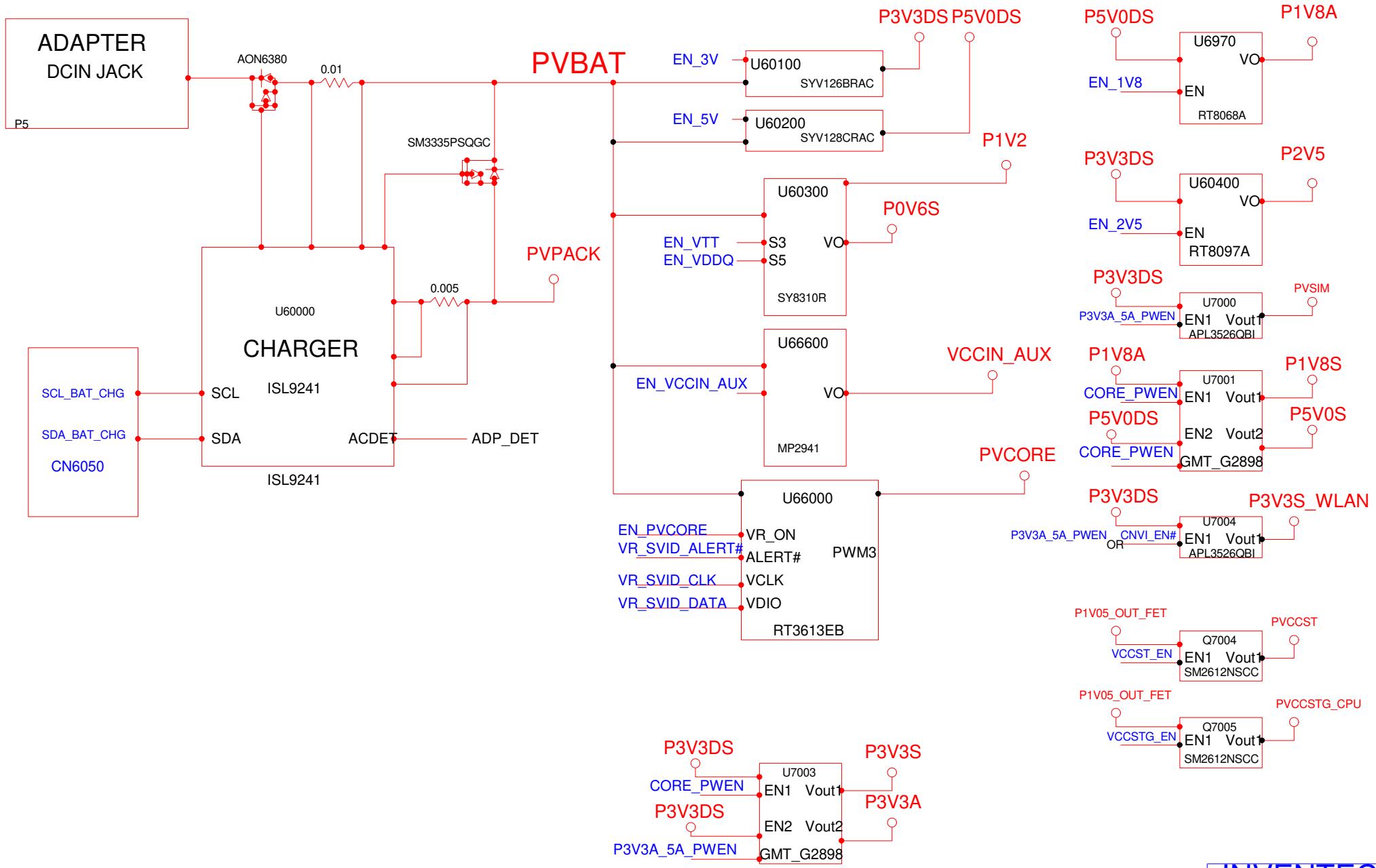

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION		
	Block Diagram		
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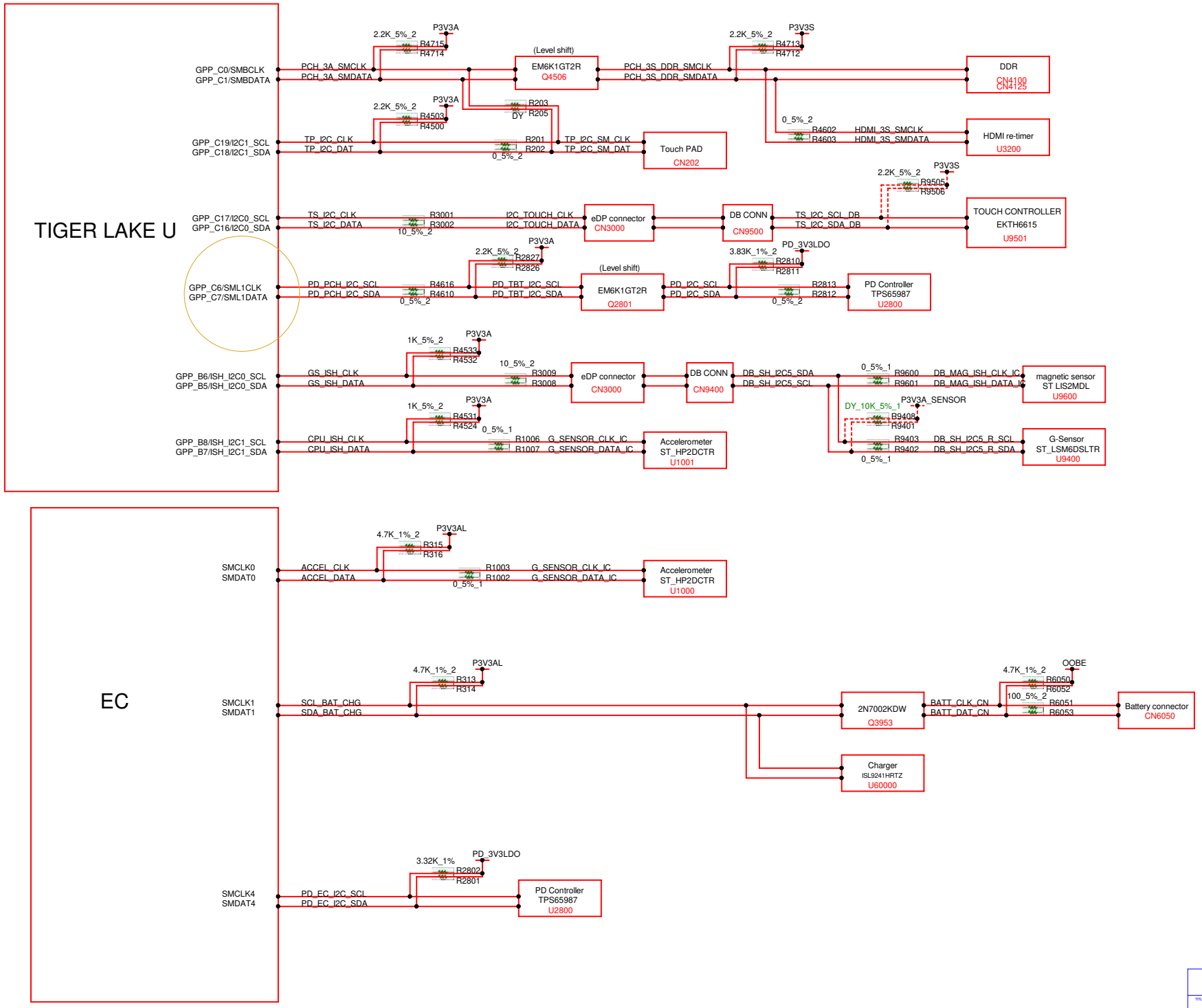

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MODEL,PROJECT,FUNCTION

KBC

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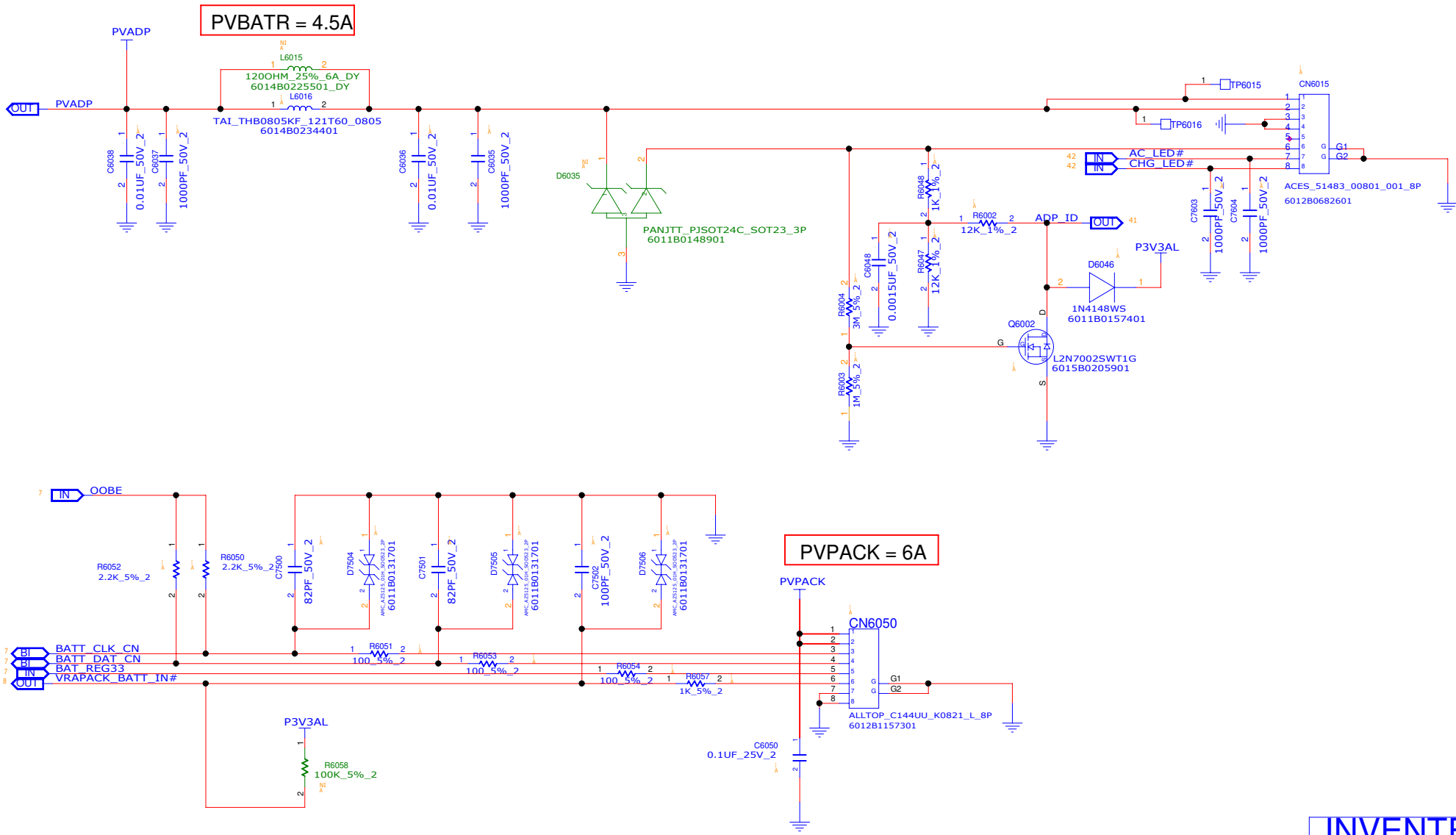
SELECTOR

VER.04_20171113



INVENTEC

TITLE: MODEL, PROJECT, FUNCTION
Block Diagram

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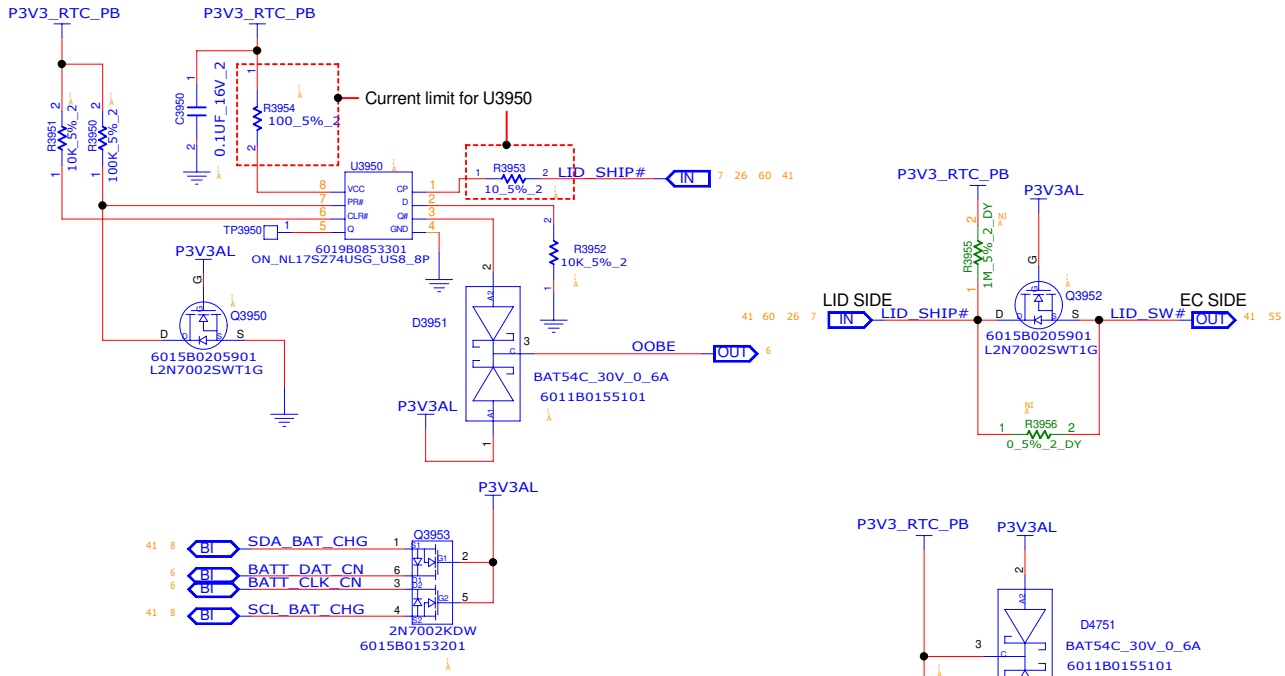
PCB P/N	60xxxxxxxxx	PCB VER	XXX

STORAGE MODE

VER.01_20170918



TRUTH TABLE

INPUT				OUTPUT		OPARATING MODE
PR#	CLR#	CP	D	Q	Q#	
L	H	X	X	H	L	ASYNCHRONOUS SET
H	L	X	X	L	H	ASYNCHRONOUS CLEAR
L	L	X	X	H	H	UNDETERNLNED
H	H	↑	H	H	L	LOAD AND READ REGISTER
H	H	↑	L	L	H	

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Storage Mode

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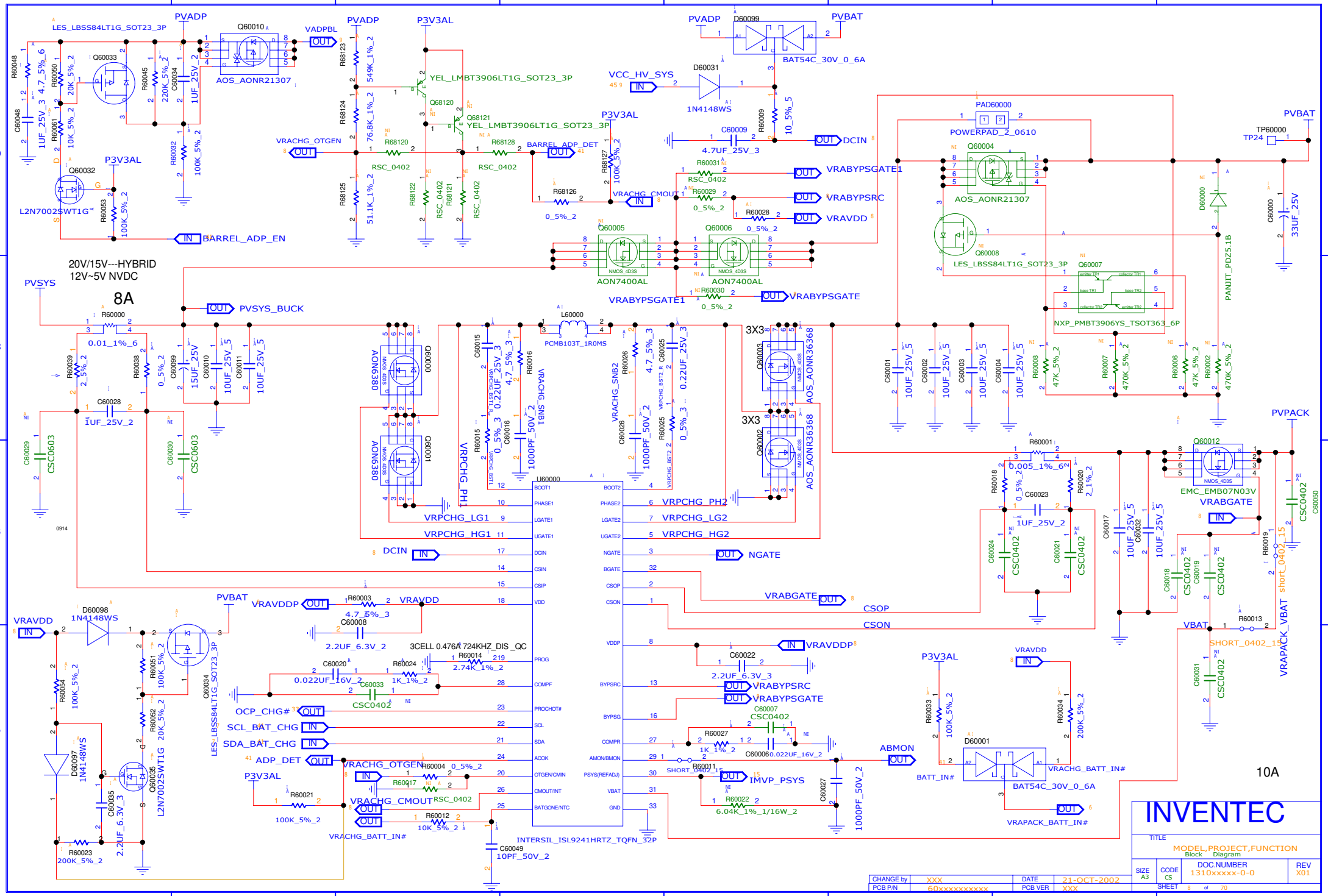
20V/15V---HYBRID
12V~5V NVDC
8A
10A
PVSYS
PVADP
PVBAT
PVPACK
P3V3AL
VADPBL
PVSYS_BUCK
BARREL_ADP_EN
BARREL_ADP_DET
VRACHG_OTGEN
VRACHG_CMOUT
DCIN
VRABYPSGATE1
VRABYPSRC
VRAVDD
VRABYPSGATE
VRABGATE
VRAVDDP
VRPCHG_PH1
VRPCHG_PH2
VRPCHG_LG1
VRPCHG_LG2
VRPCHG_HG1
VRPCHG_HG2
NGATE
CSOP
CSON
OCP_CHG#
SCL_BAT_CHG
SDA_BAT_CHG
ADP_DET
IMVP_PSYS
ABMON
VRACHG_BATT_IN#
VRAPACK_BATT_IN#
VBAT
VRAPACK_VBAT
AOS_AONR21307
AON7400AL
AOS_AONR36368
PCMB103T_1R0MS
INTERSIL_ISL9241HRTZ_TQFN_32P
3CELL 0.476A 724KHZ_DIS_QC
BAT54C_30V_0_6A
1N4148WS
POWERPAD_2_0610
NXP_PMBT3906YS_TSOT363_6P
EMC_EMB07N03V
PANJIT_PD25.1B
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21-OCT-2002
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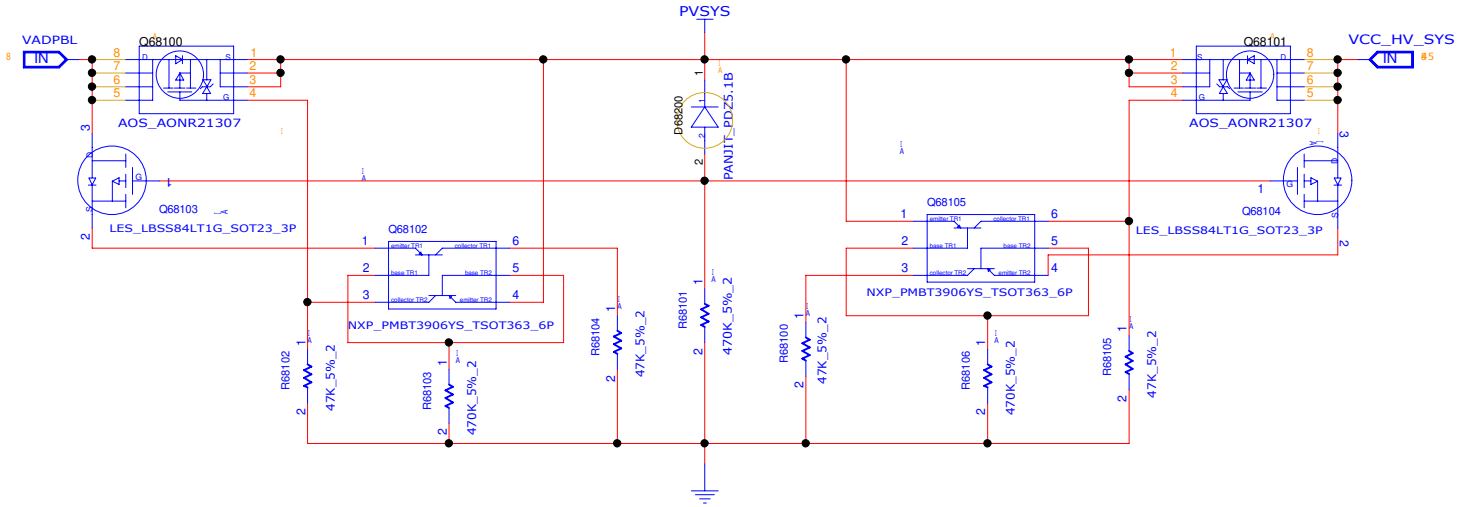
XXX



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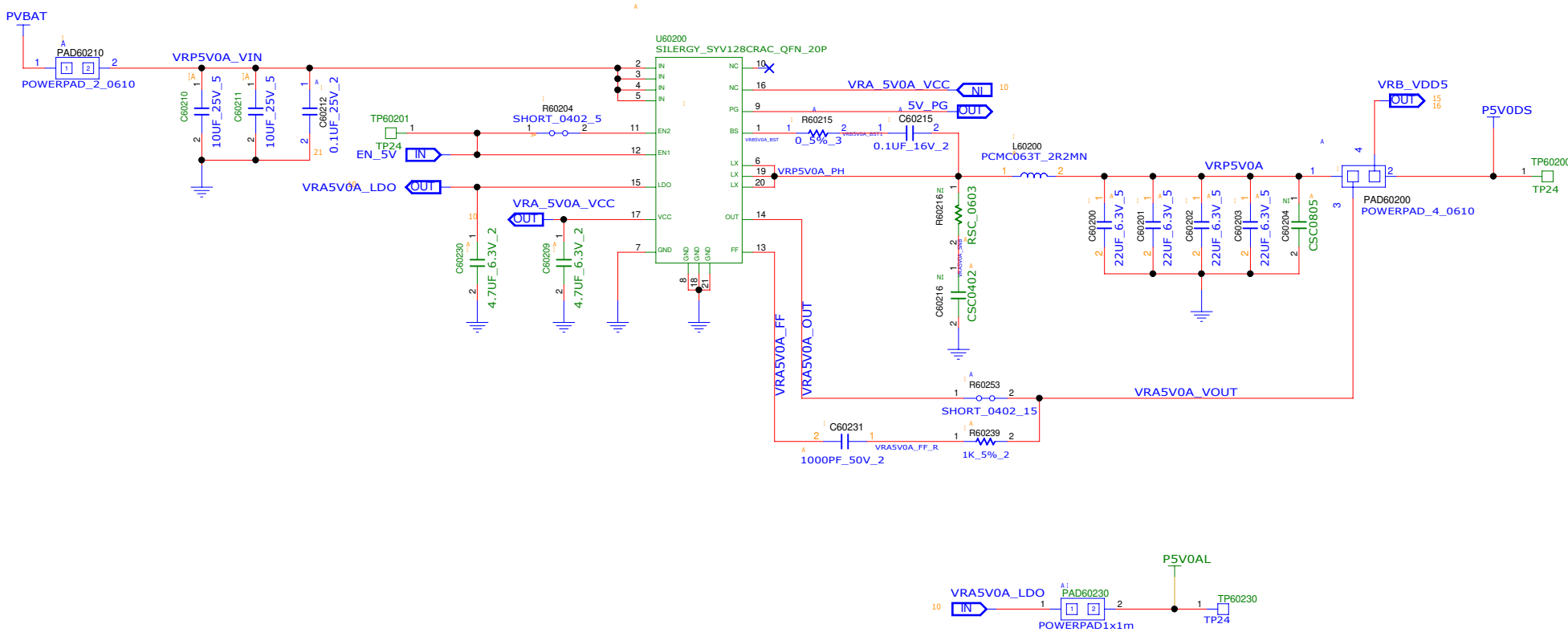

INVENTEC

TITLE
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Block Diagram

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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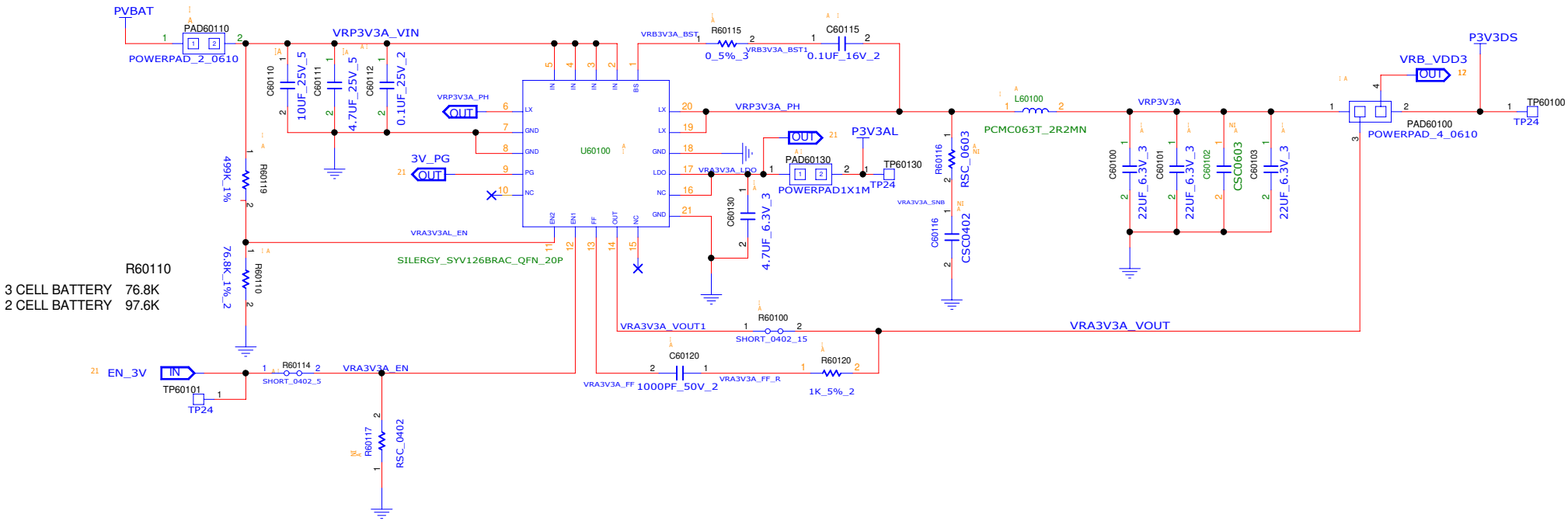

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SIZE	CODE	DOC.NUMBER	REV
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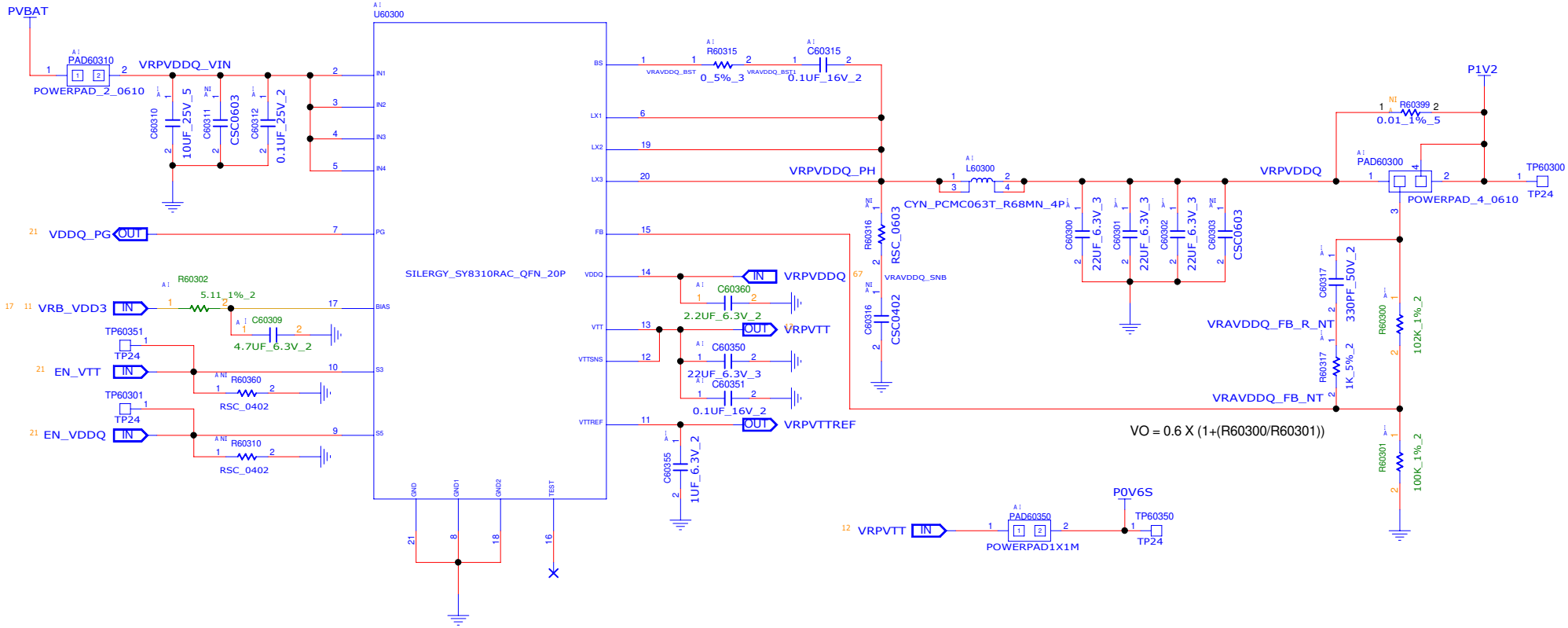

S3	S5	STATE	BUCK	VTTREF	VTT
High	High	S0	On	On	On
Low	High	S3	On	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
S5/S3 Rising Threshold	$V_{S,R}$		1			V
S5/S3 Falling Threshold	$V_{S,F}$				0.3	V
S5 Voltage for USM Mode	$V_{S5,USM}$		1		1.8	V
S5 Voltage for PFM Mode	$V_{S5,PFM}$		2.1		V_{IN}	V

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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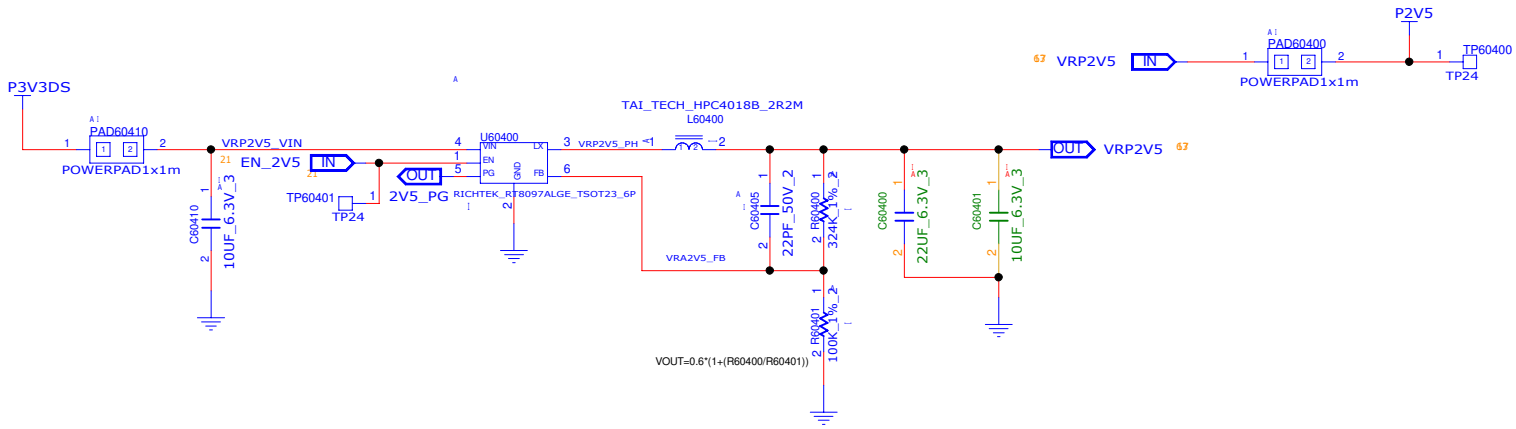

INVENTEC

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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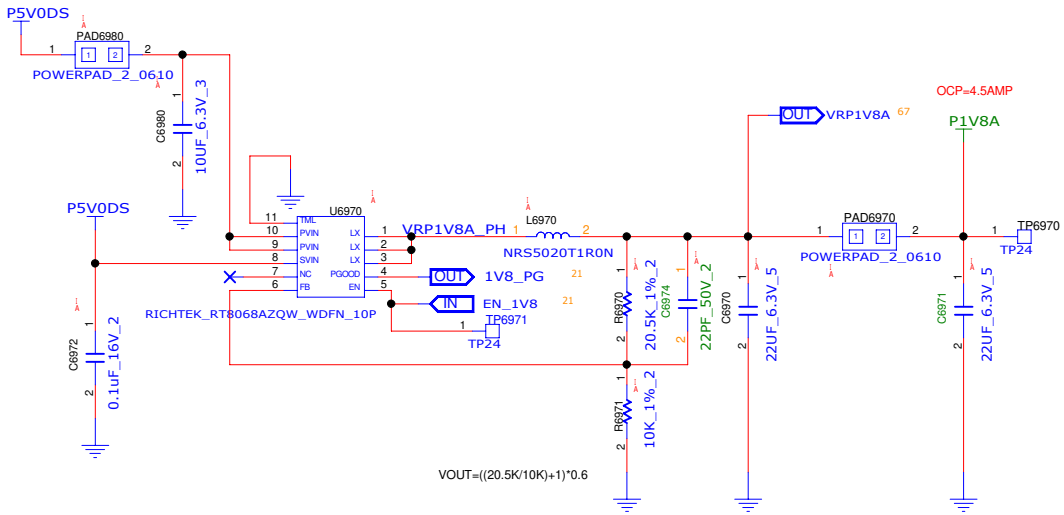

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SIZE	CODE	DOC.NUMBER	REV
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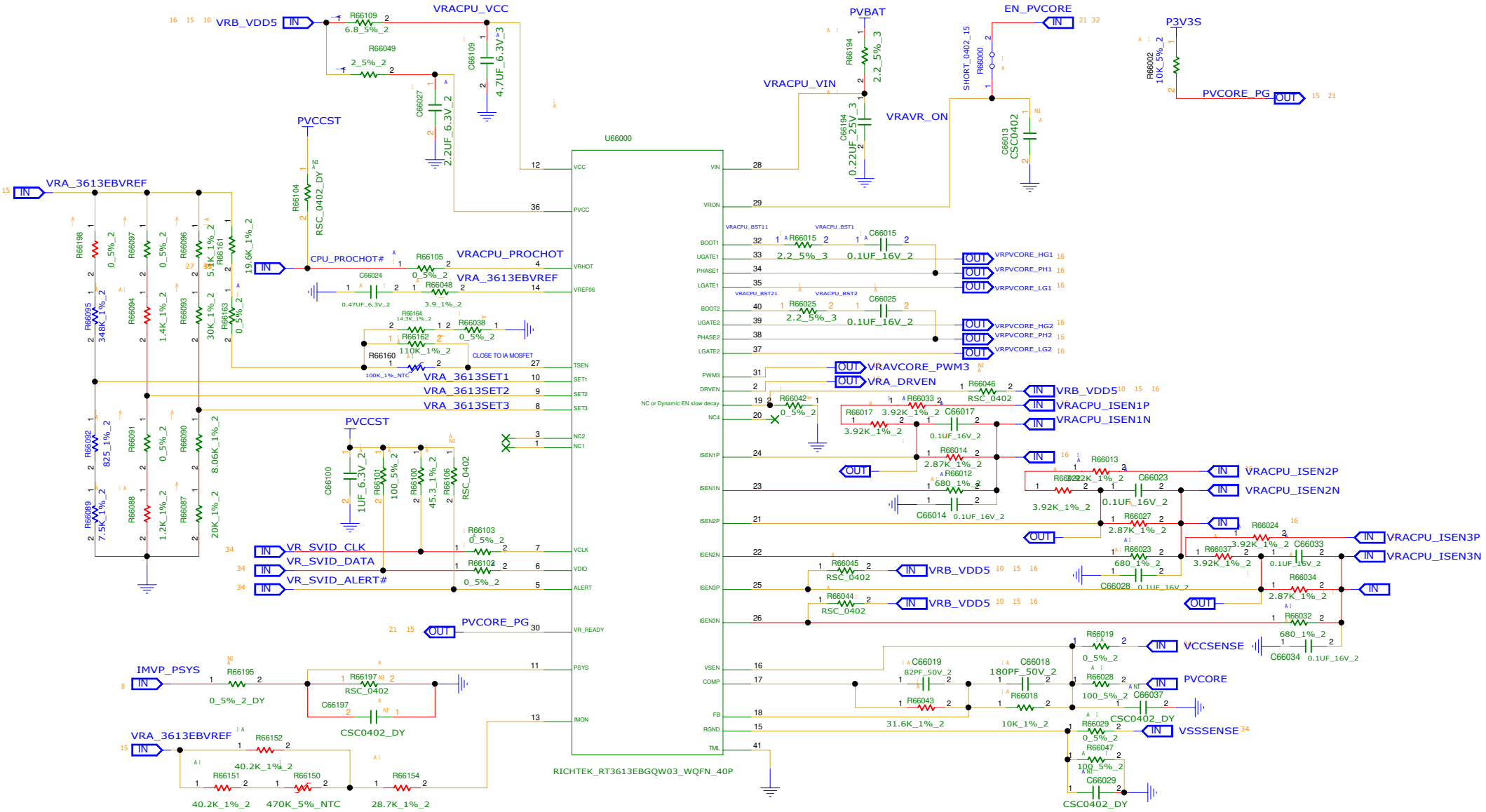

Laika	Vboot =1.8V 2 Phase	Vboot =0V 2 Phase	Vboot =1.8V 3 Phase	Vboot =0V 3 Phase
R66198	11.8k	0 ohm	0 ohm	0 ohm
R66095	80.6k	80.6k	402k	348k
R66092	2k	590 ohm	2k	825 ohm
R66089	8.45k	8.45k	7.5k	7.5k

			IA			Power limit (W)		
	Thermal sku		IccMax (A)	I_PL2 (A)	LL (mΩ)	PL1	PL2	PL4
TGL 15	U42	Baseline	47	30	2	15	51	93

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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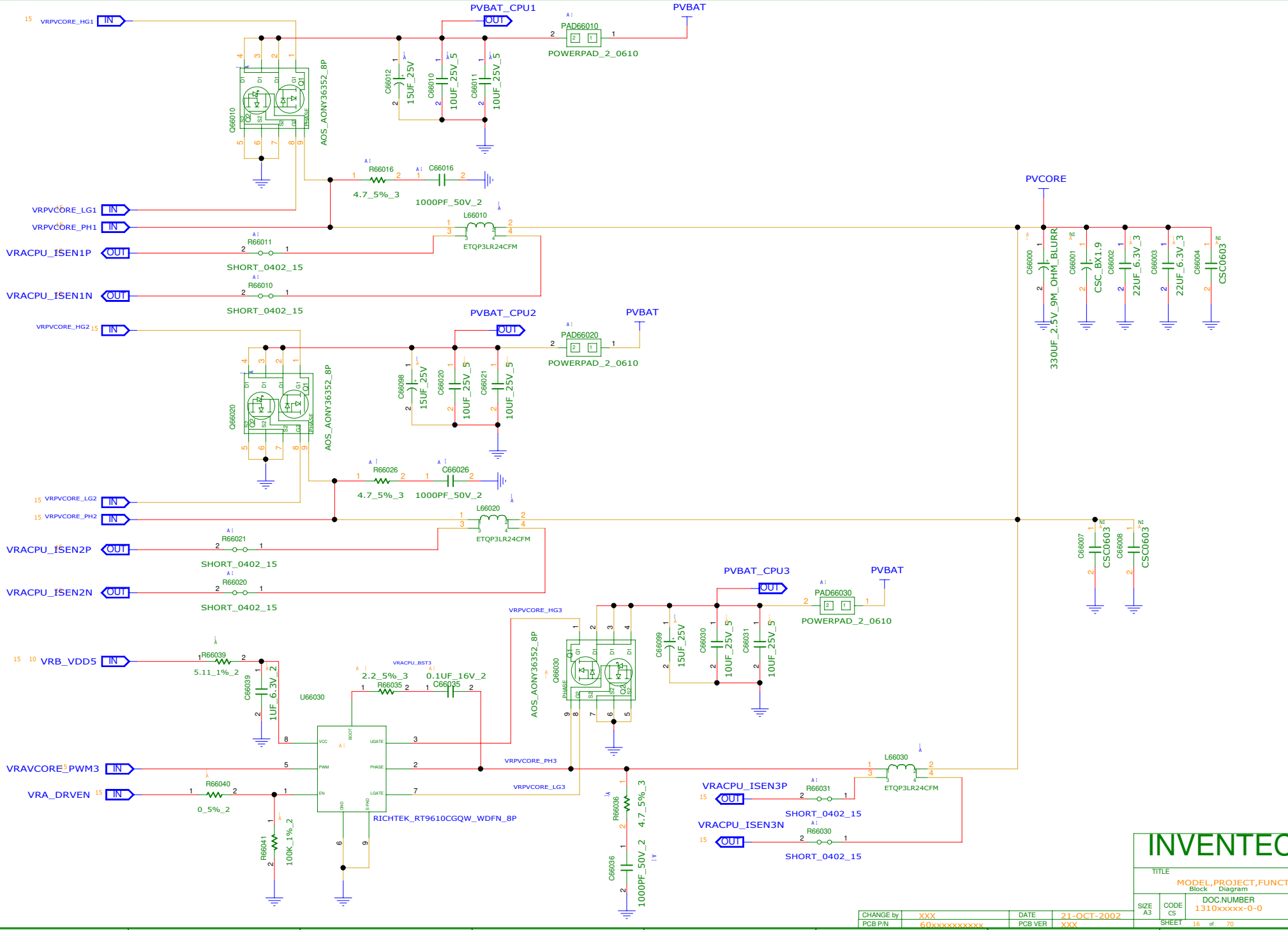
PVBAT_CPU1
PVBAT
PAD66010
POWERPAD_2_0610
VRPVCORE_HG1
VRPVCORE_LG1
VRPVCORE_PH1
VRACPU_ISEN1P
VRACPU_ISEN1N
AOS_AONY36352_8P
C66012 15UF_25V
C66010 10UF_25V_5
C66011 10UF_25V_5
R66016 4.7_5%_3
C66016 1000PF_50V_2
L66010 ETQP3LR24CFM
R66011 SHORT_0402_15
R66010 SHORT_0402_15
PVCORE
C66000 330UF_2.5V_9M_OHM_BLURR
C66001 CSC_BX1.9
C66002 22UF_6.3V_3
C66003 22UF_6.3V_3
C66004 CSC0603
PVBAT_CPU2
PAD66020
VRPVCORE_HG2
VRPVCORE_LG2
VRPVCORE_PH2
VRACPU_ISEN2P
VRACPU_ISEN2N
C66098 15UF_25V
C66020 10UF_25V_5
C66021 10UF_25V_5
R66026 4.7_5%_3
C66026 1000PF_50V_2
L66020 ETQP3LR24CFM
R66021 SHORT_0402_15
R66020 SHORT_0402_15
C66007 CSC0603
C66008 CSC0603
PVBAT_CPU3
PAD66030
VRPVCORE_HG3
VRB_VDD5
VRAVCORE_PWM3
VRA_DRVEN
VRACPU_BST3
U66030
RICHTEK_RT9610CGQW_WDFN_8P
C66039 1UF_6.3V_2
R66039 5.11_1%_2
R66035 2.2_5%_3
C66035 0.1UF_16V_2
R66040 0_5%_2
R66041 100K_1%_2
C66099 15UF_25V
C66030 10UF_25V_5
C66031 10UF_25V_5
VRPVCORE_PH3
VRPVCORE_LG3
R66036 4.7_5%_3
C66036 1000PF_50V_2
L66030 ETQP3LR24CFM
VRACPU_ISEN3P
VRACPU_ISEN3N
R66031 SHORT_0402_15
R66030 SHORT_0402_15
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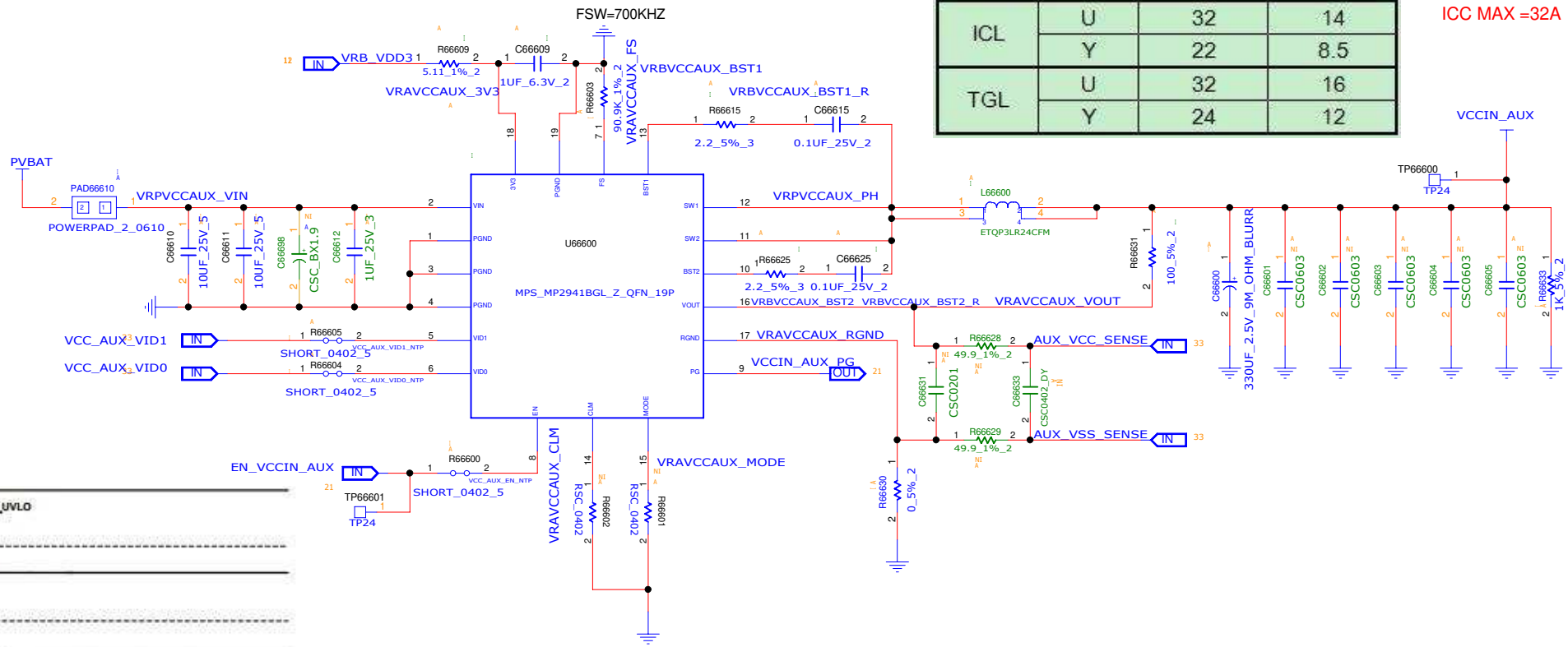
PCB VER XXX

Platfrom		IccMAX (A)	TDC (A)
ICL	U	32	14
	Y	22	8.5
TGL	U	32	16
	Y	24	12

TDC=16A
ICC MAX =32A



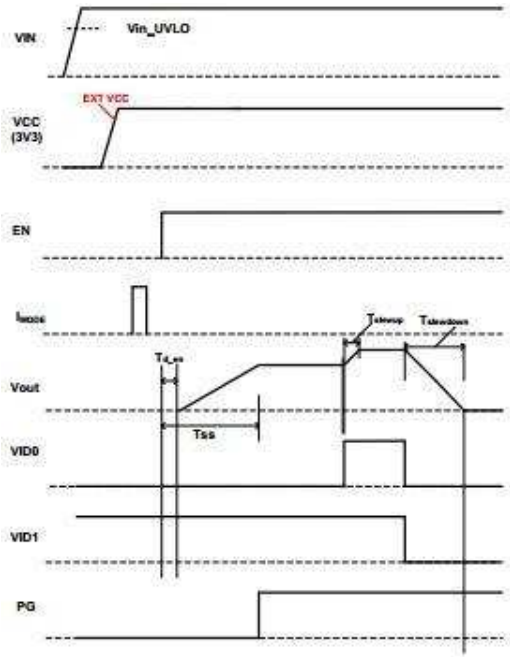


Figure 4—Start-up power sequence

Table 1—MODE Select

State	Interleaving	VID Down	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90 K
M3	Y	Decay	150 K
M4	N	Decay	>230 K or float

Table 2—FS Selection

State	Fs	Resistor to GND
M1	500kHz	0
M2	700kHz	90 K
M3	1000kHz	150 K
M4	1200kHz	>230 K or float

Table 3—VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table 4—CLM/Phase Selection

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90 K
M3	13A	150 K
M4	16A	>230 K or float

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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POWER ON SEQUENCE

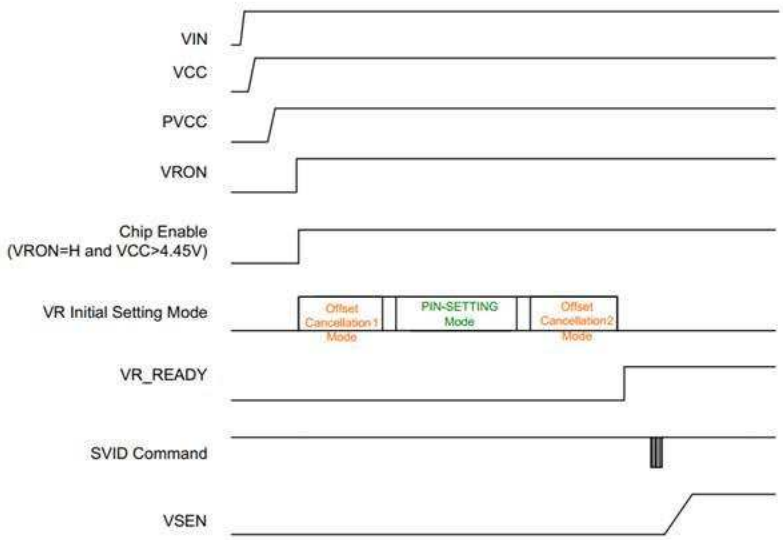

Figure 2. Typical Timing of Controller Power-On

Laika	Vboot =1.8V 2 Phase	Vboot =0V 2 Phase	Vboot =1.8V 3 Phase	Vboot =0V 3 Phase
R66198	11.8k	0 ohm	0 ohm	0 ohm
R66095	80.6k	80.6k	402k	348k
R66092	2k	590 ohm	2k	825 ohm
R66089	8.45k	8.45k	7.5k	7.5k

BTO Table

TGL	L=0.24H, DCR=1.19mohm, LL=2mohm, Iccmax=47A, F=450KHz	
	2phase	3phase
R66198	11.8k_1%_2	0_5%_2 (60130B0000ZT)
R66095	80.6k_1%_2	402k (6013A0084801)
R66089	8.45k_1%_2	7.5k_1%_2 (6013A0085901)
R66036	NI	4.7_5%_3
C66036	NI	1000pF_50V_2
R66035	NI	2.2_5%_3
R66039	NI	5.1_5%_2
R66040	NI	0_5%_2
R66041	NI	100K_1%_2
C66035	NI	0.1UF_16V_2
C66039	NI	1UF_6.3V_2
C66030	NI	10UF_25V_5
C66031	NI	10UF_25V_5
R66030	NI	SHORT_0402_15
R66031	NI	SHORT_0402_15
U66030	NI	RICHTEK_RT9610CGQWP
Q66030	NI	AOS_AONY36352
L66030	NI	ETQP3LR24CFM
PAD66030	NI	I
R66024	NI	3.92K_1%_2_(6013A0019001)
R66032	NI	680_1%_2
R66034	NI	2.87K_1%_2
R66037	NI	3.92K_1%_2_(6013A0019001)
C66033	NI	0.1UF_16V_2
C66034	NI	0.1UF_16V_2
R66044	10K_5%_2_(60130B1030ZT)	NI
R66045	10K_5%_2_(60130B1030ZT)	NI
C66099	NI	15UF_25V_(6010B0185101)

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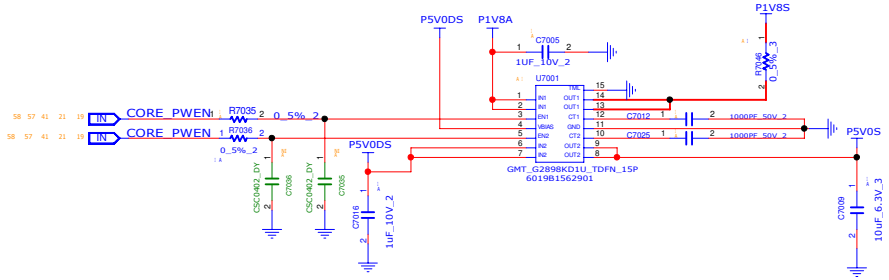
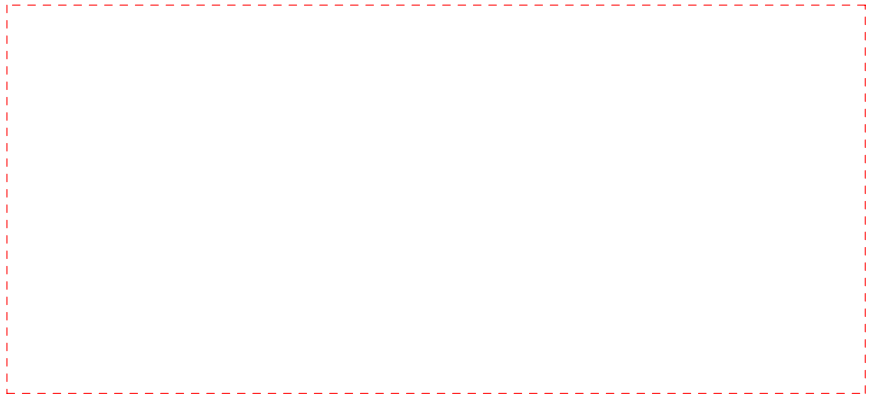
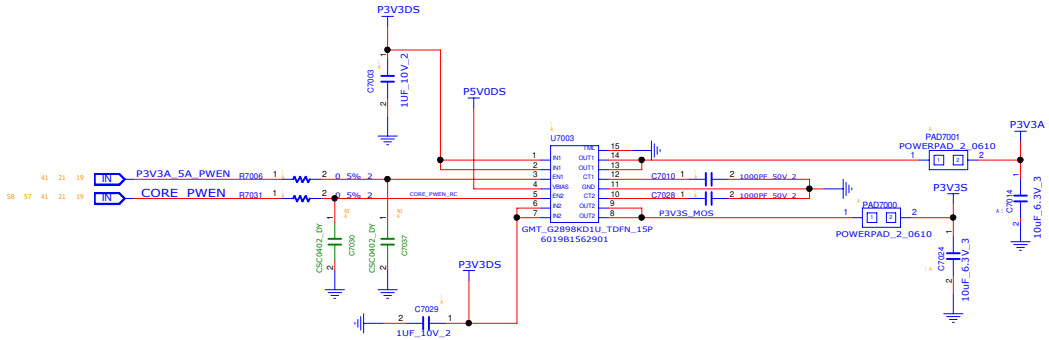
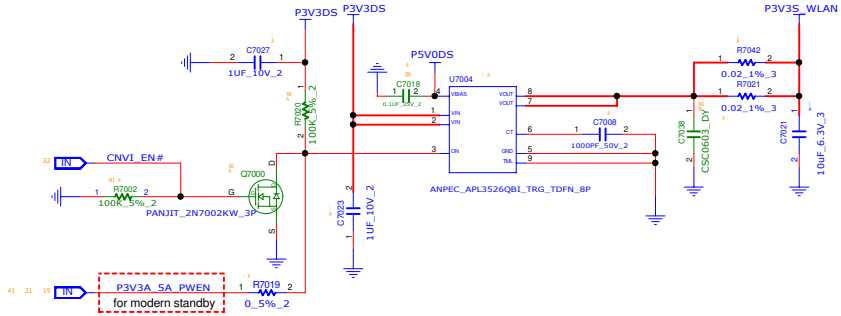








CHANGE NO	XXX	DATE	
PCB P/N	50.xxxxx.xxxx	PCB VER	1

INVENTEC

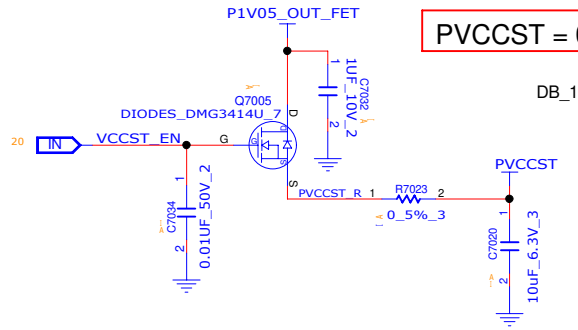
TITLE: MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxxx-0-0	X01

SHEET 19 of 70

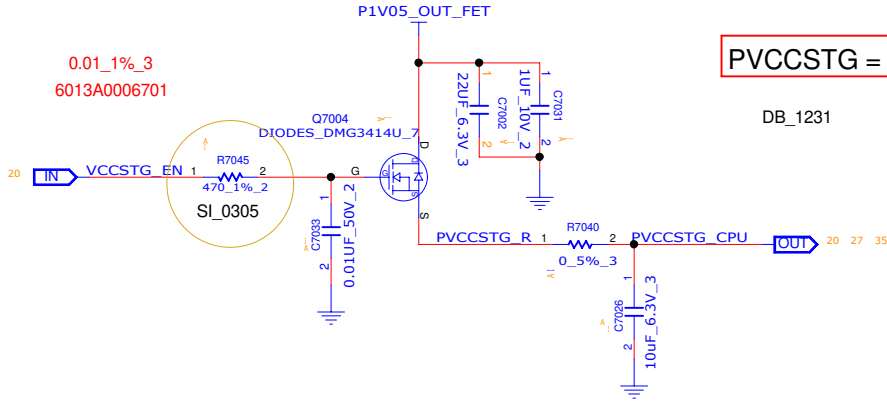
PVCCST = 0.06A

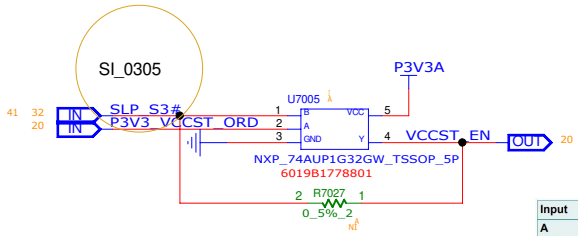
DB_1231



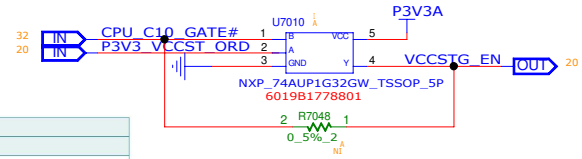
PVCCSTG = 0.02A

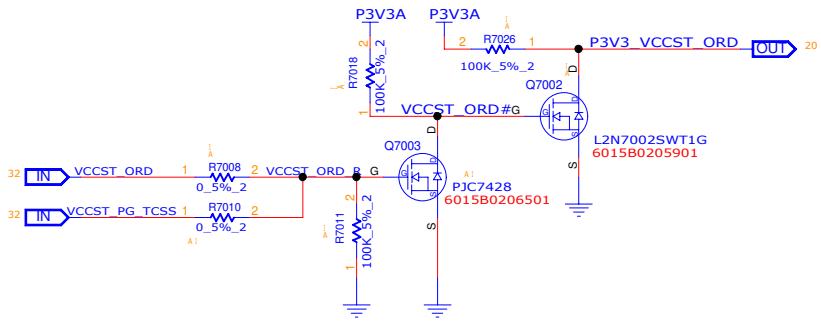
DB_1231





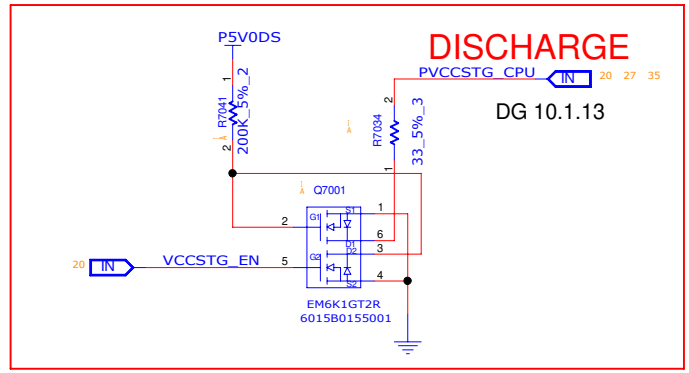
Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H





DISCHARGE

DG 10.1.13



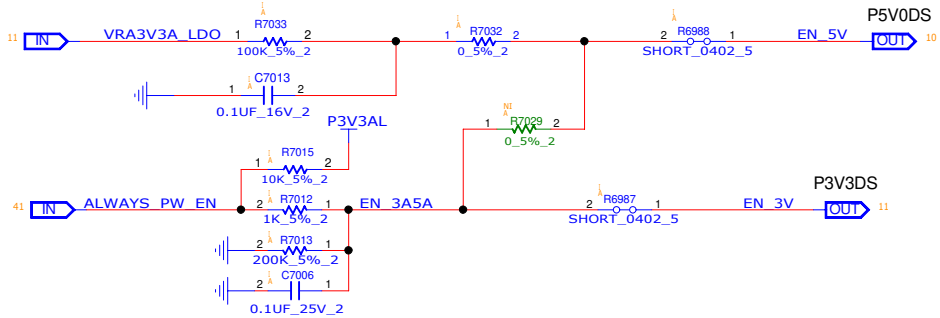
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

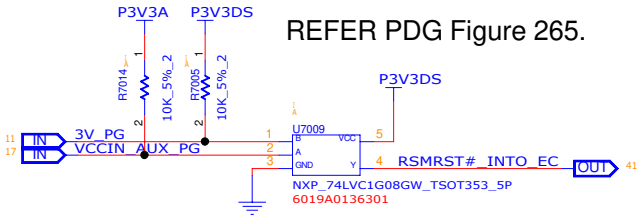
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

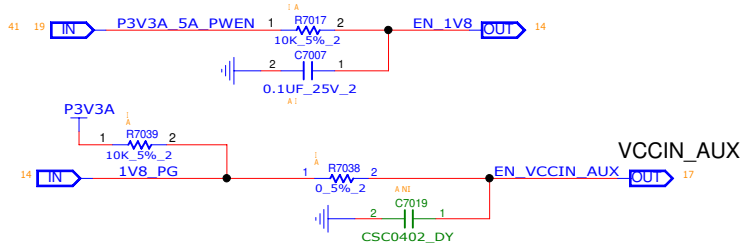
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

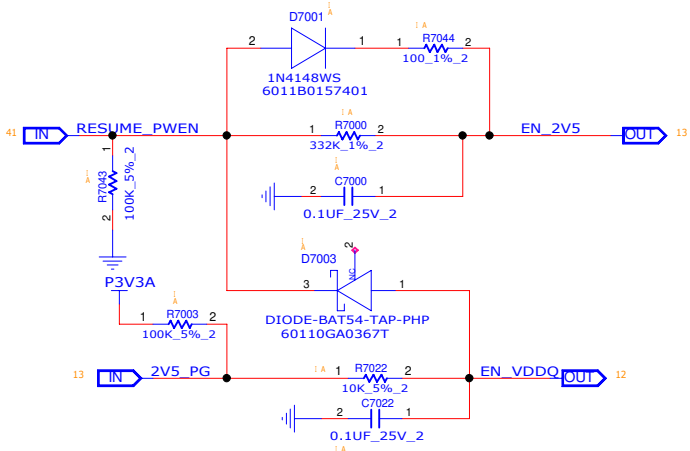
SHEET 20 of 70

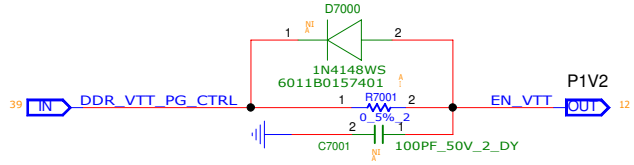


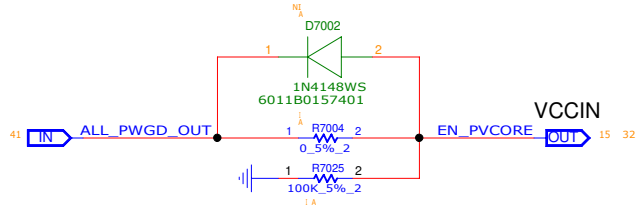
REFER PDG Figure 265.

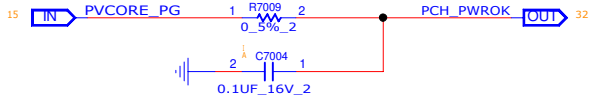


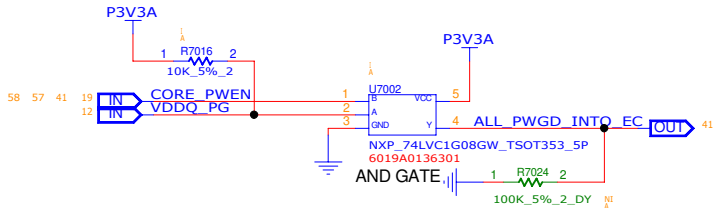








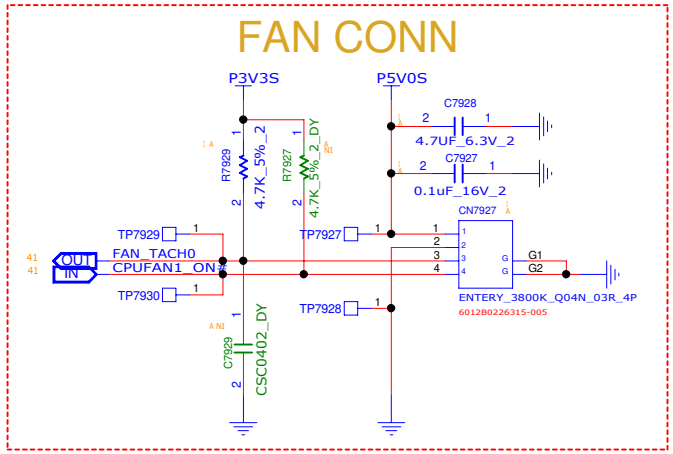




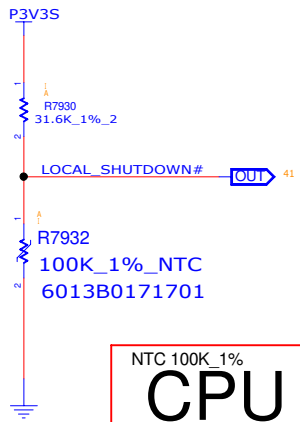
FAN & THERMAL

FOR BIG CORE USE

VER.04_20171011

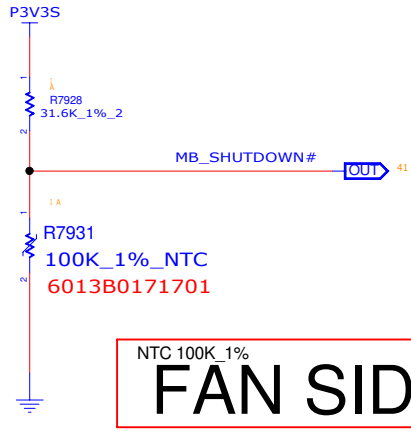


THERMAL



NTC 100K_1%

CPU SIDE



NTC 100K_1%

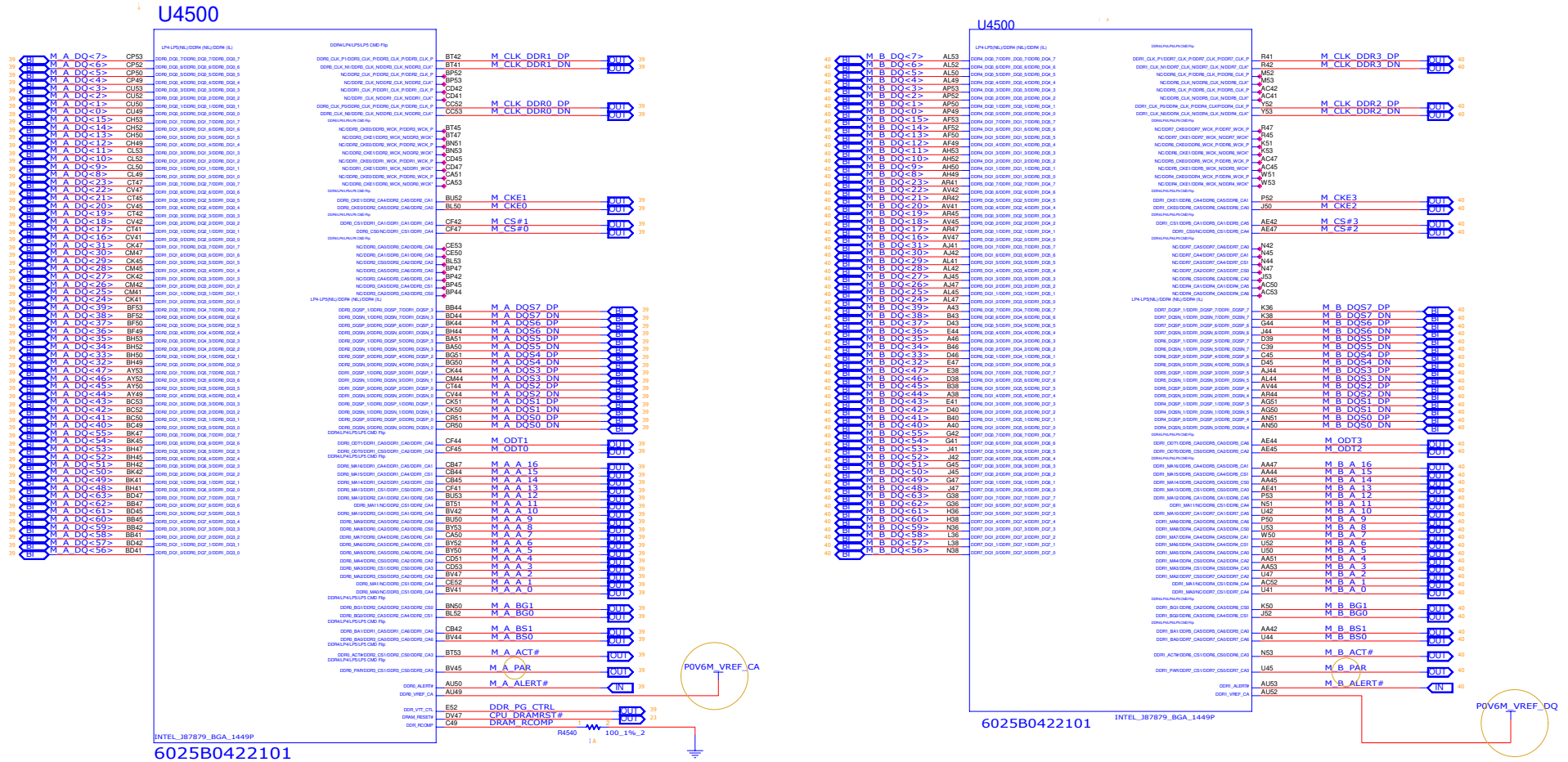
FAN SIDE

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION THERMAL & FAN		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 22 of 70			

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

MCP-MEMORY



REFERENCE:4500~4949

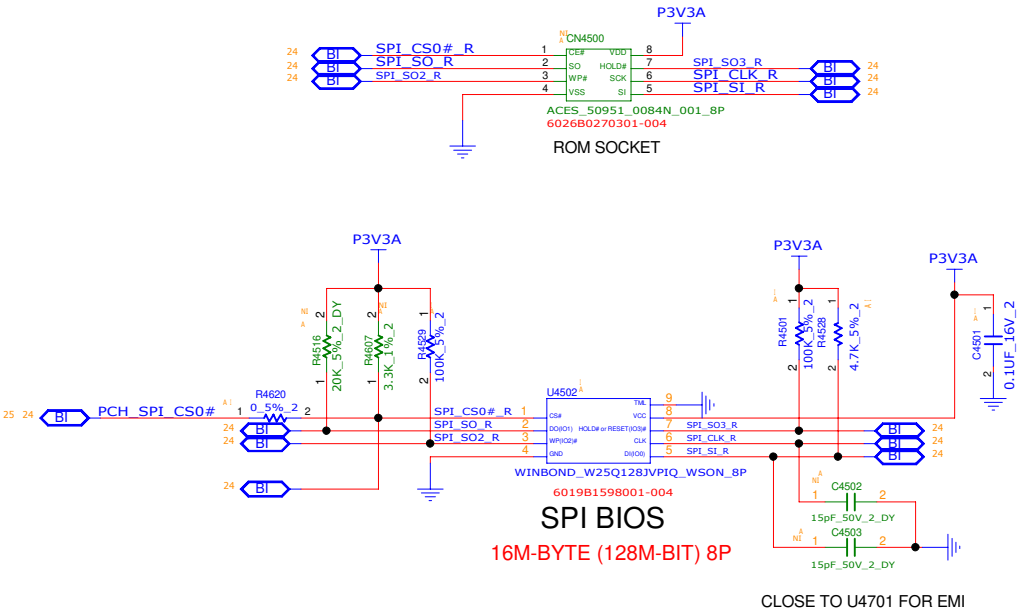
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION DDR3_SO-DIMM0		
SIZE: C	CODE: CS	DOC NUMBER: 1310xxxxx-0-0	REV: X01
	SHEET:	of 23	70

CHANGE N	XXX	DATE	
PCB P/N	60xxxxxxxxx	PCB VER	2

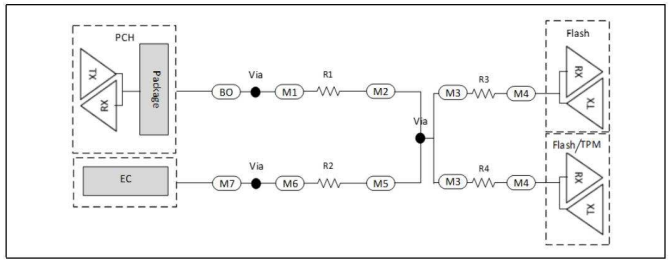
CORE - SPI ROM

SPI FLASH & SOCKET CO-LAYOUT



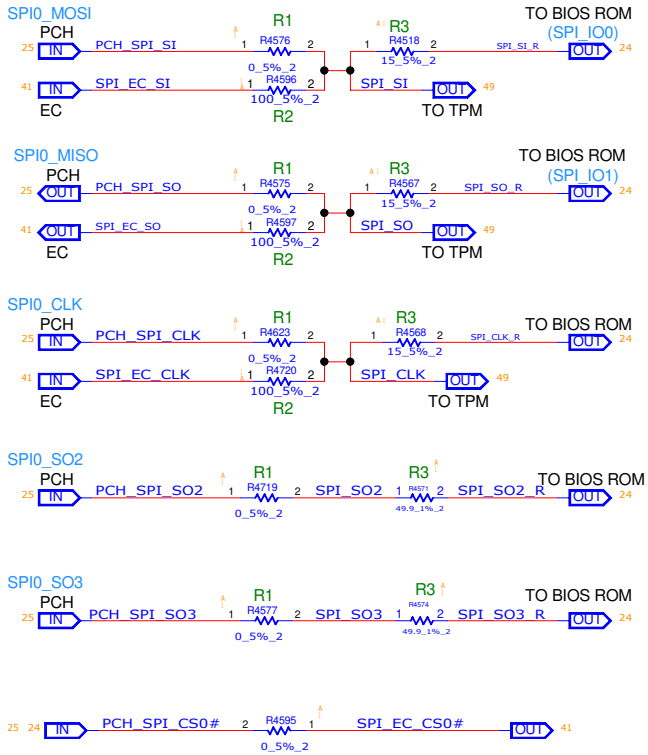
PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
S SOIC-8 208-mil	128M-bit	W25Q128JVSIQ	25Q128JVSQ
F SOIC-16 300-mil	128M-bit	W25Q128JVFIQ	25Q128JVFQ
P WSON-8 6x5-mm	128M-bit	W25Q128JVPIQ	25Q128JVPQ
E WSON-8 8x6-mm	128M-bit	W25Q128JVEIQ	25Q128JVEQ
B(1) TFBGA-24 8x6-mm (5x5 Ball Array)	128M-bit	W25Q128JVBIQ	25Q128JVBQ
C(1) TFBGA-24 8x6-mm (6x4 Ball Array)	128M-bit	W25Q128JVCIQ	25Q128JVCQ

Figure 6-84. SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology



INTEL#607872 SCHCHK

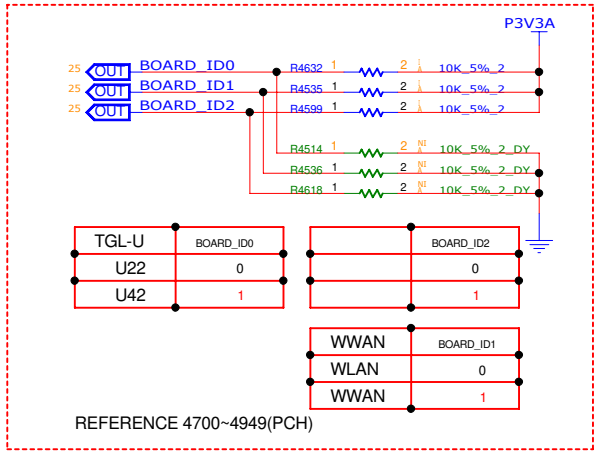
SPI0 2 LOAD TOPOLOGY WITH EC WIRED-OR FLASH SHARING(1 FLASH AND 1 TPM):

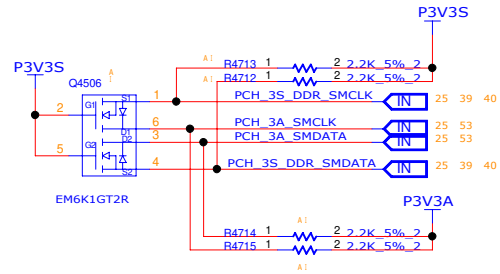


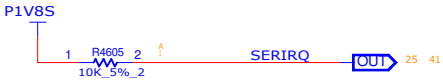
INVENTEC

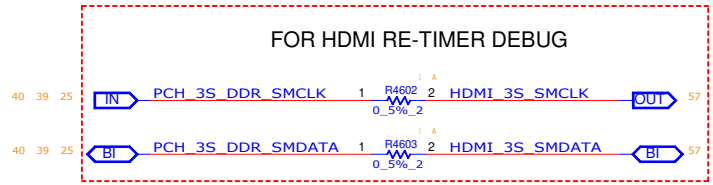
TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 24 of 70
PCB P/N 60xxxxxxxxx		PCB VER XXX	

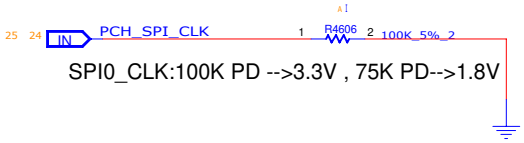
MCP-GPIO1/LPC/SPI

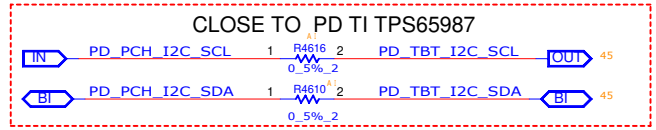


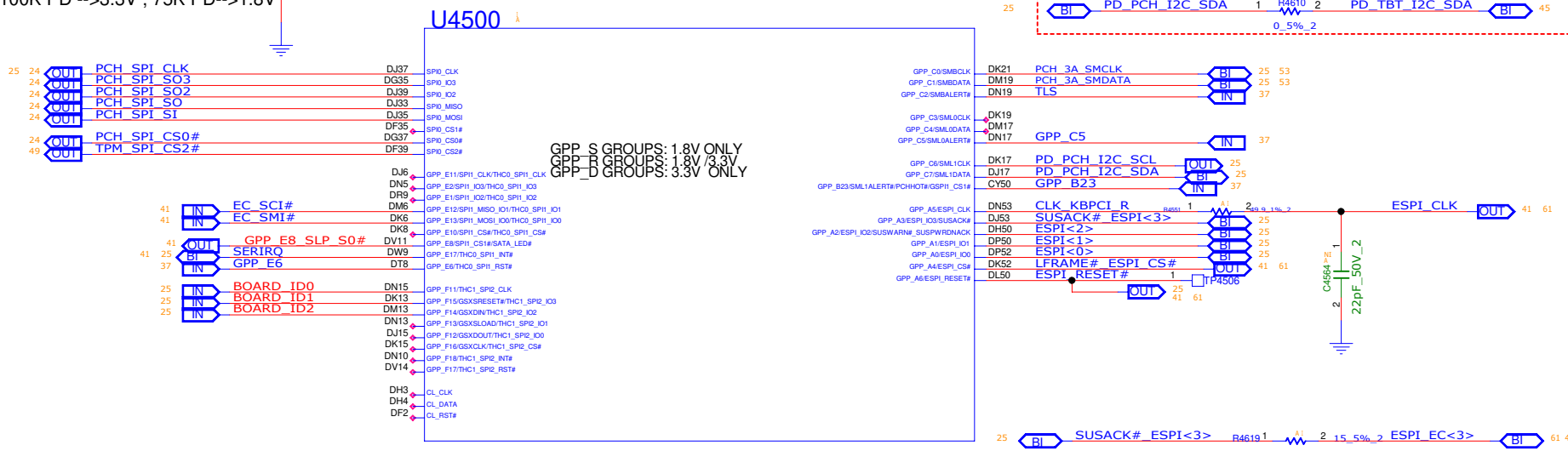


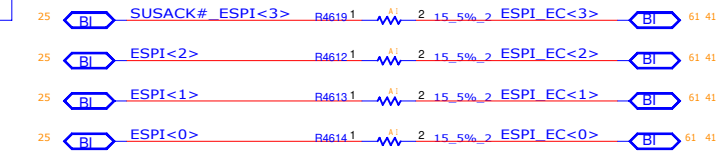


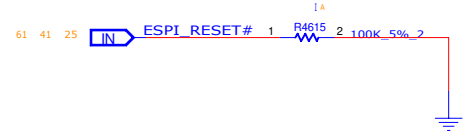










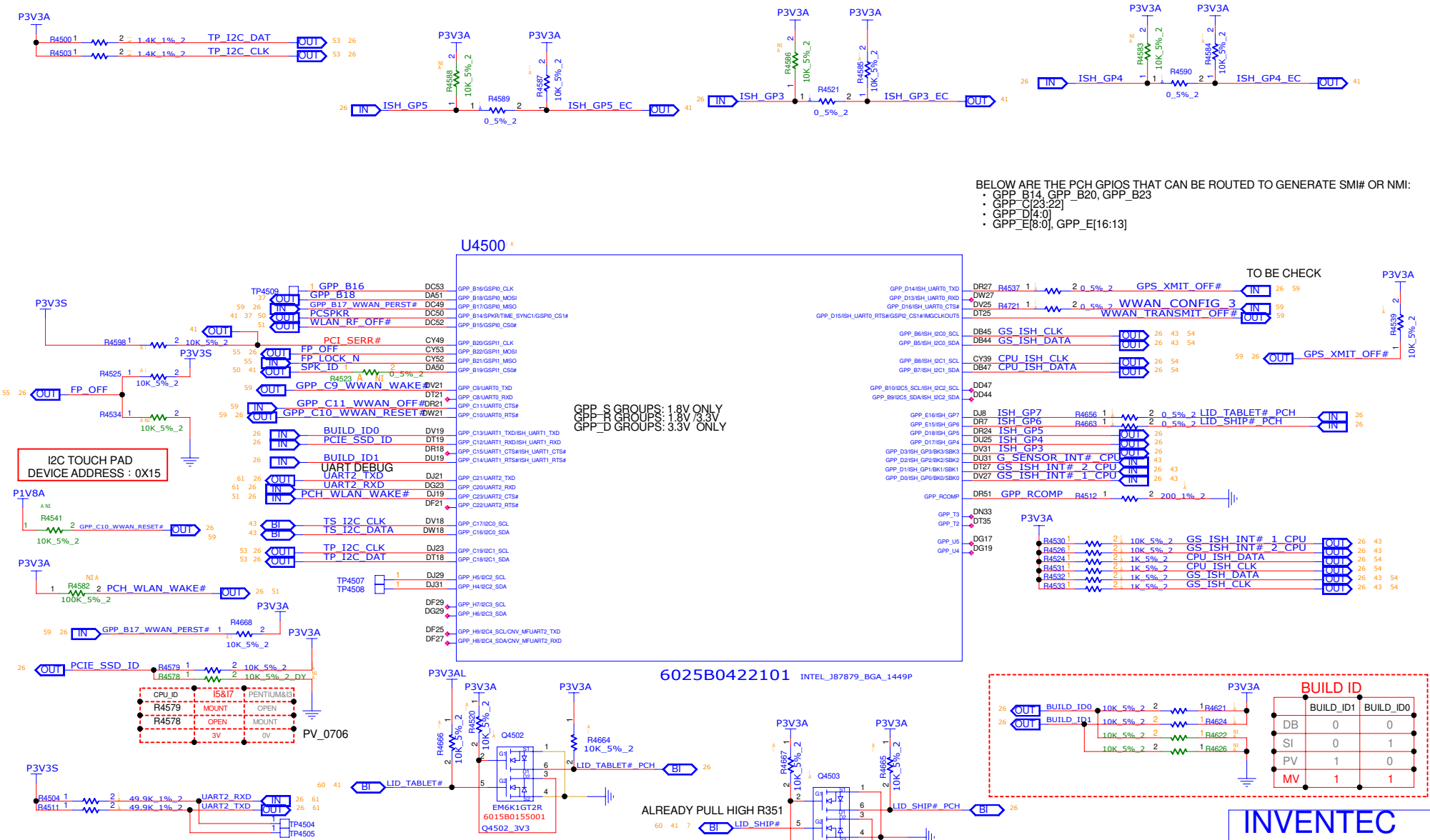


REFERENCE:4500~4949

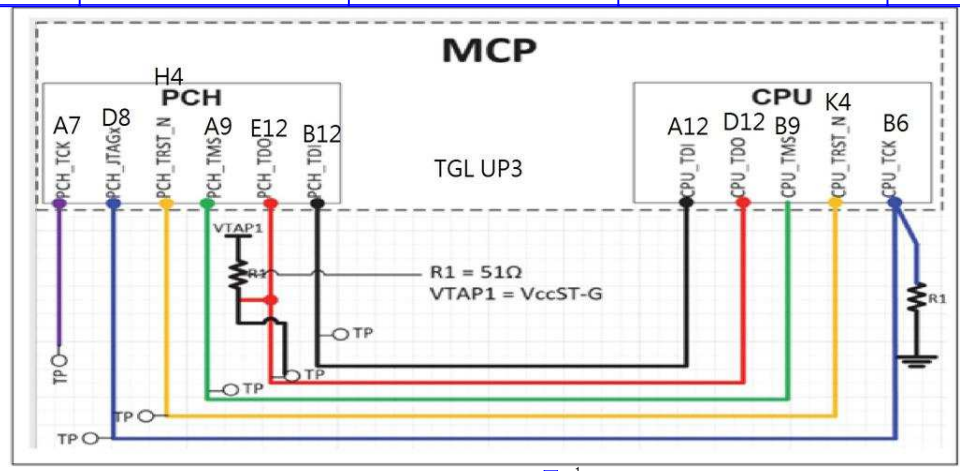
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 25 of 70			
CHANGE by <ENG>		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER <VER>	

MCP-GPIO2/I2C/UART



MCP-MISC/HDA/JTAG



PVCCST

R4604 1K_5%_2 CATERR# OUT 27

R4569 1K_5%_2 CPU_THERMTRIP# OUT 27

PVCCSTG

R4517 1K_5%_2

R4515 499_1%_2

C4514 47PF_50V_2

41 33 15 IN CPU_PROCHOT#

P3V3A

1008

R4718 10K_5%_2 TOUCHPAD_I2C_INT# OUT 27 41 53

U4500

27 OUT	CATERR#	M7	CATERR#
41 OUT	H_PECI	BK9	PECI
	CPU_PROCHOT#_R	E2	PROCHOT#
27 OUT	CPU_THERMTRIP#	M5	THRMTRIP#
R4600 49.9_1%_2	PROC_RCOMP	CT39	PROC_POPIRCOMP
R4601 49.9_1%_2	PCH_RCOMP	CB9	PCH_OPIRCOMP
		CW12	TP_1
		CM39	TP_2
37 IN	DBG_PMODE	DF4	DBG_PMODE
53 41 27 IN	TOUCHPAD_I2C_INT#	DB42	GPP_B4/CPU_GP3
43 IN	TS_INT#	DB41	GPP_B3/CPU_GP2
43 IN	TS_RST#	DF8	GPP_E7/CPU_GP1
TP4510	GPP_E3	DU5	GPP_E3/CPU_GP0
37 IN	GPP_H2	DF31	GPP_H2
37 IN	GPP_H1	DV32	GPP_H1
37 IN	GPP_H0	DW32	GPP_H0
		DJ27	GPP_H19/TIME_SYNC0

PROC_TRST#	K4	H_TRST#	OUT 27
PROC_TMS	B9	H_TMS	IN 27
PROC_TDO	D12	H_TDO	IN 27
PROC_TDI	A12	H_TDI	IN 27
PROC_TCK	B6	H_TCK	IN 27
PCH_JTAGX	D8		
PCH_TMS	A9	H_TMS	OUT 27
PCH_TDO	E12	H_TDO	IN 27
PCH_TDI	B12	H_TDI	IN 27
PCH_TCK	A7	PCH_TCK	TP4516
PCH_TRST#	H4	H_TRST#	IN 27
PROC_PREQ#	C11		
PROC_PRDY#	D11		
EAR_N_TEST_NCTF	G1	CPU_EAR	
GPP_F7	DT15	GPP_F7	IN 37
GPP_F9	DR15		
GPP_F10	DT14	GPP_F10	IN 37

TP4517 TP4518 TP4519 TP4520

PVCCSTG_CPU IN 20 35

R4717 1K_5%_2

INTEL_J87879_BGA_1449P

6025B0422101

PLACE NEAR CPU

27 IN H_TDO R4716 51_5%_2

PLACE NEAR CPU

27 IN H_TCK R4509 51_5%_2

PVCCSTG

NI R4543 100K_5%_2 IN HDA_BITCLK_PCH

U4500

DW15	GPP_F8/I2S_MCLK2_INOUT	DR38	HDA_BITCLK_PCH R4634 33_5%_2 HDA_BITCLK BI 50
DW24	GPP_D19/I2S_MCLK1	DU37	HDA_SYNC_PCH R4635 33_5%_2 HDA_SYNC BI 50
DG41	GPP_A23/I2S1_SCLK	DT37	HDA_SDO_PCH R4636 33_5%_2 HDA_SDO_R OUT 38
DT38	GPP_R7/I2S1_SFRM	DV37	HDA_SDIN0_PCH R4630 33_5%_2 HDA_SDIN0 IN 50
DV38	GPP_R6/I2S1_TXD	DV41	HDA_RST# TP4521
DW38	GPP_R5/HDA_SDI1/I2S1_RXD	DL53	
DN31	GPP_S6/SNDW3_CLK/DMIC_CLK_A0	DG51	CNV_RF_RESET# IN 27 51
DM31	GPP_S7/SNDW3_DATA/DMIC_DATA0	DG50	
DK33	GPP_S4/SNDW2_CLK/DMIC_CLK_A1	DL49	CNV_CLKREQ IN 51
DK31	GPP_S5/SNDW2_DATA/DMIC_DATA1	DL52	
DW35	GPP_S2/SNDW1_CLK/DMIC_CLK_B0	DH49	2ND_WLAN_RF_OFF# OUT 51
DV35	GPP_S3/SNDW1_DATA/DMIC_CLK_B1	DF33	SNDW_RCOMP R4639 200_5%_2
DT32	GPP_S0/SNDW0_CLK		
DR35	GPP_S1/SNDW0_DATA		

43 IN DMIC_CLK_R_PCH — R4553 33_5%_2 — DMIC_CLK_PCH

43 OUT DMIC_DAT_R_PCH — R4552 0_5%_2 — DMIC_DAT_PCH

C4559 10PF_50V_2

R4513 RSC_0402_DY

C4558 CSC0402_DY

51 27 IN CNV_RF_RESET#

R4617 75K_1%_2

INTEL_J87879_BGA_1449P

6025B0422101

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION

Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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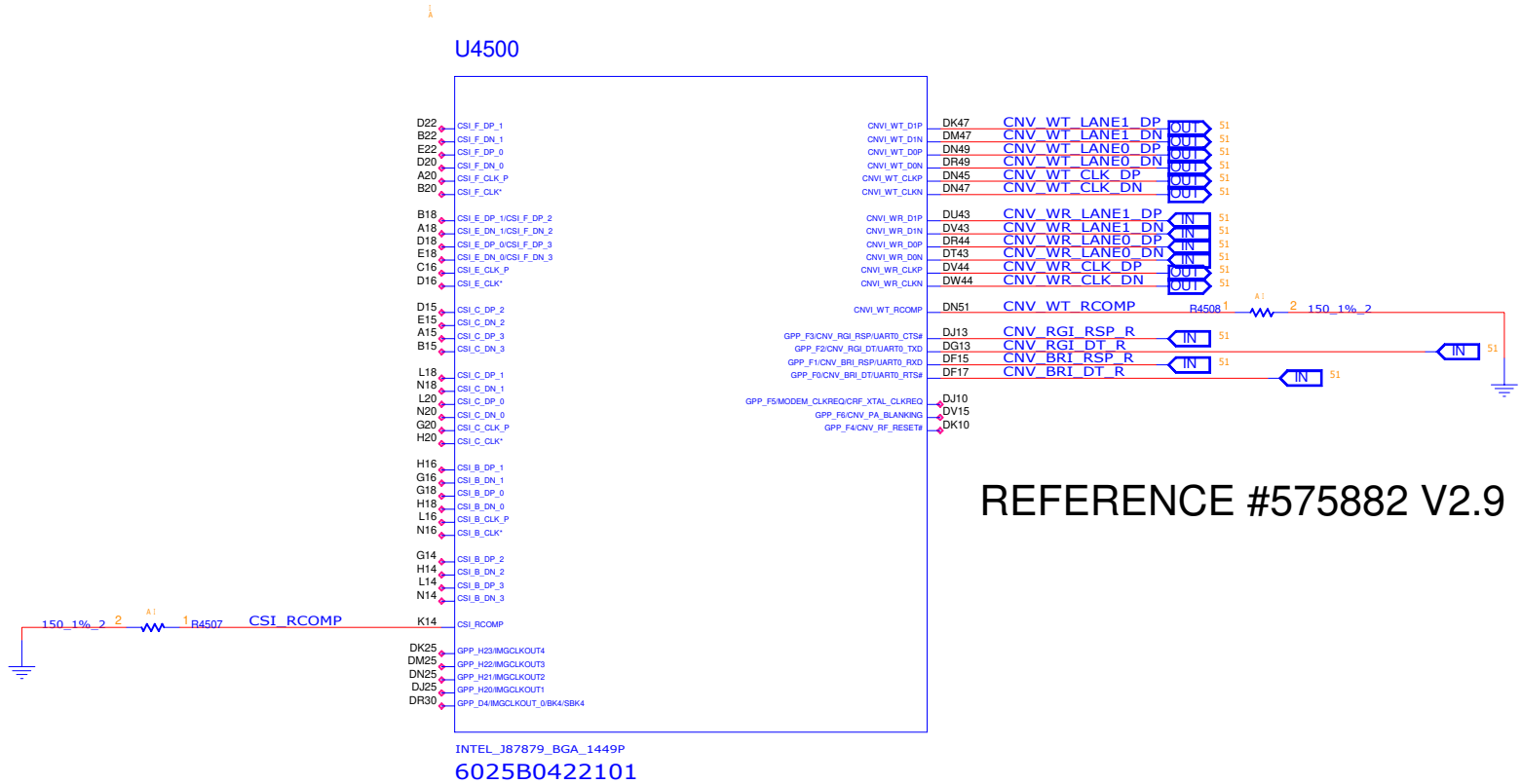
MCP-CSI/CNV



REFERENCE #575882 V2.9

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 28 of 70

MCP-PCIE/USB3/USB2

PORT# TABLE

M2.SSD	PCIE	PCIE4
0	12	0
1	11	1
2	10	2
3	9	3

CHIPSET SKU	Max USB 2.0 Nbr of Ports	USB 2.0 P1	USB 2.0 P2	USB 2.0 P3	USB 2.0 P4	USB 2.0 P5	USB 2.0 P6	USB 2.0 P7	USB 2.0 P8	USB 2.0 P9	USB 2.0 P10 (or CNVi BT)	USBr1	USBr2
PREMIUM-UP4	6												
PREMIUM-UP3	10												
MAINSTREAM BASE-UP3	8												

Port Disabled | Port Enabled | Port Enabled for Intel® Wireless-AC only

Table 72. PCH PCIe* Configuration Lane Reversal Mapping

PCIe* Configuration	PCI Express* Lanes				PCI Express* Down Device or Connector Lanes
	PCIe* Controller #1	PCIe* Controller #2 PCH-LP (UP3)	PCIe* Controller #2 PCH-LP (UP4)	PCIe* Controller #3	
1x4	1	5	Not Available	9	3
	2	6	Not Available	10	2
	3	7	Not Available	11	1
	4	8	Not Available	12	0

U4500

INTEL_J87879_BGA_1449P

6025B0422101

SSD

CARD READER

WLAN

WWAN

USB3.0 PORT R1

USB3.0 PORT L1

BLUETOOTH

WWAN

FP

WEBCAM

USB2.0 PORT TC MB (FOR TCP2 MAPPING)

USB2.0 PORT L1 MB

USB2.0 PORT R1 DB

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION

Block Diagram

SIZE A3 | CODE CS | DOC.NUMBER 1310xxxxx-0-0 | REV X01

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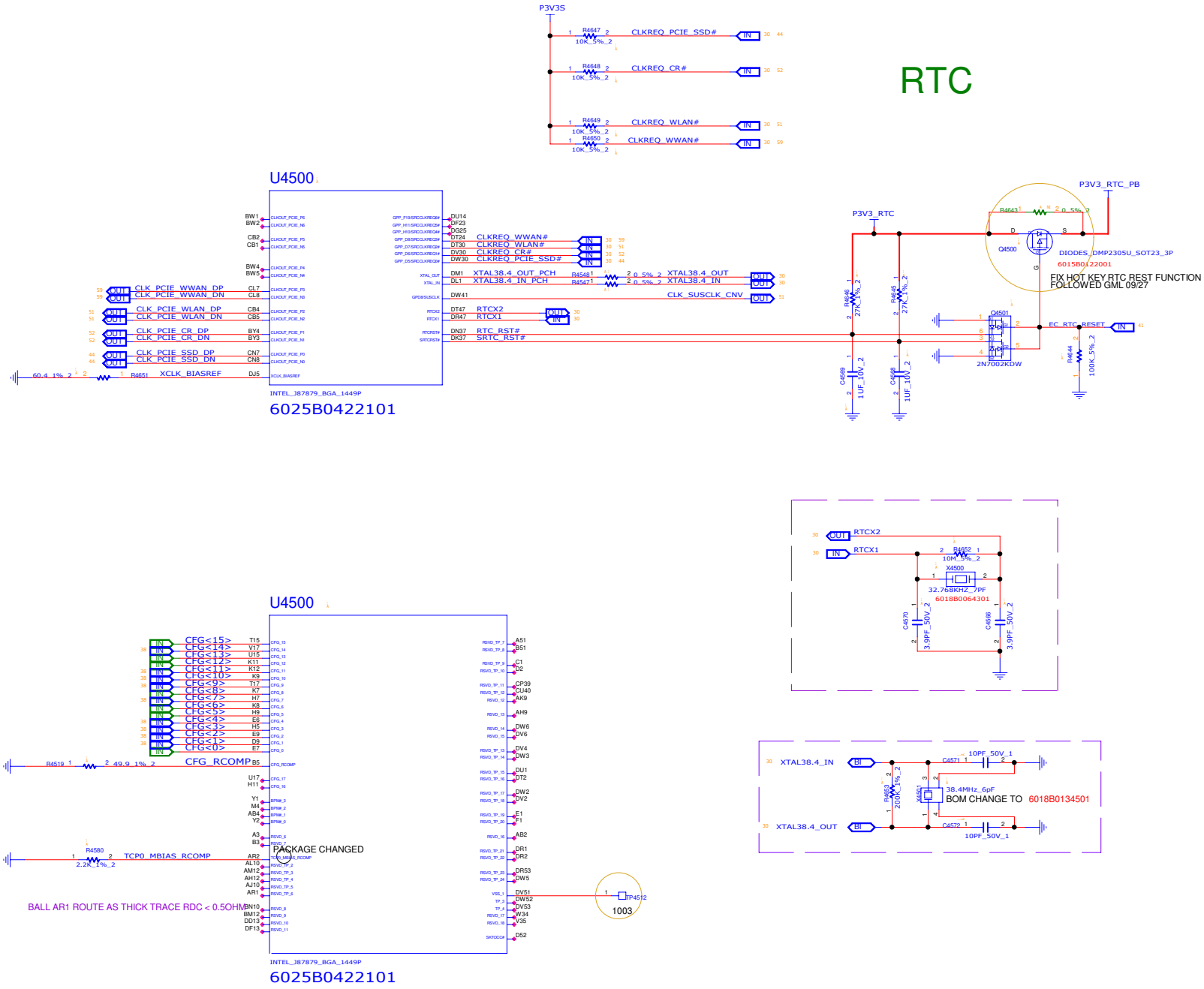
CHANGE by <ENG> | DATE 21-OCT-2002

PCB P/N 60xxxxxxxxxx | PCB VER <VER>

MCP-CLK/RTC/CFG



REFERENCE:4500~4949

CHANGE NO	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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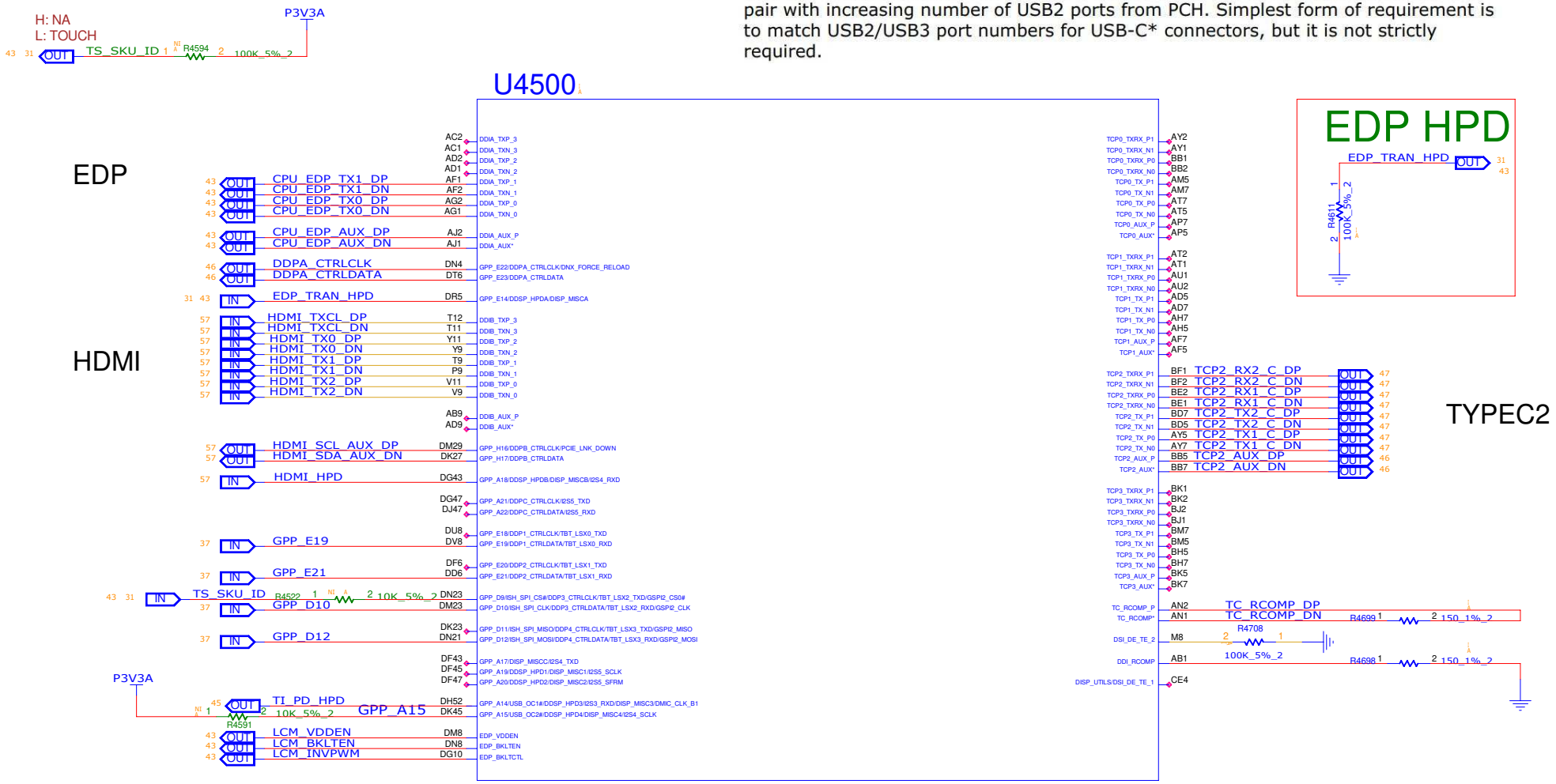
MCP-DDI/TCP

Table 32. USB3/USB2 Port Pairing for USB-C* Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.



INTEL_J87879_BGA_1449P

6025B0422101

REFERENCE:4500~4949

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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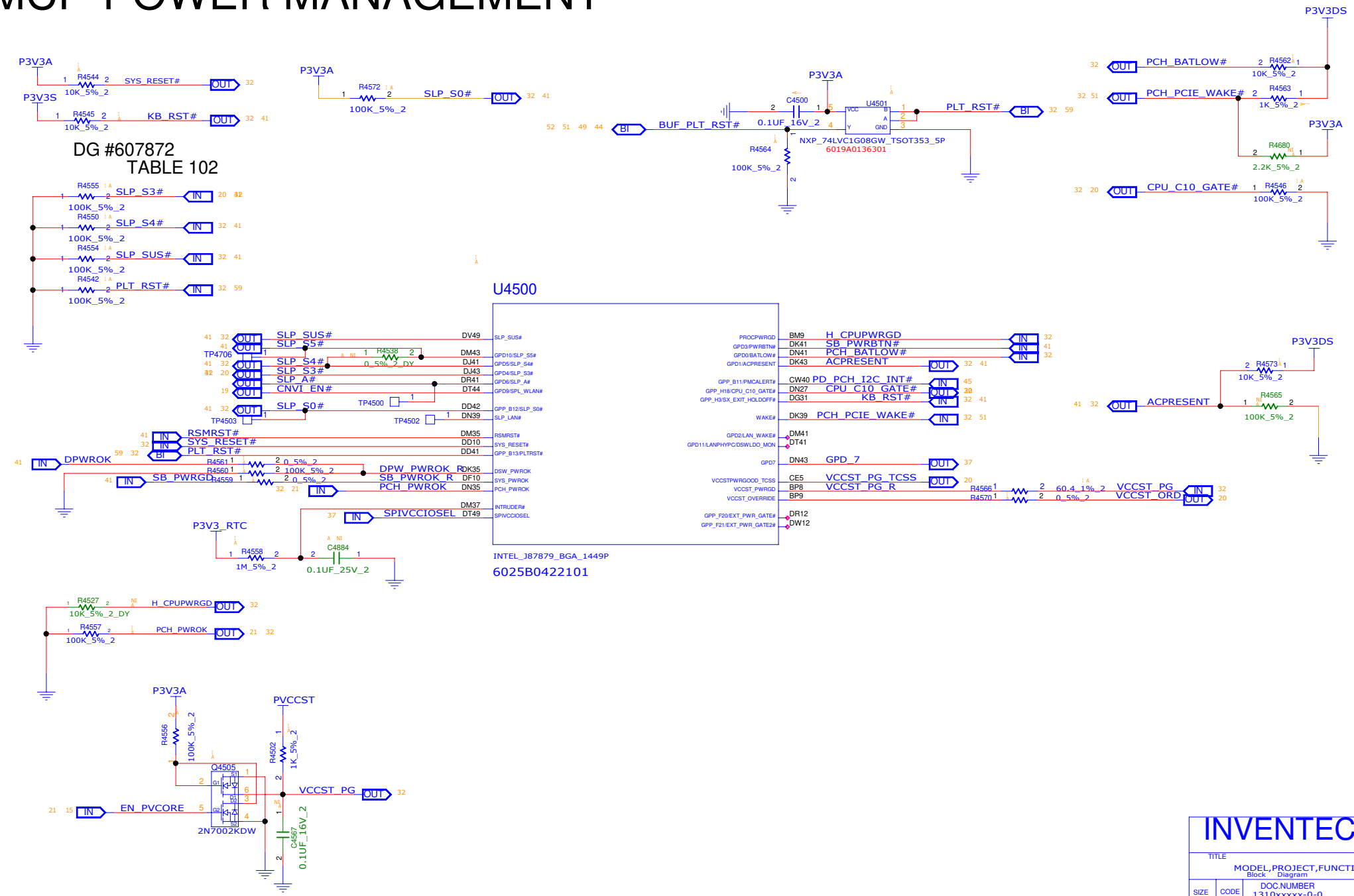
MCP-POWER MANAGEMENT



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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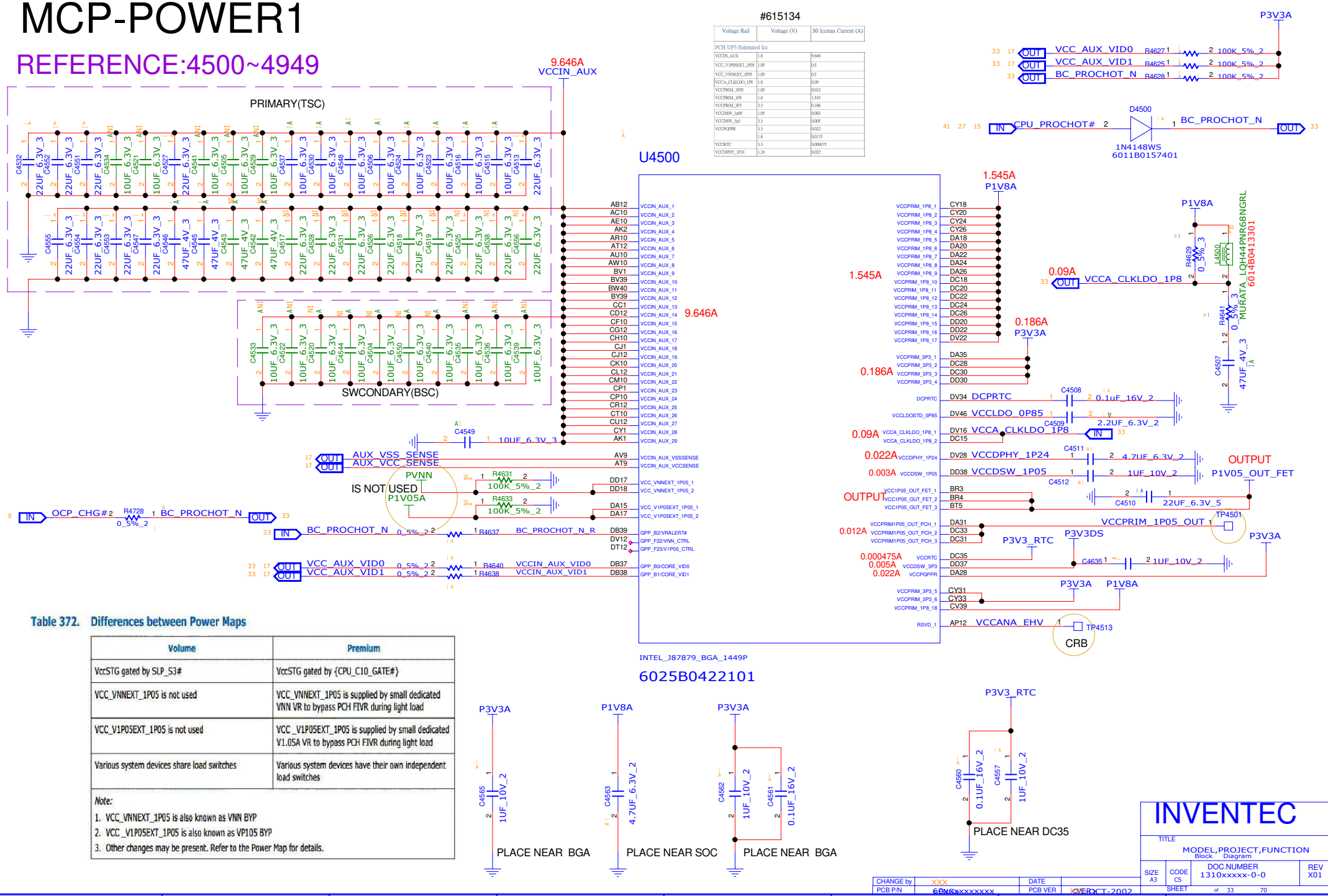
MCP-POWER1

REFERENCE:4500~4949



Voltage Rail	Voltage (V)	S0 Iccmax Current (A)
PCH UP3 Estimated Icc		
VCCIN_AUX	1.8	9.646
VCC_V1P05EXT_1P05	1.05	0.5
VCC_VNNEXT_1P05	1.05	0.5
VCCA_CLKLDO_1P8	1.8	0.09
VCCPRIM_1P05	1.05	0.012
VCCPRIM_1P8	1.8	1.545
VCCPRIM_3P3	3.3	0.186
VCCDSW_1p05	1.05	0.003
VCCDSW_3p3	3.3	0.005
VCCPGPPR	3.3	0.022
	1.8	0.0175
VCCRTC	3.3	0.000075
VCCDPHY_1P24	1.24	0.022

Table 372. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC_V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

Note:

1. VCC_VNNEXT_1P05 is also known as VNN BYP
2. VCC_V1P05EXT_1P05 is also known as VP105 BYP
3. Other changes may be present. Refer to the Power Map for details.

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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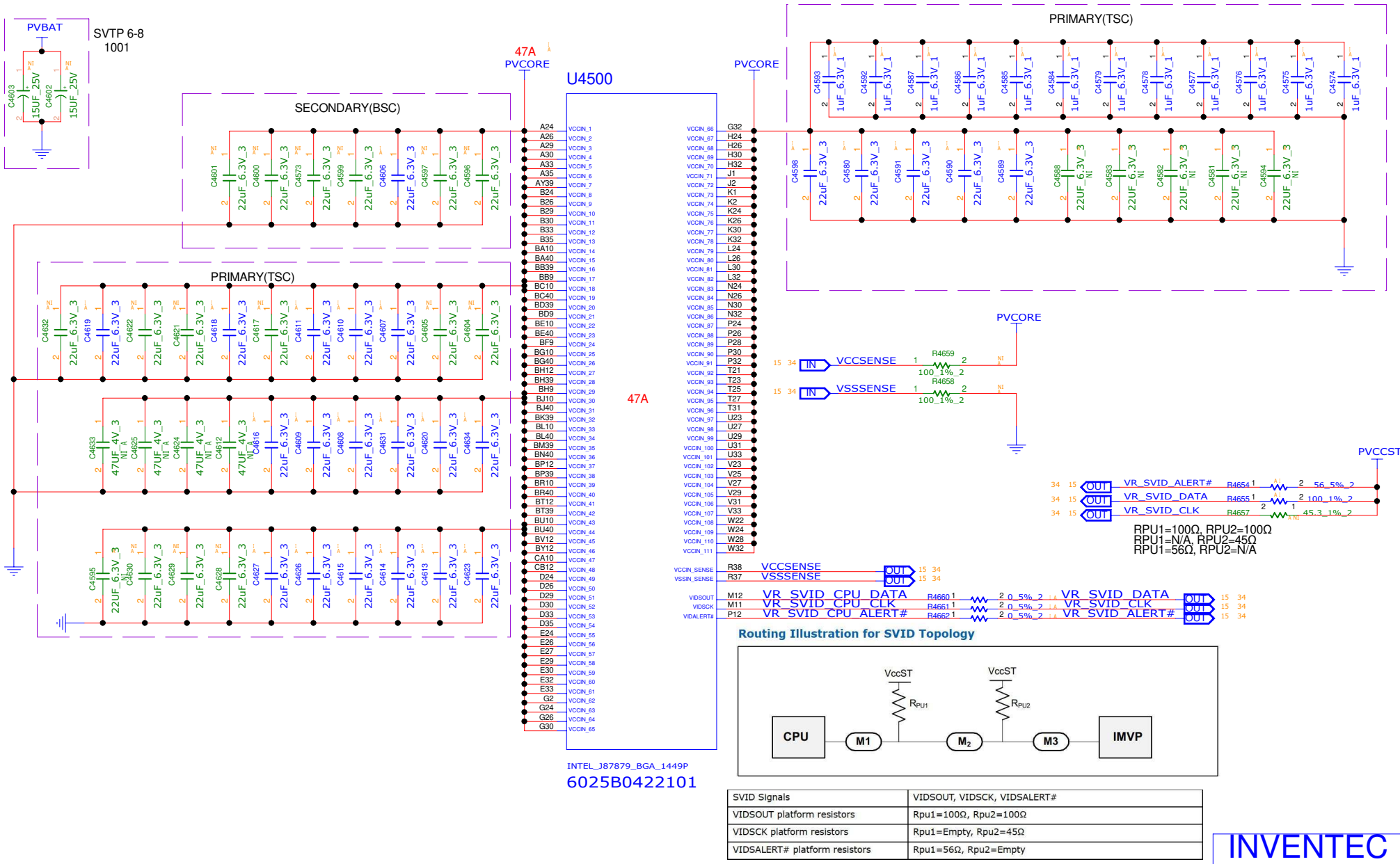
CHANGE by	XXX	DATE	
PCB P/N	60NXXXXXXXX	PCB VER	X01

OCT-2002

MCP-POWER2



Routing Illustration for SVID Topology

SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty

REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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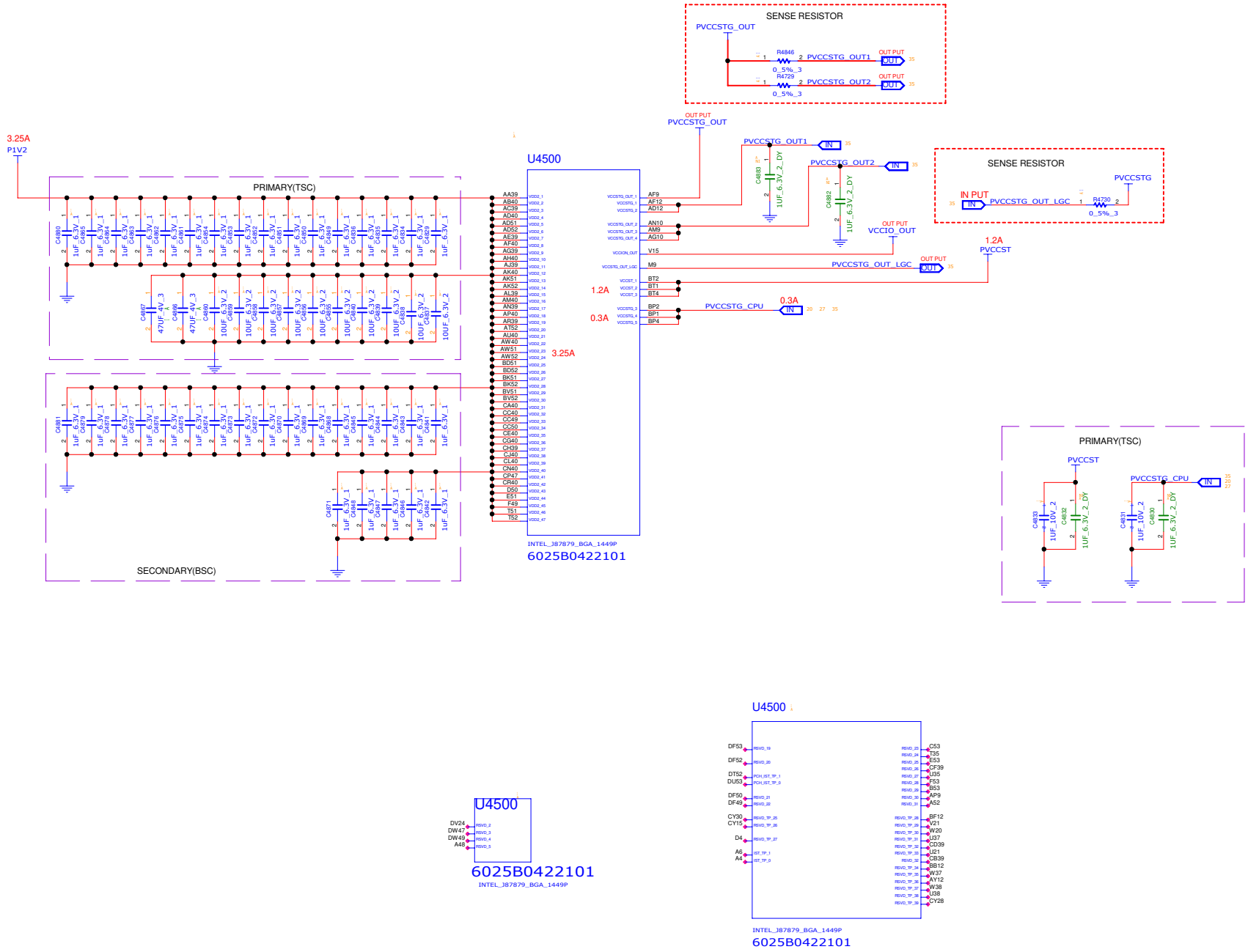
MCP-POWER3



REFERENCE:4500~4949

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

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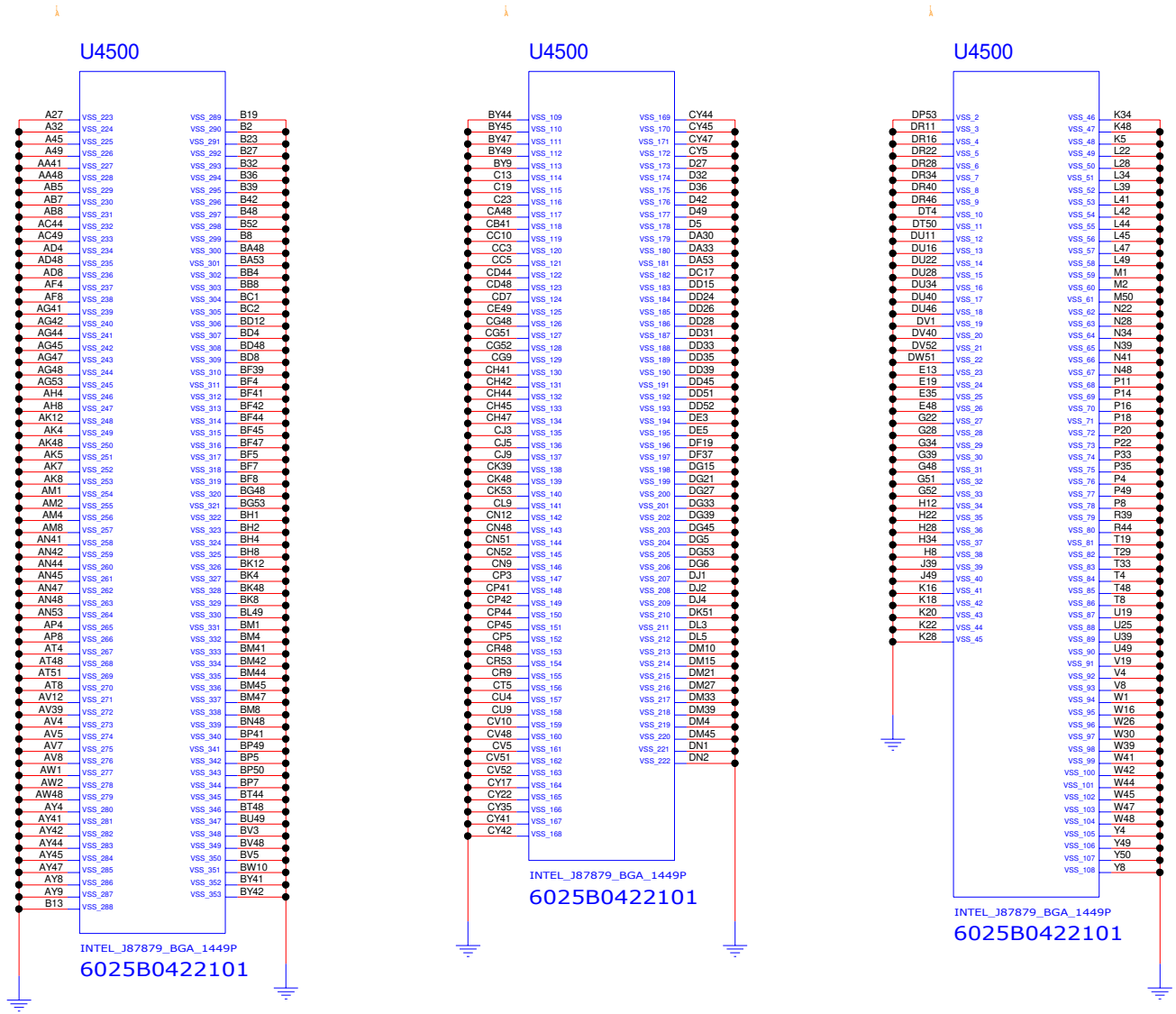
MCP-GND



REFERENCE:4500~4949

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	<ENG>	DATE	21-OCT-2002	SIZE A3	DOC.NUMBER 1310xxxxx-0-0
PCB P/N	60xxxxxxxxx	PCB VER	<VER>	CODE CS	REV X01

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#576591 PIN STRAP

TOP SWAP OVERRIDE

P3V3A — R4609 20K_5%_2_DY — GPP_B14 (IN) — PCSPKR

THE INTERNAL PULL-DOWN IS DISABLED AFTER PCH_PWROK IS HIGH.

THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "TOP SWAP" MODE. (DEFAULT)
1=>ENABLE "TOP SWAP" MODE.

NO REBOOT

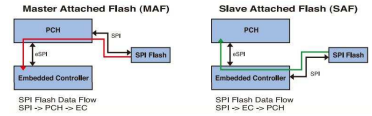
P3V3A — R4696 4.7K_5%_2_DY — GPP_B18 (IN) — R4707 20K_5%_2

THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "NO REBOOT" MODE. (DEFAULT)
1=>ENABLE "NO REBOOT" MODE (PCH WILL DISABLE THE TCO TIMER SYSTEM REBOOT FEATURE)
THIS FUNCTION IS USEFUL WHEN RUNNING ITP/XDP.

BOOT STRAP

P3V3A

	R	GPP	Pin
BOOT STRAP 0	R4703 4.7K_5%_2_DY / R4704 20K_5%_2	GPP_C5 (IN)	25
BOOT STRAP 1	R4683 4.7K_5%_2_DY / R4684 20K_5%_2	GPP_H0 (IN)	27
BOOT STRAP 2	R4672 4.7K_5%_2_DY / R4678 20K_5%_2	GPP_H1 (IN)	27
BOOT STRAP 3	R4671 4.7K_5%_2_DY / R4673 20K_5%_2	GPP_H2 (IN)	27



THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
THIS STRAP IS USED IN CONJUNCTION WITH BOOT STRAP 1,2,3, (ON GPP_H0, GPP_H1, GPP_H2 RESPECTIVELY).
0000 = MASTER ATTACHED FLASH CONFIGURATION (BIOS / CSME ON SPI). ESPI IS ENABLED

THE INTERNAL PULL-DOWN IS DISABLED AFTER RSMRST# DE-ASSERTS.

TLS CONFIDENTIALITY

P3V3A — R4697 4.7K_5%_2_DY — TLS — GPP_C2 (IN) — R4702 20K_5%_2

THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
0=>DISABLE "NO REBOOT" MODE. (DEFAULT)

THIS FUNCTION IS USEFUL WHEN RUNNING ITP/XDP.

CPUNSSC CLOCK FREQUENCY

P3V3A — R4682 4.7K_5%_2_DY — GPP_B23 (IN) — R4723 20K_5%_2

0 = 38.4 MHZ CLOCK (DIRECT FROM CRYSTAL) (DEFAULT)
1 = 19.2 MHZ CLOCK (DERIVED FROM 38.4 MHZ CRYSTAL)

THE STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

P1V05_OUT_FET

RESERVED

R4679 1K_5%_2 — DBG_PMODE (IN)

THIS STRAP SHOULD SAMPLE HIGH

RESERVED

GPP_F10 (IN) — R4690 20K_5%_1

THIS STRAP SHOULD SAMPLE LOW

SPI0_IO3 SPI0_IO2 SPI0_MOSI

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

RESERVED

P3V3A — R4705 10K_1%_2 — GPP_E6 (IN)

EXTERNAL PULL-UP IS REQUIRED.

RESERVED

GPD_7 (IN) — R4681 20K_5%_2

THIS STRAP SHOULD SAMPLE LOW.
THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

RESERVED

GPP_F7 (IN) — R4692 20K_5%_1

THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.
THIS STRAP SHOULD SAMPLE LOW.

THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

P3V3A

0 = DDP3 I2C / TBT_LSX2 PIN AT 1.8V
1 = DDP3 I2C / TBT_LSX2 PIN AT 3.3V

R4689 4.7K_5%_2 — GPP_D10 (IN) — R4725 20K_5%_2
R4722 4.7K_5%_2 — GPP_D12 (IN) — R4581 20K_5%_2

0 = DDP4 I2C / TBT_LSX3 PINS AT 1.8V
1 = DDP4 I2C / TBT_LSX3 PINS AT 3.3

TCP3 PU =HDMI / PD =TBT & USB C

THIS STRAP HAS A 20 KOHM ± 30% INTERNAL PULL-DOWN.

P3V3A

0 = DDP1 I2C / TBT_LSX0 PINS AT 1.8V
1 = DDP1 I2C / TBT_LSX0 PINS AT 3.3V

R4669 4.7K_5%_2 — GPP_E19 (IN) — R4670 20K_5%_2
R4727 4.7K_5%_2 — GPP_E21 (IN) — R4724 20K_5%_2

0 = DDP2 I2C / TBT_LSX1 PINS AT 1.8V
1 = DDP2 I2C / TBT_LSX1 PINS AT 3.3V

0 = SPI VOLTAGE IS 3.3V (4.7 KOHM PULL-DOWN TO GND)
1 = SPI VOLTAGE IS 1.8V (4.7K PULL-UP TO DSW_PWROK)

SPIVCCIOSEL (IN) — R4685 4.7K_5%_2

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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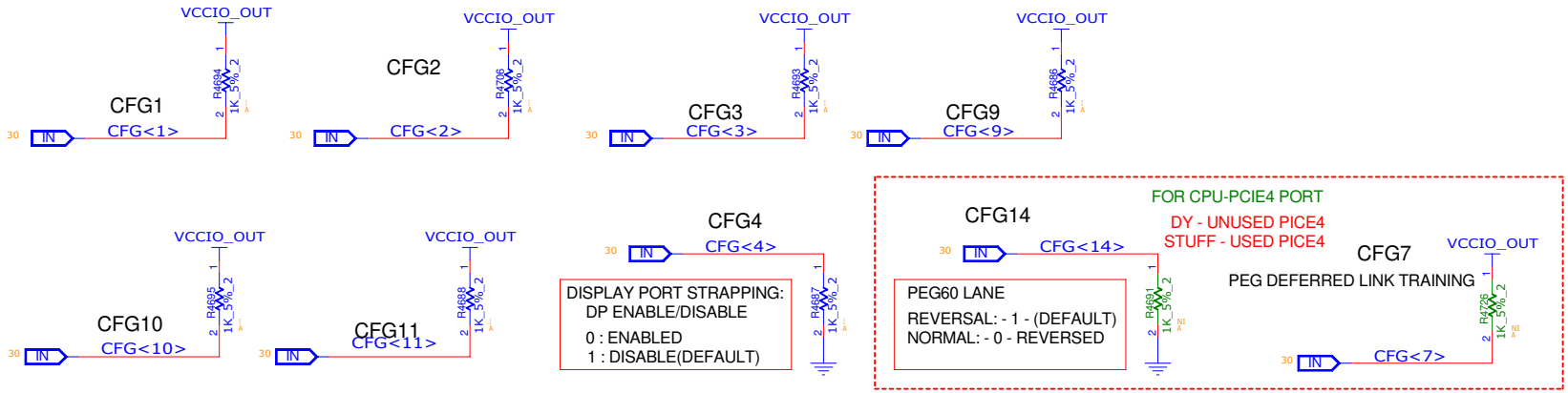
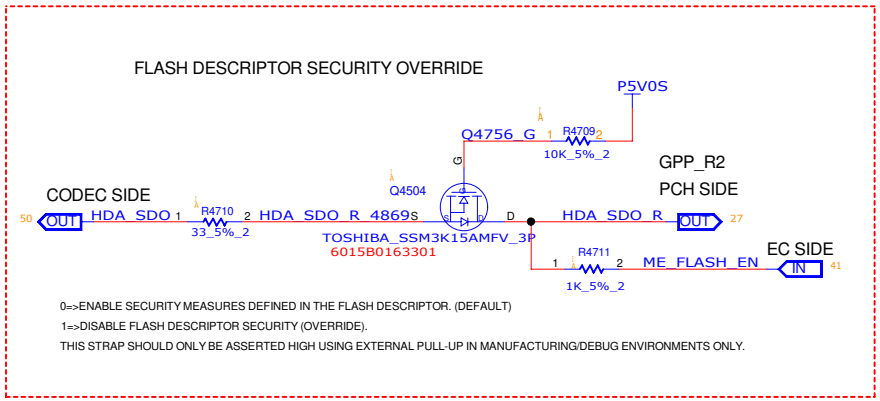
MCP-STRAPS-1

607872 TABLE62



ME UNLOCK FLASH



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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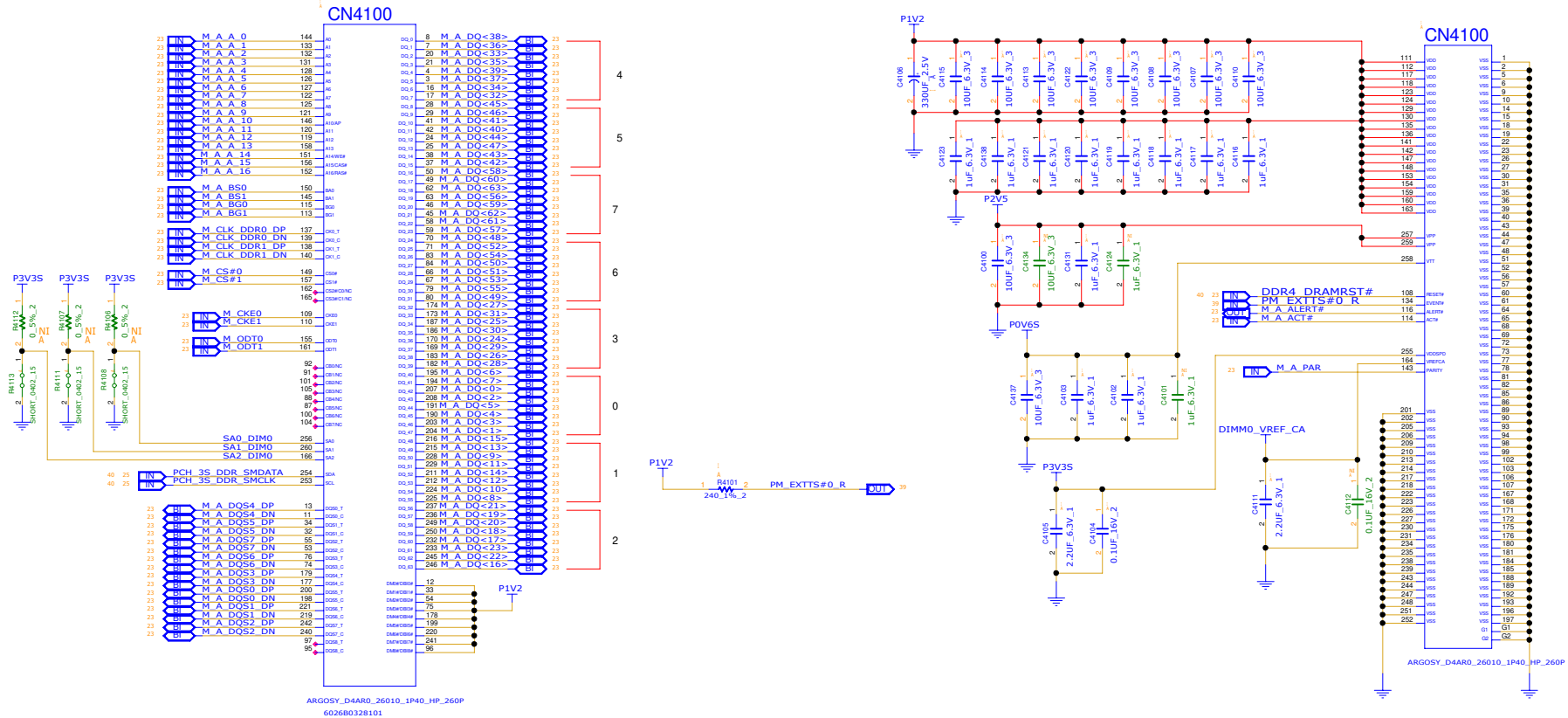
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



SPD ADDRESS FOR CHANNEL-0

WRITE ADDRESS:0XA0

RED ADDRESS :0XA1

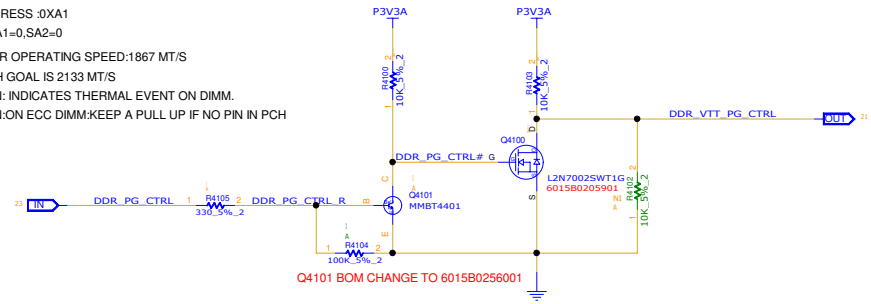
SA0=0,SA1=0,SA2=0

DDR4 FOR OPERATING SPEED:1867 MT/S

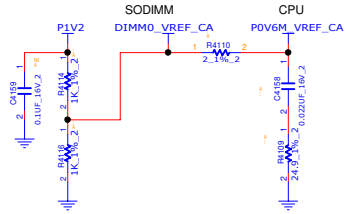
STRETCH GOAL IS 2133 MT/S

EVENT_N: INDICATES THERMAL EVENT ON DIMM.

EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH



Q4101 BOM CHANGE TO 6015B0256001



CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	50xxxxxxxxx	PCB VER	XXX

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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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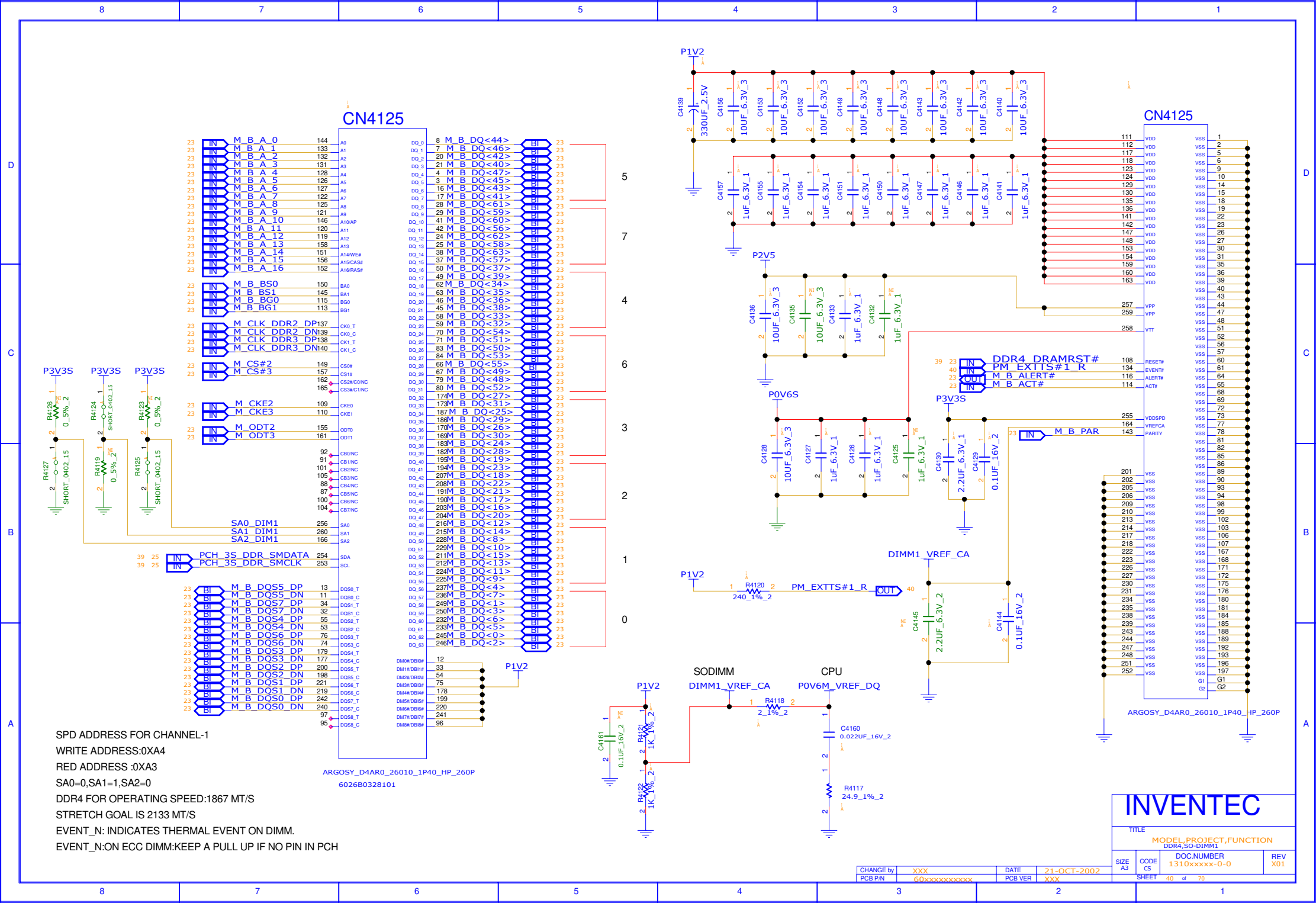
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M_B_BS1
M_B_BG0
M_B_BG1
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M_CLK_DDR3_DP
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M_CS#2
M_CS#3
M_CKE2
M_CKE3
M_ODT2
M_ODT3
P3V3S
R4126
R4124
R4123
R4127
R4119
R4125
SHORT_0402_15
0_5%_2
SA0_DIM1
SA1_DIM1
SA2_DIM1
PCH_3S_DDR_SMDATA
PCH_3S_DDR_SMCLK
M_B_DQS5_DP
M_B_DQS5_DN
M_B_DQS7_DP
M_B_DQS7_DN
M_B_DQS4_DP
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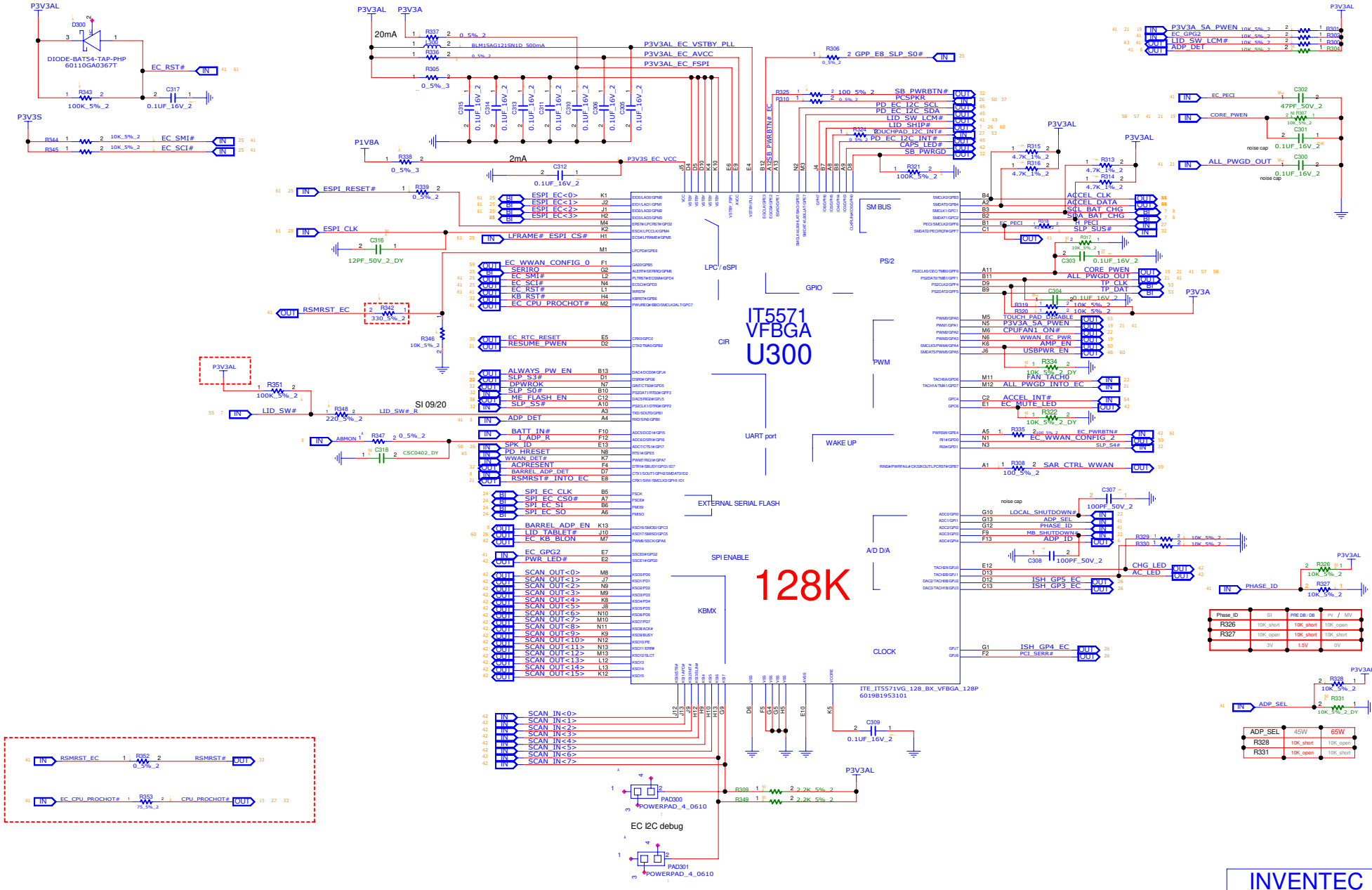
M_B_DQ<6>
M_B_DQ<5>
M_B_DQ<0>
M_B_DQ<2>
P1V2
ARGOSY_D4AR0_26010_1P40_HP_260P
6026B0328101
SPD ADDRESS FOR CHANNEL-1
WRITE ADDRESS:0XA4
RED ADDRESS :0XA3
SA0=0,SA1=1,SA2=0
DDR4 FOR OPERATING SPEED:1867 MT/S
STRETCH GOAL IS 2133 MT/S
EVENT_N: INDICATES THERMAL EVENT ON DIMM.
EVENT_N:ON ECC DIMM:KEEP A PULL UP IF NO PIN IN PCH
P1V2
C4139
330UF_2.5V
C4156
C4153
C4152
C4149
C4148
C4143
C4142
C4140
10UF_6.3V_3
C4157
C4155
C4154
C4151
C4150
C4147
C4146
C4141
1uF_6.3V_1
P2V5
C4136
C4135
C4133
C4132
P0V6S
C4128
C4127
C4126
C4125
P3V3S
C4130
C4129
2.2UF_6.3V_1
0.1UF_16V_2
DDR4_DRAMRST#
PM_EXTTS#1_R
M_B_ALERT#
M_B_ACT#
M_B_PAR
CN4125
VDD
VSS
VPP
VTT
VDDSPD
VREFCA
PARITY
RESET#
EVENT#
ALERT#
ACT#
ARGOSY_D4AR0_26010_1P40_HP_260P
DIMM1_VREF_CA
R4120
240_1%_2
C4145
C4144
SODIMM
CPU
P0V6M_VREF_DQ
R4118
2_1%_2
C4160
0.022UF_16V_2
R4117
24.9_1%_2
C4161
R4121
R4122
1K_1%_2
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
DDR4,SO-DIMM1
SIZE
A3
CODE
CS
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET
40
of
70
CHANGE by
XXX
DATE
21-OCT-2002
PCB P/N
60xxxxxxxxx
PCB VER
XXX

EC



Phase_ID	SI	PRE DB / DB	PV / MV
R326	10K_short	10K_short	10K_open
R327	10K_open	10K_short	10K_short
	3V	1.5V	0V

ADP_SEL	45W	65W
R328	10K_short	10K_open
R331	10K_open	10K_short

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE N	XXX	DATE	21-OCT-2002
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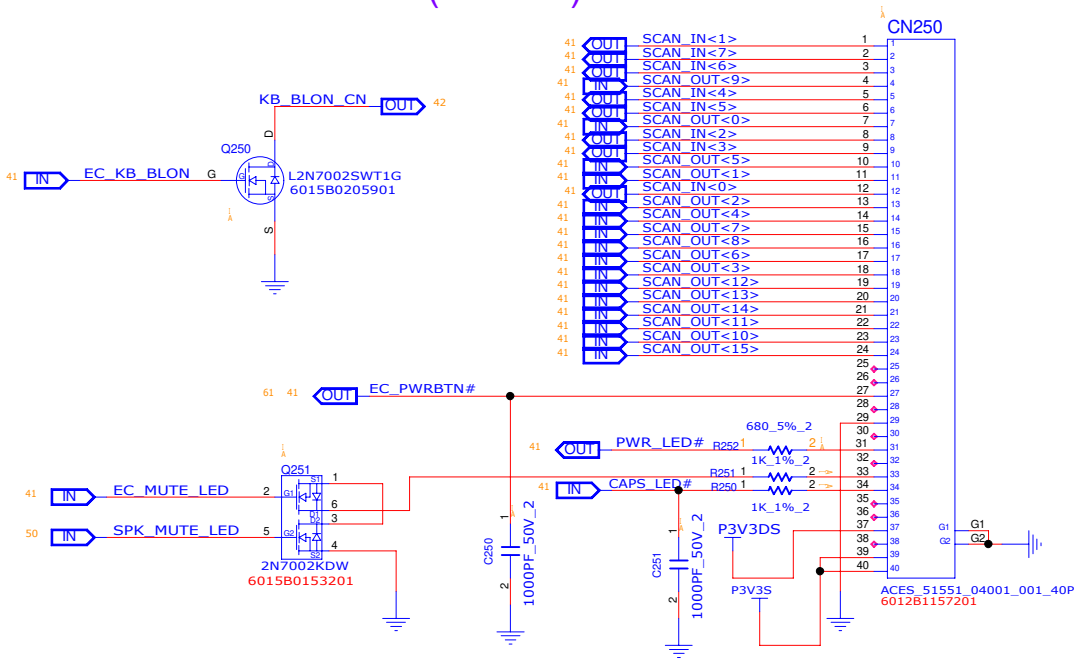
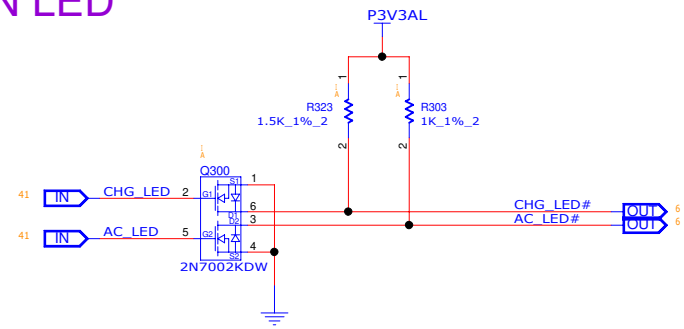
KEYBOARD CONNECTOR

KEYBOARD CONN(40 PIN)



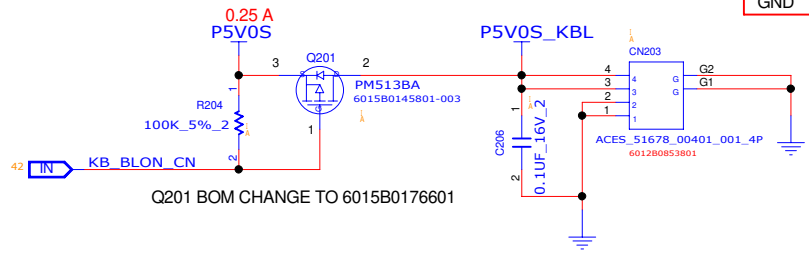
AC-IN LED



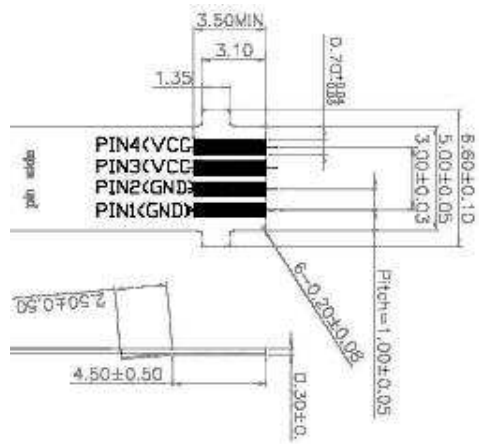
CONNECTOR KEY BOARD 200~299

KEYBOARD BACKLIGHT

VCC	PIN1
VCC	PIN2
GND	PIN3
GND	PIN4



Q201 BOM CHANGE TO 6015B0176601



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION KB CONN & LED		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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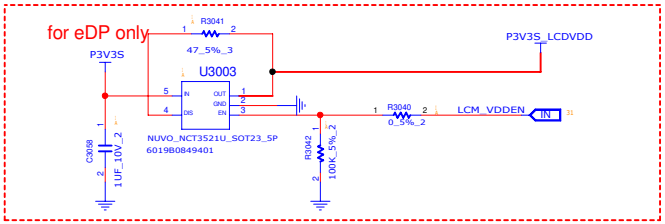
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

LCM :

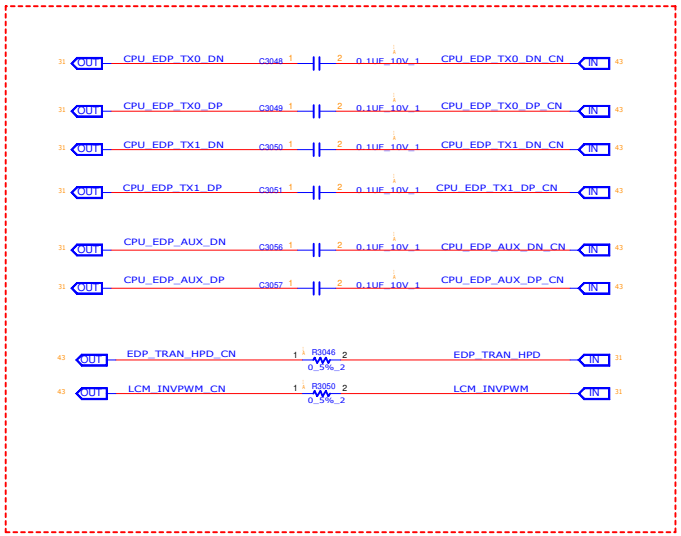
LOCATION 3000 ~ 3049

VER.14_20171119

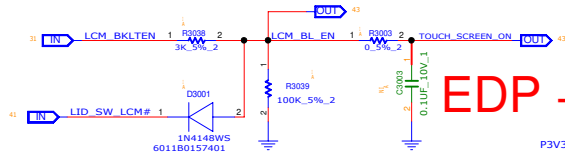
eDP



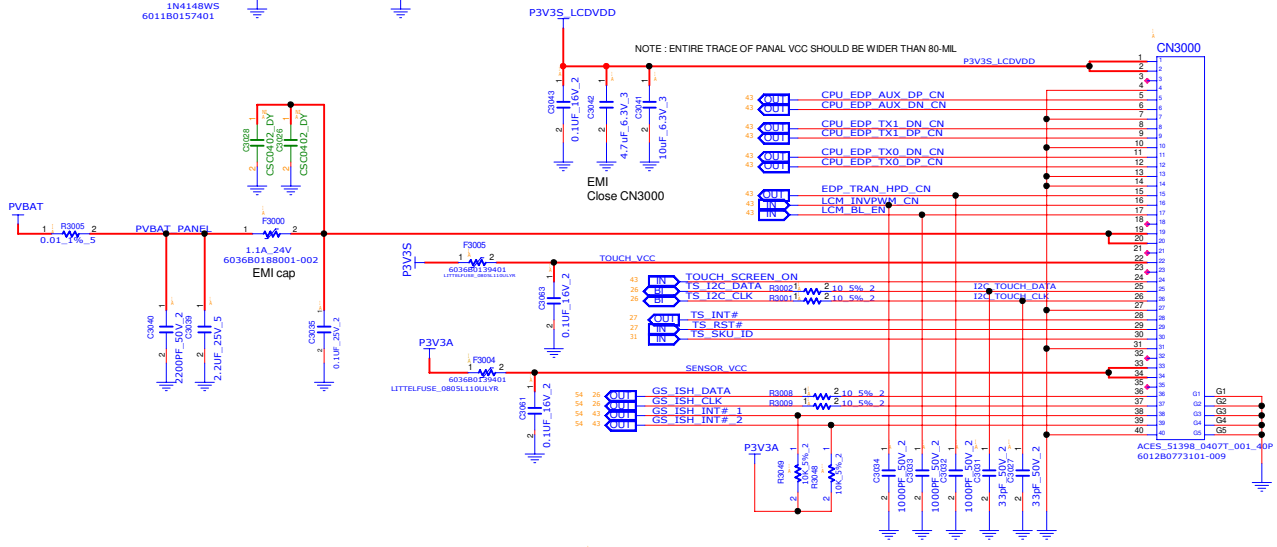
eDP

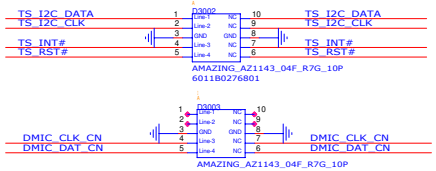


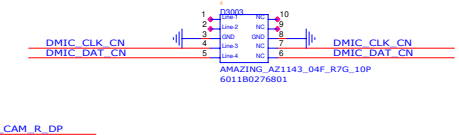
eDP



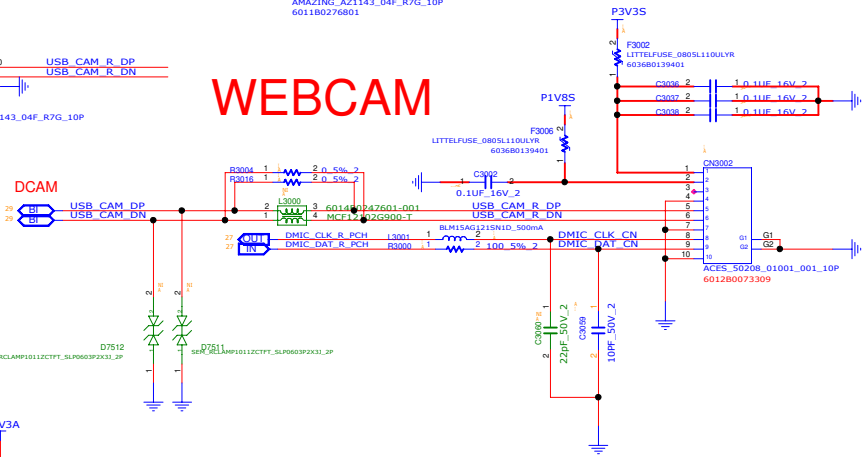
EDP + TOUCH SCREEN + G-SENSOR

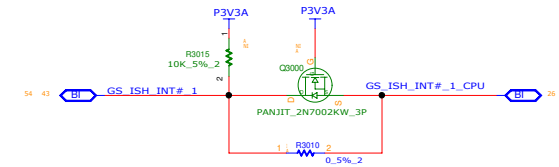


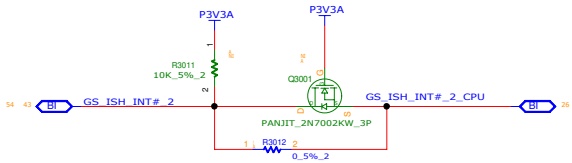


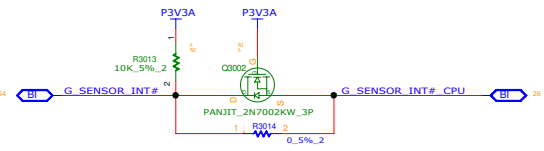


WEBCAM









INVENTEC

MODEL,PROJECT,FUNCTION

LVDS

SIZE	CODE	DOC NUMBER	REV
C	CS	131Oxxxxx-0-0	X01

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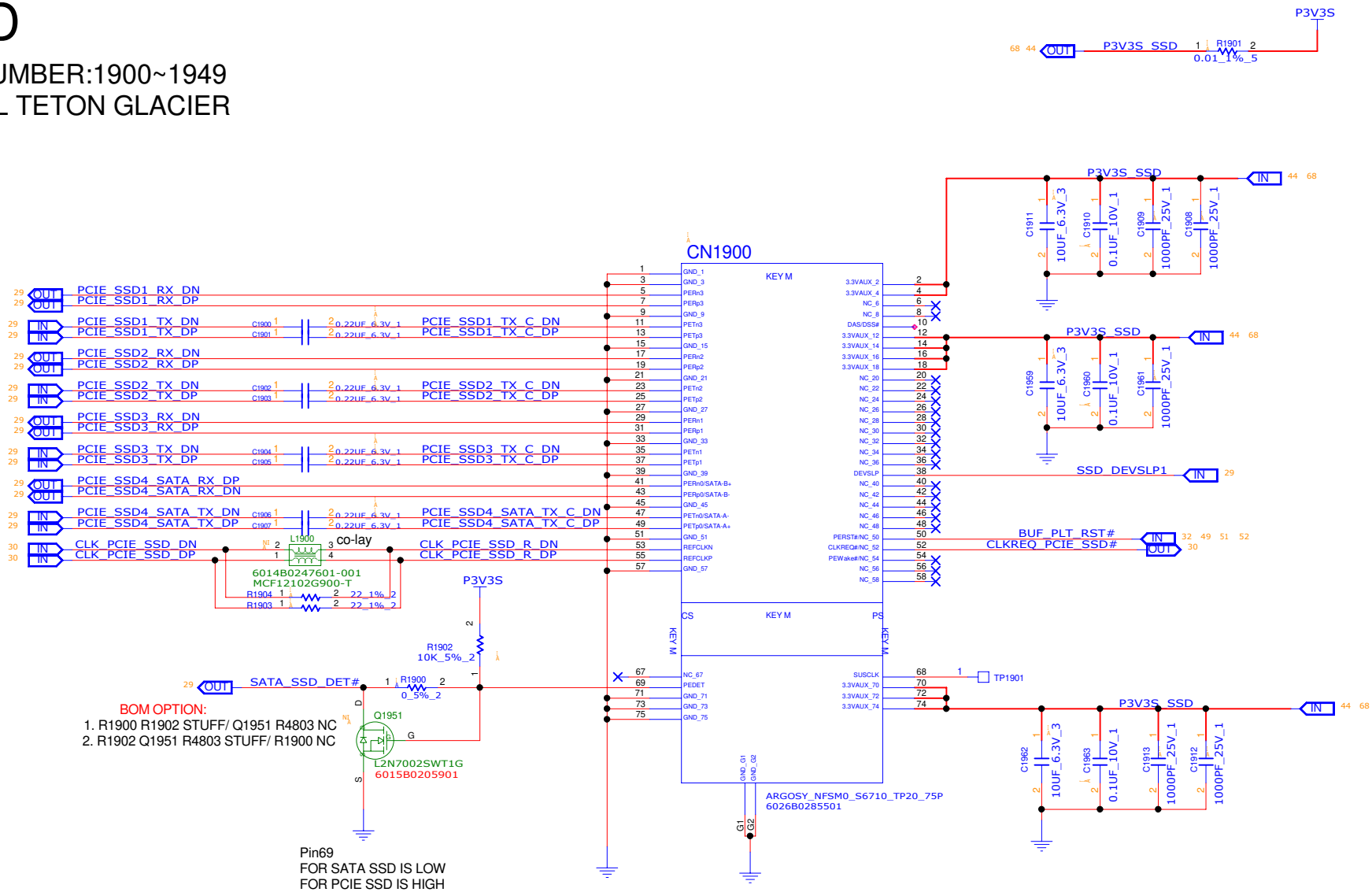
CHANGE by	XXX	DATE	
PCB P/N	60.xxxxx.xxxx	PCB VER	OPTION

M.2 SSD

REFERENCE NUMBER:1900~1949
SUPPORT INTEL TETON GLACIER



CHANGE by	<ENG>	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	<VER>		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NGFF- SSD

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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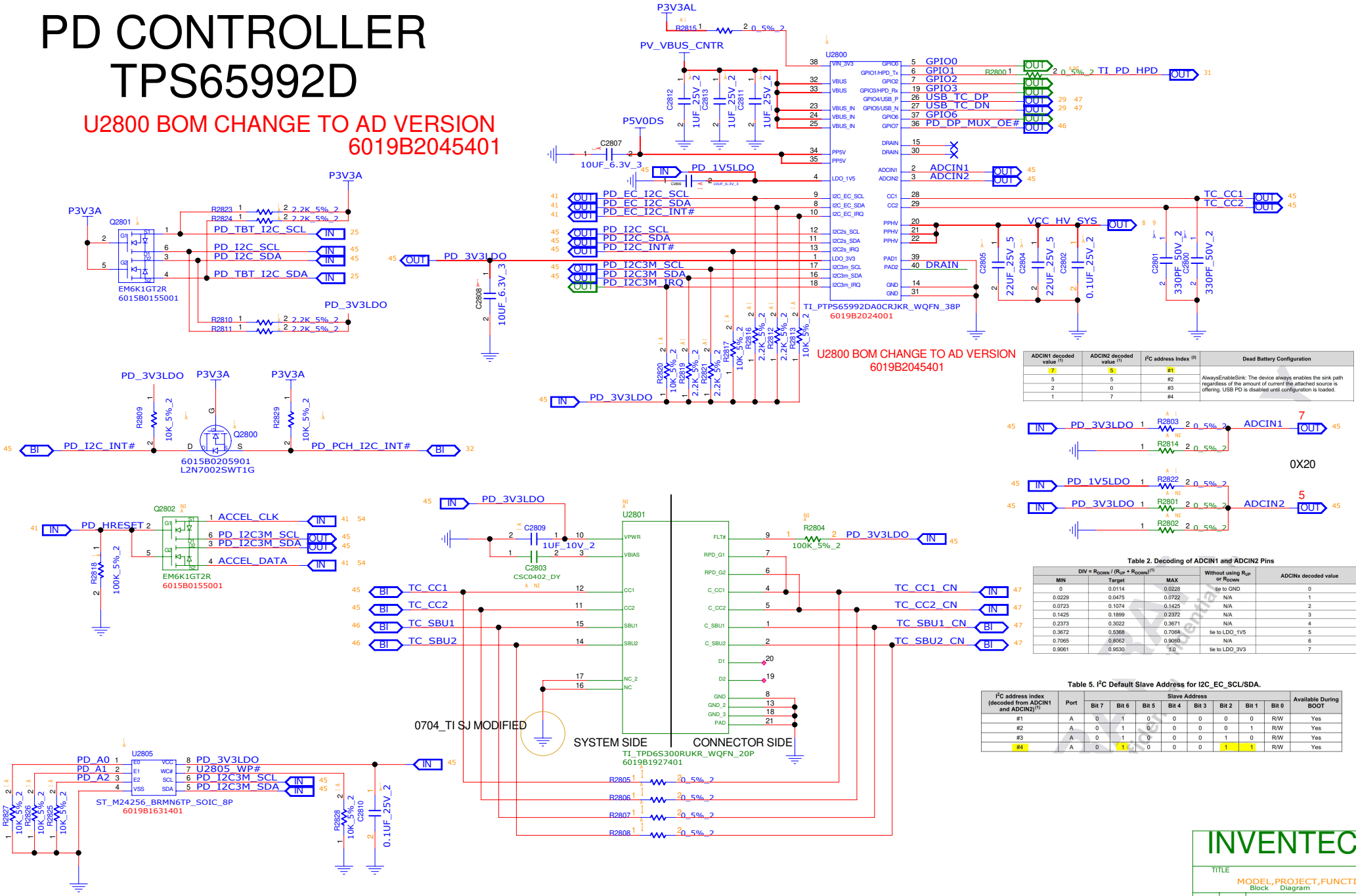
PD CONTROLLER
TPS65992D

U2800 BOM CHANGE TO AD VERSION
6019B2045401



ADCIN1 decoded value (1)	ADCIN2 decoded value (1)	I²C address Index (2)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN}) (1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

Table 5. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2) (1)	Port	Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	A	0	1	0	0	0	0	0	R/W	Yes
#2	A	0	1	0	0	0	0	1	R/W	Yes
#3	A	0	1	0	0	0	1	0	R/W	Yes
#4	A	0	1	0	0	0	1	1	R/W	Yes

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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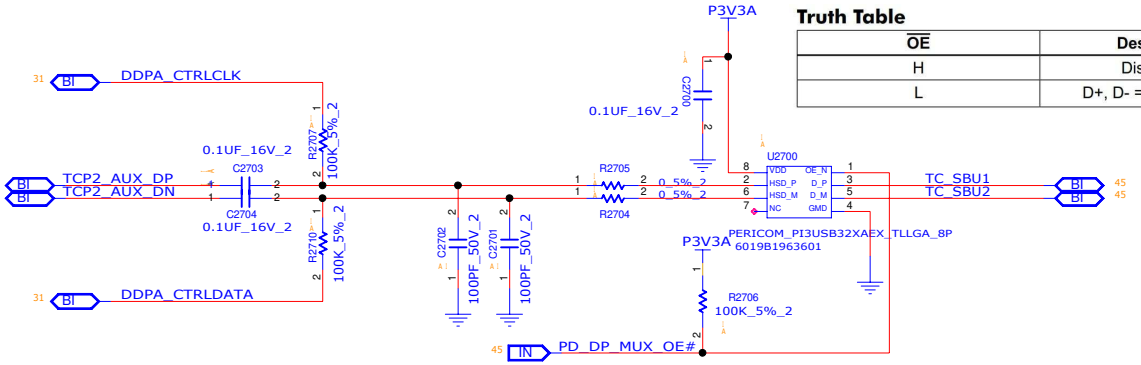
TGL DP ALTERNATE MODE W/O RE-TIMER

TYPE C CONNECTOR

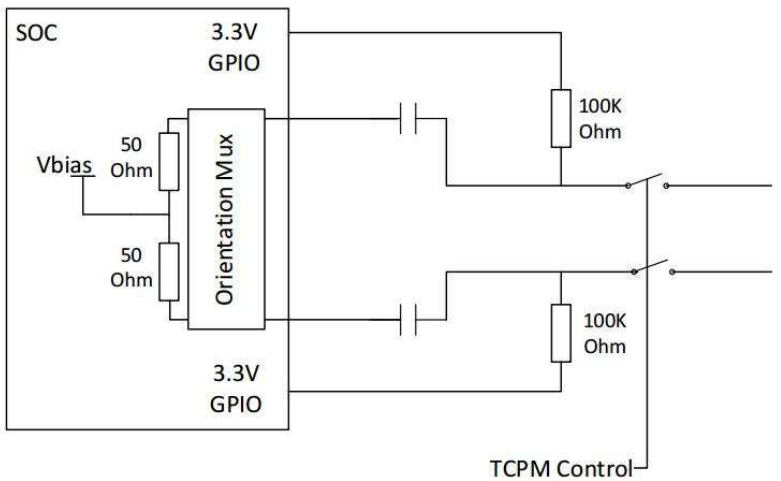
SOC



Truth Table

$\overline{OE}$	Description
H	Disconnect
L	D+, D- = HSD+, HSD-

PD



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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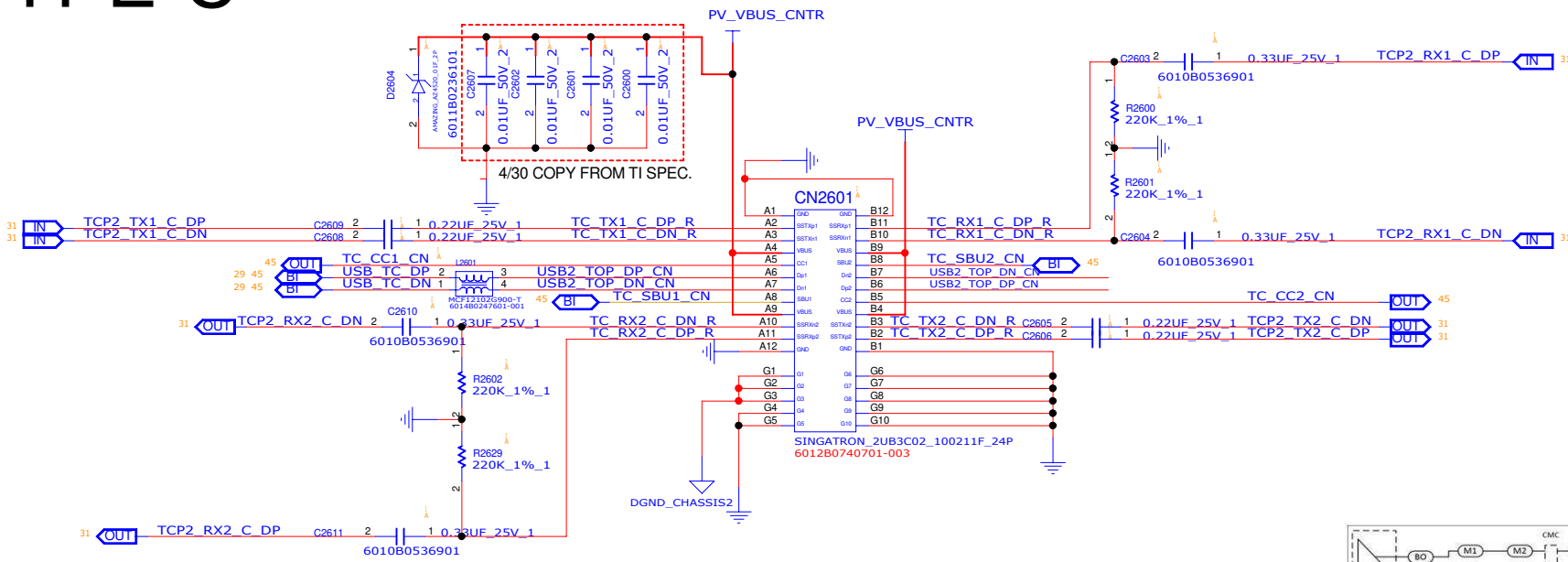
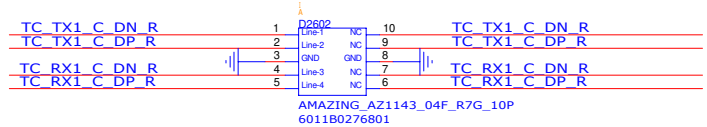
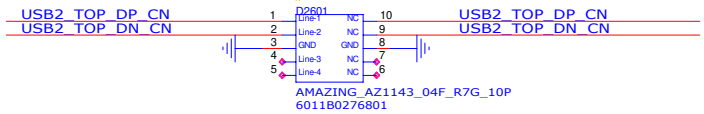
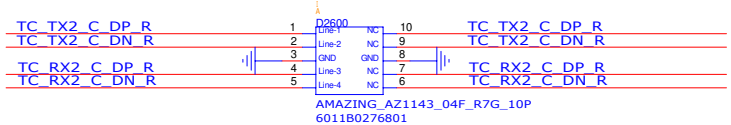
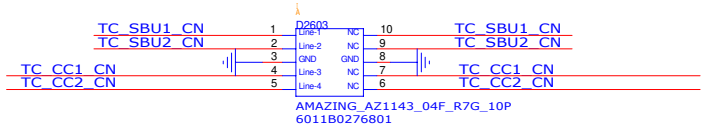
TYPE-C

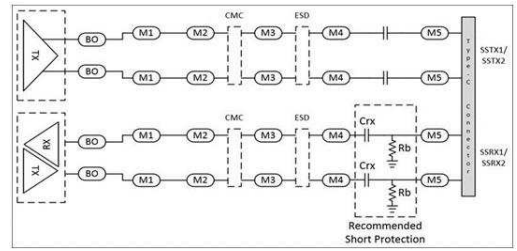




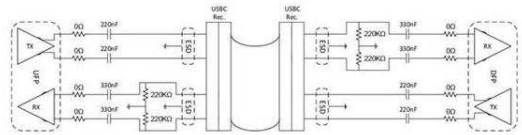








New TBT3 CIO Lines Topology



- ✓ 0Ω resistor might change up to 3Ω to better limit the surge current in an event of VBUS-short to SSTX/RX.
- ✓ RX capacitor (330nF ± 10%) was added for better VBUS-short protection on SSRX lines.
- ✓ Discharge resistor (220KΩ) was added to bias SSRX lines due to the new 330nF RX capacitor.
- ✓ TX capacitor (220nF ± 20%) didn't change.
- ✓ ESD (TVS diodes) didn't change.

THUNDERBOLT

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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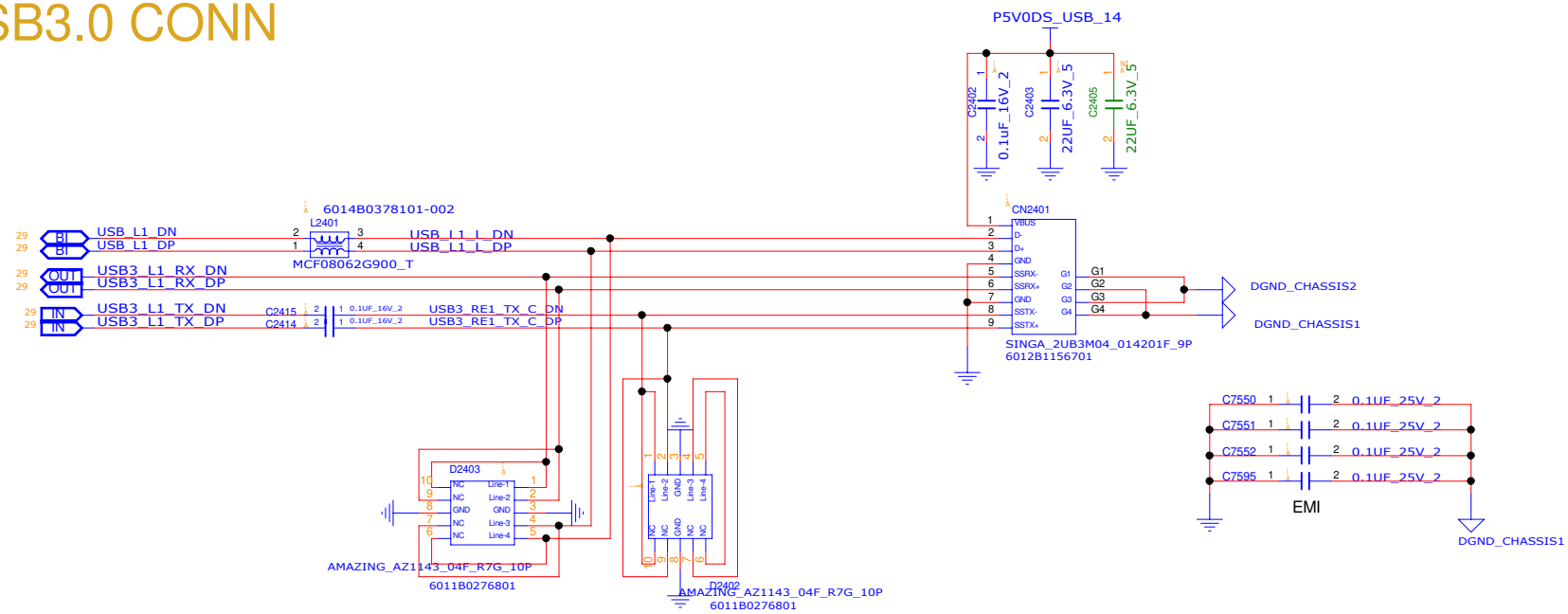
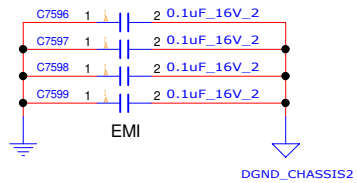
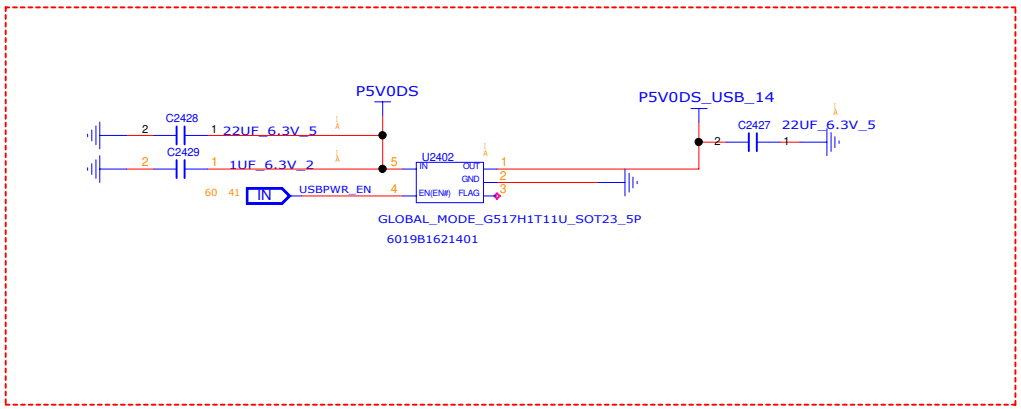
USB3.0 CONN



TOP X2, Bottom x2





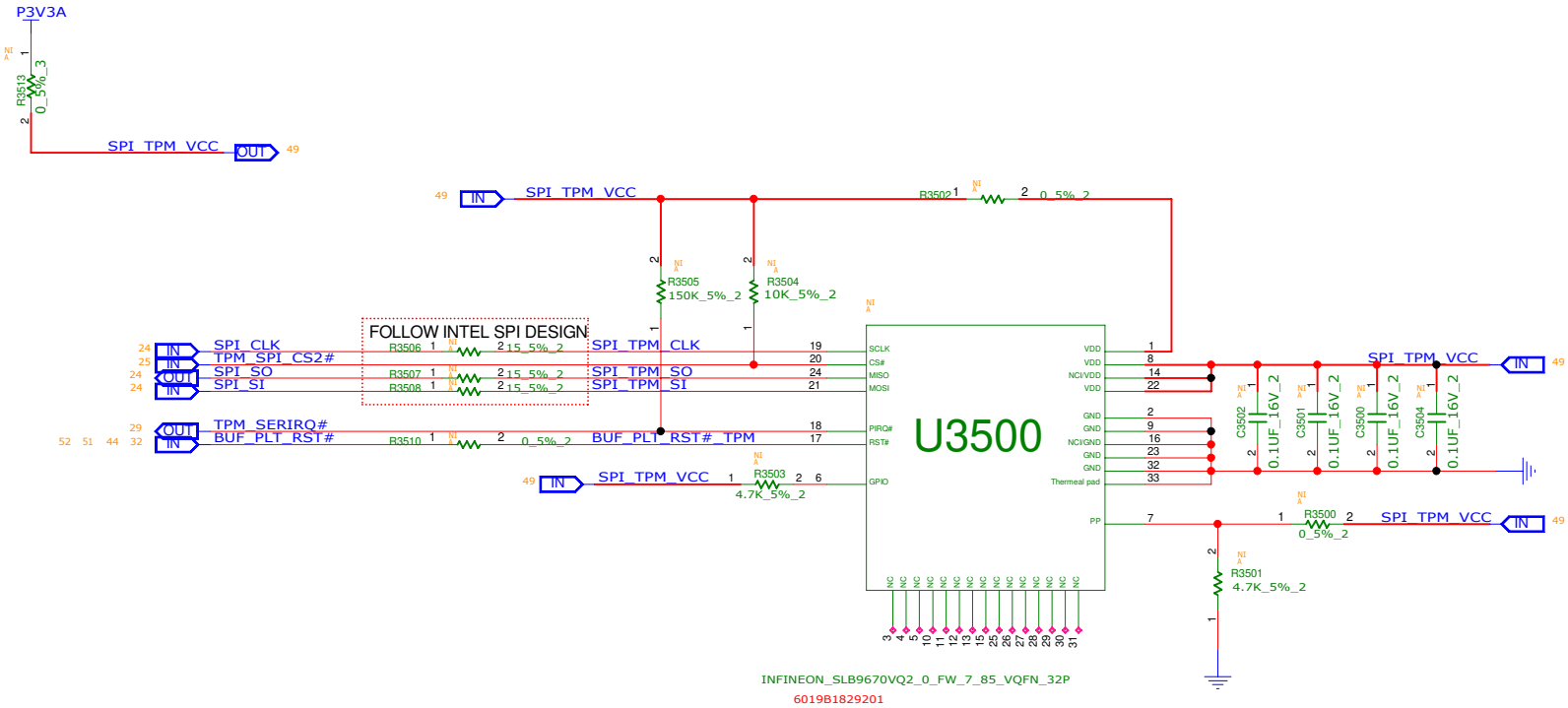
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION USB 3.0 CONN & M/B TO D/B CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET of 48 70			

CHANGE by	XXX	DATE	
PCB P/N	60NBxxxxxxxx	PCB VER	XX

VER:OCT-2002

TPM2.0



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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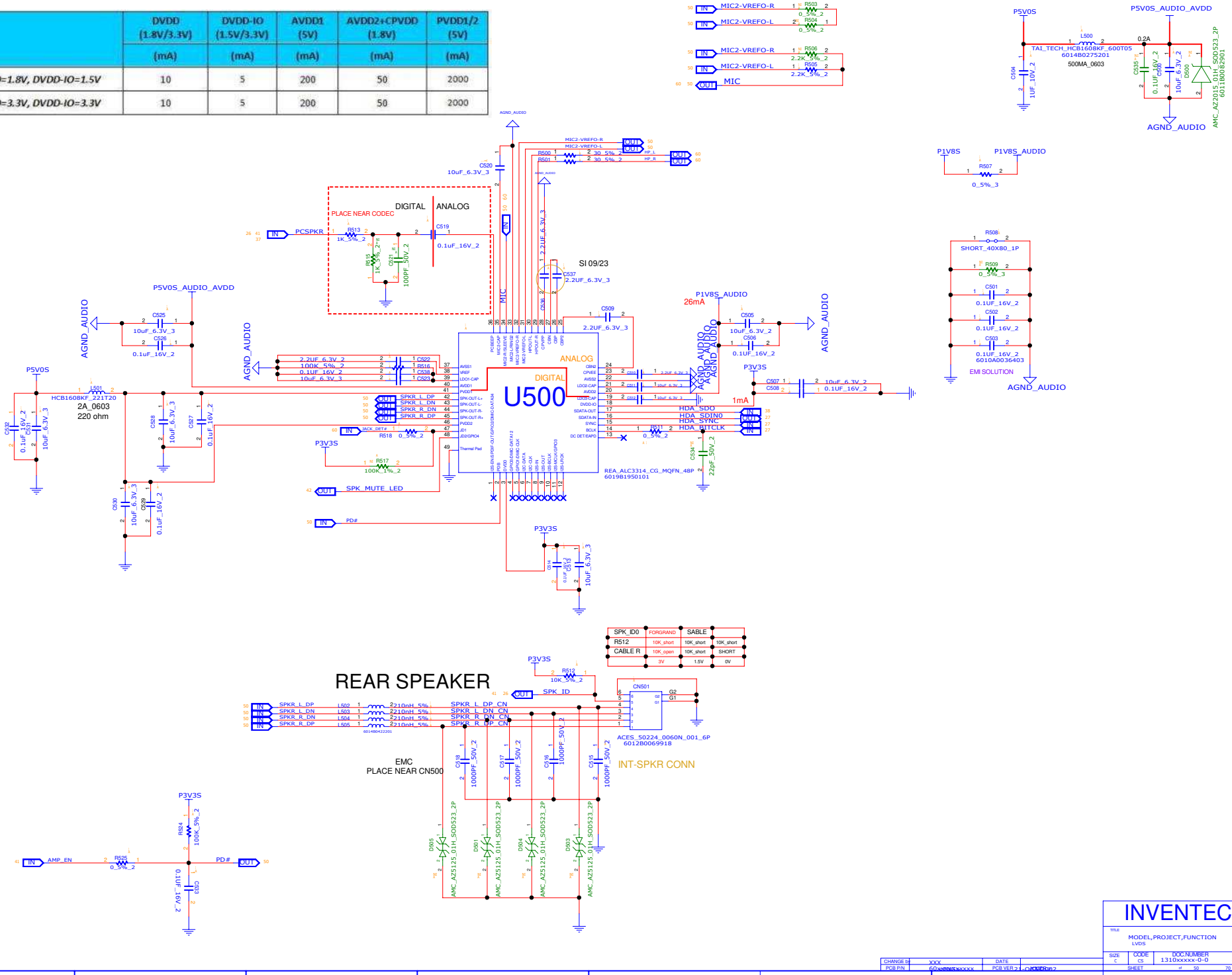
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

Audio Codec

		DVDD (1.8V/3.3V) (mA)	DVDD-IO (1.5V/3.3V) (mA)	AVDD1 (5V) (mA)	AVDD2+CPVDD (1.8V) (mA)	PVDD1/2 (5V) (mA)
1	*DVDD=1.8V, DVDD-IO=1.5V*	10	5	200	50	2000
2	*DVDD=3.3V, DVDD-IO=3.3V*	10	5	200	50	2000

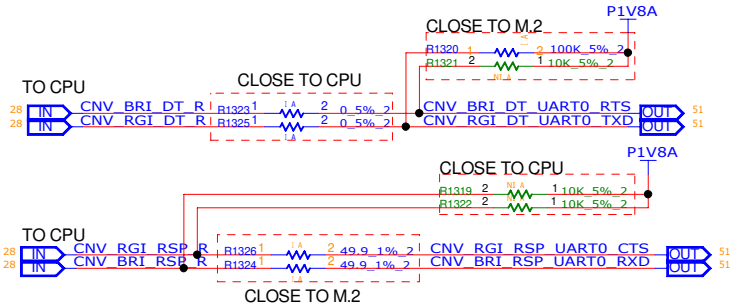


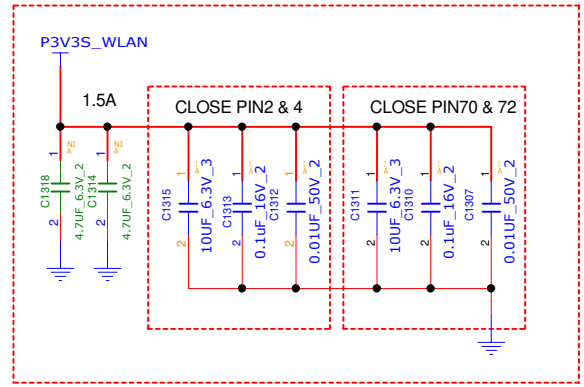
CNVI-WLAN
HYBRIDE-M.2E KEY

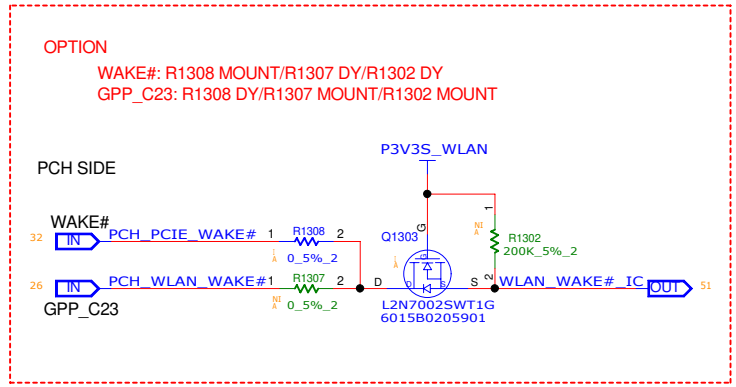
BRI / RGI damping resistor and PU placement :

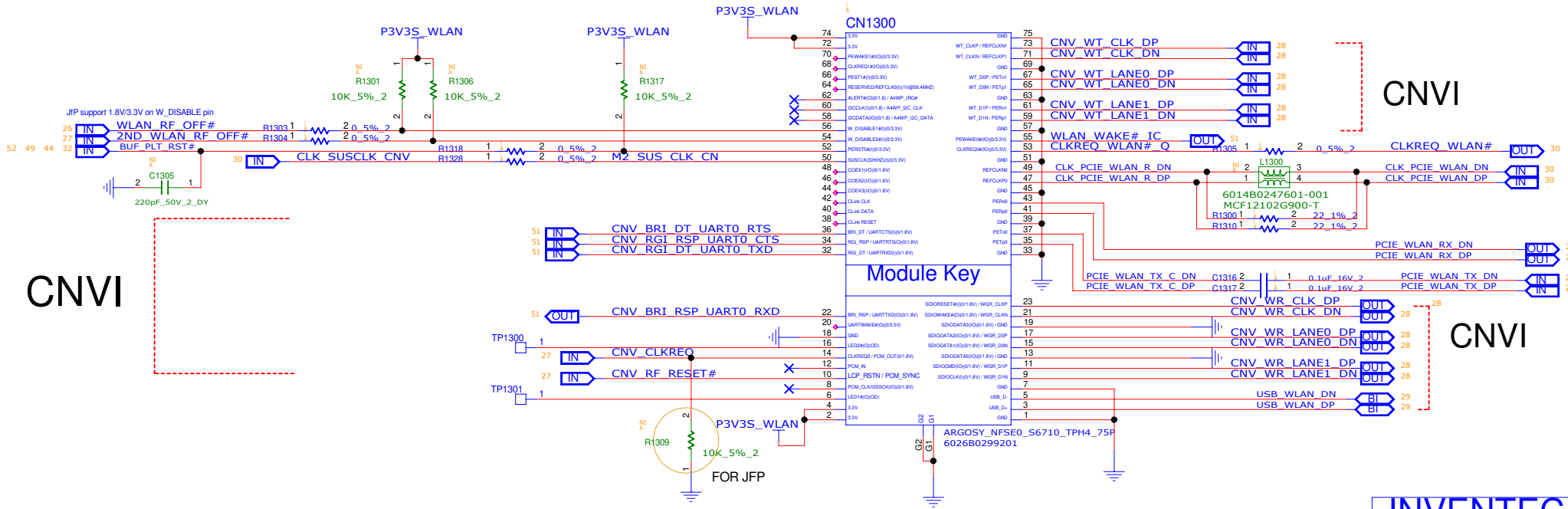
RGI_DT / BRI_DT damping resistor clsoe to the SoC/PCH ; PU close to the M.2.

RGI_RSP / BRI_RSP damping resistor clsoe to the M.2 ; PU close to SoC/PCH.









CHANGE by	XXX	DATE	
PCB P/N	60NSxxxxxxx	PCB VER	XX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
WLAN & BT

SIZE	CODE	DOC.NUMBER	REV
3	CS	1310xxxxx-0-0	X01

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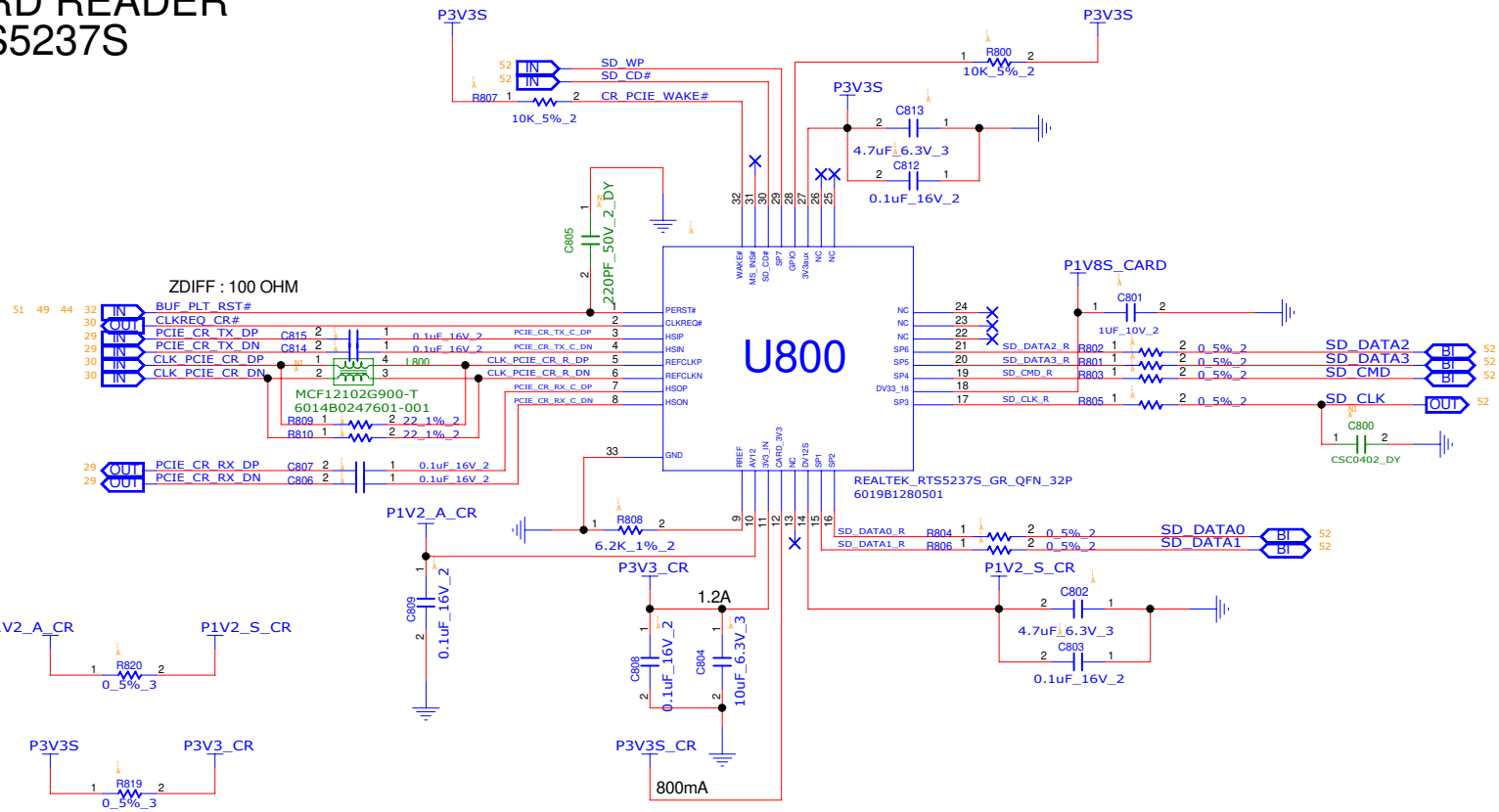
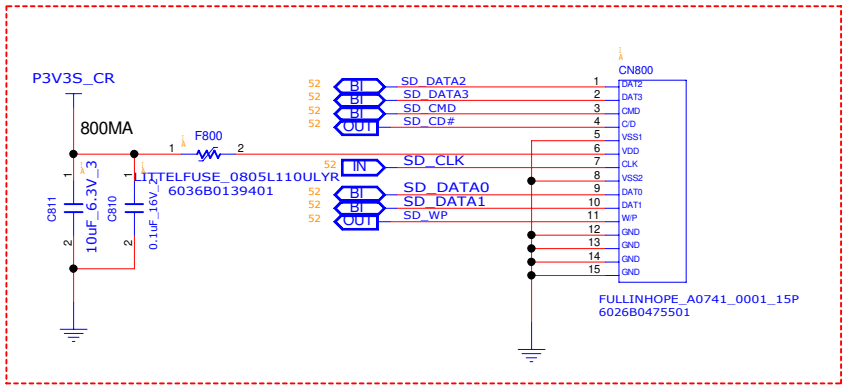
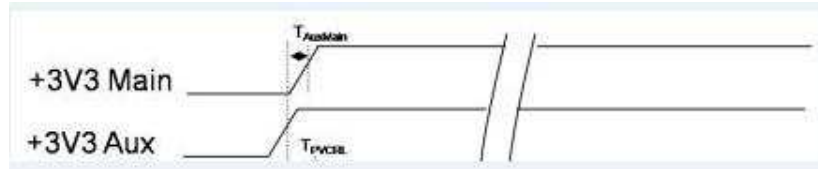
CARD READER
RTS5237S







Symbol	Description	Min.	Max.	Unit
TAUXMAIN	Power-on timing between AUX_PWR to MAIN_PWR	0	100	us

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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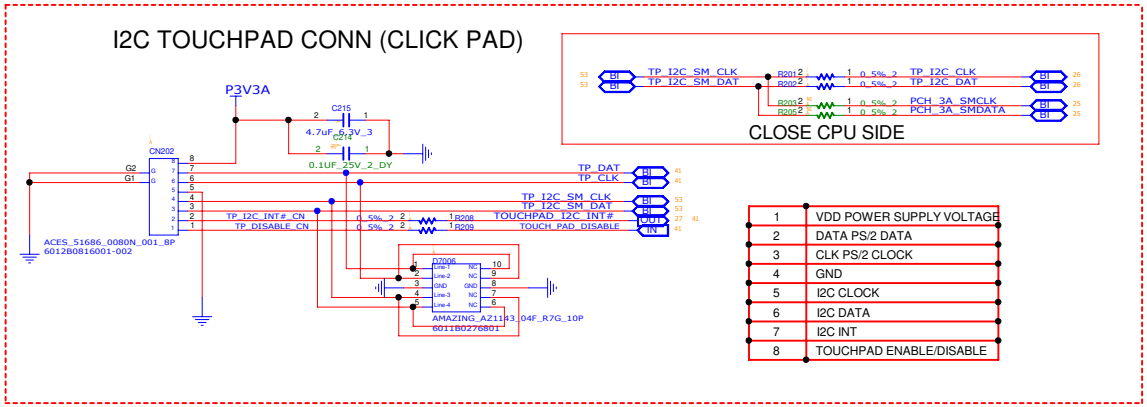
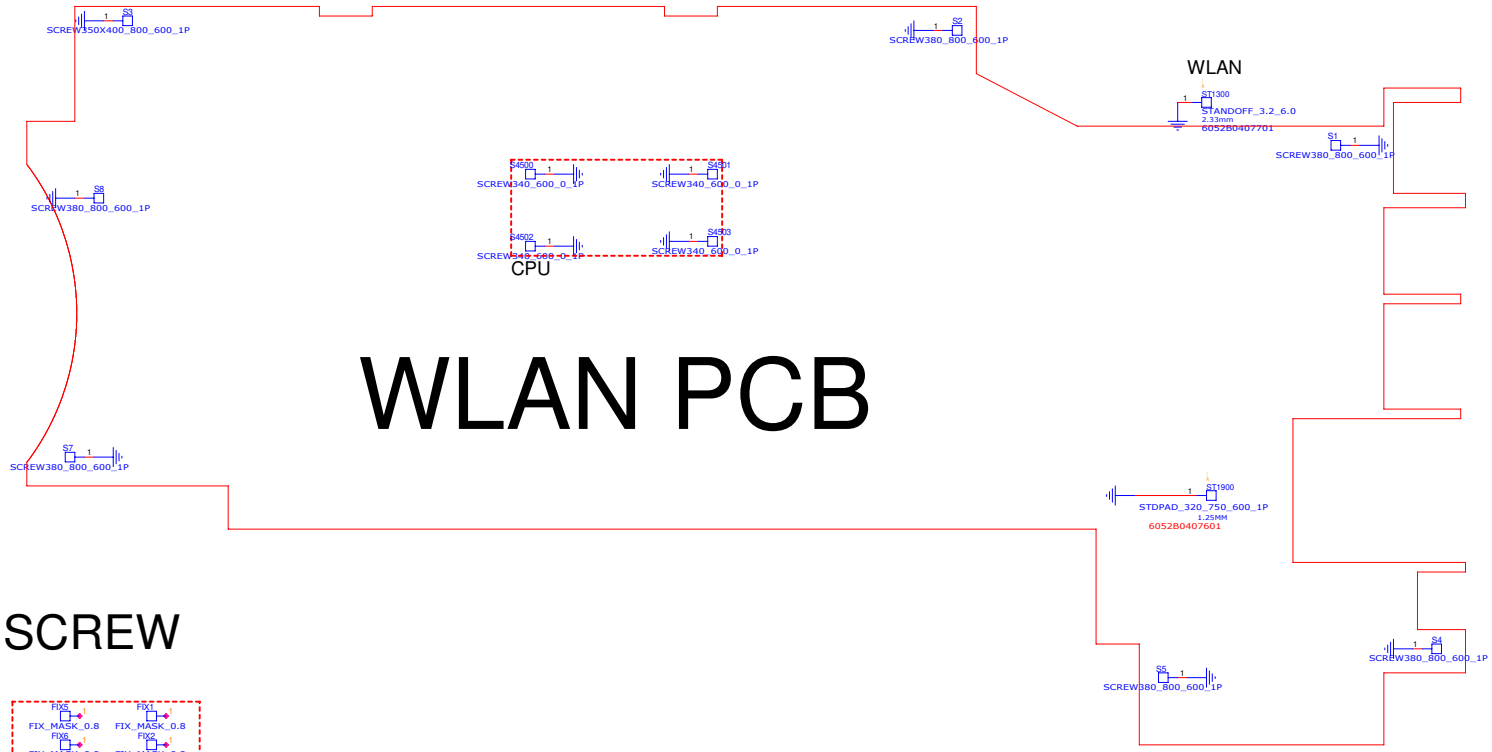
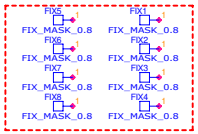
TOUCH PAD



1	VDD POWER SUPPLY VOLTAGE
2	DATA PS/2 DATA
3	CLK PS/2 CLOCK
4	GND
5	I2C CLOCK
6	I2C DATA
7	I2C INT
8	TOUCHPAD ENABLE/DISABLE



SCREW



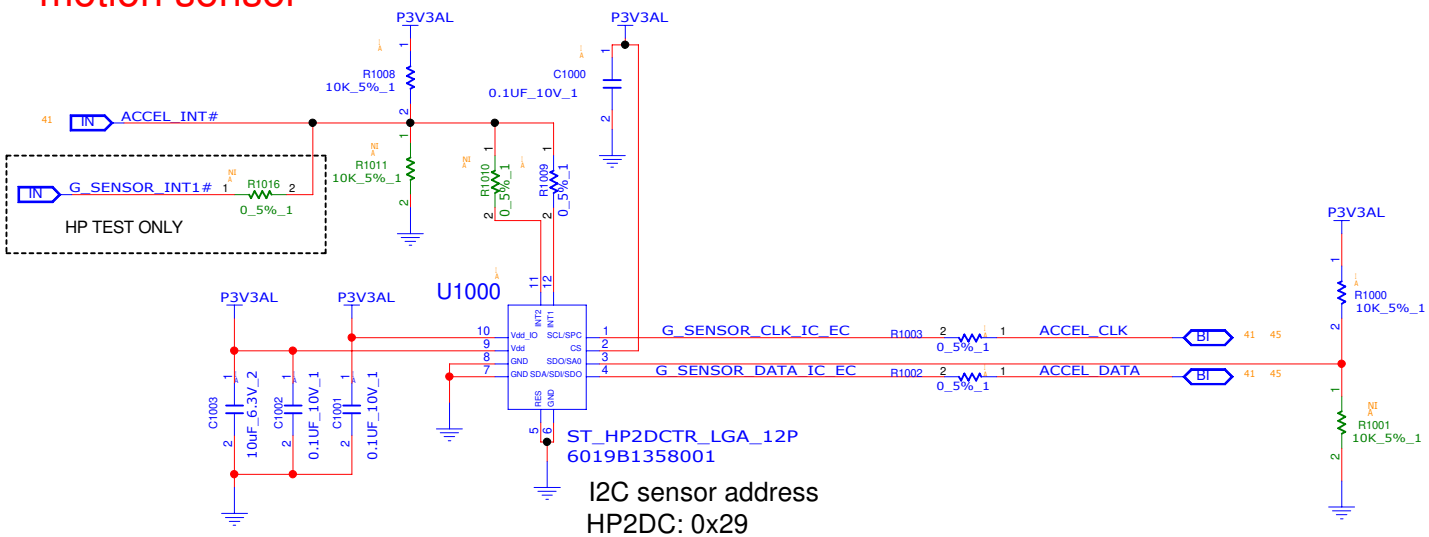
INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0			REV X01
SHEET 53 of 70					
CHANGE N	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

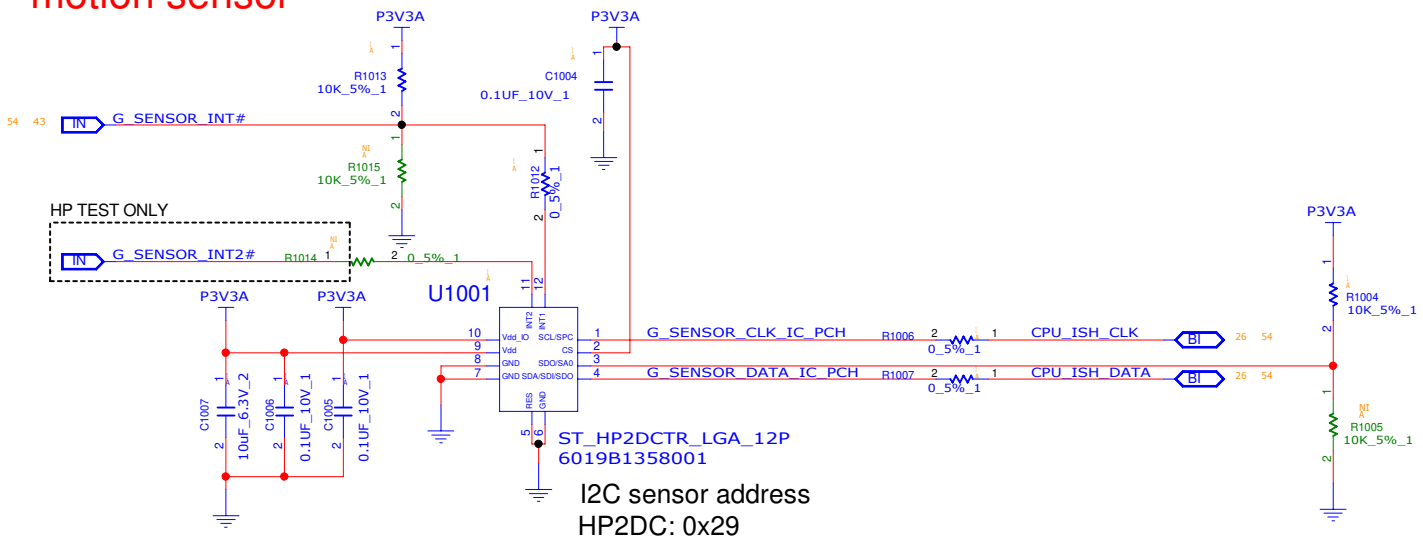
3-axis "femto" accelerometer
motion sensor

EC SIDE



3-axis "femto" accelerometer
motion sensor

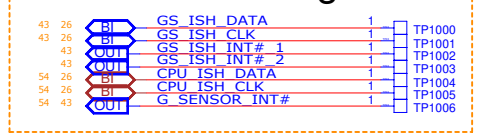
PCH SIDE



Applications

- Motion-activated functions
- Display orientation
- Shake control
- Pedometer
- Gaming and virtual reality input devices
- Impact recognition and logging

Sensor Debug Port

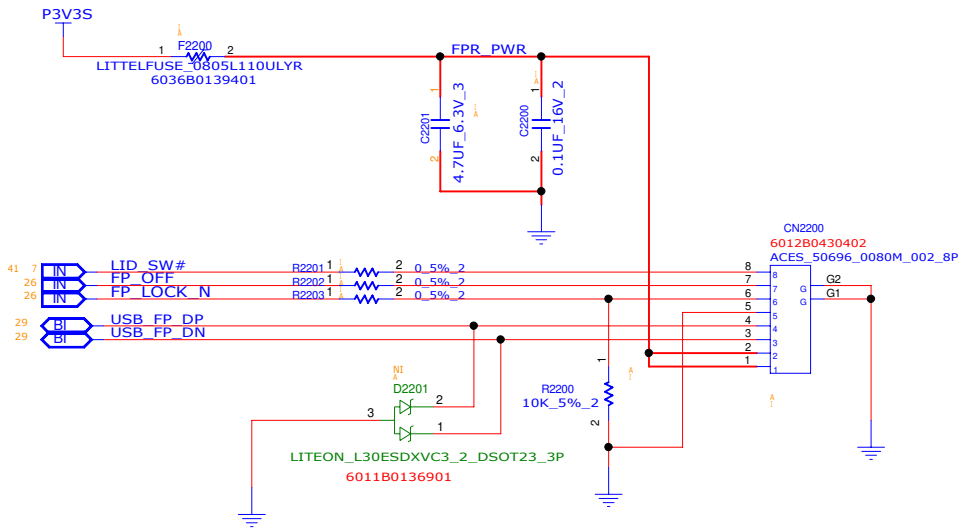


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION CAMERA		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 54 of 70			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

FINGER PRINTER



Pin Define	
PIN 1	3.3v
PIN 2	3.3V
PIN 3	D-
PIN 4	D+
PIN 5	GND
PIN 6	LOCK_N
PIN 7	FPR_OFF
PIN 8	Lid-Close

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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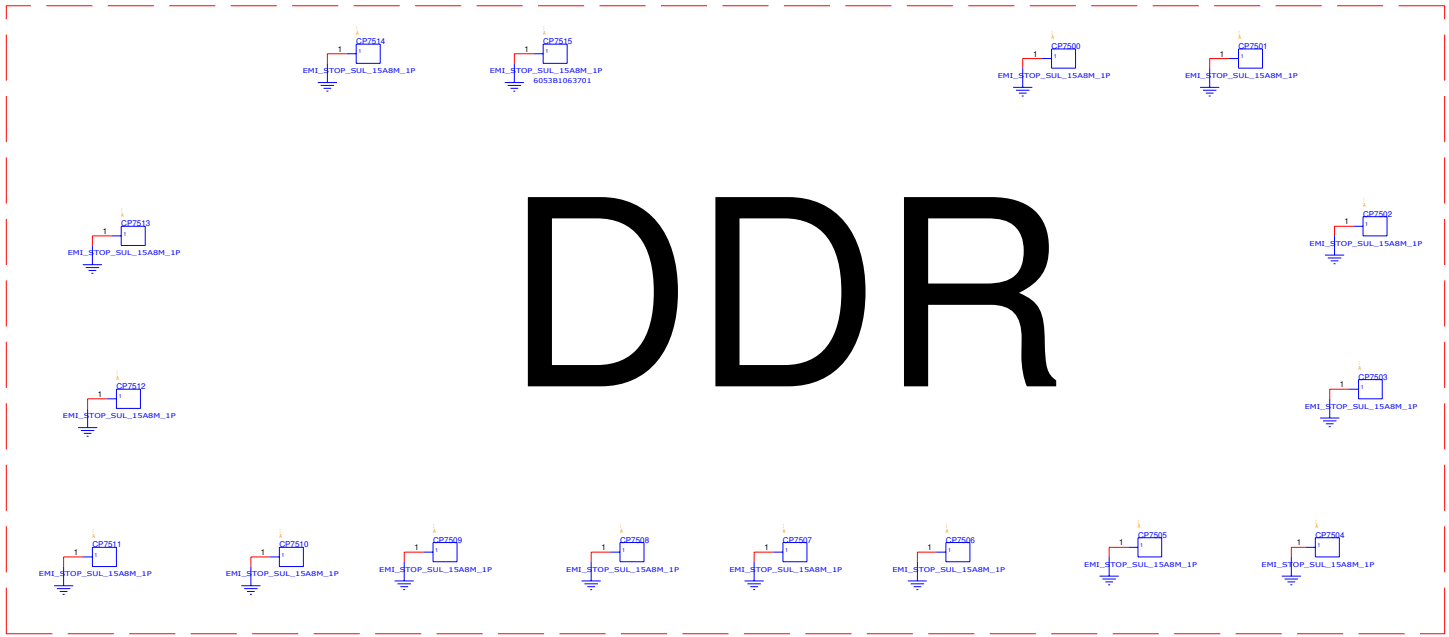
CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

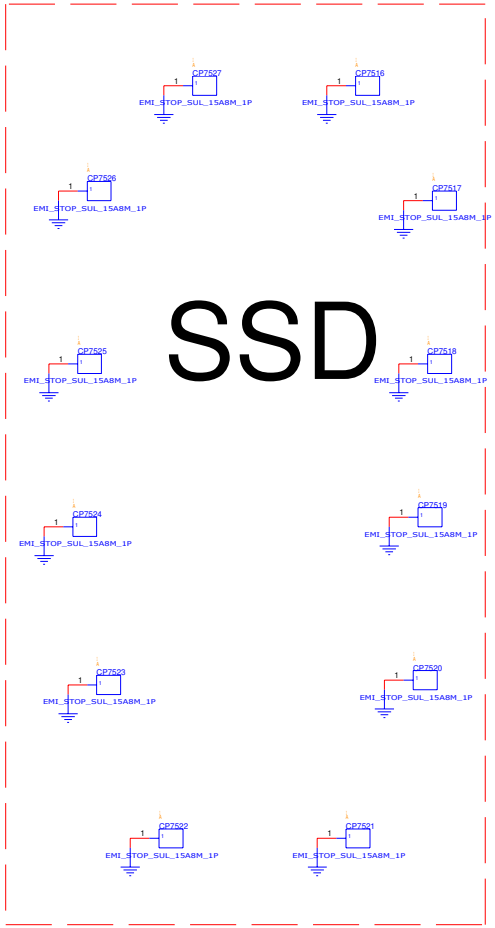
FINGER CLIP FOR MEMORY

6053B1063701

DDR

SSD





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

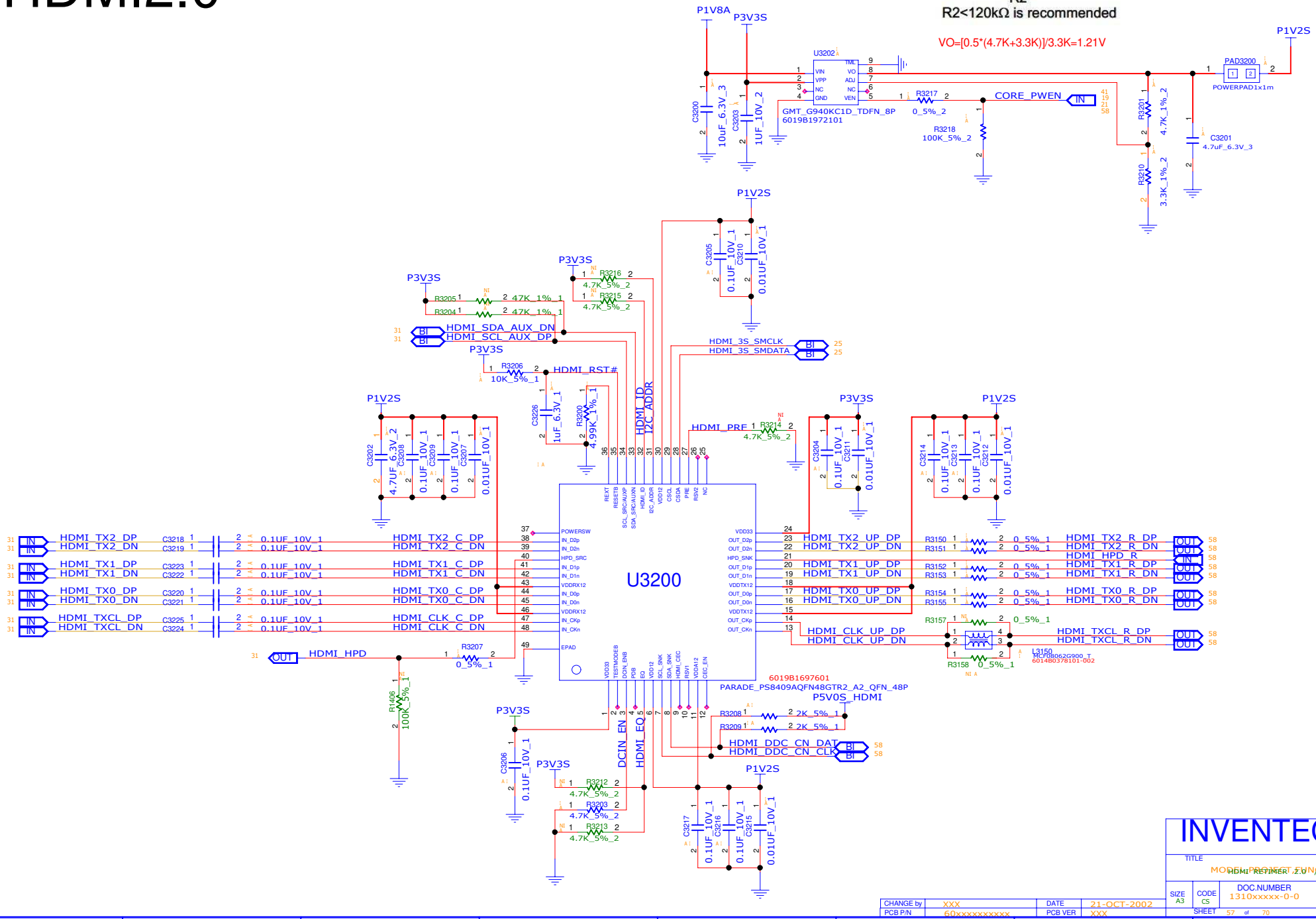
SHEET 56 of 70

HDMI2.0

$$VO = \frac{0.5\,(R1+R2)}{R2}\ \text{Volts}$$

R2<120kΩ is recommended

VO=[0.5*(4.7K+3.3K)]/3.3K=1.21V



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

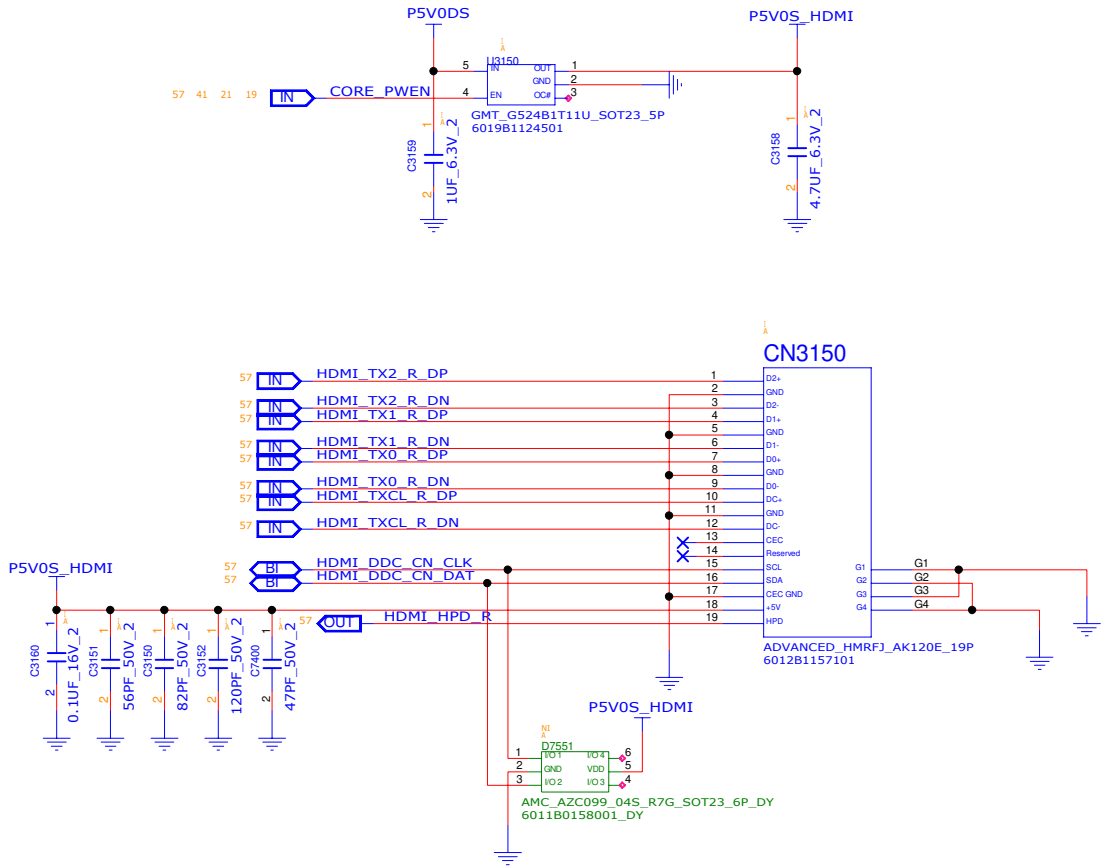
INVENTEC

TITLE: MODEL PROJECT FUNCTION — HDMI RETIMER 2.0 /CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 57 of 70

HDMI



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
HDMI CONN

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 58 of 70

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

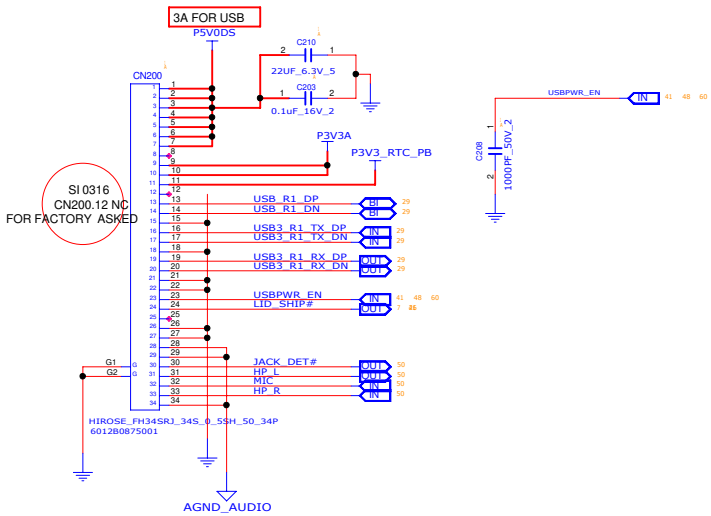
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

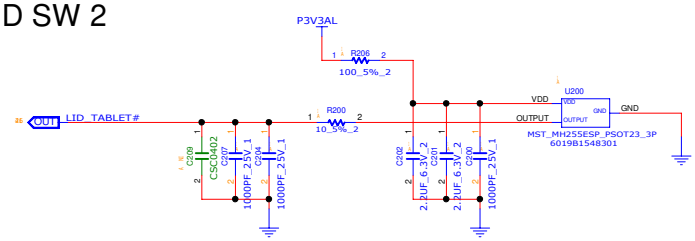
SHEET 59 of 70

MB TO USB AUDIO BOARD CONN

MB TO USB&AUDIO



LID SW 2



CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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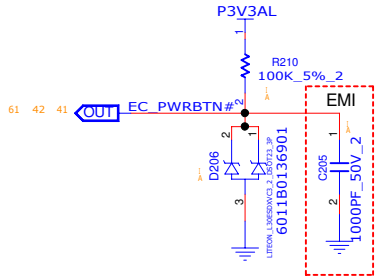
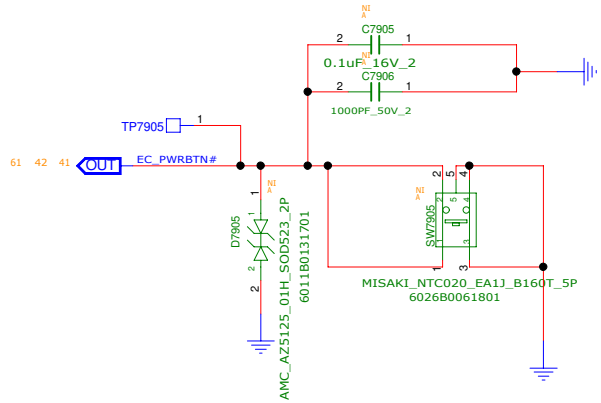
DEBUG PORT / ESPI DEBUG CNTR

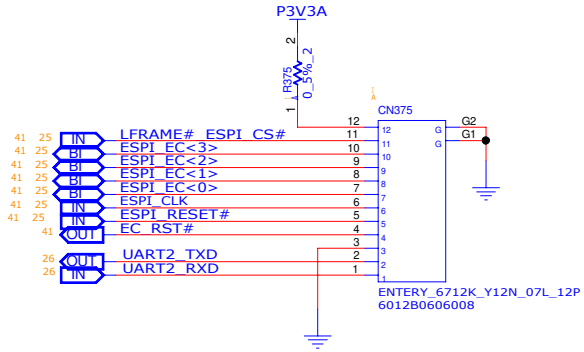
DEBUG PORT

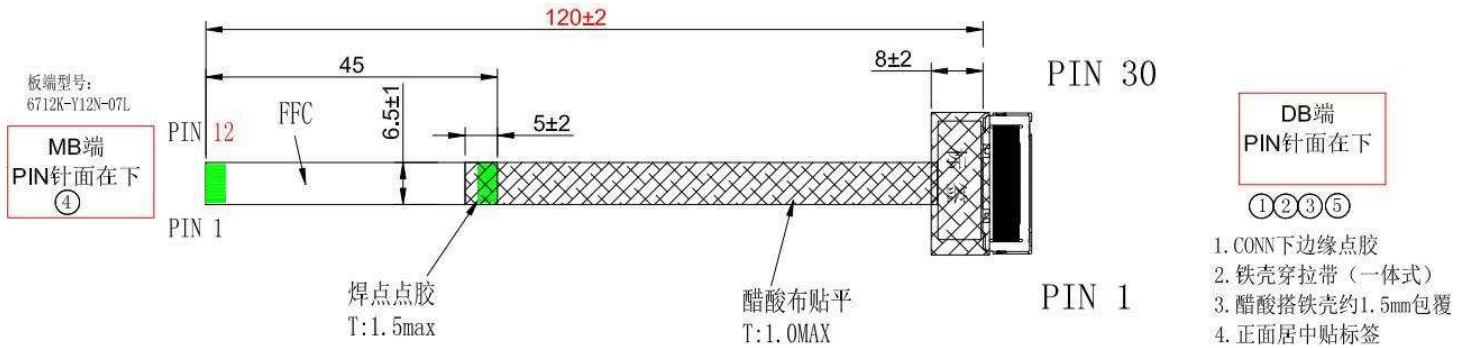
DB	MB	PIN DEFINE
22	1	P3V3A
6	2	LPC_FRAME_ESPI_CS
7	3	LPC_ESPI_IO<3>
8	4	LPC_ESPI_IO<2>
9	5	LPC_ESPI_IO<1>
10	6	LPC_ESPI_IO<0>
11	7	ESPI_CLK_33MHz
12	8	ESPI_RST_N
16	9	EC_RST#
3	10	DGND
28	11	UART_HEADER_TXD
29	12	UART_HEADER_RXD



TACK SWITCH







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

SMALL BOARD

DATE	CHANGE NO.	REV
21-OCT-2002		A

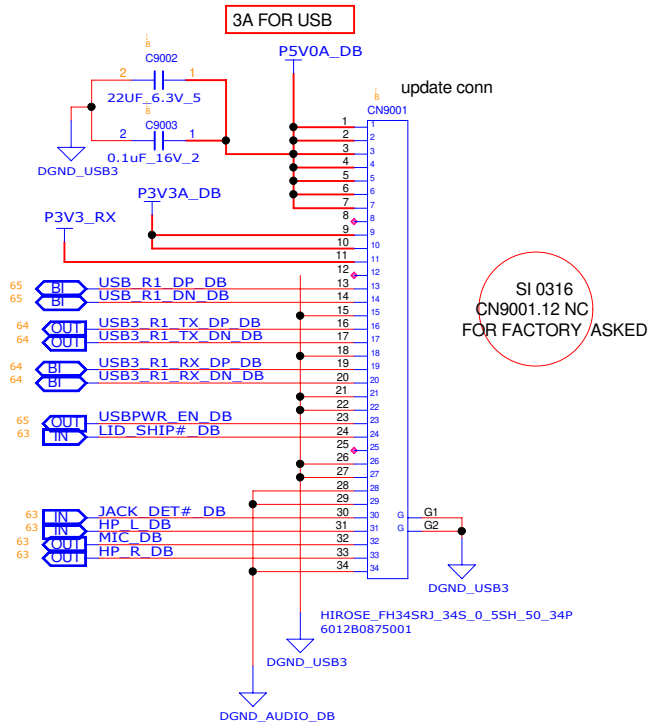
DESIGN / DRAWER	SEB CHANG	DATE	21-OCT-2002
CHECK	SEB CHANG		
APPROVAL	CHO ADAM		
FILE NAME	W:\WINCE\TOUCH SCREEN BPARD		
PCB P/N	50xxxxxxxxxx	PCB VER	XXX

INVENTEC

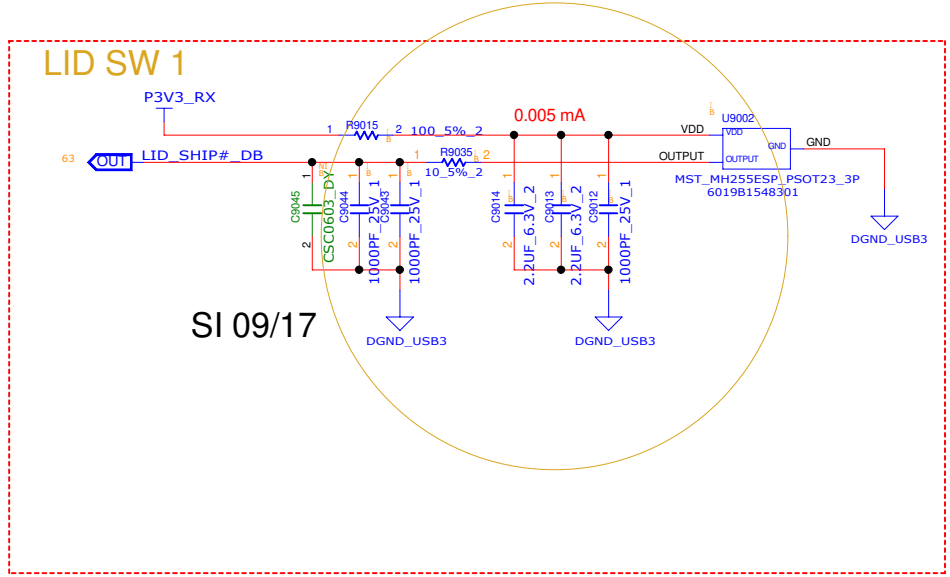
TITLE	MODEL,PROJECT,FUNCTION		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 62 of 70			

USB BOARD

VER.09_20171109
LOCATION: 9000~9200

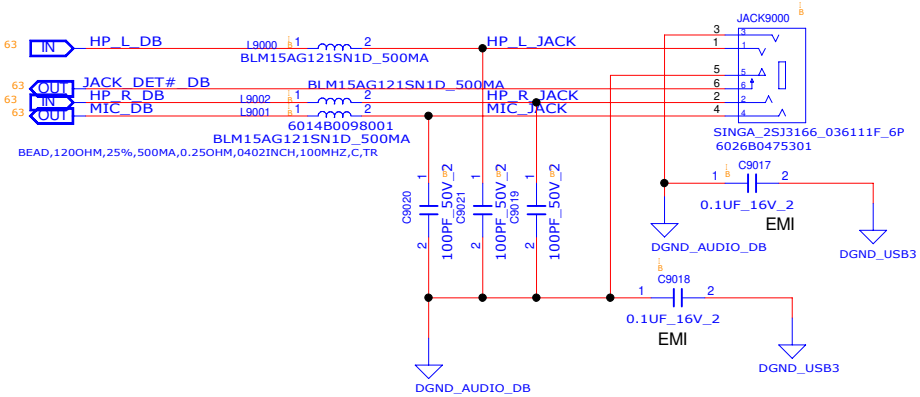


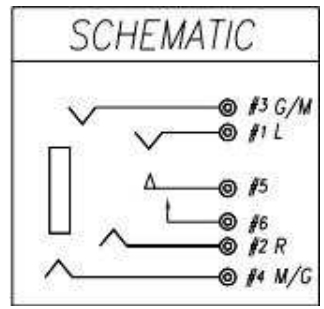
SI 0316
CN9001.12 NC
FOR FACTORY ASKED



SI 09/17

COMBO JACK





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

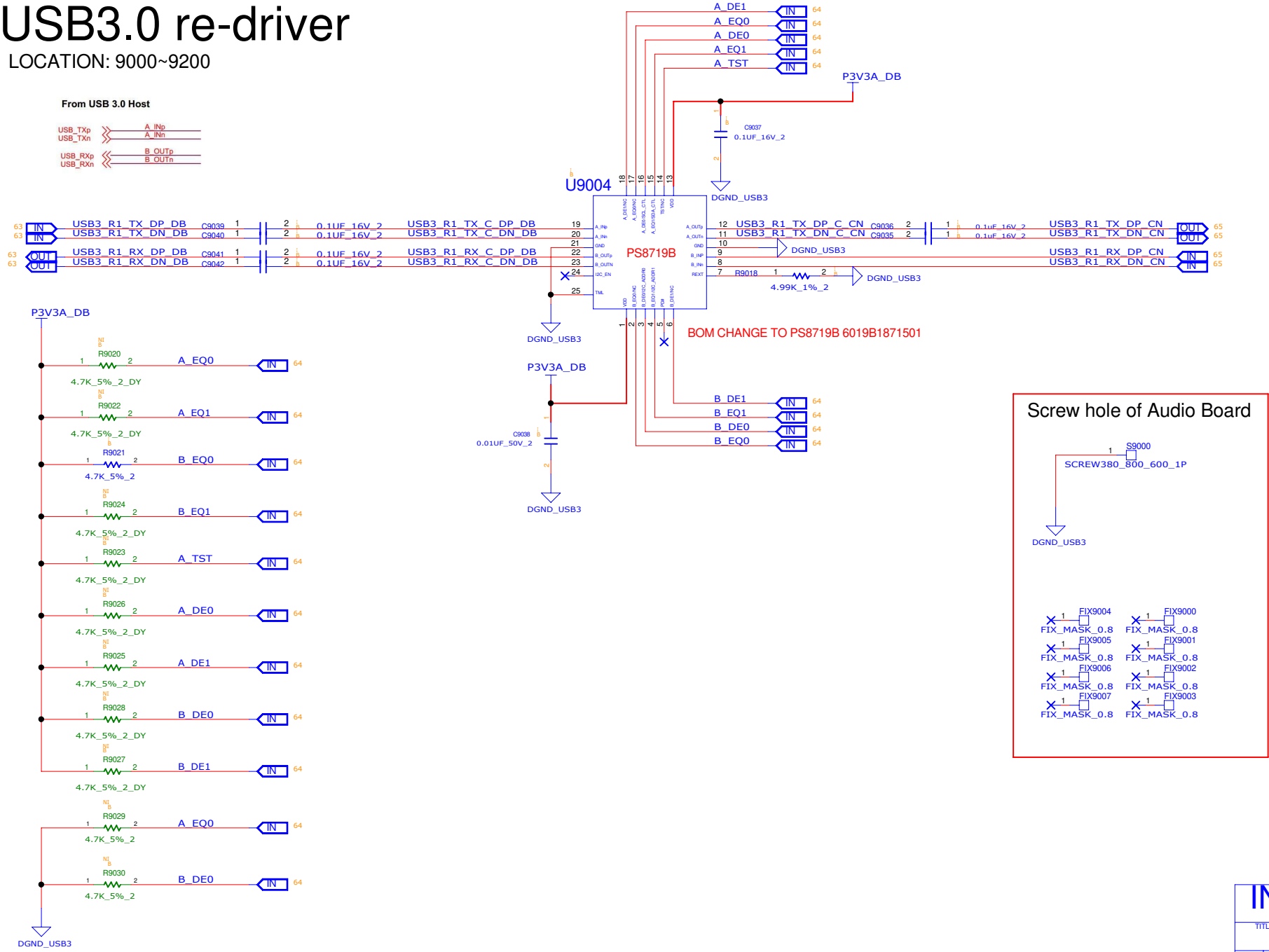
SHEET of 63 70

CHANGE by	XXX	DATE	
PCB P/N	60.NSxxxxxxxx	PCB VER	XX

OCT-2002

USB3.0 re-driver

LOCATION: 9000~9200



Screw hole of Audio Board

INVENTEC

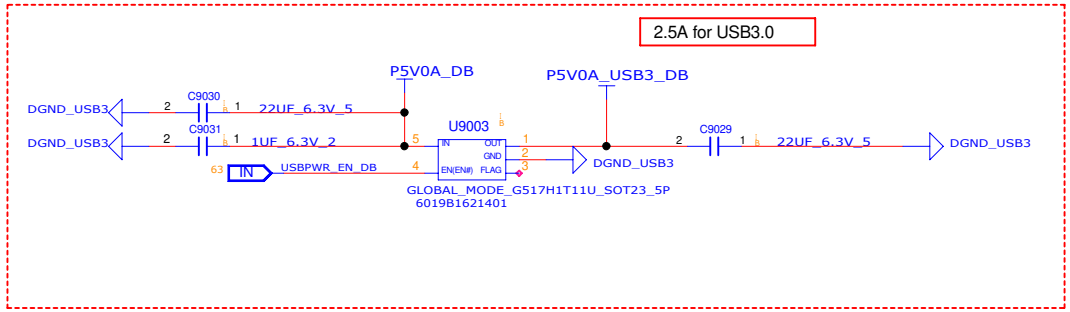
TITLE	MODEL,PROJECT,FUNCTION USB 3.0 CONN & M/B TO D/B CONN		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET of 64 70			

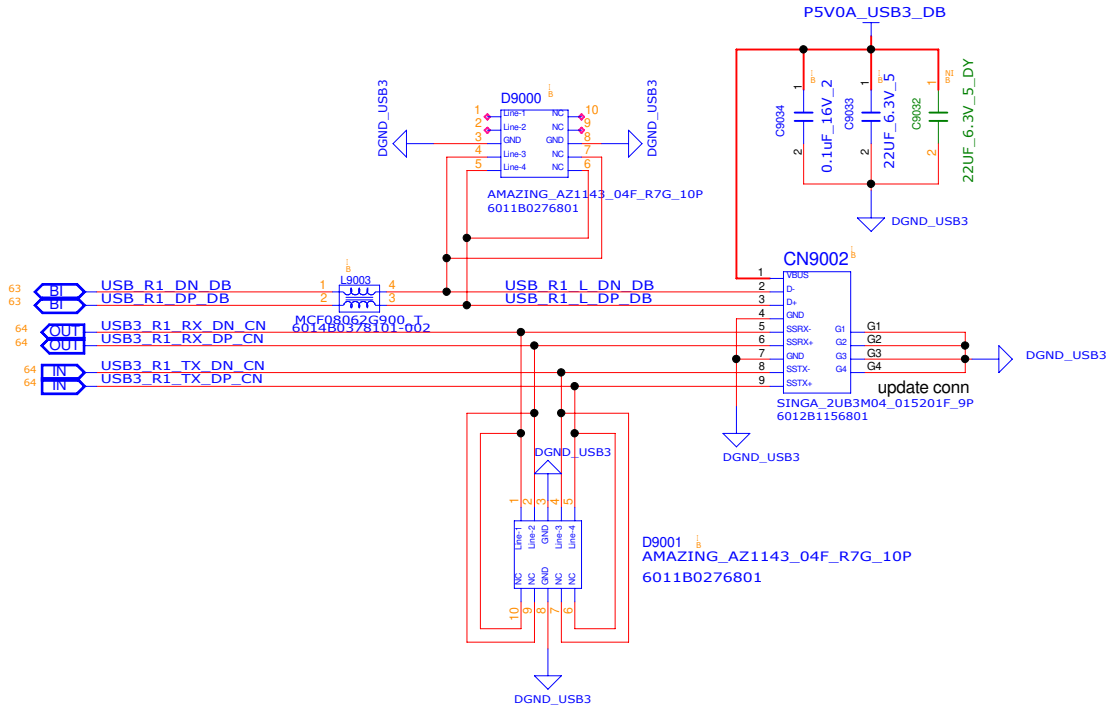
CHANGE by	XXX	DATE	
PCB P/N	60NSxxxxxxx	PCB VER	XX DCT-2002

USB3.0

LOCATION 2400~2499

LOCATION: 9000~9200





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

CHANGE by	XXX	DATE	
PCB P/N	60NS6xxxxxxx	PCB VER	X01

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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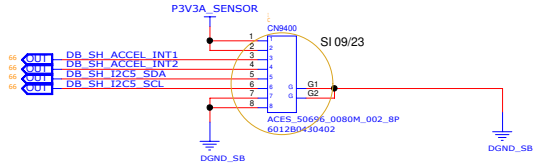
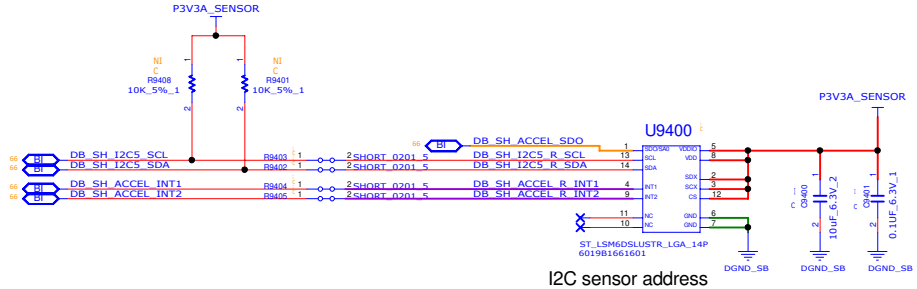
G-Sensor Board

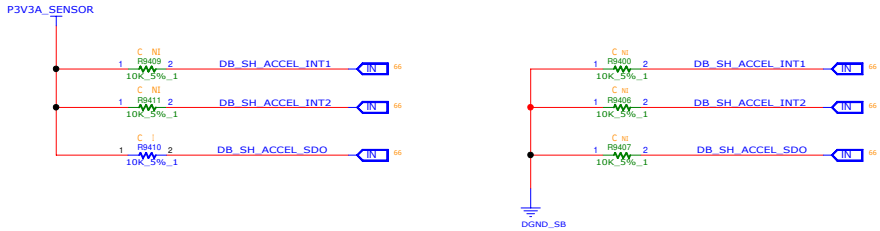
REFERENCE NUMBER:9400~9499

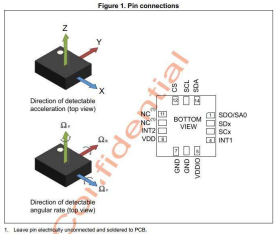
I = Monut
NI = No Monut

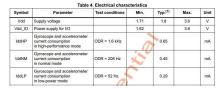




I2C sensor address
LSM6DSL: 0x6b





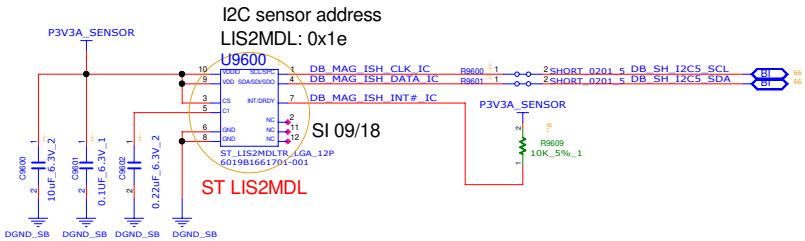


LSM6DSLUS
6D orientation
always-on 3D accelerometer and 3D gyroscope

3-axis magnetometer

magnetic sensor

I = Monut
NI = No Monut



Applications

- Tilt-compensated compasses
- Map rotation
- Intelligent power saving for handheld devices
- Gaming and virtual reality input devices

Base on Balos schematic , the I2C slave address is as following.
LIS2MDL: 0x1e
HP2DC: 0x29
LSM6DSL: 0x6b

CHANGE N	XXX	DATE	
PCB P/N	60.xxxxx.xxxx	PCB VER	XXXRev

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
LVDS

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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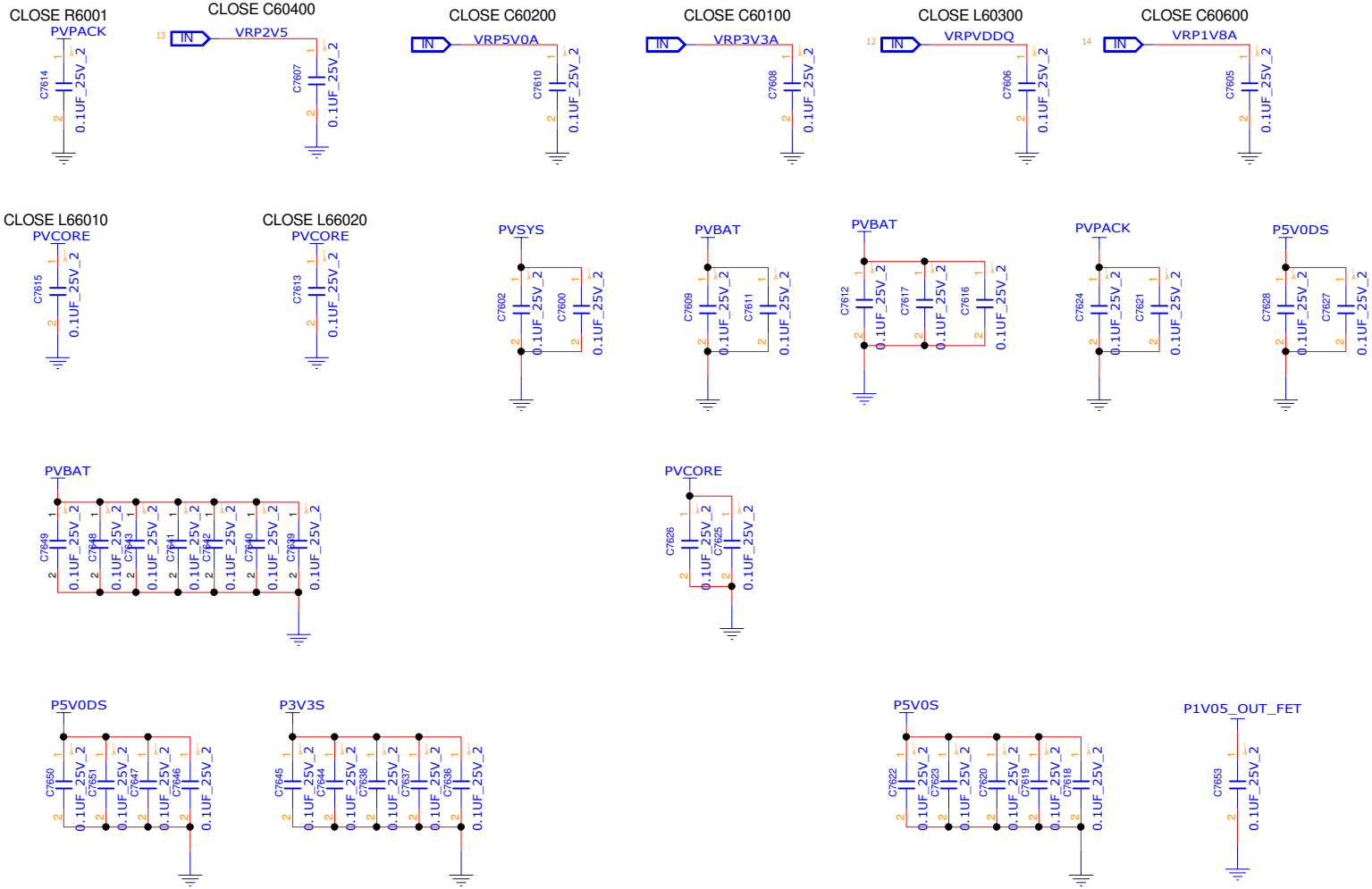
EMI SOLUTION



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

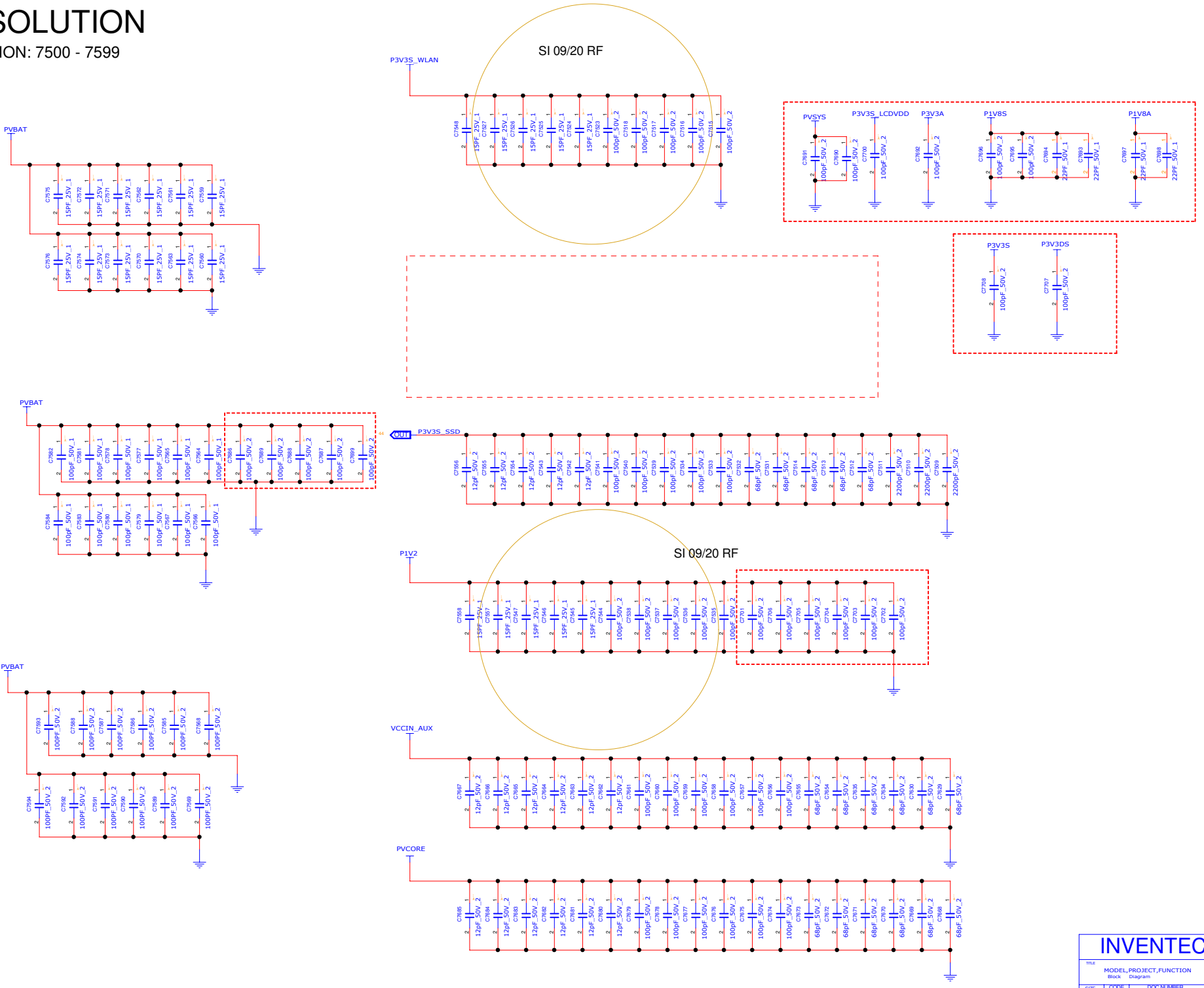
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 67 of 70

RF SOLUTION

LOCATION: 7500 - 7599



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	50xxxxxxxxxx	PCB VER	XXX

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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8	7	6	5	4	3	2	1

D C B A

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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8 7 6 5 4 3 2 1