MS-7D15

ATX

Ver: 1.0/2.0

Intel -RKL-S plamform

CPU:

RKL- S 125W

PWM:

RAA229001

Onboard Chip:

HD Audio Codec:ALC897
Dual LAN- RTL8125B/i219
SIO:NTC6687
Flash ROM: SPI 128 MB X1

System Chipset:

B560 PCH_H

Display Output:

HDMI Port

DP Port

Main Memory:

*DDRIV (2933MHz) * 4 (Dual Channel)*

ACPI:

LDO

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 1*
*M.2 Slot * 3*

msi MICRO-STAR INT'L CO.,LTD.

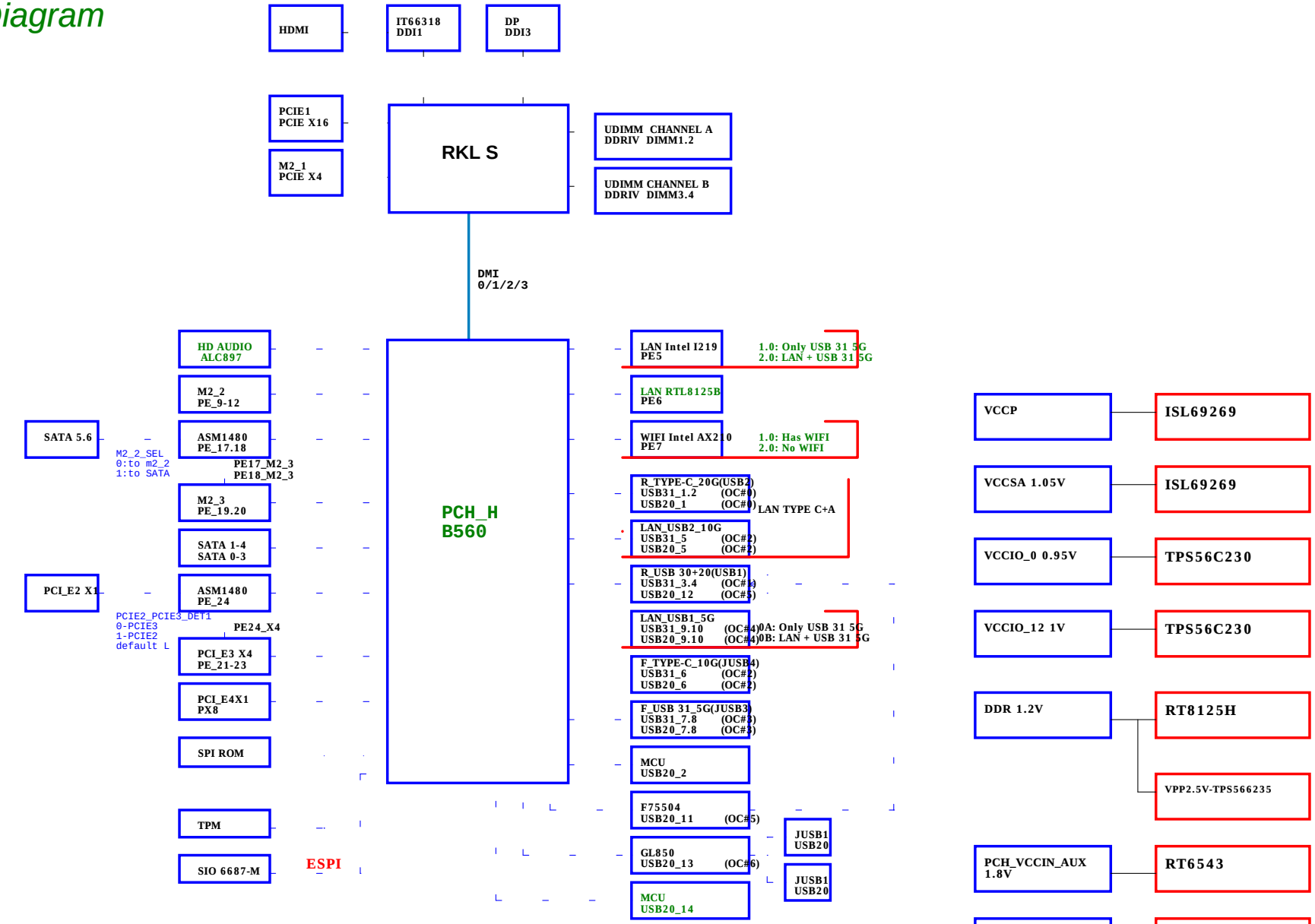
Title: Cover Sheet

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 Sheet 1 of 76

MS-7D15 Block Diagram

SMBUS ADRESS:
VCORE PWM:0X60
MCU:0X52
3933:0X20;0X26
DIMM_A0:WRITE 0XA0; READ 0XA1
DIMM_A1:WRITE 0XA2; READ 0XA3
DIMM_B0:WRITE 0XA4; READ 0XA5
DIMM_B1:WRITE 0XA6; READ 0XA7



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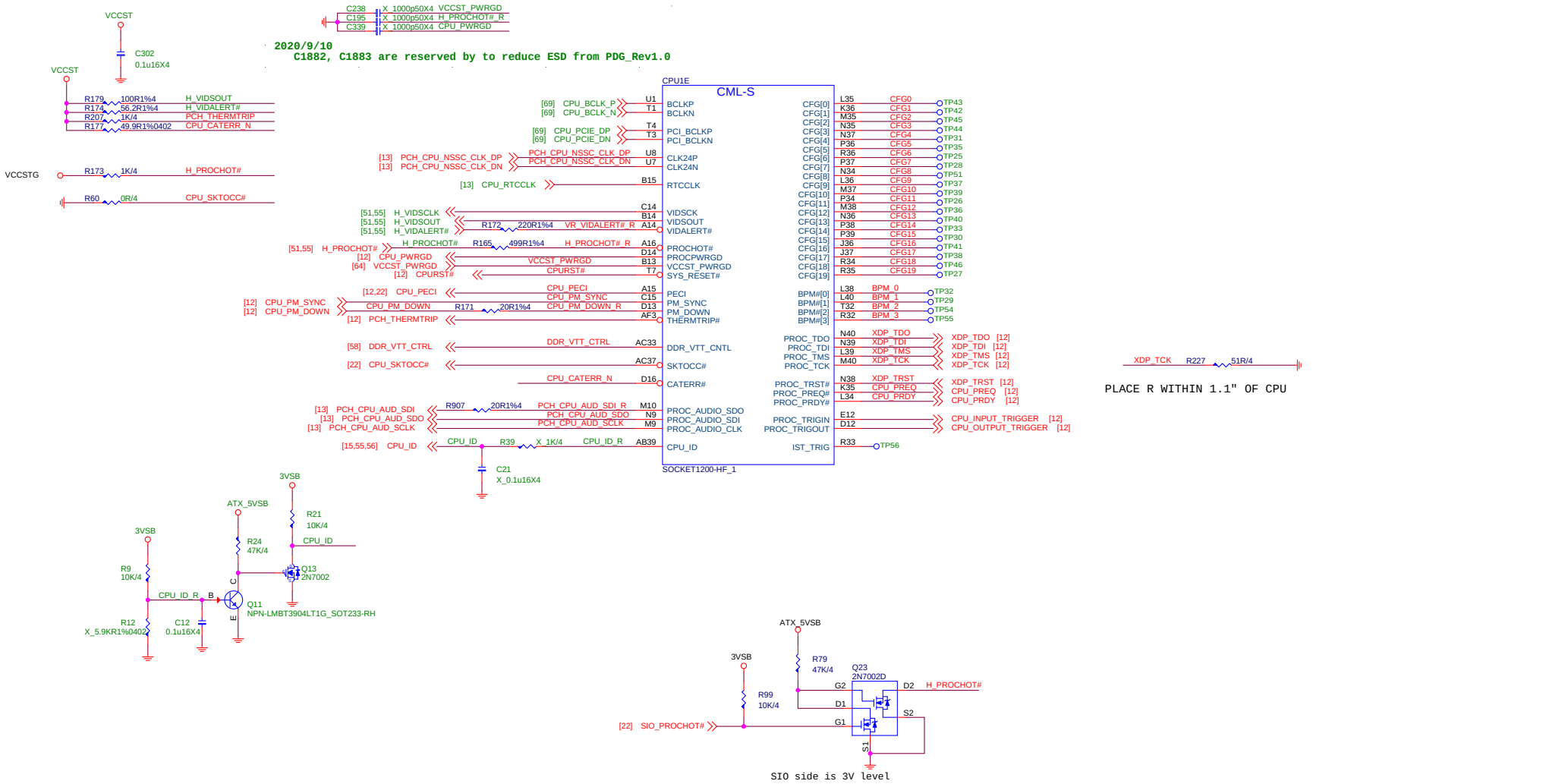
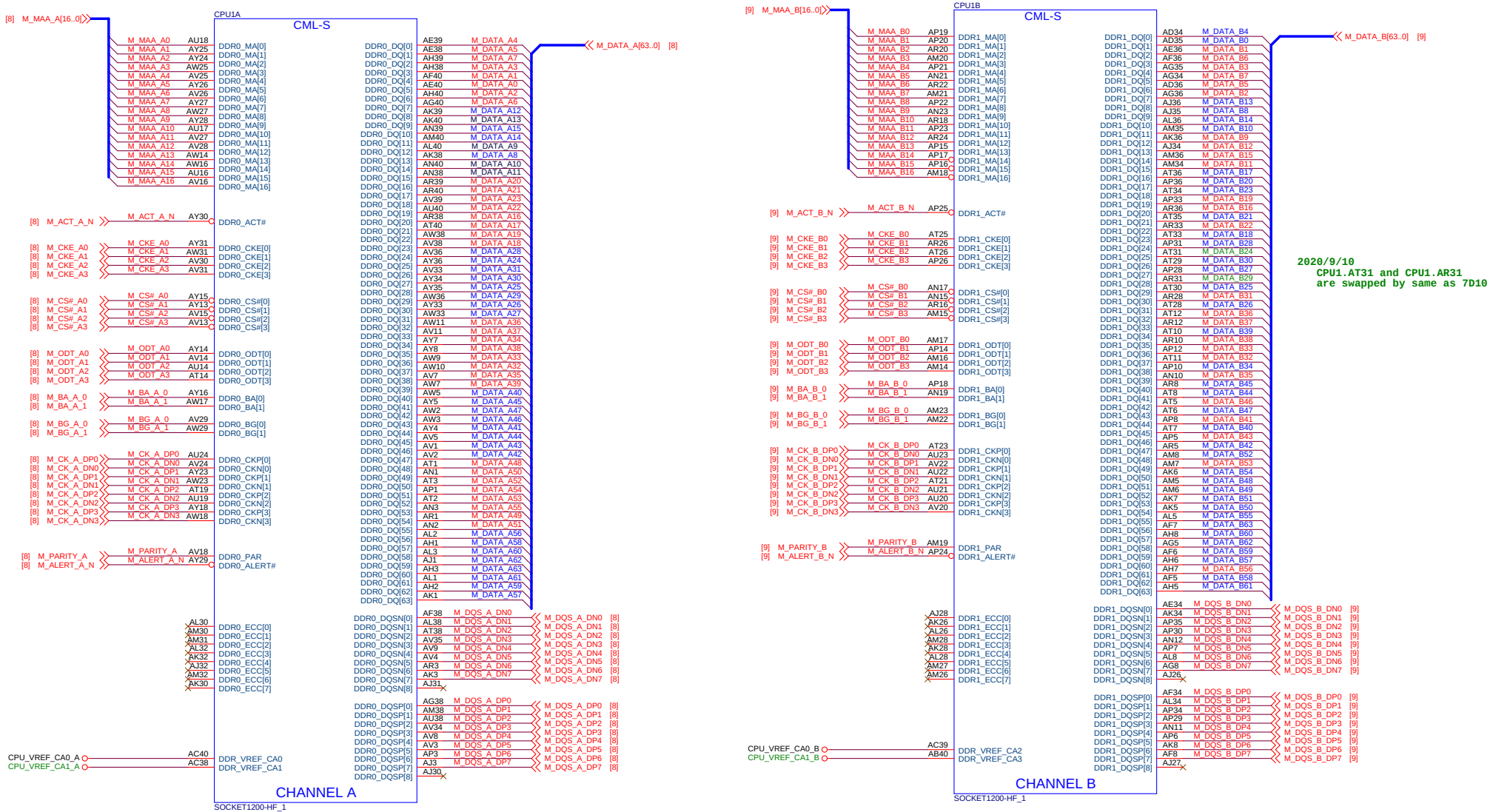
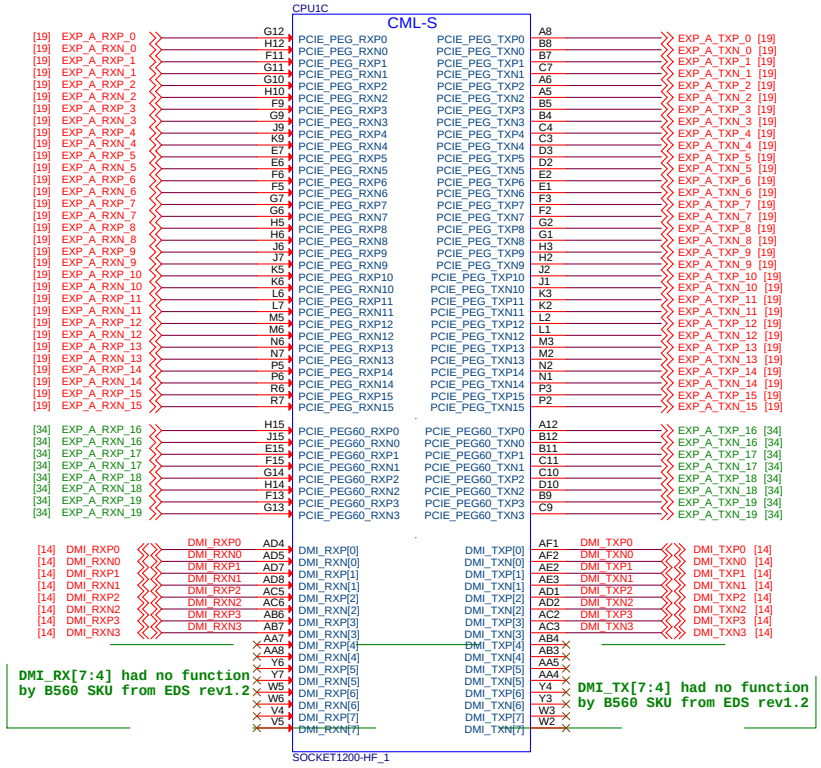
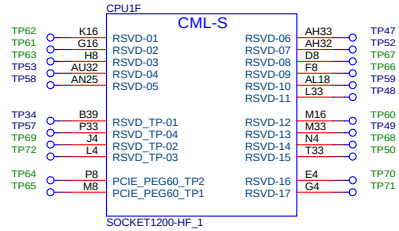
Title	Block Diagram	
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 2 of 76	

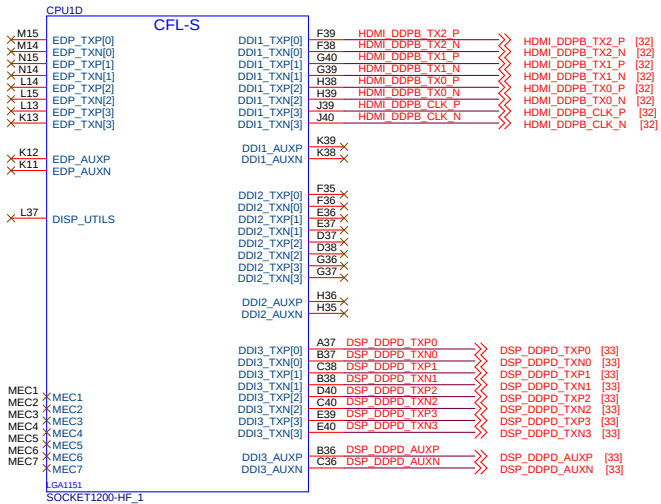


MSI	MICRO-STAR INT'L CO.,LTD.	
Title	CPU-Control/MISC/CFG	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 3 of 76	


CPU1A
CML-S
[8] M_MAA_A[16..0]
M_MAA_A0 AU18
M_MAA_A1 AY25
M_MAA_A2 AY24
M_MAA_A3 AW25
M_MAA_A4 AY25
M_MAA_A5 AY26
M_MAA_A6 AY26
M_MAA_A7 AY27
M_MAA_A8 AW27
M_MAA_A9 AY28
M_MAA_A10 AU17
M_MAA_A11 AY27
M_MAA_A12 AY28
M_MAA_A13 AW14
M_MAA_A14 AW16
M_MAA_A15 AU16
M_MAA_A16 AV16
DDR0_MA[0]
DDR0_MA[1]
DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]
DDR0_MA[6]
DDR0_MA[7]
DDR0_MA[8]
DDR0_MA[9]
DDR0_MA[10]
DDR0_MA[11]
DDR0_MA[12]
DDR0_MA[13]
DDR0_MA[14]
DDR0_MA[15]
DDR0_MA[16]
[8] M_ACT_A_N
M_ACT_A_N AY30
DDR0_ACT#
[8] M_CKE_A0
[8] M_CKE_A1
[8] M_CKE_A2
[8] M_CKE_A3
M_CKE_A0 AY31
M_CKE_A1 AW31
M_CKE_A2 AY30
M_CKE_A3 AY31
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
[8] M_CS#_A0
[8] M_CS#_A1
[8] M_CS#_A2
[8] M_CS#_A3
M_CS#_A0 AY15
M_CS#_A1 AY13
M_CS#_A2 AW15
M_CS#_A3 AV13
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
[8] M_ODT_A0
[8] M_ODT_A1
[8] M_ODT_A2
[8] M_ODT_A3
M_ODT_A0 AY14
M_ODT_A1 AW14
M_ODT_A2 AU14
M_ODT_A3 AT14
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
[8] M_BA_A_0
[8] M_BA_A_1
M_BA_A_0 AY16
M_BA_A_1 AW17
DDR0_BA[0]
DDR0_BA[1]
[8] M_BG_A_0
[8] M_BG_A_1
M_BG_A_0 AV29
M_BG_A_1 AW29
DDR0_BG[0]
DDR0_BG[1]
[8] M_CK_A_DP0
[8] M_CK_A_DN0
[8] M_CK_A_DP1
[8] M_CK_A_DN1
[8] M_CK_A_DP2
[8] M_CK_A_DN2
[8] M_CK_A_DP3
[8] M_CK_A_DN3
M_CK_A_DP0 AU24
M_CK_A_DN0 AV24
M_CK_A_DP1 AY23
M_CK_A_DN1 AW23
M_CK_A_DP2 AT19
M_CK_A_DN2 AU19
M_CK_A_DP3 AY18
M_CK_A_DN3 AW18
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
[8] M_PARITY_A
[8] M_ALERT_A_N
M_PARITY_A AV18
M_ALERT_A_N AY29
DDR0_PAR
DDR0_ALERT#
AL30
AM30
AM31
AL32
AK32
AJ32
AM32
AK30
DDR0_ECC[0]
DDR0_ECC[1]
DDR0_ECC[2]
DDR0_ECC[3]
DDR0_ECC[4]
DDR0_ECC[5]
DDR0_ECC[6]
DDR0_ECC[7]
CPU_VREF_CA0_A
CPU_VREF_CA1_A
AC40
AC38
DDR_VREF_CA0
DDR_VREF_CA1
DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]
DDR0_DQ[17]
DDR0_DQ[18]
DDR0_DQ[19]
DDR0_DQ[20]
DDR0_DQ[21]
DDR0_DQ[22]
DDR0_DQ[23]
DDR0_DQ[24]
DDR0_DQ[25]
DDR0_DQ[26]
DDR0_DQ[27]
DDR0_DQ[28]
DDR0_DQ[29]
DDR0_DQ[30]
DDR0_DQ[31]
DDR0_DQ[32]
DDR0_DQ[33]
DDR0_DQ[34]
DDR0_DQ[35]
DDR0_DQ[36]
DDR0_DQ[37]
DDR0_DQ[38]
DDR0_DQ[39]
DDR0_DQ[40]
DDR0_DQ[41]
DDR0_DQ[42]
DDR0_DQ[43]
DDR0_DQ[44]
DDR0_DQ[45]
DDR0_DQ[46]
DDR0_DQ[47]
DDR0_DQ[48]
DDR0_DQ[49]
DDR0_DQ[50]
DDR0_DQ[51]
DDR0_DQ[52]
DDR0_DQ[53]
DDR0_DQ[54]
DDR0_DQ[55]
DDR0_DQ[56]
DDR0_DQ[57]
DDR0_DQ[58]
DDR0_DQ[59]
DDR0_DQ[60]
DDR0_DQ[61]
DDR0_DQ[62]
DDR0_DQ[63]
AE39 M_DATA_A4
AE38 M_DATA_A5
AH39 M_DATA_A7
AH38 M_DATA_A3
AF40 M_DATA_A1
AE40 M_DATA_A0
AH40 M_DATA_A2
AG40 M_DATA_A6
AK39 M_DATA_A12
AK40 M_DATA_A13
AN39 M_DATA_A15
AM40 M_DATA_A14
AL40 M_DATA_A9
AK38 M_DATA_A8
AN40 M_DATA_A10
AN38 M_DATA_A11
AR39 M_DATA_A20
AR40 M_DATA_A21
AV39 M_DATA_A23
AU40 M_DATA_A22
AR38 M_DATA_A16
AT40 M_DATA_A17
AW38 M_DATA_A19
AV38 M_DATA_A18
AV36 M_DATA_A28
AY36 M_DATA_A24
AV33 M_DATA_A31
AY34 M_DATA_A30
AY35 M_DATA_A25
AW36 M_DATA_A29
AY33 M_DATA_A26
AW33 M_DATA_A27
AW11 M_DATA_A36
AV11 M_DATA_A37
AY7 M_DATA_A34
AY8 M_DATA_A38
AW9 M_DATA_A33
AW10 M_DATA_A32
AV7 M_DATA_A35
AW7 M_DATA_A39
AW5 M_DATA_A40
AY5 M_DATA_A45
AW2 M_DATA_A47
AW3 M_DATA_A46
AY4 M_DATA_A41
AV5 M_DATA_A44
AV1 M_DATA_A43
AV2 M_DATA_A42
AT1 M_DATA_A48
AN1 M_DATA_A50
AT3 M_DATA_A52
AP1 M_DATA_A54
AT2 M_DATA_A53
AN3 M_DATA_A55
AR1 M_DATA_A49
AN2 M_DATA_A51
AL2 M_DATA_A56
AH1 M_DATA_A58
AL3 M_DATA_A60
AJ1 M_DATA_A62
AH3 M_DATA_A63
AL1 M_DATA_A61
AH2 M_DATA_A59
AK1 M_DATA_A57
M_DATA_A[63..0] [8]
DDR0_DQSN[0]
DDR0_DQSN[1]
DDR0_DQSN[2]
DDR0_DQSN[3]
DDR0_DQSN[4]
DDR0_DQSN[5]
DDR0_DQSN[6]
DDR0_DQSN[7]
DDR0_DQSN[8]
AF38 M_DQS_A_DN0
AL38 M_DQS_A_DN1
AT38 M_DQS_A_DN2
AV35 M_DQS_A_DN3
AV9 M_DQS_A_DN4
AV4 M_DQS_A_DN5
AR3 M_DQS_A_DN6
AK3 M_DQS_A_DN7
AJ31
M_DQS_A_DN0 [8]
M_DQS_A_DN1 [8]
M_DQS_A_DN2 [8]
M_DQS_A_DN3 [8]
M_DQS_A_DN4 [8]
M_DQS_A_DN5 [8]
M_DQS_A_DN6 [8]
M_DQS_A_DN7 [8]
DDR0_DQSP[0]
DDR0_DQSP[1]
DDR0_DQSP[2]
DDR0_DQSP[3]
DDR0_DQSP[4]
DDR0_DQSP[5]
DDR0_DQSP[6]
DDR0_DQSP[7]
DDR0_DQSP[8]
AG38 M_DQS_A_DP0
AM38 M_DQS_A_DP1
AU38 M_DQS_A_DP2
AV34 M_DQS_A_DP3
AV8 M_DQS_A_DP4
AV3 M_DQS_A_DP5
AP3 M_DQS_A_DP6
AJ3 M_DQS_A_DP7
AJ30
M_DQS_A_DP0 [8]
M_DQS_A_DP1 [8]
M_DQS_A_DP2 [8]
M_DQS_A_DP3 [8]
M_DQS_A_DP4 [8]
M_DQS_A_DP5 [8]
M_DQS_A_DP6 [8]
M_DQS_A_DP7 [8]
CHANNEL A
SOCKET1200-HF_1
CPU1B
CML-S
[9] M_MAA_B[16..0]
M_MAA_B0 AP19
M_MAA_B1 AP20
M_MAA_B2 AR20
M_MAA_B3 AM20
M_MAA_B4 AP21
M_MAA_B5 AN21
M_MAA_B6 AR22
M_MAA_B7 AM21
M_MAA_B8 AP22
M_MAA_B9 AN23
M_MAA_B10 AR18
M_MAA_B11 AP23
M_MAA_B12 AR24
M_MAA_B13 AP15
M_MAA_B14 AP17
M_MAA_B15 AP16
M_MAA_B16 AM18
DDR1_MA[0]
DDR1_MA[1]
DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]
DDR1_MA[6]
DDR1_MA[7]
DDR1_MA[8]
DDR1_MA[9]
DDR1_MA[10]
DDR1_MA[11]
DDR1_MA[12]
DDR1_MA[13]
DDR1_MA[14]
DDR1_MA[15]
DDR1_MA[16]
[9] M_ACT_B_N
M_ACT_B_N AP25
DDR1_ACT#
[9] M_CKE_B0
[9] M_CKE_B1
[9] M_CKE_B2
[9] M_CKE_B3
M_CKE_B0 AT25
M_CKE_B1 AR26
M_CKE_B2 AT26
M_CKE_B3 AP26
DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
[9] M_CS#_B0
[9] M_CS#_B1
[9] M_CS#_B2
[9] M_CS#_B3
M_CS#_B0 AN17
M_CS#_B1 AN15
M_CS#_B2 AR16
M_CS#_B3 AM15
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
[9] M_ODT_B0
[9] M_ODT_B1
[9] M_ODT_B2
[9] M_ODT_B3
M_ODT_B0 AM17
M_ODT_B1 AP14
M_ODT_B2 AM16
M_ODT_B3 AM14
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
[9] M_BA_B_0
[9] M_BA_B_1
M_BA_B_0 AP18
M_BA_B_1 AN19
DDR1_BA[0]
DDR1_BA[1]
[9] M_BG_B_0
[9] M_BG_B_1
M_BG_B_0 AM23
M_BG_B_1 AM22
DDR1_BG[0]
DDR1_BG[1]
[9] M_CK_B_DP0
[9] M_CK_B_DN0
[9] M_CK_B_DP1
[9] M_CK_B_DN1
[9] M_CK_B_DP2
[9] M_CK_B_DN2
[9] M_CK_B_DP3
[9] M_CK_B_DN3
M_CK_B_DP0 AT23
M_CK_B_DN0 AU23
M_CK_B_DP1 AV22
M_CK_B_DN1 AU22
M_CK_B_DP2 AT21
M_CK_B_DN2 AU21
M_CK_B_DP3 AU20
M_CK_B_DN3 AV20
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
[9] M_PARITY_B
[9] M_ALERT_B_N
M_PARITY_B AM19
M_ALERT_B_N AP24
DDR1_PAR
DDR1_ALERT#
AJ28
AK26
AL26
AM28
AK28
AL28
AM27
AM26
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]
CPU_VREF_CA0_B
CPU_VREF_CA1_B
AC39
AB40
DDR_VREF_CA2
DDR_VREF_CA3
DDR1_DQ[0]
DDR1_DQ[1]
DDR1_DQ[2]
DDR1_DQ[3]
DDR1_DQ[4]
DDR1_DQ[5]
DDR1_DQ[6]
DDR1_DQ[7]
DDR1_DQ[8]
DDR1_DQ[9]
DDR1_DQ[10]
DDR1_DQ[11]
DDR1_DQ[12]
DDR1_DQ[13]
DDR1_DQ[14]
DDR1_DQ[15]
DDR1_DQ[16]
DDR1_DQ[17]
DDR1_DQ[18]
DDR1_DQ[19]
DDR1_DQ[20]
DDR1_DQ[21]
DDR1_DQ[22]
DDR1_DQ[23]
DDR1_DQ[24]
DDR1_DQ[25]
DDR1_DQ[26]
DDR1_DQ[27]
DDR1_DQ[28]
DDR1_DQ[29]
DDR1_DQ[30]
DDR1_DQ[31]
DDR1_DQ[32]
DDR1_DQ[33]
DDR1_DQ[34]
DDR1_DQ[35]
DDR1_DQ[36]
DDR1_DQ[37]
DDR1_DQ[38]
DDR1_DQ[39]
DDR1_DQ[40]
DDR1_DQ[41]
DDR1_DQ[42]
DDR1_DQ[43]
DDR1_DQ[44]
DDR1_DQ[45]
DDR1_DQ[46]
DDR1_DQ[47]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
AD34 M_DATA_B4
AD35 M_DATA_B0
AE36 M_DATA_B1
AF36 M_DATA_B6
AG35 M_DATA_B3
AG34 M_DATA_B7
AD36 M_DATA_B5
AG36 M_DATA_B2
AJ36 M_DATA_B13
AJ35 M_DATA_B8
AL36 M_DATA_B14
AM35 M_DATA_B10
AK36 M_DATA_B9
AJ34 M_DATA_B12
AM36 M_DATA_B15
AM34 M_DATA_B11
AT36 M_DATA_B17
AP36 M_DATA_B20
AT34 M_DATA_B23
AP33 M_DATA_B19
AR36 M_DATA_B16
AT35 M_DATA_B21
AR33 M_DATA_B22
AT33 M_DATA_B18
AP31 M_DATA_B28
AT31 M_DATA_B24
AT29 M_DATA_B30
AP28 M_DATA_B27
AR31 M_DATA_B29
AT30 M_DATA_B25
AR28 M_DATA_B31
AT28 M_DATA_B26
AT12 M_DATA_B36
AR12 M_DATA_B37
AT10 M_DATA_B39
AR10 M_DATA_B38
AP12 M_DATA_B33
AT11 M_DATA_B32
AP10 M_DATA_B34
AN10 M_DATA_B35
AR8 M_DATA_B45
AT8 M_DATA_B44
AT5 M_DATA_B46
AT6 M_DATA_B47
AP8 M_DATA_B41
AT7 M_DATA_B40
AP5 M_DATA_B43
AR5 M_DATA_B42
AM8 M_DATA_B52
AM7 M_DATA_B53
AK6 M_DATA_B54
AM5 M_DATA_B48
AM6 M_DATA_B49
AK7 M_DATA_B51
AK5 M_DATA_B50
AL5 M_DATA_B55
AF7 M_DATA_B63
AH8 M_DATA_B60
AG5 M_DATA_B62
AF6 M_DATA_B59
AH6 M_DATA_B57
AH7 M_DATA_B56
AF5 M_DATA_B58
AH5 M_DATA_B61
M_DATA_B[63..0] [9]
DDR1_DQSN[0]
DDR1_DQSN[1]
DDR1_DQSN[2]
DDR1_DQSN[3]
DDR1_DQSN[4]
DDR1_DQSN[5]
DDR1_DQSN[6]
DDR1_DQSN[7]
DDR1_DQSN[8]
AE34 M_DQS_B_DN0
AK34 M_DQS_B_DN1
AP35 M_DQS_B_DN2
AP30 M_DQS_B_DN3
AN12 M_DQS_B_DN4
AP7 M_DQS_B_DN5
AL8 M_DQS_B_DN6
AG8 M_DQS_B_DN7
AJ26
M_DQS_B_DN0 [9]
M_DQS_B_DN1 [9]
M_DQS_B_DN2 [9]
M_DQS_B_DN3 [9]
M_DQS_B_DN4 [9]
M_DQS_B_DN5 [9]
M_DQS_B_DN6 [9]
M_DQS_B_DN7 [9]
DDR1_DQSP[0]
DDR1_DQSP[1]
DDR1_DQSP[2]
DDR1_DQSP[3]
DDR1_DQSP[4]
DDR1_DQSP[5]
DDR1_DQSP[6]
DDR1_DQSP[7]
DDR1_DQSP[8]
AF34 M_DQS_B_DP0
AL34 M_DQS_B_DP1
AP34 M_DQS_B_DP2
AP29 M_DQS_B_DP3
AN11 M_DQS_B_DP4
AP6 M_DQS_B_DP5
AK8 M_DQS_B_DP6
AF8 M_DQS_B_DP7
AJ27
M_DQS_B_DP0 [9]
M_DQS_B_DP1 [9]
M_DQS_B_DP2 [9]
M_DQS_B_DP3 [9]
M_DQS_B_DP4 [9]
M_DQS_B_DP5 [9]
M_DQS_B_DP6 [9]
M_DQS_B_DP7 [9]
CHANNEL B
SOCKET1200-HF_1
2020/9/10
CPU1.AT31 and CPU1.AR31
are swapped by same as 7D10
MICRO-STAR INT'L CO.,LTD.
Title
CPU-Memory
Size
Document Number
MS-7D15..
Rev
10/20
Date: Tuesday, November 03, 2020
Sheet 4 of 76





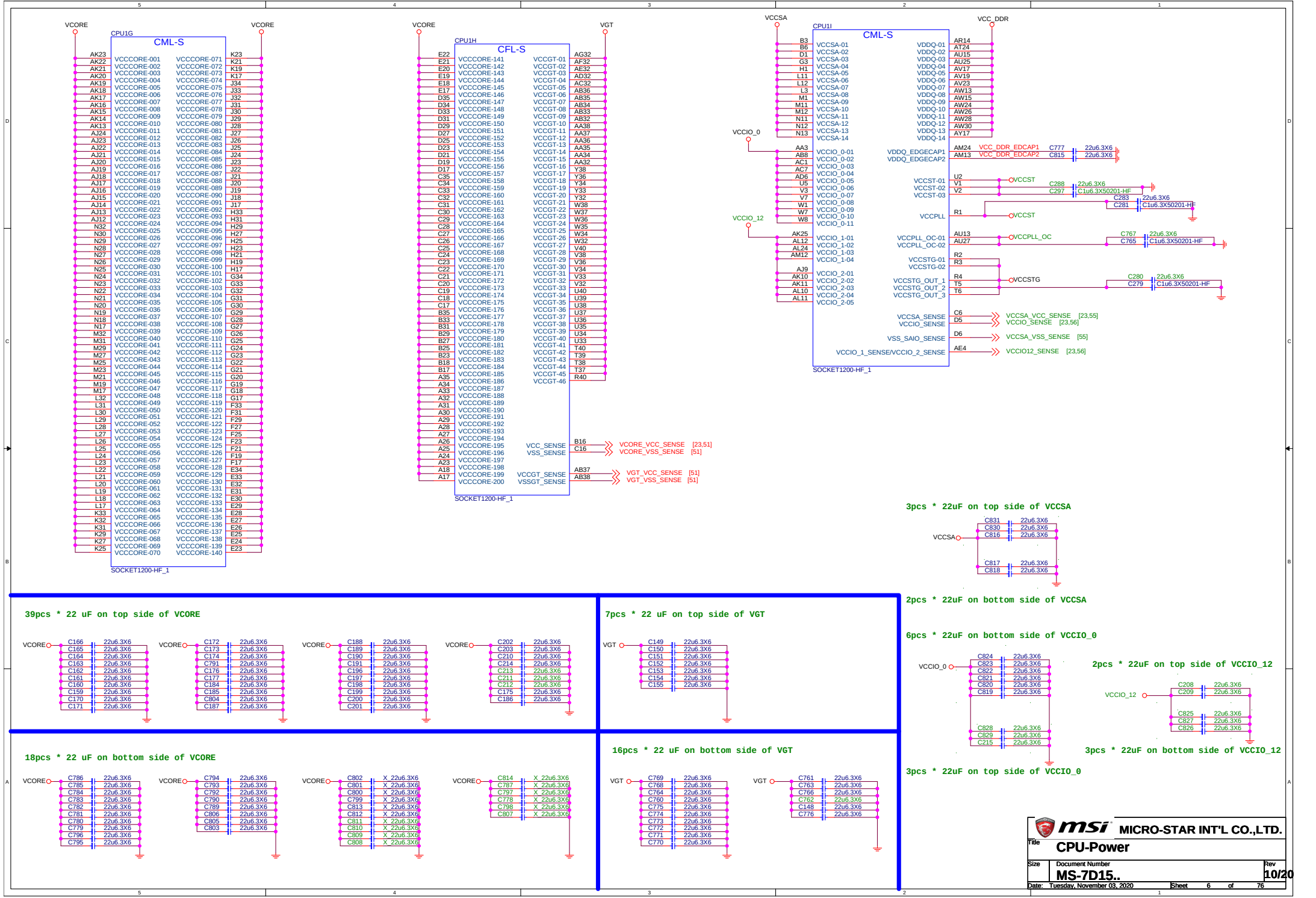


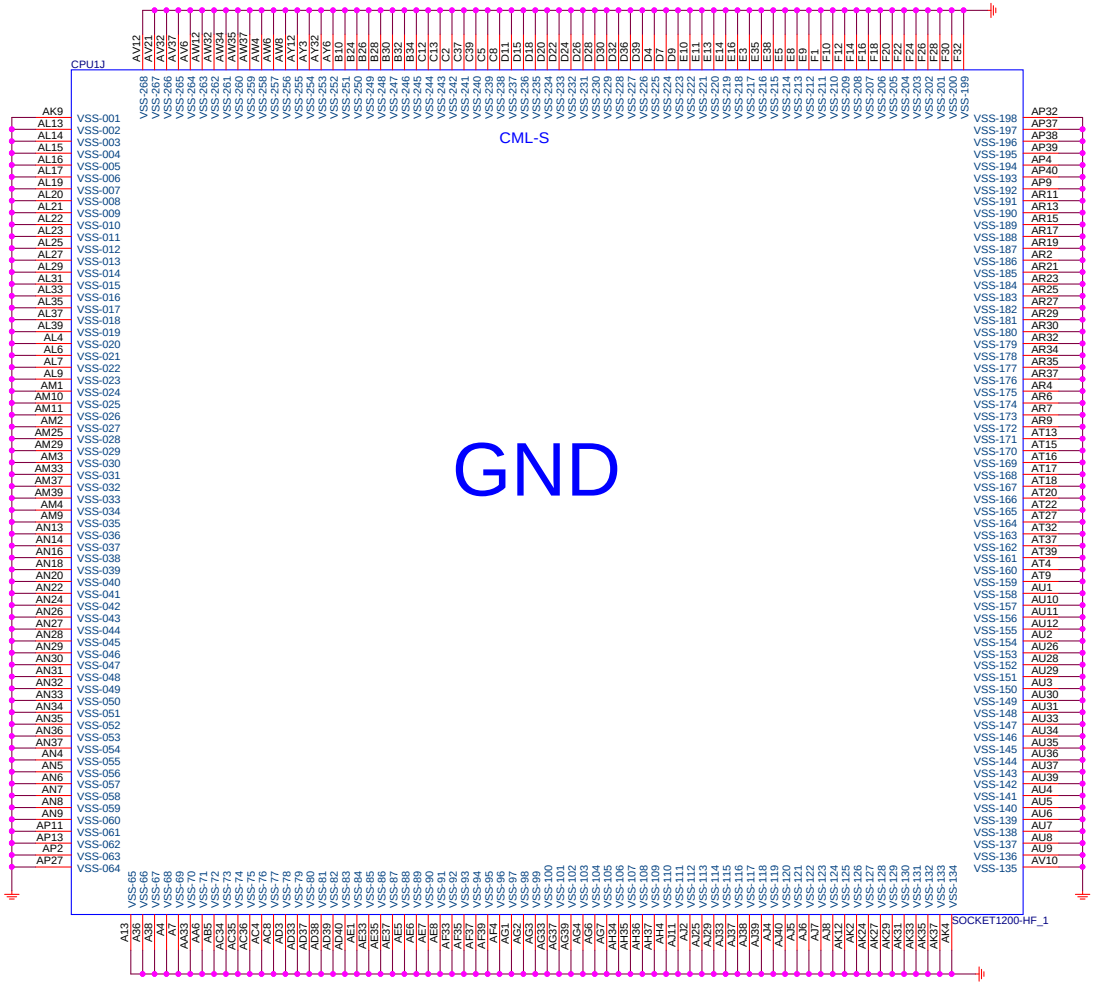
MICRO-STAR INT'L CO.,LTD.

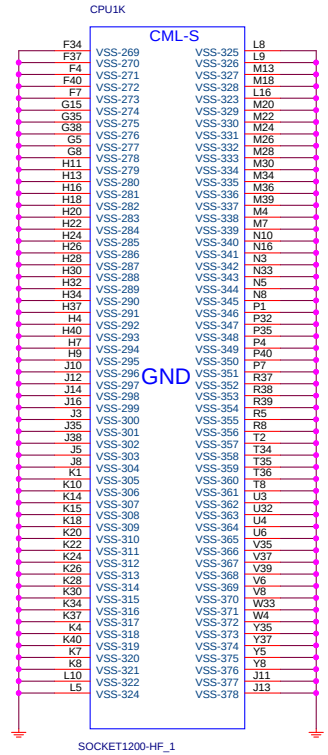
Title: CPU-PEG/Display/RSD

Size | Document Number: MS-7D15.. | Rev: 10/20

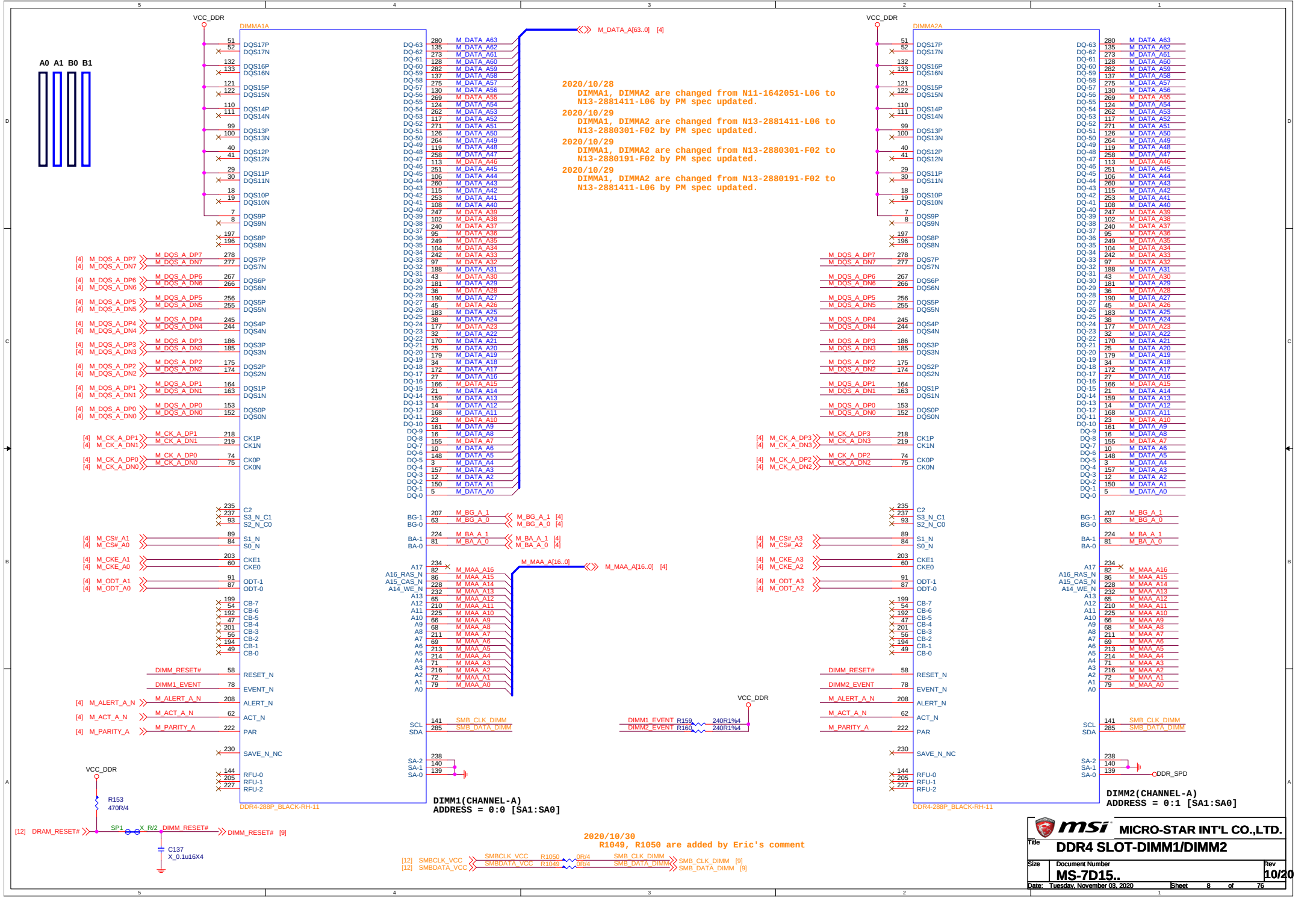
Date: Tuesday, November 03, 2020 | Sheet 5 of 76


CPU1G
CML-S
SOCKET1200-HF_1
CPU1H
CFL-S
SOCKET1200-HF_1
CPU1I
CML-S
SOCKET1200-HF_1
VCORE_VCC_SENSE [23,51]
VCORE_VSS_SENSE [51]
VGT_VCC_SENSE [51]
VGT_VSS_SENSE [51]
VCCSA_VCC_SENSE [23,55]
VCCIO_SENSE [23,56]
VCCSA_VSS_SENSE [55]
VCCIO12_SENSE [23,56]
3pcs * 22uF on top side of VCCSA
2pcs * 22uF on bottom side of VCCSA
39pcs * 22 uF on top side of VCORE
7pcs * 22 uF on top side of VGT
6pcs * 22uF on bottom side of VCCIO_0
2pcs * 22uF on top side of VCCIO_12
3pcs * 22uF on bottom side of VCCIO_12
3pcs * 22uF on top side of VCCIO_0
18pcs * 22 uF on bottom side of VCORE
16pcs * 22 uF on bottom side of VGT
MICRO-STAR INT'L CO.,LTD.
CPU-Power
MS-7D15..
10/20
Tuesday, November 03, 2020
Sheet 6 of 76





MSI	MICRO-STAR INT'L CO.,LTD.		
Title	CPU-GND		
Size	Document Number		Rev
	MS-7D15..		10/20
Date:	Tuesday, November 03, 2020	Sheet 7 of 76	

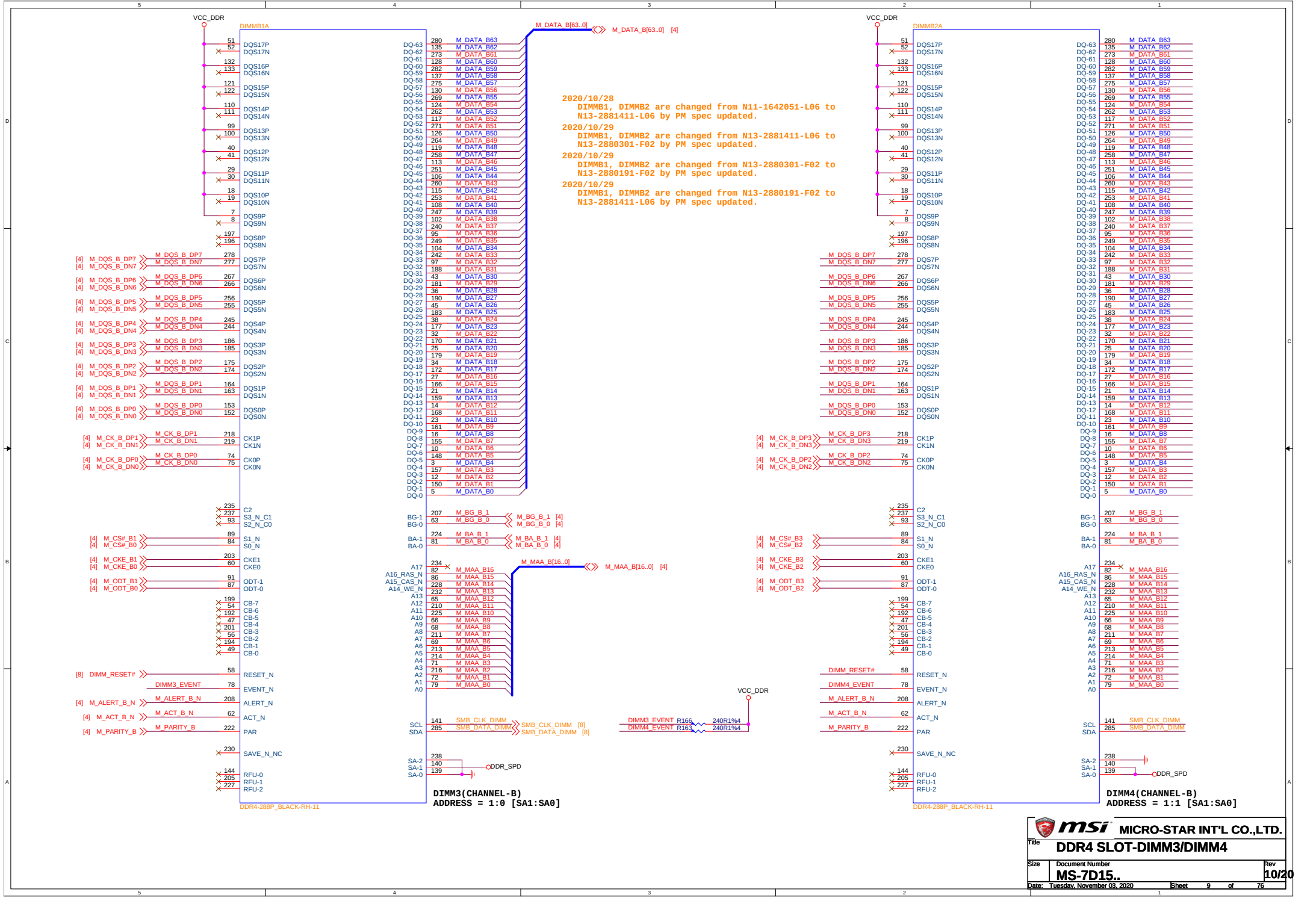


MICRO-STAR INT'L CO.,LTD.

Title: DDR4 SLOT-DIMM1/DIMM2

Size: | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 8 of 76


2020/10/28
DIMMB1, DIMMB2 are changed from N11-1642051-L06 to N13-2881411-L06 by PM spec updated.
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2881411-L06 to N13-2880301-F02 by PM spec updated.
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2880301-F02 to N13-2880191-F02 by PM spec updated.
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2880191-F02 to N13-2881411-L06 by PM spec updated.
VCC_DDR
DIMMB1A
M_DATA_B[63..0]
M_DATA_B[63..0] [4]
M_MAA_B[16..0]
M_MAA_B[16..0] [4]
DDR4-288P_BLACK-RH-11
DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DIMMB2A
DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
DIMM3_EVENT R166 240R1%4
DIMM4_EVENT R163 240R1%4
DDR_SPD
MICRO-STAR INT'L CO.,LTD.
Title
DDR4 SLOT-DIMM3/DIMM4
Size
Document Number
MS-7D15..
Rev
10/20
Date: Tuesday, November 03, 2020
Sheet 9 of 76

2020/10/28
DIMMA1, DIMMA2 are changed from N11-1642051-L06 to N13-2881411-L06 by PM spec updated.

2020/10/29
DIMMA1, DIMMA2 are changed from N13-2881411-L06 to N13-2880301-F02 by PM spec updated.

2020/10/29
DIMMA1, DIMMA2 are changed from N13-2880301-F02 to N13-2880191-F02 by PM spec updated.

2020/10/29
DIMMA1, DIMMA2 are changed from N13-2880191-F02 to N13-2881411-L06 by PM spec updated.

DIMMA1C

DDR4-288P_BLACK-RH-11

DIMMA2C

DDR4-288P_BLACK-RH-11

DIMMA1B

DDR4-288P_BLACK-RH-11

DIMMA2B

DDR4-288P_BLACK-RH-11

F5
F-SPR-P260T-2.6A

DT CRB VCC3
Server CRB VPP

Between in CPU and DIMM Slot

MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-1

Size | Document Number: MS-7D15.. | Rev: 10/20

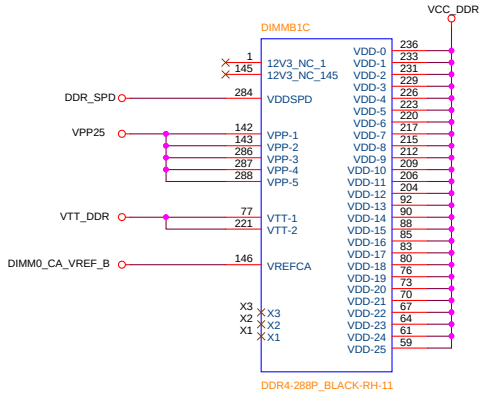
Date: Tuesday, November 03, 2020 | Sheet 10 of 76

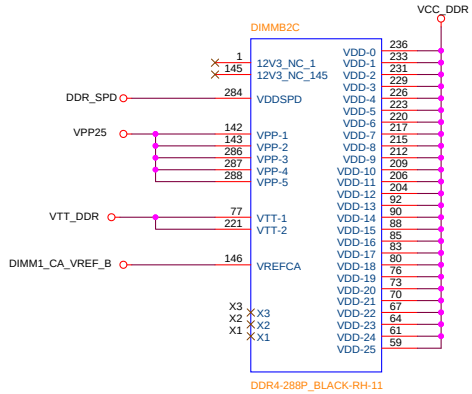
2020/10/28
DIMMB1, DIMMB2 are changed from N11-1642051-L06 to N13-2881411-L06 by PM spec updated.

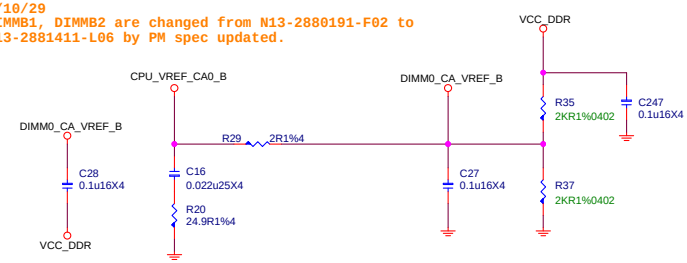
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2881411-L06 to N13-2880301-F02 by PM spec updated.

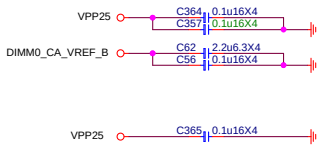
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2880301-F02 to N13-2880191-F02 by PM spec updated.

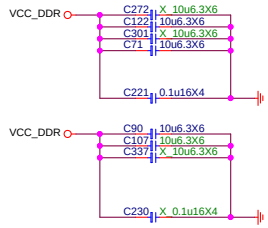
2020/10/29
DIMMB1, DIMMB2 are changed from N13-2880191-F02 to N13-2881411-L06 by PM spec updated.

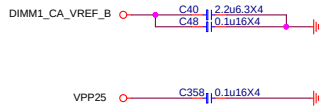


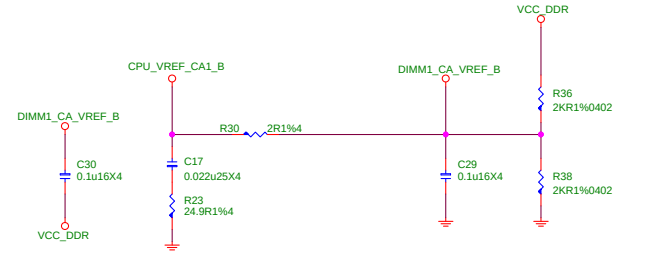


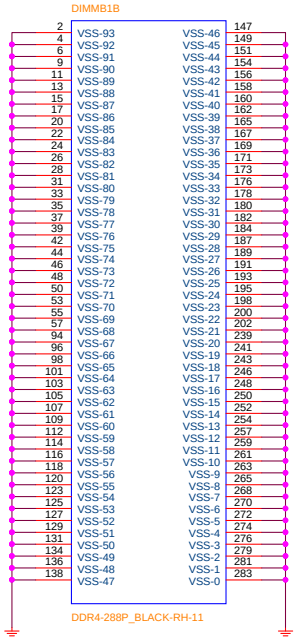


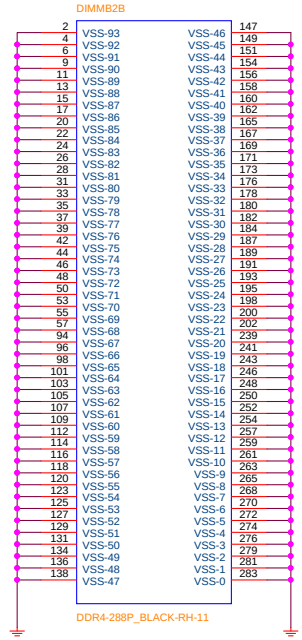


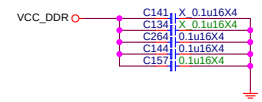












MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 11 of 76

2020/8/14
ESPI_RST# delete to repeat pull-down resistor

2020/7/27
R2211, R2212 are added by 500 series updated

PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan

PCH1A

eSPI
Power Management
GPP_D 1.8V
SMB
VID
STRAP
SPI
JTAG
Strap

RKL_PCH_H

M2_1 SEL

ID

2020/8/14
R1834 is changed from 100Kohm to 75Kohm by page 421 on PDG_Rev1.0

2020/9/10
C1888, C1889 are reserved by to reduce ESD from PDG_Rev1.0

RTC

Chassis Intrusion

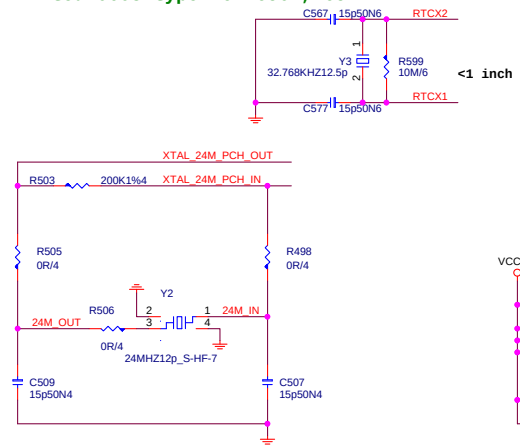
Title	PCH-LPC/SPI/SMBUS/MISC
Size	Document Number: MS-7D15..
Rev	10/20
Date:	Tuesday, November 03, 2020
Sheet	12 of 76

MICRO-STAR INT'L CO.,LTD.

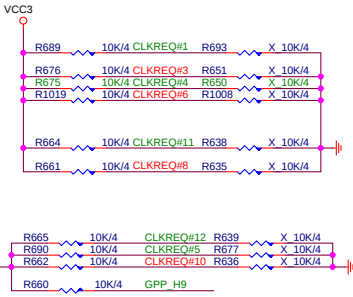
PCH_CLK

Close to PCH

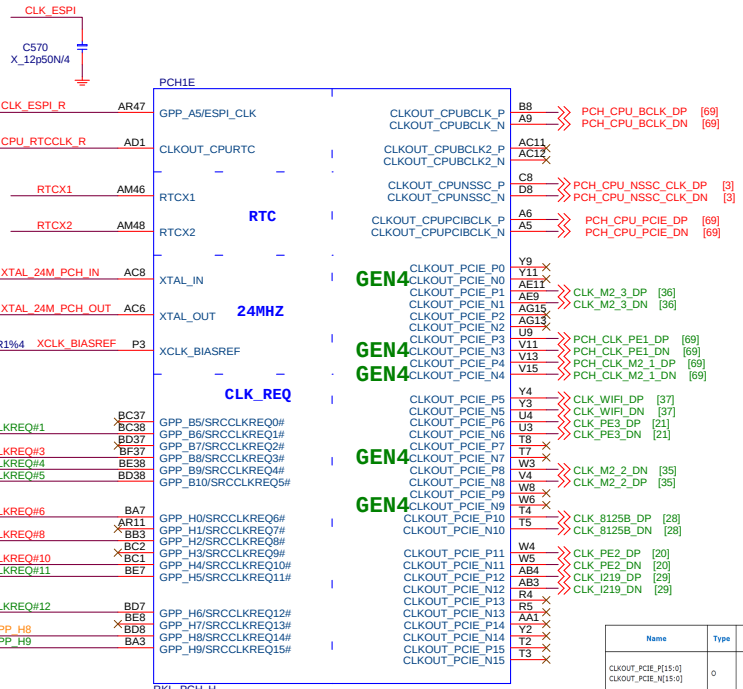
Limited 0603 type for C567, C577



XCLK_BIASREF < 1000 mil



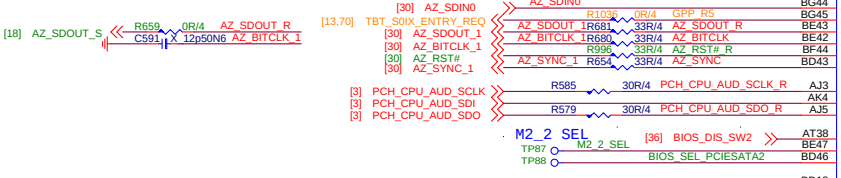
2020/10/27
R690.2 is changed from VCC3 to 3VSB
R661.2 is changed from 3VSB to VCC3
by circuit correctness
2020/11/2
R665.2 is changed from VCC3 to 3VSB
by circuit correctness

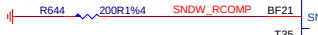


Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	**PCI Express* Clock Output**: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support
			• CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

PCH_AUDIO

2020/10/27
R1036 is added by Robert's comment

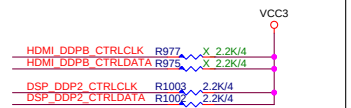




2020/10/27
R1037 is reversed by Robert's comment

To I225

2020/10/22
R977, R975 are unstuffed by page32 already pull-up.



GPP_K10 R981 X_100K1%4

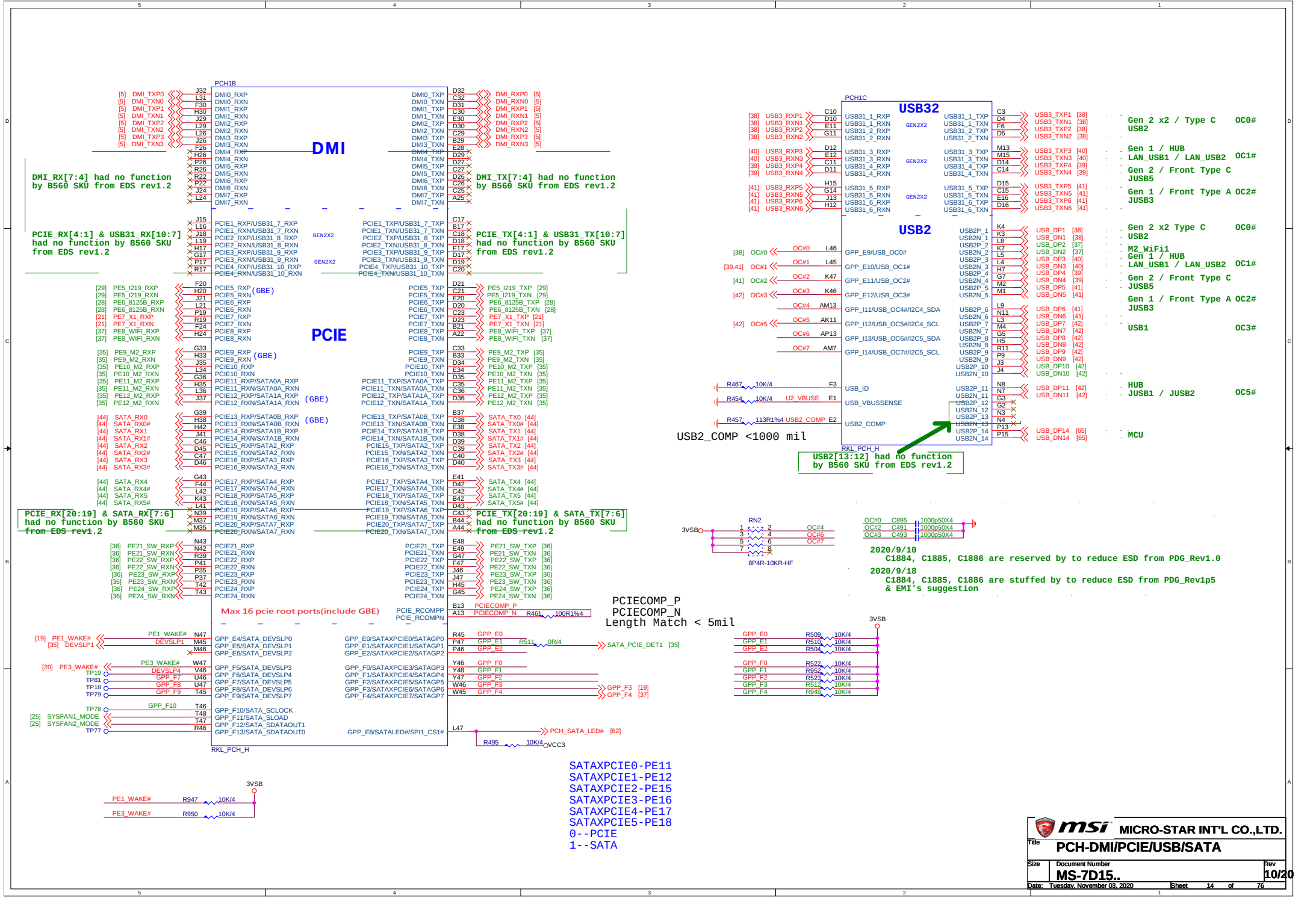
2020/10/27
R958 is unstuffed and R1038 is added by Robert's comment

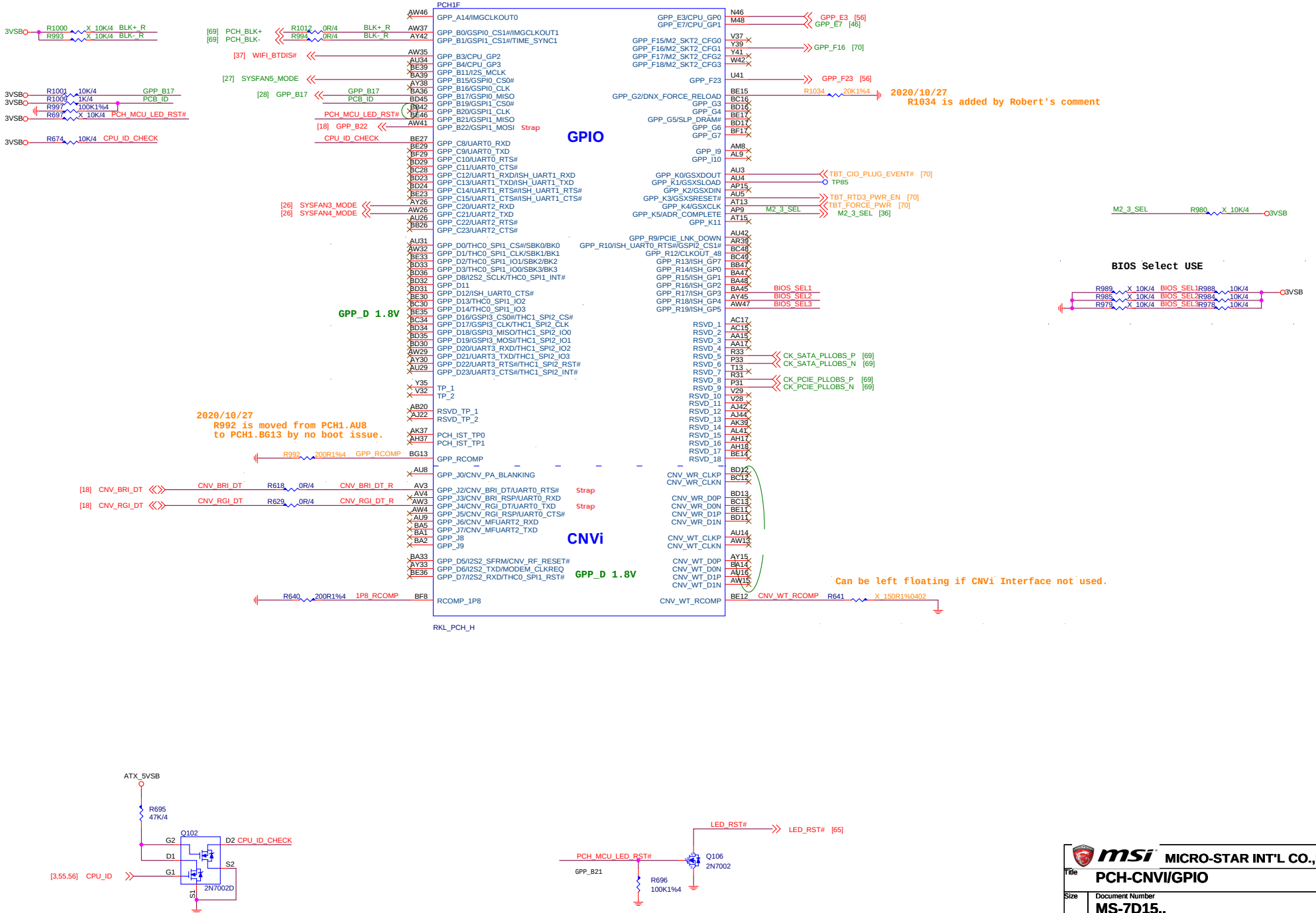
MICRO-STAR INT'L CO.,LTD.

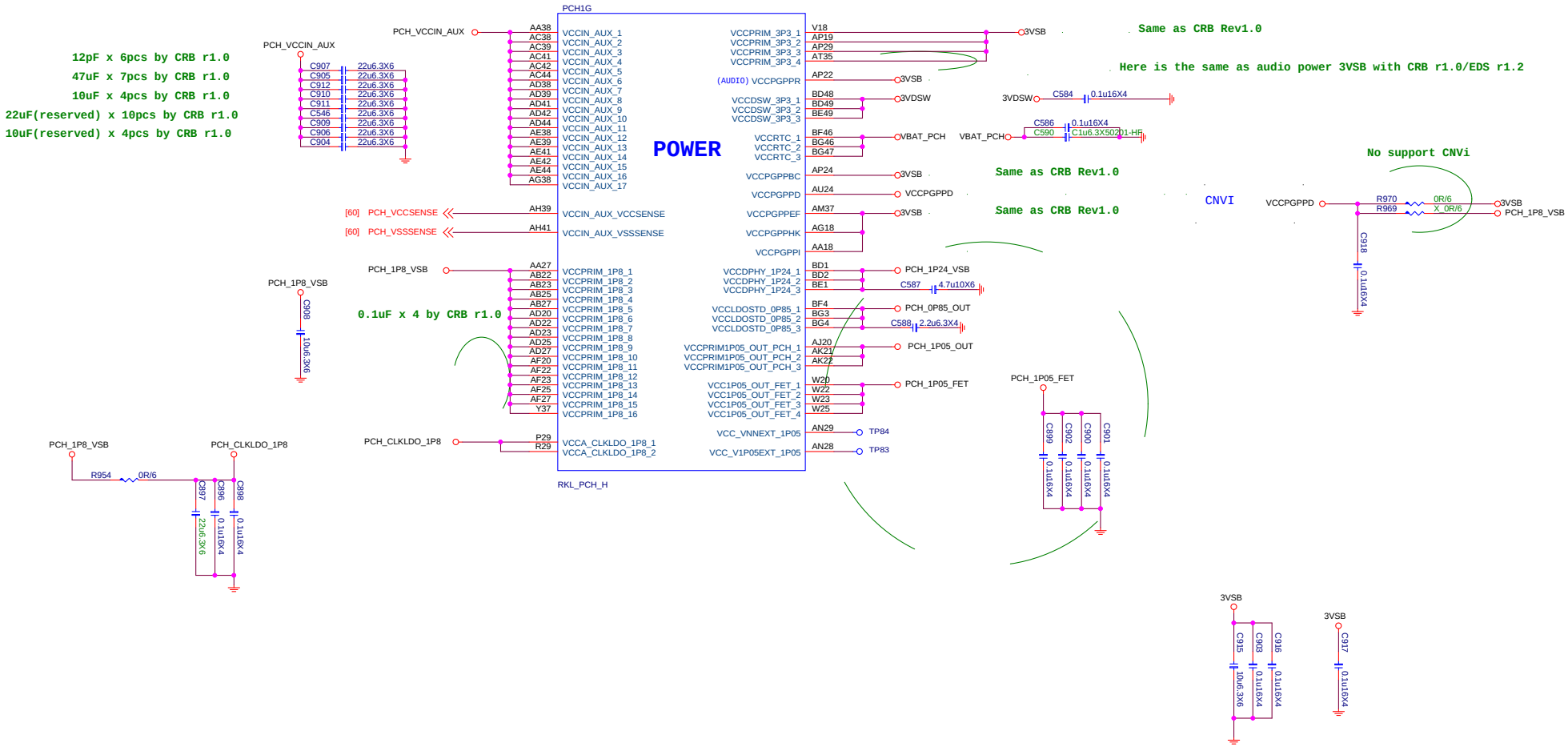
Title: Clock/Audio

Size: | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 13 of 76


PCH1B
DMI
DMI_RX[7:4] had no function by B560 SKU from EDS rev1.2
DMI_TX[7:4] had no function by B560 SKU from EDS rev1.2
PCIE_RX[4:1] & USB31_RX[10:7] had no function by B560 SKU from EDS rev1.2
PCIE_TX[4:1] & USB31_TX[10:7] had no function by B560 SKU from EDS rev1.2
PCIE
PCIE_RX[20:19] & SATA_RX[7:6] had no function by B560 SKU from EDS rev1.2
PCIE_TX[20:19] & SATA_TX[7:6] had no function by B560 SKU from EDS rev1.2
Max 16 pcie root ports(include GBE)
RKL_PCH_H
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
SATAXPCIE0-PE11
SATAXPCIE1-PE12
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
PCH1C
USB32
USB2
USB2_COMP <1000 mil
USB2[13:12] had no function by B560 SKU from EDS rev1.2
2020/9/10
C1884, C1885, C1886 are reserved by to reduce ESD from PDG_Rev1.0
2020/9/18
C1884, C1885, C1886 are stuffed by to reduce ESD from PDG_Rev1p5 & EMI's suggestion
MICRO-STAR INT'L CO.,LTD.
PCH-DMI/PCIE/USB/SATA
MS-7D15..
10/20
Tuesday, November 03, 2020
Sheet 14 of 76


PCH1F
GPIO
GPP_D 1.8V
CNVi
GPP_D 1.8V
RKL_PCH_H
GPP_A14/IMGCLKOUT0
GPP_B0/GSPI0_CS1#/IMGCLKOUT1
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_B11/I2S_MCLK
GPP_B15/GSPI0_CS0#
GPP_B16/GSPI0_CLK
GPP_B17/GSPI0_MISO
GPP_B19/GSPI1_CS0#
GPP_B20/GSPI1_CLK
GPP_B21/GSPI1_MISO
GPP_B22/GSPI1_MOSI Strap
GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#
GPP_C12/UART1_RXD/ISH_UART1_RXD
GPP_C13/UART1_TXD/ISH_UART1_TXD
GPP_C14/UART1_RTS#/ISH_UART1_RTS#
GPP_C15/UART1_CTS#/ISH_UART1_CTS#
GPP_C20/UART2_RXD
GPP_C21/UART2_TXD
GPP_C22/UART2_RTS#
GPP_C23/UART2_CTS#
GPP_D0/THC0_SPI1_CS#/SBK0/BK0
GPP_D1/THC0_SPI1_CLK/SBK1/BK1
GPP_D2/THC0_SPI1_IO1/SBK2/BK2
GPP_D3/THC0_SPI1_IO0/SBK3/BK3
GPP_D8/I2S2_SCLK/THC0_SPI1_INT#
GPP_D11
GPP_D12/ISH_UART0_CTS#
GPP_D13/THC0_SPI1_IO2
GPP_D14/THC0_SPI1_IO3
GPP_D16/GSPI3_CS0#/THC1_SPI2_CS#
GPP_D17/GSPI3_CLK/THC1_SPI2_CLK
GPP_D18/GSPI3_MISO/THC1_SPI2_IO0
GPP_D19/GSPI3_MOSI/THC1_SPI2_IO1
GPP_D20/UART3_RXD/THC1_SPI2_IO2
GPP_D21/UART3_TXD/THC1_SPI2_IO3
GPP_D22/UART3_RTS#/THC1_SPI2_RST#
GPP_D23/UART3_CTS#/THC1_SPI2_INT#
TP_1
TP_2
RSVD_TP_1
RSVD_TP_2
PCH_IST_TP0
PCH_IST_TP1
GPP_RCOMP
GPP_J0/CNV_PA_BLANKING
GPP_J2/CNV_BRI_DT/UART0_RTS# Strap
GPP_J3/CNV_BRI_RSP/UART0_RXD
GPP_J4/CNV_RGI_DT/UART0_TXD Strap
GPP_J5/CNV_RGI_RSP/UART0_CTS#
GPP_J6/CNV_MFUART2_RXD
GPP_J7/CNV_MFUART2_TXD
GPP_J8
GPP_J9
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D7/I2S2_RXD/THC0_SPI1_RST#
RCOMP_1P8
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_F15/M2_SKT2_CFG0
GPP_F16/M2_SKT2_CFG1
GPP_F17/M2_SKT2_CFG2
GPP_F18/M2_SKT2_CFG3
GPP_F23
GPP_G2/DNX_FORCE_RELOAD
GPP_G3
GPP_G4
GPP_G5/SLP_DRAM#
GPP_G6
GPP_G7
GPP_I9
GPP_I10
GPP_K0/GSXDOUT
GPP_K1/GSXSLOAD
GPP_K2/GSXDIN
GPP_K3/GSXSRESET#
GPP_K4/GSXCLK
GPP_K5/ADR_COMPLETE
GPP_K11
GPP_R9/PCIE_LNK_DOWN
GPP_R10/ISH_UART0_RTS#/GSPI2_CS1#
GPP_R12/CLKOUT_48
GPP_R13/ISH_GP7
GPP_R14/ISH_GP0
GPP_R15/ISH_GP1
GPP_R16/ISH_GP2
GPP_R17/ISH_GP3
GPP_R18/ISH_GP4
GPP_R19/ISH_GP5
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
RSVD_18
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WR_D0P
CNV_WR_D0N
CNV_WR_D1P
CNV_WR_D1N
CNV_WT_CLKP
CNV_WT_CLKN
CNV_WT_D0P
CNV_WT_D0N
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_RCOMP
2020/10/27
R1034 is added by Robert's comment
2020/10/27
R992 is moved from PCH1.AU8
to PCH1.BG13 by no boot issue.
BIOS Select USE
Can be left floating if CNVi Interface not used.
ATX_5VSB
Q102
2N7002D
Q106
2N7002
LED_RST#
PCH_MCU_LED_RST#
GPP_B21
MICRO-STAR INT'L CO.,LTD.
PCH-CNVI/GPIO
MS-7D15..
10/20
Tuesday, November 03, 2020
Sheet 15 of 76

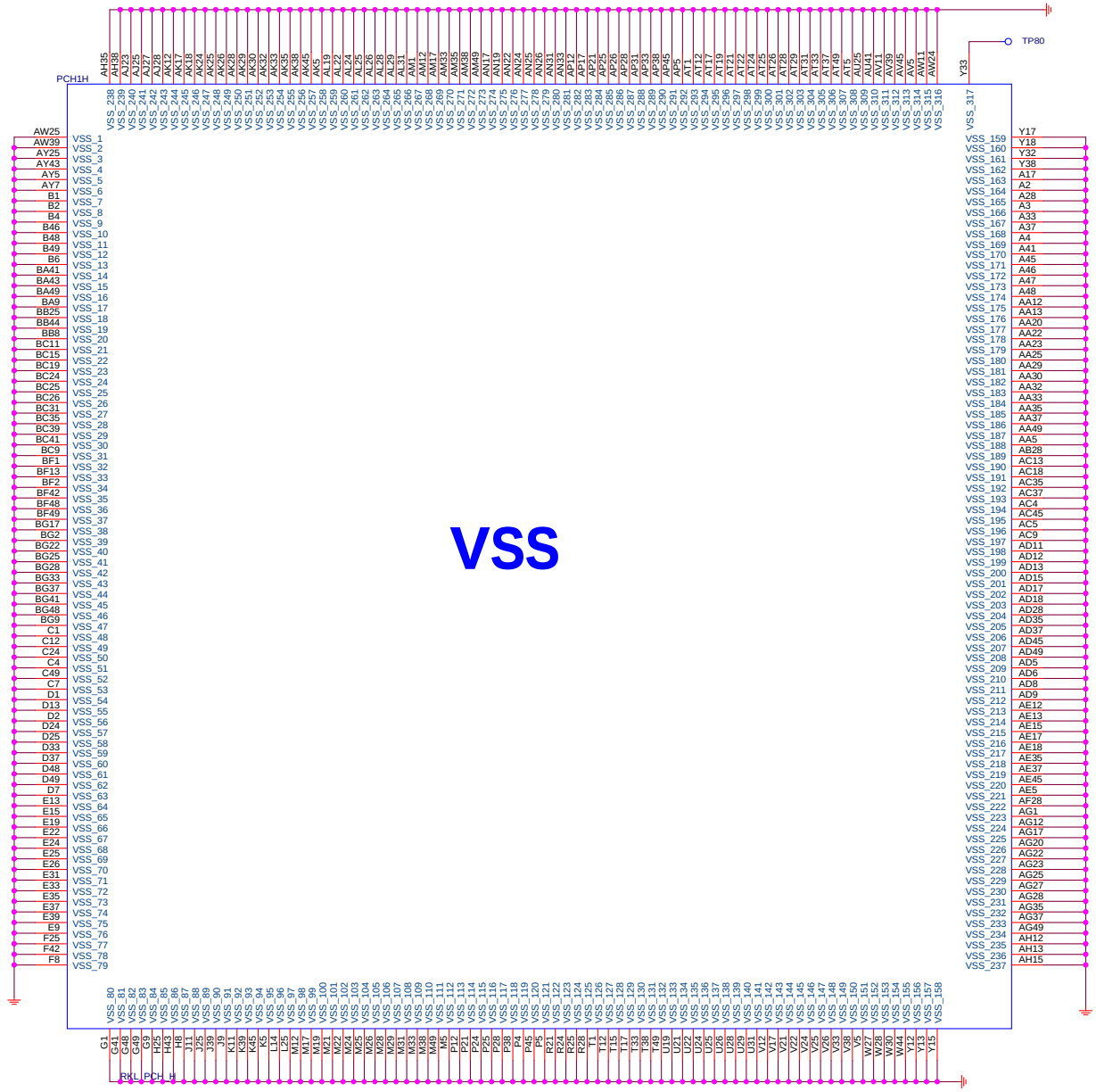


MICRO-STAR INT'L CO.,LTD.

Title: PCH-Power

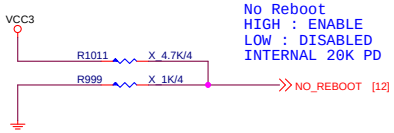
Size | Document Number: MS-7D15.. | Rev: 10/20

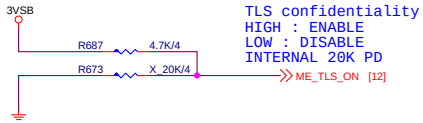
Date: Tuesday, November 03, 2020 | Sheet 16 of 76

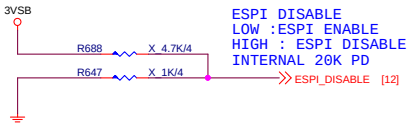


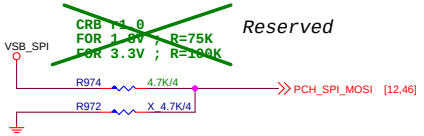
Title	PCH-GND
Size	Document Number: MS-7D15..
Rev	10/20
Date:	Tuesday, November 03, 2020
Sheet	17 of 76

MICRO-STAR INT'L CO.,LTD.

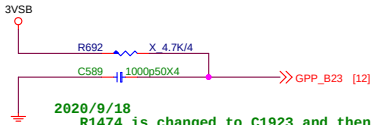




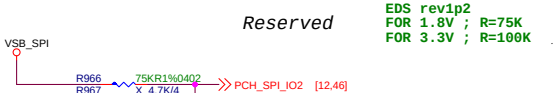


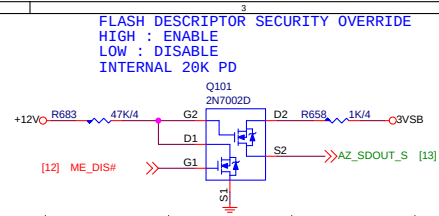


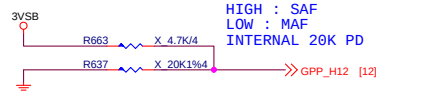
2020/9/15
R853 is changed from 75Kohm to 4.7Kohm by same as SCH__Rev1p1 & ug-rev0p5
2020/9/17
Intel FAE agreed to stuff 4.7k at R853

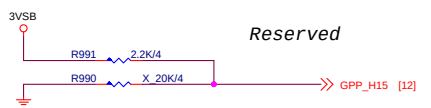


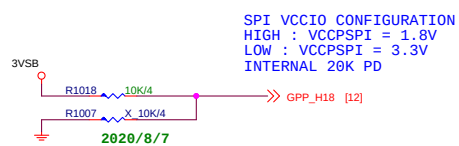
2020/9/18
R1474 is changed to C1923 and then is stuffed 0.1uF
by to reduce ESD from PDG_Rev1p5 & EMI's suggestion



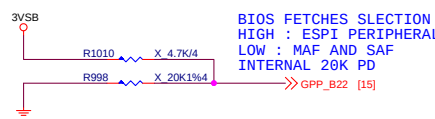


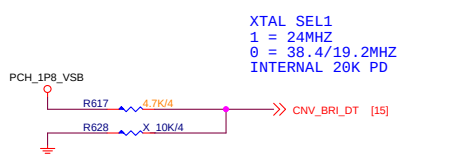


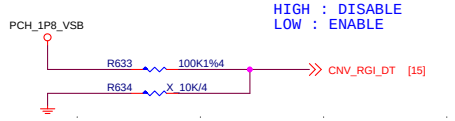


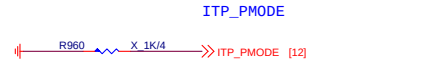


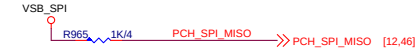
2020/8/7
R828 is stuffed by Robert's comment

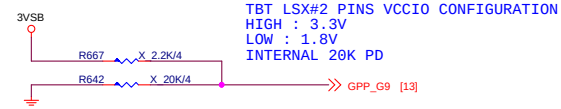


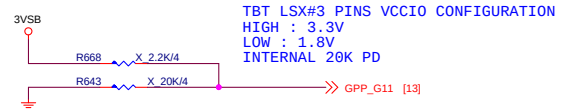


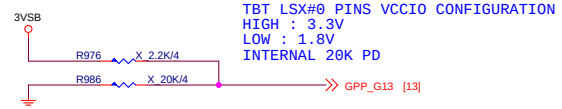


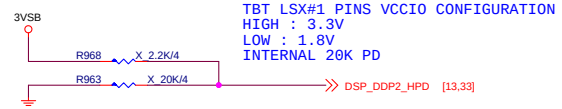












MICRO-STAR INT'L CO.,LTD.

Title: PCH-STRAP

Size: | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 18 of 76

PCI_Express X16 Slot

12V - 5.5A
VCC3 - 3A
3VSB- 375mA

SMBus ESD

D19
SMBDATA_VSB_R
SMBCLK_VSB_R
ESD-AOZ8906

Under Checking

2020/7/17
PCIE_PWR1 is added by PM spec updated

2020/10/27
The p/n of PCI_E1 is changed to N11-1642051-L06 by same as PM spec

2020/10/30
R1048, D45, D46 are added by Rober's comment

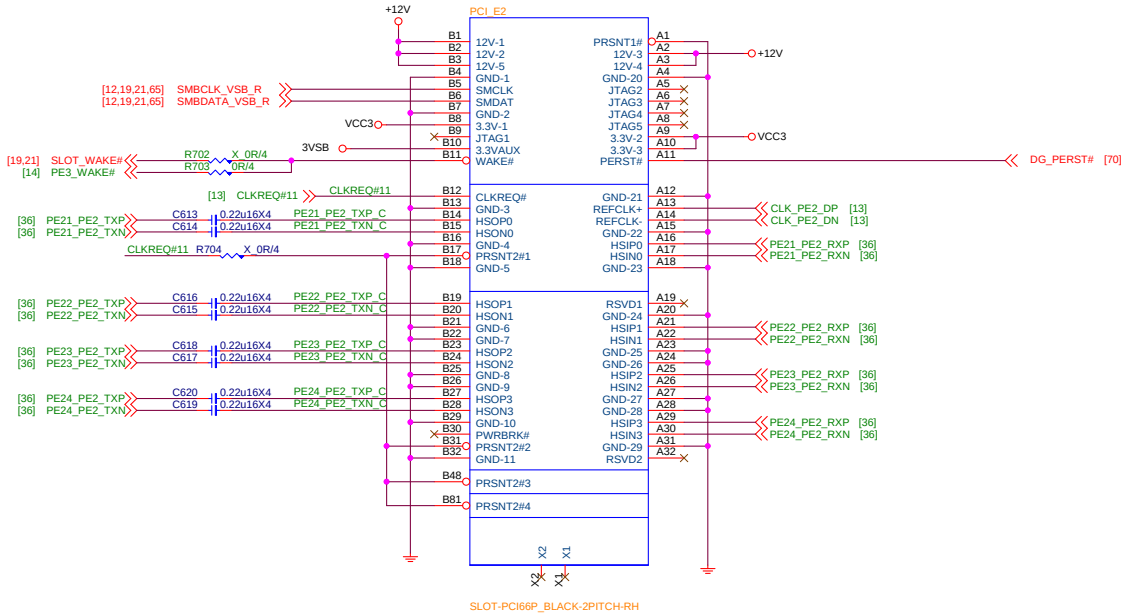
SLOT-PCI164P_BLACK-2PITCH-RH-77

Title	PCIE SLOT X16
Size	Document Number: MS-7D15..
Rev	10/20
Date:	Tuesday, November 03, 2020
Sheet	19 of 76

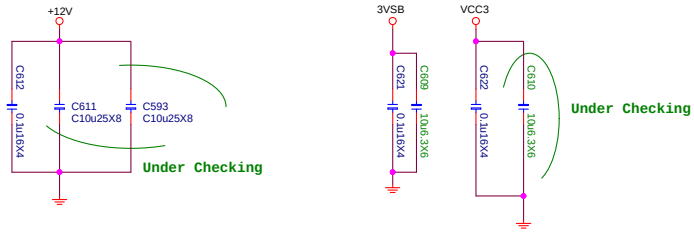
MICRO-STAR INT'L CO.,LTD.

PCI_Express X4 Slot

2.1A at +12V
3A at VCC3
375mA at 3VSB

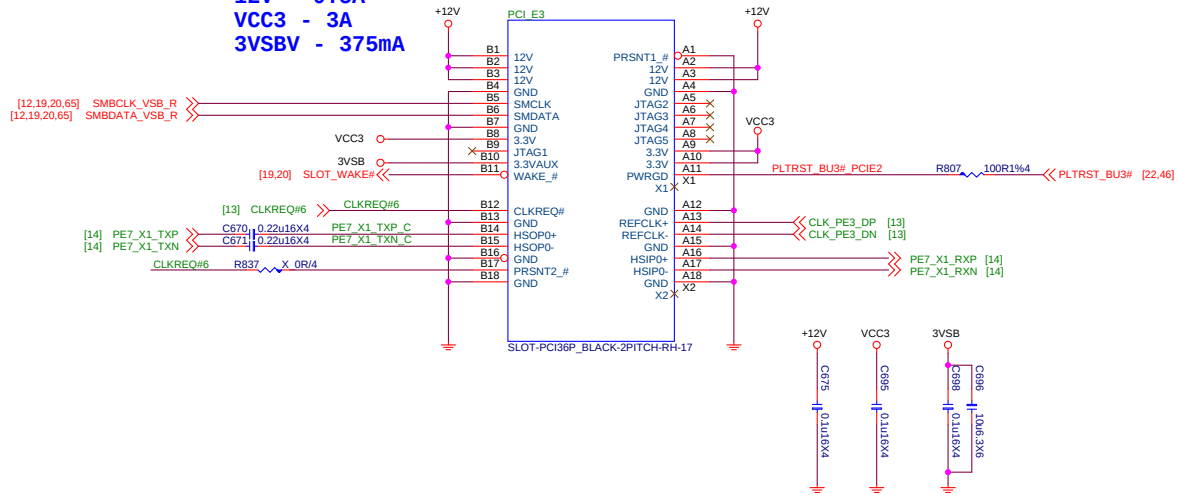


2020/10/27
The footprint of PCI_E2 is changed from SLOT_PCIEXP100_3 to SLOT_PCIEXP66P by PM spec updated.



MICRO-STAR INT'L CO.,LTD.		
Title: PCIE SLOT (X4)		
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 20 of 76	

12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



	MICRO-STAR INT'L CO.,LTD.	
Title	PCIE SLOT-PCH(X1)	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 21 of 76	

POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA
10	P80_EN	GPIO53	Default PORT80	Default GPI	3VA

2020/10/30
R476 is unstuffed and
R475 is stuffed by Pin
7,8,13 were NC
2020/10/30
R470 is stuffed 1Kohm and
R469 is unstuffed by same
as 7D10

change SPEC H disable L enable

190909:Add GPIO53 for PORT80 Strap

2020/8/7
R928 is stuffed by Robert's comment

for s0ix

Closed PIN1 Closed PIN46,85 Closed PIN99

RTCRST_DET

3V Analog Power

SPI ROM

15mA

DEBUG PORT

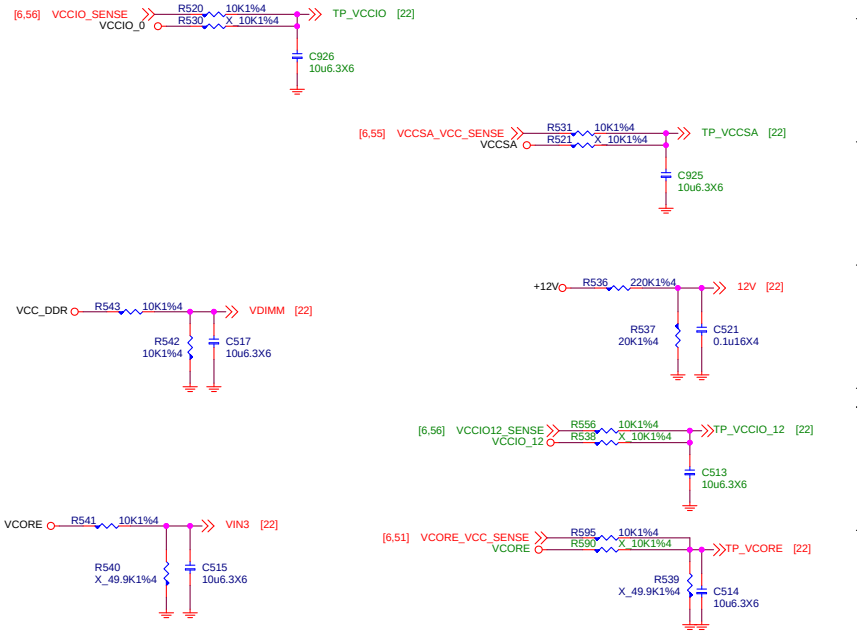
MX25V2033FM1I-HF

Title	SIO-NCT6687-1
Size	Document Number MS-7D15.. Rev 10/20
Date:	Tuesday, November 03, 2020 Sheet 22 of 76

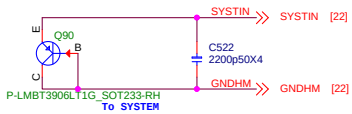
MICRO-STAR INT'L CO.,LTD.

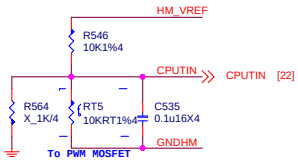
HW Monitor - Voltage

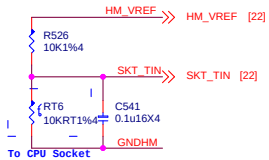
SIO HM Voltage Over 2V will Not Detect



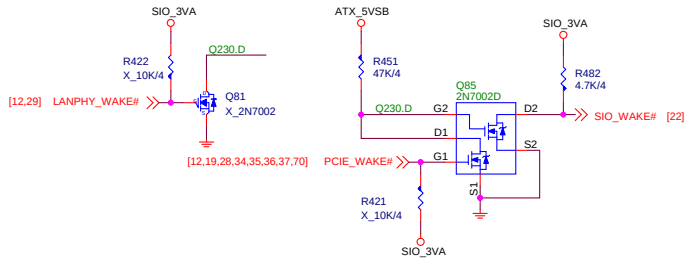
Thermal







for LAN wake



MICRO-STAR INT'L CO.,LTD.

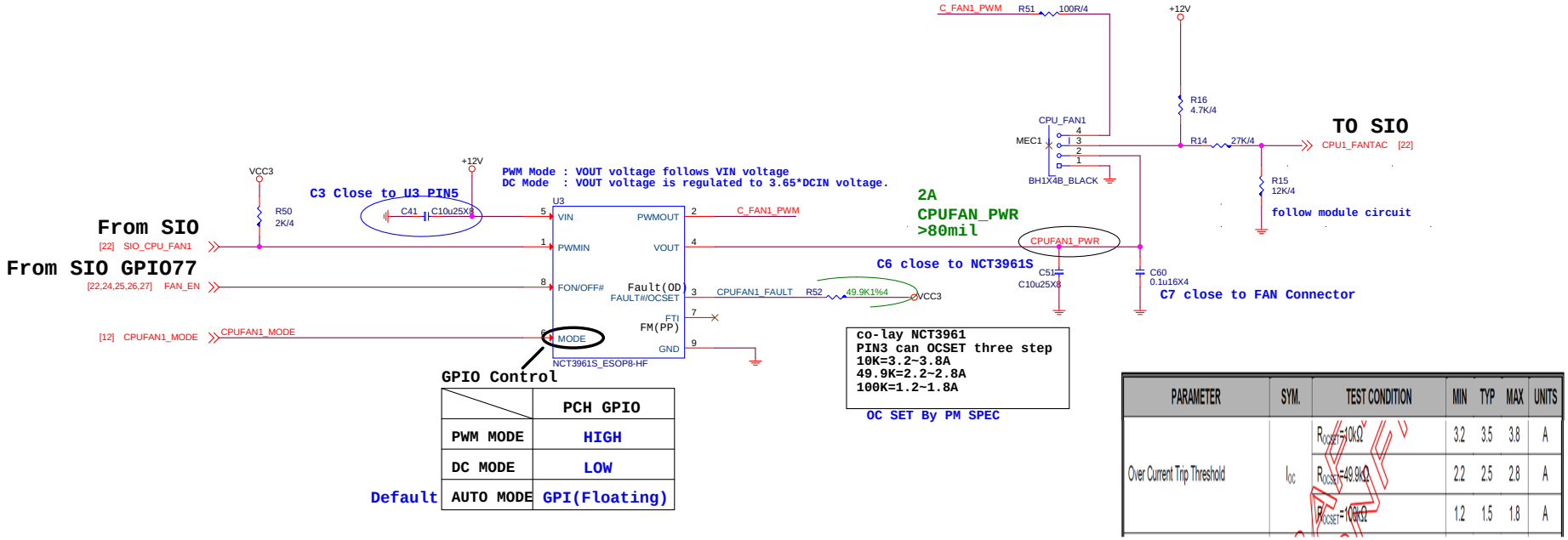
Title: SIO-NCT6687-2

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 23 of 76

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

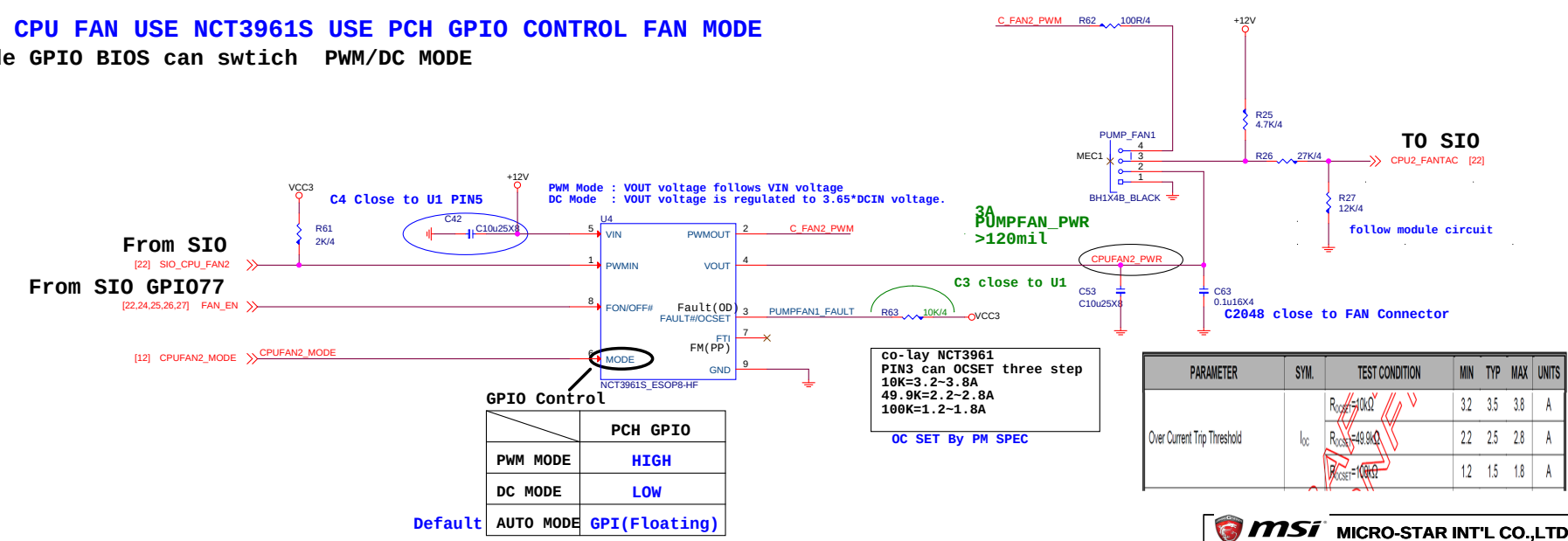


	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

PARAMETER	SYM.	TEST CONDITION	MIN	TYP	MAX	UNITS
Over Current Trip Threshold	I_{OC}	R_{OCSET}=10kΩ	3.2	3.5	3.8	A
		R_{OCSET}=49.9kΩ	2.2	2.5	2.8	A
		R_{OCSET}=100kΩ	1.2	1.5	1.8	A

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

PARAMETER	SYM.	TEST CONDITION	MIN	TYP	MAX	UNITS
Over Current Trip Threshold	I_{OC}	R_{OCSET}=10kΩ	3.2	3.5	3.8	A
		R_{OCSET}=49.9kΩ	2.2	2.5	2.8	A
		R_{OCSET}=100kΩ	1.2	1.5	1.8	A

MICRO-STAR INT'L CO.,LTD.

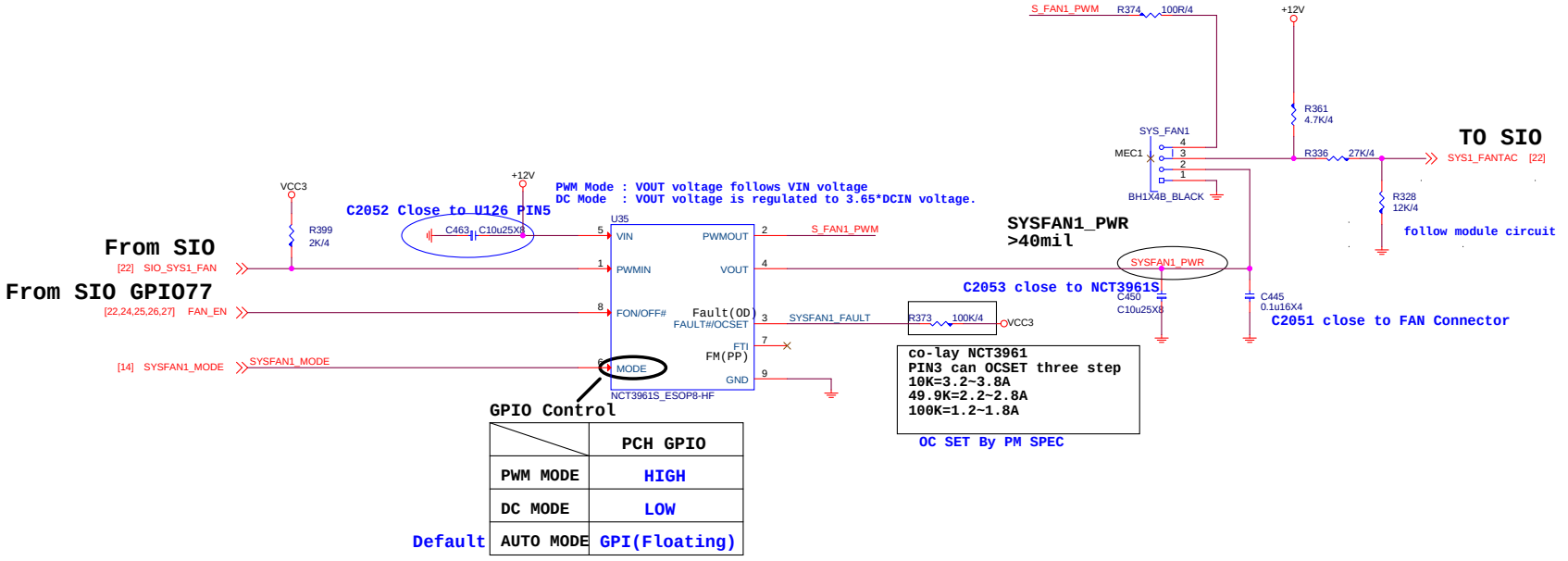
Title: CPU and PUMP FAN

Size | Document Number: MS-7D15.. | Rev: 10/20

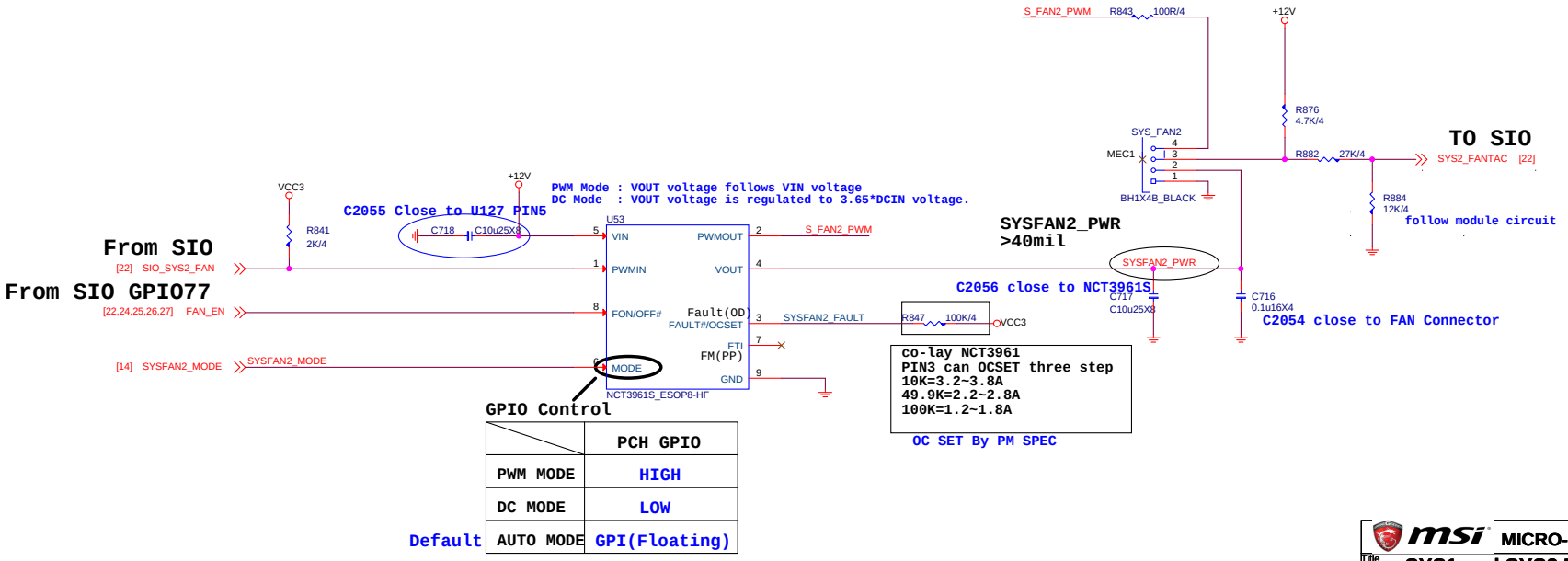
Date: Tuesday, November 03, 2020 | Sheet 24 of 76

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD.

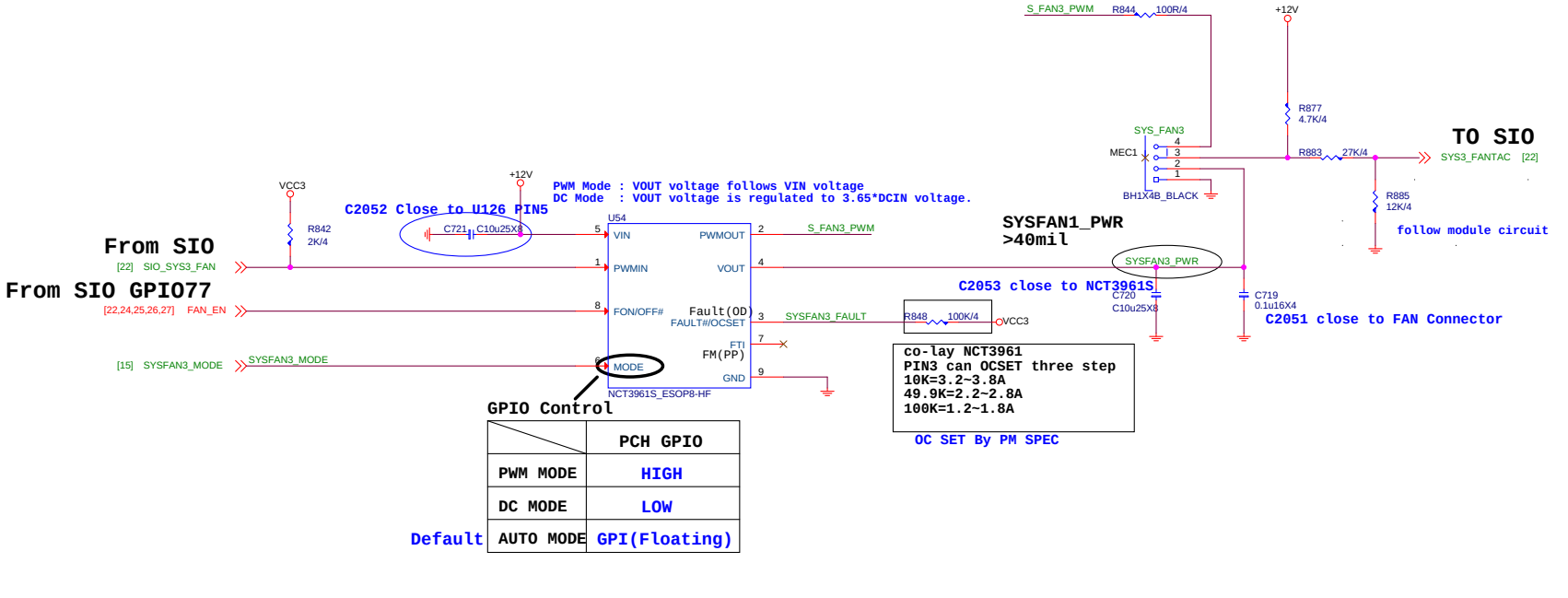
Title: SYS1 and SYS2 FAN

Size | Document Number: MS-7D15.. | Rev: 10/20

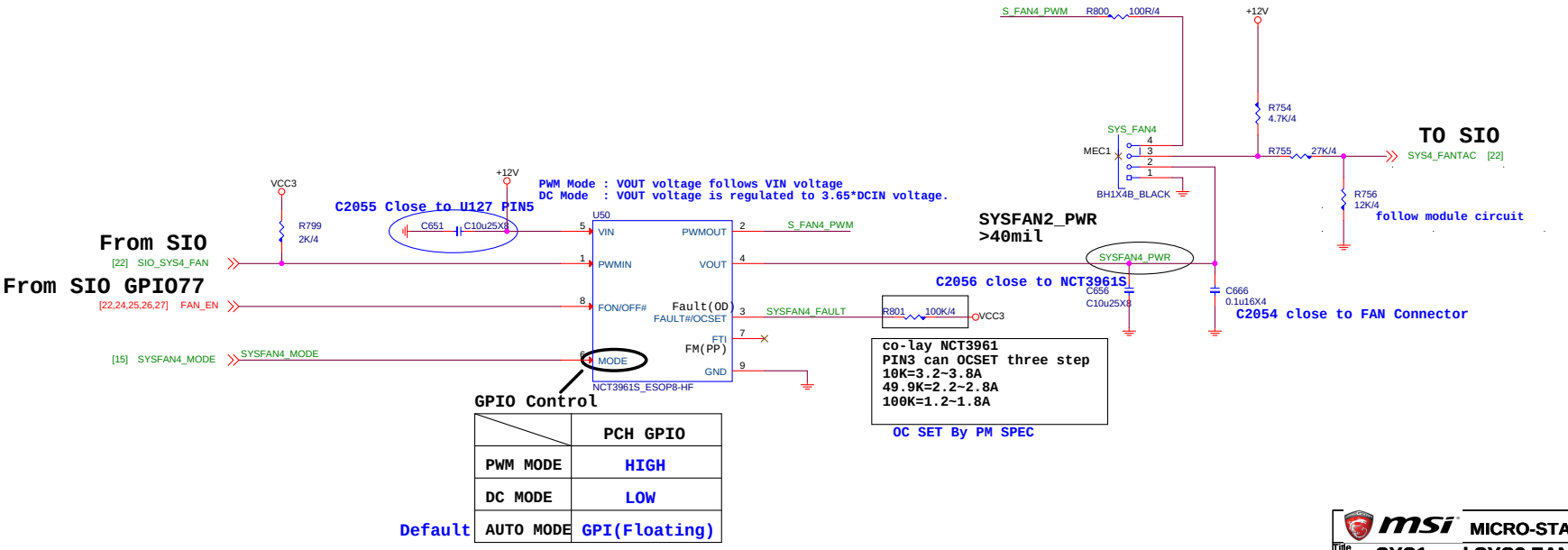
Date: Tuesday, November 03, 2020 | Sheet 25 of 76

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD.

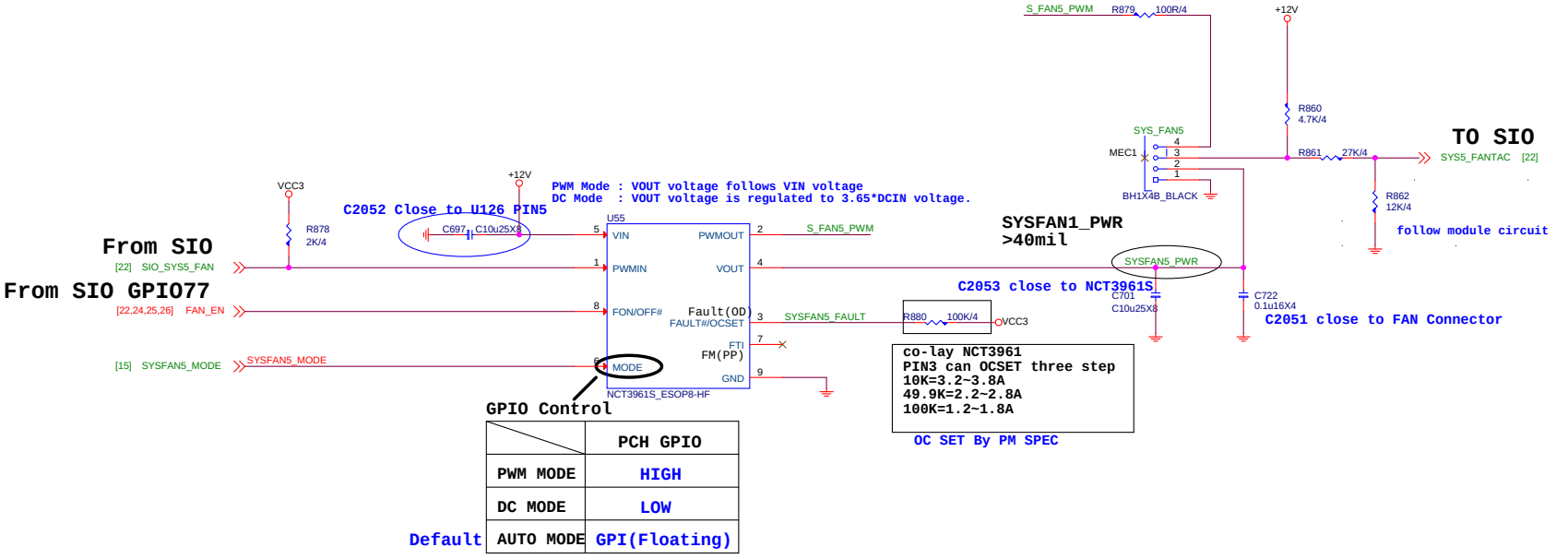
Title: SYS1 and SYS2 FAN

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 Sheet 26 of 76

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD.

Title: SYS5 FAN

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 Sheet 27 of 76

RTL8125B 10/100/1000/2.5G LAN Controller

For RTD3 Control ISOLATEB
ISOLATEB pull up Main Power,not aux power
check GPIO
if GPIO have power in S5/S4/S3 ->stuff RL32&RL34&QL457,RL33 NC

Under checking

pull up voltage need same with PCH_WAKE#

if RL13 stuff->DL2&RL37&RL38 NC

Place RL6 Close to IC

Pin49: 16 via from top layer to GND layer and make the via at the center of IC.

ESD Protect

UL3&UL4 close to connector

UL3 ESD-AOZ8S312BD4-03-HF

UL2 ESD-AOZ8S312BD4-03-HF

LAN Connector

LAN_USB1B

RJ45_USBX2_LEDX2-RH-42

Main:D0G-1020530-I05
AVL:D0G-8010510-SI0

2020/8/11
CHOKE24 is changed from L04-24B7070-M09 to L04-24B7060-T15 by Ivy's comment

0.95V / 0.65A

2020/8/31
The footprint of LAN_USB1 used to N58-32F0911-S42 by PM request

2020/9/4
LAN_USB1 changed from N58-32F0891-F02 to N58-32F0911-S42 by PM spec updated

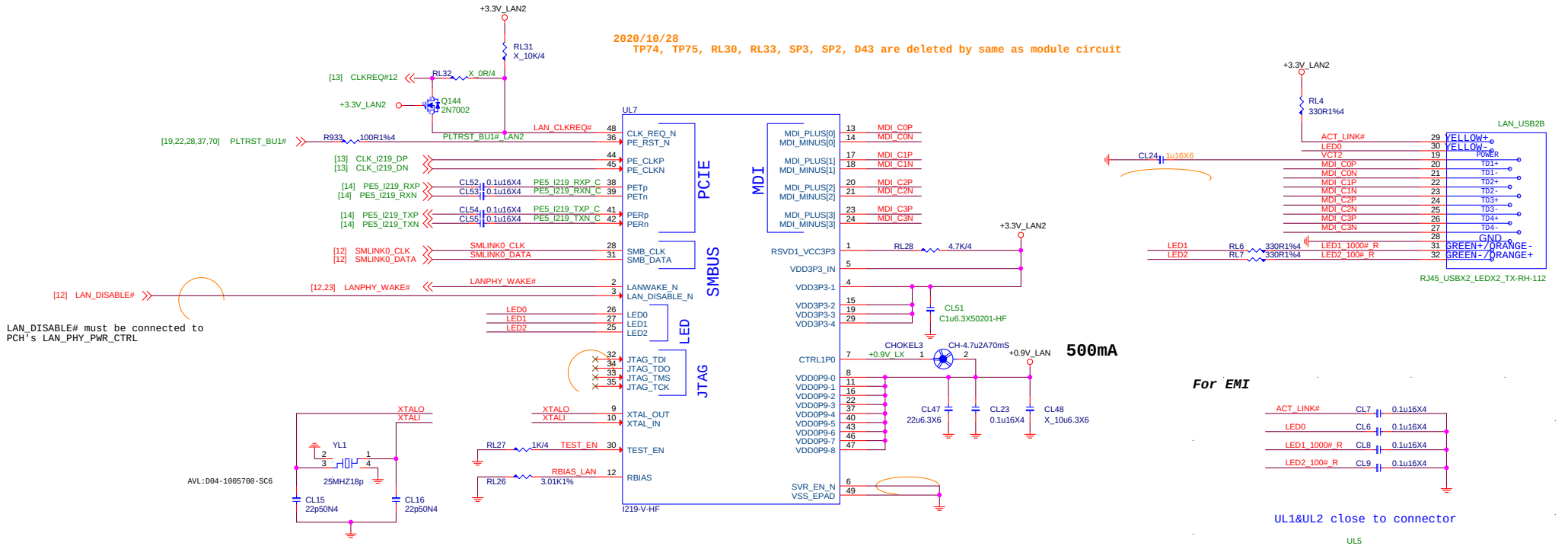
MICRO-STAR INT'L CO.,LTD.			
Title: LAN RTL8125B			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 28 of 76		

Option BOM for 2.0 only

Intel Lan2- i219

LAN Connector

2020/10/28
TP74, TP75, RL30, RL33, SP3, SP2, D43 are deleted by same as module circuit

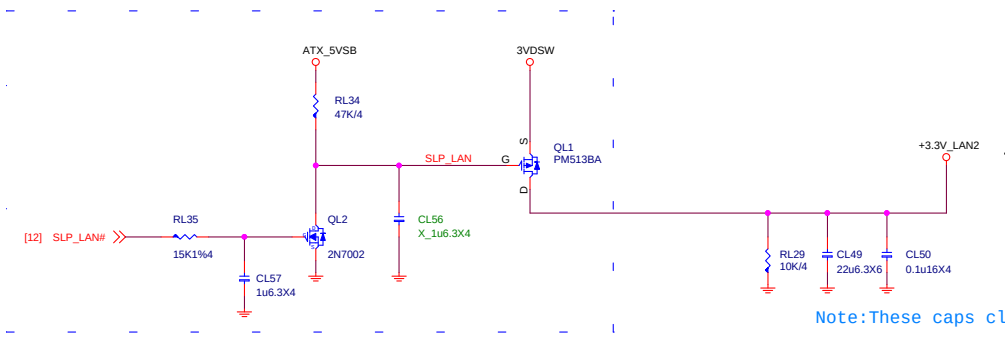


LAN_DISABLE# must be connected to
PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

The 10Kohm pull-up resistor (RL16) of CLK_REQ_N
is connected to 3.3V Suspend/Core/etc.
power well, depending on the power well
of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



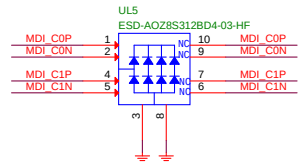
+3.3V_LAN2

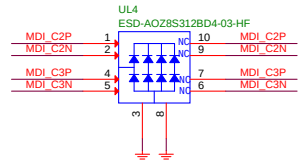
I218:132mA
I219:542mW

Note:These caps closed to PHY

For EMI

UL1&UL2 close to connector





Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue). Otherpairing combination is ok.

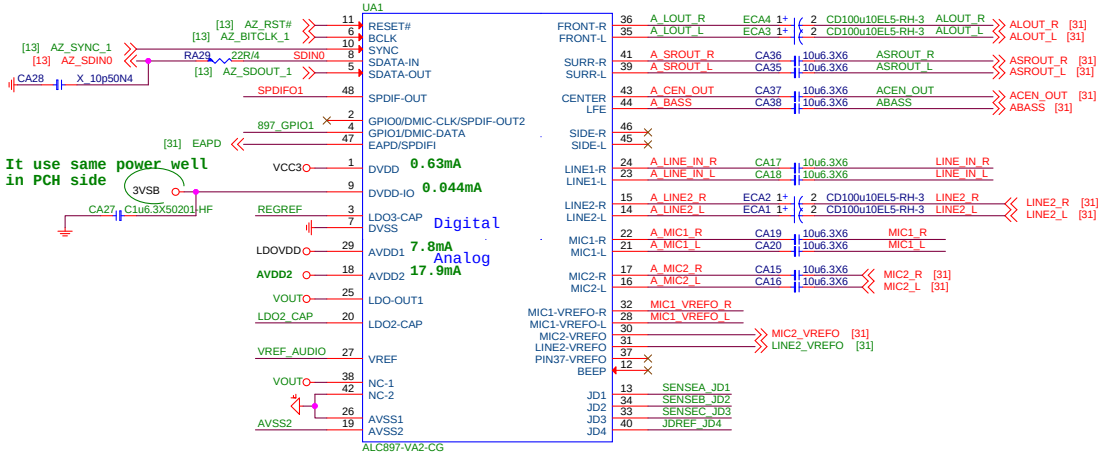
MICRO-STAR INT'L CO.,LTD.		
Title: Intel Lan- i219		
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 29 of 76	

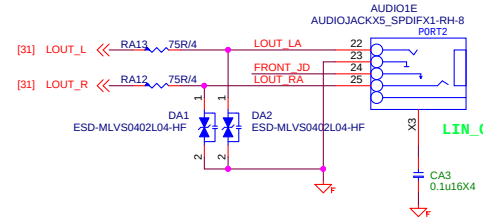
ALC897

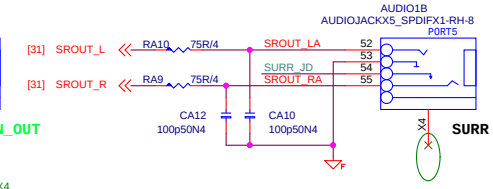
2020/8/12
UA1 is changed from B05-012000C-R09 to B05-012205C-R09 by PM spec updated
2020/8/19
UA1 is changed from B05-012205C-R09 to ALC897 by PM spec updated

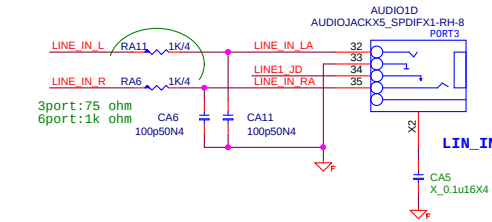
2020/7/17
The pin X1, X4 are changed from AGND to floating and CA46, CA47 are added for AUDIO1 by Ivy's comment

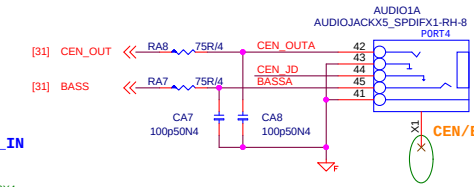
2020/9/18
CA46 is stuffed by EMI's suggestion

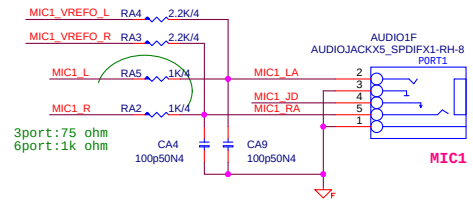


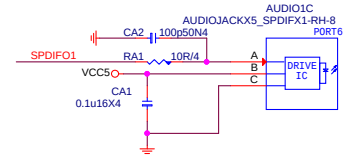


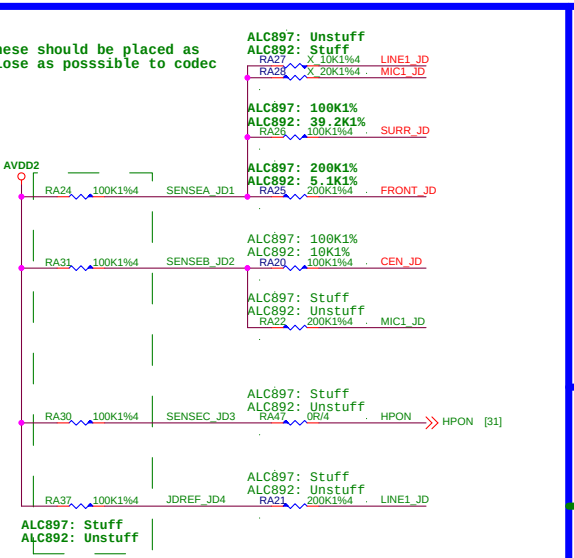


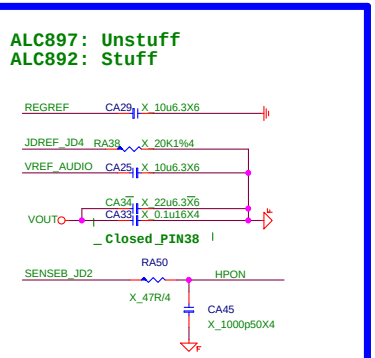


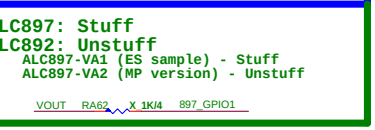




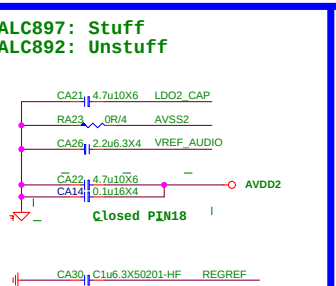


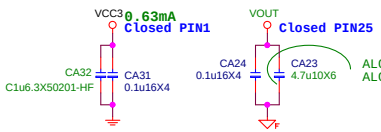


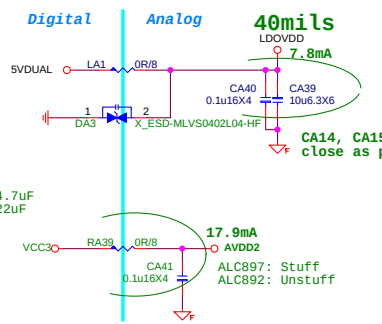


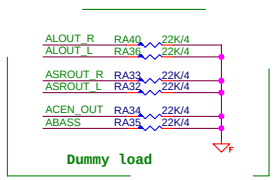


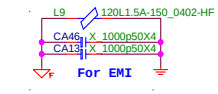
2020/10/16
UA1 is changed from OB5-7D10001-R09 to OB5-7D10002-R09
and RA62 is unstuffed by PM spec updated

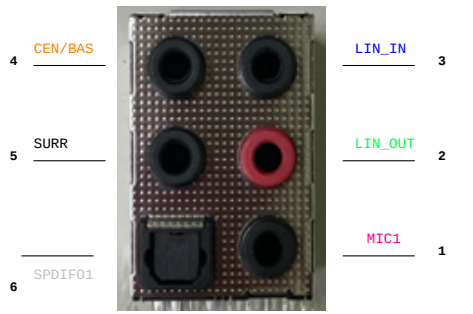






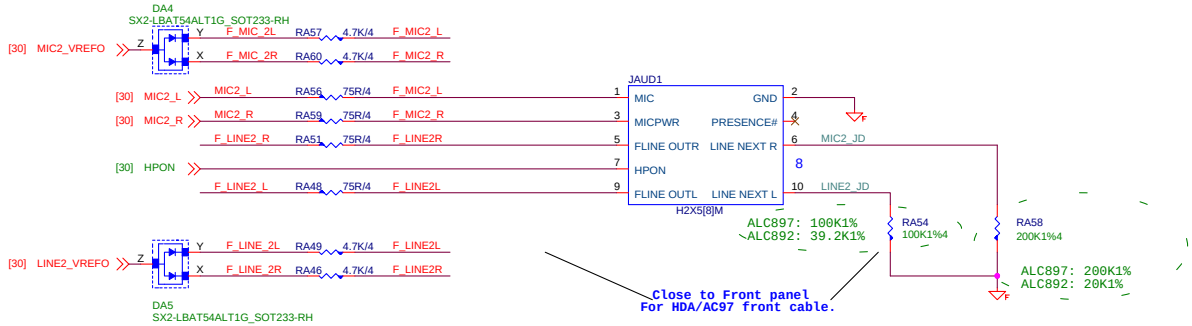






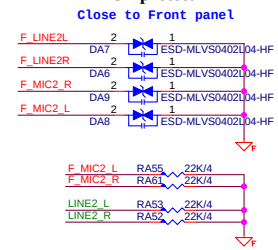
2020/8/28
CA11, CA12 are unstuffed because audio performance concern by vendor' suggestion

msi MICRO-STAR INT'L CO.,LTD.		
Title: AUDIO-ALC897-1		
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 30 of 76	



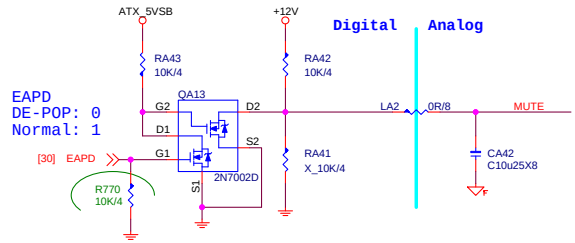
ESD protect

Close to Front panel

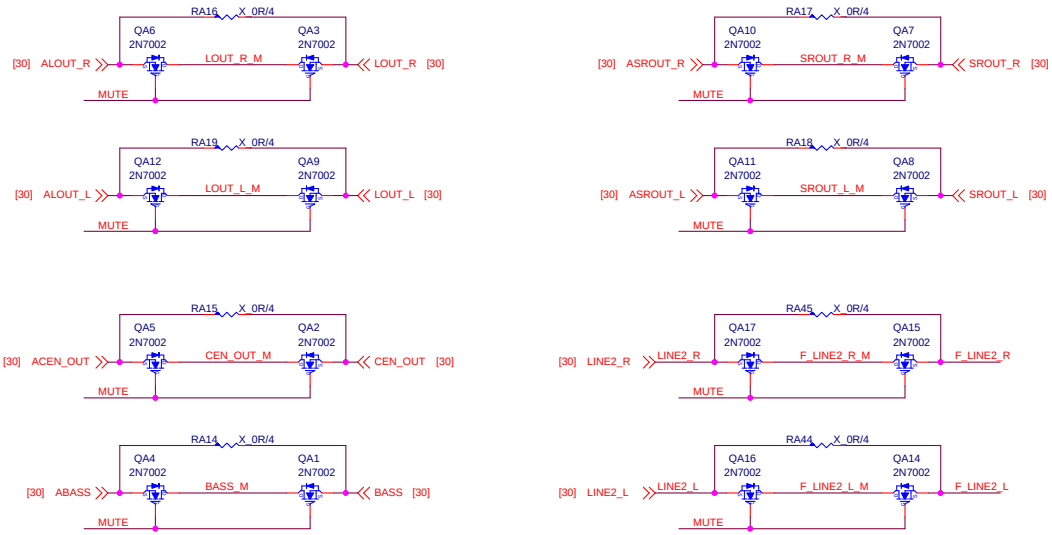


De-POP circuit

2020/7/17
de-pop is added by PM spec



2020/9/1
R2551 is added by vendor's comment

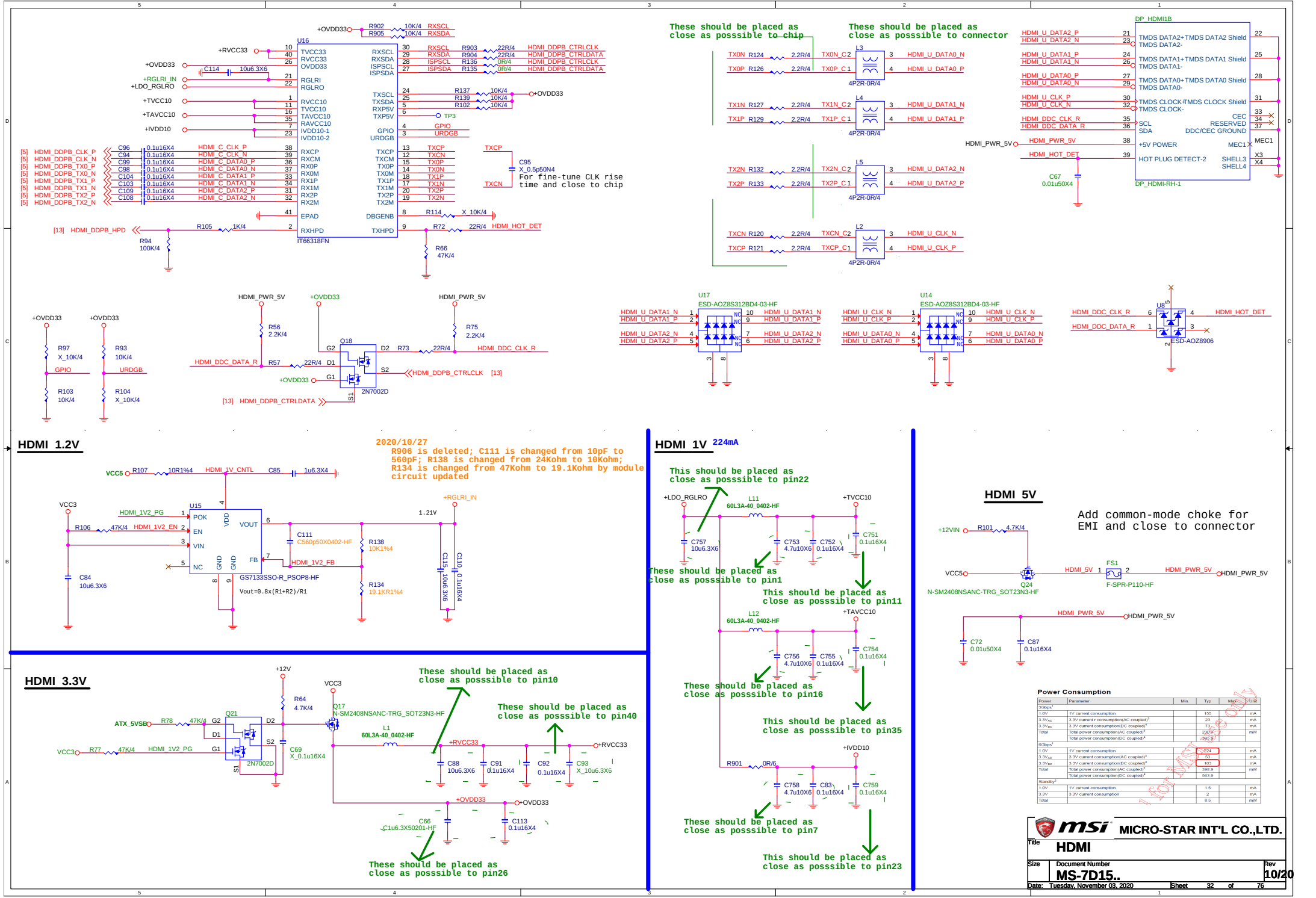


MICRO-STAR INT'L CO.,LTD.

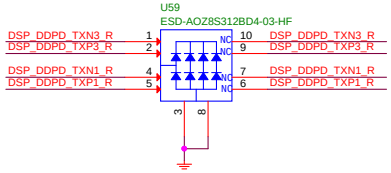
Title: AUDIO-ALC897-2

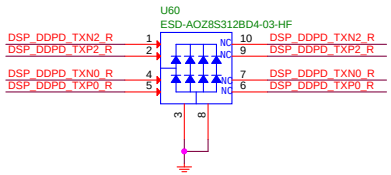
Size | Document Number: MS-7D15.. | Rev: 10/20

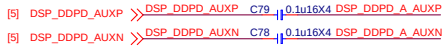
Date: Tuesday, November 03, 2020 | Sheet 31 of 76

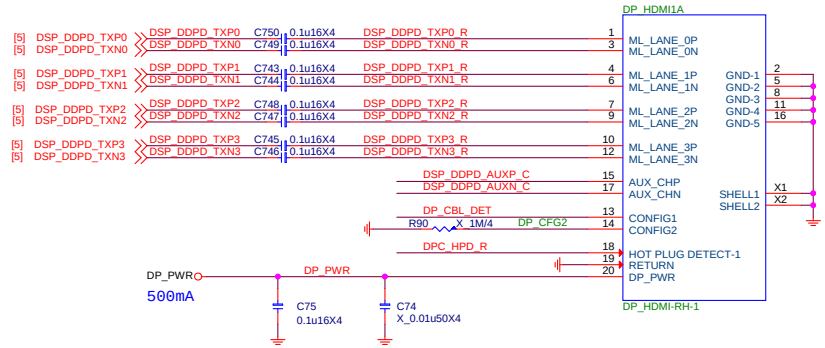

U16
IT66318FN
TVCC33
RVCC33
OVDD33
RGLRI
RGLRO
RVCC10
TVCC10
TAVCC10
RAVCC10
IVDD10-1
IVDD10-2
EPAD
RXHPD
RXSCL
RXSDA
ISPSCL
ISPSDA
GPIO
URDGB
TXCP
TXCM
TX0P
TX0M
TX1P
TX1M
TX2P
TX2M
DBGENB
TXHPD
RXCP
RXCM
RX0P
RX0M
RX1P
RX1M
RX2P
RX2M
TP3
HDMI_DDPB_HPD
HDMI_HOT_DET
HDMI_DDPB_CTRLCLK
HDMI_DDPB_CTRLDATA
HDMI_C_CLK_P
HDMI_C_CLK_N
HDMI_C_DATA0_P
HDMI_C_DATA0_N
HDMI_C_DATA1_P
HDMI_C_DATA1_N
HDMI_C_DATA2_P
HDMI_C_DATA2_N
These should be placed as close as posssible to chip
These should be placed as close as posssible to connector
DP_HDMI1B
DP_HDMI-RH-1
TMDS DATA2+
TMDS DATA2 Shield
TMDS DATA2-
TMDS DATA1+
TMDS DATA1 Shield
TMDS DATA1-
TMDS DATA0+
TMDS DATA0 Shield
TMDS DATA0-
TMDS CLOCK+
TMDS CLOCK Shield
TMDS CLOCK-
CEC
RESERVED
DDC/CEC GROUND
SCL
SDA
+5V POWER
HOT PLUG DETECT-2
SHELL3
SHELL4
MEC1
HDMI_PWR_5V
HDMI_HOT_DET
U17
U14
ESD-AOZ8S312BD4-03-HF
ESD-AOZ8906
U8
Q18
2N7002D
HDMI_DDC_CLK_R
HDMI_DDC_DATA_R
HDMI 1.2V
2020/10/27
R906 is deleted; C111 is changed from 10pF to 560pF; R138 is changed from 24Kohm to 10Kohm; R134 is changed from 47Kohm to 19.1Kohm by module circuit updated
VCC5
HDMI_1V_CNTL
HDMI_1V2_PG
HDMI_1V2_EN
HDMI_1V2_FB
GS7133SSO-R_PSOP8-HF
Vout=0.8x(R1+R2)/R1
+RGLRI_IN
1.21V
HDMI 1V
224mA
This should be placed as close as posssible to pin22
This should be placed as close as posssible to pin1
This should be placed as close as posssible to pin11
This should be placed as close as posssible to pin16
This should be placed as close as posssible to pin35
This should be placed as close as posssible to pin7
This should be placed as close as posssible to pin23
L11
L12
60L3A-40_0402-HF
+LDO_RGLRO
+TVCC10
+TAVCC10
+IVDD10
HDMI 5V
Add common-mode choke for EMI and close to connector
+12VIN
FS1
F-SPR-P110-HF
N-SM2408NSANC-TRG_SOT23N3-HF
HDMI_PWR_5V
HDMI 3.3V
ATX_5VSB
+12V
+RVCC33
+OVDD33
These should be placed as close as posssible to pin10
These should be placed as close as posssible to pin40
These should be placed as close as posssible to pin26
Power Consumption
MICRO-STAR INT'L CO.,LTD.
Title
HDMI
Size
Document Number
MS-7D15..
Rev
10/20
Date: Tuesday, November 03, 2020
Sheet 32 of 76

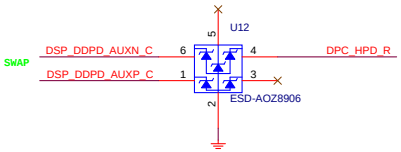
DP





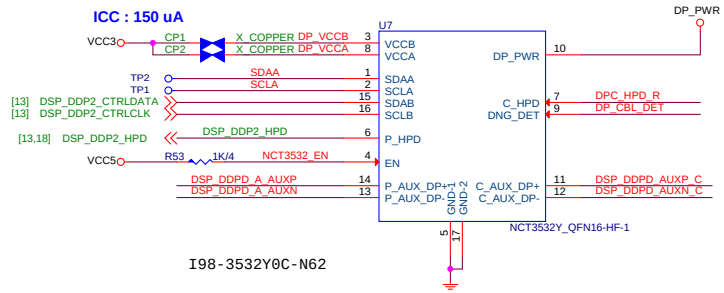




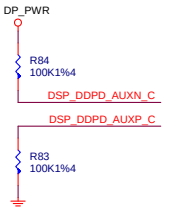


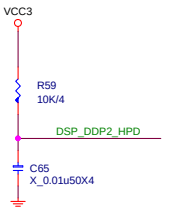
DP_VCCB trace don't less than 30 mil

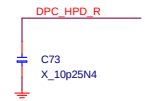
ICC : 150 uA

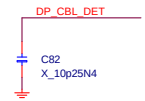


I98-3532Y0C-N62







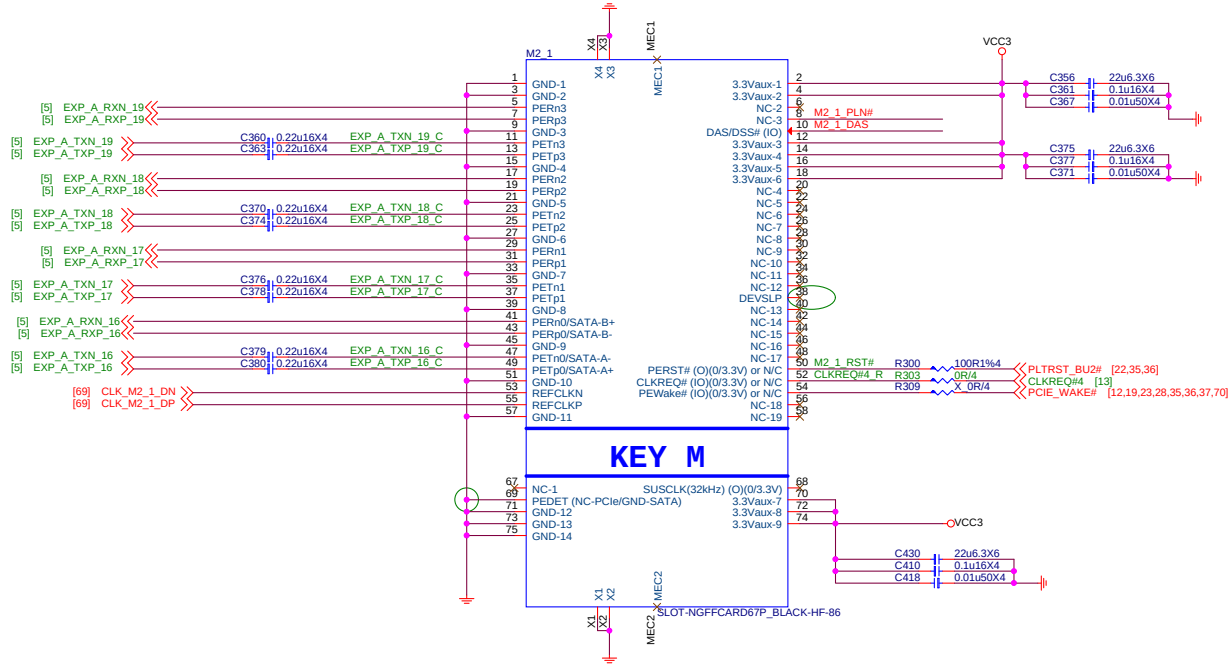


MICRO-STAR INT'L CO.,LTD.

Title: DisplayPort Connector

Size | Document Number: MS-7D15.. | Rev: 10/20

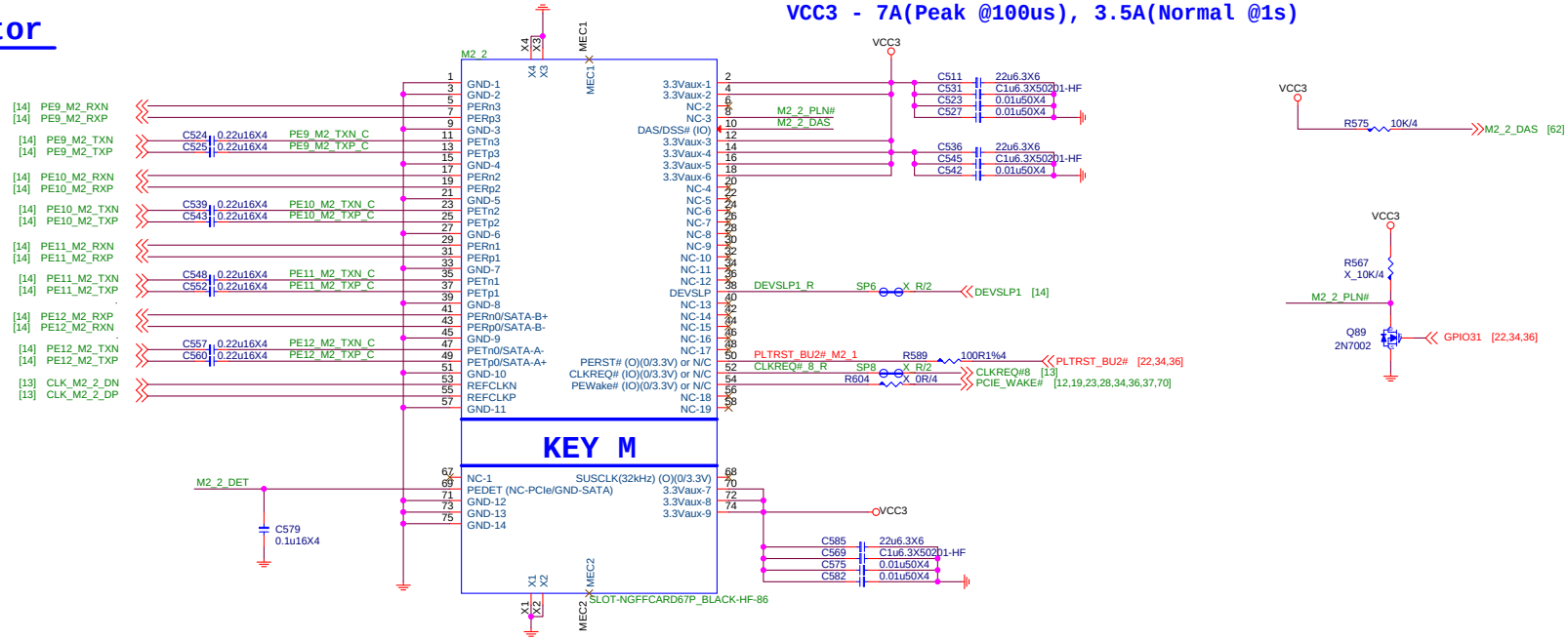
Date: Tuesday, November 03, 2020 | Sheet 33 of 76

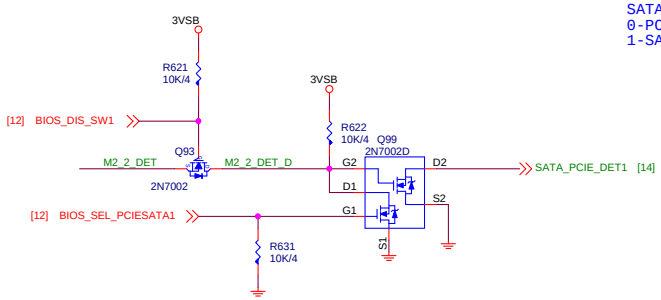


MICRO-STAR INT'L CO.,LTD.		
Title: M.2-SLOT1		
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 34 of 76	

M.2 Connector

VCC3 - 7A(Peak @100us), 3.5A(Normal @1s)



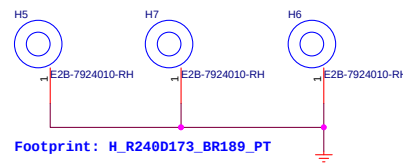


SATA_PCIE_DET0
0-PCIE
1-SATA

BIOS_MODE

BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

22 * 80



Footprint: H_R240D173_BR189_PT

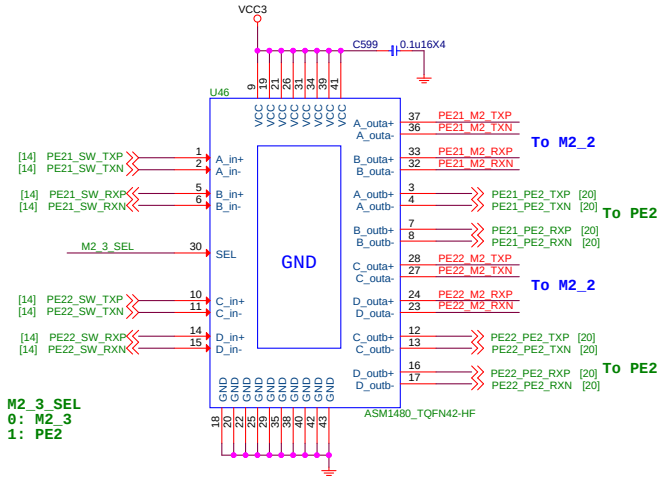
MICRO-STAR INT'L CO.,LTD.

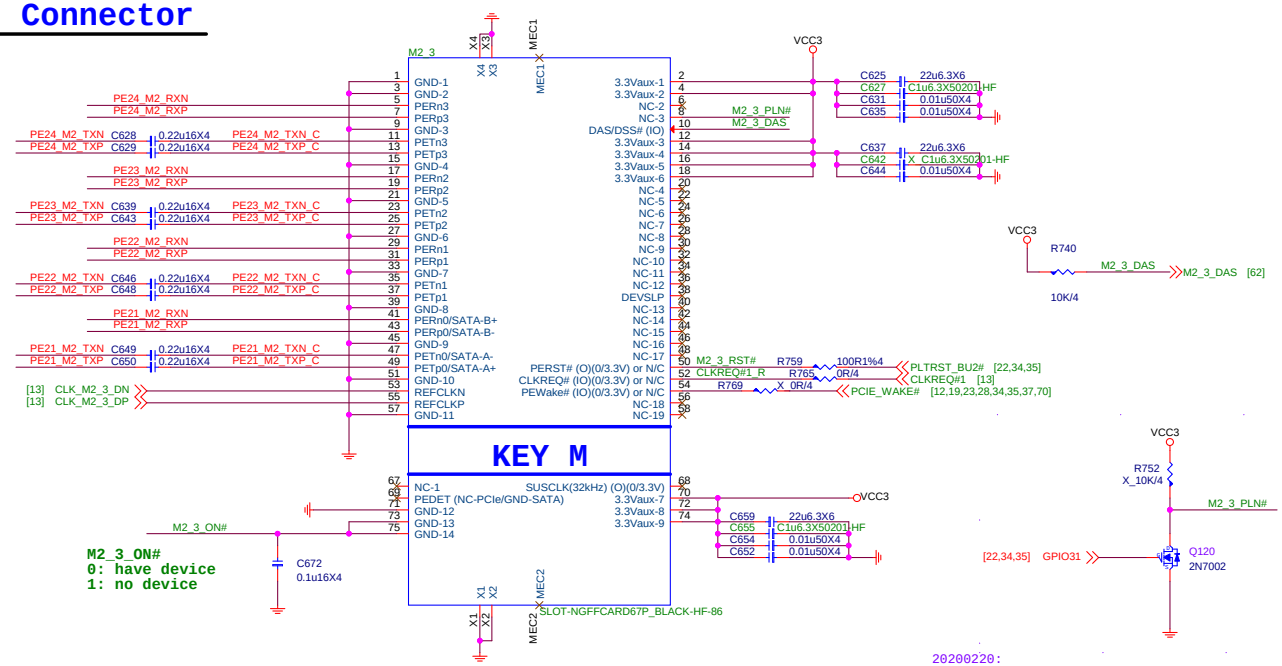
Title: M.2-SLOT2

Size | Document Number: MS-7D15.. | Rev: 10/20

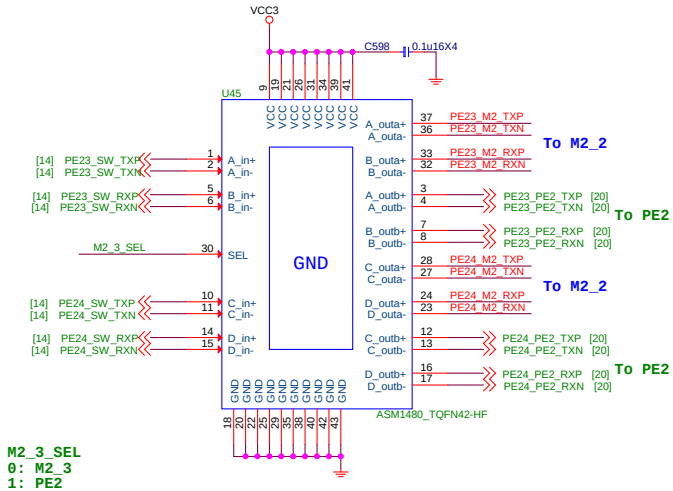
Date: Tuesday, November 03, 2020 | Sheet 35 of 76

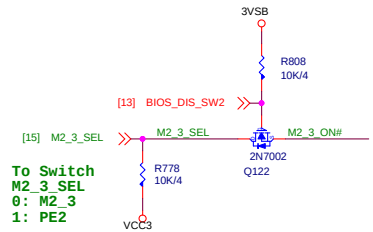
M.2 Connector





20200220:
follow 400 update, for NVMe SSD PLN fuction

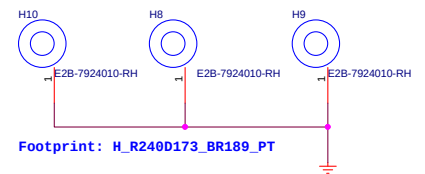


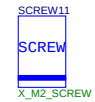


GPP_G7 GPP_G6

BIOS_DIS_SW2	M2_2_SEL	M.2_2_ON#	Mode
GPI(1)	GPI(1)	1	AUTO(PE3)
GPI(1)	GPI(0)	0	AUTO(M.2_2)
0	1		PE3
0	0		M.2_2-PCIE

22 * 80





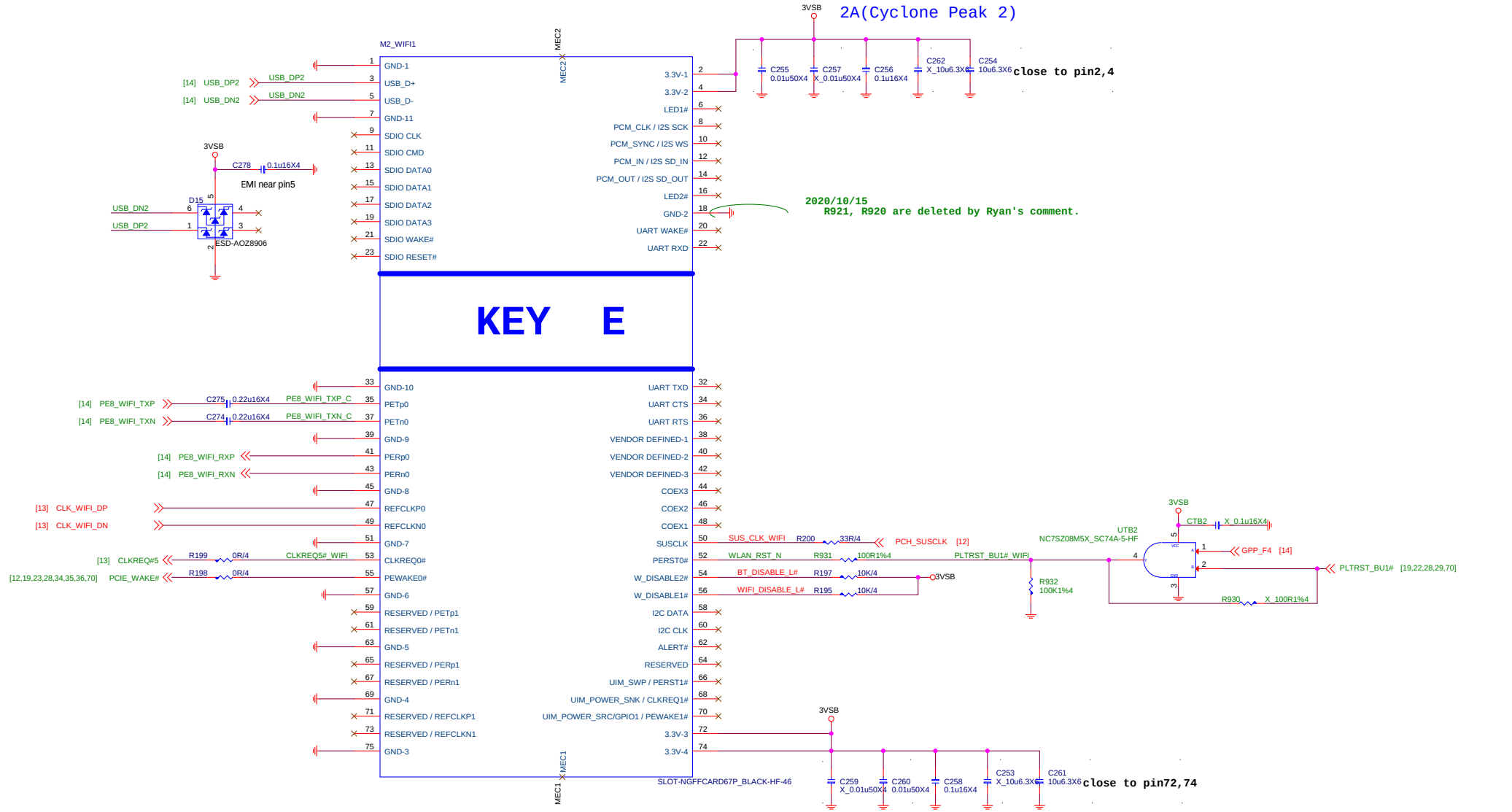
MICRO-STAR INT'L CO.,LTD.

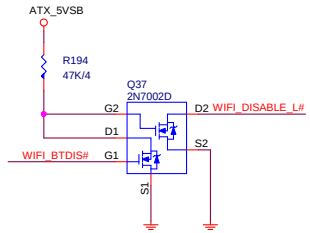
Title: M.2-SLOT3

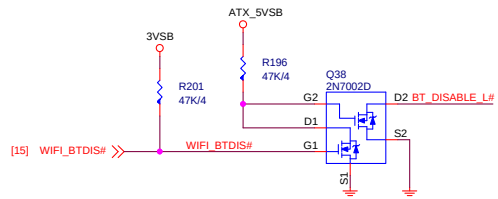
Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 36 of 76

Option BOM for 0A only







2020/10/20
SCREW5, SCREW6 are changed from E43-1204046-P65 to E43-1204008-P65 by PM spec updated

2020/10/22
SCREW5, SCREW6, WIRELESS1 are unstuffed by PM request

MICRO-STAR INT'L CO.,LTD.

Title: M2_WIFI

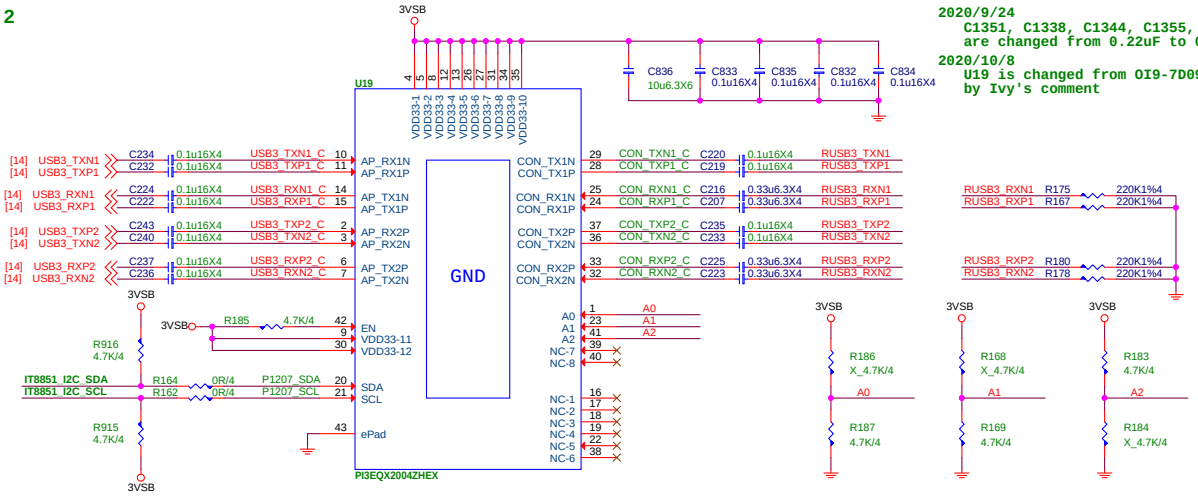
Size | Document Number: MS-7D15.. | Rev: 10/20

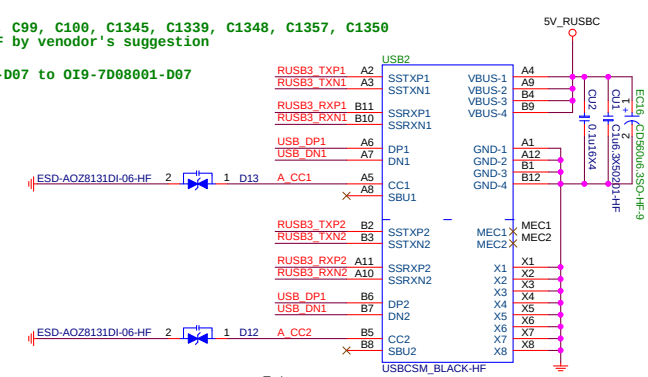
Date: Tuesday, November 03, 2020 | Sheet 37 of 76

Rear USB3.2 Gen2 x 2

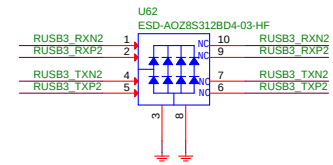
2020/9/24
C1351, C1338, C1344, C1355, C98, C99, C100, C1345, C1339, C1348, C1357, C1350 are changed from 0.22uF to 0.1uF by venodor's suggestion

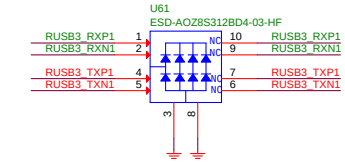
2020/10/8
U19 is changed from OI9-7D09002-D07 to OI9-7D08001-D07 by Ivy's comment

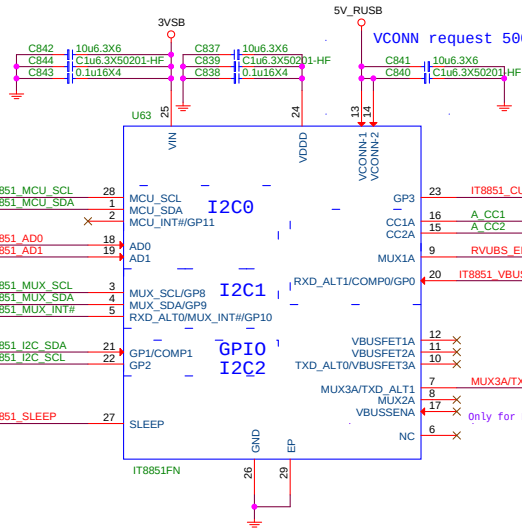




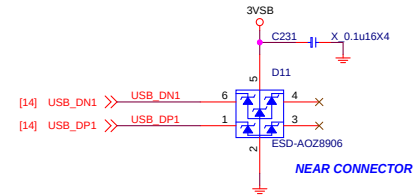
*Note:
A2/A1/A0 for I2C address selection



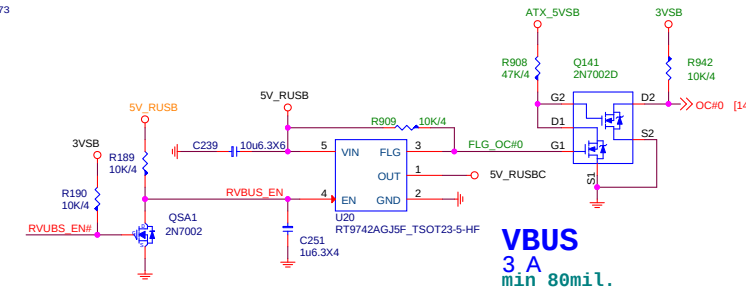




H:3A under S0 mode
L:1.5A under S3, S5 mode



if length too much , can use 0.1u solution.
test pass can remove.



	Pin No	Name	IN/OUT	Note
IT8851	7	MUX3A/TXD1	OUTPUT	TEST Point for Debug
	8	MUX2A	OUTPUT	NC
	9	MUX1A	OUTPUT	VBUS EN(Active Low)
	10	VBUSFET3A	OUTPUT	NC
	11	VBUSFET2A	OUTPUT	NC
	12	VBUSFET1A	OUTPUT	NC
	20	GP0	IN	VBUS_SENSE
	21	GP1	IN/OUT	GPIO I2C2 SDA to Re-driver
	22	GP2	IN/OUT	GPIO I2C2 CLK to Re-driver
	23	GP3	IN/OUT	NC
	1	MCU SDA0	I2C0	to PCH I2C for UcmCX
	28	MCU SDCL0	I2C0	to PCH I2C for UcmCX
	2	MCU_INT0#/GP11	I2C0	to PCH GPI for UcmCX
	3	MUX_SCL1	I2C1	to PCH SML1 for GEN2X2
	4	MUX_SDA1	I2C1	to PCH SML1 for GEN2X2
	5	MUX_INT#/GP10	I2C1	to PCH Alert for GEN2X2
	17	VBUSSENA	N/A	NC

Table 6-1. I2C0 Slave ID Decode

AD1	AD0	Slave ID
0	0	7'h40
0	1	7'h42
1	0	7'h50
1	1	7'h52

2020/10/27
R189.2 is changed from 5VDUAL to 5V_RUSB by circuit correctness

MICRO-STAR INT'L CO.,LTD.
Title: Rear USB3.2 Gen2 x 2
Size: Document Number: MS-7D15.. Rev: 10/20
Date: Tuesday, November 03, 2020 Sheet 38 of 75

USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)

2020/9/30
R2257, R2259 are stuffed 1Kohm by traces length from PI3EQX1004

EQ	dB	
L	12.4	1K to GND
R	8	68K to GND
F	10.6	NC
H	14.6	1K to VDD

FG	dB	
L	-1.6	1K to GND
R	-0.5	68K to GND
F	+1.0	NC
H	+2.7	1K to VDD

1104 suggest 0.1uF.

	7-bit High	7-bit Low	NC
F3220_ FPORT	ADD	0x67 DFP(V)	0x47 UFP GPIO mode(V) DRP

2020/8/27
R251, R250, R248, R249 are changed from 220Kohm to 200Kohm by vendor's comment

VBUS EN

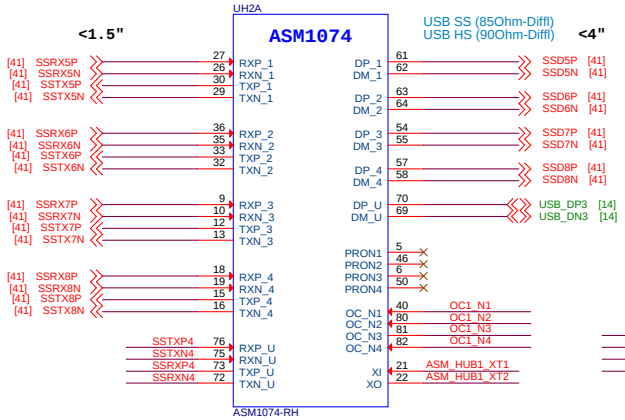
VBUS 3 A
min 80mil.

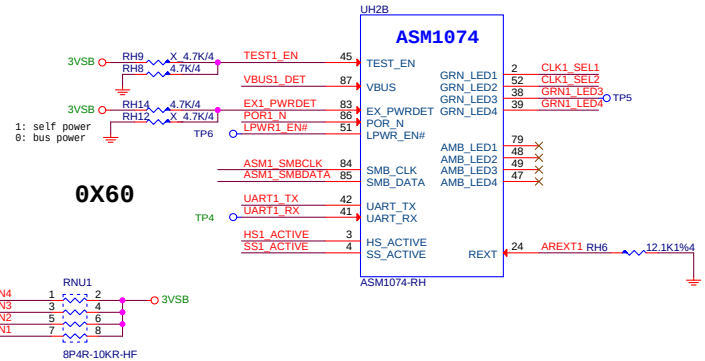
Current Mode

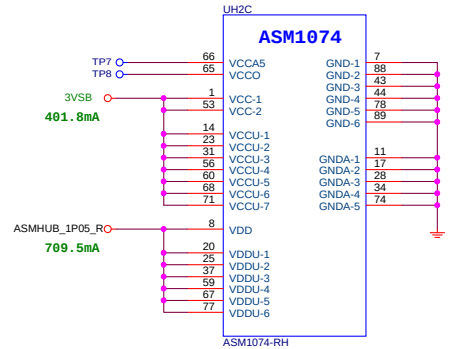
ESD Protection
NEAR CONNECTOR

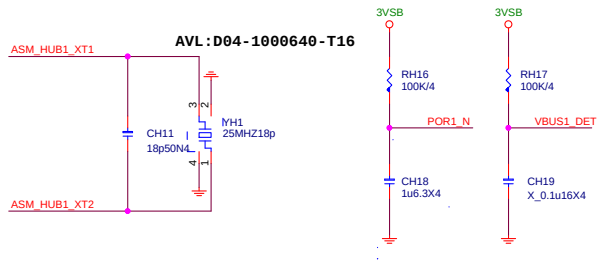
close to Type C Connector

MSI	MICRO-STAR INT'L CO.,LTD.
Title	Front TYPEC USB - JUSB2
Size	Document Number: MS-7D15.. Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 39 of 76



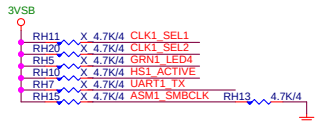






Stuff to meet ASM1074 power sequence.

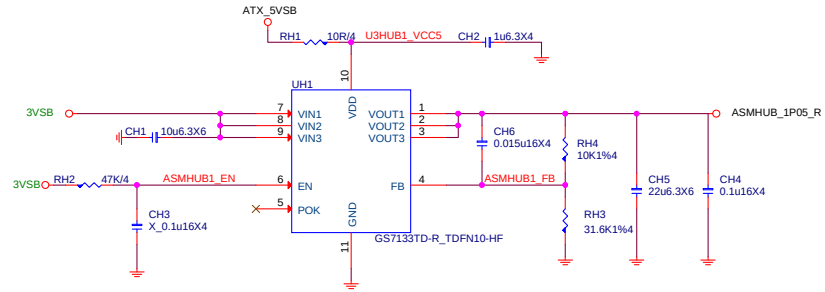
H/W Strapping



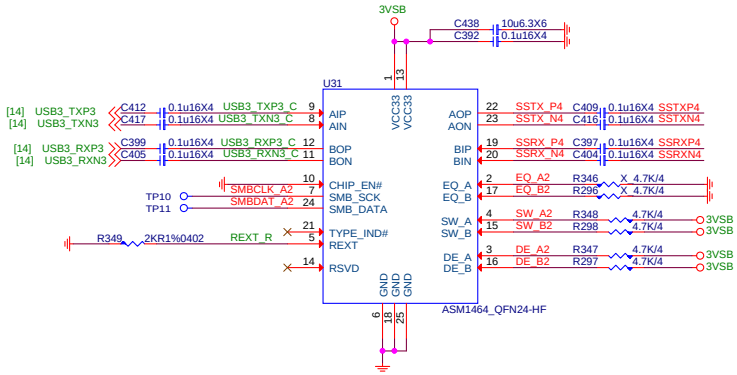
Strapping Table

GRN_LED2 (CLK_SEL1)	GRN_LED1 (CLK_SEL0)	
0	0	25MHz Default
1	0	30MHz
1	1	20MHz

ASM1074 USB3.0 HUB core Power

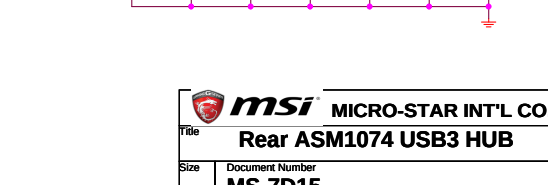


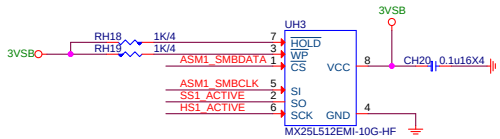
130mA



- **Disabling Power Saving Mode:**

Mode	Ports	VCC			VDD			Units
		Idle	Suspend	Run Junior	Idle	Suspend	Run Junior	
USB 3.0	USP	159	135.6	NA	215.7	183.3	NA	
USB2.0	Port 1	187.2	135.7	187.2	223.8	184.1	223.8	mA
	Port 1+2	210.8	135.7	210.7	227.4	185.4	229.1	mA
	Port 1+2+3	234.3	135.7	233.9	231.2	184.5	256.3	mA
	Port 1+2+3+4	257.7	135.7	257.2	235.1	186.3	261.1	mA
USB3.0	Port 1	151.7	128.1	151.6	290.3	186.4	292.4	mA
	Port 1+2	151.8	88.2	151.8	334.1	137.4	335.6	mA
	Port 1+2+3	147.8	84	147.8	388.2	139.4	388.1	mA
	Port 1+2+3+4	144.1	39.15	144.09	448.4	90.93	437	mA





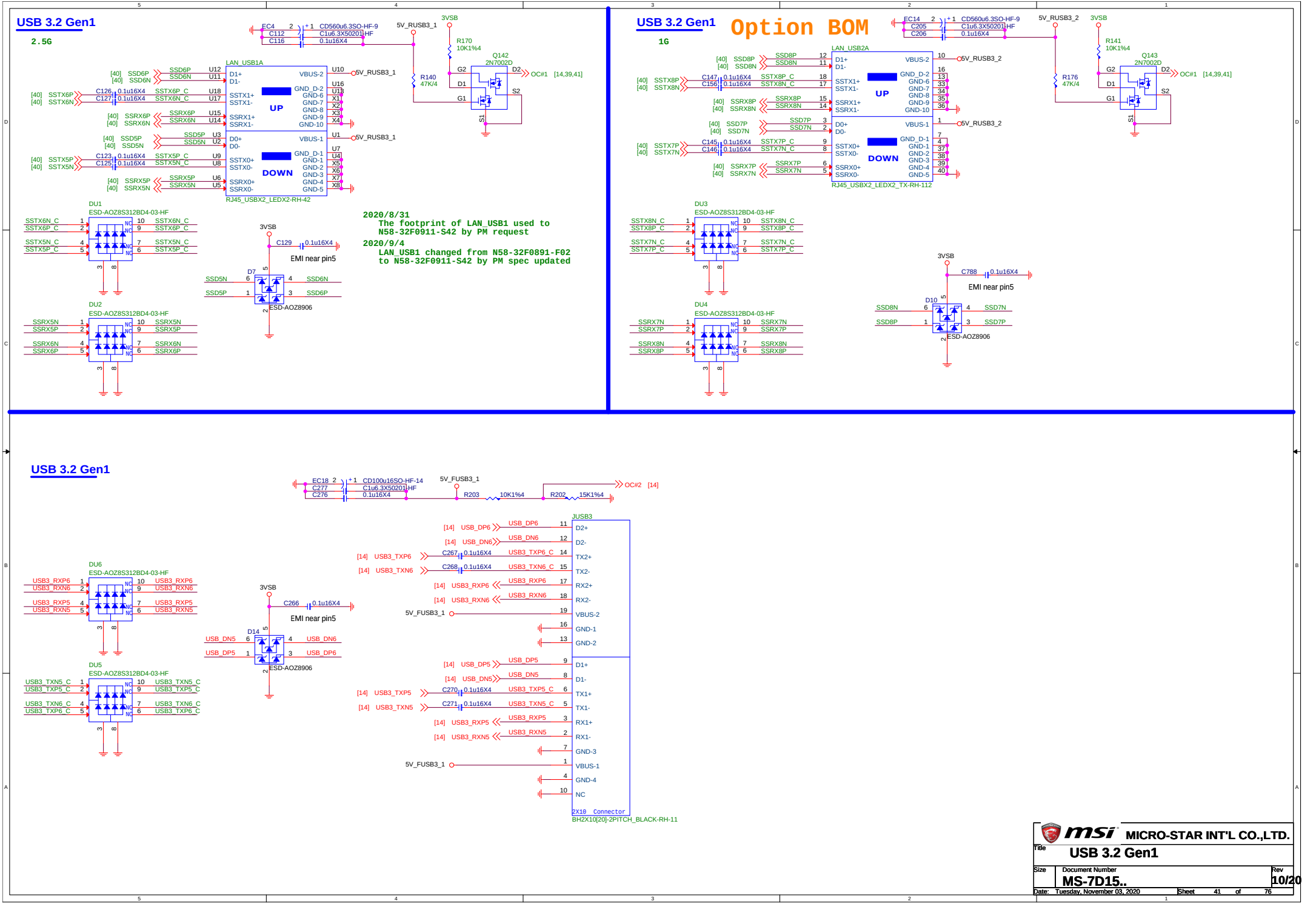
AVL:M31-25X0503-W03

MICRO-STAR INT'L CO.,LTD.

Title: Rear ASM1074 USB3 HUB

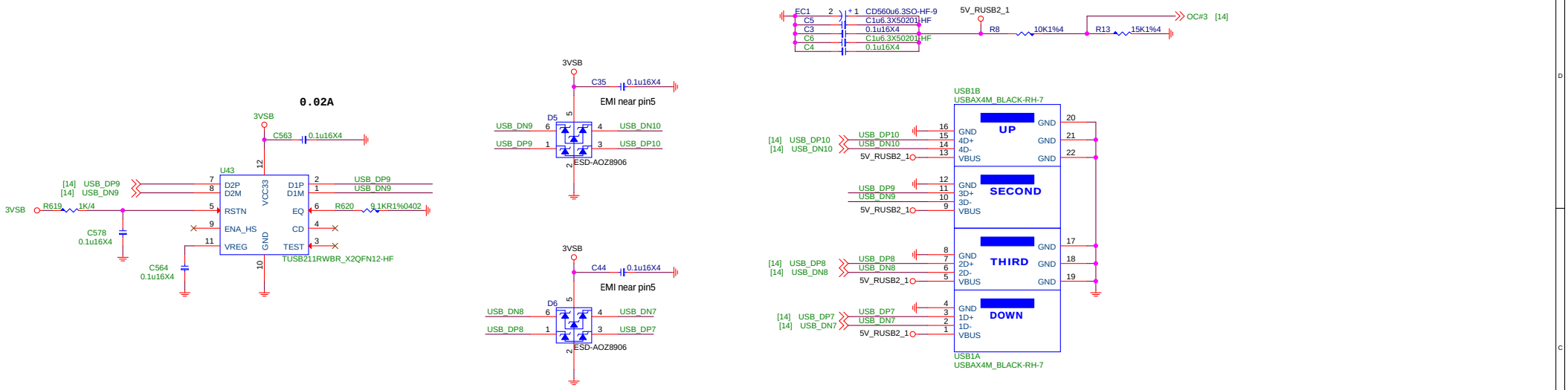
Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 40 of 76

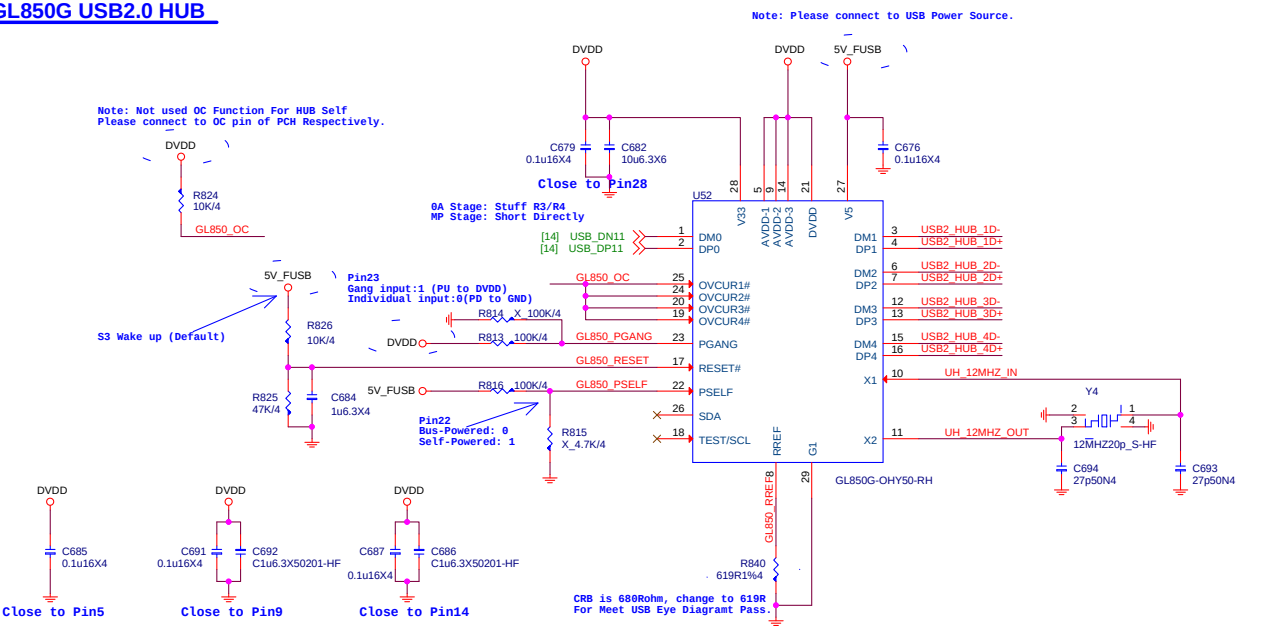


MSI MICRO-STAR INT'L CO.,LTD.			
Title: USB 3.2 Gen1			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 41 of 76		

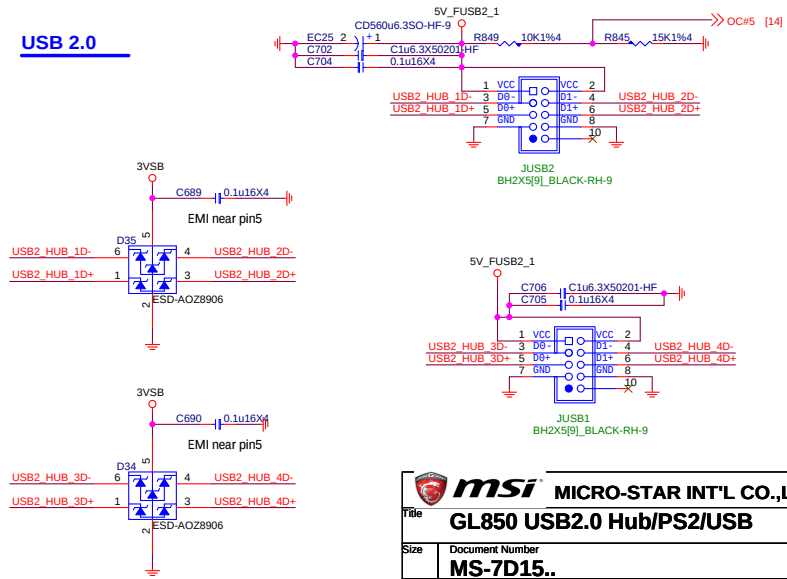
USB 2.0



GL850G USB2.0 HUB



USB 2.0

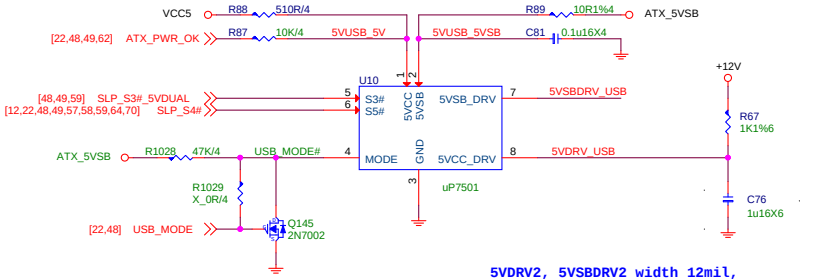


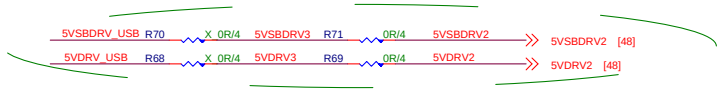
Title	MICRO-STAR INT'L CO.,LTD.	
	GL850 USB2.0 Hub/PS2/USB	
Size	Document Number	Rev
	MS-7D15..	10/20
Date: Tuesday, November 03, 2020	Sheet 42 of 76	

USB POWER

TO:NCT6779 GP72

H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3





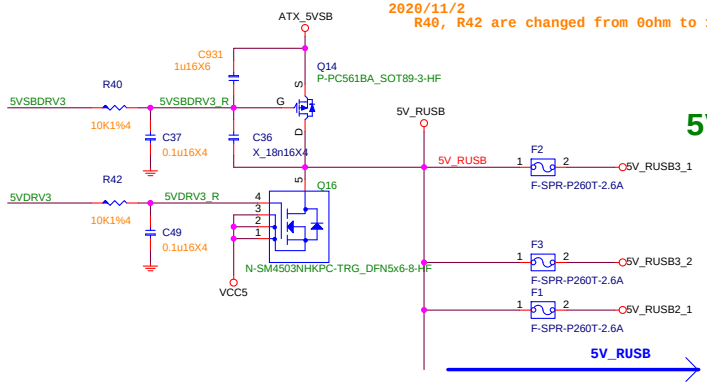
2020/10/8
Q145, R1029, R1028 are added by eSIO strap(default=high) from Robert's comment

5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

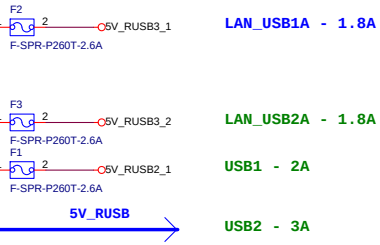
REAR USB PORT POWER

2020/11/2
C931 is reserved by James's comment

2020/11/2
R40, R42 are changed from 0ohm to 10Kohm/1%; C931 is stuffed 1uF; C37, C49 are stuffed 0.1uF by Robert's comment



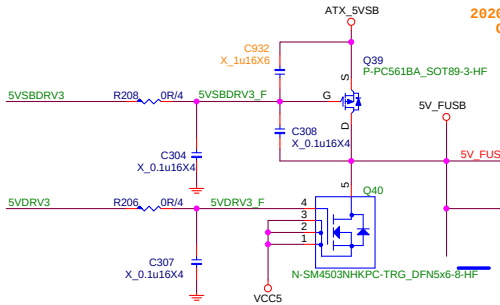
5V_RUSB:8.6A



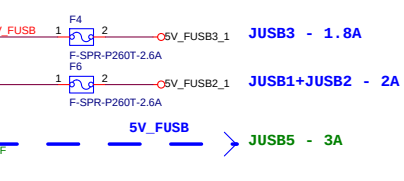
LAN_USB1A - 1.8A
LAN_USB2A - 1.8A
USB1 - 2A
USB2 - 3A

FRONT USB PORT POWER

2020/11/2
C932 is reserved by James's comment



5V_FUSB:6.8A



JUSB3 - 1.8A
JUSB1+JUSB2 - 2A
JUSB5 - 3A

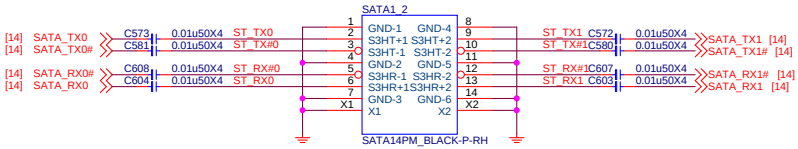
MICRO-STAR INT'L CO.,LTD.

Title: USB /PS2 Power

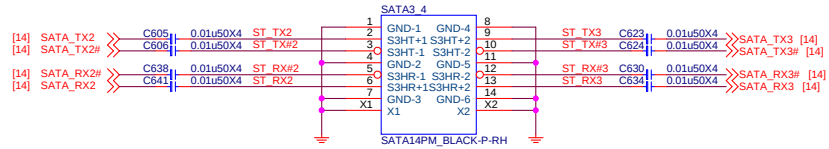
Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 43 of 76

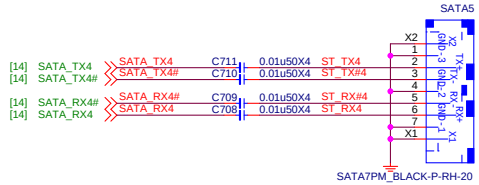
SATA 6G PORT 0.1

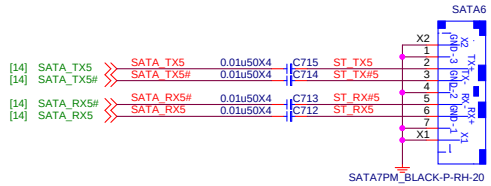


SATA 6G PORT 2.3



SATA 6G PORT 4.5





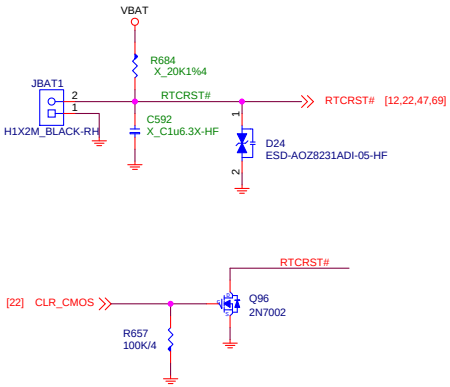
MICRO-STAR INT'L CO.,LTD.

Title: SATA CNT

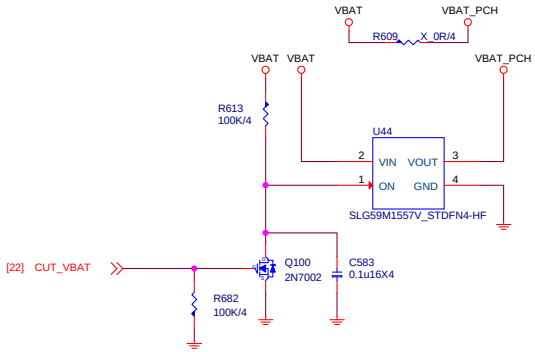
Size | Document Number: MS-7D15.. | Rev: 10/20

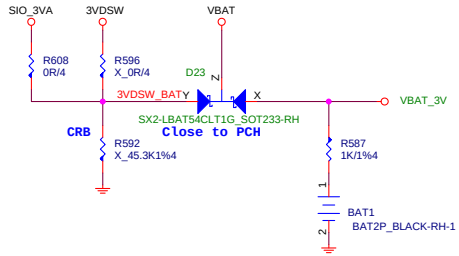
Date: Tuesday, November 03, 2020 | Sheet 44 of 76

CLR CMOS



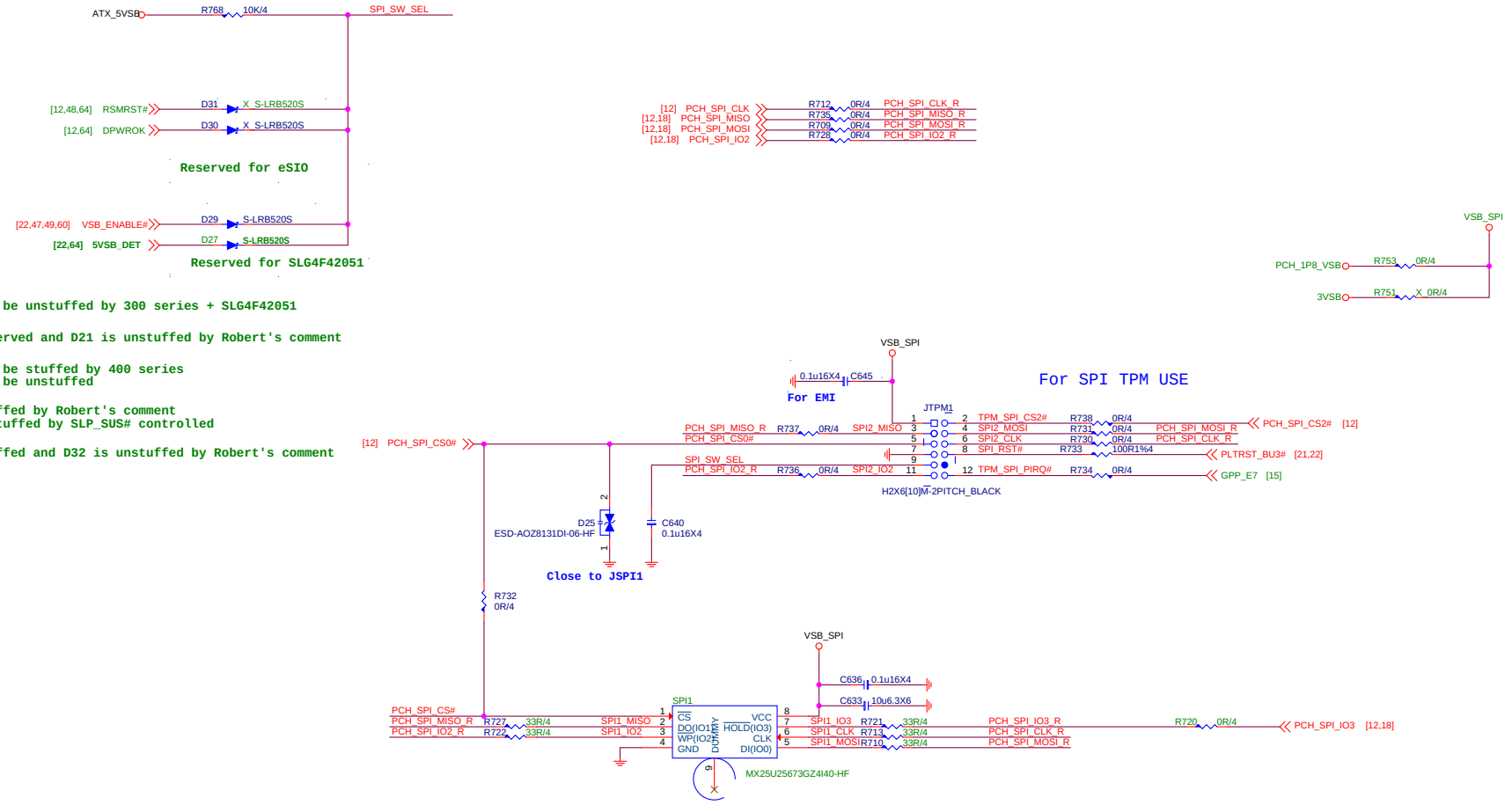
VBAT





MICRO-STAR INT'L CO.,LTD.

Title	Clear CMOS	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 45 of 76	



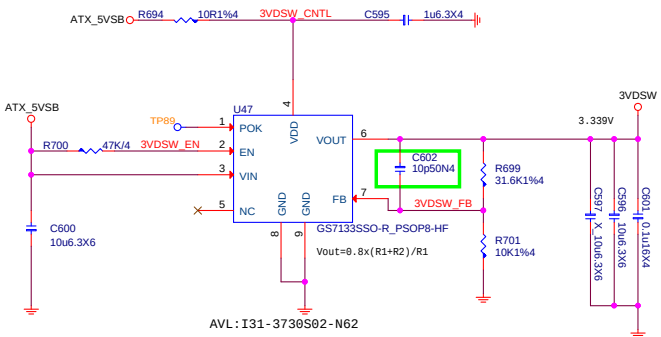
MICRO-STAR INT'L CO.,LTD.

Title: BIOS ROM

Size | Document Number: MS-7D15.. | Rev: 10/20

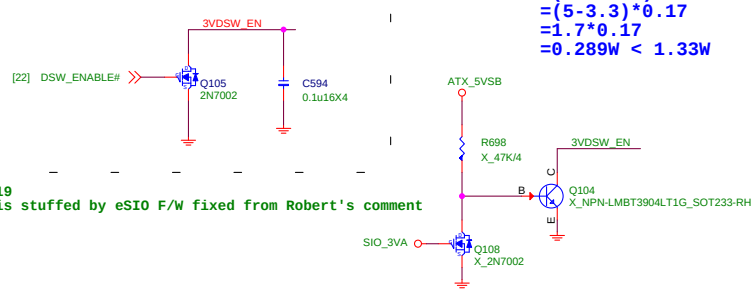
Date: Tuesday, November 03, 2020 | Sheet 46 of 76

3VDSW



AVL:I31-3730S02-N62

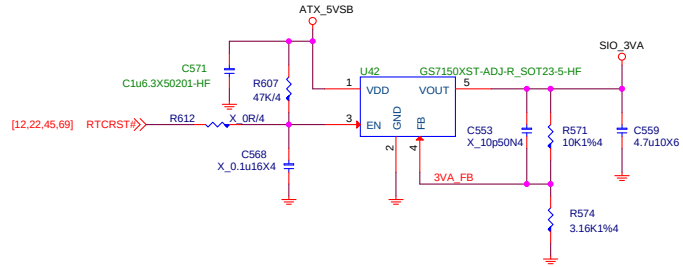
Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.17
=1.7*0.17
=0.289W < 1.33W



2020/10/19
Q105 is stuffed by eSIO F/W fixed from Robert's comment

SIO_3VA

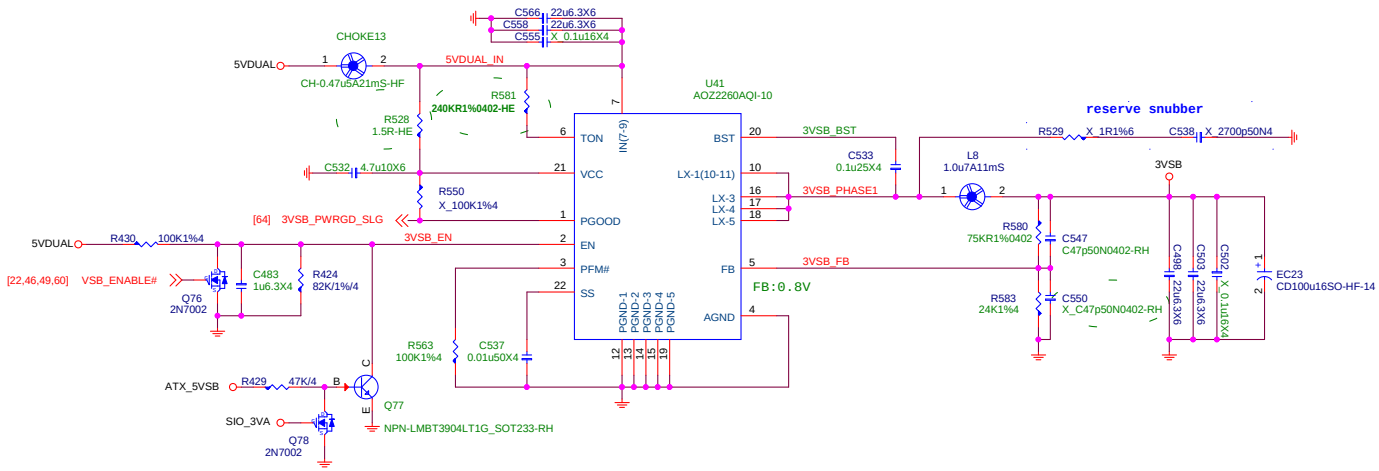
2020/7/8
U33 is changed from I31-7116S09-N03 to I31-7150X09-GA9 by Ivy's comment



SYS_3VSB

3.3V/4.992A

2020/9/21
R2557 is changed from 270Kohm to 240Kohm;
R2581 is added with 1.5ohm;
C1924 is reserved;
by vendor's suggestion



For S5-G3 3VSB EN issue

MICRO-STAR INT'L CO.,LTD.

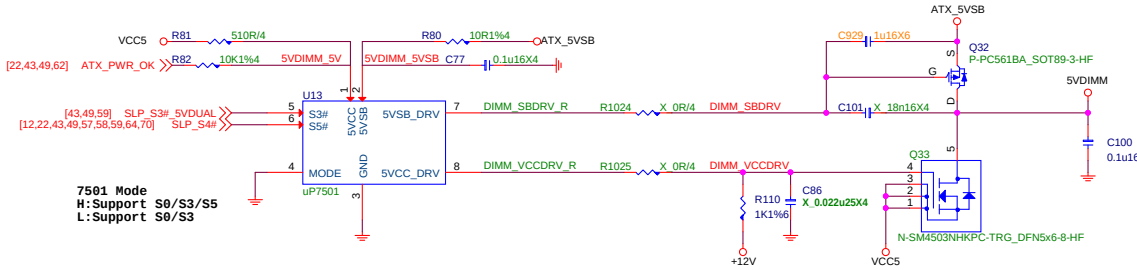
Title: 3VSB/3VDSW/SIO_3VA

Size | Document Number: MS-7D15.. | Rev: 10/20

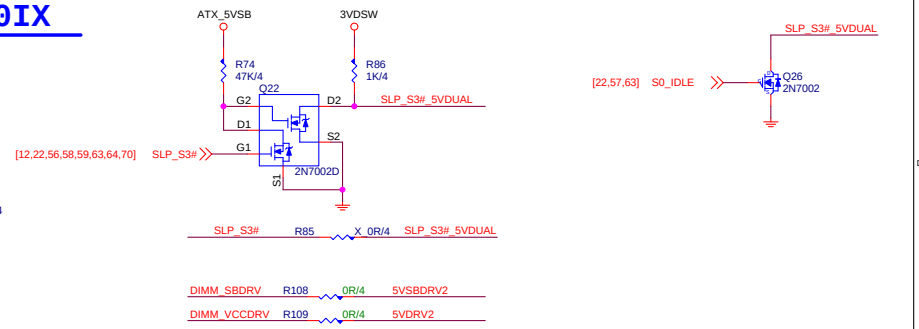
Date: Tuesday, November 03, 2020 | Sheet 47 of 76

5VDIMM FOR DDR

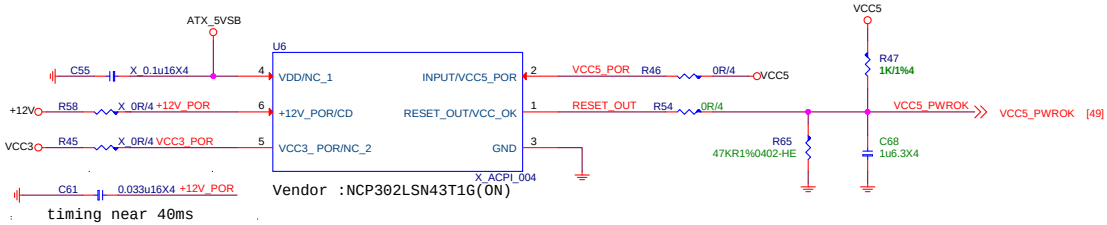
2020/10/16
C86 is stuffed by Robert's comment
2020/10/23
C101, C86 are unstuffed by James's comment
2020/10/30
C929 is added 1uF by James's comment



S0IX



5VDIMM COLAY



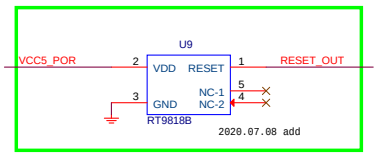
Vendor :NCP302LSN43T1G(ON)

timing near 40ms

PIN6 CAP for fine tune RESET_OUT dealy time use
When INPUT rising up to 4.3V(Vth) level besides delay 35ms~40ms send Reset Output

	SLP_S5#	SLP_S3#	USB_MODE	5VSB_DRV2	5VSBDRV2
S3	1	0	0	1	0 (PMOS on)
S4/S5	0	0	0	0	1 (PMOS off)
S0/First	1	1	0	0	1 (PMOS off)
S0/First	X	1	1	0	1 (PMOS off)
S3/S4/S5	X	0	1	1	0 (PMOS on)

USB MODE

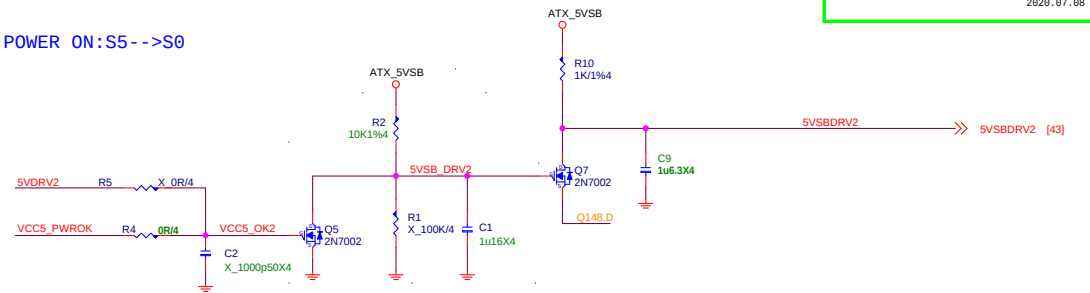


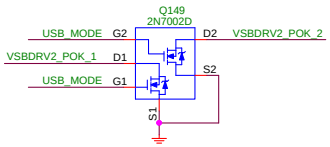
control P-MOS soft start and waiting ATX_5VSB ramp to 100%

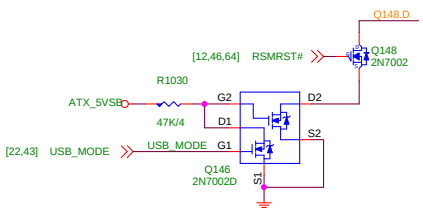
2020/10/16
Q3, R3, Q1, Q4 are deleted; C9 is stuffed 0.1uF; C1 is changed from 0.022uF to 1uF; C10 is changed from 0.1uF to 1uF; C8 is unstuffed; Q149, Q147, R1033, C928, R1031, R1032, C927, Q148, Q146, R1030 are added; R2, R4, R11 are changed from 10Kohm/5% to 10Kohm/1%; R47 is changed from 1Kohm/5% to 1Kohm/1%; R6 is changed from 100Kohm/5% to 100Kohm/1%; R65 is changed from 47Kohm/5% to 47Kohm/1% by Robert's comment

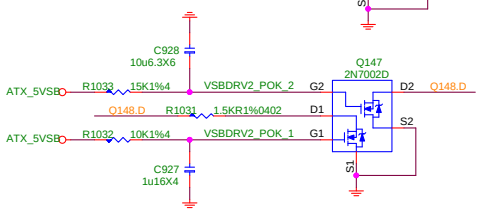
2020/10/23
C8 is stuffed 1uF; C9 is changed from 0.1uF to 1uF; R4 is changed from 10Kohm to 0ohm; C2 is unstuffed; by James's comment

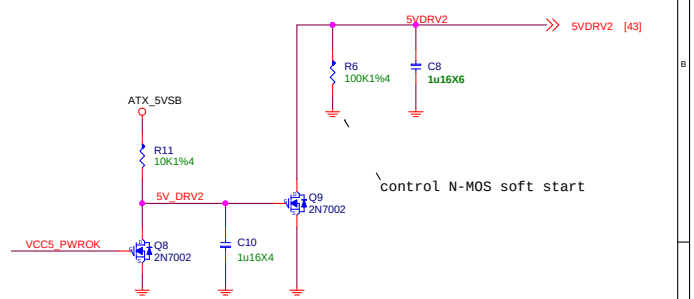
POWER ON:S5-->S0



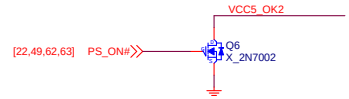








POWER OFF:S0-->S5



MICRO-STAR INT'L CO.,LTD.

Title: 5VDIMM

Size: | Document Number: MS-7D15.. | Rev: 10/20

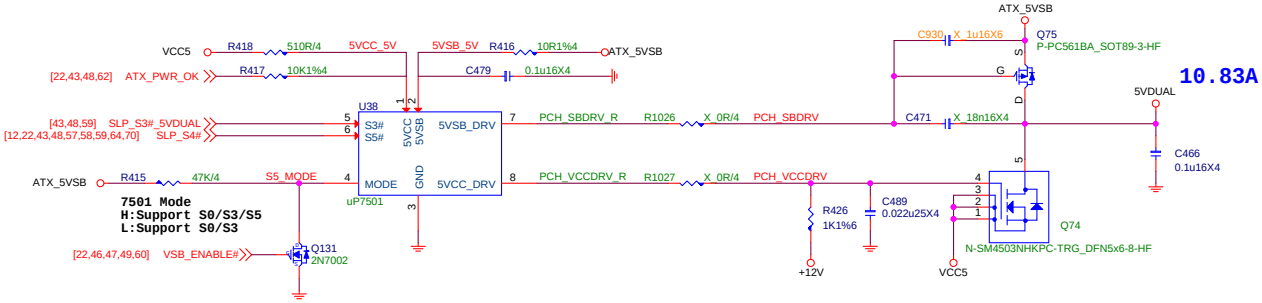
Date: Tuesday, November 03, 2020 | Sheet 48 of 76

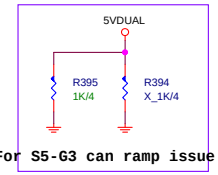
5VDUAL

2020/10/23
C471 is unstuffed by James's comment

2020/10/30
C930 is reserved by James's comment

2020/10/23
R395 is stuffed 1Kohm by James's comment



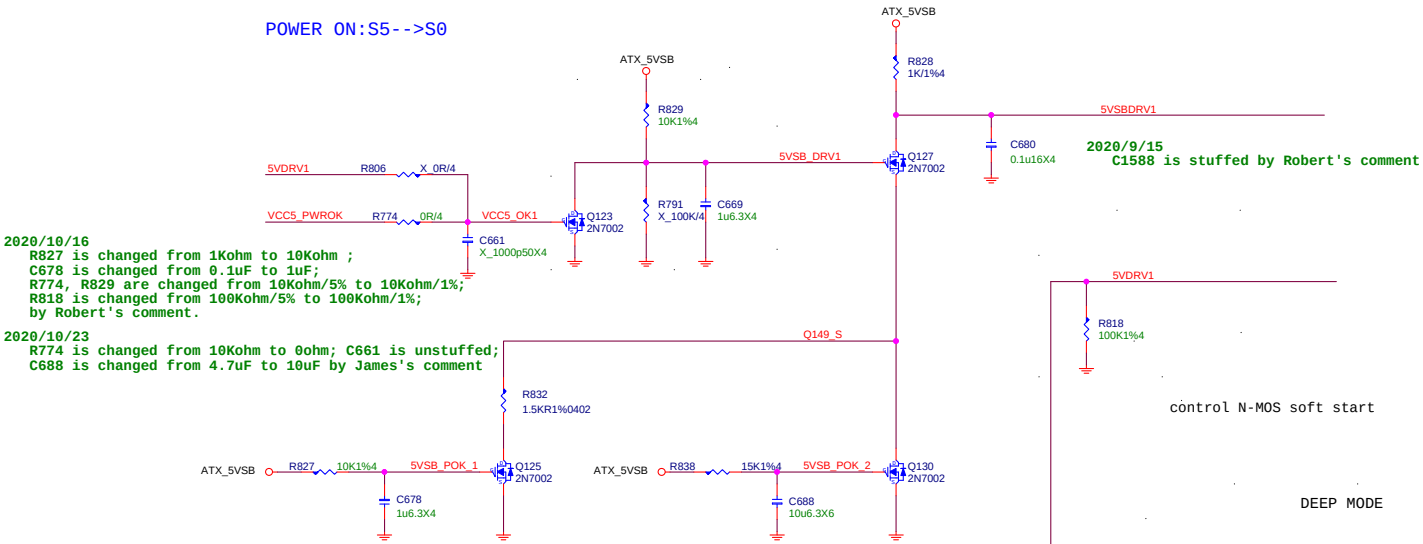


200302:un-stuff R419&R420

PCH_SBDRV R441 0R/4 5VSBDRV1
PCH_VCCDRV R442 0R/4 5VDRV1

control P-MOS soft start and waiting ATX_5VSB ramp to 100%

POWER ON:S5-->S0



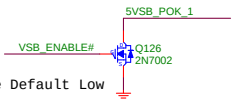
2020/9/15
C1588 is stuffed by Robert's comment

2020/10/16
R827 is changed from 1Kohm to 10Kohm ;
C678 is changed from 0.1uF to 1uF;
R774, R829 are changed from 10Kohm/5% to 10Kohm/1%;
R818 is changed from 100Kohm/5% to 100Kohm/1%;
by Robert's comment.

2020/10/23
R774 is changed from 10Kohm to 0ohm; C661 is unstuffed;
C688 is changed from 4.7uF to 10uF by James's comment

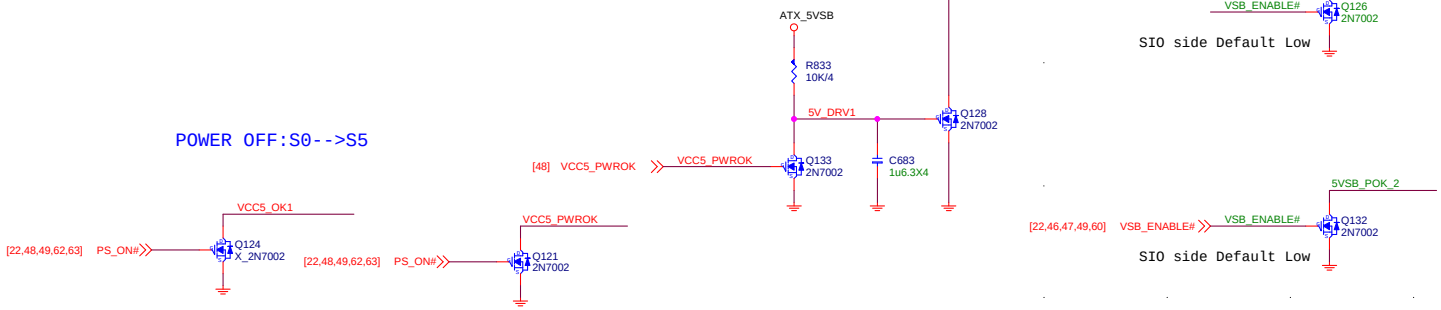
control N-MOS soft start

DEEP MODE



SIO side Default Low

POWER OFF:S0-->S5



SIO side Default Low

MICRO-STAR INT'L CO.,LTD.

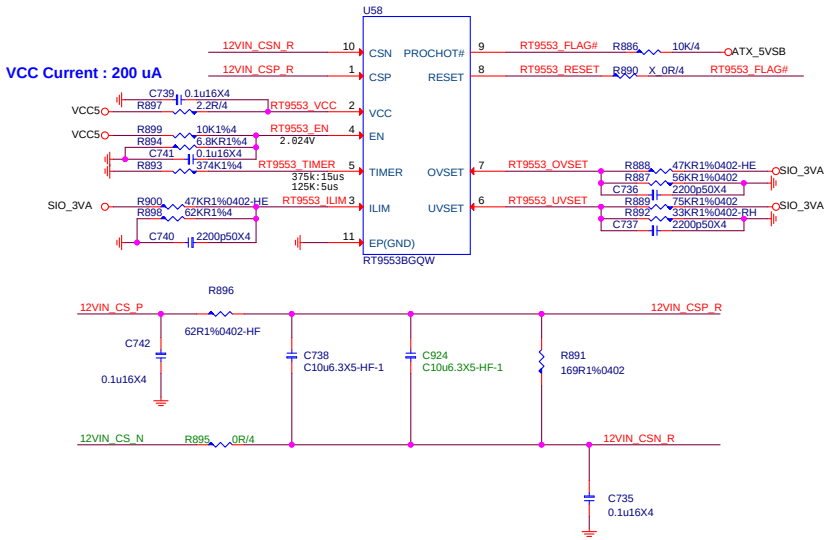
Title: 5VDUAL

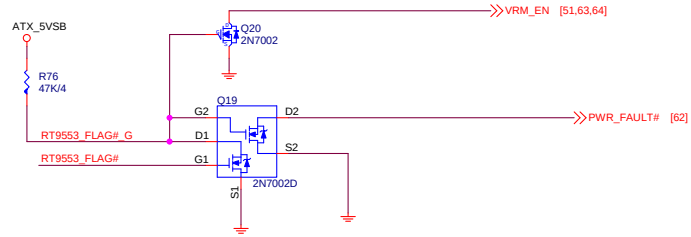
Size | Document Number: MS-7D15.. | Rev: 10/20

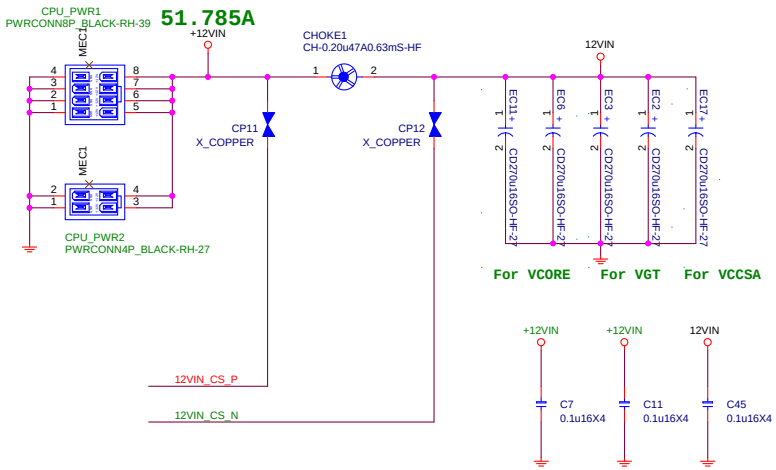
Date: Tuesday, November 03, 2020 | Sheet 49 of 76

OCP: 45A For 8 core 245A Support

Under Checking







D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.72	> output Vcore
D	=	0.143333	

I o = Icore(max)*0.8			
I core(max)	=	245	> Vcore current
I avg.	=	196	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	12	phase
I ripple	=	5.723403	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	55	> Vcore current
I avg.	=	44	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	7.317182	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.05	> output Vcore
D	=	0.0875	

I o = Icore(max)*0.8			
I core(max)	=	22.1	> Vcore current
I avg.	=	17.68	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	4.995773	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COE TEMP	=	1	
Input Cap.	=	1	pcs.

MICRO-STAR INT'L CO.,LTD.

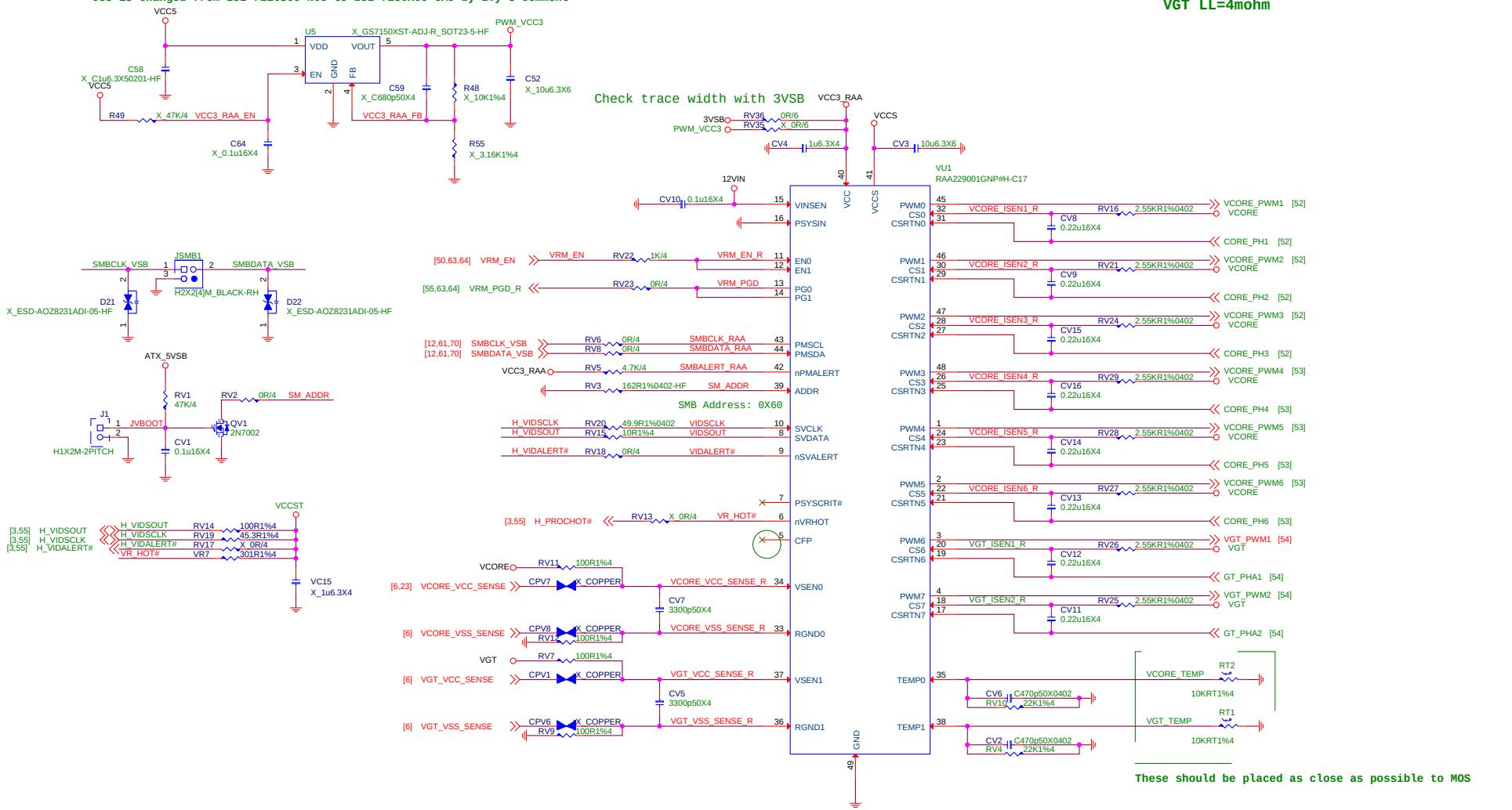
Title: 12VIN/CURRENT SENSE-RT9553

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 50 of 76

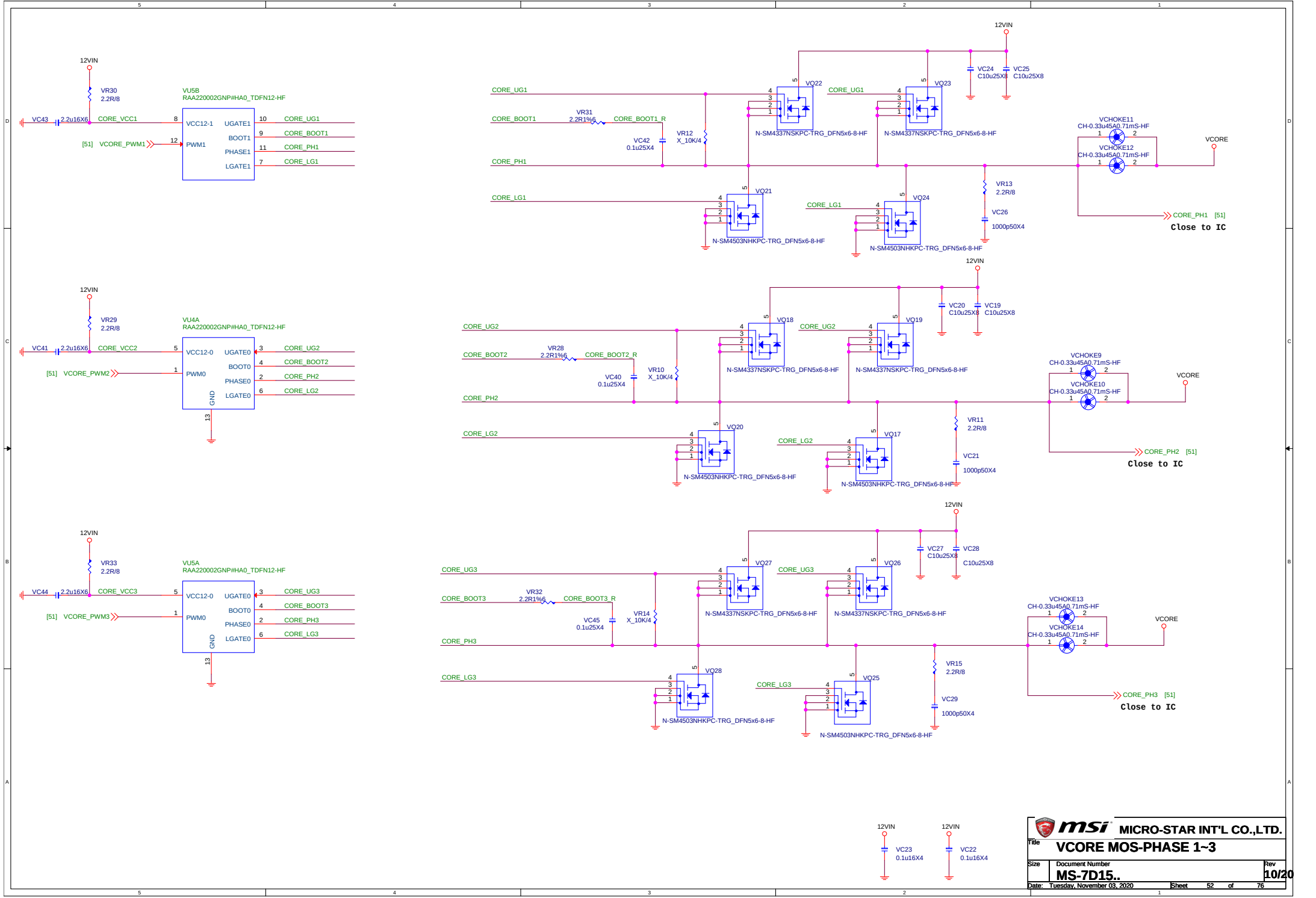
2020/7/8
U33 is changed from I31-7116S09-N03 to I31-7150X09-GA9 by Ivy's comment

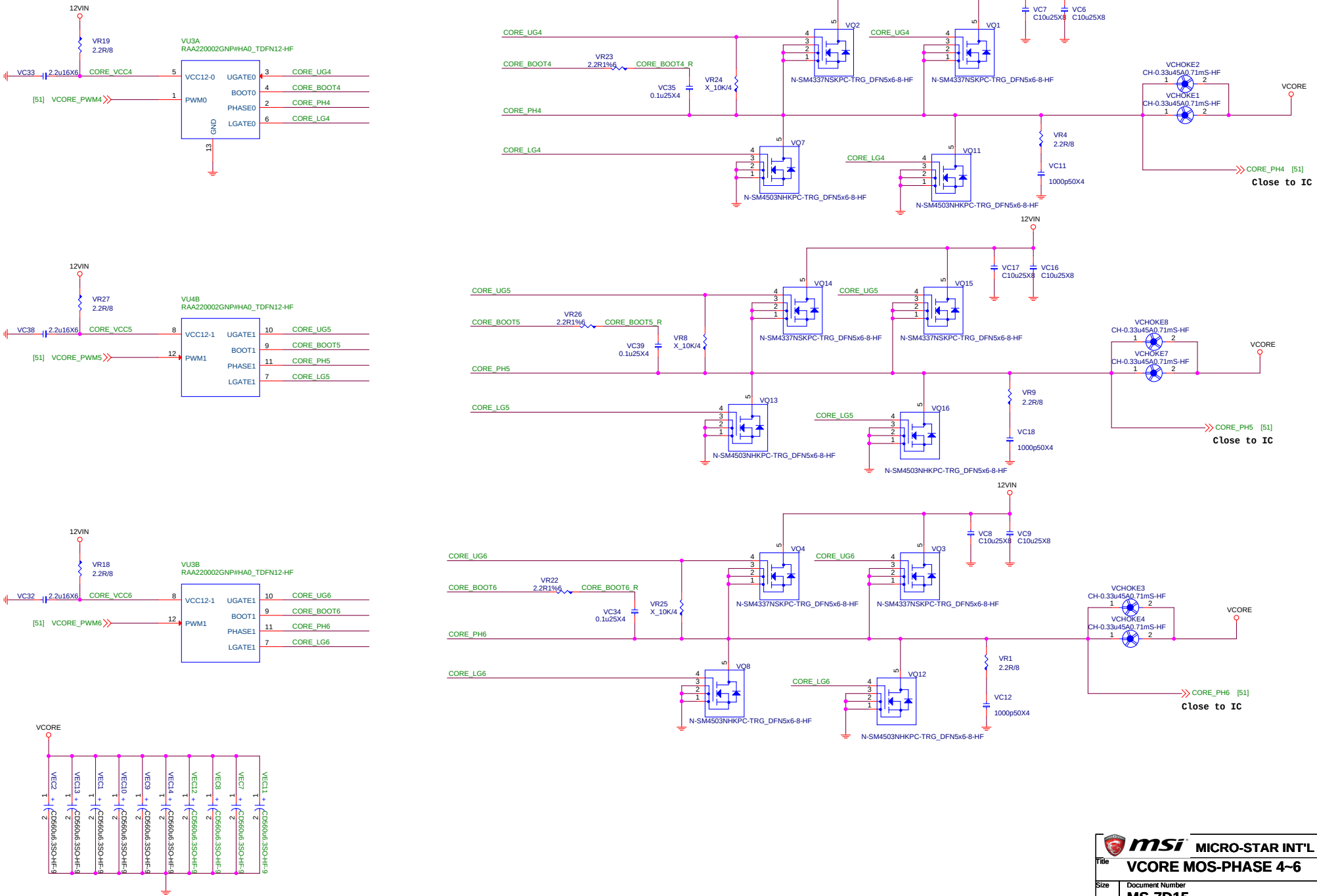
VCORE Iccmax 245A,TDC ?A, OCP ?A.
VGT Iccmax 55A,TDC ?A, OCP ?A
VCORE LL=1.1mohm
VGT LL=4mohm



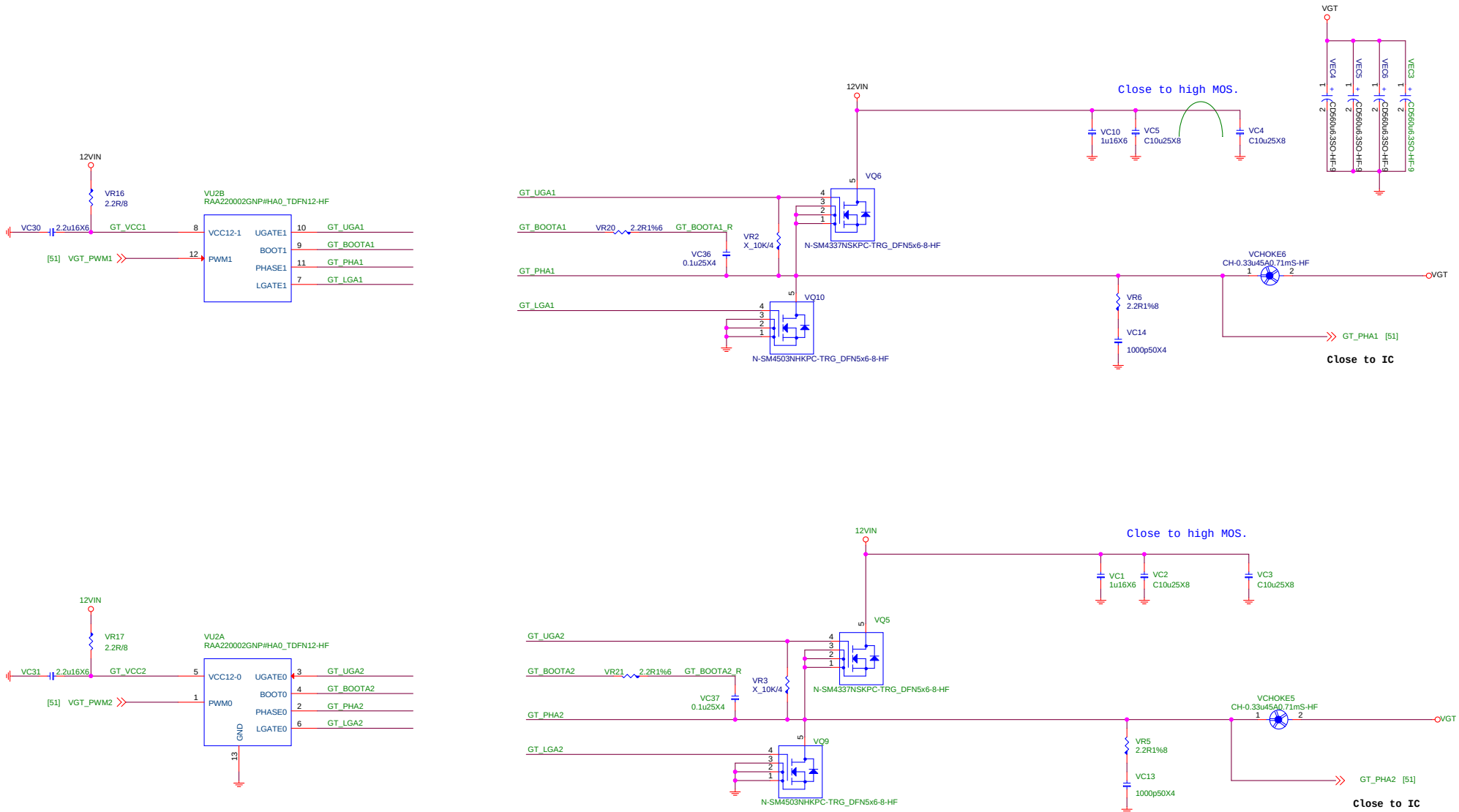
Title	PWM Solution	
Size	Document Number	Rev
	MS-7D15..	10/20
Date: Tuesday, November 03, 2020	Sheet 51 of 76	

MICRO-STAR INT'L CO.,LTD.


12VIN
VR30
2.2R/8
VU5B
RAA220002GNP#HA0_TDFN12-HF
VC43
2.2u16X6
CORE_VCC1
8
VCC12-1
UGATE1
10
CORE_UG1
BOOT1
9
CORE_BOOT1
[51] VCORE_PWM1
12
PWM1
PHASE1
11
CORE_PH1
LGATE1
7
CORE_LG1
VR29
2.2R/8
VU4A
RAA220002GNP#HA0_TDFN12-HF
VC41
2.2u16X6
CORE_VCC2
5
VCC12-0
UGATE0
3
CORE_UG2
[51] VCORE_PWM2
1
PWM0
BOOT0
4
CORE_BOOT2
PHASE0
2
CORE_PH2
GND
LGATE0
6
CORE_LG2
13
VR33
2.2R/8
VU5A
RAA220002GNP#HA0_TDFN12-HF
VC44
2.2u16X6
CORE_VCC3
5
VCC12-0
UGATE0
3
CORE_UG3
[51] VCORE_PWM3
1
PWM0
BOOT0
4
CORE_BOOT3
PHASE0
2
CORE_PH3
GND
LGATE0
6
CORE_LG3
13
12VIN
VC24
C10u25X8
VC25
C10u25X8
CORE_UG1
VQ22
VQ23
CORE_UG1
CORE_BOOT1
VR31
2.2R1%6
CORE_BOOT1_R
VC42
0.1u25X4
VR12
X_10K/4
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4337NSKPC-TRG_DFN5x6-8-HF
VCHOKE11
CH-0.33u45A0.71mS-HF
VCHOKE12
CH-0.33u45A0.71mS-HF
VCORE
CORE_PH1
CORE_LG1
VQ21
VQ24
CORE_LG1
VR13
2.2R/8
VC26
1000p50X4
N-SM4503NHKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
CORE_PH1 [51]
Close to IC
12VIN
VC20
C10u25X8
VC19
C10u25X8
CORE_UG2
VQ18
VQ19
CORE_UG2
CORE_BOOT2
VR28
2.2R1%6
CORE_BOOT2_R
VC40
0.1u25X4
VR10
X_10K/4
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4337NSKPC-TRG_DFN5x6-8-HF
VCHOKE9
CH-0.33u45A0.71mS-HF
VCHOKE10
CH-0.33u45A0.71mS-HF
VCORE
CORE_PH2
CORE_LG2
VQ20
VQ17
CORE_LG2
VR11
2.2R/8
VC21
1000p50X4
N-SM4503NHKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
CORE_PH2 [51]
Close to IC
12VIN
VC27
C10u25X8
VC28
C10u25X8
CORE_UG3
VQ27
VQ26
CORE_UG3
CORE_BOOT3
VR32
2.2R1%6
CORE_BOOT3_R
VC45
0.1u25X4
VR14
X_10K/4
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4337NSKPC-TRG_DFN5x6-8-HF
VCHOKE13
CH-0.33u45A0.71mS-HF
VCHOKE14
CH-0.33u45A0.71mS-HF
VCORE
CORE_PH3
CORE_LG3
VQ28
VQ25
CORE_LG3
VR15
2.2R/8
VC29
1000p50X4
N-SM4503NHKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
CORE_PH3 [51]
Close to IC
12VIN
VC23
0.1u16X4
12VIN
VC22
0.1u16X4
MICRO-STAR INT'L CO.,LTD.
Title
VCORE MOS-PHASE 1~3
Size
Document Number
MS-7D15..
Rev
10/20
Date: Tuesday, November 03, 2020
Sheet 52 of 76



msi MICRO-STAR INT'L CO.,LTD.			
Title: VCORE MOS-PHASE 4~6			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 53 of 76		



MICRO-STAR INT'L CO.,LTD.

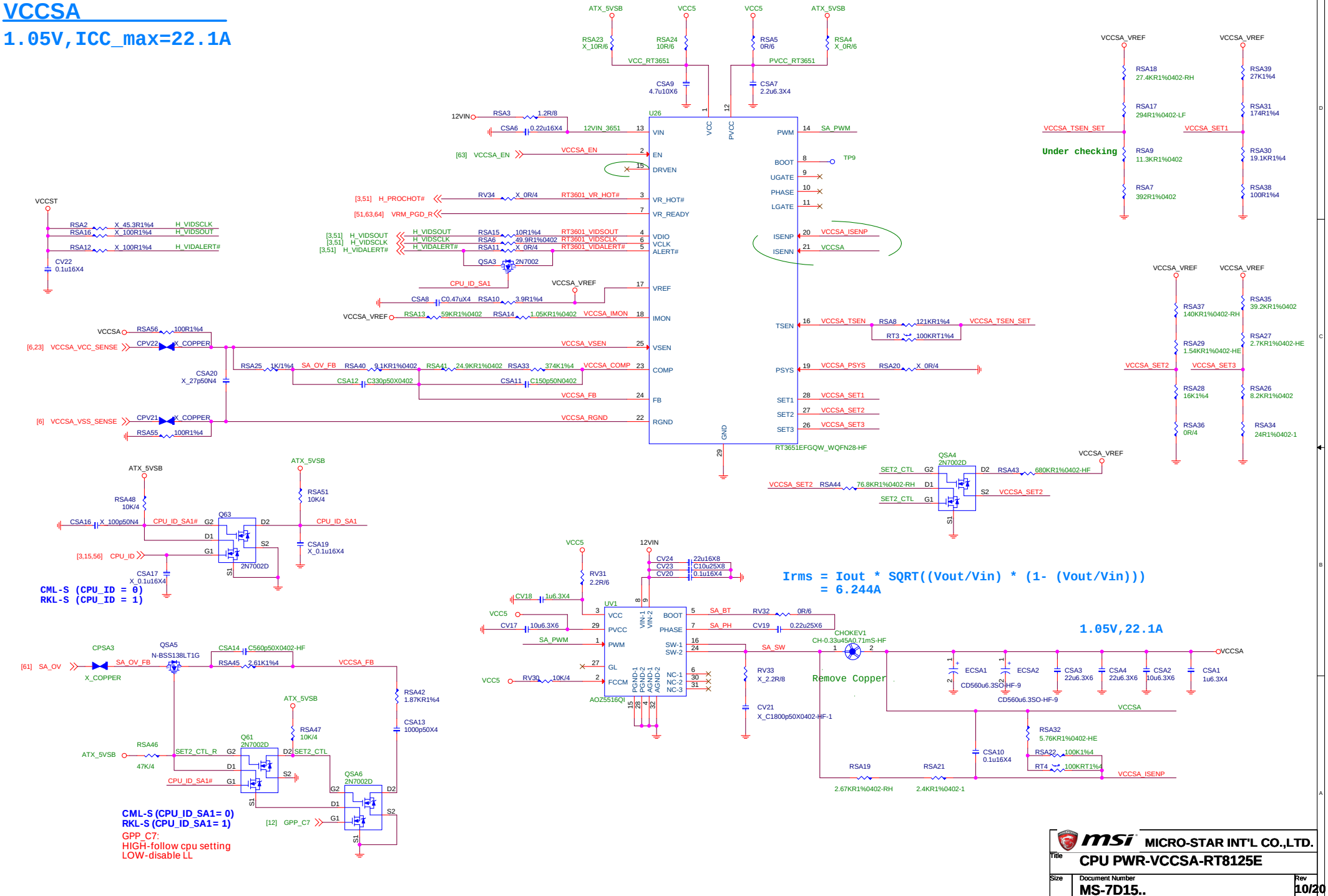
Title: VGT MOS-PHASE 1~2

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 54 of 76

VCCSA

1.05V,ICC_max=22.1A



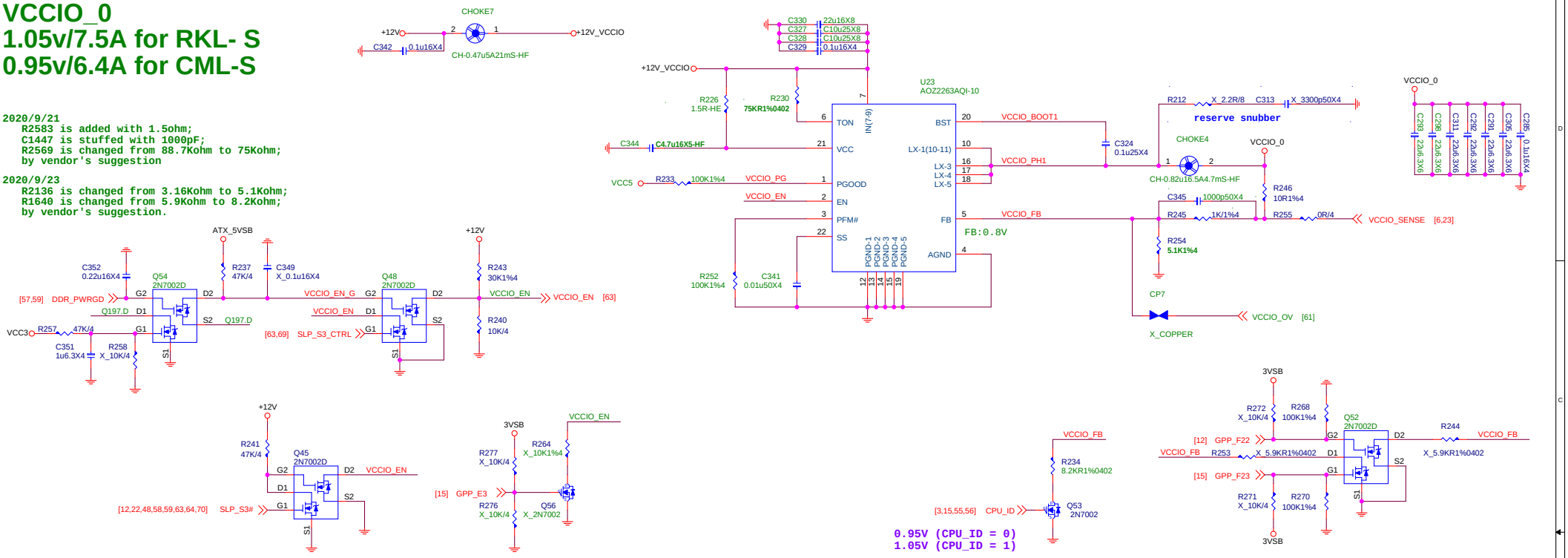
MICRO-STAR INT'L CO.,LTD.

Title	CPU PWR-VCCSA-RT8125E	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 55 of 76	

VCCIO_0
1.05v/7.5A for RKL- S
0.95v/6.4A for CML-S

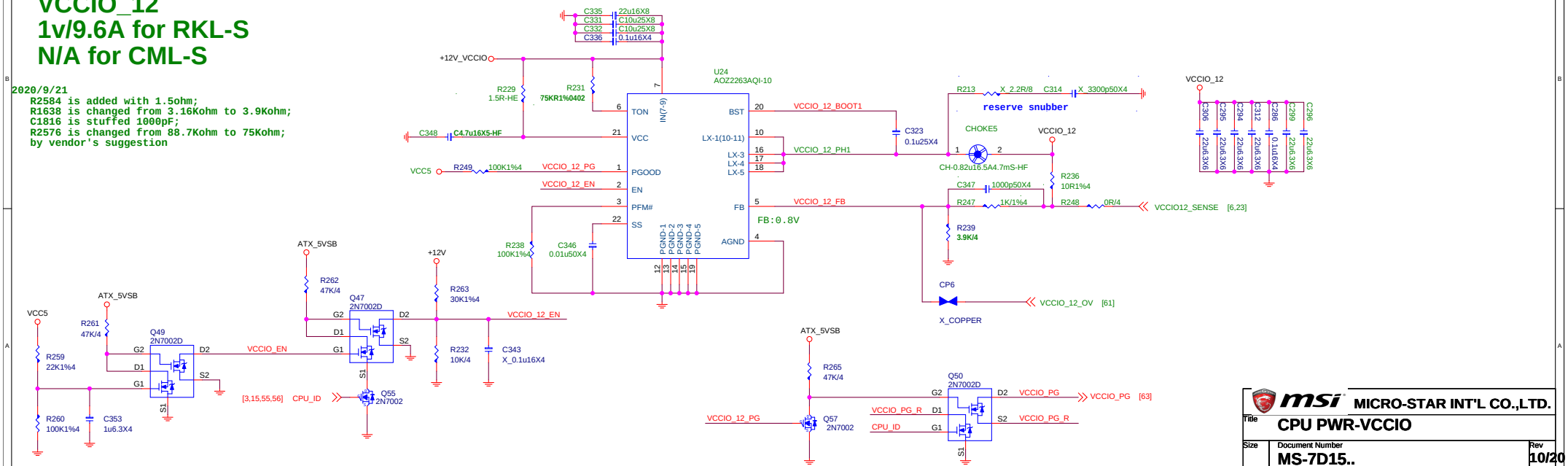
2020/9/21
R2583 is added with 1.5ohm;
C1447 is stuffed with 1000pF;
R2569 is changed from 88.7Kohm to 75Kohm;
by vendor's suggestion

2020/9/23
R2136 is changed from 3.16Kohm to 5.1Kohm;
R1640 is changed from 5.9Kohm to 8.2Kohm;
by vendor's suggestion.



VCCIO_12
1v/9.6A for RKL-S
N/A for CML-S

2020/9/21
R2584 is added with 1.5ohm;
R1638 is changed from 3.16Kohm to 3.9Kohm;
C1816 is stuffed 1000pF;
R2576 is changed from 88.7Kohm to 75Kohm;
by vendor's suggestion



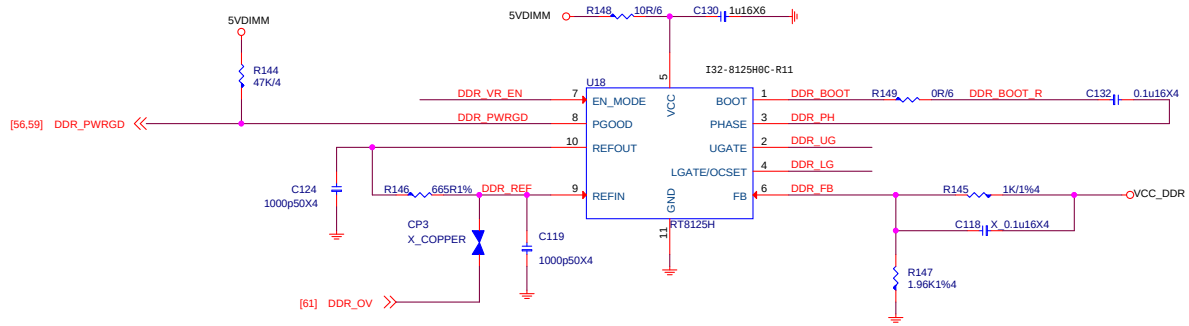
msi MICRO-STAR INT'L CO.,LTD.			
Title: CPU PWR-VCCIO			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 56 of 76		

DDR4 Power:1.2V,14.149A OCP:18A

4.3A For CPU
9.1A For 4DIMM
0.7A For DDR VTT
Iout = 3.7+9.1+0.7=14.149A

Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/5.1m
=14.3529A
Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/3.9m
=18.769A

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=20A	-	2.5	3	mΩ
		T_J=125°C	-	3.75	-	
		V_{GS}=4.5V, I_{DS}=15A	-	3.9	5.1	



$$V_{OUT} = \left[V_{REFOUT} \times \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \right] + \frac{\Delta V_{OUT}}{2}$$

Vout=Vrefout*(1+R1/R2)
=0.794x(1+1/1.96)
=1.1991v

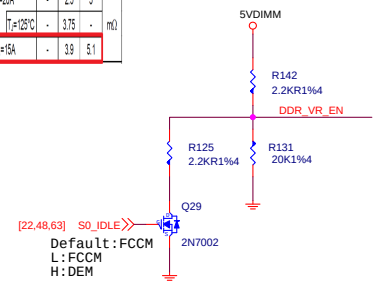


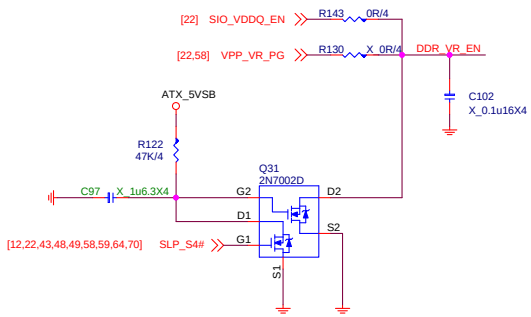
Table 1. States of EN_MODE Control Circuit

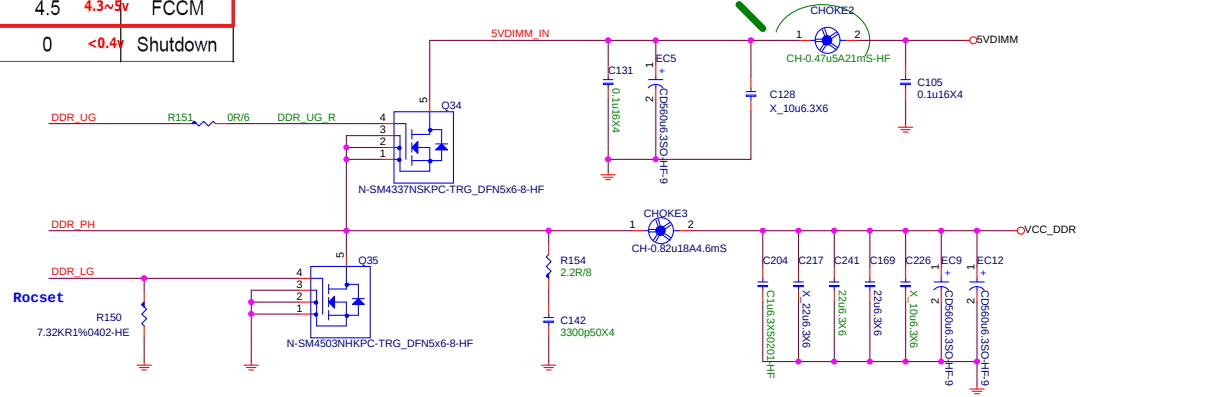
Q1	Q2	V_{EN_MODE} (V)	Mode
ON	OFF	2.37 2.1~2.7v	DEM
OFF	OFF	4.5 4.3~5v	FCCM
OFF	ON	0 <0.4v	Shutdown

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 14.149 * SQRT(0.1824)
= 6.043A

Under Checking





ΔIL=(Vin-Vout)/(L*Fsw) * Vout/Vin
=(5-1.2)/(0.82u*300K)*(1.2/5)
=3.7073A

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Rocset = [(1.3* Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= [(1.3*14.149) -(0.5*3.7073)]* 3.9m / 10u
= 6.45Kohm

Rocset = [(1.3*Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= ((1.3*14.149) - (0.5*3.7073)]* 5.1m / 10u
= 8.435Kohm

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.2*14.149) * (1.2/5)
= 1.074uH

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.4*14.149) * (1.2/5)
= 0.53714uH

So L range = 0.53714uH ~ 1.074uH

MICRO-STAR INT'L CO.,LTD.

Title: DDR4 Power

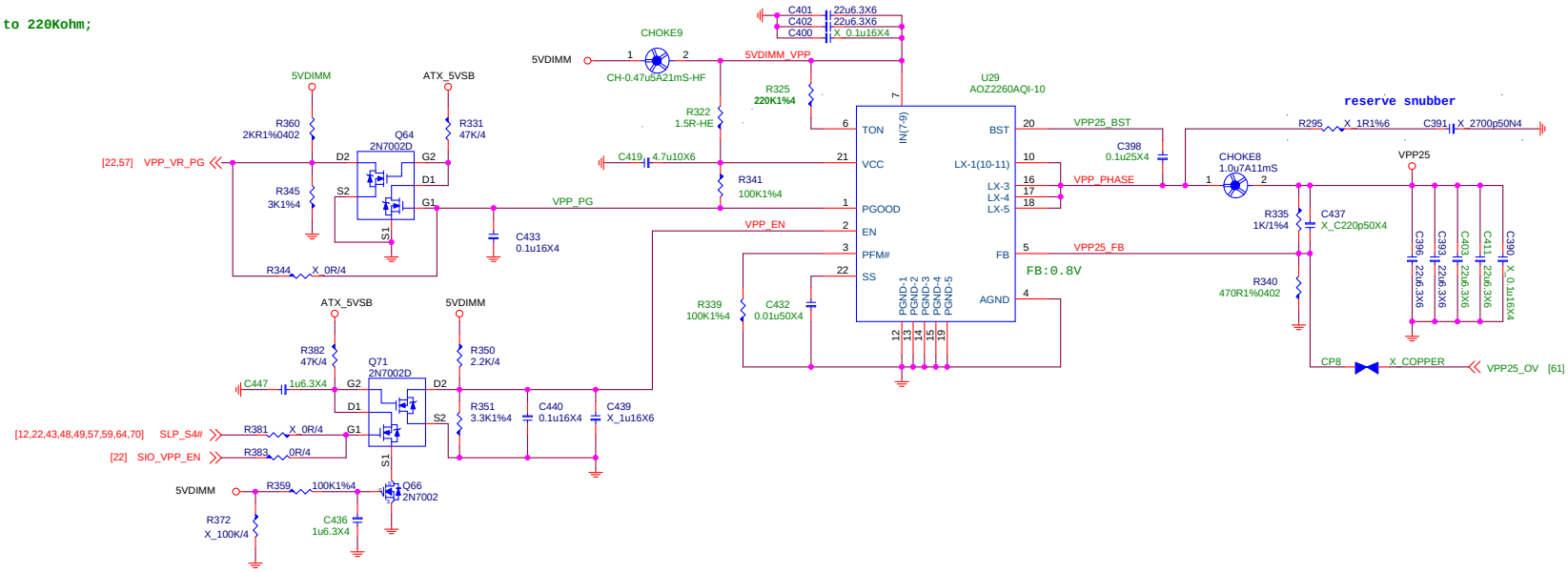
Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 57 of 76

VPP2.5V Power:2.5V,6A(for dimm LED)

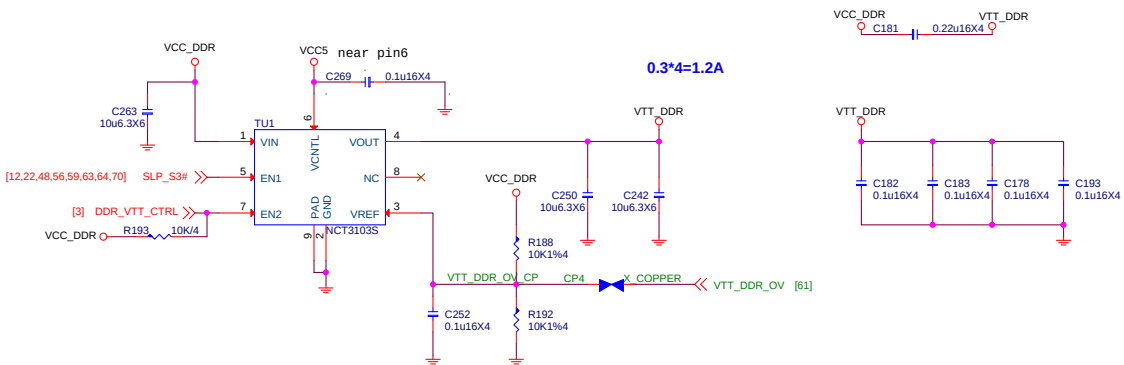
IC OCP:7.6A(6.6A~8.6A)

2020/9/21
R2563 is changed from 180Kohm to 220Kohm;
R2582 is added with 1.5ohm;
by vendor's suggestion



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

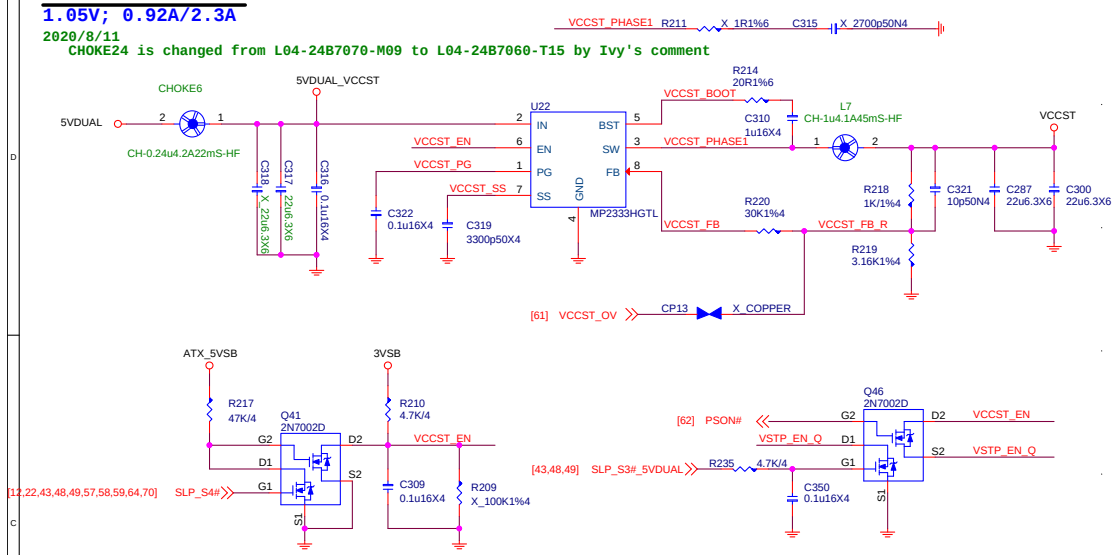


MICRO-STAR INT'L CO.,LTD.		
Title: DDR PWR VPP25/VTT		
Size	Document Number: MS-7D15..	Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 58 of 76	

VCCST

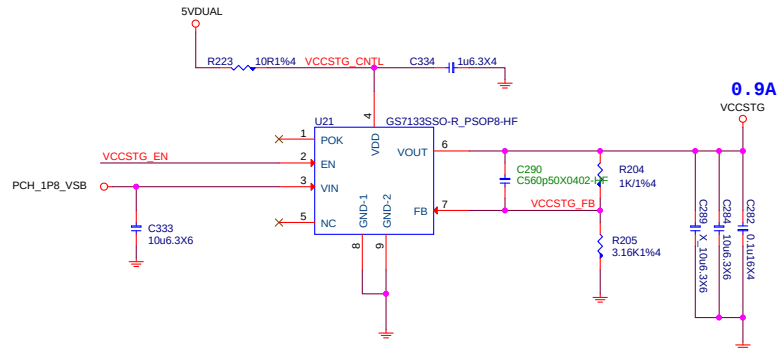
1.05V; 0.92A/2.3A

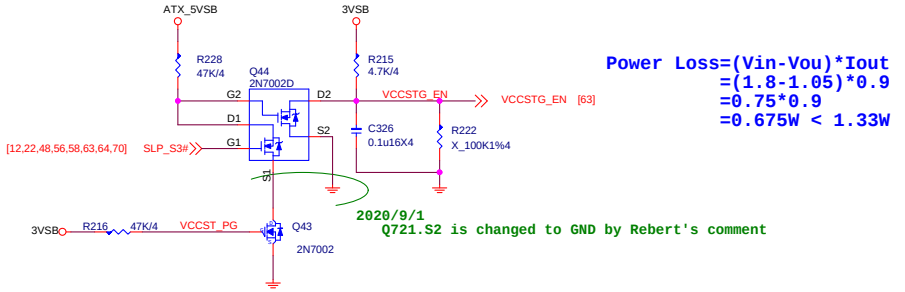
2020/8/11
CHOKE24 is changed from L04-24B7070-M09 to L04-24B7060-T15 by Ivy's comment



VCCSTG

1.05V; 0.2A/0.9A





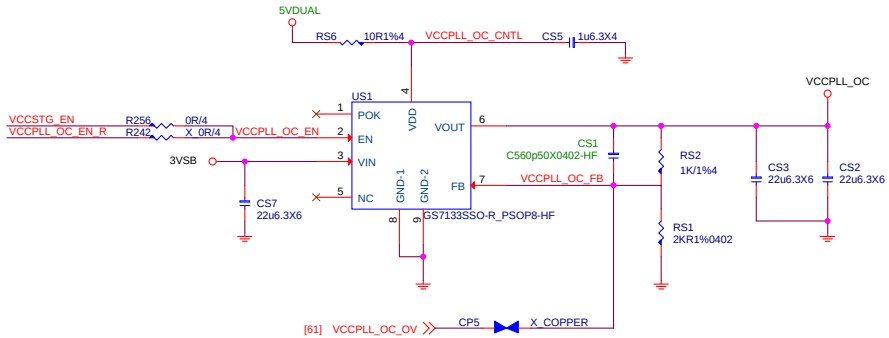
Power Loss=(Vin-Vou)*Iout
=(1.8-1.05)*0.9
=0.75*0.9
=0.675W < 1.33W

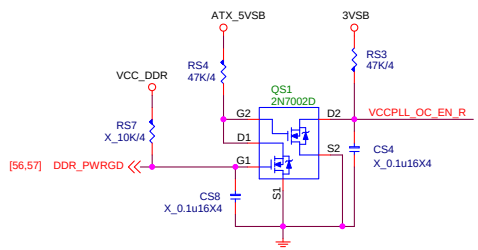
VCCPLL_OC

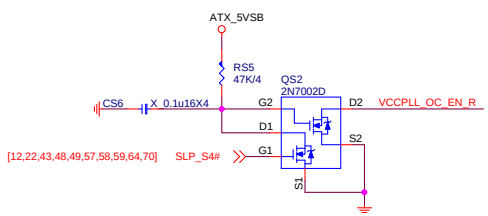
1.2V; 250mA

2020/7/1
VCCPLL_OC is connected directly to VCC_DDR by B560/H510 project from Ivy'comment

2020/8/3
VCCPLL_OC curcuit is added from Eric'comment







Title	CPU PWR-VCCST/PLL	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 59 of 76	

MICRO-STAR INT'L CO.,LTD.

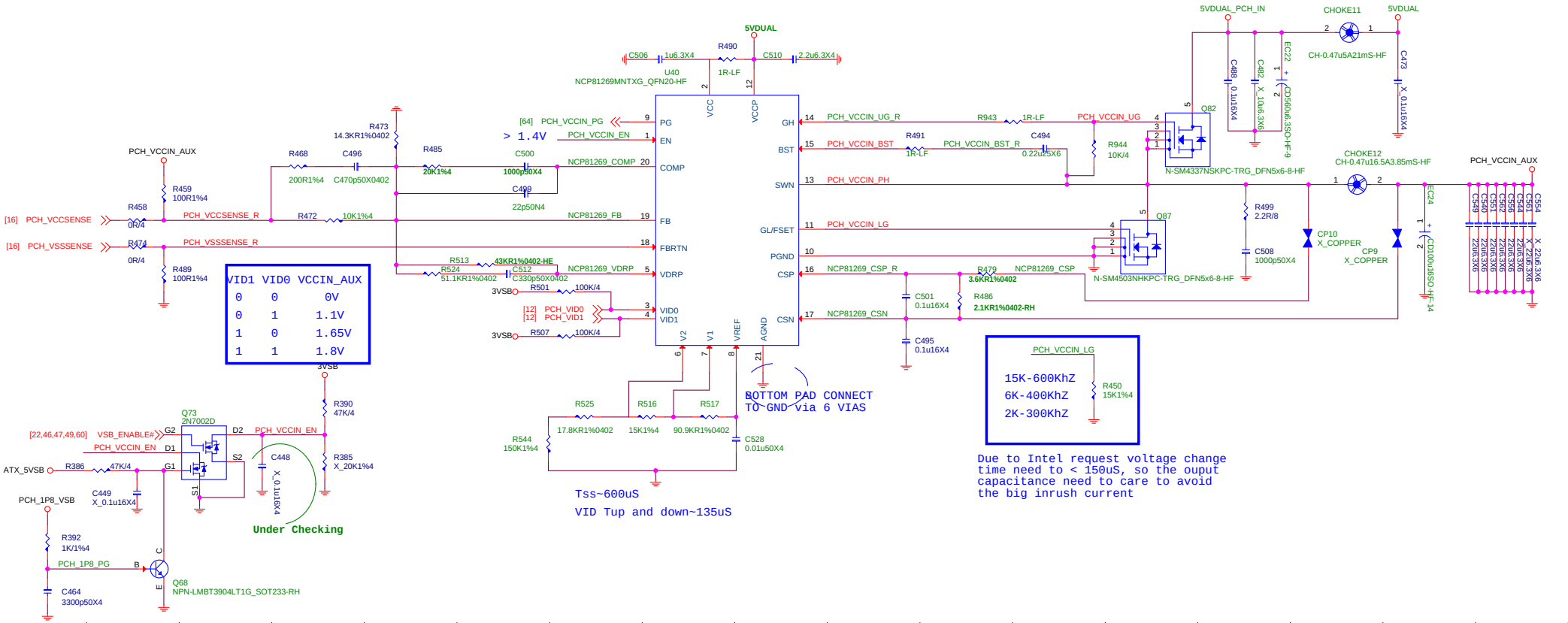
PCH_Power:VCCIN_AUX

1.8V 9.646A

OCP=18.6A

Vin=5V
FS=600KHz
OCP=16.8~22.4A
Iout=11.2A
Output Choke=0.47uH/ Isat=25A

2020/9/28
C1975 is changed from 330pF to 1000pF; R1592 is changed from 75Kohm to 20Kohm; the power rail of U464.12, U464.2 are changed from 5VDUAL_PCH_IN to 5VDUAL; R2650 is changed from 17.8Kohm to 43Kohm; R2658 is changed from 8.2Kohm to 3.6Kohm; R2657 is changed from 12Kohm to 2.1Kohm by vendor's suggestion

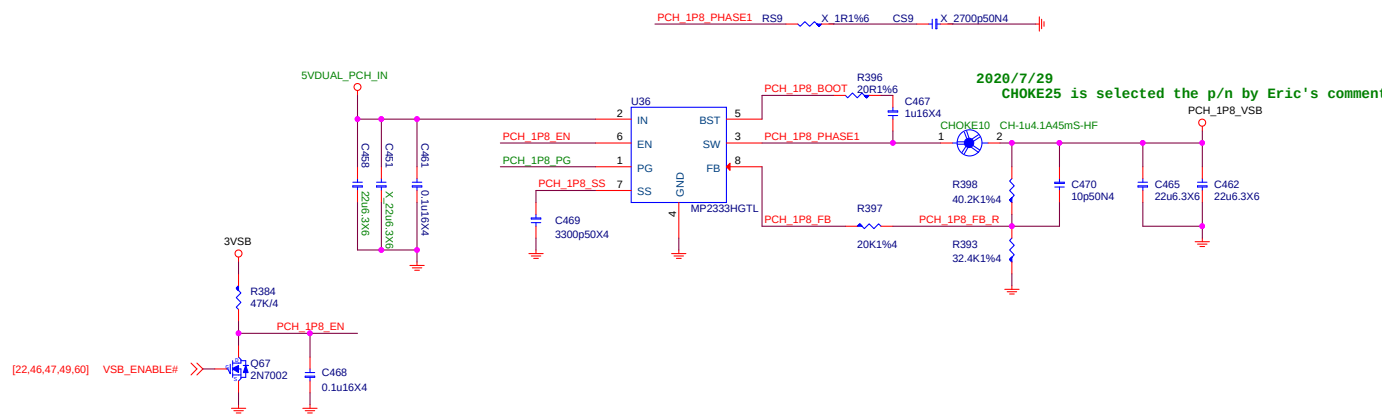


PCH_1P8_VSB

1.8V; 1.635A

PCH_CLKLDO_1P8(0.09A)

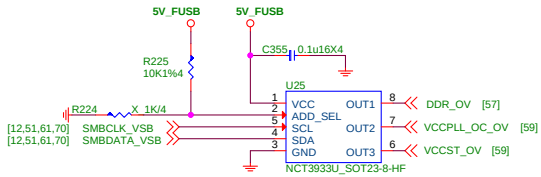
VCCPRIM_1P8(1.545A)



MICRO-STAR INT'L CO.,LTD.			
Title: PCH POWER-NCP81269/1P8_VSB			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 60 of 76		

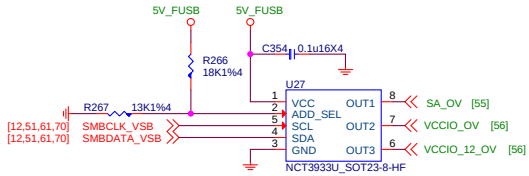
UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



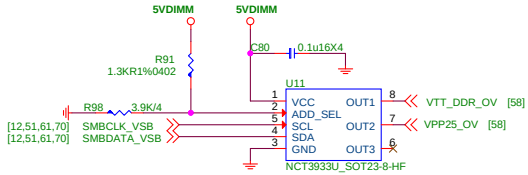
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE

0x22:RH=1.3K,RL=3.9K



2020/8/25
U498, C1860, R2542, R2543 are added by Ivy's comment

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

NCT3933 SMBUS ADD	0X26
OUT1(PIN8)	VCCSA
OUT2(PIN7)	VCCIO0
OUT3(PIN6)	VCCIO1_2
NCT3933 SMBUS ADD	0X20
OUT1(PIN8)	VCC_DDR
OUT2(PIN7)	**VCCPLL_OC**
OUT3(PIN6)	VCCST

NCT3933 SMBUS ADD	0X22
OUT1(PIN8)	DDR VTT
OUT2(PIN7)	DDR VPP25
OUT3(PIN6)	N/A

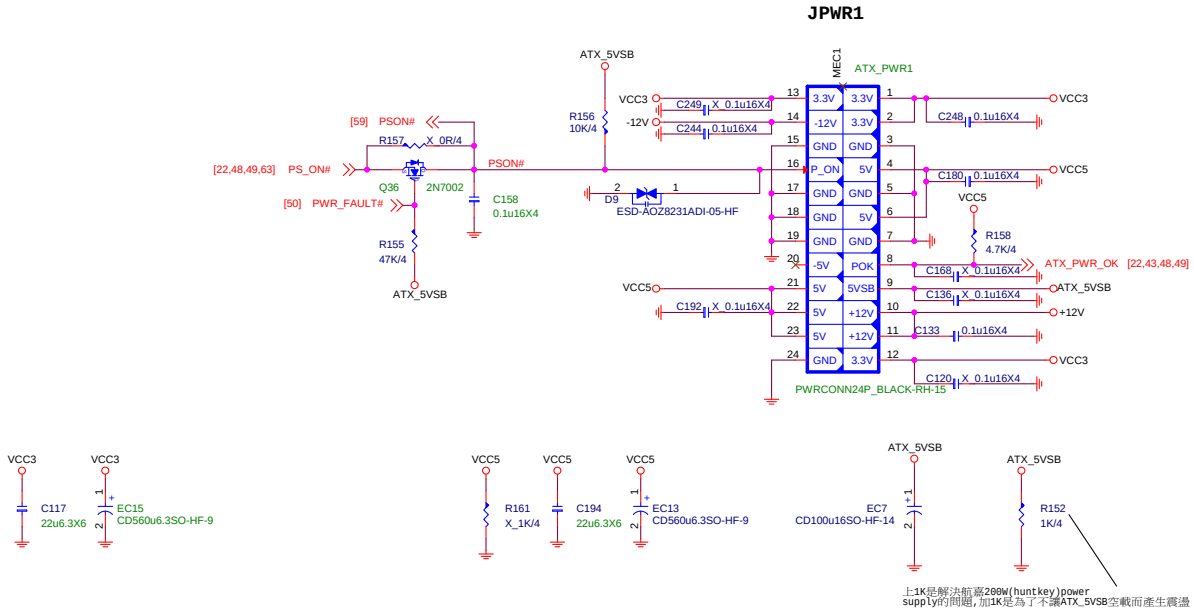
MICRO-STAR INT'L CO.,LTD.

Title: GS7133/OV

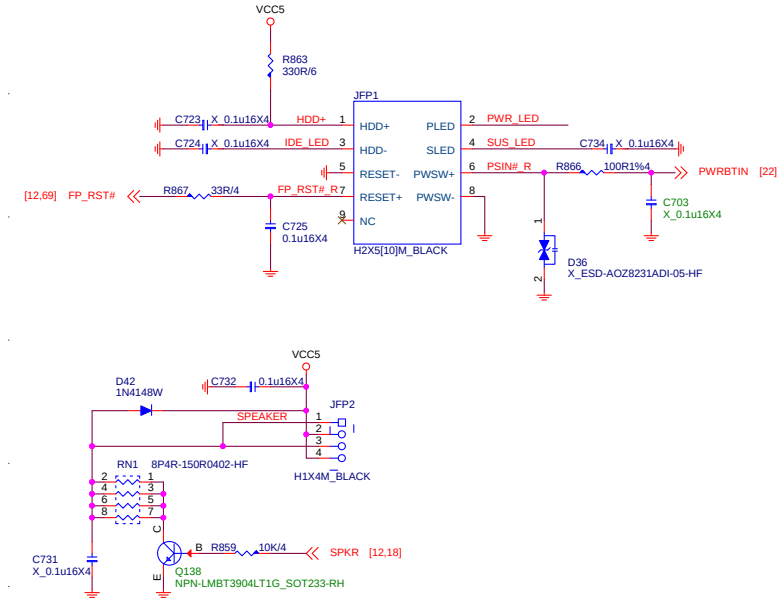
Size | Document Number: MS-7D15.. | Rev: 10/20

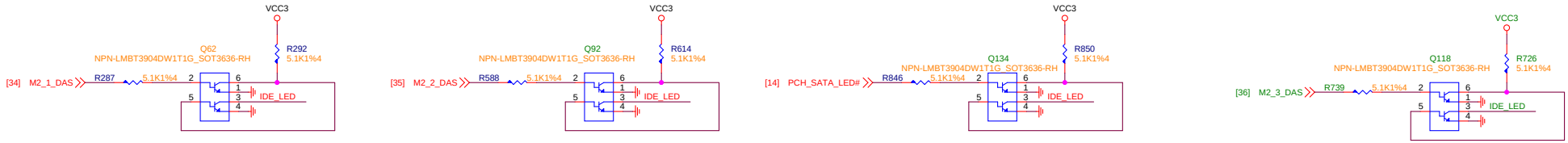
Date: Tuesday, November 03, 2020 | Sheet 61 of 76

ATX POWER CONNECTOR



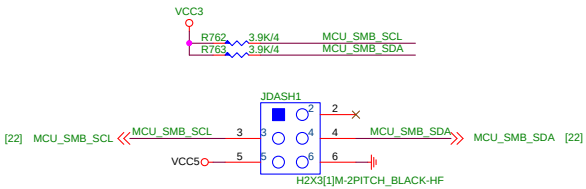
FRONT PANNEL





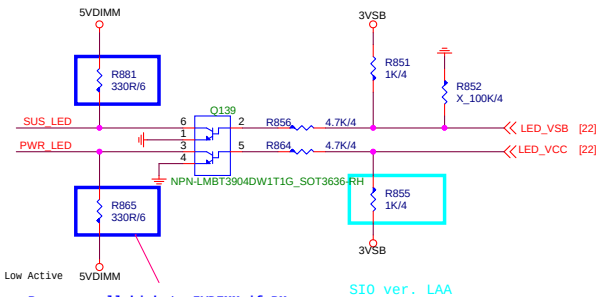
2020/10/27
Q62, Q92, Q134,Q118 are changed from 7002 to 3904; R287, R588, R846, R739 are 0ohm to 5.1Kohm; R292, R614, R850, R726 are changed from 10Kohm to 5.1Kohm by Robert's comment.

JDASH1



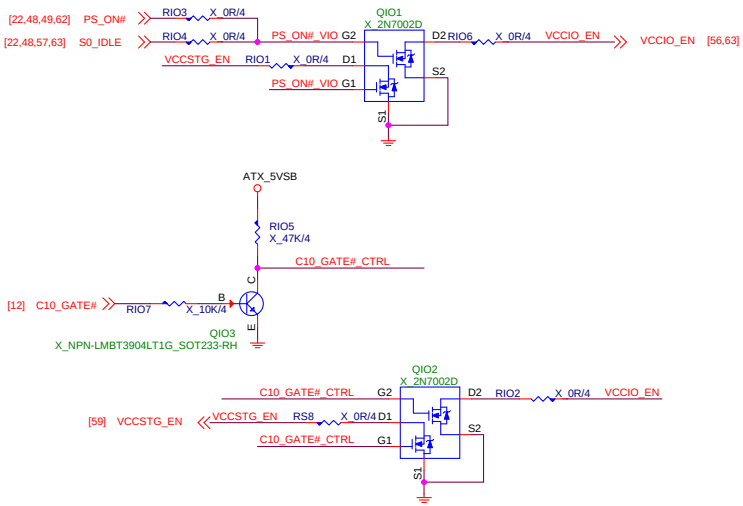
2020/8/12
JDASH1 is added by PM spec updated
2020/8/20
JDASH1 is changed from N32-2020161-H06 to N31-2031431-H06 by PM spec updated

Front Panel LED

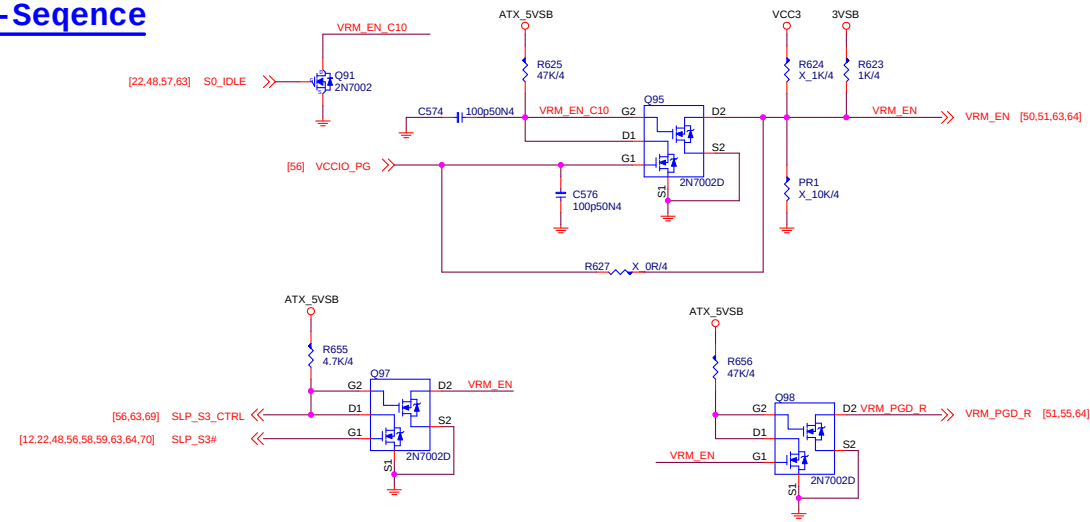


MSI	MICRO-STAR INT'L CO.,LTD.	
Title	ATX Connector/F_Panel	
Size	Document Number MS-7D15..	Rev 10/20
Date: Tuesday, November 03, 2020	Sheet 62 of 76	

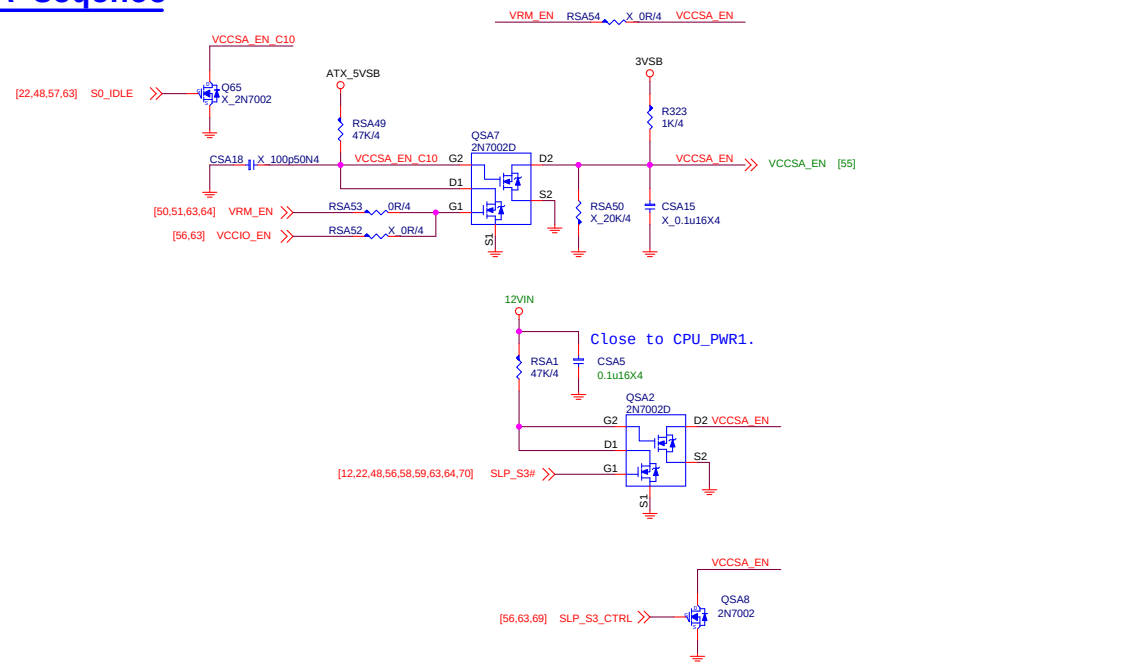
S0IX: VCCIO/VCCSTG OFF



PWR-VRM-Seqence



PWR-VCCSA-Seqence



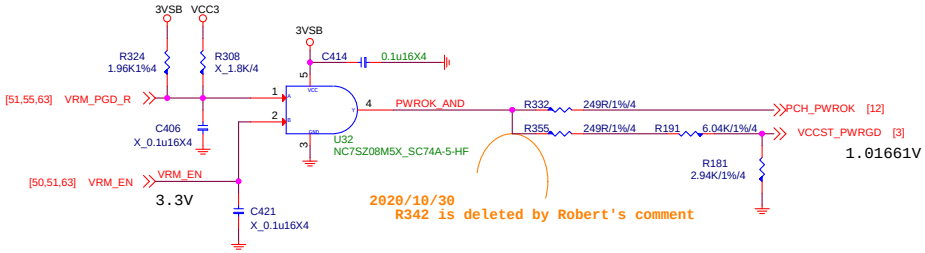
MICRO-STAR INT'L CO.,LTD.

Title: CPU VRM-Seqence/VCCAPLL

Size | Document Number: MS-7D15.. | Rev: 10/20

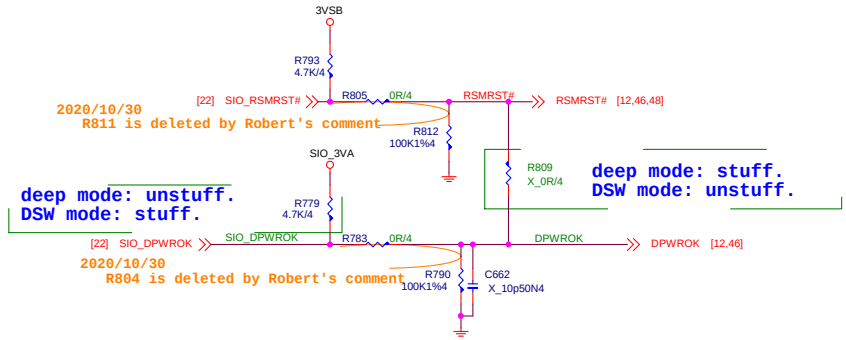
Date: Tuesday, November 03, 2020 | Sheet 63 of 76

PCH_PWROK/VCCST_PWRGD



1.01661V

2020/10/30
R342 is deleted by Robert's comment

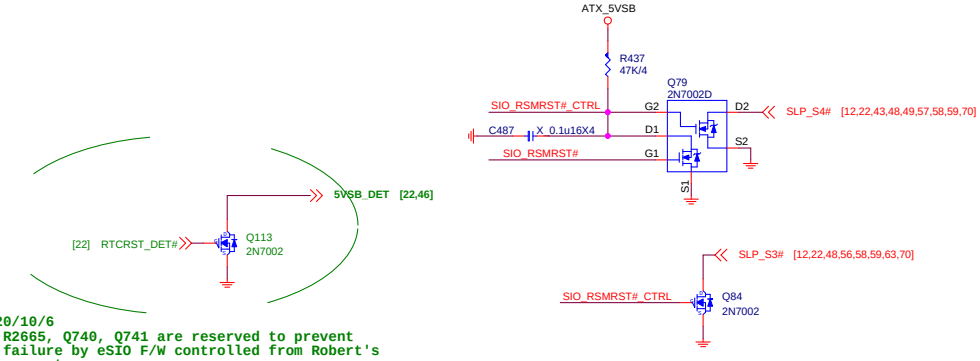


2020/10/30
R811 is deleted by Robert's comment

deep mode: unstuff.
DSW mode: stuff.

deep mode: stuff.
DSW mode: unstuff.

2020/10/30
R804 is deleted by Robert's comment



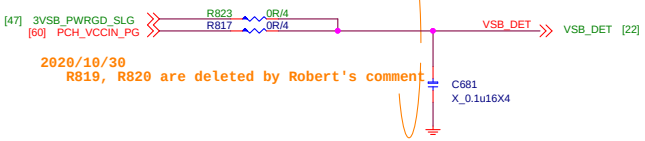
2020/10/6
R2665, Q740, Q741 are reserved to prevent failure by eSIO F/W controlled from Robert's comment.

2020/10/15
Q119, R729 are deleted; Q113 is stuffed and is modified by Robert's comment.

FOR RSMRST#/DPWROK/SLP_SUS# INTEL seqence request

2020/10/30
U51, D28, C663, R786, R787, C657, R803, R810, C667, C674, R821, R822, R830, Q129, R776, R788, R782, R777, C658 are deleted by Robert's comment

VSB_DET:2250mV



2020/10/30
R819, R820 are deleted by Robert's comment

MICRO-STAR INT'L CO.,LTD.

Title: ACPI-3VSB/3VDSW

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 64 of 76

IF no JPWRLED1 & JPIPE_LED spec

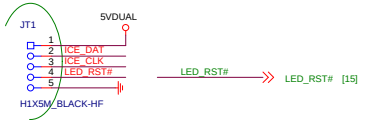
MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test

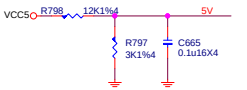
– – Check with LED model spec

JT1 for FW update

JT1 轉 MP BOM 可移除

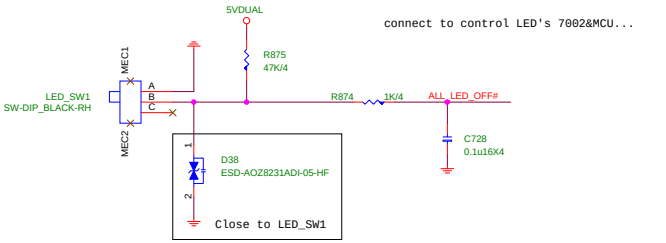


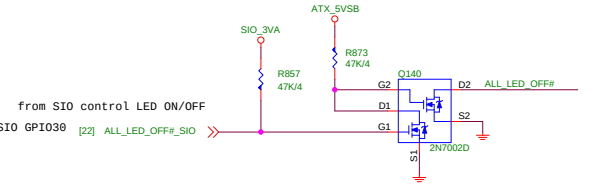
HW Monitor Voltage & Thermal



LED SWITCH

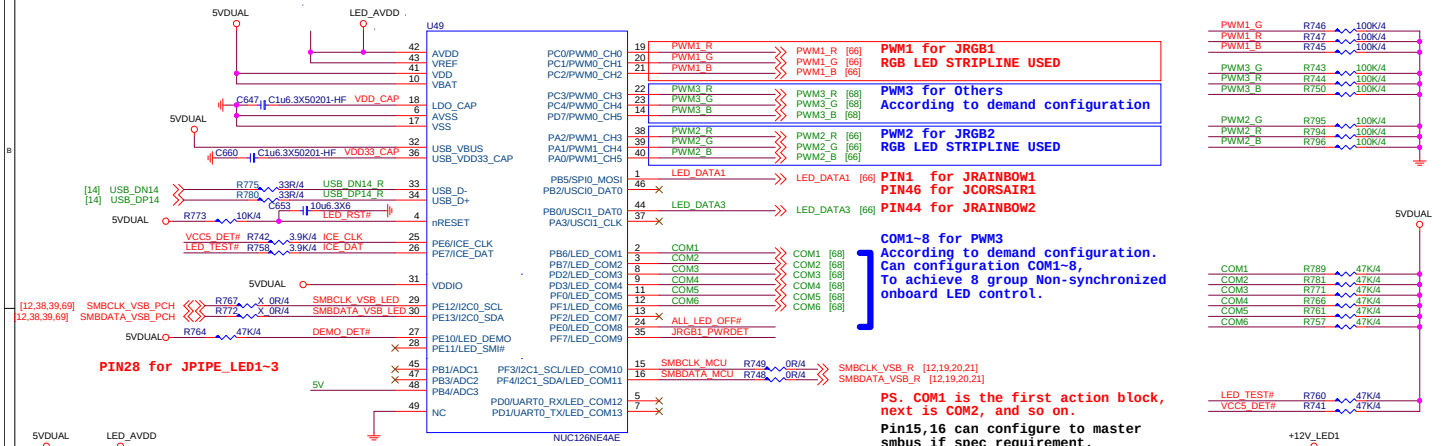
B-C:LED ON (Default)
B-A:LED OFF

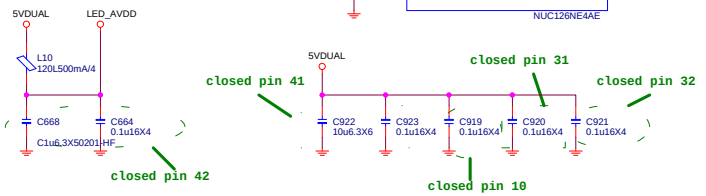


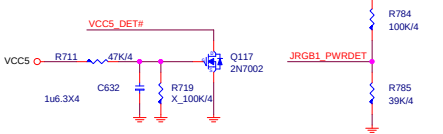


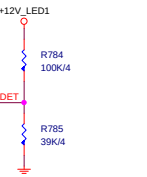
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.









Control	Net Name	PWM USE
PCH	LED_DATA4	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_DATA1	No Use
JRAINBOW2	LED_DATA3	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~12	PWM2

MICRO-STAR INT'L CO.,LTD.

Title: LED MCU Control

Size | Document Number: MS-7D15.. | Rev: 10/20

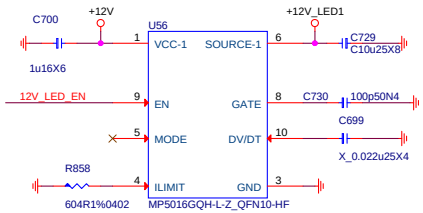
Date: Tuesday, November 03, 2020 | Sheet 65 of 76

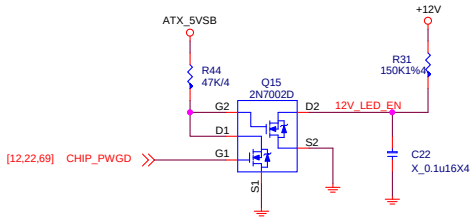
JRGB1

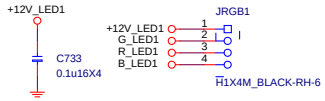
>60mil

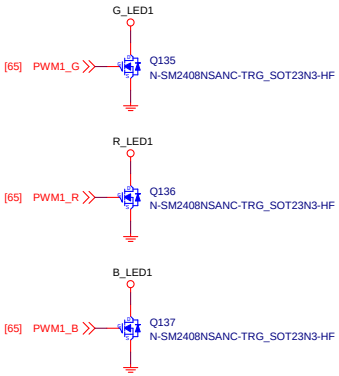
Trip@3.6A

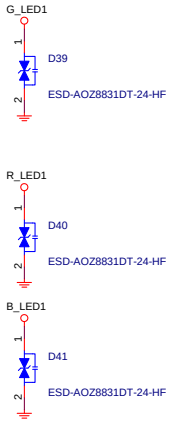
>60mil









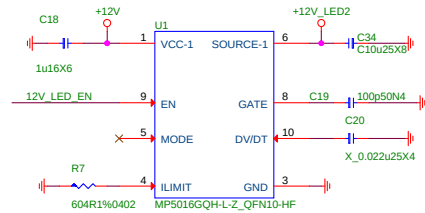


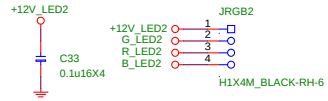
JRGB2

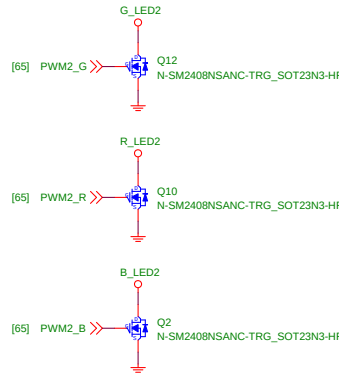
>60mil

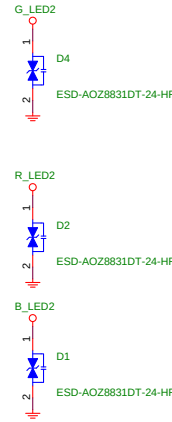
Trip@3.6A

>60mil

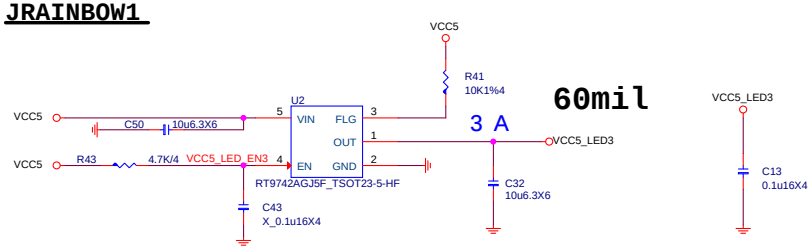




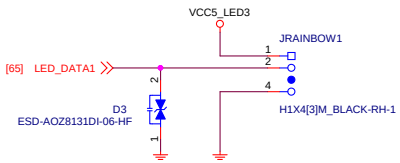




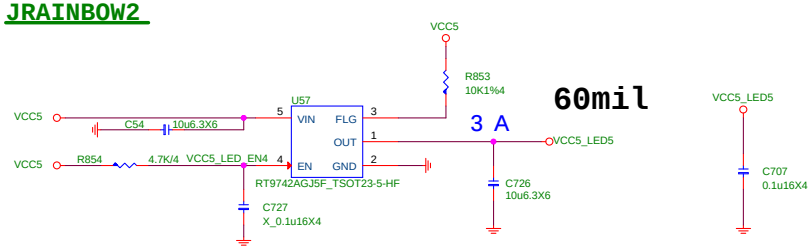
JRAINBOW1



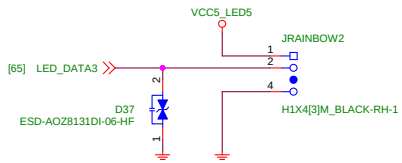
60mil



JRAINBOW2



60mil



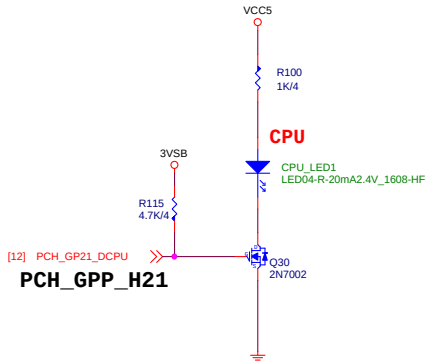
MICRO-STAR INT'L CO.,LTD.

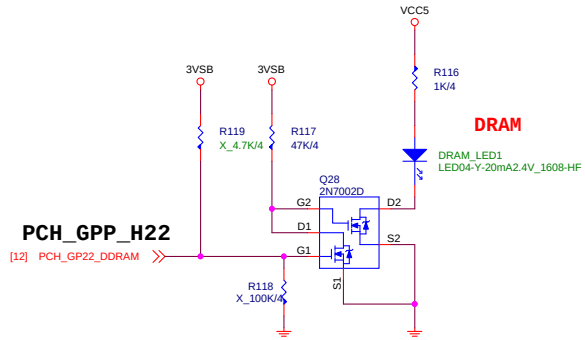
Title: LED PIN HEADER

Size | Document Number: MS-7D15.. | Rev: 10/20

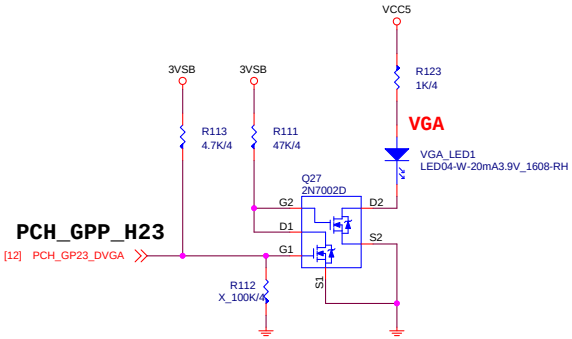
Date: Tuesday, November 03, 2020 | Sheet 66 of 76

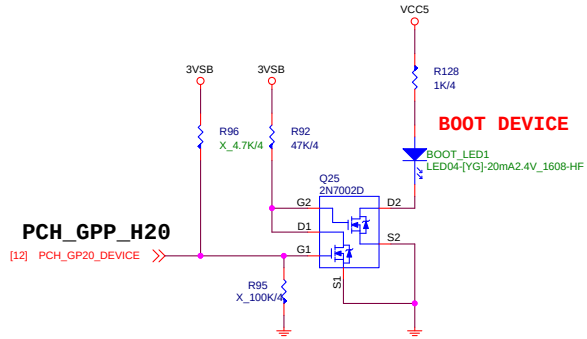
EZ DEBUG LED





2020/10/27
R119, R96 are unstuffed by avoiding double pull-up





GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

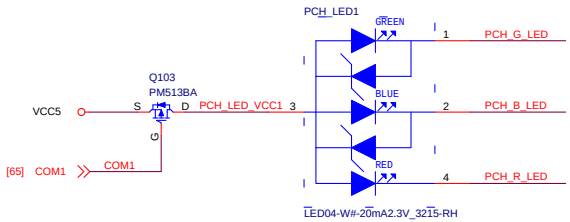
MICRO-STAR INT'L CO.,LTD.

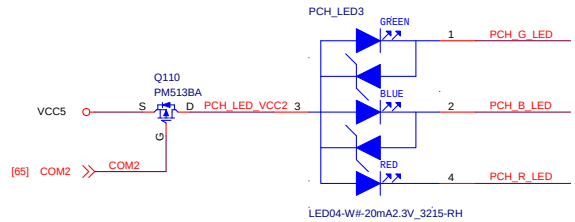
Title: EZ DEBUG LED

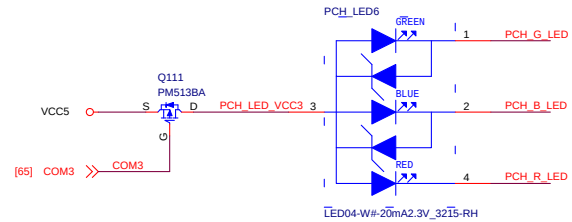
Size | Document Number: MS-7D15.. | Rev: 10/20

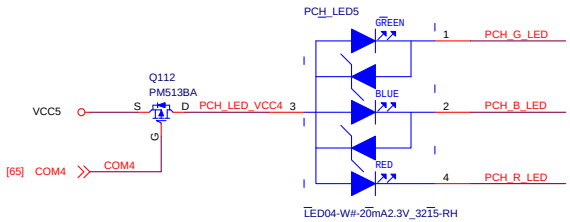
Date: Tuesday, November 03, 2020 | Sheet 67 of 76

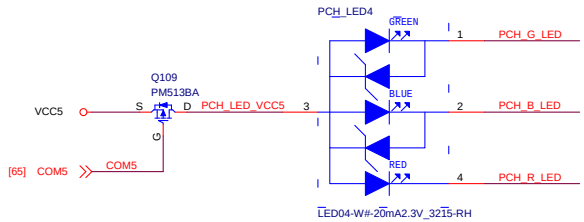
PCH_LED

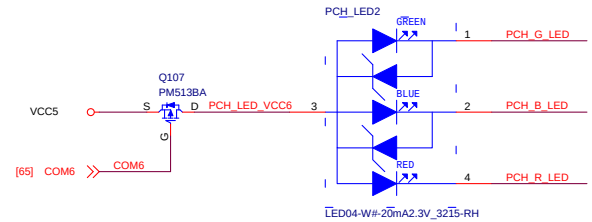


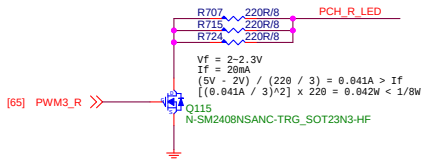


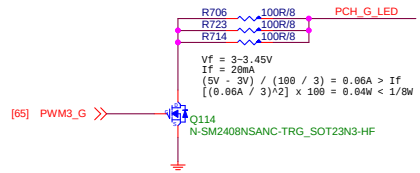


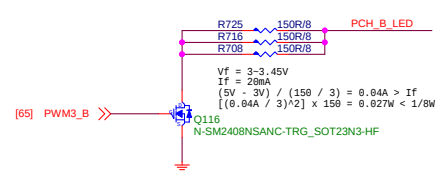












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Title: PCH LED

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 | Sheet 68 of 76

2020/10/29
R282, R279 are unstuffed and then R281, R278 are stuffed by Reed's comment

From PCH

to CPU

to CPU

M2_1

PCI_E1

SMB Add: 0xD8(8bit)

SMB_A0	ADDR
0	D2/D3
1	D8/D9

CPU_SEL	SRC_SEL	CPU(2:0)	SRC(5:0)	Notes
0	0	CPUPLL	CPUPLL	
0	1	CPUPLL	SRCPLL	Default
1	0	N/A	N/A	
1	1	SRCPLL	SRCPLL	

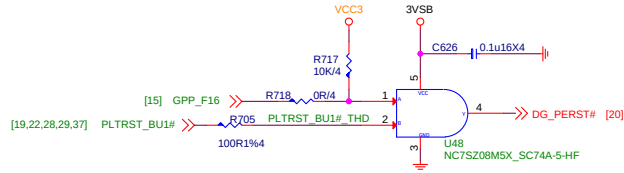
20180509
change to 1.0

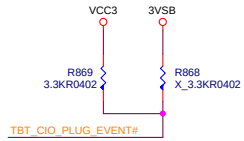
Title	CLKGEN
Size	
Document Number	MS-7D15..
Rev	10/20
Date:	Tuesday, November 03, 2020
Sheet	69 of 76

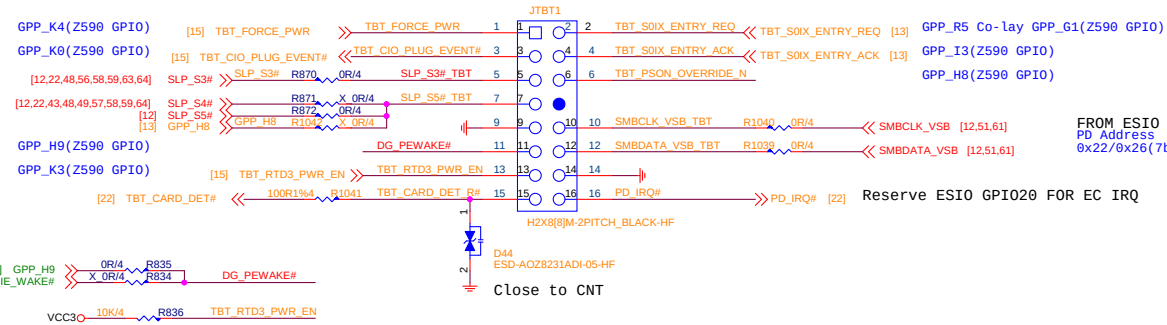
MICRO-STAR INT'L CO.,LTD.

Thunderbolt card support

2020/10/27
R717.2 is changed from 3VSB to VCC3 by double check with Robert





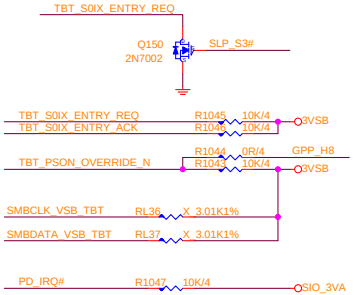


GPP_R5 Co-lay GPP_G1(Z590 GPIO)
GPP_I3(Z590 GPIO)
GPP_H8(Z590 GPIO)

FROM ESIO PIN90/PIN91
PD Address
0x22/0x26(7bit)->0x44/0x4C(8bit)

Reserve ESIO GPIO20 FOR EC IRQ

Close to CNT



2020/10/28
R836 is stuffed by Robert's comment

MICRO-STAR INT'L CO.,LTD.			
Title: JTBT			
Size	Document Number: MS-7D15..		Rev: 10/20
Date: Tuesday, November 03, 2020	Sheet 70 of 76		

BAT1_X1

BAT-BCR2032P-RH

CPU_H1

CPU 鐵座

AZIF0208-P001C

OK

BIOS_LA1

AMI

AMI

PCB1

PD0-07D1510-G37

M2_1-COVER1

0436-3156R

M2_2-COVER1

0436-3157R

N_MOS_HS1

0P10B08818

W_MOS_HS1

0P10B08819

PCH_HS1

0P10B08817

MOS H/S Holes

HS_H1

X_HS_H

HS_H4

X_HS_H

HS_H3

X_HS_H

HS_H2

X_HS_H

2020/7/16
HS_H1, HS_H2, HS_H3, HS_H4 are added by EMI Cloud comment

2020/7/29
The footprint of HS_H1, HS_H2, HS_H3, HS_H4 are changed from H_NR162D120_EMI to H_R162D120_BR182_EMI by Eric's comment

2020/8/3
The footprint of HS_H1, HS_H2, HS_H3, HS_H4 are changed from H_NR162D120_EMI to H_R162D120_BR182_EMI by Min's comment

Optical Fiducial Marks-120

FM3 FM6 FM5 FM7

X_FM X_FM X_FM X_FM

FM1 FM8 FM4 FM2

X_FM X_FM X_FM X_FM

Simulation

SIM1 SIM4 X_PIN1*2

SIM2 SIM3 X_PIN1*2

Mounting Holes

MH1 MH3 MH9

MH2 MH5 MH4

MH6 MH8 MH7

X_MH001

CA44 0.1u16X4

CA43 0.1u16X4

0A SKU

DUAL_USB2

DUAL USB

X_USBAX2M_BLUE-RH-6

0B SKU

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Title: Manual Parts

Size | Document Number: MS-7D15.. | Rev: 10/20

Date: Tuesday, November 03, 2020 Sheet 71 of 76