catalog

INTEL Chief River Platform

Version : A

Drawing by : Wain

Notes:

Part Value Prefix : "@" means nopop

Net Value suffix : "#" means Low Active

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Size	Sheet Name	Rev
C	Cover Sheet	A

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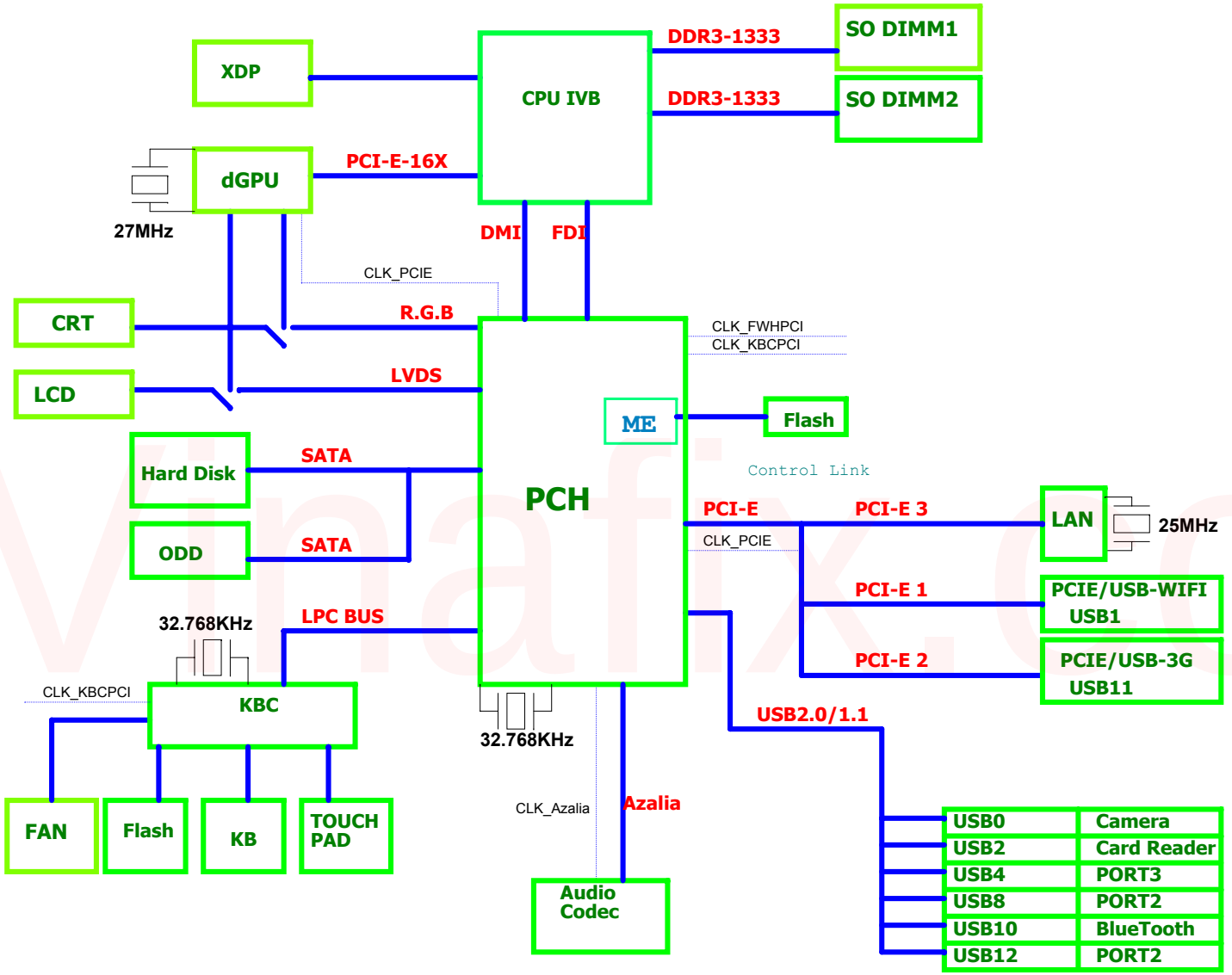
Date: Thursday, March 21, 2013 Sheet 1 of 38

X300DE/X300V/X300 BLOCK DIAGRAM



System Power
TPS51125

CPU & GFX Power
ISL95831

dGPU Power
TPS51621

Chipset Power
TPS51117

DDR3 Power
TPS51116

Charger
BQ24725

S3/S4 Control
and Discharge

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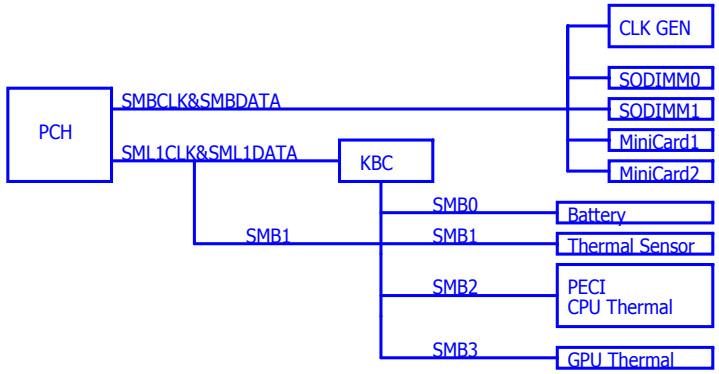
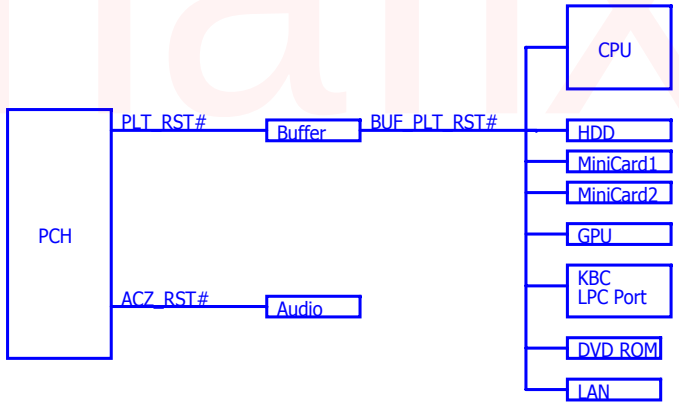
SMBUS TOPOLOGY



RESET TOPOLOGY



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C	SMBUS & RESET TOPOLOGY	A

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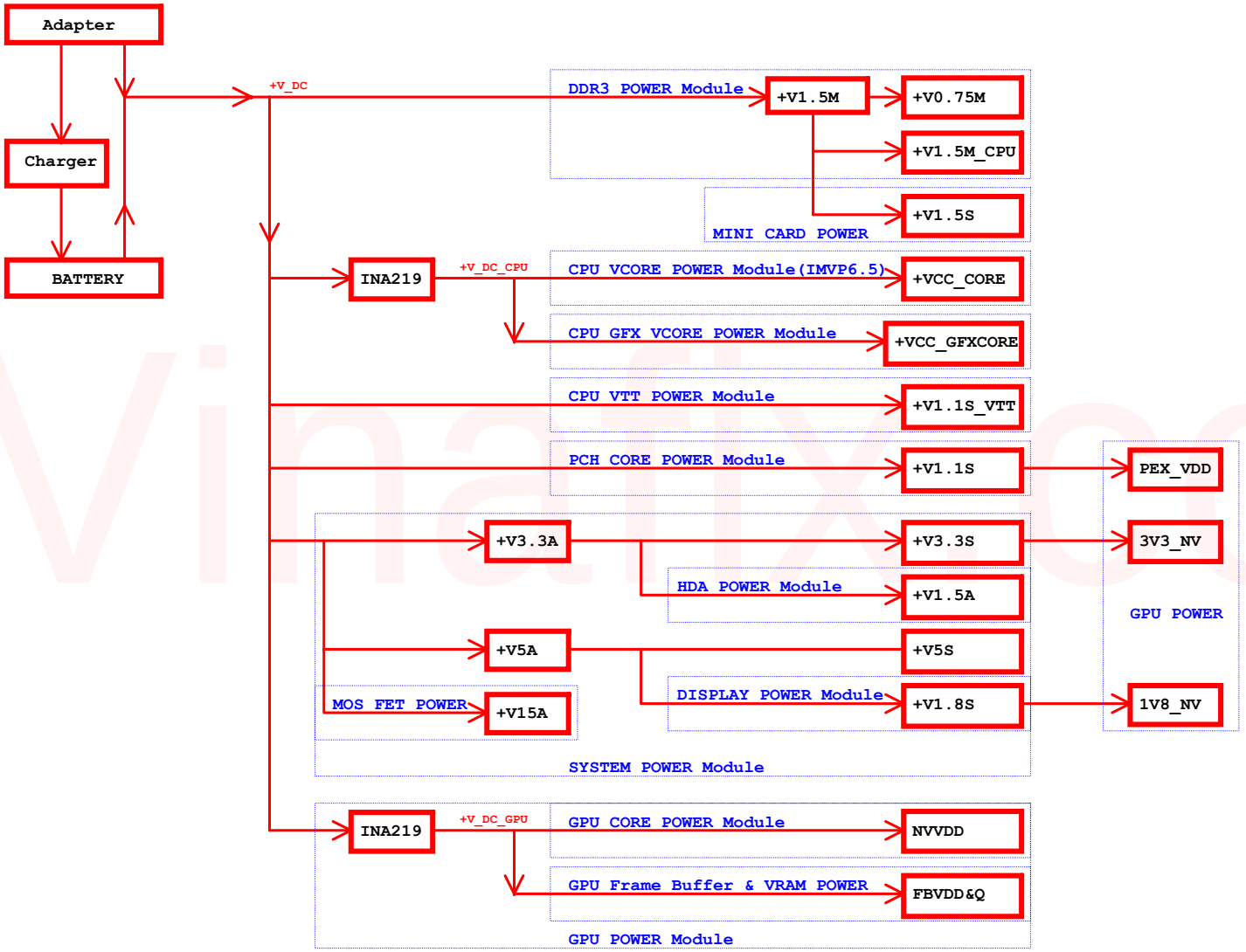
POWER Delivery Architectural Block Diagram

POWER Delivery Architectural Block Diagram



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C	Power_Block	A

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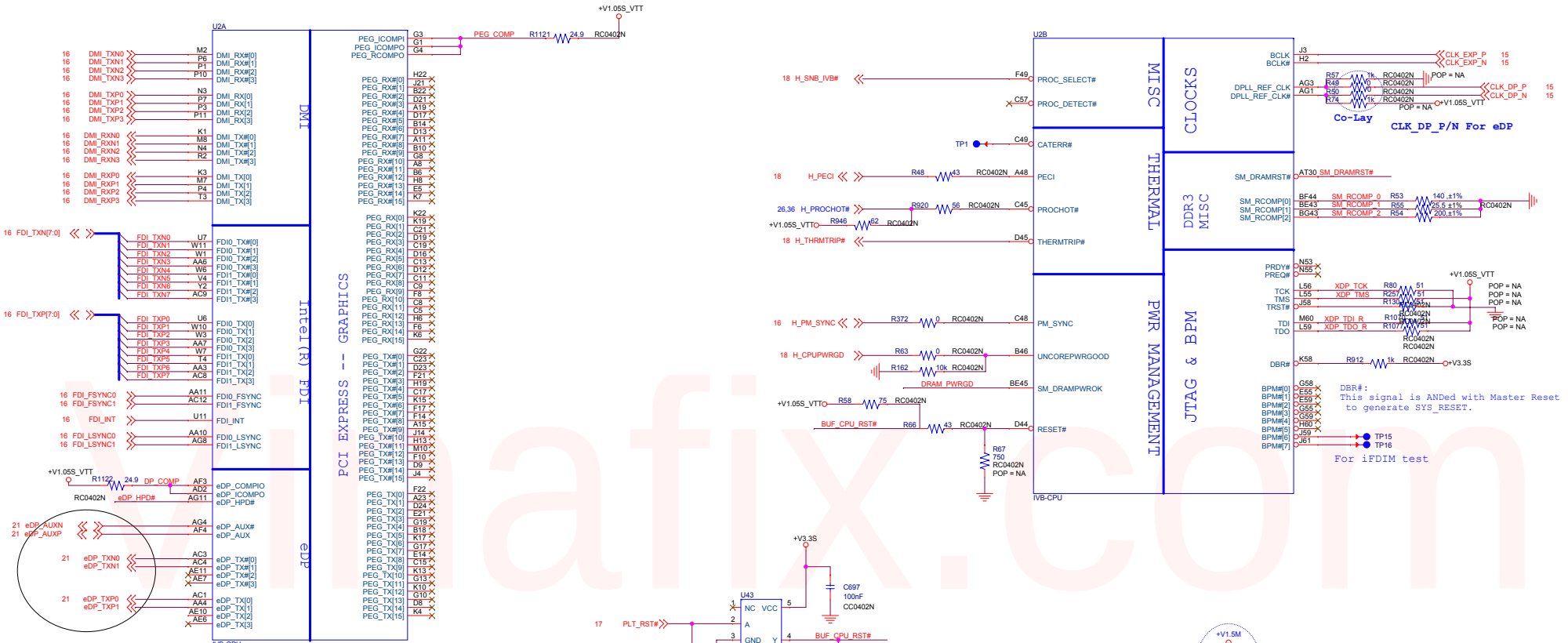
CAD NOTE: PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

Host Clock Routing Topology

Host clock (100 MHz DMI/BCLK and 120 MHz e-DP clocks) routes out of PCH do not need any series termination.



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Size	Sheet Name	Rev
C	CPU1	A

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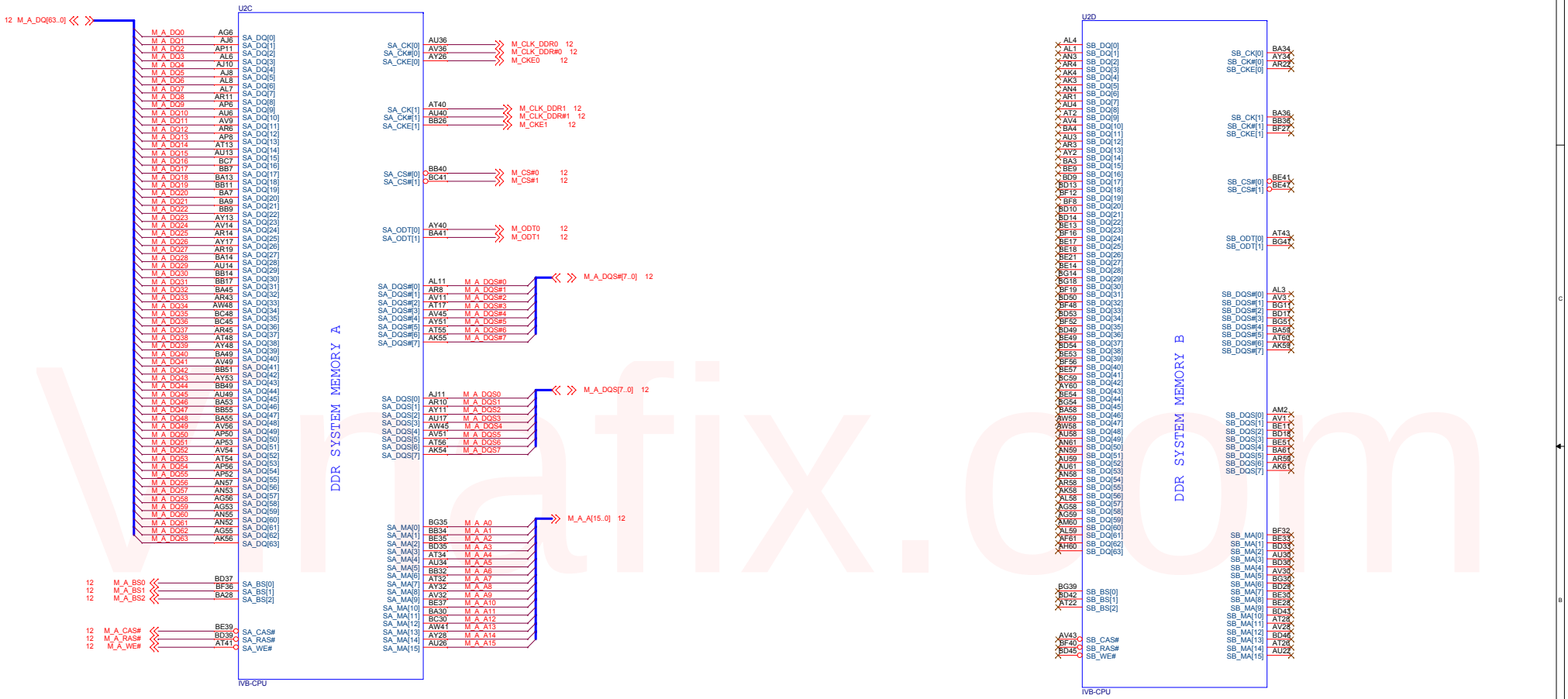

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Size	Sheet Name	Rev
C	CPU2	A

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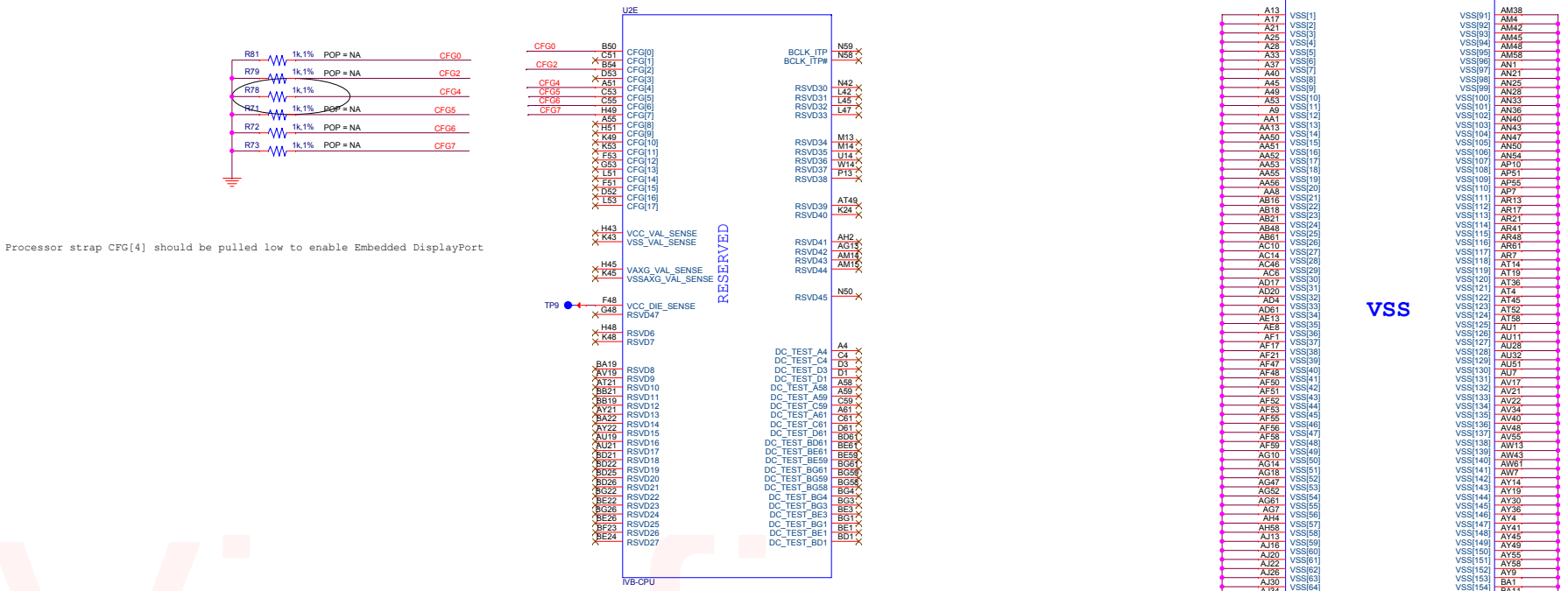

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Size	Sheet Name	Rev
C	CPU3	A

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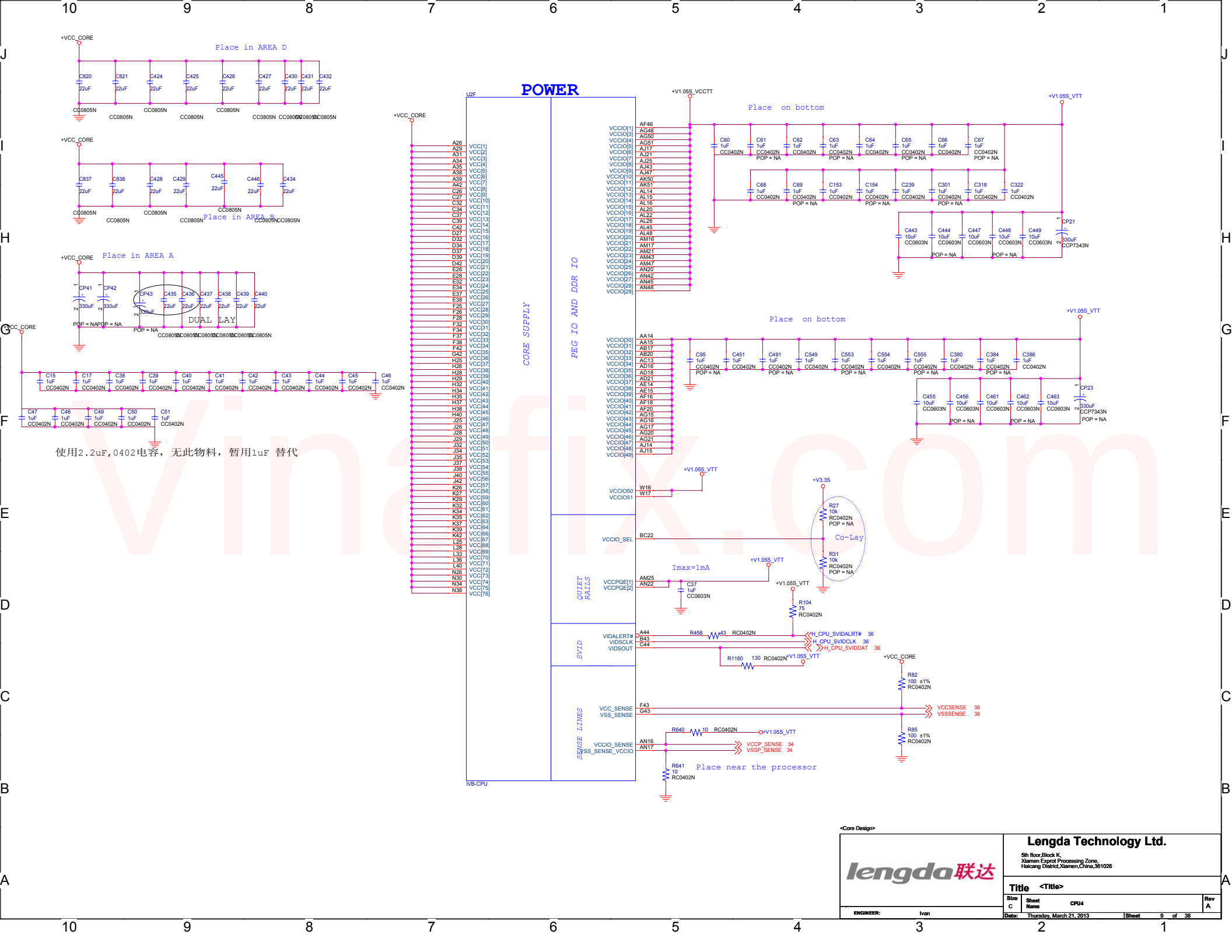
POWER
Place in AREA D
Place in AREA B
Place in AREA A
DUAL LAY
Place on bottom
Place on bottom
Place near the processor
使用2.2uF,0402电容，无此物料，暂用1uF 替代
U2F
IVB-CPU
CORE SUPPLY
PEG IO AND DDR IO
QUIET RAILS
SVID
SENSE LINES
Imax=1mA
Co-Lay
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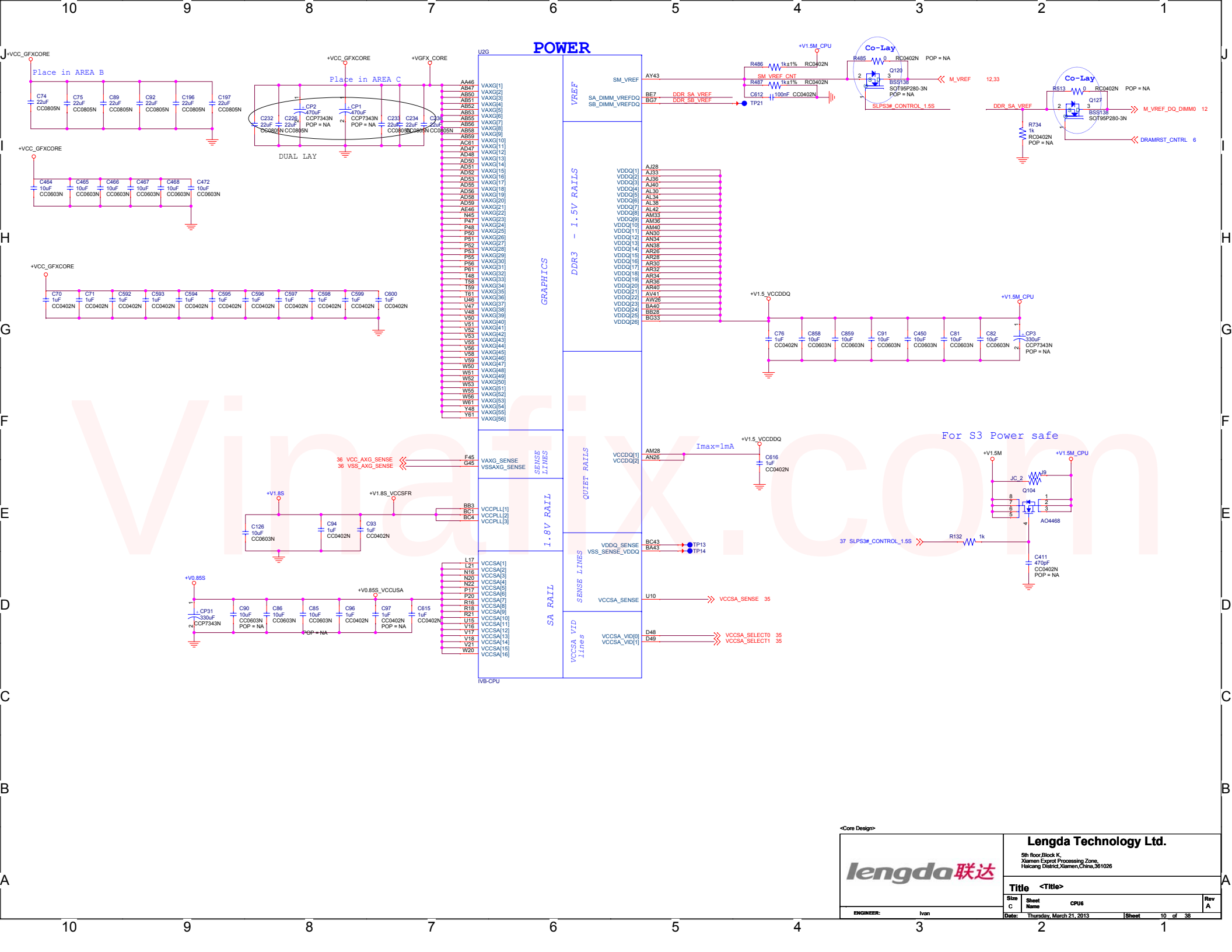
POWER
U2G
GRAPHICS
VREF
DDR3 - 1.5V RAILS
SENSE LINES
QUIET RAILS
1.8V RAIL
SA RAIL
VCCSA VID lines
IVB-CPU
Place in AREA B
Place in AREA C
DUAL LAY
Co-Lay
For S3 Power safe
Imax=1mA
+VCC_GFXCORE
+VGFX_CORE
+V1.5M_CPU
+V1.5_VCCDDQ
+V1.8S
+V1.8S_VCCSFR
+V0.85S
+V0.85S_VCCUSA
SM_VREF
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
DDR_SA_VREF
DDR_SB_VREF
SM_VREF_CNT
SLPS3#_CONTROL_1.5S
M_VREF
M_VREF_DQ_DIMM0
DRAMRST_CNTRL
VAXG_SENSE
VSSAXG_SENSE
VDDQ_SENSE
VSS_SENSE_VDDQ
VCCSA_SENSE
VCCSA_SELECT0
VCCSA_SELECT1
AO4468
BSS138
SOT95P280-3N
POP = NA
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Title <Title>
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Rev A
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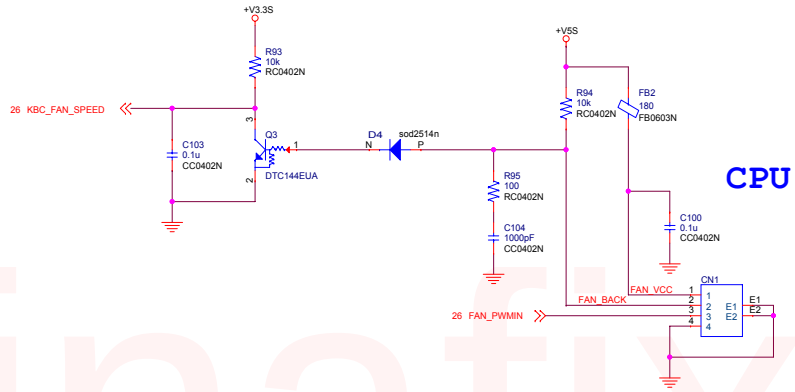

CPU FAN Control

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C	THERMAL	A

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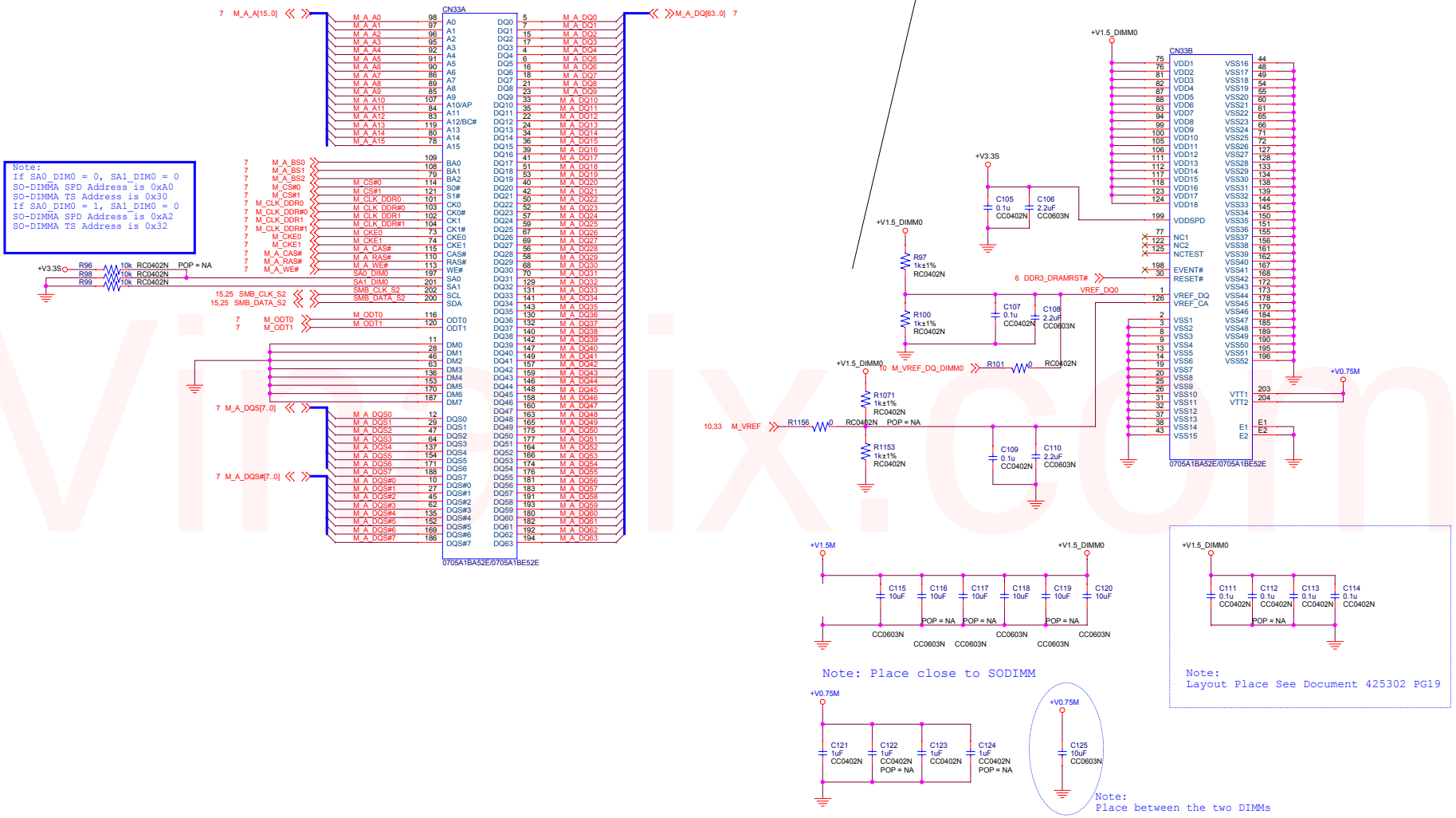
DDR3 SODIMM0



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Size	Sheet Name	Rev
C	DDR3_SODIMM0	A

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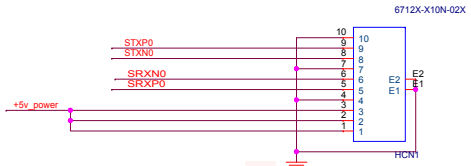
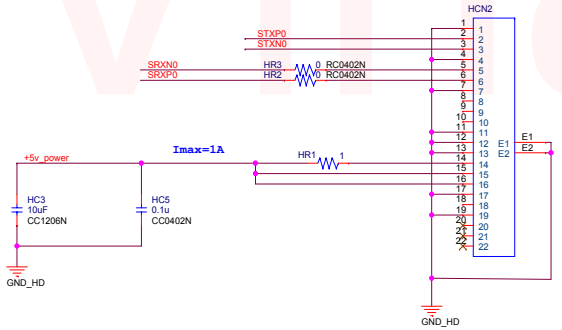
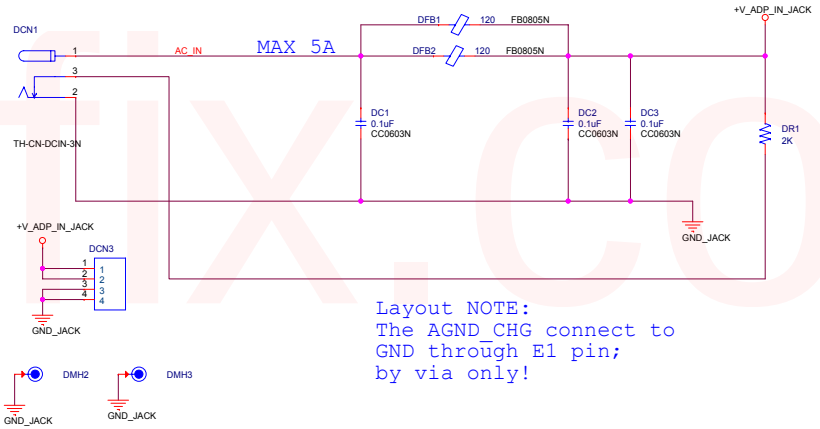
HDD CONN



HDD CONN



ADP_IN



Layout NOTE:
The AGND_CHG connect to
GND through E1 pin;
by via only!

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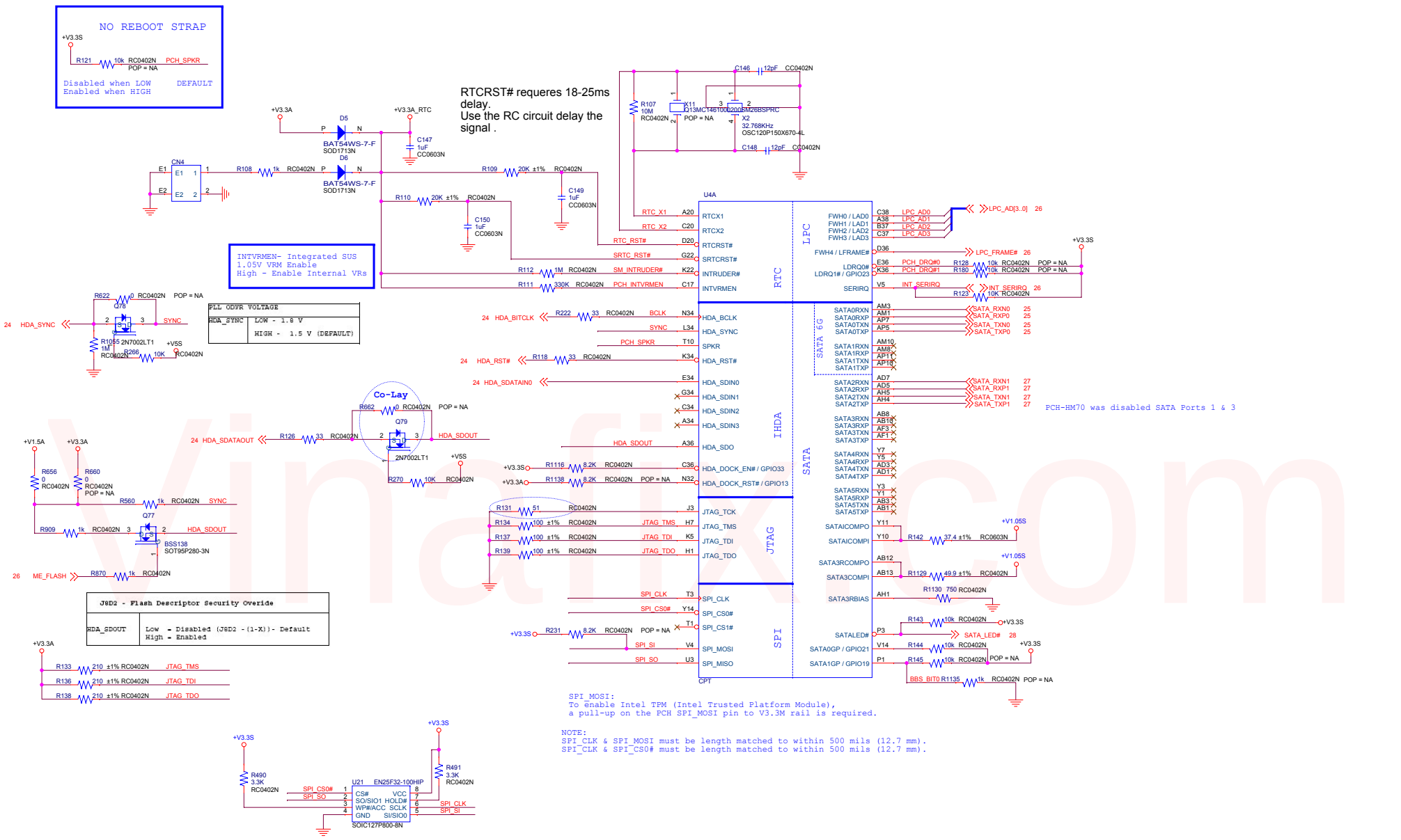

HDA_SDO is a signal used for Flash Descriptor Security Override/ME Debug Mode. It has a weak internal pull-down. When it is sampled high, via external pull up, the Flash Security gets overridden. This signal should be only asserted high through external pull up (1K±5%) ONLY.

GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. It has a weak internal pull-up. When GPIO33 is sampled low, the Flash Security gets overridden as well as Intel ME gets halt. This signal should be only asserted low through an external pull-down (1 kW ±5%) in manufacturing or debug environments ONLY.

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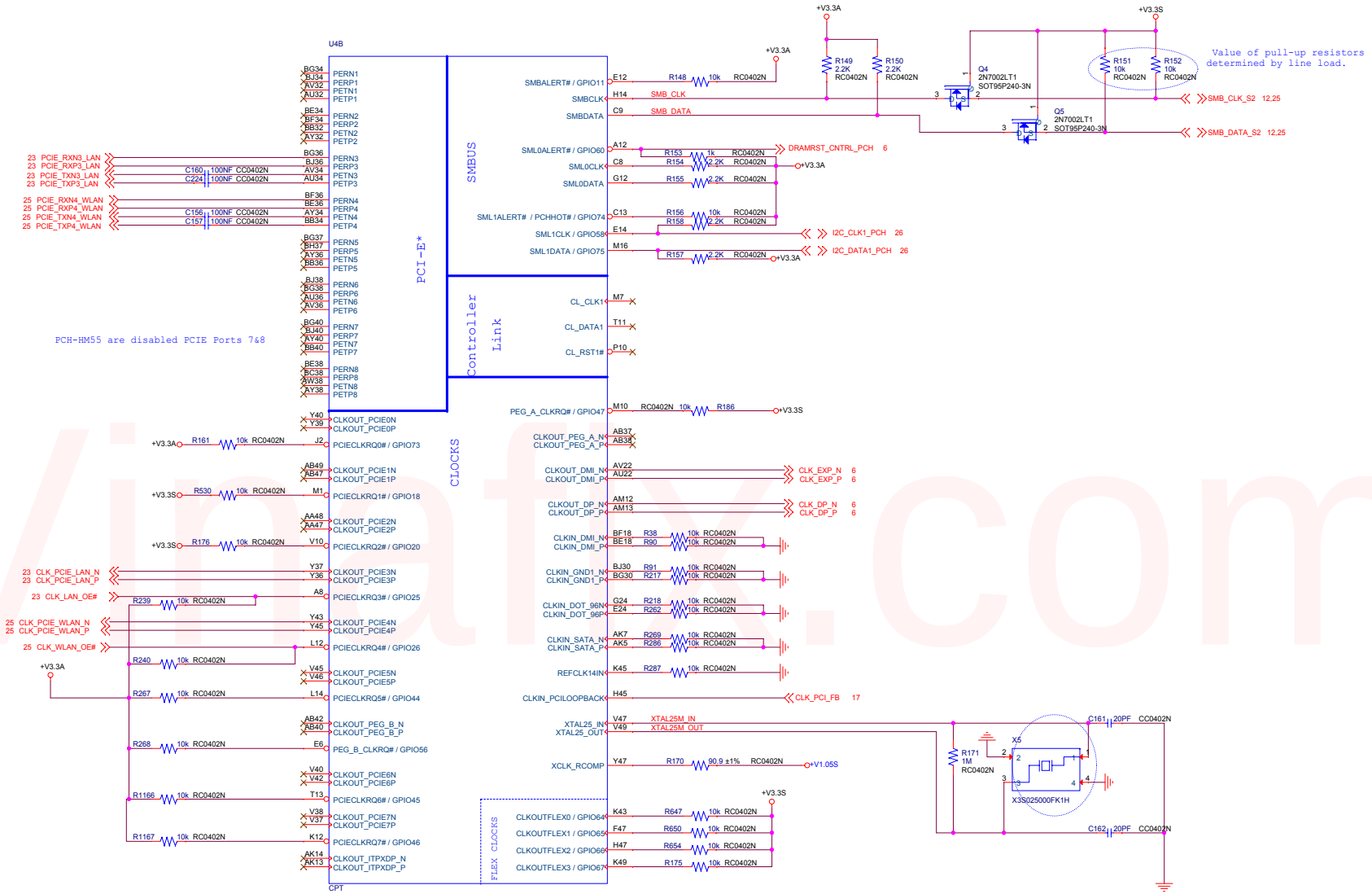

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Size	Sheet Name	Rev
C	PCH2	A

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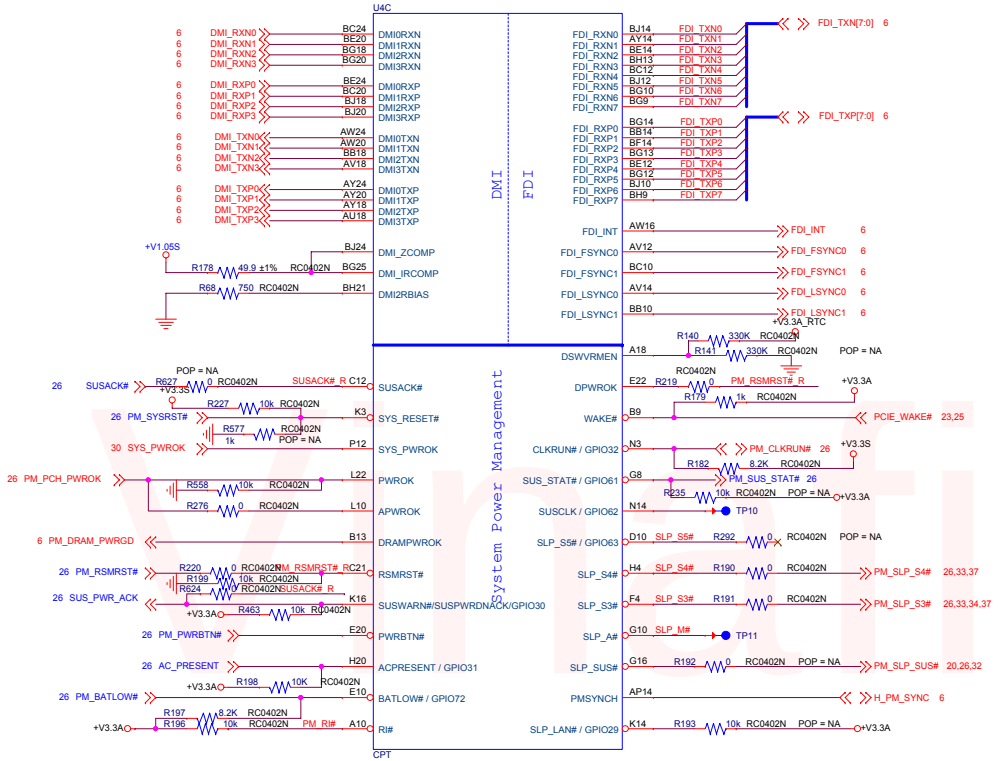
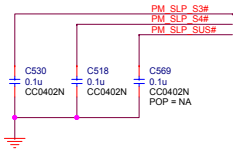
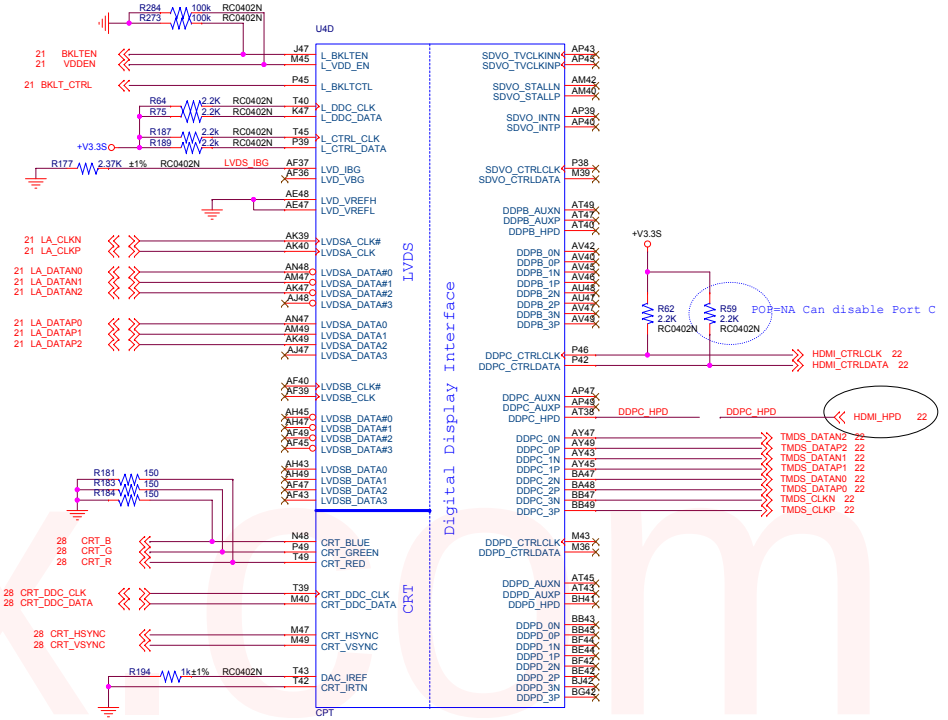


SLP_M#:
Can be left as NC when Intel AMT is not supported on the platform.
MEPWROK:
Should be asserted when all Intel ME power rails are up and stable.
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



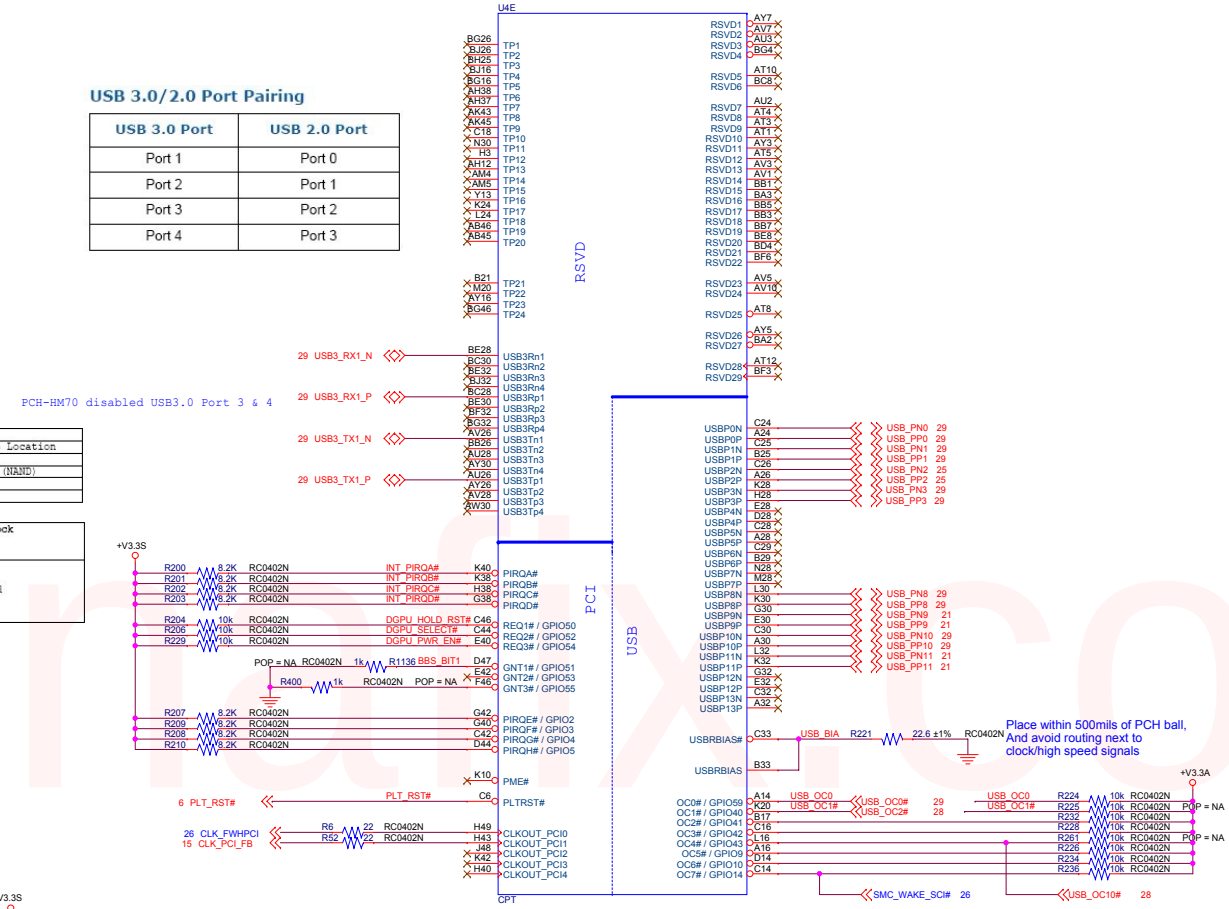


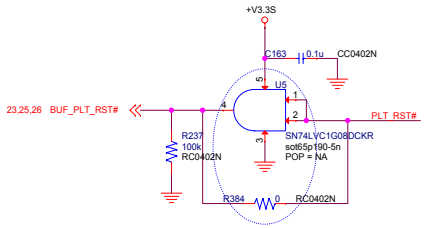
USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default





Allocation	USB Devices
USB0	USB3.0 Port1
USB1	Fingerprint
USB2	Port 2
USB3	Cardreader
USB4	NA
USB5	NA
USB8	Port 3
USB9	Camera
USB10	WLAN
USB11	TOUCH PANEL
USB12	NA
USB13	NA

PCH-HM70 disabled USB2.0 Port 4,5,6,7 & 12,13
PCH-HM76 disabled USB2.0 Port 6,7

OC Pin	PCH Mapping
OC#0	Port 0 & 1
OC#1	Port 2 & 3
OC#2	Port 4 & 5
OC#3	Port 6 & 7
OC#4	Port 8 & 9
OC#5	Port 10 & 11
OC#6	Port 12 & 13
OC#7	Floater OC# (not used)

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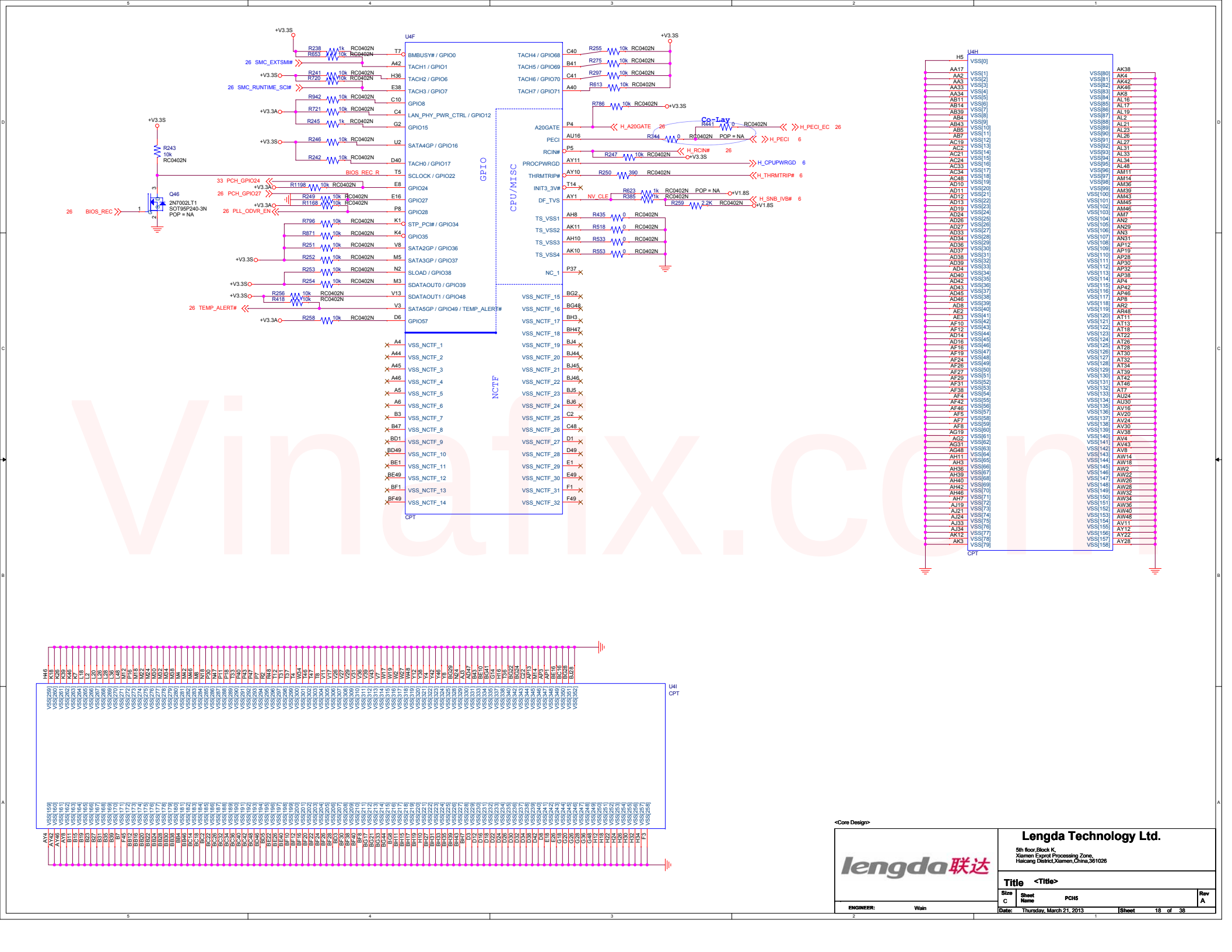

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Size	Sheet Name	Rev
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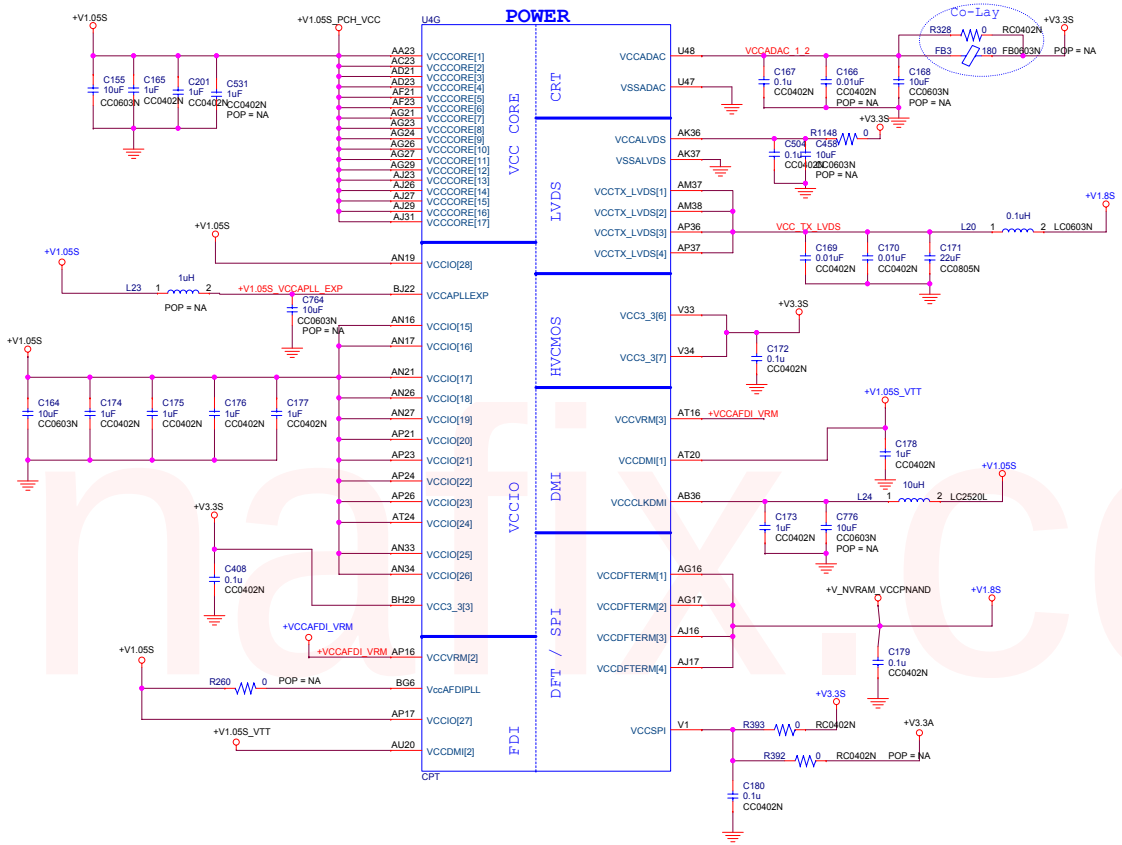

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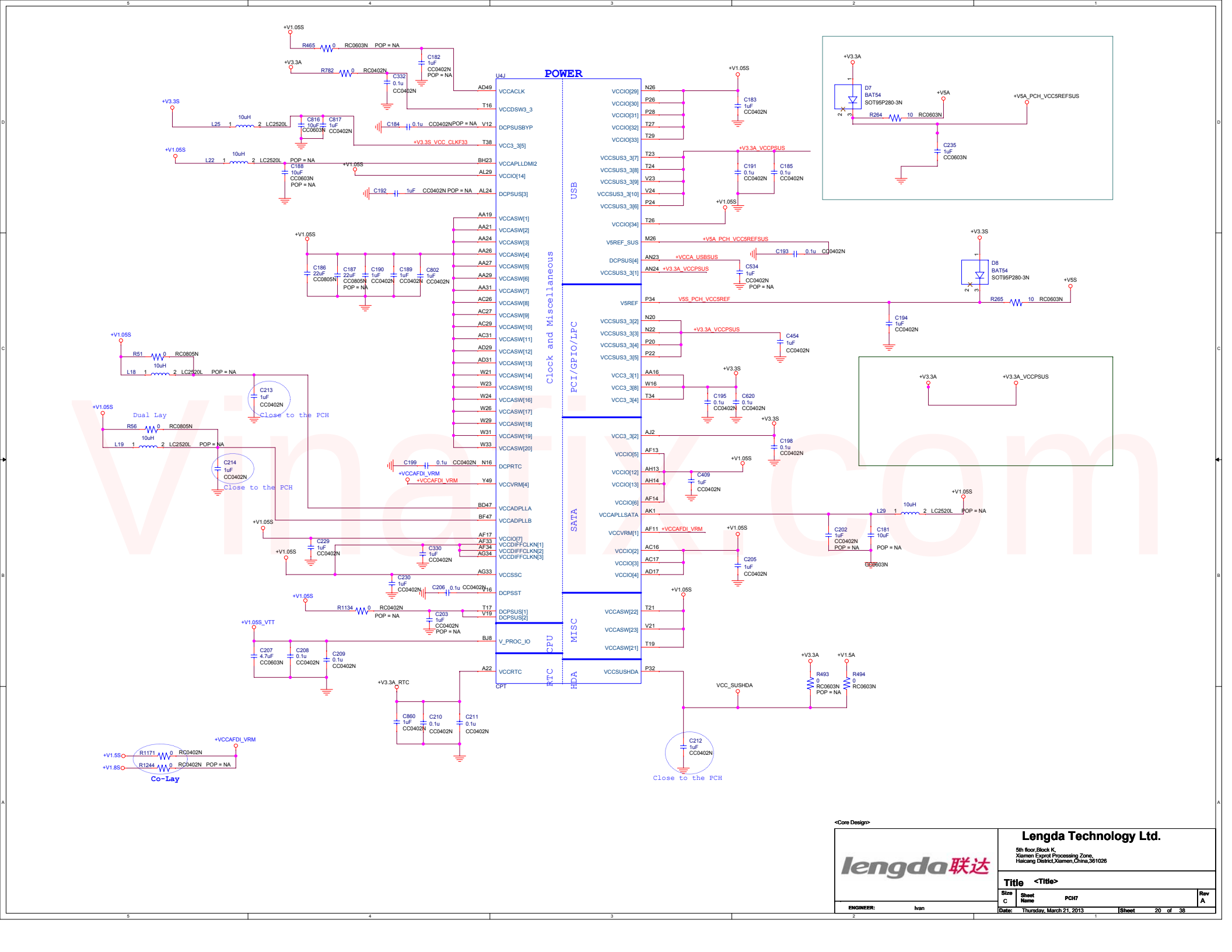

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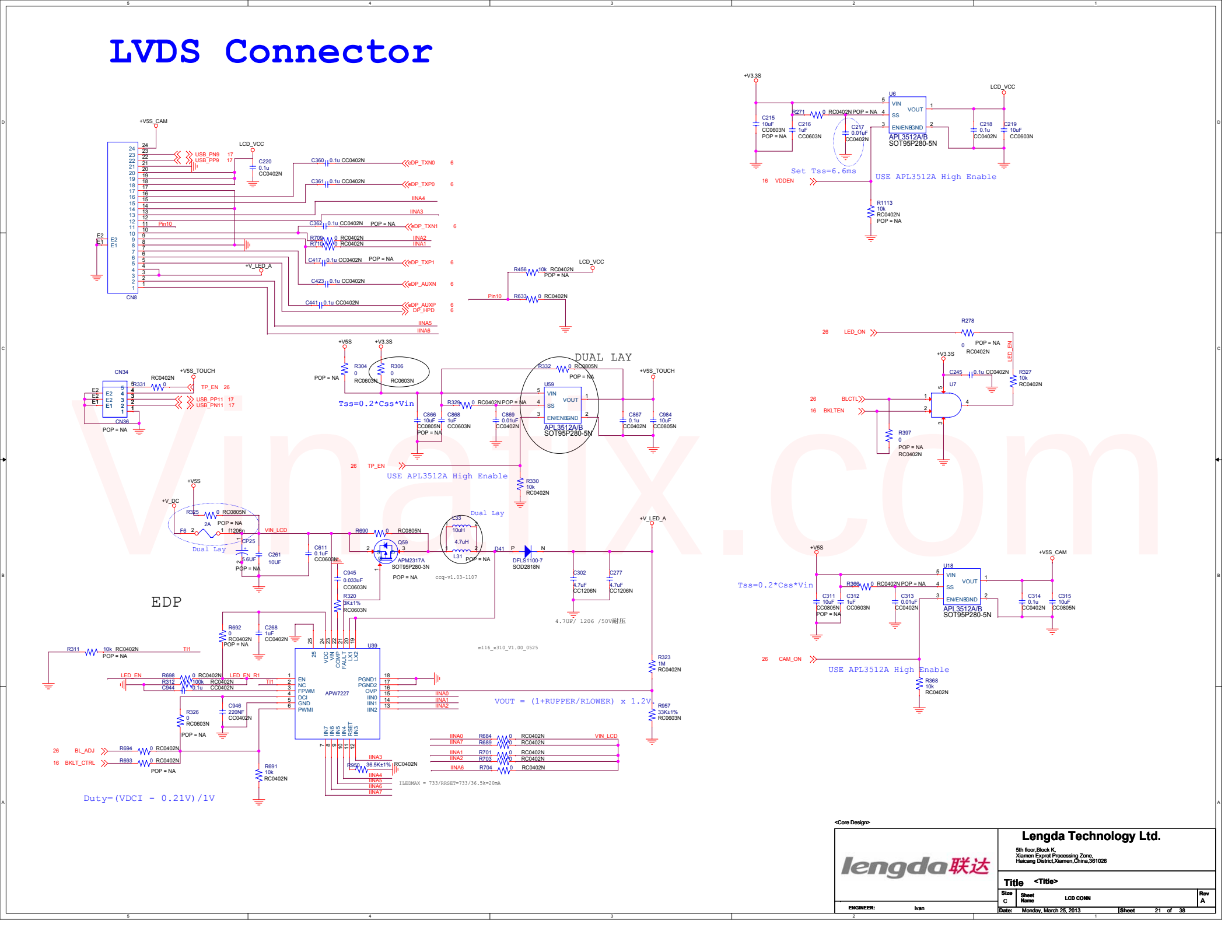
LVDS Connector



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Size	Sheet Name	Rev
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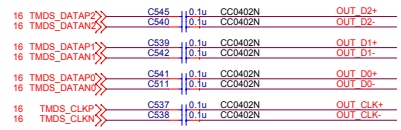

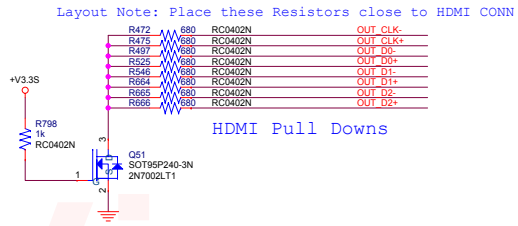

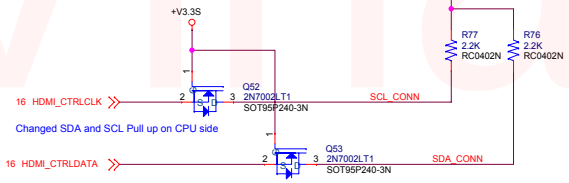

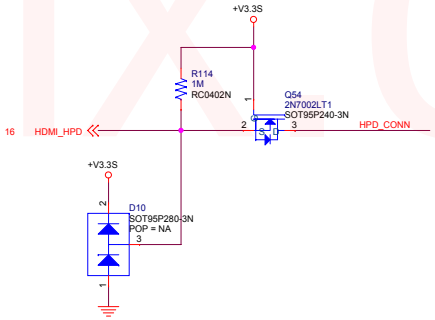

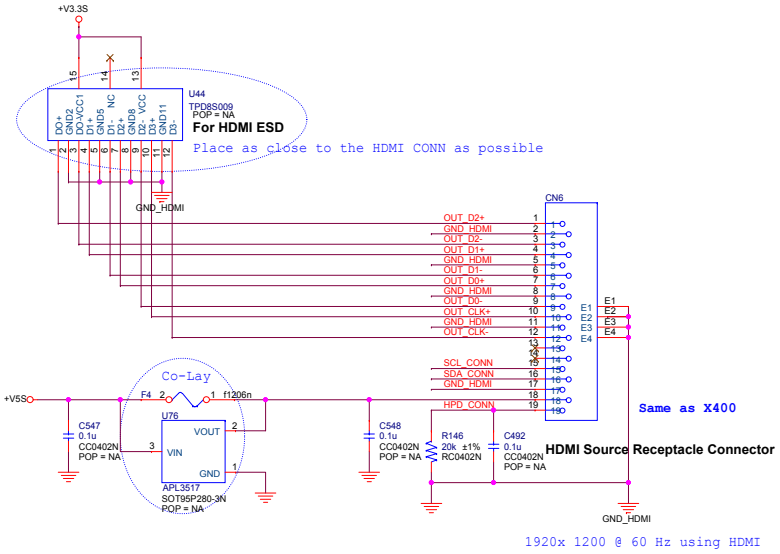

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Size	Sheet Name	Rev
C	HDMI Port	A

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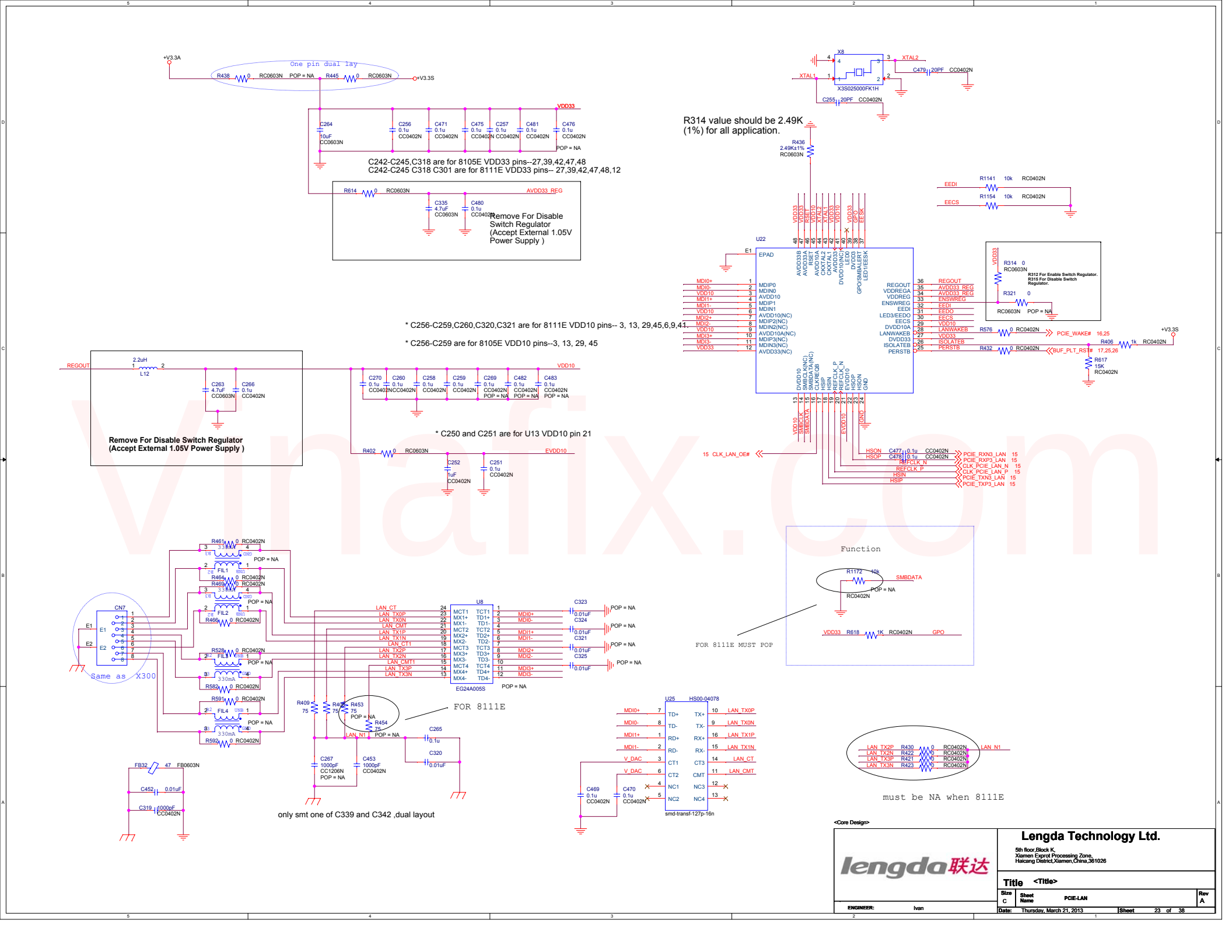
C242-C245,C318 are for 8105E VDD33 pins--27,39,42,47,48
C242-C245 C318 C301 are for 8111E VDD33 pins-- 27,39,42,47,48,12
Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)
R314 value should be 2.49K (1%) for all application.
* C256-C259,C260,C320,C321 are for 8111E VDD10 pins-- 3, 13, 29,45,6,9,41.
* C256-C259 are for 8105E VDD10 pins--3, 13, 29, 45
* C250 and C251 are for U13 VDD10 pin 21
Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)
FOR 8111E
FOR 8111E MUST POP
Function
only smt one of C339 and C342 ,dual layout
must be NA when 8111E
Same as X300
EG24A005S
smd-transf-127p-16n
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Rev A
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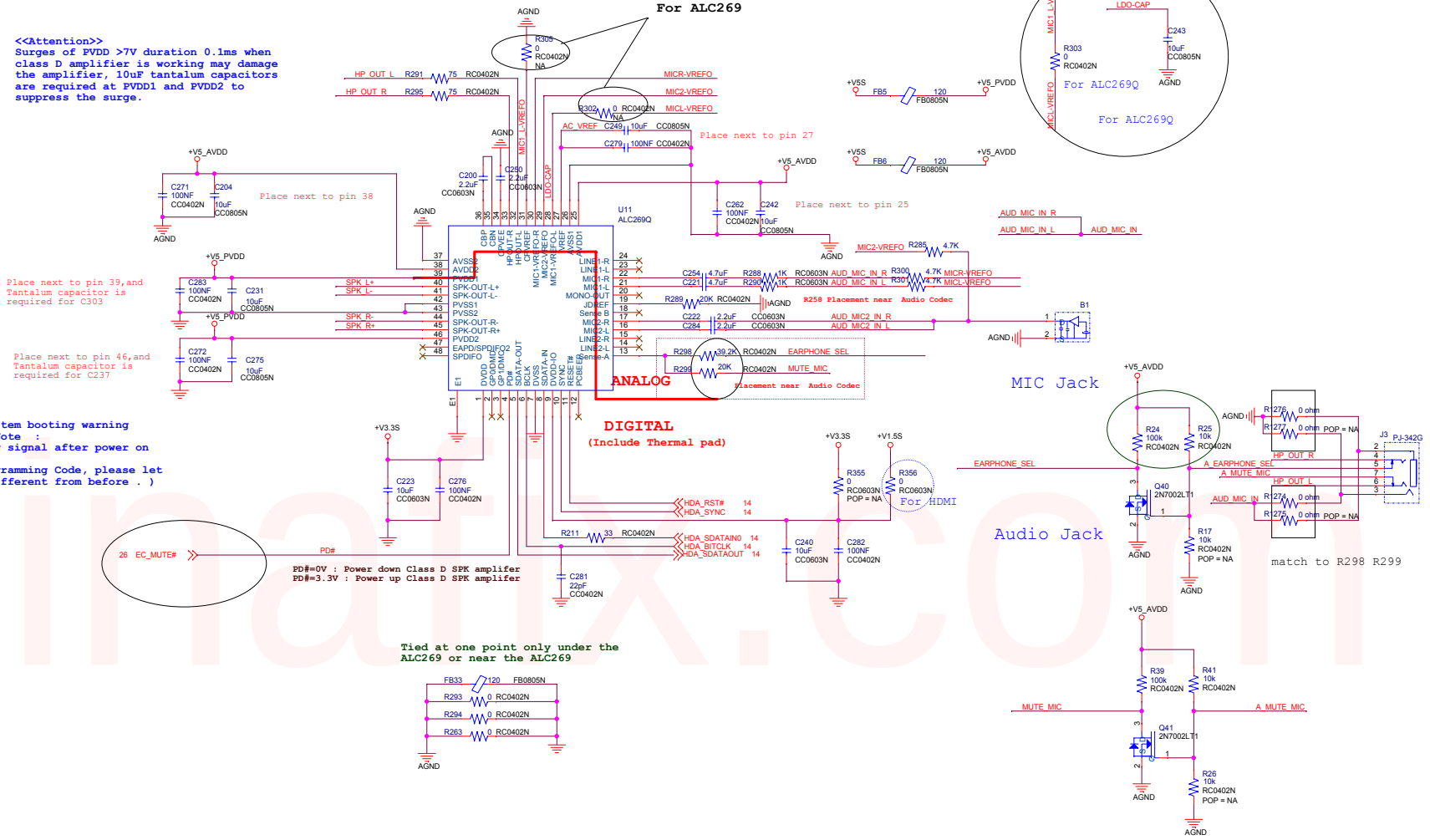
notice: if use ALC269, then r226,r227 is used r226, c243 is NC.
if use ALC269Q, then use R226,C243, r226,r227 is NC

For ALC269

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2.When you want to exit your Bios Programming Code, please let the EC_MUTE# Low.(The programming is different from before .)



<<Attention>>
If mount the LC filter((L9~L12;C295/C299;C300/C293/C294/C296),Please let them together and close to codec. If the PCB trace and Speaker wire length is less than 20cm, don't need the LC filter(L9~L12;C295/C299) to eliminate the EMI,If L9,L0,L11,L12 are replaced by 0 ohm/1.6A resistetor(please don't use general bead, because it may influence the THD+N quality) ,and C295,C299 should be NC.And,please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
C300/C293/C294/C296 are reserved for EMI fine-tune ; For EMI issue, please also refer our ALC269 Layout guide document

Tied at one point only under the ALC269 or near the ALC269

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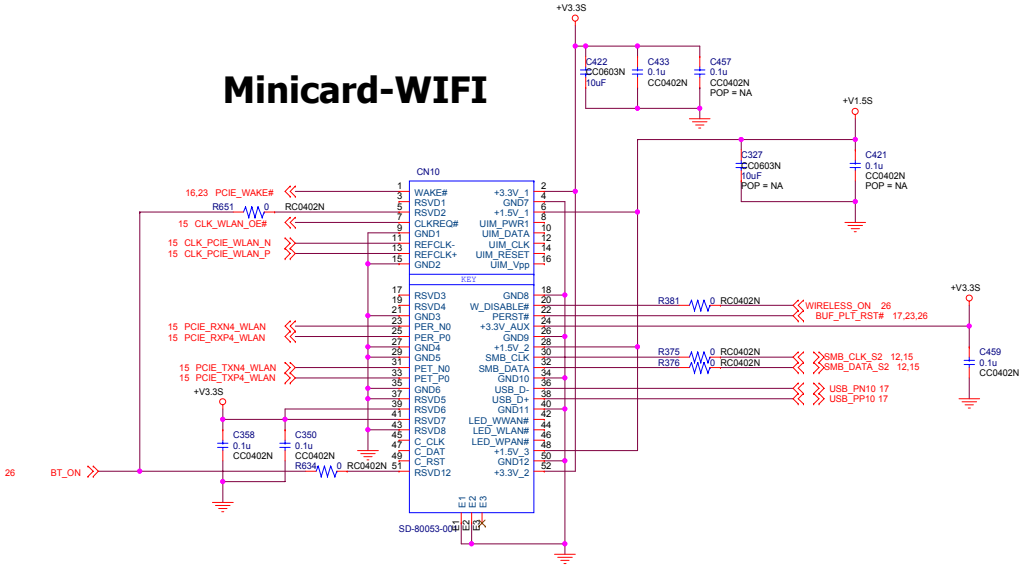
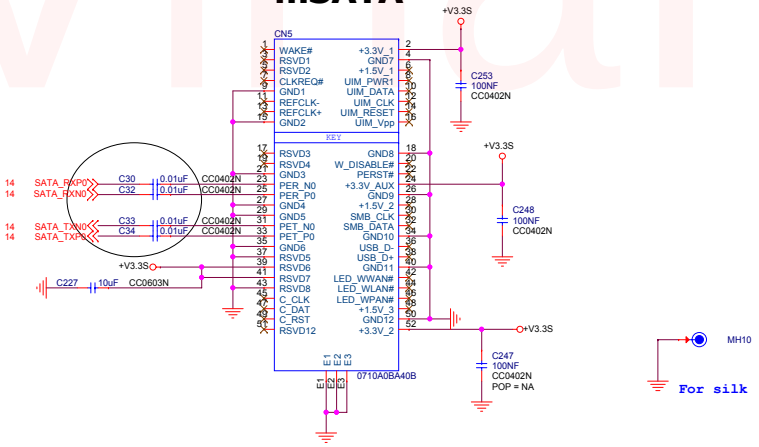
Minicard-WIFI



mSATA



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Size	Sheet Name	Rev
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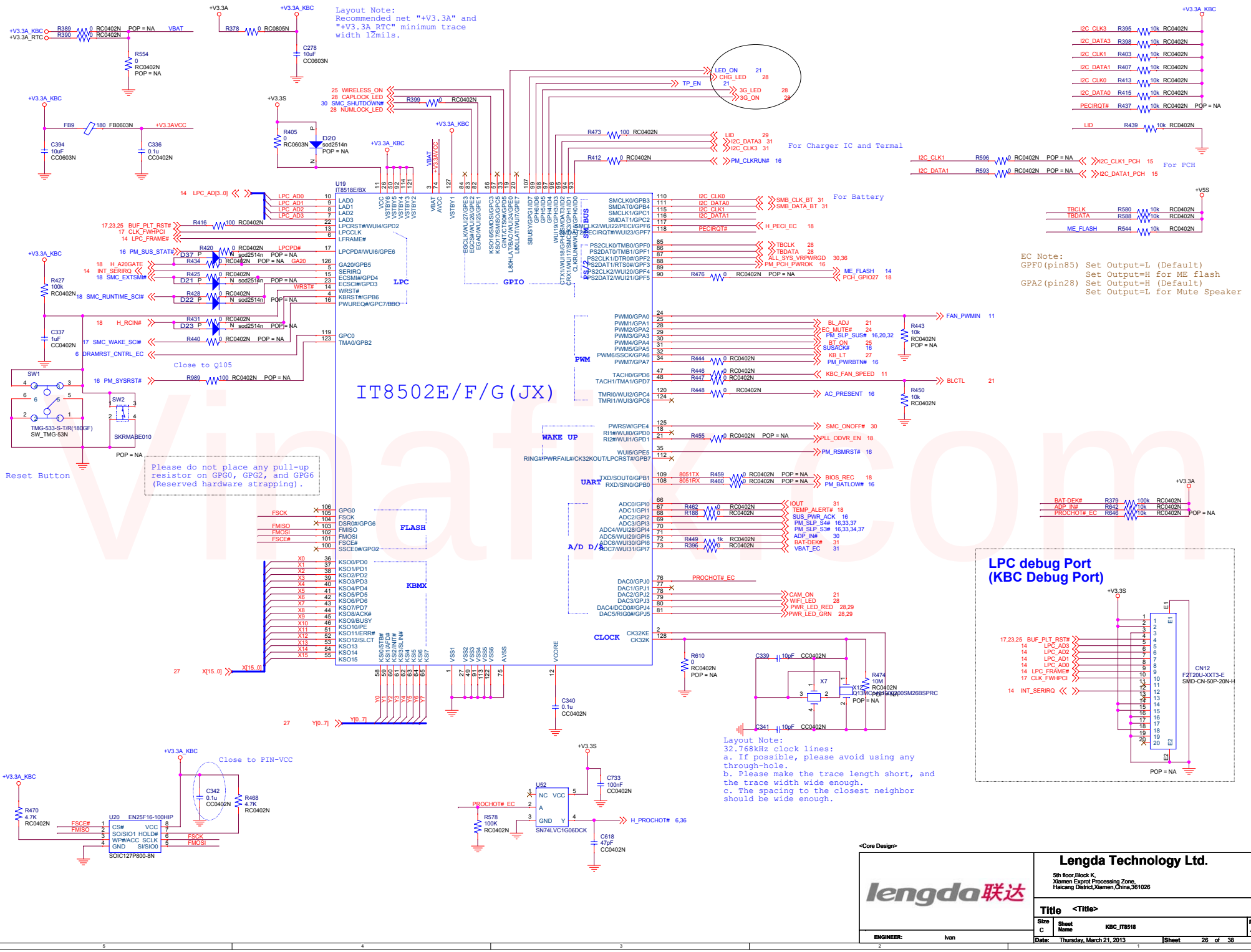
IT8502E/F/G(JX)
Layout Note:
Recommended net "+V3.3A" and "+V3.3A_RTC" minimum trace width 12mils.
For Charger IC and Termal
For Battery
For PCH
EC Note:
GPF0(pin85) Set Output=L (Default)
Set Output=H for ME flash
GPA2(pin28) Set Output=H (Default)
Set Output=L for Mute Speaker
Close to Q105
Reset Button
Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).
Close to PIN-VCC
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
LPC debug Port
(KBC Debug Port)
CN12
F2T20U-XXT3-E
SMD-CN-50P-20N-H
LPC
GPIO
PS/2
PWM
WAKE UP
UART
A/D D/A
FLASH
KBMX
CLOCK
SMBUS
U19
IT8518E/BX
U20 EN25F16-100HIP
SOIC127P800-8N
U52
SN74LVC1G06DCK
SW1
SW2
TMG-533-S-T/R(180GF)
SW_TMG-53N
SKRMABE010
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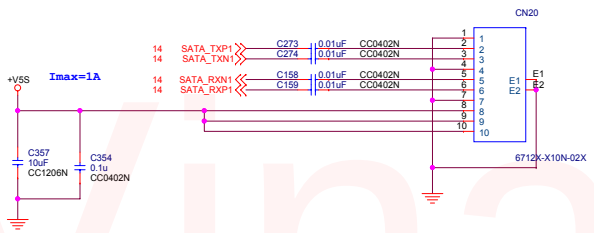
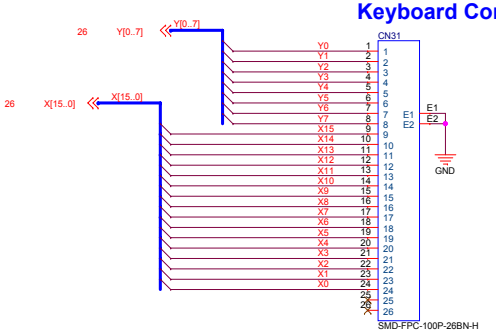
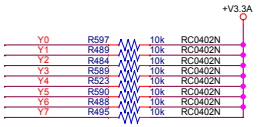
HDD CONN



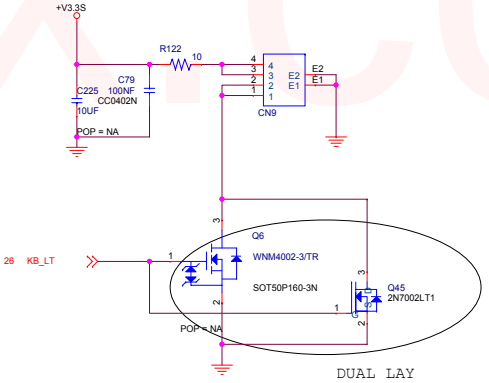
Keyboard Connector



Same as X300



KB LIGHT CONN



DUAL LAY

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ENGINEER: Ivan	Title <Title>	
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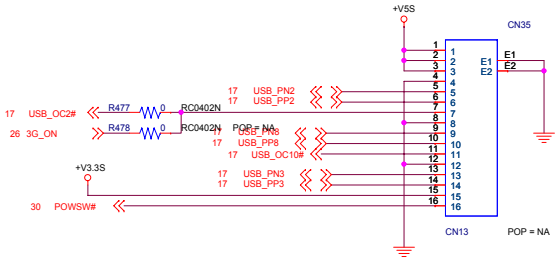
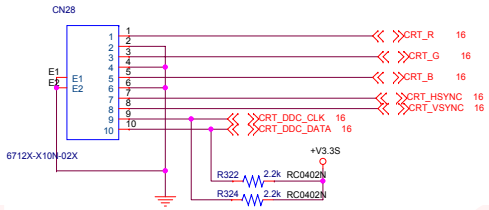
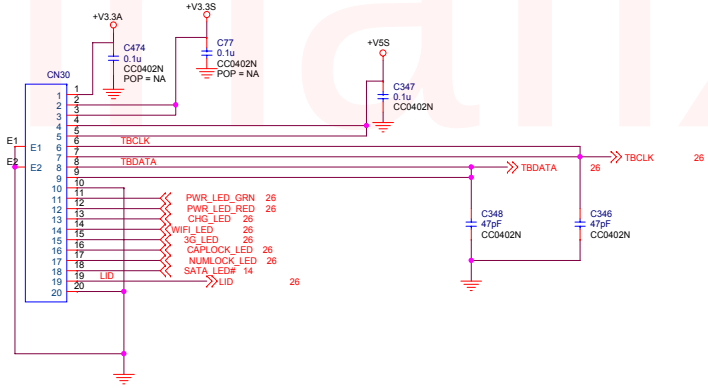
TO USB BOARD







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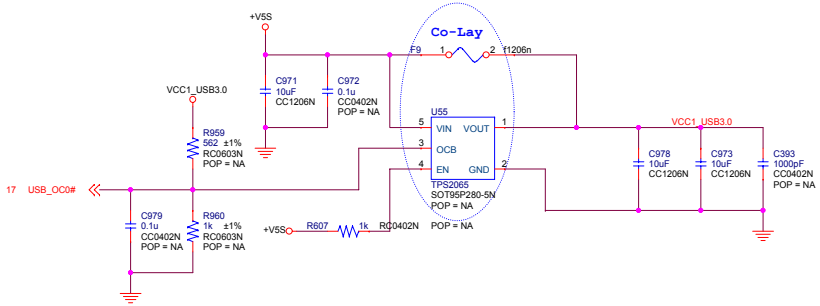

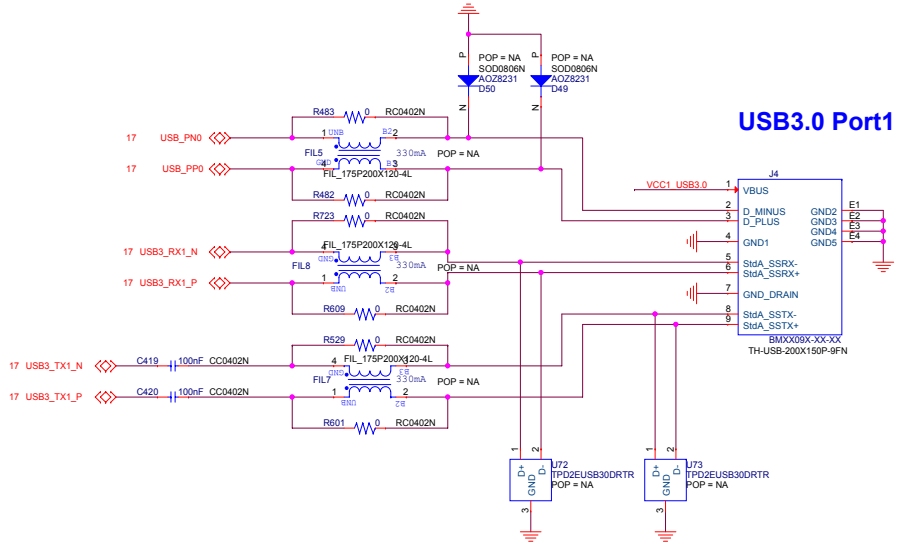

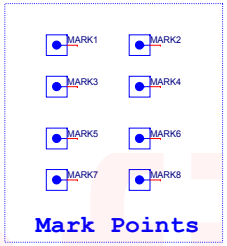

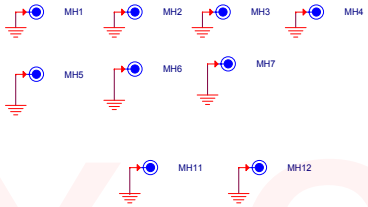

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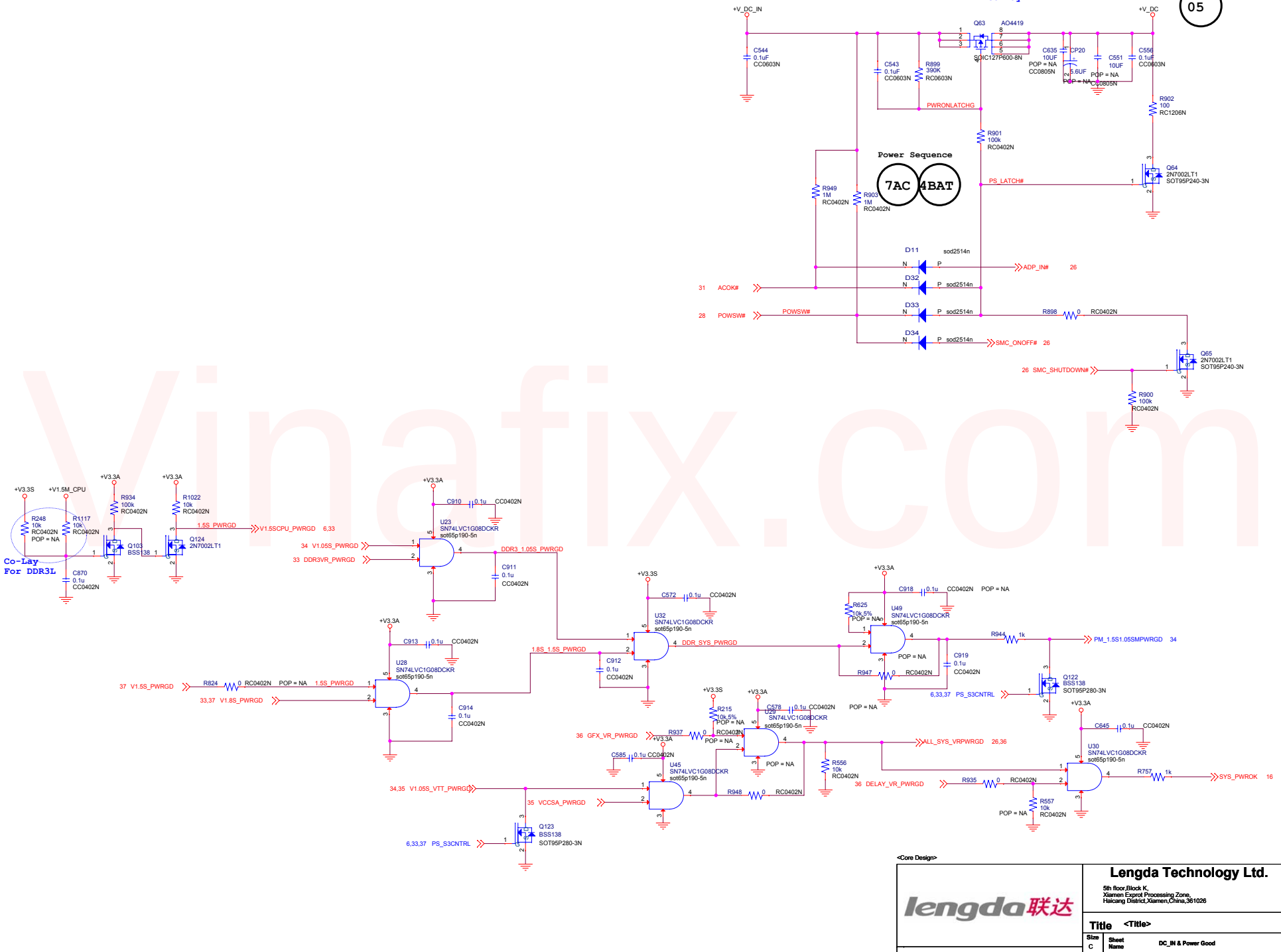
Power Button Detect & Latch

Co-Lay

Power Sequence 05



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Title	<Title>		
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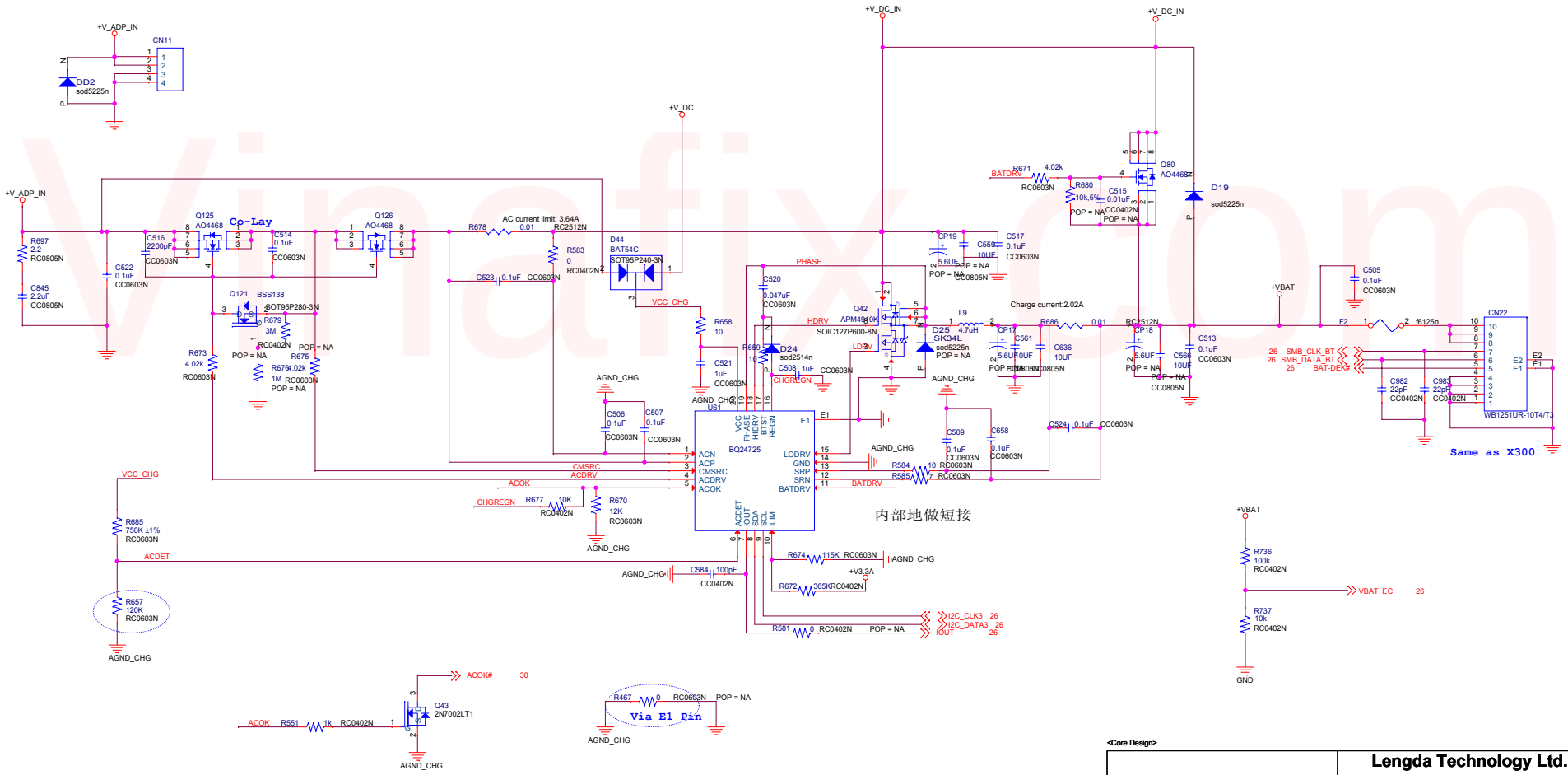

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Size	Sheet Name	Rev
C	Power Charger & Battery Conn	A

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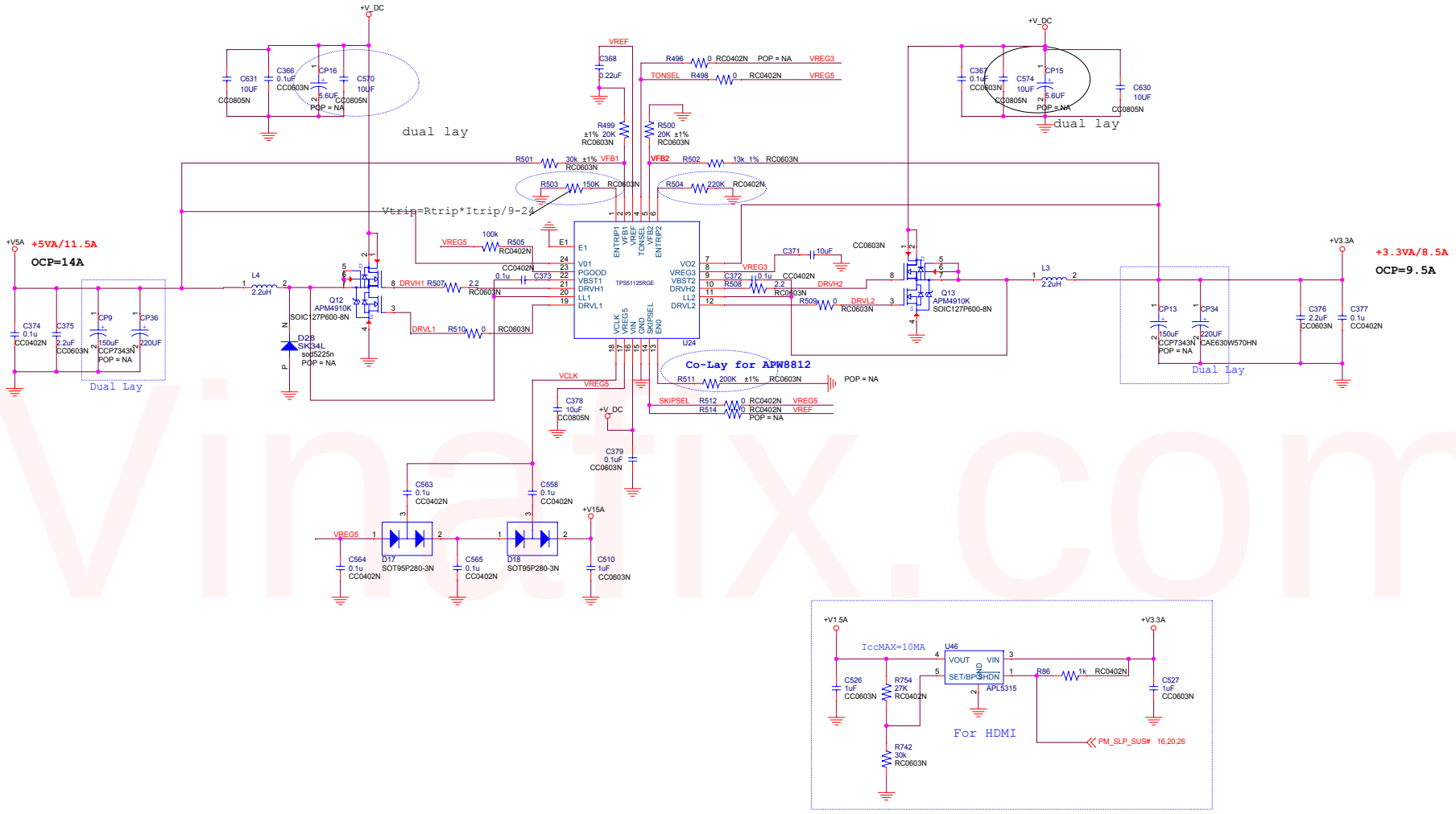

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Size	Sheet Name	Rev
C	Power_System	A

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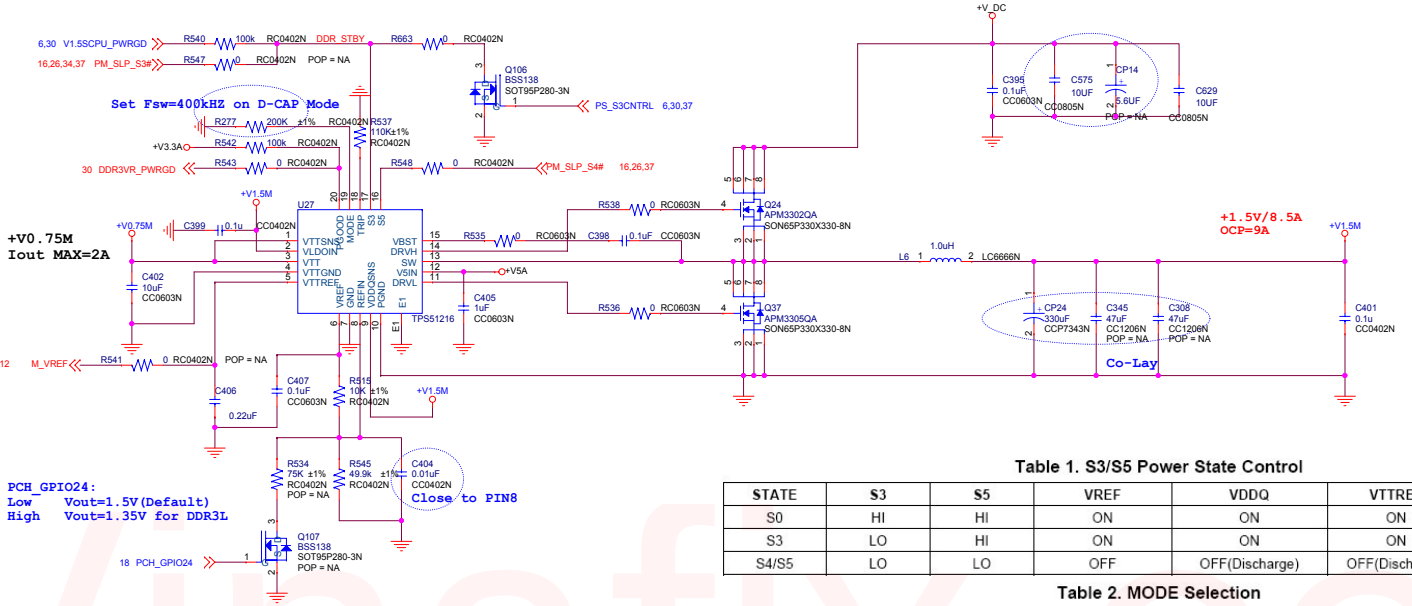

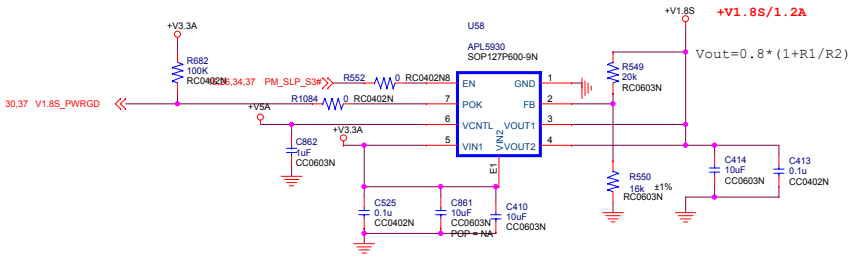

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	

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C	Power_DDR3/DDR3L	A

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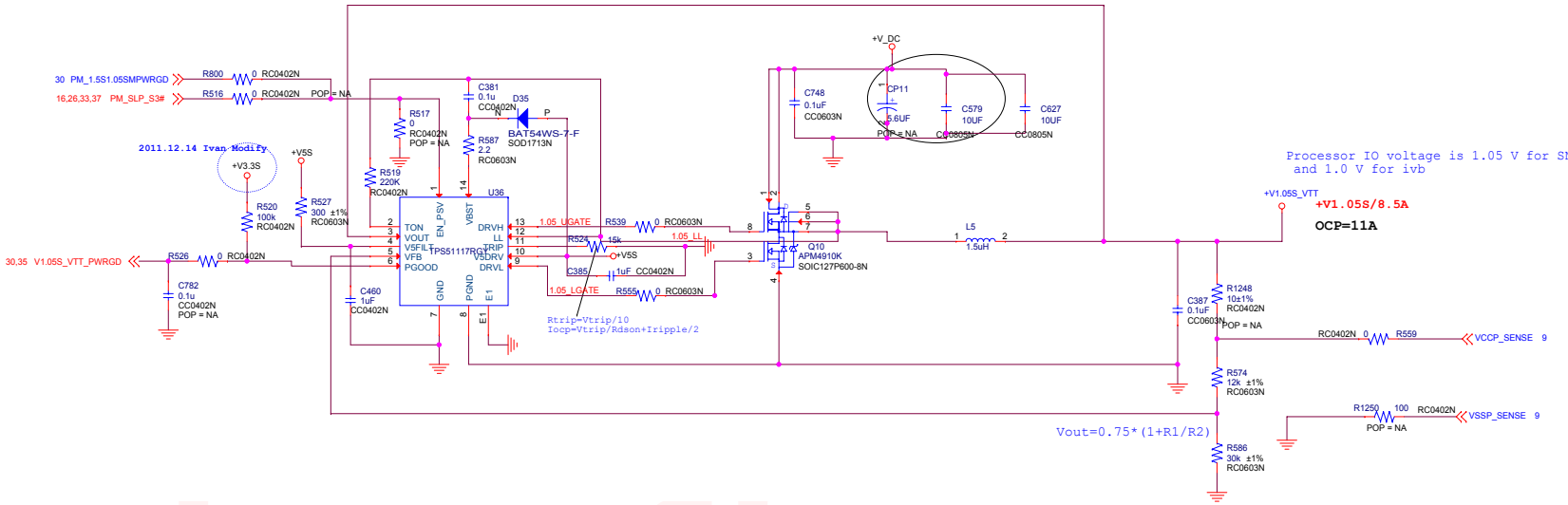

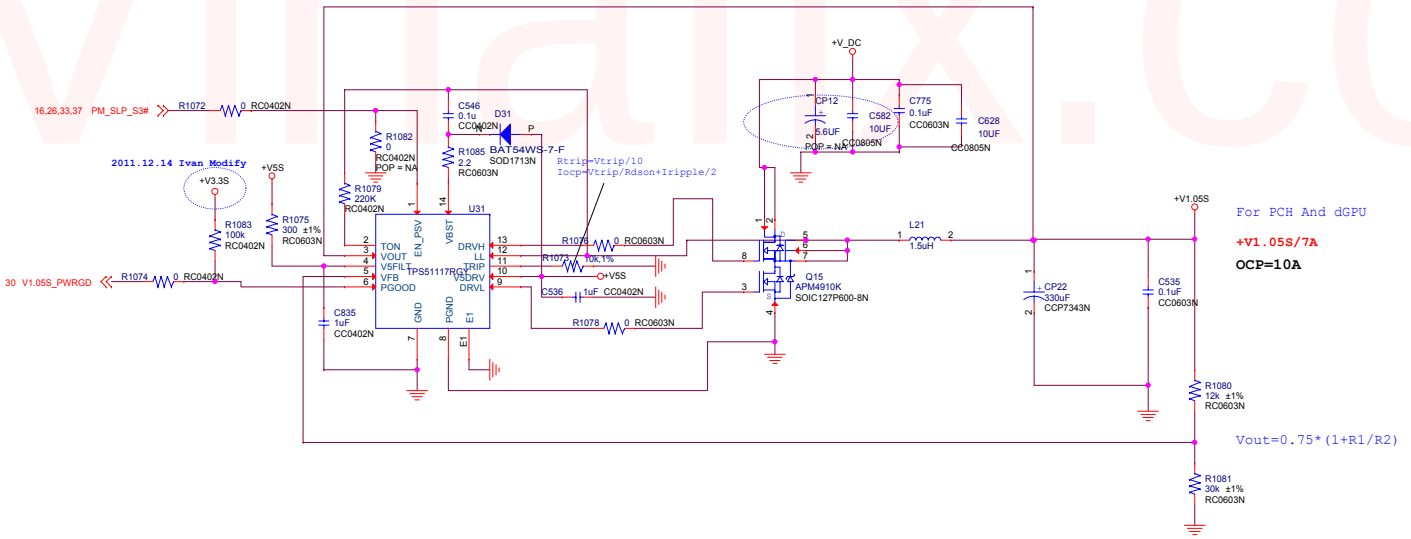

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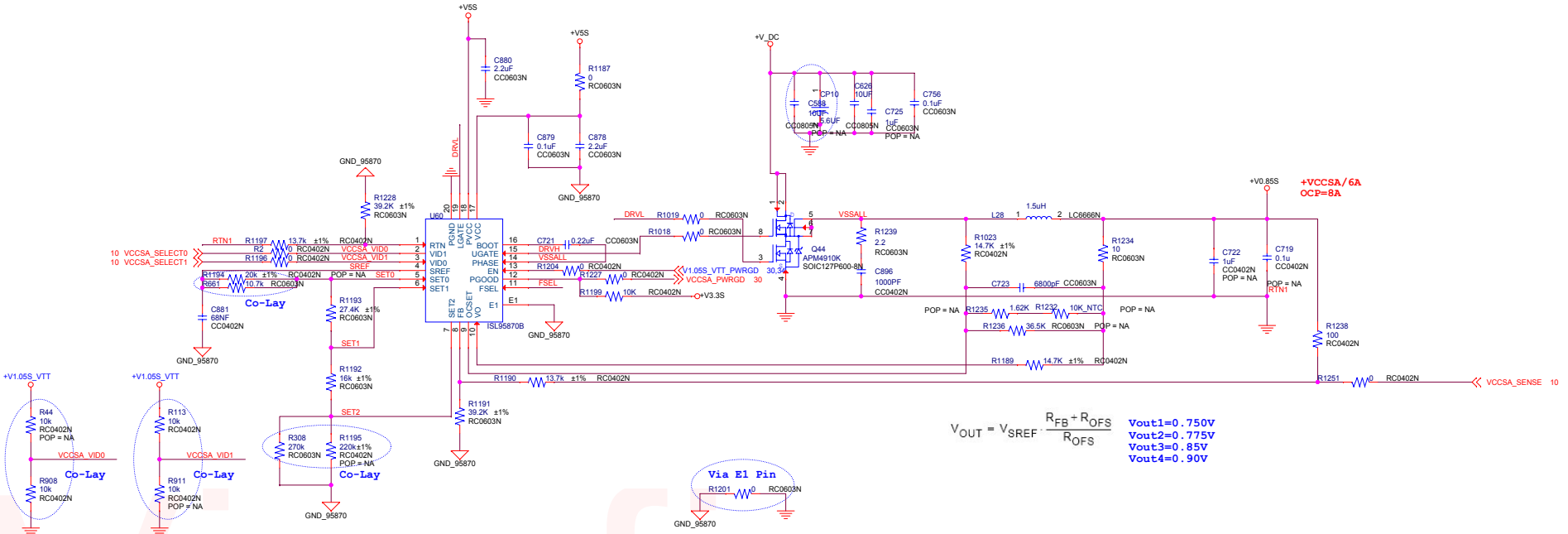

$$V_{OUT} = V_{SREF} \cdot \frac{R_{FB} + R_{OFS}}{R_{OFS}}$$

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

VCCSA_SEL Voltage Selection Table

VID[0] Pin D48	VID[1] Pin D49	VCCSA Vout XE, QC, SV	VCCSA Vout ULV Only
0	0	0.90 V	0.90 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.750 V

FSEL VOLTAGE	FREQUENCY(KHZ)
GND	300KHZ
FLOAT	500KHZ
100K to GND	600KHZ
5.0V	1000KHZ

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

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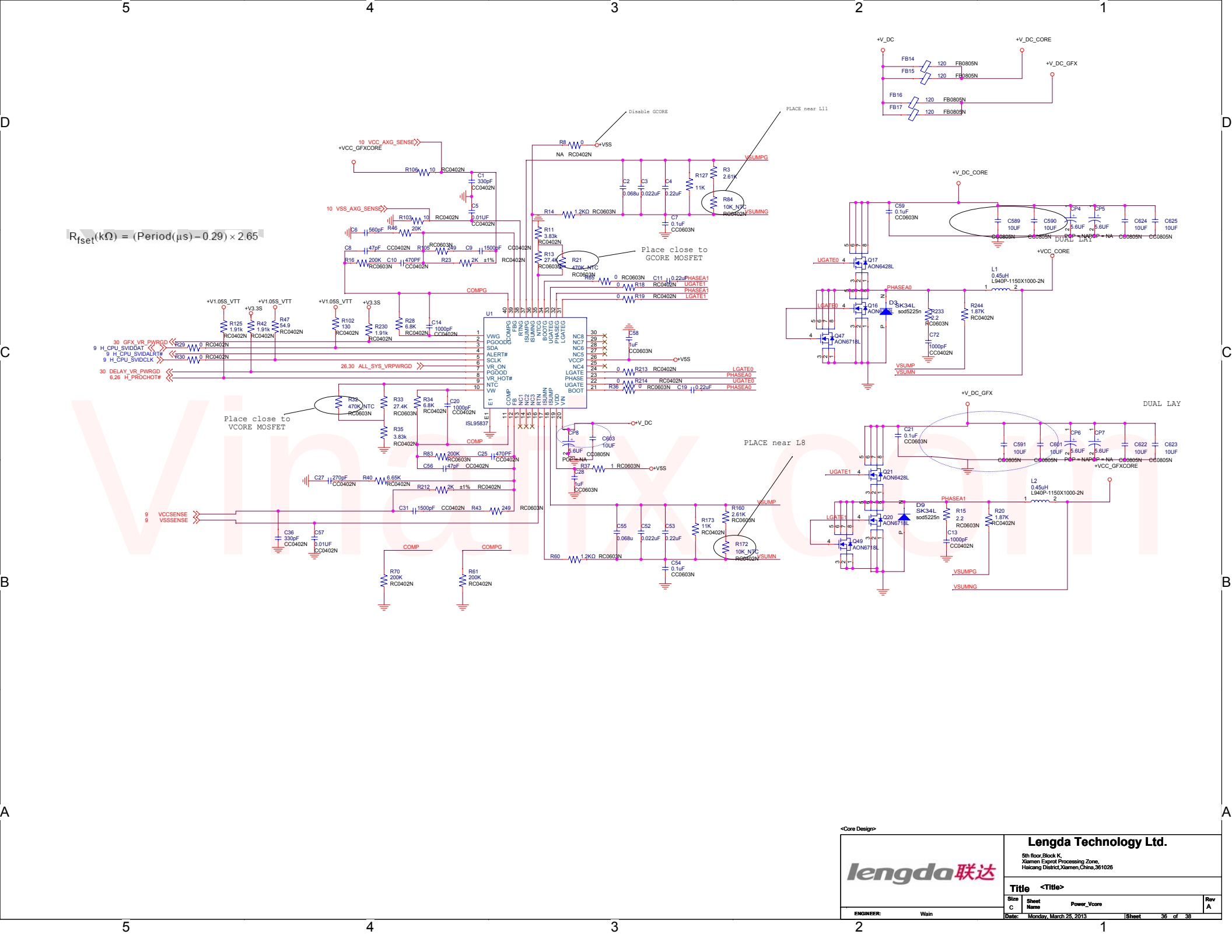
$R_{fset}(k\Omega) = (Period(\mu s) - 0.29) \times 2.65$
Disable GCORE
PLACE near L11
Place close to GCORE MOSFET
Place close to VCORE MOSFET
PLACE near L8
DUAL LAY
U1
ISL95837
+V_DC
+V_DC_CORE
+V_DC_GFX
+VCC_CORE
+VCC_GFXCORE
+V3.3S
+V1.05S_VTT
+V5S
VSUMP
VSUMN
VSUMPG
VSUMNG
COMP
COMPG
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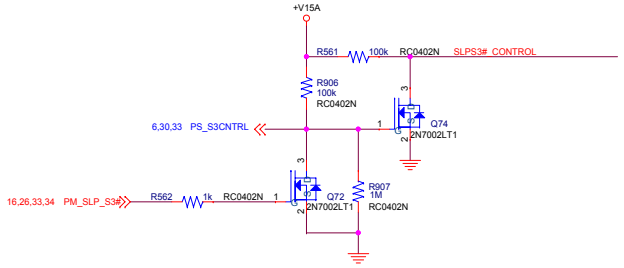
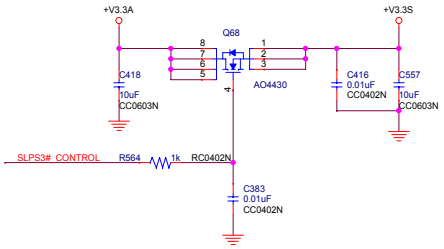
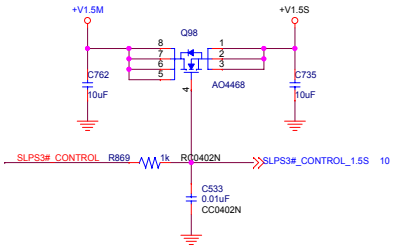
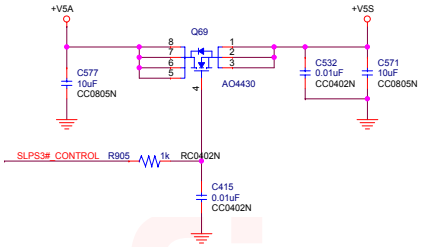
S3 /S4 Power control



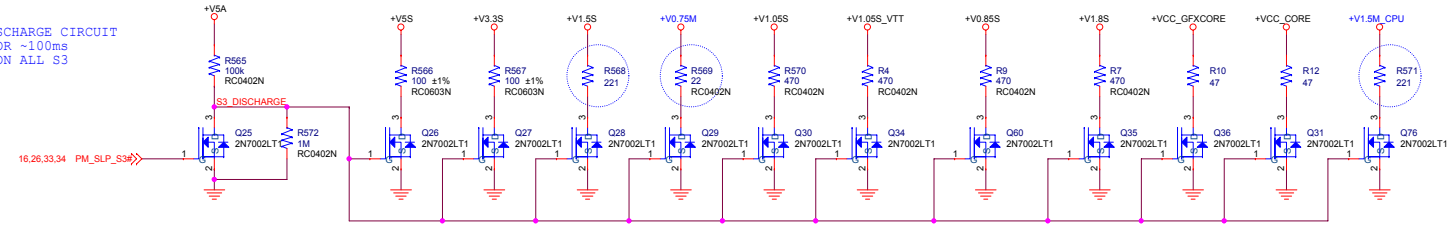




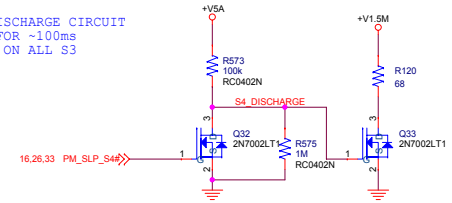


Power Discharge Circuit

SLP_S3# DISCHARGE CIRCUIT
DESIGNED FOR ~100ms
DISCHARGE ON ALL S3
RAILS.



SLP_S4# DISCHARGE CIRCUIT
DESIGNED FOR ~100ms
DISCHARGE ON ALL S3
RAILS.



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Changelist V1.01

1、VCORE 和GFX电源增加磁珠
2、封装1206 10uf电容增加duallay 1210封装极性电容
3、DD2结构干涉，挪到主板端
4、R17，R25，R67，R58丝印错误----------layout更改
5、MH7丝印改在BOT，TH区域标注有2个--------layout更改
6、增加touch pannel 电源控制TP_EN
7、LCD driver IC增加5V预留

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D	Change List	A

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