FUSION

(MS-7857M1 Ver:10)

mATX: 9.6 inch * 8.86 inch

CPU:

AMD FM2(Richland uPGA FAMILIES)

System Chipset:

AMD - Bolton D3

On Board Chipset:

CLOCK GEN --FCH internal clock gen
LPC Super I/O --F71808A
LAN-Realtek 8111E

Azalia CODEC - Realtek ALC887/662

Main Memory:

DDR III * 2 (16 GB)

Expansion Slots:

PCI Express X16 Slot * 1
PCI Express X1 Slot * 2

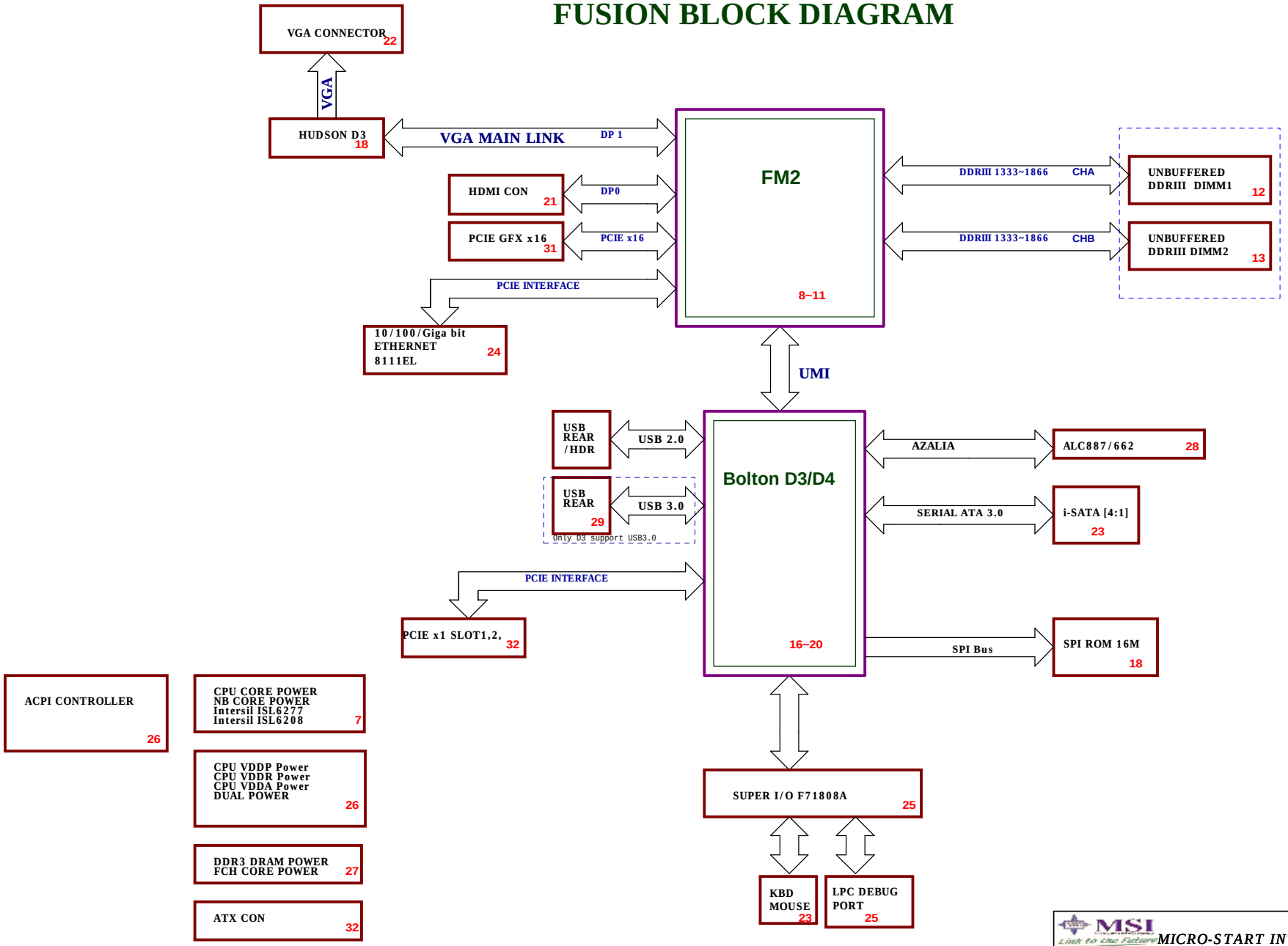
VRM

Controller - Intersil 6277 3+2 Phase

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: MS-7857		
Size: Custom	Document Number: Cover Sheet	Rev: 10
Date: Monday, December 17, 2012	Sheet 1 of 37	

FUSION BLOCK DIAGRAM



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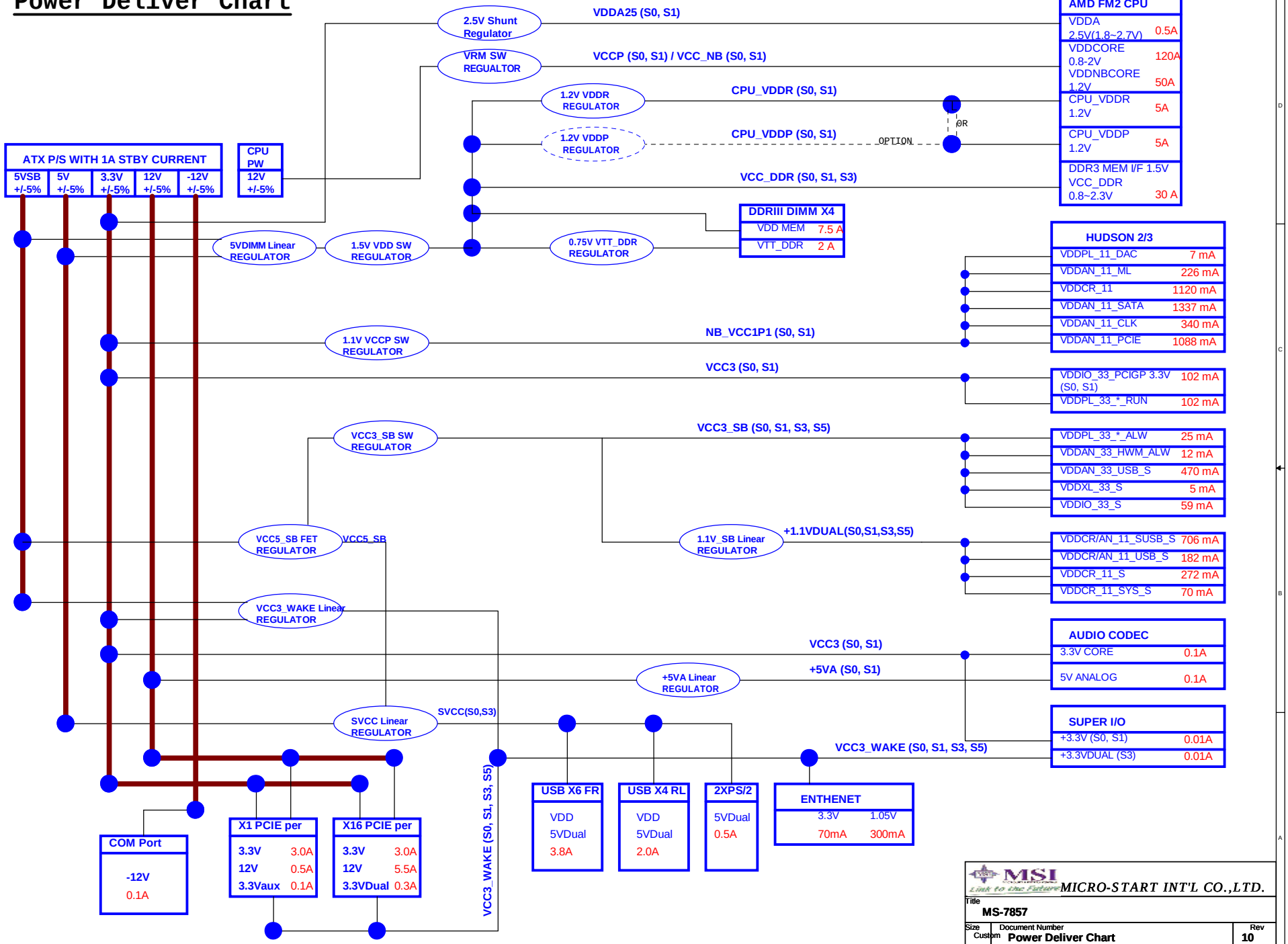
Title: MS-7857		
Size: Custom	Document Number: Block Diagram	Rev: 10
Date: Monday, December 17, 2012	Sheet 2 of 37	

Power Deliver Chart



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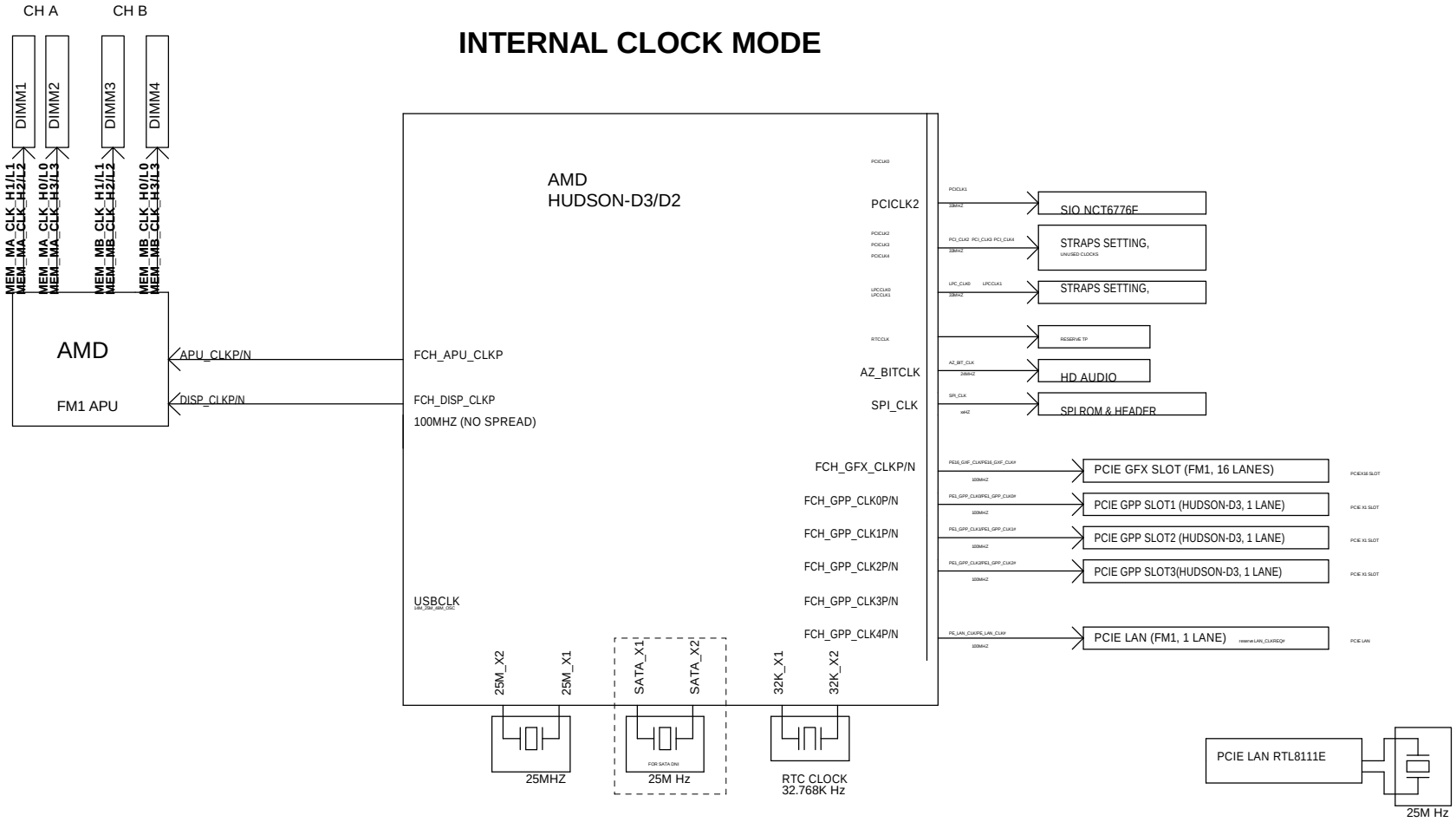
Title: MS-7857

Size: Custom | Document Number: Power Deliver Chart | Rev: 10

Date: Monday, December 17, 2012 | Sheet 3 of 37

INTERNAL CLOCK MODE



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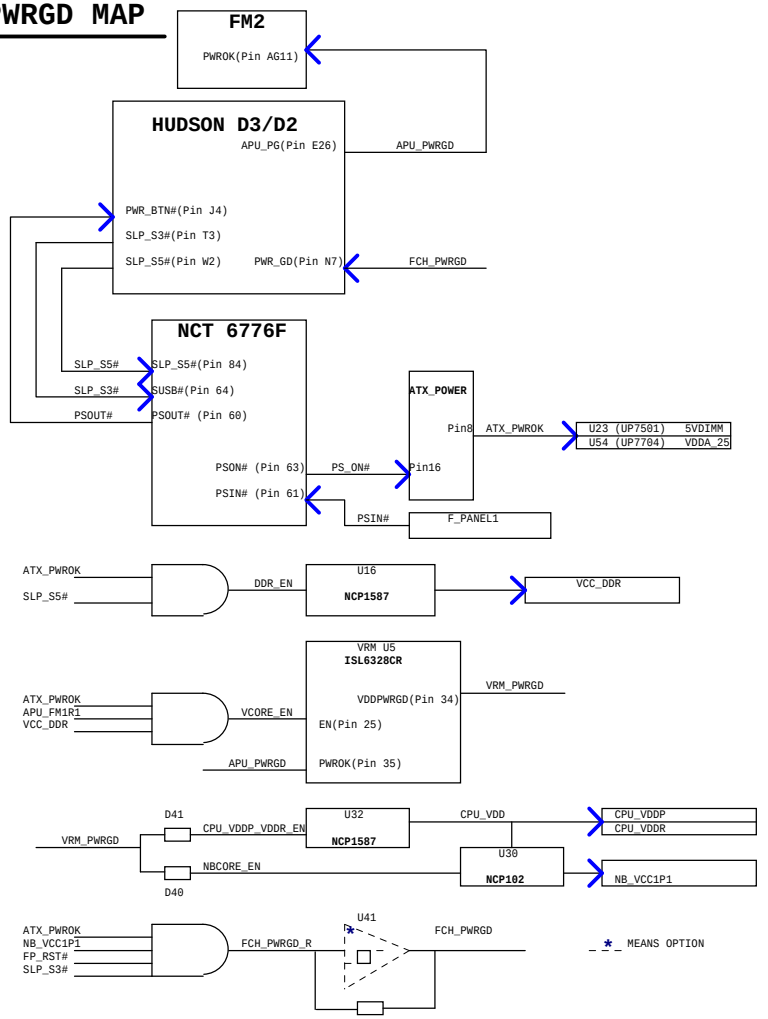
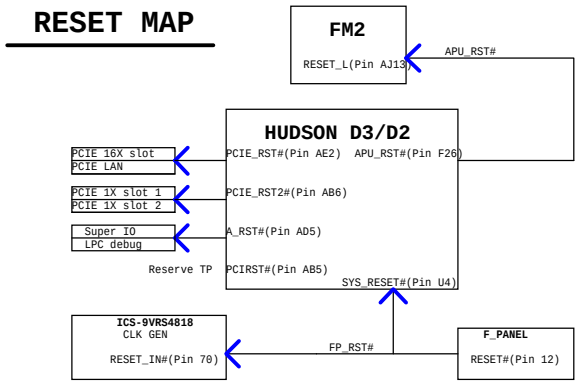
Title: MS-7857		
Size: Custom	Document Number: Clock Distribution	Rev: 10
Date: Monday, December 17, 2012	Sheet 4 of 37	

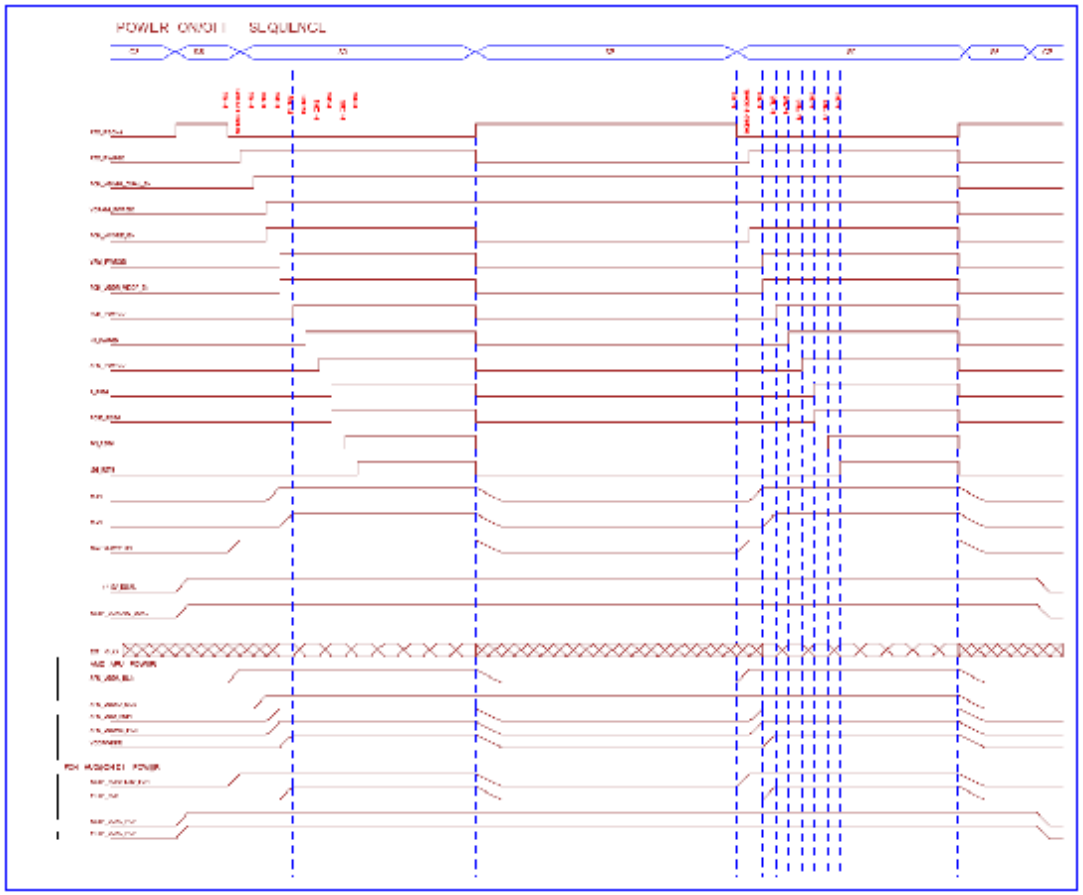
PWRGD MAP



RESET MAP



POWER ON SEQUENCE



MSI MICRO-STAR INT'L CO.,LTD.

Title: MS-7857

Size: Custom | Document Number: PWRGD/RESET MAP | Rev: 10

Date: Monday, December 17, 2012 | Sheet 5 of 37

SIO Fintek 71808A GPIO Config

Pin	GPIO	Power Rail	Function description	Comment
18	GP20	VSB	IO_PME#	
22	LED_VSB/GP24	VSB	SUS_LED	reserved
23	LED_VCC/GP25	VSB	PWR_LED	
42	GP67	VSB	USB_EN	OD
53	GP00	VSB	MB_ID0	GPI reserved
54	GP01	VSB	MB_ID1	GPI reserved
55	GP02	VSB	MB_ID2	GPI reserved
56	GP03	VCC	USB_MODE1	IO/OD
19	GP21	VSB	USB_MODE2	IO/OD
49	GP30	VSB	SIO_VCORE_EN	GPI reserved
50	GP31	VSB	SIO_VLDT_EN	GPI reserved

FCH HUDSON D3/D2GPIO Config

Pin	pin Name	Function description
AJ3	AD0/GPIO0	
J2	IR_LED#/LLB#/GPIO184	
AD22	SATA_ACT#/GPIO67	
M6	TEMPIN3/TALERT#/ GPIO174	FCH_TALERT#:Thermal Alert. The FCH can be programmed to generate an SMI, SCI, or IRQ13 through GPE, or generate an SMI without GPE in response to the signal*s assertion.
V3	SPI_CLK/GPIO162	SPI Clock
V6	SPI_DI/GPIO164	SPI Data In
V5	SPI_DO/GPIO163	SPI Data Output
T6	SPI_CS1#/GPIO165	SPI Chip Select1#
V1	ROM_RST#/SPI_WP#/GPIO161	SPI write protect (active low)
Y6	SPI_HOLD#/GEVENT9#	SPI HOLD#. Assert low to hold the SPI transaction.
T8	USB_OC0#/SPI_TPM_CS#/ TRST#/GEVENT12#	OC#0:USB 3.0 port 3,USB 2.0 port 13
J7	USB_OC1#/TDI/GEVENT13#	OC#1:USB2.0 port 4,5
P5	USB_OC2#/TCK/GEVENT14#	OC#2:USB2.0 port 8,9
P5	USB_OC3#/ AC_PRES/TDO/GEVENT15#	OC#3:USB 3.0 port 0,USB 2.0 port 10
P6	USB_OC4#/IR_RX0/ GEVENT16#	OC#4:USB 3.0 port 1,USB 2.0 port 11
T1	USB_OC5#/IR_TX0/ GEVENT17#	OC#5:USB2.0 port 2,3
R8	USB_OC6#/IR_TX1/ GEVENT6#	OC#6:USB2.0 port 0,1
M7	BLINK/USB_OC7#/ GEVENT18#	OC#7:USB 3.0 port 2,USB 2.0 port12
	GPIO[171::173];GPIO[175::182]; GPIO[193::194]	Configure as one of the following: 10-k次 5% pull-up resistor to +3.3V_S5. 10-k次 5% pull-down resistor.

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1 CH-A	10100000B A0H	MEM_MA_CLK_H1/L1 MEM_MA_CLK_H2/L2
DIMM 2 CH-B	10100001B A2H	MEM_MB_CLK_H1/L1 MEM_MB_CLK_H2/L2

SMBus TABLE

SOURCE	SINGLE NAME	LINKED DEVICE
APU	DP0_AUXP_C /DP0_AUXN_C	HDMI
	DP1_AUXP_C /DP1_AUXN_C	Hudson D2/3 DP to VGA translator
FCH	SCLK0/SDATA0	DIMMs,
	SCLK1/SDATA1	PCIE SLOTs,
	SCLK3/SDATA3	TP

RESET TABLE

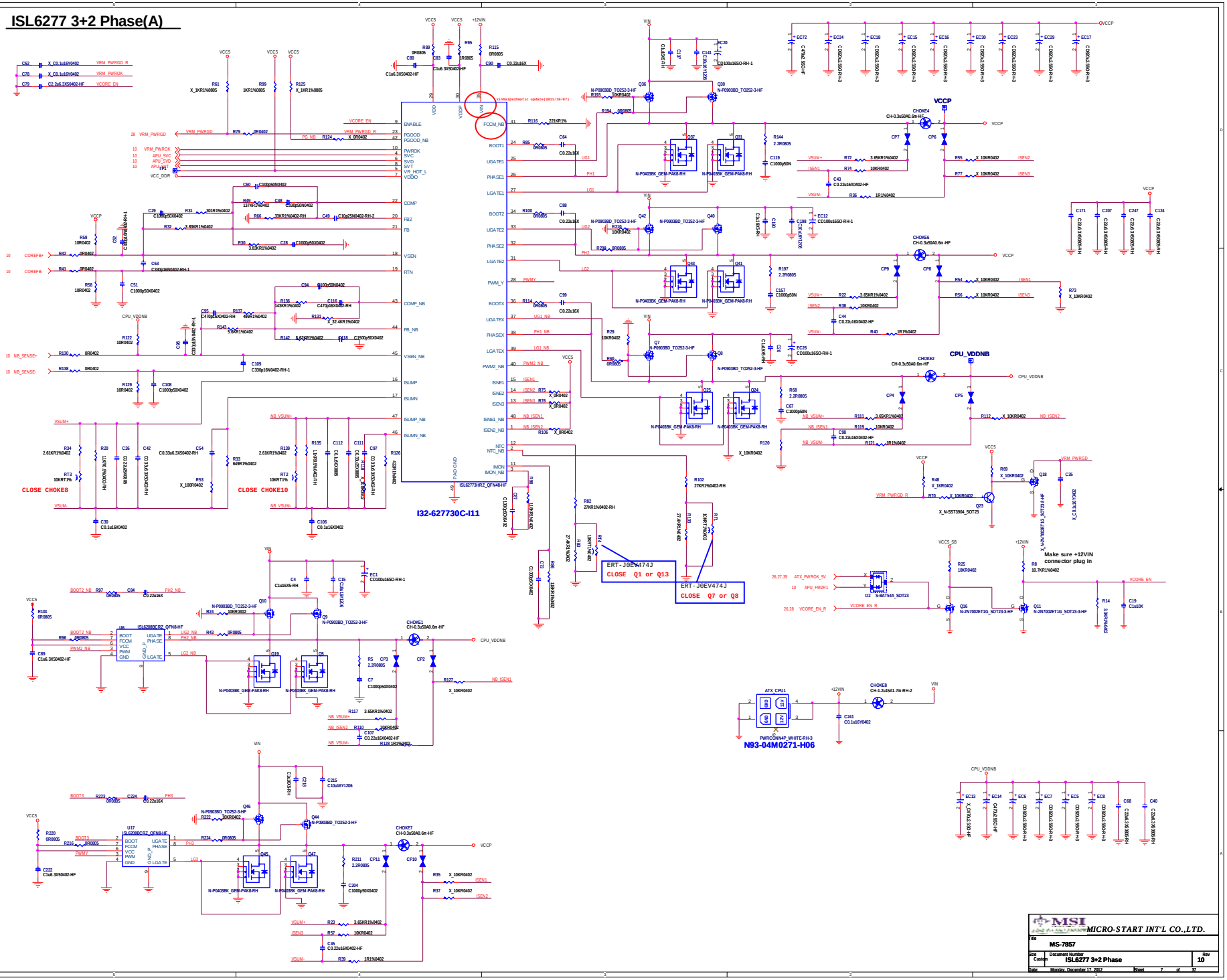
SOURCE	SINGLE NAME	LINKED DEVICE
FCH	PCIE_RST#	PCIe 16X,LAN
	A_RST#	SIO,LPC debug
	PCIE_RST2#	PCIE_1X
	LDT_RST#	APU
	AZ_RST#	AZALIA CODEC
	DDR3_RST#	NC
	FC_RST#	DEBUG BUS
	ROM_RST#	NC
FRONT PANEL	FP_RST#	FCH

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: MS-7857

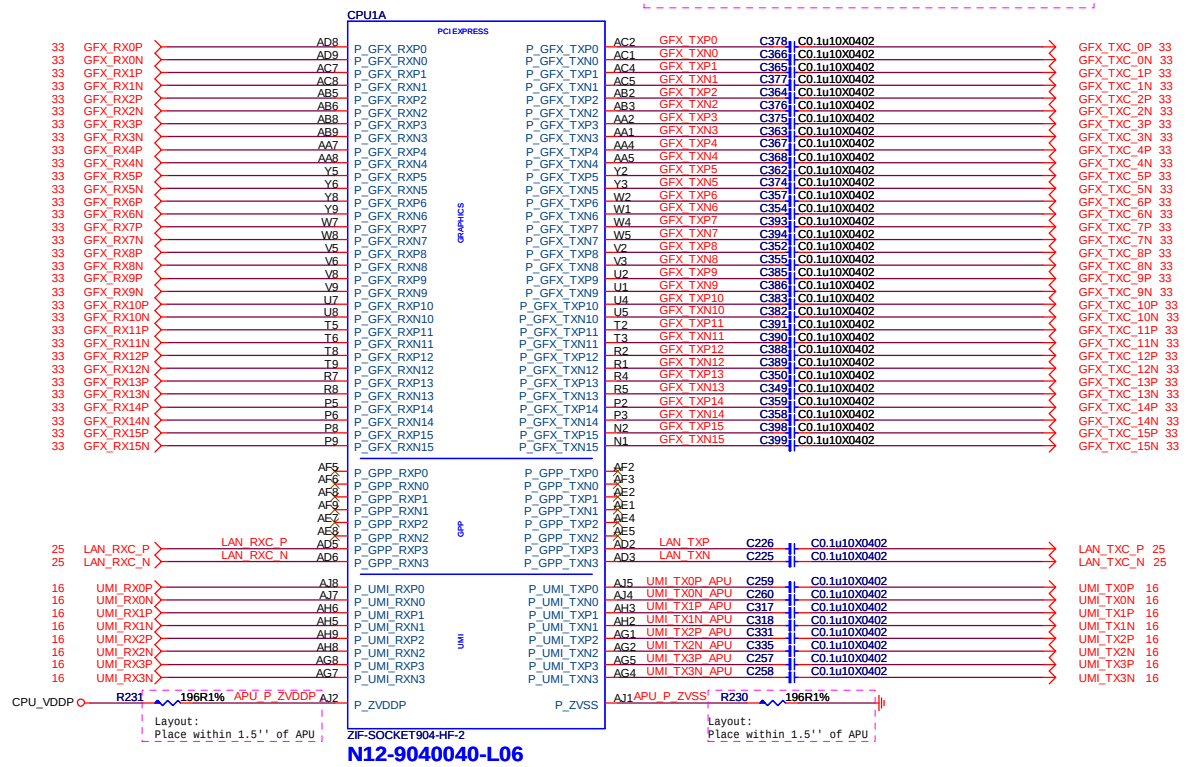
Size: Custom | Document Number: GPIO/MSIC TABLE | Rev: 10

Date: Monday, December 17, 2012 | Sheet 6 of 37



FM2 PCIE I/F

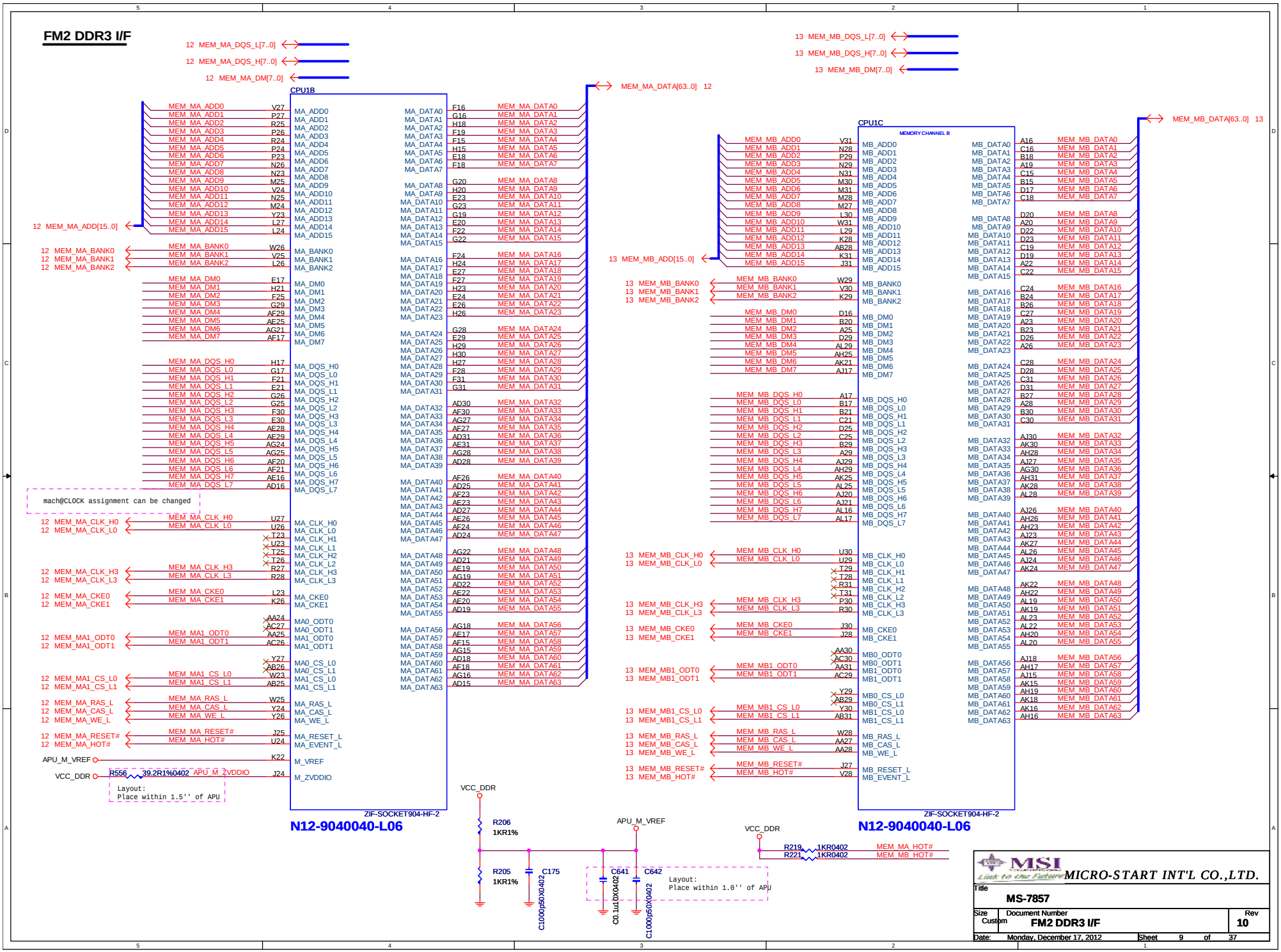
mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



MICRO-START INT'L CO.,LTD.

Title	MS-7857	
Size: Custom	Document Number: FM2 PCIE I/F	Rev: 10
Date: Monday, December 17, 2012	Sheet 8 of 37	

FM2 DDR3 I/F



MICRO-START INT'L CO.,LTD.		
Title: MS-7857		
Size: Custom	Document Number: FM2 DDR3 I/F	Rev: 10
Date: Monday, December 17, 2012	Sheet 9 of 37	

FM2 DISPLAY I/F

ROUTE PCIE AS 85OHM +/-10%

PLACE CAPS WITH APU < 1 INCH
Trace length within 10"

mach@DP0 for HDMI

22	DP0_TX0P	C146 C0.1u10X0402	DP0_TX0P_APU	N4	DP0_TXP0
22	DP0_TX0N	C142 C0.1u10X0402	DP0_TX0N_APU	N5	DP0_TXN0
22	DP0_TX1P	C148 C0.1u10X0402	DP0_TX1P_APU	M2	DP0_TXP1
22	DP0_TX1N	C153 C0.1u10X0402	DP0_TX1N_APU	M3	DP0_TXN1
22	DP0_TX2P	C140 C0.1u10X0402	DP0_TX2P_APU	L2	DP0_TXP2
22	DP0_TX2N	C138 C0.1u10X0402	DP0_TX2N_APU	L1	DP0_TXN2
22	DP0_TX3P	C155 C0.1u10X0402	DP0_TX3P_APU	L4	DP0_TXP3
22	DP0_TX3N	C158 C0.1u10X0402	DP0_TX3N_APU	L5	DP0_TXN3

mach@DP1_for_CRT

18	DP1_TX0P	C193 C0.1u10X0402	DP1_TX0P_APU	K2	DP1_TXP0
18	DP1_TX0N	C197 C0.1u10X0402	DP1_TX0N_APU	K3	DP1_TXN0
18	DP1_TX1P	C195 C0.1u10X0402	DP1_TX1P_APU	J2	DP1_TXP1
18	DP1_TX1N	C194 C0.1u10X0402	DP1_TX1N_APU	J1	DP1_TXN1
18	DP1_TX2P	C203 C0.1u10X0402	DP1_TX2P_APU	J4	DP1_TXP2
18	DP1_TX2N	C206 C0.1u10X0402	DP1_TX2N_APU	J5	DP1_TXN2
18	DP1_TX3P	C174 C0.1u10X0402	DP1_TX3P_APU	H2	DP1_TXP3
18	DP1_TX3N	C178 C0.1u10X0402	DP1_TX3N_APU	H3	DP1_TXN3

CPU1D

ANALOG/DISPLAY/MISC

DP2_TXP0	L7	DP2_TX0P_APU	
DP2_TXN0	L8	DP2_TX0N_APU	
DP2_TXP1	K5	DP2_TX1P_APU	
DP2_TXN1	K6	DP2_TX1N_APU	
DP2_TXP2	K8	DP2_TX2P_APU	
DP2_TXN2	K9	DP2_TX2N_APU	
DP2_TXP3	J7	DP2_TX3P_APU	
DP2_TXN3	J8	DP2_TX3N_APU	
DP2_TXP4	N7	DP2_TX4P_APU	
DP2_TXN4	N8	DP2_TX4N_APU	
DP2_TXP5	M5	DP2_TX5P_APU	
DP2_TXN5	M6	DP2_TX5N_APU	
DP2_TXP6	M8	DP2_TX6P_APU	
DP2_TXN6	M9	DP2_TX6N_APU	

DISPLAY PORT 0 / DISPLAY PORT MISC. / DISPLAY PORT 1 / DISPLAY PORT 2

DP_AUX_ZVSS	G9	DP_AUX_ZVSS	R555 150R1%0402
DP_BLON	F8	APU_BLON	
DP_DIGON	G8	APU_DIGON	
DP_VARY_BL	E8	APU_BLPWM	
DP0_AUXP	E1	DP0_AUXP_C	22
DP0_AUXN	E2	DP0_AUXN_C	22
DP1_AUXP	F1	DP1_AUXP_C	18
DP1_AUXN	F2	DP1_AUXN_C	18
DP2_AUXP	G1		
DP2_AUXN	G2		
DP3_AUXP	E5		
DP3_AUXN	E6		
DP4_AUXP	F5		
DP4_AUXN	F6		
DP5_AUXP	G5		
DP5_AUXN	G6		
DP0_HPD	E3	DP0_HPD_HDMI_C	22
DP1_HPD	F3	DP1_HPD_VGA_C	18
DP2_HPD	G3	DP2_HPD R204 100KR0402	
DP3_HPD	E7	DP3_HPD R187 100KR0402	
DP4_HPD	F7	DP4_HPD R188 100KR0402	
DP5_HPD	G7	DP5_HPD R180 100KR0402	

TEST4	T21	APU_TEST4	TP37
TEST5	U21	APU_TEST5	TP38
TEST6	AD14	APU_TEST6	TP41
TEST9	P21	APU_TEST9	TP34
TEST10	R21	APU_TEST10	TP36
TEST14	F12	APU_TEST14	TP28
TEST15	E12	APU_TEST15	TP27
TEST16	F13	APU_TEST16	TP33
TEST17	E13	APU_TEST17	TP25
TEST18	G13	APU_TEST18	R156 1KR0402
TEST19	G14	APU_TEST19	R148 1KR0402
TEST20	F14	APU_TEST20	R149 1KR0402
TEST24	E14	APU_TEST24	R153 1KR0402
TEST25_H	AJ11	APU_TEST25_H	R236 511R1%0402
TEST25_L	AH11	APU_TEST25_L	R557 511R1%0402
TEST28_H	H10	APU_TEST28_H	TP32
TEST28_L	J10	APU_TEST28_L	TP31
TEST30_H	T22	APU_TEST30_H	TP40
TEST30_L	U22	APU_TEST30_L	TP42
TEST31	AG31	APU_TEST31	R218 39.2R1%0402
TEST32_H	V22	APU_TEST32_H	TP39
TEST32_L	R22	APU_TEST32L	TP35
TEST35	AE14	APU_TEST35	R229 X_300R0402
			R234 300R0402

TEST

CLKIN_H	AL12	16 APU_CLK	
CLKIN_L	AK12	16 APU_CLK#	
DISP_CLKIN_H	AG12	16 DISP_CLK	
DISP_CLKIN_L	AF12	16 DISP_CLK#	

CLK

SVC	C1	APU_SVC_R	
SVD	C2	APU_SVD_R	
SVT	D1	APU_SVT_R	
SIC	AK14	26 APU_SIC	C292 X_C10p50N0402 R238 10R0402 APU_SIC_R
SID	AL14	26 APU_SID	C291 C180p50N0402
RESET_L	AF10	16 APU_RST#	
PWROK	AF14	16 APU_PWRGD	C301 C180p50N0402
PROCHOT_L	AE10	APU_PROCHOT#	
THERMTRIP_L	AH14	APU_THERMTRIP#	
ALERT_L	AJ14	APU_ALERT#	

SER. / MISC / CTRL

TDI	G11	CPU_TDI	
TDO	E10	CPU_TDO	
TCK	E11	CPU_TCK	
TMS	F11	CPU_TMS	
TRST_L	F10	CPU_TRST_L	
DBRDY	G10	CPU_DBRDY	
DBREQ_L	E9	CPU_DBREQ_L	

JTAG

RSVD1	AJ13		
RSVD2	AH13		
RSVD3	AD13		
RSVD4	K23		
RSVD5	K25		
RSVD6	AB23		
RSVD7	AC24		
RSVD8	AG10		

RSVD

VDDP_SENSE	C3	VDDP_SENSE	28
VDDNB_SENSE	A3	NB_SENSE+	7
VDDIO_SENSE	A4	VDDIOFB+	28
VDD_SENSE	B3	COREFB+	7
VDDR_SENSE	C4	VDDR_SENSE	28
VSS_SENSE	B4	COREFB-	7

SENSE

R179 0R0402

R186 0R0402

NB_SENSE- 7

ZIF-SOCKET904-HF-2

N12-9040040-L06

DP0	DP0_TX0,TX1,TX2 and TX3 DP0_AUX0 and DP0_HPD
DP1	DP1_TX0,TX1,TX2 and TX3 DP1_AUX0 and DP1_HPD

PULL UP

VCC_DDR

R235 1KR0402	APU_SIC_R	
R237 1KR0402	APU_SID	
R244 300R0402	APU_RST#	
R239 300R0402	APU_PWRGD	
R263 300R0402	APU_PROCHOT#	
R298 1KR0402	APU_THERMTRIP#	
R295 1KR0402	APU_ALERT#	

HDT+ Connector

VCC_DDR

J1

1	CPU_VDDIO	CPU_TCK	2 CPU_TCK
3	GND	CPU_TMS	4 CPU_TMS
5	GND	CPU_TDI	6 CPU_TDI
7	GND	CPU_TDO	8 CPU_TDO
9	CPU_TRST_L	CPU_PWROK_BUF	10 APU_PWROK_BUF
11	CPU_DBRDY3	CPU_RST_L_BUF	12 APU_LDT_RST_BUF
13	CPU_DBRDY2	CPU_DBRDY0	14 CPU_DBRDY
15	CPU_DBRDY1	CPU_DBREQ_L	16 CPU_DBREQ_L
17	GND	CPU_PLLTEST0	18 APU_TEST19
19	CPU_VDDIO	CPU_PLLTEST1	20 APU_TEST18

X_H2X10SM-1.27PITCH_BLUE-RH

N31-2100170-S88

CPU_TRST_L R551 X_0R0402
R552 X_10KR0402
R553 X_10KR0402
R554 X_10KR0402

VCC3

R3 X_10KR0402

Q2 X_N-SST3904_SOT23

APU_PWRGD — APU_PWROK_BUF

VCC3

R2 X_10KR0402

Q1 X_N-SST3904_SOT23

APU_RST# R1 X_0R0402 — APU_LDT_RST_BUF

VID OVERRIDE CIRCUIT

VCC_DDR

R175 1KR0402
R177 1KR0402
R160 1KR0402

R166 X_1KR0402
R163 X_1KR0402
R152 X_1KR0402

APU_SVC_R	R162	0R0402	APU_SVC 7
APU_SVD_R	R167	0R0402	APU_SVD 7
APU_SVT_R	R155	33R0402	APU_SVT 7
APU_PWRGD	R87	X_R/2	VRM_PWROK 7

R159 X_1KR0402
R154 X_1KR0402
R151 X_1KR0402
R91 X_220R0402

To overide VID:remove
R520,R521
Stuff R82 to enter FIX mode

BOOT_Voltage			
SVC	SVD	Pre-PWROK metel VID	V_FIX MODE
0	0	1.1	1.4
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

CPU_VDDP

VCC_DDR

Sabine HDMI Design Guidance
HDMI enable strapping:
TEST35 PU TO VCC_DDR thru 300R

3VDUAL

APU_FM2R1 R47 10KR0402

VCC_DDR

FCH_DMA_ACTIVE# R228 1KR0402

LDTSTOP_L R233 1KR0402

SCAN Conn,

APU_TEST18	TP20
APU_TEST19	TP19
APU_TEST24	TP24
APU_TEST20	TP23

WARM RESET

APU_RST# — TP43

GPU DEBUG

APU_BLON	TP29
APU_DIGON	TP30
APU_BLPWM	TP26
DP1_HPD_VGA_C	TP21
VDDIOFB+	TP2
COREFB+	TP22

VCC_DDR

R161 1KR0402
R51 10KR0402

Q21 N-SST3904_SOT23

FM_IDLEEXIT_L — FCH_IDLEEXIT_L 17

VCC_DDR Layout: Place close to HDT header

R181	1KR0402	CPU_TDI
R168	1KR0402	CPU_TCK
R176	1KR0402	CPU_TMS
R164	1KR0402	CPU_TRST_L
R189	300R0402	CPU_DBREQ_L

VCC_DDR 3VDUAL

R300 10KR0402
R430 10KR0402

Q52 N-SST3904_SOT23

APU_THERMTRIP# — FCH_THERMTRIP# 17

VCC_DDR 3VDUAL

R296 10KR0402
R416 10KR0402

Q53 N-SST3904_SOT23

APU_ALERT# — FCH_TALERT# 18

VCC_DDR 3VDUAL

R262 X_10KR0402
R267 X_10KR0402

Q48 X_N-SST3904_SOT23

APU_PROCHOT# — FCH_PROCHOT# 16

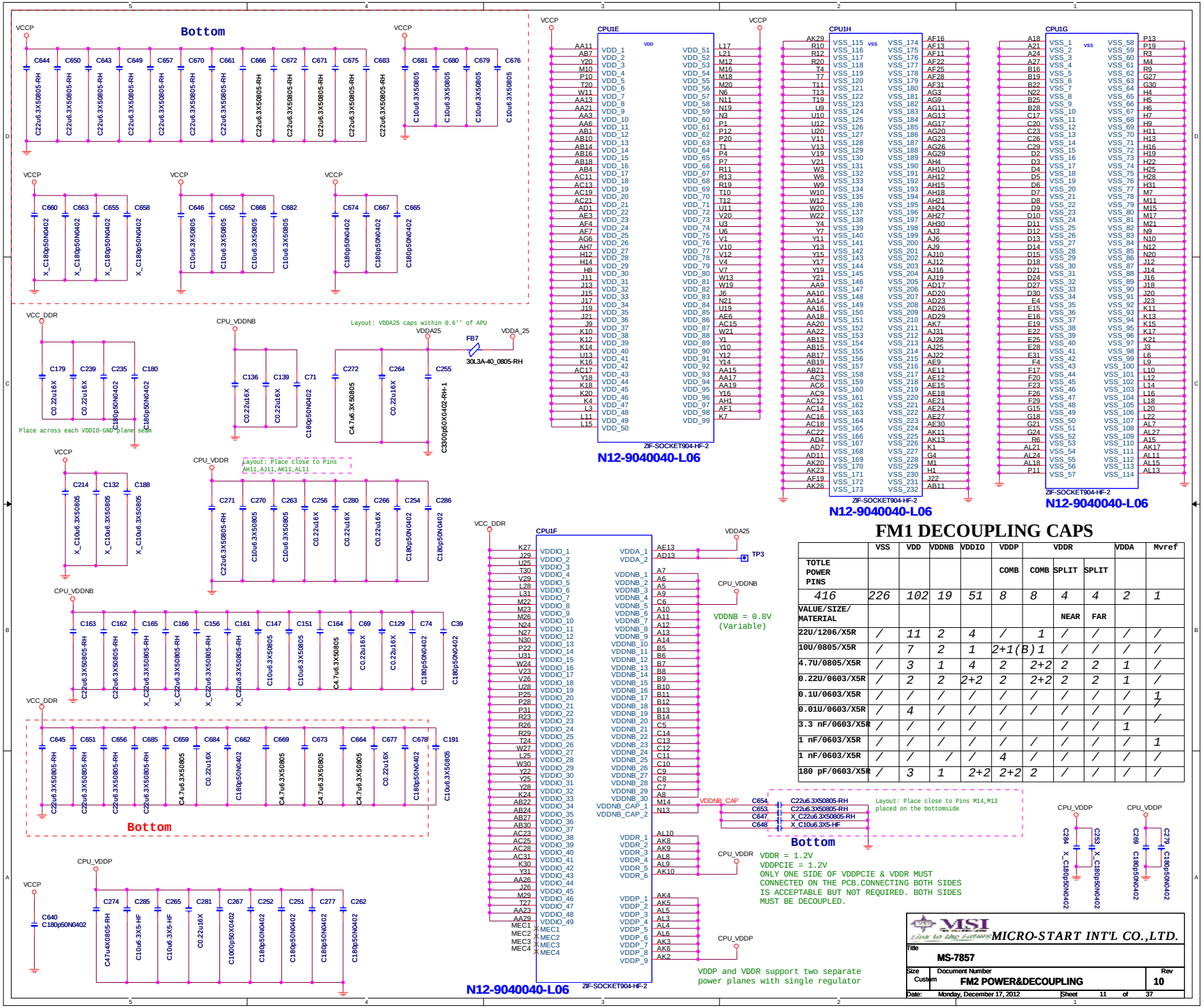
R265 0R0402

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: MS-7857

Size: Custom | Document Number: FM2 DISPLAY/MSIC | Rev: 10

Date: Monday, December 17, 2012 | Sheet 10 of 37

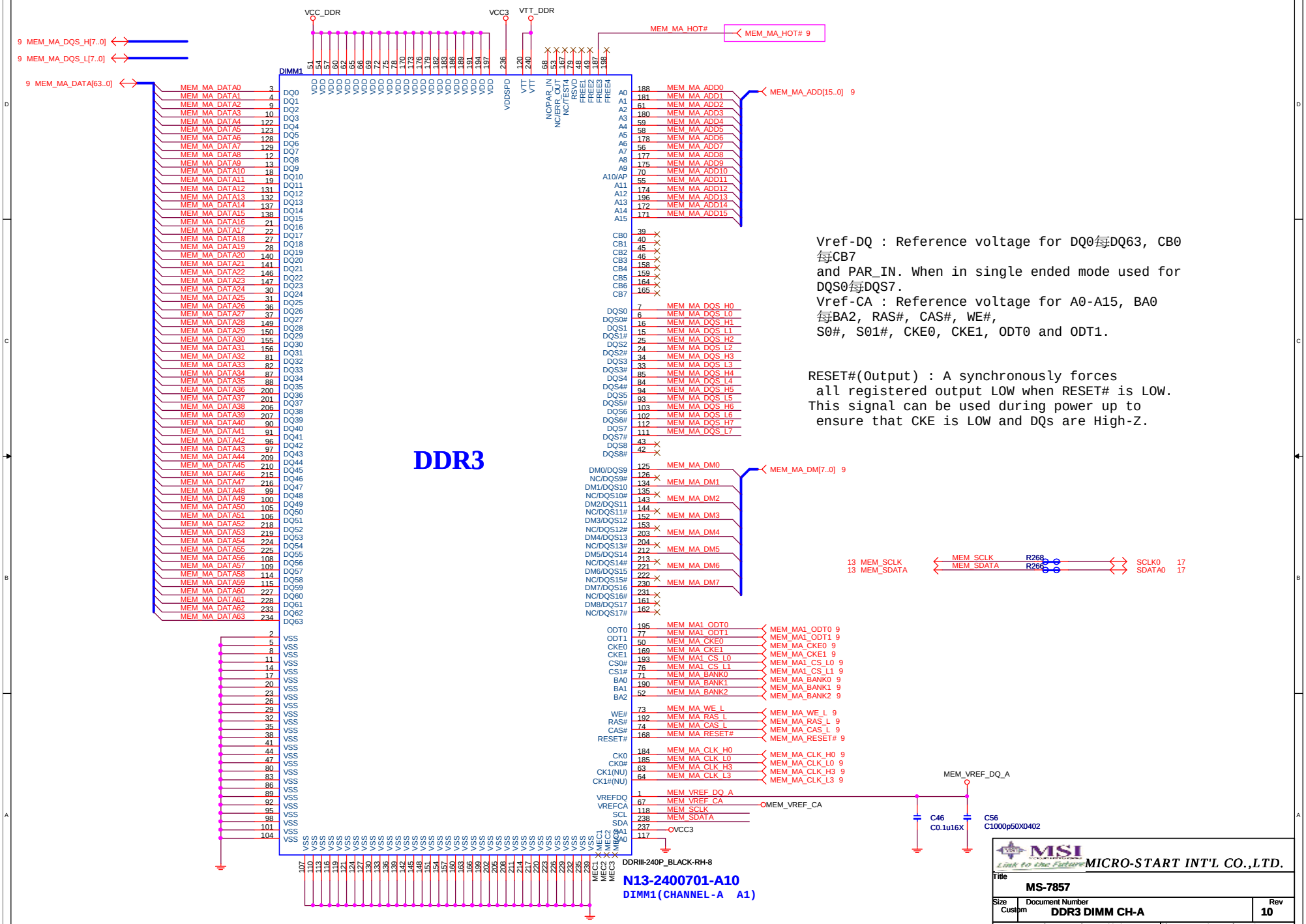


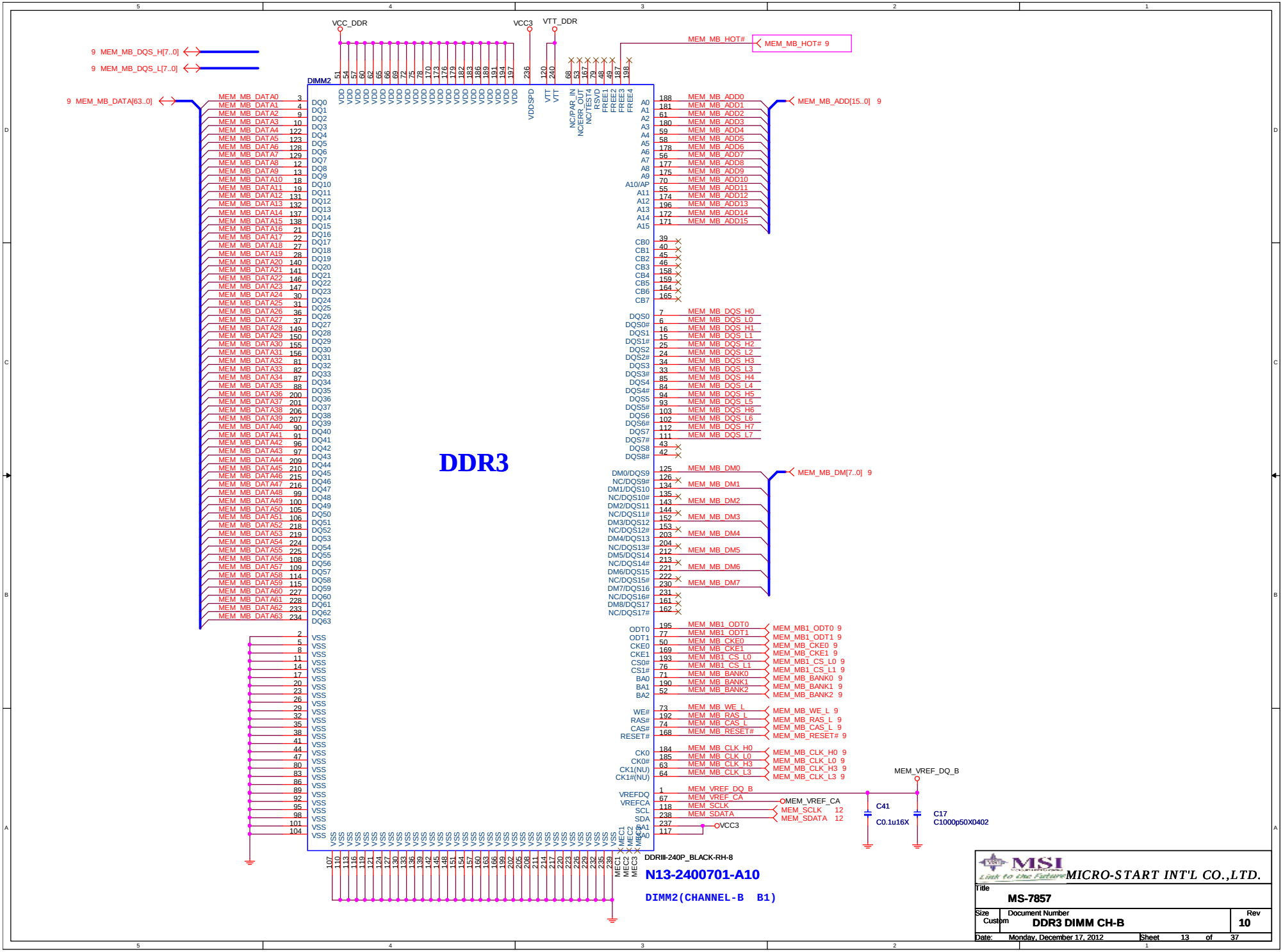
FM1 DECOUPLING CAPS

	VSS	VDD	VDDNB	VDDIO	VDDP	VDDR			VDDA	Mvref
TOTLE POWER PINS					COMB	COMB	SPLIT	SPLIT		
416	226	102	19	51	8	8	4	4	2	1
VALUE/SIZE/ MATERIAL							NEAR	FAR		
22U/1206/X5R	/	11	2	4	/	1	/	/	/	/
10U/0805/X5R	/	7	2	1	2+1(B)	1	/	/	/	/
4.7U/0805/X5R	/	3	1	4	2	2+2	2	2	1	/
0.22U/0603/X5R	/	2	2	2+2	2	2+2	2	2	1	/
0.1U/0603/X5R	/	/	/	/	/	/	/	/	/	1
0.01U/0603/X5R	/	4	/	/	/	/	/	/	/	/
3.3 nF/0603/X5R	/	/	/	/	/		/	/	1	/
1 nF/0603/X5R	/	/	/	/	/	/	/	/	/	1
1 nF/0603/X5R	/	/	/	/	4	/	/	/	/	/
180 pF/0603/X5R	/	3	1	2+2	2+2	2	/	/	/	/

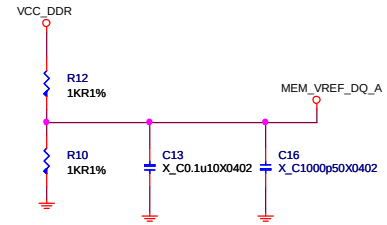
MICRO-START INT'L CO.,LTD.

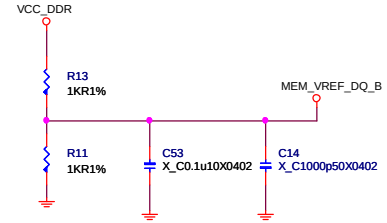
Title	MS-7857		
Size: Custom	Document Number: FM2 POWER&DECOUPLING		Rev: 10
Date: Monday, December 17, 2012	Sheet 11 of 37		

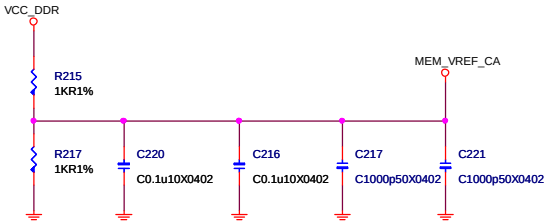




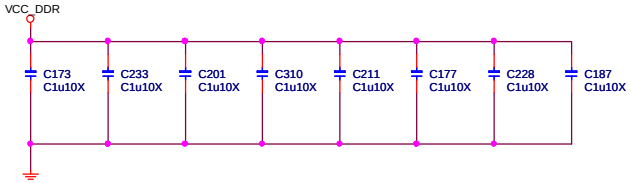
DDR REF POWER & CAPS

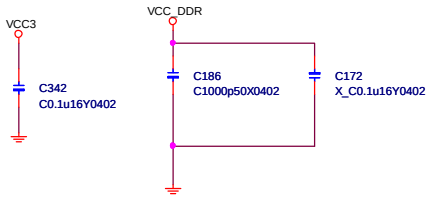


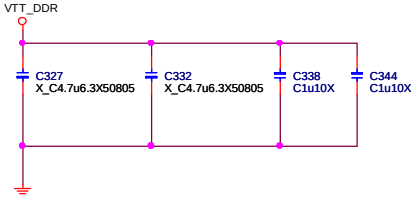




De-coupling Caps For DIMMs



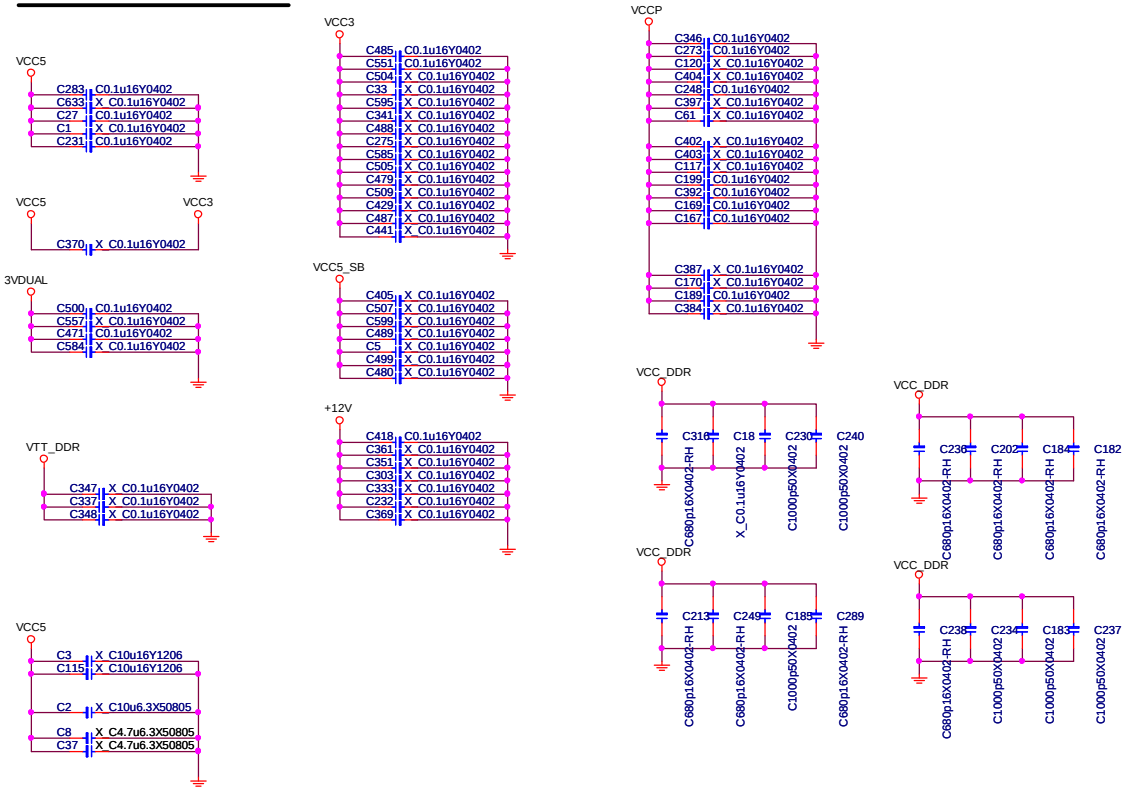




MICRO-START INT'L CO.,LTD.

Title: MS-7857		
Size: Custom	Document Number: DDR REF POWER AND CAPS	Rev: 10
Date: Monday, December 17, 2012	Sheet 14 of 37	

EMI Reserved



MSI Limit to Our Failure MICRO-START INT'L CO.,LTD.

Title: MS-7857		
Size: Custom	Document Number: EMI Reserved	Rev: 10
Date: Monday, December 17, 2012	Sheet 15 of 37	

HUDSON PCIE/PCI/APU/LPC/CLK

If PCI not implemented: Provide test points
or other means to allowaccess for debug purposes.
use these balls for alternate GPIO/GPO functions
or leave unconnected.

CLEAR CMOS

CMOS CLEAR JUMPER
CLR_COMS Clear CMOS

1 - 2	Normal
2 - 3	Clear CMOS

N41-1030191-H06

OB1-7857001

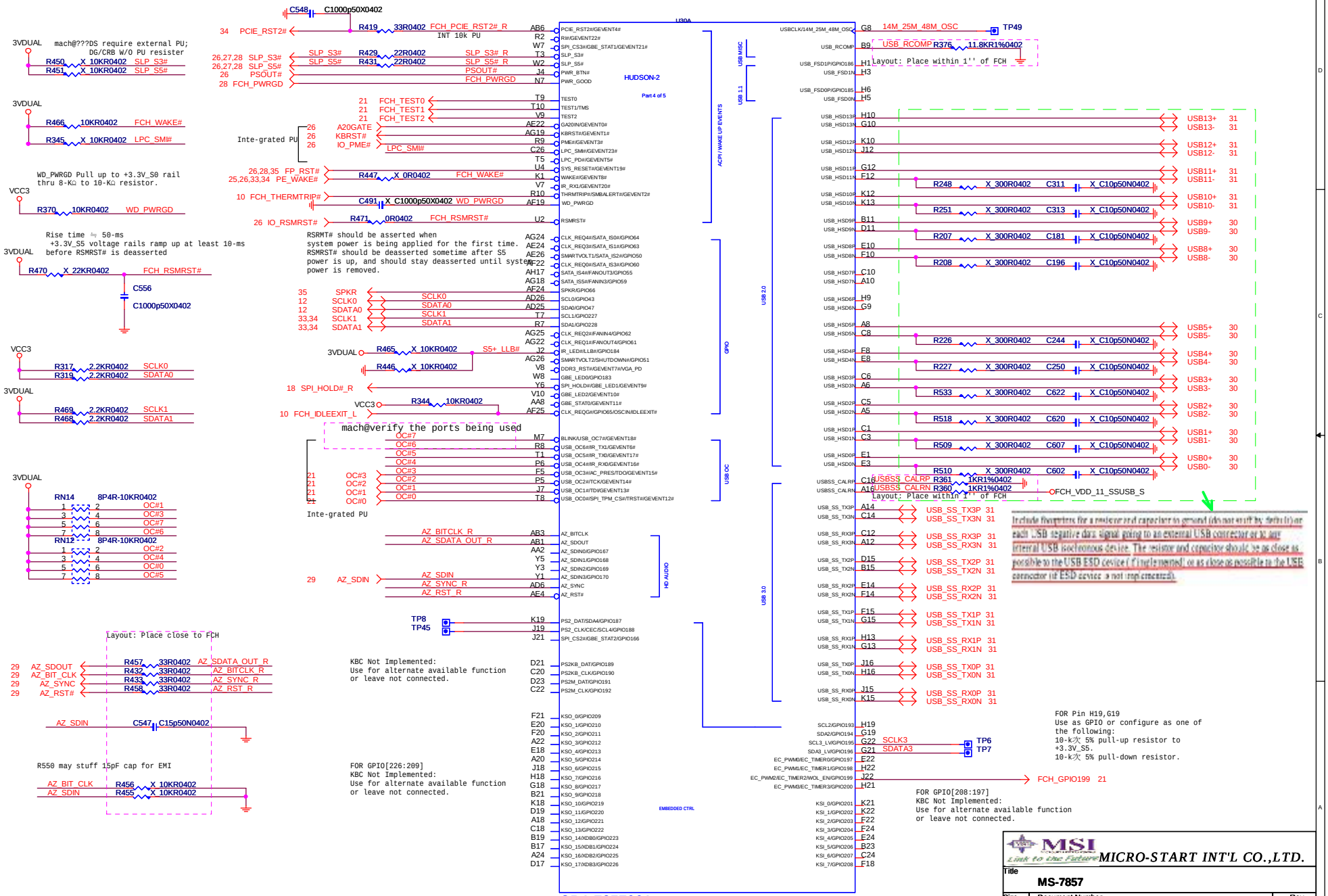
Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the APU I/O rail.
They are also in the S5 domain to prevent glitching at
power up.

PLACE THESE COMPONENTS CLOSE TO
U600, AND USE GROUND GUARD FOR
32K_X1 AND 32K_X2

MICRO-START INT'L CO.,LTD.

Title	MS-7857	
Size: Custom	Document Number: HUDSON PCIE/PCI/APU/LPC/CLK	Rev: 10
Date: Monday, December 17, 2012	Sheet 16 of 37	

HUDSON ACPI/USB/AZ/GPIO



MICRO-START INT'L CO.,LTD.

Title	MS-7857		
Size: Custom	Document Number: HUDSON ACPI/USB/AZ/GPIO		Rev: 10
Date: Monday, December 17, 2012	Sheet 17 of 37		

HUDSON SATA/VGA/SPI/HWM

LAYOUT:
ROUTE SATA TX DIFF PAIR @ 100 OHM+/-10%
RX DIFF PAIR @ 90 OHM+/-10%

SATA[3::0]Route to iSATA
GEN III 6.0 Gbit/S

U30B
HUDSON-2
Part 2 of 5

SATA_TX0+ AK19 SATA_TX0P
SATA_TX0- AM19 SATA_TX0N
SATA_RX0- AL20 SATA_RX0N
SATA_RX0+ AN20 SATA_RX0P
SATA_TX1+ AN22 SATA_TX1P
SATA_TX1- AL22 SATA_TX1N
SATA_RX1- AH20 SATA_RX1N
SATA_RX1+ AJ20 SATA_RX1P
SATA_TX2+ AJ22 SATA_TX2P
SATA_TX2- AH22 SATA_TX2N
SATA_RX2- AM23 SATA_RX2N
SATA_RX2+ AK23 SATA_RX2P
SATA_TX3+ AH24 SATA_TX3P
SATA_TX3- AJ24 SATA_TX3N
SATA_RX3- AN24 SATA_RX3N
SATA_RX3+ AL24 SATA_RX3P
AL26 SATA_TX4P
AN26 SATA_TX4N
AJ26 SATA_RX4N
AH26 SATA_RX4P
AN29 SATA_TX5P
AL28 SATA_TX5N
AK27 SATA_RX5N
AM27 SATA_RX5P
AL29 NC6
AN31 NC7
AL31 NC8
AL33 NC9
AH33 NC10
AH31 NC11
AJ33 NC12
AJ31 NC13
SERIAL ATA

Layout: Place within 1'' of FCH
R563 1KR1%0402 SATA_CALRP AF28 SATA_CALRP
FCH_VDD11_RUN
R573 931R1%0402 SATA_CALRN AF27 SATA_CALRN
35 SATA_LED# SATA_LED# AD22 SATA_ACT#/GPIO67

TP46 FCH_SATA_X1 AF21 SATA_X1
External Clock Generator Mode:
Connect to 25.000-MHz XTAL or connect SATA_X1/X2 balls to
100MHz differential clock from external clock generator.
Integrated Clock Mode:
Leave unconnected.
TP44 FCH_SATA_X2 AG21 SATA_X2

21 FANOUT0 AH16 FANOUT0/GPIO52
AM15 FANOUT1/GPIO53
AJ16 FANOUT2/GPIO54
PIN K3,K5,K6:
Use as GPIO182 or configure as one of
the following:
10-k次 5% pull-up resistor to
+3.3V_S5.
10-k次 5% pull-down resistor.
AK15 FANIN0/GPIO56
AN16 FANIN1/GPIO57
AL16 FANIN2/GPIO58
K6 TEMPIN0/GPIO171
K5 TEMPIN1/GPIO172
K3 TEMPIN2/GPIO173
10 FCH_TALERT# FCH_TALERT# M6 TEMPIN3/TALERT#/GPIO174
HW MONITOR

SD_CLK/SCLK_2/GPIO73 AL14
SD_CMD/SLOAD_2/GPIO74 AN14
SD_CD#/GPIO75 AJ12
SD_WP/GPIO76 AH12
SD_DATA0/SDATI_2/GPIO77 AK13
SD_DATA1/SDATO_2/GPIO78 AM13
SD_DATA2/GPIO79 AH15
SD_DATA3/GPIO80 AJ14
SD CARD

GBE_COL AC4 GBE_COL
GBE_CRS AD3 GBE_CRS
GBE_MDC AD9
GBE_MDIO W10 GBE_MDIO
GBE_RXCLK AB8
GBE_RXD3 AH7
GBE_RXD2 AF7
GBE_RXD1 AE7
GBE_RXD0 AD7
GBE_RXCTL/RXDV AG8
GBE_RXERR AD1 GBE_RXERR
GBE_TXCLK AB7
GBE_TXD3 AF9
GBE_TXD2 AG6
GBE_TXD1 AE8
GBE_TXD0 AD8
GBE_TXCTL/TXEN AB9
GBE_PHY_PD AC2
GBE_PHY_RST# AA7
GBE_PHY_INTR W9 GBE_PHY_INTR
SPI_CLK
C630 X_C10p50N0402
GBE LAN

SPI_DI/GPIO164 V6 SPI_DATAIN
SPI_DO/GPIO163 V5 SPI_DATAOUT
SPI_CLK/GPIO162 V3 SPI_CLK
SPI_CS1#/GPIO165 T6 SPI_CS#
ROM_RST#/SPI_WP#/GPIO161 V1 SPI_WP#_R
SPI ROM

VGA_RED L30 HUDSON_VGA_R
R327 150R1%0402 HUDSON_VGA_R 23
VGA_GREEN L32 HUDSON_VGA_G
R325 150R1%0402 HUDSON_VGA_G 23
VGA_BLUE M29 HUDSON_VGA_B
R323 150R1%0402 HUDSON_VGA_B 23
VGA_HSYNC/GPO68 M28 HUDSON_VGA_HSYNC 23
VGA_VSYNC/GPO69 N30 HUDSON_VGA_VSYNC 23
VGA_DDC_SDA/GPO70 M33 HUDSON_VGA_SDAT 23
VGA_DDC_SCL/GPO71 N32 HUDSON_VGA_SCLK 23
Layout: R within 1''
VGA_DAC_RSET K31 DAC_RSET R568 715R1%0402
VGA DAC

AUX_VGA_CH_P V28 AUX_VGA_CH_P
AUX_VGA_CH_N V29 AUX_VGA_CH_N
AUXCAL U28 AUXCAL R574 100R1%0402 FCH_VDD11_RUN
ML_VGA_L0P T31 DP1_TX0P 10
ML_VGA_L0N T33 DP1_TX0N 10
ML_VGA_L1P T29 DP1_TX1P 10
ML_VGA_L1N T28 DP1_TX1N 10
ML_VGA_L2P R32 DP1_TX2P 10
ML_VGA_L2N R30 DP1_TX2N 10
ML_VGA_L3P P29 DP1_TX3P 10
ML_VGA_L3N P28 DP1_TX3N 10
ML_VGA_HPD/GPIO229 C29 ML_VGA_HPD
VGA MAIN LINK

VIN0/GPIO175 N2
VIN1/GPIO176 M3
VIN2/SDATI_1/GPIO177 L2
VIN3/SDATO_1/GPIO178 N4
VIN4/SLOAD_1/GPIO179 P1
VIN5/SCLK_1/GPIO180 P3
VIN6/GBE_STAT3/GPIO181 M1
VIN7/GBE_LED3/GPIO182 M5
PIN N2,M3,L2,N4,P1,P3,M1,M5
Use as GPIO182 or configure as one of
the following:
10-k次 5% pull-up resistor to
+3.3V_S5.
10-k次 5% pull-down resistor.
NC1 AG16
NC2 AH10
NC3 A28
NC4 G27
NC5 L4

SPI ROM & DEBUG HEADER

3VDUAL D32 X_B140-13-F_SMA-RH
R511 X_R0805
VCC3_ROM EC69 1+ 2 CD10u16EL5-RH-1
C624 C0.1u16Y0402

VCC3_ROM SPI1
SPI_DATAIN 3 4 SPI_DATAOUT
SPI_CS# 5 6 SPI_CLK
SPI_HOLD# 9
H2X5[10]M-2PITCH_BLACK-RH-2

VCC3_ROM R547 1KR0402 R520 10KR0402
SPI_CS#
SPI_DATAIN R546 0R0402 SPI_DATAIN_R
SPI_WP#_R R582 X 0R0402 SPI_WP#
U41
CS# VCC SPI_HOLD#
SO/SIO1 HOLD# SPI_CLK
WP# SCLK SPI_DATAOUT
GND SI/SIO0
W25Q32BVSSIG-HF
VCC3_ROM R545 10KR0402
MACH@Reserve 0R serial resisters for
SI overshoot/undershoot debug
M31-25Q3203-W03

SPI_HOLD# R577 X 0R0402 SPI_HOLD#_R 17

GBE NOT ENABLED

3VDUAL
R403 10KR0402 GBE_MDIO
GBE_COL
GBE_CRS
GBE_RXERR
GBE_PHY_INTR
RN11 8P4R-10KR0402

VGA HPD

VCC3
For FM1
VCC_DDR
R306 X_10KR0402
ML_VGA_HPD
0.26mA
R309 X_10KR0402
Q54 X_N-SST3904_SOT23
R310 0R0402 DP1_HPD_VGA_C 10
R311 100KR0402

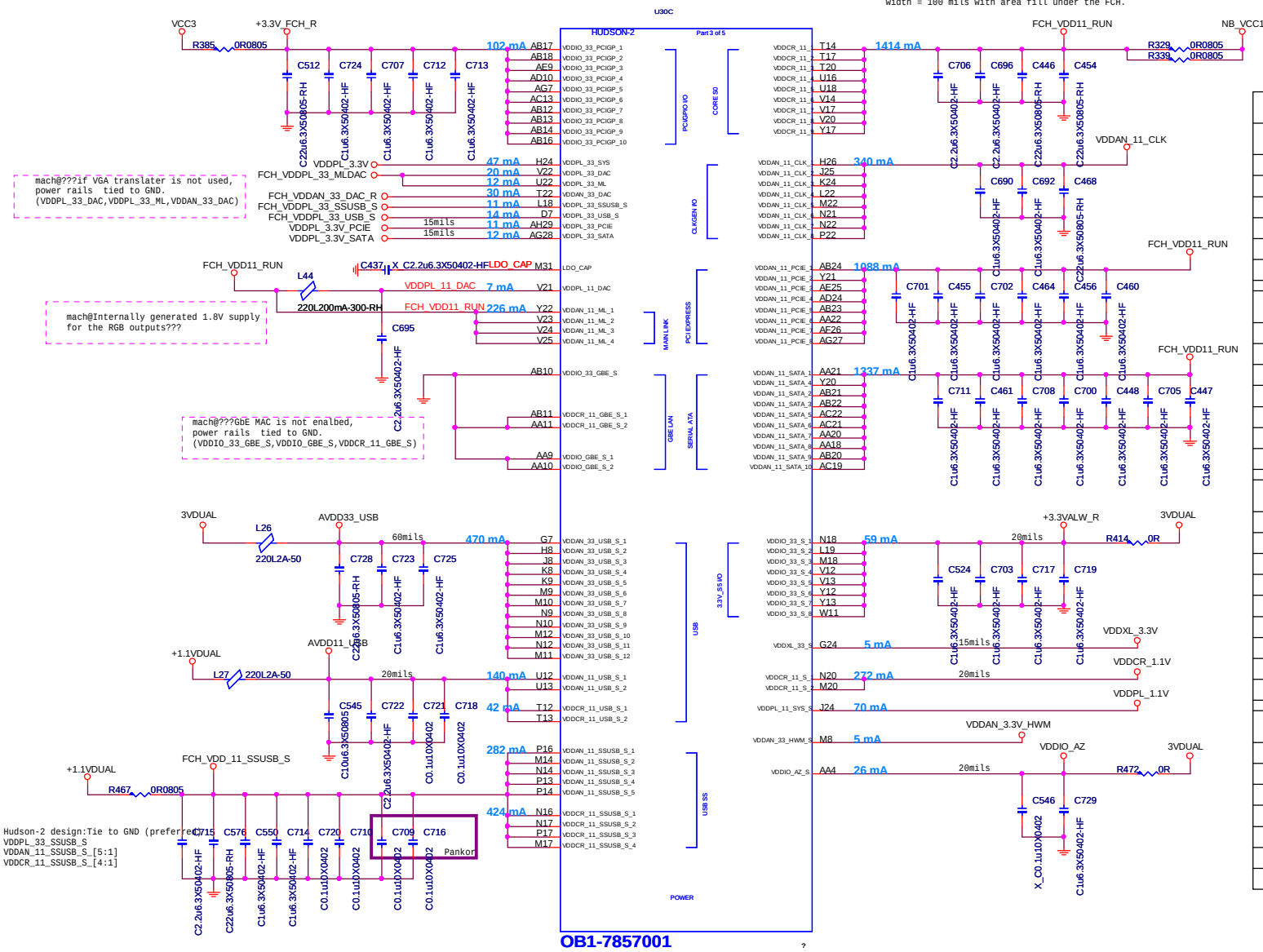
R321 100KR0402
AUX_VGA_CH_P C425 C0.1u10X0402 DP1_AUXP_C 10
AUX_VGA_CH_N C428 C0.1u10X0402 DP1_AUXN_C 10
R324 100KR0402 VCC3
R249 1.8KR0402 R252 1.8KR0402

HUDSON_VGA_R C443 C10p50N0402
HUDSON_VGA_G C440 C10p50N0402
HUDSON_VGA_B C432 C10p50N0402

OB1-7857001

MSI Link to the Future MICRO-START INT'L CO.,LTD.
Title: MS-7857
Size: Custom | Document Number: HUDSON SATA/VGA/HWM/SPI | Rev: 10
Date: Monday, December 17, 2012 | Sheet 18 of 37

HUDSON POWER&DECOUPLING



Power Rails	Hudson D3
NB_VCC1P1	max 4118 mA
VDDCR_11_[9:1]	1120 mA
VDDAN_11_CLK_[8:1]	340 mA
VDDAN_11_PCIE_[8:1]	1088 mA
VDDAN_11_SATA_[10:1]	1337 mA
VDDAN_11_ML_[4:1]	226 mA
VDDPL_11_DAC	7 mA
VCC3	max 234 mA
VDDIO_33_PCIGP_[10:1]	102 mA
VDDPL_33_SYS	47 mA
VDDPL_33_DAC	20 mA
VDDPL_33_ML	12 mA
VDDPL_33_PCIE	11 mA
VDDPL_33_SATA	12 mA
VDDAN_33_DAC	30 mA
VCC3_SB	max 597 mA
VDDIO_33_S_[8:1]	59 mA
VDDIO_AZ_S	26 mA
VDDXL_33_S	5 mA
VDDAN_33_HWM_S	12 mA
VDDIO_GBE_S[2:1]	GND
VDDIO_33_GBE_S	GND
VDDPL_33_USB_S	14 mA
VDDAN_33_USB_S_[12:1]	470 mA
VDDPL_33_SSUSB_S	11 mA
+1.1VDUAL	max 1230 mA
VDDCR_11_S_[2:1]	272 mA
VDDCR_11_GBE_S[2:1]	GND
VDDPL_11_SYS_S	70 mA
VDDAN_11_USB_S_[2:1]	140 mA
VDDCR_11_USB_S_[2:1]	42 mA
VDDAN_11_SSUSB_S_[5:1]	282 mA
VDDCR_11_SSUSB_S_[4:1]	424 mA

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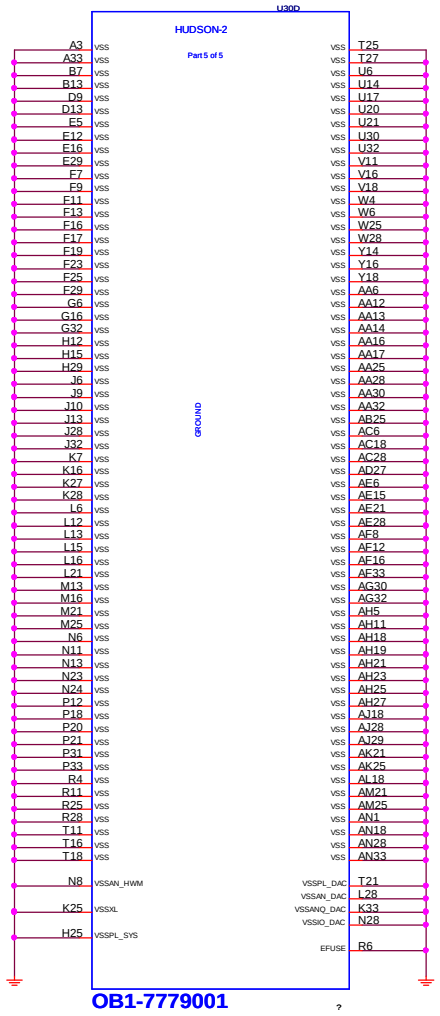
Title: MS-7857

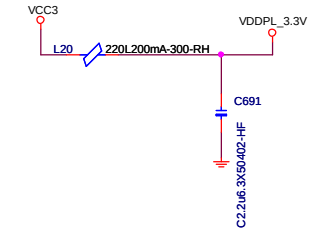
Size: Custom | Document Number: HUDSON POWER | Rev: 10

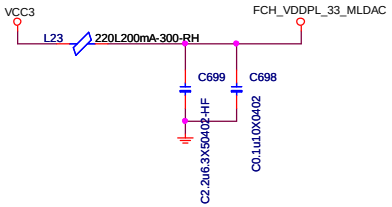
Date: Monday, December 17, 2012 | Sheet 19 of 37

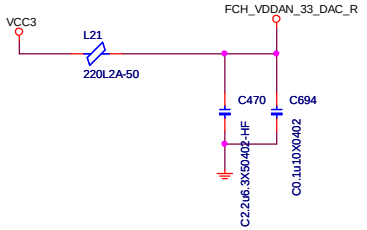


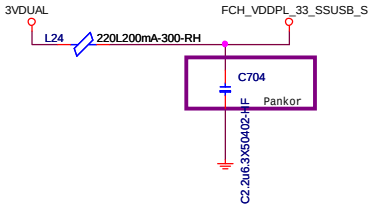
Layout:
VSSPL_SYS;VSSAN_HWM CONNECT TO GND
WITH A SEPREATED VIA

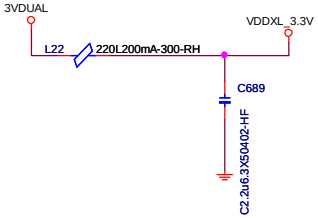
LAYOUT:
ROUTE THE POWER TRACES 15MILS WIDTH AT LEAST
PLACE THE DECOUPING CAPS CLOSE TO FCH ASAP
PLACE FB<=1" ,CAPS <=0.2"

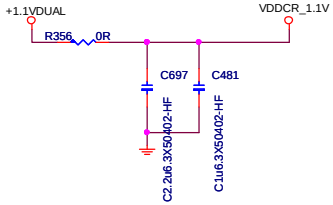


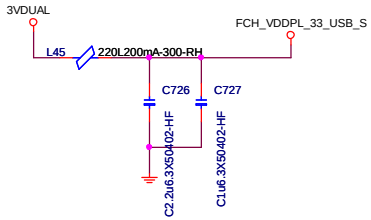


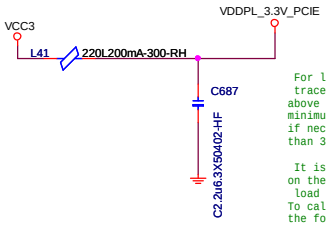






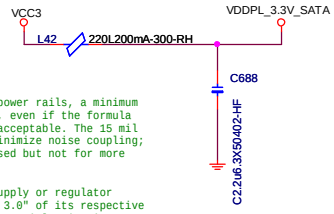


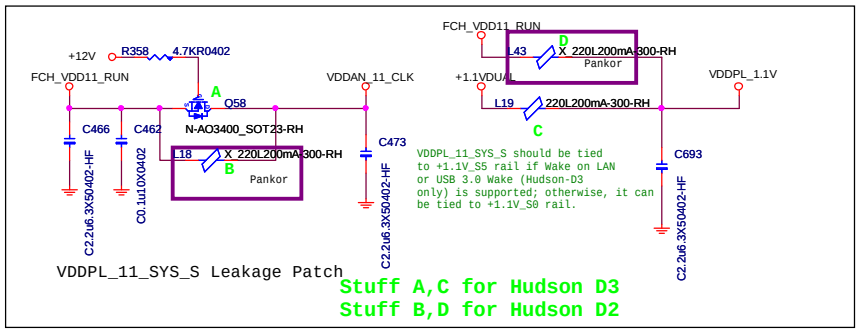


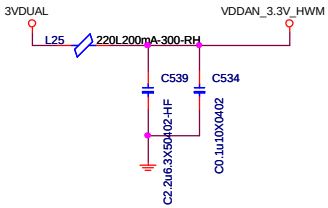


For low current PLL, analog and IO power rails, a minimum trace width of 15 mils must be used, even if the formula above shows that a thinner trace is acceptable. The 15 mil minimum trace width is required to minimize noise coupling; if necessary, thinner trace can be used but not for more than 300 mils of trace length

It is recommended that each power supply or regulator on the motherboard be located within 3.0" of its respective load to minimize voltage drop and potential noise issues. To calculate the minimum power delivery trace width, use the formula: Vdroop = I*R, where R=老*L/A (老 = resistivity of material, L = trace length, A = trace cross-sectional area). Vdroop must be < 2.5% of the nominal power rail voltage under maximum current conditions



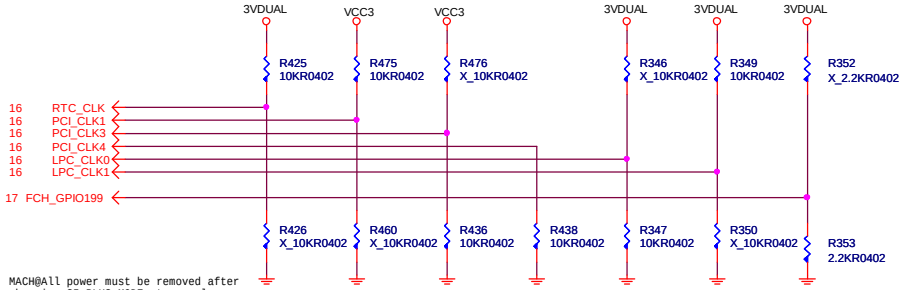




MICRO-START INT'L CO.,LTD.

Title	MS-7857	
Size: Custom	Document Number: HUDSON GND	Rev: 10
Date: Monday, December 17, 2012	Sheet 20 of 37	

FCH REQUIRED STRAPS



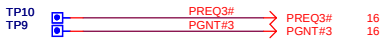
	RTCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5 PLUS MODE DISABLED DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	Reserved	EC ENABLED	INTERNAL CLOCK GEN ENABLED DEFAULT	LPC ROM
PULL LOW	S5 PLUS MODE ENABLED	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Required setting for intergrated CLOCK MODE DEFAULT	EC DISABLED DEFAULT	INTERNAL CLOCK GEN DISABLED	SPI ROM DEFAULT

FCH DEBUG STRAPS

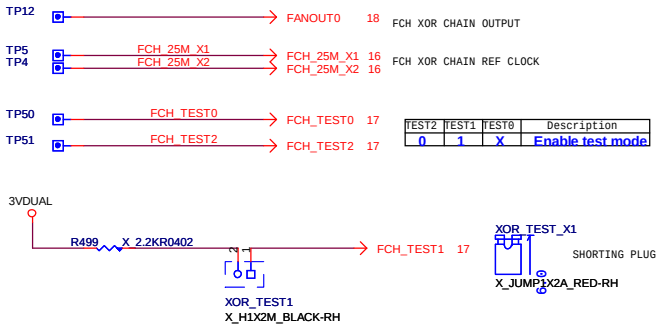
Provided test point access for lab use.
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED	Normal REFCLK Termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL DOWN	BYPASS PCI PLL	RESERVED	Inverted REFCLK Termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

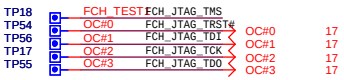
FCH PCIE EEPROM STRAPS



FCH XOR CHAIN TEST



FCH ICE DEBUG /JTAG TEST PINS



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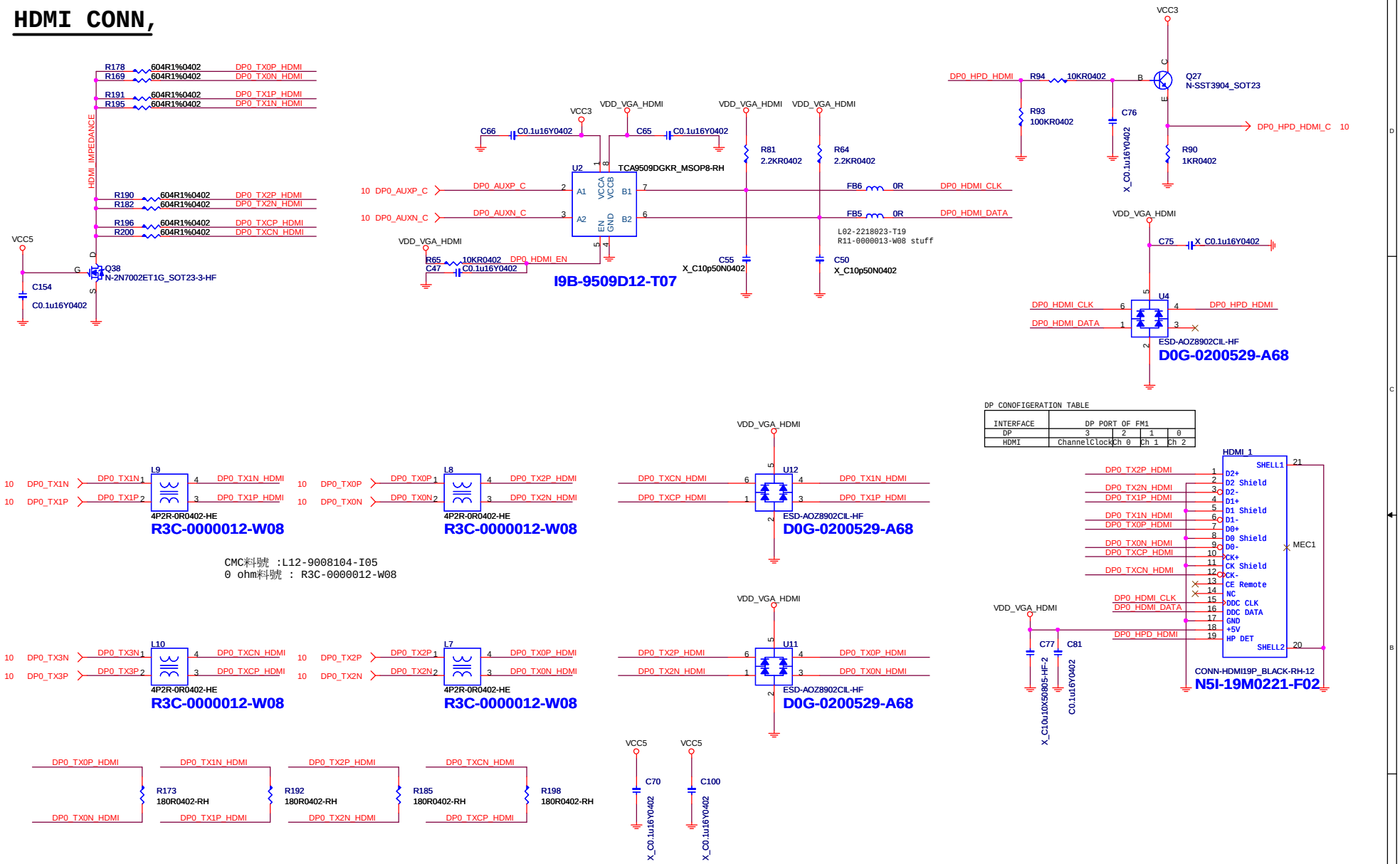
Title	MS-7857	
Size: Custom	Document Number: HUDSON STRAPS	Rev: 10
Date: Monday, December 17, 2012	Sheet 21 of 37	

HDMI CONN,



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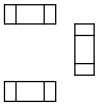
Title	MS-7857	
Size: Custom	Document Number: HDMI CONN.	Rev: 10
Date: Monday, December 17, 2012	Sheet 22 of 37	

VGA CONNECTOR

R932-R934 CLOSE TO CRT CONNECTOR, THE
TRACE IMPEDANCE BETWEEN NB AND 150OHM
RESISTOR SHOULD BE 37OHM+/-15%, THE
TRACE IMPEDANCE BETWEEN THE 2 150OHM

RESISTOR SHOULD BE 50 OHM +/-15%,

THE IMPEDANCE BETWEEN THE 2ND RESISTOR
TO THE CONNECTOR SHOULD BE 75OHM+/-15%



Layout:PLACE L 90 DEGREE
FROM EACH OTHER

VDD_VGA_HDMI

C127 X_C0.1u16X0402

U10
ESD-AOZ8902CIL-HF

BLUE_CONN
RED_CONN
GREEN_CONN

D0G-0200529-A68

PLACE ESD PROTECTION DIODES
1. CLOSE TO CONNECTOR PINS
2. DIRECTLY ON SIGNAL TRACES
3. +5V & GND TRACE TO DIODE SHOULDBE
   LESS THAN 100MILS AND 20MILS WIDE
4. THE ESD DIODE SHOULD BE THE FIRST DEVICE
   FROM CONNECTOR

VDD_VGA_HDMI

C92 X_C0.1u16X0402

U8
ESD-AOZ8902CIL-HF

VSYNC_CONN
HSYNC_CONN
DDCDATA_CONN
DDCCLK_CONN

D0G-0200529-A68

mach@The value of L,C refer to demo board,maybe adjusted for test

CLOSE TO VGA Connector

18 HUDSON_VGA_R

L6 10n300mA — VGA_R — L5 10n300mA

R157 150R1%0402
C131 C3.3p50N0402
C134 C3.3p50N0402
C130 C10p50N0402

18 HUDSON_VGA_G

L4 10n300mA — VGA_G — L3 10n300mA

R146 150R1%0402
C126 C3.3p50N0402
C128 C3.3p50N0402
C125 C10p50N0402

18 HUDSON_VGA_B

L2 10n300mA — VGA_B — L1 10n300mA

R145 150R1%0402
C122 C3.3p50N0402
C123 C3.3p50N0402
C121 C10p50N0402

VDD_VGA_HDMI

DDCCLK_5V R133 33R0402 DDCCLK_CONN
VSYNC_5V R108 27R0402 VSYNC_CONN
HSYNC_5V R134 27R0402 HSYNC_CONN
DDCDATA_5V R107 33R0402 DDCDATA_CONN

C113 X_C100p50N0402
C103 X_C18p50N0402
C110 X_C18p50N0402
C93 X_C100p50N0402

VGA_1
DSUB-VGAF_BLUE-RH-18
N51-15F0801-K06

BLUE_CONN
GREEN_CONN
RED_CONN

VDD_VGA_HDMI

VCC5
C105 C0.1u16Y0402
R141 X_2.2KR0402
18 HUDSON_VGA_HSYNC
HSYNC_5V
U9
AHCT1G126GV_SOT23-5-RH
T34-1G12609-N47
C114 X_C10p50N0402

VDD_VGA_HDMI

VCC5
C91 C0.1u16Y0402
R109 X_2.2KR0402
18 HUDSON_VGA_VSYNC
VSYNC_5V
U7
AHCT1G126GV_SOT23-5-RH
T34-1G12609-N47
C104 X_C10p50N0402

VDD_VGA_HDMI

R104 4.7KR0402
R132 4.7KR0402
18 HUDSON_VGA_SDAT
R105
DDCDATA_5V
18 HUDSON_VGA_SCLK
R140
DDCCLK_5V

+12V
R92 4.7KR0402
VCC5
Q26
N-2N7002ET1G_SOT23-3-HF
F-MICROSMD110F-RH
D08-0100210-R02

VDD_VGA_HDMI

C85 X_C10u10X5080S-HF-2
C86 C0.1u16Y0402

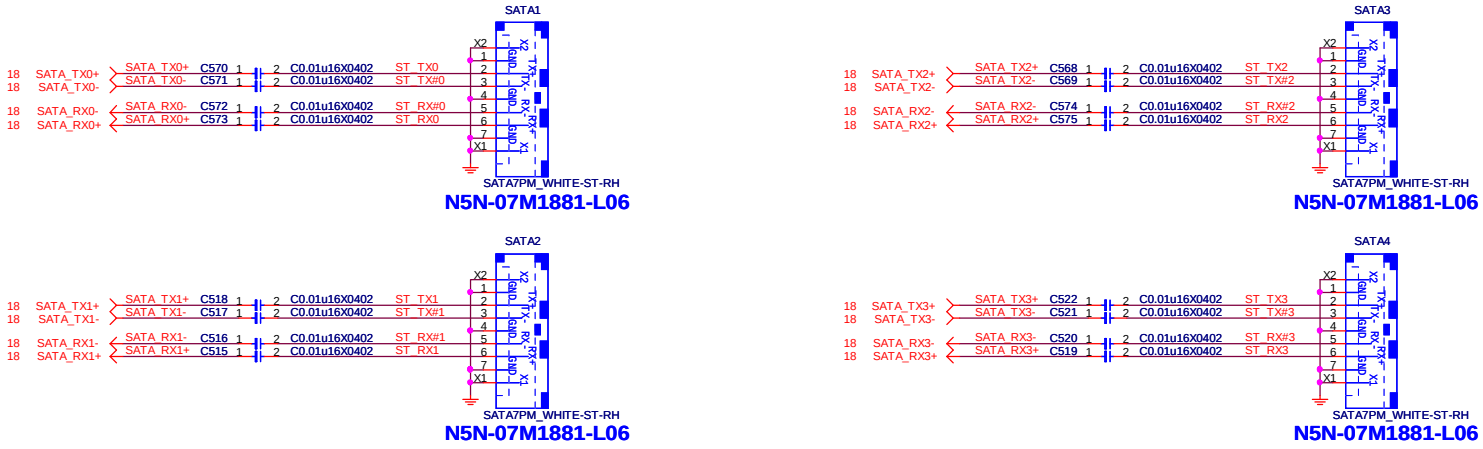
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: MS-7857		
Size: Custom	Document Number: VGA CONN.	Rev: 10
Date: Monday, December 17, 2012	Sheet 23 of 37	

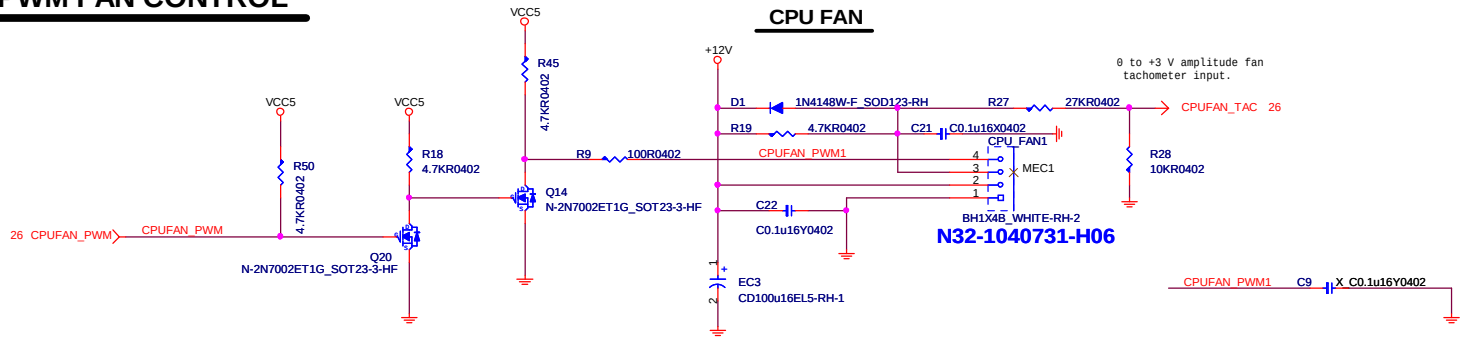
iSATA CONNECTOR

Multiple eSATA function

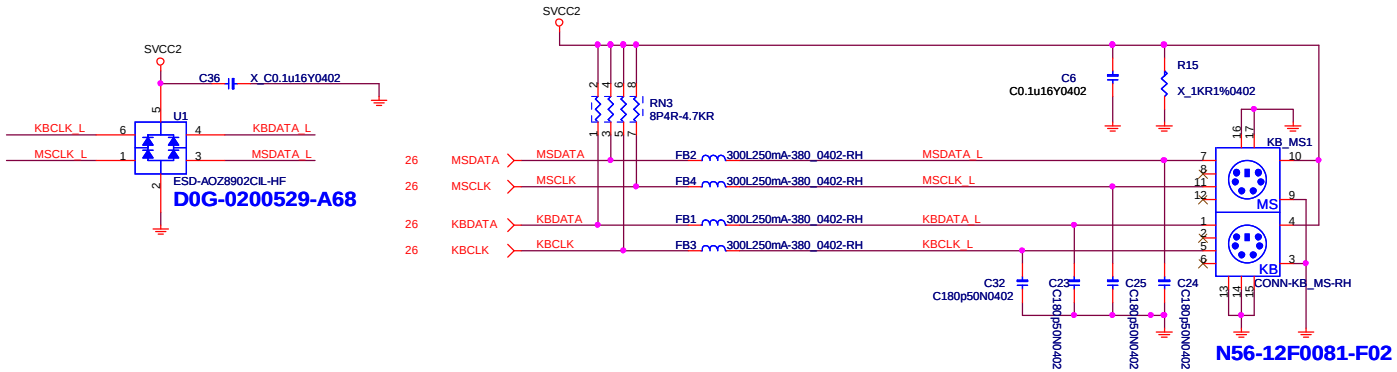
Layout:For Gen 3.0,trace length within 2.5''



PWM FAN CONTROL



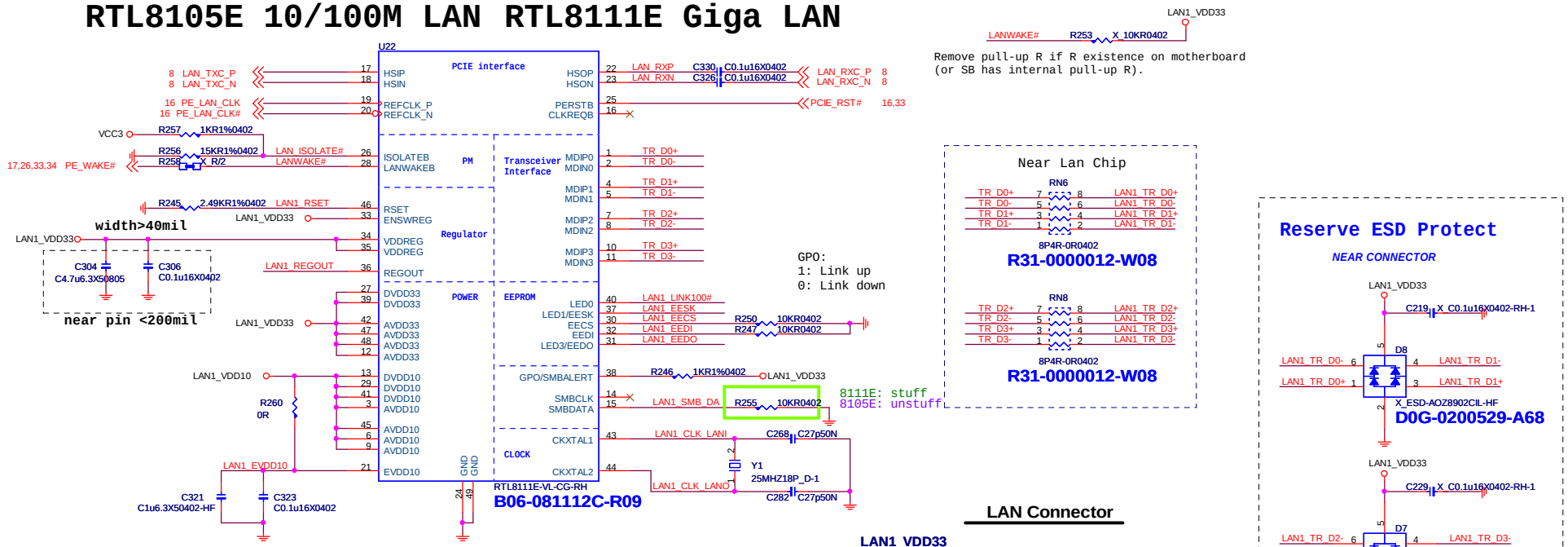
PS2 KEYBOARD & MOUSE CONNECTOR



MICRO-START INT'L CO.,LTD.

Title	MS-7857		
Size: Custom	Document Number: SATA/PS2/FAN		Rev: 10
Date: Monday, December 17, 2012	Sheet 24 of 37		

RTL8105E 10/100M LAN RTL8111E Giga LAN



Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).

Near Lan Chip

RN6
8P4R-0R0402
R31-0000012-W08

RN8
8P4R-0R0402
R31-0000012-W08

Reserve ESD Protect

NEAR CONNECTOR

D8
X_ESD-AOZ8902CIL-HF
D0G-0200529-A68

D7
X_ESD-AOZ8902CIL-HF
D0G-0200529-A68

1pF	2pF
D0G-0422003-P03	D0G-0200529-A68
D0G-0422003-N47	D0G-0303309-C12

3.3v Power on rise time : 1~100ms.

Place near pin 27 39 42 47 48 12

MAX: 163mA

8111E: stuff
8105E: unstuff

8111E: 0R

Place near pin 3 13 19 45 41 6 9

8111E: stuff
8105E: unstuff

8111E: unstuff
8105E: stuff

LAN Connector

LAN1_VDD33

For EMI

8111E: 200R

RJ45_USBX2_LEDX2_TX-GIGA-RH-5
N58-22F0731-F02

R14, R15, R17請依據所使用的LAN connector上的LED亮度去調整阻值

Giga-Lan	10/100-Lan
N58-22F0731-F02	N58-22F0061-S42
N58-22F0731-S42	N58-22F0061-F02
N58-22F0731-I60	
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	

19 Yellow 20
21 Orange 22 Green

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

width>60mil
LAN1_VDD10
CHOKE9
CH-4.7u0.85A170mS-HF
L04-47A7340-T04
OL4-7672004
near pin36 <200mil

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

D5 D9 D10

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Title	MS-7857	
Size: Custom	Document Number: LAN - RTL8111E	Rev: 10
Date: Monday, December 17, 2012	Sheet 25 of 37	

Super I/O

LPC SUPER I/O F71808A

U33

F71808A

F71808AU-LAB-RH

B02-7180834-F34

F71808A EUP Function

FCH HAS INTE-GRATED PU RESISTER

PWRBTN Check list pull up

VOLTAGE SENSING(H/W Monitor)

The best voltage input level is about 1V.

M/B ID

2	1	0	ROM TYPE
0	0	0	defaul
0	0	1	Lenovo
0	1	0	Reserved
0	1	1	Reserved

Temperature Sensing

Diode / Resistor SENSING CIRCUIT

close to PWM MOS

D02-0390619-P03

close to SIO

D02-0390619-P03

LPC Debug Port

H2X7[10]M-2PITCH_BLACK-HF

N31-2071271-H06

USB_MODE CONTROL

LPC I/O STRAPPING RESISTOR

POWER-ON TRIP

PIN	Function	NET Name	HI	LO
59	Config 4E/2E	SOUTA	4E	2E
57	STRAP_PWOK	STRAP_PWOK	PWOK (pin 35) for AMD	PWOK (pin 35) for Intel

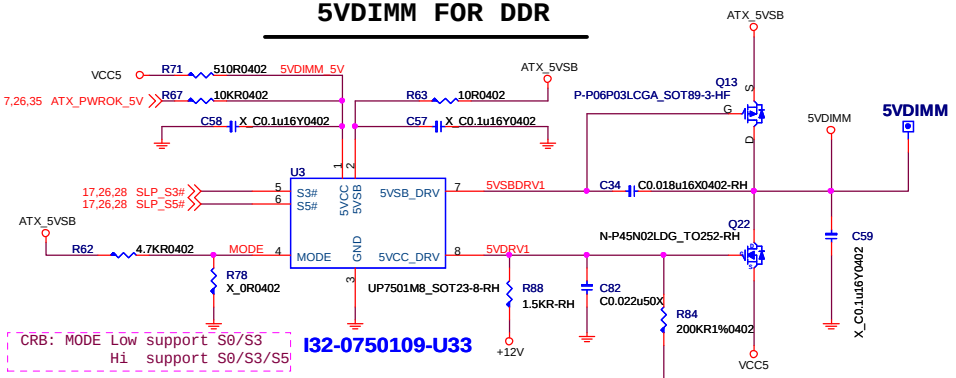
MICRO-STAR INT'L CO.,LTD.

Title: MS-7857

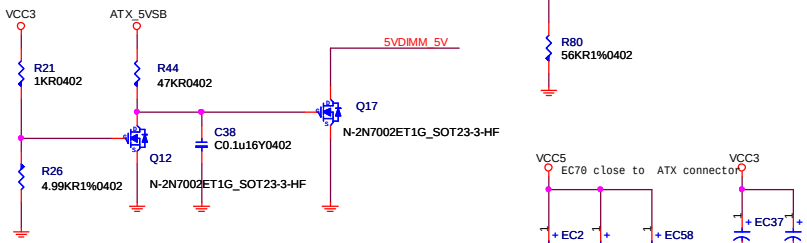
Size: Custom | Document Number: SUPER I/O 71808A | Rev: 10

Date: Monday, December 17, 2012 | Sheet 26 of 37

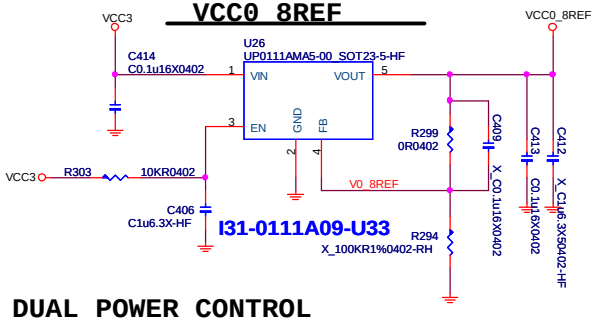
5VDIMM FOR DDR

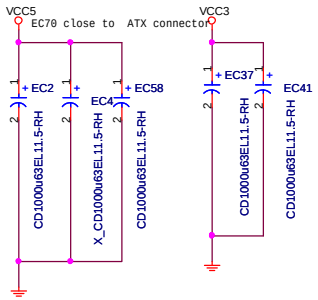


For special PSU sequence

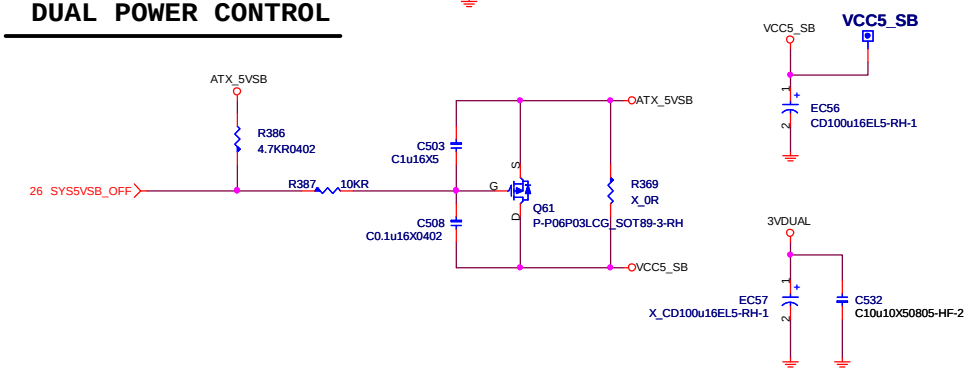


VCC0_8REF





DUAL POWER CONTROL

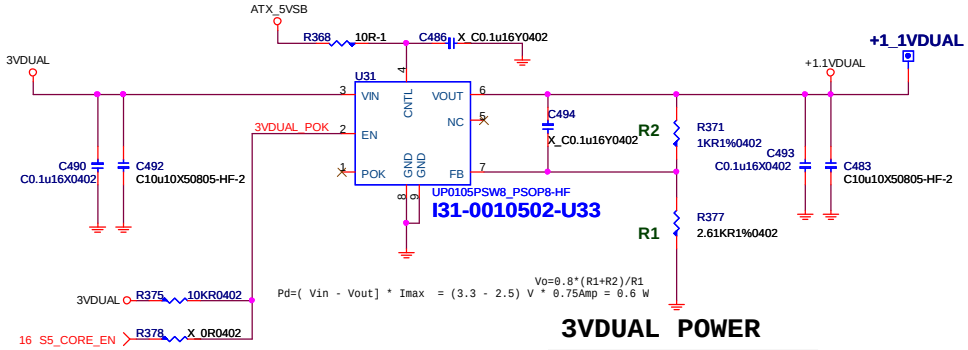


1.1VDUAL_POWER

1.V@1.23A

measurement:700mA

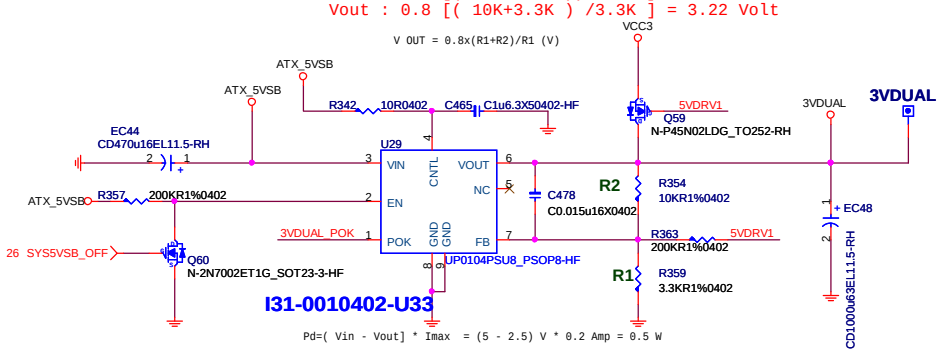
S0,S1,S3



3VDUAL_POWER

S0,S1,S3,S5,DEEP_S5 mach@Stuff when turn off VCC3_WAKE on S5 state

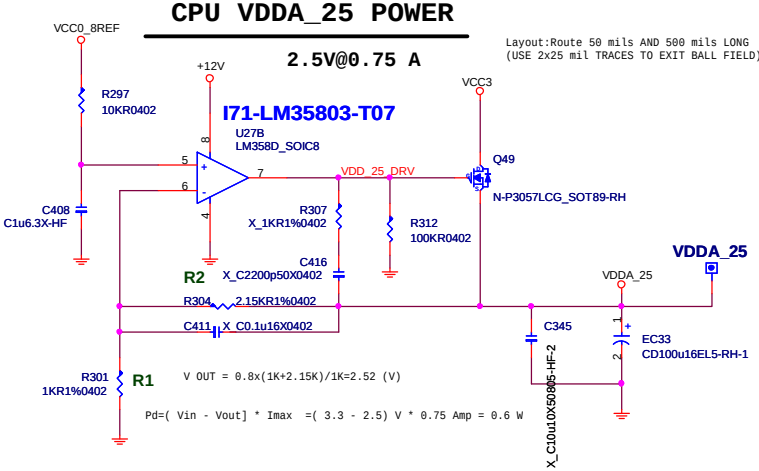
Vout : 0.8 [(R593+R599))/R599] = 3.3 Volt
Vout : 0.8 [(10K+3.3K) /3.3K] = 3.22 Volt



CPU VDDA_25 POWER

2.5V@0.75 A

Layout:Route 50 mils AND 500 mils LONG
(USE 2x25 mil TRACES TO EXIT BALL FIELD)



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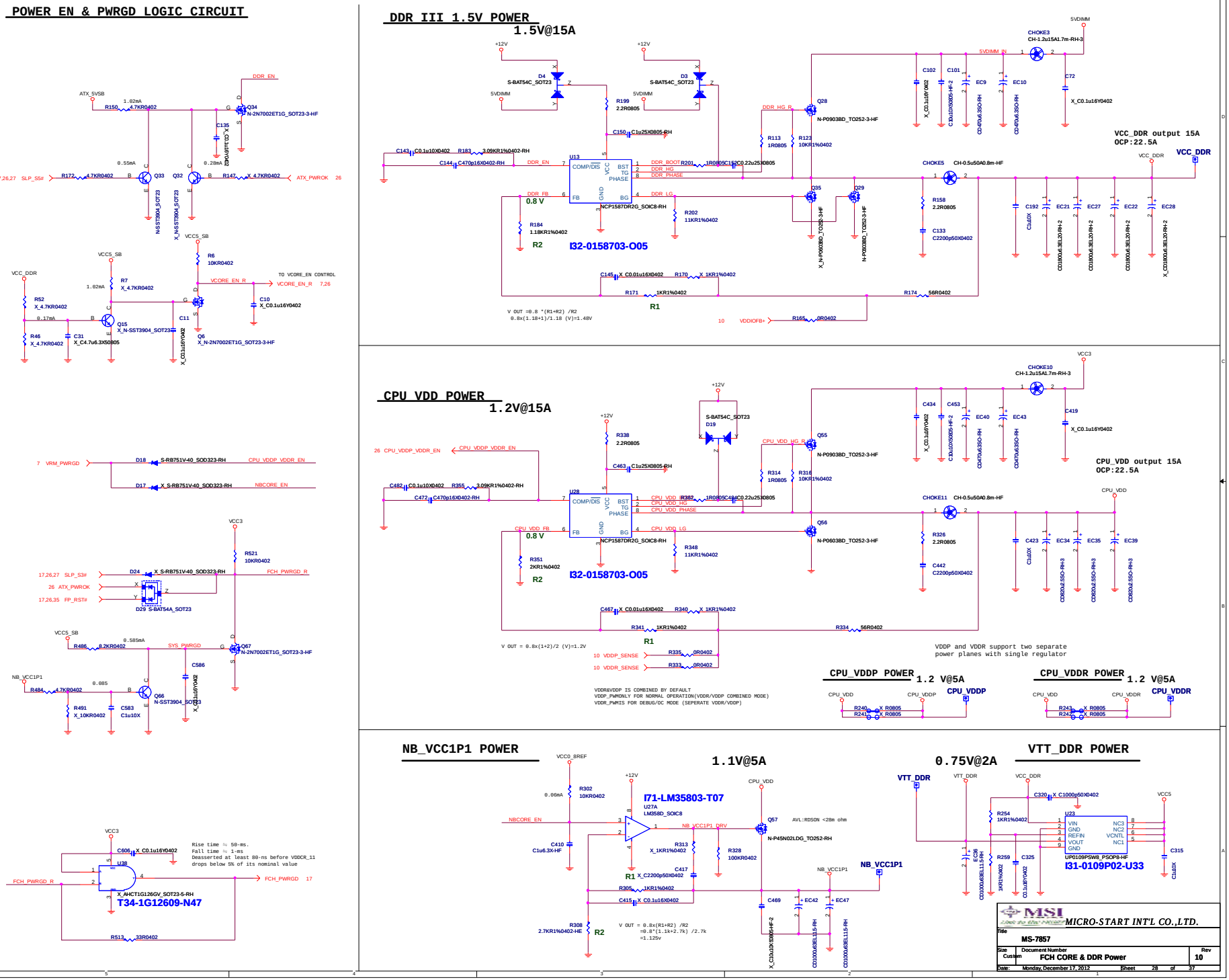
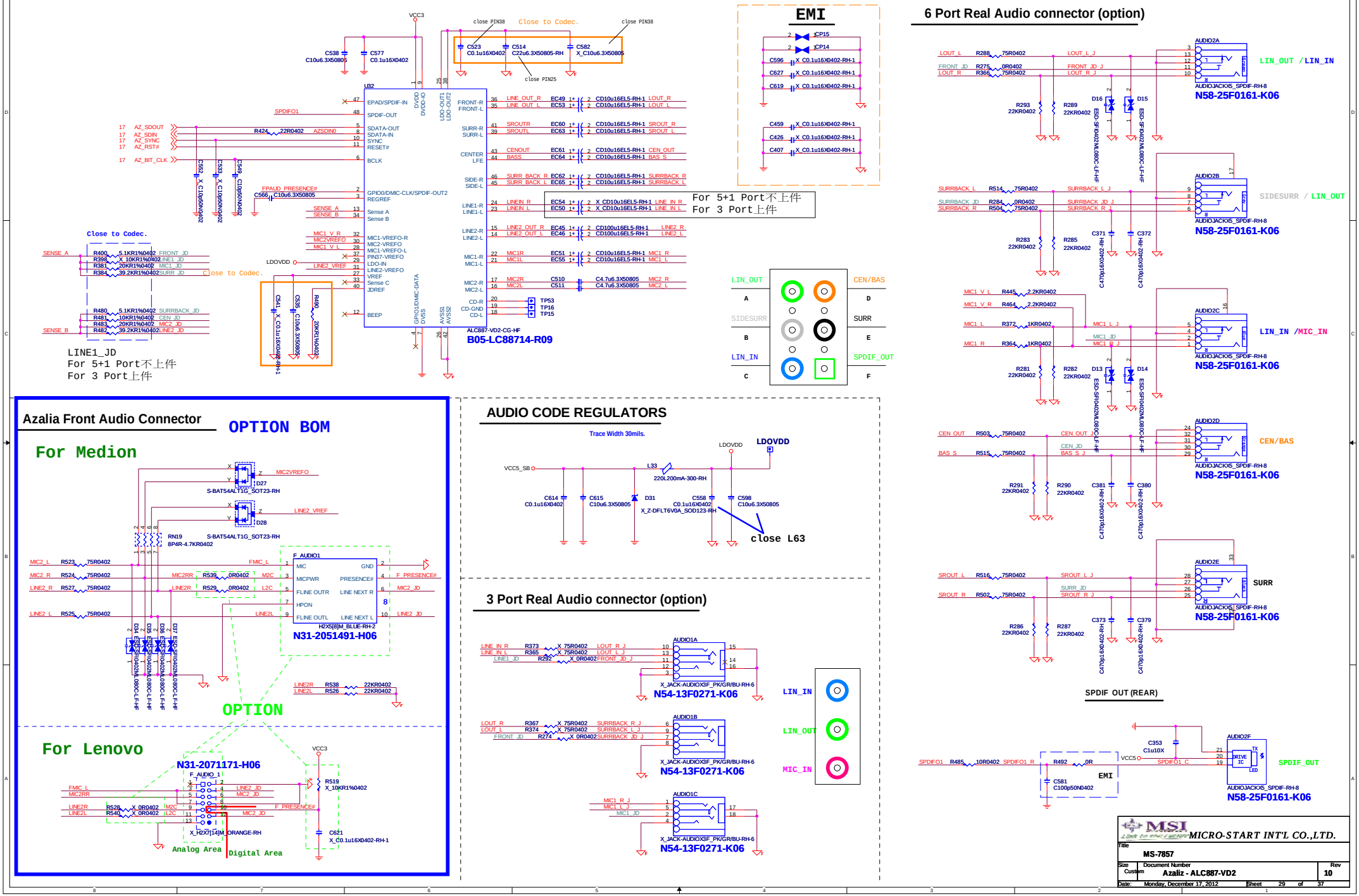
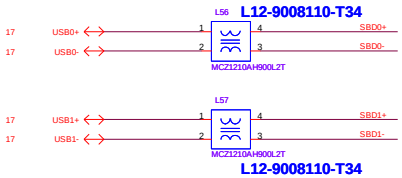
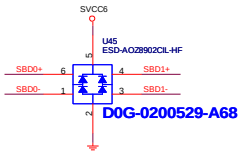
Title	MS-7857		
Size: Custom	Document Number: ACPI UPI & SYS POWER		Rev: 10
Date: Monday, December 17, 2012	Sheet 27 of 37		

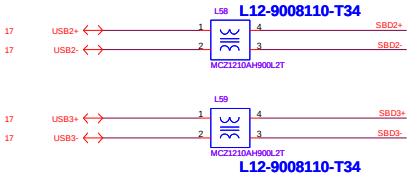


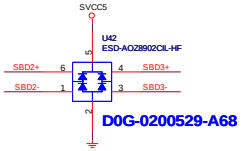


FRONT USB PIN HEADER

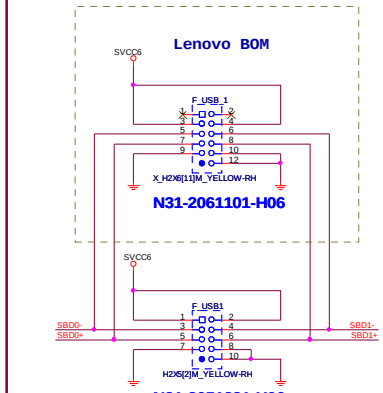


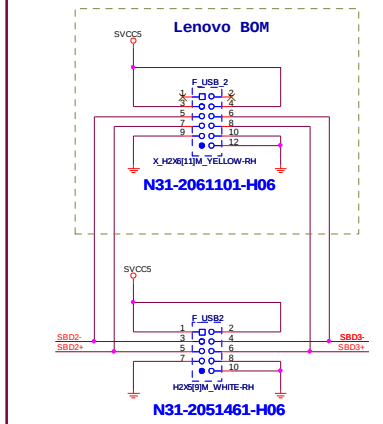






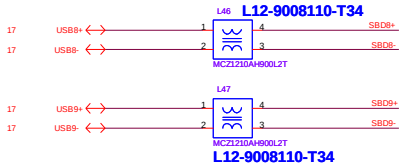
BOM Option

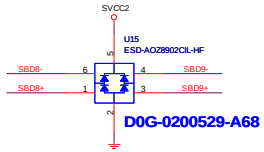


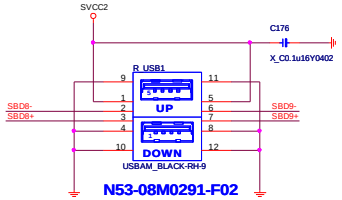


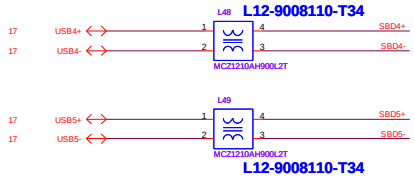
REAR PANEL USB CONNECTOR

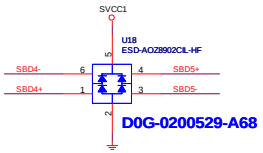
NEAR USB CONNECTOR

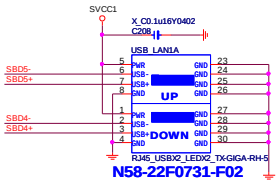












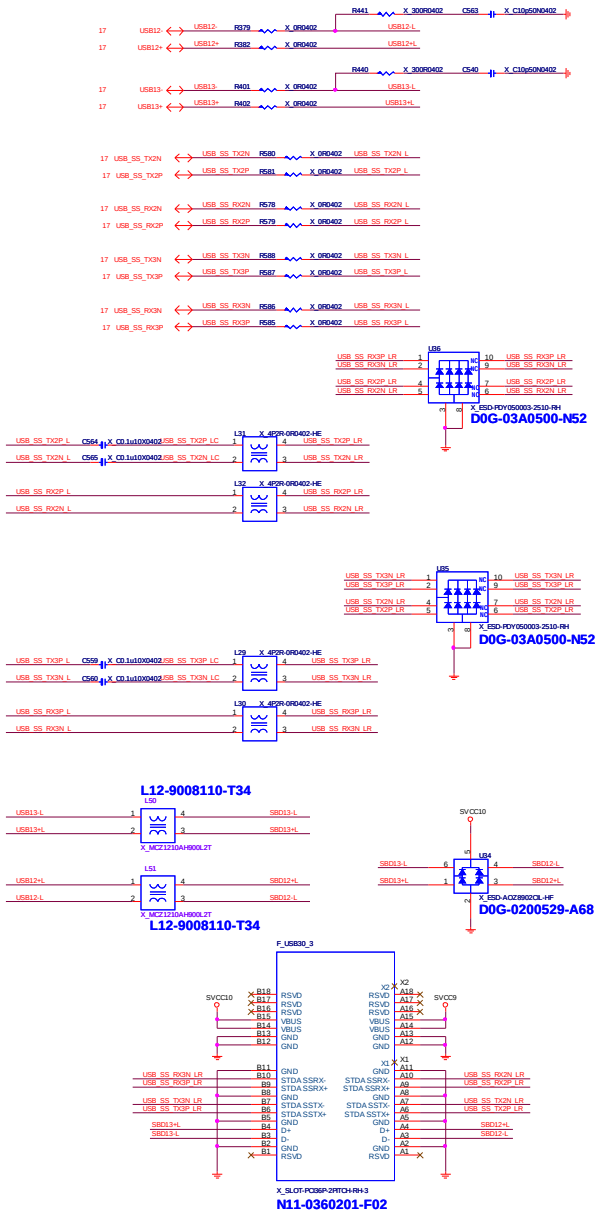
USB 2.0 trace length
REAR side within 18'';
FRONT side within 6''

MICRO-START INT'L CO.,LTD.

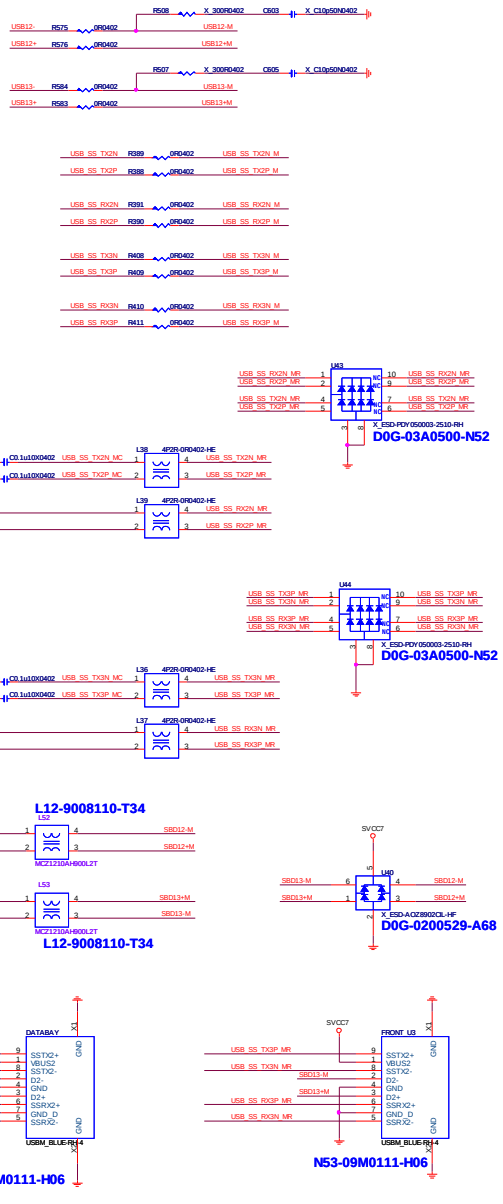
Title	MS-7857	
Size C	Document Number USB 2.0 CONN.	Rev 10
Date: Monday, December 17, 2012	Sheet 30 of 37	

Option BOM

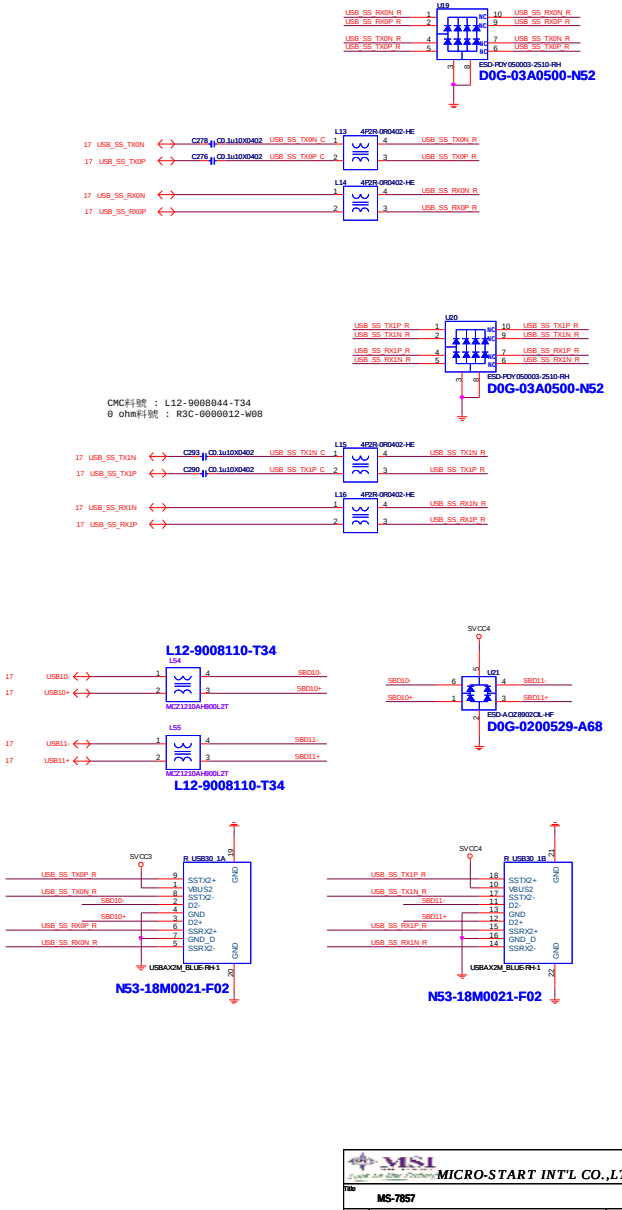
For Lenovo front USB3.0



For Medion front USB3.0



USB 3.0 trace length
Rear connector within 8''



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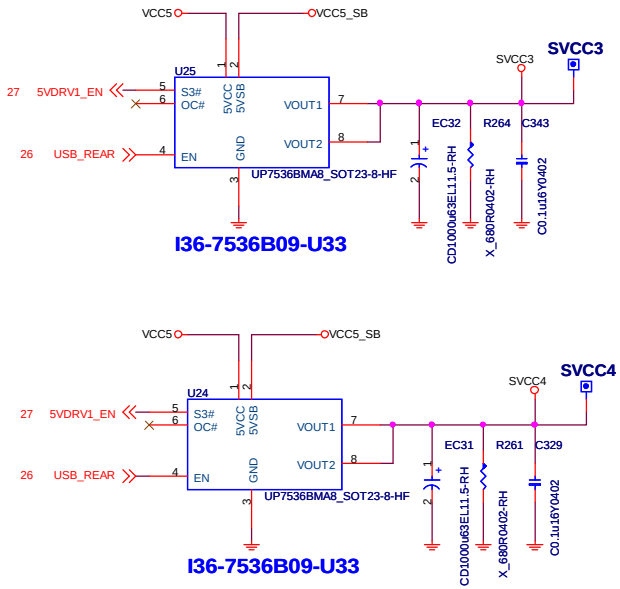
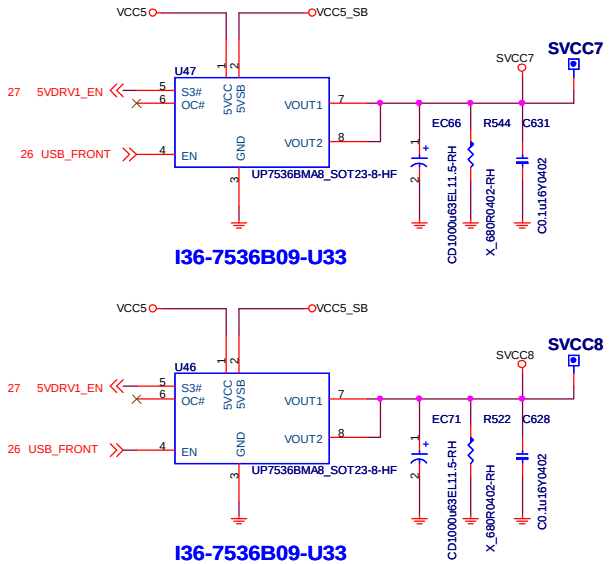
Title	MS-7857	
Size: Custom	Document Number: USB 3.0 CONN.	Rev: 10
Date: Monday, December 17, 2012	Sheet 31 of 37	

Rear USB30 Power SVCC3 SVCC4

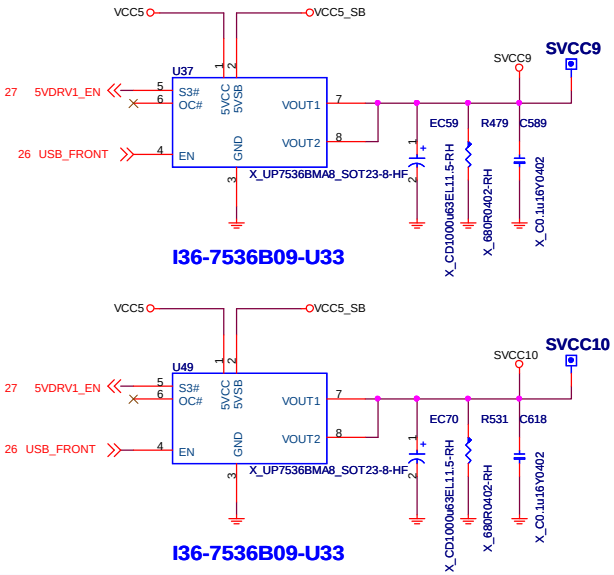


Option BOM

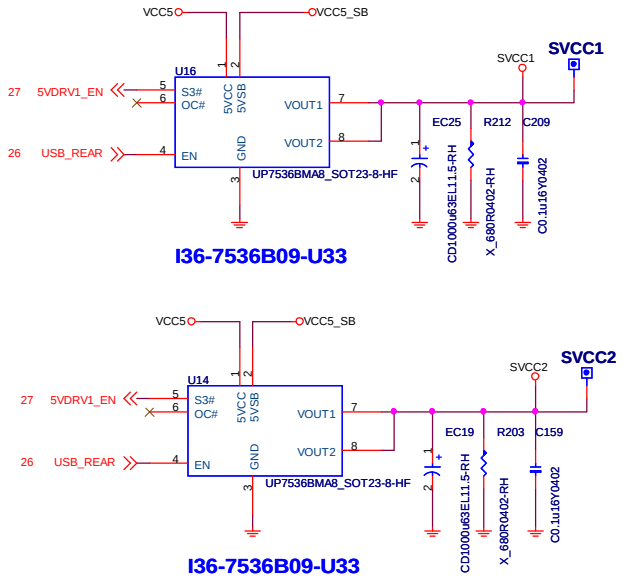
Front USB30 Power SVCC7 SVCC8(Medion)



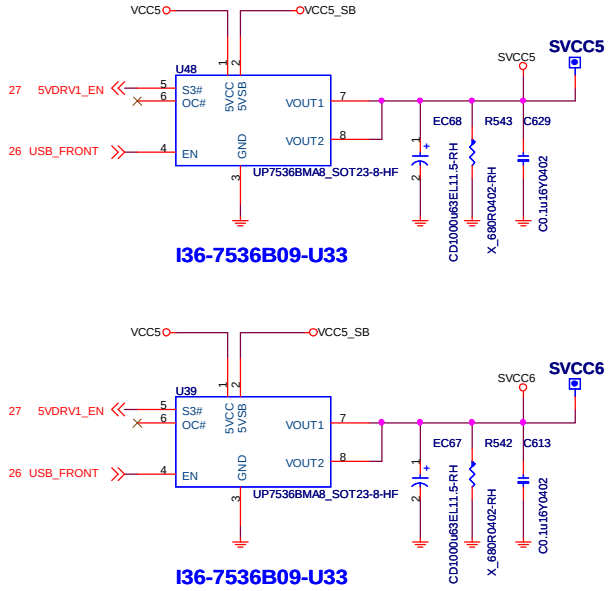
Front USB30 Power SVCC7 SVCC8(Lenovo)

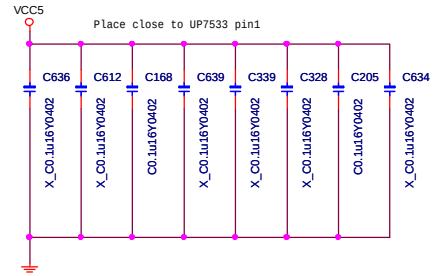


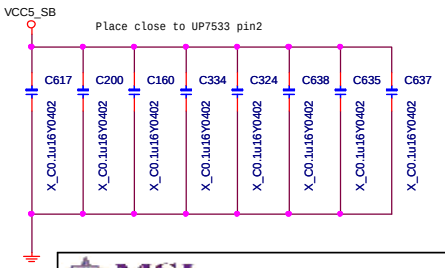
Rear USB20 Power SVCC1 SVCC2



Front USB20 Power SVCC5 SVCC6







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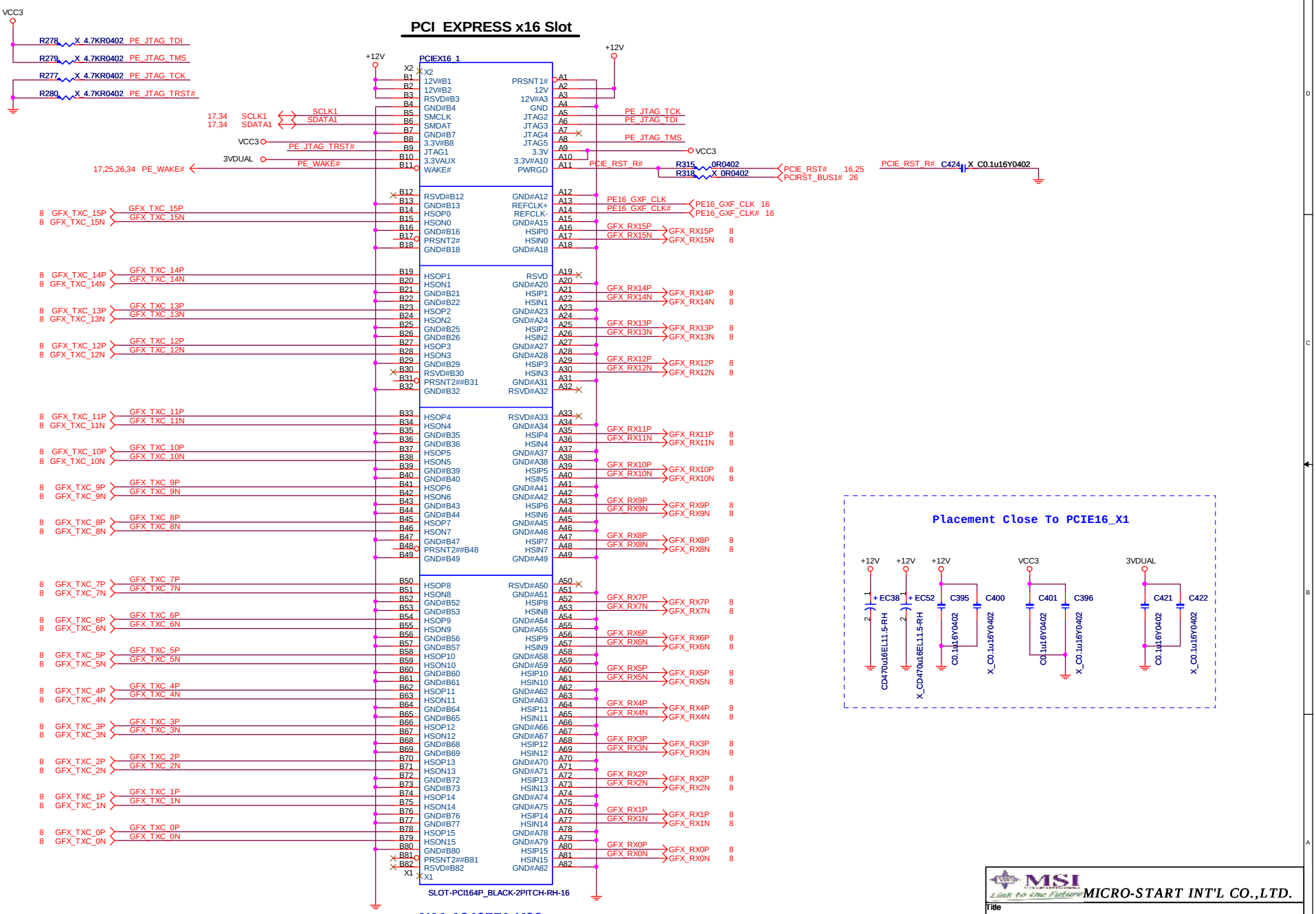
Title: MS-7857			
Size: Custom	Document Number: FUSION		Rev: 10
Date: Monday, December 17, 2012	Sheet 32 of 37		

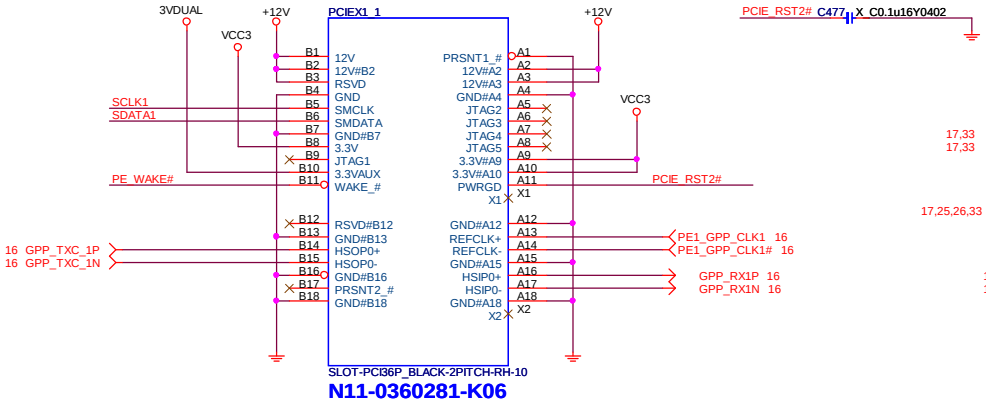
PCI Express Slot x16



N11-1640551-K06

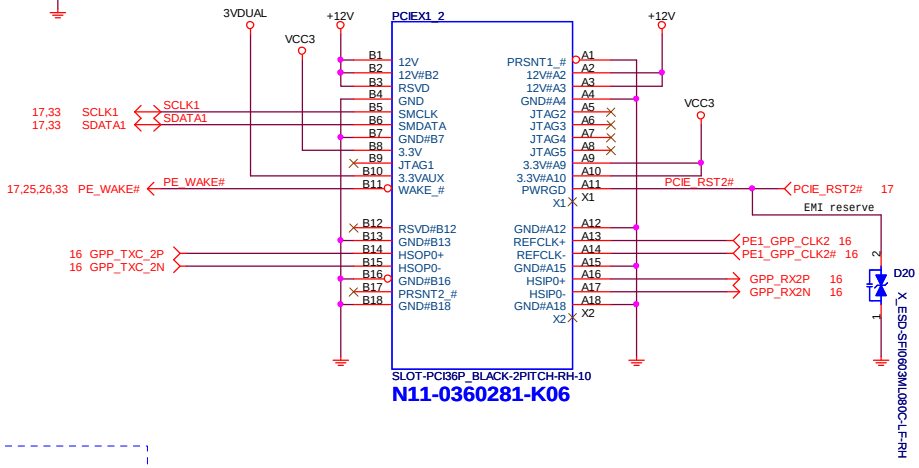
MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: MS-7857		
Size: Custom	Document Number: PCIE X16 SLOT	Rev: 10
Date: Monday, December 17, 2012	Sheet 33 of 37	

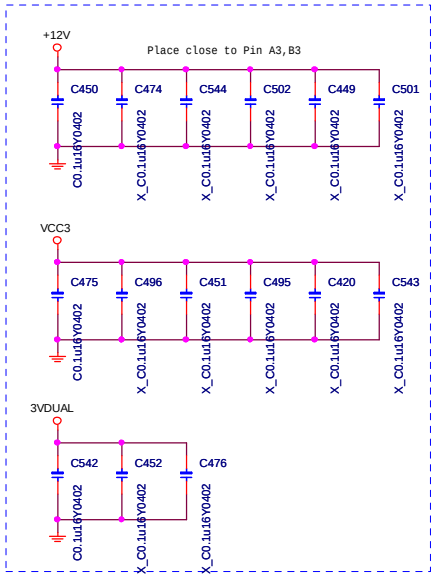
PCI EXPRESS X1 Slot-2



PCIE_RST2# C477 X_C0.1u16Y0402

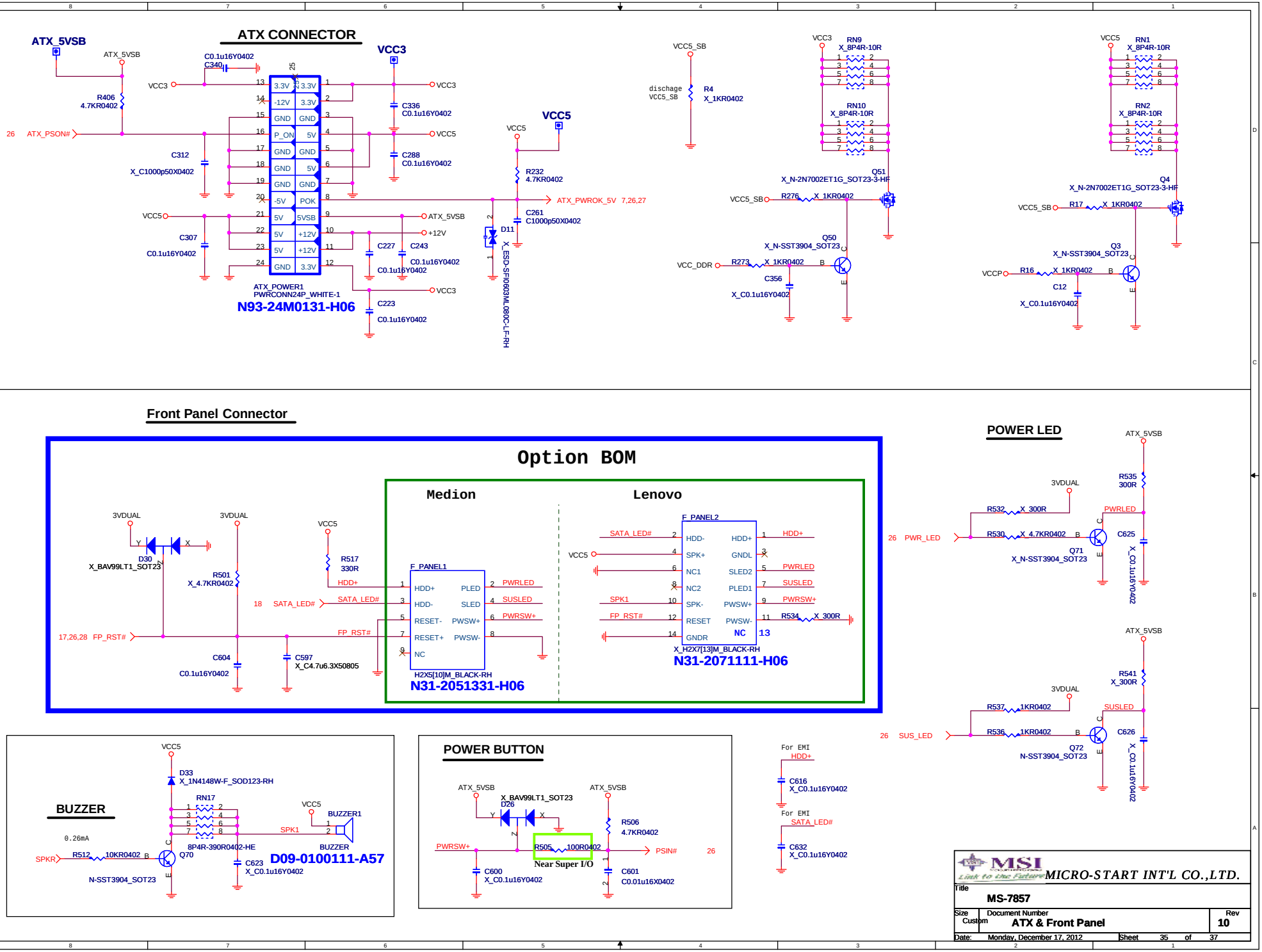
PCI EXPRESS X1 Slot-3





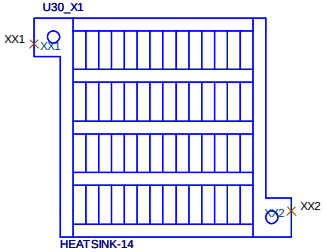
MICRO-START INT'L CO.,LTD.

Title: MS-7857		
Size: Custom	Document Number: FUSION	Rev: 10
Date: Monday, December 17, 2012	Sheet 34 of 37	



HEAT SINK

U30_X1



HEAT SINK-14

E31-0404831-K08

BIOS_LABEL

PCB

AMI BIOS

Label

HDMI Logo

HDMI Royalty

Y01-RHDMI03-000

Label1

HDMI Logo

HDMI Sticker

G51-M1SPX33-Q13

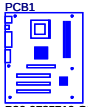
MANUAL PART

AVL:
D06-0100161-F52
D06-0100101-K26

BAT1_X1

BAT-BCR2032P-RH

PCB1



P30-0785710-G37

P30-0785710-G37

CPU RM

PROCESSOR1

E95-0000003-H06

E95-0000003-H06

Rubber1 Rubber2

PCB PCB

rubber1/2 rubber1/2

Pangkor

U902

HUDSON D2

X_AMD-218-0755064-A13-RH

U909

ALC662

X_ALC662-VC1-GR-C1-RH

U912

75R

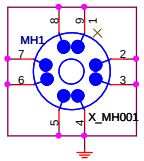
X_75R0402

U913

0R

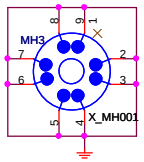
X_0R0402

MH1 MH2



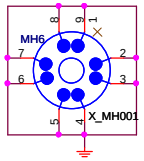
X_MH001 X_MH001

MH3 MH4



X_MH001 X_MH001

MH6 MH5



X_MH001 X_MH001

L10

BARCODE1

PCB

外部條碼

GD1-BC00038-F32

BARCODE2

PCB

置保貼紙

GD1-BC00201-F32

Hudson-D3

AMD-218-0755111-A14-RH-3

B01-21807S5-A08

LAN
Symbol ValueMSIP/N
RTL8111E-VB-GR-RHB06-081110C-R09金製程
RTL8111E-VL-CG-RHB06-081112C-R09銅製程

CODEC
ALC887-VD-GR-RHB05-LC88704-R09金製程
ALC887-VD2-CG-HFB05-LC88714-R09銅製程

ALC892-GR-RHB05-LC89204-R09金製程
ALC892-CG-RHB05-LC89214-R09 銅製程

ALC662-VC1-GR-C1-RHB09-LC66234-R09金製程
ALC662-CG-RHB05-LC66204-R09銅製程

Optics Orientation Holes

FM3 FM2
X_FM120 X_FM120
FM6 FM5
X_FM120 X_FM120
FM8 FM1
X_FM120 X_FM120
FM4 FM7
X_FM120 X_FM120

Simulation

X_JS2

VCC5 SIM1

X_PIN1*2

X_JS1

SIM2

X_PIN1*2

MICRO-START INT'L CO.,LTD.

Title: MS-7857

Size: Custom | Document Number: Auto BOM manual | Rev: 10

Date: Monday, December 17, 2012 | Sheet 36 of 37