Selek 15" Schematic

CFL-H refresh

2019/04/03

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

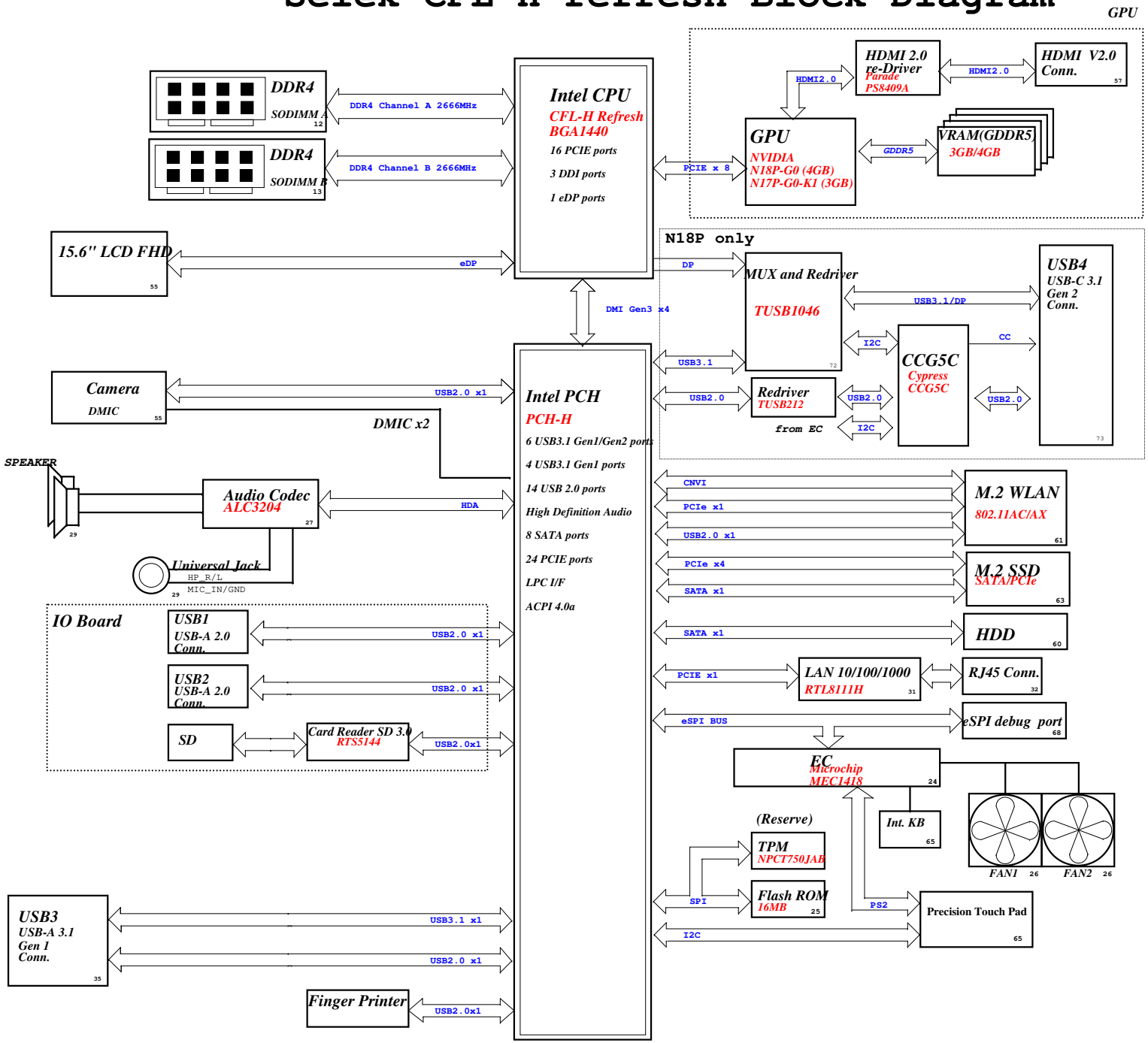
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A4	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 1 of 105	

Project Code : 4PD0H7010001
PCB P/N : 18825-1
Revision : A00

Selek CFL-H refresh Block Diagram



CHARGER		
ISL88739		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225RUKR-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5	

CPU Core Power		
NCP81208MNTXG NCP81382MNTXG x 2 NCP81382MNTXG (23e) NCP81253MNTBG		46~50
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCGT (23e)	
DCBATOUT	+VCCSA	

DDR4 SUS		
RT8231AGQW-GP APL5930KAI-TRG		51
INPUTS	OUTPUTS	
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3	

CPU VCCPRIM_CORE 1V		
		11
INPUTS	OUTPUTS	
1D0V_S5	+VCCPRIM_CORE	

CPU DCDC-V1D00A		
AOZ2262QI-10-GP-U		53
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	

LDO-V1D8V		
APL5930KAI-TRG		54
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	

5V/3V S0		
TPS22966DPUR-GP		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	

EOPIO/EDRAM (23e)		
TPS22961DNYT		40
INPUTS	OUTPUTS	
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR	

3D3V VGA		
AO3419L		86
INPUTS	OUTPUTS	
3D3V_S0	3D3V_VGA_S0	

VGA_CORE		
ISL62771HRTZ-GP-U		85
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	

1D5V_VGA_S0		
Y8288RAC-GP		86
INPUTS	OUTPUTS	
DCBATOUT	1D5V_VGA_S0	

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 2 of 105

HDMI

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N3

55 eDP_AUX_CPU_P
55 eDP_AUX_CPU_N

Soc AUD

15 AUD_AZACPU_SCLK
15 AUD_AZACPU_SDO
15 AUD_AZACPU_SDI_R

71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N0

71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N1

71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N2

71 DP1_DDI_TX_P3
71 DP1_DDI_TX_N3

71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P

PEG

76 GFX_PCIE_RX_P7
76 GFX_PCIE_RX_N7

76 GFX_PCIE_RX_P6
76 GFX_PCIE_RX_N6

76 GFX_PCIE_RX_P5
76 GFX_PCIE_RX_N5

76 GFX_PCIE_RX_P4
76 GFX_PCIE_RX_N4

76 GFX_PCIE_RX_P3
76 GFX_PCIE_RX_N3

76 GFX_PCIE_RX_P2
76 GFX_PCIE_RX_N2

76 GFX_PCIE_RX_P1
76 GFX_PCIE_RX_N1

76 GFX_PCIE_RX_P0
76 GFX_PCIE_RX_N0

76 GFX_PCIE_TX_CON_P7
76 GFX_PCIE_TX_CON_N7

76 GFX_PCIE_TX_CON_P6
76 GFX_PCIE_TX_CON_N6

76 GFX_PCIE_TX_CON_P5
76 GFX_PCIE_TX_CON_N5

76 GFX_PCIE_TX_CON_P4
76 GFX_PCIE_TX_CON_N4

76 GFX_PCIE_TX_CON_P3
76 GFX_PCIE_TX_CON_N3

76 GFX_PCIE_TX_CON_P2
76 GFX_PCIE_TX_CON_N2

76 GFX_PCIE_TX_CON_P1
76 GFX_PCIE_TX_CON_N1

76 GFX_PCIE_TX_CON_P0
76 GFX_PCIE_TX_CON_N0

DMI

18 DMI_RX_CPU_P0
18 DMI_RX_CPU_N0

18 DMI_RX_CPU_P1
18 DMI_RX_CPU_N1

18 DMI_RX_CPU_P2
18 DMI_RX_CPU_N2

18 DMI_RX_CPU_P3
18 DMI_RX_CPU_N3

18 DMI_TX_CPU_P0
18 DMI_TX_CPU_N0

18 DMI_TX_CPU_P1
18 DMI_TX_CPU_N1

18 DMI_TX_CPU_P2
18 DMI_TX_CPU_N2

18 DMI_TX_CPU_P3
18 DMI_TX_CPU_N3

DP to Type-C

CPU1D 4 OF 13

DP1_DDI_TX_P0 K36 DDI1_TXP_0 EDP_TXP_0 D29 eDP_TX_CPU_P0
DP1_DDI_TX_N0 K37 DDI1_TXN_0 EDP_TXN_0 E29 eDP_TX_CPU_N0
DP1_DDI_TX_P1 J35 DDI1_TXP_1 EDP_TXP_1 F28 eDP_TX_CPU_P1
DP1_DDI_TX_N1 J34 DDI1_TXN_1 EDP_TXN_1 E28 eDP_TX_CPU_N1
DP1_DDI_TX_P2 H37 DDI1_TXP_2 EDP_TXP_2 A26 eDP_TX_CPU_P2
DP1_DDI_TX_N2 H36 DDI1_TXN_2 EDP_TXN_2 B29 eDP_TX_CPU_N2
DP1_DDI_TX_P3 J37 DDI1_TXP_3 EDP_TXP_3 C26 eDP_TX_CPU_P3
DP1_DDI_TX_N3 J38 DDI1_TXN_3 EDP_TXN_3 B28 eDP_TX_CPU_N3

Port B

DP1_AUX_CPU_P D27 DDI1_AUXP EDP_AUXP C26 eDP_AUX_CPU_P
DP1_AUX_CPU_N E27 DDI1_AUXN EDP_AUXN B26 eDP_AUX_CPU_N

H34 DDI2_TXP_0
H33 DDI2_TXN_0
F37 DDI2_TXP_1 EDP_DISP_UTIL A33
G38 DDI2_TXN_1
F34 DDI2_TXP_2 EDP_RCOMP D37
F35 DDI2_TXN_2
E37 DDI2_TXP_3

Port C

E36 DDI2_TXN_3

F26 DDI2_AUXP
E26 DDI2_AUXN

C34 DDI3_TXP_0
D34 DDI3_TXN_0
B36 DDI3_TXP_1
B34 DDI3_TXN_1
F33 DDI3_TXP_2
E33 DDI3_TXN_2
C33 DDI3_TXP_3
B33 DDI3_TXN_3

Port D

A27 DDI3_AUXP PROC_AUDIO_CLK G27 AUD_AZACPU_SCLK
B27 DDI3_AUXN PROC_AUDIO_SDI G26 AUD_AZACPU_SDO
PROC_AUDIO_SDO G29 AUD_AZACPU_SDI

4 of 13

Do Not Stuff

0D95V_VCCIO
R301 2 1 24D9R2F-L-GP
R302 1 2 20R2J-3-GP
AUD_AZACPU_SDI_R

Layout Note:
Trace Width:12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

Layout Note:
Trace Width:12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)

CPU1C 3 OF 13

E25 D25 PEG_RXP_0 PEG_TXP_0 B25 A25 PEG_TXN_0
E24 F24 PEG_RXP_1 PEG_TXP_1 B24 C24 PEG_TXN_1
E23 D23 PEG_RXP_2 PEG_TXP_2 B23 A23 PEG_TXN_2
E22 F22 PEG_RXP_3 PEG_TXP_3 B22 C22 PEG_TXN_3
E21 D21 PEG_RXP_4 PEG_TXP_4 B21 A21 PEG_TXN_4
E20 F20 PEG_RXP_5 PEG_TXP_5 B20 C20 PEG_TXN_5
E19 D19 PEG_RXP_6 PEG_TXP_6 B19 A19 PEG_TXN_6
E18 F18 PEG_RXP_7 PEG_TXP_7 B18 C18 PEG_TXN_7

GFX_PCIE_RX_P7 D17 PEG_RXP_8 PEG_TXP_8 A17 GFX_PCIE_TX_P7 C323 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P7
GFX_PCIE_RX_N7 E17 PEG_RXN_8 PEG_TXN_8 B17 GFX_PCIE_TX_N7 C324 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N7
GFX_PCIE_RX_P6 F16 PEG_RXP_9 PEG_TXP_9 C16 GFX_PCIE_TX_P6 C321 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P6
GFX_PCIE_RX_N6 E16 PEG_RXN_9 PEG_TXN_9 B16 GFX_PCIE_TX_N6 C322 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N6
GFX_PCIE_RX_P5 D15 PEG_RXP_10 PEG_TXP_10 A15 GFX_PCIE_TX_P5 C318 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P5
GFX_PCIE_RX_N5 E15 PEG_RXN_10 PEG_TXN_10 B15 GFX_PCIE_TX_N5 C320 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N5
GFX_PCIE_RX_P4 F14 PEG_RXP_11 PEG_TXP_11 C14 GFX_PCIE_TX_P4 C307 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P4
GFX_PCIE_RX_N4 E14 PEG_RXN_11 PEG_TXN_11 B14 GFX_PCIE_TX_N4 C316 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N4
GFX_PCIE_RX_P3 D13 PEG_RXP_12 PEG_TXP_12 A13 GFX_PCIE_TX_P3 C314 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P3
GFX_PCIE_RX_N3 E13 PEG_RXN_12 PEG_TXN_12 B13 GFX_PCIE_TX_N3 C304 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N3
GFX_PCIE_RX_P2 F12 PEG_RXP_13 PEG_TXP_13 C12 GFX_PCIE_TX_P2 C309 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P2
GFX_PCIE_RX_N2 E12 PEG_RXN_13 PEG_TXN_13 B12 GFX_PCIE_TX_N2 C313 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P1 D11 PEG_RXP_14 PEG_TXP_14 A11 GFX_PCIE_TX_P1 C312 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P1
GFX_PCIE_RX_N1 E11 PEG_RXN_14 PEG_TXN_14 B11 GFX_PCIE_TX_N1 C302 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P0 F10 PEG_RXP_15 PEG_TXP_15 C10 GFX_PCIE_TX_P0 C310 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_P0
GFX_PCIE_RX_N0 E10 PEG_RXN_15 PEG_TXN_15 B10 GFX_PCIE_TX_N0 C311 1 SCD22U10V2KX-2-GP GFX_PCIE_TX_CON_N0

0D95V_VCCIO
R303 1 2 24D9R2F-L-GP
PEG_RCOMPO G2 PEG_RCOMP

DMI_RX_CPU_P0 D8 DMI_RXP_0 DMI_TXP_0 B8 DMI_TX_CPU_P0
DMI_RX_CPU_N0 E8 DMI_RXN_0 DMI_TXN_0 A8 DMI_TX_CPU_N0
DMI_RX_CPU_P1 E6 DMI_RXP_1 DMI_TXP_1 C6 DMI_TX_CPU_P1
DMI_RX_CPU_N1 F6 DMI_RXN_1 DMI_TXN_1 B6 DMI_TX_CPU_N1
DMI_RX_CPU_P2 D5 DMI_RXP_2 DMI_TXP_2 B5 DMI_TX_CPU_P2
DMI_RX_CPU_N2 E5 DMI_RXN_2 DMI_TXN_2 A5 DMI_TX_CPU_N2
DMI_RX_CPU_P3 J6 DMI_RXP_3 DMI_TXP_3 D4 DMI_TX_CPU_P3
DMI_RX_CPU_N3 J5 DMI_RXN_3 DMI_TXN_3 B4 DMI_TX_CPU_N3

3 OF 13

Do Not Stuff

Do Not Stuff

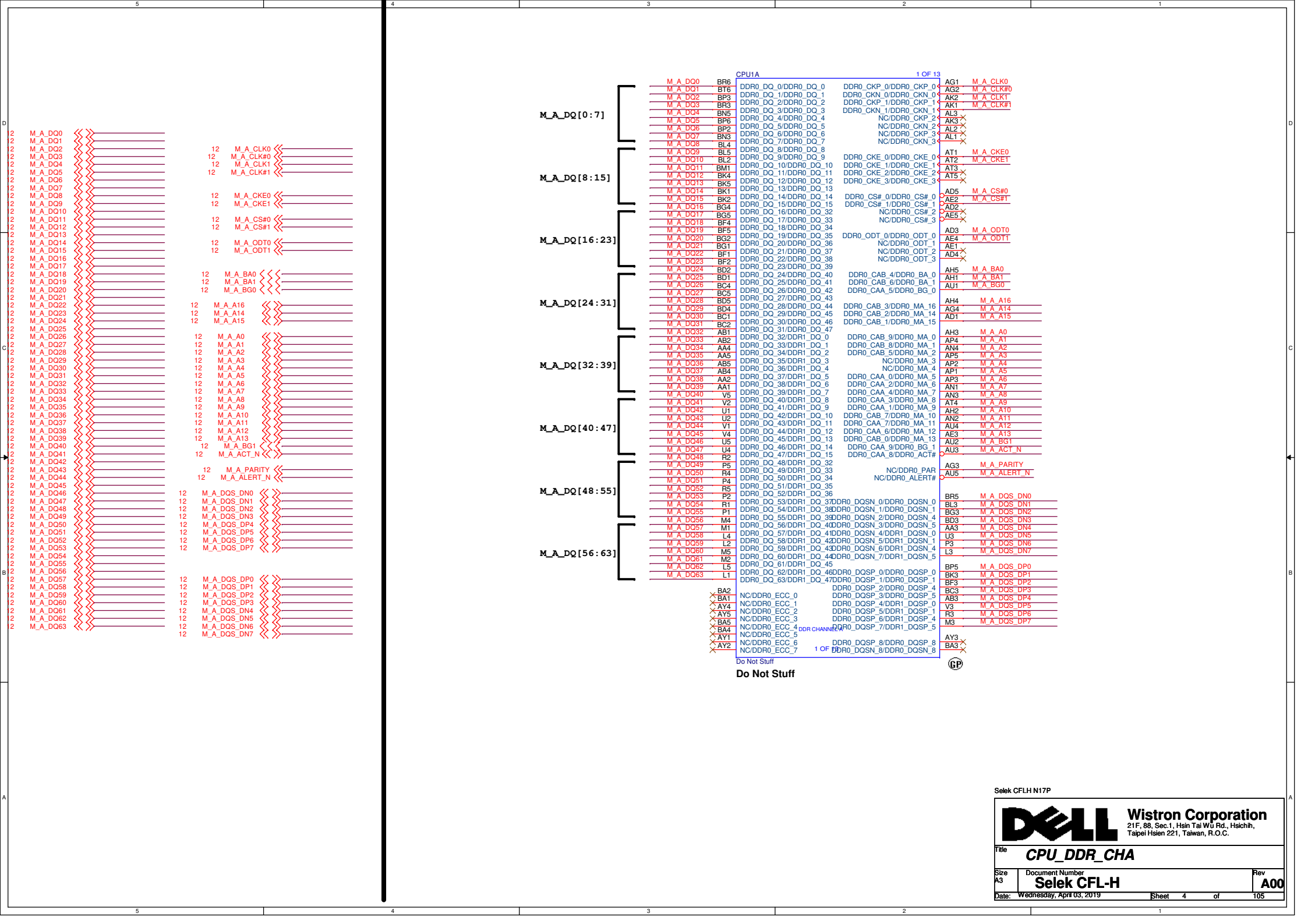
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

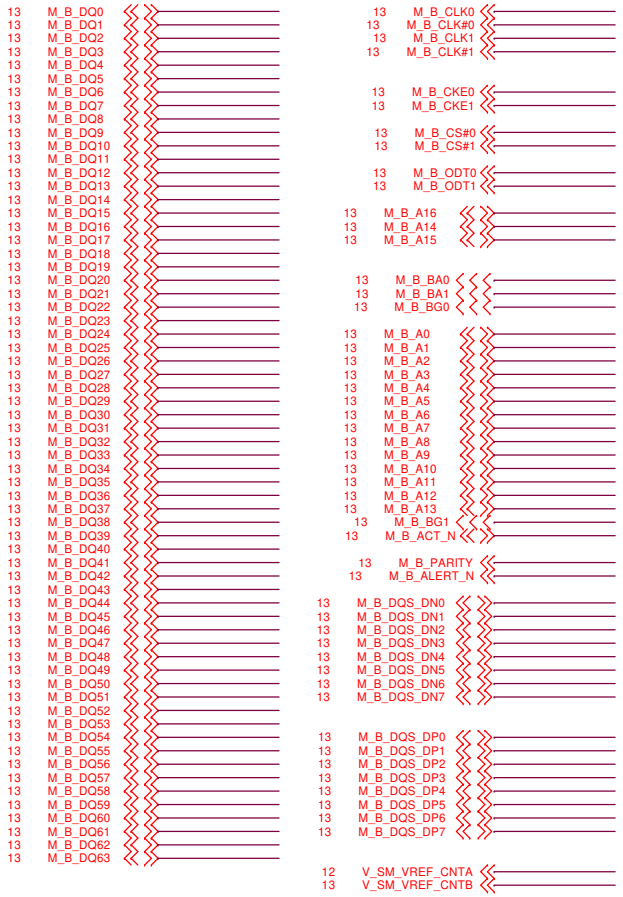
Title: CPU (PCIE/DMI/FDI)

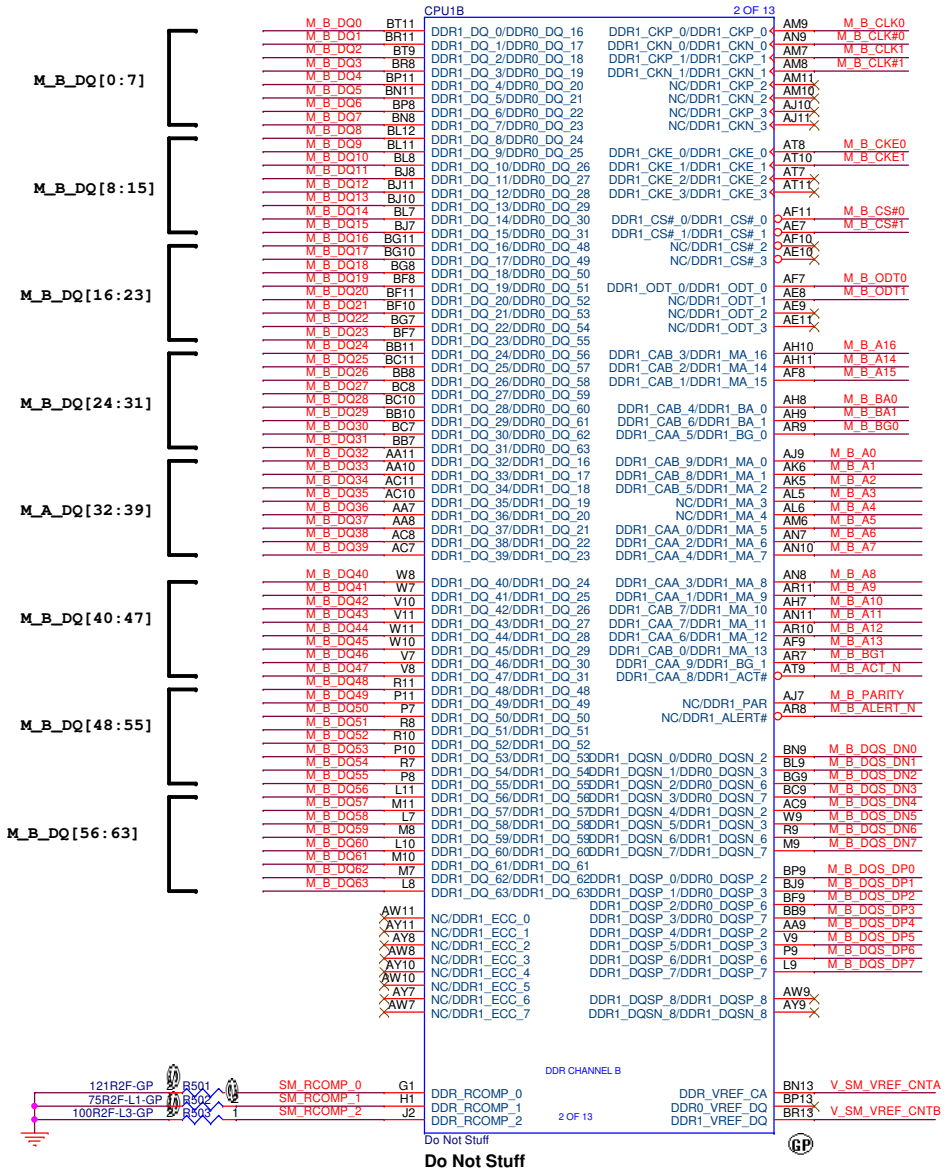
Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 3 of 105


M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
M_A_DQ22
M_A_DQ23
M_A_DQ24
M_A_DQ25
M_A_DQ26
M_A_DQ27
M_A_DQ28
M_A_DQ29
M_A_DQ30
M_A_DQ31
M_A_DQ32
M_A_DQ33
M_A_DQ34
M_A_DQ35
M_A_DQ36
M_A_DQ37
M_A_DQ38
M_A_DQ39
M_A_DQ40
M_A_DQ41
M_A_DQ42
M_A_DQ43
M_A_DQ44
M_A_DQ45
M_A_DQ46
M_A_DQ47
M_A_DQ48
M_A_DQ49
M_A_DQ50
M_A_DQ51
M_A_DQ52
M_A_DQ53
M_A_DQ54
M_A_DQ55
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
M_A_CLK0
M_A_CLK#0
M_A_CLK1
M_A_CLK#1
M_A_CKE0
M_A_CKE1
M_A_CS#0
M_A_CS#1
M_A_ODT0
M_A_ODT1
M_A_BA0
M_A_BA1
M_A_BG0
M_A_A16
M_A_A14
M_A_A15
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_BG1
M_A_ACT_N
M_A_PARITY
M_A_ALERT_N
M_A_DQS_DN0
M_A_DQS_DN1
M_A_DQS_DN2
M_A_DQS_DN3
M_A_DQS_DP4
M_A_DQS_DP5
M_A_DQS_DP6
M_A_DQS_DP7
M_A_DQS_DP0
M_A_DQS_DP1
M_A_DQS_DP2
M_A_DQS_DP3
M_A_DQS_DN4
M_A_DQS_DN5
M_A_DQS_DN6
M_A_DQS_DN7
M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]
CPU1A
1 OF 13
DDR0_DQ_0/DDR0_DQ_0
DDR0_DQ_1/DDR0_DQ_1
DDR0_DQ_2/DDR0_DQ_2
DDR0_DQ_3/DDR0_DQ_3
DDR0_DQ_4/DDR0_DQ_4
DDR0_DQ_5/DDR0_DQ_5
DDR0_DQ_6/DDR0_DQ_6
DDR0_DQ_7/DDR0_DQ_7
DDR0_DQ_8/DDR0_DQ_8
DDR0_DQ_9/DDR0_DQ_9
DDR0_DQ_10/DDR0_DQ_10
DDR0_DQ_11/DDR0_DQ_11
DDR0_DQ_12/DDR0_DQ_12
DDR0_DQ_13/DDR0_DQ_13
DDR0_DQ_14/DDR0_DQ_14
DDR0_DQ_15/DDR0_DQ_15
DDR0_DQ_16/DDR0_DQ_32
DDR0_DQ_17/DDR0_DQ_33
DDR0_DQ_18/DDR0_DQ_34
DDR0_DQ_19/DDR0_DQ_35
DDR0_DQ_20/DDR0_DQ_36
DDR0_DQ_21/DDR0_DQ_37
DDR0_DQ_22/DDR0_DQ_38
DDR0_DQ_23/DDR0_DQ_39
DDR0_DQ_24/DDR0_DQ_40
DDR0_DQ_25/DDR0_DQ_41
DDR0_DQ_26/DDR0_DQ_42
DDR0_DQ_27/DDR0_DQ_43
DDR0_DQ_28/DDR0_DQ_44
DDR0_DQ_29/DDR0_DQ_45
DDR0_DQ_30/DDR0_DQ_46
DDR0_DQ_31/DDR0_DQ_47
DDR0_DQ_32/DDR1_DQ_0
DDR0_DQ_33/DDR1_DQ_1
DDR0_DQ_34/DDR1_DQ_2
DDR0_DQ_35/DDR1_DQ_3
DDR0_DQ_36/DDR1_DQ_4
DDR0_DQ_37/DDR1_DQ_5
DDR0_DQ_38/DDR1_DQ_6
DDR0_DQ_39/DDR1_DQ_7
DDR0_DQ_40/DDR1_DQ_8
DDR0_DQ_41/DDR1_DQ_9
DDR0_DQ_42/DDR1_DQ_10
DDR0_DQ_43/DDR1_DQ_11
DDR0_DQ_44/DDR1_DQ_12
DDR0_DQ_45/DDR1_DQ_13
DDR0_DQ_46/DDR1_DQ_14
DDR0_DQ_47/DDR1_DQ_15
DDR0_DQ_48/DDR1_DQ_32
DDR0_DQ_49/DDR1_DQ_33
DDR0_DQ_50/DDR1_DQ_34
DDR0_DQ_51/DDR1_DQ_35
DDR0_DQ_52/DDR1_DQ_36
DDR0_DQ_53/DDR1_DQ_37
DDR0_DQ_54/DDR1_DQ_38
DDR0_DQ_55/DDR1_DQ_39
DDR0_DQ_56/DDR1_DQ_40
DDR0_DQ_57/DDR1_DQ_41
DDR0_DQ_58/DDR1_DQ_42
DDR0_DQ_59/DDR1_DQ_43
DDR0_DQ_60/DDR1_DQ_44
DDR0_DQ_61/DDR1_DQ_45
DDR0_DQ_62/DDR1_DQ_46
DDR0_DQ_63/DDR1_DQ_47
NC/DDR0_ECC_0
NC/DDR0_ECC_1
NC/DDR0_ECC_2
NC/DDR0_ECC_3
NC/DDR0_ECC_4
NC/DDR0_ECC_5
NC/DDR0_ECC_6
NC/DDR0_ECC_7
DDR CHANNEL A
1 OF 13
DDR0_CKP_0/DDR0_CKP_0
DDR0_CKN_0/DDR0_CKN_0
DDR0_CKP_1/DDR0_CKP_1
DDR0_CKN_1/DDR0_CKN_1
NC/DDR0_CKP_2
NC/DDR0_CKN_2
NC/DDR0_CKP_3
NC/DDR0_CKN_3
DDR0_CKE_0/DDR0_CKE_0
DDR0_CKE_1/DDR0_CKE_1
DDR0_CKE_2/DDR0_CKE_2
DDR0_CKE_3/DDR0_CKE_3
DDR0_CS#_0/DDR0_CS#_0
DDR0_CS#_1/DDR0_CS#_1
NC/DDR0_CS#_2
NC/DDR0_CS#_3
DDR0_ODT_0/DDR0_ODT_0
NC/DDR0_ODT_1
NC/DDR0_ODT_2
NC/DDR0_ODT_3
DDR0_CAB_4/DDR0_BA_0
DDR0_CAB_6/DDR0_BA_1
DDR0_CAA_5/DDR0_BG_0
DDR0_CAB_3/DDR0_MA_16
DDR0_CAB_2/DDR0_MA_14
DDR0_CAB_1/DDR0_MA_15
DDR0_CAB_9/DDR0_MA_0
DDR0_CAB_8/DDR0_MA_1
DDR0_CAB_5/DDR0_MA_2
NC/DDR0_MA_3
NC/DDR0_MA_4
DDR0_CAA_0/DDR0_MA_5
DDR0_CAA_2/DDR0_MA_6
DDR0_CAA_4/DDR0_MA_7
DDR0_CAA_3/DDR0_MA_8
DDR0_CAA_1/DDR0_MA_9
DDR0_CAB_7/DDR0_MA_10
DDR0_CAA_7/DDR0_MA_11
DDR0_CAA_6/DDR0_MA_12
DDR0_CAB_0/DDR0_MA_13
DDR0_CAA_9/DDR0_BG_1
DDR0_CAA_8/DDR0_ACT#
NC/DDR0_PAR
NC/DDR0_ALERT#
DDR0_DQSN_0/DDR0_DQSN_0
DDR0_DQSN_1/DDR0_DQSN_1
DDR0_DQSN_2/DDR0_DQSN_4
DDR0_DQSN_3/DDR0_DQSN_5
DDR0_DQSN_4/DDR1_DQSN_0
DDR0_DQSN_5/DDR1_DQSN_1
DDR0_DQSN_6/DDR1_DQSN_4
DDR0_DQSN_7/DDR1_DQSN_5
DDR0_DQSP_0/DDR0_DQSP_0
DDR0_DQSP_1/DDR0_DQSP_1
DDR0_DQSP_2/DDR0_DQSP_4
DDR0_DQSP_3/DDR0_DQSP_5
DDR0_DQSP_4/DDR1_DQSP_0
DDR0_DQSP_5/DDR1_DQSP_1
DDR0_DQSP_6/DDR1_DQSP_4
DDR0_DQSP_7/DDR1_DQSP_5
DDR0_DQSP_8/DDR0_DQSP_8
DDR0_DQSN_8/DDR0_DQSN_8
Do Not Stuff
Do Not Stuff
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_DDR_CHA
Size
A3
Document Number
Selek CFL-H
Rev
A00
Date:
Wednesday, April 03, 2019
Sheet
4
of
105

SSID = CPU



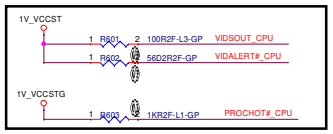


Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_DDR_CHB	
Size A3	Document Number Selek CFL-H	Rev A00
Date: Wednesday, April 03, 2019	Sheet 5 of 105	

AROUND_CPU



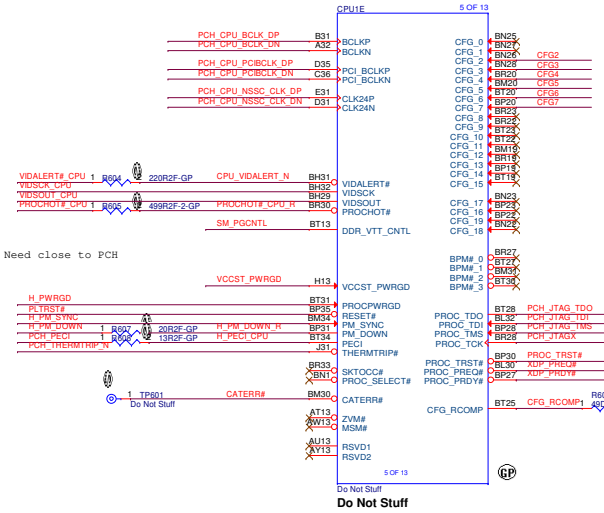


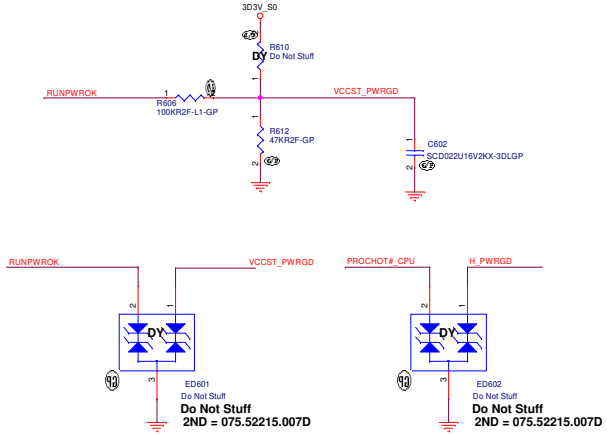
Table 6-8. Reset and Miscellaneous Signals

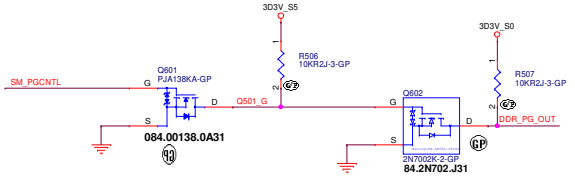
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]**: Reserved configuration lane. • **CFG[4]**: eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]**: PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]**: Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

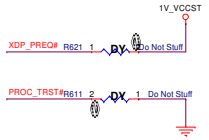
Table 13-14. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	WS1 [inches]	WS2 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to *"Power Architecture Guide"*.







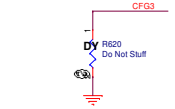
GPD11 pull high by Intel PDG1.3 request

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

eDP Enable	
CFG4	1:Disable 0:Enable

PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.

Physical_Debug_Enabled (DFX privacy)	
CFG4	1:Disable 0:Enable (Set DXF enables bit in debug)



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	$V_{CC_{IO}}$	16-60 Ω
PREQ# |	Pull Up	$V_{CC_{ST}}$	3 kΩ
PROC_TDI	Pull Up	$V_{CC_{STG}}$[1]	3 kΩ
PROC_TMS	Pull Up	$V_{CC_{SGT}}$[1]	3 kΩ
CFG[19:0]	Pull Up	$V_{CC_{IO}}$	3 kΩ

Note:
1. For SKL-S it should be $V_{CC_{ST}}$

1208

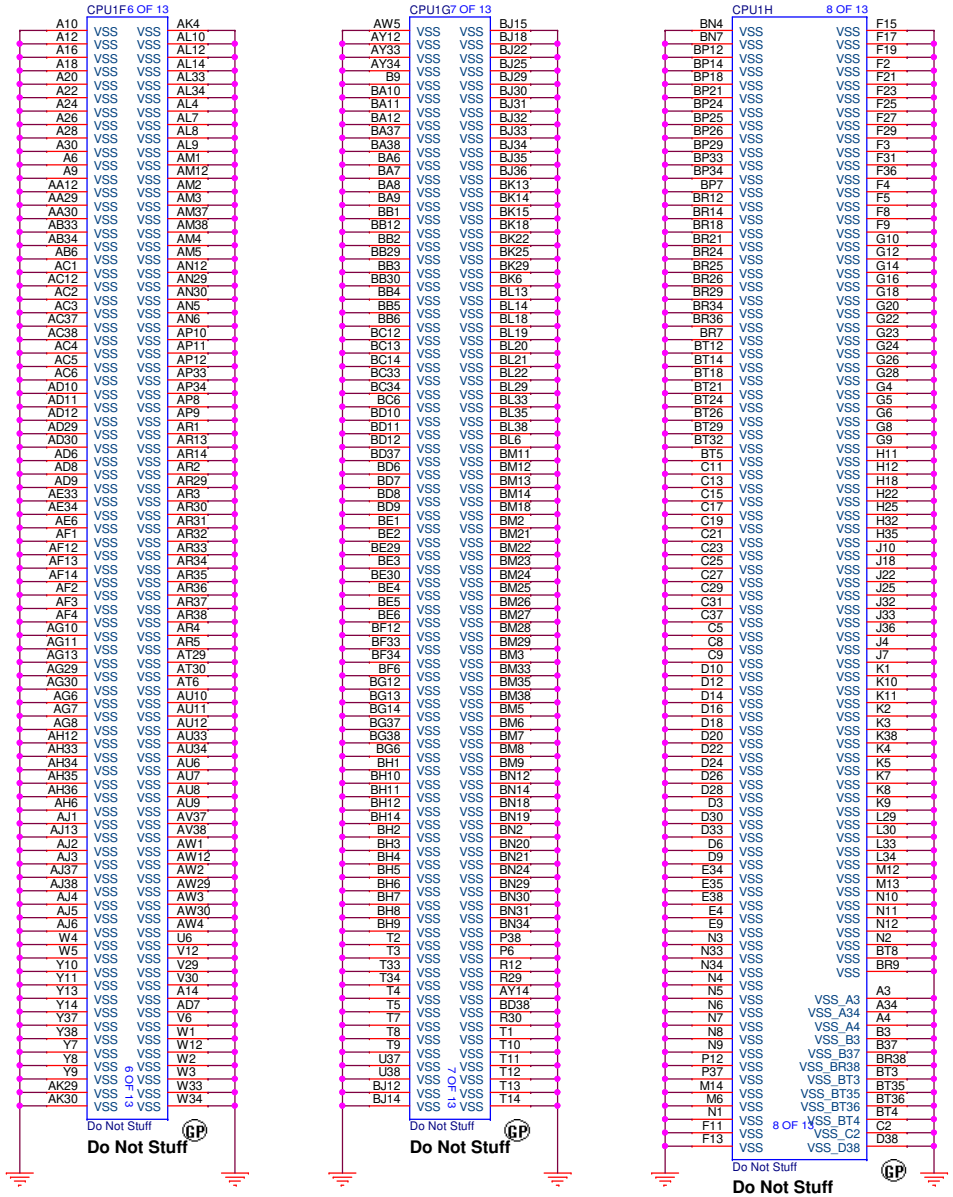
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_CFG_CFG STRAP

Size: A2 | Document Number: Selek CFL-H | Rev: A00

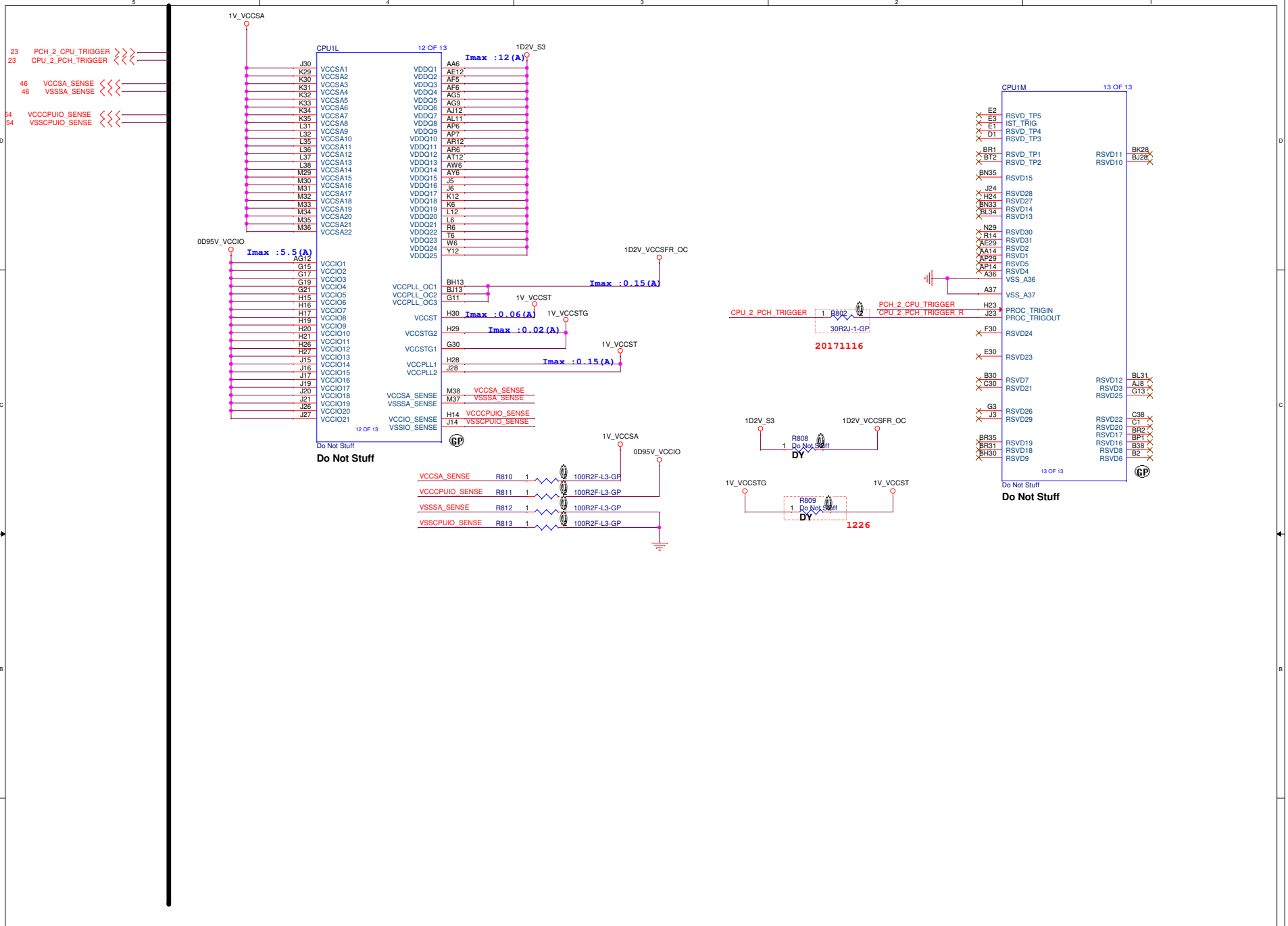
Date: Wednesday, April 03, 2019 | Sheet 6 of 105



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_GND*	
Size A3	Document Number **Selek CFL-H**	Rev **A00**
Date: Wednesday, April 03, 2019	Sheet 7 of 105	



Selek CFLH N17P

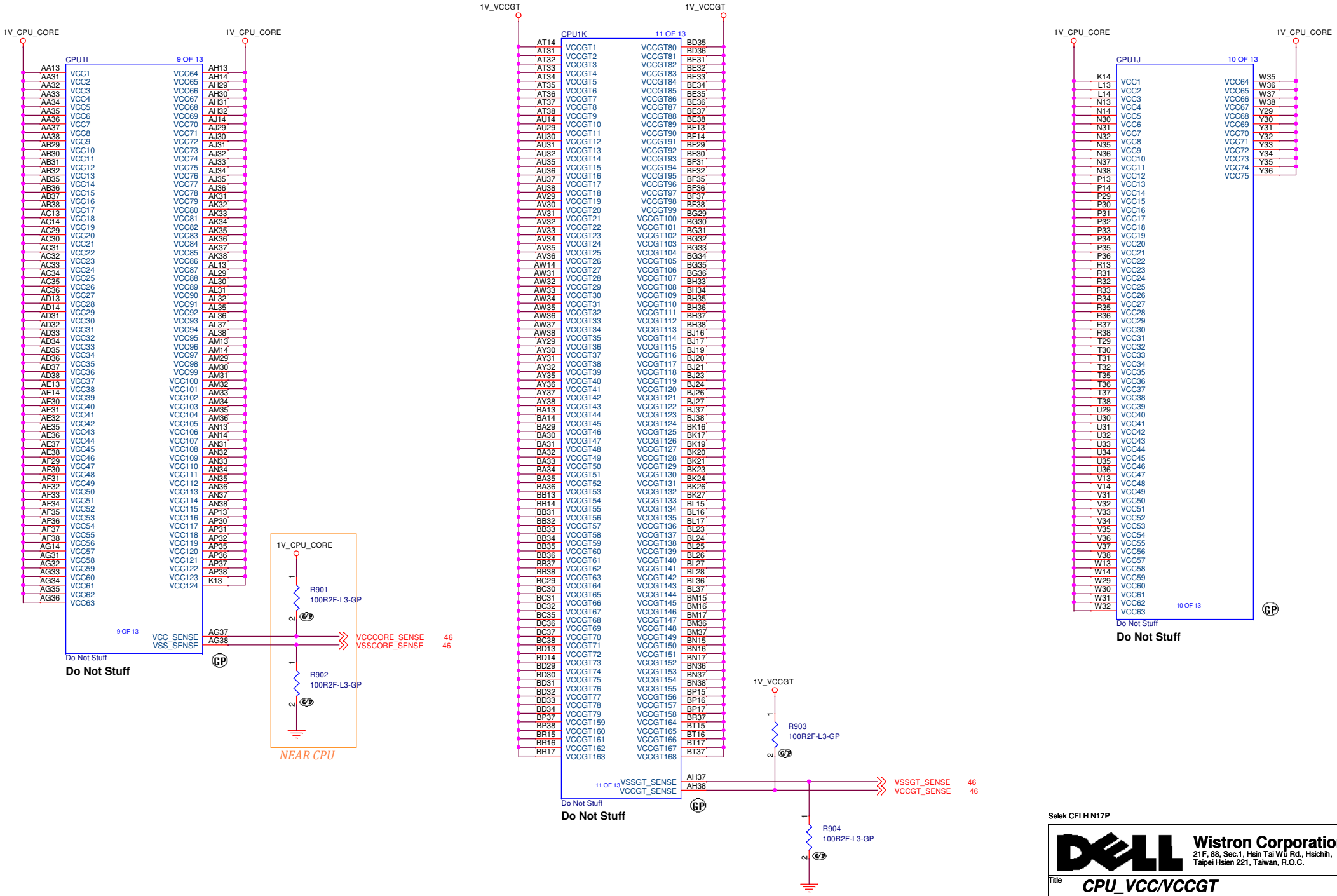
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_POWER(VCCSA/VCCIO/VDD)***

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 8 of 105

SSID = CPU



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

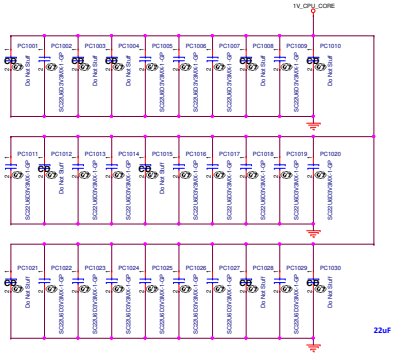
Title	*CPU_VCC/VCCGT*	
Size A3	Document Number **Selek CFL-H**	Rev **A00**
Date: Wednesday, April 03, 2019	Sheet 9 of 105	

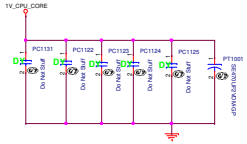
Main Func = CPU

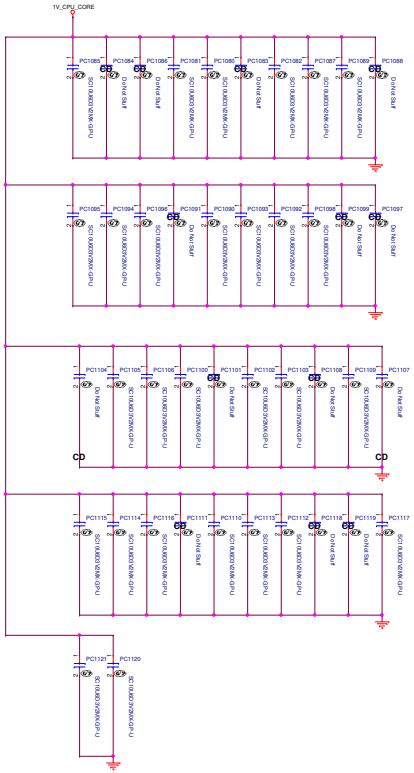
VCORE

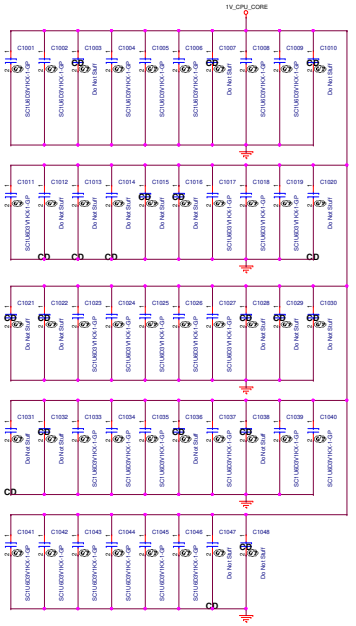
CFL-H_45W

H-line 45W
IccMax current-10ms max = 128A





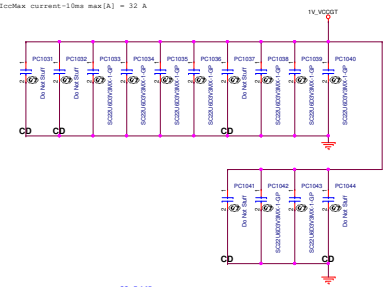


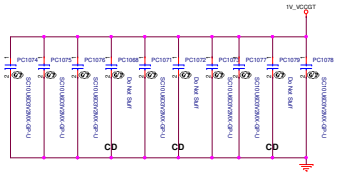


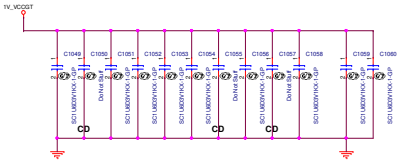
VCCGT

CFL-H_45W

IccMax current-10ms max[A] = 32 A



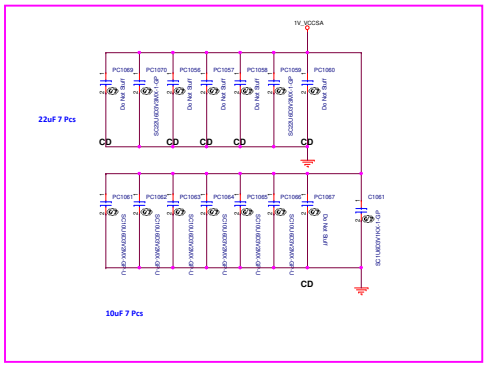


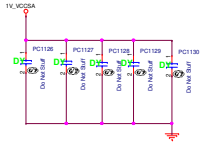


VCCSA

H-Line

IccMax current-10ms max[A] = 11.1 A





Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 10 of 105

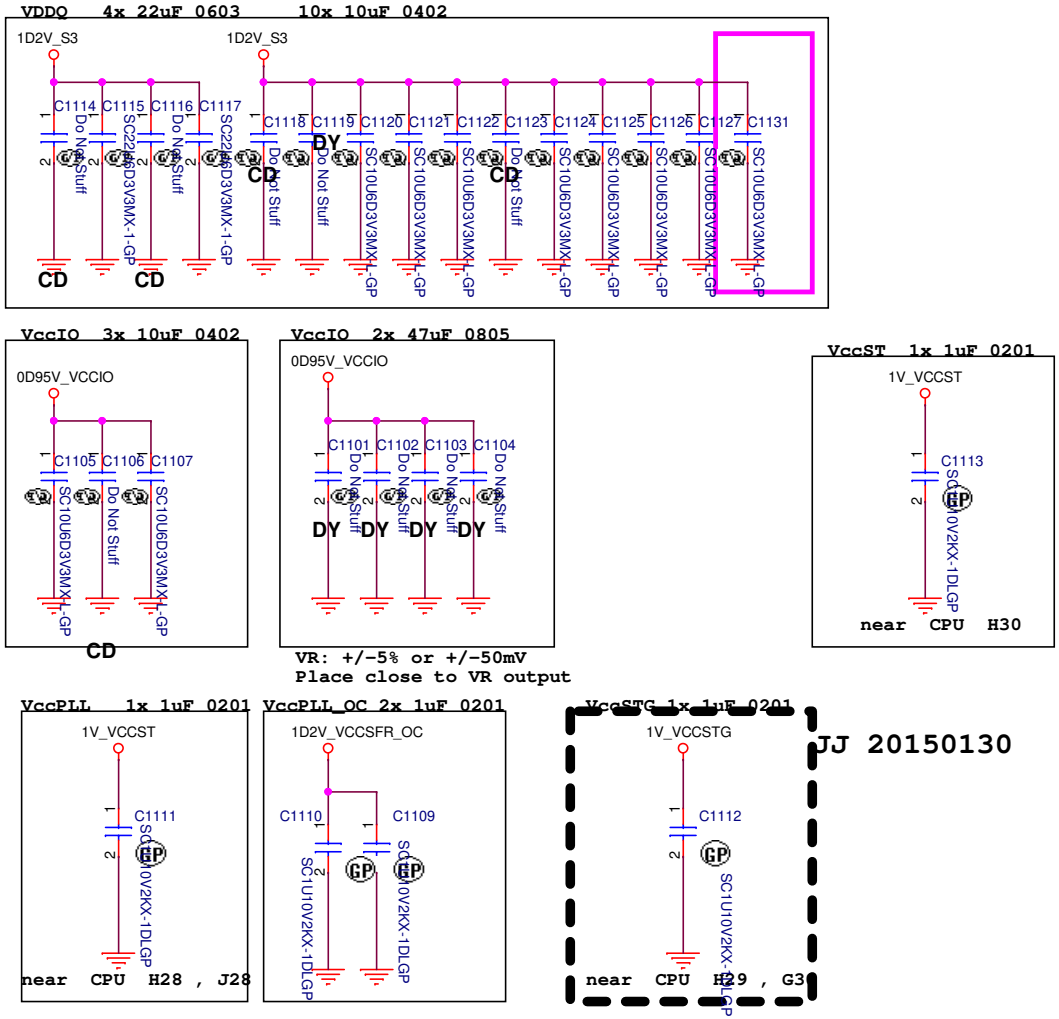


Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 1 of 2)

Domain	Board Edge cap	Backside cap	Notes
Vcc	2x 22uF 0603		
	8x 47uF 0805		
		48x 1uF 0201	
		42x 10uF 0402	
		10x 22uF 0603	
Vcc_{GT}	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
Vcc_{SA}	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
		1x 1uF 0201	
V_{DDQ}		4x 22uF 0603	
		11x 10uF 0402	
Vcc_{IO}		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
Vcc_{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail
Vcc_{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
	1x 22uF/47uF 0805 (placeholder)		*Placeholder not stuffed.* To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.

Domain	Board Edge cap	Backside cap	Notes
Vcc_{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with V_{DDQ}. Board resistance from BGA to Power gate should be less than 86mOhm.

Note: High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.

Note: It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

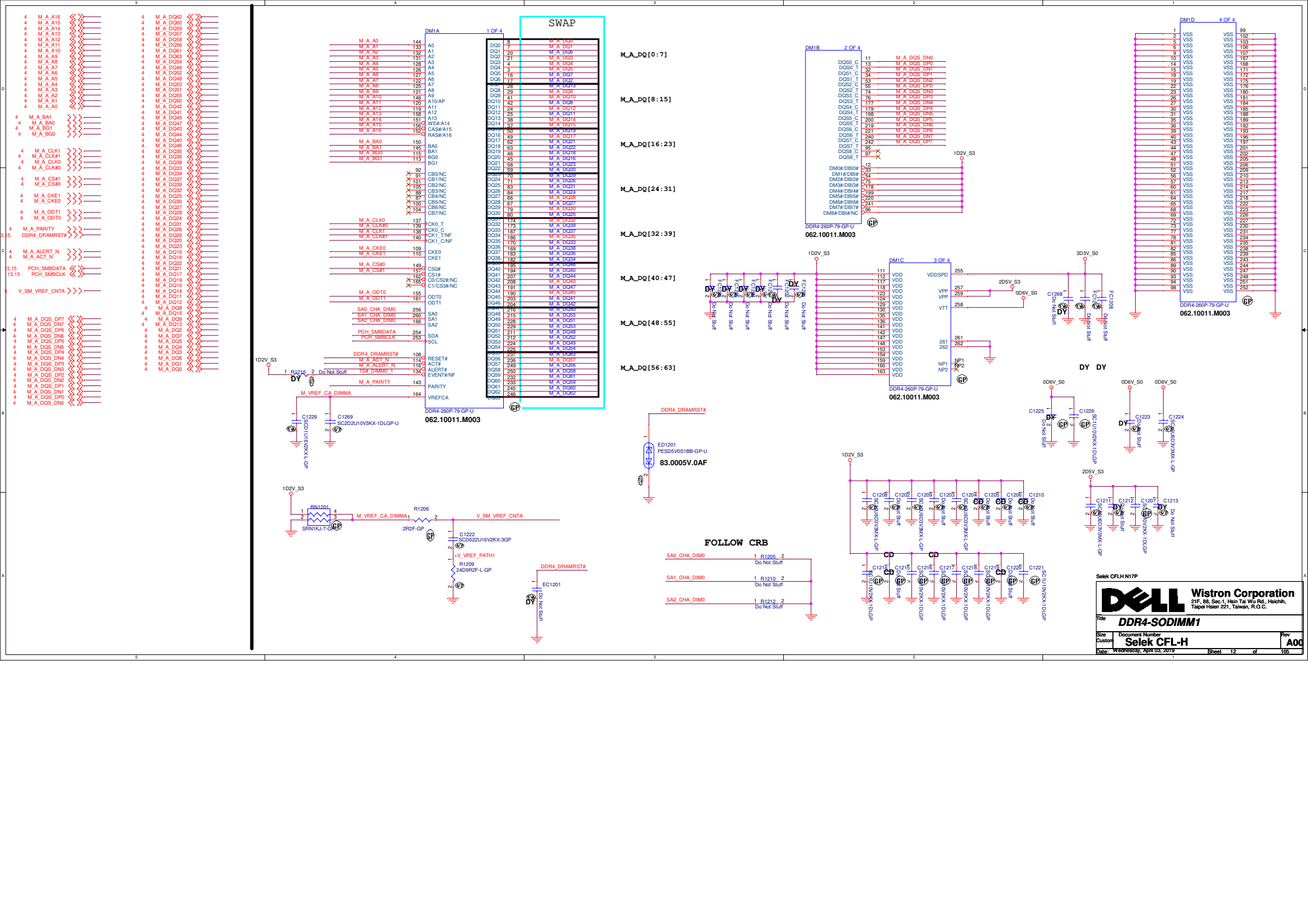
Selek CFLH N17P

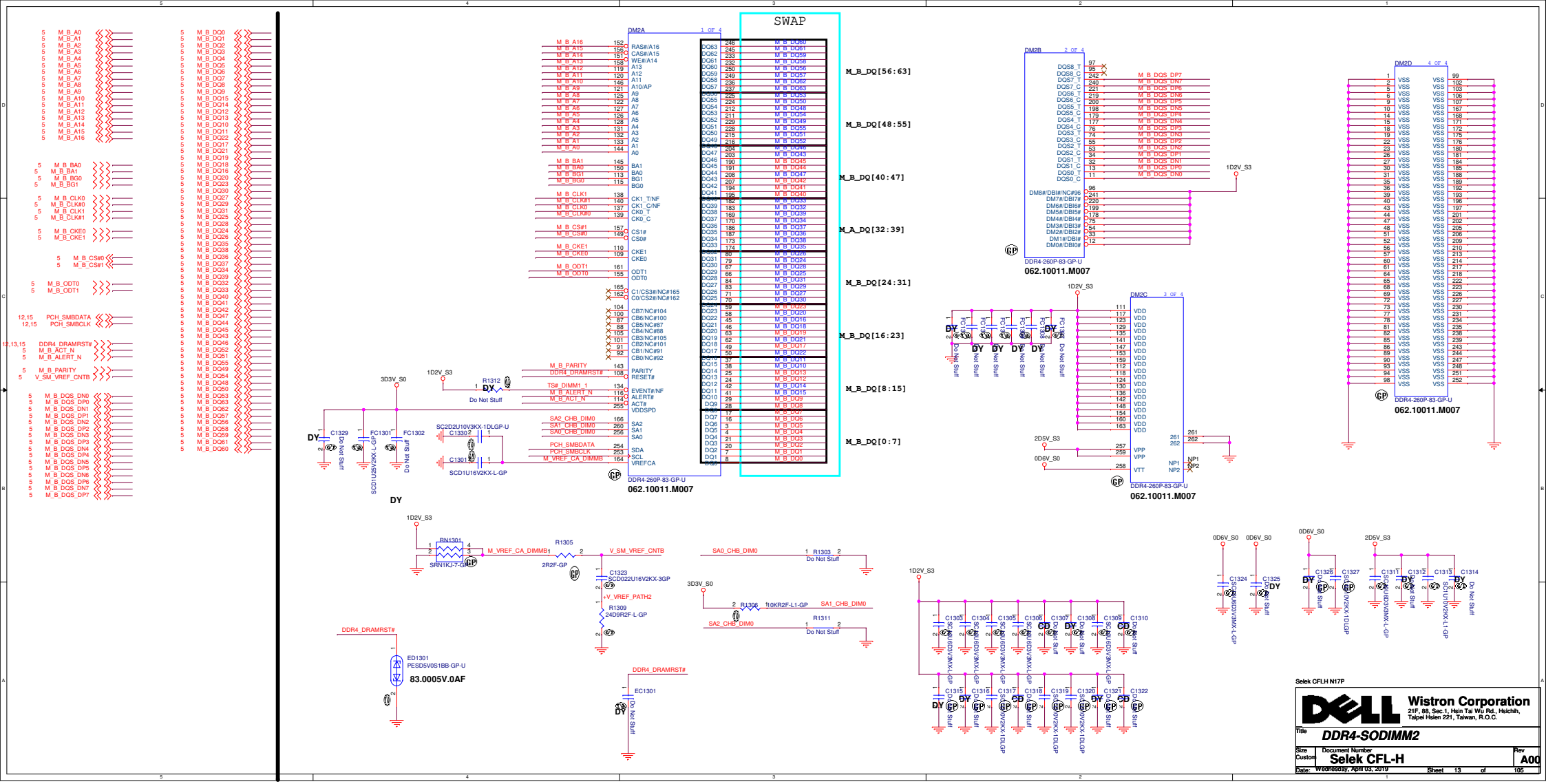
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (Power CAP2)*

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 11 of 105


SWAP
DM1A
1 OF 4
DM1B
2 OF 4
DM1C
3 OF 4
DM1D
4 OF 4
M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_A_DQ[48:55]
M_A_DQ[56:63]
DDR4-260P-79-GP-U
062.10011.M003
FOLLOW CRB
DY DY
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4-SODIMM1
Size
Custom
Document Number
Selek CFL-H
Rev
A00
Date: Wednesday, April 03, 2019
Sheet 12 of 105


SWAP
DM2A
M_B_DQ[56:63]
M_B_DQ[48:55]
M_B_DQ[40:47]
M_A_DQ[32:39]
M_B_DQ[24:31]
M_B_DQ[16:23]
M_B_DQ[8:15]
M_B_DQ[0:7]
DDR4-260P-83-GP-U
062.10011.M007
DM2B
DM2C
DM2D
1D2V_S3
3D3V_S0
2D5V_S3
0D6V_S0
DY
Do Not Stuff
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4-SODIMM2
Size
Custom
Document Number
Selek CFL-H
Rev
A00
Date: Wednesday, April 03, 2019
Sheet 13 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 14 of 105

SPI ROM

25,91 SPI_CLK_CPU
15,21,25,91 SPI_SO_CPU
15,21,25,91 SPI_SI_CPU
15,21,25 SPI_WP_CPU
15,21,25 SPI_HOLD_CPU
25 SPI_CS_ROM_N0
25 SPI_CS_ROM_N1

TPM

91 SPI_CS_CPU_N2
91 TPM_SPI_IRQ#

26,31,61,63,79,91 PLT_RST#
6 H_PWRGD
24 SIO_PWRBTN#
61 SUS_CLK
24 GC6_THM_DIS#
3 AUD_AZACPU_SDO
3 AUD_AZACPU_SDI
3 AUD_AZACPU_SCLK
6 PCH_JTAG_TMS
6 PCH_JTAG_TDO
6 PCH_JTAG_TDI
12,13 DDR4_DRAMRST#
21 CPU_SMB_ALERT#_P1
27 HDA_BITCLK_CODEC
27 HDA_SDIN0_CPU
27 HDA_SDOUT_CODEC
27 HDA_SYNC_CODEC
24 ME_FWP
55 DMIC_PCH_DATA
55 DMIC_PCH_CLK
24,31 LAN_WAKE#
21 GPP_H15
61 CNV_RF_RESET#
61 CLKREQ_CNV#

PCH Strap

21 CPU_SMB_ALERT#
21 CPU_SMB_ALERT#_P0

SIO

15,21,25 SPI_WP_CPU
15,21,25 SPI_HOLD_CPU
15,21,25,91 SPI_SI_CPU
15,21,25,91 SPI_SO_CPU

40,91 PM_SLP_S0#
27,40,54,57 PM_SLP_S3#
40,44,51,92 PM_SLP_S4#
24 PCH_WAKE_N
24,26,79 CPU_SMB_SCL_P0
24,26,79 CPU_SMB_SDA_P0
24,76,86 DGPU_PWROK
24 SYS_PWROK
24,65 TP_WAKE_KBC#
21,27 SPKR
24,26 RESET_OUT#
12,13 PCH_SMBDATA
12,13 PCH_SMBCLK
6 PCH_JTAGX
25,40,45 3V_5V_POK
24 PCH_RSMRST#
43,44 ACOK_IN_M
64 PM_RSMRST#

SPI ROM

TPM

Azalia I/F EMI Close to PCH

HDA_SDOUT_CODEC
HDA_SYNC_CODEC
EC1501 22P/50V/NPO/0402/SMT
EC1502 22P/50V/NPO/0402/SMT

EMI 1229

PCH_PLTRST#
ED1501 NZS120-4R5-R7G-GP
75.05125.07D
2nd = 075.00363.0A7D
3rd = 075.02215.007D

SMBUS

3D3V_S0
RN1503 SRN2K2J-1-GP
CPU_SMB_SDA
PCH_SMBDATA
Q1502 2N7002DW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C
CPU_SMB_SCL
PCH_SMBCLK

IntelR Display Audio Interface To CPU

Close to PCH

RTC_AUX_S5 1214

CRB pull 30.1k , but PDG use 20k
RN1507 SRN20KJ-1-GP
SRTC_RST#
C1518 1U/6.3V/X5R/0402/SMT
Q1501 2N7002DW-1-GP
C1517 1U/6.3V/X5R/0402/SMT
C1519 0.1U/25V/X7R/0402/SMT
C1520 0.1U/25V/X7R/0402/SMT

Layout: Place at the open door area

Reserve by NON DS3 function 20150413

D1501 RB521S30-GP
83.R2003.A6M
2ND = 083.S2030.008F
ACOK_IN_M
AC_PRESENT
Q1502 2N7002DW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(Audio/SMBUS/JTAG/GPIO)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 15 of 105

TO CPU CLOCK

6 PCH_CPU_BCLK_DP
6 PCH_CPU_BCLK_DN

6 PCH_CPU_PCIBCLK_DP
6 PCH_CPU_PCIBCLK_DN

6 PCH_CPU_NSSC_CLK_DP
6 PCH_CPU_NSSC_CLK_DN

31 LAN_CLK_CPU_N
31 LAN_CLK_CPU_P
31 LAN_CLKREQ_CPU_N

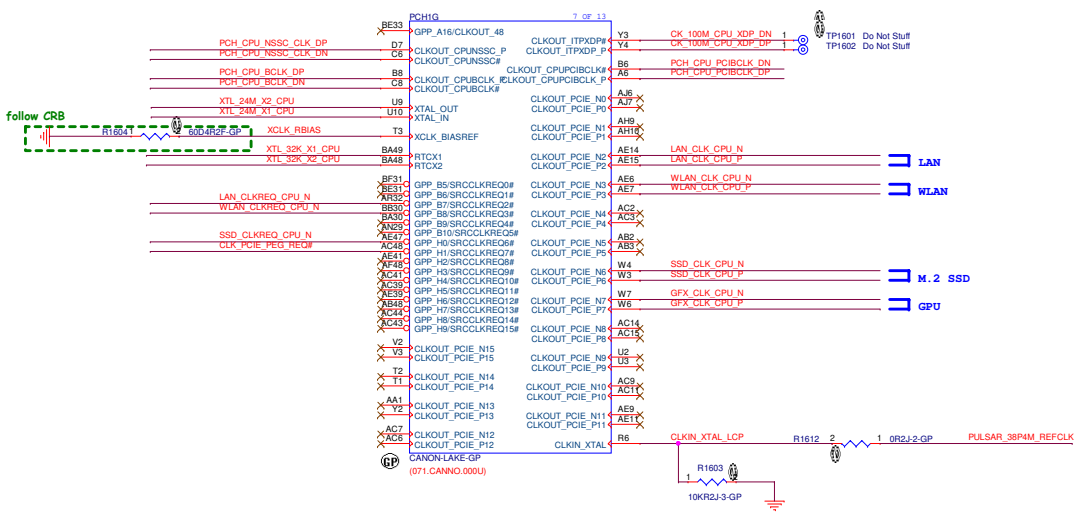
61 WLAN_CLK_CPU_N
61 WLAN_CLK_CPU_P
61 WLAN_CLKREQ_CPU_N

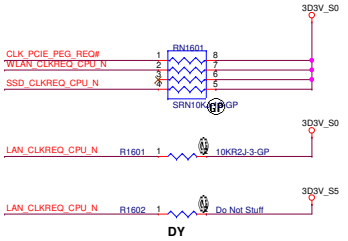
63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N

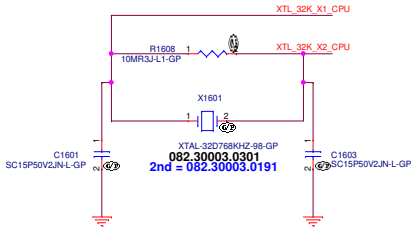
76 GFX_CLK_CPU_N
76 GFX_CLK_CPU_P
76 CLK_PCIE_PEG_REQ#

61 PULSAR_38P4M_REFCLK

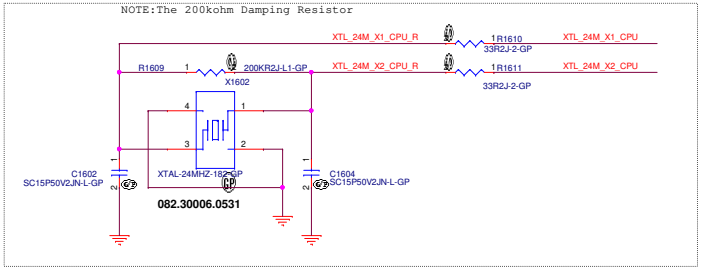
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







follow PDG
Frequecy: 32.768KHz
ESR: 50kohm
CL: 12pF



follow PDG
Frequecy: 24MHz
Series Resistance :< 30ohm MAX
CL: 12pF

24 MHz Crystal Specifications (Sheet 1 of 2)

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	

Parameter	Values	Units	Max/Min Range
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

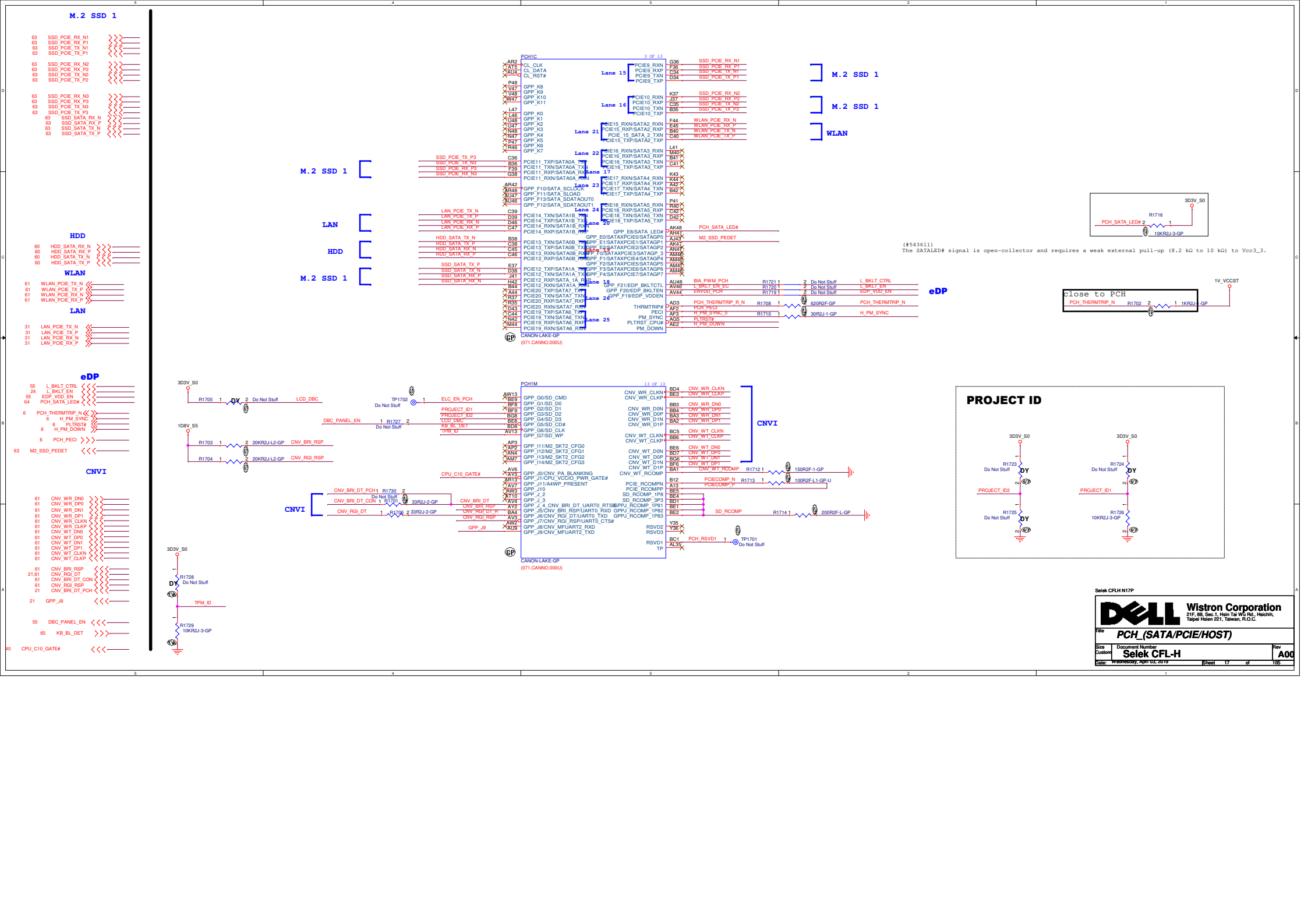
Selek CFLH N17P

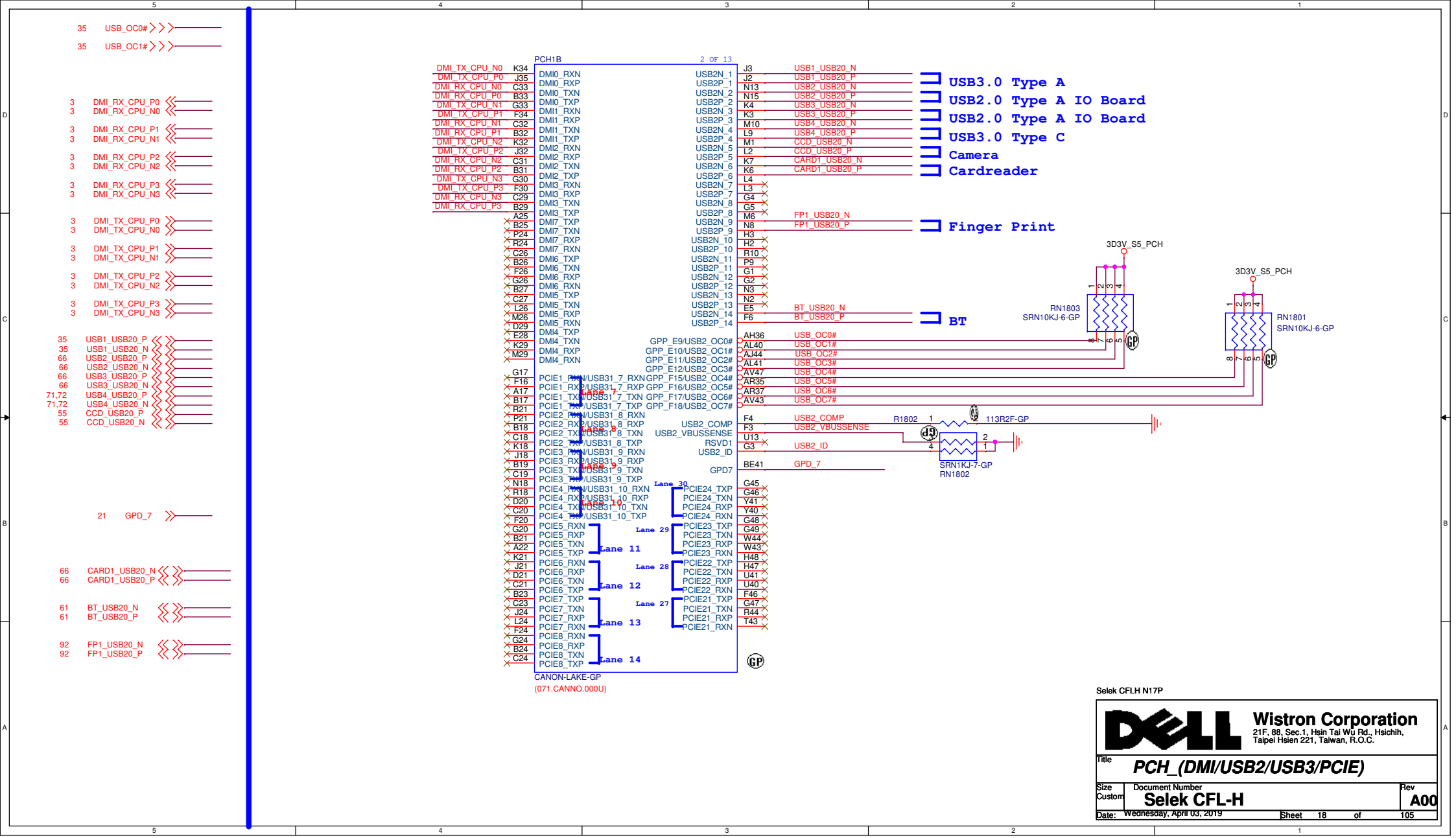
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (CLK)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 16 of 105


M.2 SSD 1
63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1
63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2
63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3
63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P
HDD
60 HDD_SATA_RX_N
60 HDD_SATA_RX_P
60 HDD_SATA_TX_N
60 HDD_SATA_TX_P
WLAN
61 WLAN_PCIE_TX_N
61 WLAN_PCIE_TX_P
61 WLAN_PCIE_RX_N
61 WLAN_PCIE_RX_P
LAN
31 LAN_PCIE_TX_N
31 LAN_PCIE_TX_P
31 LAN_PCIE_RX_N
31 LAN_PCIE_RX_P
eDP
55 L_BKLT_CTRL
24 L_BKLT_EN
55 EDP_VDD_EN
64 PCH_SATA_LED#
6 PCH_THERMTRIP_N
6 H_PM_SYNC
6 PLTRST#
6 H_PM_DOWN
6 PCH_PECI
63 M2_SSD_PEDET
CNVI
61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1
61 CNV_WR_CLKN
61 CNV_WR_CLKP
61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1
61 CNV_WT_CLKN
61 CNV_WT_CLKP
61 CNV_BRI_RSP
21,61 CNV_RGI_DT
61 CNV_BRI_DT_CON
61 CNV_RGI_RSP
21 CNV_BRI_DT_PCH
21 GPP_J9
55 DBC_PANEL_EN
65 KB_BL_DET
40 CPU_C10_GATE#
PCH1C
3 OF 13
CANON-LAKE-GP
(071.CANNO.000U)
Lane 15
Lane 16
Lane 21
Lane 22
Lane 17
Lane 23
Lane 24
Lane 20
Lane 18
Lane 26
Lane 25
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
LAN_PCIE_TX_N
LAN_PCIE_TX_P
LAN_PCIE_RX_N
LAN_PCIE_RX_P
HDD_SATA_TX_N
HDD_SATA_TX_P
HDD_SATA_RX_N
HDD_SATA_RX_P
SSD_SATA_TX_P
SSD_SATA_TX_N
SSD_SATA_RX_P
SSD_SATA_RX_N
PCH_SATA_LED#
M2_SSD_PEDET
BIA_PWM_PCH
L_BKLT_EN_EC
EDVDD_PCH
PCH_THERMTRIP_R_N
PCH_PECI
H_PM_SYNC_0
PLTRST#
H_PM_DOWN
R1721 Do Not Stuff L_BKLT_CTRL
R1720 Do Not Stuff L_BKLT_EN
R1719 Do Not Stuff EDP_VDD_EN
R1708 620R2F-GP PCH_THERMTRIP_N
R1710 30R2J-1-GP H_PM_SYNC
M.2 SSD 1
M.2 SSD 1
WLAN
LAN
HDD
M.2 SSD 1
eDP
3D3V_S0
R1716
PCH_SATA_LED#
10KR2J-3-GP
(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.
1V_VCCST
Close to PCH
PCH_THERMTRIP_N
R1702 1KR2J-GP
3D3V_S0
R1705 DY Do Not Stuff LCD_DBC
1D8V_S5
R1703 20KR2J-L2-GP CNV_BRI_RSP
R1704 20KR2J-L2-GP CNV_RGI_RSP
TP1702 Do Not Stuff
ELC_EN_PCH
PROJECT_ID1
PROJECT_ID2
LCD_DBC
KB_BL_DET
TPM_ID
DBC_PANEL_EN
R1727 Do Not Stuff
CPU_C10_GATE#
CNV_BRI_DT_PCH R1730 Do Not Stuff
CNV_BRI_DT_CON R1701 33R2J-2-GP CNV_BRI_DT
CNV_RGI_DT R1706 33R2J-2-GP CNV_RGI_DT
CNV_BRI_RSP
CNV_RGI_DT_R
CNV_RGI_RSP
GPP_J9
PCH1M
13 OF 13
CANON-LAKE-GP
(071.CANNO.000U)
CNVI
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WR_DN0
CNV_WR_DP0
CNV_WR_DN1
CNV_WR_DP1
CNV_WT_CLKN
CNV_WT_CLKP
CNV_WT_DN0
CNV_WT_DP0
CNV_WT_DN1
CNV_WT_DP1
CNV_WT_RCOMP
R1712 150R2F-1-GP
PCIECOMP_N R1713 100R2F-L1-GP-U
PCIECOMP_P
SD_RCOMP R1714 200R2F-L-GP
PCH_RSVD1 TP1701 Do Not Stuff
3D3V_S0
R1728 DY Do Not Stuff
TPM_ID
R1729 10KR2J-3-GP
PROJECT ID
3D3V_S0
R1723 Do Not Stuff DY
PROJECT_ID2
R1725 Do Not Stuff DY
3D3V_S0
R1724 Do Not Stuff DY
PROJECT_ID1
R1726 10KR2J-3-GP
Selek CFLH N17P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH_(SATA/PCIE/HOST)
Size Custom
Document Number
Selek CFL-H
Rev
A00
Date: Wednesday, April 03, 2019
Sheet 17 of 105



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH_(DMI/USB2/USB3/PCIE)***

Size	Document Number	Rev
Custom	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 18 of 105

91 PIRQA#

19,60 HDD_DEVSLP

71,72 CPU_DP_HPD_R

55 EDP_HPD

19,60 HDD_DEVSLP

19,63 mSATA_DEVSLP

19,63 mSATA_DEVSLP

24,68 ESPI_IO[3..0]

35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB30_RX_N
35 USB1_USB30_RX_P

71 USB4_USB30_TX_N
71 USB4_USB30_TX_P
71 USB4_USB30_RX_N
71 USB4_USB30_RX_P

24,68 ESPI_CS#

24,68 ESPI_RESET#

24,68 ESPI_CLK

3D3V_S0

CPU_DP_CTRL_CLK
CPU_DP_CTRL_DATA
RN2011
SRN2K2J-1-GP

Add RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH
R1906 10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
R1905 10KR2J-3-GP
RTC_RST
Q1901
CPU_DDI1HPD
CPU_DP_HPD_R
CPU_DP_HPD_P
RTC_RST
common part
2N7002KDW-3-GP
75.27002.F7C
2nd = 075.27002.0E7C
R1907 Do Not Stuff
DY

CPU_DDI1HPD
R1902 100KR2J-1-GP

PCH1E 5 OF 13
CPU_DDI1HPD AT6 GPP_I0/DDPB_HPD0/DISP_MISC0
AN10 GPP_I1/DDPC_HPD1/DISP_MISC1
AP9 GPP_I2/DPPD_HPD2/DISP_MISC2
AL15 GPP_I3/DPPE_HPD3/DISP_MISC3
EDP_HPD AN6 GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK AL13 CPU_DP_CTRL_CLK
GPP_I6/DDPB_CTRLDATA AR8 CPU_DP_CTRL_DATA
GPP_I7/DDPC_CTRLCLK AN13
GPP_I8/DDPC_CTRLDATA AL10
GPP_I9/DDPD_CTRLCLK AL9
GPP_I10/DDPD_CTRLDATA AR3
GPP_F23/DDPF_CTRLDATA AN40 PCIAUX_GATE
GPP_F22/DDPF_CTRLCLK AT49
GPP_F14/EXT_PWR_GATE#/PS_ON# AP41 PROC_DETECT#
GPP_K23/IMGCLKOUT1 M45
GPP_K22/IMGCLKOUT0 L48
GPP_K21 T45
GPP_K20 T46
GPP_H23/TIME_SYNC0 AJ47
CANON-LAKE-GP
(071.CANNO.000U)
TP1901 Do Not Stuff

6.3.3 Embedded DisplayPort* Hot-Plug Detect Implementation

Hot-plug detect (HPD) is an output from eDP* sink device and it is a active high signal.

Note: When using eDP bifurcation for DP-VGA Topology, need to use HPD for DDIE (DDPE_HPD) for HPD connectivity.

For eSPI

ESPI_IO[3..0]
ESPI_IO0 R1921 15R2F-2-GP ESPI_IO0_R
ESPI_IO1 R1922 15R2F-2-GP ESPI_IO1_R
ESPI_IO2 R1923 15R2F-2-GP ESPI_IO2_R
ESPI_IO3 R1924 15R2F-2-GP ESPI_IO3_R

3D3V_S5_PCH 1214
PROC_DETECT# R1920 20KR2J-L2-GP

3D3V_S0
PIRQA# R19111 10KR2J-3-GP
ESPI_ALERT1# R1912 DY Do Not Stuff

ESPI_RESET# R1919 DY Do Not Stuff

USB3.0 Type A

USB3.0 Type C(for N18P)

PCH1F 6 OF 13
USB1_USB30_TX_N F9 USB31_1_TXN
USB1_USB30_TX_P F7 USB31_1_TXP
USB1_USB30_RX_N D11 USB31_1_RXN
USB1_USB30_RX_P C11 USB31_1_RXP
Lane 1
C3 USB31_2_TXN
D4 USB31_2_TXP
B9 USB31_2_RXN
C9 USB31_2_RXP
Lane 2
C17 USB31_6_TXN
C16 USB31_6_TXP
G14 USB31_6_RXN
F14 USB31_6_RXP
Lane 6
C15 USB31_5_TXN
B15 USB31_5_TXP
J13 USB31_5_RXN
K13 USB31_5_RXP
Lane 5
G12 USB31_3_TXP
F11 USB31_3_TXN
C10 USB31_3_RXP
B10 USB31_3_RXN
Lane 3
USB4_USB30_TX_P C14 USB31_4_TXP
USB4_USB30_TX_N B14 USB31_4_TXN
USB4_USB30_RX_P J15 USB31_4_RXP
USB4_USB30_RX_N K16 USB31_4_RXN
Lane 4
CANON-LAKE-GP
(071.CANNO.000U)

GPP_A1/LAD0/ESPI_IO0 BB39 ESPI_IO0_R
GPP_A2/LAD1/ESPI_IO1 AW37 ESPI_IO1_R
GPP_A3/LAD2/ESPI_IO2 AV37 ESPI_IO2_R
GPP_A4/LAD3/ESPI_IO3 BA38 ESPI_IO3_R
GPP_A5/LFRAME#/ESPI_CS0# BE38 ESPI_CS#
GPP_A6/SERIRQ/ESPI_CS1# AW35
GPP_A7/PIRQA#/ESPI_ALERT0# BA36 PIRQA#
GPP_A0/RCIN#/ESPI_ALERT1# BE39 ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET# BF38 ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK BB36 ESPI_CLK_R
GPP_A10/CLKOUT_LPC1 BB34
GPP_K19/SMI# T48
GPP_K18/NMI# T47
GPP_E6/SATA_DEVSLP2 AH40
GPP_E5/SATA_DEVSLP1 AH38 mSATA_DEVSLP
GPP_E4/SATA_DEVSLP0 AL48 HDD_DEVSLP
GPP_F9/SATA_DEVSLP7 AP47
GPP_F8/SATA_DEVSLP6 AN37
GPP_F7/SATA_DEVSLP5 AN46
GPP_F6/SATA_DEVSLP4 AR41
GPP_F5/SATA_DEVSLP3 AP48

ESPI_CLK_R R1914 33R2F-3-GP ESPI_CLK
DY Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(DDI/USB3/GPIO)
Size: Custom | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 19 of 105

79,86 GC6_FB_EN
79 GPU_EVENT#
25 RTC_DET#_PCH
24 SIO_EXT_WAKE#
29 SPK_ID
65 KB_DET#
57,77 HDMI_HPD_GPU
68 UART_2_CTXD_DRXD
68 UART_2_CRXD_DTXD
61 BT_RADIO_DIS#

TOUCH PAD

65,66 CPU_I2C_SCL_P1
65,66 CPU_I2C_SDA_P1
24 TABLE_MODE#
79 DGPU_HOLD_RST#
61 WLAN_WIGIG60GHZ_DIS#
86 DGPU_PWR_EN
61 CNV_DET#

70 GSEN2_INT1_C
70 GSEN2_INT2_C
70 CPU_I2C_SDA_ISH
70 CPU_I2C_SCL_ISH

PCH1K 11 OF 13

BBS_BIT0 — BA26 GPP_B22/GSPI1_MOSI
SIO_EXT_SCI# — BD30 GPP_B21/GSPI1_MISO
NRB_BIT — AU26 GPP_B20/GSPI1_CLK
AW26 GPP_B19/GSPI1_CS0#
BE30 GPP_B18/GSPI0_MOSI
GC6_FB_EN — R2046 Do Not Stuff — GC6_FB_EN_MCP — BD29 GPP_B17/GSPI0_MISO
GPU_EVENT# — BB26 GPP_B16/GSPI0_CLK
BF29 GPP_B15/GSPI0_CS0#
SPK_ID — BB24 GPP_C9/UART0_TXD
BT_RADIO_DIS# — BE23 GPP_C8/UART0_RXD
AP24 GPP_C11/UART0_CTS#
BA24 GPP_C10/UART0_RTS#
HDMI_HPD_GPU — R2031 Do Not Stuff — HDMI_HPD_PCH — BD21 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
AW24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AP21 GPP_C13/UART1_TXD/ISH_UART1_TXD
AU24 GPP_C12/UART1_RXD/ISH_UART1_RXD
SIO_EXT_WAKE# — AV21 GPP_C23/UART2_CTS#
UART_2_CTXD_DRXD — AW21 GPP_C22/UART2_RTS#
UART_2_CRXD_DTXD — BE20 GPP_C21/UART2_TXD
BD20 GPP_C20/UART2_RXD
CPU_I2C_SCL_P1 — BE21 GPP_C19/I2C1_SCL
CPU_I2C_SDA_P1 — BF21 GPP_C18/I2C1_SDA
BC22 GPP_C17/I2C0_SCL
BF23 GPP_C16/I2C0_SDA
BE15 GPP_D4/ISH_I2C2_SDA/I2C3_SDA/SBK4_BK4
BE14 GPP_D23/ISH_I2C2_SCL/I2C3_SCL

BA20 GPP_D9/ISH_SPI_CS#/GSPI2_CS0#
BB20 GPP_D10/ISH_SPI_CLK/GSPI2_CLK — DGPU_HOLD_RST#
BB16 GPP_D11/ISH_SPI_MISO/GP_BSSB_CLK/GSPI2_MISO — WLAN_WIGIG60GHZ_DIS#
AN18 GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI — DGPU_PWR_EN
BE14 GPP_D16/ISH_UART0_CTS#/CNV_WCEN
AR18 GPP_D15/ISH_UART0_RTS#/GSPI2_CS1#/CNV_WFEN
BF17 GPP_D14/ISH_UART0_TXD/I2C2_SCL
BE17 GPP_D13/ISH_UART0_RXD/I2C2_SDA — RTC_DET#_PCH
AG45 GPP_H20/ISH_I2C0_SCL — CPU_I2C_SCL_ISH0 — R2058 FFS Do Not Stuff — CPU_I2C_SCL_ISH
AH46 GPP_H19/ISH_I2C0_SDA — CPU_I2C_SDA_ISH0 — R2059 FFS Do Not Stuff — CPU_I2C_SDA_ISH
AH47 GPP_H22/ISH_I2C1_SCL
AH48 GPP_H21/ISH_I2C1_SDA
AV34 GPP_A23/ISH_GP5 — TABLE_MODE#_PCH — R2062 FFS Do Not Stuff — TABLE_MODE#
AW32 GPP_A22/ISH_GP4
BA32 GPP_A21/ISH_GP3 — KB_DET#
BE34 GPP_A20/ISH_GP2 — GSEN2_INT2_ISH — R2061 FFS Do Not Stuff — GSEN2_INT2_C
BD34 GPP_A19/ISH_GP1 — GSEN2_INT1_ISH — R2060 FFS Do Not Stuff — GSEN2_INT1_C
BF35 GPP_A18/ISH_GP0
BD38 GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7

CANON-LAKE-GP
(071.CANNO.000U)

1D8V_S5
KB_DET# — R2045 10KR2J-3-GP
TABLE_MODE#_PCH — R2016 DY Do Not Stuff
DGPU_HOLD_RST# — R2013 10KR2F-L1-GP

1D8V_S0
DGPU_PWR_EN — R2014 10KR2F-L1-GP
R2057 DY Do Not Stuff

BBS_BIT0 — R2015 DY Do Not Stuff

TOUCH PAD

3D3V_S5_PCH
R2041 10KR2J-3-GP — SIO_EXT_WAKE#
R2042 10KR2J-3-GP — GPU_EVENT#

3D3V_S0
R2001 10KR2J-3-GP — SIO_EXT_SCI#
RN2010 DY Do Not Stuff — CPU_I2C_SCL_P1 / CPU_I2C_SDA_P1
RN2007 FFS Do Not Stuff — CPU_I2C_SCL_ISH0 / CPU_I2C_SDA_ISH0
51KR2J-1-GP DEBUG — R2056 — UART_2_CRXD_DTXD
51KR2J-1-GP DEBUG — R2055 — UART_2_CTXD_DRXD

UART_2_CRXD_DTXD — R2030 DY Do Not Stuff — CNV_DET#

Assign CNV_DET# for reserved

PHASE ID

3D3V_S0
R2050 DY Do Not Stuff — BOARD_ID_2
R2049 DY Do Not Stuff

3D3V_S0
R2051 DY Do Not Stuff — BOARD_ID_1
R2048 DY Do Not Stuff

1D8V_S0
R2002 FFS Do Not Stuff
TABLE_MODE#_PCH

1D8V_S0
Q2001 FFS Do Not Stuff
G / S / D

3D3V_S0
R2003 FFS Do Not Stuff — TABLE_MODE#

3D3V_S5_PCH
1214
R2047 DY Do Not Stuff — NRB_BIT
R2019 DY Do Not Stuff

R2052 100KR2J-1-GP — HDMI_HPD_PCH

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

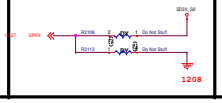
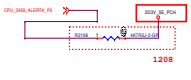
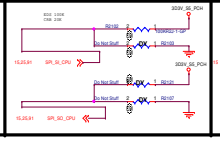
Title: PCH_(UART/GPIO/I2C)

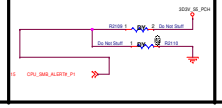
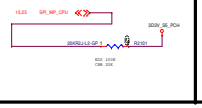
Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 20 of 105

571182-cnl-pch-eds-h-vol1of2-rev2p1

CRB P.103 P.104

GPIO	GPP_B14 SPKR	GPP_B18 GSPIO_MOSI	GPP_C2 SMBALERT#	GPP_B22 GSPI1_MOSI	GPP_C5 SM0ALERT#	SPI0_MOSI SPI0_MISO	GPP_H15 SML3ALERT#
Schematic		default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side			

GPIO	GPP_B23 SML1ALERT# PCHHOT#	SPI0_IO2	SPI0_IO3	HDA_SDO/ I2S0_TXD	GPP_H12 SML2ALERT#	GPP_I6 DDPB_CTRLDATA	GPP_I8 DDPC_CTRLDATA
Schematic					internal pull down	Pull high at page 19	internal pull down

need check the latest CRB,PDG

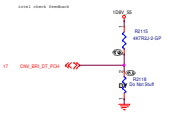
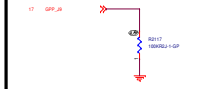
GPIO	GPP_I10	GPP_F23/ DPPF_CTRLDATA	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_J9	GPD7	
Schematic		internal pull down					

Table 9-1. Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address bit which selects the BIOS image such that the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate equivalent SPI or LPC cycles. The A16 is selected in Top Swap Block size soft strap. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DC5, bit 4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel® ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel® ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel® AMT with TLS. **Notes:** 1. The internal pull-down is disabled after RSMRST# is de-asserted. 2. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
GPP_B22 / GSPI1_MOSI	Boot BIOS Destination	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DC5, bit 6). Bit 6 — Boot BIOS Destination 1 — SPI (default) 0 — LPC **Notes:** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If "Boot BIOS Destination" is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC is functional only for debug purposes. Production systems will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SM0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: If the strap is configured to '0' (eSPI Flash Sharing Mode) and no Flash Sharing mode strap must be configured to '0' (eSPI is configured to '0').
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull up is required. Recommend 1K ohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	External pull up is required. Recommend 1K ohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2 / SML1ALERT# / PCHHOT#	eSPI (EC Used)	Rising edge of RSMRST#	External pull up is required. Recommend 20K ohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH if eSPI is enabled in order to disable Intel® Flash Descriptor Security Override strap. This strap should only be asserted High using external Pull-up in manufacturing/debug environments ONLY. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull up is required. Recommend 20K ohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull up is required. Recommend 1K ohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Intel® Flash Descriptor Security Override. This strap should only be asserted High using external Pull-up in manufacturing/debug environments ONLY. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_H12 / SML2ALERT#	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. **Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is enabled).**
GPP_J0 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_J1 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-Down. 0 = Port C is not detected. (Default) 1 = Port C is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
ITP_PMODE	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Signal	Usage	When Sampled	Comment
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. **Notes:** 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. Platforms that do not support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	A weak external pull-up is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. **Note:** When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down must be overcome and pull the strap load to enable CNVi interface.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

Selek CFL-H/H17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
New Taipei City, Taiwan, R.O.C.

PCH_(Strap Pin)

Size: Document Number: Rev: A00
Custom: Selek CFL-H
Date: Wednesday, April 03, 2019 Sheet 35 of 55

VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.

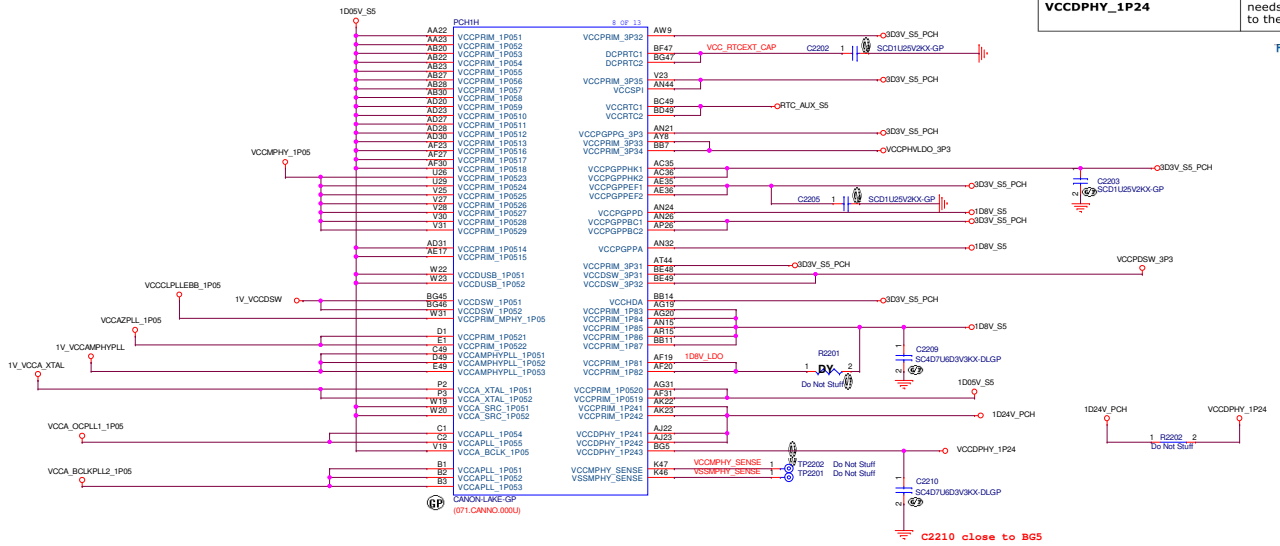
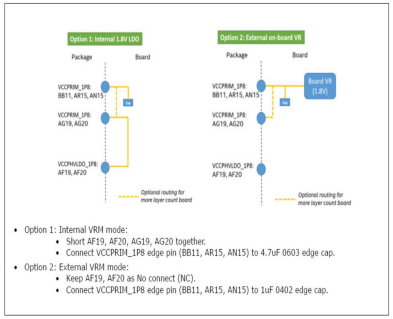
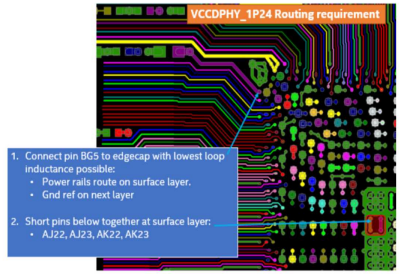


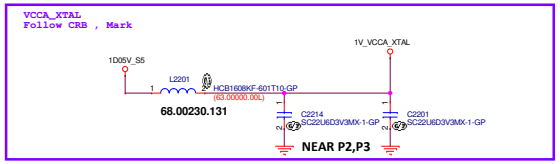
Figure 50-9. CFL PCH-H Power Rail VRM Recommendations

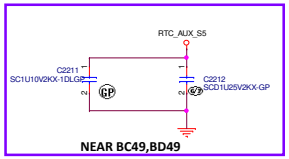


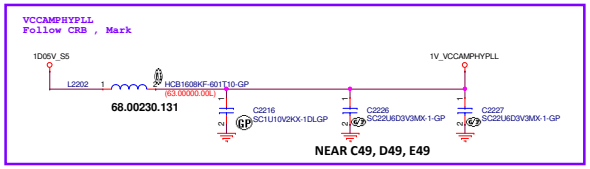
- Option 1: Internal VRM mode:
  - Short AF19, AF20, AG19, AG20 together.
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 4.7uF 0603 edge cap.
- Option 2: External VRM mode:
  - Keep AF19, AF20 as No connect (NC).
  - Connect VCCPRIM_1P8 edge pin (BB11, AR15, AN15) to 1uF 0402 edge cap.

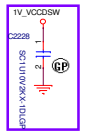
CFL PCH-H VCCDPHY_1P24 Routing

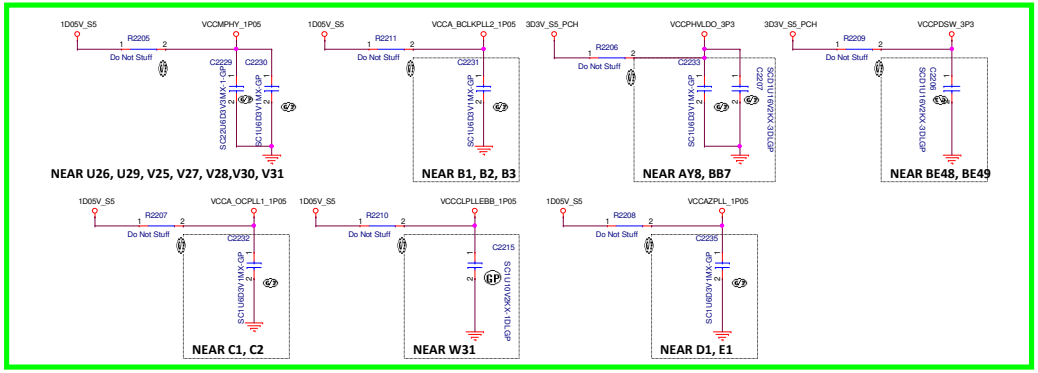








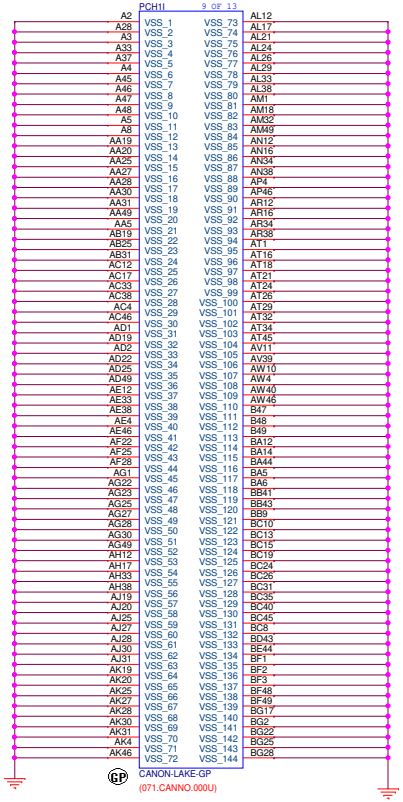


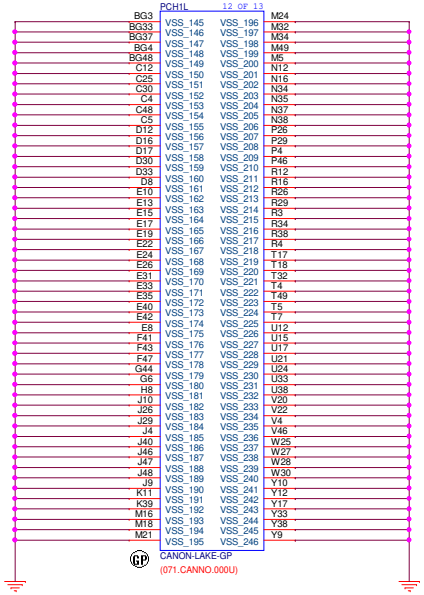


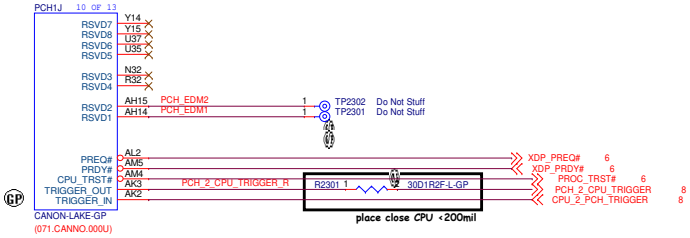
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_POWER		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 22 of 105	







Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS/GPIO)

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 23 of 105

Main Func = KBC

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	ULL-HIGH RESISTO	VOLTAGE
1	Nivida-N17P-G0-K1	100.0K	**10.0K**	3
2		100.0K	**17.8K**	2.801
3	Nivida-N18P-G0	100.0K	**27.0K**	2.598
4		100.0K	**37.4K**	2.402
5	Nivida-N18E-G0	100.0K	**49.9K**	2.201
6		100.0K	**64.9K**	2.001
7	Nivida-N18E-G1	100.0K	**82.5K**	1.808
8		100.0K	**107K**	1.594
9		100.0K	**154K**	1.299
10		100.0K	**200K**	1.1
11	Reserve	100.0K	**TBD**	0.9
12	Reserve	100.0K	**TBD**	0.7
13	Reserve	100.0K	**TBD**	0.5
14	Reserve	100.0K	**TBD**	0.3

Layout Note:
Need very close to EC

X01 20161227 change

BATTER /CHARGER

CPU/ GPU/ Thermal
For I2C/USB Mux

Need very close to EC,
PDG: <0.5 inches.

071.01416.000G

ALL_SYS_PWRGD (RUNPWROK)assert,
delay 10ms; PCH_PWROK (RESET_OUT#)assert.

082.30003.0301
2nd = 082.30003.0191

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

75.02054.A7D

DEBUG
20.K0691.006

For eSPI

GPIO102 (CR_STRAP) GPIO123 (BSS_STRAP)

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

EC LCD test

For USB TypeC

For CCG5

Need check

Follow EV project circuit DY Q2417 (RO13_20171026)

Power Switch Logic(PSL)

84.2N702.J31
2ND = 084.27002.0N31

EMI 1229

Do Not Stuff
2ND = 83.0005V.0AF

75.27002.F7C
2nd = 075.67002.007C
3rd = 075.06S01.007C

84.2N702.J31
2ND = 084.27002.0N31

180118

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

KBC MEC1416

Size	Document Number	Rev
A1	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 24 of 105

SSID = Flash.ROM

SPI FLASH ROM (32M byte) for PCH

15 SPI_CS_ROM_N0
15,21,91 SPI_SO_CPU
15,21 SPI_WP_CPU
15,21 SPI_HOLD_CPU
15,91 SPI_CLK_CPU
15,21,91 SPI_SI_CPU
15 SPI_CS_ROM_N1

3D3V_S5_PCH
C2501 SC10U6D3V3MX-DL-GP
C2502 SCD1U16V2KX-3DLGP
R2501 4K7R2J-2-GP
SPI25
CS# SO/SIO1 SIO2 GND
VCC SIO3 SCLK SI/SIO0
MX25L12872FM2I-10G-GP
072.25128.0D61
R2518 R2517 33R2F-3-GP
R2519 R2520 R2521 33R2F-3-GP
SPI_CS_ROM_N0 SPI_SO_ROM SPI_WP_ROM SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM
SPI_SO_CPU SPI_WP_CPU SPI_HOLD_CPU SPI_CLK_CPU SPI_SI_CPU

R2502 Do Not Stuff DY
SPI251
R2526 R2525 Do Not Stuff DY
R2522 R2523 R2524 Do Not Stuff DY
SPI_CS_ROM_N1 SPI_SO_ROM SPI_WP_ROM SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM
Do Not Stuff

Main Func = RTC

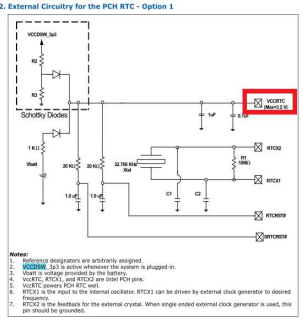
BTY RTC CR2016_30MM KTS 2PIN
1st= 23.25212.011
-1 20161118

3D3V_AUX_S5
R2505 0R2J-2-GP
3D3V_RTC_SYS
R2503 Do Not Stuff DY
3D3V_RTC_PWR
3D3V_RTC_AUX
D2501 BAT54C-12-GP
75.00054.A7D
C2503 SCD47U25V3KX-1-DL-GP
RTC1 PWR GND NP1 NP2
BAT-560201-062A-GP-U
062.70001.0101
R2506 1KR2J-1-GP

Q2505 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
R2504 10MR2J-L-GP
RTC_DET# D2504 A RTC_DET#_PCH
1SS355T1G-GP
83.00355.G1F
20180102

3D3V_S5_PCH
R2040 10KR2J-3-GP RTC_DET#

Figure 28-2. External Circuitry for the PCH RTC - Option 1



20 RTC_DET#_PCH
24 RTCRST_ON
24 VCCDSW_EN#
15,40,45 3V_5V_POK
52,53 3V_5V_DSW_OK

3D3V_RTC_AUX
R2515 Do Not Stuff
NON_RTC_RST
Q2501 PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
RTC_RST
RTC_AUX_S5
R2514 4K7R2J-2-GP
RTC_3P3_EN_D
D2503 Do Not Stuff DY
2ND = 83.R5003.T8F
Q2502 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31
4th = 84.2N702.W31
R2512 1MR2J-1-GP
RTCRST_ON
RTC_3P3_EN_G
R2513 100KR2J-1-GP
C2504 SCD022U16V2KX-3DLGP

3D3V_S5
R2509 100KR2J-1-GP
VCCDSW_EN#
C2505 Do Not Stuff DY
R2508 Do Not Stuff
NON_RTC_RST
R2510 10KR2J-3-GP
3V_5V_POK
D2502 BAT54A-11-GP
3V_5V_DSW_OK
RTC_RST
75.BAT54.07D
2ND = 75.00054.Q7D
U2502 SY6288C20AAC-GP
EN IN OC# GND OUT
074.06288.007B
2nd = 074.03553.007F
R2516 Do Not Stuff
NON_RTC_RST

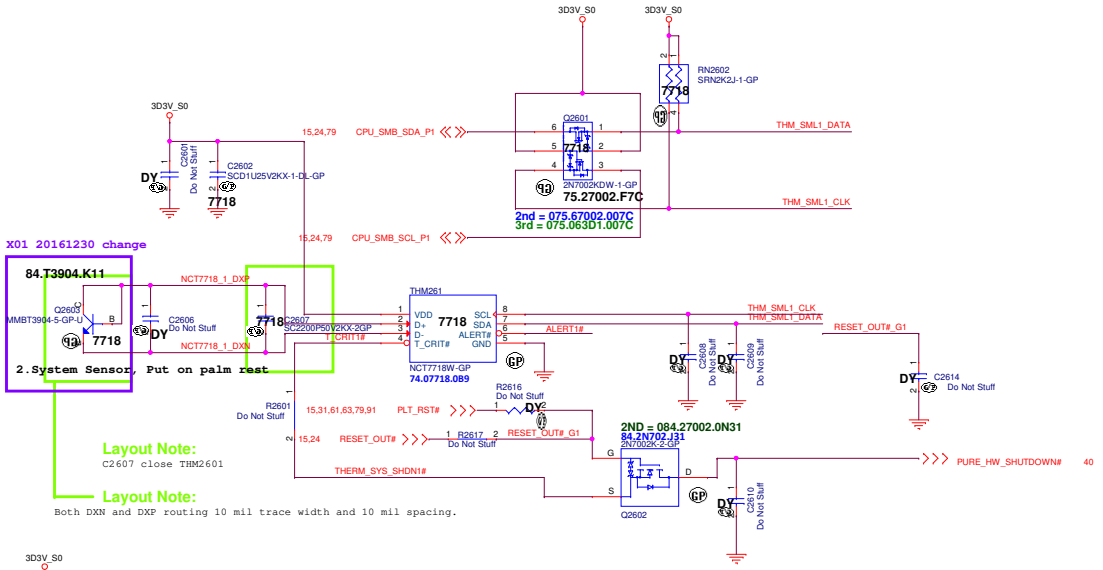
RTC GEN9

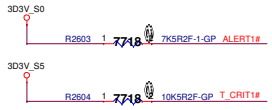
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC
Size: A2
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 25 of 105

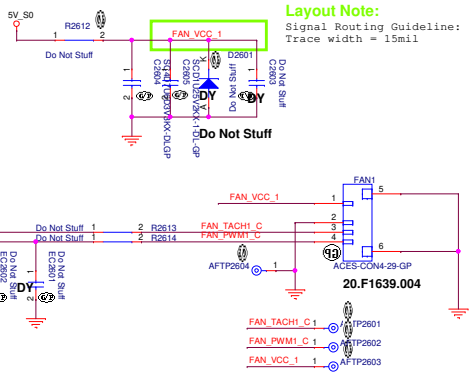
Main Func = Thermal Sensor



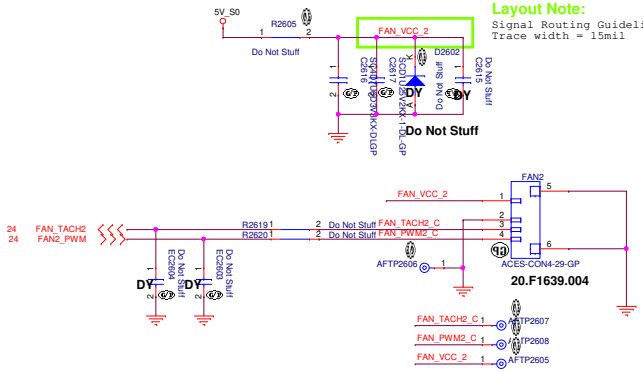


TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1



PWM FAN2



Selek CFLH N17P

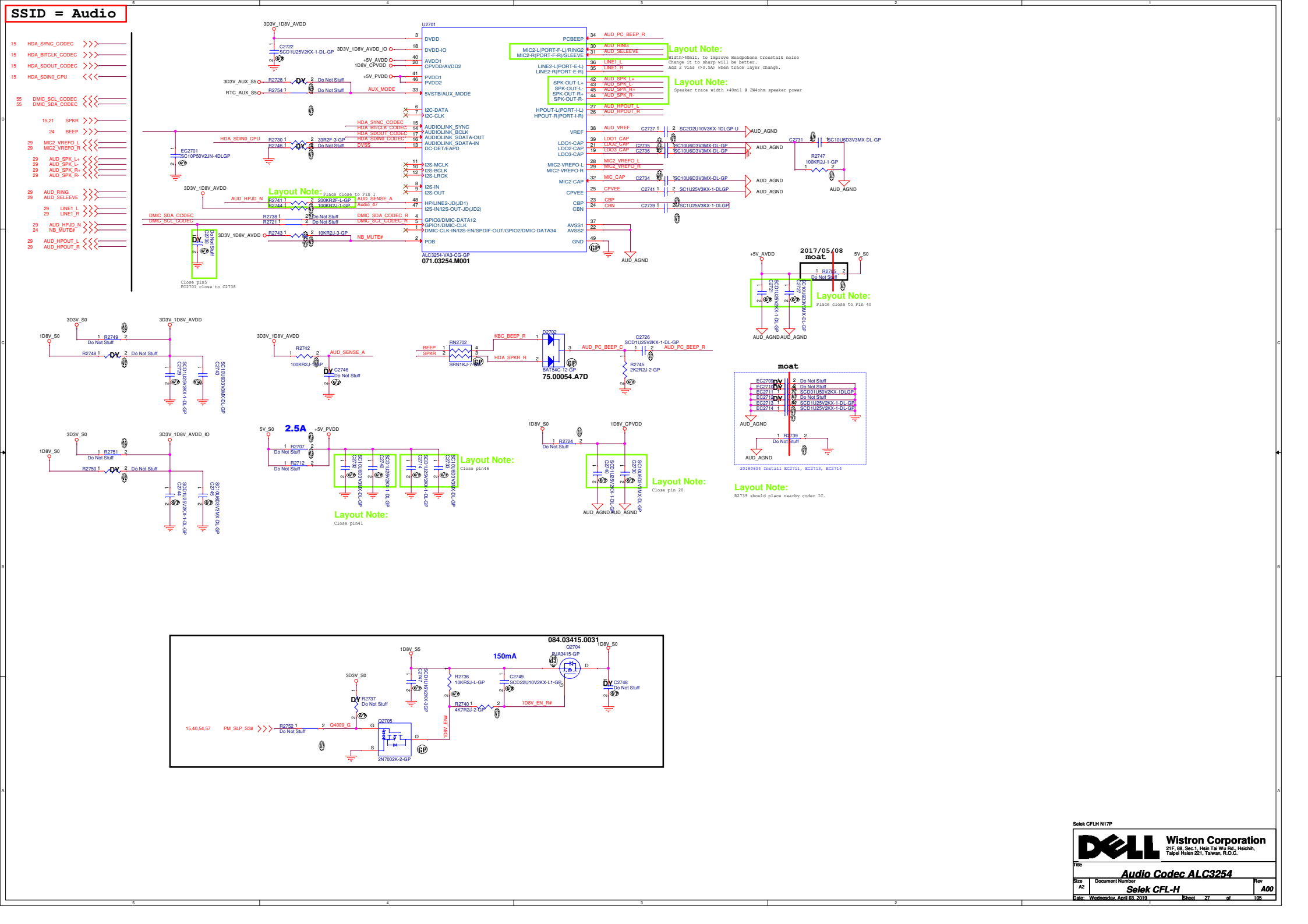
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 26 of 105

SSID = Audio



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3254

Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 27 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 28 of 105

Main Func = Audio

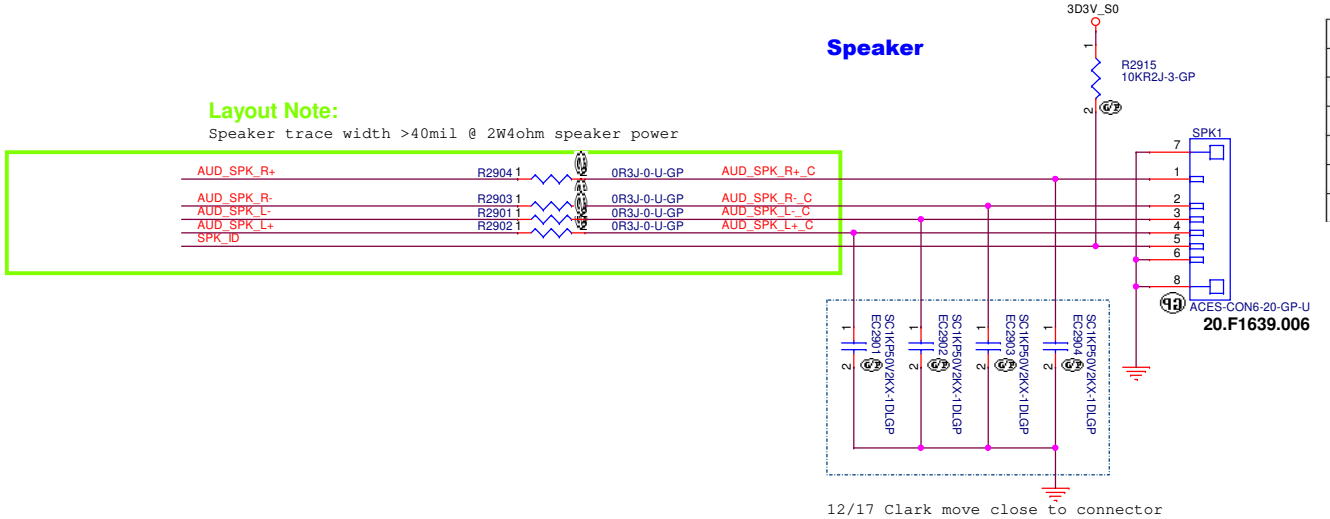
20 SPK_ID

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

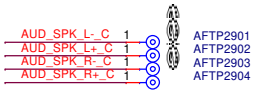
27 MIC2_VREFO_R
27 MIC2_VREFO_L
27 AUD_RING
27 AUD_HPOUT_L
27 LINE1_L
27 AUD_HPOUT_R
27 LINE1_R
27 AUD_SELEEVE
27 AUD_HPJD_N

Speaker

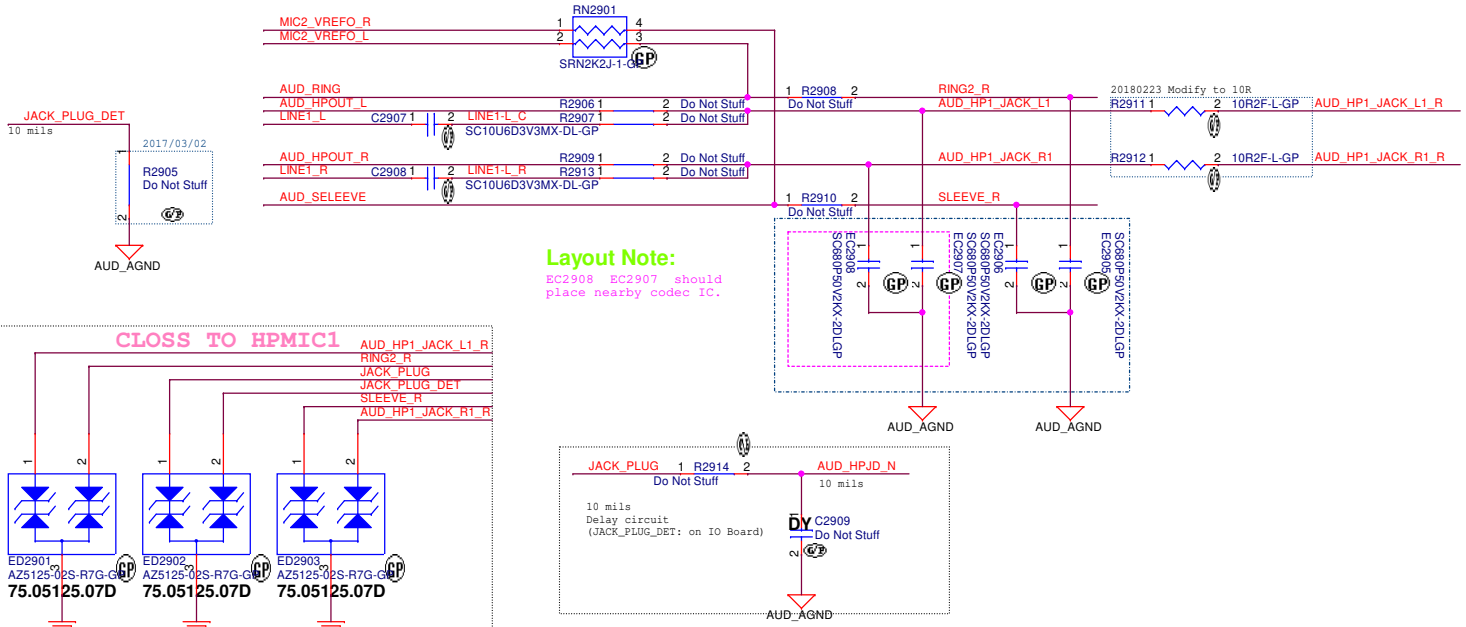
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND



Universal Jack (Moved to I/O Board)



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio IO**

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 29 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 30 of 105

16 LAN_CLK_CPU_P
16 LAN_CLK_CPU_N
16 LAN_CLKREQ_CPU_N

17 LAN_PCIE_TX_P
17 LAN_PCIE_TX_N

17 LAN_PCIE_RX_N
17 LAN_PCIE_RX_P

15,26,61,63,79,91 PLT_RST#

15,24 LAN_WAKE#

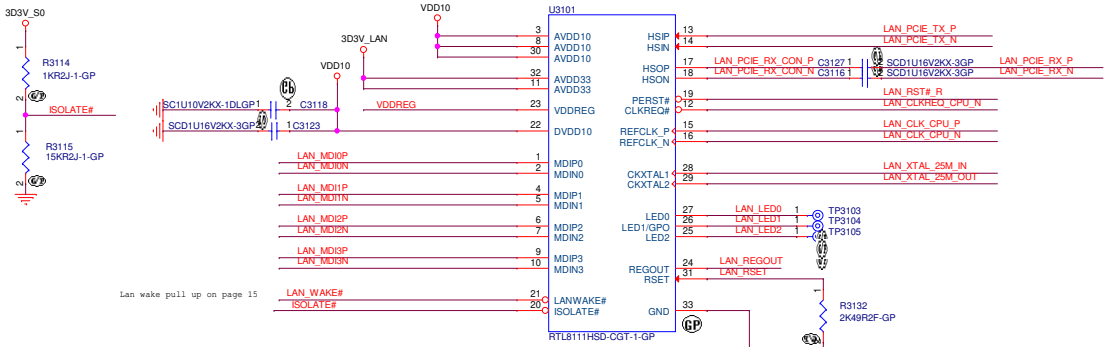
32 LAN_MDI0P
32 LAN_MDI0N

32 LAN_MDI1P
32 LAN_MDI1N

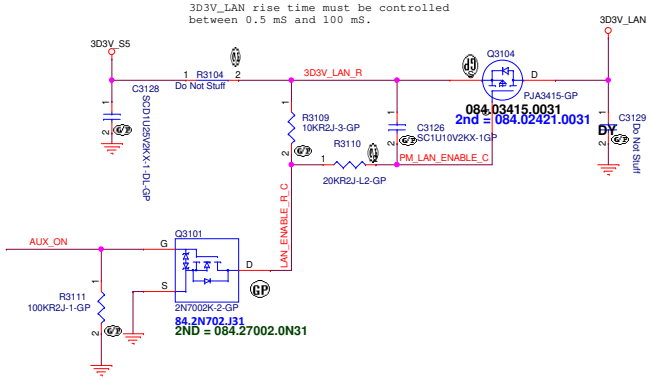
32 LAN_MDI2P
32 LAN_MDI2N

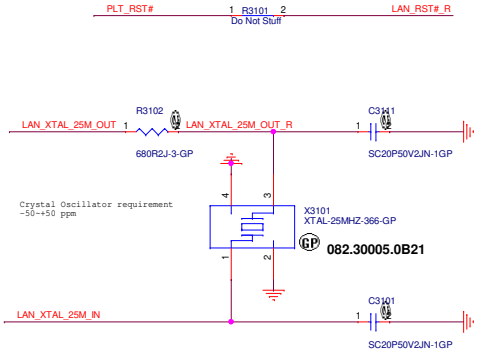
32 LAN_MDI3P
32 LAN_MDI3N

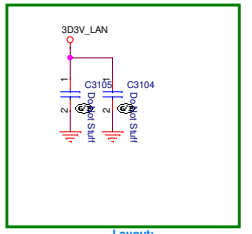
24 AUX_ON



1219 BOM change to 071.8111H.0003





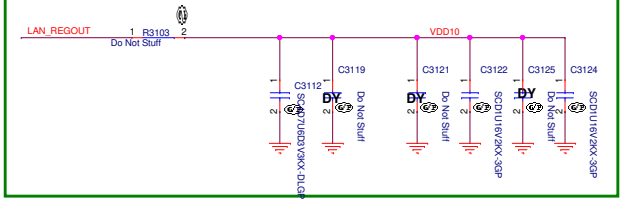


Layout:
C3104: close to Pin11
C3105: close to Pin32

RTL8111HSD-CGT
071.8111H.M001
SWR mode
10/100/1000M

Layout:
For RTL8111G(S)
* Place Ca~Cd close to each VDD10 pin-- 8, 30, 3, 22
For RTL8106E
* Place Ca,Cb close to each VDD10 pin-- 8, 30

C3121: colse to Pin8
C3122 close to Pin3
C3125: close to Pin30
C3124: close to Pin22

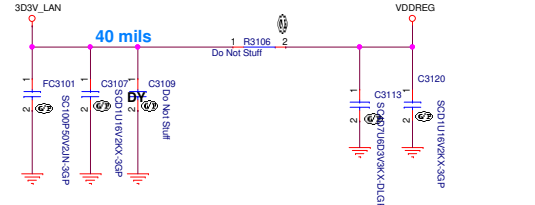


Layout:
For RTL8111G(S)
* Place Ce and Cf close to each VDD33 pin-- 11, 32
For RTL8106E
* Place Cg and Cf close to each VDD33 pin-- 23, 32

Cf: close to Pin32
Ce: close to Pin11
Cg: close to Pin23

150mA

LAN power Noise 1.0V < 100mV Vpeak to Vpeak.



Selek CFLH N17P

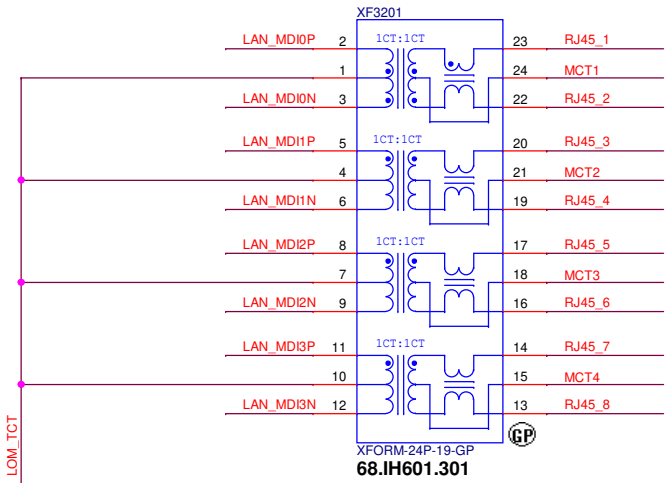
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

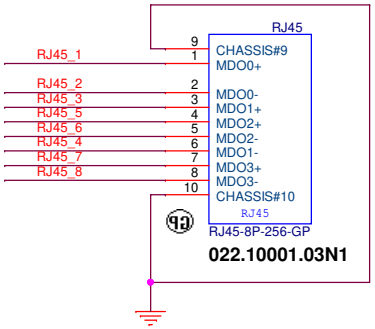
Title: LAN RTL8111H

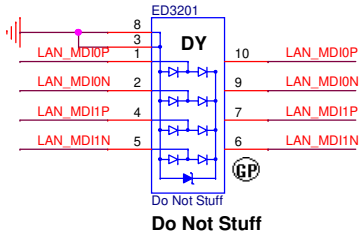
Size: Custom | Document Number: Selek CFL-H | Rev: A00

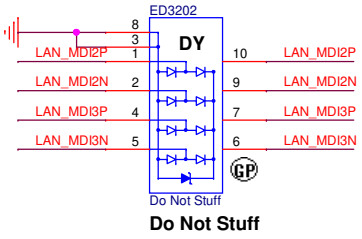
Date: Wednesday, April 03, 2019 | Sheet 31 of 105

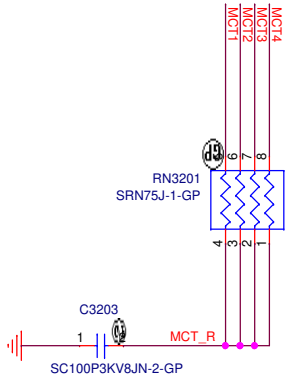
SSID = LAN











Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RJ45+Transformer*		
Size: B	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 32 of 105	

SSID = Card Reader

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 33 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 34 of 105

19 USB1_USB30_RX_N
19 USB1_USB30_RX_P
19 USB1_USB30_TX_N
19 USB1_USB30_TX_P
18 USB1_USB20_P
18 USB1_USB20_N

24,35 USB_EN#
18 USB_OC0#

24,35 USB_EN#
18 USB_OC1#

USB1_USB30_RX_N — R3501 0R2J-2-GP — USB1_USB30_RX_CON_N

USB1_USB30_RX_P — R3502 0R2J-2-GP — USB1_USB30_RX_CON_P

USB1_USB30_TX_N — C3508 SCD1U25V2KX-1-DL-GP — USB1_USB30_TX_N_R — R3503 0R2J-2-GP — USB1_USB30_TX_CON_N

USB1_USB30_TX_P — C3509 SCD1U25V2KX-1-DL-GP — USB1_USB30_TX_P_R — R3504 0R2J-2-GP — USB1_USB30_TX_CON_P

ED3501
USB1_USB30_RX_CON_N ↔ USB1_USB30_RX_CON_N
USB1_USB30_RX_CON_P ↔ USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N ↔ USB1_USB30_TX_CON_N
USB1_USB30_TX_CON_P ↔ USB1_USB30_TX_CON_P
L05ESDL5V0NA-4-GP
075.00550.0071

USB1_USB20_P / USB1_USB20_N — EL3501 FILTER-4P-213-GP — USB1_USB20_CON_P / USB1_USB20_CON_N
068.MCF86.2001

ED3502
I/O1, I/O4, GND, VDD, I/O2, I/O3
USB1_USB20_CON_N — O5V_S5 — USB1_USB20_CON_P
AZC099-04S-2-GP
075.09904.0A7C
2nd = 75.08902.07C

USB30_VCCA
USB2
USB1_USB20_CON_N / USB1_USB20_CON_P
USB1_USB30_RX_CON_N / USB1_USB30_RX_CON_P
USB1_USB30_TX_CON_N / USB1_USB30_TX_CON_P
VBUS, D-, D+, SSRX-, SSRX+, SSTX-, SSTX+, PGND, GND, CHASSIS#10–#13
USB3.0
SKT-USB13-431-GP
022.10005.0FH1

USB30_VCCA
C3504 SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

For USB3.0 port use

5V_S5 — U3501 SY6288DAAC-GP — USB30_VCCA
IN, OUT, GND, EN#, OC#, Active_Low
C3520 SCD1U16V2KX-1DLGP
C3519 SCD1U16V2KX-1-GP
C3518 SC1U50V3KX-1-GP
USB_EN#
USB_OC0#
074.06288.009B
2ND = 074.03553.007G

For IO USB2.0 port use

5V_S5 — U3502 SY6288DAAC-GP — USB30_VCCB
IN, OUT, GND, EN#, OC#, Active_Low
C3524 SCD1U16V2KX-1DLGP
C3523 SCD1U16V2KX-1-GP
C3522 SC1U50V3KX-1-GP
USB_EN#
USB_OC1#
074.06288.009B
2ND = 074.03553.007G

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0*2 CONN
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 35 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Charger***

Size	Document Number	Rev
B	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 36 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 37 of 105

SSID = USB3.0 Redrivere

USB 3.0 Re-driver Pull High / Low

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Redriver

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 38 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 39 of 105

Power Sequence

15,27,54,57 PM_SLP_S3#

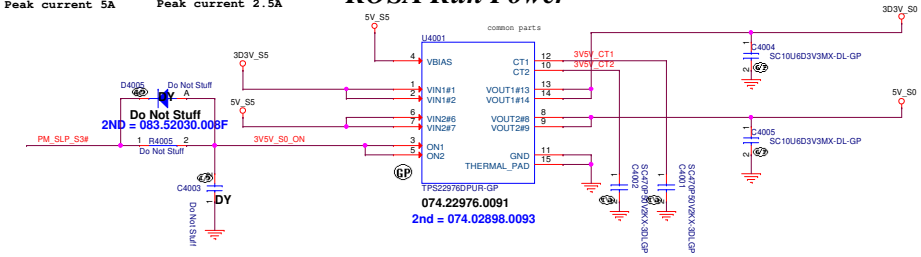
5V_S0

5V_S0 Comsumption
Peak current 5A

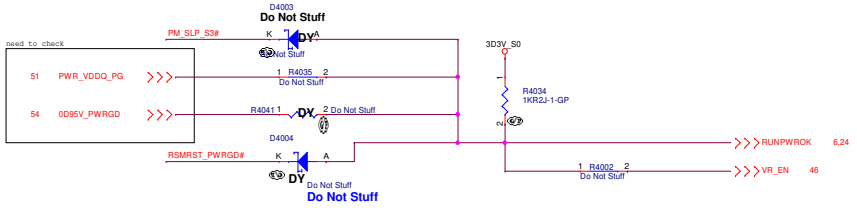
3D3V_S0

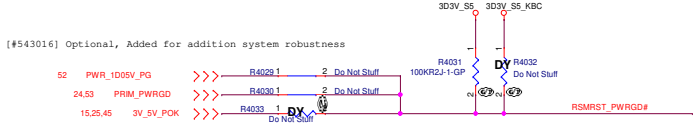
3D3V_S0 Comsumption
Peak current 2.5A

ROSA Run Power

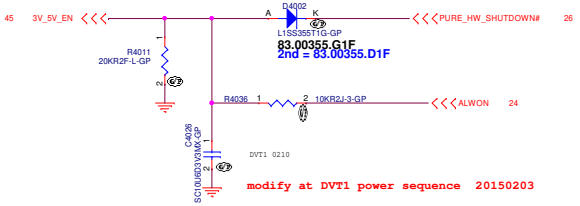


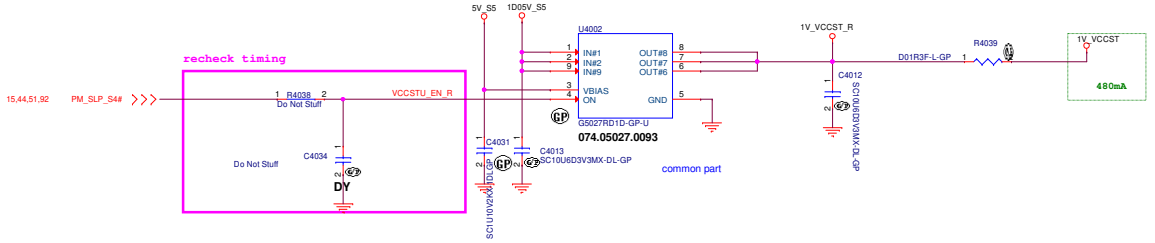
Power Good





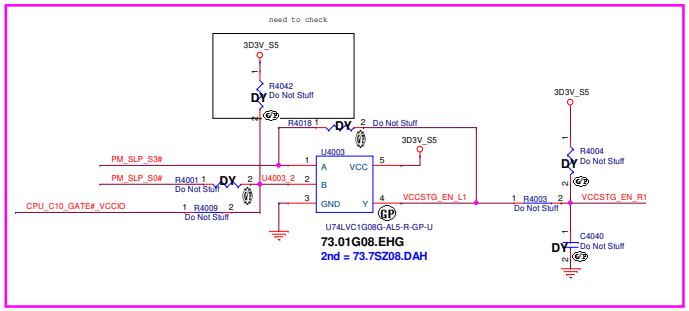
1V_VCCST



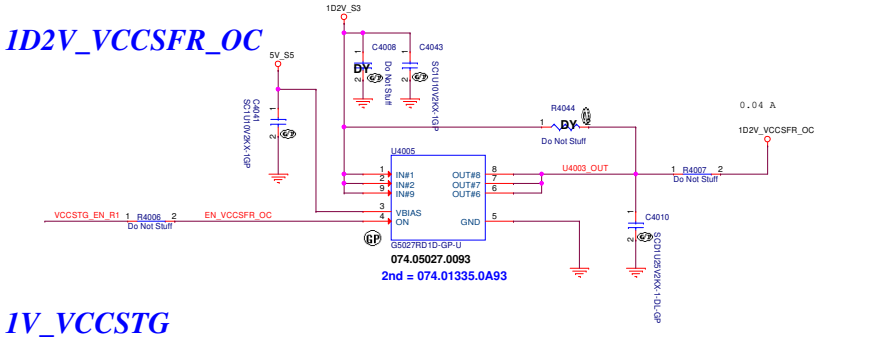


15,91 PM_SLP_S0#
17 CPU_C10_GATE#
54 CPU_C10_GATE#_VCCIO

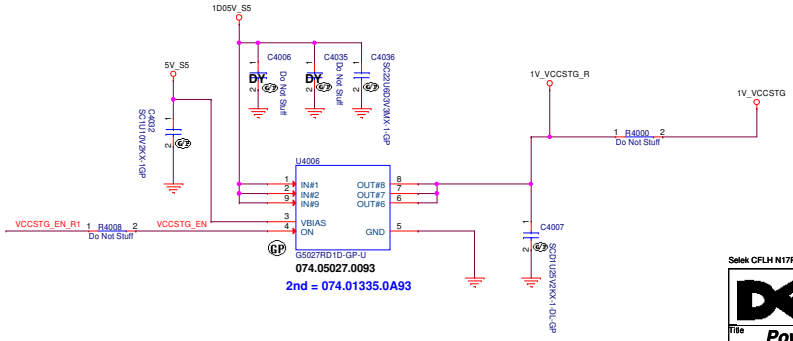
Sequence reserve

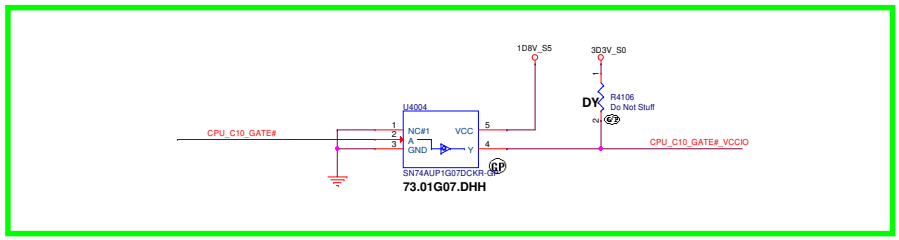


1D2V_VCCSFR_OC



1V_VCCSTG





Selek CFLH N17P

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 40 of 105

Main Func = Power & Sequence

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(1/2)+DS3*

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 41 of 105

Selek CFLH N17P

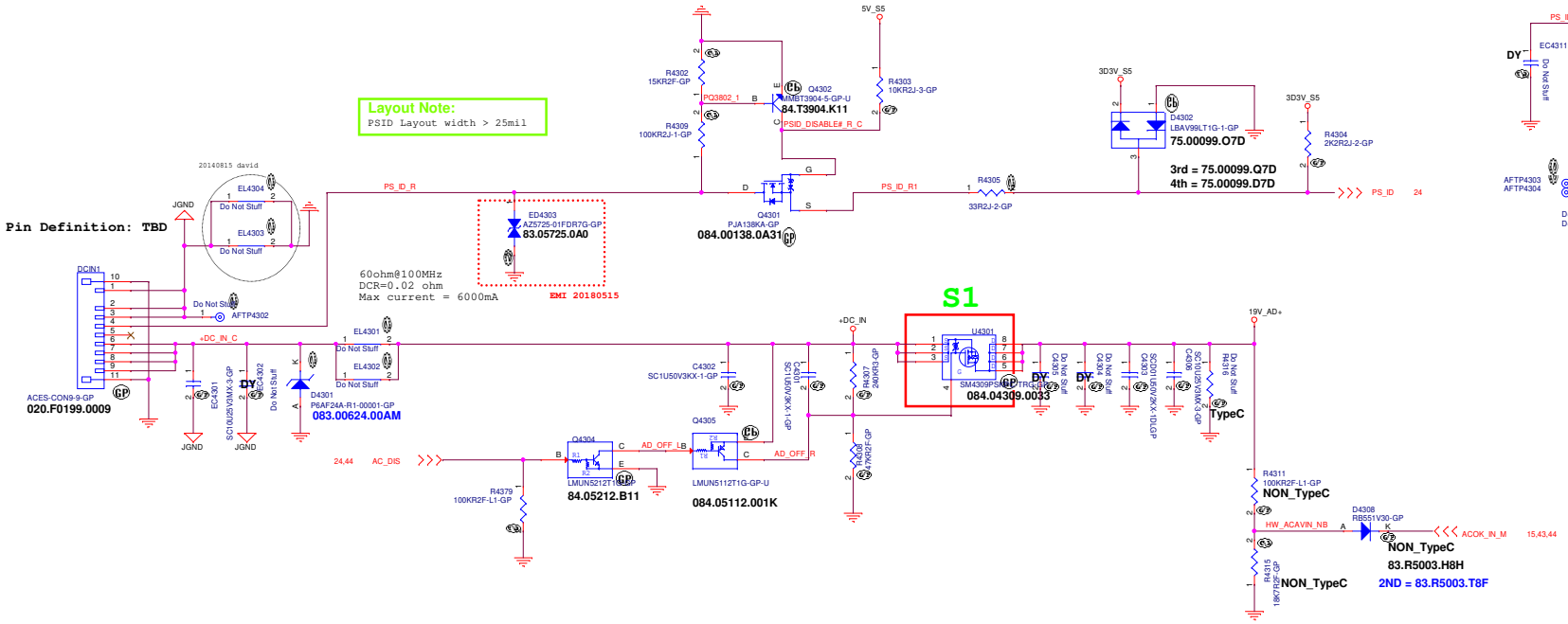
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

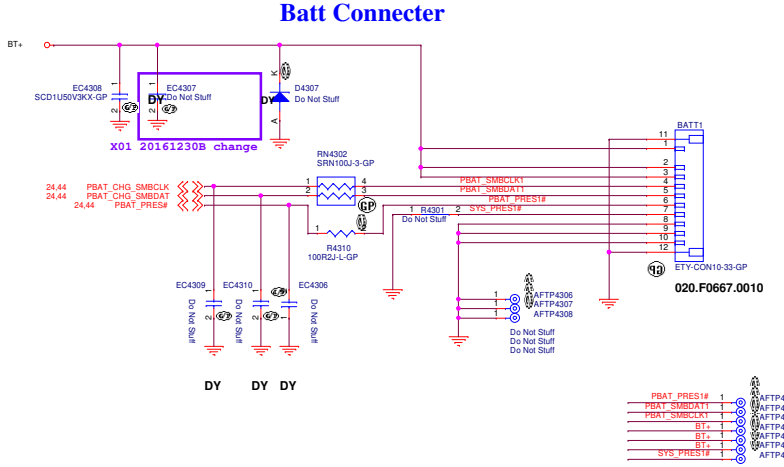
Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

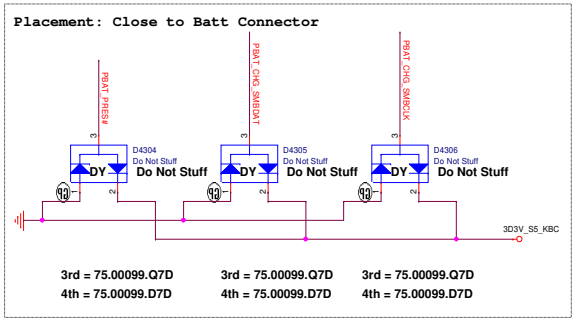
Date: Wednesday, April 03, 2019 Sheet 42 of 105

Main Func = ADT Input

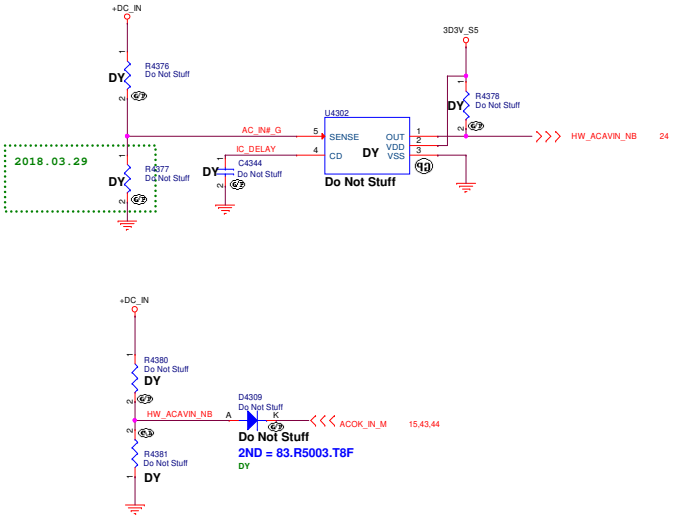


Main Func = M-BAT Input





Barrel Adapter Piug-in Detect



Selek CFLH N17P

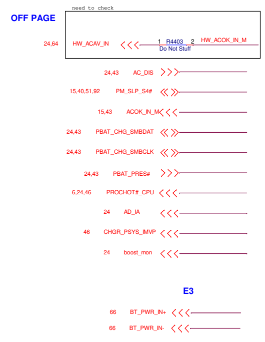
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

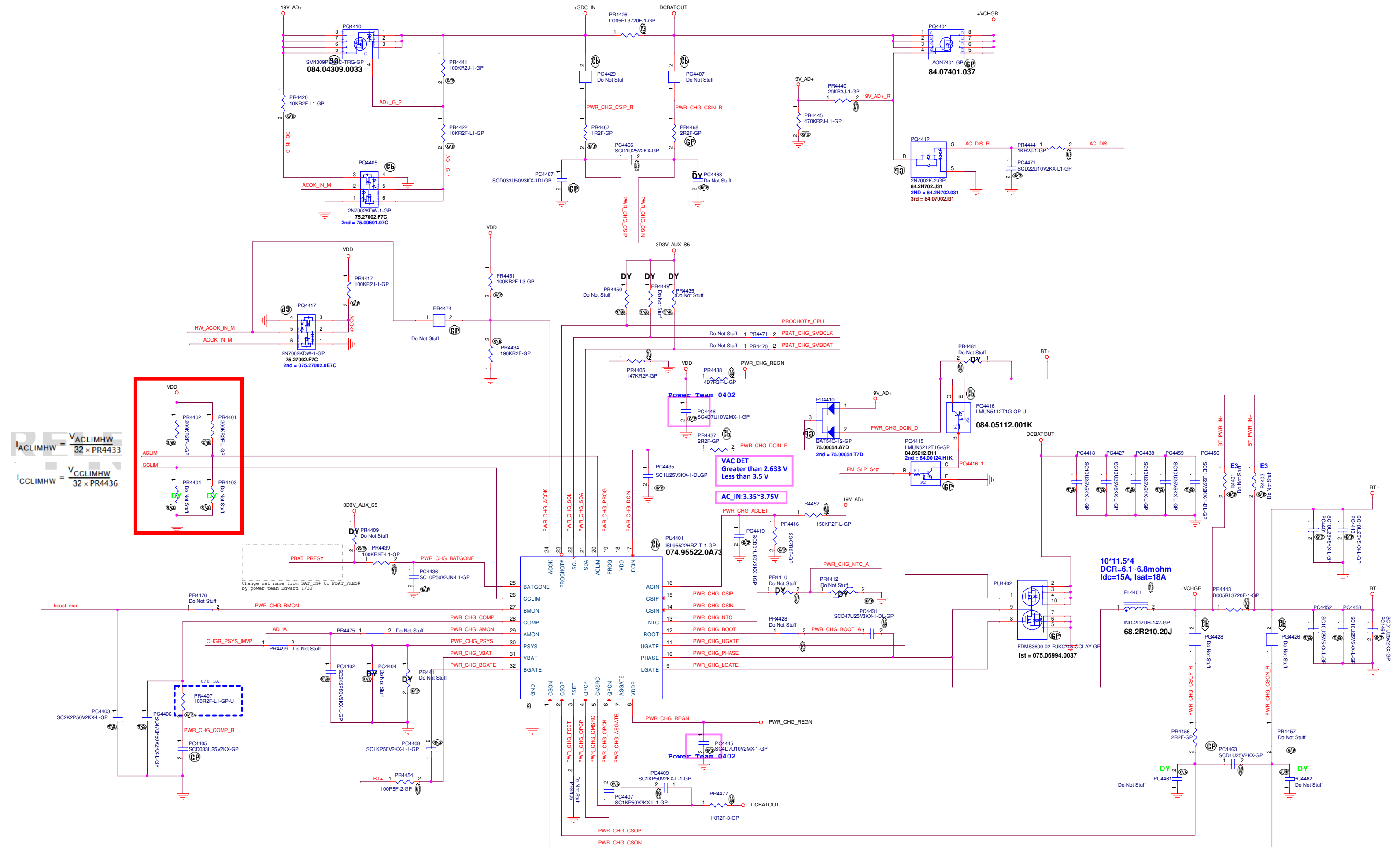
Title		
DCIN		
Size: A2	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 43 of 105	

Main Func = Charger

ISL95522 Hybrid Charger

OFF PAGE



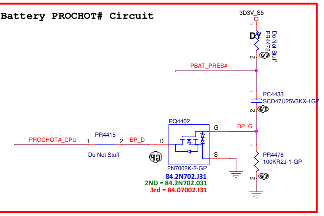


$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times PR4433}$$

$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times PR4436}$$

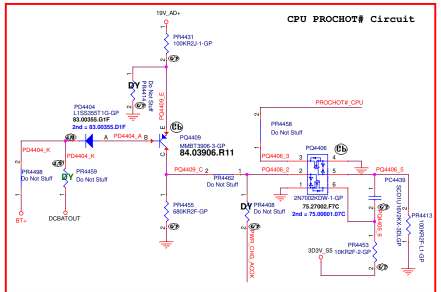
Need fine tune

Battery PROCHOT# Circuit



PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

CPU PROCHOT# Circuit



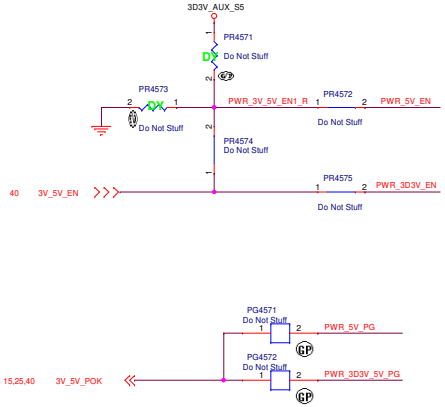
Selek CFL-H N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

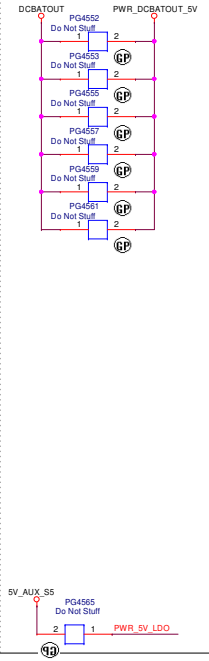
Title: Charger
Size: A1 | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 44 of 105

SSID = PWR.Plane.Regulator_5V

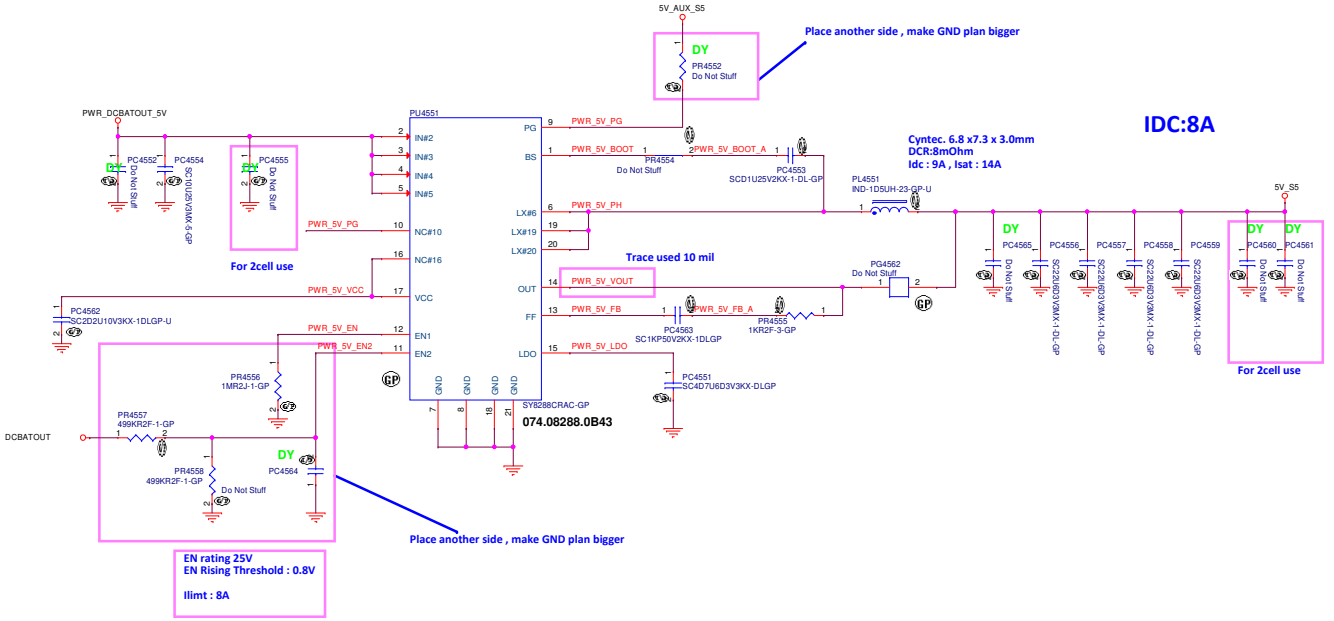
OFFPAGE-Signal



OFFPAGE-GAP



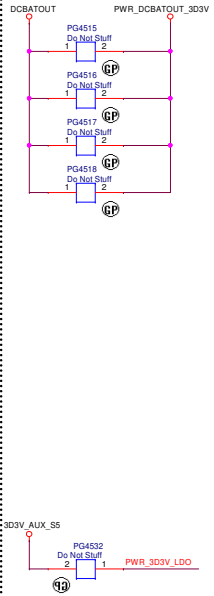
SY8288C For 5V



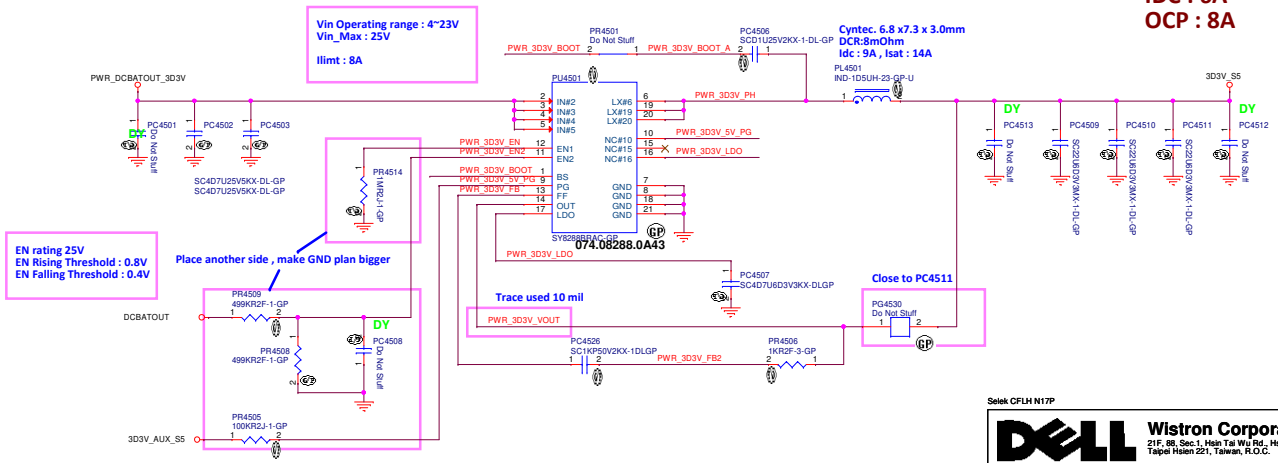
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



SY8286B For 3D3V



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (SY8288_5V/3D3V)

Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 45 of 105

OFFPAGE

VCCSA SENSE

VCCCORE SENSE

VCCGT_I SENSE

Close to VCCSA Choke

Close to Vcore Choke

Close to VCCGT_I Choke

VCCCORE Feedback

VCCGT Feedback

VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V

Close to VCORE Dr.MOS

Close to VCCGT_I Dr.MOS

Add : PWR GAP
change GND symbol on this page ALL GND

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC IMVP8

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 46 of 105

For acousaic noise 1228

DCBATOUT
PWR_DCBATOUT_VCCCORE
PL4711
PBY201209T-170Y-N-GP
PL4712
PBY201209T-170Y-N-GP
PT4711
SE33U25VM-11-GP
PL4701
DY
Do Not Stuff

EE 0401

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

PC4713 PC4714 PC4715 PC4716 PC4717
SC10U25V5KX-DL-GP
SCD1U25V2KX-1DL-GP

PU4702
NCP302045MNTWG-1-GP
ON
074.30204.0AE3

VIN PHASE BOOT VCC VCCD
PWM DISB#
THWN SMOD#
PGND
GL#27 GL#33 NC#6 AGND CGND
VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22
VSW#26 VSW#25 VSW#24 VSW#23

PR4703 3D9R3-GP
PC4702 SCD22U25V3KX-GP
PWR_CORE_BOOT_PH1
PWR_CORE_BOOT_A_PH1
PWR_CORE_PHASED_PH1

5V_S5
PWR_CORE_VCCA
PR4704 2R2J-2-GP
PC4703 SC1U10V2KX-1GP
PC4704 SC1U10V2KX-1GP

PWR_CORE_DISB#_PH1
PR4705 Do Not Stuff
PR4717 DY Do Not Stuff
PWR_VCCCORE_PWM1 46
PWR_CORE_DRVON 46,47,48,49,50
PWR_CORE_THWN_PH1
5V_S5
PWR_CORE_PH1
PWR_CORE_SNB_PH1

PC4705 SC680P50V2KX-2DLGP
PR4708 2D2R3-1-U-GP

PL4701
COIL-D15UH-2-GP
68.R1510.20A
1V_CPU_CORE

PG4701 Do Not Stuff
PG4702 Do Not Stuff
PWR_CORE_ISEN1_N 46
PWR_CORE_ISEN1_P 46

CFL_H-45W
IMAX 96 A / TDC 75 A / OCP 120 A
PT4701 PT4702 PT4703 PT4704
SE330U2DM-4-GP
330uF 4 Pcs

EE 0401

MLCCs must be placed symmetrically on Top and Bottom.

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

PC4757 PC4758 PC4759 PC4760 PC4761
SC10U25V5KX-DL-GP
SCD1U25V2KX-1DL-GP

PU4701
NCP302045MNTWG-1-GP
ON
074.30204.0AE3

VIN PHASE BOOT VCC VCCD
PWM DISB#
THWN SMOD#
PGND
GL#27 GL#33 NC#6 AGND CGND
VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22
VSW#26 VSW#25 VSW#24 VSW#23

PR4711 3D9R3-GP
PC4706 SCD22U25V3KX-GP
PWR_CORE_BOOT_PH2
PWR_CORE_BOOT_A_PH2
PWR_CORE_PHASED_PH2

5V_S5
PWR_CORE_VCCB
PR4712 2R2J-2-GP
PC4707 SC1U10V2KX-1GP
PC4708 SC1U10V2KX-1GP

PWR_CORE_DISB#_PH2
PR4713 Do Not Stuff
PR4718 DY Do Not Stuff
PWR_VCCCORE_PWM2 46
PWR_CORE_DRVON 46,47,48,49,50
PWR_CORE_THWN_PH2
5V_S5
PWR_CORE_PH2
PWR_CORE_SNB_PH2

PC4774 SC680P50V2KX-2DLGP
PR4716 2D2R3-1-U-GP

PL4702
COIL-D15UH-2-GP
68.R1510.20A
1V_CPU_CORE

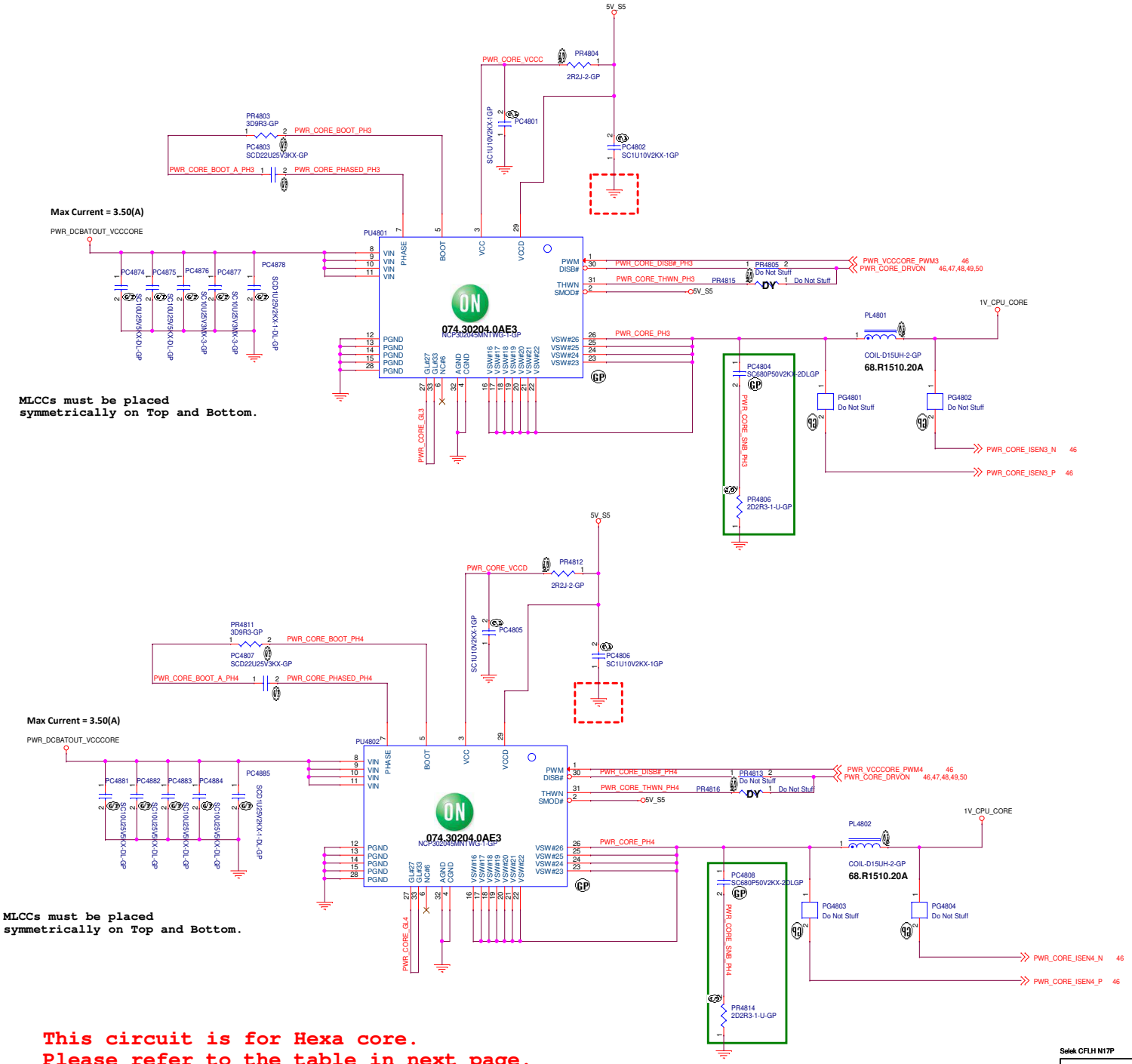
PG4703 Do Not Stuff
PG4704 Do Not Stuff
PWR_CORE_ISEN2_N 46
PWR_CORE_ISEN2_P 46

MLCCs must be placed symmetrically on Top and Bottom.

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

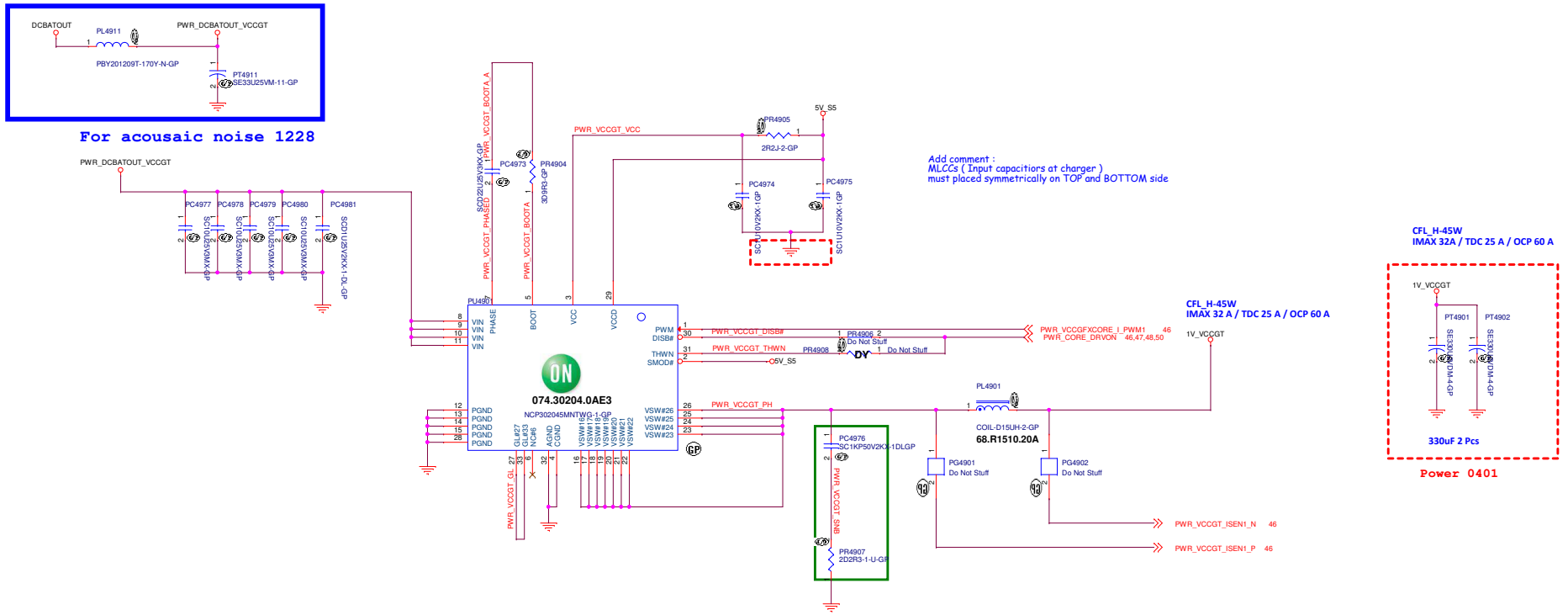
Title: DC/DC VCCCPUCORE (1/2)
Size: C
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 47 of 105



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC/DC VCCCPUCORE (2/2)	
Size: C	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 48 of 105	



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCGFXCORE_I(NCP302045)

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 49 of 105

MLCCs must be placed
symmetrically on Top and Bottom.

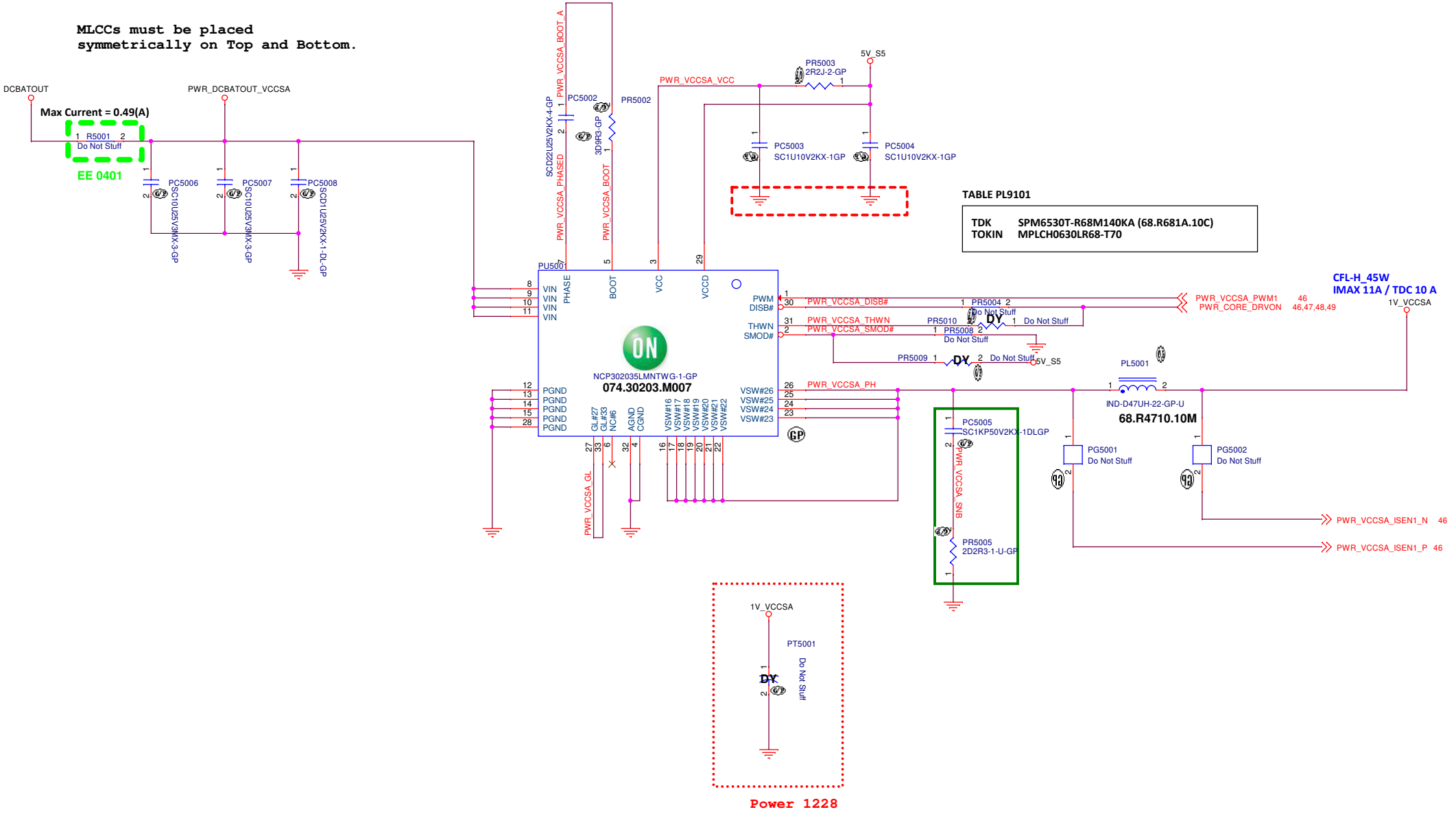


TABLE PL9101

TDK	SPM6530T-R68M140KA (68.R681A.10C)
TOKIN	MPLCH0630LR68-T70

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCSA(NCP302035)

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 50 of 105

SSID = PWR.Plane.Regulator_1D2V/0D6V

OFFPAGE-Signal

S5

S3

6 DDR_PG_OUT → DDR_PG_OUT

PH on EE Side

40 PWR_VDDQ_PG → PWR_VDDQ_PG

DDR_PG_OUT — R5102 Do Not Stuff — PWR_VTT_EN

OFFPAGE-GAP

DCBATOUT — PG5101 Do Not Stuff — PWR_DCBATOUT_VDDQ

PG5102 Do Not Stuff

PG5103 Do Not Stuff

1D2V_S3 — PG5105 Do Not Stuff — PWR_VDDQ

PG5106 Do Not Stuff

PG5107 Do Not Stuff

PG5108 Do Not Stuff

PG5109 Do Not Stuff

PG5110 Do Not Stuff

PG5112 Do Not Stuff

PG5114 Do Not Stuff

1D2V_S3 — PG5115 Do Not Stuff — PWR_VDDQ_VLDOIN

PG5116 Do Not Stuff

0D6V_S0 — PG5111 Do Not Stuff — PWR_VDDQ_VTT

PG5113 Do Not Stuff

G5388 For VDDQ/VTT

5V_S5 — PR5101 10R2J-L-GP — PWR_VDDQ_VCC

PC5102 DY — Do Not Stuff — If 5V has droop Please mount it

PC5104 SC1U10V2KX-1DLGP

PR5102 6K49R2F-1-GP

3D3V_S5 — PR5104 DY Do Not Stuff

PR5108 = 510K
Fs = 400~550KHz

PWR_DCBATOUT_VDDQ — PR5108 510KR2F-GP

PWR_VDDQ_PG — PWR_VDDQ_TON — PWR_VDDQ_EN — PWR_VTT_EN

PWR_VDDQ_VLDOIN — PC5103 SC1U10V2KX-1DLGP

PWR_VDDQ_VTT — PC5111 DY — PC5112

Do Not Stuff SC10U6D3V3MX-DL-GP

G5388K11U-GP

PU5101

PGOOD, TON, S5, S3, VLDOIN, VTTGND, VTTSNS, NC#26, GND, VTTREF, VDDQSNS, VDDQSET, CS, VCC, V+, V5, BST, LX#25, LX#17, LX#18, LX#19, LX#20, LX#35, PGND

PWR_VDDQ_BOOT — PR5111 Do Not Stuff — PWR_VDDQ_BOOTA — PC5110 SCD1U25V2KX-1-DL-GP

PWR_VDDQ_BOOTB

PWR_VDDQ_PH — PL5101 COIL-1UH-34-GP-U1

Cyntec, 7 x 7 x 3.0 mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC : 8A

PWR_VDDQ_VDDQ — PG5104 Do Not Stuff

PC5106 PC5107 PC5109 PC5113 — 5SC220U6D3V3MX-1DLGP

PWR_VDDQ_FB

R1 — PR5105 6K2R2F-GP

R2 — PR5106 10K2R2F-GP

PWR_VDDQ_VTTREF — PC5114 SCD1U25V2KX-1-DL-GP

Vout= 0.75*(1+R1/R2) = 1.2

PWR_VDDQ_PH — DY PR5110 Do Not Stuff — PWR_VDDQ_SNB — DY PC5115 Do Not Stuff

PWR_DCBATOUT_VDDQ — PC5108 DY — PC5101 — PC5105 — SC10U25V5KX-DL-GP SC10U25V5KX-DL-GP

PR5101 DY Do Not Stuff

for PU5101 2nd source: APW8861(074.08861.0043) request DY

SSID = PWR.Plane.Regulator_2D5V

OFFPAGE-Signal

15,40,44,92 PM_SLP_S4# → PM_SLP_S4#

OFFPAGE-GAP

2D5V_S3 — PG5152 D01R5F-GP — PWR_2D5V

APL5934 For 2D5V

5V_S5 — PC5151 SC1U10V2KX-1DLGP

3D3V_S5 — PR5152 10KR2F-2-GP

PG5151 Do Not Stuff

PWR_VDDQ_EN — PM_SLP_S4# — PR5133 Do Not Stuff

PR5156 Do Not Stuff

PR5151 Do Not Stuff — PC5156 Do Not Stuff

PU5151 APL5934KAI-TRG-GP-U

VCNTL, POK, EN, VIN#9, VIN#5, VOUT#4, VOUT#3, FB, GND

PWR_2D5V_PG — PWR_2D5V_EN — *PWR_2D5V_FB

PC5155 SC10U6D3V3MX-DL-GP

Design current=700mA

PWR_2D5V

R1 — PR5154 28K4R2F-GP

R2 — PR5155 13K7R2F-GP

PC5152 Do Not Stuff — PC5153 Do Not Stuff — PC5154 SC10U6D3V3MX-DL-GP

Vout=0.8V*(R1+R2)/R2

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (G5388_VDDQ_VTT_VPP)

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 51 of 105

SSID = PWR.Plane.Regulator_1D05V

OFFPAGE-Signal

PH on EE Side

40 PWR_1D05V_PG

53 3V_5V_DSW_OK

53 PWR_1D8V_PG

OFFPAGE-GAP

DCBATOUT — PWR_DCBATOUT_1D05V

PG5201 Do Not Stuff

PG5202 Do Not Stuff

PG5203 Do Not Stuff

1D05V_S5 — PWR_1D05V

PG5204 Do Not Stuff

PG5205 Do Not Stuff

PG5206 Do Not Stuff

PG5207 Do Not Stuff

PG5208 Do Not Stuff

PG5209 Do Not Stuff

PG5211 Do Not Stuff

PG5212 Do Not Stuff

PG5213 Do Not Stuff

PG5214 Do Not Stuff

COM \ IC	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 For 1D05V

Cyntec. 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC : 10A

5V_S5

PC5202 SC4D7U25V5KX-DL-GP

PU5201

VCC, IN#7, IN#8, IN#9, TON, PGOOD, EN, PFM#, SS, BST, FB, AGND, PGND

LX#18 LX#17 LX#16 LX#11 LX#10

AOZ2262QI-10-GP-U

PWR_DCBATOUT_1D05V

PC5208 LY Do Not Stuff

PC5209 SC10U25V5KX-DL-GP

PC5210 SC10U25V5KX-DL-GP

PR5201 88K7R2F-L1-GP

PWR_1D05V_TON

PWR_1D05V_PG

PWR_1D05V_EN

PWR_1D05V_PFM

PWR_1D05V_SS

PC5214 SC1KP50V2KX-1DLGP

PR5203 100KR2F-L3-GP

PC5213 SCD01U50V2KX-1GP

PWR_1D05V_PH

PWR_1D05V_BT

PWR_1D05V_VFB

PL5201 COIL-1UH-34-GP-U1

PC5204 SCD1U25V2KX-1-DL-GP

PG5210 Do Not Stuff

PWR_1D05V_VFB_A

PR5202 3K16R2F-GP R1

PR5204 10KR2F-L1-GP R2

PC5212 Do Not Stuff DY

PWR_1D05V

PC5201 PC5203 PC5205 PC5207 PC5206 DY

SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP
SC22U6D3V3MX-1-DL-GP Do Not Stuff

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.0528V

3D3V_S5

PR5208 Do Not Stuff DY

PWR_1D05V_PG

3V_5V_DSW_OK — R5202 1 DY Do Not Stuff — PWR_1D05V_EN

PWR_1D8V_PG — 1 R5205 2 Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ2262_1D05V)

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 52 of 105

Main Func = 1D8V

OFFPAGE

25,52 3V_5V_DSW_OK

PH on EE Side

24,46 PRIM_PWRGD

R5304 DY Do Not Stuff

PWR_1D8V_PG

52 PWR_1D8V_PG

OFFPAGE_GAP

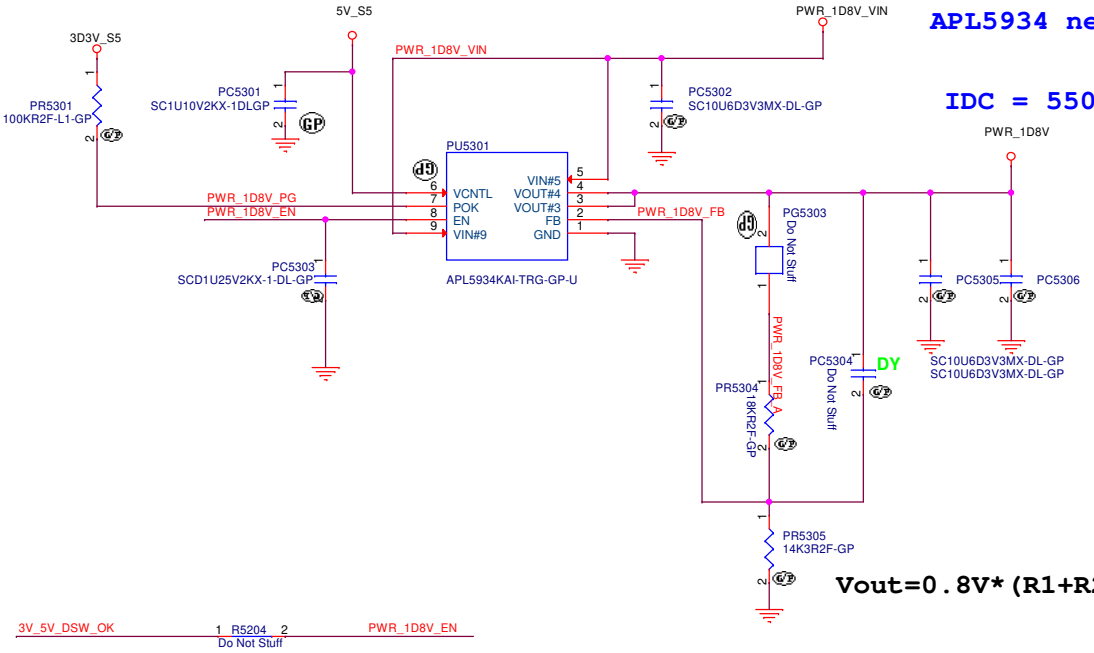
3D3V_S5 — PG5302 Do Not Stuff — PWR_1D8V_VIN

1D8V_S5 — PG5301 Do Not Stuff — PWR_1D8V

APL5934 for 1D8V

APL5934 need <1.8W

IDC = 550mA



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
POWER (APL5934_1D8V)		
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet	of

NB694 for VCCIO

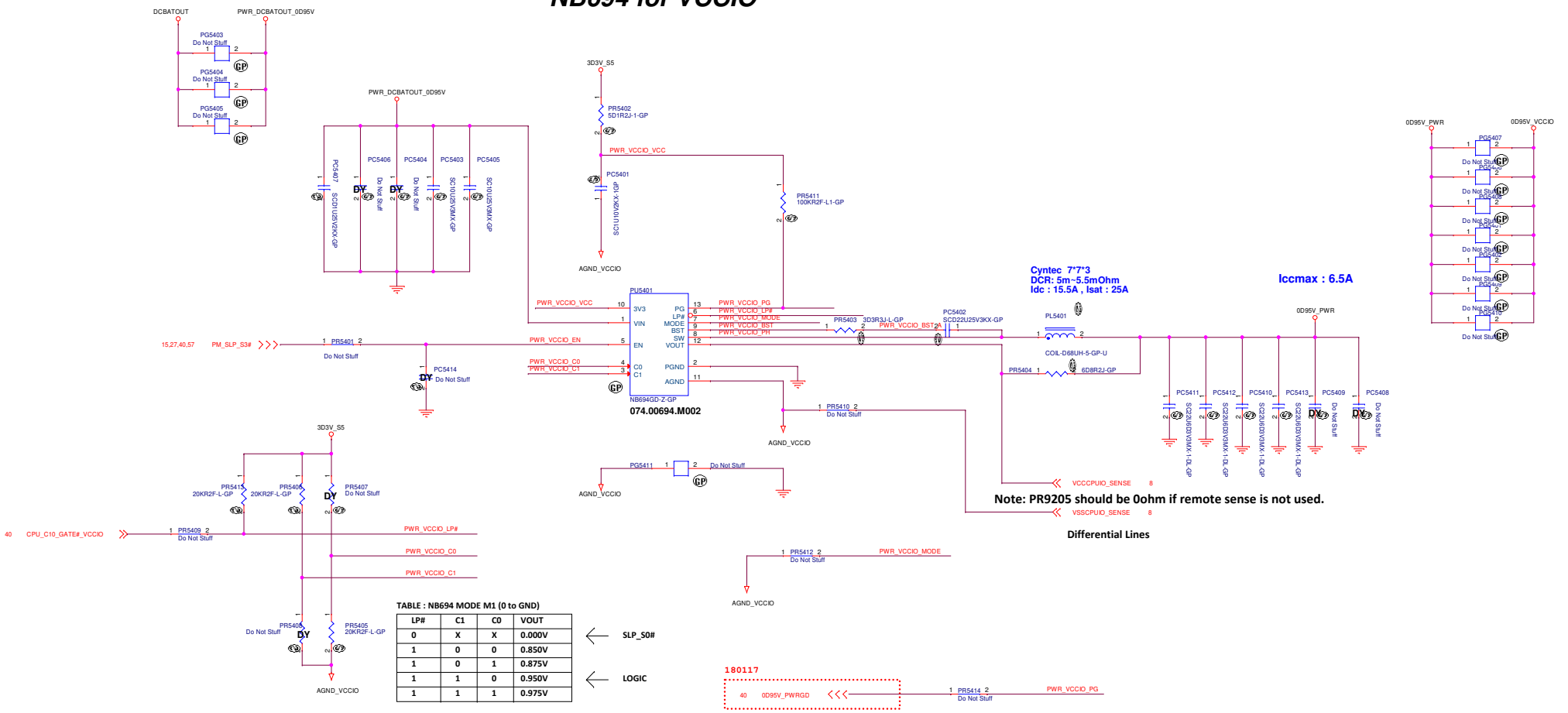


TABLE : NB694 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	LOGIC
1	1	1	0.975V	

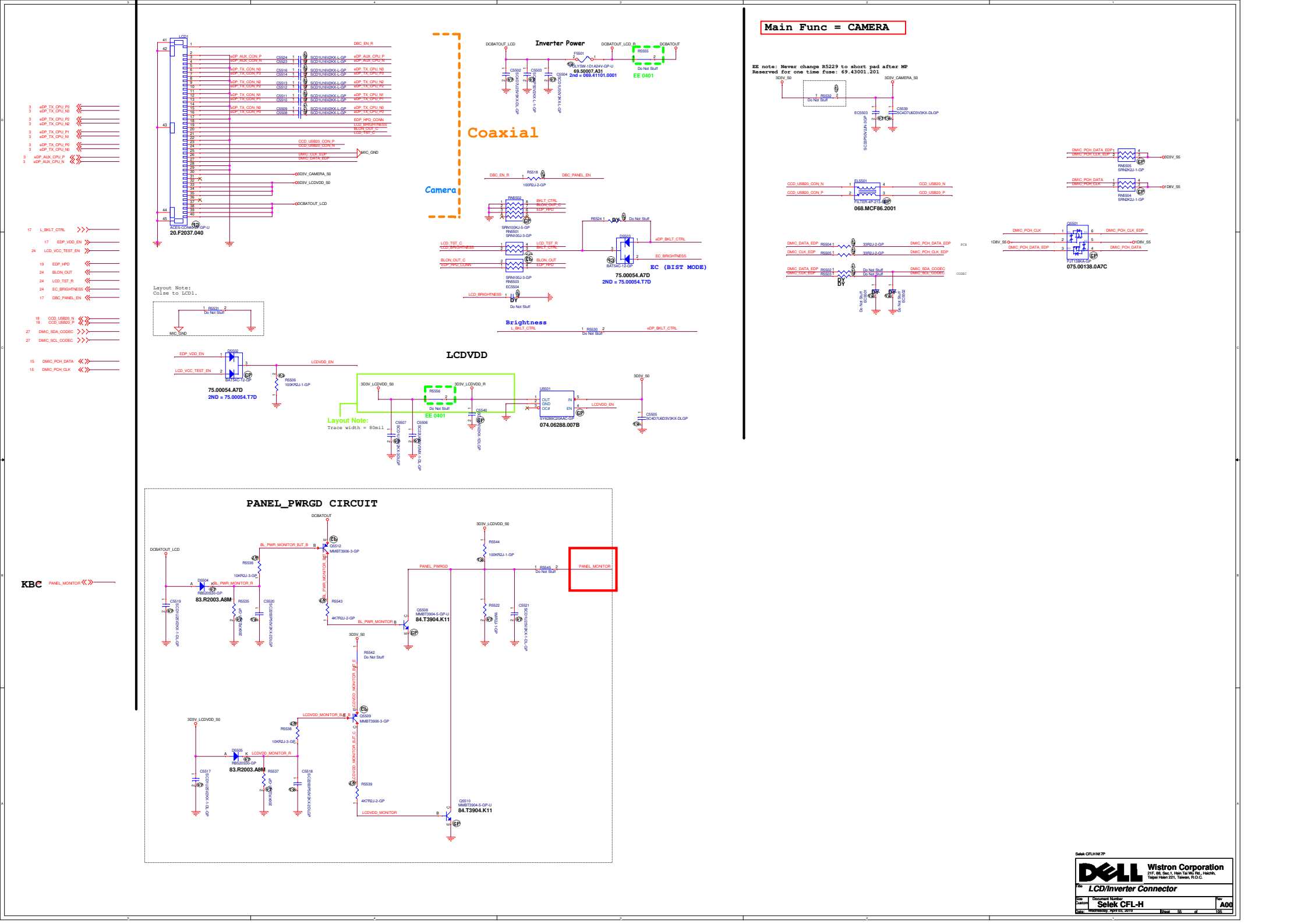
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB964 for 0D95V

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 54 of 105


Main Func = CAMERA
EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201
Coaxial
Camera
Inverter Power
69.50007.A1
2nd = 069.41101.0001
EE 0401
EC (BIST MODE)
75.00054.A7D
2ND = 75.00054.T7D
Brightness
LCDVDD
Layout Note:
Colse to LCD1.
Layout Note:
Trace width = 80mil
20.F2037.040
075.00138.0A7C
074.06288.007B
PANEL_PWRGD CIRCUIT
83.R2003.A8M
84.T3904.K11
KBC
Wistron Corporation
LCD/Inverter Connector
Selek CFL-H
A00

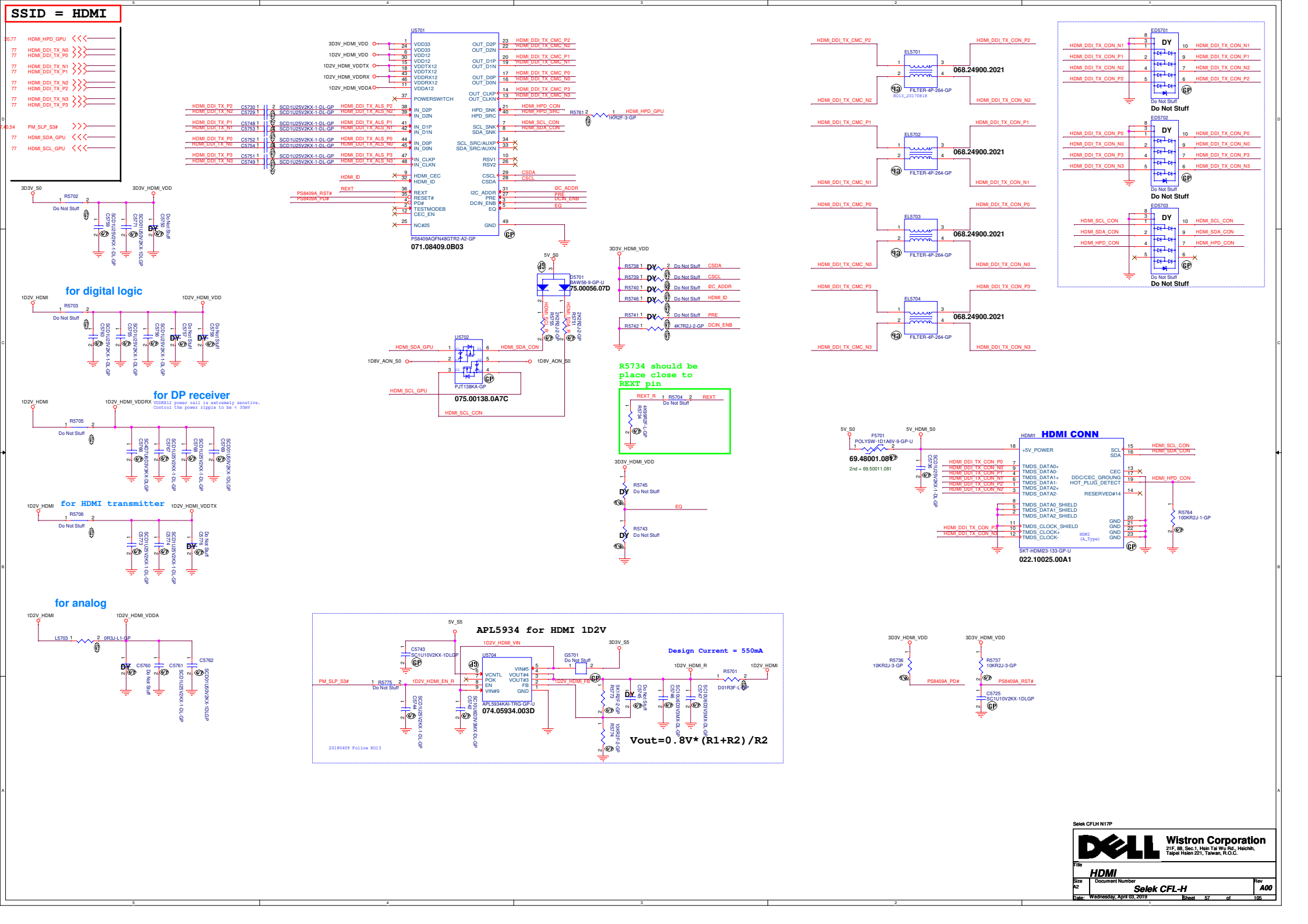
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD/Inverter Connector*

Size	Document Number	Rev
Custom	Selek CFL-H	A00
Date: Wednesday, April 03, 2019	Sheet 56 of 105	

SSID = HDMI



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 57 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 58 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

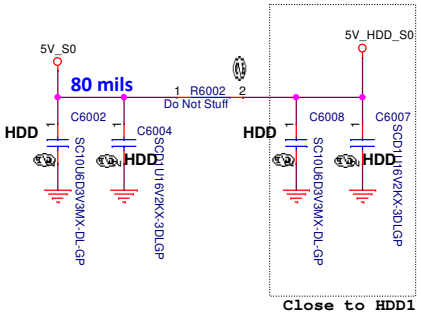
Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

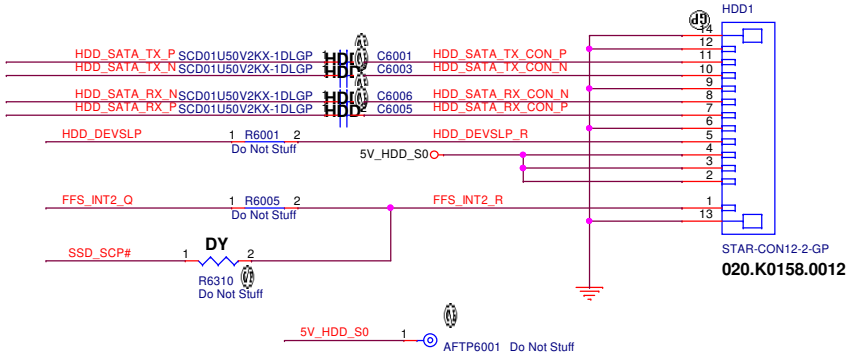
Date: Wednesday, April 03, 2019 Sheet 59 of 105

Main Func = HDD

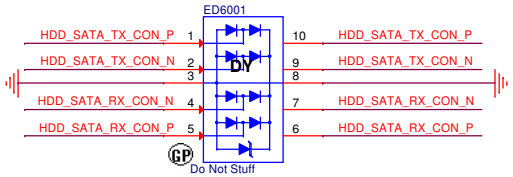
SATA HDD Connector

17 HDD_SATA_TX_P
17 HDD_SATA_TX_N
17 HDD_SATA_RX_N
17 HDD_SATA_RX_P
19 HDD_DEVSLP
70 FFS_INT2_Q
24,63 SSD_SCP#





Layout Note:
Place near HDD1



Do Not Stuff
2nd = 75.01045.073

Table 16-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[1]	None[2]	None[3]

Notes:
1. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
2. For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
3. For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Use a non-interleaved breakout to isolate Tx and Rx.

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA HDD
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 60 of 105

Main Func = WLAN

17 WLAN_PCIE_RX_N
17 WLAN_PCIE_RX_P
17 WLAN_PCIE_TX_N
17 WLAN_PCIE_TX_P
16 WLAN_CLK_CPU_P
16 WLAN_CLK_CPU_N
16 WLAN_CLKREQ_CPU_N

18 BT_USB20_N
18 BT_USB20_P

16 PULSAR_38P4M_REFCLK

15,26,31,63,79,91 PLT_RST#

17 CNV_WR_DN1
17 CNV_WR_DP1
17 CNV_WR_DN0
17 CNV_WR_DP0
17 CNV_WR_CLKN
17 CNV_WR_CLKP
17 CNV_WT_DN1
17 CNV_WT_DP1
17 CNV_WT_DN0
17 CNV_WT_DP0
17 CNV_WT_CLKN
17 CNV_WT_CLKP
17 CNV_BRI_RSP
17,21 CNV_RGI_DT
17 CNV_BRI_DT_CON
17 CNV_RGI_RSP
15 CNV_RF_RESET#

15 CLKREQ_CNV#

20 WLAN_WIGIG60GHZ_DIS#
20 BT_RADIO_DIS#
15 SUS_CLK
20 CNV_DET#

3D3V_S5 3D3V_WLAN_R 3D3V_WLAN
3D3V_S0
R6106 1 2 Do Not Stuff
R6108 1 DY Do Not Stuff
R6155 1 D01R3F-L-GP
C6101 SCD1U16V2KX-3DLGP
C6103 SCD1U16V2KX-3DLGP
C6104 SC220U6D3VM3X-1DL-GP

1D8V_S0 1D8V_S0
R6117 10KR2J-3-GP
Q6101 PJA138KA-GP 084.00138.0A31
R6109 10KR2J-3-GP
WLAN_WIGIG60GHZ_DIS#
WLAN_WIGIG60GHZ_DIS#_R
3D3V_WLAN
R6110 10KR2J-3-GP
BT_RADIO_DIS# RB520S30-GP D6102 BT_RADIO_DIS#_R

83.R2003.A8M
2ND = 083.52030.008F

R6111 1 2 0R2J-2-GP
R6113 1 2 0R2J-2-GP
BT_USB20_P BT_USB20_P_CON
BT_USB20_N BT_USB20_N_CON

1090mA

NGFF_KEY_E_75P

NP1 NP2
GND USB_D+ USB_D- GND SDIO_CLK SDIO_CMD SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3 SDIO_WAKE SDIO_RESET
3_3VAUX 3_3VAUX LED#1 PCM_CLK PCM_SYNC PCM_IN PCM_OUT LED#2 GND UART_WAKE UART_RX
UART_TX UART_RTS UART_CTS CLINK_RESET CLINK_DATA CLINK_CLK COEX3 COEX2 COEX1 SUSCLK_32KHZ PERST0# RESERVED#54/W_DISABLE#2 W_DISABLE#1 NFC_I2C_SM_DATA NFC_I2C_SM_CLK NFC_I2C_IRQ/MGPIO5 GPIO0_NFC_RESET#/MGPIO7 RESERVED#66 RESERVED#68 RESERVED#70 3_3VAUX 3_3VAUX
GND GND PETP0 PETN0 GND PERP0 PERN0 GND REFCLKP0 REFCLKN0 GND CLKREQ0# PEWAKE0# GND RESERVED#59/2ND_LANE_PETP1 RESERVED#61/2ND_LANE_PETN1 GND RESERVED#65/2ND_LANE_PERP1 RESERVED#67/2ND_LANE_PERN1 GND RESERVED#71 RESERVED#73 GND 77

BT_USB20_P_CON BT_USB20_N_CON
CNV_WR_DN1 R6114 1 2 Do Not Stuff CNV_WR_DN1_R
CNV_WR_DP1 R6115 1 2 Do Not Stuff CNV_WR_DP1_R
CNV_WR_DN0 R6116 1 2 Do Not Stuff CNV_WR_DN0_R
CNV_WR_DP0 R6118 1 2 Do Not Stuff CNV_WR_DP0_R
CNV_WR_CLKN R6119 1 2 Do Not Stuff CNV_WR_CLKN_R
CNV_WR_CLKP R6120 1 2 Do Not Stuff CNV_WR_CLKP_R
WLAN_PCIE_TX_P C6115 1 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_P_C
WLAN_PCIE_TX_N C6102 1 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_N_C
WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N
CNV_WT_DN1 R6121 1 2 Do Not Stuff CNV_WT_DN1_R
CNV_WT_DP1 R6122 1 2 Do Not Stuff CNV_WT_DP1_R
CNV_WT_DN0 R6123 1 2 Do Not Stuff CNV_WT_DN0_R
CNV_WT_DP0 R6124 1 2 Do Not Stuff CNV_WT_DP0_R
CNV_WT_CLKN R6125 1 2 Do Not Stuff CNV_WT_CLKN_R
CNV_WT_CLKP R6126 1 2 Do Not Stuff CNV_WT_CLKP_R

3D3V_WLAN
2017.10.16
Andy share CNV_DET connect to CNV_RST PIN .
Need to confirm Hi det/low det to ph/pl
R6132 1 DY Do Not Stuff CNV_DET#
CNV_RF_RESET#
CLKREQ_CNV#
R6127 1 22R2J-2-GP CNV_BRI_RSP
R6112 1 22R2J-2-GP CNV_RGI_RSP
CNV_BRI_RSP_R
CNV_RGI_DT
CNV_RGI_RSP_R
CNV_BRI_DT_CON
SUS_CLK_WLAN R6135 1 2 33R2J-2-GP SUS_CLK
WLAN_RST# R6131 1 2 Do Not Stuff PLT_RST#
BT_RADIO_DIS#_R
WLAN_WIGIG60GHZ_DIS#_R
PULSAR_38P4M_REFCLK
3D3V_WLAN

CNV_RF_RESET# 1 R6101 75KR2F-GP
CLKREQ_CNV# 1 R6102 75KR2F-GP

WLAN1
SKT-NGFF75P-196-GP-U
062.10003.00R1

Selek CFLH N17P

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini card-WLAN
Size: Custom
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 61 of 105

SSID = Wireless

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

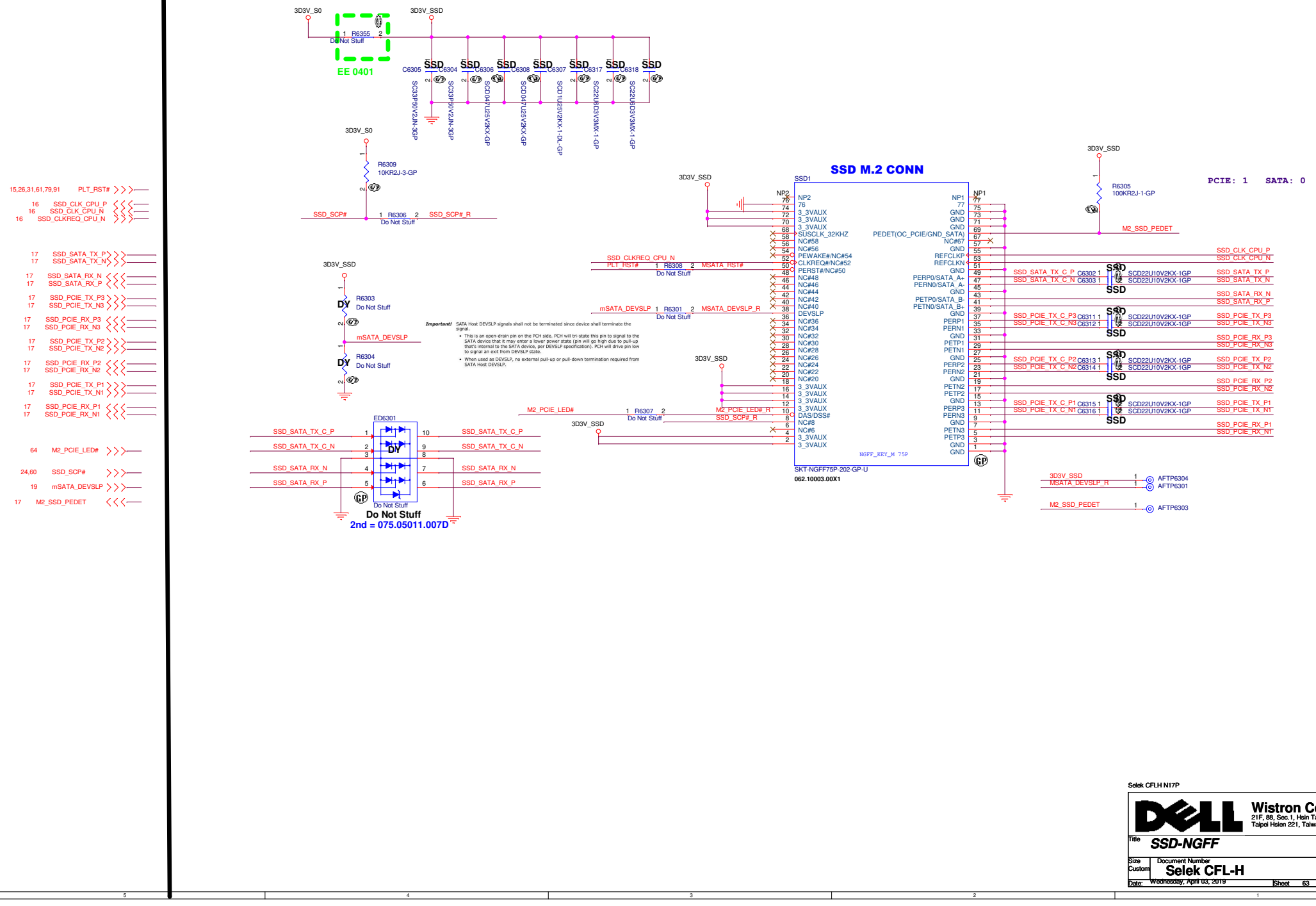
Title: ***(Reserved)WWAN***

Size	Document Number	Rev
A	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 62 of 105

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA



Selek CFLH N17P

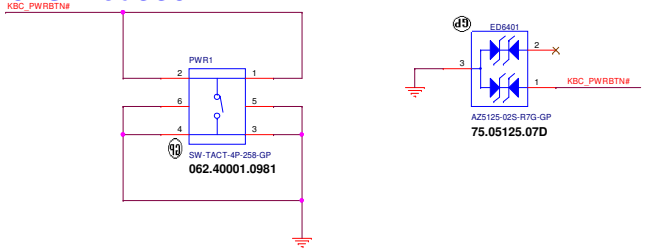
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SSD-NGFF		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 63 of 105	

SSID = User.Interface

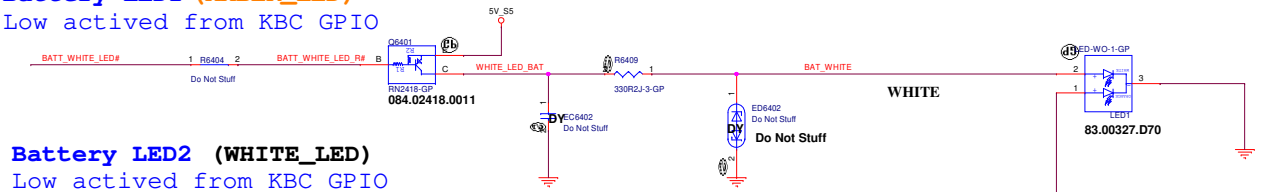
Power button

NONE FINGER PRINT 才會上件



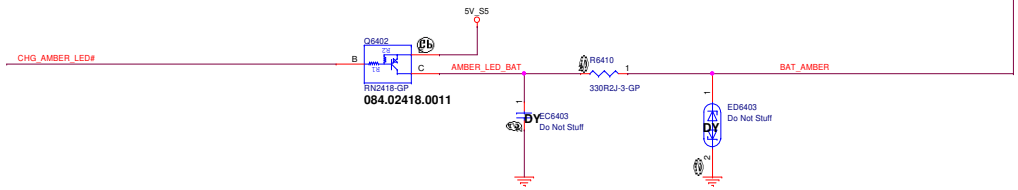
Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

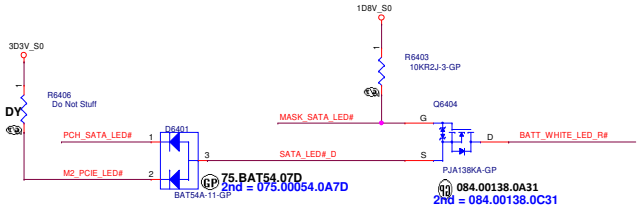


Battery LED2 (WHITE_LED)

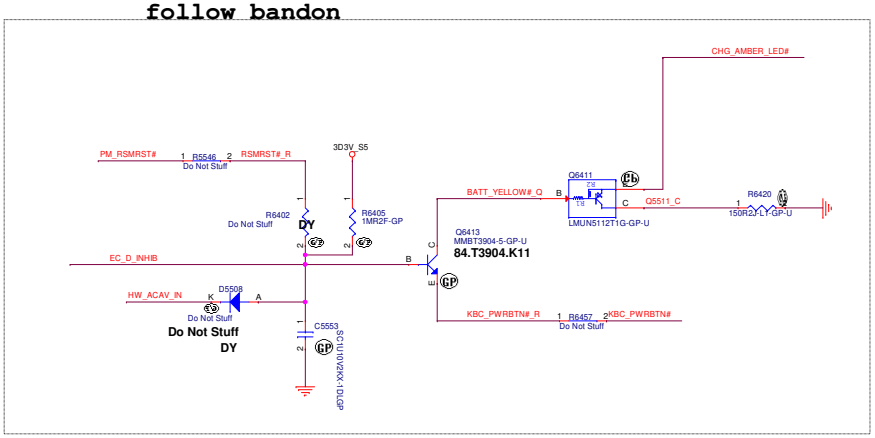
Low actived from KBC GPIO



SATA LED



M-BIST for G10 (Proposed schematic) follow bandon



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Light Bar/Power Button

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 64 of 105

Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

5V_S0 → R6502 (POLYSW-1D1A8V-9-GP) → +5V_KB_BL

69.48001.081
2nd = 69.50011.081
KBBL

Q6501 SI2301BDS-T1-GE3-GP — KBBL
X01 20161228 change

+5V_KB_BL
KB_LED_DET_C
KB_BL_CTRL#
KBBL1 STM-CON4-2-GP
020.K0311.0004

D6506 DY
D6507 DY

24 KSI[0..7]
24 KSO[0..16]

20 KB_DET#

AFTP6542 KSI7
AFTP6543 KSI6
AFTP6544 KSI4
AFTP6545 KSI2
AFTP6546 KSI5
AFTP6547 KSI1
AFTP6550 KSI3
AFTP6548 KSI0
AFTP6549 KSO5
AFTP6551 KSO4
AFTP6552 KSO7
AFTP6553 KSO6
AFTP6554 KSO8
AFTP6555 KSO3
AFTP6558 KSO1
AFTP6556 KSO2
AFTP6557 KSO0
AFTP6559 KSO12
AFTP6560 KSO15
AFTP6561 KSO10
AFTP6562 KSO13
AFTP6564 KSO14
AFTP6563 KSO9
AFTP6565 KSO11
AFTP6566 KSO16

CAP_LED
AFTP6541

KB1 STAR-CON30-2-GP
20.K0750.030

KB_BL_CTRL#
Q6501 AO3418L-GP — 84.03418.A31
24 KB_LED_PWM
R6509 Do Not Stuff DY
X01 20170105 change

17 KB_BL_DET
R6507 51KR2J-1-GP
KBBL
R6508 100KR2J-1-GP
KB_LED_DET_C
C6504 Do Not Stuff DY

+5V_KB_BL
KB_BL_CTRL#
AFTP6529
AFTP6530

CAP LED Control
LOW actived from KBC GPIO

X02 0414

24 CAP_LED#_R
R6512 Do Not Stuff
CAP_LED_R#
Q6505 PJA138K-GP — 084.02418.0011
5V_S5
CAP_LED_Q
R6513 1KR2J-1-GP
CAP_LED
CAP_LED_Q
EC6507 DY Do Not Stuff

Main Func = TPAD

3D3V_S0 → R6502 Do Not Stuff → NON TP_WAKE → TP_VDD
3D3V_S5 → R6514 Do Not Stuff → TP_WAKE

GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

EC I2C
I2C

TP_VDD
RN6501 Do Not Stuff

24 DAT_TP_SIO_I2C_CLK
24 CLK_TP_SIO_I2C_DATA
R6515 Do Not Stuff
R6516 Do Not Stuff
I2C0_SCL_R
I2C0_SDA_R
20,66 CPU_I2C_SCL_P1
20,66 CPU_I2C_SDA_P1
R6505 Do Not Stuff
R6506 Do Not Stuff
NON TP_WAKE
NON TP_WAKE

EC6501 Do Not Stuff DY
D6508 DY
D6509 DY
D6510 DY
D6511 DY

TP_VDD
RN6503 SRN2K2J-1-GP

TP_VDD
C6505 SCD1U25V2KX-1-GP
I2C0_SCL_R
I2C0_SDA_R
15,24 TP_WAKE_KBC#
24 PTP_DISB#
TP1 FITWO-CON8-16-GP
020.K0255.0008
AFTP6540

Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low
~~and check if there is PU~~ on TPAD side.

X02 0415

TP_VDD
R6511 10KR2J-3-GP
TP_WAKE_KBC#

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

TP_VDD → AFTP6531
I2C0_SCL_R → AFTP6534
I2C0_SDA_R → AFTP6535
TP_WAKE_KBC# → AFTP6536
PTP_DISB# → AFTP6537

Selek CFLH N17P

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

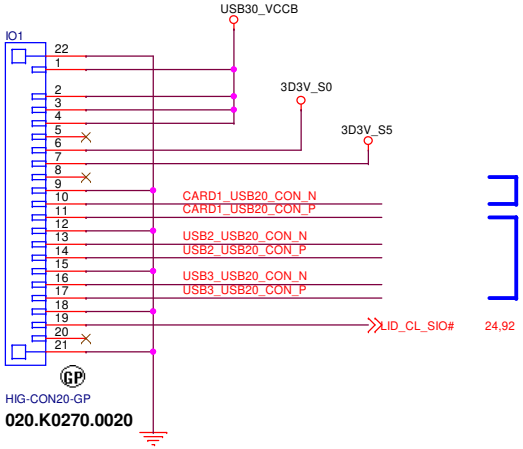
Title: Key Board&Touch Pad
Size: Custom | Document Number: Selek CFL-H | Rev: A00
Date: Wednesday, April 03, 2019 | Sheet 65 of 105

18 USB3_USB20_P
18 USB3_USB20_N
18 USB2_USB20_P
18 USB2_USB20_N

18 CARD1_USB20_N
18 CARD1_USB20_P

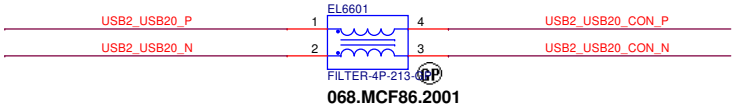
20,65 CPU_I2C_SCL_P1
20,65 CPU_I2C_SDA_P1

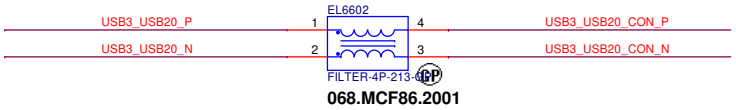
44 BT_PWR_IN-
44 BT_PWR_IN+

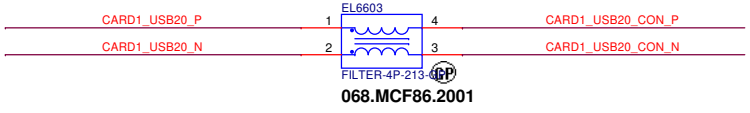


Cardreader

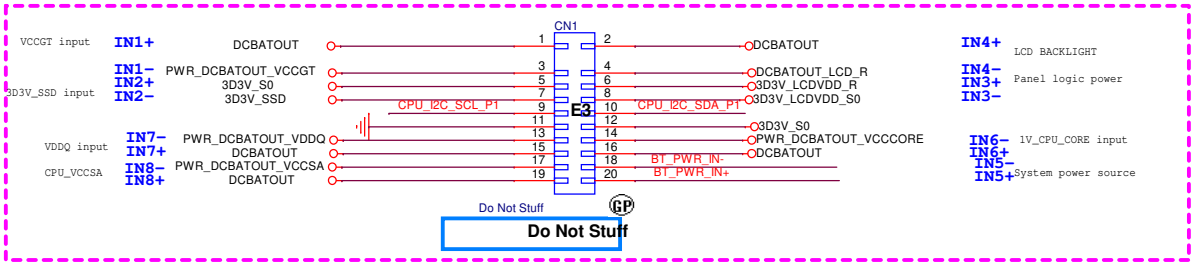
USB 2.0 Gen1 *2







E3 reserve



Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 66 of 105

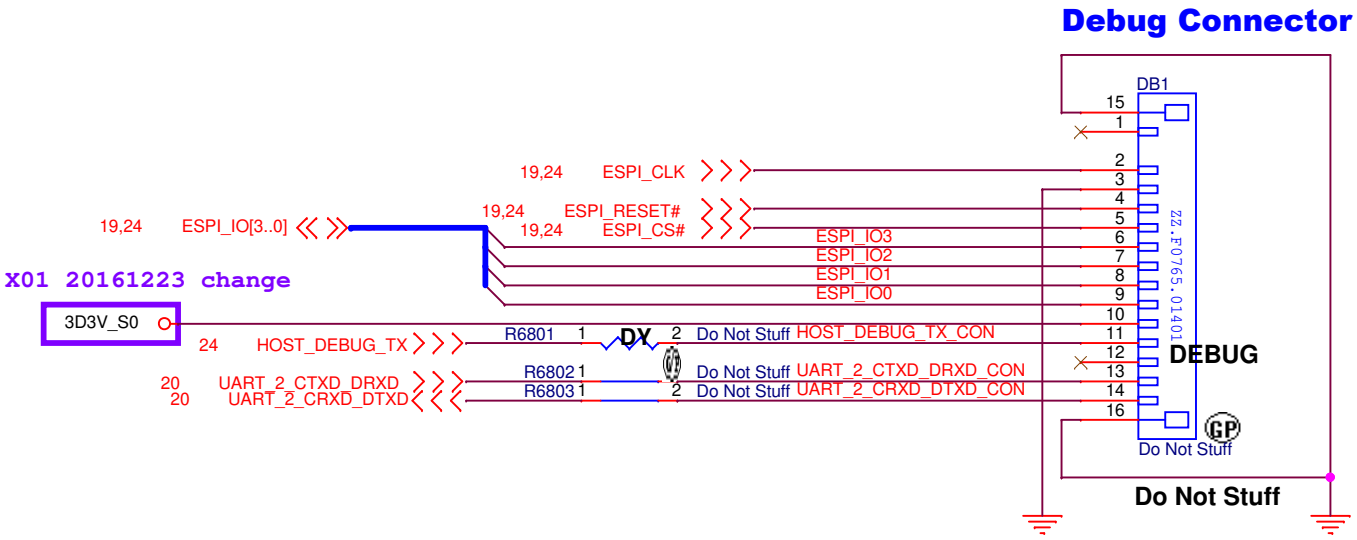
Main Func = Hall Sensor

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Hall Sensor*	
Size: A	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 67 of 105	

Main Func = Debug



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*		
Size: A4	Document Number: **Selek CFL-H**	Rev: **A00**
Date: Wednesday, April 03, 2019	Sheet 68 of 105	

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *Reserved*

Size	Document Number	Rev
A4	Selek CFL-H	A00

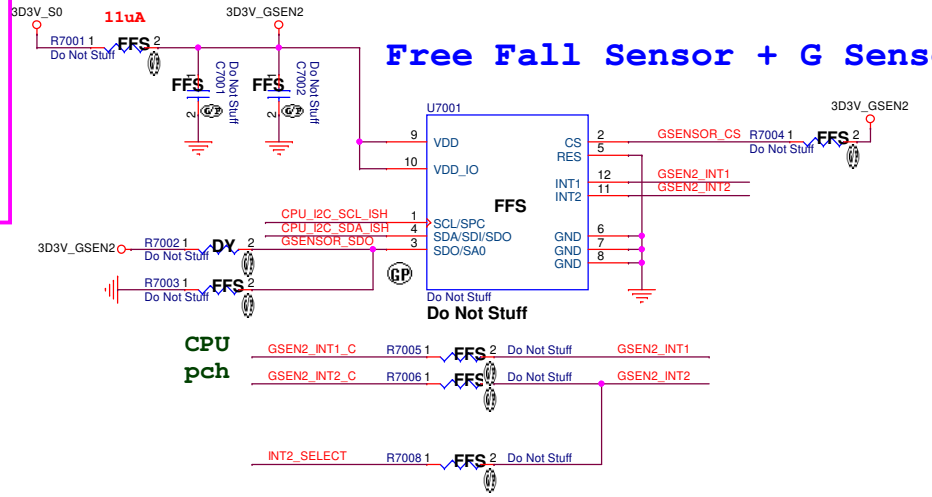
Date: Wednesday, April 03, 2019 Sheet 69 of 105

SSID = Free Fall Sensor

20 GSEN2_INT1_C
20 GSEN2_INT2_C
20 CPU_I2C_SDA_ISH
20 CPU_I2C_SCL_ISH
60 FFS_INT2_Q

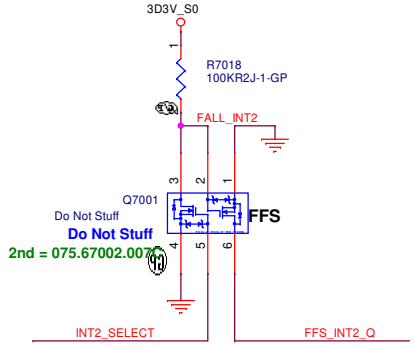
20180726 need DELL GPIO table

Free Fall Sensor + G Sensor



CPU pch

Please help to close with U6602



Selek CFLH N17P

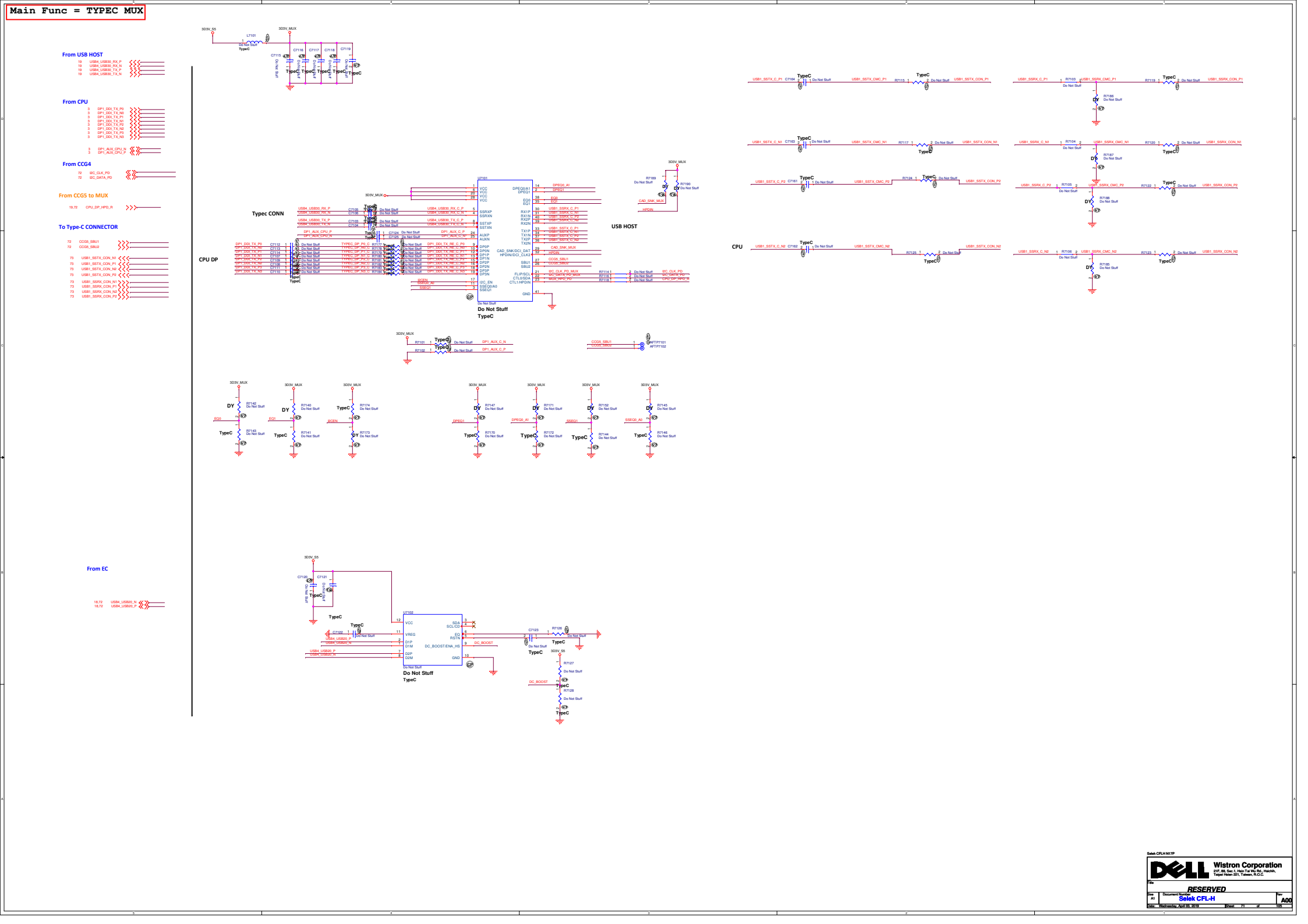
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

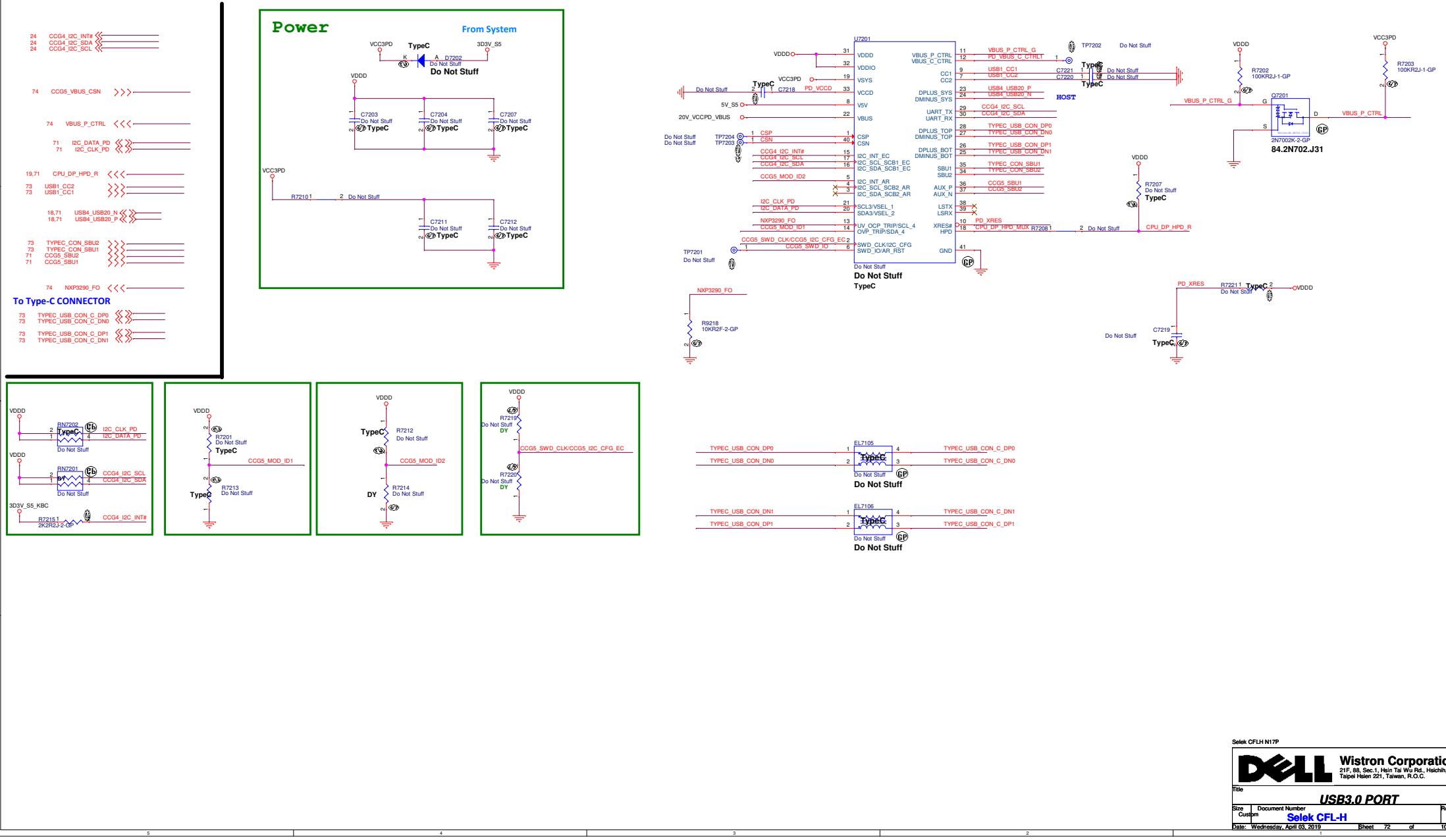
Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 70 of 105

Main Func = TYPEC MUX



Main Func = TYPEC CONTROLLER



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 PORT

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 72 of 105

Main Func = TYPEC CONNECTOR

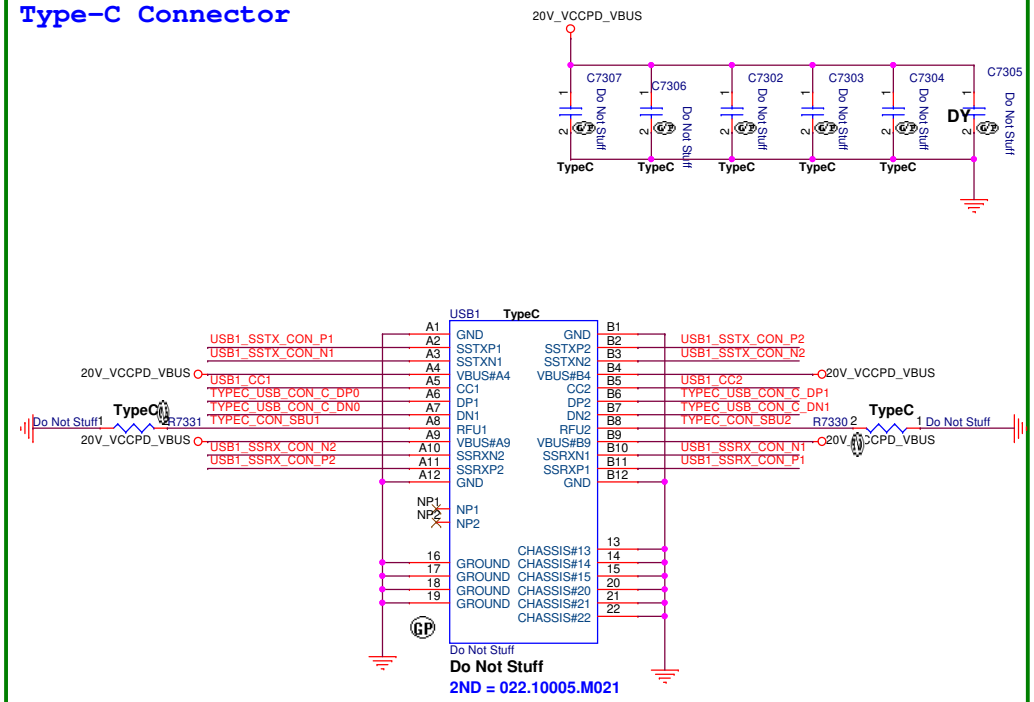
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2

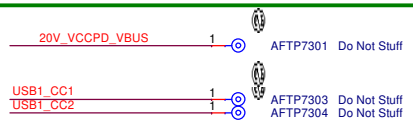
72 TYPEC_CON_SBU1
72 TYPEC_CON_SBU2
72 USB1_CC1
72 USB1_CC2

From USB2.0/ I2C Mux

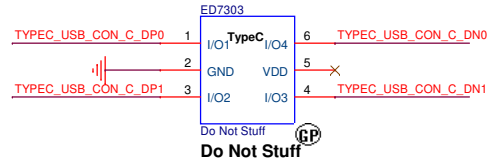
72 TYPEC_USB_CON_C_DP0
72 TYPEC_USB_CON_C_DN0
72 TYPEC_USB_CON_C_DP1
72 TYPEC_USB_CON_C_DN1

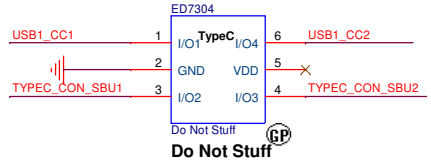
Type-C Connector



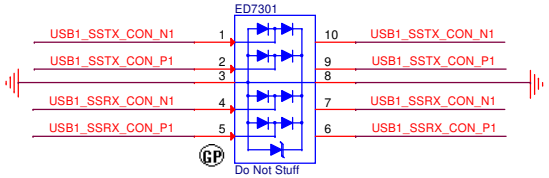


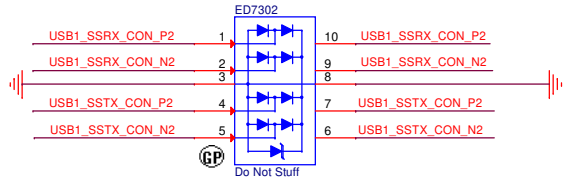
EMI





USB3.1 ESD





Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TYPEC CONN

Size	Document Number	Rev
A3	Selek CFL-H	A00

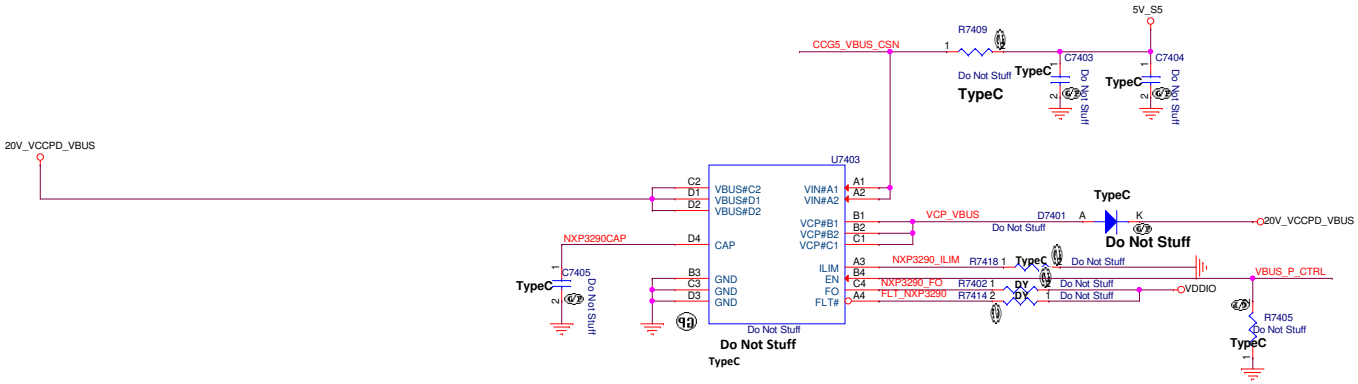
Date: Wednesday, April 03, 2019 Sheet 73 of 105

Main Func = LPS

72 VBUS_P_CTRL

72 NXP3290_FO

72 CCG5_VBUS_CSN



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPS

Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 74 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)Thunderbolt (5/5)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 75 of 105

- PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
PEX_DVDD Supply Rail					
GB4C-128, GB4D-128	1.0 µF[1] X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1] X6S	0201W	12	0	Under GPU
	4.7 µF X6S	0603	0	2	Near GPU
	4.7 µF X6S	0603	3	0	Under GPU
	10 µF X5R	0805	0	1	Midway between GPU and power supply
	10 µF X6S	0805	3	0	Near GPU
	22 µF X5R	0805	0	1	Midway between GPU and power supply
	22 µF X6S	0805	2	0	Near GPU

PEX_HVDD Supply Rail						
GB4C-128, GB4D-128	1.0 µF[1]	X6S	0402 or 0201W	0	4	Under GPU
	0.47 µF[1]	X6S	0201W	13	0	Under GPU
	4.7 µF	X6S	0603	0	2	Near GPU
	4.7 µF	X6S	0603	3	0	Under GPU
	10 µF	X5R	0805	0	2	Midway between GPU and power supply
	10 µF	X6S	0805	3	0	Near GPU
	22 µF	X5R	0805	0	1	Midway between GPU and power supply
	22 µF	X6S	0805	2	0	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

EMI Reserved
VGA_RST#
EC7601
1D0 Do Not Stuff

15,24,86 DGPU_PWROK
16 CLK_PCIE_PEG_REQ#
79 VGA_RST#
16 GFX_CLK_CPU_P
16 GFX_CLK_CPU_N

3 GFX_PCIE_RX_P7 / 3 GFX_PCIE_RX_N7
3 GFX_PCIE_RX_P6 / 3 GFX_PCIE_RX_N6
3 GFX_PCIE_RX_P5 / 3 GFX_PCIE_RX_N5
3 GFX_PCIE_RX_P4 / 3 GFX_PCIE_RX_N4
3 GFX_PCIE_RX_P3 / 3 GFX_PCIE_RX_N3
3 GFX_PCIE_RX_P2 / 3 GFX_PCIE_RX_N2
3 GFX_PCIE_RX_P1 / 3 GFX_PCIE_RX_N1
3 GFX_PCIE_RX_P0 / 3 GFX_PCIE_RX_N0

3 GFX_PCIE_TX_CON_P7 / 3 GFX_PCIE_TX_CON_N7
3 GFX_PCIE_TX_CON_P6 / 3 GFX_PCIE_TX_CON_N6
3 GFX_PCIE_TX_CON_P5 / 3 GFX_PCIE_TX_CON_N5
3 GFX_PCIE_TX_CON_P4 / 3 GFX_PCIE_TX_CON_N4
3 GFX_PCIE_TX_CON_P3 / 3 GFX_PCIE_TX_CON_N3
3 GFX_PCIE_TX_CON_P2 / 3 GFX_PCIE_TX_CON_N2
3 GFX_PCIE_TX_CON_P1 / 3 GFX_PCIE_TX_CON_N1
3 GFX_PCIE_TX_CON_P0 / 3 GFX_PCIE_TX_CON_N0

1D8V_AON_S0
R7604 10KR2J-L-GP
DGPU_PWROK
CLK_PCIE_PEG_REQ#
Q7601 PJA138KA-GP 084.00138.0A31
MAX Vth=1V
VGA_RST#
PEG_CLKREQ_dGPU#
GFX_CLK_CPU_P
GFX_CLK_CPU_N

GPU1A 1 OF 17

GFX_PCIE_RX_P0 / GFX_PCIE_RX_N0	C7601 C7606 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P0 / GFX_PCIE_RX_CON_N0	AK14 / AJ14 PEX_TX0 / PEX_TX0*
GFX_PCIE_TX_CON_P0 / GFX_PCIE_TX_CON_N0			AN12 / AM12 PEX_RX0 / PEX_RX0*
GFX_PCIE_RX_P1 / GFX_PCIE_RX_N1	C7607 C7608 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P1 / GFX_PCIE_RX_CON_N1	AH14 / AG14 PEX_TX1 / PEX_TX1*
GFX_PCIE_TX_CON_P1 / GFX_PCIE_TX_CON_N1			AN14 / AM14 PEX_RX1 / PEX_RX1*
GFX_PCIE_RX_P2 / GFX_PCIE_RX_N2	C7613 C7614 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P2 / GFX_PCIE_RX_CON_N2	AK15 / AJ15 PEX_TX2 / PEX_TX2*
GFX_PCIE_TX_CON_P2 / GFX_PCIE_TX_CON_N2			AP14 / AP15 PEX_RX2 / PEX_RX2*
GFX_PCIE_RX_P3 / GFX_PCIE_RX_N3	C7615 C7616 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P3 / GFX_PCIE_RX_CON_N3	AL16 / AK16 PEX_TX3 / PEX_TX3*
GFX_PCIE_TX_CON_P3 / GFX_PCIE_TX_CON_N3			AN15 / AM15 PEX_RX3 / PEX_RX3*
GFX_PCIE_RX_P4 / GFX_PCIE_RX_N4	C7617 C7618 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P4 / GFX_PCIE_RX_CON_N4	AK17 / AJ17 PEX_TX4 / PEX_TX4*
GFX_PCIE_TX_CON_P4 / GFX_PCIE_TX_CON_N4			AN17 / AM17 PEX_RX4 / PEX_RX4*
GFX_PCIE_RX_P5 / GFX_PCIE_RX_N5	C7619 C7620 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P5 / GFX_PCIE_RX_CON_N5	AH17 / AG17 PEX_TX5 / PEX_TX5*
GFX_PCIE_TX_CON_P5 / GFX_PCIE_TX_CON_N5			AP17 / AP18 PEX_RX5 / PEX_RX5*
GFX_PCIE_RX_P6 / GFX_PCIE_RX_N6	C7621 C7622 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P6 / GFX_PCIE_RX_CON_N6	AK18 / AJ18 PEX_TX6 / PEX_TX6*
GFX_PCIE_TX_CON_P6 / GFX_PCIE_TX_CON_N6			AN18 / AM18 PEX_RX6 / PEX_RX6*
GFX_PCIE_RX_P7 / GFX_PCIE_RX_N7	C7625 C7626 SCD22U10V2KX-1GP	GFX_PCIE_RX_CON_P7 / GFX_PCIE_RX_CON_N7	AL19 / AK19 PEX_TX7 / PEX_TX7*
GFX_PCIE_TX_CON_P7 / GFX_PCIE_TX_CON_N7			AN20 / AM20 PEX_RX7 / PEX_RX7*

PEX_WAKE# AJ11
PEX_RST* AJ12
PEX_CLKREQ# AK12
PEX_REFCLK AL13
PEX_REFCLK* AK13
PEX_TX8 / PEX_TX8* AK20 / AJ20
PEX_RX8 / PEX_RX8* AP20 / AP21
PEX_TX9 / PEX_TX9* AH20 / AG20
PEX_RX9 / PEX_RX9* AN21 / AM21
PEX_TX10 / PEX_TX10* AK21 / AJ21
PEX_RX10 / PEX_RX10* AN23 / AM23
PEX_TX11 / PEX_TX11* AL22 / AK22
PEX_RX11 / PEX_RX11* AP23 / AP24
PEX_TX12 / PEX_TX12* AK23 / AJ23
PEX_RX12 / PEX_RX12* AN24 / AM24
PEX_TX13 / PEX_TX13* AH23 / AG23
PEX_RX13 / PEX_RX13* AN26 / AM26
PEX_TX14 / PEX_TX14* AK24 / AJ24
PEX_RX14 / PEX_RX14* AP26 / AP27
PEX_TX15 / PEX_TX15* AL25 / AK25
PEX_RX15 / PEX_RX15* AN27 / AM27

Do Not Stuff

PCIE/PLL DIGITAL PWR 1V Interface
PEX_DVDD_1 AG21
PEX_DVDD_2 AG23
PEX_DVDD_3 AG24
PEX_DVDD_4 AH25
PEX_CVDD_1 AG19
PEX_CVDD_2 AH21

PCIE/PLL ANALOG PWR 1.8V Interface
PEX_HVDD_1 AG13
PEX_HVDD_2 AG15
PEX_HVDD_3 AG16
PEX_HVDD_4 AG18
PEX_HVDD_5 AG25
PEX_HVDD_6 AH15
PEX_HVDD_7 AH18
PEX_HVDD_8 AH26
PEX_HVDD_9 AH27
PEX_HVDD_10 AJ27
PEX_HVDD_11 AL27
PEX_HVDD_12 AM28
PEX_HVDD_13 AN28
PEX_HVDD_14
PEX_PLL_HVDD AH12
PEX_TERMP AP29

R7607 Close to GPU
PEX_TERMP 1 R7607 2K49R2F-2-L-GP

1V_VGA_S0
1U*4 X6S Place under GPU
4.7U*2 X6S Place near GPU
10U*1 X5R Midway between GPU and VR
22U*1 X5R Midway between GPU and VR
0.47U*12 X6S Place under GPU
Change to 1uF 0201 X6S *6 use two 0201W 0.47uF X6s for each 0201W 1uF
4.7U*3 X6S Place under GPU
10U*3 X6S Place near GPU
22U*2 X6S Place near GPU

1D8V_VGA_S0
1U*4 X6S Place under GPU
4.7U*2 X6S Place near GPU
10U*2 X5R Midway between GPU and VR
22U*1 X5R Midway between GPU and VR
0.47U*13 X6S Place under GPU
Change to 1uF 0201 X6S *6 use two 0201W 0.47uF X6s for each 0201W 1uF
4.7U*3 X6S Place under GPU
10U*3 X6S Place near GPU
22U*2 X6S Place near GPU

1D8V_VGA_S0
0.1U*1 X5R Place under GPU
0.47U*1 X6S Place under GPU
no 0201W 0.47uF X6s,so change to 1uF 0201W X6s

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_960M_PEG (1/5)
Size: A2
Document Number: Selek CFL-H
Rev: A00
Date: Wednesday, April 03, 2019
Sheet 76 of 105

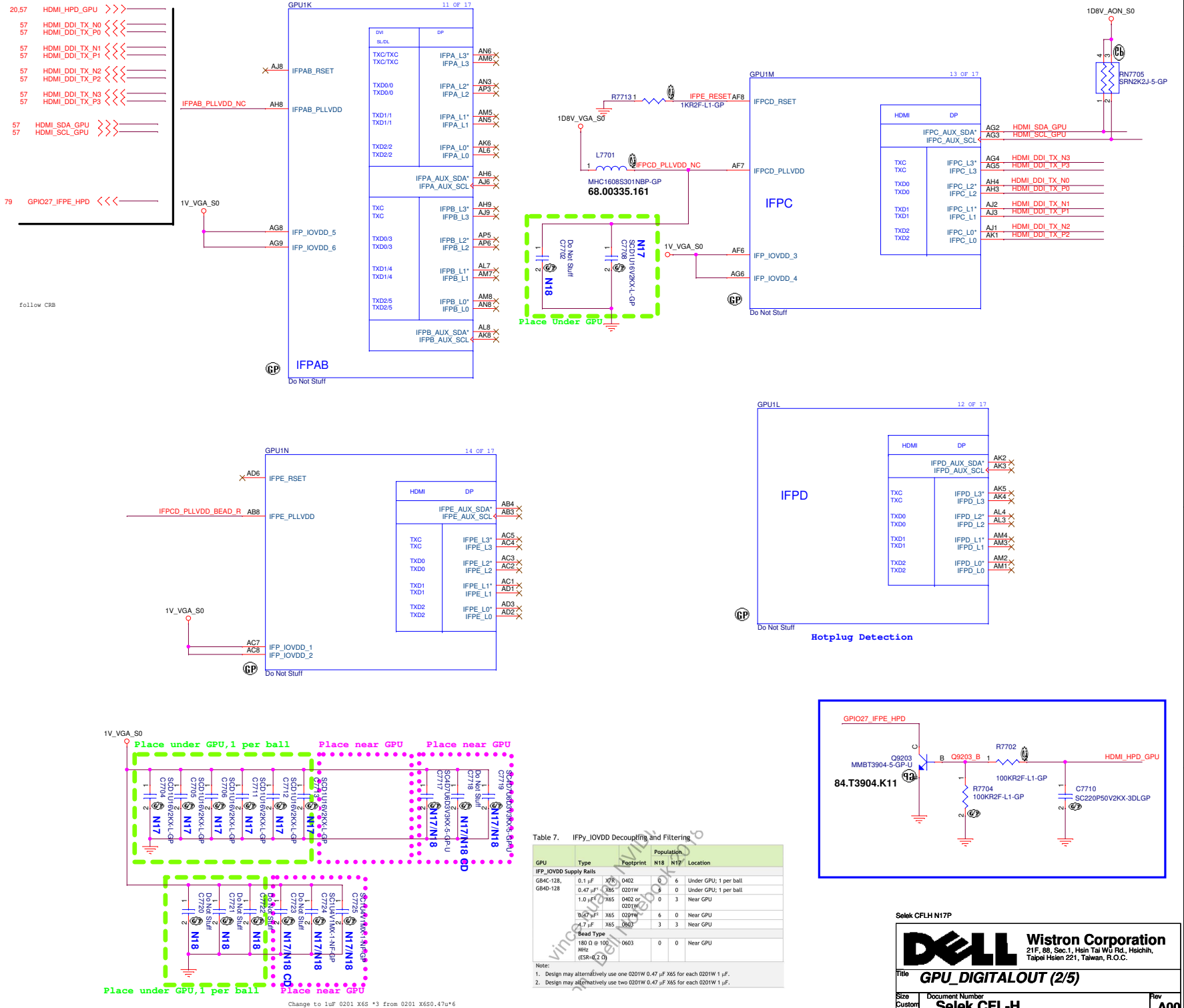


Table 7. IFPy_IOVDD Decoupling and Filtering

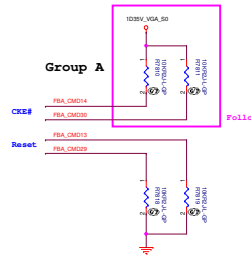
GPU	Type	Footprint	Population N18	Population N17	Location
IFP_IOVDD Supply Rails					
GB4C-128, GB4D-128	0.1 µF	X7R 0402	0	6	Under GPU; 1 per ball
	0.47 µF[1]	X6S 0201W	0	6	Under GPU; 1 per ball
	1.0 µF[2]	X6S 0402 or 0201W	0	3	Near GPU
	0.47 µF[2]	X6S 0201W	6	0	Near GPU
	4.7 µF	X6S 0603	3	3	Near GPU
	Bead Type				
	180 Ω @ 100 MHz (ESR=0.2 Ω)	0603	0	0	Near GPU

Note:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0201W 1 µF.
2. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Selek CFLH N17P

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU_DIGITALOUT (2/5)		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 77 of 105	

FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

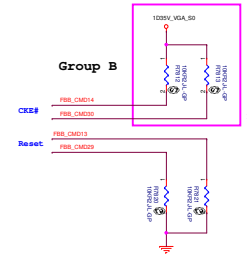


Table 4. Frame Buffer PLL3 Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
FB PLL Supply Rail for GDDR5					
G84C-128, G84D-128	0.1 uF	X7R 0402	0	3	Under GPU
	0.47 uF	X6S 0201W	3	0	Under GPU
	22 uF	X5R 0805	0	1	Near GPU
	10 uF	X6S 0805	1	0	Near GPU
	4.7 uF	X6S 0603	2	0	Near GPU
Bead Type					
	30 Ω (ESR) 2A (1)	0603	1	1	Near GPU

Notes:
1. Design may alternatively use one 0201W 0.47 µF X6S for each 0201W 1 µF.

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
FBVDDQ/Q Supply Rail for GDDR5					
G84C-128, G84D-128	0.47 µF[1]	X6S 0201W or 0201W	24	0	Under GPU
	1 µF[1]	X6S 0402 or 0201W	0	12	Under GPU
	10 µF	X6S 0603	4	4	Under GPU
	10 µF	X6S 0603	2	2	Near GPU
	22 µF	X6S 0603	5	5	Near GPU

Notes:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

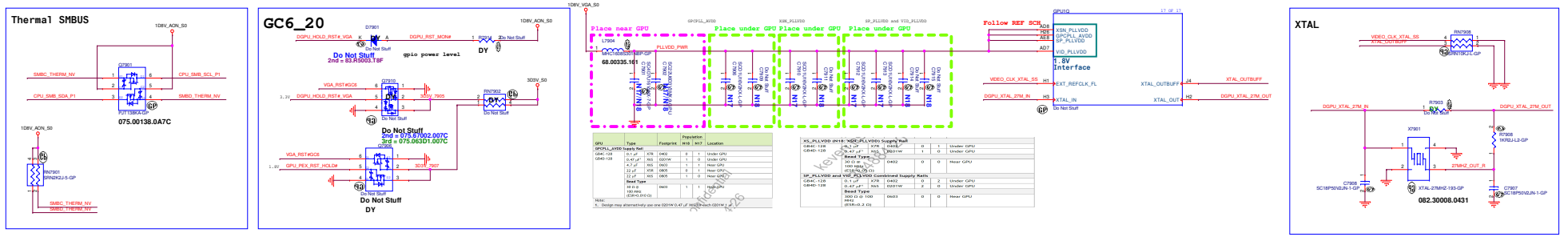
Selek CFLH N17P

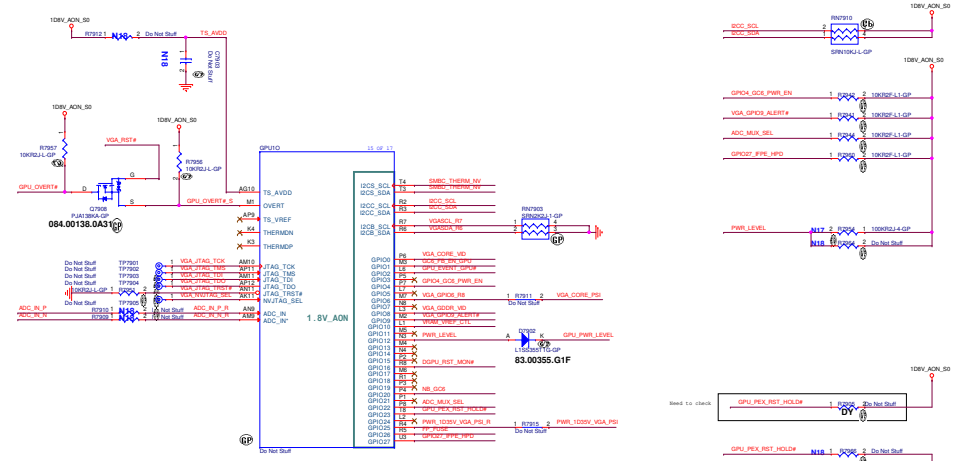
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: GPU_VRAM I/F (3/5)

Size: A1 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 02, 2008 | Sheet 7 of 105





Strap2	Strap1	Strap0	vendor	vendor number	wistron P/N	strap	GPU
L	L	L	Samsung	K4G80325FB-HC28	N1MMH$AA	0x0	N17P
L	L	H	Micron	MT51J256M32HF-80:B	MHVDX$AA	0x1	N18P
L	H	L	Hynix	H5GC8H24AJR-R2C	GVK6K$AA	0x2	N18P
L	L	L	Samsung	K4G80325FC-HC25	J62CN$AA	0x0	N18P

Table 3. N17P-G1/G0/G0-K1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	N/A	Post production ready
			Hynix	H5GC8H24MJR-R2C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver
			Hynix	H5GC8H24AJR-R0C	A-die	0x5	7 Gbps	N/A	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x5	8 Gbps	N/A	N/A	Substitution allowed with waiver

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.5V	Micron	MT51J256M32HF-80:B	B-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24AJR-R2C	A-die	0x2	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	N/A	Full	Production candidate

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000a)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	L	M	25 (0x0019)
H	M	M	26 (0x001A)

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

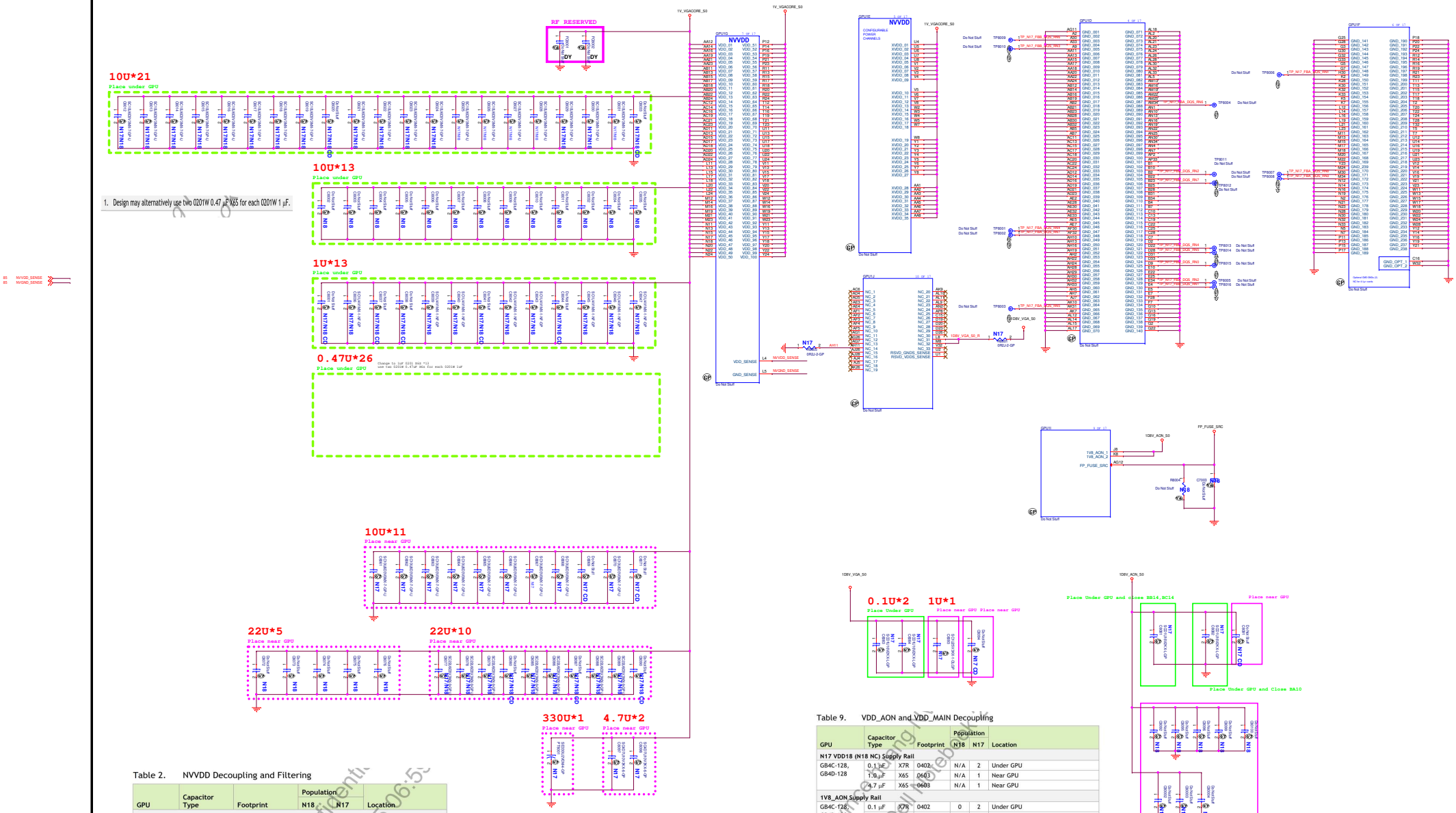
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: GPU_GPIO/STRAP

Size: A1 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 79 of 105



1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
NVVDD Supply Net					
GB4C-128, GB4D-128	10 µF	X6S 0603	34	21	Under GPU
	1 µF[1]	X6S 0402 or 0201W	0	13	Under GPU
	0.47 µF[1]	X6S 0402 or 0201W	26	0	Under GPU
	10 µF	X6S 0603	0	11	Near GPU
	22 µF	X6S 0805	15	10	Near GPU
	4.7 µF	X6S 0603	0	2	Near GPU
	330 µF	POS 7343	0	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population N18	Population N17	Location
N17 VDD18 (N18 NC) Supply Rail					
GB4C-128, GB4D-128	0.1 µF	X7R 0402	N/A	2	Under GPU
	1.0 µF	X6S 0603	N/A	1	Near GPU
	4.7 µF	X6S 0603	N/A	1	Near GPU
1V8_AON Supply Rail					
GB4C-128, GB4D-128	0.1 µF	X7R 0402	0	2	Under GPU
	0.47 µF	X6S 0201W	4	0	Under GPU
	1.0 µF[1]	X6S 0402 or 0201W	0	1	Near GPU
	0.47 µF[1]	X6S 0201W	6	0	Near GPU
	4.7 µF	X6S 0603	3	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 µF X6S for each 0201W 1 µF.

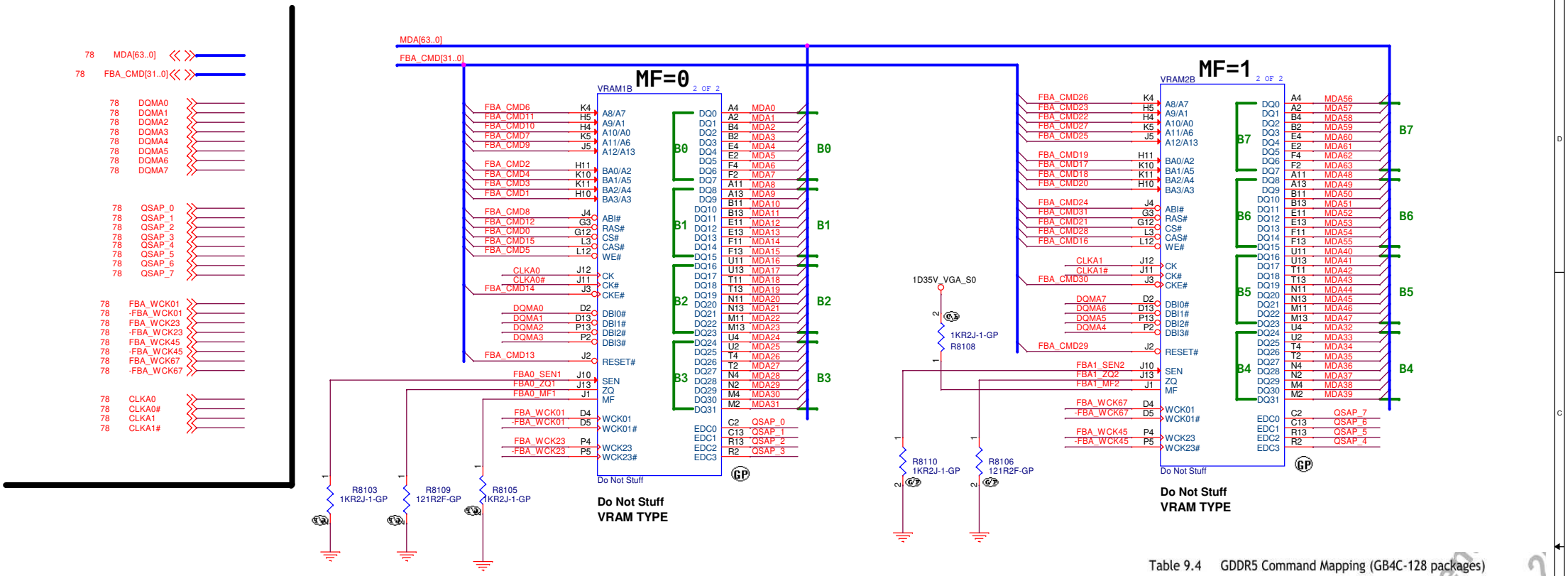
Selek CFLHN17P

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

GPU_POWER/GND (5/5)

Size: Custom | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 25, 2018 | Sheet 85 of 105



GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

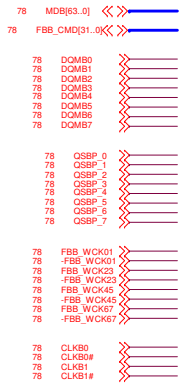
Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

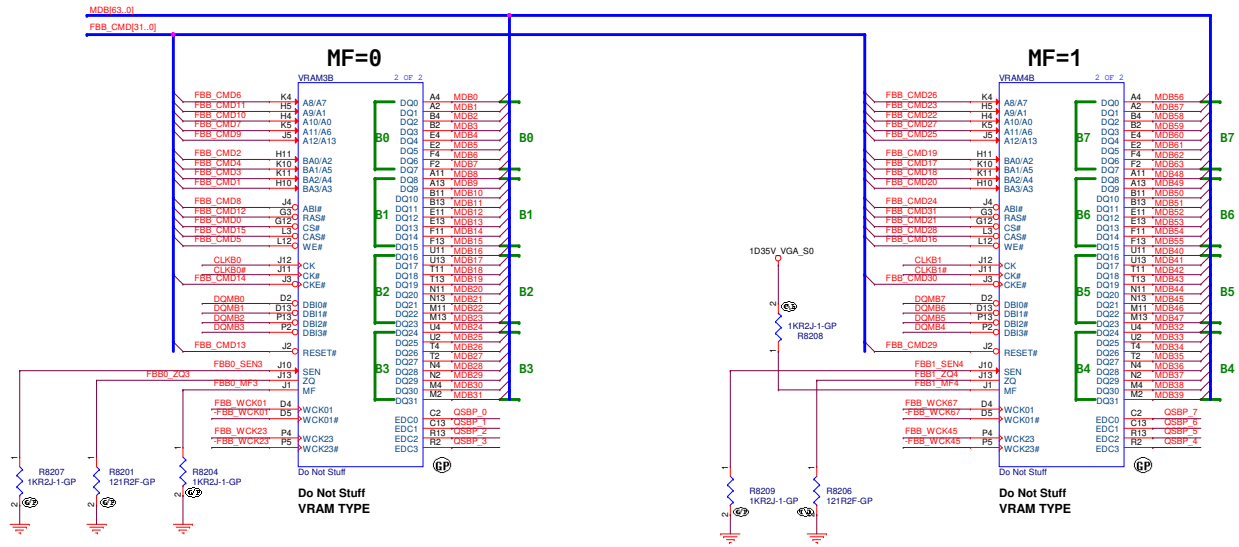
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM 1,2 (1/4)	
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 81 of 105	





GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)

GDDR5 CLK Mapping			
WCK01	WCK23 (WCK45)	WCK23	WCK01 (WCK67)
WCK01#	WCK23# (WCK45#)	WCK23#	WCK01# (WCK67#)
CK	CK		
CK#	CK#		

Others			
MF	MF	SEN	SEN
ZQ	ZQ	RESET#	RESET#

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

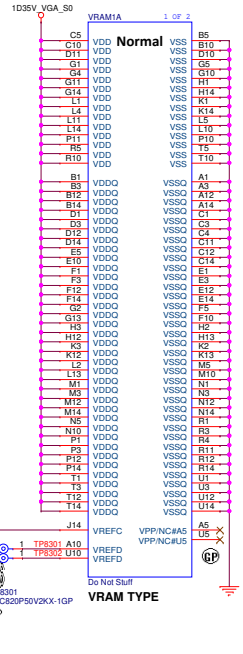
Selek CFLH N17P

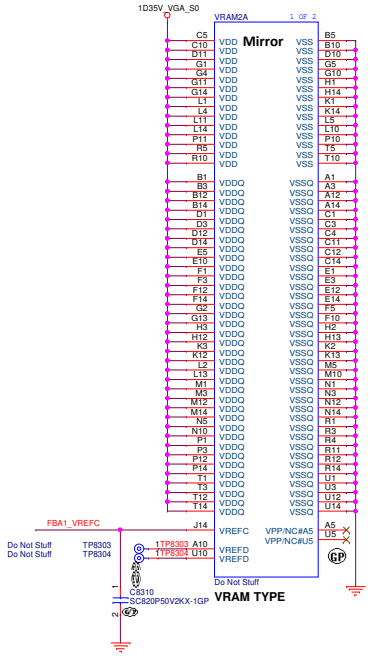
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM 3,4 (2/4)

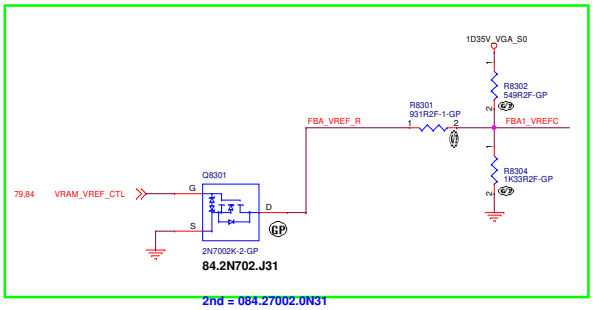
Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 82 of 105

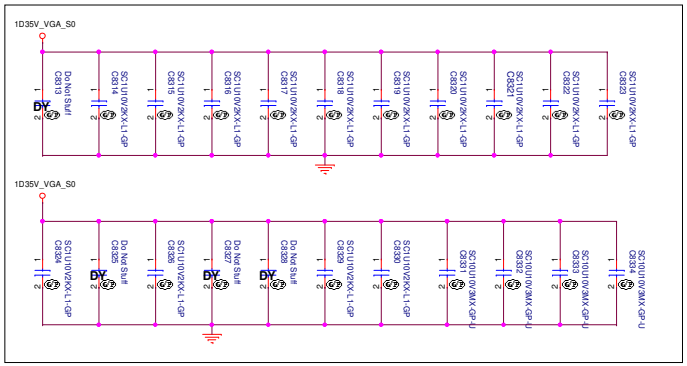




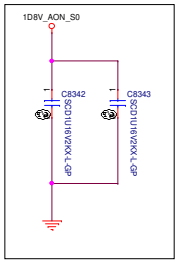
CLOSE TO VRAM



FOR VRAM1/ VRAM2

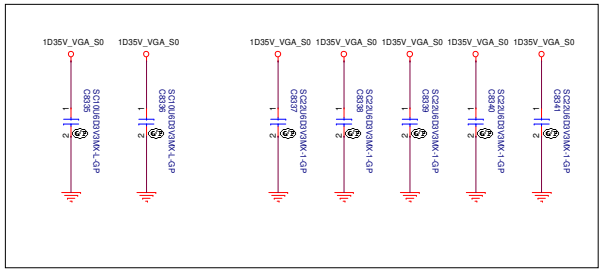


UNDER THE MEMORY



UNDER THE MEMORY

FOR VRAM1/ VRAM2



CLOSE TO THE MEMORY

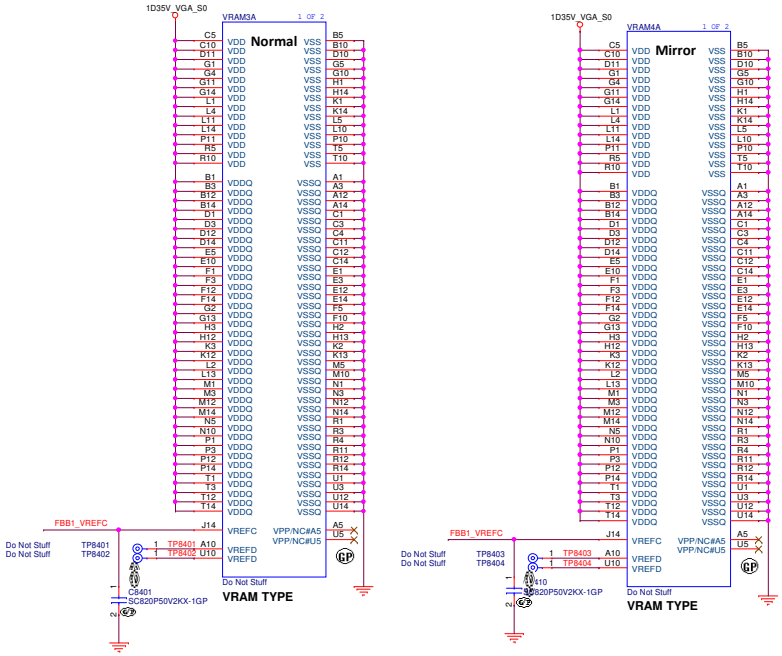
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

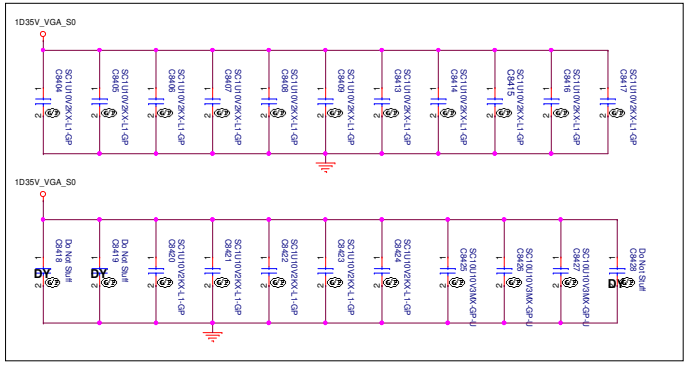
Title: *VGA Power A*

Size: A2 | Document Number: Selek CFL-H | Rev: A00

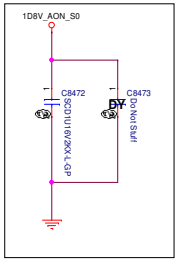
Date: Wednesday, April 03, 2019 | Sheet 83 of 105



FOR VRAM3/ VRAM4

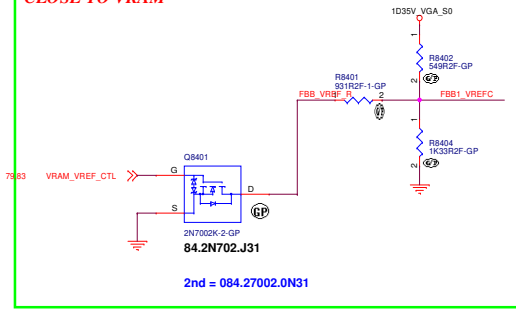


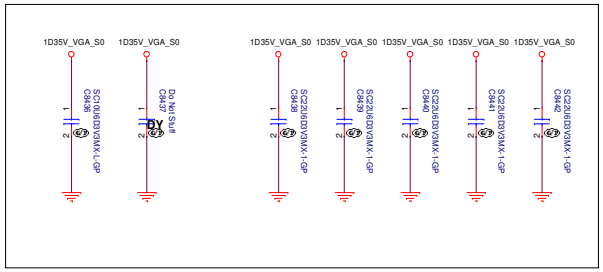
UNDER TO THE MEMORY



UNDER THE MEMORY

CLOSE TO VRAM





CLOSE TO THE MEMORY

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA Power B		
Size: A2	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 84 of 105	

OFFPAGE

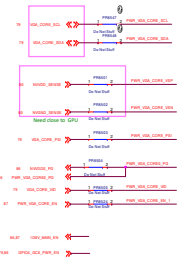


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels til	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.249
C	nF	0.1

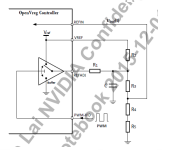
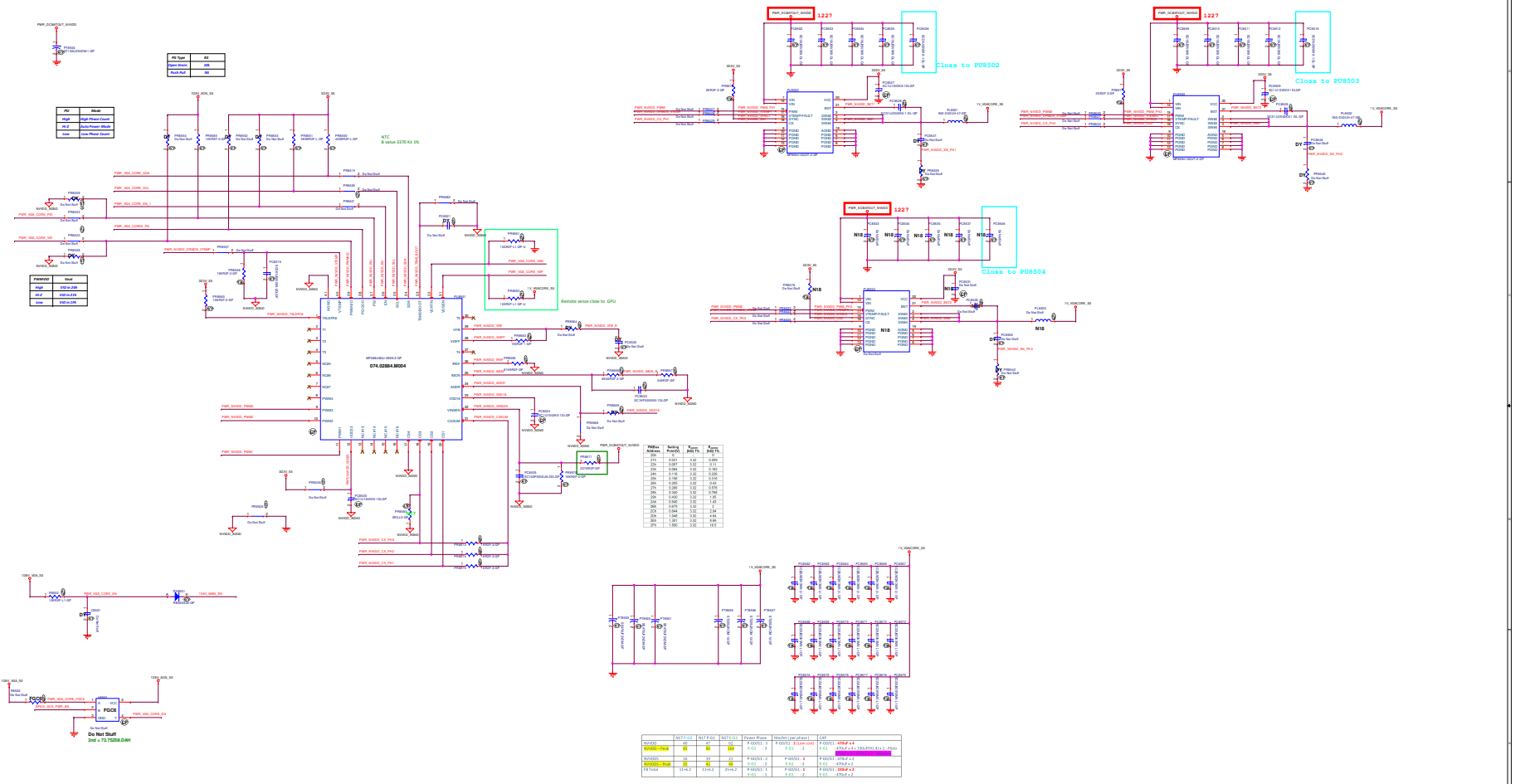


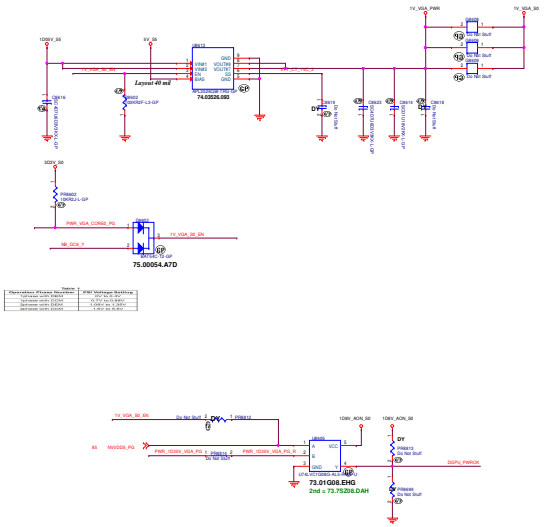
Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		
		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{OMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.249
C	nF	0.1



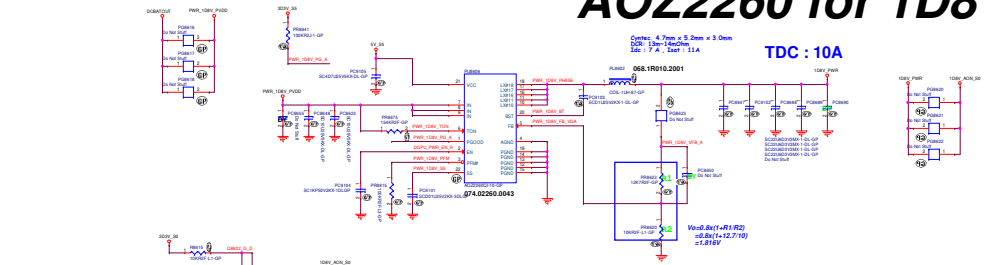
OFFPAGE

APL3526QB for 1V_VGA_S0

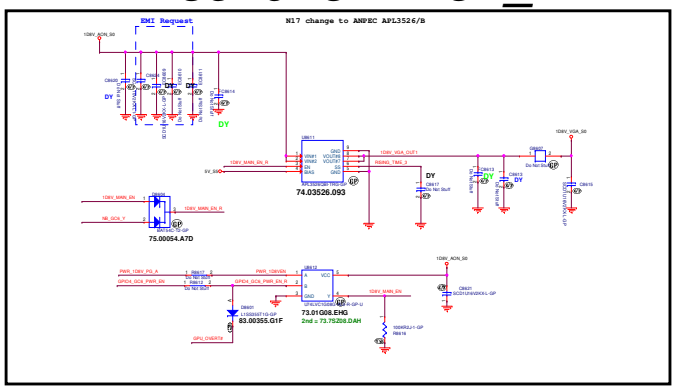


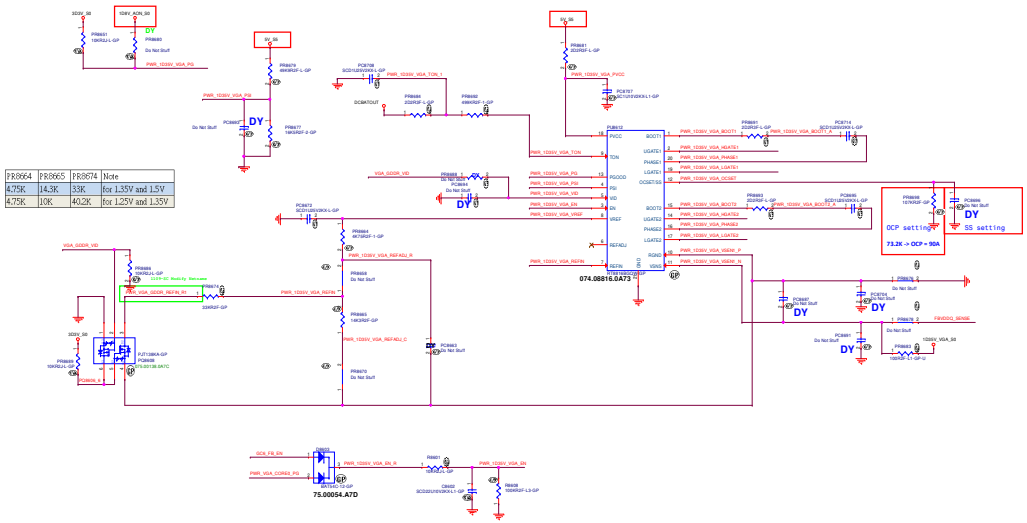
AOZ2260 for 1D8V_AON

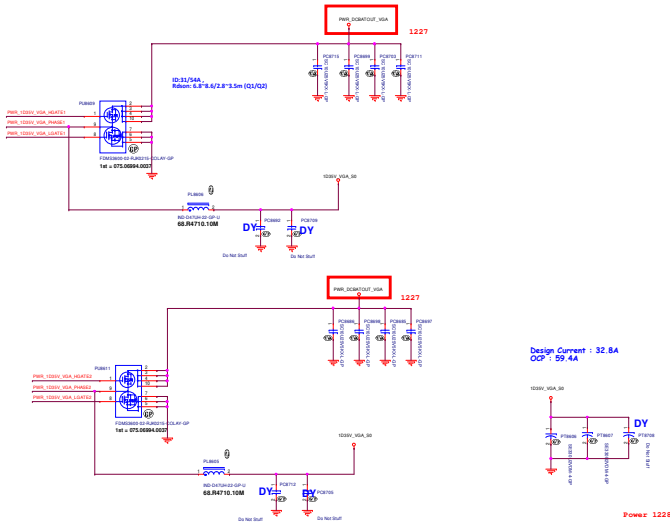
TDC : 10A



APL3526 for 1D8V_MAIN





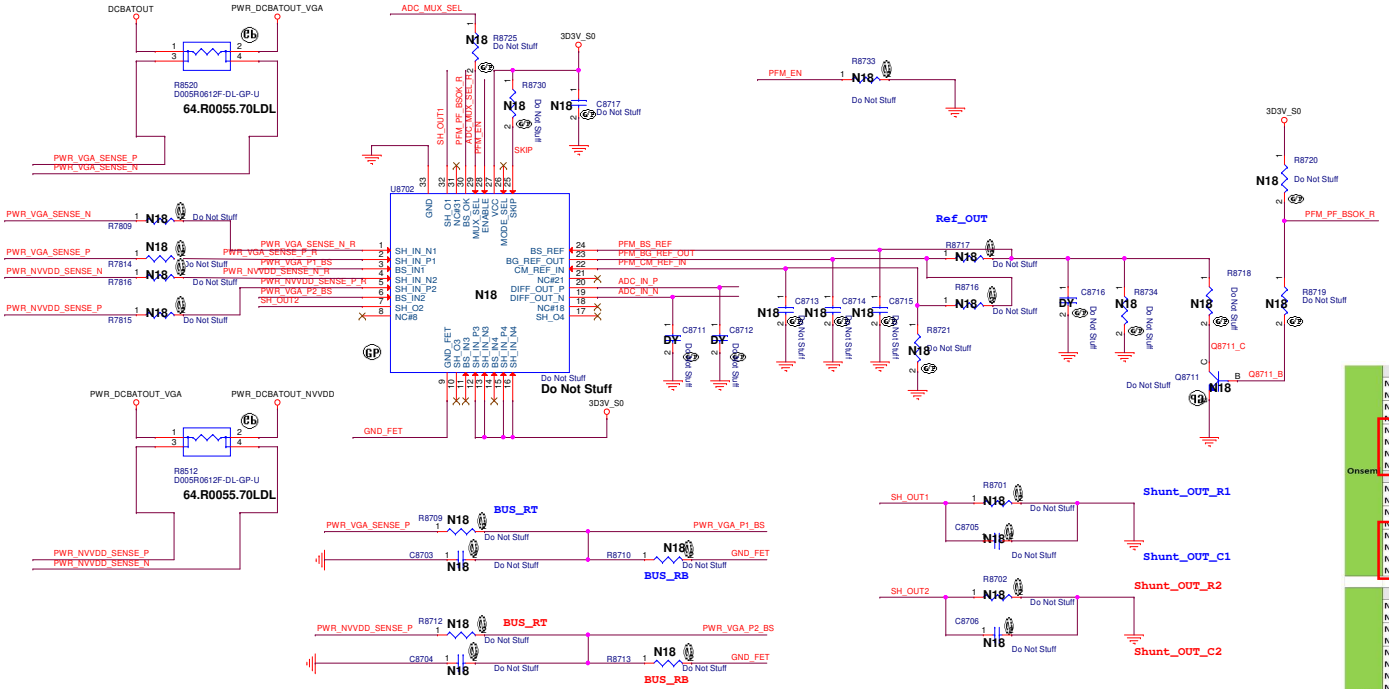


Design Current : 32.8A
OCP : 59.4A

Power: 1228

Quanta Computer Inc.			
PROJECT :	Selek CFL-H		REV : A00
Size	Document Number		
Date:	Sheet	of	

GPU GDDR 1D35V



	TGP Current (GPU sku)	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
Onsem	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	169Ω	15nF	750K	6.49K	100pF	243K
	N18E-G2, N18E-G2 MAX-Q			191Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			287Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	169Ω	15nF	750K	6.49K	100pF	
	N18E-G2, N18E-G2 MAX-Q			191Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			287Ω					

	TGP Current (GPU sku)	Rs1	Shunt in R1	Shunt out R1	Shunt out C1	Bus RT	Bus RB	Bus Cap	R Ref_out
upi	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	127Ω	15nF	750K	4.87K	100pF	324k
	N18E-G2, N18E-G2 MAX-Q			143Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			215Ω					
	NVVDD Current	Rs2	Shunt in R2	Shunt out R2	Shunt out C2	Bus RT	Bus RB	Bus Cap	
	N18E-G3, N18E-G3 MAX-Q	0.005Ω	100Ω	127Ω	15nF	750K	4.87K	100pF	
	N18E-G2, N18E-G2 MAX-Q			143Ω					
	N18E-G1, N18E-G1 MAX-Q N18E-G0, N18E-G0 MAX-Q			215Ω					

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Discharge

Size: A2 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 87 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *(Reserved)*

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 88 of 105

HS1
STF236R128H101-3-GP
34.4YG18.001

HS2
STF237R113H184-GP
434.0H70B.0001

H16
Do Not Stuff
Do Not Stuff

H15
Do Not Stuff
Do Not Stuff

SPR1
Do Not Stuff
DY
Do Not Stuff

SPR2
SPRING-43-GP-U
34.15J03.001

SPR3
Do Not Stuff
DY
Do Not Stuff

SPR4
Do Not Stuff
DY
Do Not Stuff

H1
Do Not Stuff
Do Not Stuff

H2
Do Not Stuff
Do Not Stuff

H4
Do Not Stuff
Do Not Stuff

H5
Do Not Stuff
Do Not Stuff

H6
Do Not Stuff
Do Not Stuff

H9
Do Not Stuff
Do Not Stuff

H10
Do Not Stuff
Do Not Stuff

H11
Do Not Stuff
Do Not Stuff

H12
Do Not Stuff
Do Not Stuff

H13
Do Not Stuff
Do Not Stuff

H14
Do Not Stuff
Do Not Stuff

EMI Request

5V_S5

EC8938 EC8936 EC8937 EC8939 EC8940

DY Do Not Stuff — SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

SB 20160831

5V_S0

EC8943 EC8941 EC8942 EC8944 EC8945

SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

EMI Request

DCBATOUT

EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909 EC8910

SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

EC8917 EC8914 EC8912 EC8915 EC8916 EC8911 EC8913

SCD1U25V2KX-L-GP

EMI Request

1D2V_S3

SB 20160822

EC8918 EC8919 EC8920 EC8921 EC8922 EC8923 EC8924 EC8925

SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

SC100P50V2JN-L-GP

SC1KP50V2KX-L-GP

SC1KP50V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

EMI Request

1D35V_VGA_S0

SB 20160822

EC8932 EC8930 EC8927 EC8931 EC8929 EC8933 EC8926 EC8928 EC8934 EC8935

SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

SC1KP50V2KX-L-GP

SCD1U25V2KX-L-GP

SCD1U25V2KX-L-GP

SC1KP50V2KX-L-GP

DY Do Not Stuff — SCD1U25V2KX-L-GP

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 89 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 90 of 105

SSID = TPM

19 PIRQA#
15 TPM_SPI_IRQ#
26,31,61,63,79 PLT_RST#
15,40 PM_SLP_S0#
15 SPI_CS_CPU_N2
15,21,25 SPI_SO_CPU
15,21,25 SPI_SI_CPU
15,25 SPI_CLK_CPU

reserve RTC Gen 9 reset circuit_20170814
leakage issue

3D3V_S5_PCH — R9148 — TPM — Do Not Stuff
3D3V_TPM_VHIO — R9140 — DY — Do Not Stuff

SPI_CS_CPU_N2 — R9130 — TPM — Do Not Stuff — SPI_CS2_TPM
SPI_SI_CPU — R9133 — TPM — Do Not Stuff — SPI_SI_TPM
SPI_SO_CPU — R9132 — TPM — Do Not Stuff — SPI_SO_TPM
SPI_CLK_CPU — R9138 — TPM — Do Not Stuff — SPI_CLK_TPM

Change to stuff vendor suggest 11/05

3D3V_TPM_VHIO — R9149 — DY — SPI_IRQ#_TPM2
Do Not Stuff

SPI_IRQ#_TPM2 — R9139 — DY — Do Not Stuff — TPM_SPI_IRQ#

3D3V_S0 — R9127 — TPM — Do Not Stuff
3D3V_S5 — R9126 — DY — Do Not Stuff

3D3V_TPM_VHIO
C9109 TPM Do Not Stuff
C9112 TPM Do Not Stuff
C9113 TPM Do Not Stuff

reserve for modern standby

3D3V_S5 — R9143 — TPM — Do Not Stuff
3D3V_TPM_VSB
C9106 TPM Do Not Stuff
C9108 TPM Do Not Stuff

U9102

8	VHIO	SDA/GPIO0	29 TPM_GPIO0 — R9141 DY Do Not Stuff PM_SLP_S0#
22	VHIO	SCL/GPIO1	30
1	VSB	PIRQ#/GPIO2	18 SPI_IRQ#_TPM2 — R9137 TPM Do Not Stuff PIRQA#
		GPIO3	6
		GPIO4	13
		PP/GPIO6	4
SPI_SI_TPM 21	MOSI/GPIO7		
SPI_SO_TPM 24	MISO		
SPI_CS2_TPM 20	SCS#/GPIO5		
SPI_CLK_TPM 19	SCLK		
PLT_RST# — R9136 TPM Do Not Stuff PLT_RST#_Q_TPM2 17	PLTRST#		
16	GND		
23	GND		
33	GND		
2	NC#2	NC#7	7
3	NC#3	NC#9	9
5	NC#5	NC#10	10
		NC#11	11
		NC#12	12
		NC#14	14
		NC#15	15
		NC#25	25
		NC#26	26
		NC#27	27
		NC#28	28
		NC#31	31
		NC#32	32

TPM
GP
Do Not Stuff
Do Not Stuff

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM2.0**

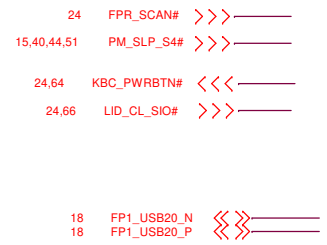
Size	Document Number	Rev
A4	Selek CFL-H	A00

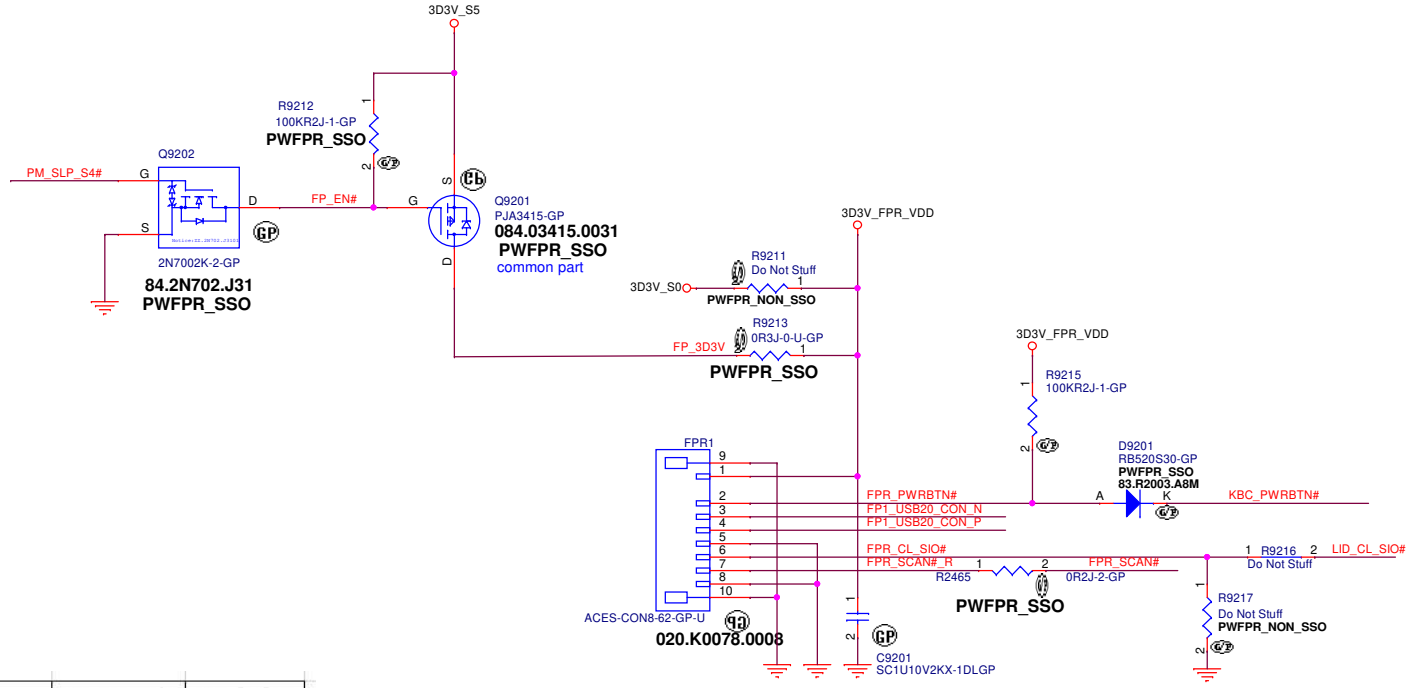
Date: Wednesday, April 03, 2019 Sheet 91 of 106

Main Func = FPR

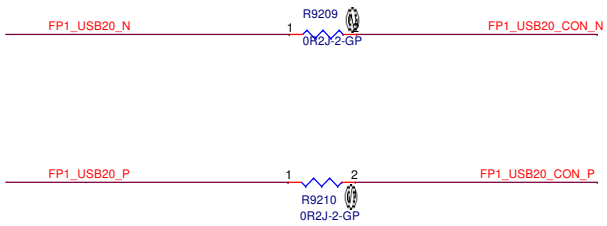
FBR(Botton side finger Print Sensor)

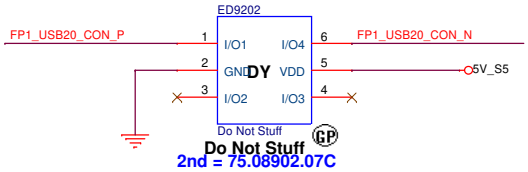
PWFPR_SSO: GOODIX module
PWFPR_NON_SSO: ELAN module(R9211 R9214 R9217)





	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0





GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)Finger Print

Size: A3 | Document Number: Selek CFL-H | Rev: A00

Date: Wednesday, April 03, 2019 | Sheet 92 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 93 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A4	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 94 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 95 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 96 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 97 of 105

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 98 of 105

Main Func = XDP

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_XDP;PCH_XDP*	
Size: A3	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 99 of 105	

Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ***Table of Content***

Size	Document Number	Rev
A	**Selek CFL-H**	**A00**

Date: Wednesday, April 03, 2019 Sheet 100 of 105

Selek CFLH N17P

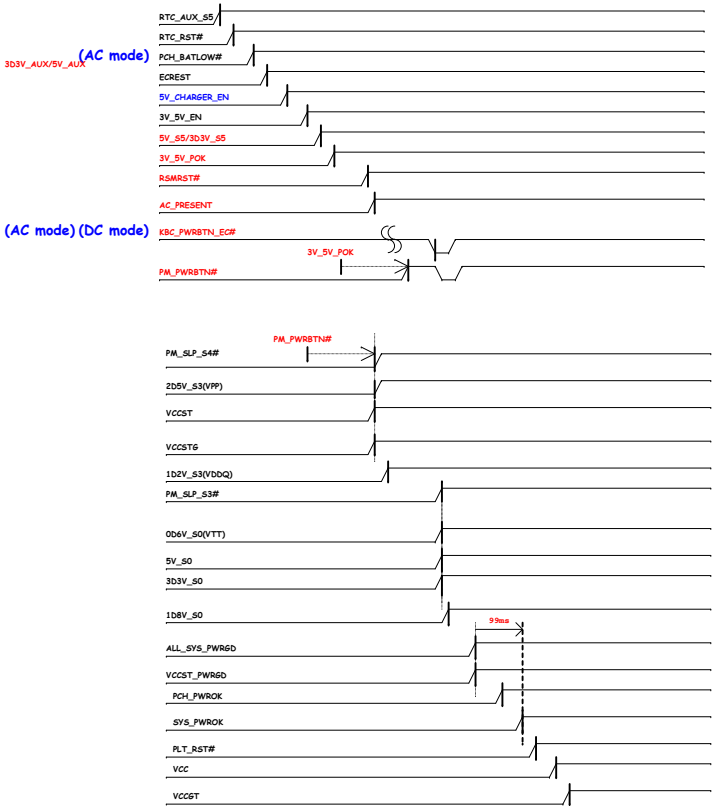
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

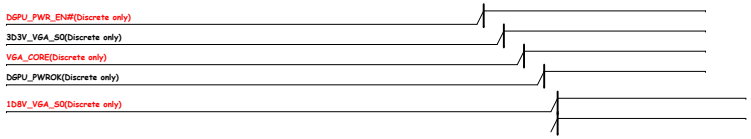
Title *Change History*

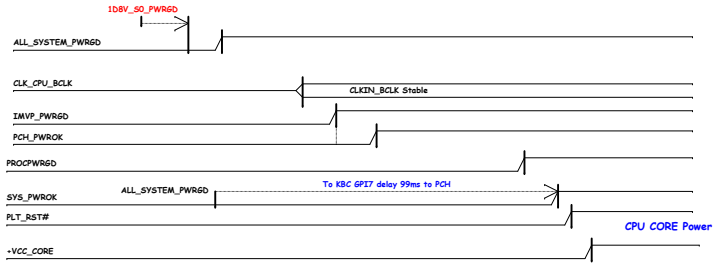
Size	Document Number	Rev
A	Selek CFL-H	A00

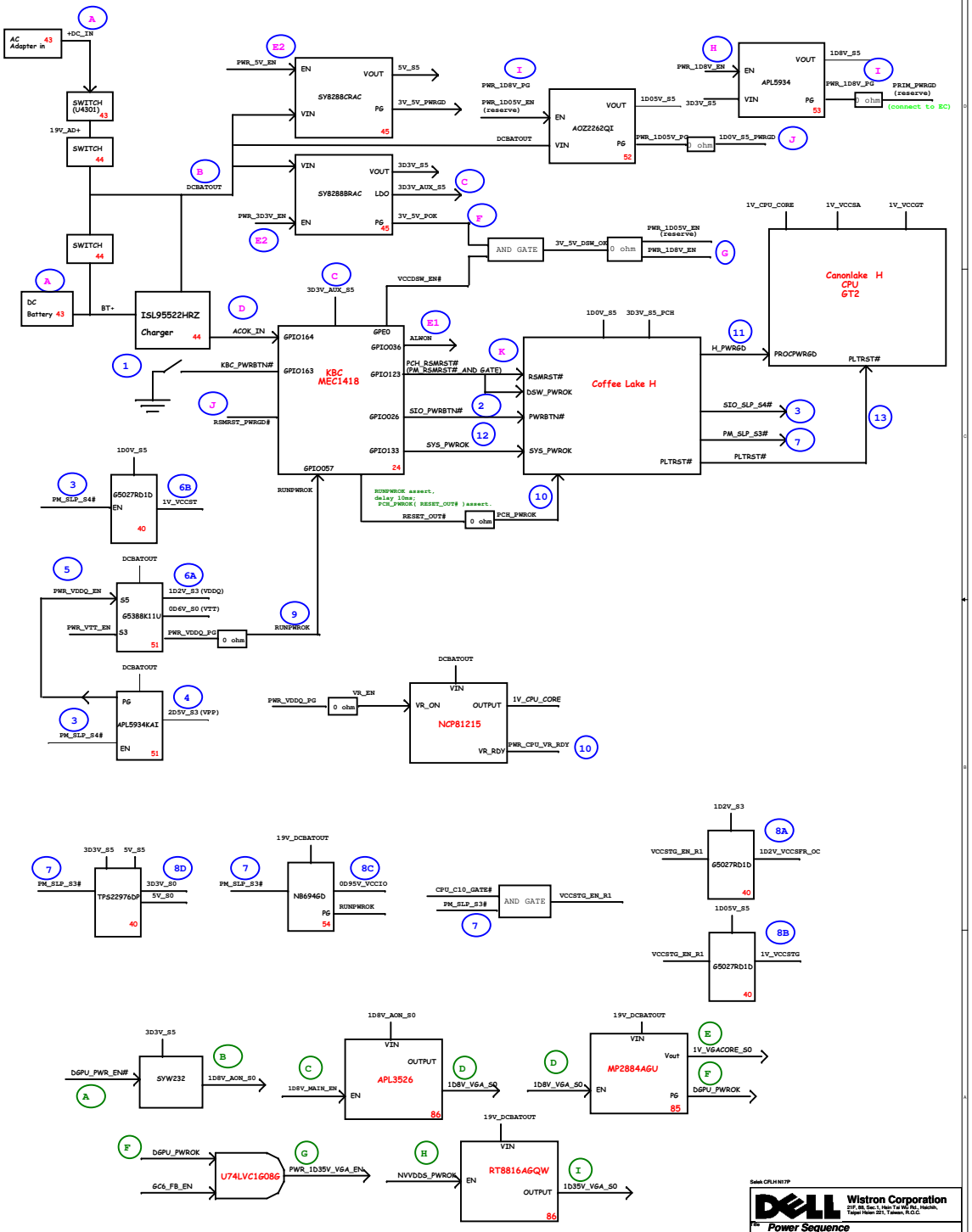
Date: Wednesday, April 03, 2019 Sheet 101 of 105

Intel-Power Up Sequence









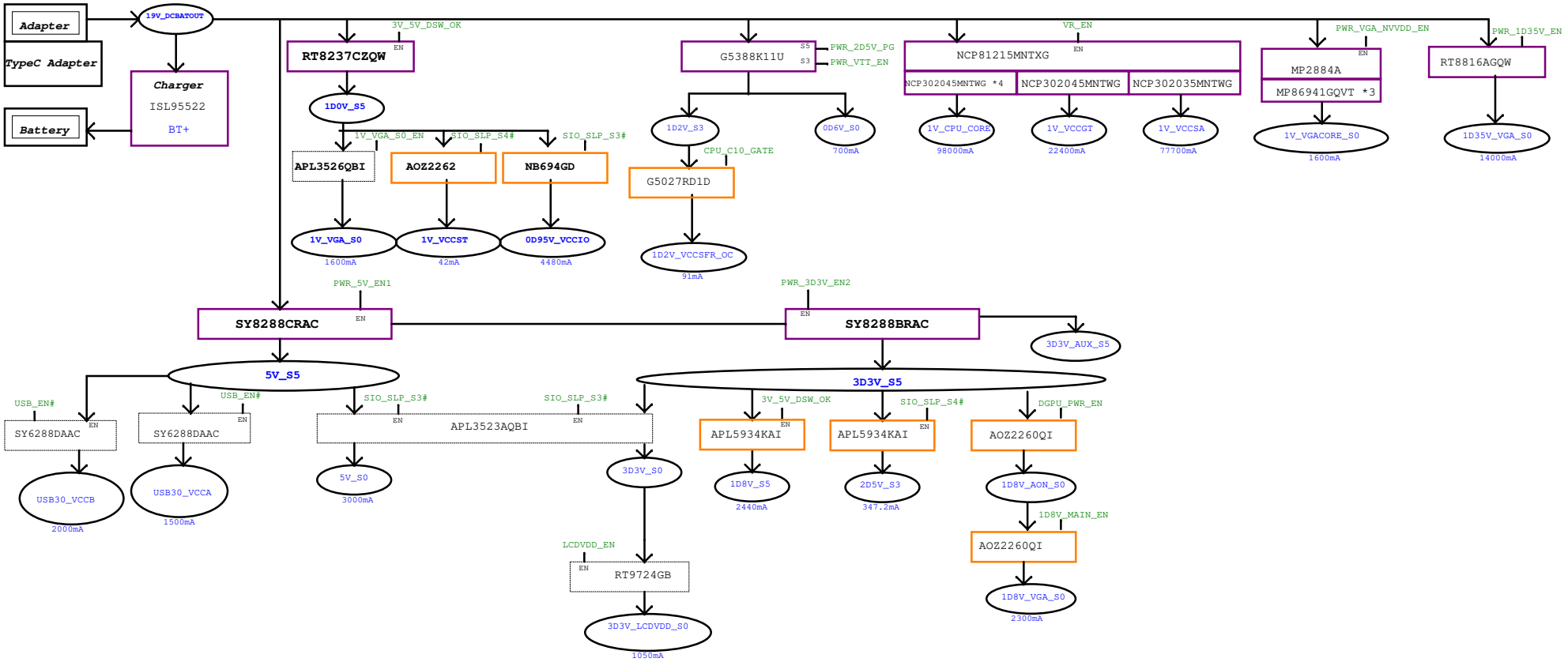
Selek CFLH N17P

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
M	Selek CFL-H	A00

Date: Wednesday, April 08, 2019 Sheet 109 of 109



Power Shape

Regulator	LDO	Switch

Selek CFLH N17P

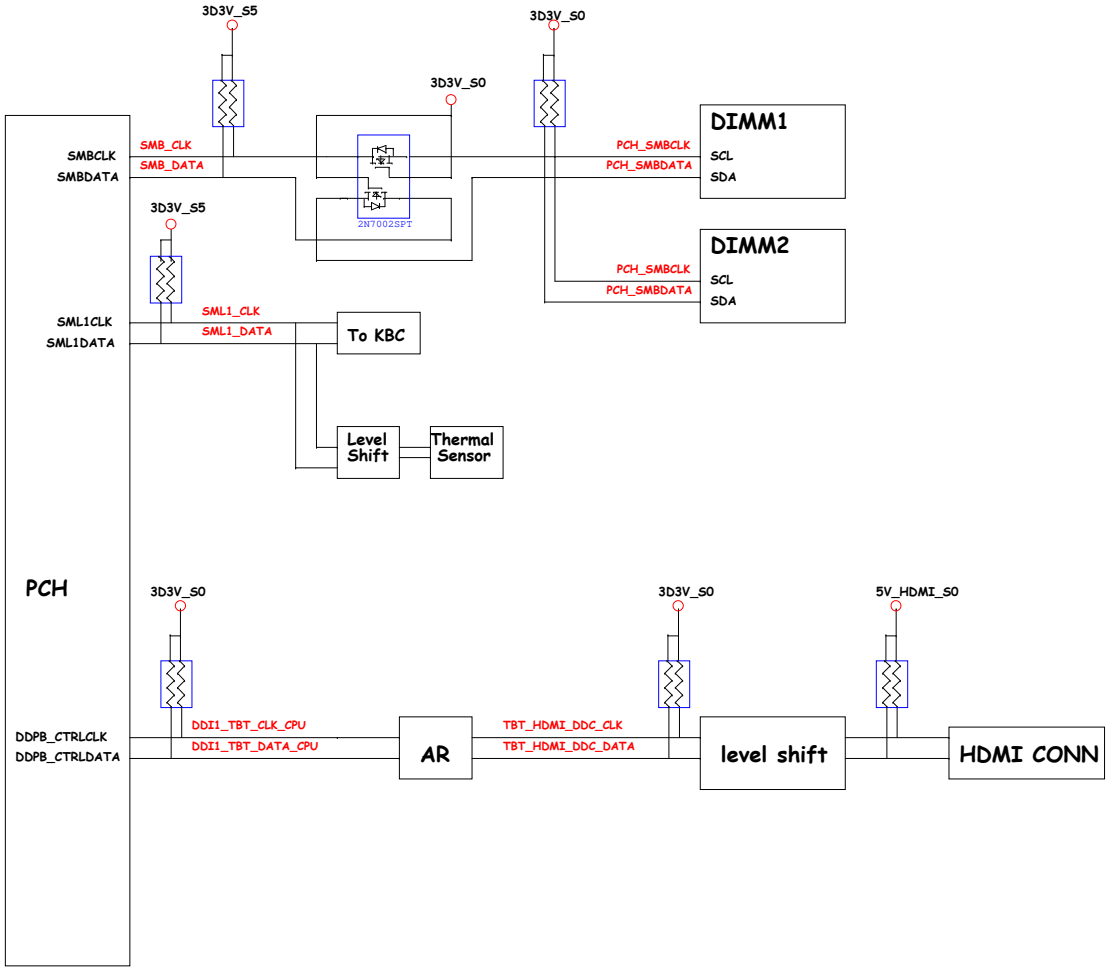
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

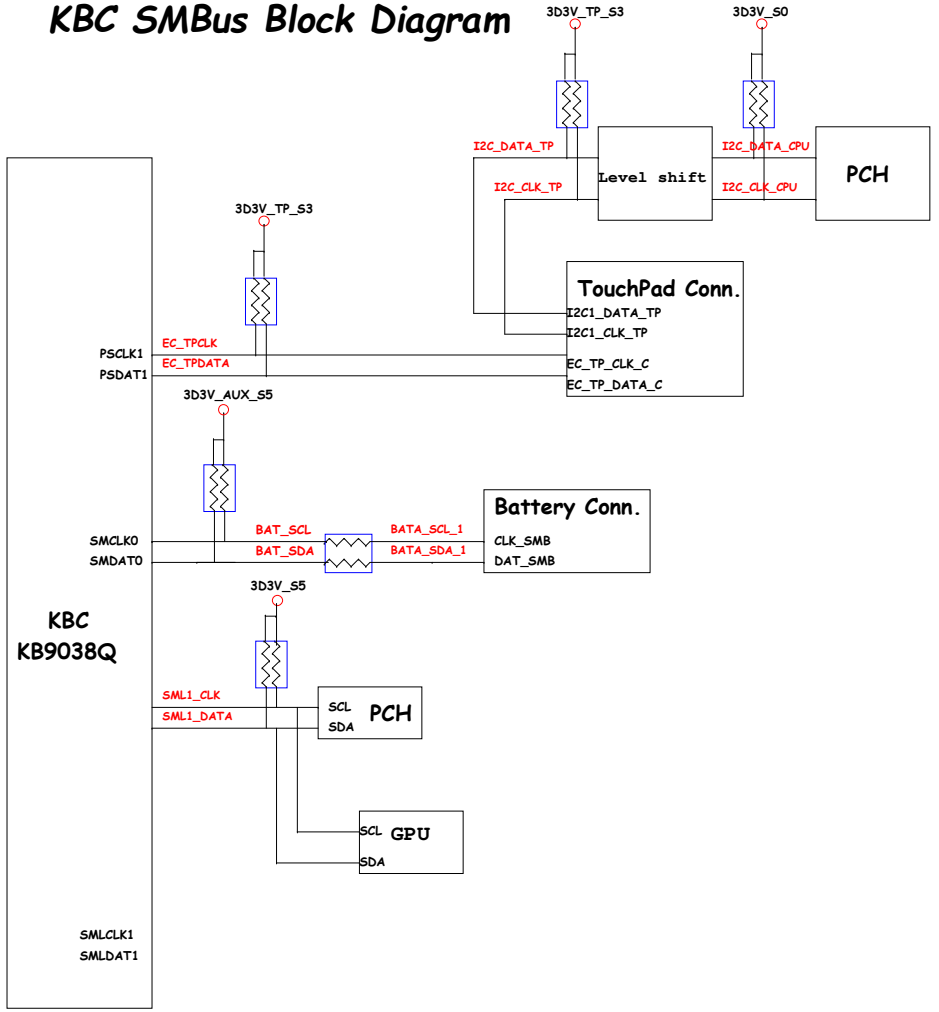
Size	Document Number	Rev
A2	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 103 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



Selek CFLH N17P

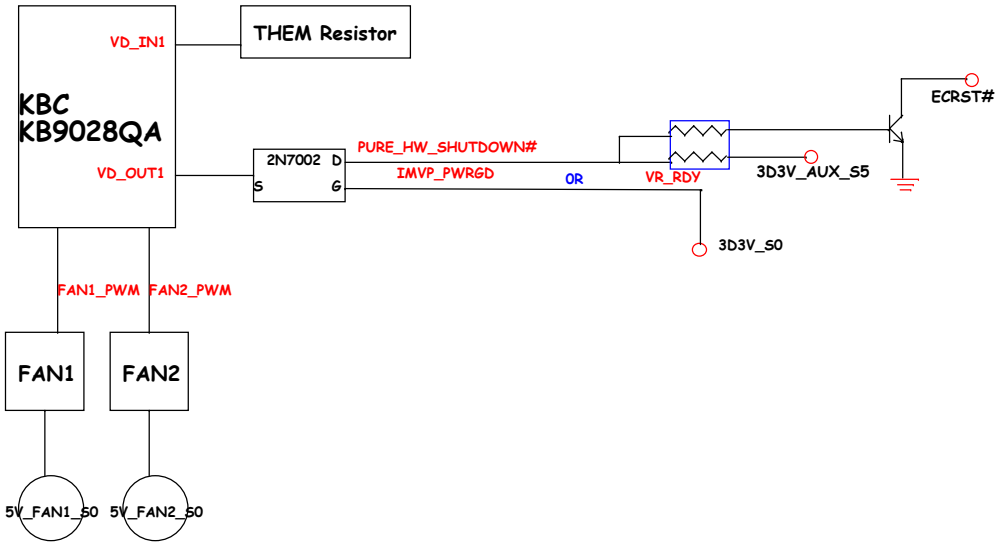
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

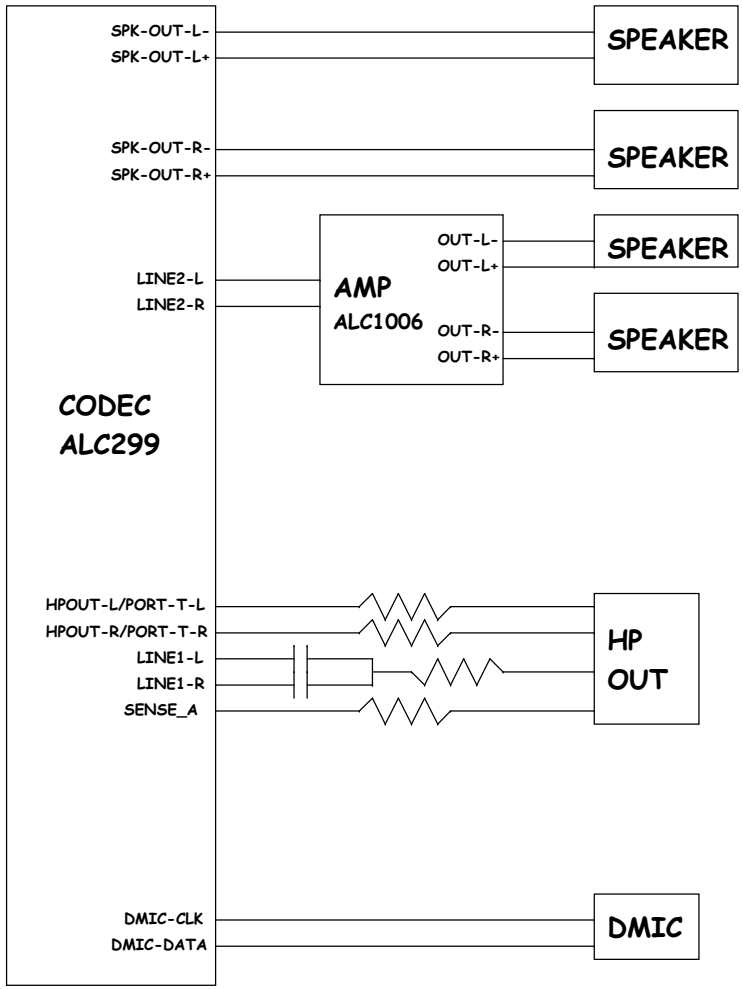
Size	Document Number	Rev
Custom	Selek CFL-H	A00

Date: Wednesday, April 03, 2019 Sheet 104 of 105

Thermal Block Diagram



Audio Block Diagram



Selek CFLH N17P

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal /AUDIO Block Diagram		
Size: Custom	Document Number: Selek CFL-H	Rev: A00
Date: Wednesday, April 03, 2019	Sheet 105 of 105	