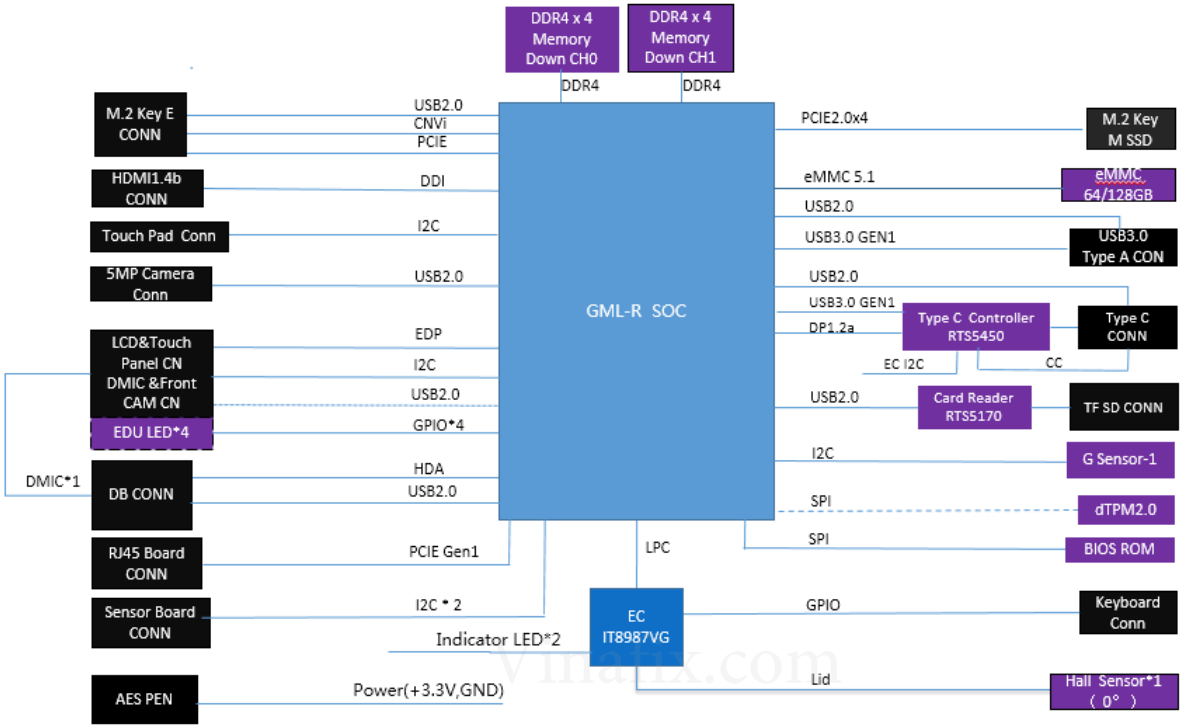
B1 V1 DDR4*2 Channel

Intel Gemini Lake Refresh Platform

		Huaqin Telecom Technology Com.,Ltd.			
		HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	COVER PAGE	Size	B
PAGE_DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet	1 of 59



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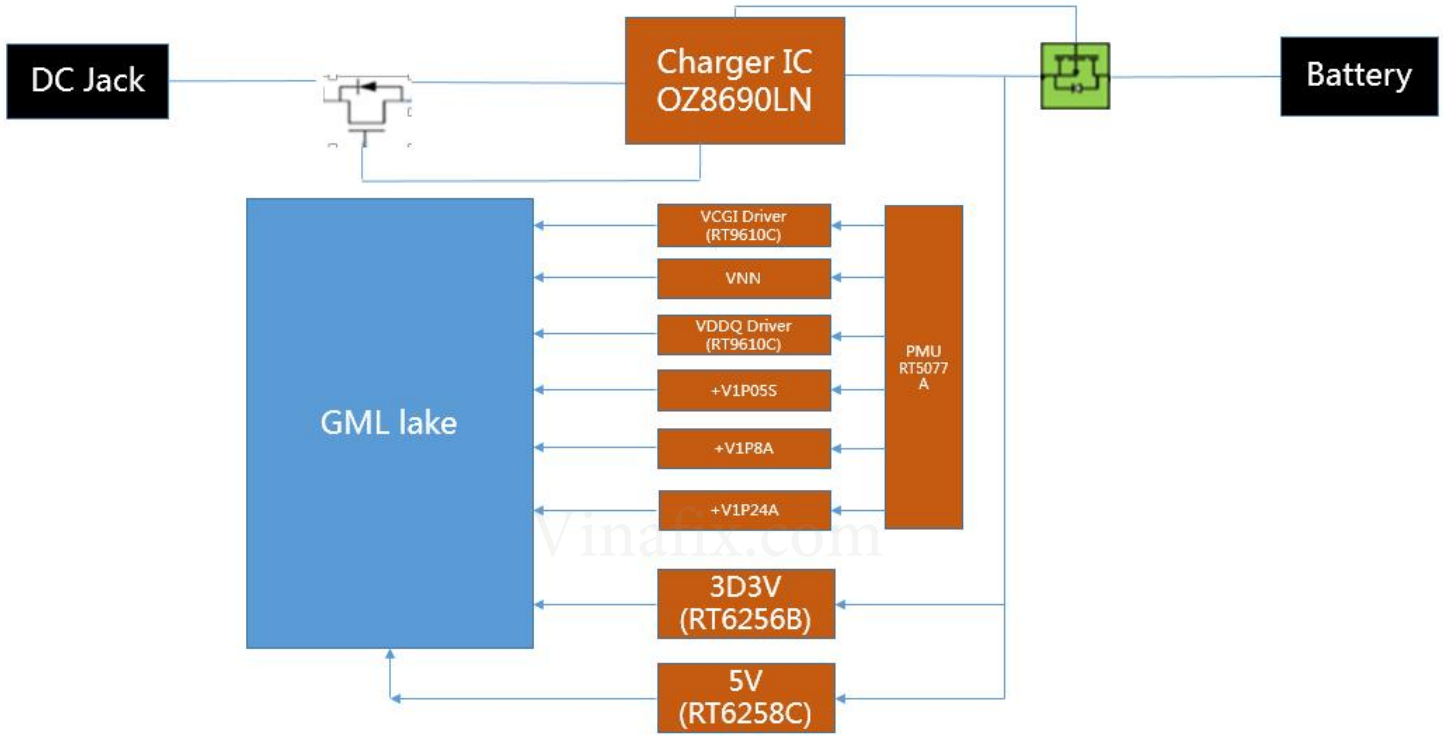
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	2 of 59



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		HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	<OrgAddr3>	Size	B
PAGE_DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet	3 of 59

Power States(Adapter)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	V1P05S	+V1P2U_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_CWS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF[1]
S4(STD)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF[1]
S5(SoftOff)	LOW	LOW	LOW	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF[1]

Note1:CNVi moudle on,Pcie moudle off

Power States(Battery)

Signal	SLP_S0#	SLP_S3#	SLP_S4#	+V5P0A	+V3P3A	VNN	V1P8A	V1P2A	VCGI	+V1P05S	+V1P2U_VDDQ	+3P3SX	+1P8SX	+5P0SX	+V3P3SX_CWS
S0(Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	LOW	LOW	HIGH	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON/OFF[1]
S4(STD)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF[1]
S5(SoftOff)	LOW	LOW	LOW	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON/OFF[1]

Note1:CNVi moudle on,Pcie moudle off

MEM ID

MEM_ID2	MEM_ID1	MEM_ID0	
0	0	0	4x HYNIX 1GB(H5AN8G6NCJR-VKC)
0	0	1	4x Micron 1GB(MT40A512M16LY-075:E)
0	1	0	(512*16)H5AN8G6NCJR-VKC HYNIX
0	1	1	8x MT40A512M16LY-075:E MICRON
1	0	0	xxx
1	0	1	xxx

MB ID

			HW_ID6	HW_ID5	HW_ID2	HW_ID1	HW_ID0
NB2372	DVT	Clamshell(180°)	X	X	1	1	0
NB2372	DVT	Convertible 860°)	X	X	1	1	1

PCIe Port

Port	Device
0-3	SSD
4	LAN
5	WLAN

SATA Port

Port	Device
0	SSD

USB2.0 Port

Port	Device
0	USB3.0 Type-A
1	Rear Camera
2	USB3.0 Type-A(DB)
3	USB3.0 Type-C
4	WLAN
5	Touch screen
6	Front Camera
7	SD Card

USB3.0 Port

Port	Device
0	USB3.0 Type-A
1	USB3.0 Type-C
5	USB3.0 Type-A(DB)

Huaqin Telecom Technology Com.,Ltd.

HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	<OrgAddr3>	Size	B
PAGE DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet	4 of 59

Huaqin Telecom Technology Com.,Ltd.			
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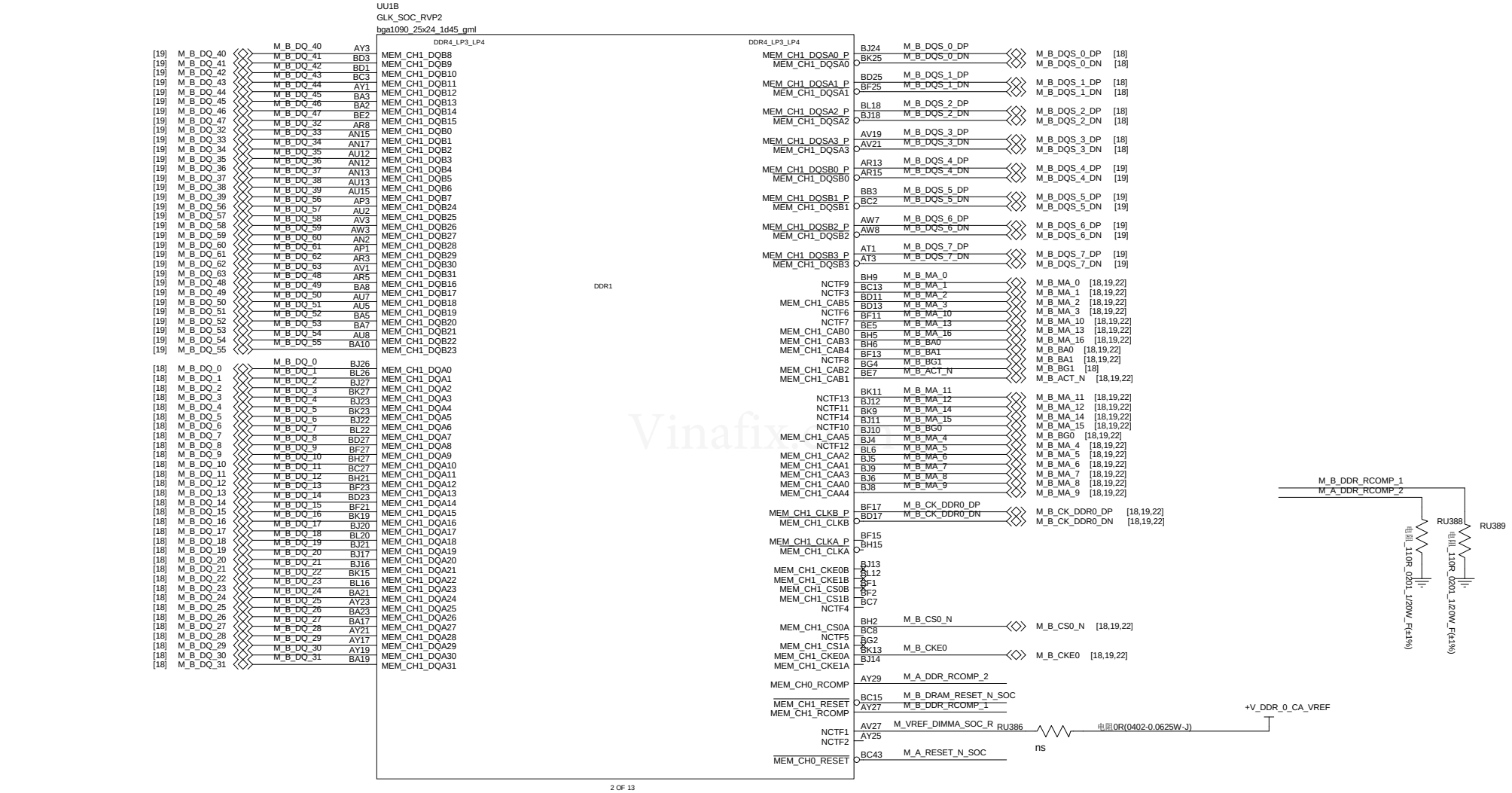

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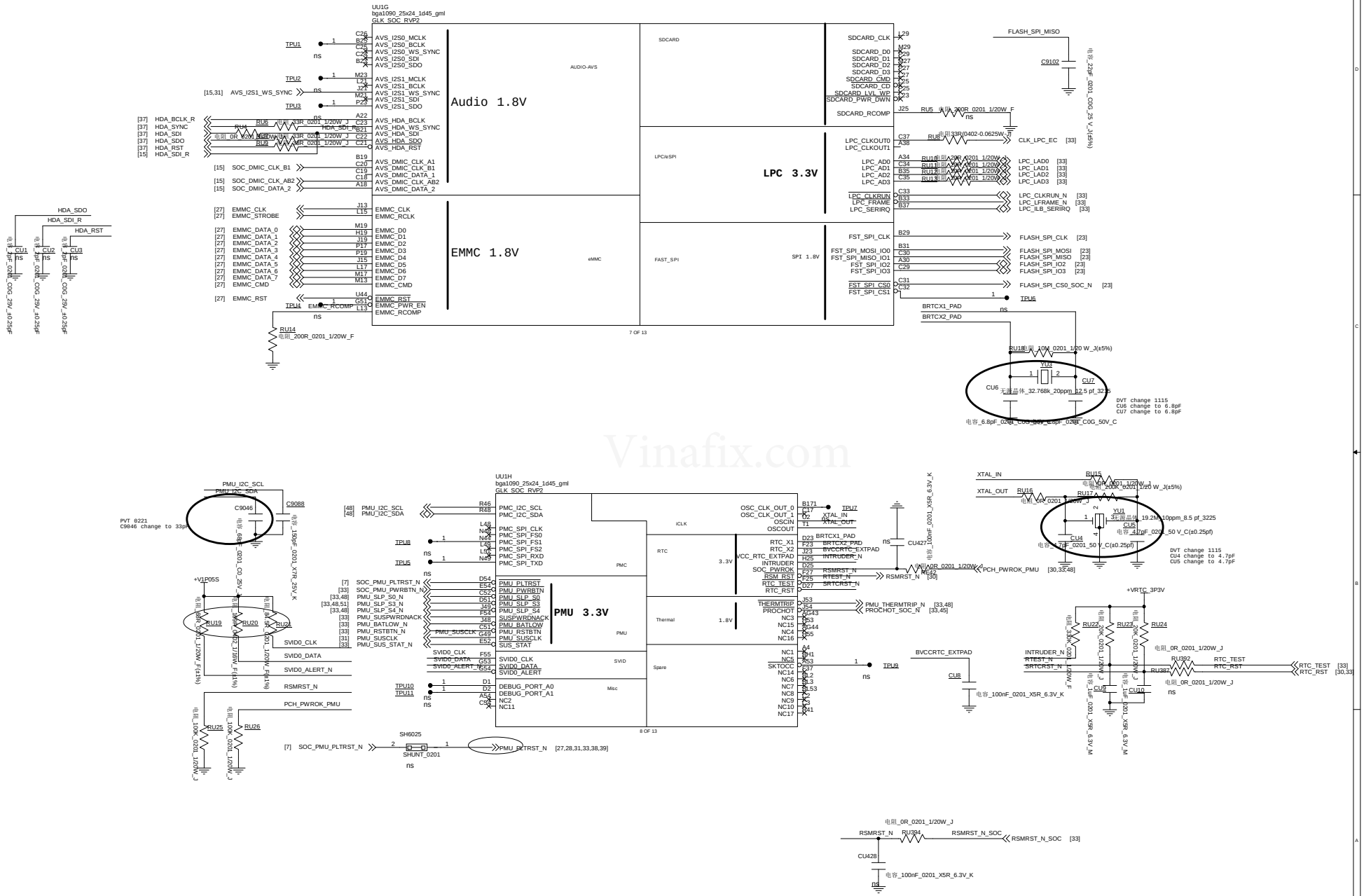

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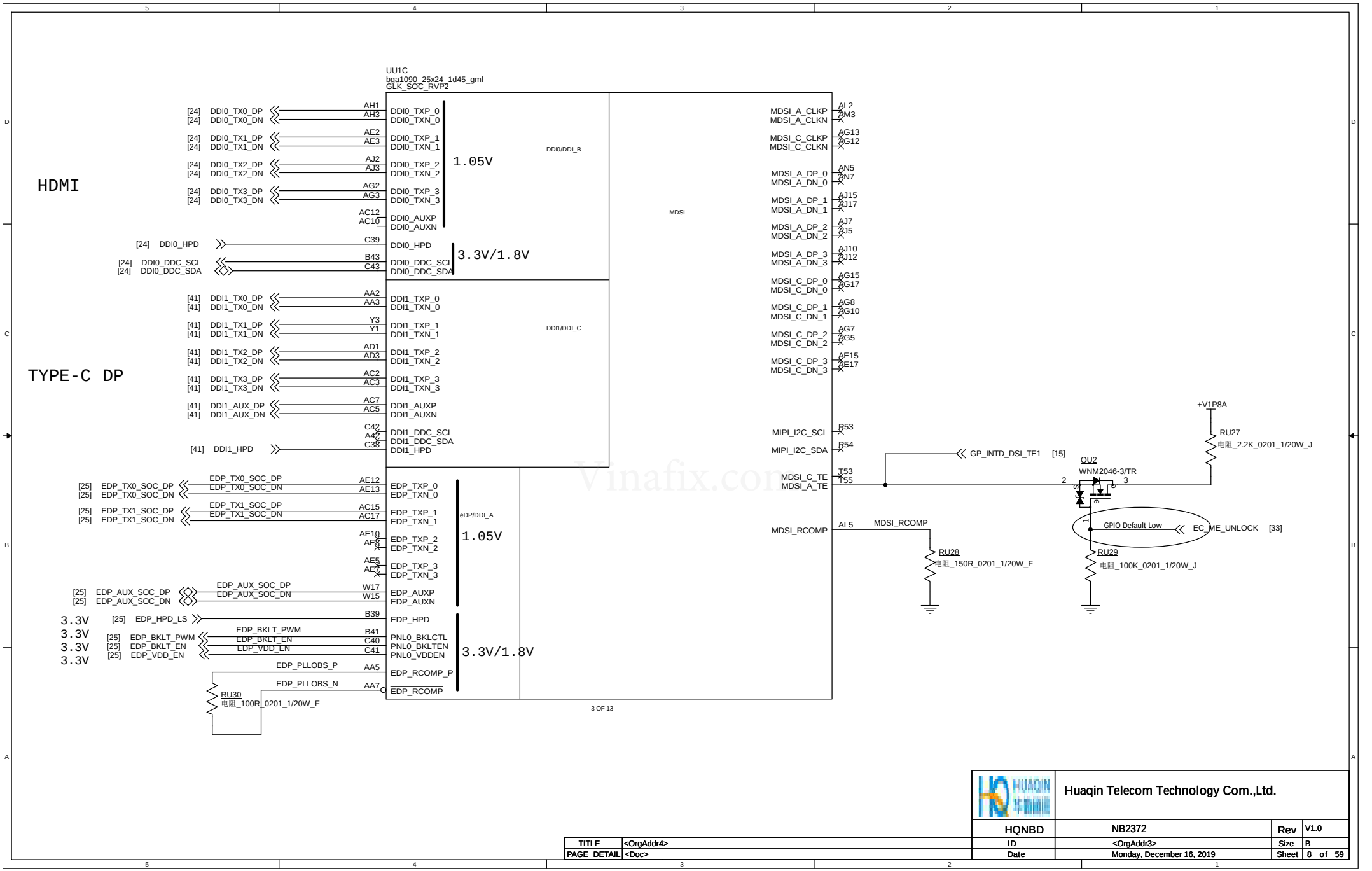
		Size	C
		Sheet	7 of 59



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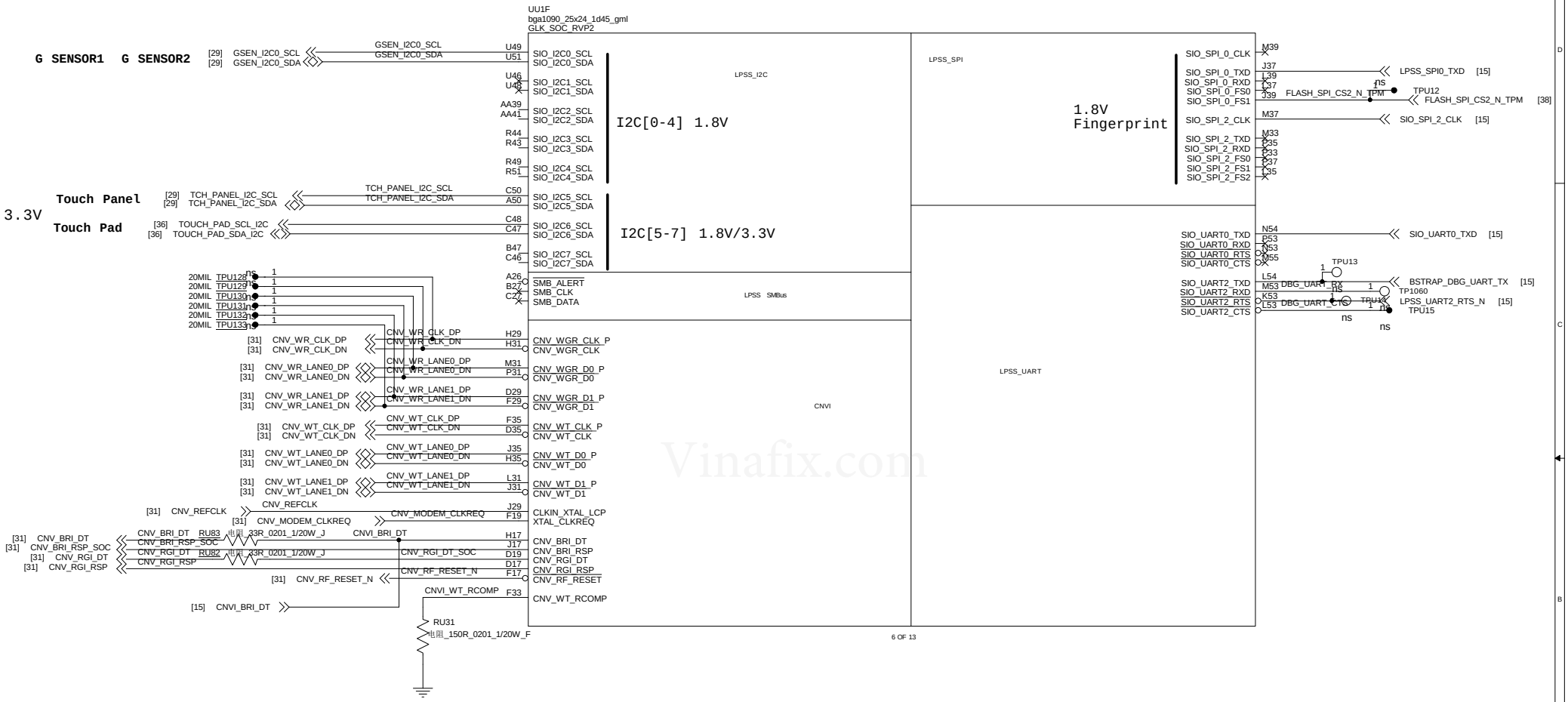

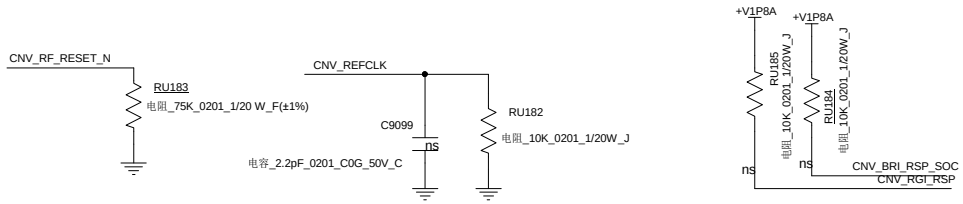

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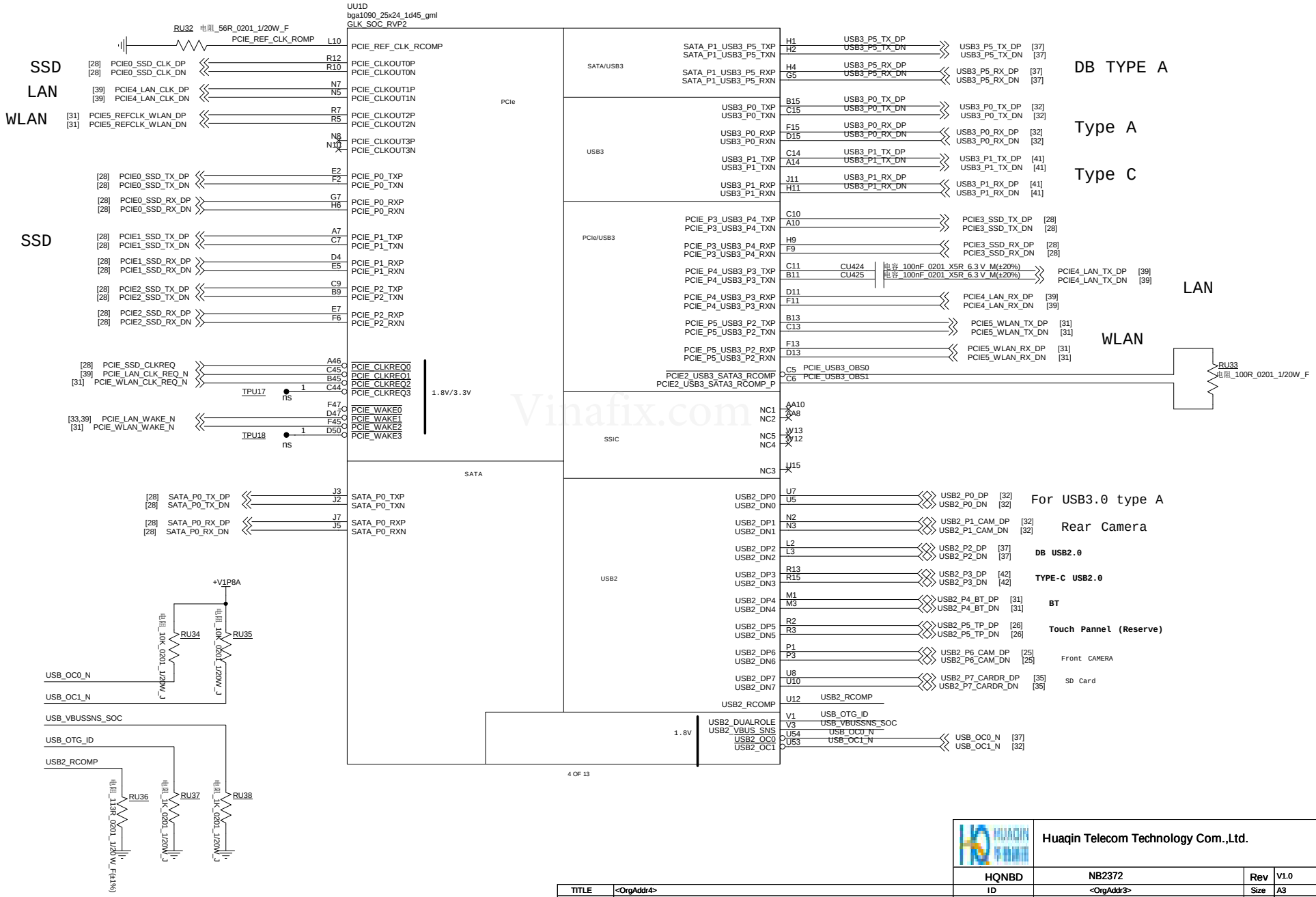

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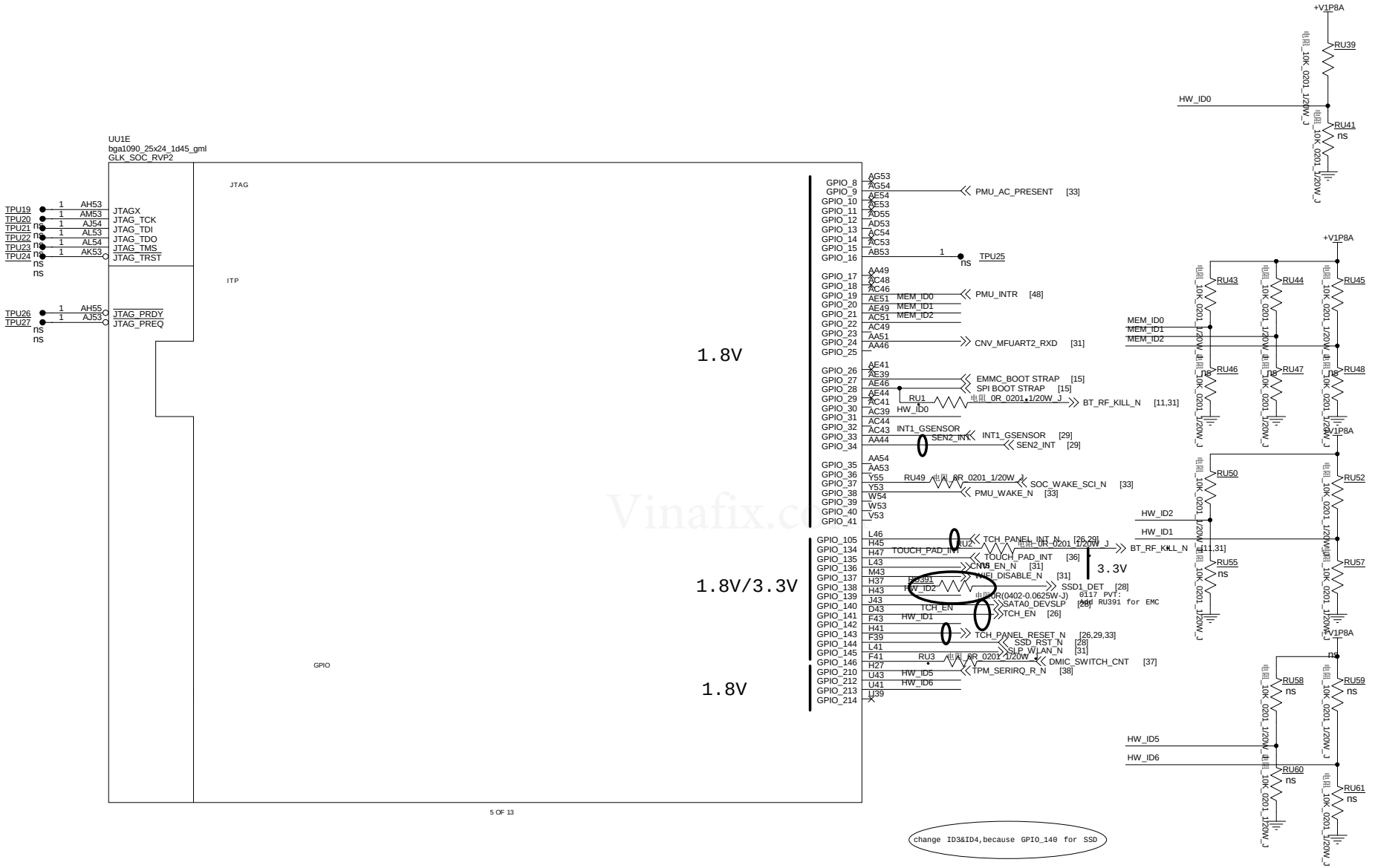

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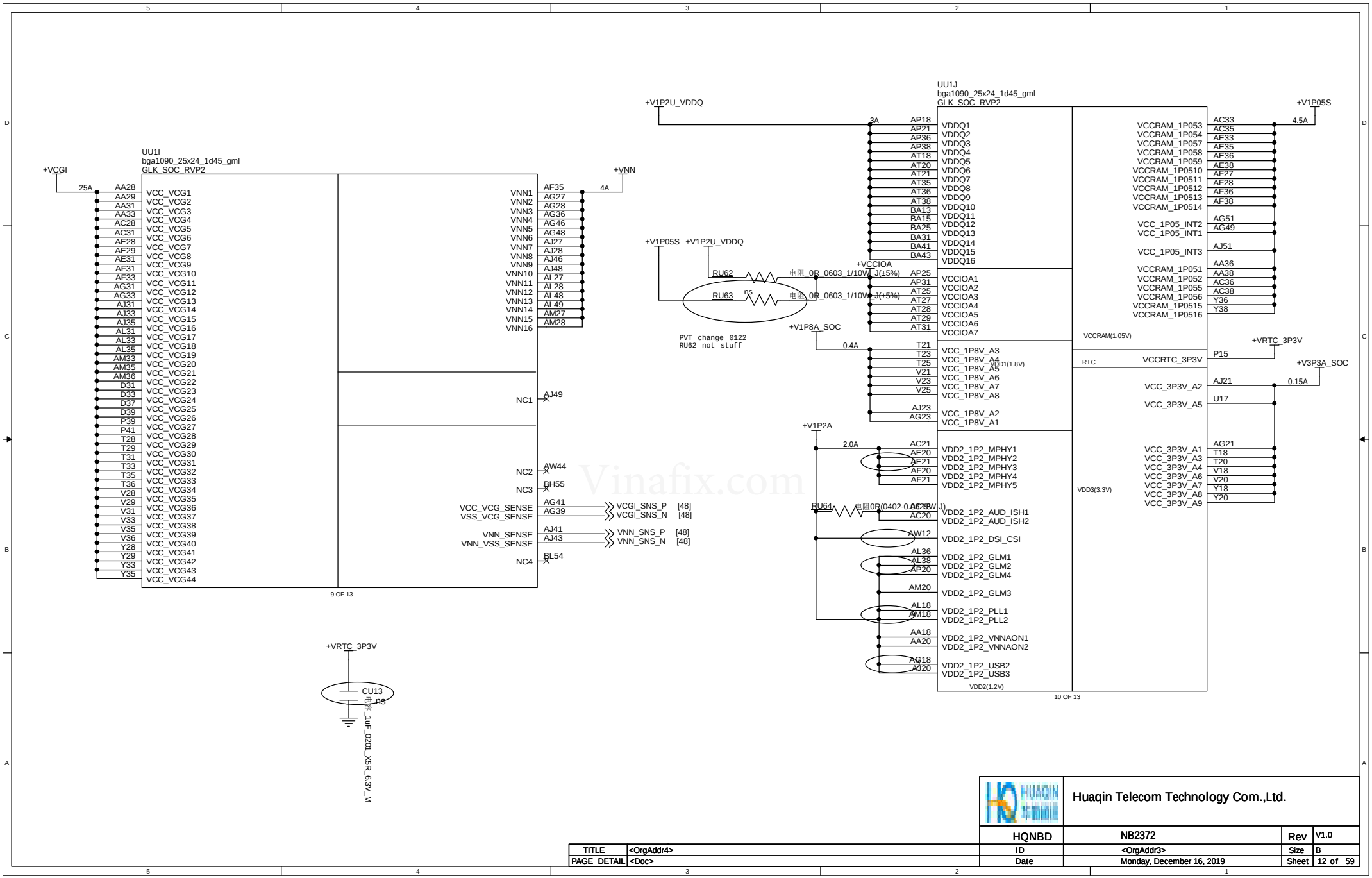

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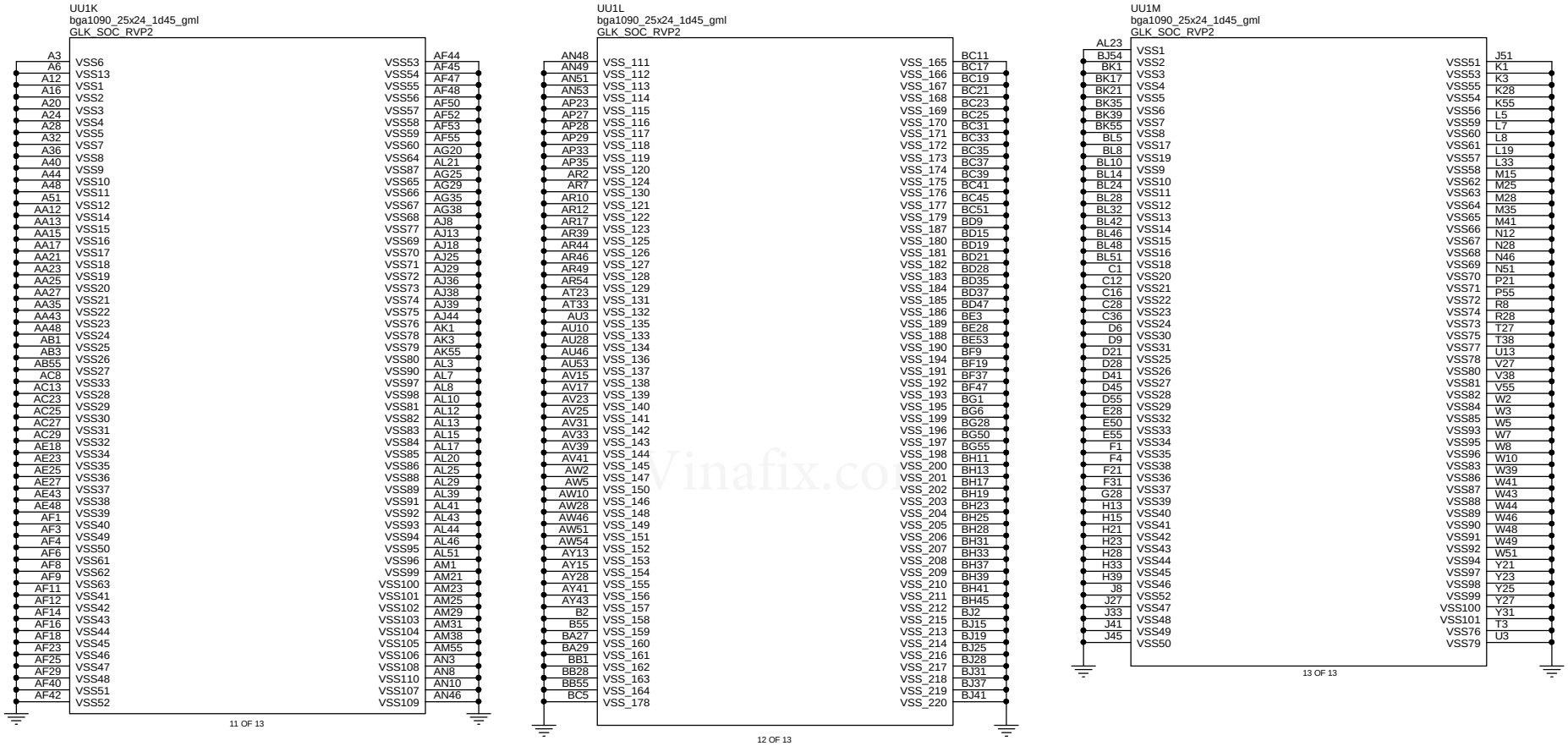

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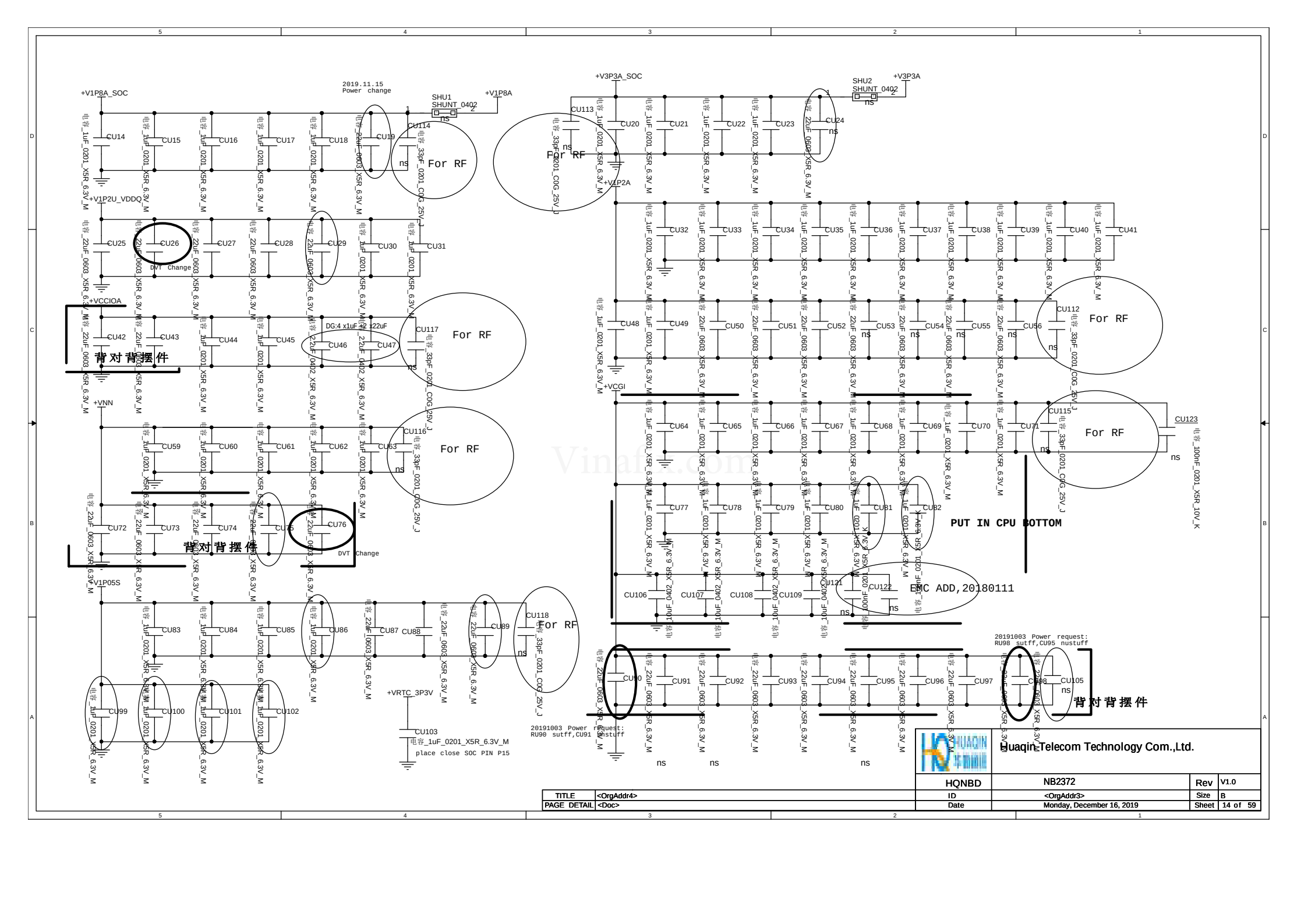
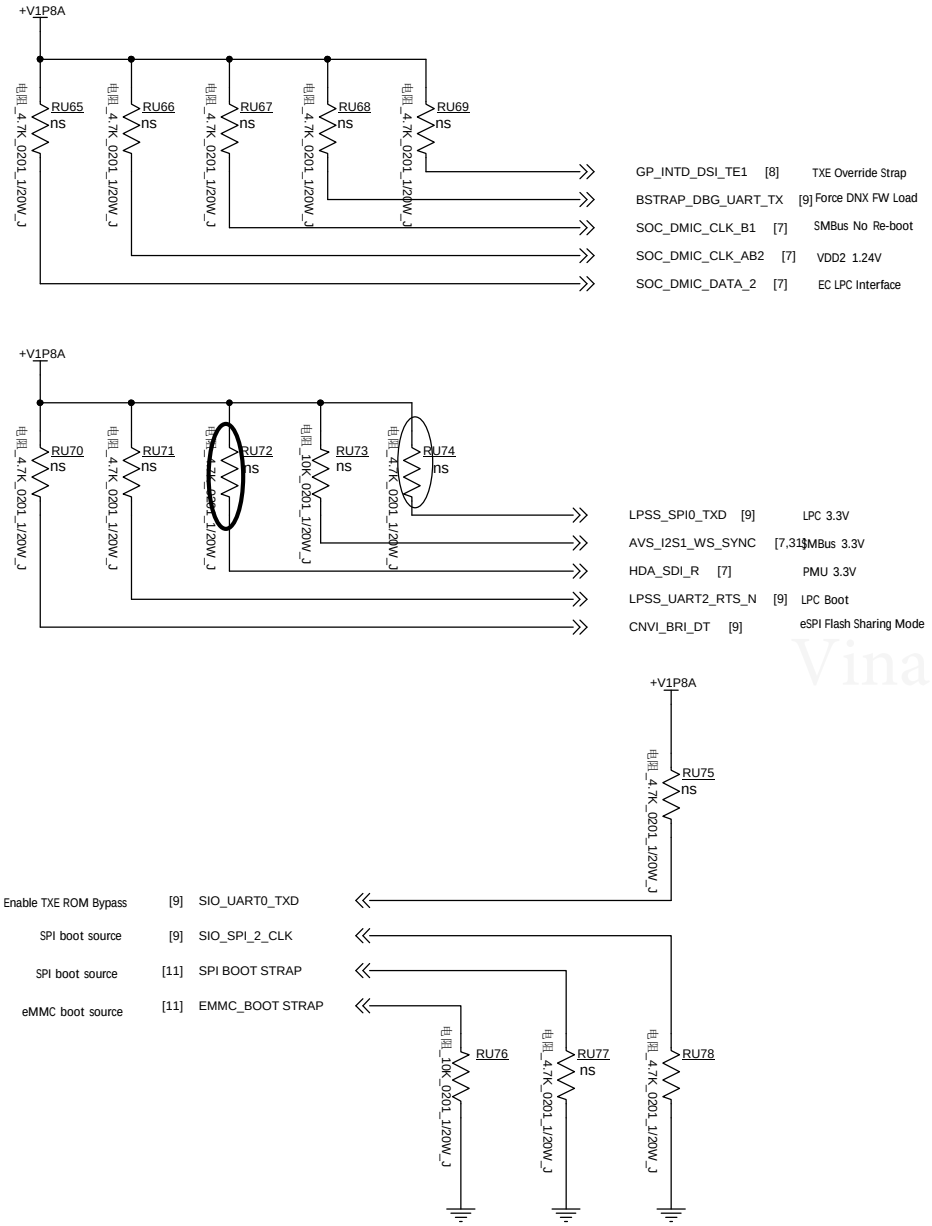
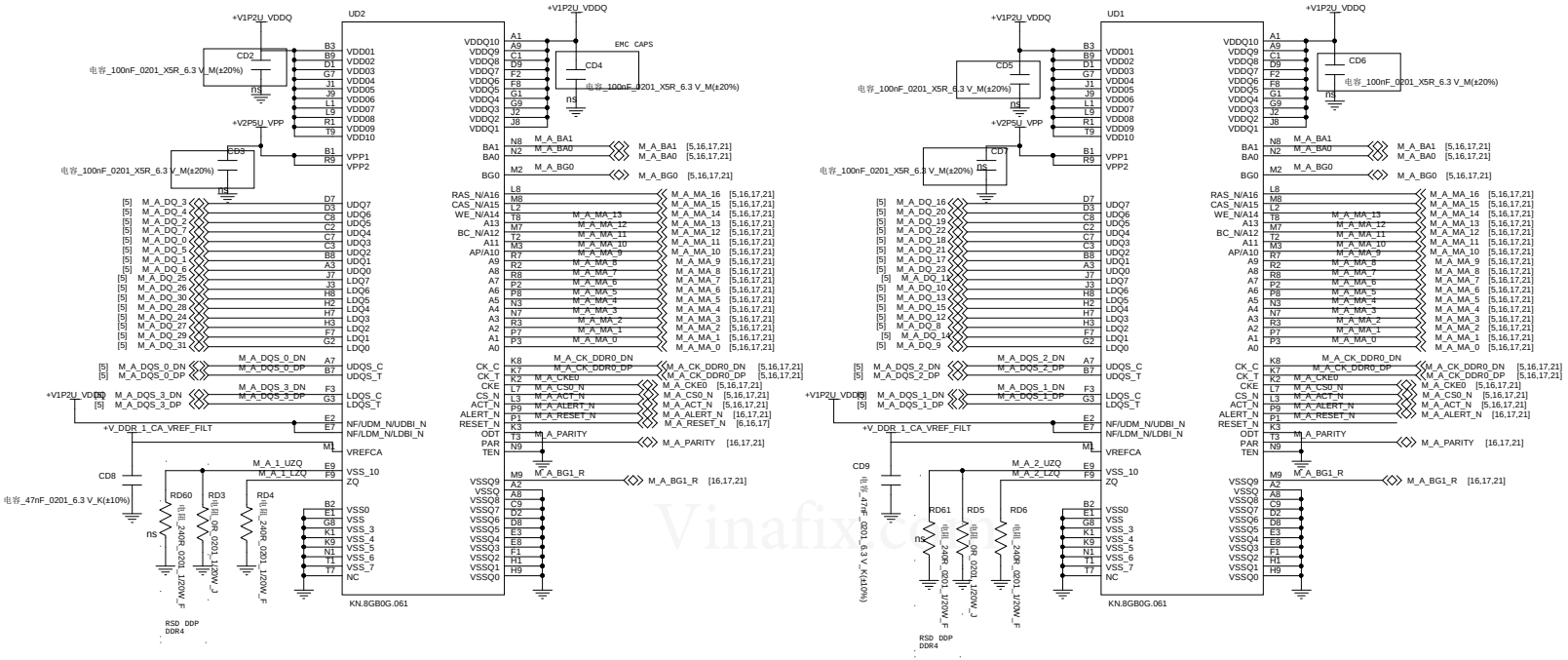

+V1P8A_SOC
2019.11.15
Power change
SHU1
SHUNT_0402
+V1P8A
For RF
+V1P2U_VDDQ
DVT Change
+VCCIOA
背对背摆件
DG:4 x1uF x 22uF
+VNN
+V1P05S
+V3P3A_SOC
SHU2
SHUNT_0402
+V3P3A
+V1P2A
+VCGI
PUT IN CPU BOTTOM
EMC ADD,20180111
20191003 Power request:
RU98 sutff,CU95 nustuff
+VRTC_3P3V
place close SOC PIN P15
Huaqin Telecom Technology Com.,Ltd.
HQNBD
NB2372
Rev
V1.0
TITLE
<OrgAddr4>
ID
<OrgAddr3>
Size
B
PAGE_DETAIL
<Doc>
Date
Monday, December 16, 2019
Sheet
14 of 59

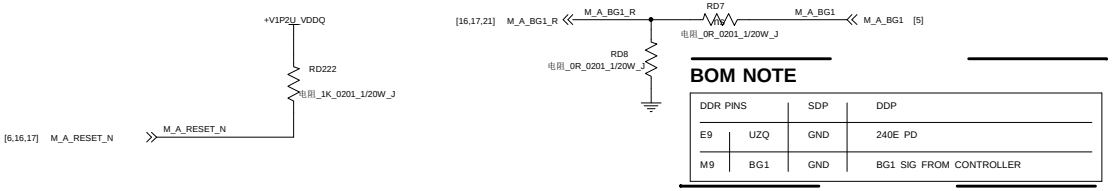


LPSS_SPI0_TXD	GPIO_83	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
AVS_I2S1_WS_SYNC	GPIO_163	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
HDA_SDI_R	GPIO_168	PMU 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
LPSS_UART2_RTS_N	GPIO_66	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default)
CNVI_BRI_DT	GPIO_191	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default)
EMMC_BOOT STRAP	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable;
SPI BOOT STRAP	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
SIO_SPI_2_CLK	GPIO_84	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
SIO_UART0_TXD	GPIO_61	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default)
SOC_DMIC_DATA_2	GPIO_175	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default)
SOC_DMIC_CLK_AB2	GPIO_174	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
SOC_DMIC_CLK_B1	GPIO_172	SMBus No Re Boot	20K PD	1 = Enable 0 = Disable (default)
LPSS_UART2_TXD	GPIO_65	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default)
GP_INTD_DSI_TE1	GPIO_42	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override

Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	B
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	15 of 59



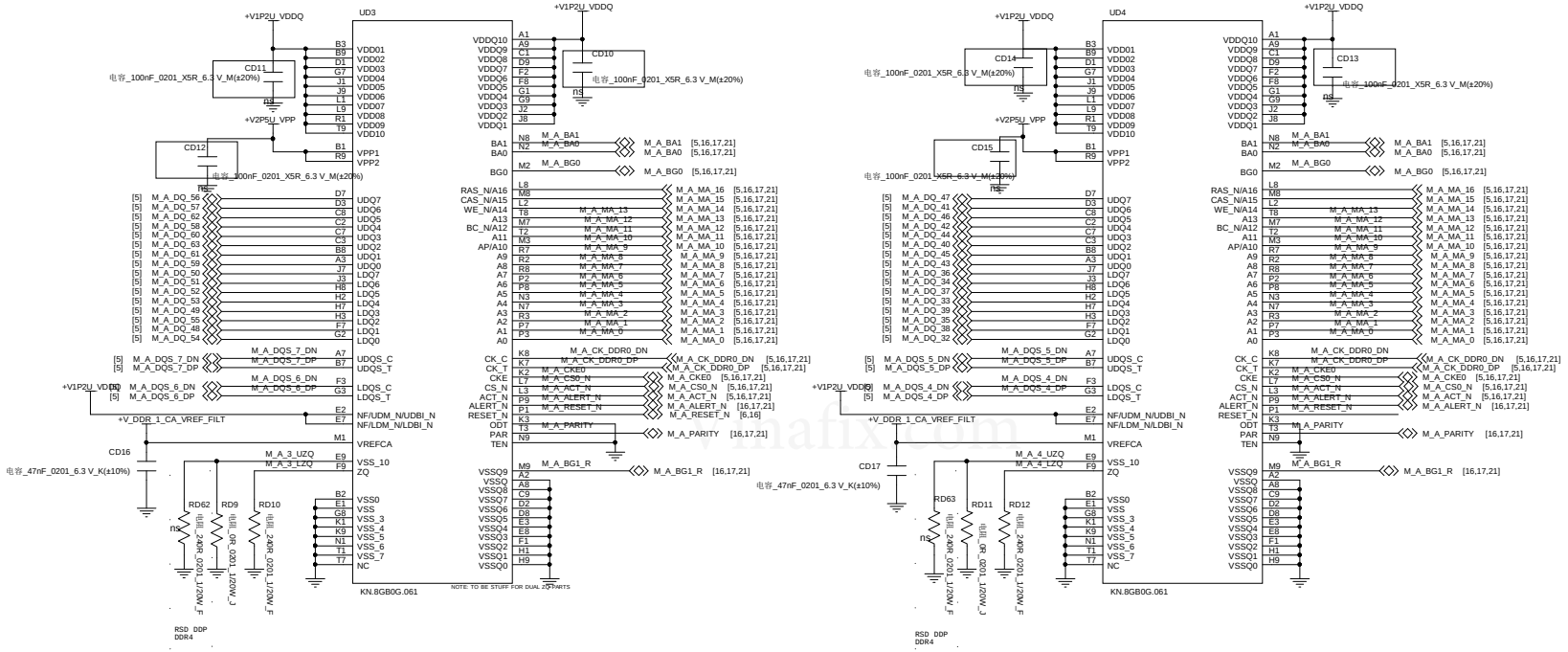
NOTE: TO BE STUFF FOR DUAL ZQ PARTS



BOM NOTE

DDR PINS		SDP	DDP
E9	UZQ	GND	240E PD
M9	BG1	GND	BG1 SIG FROM CONTROLLER

Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>		ID <OrgAddr3>	Size C
PAGE_DETAIL <Doc>		Date Monday, December 16, 2019	Sheet 16 of 59



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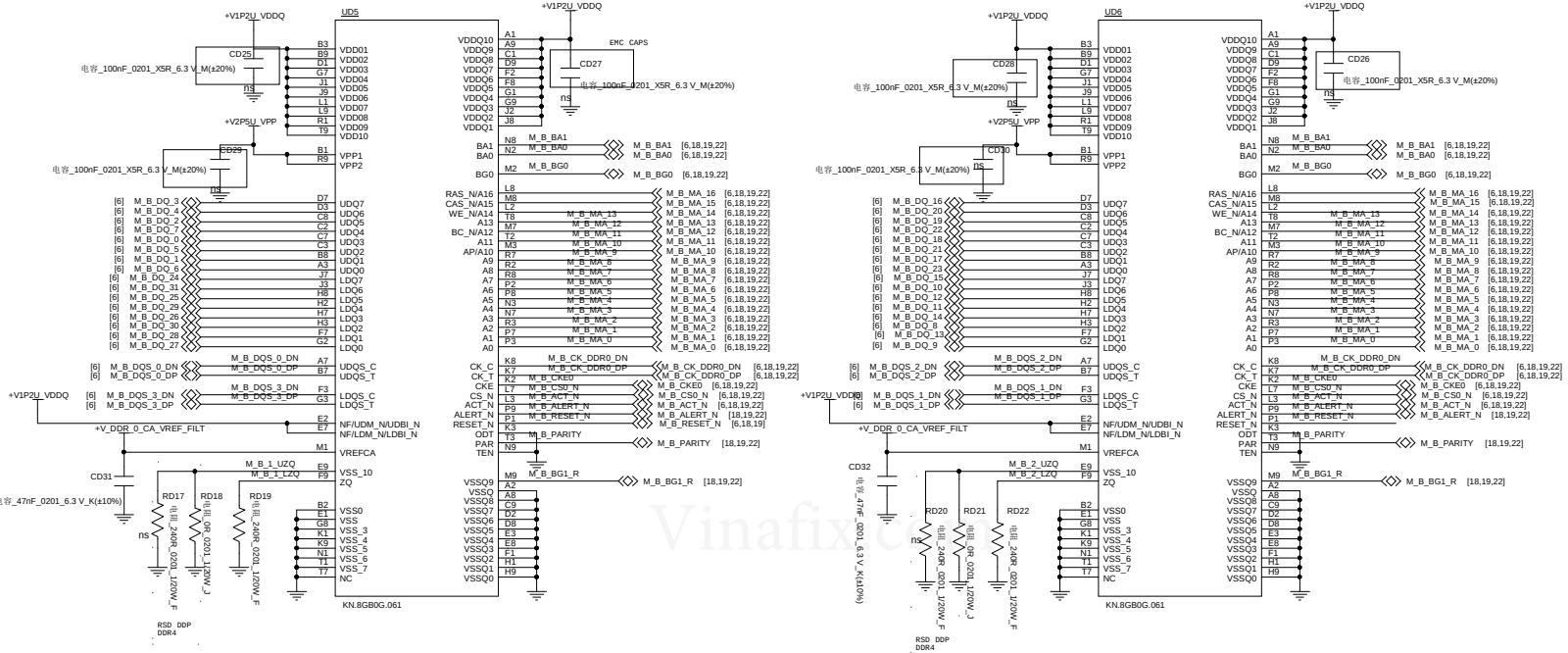
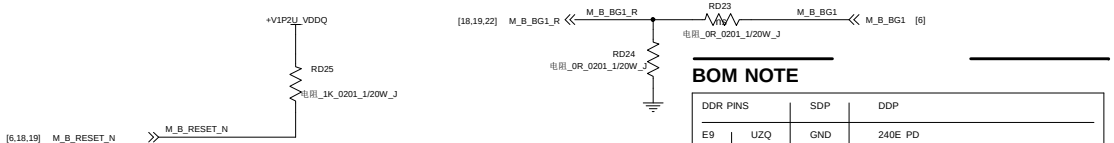
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	17 of 59



NOTE: TO BE STUFF FOR DUAL ZQ PARTS



BOM NOTE

DDR PINS		SDP	DDP
E9	UZQ	GND	240E PD
M9	BG1	GND	BG1 SIG FROM CONTROLLER

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HQNBD	NB2372	Rev	V1.0
		ID	<OrgAddr3>
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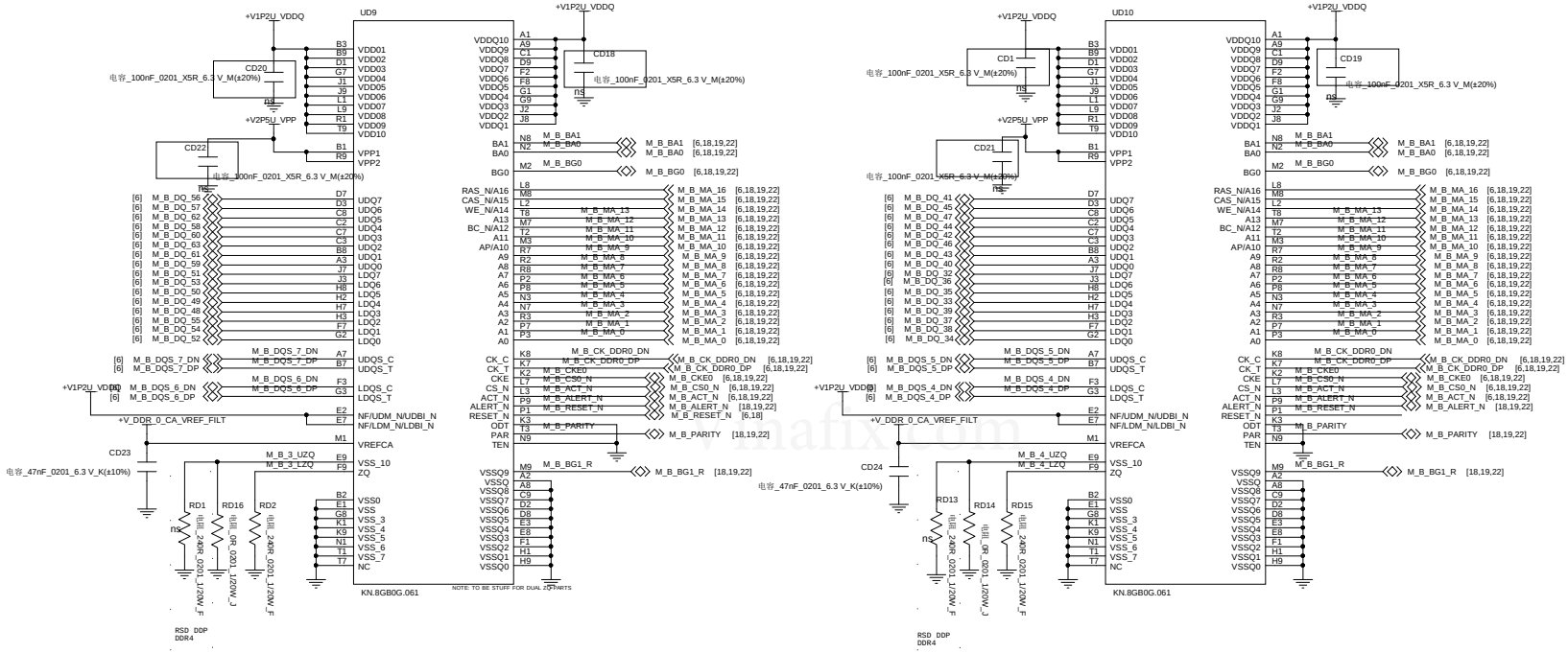
TITLE	<OrgAddr4>	Date	Monday, December 16, 2019
PAGE_DETAIL	<Doc>	Sheet	18 of 59



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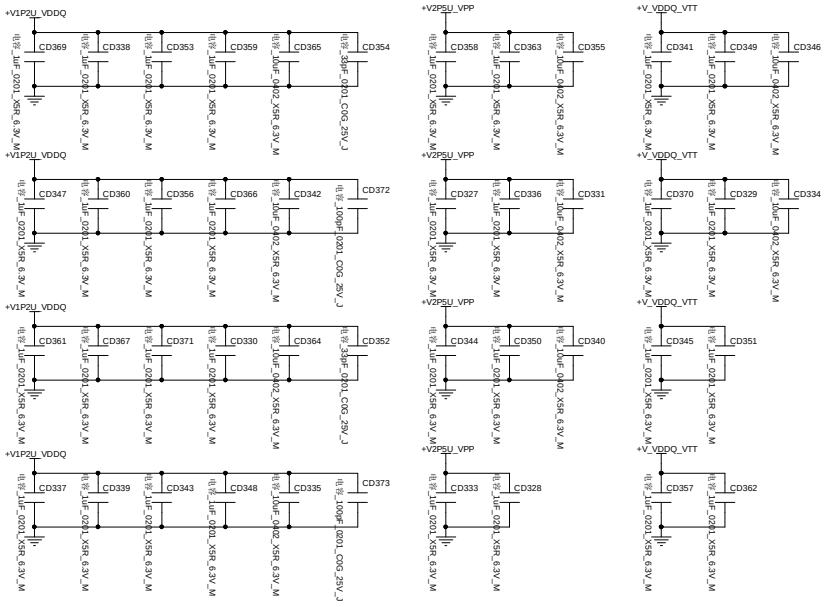
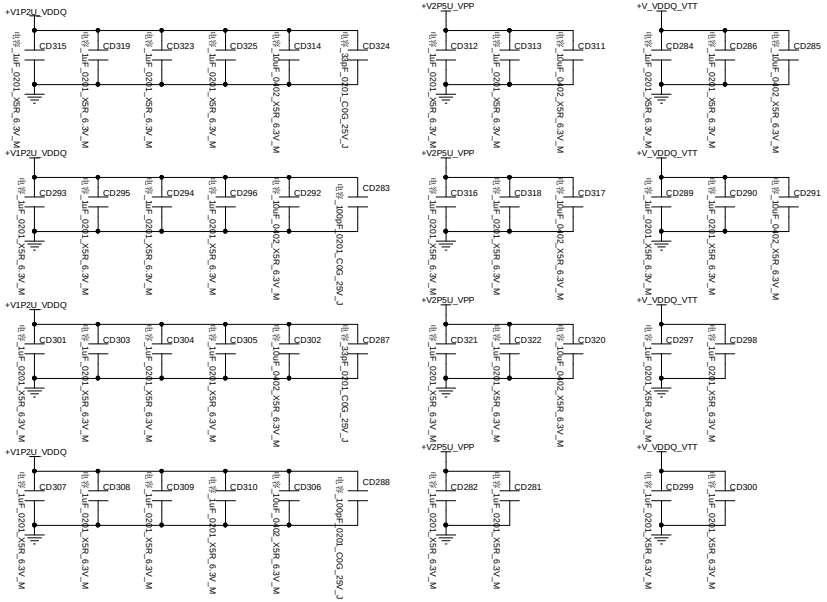
PAGE_DETAIL	<Doc>	HQNBD / NB2372	Rev V1.0
		ID <OrgAddr3>	Size C
		Date Monday, December 16, 2019	Sheet 19 of 59

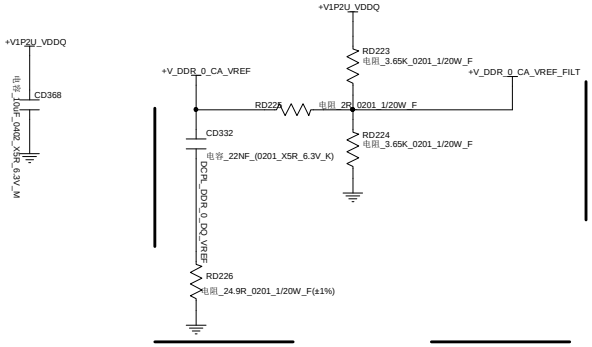
DECOUPLING CAPACITORS FOR DDR CHANNEL B



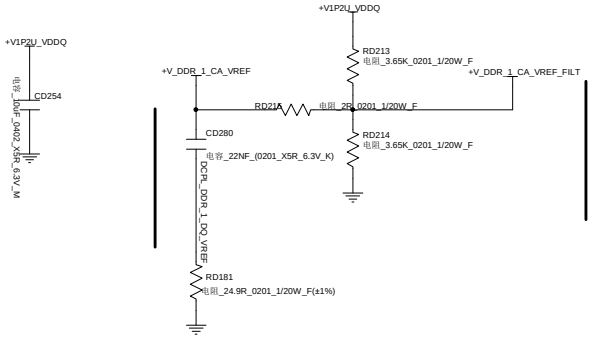
DECOUPLING CAPACITORS FOR DDR CHANNEL A



DDR4 CH B REF GENERATION



DDR4 CH A REF GENERATION



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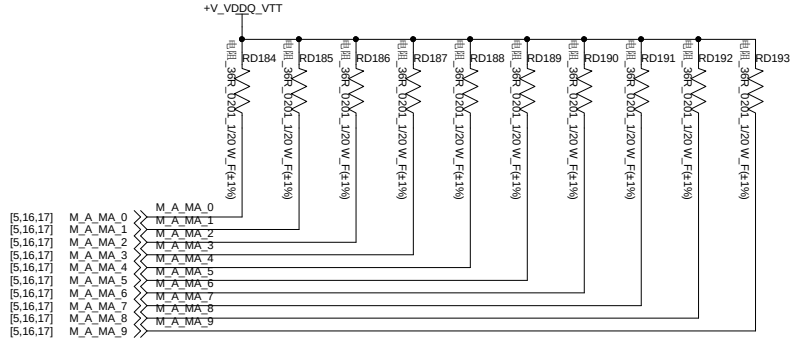
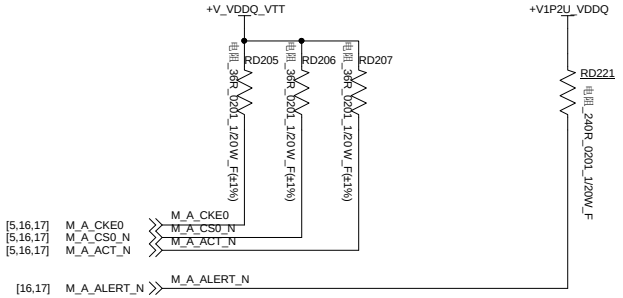
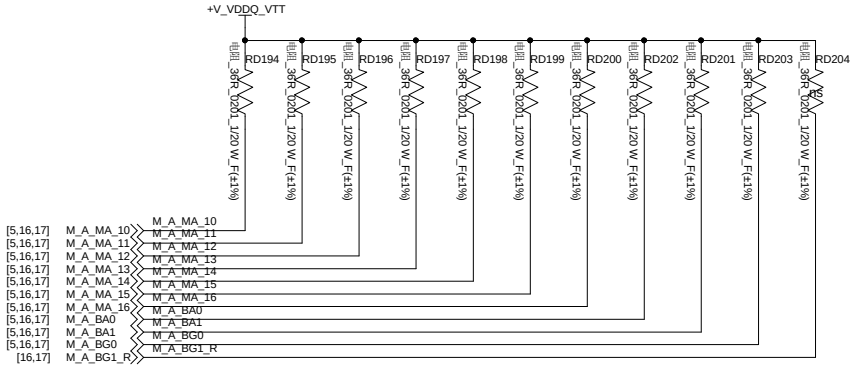
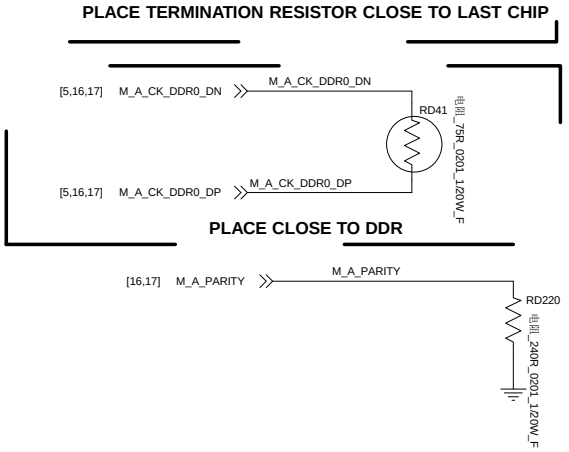
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	C
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	20 of 59

MEMORY TERMINATIONS MD CHANNEL A









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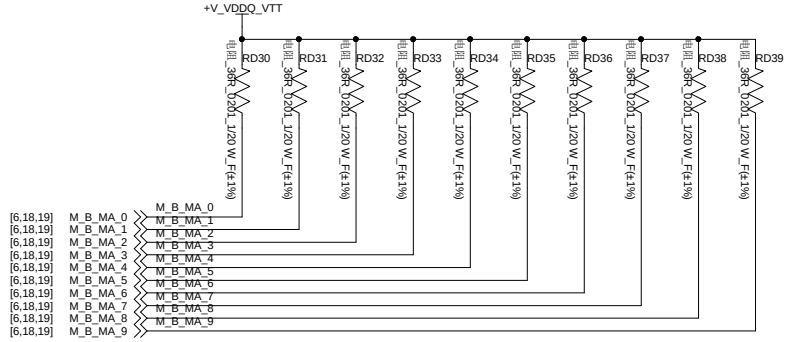
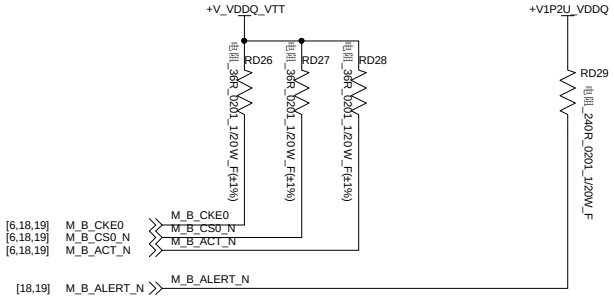
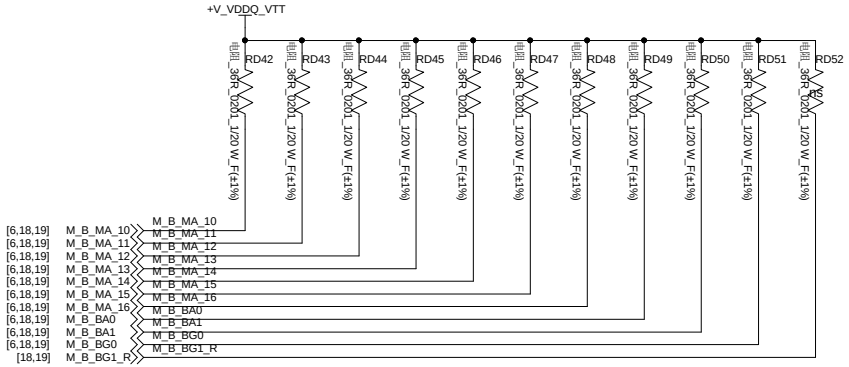
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	21 of 59

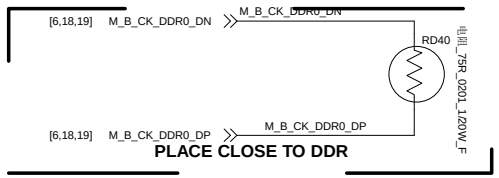
MEMORY TERMINATIONS MD CHANNEL B



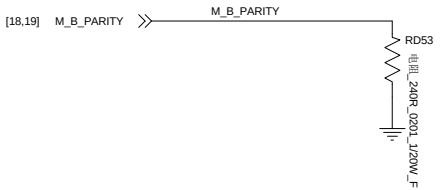




PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP



PLACE CLOSE TO DDR



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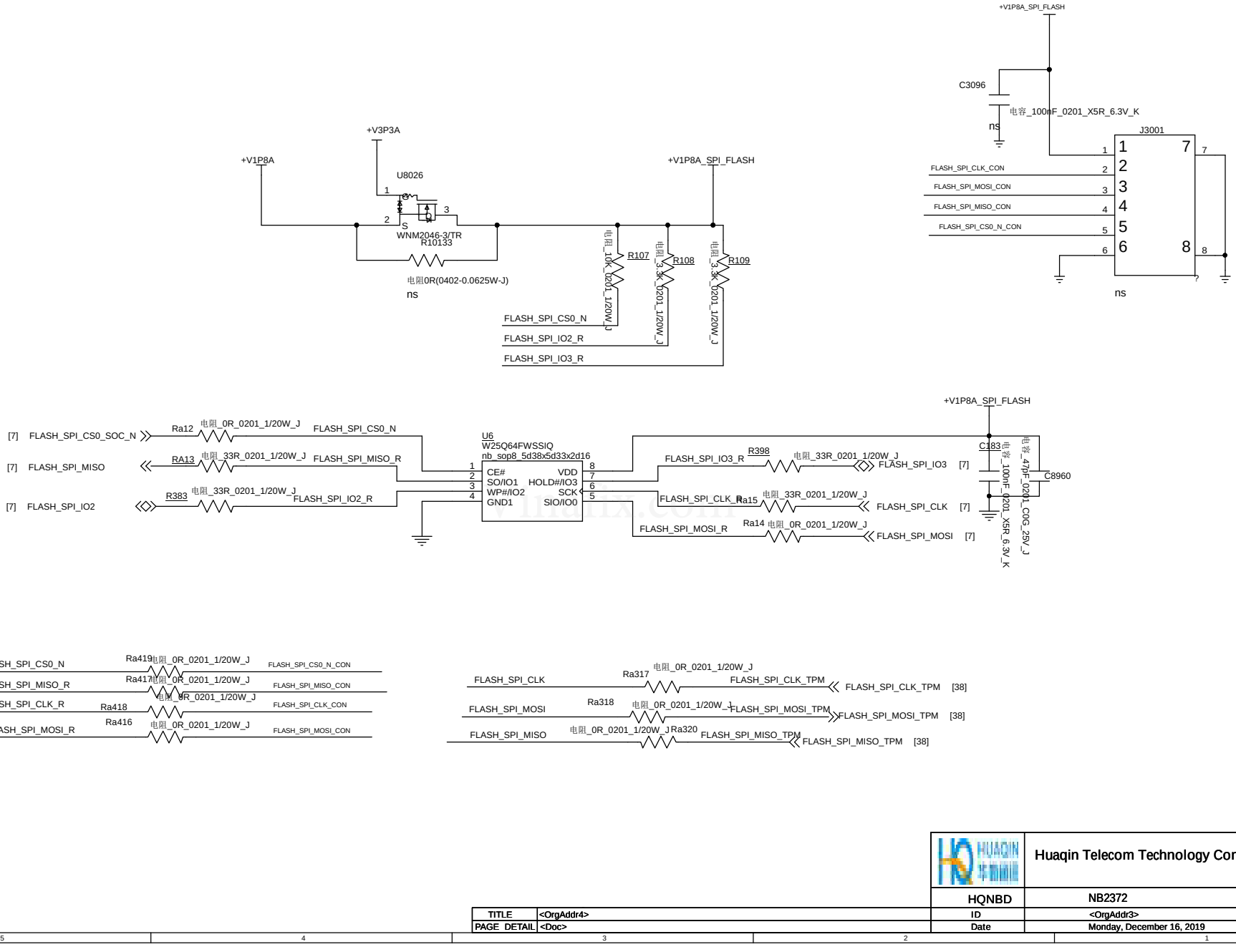
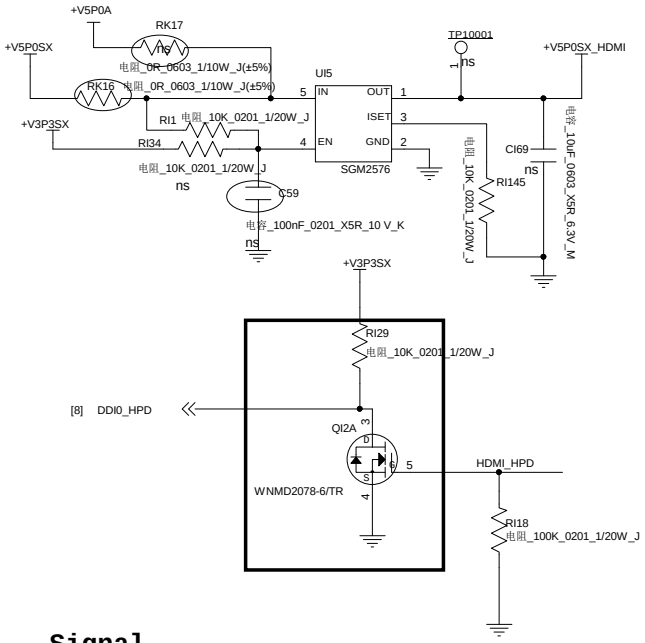
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	22 of 59



Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	B
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	23 of 59

Power 1



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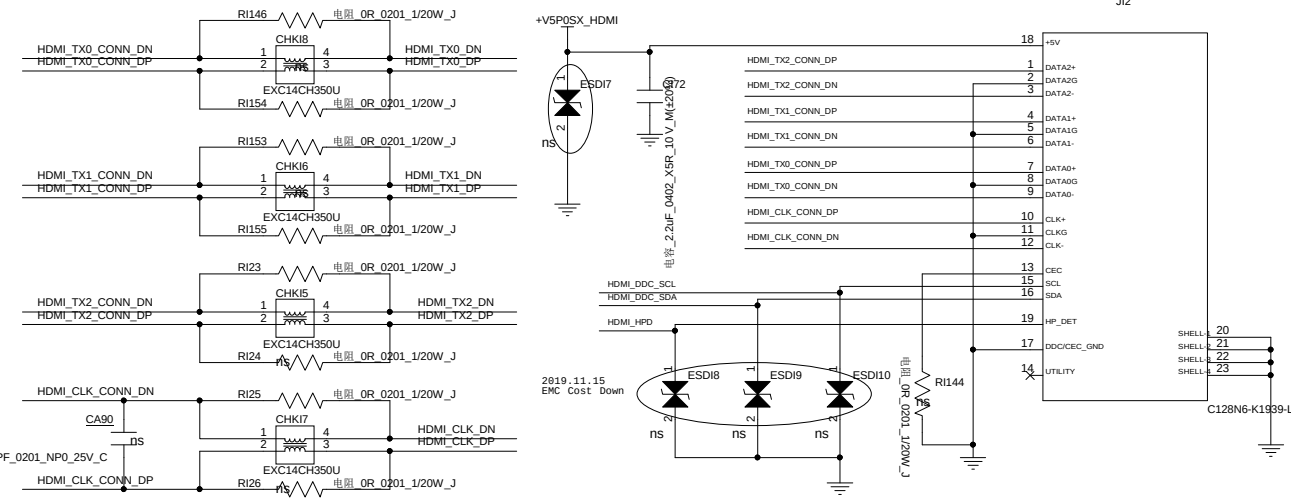

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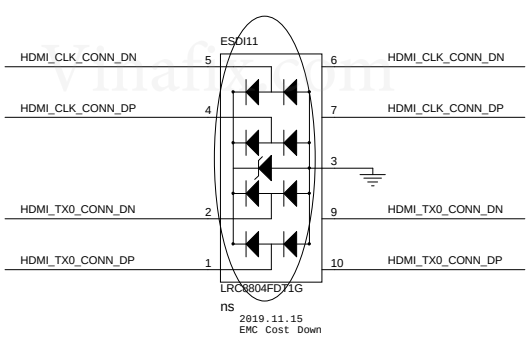
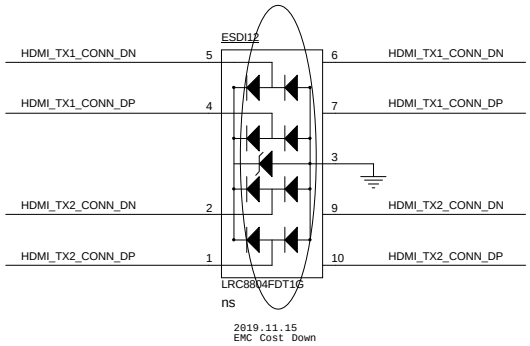
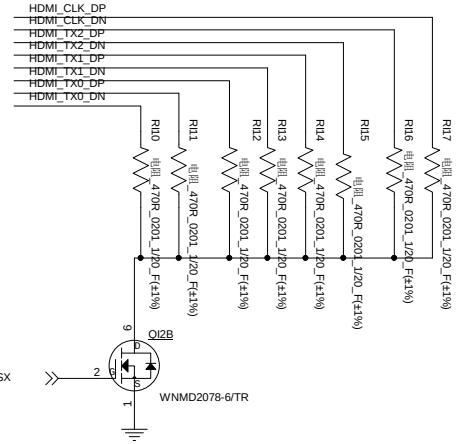
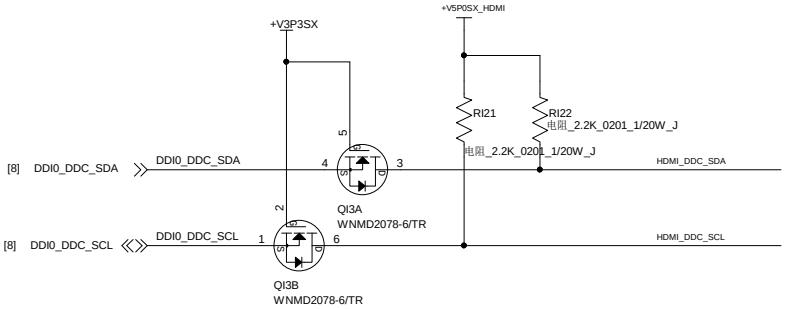
ESD









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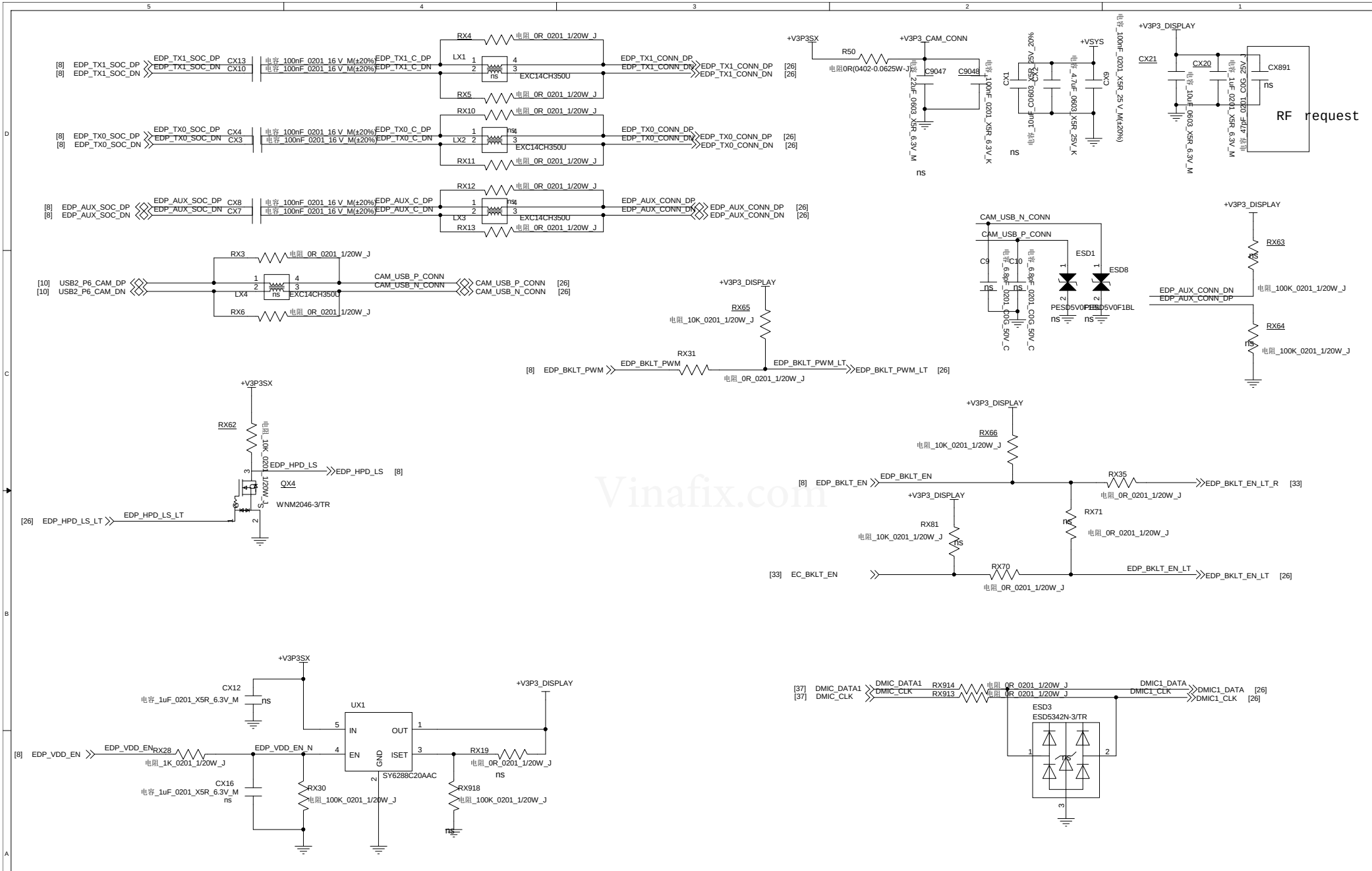

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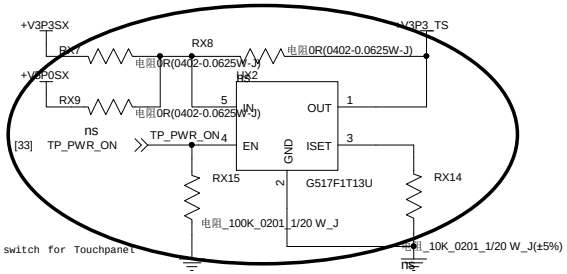
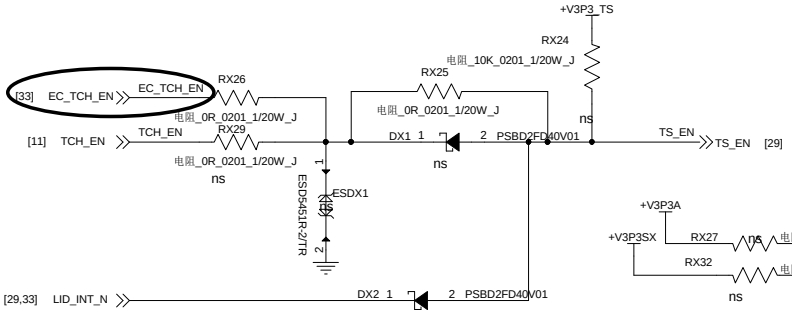
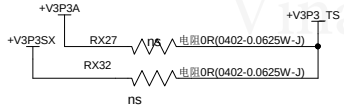
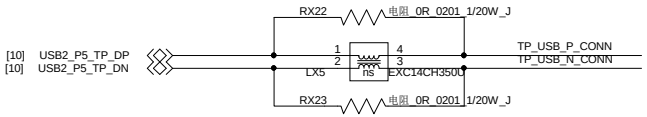
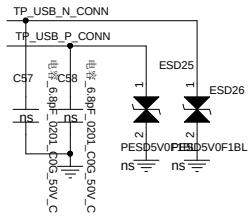


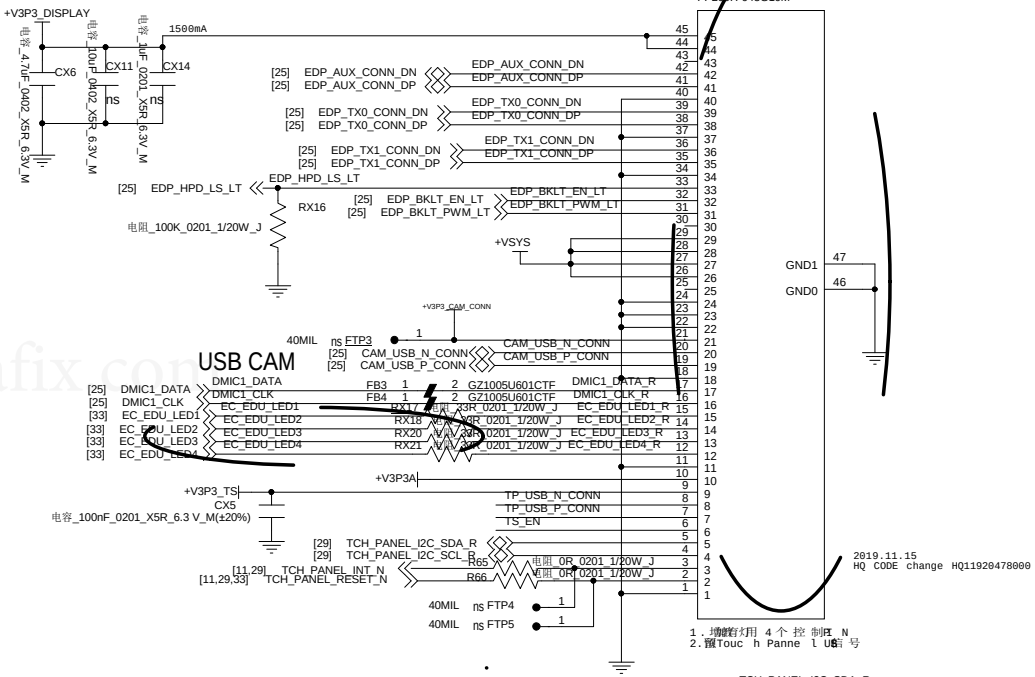
为满足 TouchPanel 的要求，需上件 Power switch

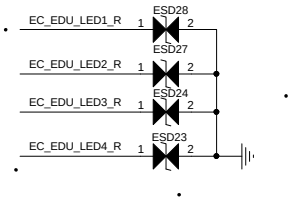


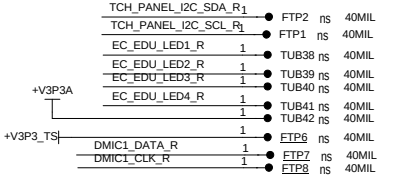












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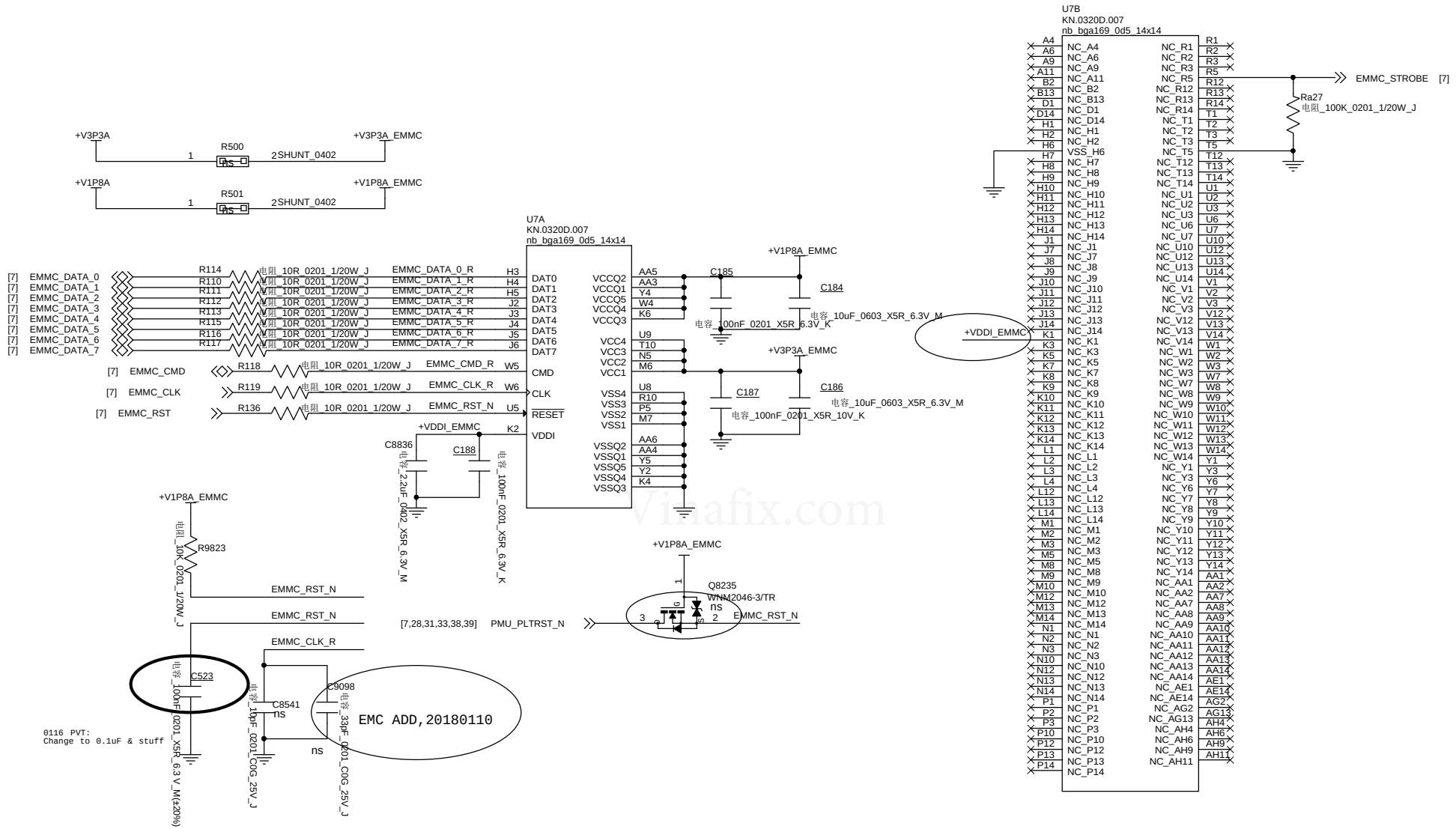

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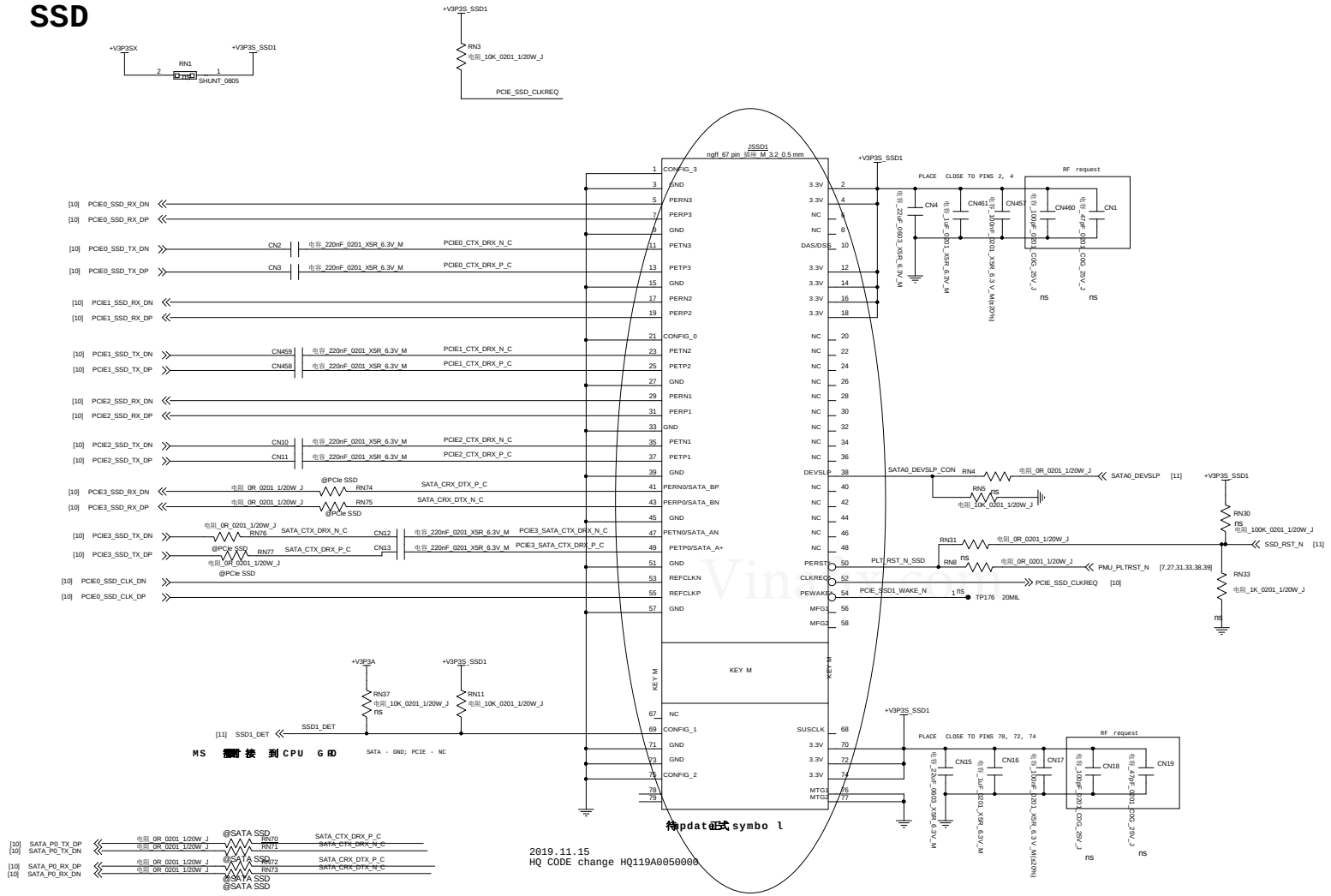

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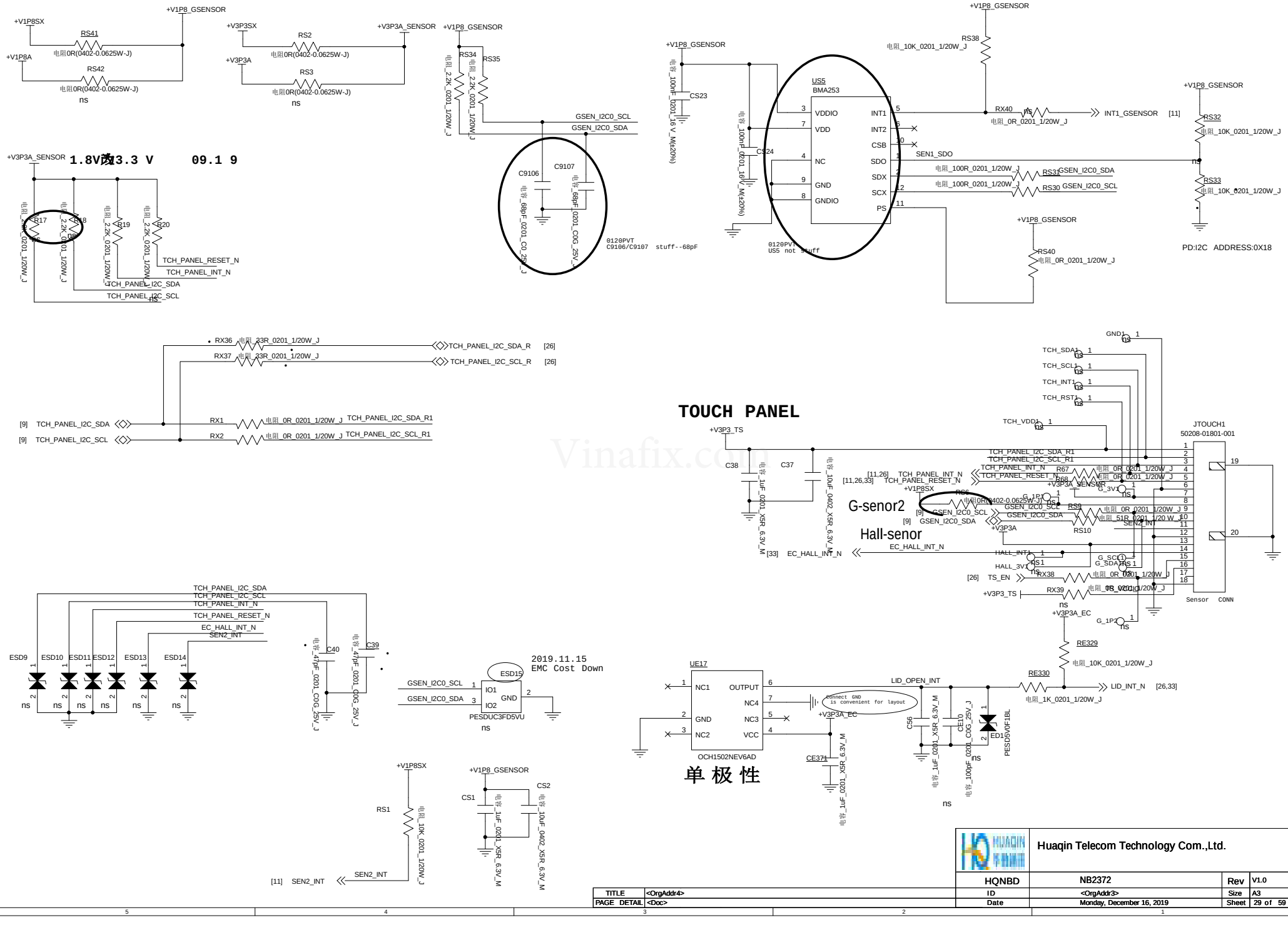

Vinafix.com

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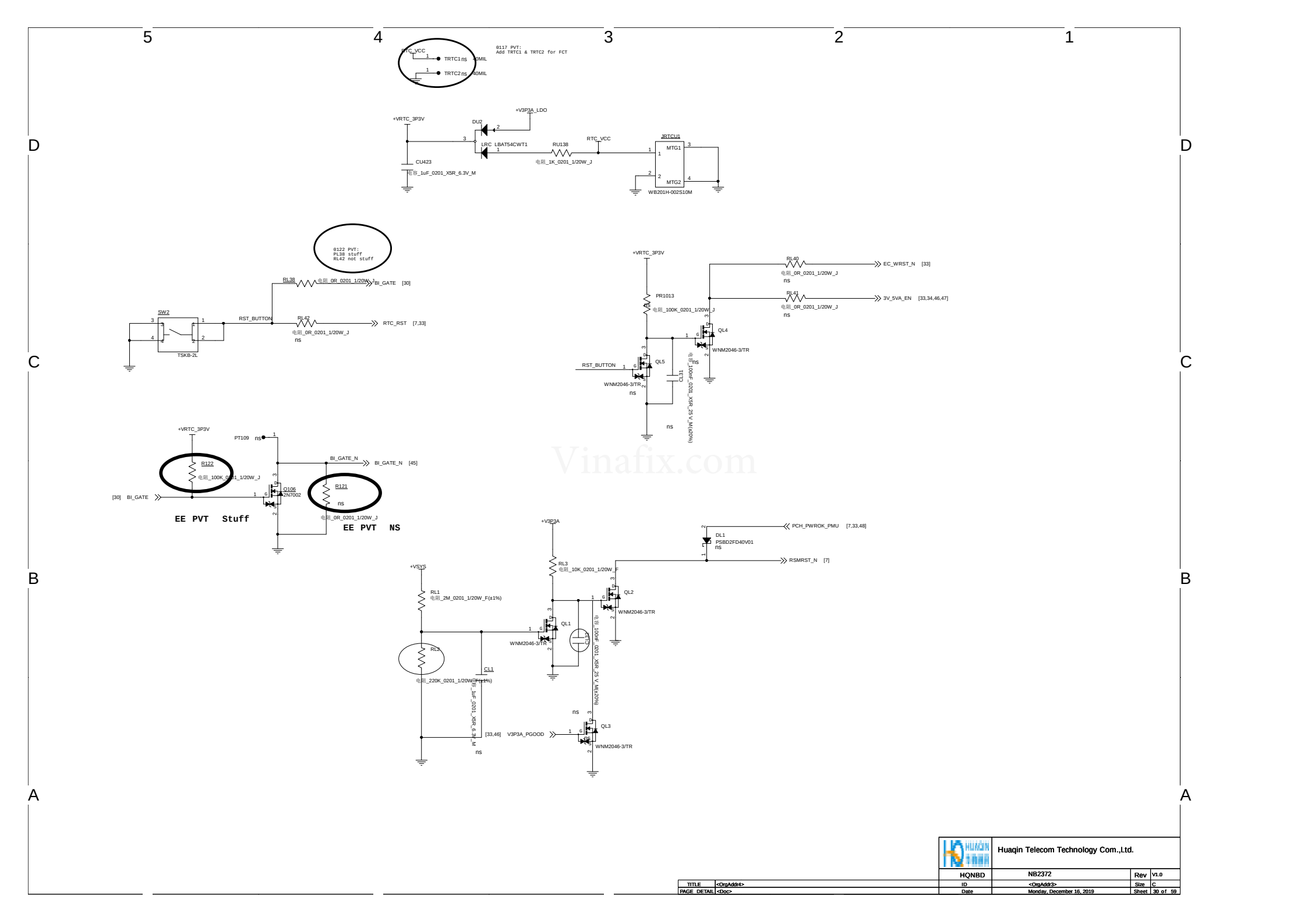

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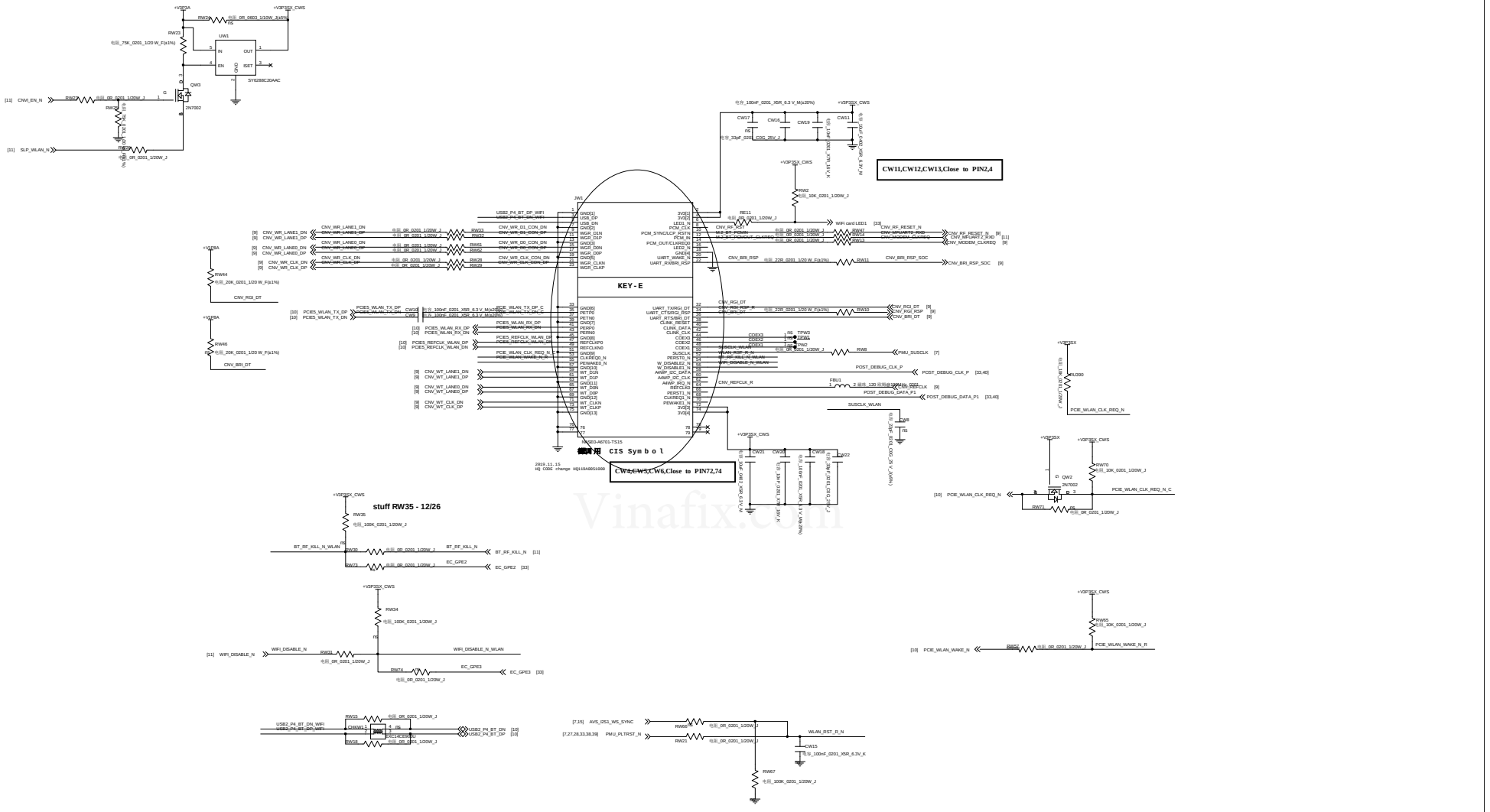

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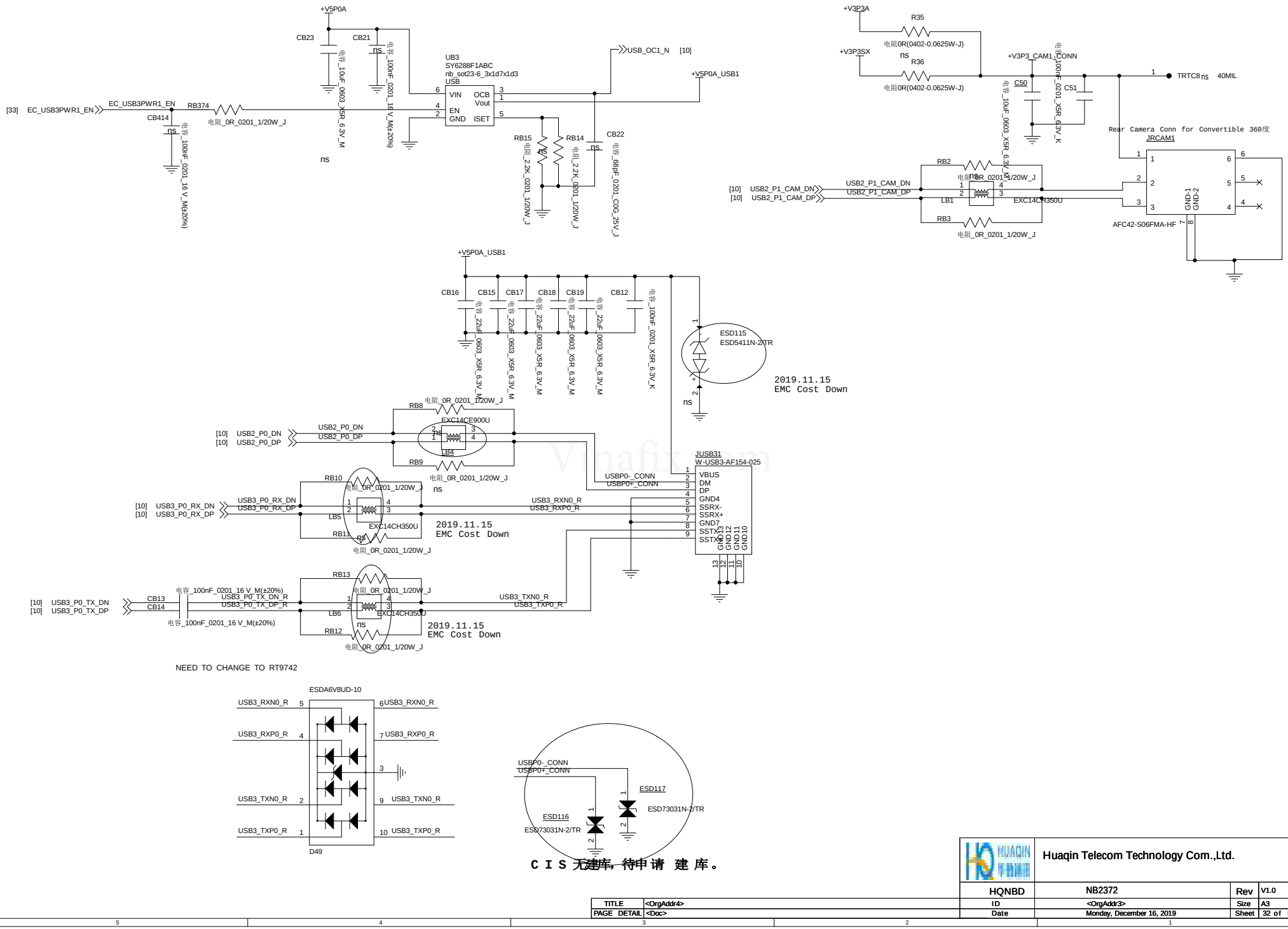

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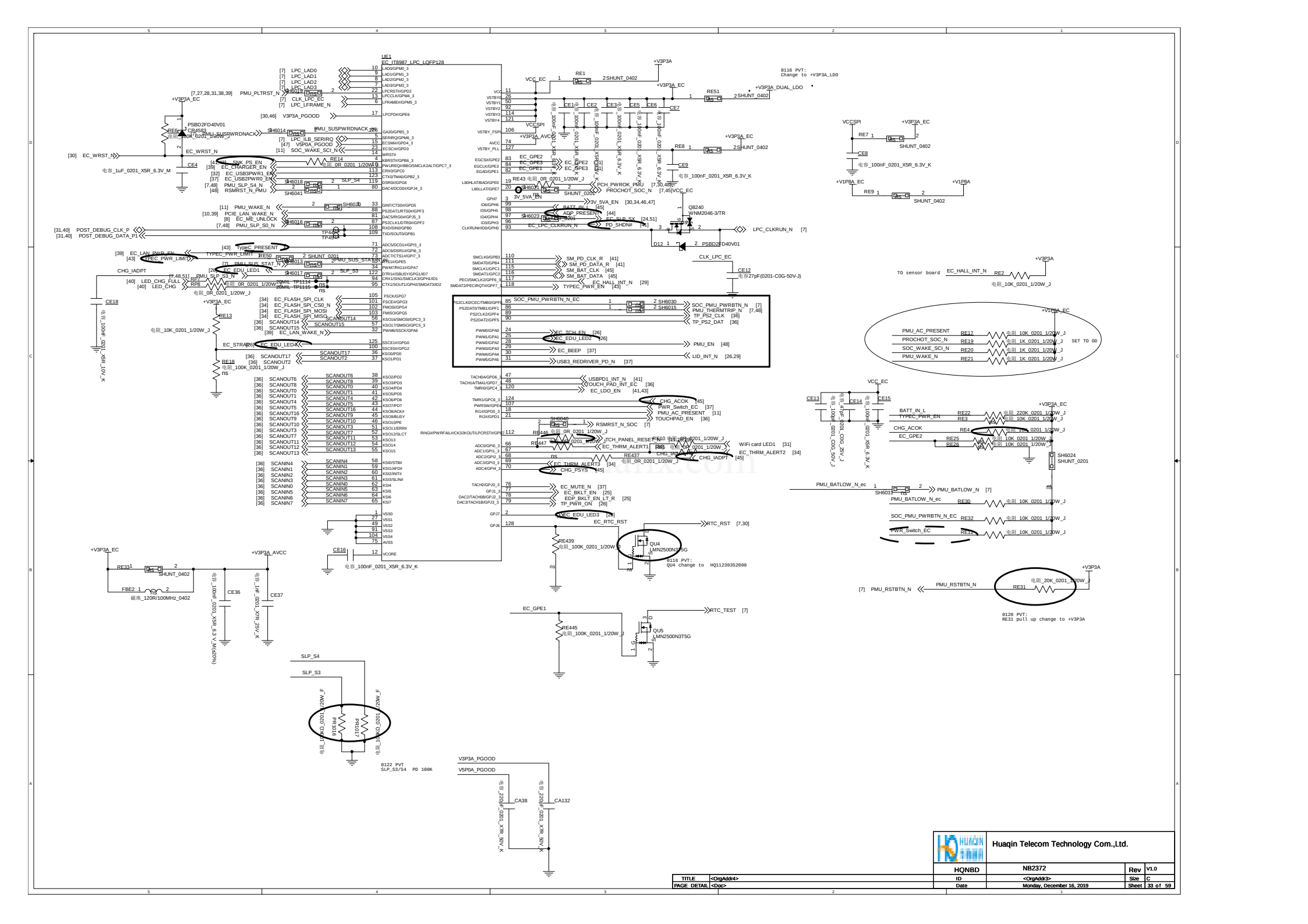

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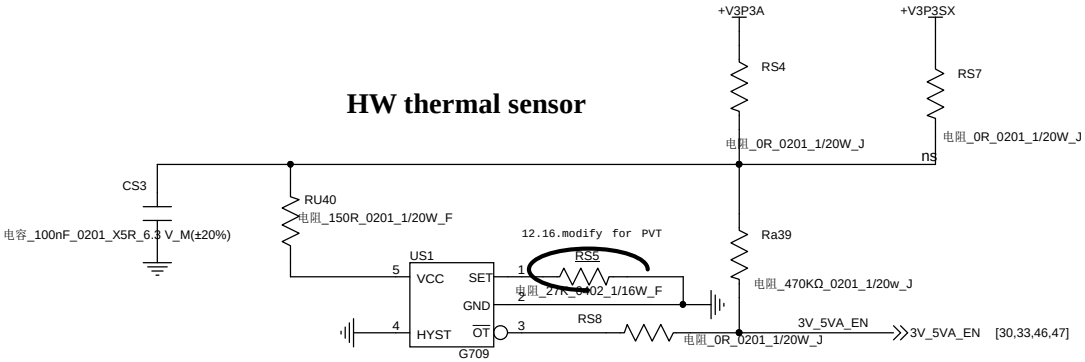
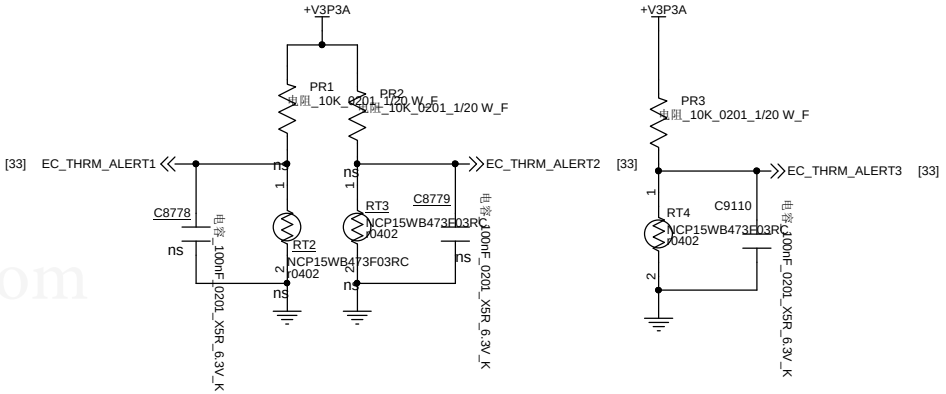
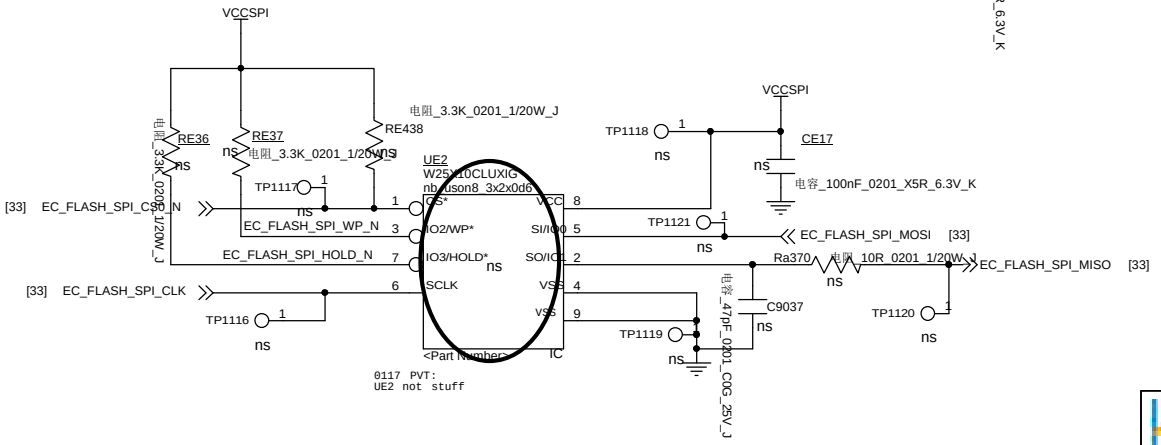
HW thermal sensor



NOTE:
HW thermal sensor ....??

US1 For HW Shutdown close to +VCGI





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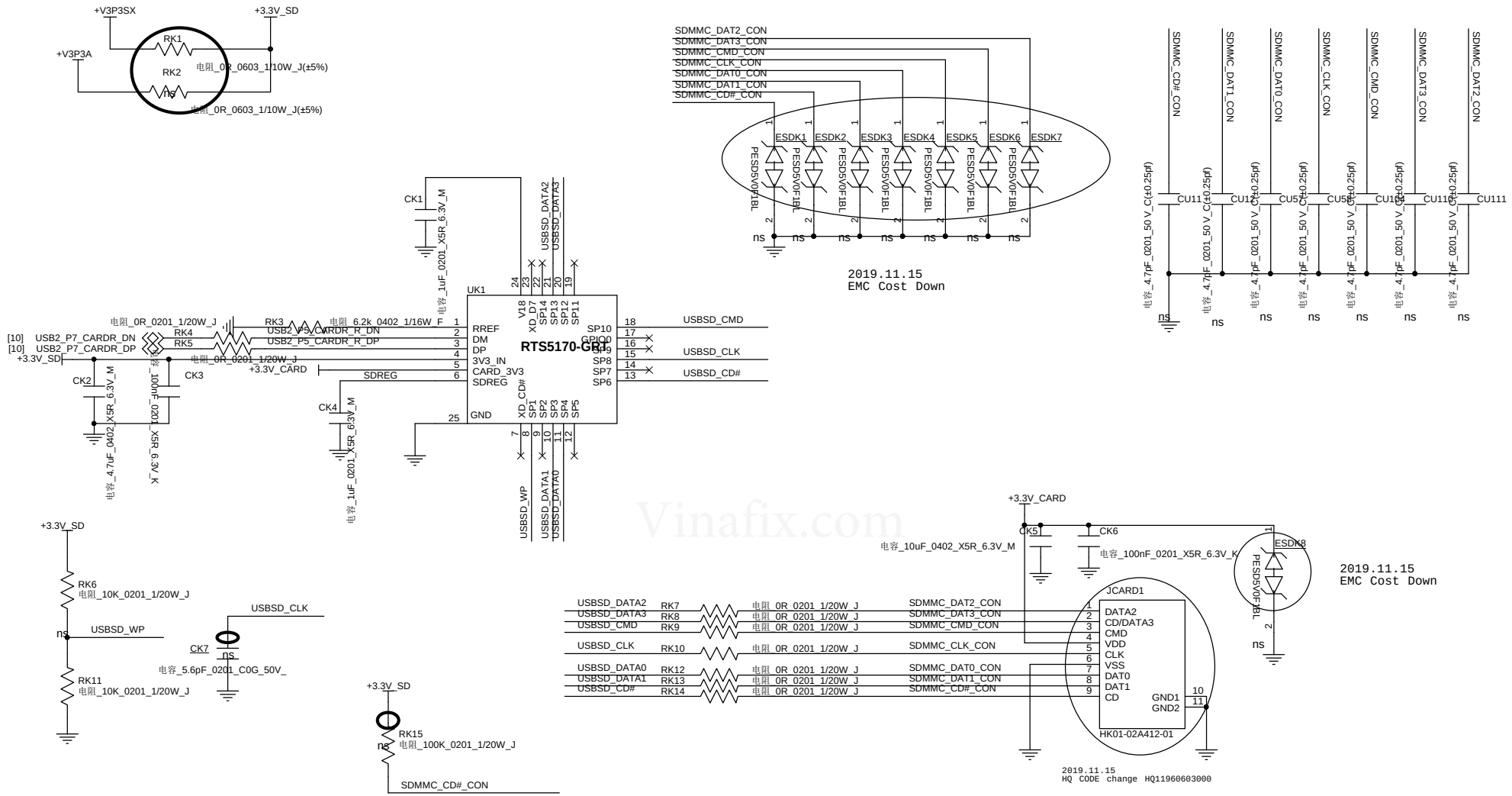

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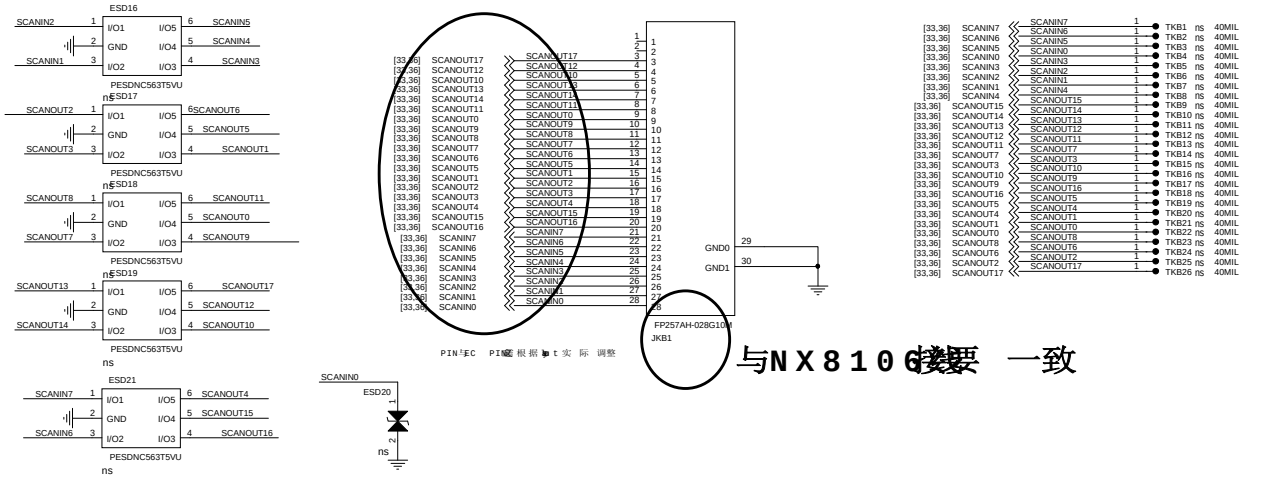
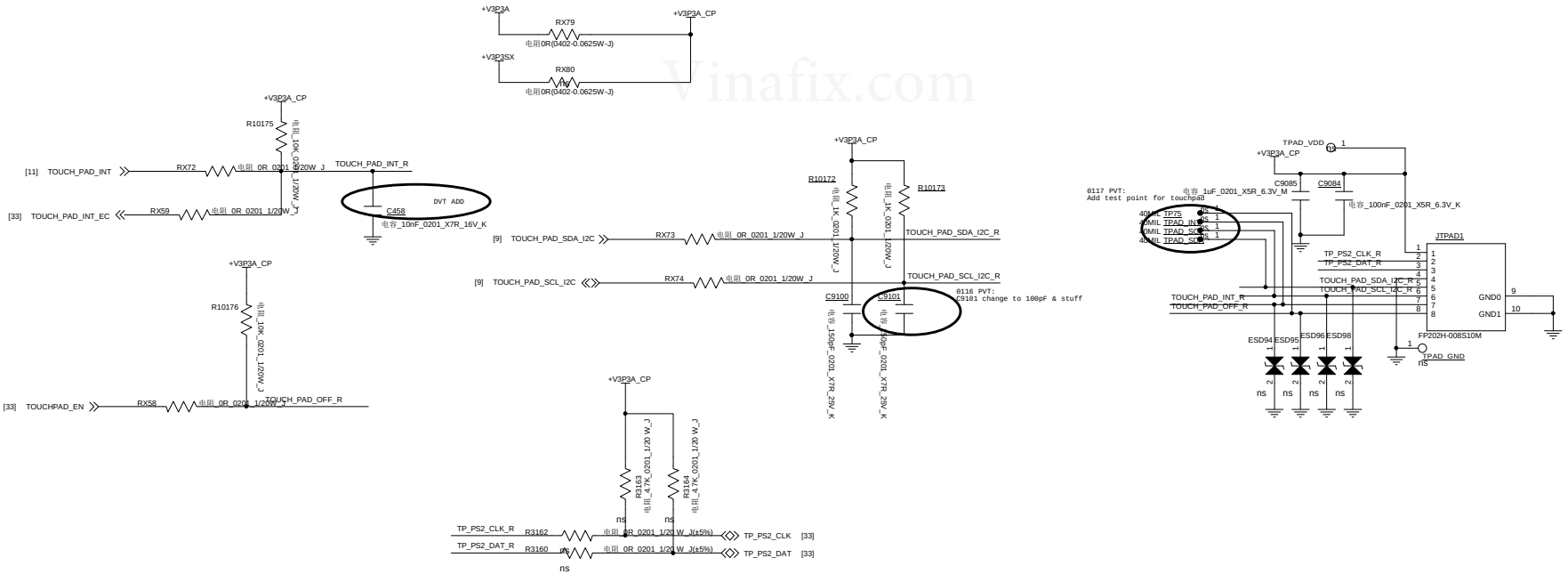


与NX8106接要 一致

Touch Pad



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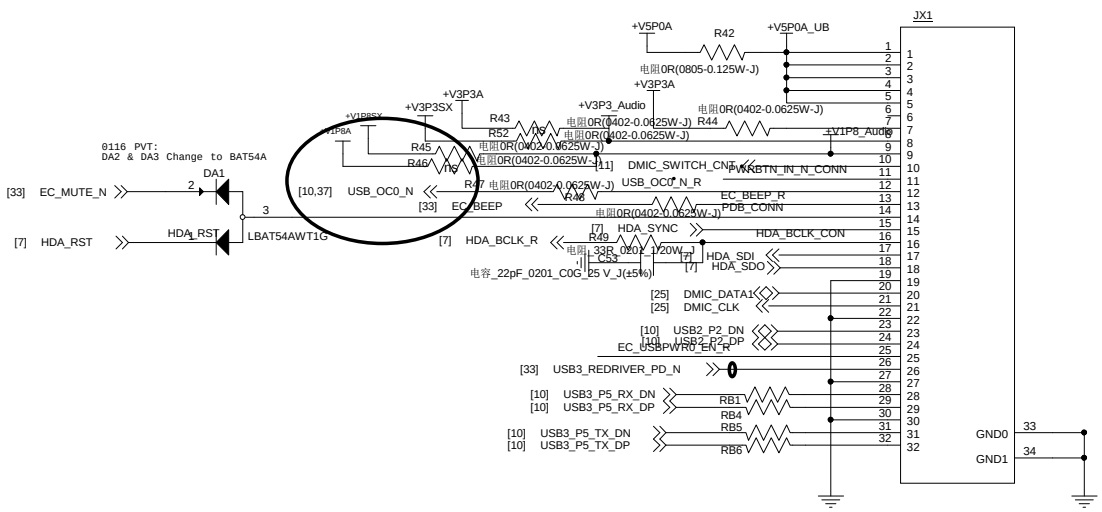
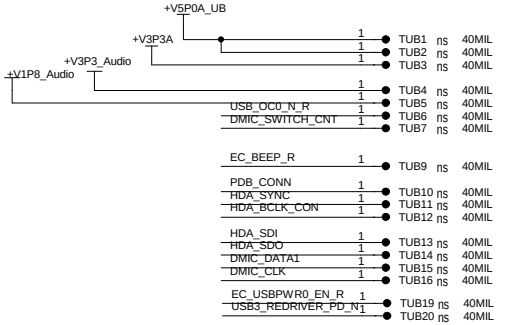
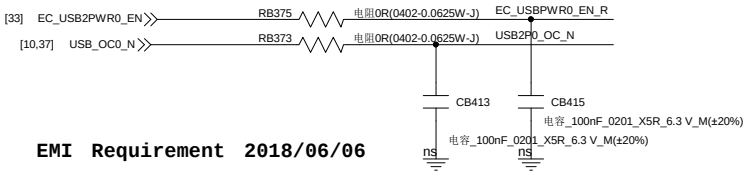
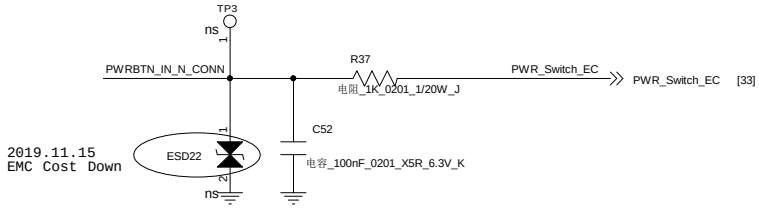






EMI Requirement 2018/06/06



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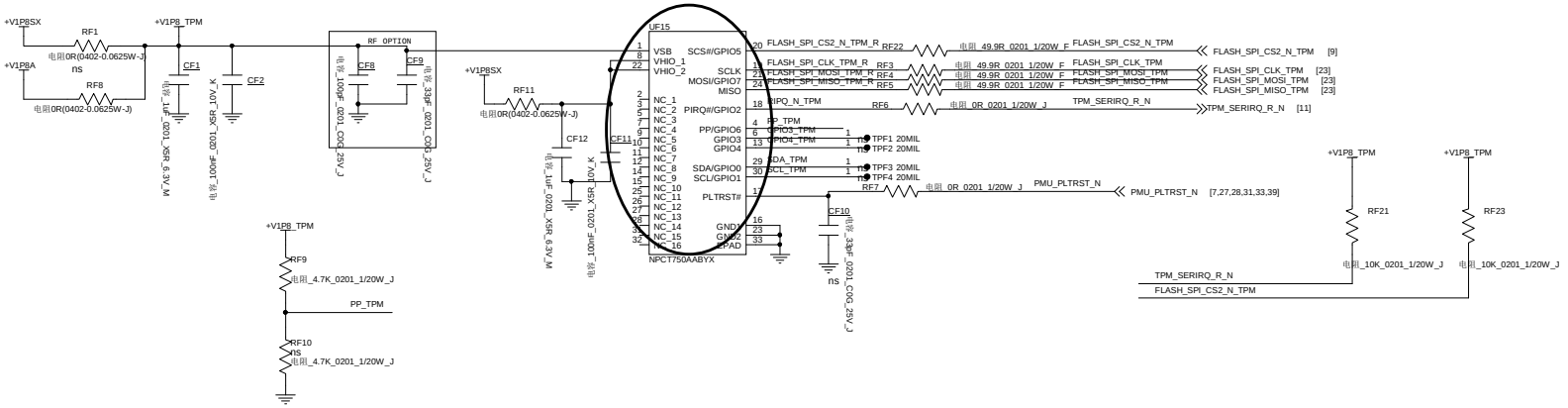

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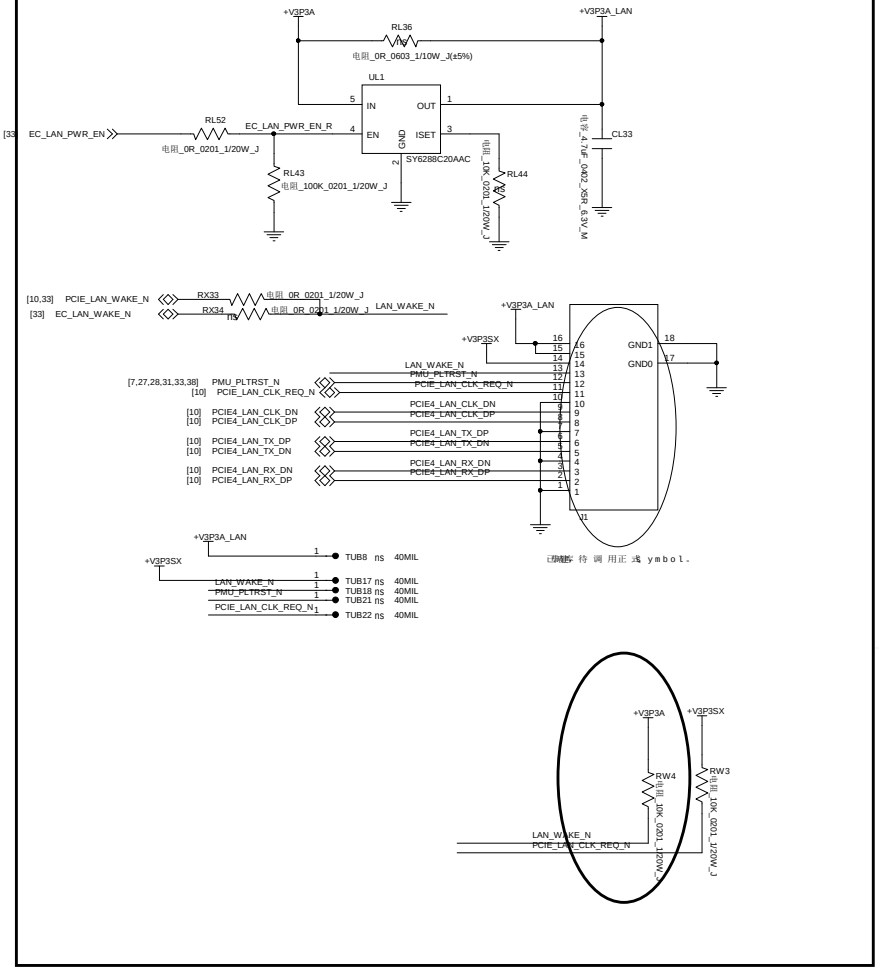
		Sheet	38 of 59

RJ45 CONN

Suport S5 LAN WAKE



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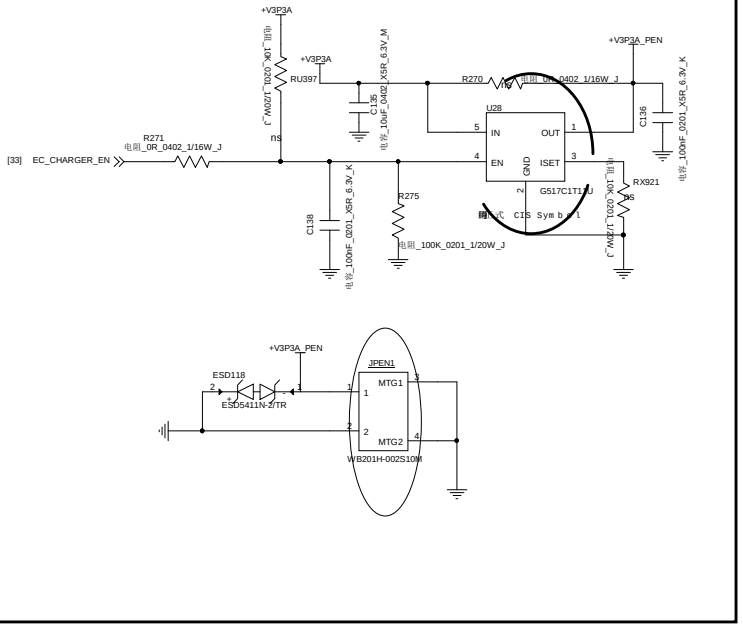

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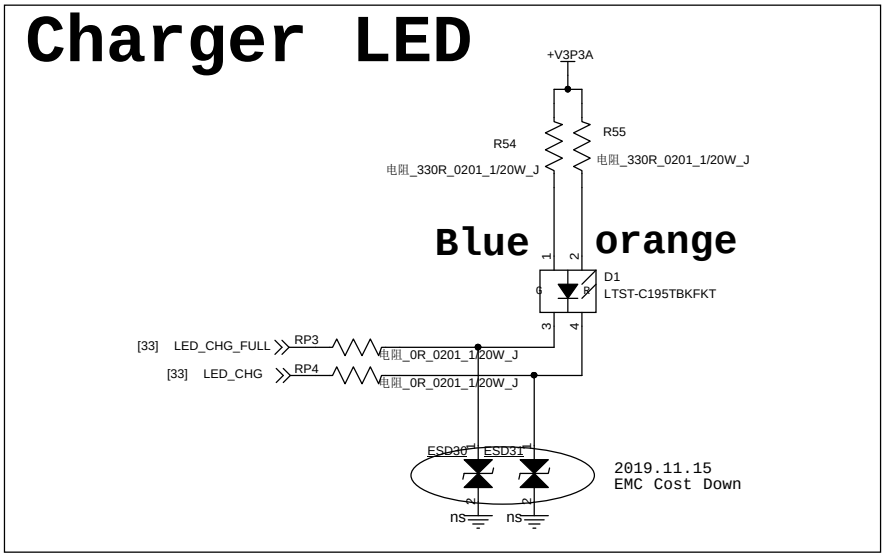
Charger LED



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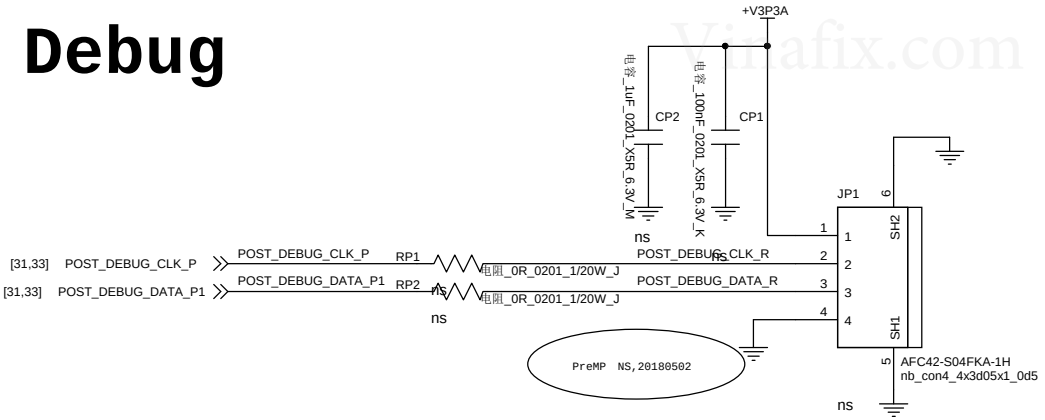

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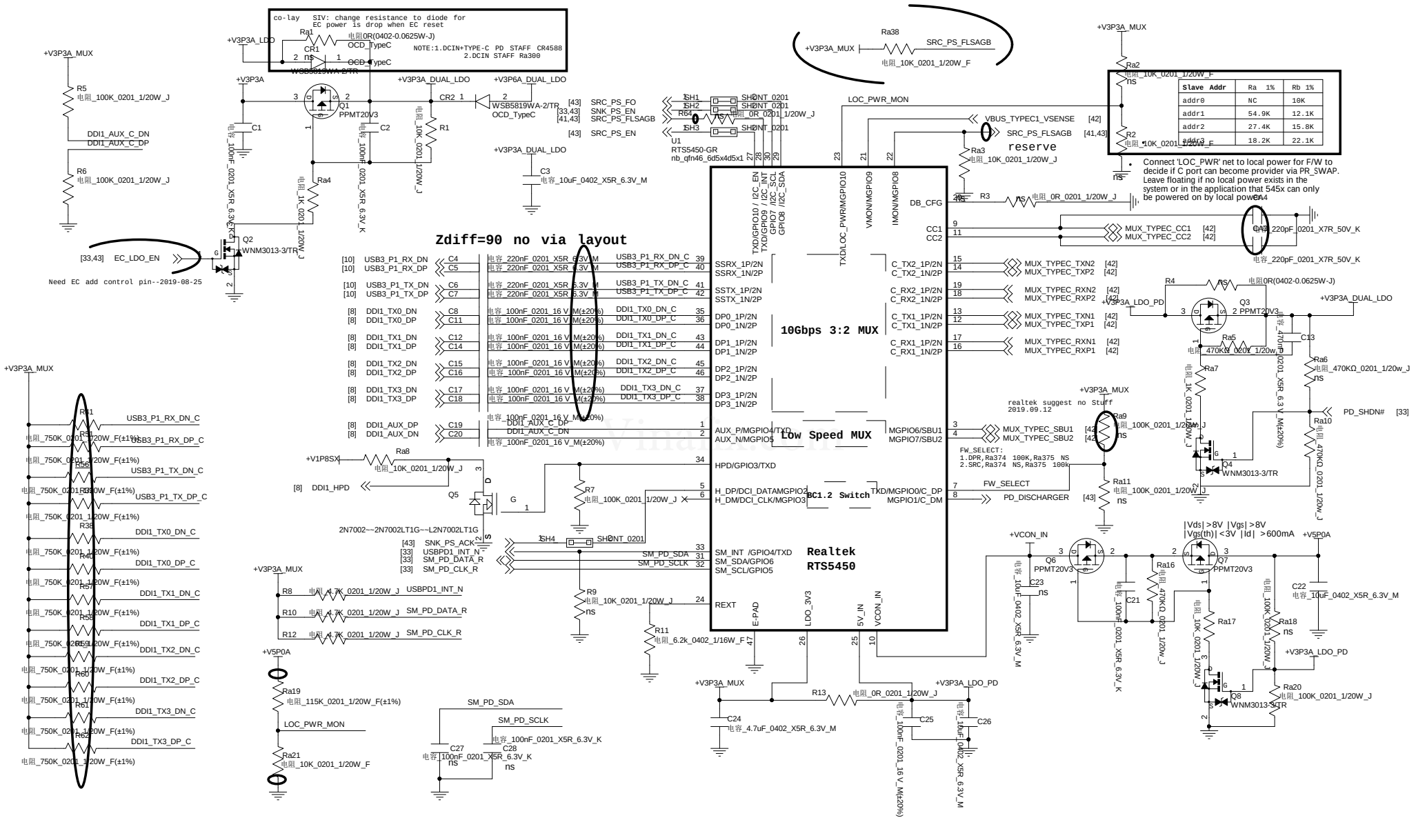

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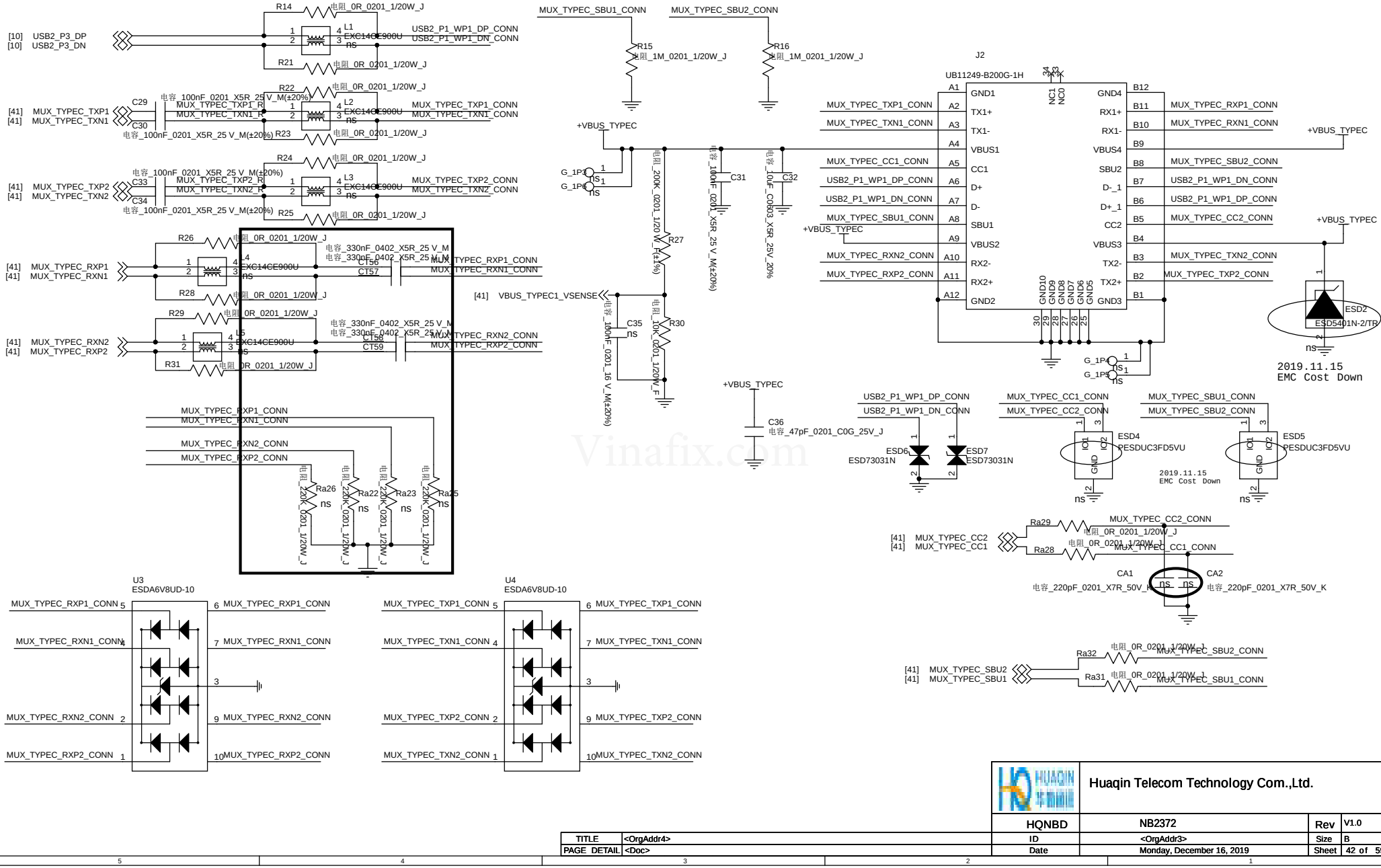

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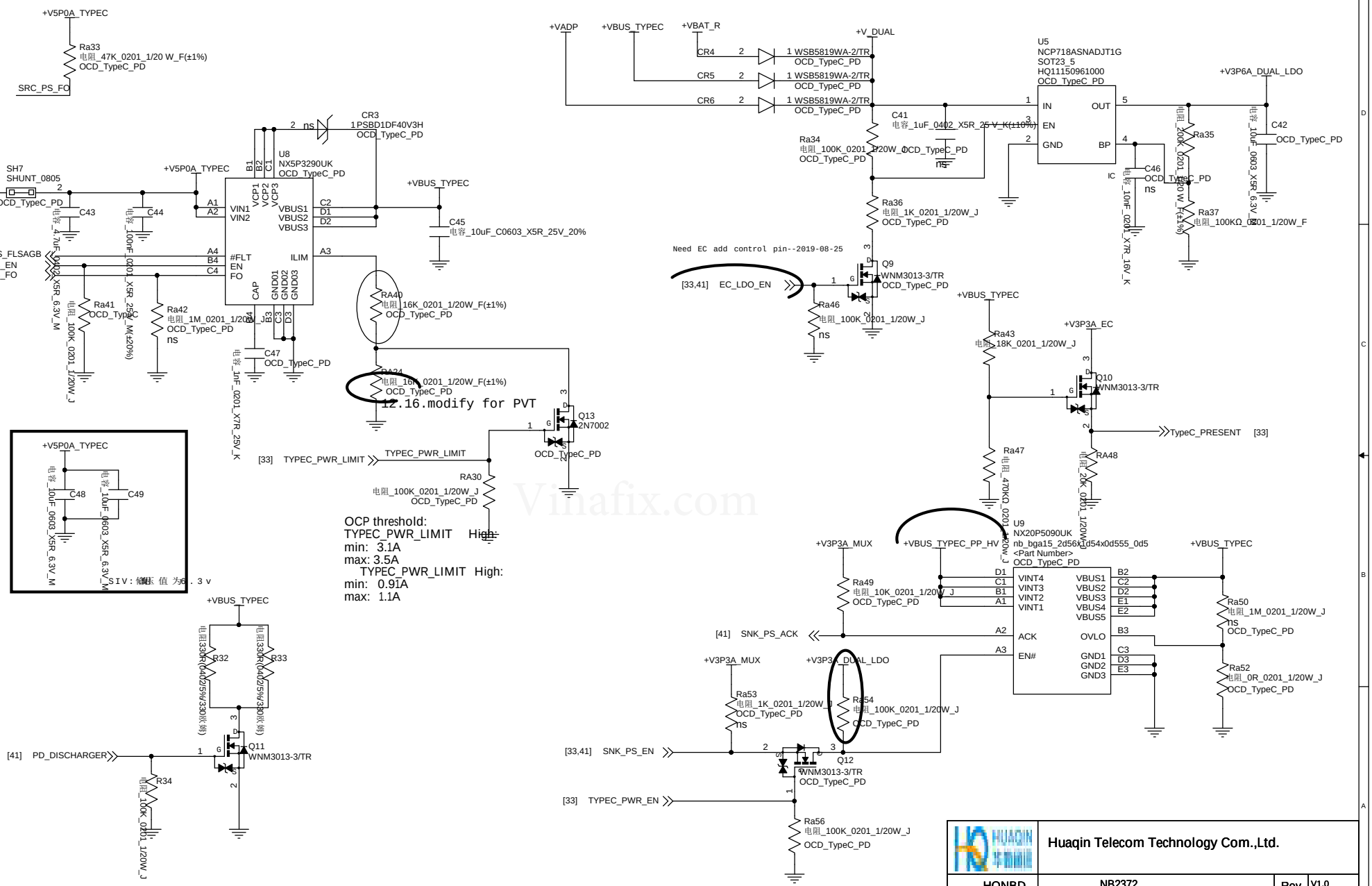

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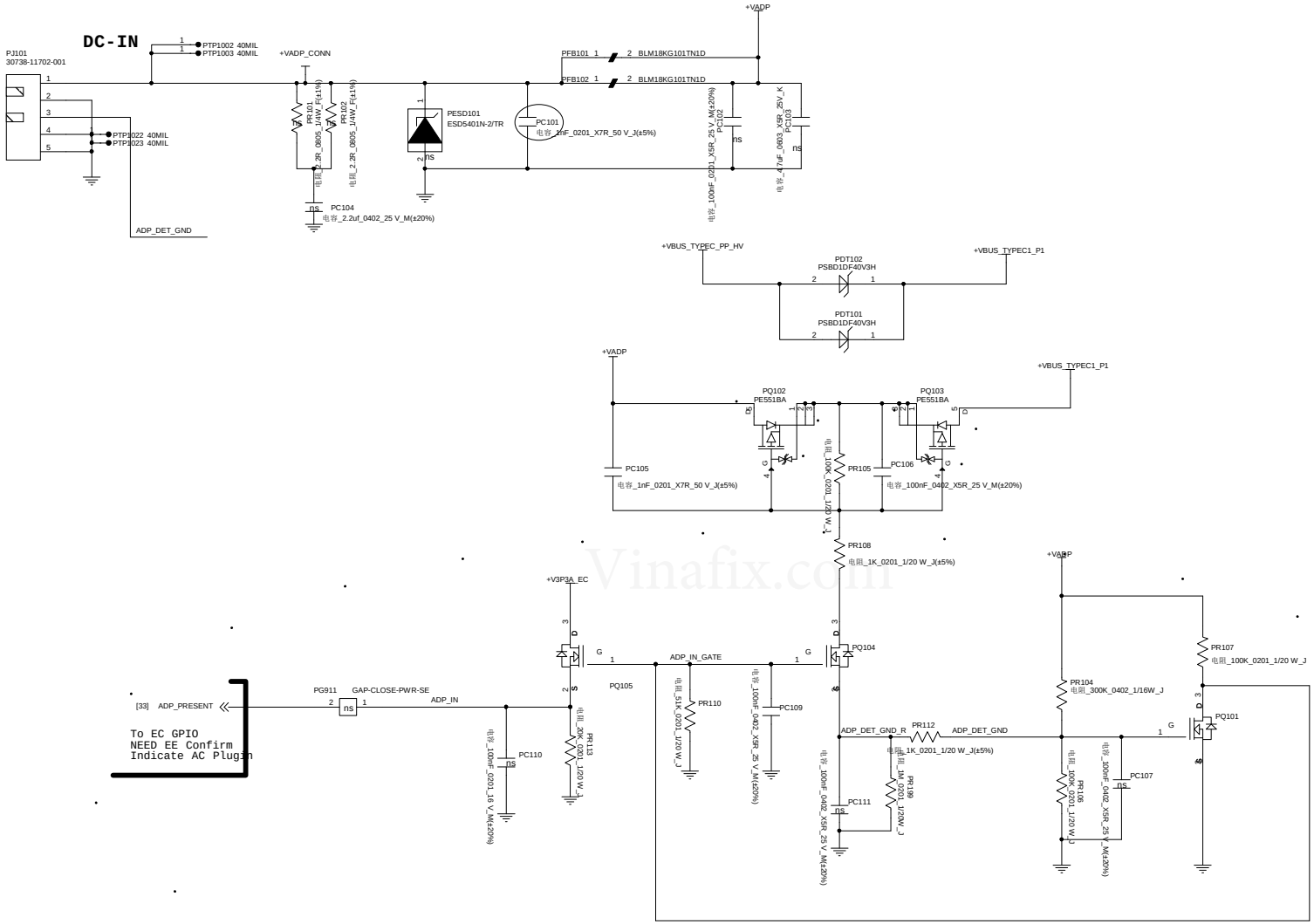

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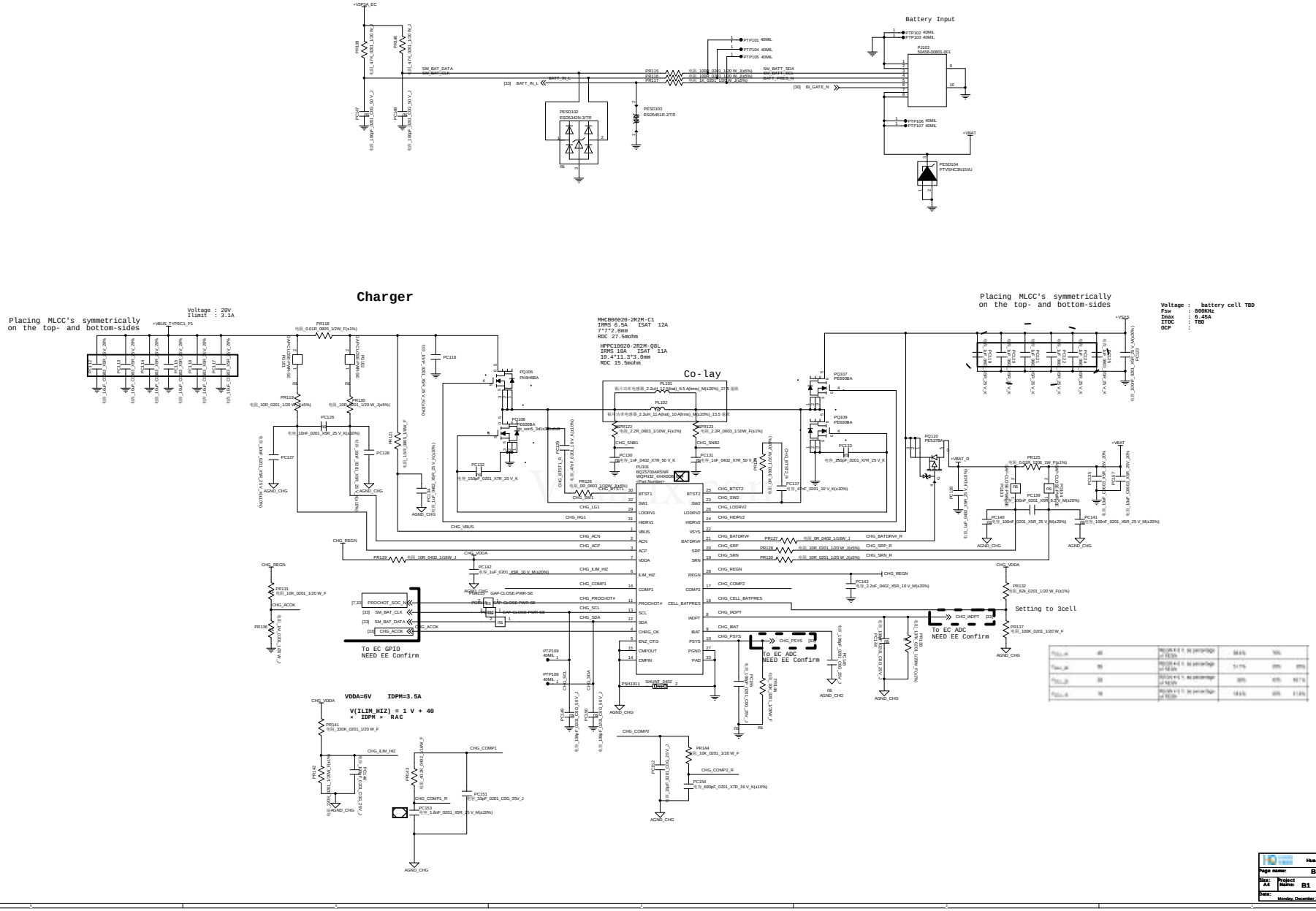
Battery Input
Charger
Placing MLCC's symmetrically on the top- and bottom-sides
Voltage : 20V
Ilimit : 3.1A
Placing MLCC's symmetrically on the top- and bottom-sides
Voltage : battery cell TBD
Fsw : 800KHz
Imax : 6.45A
ITDC : TBD
OCP :
MWCR06020-2R2M-C1
IRMS 6.5A ISAT 12A
7*7*2.0mm
RDC 27.5mohm
HPPC10020-2R2M-Q8L
IRMS 10A ISAT 11A
10.4*11.3*3.0mm
RDC 15.5mohm
Co-lay
Setting to 3cell
To EC GPIO NEED EE Confirm
To EC ADC NEED EE Confirm
To EC ADC NEED EE Confirm
VDDA=6V IDPM=3.5A
V(ILIM_HIZ) = 1 V + 40 × IDPM × RAC
Huagin Telecom Technology Com.,Ltd.
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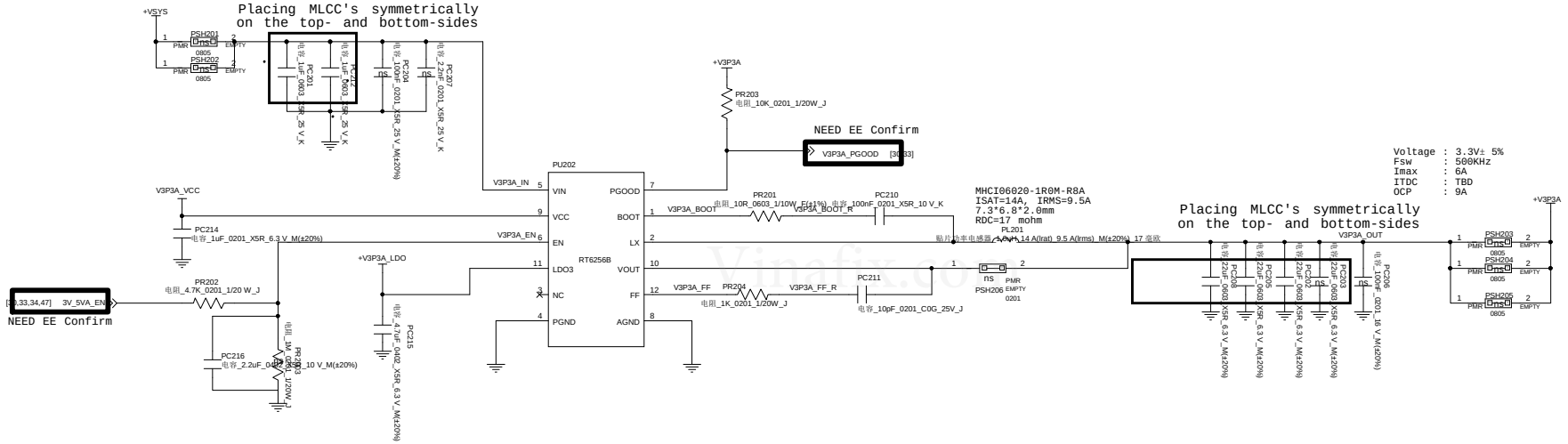
Size: A4
Project Name: B1
REV: V1.0
Date: Monday, December 16, 2019
Sheet: of 45 57



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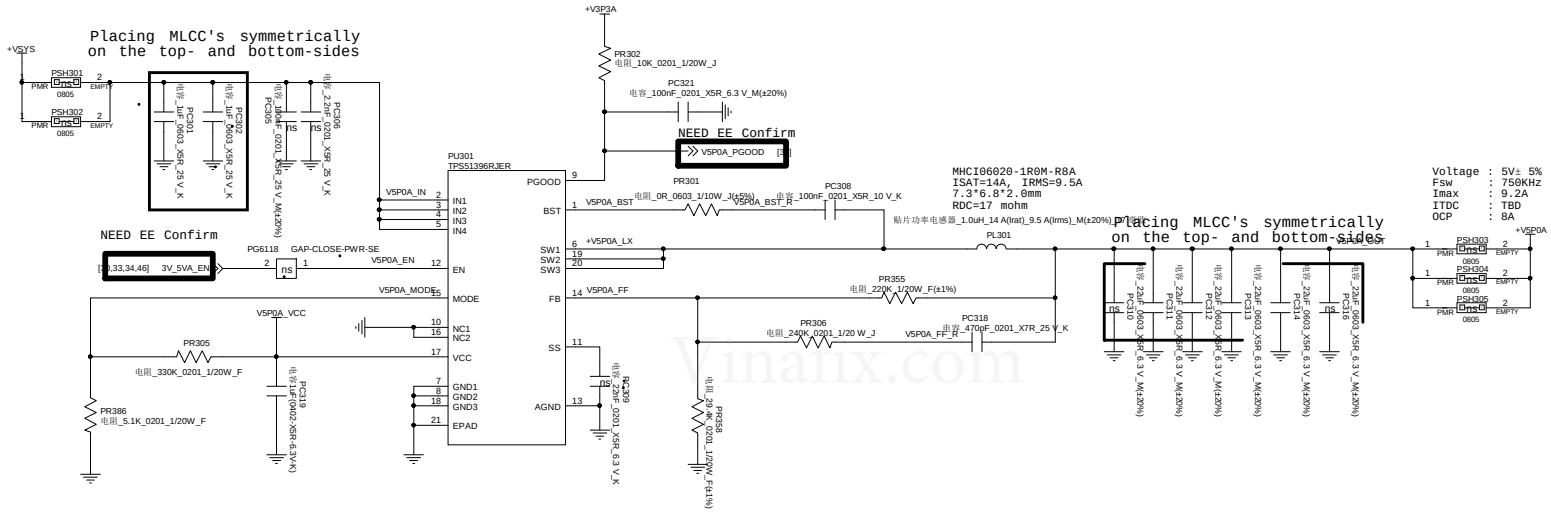

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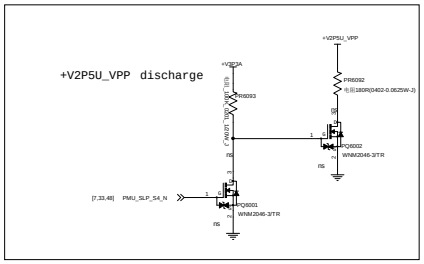
Date: Monday, December 16, 2019	Sheet: 47 of 57	

Table 2. Buck6 (DDR) Voltage Selection

DDR_SEL Pin State	Buck6 Nominal Output Voltage	DDR Technology
H	1.2V	LPDDR3
Floating	1.2V	DDR4 (optional)
L	1.1V	LPDDR4



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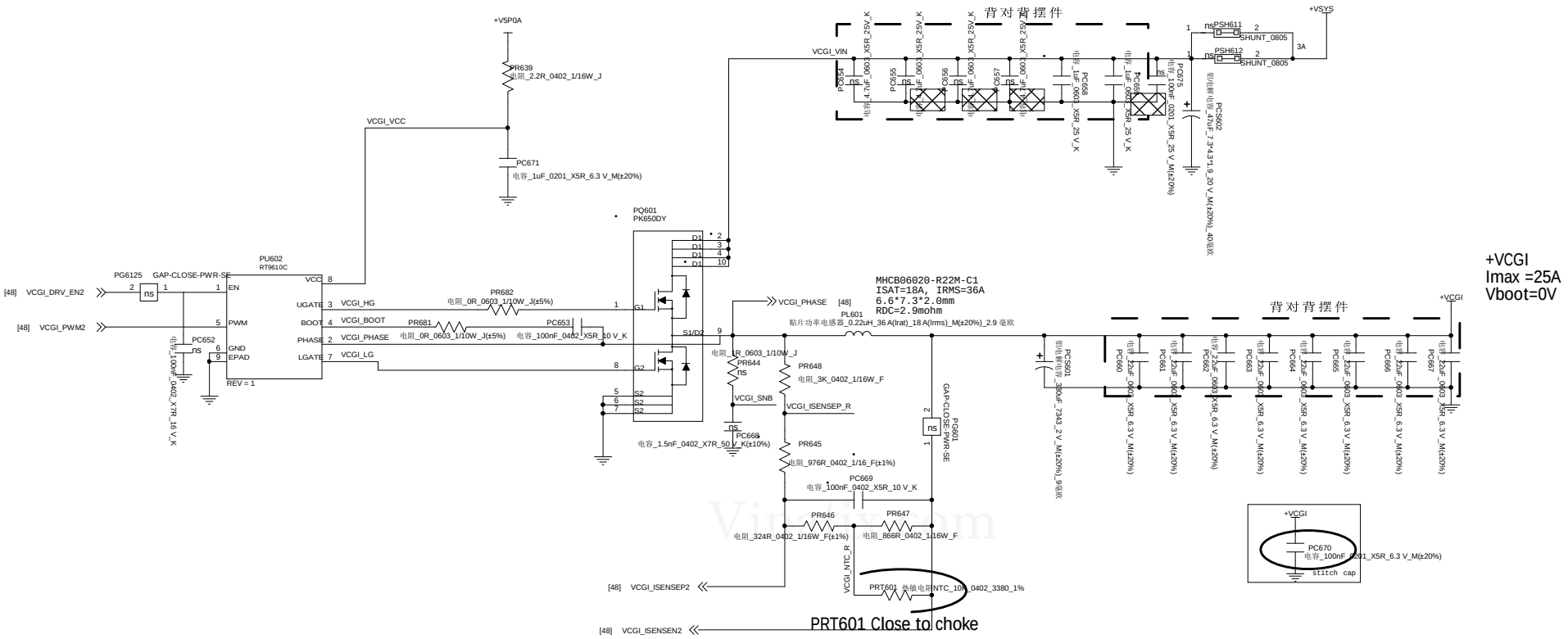
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	46 of 57

VCGI



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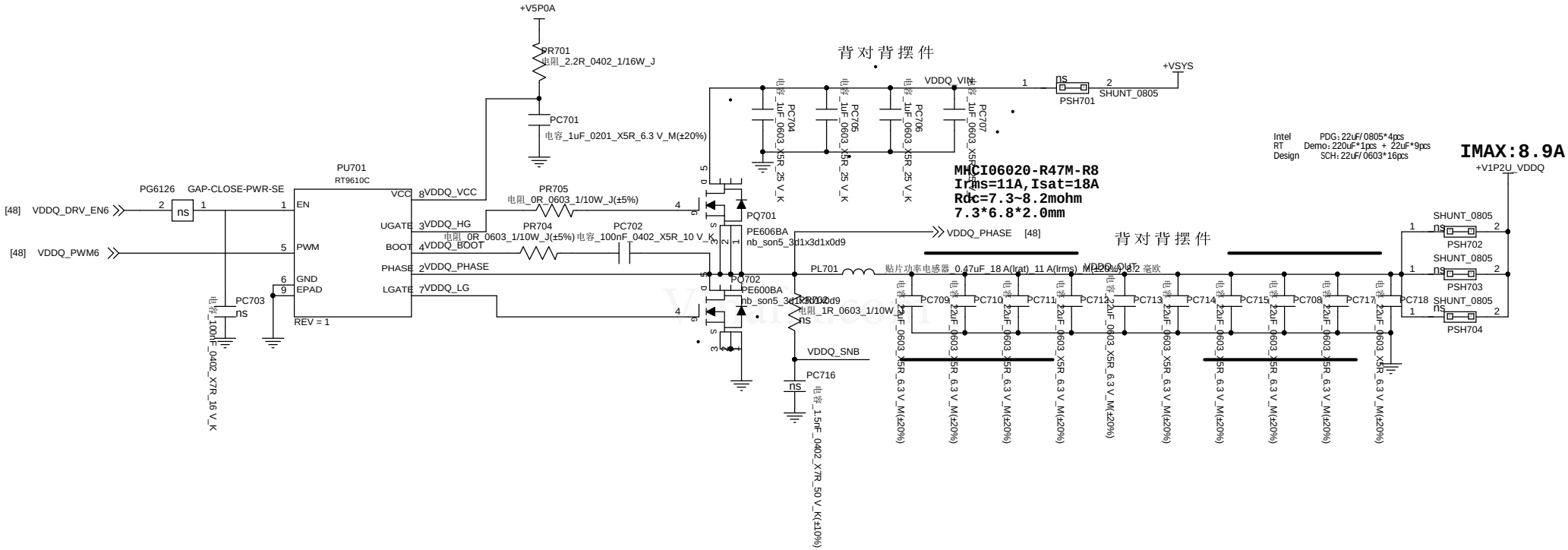
HQNBD	NB2372	Rev	<RevCode>
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	Custom
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	49 of 57

VDDQ



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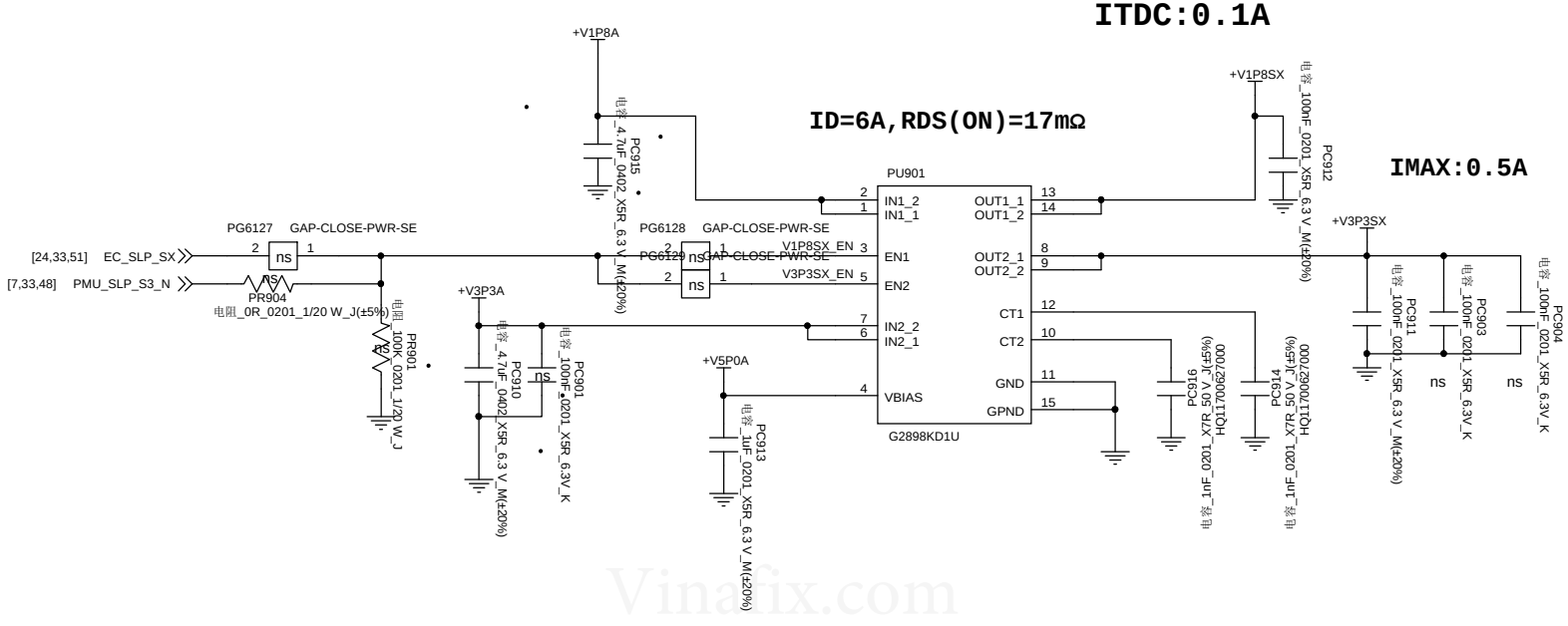
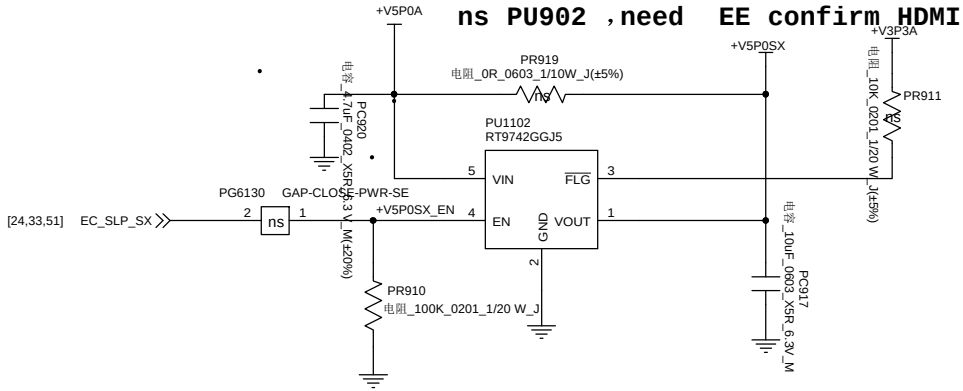
HQNBD	NB2372	Rev	<RevCode>
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	B
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	50 of 57

V3P3SX V5P0SX V1P8SX



ns PU902 ,need EE confirm HDMI sequence



Huaqin Telecom Technology Com.,Ltd.			
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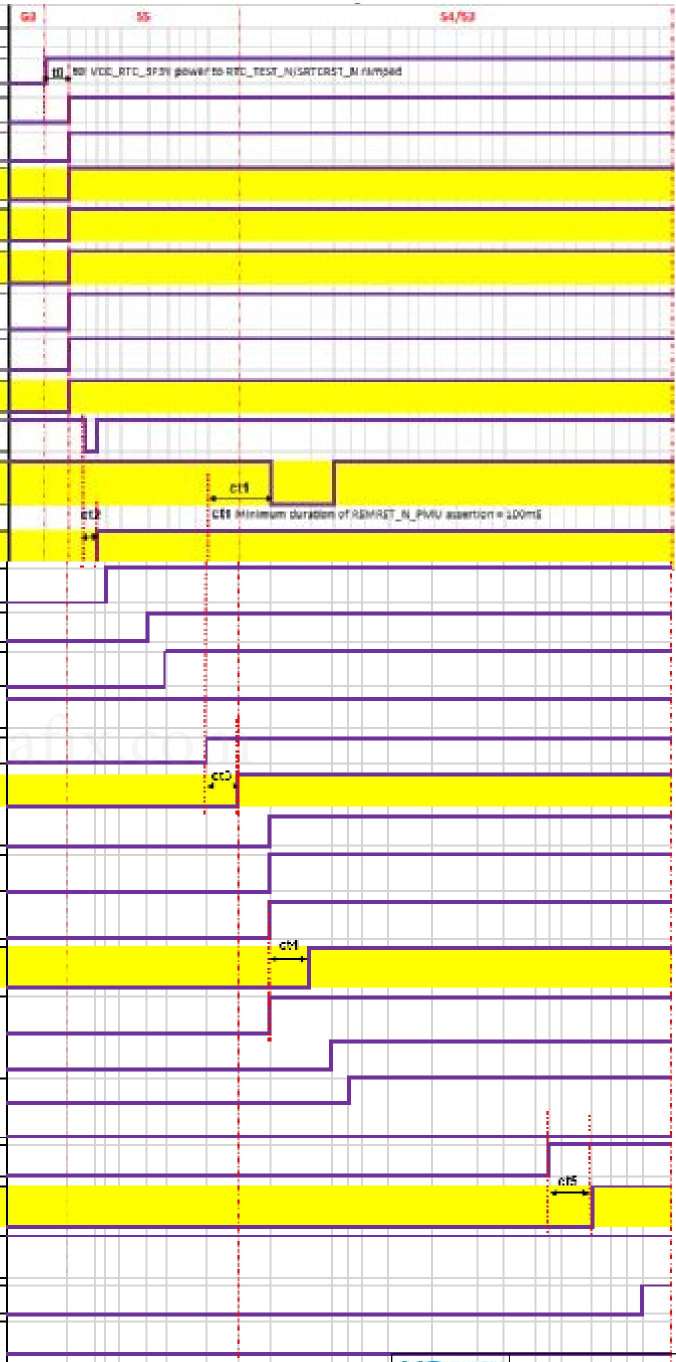
TITLE	<OrgAddr4>	ID	<OrgAddr3>
PAGE_DETAIL	<Doc>	Date	Monday, December 16, 2019
		Size	B
		Sheet	51 of 57

	Huaqin Telecom Technology Com.,Ltd.
Page name:	POWER DELIVERY_Load switch
Size: A4	Project Name: B1
REV:	V1.0
Date:	Monday, December 16, 2019
Sheet:	52 of 57

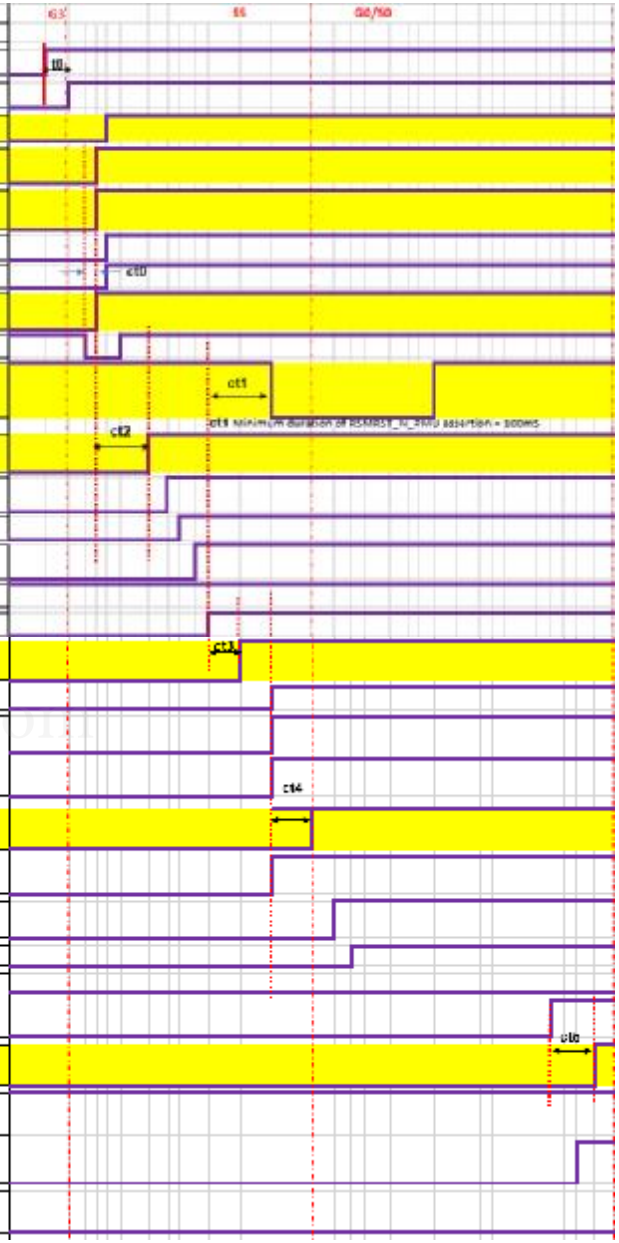
Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Monday, December 16, 2019	Sheet 53 of 57		

返回		INTEL_SPEC			EC setting		
Function	Net Name	Label	min	max	Label	setting	Note
PWR	+VRTC_SOC					NA	
PCH_IN	RTEST_N	t0	10ms	20ms		Auto	
EC_I	ADP_PRESENT					NA	
EC_O	PMU_AC_PRESENT					1ms	ADP_PRESENT high to PMU_AC_PRESENT high
EC_O	PD_SHDN#					1ms	ADP_PRESENT high to PD_SHDN# high
EC_O	V3P3A_EN					2ms	ADP_PRESENT high to V3P3A_EN high
PWR	+V3P3A&+V3P3A_SOC					NA	
VR_O	V3P3A_PGOOD					NA	
EC_O	EC_V5P0A_EN					2ms	ADP_PRESENT high to EC_V5P0A_EN
EC_I	PWR_Switch_EC					50ms	ON/OFF de-bance min 50ms
EC_O	SOC_PMU_PWRBTN_N				ct1	100ms	Minimum duration of RSMRST_N_PMU assertion = 100mS
EC_O	PMU_EN				ct2	6ms	PWR_Switch_EC delay 1ms
PMIC_OUT	+VNN					NA	
PMIC_OUT	+V1P8A					NA	
PMIC_OUT	+V1P2A					NA	
PCH_OUT	PMU_THERMTRIP_N						
EC_I	RSMRST_N_PMU						
EC_O	RSMRST_N_SOC	ct3	10	no requirement	ct3	2ms	RSMRST_N_PMU high to RSMRST_N_SOC high
PCH_OUT	PMU_SUSCLK						
PCH_OUT	PMU_SLP_S4_N						
PCH_OUT	PMU_SLP_S3_N						
EC_OUT	EC_SLP_S4				ct4	1ms	EC_SLP_S4 high to PMU_SLP_S3_N high
PCH_OUT	PMU_SLP_S0_N						
VR_O	PVDDQ						
PMIC_O	+V1P05S						
VR_O	PVCCI						
EC_I	PCH_PWROK_PMU						
EC_OUT	PCH_PWROK_SOC	t11,t15	5	no requirement	ct5	2ms	PCH_PWROK_PMU high to PCH_PWROK_SOC high
PCH_OUT	EMMC_RST						
PCH_OUT	PMU_SUS_STAT_N						
PCH_OUT	SOC_PMU_PLTRST_N						

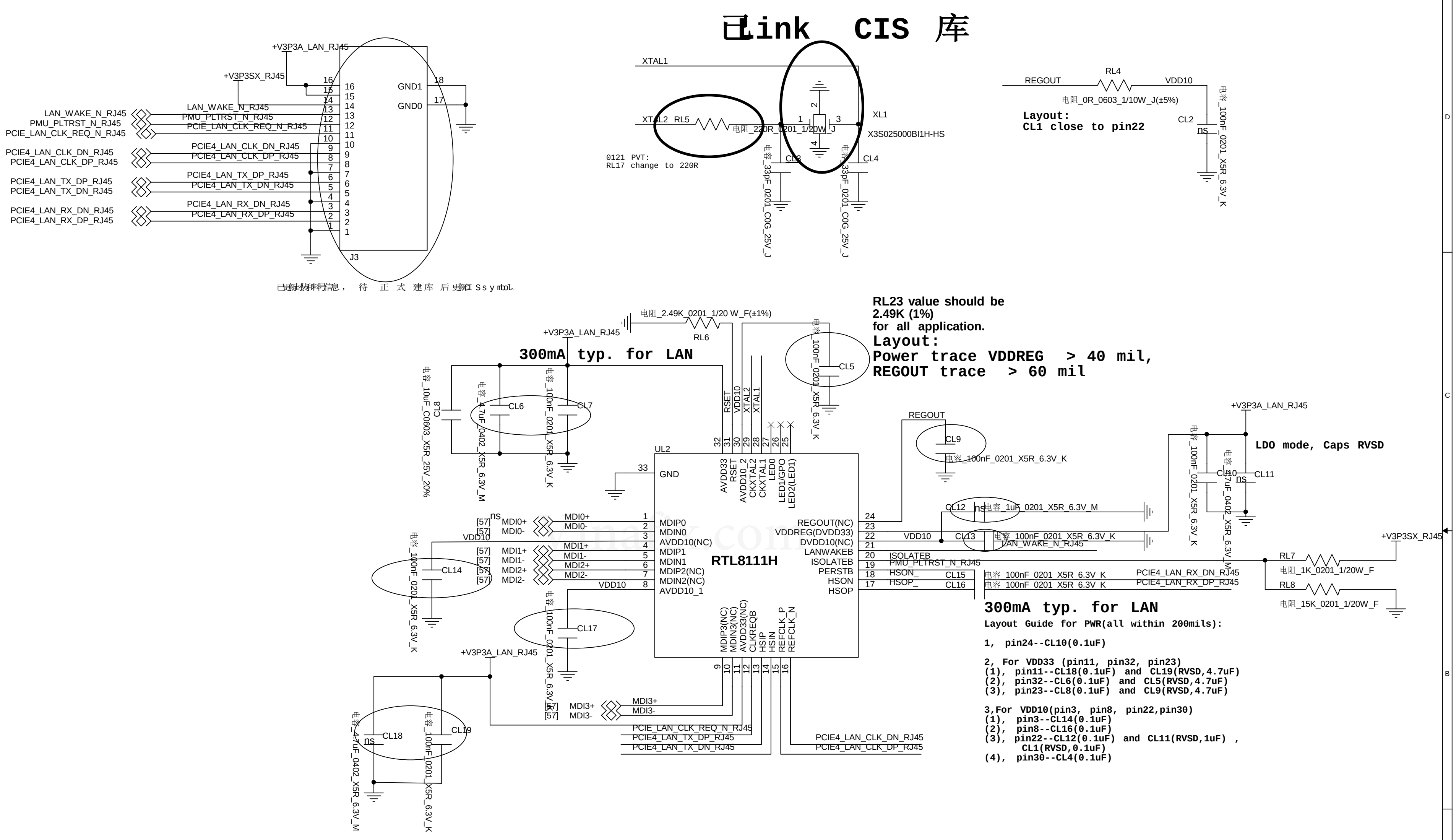


Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>		
PAGE DETAIL	<Doc>		
ID	<OrgAddr3>	Size	Custom
Date	Monday, December 16, 2019	Sheet	54 of 59

		INTEL_SPEC			EC setting		
Function	Net Name	Label	min	max	Label	setting	Note
PWR	+VRTC_SOC						
PCH_IN	RTEST_N	t0	10ms	20ms	t0		
EC_O	PMU_BATLOW_N						
EC_O	PD_SHDN#					1ms	PWR_Switch_EC input Valid to PD_SHDN# high
EC_O	V3P3A_EN				ct0	2ms	PWR_Switch_EC input Valid to V3P3A_EN high
PWR	+V3P3AS+V3P3A_SOC					NA	
VR_O	V3P3A_PGOOD					NA	
EC_O	EC_VSP0A_EN				ct0	2ms	PWR_Switch_EC input Valid to EC_VSP0A_EN high
EC_I	PWR_Switch_EC					50ms	ON/OFF de-bance min 50ms
EC_O	SOC_PMU_PWRBTN_N				ct1	100ms	Minimum duration of RSMRST_N_PMU assertion = 100mS
EC_O	PMU_EN				ct2	20ms	PMU_EN to EC_VSP0A_EN high
PMIC_OUT	+V1P8A					NA	
PMIC_OUT	+V1P2A					NA	
PCH_OUT	PMU_THERMTRIP_N					NA	
EC_I	RSMRST_N_PMU					NA	
EC_O	RSMRST_N_SOC		10	no requirement	ct3	2ms	RSMRST_N_PMU high to RSMRST_N_SOC
PCH_OUT	PMU_SUSCLK						
PCH_OUT	PMU_SLP_S4_N						
PCH_OUT	PMU_SLP_S3_N						
EC_OUT	EC_SLP_SX				ct4	0ms	EC_SLP_SX high to PMU_SLP_S3_N low
PCH_OUT	PMU_SLP_S0_N						
VR_O	+V0P6S						
PMIC_O	+VLP05S						
VR_O	+VCCI						
EC_I	PCH_PWROK_PMU						
EC_OUT	PCH_PWROK_SOC		5	no requirement	ct5	2ms	PCH_PWROK_PMU high to PCH_PWROK_SOC high
PCH_OUT	PMIC_RST						
PCH_OUT	PMU_SUS_STAT_N						
PCH_OUT	SOC_PMU_PLTRST_N						



Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	Custom
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	55 of 59



300mA typ. for LAN

Layout Guide for PWR(all within 200mils):

1, pin24--CL10(0.1uF)

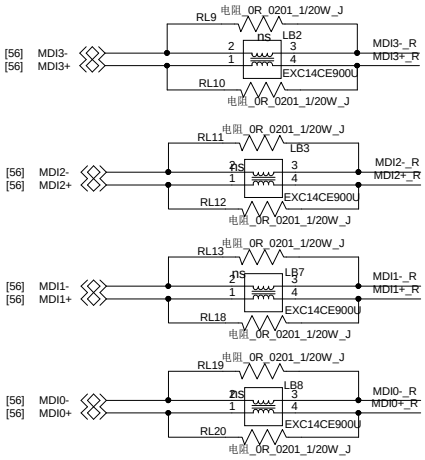
2, For VDD33 (pin11, pin32, pin23)
(1), pin11--CL18(0.1uF) and CL19(RVSD,4.7uF)
(2), pin32--CL6(0.1uF) and CL5(RVSD,4.7uF)
(3), pin23--CL8(0.1uF) and CL9(RVSD,4.7uF)

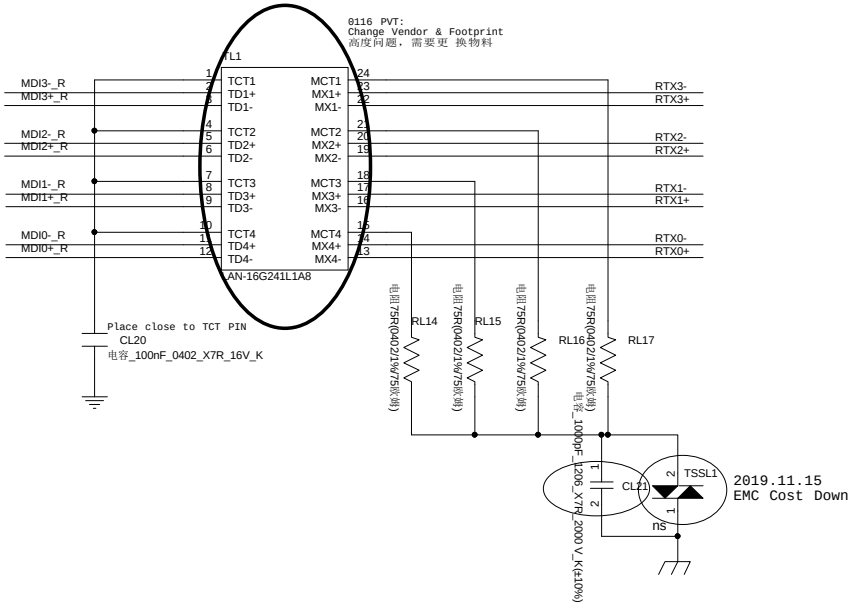
3,For VDD10(pin3, pin8, pin22,pin30)
(1), pin3--CL14(0.1uF)
(2), pin8--CL16(0.1uF)
(3), pin22--CL12(0.1uF) and CL11(RVSD,1uF) ,
CL1(RVSD,0.1uF)
(4), pin30--CL4(0.1uF)

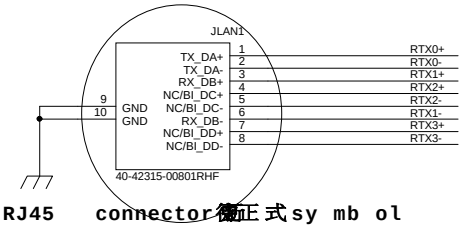
0120 PVT:
pull up power change to +3P3A

		Huaqin Telecom Technology Com.,Ltd.			
		HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	<OrgAddr3>	Size	A3
PAGE DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet	56 of 59

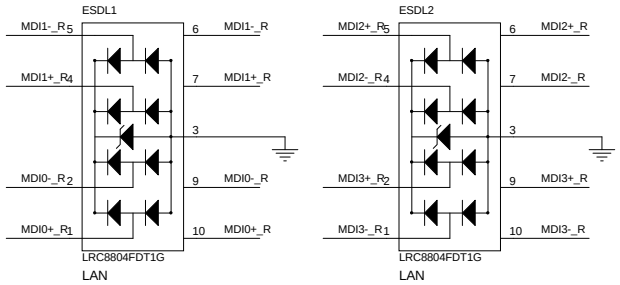
RJ45

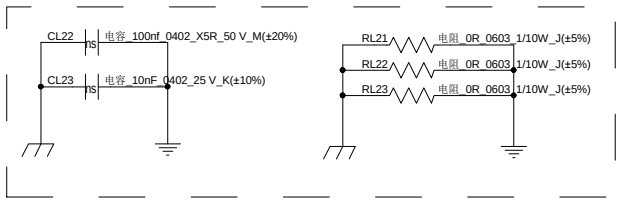


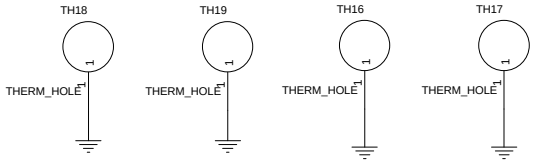




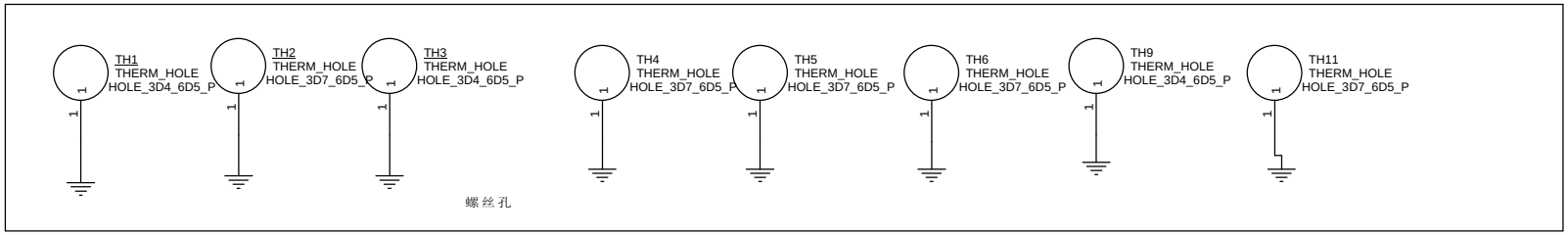
RJ45 connector官正式sy mb ol

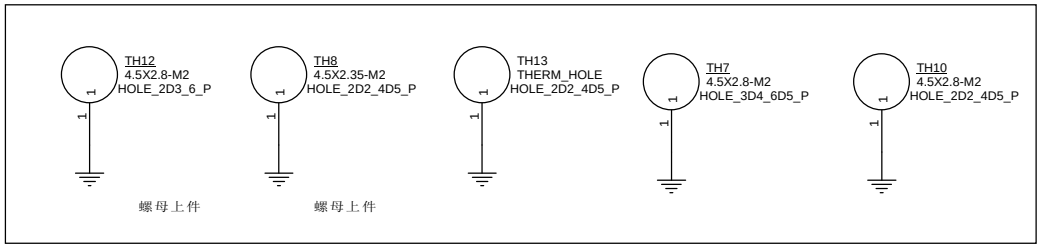


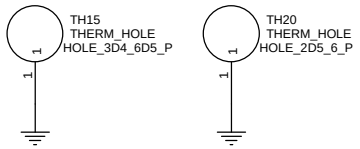




Huaqin Telecom Technology Com.,Ltd.			
HQNBD	NB2372	Rev	V1.0
TITLE <OrgAddr4>	ID <OrgAddr3>	Size	A3
PAGE_DETAIL <Doc>	Date Monday, December 16, 2019	Sheet	57 of 59







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		HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	<OrgAddr3>	Size	B
PAGE_DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet	58 of 59

1.Add Battery SMBUS test point,PT603,PT604.----20180131

2.JHDD1 PIN4&PIN5 NC.----20180131

3.Memory ID table order from ID0,ID1,ID2 to ID2,ID1,ID0--20180202

4.P39 删除LAN线路， 增加RJ45 _ UB_CONN 2 1 5

		Huaqin Telecom Technology Com.,Ltd.		
	HQNBD	NB2372	Rev	V1.0
TITLE	<OrgAddr4>	ID	<OrgAddr3>	Size B
PAGE DETAIL	<Doc>	Date	Monday, December 16, 2019	Sheet 59 of 59